Compal Confidential

TESLA 3A
DIS M/B Schematics Document

Intel Broadwell U Processor with DDR3L
Nvidia N16V-GM(920M)

2014-09-26

LA-C311P

REV：0.1

Compal Electronics, Inc.		
Title: Cover Page		
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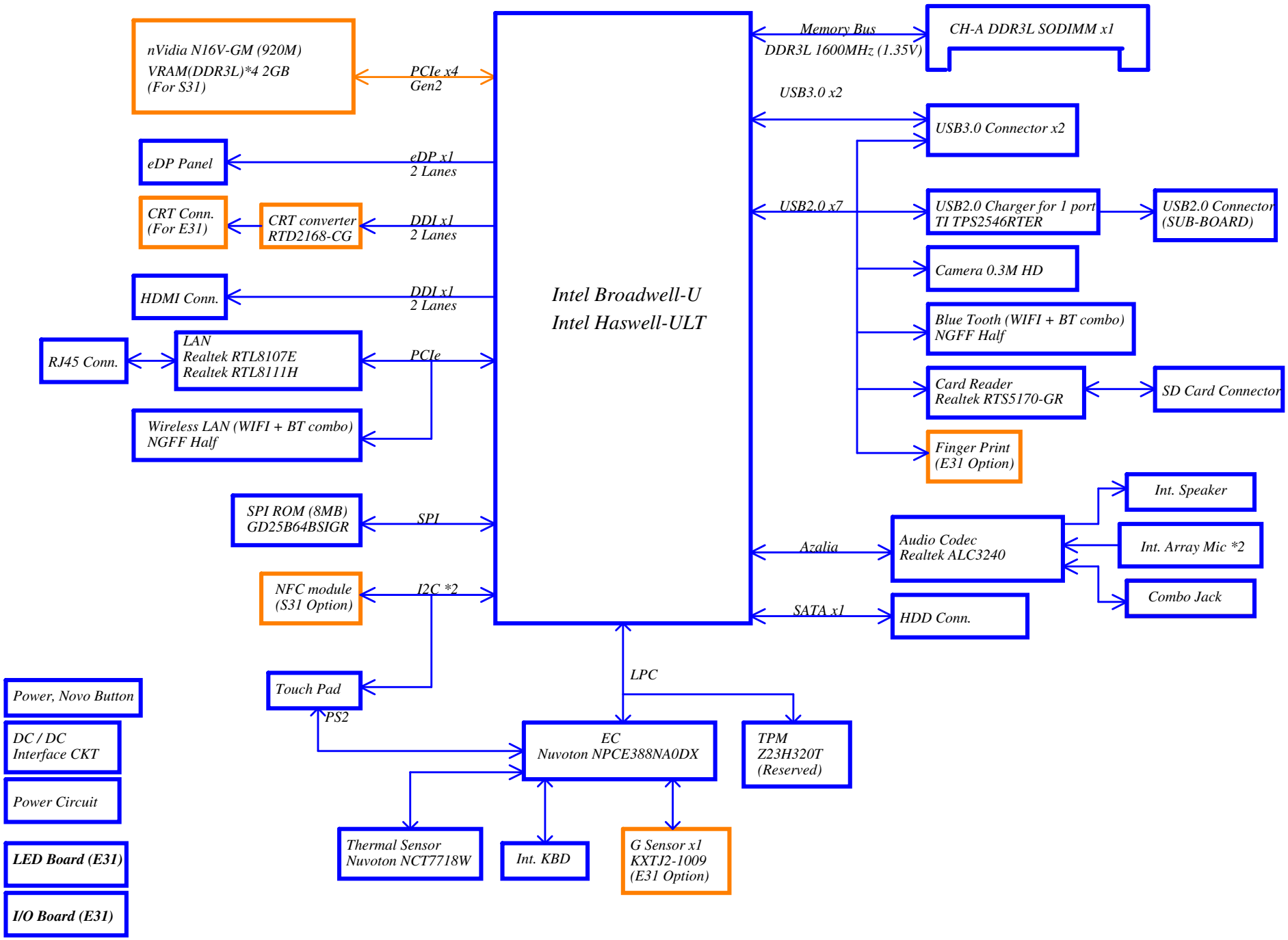

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Title: **MB Block Diagram**

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port USB3.0
		1	USB Port USB3.0
	UHCI1	2	
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	NGFF(BT)
		9	USB Port (Charge)
	UHCI5	10	NGFF(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure
LAN 10/100 Transformer	100@
LAN GIGA Transformer	GIGA@
LAN RTL8111H	8111H@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@
For Green CLK	GCLK@
For No Green CLK	NoGCLK@
For DIS	DIS@
For TPM	TPM@
For Camera	CMOS@
For NFC Option	NFC@
For ST APS	GSST@
For Bosch APS	GSB@
For E31 PWR Button ESD	@E31ESD@
For FP Option	FP@
For Green clock with DIS	GCLKDIS@
For Green clock with UMA	GCLKUMA@
For U31 Option	U31@
For E31 Option	E31@
Connector	ME@
No EMI	@EMI@
No ESD	@ESD@
For Hynix Memory	H2G@
For Samsung Memory	S2G@
For Micron Memory	M2G@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h
BMA250E	0001 100X 18h

ME SM Bus address

Device	Address
NFC	0010 1000 28h

PCH SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
Touch Pad	

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SIGNAL / STATE	SCD&UE	VGA	BATT	NEULESS	SODIMM	WLAN	Thermal	DGPU	NFC	TP	TPM
SMBus_THERM_DAT	NEULESS	+3VALW									
SMBus_THERM_CLK	NEULESS	+3VALW									
SMBus_BAT_DAT	TPM										
SMBus_BAT_CLK	TPM										
SMBus_DGPU_DAT	TPM										
SMBus_DGPU_CLK	TPM										

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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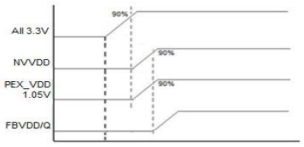
GPU Power Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.

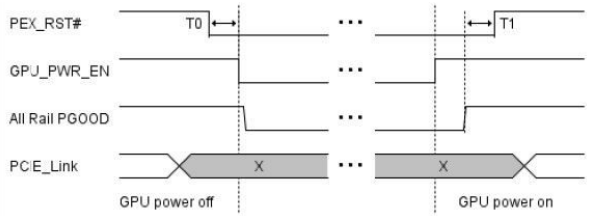


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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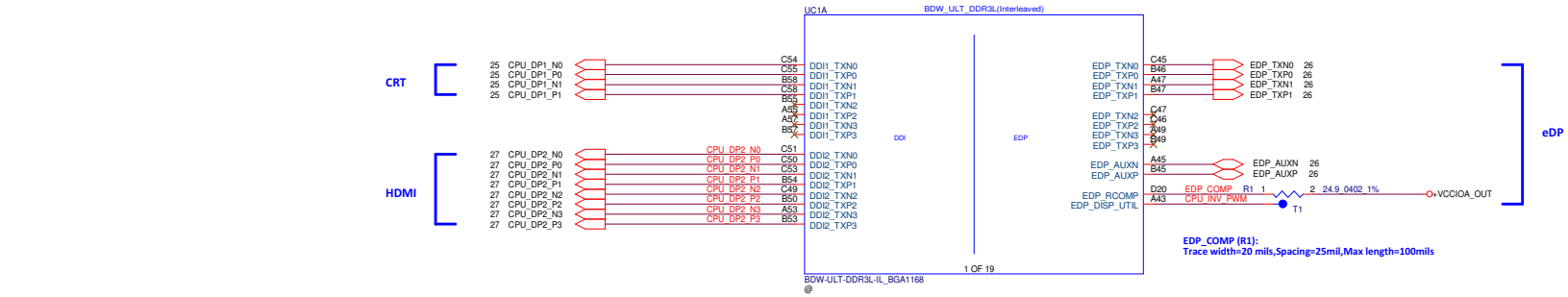

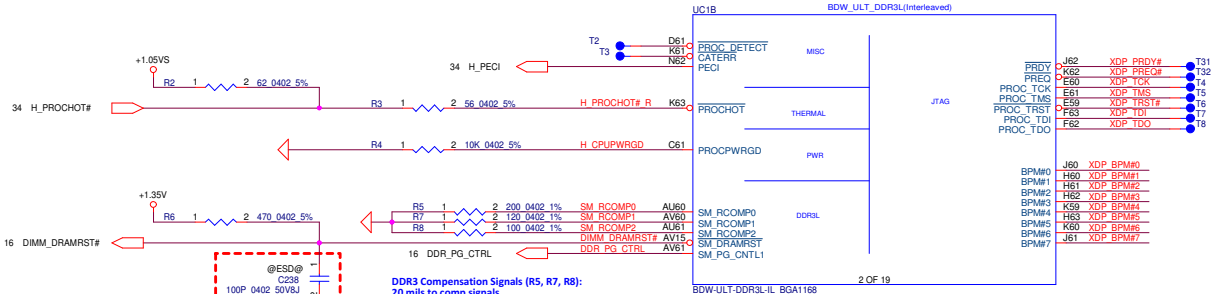

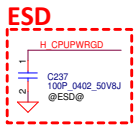

UC1
SA00007M750
S IC CL8064701477301 QEAF D0 2G BGA C38
i7_4510U@

UC1
SA00007LO10
S IC CL8064701477802 QEAK D0 1.7G BGA
i5_4210U@

UC1
SA00007TX10
S IC CL8064701553300 QEZA D0 2G BGA 1168
i3_4120U@

UC1
SA00007TA10
S IC CL8064701552900 QEZ6 D0 1.9G BGA
i3_4030U@

UC1
SA00007TW10
S IC CL8064701553401 QEZB D0 1.9G C38
i3_4025U@

UC1
SA00007G030
Intel 2957U 1.4G 2M D0 2cBGA CPU
2957U@

UC1
SA00007G230
S IC CL8064701569500 QFAN D0 1.7G BGA
3558U@

UC1
SA00006SLA0
S IC CL8064701477202 QEVD C0 1.8G BGA
i7_4500U@

UC1
SA00006SMC0
S IC CL8064701477702 SR170 C0 1.6G C38!
i5_4200U@

UC1
SA00007AM00
S IC CL8064701614813 QFSY C0 1.6G BGA
QFSY@

UC1
SA00006SU30
S IC CL8064701476302 SR16P C0 1.8G C38!
i3_4100U@

UC1
SA00007Q50
S IC CL8064701478404 QEAR D0 1.7G C38
i3_4005U@

UC1
SA00006SX80
S IC CL8064701478202 SR16Q C0 1.7G C38!
i3_4010U@

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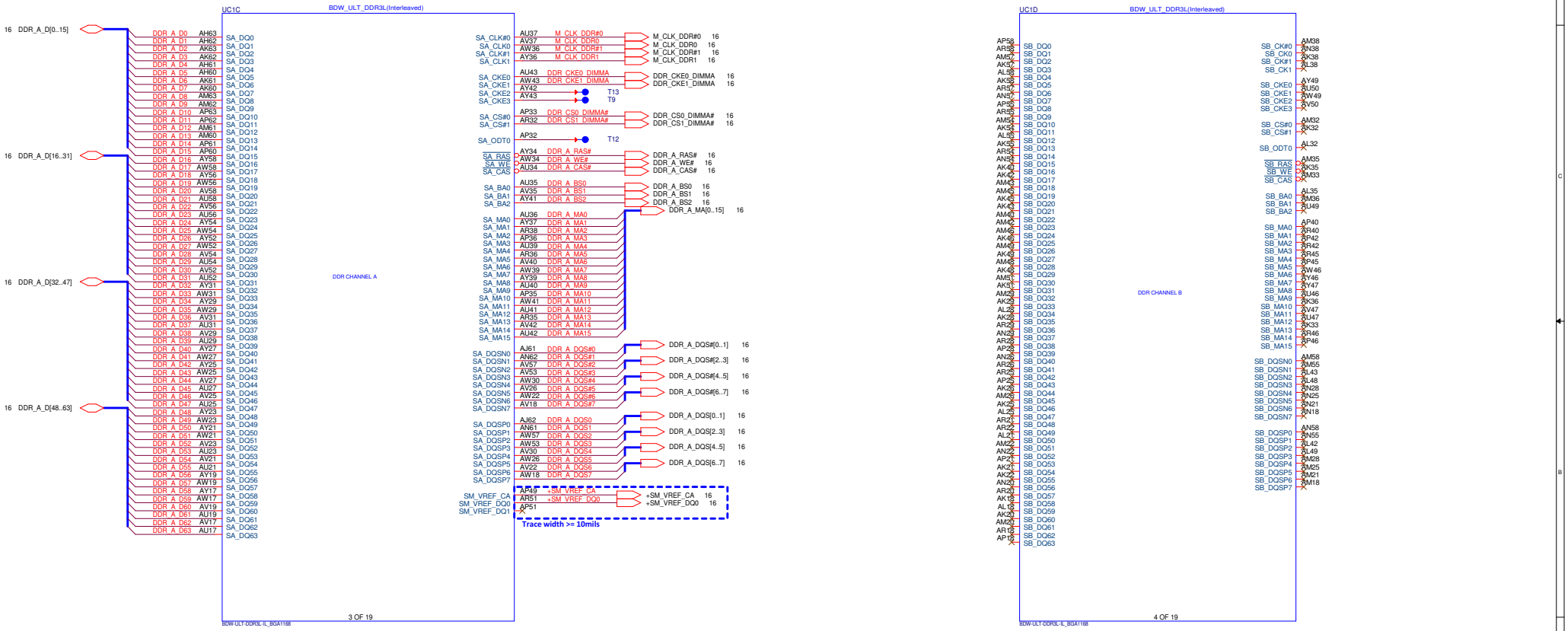
Interleaved Memory



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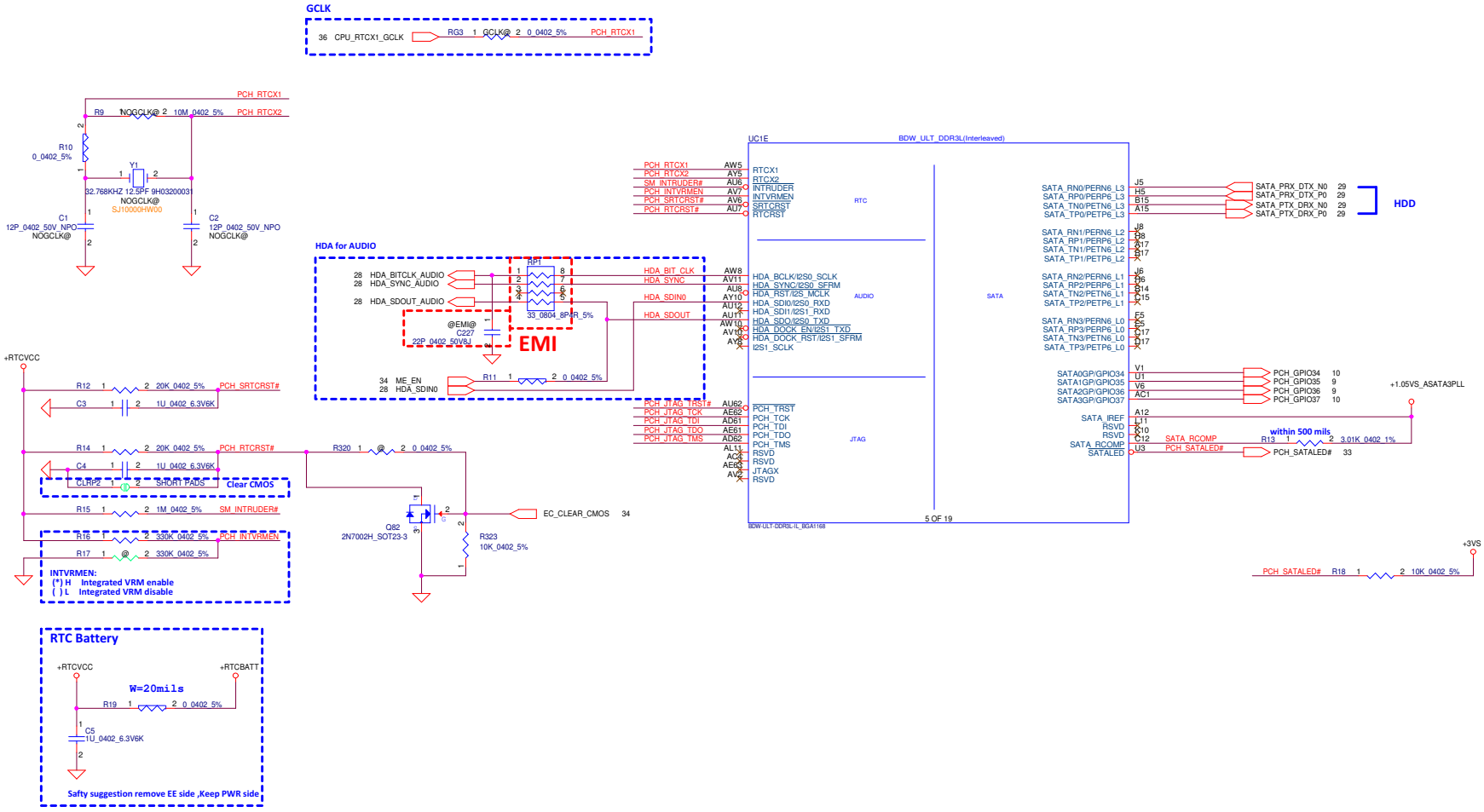

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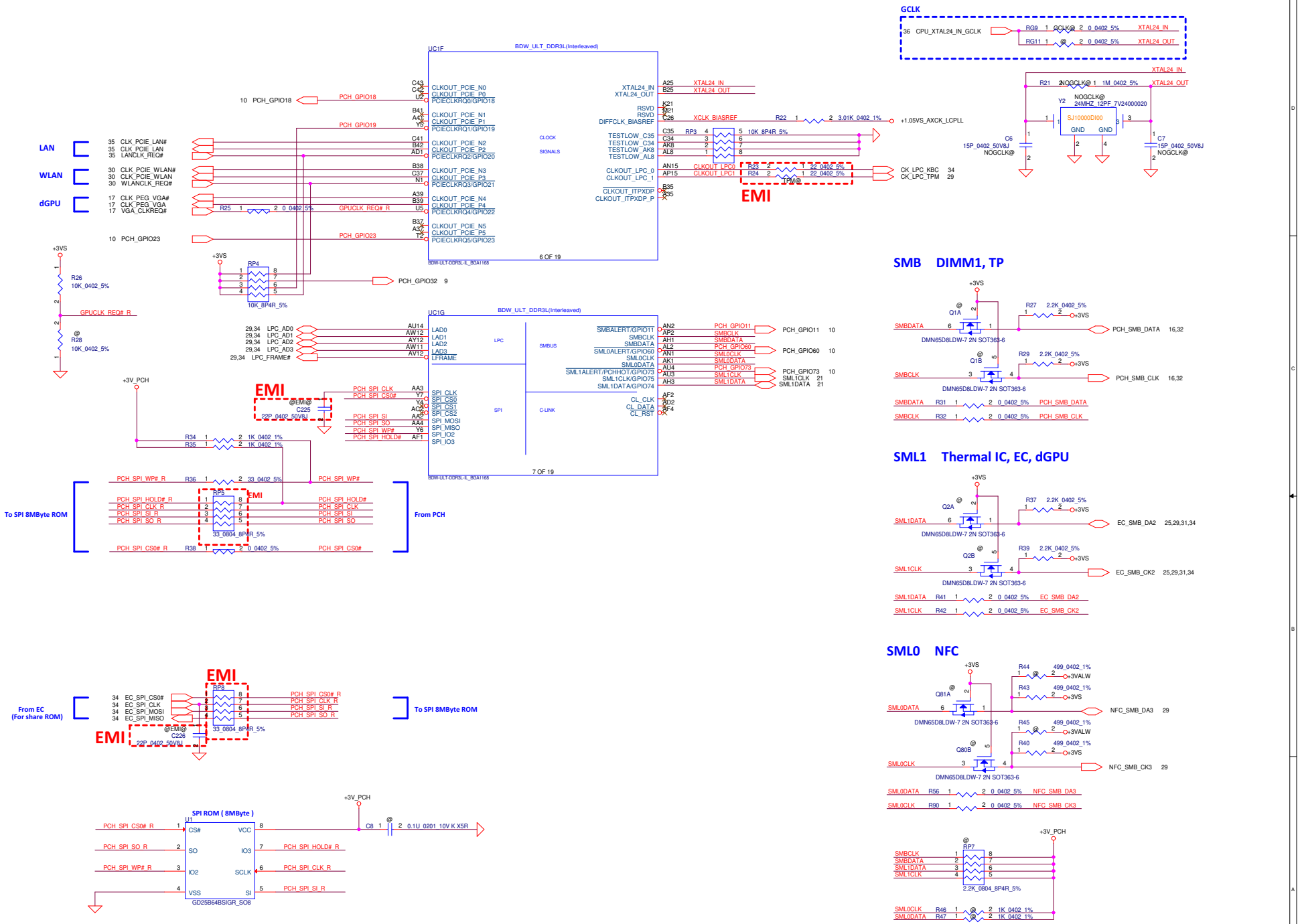

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ESD

SYS_PWROK — @ESD@ C239 100P_0402_50V8J
EC_RSMRST# — @ESD@ C240 100P_0402_50V8J
PCH_PWROK — @ESD@ C242 100P_0402_50V8J
SYS_RESET# — @ESD@ C243 100P_0402_50V8J

DSWODVREN - On Die DSW VR Enable
(*) H Enable(DEFAULT)
( ) L Disable

+RTCVCC
R49 330K_0402_5%
R50 330K_0402_5%

+3VALW
R54 10K_0402_5%
AC_PRESENT

UC1H — BDW_ULT_DDR3L(Interleaved)
SYSTEM POWER MANAGEMENT
8 OF 19
BDW-ULT-DDR3L-IL_BGA1168

41 SUSACK#
10 SYS_RESET#
34 SYS_PWROK
34 PCH_PWROK
R51 0_0402_5%
R55 0_0402_5%
SUSACK# R — AK2 SUSACK
SYS_RESET# — AC3 SYS_RESET#
SYS_PWROK — AG2 SYS_PWROK
PCH_PWROK — AY7 PCH_PWROK
APWROK_R — AB5 APWROK
CPU_PLT_RST# — AG7 PLTRST

34 EC_RSMRST#
34 PBTN_OUT#
EC_RSMRST# — AW6 RSMRST
PCH_GPIO30 — AV4 SUSWARN/SUSPWRDNACK/GPIO30
PBTN_OUT# — AL7 PWRBTN
AC_PRESENT — AJ8 ACPRESENT/GPIO31
PCH_GPIO72 — AN4 BATLOW/GPIO72
T15 @ — AF3 SLP_S0
PCH_GPIO29 — AM5 SLP_WLAN/GPIO29

DSWVRMEN — AW7 DSWODVREN
DPWROK — AV5 PCH_DPWROK
WAKE — AJ5
PCH_PCIE_WAKE# — R53 0_0402_5% EC_RSMRST#; R57 100K_0402_5%; R58 0_0402_5%
PCIE_WAKE# 30,34,35

CLKRUN/GPIO32 — V5 PCH_GPIO32 — PCH_GPIO32 8
SUS_STAT/GPIO61 — AG4 — LPC_PD# 29
SUSCLK/GPIO62 — AE6 SUSCLK — SUSCLK 30
SLP_S5/GPIO63 — AP5 PM_SLP_S5# — PM_SLP_S5# 34
SLP_S4 — AJ6 PM_SLP_S4# — PM_SLP_S4# 34
SLP_S3 — AT4 PM_SLP_S3# — PM_SLP_S3# 34
SLP_A — AL5
SLP_SUS — AP4
SLP_LAN — AJ7

+3VS
R107 10K_0402_5% — PCH_GPIO36 7
RP10 10K_8P4R_5%
R52 0_0402_5% — GS_INT2 29; SERIRQ — SERIRQ 10,29,34
TPMPD# — TPMPD# 10; PCH_GPIO35 7
RP12 10K_8P4R_5%
PCH_GPIO68 — PCH_GPIO68 10
DGPU_PWROK — PCH_GPIO55 — PCH_GPIO52
R61 2.2K_0402_5% — DDI1_CTRL_CK
R62 2.2K_0402_5% — DDI1_CTRL_DATA

R59 0_0402_5%
CPU_PLT_RST#
U3 U74AHC1G08G-AL5-R_SOT353-5
R60 100K_0402_5%
PCI_RST# 17,29,30,34,35

UC1I — BDW_ULT_DDR3L(Interleaved)
DISPLAY
9 OF 19
BDW-ULT-DDR3L-IL_BGA1168

+3V_PCH
R64 10K_0402_5% — PCH_GPIO30
R65 10K_0402_5% — PCH_GPIO72

+3VALW
R66 10K_0402_5% — PCH_GPIO29
R67 1K_0402_5% — PCH_PCIE_WAKE#

+3VGS +3VS
R223 10K_0402_5% — DGPU_PWR_EN
R224 10K_0402_5%

+3VGS +3VS
R225 10K_0402_5% — DGPU_HOLD_RST#
R226 10K_0402_5%

26 INVPWM
26,34 ENBKL
26 PCH_ENVDD
R63 0_0402_5% — EDP_BKCTL
EDP_BKLCTL — B8
EDP_BKLEN — A9
EDP_VDDEN — C6
eDP SIDEBAND

17,20,47 DGPU_PWROK
20,34,47 DGPU_PWR_EN
17 DGPU_HOLD_RST#
10,30 WLBT_OFF#
T16 @
PIRQA/GPIO77 — U6
PIRQB/GPIO78 — P4
PIRQC/GPIO79 — N4
PIRQD/GPIO80 — N2
PME — AD4
PCIE

PCH_GPIO55 — U7 GPIO55
PCH_GPIO52 — L1 GPIO52
PCH_GPIO54 — L3 GPIO54
PCH_GPIO51 — R5 GPIO51
PCH_GPIO53 — L4 GPIO53
10 PCH_GPIO54
10 PCH_GPIO51
10 PCH_GPIO53

DDPB_CTRLCLK — B9 DDI1_CTRL_CK
DDPB_CTRLDATA — C9 DDI1_CTRL_DATA
DDPC_CTRLCLK — D9 HDMICLK_NB 27
DDPC_CTRLDATA — D11 HDMIDAT_NB 27
HDMI DDC (Port C)

DDPB_AUXN — C5 DDI1_AUX_DN — DDI1_AUX_DN 25 — DP Aux (Port B for VGA)
DDPB_AUXP — B5 DDI1_AUX_DP — DDI1_AUX_DP 25 — DP Aux (Port B for VGA)
DDPC_AUXN — B6
DDPC_AUXP — A6

DDPB_HPD — C8
DDPC_HPD — A8 DDPC_HPD R148 0_0402_5% — DDI1_HPD 25; TMDS_B_HPD 27; EDP_HPD 26
EDP_HPD — D6
From VGA Trans.
From HDMI
From eDP

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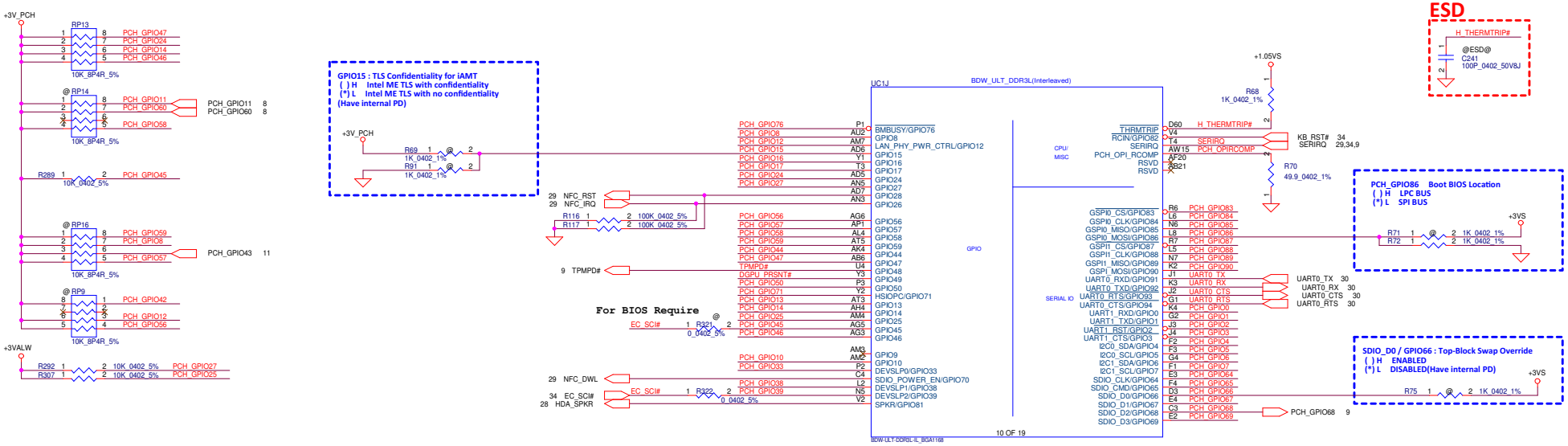

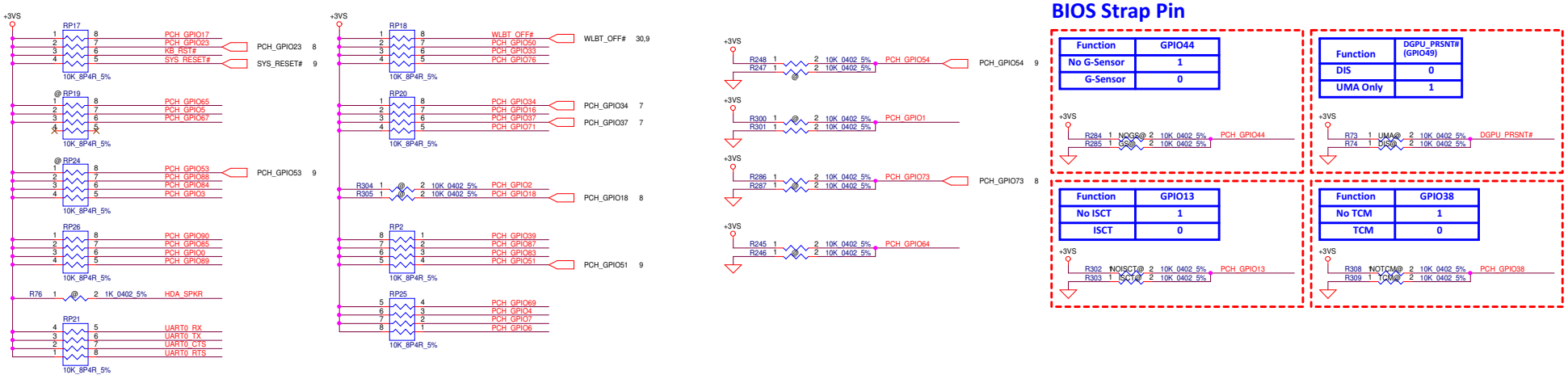

Platfrom	RP21
Broadwell	10K
Skylake	50K

BIOS Strap Pin

Function	GPIO44
No G-Sensor	1
G-Sensor	0

+3VS R284 1 NOGS@ 2 10K_0402_5% PCH_GPIO44
R285 1 GS@ 2 10K_0402_5%

Function	DGPU_PRSNT# (GPIO49)
DIS	0
UMA Only	1

+3VS R73 1 UMA@ 2 10K_0402_5% DGPU_PRSNT#
R74 1 DIS@ 2 10K_0402_5%

Function	GPIO13
No ISCT	1
ISCT	0

+3VS R302 1 NOISCT@ 2 10K_0402_5% PCH_GPIO13
R303 1 ISCT@ 2 10K_0402_5%

Function	GPIO38
No TCM	1
TCM	0

+3VS R308 1 NOTCM@ 2 10K_0402_5% PCH_GPIO38
R309 1 TCM@ 2 10K_0402_5%

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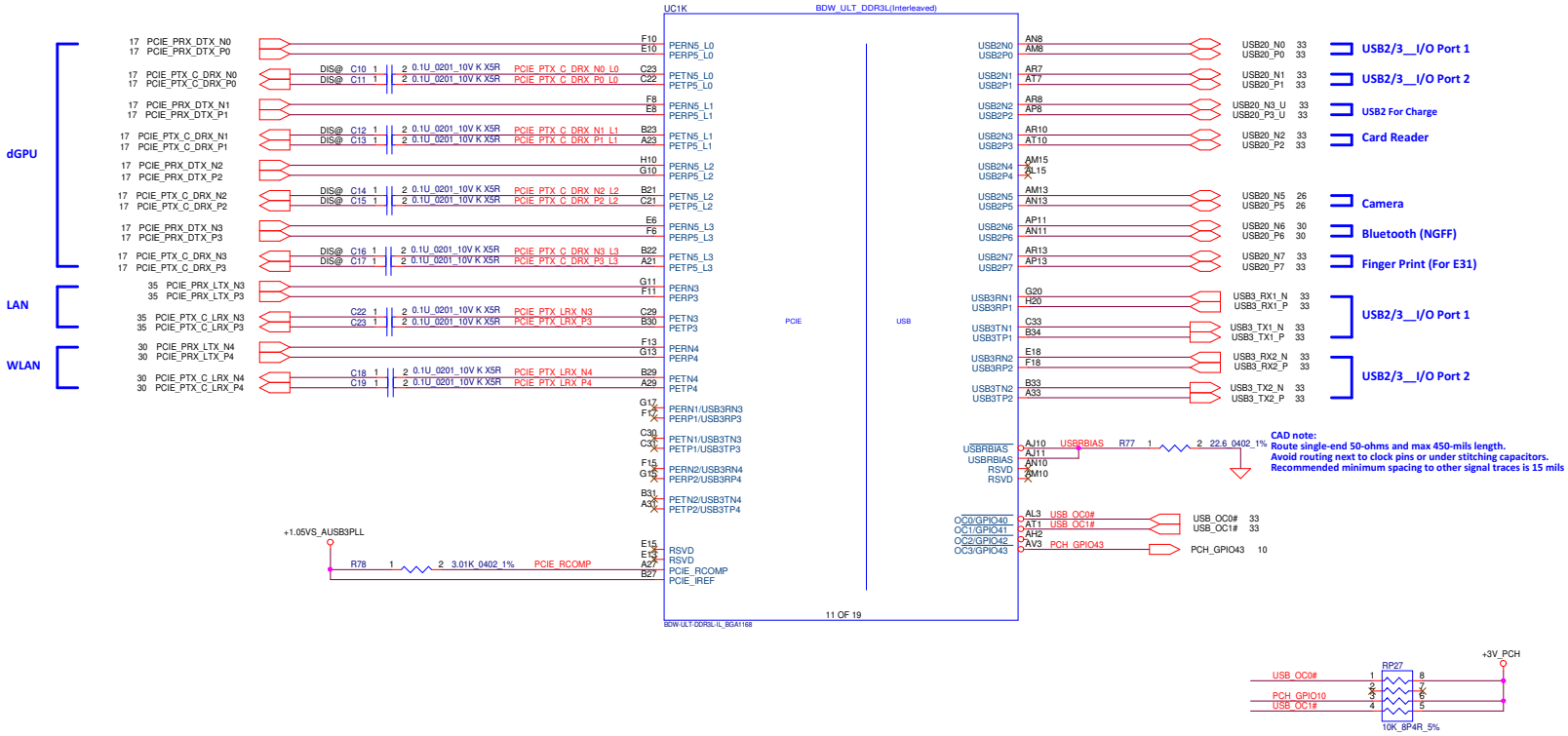

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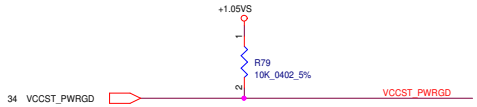

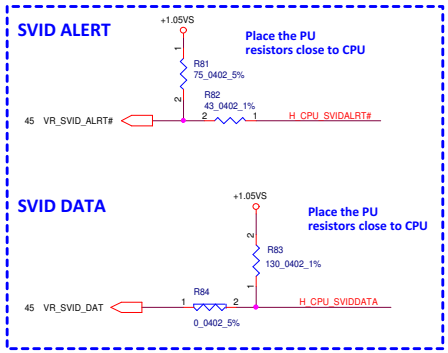

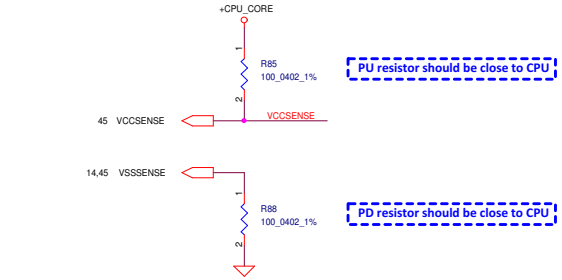

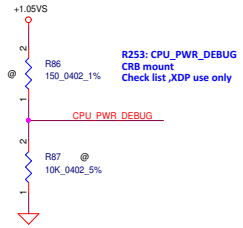

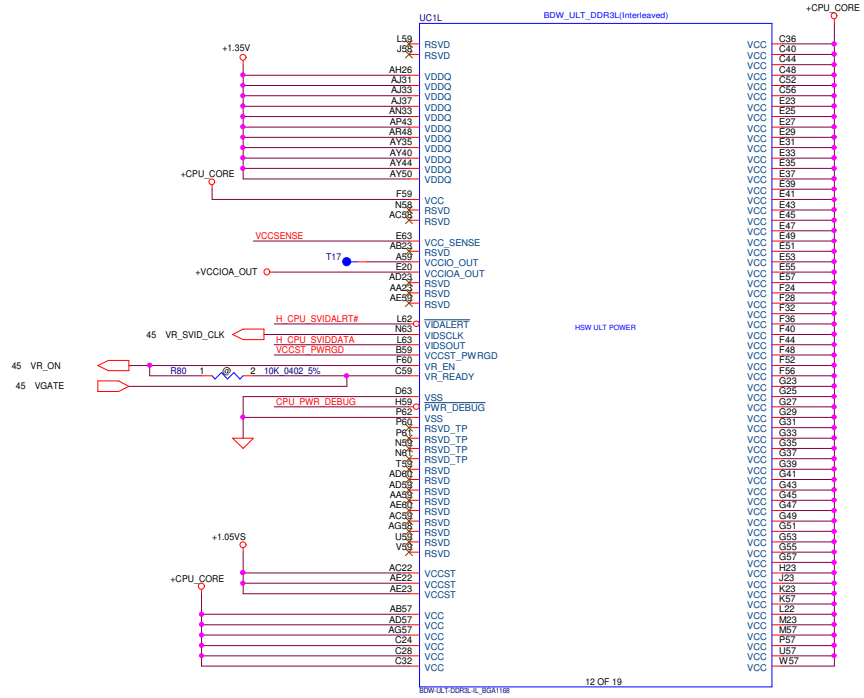

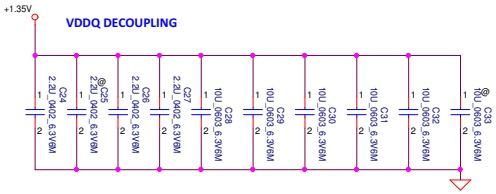

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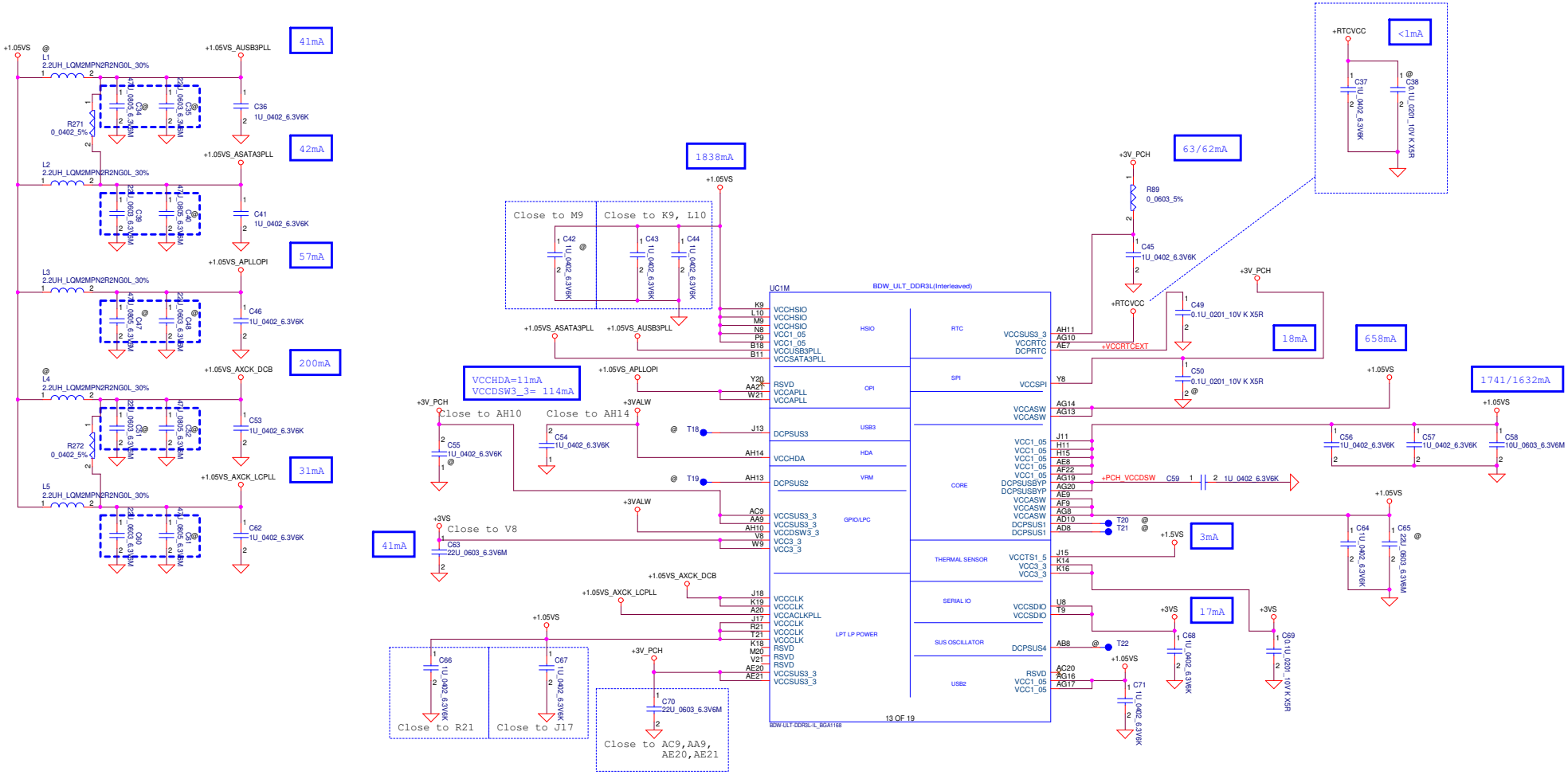

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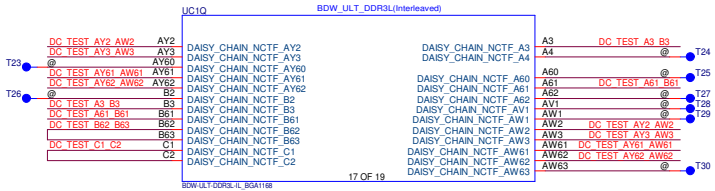
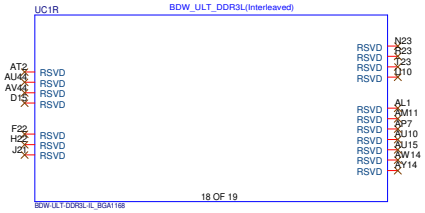
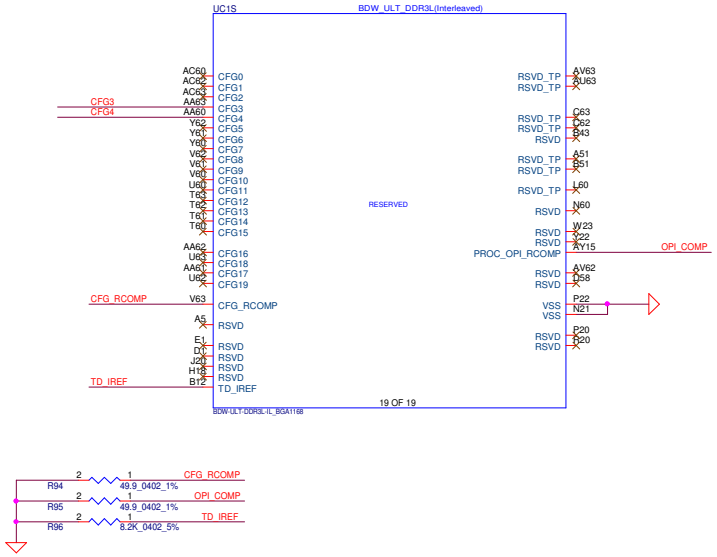
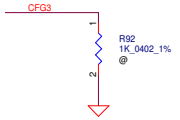


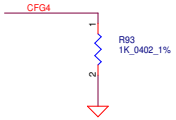




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.			
Title: HSW MCP(11/11) RSVD			
Size: C	Document Number: LA-C311P		Rev: 0.1
Date: Friday, September 26, 2014	Sheet 15 of 48		

DIMM1 Reverse Type Near CPU

D/DQ Signals link to CPU
CMD Signals from CPU
Clock Signals from CPU
CTL Signals from CPU
SMBUS Signals link to CPU

JDIMM1
LCN_DAN06-K4406-0103

ESD

Layout Note: Place near JDIMM1

Layout Note: Place near JDIMM1.203,204

Layout Note: Place near JDIMM1.199

Address : 00

DDR3L SODIMM ODT GENERATION

For ODT & VTT power control

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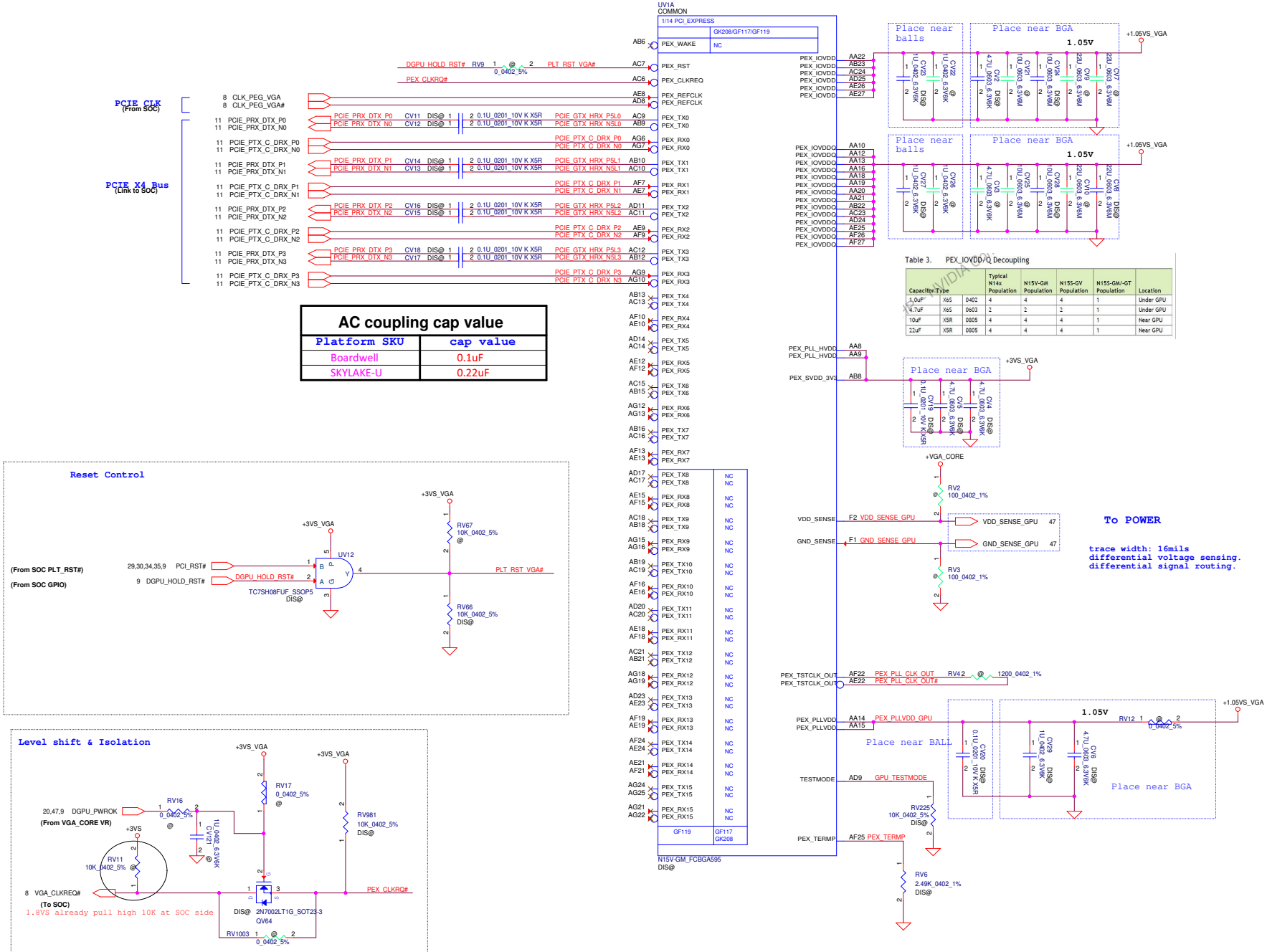
Compal Electronics, Inc.

Title: DDR3L DIMMA

Size: C | Document Number: LA-C311P | Rev: 0.1

Date: Friday, September 26, 2014 | Sheet 16 of 48



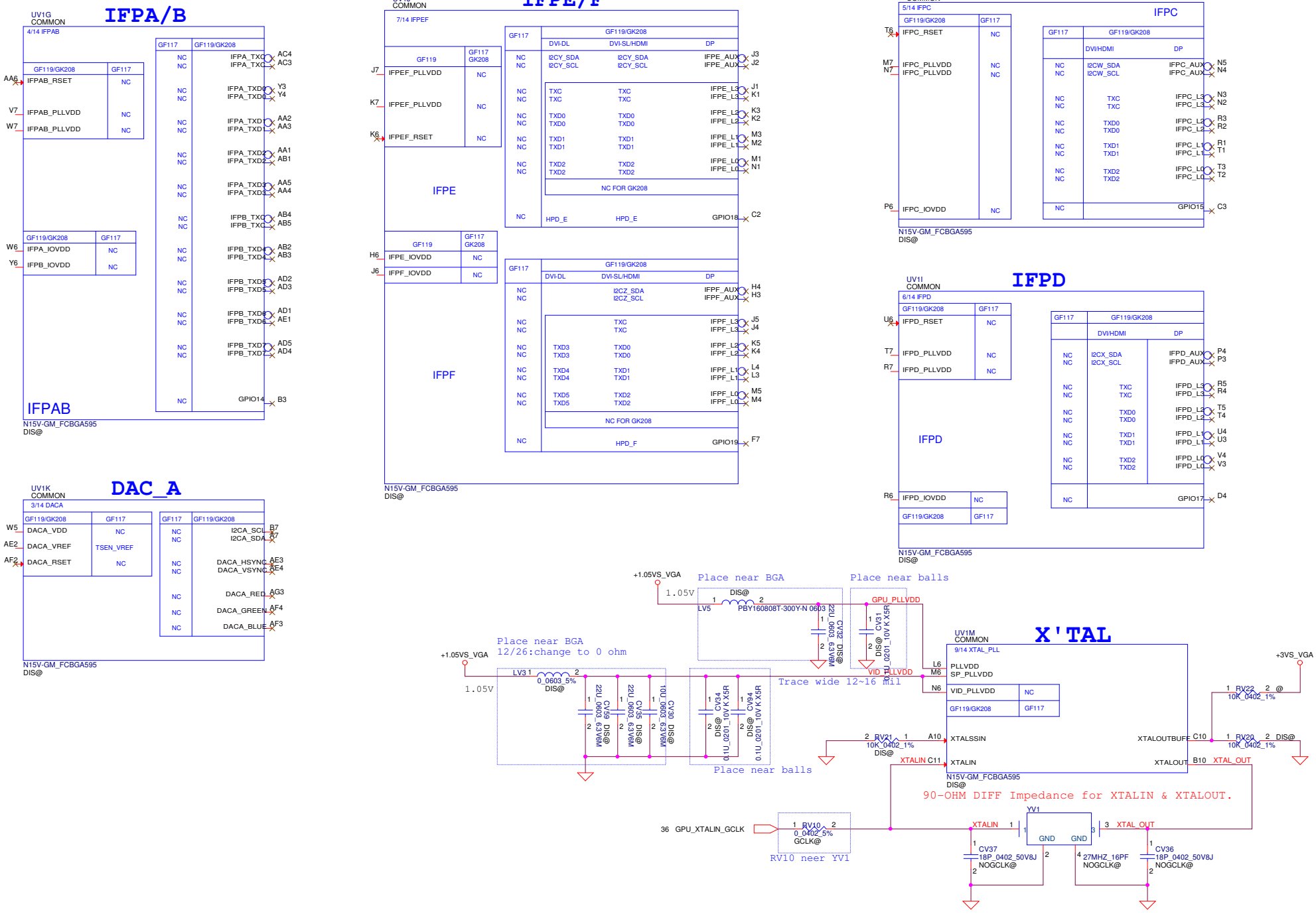
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: NV(1/5)-PCIE

Size: D | Document Number: LA-C311P | Rev: 0.1

Date: Friday, September 26, 2014 | Sheet 17 of 48

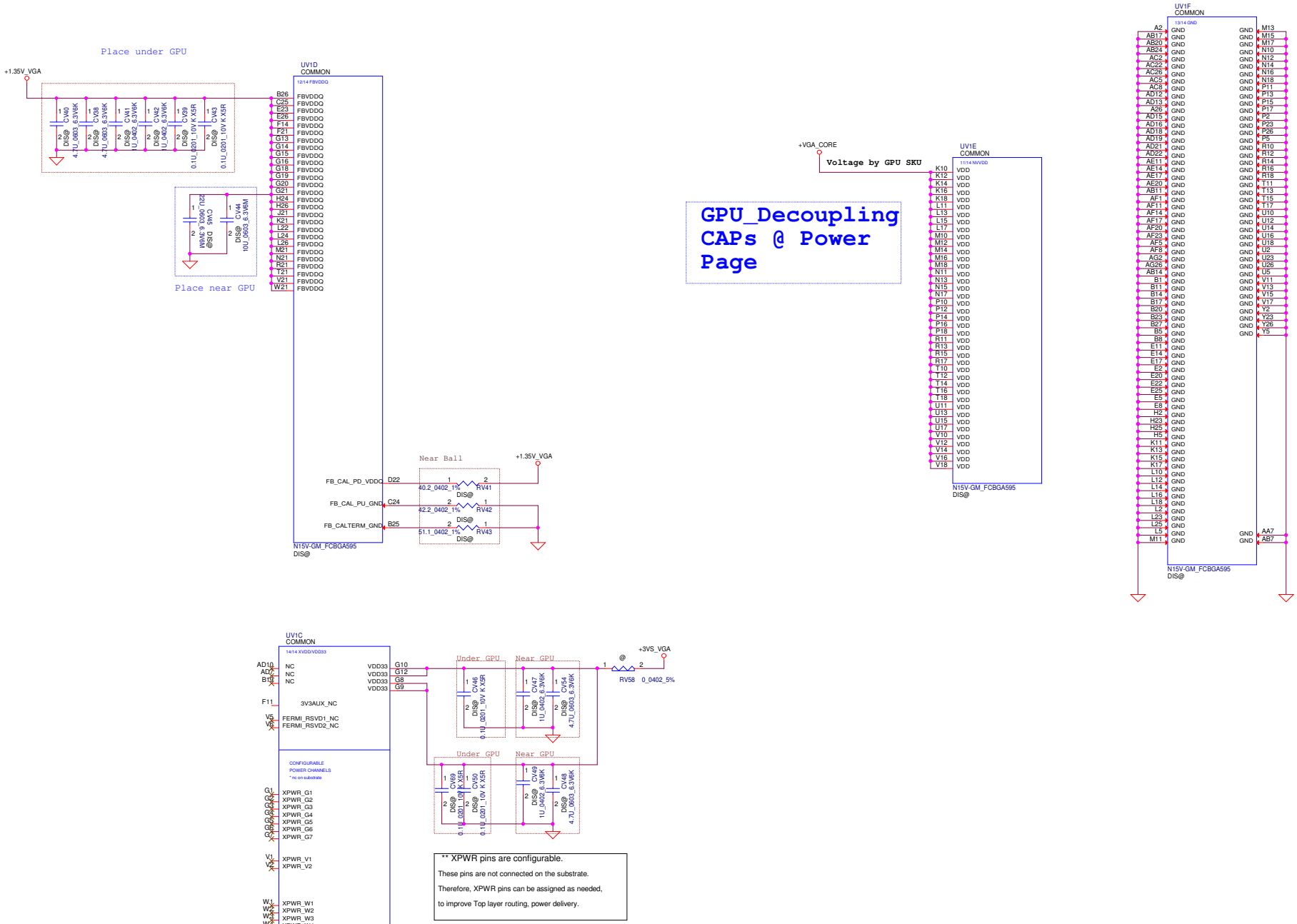


Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **NV(2/5)-IFP ABCDEF DAC XTAL**

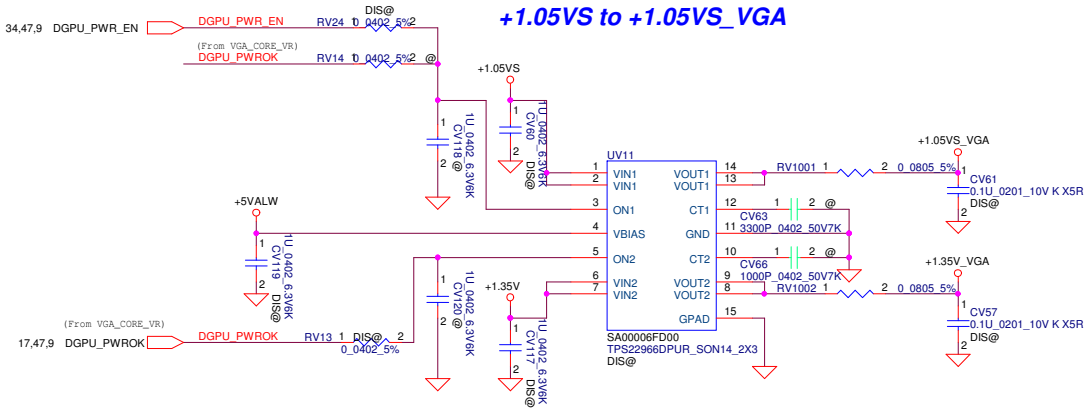
Size: Custom	Document Number: LA-C311P	Rev: 0.1
Date: Friday, September 26, 2014	Sheet 18 of 48	



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

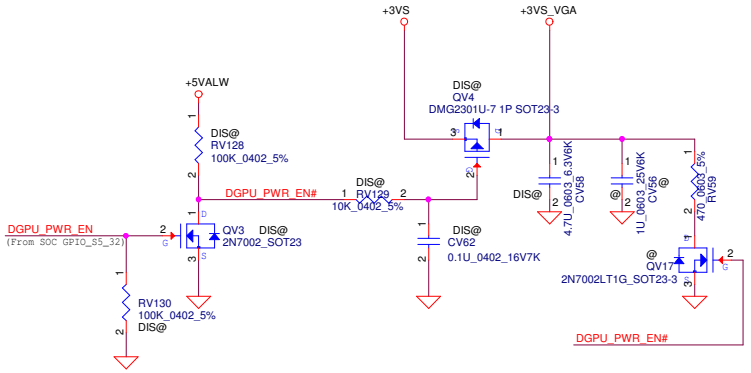
Compal Electronics, Inc.			
Title: NV(3/5)-POWER			
Size: C	Document Number: LA-C311P		Rev: 0.1
Date: Friday, September 26, 2014	Sheet 19 of 48		

+1.05VS to +1.05VS_VGA

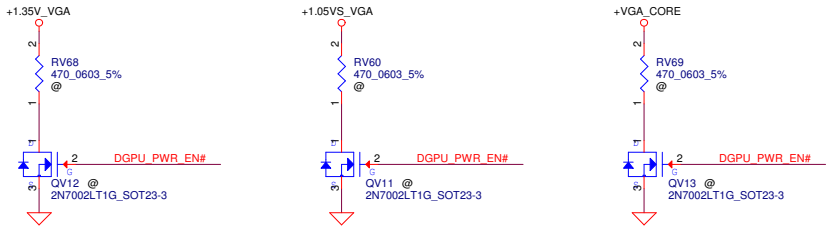


+1.35V to +1.35V_VGA

+3VS to +3VS_VGA

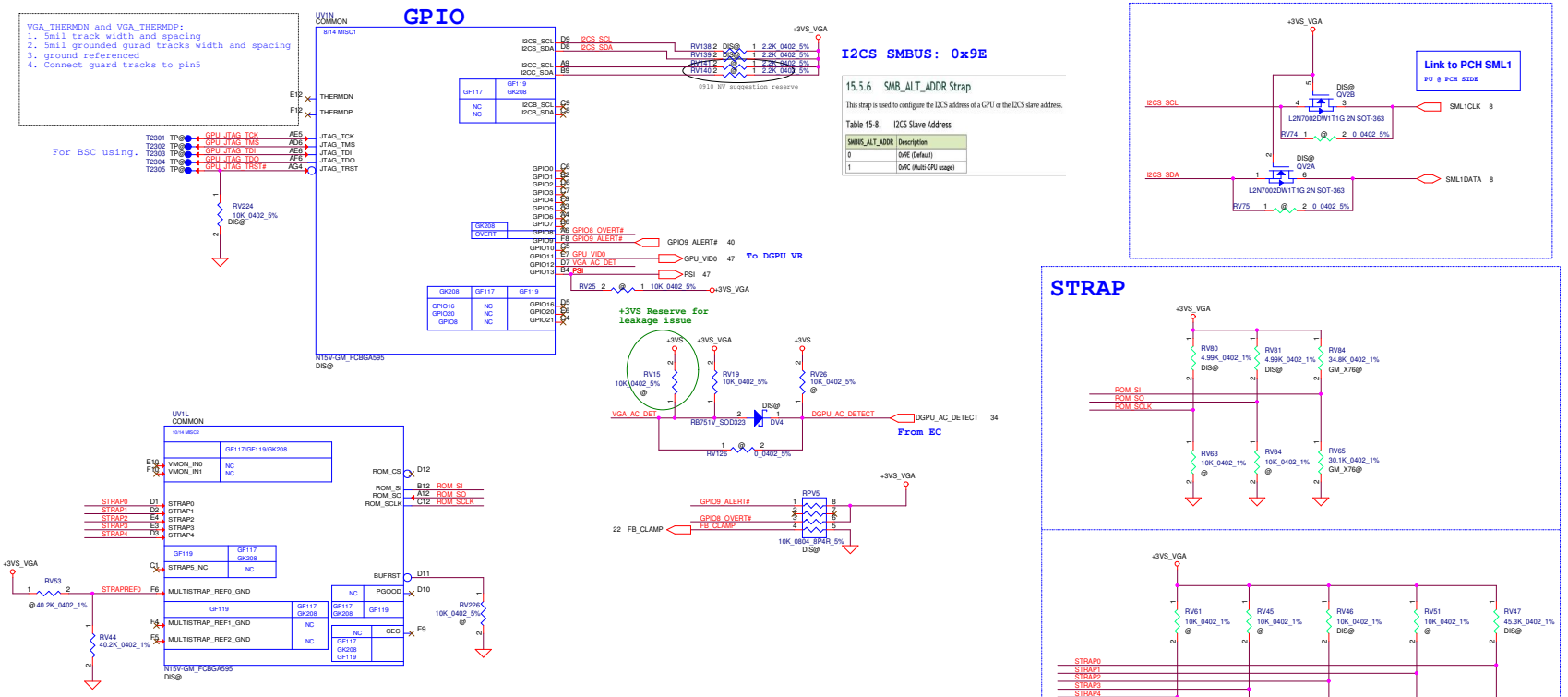


GPU Power Discharge



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.		
Title: DGPU_DC/DC Interface		
Size	Document Number	Rev 0.1
Date: Friday, September 26, 2014	Sheet 20 of 48	



N16V-GM Binary Staps

N16V-GM VRAM Straps: RAM_CFG (3..0) [ROM_SI (3..0)]

GK208s SKU	
Item	N16V-GM-S
Device ID	0X1299
Package	GB2-64
Internal P/N	GK208-620,28nm
ROM_SI	Refer to N16x_RAM_Straps table
ROM_SO	0x8, 5K pull up for Optimus
ROM_SCLK	0x1000,0x8, 4.99Kohm pull up
Strap0	User Strap, 0xF, 45kohm pull up
Strap1	SGIO_PAD_Config, 0x7, 45kohm pull down
Strap2	Device_ID, 0x1001_ 10Kohm pull UP
Strap3	0x0 for Optimus, 5kohm pull low
Strap4	0x0111, 45kohm pull down(PCIE_SPEED_CHANGE=1)
Open_VRG SKU	Config B[PSI not supported]
NVVDD Boot Voltage	0.9V

GPU	VRAM Vendor	Type	F8VDD/ F8VDDQ	Memory Density	Configuration	VRAM P/N	Max Speed CLK	D/C Mini	Die-Revision	RAM_CFG	ROM_SI	Status
N16V-GM-S	DDR3L											
	Hynix	DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	H5TC2G63FFR-11C	900Mhz	NA	F-Die	0x8	PU 20K	Production ready
	Micron	DDR3L	1.35V/ 1.35V	128Mx16		MT41J128M16JT-093G:K	900Mhz	1322	K-Die	0x8	PU 4.99K	Production ready
	Samsung	DDR3L	1.35V/ 1.35V	128Mx16		K4W2G1646Q-BC1A	900Mhz	NA	Q-die	0x7	PD 45.3K	Production ready
	Hynix	DDR3L	1.35V/ 1.35V	256Mx16		H5TC4G63AFR-11C	900Mhz	NA	A-Die	0xE	PU 34.8K	Production ready
	Micron	DDR3L	1.35V/ 1.35V	256Mx16		MT41J256M16HA-093G:E	900Mhz	NA	E-die	0xD	PU 30.1K	Production ready
	Samsung	DDR3L	1.35V/ 1.35V	256Mx16		K4W4G1646D-BC1A	900Mhz	NA	D-Die	0x5	PD 30.1K	Production ready

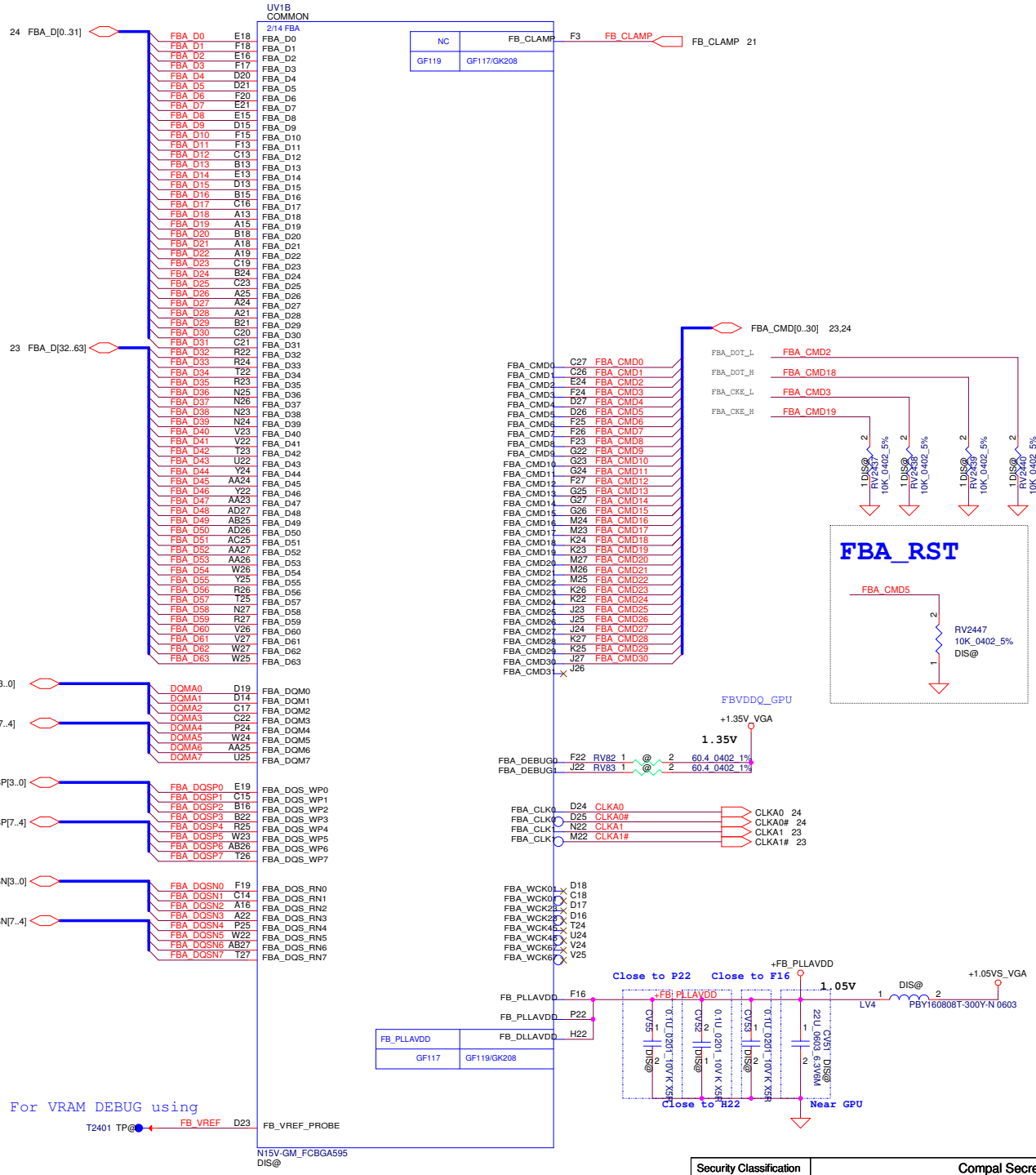
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: NV(4/5)-GPIO/Strap

Size: Custom | Document Number: LA-C311P | Rev: 0.1

Date: Friday, September 26, 2014 | Sheet 21 of 48



6.1.10 Memory ODTx, CKEx, and RST Termination

DDR3 requires Memory Termination on CKEx, ODTx and Memory Reset (RST). Table 6-8 describes the required termination.

Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 k
CKEx	10 k
RST	10 k
CS*	No Termination

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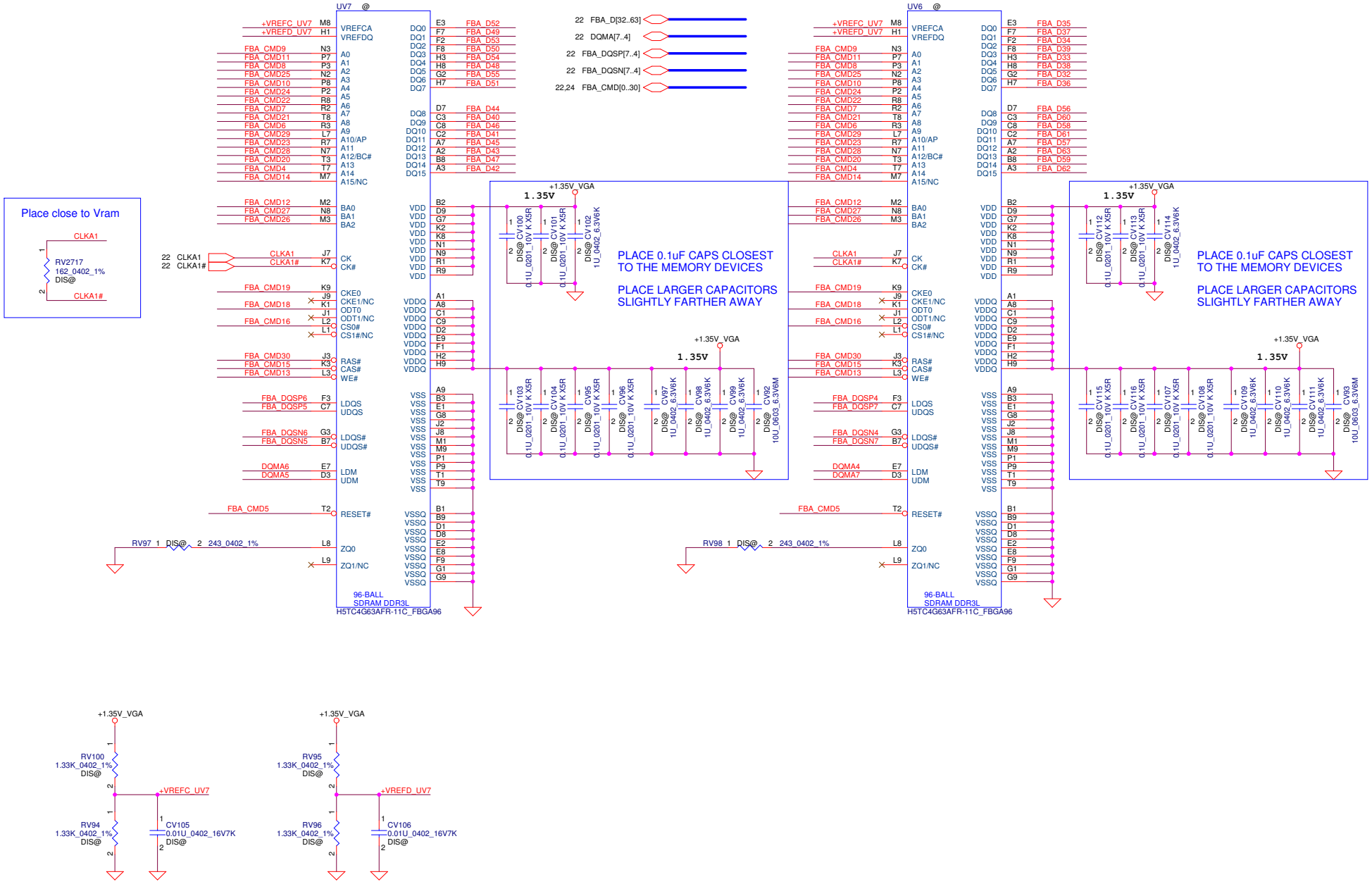
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.			
Title: NV(2/5)-MEMORY FBA			
Size: Custom	Document Number: LA-C311P		Rev: 0.1
Date: Friday, September 26, 2014	Sheet: 22	of: 48	

Memory Partition A - Upper 32 bits [64..32]



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: VRAM_DDR3_A Upper

Size	Document Number	Rev
Custom	LA-C311P	0.1

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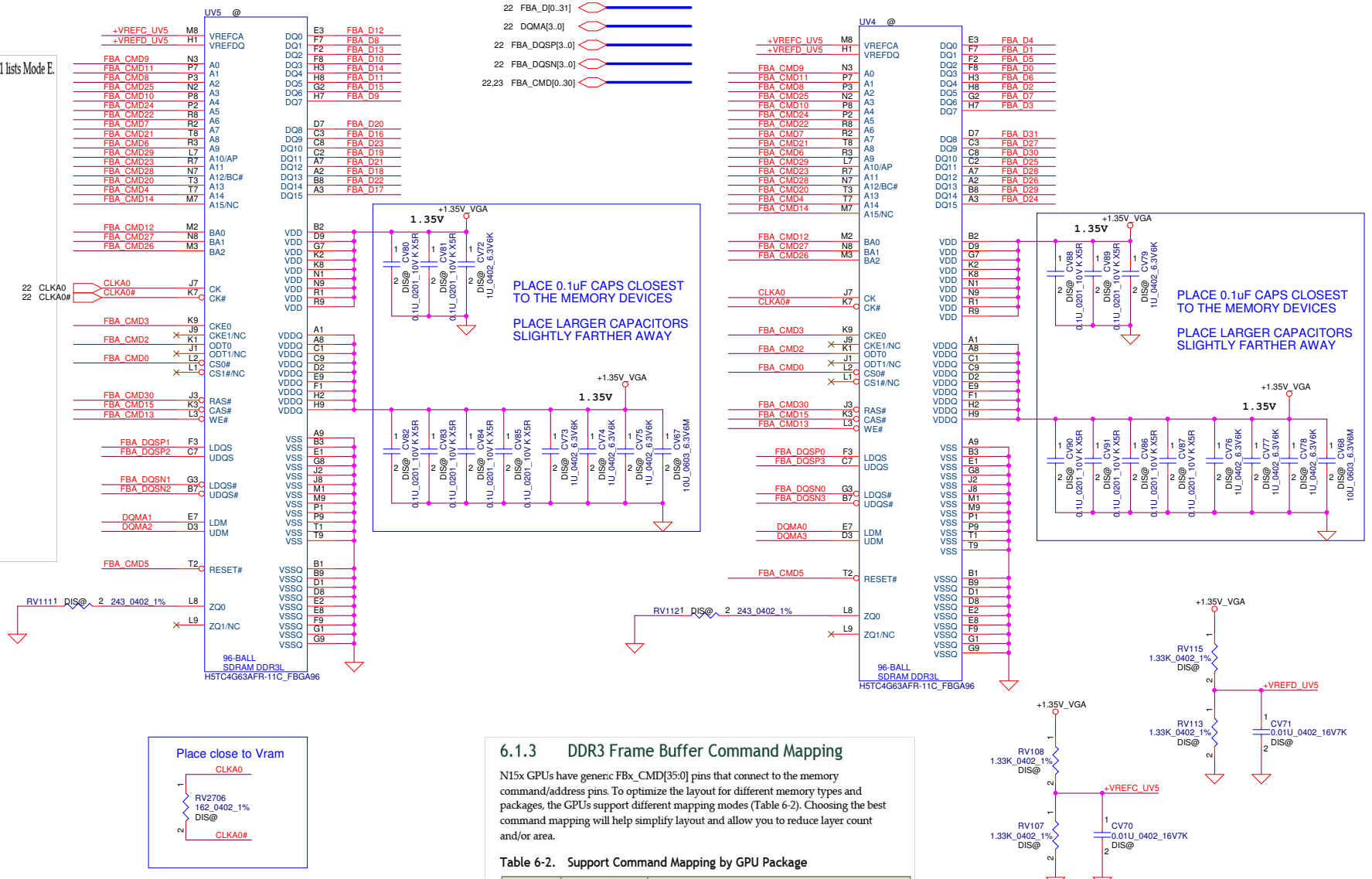
Memory Partition A – Lower 32 bits [31..0]

Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

Table 6-3. Mode D Command Mapping

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11



6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for N15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers[1]. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

Note: [1]Not including two additional layers for power planes.

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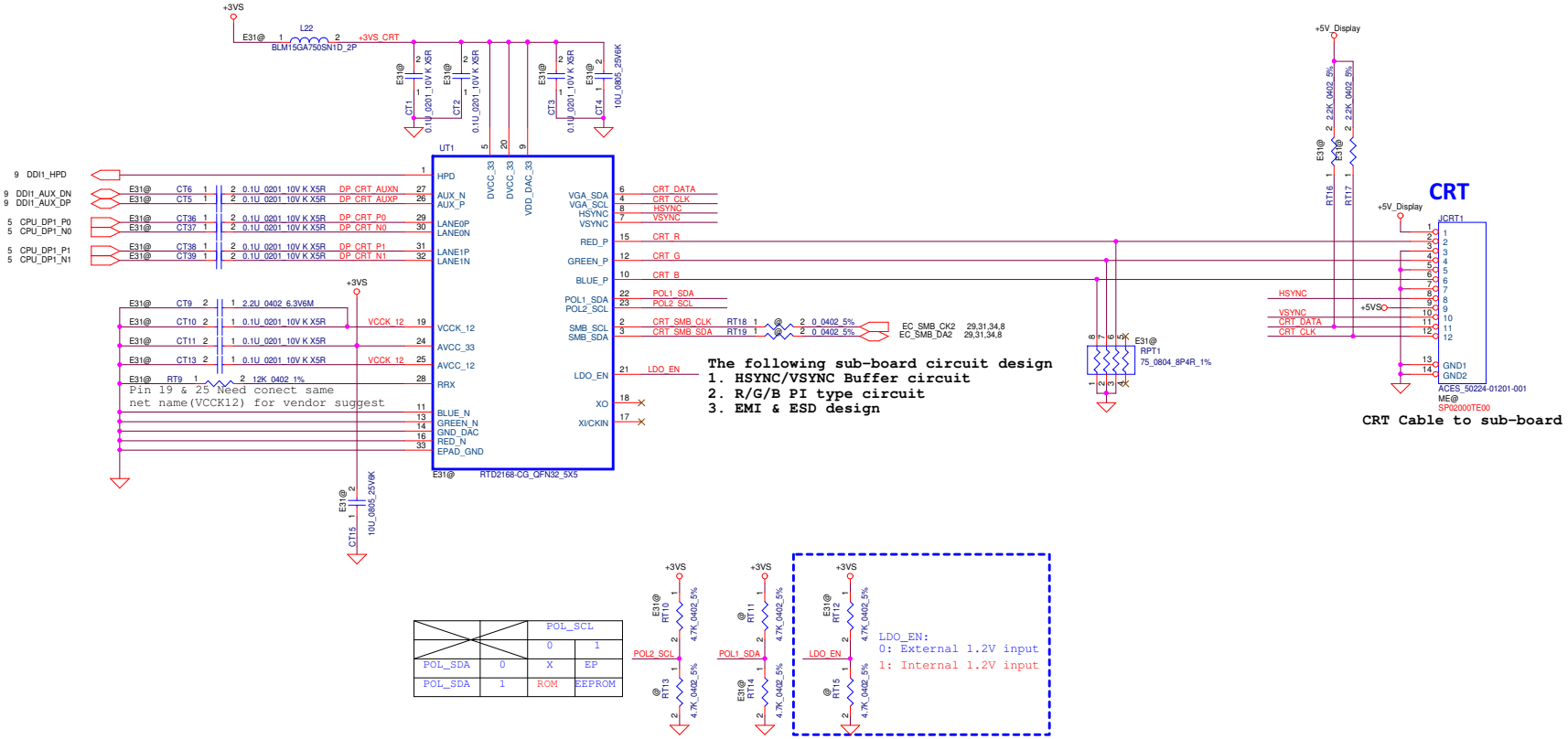
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.			
Title: VRAM_DDR3_A Lower			
Size: Custom	Document Number: LA-C311P		Rev: 0.1
Date: Friday, September 26, 2014	Sheet 24 of 48		



		POL_SCL	
		0	1
POL_SDA	0	X	EP
POL_SDA	1	ROM	EEPROM

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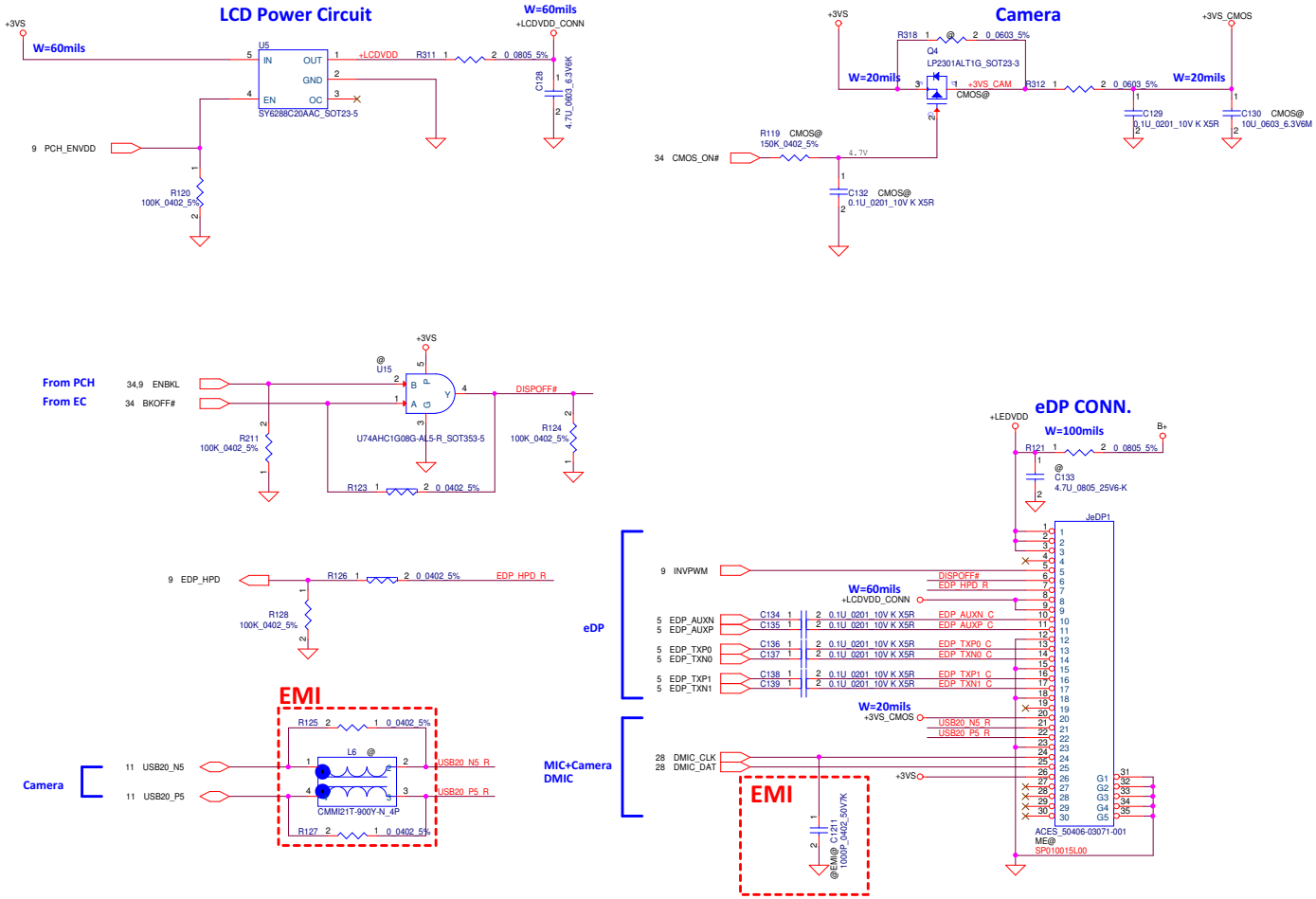
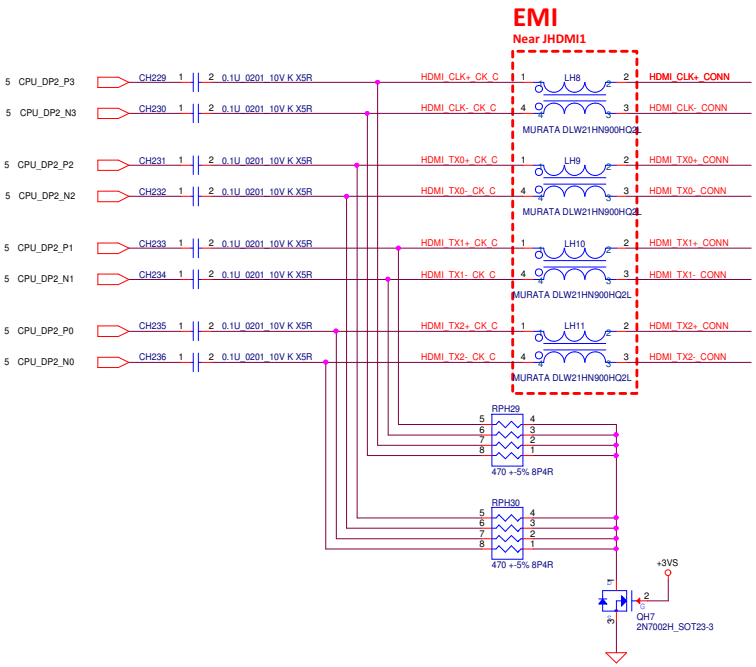
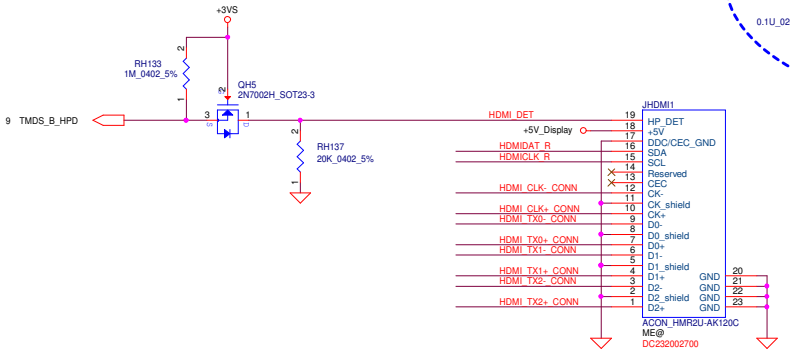
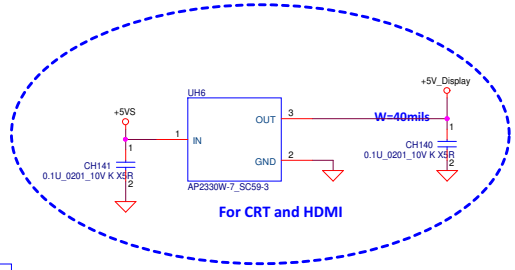


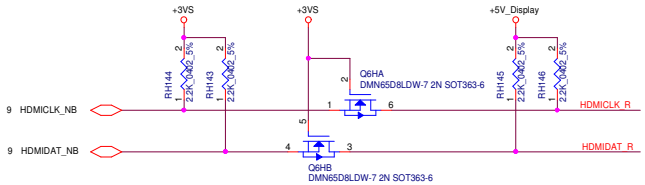
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: eDP / Camera			
Size: C	Document Number: LA-C311P		Rev: 0.1
Date: Friday, September 26, 2014	Sheet 26 of 48		

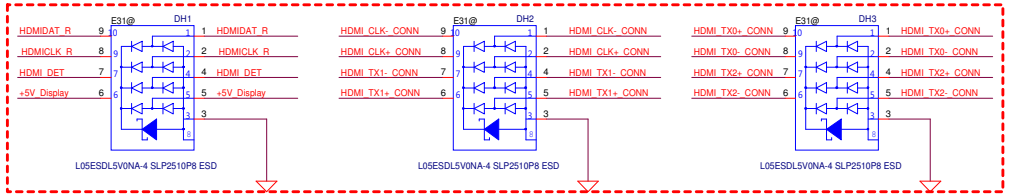








ESD



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: **HDMI**

Size	Document Number	Rev
C	LA-C311P	0.1

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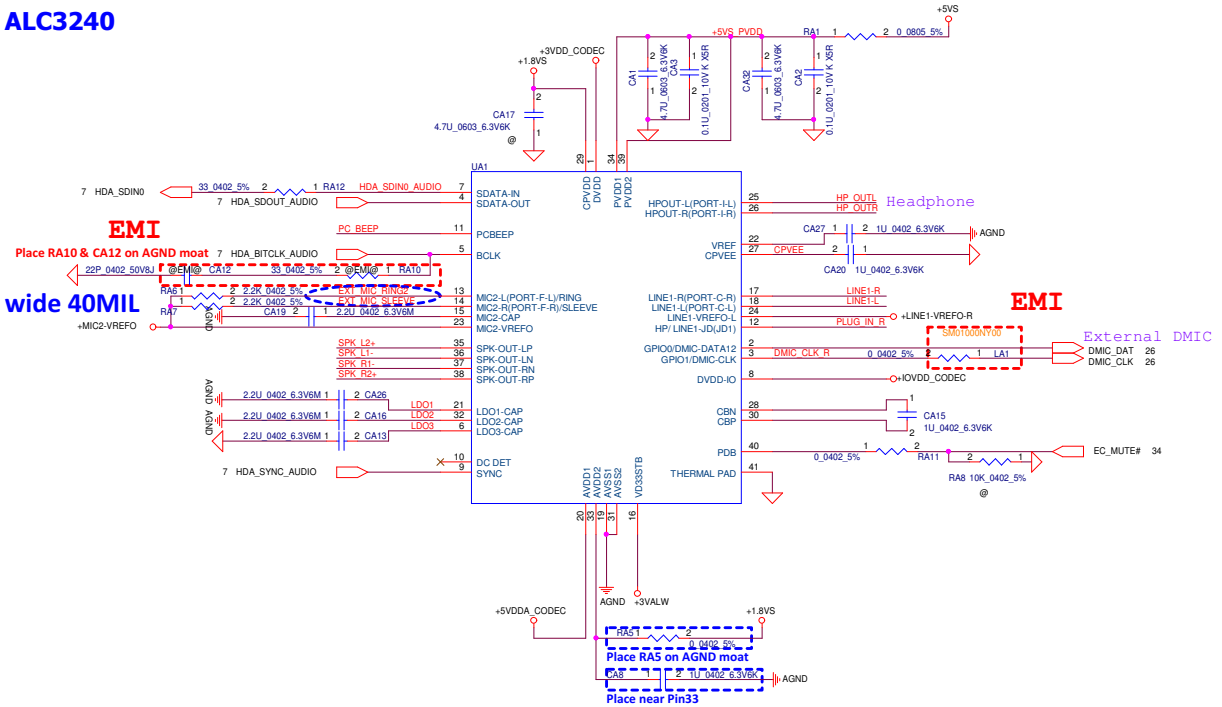
ALC3240

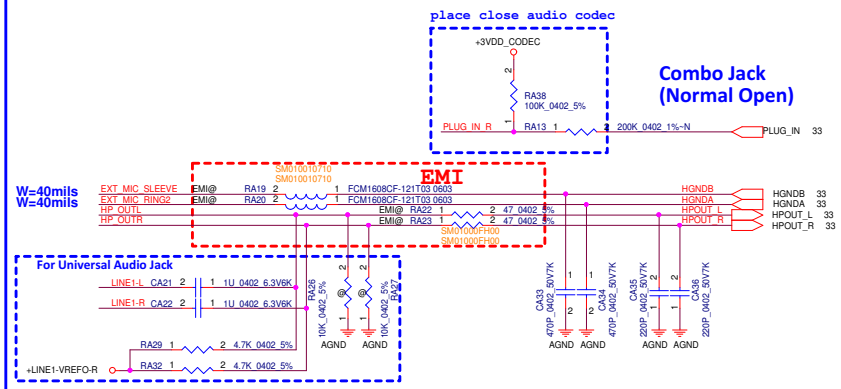


EMI

Place RA10 & CA12 on AGND moat

wide 40MIL

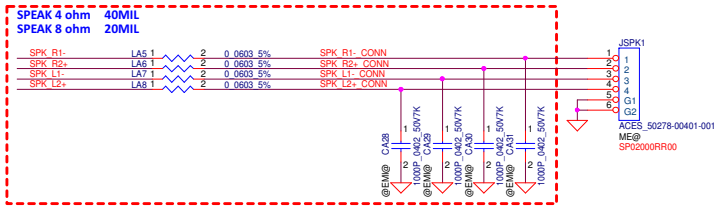
Input



Output

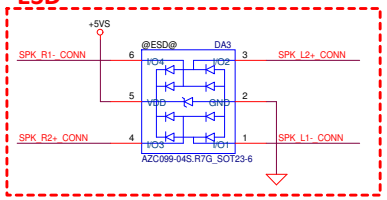
EMI

SPEAK 4 ohm 40MIL
SPEAK 8 ohm 20MIL

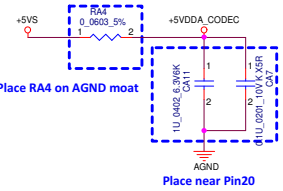


ESD protection needs to be placed near connector side

ESD



+5VS +5VDDA_CODEC



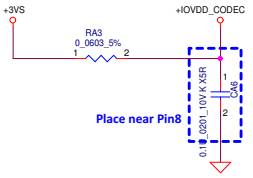
Each Platform Power Net Support List

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

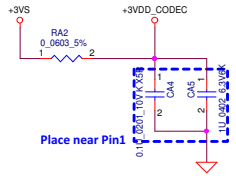
Each Platform HDA Link Voltage Support (Pin 8)

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

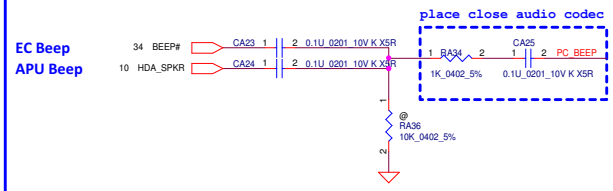
+3VS +IOVDD_CODEC



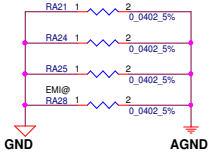
+3VS +3VDD_CODEC



PC Beep



EMI



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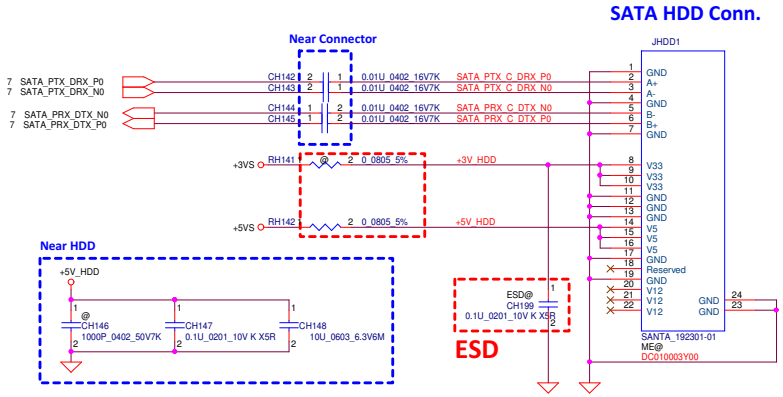
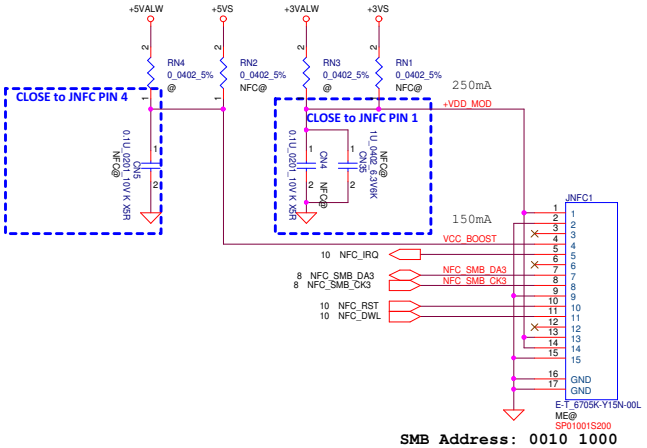
Issued Date	2014/08/04	Deciphered Date	2015/08/04
Title	HD Audio Codec_ALC3240		
Size C	Document Number LA-C311P		Rev 0.1
Date: Friday, September 26, 2014	Sheet 28 of 48		

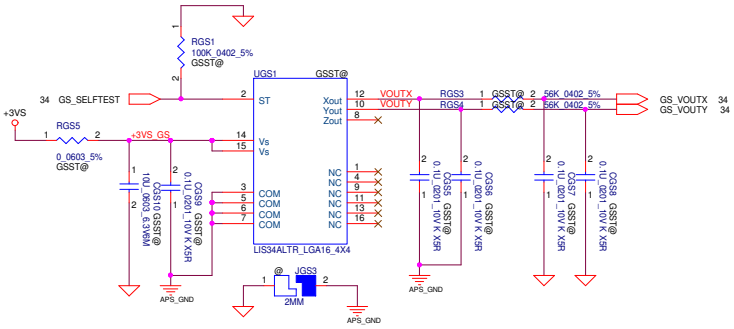
HDD

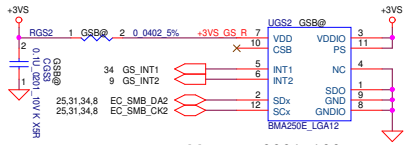


NFC

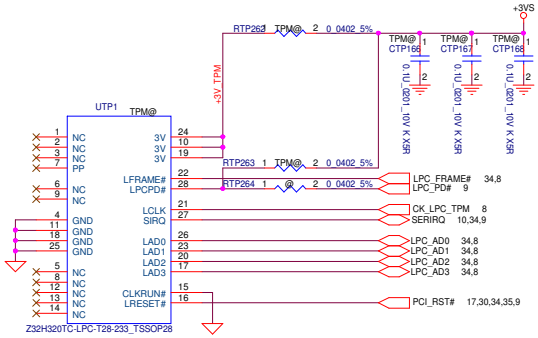


APS (G-Sensor)





TPM



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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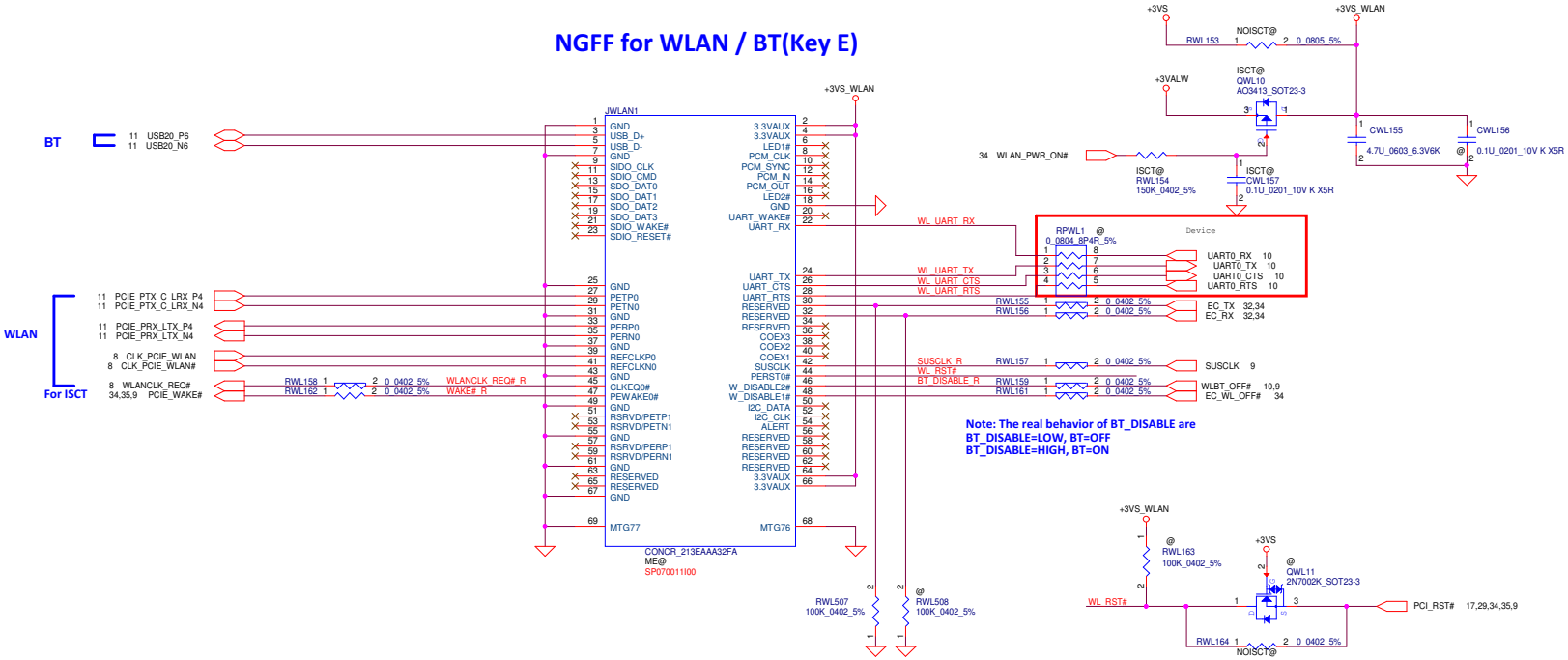
Compal Electronics, Inc.			
Title: HDD/TPM/APS/NFC			
Size: C	Document Number: LA-C311P		Rev: 0.1
Date: Friday, September 26, 2014	Sheet 29 of 48		

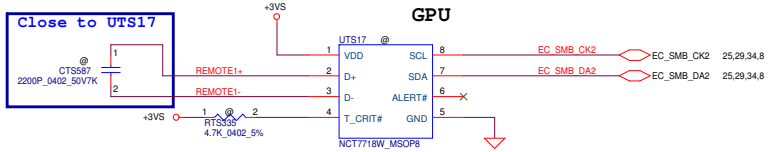
NGFF for WLAN / BT(Key E)



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

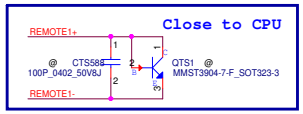
Compal Electronics, Inc.			
Title: NGFF WLAN / BT			
Size	Document Number: LA-C311P		Rev: 0.1
Date: Friday, September 26, 2014	Sheet 30 of 48		

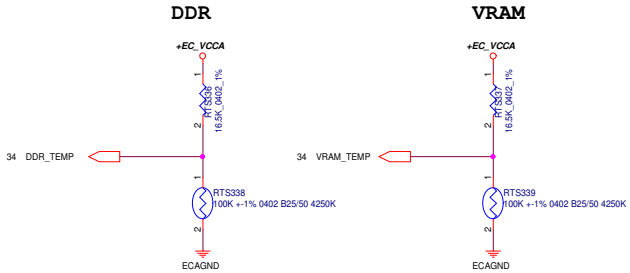
Thermal Sensor

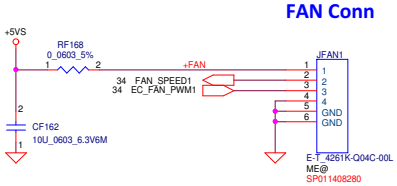


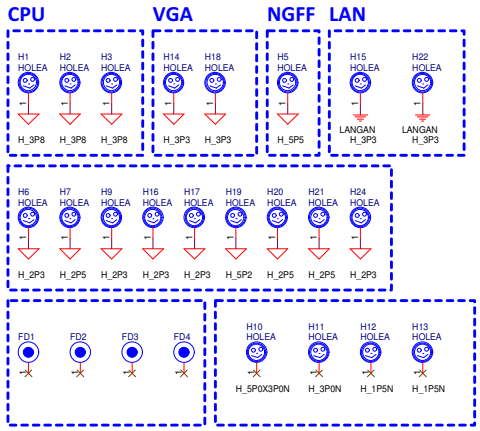
SMB Address: 1001100x

REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"









Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

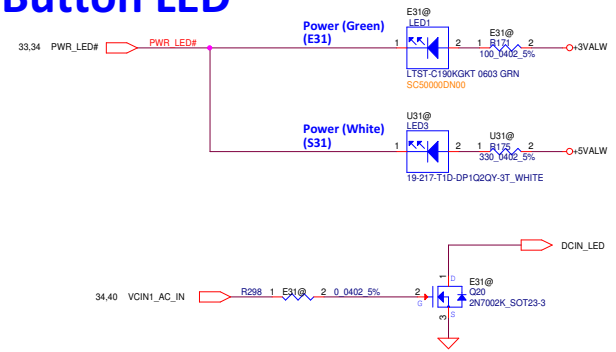
Compal Electronics, Inc.

Title: **FAN / Thermal Senser**

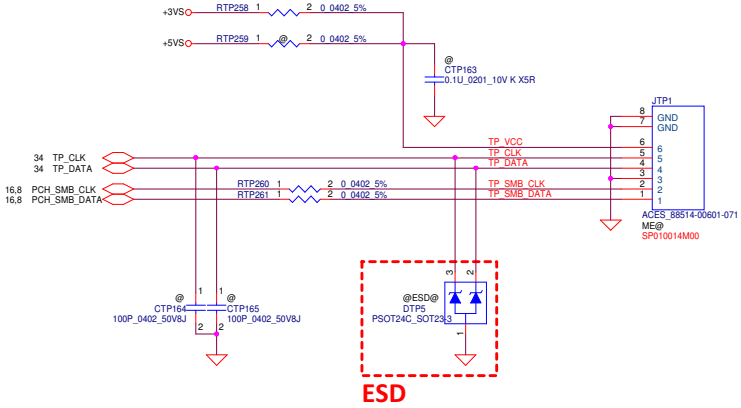
Size	Document Number	Rev
C	LA-C311P	0.1

Date: Friday, September 26, 2014 Sheet 31 of 48

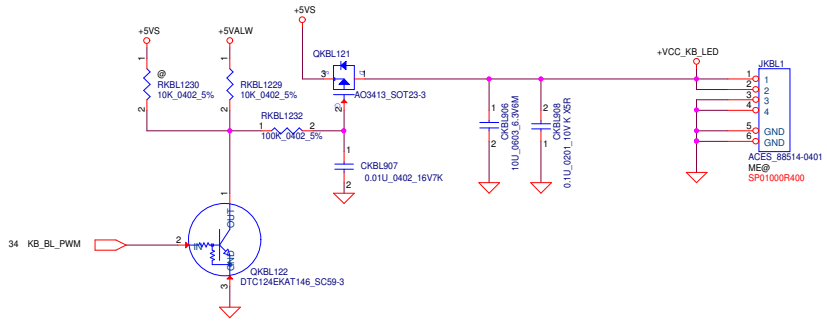
Power Button LED



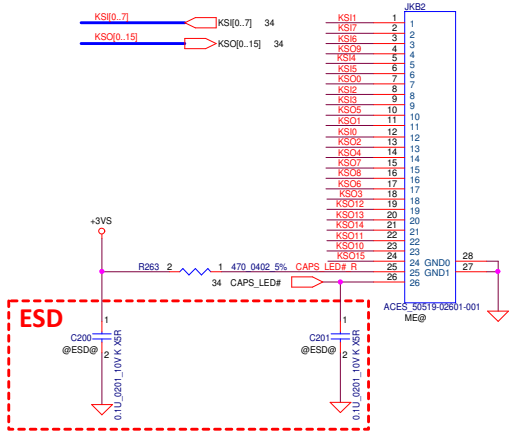
Touch Pad



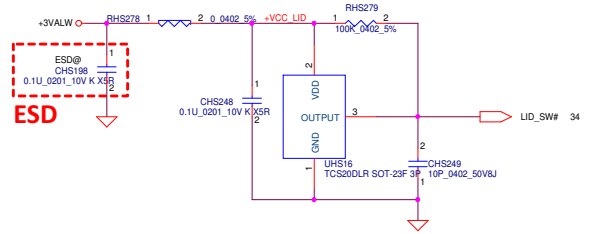
Keyboard Backlight



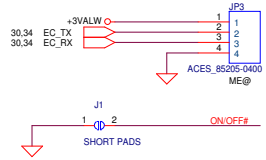
Keyboard



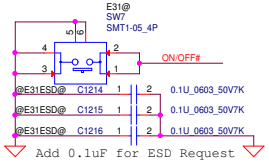
Hall Senser & Button



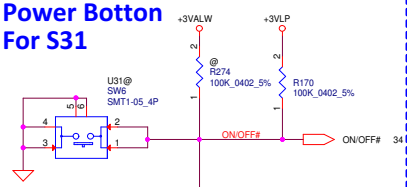
For Debug



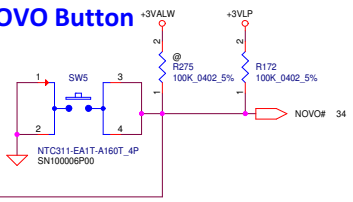
Power Botton For E31



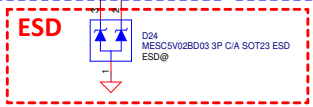
Power Botton For S31



NOVO Button



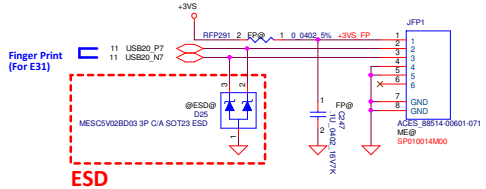
ESD



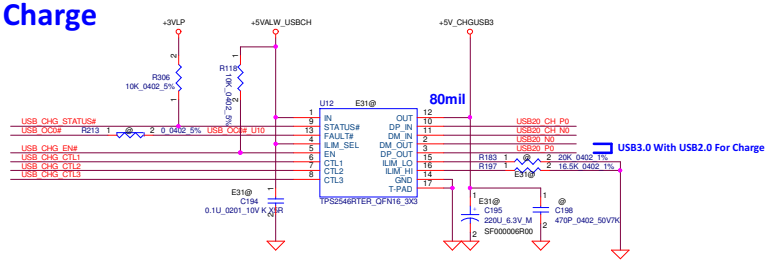
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

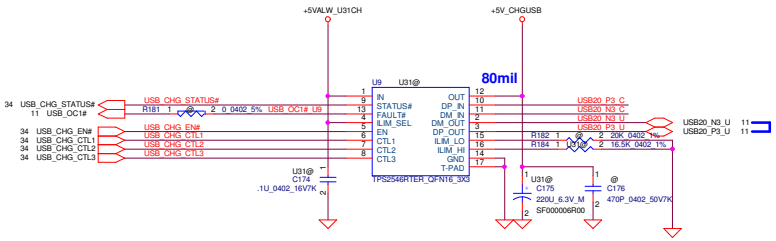
Title	Compal Electronics, Inc. KBL/KBD/LED/TP/HS Conn.		
Size C	Document Number LA-C311P		Rev 0.1
Date: Friday, September 26, 2014	Sheet 32 of 48		

Finger Print

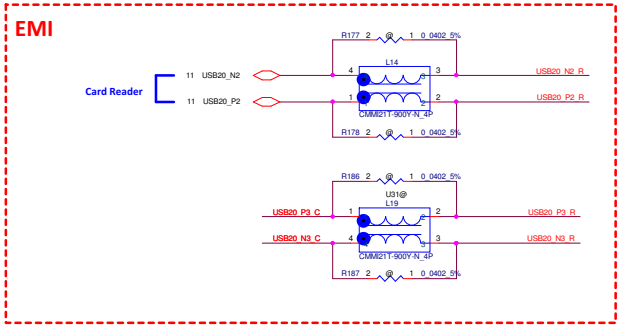


USB Charge

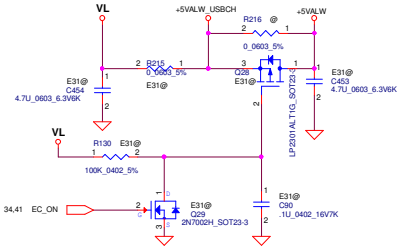




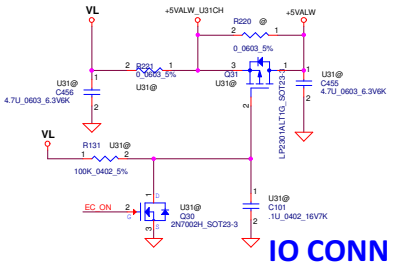
EMI



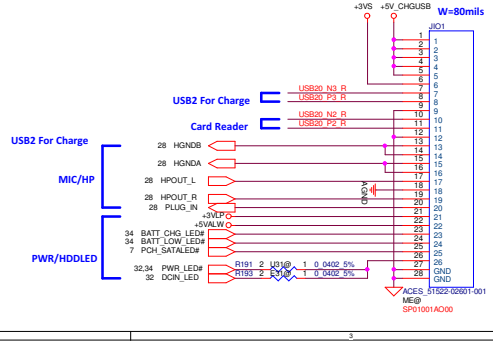
E31 USB Charge switch



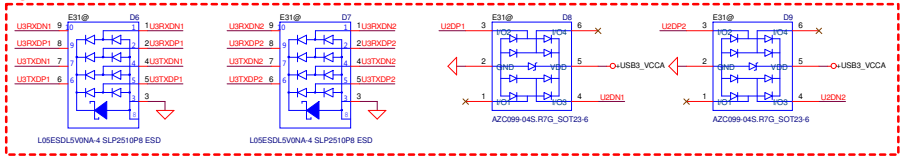
U31 USB Charge switch



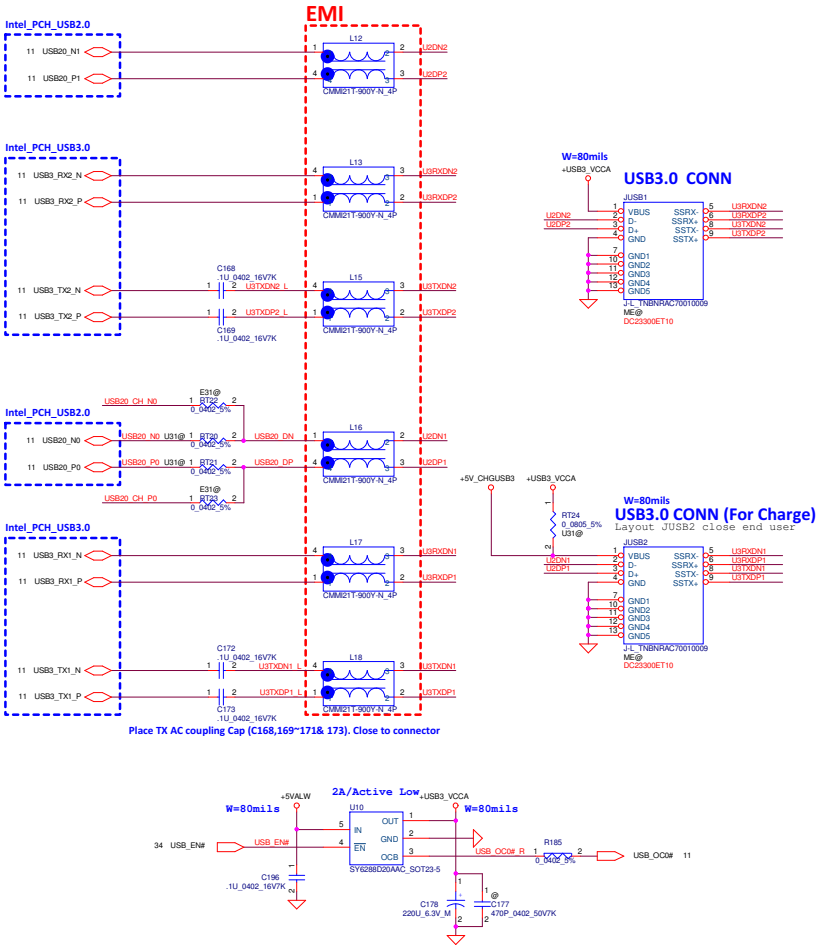
IO CONN



ESD



USB3.0_Port



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

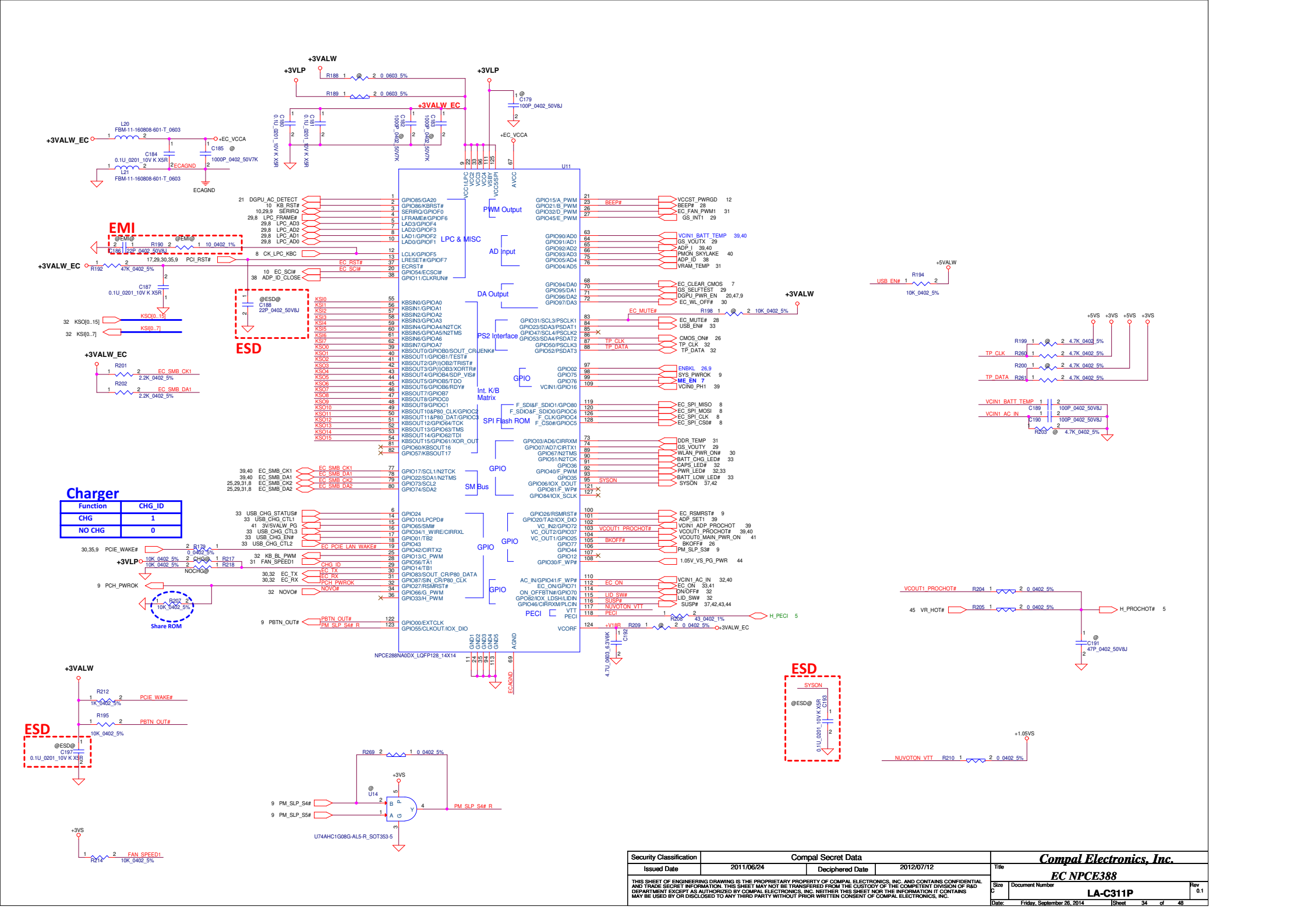
Compal Electronics, Inc.

Title: USB2 / USB3 / FP / IO Board

Document Number: LA-C311P

Rev: 0.1

Date: Friday, September 26, 2014 Sheet 33 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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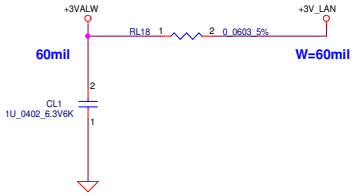
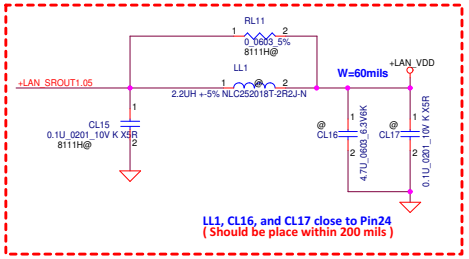
Compal Electronics, Inc.

Title: **EC NPCE388**

Size	Document Number	Rev
C	LA-C311P	0.1

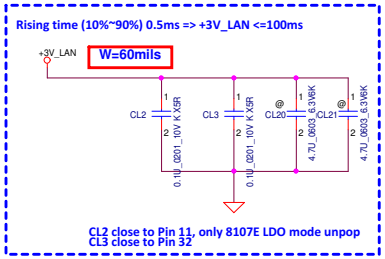
Date: Friday, September 26, 2014 | Sheet 34 of 48

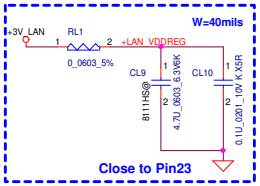


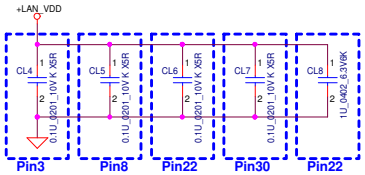


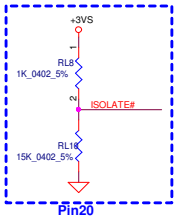
	1.0V Source	LL1	CL16,CL17	CL9,CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O
RTL8107E	LDO	X	X	X	X	X

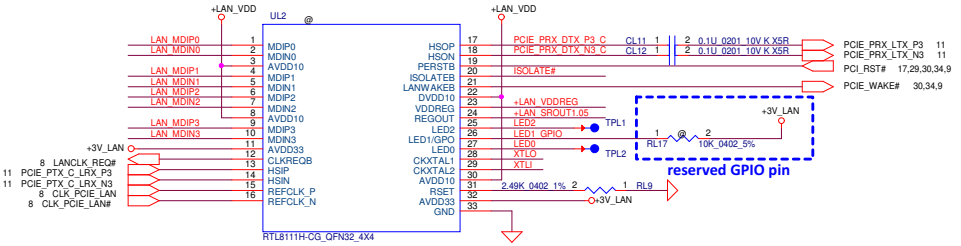
Please refer to the table above when using different 1.0V supply source.

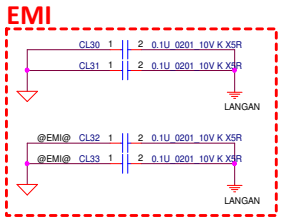


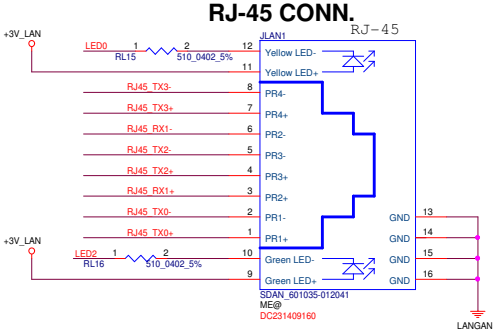


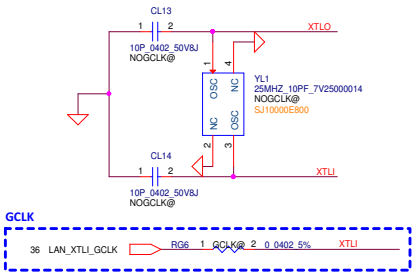


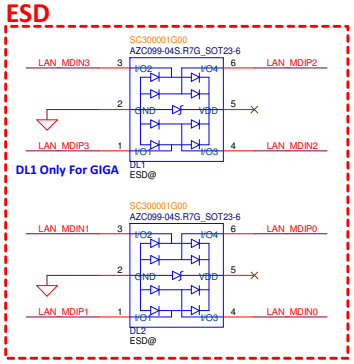


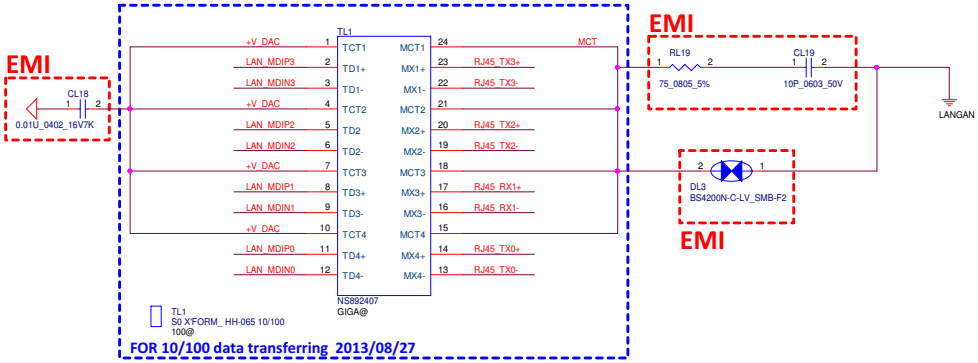












Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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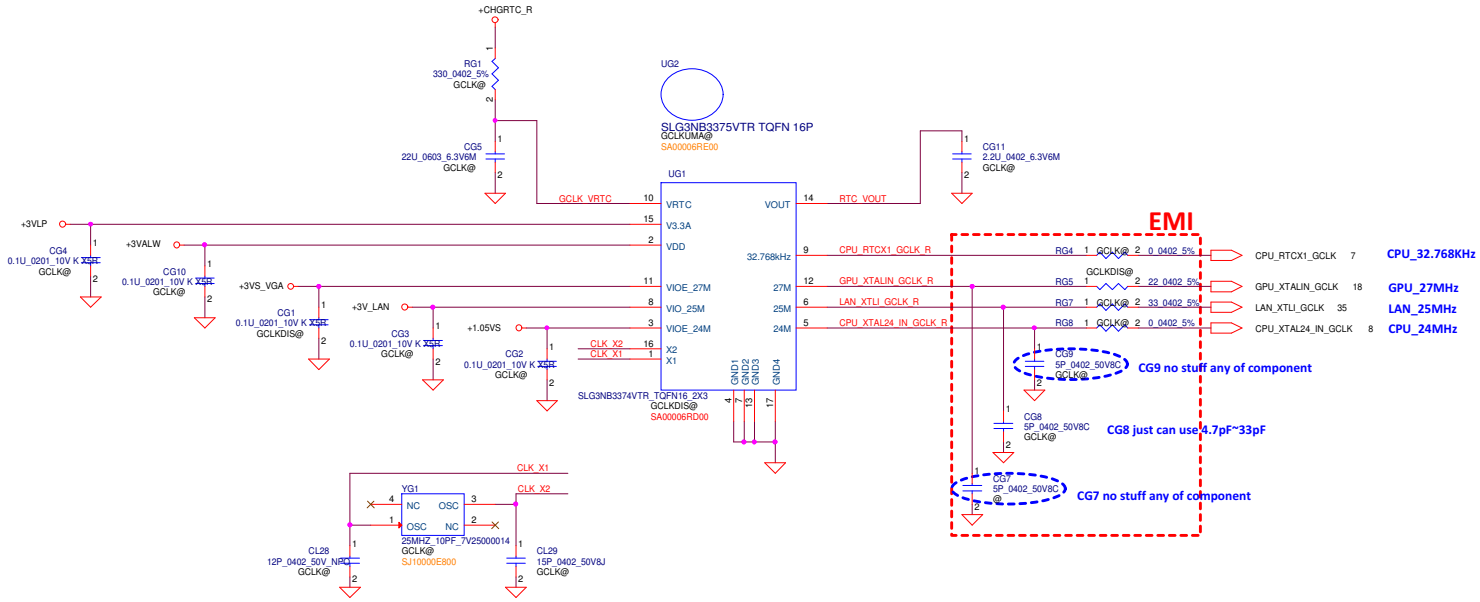
Compal Electronics, Inc.

Title: LAN_RTL8111H / RTL8107E

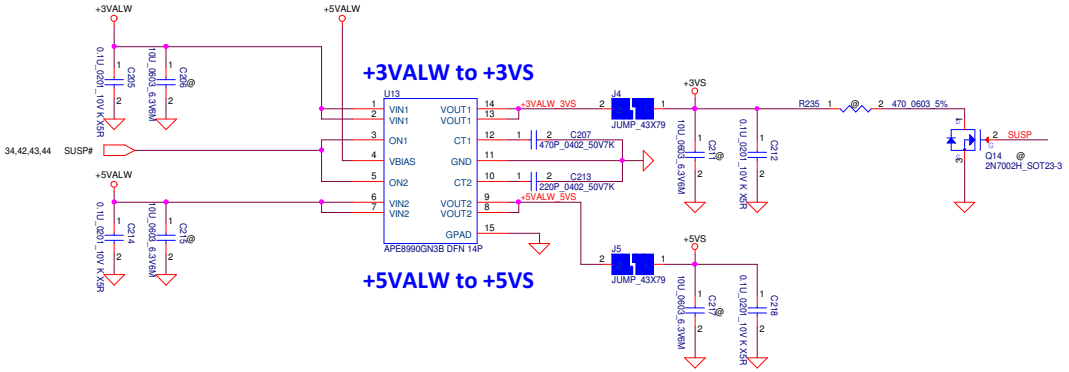
Size	Document Number	Rev
C	LA-C311P	0.1

Date: Friday, September 26, 2014 Sheet 35 of 48

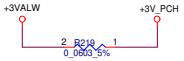


Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

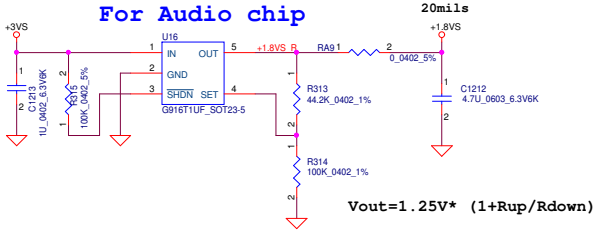
Compal Electronics, Inc.			
Title	GCLK_SLG3NB3374VTR		
Size	Document Number		Rev
	LA-C311P		0.1
Date:	Friday, September 26, 2014	Sheet	36 of 48



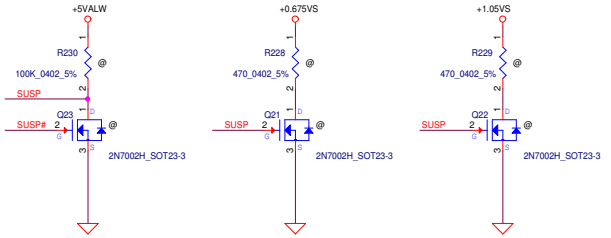
+3VALW to +3V_PCH

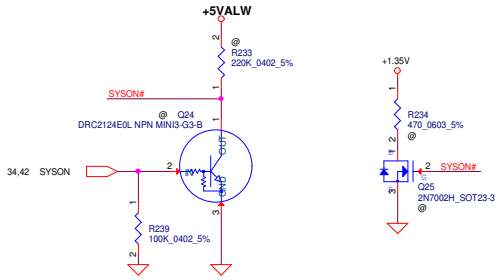


For Audio chip

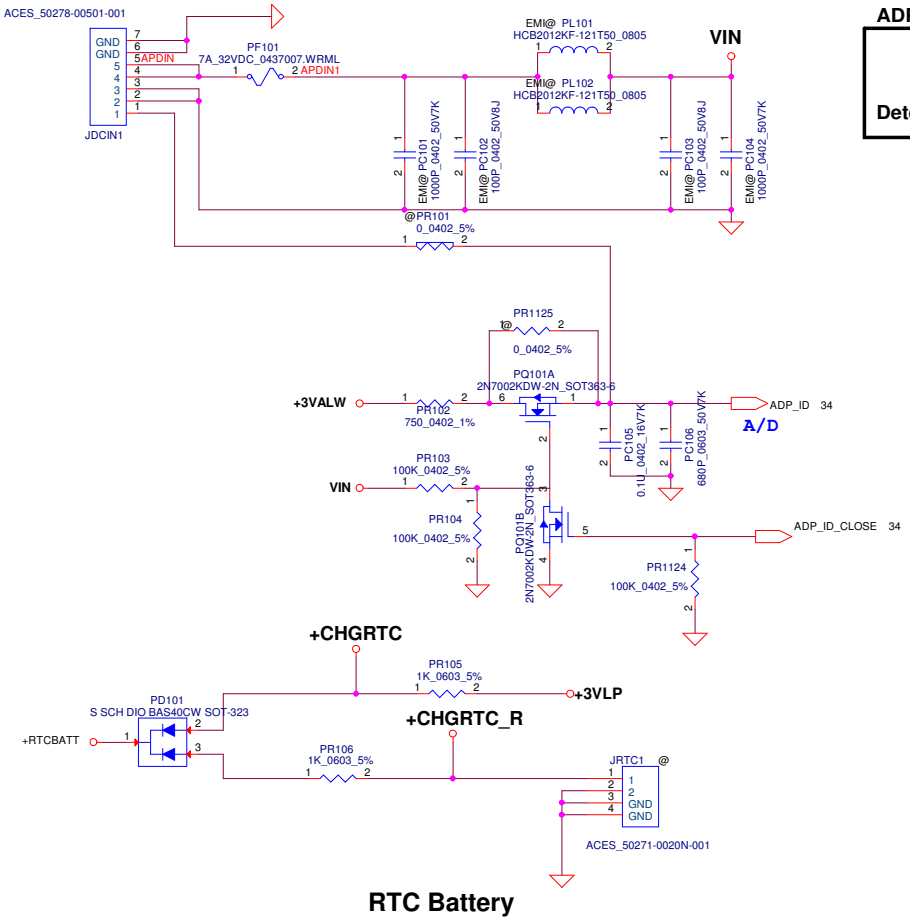


Vout=1.25V* (1+Rup/Rdown)





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	DC TO DC		
Size C	Document Number LA-C311P		Rev 0.1
Date: Friday, September 26, 2014	Sheet 37 of 48		



ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

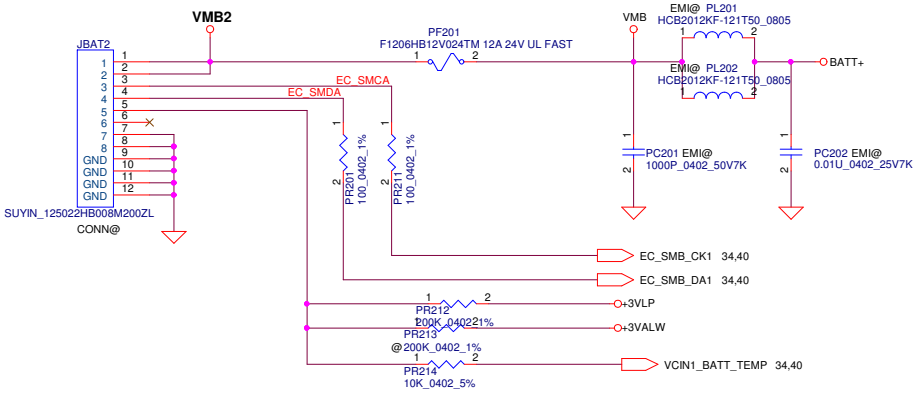
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

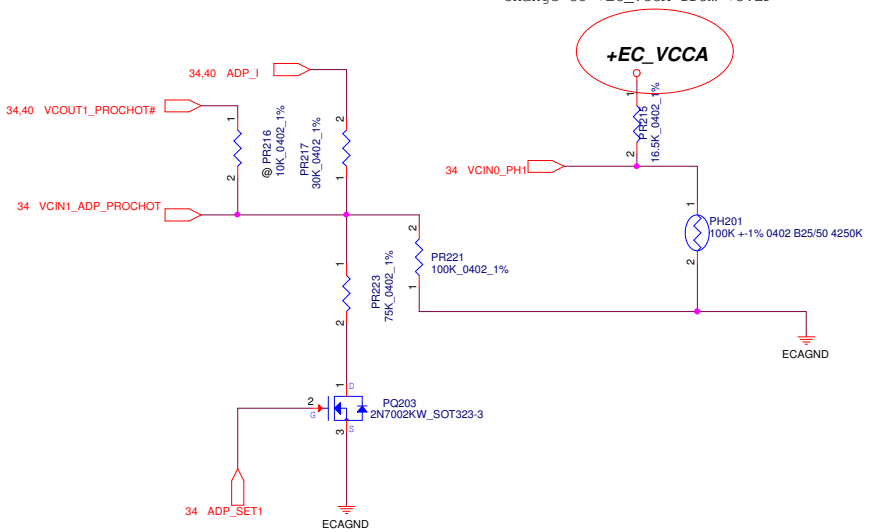
Size: Custom | Document Number: BDW | Rev: 0.1

Date: Friday, September 26, 2014 | Sheet 38 of 48



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

20120314
Change to +EC_VCCA from +3VLP



135W: 150W(Turbo_V=1.2) active 135W(Turbo_V=1.072) recovery
90W : 100W(Turbo_V=1.2) active 90W(Turbo_V=0.903) recovery
65W : 70W(Turbo_V=1.2) active 65W(Turbo_V=0.918) recovery
45W : 65W(Turbo_V=1.2) active 45W(Turbo_V=0.829) recovery

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	BDW	0.1

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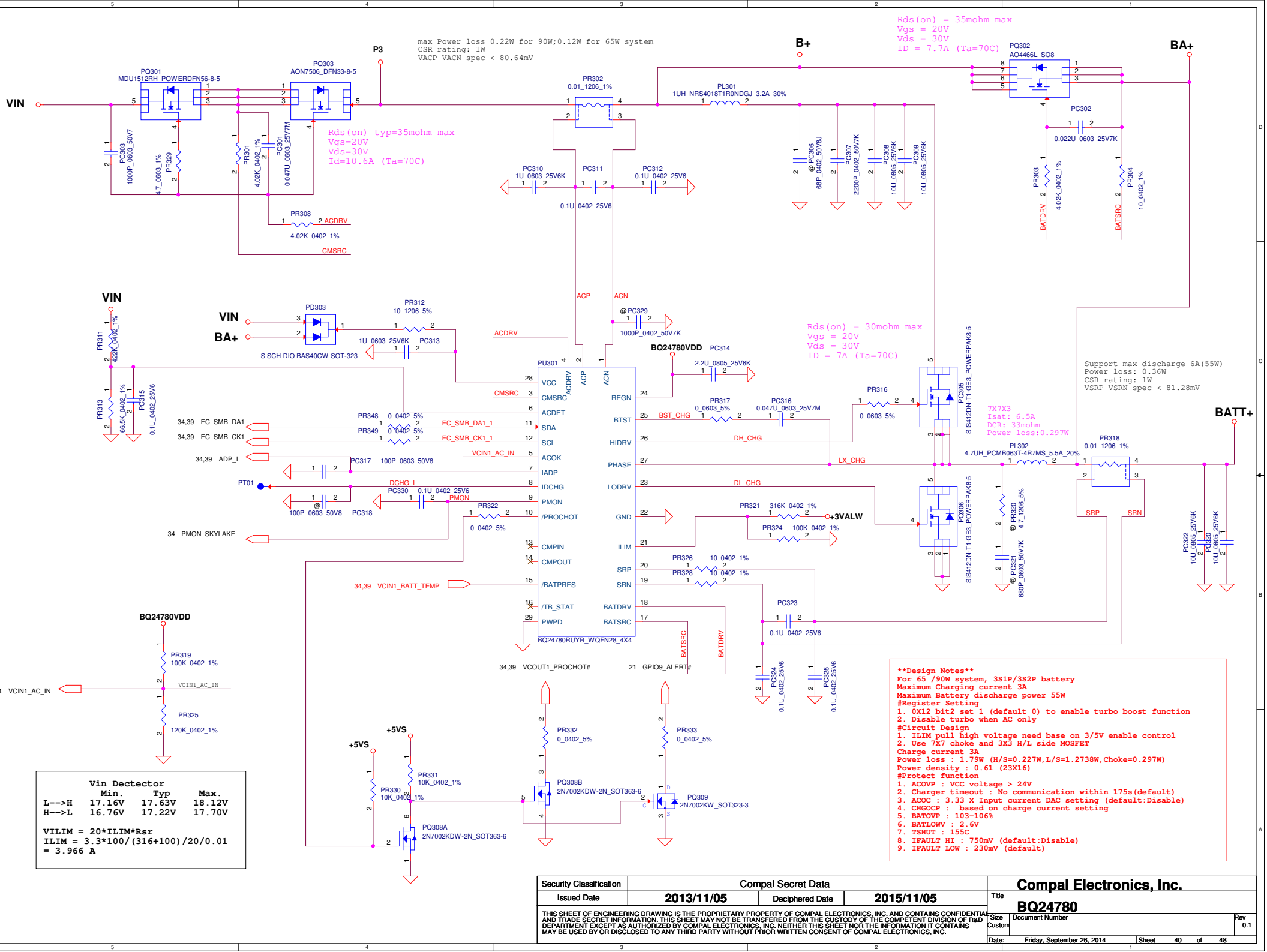
max Power loss 0.22W for 90W;0.12W for 65W system
CSR rating: 1W
VACP-VACN spec < 80.64mV
Rds(on) = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)
Rds(on) typ=35mohm max
Vgs=20V
Vds=30V
Id=10.6A (Ta=70C)
Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)
Support max discharge 6A(55W)
Power loss: 0.36W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV
7X7X3
Isat: 6.5A
DCR: 33mohm
Power loss:0.297W
VIN
BA+
B+
BATT+
P3
+3VALW
+5VS
BQ24780VDD
PQ301 MDU1512RH_POWERDFN56-8-5
PQ303 AON7506_DFN33-8-5
PQ302 AO4466L_SO8
PR302 0.01_1206_1%
PL301 1UH_NRS4018T1R0NDGJ_3.2A_30%
PR308 4.02K_0402_1%
CMSRC
ACDRV
ACP
ACN
PD303 S SCH DIO BAS40CW SOT-323
PR312 10_1206_5%
PC313 1U_0603_25V6K
PC314 2.2U_0805_25V6K
PU301
BQ24780RUYR_WQFN28_4X4
VCC
CMSRC
ACDET
SDA
SCL
ACOK
IADP
IDCHG
PMON
/PROCHOT
CMPIN
CMPOUT
/BATPRES
/TB_STAT
PWPD
REGN
BTST
HIDRV
PHASE
LODRV
GND
ILIM
SRP
SRN
BATDRV
BATSRC
34,39 EC_SMB_DA1
34,39 EC_SMB_CK1
34,39 ADP_I
PT01
34 PMON_SKYLAKE
34,39 VCIN1_BATT_TEMP
34,39 VCOUT1_PROCHOT#
21 GPIO9_ALERT#
VCIN1_AC_IN
BST_CHG
DH_CHG
LX_CHG
DL_CHG
PR316 0_0603_5%
PR317 0_0603_5%
PC316 0.047U_0603_25V7M
PR318 0.01_1206_1%
PL302 4.7UH_PCMB063T-4R7MS_5.5A_20%
PQ305 SIS412DN-T1-GE3_POWERPAK8-5
PQ306 SIS412DN-T1-GE3_POWERPAK8-5
PR319 100K_0402_1%
PR325 120K_0402_1%
PR321 316K_0402_1%
PR324 100K_0402_1%
PR326 10_0402_1%
PR328 10_0402_1%
PR320 4.7_1206_5%
PC321 680P_0603_50V7K
PC322 10U_0805_25V6K
PC320 10U_0805_25V6K
PC323 0.1U_0402_25V6
PC324 0.1U_0402_25V6
PC325 0.1U_0402_25V6
PR331 10K_0402_1%
PR330 10K_0402_1%
PR332 0_0402_5%
PR333 0_0402_5%
PQ308A 2N7002KDW-2N_SOT363-6
PQ308B 2N7002KDW-2N_SOT363-6
PQ309 2N7002KW_SOT323-3
Vin Dectector
Min. Typ Max.
L-->H 17.16V 17.63V 18.12V
H-->L 16.76V 17.22V 17.70V
VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(316+100)/20/0.01
= 3.966 A
Design Notes
For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3A
Maximum Battery discharge power 55W
#Register Setting
1. 0X12 bit2 set 1 (default 0) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ILIM pull high voltage need base on 3/5V enable control
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting (default:Disable)
4. CHGOCP : based on charge current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.6V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default:Disable)
9. IFAULT LOW : 230mV (default)
Security Classification
Compal Secret Data
Issued Date
2013/11/05
Deciphered Date
2015/11/05
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Title
BQ24780
Size
Custom
Document Number
Rev
0.1
Date: Friday, September 26, 2014
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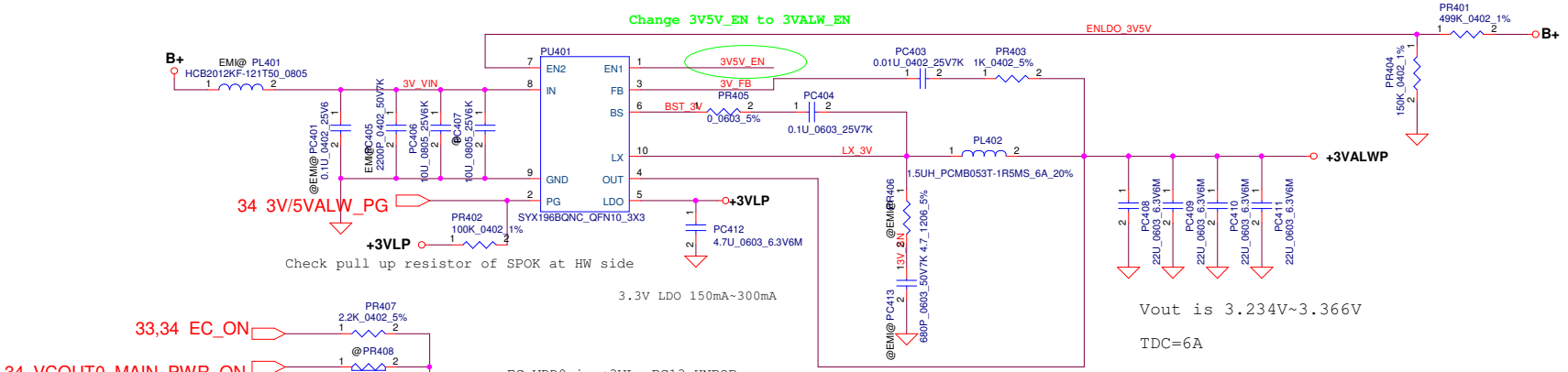
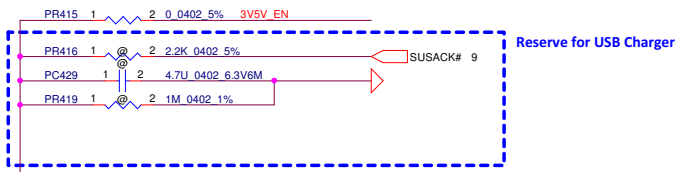
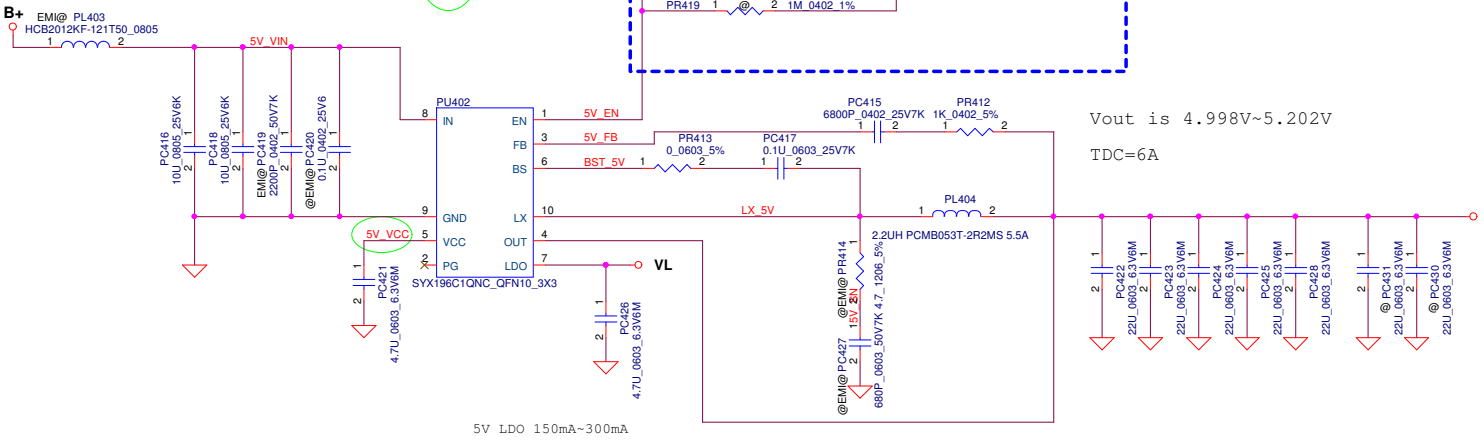
EN1 and EN2 dont't floating

Change 3V5V_EN to 3VALW_EN







Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: BDW | Rev: 0.1

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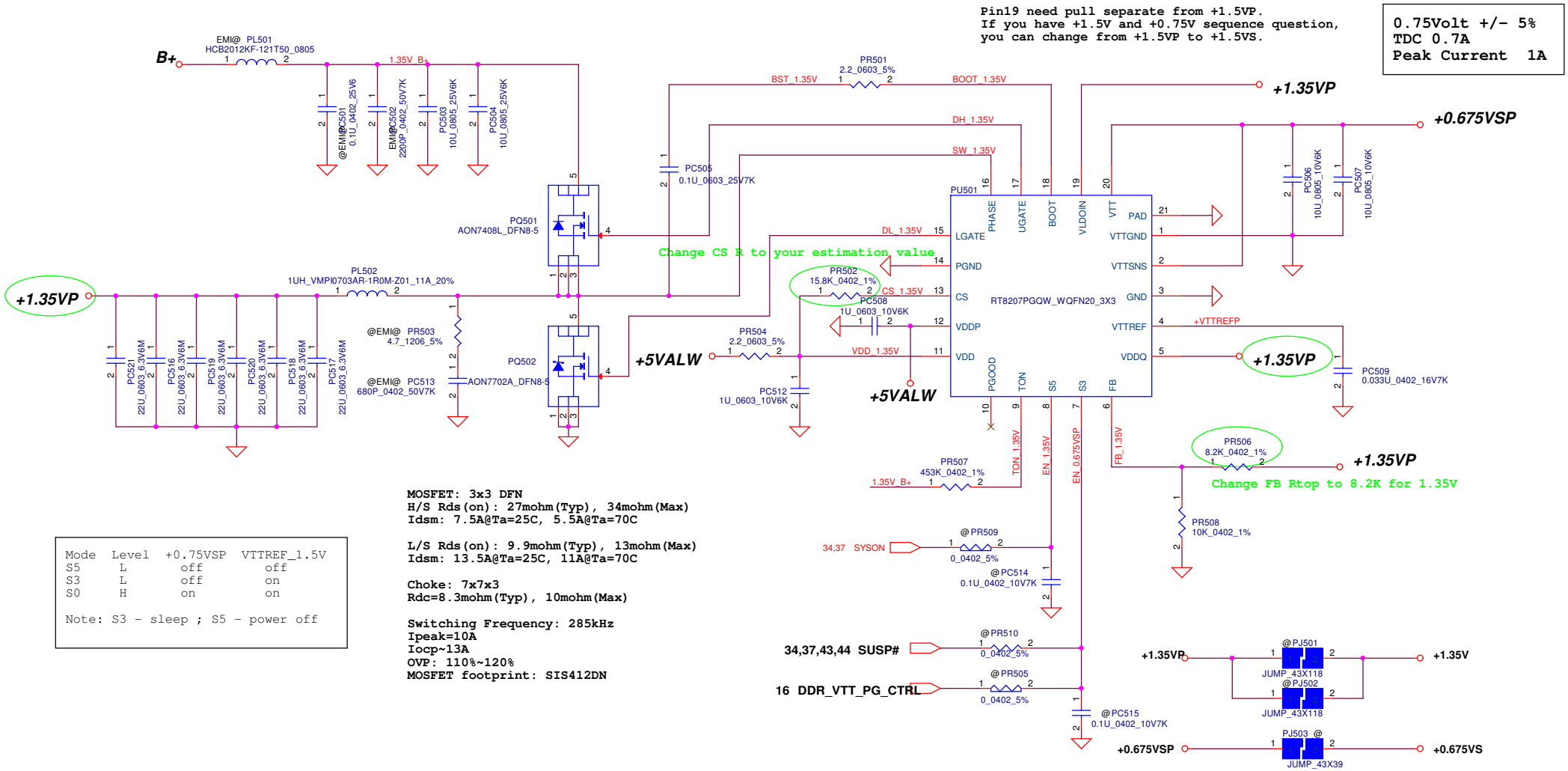

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: RT8207M

Size: Custom | Document Number: BDW | Rev: 0.1

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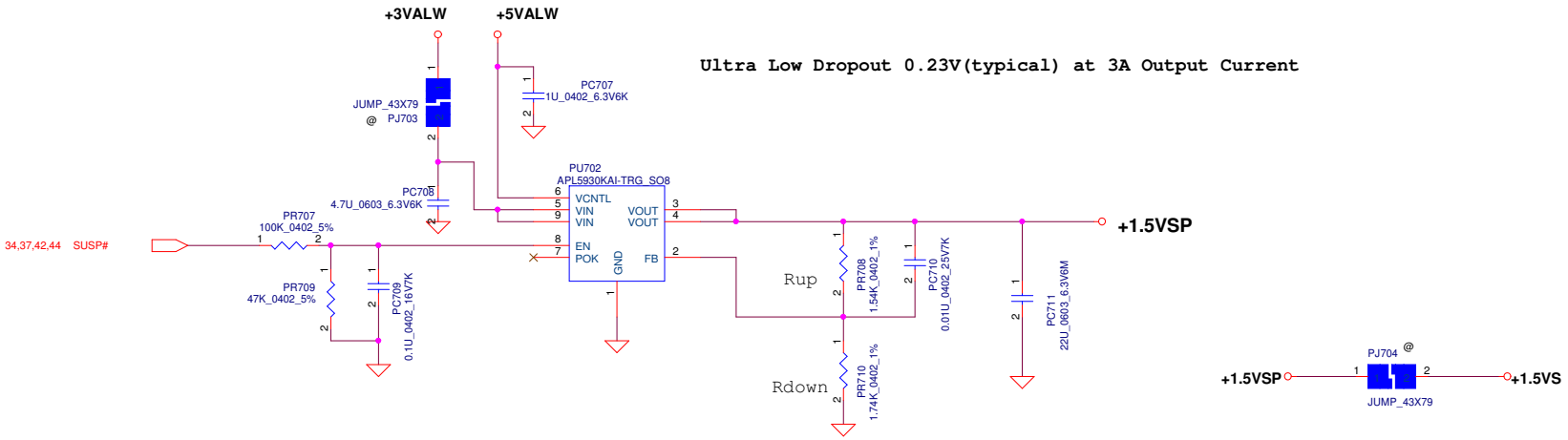

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: +1.5VS

Size	Document Number	Rev
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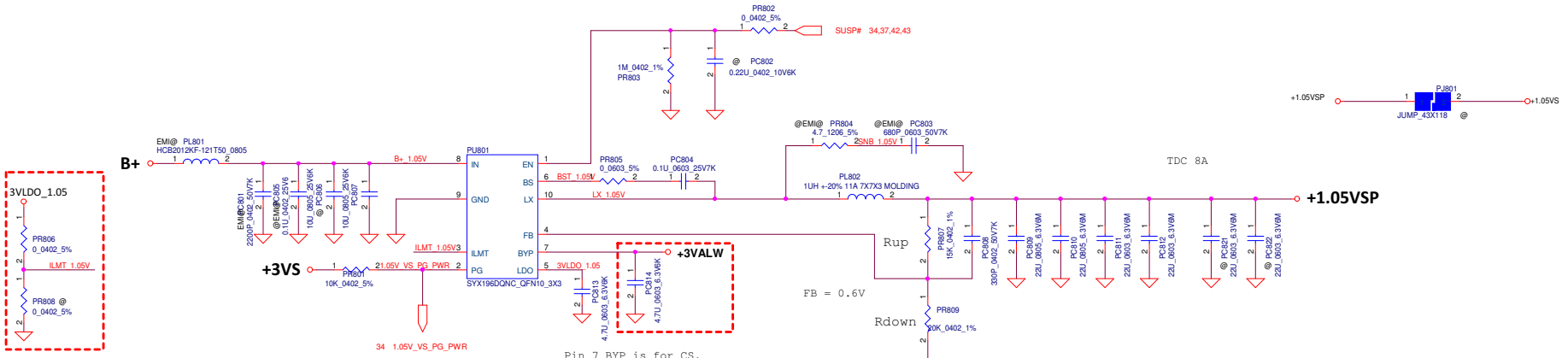
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

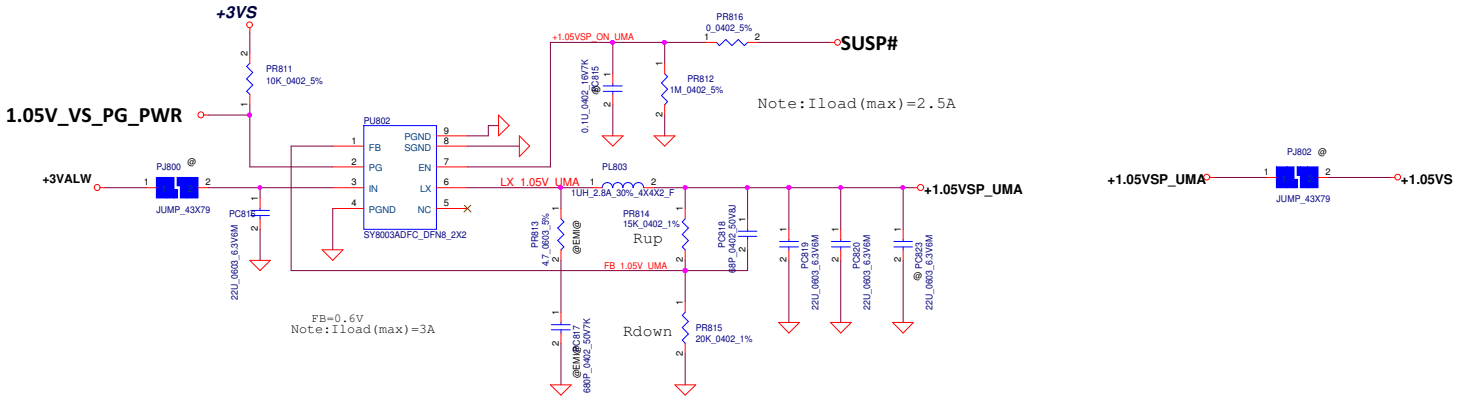


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.05V



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: +1.05VS

Size	Document Number	Rev
C	BDW	0.1

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Base on BDW PDDG Rev_0_73		
Location	15W TDC 14A MAX 32A OCP 39A Loadline=-2.0mv/A	Note
PR1120	499 Ohm	OCP
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Rdc=0.62mohm +-5%
Heat Rating Current=41.5A
Saturation Current=41A

+1.05VS
Follow intel guideline
PR1102 130_0402_1%
PR1103 54.9_0402_1%
PC1102 1U_0402_6.3V6K

Note:
VR_SVID_ALRT# Pull high on HW side

12 VR_SVID_DAT
12 VR_SVID_ALRT#
12 VR_SVID_CLK
12 VR_ON
12 VGATE
34 VR_HOT#

Note:
VR_HOT# Pull high on HW side

PU1101 ISL95813HRZ-T_QFN20_3X4
PAD SCLK ALERT# SDA PRGM1
VR_ON PGOOD IMON VR_HOT# NTC COMP FB ISUMN ISUMP RTN
LGATE PHASE UGATE BOOT VCC PRGM2

PR1104 169K_0402_1%
Note:
PR1104=169K
=>Icc(max)=33A
fsw=700KHz

PR1105 0_0603_5%
PR1108 2.2_0603_5%
PC1108 0.22U_0603_16V7K
PC1111 0.1U_0402_25V6
PR1112 124K_0402_1%
Note:
PR1112=124K
=>Slew rate=53mV/us
Vboot = 1.7V

+5VS

PR1122 1.5K_0402_1%
PC1101 1000P_0402_50V7K
PR1106 95.3K_0402_1%
PH1101 470K +-5% 0402 B25/50 4700K
PR1110 3.83K_0402_1%
PR1111 27.4K_0402_1%
PC1109 47P_0402_50V8J

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

PR1113 909_0402_1%
@PC1112 33P_0402_50V8J
PC1113 6800P_0402_25V7K

Droop
@PR1114 2K_0402_1%
@PC1114 330P_0402_50V7K
@PR1115 10_0402_1%
@PC1115 390P_0402_50V7K
PR1116 1.27K_0402_1%

PR1117 4.99M_0402_1%

RC Match
PC1116 0.033U_0402_25V7K
PC1117 0.1U_0402_16V4Z
PR1119 11K_0402_1%
PR1118 4.42K_0402_1%
PH1102 10K +-5% 0402 B25/50 4250K

OCP Setting
PR1120 287_0402_1%

12 VCCSENSE
12,14 VSSSENSE

@PC1118 330P_0402_50V7K
@PC1119 0.082U_0402_16V7K
PC1120 0.01U_0402_50V7K

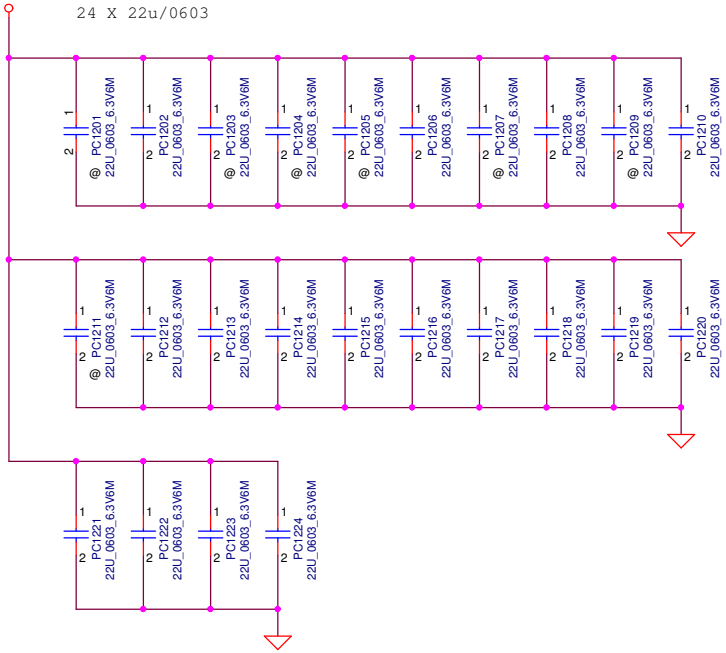
@PC1121 4700P_0402_25V7K
@PR1121 1.5K_0402_1%

Local sense put on HW site

CPU_B+
PQ1101 MDV1525URH_PDFN33-8-5
PQ1103 MDU1511RH_POWERDFN56-8-5
PQ1102 MDU1511RH_POWERDFN56-8-5
PC1103 10U_0805_25V6K
PC1104 10U_0805_25V6K
EM@PC1105 0.01U_0402_50V7K
EM@PC1106 220P_0402_50V7K
@RF@ PC1107 0.022U_0402_25V7K
PC1123 33U_25V_NC_6.3X4.5
PC1122 33U_25V_NC_6.3X4.5
EMI@ PL1103 HCB2012KF-121T50_0805
@EMI@ PL1104 HCB2012KF-121T50_0805
B+

PL1102 0.15UH_PCME064T-R15MS_36A_20%
+CPU_CORE
PR1109 3.65K_0603_1%
@EM@PR1107 4.7_1206_5%
@EM@PC1110 680P_0603_50V7K

+CPU_CORE



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: **PWR-PROCESSOR DECOUPLING**

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Remark:
1. Switching frequency setting:(Ton pin)
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)
=448Khz

2. Soft-Start:(SS pin)
SS time (Internal) is 0.7ms (PC18 un-pop)
SS time(External): (PC18 pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms

4.Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(20-1.028)*1.028/(448Khz*0.22u*20)=9.89A

OCP=54A/2=27A per phase
Ivalley=27A-9.89A/2=22.055A

H-side MOS:TPCA8065
Rds(on):
11.7mohm@Vgs=10V
9.4mohm@Vgs=4.5V
Id :16A@Ta=25 degC

L-side MOS:TPCA8057
Rds(on):
2.0mohm@Vgs=10V
2.6~3.2mohm@Vgs=4.5V
Id :42A@Ta=25 degC

Choke: 0.36uH (Size:10*10*4)
Rdc=1.1mohm +-5%
Heat Rating Current=30A
Saturation Current=50A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=9.89A*3mohm=29.67mV

3.PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B
Vmin		0.6V	0.6V
Vmax		1.2V	1.2V
Vboot		0.875V	0.9V
Voltage step		6.25mV	6.25mV
N of Voltage level		96	96
Rrefadj	PR806	39K	20K
Rref1	PR803	39K	20K
Rboot	PR805	1.5K	2K
Rref2=PR20+PR21	PR809	30K	18K
	PR812	1.5K	0
C	PC829	1.5nf	2.7nf

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

5.OpenVReg Configurations:(PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 2V
Active phase with CCM	2.4V to 5.5V

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

20130909
1. Change net name to GPU_PWR_EN from DGPU_PWR_EN
2.Unpop PR801 0_0402_5%
3.Add PR824 10K_0402_5% to pull high to +3VS_VGA
4.Reserve PC834 5600P_0402_50V7K SE000009C80
20131024
1.Change PR814 pull high to +5VALWS from +5VS

20130905
Change PC816
to SE00000M000 S CER CAP 22U 6.3V M X5R 0603
from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

+VGA_CORE Under GPU Core GB2-64 package

+VGA_CORE Near GPU Core

PSI Pull high on HW side

Pull high on HW side

Rref1 Rboot Rrefadj Rref2 C Rocset Rton Csst

RT8812AGQW_WQFN20_3X3

+VGA_CORE
EDP-Continuous 33.5A
EDP-Peak 51.5A
OCP min 62A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title PWR-+VGA_CORE

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.

Title: PIR (PWR)

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