LCFC Confidential

Yoga C740 MB Schematic Document

CometLake_U42 with DDR4

2018-08
REV:0.1

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: Cover Page		
Size: C	Document Number: FYG41	Rev: 0.1
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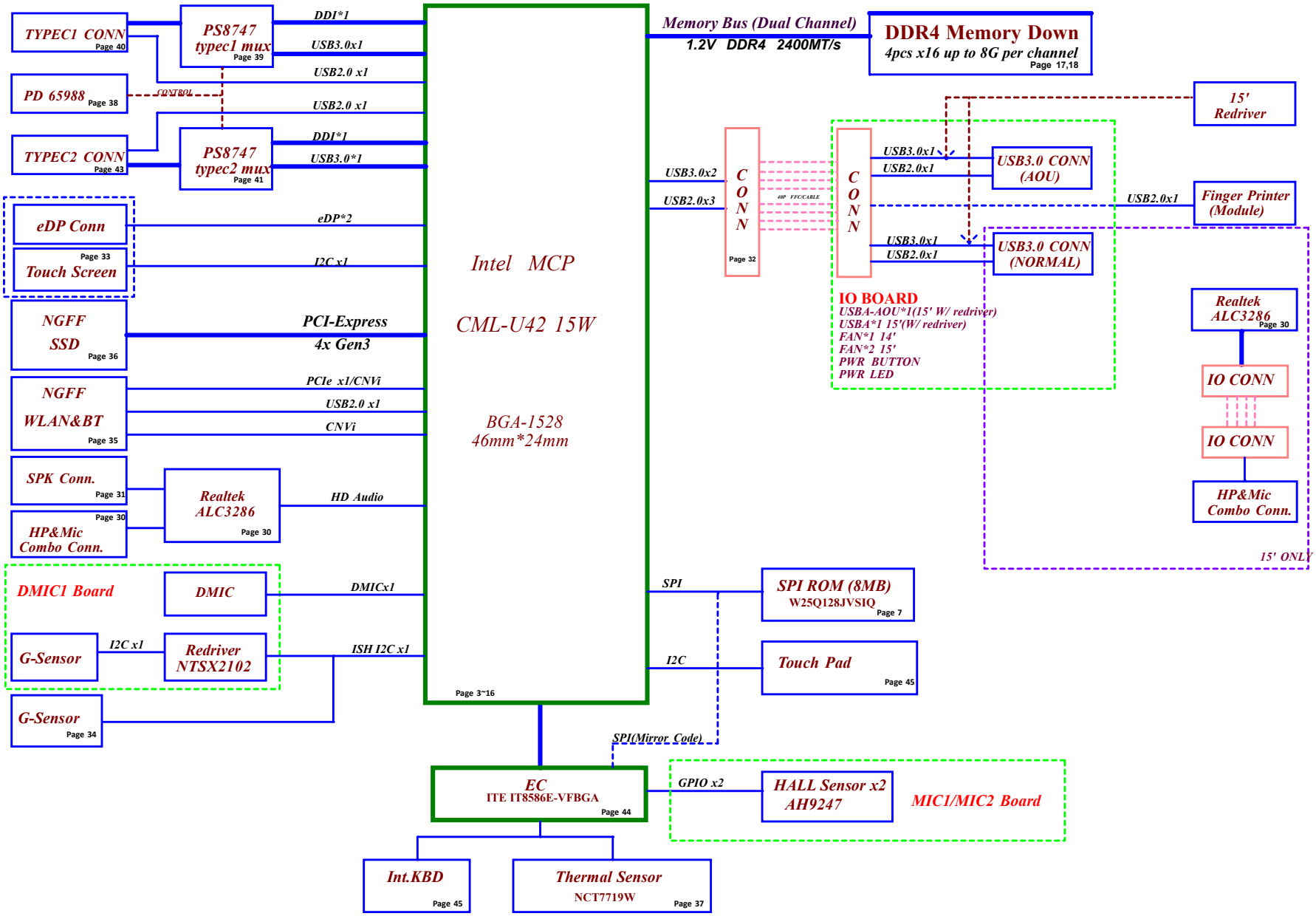

Security Classification	LC Future Center Secret Data		
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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCSA +0.6VS	+VCCIO +VCC_GT +VCCSTG +CPU_CORE +VCCPLL_OC VCC_PRIM_CORE
S0	O	O	O	O	O
S0IX	O	O	O	O	X
S3	O	O	O	X	X
S3 Battery only	O	O	O	X	X
S5 S4 AC Only	O	O	X	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
BL@	For KB backlight part
EMC@	For EMC part
EMC_14@	For EMC 14" part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME@
MP@	For MP part
NPI@	For NPI part
CNVI@	For CNVI WLAN
DDP@	For DDP MD part
SDP@	For SDP MD part
RF@	For RF part
RF_NS@	For RF un-stuff part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	VR	Thermal Sensor	WLAN WiMAX	PD
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	V	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	X	V +3VS	X	X	X	X	V	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X	V
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	X	X	X	X	X	X

HSIO PORT		Function
USB3.0	1	USB Type-C1
	2	USB Type-A AOU
	3	USB Type-A
	4	USB Type-C2
	5	NC
	6	NC
USB2.0	1	USB Type-A AOU
	2	USB Type-A
	3	NC
	4	Finger Printer
	5	NC
	6	NC
	7	CAMERA
	8	USB Type-C1
	9	USB Type-C2
	10	BT
PCIE	1~8	1~4 SUB3.0 5~4 NC
	9	WLAN
	10~12	NC
	13~16 X4	SSD-2

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001_001xb
PMIC	0x34

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7719W)	1001_100xb

EC SMBus3 address

Device	Address
PD	0100_111xb

PCH SM Bus address

Device	Address

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Title: **Notes List**

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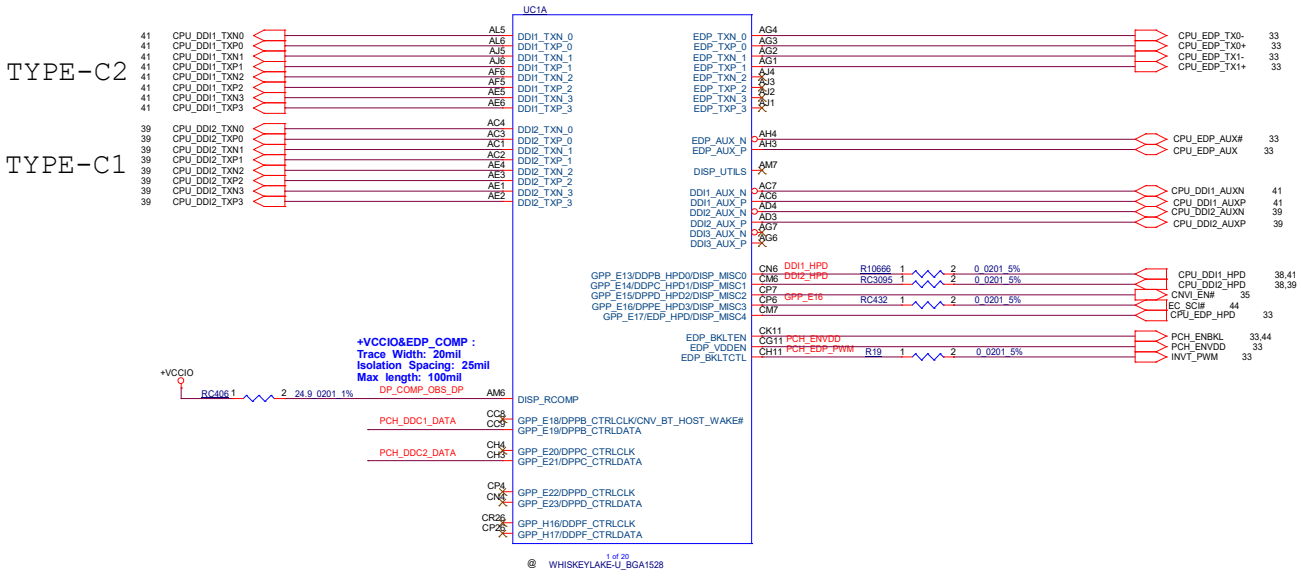
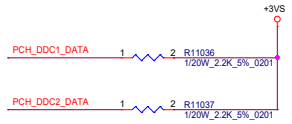


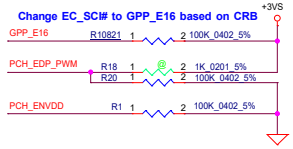
DDP*_CTRLDATA strapping sampled on the rising edge of PCH_PWROK

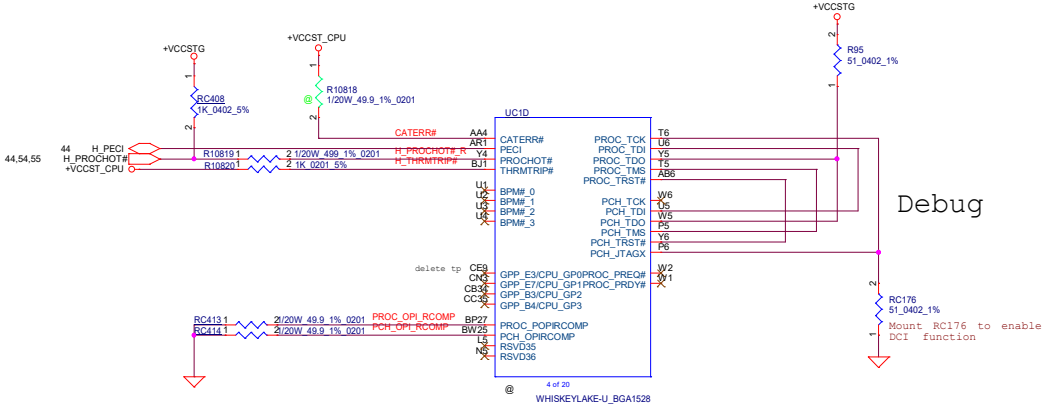
Port	Strap	Enable	Disable
Port 1	GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Pull up to 3.3 V with 2.2Kohm ★	NC
Port 2	GPP_E21 / DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm ★	NC
Port 3	GPP_E23 / DDPD_CTRLDATA	Pull up to 3.3 V with 2.2Kohm ★	NC
Reserve	GPP_H17/ DPFF_CTRLDATA	Pull up to 3.3 V with 2.2Kohm ★	NC

DDI enable: PCH_DDC1_DATA & PCH_DDC2_DATA need pull up
Reserve ddi_clk



Change EC_SC# to GPP_E16 based on CRB





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Title	MCP (DDI,EDP)		
Size	Document Number		Rev
C	Yoga C740		0.1
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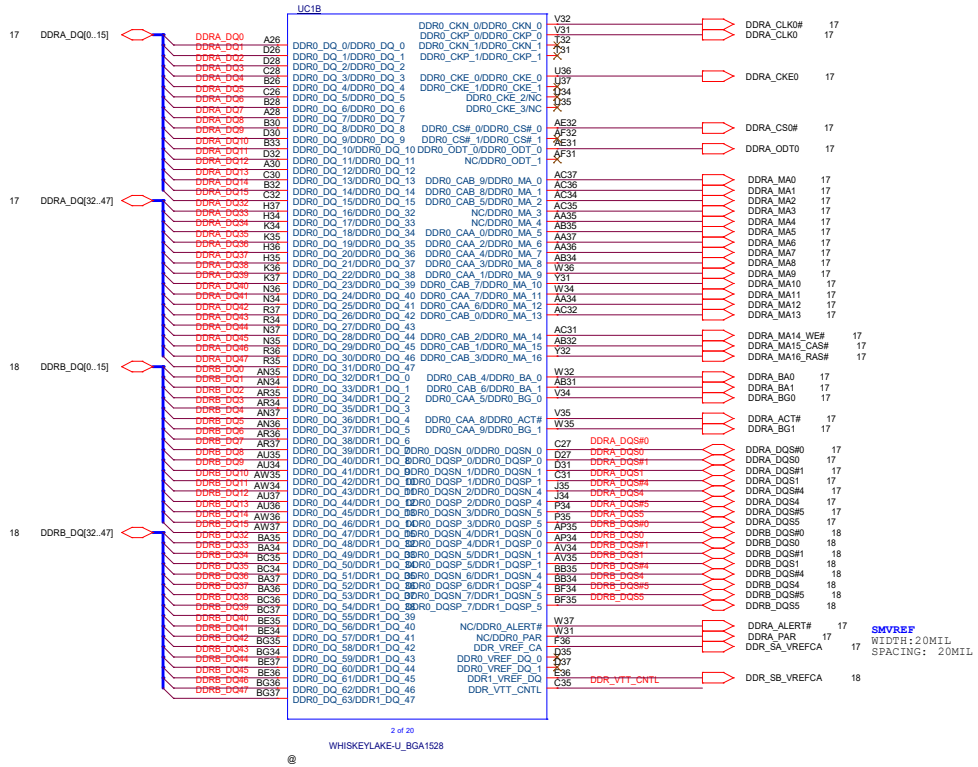

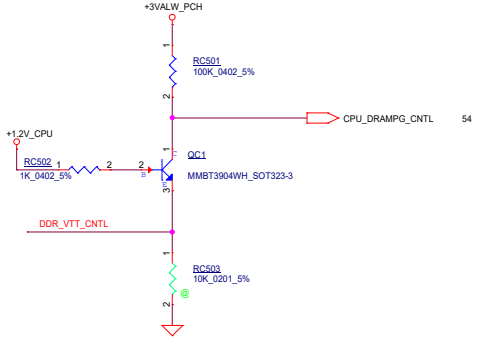

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	MCP (DDR4)		
Size	Document Number		Rev
C	Yoga C740		0.1
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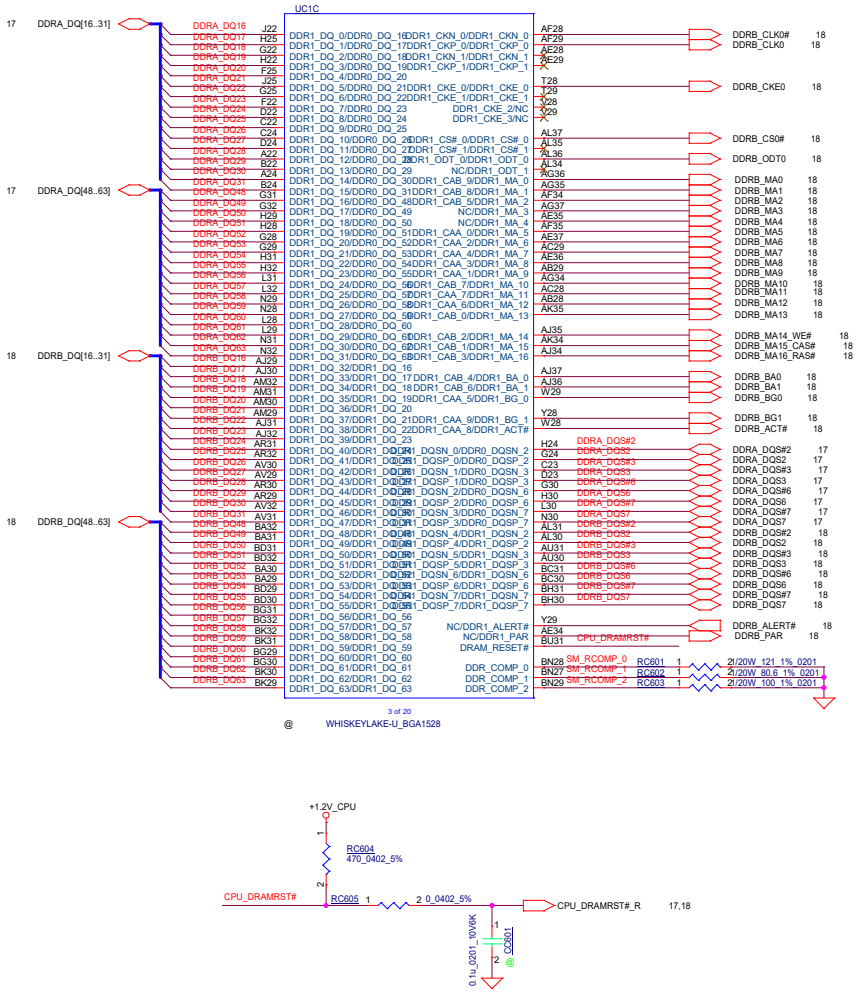

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: MCP (DDR4)

Size	Document Number	Rev
C	Yoga C740	0.1

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Security Classification	LC Future Center Secret Data		
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Title	MCP (JTAG,SPI,LPC,SMB)		
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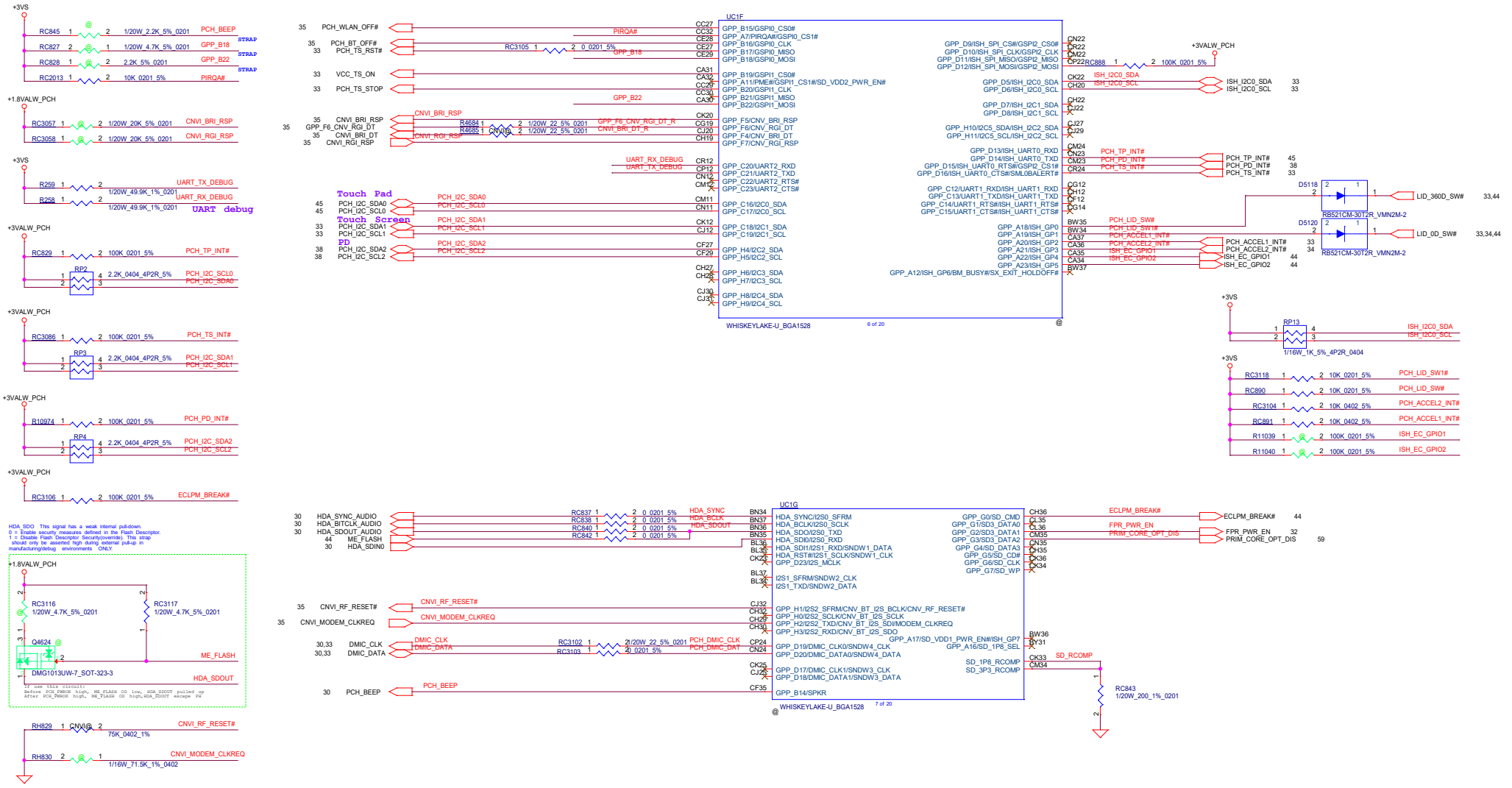
Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

Enable: PCH will disable the TCO Timer system reboot feature.
This function is useful when runing ITP/XDP



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: MCP (LPSS,ISH,AUDIO,SDIO)

Size	Document Number	Rev
C	Yoga C740	0.1

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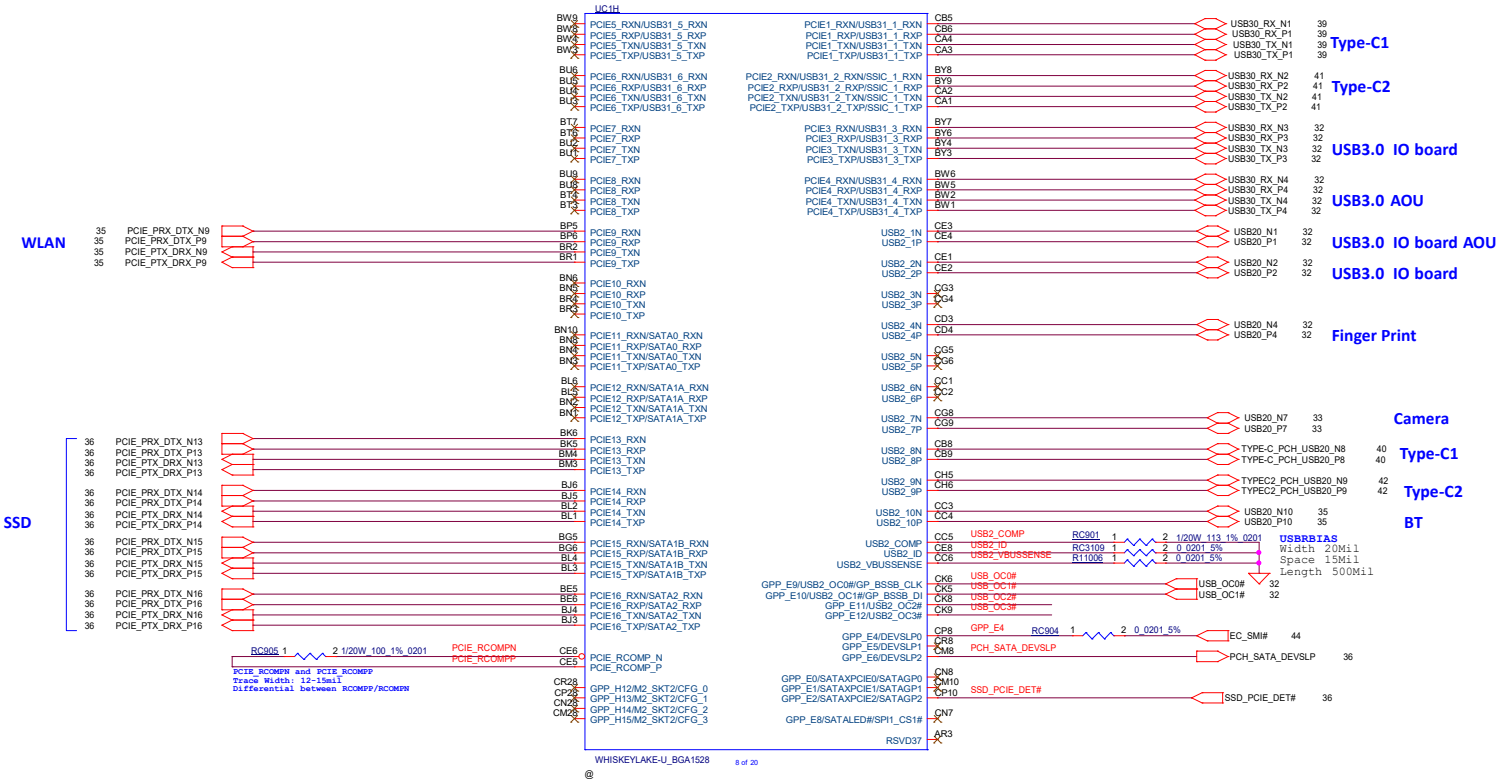

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	MCP (PCIE,SATA,USB3,USB		
Size C	Document Number Yoga C740		Rev 0.1
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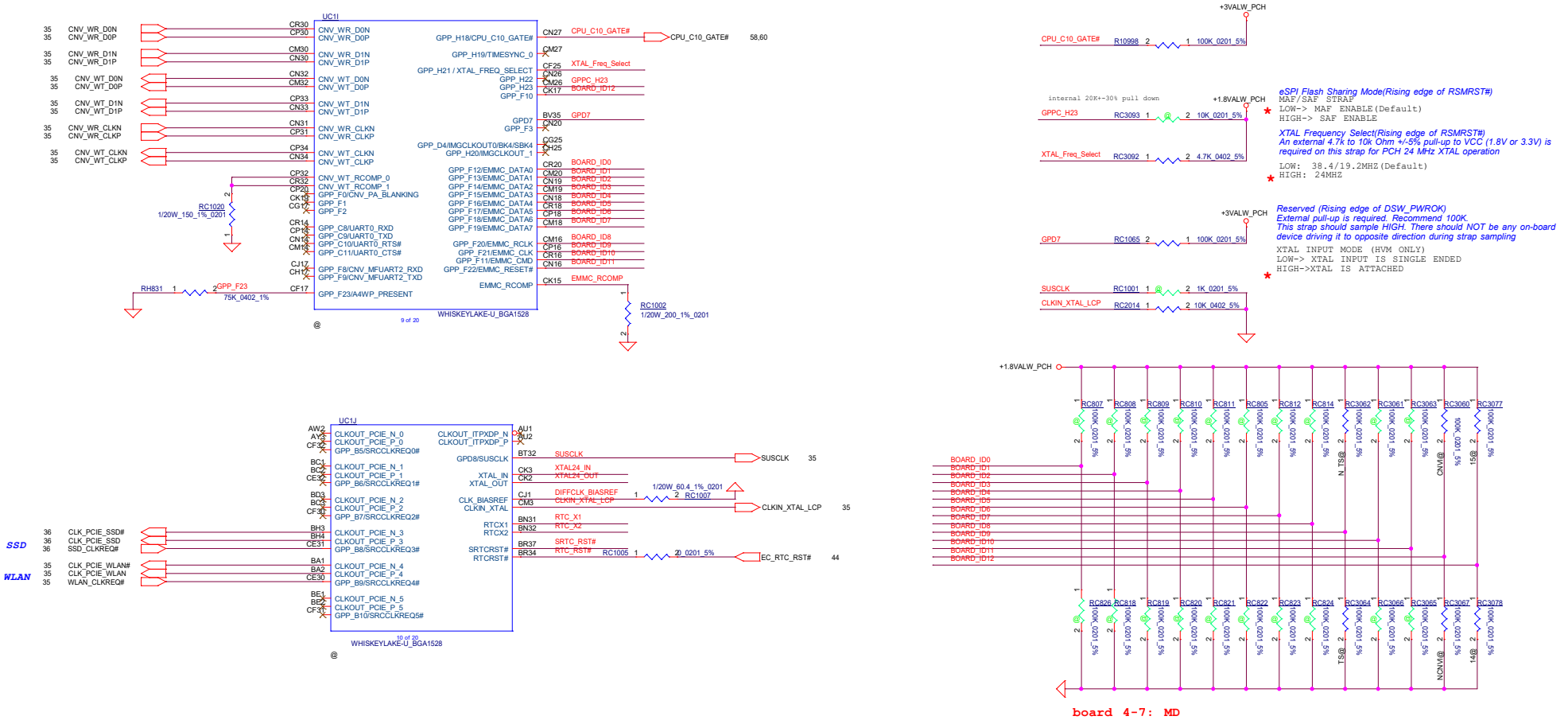

Security Classification	LC Future Center Secret Data		
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Title	MCP (CNVI,CLOCK)		
Size C	Document Number	Yoga C740	Rev 0.1
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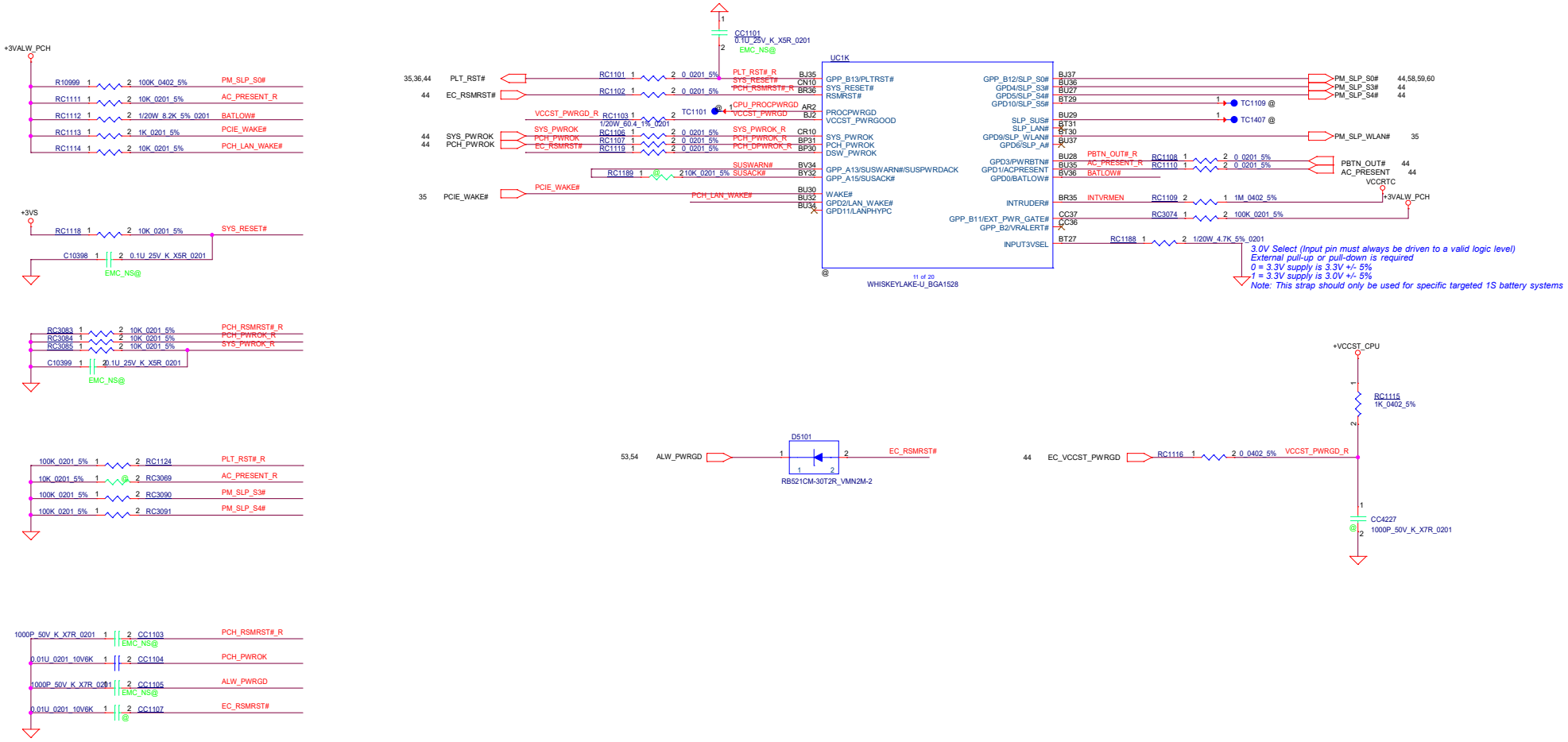

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	MCP (SYSTEM PWR MANAGEMENT)		
Size C	Document Number		Rev 0.1
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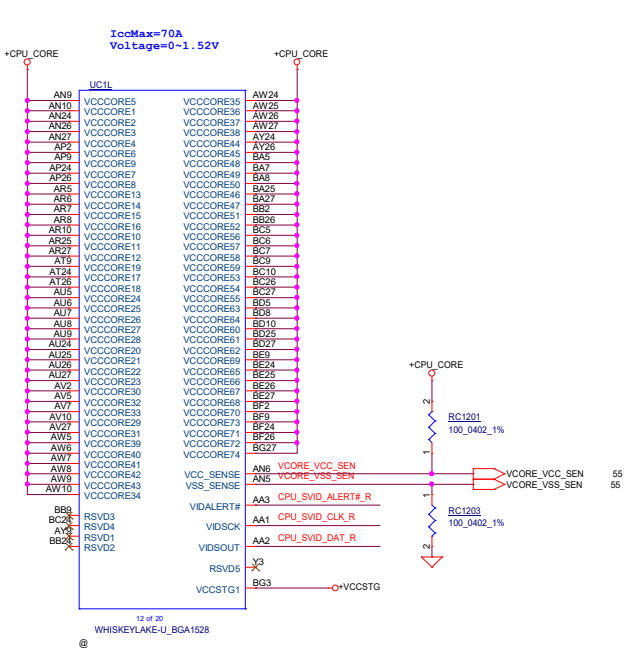

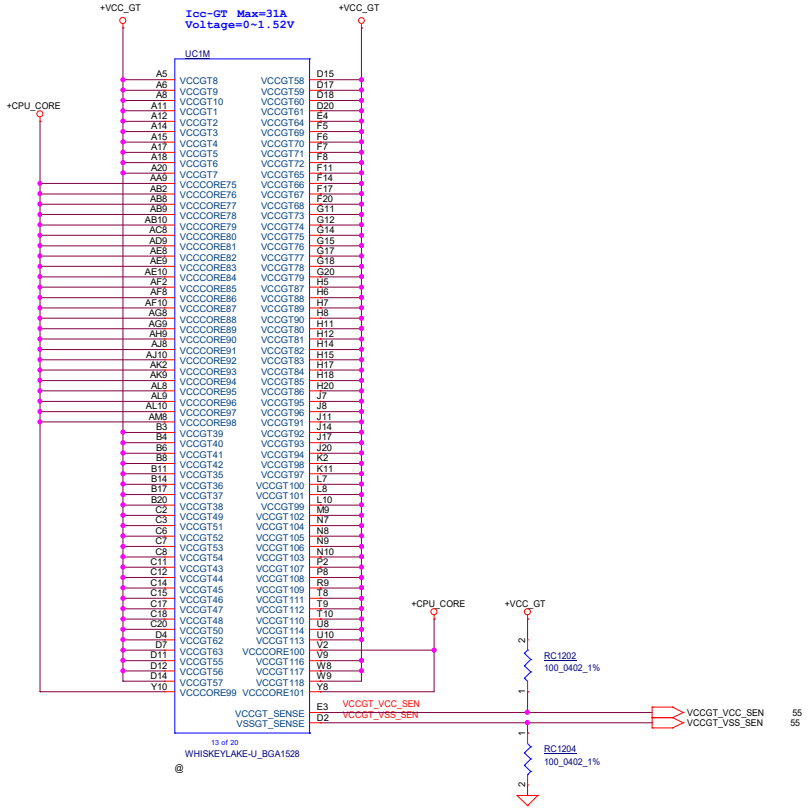

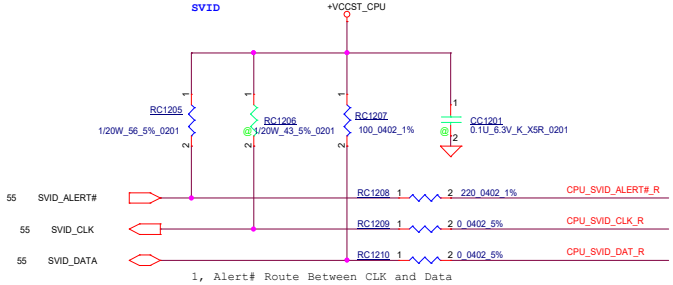

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2017/12/13

Title	MCP (CPU PWR1)		
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C	Yoga C740		0.1
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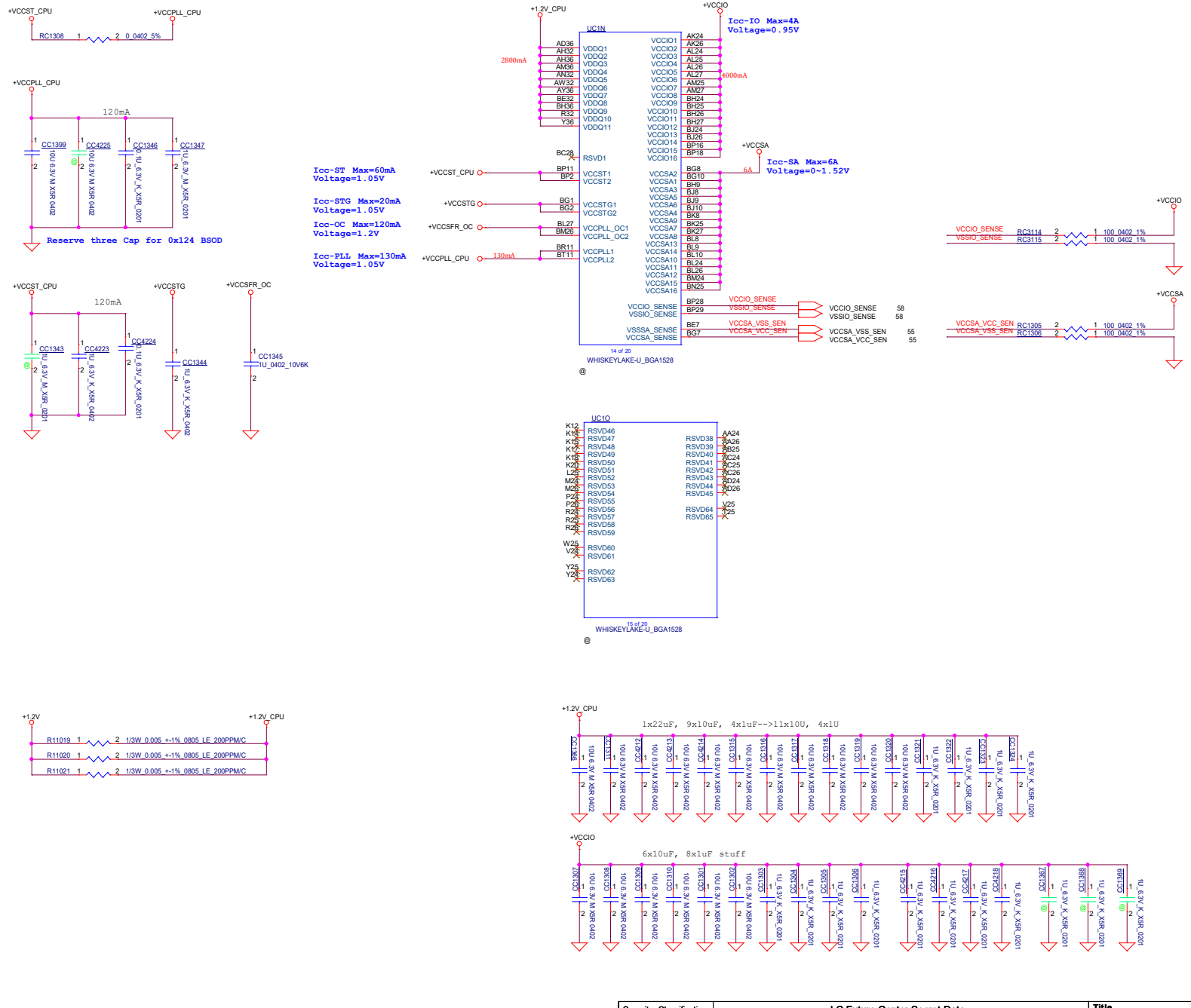

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: MCP (CPU PWR2)

Size	Document Number	Rev
C	Yoga C740	0.1

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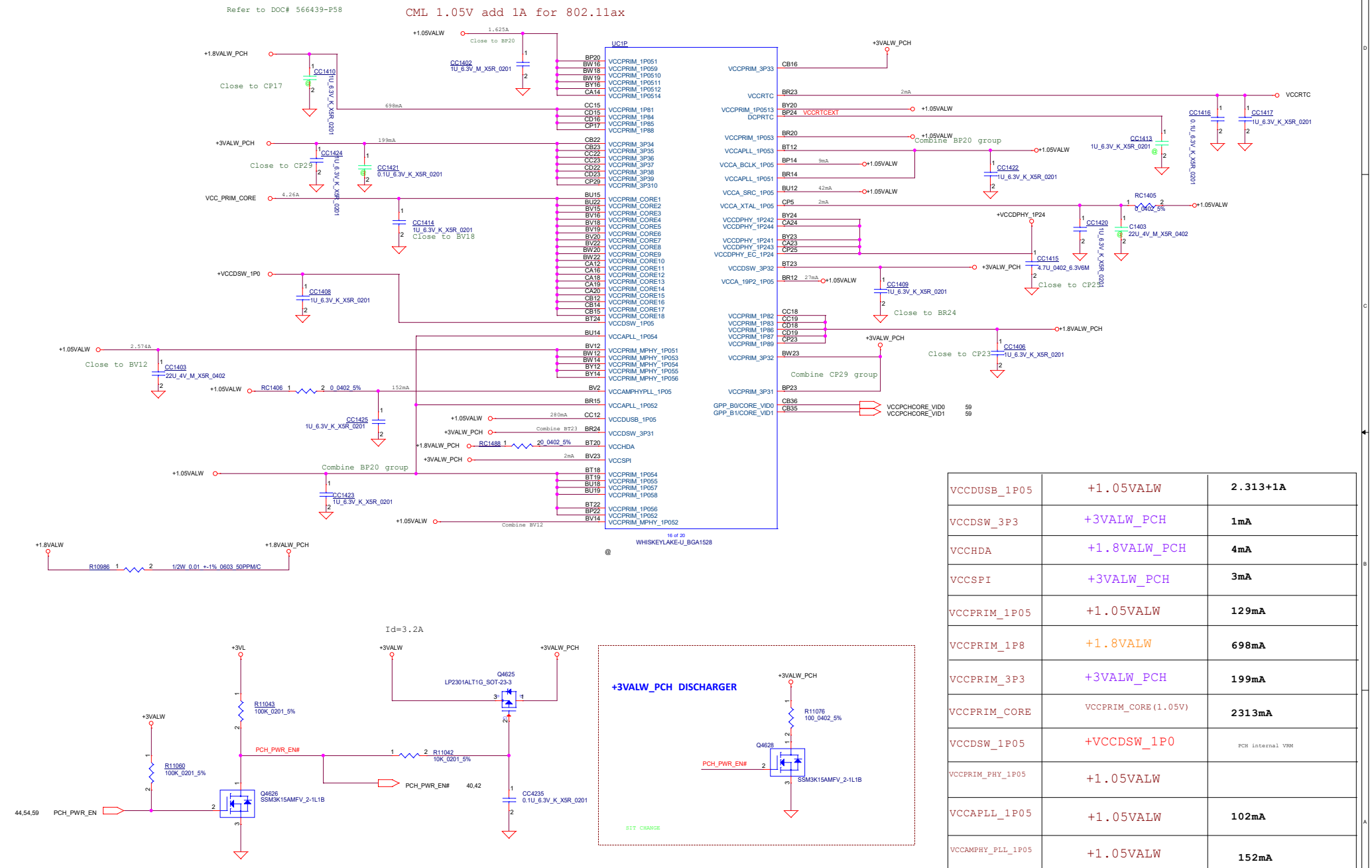

VCCDUSB_1P05	+1.05VALW	2.313+1A
VCCDSW_3P3	+3VALW_PCH	1mA
VCCHDA	+1.8VALW_PCH	4mA
VCCSPI	+3VALW_PCH	3mA
VCCPRIM_1P05	+1.05VALW	129mA
VCCPRIM_1P8	+1.8VALW	698mA
VCCPRIM_3P3	+3VALW_PCH	199mA
VCCPRIM_CORE	VCCPRIM_CORE(1.05V)	2313mA
VCCDSW_1P05	+VCCDSW_1P0	PCH internal VRM
VCCPRIM_PHY_1P05	+1.05VALW	
VCCAPLL_1P05	+1.05VALW	102mA
VCCAMPHY_PLL_1P05	+1.05VALW	152mA

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Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	MCP (PCH PWR)		
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C	Yoga C740		0.1
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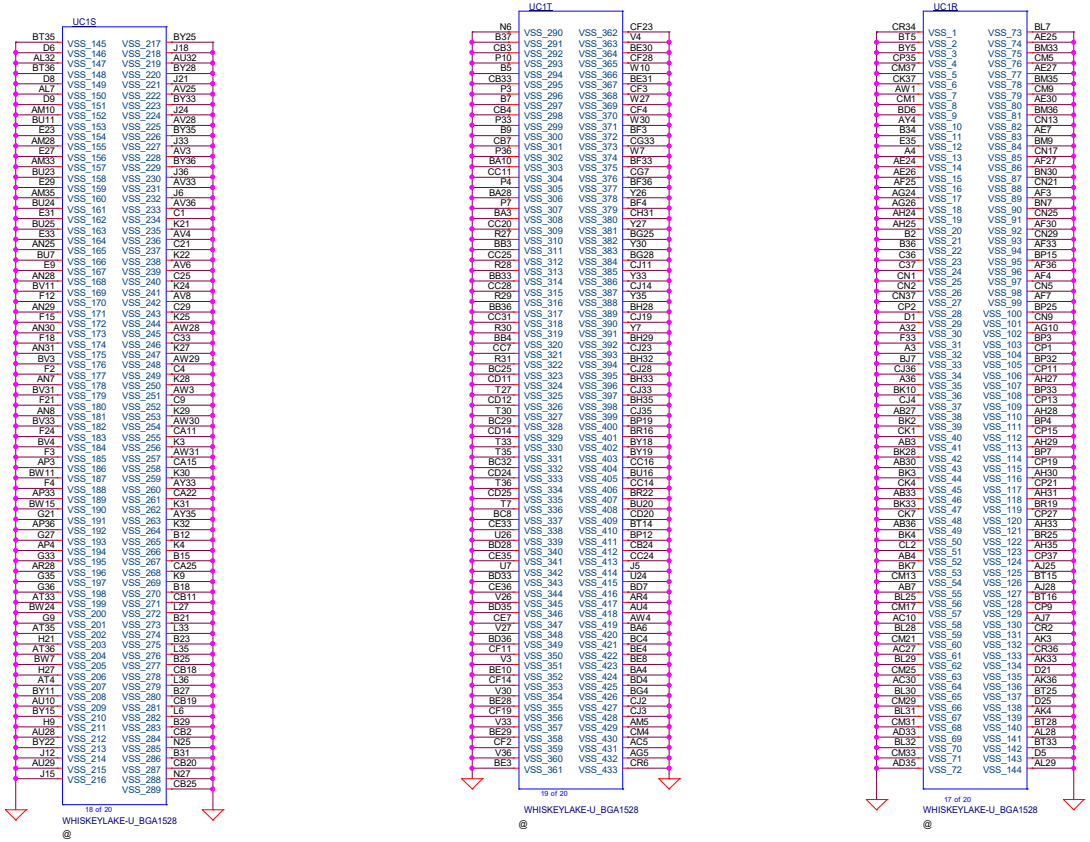

Security Classification	LC Future Center Secret Data		
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Title: **MCP (VSS)**

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C	Yoga C740	0.1

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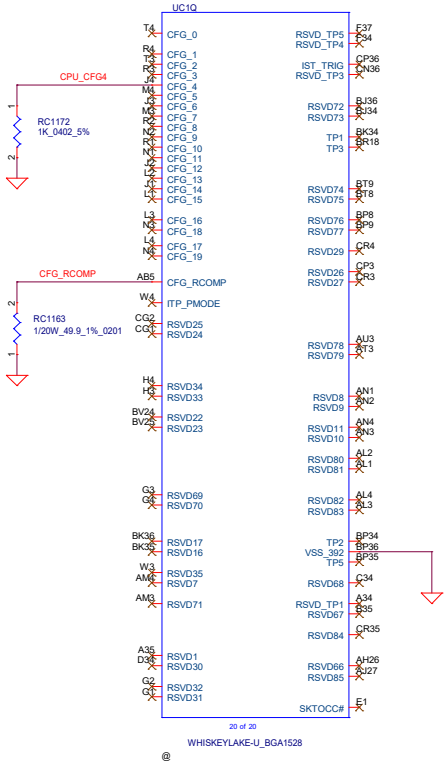

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Title: **MCP CFG**

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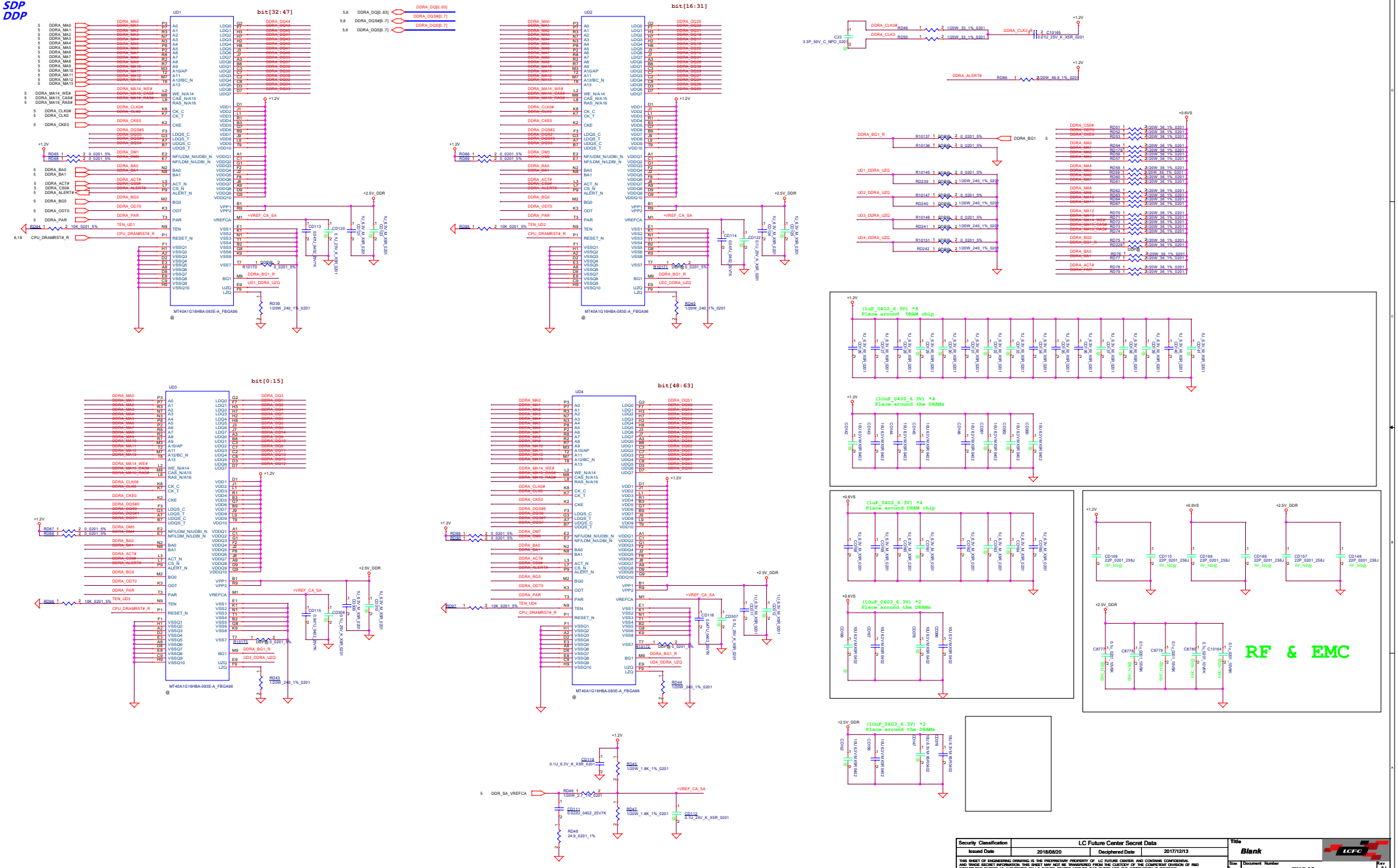
8Gb SDP
16Gb DDP



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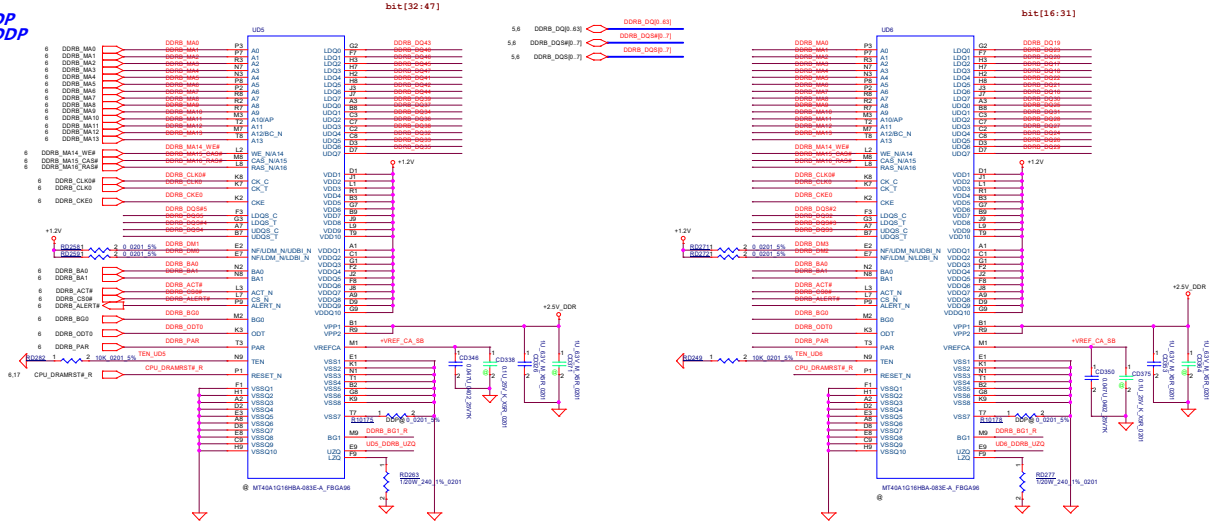
8Gb SDP
16Gb DDP



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Title	DDR4 SO-DIMM		
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Title

VGA Notes List

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Title

GPU_PCIE Interface

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Title

GPU_MEM Interface

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Title

GPU_+VGA_CORE,FBVDDQ

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Title

GPU_AON/MAIN PWR/SEQ

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Title

GPU_GND

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Title

GPU_STRAP/DP/HDMI

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Title

GPU_GPIO/JTAG

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Title

GPU_GDDR5_Rank0_[31:0]

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Title

GPU_GDDR5_Rank0_[64:32]

Size	Document Number	Rev
C	*FYG41*	0.1

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Title

GPU_MISC

Size	Document Number	Rev
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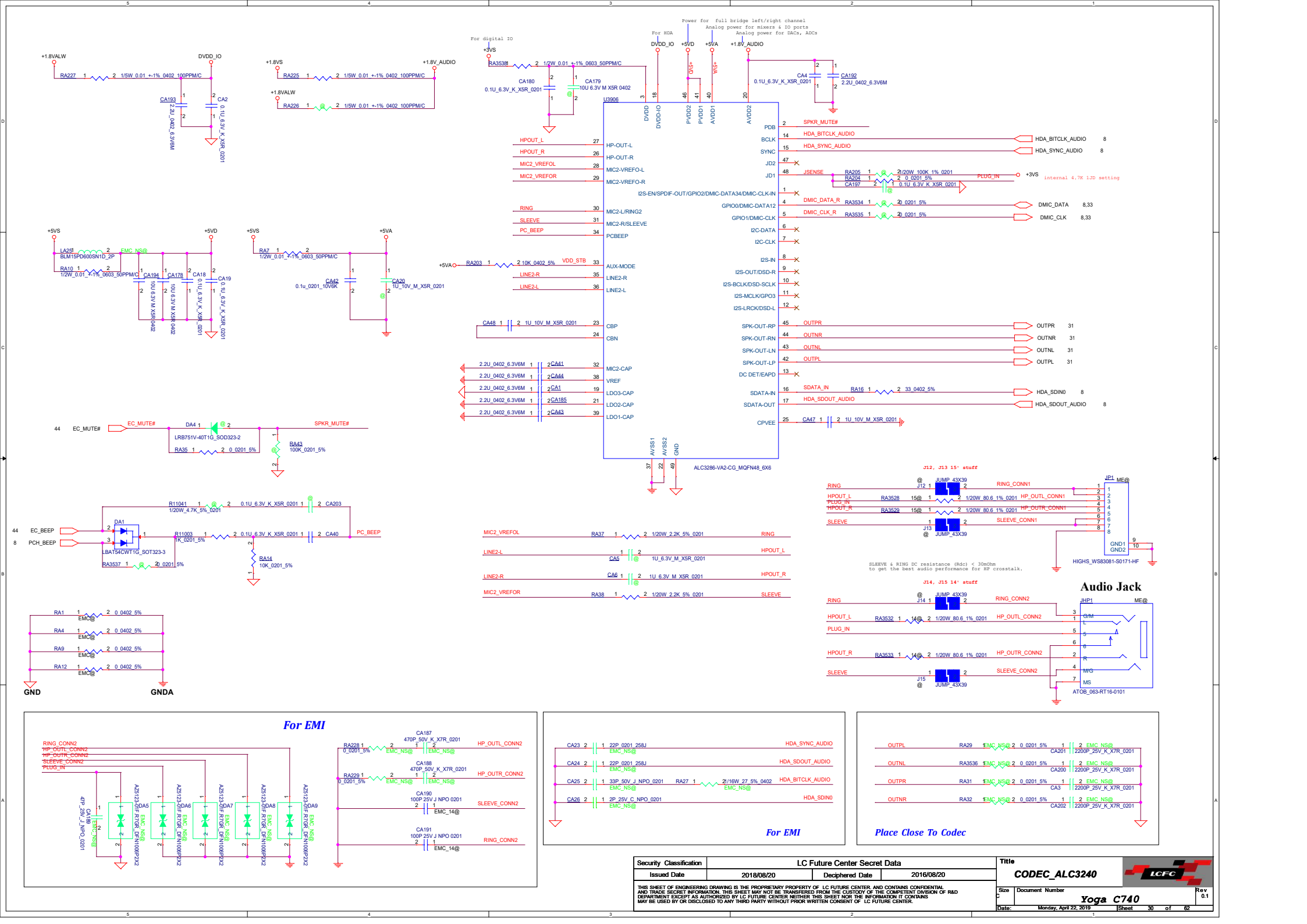

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Title	CODEC_ALC3240		
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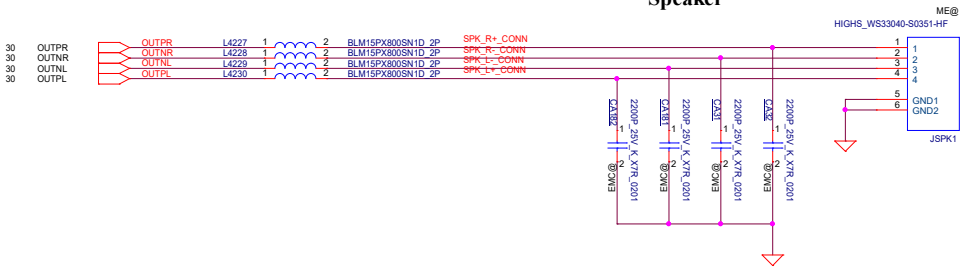
Internal Speaker connector
Placement near Audio Codec

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

Speaker



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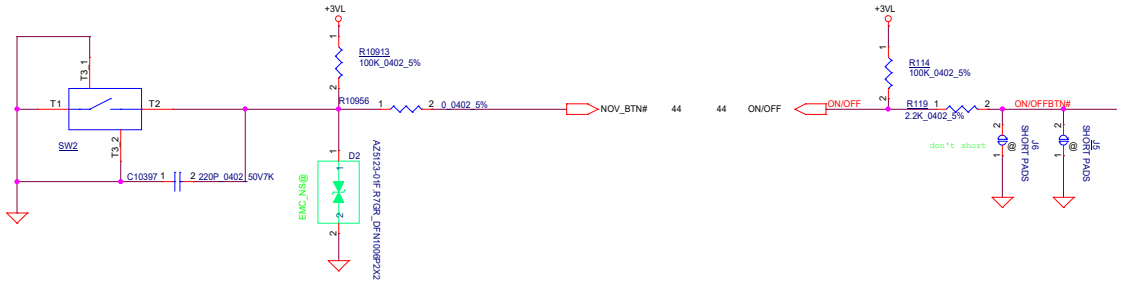
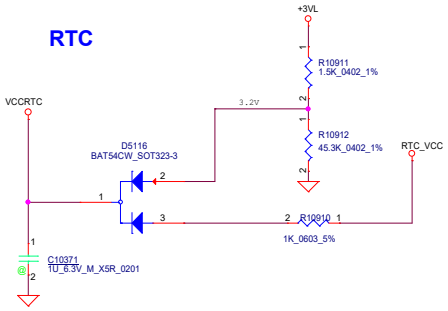
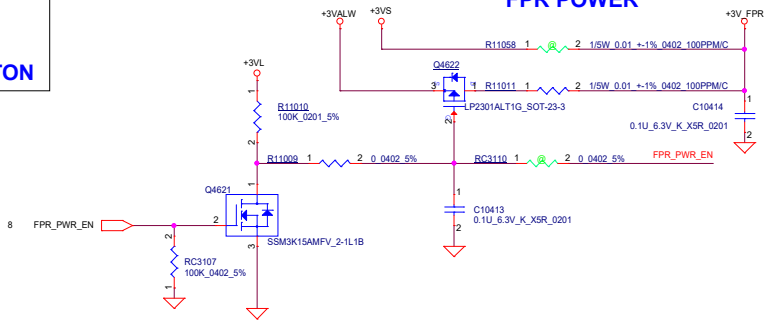
BUTTON



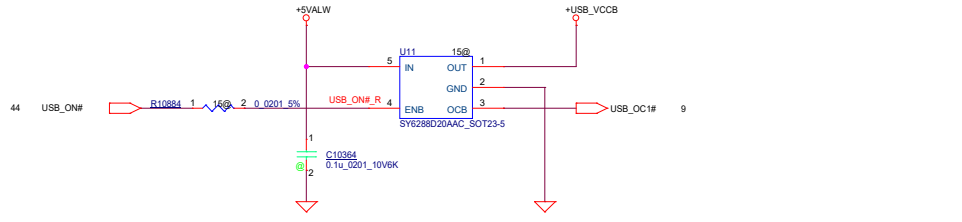
RTC



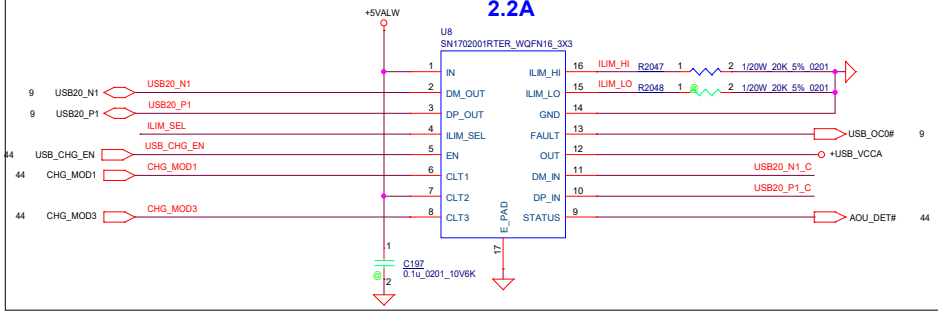
FPR POWER



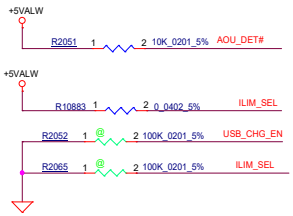
USB POWER SW

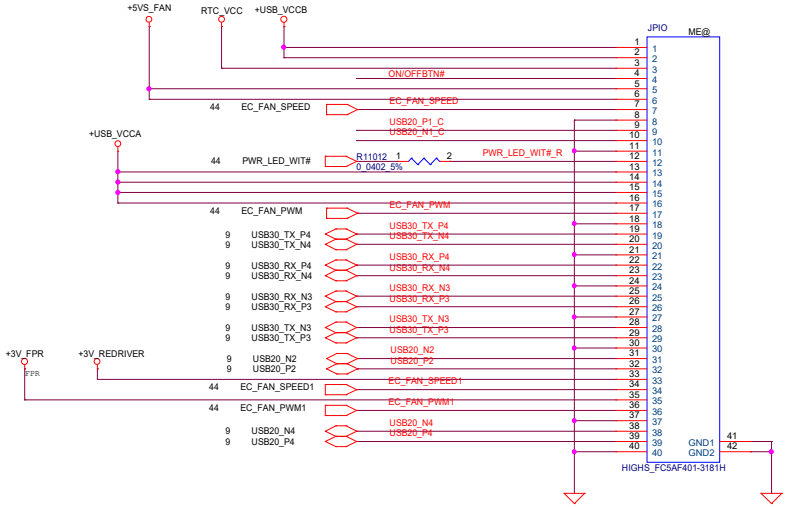


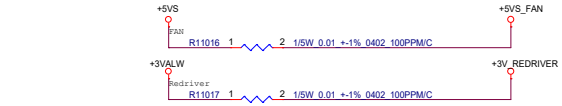
USB Charger 2.2A



	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
*	0	0	0	X	DCH	OUT held low
*	1	1	1	1	CDP	Data Connected and Load Detect Active
*	1	1	1	0	SDP2	Data Connected
*	1	1	0	X	SDP1	Data Connected
*	0	1	0	X	SDP1	Data Connected
*	1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
*	1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	DCP_Auto	Data Disconnected and Load Detect Active
*	0	0	1	X	DCP_Auto	Data Disconnected and Load Detect Active







Security Classification	LC Future Center Secret Data	
Issued Date	2018/08/20	Deciphered Date 2016/08/20

Title	I/O_DB_CONN		
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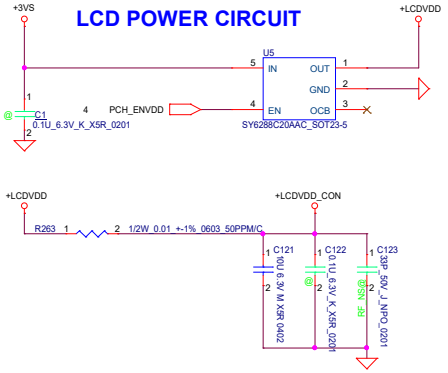
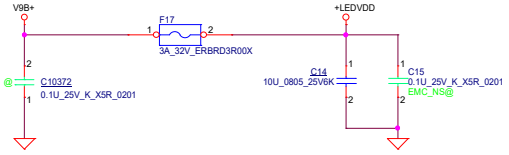
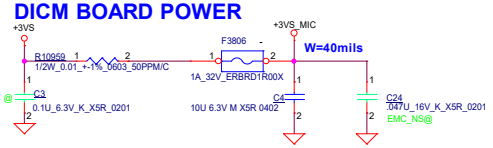
LCD POWER CIRCUIT

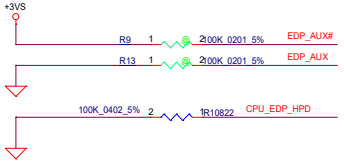


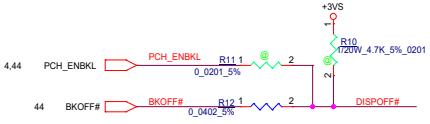
LED POWER

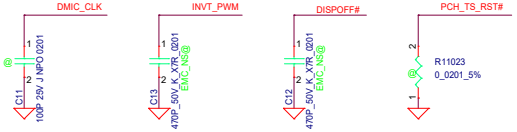


DICM BOARD POWER

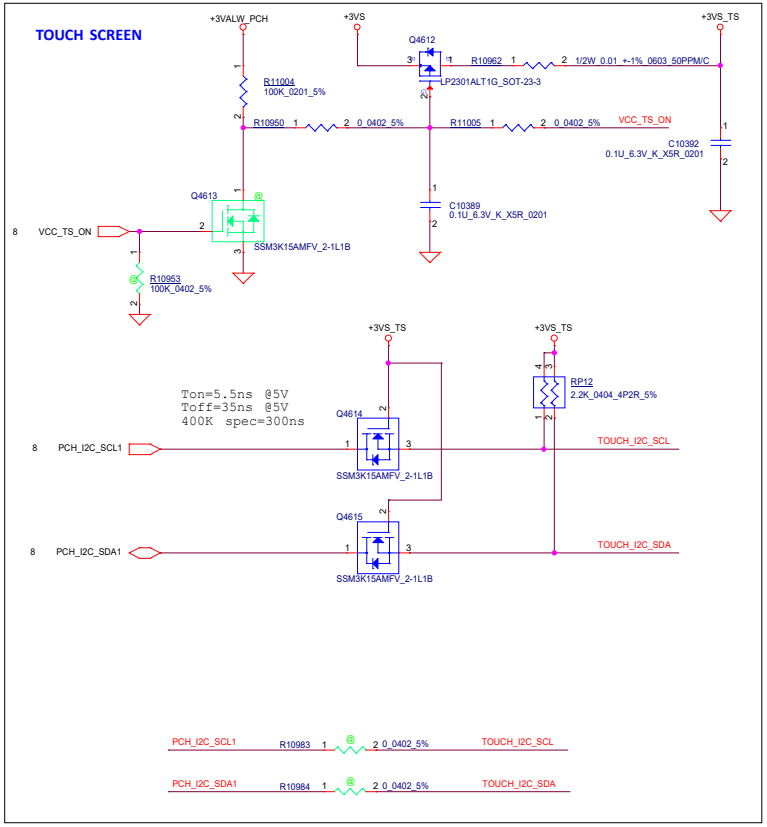




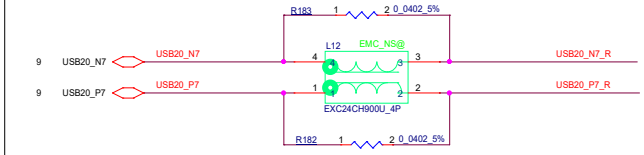




TOUCH SCREEN

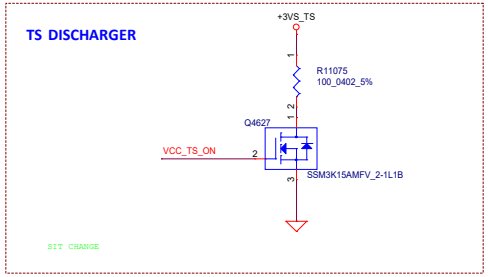


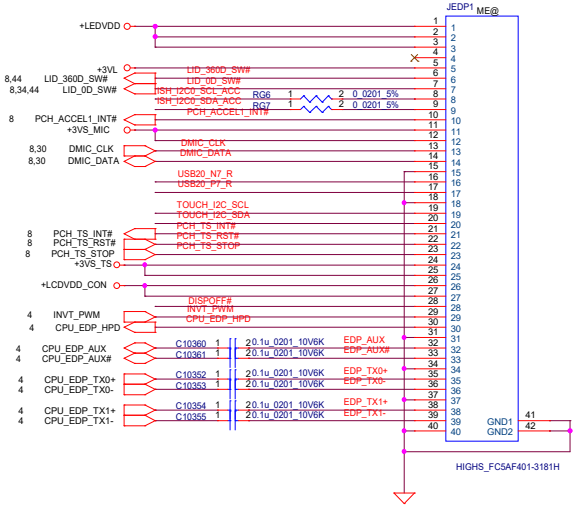
Camera



Sensor

TS DISCHARGER





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: eDP/CAMERA/TS_CONN

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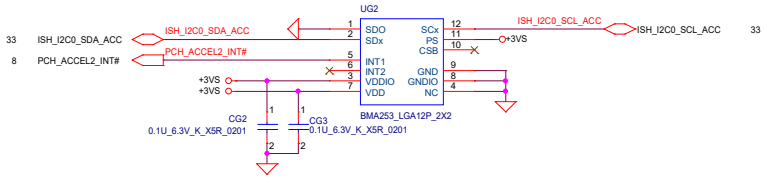
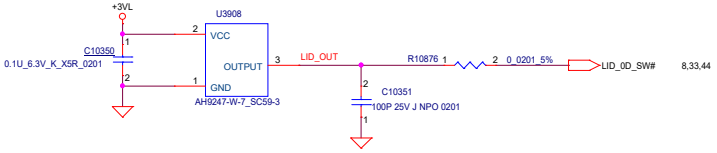
ACC-SENSOR



LID-SENSOR



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: **HALL/G Sensor**

Size	Document Number	Rev
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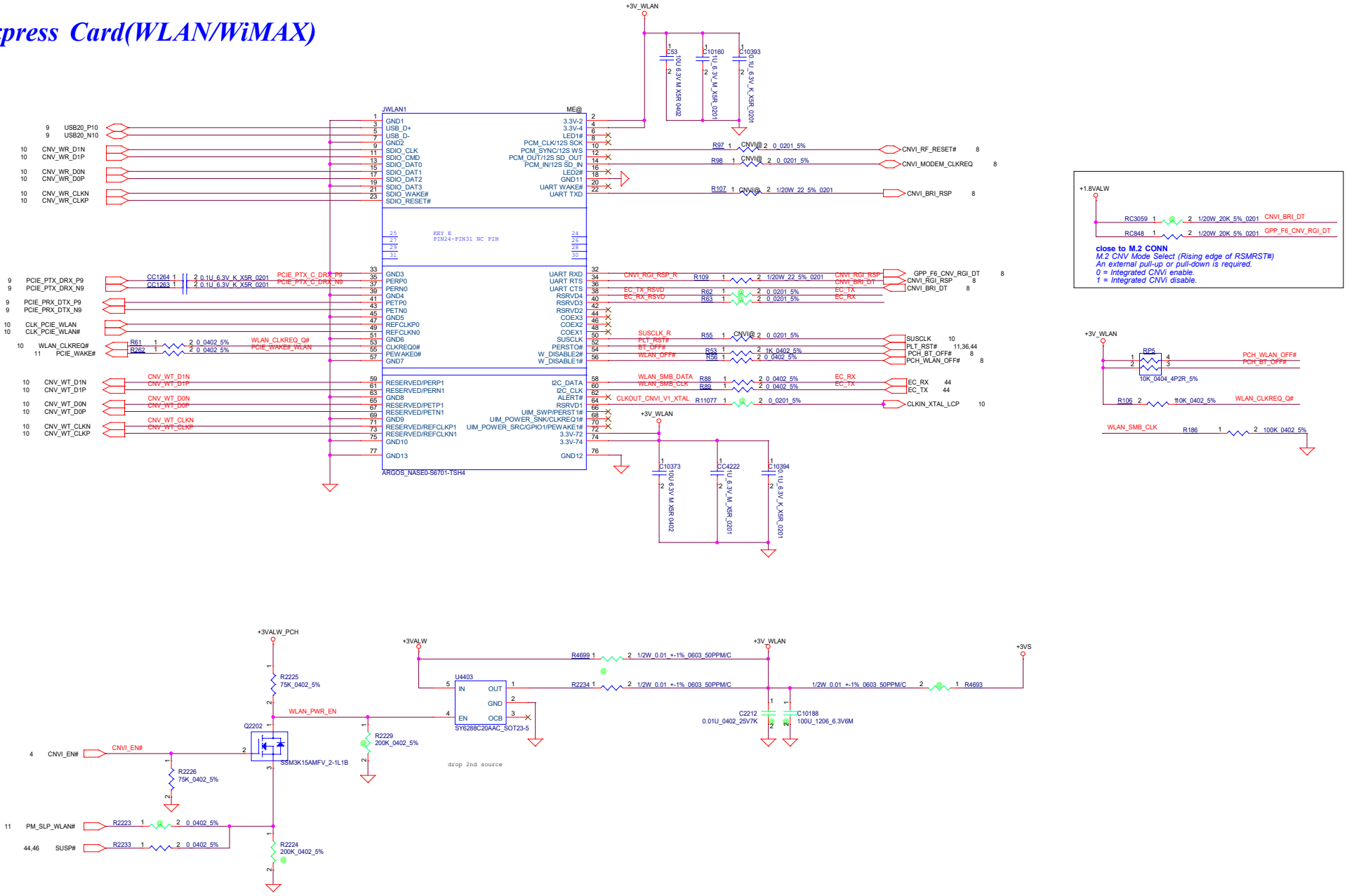
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2017/12/13

Title	NGFF_WLAN		
Size	Document Number		Rev
C	Yoga C740		0.1
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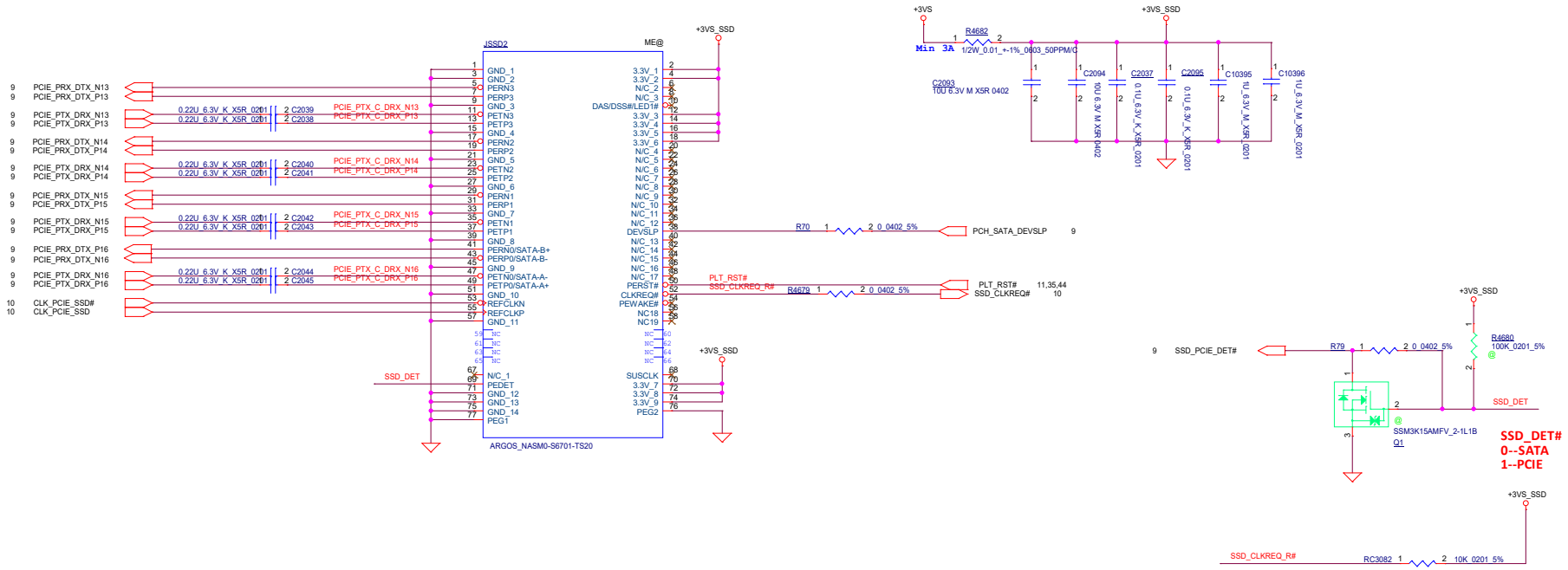

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: NGFF_SSD_1

Size	Document Number	Rev
C	Yoga C740	0.1

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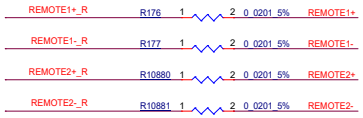

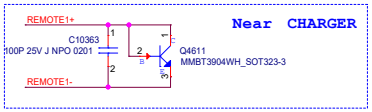

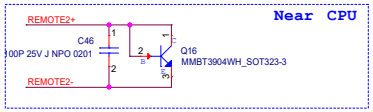

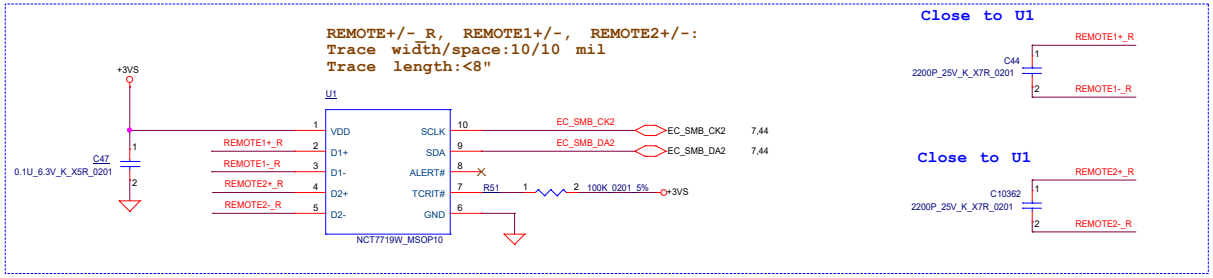

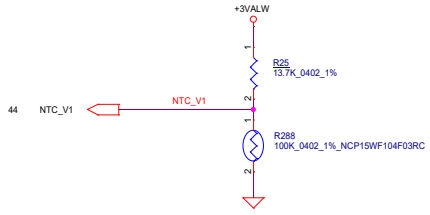

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2017/08/15

Title: **Thermal Sensor**

Size	Document Number	Rev
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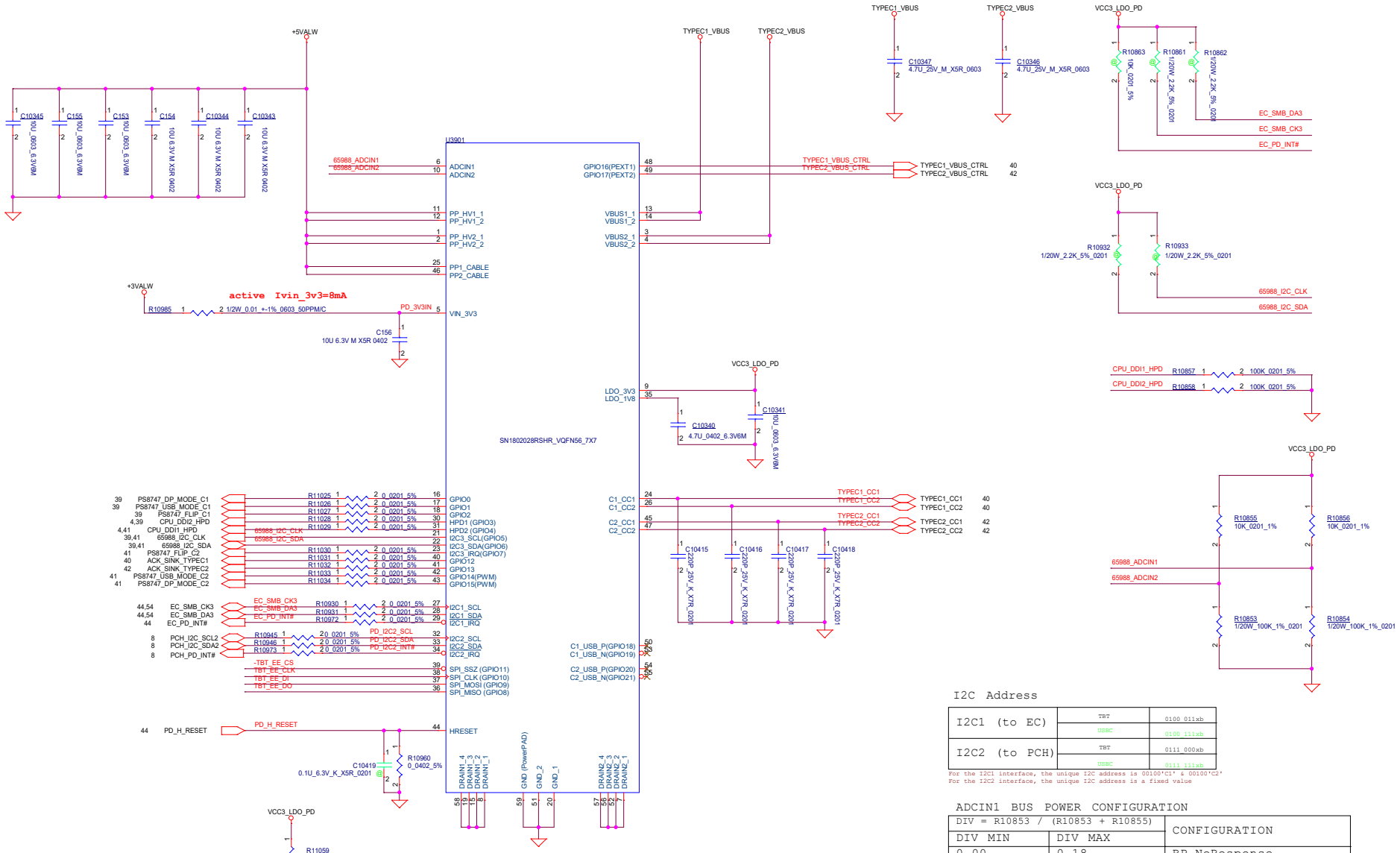

I2C Address

I2C1 (to EC)	TBT	0100 011xb
	USBC	0100 111xb
I2C2 (to PCH)	TBT	0111 000xb
	USBC	0111 111xb

For the I2C1 interface, the unique I2C address is 0100'C1' & 0100'C2'
For the I2C2 interface, the unique I2C address is a fixed value

ADCIN1 BUS POWER CONFIGURATION

DIV = R10853 / (R10853 + R10855)		CONFIGURATION
DIV MIN	DIV MAX	
0.00	0.18	BP_NoResponse
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

For dear battery mode

ADCIN2 I2C Address Setting

DIV = R10854 / (R10854 + R10856)		I2C Unique Address [3:1]	
DIV MIN	DIV MAX	ADC_ADDR_DECODE_C1	ADC_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	PD TPS65988		
Size	Document Number		Rev
C	FYG41		0.1
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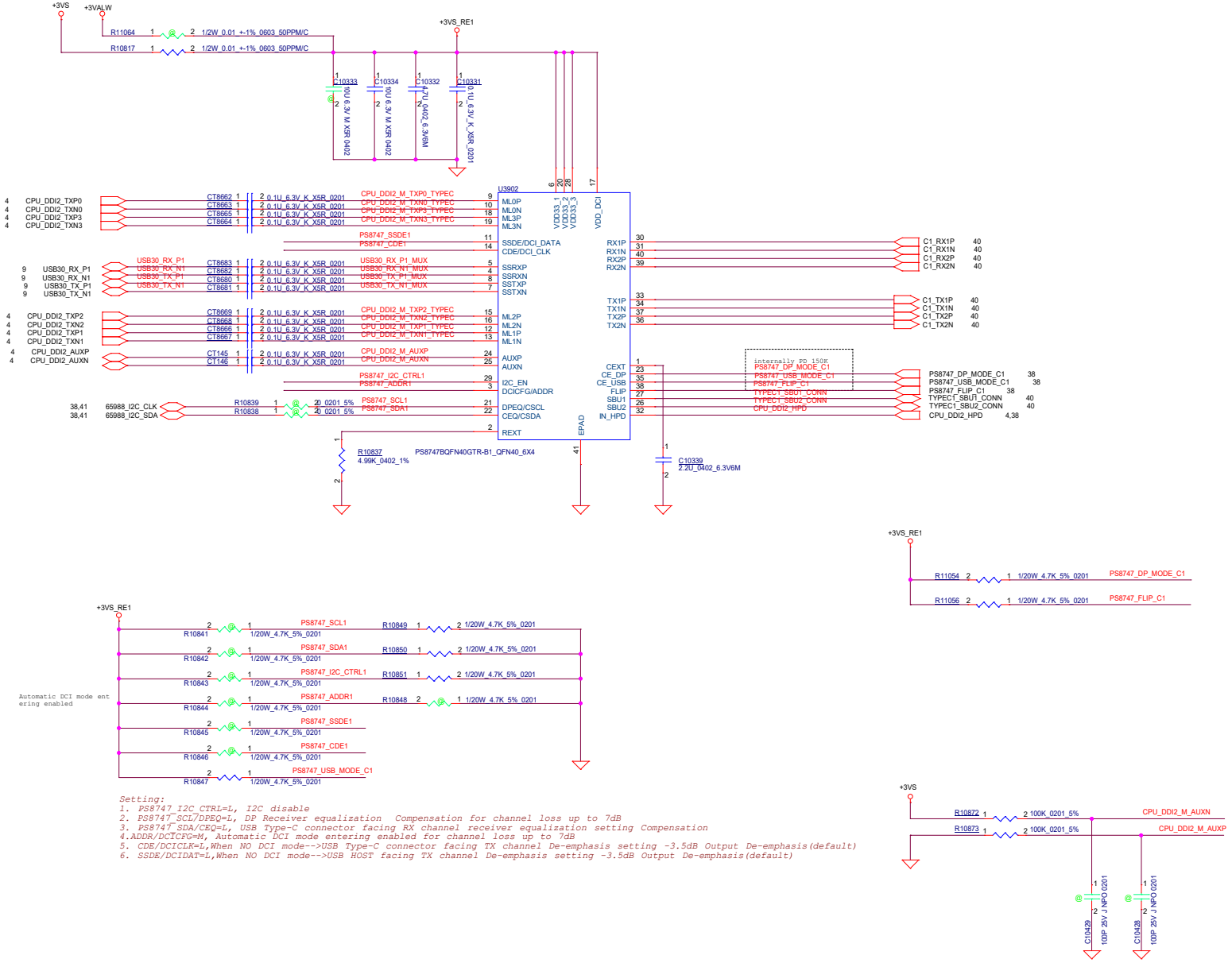

Setting:
1. PS8747_I2C_CTRL=L, I2C disable
2. PS8747_SCL/DPEQ=L, DP Receiver equalization Compensation for channel loss up to 7dB
3. PS8747_SDA/CEQ=L, USB Type-C connector facing RX channel receiver equalization setting Compensation
4.ADDR/DCICFG=M, Automatic DCI mode entering enabled for channel loss up to 7dB
5. CDE/DCICLK=L,When NO DCI mode-->USB Type-C connector facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)
6. SSDE/DCIDAT=L,When NO DCI mode-->USB HOST facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)

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Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title			
TYPE-C_RTS5448			
Size: C	Document Number: Yoga C740		Rev: 0.1
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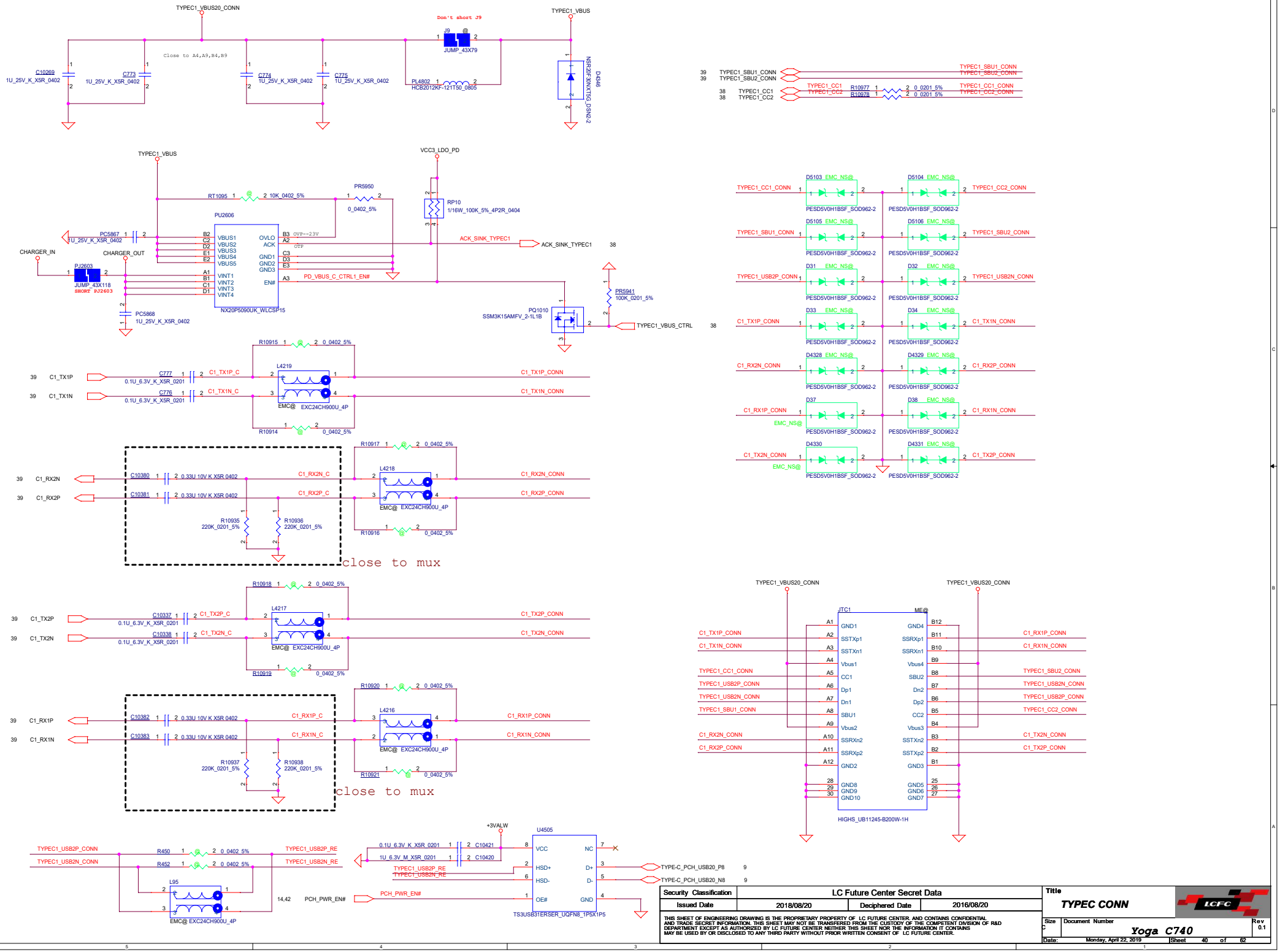

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: TYPEC CONN

Size	Document Number	Rev
C	Yoga C740	0.1

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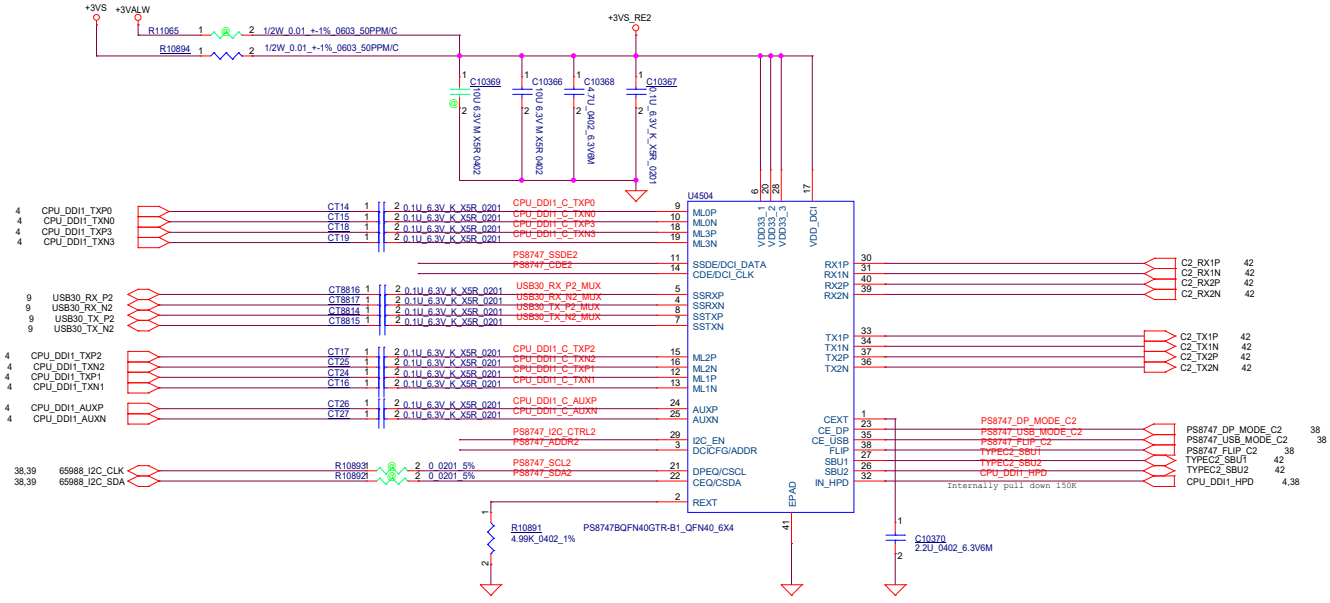
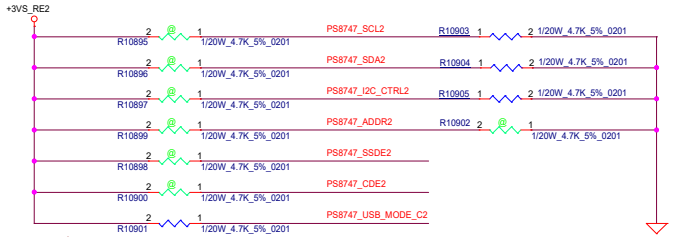
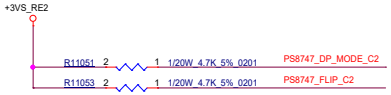
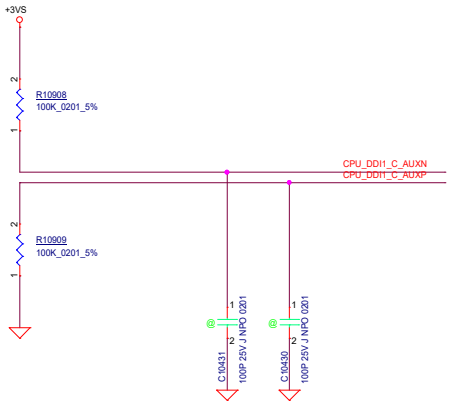






Setting:
1. PS8747_I2C_CTRL=L, I2C disable
2. PS8747_SCL/DPEQ=L, DP Receiver equalization Compensation for channel loss up to 7dB
3. PS8747_SDA/CEQ=L, USB Type-C connector facing RX channel receiver equalization setting Compensation
4.ADDR/DCICFG=M, Automatic DCI mode entering enabled for channel loss up to 7dB
5. CDE/DCICLK=L,When NO DCI mode-->USB Type-C connector facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)
6. SSDE/DCIDAT=L,When NO DCI mode-->USB HOST facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	TYPE-C_RTS5448		
Size	Document Number		Rev
C	Yoga C740		0.1
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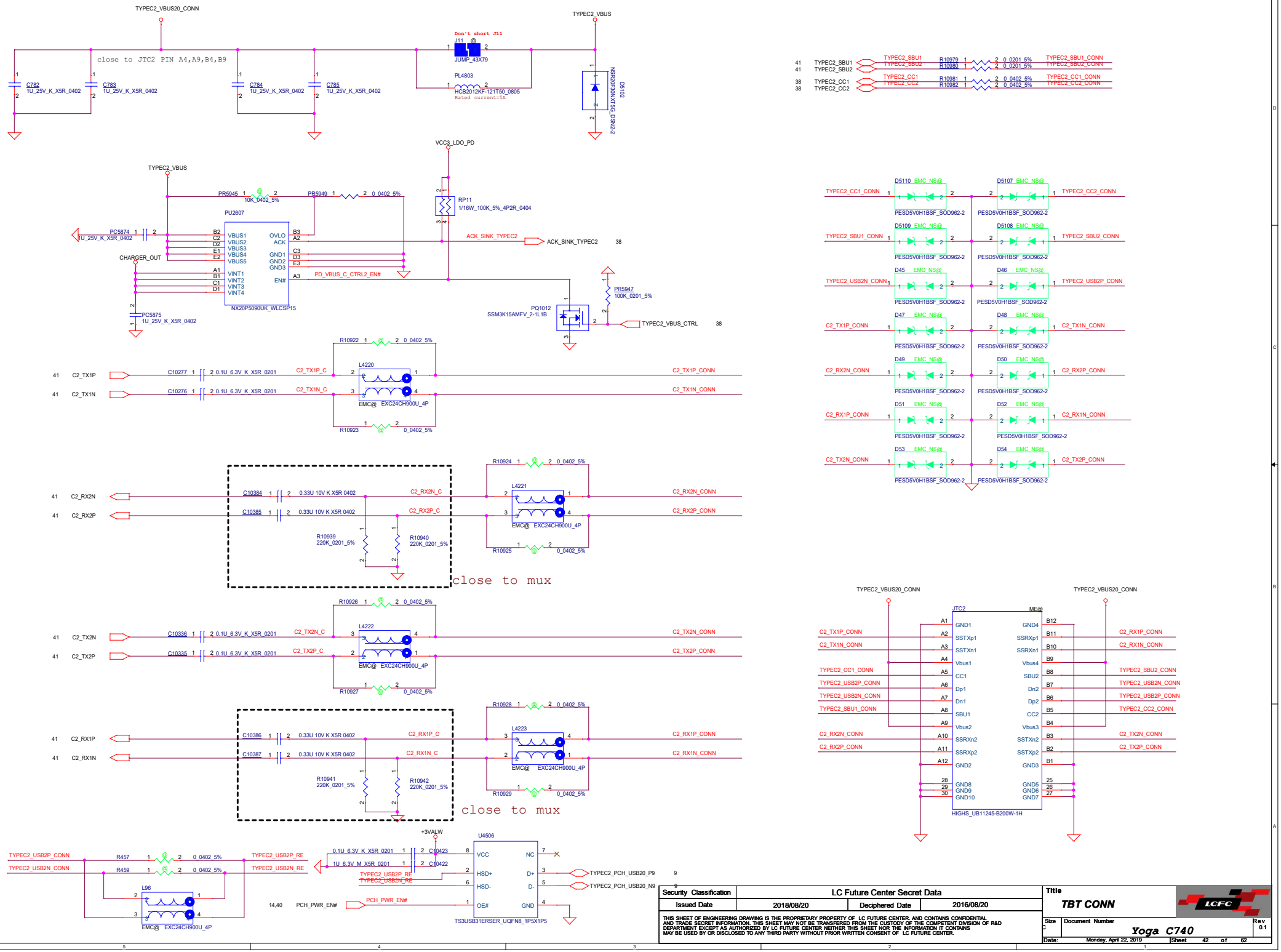

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Title: **TBT CONN**

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Title: *Blank*

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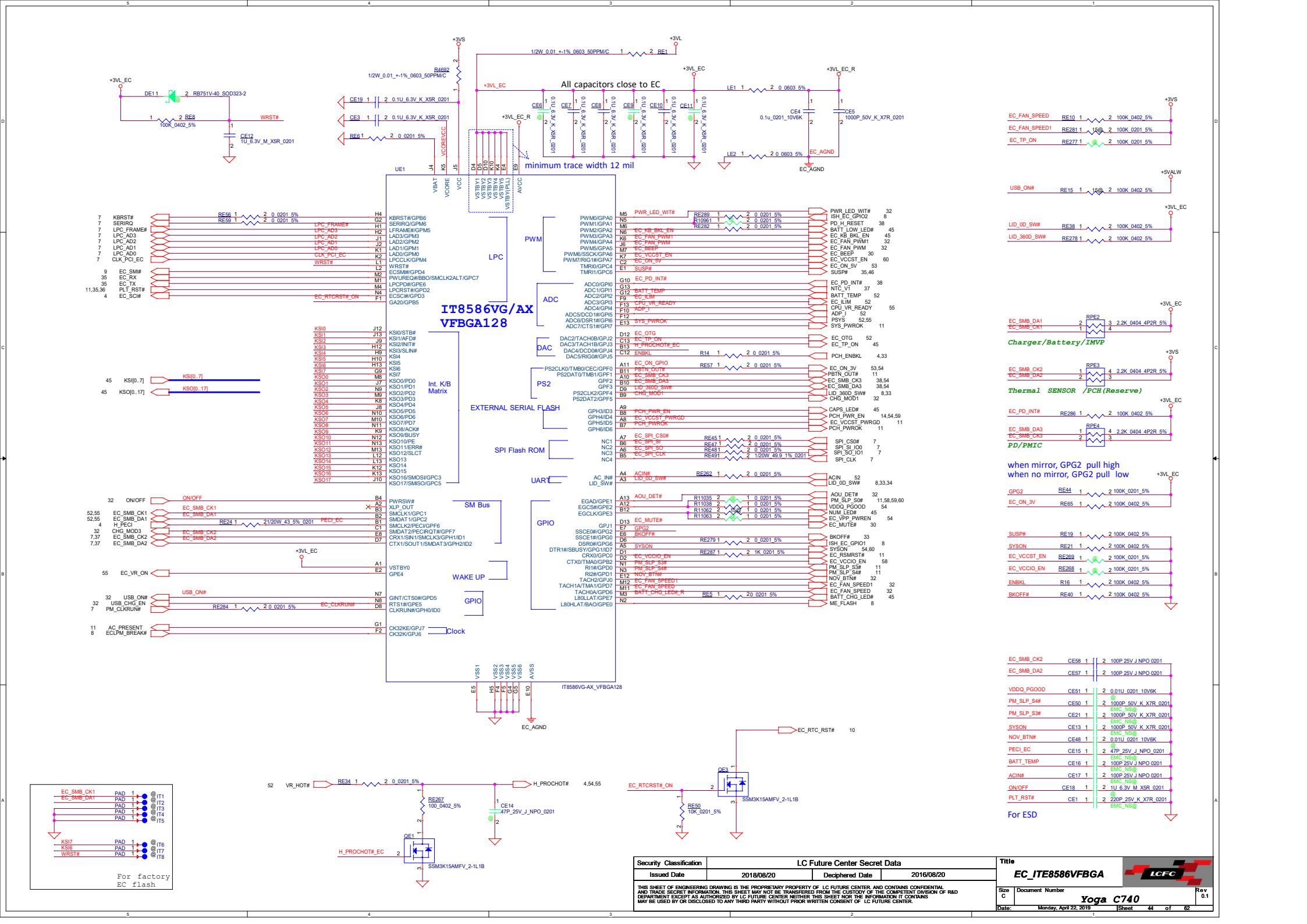
All capacitors close to EC
minimum trace width 12 mil
IT8586VG/AX
VFBGA128
LPC
PWM
ADC
DAC
PS2
Int. K/B Matrix
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
Charger/Battery/IMVP
Thermal SENSOR /PCH(Reserve)
PD/PMIC
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
For ESD
For factory EC flash
IT8586VG-AX_VFBGA128
SSM3K15AMFV_2-1L1B
Security Classification
LC Future Center Secret Data
Issued Date
2018/08/20
Deciphered Date
2016/08/20
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EC_ITE8586VFBGA
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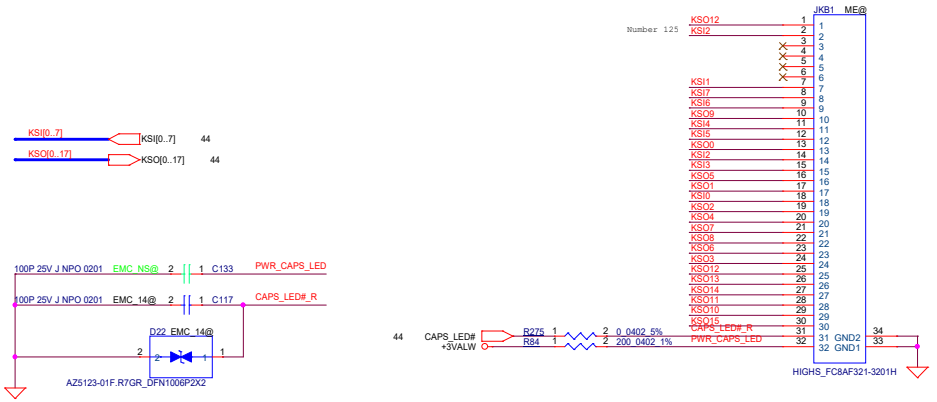
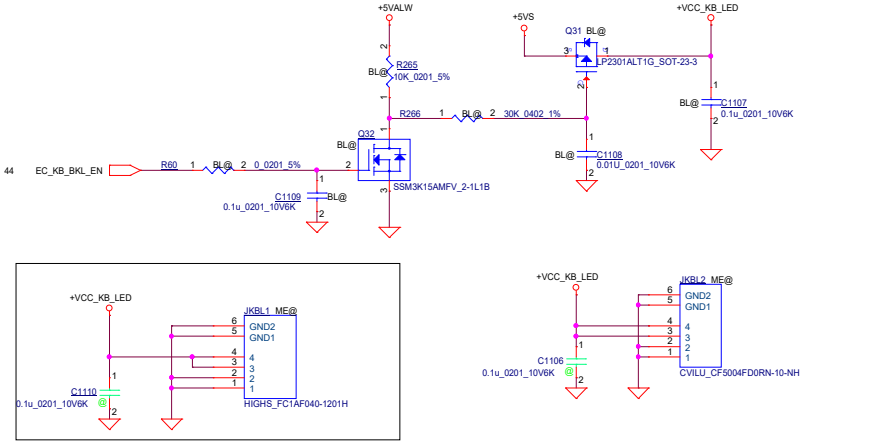
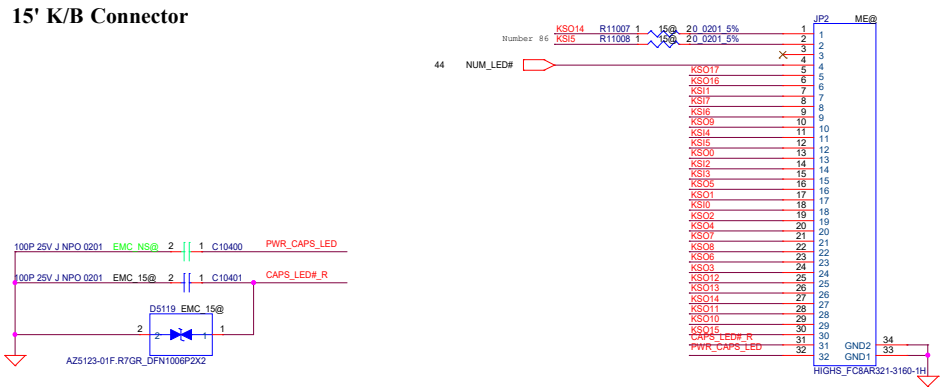
14' K/B Connector



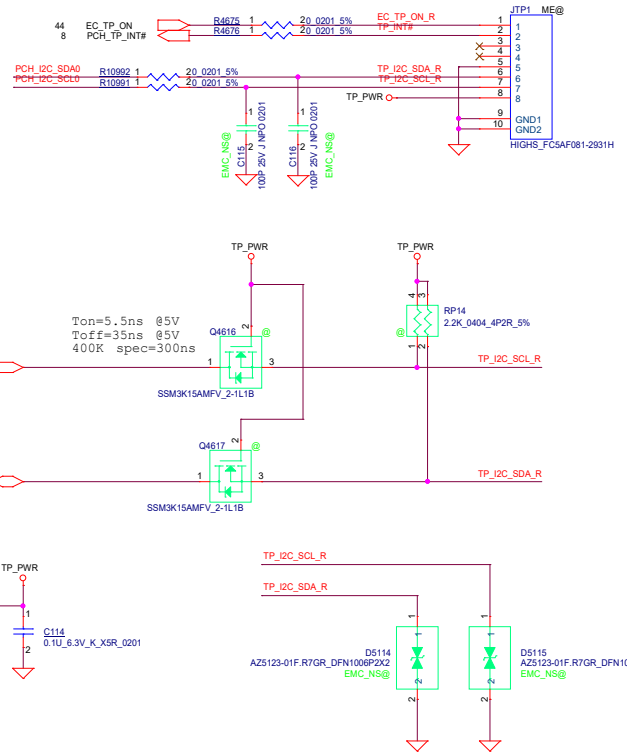
KB Backlight Connector

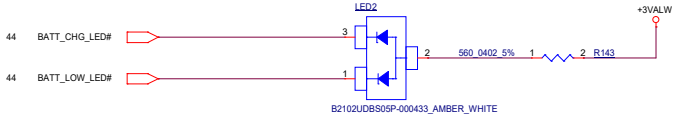


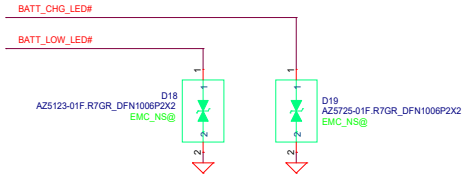
15' K/B Connector



TP/B Connector







LED	Stute	LED Behavior
Charge LED	Battery only	OFF
	Charging	Amber_on(battery:1%~90%)
		White_on(battery:91%~100%)

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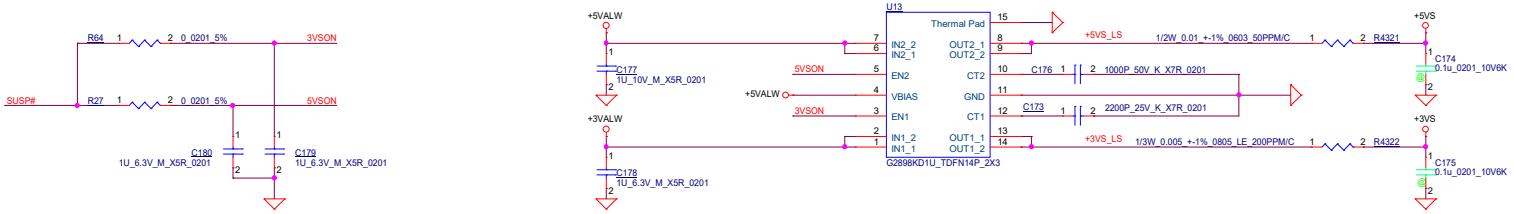
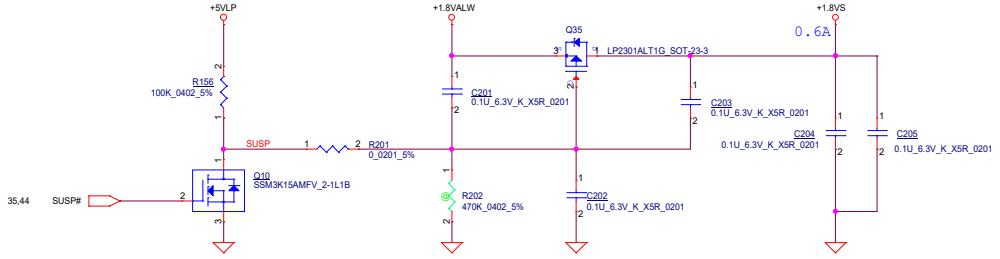
VS LOAD SW



1.8VS LOAD SW



DISCHARGE

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Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	DC V TO VS INTERFACE		
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20181105:
1. change L96 to EXC24CH900U_4P
2. RA1,RA4,RA12 change BOM structure to pop
3. C15 change to EMC@
4. CA190 change to 100p_25V
5. Change CA190,CA196 to pop
6. delete RA2,RA3,CA195,CA196
7. Change RA228,RA229,CA187,CA188 BOM structure to EMC_NS@
8. CA190,CA191 connect to RING_CONN2 and SLEEVE_CONN2
9. RA43 change to pop
10. Add CA196,CA199 on DMIC as EMC request
11. C10380~C10387 change to 0.33u_10V from 0.33u_25V
12. Add C10398, C10399 as EMC request
13. Add C10400, C10401, D5119 as EMC request

14. Change CA187.2 to HP_OUTL_CONN2, CA188.2 to HP_OUTR_CONN2
15. Change U4507 to TI SN74LVC1G17DCKR
16. Add PM_CLKRUN# for MS support
17. Change EC_OTG to EC pin D12
18. RC3102 change to 22ohm as EMC request
19. CA198.1 and CA199.1 change net
20. P31 add SPK EMC request
21. Change RP5 ph to +3VS_WLAN
22. Change GPIO of PCH_WLAN_OFF#, PCH_BT_OFF#
23. VCC_TS_ON# change net name to VCC_TS_ON
24.
25. RC3104,RC891, RP13, RP14 ph change to +3vs

26. Add R10986 for +1.8VALW_PCH
27. Change RC1111~RC1114,RC1T17, RC1118 VALUE
27. Change RC3083,RC3084, RC3085 VALUE
28. Delete Q6
29. Add CPU_C10_GATA control
30. Delete TSH_DEBUG circuit
31. change ts GPIO
32. change AOAC#, ECLPM-break#,I2C INT GPIO
33. change NTC_V2 to NTC_V1
34. Delete AOAC# circuit
35. Reserve +3V_WLAN rise time control
36. Change SPI TO2/IO3 net name
37. delete net CLK_PCIE_XDP and CLK_PCIE_XDP#
38. change BOARD_ID PH/PL res to 100k
39. minimum Codec res size
40. delete PCH_PWR_EN. use EC_ON_ALW(EC_ON changed) instead
41. chage FPR_PWR_EN to PCH control from EC

42. RP8 change to 10K

20181107
43. SW2 change new part as ME request
44. RP2,RC829 PH with +3VALW_PCH, reserve level shift of TP I2C
45. Delete RC830,RC831
46. update Page 3 notes
47. update P38 PD I2C address according datasheet
48. change C10172 BOM structure to EMC_NS@
49. add RC3107 for FPR_PWR_EN
50. reserve 0ohm for VCCPLL_OC and VCCPRIMCORE
51. reserve SLP_S0# PH and PD @ Page11
52. add C10_gate LS @ page 10
53. change VCCST_CPU solution @ page 60
54. add FPR_PWR_EN PH @ page 8
55. change PRIM_CORE_OPT_DIS GPIO to page8
56. delete SLP_S0 leVel Shift @ page 59
57. delege N8695 on VCCIO, remove VCCIO to PMIC, delete sense net @ page 13
58. change RC3089 to 0ohm @ page 44
59. HDA bus serial res change to 0ohm

20181108
1. Recovery VCCIO N8695 solution
2. add RC delay for VCCPRIM_1P05 enable and VCCPRIMCOARE enable
3. add PR8811 and NC PR8010 of VCCPRIM_CORE path
4. delete un-used component RC3099, R3T98, QC2, R157, R1303, R1055, RC3080
5. delete Page 44 un un-used RE36, RE18, QE2, RE42, RE46
6. U4507 change to @
7. RC 709 change to 8.2K follow intel
8. add R1003 to meet BEEP 14Vrms full scale input
9. R4684, R4685 change to 33ohm
10. RC710, RC711 change to 10K

20181109
1. modify net name of C1_RX2N_C
2. delete RC1123
3. delete Q5

20121112
1. modify VCC_TS circuit
2. add 50Pin connector for UHD
3. change eDP connector pin define for UHD and FHD cor-lay
4. delete R24

20181113
1. modify FHD edp Conn pin define
2. Change +3VS_EDP to +3VS_MIC

20181115
1. delete TP268,Tp269. add Res to GND as PCH eds request,
even though intel reference sch left it un-connected
2. delete TP266,TP267
3. delete RP5, change RP6 to 8P4R from 4P2R

20181116
1. Modify 15' KB pin defien for number86
2. reserve RE285 for EC ID
3. remove extra AC-CAP on edp AUX/TX0/TX1 @ page 33
4. add 0ohm on KB 15' KB for number80 choose
5. Delete BPM0#-BPM3# test point for XDP not used

20181119
1. change JPIO pin define@ page 32
2. move FPR power control circuit from DB to MB @ page 32
3. modify page17/page18 power decoupling BOM strucuere
4. change RC1307 to pop, reserve 0ohm to EM5201 for MS

20181120
1. Add KSO14,KSO17 on JP2 @ page 45
2. R11006 change to 0ohm
3. delete RE3
4. add Precision resistor R11011
5. delete R10594, R10524, R10523, R10593
6. Delete VCCIO enable diode on SLP_S3# and VCCIO_EN @ page 58

20181121
1. delete RC1057
2. CC1108 change to @
3. delete TC1414
4. delete CD318, CD48, CD108, CD313
5. change JP1 pin define @ page 30
6. change JSPK1 pin define @ page 31

20181123
1. delete PWR_AMBER_LED
2. add PCH_PWR_EN to enable primary power
3. delete R110T00

20181126
1. exchange LID_SW# and LID_KB_DIS_SW# GPIO on EC
2. change net EC_ON_ALW to Ec_ON_3V
3. change some CPU Res to 020I aS placement require
4. add hole
5. change JPIO pin define
6. JCM0S change to short pad

20181127
1. add precision res on FAN power and USB redriver power @ page 32
2. RE50 change to 10K for issue fix
3. U13 change to G2898 from TPS22976
4. L95,L96,L4221,L4220 swap pin
5. RP8 10K_0404_4P2R change to R11018 10K_0201_5%,delete net SATA0GP
6. L12 EMC_NS@ and SWAP pin
7. delete CPU_C10_GATE# level shift circuit

20181128
1. move 1.2V precision res to CPU side @ page13
2. U4507 VCC change to +3VALW_PCH
3. delete test point T4,T5,TP265
4. Delete UHD

20181129
1. RC2550 change to 0ohm
2. add CC4234
3. CC1298 change to 1u

20181130
1. EC_SMB3 change to +3VL_EC_pull up
2. add RE286 for PD to EC_I2C_INT#

20181203
1. RP2 pin swap
2. change page 58/59 GND symbol of DGND and AGND
3. delete RC3108
4. R4321 change to 0603
5. RE65 change to @

20181204
1. exchange USB3.0 P2 and P4
2. R10986 and R4323 change to 0603
3. RC502/RC604 pull high change to 1.2V_CPU
4. U4503 change to SA000079B00

20181205
1. U4503 change to SA000079B00
2. add R11022 for edp LED power
3. C178 change to stuff
4. RA43 change to not stuff--follow realtek suggestion
5. remove CFG portion to Page 16

20181206
1. R10975/R10976/R10977/R10978 change to R0201
2. delete one 43*79 jumper on CHARGER_IN
3. change RP1 net and change ph power to +3VALW_PCH

20181207
1. R258/R259 change PN to SD00001440J

20181210
1. add R11023 for TS reset connect to GND directly
2. PD U3901 change PN to SA000098Z003
3. Correct SS MUX power net from +3VS_R1/R2 to +3VS_RE1/RE2
4. change 15' KB BL connector as ME request

20181211
1. C123/C154/C10344/C10343/C10341 change to 10U 0402
2. R10889 change to stuff
3. PD drain1 and drain2 don't connect to GND
4. add C10415/C10416/C10417/C10418 for CC protect
5. reserve C10419 for PD_H_RESET
6. Reserve R11024 foe EC_boot
7. C10345/C155 change to 0402 6.3V
8. R143 change to 300ohm
9. add 0ohm on PD GPIO
10. delete PR5940/PR5946
11. change type-c ACIN control to low active

20181212
1. change RC890, RC891 and RC3104 to 10k Ohm
2. RA16 change to 33ohm
3. codec PN update to AV2
4. delete R4678
5. add vccio sense rese

20181213
1. CC1347/CC1343 change to 0201 size
2. Change SPI topology

20181214
1. add R11035 for SLP_S0# to EC
2. Q31 gate change to 0.01u+30K
3. CC1409 change to 1U
4. reserve RE287
5. DDI_DDC_CLK delete

20181217
1. Change LID_SW# and LID_KB_DIS_SW# net name
for easy recoginize and change lid to PCH
2. add ME flash MOS circuit as intel suggest
3. Delete RC1117, RC834
4. change C156 to PD side

20181218
1. exchange USB3 port4 P/N @ JPIO pin define
2. Add 3 ohm res for ISH EC GPIO
3. Set typec ACIN control as high active
4. PR5941/PR5947 change to 100Kand connect to GND

20181219
1. add ISH GPIO to EC for mode description

20181220
1. CD363/CD111 change to 0402 for 0201 material shortage
2. change H2 footprint
3. delete RE58
4. Adjust MD decoupling cap base layout position

20181221
1. Change H8,H8,H10 footprint

20181224
1. change WLAN power from load SW
2. follow intel comment of CNVi
3. delete U4507
4. add one more hole H14
5. change Codec JD detect value-->use internal 47K
6. change TS and FPR power SW logic
7. reserve R11058/R11044
7. add +3VALW_PCH power SW

20181225
1. PD ROM power diode replaced by 0ohm
2. delete R11044
3. delete U225, U226
4. DELETE R11055/R11052

20181229
1. Add PR4902 for charger option of 15'

20190108
1. change CC1001/CC1002 to K level
2. R266 change to 0402 size for shortage
3. RE65 change to pop

20190121
1. Change U11 pin connection
2. change FPR power control circiut
3. change +3VALW_PCH circiut

20190214
1. Change VPP enable to SYSON, use original EC GPIO for NUMLCK
2. Add RH831
3. Add RA3538

20190218
1. wlan power SW gate pull up to +3valw_pch
2. reserve +3valw to mux
3. remove u4 and related

20190219
1. R51,R176,R177,R10880,R10881 change to 0201
2. RA30,RA34, RA221,RA222 change to bead L4227,L4228,L4229,L4230
3.CA182,CA181,CA31,CA32 change to 2200p
4. C11 change to pop

20190220
1. add SW U4505,U4506 for USB2.0 of USB-C
2. add D5120,RC3118 for 0d sensor to PCH
3. change RC890 to 0201
4. R11004 connect to +3VALW_PCH
5. SS mux reserve +3VALW_PCH
6. ECLPM_BREAK change to ECLPM_BREAK#
7. add CE58,CE59

20190221
1. swap UC.BW35 &UC.BW34
2. mux use +3vs, reserve +3valw
3. reserve +3vs for FPR

20190222
1. Correct RC3118 net to PCH_LID_SW1#
2. Add R11066 for USB2 SW enable

20190415
1. add +3VALW_PCH discharger circuit
2. add VCC_TS discharger circuit
3. SPK_R/L swap
4. change TC USB2.0 BUS switch enable control
5. C11 change not stuff,,CA199 stuff
6. R143 change to 560ohm
7. RESERVE R11077 for CNVI CLK out
8. remove power debug conn JP3

20190419
1. add cap for 0.6V
2. USB SW change to +3VALW power supply
3. change Codec beep circuit

20190422
1. remove LEDVDD rsense
2. add 0ohm for sub-board ACC-sensor
3. add 100p_0201 for TC mux AUX signals
4. RE44 change to 0201

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: *change list*

Size	Document Number	Rev
C	FYG41	0.1

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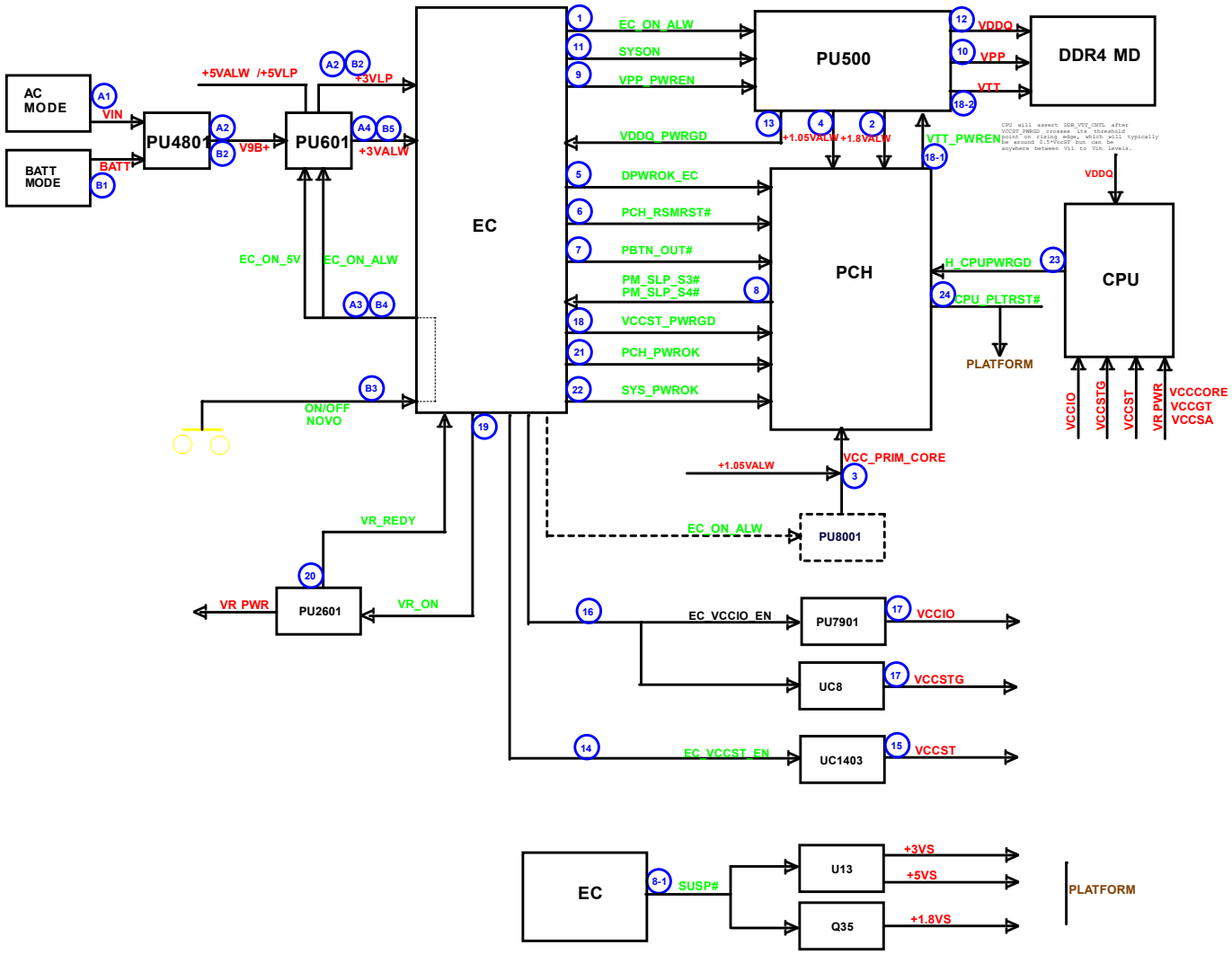
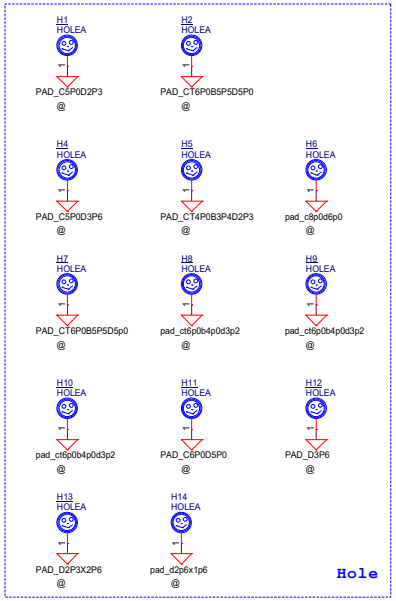


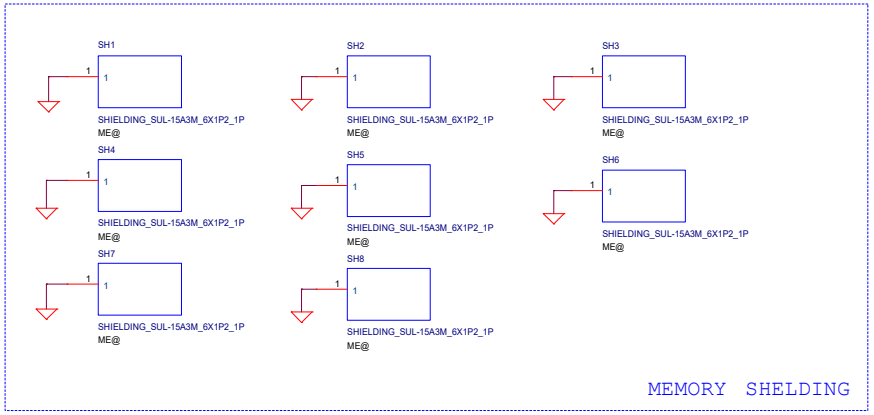
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

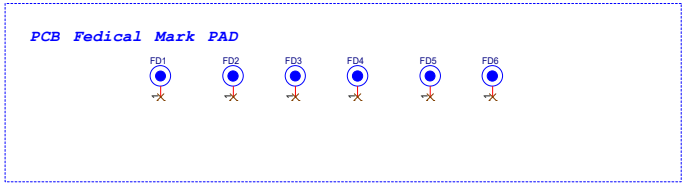
Title: **Power sequence block**

Size	Document Number	Rev
C	Yoga C740	0.1

Date: Monday, April 22, 2019 | Sheet 48 of 62







Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	Hole		
Size	Document Number		Rev
C	FYG41		0.1
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

SYMBOL

Size	Document Number	Rev
C	FYG41	0.1

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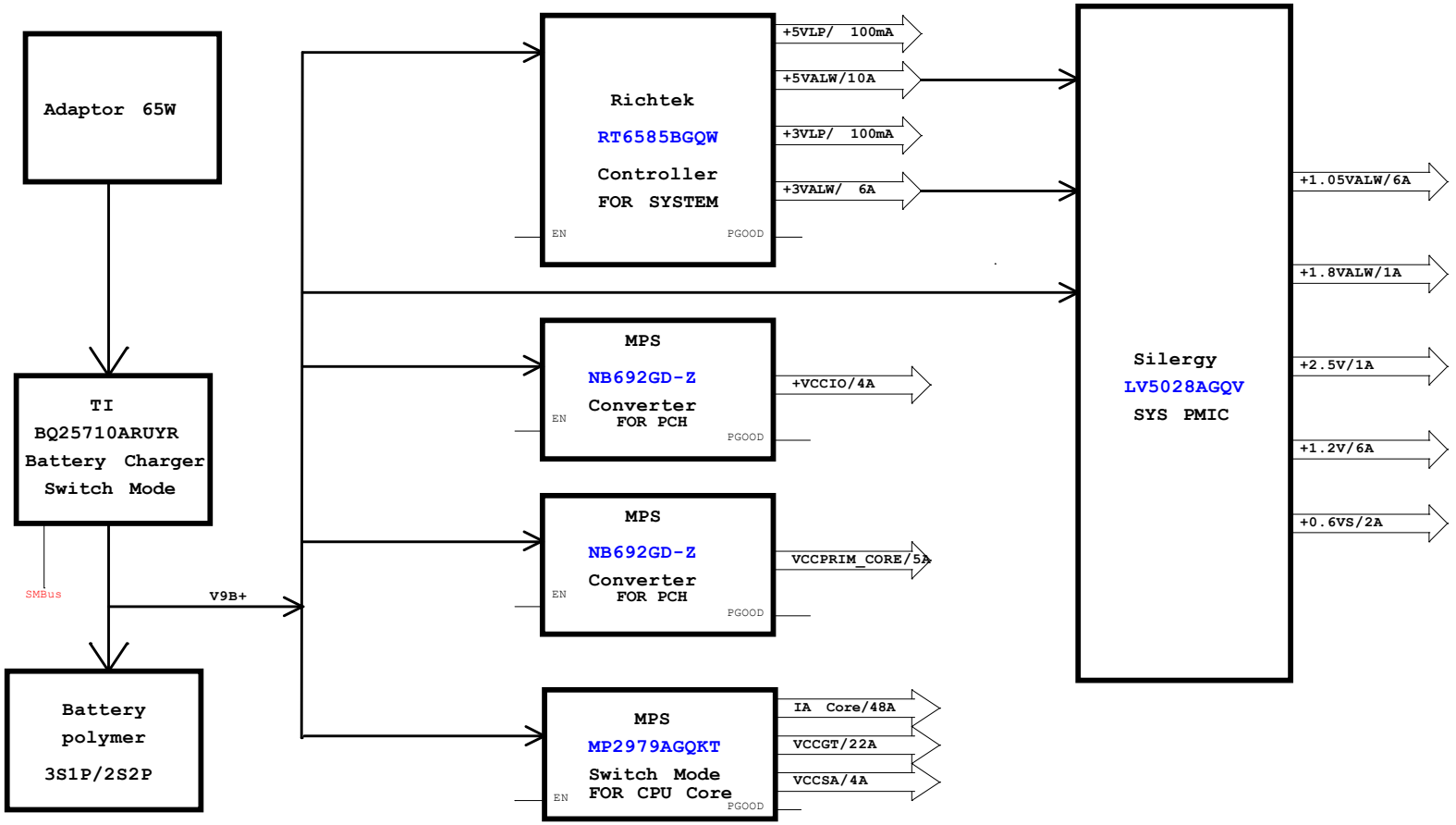
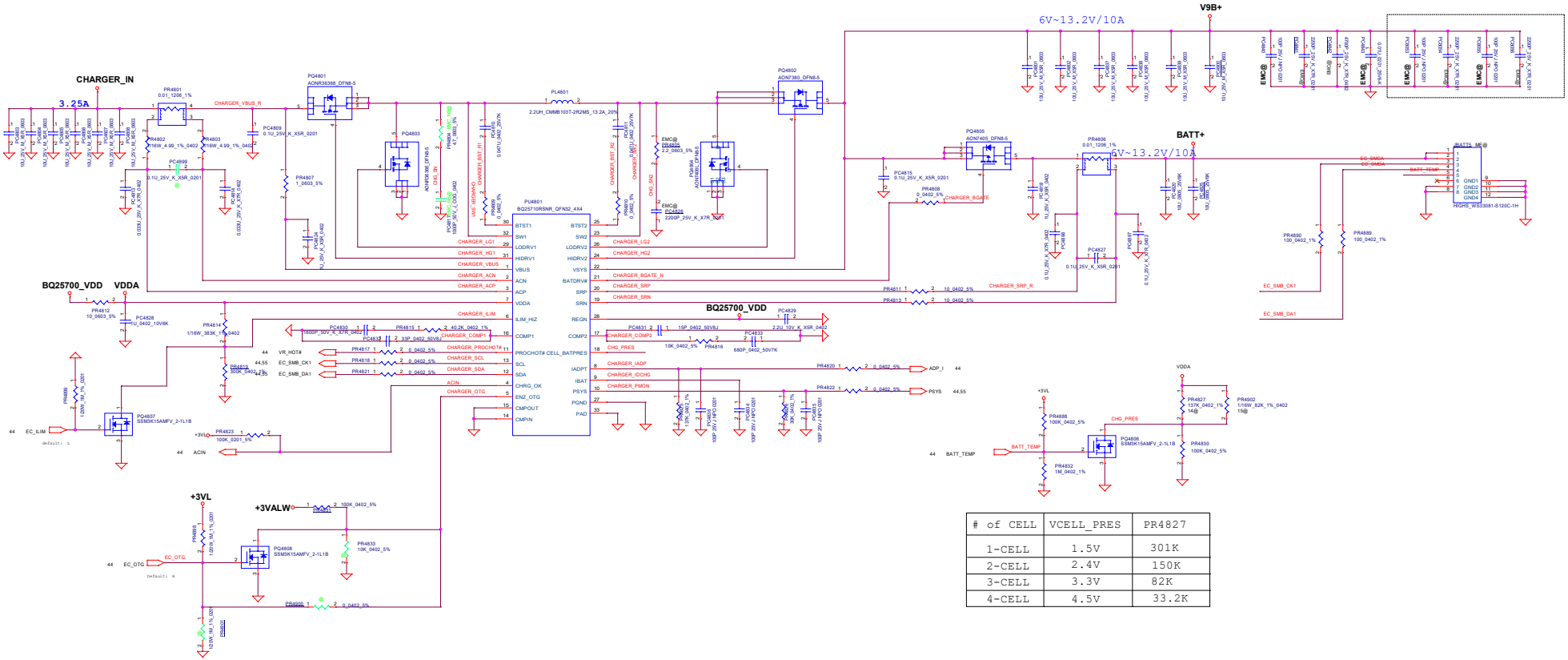


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-Power Diagram

Size: Custom	Document Number: Yoga C740	Rev: 0.1
Date: Monday, April 22, 2019	Sheet 51 of 61	



# of CELL	VCELL_PRES	PR4827
1-CELL	1.5V	301K
2-CELL	2.4V	150K
3-CELL	3.3V	82K
4-CELL	4.5V	33.2K

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PWR-CHARGER
Size	D
Document Number	Yoga C740
Rev	0.1
Date	Monday, April 22, 2019
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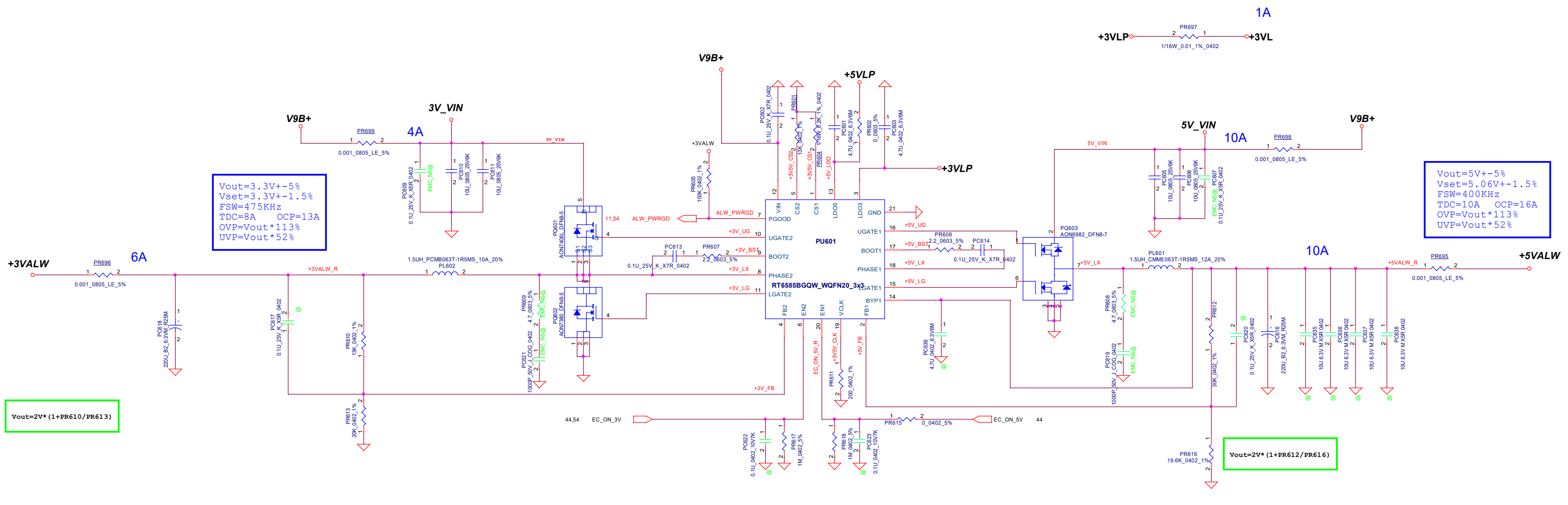

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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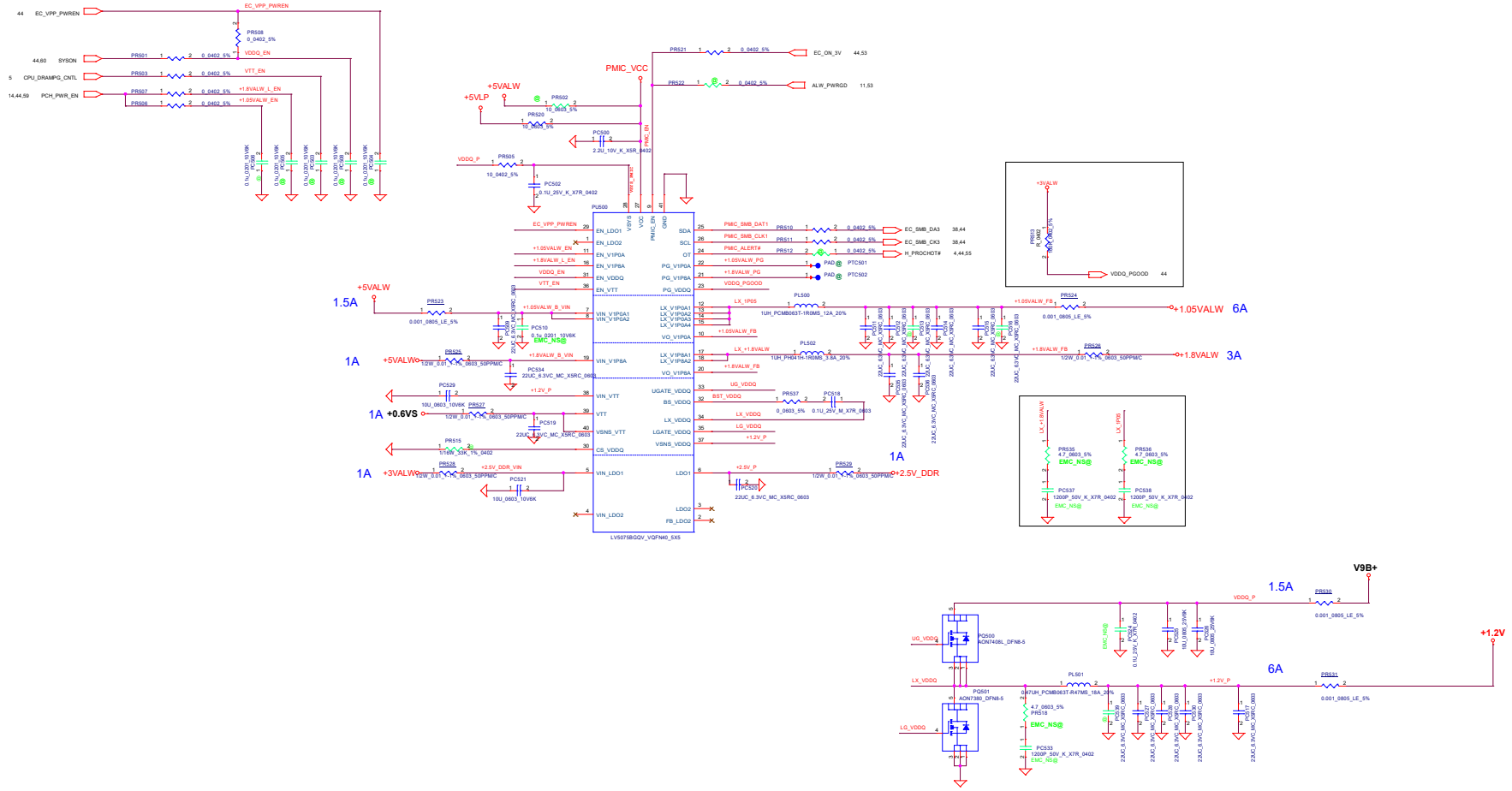
Title: PWR_3VALW/5VALW

LCFC

Size: D — Document Number: Yoga C740 — Rev: 0.1

Date: Monday, April 22, 2019 — Sheet 53 of 62



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR PMIC-DDR4/1.0ALW/1.8ALW/1.2V

Size	Document Number	Rev
D	Yoga C740	0.1

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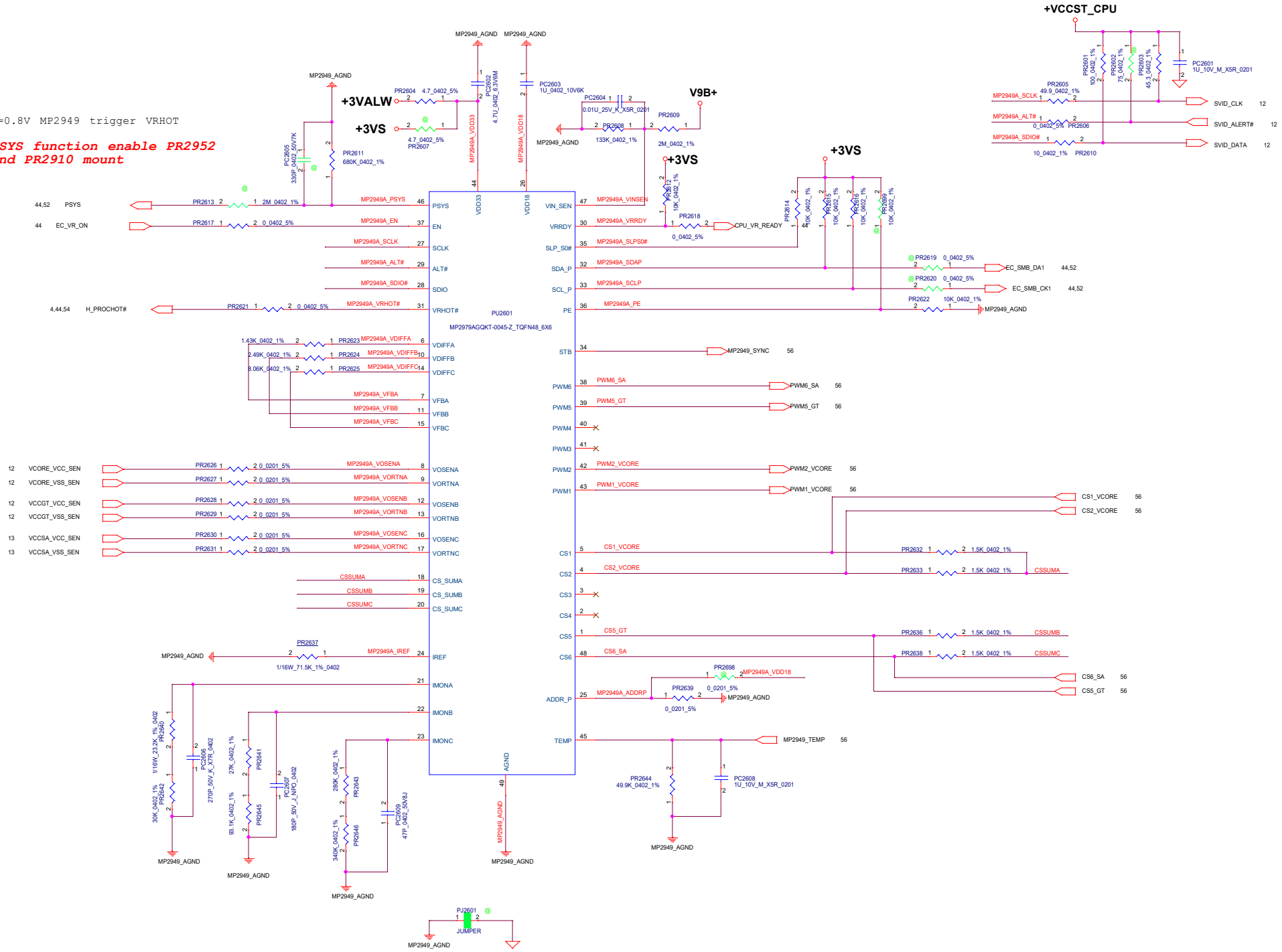
PSYS=0.8V MP2949 trigger VRHOT

PSYS function enable PR2952 and PR2910 mount



Security Classification	LC Future Center Secret Data		
Issued Date	2015/12/08	Deciphered Date	2016/12/08

Title	PWR_IMVP8		
Size	Document Number		Rev
C	Yoga C740		0.1
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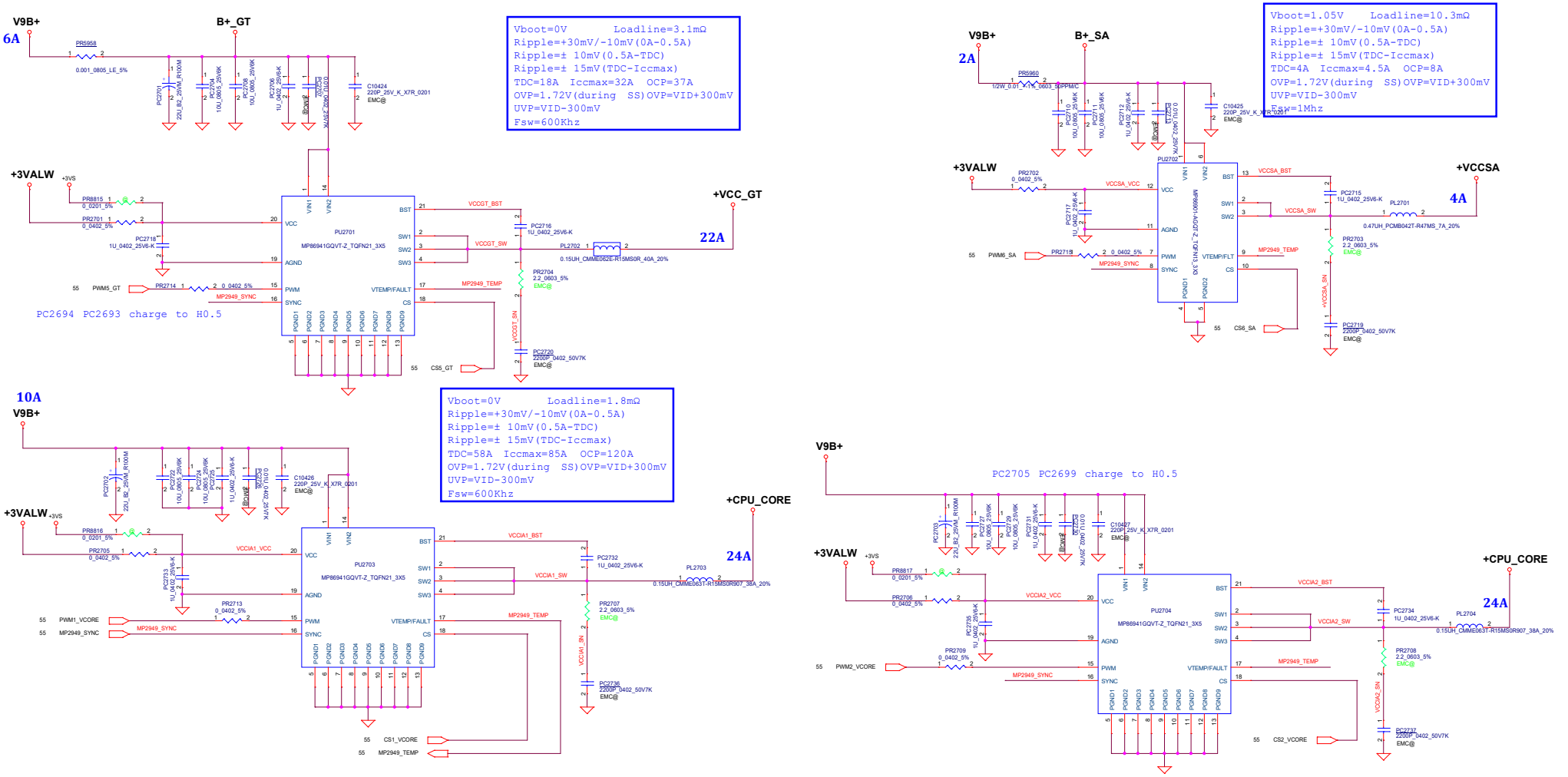
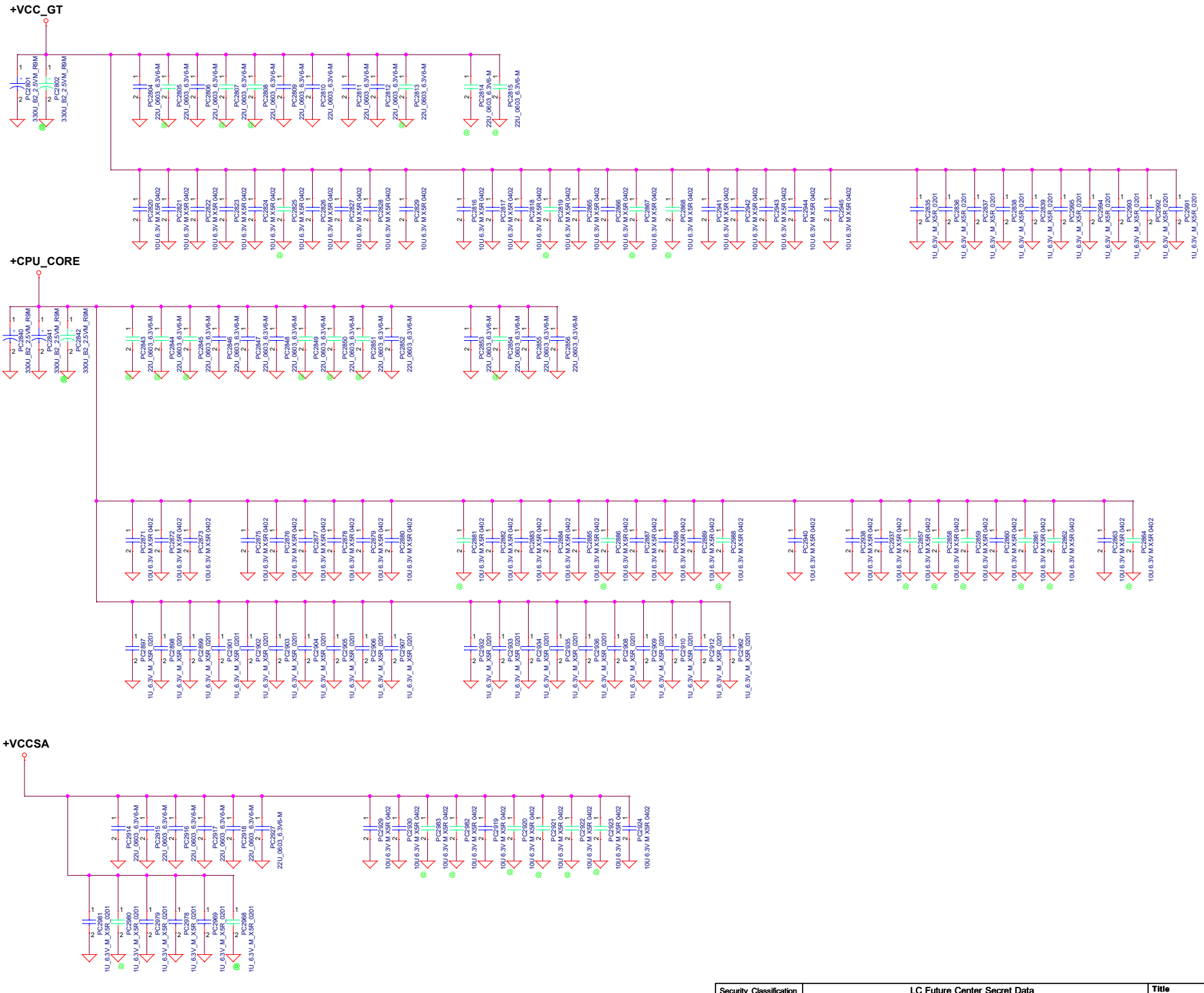


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	VCORE DMOS		
Size	Document Number		Rev
Custom	Yoga C740		0.1
Date:	Monday, April 22, 2019	Sheet	56 of 62



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	PWR-Decoup	
Size: Custom	Document Number: Yoga C740	Rev: 0.1
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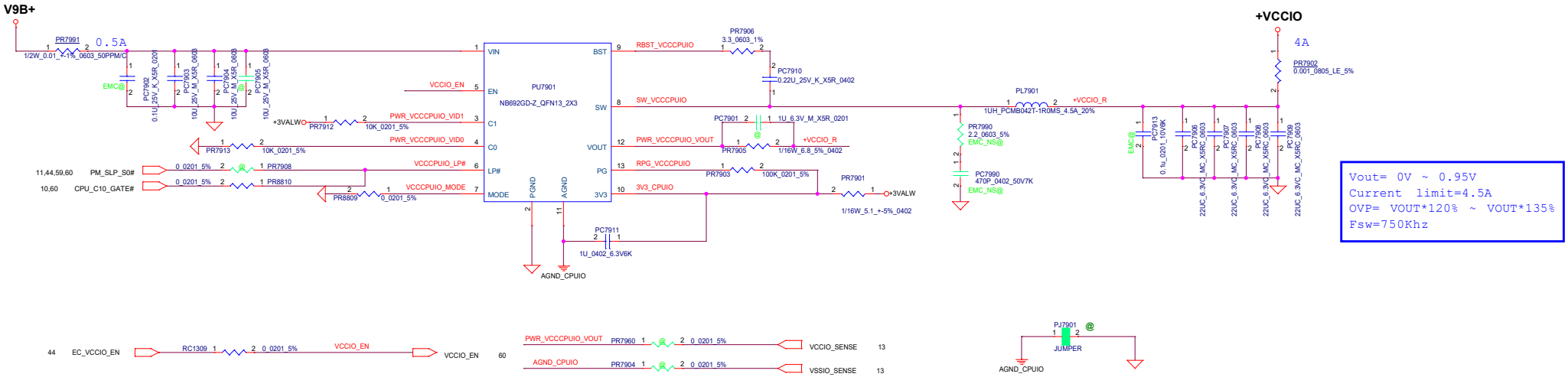
Control Bit Logics				
	LP#	C1	C0	VOUT
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.75
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1.0
	1	1	1	1.05

Vout= 0 under S0Ix



Vout= 0V ~ 0.95V
Current limit=4.5A
OVP= VOUT*120% ~ VOUT*135%
Fsw=750Khz

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	VCCIO		
Size	Document Number		Rev
C	Yoga C740		0.1
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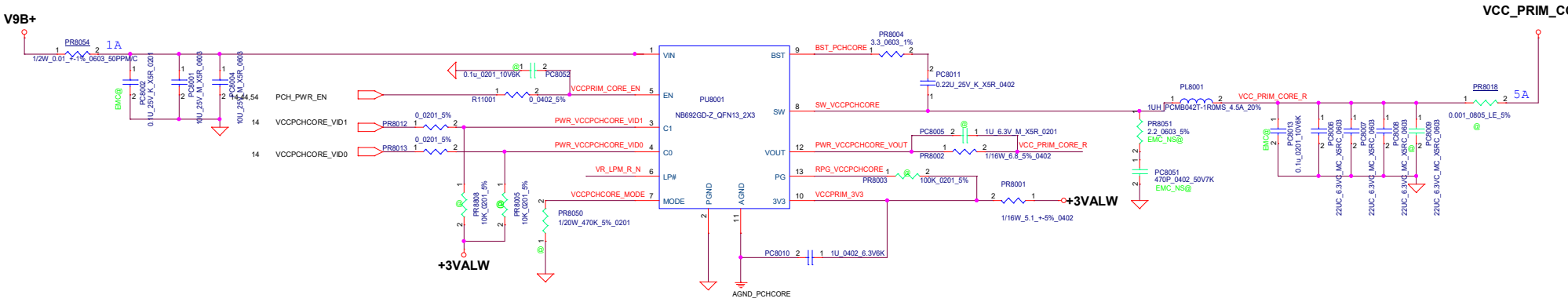
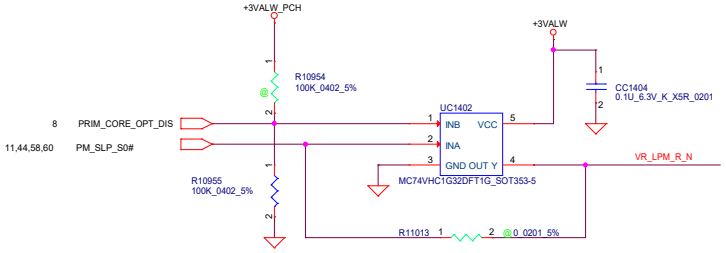
Vout= 0.950V ~ 1.05V
Current limit=4.5A
OVP= VOUT*120% ~ VOUT*135%
Fsw=750Khz

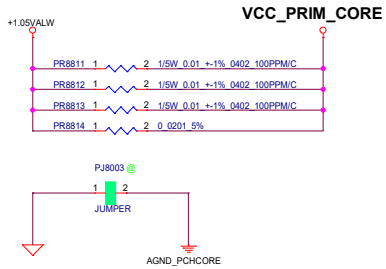
Control Bit Logics

	LP#	C1	C0	VOUT
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.75
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1.0
	1	1	1	1.05

Vout= 0.75 under S0Ix







Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: VCC_PRIM_CORE

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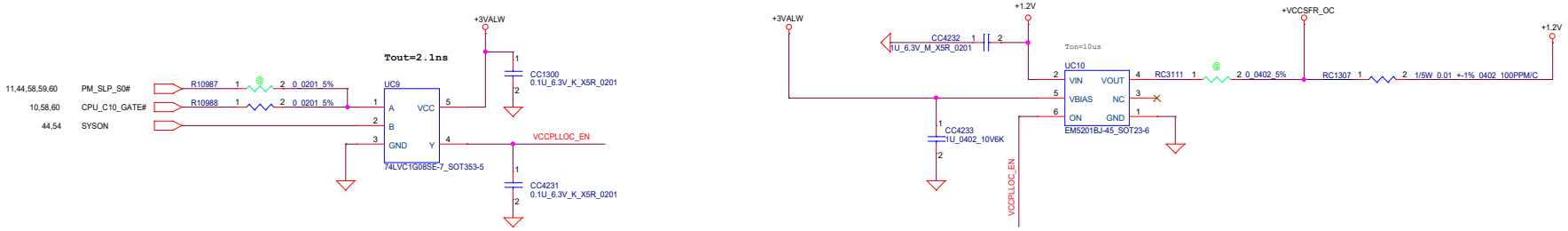
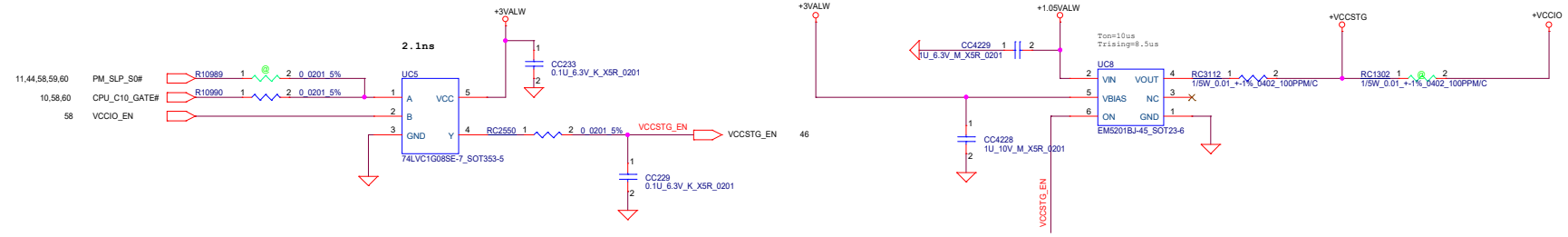
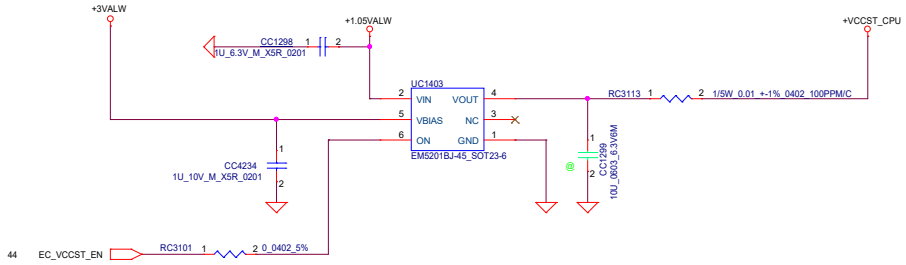
+VCCSFR_OC



+VCCSTG



+VCCST_CPU



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	VCCST/VCCSTG		
Size	Document Number		Rev
C	FYG41		0.1
Date:	Monday, April 22, 2019	Sheet	60 of 62

20181031:
Renumber the schematic,add predise resistance
20181105:
delete some vcore input output mlcc
20181106:
change some rc according to vendor's suggestion
20181119:
change some rc & pn
20181121:
change charger accuracy resistence
20181126:
change some 0402 to 0201
20181126:
change ALL jump to accuracy resistence

20190215
1. PR4819 change to 300K
2. PR601 change to 13K PR604 change to 6.2K
3. PC2701 change NET to B+_G7

20190218
1. PR2637 change to 71.5K
2. delete PR5961 PR5959
3. page57 decoupling change

20190220
1,V9b+ net add cap:100pF+2200pF+4700pF+0.01uF,
2.PR2704,PR2703,PR2707,PR2708 pop 2.2ohm; PC2720,PC2719,PC2736,PC2737 pop 2200pF
3.PC2707,PC2713,PC2726,PC2730 change to 0.01uF.

20190221
1. reserve 3vs for vcore/vccgt drmos

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: **POWER CHANGE LIST**

Size	Document Number	Rev
C	FYG41	0.1

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

POWER SYMBOL

Size	Document Number	Rev
C	FYG41	0.1

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