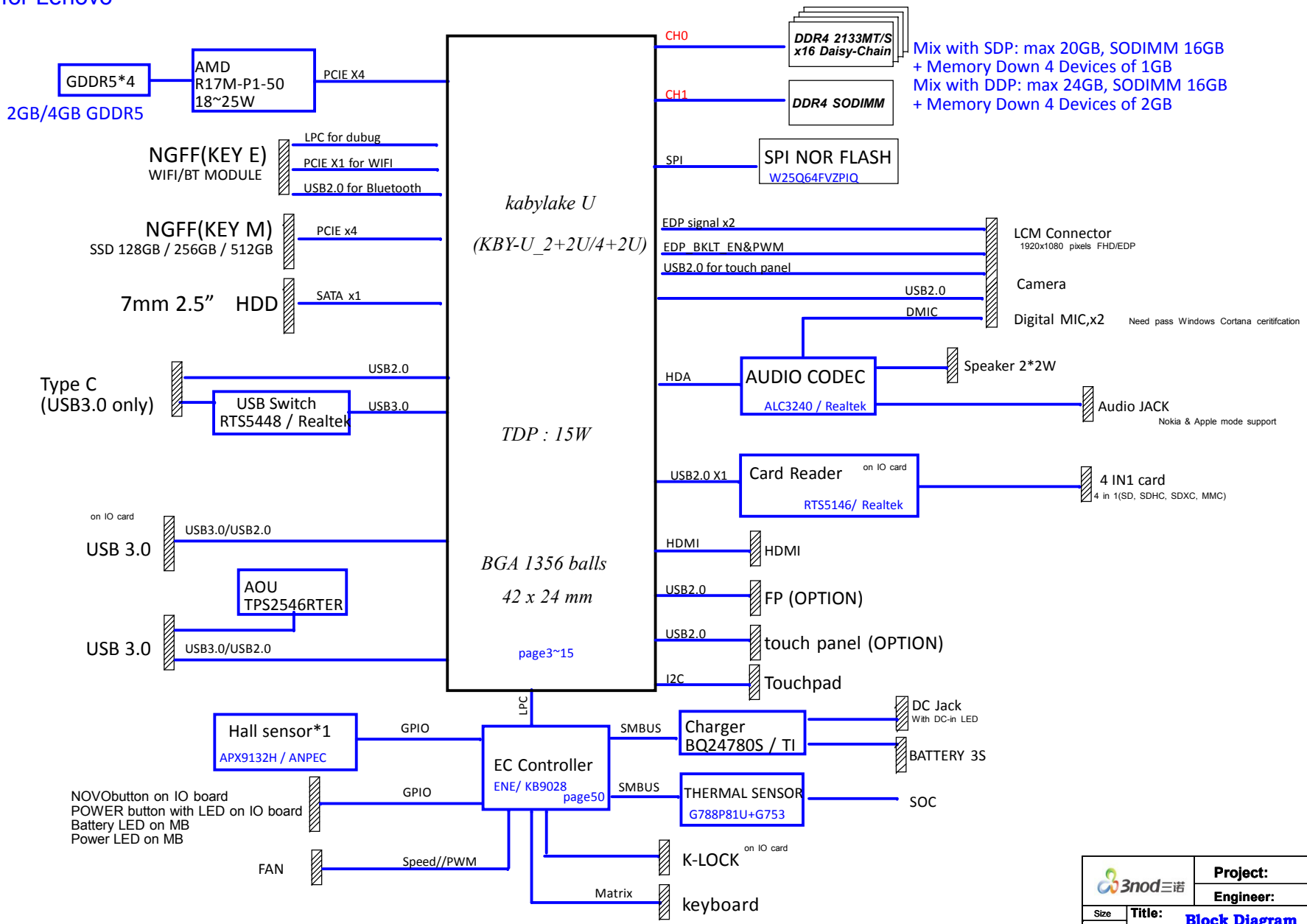
330S-14&15 for Lenovo



3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: Block Diagram	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 1 of 81	

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INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd:_
Wed Jun 03 11:22:42 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: TABLE OF CONTENTS	Rev: V01
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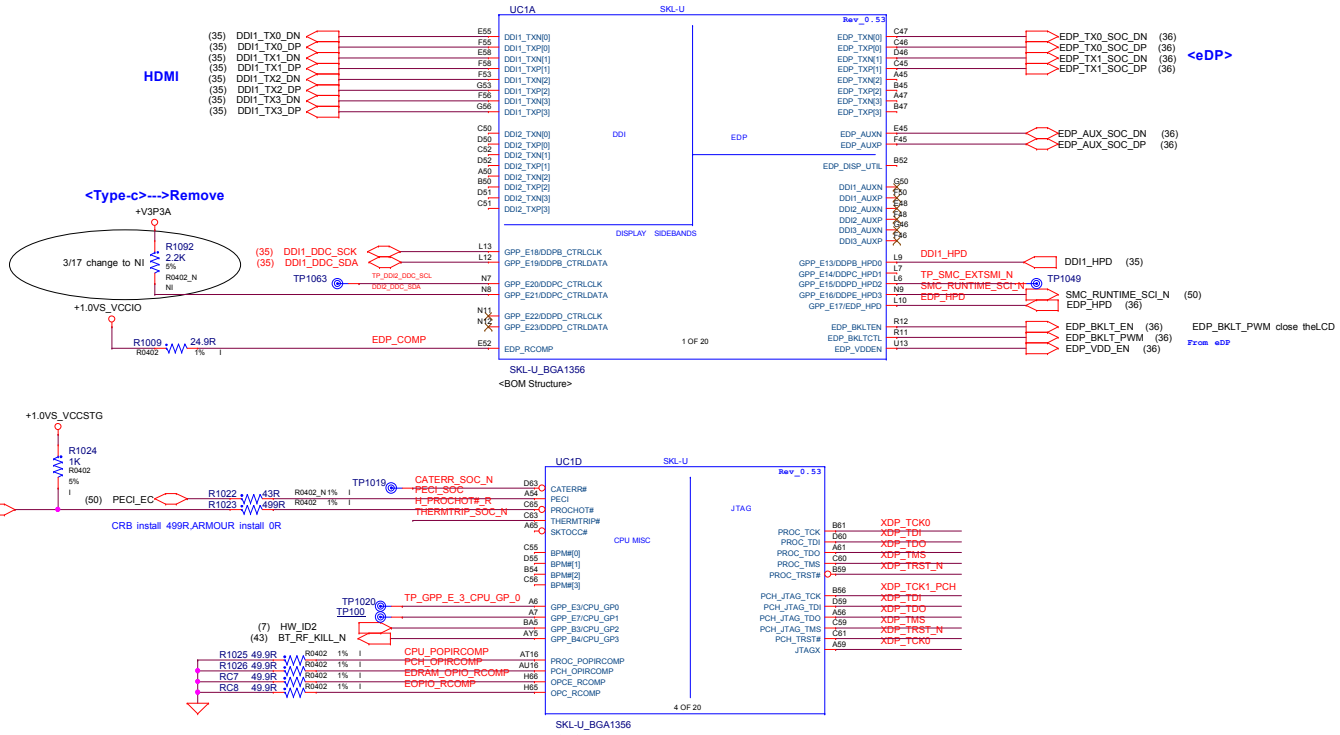
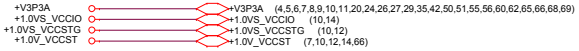
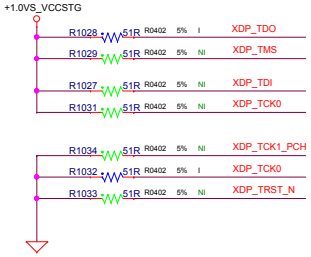
DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.







Project:	330S-14&15		
Engineer:	Luffy		
Size: Custom	Title: KBL-U(1/12)DDI,MISC,XDP,EDP		Rev: V01
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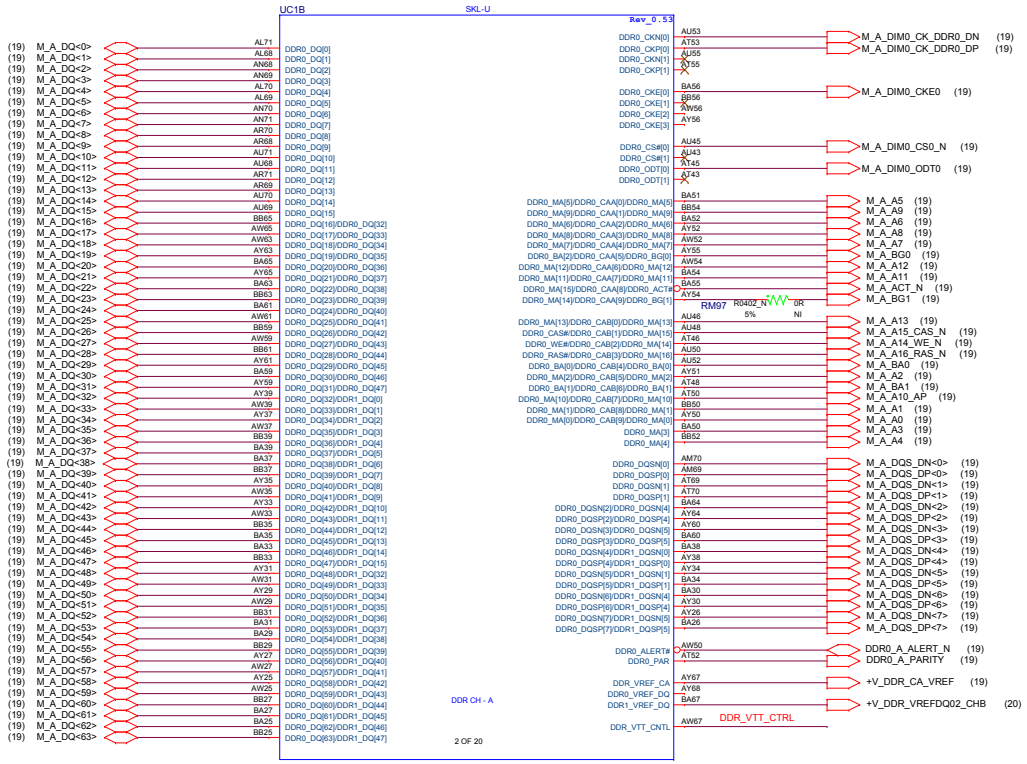
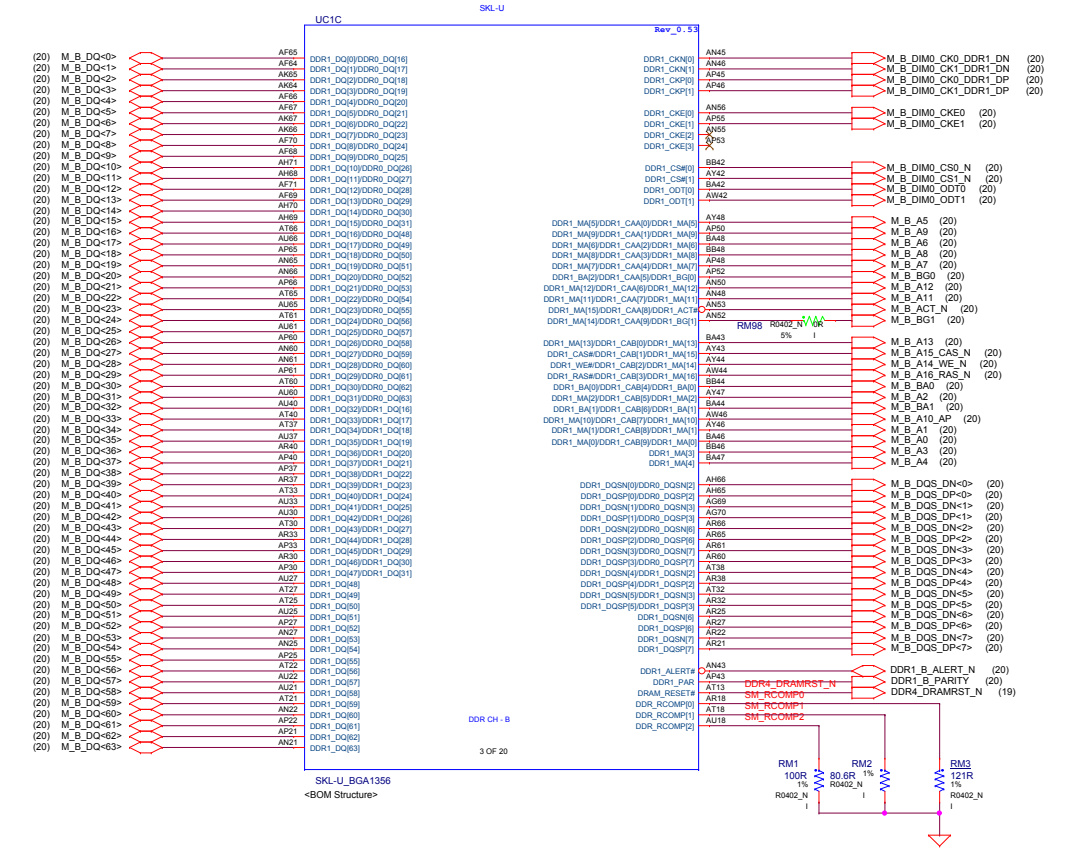
Interleaved



Interleaved

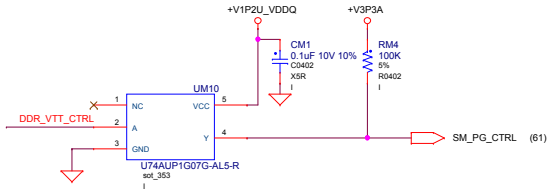


1. To support DDP, need to change two pins on DRAM. You have reserved them. Pls install the BOM.

	X16 SDP	X16 DDP TwinDie
DRAM M9 pin	VSS	Connect to CPU BG1
DRAM E9 Pin	VSS	UZQ

Default

Memory size	4Gb or 8Gb	16Gb	
DRAM M9 pin	RM95,RM96,RM97,RM98 need uninstall RM99,RM100 need install	RM95,RM96,RM97,RM98 need install RM99,RM100 need uninstall	page4,19,20
DRAM E9 pin	RM79,RM81,RM83,RM85, RM87,RM89,RM91,RM93 need install 0 ohm	RM79,RM81,RM83,RM85, RM87,RM89,RM91,RM93 need install 240 ohm	page19,20
SOC RCOMP0	RM3 121 ohm need install		page4



+V3P3A
+V1P2U_VDDQ
+V3P3A (3,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)
+V1P2U_VDDQ (10,19,20,21,61,68)

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title:	KBL-U(2/12)DDR4
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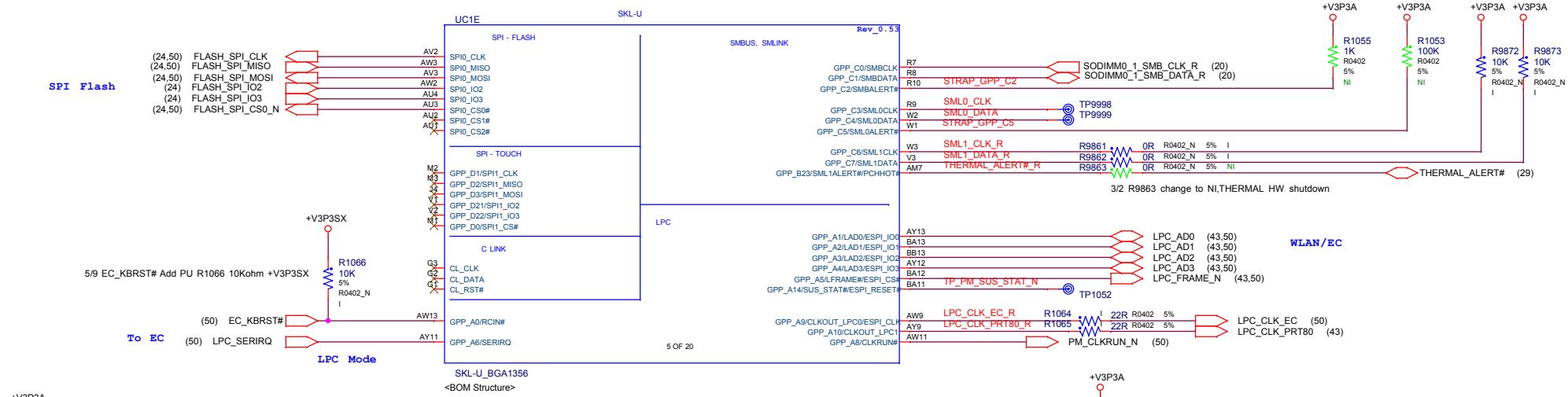

SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SML1ALERT# / PCHHOT#/ GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: KBL-U(3/12)SPI,ESPI,SMB,LPC	Rev: V01
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To Enable ME Override

(50) ME_Flash_EN — R9848 0R 5% I (R0402_N) — STRAP_HDA_SDO_SOC

Difference with armour
Add EC to enable ME override

5/23 R9848 install,BIOS request

HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.

SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

(46) HDA_SYNC — RC393 33R R0402 5% I — HDA_SYNC_SOC
(46) HDA_BCLK_R — R1086 33R R0402 5% NI — HDA_BCLK
(46) STRAP_HDA_SDO — RC395 33R R0402 5% I — STRAP_HDA_SDO_SOC
TP10056 — RC394 33R R0402 5% I — HDA_RST_N_SOC

Note: RESET# is not required for the ALC3240.

+V3P3A — R1054 1K R0402 5% NI

HDA for AUDIO

UC1G — SKL-U — Rev_0.53

AUDIO

HDA_SYNC_SOC — BA22 HDA_SYNC/I2S0_SFRM
HDA_BCLK — AY22 HDA_BLK/I2S0_SCLK
STRAP_HDA_SDO_SOC — BB22 HDA_SDO/I2S0_TXD
(46) HDA_SDI0 — BA21 HDA_SDI0/I2S0_RXD
HDA_RST_N_SOC — AY21 HDA_SDI1/I2S1_RXD
AW22 HDA_RST#/I2S1_SCLK
I5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD

AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD

(43) WIFI_DISABLE_N — H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1

+V3P3SX — R1052 100K 5% NI (R0402) — AW5 GPP_B14/SPKR
(46) HDA_SPKR

1/4 Connect codec

SDIO/SDXC

AB11 GPP_G0/SD_CMD
AB13 GPP_G1/SD_DATA0
AB12 GPP_G2/SD_DATA1
W12 GPP_G3/SD_DATA2
W11 GPP_G4/SD_DATA3
W10 GPP_G5/SD_CD#
W8 GPP_G6/SD_CLK
W7 GPP_G7/SD_WP — TP_SD_WP — R9864 0R R0402_N 5% NI

Difference with armour
Add 0ohm NI

BA9 GPP_A17/SD_PWR_EN#/ISH_GP7
BB9 GPP_A16/SD_1P8_SEL

AB7 SD_RCOMP — SDMMC_RCOMP — R1015 200R R0402 1% I

AF13 GPP_F23

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SKL-U_BGA1356
<BOM Structure>

+V3P3A
+V3P3SX

+V3P3A (3,4,5,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)
+V3P3SX (5,7,8,9,10,20,25,26,27,28,30,35,36,43,46,50,52)

UC1I — SKL_ULT — Rev_0.53

CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C38 CSI2_DN1
D38 CSI2_DP1
C36 CSI2_DN2
D36 CSI2_DP2
A38 CSI2_DN3
B38 CSI2_DP3

C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

C37 CSI2_CLKN0
D37 CSI2_CLKP0
C32 CSI2_CLKN1
D32 CSI2_CLKP1
C29 CSI2_CLKN2
D29 CSI2_CLKP2
B26 CSI2_CLKN3
A26 CSI2_CLKP3

E13 CSI2_COMP — CSI2_COMP — R1013 100R R0402 1% I
B7 GPP_D4/FLASHTRIG — CSI2_FLASH_STROBE — TP1061

3/18 Add TP1061

EMMC

AP2 GPP_F13/EMMC_DATA0
AP1 GPP_F14/EMMC_DATA1
AP3 GPP_F15/EMMC_DATA2
AN3 GPP_F16/EMMC_DATA3
AN1 GPP_F17/EMMC_DATA4
AN2 GPP_F18/EMMC_DATA5
AM4 GPP_F19/EMMC_DATA6
AM1 GPP_F20/EMMC_DATA7

AM2 GPP_F21/EMMC_RCLK
AM3 GPP_F22/EMMC_CLK
AP4 GPP_F12/EMMC_CMD

AT1 EMMC_RCOMP — EMMC_RCOMP — R1014 200R R0402 1% I

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SKL-U_BGA1356
<BOM Structure>

5/10 Del TP1055,TP1056,TP1057,TP1058,TP1059,TP1060,TP1016,TP1017,
MIPI defferential don't test point

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title:	KBL-U(4/12)HDA,EMMC,SD
	Rev	V01
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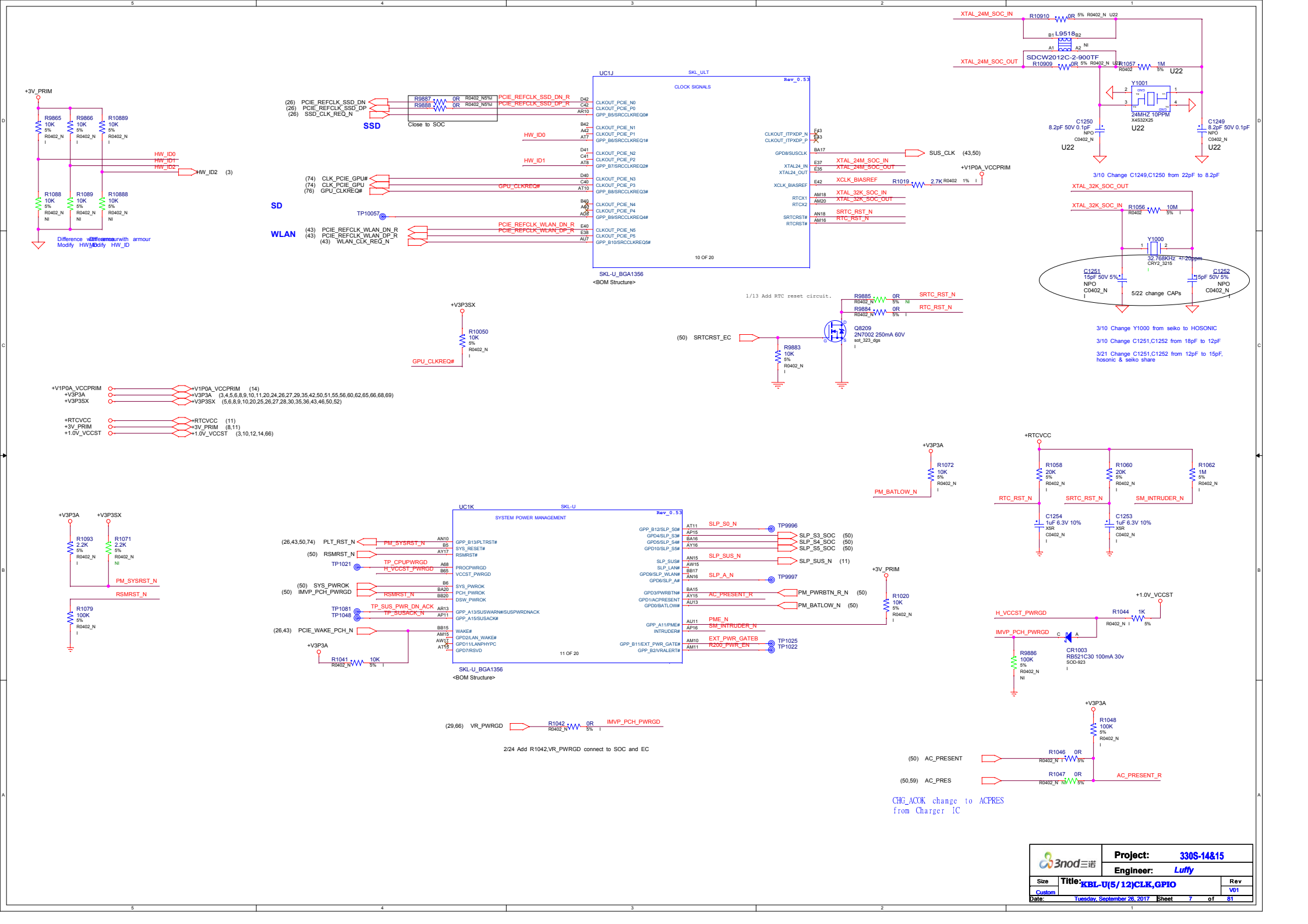
+3V_PRIM
R9865 10K 5% R0402_N I
R9866 10K 5% R0402_N I
R10889 10K 5% R0402_N I
HW_ID0
HW_ID1
HW_ID2
HW_ID2 (3)
R1088 10K 5% R0402_N NI
R1089 10K 5% R0402_N NI
R10888 10K 5% R0402_N NI
Difference with armour Modify HW_ID
Difference with armour Modify HW_ID
UC1J
SKL_ULT
Rev_0.53
CLOCK SIGNALS
(26) PCIE_REFCLK_SSD_DN
(26) PCIE_REFCLK_SSD_DP
(26) SSD_CLK_REQ_N
R9887 0R R0402_N5%I
R9888 0R R0402_N5%I
PCIE_REFCLK_SSD_DN_R
PCIE_REFCLK_SSD_DP_R
SSD
Close to SOC
HW_ID0
HW_ID1
(74) CLK_PCIE_GPU#
(74) CLK_PCIE_GPU
(76) GPU_CLKREQ#
GPU_CLKREQ#
SD
TP10057
WLAN
(43) PCIE_REFCLK_WLAN_DN_R
(43) PCIE_REFCLK_WLAN_DP_R
(43) WLAN_CLK_REQ_N
PCIE_REFCLK_WLAN_DN_R
PCIE_REFCLK_WLAN_DP_R
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
GPD8/SUSCLK
SUS_CLK (43,50)
XTAL24_IN
XTAL24_OUT
XTAL_24M_SOC_IN
XTAL_24M_SOC_OUT
+V1P0A_VCCPRIM
XCLK_BIASREF
R1019 2.7K R0402 1%
XCLK_BIASREF
RTCX1
RTCX2
XTAL_32K_SOC_IN
XTAL_32K_SOC_OUT
SRTCRST#
RTCRST#
SRTC_RST_N
RTC_RST_N
10 OF 20
SKL-U_BGA1356
<BOM Structure>
XTAL_24M_SOC_IN
R10910 0R 5% R0402_N U22
L9518
SDCW2012C-2-900TF
XTAL_24M_SOC_OUT
R10909 0R 5% R0402_N U22
R1057 1M 5% R0402 U22
Y1001
24MHZ 10PPM
X4S32X25
C1250 8.2pF 50V 0.1pF NPO C0402_N U22
C1249 8.2pF 50V 0.1pF NPO C0402_N U22
3/10 Change C1249,C1250 from 22pF to 8.2pF
XTAL_32K_SOC_OUT
XTAL_32K_SOC_IN
R1056 10M 5% R0402 I
Y1000
32.768KHz +/-20ppm
CRY2_3215
C1251 15pF 50V 5% NPO C0402_N I
C1252 15pF 50V 5% NPO C0402_N I
5/22 change CAPs
3/10 Change Y1000 from seiko to HOSONIC
3/10 Change C1251,C1252 from 18pF to 12pF
3/21 Change C1251,C1252 from 12pF to 15pF, hosonic & seiko share
+V3P3SX
R10050 10K 5% R0402_N I
GPU_CLKREQ#
1/13 Add RTC reset circuit.
R9885 0R R0402_N 5% NI SRTC_RST_N
R9884 0R R0402_N 5% I RTC_RST_N
(50) SRTCRST_EC
R9883 10K 5% R0402_N I
Q8209 2N7002 250mA 60V sot_323_dgs I
+V1P0A_VCCPRIM
+V3P3A
+V3P3SX
+V1P0A_VCCPRIM (14)
+V3P3A (3,4,5,6,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)
+V3P3SX (5,6,8,9,10,20,25,26,27,28,30,35,36,43,46,50,52)
+RTCVCC
+3V_PRIM
+1.0V_VCCST
+RTCVCC (11)
+3V_PRIM (8,11)
+1.0V_VCCST (3,10,12,14,66)
+V3P3A
R1072 10K 5% R0402_N I
PM_BATLOW_N
+RTCVCC
R1058 20K 5% R0402_N I
R1060 20K 5% R0402_N I
R1062 1M 5% R0402_N I
RTC_RST_N
SRTC_RST_N
SM_INTRUDER_N
C1254 1uF 6.3V 10% X5R C0402_N I
C1253 1uF 6.3V 10% X5R C0402_N I
+V3P3A
+V3P3SX
R1093 2.2K 5% R0402_N I
R1071 2.2K 5% R0402_N NI
PM_SYSRST_N
RSMRST_N
R1079 100K 5% R0402_N I
UC1K
SKL-U
Rev_0.53
SYSTEM POWER MANAGEMENT
(26,43,50,74) PLT_RST_N
PM_SYSRST_N
GPP_B13/PLTRST#
SYS_RESET#
(50) RSMRST_N
RSMRST#
TP1021
TP_CPUPWRGD
H_VCCST_PWRGD
PROCPWRGD
VCCST_PWRGD
(50) SYS_PWROK
(50) IMVP_PCH_PWRGD
RSMRST_N
SYS_PWROK
PCH_PWROK
DSW_PWROK
TP1081
TP1048
TP_SUS_PWR_DN_ACK
TP_SUSACK_N
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
(26,43) PCIE_WAKE_PCH_N
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD
+V3P3A
R1041 10K 5% R0402_N I
11 OF 20
SKL-U_BGA1356
<BOM Structure>
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_S0_N
TP9996
SLP_S3_SOC (50)
SLP_S4_SOC (50)
SLP_S5_SOC (50)
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
SLP_SUS_N
SLP_SUS_N (11)
SLP_A_N
TP9997
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
AC_PRESENT_R
PM_PWRBTN_R_N (50)
PM_BATLOW_N (50)
+3V_PRIM
R1020 10K 5% R0402_N I
GPP_A11/PME#
INTRUDER#
PME_N
SM_INTRUDER_N
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
EXT_PWR_GATEB
R200_PWR_EN
TP1025
TP1022
+1.0V_VCCST
H_VCCST_PWRGD
R1044 1K 5% R0402_N I
IMVP_PCH_PWRGD
R9886 100K 5% R0402_N NI
CR1003 RB521C30 100mA 30v SOD-923
(29,66) VR_PWRGD
R1042 0R 5% R0402_N I
IMVP_PCH_PWRGD
2/24 Add R1042,VR_PWRGD connect to SOC and EC
+V3P3A
R1048 100K 5% R0402_N I
(50) AC_PRESENT
R1046 0R 5% R0402_N I
(50,59) AC_PRES
R1047 0R 5% R0402_N NI
AC_PRESENT_R
CHG_ACOK change to ACPRES from Charger IC
3nod三诺
Project: 330S-14&15
Engineer: Luffy
Size Custom
Title: KBL-U(5/12)CLK,GPIO
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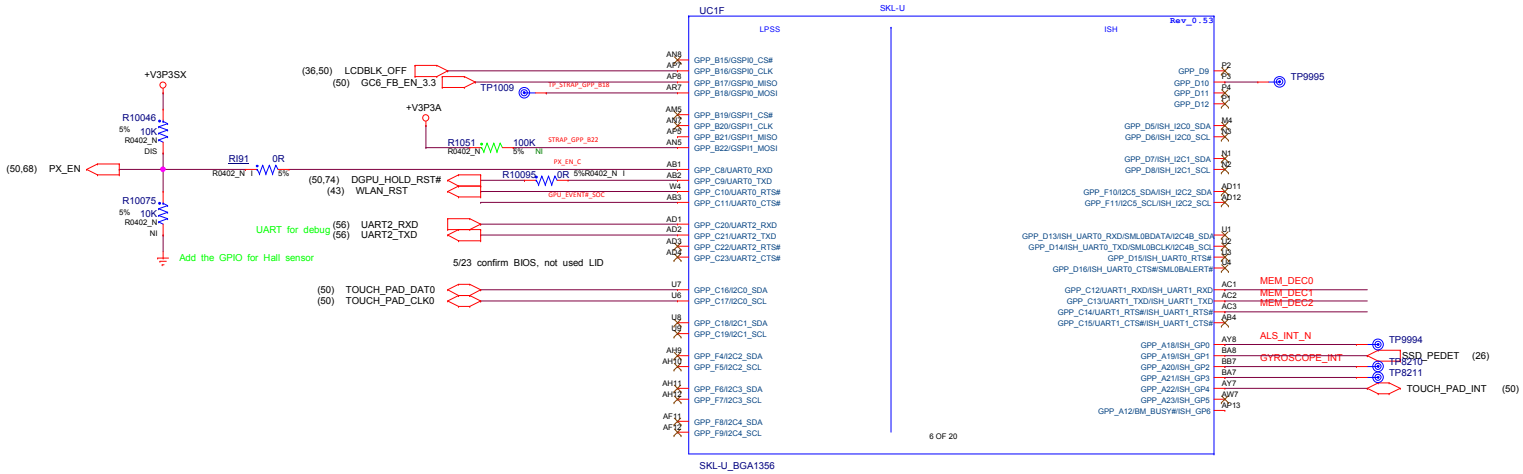
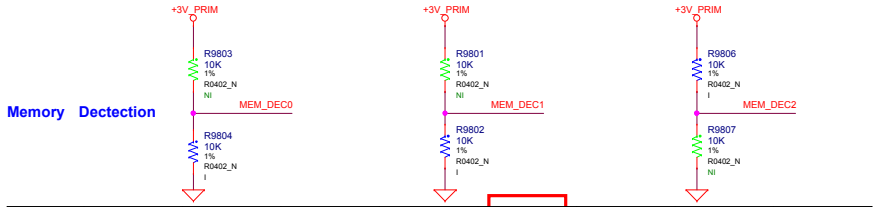


+3V_PRIM +3V_PRIM (7,11)
+V3P3SX +V3P3SX (5,6,7,9,10,20,25,26,27,28,30,35,36,43,46,50,52)
+V3P3A +V3P3A (3,4,5,6,7,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)

(76) GPU_EVENT# DIS SOD_323 BAT54WS D6607 GPU_EVENT#_SOC



Memory Dectection

	Samsung_4GB	Micron_4GB	Hynix_4GB	Samsung_8GB	Micron_8GB	Hynix_8GB	Samsung_16GB	Micron_16GB
MEM_DEC0	0	1	0	1	0	1	0	1
MEM_DEC1	0	0	1	1	0	0	1	1
MEM_DEC2	0	0	0	0	1	1	1	1

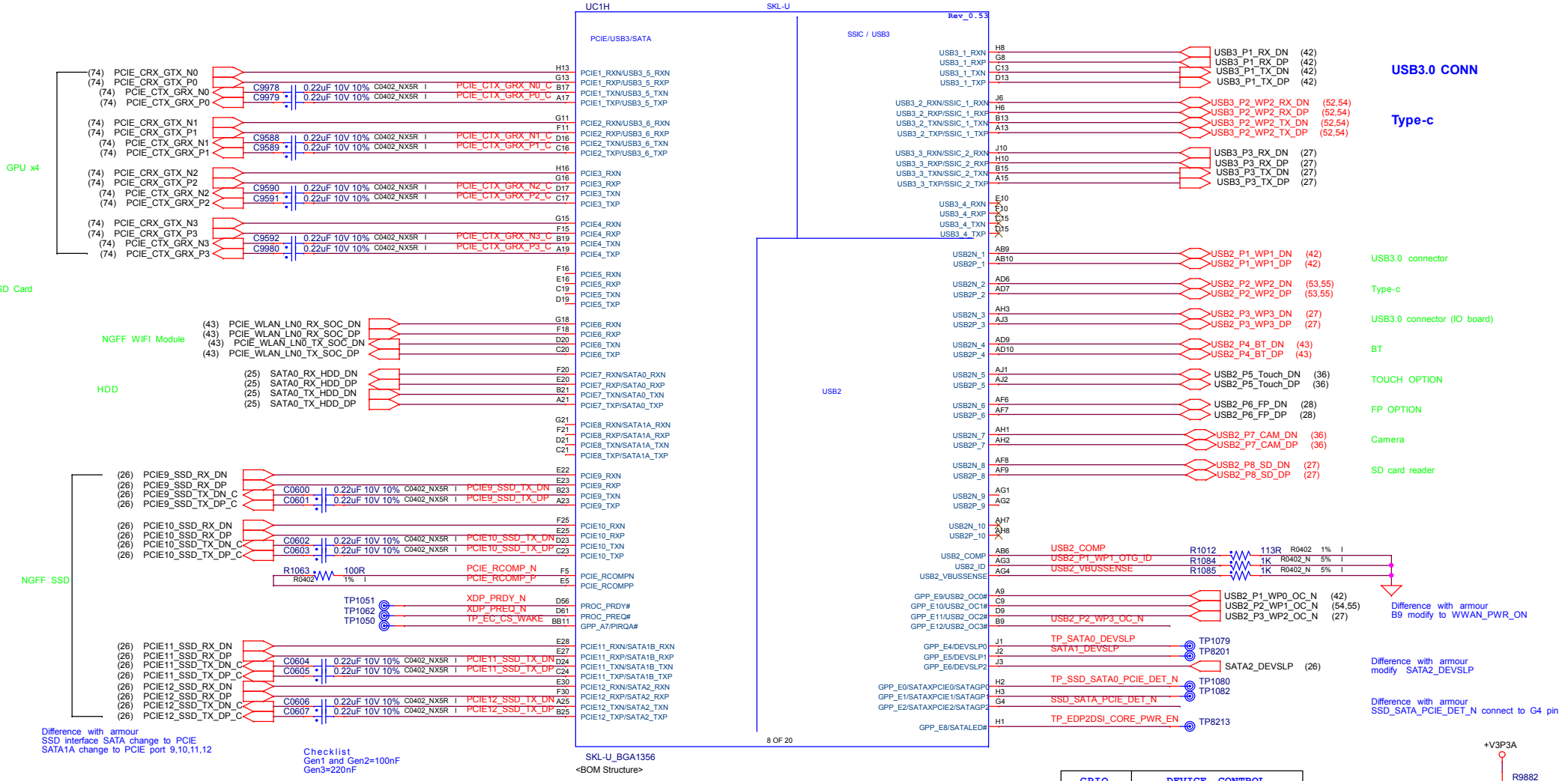
Default

GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Keyparts	Character	Supplier	Description	3NOD PN	Lenovo P/N
Lenovo B/S part sourcing plan					
CPU	Intel® 6th Gen Core™	Intel	i3-6100U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U_6th Gen Intel Core I i3-6100U 2.3G/2C/3M intel)	457100266700	SSA0K07374
		Intel	i5-6200U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U_6th Gen Intel Core I i5-6200U 2.3G/2C/3M intel)	457100266800	SSA0K07375
		Intel	i7-6500U 2.5G/2C/4M(CPU 7.5w BGA1356 2 Skylake-U_6th Gen Intel Core I i7-6500U 2.5G/2C/4M intel)	457100266900	SSA0K07377
DRAM	4Gbx16 DDR4 2400 SDRAM (單顆容量 0.5GB)	Samsung	K4A4G165WE-BCRC (MEMORY DDR4-2400 256Mx16 96FBGA K4A4G165WE-BCRC Samsung SM30L08878)	403670650600	SM30L08878
		Micron(Elpida)	MT40A256M16GE-083E:B		SM30L08871
		Hynix	H5AN4G6NAFR-UHC (MEMORY DDR4 2400 256M x 16 96ball FBGA H5AN4G6NAFR-UHC Hynix SM30L08876)	403670650800	SM30L08876
	8Gbx16 DDR4 2400 SDRAM (單顆容量 1GB)	Samsung	K4A8G165WB-BCRC (MEMORY DDR4-2400 512Mx16 96FBGA K4A8G165WB-BCRC Samsung SM30L08874)	403670650700	SM30L08874
		Micron(Elpida)	MT40A512M16JY-083E:B	403670650900	SM30L08877
		Hynix	H5AN8G6NAFR-UHC (MEMORY DDR4 2400 512M*16 96FBGA MT40A512M16JY-083E:B Micron SM30L08877)		SM30L08875

3nod三诺

Project:	330S-14&15
Engineer:	Luffy
Size: Custom	Title: KBL-U(6/12)GPIO
Rev	V01
Date: Tuesday, September 26, 2017	Sheet 8 of 81



High Speed I/O (HSIO) Lane Multiplexing in SKL U

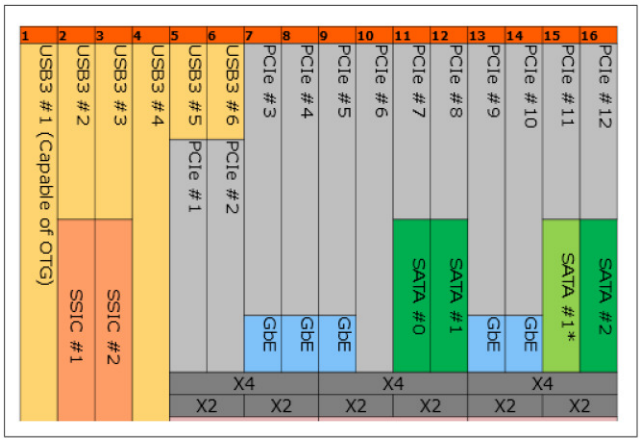


Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

GPIO	DEVICE CONTROL
USB_OC0#	Type C
USB_OC1#	USB2 Port 2
USB_OC2#	NA
USB_OC3#	WWAN_PWR_ON
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NGFF SSD KEY M
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	SSD_SATA_PCIE_DET_N

+V3P3A
+V3P3SX (5,6,7,8,10,20,25,26,27,28,30,35,36,43,46,50,52)

Project:	330S-14&15
Engineer:	Luffy
Size: Custom	Title: KBL-U(7/12)PCIE,USB,SATA
Rev: V01	
Date: Tuesday, September 26, 2017	Sheet 9 of 81

20170718
yanzw
genhuan

11/17 Follow 543977_SKL_PDDG_Rev0_91
CC95 10PF ->22us(Spec:<= 65us)

1/4 modify OK

+1.0V_PRIM to +1.0VS_VCCSTG / +1.0VS_VCCIO

2/24 pin9 connect GND,need change to +1.0V_PRIM

5/31 add CAP, change to 330uF

Imax : 2.73 A

5/31 uninstall CAPs
1/27 Intel Add 10uF x2

PSC Side

BSC Side

RC208 Follow 544669_SKL_U__DDR3L_RVP7_Schematic_Rev1.0

+1.0V_PRIM to +1.0V_VCCSTU

+1.8V_PRIM to +V1P8S

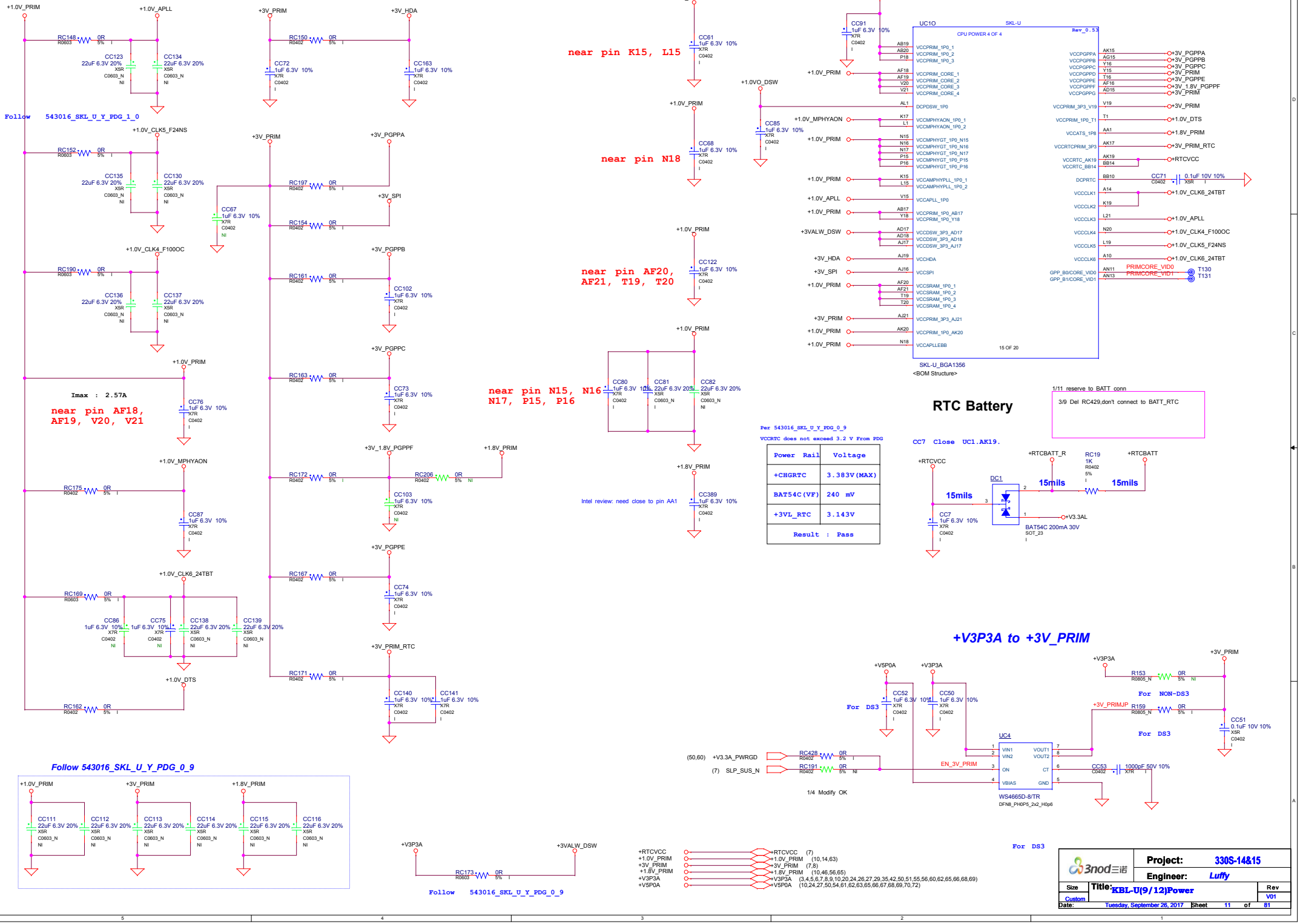
11/24 椒 椒+V1P8 S
for Finger print,Audio codec

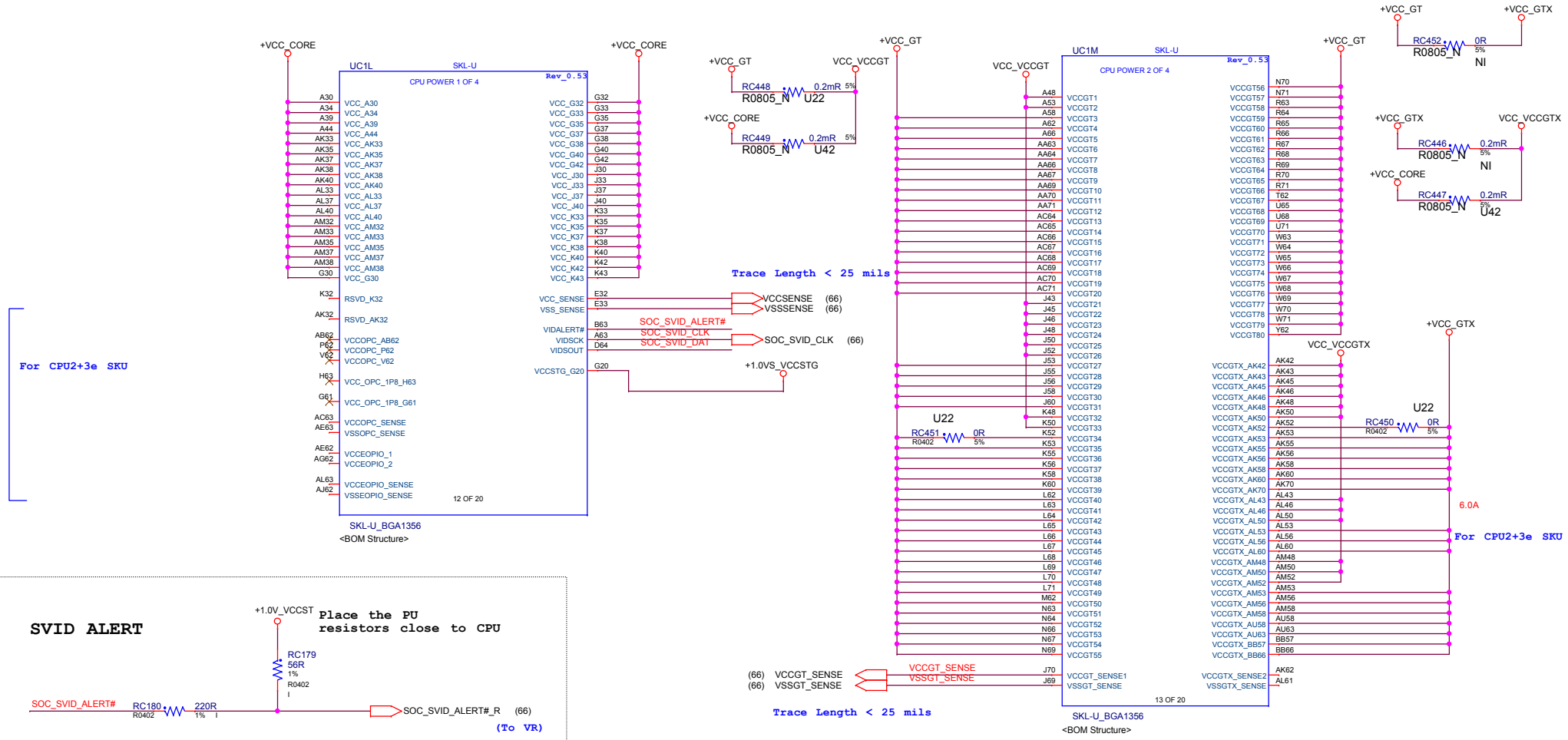
RC208 Follow 544669_SKL_U__DDR3L_RVP7_Schematic_Rev0_53

CC47 Follow 543016_SKL_U_Y_PDG_0_9

+V1P2U_VDDQ: 10UF/6.3V/0603 *4
22UF/6.3V/0402 *3

3nod三诺	Project:	330S-14&15	
	Engineer:	Luffy	
Size: C	Title:	KBL-U(8/12)Power	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 10 of 81		


+1.0V_PRIM
+1.0V_APLL
RC148 0R R0603
CC123 22uF 6.3V 20% X5R C0603_N NI
CC134 22uF 6.3V 20% X5R C0603_N NI
Follow 543016_SKL_U_Y_PDG_1_0
+1.0V_CLK5_F24NS
RC152 0R R0603
CC135 22uF 6.3V 20% X5R C0603_N NI
CC130 22uF 6.3V 20% X5R C0603_N NI
+1.0V_CLK4_F100OC
RC190 0R R0603
CC136 22uF 6.3V 20% X5R C0603_N NI
CC137 22uF 6.3V 20% X5R C0603_N NI
+1.0V_PRIM
Imax : 2.57A
near pin AF18, AF19, V20, V21
CC76 1uF 6.3V 10% X7R C0402
+1.0V_MPHYAON
RC175 0R R0402
CC87 1uF 6.3V 10% X7R C0402
+1.0V_CLK6_24TBT
RC169 0R R0603
CC86 1uF 6.3V 10% X7R C0402 NI
CC75 1uF 6.3V 10% X7R C0402 NI
CC138 22uF 6.3V 20% X5R C0603_N NI
CC139 22uF 6.3V 20% X5R C0603_N NI
+1.0V_DTS
RC162 0R R0402
+3V_PRIM
RC150 0R R0402
CC72 1uF 6.3V 10% X7R C0402
+3V_HDA
CC163 1uF 6.3V 10% X7R C0402
+3V_PRIM
RC197 0R R0402
CC67 1uF 6.3V 10% X7R C0402 NI
+3V_PGPPA
+3V_SPI
RC154 0R R0402
+3V_PGPPB
RC161 0R R0402
CC102 1uF 6.3V 10% X7R C0402
+3V_PGPPC
RC163 0R R0402
CC73 1uF 6.3V 10% X7R C0402
+3V_1.8V_PGPPF
+1.8V_PRIM
RC172 0R R0402
RC206 0R R0402 5% NI
CC103 1uF 6.3V 10% X7R C0402 NI
+3V_PGPPE
RC167 0R R0402
CC74 1uF 6.3V 10% X7R C0402
+3V_PRIM_RTC
RC171 0R R0402
CC140 1uF 6.3V 10% X7R C0402
CC141 1uF 6.3V 10% X7R C0402
Follow 543016_SKL_U_Y_PDG_0_9
+1.0V_PRIM
CC111 22uF 6.3V 20% X5R C0603_N NI
CC112 22uF 6.3V 20% X5R C0603_N NI
+3V_PRIM
CC113 22uF 6.3V 20% X5R C0603_N NI
CC114 22uF 6.3V 20% X5R C0603_N NI
+1.8V_PRIM
CC115 22uF 6.3V 20% X5R C0603_N NI
CC116 22uF 6.3V 20% X5R C0603_N NI
+1.0V_PRIM
near pin K15, L15
CC61 1uF 6.3V 10% X7R C0402
+1.0V_PRIM
near pin N18
CC68 1uF 6.3V 10% X7R C0402
+1.0V_PRIM
near pin AF20, AF21, T19, T20
CC122 1uF 6.3V 10% X7R C0402
+1.0V_PRIM
near pin N15, N16 N17, P15, P16
CC80 1uF 6.3V 10% X7R C0402
CC81 22uF 6.3V 20% X5R C0603_N NI
CC82 22uF 6.3V 20% X5R C0603_N NI
+1.8V_PRIM
Intel review: need close to pin AA1
CC389 1uF 6.3V 10% X7R C0402
+1.0V_PRIM
CC91 1uF 6.3V 10% X7R C0402
+1.0VO_DSW
CC85 1uF 6.3V 10% X7R C0402
+1.0V_PRIM
+1.0V_MPHYAON
+1.0V_PRIM
+1.0V_APLL
+1.0V_PRIM
+3VALW_DSW
+3V_HDA
+3V_SPI
+1.0V_PRIM
+3V_PRIM
+1.0V_PRIM
+1.0V_PRIM
UC1O SKL-U
CPU POWER 4 OF 4
Rev_0.53
VCCPRIM_1P0_1
VCCPRIM_1P0_2
VCCPRIM_1P0_3
VCCPRIM_CORE_1
VCCPRIM_CORE_2
VCCPRIM_CORE_3
VCCPRIM_CORE_4
DCPDSW_1P0
VCCMPHYAON_1P0_1
VCCMPHYAON_1P0_2
VCCMPHYGT_1P0_N15
VCCMPHYGT_1P0_N16
VCCMPHYGT_1P0_N17
VCCMPHYGT_1P0_P15
VCCMPHYGT_1P0_P16
VCCAMPHYPLL_1P0_1
VCCAMPHYPLL_1P0_2
VCCAPLL_1P0
VCCPRIM_1P0_AB17
VCCPRIM_1P0_Y18
VCCDSW_3P3_AD17
VCCDSW_3P3_AD18
VCCDSW_3P3_AJ17
VCCHDA
VCCSPI
VCCSRAM_1P0_1
VCCSRAM_1P0_2
VCCSRAM_1P0_3
VCCSRAM_1P0_4
VCCPRIM_3P3_AJ21
VCCPRIM_1P0_AK20
VCCAPLLEBB
15 OF 20
SKL-U_BGA1356
<BOM Structure>
VCCPGPPA +3V_PGPPA
VCCPGPPB +3V_PGPPB
VCCPGPPC +3V_PGPPC
VCCPGPPD +3V_PRIM
VCCPGPPE +3V_PGPPE
VCCPGPPF +3V_1.8V_PGPPF
VCCPGPPG +3V_PRIM
VCCPRIM_3P3_V19 +3V_PRIM
VCCPRIM_1P0_T1 +1.0V_DTS
VCCATS_1P8 +1.8V_PRIM
VCCRTCPRIM_3P3 +3V_PRIM_RTC
VCCRTC_AK19 VCCRTC_BB14 +RTCVCC
DCPRTC CC71 0.1uF 10V 10% X5R C0402
VCCCLK1 +1.0V_CLK6_24TBT
VCCCLK2
VCCCLK3 +1.0V_APLL
VCCCLK4 +1.0V_CLK4_F100OC
VCCCLK5 +1.0V_CLK5_F24NS
VCCCLK6 +1.0V_CLK6_24TBT
GPP_B0/CORE_VID0 PRIMCORE_VID0 T130
GPP_B1/CORE_VID1 PRIMCORE_VID1 T131
Per 543016_SKL_U_Y_PDG_0_9
VCCRTC does not exceed 3.2 V From PDG
Power Rail | Voltage
+CHGRTC | 3.383V(MAX)
BAT54C(VF) | 240 mV
+3VL_RTC | 3.143V
Result : Pass
RTC Battery
1/11 reserve to BATT conn
3/9 Del RC429,don't connect to BATT_RTC
CC7 Close UC1.AK19.
+RTCVCC
15mils
CC7 1uF 6.3V 10% X7R C0402
DC1
+RTCBATT_R
15mils
RC19 1K R0402 5%
15mils
+RTCBATT
+V3.3AL
BAT54C 200mA 30V SOT_23
+V3P3A to +3V_PRIM
+V5P0A
+V3P3A
For DS3
CC52 1uF 6.3V 10% X7R C0402
CC50 1uF 6.3V 10% X7R C0402
(50,60) +V3.3A_PWRGD
(7) SLP_SUS_N
RC428 0R R0402
RC191 0R R0402 NI
EN_3V_PRIM
UC4
VIN1 VIN2 VOUT1 VOUT2 ON CT VBIAS GND
WS4665D-8/TR
DFN8_PH0P5_2x2_H0p6
CC53 1000pF 50V 10% X7R C0402
1/4 Modify OK
+3V_PRIM
+V3P3A
R153 0R R0805_N 5% NI
For NON-DS3
+3V_PRIMJP
R159 0R R0805_N 5%
For DS3
CC51 0.1uF 10V 10% X5R C0402
For DS3
+V3P3A
+3VALW_DSW
RC173 0R R0603 5%
Follow 543016_SKL_U_Y_PDG_0_9
+RTCVCC
+1.0V_PRIM
+3V_PRIM
+1.8V_PRIM
+V3P3A
+V5P0A
+RTCVCC (7)
+1.0V_PRIM (10,14,63)
+3V_PRIM (7,8)
+1.8V_PRIM (10,46,56,65)
+V3P3A (3,4,5,6,7,8,9,10,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)
+V5P0A (10,24,27,50,54,61,62,63,65,66,67,68,69,70,72)
3nod三诺
Project: 330S-14&15
Engineer: Luffy
Size Custom
Title: KBL-U(9/12)Power
Rev V01
Date: Tuesday, September 26, 2017 Sheet 11 of 81

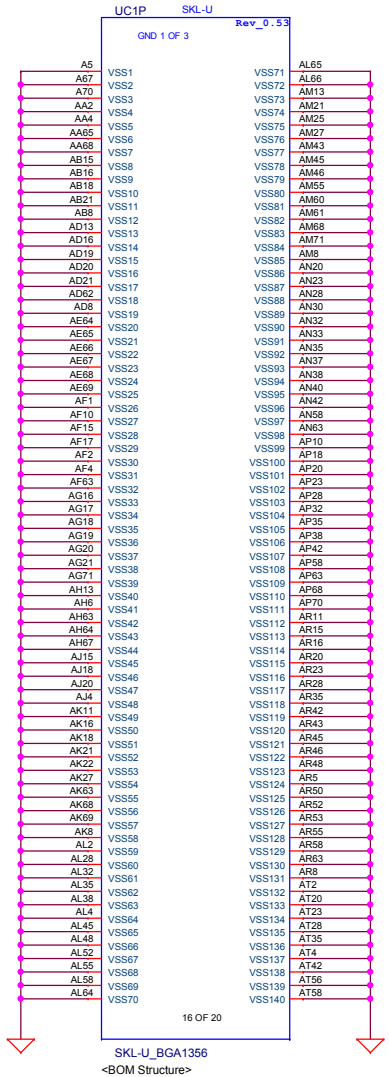


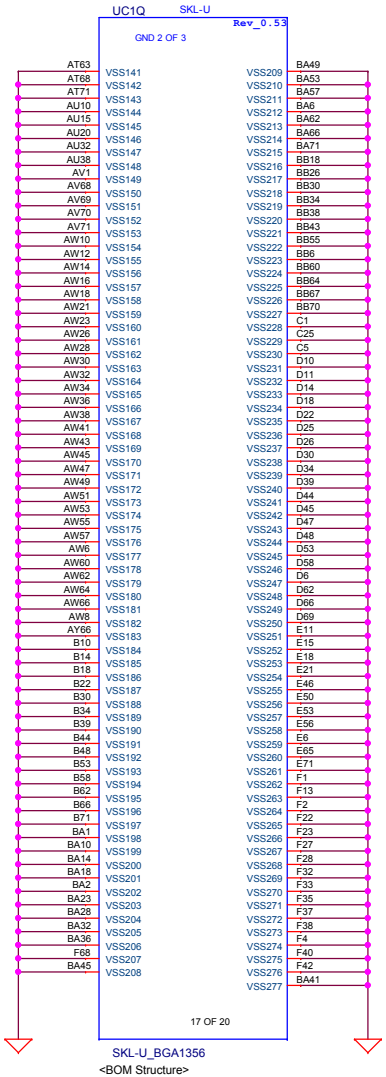
Package Sensing Recommendations

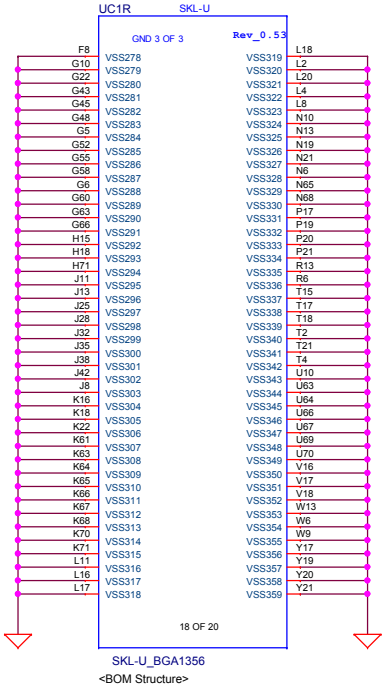
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
V_{CC_SENSE} / V_{SS_SENSE}	100Ω	50Ω	<25 mils
V_{CCGT_SENSE} / V_{SSGT_SENSE}			
V_{CCGTx_SENSE} / V_{SSGTx_SENSE}			
V_{CCSA_SENSE} / V_{SSSA_SENSE}			
V_{CCIO_SENSE} / V_{SSIO_SENSE}[1]		NA	

Note: [1] Does not apply when rails are merged.

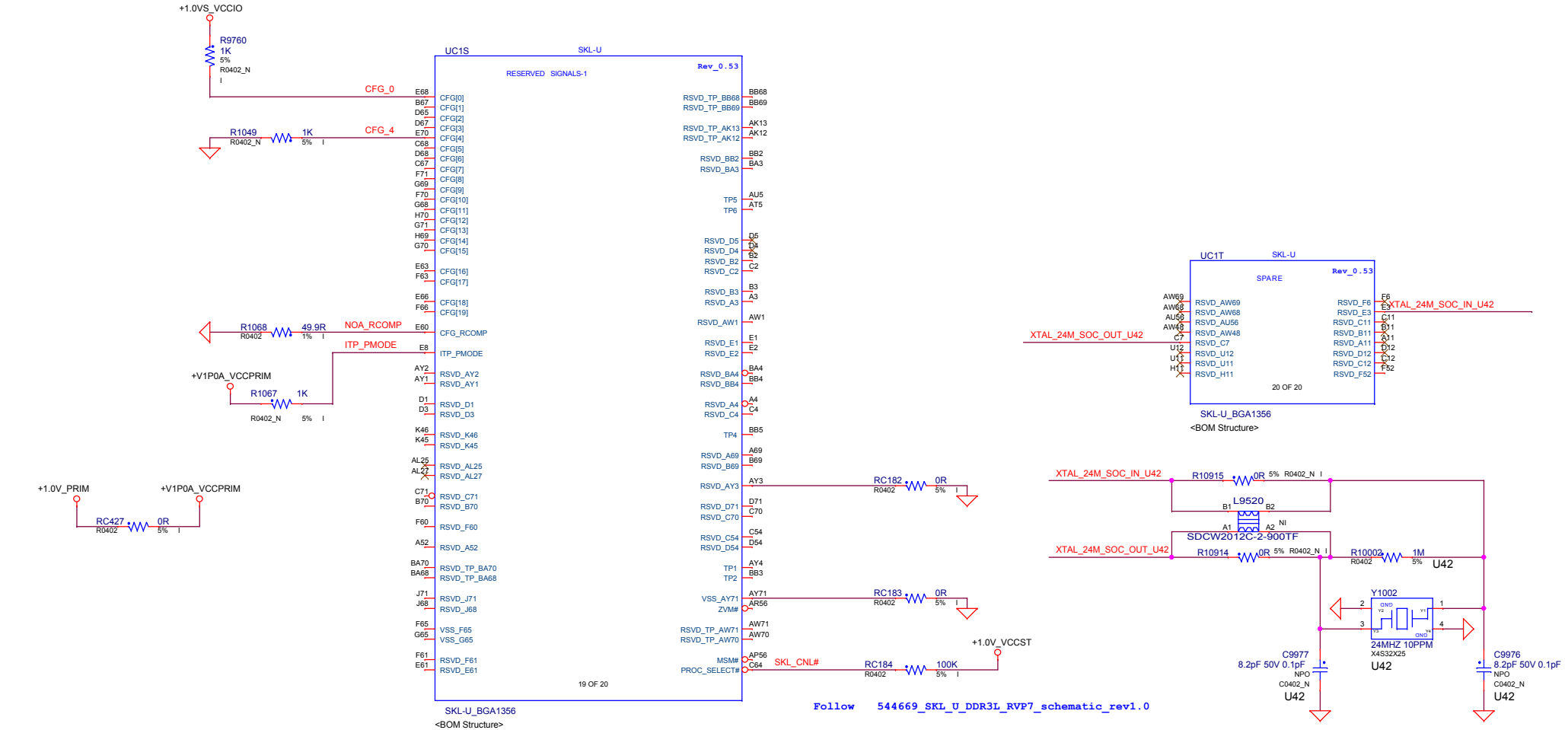
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: KBL-U(10/12)Power,SVID	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 12 of 81	







3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: KBL-U(11/12)GND	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 13 of 81	



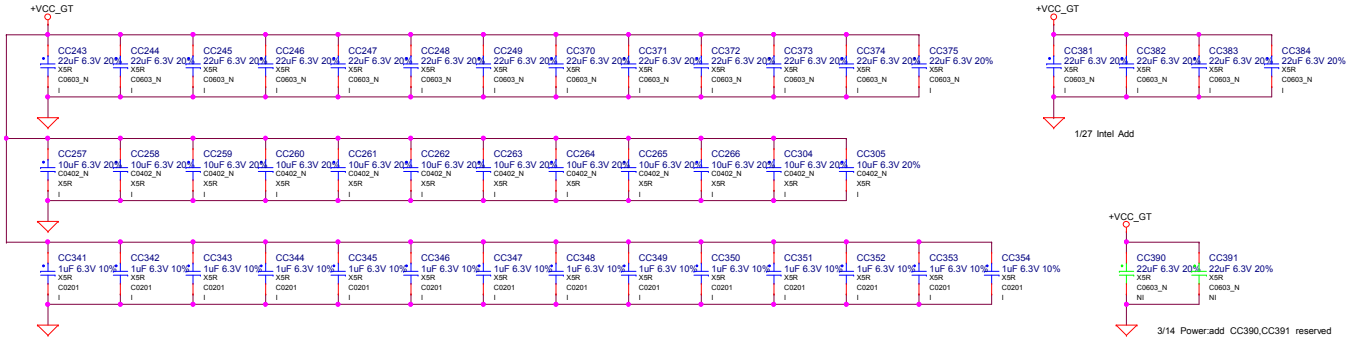
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: KBL-U(12/12)RSVD	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 14 of 81	

12/30 check PDG
& 220uF pull power side

+VCC_CORE

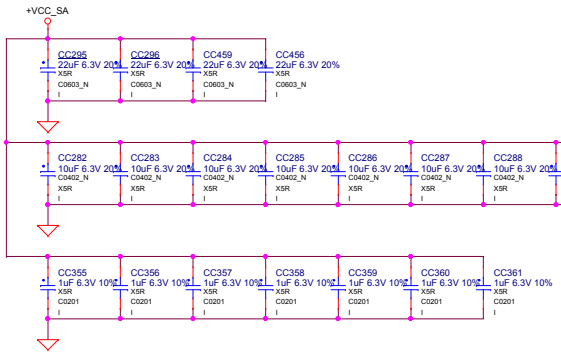
47uF	x8	change	47uF x4
22uF	x9	cgange	22uF x17
10uF	x15		
1uF	x35		



12/30 check PDG
& 220uF pull power side

+VCC_GT

47uF	x3	change	47uF x0
22uF	x7	cgange	22uF x13
10uF	x12		
1uF	x14		



+VCC_SA

47uF	x2		
10uF	x13		
1uF	x7		

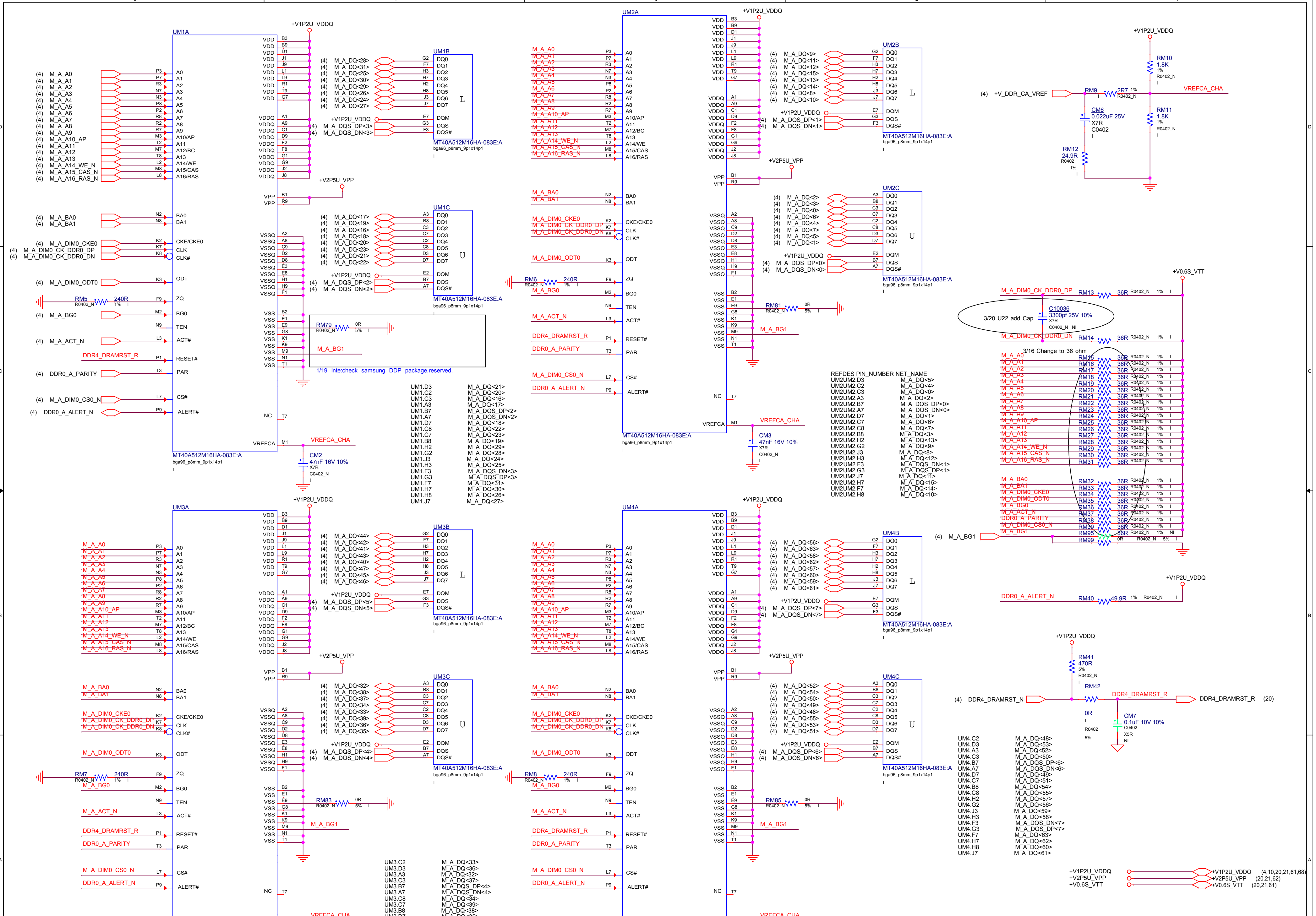
12/30 check PDG

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: C	Title: SOC (DECOUPLING)	Rev: V01
Date: Wednesday, September 27, 2017	Sheet 15 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: *Luffy*	
Size: B	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 16 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: *Luffy*	
Size: B	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 17 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 18 of 81	


UM1A
UM1B
UM1C
UM2A
UM2B
UM2C
UM3A
UM3B
UM3C
UM4A
UM4B
UM4C
MT40A512M16HA-083E:A
bga96_p8mm_9p1x14p1
+V1P2U_VDDQ
+V2P5U_VPP
+V0.6S_VTT
VREFCA_CHA
(4) +V_DDR_CA_VREF
RM9 2R7 1% R0402_N
RM10 1.8K 1% R0402_N
RM11 1.8K 1% R0402_N
RM12 24.9R R0402 1%
CM6 0.022uF 25V X7R C0402
CM2 47nF 16V 10% X7R C0402_N
CM3 47nF 16V 10% X7R C0402_N
CM4 47nF 16V 10% X7R C0402_N
CM5 47nF 16V 10% X7R C0402_N
RM5 240R 1% R0402_N
RM6 240R 1% R0402_N
RM7 240R 1% R0402_N
RM8 240R 1% R0402_N
RM79 0R 5% R0402_N
RM81 0R 5% R0402_N
RM83 0R 5% R0402_N
RM85 0R 5% R0402_N
1/19 Inte:check samsung DDP package,reserved.
3/20 U22 add Cap
C10036 3300pf 25V 10% X7R C0402_N NI
3/16 Change to 36 ohm
RM13 36R R0402_N 1%
RM14 36R R0402_N 1%
RM15 – RM38 36R R0402_N 1%
RM95 36R R0402_N 1% NI
RM99 0R R0402_N 5%
RM40 49.9R 1% R0402_N
DDR0_A_ALERT_N
RM41 470R 5% R0402_N
RM42 0R R0402 5%
CM7 0.1uF 10V 10% C0402 X5R NI
(4) DDR4_DRAMRST_N
DDR4_DRAMRST_R (20)
+V1P2U_VDDQ (4,10,20,21,61,68)
+V2P5U_VPP (20,21,62)
+V0.6S_VTT (20,21,61)
UM1.D3 M_A_DQ<21>
UM1.C2 M_A_DQ<20>
UM1.C3 M_A_DQ<16>
UM1.A3 M_A_DQ<17>
UM1.B7 M_A_DQS_DP<2>
UM1.A7 M_A_DQS_DN<2>
UM1.D7 M_A_DQ<18>
UM1.C8 M_A_DQ<22>
UM1.C7 M_A_DQ<23>
UM1.B8 M_A_DQ<19>
UM1.H2 M_A_DQ<29>
UM1.G2 M_A_DQ<28>
UM1.J3 M_A_DQ<24>
UM1.H3 M_A_DQ<25>
UM1.F3 M_A_DQS_DN<3>
UM1.G3 M_A_DQS_DP<3>
UM1.F7 M_A_DQ<31>
UM1.H7 M_A_DQ<30>
UM1.H8 M_A_DQ<26>
UM1.J7 M_A_DQ<27>
REFDES PIN_NUMBER NET_NAME
UM2UM2.D3 M_A_DQ<5>
UM2UM2.C2 M_A_DQ<4>
UM2UM2.C3 M_A_DQ<0>
UM2UM2.A3 M_A_DQ<2>
UM2UM2.B7 M_A_DQS_DP<0>
UM2UM2.A7 M_A_DQS_DN<0>
UM2UM2.D7 M_A_DQ<1>
UM2UM2.C7 M_A_DQ<6>
UM2UM2.C8 M_A_DQ<7>
UM2UM2.B8 M_A_DQ<3>
UM2UM2.H2 M_A_DQ<13>
UM2UM2.G2 M_A_DQ<8>
UM2UM2.J3 M_A_DQ<9>
UM2UM2.H3 M_A_DQ<12>
UM2UM2.F3 M_A_DQS_DN<1>
UM2UM2.G3 M_A_DQS_DP<1>
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UM2UM2.F7 M_A_DQ<14>
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UM3.C2 M_A_DQ<33>
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UM3.B7 M_A_DQS_DP<4>
UM3.A7 M_A_DQS_DN<4>
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UM3.G2 M_A_DQ<44>
UM3.H3 M_A_DQ<45>
UM3.J3 M_A_DQ<41>
UM3.F3 M_A_DQS_DN<5>
UM3.G3 M_A_DQS_DP<5>
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UM4.G3 M_A_DQS_DP<7>
UM4.F7 M_A_DQ<63>
UM4.H7 M_A_DQ<62>
UM4.H8 M_A_DQ<60>
UM4.J7 M_A_DQ<61>

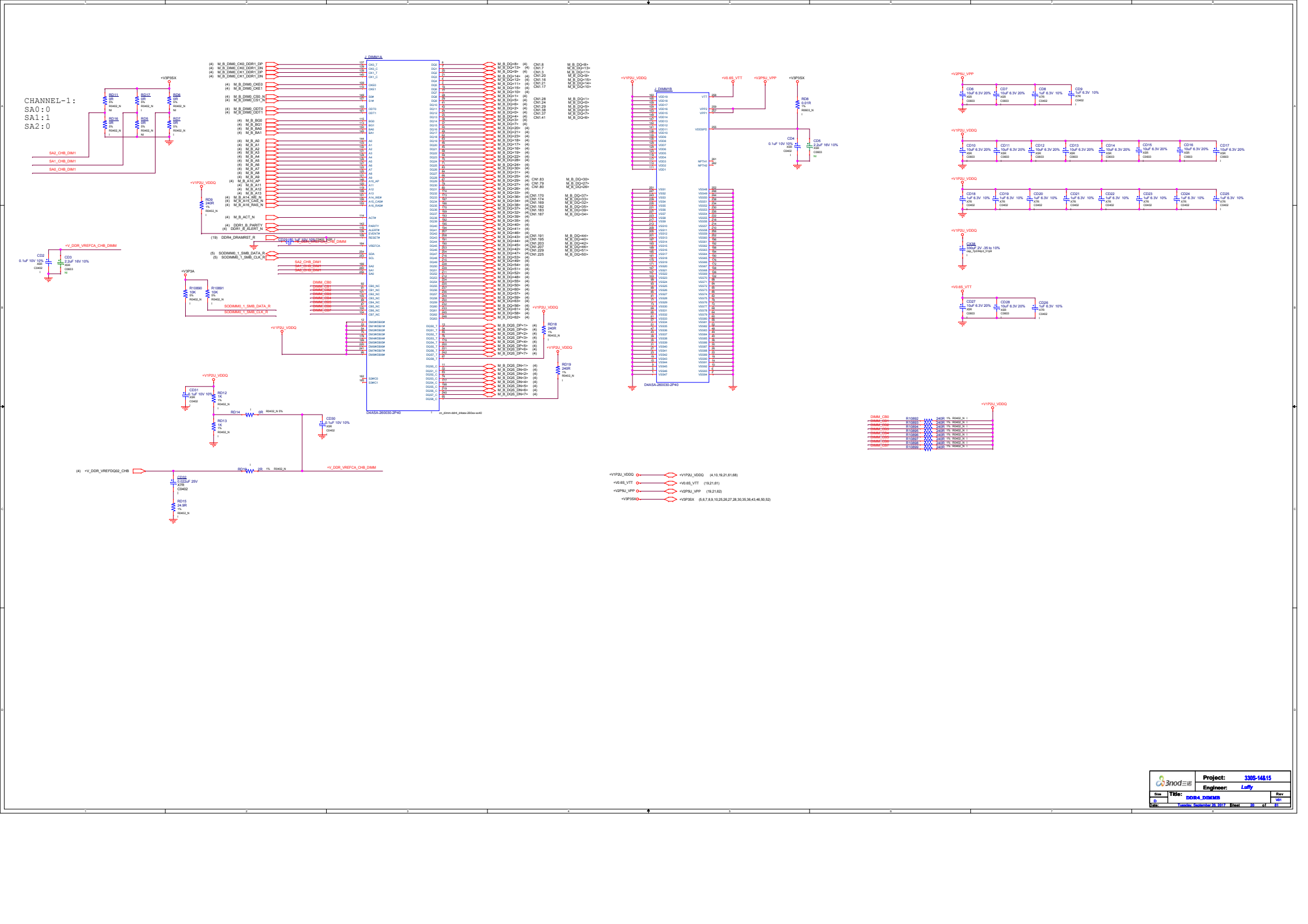
3nod 三诺

Project: 330S-14&15

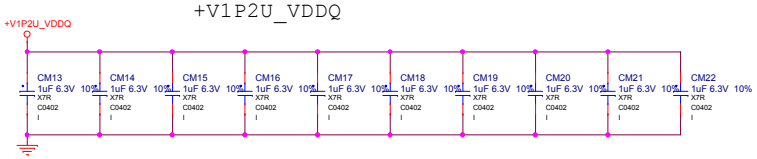
Engineer: Luffy

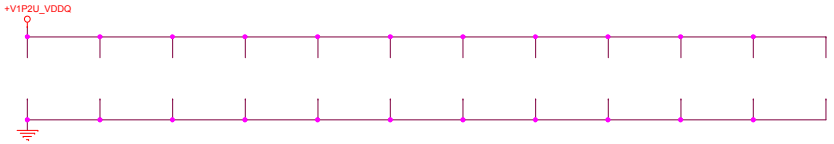
Size	Title: DDR4_CHA	Rev
C		V01

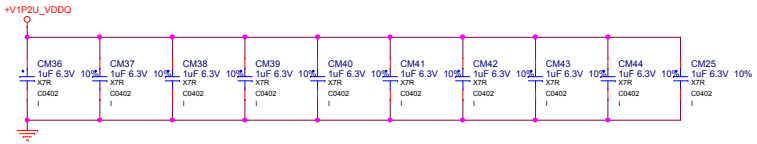
Date: Tuesday, September 26, 2017 Sheet 19 of 81


CHANNEL-1:
SA0:0
SA1:1
SA2:0
SA2_CHB_DIM1
SA1_CHB_DIM1
SA0_CHB_DIM1
+V3P3SX
RD11 0R 5% R0402_N NI
RD17 0R 5% R0402_N NI
RD8 0R 5% R0402_N NI
RD16 0R 5% R0402_N NI
RD6 0R 5% R0402_N NI
RD7 0R 5% R0402_N NI
J_DIMM1A
J_DIMM1B
04ASA-2B0030-2F40
cn_dimm-ddr4_d4asa-260xx-sv40
+V1P2U_VDDQ
+V0.6S_VTT
+V2P5U_VPP
+V3P3A
+V_DDR_VREFCA_CHB_DIMM
+V_DDR_VREFDQ02_CHB
DIMM_CB0
SODIMM0_1_SMB_DATA_R
SODIMM0_1_SMB_CLK_R
DDR4_DRAMRST_R
M_B_DIMM_CK0_DDR1_DP
M_B_DIMM_CK0_DDR1_DN
M_B_DIMM_CK1_DDR1_DP
M_B_DIMM_CK1_DDR1_DN
M_B_DIMM_CKE0
M_B_DIMM_CKE1
M_B_DIMM_CS0_N
M_B_DIMM_CS1_N
M_B_DIMM_ODT0
M_B_DIMM_ODT1
M_B_BG0
M_B_BG1
M_B_BA0
M_B_BA1
M_B_ACT_N
DDR1_B_PARITY
DDR1_B_ALERT_N
M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7
M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15
M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23
M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31
M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39
M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47
M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55
M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63
M_B_DQS_DP<1:0> M_B_DQS_DP<3:2> M_B_DQS_DP<5:4> M_B_DQS_DP<7:6>
M_B_DQS_DN<1:0> M_B_DQS_DN<3:2> M_B_DQS_DN<5:4> M_B_DQS_DN<7:6>
+V1P2U_VDDQ (4,10,19,21,61,68)
+V0.6S_VTT (19,21,61)
+V2P5U_VPP (19,21,62)
+V3P3SX (5,6,7,8,9,10,25,26,27,28,30,35,36,43,46,50,52)
Project: 330S-14&15
Engineer: Luffy
Title: DDR4_DIMMB
Rev V01
Date: Tuesday, September 26, 2017 Sheet 20 of 51

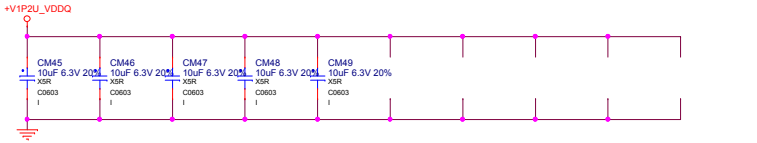
+V1P2U_VDDQ





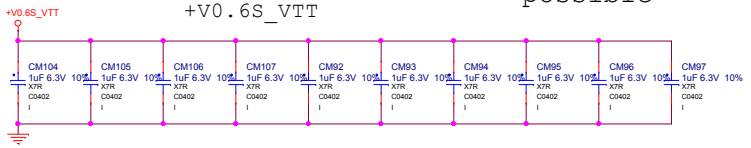


1uF:4 as near each x16 DRAM device as possible

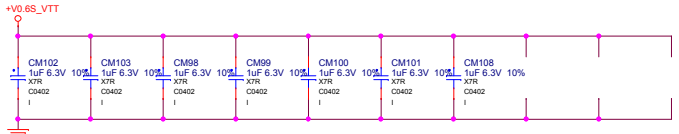


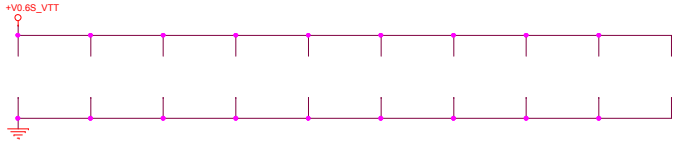
10uF:Distributed around the DRAM devices

+V0.6S_VTT

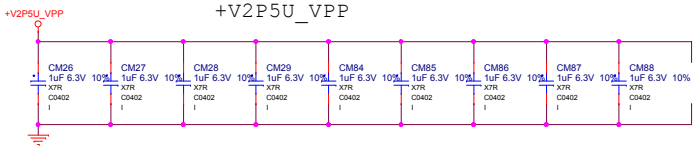


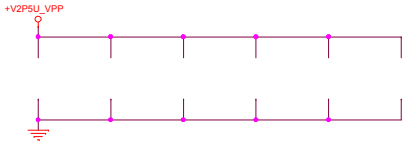
1uF:2 as near each x20 DRAM device as possible



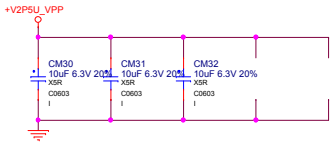


+V2P5U_VPP

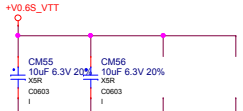




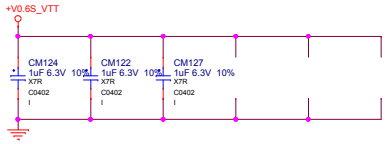
1uF:2 as near each x16 DRAM device as possible



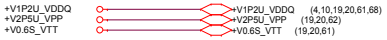
10uF:Distributed around the DRAM devices



10uF:Distributed around the DRAM devices



3/31 add CAPs

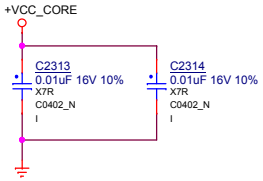


3nod三诺	Project: 330S-1415	
	Engineer: Luffy	
Size: C	Title: DDR4 Decoupling	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 21 of 81	

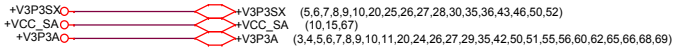
3nod三诺	Project: 330S-14&15	
	Engineer: *Luffy*	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 22 of 81	

RF Solution

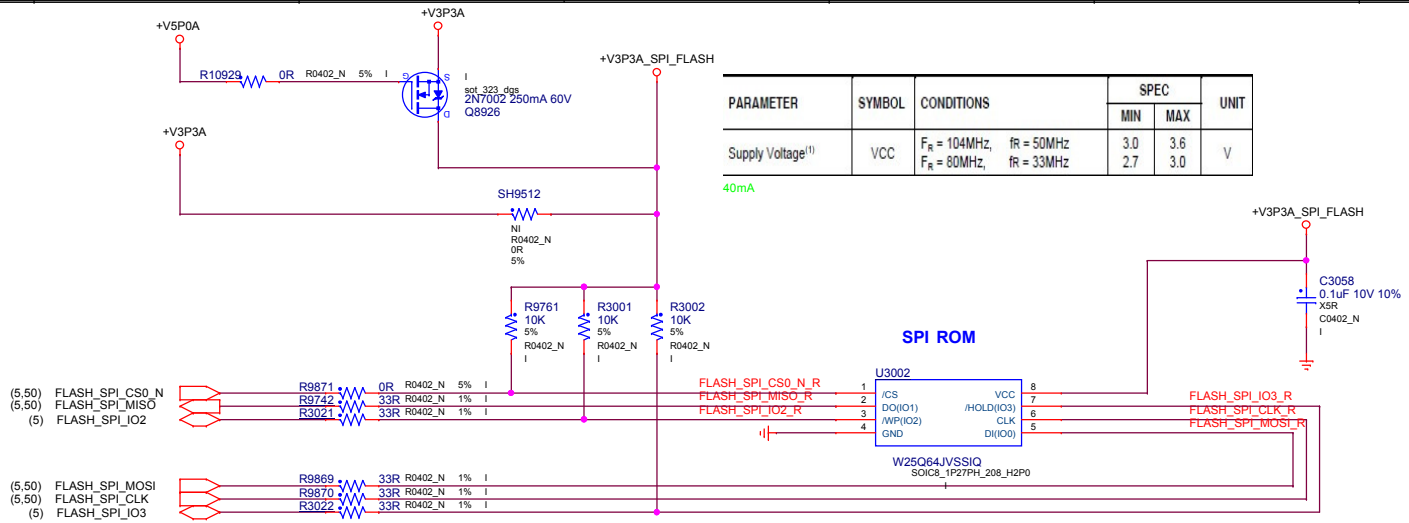
Cross Moat Cap.



EMC Solution



3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: RF / EMC Solution	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 23 of 81	



PARAMETER	SYMBOL	CONDITIONS	SPEC MIN	SPEC MAX	UNIT
Supply Voltage(1)	VCC	F_R = 104MHz, fR = 50MHz	3.0	3.6	V
		F_R = 80MHz, fR = 33MHz	2.7	3.0	

40mA

Difference with ARMOUR
Series-resistor 0R
change to 33R

4/5 Remove BIOS Socket

ROM Socket

2/24 SIV:Delet ROM Socket @U3002

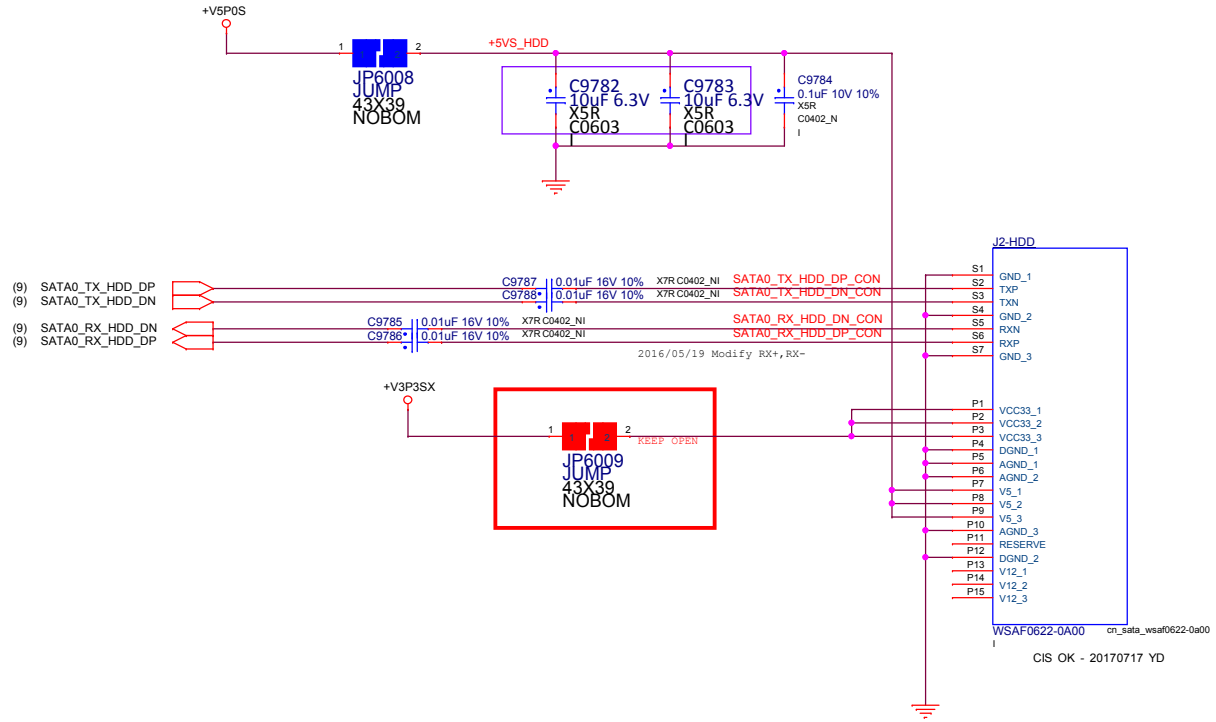
+V3P3A +V3P3A (3,4,5,6,7,8,9,10,11,20,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:52 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: SYSTEM FLASH	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 24 of 81	



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BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:52 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: HDD	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 25 of 81	

M.2 SSD Module

1.4A @ADATA 128GB SSD
2.6A @ADATA 256GB SSD

+V3P3SX — SH4200 — +V3P3A_SSD

SH4200: 0R, I, R0805_N, 5%

Change SH4200 0805 shunt to resistor

+V3P3A_SSD

C4209	C4204	C4205	C4206	C4207	C4208
22uF 6.3V 20%	22uF 6.3V 20%	0.1uF 10V 10%	0.1uF 10V 10%	0.1uF 10V 10%	0.1uF 10V 10%
X5R	X5R	X5R	X5R	X5R	X5R
C0603_N	C0603_N	C0402_N	C0402_N	C0402_N	C0402_N
I	I	I	I	I	I

JSSD1

1	GND_1	2	3.3V_2
3	GND_3	4	3.3V_4
5	PERn3	6	Reserved_6
7	PERp3	8	Reserved_8
9	GND_9	10	DAS/DSS# (O)(OD)
11	PETn3	12	3.3V_12
13	PETp3	14	3.3V_14
15	GND_15	16	3.3V_16
17	PERn2	18	3.3V_18
19	PERp2	20	Reserved_20
21	GND_21	22	Reserved_22
23	PETn2	24	Reserved_24
25	PETp2	26	Reserved_26
27	GND_27	28	Reserved_28
29	PERn1	30	Reserved_30
31	PERp1	32	Reserved_32
33	GND_33	34	Reserved_34
35	PETn1	36	Reserved_36
37	PETp1	38	DEVSLP (I)(0/3.3V)
39	GND_39	40	Reserved_40
41	PERn0/SATA-B+	42	Reserved_42
43	PERp0/SATA-B-	44	Reserved_44
45	GND_45	46	Reserved_46
47	PETn0/SATA-A-	48	Reserved_48
49	PETp0/SATA-A+	50	PERST# (I)(0/3.3V)
51	GND_51	52	CLKREQ# (IO)(0/3.3V)
53	REFCLKN	54	PEWake# (IO)(0/3.3V)
55	REFCLKP	56	Reserved_56
57	GND_57	58	Reserved_58
67	NC32	68	SUSCLK(32kHz) (I)(0/3.3V)
69	PEDET (OC-PCIe)	70	3.3V_70
71	GND_71	72	3.3V_72
73	GND_73	74	3.3V_74
75	GND_75		
GND12		GND13	
76		77	

Key M

51750-0750P-012

I

CON_75P_PH05_SMD_51736_RVS_M

20170718
yanzw
genhuan

PCIE12 RX
follow intel CRB

Difference with armour
SSD interface SATA change to PCIE
If install SATA CARD,R4200,R4201 need install 0.01uF
C0606,C0607 need install 0.01uF

(9) PCIE9_SSD_RX_DN
(9) PCIE9_SSD_RX_DP
(9) PCIE9_SSD_TX_DN_C
(9) PCIE9_SSD_TX_DP_C
(9) PCIE10_SSD_RX_DN
(9) PCIE10_SSD_RX_DP
(9) PCIE10_SSD_TX_DN_C
(9) PCIE10_SSD_TX_DP_C
(9) PCIE11_SSD_RX_DN
(9) PCIE11_SSD_RX_DP
(9) PCIE11_SSD_TX_DN_C
(9) PCIE11_SSD_TX_DP_C
(9) PCIE12_SSD_RX_DP
(9) PCIE12_SSD_RX_DN
(9) PCIE12_SSD_TX_DN_C
(9) PCIE12_SSD_TX_DP_C
(7) PCIE_REFCLK_SSD_DN
(7) PCIE_REFCLK_SSD_DP

R4200 0R R0402_N5% I PCIE12_SSD_RX_DP_R
R4201 0R R0402_N5% I PCIE12_SSD_RX_DN_R

+V3P3A

R10869 100K 5% R0402_N I
R10870 100K 5% R0402_N NI

(8) SSD_PEDET — R10900 0R R0402_N5% NI

Pin69
PICE module spec is N/C
SATA module spec is GND

+V3P3A_SSD

SATA2_DEVSLP (9)

+V3P3A_SSD — R4207 10K 5% R0402_N I — 1/4 Add R4206 PU

SSD_CLK_REQ_N_R
M.2_SSD_PE_WAKE_N

R4206 0R R0402_N5% I
R4205 0R 5% R0402_N NI

PLT_RST_N (7,43,50,74)
SSD_CLK_REQ_N (7)
PCIE_WAKE_PCH_N (7,43)

Pin54
PICE module spec is N/C
SATA module spec is N/C

PM_SUSCLK_SSD — TP9980

Pin68
PICE module spec is N/C
SATA module spec is N/C

NGFF SSD module interface	PCIE	SATA
Reference	R4200,R4201 install 0ohm C0606,C0607 install 0.22uF	R4200,R4201 install 0.01uF C0606,C0607 install 0.01uF
Detect pin	R1050 install 10Kohm R1087 uninstall 100Kohm	R1050 uninstall 10Kohm R1087 install 100Kohm

Default

3/16 Add SSD(PCIE or SATA) BOM option table

Co-lay PCIE12 RX, reserved R4202,R4203
please close to R4200,R4201

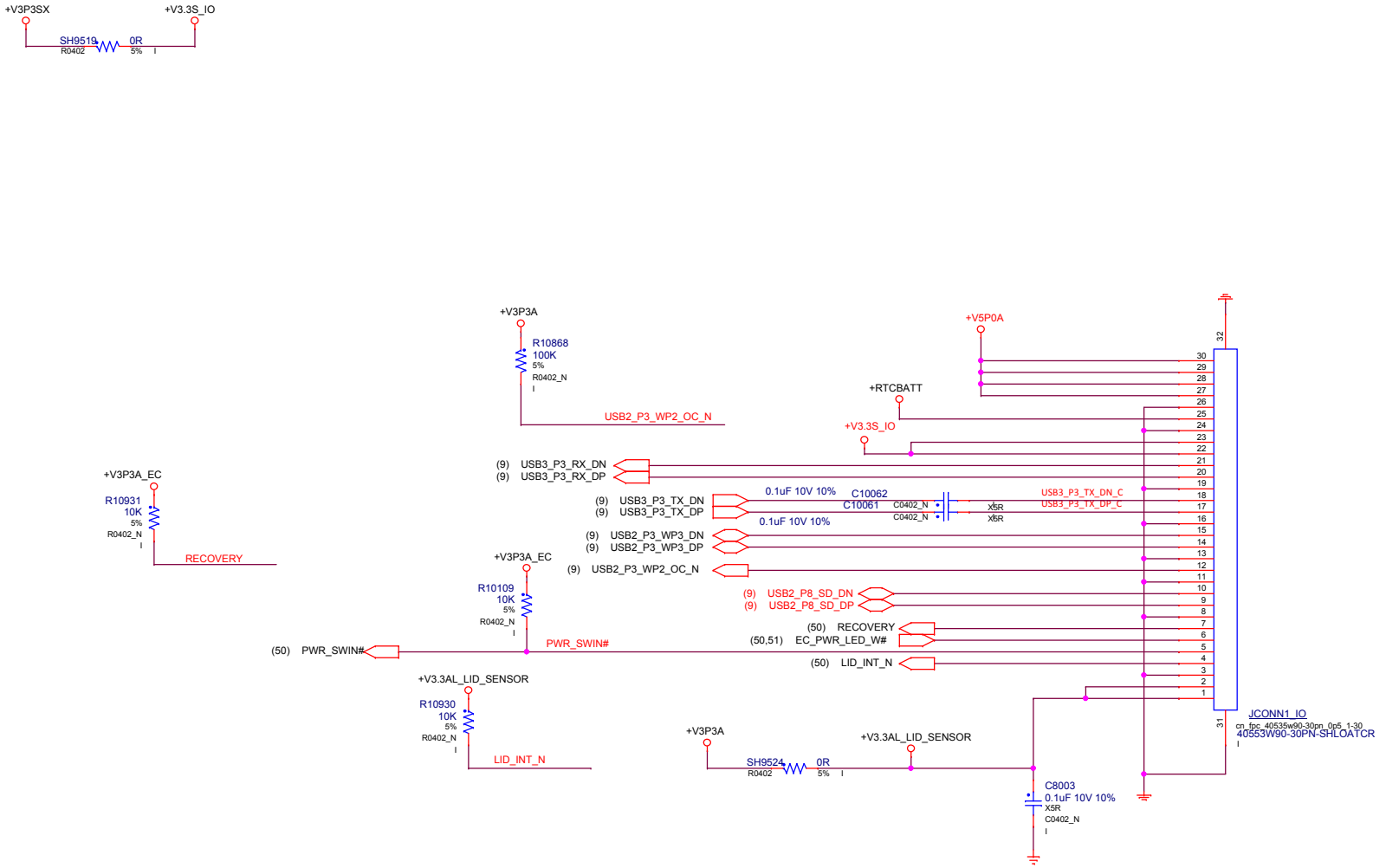
+V3P3SX — +V3P3SX (5,6,7,8,9,10,20,25,27,28,30,35,36,43,46,50,52)

INTERNAL ONLY

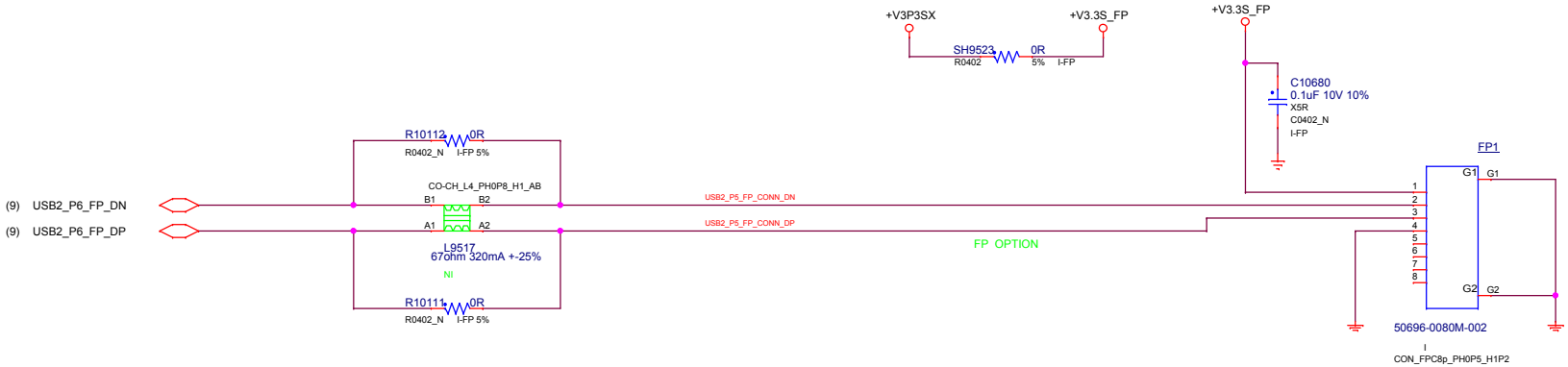
BPAGE DRAWING

sky_y_mrd.+V3P3.26
Wed Jun 03 11:22:52 2015

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: PCIE SSD MODULE	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 26 of 81	



3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: IO CONNECTOR	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 27 of 81	



INTERNAL ONLY

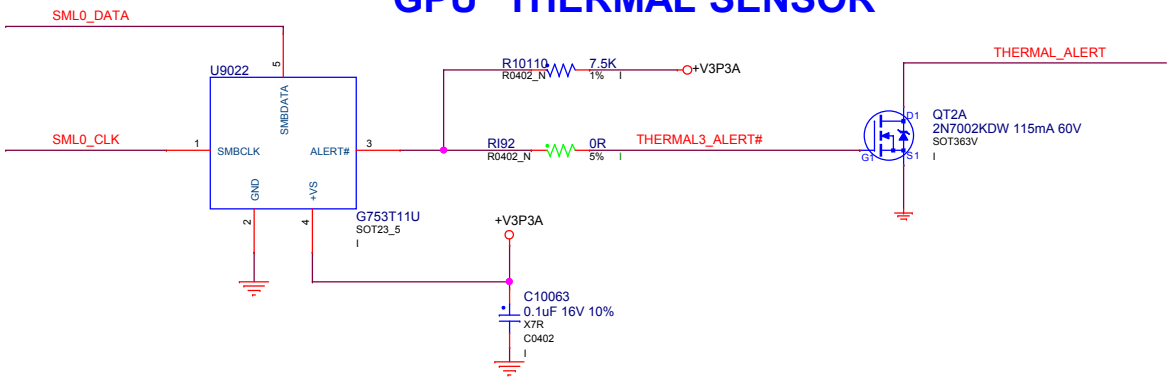
BPAGE DRAWING

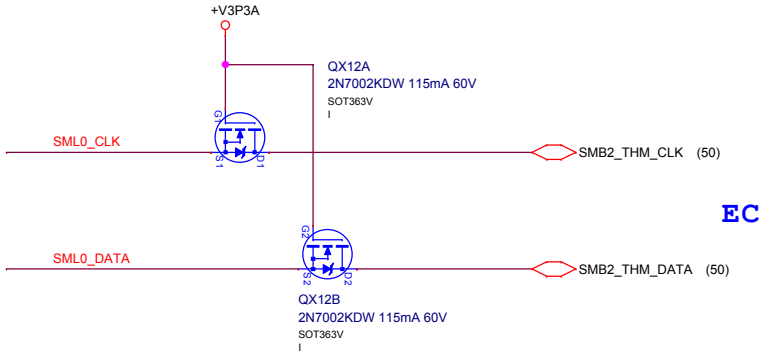
sky_y_mrd.GND

Wed Jun 03 11:22:53 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: FINGER PRINT	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 28 of 81	

GPU THERMAL SENSOR

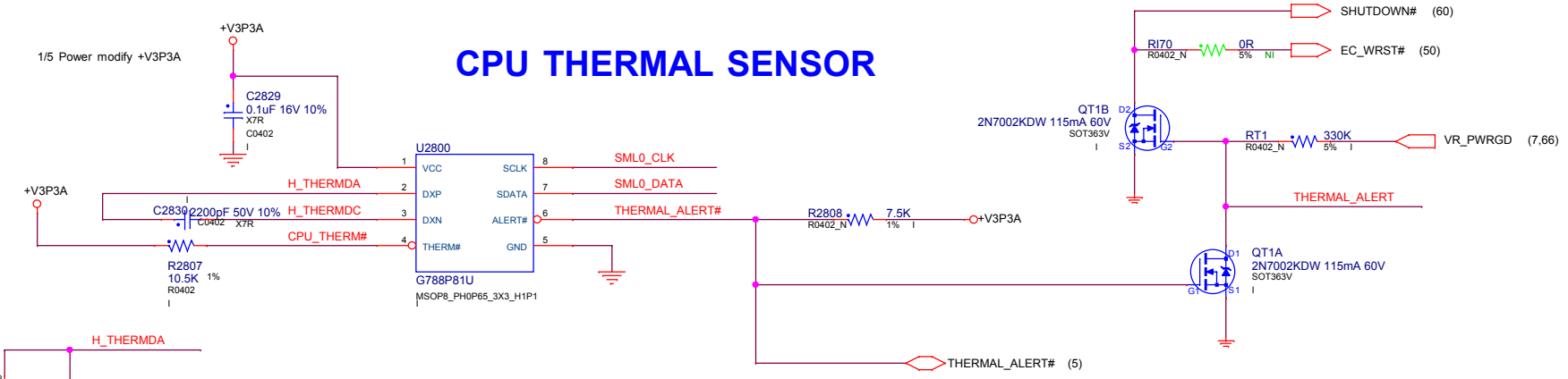




EC

1/4 Add connect to SOC & EC

CPU THERMAL SENSOR



CHARGE THERMAL SENSOR

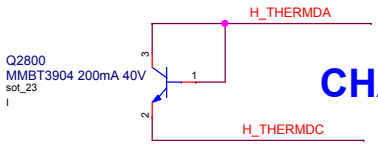
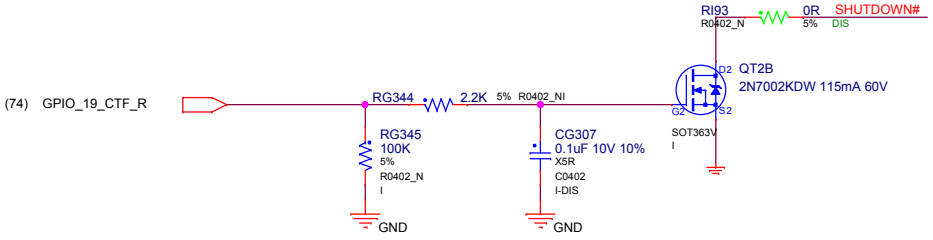


Table 10. Remote temperature $\overline{\text{THERM}}$ limit

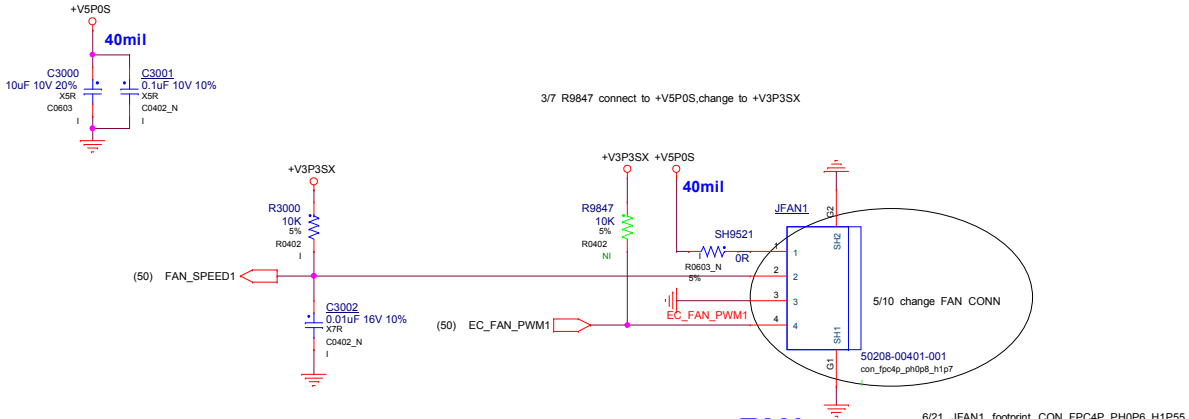
The default value is trapping after power up 100ms by different pull-up resistors of $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ pin:

TEMPERATURE (°C)		$\overline{\text{THERM}}$				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



+V3P3A +V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,35,42,50,51,55,56,60,62,65,66,68,69)

3nod三诺	Project:	330S-14&15	
	Engineer:	Luffy	
Size: B	Title: CPU THERMAL SENSOR		Rev: V01
Date: Tuesday, September 26, 2017	Sheet 29 of 81		



FAN conn

CIS ok

1/11 Update FAN pin define

+V5P0S
+V3P3SX

+V5P0S (10,25,35,36,46)
+V3P3SX (5,6,7,8,9,10,20,25,26,27,28,35,36,43,46,50,52)

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: FAN conn	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 30 of 81	

3nod三诺	Project: 330S-14&15		
	Engineer: Luffy		
Size: E	Title: NA		Rev: V01
Date: Tuesday, September 26, 2017	Sheet 31 of 81		

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.32
Wed Jun 03 11:22:55 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 32 of 81	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V1P0.33
Wed Jun 03 11:22:55 2015

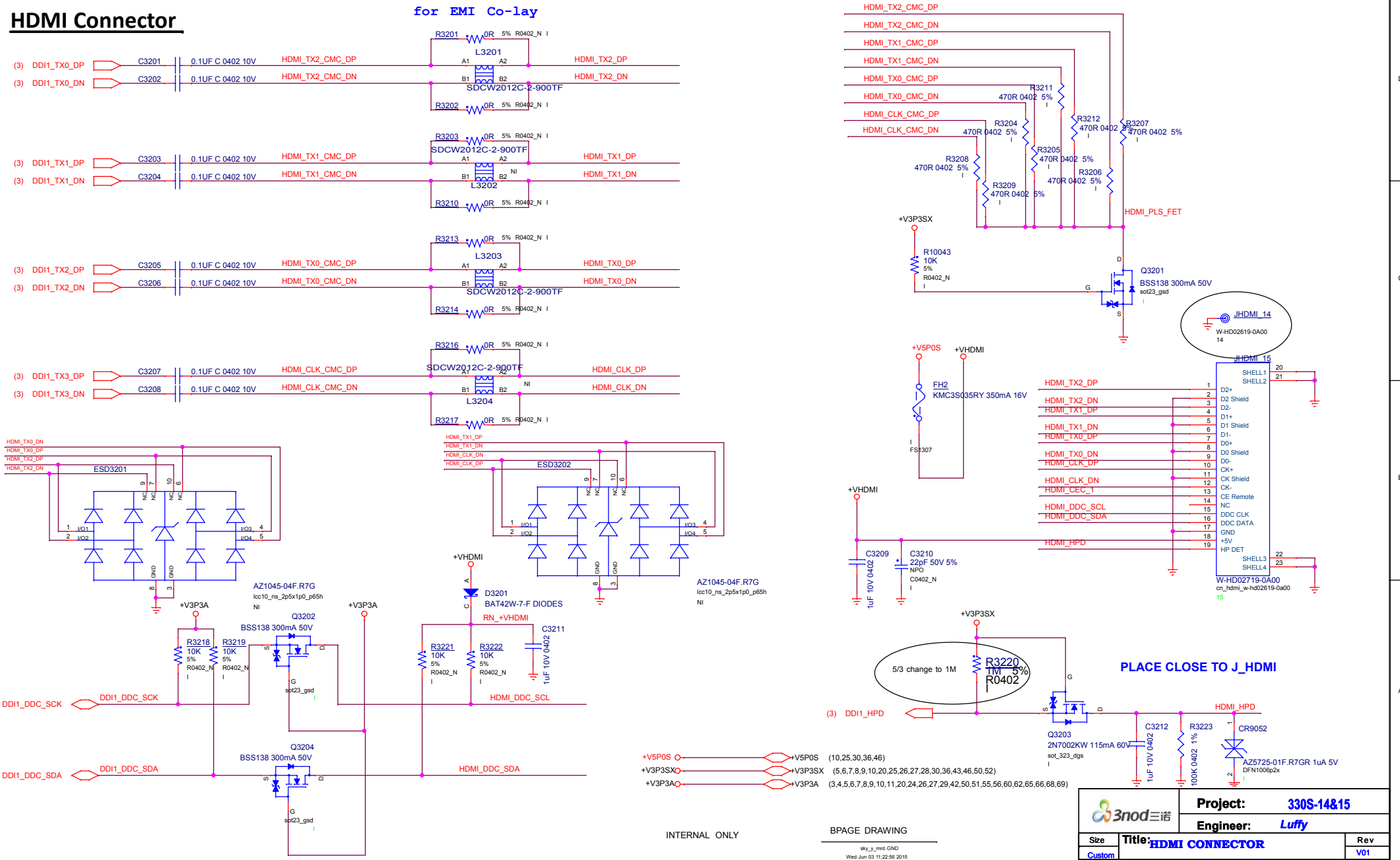
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 33 of 81	

Wed Jun 03 11:22:56 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 34 of 81	

HDMI Connector

for EMI Co-lay



EDP DISPLAY 1920X1200 (12.2INCH)

3/22 FB8200 0603 Bead change to JP8200 JUMP_43X79

BL_PWR	LED Power Supply,6V-8.4V

Change the SH8200 SH8201 0402
shunt to resistor

10	Backlight power consumption	3.94W
11	Panel power consumption	1.03W

LCD_VCC	Power Supply,3.3V(typ.)

BL_PWM_DIM	LED PWM signal input. H=3.3V
BL_ENABLE	LED enable input. H=3.3V

Difference with armour
U8201 WS4601E-5/TR
change to APL3512ABI-TRG

Difference with armour
Add R8221 change to install

5/11 change CAPs

2/22 change CONN

CIS ok

3/23 Add

6.5V x [80.6/(220+80.6)] = 1.743V VGS= -4.5V
1.743V - 6.5V = -4.757V

Project:	330S-14&15		
Engineer:	Luffy		
Size: Custom	Title: DISPLAY		Rev: V01
Date: Tuesday, September 26, 2017	Sheet 36 of 81		

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:32 2016

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: USB2.0	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 37 of 81	

Sensors

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: LID	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 38 of 81	

3nod三诺	Project: 330S-14&15	
	Engineer: *Luffy*	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 39 of 81	

Wed Jun 03 11:22:59 2015

3nod三诺	Project: 330S-14&15		
	Engineer: Luffy		
Size: Custom	Title: NA		Rev: V01
Date: Tuesday, September 26, 2017	Sheet 40 of 81		

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.41
Wed Jun 03 11:22:59 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 41 of 81	

USB3.0

+V5P0A
+V3P3A
+V5P0A (10,11,24,27,50,54,61,62,63,65,66,67,68,69,70,72)
+V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)

+V5CP — R10060 0R R0805_N 5% I — +V5CP_R

+V5CP_R

4/20 change rating
CC452 22uF 6.3V 20% X5R C0603_N I
C3900 0.1uF 10V 10% X5R C0402_N I

R3902 20K 5% R0402_N I

5/23 change to 110K.
R3903 110K 1% R0402 I

+V3P3A
R3904 100K 5% R0402_N I
USB2_P1_WP0_OC_N (9)

U3900
+V5P0A_USB_WP2
PWPd, ILIM_HI, ILIM_LO, GND, FAULT
IN, DM_OUT, DP_OUT, ILIM_SEL, EN
OUT, DM_IN, DP_IN, STATE#
CTL1, CTL2, CTL3
TPS2546RTER I

(9) USB2_P1_WP1_DN
(9) USB2_P1_WP1_DP
USB2_P1_DN
USB2_P1_DP

+V3.3AL 4/7 change from +V3P3A to +V3.3AL
R3958 100K 5% R0402_N I
USB_STATUS# — USB_STATUS# (50)

TPS2546_CTL3 (50)
TPS2546_CTL2 (50)
TPS2546_CTL1 (50)

D+/D- ESD

USB2_P1_WP1_DP_CONN
USB2_P1_WP1_DN_CONN

CR9012 AZ5725-01F.R7GR 1uA 5V DFN1006p2x NI
CR9013 AZ5725-01F.R7GR 1uA 5V DFN1006p2x NI

+V3.3AL
R3900 100K 5% R0402 I
(50) EC_ACDET — R3961 0R R0402_N 5% I
R3901 0R R0402_N 5% NI

EC_USB_PWR_EN_R
R3960 0R R0402_N 5% I
(50) EC_USB_PWR_EN

+V5P0A_USB_WP2

5/22 change to 100uF
C10022 100uF 6.3V +/-20% SMD3.5X2.8mm
C9006 470pF 50V 5% COG C0402_N I
C9007 4.7uF 10V 10% X5R C0603_N I
CR9054 AZ5725-01F.R7GR 1uA 5V DFN1006p2x I

5/22 add ESD
CR9081 0R 5% NI R0603_N

JUSB3-15
GND3, GND4, GND1, GND2
VBUS, D-, D+, GND, STDA_SSRX-, STDA_SSRX+, GND_DRAIN, STDA_SSTX-, STDA_SSTX+
W-US09809-0A00
cn_usb-3_w-us09809-0a00
15

JUSB3-14
W-US09709-0A00
14

USB3_P1_TX_DP_CONN
USB3_P1_TX_DN_CONN
USB3_P1_RX_DN_CONN
USB3_P1_RX_DP_CONN

CR9006
NC, I/O1, I/O2, I/O3, I/O4, GND
AZ1045-04F.R7G
lcc10_ns_2p5x1p0_p65h
NI

R9007 0R R0402_N I 5%
L9003 A1 A2 NI B1 B2
67ohm 320mA +-25%
CO-CH_L4_PH0P8_H1_AB
R9006 0R R0402_N I 5%

R9853 0R R0402_N I 5%
(9) USB3_P1_RX_DN
(9) USB3_P1_RX_DP
L9508 NI
R9852 0R R0402_N I 5%

R9012 0R R0402_N I 5%
(9) USB3_P1_TX_DN — C1271 0.1uF 10V 10% X5R C0402_N
(9) USB3_P1_TX_DP — C1270 0.1uF 10V 10% X5R C0402_N
L9002 NI
R9011 0R R0402_N I 5%

+V3.3AL (11,50,51,58,60)
+V5CP (10,60)
+V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)

CIS OK - 20170717 YD

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: USB3.0 CONN	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 42 of 81	

WIFI & BT Module

+V3P3SX — SH4302 — +V3P3SX_CWS

0R
R0603_N
5%

2/16 change CONN

THIS DESIGN SUPPORTS STONE PEAK ONLY

CIS ok

+V3P3SX_CWS

C4320 4.7uF 6.3V 10% X5R C0603_N
C4321 4.7uF 6.3V 10% X5R C0603_N
C4322 0.1uF 10V 10% X5R C0402_N
C4323 0.1uF 10V 10% X5R C0402_N

C6001 & C6003 FOR PIN 72 &73
C6002 & C6000 FOR PIN 4 & 5

JWLAN1

SLOT A KEY E

1	GND_1	3.3V_2	2
3	USB_D+	3.3V_4	4
5	USB_D-	LED1_N	6
7	GND_7	PCM_CLK/I2S_SCK	8
9	SDIO_CLK	PCM_SYNC/I2S_WS	10
11	SDIO_CMD	PCM_IN/I2S_SD_IN	12
13	SDIO_DATA0	PCM_OUT/I2S_SD_OUT	14
15	SDIO_DATA1	LED2_N	16
17	SDIO_DATA2	GND_18	18
19	SDIO_DATA3	UART_WAKE_N	20
21	SDIO_WAKE_N	UART_RX	22
23	SDIO_RESET_N		

KEY E
PLATFORM PIN OUT

33	GND_33	UART_TX	32
35	PETP0	UART_CTS	34
37	PETN0	UART_RTS	36
39	GND_39	RESERVED_38	38
41	PERP0	RESERVED_40	40
43	PERN0	RESERVED_42	42
45	GND_45	COEX3	44
47	REFCLKP0	COEX2	46
49	REFCLKN0	COEX1	48
51	GND_51	SSCLK	50
53	CLKREQ0_N	PERST0_N	52
55	PEWAKE0_N	RESERVED_W_DISABLE2_N	54
57	GND_57	W_DISABLE1_N	56
59	RESERVED_2ND_PETP1	I2C_DATA	58
61	RESERVED_2ND_PETN1	I2C_CLK	60
63	GND_63	ALERT	62
65	RESERVED_2ND_PERP1	RESERVED_64	64
67	RESERVED_2ND_PERN1	UIM_SWP/PERST1_N	66
69	GND_69	UIM_PWR_SNK/CLREQ1_N	68
71	RESERVED/REFCLKN1	UIM_PWR_SRC/GPIO1/PEWAKE1_N	70
73	RESERVED/REFCLKP1	3.3V_72	72
75	GND_75	3.3V_74	74
	GND76	GND77	
	76	77	

51750-0750P-005
TBD

CIS OK - 20170717 YD

20170718
yanzw
genhuan

(9) USB2_P4_BT_DP
(9) USB2_P4_BT_DN

TP9992
TP9993
WIFI/BT_SLOT_TX — TP9976
WIFI/BT_SLOT_RX — TP9977

C4318 0.1uF 10V 10%
C4319 0.1uF 10V 10%
C0402_N X5R

(9) PCIE_WLAN_LN0_TX_SOC_DP
(9) PCIE_WLAN_LN0_TX_SOC_DN
(9) PCIE_WLAN_LN0_RX_SOC_DP
(9) PCIE_WLAN_LN0_RX_SOC_DN
(7) PCIE_REFCLK_WLAN_DP_R
(7) PCIE_REFCLK_WLAN_DN_R
R9890 0R R0402_N5%I PCIE_REFCLK_WLAN_DP
R9889 0R R0402_N5%I PCIE_REFCLK_WLAN_DN

(7) WLAN_CLK_REQ_N
(7,26) PCIE_WAKE_PCH_N

(5,50) LPC_FRAME_N
(5,50) LPC_AD3
(5,50) LPC_AD2
(5,50) LPC_AD1
(5,50) LPC_AD0

(5) LPC_CLK_PRT80 — R4319 0R R0402_N I 5%

R4320 0R R0402_N 5% I
SUS_CLK_R — SUS_CLK (7,50)
WLAN_RST_R
BT_RF_KILL_N (3)
WIFI_DISABLE_N (6)
SM_BAT_DATA_DEBUG — TP10009
SM_BAT_CLK_DEBUG — TP10010

4/21 Add SM_BAT_DATA connect to JWLAN1.58,
Add SM_BAT_CLK connect to JWLAN1.60,
Debug card need.

4/21 Add R4325,R4326 0ohm for Debug card

6/27 R4325,R4326 change to NI,
because WLAN card "Intel 2x2AC 8260" I2C is 1.8V,
mother board I2C is 3.3V

WLAN PCIE AC CAPS

+V3P3SX_CWS
R4321 10K 5% R0402_N I
WLAN_CLK_REQ_N

Difference with armour
Reserve PLT_RST_N to reset pin and install

WLAN_RST_R — R4323 0R R0402_N 5% — PLT_RST_N (7,26,50,74)
R4324 0R R0402_N NI 5% — WLAN_RST (8)

+V3P3SX — +V3P3SX (5,6,7,8,9,10,20,25,26,27,28,30,35,36,46,50,52)

INTERNAL ONLY

BPAGE DRAWING
sky_y_mrd.+V3P3.43
Wed Jun 03 11:23:00 2015

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: WLAN WIFI BT MODULE	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 43 of 81	

Project:	330S-14&15
Engineer:	Luffy
Size: Custom	Title: NA
Rev:	V01
Date:	Tuesday, September 26, 2017
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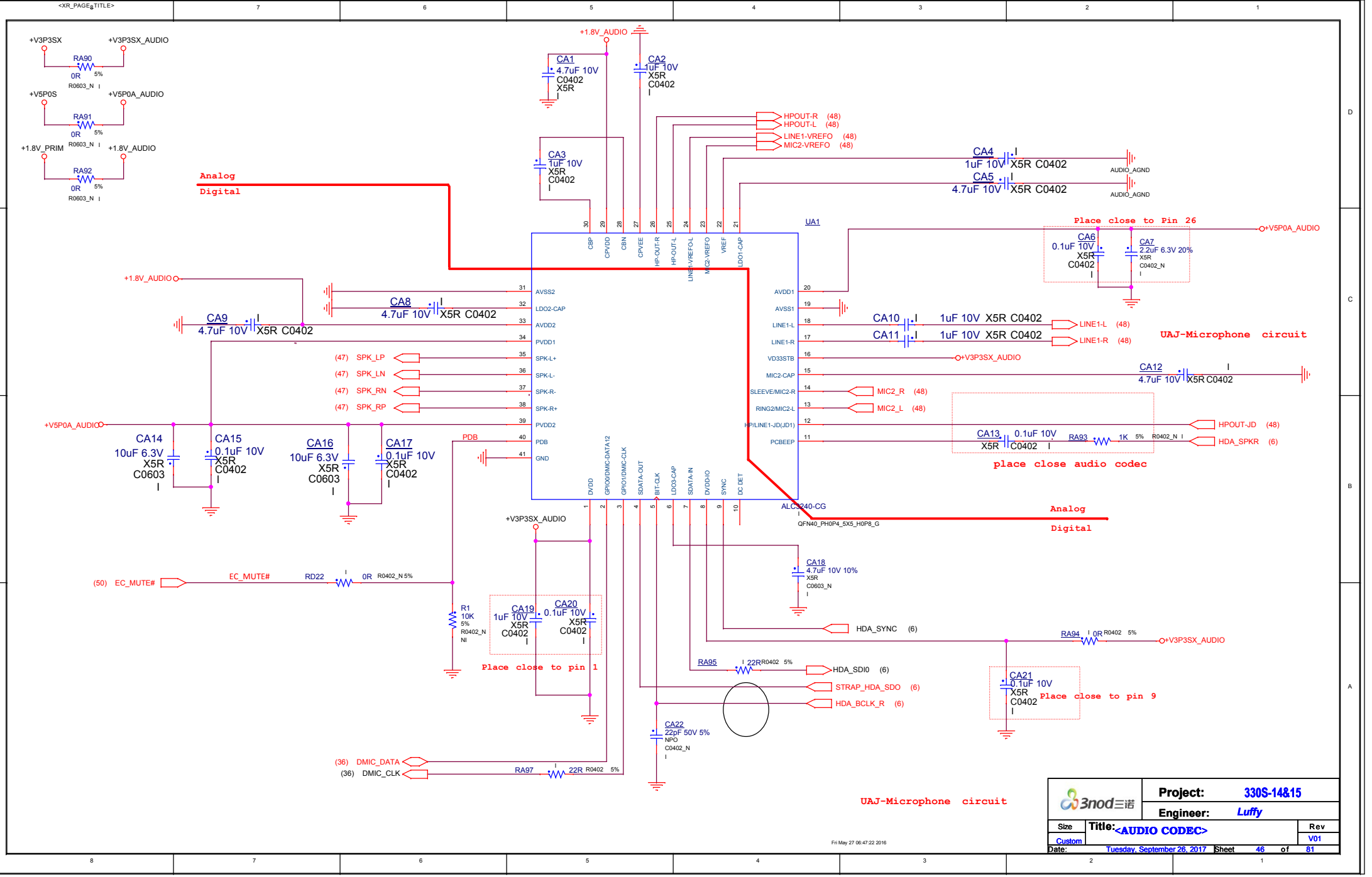
INTERNAL ONLY

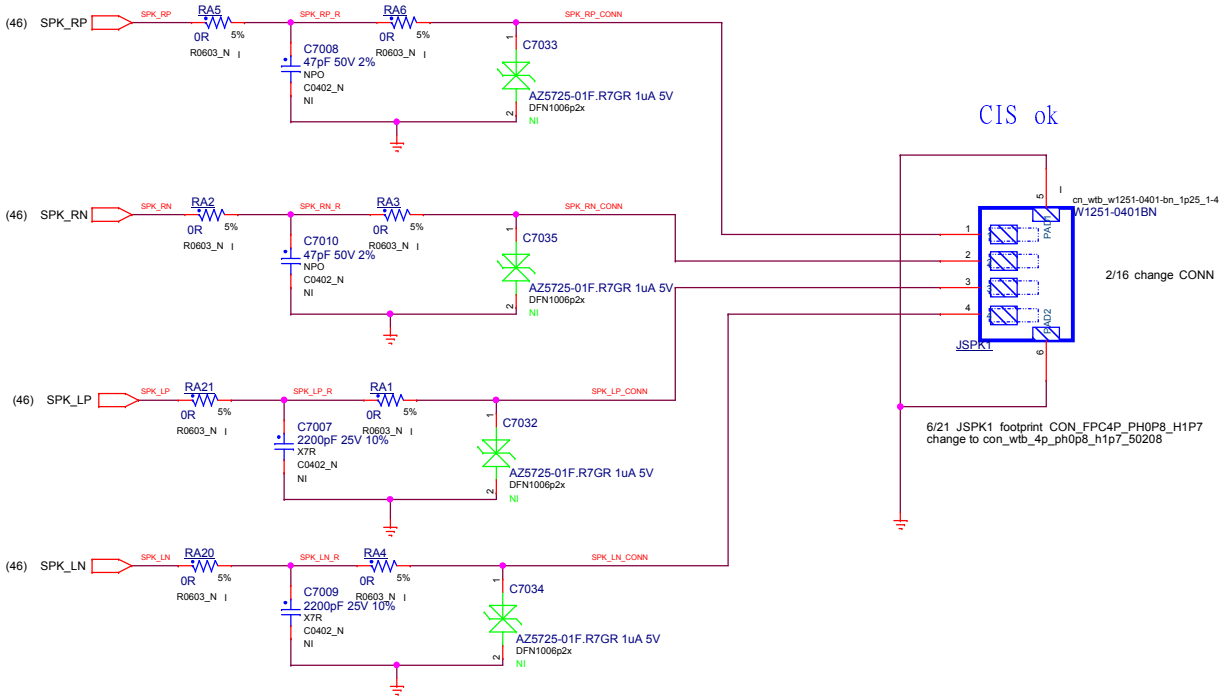
BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:23:01 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 45 of 81	


+V3P3SX
+V3P3SX_AUDIO
RA90
0R
+V5P0S
+V5P0A_AUDIO
RA91
0R
+1.8V_PRIM
+1.8V_AUDIO
RA92
0R
Analog
Digital
+1.8V_AUDIO
CA1
4.7uF 10V
C0402
X5R
CA2
1uF 10V
X5R
C0402
CA3
1uF 10V
X5R
C0402
HPOUT-R (48)
HPOUT-L (48)
LINE1-VREFO (48)
MIC2-VREFO (48)
CA4
1uF 10V X5R C0402
CA5
4.7uF 10V X5R C0402
AUDIO_AGND
AUDIO_AGND
UA1
CBP
CPVDD
CBN
CPVEE
HP-OUT-R
HP-OUT-L
LINE1-VREFO-L
MIC2-VREFO
VREF
LDO1-CAP
Place close to Pin 26
+V5P0A_AUDIO
CA6
0.1uF 10V
X5R
C0402
CA7
2.2uF 6.3V 20%
X5R
C0402_N
+1.8V_AUDIO
CA8
4.7uF 10V X5R C0402
CA9
4.7uF 10V X5R C0402
AVSS2
LDO2-CAP
AVDD2
PVDD1
(47) SPK_LP
(47) SPK_LN
(47) SPK_RN
(47) SPK_RP
SPK-L+
SPK-L-
SPK-R-
SPK-R+
PVDD2
PDB
GND
AVDD1
AVSS1
LINE1-L
LINE1-R
VD33STB
MIC2-CAP
SLEEVE/MIC2-R
RING2/MIC2-L
HP/LINE1-JD(JD1)
PCBEEP
CA10
1uF 10V X5R C0402
CA11
1uF 10V X5R C0402
LINE1-L (48)
LINE1-R (48)
+V3P3SX_AUDIO
CA12
4.7uF 10V X5R C0402
MIC2_R (48)
MIC2_L (48)
UAJ-Microphone circuit
+V5P0A_AUDIO
CA14
10uF 6.3V
X5R
C0603
CA15
0.1uF 10V
X5R
C0402
CA16
10uF 6.3V
X5R
C0603
CA17
0.1uF 10V
X5R
C0402
PDB
CA13
0.1uF 10V
X5R
C0402
RA93
1K
HPOUT-JD (48)
HDA_SPKR (6)
place close audio codec
DVDD
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
SDATA-OUT
BIT-CLK
LDO3-CAP
SDATA-IN
DVDD-IO
SYNC
DC DET
ALC3240-CG
QFN40_PH0P4_5X5_H0P8_G
Analog
Digital
+V3P3SX_AUDIO
CA18
4.7uF 10V 10%
X5R
C0603_N
(50) EC_MUTE#
EC_MUTE#
RD22
0R
HDA_SYNC (6)
RA94
0R
+V3P3SX_AUDIO
R1
10K
5%
R0402_N
NI
CA19
1uF 10V
X5R
C0402
CA20
0.1uF 10V
X5R
C0402
Place close to pin 1
RA95
22R
HDA_SDI0 (6)
STRAP_HDA_SDO (6)
HDA_BCLK_R (6)
CA21
0.1uF 10V
X5R
C0402
Place close to pin 9
CA22
22pF 50V 5%
NPO
C0402_N
(36) DMIC_DATA
(36) DMIC_CLK
RA97
22R
UAJ-Microphone circuit
Fri May 27 06:47:22 2016
3nod三诺
Project: 330S-14&15
Engineer: Luffy
Size
Custom
Title: <AUDIO CODEC>
Rev
V01
Date: Tuesday, September 26, 2017
Sheet 46 of 81

Speaker



CIS ok

2/16 change CONN

6/21 JSPK1 footprint CON_FPC4P_PH0P8_H1P7
change to con_wtb_4p_ph0p8_h1p7_50208

INTERNAL ONLY

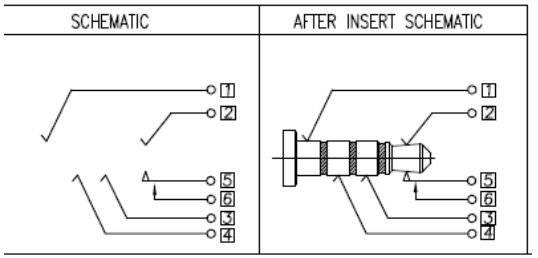
BPAGE DRAWING

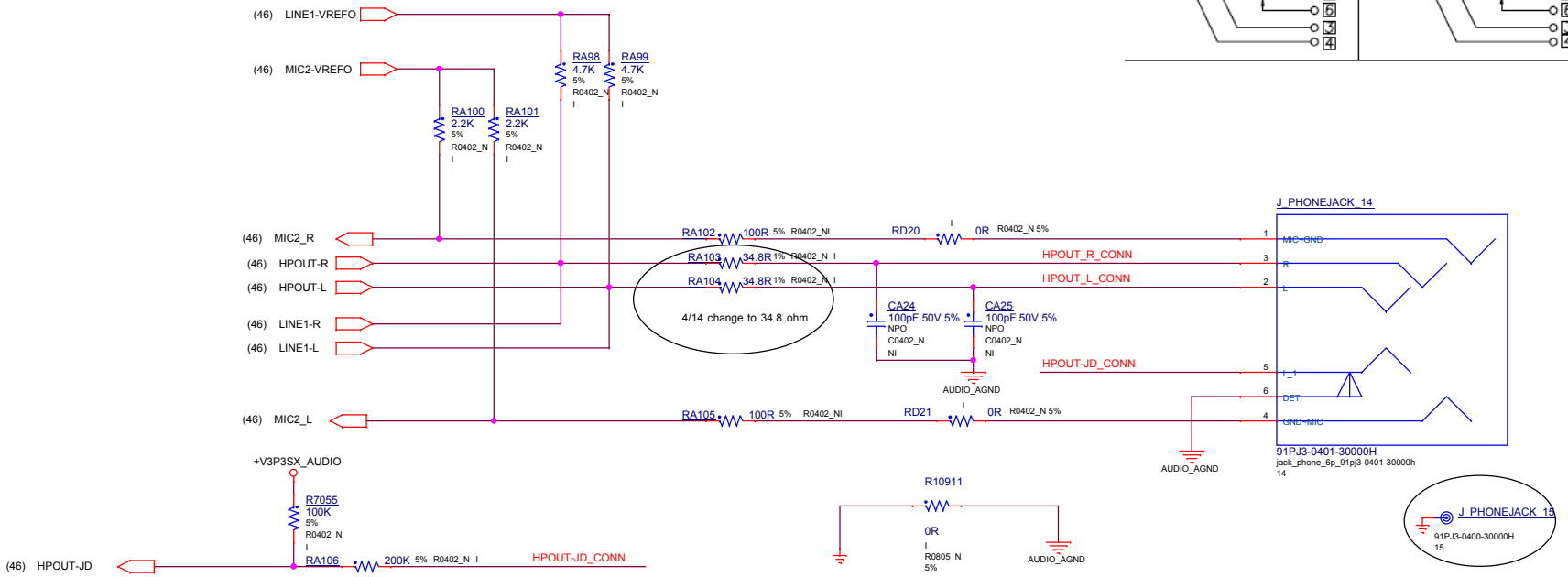
sky_y_mrd.GND
Wed Jun 03 11:23:02 2015

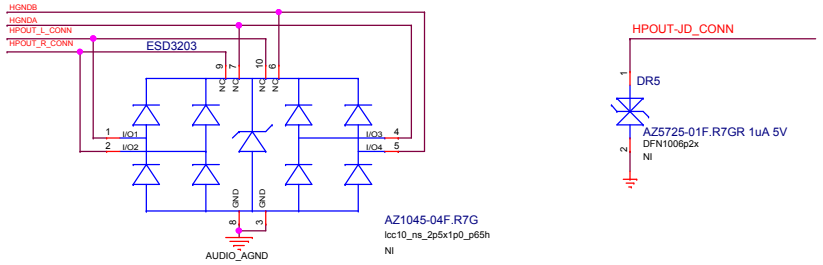
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: Speaker	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 47 of 81	

HEADSET JACK (Supports CTIA and OMTP headsets)

Important:
To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.







+V3P3SX_AUDIO +V3P3SX_AUDIO (46)

INTERNAL ONLY

BPAGE DRAWING

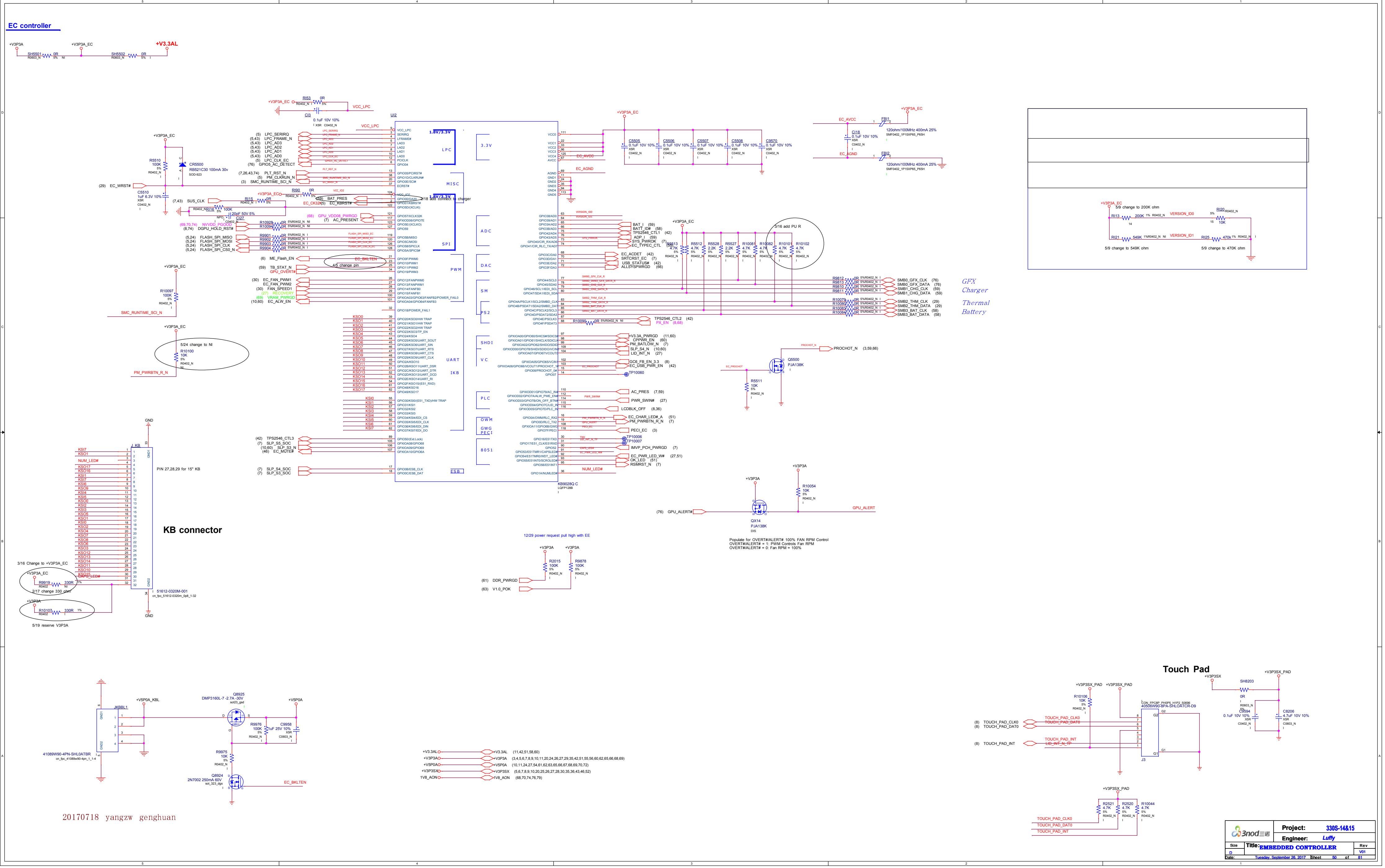
apl_ff.8A
Fri May 27 06:47:24 2016

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: <AUDIO_HEADSET>	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 48 of 81	

BPAGE DRAWING

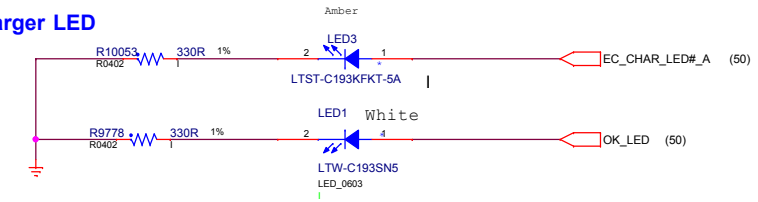
sky_y_mrd.+VCHG.49
Wed Jun 03 11:23:03 2015

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 49 of 81	

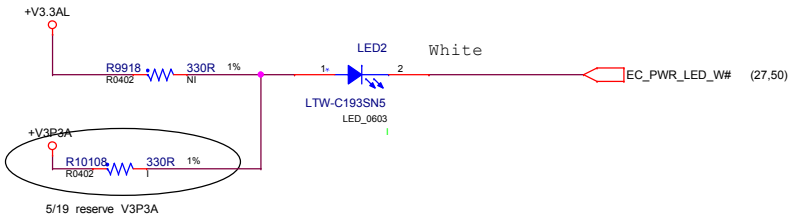


EC controller
+V3P3A
+V3P3A_EC
+V3.3AL
KB9028Q C
LPC
MISC
SPI
ADC
DAC
PWM
UART
IKB
SHDI
PLC
PS2
8051
ESB
VCC_LPC
EC_AVCC
EC_AGND
GFX
Charger
Thermal
Battery
5/9 change to 200K ohm
5/9 change to 549K ohm
5/9 change to 470K ohm
VERSION_ID0
VERSION_ID1
3/16 add PU R
4/5 change pin
5/24 change to NI
PIN 27,28,29 for 15" KB
KB connector
3/16 Change to +V3P3A_EC
2/17 change 330 ohm
5/19 reserve V3P3A
12/29 power request pull high with EE
Populate for OVERT#/ALERT# 100% FAN RPM Control
OVERT#/ALERT# = 1: PWM Controls Fan RPM
OVERT#/ALERT# = 0: Fan RPM = 100%
Touch Pad
EC_BKLTEN
PROCHOT_N
GPU_ALERT
TOUCH_PAD_CLK0
TOUCH_PAD_DAT0
TOUCH_PAD_INT
20170718 yangzw genghuan
3nod
Project: 330S-14&15
Engineer: Luffy
Title: EMBEDDED CONTROLLER
Size D
Rev V01
Date: Tuesday, September 26, 2017
Sheet 50 of 81

Charger LED

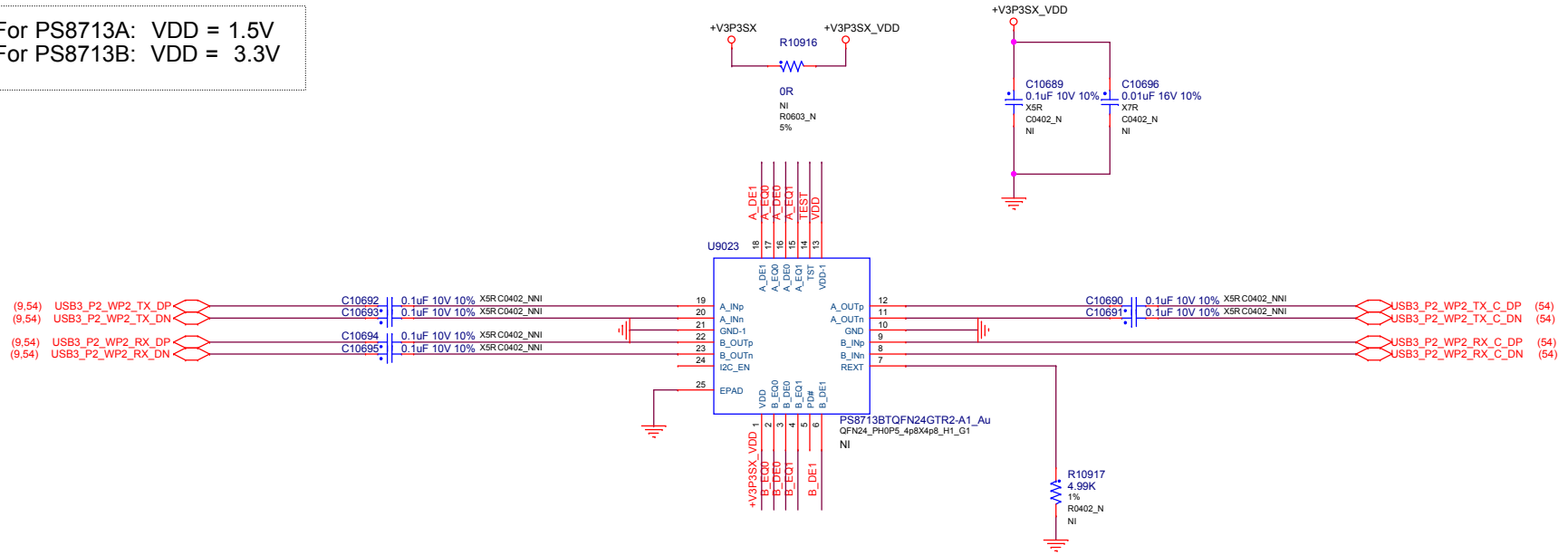


SYS LED



3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: BUTTON & LED	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 51 of 81	

For PS8713A: VDD = 1.5V
For PS8713B: VDD = 3.3V



A_EQ0
A_EQ1
R10923 4.7K 5% R0402_N NI
R10922 4.7K 5% R0402_N NI
+V3P3SX_VDD

Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~150KΩ
[A_EQ1, A_EQ0] ==
LL: program EQ for channel loss up to 9.5dB(default)
LH: program EQ for channel loss up to 13dB
HL: program EQ for channel loss up to 4.5dB
HH: program EQ for channel loss up to 7.5dB

A_DE0
A_DE1
R10918 4.7K 5% R0402_N NI
R10919 4.7K 5% R0402_N NI
+V3P3SX_VDD

Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~150KΩ
[A_DE1, A_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

B_EQ0
B_EQ1
R10925 4.7K 5% R0402_N NI
R10924 4.7K 5% R0402_N NI
+V3P3SX_VDD

Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~150KΩ
[B_EQ1, B_EQ0] ==
LL: program EQ for channel loss up to 9.5dB(default)
LH: program EQ for channel loss up to 13dB
HL: program EQ for channel loss up to 4.5dB
HH: program EQ for channel loss up to 7.5dB

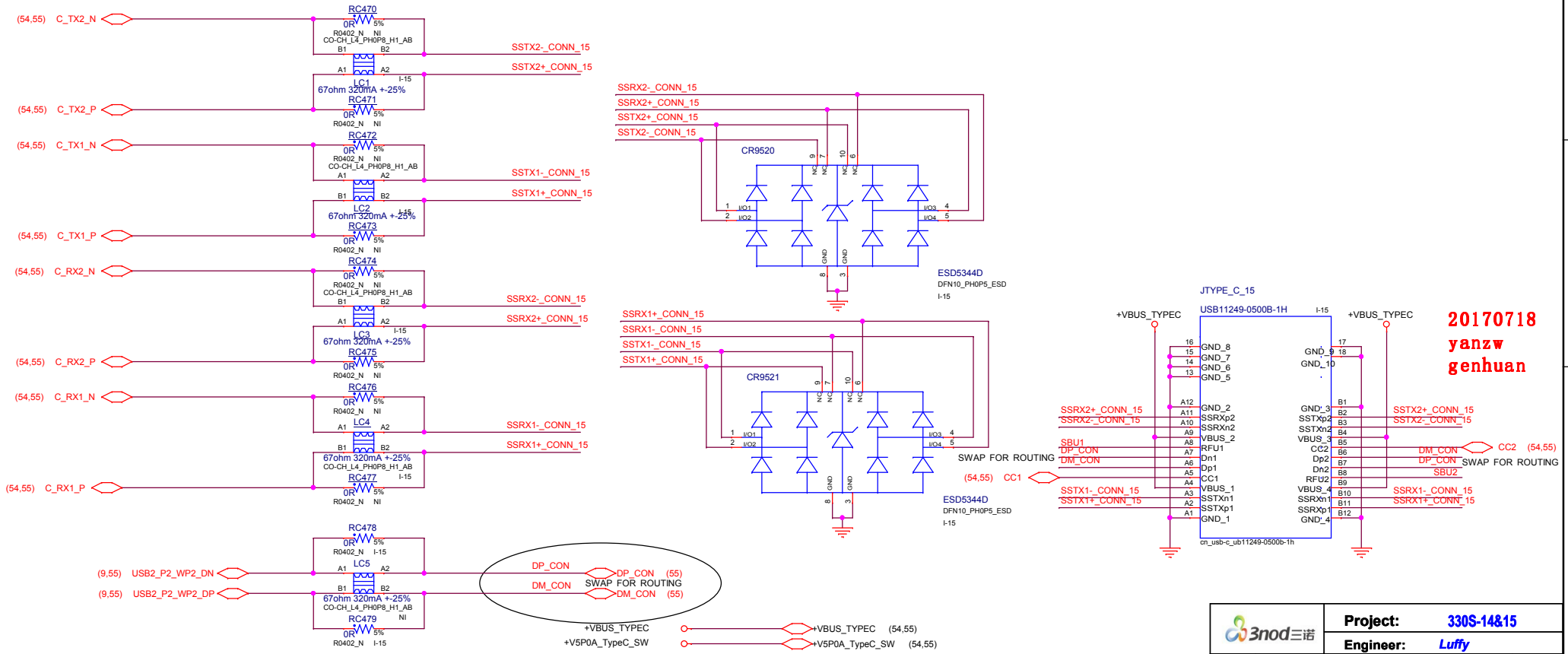
B_DE0
B_DE1
R10921 4.7K 5% R0402_N NI
R10920 4.7K 5% R0402_N NI
+V3P3SX_VDD

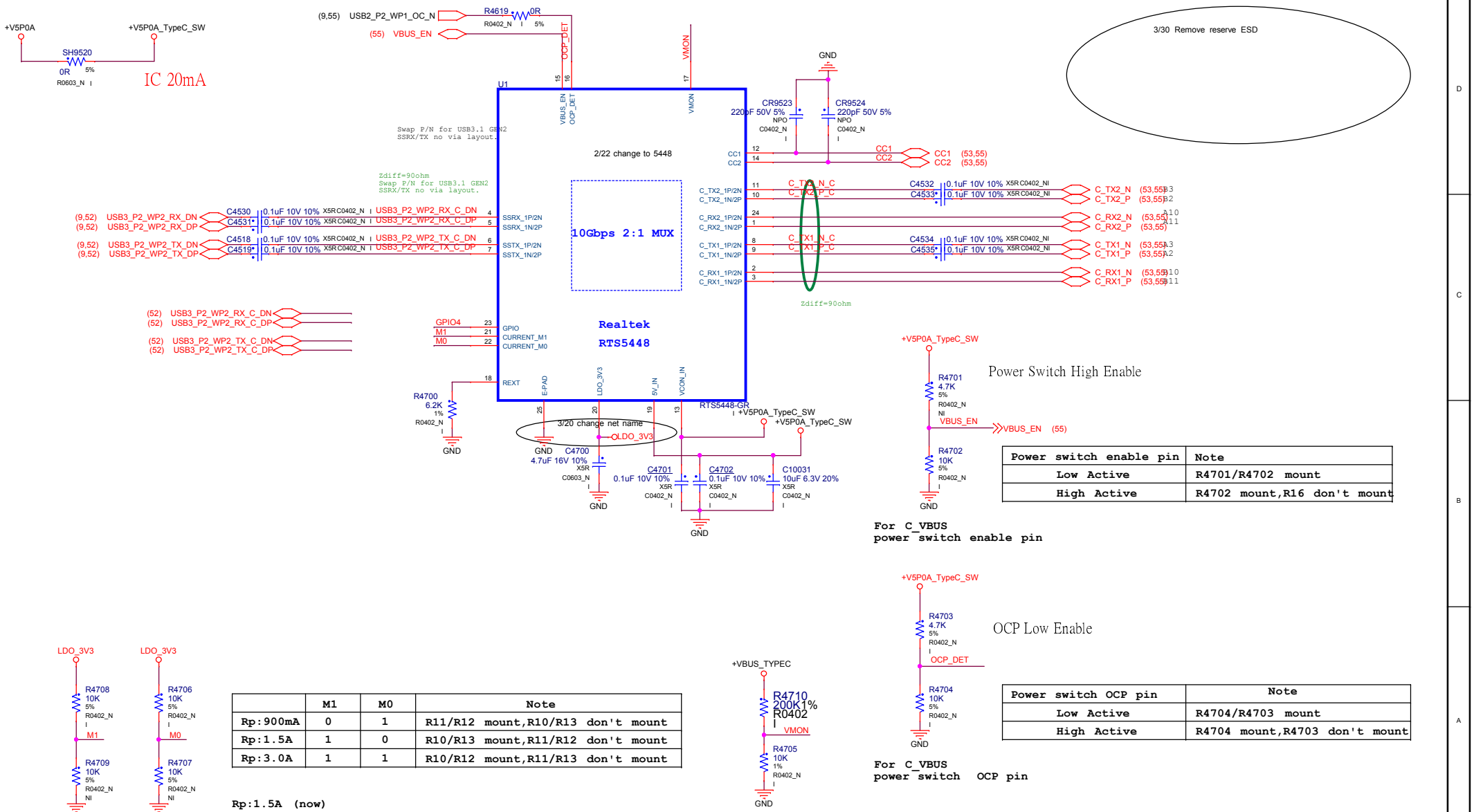
Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~150KΩ
[B_DE1, B_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

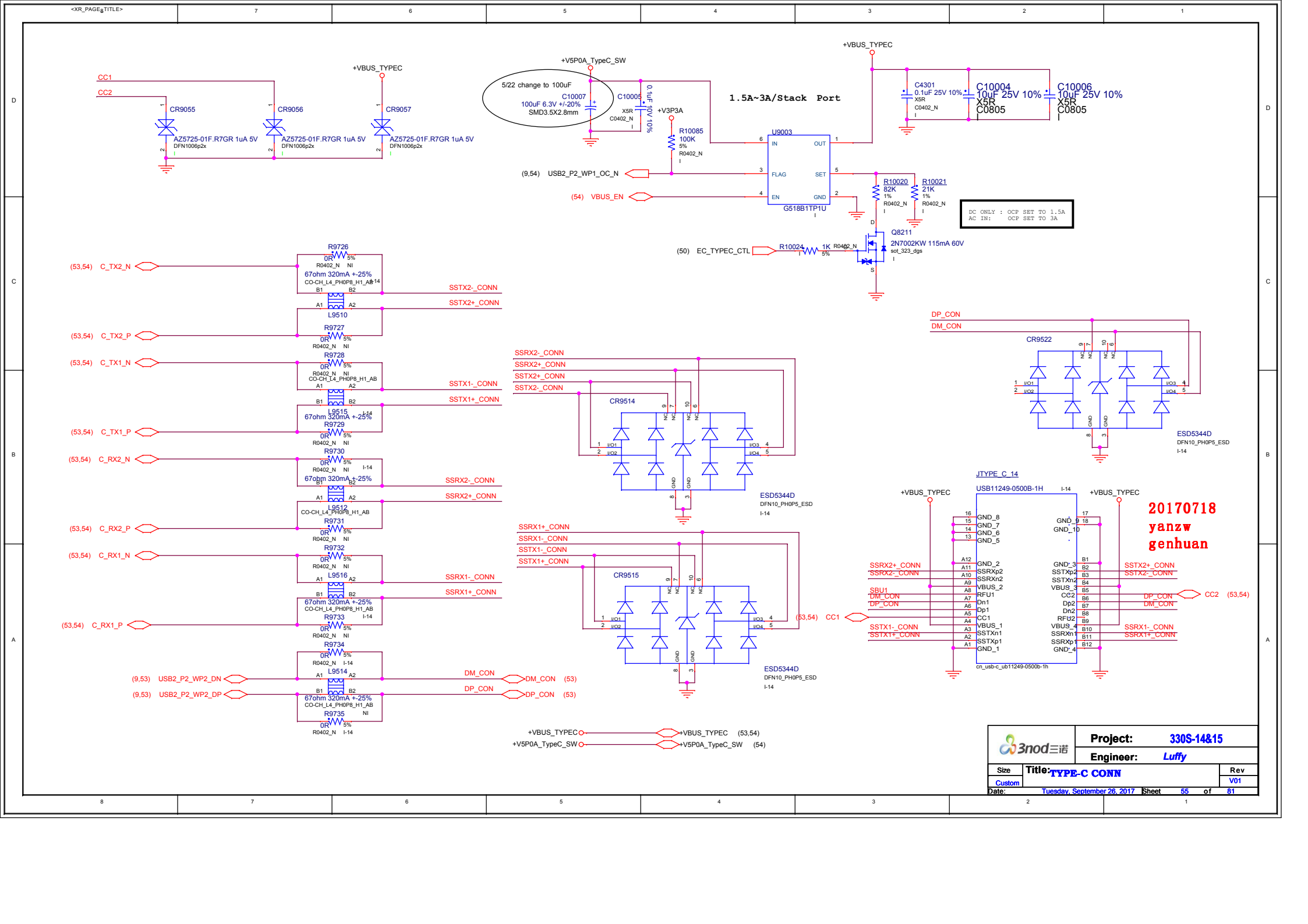
TEST
R10927 4.7K 5% R0402_N NI
+V3P3SX_VDD

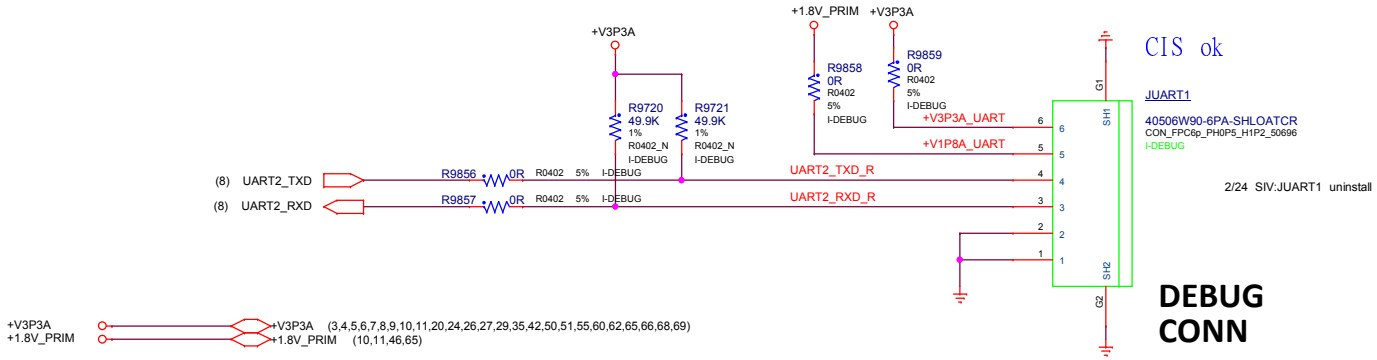
LFPS swing adjust.
3.3V tolerant. Internally pulled down at ~150KΩ .
TEST ==
L: Normal LFPS swing (default)
H: Turn down LFPS swing

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: TYPE-C Switch	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 52 of 81	

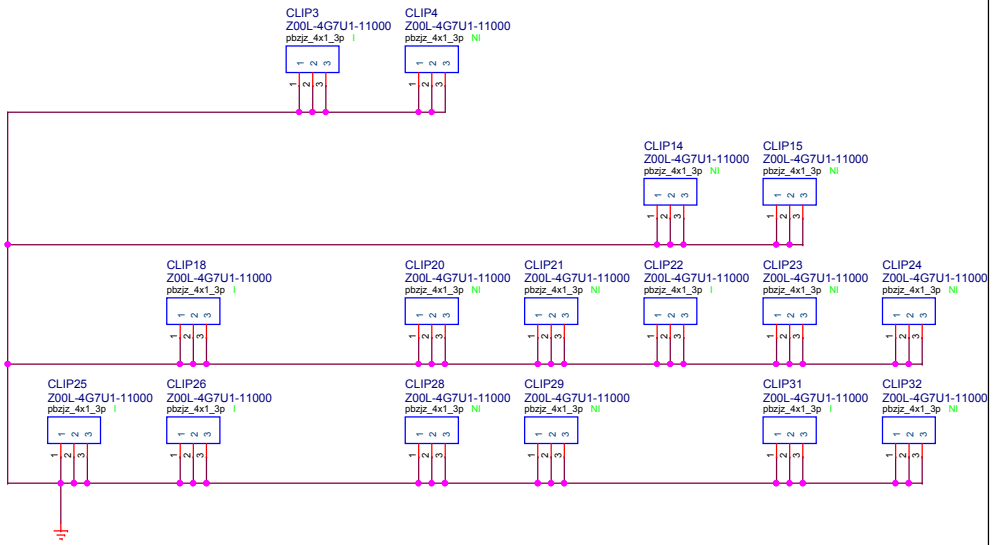

(54,55) C_TX2_N
RC470
0R 5%
R0402_N NI
CO-CH_L4_PH0P8_H1_AB
B1 B2
SSTX2-_CONN_15
A1 A2
SSTX2+_CONN_15
LC1
67ohm 320mA +-25%
I-15
(54,55) C_TX2_P
RC471
0R 5%
R0402_N NI
(54,55) C_TX1_N
RC472
0R 5%
R0402_N NI
CO-CH_L4_PH0P8_H1_AB
SSTX1-_CONN_15
SSTX1+_CONN_15
LC2
67ohm 320mA +-25%
I-15
(54,55) C_TX1_P
RC473
0R 5%
R0402_N NI
(54,55) C_RX2_N
RC474
0R 5%
R0402_N NI
CO-CH_L4_PH0P8_H1_AB
SSRX2-_CONN_15
SSRX2+_CONN_15
LC3
67ohm 320mA +-25%
I-15
(54,55) C_RX2_P
RC475
0R 5%
R0402_N NI
(54,55) C_RX1_N
RC476
0R 5%
R0402_N NI
SSRX1-_CONN_15
SSRX1+_CONN_15
LC4
67ohm 320mA +-25%
CO-CH_L4_PH0P8_H1_AB
I-15
(54,55) C_RX1_P
RC477
0R 5%
R0402_N NI
RC478
0R 5%
R0402_N I-15
(9,55) USB2_P2_WP2_DN
(9,55) USB2_P2_WP2_DP
LC5
67ohm 320mA +-25%
CO-CH_L4_PH0P8_H1_AB
RC479
NI
0R 5%
R0402_N I-15
DP_CON
DM_CON
SWAP FOR ROUTING
DP_CON (55)
DM_CON (55)
+VBUS_TYPEC
+V5P0A_TypeC_SW
+VBUS_TYPEC (54,55)
+V5P0A_TypeC_SW (54,55)
SSRX2-_CONN_15
SSRX2+_CONN_15
SSTX2+_CONN_15
SSTX2-_CONN_15
CR9520
ESD5344D
DFN10_PH0P5_ESD
I-15
SSRX1+_CONN_15
SSRX1-_CONN_15
SSTX1-_CONN_15
SSTX1+_CONN_15
CR9521
ESD5344D
DFN10_PH0P5_ESD
I-15
SWAP FOR ROUTING
(54,55) CC1
JTYPE_C_15
USB11249-0500B-1H
I-15
+VBUS_TYPEC
+VBUS_TYPEC
GND_8
GND_7
GND_6
GND_5
GND_2
SSRXp2
SSRXn2
VBUS_2
RFU1
Dn1
Dp1
CC1
VBUS_1
SSTXn1
SSTXp1
GND_1
GND_3
SSTXp2
SSTXn2
VBUS_3
CC2
Dp2
Dn2
RFU2
VBUS_4
SSRXn1
SSRXp1
GND_4
SSRX2+_CONN_15
SSRX2-_CONN_15
SBU1
DP_CON
DM_CON
SSTX1-_CONN_15
SSTX1+_CONN_15
SSTX2+_CONN_15
SSTX2-_CONN_15
DM_CON
DP_CON
SBU2
SSRX1-_CONN_15
SSRX1+_CONN_15
CC2 (54,55)
SWAP FOR ROUTING
cn_usb-c_ub11249-0500b-1h
20170718
yanzw
genhuan
3nod三诺
Project: 330S-14&15
Engineer: Luffy
Size
Custom
Title: TYPE-C CONN
Rev
V01
Date: Tuesday, September 26, 2017
Sheet 53 of 81


+V5P0A
+V5P0A_TypeC_SW
SH9520
0R
5%
R0603_N
IC 20mA
(9,55) USB2_P2_WP1_OC_N
R4619
0R
R0402_N
5%
(55) VBUS_EN
OCP_DET
VMON
U1
VBUS_EN
OCP_DET
VMON
3/30 Remove reserve ESD
GND
CR9523
220pF 50V 5%
NPO
C0402_N
CR9524
220pF 50V 5%
NPO
C0402_N
Swap P/N for USB3.1 GEN2
SSRX/TX no via layout.
2/22 change to 5448
Zdiff=90ohm
Swap P/N for USB3.1 GEN2
SSRX/TX no via layout.
10Gbps 2:1 MUX
CC1
CC2
CC1 (53,55)
CC2 (53,55)
(9,52) USB3_P2_WP2_RX_DN
(9,52) USB3_P2_WP2_RX_DP
C4530
C4531
0.1uF 10V 10%
X5R C0402_N
USB3_P2_WP2_RX_C_DN
USB3_P2_WP2_RX_C_DP
SSRX_1P/2N
SSRX_1N/2P
(9,52) USB3_P2_WP2_TX_DN
(9,52) USB3_P2_WP2_TX_DP
C4518
C4519
USB3_P2_WP2_TX_C_DN
USB3_P2_WP2_TX_C_DP
SSTX_1P/2N
SSTX_1N/2P
C_TX2_1P/2N
C_TX2_1N/2P
C_TX1_1P/2N
C_TX1_1N/2P
C_RX2_1P/2N
C_RX2_1N/2P
C_RX1_1P/2N
C_RX1_1N/2P
C4532
C4533
C4534
C4535
X5R C0402_NI
C_TX2_N (53,55)
C_TX2_P (53,55)
C_RX2_N (53,55)
C_RX2_P (53,55)
C_TX1_N (53,55)
C_TX1_P (53,55)
C_RX1_N (53,55)
C_RX1_P (53,55)
Zdiff=90ohm
(52) USB3_P2_WP2_RX_C_DN
(52) USB3_P2_WP2_RX_C_DP
(52) USB3_P2_WP2_TX_C_DN
(52) USB3_P2_WP2_TX_C_DP
GPIO4
M1
M0
GPIO
CURRENT_M1
CURRENT_M0
Realtek
RTS5448
REXT
R4700
6.2K
1%
R0402_N
E-PAD
LDO_3V3
5V_IN
VCON_IN
RTS5448-GR
3/20 change net name
LDO_3V3
C4700
4.7uF 16V 10%
X5R
C0603_N
C4701
0.1uF 10V 10%
C4702
0.1uF 10V 10%
C10031
10uF 6.3V 20%
X5R
C0402_N
+V5P0A_TypeC_SW
Power Switch High Enable
R4701
4.7K
5%
R0402_N
NI
VBUS_EN
VBUS_EN (55)
R4702
10K
5%
R0402_N
For C_VBUS
power switch enable pin
Power switch enable pin | Note
Low Active | R4701/R4702 mount
High Active | R4702 mount,R16 don't mount
LDO_3V3
R4708
10K
5%
R0402_N
M1
R4709
10K
5%
R0402_N
NI
R4706
10K
5%
R0402_N
M0
R4707
10K
5%
R0402_N
NI
Rp configuration
M1 | M0 | Note
Rp:900mA | 0 | 1 | R11/R12 mount,R10/R13 don't mount
Rp:1.5A | 1 | 0 | R10/R13 mount,R11/R12 don't mount
Rp:3.0A | 1 | 1 | R10/R12 mount,R11/R13 don't mount
Rp:1.5A (now)
+VBUS_TYPEC
R4710
200K1%
R0402
VMON
R4705
10K
1%
R0402_N
OCP_DET
R4703
4.7K
5%
R0402_N
R4704
10K
5%
R0402_N
OCP Low Enable
Power switch OCP pin | Note
Low Active | R4704/R4703 mount
High Active | R4704 mount,R4703 don't mount
For C_VBUS
power switch OCP pin
+VBUS_TYPEC (53,55)
+V5P0A_TypeC_SW (55)
+V5P0A (10,11,24,27,50,61,62,63,65,66,67,68,69,70,72)
3nod三诺
Project: 330S-14&15
Engineer: Luffy
Size: Custom
Title: TYPE-C Switch
Rev: V01
Date: Tuesday, September 26, 2017
Sheet 54 of 81


CC1
CC2
CR9055
CR9056
CR9057
AZ5725-01F.R7GR 1uA 5V
DFN1006p2x
+VBUS_TYPEC
+V5P0A_TypeC_SW
5/22 change to 100uF
C10007
100uF 6.3V +/-20%
SMD3.5X2.8mm
C10005
0.1uF 10V 10%
X5R
C0402_N
+V3P3A
R10085
100K
5%
R0402_N
1.5A~3A/Stack Port
U9003
IN
OUT
FLAG
SET
EN
GND
G518B1TP1U
(9,54) USB2_P2_WP1_OC_N
(54) VBUS_EN
C4301
0.1uF 25V 10%
C10004
10uF 25V 10%
X5R
C0805
C10006
10uF 25V 10%
X5R
C0805
R10020
82K
1%
R10021
21K
1%
DC ONLY : OCP SET TO 1.5A
AC IN: OCP SET TO 3A
Q8211
2N7002KW 115mA 60V
sot_323_dgs
(50) EC_TYPEC_CTL
R10024
1K
(53,54) C_TX2_N
(53,54) C_TX2_P
(53,54) C_TX1_N
(53,54) C_TX1_P
(53,54) C_RX2_N
(53,54) C_RX2_P
(53,54) C_RX1_N
(53,54) C_RX1_P
R9726
R9727
R9728
R9729
R9730
R9731
R9732
R9733
R9734
R9735
67ohm 320mA +-25%
CO-CH_L4_PH0P8_H1_AB
L9510
L9515
L9512
L9516
L9514
SSTX2-_CONN
SSTX2+_CONN
SSTX1-_CONN
SSTX1+_CONN
SSRX2-_CONN
SSRX2+_CONN
SSRX1-_CONN
SSRX1+_CONN
(9,53) USB2_P2_WP2_DN
(9,53) USB2_P2_WP2_DP
DM_CON
DP_CON
(53) DM_CON
(53) DP_CON
CR9514
CR9515
CR9522
ESD5344D
DFN10_PH0P5_ESD
I/O1
I/O2
I/O3
I/O4
GND
NC
(53,54) CC1
DP_CON
DM_CON
JTYPE_C_14
USB11249-0500B-1H
+VBUS_TYPEC
GND_8
GND_7
GND_6
GND_5
GND_2
SSRXp2
SSRXn2
VBUS_2
RFU1
Dn1
Dp1
CC1
VBUS_1
SSTXn1
SSTXp1
GND_1
GND_3
SSTXp2
SSTXn2
VBUS_3
CC2
Dp2
Dn2
RFU2
VBUS_4
SSRXn1
SSRXp1
GND_4
SBU1
cn_usb-c_ub11249-0500b-1h
20170718
yanzw
genhuan
(53,54) CC2
(54) +VBUS_TYPEC
(54) +V5P0A_TypeC_SW
Project: 330S-14&15
Engineer: Luffy
Size: Custom
Title: TYPE-C CONN
Rev: V01
Date: Tuesday, September 26, 2017
Sheet 55 of 81



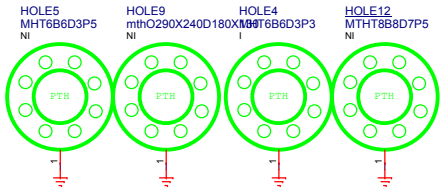
Shielding



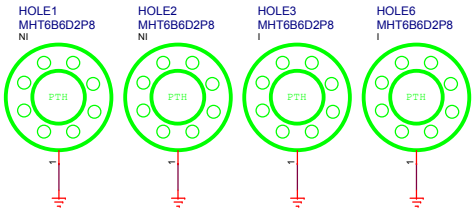
Holes

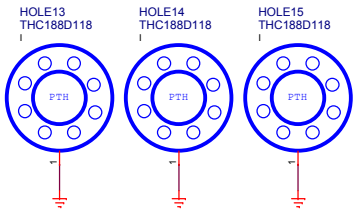
3/30 chnage screw

2.8mm

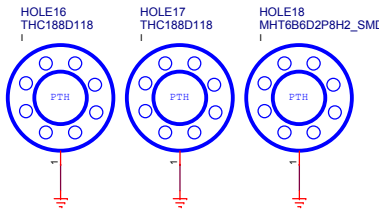


MB assembly HOLE





GPU THERMAL HOLE



CPU THERMAL HOLE

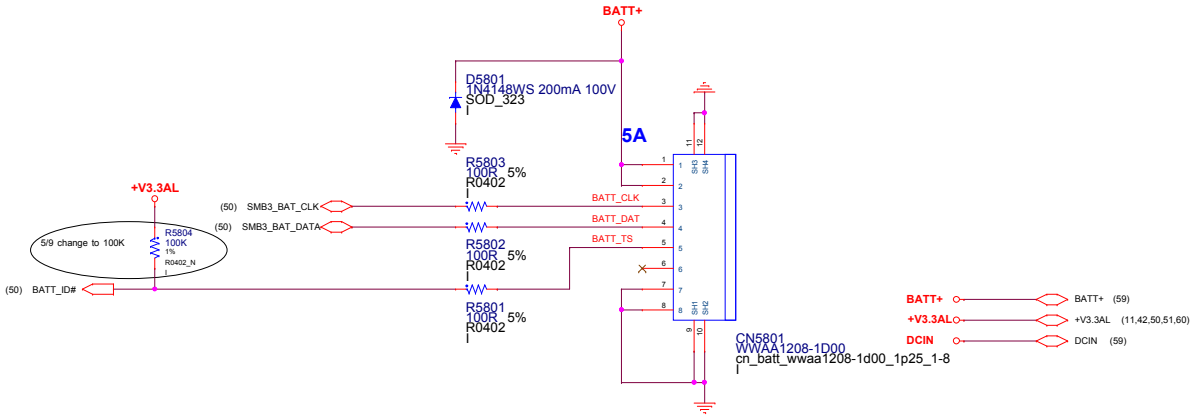
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: UART CONN & HOLE & CLIP	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 56 of 81	

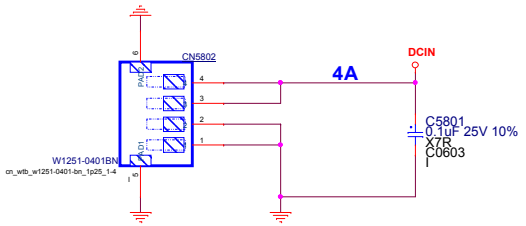
EVT=>SIV

No.	Change details	Change Reason
1	LID_INT_N change PU to +V3.3AL.	EC need recognize LID in S5.
2	Change KBL CONN Pin define.	EVT CE not confirm the Pin define correct.
3	Change Touch PAD Pin define.	Touch PAD SPEC update, add LID control Pin.
4	Change Keyboard power LED voltage to +V3.3AL.	Synchronize with System LED.
5	Type C IC Pin.20 change to LDO_3V3.	LDO_3V3 lose connection.
6	Install R574,R537.	Install for GPU.
7	remove DR3,DR4.	unnecessary
8	Change UBD2 solution.	for support 1V voltage
9	Add PU for SMB2_THM_CLK,DATA.	lose SMB PU
10	remove C10026.	unnecessary

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: HW Change list	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 57 of 81	

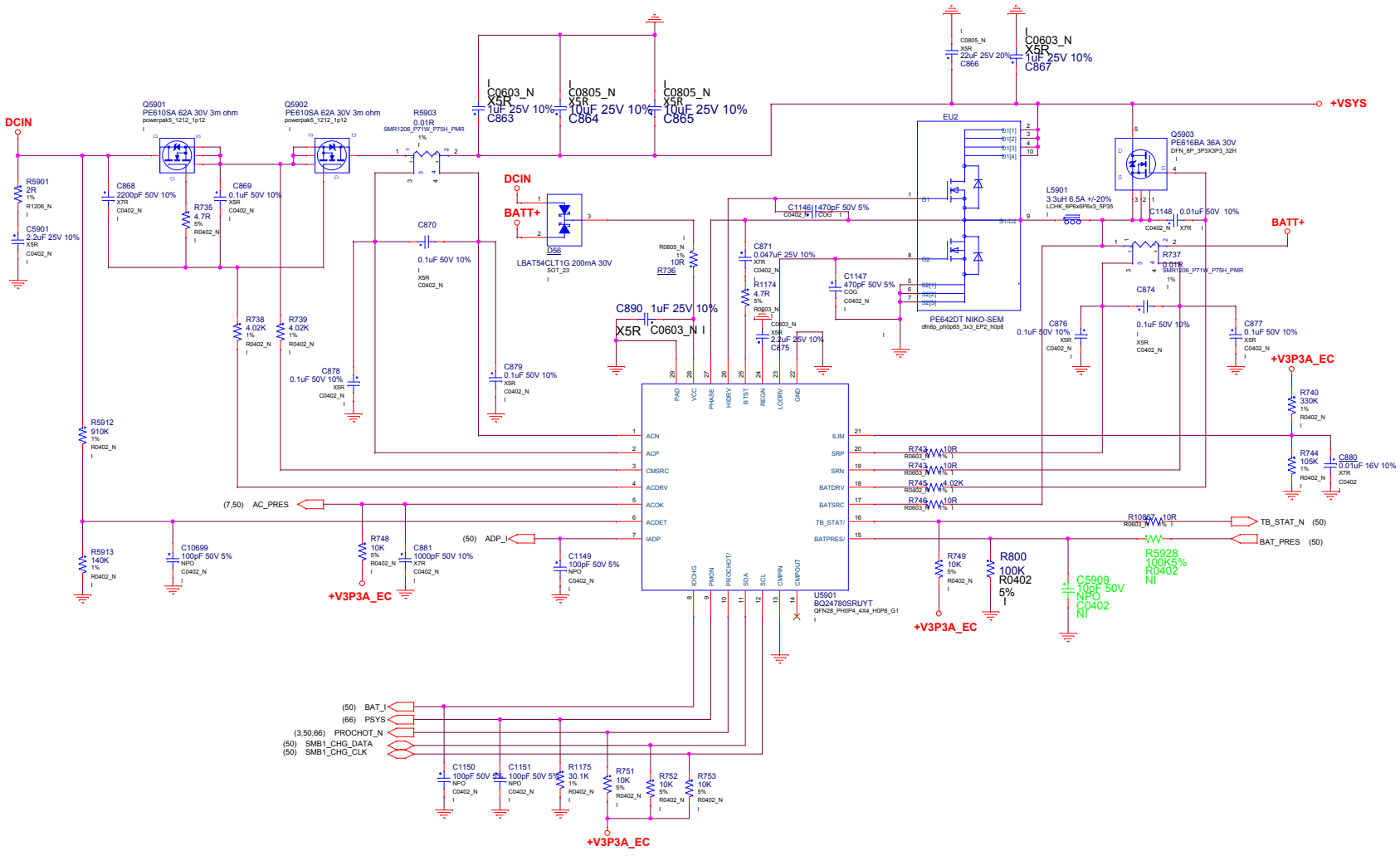
58: BATTERY CONNECTOR





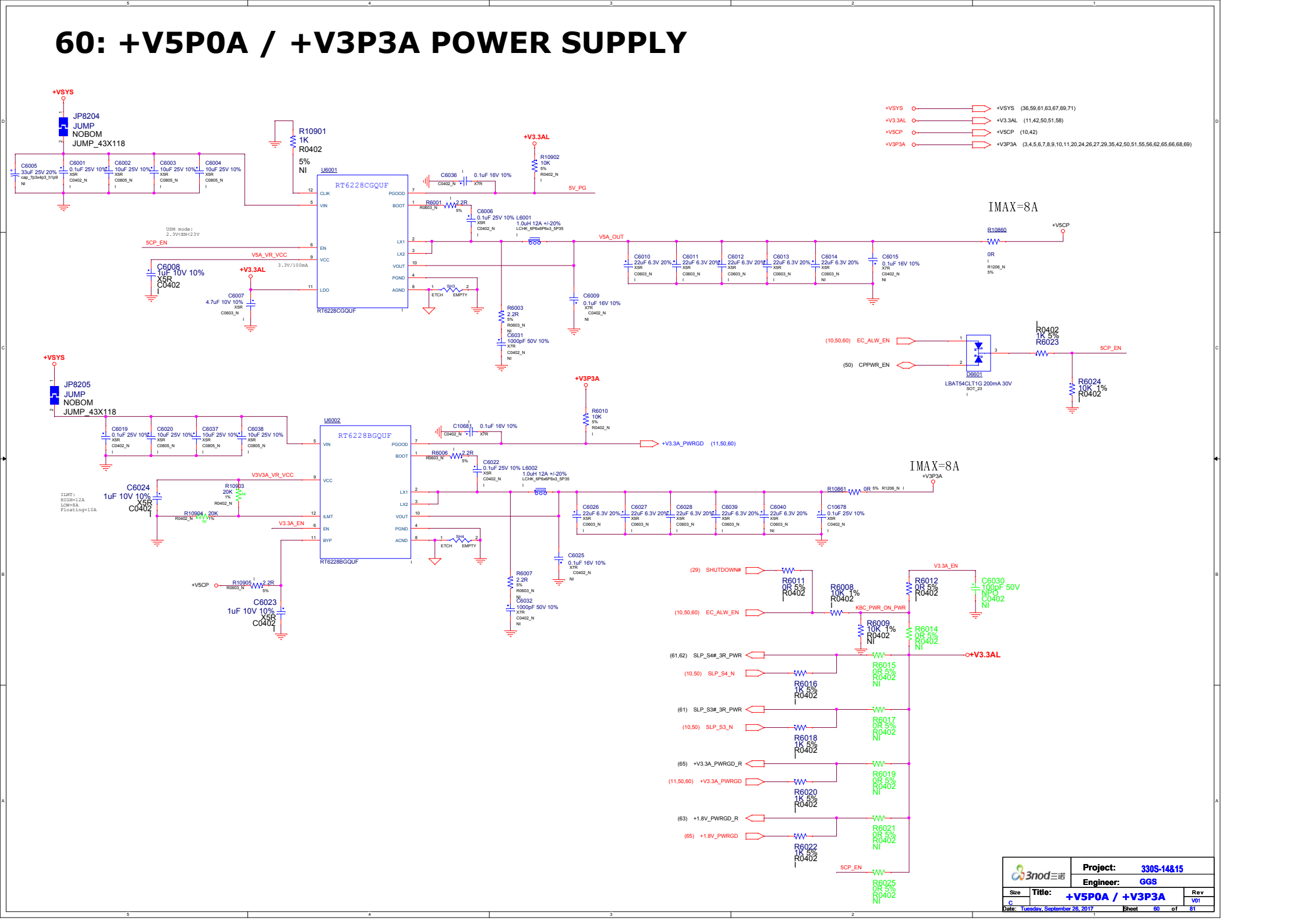
3nod三诺	Project: 330S-14&15		
	Engineer: Luffy		
Size C	Title: BATT CONN DC-IN		Rev V01
Date: Tuesday, September 26, 2017		Sheet 58 of 81	

59: BATTERY CHARGER



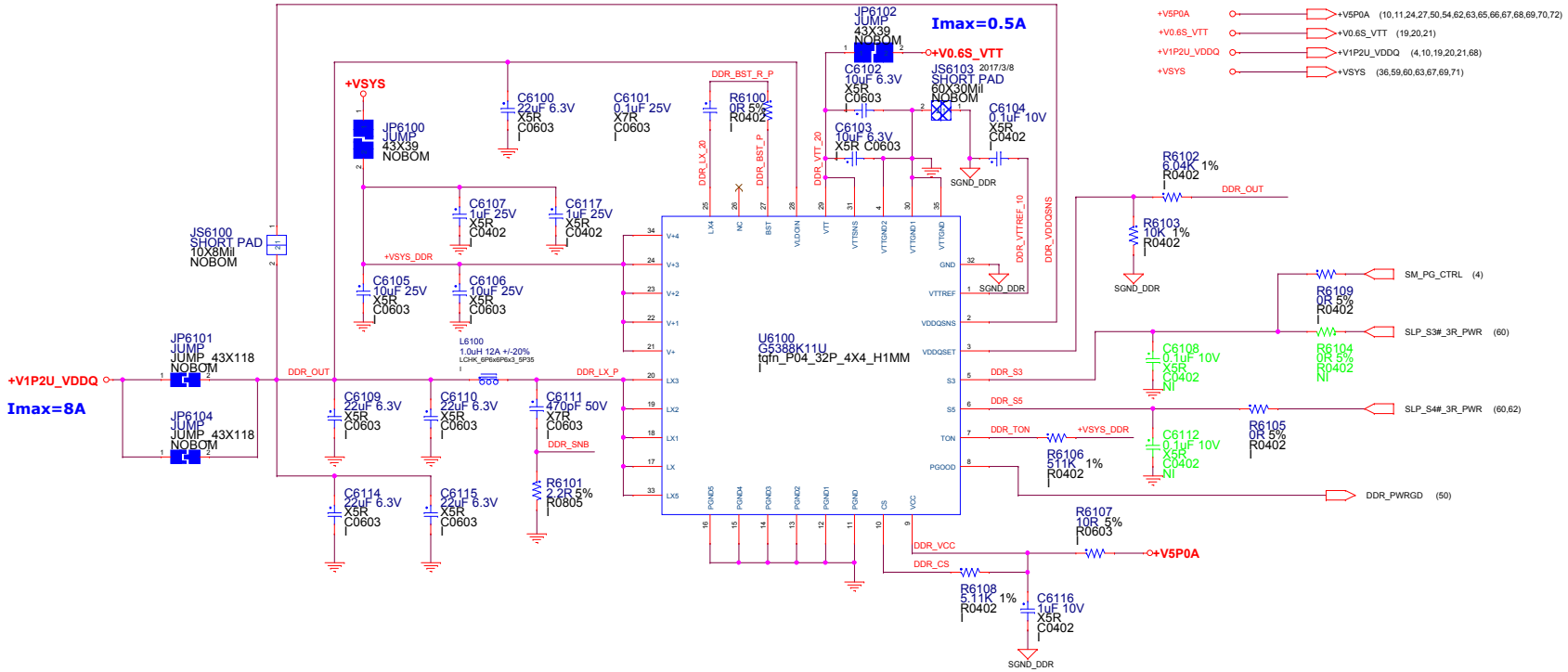
3nod三诺	Project:	330S-14&15
	Engineer:	GGS
Size: C	Title: CHARGER	Rev: V01
Date: Wednesday, September 27, 2017	Sheet 59 of 81	

60: +V5P0A / +V3P3A POWER SUPPLY



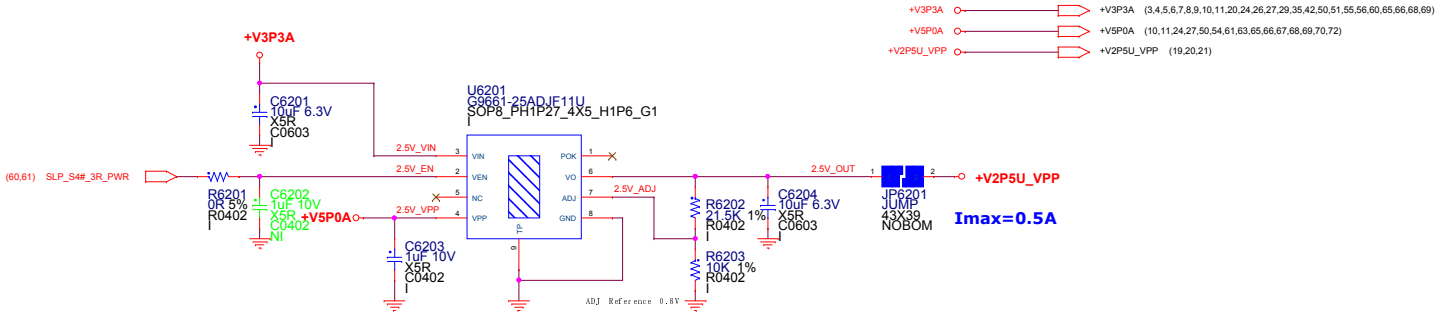
3nod三诺	Project:	330S-14&15	
	Engineer:	GGS	
Size: C	Title:	+V5P0A / +V3P3A	Rev: V01
Date: Tuesday, September 26, 2017	Sheet	60 of 81	

61: DDR POWER SUPPLY



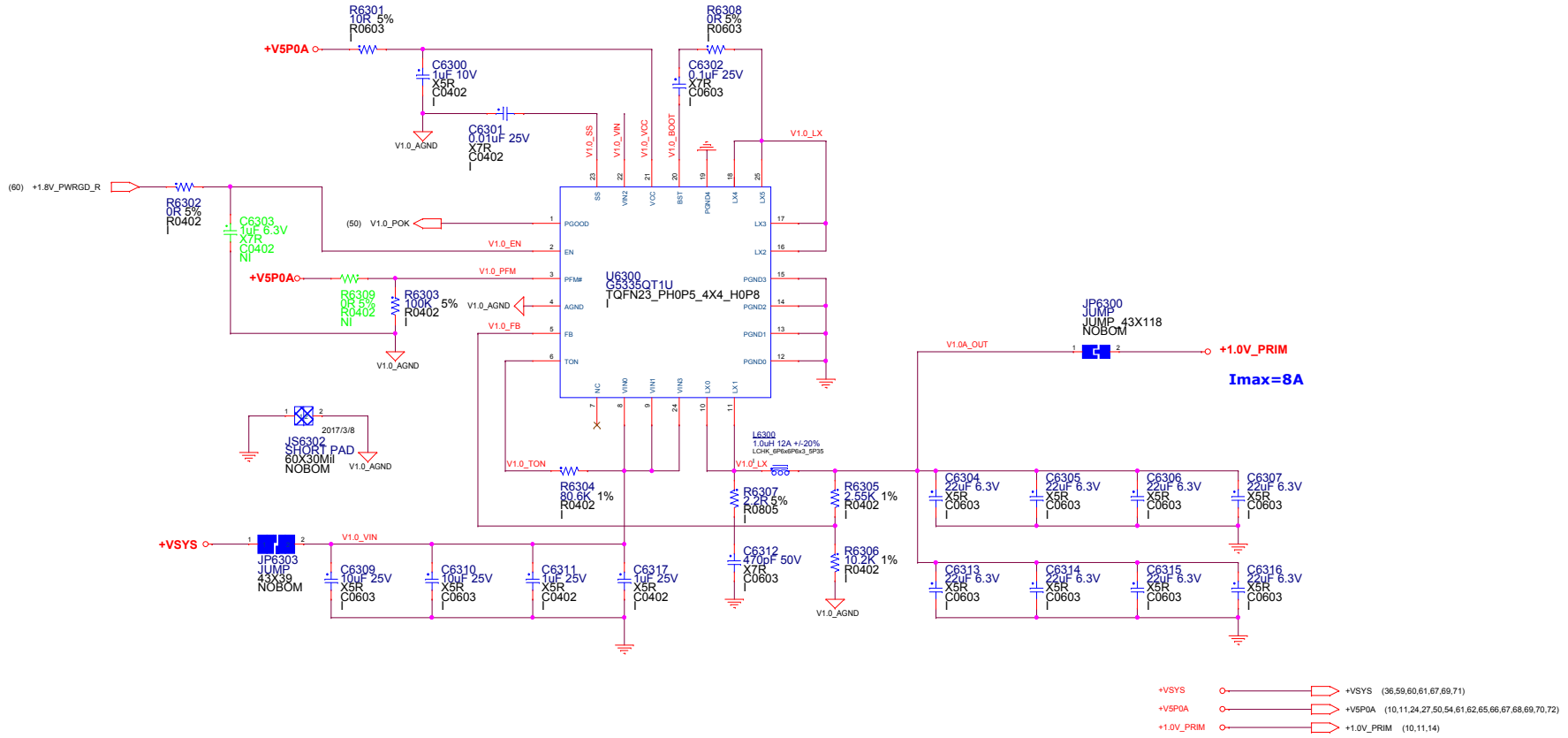
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: DDR Power	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 61 of 81	

62: +V2P5U_VPP POWER SUPPLY



3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: +V2P5U_VPP	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 62 of 81	

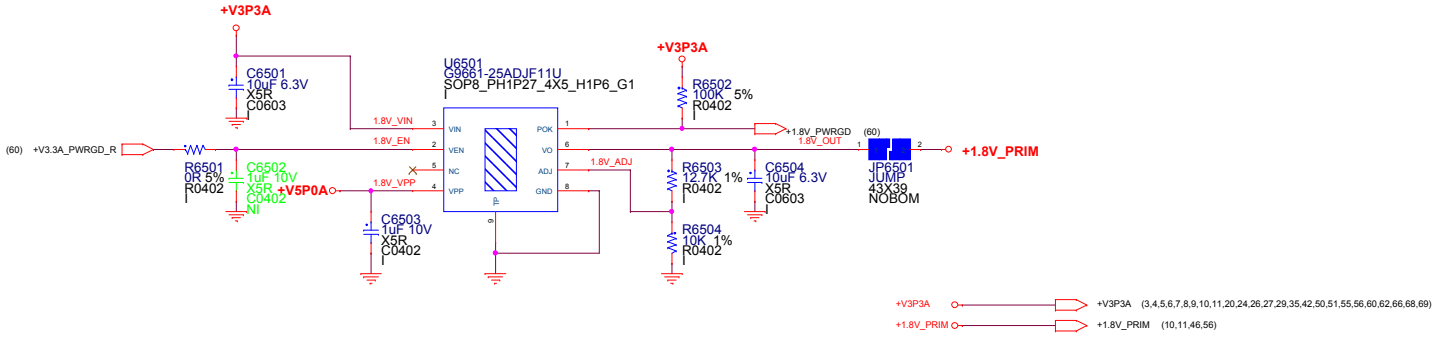
63: +1.0V_PRIM POWER SUPPLY



3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: C	Title:	+1.0V_PRIM
		Rev: V01
Date: Tuesday, September 26, 2017	Sheet 63 of 81	

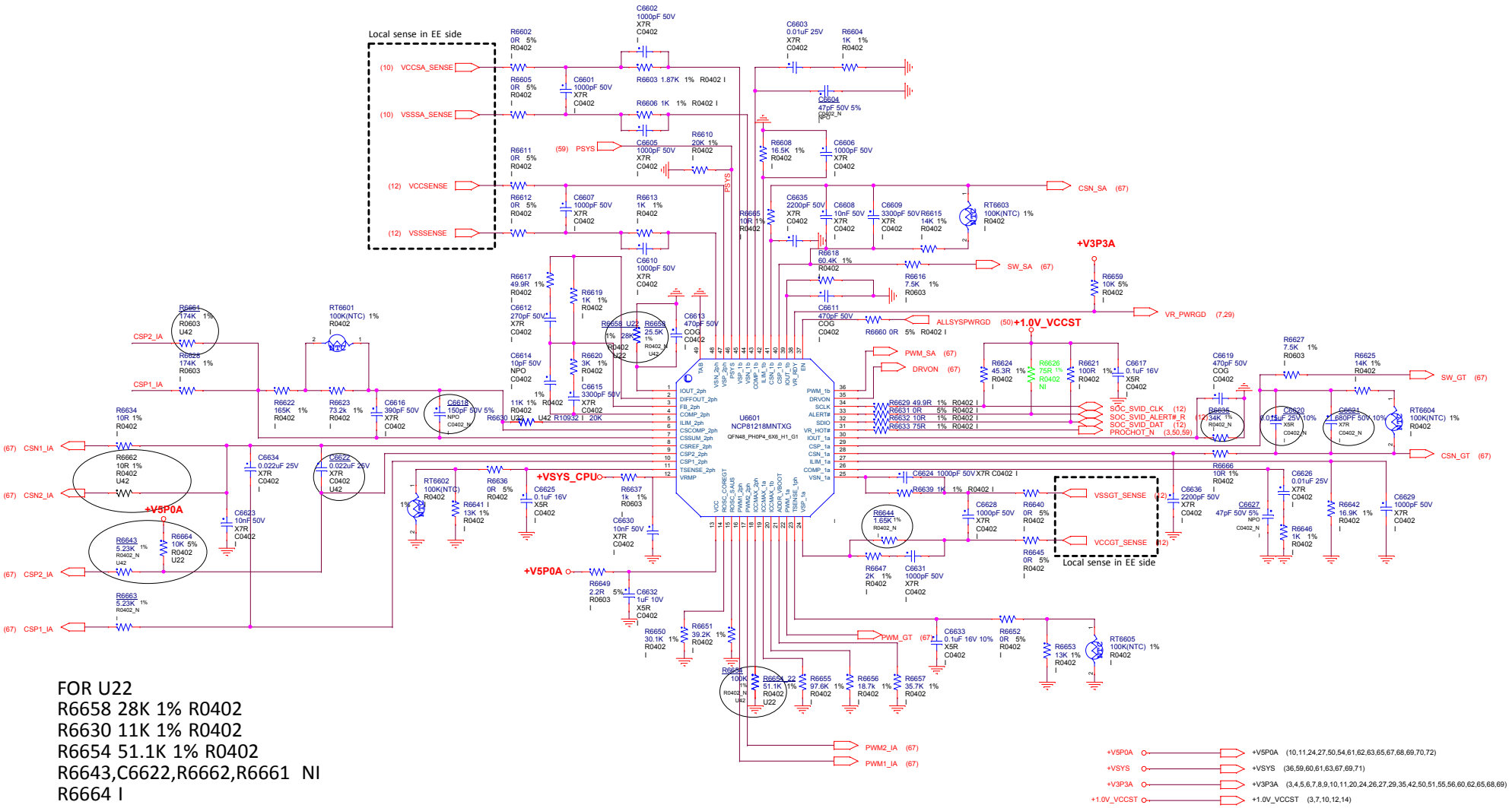
3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: NA	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 64 of 81	

65: +1.8V_PRIM POWER SUPPLY



3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: +1.8V_PRIM	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 65 of 81	

66: CPU POWER SUPPLY



FOR U22
R6658 28K 1% R0402
R6630 11K 1% R0402
R6654 51.1K 1% R0402
R6643,C6622,R6662,R6661 NI
R6664 I
C6744 NI

3nod三诺	Project:	330S-14&15	
	Engineer:	Luffy	
Size: C	Title:	CPU VR IC	Rev: V01
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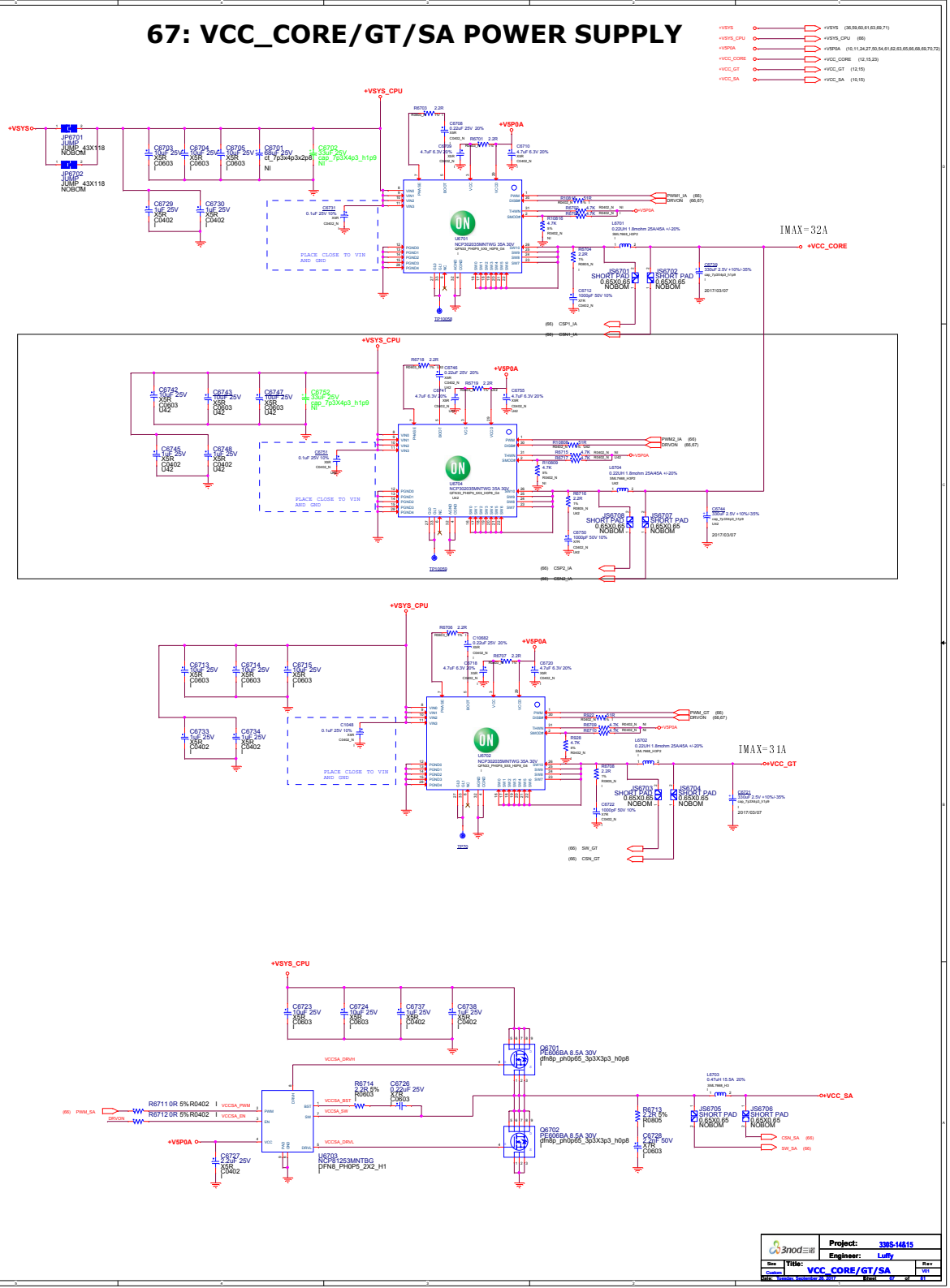
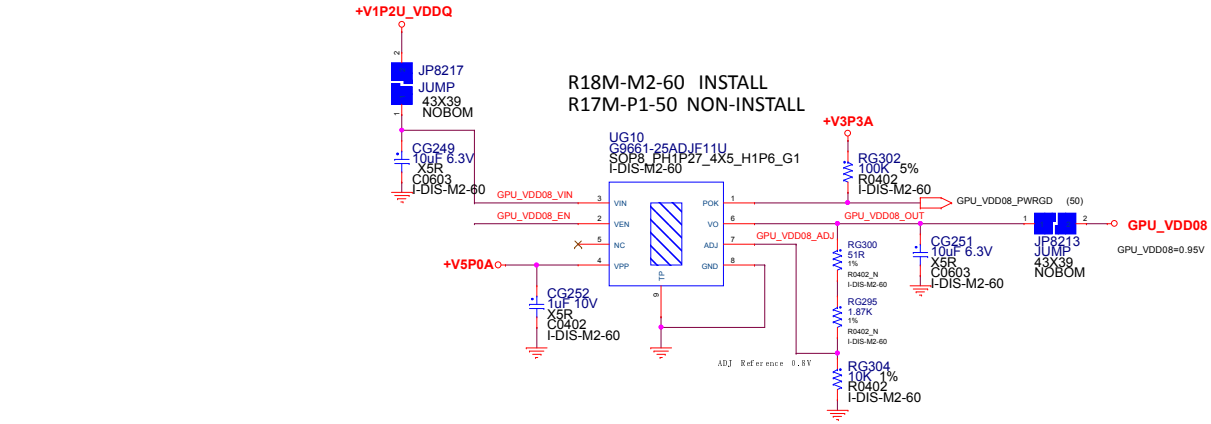
67: VCC_CORE/GT/SA POWER SUPPLY



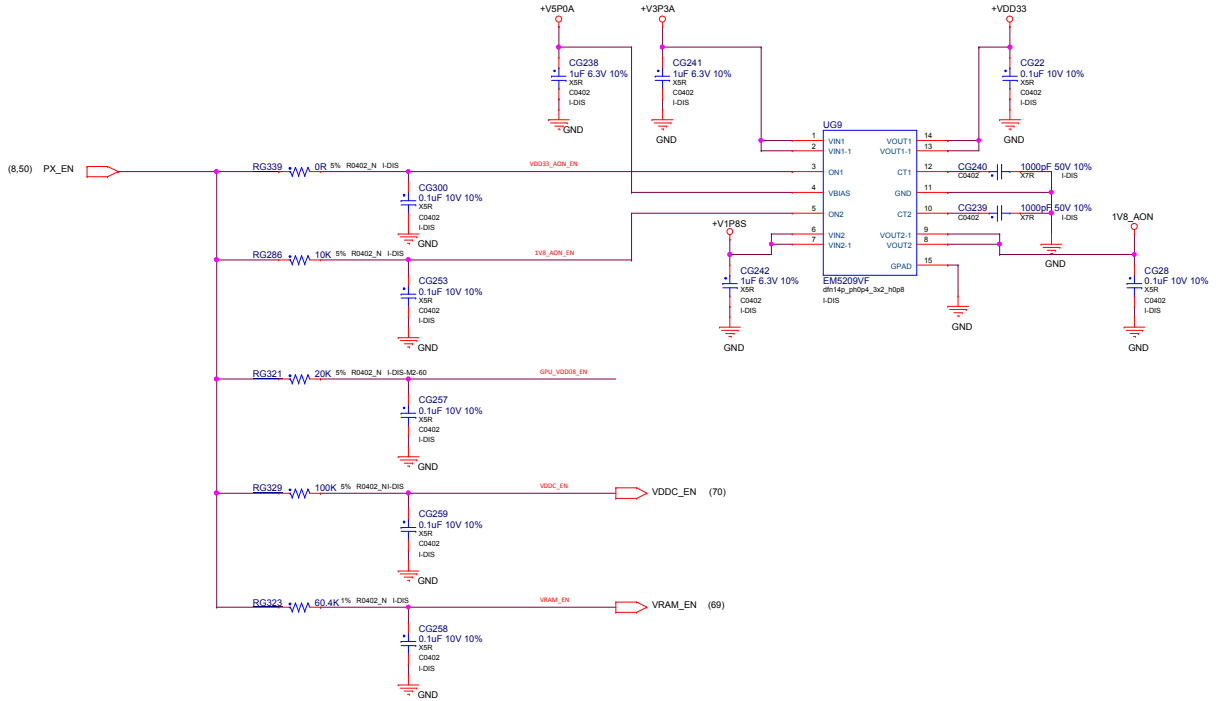
Project:	3385-14815
Engineer:	Luffy
Title:	VCC_CORE/GT/SA

VDD POWER SUPPLY for M2-60

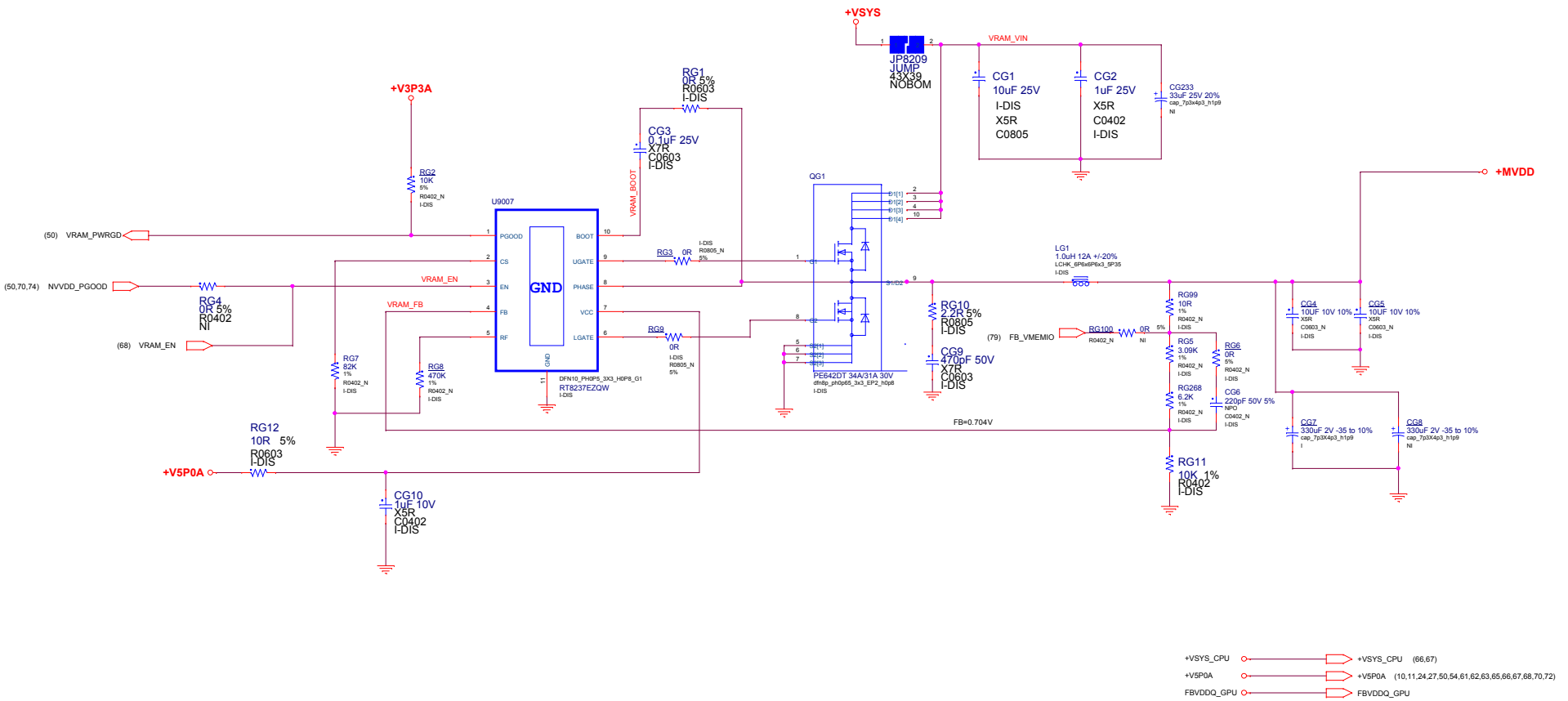


+V3P3A +V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,69)

GPU_VDD08 GPU_VDD08 (72,79)

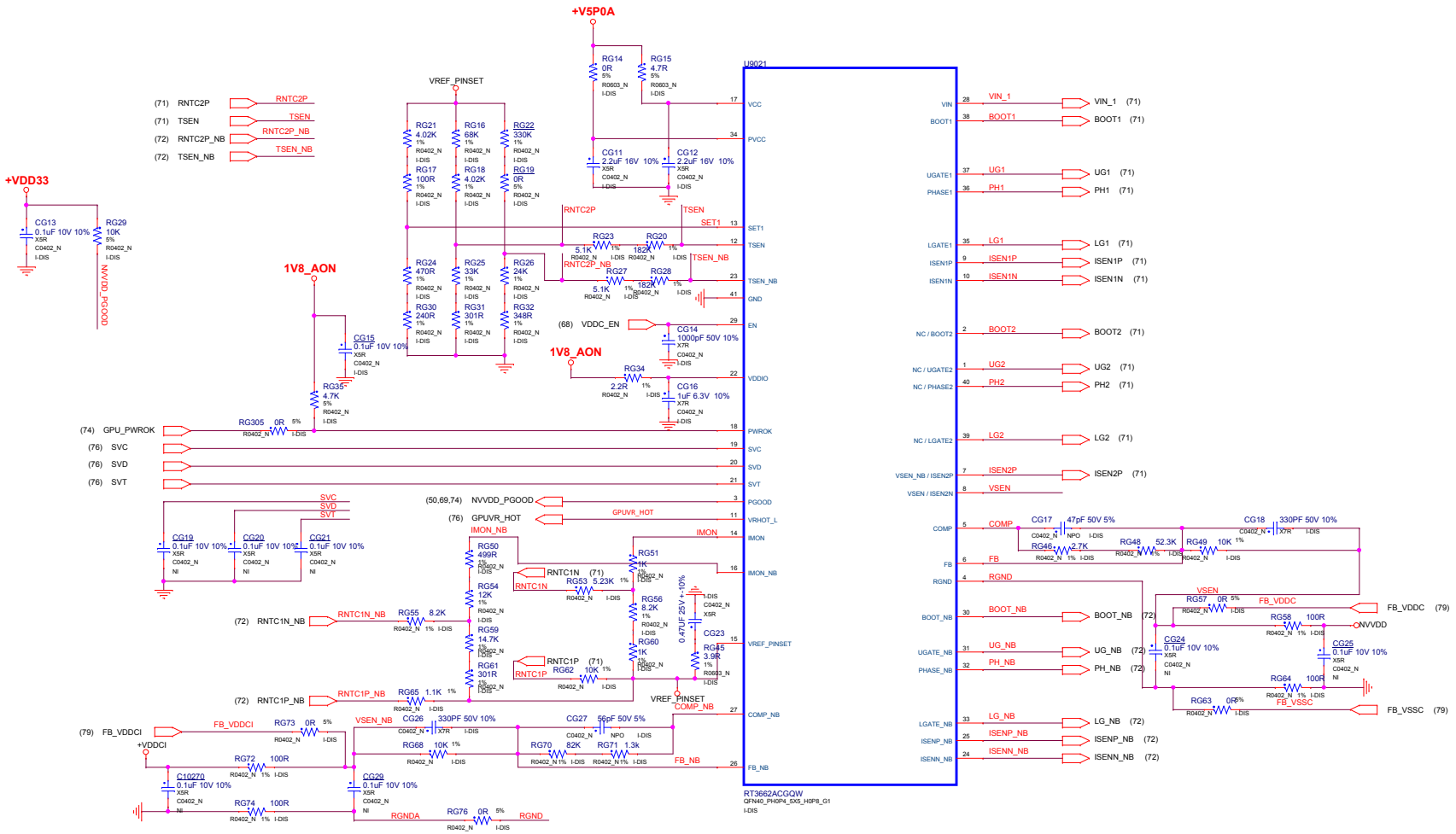


3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: GPU-VDD08	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 68 of 81	

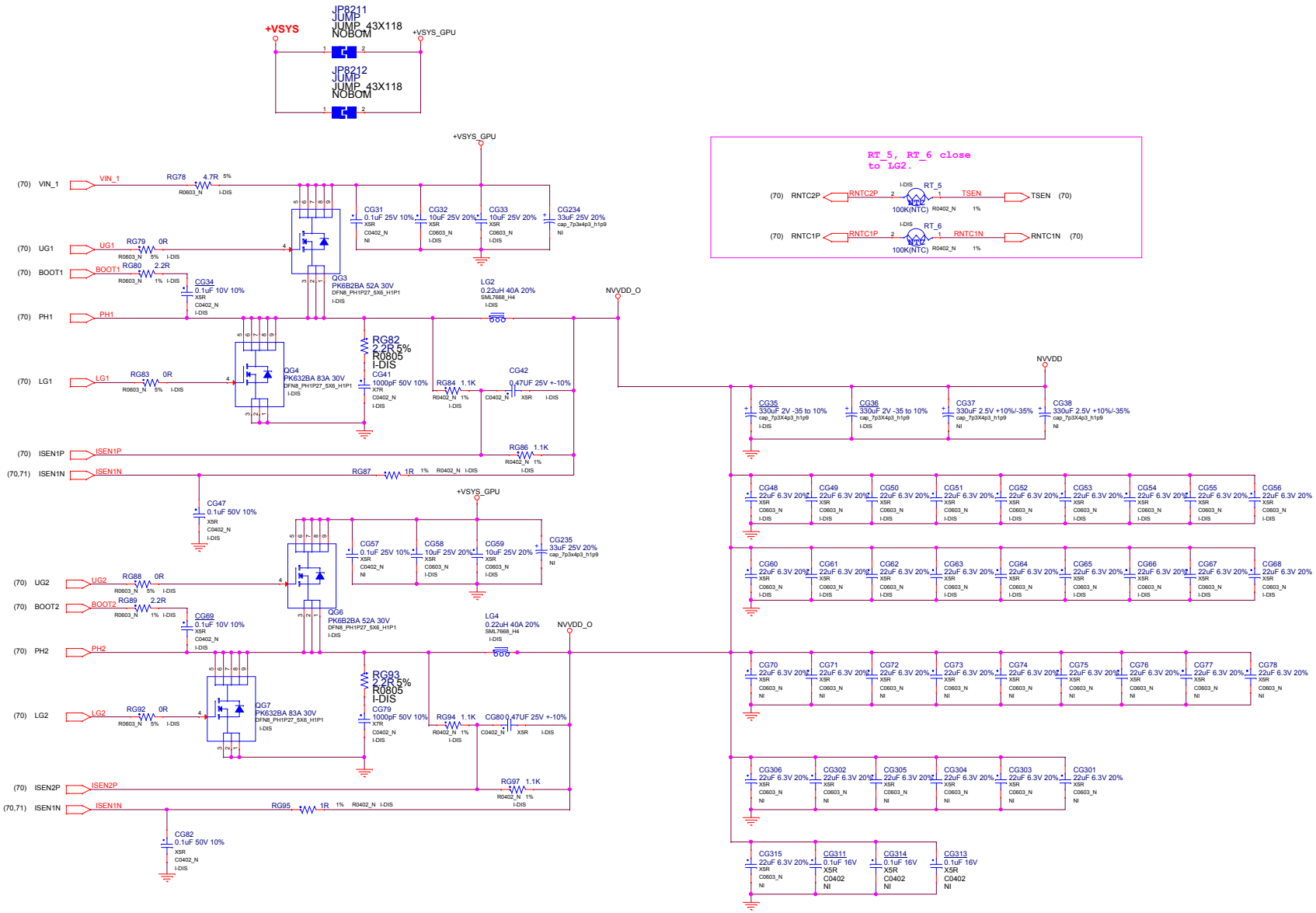


3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: C	Title:	VRAM POWER SUPPLY
Rev: V01		
Date: Wednesday, September 27, 2017	Sheet 69 of 81	

70: GPU POWER

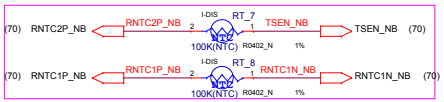


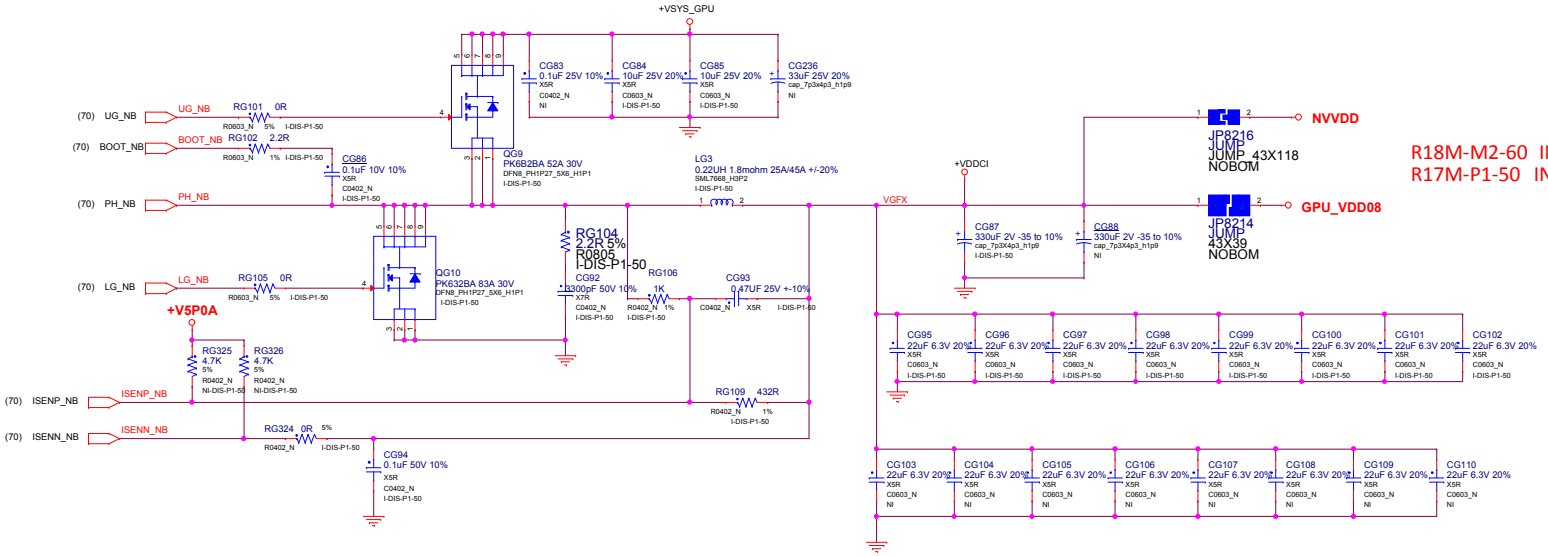
3nod三诺	Project:	330S-14&15	
	Engineer:	Luffy	
Size: C	Title:	GPU NVVDD	Rev: V01
Date: Tuesday, September 26, 2017	Sheet	70 of 81	



3nod三诺	Project:	330S-14&15	
	Engineer:	Luffy	
Size: C	Title:	GPU NVDD	Rev: V01
Date: Tuesday, September 26, 2017	Sheet	71 of 81	

RT_7, RT_8 close to LG3.





R18M-M2-60 INSTALL JP8216 AND NC this phase
R17M-P1-50 INSTALL JP8214, non-install JP8216

R18M-M2-60 INSTALL RG325/RG326

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: C	Title: VDDCI	Rev: V01
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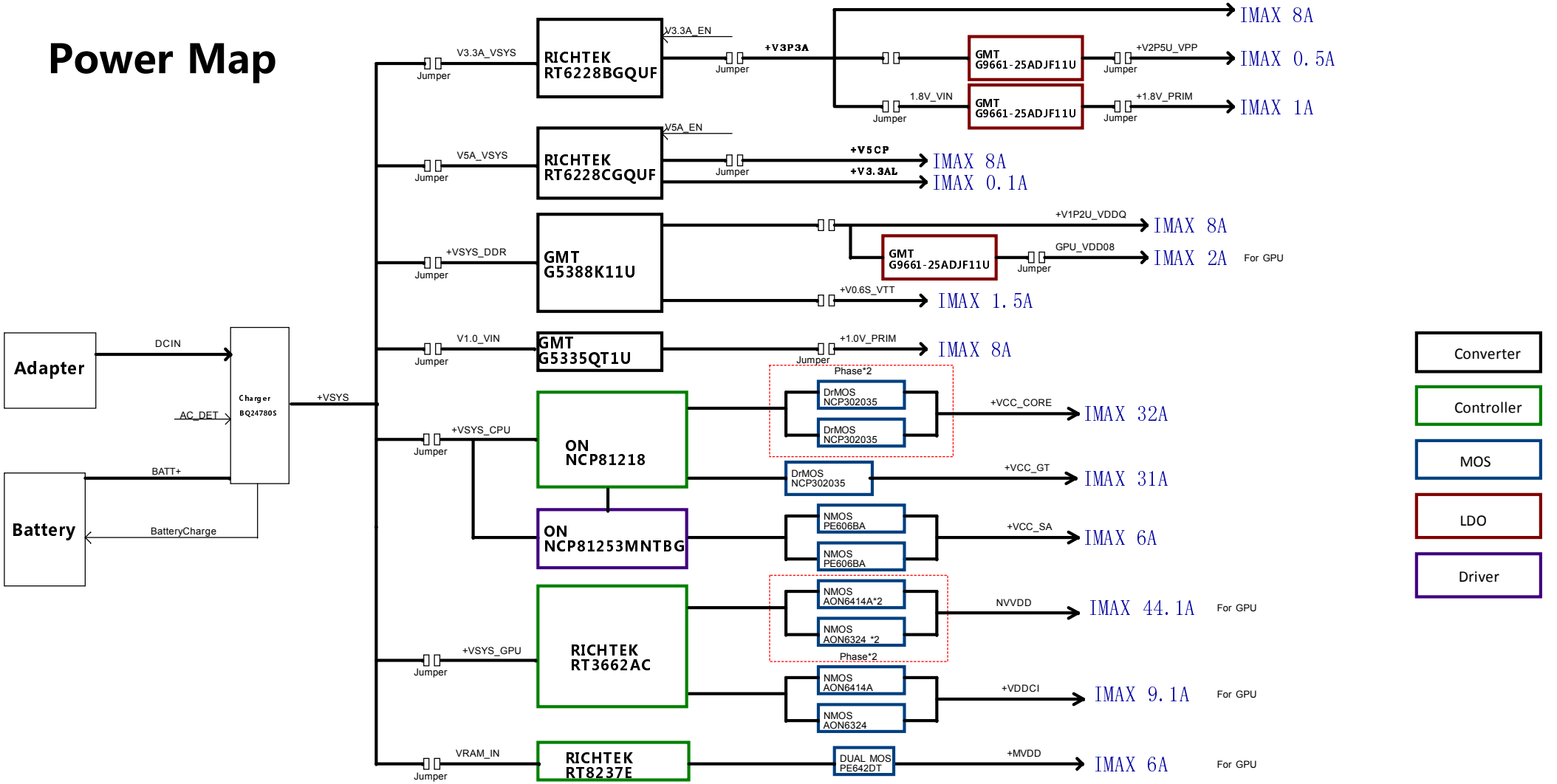
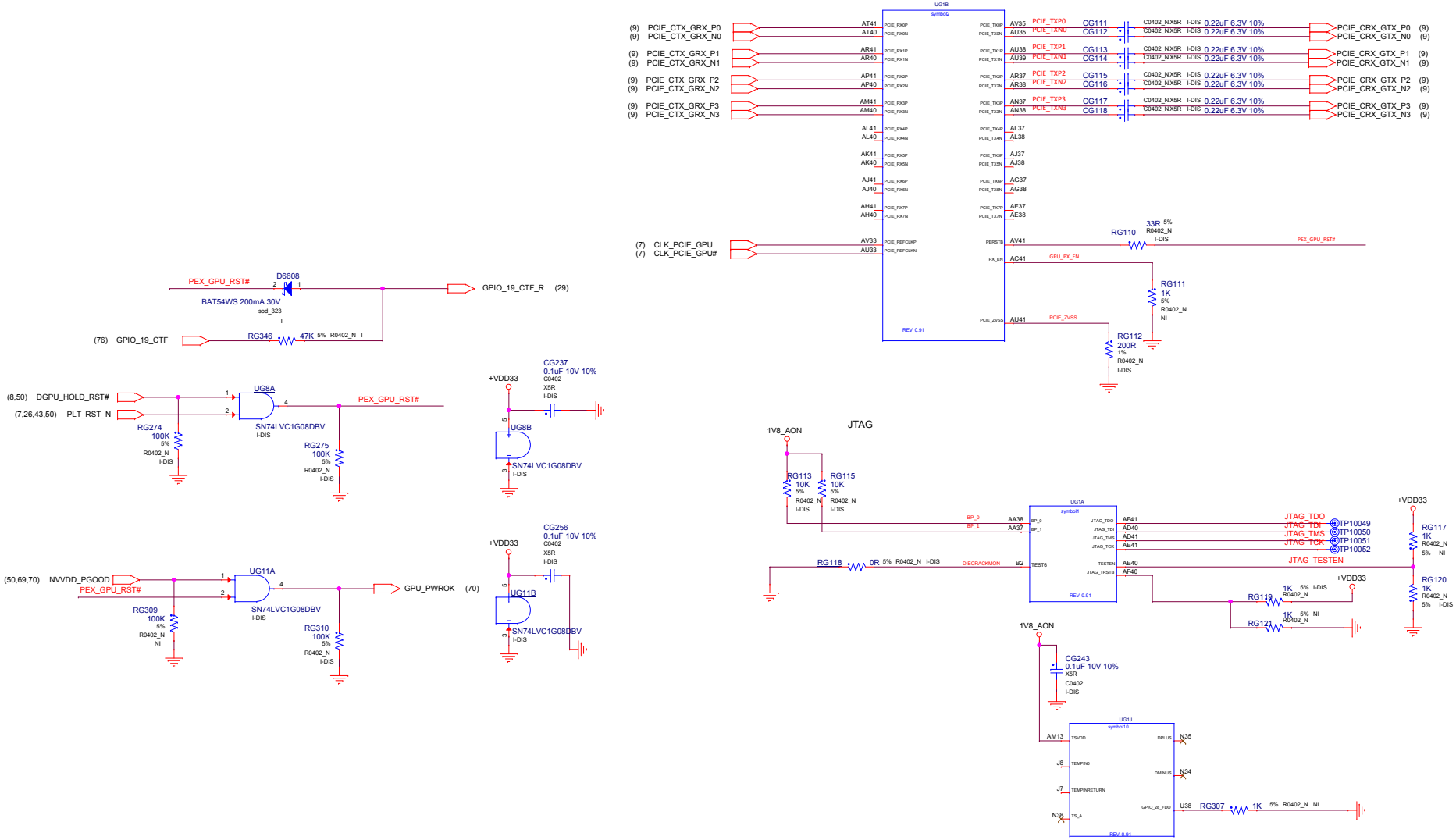
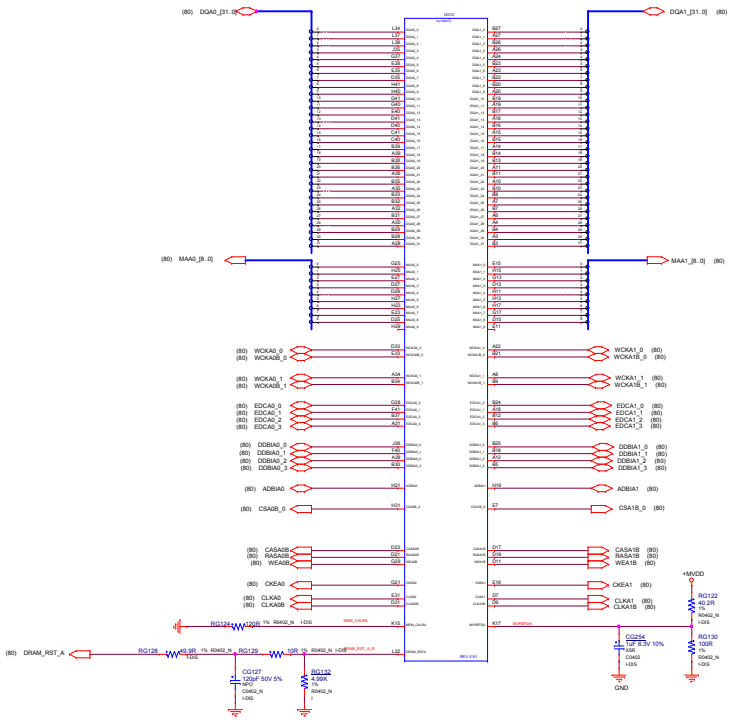
Power Map

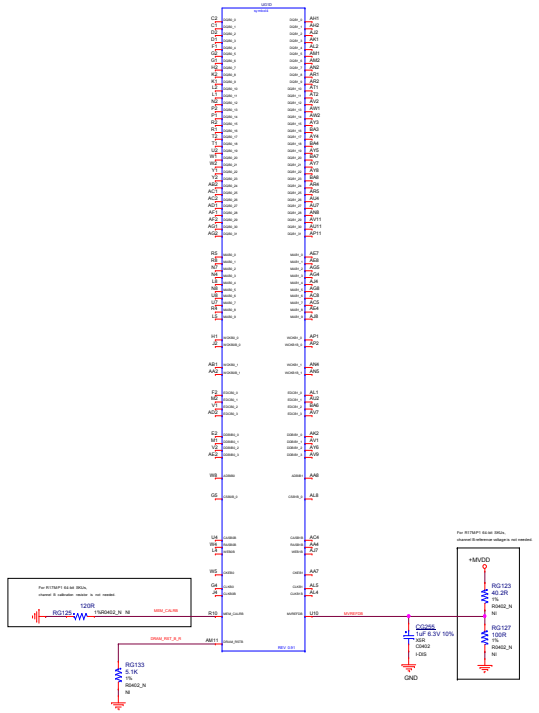


3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: B	Title: POWER MAP	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 73 of 81	

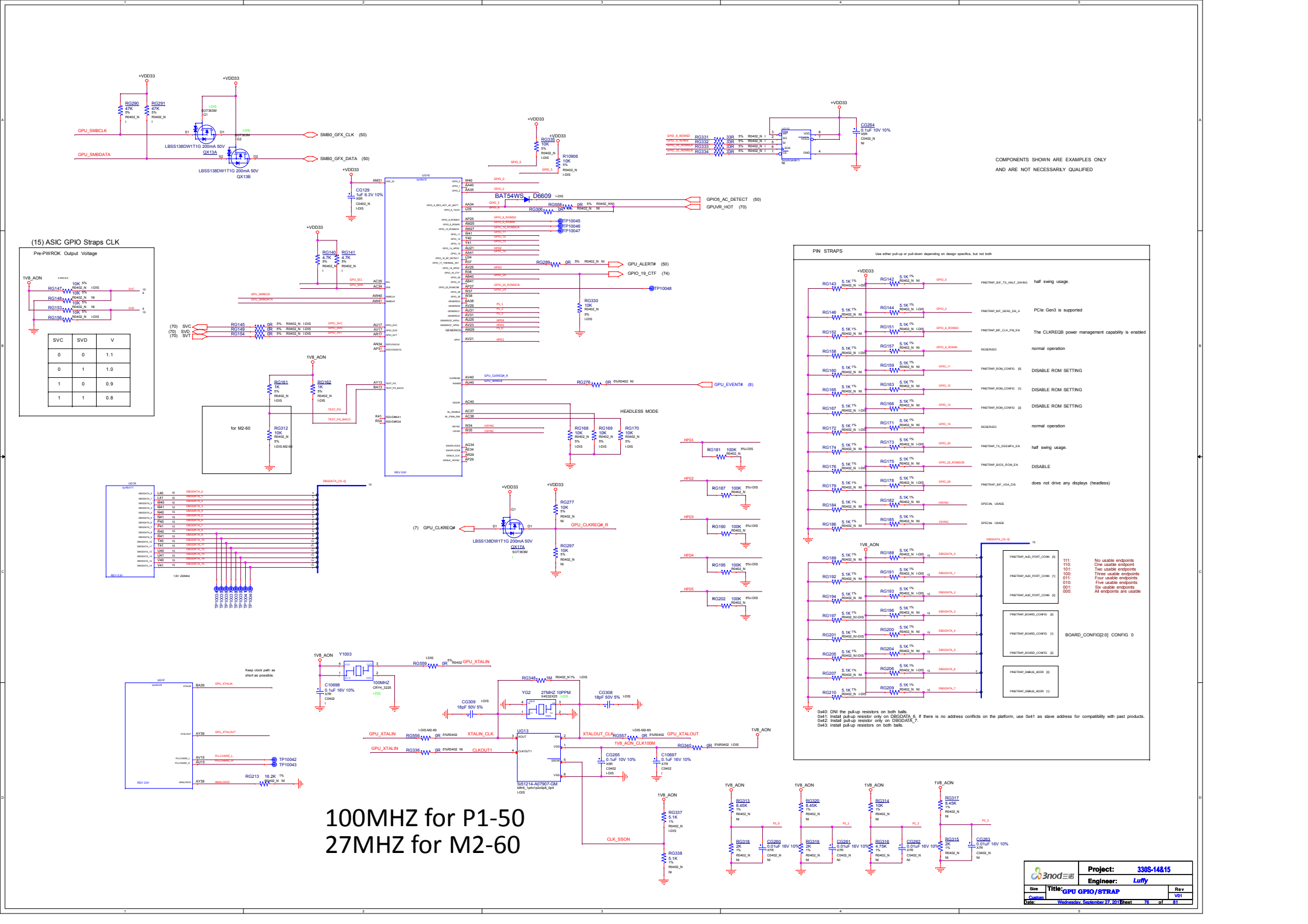


3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: Custom	Title: GPU PCIE/DP	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 74 of 81	





3nod三诺	Project:	3305-14&15
	Engineer:	Luffy
Size: D	Title: GPU MEM	Rev: MH
Date: Tuesday, September 26, 2017	Sheet 75 of 81	


(15) ASIC GPIO Straps CLK
Pre-PWROK Output Voltage
SVC SVD V
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
PIN STRAPS
Use either pull-up or pull-down depending on design specifics, but not both
PINSTRAP_BIF_TX_HALF_SWING half swing usage.
PINSTRAP_BIF_GEN3_EN_A PCIe Gen3 is supported
PINSTRAP_BIF_CLK_PM_EN The CLKREQB power management capability is enabled
RESERVED normal operation
PINSTRAP_ROM_CONFIG [0] DISABLE ROM SETTING
PINSTRAP_ROM_CONFIG [1] DISABLE ROM SETTING
PINSTRAP_ROM_CONFIG [2] DISABLE ROM SETTING
RESERVED normal operation
PINSTRAP_TX_DEEMPH_EN half swing usage.
PINSTRAP_BIOS_ROM_EN DISABLE
PINSTRAP_BIF_VGA_DIS does not drive any displays (headless)
SPECIAL USAGE
SPECIAL USAGE
PINSTRAP_AUD_PORT_CONN [0]
PINSTRAP_AUD_PORT_CONN [1]
PINSTRAP_AUD_PORT_CONN [2]
111: No usable endpoints
110: One usable endpoint
101: Two usable endpoints
100: Three usable endpoints
011: Four usable endpoints
010: Five usable endpoints
001: Six usable endpoints
000: All endpoints are usable
PINSTRAP_BOARD_CONFIG [0]
PINSTRAP_BOARD_CONFIG [1]
PINSTRAP_BOARD_CONFIG [2]
BOARD_CONFIG[2:0] CONFIG 0
PINSTRAP_SMBUS_ADDR [0]
PINSTRAP_SMBUS_ADDR [1]
0x40: DNI the pull-up resistors on both balls.
0x41: Install pull-up resistor only on DBGDATA_6. If there is no address conflicts on the platform, use 0x41 as slave address for compatibility with past products.
0x42: Install pull-up resistor only on DBGDATA_7.
0x43: Install pull-up resistors on both balls.
COMPONENTS SHOWN ARE EXAMPLES ONLY
AND ARE NOT NECESSARILY QUALIFIED
100MHZ for P1-50
27MHZ for M2-60
Project: 330S-14&15
Engineer: Luffy
Title: GPU GPIO/STRAP
Rev V01
Date: Wednesday, September 27, 2017
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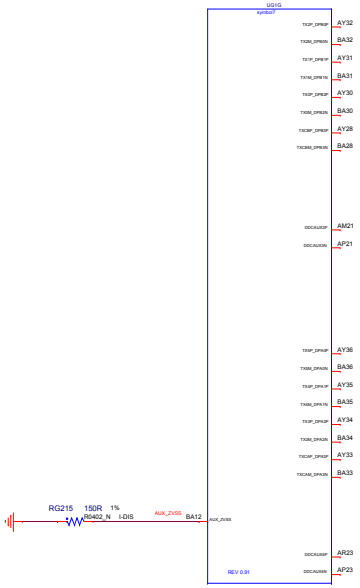
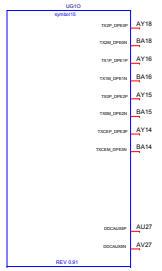
ASIC - TMDP (A/B)



ASIC - TMDP (C/D)

ASIC - TMDP (E)



3nod三诺	Project: 330S-14&15		
	Engineer: Luffy		
Size: Custom	Title: GPU DISPLAY INTERFACE		Rev: V01
Date: Tuesday, September 26, 2017	Sheet 77 of 81		

3nod三诺	Project: 330S-14&15	
	Engineer: Luffy	
Size: C	Title: NV N17S(5/5)_MEM	Rev: V01
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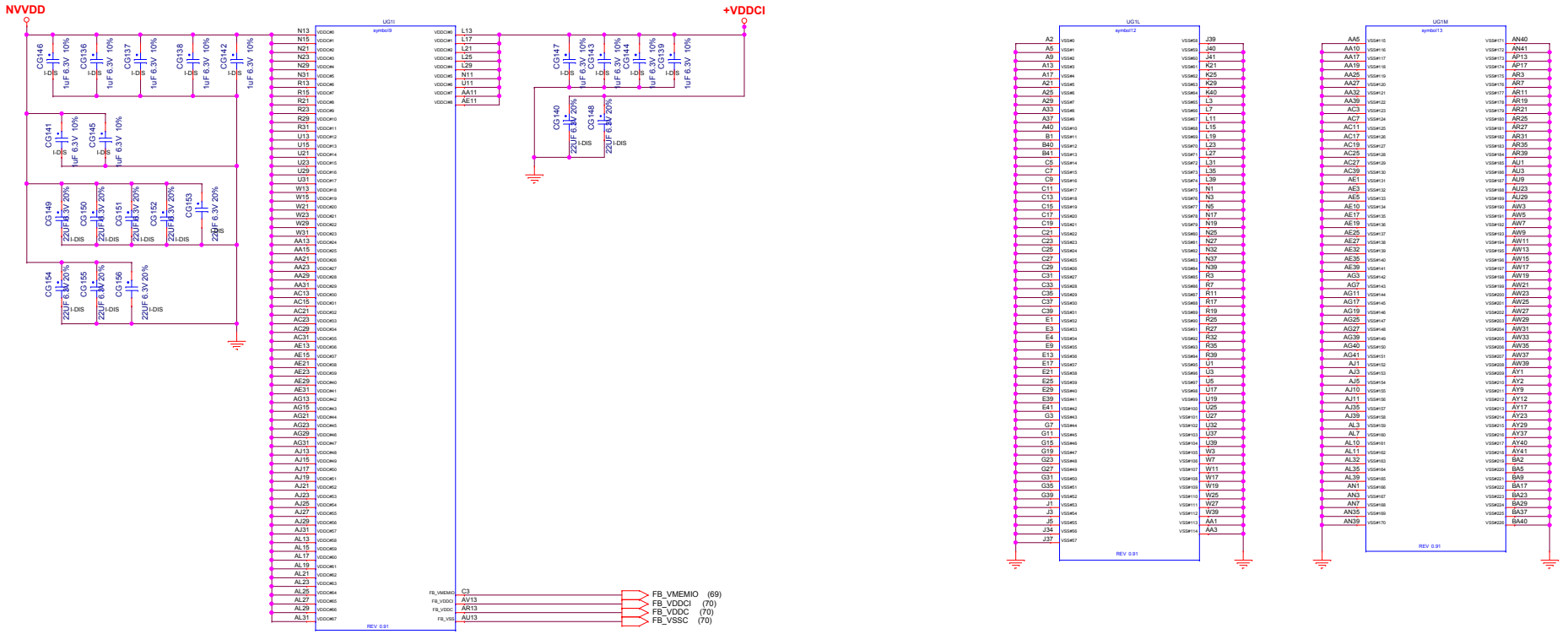

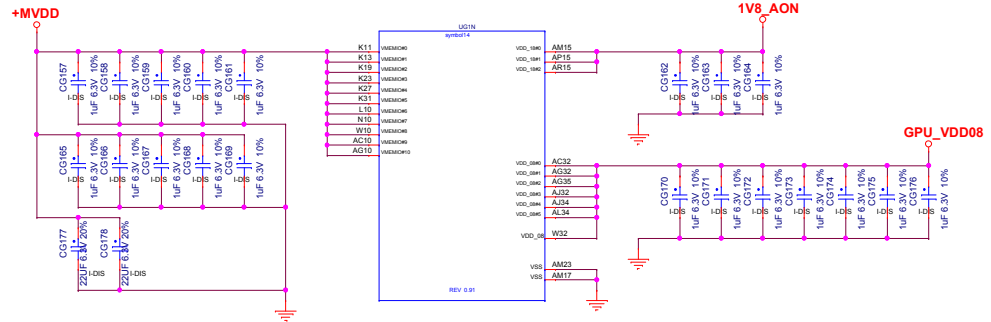

For cost effective designs where VDDCI and VDD_08 are supplied by one regulator, have the VDDCI and VDD_08 balls joined on a unified power plane.

3nod三诺	Project:	330S-1415	
	Engineer:	Luffy	
Size: C	Title: GPU POWER/GND		Rev: V01
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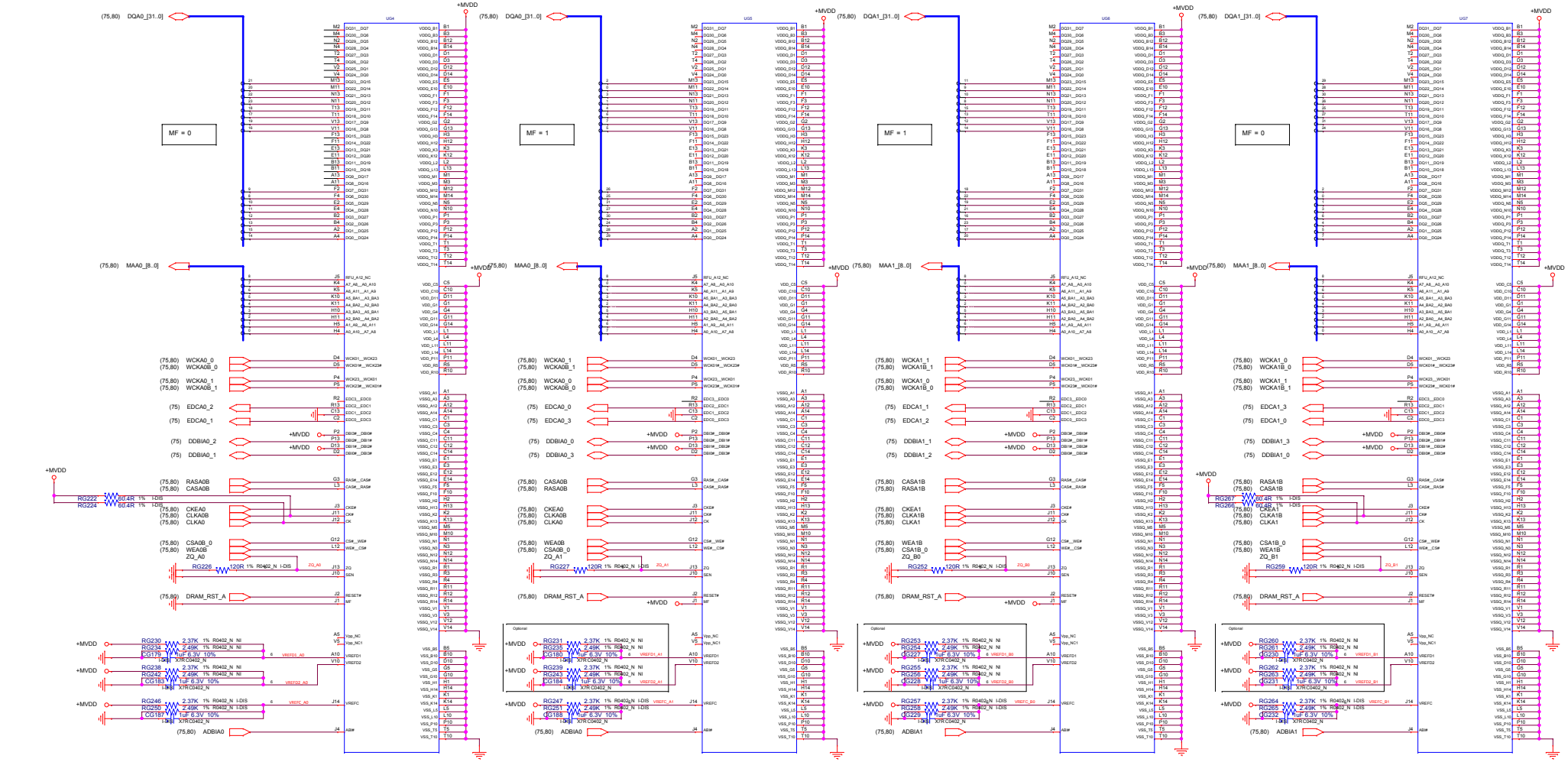
(6) GDDR5 Memory Channels A & B (x32 Mode)

COMPONENTS SHOWN ARE EXAMPLES ONLY

AND ARE NOT NECESSARILY QUALIFIED



3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: Custom	Title: VRAM (GDDR5)	Rev: V01
Date: Tuesday, September 26, 2017	Sheet 80 of 81	

3nod三诺	Project:	330S-14&15
	Engineer:	Luffy
Size: D	Title: RSVD	Rev: V01
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