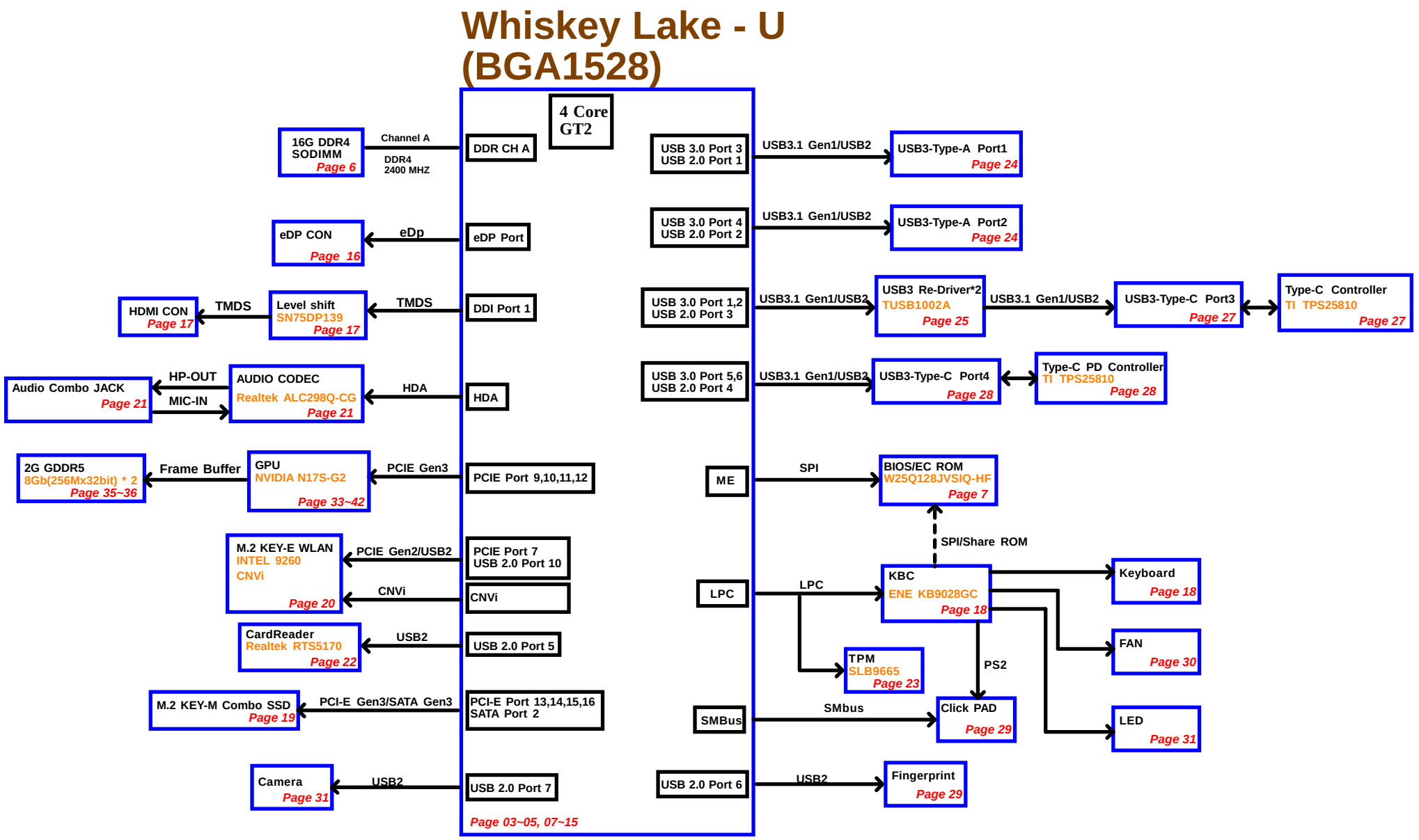
WhiskeyLake - U Processor PlatformMS-14B3 VER : B



MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-14B3 | Rev: 0A

Date: Friday, November 16, 2018 | Sheet 1 of 57

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER STATES

Voltage	Description	Control Signal	SLP_S5#	SLP_S4#	SLP_S3#
PWR_SRC	AC ADAPTER OR BATTERY IN		H	H	H
+5VALW	5.0V always on power rail	PWR_SRC	L	L	L
+3VALW	3.3V always on power rail	PWR_SRC	L	L	L
+5VSUS	5.0V power rail	SUS_ON	L	L	L
+3VSUS	3.3V power rail	SUS_ON	L	L	L
+1_8VSUS	1.8V power rail	3V5VSUSPWRGD	L	L	L
+1_05VSUS	1.05V power rail	1_8VSUSPWRGD	L	L	L
+2_5VMEM_VPP	2.5V power rail DDR (off in S4-S5)	DIMM_ON_VPP	H	L	L
+VCCST	1.05V power rail CPU (off in S4-S5)	DIMM_ON_VPP	H	L	L
+VCCPLL	1.05V power rail CPU (off in S4-S5)	+VCCST	H	L	L
+1_2VDIMM	1.2V power rail DDR (off in S4-S5)	DIMM_ON_VDDQ	H	L	L
+VDDQC	1.2V power rail CPU DRAM (off in S4-S5)	+1_2VDIMM	H	L	L
+VCCPLL_OC	1.2V power rail CPU (off in S4-S5)	+1_2VDIMM	H	L	L
+5VRUN	5.0V switched power rail (off in S3-S5)	RUND	H	H	L
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUND	H	H	L
+1_8VRUN	1.8V power rail AUDIO (off in S3-S5)	RUND	H	H	L
+VCC_IO	1.05V rail for Processor & PCH (off in S3-S5)	RUND	H	H	L
+VCCSTG	1.05V power rail CPU (off in S3-S5)	+VCC_IO	H	H	L
+0_6VTT_RUN	0.6V DDR Termination voltage (off in S3-S5)	DDR_VTT_CTRL	H	H	L
+VCC_SA	0.55V to 1.15V Voltage for Processor	VR_ON	H	H	L
+VCC_CORE	0.55V to 1.5V Voltage for Processor	VR_ON	H	H	L
+VCC_GT	0.55V to 1.52V Core Voltage for Processor	VR_ON	H	H	L

Note: WHEN AC MODE, System turn on then +*VSUS will always keep high

S4(Suspend to Disk)
S3(Suspend to RAM)
S0(Full ON)

MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

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Reference 16S1

CPU1A

Port B
HDMI
DDI1

<17> HDMI1_TX2_DN — AL5 DDI1_TXN_0
<17> HDMI1_TX2_DP — AL6 DDI1_TXP_0
<17> HDMI1_TX1_DN — AJ5 DDI1_TXN_1
<17> HDMI1_TX1_DP — AJ6 DDI1_TXP_1
<17> HDMI1_TX0_DN — AF6 DDI1_TXN_2
<17> HDMI1_TX0_DP — AF5 DDI1_TXP_2
<17> HDMI1_CLK_DN — AE5 DDI1_TXN_3
<17> HDMI1_CLK_DP — AE6 DDI1_TXP_3

AC4 DDI2_TXN_0
AC3 DDI2_TXP_0
AC1 DDI2_TXN_1
AC2 DDI2_TXP_1
AE4 DDI2_TXN_2
AE3 DDI2_TXP_2
AE1 DDI2_TXN_3
AE2 DDI2_TXP_3

Remove DDI2 #2018.08.28

Port A
eDP
DDI0

EDP_TXN_0 AG4 EDP_TX0_DN — EDP_TX0_DN <16>
EDP_TXP_0 AG3 EDP_TX0_DP — EDP_TX0_DP <16>
EDP_TXN_1 AG2 EDP_TX1_DN — EDP_TX1_DN <16>
EDP_TXP_1 AG1 EDP_TX1_DP — EDP_TX1_DP <16>
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1

EDP_AUX AH4 EDP_AUX_DN — EDP_AUX_DN <16>
EDP_AUX_P AH3 EDP_AUX_DP — EDP_AUX_DP <16>

DISP_UTILS AM7 EDP_DISP_UTIL — TPJNC47

DDI1_AUX AC7
DDI1_AUX_P AC6
DDI2_AUX AD4
DDI2_AUX_P AD3
DDI3_AUX AG7
DDI3_AUX_P AG6

Port C

Remove DDI2 #2018.08.08

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 — HDMI_HPD <17> **Internal pull-down with 130k ohm**
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 — Remove DP_HDP #2018.08.28
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 — KBSMI# <18>
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 — KBSCI# <18>
GPP_E17/EDP_HPD/DISP_MISC4 CM7 — EDP_HPD <16>

KBSMI#/SCI#
Follow MS-N1131

EDP_BKLTEN CK11 — EDP_BKLT_EN <18>
EDP_VDDEN CG11 — EDP_VDDEN <16>
EDP_BKLTCTL CH11 — EDP_BKLTCTL <16>

+VCC_IO
R359 24.9R1%0402 DISP_RCOMP AM6 — DISP_RCOMP

Pull up on level shift page

<17> DDI1_CTRL_CLK — CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
<17> DDI1_CTRL_DATA — CC9 GPP_E19/DPPB_CTRLDATA

Port B
Port C

CH4 GPP_E20/DPPC_CTRLCLK
CH3 GPP_E21/DPPC_CTRLDATA

Remove DDI2 #2018.08.28

R64 100KR0402 — R74 100KR0402 — R98 100KR0402

Remove DP_HDP Pull-Down #2018.08.28

CP4 GPP_E22/DPPD_CTRLCLK
CN4 GPP_E23/DPPD_CTRLDATA

CR26 GPP_H16/DDPF_CTRLCLK
CP26 GPP_H17/DDPF_CTRLDATA

WHL-i7-8565U 1 of 20
A0D-8565U05-I06

CPU2 — CPU — X_WHL-U_i5-8265U — OAC-13G3001-I06
CPU3 — CPU — X_WHL-U_i7-8565U — OAD-13G3001-I06
CPU5 — CPU — X_WHL-U_i3-8145U — OAB-13M1001-I06

CPU6 — CPU — X_WHL-U_i7-8565U — A0D-8565U05-I06

CPU4 — CPU INTERPOSER — X_WHISKEY LAKE,CPU INTERPOSER — OS1-16S1001-I06

MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U(EDP,DDI)

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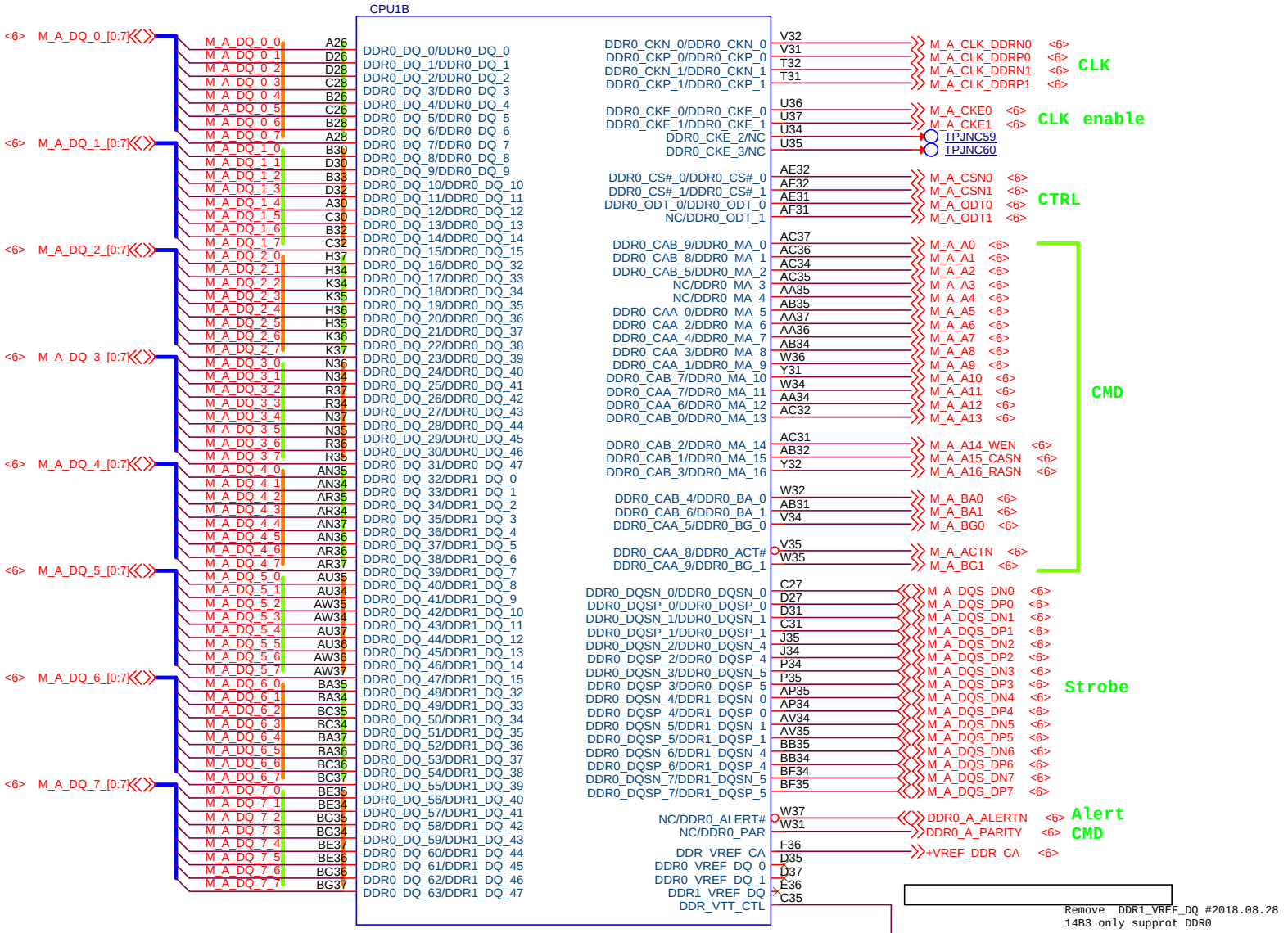
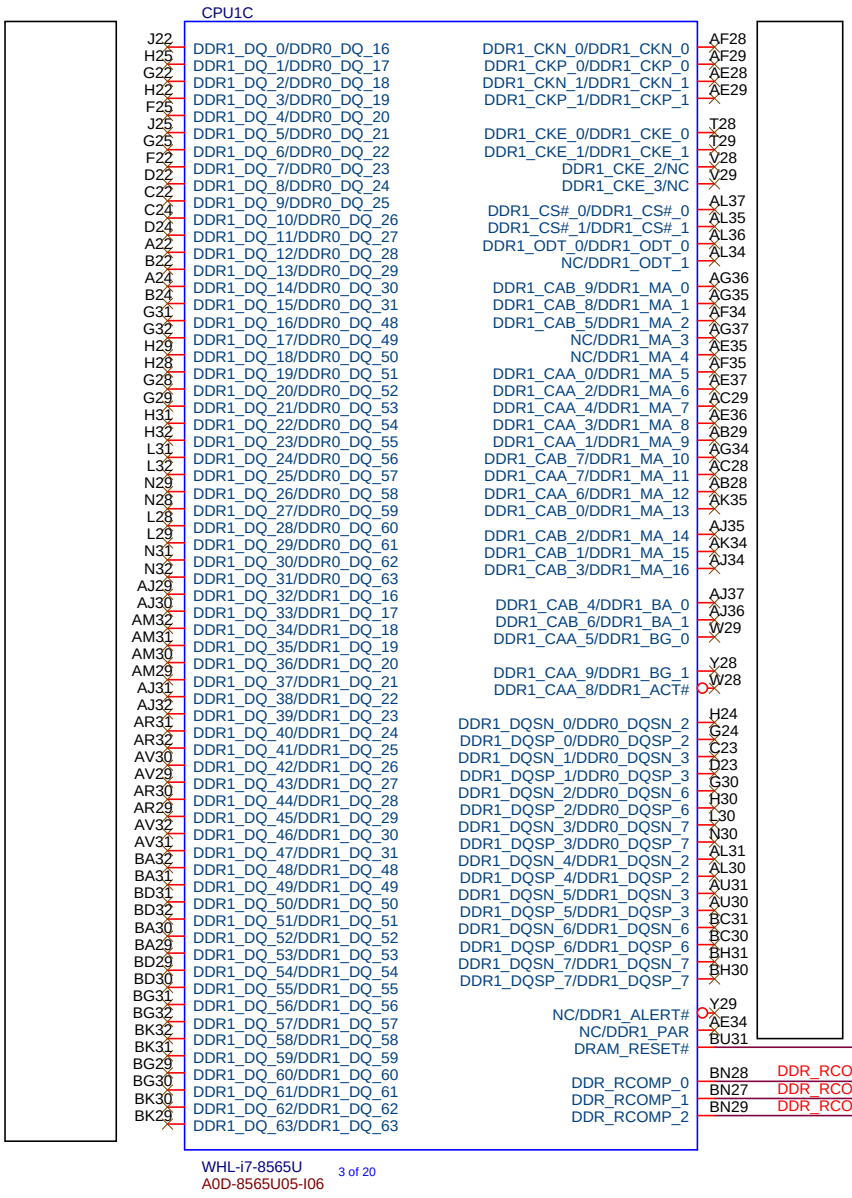
SODIMM_A

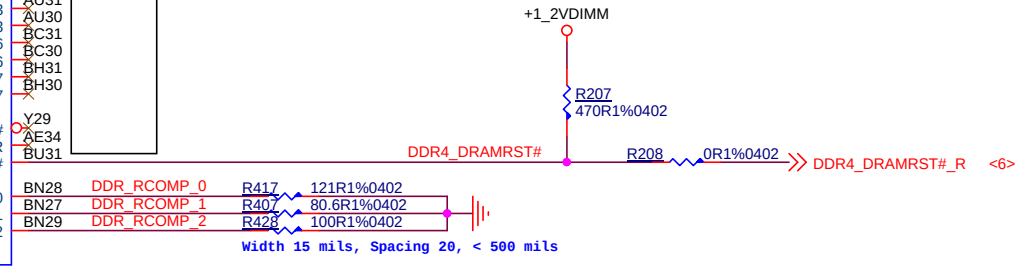


MSI	MICRO-STAR INT'L CO.,LTD.	
Title	Whiskey lake (DDR4)CHA	
Size: Custom	Document Number: MS-14B3	Rev: 0A
Date: Friday, November 16, 2018	Sheet 4 of 57	

SODIMM_B



Remove DDR1 #2018.08.28
14B3 only supprot DIMMA



MICRO-STAR INT'L CO.,LTD.

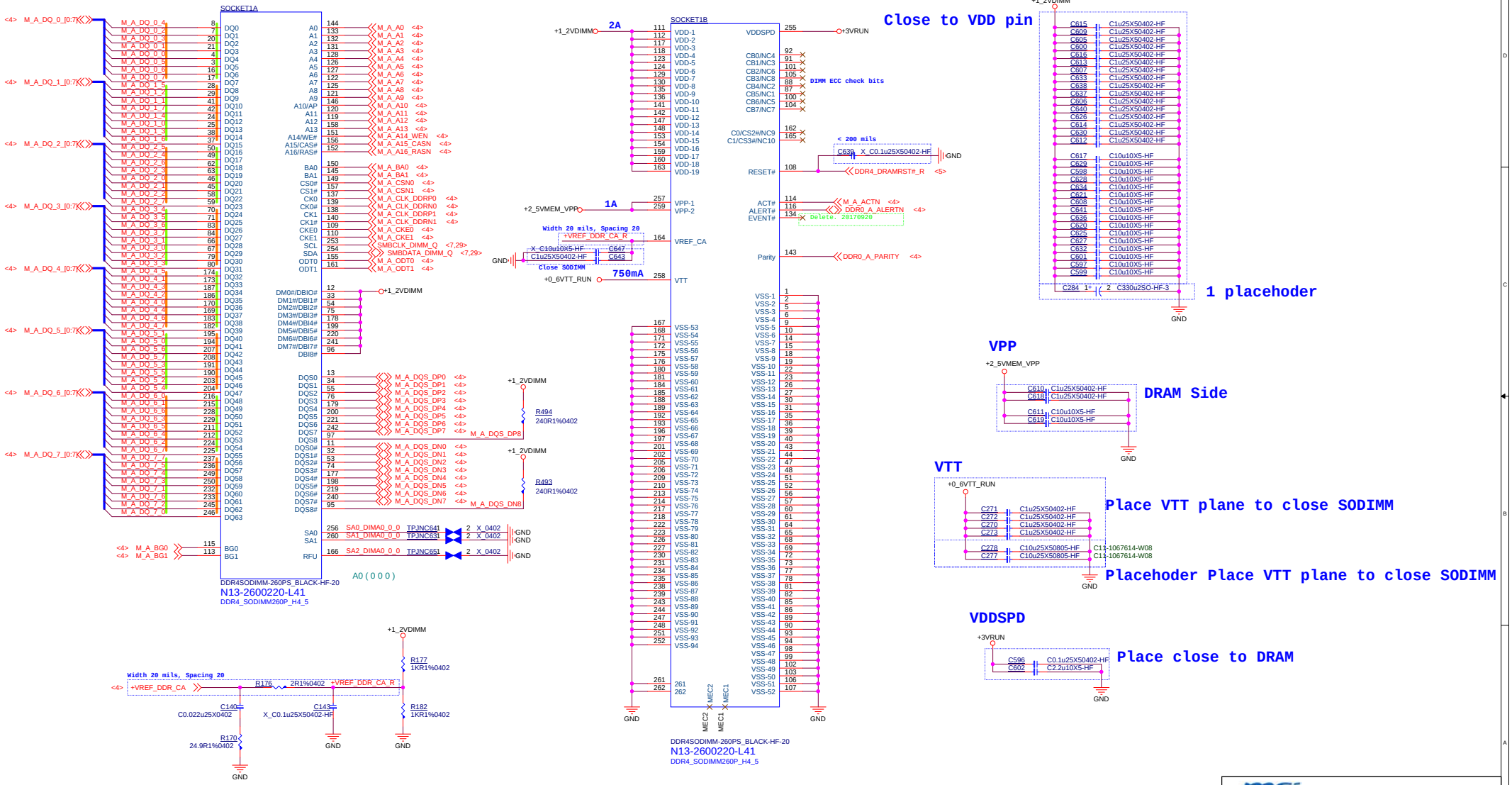
Title: Whiskey lake (DDR4)CHB

Size: Custom | Document Number: MS-14B3 | Rev: 0A

Date: Friday, November 16, 2018 | Sheet 5 of 57

SODIMM_A DDR4 SODIMM Interleave (IL)

Follow 14B1 to change location for placement #2018.08.22



MSI	MICRO-STAR INT'L CO.,LTD.
Title	DDR4_SODIMM_A
Size: Custom	Document Number: MS-14B3
Rev	0A
Date: Friday, November 16, 2018	Sheet 6 of 57

Reference 16S1

+3VRUN
R431 10KR1%0402 PCIE_CLK_SSD_REQ#
R125 10KR1%0402 GPU_CLKREQ#
R416 10KR1%0402 PCIE_CLK_WLAN_REQ#
Add WLAN REQ# for WLAN #2018.08.28

CPU1J 100Mhz
AW2 CLKOUT_PCIE_N0
AY3 CLKOUT_PCIE_P0
CF32 GPP_B5/SRCCLKREQ0#
BC1 CLKOUT_PCIE_N1
BC2 CLKOUT_PCIE_P1
CE32 GPP_B6/SRCCLKREQ1#
BD3 CLKOUT_PCIE_N2
BC3 CLKOUT_PCIE_P2
CF30 GPP_B7/SRCCLKREQ2#
BH3 CLKOUT_PCIE_N3
BH4 CLKOUT_PCIE_P3
CE31 GPP_B8/SRCCLKREQ3#
BA1 CLKOUT_PCIE_N4
BA2 CLKOUT_PCIE_P_4
CE30 GPP_B9/SRCCLKREQ4#
BE1 CLKOUT_PCIE_N5
BE2 CLKOUT_PCIE_P5
CE31 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL_IN
XTAL_OUT
XCLK_BIASREF
CLKIN_XTAL
RTCX1
RTCX2
SRTCRST#
RTCRST#
WHL-i7-8565U 10 of 20
A0D-8565U05-I06

Remove CLKOUT #2018.08.28
Add CLK for WLAN #2018.08.28
WLAN
<20> CLKOUT_PCIEN_WLAN
<20> CLKOUT_PCIEP_WLAN
<20> PCIE_CLK_WLAN_REQ#
GPU
<33> GFX_REFCLK#
<33> GFX_REFCLK
<33> GPU_CLKREQ#
COMBO SSD
<19> CLKOUT_PCIEN_SSD
<19> CLKOUT_PCIEP_SSD
<19> PCIE_CLK_SSD_REQ#

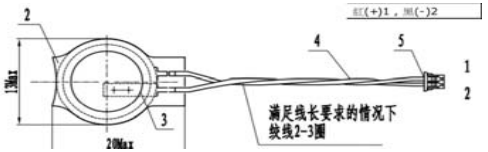
Debug port
AU1 CLKOUT_ITP#
AU2 CLKOUT_ITP
TPJNC8
TPJNC4
Add SUSCLK_WLAN to M.2 WLAN #2018.08.28
BT32 SUSCLK
SUSCLK_WLAN <20>
CK3 XTAL24_IN
CK2 XTAL24_OUT
R51 0R0402
R55 0R0402
Add 0 ohm close to PCH
CJ1 XCLK_BIASREF R48 60.4R1%0402
CM3 CLKIN_LCP
CLKIN_LCP <20>
XCLK_BIASREF change form PU to 60.4 ohm PD
Add CNVi function
BN31 RTC_X1
BN32 RTC_X2
BR37 SRTC_RST_N
BR34 RTC_RST_N
20KR1%0402 R467
20KR1%0402 R451
RTCVCC
C567 C1u25X50402-HF
C581 C1u25X50402-HF

Resistor form 1M ohm to 200K ohm
XTAL24_IN_R
C60 C12p50N0402
R52 200KR1%0402
Y1 24MHZ12p_S-HF-8 D04-3904000-SC6
XTAL24_OUT_R
C62 C12p50N0402
C3.9p50N0402 C580
R463 10MR1%0402
Y3 32.768KHZ7p_S-HF-2 D04-0307000-C11 OSC_3_2X1_5_1
C3.9p50N0402 C584
Follow PDG change BIAS R from 10M 5% to 10M 1% #2018.08.23
2018.05.30 Update Crystal 24M component (<30 ohm)
0B. Change C580 & C584 from 4.7pF to 3.9pF(C11-39A1822-W08) by Vender matching report #2018.11.12

+3VRUN
SMBCLK_DIMM_Q R129 2.2KR1%0402
SMBDATA_DIMM_Q R114 2.2KR1%0402
+3VSUS
SMBCLK_DIMM R103 2.2KR0402
SMBDATA_DIMM R118 2.2KR0402
SMBALERT# R113 X 4.7KR0402
SML1ALERT# R447 X 4.7KR0402
SML0ALERT# R89 X 4.7KR0402
RN1 8P4R-2.2KR0402
SML0_CLK 1 2
SML0_DATA 3 4
SMB_CLK_R 5 6
SMB_DATA_R 7 8
SMBCLK_DIMM_Q EC9 X C100p50N0402
SMBDATA_DIMM_Q EC7 X C100p50N0402
SMBCLK_DIMM EC6 X C100p50N0402
SMBDATA_DIMM EC8 X C100p50N0402
SML0ALERT# R90 X 20KR1%0402
CLKIN_LCP R59 10KR0402
close to SOC
2018.05.29 Change CLKIN_LCP PD resistor to PCH side

SUS
Q16
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
SMBCLK_DIMM D1 S1 G1 SMBCLK_DIMM_Q <6,29>
SMBDATA_DIMM D2 S2 G2 SMBDATA_DIMM_Q <6,29>
RUN
Vgs(th) = 0.5, 1.2, 1.5V
ID = 0.2A
C114 C0.1u25X50402-HF GND
+3VRUN

+3VALW
R248 1.5KR0402
+3VALW_R
R243 X_45.3KR1%0402
GND
Follow 16S1 0B add discharge circuit on SRTC_RST & RTC_RST #2018.09.13
R512 & R246 place on CPU side and close ball out
SRTC_RST_N R512 0R0402 D1
RTC_RST_N R246 0R0402
R253 X 0R0402 D2
Vgs(th) = 0.5, 1.2, 1.5V
ID = 0.2A
Q30
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
S1 G1 S2 G2 GND GND
EC_RTC_RST <18>
R240 100KR1%0402
RTCVCC
GND
D5 S-BAT54C_SOT23
D4 S-BAS40WS_SOD323-RH
D01-BAS4000-P15
DIODE_SOD323
+RTC_D
+RTC_R
C174 C1u25X5-HF
GND
R247 1KR1%0402
+RTC
CON7
BH1X2#S-1.25PITCH_BLACK-HF
N32-10200Q0-A81
SD_53261_0210_2P
BAT1
BCR1220H2
D06-0105701-K26
Follow 14B1



+3VSUS
Strap Pin require
R157 100KR0402
Add CS Pin PU
R139 10KR0402
C118 C0.1u25X50402
R154 100KR0402
R175 100KR0402
U12
SPI_CS0# 1 CS VCC 8
SPI_MISO 2 DO(IO1) HOLD(IO3) 7 SPI_HOLD#_B
SPI_WP# 3 WP(IO2) CLK 6 SPI_CLK
GND 4 DI(IO0) 5 SPI_MOSI
W25Q128JVSIQ-HF
M31-2512893-W03
ROM from 8M change to 16MB
0B. Remove BIOS ROM socket & place BIOS ROM M31-2512893-W03 #2018.11.09

SPI_CLK_R R145 100KR0402
For glitch free implementation requirements

SPI resistance form 15ohm change to 49.9ohm
EC11 X_C10p50N0402
SPI_CLK R149 49.9R1%0402 SPI_CLK_R
SPI_MISO R171 49.9R1%0402 SPI_MISO_R
SPI_MOSI R174 49.9R1%0402 SPI_MOSI_R
SPI_WP# R156 49.9R1%0402 SPI_WP#_R
SPI_HOLD#_B R153 49.9R1%0402 SPI_HOLD#_B_R
SPI_CS0#
<18> SPI_CLK
<18> SPI_CS0#
<18> SPI_MISO
<18> SPI_MOSI

CPU1E
SPI0_CLK CH37
SPI0_MISO CF37
SPI0_MOSI CF36
SPI0_IO2 CF34
SPI0_IO3 CG34
SPI0_CS0# CG36
SPI0_CS1# CG35
SPI0_CS2# CH34
GPP_D1/SPI1_CLK/BK1/SBK1
GPP_D2/SPI1_MISO_IO1/BK2/SBK2
GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
GPP_D21/SPI1_IO2 CF23
GPP_D22/SPI1_IO3 CG23
GPP_D0/SPI1_CS0#/BK0/SBK0 CG20
CL_CLK CH7
CL_DATA CH8
CL_RST# CH9
GPP_A0/RCIN#/TIME_SYNC1 BV29
GPP_A6/SERIRQ BV28
WHL-i7-8565U
A0D-8565U05-I06
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Remove SMBCLK_DIMM & SMBDATA_DIMM off-page #2018.08.28
GPP_C0/SMBCLK CK14 SMBCLK_DIMM
GPP_C1/SMBDATA CH15 SMBDATA_DIMM
GPP_C2/SMBALERT# CJ15 SMBALERT#
GPP_C3/SML0CLK CH14 SML0_CLK
GPP_C4/SML0DATA CF15 SML0_DATA
GPP_C5/SML0ALERT# CG15 SML0ALERT#
GPP_C6/SML1CLK CN15 SMB_CLK_R
GPP_C7/SML1DATA CM15 SMB_DATA_R
GPP_B23/SML1ALERT#/PCHHOT# CC34 SML1ALERT#
NOT used
SML1ALERT# : (eSPI/LPC):This signal has a weak internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
SML0ALERT# : (eSPI/LPC):This signal has a weak internal pull-down.
0 = LPC is selected for EC (Default) ;
1 = eSPI is selected for EC

Follow PDG resistor can be up to 22 ohm
GPP_A1/LAD0/ESPI_IO0 CA29 LPC_AD0_R R472 22R0402 LPC_AD0
GPP_A2/LAD1/ESPI_IO1 BY29 LPC_AD1_R R475 22R0402 LPC_AD1
GPP_A3/LAD2/ESPI_IO2 BV27 LPC_AD2_R R457 22R0402 LPC_AD2
GPP_A4/LAD3/ESPI_IO3 BV27 LPC_AD3_R R480 22R0402 LPC_AD3
GPP_A5/LFRAME#/ESPI_CS# CA28 LPC_FRAME#_R R460 22R0402 LPC_FRAME#
GPP_A14/SUS_STAT#/ESPI_RESET# CA27 SUS_STAT#
TPJNC50
GPP_A9/CLKOUT_LPC0/ESPI_CLK BV32 CLKOUT_PCI0 R185 22R1%0402 CLK_PCI_KBC <18>
GPP_A10/CLKOUT_LPC1 BV30 CLKOUT_BLF R465 22R1%0402 CLK_PCI_TPM <23>
GPP_A8/CLKRUN# BV30 EC_CLKRUN# <18>
LPC_AD0 <18,23>
LPC_AD1 <18,23>
LPC_AD2 <18,23>
LPC_AD3 <18,23>
LPC_FRAME# <18,23>
CLK_PCI_TPM <23>

LPC_FRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
EC43 EC44 EC40 EC45 EC41 X_C10p50N0402
Can be up to 27pF
Follow PDG(P.294) reserve capacitor to GND for EMI issue #2018.08.15

+3VRUN
R479 10KR0402
<18,23> SERIRQ
<18> KBRST#
EC_CLKRUN# R190 8.2KR0402
EC12 EC42 X_C10p50N0402

MICRO-STAR INT'L CO.,LTD.
Title: Whiskey lake U (RTC;LPC;CLOCK)
Size: Custom
Document Number: MS-14B3
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Reference 16S1

follow 13H1 reserve MB ID[0:3] #2018.08.10

+3VRUN

MB_ID0 R411 X_10KR0402
MB_ID1 R456 X_10KR0402
MB_ID2 R423 X_10KR0402
MB_ID3 R430 X_10KR0402

MB_ID0 R412 10KR0402
MB_ID1 R441 10KR0402
MB_ID2 R422 10KR0402
MB_ID3 R429 10KR0402

MB_ID2 CC27
PIRQA# CC32
MB_ID3 CE28
MB_ID0 CE27
CE29

MB_ID1 CA31
TPJNC53 PME# CA32
CC29
CC30
CA30

CPU1F

GPP_B15/GSPI0_CS0#
GPP_A7/PIRQA#/GSPI0_CS1#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI

GPP_B19/GSPI1_CS0#
GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI

CK20
GPP_F5/CNV_BRI_RSP CG19
GPP_F6/CNV_RGI_DT CJ20
GPP_F4/CNV_BRI_DT CH19
GPP_F7/CNV_RGI_RSP

1.8V

<20> CNVI_BRI_RSP
<20> CNVI_RGI_DT
<20> CNVI_BRI_DT
<20> CNVI_RGI_RSP

R438 33R0402 CNVI_RGI_DT_R
R437 33R0402 CNVI_BRI_DT_R

Follow MOW Table 5-1 change R7042 & R7034 from 75 to 33ohm #2018.08.29

CR12
CP12
CN12
CM12

GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#

SMI# / NMI

Remove USB-SMI# #2018.08.28

I2C_DATA_TP CM11
I2C_CLK_TP CN11

GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL

Remove TP_INT# #2018.08.28

CK12
CJ12

GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL

CF27
CF29

GPP_H4/I2C2_SDA
GPP_H5/I2C2_SCL

CH27
CH28

GPP_H6/I2C3_SDA
GPP_H7/I2C3_SCL

CJ30
CJ31

GPP_H8/I2C4_SDA
GPP_H9/I2C4_SCL

GPU

<40> GPIO2_GPU_EVENT_PCH
<40,41> GPIO1_GC6_FB_EN
Change netname to GPIO1_GC6_FB_EN #2018.08.28
<18,33,41> DGPU_PWRGD
<40> DGPU_HOLD_RST#
<41> DGPU_PWR_EN

TPJNC52
TPJNC20

3.3V

Active HI

GND R435 100KR1%0402
GND R126 100KR1%0402

Follow 14B1 reserve R657 for CFG_UMA sku. #2018.08.10

WHL-i7-8565U
A0D-8565U05-I06

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CN22
CR22
CM22
CP22

GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI

GPP_D10 TPJNC16
GPP_D12

Follow PDG DCI OOB implementation

CK22
CH20

GPP_D5/ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL

CH22
CJ22

GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL

CJ27
CJ29

GPP_H10/I2C5_SDA/ISH_I2C2_SDA
GPP_H11/I2C5_SCL/ISH_I2C2_SCL

GPP_H10 TPJNC22
GPP_H11 TPJNC51

CM24
CN23
CM23
CR24

GPP_D13/ISH_UART0_RXD
GPP_D14/ISH_UART0_TXD
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#
GPP_D16/ISH_UART0_CTS#/SML0BALERT#

CG12
CH12
CF12
CG14

GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#

BW35
BW34
CA37
CA36
CA35
CA34
BW37

GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#

+3VSUS

I2C_CLK_TP R78 2.2KR0402
I2C_DATA_TP R73 2.2KR0402

Remove USB-SMI# & TP_INT# PU #2018.08.28

GPP_D12 R96 100KR0402

+3VRUN

I2C_CLK_TP_Q R67 2.2KR0402
I2C_DATA_TP_Q R66 2.2KR0402

Remove USB-SMI# & TP_INT# PU #2018.08.28

I2C_CLK_TP_Q EC5 X_C100p50N0402
I2C_DATA_TP_Q EC4 X_C100p50N0402

Remove USB-SMI# & TP_INT# Cap to GND #2018.08.28

GND
+1_8VSUS

CNVI_BRI_RSP R400 X_20KR0402-2
CNVI_RGI_RSP R391 X_20KR0402-2

DT resistance close to module
RSP resistance close to SOC

2018.06.14 PCIE_WAKE# signal follow CRB Pull up 8.2k ohm
2018.06.14 Del PM_SLP_S0# and EXT_PWR_GATE# pull up resistor
Becasue function pin is output pin and isn't be used

+3VSUS

For glitch free implementation requirements

PCIE_WAKE# R464 8.2KR0402

Change R7051 from 10k to 4.7k #2018.08.24
SOC Internal Pull Down 15k~40k ohm

AC_PRESENT R454 4.7KR0402
PM_BATLOW# R462 8.2KR0402

EC_PWRBTN# R217 X_10KR0402

2018.06.13 Del SUSPWRDNACK pull up resistor for PDG suggest

+3VRUN

PIRQA# R425 10KR0402

RSMRST# R459 10KR0402
PCH_PWROK R478 10KR0402
AC_PRESENT R455 X_100KR0402

For glitch free implementation requirements

PM_SLP_S3# R200 100KR0402
PM_SLP_S4# R184 100KR0402

Remove level shift

Q11
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363

SUS

I2C_CLK_TP D1
I2C_DATA_TP D2

S1
G1
S2
G2

RUN

I2C_CLK_TP_Q I2C_CLK_TP_Q <29>
I2C_DATA_TP_Q I2C_DATA_TP_Q <29>

Vgs(th) = 0.5V,1.2V,1.5V

C87 C0.1u25X50402-HF GND
+3VRUN

CPU1K

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#

PROCPWRGD
VCCST_PWRGOOD

SYS_PWROK
PCH_PWROK
DSW_PWROK

GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#

WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC

GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#

SLP_SUS#
SLP_LAN#
GPD9/SPI_WLAN#
GPD6/SLP_A#

GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#

INTRUDER#

GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#

INPUT3VSEL

PLT_RST# BJ35
SYS_RESET#_JNC CN10
BR36

+3VRUN R75 10KR0402
<18> RSMRST#

TPJNC3 PROCPWRGD AR2
VCCST_PWRGD BJ2

<18> SYS_PWROK R76 0R0402 CR10
<18> PCH_PWROK R471 0R0402 BP31
DSW_PWROK BP30

Follow 14B1 add SUS_PWR_ACK #2018.08.28

TPJNC30 SUS_PWR_ACK BV34
<18> SUS_PWR_ACK BY32

<20> WLAN_WAKE# R468 0R0402 PCIE_WAKE# BU30
BU32
BU34

Follow 14B1 add WLAN_WAKE# #2018.08.28

R204 61.9KR1%0402-RH

For glitch free implementation requirements

DSWROK can be tied to RSMRST# for platforms that dose not support the Deep Sx state.

DSW_PWROK R458 0R0402 RSMRST#

BJ37 PM_SLP_S0#
BU36 PM_SLP_S3#
BU27 PM_SLP_S4#
BT29 PM_SLP_S5# R439 0R0402

TPJNC29

PM_SLP_S3# <18,46>
PM_SLP_S4# <18,45,47>
PM_SLP_S5# <18>

Remove SLP_S0# function, 14B3 did not support #2018.08.09

Follow 13H1 add SLP_S5# to EC #2018.08.28

BU29
BT31
BT30
BU37

BU28 EC_PWRBTN#
BU35 AC_PRESENT
BV36 PM_BATLOW#

EC_PWRBTN# <18>
AC_PRESENT <18>

Change PM_PWRBTN# to EC_PWRBTN# #2018.08.28

BR35 SM_INTRUDER_N 1MR0402 R466

RTCVCC
+3VSUS

CC37 EXT_PWR_GATE#
CC36

TPJNC57

R469 X_4.7KR0402

BT27 INPUT3VSEL

R470 4.7KR0402

2018/01/30 3V Select Strap
Low ->3.3V +-5%
High -> 3.0V +-5%

WHL-i7-8565U
A0D-8565U05-I06

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+3VSUS
C0.1u25X50402 C163

U16
74HC1G08GW_TSSOP5-HF

<18,19,23,40> BUF_PLT_RST#

R198 100KR0402

Follow 14B1 add WLAN_RST to GPU #2018.08.28

+3VSUS
C0.1u25X50402-HFC165
GND

<20> WLAN_RST#

R218 100KR1%0402

U17
NL17SZ08DFT2G_SC70-5-HF
T70-7SZ0870-O05
SC70_5

EC_WLAN_RST# <18>

GND

+3VSUS
+VCCST

C45 C0.1u25X50402

R38 1KR0402

U3
74AHC1G07GW_SOT353-RH

<18,48> EC_ALLSYSPG

VCCST_PWRGD_R R42 60.4R1%0402 VCCST_PWRGD

2018.06.13 VCCST_PWRGD of signal add series resistor to follow PDG suggest

MSI MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U (LPSS;ISH;I2C)

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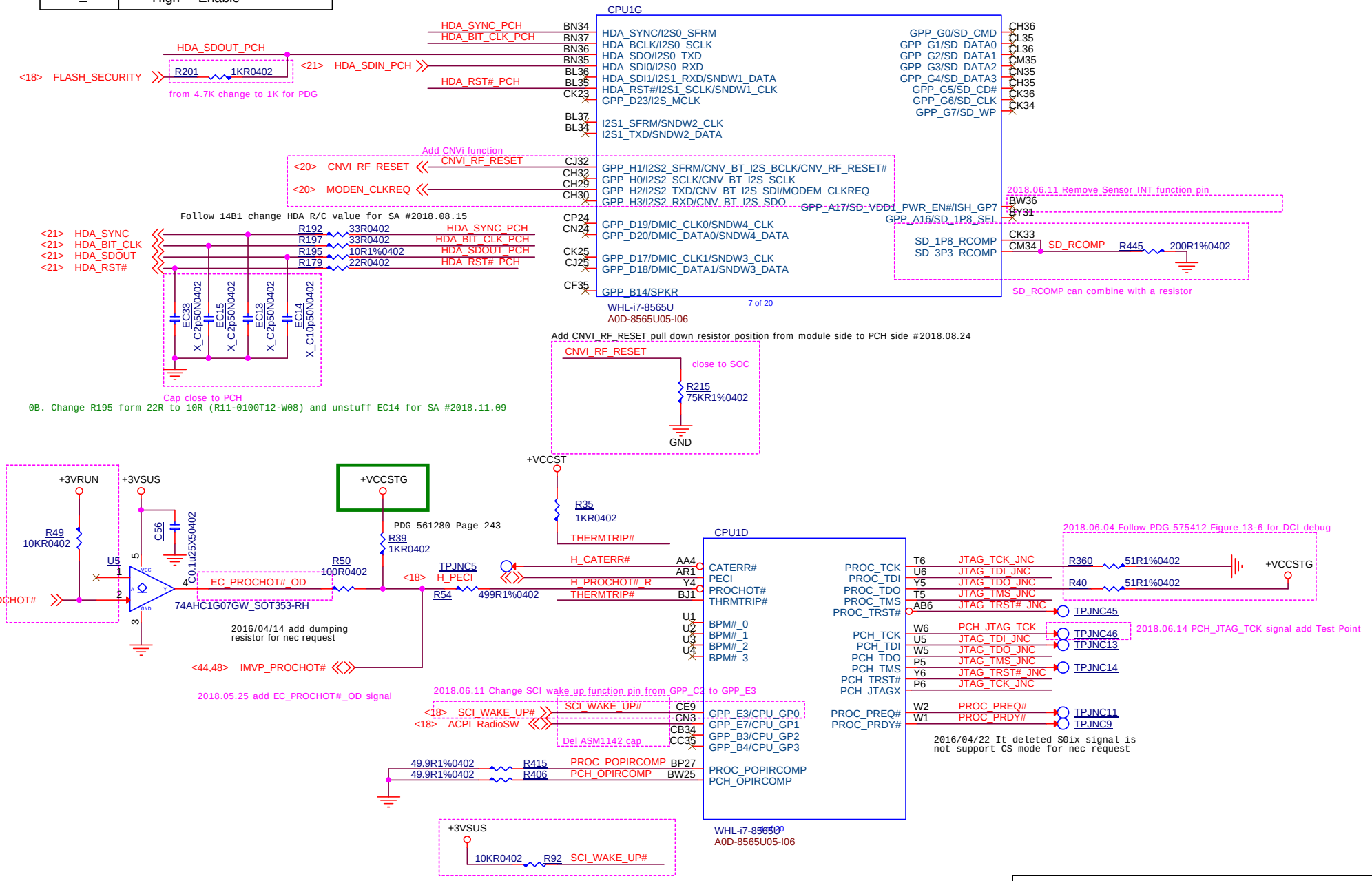
Reference 16S1

Flash Descriptor Security Override	
HDA_SDO	Low = Disable High = Enable



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Whiskey lake U(HDA;MISC,JTAG)		
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AC coupling capacitors on motherboard are recommended to be placed
closer to either the connector or processor side.
Avoid placing AC caps at the center of the motherboard.

Change to 14B3 configuration #2018.08.28

CPU1H

Change USB3.1 port1/2/3/4 order for layout #2018.09.04

Port5,6 : USB3.1 TypeC Port4

<28> USB3_RXN_TYPEC3 — BW9 PCIE5_RXN/USB31_5_RXN
<28> USB3_RXP_TYPEC3 — BW8 PCIE5_RXP/USB31_5_RXP
<28> USB3_TXN_TYPEC3 — BW4 PCIE5_TXN/USB31_5_TXN
<28> USB3_TXP_TYPEC3 — BW3 PCIE5_TXP/USB31_5_TXP

<28> USB3_RXN_TYPEC4 — BU6 PCIE6_RXN/USB31_6_RXN
<28> USB3_RXP_TYPEC4 — BU5 PCIE6_RXP/USB31_6_RXP
<28> USB3_TXN_TYPEC4 — BU4 PCIE6_TXN/USB31_6_TXN
<28> USB3_TXP_TYPEC4 — BU3 PCIE6_TXP/USB31_6_TXP

Port7 : M.2 WLAN

<20> PCIE_RXN_WLAN — BT7 PCIE7_RXN
<20> PCIE_RXP_WLAN — BT6 PCIE7_RXP
<20> PCIE_TXN_WLAN — BU2 PCIE7_TXN
<20> PCIE_TXP_WLAN — BU1 PCIE7_TXP

BU9 PCIE8_RXN
BU8 PCIE8_RXP
BT4 PCIE8_TXN
BT3 PCIE8_TXP

Port9~12: PCI-E 1 x 4 GPU

<33> PCIE9_RXN — BP5 PCIE9_RXN
<33> PCIE9_RXP — BP6 PCIE9_RXP
<33> PCIE9_TXN — BR2 PCIE9_TXN
<33> PCIE9_TXP — BR1 PCIE9_TXP

<33> PCIE10_RXN — BN6 PCIE10_RXN
<33> PCIE10_RXP — BN5 PCIE10_RXP
<33> PCIE10_TXN — BR4 PCIE10_TXN
<33> PCIE10_TXP — BR3 PCIE10_TXP

<33> PCIE11_RXN — BN10 PCIE11_RXN/SATA0_RXN
<33> PCIE11_RXP — BN8 PCIE11_RXP/SATA0_RXP
<33> PCIE11_TXN — BN4 PCIE11_TXN/SATA0_TXN
<33> PCIE11_TXP — BN3 PCIE11_TXP/SATA0_TXP

<33> PCIE12_RXN — BL6 PCIE12_RXN/SATA1A_RXN
<33> PCIE12_RXP — BL5 PCIE12_RXP/SATA1A_RXP
<33> PCIE12_TXN — BN2 PCIE12_TXN/SATA1A_TXN
<33> PCIE12_TXP — BN1 PCIE12_TXP/SATA1A_TXP

Port13~16/SATA2 : PCI-E SSD

<19> PCIE_RXN_SSD1 — BK6 PCIE13_RXN
<19> PCIE_RXP_SSD1 — BK5 PCIE13_RXP
<19> PCIE_TXN_SSD1 — BM4 PCIE13_TXN
<19> PCIE_TXP_SSD1 — BM3 PCIE13_TXP

<19> PCIE_RXN_SSD2 — BJ6 PCIE14_RXN
<19> PCIE_RXP_SSD2 — BJ5 PCIE14_RXP
<19> PCIE_TXN_SSD2 — BL2 PCIE14_TXN
<19> PCIE_TXP_SSD2 — BL1 PCIE14_TXP

<19> PCIE_RXN_SSD3 — BG5 PCIE15_RXN/SATA1B_RXN
<19> PCIE_RXP_SSD3 — BG6 PCIE15_RXP/SATA1B_RXP
<19> PCIE_TXN_SSD3 — BL4 PCIE15_TXN/SATA1B_TXN
<19> PCIE_TXP_SSD3 — BL3 PCIE15_TXP/SATA1B_TXP

<19> PCIE_SATA_RXN_SSD — BE5 PCIE16_RXN/SATA2_RXN
<19> PCIE_SATA_RXP_SSD — BE6 PCIE16_RXP/SATA2_RXP
<19> PCIE_SATA_TXN_SSD — BJ4 PCIE16_TXN/SATA2_TXN
<19> PCIE_SATA_TXP_SSD — BJ3 PCIE16_TXP/SATA2_TXP

PCIE_RCOMPN — CE6 PCIE_RCOMP
R370 100R1%0402 PCIE_RCOMPP — CE5 PCIE_RCOMP_P

4 mils min (breakout) 12-15 mils (trace)
At least 12 mils to any adjacent high speed I/O.

CR28 GPP_H12/M2_SKT2_CFG0
CP28 GPP_H13/M2_SKT2_CFG1
CN28 GPP_H14/M2_SKT2_CFG2
CM28 GPP_H15/M2_SKT2_CFG3

WHL-i7-8565U
A0D-8565U05-I06
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PCIE1_RXN/USB31_1_RXN — CB5 — USB3_RXN_TYPEC1 <25>
PCIE1_RXP/USB31_1_RXP — CB6 — USB3_RXP_TYPEC1 <25>
PCIE1_TXN/USB31_1_TXN — CA4 — USB3_TXN_TYPEC1 <25>
PCIE1_TXP/USB31_1_TXP — CA3 — USB3_TXP_TYPEC1 <25>

Port3,4 : USB3.1 TypeC Port3

PCIE2_RXN/USB31_2_RXN/SSIC_1_RXN — BY8 — USB3_RXN_TYPEC2 <25>
PCIE2_RXP/USB31_2_RXP/SSIC_1_RXP — BY9 — USB3_RXP_TYPEC2 <25>
PCIE2_TXN/USB31_2_TXN/SSIC_1_TXN — CA2 — USB3_TXN_TYPEC2 <25>
PCIE2_TXP/USB31_2_TXP/SSIC_1_TXP — CA1 — USB3_TXP_TYPEC2 <25>

PCIE3_RXN/USB31_3_RXN — BY7 — USB3_RXN_TYPEA1 <24>
PCIE3_RXP/USB31_3_RXP — BY6 — USB3_RXP_TYPEA1 <24>
PCIE3_TXN/USB31_3_TXN — BY4 — USB3_TXN_TYPEA1 <24>
PCIE3_TXP/USB31_3_TXP — BY3 — USB3_TXP_TYPEA1 <24>

Port1 : USB3.1 TypeA Port1

PCIE4_RXN/USB31_4_RXP — BW6 — USB3_RXN_TYPEA2 <24>
PCIE4_RXP/USB31_4_RXP — BW5 — USB3_RXP_TYPEA2 <24>
PCIE4_TXN/USB31_4_TXN — BW2 — USB3_TXN_TYPEA2 <24>
PCIE4_TXP/USB31_4_TXP — BW1 — USB3_TXP_TYPEA2 <24>

Port2 : USB3.1 TypeA Port2

USB2N_1 — CE3 — USB2N_TYPEA1 <24>
USB2P_1 — CE4 — USB2P_TYPEA1 <24>

Port1 : USB3.1 TypeA Port1

USB2N_2 — CE1 — USB2N_TYPEA2 <24>
USB2P_2 — CE2 — USB2P_TYPEA2 <24>

Port2 : USB3.1 TypeA Port2

USB2N_3 — CG3 — USB2N_TYPEC1 <27>
USB2P_3 — CG4 — USB2P_TYPEC1 <27>

Port3 : USB3.1 TypeC Port3

USB2N_4 — CD3 — USB2N_TYPEC2 <28>
USB2P_4 — CD4 — USB2P_TYPEC2 <28>

Port4 : USB3.1 TypeC Port4

USB2N_5 — CG5 — USB2N_CardReader <22>
USB2P_5 — CG6 — USB2P_CardReader <22>

Port5 : Card reader

USB2N_6 — CC1 — USB2N_FP <29>
USB2P_6 — CC2 — USB2P_FP <29>

Port6 : Finger printer

USB2N_7 — CG8 — USB2N_CAMERA <31>
USB2P_7 — CG9 — USB2P_CAMERA <31>

Port7 : Camera

USB2N_8 — CB8
USB2P_8 — CB9

USB2N_9 — CH5
USB2P_9 — CH6

USB2N_10 — CC3 — USB2N_BT <20>
USB2P_10 — CC4 — USB2P_BT <20>

Port10: M.2 BT

USB2_COMP — CC5 USB2_RCOMP R356 113R1%0402
USB_ID — CE8
USB_VBUSSENSE — CC6 USB2_VBUSSENSE R381 1KR0402

+3VSUS

GPP_E9/USB2_OC0#/GP_BSSB_CLK — CK6 USB2_OC0# R68 0R1%0402 — OC0# <24> — USB2_OC0# R69 10KR1%0402
GPP_E10/USB2_OC1#/GP_BSSB_DI — CK5 USB2_OC1# R72 0R1%0402 — OC1# <24> — USB2_OC1# R71 10KR1%0402
GPP_E11/USB2_OC2# — CK8 USB2_OC2# R81 0R1%0402 — OC2# <27> — USB2_OC2# R80 10KR1%0402
GPP_E12/USB2_OC3# — CK9 USB2_OC3# R84 0R1%0402 — OC3# <28> — USB2_OC3# R83 10KR1%0402

Follow 14B1 add OC[0:3]# funciton #2018.08.28

GPP_E4/DEVSLP0 — CP8
GPP_E5/DEVSLP1 — CR8
GPP_E6/DEVSLP2 — CM8 — DEVSLP2_SSD <19>

Remove DEVSLP0 #2018.08.28

GPP_E0/SATAXPCIE0/SATAGP0 — CN8
GPP_E1/SATAXPCIE1/SATAGP1 — CM10
GPP_E2/SATAXPCIE2/SATAGP2 — CP10 — SSD_CFG <19>

GPP_E8/SATALED#/SPI1_CS1# — CN7

SATAXPCIE0 -> SATA Port 0
SATAXPCIE1 -> SATA Port 1
SATAXPCIE2 -> SATA Port 2

RSVD_1/FS_RESET#/RSVD_1 — AR3

Note.
The OC0# is USB3 Port 1, USB2 Port 1
The OC1# is USB3 Port 2, USB2 Port 2
The OC2# is USB3 Port 3,4, USB2 Port 3
The OC3# is USB3 Port 5,6, USB2 Port 4

Reference 16S1

MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U(PCIE;USB;SATA)

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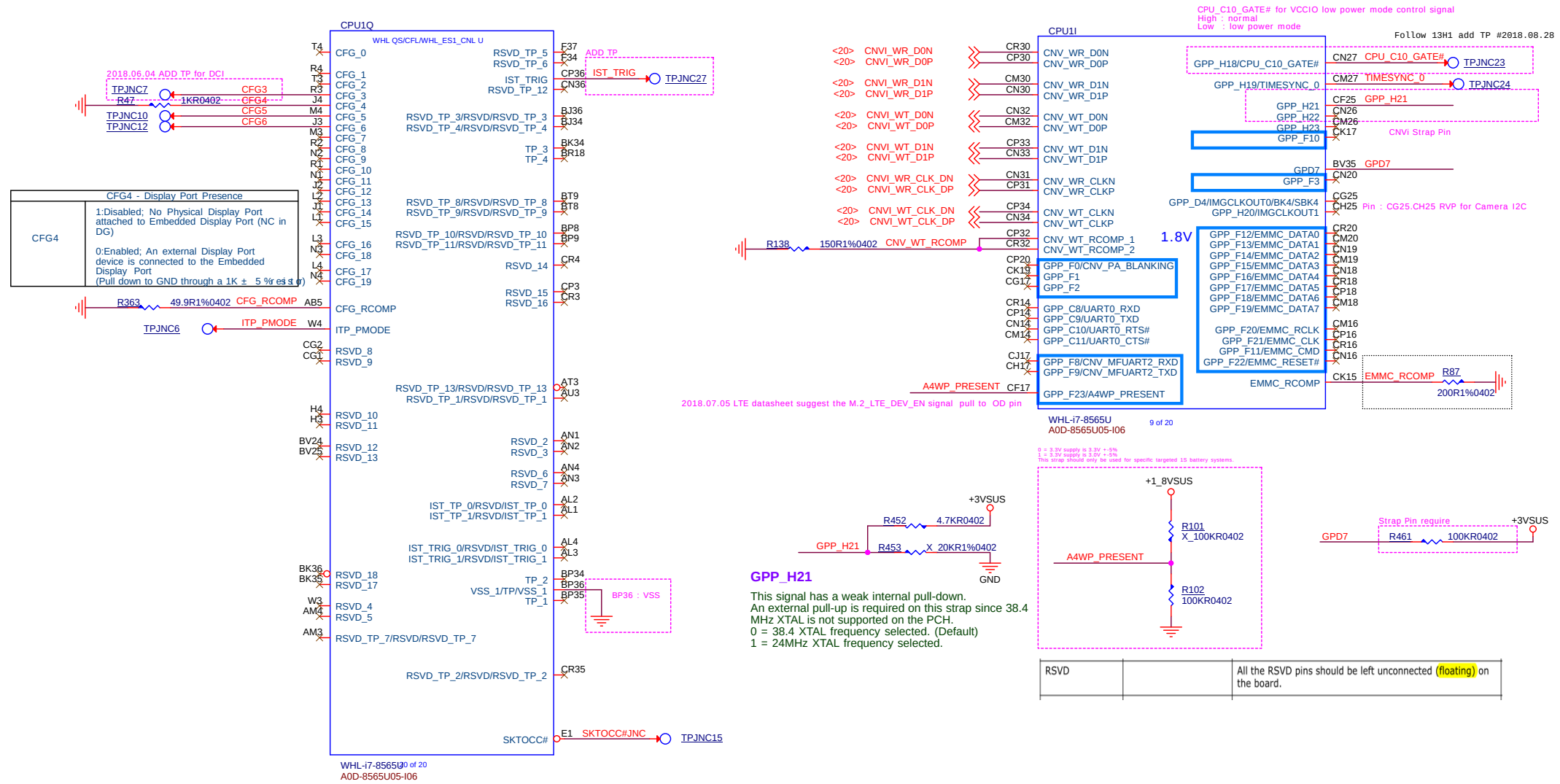

Reference 16S1

MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U (CFG;CSI;RSVD)

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Reference 16S1

22x10 uf 0402 ZRB15XR60J106ME12D

70A

18x47uf 0603 ZRB18AR60G476ME01L

9x22uf 0603 ZRB18AR60J226ME01L

42x1uf 0201

1x22 uf 0603
9x10 uf 0402
4x1 uf 0201

NA

6x10 uF 0402
4x1 uf 0201
4x 0402 reserve

4A

0.12A

0.06A

0.02A

0.12A

0.13A

6A

2x47 uf 0805
13x10uf 0402
7x1uf 0201
2x0805 reserve
4x0402 reserve

Refer to PDG 575412 Table 11-2

Domain	Primary side cap	Secondary Side cap
VCC	8x10uF 0402	42x1uF 0201 14x10uF 0402 9x22uF 0603
	18x47uF 0805	
VCCSA	6x10uF 0402 2x47uF 0805 2x0805	7x10uF 0402 4x0402
VCCIO	4x1uF 0201 4x0402	
	6x10uF 0402	
VDDQ	1x22uF 0603 6x10uF 0402	4x1uF 0201 3x10uF 0402

Add Reserve Cap, refer to PDG 575412 Table 11-2 #2018.08.23

Add Reserve Cap, refer to PDG 575412 Table 11-2 #2018.08.23

2018.06.11 Refer to PDG 575412 Table 11-2

2015/07/01 Follow NEC +VCCST design rule 4-2-39 SVID

2015/07/01 Follow NEC design rule 4-2-39 SVID

EDS 544924 7.1:In case of direct connection (VCCpll_oc is shorted to VDDQ,no laod switch),platform should ensure that VCCst is ON while VCCpll_oc is ON.

Remove RUN_ON_C10 & SLP_S0# control, 14B3 did not support #2018.08.09
Follow 13H1 add RUN_ON control

MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U (CPU POWER)

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ZRB18AR60G476ME01L
ZRB18AR60J226ME01L

4x47 uf 0603
15x22 uf 0603

ZRB15XR60J106ME12D

Reference 16S1

+VCC_GT

31A

CPU1M

WHL QS/CFL/WHL_ES1_CNL U

C408 C405 C450 C407 C70 C409 C459 — C22u6.3X

C526 C69 C71 C72 C441 C404 C406 C531 — C22u6.3X

2018.06.11 Refer to PDG 575412 Table 11-2

C529 C527 C528 C473 — C47u4X

A5	VCCGT_1	VCCGT_60	H12
A6	VCCGT_2	VCCGT_61	H14
A8	VCCGT_3	VCCGT_62	H15
A11	VCCGT_4	VCCGT_63	H17
A12	VCCGT_5	VCCGT_64	H18
A14	VCCGT_6	VCCGT_65	H20
A15	VCCGT_7	VCCGT_66	J7
A17	VCCGT_8	VCCGT_67	J8
A18	VCCGT_9	VCCGT_68	J11
A20	VCCGT_10	VCCGT_69	J14
B3	VCCGT_11	VCCGT_70	J17
B4	VCCGT_12	VCCGT_71	J20
B6	VCCGT_13	VCCGT_72	K2
B8	VCCGT_14	VCCGT_73	K11
B11	VCCGT_15	VCCGT_74	L7
B14	VCCGT_16	VCCGT_75	L8
B17	VCCGT_17	VCCGT_76	L10
B20	VCCGT_18	VCCGT_77	M9
C2	VCCGT_19	VCCGT_78	N7
C3	VCCGT_20	VCCGT_79	N8
C6	VCCGT_21	VCCGT_80	N9
C7	VCCGT_22	VCCGT_81	N10
C8	VCCGT_23	VCCGT_82	P2
C11	VCCGT_24	VCCGT_83	P8
C12	VCCGT_25	VCCGT_84	R9
C14	VCCGT_26	VCCGT_85	T8
C15	VCCGT_27	VCCGT_86	T9
C17	VCCGT_28	VCCGT_87	T10
C18	VCCGT_29	VCCGT_88	U8
C20	VCCGT_30	VCCGT_89	U10
D4	VCCGT_31	VCCGT_90	V9
D7	VCCGT_32	VCCGT_91	W8
D11	VCCGT_33	VCCGT_92	W9
D12	VCCGT_34	VCCCORE_1/VCCGT_93/VCCGT_93	AA9
D14	VCCGT_35	VCCCORE_2/VCCGT_94/VCCGT_94	AB2
D15	VCCGT_36	VCCCORE_3/VCCGT_95/VCCGT_95	AB8
D17	VCCGT_37	VCCCORE_4/VCCGT_96/VCCGT_96	AB9
D18	VCCGT_38	VCCCORE_5/VCCGT_97/VCCGT_97	AB10
D20	VCCGT_39	VCCCORE_6/VCCGT_98/VCCGT_98	AC8
E4	VCCGT_40	VCCCORE_7/VCCGT_99/VCCGT_99	AD9
F5	VCCGT_41	VCCCORE_8/VCCGT_100/VCCGT_100	AE8
F6	VCCGT_42	VCCCORE_9/VCCGT_101/VCCGT_101	AE9
F7	VCCGT_43	VCCCORE_10/VCCGT_102/VCCGT_102	AE10
F8	VCCGT_44	VCCCORE_11/VCCGT_103/VCCGT_103	AF2
F11	VCCGT_45	VCCCORE_12/VCCGT_104/VCCGT_104	AF8
F14	VCCGT_46	VCCCORE_13/VCCGT_105/VCCGT_105	AF10
F17	VCCGT_47	VCCCORE_14/VCCGT_106/VCCGT_106	AG8
F20	VCCGT_48	VCCCORE_15/VCCGT_107/VCCGT_107	AG9
G11	VCCGT_49	VCCCORE_16/VCCGT_108/VCCGT_108	AH9
G12	VCCGT_50	VCCCORE_17/VCCGT_109/VCCGT_109	AJ8
G14	VCCGT_51	VCCCORE_18/VCCGT_110/VCCGT_110	AJ10
G15	VCCGT_52	VCCCORE_19/VCCGT_111/VCCGT_111	AK2
G17	VCCGT_53	VCCCORE_20/VCCGT_112/VCCGT_112	AK9
G18	VCCGT_54	VCCCORE_21/VCCGT_113/VCCGT_113	AL8
G20	VCCGT_55	VCCCORE_22/VCCGT_114/VCCGT_114	AL9
H5	VCCGT_56	VCCCORE_23/VCCGT_115/VCCGT_115	AL10
H6	VCCGT_57	VCCCORE_24/VCCGT_116/VCCGT_116	AM8
H7	VCCGT_58	VCCCORE_25/VCCGT_117/VCCGT_117	V2
H8	VCCGT_59	VCCCORE_26/VCCGT_118/VCCGT_118	Y8
H11	VCCGT_0	VCCCORE_27/VCCGT_119/VCCGT_119	Y10
		VCCGT_SENSE	E3
		VSSGT_SENSE	D2

WHL-i7-8565U 10 of 20
A0D-8565U05-I06

+VCC_GT — **15x10 uf 0402**

C6P33 C6P2 C6P1 C6P8 C389 C506 C411 C449 C461 C429 C451 C532 C478 C396 C423 — C10u6.3X50402

+VCC_GT — **11x1 uf 0201**

C6P21 C6P20 C6P13 C6P29 C6P30 C6P7 C6P4 C6P19 C403 C421 C448 — C1u6.3X50201

+VCC_CORE

PWR short to Vcore for WHL ES2 Pin out
Cap close to Pin out

Refer to PDG 575412 Table 11-6

Domain	Primary side cap	Secondary Side cap
VCCGT	15x22uF 0603 4x47uF 0805	11x1uF 0201 15x10uF 0402

+VCC_GT

R53 100R1%0402

R58 100R1%0402

GT_SENSE <48>
GT_GSENSE <48>

VCCOPC/VCCOPC_1P8 . VCCEOPIO for U43e only

CPU1O

WHL QS/CFL U/WHL ES1_CNL U23 / WHL QS/CFL U/WHL ES1_CNL U22

K12	RSVD_25/VCC_OPC_1/RSVD_25	RSVD_39/VCCEOPIO_1/RSVD_39	AA24
K14	RSVD_26/VCC_OPC_2/RSVD_26	RSVD_40/VCCEOPIO_2/RSVD_40	AA26
K15	RSVD_27/VCC_OPC_3/RSVD_27	RSVD_41/VCCEOPIO_3/RSVD_41	AB25
K17	RSVD_28/VCC_OPC_4/RSVD_28	RSVD_42/VCCEOPIO_4/RSVD_42	AC24
K18	RSVD_29/VCC_OPC_5/RSVD_29	RSVD_43/VCCEOPIO_5/RSVD_43	AC25
K20	RSVD_30/VCC_OPC_6/RSVD_30	RSVD_44/VCCEOPIO_6/RSVD_44	AC26
L25	RSVD_31/VCC_OPC_7/RSVD_31	RSVD_45/VCCEOPIO_7/RSVD_45	AD24
M24	RSVD_32/VCC_OPC_8/RSVD_32	RSVD_46/VCCEOPIO_8/RSVD_46	AD26
M26	RSVD_33/VCC_OPC_9/RSVD_23	RSVD_19/VCCEOPIO_SENSE/RSVD_19	V25
P24	RSVD_34/VCC_OPC_10/RSVD_34	RSVD_20/VSSEOPIO_SENSE/RSVD_20	T25
P26	RSVD_35/VCC_OPC_11/RSVD_35	RSVD_56	A35
R24	RSVD_36/VCC_OPC_12/RSVD_36	RSVD_57	D34
R25	RSVD_37/VCC_OPC_13/RSVD_37	RSVD_58/OPC_RCOMP/RSVD_58	N5
R26	RSVD_38/VCC_OPC_14/RSVD_38		
V24	RSVD_21/VCC_OPC_1P8_3/RSVD_21		
W25	RSVD_22/VCC_OPC_1P8_4/RSVD_22		
Y24	RSVD_23/VCC_OPC_1P8_1/RSVD_23		
Y25	RSVD_24/VCC_OPC_1P8_2/RSVD_24		
G2	RSVD_47		
G1	RSVD_48		
C34	RSVD_49/VSS_435/RSVD_49		
G3	RSVD_50/VSS_436/RSVD_50		
G4	RSVD_51/VSS_437/RSVD_51		
A34	RSVD_52/RSVD_TP/RSVD_52		
B35	RSVD_53/RSVD_TP/RSVD_53		
AJ27	RSVD_54/MSM#/RSVD_54		
AH26	RSVD_55/ZVM#/RSVD_55		
L5	RSVD_59/OPCE_RCOMP/RSVD_59		

OPC_RCOMP — X_49.9R1%0402 R354 — For Coffee lake

15 of 20

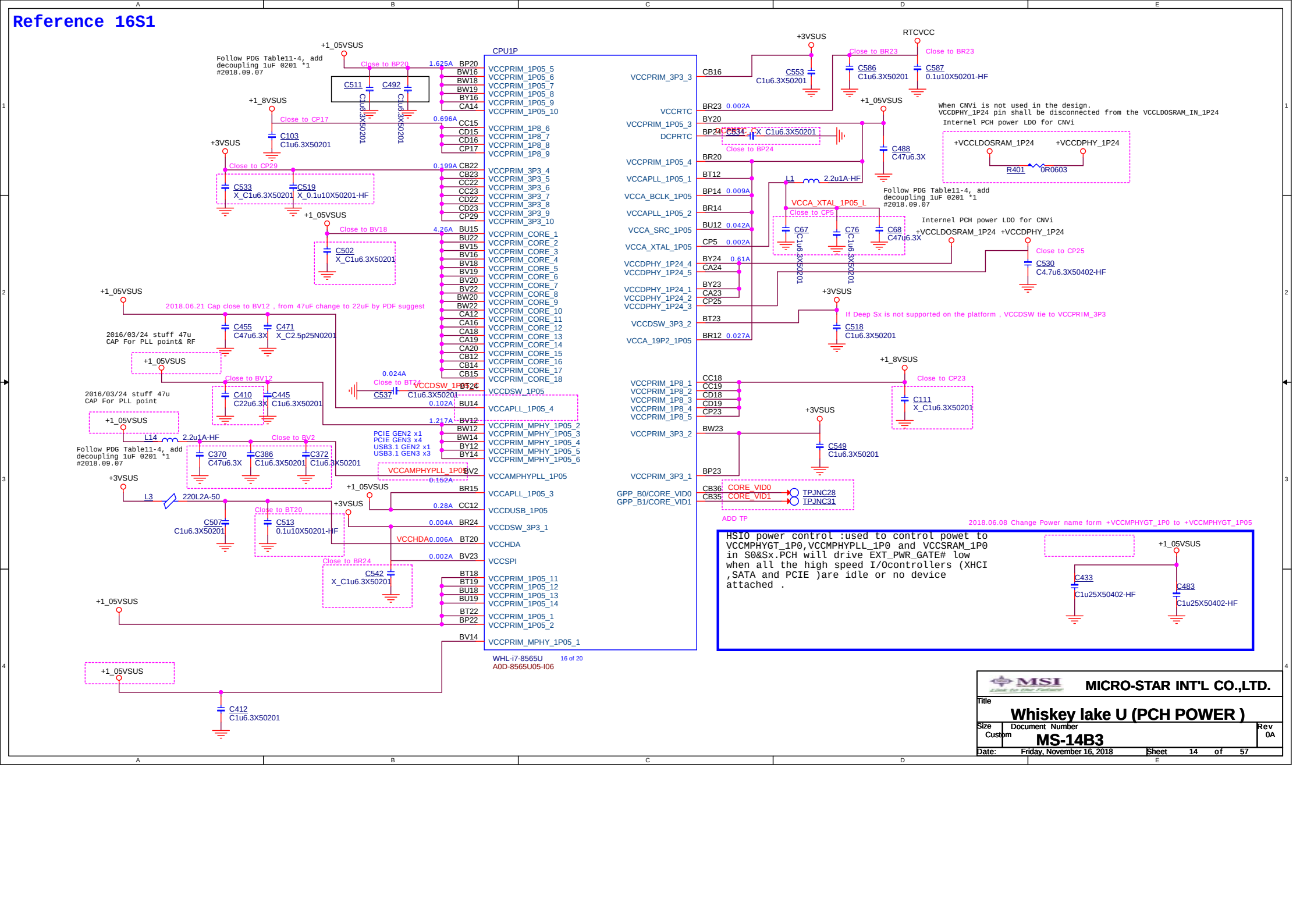
WHL-i7-8565U
A0D-8565U05-I06

All O package pinout is RSVD in WHL

TPJNC48 MSM#
TPJNC49 LPM_ZVM#
OPCE_RCOMP
X_49.9R1%0402 R353
For Coffee lake

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Whiskey lake U (GT POWER)		
Size: Custom	Document Number: MS-14B3		Rev: 0A
Date: Friday, November 16, 2018	Sheet 13 of 57		

Reference 16S1

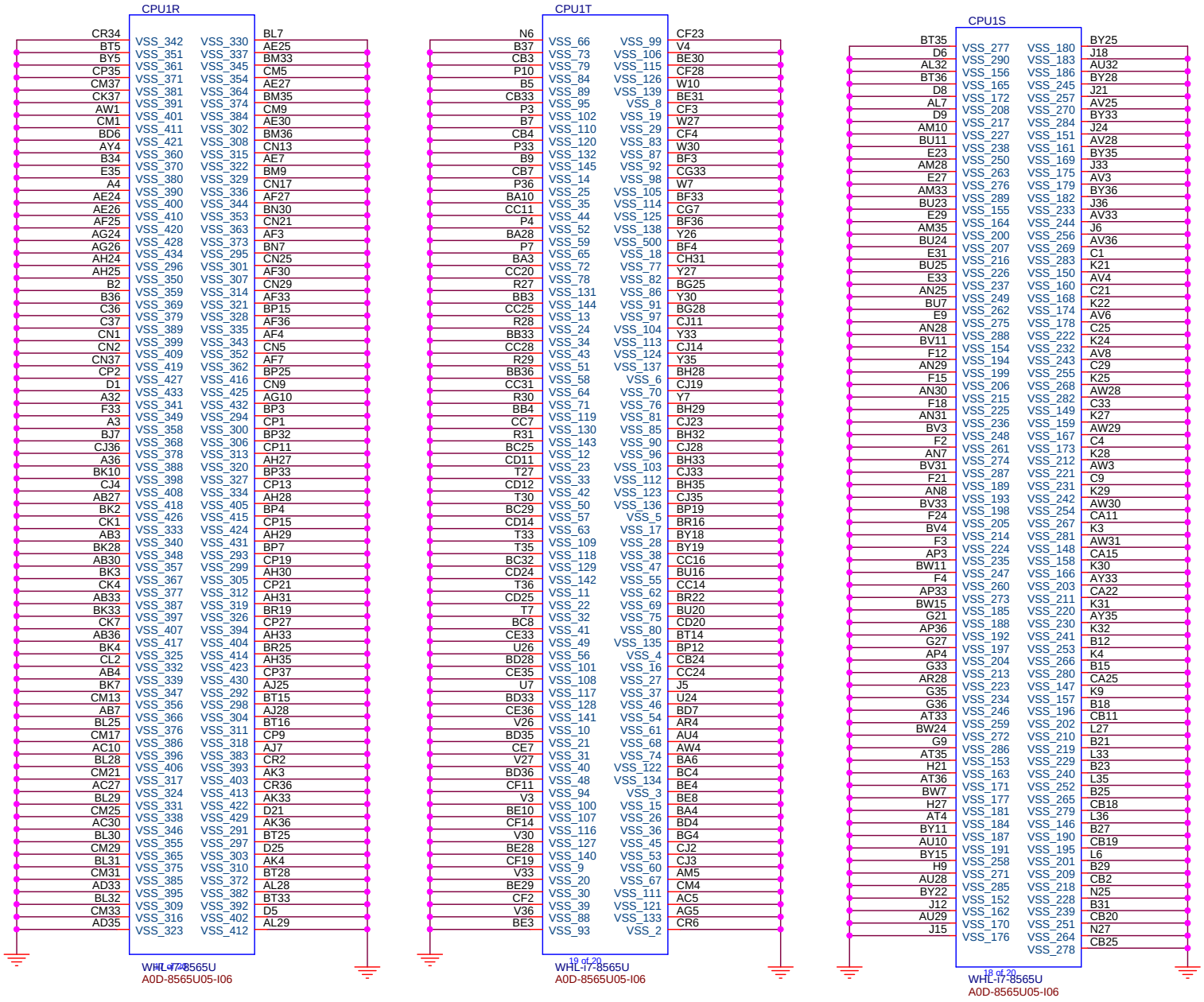


MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U (PCH POWER)

Size: Custom | Document Number: MS-14B3 | Rev: 0A

Date: Friday, November 16, 2018 | Sheet 14 of 57



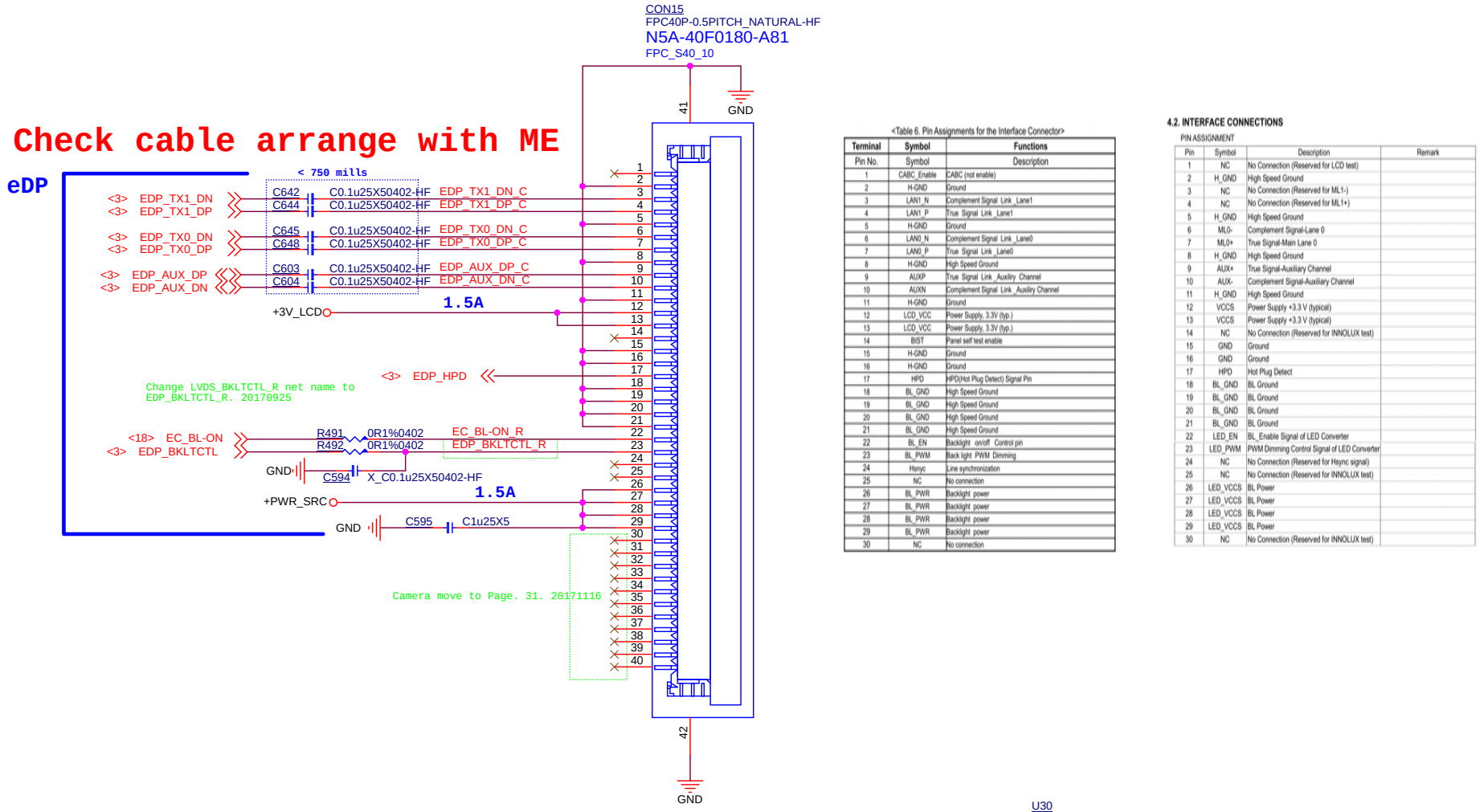
Reference 16S1

MICRO-STAR INT'L CO.,LTD.

Title: **Whiskey lake U (GND)**

Size	Document Number	Rev
Custom	MS-14B3	0A

Date: Friday, November 16, 2018 Sheet 15 of 57



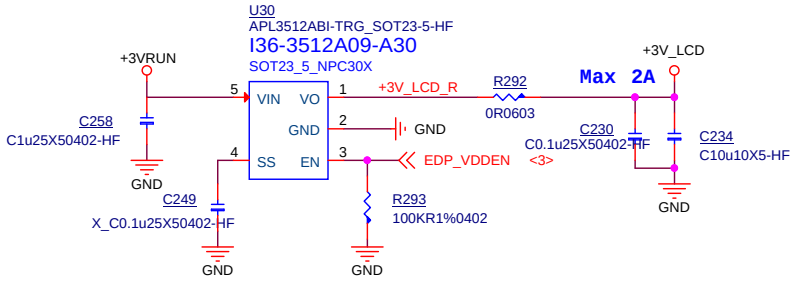
<Table 6. Pin Assignments for the Interface Connector>

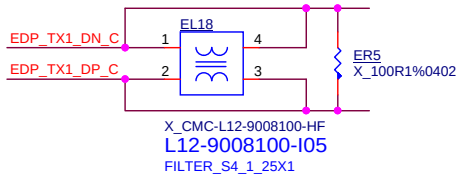
Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	CABC_Enable	CABC (not enable)
2	H-GND	Ground
3	LAN1_N	Complement Signal Link_Lane1
4	LAN1_P	True Signal Link_Lane1
5	H-GND	Ground
6	LAN0_N	Complement Signal Link_Lane0
7	LAN0_P	True Signal Link_Lane0
8	H-GND	High Speed Ground
9	AUXP	True Signal Link_Auxiliry Channel
10	AUXN	Complement Signal Link_Auxiliry Channel
11	H-GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel self test enable
15	H-GND	Ground
16	H-GND	Ground
17	HPD	HPD(Hot Plug Detect) Signal Pin
18	BL_GND	High Speed Ground
19	BL_GND	High Speed Ground
20	BL_GND	High Speed Ground
21	BL_GND	High Speed Ground
22	BL_EN	Backlight on/off Control pin
23	BL_PWM	Back light PWM Dimming
24	Hsync	Line synchronization
25	NC	No connection
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connection

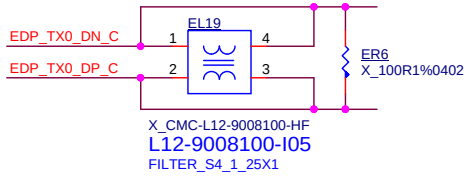
4.2. INTERFACE CONNECTIONS

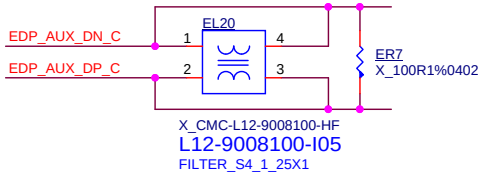
PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	NC	No Connection (Reserved for ML1-)	
4	NC	No Connection (Reserved for ML1+)	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for INNOLUX test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for Hsync signal)	
25	NC	No Connection (Reserved for INNOLUX test)	
26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for INNOLUX test)	









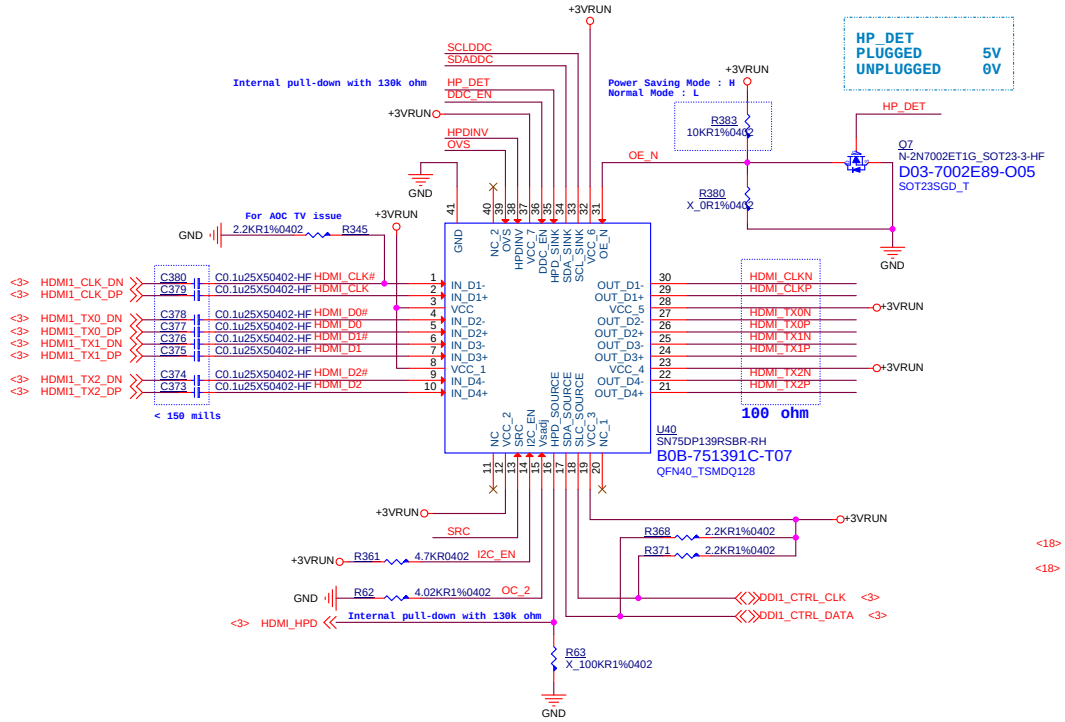
MICRO-STAR INT'L CO.,LTD.

Title: eDP Pannel

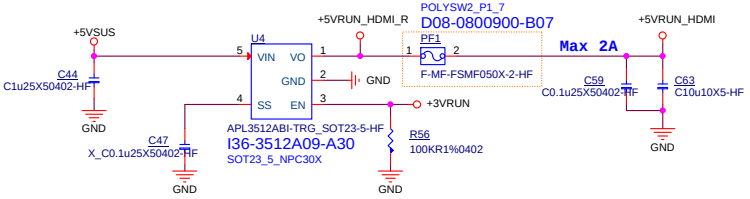
Size: Custom | Document Number: MS-14B3 | Rev: 0A

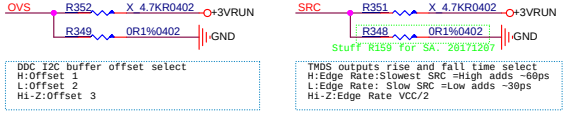
Date: Friday, November 16, 2018 | Sheet 16 of 57

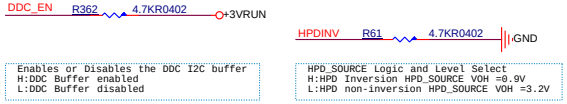
HDMI Level Shifter



Change R322 to PF1(D08-0800900-B07) for Safety. 20180202

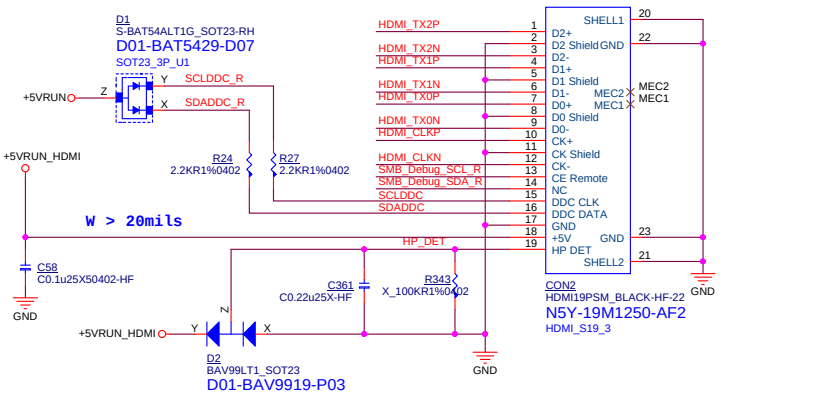


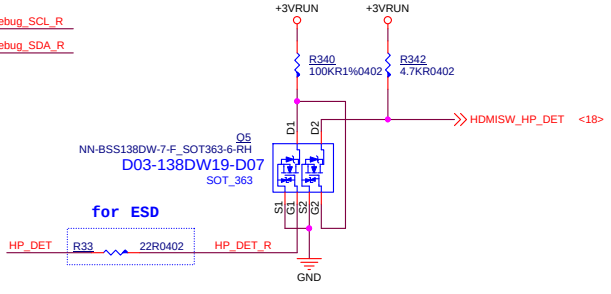




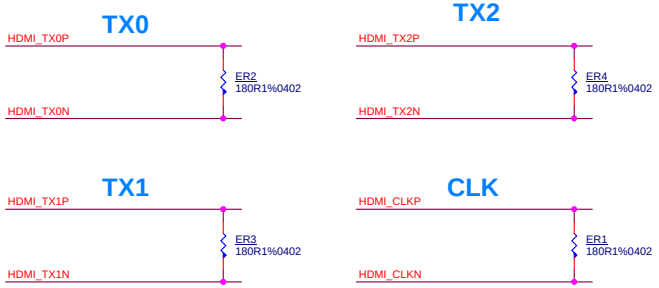
HDMI Connector

Change CON3 P/N from N5Y-19M0910-AF2 to N5Y-19M1250-AF2 for ME. 20171102A

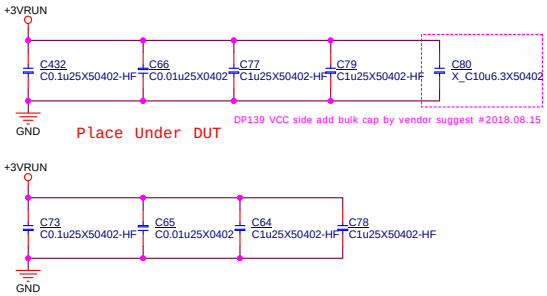




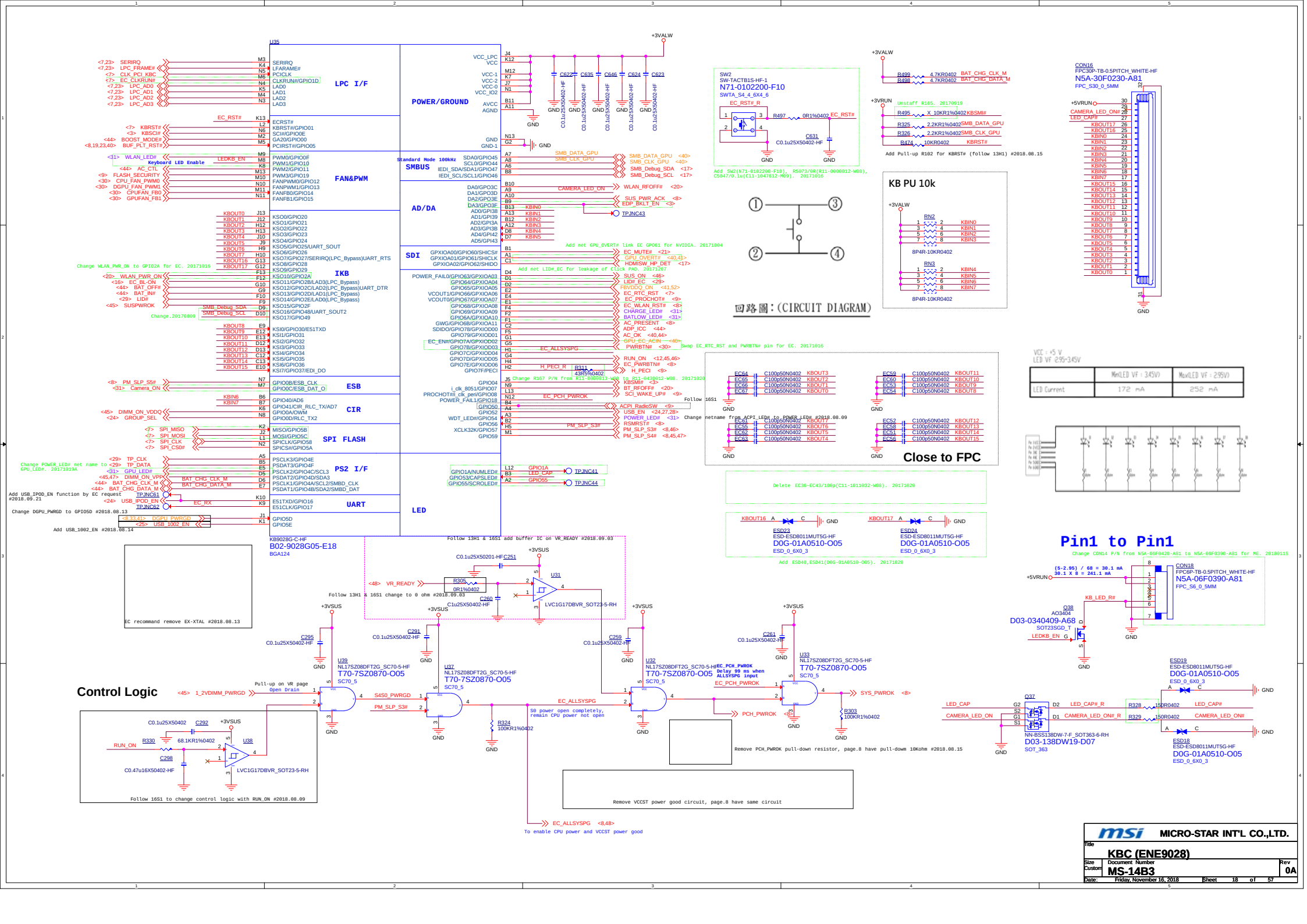
EMI Close Connector



Delete EL4~7(L12-9008100-I05) for Layout. 20171024A



MICRO-STAR INT'L CO.,LTD.			
Title: HDMI Level Shifter_SN75DP139			
Size: Custom	Document Number: MS-14B3		Rev: 0A
Date: Friday, November 16, 2018	Sheet 17 of 57		



	MaxLED VF : 3.45V)	MaxLED VF : 2.95V)
LED Current	172 mA	252 mA

Title	KBC (ENE9028)	
Size: Custom	Document Number: MS-14B3	Rev: 0A
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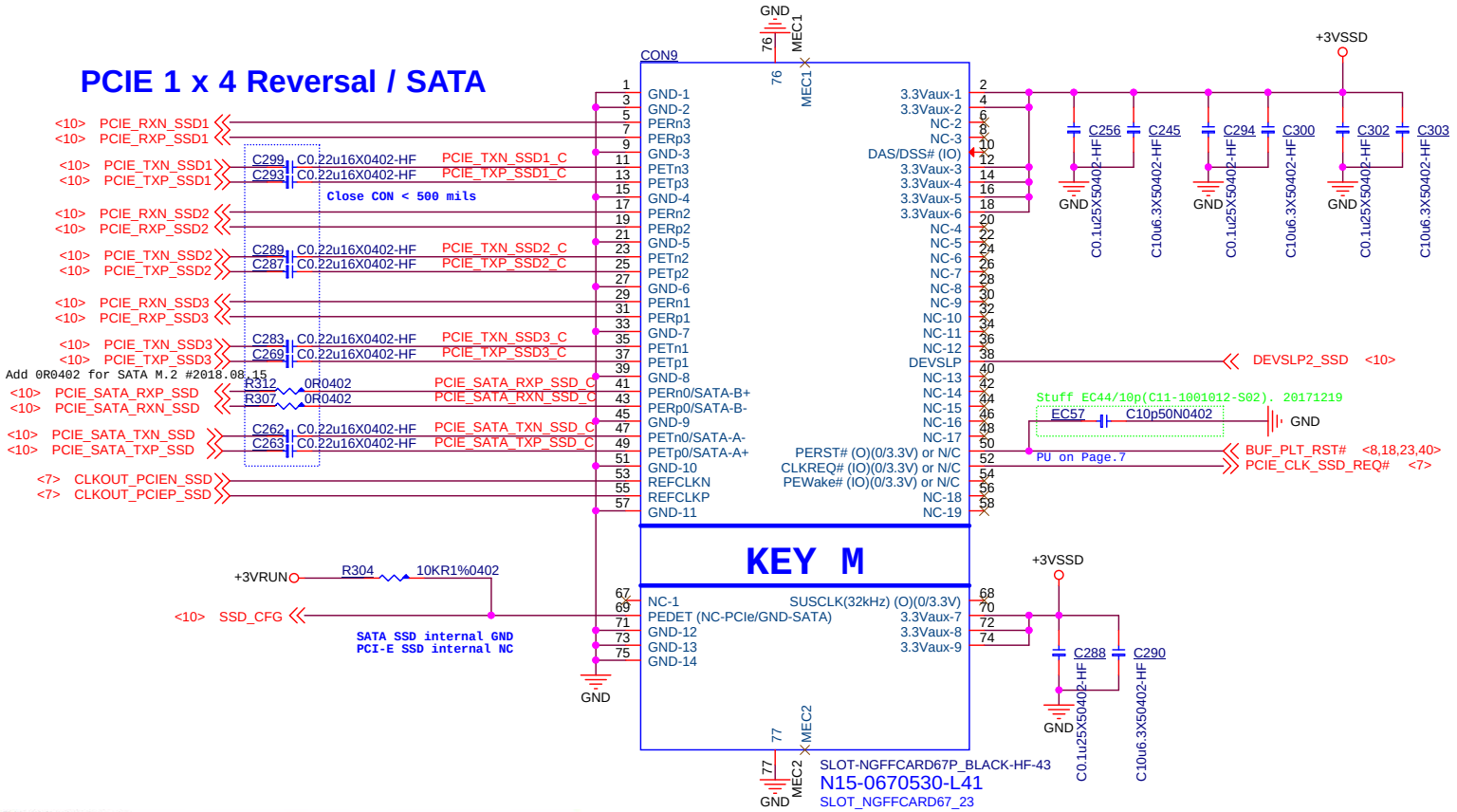
MICRO-STAR INT'L CO.,LTD.

PCIE 1 x 4 Reversal / SATA



74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWake# (IO)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)(0/3.3V)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I)(OD)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

[Table 10] Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	N/C	N/C
9	GND	Return current path	10	LED1#[1]	Device Active Signal (Refer to [Table 11])
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCIe TX	42	N/C	N/C
43	PETp0	PCIe TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCIe Reference Clock	56	Reserved for MFG_Data	N/C
57	GND	Return current path	58	Reserved for MFG_CLOCK	N/C
67	N/C	N/C	68	SUSCLK	N/C
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

+3VRUN R296 0R0603 +3VSSD

Add R5035/0R and +3VSSD. 20170926

PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLK+/ REFCLK-	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST#	O	PE-Reset is a functional reset to the card as defined by the PCIe Mini Card CEM specification	3.3V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates	3.3V
	WAKE#/OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3V

SSD STAND OFF

Spacer Support
UME23
E2B-16K1010-RH
E2B-16K1010-A89
H_R201D118_PT_N
GND

Add UME29 P/N:E2B-16K1010-A89 Footprint:H_R201D118_PT for ME.20171014
Change UME29 footprint to H_R201D118_PT_N for Layout. 20171030

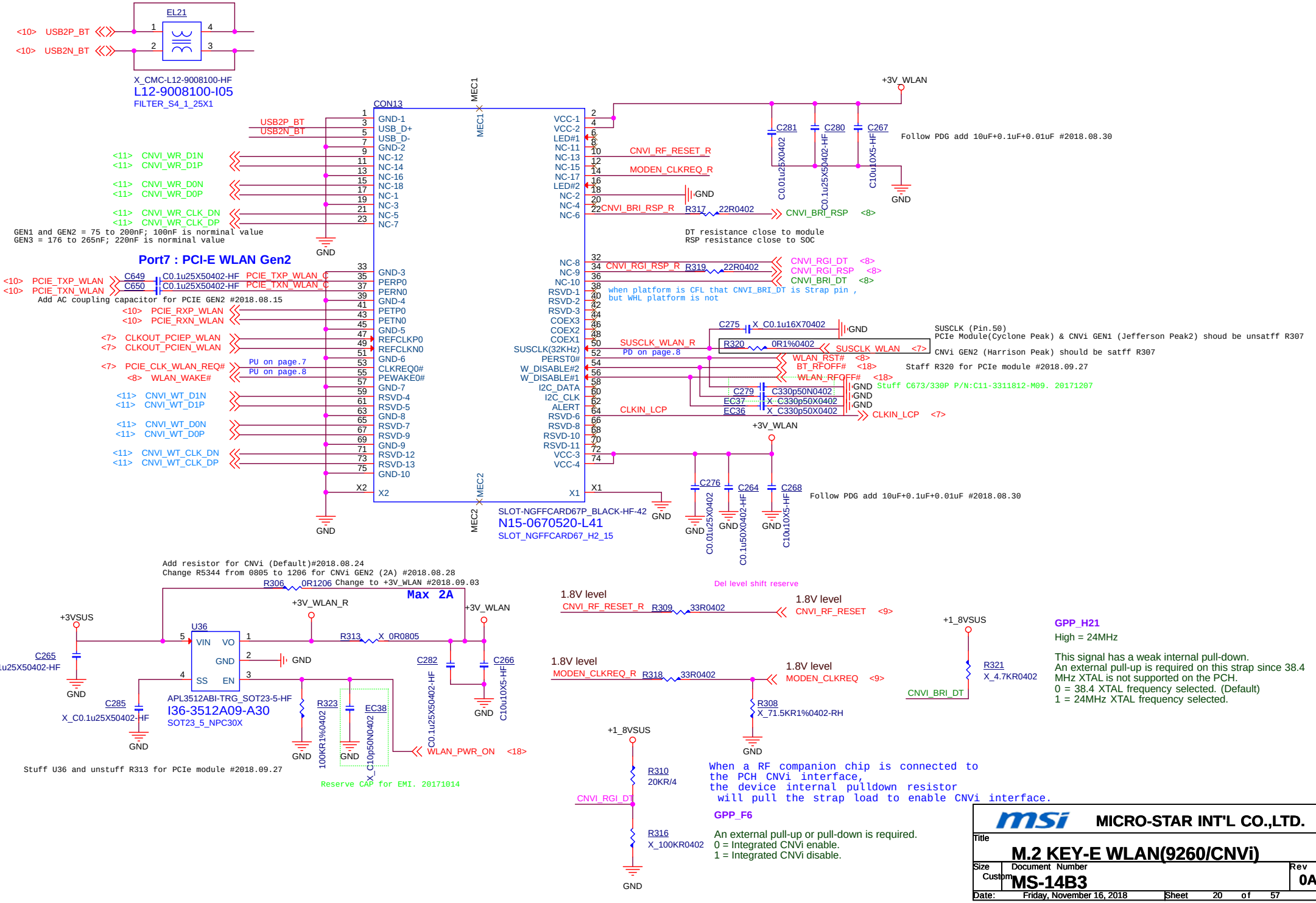
MICRO-STAR INT'L CO.,LTD.

Title: M.2 KEY-M Combo SSD

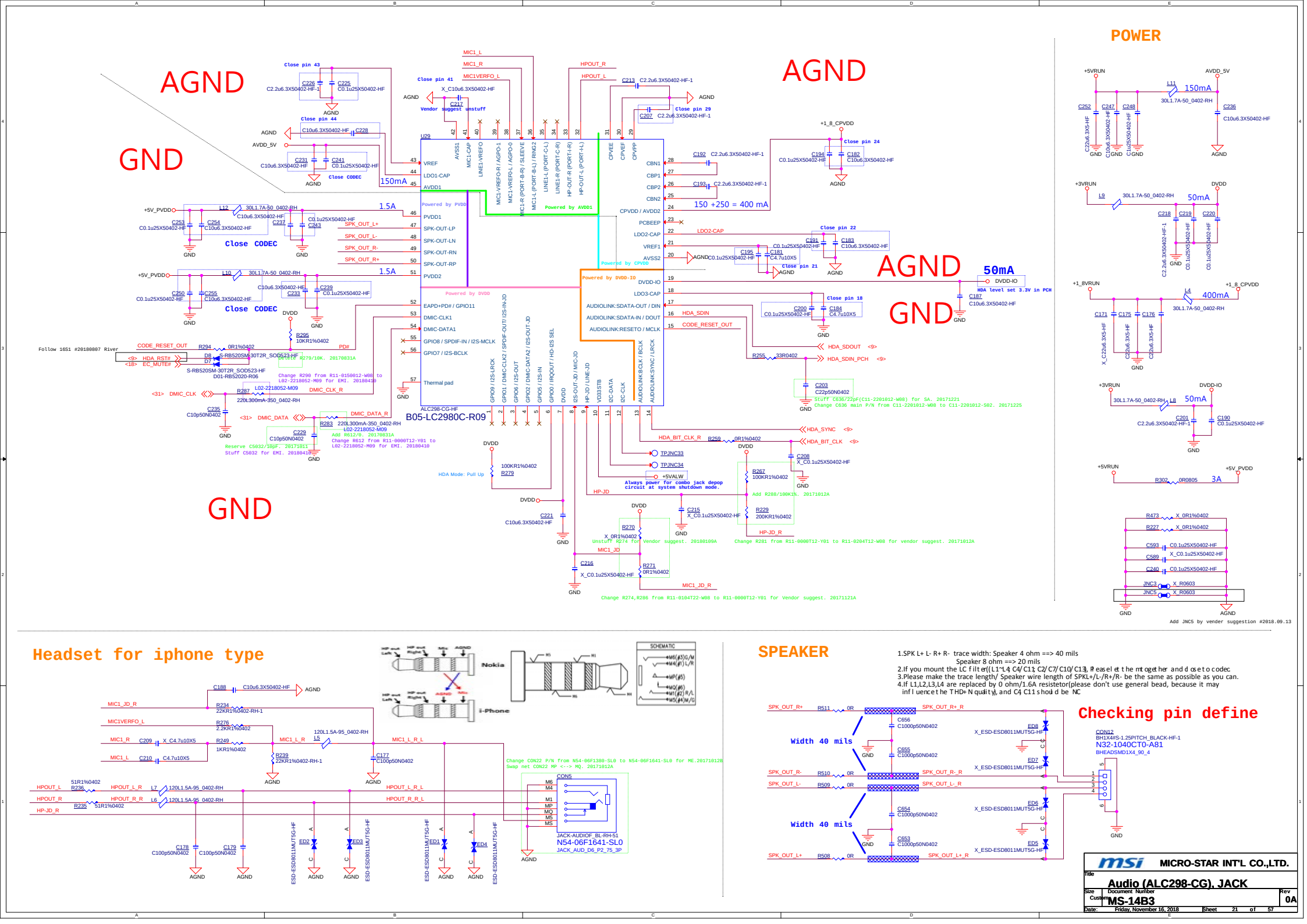
Size: Custom | Document Number: MS-14B3 | Rev: 0A

Date: Friday, November 16, 2018 | Sheet 19 of 57

Add CNVi function by PM request #2018.08.24

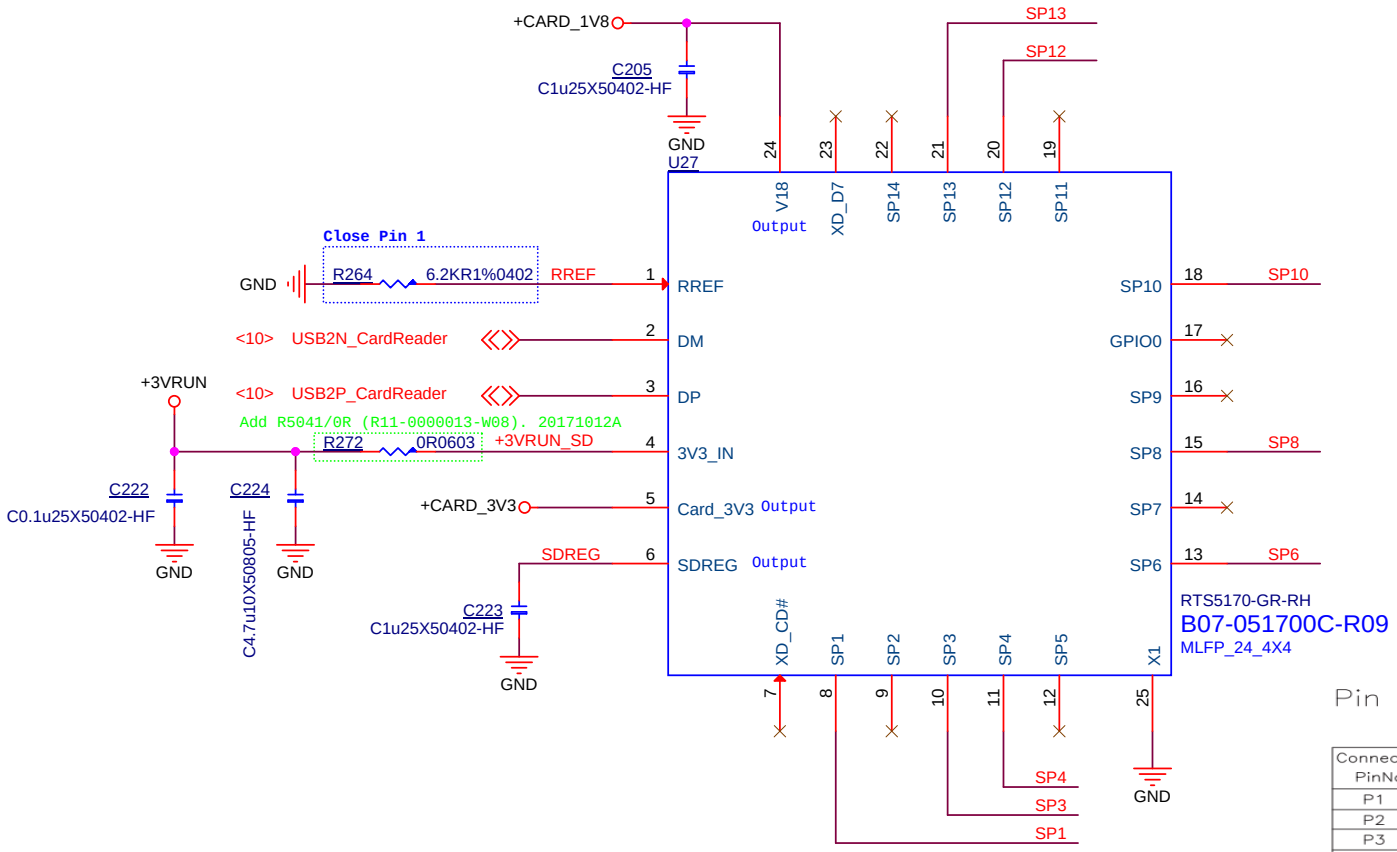


MICRO-STAR INT'L CO.,LTD.			
Title: M.2 KEY-E WLAN(9260/CNVi)			
Size: Custom	Document Number: MS-14B3		Rev: 0A
Date: Friday, November 16, 2018	Sheet 20 of 57		



1.SPK L+ L- R+ R- trace width: Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
2.If you mount the LC filter((L1~L4, C4/C11; C2/C7/C10/C13), Please let the mt oget her and d ose to codec
3.Please make the trace length/ Speaker wire length of SPKL+/L-/R+/R- be the same as possible as you can.
4.If L1,L2,L3,L4 are replaced by 0 ohm/1.6A resistetor(please don't use general bead, because it may
inf l uence t he THD+ N quality), and C4 C11 s hou l d be NC

Add JNC5 by vender suggestion #2018.09.13



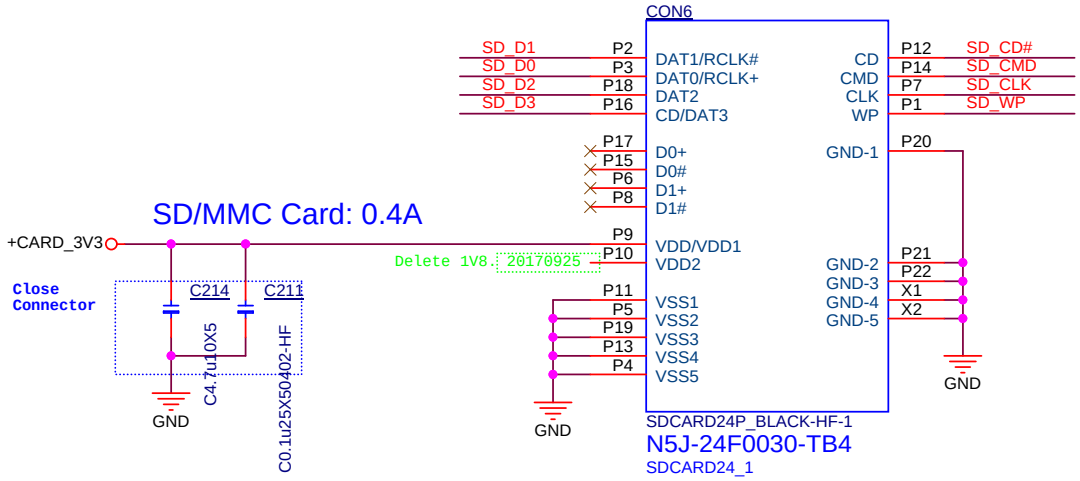
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

For EMI and Close to RTS5170

SP1	0R1%0402	R280	SD_WP	EC24	X_C10p50N0402
SP3	0R1%0402	R281	SD_D1	EC25	C15p50N0402
SP4	0R1%0402	R282	SD_D0	EC26	C15p50N0402
SP6	0R1%0402	R273	SD_CD#	EC23	X_C10p50N0402
SP8	0R1%0402	R269	SD_CLK	EC22	C15p50N0402
SP10	0R1%0402	R266	SD_CMD	EC20	X_C10p50N0402
SP12	0R1%0402	R257	SD_D3	EC19	C15p50N0402
SP13	0R1%0402	R256	SD_D2	EC18	C15p50N0402

Stuff EC61~64, EC67/15pF(C11-1501012-S02) for SA. 20171221

GND



Pin Define

Connector PinNo.	Specifications SD4.0 PinNo.	Specifications MMC PinNo.	SD Mode Name	Type	Description
P1			WP		
P2	P8		DAT1	I/O/PP	Data Line[Bit 1]
P3	P7	P7	DAT0	I/O/PP	Data Line[Bit 0]
P4	P17		—		Not Used(Connected to ground)
P5	P6	P6	VSS2	S	Supply voltage ground
P6	P16		—		Not Used
P7	P5	P5	CLK	I	Clock
P8	P15		—		Not Used
P9	P4	P4	VDD	S	Supply voltage
P10	P14		—		Not Used
P11	P3	P3	VSS1	S	Supply voltage ground
P12			CD		
P13	P13		—		Not Used(Connected to ground)
P14	P2	P2	CMD	PP	Command/Response
P15	P12		—		Not Used
P16	P1	P1	CD/DAT3	I/O/PP	Card Detect/ Data Line[Bit 3]
P17	P11		—		Not Used
P18	P9		DAT2	I/O/PP	Data Line[Bit 2]
P19	P10		—		Not Used(Connected to ground)
P20			GND		
P21			GND		
P22			GND		
P23			GND		
P24			GND		

MICRO-STAR INT'L CO.,LTD.

Title: **Card Reader (RTS5170)**

Size	Document Number	Rev
Custom	MS-14B3	0A

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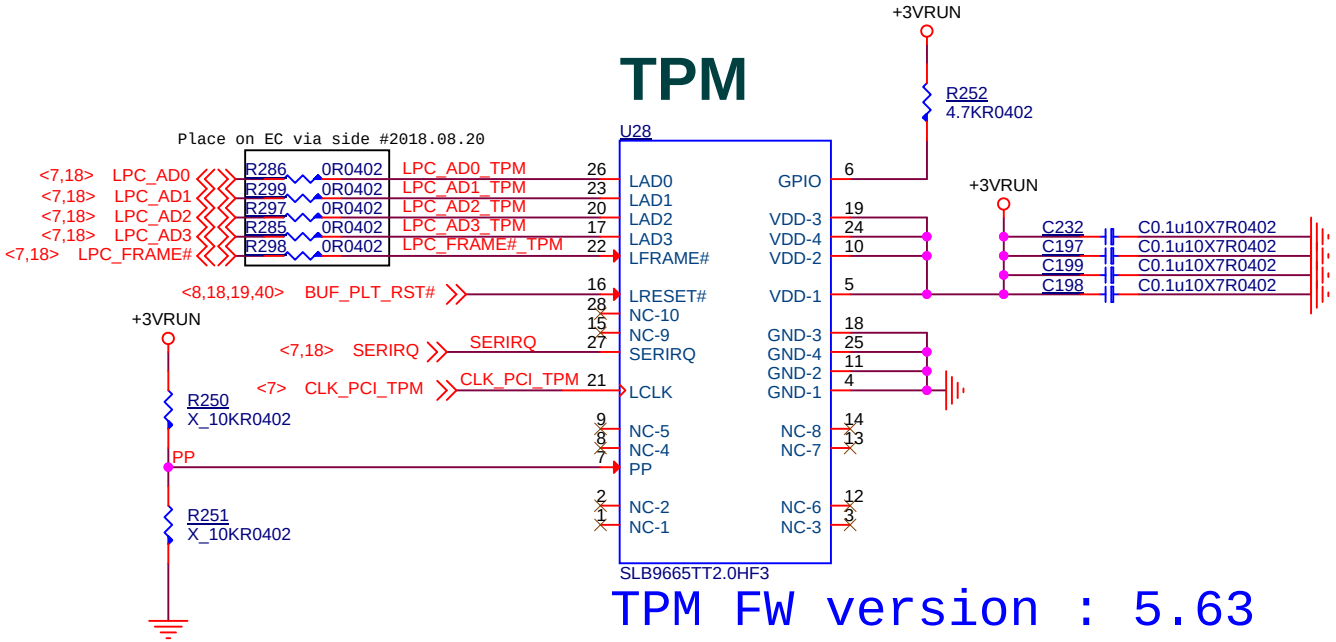
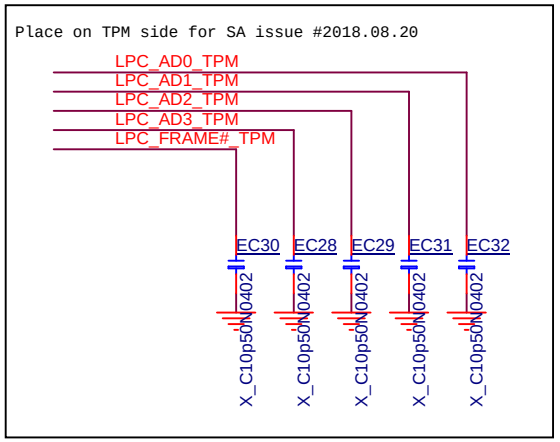
TPM





TPM FW version : 5.63

PP (Physical Presence) :
The TPM 2.0 device does not use this functionality

0B. Add TPM BOM control table for ODM & OBM #2018.11.13

	ODM	OBM
U28	X	V
R R285 R286 R297 R298 R299 R252	X	V
C C197 C198 C199 C232	X	V

MICRO-STAR INT'L CO.,LTD.

Title: TPM

Size: A4 | Document Number: MS-14B3 | Rev: 0A

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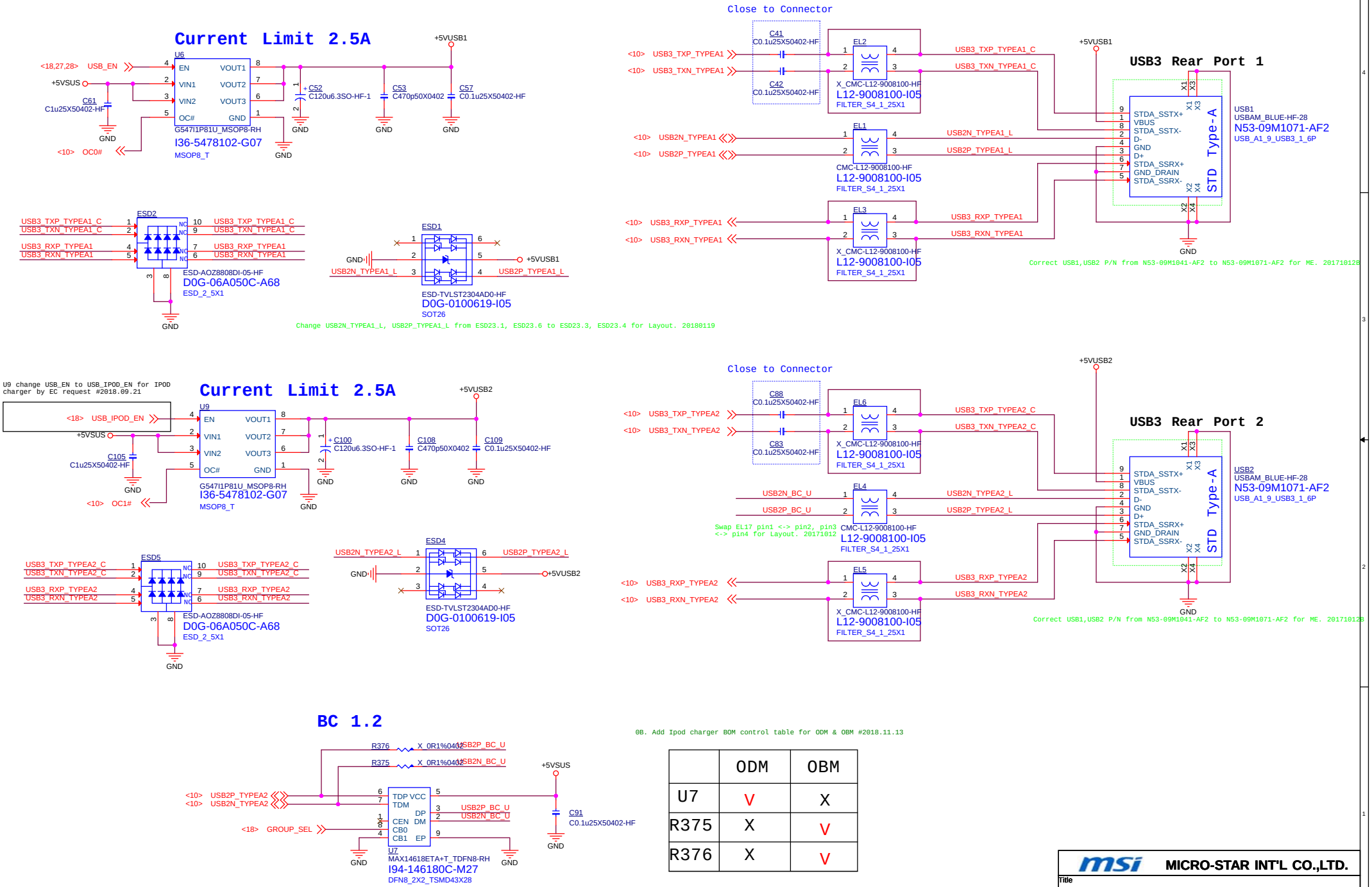

	ODM	OBM
U7	V	X
R375	X	V
R376	X	V

MICRO-STAR INT'L CO.,LTD.

Title: USB3 Type-A Port1,2

Size: Custom | Document Number: MS-14B3 | Rev: 0A

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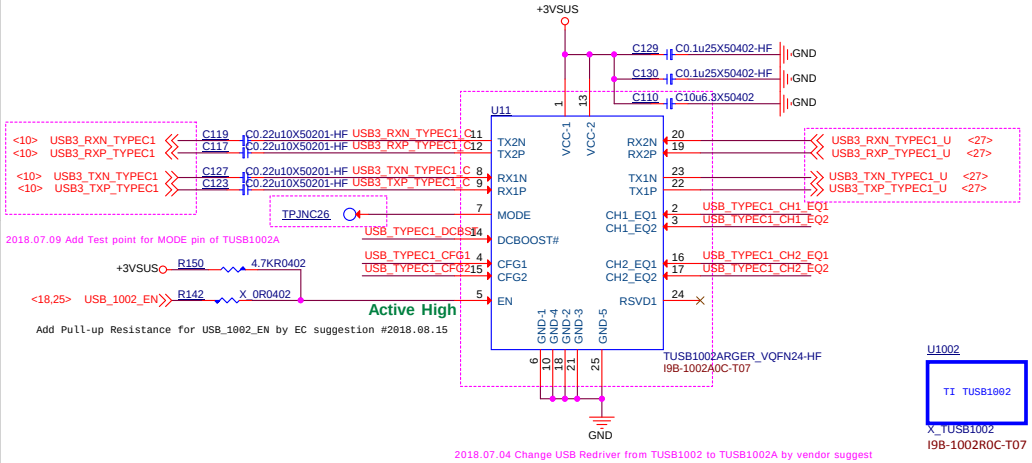
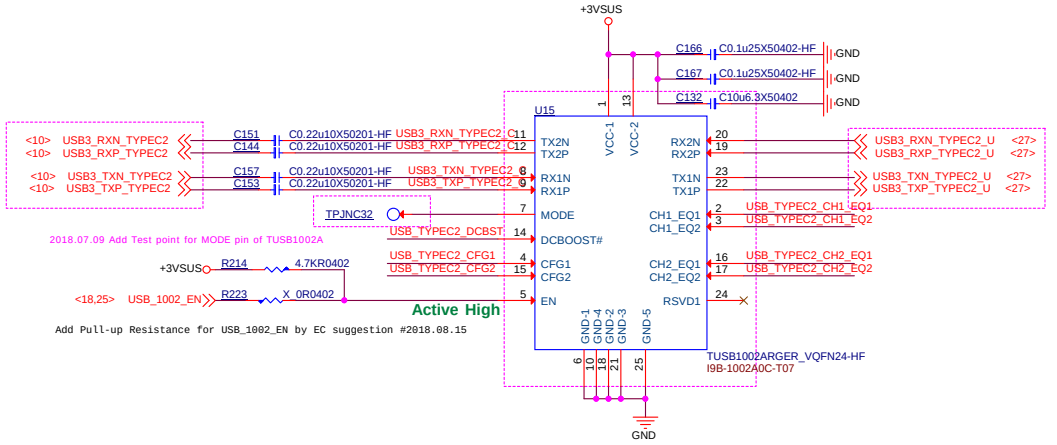
Reference 13H1

USB3.0 TYPE-C Port 3 Redriver TOP



2018.07.04 Change USB Redriver from TUSB1002 to TUSB1002A by vendor suggest

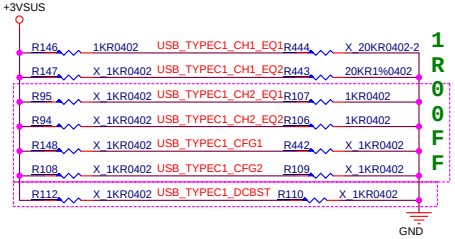
USB3.0 TYPE-C Port 3 Redriver BOT



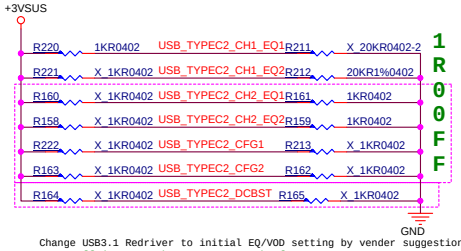
TUSB1002A

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.



2018.07.04 DCBST:When asserted low, DC Gain levels in Table 3 are increased by +1dB.
2018.07.17 Change CFG1/CFG2 to 900mV(0,0) by vendor suggest
2018.07.17 Change CH2_EQ[1:2] = 0,0 because TUSB1002A will place cllosed to connector by vendor suggest
Change USB3.1 Redriver to initial EQ/VOD setting by vender suggestion #2018.09.14
0B. Change R443 & R212 from 20k ohm to 1k ohm by vender suggestion #2018.11.02
0B. Stuffed R146 & change R443 to 20kR for SA #2018.11.09



Change USB3.1 Redriver to initial EQ/VOD setting by vender suggestion #2018.09.14
0B. Stuffed R220 & change R212 to 20kR for SA #2018.11.09

Table 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting

EQ SETTING #	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5GHz / 5 GHz (dB)
1	0	0	1.0 / 3.6
2	0	R	2.1 / 5.5
3	0	F	3.0 / 6.8
4	0	1	4.0 / 8.1
5	R	0	4.6 / 9.0
6	R	R	5.5 / 10.0
7	R	F	6.2 / 10.8
8	R	1	6.9 / 11.6
9	F	0	7.3 / 11.9
10	F	R	7.9 / 12.6
11	F	F	8.4 / 13.1
12	F	1	9.0 / 13.7
13	1	0	9.4 / 14.1
14	1	R	9.9 / 14.6
15	1	F	10.3 / 14.9
16	1	1	10.7 / 15.3

Table 3. VOD Linear Range and DC Gain

SETTING #	CFG1 PIN LEVEL	CFG2 PIN LEVEL	CH1 DC GAIN (dB)	CH2 DC GAIN (dB)	CH1 V_{OD} LINEAR RANGE (mVpp)	CH2 V_{OD} LINEAR RANGE (mVpp)
1	0	0	+1	0	900	900
2	0	R	0	+1	900	900
3	0	F	0	0	900	900
4	0	1	+1	+1	900	900
5	R	0	0	0	1000	1000
6	R	R	+1	0	1000	1000
7	R	F	0	-1	1000	1000
8	R	1	+2	+2	1000	1000
9	F	0	-1	-1	1200	1200
10	F	R	+2	+2	1200	1200
11	F	F	0	0	1200	1200
12	F	1	+1	+1	1200	1200
13	1	0	+2	0	1200	1200
14	1	R	0	+2	1200	1200
15	1	F	0	+1	1200	1200
16	1	1	+1	0	1200	1200

MICRO-STAR INT'L CO.,LTD.

Title: U3 Re-driver TYPE-C Port3

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msi MICRO-STAR INT'L CO.,LTD.			
Title: BLANK			
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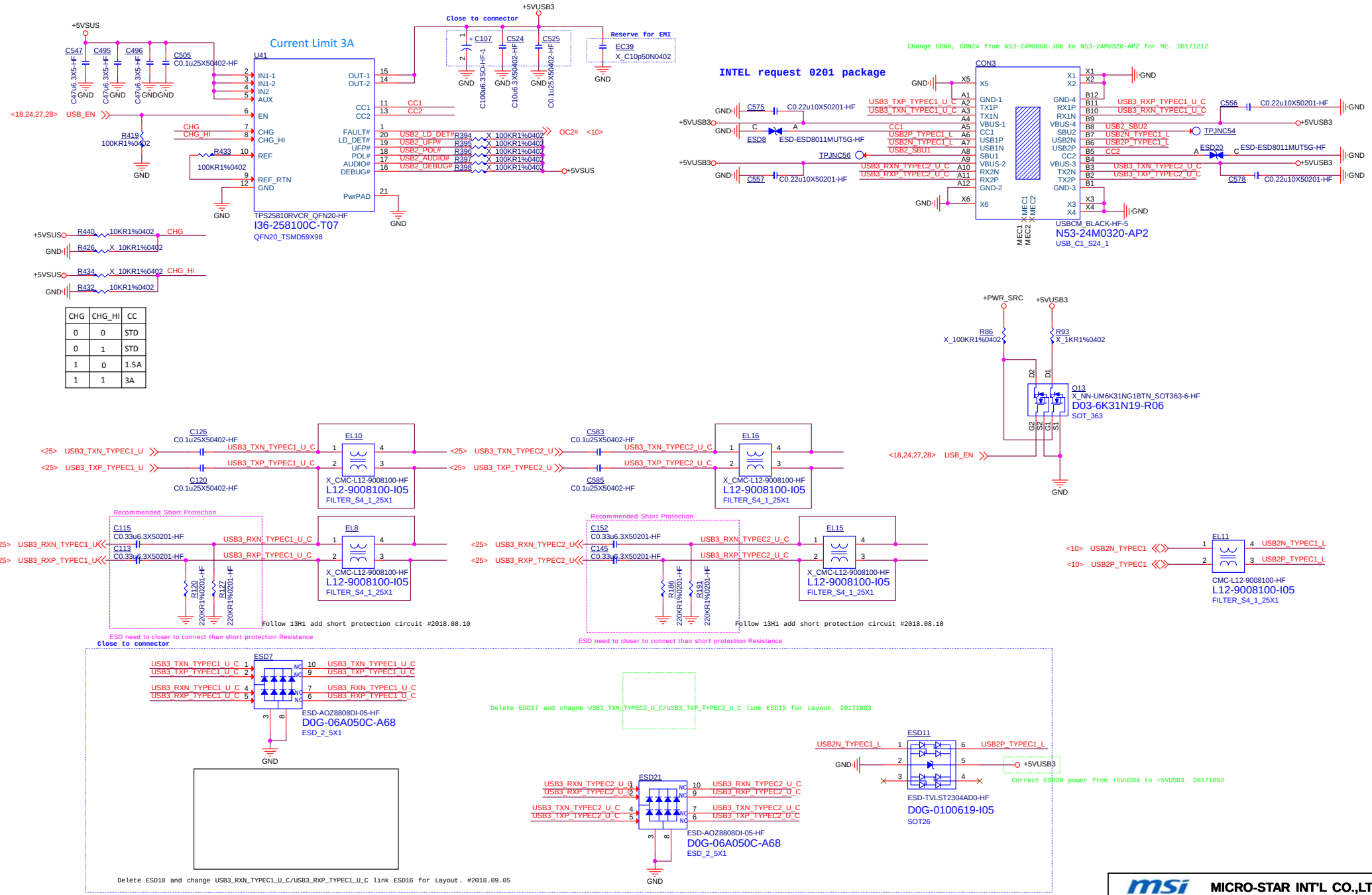

CHG	CHG_HI	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

MICRO-STAR INT'L CO.,LTD.

Title: USB Type-C (TPS25810) Port3

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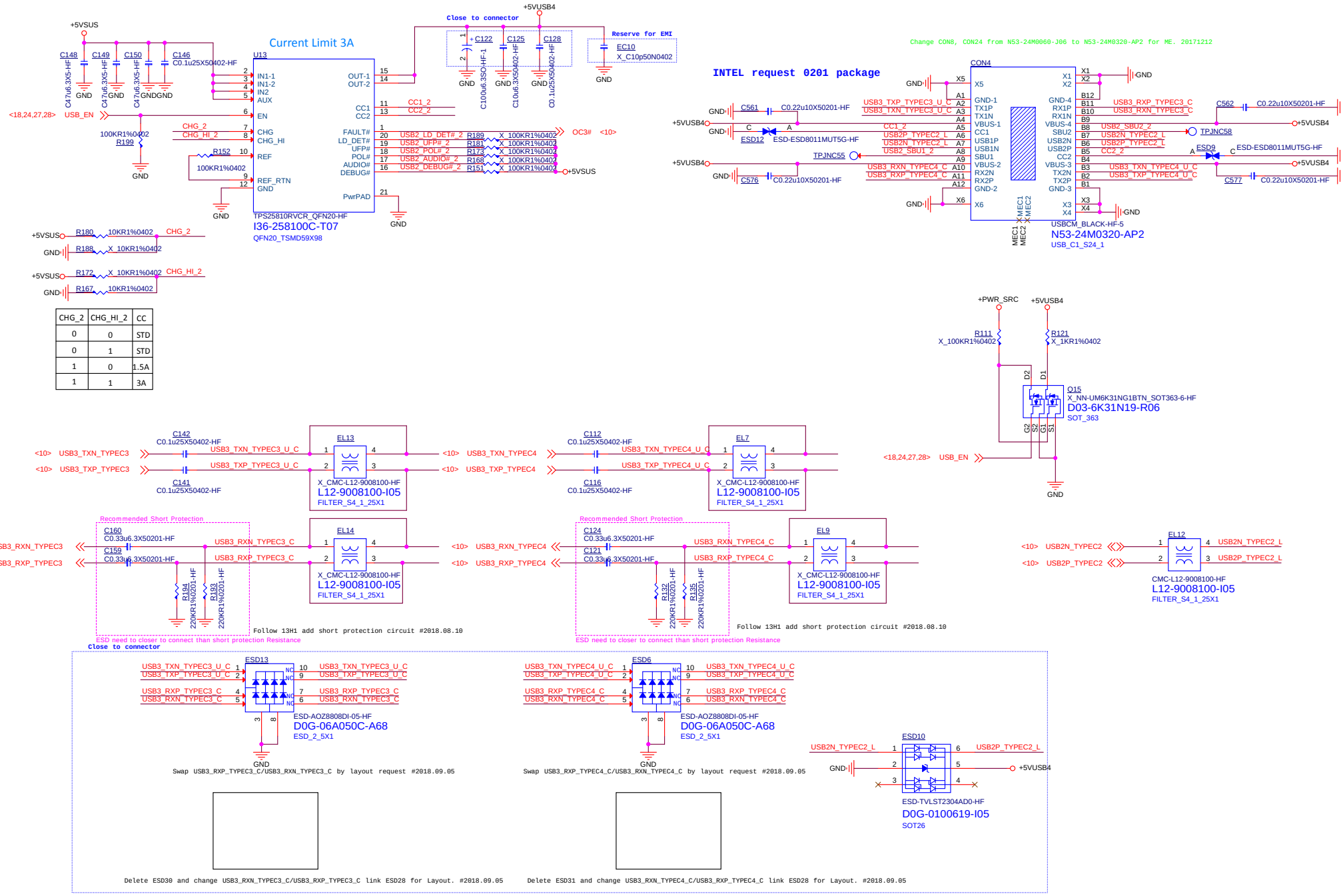

CHG_2	CHG_HI_2	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

MICRO-STAR INT'L CO.,LTD.

Title: USB Type-C(TPS25810) Port4

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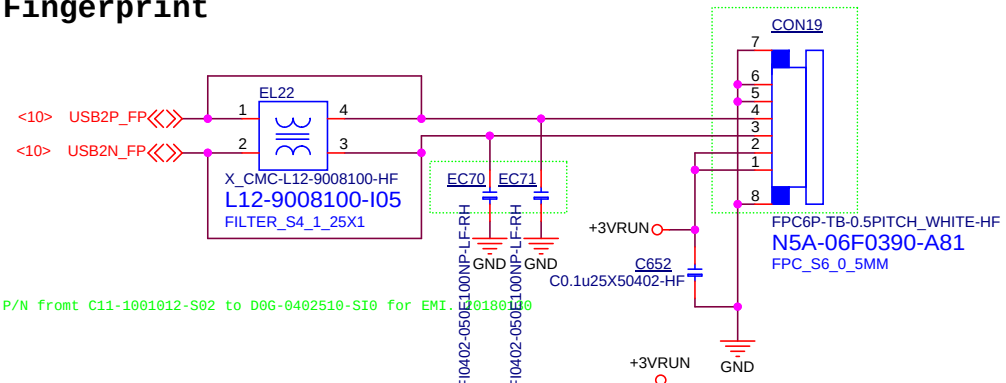
Fingerprint

Change CON16 P/N from N5A-06F0420-A81 to N5A-06F0390-A81 for ME. 20180115
Mirror CON16 vertical for FFC. 20171017

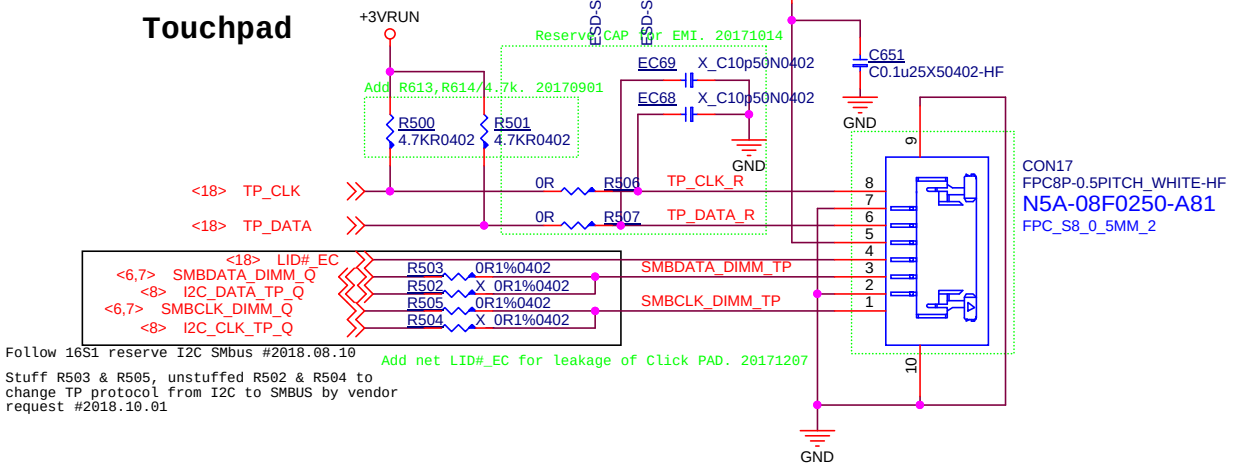


Change EC2,EC3 P/N fromt C11-1001012-S02 to D0G-0402510-SI0 for EMI. 20180130

J2 Pin Assignments and Definitions

Pin Number	Pin Name	Description
1	VDD	Power Supply
2	VDD	Power Supply
3	USB D-	USB D-
4	USB D+	USB D+
5	GND	Ground
6	GND	Ground

Touchpad



Follow 16S1 reserve I2C SMbus #2018.08.10

Stuff R503 & R505, unstuffed R502 & R504 to change TP protocol from I2C to SMBUS by vendor request #2018.10.01

Add net LID#_EC for leakage of Click PAD. 20171207

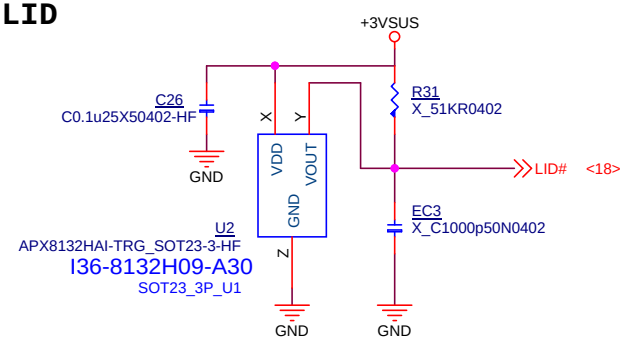
J1 (Host Interface) Pin Assignments and Definitions

Pin Number	Pin Name	Description
1	SMB_CLK	SMbus Clock
2	GND	Ground
3	SMB_DAT	SMbus Data
4	LID Close	Disable when lid is closed(1)
5	VDD	Power Supply
6	PS2_DAT	PS2 Data
7	GND	Ground
8	PS2_CLK	PS2 Clock

(1) Disable Touchpad when lid is closed (system sleep), to prevent from LCD noise coupling to touchpad and cause sensor malfunction

Change CON17 P/N from N5A-08F0160-A81 to N5A-08F0300-A81 for ME.20171004
Change CON17 P/N from N5A-08F0300-A81 to N5A-08F0250-A81 for ME. 20180115

LID



MICRO-STAR INT'L CO.,LTD.

Title: Click,FingerPrint,LID

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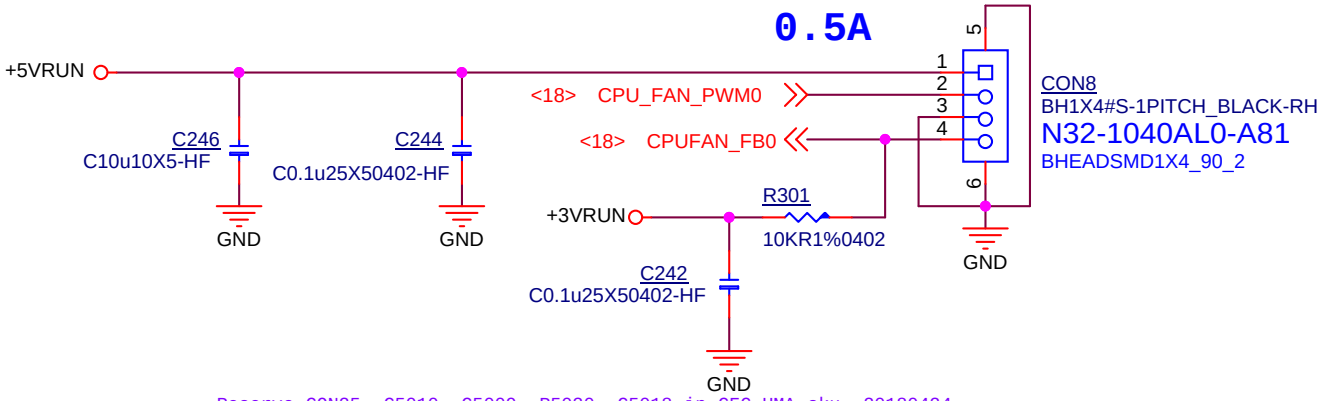
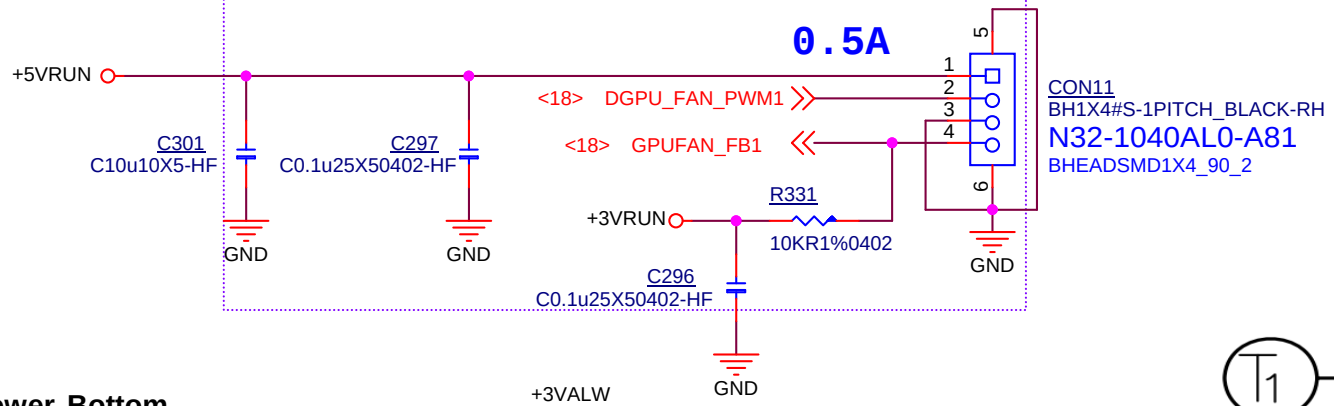
FAN

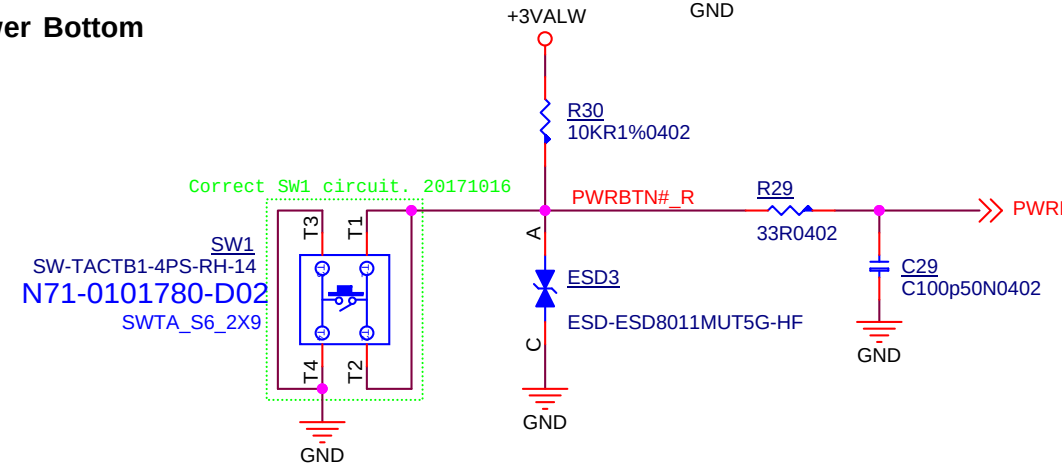
PIN NO.	LEAD COLOR
1	RED(+)
2	BLUE(PWM)
3	BLACK(−)
4	YELLOW(FG)



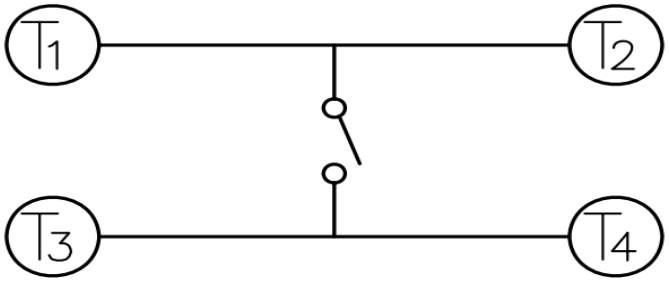
Reserve CON25, C5010, C5009, R5030, C5018 in CFG_UMA sku. 20180424



Power Bottom



Change SW1 P/N from N71-0103361-D02 to N71-0101780-D02 for ME. 20170929



CIRCUIT DIAGRAM

MICRO-STAR INT'L CO.,LTD.

Title: FAN,Power SW

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Change LED1,LED2,LED3 P/N from D0C-0405800-L05 to D0C-040C300-L05 for ME. 20171117A
Change LED4 P/N from D0C-0405400-L05 to D0C-040J800-L05 for ME. 20171117A

+5VSUS — R242 330R0402 — LED1 LED04-WHI-20mA3.15V_1608-RH D0C-040C300-L05 LEDS_19_21SYGC — (5-2.8)/330 = 6.7mA — POWER_LED# <18>

Change netname from ACPI_LED# to POWER_LED# #2018.08.09

+5VALW

R268 330R0402 — LED2 LED04-WHI-20mA3.15V_1608-RH D0C-040C300-L05 LEDS_19_21SYGC — (5-2.8)/330 = 6.7mA — CHARGE_LED# <18>

R277 330R0402 — LED3 LED04-O-30mA2.3V_1608-RH D0C-040J800-L05 LEDS_19_21SYGC — (5-2)/330 = 9mA — BATLOW_LED# <18>

Change charge_LED# pull up to +5VALW #2018.08.09

0.23A

+5VRUN — R481 0R0603 — +5VRUN_Camera

Delete Camera power switch circuit. 20170926

R300 330R0402 — LED4 LED04-WHI-20mA3.15V_1608-RH D0C-040C300-L05 LEDS_19_21SYGC — (5-2.8)/330 = 6.7mA — WLAN_LED# <18>

R496 330R0402 — LED5 LED04-WHI-20mA3.15V_1608-RH D0C-040C300-L05 LEDS_19_21SYGC — (5-2.7)/330 = 6.9mA — GPU_LED# <18>

Reserve LED5, R5036 in CFG_UMA sku. 20180424

Change POWER_LED# net name to GPU_LED#. 20171019A

USB2P_CAMERA, USB2N_CAMERA — EL17 (1, 2, 3, 4)

X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1

Change CON26 P/n from N5A-10F0240-A81 to N5A-10F0220-A81 for ME. 20180115
Correct CON26 P/N:N5A-10F0240-A81. 20171212B
Change CON26 from N5A-10F0240-A81 to N5Q-10F0030-A81 for ME. 20171212

CON14
N5A-10F0220-A81
FPC_S10_0_5MM_1
FPC10P-TB-0.5PITCH_WHITE-HF

GND-2, GND-1

<21> DMIC_CLK
<21> DMIC_DATA

0.01A

+3VRUN

<18> Camera_ON
+5VRUN_Camera

<10> USB2P_CAMERA
<10> USB2N_CAMERA
USB2P_CAMERA
USB2N_CAMERA

Delete TPM circuit for Layout space. 20171018

Reserve CAP for EMI. 20171017

EC47 X_C10p50N0402 GND
EC46 X_C10p50N0402 GND
EC48 C330p50X0402 GND
C590 C0.1u25X50402-HF GND
C591 C0.1u25X50402-HF GND

GND

Stuff EC1(C11-3312012-M09) for EMI. 20171218

ESD14 ESD-ESD8011MUT5G-HF D0G-01A0510-O05 ESD_0_6X0_3
ESD15 ESD-ESD8011MUT5G-HF D0G-01A0510-O05 ESD_0_6X0_3
ESD16 ESD-ESD8011MUT5G-HF D0G-01A0510-O05 ESD_0_6X0_3
ESD17 ESD-ESD8011MUT5G-HF D0G-01A0510-O05 ESD_0_6X0_3
ESD22 ESD-ESD8011MUT5G-HF D0G-01A0510-O05 ESD_0_6X0_3

GND

Reserve ESD39 in CFG_UMA sku. 20180424

Pin Description							
Pin No.	Name	Pin Type	Function Des.	Pin No.	Name	Pin Type	Function Des.
1	DMIC_CLK	CLK	D-MIC clock	6	EN	Power	EN_3.3V
2	DMIC_DATA	Data	D-MIC data	7	VCC	Power	Cam_5V
3	GND	GND	GND	8	GND	GND	GND
4	MIC_VCC	Power	MIC_3.3V	9	D+	Data	USB_DP
5	NC	NC	NC	10	D-	Data	USB_DM

MICRO-STAR INT'L CO.,LTD.

Title: LED / Camera

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CPU STAND OFF

Delete UME1 for thermal solution change #2018.09.06

UME15 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N

0B. Unstuffed Mylar for EVT by PM request #2018.11.13

MYL2 Mylar MYLAR,FR283,64*25.5*0.15mm E2P-0112911-G40

MYL22 GASKET GASKET E2Y-X027311-CA7

0B. Add Gasket MYL22 (E2Y-X027311-CA7) by EMI request #2018.11.13

UME14 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N

UME5 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N

Change CPU & GPU stand off to 16S1 type by ME request #2018.09.18

MYL3 RUBBER RUBBER E2Y-6K21111-Y40

MYL4 RUBBER RUBBER E2Y-6K21111-Y40

MYL5 RUBBER RUBBER E2Y-6K21111-Y40

MYL6 RUBBER RUBBER E2Y-6K21111-Y40

MYL7 GASKET GASKET E2Y-X007111-CA7

MYL8 GASKET GASKET E2Y-X007111-CA7

MYL9 FOIL FOIL E2M-4B10711-G40

MYL10 FOIL FOIL E23-1047010-G40

Add E2Y-6K21111-Y40 *4, E2Y-X007111-CA7 *2, E2M-4B10711-Y42, E23-1047010-G40 for ME. 20180306

Change MYL9 from E2M-4B10711-Y42 to E2M-4B10711-G40 for ME. 20180330

UME24 H_R276D118_N UME4 H_R276D118_N UME9 H_R276D118_NH UME3 H_R276D118_N UME13 H_R276D118_N UME8 H_R276D118_N

UME2 H_R276D118_N UME10 H_R276D118_N UME19 H_R276D118_N

SPRING1 X_E23-1004060-CA7 SPRING2 X_E23-1004060-CA7

MYL16 Mylar MYLAR,6*3*1.2mm E2P-6F31611-G40

MYL17 Mylar MYLAR,6*3*1.2mm E2P-6F31611-G40

MYL18 Mylar MYLAR,6*3*1.2mm E2P-6F31611-G40

Add E2P-6F31611-G40 *3 for UMA sku by ME. 20180522

GPU STAND OFF

UME7 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N

UME6 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N

UME12 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N

UME11 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N

MYL11 TAPE CONDUCTION_TAPE,5*5*0.13mm E2Y-X043011-G40

MYL12 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40

MYL13 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40

MYL14 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40

MYL15 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40

Add E2Y-X043011-G40 *1, E2P-4B11711-G40 *3 for PM. 20180316

UME17 NPTH_98 UME1 NPTH_98 UME20 NPTH_98 X1 H_NR118D118 X2 H_NR118D118 X4 H_NR118D118 X3 H_NR118D118

0B. Unstuffed Mylar for EVT by PM request #2018.11.13

Add LABEL1(Y01-RHDMI03-000), LABEL2(G51-N1CO041-A09). 20180130

LABEL2 BIOS LABEL BIOS_LABEL G51-N1CO041-A09

LABEL1 HDMI ROYALTY Certificated HDMI_ROYALTY_0.04 Y01-RHDMI03-000

+PWR_SRC

EC2 X_C0.1u25X50402-HF

EC21 X_C0.1u25X50402-HF

EC27 X_C0.1u25X50402-HF

EC17 X_C0.1u25X50402-HF

EC16 X_C0.1u25X50402-HF

EC35 X_C0.1u25X50402-HF

EC1 X_C0.1u25X50402-HF

+5VSUS

EC72 X_C0.1u25X50402-HF

EC73 X_C0.1u25X50402-HF

EC74 X_C0.1u25X50402-HF

+3VRUN

Reserve +5VSUS 0402 0.1u cap *3 to GND by EMI request #2018.09.17

EC75 X_C0.1u25X50402-HF

Reserve +3VRUN 0402 0.1u cap *1 to GND by EMI request #2018.09.17

Change UME23, UME14, UME15 footprint to H_R276D118_V5_N for Layout. 20171030

UME21 H_R276D118_V5_N UME25 H_R276D118_V5_N UME18 H_R276D118_V5_N UME16 H_R276D118_V8_N UME22 H_R276D118_V8_N

MYL19 Mylar MYLAR,73*10*1.3T E2P-4B12611-Y42

MYL20 Mylar MYLAR,15*10*1.3T E2P-4B12511-Y42

MYL21 Mylar MYLAR,15*10*1.3T E2P-4B12511-Y42

Add E2P-4B12611-Y42 *1, E2P-4B12511-Y42*2 for UMA sku by ME. 20180712

PCB1 PD0-14B310B-H73 PD0-14B310B-H73

0B.Change PCB P/N to PD0-14B310B-H73 #2018.11.13

+5VRUN EC34 X_C0.1u25X50402-HF

FM3 FM13 FM11 FM4 FM17 FM25 FM26 FM14 FM18 FM7 FM19 FM23 FM24 FM6 FM20 FM8 FM16 FM27 FM5 FM21 FM9 FM1 FM22 FM10 FM2 FM12 FM15

Single 40 Ohm

J20 L1_4.5mil_40_Ohm_G2 GND2

J10 L3_3.5mil_40_Ohm_G2G4 GND2GND4

J17 L10_3.5mil_40_Ohm_G9G11 GND9GND11

J15 L12_4.5mil_40_Ohm_G11 GND11

Single 50 Ohm

J21 L1_3mil_50_Ohm_G2 GND2

J11 L3_2.5mil_50_Ohm_G2G4 GND2GND4

J4 L5_2.5mil_50_Ohm_G4G6 GND4GND6

J19 L10_2.5mil_50_Ohm_G9G11 GND9GND11

J14 L12_3mil_50_Ohm_G11 GND11

River #2018.09.10

Single 45 Ohm

J9 L1_4mil_45_Ohm_G2 GND2

J13 L3_3mil_45_Ohm_G2G4 GND2GND4

Differential 100 ohm

J7 L1_DIFF_2.5/7/2.5_100_Ohm+_G2 L1_DIFF_2.5/7/2.5_100_Ohm-_G2 GND2 GND2 X_H1X2_black

J2 L12_DIFF_2.5/7/2.5_100_Ohm+_G11 L12_DIFF_2.5/7/2.5_100_Ohm-_G11 GND11 GND11 X_H1X2_black

Differential 85 ohm

J22 L1_DIFF_3.5/5.5/3.5_85_Ohm+_G2 L1_DIFF_3.5/5.5/3.5_85_Ohm-_G2 GND2 GND2 X_H1X2_black

J12 L3_DIFF_3.5/5.5/3.5_85_Ohm+_G2G4 L3_DIFF_3.5/5.5/3.5_85_Ohm-_G2G4 GND2GND4 GND2GND4 X_H1X2_black

J5 L5_DIFF_3.5/5.5/3.5_85_Ohm+_G4G6 L5_DIFF_3.5/5.5/3.5_85_Ohm-_G4G6 GND4GND6 GND4GND6 X_H1X2_black

J1 L10_DIFF_3.5/5.5/3.5_85_Ohm+_G9G11 L10_DIFF_3.5/5.5/3.5_85_Ohm-_G9G11 GND9GND11 GND9GND11 X_H1X2_black

J16 L12_DIFF_3.5/5.5/3.5_85_Ohm+_G11 L12_DIFF_3.5/5.5/3.5_85_Ohm-_G11 GND11 GND11 X_H1X2_black

Differential 80 ohm

J8 L1_DIFF_3.5/3.5/3.5_80_Ohm+_G2 L1_DIFF_3.5/3.5/3.5_80_Ohm-_G2 GND2 GND2 X_H1X2_black

J6 L3_DIFF_3.5/3.5/3.5_80_Ohm+_G2G4 L3_DIFF_3.5/3.5/3.5_80_Ohm-_G2G4 GND2GND4 GND2GND4 X_H1X2_black

J18 L10_DIFF_3.5/3.5/3.5_80_Ohm+_G9G11 L10_DIFF_3.5/3.5/3.5_80_Ohm-_G9G11 GND9GND11 GND9GND11 X_H1X2_black

J3 L12_DIFF_3.5/3.5/3.5_80_Ohm+_G11 L12_DIFF_3.5/3.5/3.5_80_Ohm-_G11 GND11 GND11 X_H1X2_black

ST1 STAND UMA X_E2B-13F2020-RH E2B-13F2020-A89

Add E2B-13F2020-A89 *1 for UMA Sku by ME. 20180713

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Title: ME,EMI

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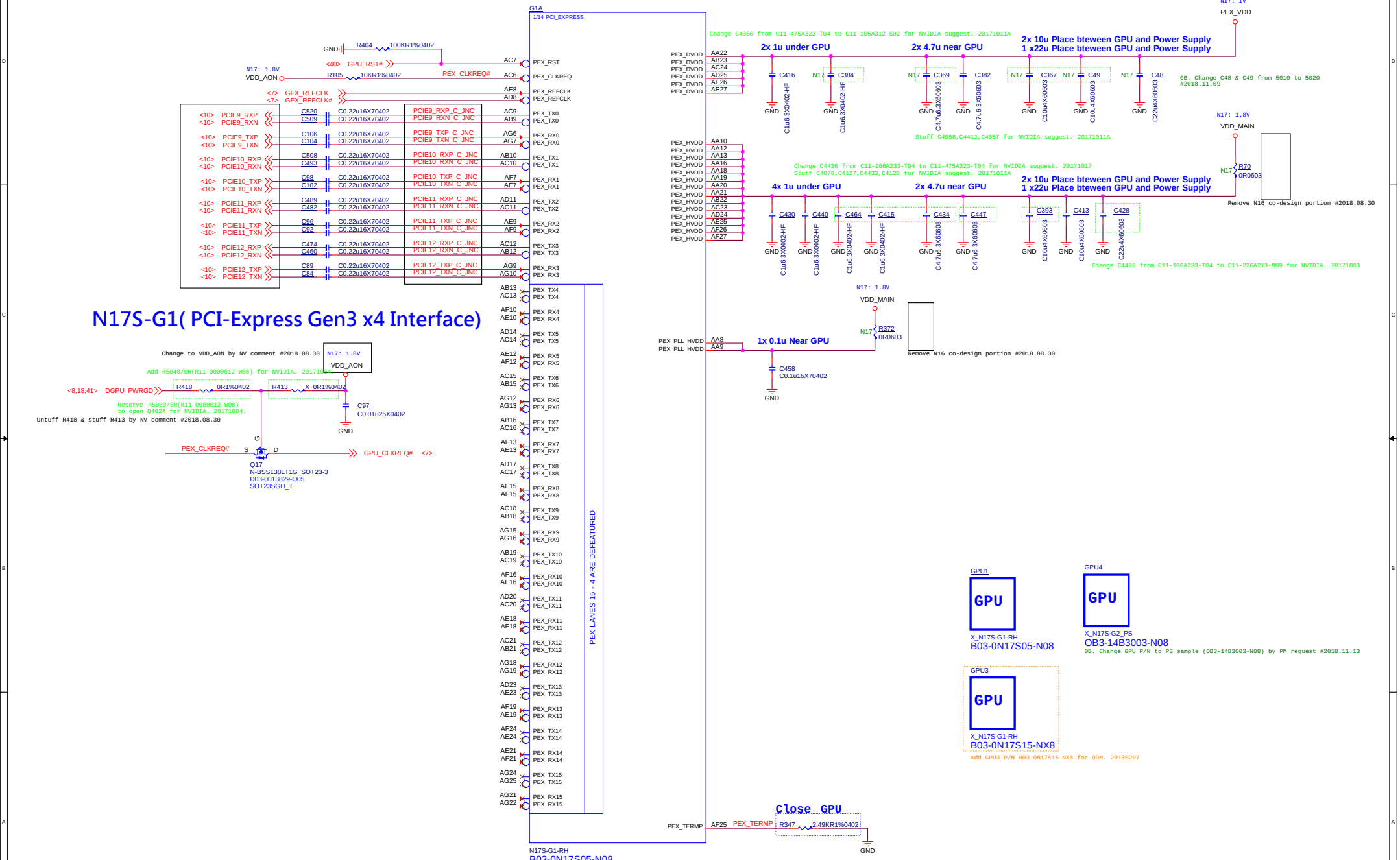
N17S-G1(PCI-Express Gen3 x4 Interface)



MICRO-STAR INT'L CO.,LTD.	
Title	N17S-G1 PCI-E Host
Size: Custom	Document Number: MS-14B3
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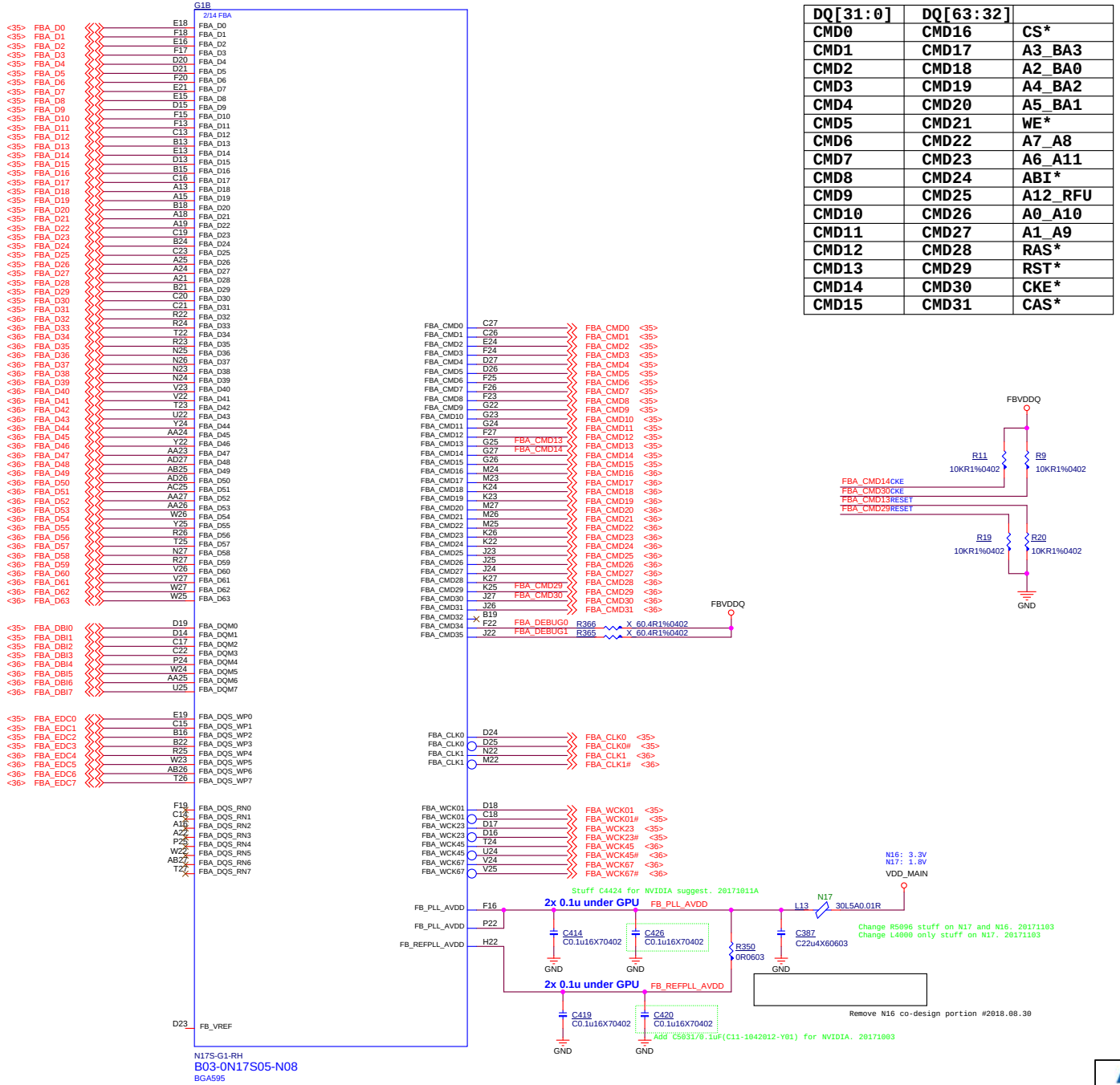
N17S-G1(Frame Buffer Interface)

GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	N17S-G1 MEM IF-A		
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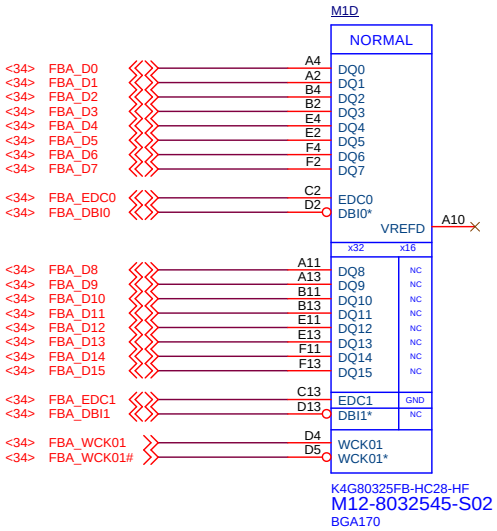
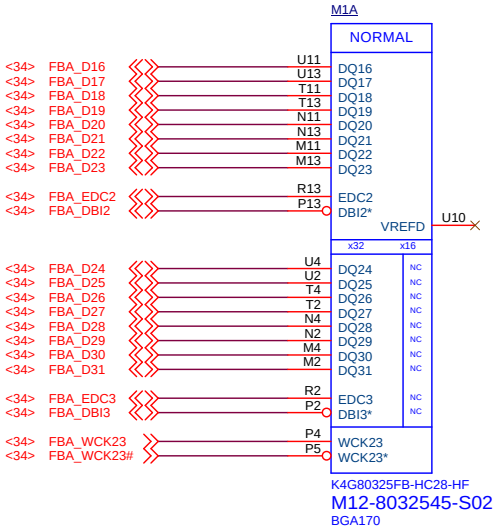
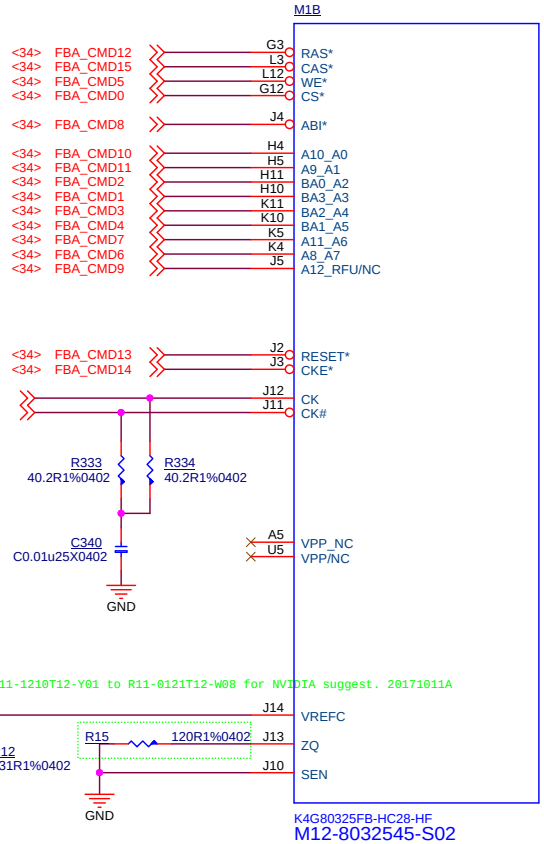
N17S-G1_GDDR5 Frame A-1

GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*







GDDR1

GDDR5

X_SAMSUNG/K4G80325FB-HC25

M12-8032535-S02

GDDR2

GDDR5

X_HYNIX/H5GC8H24AJR-R2C

M12-5GC8HB5-H23

GDDR5 SGRAM,8G(256Mx32bit)

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Title: N17S-G1_GDDR5 Frame A-1

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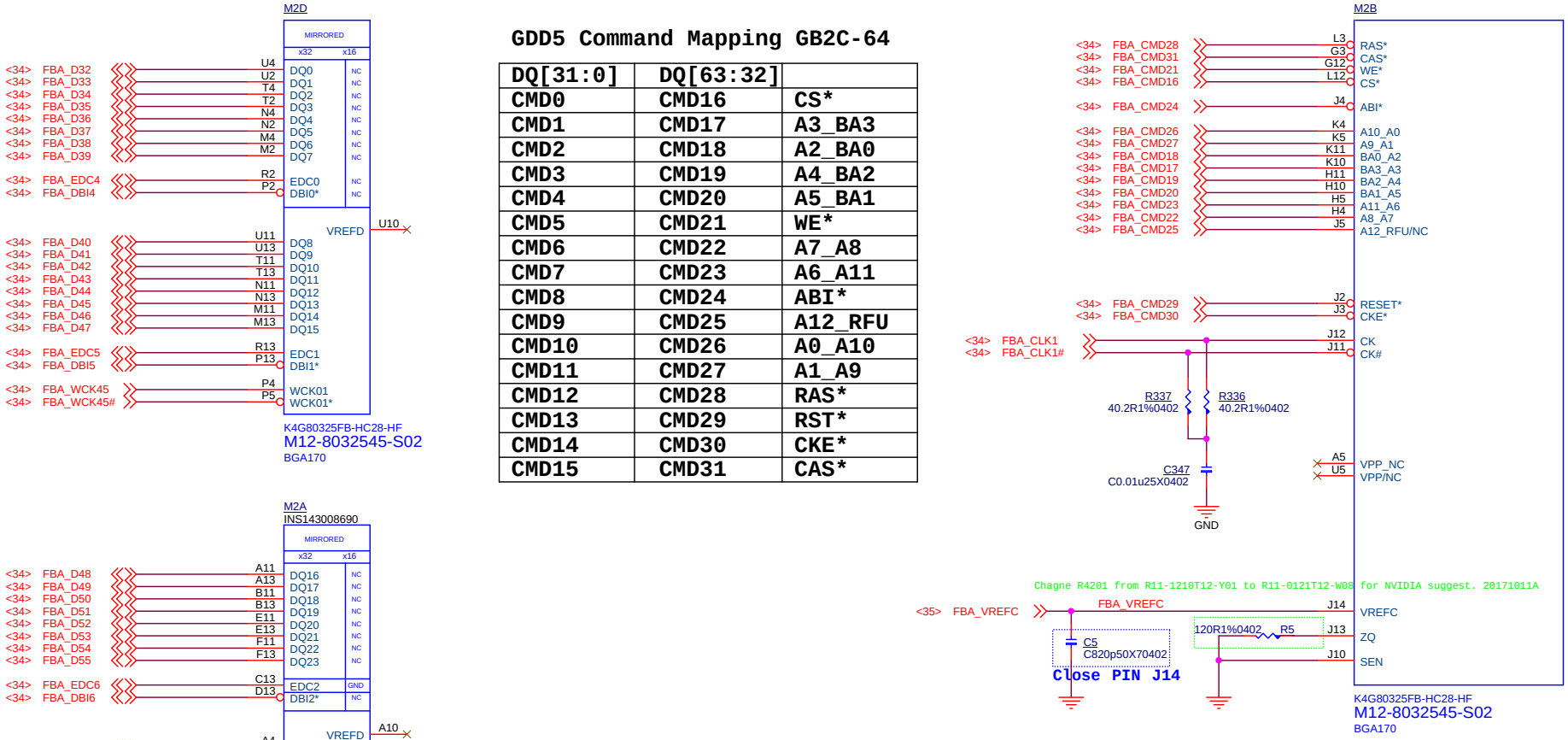
N17S-G1_GDDR5 Frame A-2



GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

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Title: N17S-G1_GDDR5 Frame A-2		
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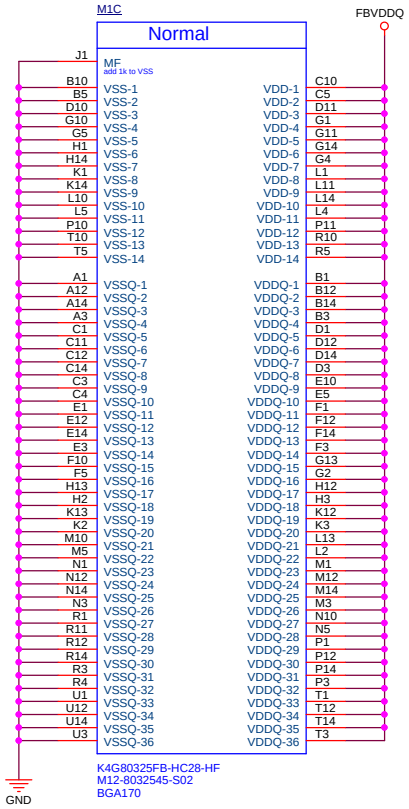
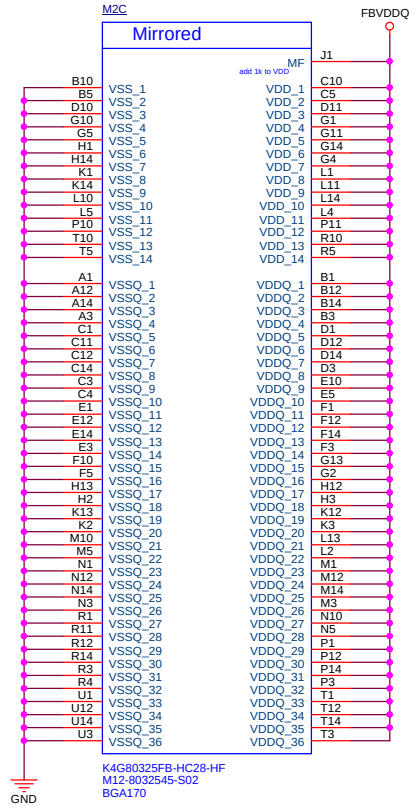
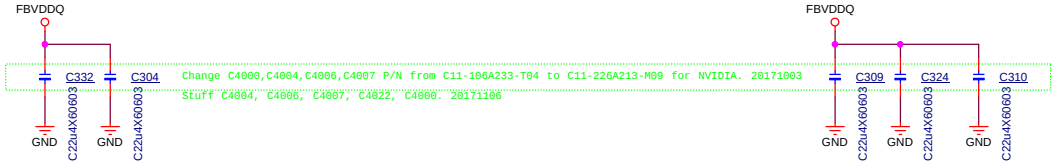
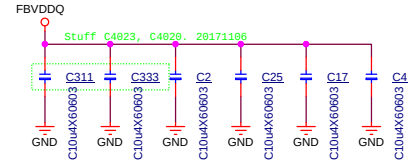
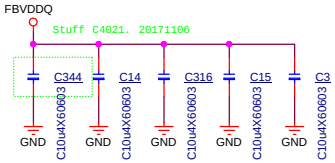
N17S-G1_GDDR5_DECOUPLING

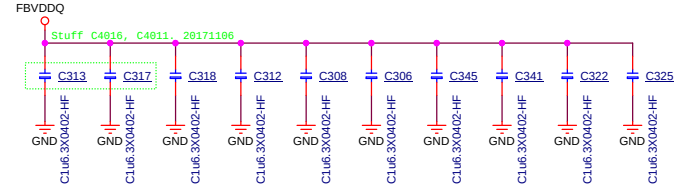


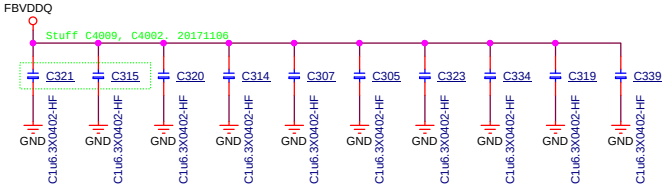












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Title: N17S-G1_GDDR5_DECOUPLING		
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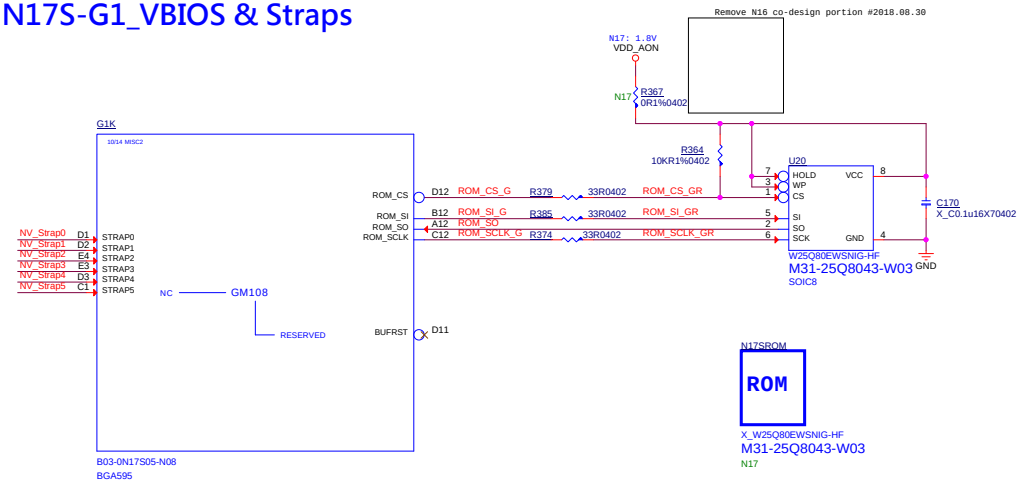
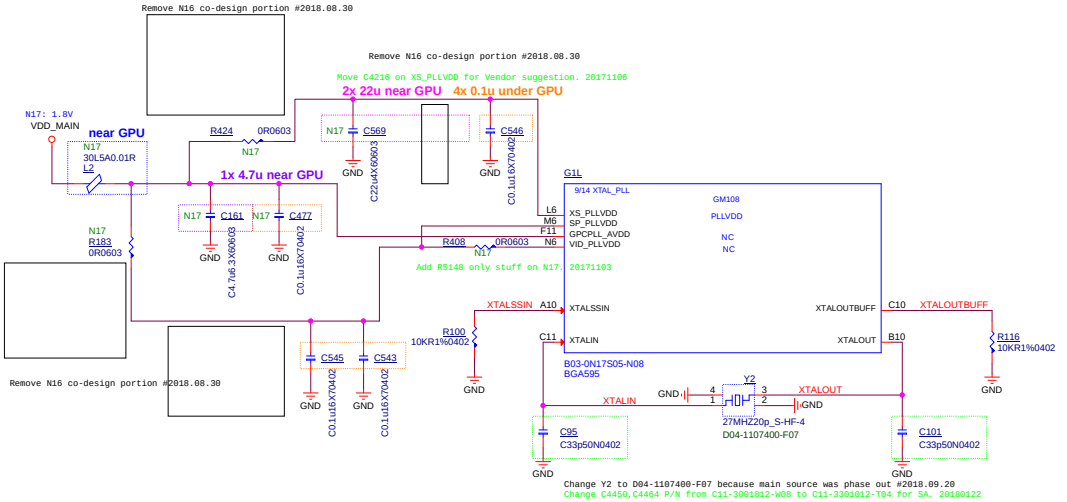
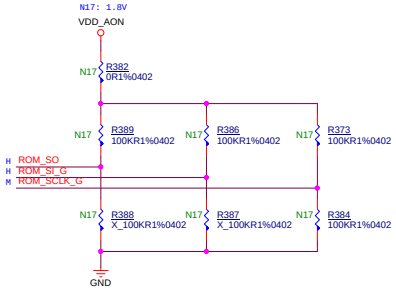
N17S-G1_VBIOS & Straps

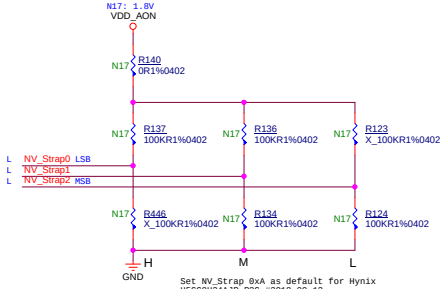






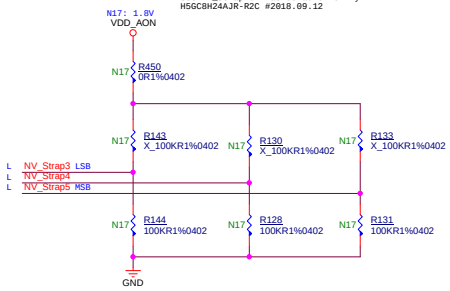
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	1:ENABLE	0:DISABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE

256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
	Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver[2]



STRAP 2	STRAP 1	STRAP 0		N17S-G1 3.0G RAM	
L	L	L	0x0	Samsung K4G80325FB-HC28	
L	L	H	0x1	Microm MT51J2256M32HF-70:A	256M*32
L	H	L	0x2	Hynix H5GC8H24MJR-R0C	
H	H	L	0x6	Hynix H5GC4H24AJR-R0C	
H	H	H	0x7	Samsung K4G41325FE-HC28	128M*32
L	L	M	0x8	Microm EDW4032BABG-70-F	

STRAP 2	STRAP 1	STRAP 0		N17S-G2 3.5G RAM	
L	M	L	0x9	MICRON MT51J256M32HF-80:B	256M*32
L	M	H	0xA	HYNIX H5GC8H24AJR-R2C	



STRAP 5	STRAP 4	STRAP 3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	Optimus
L	L	H	0	0	0	1	Discrete
H	L	H	0	1	0	1	Discrete with Gsync

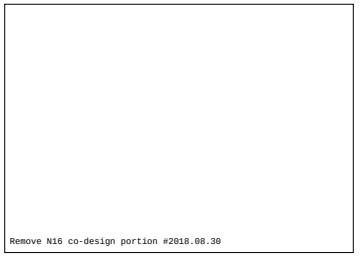


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 12. N16/GB2B-64 Multi-Level Straps

Strap Pin	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Stuff 49.9 kΩ pull-up to VDD_AON (3.3V).			
STRAP1	Reserved			
STRAP2	Reserved			
STRAP3	Reserved			
STRAP4	Reserved			

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Title: N17S-G1 VBIOS & Straps

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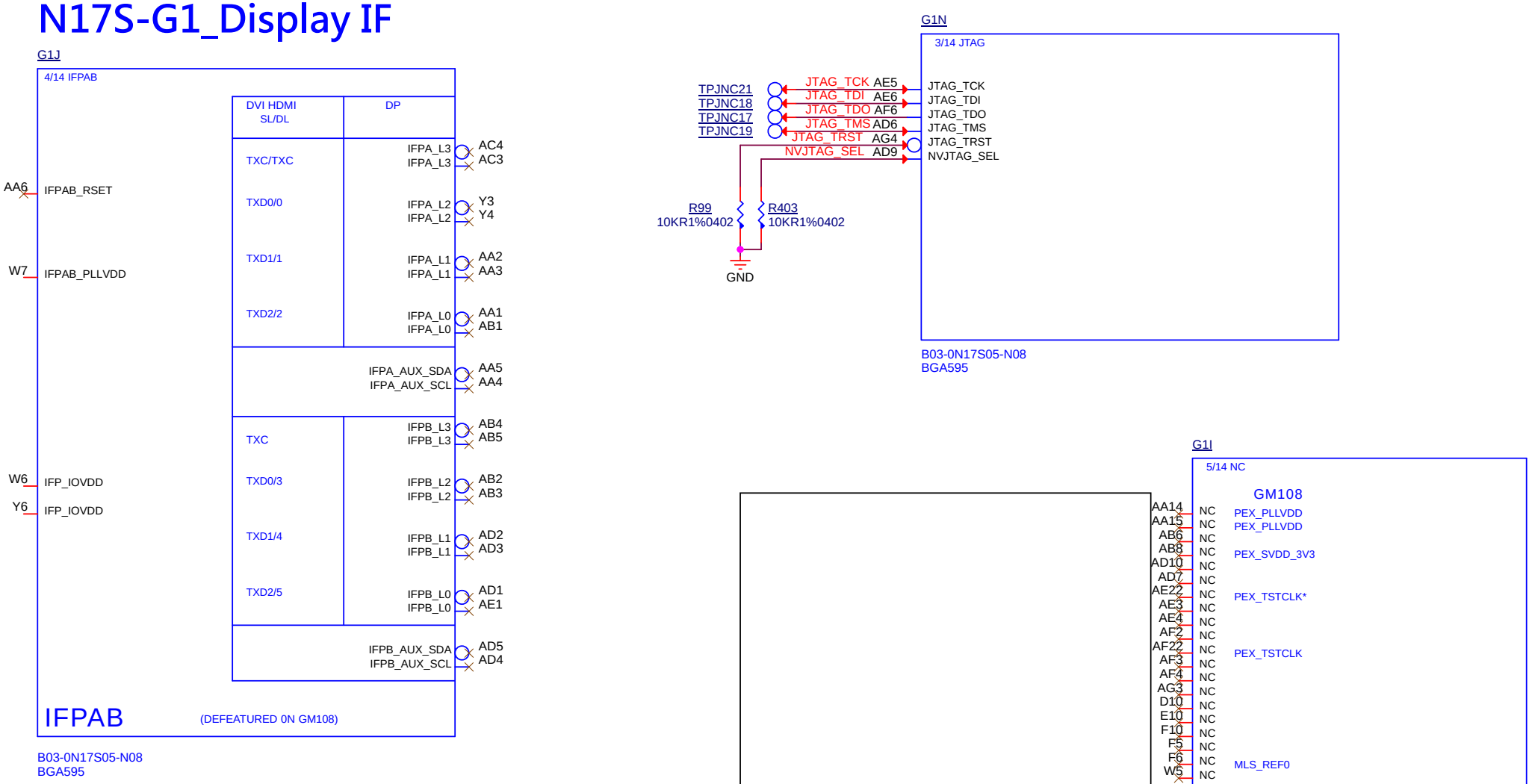
N17S-G1_Display IF



15.2 INTERFACE CONFIGURATION, CIRCUITRY, SAMPLE CIRCUITRY

To select different Strap Mode, MULTI_STRAP_REF0_GND pins need to be stuffed accordingly. Table 15-1 provides the necessary connections to set the correct strapping mode for each device.

Table 15-1. Device Specific Strap Mode Selection

	All N16x GPUs
Multi_Strap_Ref0_GND	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 40.2k 1% to GND

MICRO-STAR INT'L CO.,LTD.

Title: N17S-G1_Display IF

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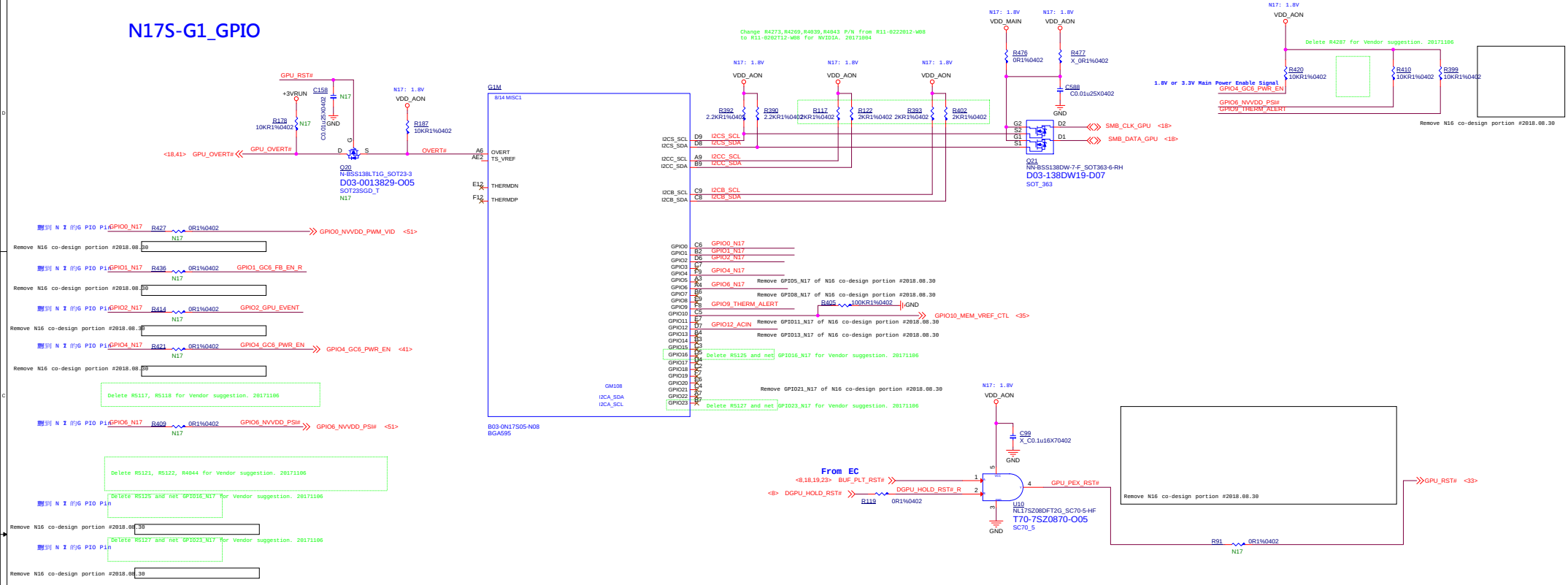
N17S-G1_GPIO



AC_OK#	GPU_ACIN1 (EC Ctrol)	GPIO12_GPU_ACIN
0	0	1
0	1	1
1	0	1
1	1	0

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	O	PWM Output To Contral NVVDD	0 TO 1V8 PWM Output
GPIO1	GC6M:GC6_FB_EN	O	FB Enable For GC6 2.1	Open Source 10K Pull-Down
GPIO2	GC6M:GC6_EVENT / WAKE	I	GPU Wake Signal For GC6 2.1	10K Pull-Up To 1V8_AON Unless Driven Actively
GPIO3	NVVDDS_PWM(NC)	I/O	PWM Output To Control The NVVDS Power Supply	0 TO 1V8 Output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU Power Sequencing For GC6 2.1	Open Drain 10K Pull-Up To 1V8_AON
GPIO5	FRM_LCK	I	Active Low Frame Lock	Open Drain 10K Pull-Up To 1V8_AON
GPIO6	NVVDD_PSI/NVVDDS_PSI	O	Phase Shedding	10K Pull-Up To 1V8_AON To Enable Multiple Phases
GPIO7	LCD_BL_PWM(NC)	O	Panel Backlight Enable	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	Pull-Up/Pull-Down To Set The FBVDD/Q Power ON Voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10K Pull-Up To 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD(NC)	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC Power Detect Or Power Supply Overdraw Input	10OK Pull-Up To 1V8_AON
GPIO13	LCD_BLEN(NC)	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA(NC)	I	Hot Plug Detect for IFPA	
GPIO15	HPD_IFPB(NC)	I	Hot Plug Detect for IFPB	
GPIO16	GC6M:SYS_PEX_RST_MON	I	System Side PCIE Reset Monitor	10K Pull-Up To 1V8_AON Unless Driven Actively
GPIO17	UNUSED(NC)	I/O		
GPIO18	UNUSED(NC)	I/O		
GPIO19	3D Vision(NC)	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE(NC)	I/O		
GPIO21	OC_WARN/HT	I	Over Current Throttling Trigger	10K Pull-Up To 1V8_AON
GPIO22	UNUSED(NC)	I/O		
GPIO23	GC6M:GPU_PEX_RST_HOLD	O	GPU PCIE Self Reset Control	Open Drain 10K Pull-Up To Gated 3V3

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Title: N17S-G1_GPIO

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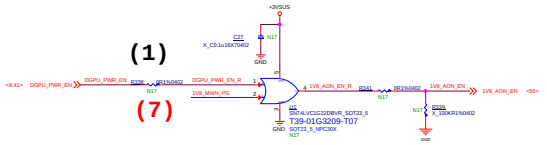
N17S-G1_Power Control

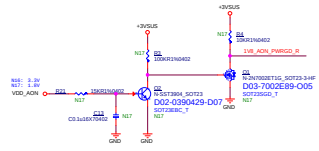
Power on = 1V8_AON -> (VDD_MAIN) 1V8_MAIN -> NVVDD+NVVDDS -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power down = PEX_VDD/FBVDDQ -> NVVDD+NVVDDS -> 1V8_MAIN -> 1V8_AON

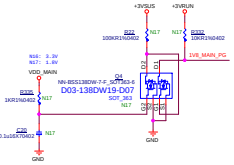
1V8_AON



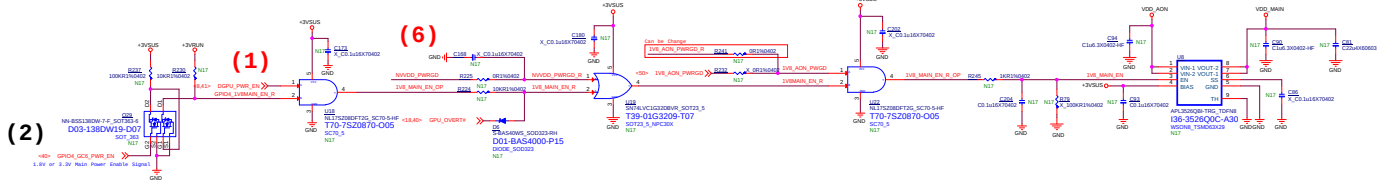
1V8_AON POWER GOOD



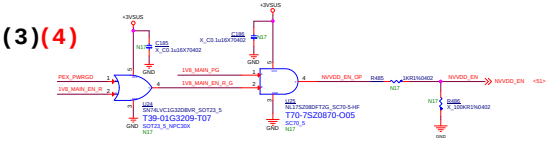
1V8_MAIN POWER GOOD



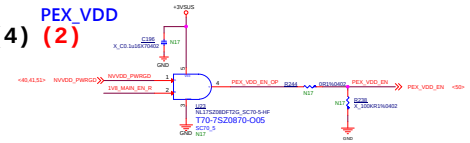
1V8_MAIN



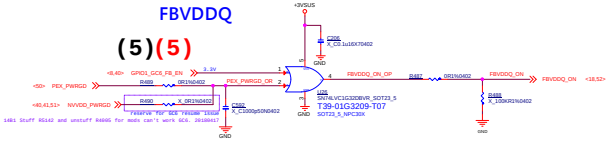
NVVDD



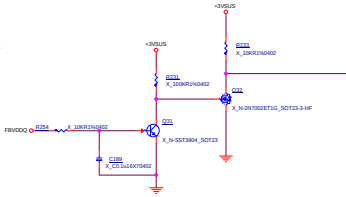
PEX_VDD



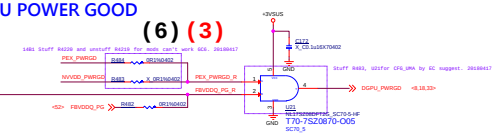
FBVDDQ



FBVDDQ POWER GOOD



DGPU POWER GOOD

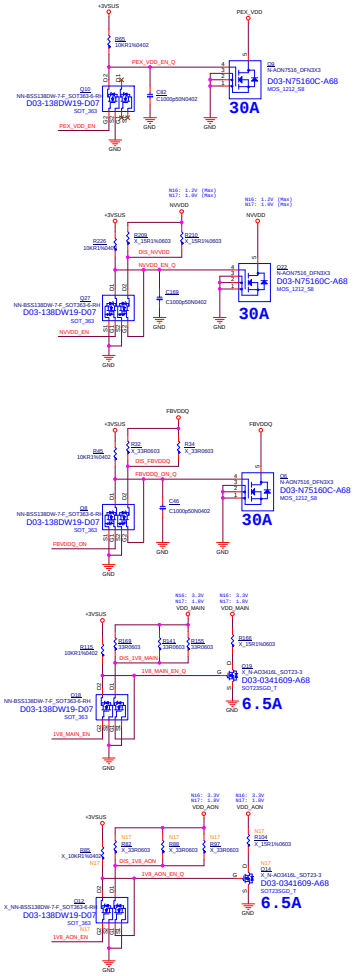


N16S_Power Control

Power on = 3V3_AON -> VDD_MAIN (3V3_MAIN) (3V3_NV) -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD

Remove N16 co-design portion #2018.08.30

Discharge Circuit



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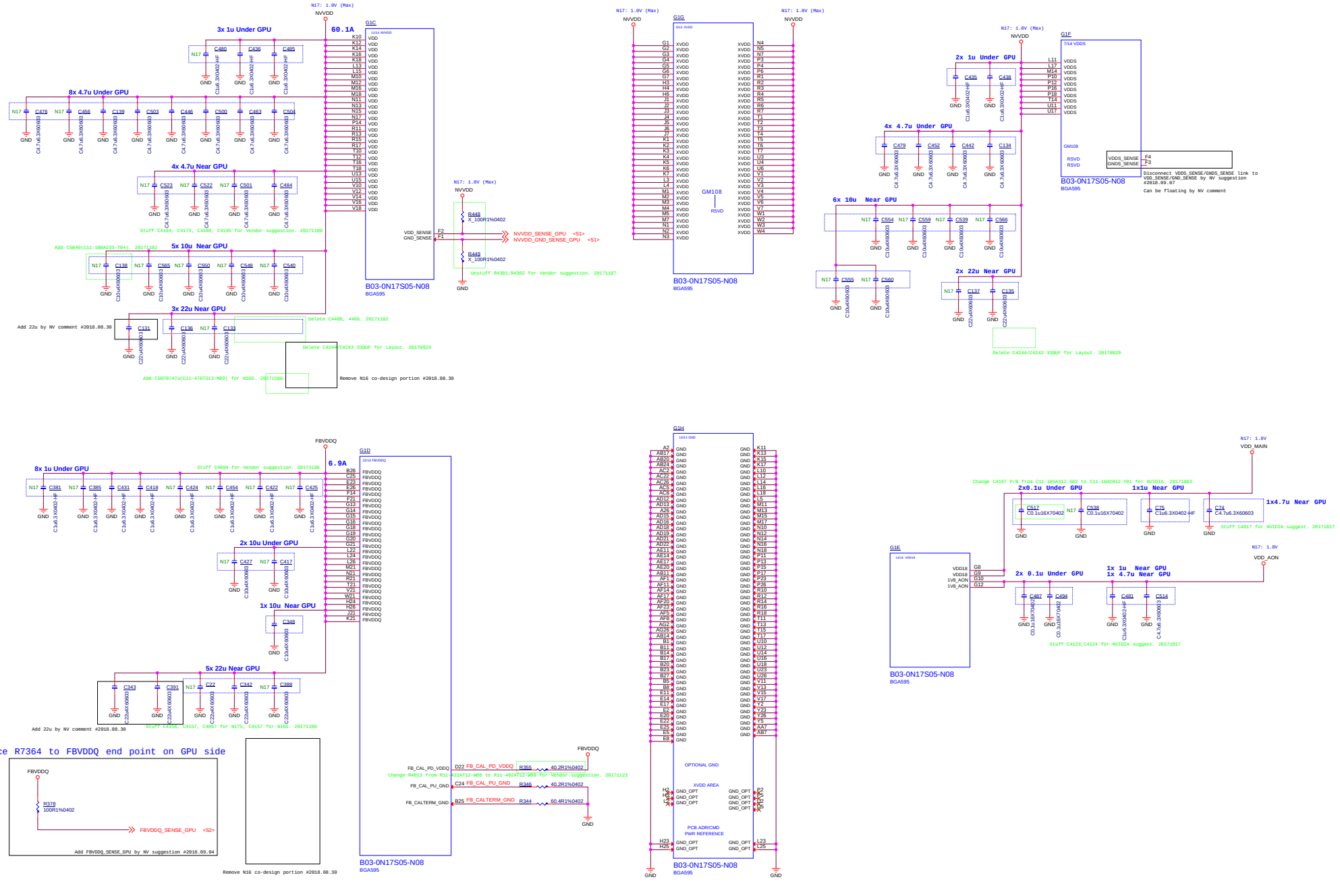
N17S-G1_Power Control

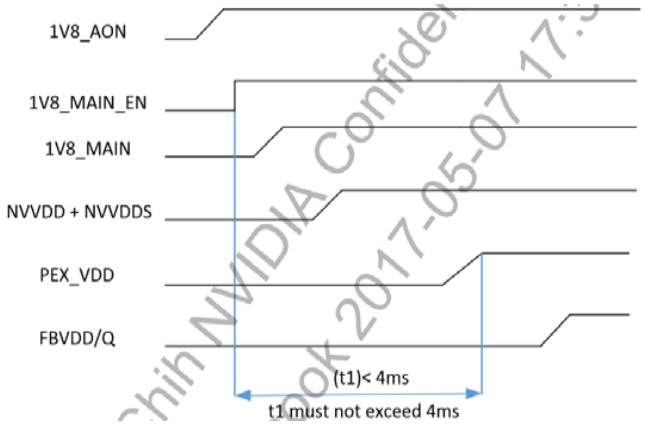
MS-14B3

0A

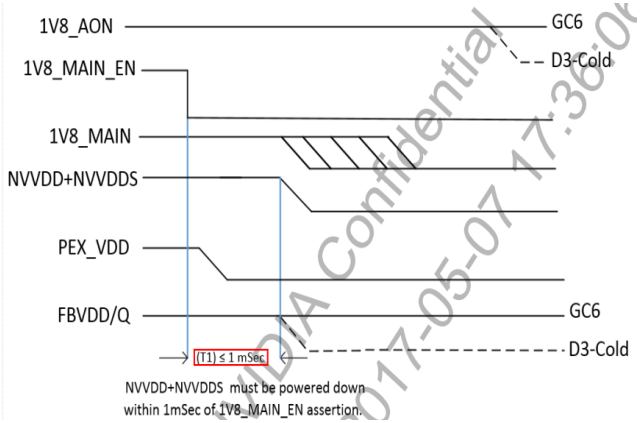
N17S-G1_Power & GND



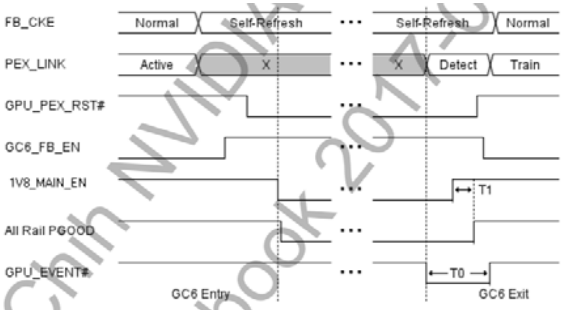
N17 Power Up



N17 Power Down



GC6 2.1



GC6 2.1 Entry/Exit Sequence Timing Diagram

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

N16 Power Up

Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.

GC6 2.0

18.3.4.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-14 and Table 18-3 describes the GC6 2.0 entry and exit sequence and timing requirements.

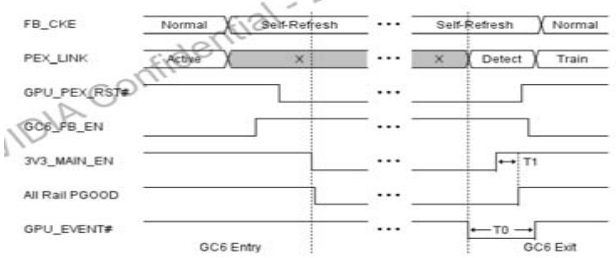


Figure 18-14. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:

- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

Optimus

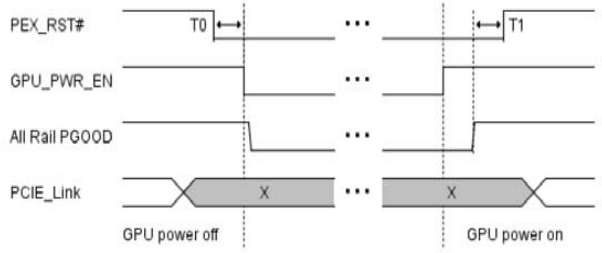
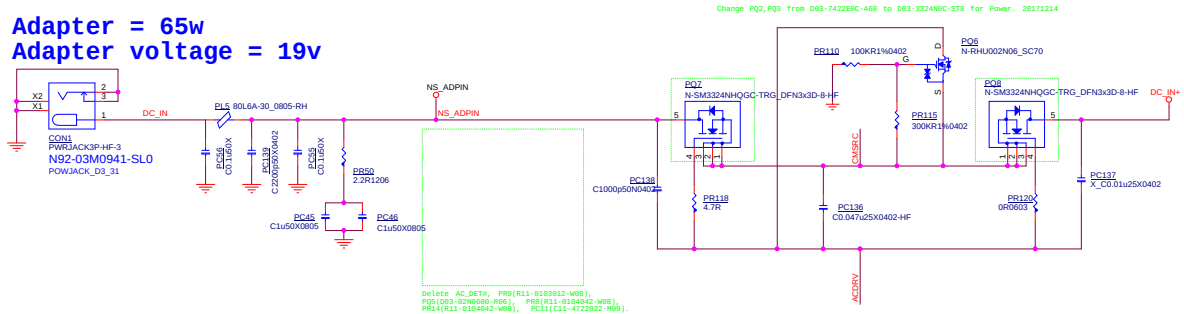


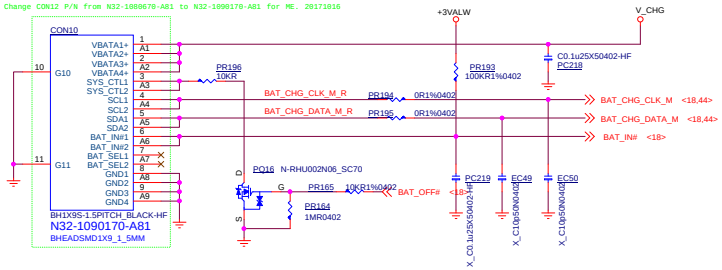
Figure 18-7. Optimus Entry/Exit Timing Diagram

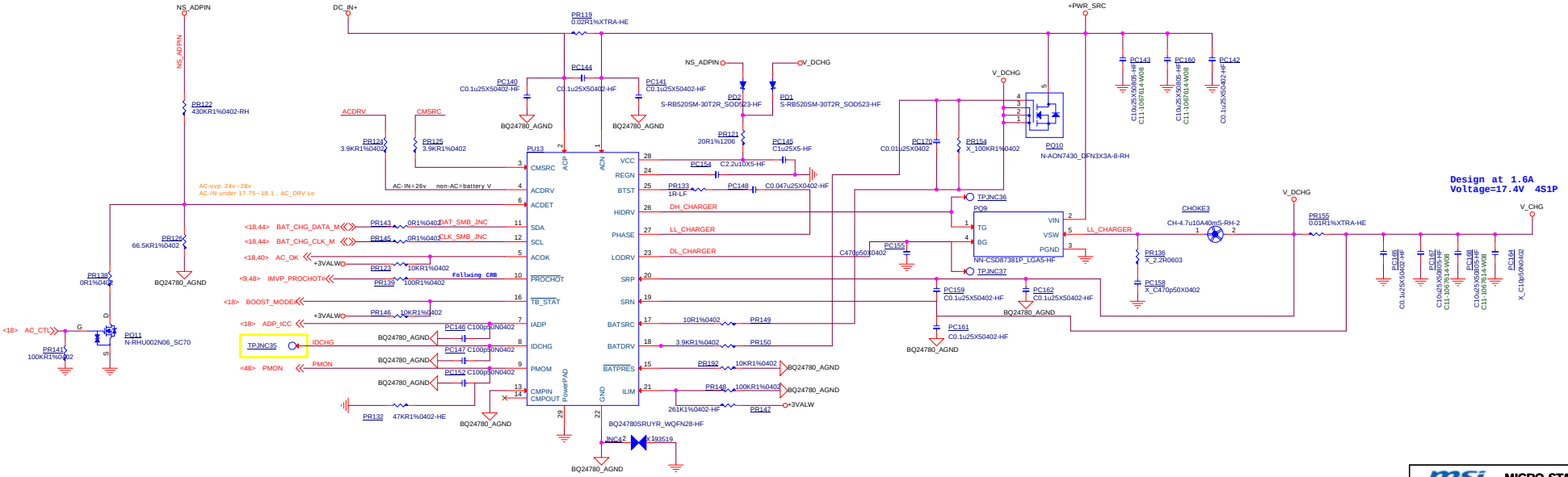
Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Adapter = 65w
Adapter voltage = 19v







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Title: **AC_IN & Battery charge**

Size: Custom | Document Number: **MS-14B3** | Rev: **0A**

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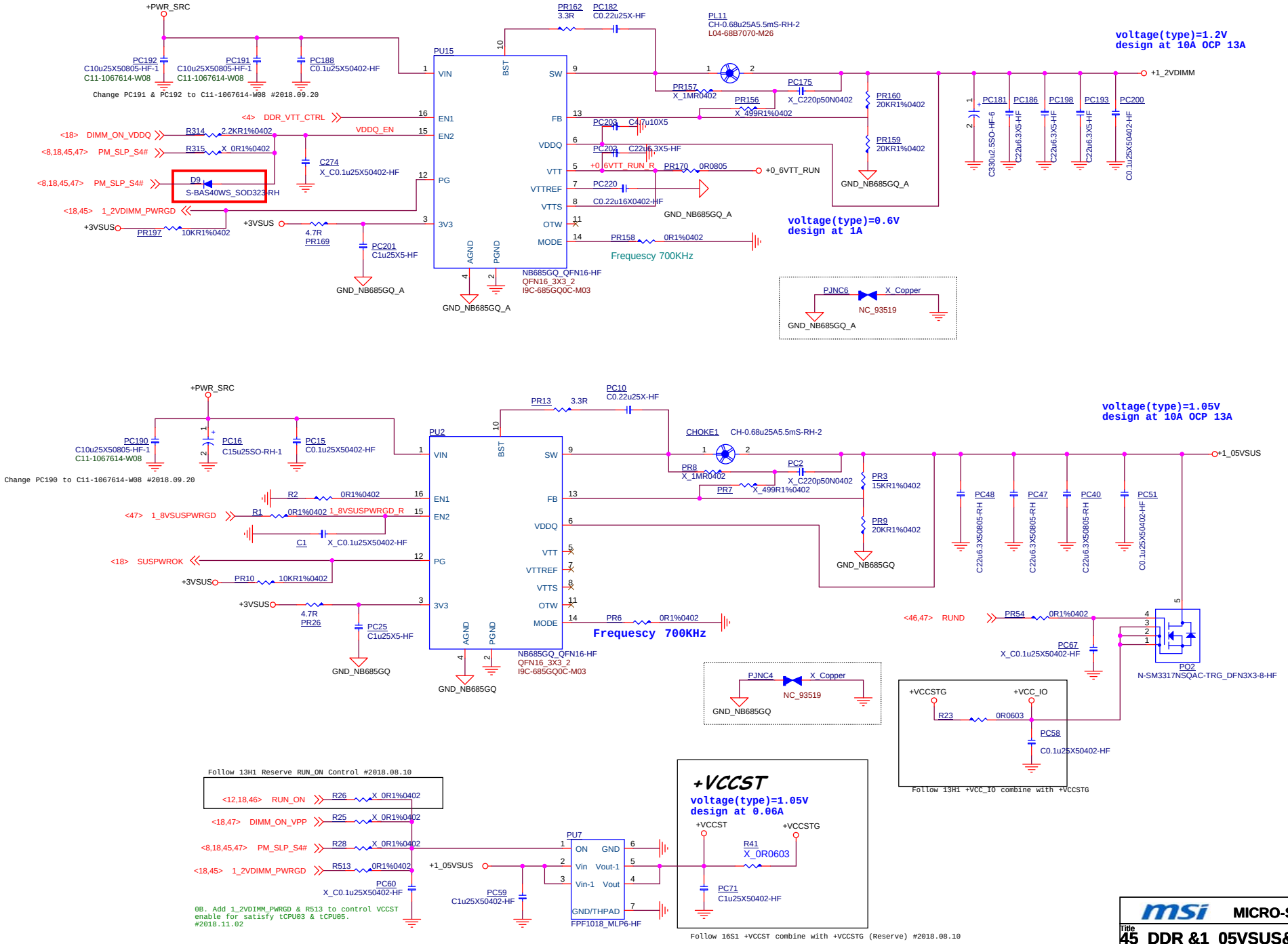

Title	45_DDR &1_05VSUS& VCCST & VCCIO
Size	Custom
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Date:	Friday, November 16, 2018
Sheet	45 of 57

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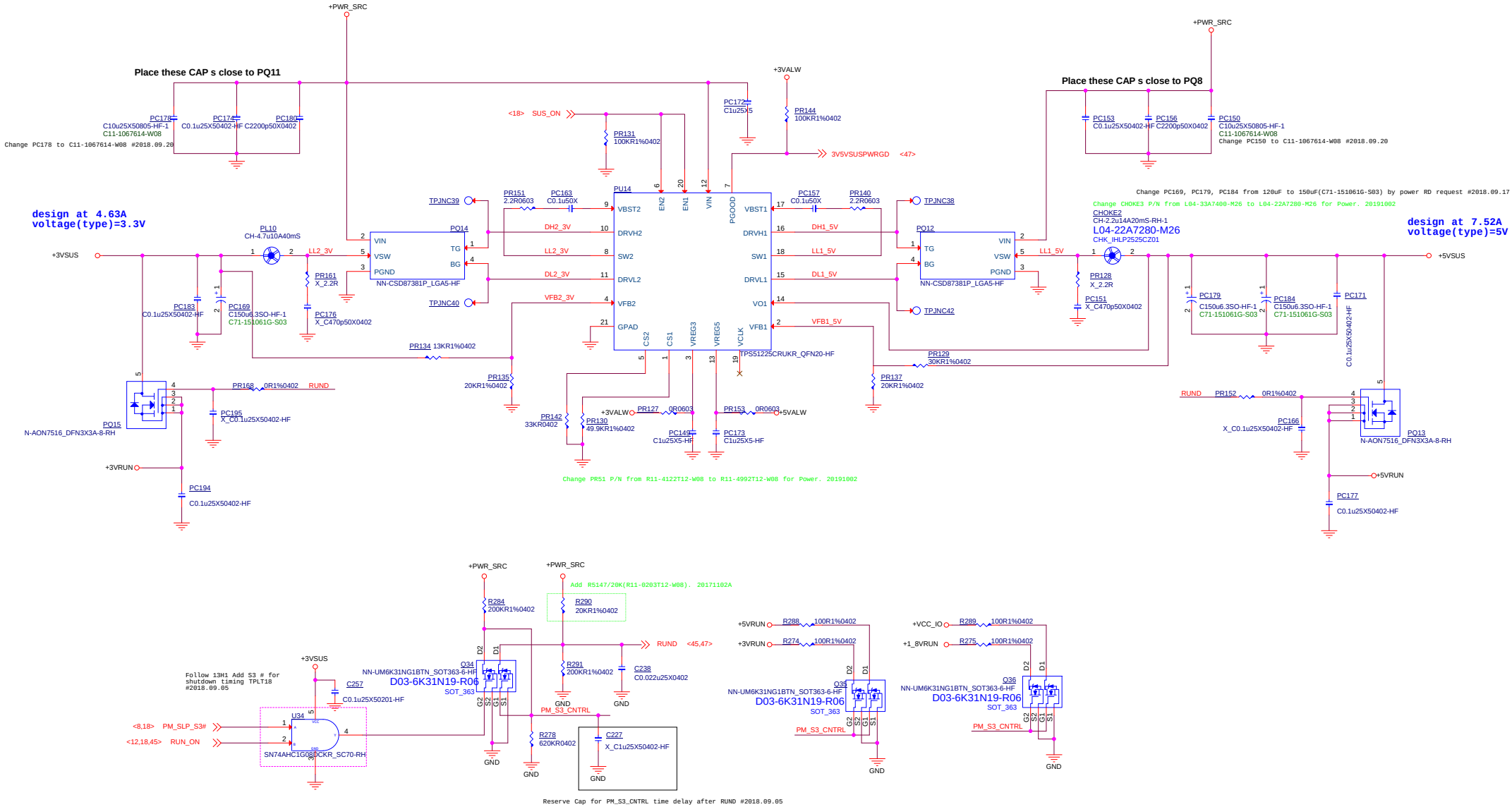

Title	System Power
Size	Custom
Document Number	MS-14B3
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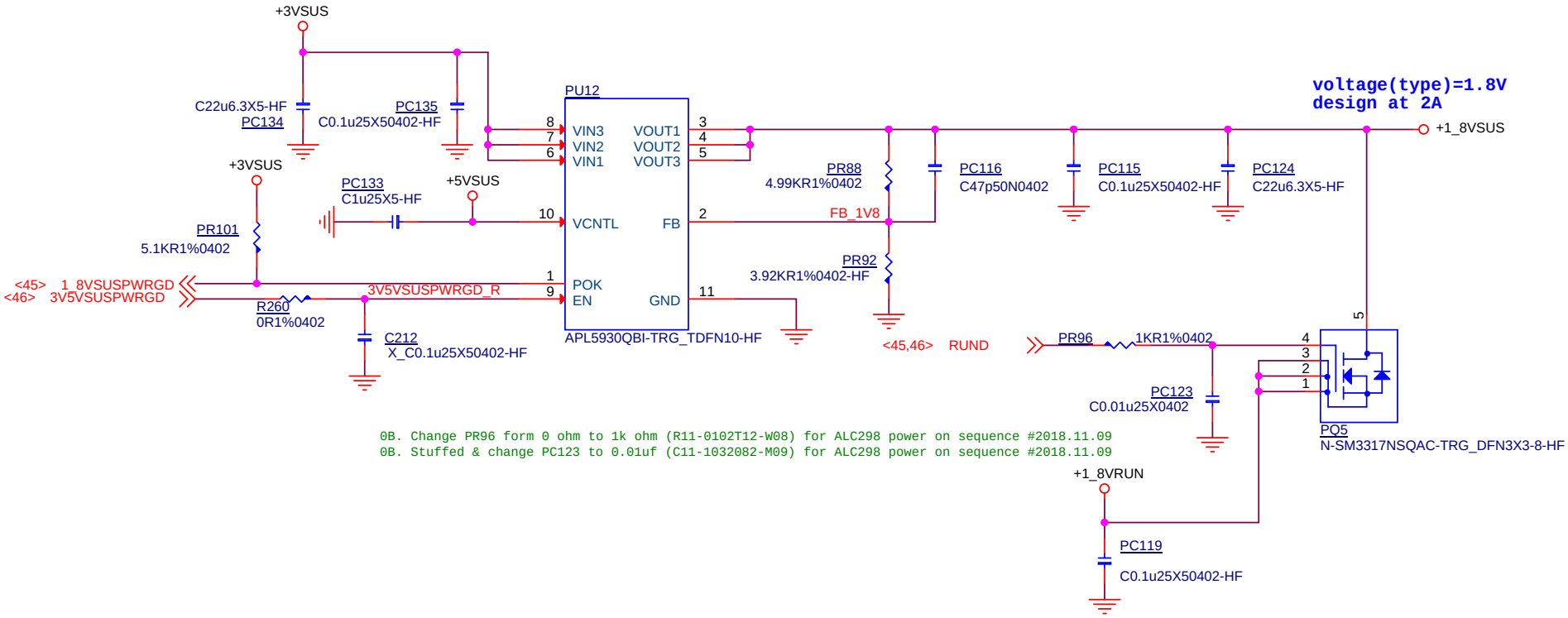

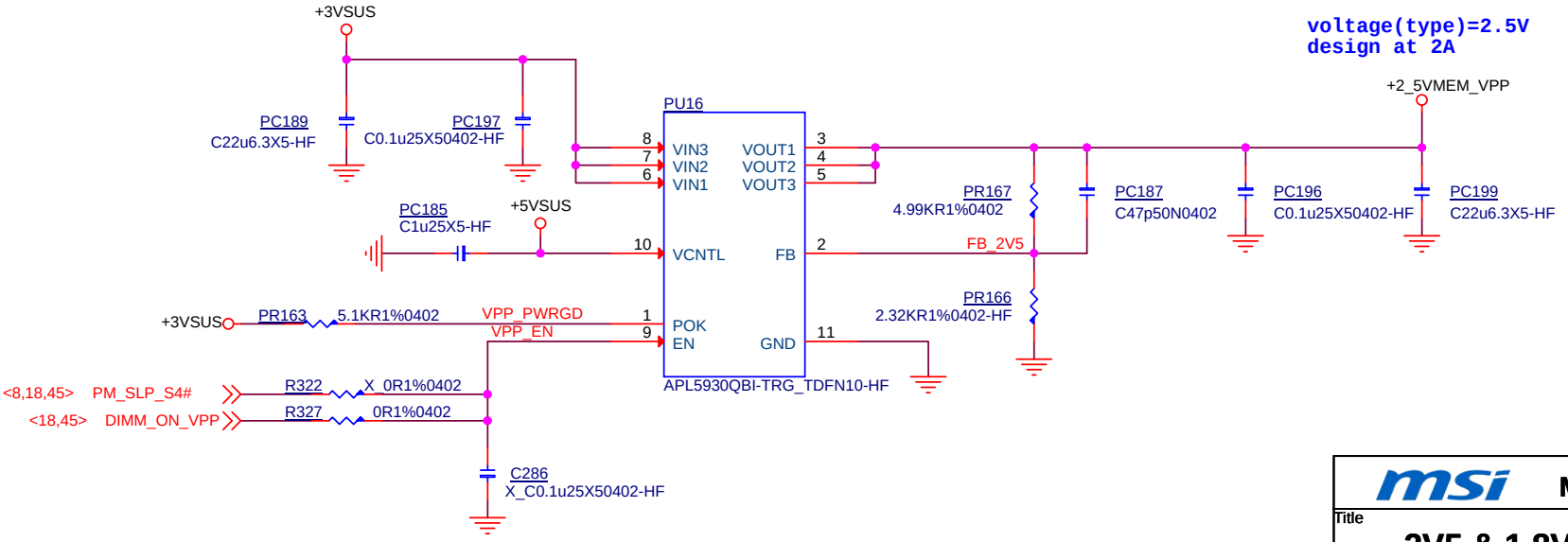

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Title: 2V5 & 1.8VSUS

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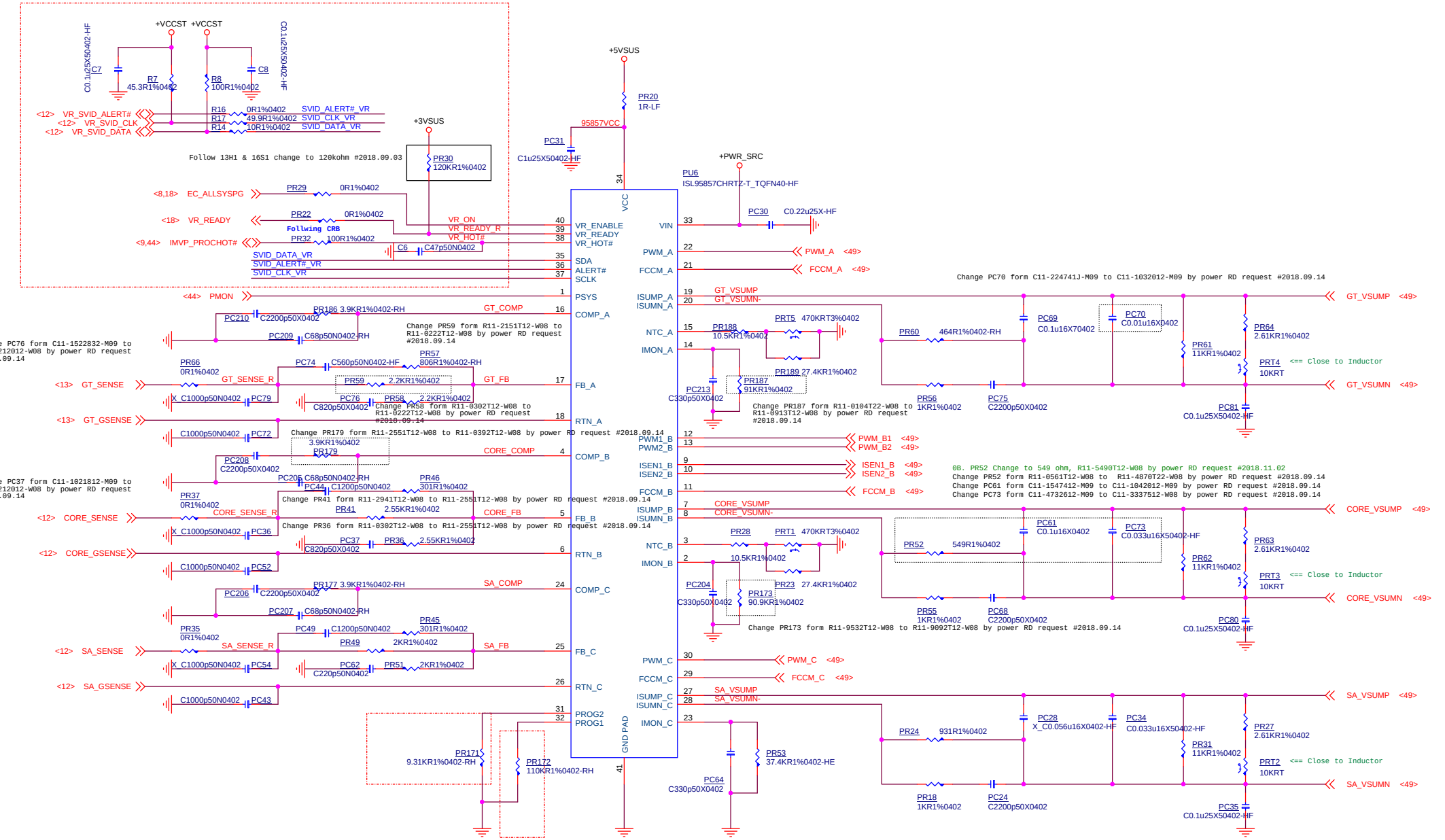

MICRO-STAR INT'L CO.,LTD.

Title: +VCC_CORE(1)

Size: Custom | Document Number: MS-14B3 | Rev: 0A

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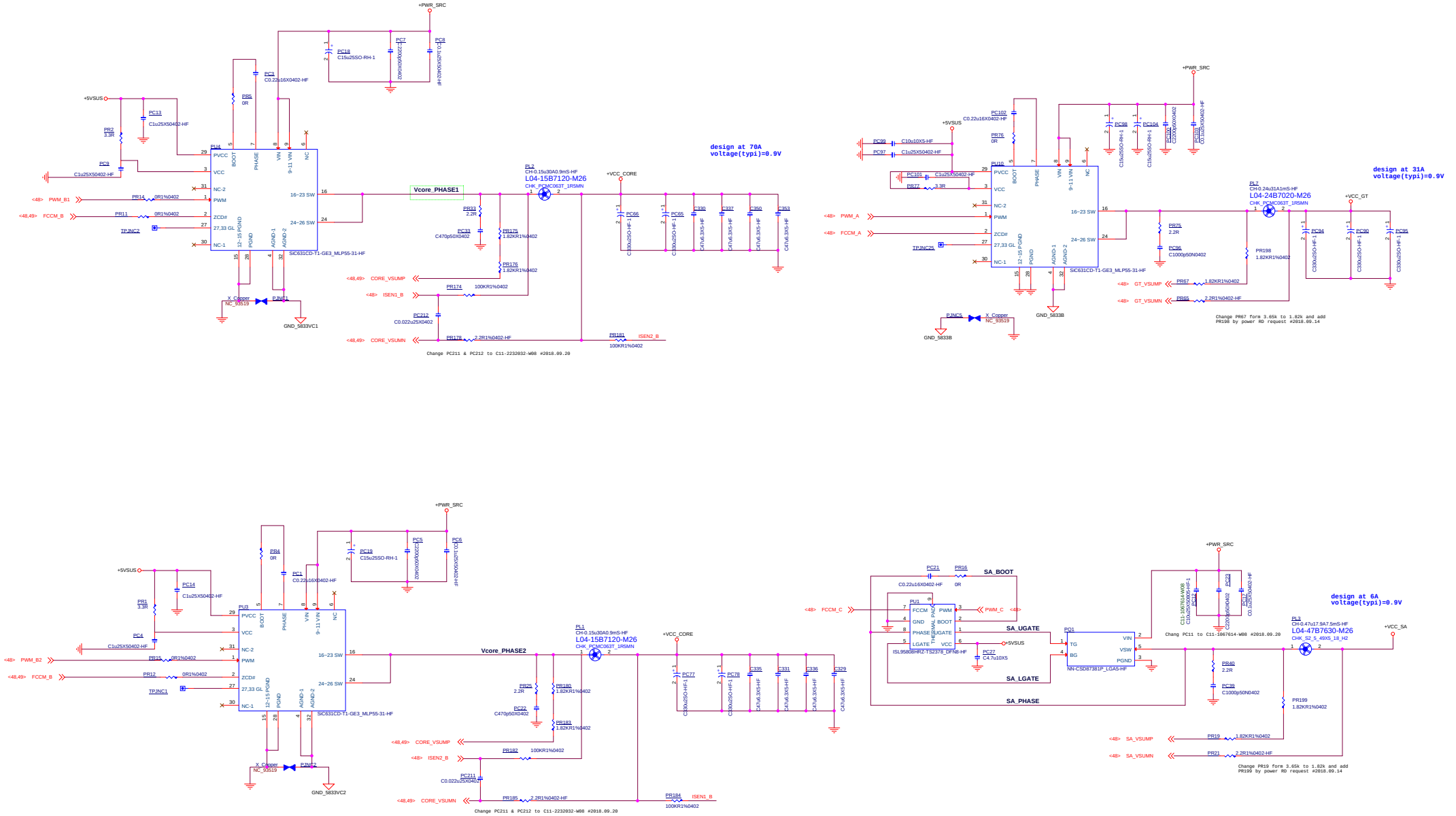

msi MICRO-STAR INT'L CO.,LTD.			
Title: +VCC_CORE(2)			
Size: Custom	Document Number: MS-14B3		Rev: 0A
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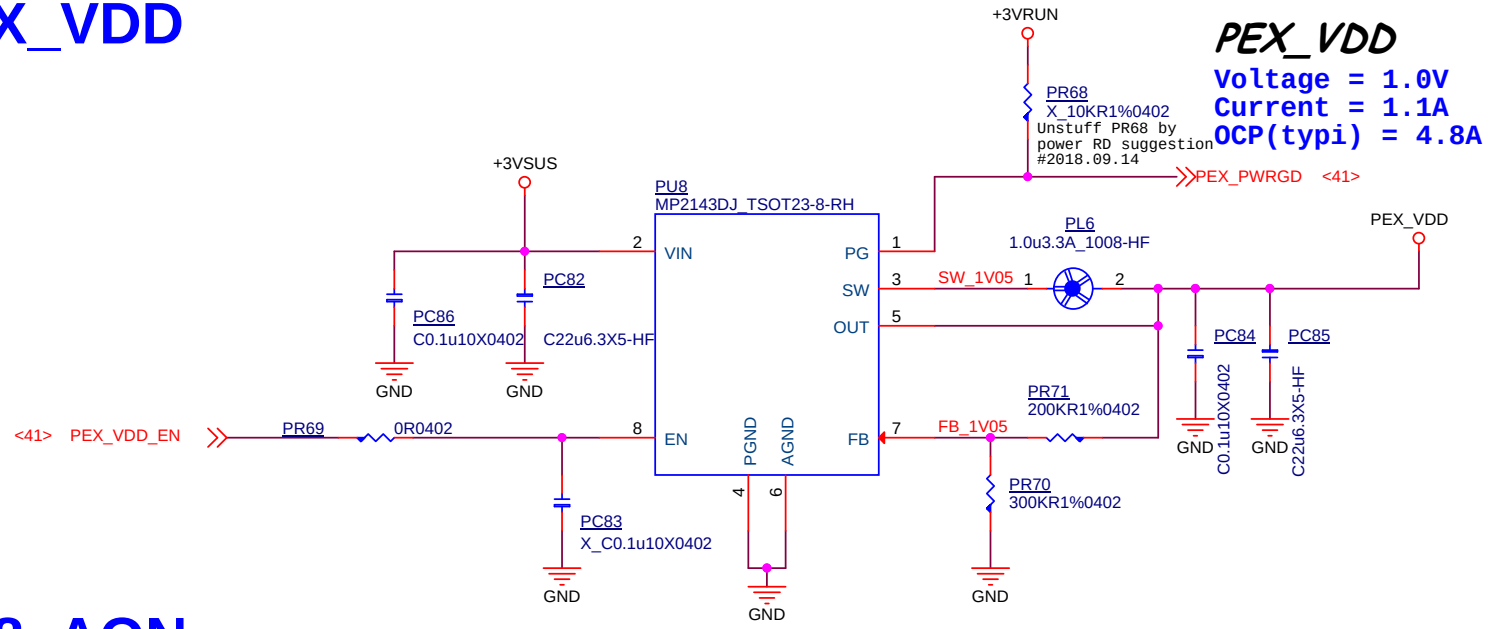
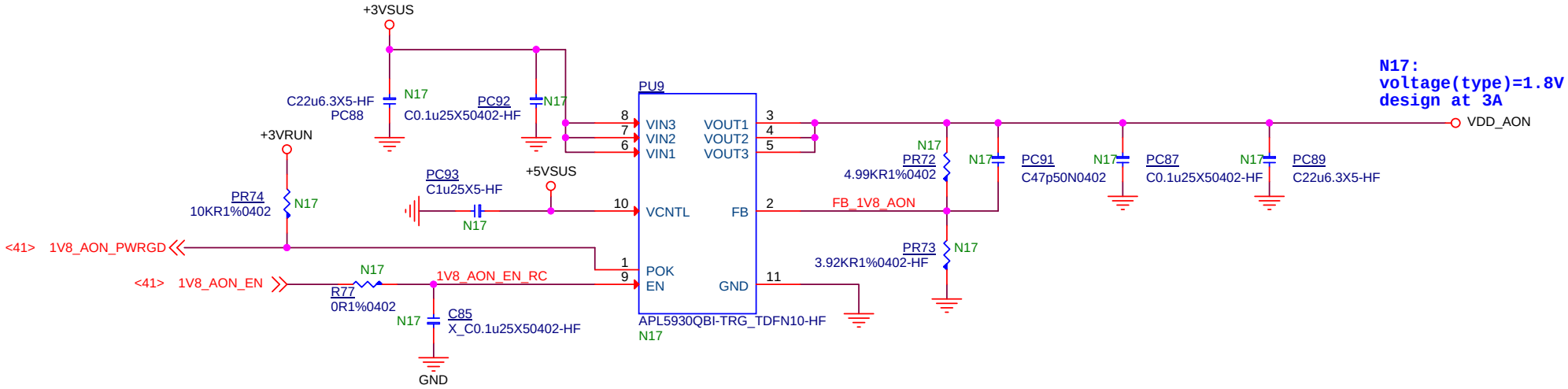
PEX_VDD



1V8_AON



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU POWER PEX_VDD/1V8_AON			
Size: Custom	Document Number: MS-14B3		Rev: 0A
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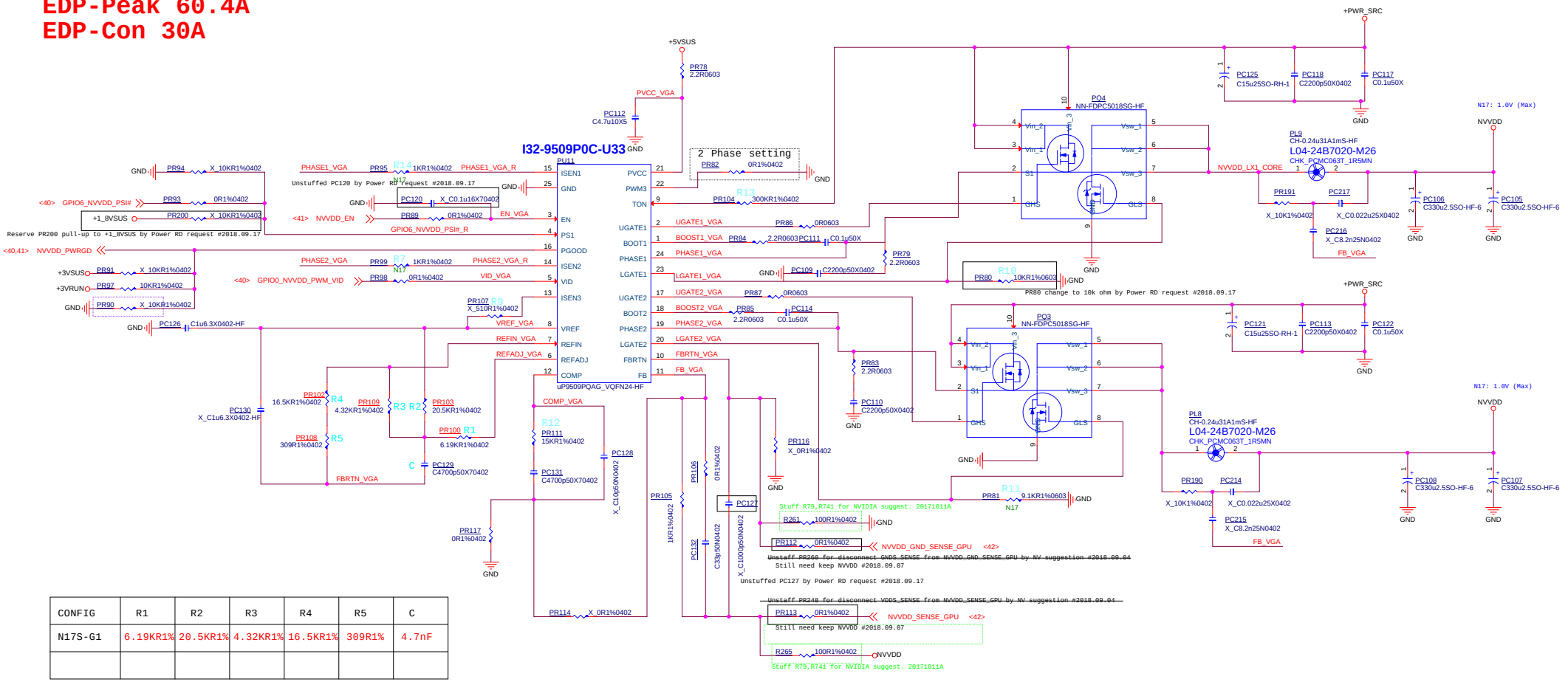
DGPU POWER NVVDD

CONFIG A
VBoot: N17S-0.8V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 60.4A
EDP-Con 30A



CONFIG	R1	R2	R3	R4	R5	C
N17S-G1	6.19KR1%	20.5KR1%	4.32KR1%	16.5KR1%	309R1%	4.7nF

CONFIG	R6	R7	R8	R9	R10	R11	R12	R13	R14
N17S-G1	NC	1KR1%	NC	NC	20KR1%	9.1KR1%	15KR1%	300KR1%	1KR1%

N17

N17R1	N17R2	N17R3	N17R4	N17R5	CA	PWM1	N17R12	N17R13
R1	R2	R3	R4	R5	C	PWM	R12	R13
X_6.19KR1%0402	X_20.5KR1%0402	X_4.32KR1%0402	X_16.5KR1%0402	X_309R1%0402	X_C4700p50X70402	X_uP9509PQAG_VQFN24-HF	X_15KR1%0402	X_300KR1%0402
R11-6191T12-W08	R11-2052T12-W08	R11-4321T12-W08	R11-1652T12-W08	R11-3090T12-R01	C11-4722812-M09	I32-9509P0C-U33	R11-0153T12-W08	R11-0304T12-W08
N17	N17	N17	N17	N17	N17	N17	N17	N17

190.Change R1A name to N17R1 for BOM. 20171127.
191.Change R1B name to N16R1 for BOM. 20171127.
192.Change R2A name to N17R2 for BOM. 20171127.
193.Change R2B name to N16R2 for BOM. 20171127.
194.Change R3A name to N17R3 for BOM. 20171127.
195.Change R3B name to N16R3 for BOM. 20171127.
190.Change R4A name to N17R4 for BOM. 20171127.
191.Change R4B name to N16R4 for BOM. 20171127.
192.Change R5A name to N17R5 for BOM. 20171127.
193.Change R5B name to N16R5 for BOM. 20171127.
194.Change R12A name to N17R12 for BOM. 20171127.
195.Change R12B name to N16R12 for BOM. 20171127.
194.Change R13A name to N17R13 for BOM. 20171127.
195.Change R13B name to N16R13 for BOM. 20171127.

234.Change N16R13 P/N from R11-0913T12-W0B to R11-0683T12-W08 for Power. 20180109

Remover N16 BOM option #2018.09.20

以後注意Option的Location不要跟會跟其他Location撞到的, 因為程式不會分 A/B-

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Title: DGPU POWER NVVDD

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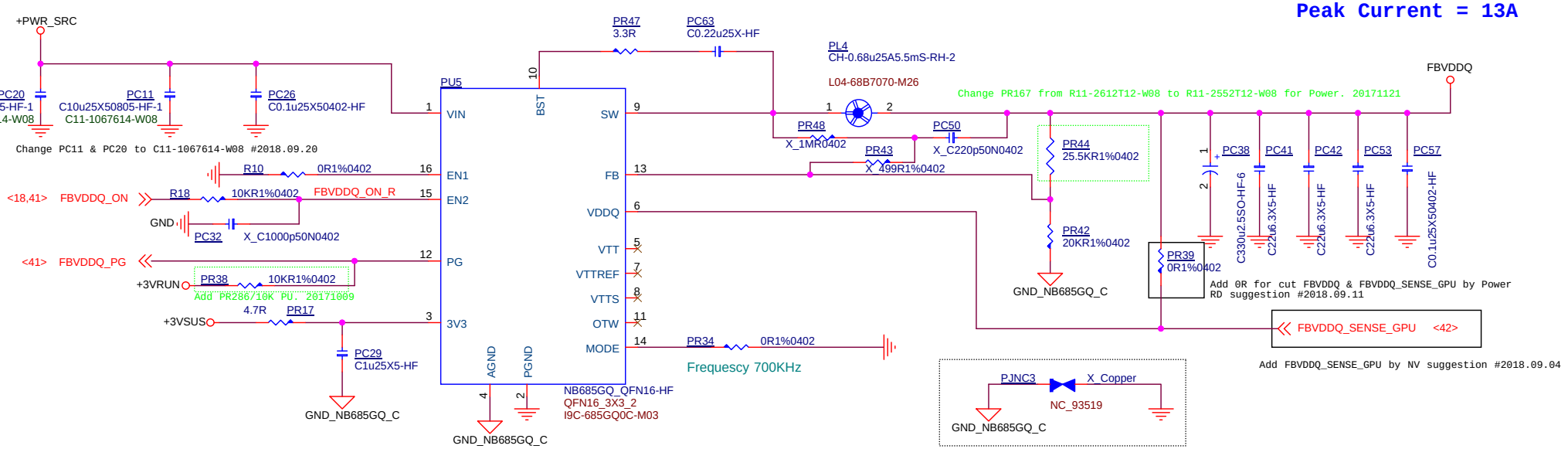
FBVDDQ POWER



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Title: DGPU POWER FBVDDQ			
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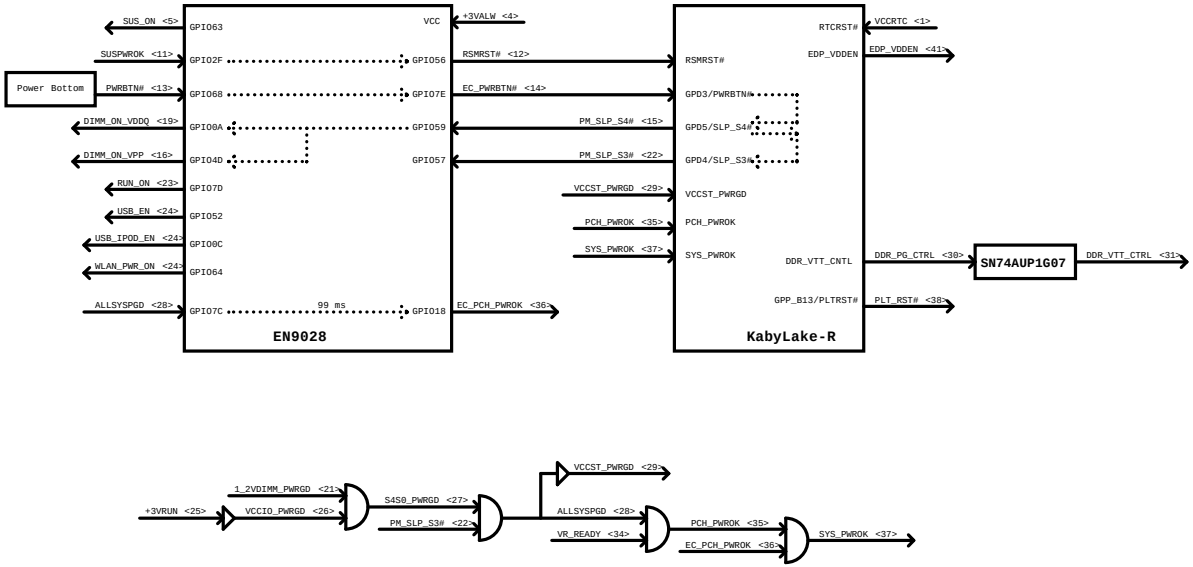
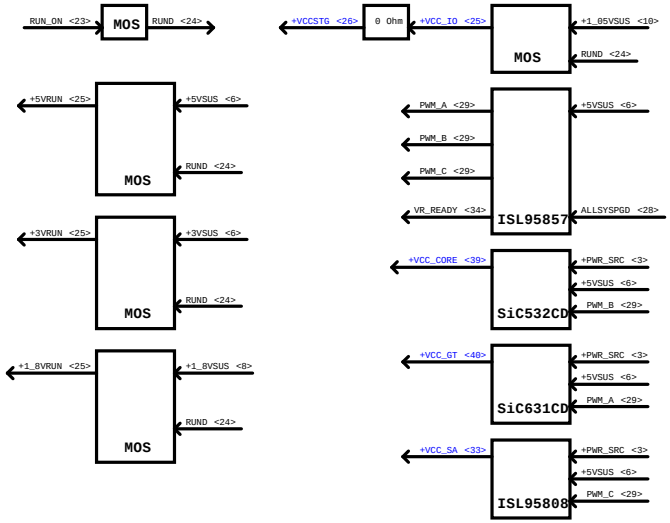
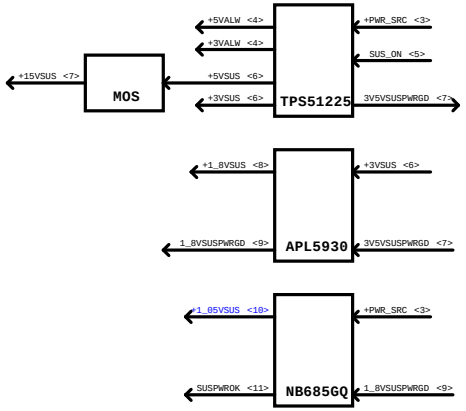


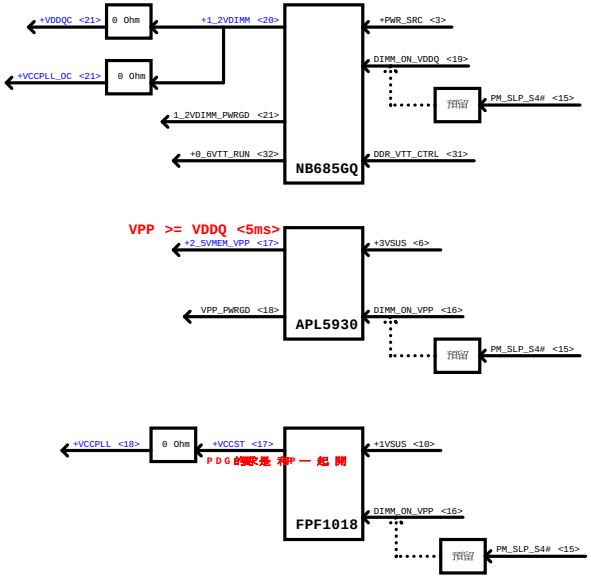
S0

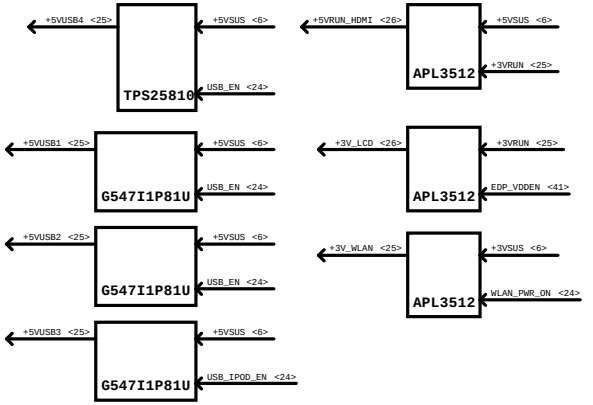


S4/S5



S3





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Title: Power on Block Diagram

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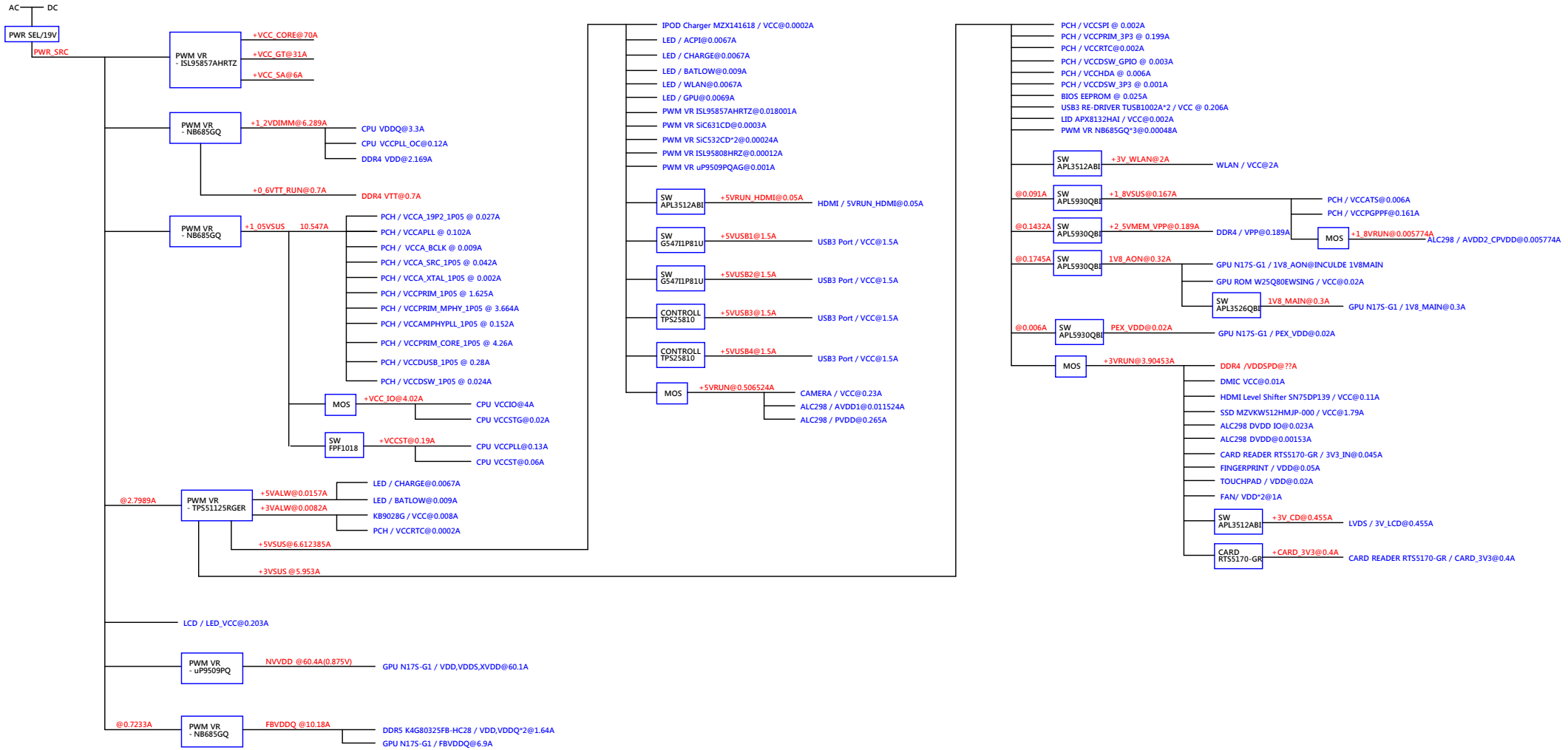
14B3 Power Delivery Chart



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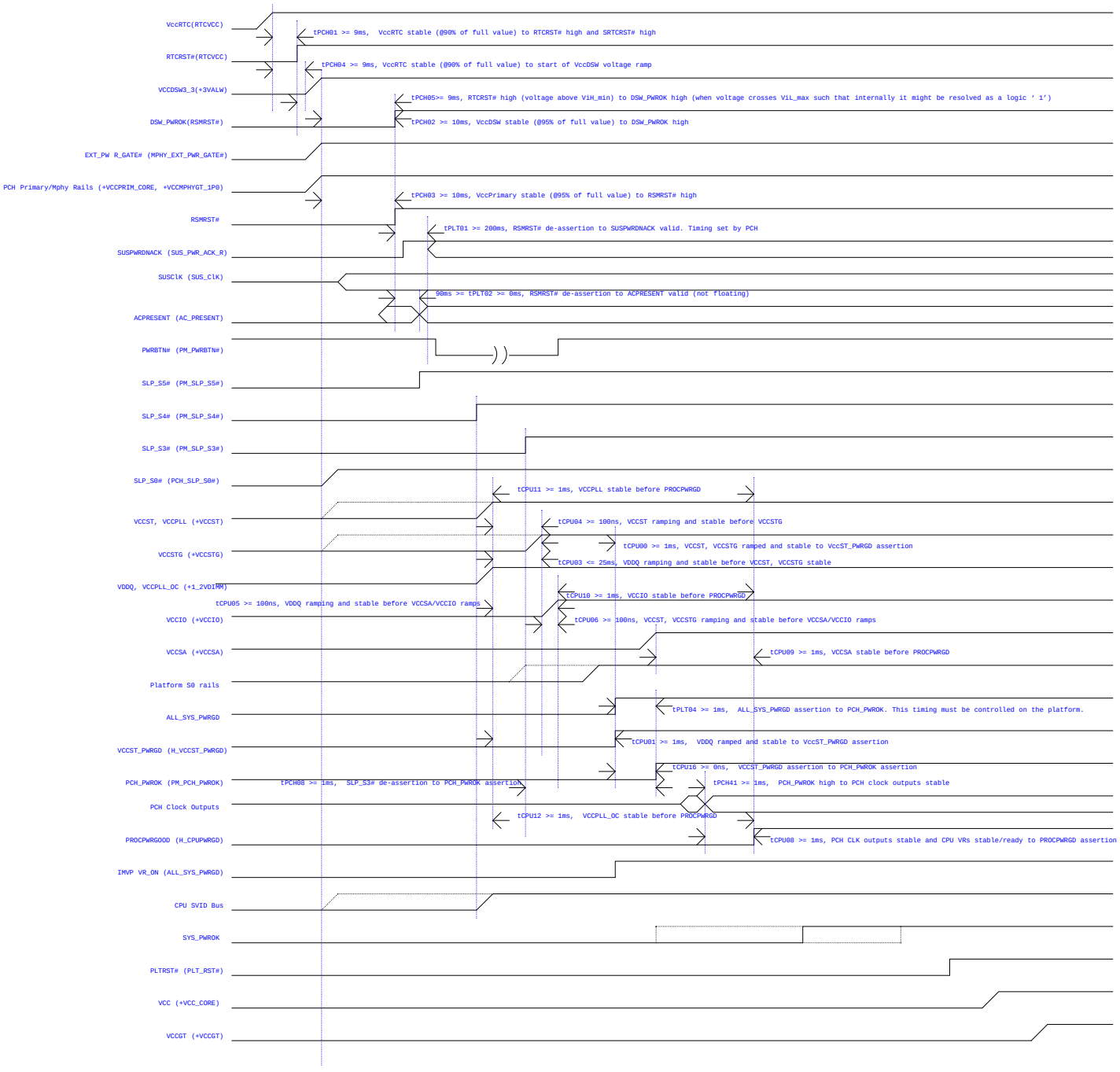
Power Delivery Chart

MS-14B3

0A

G3 to S0



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Title: G3 into S0 without M

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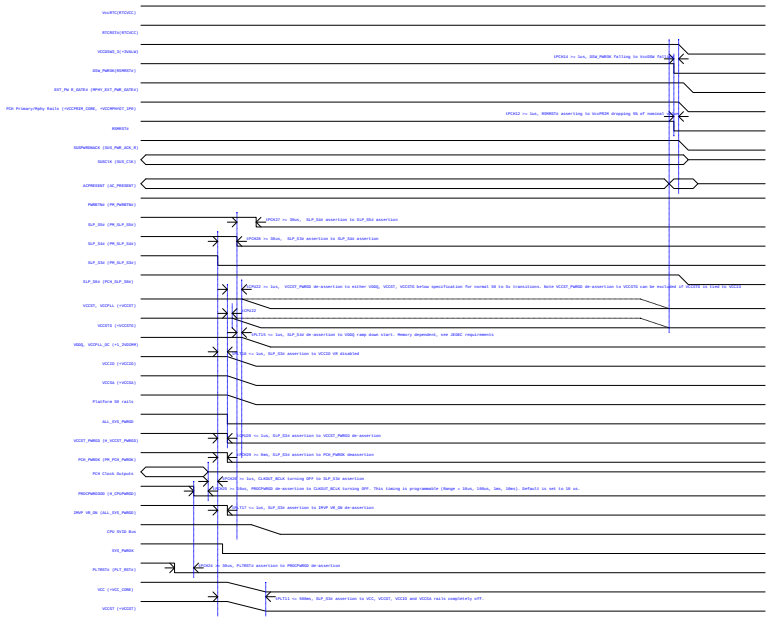
S0 to G3



MICRO-STAR INT'L CO.,LTD.		
Title: S0 into G3 without M		
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14B3 0A Change History

1. Page.31 Change Charge_LED#/BATLOW_LED# pull up to +5VALW #2018.08.09
2. Page.8/12 Remove SLP_S0# function, 14B3 did not support #2018.08.09
3. Page.12 Remove RUN_ON_C10 control, 14B3 did not support #2018.08.09
4. Page.18 Follow 16S1 to change control logic with RUN_ON #2018.08.09
5. Page.18 Change netname from ACPI_LED# to POWER_LED# #2018.08.09
6. Page.29 Follow 16S1 reserve I2C SMbus for TP #2018.08.10
7. Page.8 Follow 14B1 reserve R657 for CFG_UMA sku. #2018.08.10
8. Page.8 Follow 13H1 reserve M8 ID[0:3] #2018.08.10
9. Page.27/28 Follow 13H1 add short protection circuit on USB Type-C RX #2018.08.10
10. Page.45 Add +VCCSTG power combine with +VCC_IO (follow 13H1) #2018.08.10
11. Page.45 Reserve +VCCSTG power combine with +VCCST (follow 16S1) #2018.08.10
12. Page.45 Follow 13H1 reserve control signal RUN_ON for +VCCST #2018.08.10
13. Page.7 Add Pull-up R5318 for PCIE_CLK_WLAN_REQ# #2018.08.13
14. Page.23 Add TPM page #2018.08.13
15. Page.18 Change DGPU_PWRGD to GPIO5D #2018.08.13
16. Page.18 EC recommend remove EX-XTAL #2018.08.13
17. Page.25 Change USB3.1 re-driver from 1002 to 1002A(Follow13H1) #2018.08.14
18. Page.18 Add USB_1002_EN on GPIO5E #2018.08.14
19. Page.17 DP139 VCC side add bulk cap by vendor suggest #2018.08.15
20. Page.3 Remove Pull-Down R51S3, page.17 have reserve same pull-down #2018.08.15
21. Page.18 Add Pull-up R102 for KBRST# (follow 13H1) #2018.08.15
22. Page.23 Add Pull-up Resistor for USB_1002_EN by EC suggistion #2018.08.15
23. Page.7 Follow PDG(P.294) reserve capacitor to GND for EMI issue #2018.08.15
24. Page.9 Follow 14B1 change HDA R/C value for SA #2018.08.15
25. Page.18 Remove PCH_PWROK pull-down resistor, page.8 have pull-dowm 10Kohm #2018.08.15
26. Page.19 Add 0R0402 for SATA M.2 #2018.08.15
27. Page.20 Add AC coupling capacitor for PCIE GEN2 #2018.08.15
28. Page.44~52 Combine power change for improve power loadline #2018.08.16
29. Page.23 Add resistor 0ohm and place on T-routing via side #2018.08.20
30. Page.23 Reserve capacitance and place on TPM side for SA issue #2018.08.20
31. Page.6 Follow 14B1 to change location for placement #2018.08.22
32. Page.7 Follow PDG change BIAS R from 10M 5% to 10M 1% #2018.08.23
33. Page.12 Add Reserve Cap, refer to PDG 575412 Table 11-2 #2018.08.23
34. Page.8/9/11/20 Add CNVi function by PM request #2018.08.24
~~35. Page.7 Reserve RTC_RST# discharge circuit #2018.08.24~~
35. Combine layout team re-name location on CPU side #2018.08.28
36. Page.20 Change R5344 from 0805 to 1206 for CNVi GEN2 (2A) #2018.08.28
37. Page.08 Follow MOW Table 5-1 change R7042 & R7034 from 75 to 33ohm #2018.08.29
38. Page.20 Follow PDG add 10uF+0.1uF+0.01uF #2018.08.30
39. Page.33 Not Staff R5040 & staff R5039 by NV comment #2018.08.30
40. Page.33 Change to VDD_AON by NV comment #2018.08.30
41. Page.42 Add 22u for VRAM by NV comment #2018.08.30
42. Remove N16 co-design portion #2018.08.30
43. Page.20 Change R5344 connnect to +3V_WLAN #2018.09.03
44. Page.18 Follow 13H1 & 16S1 add buffer IC on VR_READY #2018.09.03
~~45. Page.51 Unstaff PR260 for disconnect GNDS_SENSE from NVVDD_GND_SENSE_GPU by NV suggestion #2018.09.04~~
~~46. Page.51 Unstaff PR248 for disconnect VDDS_SENSE from NVVDD_SENSE_GPU by NV suggestion #2018.09.04~~
47. Page.42/52 Add FBVDDQ_SENSE_GPU by NV suggestion #2018.09.04
48. Page.10 Change USB3.1 port1/2/3/4 order for layout #2018.09.04
49. Page.46 Follow 13H1 Add S3 # for shutdown timing TPLT18 #2018.09.05
50. Page.46 Reserve Cap for PM_S3_CNTRL time delay after RUND #2018.09.05
51. Page.27 Delete ESD18 and change USB3_RXN_TYPEC1_U_C/USB3_RXP_TYPEC1_U_C link ESD16 for Layout. #2018.09.05
52. Page.28 Delete ESD30 and change USB3_RXN_TYPEC3_C/USB3_RXP_TYPEC3_C link ESD28 for Layout. #2018.09.05
53. Page.28 Delete ESD31 and change USB3_RXN_TYPEC4_C/USB3_RXP_TYPEC4_C link ESD28 for Layout. #2018.09.05
54. Page.28 Swap USB3_RXP_TYPEC3_C/USB3_RXN_TYPEC3_C by layout request #2018.09.05
55. Page.28 Swap USB3_RXP_TYPEC4_C/USB3_RXN_TYPEC4_C by layout request #2018.09.05
56. Page.32 Delete UME1 for thermal solution change #2018.09.06
57. Page.42 Disconnect VDDS_SENSE/GNDS_SENSE link to VDD_SENSE/GND_SENSE by NV suggestion #2018.09.07
58. Page.14 Follow PDG Table11-4, add decoupling 1uF 0201 for PCH power rail #2018.09.07
59. Page.52 Add 0R for cut FBVDDQ & FBVDDQ_SENSE_GPU by Power RD suggestion #2018.09.11
60. Page.38 Set NV_Strap 0xA as default for Hynix H5GC8H24AJR-R2C #2018.09.12
61. Layout Re-name by layout request #2018.09.13
62. Change R0402 PCB footprint to MXM type : EC14,R454,R201,R197,R192,R311,R463,PR30,R438,R305,R437
63. Page.7 Follow 16S1 0B add discharge circuit on SRTC_RST & RTC_RST #2018.09.13
64. Page.21 Add JNCS by vender suggestion #2018.09.13
65. Page.49 Change PR57 form 3.65k to 1.82k and add PR198 by power RD request #2018.09.14
66. Page.49 Change PR19 form 3.65k to 1.82k and add PR199 by power RD request #2018.09.14
67. Page.48 Change PU6 form I32-958572C-I11 to I32-958573C-I11 by power RD request #2018.09.14
68. Page.48 Change PR59 form R11-2151T12-W08 to R11-0222T12-W08 by power RD request #2018.09.14
69. Page.48 Change PR187 form R11-0104T22-W08 to R11-0913T12-W08 by power RD request #2018.09.14
69. Page.48 Change PR58 form R11-0302T12-W08 to R11-0222T12-W08 by power RD request #2018.09.14
70. Page.48 Change PR179 form R11-2551T12-W08 to R11-0392T12-W08 by power RD request #2018.09.14
71. Page.48 Change PR41 form R11-2941T12-W08 to R11-2551T12-W08 by power RD request #2018.09.14
72. Page.48 Change PR36 form R11-0302T12-W08 to R11-2551T12-W08 by power RD request #2018.09.14
73. Page.48 Change PR52 form R11-0561T12-W08 to R11-4870T22-W08 by power RD request #2018.09.14
74. Page.48 Change PR173 form R11-9532T12-W08 to R11-9092T12-W08 by power RD request #2018.09.14
75. Page.48 Change PR172 form R11-0104T22-W08 to R11-0114T12-W08 by power RD request #2018.09.14
76. Page.48 Change PR53 form R11-9762T12-W08 to R11-4322T12-W08 by power RD request #2018.09.14
77. Page.48 Change PC70 form C11-224741-M09 to C11-1032012-M09 by power RD request #2018.09.14
78. Page.48 Change PC76 form C11-1522832-M09 to C11-8212012-W08 by power RD request #2018.09.14
79. Page.48 Change PC61 form C11-1547412-M09 to C11-1042012-M09 by power RD request #2018.09.14
80. Page.48 Change PC73 form C11-4732612-M09 to C11-3337512-W08 by power RD request #2018.09.14
81. Page.48 Change PC37 form C11-1021812-M09 to C11-8212012-W08 by power RD request #2018.09.14
82. Page.50 Unstuff PR68 by power RD suggestion #2018.09.14
83. Page.25 Change USB3.1 Redriver to initial EQ/VOD setting by vender suggestion #2018.09.14
84. Page.32 Reserve +5VSUS 0402 0.1u cap *3 to GND by EMI request #2018.09.17
85. Page.32 Reserve +3VRUN 0402 0.1u cap *1 to GND by EMI request #2018.09.17
86. Page.51 PR80 change to 10k ohm by Power RD request #2018.09.17
87. Page.51 Unstuffed PC127 by Power RD request #2018.09.17
88. Page.51 Unstuffed PC129 by Power RD request #2018.09.17
89. Page.51 Reserve PR200 pull-up to +1_8VSUS by Power RD request #2018.09.17
90. Page.46 Change PC169, PC179, PC184 from 120uF to 150uF(C71-151061G-S03) by power RD request #2018.09.17
91. Page.32 Change CPU & GPU stand off to 16S1 type by ME request #2018.09.18
92. Page.51 Remover N16 BOM option #2018.09.20
93. Page.46/49 Change C238, PC211 & PC212 to C11-2232032-W08 #2018.09.20
94. Change PC11, PC12, PC20, PC150, PC178, PC190, PC191, PC192 to C11-1067614-W08 #2018.09.20
95. Page.38 Change Y2 to D04-1107400-F07 because main source was phase out #2018.09.20
96. Page.24 U9 change USB_EN to USB_IPOD_EN for IPOD charger by EC request #2018.09.21
97. Page.20 Staff R320 for PCIe module #2018.09.27
98. Page.20 Stuff U36 and unstuff R313 for PCIe module #2018.09.27
100. Page29. Stuff R503 & R505, unstuffed R502 & R504 to change TP protocol from I2C to SMBUS by vendor request #2018.10.01

14B3 0B Change History

0B.1. Page.25 Change R443 & R212 from 20k ohm to 1k ohm by vender suggestion #2018.11.02
0B.2. Page.45 Add 1_2VDIMM_PWRGD & R513 to control VCCST enable for satisfy tCPU03 & tCPU05. #2018.11.02
0B.3. Page.48 PR52 Change to 549 ohm, R11-5490T12-W08 by power RD request #2018.11.02
0B.4. Page.48 PR53 change to 37.4kohm, R11-3742T12-W08 by power RD request #2018.11.02
0B.5. Page.07 Remove BIOS ROM socket & place BIOS ROM M31-2512893-W03 #2018.11.09
0B.6. Page.47 Change PR96 form 0 ohm to 1k ohm (R11-0102T12-W08) for ALC298 power on sequence #2018.11.09
0B.7. Page.47 Stuffed & change PC123 to 0.01uf (C11-1032082-M09) for ALC298 power on sequence #2018.11.09
0B.8. Page.33 Change C48 & C49 from 5010 to 5020 #2018.11.09
0B.9. Page.09 Change R195 form 22R to 10R (R11-0100T12-W08) and unstuff EC14 for SA #2018.11.09
0B.10.Page.25 Stuffed R146 & change R443 to 20kR for SA #2018.11.09
0B.11.Page.25 Stuffed R220 & change R212 to 20kR for SA #2018.11.09
0B.12.Page.07 Change C580 & C584 from 4.7pF to 3.9pF(C11-39A1822-W08) by Vender matching report #2018.11.12
0B.13.Page.32 Add Gasket MYL22 (E2Y-X027311-CA7) by EMI request #2018.11.13
0B.14.Page.33 Change GPU P/N to PS sample (0B3-14B3003-N0B) by PM request #2018.11.13
0B.15.Page.24 Add Ipod charger BOM control table for ODM & OBM #2018.11.13
0B.16.Page.23 Add TPM BOM control table for ODM & OBM #2018.11.13
0B.17.Page.32 Unstuffed Mylar for EVT by PM request #2018.11.13
0B.18.Page.32 Change PCB P/N to PD0-14B310B-H73 #2018.11.13

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