

Compal Confidential

Model Name : QILE1 & QILE2
File Name : LA-8131P, LA-8133P
BOM P/N:

QILE1:
4319GG39L01 : SMT MB A8131 QILE1 DIS-N13P
4319GG39L02 : SMT MB A8131 QILE1 DIS GPU-N13M
4319GG39L03 : SMT MB A8131 QILE1 UMA

QILE2:
4319GJ39L01 : SMT MB A8133 QILE2 DIS-N13P
4319GJ39L02 : SMT MB A8133 QILE2 DIS GPU-N13M
4319GJ39L03 : SMT MB A8133 QILE2 UMA

Lenovo Edge E430-E530

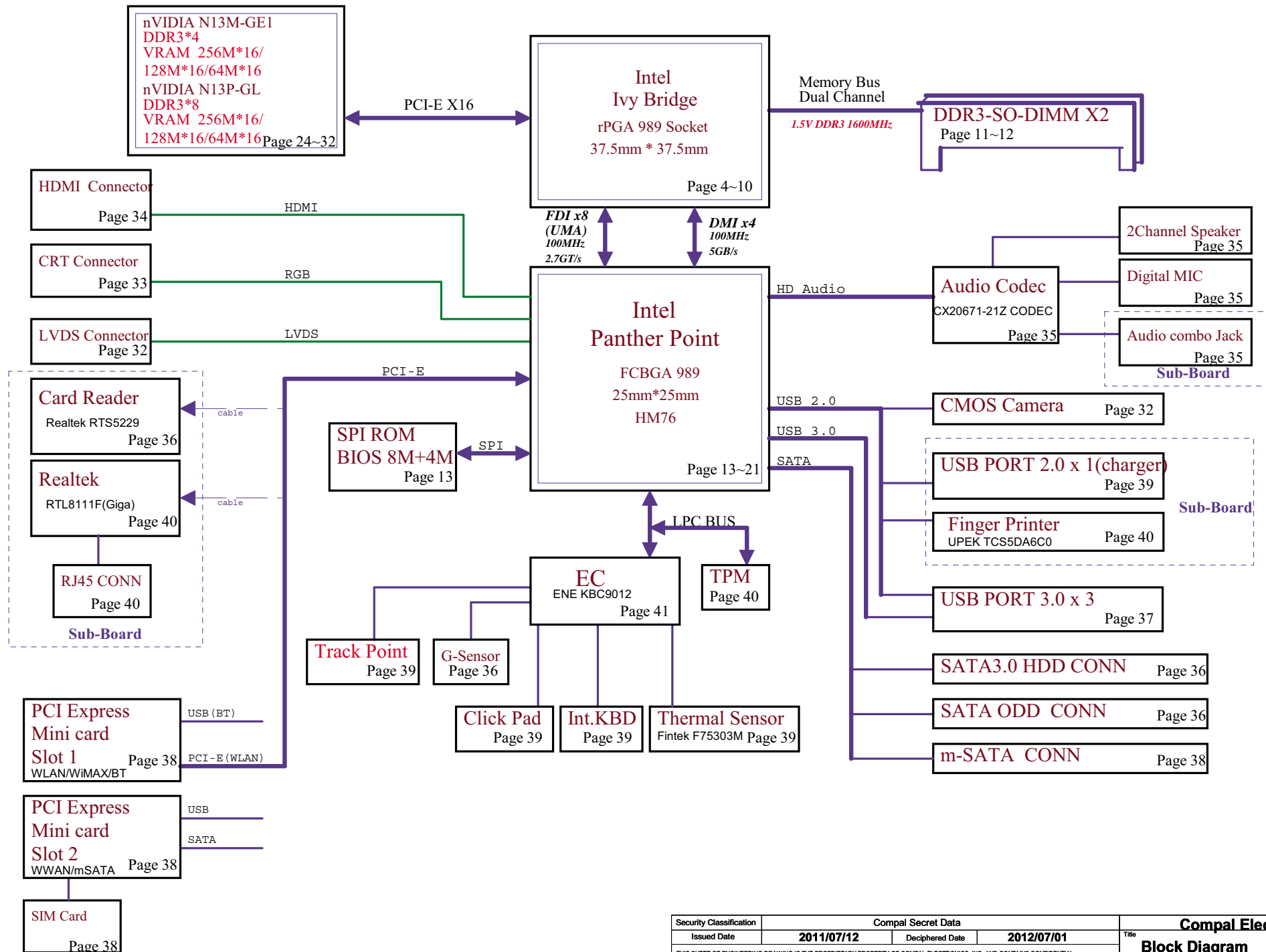
M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH
GPU nVIDIA N13M-GE1 / N13P-GL

2012-01-11

REV:1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title Cover Sheet	
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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0	○	○	○	○	○ M3 Supported
S3	○	○	○	✗	○ M3 Supported
S5 S4/AC	○	○	✗	✗	○ M3 Supported
S5 S4/ Battery only	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist	✗	✗	✗	✗	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB 3.0 Port (Left Side)
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
EHCI2		7	
	UHCI4	8	
		9	USB Port (Right Side)
	UHCI5	10	Mini Card(WLAN/BT)
		11	FPR
	UHCI6	12	Mini Card(WWAN)
		13	Blue Tooth

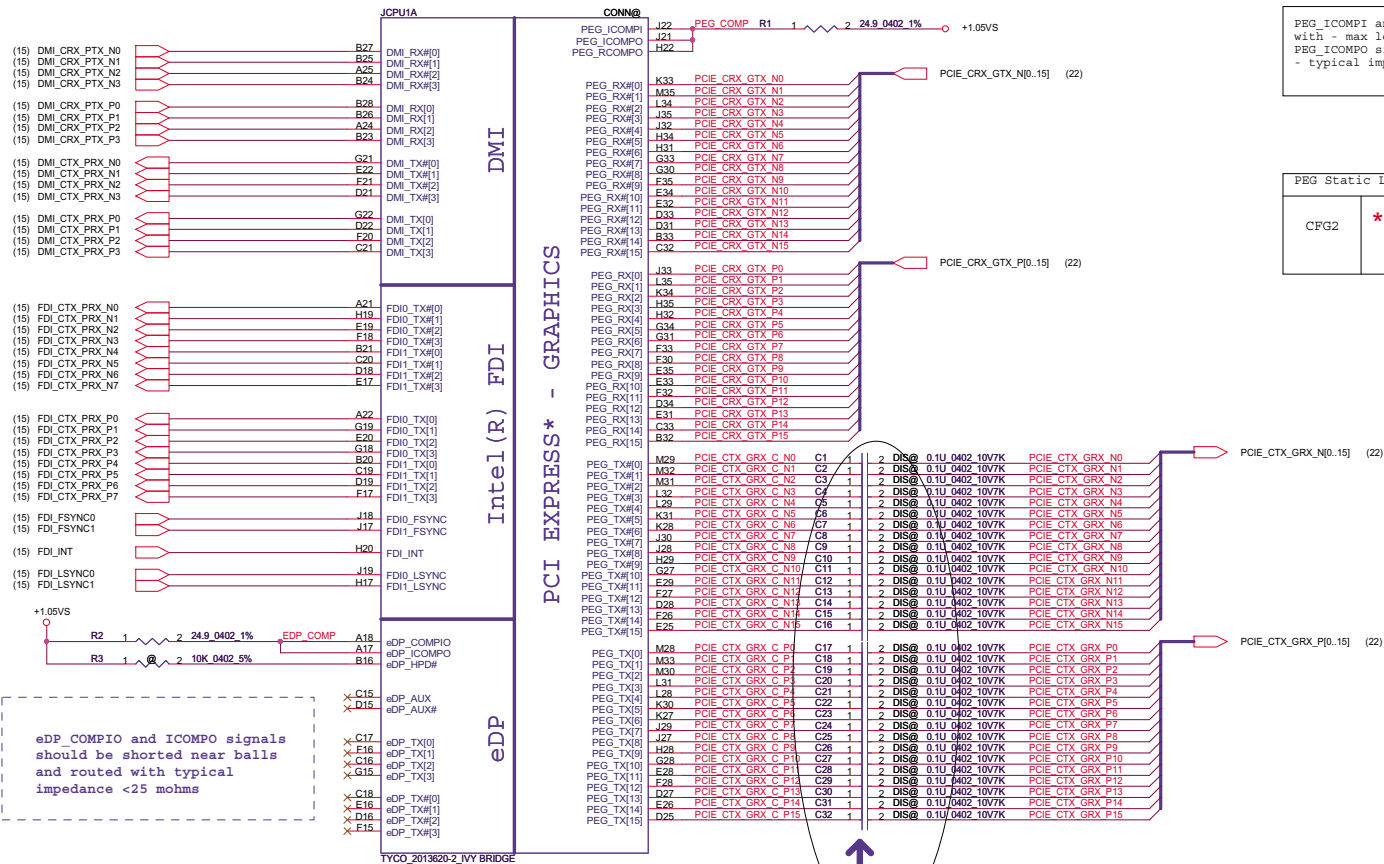
BOM Structure Table

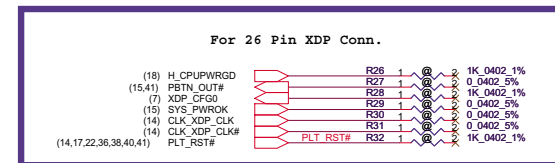
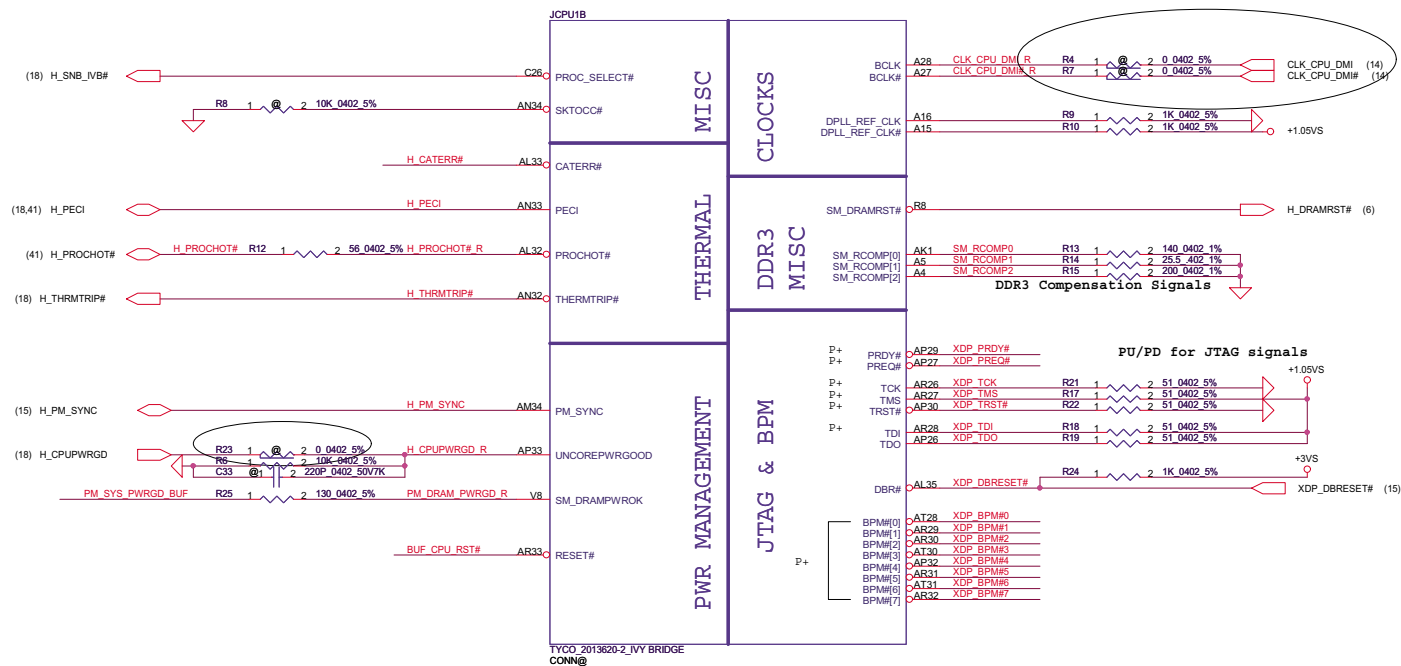
BTO Item	BOM Structure
Connector	CONN@
45 LEVEL	45@
Unpop	@
nVidia	DIS@
INTEL DD3 M3	M3@
SIM Card Slot	3G@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N13M	N13M@
GPU N13P	N13MP

SMBUS Control Table

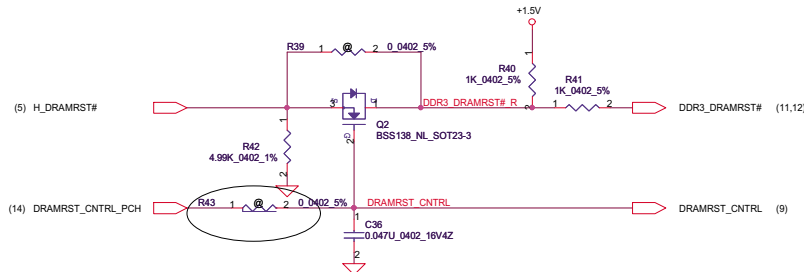
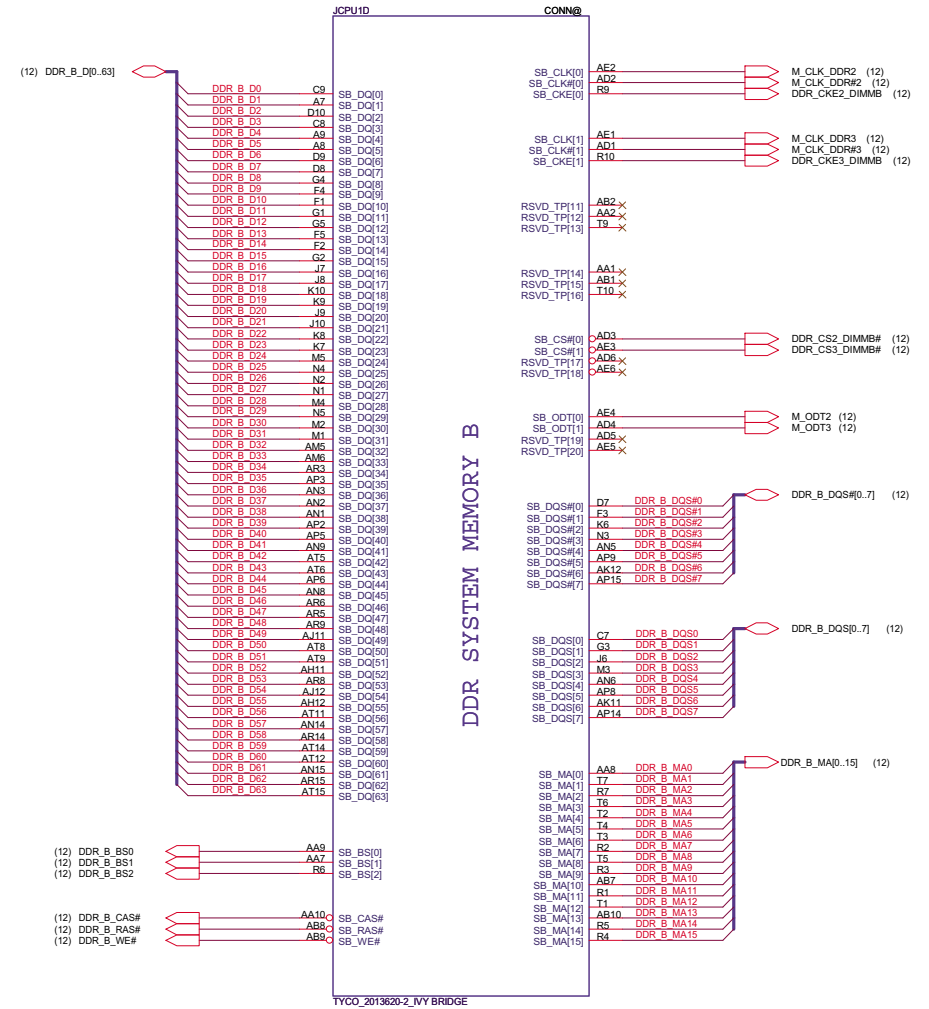
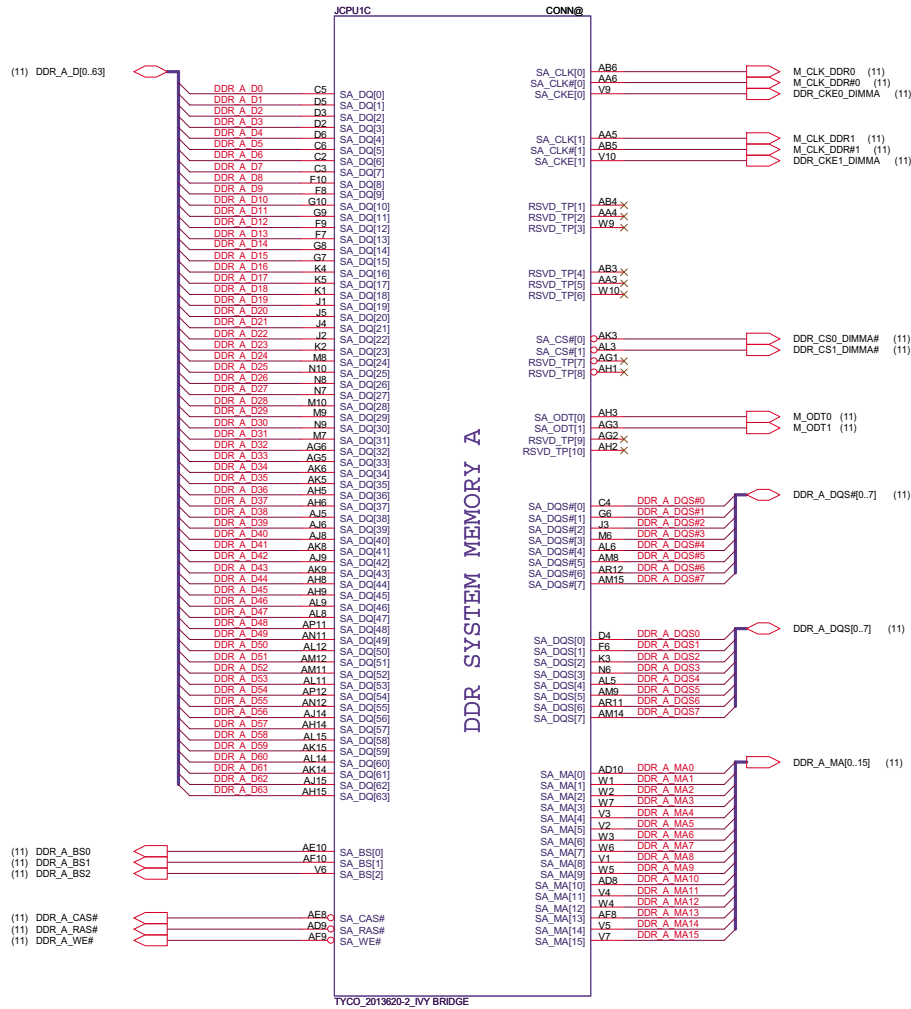
	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	✗	✗	✗	✗	✗	✗	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SMLOCLK	PCH	✗	✗	✗	✗	✗	✗	✗
SMLODATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

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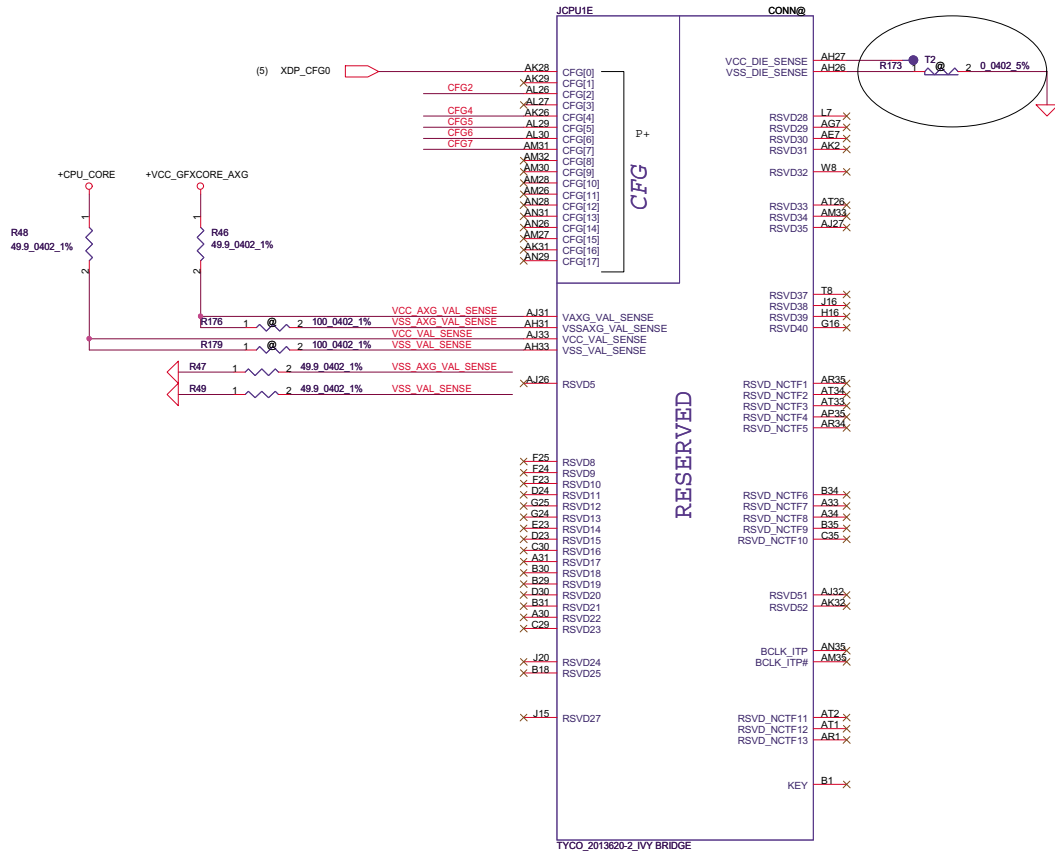




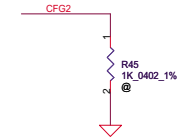
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Title		Compal Electronics, Inc.	
Size		PROCESSOR(3/7) DDRIII	
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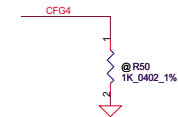


CFG Straps for Processor



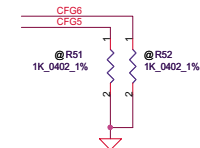
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>
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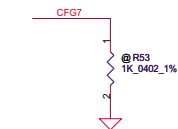
Display Port Presence Strap

CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
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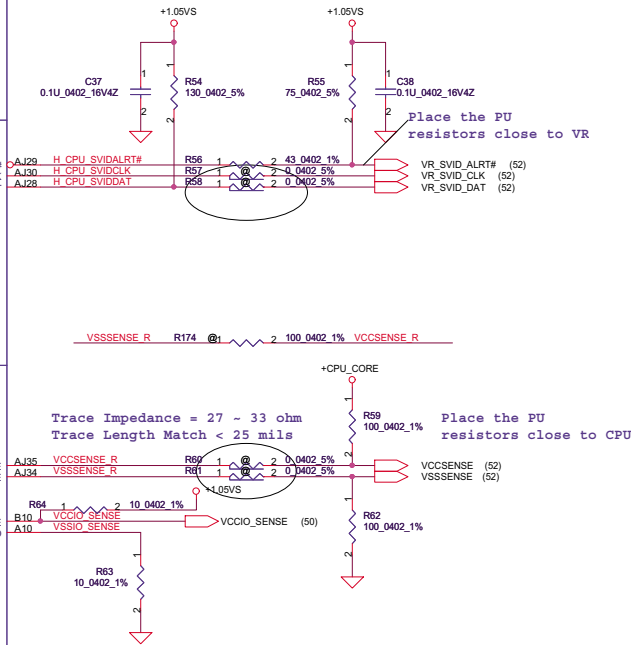
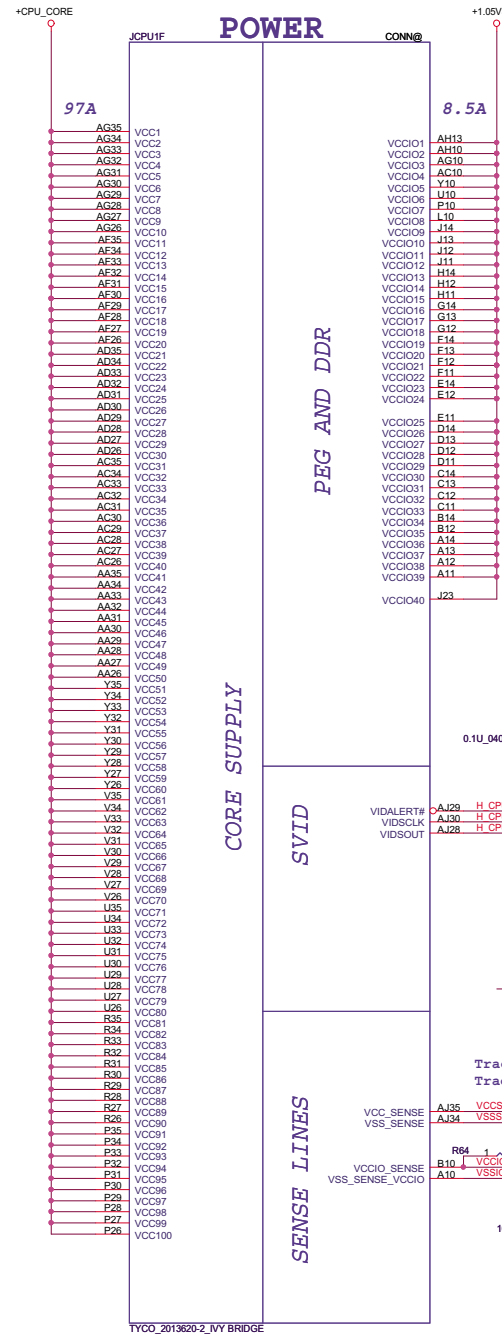
PCIe Port Bifurcation Straps

CFG[6:5]	<p>★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>
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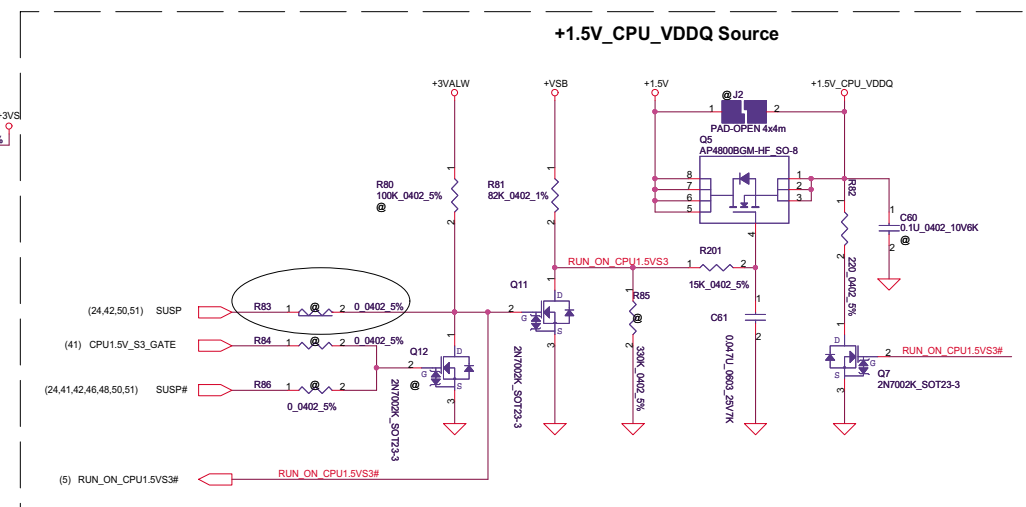
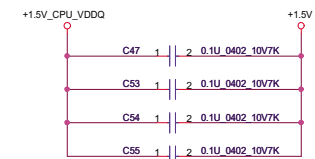
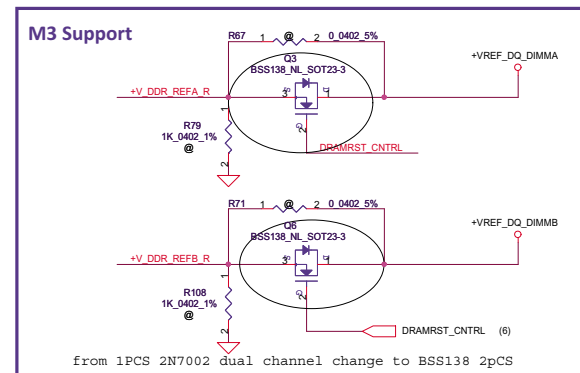


PEG DEFER TRAINING

CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
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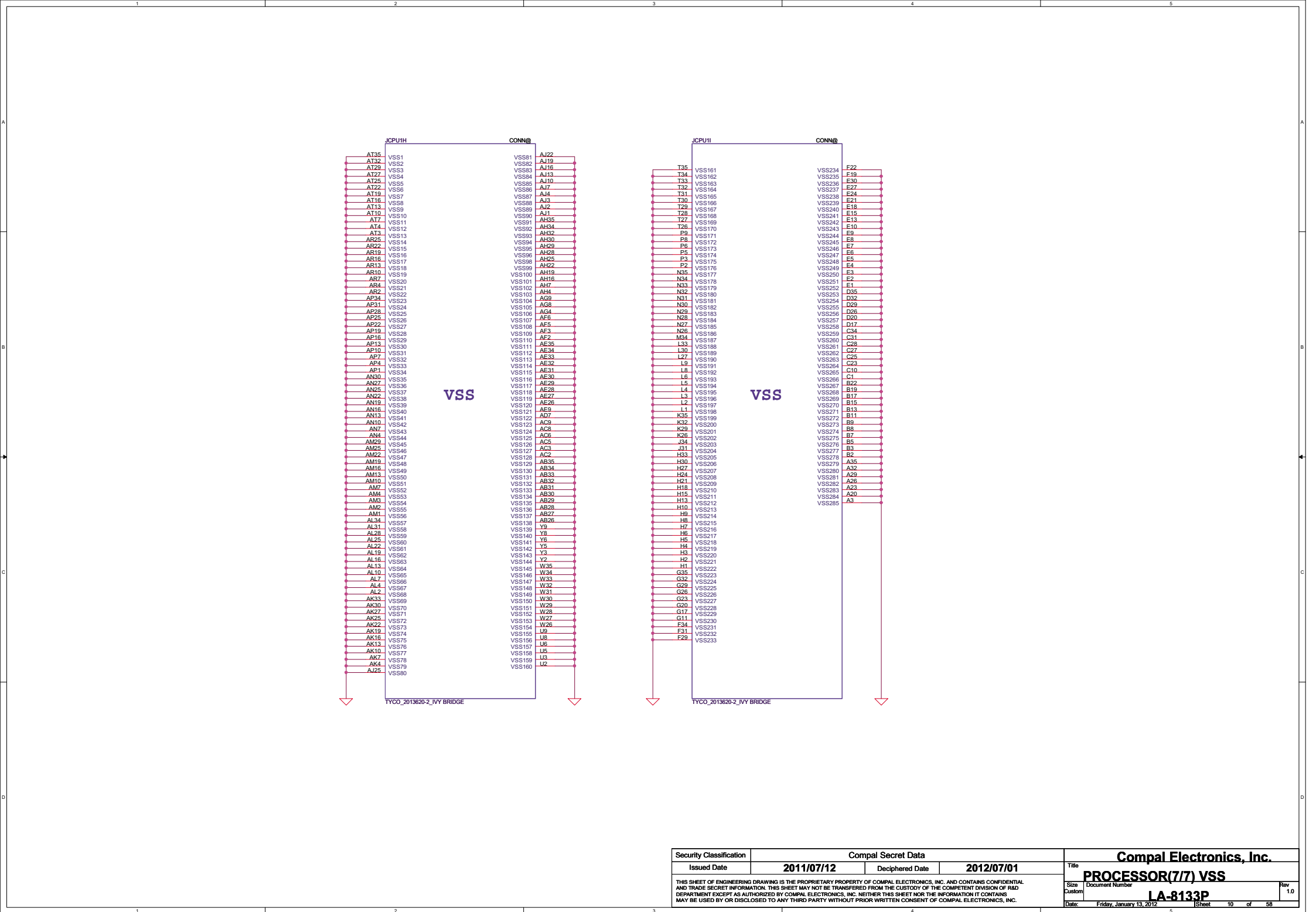


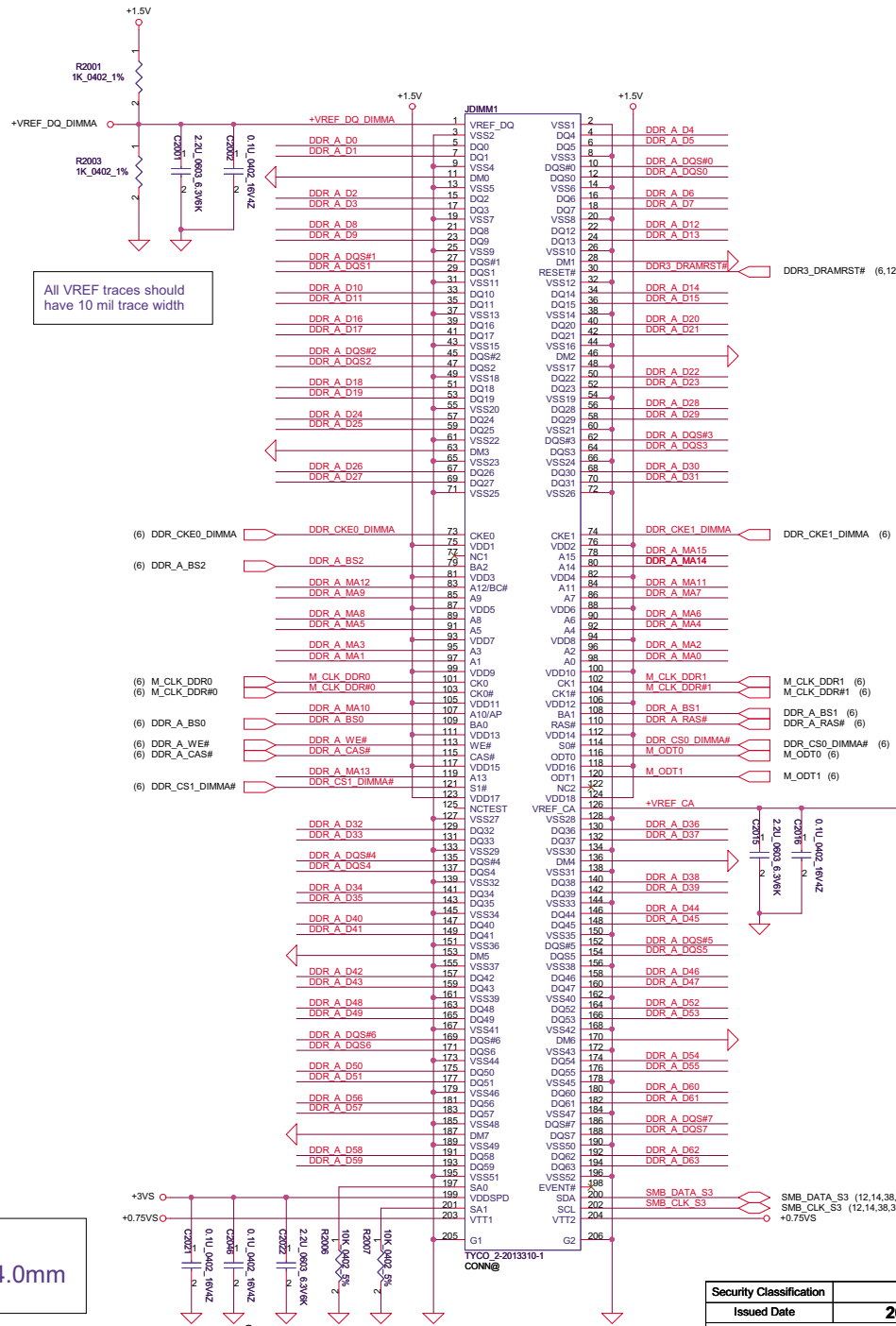
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- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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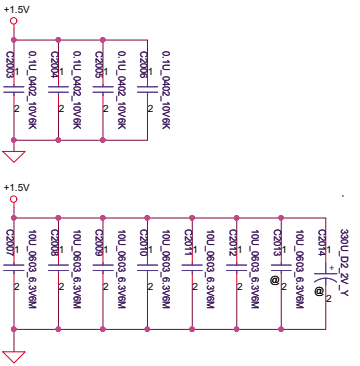


All VREF traces should have 10 mil trace width

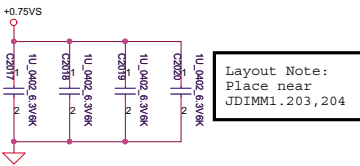
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- DDR_A_DQS#0[0..7] (6)
- DDR_A_DQS#0[0..7] (6)
- DDR_A_D[0..63] (6)
- DDR_A_MA[0..15] (6)

Layout Note:
Place near
JDDIMM1

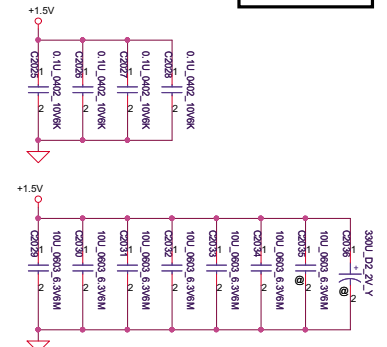


Layout Note:
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JDDIMM1.203,204

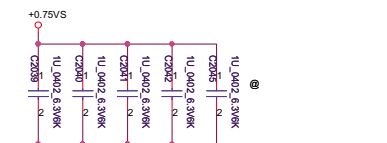




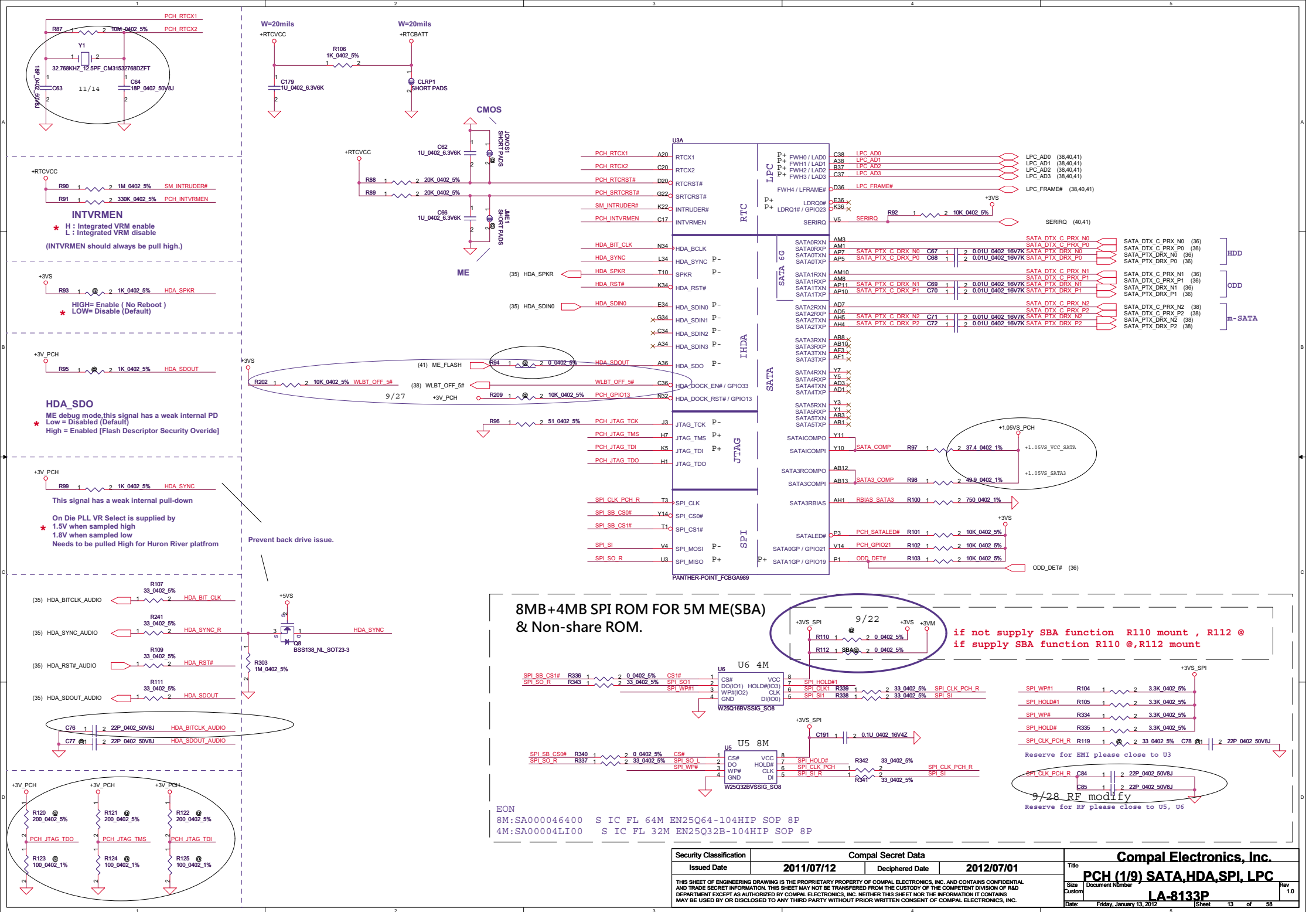
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JDIMM2

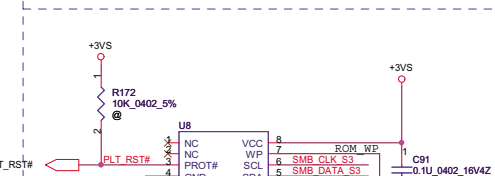
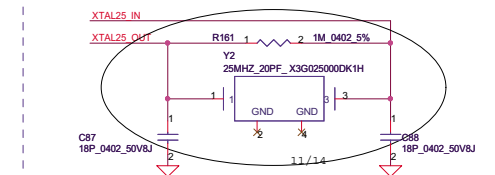
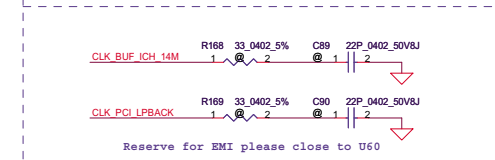
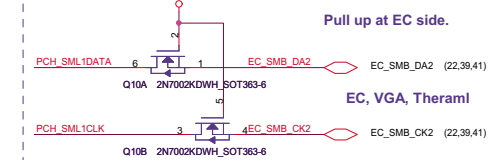
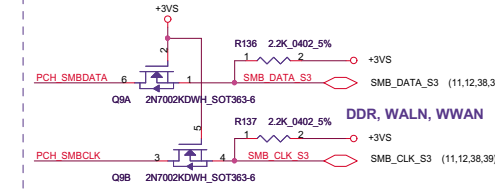
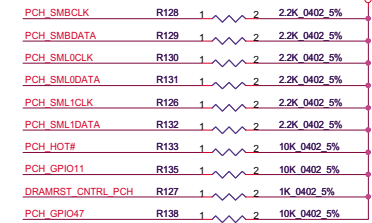
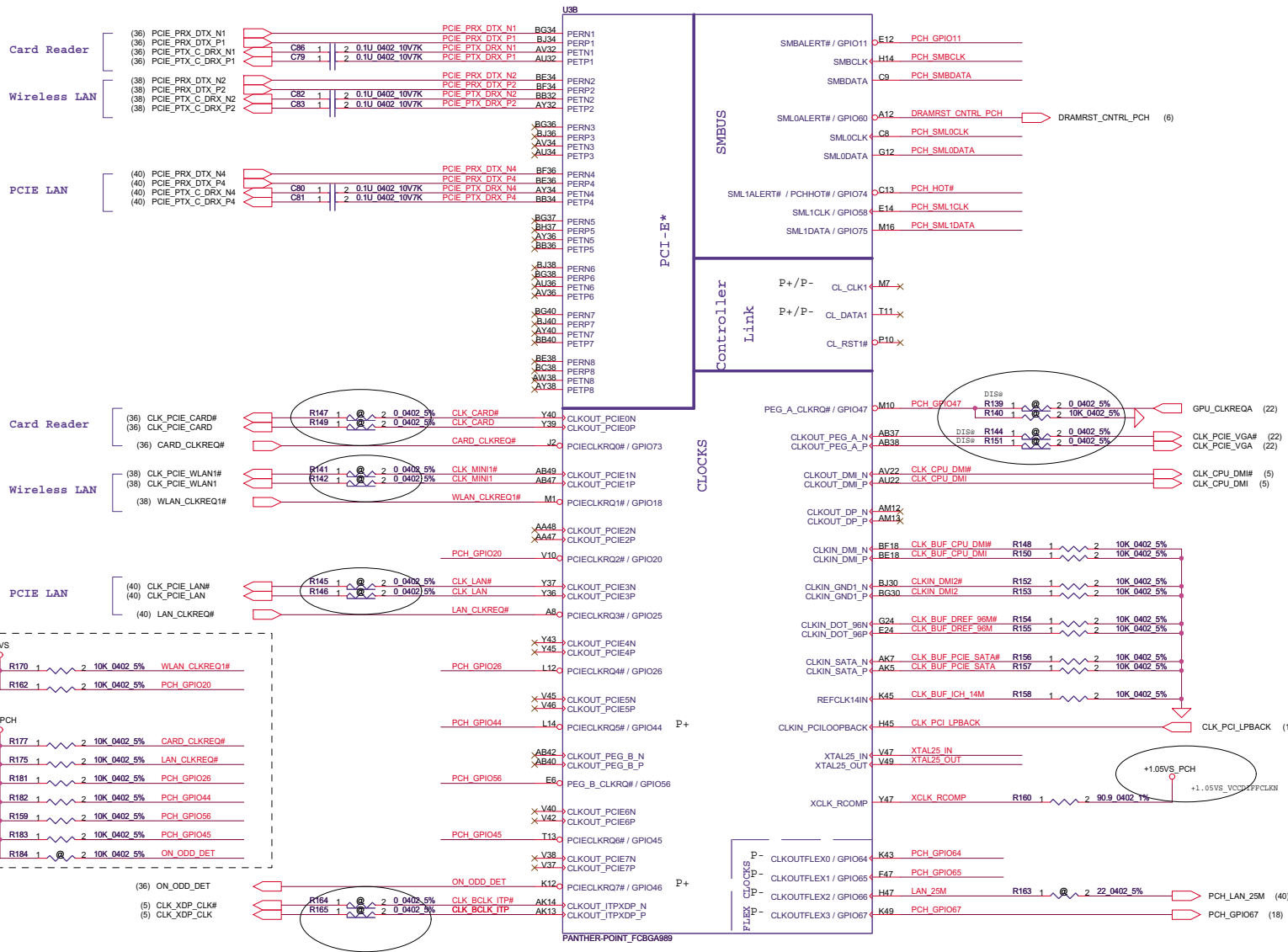


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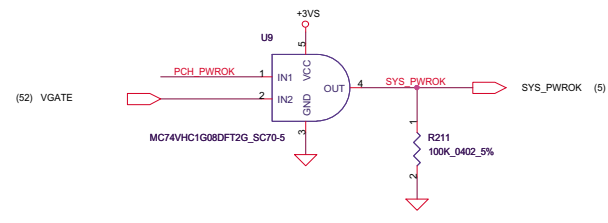
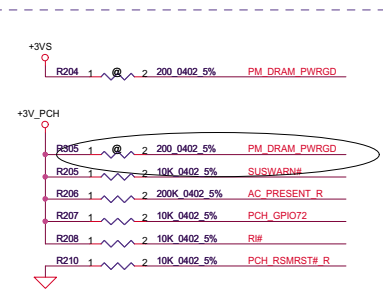
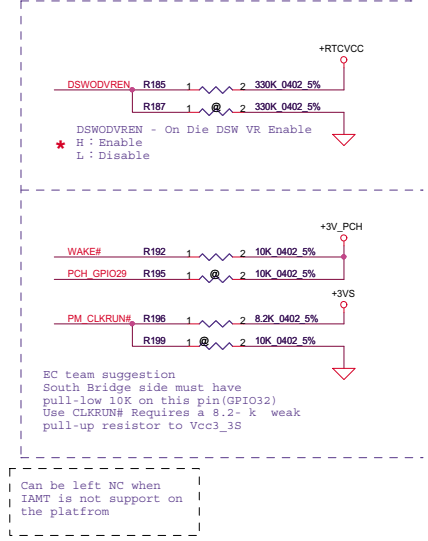
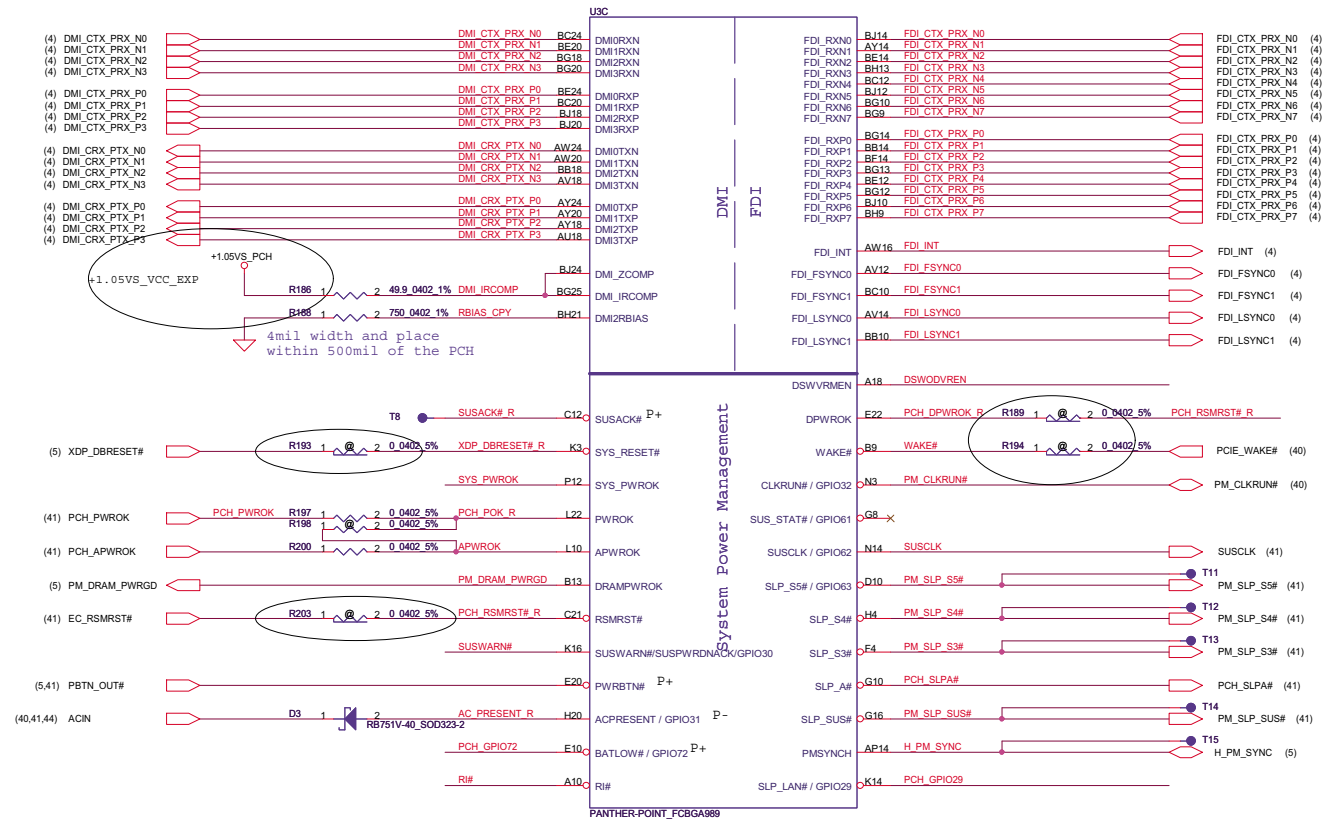


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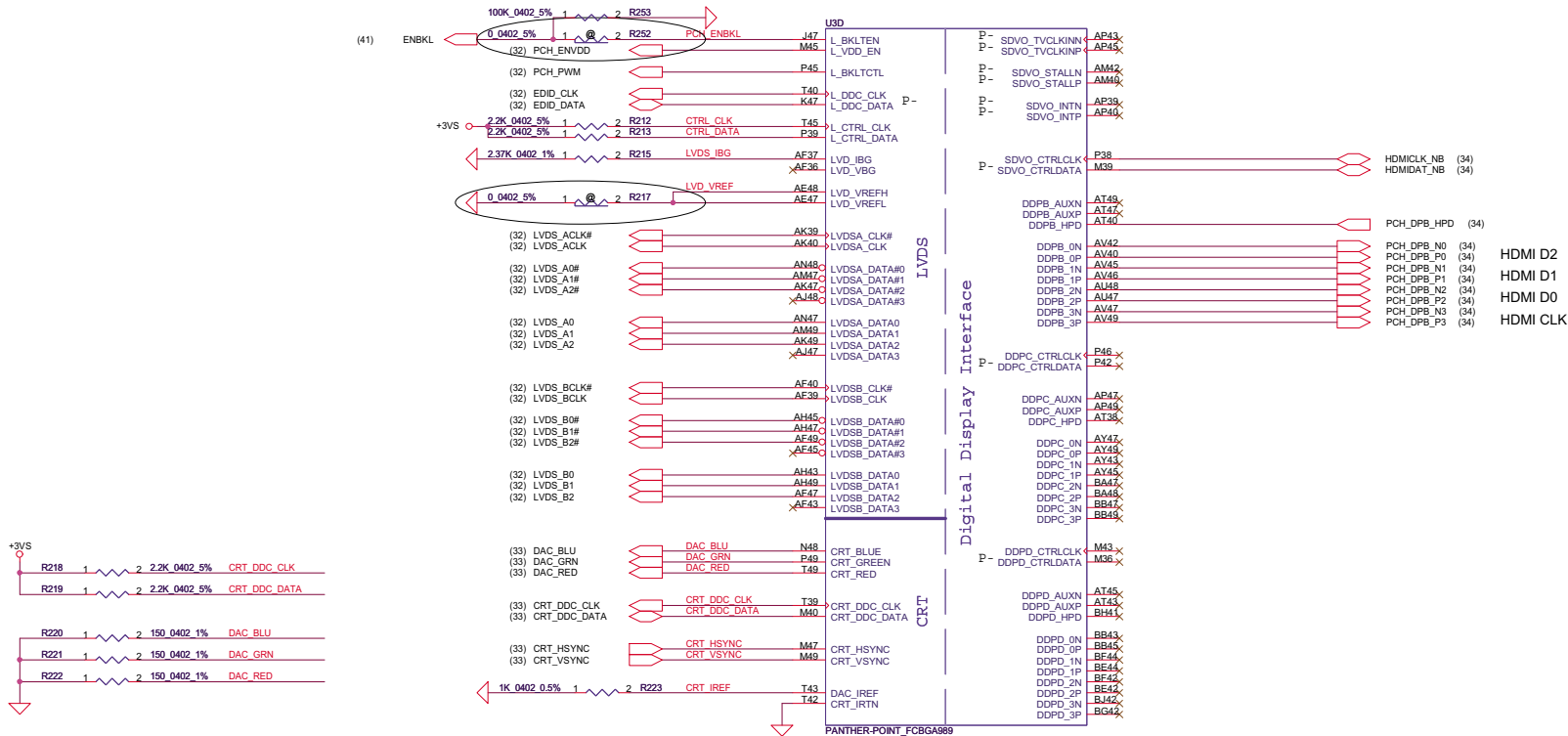




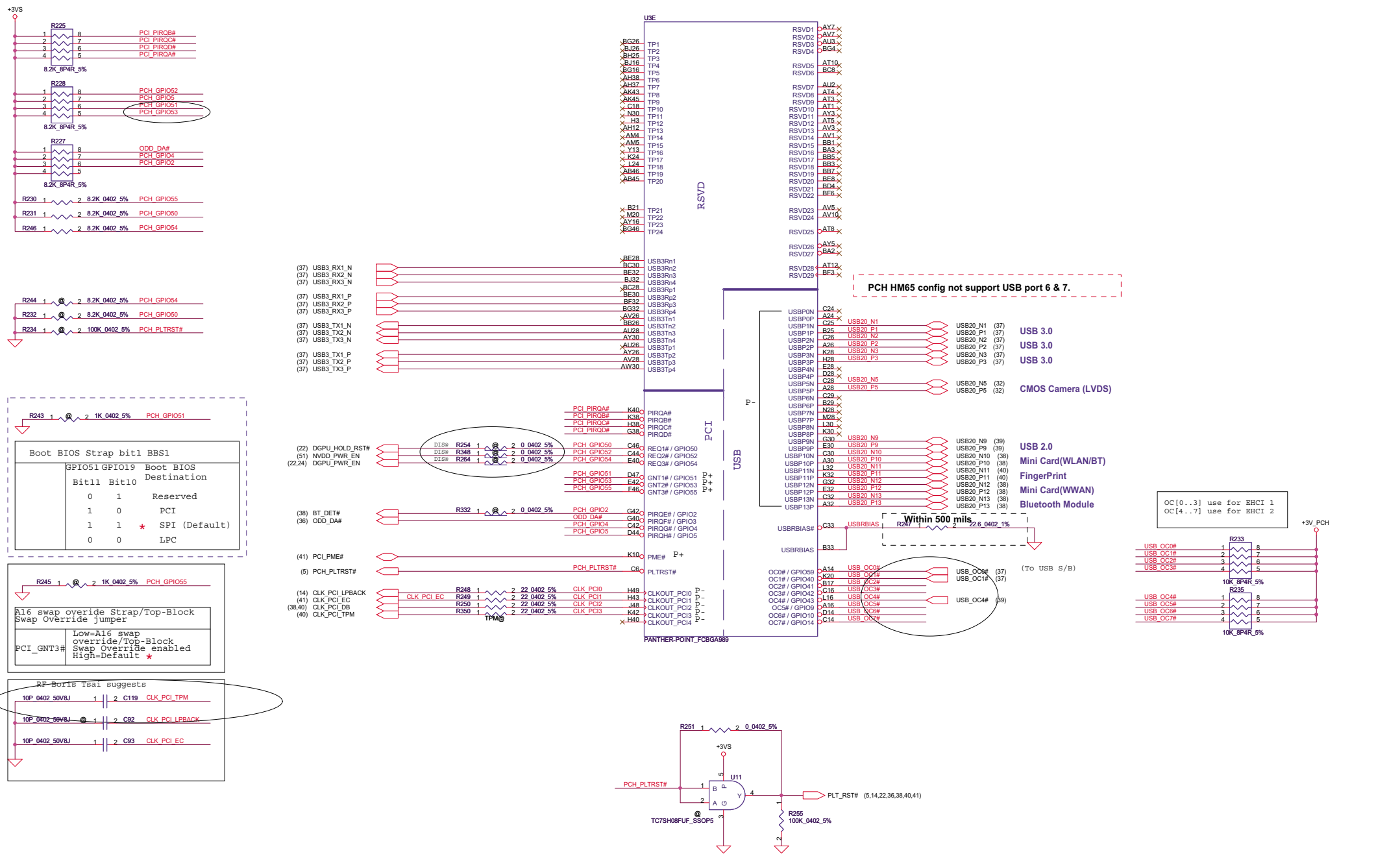
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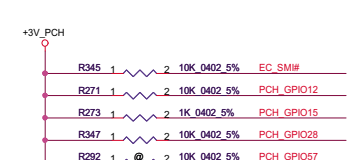
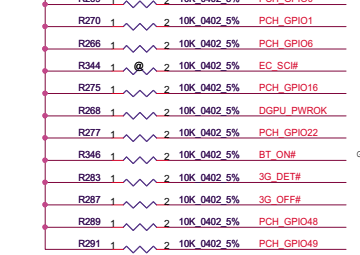
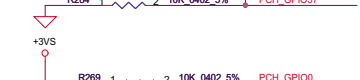
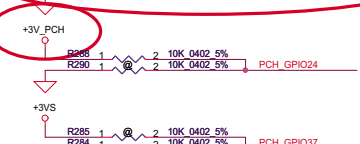
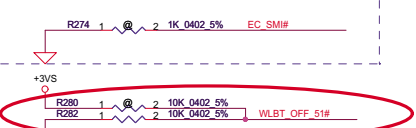
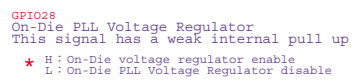
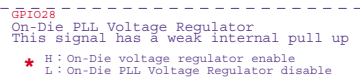


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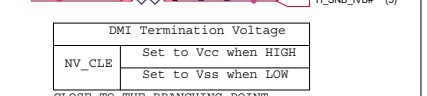
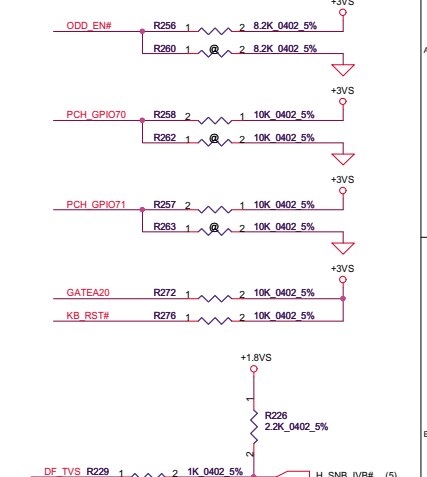
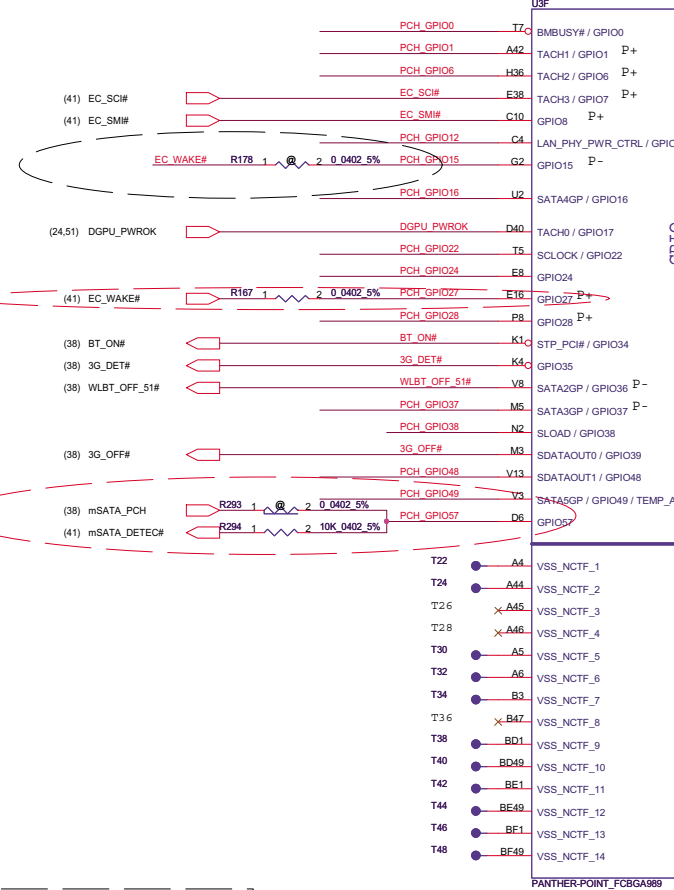
PANTHER-POINT_FCBGA989





For Edge code setting

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA

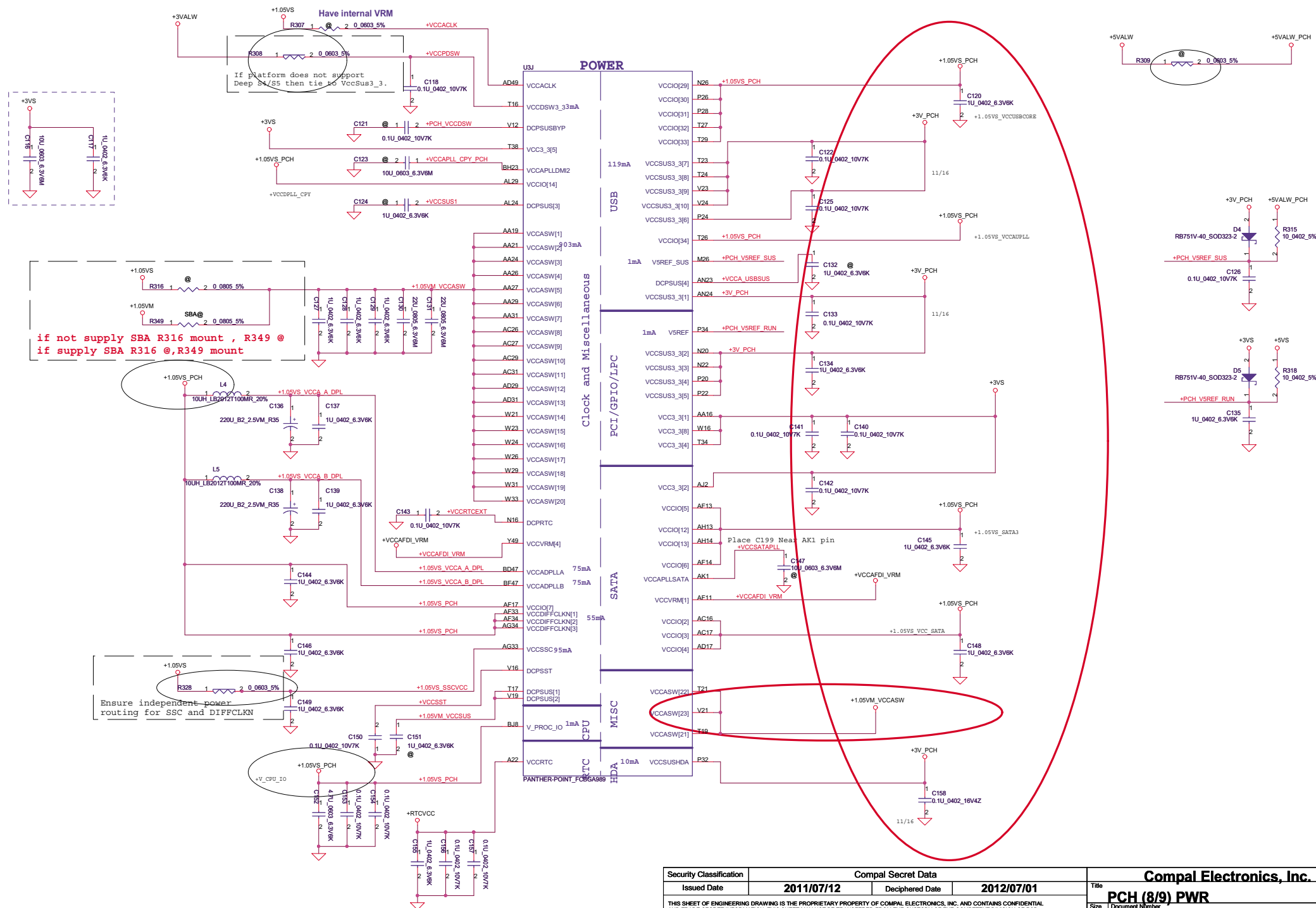


DMI Termination Voltage

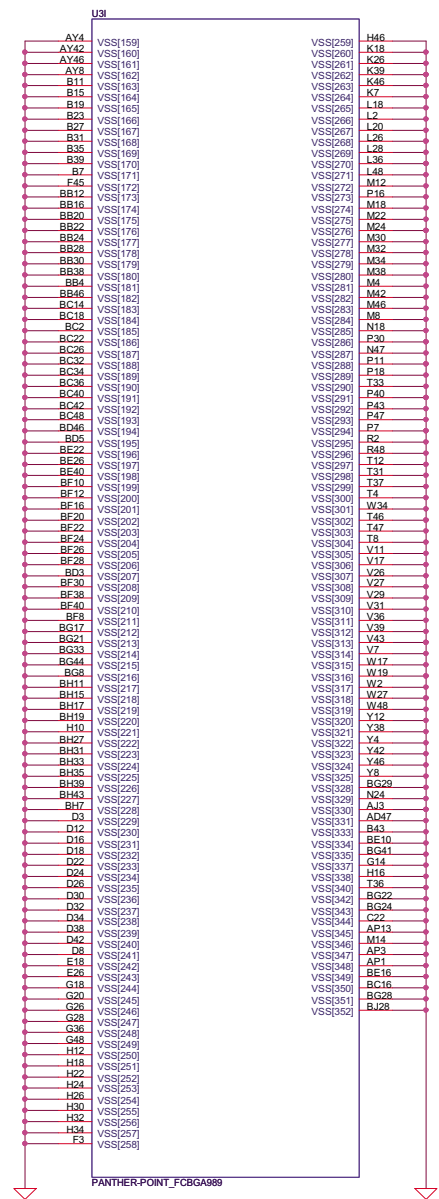
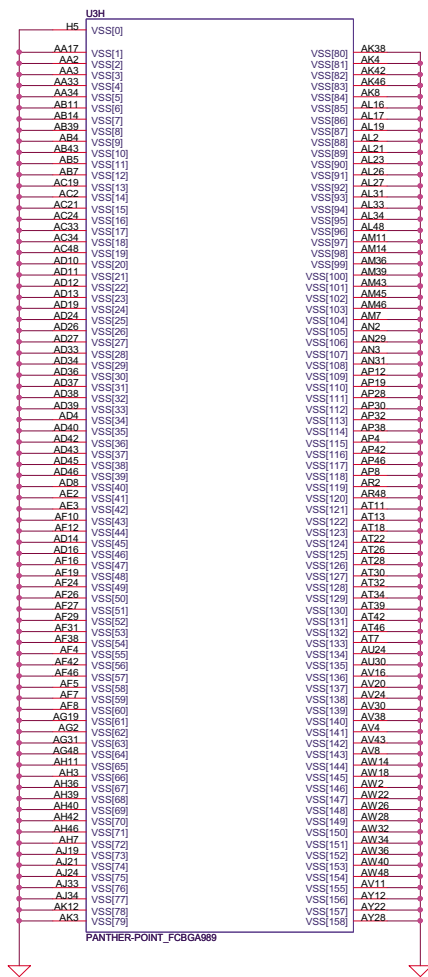
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

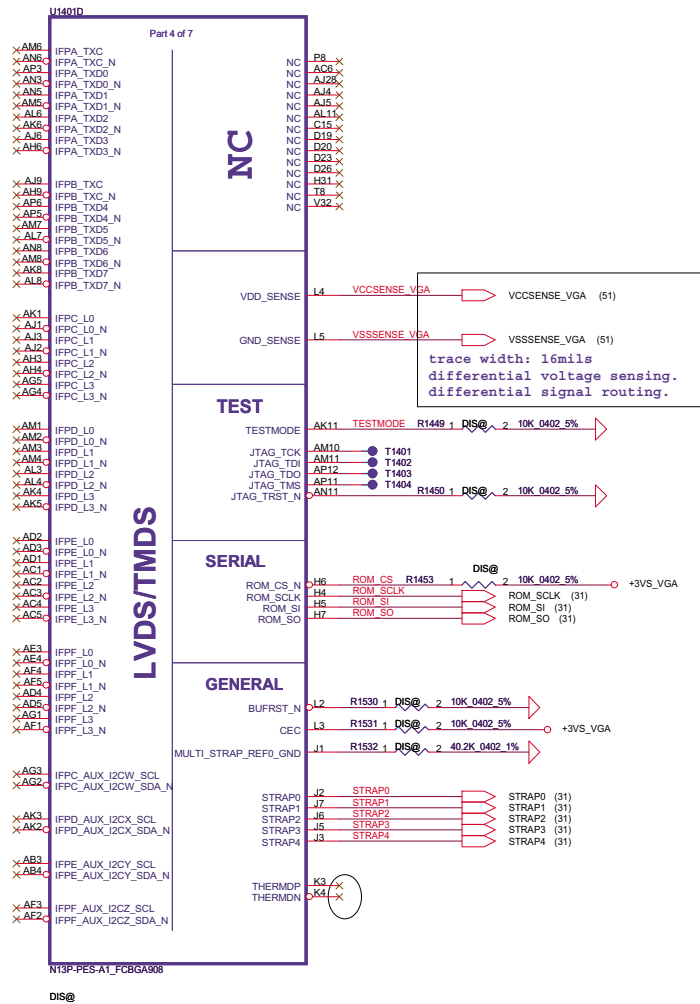
CLOSE TO THE BRANCHING POINT

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

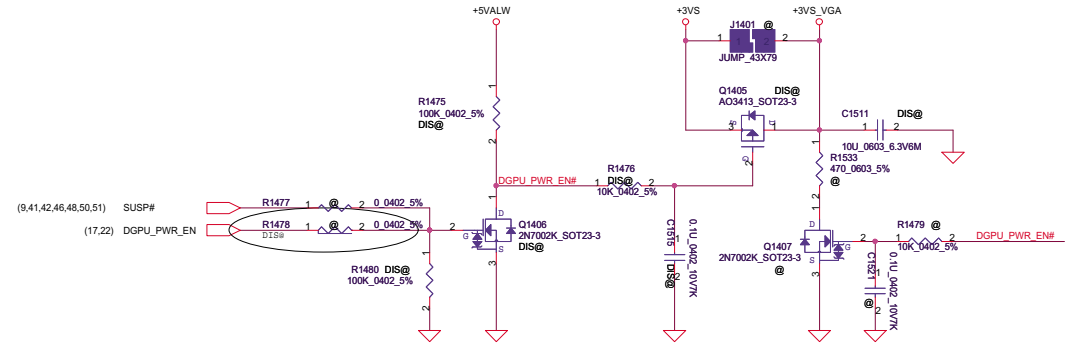
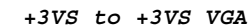
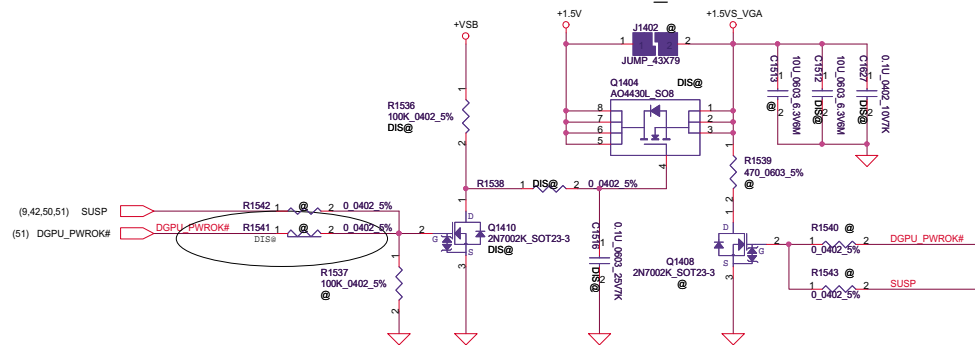
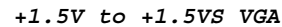
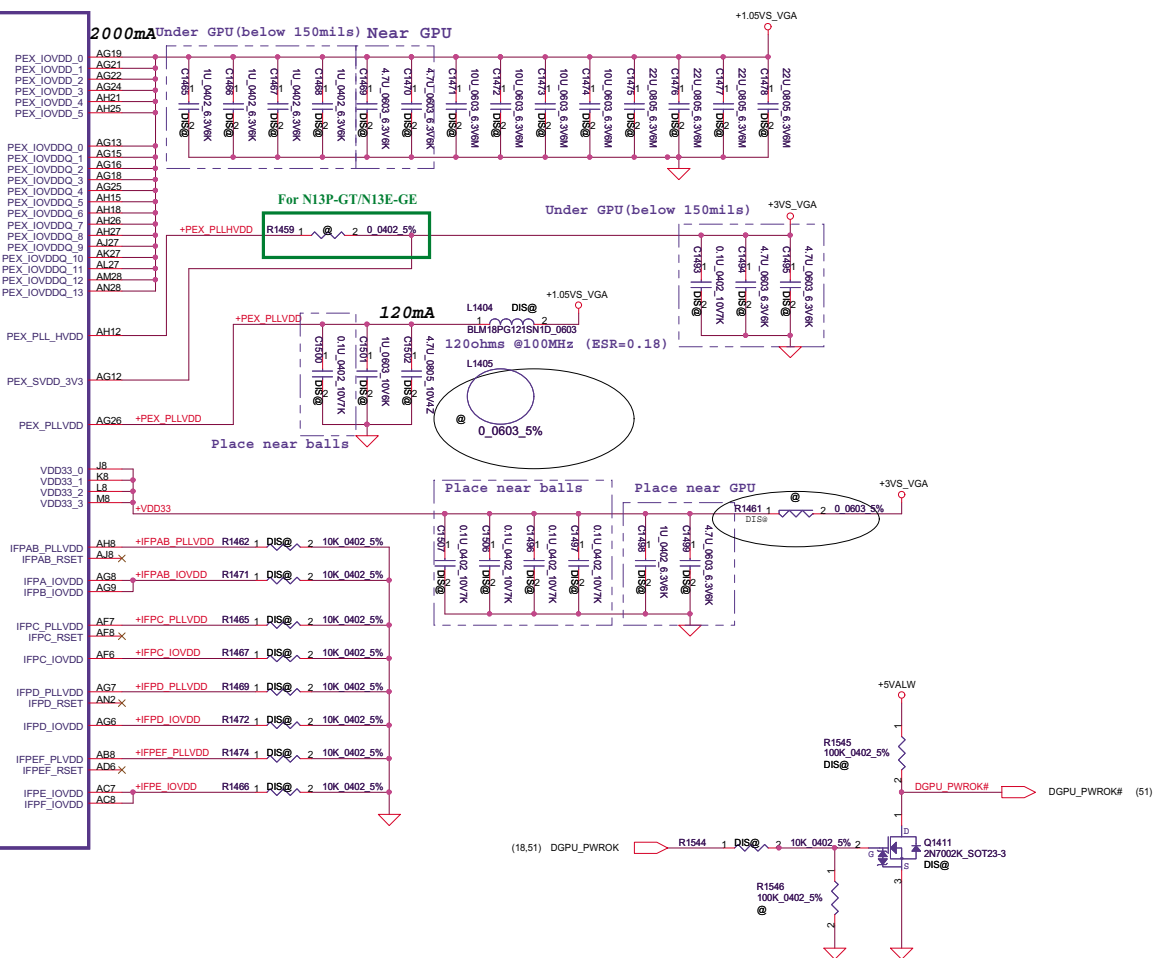
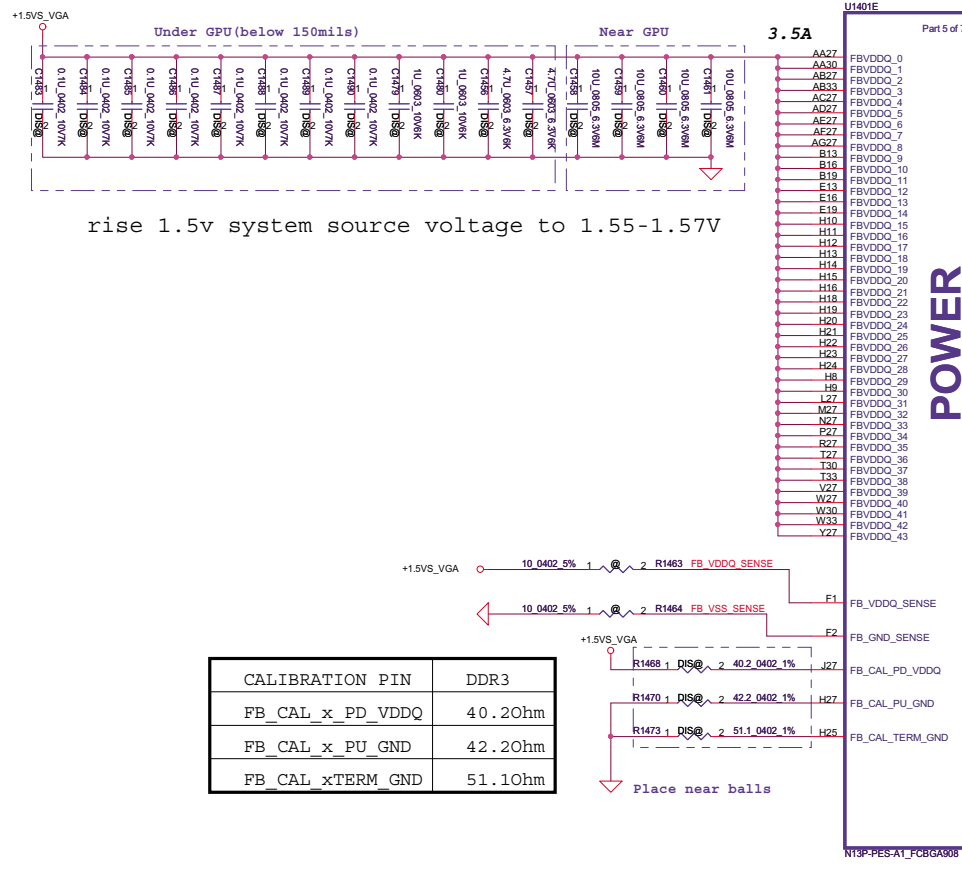


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Date		Friday, January 13, 2012		Sheet	20 of 58

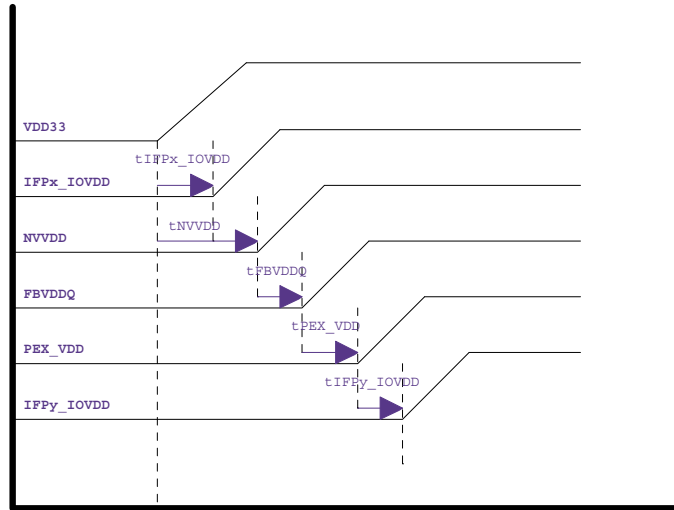
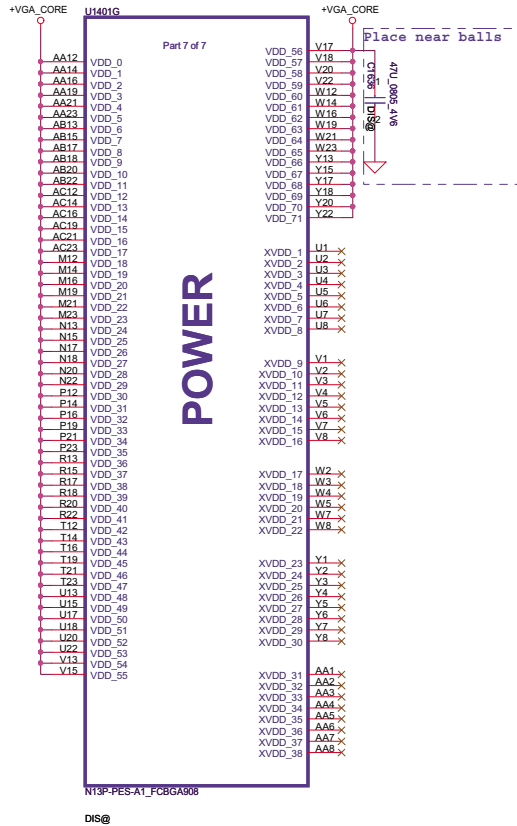




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				Date	Friday, January 13, 2012
				Sheet	23 of 58
				Rev	1.0

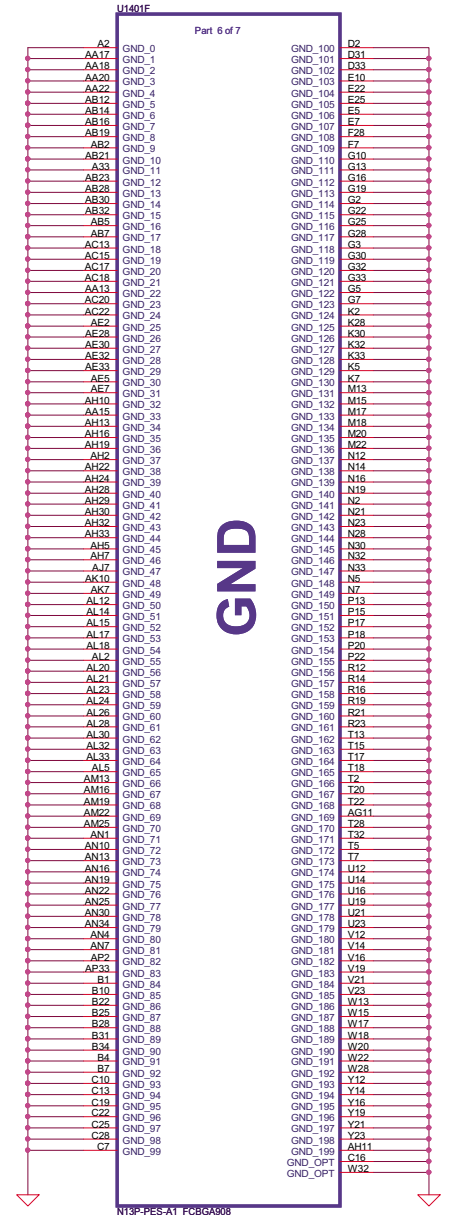


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				Date:	Friday, January 13, 2012	Sheet 24 of 58



NV Recommended Power On Sequencing Order

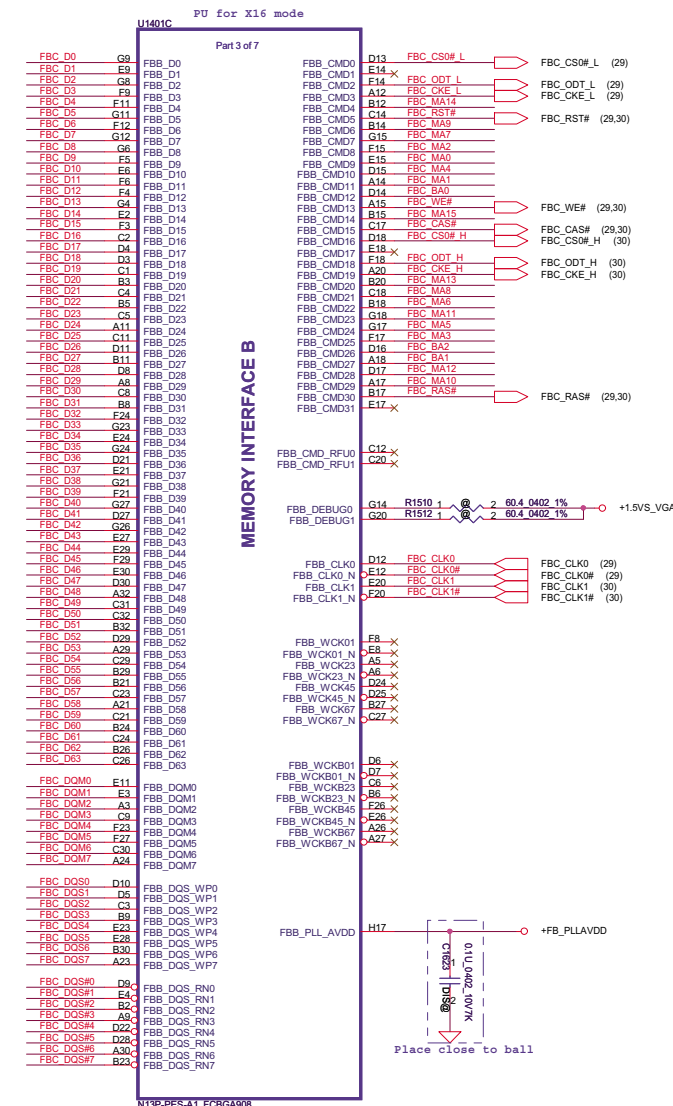
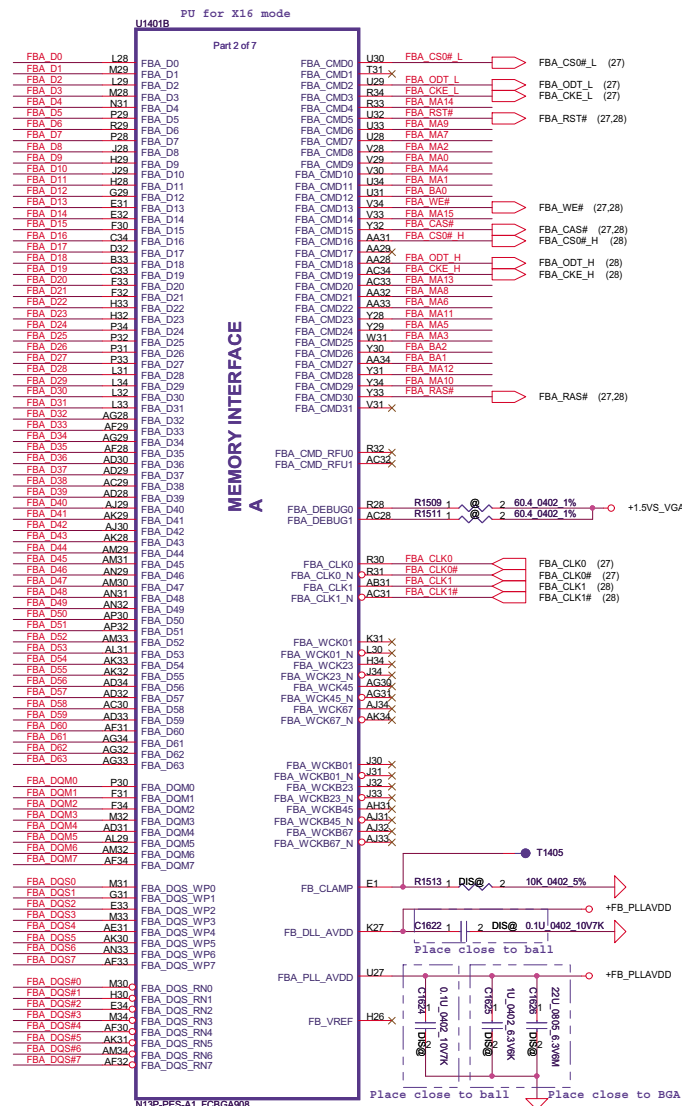
X=A and B
Y=C,D,E and F



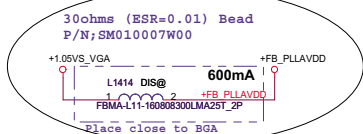
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N13X-VGA CORE, GND
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				Document Number	LA-8133P
				Date	Friday, January 13, 2012
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Mode D - Mirror Mode Mapping

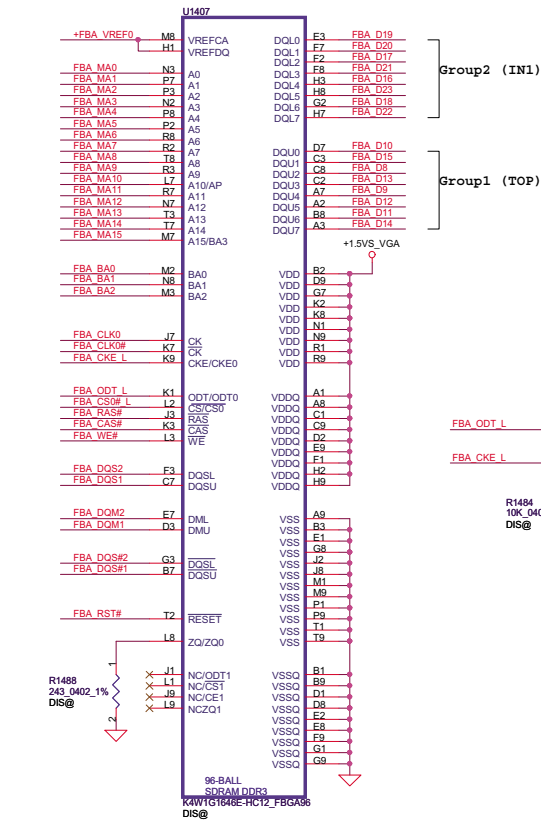
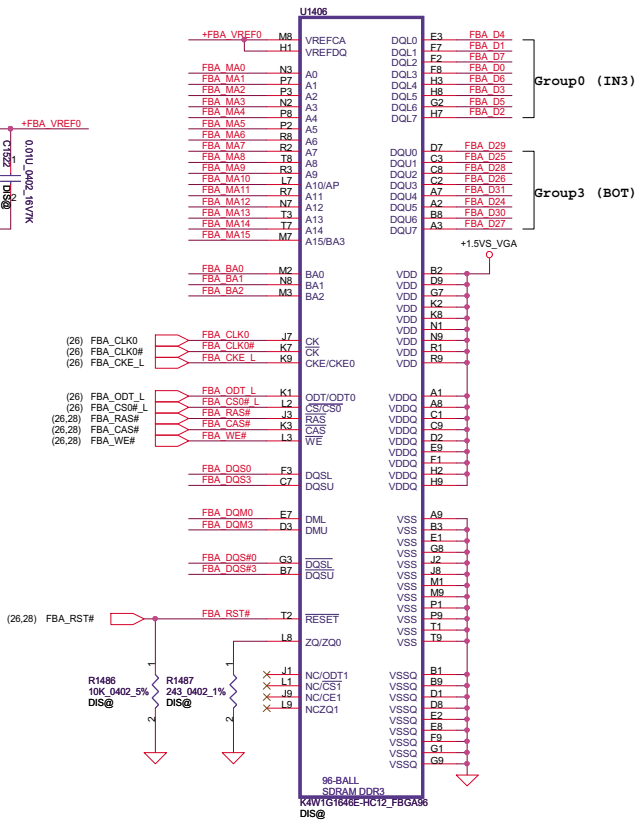


	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS0#_L	
FbX_CMD1		
FbX_CMD2	ODT_L	
FbX_CMD3	CKE_L	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE#	WE#
FbX_CMD14	A15	A15
FbX_CMD15	CAS#	CAS#
FbX_CMD16		CS0#_H
FbX_CMD17		
FbX_CMD18		ODT_H
FbX_CMD19		CKE_H
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS#	RAS#



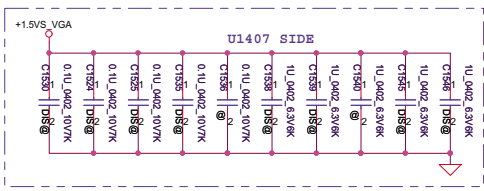
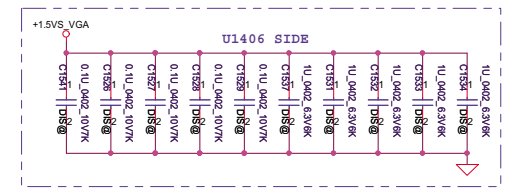
Memory Partition A - Lower 32 bits

- FBA_MA[15..0] (26,28)
- FBA_BA[2..0] (26,28)
- FBA_D[0..63] (26,28)
- FBA_DOM[7..0] (26,28)
- FBA_DQS[7..0] (26,28)
- FBA_DQS# [7..0] (26,28)

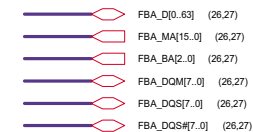
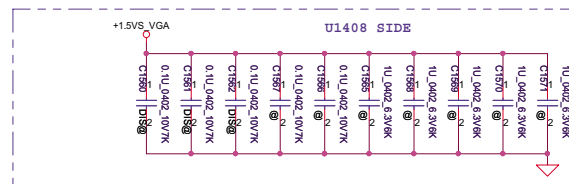
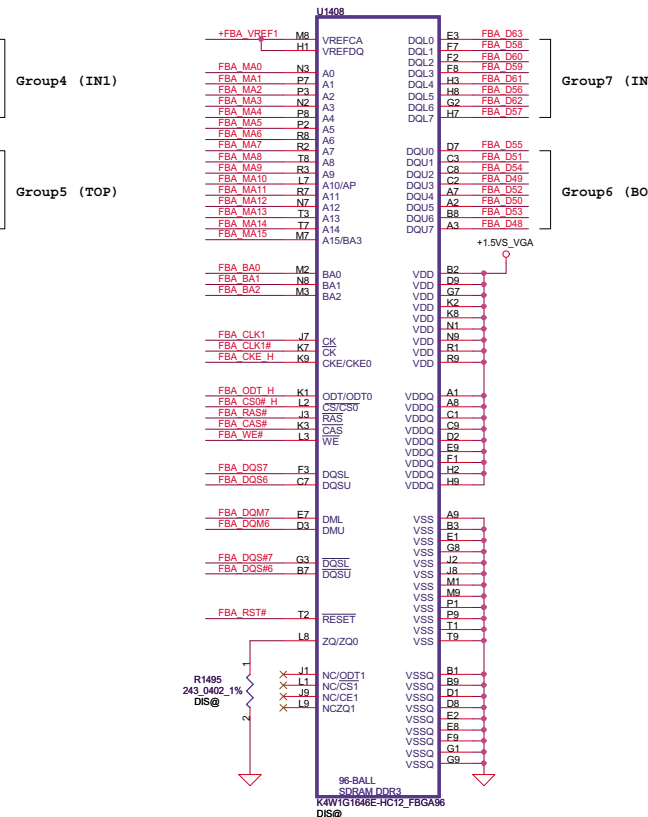
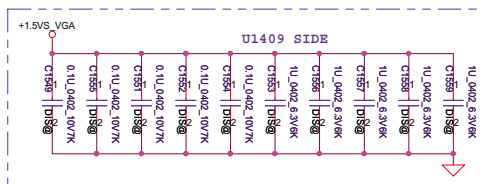
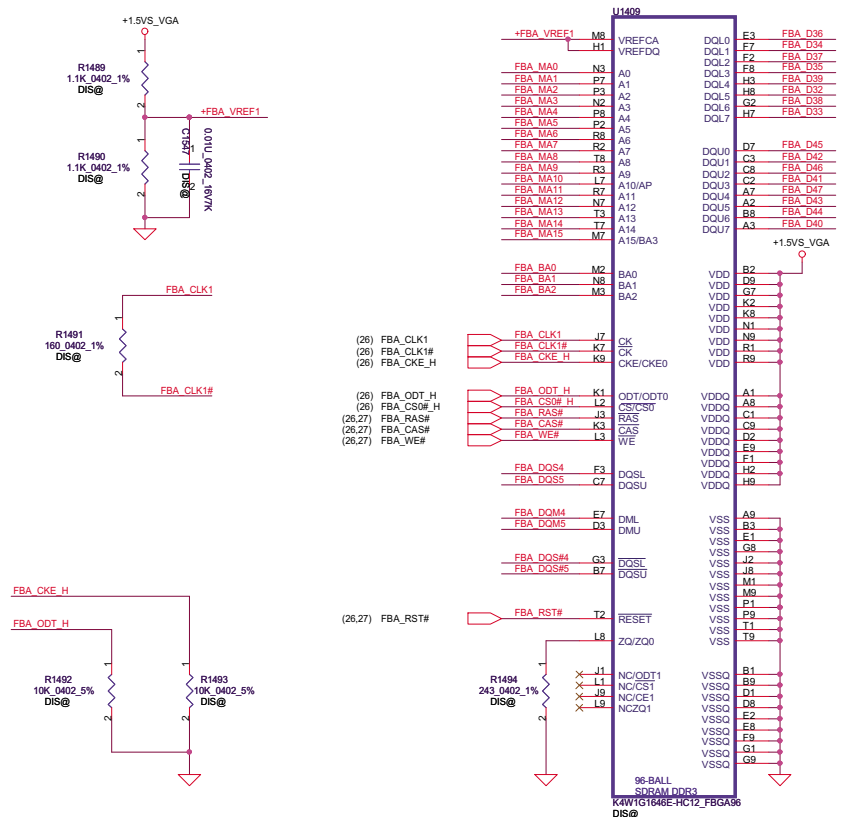


Mode D - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#



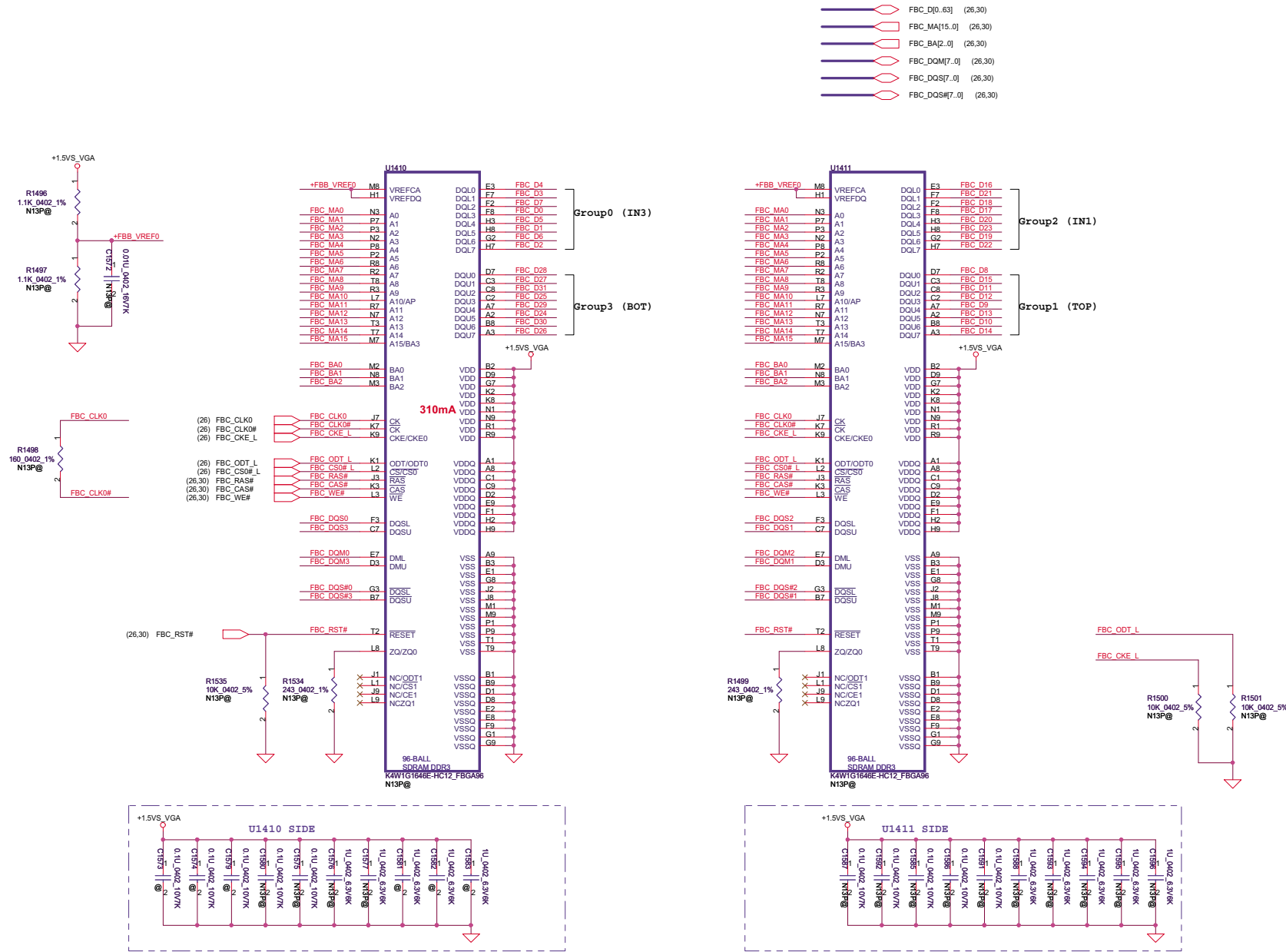
Memory Partition A - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS0#_L	
FBX_CMD1		
FBX_CMD2	ODT_L	
FBX_CMD3	CKE_L	
FBX_CMD4	A14	A14
FBX_CMD5	RST	RST
FBX_CMD6	A9	A9
FBX_CMD7	A7	A7
FBX_CMD8	A2	A2
FBX_CMD9	A0	A0
FBX_CMD10	A4	A4
FBX_CMD11	A1	A1
FBX_CMD12	BA0	BA0
FBX_CMD13	WE#	WE#
FBX_CMD14	A15	A15
FBX_CMD15	CAS#	CAS#
FBX_CMD16	CS0#	
FBX_CMD17		
FBX_CMD18		ODT_H
FBX_CMD19		CKE_H
FBX_CMD20	A13	A13
FBX_CMD21	A8	A8
FBX_CMD22	A6	A6
FBX_CMD23	A11	A11
FBX_CMD24	A5	A5
FBX_CMD25	A3	A3
FBX_CMD26	BA2	BA2
FBX_CMD27	BA1	BA1
FBX_CMD28	A12	A12
FBX_CMD29	A10	A10
FBX_CMD30	RAS#	RAS#

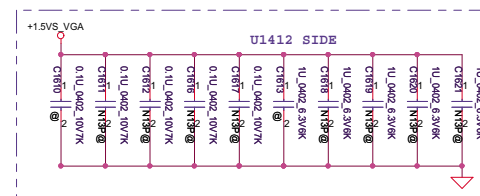
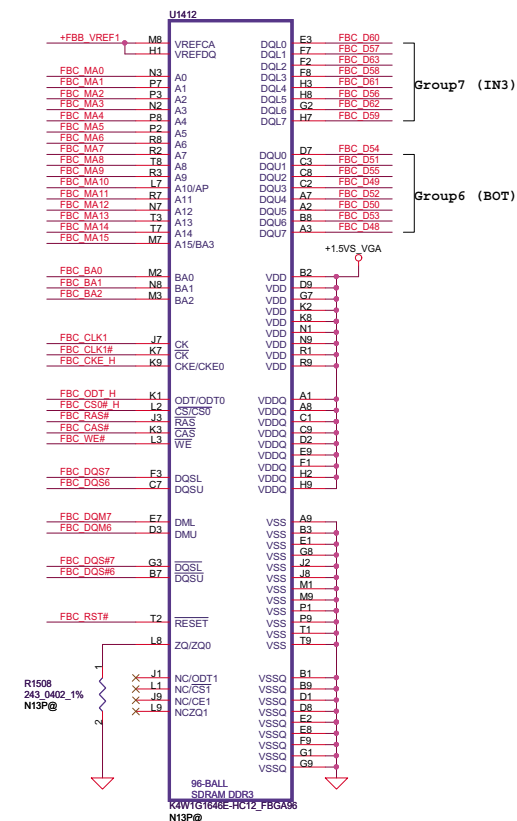
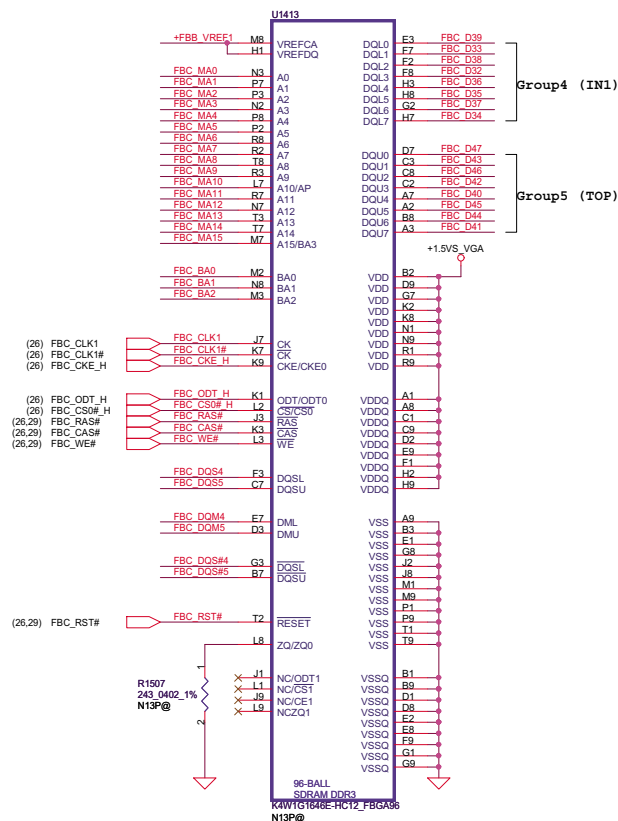
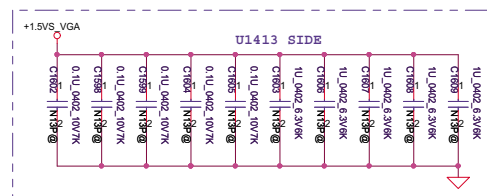
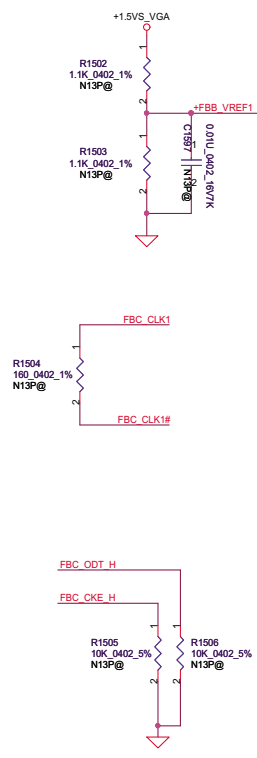
Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

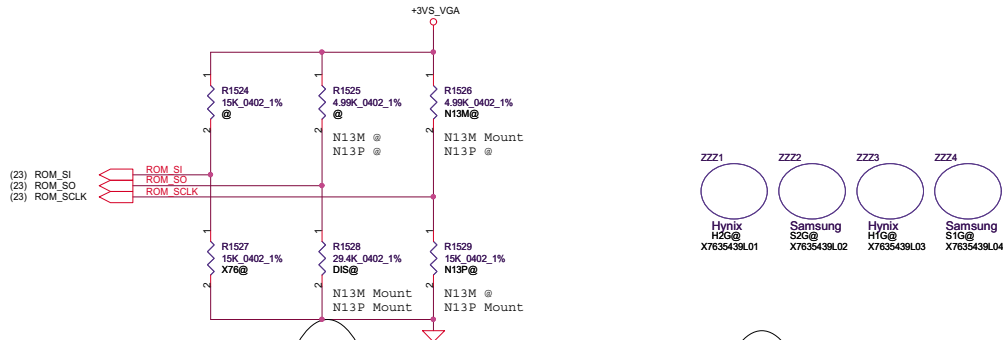
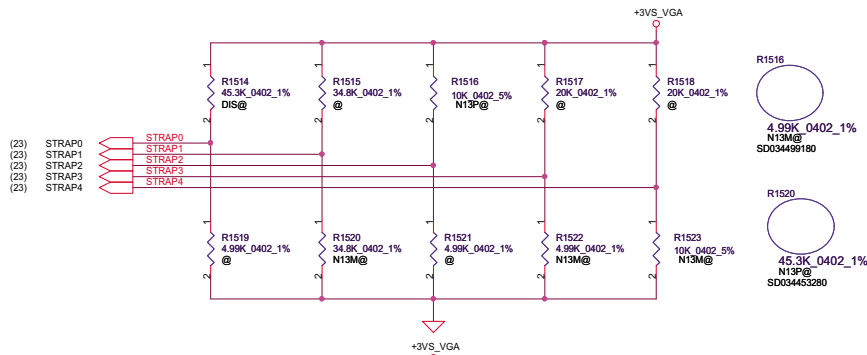
DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#

Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GL	Samsung 900MHz	K4W1G1646G-BC11	PD 10K	PD 15K	PD 20K	PU 45K	PD 45K	PU 10K	NC	NC
		64Mx16						PU 45K(ES)		
	Hynix 900MHz	H5TQ1G63DFR-11C	PD 10K	PD 15K	PD 15K	PU 45K	PD 45K	PU 10K	NC	NC
		64Mx16						PU 45K(ES)		
	Samsung 900MHz	K4W2G1646C-HC11	PD 10K	PD 15K	PD 45K	PU 45K	PD 45K	PU 10K	NC	NC
		128Mx16						PU 45K(ES)		
	Hynix 900MHz	H5TQ2G63BFR-11C	PD 10K	PD 15K	PD 35K	PU 45K	PD 45K	PU 10K	NC	NC
		128Mx16						PU 45K(ES)		

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1	Samsung 900MHz	K4W1G1646G-BC11	PD 30K	PU 5K	PD 20K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		64Mx16								
	Hynix 900MHz	H5TQ1G63DFR-11C	PD 30K	PU 5K	PD 15K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		64Mx16								
	Samsung 900MHz	K4W2G1646C-HC11	PD 30K	PU 5K	PD 45K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		128Mx16								
	Hynix 900MHz	H5TQ2G63BFR-11C	PD 30K	PU 5K	PD 35K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		128Mx16								

9/27
from 15K to 5K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

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				Date	Friday, January 13, 2012
				Sheet	31 of 58
				Rev	1.0
				LA-8133P	

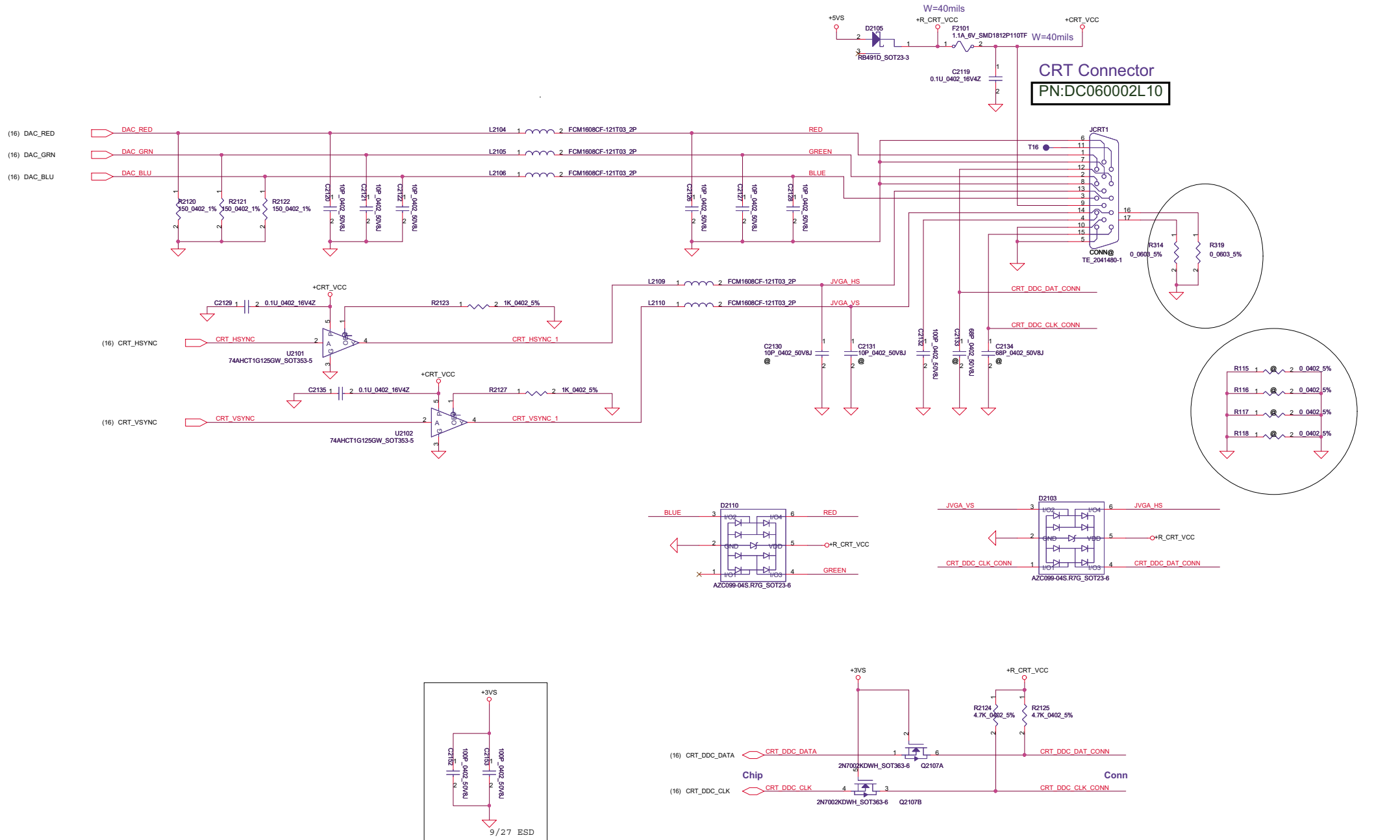




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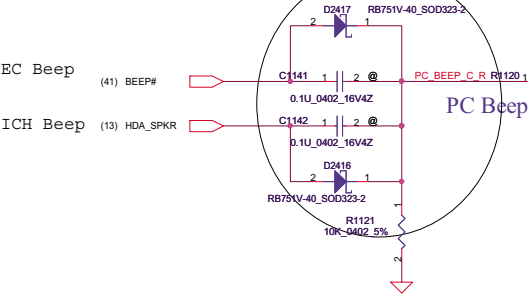


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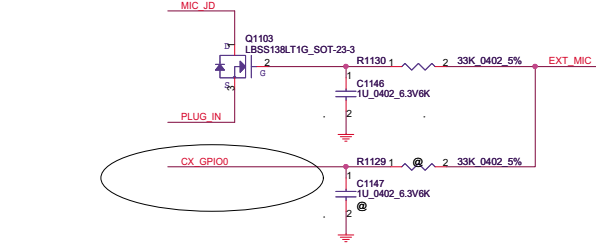


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Date: Friday, January 13, 2012				Sheet 33	of 58

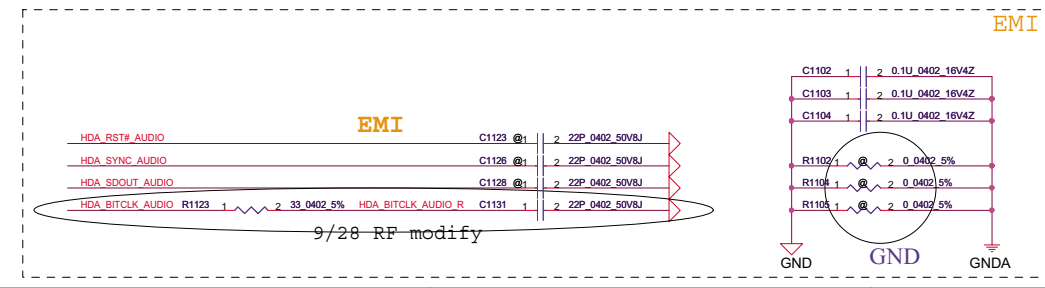
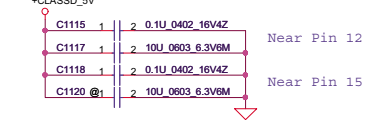
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Combo Jack detect (normal open)

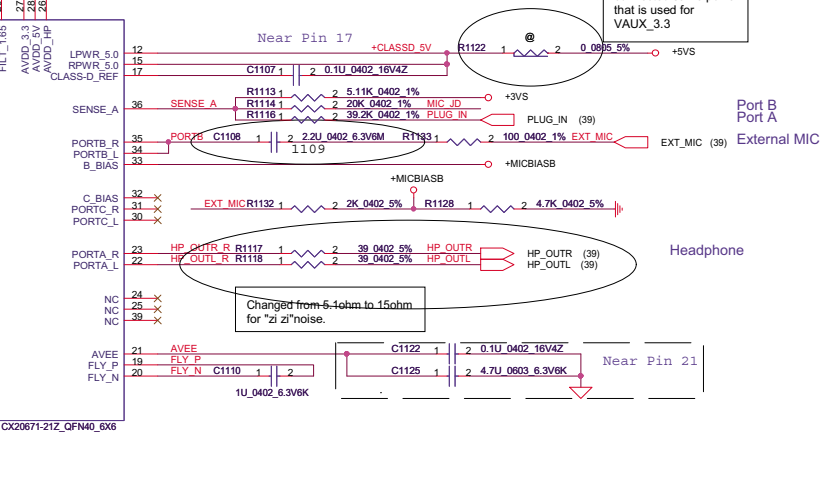
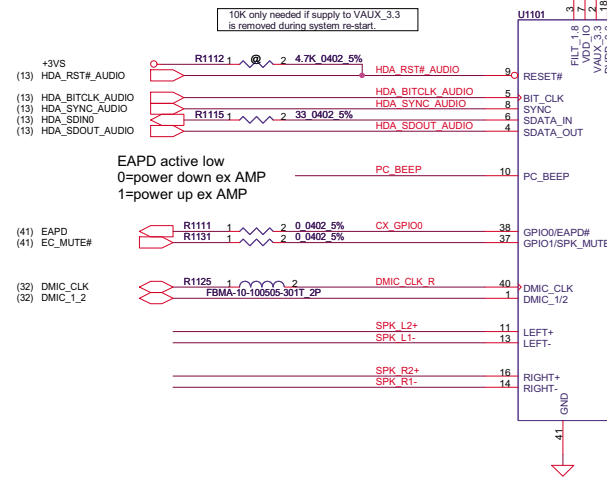
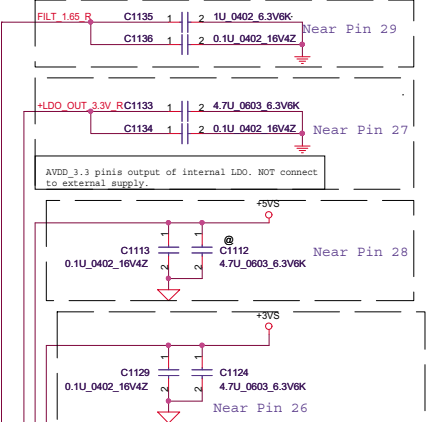
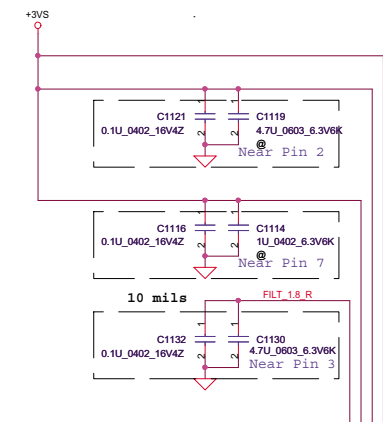


Decoupling CAP



Layout Note: Path from +5VS to Pin12,
Pin15 must be very low
resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC
VAUX_3.3 & VDD_IO pins must be powered by a rail that
is not removed unless AC power is removed.
*DSH page642 has more detail.



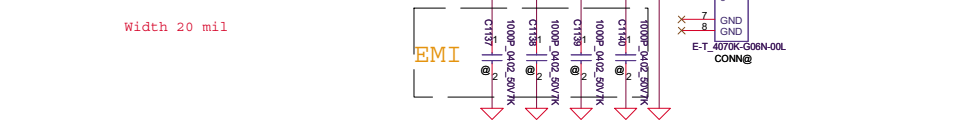
Internal Speaker

SP02000N010
SP02000SM10

EMC request
Bead 120ohm on these signals
Compal PN: SM010016720
Vendor PN: FBMA-L11-160808-121LMT

Rdc < 0.05 ohms
Rated Current > 2A

SPK R1- L1102 1 2 0.0603 5% SPK R1- CONN
SPK R2+ L1103 1 2 0.0603 5% SPK R2+ CONN
SPK L1- L1104 1 2 0.0603 5% SPK L1- CONN
SPK L2+ L1105 1 2 0.0603 5% SPK L2+ CONN
SPK RT_DET# R1134 1 2 0.0402 5% SPK RT_DET# R



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8



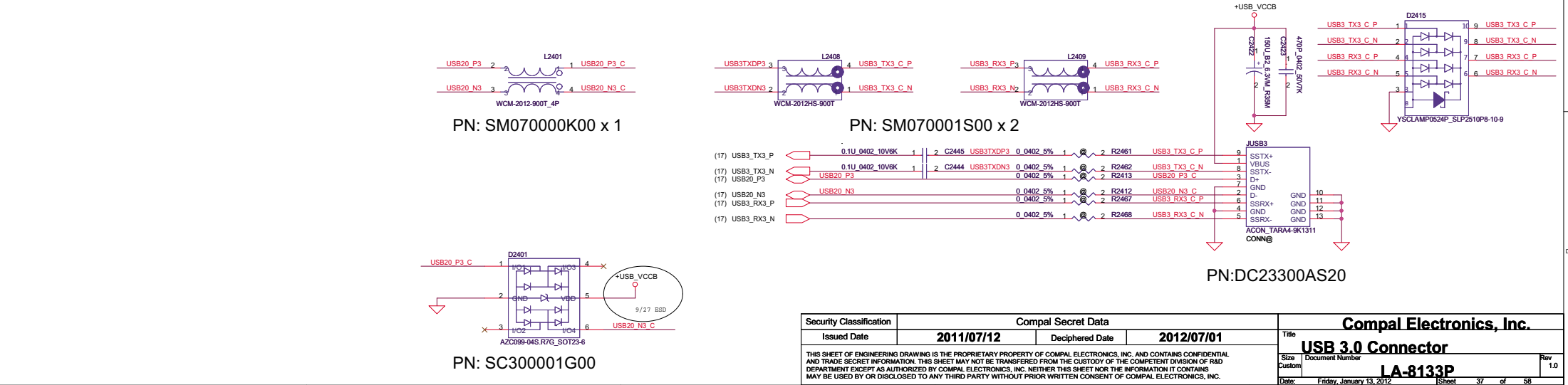
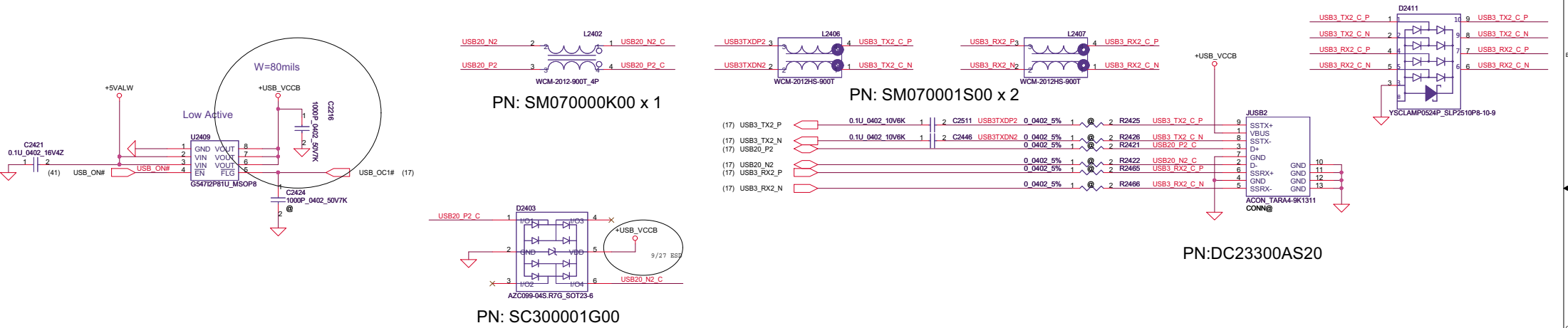
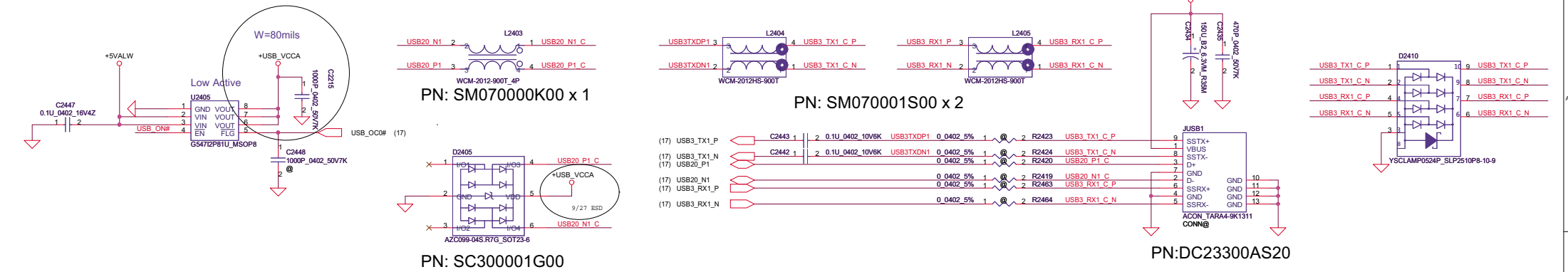
E

2

C

E

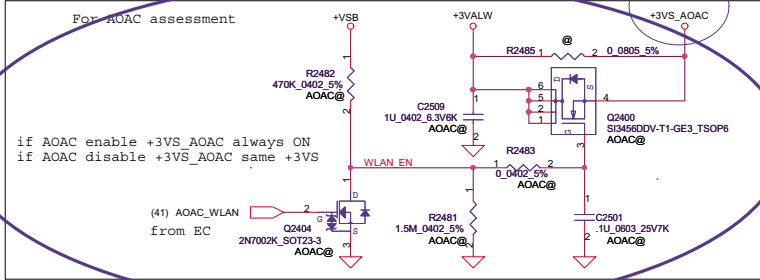
USB 3.0 Conn.



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				Document Number	LA-8133P
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Mini-Express Card(WLAN/WiMAX)

PN:SP07000JP00



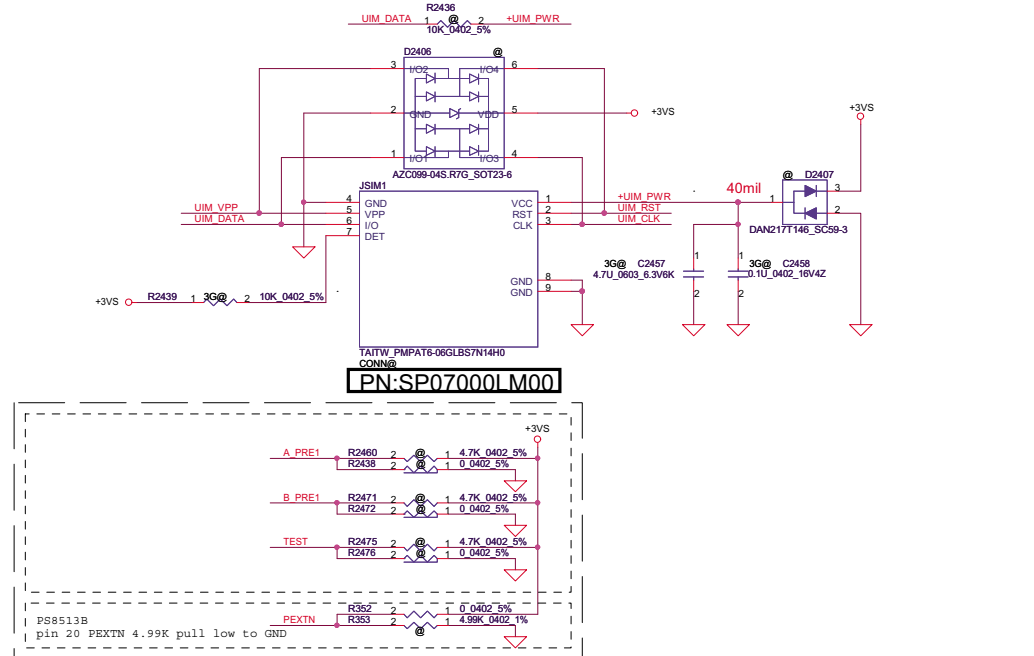
BT Connector

The schematic diagram illustrates the BT Connector circuit. The top section shows the BT1 connector with pins 1 through 8. Pin 1 is connected to +3Vaux_BT (70mA). Pins 2 and 3 are connected to USB20_P13 R and USB20_N13 R. Pins 4 and 5 are connected to USB20_P13 R and USB20_N13 R. Pins 6 and 7 are connected to BT_DET# (17). Pin 8 is connected to ACES_50224-00801-001 CONN@. The bottom section shows the BT@ connector with pins 1 through 2. Pin 1 is connected to +3V. Pin 2 is connected to BT_ON# (17). The circuit includes a Q2411 BT@ AP2301GN-HF_SOT23-3 transistor, a 470_0402_5% resistor (R2477), a 100K_0402_5% resistor (R2109), a 0.1u_0402_16V4Z capacitor (C2513), a 2N7002K_SOT23-3 MOSFET (Q2412), a 27*98_1206 1% resistor (C2506), and a 1W9A5*9_0300 700V diode (BT@).

Reserve for SW mini-pcie debug card.
Series resistors connect to KBC side.

LPC_FRAME# R	R2449	1	Ω	2	0 0402 5%	LPC_FRAME#	LPC_FRAME# (13,40,41)
LPC_AD5 R	R2450	1	Ω	2	0 0402 5%	LPC_AD5	LPC_AD5 (13,40,41)
LPC_AD2 R	R2451	1	Ω	2	0 0402 5%	LPC_AD2	LPC_AD2 (13,40,41)
LPC_AD1 R	R2452	1	Ω	2	0 0402 5%	LPC_AD1	LPC_AD1 (13,40,41)
LPC_AD0 R	R2453	1	Ω	2	0 0402 5%	LPC_AD0	LPC_AD0 (13,40,41)
PLT_RST# R	R2454	1	Ω	2	0 0402 5%	PLT_RST#	LPC_AD1 (13,40,41)
CLK_PCI_DB R	R2429	1	Ω	2	0 0402 5%	CLK_PCI_D	CLK_PCI_D (17,40)

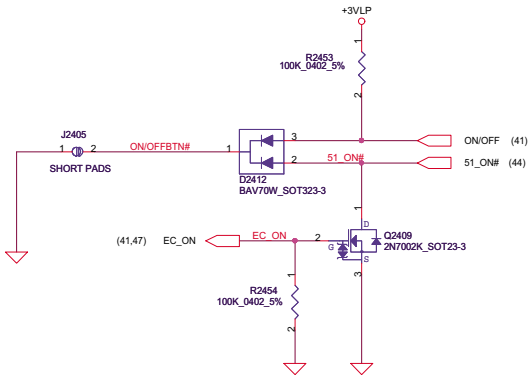
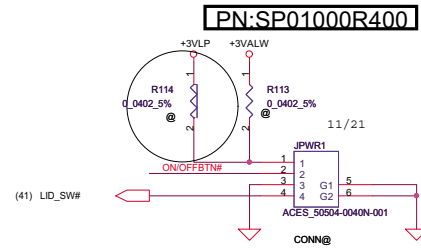
PN:SP07000JP00



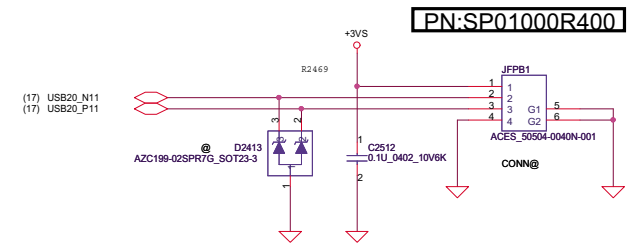
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	WLAN and WWAN/mSATA	
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				Custom		1
				Order	Edition: 1.00 Date: 2011/07/12 20 of 68	

INT_KBD Conn.

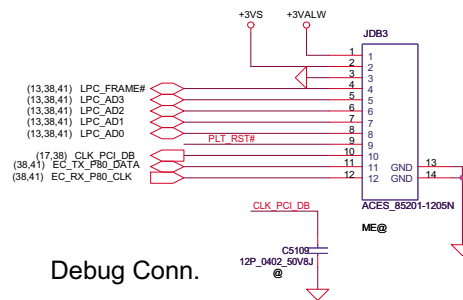
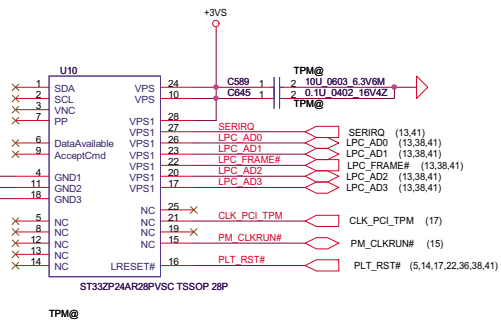
Power Button

**Power Button CONN.**

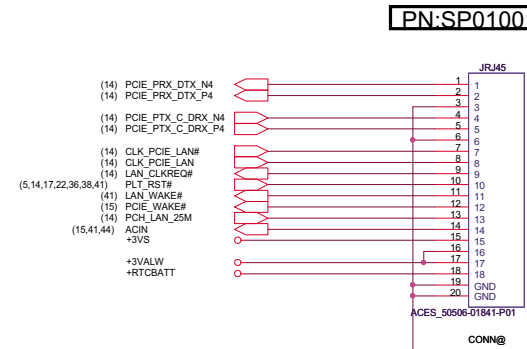
Finger Print Board



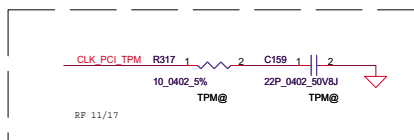
TPM



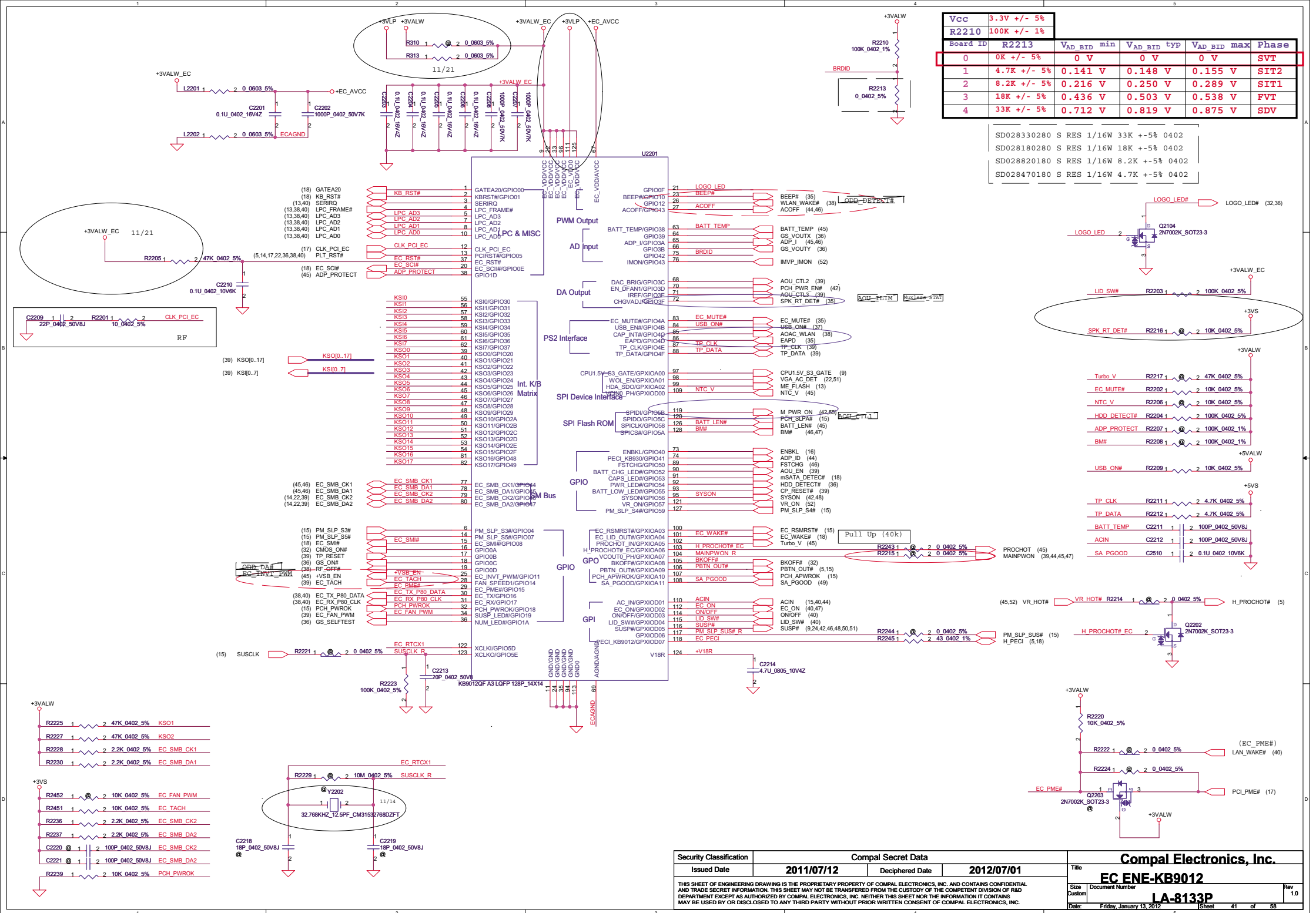
RJ45 Board



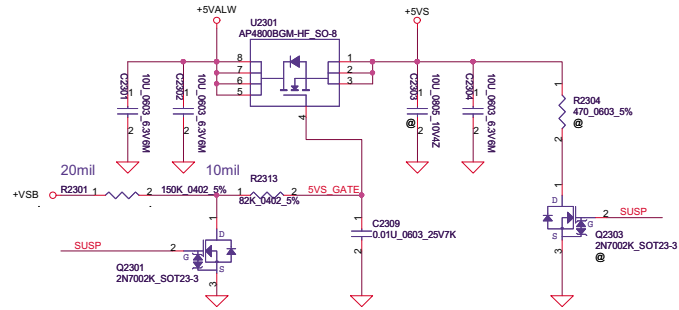
Debug Conn.



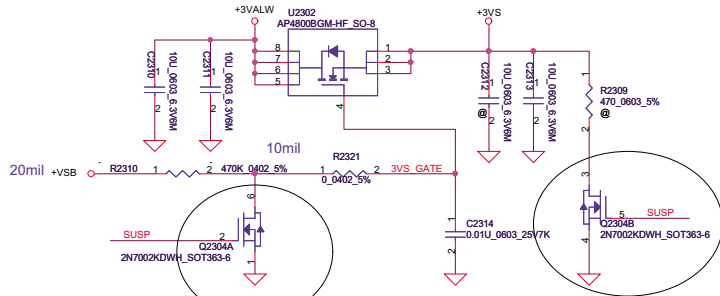
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Issued Date		2011/07/12	Deciphered Date		2012/07/01				
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						Size	Document Number		Rev
						Custom	LA-8133P		1.0
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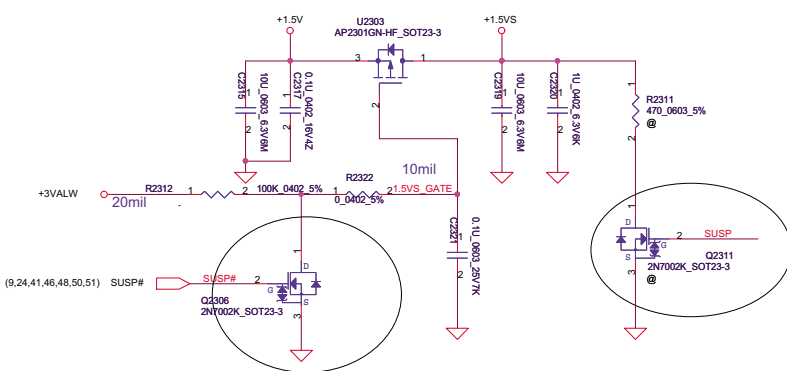
+5VALW TO +5VS



+3VALW TO +3VS

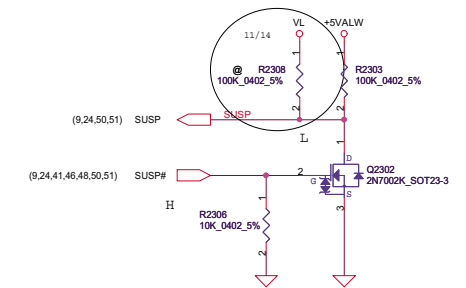
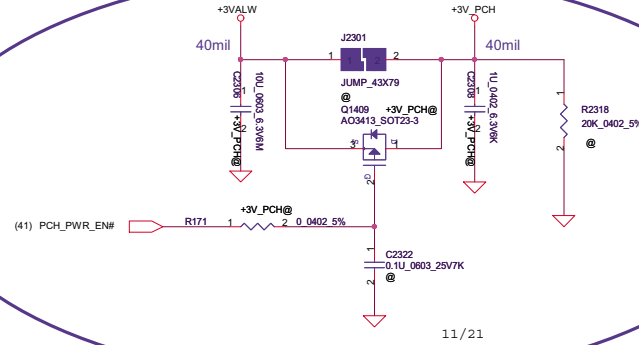


+1.5V to +1.5VS

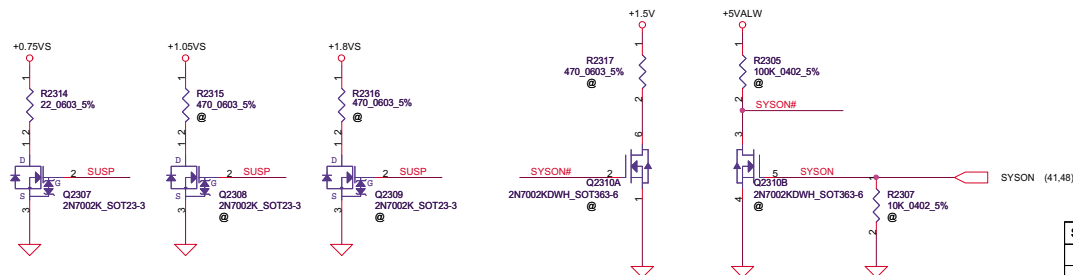
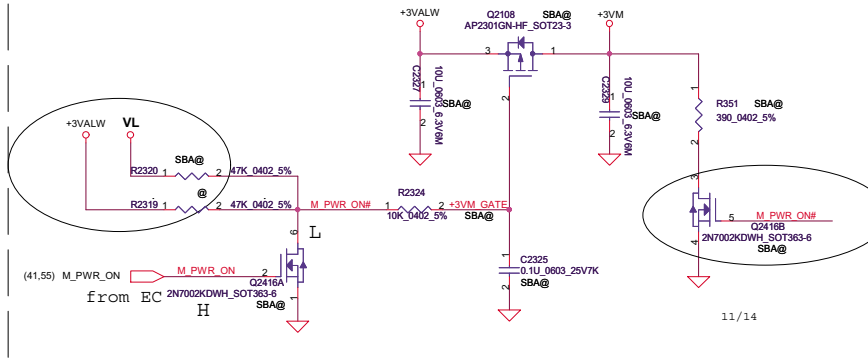


+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3

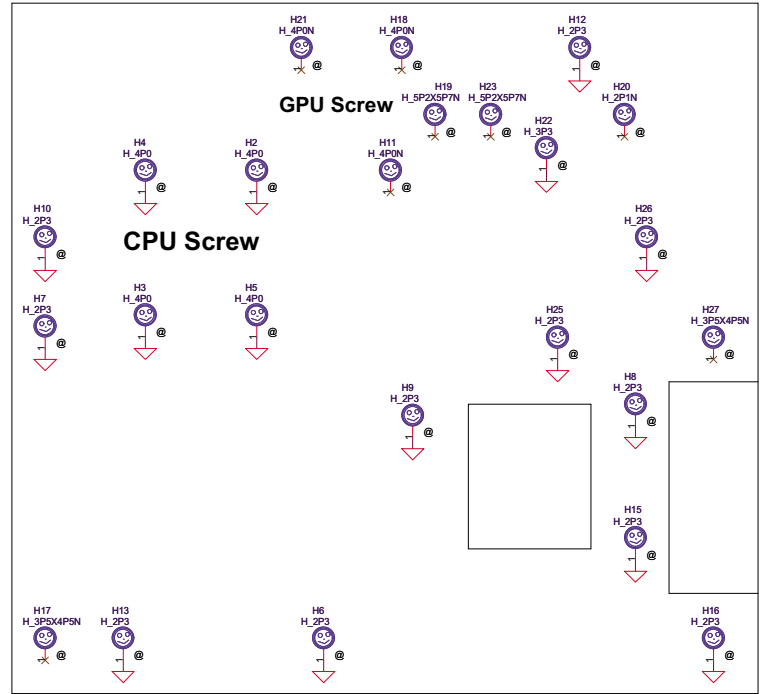


FOR SBA Function POWER(always mount)

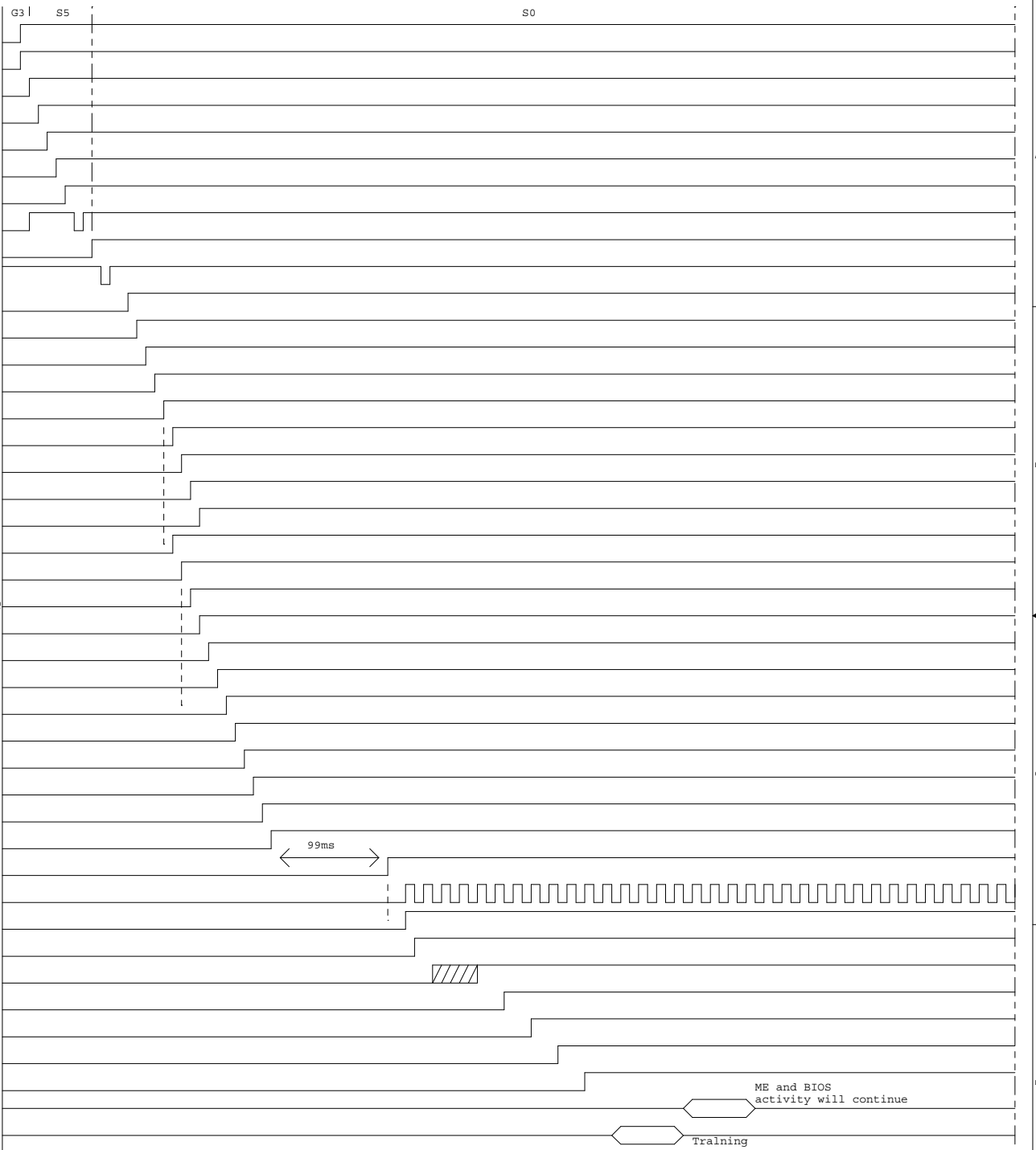


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Screw Hole & FD



RTC
RTCRST
EC_111 pin
EC_ON
MAINPWON
+5VALW
+3VALW/VCCDSW
ON/OFF#
EC_RSMRST#
PBTN_OUT#
SLP_S5#
SLP_S4#
SYSON
SYSON
PCH_SLPA#
M_PWR_ON
+3VM
+1.05VM
PCH_APWROK
SLP_S3#
SUSP#
+1.5V_CPU_VDDQ
+1.8VS
+5VS
+3VS
+1.5VS
+0.75VS
+V1.05VS (VCCP)
+VCCSA
SA_PGOOD
VR_ON
PCH_POK
PCH_CLKOUT
DRAMPWROK
H_CPUPWRGD
CPU_VID
CPU_CORE
VGATE
SYS_PWROK
BUF_PLT_RST#
SPI
DMI

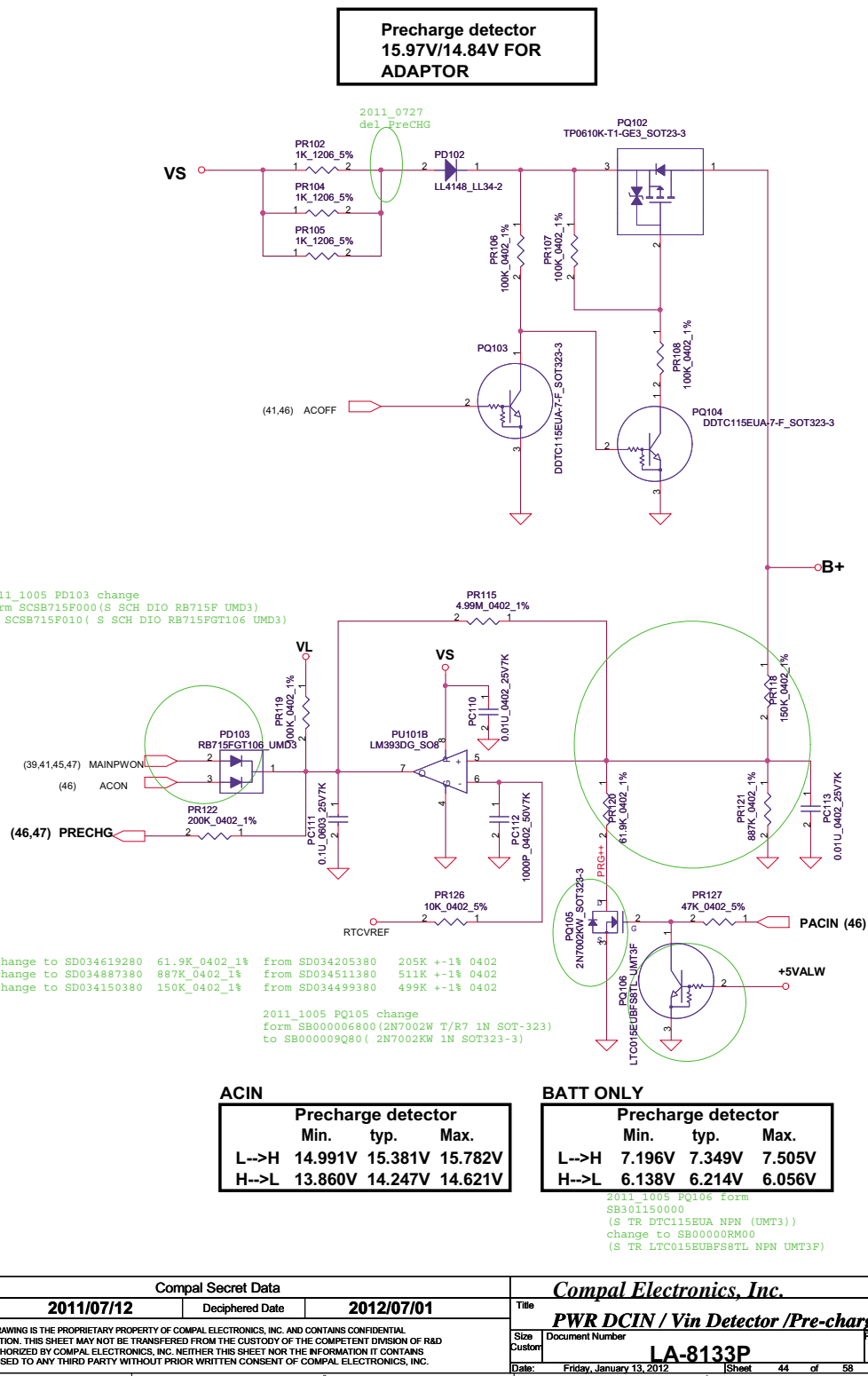
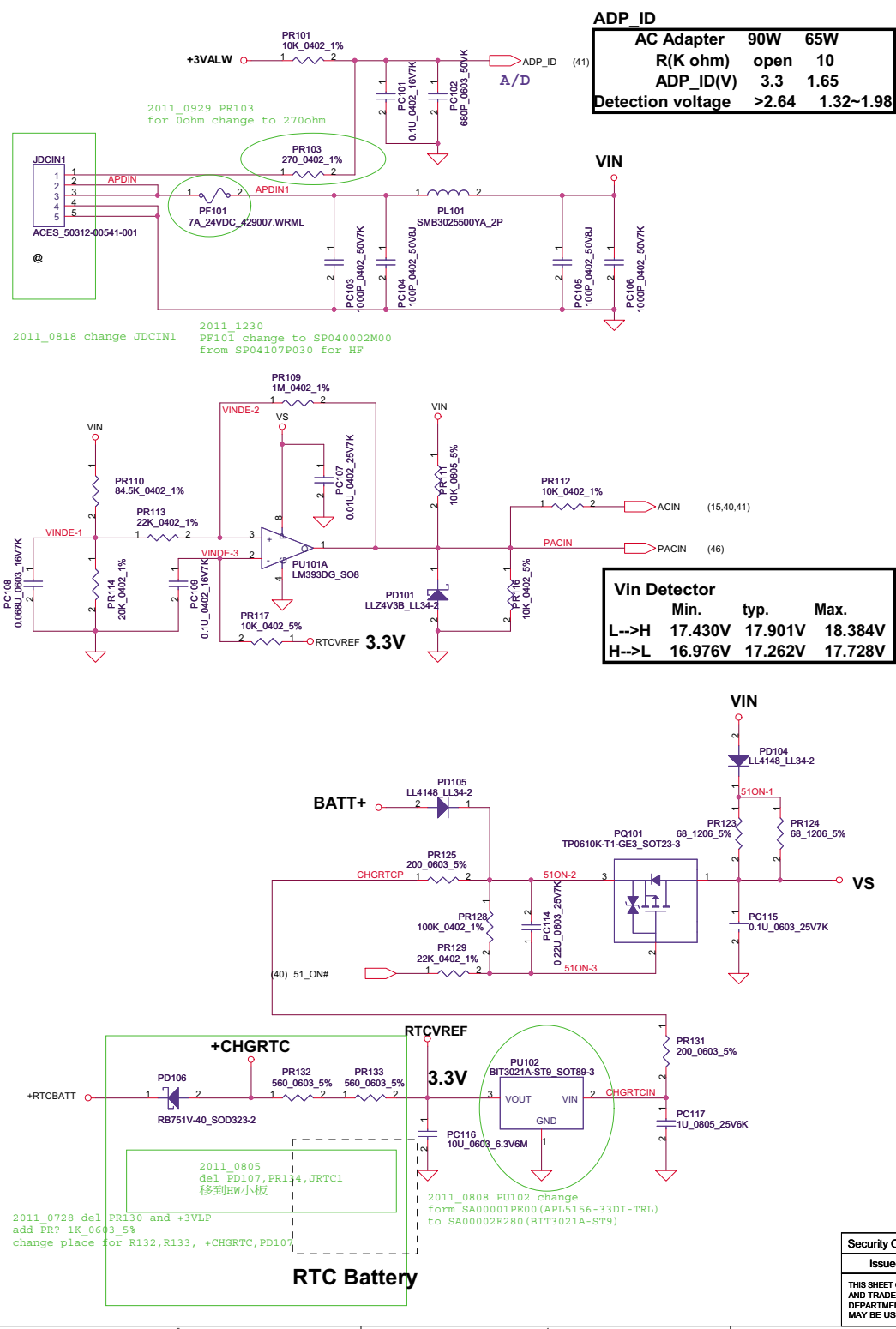


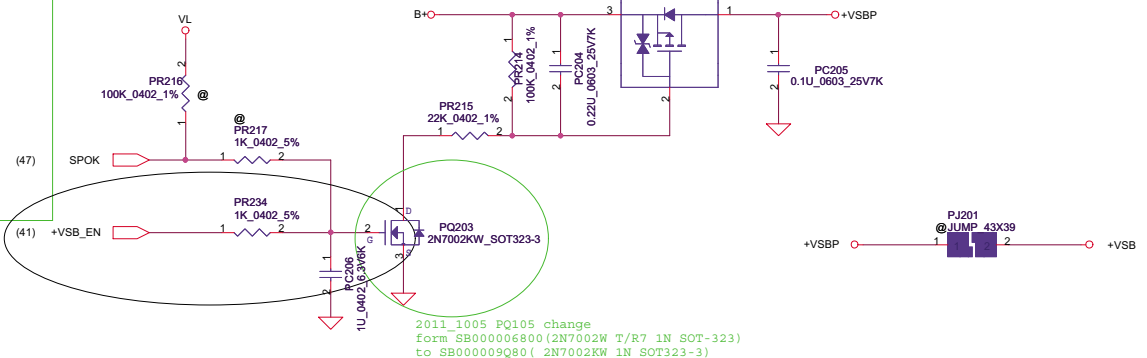
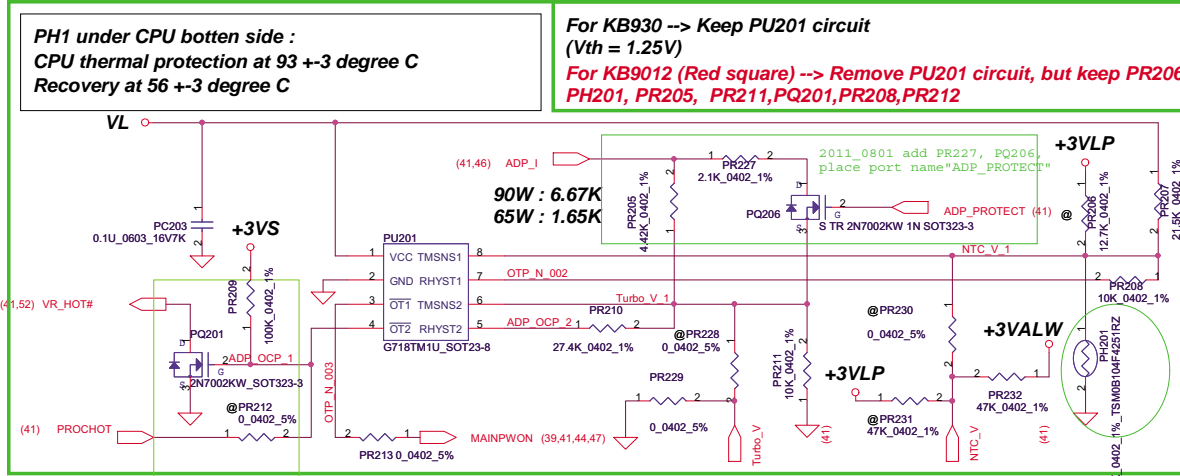
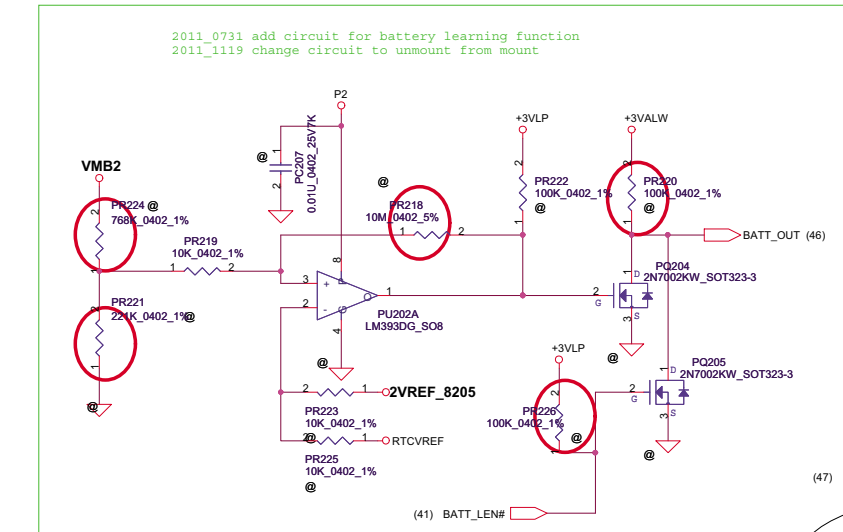
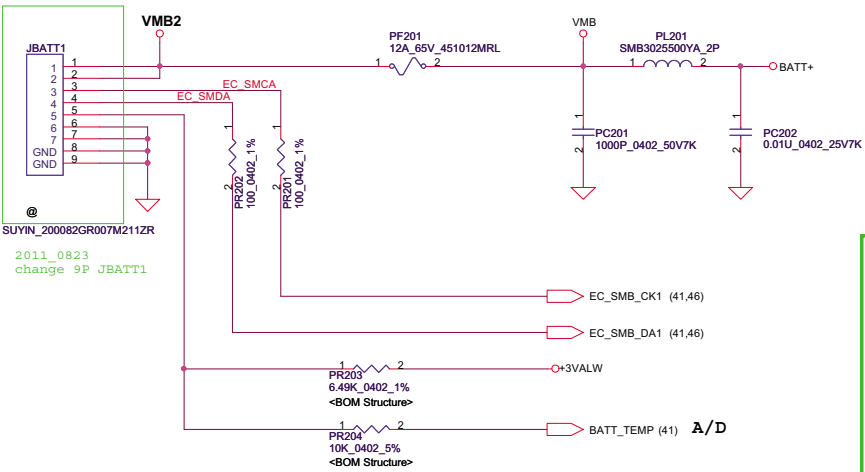
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				Date:	Friday, January 13, 2012
				Sheet	43 of 58

Compal Electronics, Inc.

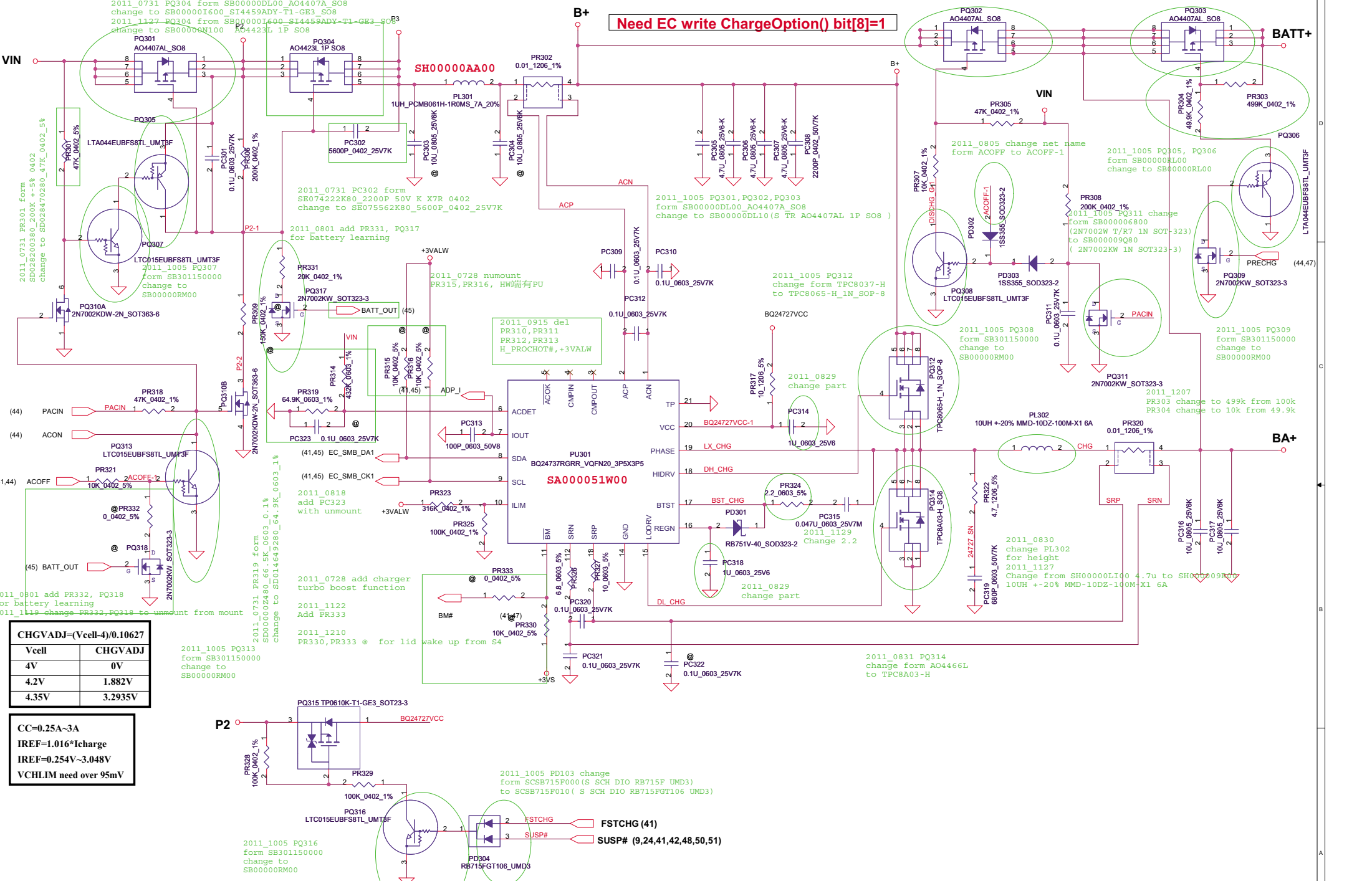
Screw Hole

Rev 1.0





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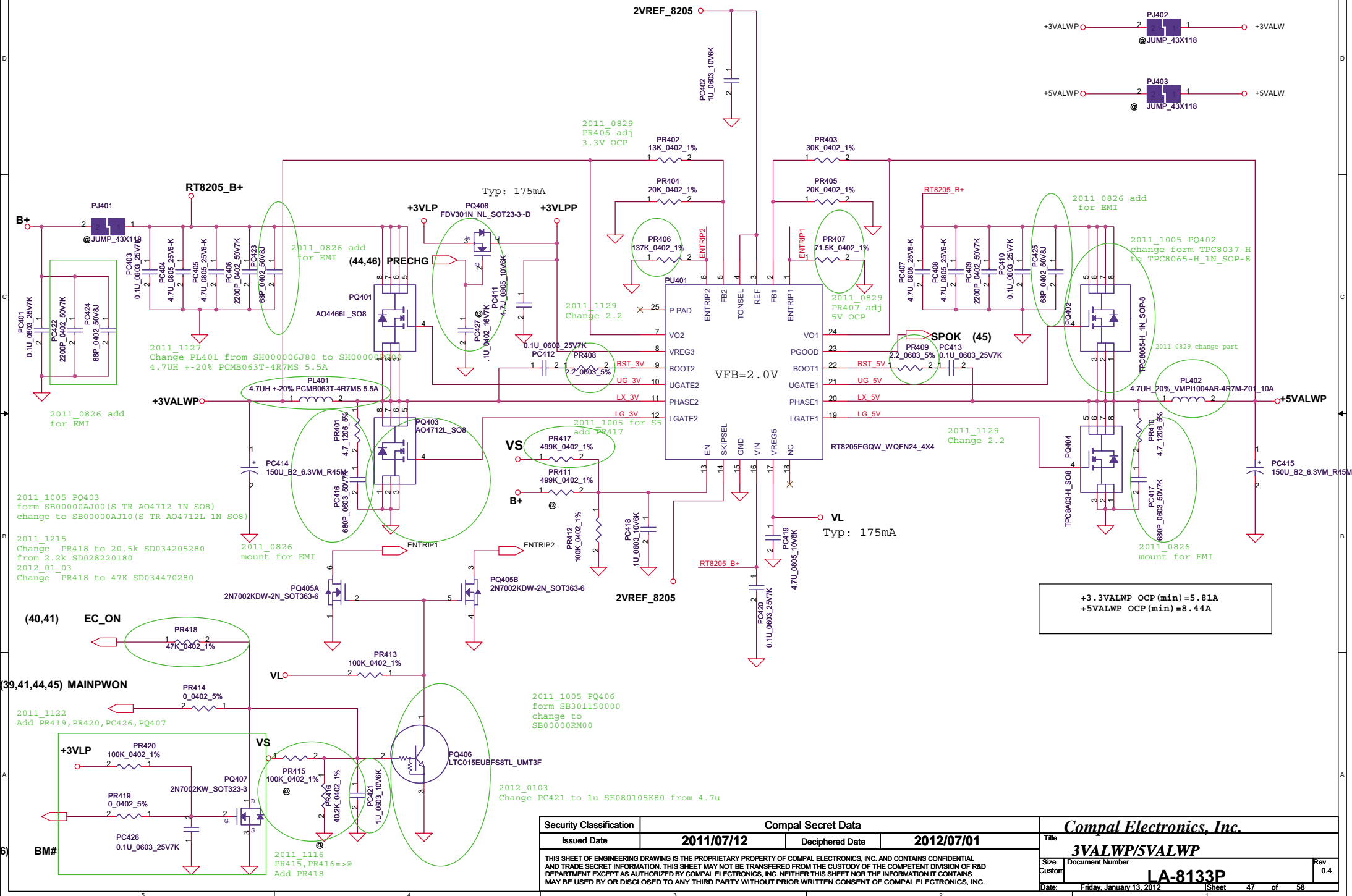


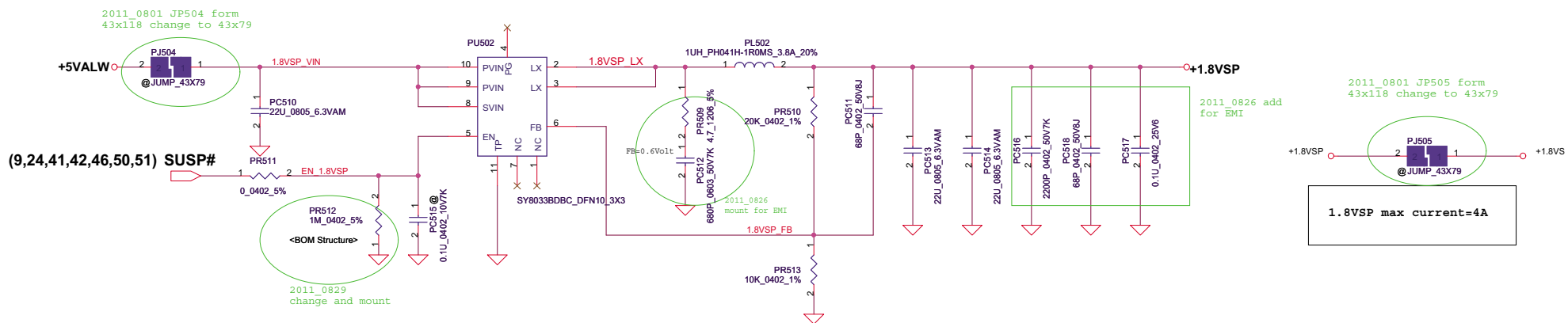
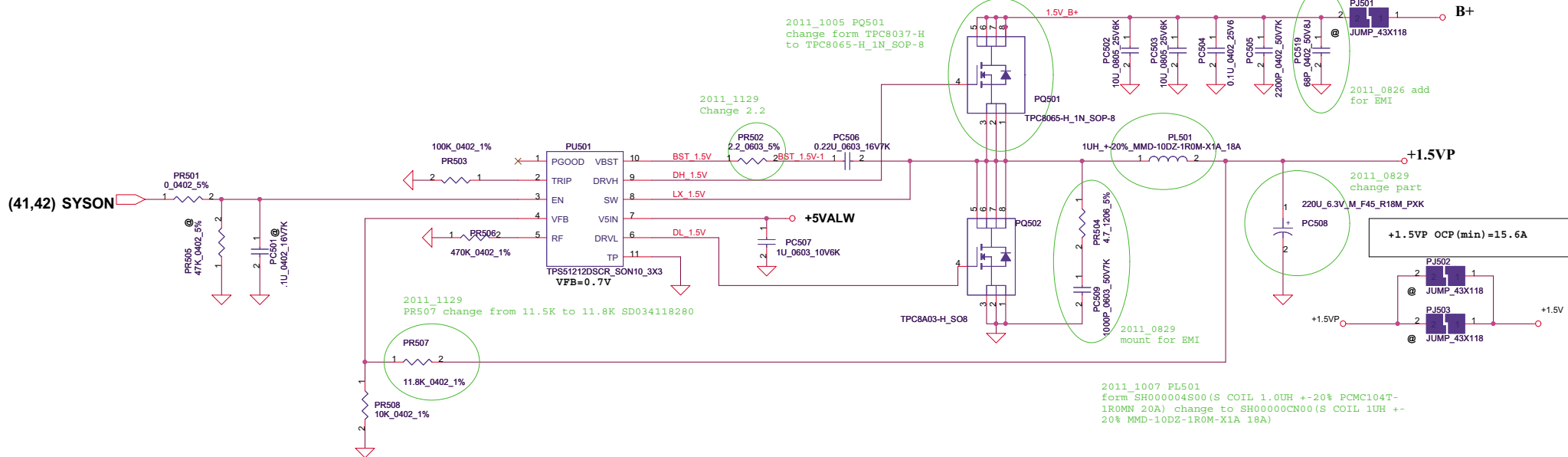
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

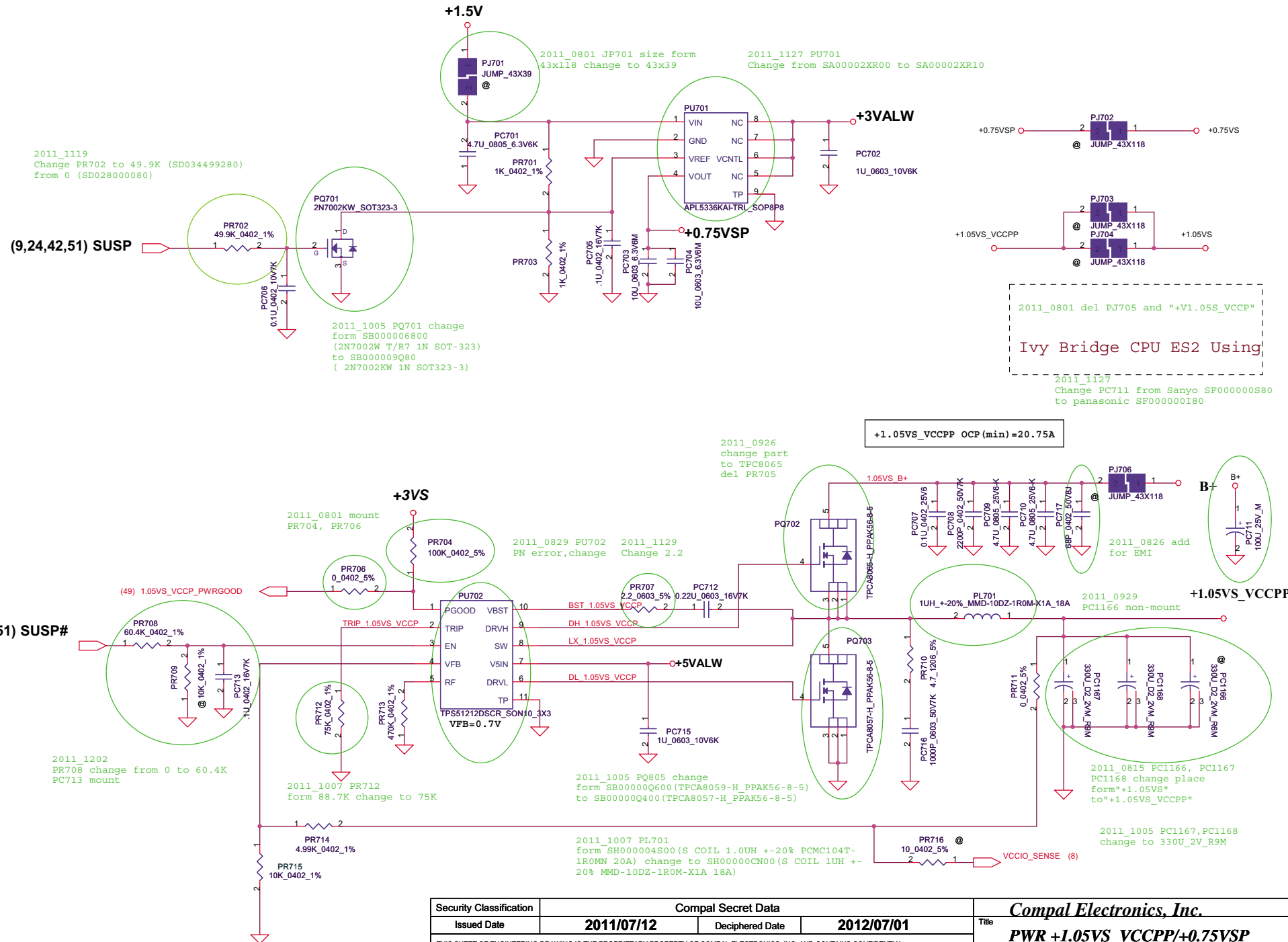
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	CHARGER
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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO





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				Date:	Friday, January 13, 2012	Sheet 48 of 56



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PWR +1.05VS_VCCPP/+0.75VSP
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				Rev	0.4

2011_1119
Change PC901,PC905 to 0.033u (SE076333K80)
from 0.033u (SE076333KN0)

2011_0829
PC909
change pa

Figure 1: Example of a BOM structure. The diagram shows a circuit schematic with components PR908, PC906, and CS9FEA. PR908 is highlighted with a red box. Below the schematic, the BOM structure is listed: 1K, 0402, 1%, <BOM Structure>, 2P: 1.65K, 1P: 1K.

PUT COLSE
TO V_GT
HOT SPOT

Option for
1 phase GFX

+5VS

PR929
0_0402_5%

CSP2A

N

2Phase: @
1Phase: install

Option for
2 phase CPU

+5VS

PR935
0_0402_5%

CSP3

N

3Phase: @
2Phase: install

PUT COLSE
TO VCORE
HOT SPOT

(9) VCC_AXG_SENSE

(9) VSS_AXG_SENSE

+1.05VS

```
2011_0819 +V1.05VS_VCCP
change to +1.05VS
```

(8) VR_SVID_DAT
(8) VR_SVID_ALRT#
(8) VR_SVID_CLK

```
2011_1005
for Intel add PC836 SE00000D180 (43P_04
```

2011_1119
Change PC936 to 47P (SE071470J80)
form 43P (SE00000D180)

TRBST#

CSCO

3P: 22p
2P: 10p

1

PR942

3P: 6.04K
2P: 4.32K

3P: 220

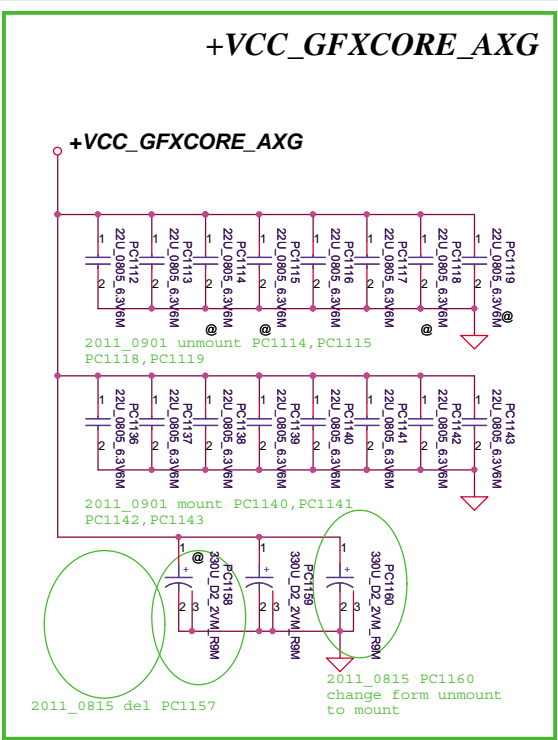
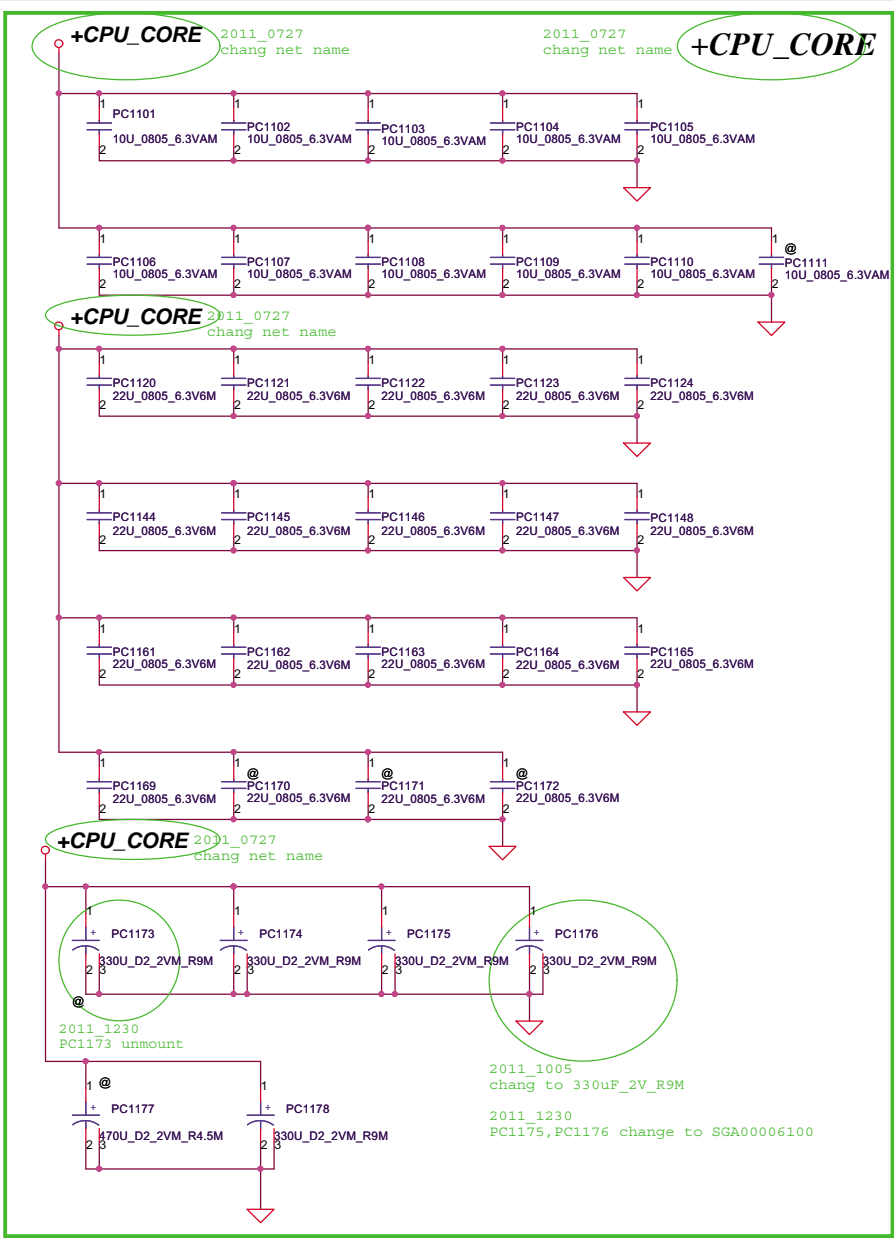
2P: 330

3P: 23.

2P: 24.

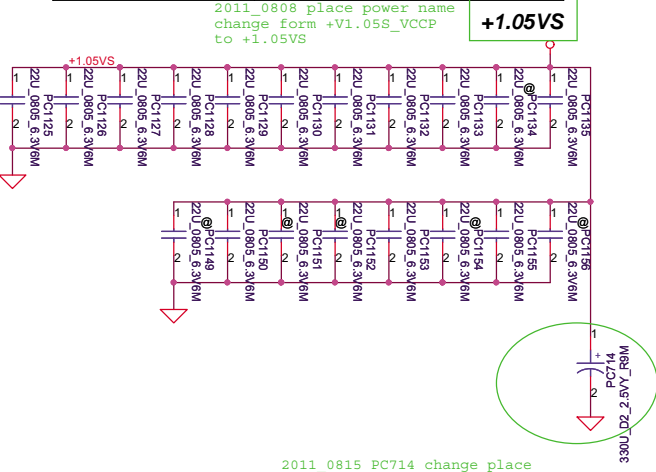


Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR-CPU_CORE1		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PWR-CPU_CORE1	
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Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

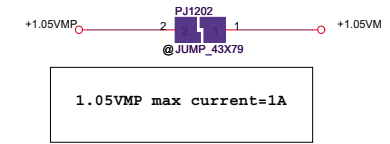
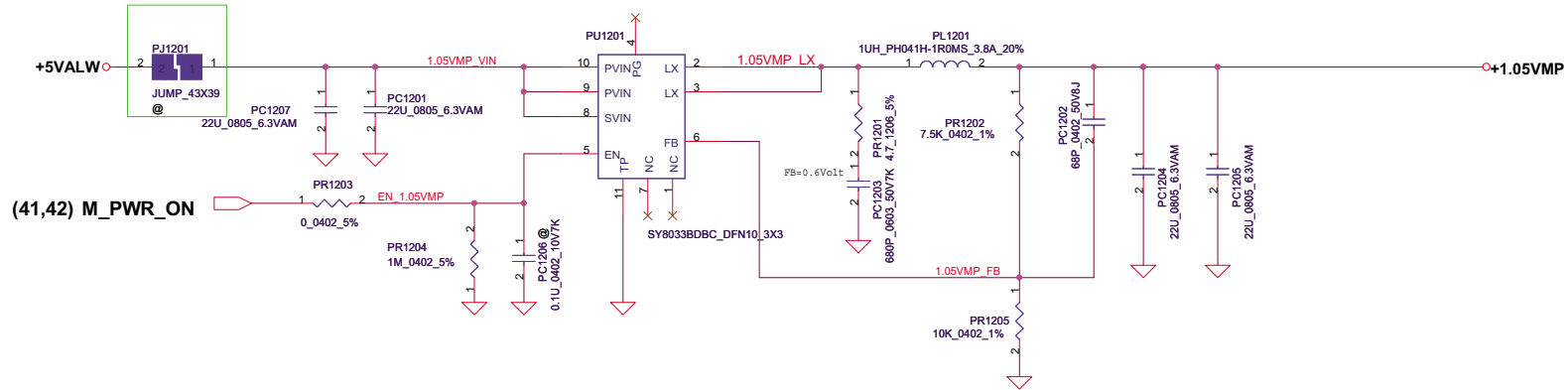


2011_0815 PC714 change place form "+1.05VS_VCCPP" to "+1.05VS"

2011_1005 PC714 change to 330uF_2V_R9M

2011_1007 PC714 form SGA00001Q802 (S POLY C 330U 2V M X LESR6M SX H1.9) change to SGA00002680 (330U_D2_2.5VY_R9M)

2011_0923 JUMP form 43X79 change to 43X79



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5		4		3		2		1	
D									
C									
B									
A									

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function																																										
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power																																										
	2011/09/15	No2		V		Del Q2305	Del SYSYON#																																										
	2011/09/15	No3		V		Add EC pin 119(M_PWR_ON) for SBA function	Add SBA function																																										
	2011/09/15	No4		V		Add EC pin 120(PCH_SLP#) from PCH to EC for SBA function	Add SBA function																																										
	2011/09/15	No5		V		Add EC pin72 (Muxless_STAT) for GPU STAT	Add Muxless_STAT function																																										
	2011/09/15	No6		V		Del PR310, PR311, PR312, PR313, net name:"H_PROCHOT#", +3VALW.	PWR-CHARGER-BQ24727																																										
	2011/09/15	No7	V			mount PC832																																											
	2011/09/15	No8		V	V	Add R2482,Q2404,C2509,R2481,R2485,Q2400,R2483,C2501	AOAC Function																																										
	2011/09/15	No9		V	V	change net name BT_OFF# to BT_ON# and change PCH EN GPIO from GPIO34 to GPIO36 R280 from @ to mount,R282 from mount to @	BT Function																																										
	2011/09/15	No10		V	V	change net name(Mini-Express) from BT_OFF# to WLBT_OFF# PCH EN GPIO change to GPIO34	BT Function																																										
	2011/09/19	No11		V	V	change +3VS_WLAN net name to +3VS_AOAC change +3VS_WWAN net name to +3VS_AOAC	AOAC Function																																										
	2011/09/19	No12		V	V	Del R1010 for LVDS CONN plug high voltage	LVDS CONN																																										
	2011/09/19	No13		V	V	R1102,R1104,R1105 from @ to mount fix MIC(ECR97236)issue	MIC function																																										
	2011/09/19	No14		V	V	Add R2470 for 80 port function	80 port function																																										
	2011/09/19	No15		V	V	Del R2476 Add Q2405	BT Function																																										
	2011/09/20	No16		V	V	Add power schematic 9/15 again modify RF PC423, PC425, PC519, PC620, PC717, PC873, PC874, PC424, PC518 PC1017, PC1018, PC1019, PC422, PC516, PC517 modify POWER在VGA的PWM IC 加加的零件PR869, PR870																																											
	2011/09/22	No17		V	V	Add U10,C589,C645 for TPM function	TPM function																																										
	2011/09/22	No18		V	V	Add R110,R112 for SPI POWER choose(SBA function)																																											
	2011/09/23	No19		V	V	modify power page 44-57(PJ1201 JUMP form 43X79 change to 43X79)																																											
	2011/09/26	No20		V	V	change CPU footprint from TYCO 2013620-2 989P-T to TYCO 2013620-2 989P-T-A39 change PCH footprint from PANTHER-POINT_FCBGA_989P-T to PANTHER-POINT_FCBGA_989P-T-A39 change GPU footprint N13P-PES-A1_FCBGA_908P to N13P-PES-A1_FCBGA_908P-A39 change VRAM footprint K4W1G1646E-HC12_FBGA_96P to K4W1G1646E-HC12_FBGA_96P-A39																																											
	2011/09/26	No21		V	V	change PCH_GPIO24(R288) pull up to +3V_PCH																																											
	2011/09/26	No22		V		change P18 (R311,R330,R286,R329) for UMA and Optimus memon																																											
	2011/09/26	No23		V		change net name PCH_THRMTRIP#_R to VGA_THRMTRIP#																																											
	2011/09/26	No24		V	V	PQ702 change to TPC8065,Del PR705 PQ1001,PQ1002,PQ1005 change to TOC8065,Del PR1001,PR1002,PR1007																																											
	2011/09/26	No25		V	V	p43 change Q2304 dual channel 2n7002 to single channel Q2304,Q2305(Q2305 @) p43 change Q2306 dual channel 2n7002 to single channel Q2306,Q2311(Q2311 @)																																											
	2011/09/27	No27	V			modify EC Board ID R2213 to 18K																																											
	2011/09/27	No28		V	V	net name CX_GPIO0 connect to U1101 pin 38																																											
	2011/09/27	No29		V	V	Add C2152,C2153,D2113 for ESD																																											
	2011/09/27	No30		V	V	change NVIDIA N13M_ROM_SCLK from 15K PU to 5K PU																																											
	2011/09/27	No31		V	V	change ESD part D2401,D2403,D2405 power from +5VALW to +USB VCCA																																											
	2011/09/27	No32		V	V	Add C2108 for GPU_CLKREQA																																											
	2011/09/27	No33				Add Q2406 , modify R2401,Change PCH_GPIO19 to ODD_DET#,for zero power ODD																																											
	2011/09/27	No34				change WLBT_OFF# to PCH_GPIO34																																											
	2011/09/27	No35				change PCH_GPIO34 to WLBT_OFF#(mini card pin5)																																											
	2011/09/27	No36				change BT_ON# connect to WLBT_OFF#(mini card pin51)																																											
	2011/09/28	No37				C76 , R1123 , c1131 , R2201,C2209 C84,C85 from @ to mount for RF team																																											
	2011/09/29	No38				R1529 change to 15K																																											
	2011/09/29	No39				Add CONN JDB3 fo debug																																											
	2011/09/29	No40				Add R2460,R2438,R2471,R2472,R2475,R2476 for PS8520B																																											
	2011/09/29	No41				change D2403 ,D2401 power to +USB_VCCB,and del D2403 ,D2401,D2405 Pin3 net																																											
	2011/09/29	No42				change power schematic del PC606 (22U_0805_6.3V6M) PR855.1 net change form +VGA_CORE to +VGA_COREP PR827 mount change to @(non-mount) PR839 for 47Kohm change to 147Kohm PR103 for 0ohm change to 270ohm PC1166 non-mount,PC1173 non-mount,PC1158 non-mount																																											
	2011/09/29	No43																																															
	2011/09/29	No44				Add Q2313,C2305,C2306,C2307,C2308,R2318,R2320,R2320,C2322 for +3V_PCH change CRT CONN to DC061109231(footprint pin modify) Add PR954,PR955																																											
	2011/09/29	No45				Add H16,H27 change Q2304,Q2305 to Q2304 modify PTH H11,H18 ,H21 Del T10 for SUS_STAT(SLP_S3# 走不出来)																																											
	2011/10/04	No46				reserve R352,R353 for SATA re-drive PS-8131B change net name from WLBT_OFF to WLBT_OFF_5# modify PCH_GPIO34 connect to BT_ON# for BT module modify PCH_GPIO36 from BT_ON# connect to WLBT_OFF_51# for mini card BT combo module changr Q2301 to 2N7002																																											
	2011/10/05	No47				Del R2469,T49,T45,T41,T37,T36,T28,T26 for ME 限高0 changer power net +3VS_FP to +3VS update power schematics P44-P57																																											
	2011/10/06	No48				change Q1202 part to SB000007H10. change JCARD1_PN to SP02000H810 footprint: ACES_87213-1400G_14P change some CONN part NO. for ME CONN list Add D2416																																											
							<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2011/07/12</td><td>Deciphered Date</td><td>2012/07/01</td><td>Title</td><td></td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size</td><td>Rev</td></tr><tr><td colspan="4"></td><td>Document Number</td><td>1.0</td></tr><tr><td colspan="4"></td><td>Custom</td><td></td></tr><tr><td colspan="4"></td><td>Date</td><td>Friday, January 13, 2012</td></tr><tr><td colspan="4"></td><td>Sheet</td><td>58 of 58</td></tr></table>	Security Classification	Compal Secret Data			Compal Electronics, Inc.		Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev					Document Number	1.0					Custom						Date	Friday, January 13, 2012					Sheet	58 of 58
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