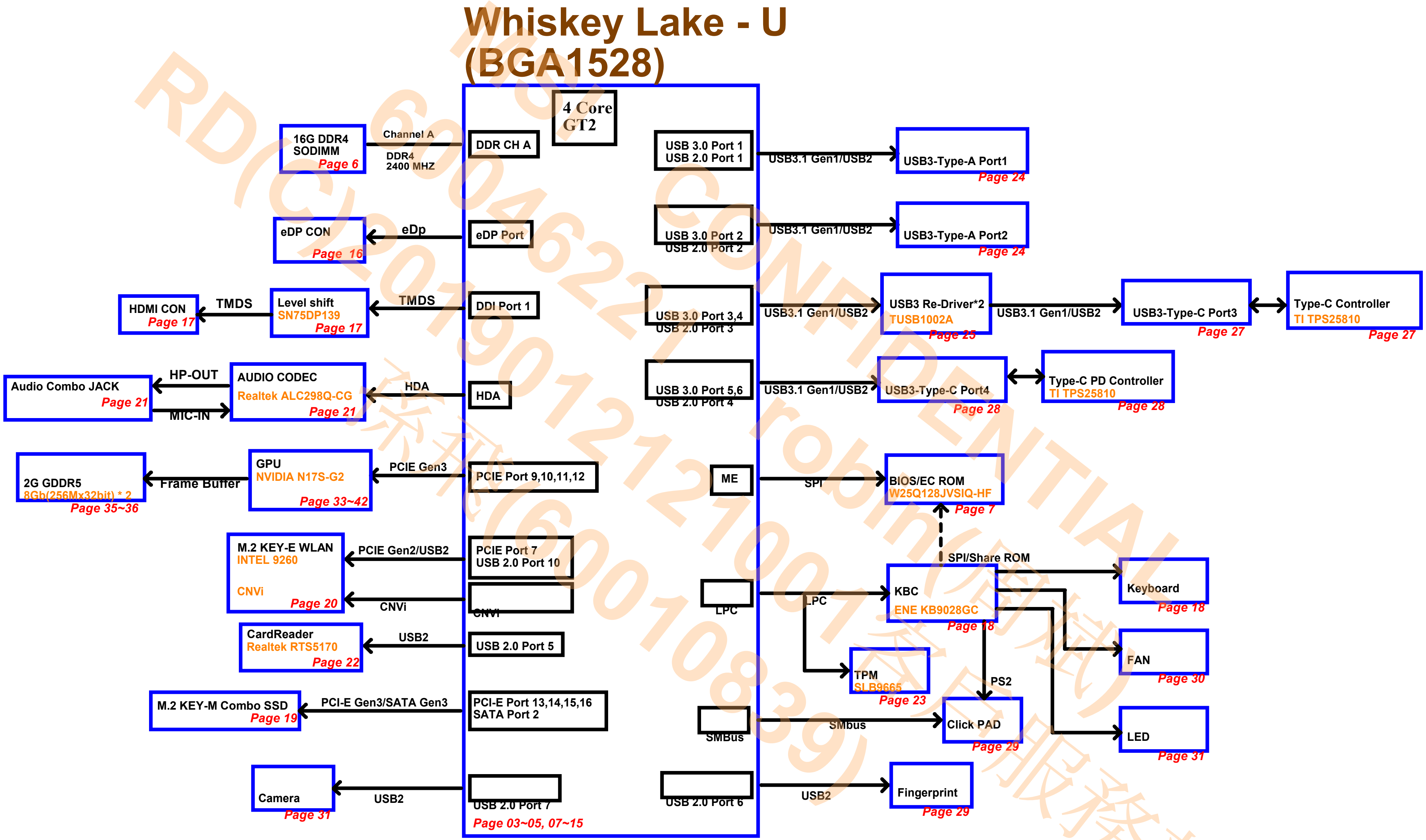
WhiskeyLake - U Processor Platform

VER : A **MS-14B3**



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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER STATES

Voltage	Description	Control Signal	SLP_S5#	SLP_S4#	SLP_S3#
PWR_SRC	AC ADAPTER OR BATTERY IN		H	H	H
+5VALW	5.0V always on power rail	PWR_SRC	L	L	L
+3VALW	3.3V always on power rail	PWR_SRC	L	L	L
+5VSUS	5.0V power rail	SUS_ON	L	L	L
+3VSUS	3.3V power rail	SUS_ON	L	L	L
+1_8VSUS	1.8V power rail	3V5VSUSPWRGD	L	L	L
+1_05VSUS	1.05V power rail	1_8VSUSPWRGD	L	L	L
+2_5VMEM_VPP	2.5V power rail DDR (off in S4-S5)	DIMM_ON_VPP	H	L	L
+VCCST	1.05V power rail CPU (off in S4-S5)	DIMM_ON_VPP	H	L	L
+VCCPLL	1.05V power rail CPU (off in S4-S5)	+VCCST	H	L	L
+1_2VDIMM	1.2V power rail DDR (off in S4-S5)	DIMM_ON_VDDQ	H	L	L
+VDDQC	1.2V power rail CPU DRAM (off in S4-S5)	+1_2VDIMM	H	L	L
+VCCPLL_OC	1.2V power rail CPU (off in S4-S5)	+1_2VDIMM	H	L	L
+5VRUN	5.0V switched power rail (off in S3-S5)	RUND	H	H	L
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUND	H	H	L
+1_8VRUN	1.8V power rail AUDIO (off in S3-S5)	RUND	H	H	L
+VCC_IO	1.05V rail for Processor & PCH (off in S3-S5)	RUND	H	H	L
+VCCSTG	1.05V power rail CPU (off in S3-S5)	+VCC_IO	H	H	L
+0_6VTT_RUN	0.6V DDR Termination voltage (off in S3-S5)	DDR_VTT_CTRL	H	H	L
+VCC_SA	0.55V to 1.15V Voltage for Processor	VR_ON	H	H	L
+VCC_CORE	0.55V to 1.5V Voltage for Processor	VR_ON	H	H	L
+VCC_GT	0.55V to 1.52V Core Voltage for Processor	VR_ON	H	H	L

Note: WHEN AC MODE, System turn on then +*VSUS will always keep high

S4(Suspend to Disk)
S3(Suspend to RAM)
S0(Full ON)

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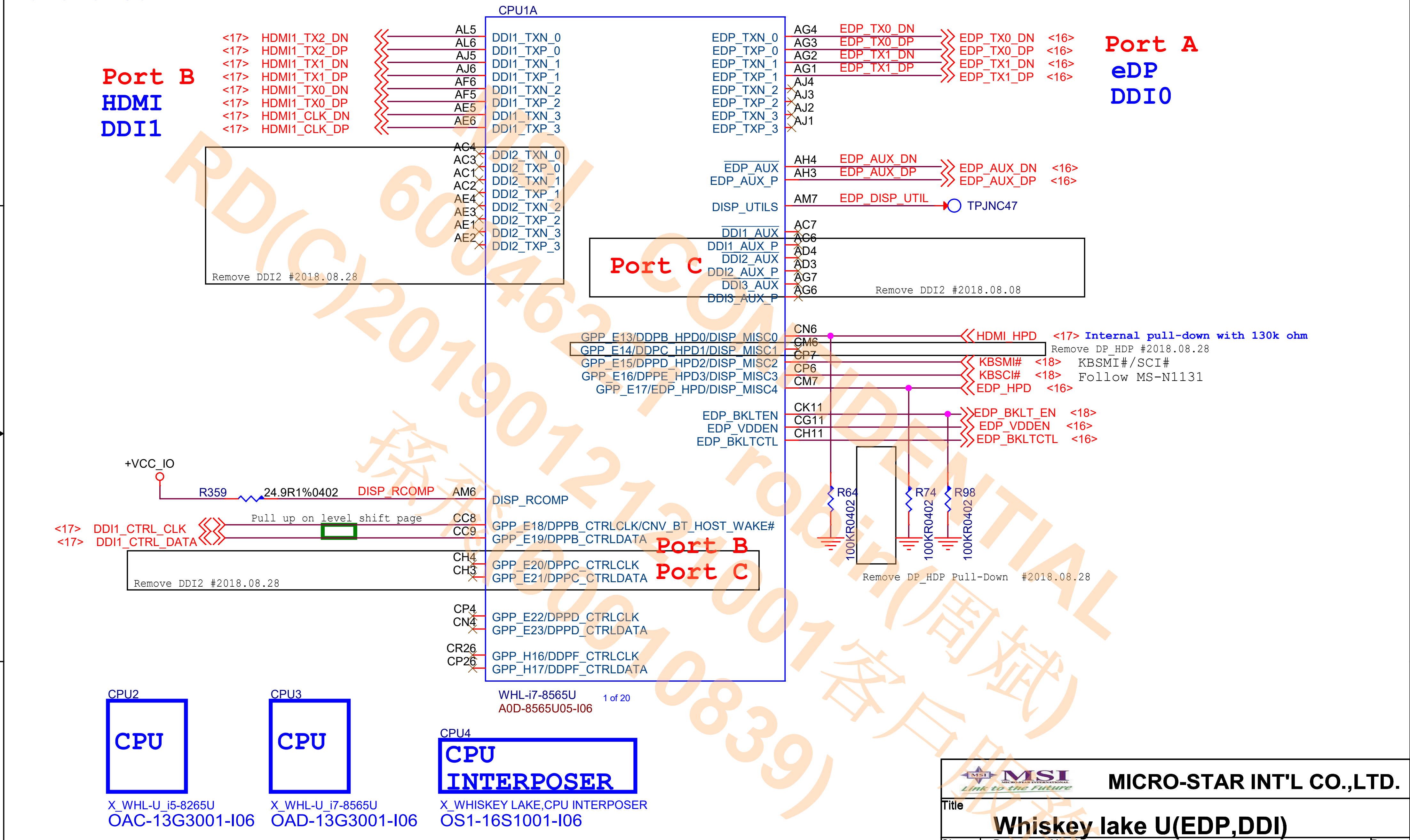
Reference 16S1



CPU1A
Port B
HDMI
DDI1
<17> HDMI1_TX2_DN
<17> HDMI1_TX2_DP
<17> HDMI1_TX1_DN
<17> HDMI1_TX1_DP
<17> HDMI1_TX0_DN
<17> HDMI1_TX0_DP
<17> HDMI1_CLK_DN
<17> HDMI1_CLK_DP
AL5 DDI1_TXN_0
AL6 DDI1_TXP_0
AJ5 DDI1_TXN_1
AJ6 DDI1_TXP_1
AF6 DDI1_TXN_2
AF5 DDI1_TXP_2
AE5 DDI1_TXN_3
AE6 DDI1_TXP_3
AC4 DDI2_TXN_0
AC3 DDI2_TXP_0
AC1 DDI2_TXN_1
AC2 DDI2_TXP_1
AE4 DDI2_TXN_2
AE3 DDI2_TXP_2
AE1 DDI2_TXN_3
AE2 DDI2_TXP_3
Remove DDI2 #2018.08.28
EDP_TXN_0 AG4 EDP_TX0_DN
EDP_TXP_0 AG3 EDP_TX0_DP
EDP_TXN_1 AG2 EDP_TX1_DN
EDP_TXP_1 AG1 EDP_TX1_DP
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1
EDP_TX0_DN <16>
EDP_TX0_DP <16>
EDP_TX1_DN <16>
EDP_TX1_DP <16>
Port A
eDP
DDI0
EDP_AUX AH4 EDP_AUX_DN
EDP_AUX_P AH3 EDP_AUX_DP
EDP_AUX_DN <16>
EDP_AUX_DP <16>
DISP_UTILS AM7 EDP_DISP_UTIL
TPJNC47
DDI1_AUX AC7
DDI1_AUX_P AC6
DDI2_AUX AD4
DDI2_AUX_P AD3
DDI3_AUX AG7
DDI3_AUX_P AG6
Port C
Remove DDI2 #2018.08.08
GPP_E13/DDPB_HPD0/DISP_MISC0 CN6
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7
HDMI_HPD <17> Internal pull-down with 130k ohm
Remove DP_HDP #2018.08.28
KBSMI# <18>
KBSCI# <18>
KBSMI#/SCI#
Follow MS-N1131
EDP_HPD <16>
EDP_BKLTEN CK11
EDP_VDDEN CG11
EDP_BKLTCTL CH11
EDP_BKLT_EN <18>
EDP_VDDEN <16>
EDP_BKLTCTL <16>
R64 100KR0402
R74 100KR0402
R98 100KR0402
Remove DP_HDP Pull-Down #2018.08.28
+VCC_IO
R359 24.9R1%0402
DISP_RCOMP AM6 DISP_RCOMP
Pull up on level shift page
<17> DDI1_CTRL_CLK
<17> DDI1_CTRL_DATA
CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
CC9 GPP_E19/DPPB_CTRLDATA
Port B
CH4 GPP_E20/DPPC_CTRLCLK
CH3 GPP_E21/DPPC_CTRLDATA
Port C
Remove DDI2 #2018.08.28
CP4 GPP_E22/DPPD_CTRLCLK
CN4 GPP_E23/DPPD_CTRLDATA
CR26 GPP_H16/DDPF_CTRLCLK
CP26 GPP_H17/DDPF_CTRLDATA
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CPU
X_WHL-U_i5-8265U
OAC-13G3001-I06
CPU3
CPU
X_WHL-U_i7-8565U
OAD-13G3001-I06
CPU4
CPU
INTERPOSER
X_WHISKEY LAKE,CPU INTERPOSER
OS1-16S1001-I06

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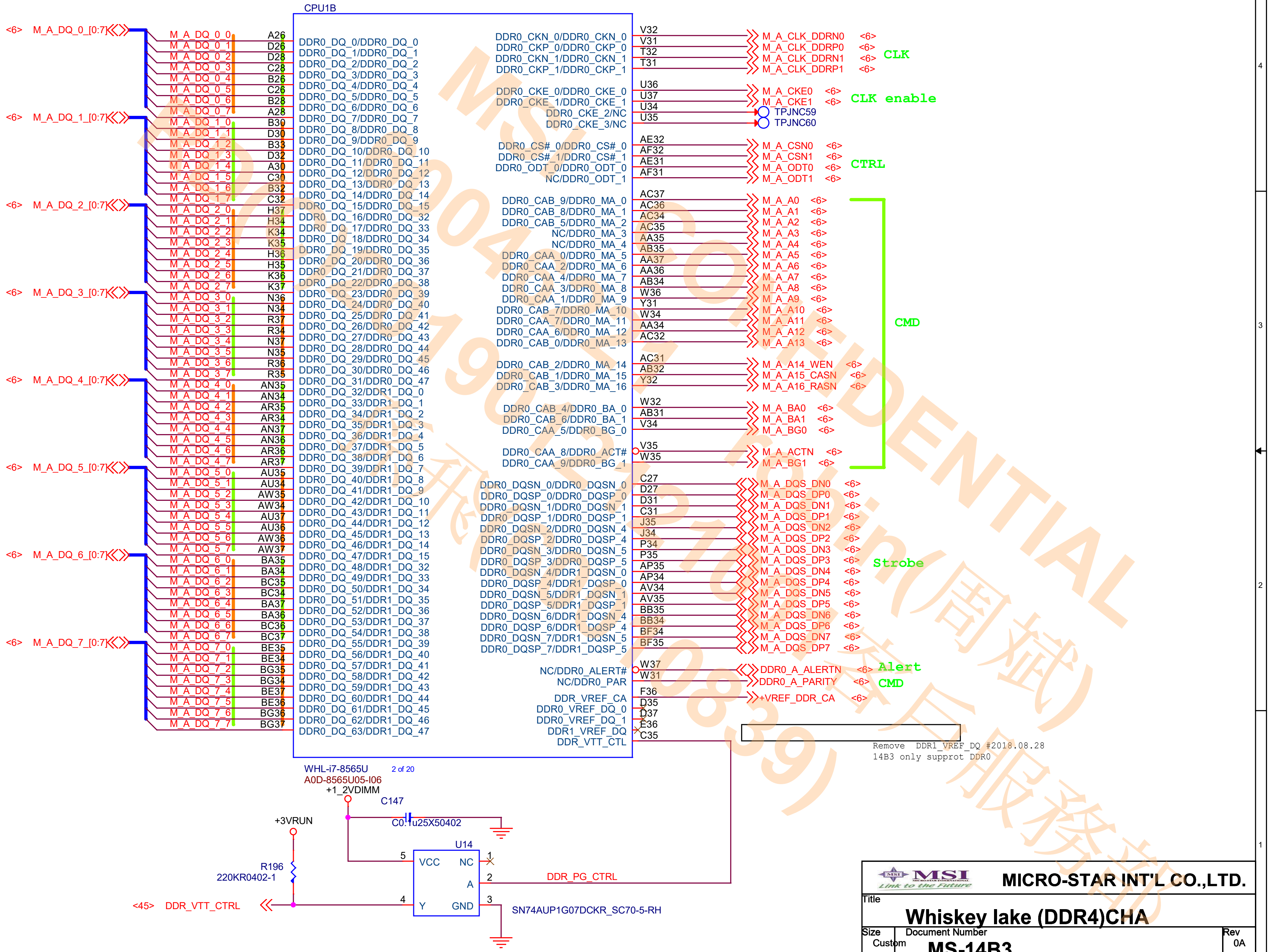
CPU1B
<6> M_A_DQ_0_[0:7]
M_A_DQ_0_0 A26 DDR0_DQ_0/DDR0_DQ_0
M_A_DQ_0_1 D26 DDR0_DQ_1/DDR0_DQ_1
M_A_DQ_0_2 D28 DDR0_DQ_2/DDR0_DQ_2
M_A_DQ_0_3 C28 DDR0_DQ_3/DDR0_DQ_3
M_A_DQ_0_4 B26 DDR0_DQ_4/DDR0_DQ_4
M_A_DQ_0_5 C26 DDR0_DQ_5/DDR0_DQ_5
M_A_DQ_0_6 B28 DDR0_DQ_6/DDR0_DQ_6
M_A_DQ_0_7 A28 DDR0_DQ_7/DDR0_DQ_7
<6> M_A_DQ_1_[0:7]
M_A_DQ_1_0 B30 DDR0_DQ_8/DDR0_DQ_8
M_A_DQ_1_1 D30 DDR0_DQ_9/DDR0_DQ_9
M_A_DQ_1_2 B33 DDR0_DQ_10/DDR0_DQ_10
M_A_DQ_1_3 D32 DDR0_DQ_11/DDR0_DQ_11
M_A_DQ_1_4 A30 DDR0_DQ_12/DDR0_DQ_12
M_A_DQ_1_5 C30 DDR0_DQ_13/DDR0_DQ_13
M_A_DQ_1_6 B32 DDR0_DQ_14/DDR0_DQ_14
M_A_DQ_1_7 C32 DDR0_DQ_15/DDR0_DQ_15
<6> M_A_DQ_2_[0:7]
M_A_DQ_2_0 H37 DDR0_DQ_16/DDR0_DQ_32
M_A_DQ_2_1 H34 DDR0_DQ_17/DDR0_DQ_33
M_A_DQ_2_2 K34 DDR0_DQ_18/DDR0_DQ_34
M_A_DQ_2_3 K35 DDR0_DQ_19/DDR0_DQ_35
M_A_DQ_2_4 H36 DDR0_DQ_20/DDR0_DQ_36
M_A_DQ_2_5 H35 DDR0_DQ_21/DDR0_DQ_37
M_A_DQ_2_6 K36 DDR0_DQ_22/DDR0_DQ_38
M_A_DQ_2_7 K37 DDR0_DQ_23/DDR0_DQ_39
<6> M_A_DQ_3_[0:7]
M_A_DQ_3_0 N36 DDR0_DQ_24/DDR0_DQ_40
M_A_DQ_3_1 N34 DDR0_DQ_25/DDR0_DQ_41
M_A_DQ_3_2 R37 DDR0_DQ_26/DDR0_DQ_42
M_A_DQ_3_3 R34 DDR0_DQ_27/DDR0_DQ_43
M_A_DQ_3_4 N37 DDR0_DQ_28/DDR0_DQ_44
M_A_DQ_3_5 N35 DDR0_DQ_29/DDR0_DQ_45
M_A_DQ_3_6 R36 DDR0_DQ_30/DDR0_DQ_46
M_A_DQ_3_7 R35 DDR0_DQ_31/DDR0_DQ_47
<6> M_A_DQ_4_[0:7]
M_A_DQ_4_0 AN35 DDR0_DQ_32/DDR1_DQ_0
M_A_DQ_4_1 AN34 DDR0_DQ_33/DDR1_DQ_1
M_A_DQ_4_2 AR35 DDR0_DQ_34/DDR1_DQ_2
M_A_DQ_4_3 AR34 DDR0_DQ_35/DDR1_DQ_3
M_A_DQ_4_4 AN37 DDR0_DQ_36/DDR1_DQ_4
M_A_DQ_4_5 AN36 DDR0_DQ_37/DDR1_DQ_5
M_A_DQ_4_6 AR36 DDR0_DQ_38/DDR1_DQ_6
M_A_DQ_4_7 AR37 DDR0_DQ_39/DDR1_DQ_7
<6> M_A_DQ_5_[0:7]
M_A_DQ_5_0 AU35 DDR0_DQ_40/DDR1_DQ_8
M_A_DQ_5_1 AU34 DDR0_DQ_41/DDR1_DQ_9
M_A_DQ_5_2 AW35 DDR0_DQ_42/DDR1_DQ_10
M_A_DQ_5_3 AW34 DDR0_DQ_43/DDR1_DQ_11
M_A_DQ_5_4 AU37 DDR0_DQ_44/DDR1_DQ_12
M_A_DQ_5_5 AU36 DDR0_DQ_45/DDR1_DQ_13
M_A_DQ_5_6 AW36 DDR0_DQ_46/DDR1_DQ_14
M_A_DQ_5_7 AW37 DDR0_DQ_47/DDR1_DQ_15
<6> M_A_DQ_6_[0:7]
M_A_DQ_6_0 BA35 DDR0_DQ_48/DDR1_DQ_32
M_A_DQ_6_1 BA34 DDR0_DQ_49/DDR1_DQ_33
M_A_DQ_6_2 BC35 DDR0_DQ_50/DDR1_DQ_34
M_A_DQ_6_3 BC34 DDR0_DQ_51/DDR1_DQ_35
M_A_DQ_6_4 BA37 DDR0_DQ_52/DDR1_DQ_36
M_A_DQ_6_5 BA36 DDR0_DQ_53/DDR1_DQ_37
M_A_DQ_6_6 BC36 DDR0_DQ_54/DDR1_DQ_38
M_A_DQ_6_7 BC37 DDR0_DQ_55/DDR1_DQ_39
<6> M_A_DQ_7_[0:7]
M_A_DQ_7_0 BE35 DDR0_DQ_56/DDR1_DQ_40
M_A_DQ_7_1 BE34 DDR0_DQ_57/DDR1_DQ_41
M_A_DQ_7_2 BG35 DDR0_DQ_58/DDR1_DQ_42
M_A_DQ_7_3 BG34 DDR0_DQ_59/DDR1_DQ_43
M_A_DQ_7_4 BE37 DDR0_DQ_60/DDR1_DQ_44
M_A_DQ_7_5 BE36 DDR0_DQ_61/DDR1_DQ_45
M_A_DQ_7_6 BG36 DDR0_DQ_62/DDR1_DQ_46
M_A_DQ_7_7 BG37 DDR0_DQ_63/DDR1_DQ_47
DDR0_CKN_0/DDR0_CKN_0 V32 M_A_CLK_DDRN0 <6>
DDR0_CKP_0/DDR0_CKP_0 V31 M_A_CLK_DDRP0 <6>
DDR0_CKN_1/DDR0_CKN_1 T32 M_A_CLK_DDRN1 <6>
DDR0_CKP_1/DDR0_CKP_1 T31 M_A_CLK_DDRP1 <6>
CLK
DDR0_CKE_0/DDR0_CKE_0 U36 M_A_CKE0 <6>
DDR0_CKE_1/DDR0_CKE_1 U37 M_A_CKE1 <6>
DDR0_CKE_2/NC U34 TPJNC59
DDR0_CKE_3/NC U35 TPJNC60
CLK enable
DDR0_CS#_0/DDR0_CS#_0 AE32 M_A_CSN0 <6>
DDR0_CS#_1/DDR0_CS#_1 AF32 M_A_CSN1 <6>
DDR0_ODT_0/DDR0_ODT_0 AE31 M_A_ODT0 <6>
NC/DDR0_ODT_1 AF31 M_A_ODT1 <6>
CTRL
DDR0_CAB_9/DDR0_MA_0 AC37 M_A_A0 <6>
DDR0_CAB_8/DDR0_MA_1 AC36 M_A_A1 <6>
DDR0_CAB_5/DDR0_MA_2 AC34 M_A_A2 <6>
NC/DDR0_MA_3 AC35 M_A_A3 <6>
NC/DDR0_MA_4 AA35 M_A_A4 <6>
DDR0_CAA_0/DDR0_MA_5 AB35 M_A_A5 <6>
DDR0_CAA_2/DDR0_MA_6 AA37 M_A_A6 <6>
DDR0_CAA_4/DDR0_MA_7 AA36 M_A_A7 <6>
DDR0_CAA_3/DDR0_MA_8 AB34 M_A_A8 <6>
DDR0_CAA_1/DDR0_MA_9 W36 M_A_A9 <6>
DDR0_CAB_7/DDR0_MA_10 Y31 M_A_A10 <6>
DDR0_CAA_7/DDR0_MA_11 W34 M_A_A11 <6>
DDR0_CAA_6/DDR0_MA_12 AA34 M_A_A12 <6>
DDR0_CAB_0/DDR0_MA_13 AC32 M_A_A13 <6>
DDR0_CAB_2/DDR0_MA_14 AC31 M_A_A14_WEN <6>
DDR0_CAB_1/DDR0_MA_15 AB32 M_A_A15_CASN <6>
DDR0_CAB_3/DDR0_MA_16 Y32 M_A_A16_RASN <6>
DDR0_CAB_4/DDR0_BA_0 W32 M_A_BA0 <6>
DDR0_CAB_6/DDR0_BA_1 AB31 M_A_BA1 <6>
DDR0_CAA_5/DDR0_BG_0 V34 M_A_BG0 <6>
DDR0_CAA_8/DDR0_ACT# V35 M_A_ACTN <6>
DDR0_CAA_9/DDR0_BG_1 W35 M_A_BG1 <6>
CMD
DDR0_DQSN_0/DDR0_DQSN_0 C27 M_A_DQS_DN0 <6>
DDR0_DQSP_0/DDR0_DQSP_0 D27 M_A_DQS_DP0 <6>
DDR0_DQSN_1/DDR0_DQSN_1 D31 M_A_DQS_DN1 <6>
DDR0_DQSP_1/DDR0_DQSP_1 C31 M_A_DQS_DP1 <6>
DDR0_DQSN_2/DDR0_DQSN_4 J35 M_A_DQS_DN2 <6>
DDR0_DQSP_2/DDR0_DQSP_4 J34 M_A_DQS_DP2 <6>
DDR0_DQSN_3/DDR0_DQSN_5 P34 M_A_DQS_DN3 <6>
DDR0_DQSP_3/DDR0_DQSP_5 P35 M_A_DQS_DP3 <6>
DDR0_DQSN_4/DDR1_DQSN_0 AP35 M_A_DQS_DN4 <6>
DDR0_DQSP_4/DDR1_DQSP_0 AP34 M_A_DQS_DP4 <6>
DDR0_DQSN_5/DDR1_DQSN_1 AV34 M_A_DQS_DN5 <6>
DDR0_DQSP_5/DDR1_DQSP_1 AV35 M_A_DQS_DP5 <6>
DDR0_DQSN_6/DDR1_DQSN_4 BB35 M_A_DQS_DN6 <6>
DDR0_DQSP_6/DDR1_DQSP_4 BB34 M_A_DQS_DP6 <6>
DDR0_DQSN_7/DDR1_DQSN_5 BF34 M_A_DQS_DN7 <6>
DDR0_DQSP_7/DDR1_DQSP_5 BF35 M_A_DQS_DP7 <6>
Strobe
NC/DDR0_ALERT# W37 DDR0_A_ALERTN <6>
NC/DDR0_PAR W31 DDR0_A_PARITY <6>
Alert
CMD
DDR_VREF_CA F36 +VREF_DDR_CA <6>
DDR0_VREF_DQ_0 D35
DDR0_VREF_DQ_1 D37
DDR1_VREF_DQ E36
DDR_VTT_CTL C35
Remove DDR1_VREF_DQ #2018.08.28
14B3 only supprot DDR0
WHL-i7-8565U 2 of 20
A0D-8565U05-I06
+1_2VDIMM
C147
C0.1u25X50402
+3VRUN
R196
220KR0402-1
U14
VCC NC A Y GND
5 1 2 4 3
DDR_PG_CTRL
<45> DDR_VTT_CTRL
SN74AUP1G07DCKR_SC70-5-RH

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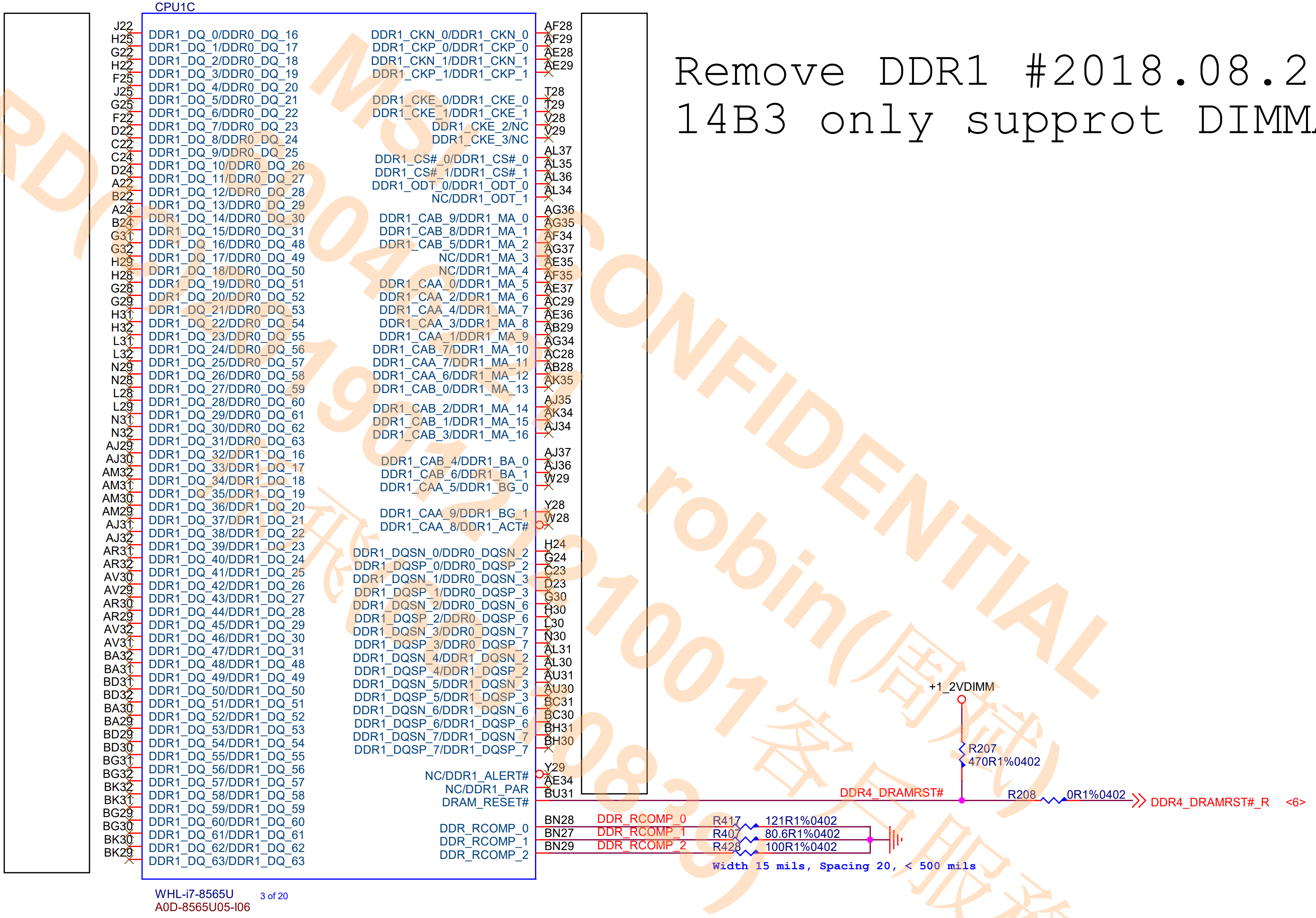
SODIMM_B



CPU1C
J22 DDR1_DQ_0/DDR0_DQ_16
H25 DDR1_DQ_1/DDR0_DQ_17
G22 DDR1_DQ_2/DDR0_DQ_18
H22 DDR1_DQ_3/DDR0_DQ_19
F25 DDR1_DQ_4/DDR0_DQ_20
J25 DDR1_DQ_5/DDR0_DQ_21
G25 DDR1_DQ_6/DDR0_DQ_22
F22 DDR1_DQ_7/DDR0_DQ_23
D22 DDR1_DQ_8/DDR0_DQ_24
C22 DDR1_DQ_9/DDR0_DQ_25
C24 DDR1_DQ_10/DDR0_DQ_26
D24 DDR1_DQ_11/DDR0_DQ_27
A22 DDR1_DQ_12/DDR0_DQ_28
B22 DDR1_DQ_13/DDR0_DQ_29
A24 DDR1_DQ_14/DDR0_DQ_30
B24 DDR1_DQ_15/DDR0_DQ_31
G31 DDR1_DQ_16/DDR0_DQ_48
G32 DDR1_DQ_17/DDR0_DQ_49
H29 DDR1_DQ_18/DDR0_DQ_50
H28 DDR1_DQ_19/DDR0_DQ_51
G28 DDR1_DQ_20/DDR0_DQ_52
G29 DDR1_DQ_21/DDR0_DQ_53
H31 DDR1_DQ_22/DDR0_DQ_54
H32 DDR1_DQ_23/DDR0_DQ_55
L31 DDR1_DQ_24/DDR0_DQ_56
L32 DDR1_DQ_25/DDR0_DQ_57
N29 DDR1_DQ_26/DDR0_DQ_58
N28 DDR1_DQ_27/DDR0_DQ_59
L28 DDR1_DQ_28/DDR0_DQ_60
L29 DDR1_DQ_29/DDR0_DQ_61
N31 DDR1_DQ_30/DDR0_DQ_62
N32 DDR1_DQ_31/DDR0_DQ_63
AJ29 DDR1_DQ_32/DDR1_DQ_16
AJ30 DDR1_DQ_33/DDR1_DQ_17
AM32 DDR1_DQ_34/DDR1_DQ_18
AM31 DDR1_DQ_35/DDR1_DQ_19
AM30 DDR1_DQ_36/DDR1_DQ_20
AM29 DDR1_DQ_37/DDR1_DQ_21
AJ31 DDR1_DQ_38/DDR1_DQ_22
AJ32 DDR1_DQ_39/DDR1_DQ_23
AR31 DDR1_DQ_40/DDR1_DQ_24
AR32 DDR1_DQ_41/DDR1_DQ_25
AV30 DDR1_DQ_42/DDR1_DQ_26
AV29 DDR1_DQ_43/DDR1_DQ_27
AR30 DDR1_DQ_44/DDR1_DQ_28
AR29 DDR1_DQ_45/DDR1_DQ_29
AV32 DDR1_DQ_46/DDR1_DQ_30
AV31 DDR1_DQ_47/DDR1_DQ_31
BA32 DDR1_DQ_48/DDR1_DQ_48
BA31 DDR1_DQ_49/DDR1_DQ_49
BD31 DDR1_DQ_50/DDR1_DQ_50
BD32 DDR1_DQ_51/DDR1_DQ_51
BA30 DDR1_DQ_52/DDR1_DQ_52
BA29 DDR1_DQ_53/DDR1_DQ_53
BD29 DDR1_DQ_54/DDR1_DQ_54
BD30 DDR1_DQ_55/DDR1_DQ_55
BG31 DDR1_DQ_56/DDR1_DQ_56
BG32 DDR1_DQ_57/DDR1_DQ_57
BK32 DDR1_DQ_58/DDR1_DQ_58
BK31 DDR1_DQ_59/DDR1_DQ_59
BG29 DDR1_DQ_60/DDR1_DQ_60
BG30 DDR1_DQ_61/DDR1_DQ_61
BK30 DDR1_DQ_62/DDR1_DQ_62
BK29 DDR1_DQ_63/DDR1_DQ_63
DDR1_CKN_0/DDR1_CKN_0 AF28
DDR1_CKP_0/DDR1_CKP_0 AF29
DDR1_CKN_1/DDR1_CKN_1 AE28
DDR1_CKP_1/DDR1_CKP_1 AE29
DDR1_CKE_0/DDR1_CKE_0 T28
DDR1_CKE_1/DDR1_CKE_1 T29
DDR1_CKE_2/NC V28
DDR1_CKE_3/NC V29
DDR1_CS#_0/DDR1_CS#_0 AL37
DDR1_CS#_1/DDR1_CS#_1 AL35
DDR1_ODT_0/DDR1_ODT_0 AL36
NC/DDR1_ODT_1 AL34
DDR1_CAB_9/DDR1_MA_0 AG36
DDR1_CAB_8/DDR1_MA_1 AG35
DDR1_CAB_5/DDR1_MA_2 AF34
NC/DDR1_MA_3 AG37
NC/DDR1_MA_4 AE35
DDR1_CAA_0/DDR1_MA_5 AF35
DDR1_CAA_2/DDR1_MA_6 AE37
DDR1_CAA_4/DDR1_MA_7 AC29
DDR1_CAA_3/DDR1_MA_8 AE36
DDR1_CAA_1/DDR1_MA_9 AB29
DDR1_CAB_7/DDR1_MA_10 AG34
DDR1_CAA_7/DDR1_MA_11 AC28
DDR1_CAA_6/DDR1_MA_12 AB28
DDR1_CAB_0/DDR1_MA_13 AK35
DDR1_CAB_2/DDR1_MA_14 AJ35
DDR1_CAB_1/DDR1_MA_15 AK34
DDR1_CAB_3/DDR1_MA_16 AJ34
DDR1_CAB_4/DDR1_BA_0 AJ37
DDR1_CAB_6/DDR1_BA_1 AJ36
DDR1_CAA_5/DDR1_BG_0 W29
DDR1_CAA_9/DDR1_BG_1 Y28
DDR1_CAA_8/DDR1_ACT# W28
DDR1_DQSN_0/DDR0_DQSN_2 H24
DDR1_DQSP_0/DDR0_DQSP_2 G24
DDR1_DQSN_1/DDR0_DQSN_3 C23
DDR1_DQSP_1/DDR0_DQSP_3 D23
DDR1_DQSN_2/DDR0_DQSN_6 G30
DDR1_DQSP_2/DDR0_DQSP_6 H30
DDR1_DQSN_3/DDR0_DQSN_7 L30
DDR1_DQSP_3/DDR0_DQSP_7 N30
DDR1_DQSN_4/DDR1_DQSN_2 AL31
DDR1_DQSP_4/DDR1_DQSP_2 AL30
DDR1_DQSN_5/DDR1_DQSN_3 AU31
DDR1_DQSP_5/DDR1_DQSP_3 AU30
DDR1_DQSN_6/DDR1_DQSN_6 BC31
DDR1_DQSP_6/DDR1_DQSP_6 BC30
DDR1_DQSN_7/DDR1_DQSN_7 BH31
DDR1_DQSP_7/DDR1_DQSP_7 BH30
NC/DDR1_ALERT# Y29
NC/DDR1_PAR AE34
DRAM_RESET# BU31
DDR_RCOMP_0 BN28
DDR_RCOMP_1 BN27
DDR_RCOMP_2 BN29
WHL-i7-8565U
3 of 20
A0D-8565U05-I06
+1_2VDIMM
R207
470R1%0402
DDR4_DRAMRST#
R208
0R1%0402
DDR4_DRAMRST#_R
<6>
DDR_RCOMP_0
DDR_RCOMP_1
DDR_RCOMP_2
R417 121R1%0402
R407 80.6R1%0402
R428 100R1%0402
Width 15 mils, Spacing 20, < 500 mils

Remove DDR1 #2018.08.28
14B3 only supprot DIMMA

MICRO-STAR INT'L CO.,LTD.

Title	Whiskey lake (DDR4)CHB	
Size: Custom	Document Number: MS-14B3	Rev: 0A
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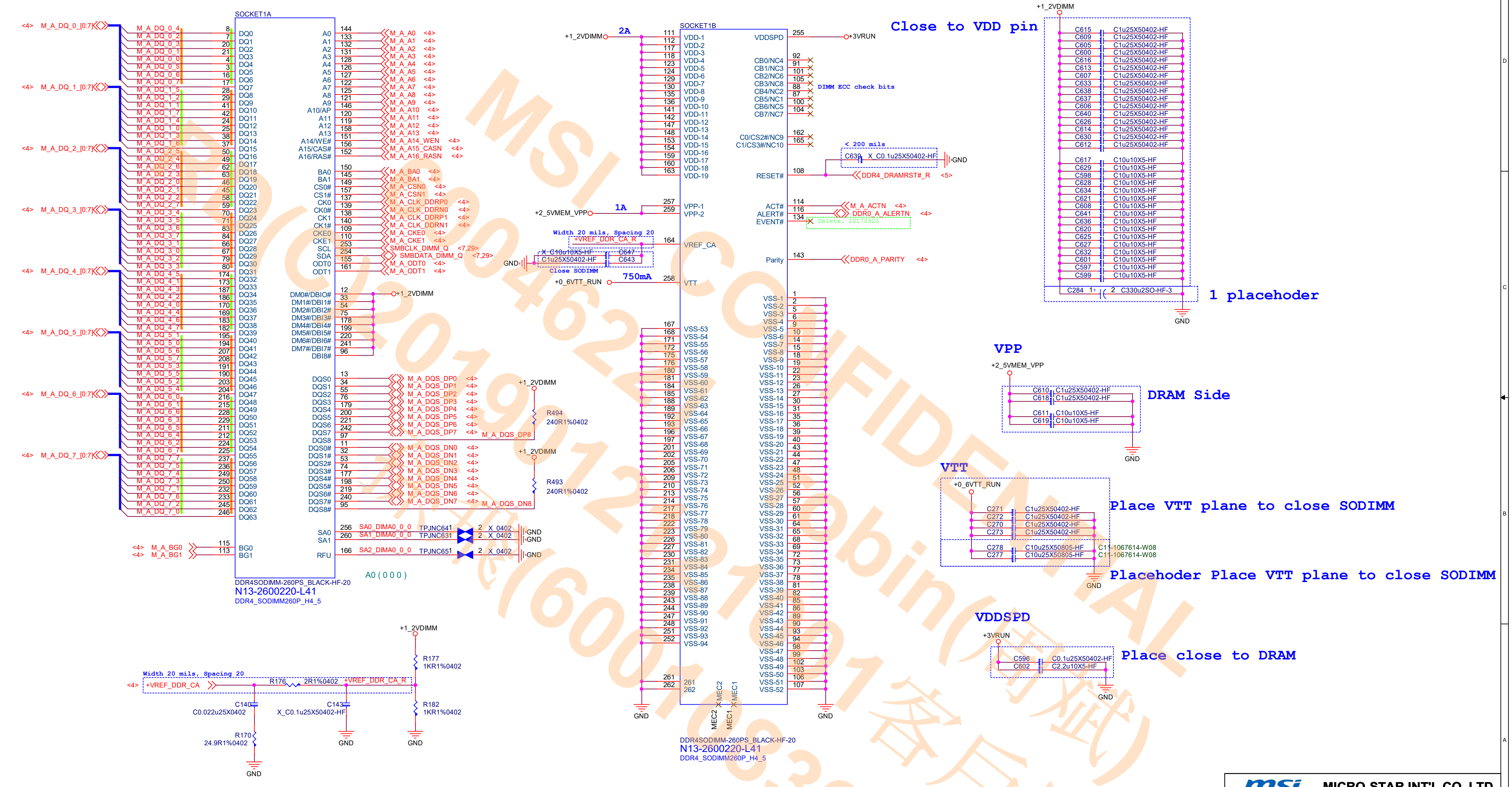
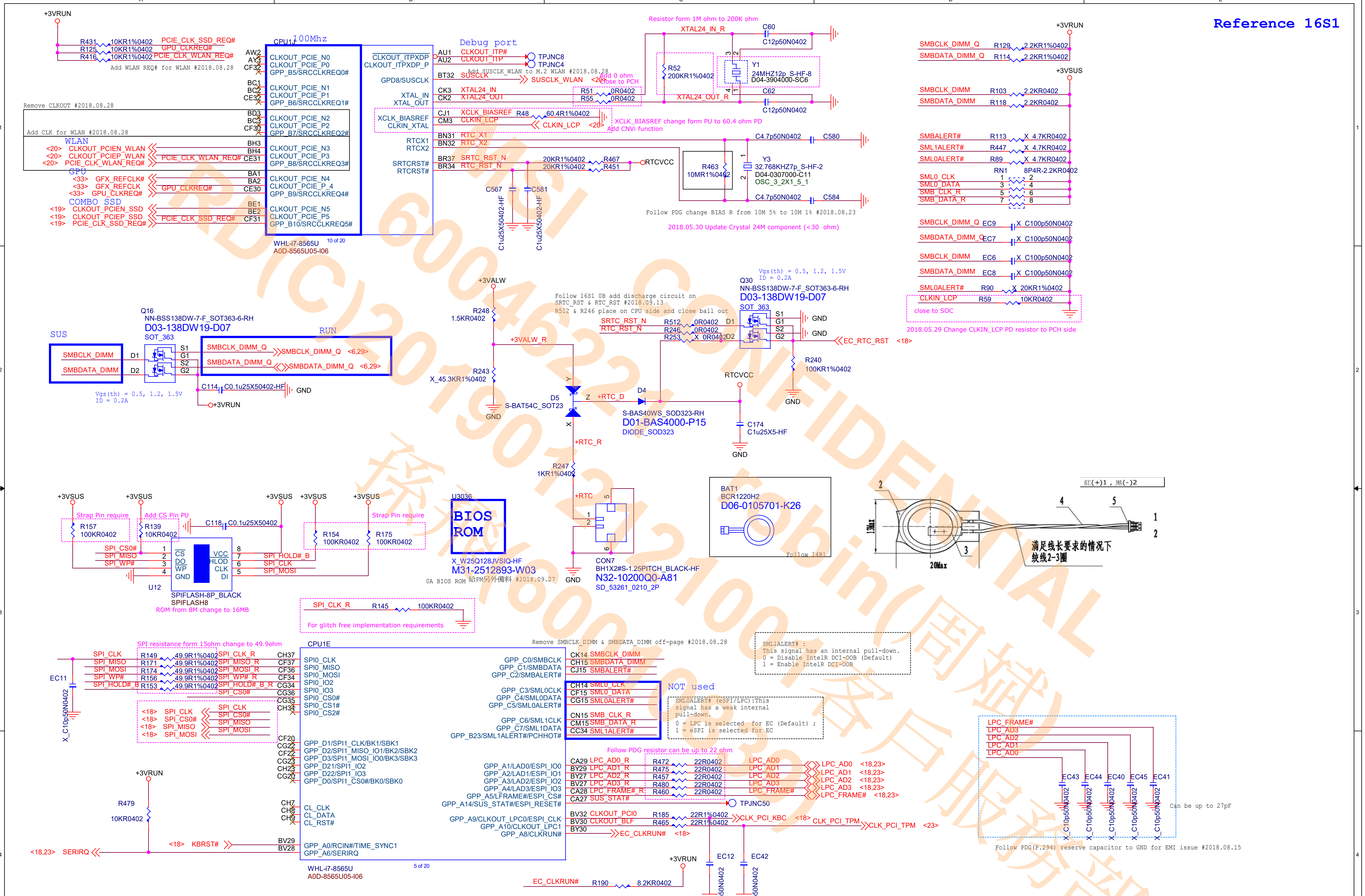
SODIMM_A DDR4 SODIMM Interleave (IL)

Follow 14B1 to change location for placement #2018.08.22



MICRO-STAR INT'L CO.,LTD.		
Title	DDR4_SODIMM_A	
Size Custom	Document Number MS-14B3	Rev 0A
Date: Monday, October 01, 2018	Sheet 6 of 57	


Reference 16S1
+3VRUN
R431 10KR1%0402 PCIE_CLK_SSD_REQ#
R125 10KR1%0402 GPU_CLKREQ#
R416 10KR1%0402 PCIE_CLK_WLAN_REQ#
Add WLAN REQ# for WLAN #2018.08.28
Remove CLKOUT #2018.08.28
Add CLK for WLAN #2018.08.28
CPU1F 100Mhz
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4
CLKOUT_PCIE_P_4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#
WLAN
<20> CLKOUT_PCIEN_WLAN
<20> CLKOUT_PCIEP_WLAN
<20> PCIE_CLK_WLAN_REQ#
GPU
<33> GFX_REFCLK#
<33> GFX_REFCLK
<33> GPU_CLKREQ#
COMBO SSD
<19> CLKOUT_PCIEN_SSD
<19> CLKOUT_PCIEP_SSD
<19> PCIE_CLK_SSD_REQ#
WHL-i7-8565U
A0D-8565U05-I06
10 of 20
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL_IN
XTAL_OUT
XCLK_BIASREF
CLKIN_XTAL
RTCX1
RTCX2
SRTCRST#
RTCRST#
Debug port
CLKOUT_ITP# TPJNC8
CLKOUT_ITP TPJNC4
Add SUSCLK_WLAN to M.2 WLAN #2018.08.28
SUSCLK SUSCLK_WLAN <20>
Add 0 ohm
Close to PCH
XTAL24_IN R51 0R0402
XTAL24_OUT R55 0R0402
XCLK_BIASREF R48 60.4R1%0402
CLKIN_LCP CLKIN_LCP <20>
XCLK_BIASREF change form PU to 60.4 ohm PD
Add CNVi function
Resistor form 1M ohm to 200K ohm
XTAL24_IN_R C60 C12p50N0402
R52 200KR1%0402
Y1 24MHZ12p_S-HF-8 D04-3904000-SC6
XTAL24_OUT_R C62 C12p50N0402
RTC_X1 C4.7p50N0402 C580
RTC_X2
R463 10MR1%0402
Y3 32.768KHZ7p_S-HF-2 D04-0307000-C11 OSC_3_2X1_5_1
C4.7p50N0402 C584
SRTC_RST_N 20KR1%0402 R467
RTC_RST_N 20KR1%0402 R451 RTCVCC
C567 C1u25X50402-HF
C581 C1u25X50402-HF
Follow PDG change BIAS R from 10M 5% to 10M 1% #2018.08.23
2018.05.30 Update Crystal 24M component (<30 ohm)
+3VRUN
SMBCLK_DIMM_Q R129 2.2KR1%0402
SMBDATA_DIMM_Q R114 2.2KR1%0402
+3VSUS
SMBCLK_DIMM R103 2.2KR0402
SMBDATA_DIMM R118 2.2KR0402
SMBALERT# R113 X_4.7KR0402
SML1ALERT# R447 X_4.7KR0402
SML0ALERT# R89 X_4.7KR0402
RN1 8P4R-2.2KR0402
SML0_CLK
SML0_DATA
SMB_CLK_R
SMB_DATA_R
SMBCLK_DIMM_Q EC9 X_C100p50N0402
SMBDATA_DIMM_Q EC7 X_C100p50N0402
SMBCLK_DIMM EC6 X_C100p50N0402
SMBDATA_DIMM EC8 X_C100p50N0402
SML0ALERT# R90 X_20KR1%0402
CLKIN_LCP R59 10KR0402
close to SOC
2018.05.29 Change CLKIN_LCP PD resistor to PCH side
SUS
SMBCLK_DIMM
SMBDATA_DIMM
Q16 NN-BSS138DW-7-F_SOT363-6-RH D03-138DW19-D07 SOT_363
RUN
SMBCLK_DIMM_Q SMBCLK_DIMM_Q <6,29>
SMBDATA_DIMM_Q SMBDATA_DIMM_Q <6,29>
C114 C0.1u25X50402-HF GND
+3VRUN
Vgs(th) = 0.5, 1.2, 1.5V
ID = 0.2A
+3VALW
R248 1.5KR0402
+3VALW_R
R243 X_45.3KR1%0402
GND
D5 S-BAT54C_SOT23
+RTC_D
D4 S-BAS40WS_SOD323-RH D01-BAS4000-P15 DIODE_SOD323
+RTC_R
R247 1KR1%0402
+RTC
Follow 16S1 0B add discharge circuit on SRTC_RST & RTC_RST #2018.09.13
R512 & R246 place on CPU side and close ball out
SRTC_RST_N R512 0R0402
RTC_RST_N R246 0R0402
R253 X_0R0402
Q30 NN-BSS138DW-7-F_SOT363-6-RH D03-138DW19-D07 SOT_363
Vgs(th) = 0.5, 1.2, 1.5V
ID = 0.2A
EC_RTC_RST <18>
R240 100KR1%0402
RTCVCC
C174 C1u25X5-HF
GND
CON7 BH1X2#S-1.25PITCH_BLACK-HF N32-10200Q0-A81 SD_53261_0210_2P
BAT1 BCR1220H2 D06-0105701-K26
Follow 14B1
紅(+)1，黑(-)2
满足线长要求的情况下 绞线2-3圈
13Max
20Max
+3VSUS
Strap Pin require
R157 100KR0402
Add CS Pin PU
R139 10KR0402
C118 C0.1u25X50402
SPI_CS0#
SPI_MISO
SPI_WP#
U12 SPIFLASH-8P_BLACK SPIFLASH8
ROM from 8M change to 16MB
SPI_HOLD#_B
SPI_CLK
SPI_MOSI
R154 100KR0402
R175 100KR0402
U3036
BIOS ROM
X_W25Q128JVSIQ-HF
M31-2512893-W03
0A BIOS ROM 給PM另外備料 #2018.09.27
SPI_CLK_R R145 100KR0402
For glitch free implementation requirements
SPI resistance form 15ohm change to 49.9ohm
SPI_CLK R149 49.9R1%0402 SPI_CLK_R
SPI_MISO R171 49.9R1%0402 SPI_MISO_R
SPI_MOSI R174 49.9R1%0402 SPI_MOSI_R
SPI_WP# R156 49.9R1%0402 SPI_WP#_R
SPI_HOLD#_B R153 49.9R1%0402 SPI_HOLD#_B_R
SPI_CS0#
EC11 X_C10p50N0402
<18> SPI_CLK
<18> SPI_CS0#
<18> SPI_MISO
<18> SPI_MOSI
CPU1E
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
GPP_D1/SPI1_CLK/BK1/SBK1
GPP_D2/SPI1_MISO_IO1/BK2/SBK2
GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS0#/BK0/SBK0
CL_CLK
CL_DATA
CL_RST#
GPP_A0/RCIN#/TIME_SYNC1
GPP_A6/SERIRQ
WHL-i7-8565U
A0D-8565U05-I06
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+3VRUN
R479 10KR0402
<18,23> SERIRQ
<18> KBRST#
Remove SMBCLK_DIMM & SMBDATA_DIMM off-page #2018.08.28
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
SMBCLK_DIMM
SMBDATA_DIMM
SMBALERT#
SML0_CLK
SML0_DATA
SML0ALERT#
SMB_CLK_R
SMB_DATA_R
SML1ALERT#
NOT used
SML1ALERT# : This signal has an internal pull-down. 0 = Disable IntelR DCI-OOB (Default) 1 = Enable IntelR DCI-OOB
SML0ALERT# (eSPI/LPC):This signal has a weak internal pull-down. 0 = LPC is selected for EC (Default) ; 1 = eSPI is selected for EC
Follow PDG resistor can be up to 22 ohm
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#
LPC_AD0_R R472 22R0402 LPC_AD0 <18,23>
LPC_AD1_R R475 22R0402 LPC_AD1 <18,23>
LPC_AD2_R R457 22R0402 LPC_AD2 <18,23>
LPC_AD3_R R480 22R0402 LPC_AD3 <18,23>
LPC_FRAME#_R R460 22R0402 LPC_FRAME# <18,23>
SUS_STAT# TPJNC50
CLKOUT_PCI0 R185 22R1%0402 CLK_PCI_KBC <18>
CLKOUT_BLF R465 22R1%0402 CLK_PCI_TPM <23>
EC_CLKRUN# <18>
+3VRUN
EC_CLKRUN# R190 8.2KR0402
EC12 X_C10p50N0402
EC42 X_C10p50N0402
LPC_FRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
EC43 EC44 EC40 EC45 EC41 X_C10p50N0402
Can be up to 27pF
Follow PDG(P.294) reserve capacitor to GND for EMI issue #2018.08.15

MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U (RTC;LPC;CLOCK)

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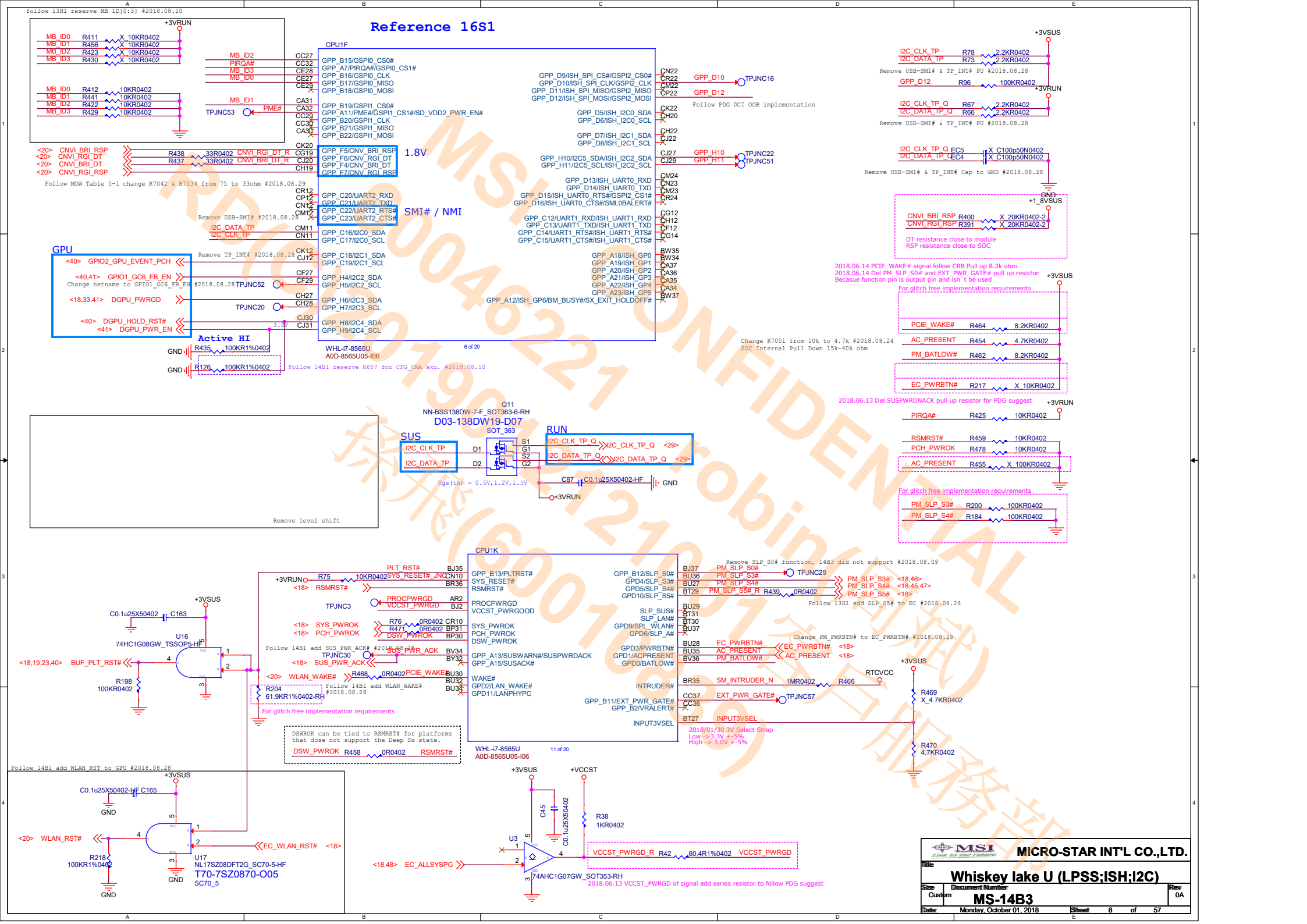
Reference 16S1
CPU1F
GPU
Active HI
SUS
RUN
Q11
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
CPU1K
WHL-i7-8565U
A0D-8565U05-I06
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1.8V
SMI# / NMI
Remove level shift
Follow 14B1 add WLAN_RST to GPU #2018.08.28
MICRO-STAR INT'L CO.,LTD.
Whiskey lake U (LPSS;ISH;I2C)
MS-14B3
Monday, October 01, 2018
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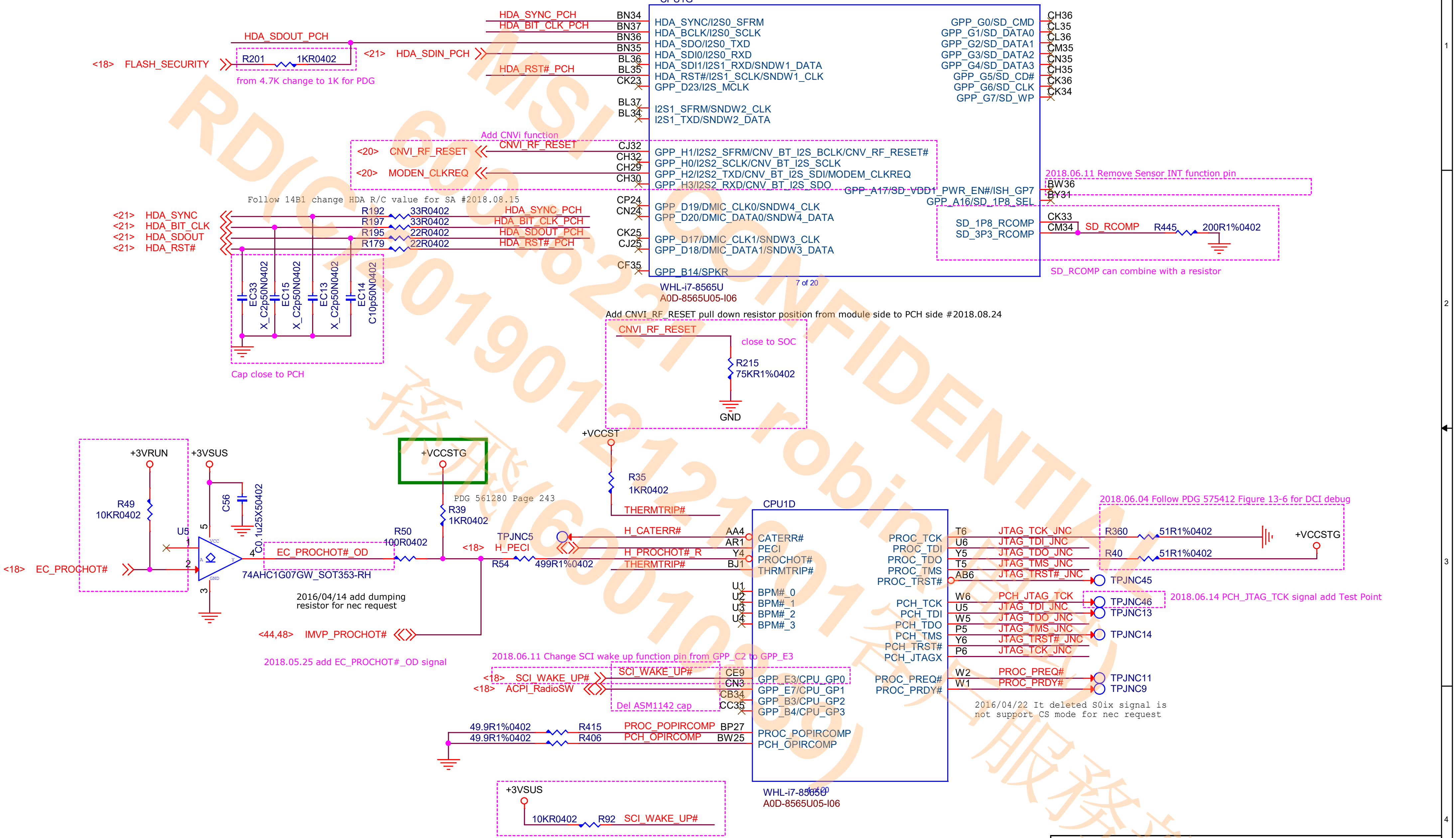
Reference 16S1

Flash Descriptor Security Override	
HDA_SDO	Low = Disable High = Enable



CPU1G
HDA_SYNC_PCH BN34 HDA_SYNC/I2S0_SFRM
HDA_BIT_CLK_PCH BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_PCH BN36 HDA_SDO/I2S0_TXD
<21> HDA_SDIN_PCH BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST#_PCH BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 GPP_D23/I2S_MCLK
BL37 I2S1_SFRM/SNDW2_CLK
BL34 I2S1_TXD/SNDW2_DATA
<18> FLASH_SECURITY
R201 1KR0402
from 4.7K change to 1K for PDG
Add CNVi function
<20> CNVI_RF_RESET CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
CH32 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
<20> MODEN_CLKREQ CH29 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
Follow 14B1 change HDA R/C value for SA #2018.08.15
<21> HDA_SYNC R192 33R0402 HDA_SYNC_PCH
<21> HDA_BIT_CLK R197 33R0402 HDA_BIT_CLK_PCH
<21> HDA_SDOUT R195 22R0402 HDA_SDOUT_PCH
<21> HDA_RST# R179 22R0402 HDA_RST#_PCH
CP24 GPP_D19/DMIC_CLK0/SNDW4_CLK
CN24 GPP_D20/DMIC_DATA0/SNDW4_DATA
CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK
CJ25 GPP_D18/DMIC_DATA1/SNDW3_DATA
CF35 GPP_B14/SPKR
EC33 X_C2p50N0402
EC15 X_C2p50N0402
EC13 X_C2p50N0402
EC14 C10p50N0402
Cap close to PCH
GPP_G0/SD_CMD CH36
GPP_G1/SD_DATA0 CL35
GPP_G2/SD_DATA1 CL36
GPP_G3/SD_DATA2 CM35
GPP_G4/SD_DATA3 CN35
GPP_G5/SD_CD# CH35
GPP_G6/SD_CLK CK36
GPP_G7/SD_WP CK34
2018.06.11 Remove Sensor INT function pin
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7 BW36
GPP_A16/SD_1P8_SEL BY31
SD_1P8_RCOMP CK33
SD_3P3_RCOMP CM34 SD_RCOMP R445 200R1%0402
SD_RCOMP can combine with a resistor
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WHL-i7-8565U
A0D-8565U05-I06
Add CNVI_RF_RESET pull down resistor position from module side to PCH side #2018.08.24
CNVI_RF_RESET
close to SOC
R215 75KR1%0402
GND
+3VRUN
+3VSUS
R49 10KR0402
U5
C56 C0.1u25X50402
<18> EC_PROCHOT#
74AHC1G07GW_SOT353-RH
EC_PROCHOT#_OD
R50 100R0402
2016/04/14 add dumping resistor for nec request
+VCCSTG
PDG 561280 Page 243
R39 1KR0402
TPJNC5
<18> H_PECI
R54 499R1%0402
<44,48> IMVP_PROCHOT#
2018.05.25 add EC_PROCHOT#_OD signal
+VCCST
R35 1KR0402
THERMTRIP#
CPU1D
H_CATERR# AA4 CATERR#
AR1 PECI
H_PROCHOT#_R Y4 PROCHOT#
THERMTRIP# BJ1 THRMTRIP#
U1 BPM#_0
U2 BPM#_1
U3 BPM#_2
U4 BPM#_3
2018.06.11 Change SCI wake up function pin from GPP_C2 to GPP_E3
<18> SCI_WAKE_UP# CE9 GPP_E3/CPU_GP0
<18> ACPI_RadioSW CN3 GPP_E7/CPU_GP1
CB34 GPP_B3/CPU_GP2
Del ASM1142 cap
CC35 GPP_B4/CPU_GP3
R415 49.9R1%0402 PROC_POPIRCOMP BP27 PROC_POPIRCOMP
R406 49.9R1%0402 PCH_OPIRCOMP BW25 PCH_OPIRCOMP
PROC_TCK T6 JTAG_TCK_JNC
PROC_TDI U6 JTAG_TDI_JNC
PROC_TDO Y5 JTAG_TDO_JNC
PROC_TMS T5 JTAG_TMS_JNC
PROC_TRST# AB6 JTAG_TRST#_JNC TPJNC45
2018.06.04 Follow PDG 575412 Figure 13-6 for DCI debug
R360 51R1%0402
R40 51R1%0402
+VCCSTG
PCH_TCK W6 PCH_JTAG_TCK TPJNC46
PCH_TDI U5 JTAG_TDI_JNC TPJNC13
PCH_TDO W5 JTAG_TDO_JNC
PCH_TMS P5 JTAG_TMS_JNC
PCH_TRST# Y6 JTAG_TRST#_JNC TPJNC14
PCH_JTAGX P6 JTAG_TCK_JNC
2018.06.14 PCH_JTAG_TCK signal add Test Point
PROC_PREQ# W2 PROC_PREQ# TPJNC11
PROC_PRDY# W1 PROC_PRDY# TPJNC9
2016/04/22 It deleted S0ix signal is not support CS mode for nec request
WHL-i7-8565U
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A0D-8565U05-I06
+3VSUS
10KR0402 R92 SCI_WAKE_UP#

MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U(HDA;MISC,JTAG)

Size	Document Number	Rev
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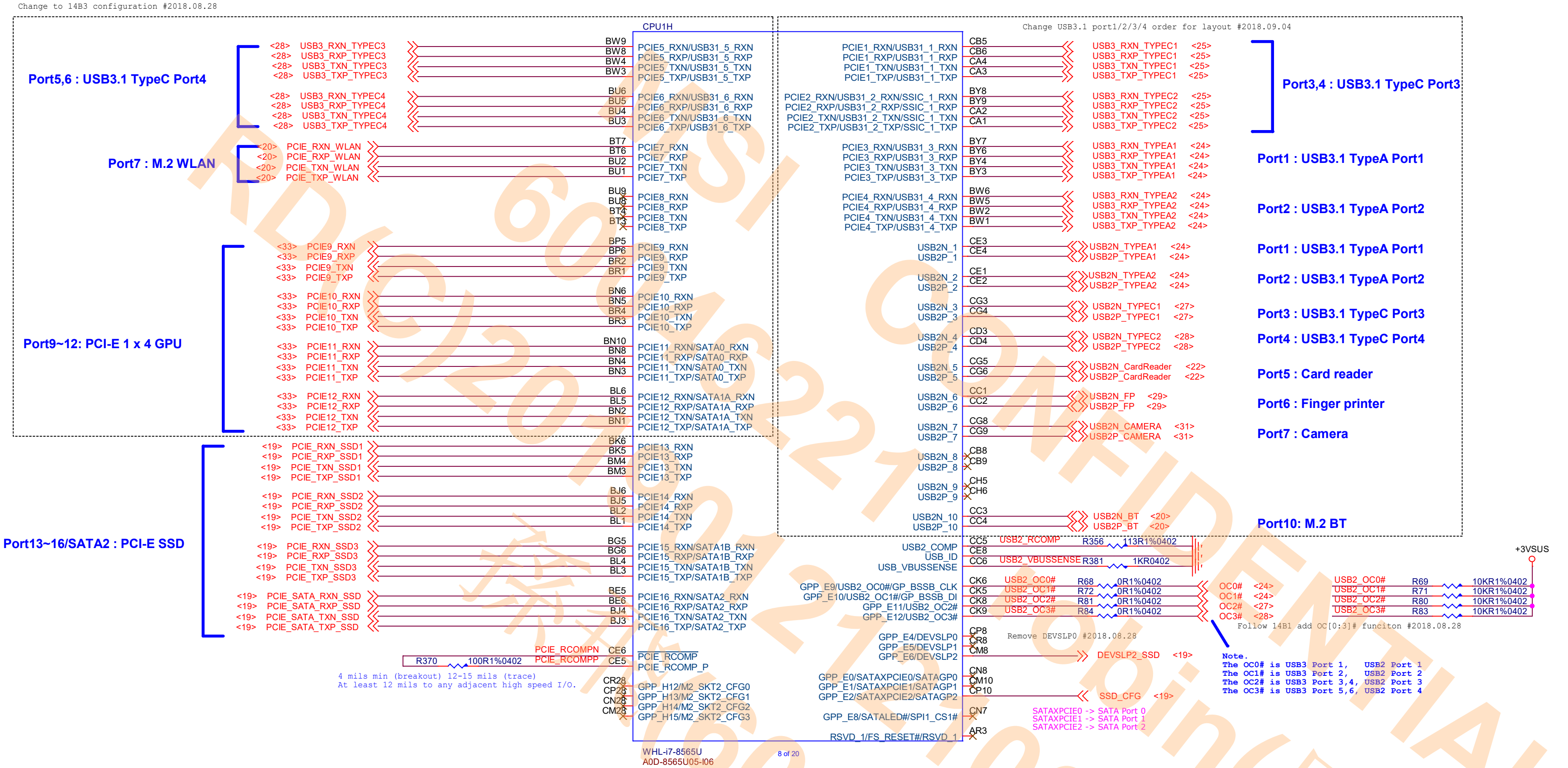
AC coupling capacitors on motherboard are recommended to be placed
closer to either the connector or processor side.
Avoid placing AC caps at the center of the motherboard.

Change to 14B3 configuration #2018.08.28



CPU1H
Change USB3.1 port1/2/3/4 order for layout #2018.09.04
Port5,6 : USB3.1 TypeC Port4
Port7 : M.2 WLAN
Port9~12: PCI-E 1 x 4 GPU
Port13~16/SATA2 : PCI-E SSD
Port3,4 : USB3.1 TypeC Port3
Port1 : USB3.1 TypeA Port1
Port2 : USB3.1 TypeA Port2
Port1 : USB3.1 TypeA Port1
Port2 : USB3.1 TypeA Port2
Port3 : USB3.1 TypeC Port3
Port4 : USB3.1 TypeC Port4
Port5 : Card reader
Port6 : Finger printer
Port7 : Camera
Port10: M.2 BT
+3VSUS
Remove DEVSLP0 #2018.08.28
Follow 14B1 add OC[0:3]# funciton #2018.08.28
Note.
The OC0# is USB3 Port 1, USB2 Port 1
The OC1# is USB3 Port 2, USB2 Port 2
The OC2# is USB3 Port 3,4, USB2 Port 3
The OC3# is USB3 Port 5,6, USB2 Port 4
SATAXPCIE0 -> SATA Port 0
SATAXPCIE1 -> SATA Port 1
SATAXPCIE2 -> SATA Port 2
4 mils min (breakout) 12-15 mils (trace)
At least 12 mils to any adjacent high speed I/O.
WHL-i7-8565U
A0D-8565U05-I06
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Reference 16S1

MICRO-STAR INT'L CO.,LTD.

Title	Whiskey lake U(PCIE;USB;SATA)	
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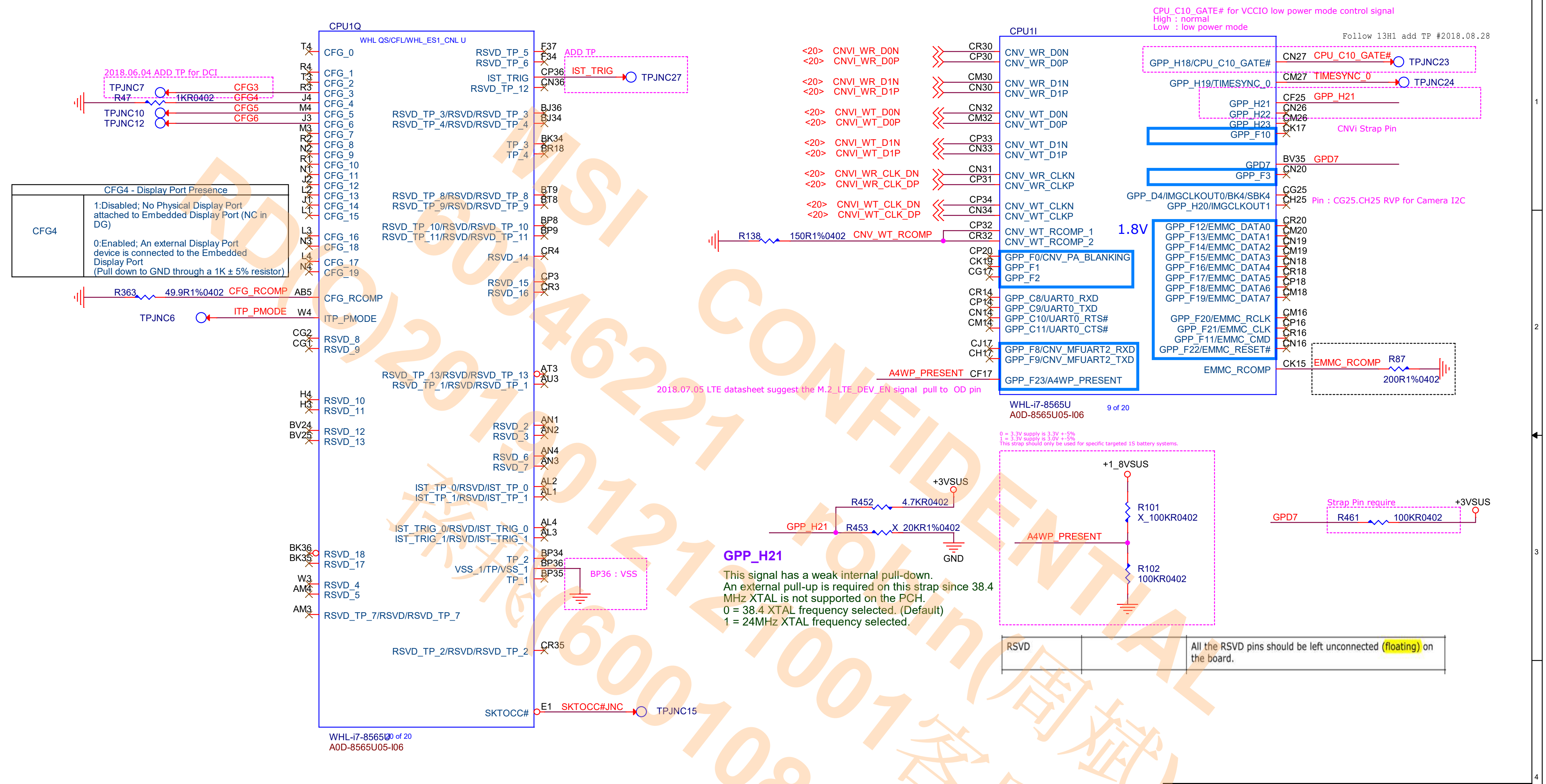
CPU1Q
WHL QS/CFL/WHL_ES1_CNL U
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_18
CFG_17
CFG_19
CFG_RCOMP
ITP_PMODE
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_18
RSVD_17
RSVD_4
RSVD_5
RSVD_TP_7/RSVD/RSVD_TP_7
RSVD_TP_5
RSVD_TP_6
IST_TRIG
RSVD_TP_12
RSVD_TP_3/RSVD/RSVD_TP_3
RSVD_TP_4/RSVD/RSVD_TP_4
TP_3
TP_4
RSVD_TP_8/RSVD/RSVD_TP_8
RSVD_TP_9/RSVD/RSVD_TP_9
RSVD_TP_10/RSVD/RSVD_TP_10
RSVD_TP_11/RSVD/RSVD_TP_11
RSVD_14
RSVD_15
RSVD_16
RSVD_TP_13/RSVD/RSVD_TP_13
RSVD_TP_1/RSVD/RSVD_TP_1
RSVD_2
RSVD_3
RSVD_6
RSVD_7
IST_TP_0/RSVD/IST_TP_0
IST_TP_1/RSVD/IST_TP_1
IST_TRIG_0/RSVD/IST_TRIG_0
IST_TRIG_1/RSVD/IST_TRIG_1
TP_2
VSS_1/TP/VSS_1
TP_1
RSVD_TP_2/RSVD/RSVD_TP_2
SKTOCC#
WHL-i7-8565U 10 of 20
A0D-8565U05-I06
2018.06.04 ADD TP for DCI
TPJNC7
R47 1KR0402
CFG3
CFG4
CFG5
CFG6
TPJNC10
TPJNC12
ADD TP
IST_TRIG
TPJNC27
R363 49.9R1%0402 CFG_RCOMP
TPJNC6 ITP_PMODE
BP36 : VSS
E1 SKTOCC#JNC TPJNC15
CFG4 - Display Port Presence
CFG4
1:Disabled; No Physical Display Port attached to Embedded Display Port (NC in DG)
0:Enabled; An external Display Port device is connected to the Embedded Display Port
(Pull down to GND through a 1K ± 5% resistor)
CPU_C10_GATE# for VCCIO low power mode control signal
High : normal
Low : low power mode
Follow 13H1 add TP #2018.08.28
CPU1I
<20> CNVI_WR_D0N
<20> CNVI_WR_D0P
<20> CNVI_WR_D1N
<20> CNVI_WR_D1P
<20> CNVI_WT_D0N
<20> CNVI_WT_D0P
<20> CNVI_WT_D1N
<20> CNVI_WT_D1P
<20> CNVI_WR_CLK_DN
<20> CNVI_WR_CLK_DP
<20> CNVI_WT_CLK_DN
<20> CNVI_WT_CLK_DP
CNV_WR_D0N
CNV_WR_D0P
CNV_WR_D1N
CNV_WR_D1P
CNV_WT_D0N
CNV_WT_D0P
CNV_WT_D1N
CNV_WT_D1P
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WT_CLKN
CNV_WT_CLKP
CNV_WT_RCOMP_1
CNV_WT_RCOMP_2
R138 150R1%0402 CNV_WT_RCOMP
GPP_F0/CNV_PA_BLANKING
GPP_F1
GPP_F2
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_F8/CNV_MFUART2_RXD
GPP_F9/CNV_MFUART2_TXD
GPP_F23/A4WP_PRESENT
A4WP_PRESENT
2018.07.05 LTE datasheet suggest the M.2_LTE_DEV_EN signal pull to OD pin
GPP_H18/CPU_C10_GATE#
GPP_H19/TIMESYNC_0
GPP_H21
GPP_H22
GPP_H23
GPP_F10
GPD7
GPP_F3
GPP_D4/IMGCLKOUT0/BK4/SBK4
GPP_H20/IMGCLKOUT1
1.8V
GPP_F12/EMMC_DATA0
GPP_F13/EMMC_DATA1
GPP_F14/EMMC_DATA2
GPP_F15/EMMC_DATA3
GPP_F16/EMMC_DATA4
GPP_F17/EMMC_DATA5
GPP_F18/EMMC_DATA6
GPP_F19/EMMC_DATA7
GPP_F20/EMMC_RCLK
GPP_F21/EMMC_CLK
GPP_F11/EMMC_CMD
GPP_F22/EMMC_RESET#
EMMC_RCOMP
CPU_C10_GATE# TPJNC23
TIMESYNC_0 TPJNC24
GPP_H21
CNVi Strap Pin
GPD7
Pin : CG25.CH25 RVP for Camera I2C
EMMC_RCOMP R87 200R1%0402
WHL-i7-8565U 9 of 20
A0D-8565U05-I06
+3VSUS
R452 4.7KR0402
GPP_H21 R453 X_20KR1%0402
GND
GPP_H21
This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.
+1_8VSUS
R101 X_100KR0402
A4WP_PRESENT
R102 100KR0402
Strap Pin require
GPD7 R461 100KR0402 +3VSUS
RSVD
All the RSVD pins should be left unconnected (floating) on the board.

Reference 16S1

MICRO-STAR INT'L CO.,LTD.

Title	Whiskey lake U (CFG;CSI;RSVD)
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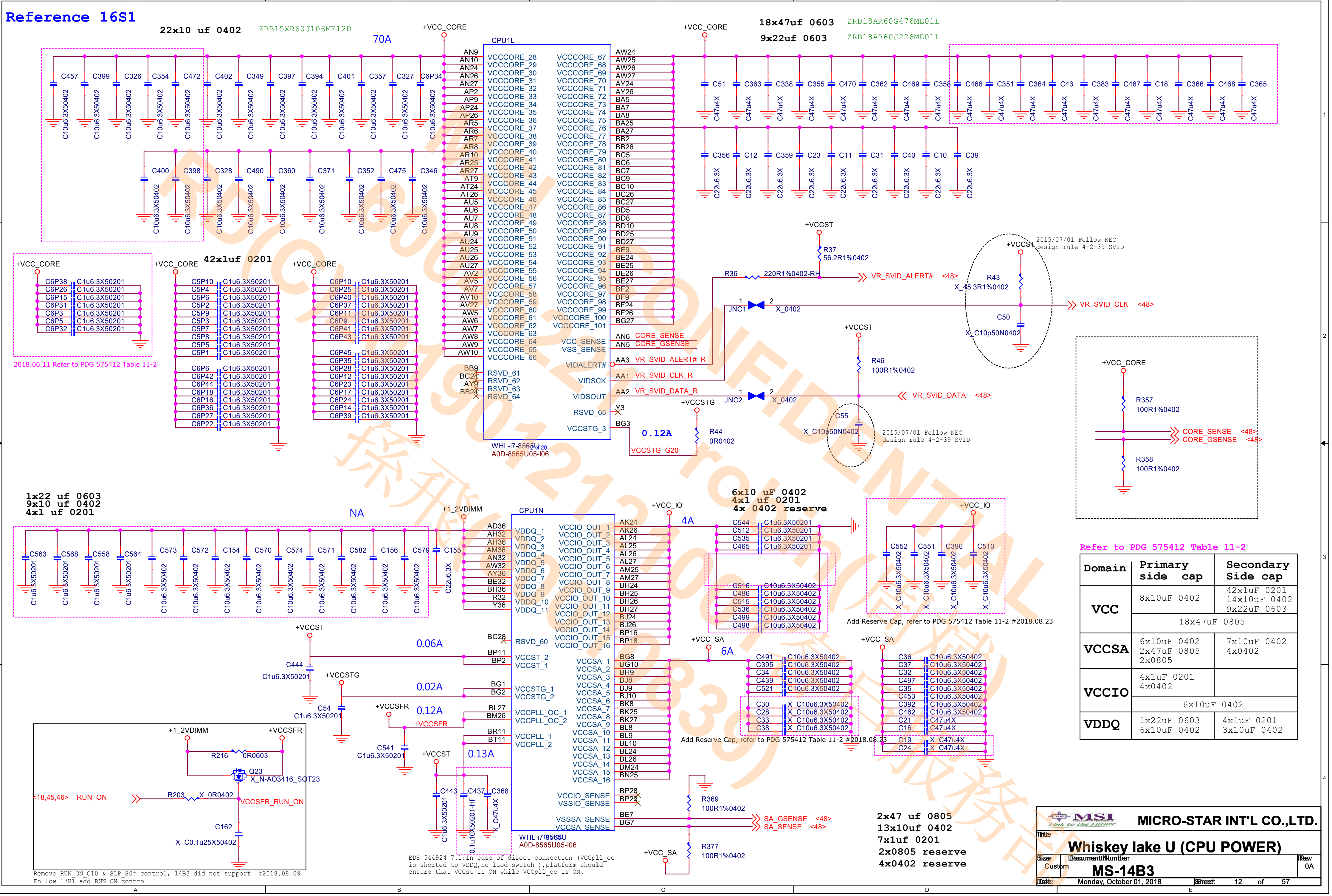

22x10 uf 0402 ZRB15XR60J106ME12D
70A
+VCC_CORE
CPU1L
18x47uf 0603 ZRB18AR60G476ME01L
9x22uf 0603 ZRB18AR60J226ME01L
42x1uf 0201
2018.06.11 Refer to PDG 575412 Table 11-2
WHL-i7-8565U
A0D-8565U05-I06
VR_SVID_ALERT# <48>
VR_SVID_CLK <48>
VR_SVID_DATA <48>
CORE_SENSE <48>
CORE_GSENSE <48>
2015/07/01 Follow NEC design rule 4-2-39 SVID
VCCSTG_G20
0.12A
1x22 uf 0603
9x10 uf 0402
4x1 uf 0201
NA
CPU1N
+1_2VDIMM
+VCC_IO
4A
6x10 uF 0402
4x1 uF 0201
4x 0402 reserve
Add Reserve Cap, refer to PDG 575412 Table 11-2 #2018.08.23
+VCCST
0.06A
+VCCSTG
0.02A
+VCCSFR
0.12A
0.13A
+VCC_SA
6A
Add Reserve Cap, refer to PDG 575412 Table 11-2 #2018.08.23
SA_GSENSE <48>
SA_SENSE <48>
<18,45,46> RUN_ON
VCCSFR_RUN_ON
Remove RUN_ON_C10 & SLP_S0# control, 14B3 did not support #2018.08.09
Follow 13H1 add RUN_ON control
EDS 544924 7.1:In case of direct connection (VCCpll_oc is shorted to VDDQ,no laod switch),platform should ensure that VCCst is ON while VCCpll_oc is ON.
2x47 uf 0805
13x10uf 0402
7x1uf 0201
2x0805 reserve
4x0402 reserve

Refer to PDG 575412 Table 11-2

Domain	Primary side cap	Secondary Side cap
VCC	8x10uF 0402	42x1uF 0201 14x10uF 0402 9x22uF 0603
	18x47uF 0805	
VCCSA	6x10uF 0402 2x47uF 0805 2x0805	7x10uF 0402 4x0402
VCCIO	4x1uF 0201 4x0402	
	6x10uF 0402	
VDDQ	1x22uF 0603 6x10uF 0402	4x1uF 0201 3x10uF 0402

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Title: Whiskey lake U (CPU POWER)

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ZRB18AR60G476ME01L
ZRB18AR60J226ME01L
4x47 uf 0603
15x22 uf 0603
+VCC_GT
31A
CPU1M
WHL QS/CFL/WHL_ES1_CNL U
C408 C405 C450 C407 C70 C409 C459
C526 C69 C71 C72 C441 C404 C406 C531
C22u6.3X
2018.06.11 Refer to PDG 575412 Table 11-2
C529 C527 C528 C473
C47u4X
VCCGT_1 VCCGT_2 VCCGT_3 VCCGT_4 VCCGT_5 VCCGT_6 VCCGT_7 VCCGT_8 VCCGT_9 VCCGT_10 VCCGT_11 VCCGT_12 VCCGT_13 VCCGT_14 VCCGT_15 VCCGT_16 VCCGT_17 VCCGT_18 VCCGT_19 VCCGT_20 VCCGT_21 VCCGT_22 VCCGT_23 VCCGT_24 VCCGT_25 VCCGT_26 VCCGT_27 VCCGT_28 VCCGT_29 VCCGT_30 VCCGT_31 VCCGT_32 VCCGT_33 VCCGT_34 VCCGT_35 VCCGT_36 VCCGT_37 VCCGT_38 VCCGT_39 VCCGT_40 VCCGT_41 VCCGT_42 VCCGT_43 VCCGT_44 VCCGT_45 VCCGT_46 VCCGT_47 VCCGT_48 VCCGT_49 VCCGT_50 VCCGT_51 VCCGT_52 VCCGT_53 VCCGT_54 VCCGT_55 VCCGT_56 VCCGT_57 VCCGT_58 VCCGT_59 VCCGT_0
VCCGT_60 VCCGT_61 VCCGT_62 VCCGT_63 VCCGT_64 VCCGT_65 VCCGT_66 VCCGT_67 VCCGT_68 VCCGT_69 VCCGT_70 VCCGT_71 VCCGT_72 VCCGT_73 VCCGT_74 VCCGT_75 VCCGT_76 VCCGT_77 VCCGT_78 VCCGT_79 VCCGT_80 VCCGT_81 VCCGT_82 VCCGT_83 VCCGT_84 VCCGT_85 VCCGT_86 VCCGT_87 VCCGT_88 VCCGT_89 VCCGT_90 VCCGT_91 VCCGT_92
VCCCORE_1/VCCGT_93/VCCGT_93 VCCCORE_2/VCCGT_94/VCCGT_94 VCCCORE_3/VCCGT_95/VCCGT_95 VCCCORE_4/VCCGT_96/VCCGT_96 VCCCORE_5/VCCGT_97/VCCGT_97 VCCCORE_6/VCCGT_98/VCCGT_98 VCCCORE_7/VCCGT_99/VCCGT_99 VCCCORE_8/VCCGT_100/VCCGT_100 VCCCORE_9/VCCGT_101/VCCGT_101 VCCCORE_10/VCCGT_102/VCCGT_102 VCCCORE_11/VCCGT_103/VCCGT_103 VCCCORE_12/VCCGT_104/VCCGT_104 VCCCORE_13/VCCGT_105/VCCGT_105 VCCCORE_14/VCCGT_106/VCCGT_106 VCCCORE_15/VCCGT_107/VCCGT_107 VCCCORE_16/VCCGT_108/VCCGT_108 VCCCORE_17/VCCGT_109/VCCGT_109 VCCCORE_18/VCCGT_110/VCCGT_110 VCCCORE_19/VCCGT_111/VCCGT_111 VCCCORE_20/VCCGT_112/VCCGT_112 VCCCORE_21/VCCGT_113/VCCGT_113 VCCCORE_22/VCCGT_114/VCCGT_114 VCCCORE_23/VCCGT_115/VCCGT_115 VCCCORE_24/VCCGT_116/VCCGT_116 VCCCORE_25/VCCGT_117/VCCGT_117 VCCCORE_26/VCCGT_118/VCCGT_118 VCCCORE_27/VCCGT_119/VCCGT_119
VCCGT_SENSE VSSGT_SENSE
WHL-i7-8565U
A0D-8565U05-I06
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+VCC_GT
15x10 uf 0402
C6P33 C6P2 C6P1 C6P8 C389 C506 C411 C449 C461 C429 C451 C532 C478 C396 C423
C10u6.3X50402
11x1 uf 0201
C6P21 C6P20 C6P13 C6P29 C6P30 C6P7 C6P4 C6P19 C403 C421 C448
C1u6.3X50201
+VCC_CORE
PWR short to Vcore for WHL ES2 Pin out
Cap close to Pin out
Refer to PDG 575412 Table 11-6
Domain	Primary side cap	Secondary Side cap
VCCGT	15x22uF 0603 4x47uF 0805	11x1uF 0201 15x10uF 0402
R53 100R1%0402
R58 100R1%0402
GT_SENSE <48>
GT_GSENSE <48>
VCCOPC/VCCOPC_1P8 . VCCEOPIO for U43e only
CPU1O
WHL QS/CFL U/WHL ES1_CNL U22
RSVD_25/VCC_OPC_1/RSVD_25 RSVD_26/VCC_OPC_2/RSVD_26 RSVD_27/VCC_OPC_3/RSVD_27 RSVD_28/VCC_OPC_4/RSVD_28 RSVD_29/VCC_OPC_5/RSVD_29 RSVD_30/VCC_OPC_6/RSVD_30 RSVD_31/VCC_OPC_7/RSVD_31 RSVD_32/VCC_OPC_8/RSVD_32 RSVD_33/VCC_OPC_9/RSVD_23 RSVD_34/VCC_OPC_10/RSVD_34 RSVD_35/VCC_OPC_11/RSVD_35 RSVD_36/VCC_OPC_12/RSVD_36 RSVD_37/VCC_OPC_13/RSVD_37 RSVD_38/VCC_OPC_14/RSVD_38 RSVD_21/VCC_OPC_1P8_3/RSVD_21 RSVD_22/VCC_OPC_1P8_4/RSVD_22 RSVD_23/VCC_OPC_1P8_1/RSVD_23 RSVD_24/VCC_OPC_1P8_2/RSVD_24 RSVD_47 RSVD_48 RSVD_49/VSS_435/RSVD_49 RSVD_50/VSS_436/RSVD_50 RSVD_51/VSS_437/RSVD_51 RSVD_52/RSVD_TP/RSVD_52 RSVD_53/RSVD_TP/RSVD_53 RSVD_54/MSM#/RSVD_54 RSVD_55/ZVM#/RSVD_55 RSVD_59/OPCE_RCOMP/RSVD_59
RSVD_39/VCCEOPIO_1/RSVD_39 RSVD_40/VCCEOPIO_2/RSVD_40 RSVD_41/VCCEOPIO_3/RSVD_41 RSVD_42/VCCEOPIO_4/RSVD_42 RSVD_43/VCCEOPIO_5/RSVD_43 RSVD_44/VCCEOPIO_6/RSVD_44 RSVD_45/VCCEOPIO_7/RSVD_45 RSVD_46/VCCEOPIO_8/RSVD_46 RSVD_19/VCCEOPIO_SENSE/RSVD_19 RSVD_20/VSSEOPIO_SENSE/RSVD_20 RSVD_56 RSVD_57 RSVD_58/OPC_RCOMP/RSVD_58
OPC_RCOMP
X_49.9R1%0402 R354
For Coffee lake
All O package pinout is RSVD in WHL
TPJNC48 TPJNC49
MSM# LPM_ZVM# OPCE_RCOMP
X_49.9R1%0402 R353
For Coffee lake
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WHL-i7-8565U
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MICRO-STAR INT'L CO.,LTD.
Title: Whiskey lake U (GT POWER)
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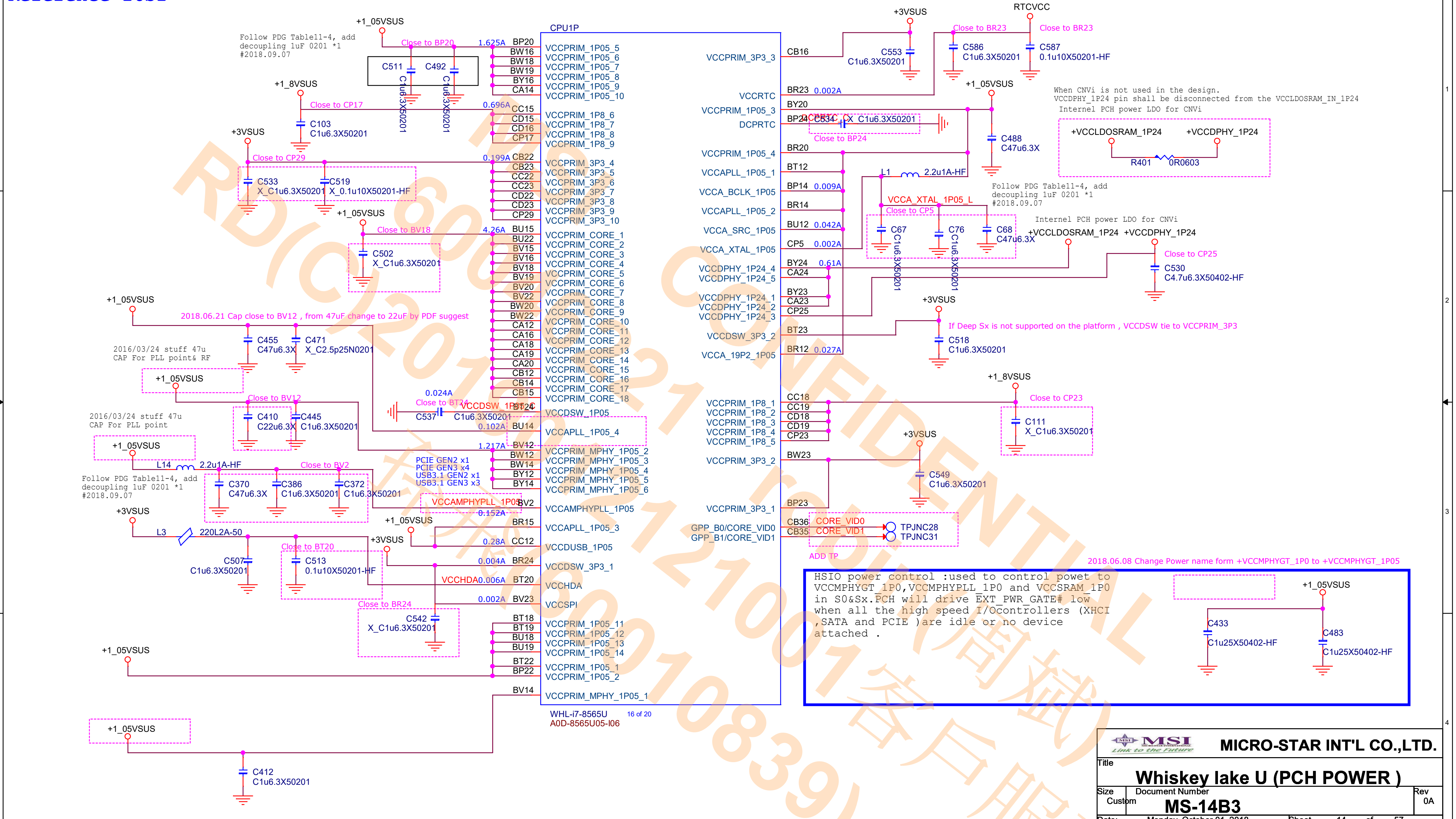
ZRB15XR60J106ME12D

Reference 16S1



CPU1P
+1_05VSUS
Follow PDG Table11-4, add decoupling 1uF 0201 *1 #2018.09.07
Close to BP20
C511 C492
C1u6.3X50201
1.625A
BP20 BW16 BW18 BW19 BY16 CA14
VCCPRIM_1P05_5
VCCPRIM_1P05_6
VCCPRIM_1P05_7
VCCPRIM_1P05_8
VCCPRIM_1P05_9
VCCPRIM_1P05_10
+1_8VSUS
Close to CP17
C103 C1u6.3X50201
0.696A
CC15 CD15 CD16 CP17
VCCPRIM_1P8_6
VCCPRIM_1P8_7
VCCPRIM_1P8_8
VCCPRIM_1P8_9
+3VSUS
Close to CP29
C533 X_C1u6.3X50201
C519 X_0.1u10X50201-HF
0.199A
CB22 CB23 CC22 CC23 CD22 CD23 CP29
VCCPRIM_3P3_4
VCCPRIM_3P3_5
VCCPRIM_3P3_6
VCCPRIM_3P3_7
VCCPRIM_3P3_8
VCCPRIM_3P3_9
VCCPRIM_3P3_10
Close to BV18
C502 X_C1u6.3X50201
4.26A
BU15 BU22 BV15 BV16 BV18 BV19 BV20 BV22 BW20 BW22 CA12 CA16 CA18 CA19 CA20 CB12 CB14 CB15
VCCPRIM_CORE_1 … VCCPRIM_CORE_18
2018.06.21 Cap close to BV12 , from 47uF change to 22uF by PDF suggest
C455 C47u6.3X
C471 X_C2.5p25N0201
2016/03/24 stuff 47u CAP For PLL point& RF
Close to BV12
C410 C22u6.3X
C445 C1u6.3X50201
2016/03/24 stuff 47u CAP For PLL point
0.024A
Close to BT24
C537 C1u6.3X50201
VCCDSW_1P05
BT24
VCCDSW_1P05
0.102A
BU14
VCCAPLL_1P05_4
1.217A
BV12 BW12 BW14 BY12 BY14
VCCPRIM_MPHY_1P05_2
VCCPRIM_MPHY_1P05_3
VCCPRIM_MPHY_1P05_4
VCCPRIM_MPHY_1P05_5
VCCPRIM_MPHY_1P05_6
PCIE GEN2 x1
PCIE GEN3 x4
USB3.1 GEN2 x1
USB3.1 GEN3 x3
L14 2.2u1A-HF
Close to BV2
C370 C47u6.3X
C386 C1u6.3X50201
C372 C1u6.3X50201
Follow PDG Table11-4, add decoupling 1uF 0201 *1 #2018.09.07
VCCAMPHYPLL_1P05
BV2
VCCAMPHYPLL_1P05
0.152A
BR15
VCCAPLL_1P05_3
L3 220L2A-50
C507 C1u6.3X50201
Close to BT20
C513 0.1u10X50201-HF
0.28A
CC12
VCCDUSB_1P05
0.004A
BR24
VCCDSW_3P3_1
VCCHDA 0.006A
BT20
VCCHDA
0.002A
BV23
VCCSPI
Close to BR24
C542 X_C1u6.3X50201
BT18 BT19 BU18 BU19
VCCPRIM_1P05_11
VCCPRIM_1P05_12
VCCPRIM_1P05_13
VCCPRIM_1P05_14
BT22 BP22
VCCPRIM_1P05_1
VCCPRIM_1P05_2
BV14
VCCPRIM_MPHY_1P05_1
C412 C1u6.3X50201
WHL-i7-8565U
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A0D-8565U05-I06
VCCPRIM_3P3_3
CB16
C553 C1u6.3X50201
RTCVCC
Close to BR23
C586 C1u6.3X50201
C587 0.1u10X50201-HF
VCCRTC
BR23 0.002A
VCCPRIM_1P05_3
BY20
DCPRTC
BP24
C534 X_C1u6.3X50201
Close to BP24
C488 C47u6.3X
When CNVi is not used in the design. VCCDPHY_1P24 pin shall be disconnected from the VCCLDOSRAM_IN_1P24
Internel PCH power LDO for CNVi
+VCCLDOSRAM_1P24
+VCCDPHY_1P24
R401 0R0603
VCCPRIM_1P05_4
BR20
VCCAPLL_1P05_1
BT12
L1 2.2u1A-HF
Follow PDG Table11-4, add decoupling 1uF 0201 *1 #2018.09.07
VCCA_BCLK_1P05
BP14 0.009A
VCCA_XTAL_1P05_L
VCCAPLL_1P05_2
BR14
Close to CP5
C67 C76 C68
C1u6.3X50201
C47u6.3X
VCCA_SRC_1P05
BU12 0.042A
VCCA_XTAL_1P05
CP5 0.002A
VCCDPHY_1P24_4
VCCDPHY_1P24_5
BY24 0.61A
CA24
Close to CP25
C530 C4.7u6.3X50402-HF
VCCDPHY_1P24_1
VCCDPHY_1P24_2
VCCDPHY_1P24_3
BY23 CA23 CP25
VCCDSW_3P3_2
BT23
If Deep Sx is not supported on the platform , VCCDSW tie to VCCPRIM_3P3
C518 C1u6.3X50201
VCCA_19P2_1P05
BR12 0.027A
Close to CP23
C111 X_C1u6.3X50201
VCCPRIM_1P8_1
VCCPRIM_1P8_2
VCCPRIM_1P8_3
VCCPRIM_1P8_4
VCCPRIM_1P8_5
CC18 CC19 CD18 CD19 CP23
VCCPRIM_3P3_2
BW23
C549 C1u6.3X50201
VCCPRIM_3P3_1
BP23
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
CB36 CORE_VID0 TPJNC28
CB35 CORE_VID1 TPJNC31
ADD TP
2018.06.08 Change Power name form +VCCMPHYGT_1P0 to +VCCMPHYGT_1P05
HSIO power control :used to control powet to VCCMPHYGT_1P0,VCCMPHYPLL_1P0 and VCCSRAM_1P0 in S0&Sx.PCH will drive EXT_PWR_GATE# low when all the high speed I/Ocontrollers (XHCI ,SATA and PCIE)are idle or no device attached .
C433 C1u25X50402-HF
C483 C1u25X50402-HF

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Title	Whiskey lake U (PCH POWER)	
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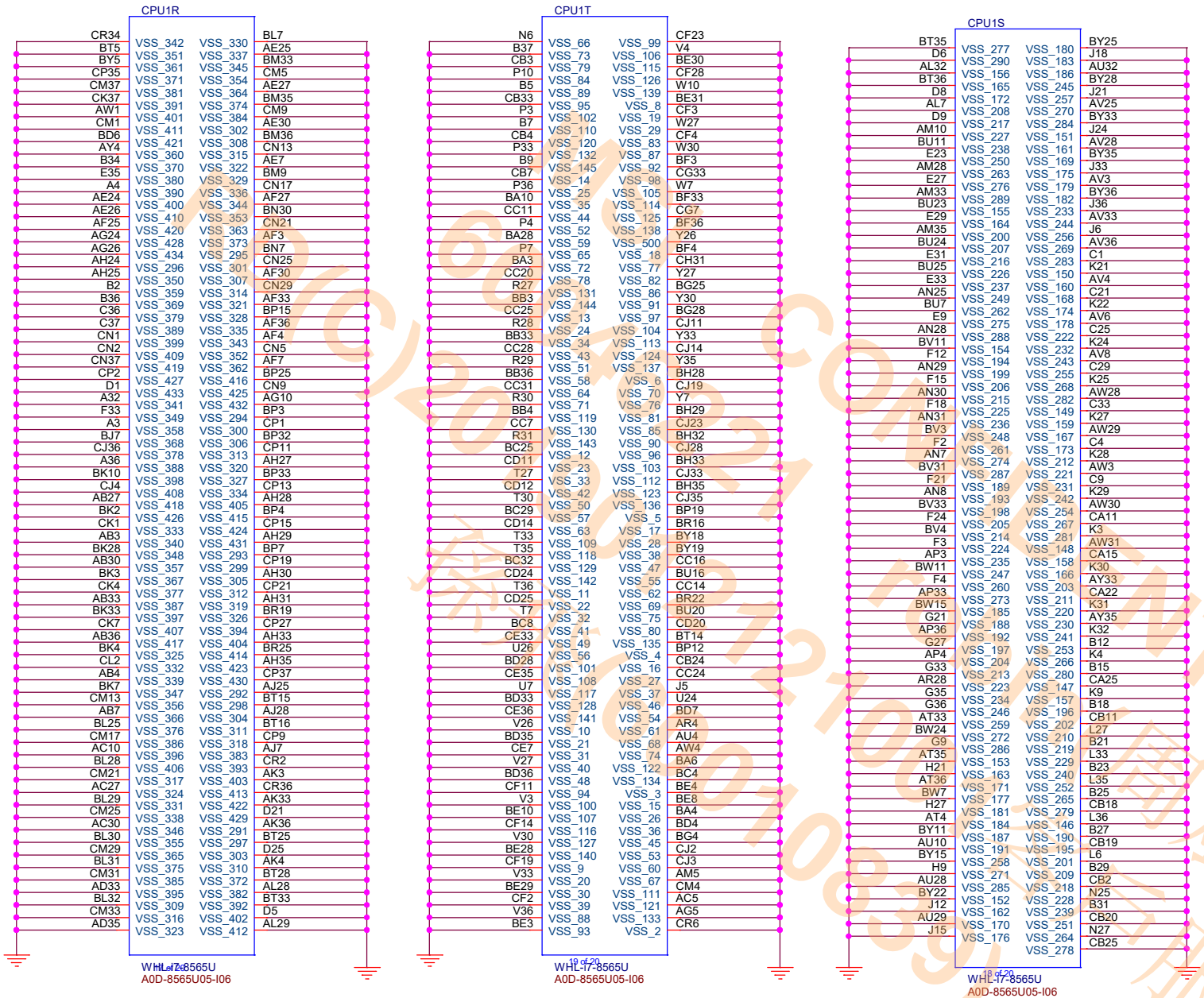

Reference 16S1

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Title: Whiskey lake U (GND)

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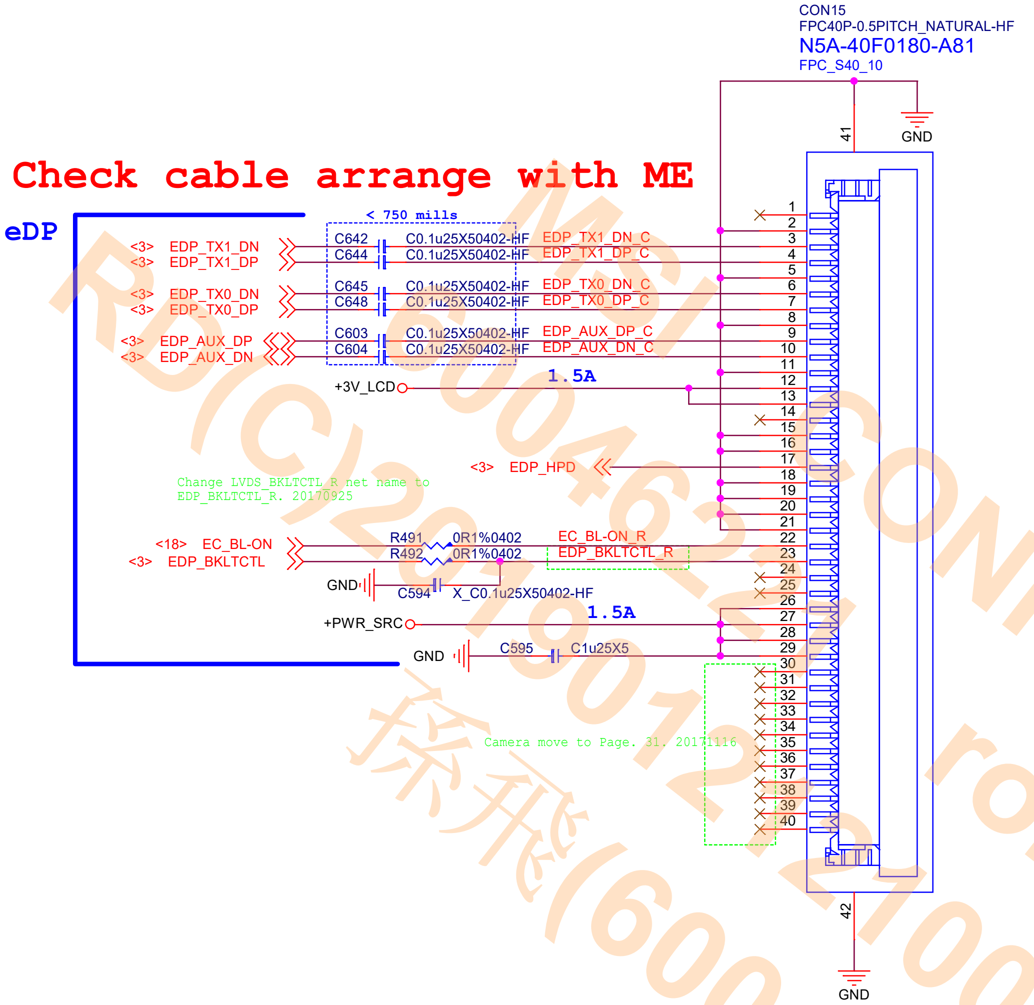

CON15
FPC40P-0.5PITCH_NATURAL-HF
N5A-40F0180-A81
FPC_S40_10
GND
Check cable arrange with ME
eDP
< 750 mills
<3> EDP_TX1_DN
<3> EDP_TX1_DP
<3> EDP_TX0_DN
<3> EDP_TX0_DP
<3> EDP_AUX_DP
<3> EDP_AUX_DN
C642 C0.1u25X50402-HF EDP_TX1_DN_C
C644 C0.1u25X50402-HF EDP_TX1_DP_C
C645 C0.1u25X50402-HF EDP_TX0_DN_C
C648 C0.1u25X50402-HF EDP_TX0_DP_C
C603 C0.1u25X50402-HF EDP_AUX_DP_C
C604 C0.1u25X50402-HF EDP_AUX_DN_C
1.5A
+3V_LCD
<3> EDP_HPD
Change LVDS_BKLTCTL_R net name to EDP_BKLTCTL_R. 20170925
<18> EC_BL-ON
<3> EDP_BKLTCTL
R491 0R1%0402 EC_BL-ON_R
R492 0R1%0402 EDP_BKLTCTL_R
GND
C594 X_C0.1u25X50402-HF
1.5A
+PWR_SRC
GND C595 C1u25X5
Camera move to Page. 31. 20171116
41
42
GND

<4.2. INTERFACE CONNECTIONS>

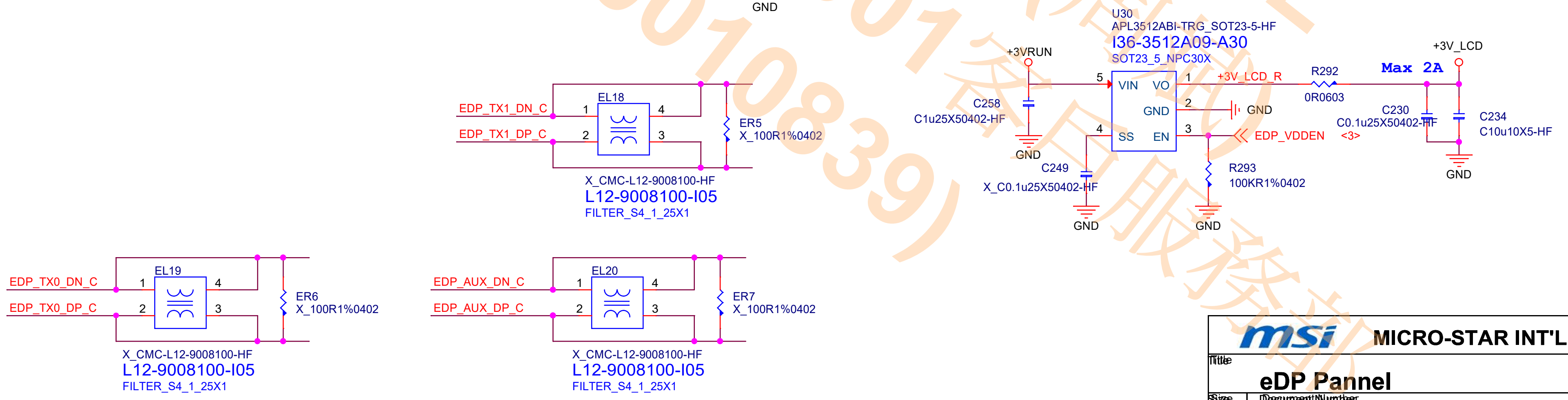
<Table 6. Pin Assignments for the Interface Connector>

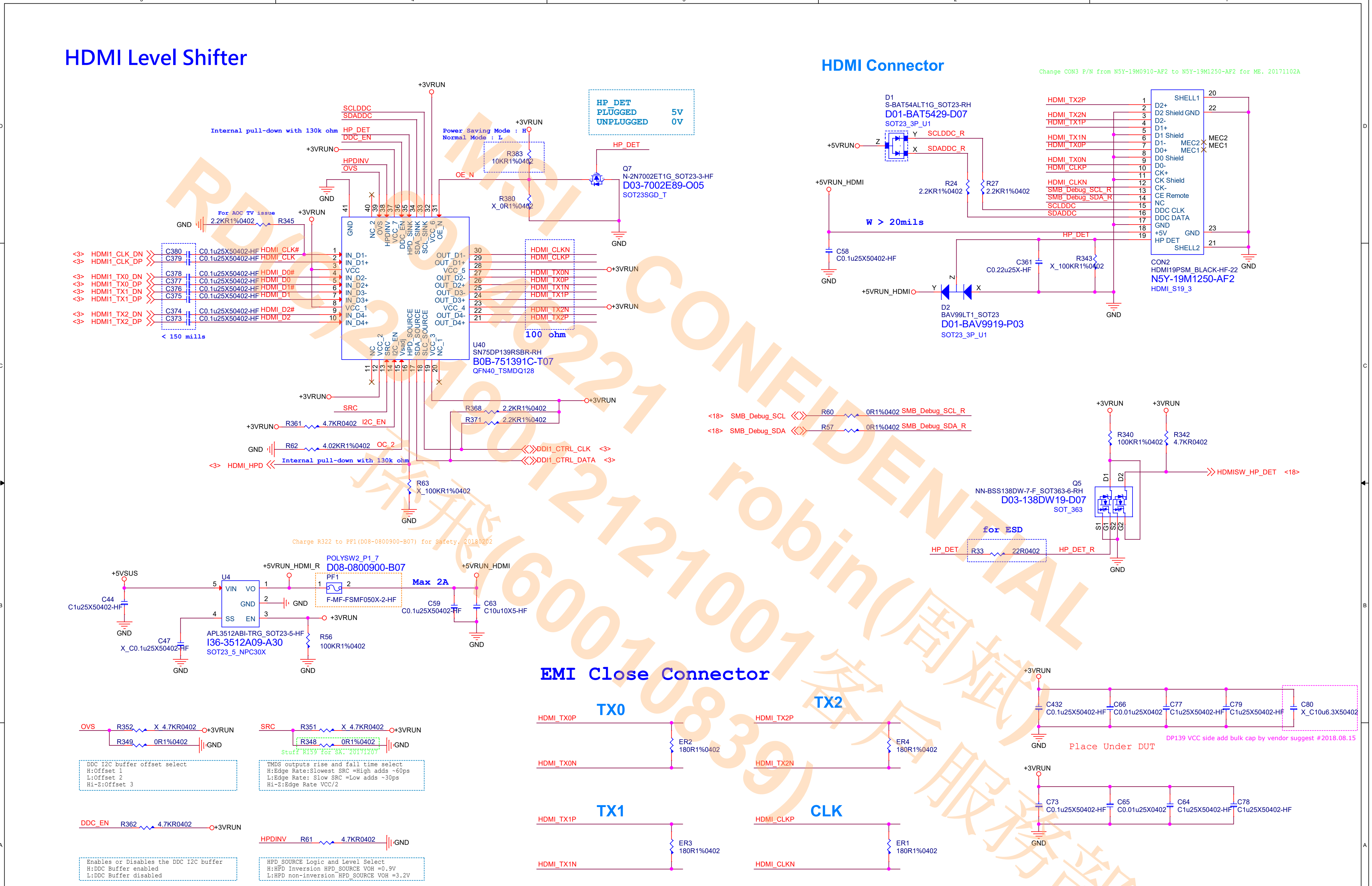
Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	CABC_Enable	CABC (not enable)
2	H-GND	Ground
3	LAN1_N	Complement Signal Link _Lane1
4	LAN1_P	True Signal Link _Lane1
5	H-GND	Ground
6	LAN0_N	Complement Signal Link _Lane0
7	LAN0_P	True Signal Link _Lane0
8	H-GND	High Speed Ground
9	AUXP	True Signal Link _Auxiliry Channel
10	AUXN	Complement Signal Link _Auxiliry Channel
11	H-GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel self test enable
15	H-GND	Ground
16	H-GND	Ground
17	HPD	HPD(Hot Plug Detect) Signal Pin
18	BL_GND	High Speed Ground
19	BL_GND	High Speed Ground
20	BL_GND	High Speed Ground
21	BL_GND	High Speed Ground
22	BL_EN	Backlight on/off Control pin
23	BL_PWM	Back light PWM Dimming
24	Hsnyc	Line synchronization
25	NC	No connection
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connection

4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	NC	No Connection (Reserved for ML1-)	
4	NC	No Connection (Reserved for ML1+)	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for INNOLUX test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for Hsync signal)	
25	NC	No Connection (Reserved for INNOLUX test)	
26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for INNOLUX test)	


U30
APL3512ABI-TRG_SOT23-5-HF
I36-3512A09-A30
SOT23_5_NPC30X
+3VRUN
C258
C1u25X50402-HF
GND
VIN VO GND SS EN
+3V_LCD_R
R292
0R0603
Max 2A
+3V_LCD
C230
C0.1u25X50402-HF
C234
C10u10X5-HF
GND
EDP_VDDEN <3>
C249
X_C0.1u25X50402-HF
R293
100KR1%0402
EDP_TX1_DN_C
EDP_TX1_DP_C
EL18
ER5
X_100R1%0402
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
EDP_TX0_DN_C
EDP_TX0_DP_C
EL19
ER6
X_100R1%0402
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
EDP_AUX_DN_C
EDP_AUX_DP_C
EL20
ER7
X_100R1%0402
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1


HDMI Level Shifter
HDMI Connector
Change CON3 P/N from N5Y-19M0910-AF2 to N5Y-19M1250-AF2 for ME. 20171102A
HP_DET
PLUGGED 5V
UNPLUGGED 0V
Internal pull-down with 130k ohm
Power Saving Mode : H
Normal Mode : L
For AOC TV issue
U40
SN75DP139RSBR-RH
B0B-751391C-T07
QFN40_TSMDQ128
100 ohm
< 150 mills
Q7
N-2N7002ET1G_SOT23-3-HF
D03-7002E89-O05
SOT23SGD_T
D1
S-BAT54ALT1G_SOT23-RH
D01-BAT5429-D07
SOT23_3P_U1
W > 20mils
D2
BAV99LT1_SOT23
D01-BAV9919-P03
SOT23_3P_U1
CON2
HDMI19PSM_BLACK-HF-22
N5Y-19M1250-AF2
HDMI_S19_3
Q5
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
for ESD
Charge R322 to PF1(D08-0800900-B07) for Safety. 20180202
POLYSW2_P1_7
D08-0800900-B07
F-MF-FSMF050X-2-HF
Max 2A
U4
APL3512ABI-TRG_SOT23-5-HF
I36-3512A09-A30
SOT23_5_NPC30X
EMI Close Connector
TX0
TX1
TX2
CLK
Place Under DUT
DP139 VCC side add bulk cap by vendor suggest #2018.08.15
Stuff R159 for SI. 20171207
DDC I2C buffer offset select
H:Offset 1
L:Offset 2
Hi-Z:Offset 3
TMDS outputs rise and fall time select
H:Edge Rate:Slowest SRC =High adds ~60ps
L:Edge Rate: Slow SRC =Low adds ~30ps
Hi-Z:Edge Rate VCC/2
Enables or Disables the DDC I2C buffer
H:DDC Buffer enabled
L:DDC Buffer disabled
HPD_SOURCE Logic and Level Select
H:HPD Inversion HPD_SOURCE VOH =0.9V
L:HPD non-inversion HPD_SOURCE VOH =3.2V
Delete EL4~7(L12-9008100-I05) for Layout. 20171024A

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Title: HDMI Level Shifter_SN75DP139

Size: Custom | Document Number: MS-14B3 | Rev: 0A

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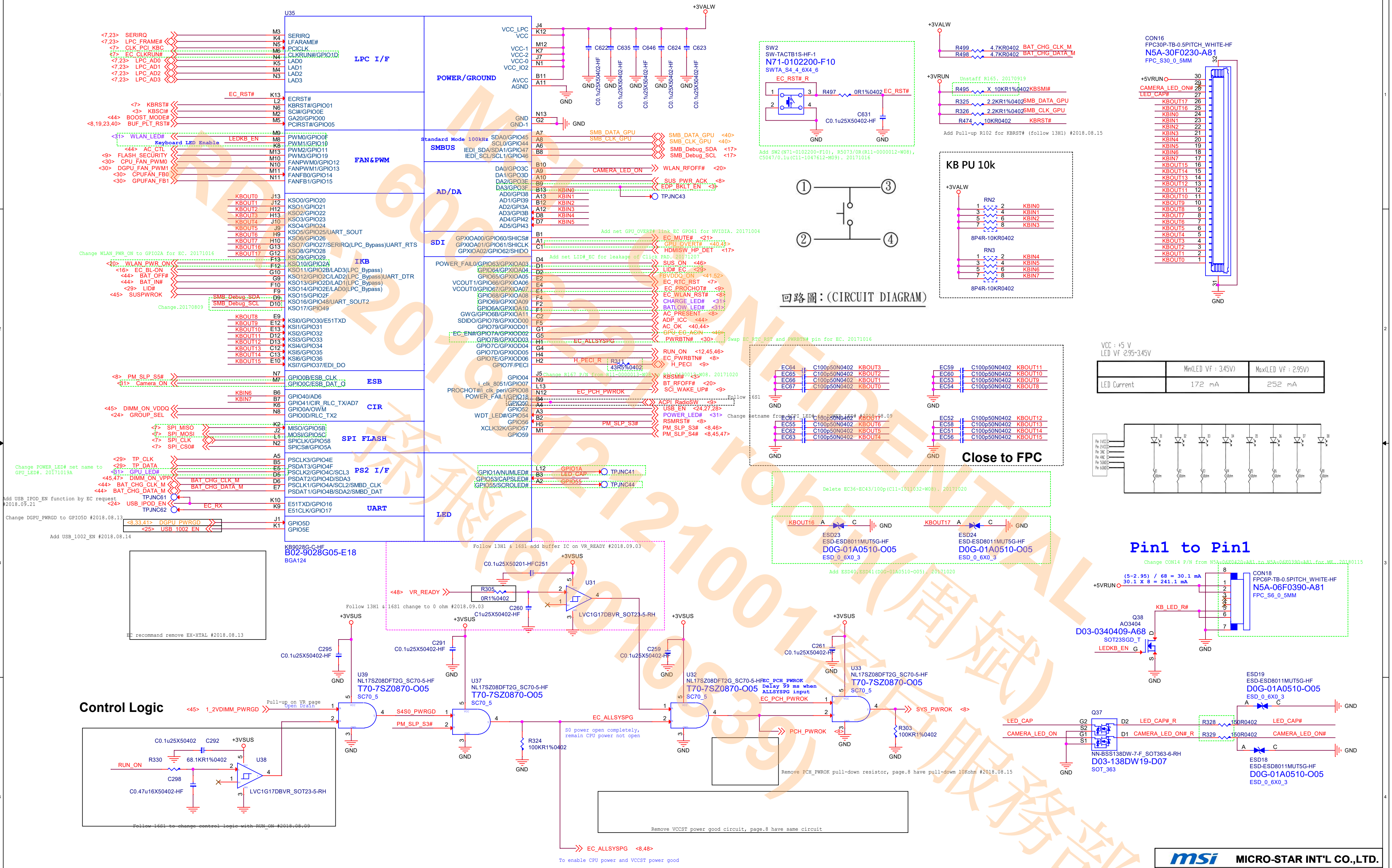

U35
LPC I/F
POWER/GROUND
FAN&PWM
AD/DA
Standard Mode 100kHz
SMBUS
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
KB9028G-C-HF
B02-9028G05-E18
BGA124
Keyboard LED Enable
SW2
SW-TACTB1S-HF-1
N71-0102200-F10
SWTA_S4_4_6X4_6
回路圖:(CIRCUIT DIAGRAM)
KB PU 10k
RN2
8P4R-10KR0402
RN3
8P4R-10KR0402
CON16
FPC30P-TB-0.5PITCH_WHITE-HF
N5A-30F0230-A81
FPC_S30_0_5MM
VCC : +5 V
LED VF :2.95~3.45V
Min(LED VF : 3.45V)
Max(LED VF : 2.95V)
LED Current
172 mA
252 mA
Close to FPC
Pin1 to Pin1
CON18
FPC6P-TB-0.5PITCH_WHITE-HF
N5A-06F0390-A81
FPC_S6_0_5MM
Q38
AO3404
D03-0340409-A68
SOT23SGD_T
ESD23
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD24
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD19
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD18
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
Q37
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
Control Logic
U31
LVC1G17DBVR_SOT23-5-RH
U38
LVC1G17DBVR_SOT23-5-RH
U39
NL17SZ08DFT2G_SC70-5-HF
T70-7SZ0870-O05
U37
NL17SZ08DFT2G_SC70-5-HF
T70-7SZ0870-O05
U32
NL17SZ08DFT2G_SC70-5-HF
T70-7SZ0870-O05
U33
NL17SZ08DFT2G_SC70-5-HF
T70-7SZ0870-O05
EC recommand remove EX-XTAL #2018.08.13
Follow 13H1 & 16S1 add buffer IC on VR_READY #2018.09.03
Follow 16S1 to change control logic with RUN_ON #2018.08.09
Remove PCH_PWROK pull-down resistor, page.8 have pull-down 10Kohm #2018.08.15
Remove VCCST power good circuit, page.8 have same circuit
To enable CPU power and VCCST power good

MICRO-STAR INT'L CO.,LTD.

Title	KBC (ENE9028)
Size	Custom
Document Number	MS-14B3
Rev	0A
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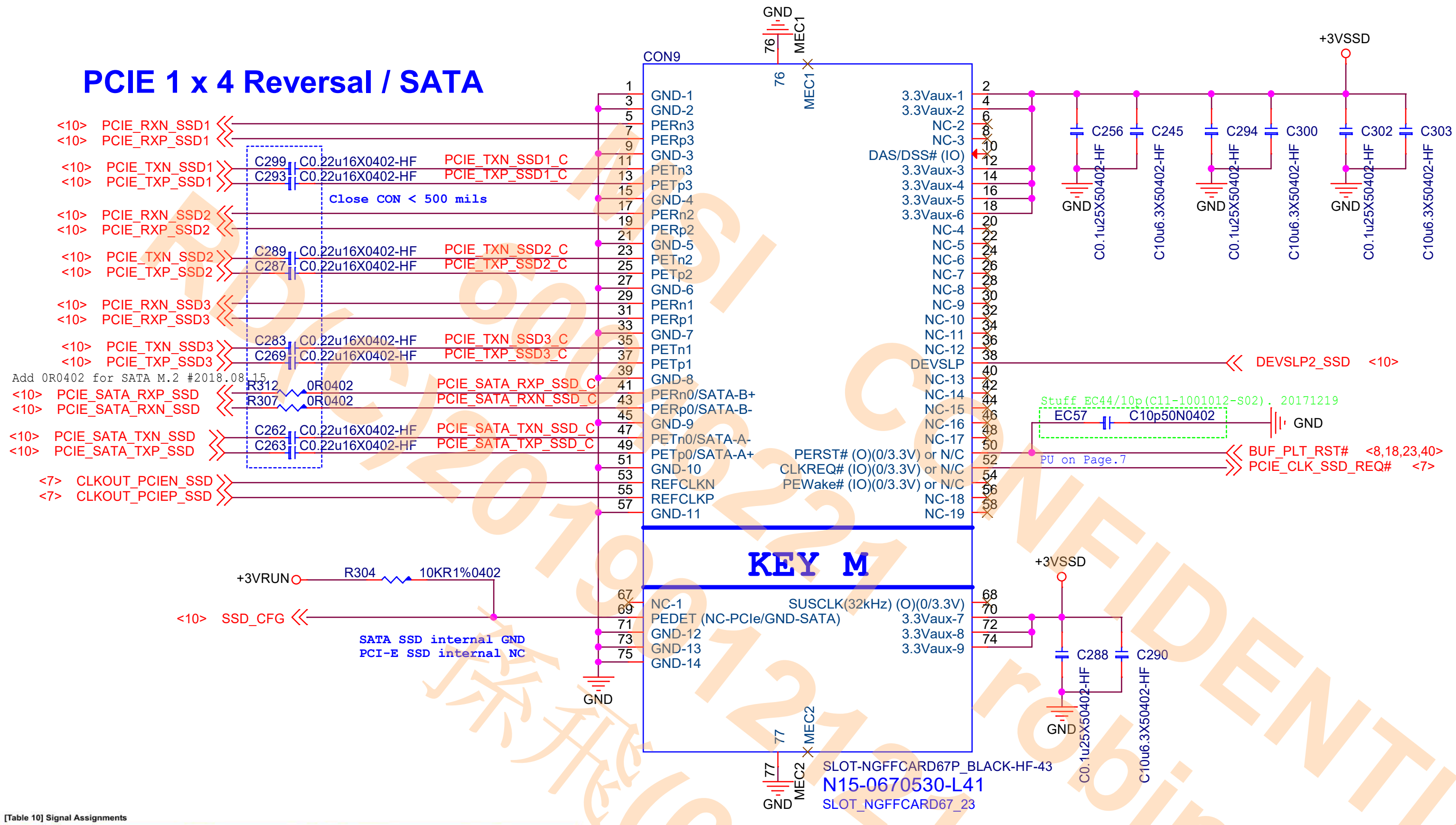
PCIE 1 x 4 Reversal / SATA

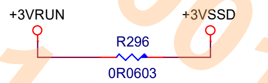


CON9
GND
76
MEC1
+3VSSD
<10> PCIE_RXN_SSD1
<10> PCIE_RXP_SSD1
<10> PCIE_TXN_SSD1
<10> PCIE_TXP_SSD1
C299 C0.22u16X0402-HF PCIE_TXN_SSD1_C
C293 C0.22u16X0402-HF PCIE_TXP_SSD1_C
Close CON < 500 mils
<10> PCIE_RXN_SSD2
<10> PCIE_RXP_SSD2
<10> PCIE_TXN_SSD2
<10> PCIE_TXP_SSD2
C289 C0.22u16X0402-HF PCIE_TXN_SSD2_C
C287 C0.22u16X0402-HF PCIE_TXP_SSD2_C
<10> PCIE_RXN_SSD3
<10> PCIE_RXP_SSD3
<10> PCIE_TXN_SSD3
<10> PCIE_TXP_SSD3
C283 C0.22u16X0402-HF PCIE_TXN_SSD3_C
C269 C0.22u16X0402-HF PCIE_TXP_SSD3_C
Add 0R0402 for SATA M.2 #2018.08.15
R312 0R0402 PCIE_SATA_RXP_SSD_C
R307 0R0402 PCIE_SATA_RXN_SSD_C
<10> PCIE_SATA_RXP_SSD
<10> PCIE_SATA_RXN_SSD
<10> PCIE_SATA_TXN_SSD
<10> PCIE_SATA_TXP_SSD
C262 C0.22u16X0402-HF PCIE_SATA_TXN_SSD_C
C263 C0.22u16X0402-HF PCIE_SATA_TXP_SSD_C
<7> CLKOUT_PCIEN_SSD
<7> CLKOUT_PCIEP_SSD
GND-1 GND-2 PERn3 PERp3 GND-3 PETn3 PETp3 GND-4 PERn2 PERp2 GND-5 PETn2 PETp2 GND-6 PERn1 PERp1 GND-7 PETn1 PETp1 GND-8 PERn0/SATA-B+ PERp0/SATA-B- GND-9 PETn0/SATA-A- PETp0/SATA-A+ GND-10 REFCLKN REFCLKP GND-11
3.3Vaux-1 3.3Vaux-2 NC-2 NC-3 DAS/DSS# (IO) 3.3Vaux-3 3.3Vaux-4 3.3Vaux-5 3.3Vaux-6 NC-4 NC-5 NC-6 NC-7 NC-8 NC-9 NC-10 NC-11 NC-12 DEVSLP NC-13 NC-14 NC-15 NC-16 NC-17
PERST# (O)(0/3.3V) or N/C
CLKREQ# (IO)(0/3.3V) or N/C
PEWake# (IO)(0/3.3V) or N/C
NC-18 NC-19
C256 C245 C294 C300 C302 C303
C0.1u25X50402-HF C10u6.3X50402-HF
DEVSLP2_SSD <10>
Stuff EC44/10p(C11-1001012-S02). 20171219
EC57 C10p50N0402 GND
PU on Page.7
BUF_PLT_RST# <8,18,23,40>
PCIE_CLK_SSD_REQ# <7>
KEY M
+3VRUN R304 10KR1%0402
<10> SSD_CFG
SATA SSD internal GND
PCI-E SSD internal NC
NC-1 PEDET (NC-PCIe/GND-SATA) GND-12 GND-13 GND-14
SUSCLK(32kHz) (O)(0/3.3V) 3.3Vaux-7 3.3Vaux-8 3.3Vaux-9
C288 C290
77 MEC2
SLOT-NGFFCARD67P_BLACK-HF-43
N15-0670530-L41
SLOT_NGFFCARD67_23

Pin	Signal	Signal	Pin
		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET (NC-PCIe/GND-SATA)	69
68	SUSCLK(32kHz) (O)(0/3.3V)	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWake# (IO)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)(0/3.3V)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I)(OD)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

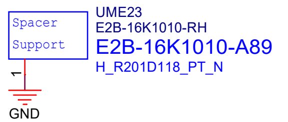
[Table 10] Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	N/C	N/C
9	GND	Return current path	10	LED1#[1)]	Device Active Signal (Refer to [Table 11])
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCIe TX	42	N/C	N/C
43	PETp0	PCIe TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCIe Reference Clock	56	Reserved for MFG_Data	N/C
57	GND	Return current path	58	Reserved for MFG_CLOCK	N/C
67	N/C	N/C	68	SUSCLK	N/C
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			



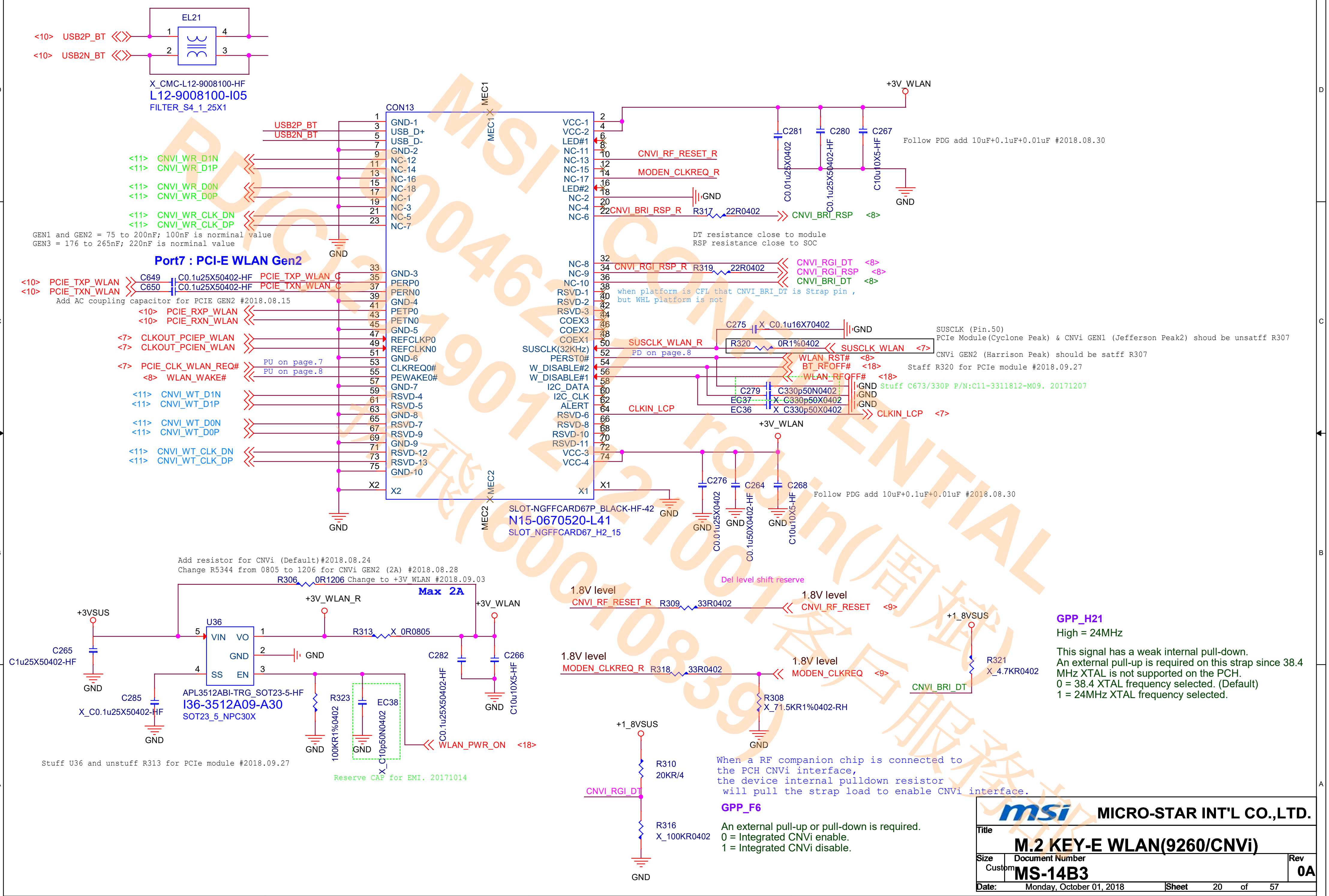
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLK+/ REFCLK-	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST#	O	PE-Reset is a functional reset to the card as defined by the PCIe Mini Card CEM specification	3.3V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates	3.3V
	WAKE#/OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3V

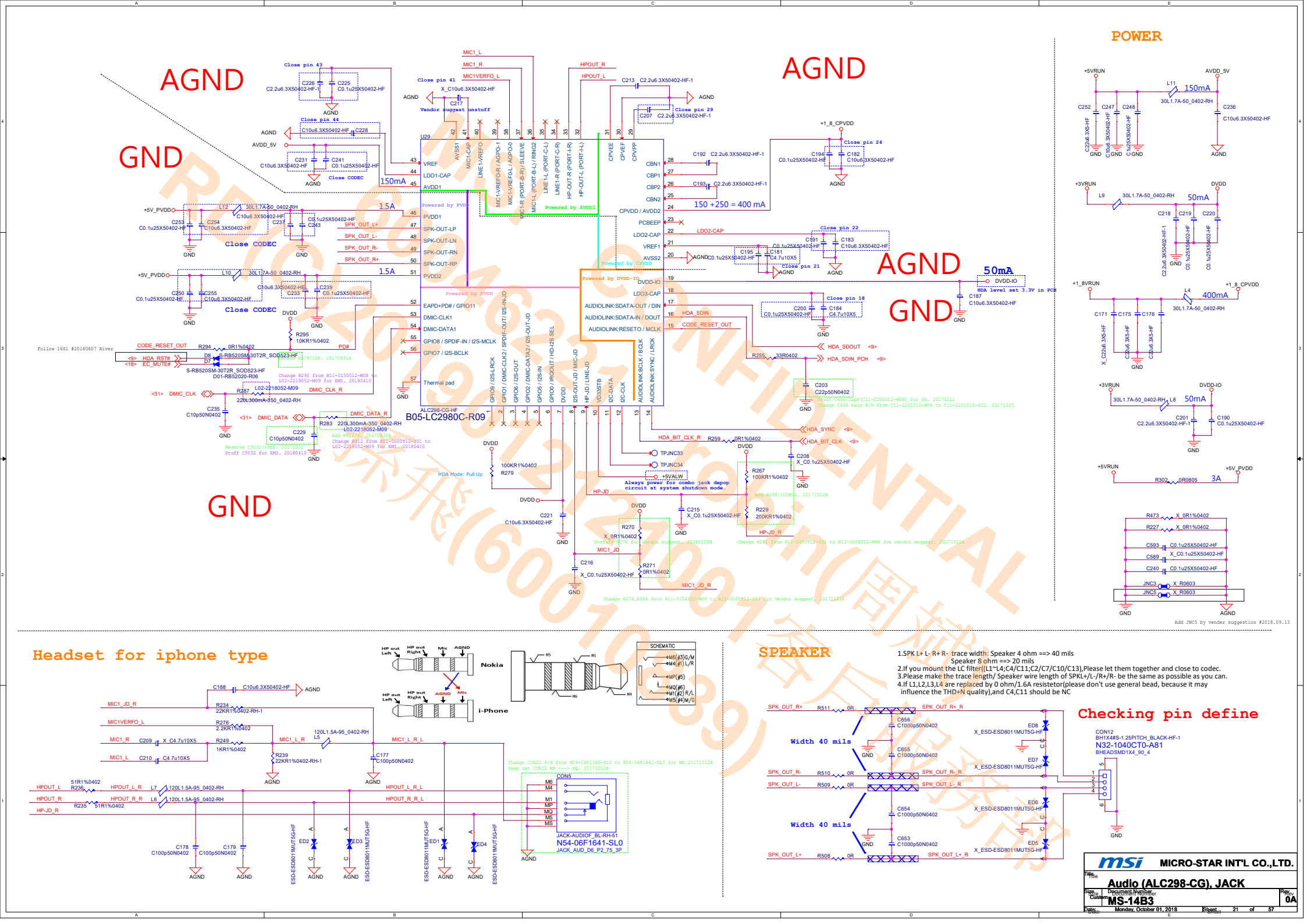
SSD STAND OFF



Add UME29 P/N:E2B-16K1010-A89 Footprint:H_R201D118_PT for ME.20171014
Change UME29 footprint to H_R201D118_PT_N for Layout. 20171030

Add CNVi function by PM request #2018.08.24




AGND
GND
AGND
GND
AGND
GND
B05-LC2980C-R09
ALC298-CG-HF
U29
POWER
Headset for iphone type
SPEAKER
Checking pin define
Width 40 mils
Width 40 mils
Nokia
i-Phone
JACK-AUDIOF_BL-RH-51
N54-06F1641-SL0
JACK_AUD_D6_P2_75_3P
MICRO-STAR INT'L CO.,LTD.
Audio (ALC298-CG), JACK
MS-14B3
Monday, October 01, 2018
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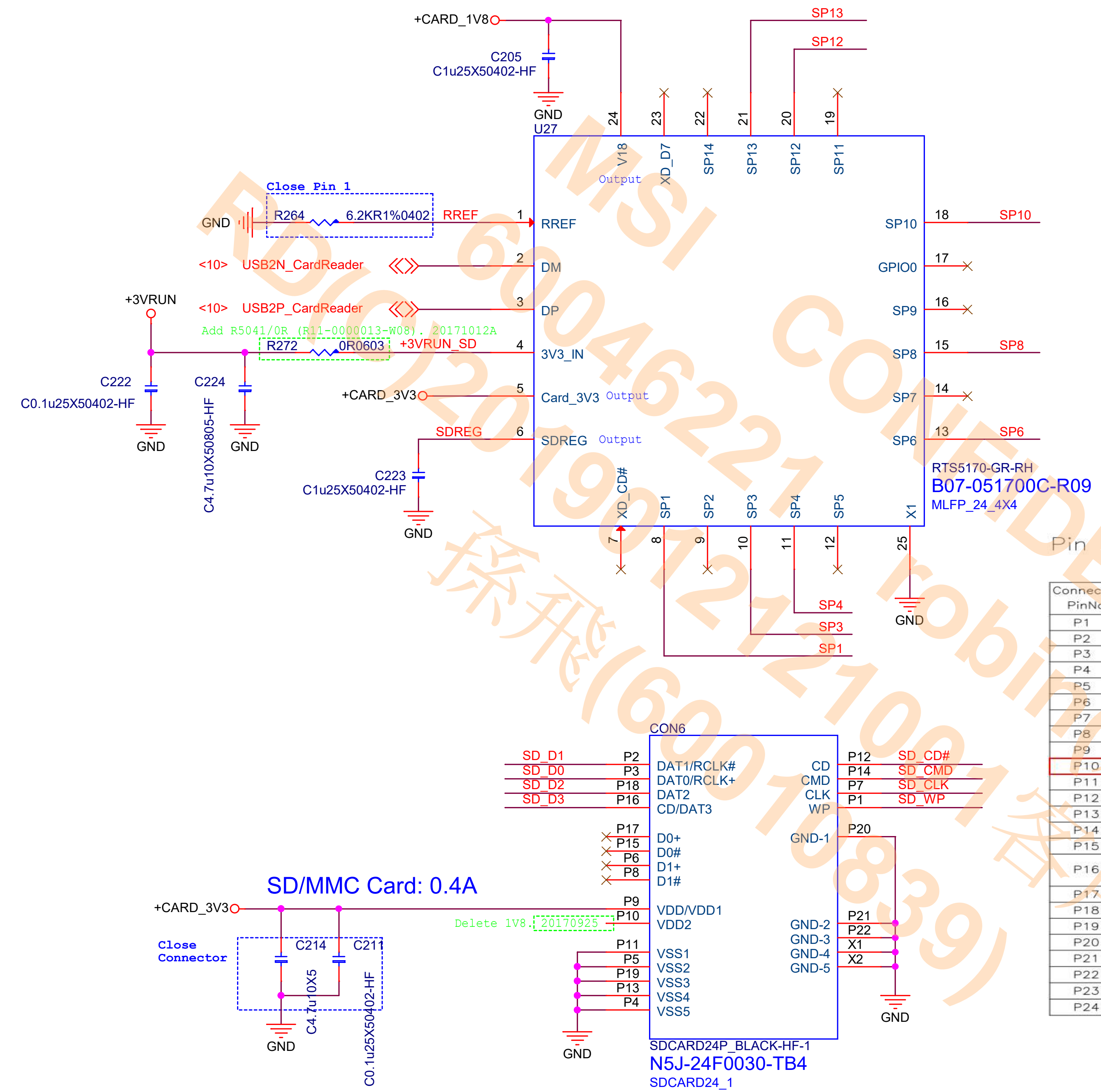
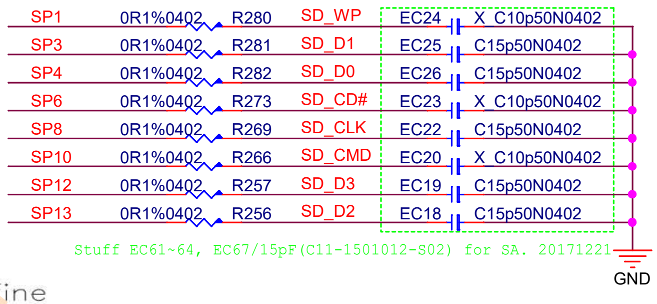
0A



+CARD_1V8
C205
C1u25X50402-HF
GND
U27
Close Pin 1
R264 6.2KR1%0402
RREF
<10> USB2N_CardReader
<10> USB2P_CardReader
+3VRUN
Add R5041/0R (R11-0000013-W08). 20171012A
R272 0R0603
+3VRUN_SD
C222
C0.1u25X50402-HF
C224
C4.7u10X50805-HF
+CARD_3V3
SDREG
C223
C1u25X50402-HF
V18
XD_D7
SP14
SP13
SP12
SP11
RREF
DM
DP
3V3_IN
Card_3V3 Output
SDREG Output
XD_CD#
SP1
SP2
SP3
SP4
SP5
X1
SP10
GPIO0
SP9
SP8
SP7
SP6
RTS5170-GR-RH
B07-051700C-R09
MLFP_24_4X4
SP13
SP12
SP10
SP8
SP6
SP4
SP3
SP1
CON6
SD_D1 SD_D0 SD_D2 SD_D3
DAT1/RCLK#
DAT0/RCLK+
DAT2
CD/DAT3
D0+ D0# D1+ D1#
VDD/VDD1
VDD2
VSS1 VSS2 VSS3 VSS4 VSS5
CD CMD CLK WP
GND-1 GND-2 GND-3 GND-4 GND-5
SD_CD# SD_CMD SD_CLK SD_WP
SD/MMC Card: 0.4A
+CARD_3V3
Delete 1V8. 20170925
Close Connector
C214 C211
C4.7u10X5
C0.1u25X50402-HF
SDCARD24P_BLACK-HF-1
N5J-24F0030-TB4
SDCARD24_1

	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

For EMI and Close to RTS5170



SP1 0R1%0402 R280 SD_WP EC24 X_C10p50N0402
SP3 0R1%0402 R281 SD_D1 EC25 C15p50N0402
SP4 0R1%0402 R282 SD_D0 EC26 C15p50N0402
SP6 0R1%0402 R273 SD_CD# EC23 X_C10p50N0402
SP8 0R1%0402 R269 SD_CLK EC22 C15p50N0402
SP10 0R1%0402 R266 SD_CMD EC20 X_C10p50N0402
SP12 0R1%0402 R257 SD_D3 EC19 C15p50N0402
SP13 0R1%0402 R256 SD_D2 EC18 C15p50N0402
GND

Stuff EC61~64, EC67/15pF(C11-1501012-S02) for SA. 20171221

Pin Define

Connector PinNo.	Specifications SD4.0 PinNo.	Specifications MMC PinNo.	SD Mode Name	Type	Description
P1			WP		
P2	P8		DAT1	I/O/PP	Data Line[Bit 1]
P3	P7	P7	DAT0	I/O/PP	Data Line[Bit 0]
P4	P17		—		Not Used(Connected to ground)
P5	P6	P6	VSS2	S	Supply voltage ground
P6	P16		—		Not Used
P7	P5	P5	CLK	I	Clock
P8	P15		—		Not Used
P9	P4	P4	VDD	S	Supply voltage
P10	P14		—		Not Used
P11	P3	P3	VSS1	S	Supply voltage ground
P12			CD		
P13	P13		—		Not Used(Connected to ground)
P14	P2	P2	CMD	PP	Command/Response
P15	P12		—		Not Used
P16	P1	P1	CD/DAT3	I/O/PP	Card Detect/ Data Line[Bit 3]
P17	P11		—		Not Used
P18	P9		DAT2	I/O/PP	Data Line[Bit 2]
P19	P10		—		Not Used(Connected to ground)
P20			GND		
P21			GND		
P22			GND		
P23			GND		
P24			GND		

MICRO-STAR INT'L CO.,LTD.

Title: **Card Reader (RTS5170)**

Size: Custom | Document Number: **MS-14B3** | Rev: 0A

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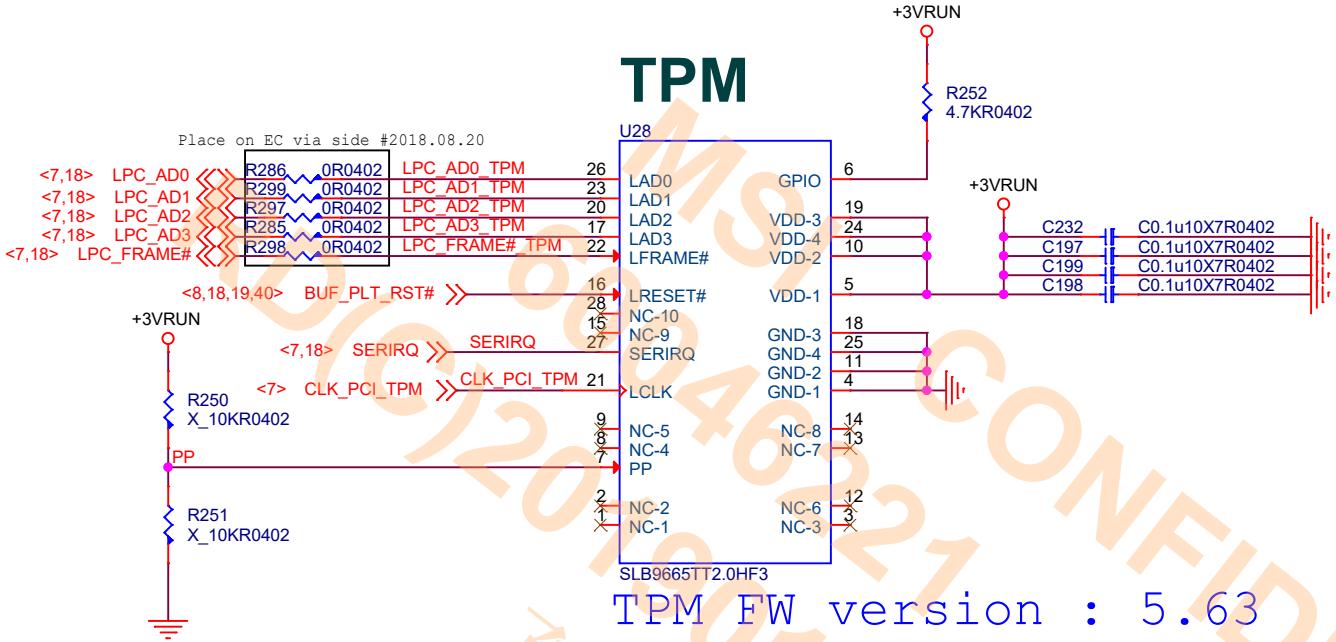
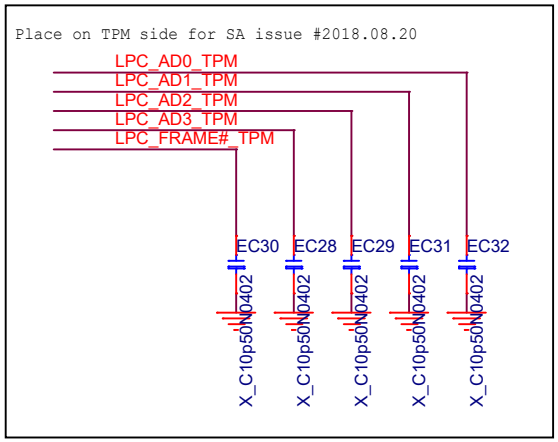
TPM





TPM FW version : 5.63

PP (Physical Presence) :
The TPM 2.0 device does not use this functionality

MICRO-STAR INT'L CO.,LTD.		
Title: TPM		
Size: A4	Document Number: MS-14B3	Rev: 0A
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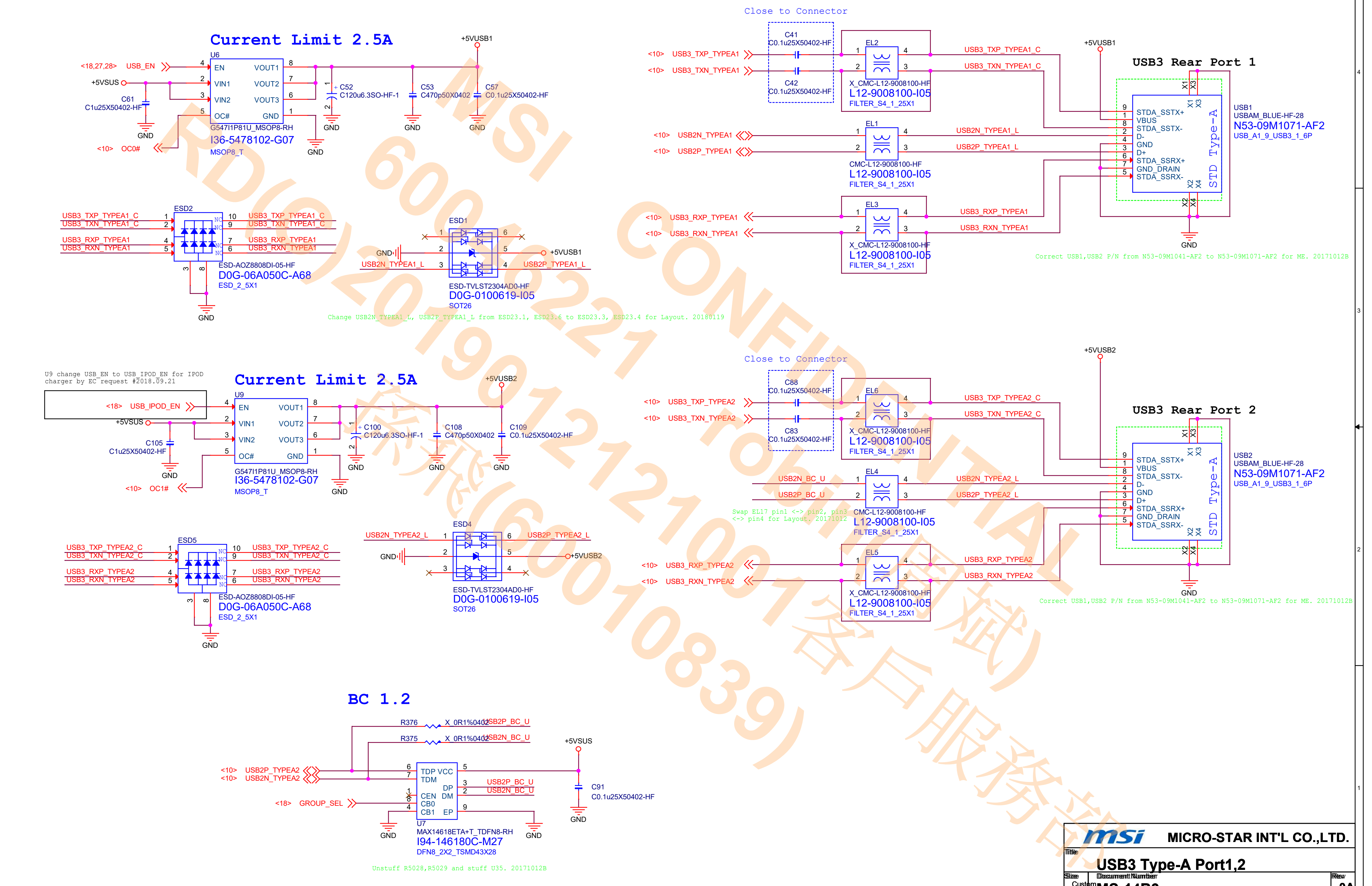
Current Limit 2.5A
U6
USB_EN
+5VSUS
C61 C1u25X50402-HF
EN VIN1 VIN2 OC#
VOUT1 VOUT2 VOUT3 GND
G547I1P81U_MSOP8-RH
I36-5478102-G07
MSOP8_T
OC0#
+5VUSB1
C52 C120u6.3SO-HF-1
C53 C470p50X0402
C57 C0.1u25X50402-HF
GND
ESD2
USB3_TXP_TYPEA1_C
USB3_TXN_TYPEA1_C
USB3_RXP_TYPEA1
USB3_RXN_TYPEA1
ESD-AOZ8808DI-05-HF
D0G-06A050C-A68
ESD_2_5X1
ESD1
USB2N_TYPEA1_L
USB2P_TYPEA1_L
ESD-TVLST2304AD0-HF
D0G-0100619-I05
SOT26
Change USB2N_TYPEA1_L, USB2P_TYPEA1_L from ESD23.1, ESD23.6 to ESD23.3, ESD23.4 for Layout. 20180119
Close to Connector
C41 C0.1u25X50402-HF
C42 C0.1u25X50402-HF
USB3_TXP_TYPEA1
USB3_TXN_TYPEA1
EL2
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
USB3_TXP_TYPEA1_C
USB3_TXN_TYPEA1_C
USB2N_TYPEA1
USB2P_TYPEA1
EL1
CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
USB2N_TYPEA1_L
USB2P_TYPEA1_L
USB3_RXP_TYPEA1
USB3_RXN_TYPEA1
EL3
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
USB3 Rear Port 1
STDA_SSTX+ VBUS STDA_SSTX- D- GND D+ STDA_SSRX+ GND_DRAIN STDA_SSRX-
STD Type-A
USB1
USBAM_BLUE-HF-28
N53-09M1071-AF2
USB_A1_9_USB3_1_6P
Correct USB1,USB2 P/N from N53-09M1041-AF2 to N53-09M1071-AF2 for ME. 20171012B
U9 change USB_EN to USB_IPOD_EN for IPOD charger by EC request #2018.09.21
Current Limit 2.5A
U9
USB_IPOD_EN
+5VSUS
C105 C1u25X50402-HF
G547I1P81U_MSOP8-RH
I36-5478102-G07
MSOP8_T
OC1#
+5VUSB2
C100 C120u6.3SO-HF-1
C108 C470p50X0402
C109 C0.1u25X50402-HF
ESD5
USB3_TXP_TYPEA2_C
USB3_TXN_TYPEA2_C
USB3_RXP_TYPEA2
USB3_RXN_TYPEA2
ESD-AOZ8808DI-05-HF
D0G-06A050C-A68
ESD_2_5X1
ESD4
USB2N_TYPEA2_L
USB2P_TYPEA2_L
ESD-TVLST2304AD0-HF
D0G-0100619-I05
SOT26
Close to Connector
C88 C0.1u25X50402-HF
C83 C0.1u25X50402-HF
USB3_TXP_TYPEA2
USB3_TXN_TYPEA2
EL6
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
USB3_TXP_TYPEA2_C
USB3_TXN_TYPEA2_C
USB2N_BC_U
USB2P_BC_U
EL4
CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
USB2N_TYPEA2_L
USB2P_TYPEA2_L
Swap EL17 pin1 <-> pin2, pin3 <-> pin4 for Layout. 20171012
USB3_RXP_TYPEA2
USB3_RXN_TYPEA2
EL5
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
USB3 Rear Port 2
USB2
USBAM_BLUE-HF-28
N53-09M1071-AF2
USB_A1_9_USB3_1_6P
Correct USB1,USB2 P/N from N53-09M1041-AF2 to N53-09M1071-AF2 for ME. 20171012B
BC 1.2
R376 X_0R1%0402 USB2P_BC_U
R375 X_0R1%0402 USB2N_BC_U
USB2P_TYPEA2
USB2N_TYPEA2
GROUP_SEL
TDP VCC TDM DP DM CEN CB0 CB1 EP
U7
MAX14618ETA+T_TDFN8-RH
I94-146180C-M27
DFN8_2X2_TSMD43X28
+5VSUS
C91 C0.1u25X50402-HF
Unstuff R5028,R5029 and stuff U35. 20171012B

MICRO-STAR INT'L CO.,LTD.

Title: USB3 Type-A Port1,2

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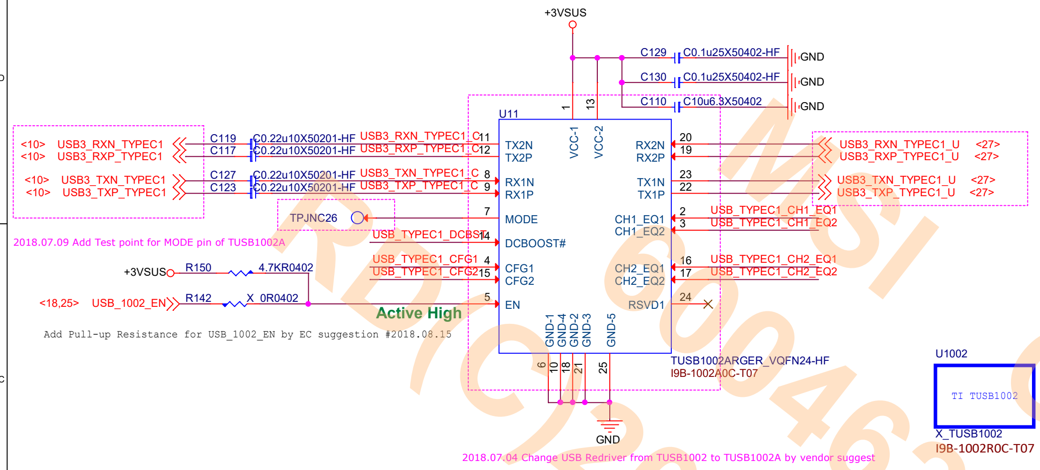
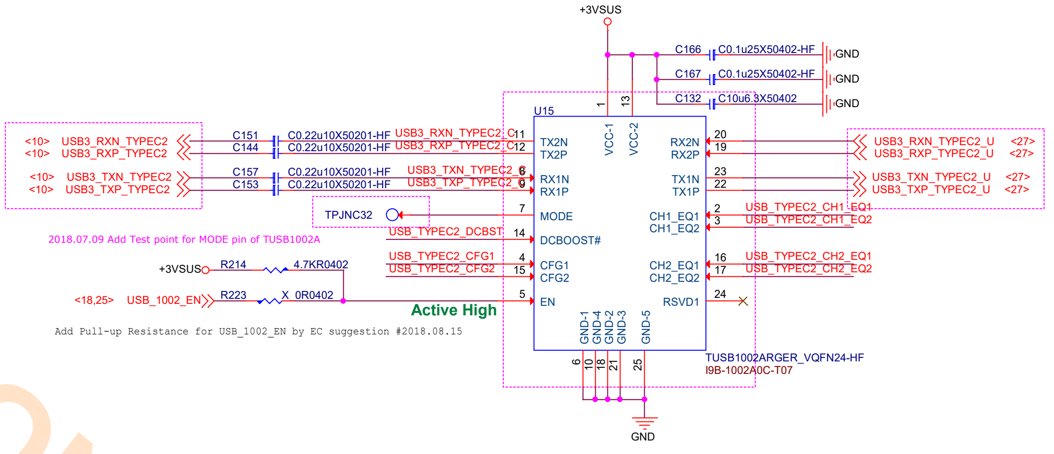
Reference 13H1

USB3.0 TYPE-C Port 3 Redriver TOP



+3VSUS
C129 C0.1u25X50402-HF GND
C130 C0.1u25X50402-HF GND
C110 C10u6.3X50402 GND
U11
<10> USB3_RXN_TYPEC1
<10> USB3_RXP_TYPEC1
<10> USB3_TXN_TYPEC1
<10> USB3_TXP_TYPEC1
C119 C0.22u10X50201-HF USB3_RXN_TYPEC1_C
C117 C0.22u10X50201-HF USB3_RXP_TYPEC1_C
C127 C0.22u10X50201-HF USB3_TXN_TYPEC1_C
C123 C0.22u10X50201-HF USB3_TXP_TYPEC1_C
TX2N TX2P RX1N RX1P MODE DCBOOST# CFG1 CFG2 EN
VCC-1 VCC-2
RX2N RX2P TX1N TX1P CH1_EQ1 CH1_EQ2 CH2_EQ1 CH2_EQ2 RSVD1
GND-1 GND-4 GND-2 GND-3 GND-5
USB3_RXN_TYPEC1_U <27>
USB3_RXP_TYPEC1_U <27>
USB3_TXN_TYPEC1_U <27>
USB3_TXP_TYPEC1_U <27>
USB_TYPEC1_CH1_EQ1
USB_TYPEC1_CH1_EQ2
USB_TYPEC1_CH2_EQ1
USB_TYPEC1_CH2_EQ2
TPJNC26
USB_TYPEC1_DCBST
2018.07.09 Add Test point for MODE pin of TUSB1002A
USB_TYPEC1_CFG1
USB_TYPEC1_CFG2
+3VSUS R150 4.7KR0402
<18,25> USB_1002_EN R142 X_0R0402
Active High
Add Pull-up Resistance for USB_1002_EN by EC suggestion #2018.08.15
TUSB1002ARGER_VQFN24-HF
I9B-1002A0C-T07
GND
U1002
TI TUSB1002
X_TUSB1002
I9B-1002R0C-T07
2018.07.04 Change USB Redriver from TUSB1002 to TUSB1002A by vendor suggest

USB3.0 TYPE-C Port 3 Redriver BOT



+3VSUS
C166 C0.1u25X50402-HF GND
C167 C0.1u25X50402-HF GND
C132 C10u6.3X50402 GND
U15
<10> USB3_RXN_TYPEC2
<10> USB3_RXP_TYPEC2
<10> USB3_TXN_TYPEC2
<10> USB3_TXP_TYPEC2
C151 C0.22u10X50201-HF USB3_RXN_TYPEC2_C
C144 C0.22u10X50201-HF USB3_RXP_TYPEC2_C
C157 C0.22u10X50201-HF USB3_TXN_TYPEC2_C
C153 C0.22u10X50201-HF USB3_TXP_TYPEC2_C
USB3_RXN_TYPEC2_U <27>
USB3_RXP_TYPEC2_U <27>
USB3_TXN_TYPEC2_U <27>
USB3_TXP_TYPEC2_U <27>
USB_TYPEC2_CH1_EQ1
USB_TYPEC2_CH1_EQ2
USB_TYPEC2_CH2_EQ1
USB_TYPEC2_CH2_EQ2
TPJNC32
USB_TYPEC2_DCBST
2018.07.09 Add Test point for MODE pin of TUSB1002A
USB_TYPEC2_CFG1
USB_TYPEC2_CFG2
+3VSUS R214 4.7KR0402
<18,25> USB_1002_EN R223 X_0R0402
Active High
Add Pull-up Resistance for USB_1002_EN by EC suggestion #2018.08.15
TUSB1002ARGER_VQFN24-HF
I9B-1002A0C-T07
GND

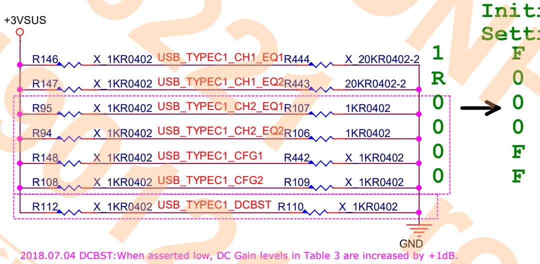
TUSB1002A

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

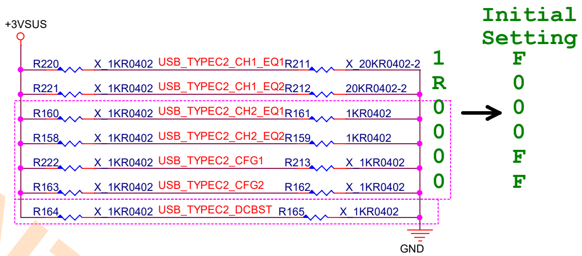
Table 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting

EQ SETTING #	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5GHz / 5 GHz (dB)
1	0	0	1.0 / 3.6
2	0	R	2.1 / 5.5
3	0	F	3.0 / 6.8
4	0	1	4.0 / 8.1
5	R	0	4.6 / 9.0
6	R	R	5.5 / 10.0
7	R	F	6.2 / 10.8
8	R	1	6.9 / 11.6
9	F	0	7.3 / 11.9
10	F	R	7.9 / 12.6
11	F	F	8.4 / 13.1
12	F	1	9.0 / 13.7
13	1	0	9.4 / 14.1
14	1	R	9.9 / 14.6
15	1	F	10.3 / 14.9
16	1	1	10.7 / 15.3



+3VSUS
R146 X_1KR0402 USB_TYPEC1_CH1_EQ1 R444 X_20KR0402-2
R147 X_1KR0402 USB_TYPEC1_CH1_EQ2 R443 20KR0402-2
R95 X_1KR0402 USB_TYPEC1_CH2_EQ1 R107 1KR0402
R94 X_1KR0402 USB_TYPEC1_CH2_EQ2 R106 1KR0402
R148 X_1KR0402 USB_TYPEC1_CFG1 R442 X_1KR0402
R108 X_1KR0402 USB_TYPEC1_CFG2 R109 X_1KR0402
R112 X_1KR0402 USB_TYPEC1_DCBST R110 X_1KR0402
GND
1 R 0 0 0 0
Initial Setting
F 0 0 0 F F

2018.07.04 DCBST:When asserted low, DC Gain levels in Table 3 are increased by +1dB.
2018.07.17 Change CFG1/CFG2 to 900mV(0,0) by vendor suggest
2018.07.17 Change CH2_EQ[1:2] = 0,0 because TUSB1002A will place cllosed to connector by vendor suggest
Change USB3.1 Redriver to initial EQ/VOD setting by vender suggestion #2018.09.14



+3VSUS
R220 X_1KR0402 USB_TYPEC2_CH1_EQ1 R211 X_20KR0402-2
R221 X_1KR0402 USB_TYPEC2_CH1_EQ2 R212 20KR0402-2
R160 X_1KR0402 USB_TYPEC2_CH2_EQ1 R161 1KR0402
R158 X_1KR0402 USB_TYPEC2_CH2_EQ2 R159 1KR0402
R222 X_1KR0402 USB_TYPEC2_CFG1 R213 X_1KR0402
R163 X_1KR0402 USB_TYPEC2_CFG2 R162 X_1KR0402
R164 X_1KR0402 USB_TYPEC2_DCBST R165 X_1KR0402
GND
1 R 0 0 0 0
Initial Setting
F 0 0 0 F F

Change USB3.1 Redriver to initial EQ/VOD setting by vender suggestion #2018.09.14

Table 3. VOD Linear Range and DC Gain

SETTING #	CFG1 PIN LEVEL	CFG2 PIN LEVEL	CH1 DC GAIN (dB)	CH2 DC GAIN (dB)	CH1 V_{OD} LINEAR RANGE (mVpp)	CH2 V_{OD} LINEAR RANGE (mVpp)
1	0	0	+1	0	900	900
2	0	R	0	+1	900	900
3	0	F	0	0	900	900
4	0	1	+1	+1	900	900
5	R	0	0	0	1000	1000
6	R	R	+1	0	1000	1000
7	R	F	0	-1	1000	1000
8	R	1	+2	+2	1000	1000
9	F	0	-1	-1	1200	1200
10	F	R	+2	+2	1200	1200
11	F	F	0	0	1200	1200
12	F	1	+1	+1	1200	1200
13	1	0	+2	0	1200	1200
14	1	R	0	+2	1200	1200
15	1	F	0	+1	1200	1200
16	1	1	+1	0	1200	1200

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Title: BLANK

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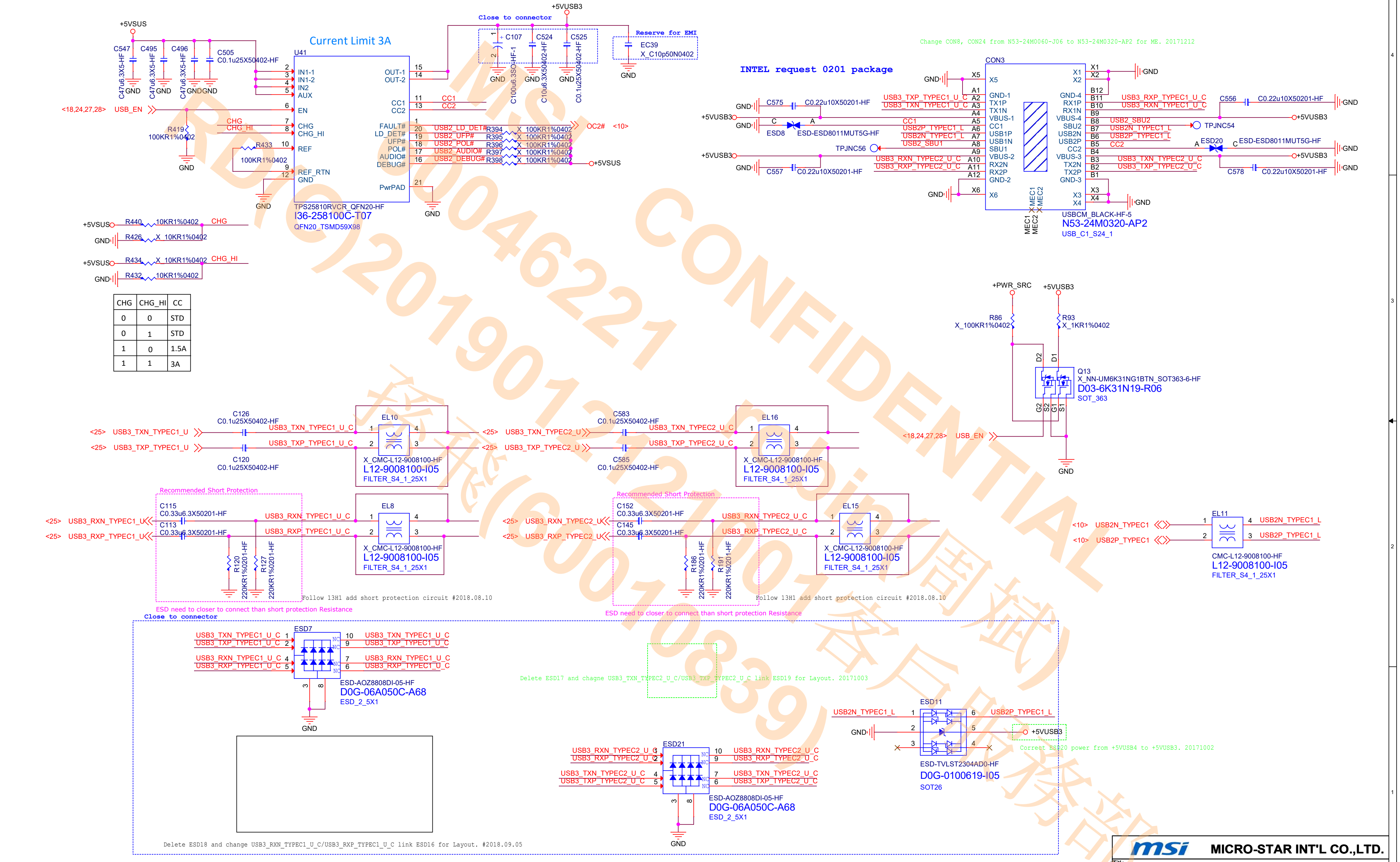

Current Limit 3A
U41
TPS25810RVCR_QFN20-HF
I36-258100C-T07
QFN20_TSMD59X98
IN1-1 IN1-2 IN2 AUX EN CHG CHG_HI REF REF_RTN GND
OUT-1 OUT-2 CC1 CC2 FAULT# LD_DET# UFP# POL# AUDIO# DEBUG# PwrPAD
+5VSUS
C547 C47u6.3X5-HF
C495 C47u6.3X5-HF
C496 C47u6.3X5-HF
C505 C0.1u25X50402-HF
<18,24,27,28> USB_EN
R419 100KR1%0402
R433 100KR1%0402
USB2_LD_DET# USB2_UFP# USB2_POL# USB2_AUDIO# USB2_DEBUG#
R394 X_100KR1%0402
R395 X_100KR1%0402
R396 X_100KR1%0402
R397 X_100KR1%0402
R398 X_100KR1%0402
OC2# <10>
+5VUSB3
Close to connector
C107 C100u6.3SO-HF-1
C524 C10u6.3X50402-HF
C525 C0.1u25X50402-HF
Reserve for EMI
EC39 X_C10p50N0402
R440 10KR1%0402 CHG
R426 X_10KR1%0402
R434 X_10KR1%0402 CHG_HI
R432 10KR1%0402
Change CON8, CON24 from N53-24M0060-J06 to N53-24M0320-AP2 for ME. 20171212
INTEL request 0201 package
CON3
USBCM_BLACK-HF-5
N53-24M0320-AP2
USB_C1_S24_1
GND-1 TX1P TX1N VBUS-1 CC1 USB1P USB1N SBU1 VBUS-2 RX2N RX2P GND-2
GND-4 RX1P RX1N VBUS-4 SBU2 USB2N USB2P CC2 VBUS-3 TX2N TX2P GND-3
USB3_TXP_TYPEC1_U_C USB3_TXN_TYPEC1_U_C USB3_RXP_TYPEC1_U_C USB3_RXN_TYPEC1_U_C
USB3_RXN_TYPEC2_U_C USB3_RXP_TYPEC2_U_C USB3_TXN_TYPEC2_U_C USB3_TXP_TYPEC2_U_C
USB2P_TYPEC1_L USB2N_TYPEC1_L USB2_SBU1 USB2_SBU2
C575 C0.22u10X50201-HF
C556 C0.22u10X50201-HF
C557 C0.22u10X50201-HF
C578 C0.22u10X50201-HF
ESD8 ESD-ESD8011MUT5G-HF
ESD20 ESD-ESD8011MUT5G-HF
TPJNC54 TPJNC56
+PWR_SRC
R86 X_100KR1%0402
R93 X_1KR1%0402
Q13 X_NN-UM6K31NG1BTN_SOT363-6-HF
D03-6K31N19-R06
SOT_363
<25> USB3_TXN_TYPEC1_U
<25> USB3_TXP_TYPEC1_U
C126 C0.1u25X50402-HF
C120 C0.1u25X50402-HF
EL10 X_CMC-L12-9008100-HF L12-9008100-I05 FILTER_S4_1_25X1
<25> USB3_TXN_TYPEC2_U
<25> USB3_TXP_TYPEC2_U
C583 C0.1u25X50402-HF
C585 C0.1u25X50402-HF
EL16 X_CMC-L12-9008100-HF L12-9008100-I05 FILTER_S4_1_25X1
Recommended Short Protection
<25> USB3_RXN_TYPEC1_U
<25> USB3_RXP_TYPEC1_U
C115 C0.33u6.3X50201-HF
C113 C0.33u6.3X50201-HF
R120 220KR1%0201-HF
R127 220KR1%0201-HF
EL8 X_CMC-L12-9008100-HF L12-9008100-I05 FILTER_S4_1_25X1
<25> USB3_RXN_TYPEC2_U
<25> USB3_RXP_TYPEC2_U
C152 C0.33u6.3X50201-HF
C145 C0.33u6.3X50201-HF
R186 220KR1%0201-HF
R191 220KR1%0201-HF
EL15 X_CMC-L12-9008100-HF L12-9008100-I05 FILTER_S4_1_25X1
<10> USB2N_TYPEC1
<10> USB2P_TYPEC1
EL11 CMC-L12-9008100-HF L12-9008100-I05 FILTER_S4_1_25X1
Follow 13H1 add short protection circuit #2018.08.10
ESD need to closer to connect than short protection Resistance
Close to connector
ESD7 ESD-AOZ8808DI-05-HF D0G-06A050C-A68 ESD_2_5X1
Delete ESD17 and chagne USB3_TXN_TYPEC2_U_C/USB3_TXP_TYPEC2_U_C link ESD19 for Layout. 20171003
ESD11 ESD-TVLST2304AD0-HF D0G-0100619-I05 SOT26
Correct ESD20 power from +5VUSB4 to +5VUSB3. 20171002
ESD21 ESD-AOZ8808DI-05-HF D0G-06A050C-A68 ESD_2_5X1
Delete ESD18 and change USB3_RXN_TYPEC1_U_C/USB3_RXP_TYPEC1_U_C link ESD16 for Layout. #2018.09.05

CHG	CHG_HI	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

MICRO-STAR INT'L CO.,LTD.

Title: USB Type-C (TPS25810) Port3

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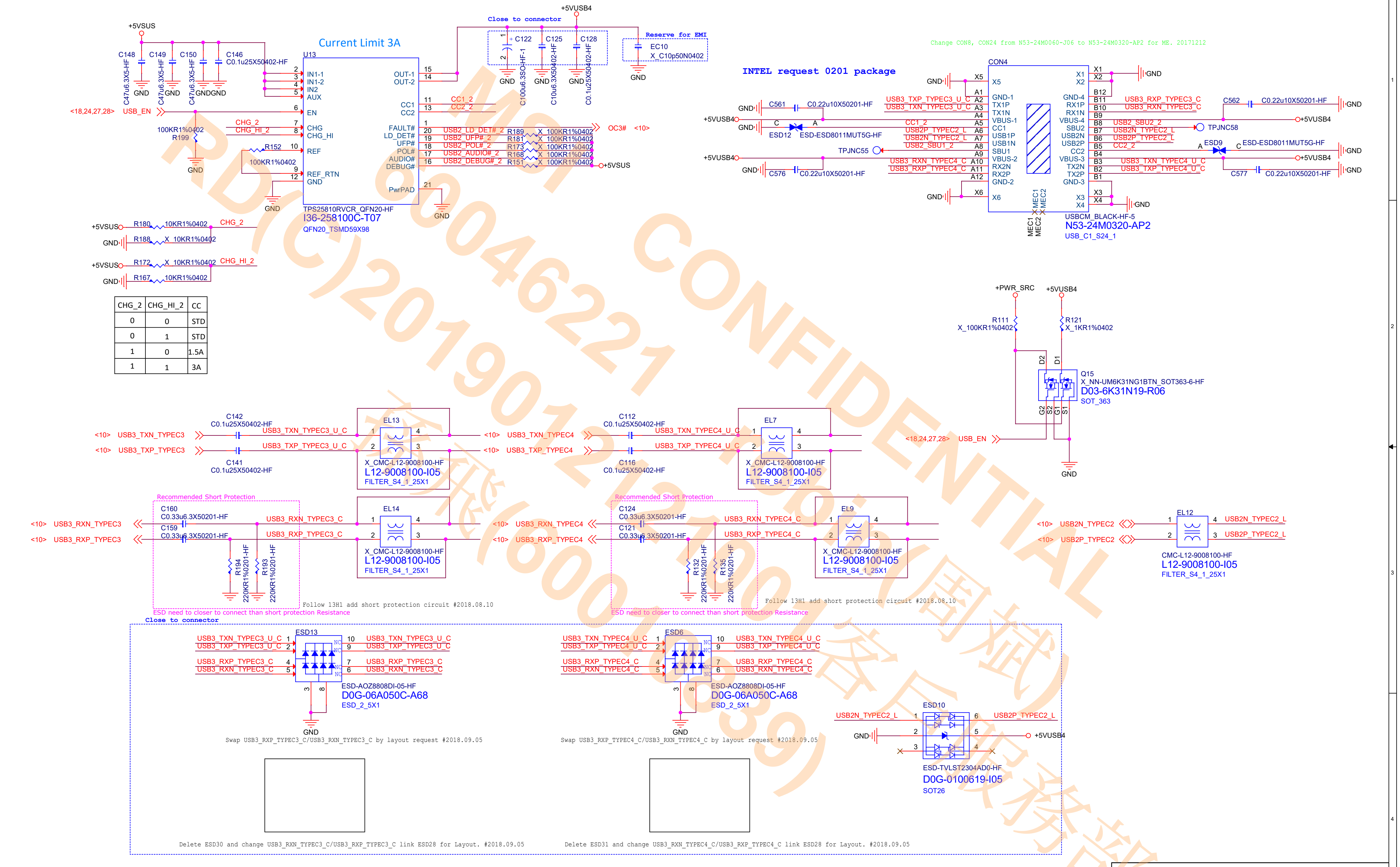

Current Limit 3A
U13
TPS25810RVCR_QFN20-HF
I36-258100C-T07
QFN20_TSMD59X98
+5VSUS
+5VUSB4
Close to connector
Reserve for EMI
EC10
X_C10p50N0402
C148 C149 C150 C146
C0.1u25X50402-HF
C122 C125 C128
IN1-1 IN1-2 IN2 AUX EN CHG CHG_HI REF REF_RTN GND
OUT-1 OUT-2 CC1 CC2 FAULT# LD_DET# UFP# POL# AUDIO# DEBUG# PwrPAD
<18,24,27,28> USB_EN
OC3# <10>
Change CON8, CON24 from N53-24M0060-J06 to N53-24M0320-AP2 for ME. 20171212
INTEL request 0201 package
CON4
USBCM_BLACK-HF-5
N53-24M0320-AP2
USB_C1_S24_1
ESD12 ESD-ESD8011MUT5G-HF
ESD9 ESD-ESD8011MUT5G-HF
TPJNC55 TPJNC58
+PWR_SRC
Q15
X_NN-UM6K31NG1BTN_SOT363-6-HF
D03-6K31N19-R06
SOT_363
EL13 EL7 EL14 EL9 EL12
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1
<10> USB3_TXN_TYPEC3
<10> USB3_TXP_TYPEC3
<10> USB3_TXN_TYPEC4
<10> USB3_TXP_TYPEC4
<10> USB3_RXN_TYPEC3
<10> USB3_RXP_TYPEC3
<10> USB3_RXN_TYPEC4
<10> USB3_RXP_TYPEC4
<10> USB2N_TYPEC2
<10> USB2P_TYPEC2
Recommended Short Protection
ESD need to closer to connect than short protection Resistance
Follow 13H1 add short protection circuit #2018.08.10
Close to connector
ESD13 ESD6
ESD-AOZ8808DI-05-HF
D0G-06A050C-A68
ESD_2_5X1
Swap USB3_RXP_TYPEC3_C/USB3_RXN_TYPEC3_C by layout request #2018.09.05
Swap USB3_RXP_TYPEC4_C/USB3_RXN_TYPEC4_C by layout request #2018.09.05
ESD10
ESD-TVLST2304AD0-HF
D0G-0100619-I05
SOT26
Delete ESD30 and change USB3_RXN_TYPEC3_C/USB3_RXP_TYPEC3_C link ESD28 for Layout. #2018.09.05
Delete ESD31 and change USB3_RXN_TYPEC4_C/USB3_RXP_TYPEC4_C link ESD28 for Layout. #2018.09.05

CHG_2	CHG_HI_2	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

MICRO-STAR INT'L CO.,LTD.

Title: USB Type-C(TPS25810) Port4

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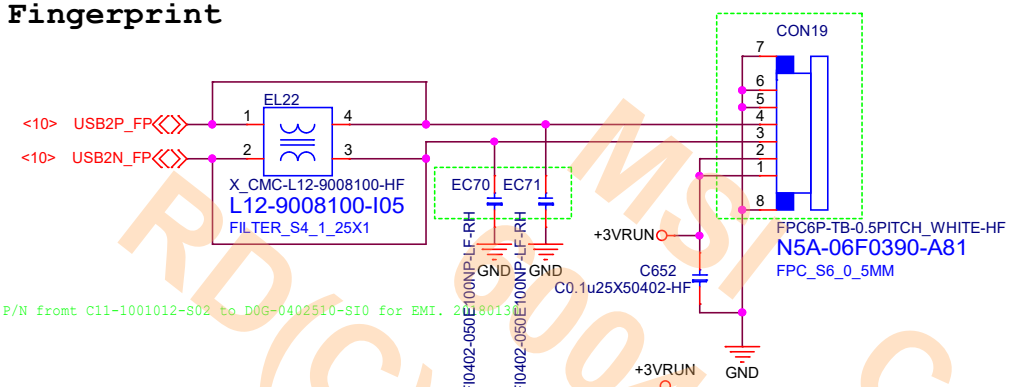
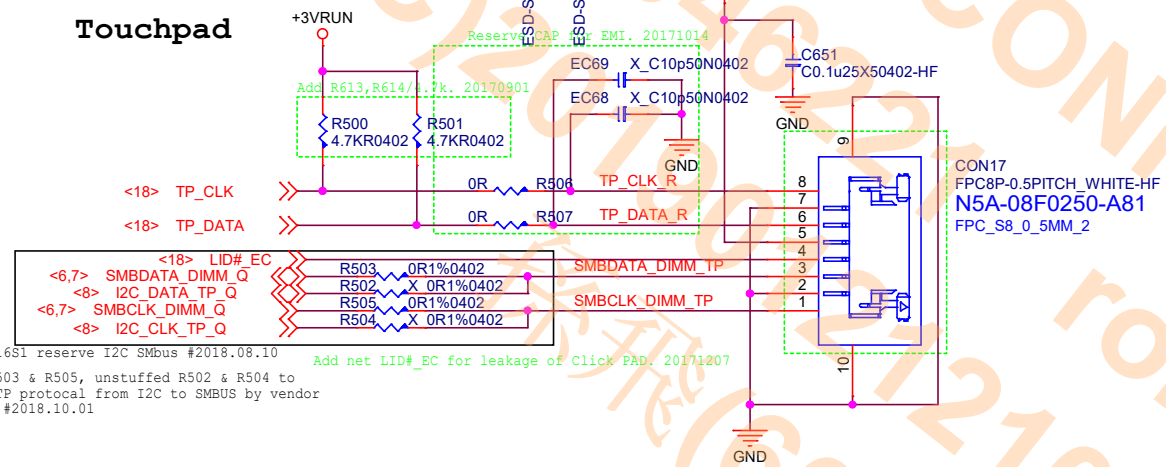
Change CON16 P/N from N5A-06F0420-A81 to N5A-06F0390-A81 for ME. 20180115
Mirror CON16 vertical for FFC. 20171017

Fingerprint



Change EC2,EC3 P/N fromt C11-1001012-S02 to D0G-0402510-SI0 for EMI. 20180131

Touchpad



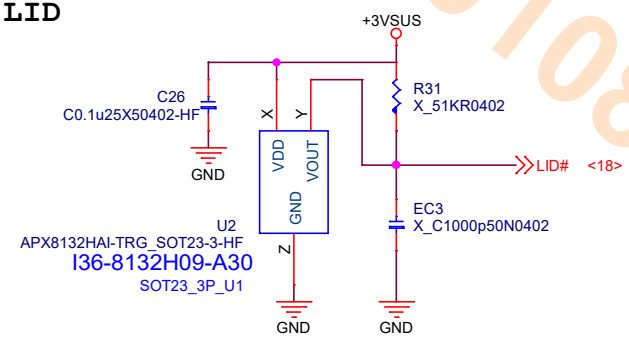
Follow 16S1 reserve I2C SMbus #2018.08.10

Stuff R503 & R505, unstuffed R502 & R504 to change TP protocal from I2C to SMBUS by vendor request #2018.10.01

Add net LID#_EC for leakage of Click PAD. 20171207

Change CON17 P/N from N5A-08F0160-A81 to N5A-08F0300-A81 for ME.20171004
Change CON17 P/N from N5A-08F0300-A81 to N5A-08F0250-A81 for ME. 20180115

LID



J2 Pin Assignments and Definitions

Pin Number	Pin Name	Description
1	VDD	Power Supply
2	VDD	Power Supply
3	USB D-	USB D-
4	USB D+	USB D+
5	GND	Ground
6	GND	Ground

J1 (Host Interface) Pin Assignments and Definitions

Pin Number	Pin Name	Description
1	SMB_CLK	SMbus Clock
2	GND	Ground
3	SMB_DAT	SMbus Data
4	LID Close	Disable when lid is closed(1)
5	VDD	Power Supply
6	PS2_DAT	PS2 Data
7	GND	Ground
8	PS2_CLK	PS2 Clock

(1) Disable Touchpad when lid is closed (system sleep), to prevent from LCD noise coupling to touchpad and cause sensor malfunction

MICRO-STAR INT'L CO.,LTD.

Title: Click,FingerPrint,LID

Size: Custom | Document Number: MS-14B3 | Rev: 0A

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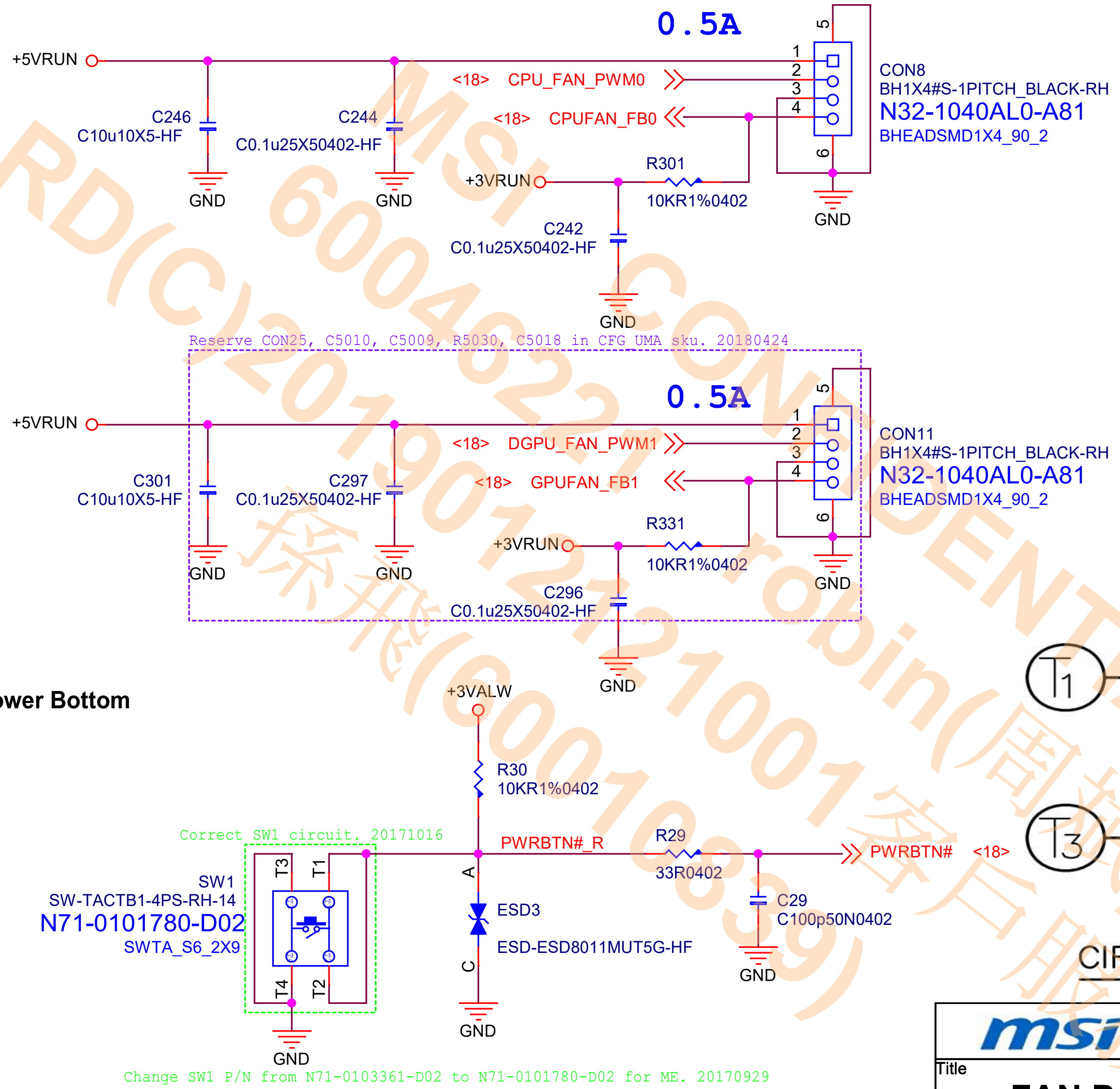
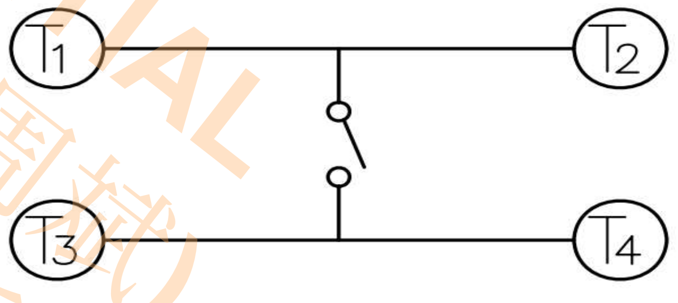
FAN



+5VRUN
C246
C10u10X5-HF
C244
C0.1u25X50402-HF
GND
0.5A
<18> CPU_FAN_PWM0
<18> CPUFAN_FB0
+3VRUN
R301
10KR1%0402
C242
C0.1u25X50402-HF
CON8
BH1X4#S-1PITCH_BLACK-RH
N32-1040AL0-A81
BHEADSMD1X4_90_2
Reserve CON25, C5010, C5009, R5030, C5018 in CFG_UMA sku. 20180424
C301
C10u10X5-HF
C297
C0.1u25X50402-HF
<18> DGPU_FAN_PWM1
<18> GPUFAN_FB1
R331
10KR1%0402
C296
C0.1u25X50402-HF
CON11
BH1X4#S-1PITCH_BLACK-RH
N32-1040AL0-A81
BHEADSMD1X4_90_2
Power Bottom
+3VALW
R30
10KR1%0402
Correct SW1 circuit. 20171016
PWRBTN#_R
R29
33R0402
PWRBTN# <18>
SW1
SW-TACTB1-4PS-RH-14
N71-0101780-D02
SWTA_S6_2X9
ESD3
ESD-ESD8011MUT5G-HF
C29
C100p50N0402
Change SW1 P/N from N71-0103361-D02 to N71-0101780-D02 for ME. 20170929

PIN NO.	LEAD COLOR
1	RED(+)
2	BLUE(PWM)
3	BLACK(-)
4	YELLOW(FG)



CIRCUIT DIAGRAM

MICRO-STAR INT'L CO.,LTD.

Title: **FAN,Power SW**

Size: Custom | Document Number: **MS-14B3** | Rev: **0A**

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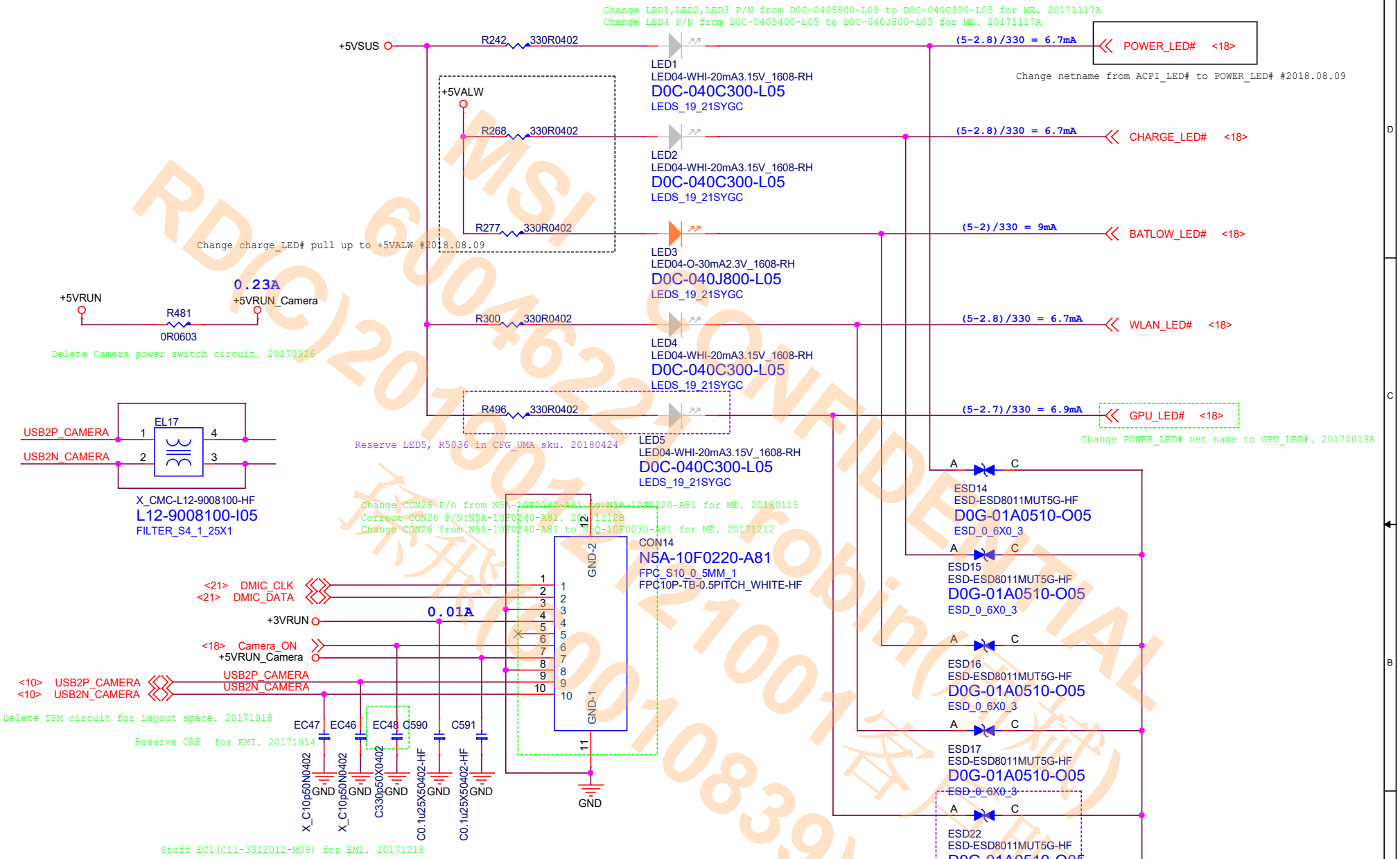

Pin Description							
Pin No.	Name	Pin Type	Function Des.	Pin No.	Name	Pin Type	Function Des.
1	DMIC_CLK	CLK	D-MIC clock	6	EN	Power	EN_3.3V
2	DMIC_DATA	Data	D-MIC data	7	VCC	Power	Cam_5V
3	GND	GND	GND	8	GND	GND	GND
4	MIC_VCC	Power	MIC_3.3V	9	D+	Data	USB_DP
5	NC	NC	NC	10	D-	Data	USB_DM

MICRO-STAR INT'L CO.,LTD.

Title: LED / Camera

Size: Custom | Document Number: MS-14B3 | Rev: 0A

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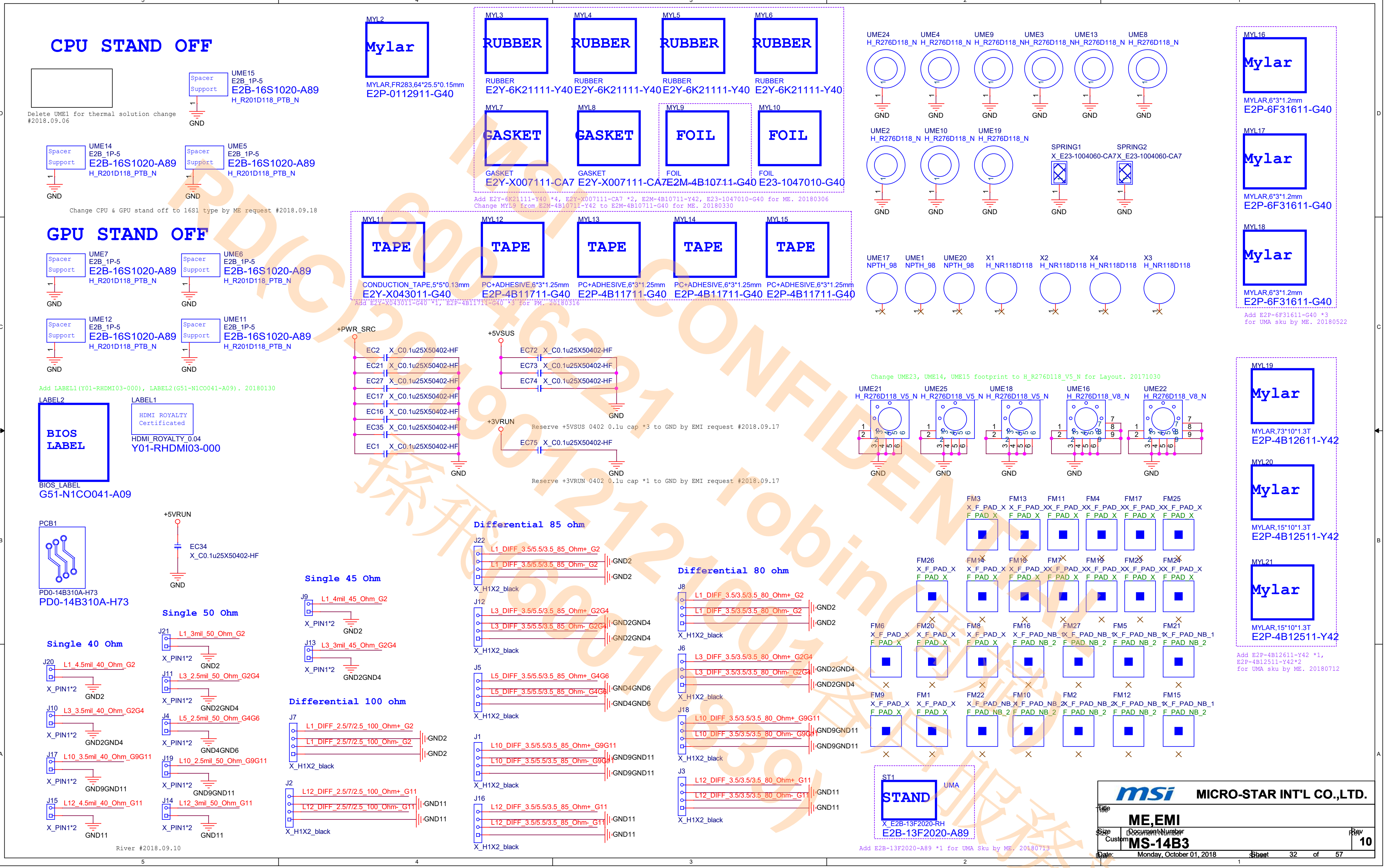

CPU STAND OFF
Delete UME1 for thermal solution change #2018.09.06
UME15 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N
UME14 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N
UME5 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N
Change CPU & GPU stand off to 16S1 type by ME request #2018.09.18
GPU STAND OFF
UME7 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N
UME6 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N
UME12 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N
UME11 E2B_1P-5 E2B-16S1020-A89 H_R201D118_PTB_N
Add LABEL1(Y01-RHDMI03-000), LABEL2(G51-N1C0041-A09). 20180130
LABEL2 BIOS LABEL BIOS_LABEL G51-N1CO041-A09
LABEL1 HDMI ROYALTY Certificated HDMI_ROYALTY_0.04 Y01-RHDMI03-000
PCB1 PD0-14B310A-H73 PD0-14B310A-H73
+5VRUN EC34 X_C0.1u25X50402-HF
MYL2 Mylar MYLAR,FR283,64*25.5*0.15mm E2P-0112911-G40
MYL3 RUBBER E2Y-6K21111-Y40
MYL4 RUBBER E2Y-6K21111-Y40
MYL5 RUBBER E2Y-6K21111-Y40
MYL6 RUBBER E2Y-6K21111-Y40
MYL7 GASKET E2Y-X007111-CA7
MYL8 GASKET E2Y-X007111-CA7
MYL9 FOIL E2M-4B10711-G40
MYL10 FOIL E23-1047010-G40
Add E2Y-6K21111-Y40 *4, E2Y-X007111-CA7 *2, E2M-4B10711-Y42, E23-1047010-G40 for ME. 20180306
Change MYL9 from E2M-4B10711-Y42 to E2M-4B10711-G40 for ME. 20180330
MYL11 TAPE CONDUCTION_TAPE,5*5*0.13mm E2Y-X043011-G40
MYL12 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40
MYL13 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40
MYL14 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40
MYL15 TAPE PC+ADHESIVE,6*3*1.25mm E2P-4B11711-G40
Add E2Y-X043011-G40 *1, E2P-4B11711-G40 *3 for PM. 20180316
+PWR_SRC EC2 EC21 EC27 EC17 EC16 EC35 EC1 X_C0.1u25X50402-HF
+5VSUS EC72 EC73 EC74 X_C0.1u25X50402-HF
Reserve +5VSUS 0402 0.1u cap *3 to GND by EMI request #2018.09.17
+3VRUN EC75 X_C0.1u25X50402-HF
Reserve +3VRUN 0402 0.1u cap *1 to GND by EMI request #2018.09.17
UME24 UME4 UME9 UME3 UME13 UME8 H_R276D118_N H_R276D118_NH
UME2 UME10 UME19 H_R276D118_N
SPRING1 SPRING2 X_E23-1004060-CA7
UME17 UME1 UME20 NPTH_98
X1 X2 X4 X3 H_NR118D118
Change UME23, UME14, UME15 footprint to H_R276D118_V5_N for Layout. 20171030
UME21 UME25 UME18 H_R276D118_V5_N
UME16 UME22 H_R276D118_V8_N
MYL16 MYL17 MYL18 Mylar MYLAR,6*3*1.2mm E2P-6F31611-G40
Add E2P-6F31611-G40 *3 for UMA sku by ME. 20180522
MYL19 Mylar MYLAR,73*10*1.3T E2P-4B12611-Y42
MYL20 MYL21 Mylar MYLAR,15*10*1.3T E2P-4B12511-Y42
Add E2P-4B12611-Y42 *1, E2P-4B12511-Y42*2 for UMA sku by ME. 20180712
FM3 FM13 FM11 FM4 FM17 FM25 FM26 FM14 FM18 FM7 FM19 FM23 FM24 FM6 FM20 FM8 FM16 FM27 FM5 FM21 FM9 FM1 FM22 FM10 FM2 FM12 FM15 X_F_PAD_X X_F_PAD_NB_1 F_PAD_NB_2
Single 40 Ohm
J20 L1_4.5mil_40_Ohm_G2 · J10 L3_3.5mil_40_Ohm_G2G4 · J17 L10_3.5mil_40_Ohm_G9G11 · J15 L12_4.5mil_40_Ohm_G11 X_PIN1*2
Single 50 Ohm
J21 L1_3mil_50_Ohm_G2 · J11 L3_2.5mil_50_Ohm_G2G4 · J4 L5_2.5mil_50_Ohm_G4G6 · J19 L10_2.5mil_50_Ohm_G9G11 · J14 L12_3mil_50_Ohm_G11
Single 45 Ohm
J9 L1_4mil_45_Ohm_G2 · J13 L3_3mil_45_Ohm_G2G4
Differential 100 ohm
J7 L1_DIFF_2.5/7/2.5_100_Ohm+_G2 L1_DIFF_2.5/7/2.5_100_Ohm-_G2 · J2 L12_DIFF_2.5/7/2.5_100_Ohm+_G11 L12_DIFF_2.5/7/2.5_100_Ohm-_G11 X_H1X2_black
Differential 85 ohm
J22 L1_DIFF_3.5/5.5/3.5_85_Ohm+_G2 · J12 L3_DIFF_3.5/5.5/3.5_85_Ohm+_G2G4 · J5 L5_DIFF_3.5/5.5/3.5_85_Ohm+_G4G6 · J1 L10_DIFF_3.5/5.5/3.5_85_Ohm+_G9G11 · J16 L12_DIFF_3.5/5.5/3.5_85_Ohm+_G11
Differential 80 ohm
J8 L1_DIFF_3.5/3.5/3.5_80_Ohm+_G2 · J6 L3_DIFF_3.5/3.5/3.5_80_Ohm+_G2G4 · J18 L10_DIFF_3.5/3.5/3.5_80_Ohm+_G9G11 · J3 L12_DIFF_3.5/3.5/3.5_80_Ohm+_G11
ST1 STAND UMA X_E2B-13F2020-RH E2B-13F2020-A89
Add E2B-13F2020-A89 *1 for UMA Sku by ME. 20180713
River #2018.09.10
MICRO-STAR INT'L CO.,LTD.
Title ME,EMI
Size Custom Document Number MS-14B3 Rev 10
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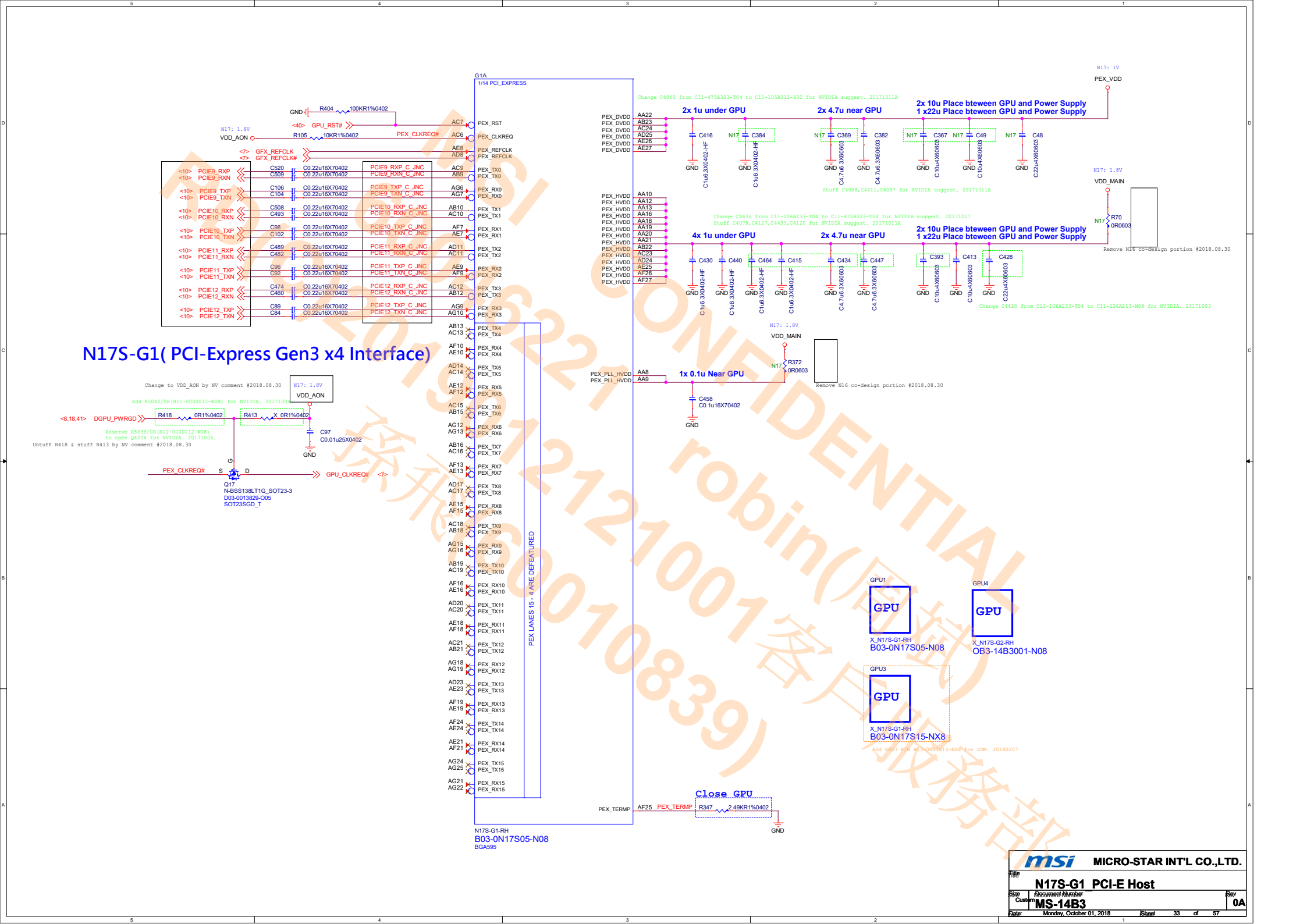
N17S-G1(PCI-Express Gen3 x4 Interface)
G1A
1/14 PCI_EXPRESS
PEX LANES 15 - 4 ARE DEFEATURED
N17S-G1-RH
B03-0N17S05-N08
BGA595
2x 1u under GPU
2x 4.7u near GPU
2x 10u Place bteween GPU and Power Supply
1 x22u Place bteween GPU and Power Supply
4x 1u under GPU
1x 0.1u Near GPU
PEX_VDD
VDD_MAIN
VDD_AON
Close GPU
GPU1
GPU4
GPU3
X_N17S-G1-RH
B03-0N17S05-N08
X_N17S-G2-RH
OB3-14B3001-N08
X_N17S-G1-RH
B03-0N17S15-NX8
MICRO-STAR INT'L CO.,LTD.
N17S-G1_PCI-E Host
MS-14B3
0A
Monday, October 01, 2018
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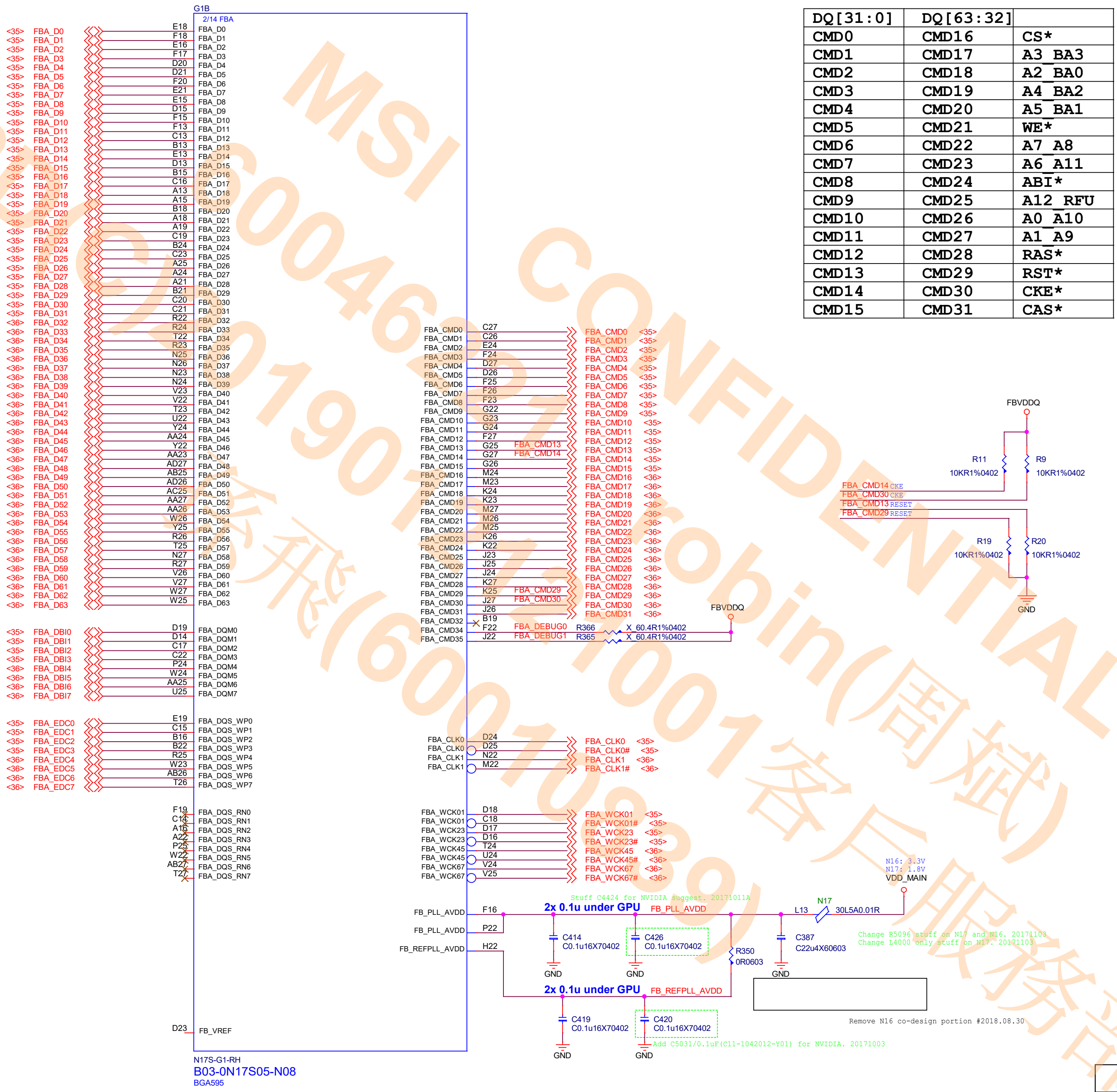
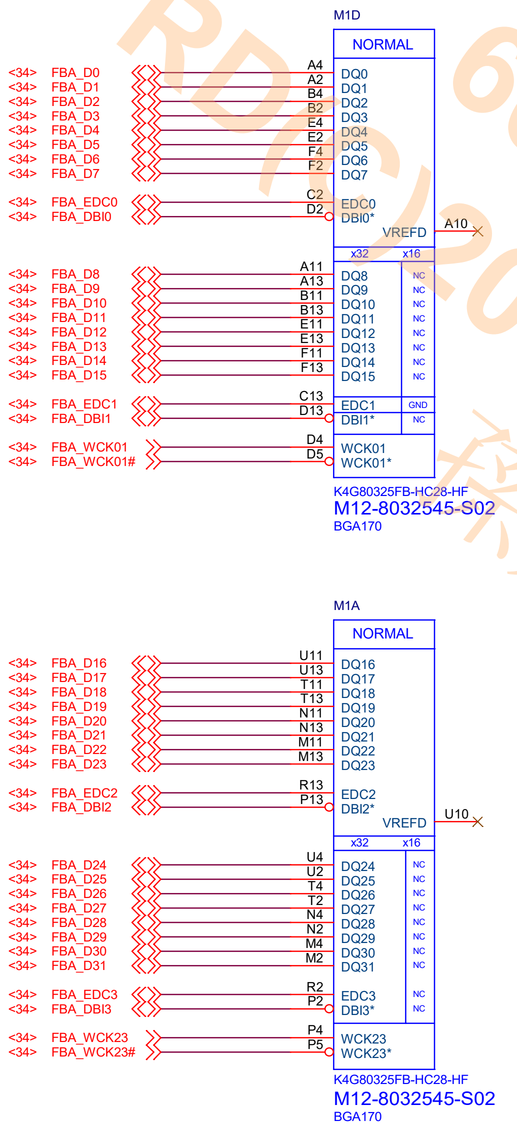
N17S-G1(Frame Buffer Interface)

GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



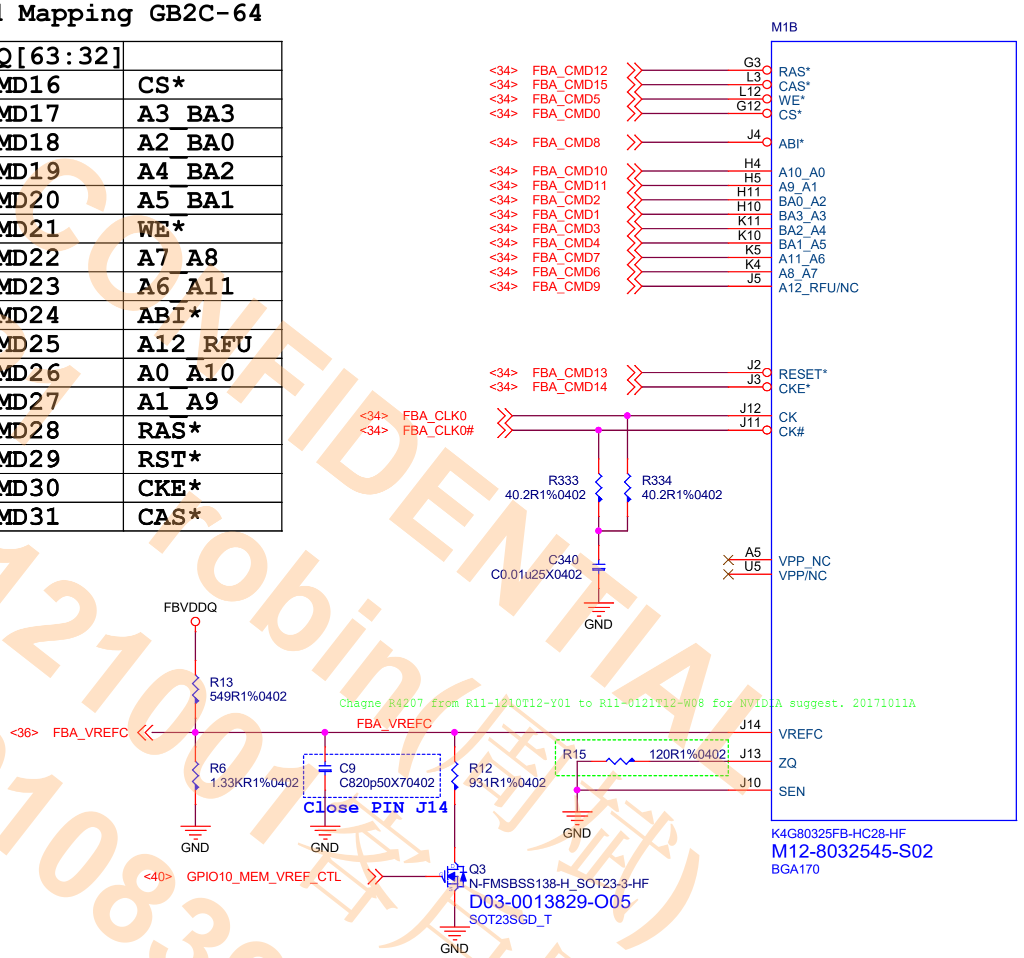
N17S-G1_GDDR5 Frame A-1



M1D
NORMAL
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7
FBA_EDC0 FBA_DBI0
VREFD A10
FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15
FBA_EDC1 FBA_DBI1
FBA_WCK01 FBA_WCK01#
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170
M1A
NORMAL
FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23
FBA_EDC2 FBA_DBI2
VREFD U10
FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31
FBA_EDC3 FBA_DBI3
FBA_WCK23 FBA_WCK23#
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170

GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



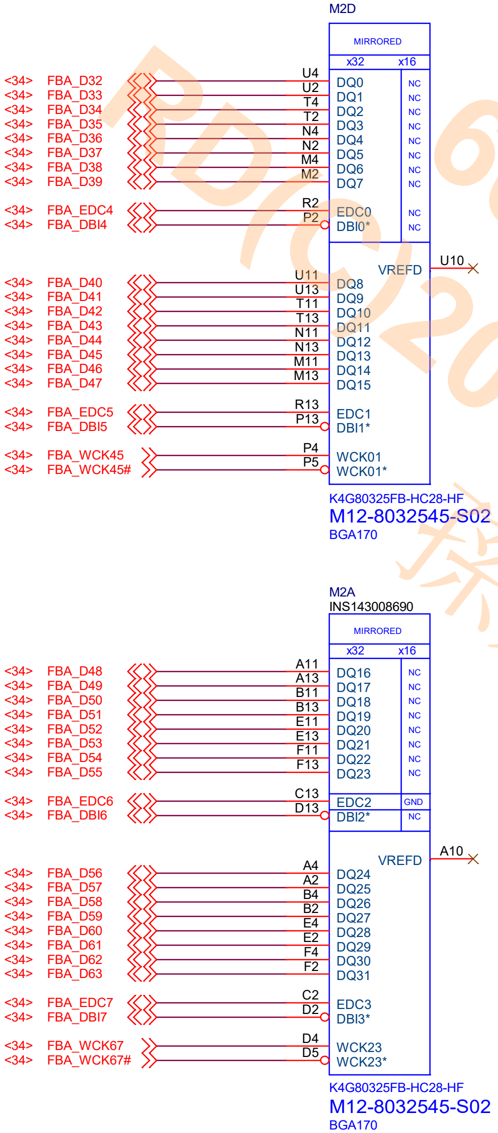
M1B
FBA_CMD12 FBA_CMD15 FBA_CMD5 FBA_CMD0 FBA_CMD8
FBA_CMD10 FBA_CMD11 FBA_CMD2 FBA_CMD1 FBA_CMD3 FBA_CMD4 FBA_CMD7 FBA_CMD6 FBA_CMD9
RAS* CAS* WE* CS* ABI* A10_A0 A9_A1 BA0_A2 BA3_A3 BA2_A4 BA1_A5 A11_A6 A8_A7 A12_RFU/NC
FBA_CMD13 FBA_CMD14 RESET* CKE*
FBA_CLK0 FBA_CLK0# CK CK#
R333 40.2R1%0402
R334 40.2R1%0402
C340 C0.01u25X0402
VPP_NC VPP/NC
FBVDDQ
R13 549R1%0402
Chagne R4207 from R11-1210T12-Y01 to R11-0121T12-W08 for NVIDIA suggest. 20171011A
FBA_VREFC VREFC ZQ SEN
R6 1.33KR1%0402
C9 C820p50X70402
Close PIN J14
R12 931R1%0402
R15 120R1%0402
GPIO10_MEM_VREF_CTL
Q3 N-FMSBSS138-H_SOT23-3-HF
D03-0013829-O05
SOT23SGD_T
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170
GND

X_SAMSUNG/K4G80325FB-HC25
M12-8032535-S02

X_HYNIX/H5GC8H24AJR-R2C
M12-5GC8HB5-H23

GDDR5 SGRAM,8G(256Mx32bit)

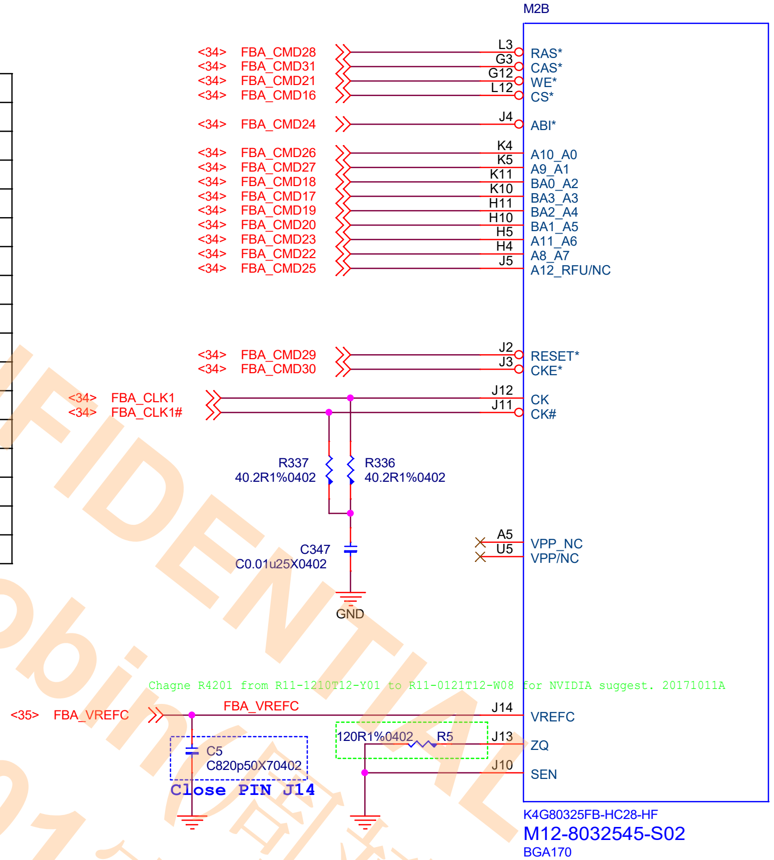
N17S-G1_GDDR5 Frame A-2



M2D
MIRRORED
x32 x16
<34> FBA_D32 U4 DQ0 NC
<34> FBA_D33 U2 DQ1 NC
<34> FBA_D34 T4 DQ2 NC
<34> FBA_D35 T2 DQ3 NC
<34> FBA_D36 N4 DQ4 NC
<34> FBA_D37 N2 DQ5 NC
<34> FBA_D38 M4 DQ6 NC
<34> FBA_D39 M2 DQ7 NC
<34> FBA_EDC4 R2 EDC0 NC
<34> FBA_DBI4 P2 DBI0* NC
VREFD U10
<34> FBA_D40 U11 DQ8
<34> FBA_D41 U13 DQ9
<34> FBA_D42 T11 DQ10
<34> FBA_D43 T13 DQ11
<34> FBA_D44 N11 DQ12
<34> FBA_D45 N13 DQ13
<34> FBA_D46 M11 DQ14
<34> FBA_D47 M13 DQ15
<34> FBA_EDC5 R13 EDC1
<34> FBA_DBI5 P13 DBI1*
<34> FBA_WCK45 P4 WCK01
<34> FBA_WCK45# P5 WCK01*
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170
M2A
INS143008690
MIRRORED
x32 x16
<34> FBA_D48 A11 DQ16 NC
<34> FBA_D49 A13 DQ17 NC
<34> FBA_D50 B11 DQ18 NC
<34> FBA_D51 B13 DQ19 NC
<34> FBA_D52 E11 DQ20 NC
<34> FBA_D53 E13 DQ21 NC
<34> FBA_D54 F11 DQ22 NC
<34> FBA_D55 F13 DQ23 NC
<34> FBA_EDC6 C13 EDC2 GND
<34> FBA_DBI6 D13 DBI2* NC
VREFD A10
<34> FBA_D56 A4 DQ24
<34> FBA_D57 A2 DQ25
<34> FBA_D58 B4 DQ26
<34> FBA_D59 B2 DQ27
<34> FBA_D60 E4 DQ28
<34> FBA_D61 E2 DQ29
<34> FBA_D62 F4 DQ30
<34> FBA_D63 F2 DQ31
<34> FBA_EDC7 C2 EDC3
<34> FBA_DBI7 D2 DBI3*
<34> FBA_WCK67 D4 WCK23
<34> FBA_WCK67# D5 WCK23*
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170

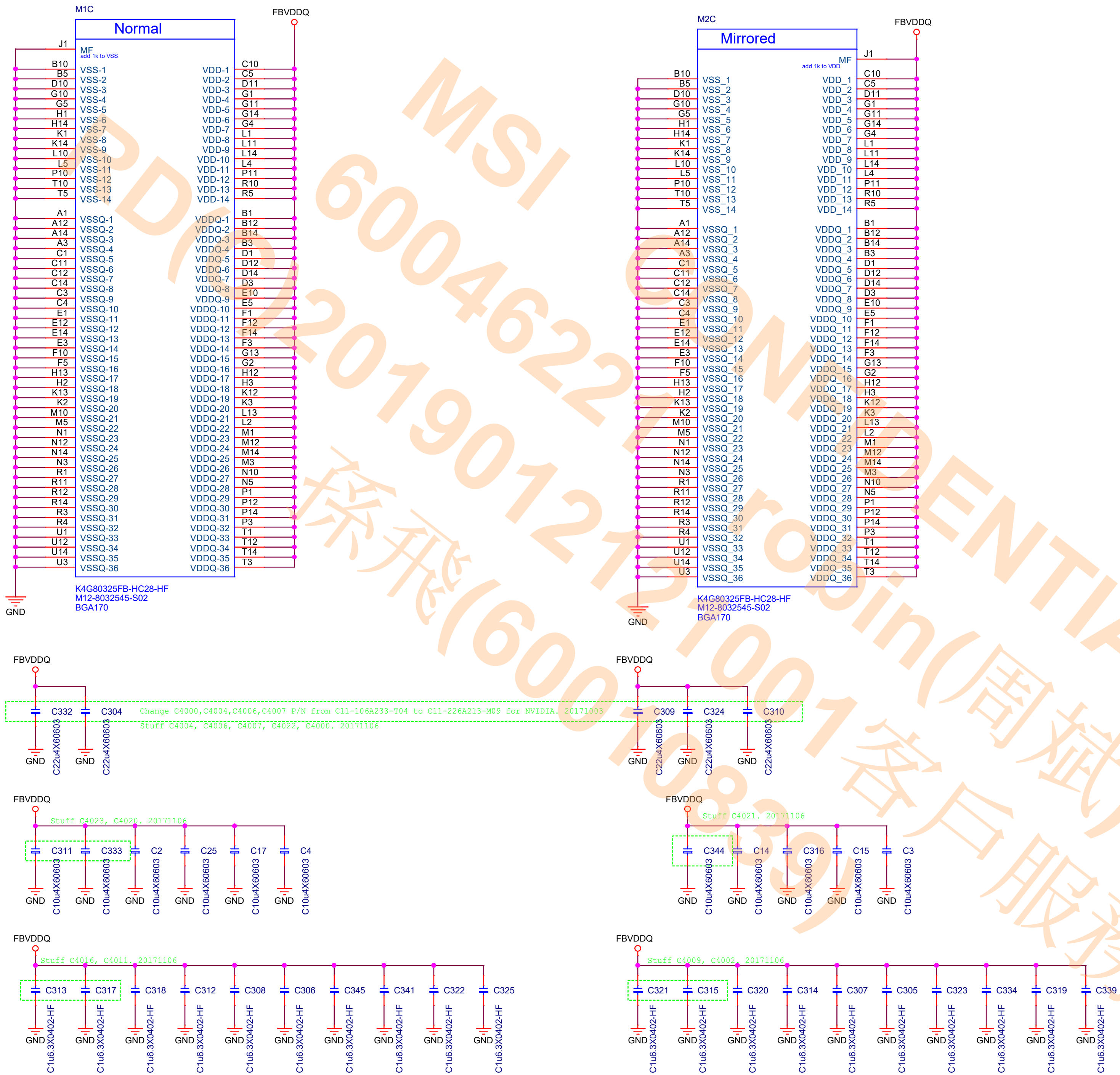
GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



M2B
<34> FBA_CMD28 L3 RAS*
<34> FBA_CMD31 G3 CAS*
<34> FBA_CMD21 G12 WE*
<34> FBA_CMD16 L12 CS*
<34> FBA_CMD24 J4 ABI*
<34> FBA_CMD26 K4 A10_A0
<34> FBA_CMD27 K5 A9_A1
<34> FBA_CMD18 K11 BA0_A2
<34> FBA_CMD17 K10 BA3_A3
<34> FBA_CMD19 H11 BA2_A4
<34> FBA_CMD20 H10 BA1_A5
<34> FBA_CMD23 H5 A11_A6
<34> FBA_CMD22 H4 A8_A7
<34> FBA_CMD25 J5 A12_RFU/NC
<34> FBA_CMD29 J2 RESET*
<34> FBA_CMD30 J3 CKE*
<34> FBA_CLK1 J12 CK
<34> FBA_CLK1# J11 CK#
R337 40.2R1%0402
R336 40.2R1%0402
C347 C0.01u25X0402
GND
A5 VPP_NC
U5 VPP/NC
Chagne R4201 from R11-1210T12-Y01 to R11-0121T12-W08 for NVIDIA suggest. 20171011A
<35> FBA_VREFC FBA_VREFC J14 VREFC
C5 C820p50X70402
120R1%0402 R5 J13 ZQ
J10 SEN
Close PIN J14
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170

N17S-G1_GDDR5_DECOUPLING



M1C
Normal
FBVDDQ
J1
MF
add 1k to VSS
VSS-1 … VSS-14
VSSQ-1 … VSSQ-36
VDD-1 … VDD-14
VDDQ-1 … VDDQ-36
GND
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170
M2C
Mirrored
add 1k to VDD
VSS_1 … VSS_14
VSSQ_1 … VSSQ_36
VDD_1 … VDD_14
VDDQ_1 … VDDQ_36
K4G80325FB-HC28-HF
M12-8032545-S02
BGA170
C332 C304 C309 C324 C310
C22u4X60603
Change C4000,C4004,C4006,C4007 P/N from C11-106A233-T04 to C11-226A213-M09 for NVIDIA. 20171003
Stuff C4004, C4006, C4007, C4022, C4000. 20171106
Stuff C4023, C4020. 20171106
C311 C333 C2 C25 C17 C4
Stuff C4021. 20171106
C344 C14 C316 C15 C3
C10u4X60603
Stuff C4016, C4011. 20171106
C313 C317 C318 C312 C308 C306 C345 C341 C322 C325
Stuff C4009, C4002. 20171106
C321 C315 C320 C314 C307 C305 C323 C334 C319 C339
C1u6.3X0402-HF

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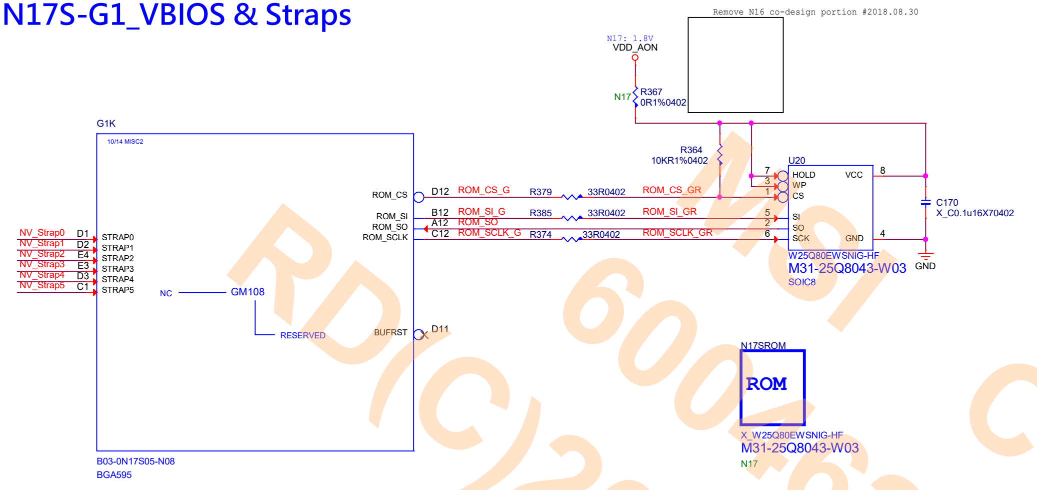
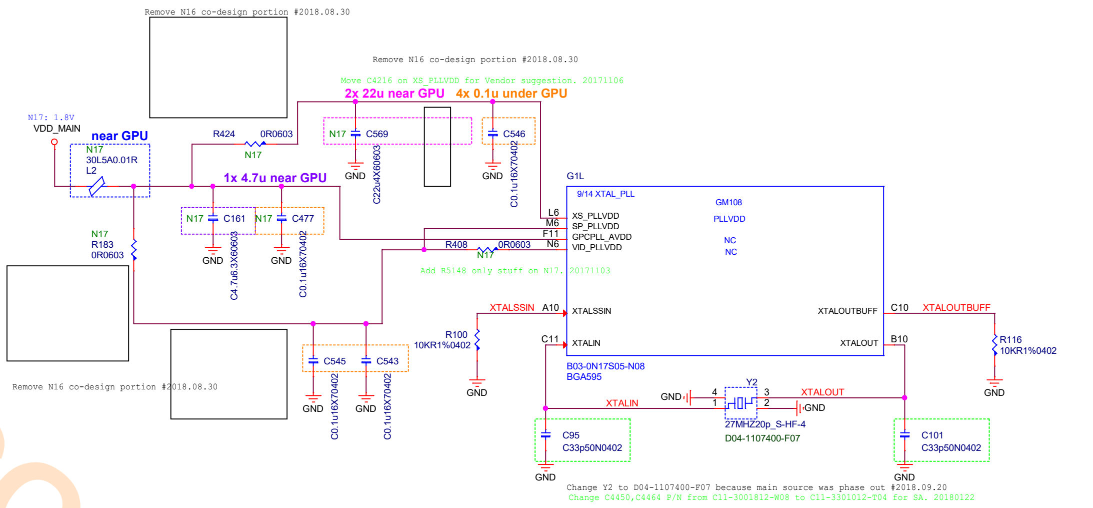
N17S-G1_VBIOS & Straps

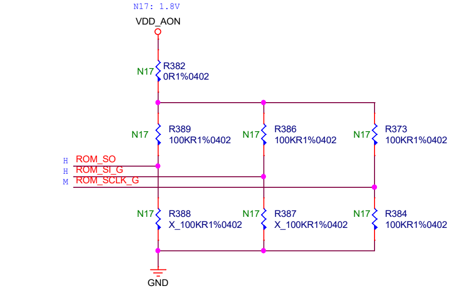


Remove N16 co-design portion #2018.08.30
N17: 1.8V
VDD_AON
N17 R367 0R1%0402
R364 10KR1%0402
U20
HOLD
WP
CS
VCC
SI
SO
SCK
GND
C170 X_C0.1u16X70402
GND
W25Q80EWSNIG-HF
M31-25Q8043-W03
SOIC8
G1K
10/14 MISC2
ROM_CS D12 ROM_CS_G R379 33R0402 ROM_CS_GR
ROM_SI B12 ROM_SI_G R385 33R0402 ROM_SI_GR
ROM_SO A12 ROM_SO
ROM_SCLK C12 ROM_SCLK_G R374 33R0402 ROM_SCLK_GR
NV_Strap0 D1 STRAP0
NV_Strap1 D2 STRAP1
NV_Strap2 E4 STRAP2
NV_Strap3 E3 STRAP3
NV_Strap4 D3 STRAP4
NV_Strap5 C1 STRAP5
NC GM108
RESERVED
BUFRST D11
B03-0N17S05-N08
BGA595
N17SROM
ROM
X_W25Q80EWSNIG-HF
M31-25Q8043-W03
N17



Remove N16 co-design portion #2018.08.30
Remove N16 co-design portion #2018.08.30
Move C4216 on XS_PLLVDD for Vendor suggestion. 20171106
2x 22u near GPU
4x 0.1u under GPU
N17: 1.8V
VDD_MAIN
near GPU
N17 30L5A0.01R L2
R424 0R0603
N17
N17 C569
C22u4X60603
C546
C0.1u16X70402
GND
1x 4.7u near GPU
N17 C161
N17 C477
C4.7u6.3X60603
C0.1u16X70402
N17 R183 0R0603
R408 0R0603
N17
Add R5148 only stuff on N17. 20171103
G1L
9/14 XTAL_PLL
XS_PLLVDD L6
SP_PLLVDD M6
GPCPLL_AVDD F11
VID_PLLVDD N6
GM108
PLLVDD
NC
NC
XTALSSIN A10
XTALSSIN
R100 10KR1%0402
XTALIN C11
XTALOUTBUFF C10 XTALOUTBUFF
XTALOUT B10
R116 10KR1%0402
B03-0N17S05-N08
BGA595
Remove N16 co-design portion #2018.08.30
C545
C543
C0.1u16X70402
XTALIN
Y2
XTALOUT
27MHZ20p_S-HF-4
D04-1107400-F07
C95 C33p50N0402
C101 C33p50N0402
GND
Change Y2 to D04-1107400-F07 because main source was phase out #2018.09.20
Change C4450,C4464 P/N from C11-3001812-W08 to C11-3001012-T06 for SA. 20180122

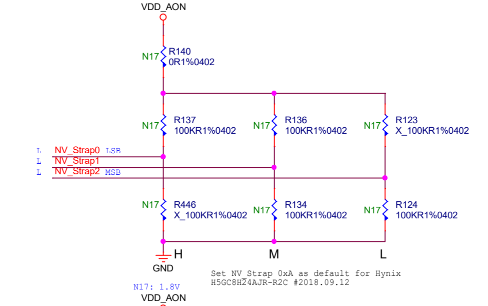
256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
	Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver[2]



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	1:ENABLE	0:DISABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



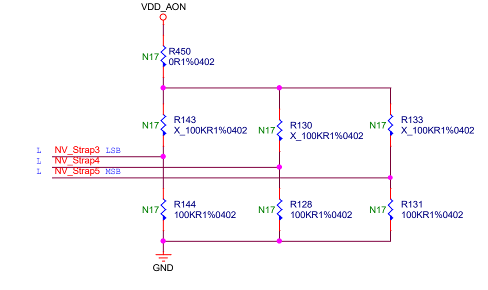
Set NV_Strap 0xA as default for Hynix H5GC8H24AJR-R2C #2018.09.12

STRAP 2	STRAP 1	STRAP 0		N17S-G1 3.0G RAM	
L	L	L	0x0	Samsung K4G80325FB-HC28	256M*32
L	L	H	0x1	Micron MT51J256M32HF-70:A	
L	H	L	0x2	Hynix H5GC8H24MJR-R0C	
H	L	L	0x6	Hynix H5GC4H24AJR-R0C	
H	H	H	0x7	Samsung K4G41325FE-HC28	128M*32
L	L	M	0x8	Micron EDW4032BABG-70-F	

STRAP 2	STRAP 1	STRAP 0		N17S-G2 3.5G RAM	
L	M	L	0x9	MICRON MT51J256M32HF-80:B	256M*32
L	M	H	0xA	HYNIX H5GC8H24AJR-R2C	

Table 12. N16/GB2B-64 Multi-Level Straps

Strap Pin	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Stuff 49.9 kΩ pull-up to VDD_AON (3.3V).			
STRAP1	Reserved			
STRAP2	Reserved			
STRAP3	Reserved			
STRAP4	Reserved			



STRAP 5	STRAP 4	STRAP 3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	Optimus
L	L	H	0	0	0	1	Discrete
H	L	H	0	1	0	1	Discrete with Gsync

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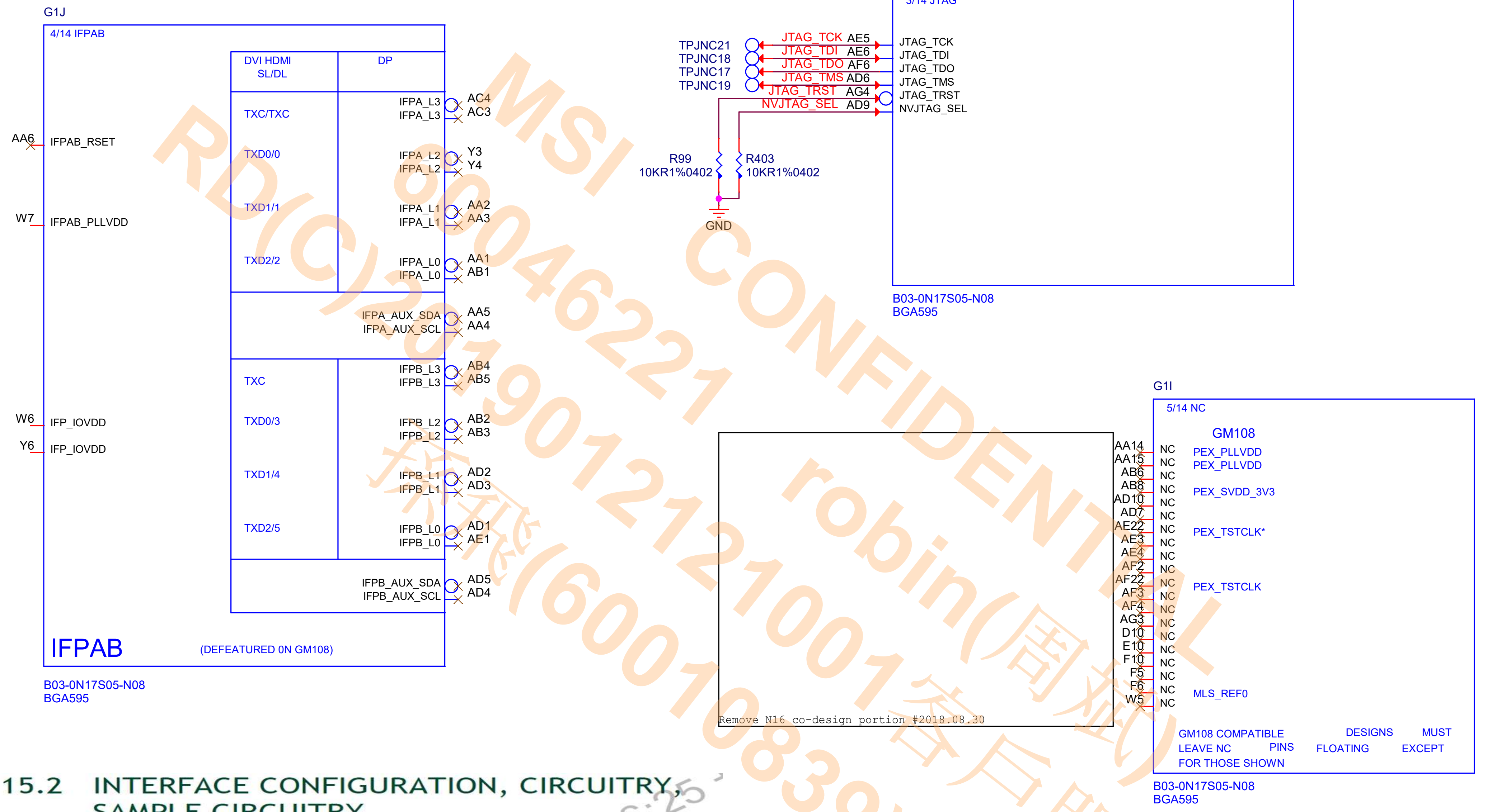
N17S-G1_Display IF


G1J
4/14 IFPAB
DVI HDMI SL/DL
DP
TXC/TXC
TXD0/0
TXD1/1
TXD2/2
TXC
TXD0/3
TXD1/4
TXD2/5
AA6 IFPAB_RSET
W7 IFPAB_PLLVDD
W6 IFP_IOVDD
Y6 IFP_IOVDD
IFPA_L3 AC4
IFPA_L3 AC3
IFPA_L2 Y3
IFPA_L2 Y4
IFPA_L1 AA2
IFPA_L1 AA3
IFPA_L0 AA1
IFPA_L0 AB1
IFPA_AUX_SDA AA5
IFPA_AUX_SCL AA4
IFPB_L3 AB4
IFPB_L3 AB5
IFPB_L2 AB2
IFPB_L2 AB3
IFPB_L1 AD2
IFPB_L1 AD3
IFPB_L0 AD1
IFPB_L0 AE1
IFPB_AUX_SDA AD5
IFPB_AUX_SCL AD4
IFPAB
(DEFEATURED 0N GM108)
B03-0N17S05-N08
BGA595
G1N
3/14 JTAG
TPJNC21 JTAG_TCK AE5 JTAG_TCK
TPJNC18 JTAG_TDI AE6 JTAG_TDI
TPJNC17 JTAG_TDO AF6 JTAG_TDO
TPJNC19 JTAG_TMS AD6 JTAG_TMS
JTAG_TRST AG4 JTAG_TRST
NVJTAG_SEL AD9 NVJTAG_SEL
R99
10KR1%0402
R403
10KR1%0402
GND
B03-0N17S05-N08
BGA595
G1I
5/14 NC
GM108
AA14 NC PEX_PLLVDD
AA15 NC PEX_PLLVDD
AB6 NC
AB8 NC PEX_SVDD_3V3
AD10 NC
AD7 NC
AE22 NC PEX_TSTCLK*
AE3 NC
AE4 NC
AF2 NC
AF22 NC PEX_TSTCLK
AF3 NC
AF4 NC
AG3 NC
D10 NC
E10 NC
F10 NC
F5 NC
F6 NC MLS_REF0
W5 NC
GM108 COMPATIBLE DESIGNS MUST
LEAVE NC PINS FLOATING EXCEPT
FOR THOSE SHOWN
B03-0N17S05-N08
BGA595
Remove N16 co-design portion #2018.08.30

15.2 INTERFACE CONFIGURATION, CIRCUITRY, SAMPLE CIRCUITRY

To select different Strap Mode, MULTI_STRAP_REF0_GND pins need to be stuffed accordingly. Table 15-1 provides the necessary connections to set the correct strapping mode for each device.

Table 15-1. Device Specific Strap Mode Selection

	All N16x GPUs
Multi_Strap_Ref0_GND	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 40.2k 1% to GND

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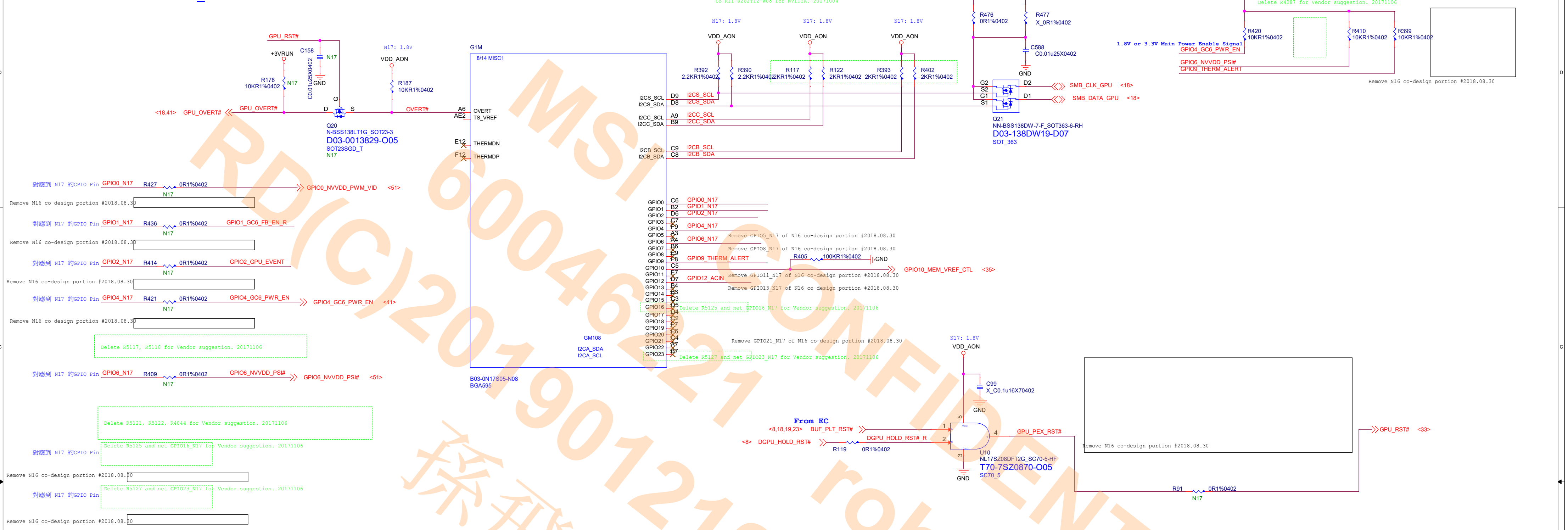
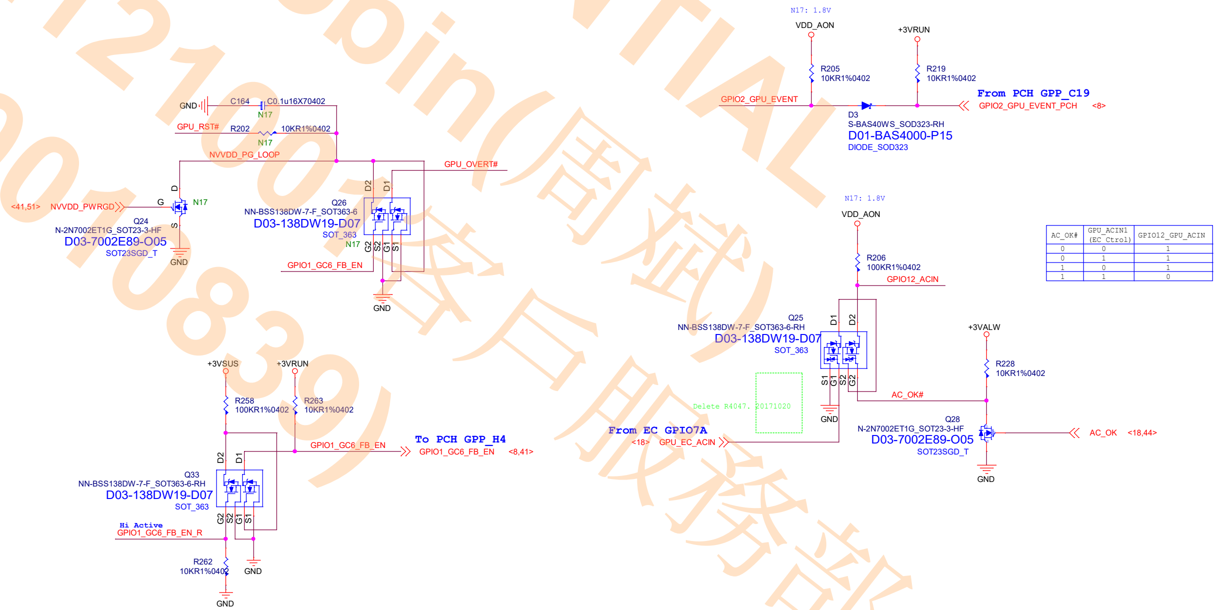
N17S-G1_GPIO



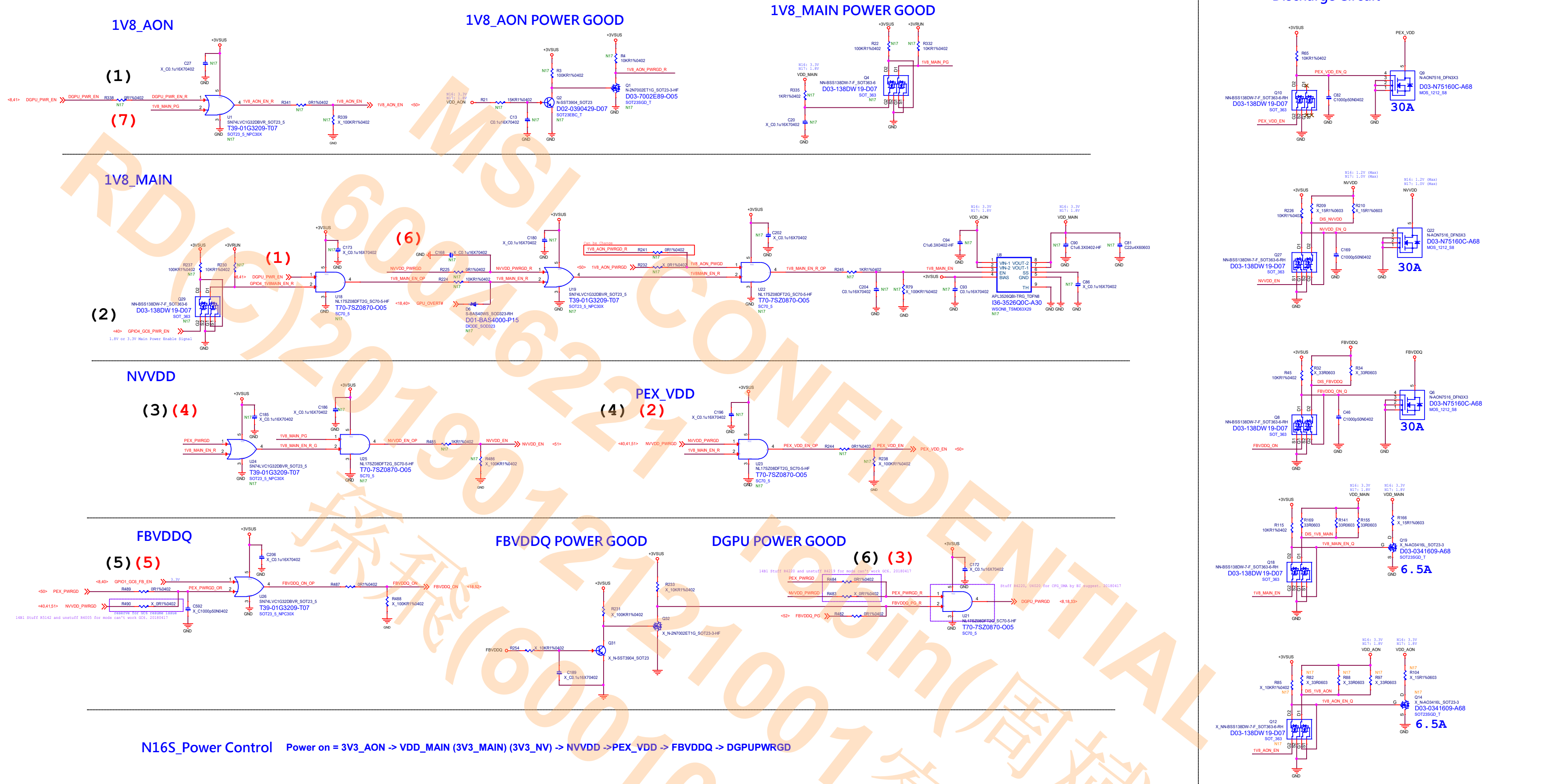


Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	O	PWM Output To Contral NVVDD	0 TO 1V8 PWM Output
GPIO1	GC6M:GC6_FB_EN	O	FB Enable For GC6 2.1	Open Source 10K Pull-Down
GPIO2	GC6M:GC6_EVENT / WAKE	I	GPU Wake Signal For GC6 2.1	10K Pull-Up To 1V8_AON Unless Driven Actively
GPIO3	NVVDDS_PWM(NC)	I/O	PWM Output To Control The NVVDS Power Supply	0 TO 1V8 Output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU Power Sequencing For GC6 2.1	Open Drain 10K Pull-Up To 1V8_AON
GPIO5	FRM_LCK	I	Active Low Frame Lock	Open Drain 10K Pull-Up To 1V8_AON
GPIO6	NVVDD_PSI/NVVDDS_PSI	O	Phase Shedding	10K Pull-Up To 1V8_AON To Enable Multiple Phases
GPIO7	LCD_BL_PWM(NC)	O	Panel Backlight Enable	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	Pull-Up/Pull-Down To Set The FBVDD/Q Power ON Voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10K Pull-Up To 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD(NC)	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC Power Detect Or Power Supply Overdraw Input	100K Pull-Up To 1V8_AON
GPIO13	LCD_BLEN(NC)	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA(NC)	I	Hot Plug Detect for IFPA	
GPIO15	HPD_IFPB(NC)	I	Hot Plug Detect for IFPB	
GPIO16	GC6M:SYS_PEX_RST_MON	I	System Side PCIE Reset Monitor	10K Pull-Up To 1V8_AON Unless Driven Actively
GPIO17	UNUSED(NC)	I/O		
GPIO18	UNUSED(NC)	I/O		
GPIO19	3D Vision(NC)	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE(NC)	I/O		
GPIO21	OC_WARN/HT	I	Over Current Throttling Trigger	10K Pull-Up To 1V8_AON
GPIO22	UNUSED(NC)	I/O		
GPIO23	GC6M:GPU_PEX_RST_HOLD	O	GPU PCIE Self Reset Control	Open Drain 10K Pull-Up To Gated 3V3

N17S-G1_Power Control

Power on = 1V8_AON -> (VDD_MAIN) 1V8_MAIN -> NVVDD+NVVDDS -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

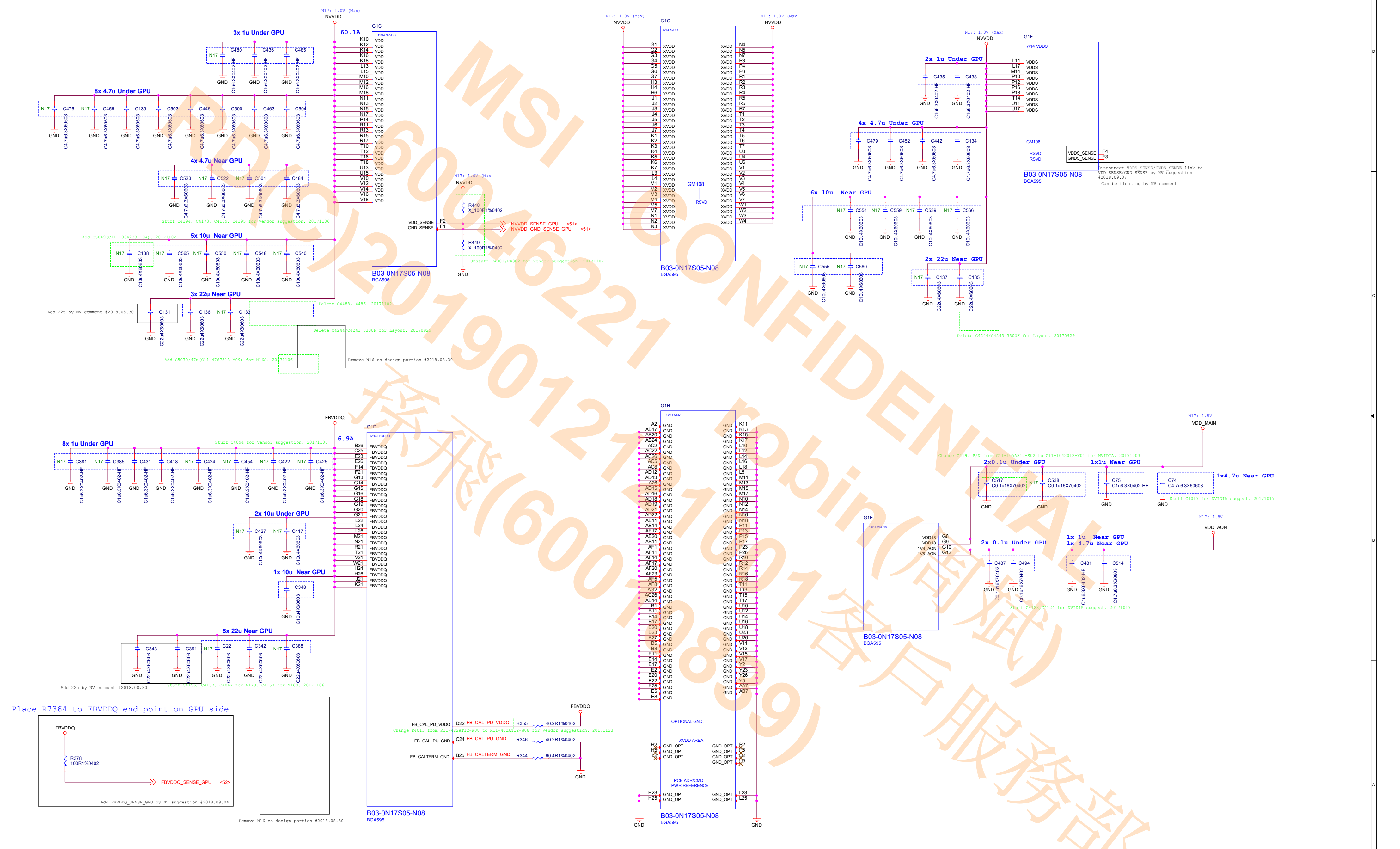
Power down = PEX_VDD/FBVDDQ -> NVVDD+NVVDDS -> 1V8_MAIN -> 1V8_AON



N16S_Power Control   Power on = 3V3_AON -> VDD_MAIN (3V3_MAIN) (3V3_NV) -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD

Remove N16 co-design portion #2018.08.30

N17S-G1_Power & GND



3x 1u Under GPU
8x 4.7u Under GPU
4x 4.7u Near GPU
5x 10u Near GPU
3x 22u Near GPU
60.1A
NVVDD
VDD_SENSE
GND_SENSE
NVVDD_SENSE_GPU
NVVDD_GND_SENSE_GPU
B03-0N17S05-N08
BGA595
2x 1u Under GPU
4x 4.7u Under GPU
6x 10u Near GPU
2x 22u Near GPU
VDDS_SENSE
GNDS_SENSE
8x 1u Under GPU
6.9A
FBVDDQ
2x 10u Under GPU
1x 10u Near GPU
5x 22u Near GPU
Place R7364 to FBVDDQ end point on GPU side
FBVDDQ_SENSE_GPU
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CALTERM_GND
2x0.1u Under GPU
1x1u Near GPU
1x4.7u Near GPU
2x 0.1u Under GPU
1x 1u Near GPU
1x 4.7u Near GPU
VDD_MAIN
VDD_AON
OPTIONAL GND:
XVDD AREA
PCB ADR/CMD PWR REFERENCE

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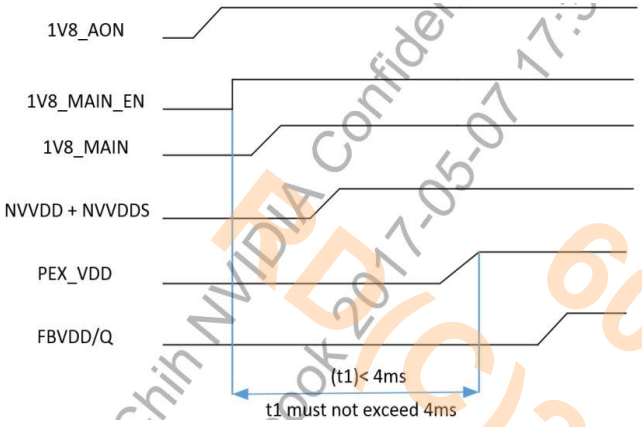
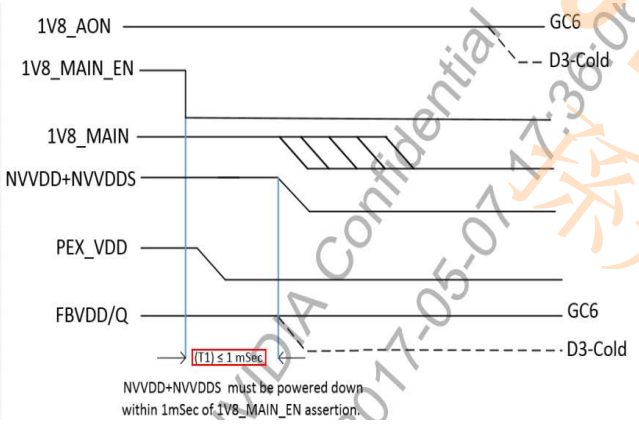
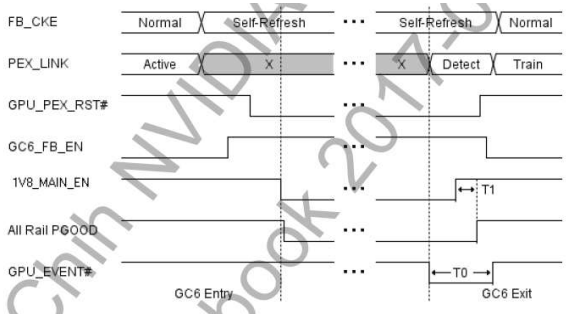
N17 Power Up



N17 Power Down



GC6 2.1



GC6 2.1 Entry/Exit Sequence Timing Diagram

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

GC6 2.0

18.3.4.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-14 and Table 18-3 describes the GC6 2.0 entry and exit sequence and timing requirements.

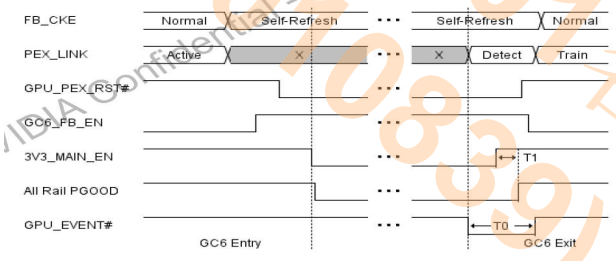


Figure 18-14. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

N16 Power Up

Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.

Optimus

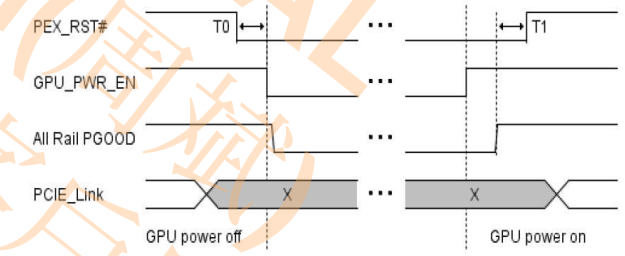


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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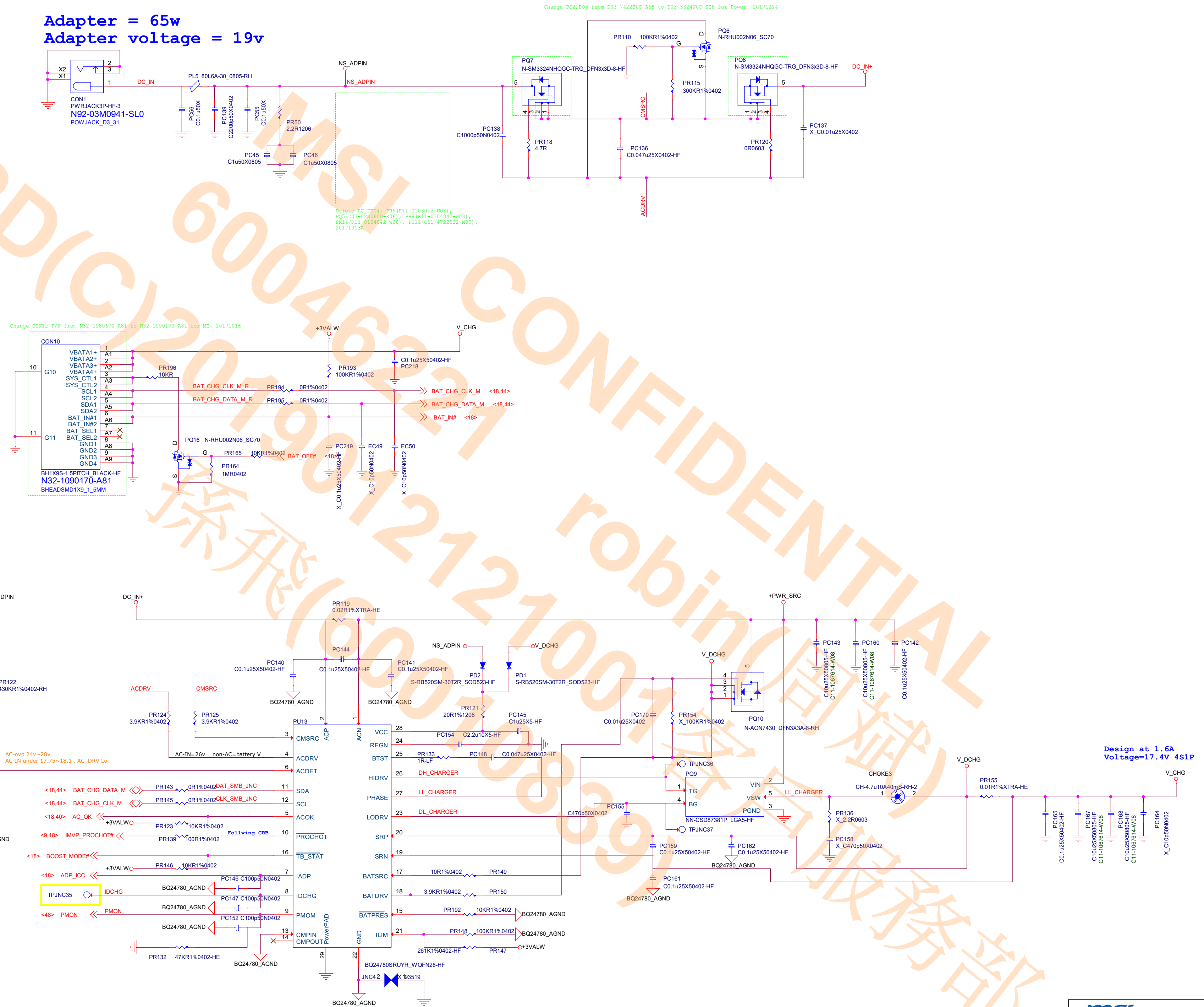

Adapter = 65w
Adapter voltage = 19v
CON1
PWRJACK3P-HF-3
N92-03M0941-SL0
POWJACK_D3_31
DC_IN
PL5 80L6A-30_0805-RH
NS_ADPIN
PC56 C0.1u50X
PC139 C2200p50X0402
PC55 C0.1u50X
PR50 2.2R1206
PC45 C1u50X0805
PC46 C1u50X0805
Change PQ2,PQ3 from D03-7422E0C-A69 to D03-3324N0C-ST8 for Power. 20171214
PQ7 N-SM3324NHQGC-TRG_DFN3x3D-8-HF
PQ8 N-SM3324NHQGC-TRG_DFN3x3D-8-HF
PQ6 N-RHU002N06_SC70
PR110 100KR1%0402
PR115 300KR1%0402
PC138 C1000p50N0402
PR118 4.7R
PC136 C0.047u25X0402-HF
PR120 0R0603
PC137 X_C0.01u25X0402
DC_IN+
CMSRC
ACDRV
Change CON12 P/N from N32-1080670-A81 to N32-1090170-A81 for ME. 20171016
CON10
VBATA1+ VBATA2+ VBATA3+ VBATA4+ SYS_CTL1 SYS_CTL2 SCL1 SCL2 SDA1 SDA2 BAT_IN#1 BAT_IN#2 BAT_SEL1 BAT_SEL2 GND1 GND2 GND3 GND4
BH1X9S-1.5PITCH_BLACK-HF
N32-1090170-A81
BHEADSMD1X9_1_5MM
+3VALW
V_CHG
PR196 10KR
PR193 100KR1%0402
PC218 C0.1u25X50402-HF
BAT_CHG_CLK_M_R
BAT_CHG_DATA_M_R
PR194 0R1%0402
PR195 0R1%0402
BAT_CHG_CLK_M <18,44>
BAT_CHG_DATA_M <18,44>
BAT_IN# <18>
PQ16 N-RHU002N06_SC70
PR165 10KR1%0402
BAT_OFF# <18>
PR164 1MR0402
PC219 X_C0.1u25X50402-HF
EC49 X_C10p50N0402
EC50 X_C10p50N0402
NS_ADPIN
DC_IN+
PR119 0.02R1%XTRA-HE
PC144 C0.1u25X50402-HF
PC140 C0.1u25X50402-HF
PC141 C0.1u25X50402-HF
BQ24780_AGND
PR122 430KR1%0402-RH
ACDRV
CMSRC
PR124 3.9KR1%0402
PR125 3.9KR1%0402
AC-ovp 24v~28v
AC-IN under 17.75~18.1 , AC_DRV Lo
AC-IN=26v non-AC=battery V
PR126 66.5KR1%0402
PR138 0R1%0402
PQ11 N-RHU002N06_SC70
<18> AC_CTL
PR141 100KR1%0402
<18,44> BAT_CHG_DATA_M
<18,44> BAT_CHG_CLK_M
<18,40> AC_OK
<9,48> IMVP_PROCHOT#
<18> BOOST_MODE#
<18> ADP_ICC
<48> PMON
TPJNC35
IDCHG
PR143 0R1%0402 DAT_SMB_JNC
PR145 0R1%0402 CLK_SMB_JNC
PR123 10KR1%0402
PR139 100R1%0402 Follwing CRB
PR146 10KR1%0402
PC146 C100p50N0402
PC147 C100p50N0402
PC152 C100p50N0402
PR132 47KR1%0402-HE
PU13
CMSRC ACDRV ACDET SDA SCL ACOK PROCHOT TB_STAT IADP IDCHG PMON CMPIN CMPOUT PowerPAD ACP ACN GND
VCC REGN BTST HIDRV PHASE LODRV SRP SRN BATSRC BATDRV BATPRES ILIM
BQ24780SRUYR_WQFN28-HF
JNC42 X_93519
PD2 S-RB520SM-30T2R_SOD523-HF
PD1 S-RB520SM-30T2R_SOD523-HF
V_DCHG
PR121 20R1%1206
PC145 C1u25X5-HF
PC154 C2.2u10X5-HF
PR133 1R-LF
PC148 C0.047u25X0402-HF
DH_CHARGER
LL_CHARGER
DL_CHARGER
PC155 C470p50X0402
PC170 C0.01u25X0402
PR154 X_100KR1%0402
PQ10 N-AON7430_DFN3X3A-8-RH
+PWR_SRC
PC143 C10u25X50805-HF C11-1067614-W08
PC160 C10u25X50805-HF C11-1067614-W08
PC142 C0.1u25X50402-HF
TPJNC36
PQ9 NN-CSD87381P_LGA5-HF
VIN TG VSW BG PGND
TPJNC37
CHOKE3 CH-4.7u10A40mS-RH-2
PR136 X_2.2R0603
PC158 X_C470p50X0402
PC159 C0.1u25X50402-HF
PC162 C0.1u25X50402-HF
PC161 C0.1u25X50402-HF
PR149 10R1%0402
PR150 3.9KR1%0402
PR192 10KR1%0402
PR148 100KR1%0402
PR147 261K1%0402-HF
Design at 1.6A
Voltage=17.4V 4S1P
PR155 0.01R1%XTRA-HE
PC165 C0.1u25X50402-HF
PC167 C10u25X50805-HF C11-1067614-W08
PC168 C10u25X50805-HF C11-1067614-W08
PC164 X_C10p50N0402

MICRO-STAR INT'L CO.,LTD.

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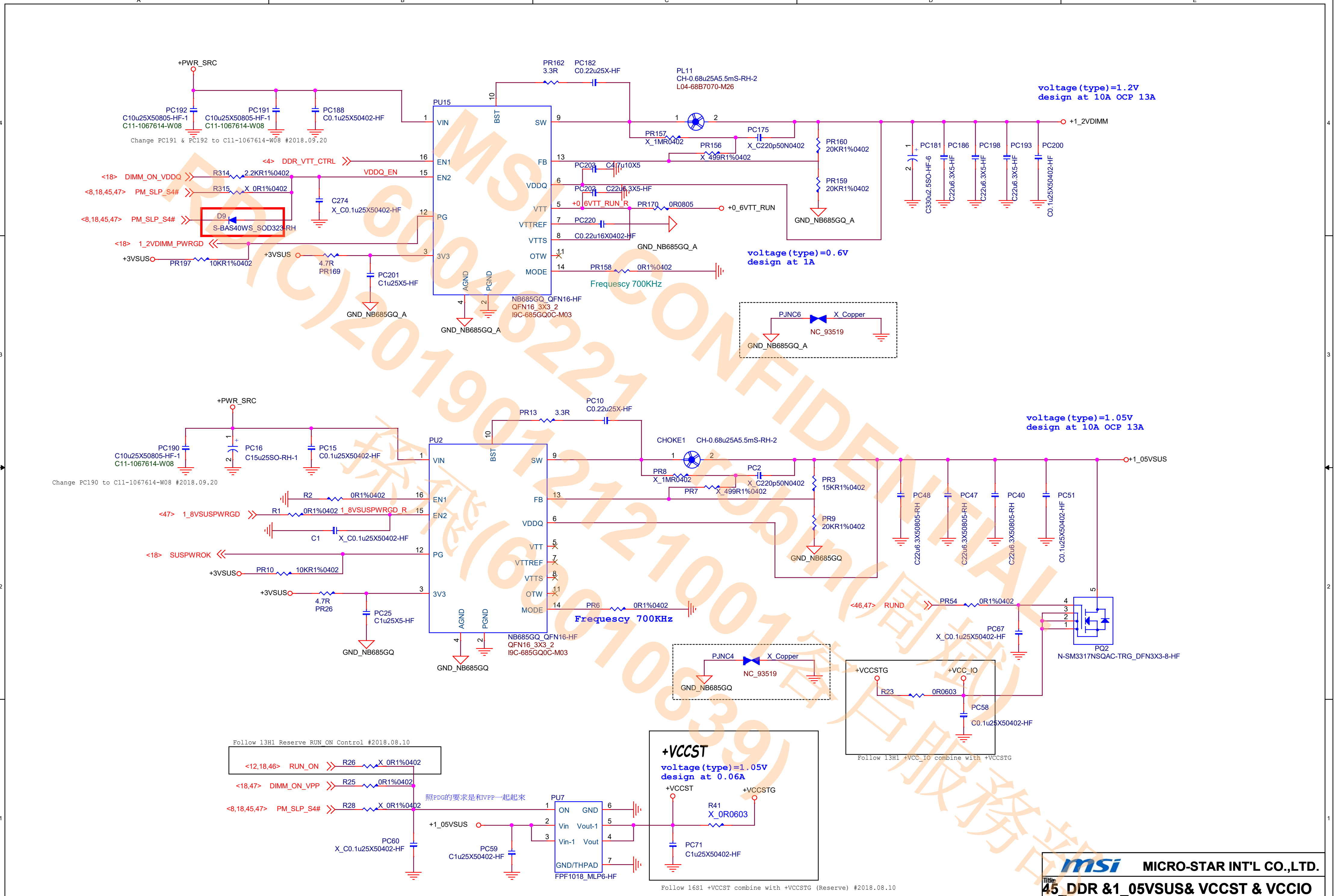
+PWR_SRC
PC192 C10u25X50805-HF-1 C11-1067614-W08
PC191 C10u25X50805-HF-1 C11-1067614-W08
PC188 C0.1u25X50402-HF
Change PC191 & PC192 to C11-1067614-W08 #2018.09.20
PR162 3.3R
PC182 C0.22u25X-HF
PL11 CH-0.68u25A5.5mS-RH-2 L04-68B7070-M26
voltage(type)=1.2V
design at 10A OCP 13A
+1_2VDIMM
PU15
VIN BST SW EN1 FB EN2 VDDQ PG VTT VTTREF VTTS 3V3 OTW MODE AGND PGND
<4> DDR_VTT_CTRL
<18> DIMM_ON_VDDQ
R314 2.2KR1%0402
VDDQ_EN
<8,18,45,47> PM_SLP_S4#
R315 X_0R1%0402
C274 X_C0.1u25X50402-HF
D9 S-BAS40WS_SOD323-RH
<18> 1_2VDIMM_PWRGD
+3VSUS
PR197 10KR1%0402
4.7R PR169
PC201 C1u25X5-HF
GND_NB685GQ_A
NB685GQ_QFN16-HF QFN16_3X3_2 I9C-685GQ0C-M03
PR157 X_1MR0402
PC175 X_C220p50N0402
PR156 X_499R1%0402
PR160 20KR1%0402
PR159 20KR1%0402
PC203 C4.7u10X5
PC202 C22u6.3X5-HF
+0_6VTT_RUN_R
PR170 0R0805
+0_6VTT_RUN
PC220 C0.22u16X0402-HF
PR158 0R1%0402
Frequescy 700KHz
voltage(type)=0.6V
design at 1A
PC181 C330u2.5SO-HF-6
PC186 C22u6.3X5-HF
PC198 C22u6.3X5-HF
PC193 C22u6.3X5-HF
PC200 C0.1u25X50402-HF
PJNC6 X_Copper NC_93519
+PWR_SRC
PC190 C10u25X50805-HF-1 C11-1067614-W08
PC16 C15u25SO-RH-1
PC15 C0.1u25X50402-HF
Change PC190 to C11-1067614-W08 #2018.09.20
PR13 3.3R
PC10 C0.22u25X-HF
CHOKE1 CH-0.68u25A5.5mS-RH-2
voltage(type)=1.05V
design at 10A OCP 13A
+1_05VSUS
PU2
R2 0R1%0402
<47> 1_8VSUSPWRGD
R1 0R1%0402 1_8VSUSPWRGD_R
C1 X_C0.1u25X50402-HF
<18> SUSPWROK
+3VSUS PR10 10KR1%0402
4.7R PR26
PC25 C1u25X5-HF
GND_NB685GQ
NB685GQ_QFN16-HF QFN16_3X3_2 I9C-685GQ0C-M03
PR8 X_1MR0402
PC2 X_C220p50N0402
PR7 X_499R1%0402
PR3 15KR1%0402
PR9 20KR1%0402
PR6 0R1%0402
Frequescy 700KHz
PC48 C22u6.3X50805-RH
PC47 C22u6.3X50805-RH
PC40 C22u6.3X50805-RH
PC51 C0.1u25X50402-HF
<46,47> RUND
PR54 0R1%0402
PC67 X_C0.1u25X50402-HF
PQ2 N-SM3317NSQAC-TRG_DFN3X3-8-HF
PJNC4 X_Copper NC_93519
+VCCSTG +VCC_IO
R23 0R0603
PC58 C0.1u25X50402-HF
Follow 13H1 +VCC_IO combine with +VCCSTG
Follow 13H1 Reserve RUN_ON Control #2018.08.10
<12,18,46> RUN_ON R26 X_0R1%0402
<18,47> DIMM_ON_VPP R25 0R1%0402
<8,18,45,47> PM_SLP_S4# R28 X_0R1%0402
照PDG的要求是和VPP一起起来
PC60 X_C0.1u25X50402-HF
+1_05VSUS
PC59 C1u25X50402-HF
PU7
ON GND Vin Vout-1 Vin-1 Vout GND/THPAD
FPF1018_MLP6-HF
+VCCST
voltage(type)=1.05V
design at 0.06A
+VCCST +VCCSTG
R41 X_0R0603
PC71 C1u25X50402-HF
Follow 16S1 +VCCST combine with +VCCSTG (Reserve) #2018.08.10

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Title: 45_DDR &1_05VSUS& VCCST & VCCIO

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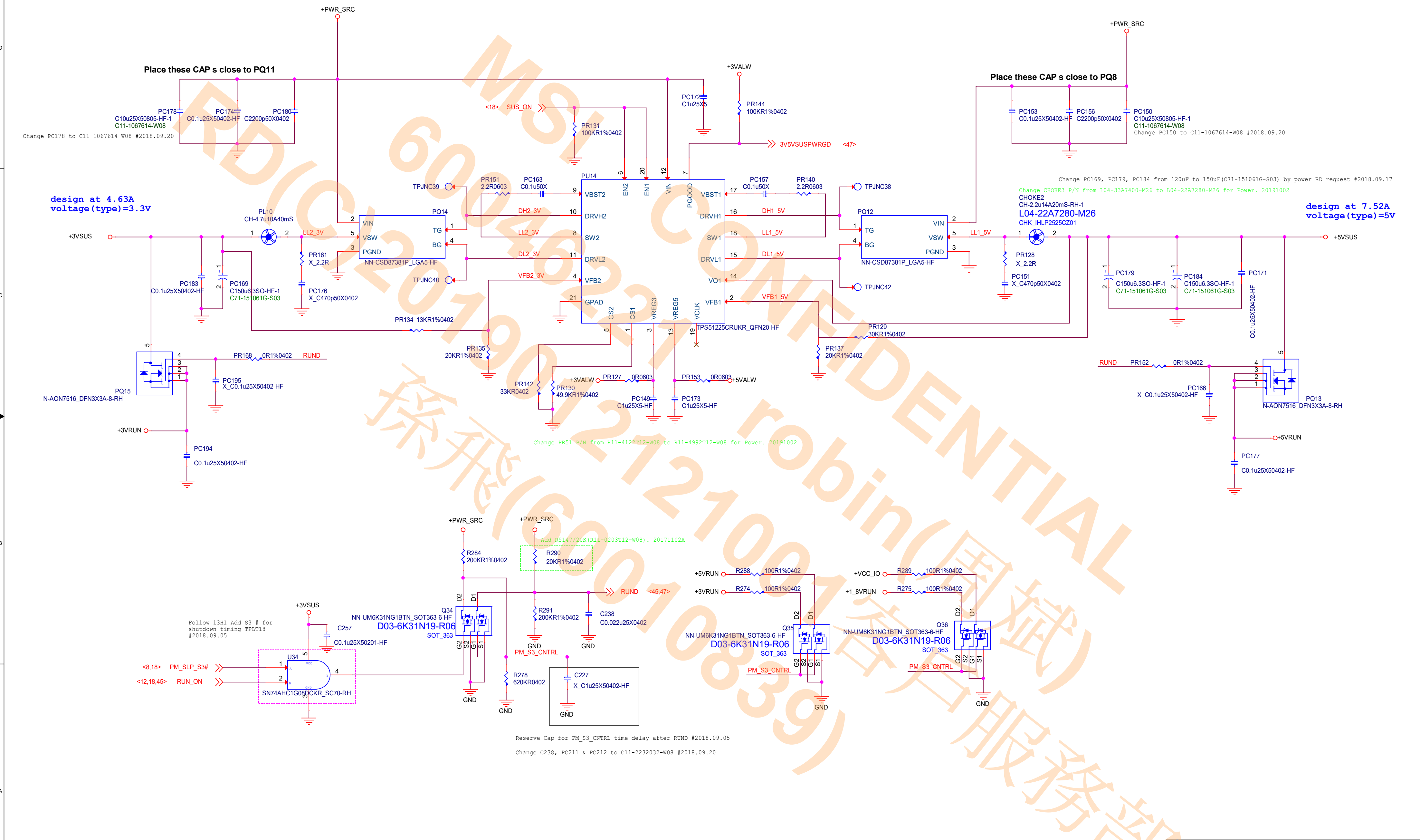

Place these CAP s close to PQ11
+PWR_SRC
PC178
C10u25X50805-HF-1
C11-1067614-W08
PC174
C0.1u25X50402-HF
PC180
C2200p50X0402
Change PC178 to C11-1067614-W08 #2018.09.20
design at 4.63A
voltage(type)=3.3V
+3VSUS
PL10
CH-4.7u10A40mS
LL2_3V
PC183
C0.1u25X50402-HF
PC169
C150u6.3SO-HF-1
C71-151061G-S03
PR161
X_2.2R
PC176
X_C470p50X0402
PQ14
NN-CSD87381P_LGA5-HF
VIN
VSW
PGND
TG
BG
TPJNC39
TPJNC40
PR151
2.2R0603
PC163
C0.1u50X
<18> SUS_ON
PR131
100KR1%0402
PC172
C1u25X5
+3VALW
PR144
100KR1%0402
3V5VSUSPWRGD <47>
PU14
TPS51225CRUKR_QFN20-HF
VBST2
DRVH2
SW2
DRVL2
VFB2
GPAD
EN2
EN1
VIN
PGOOD
VBST1
DRVH1
SW1
DRVL1
VO1
VFB1
CS2
CS1
VREG3
VREG5
VCLK
DH2_3V
LL2_3V
DL2_3V
VFB2_3V
DH1_5V
LL1_5V
DL1_5V
VFB1_5V
PC157
C0.1u50X
PR140
2.2R0603
TPJNC38
TPJNC42
PR134 13KR1%0402
PR135
20KR1%0402
PR142
33KR0402
PR130
49.9KR1%0402
PR127 0R0603
PC149
C1u25X5-HF
PR153 0R0603
+5VALW
PC173
C1u25X5-HF
PR129
30KR1%0402
PR137
20KR1%0402
Change PR51 P/N from R11-4122T12-W08 to R11-4992T12-W08 for Power. 20191002
Place these CAP s close to PQ8
PC153
C0.1u25X50402-HF
PC156
C2200p50X0402
PC150
C10u25X50805-HF-1
C11-1067614-W08
Change PC150 to C11-1067614-W08 #2018.09.20
Change PC169, PC179, PC184 from 120uF to 150uF(C71-151061G-S03) by power RD request #2018.09.17
Change CHOKE3 P/N from L04-33A7400-M26 to L04-22A7280-M26 for Power. 20191002
CHOKE2
CH-2.2u14A20mS-RH-1
L04-22A7280-M26
CHK_IHLP2525CZ01
design at 7.52A
voltage(type)=5V
PQ12
NN-CSD87381P_LGA5-HF
LL1_5V
+5VSUS
PR128
X_2.2R
PC151
X_C470p50X0402
PC179
C150u6.3SO-HF-1
C71-151061G-S03
PC184
C150u6.3SO-HF-1
C71-151061G-S03
PC171
C0.1u25X50402-HF
PQ15
N-AON7516_DFN3X3A-8-RH
PR168 0R1%0402 RUND
PC195
X_C0.1u25X50402-HF
+3VRUN
PC194
C0.1u25X50402-HF
RUND PR152 0R1%0402
PC166
X_C0.1u25X50402-HF
PQ13
N-AON7516_DFN3X3A-8-RH
+5VRUN
PC177
C0.1u25X50402-HF
+PWR_SRC
R284
200KR1%0402
+PWR_SRC
Add R5147/20K(R11-2003T12-W08). 20171102A
R290
20KR1%0402
RUND <45,47>
R291
200KR1%0402
C238
C0.022u25X0402
Q34
NN-UM6K31NG1BTN_SOT363-6-HF
D03-6K31N19-R06
SOT_363
PM_S3_CNTRL
R278
620KR0402
C227
X_C1u25X50402-HF
GND
+3VSUS
C257
C0.1u25X50201-HF
Follow 13H1 Add S3 # for shutdown timing TPLT18 #2018.09.05
U34
SN74AHC1G08DCKR_SC70-RH
<8,18> PM_SLP_S3#
<12,18,45> RUN_ON
+5VRUN R288 100R1%0402
+3VRUN R274 100R1%0402
Q35
NN-UM6K31NG1BTN_SOT363-6-HF
D03-6K31N19-R06
SOT_363
PM_S3_CNTRL
+VCC_IO R289 100R1%0402
+1_8VRUN R275 100R1%0402
Q36
NN-UM6K31NG1BTN_SOT363-6-HF
D03-6K31N19-R06
SOT_363
PM_S3_CNTRL
Reserve Cap for PM_S3_CNTRL time delay after RUND #2018.09.05
Change C238, PC211 & PC212 to C11-2232032-W08 #2018.09.20

MICRO-STAR INT'L CO.,LTD.

Title: **System Power**

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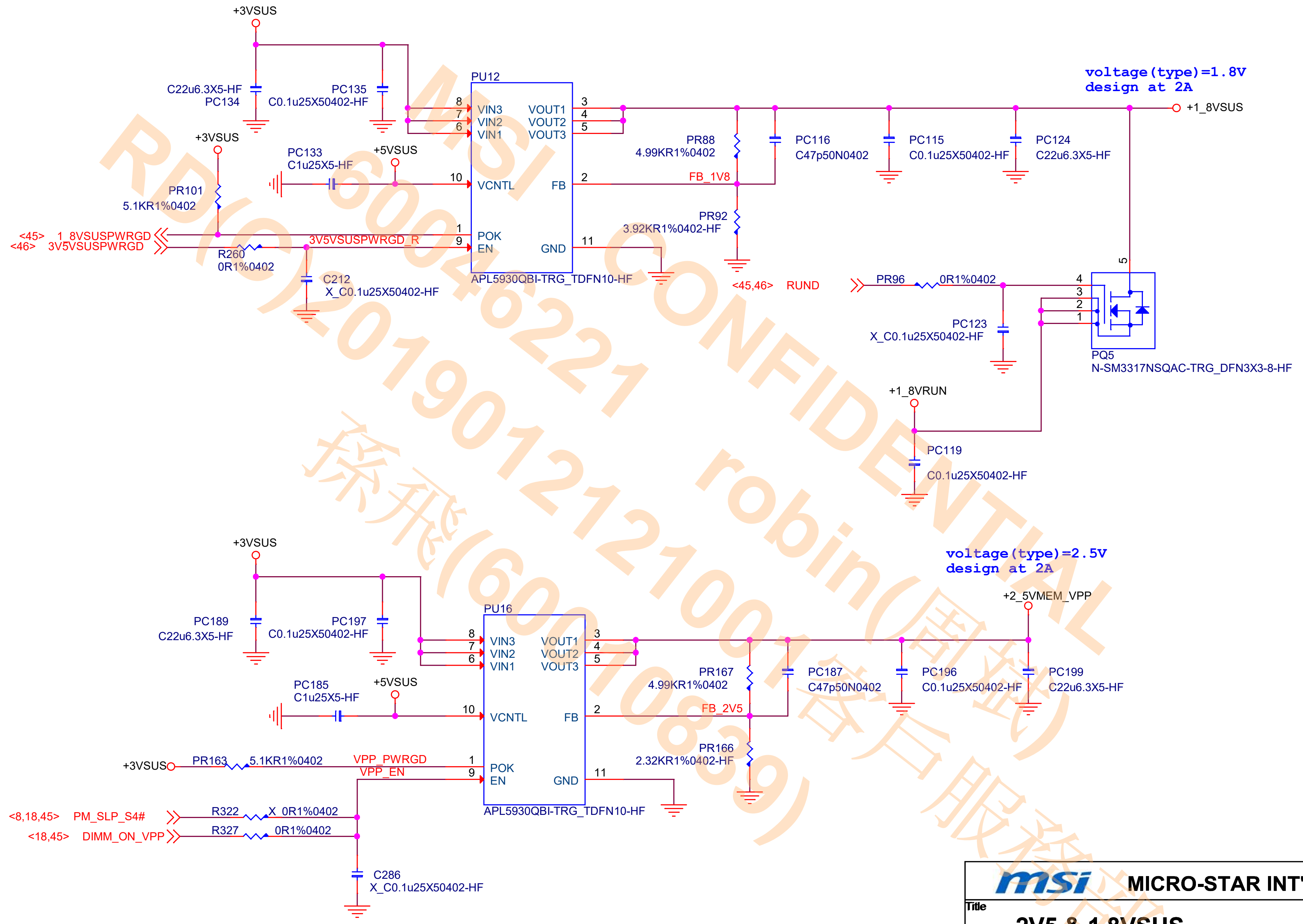
voltage(type)=1.8V
design at 2A
+3VSUS
C22u6.3X5-HF
PC134
PC135
C0.1u25X50402-HF
PU12
VIN3
VIN2
VIN1
VOUT1
VOUT2
VOUT3
VCNTL
FB
POK
EN
GND
APL5930QBI-TRG_TDFN10-HF
+1_8VSUS
PR88
4.99KR1%0402
PC116
C47p50N0402
PC115
C0.1u25X50402-HF
PC124
C22u6.3X5-HF
FB_1V8
PR92
3.92KR1%0402-HF
PC133
C1u25X5-HF
+5VSUS
PR101
5.1KR1%0402
<45> 1_8VSUSPWRGD
<46> 3V5VSUSPWRGD
3V5VSUSPWRGD_R
R260
0R1%0402
C212
X_C0.1u25X50402-HF
<45,46> RUND
PR96
0R1%0402
PC123
X_C0.1u25X50402-HF
PQ5
N-SM3317NSQAC-TRG_DFN3X3-8-HF
+1_8VRUN
PC119
C0.1u25X50402-HF
voltage(type)=2.5V
design at 2A
+2_5VMEM_VPP
PC189
C22u6.3X5-HF
PC197
C0.1u25X50402-HF
PU16
PR167
4.99KR1%0402
PC187
C47p50N0402
PC196
C0.1u25X50402-HF
PC199
C22u6.3X5-HF
PC185
C1u25X5-HF
FB_2V5
PR166
2.32KR1%0402-HF
PR163
5.1KR1%0402
VPP_PWRGD
VPP_EN
APL5930QBI-TRG_TDFN10-HF
<8,18,45> PM_SLP_S4#
<18,45> DIMM_ON_VPP
R322
X_0R1%0402
R327
0R1%0402
C286
X_C0.1u25X50402-HF

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Title: **2V5 & 1.8VSUS**

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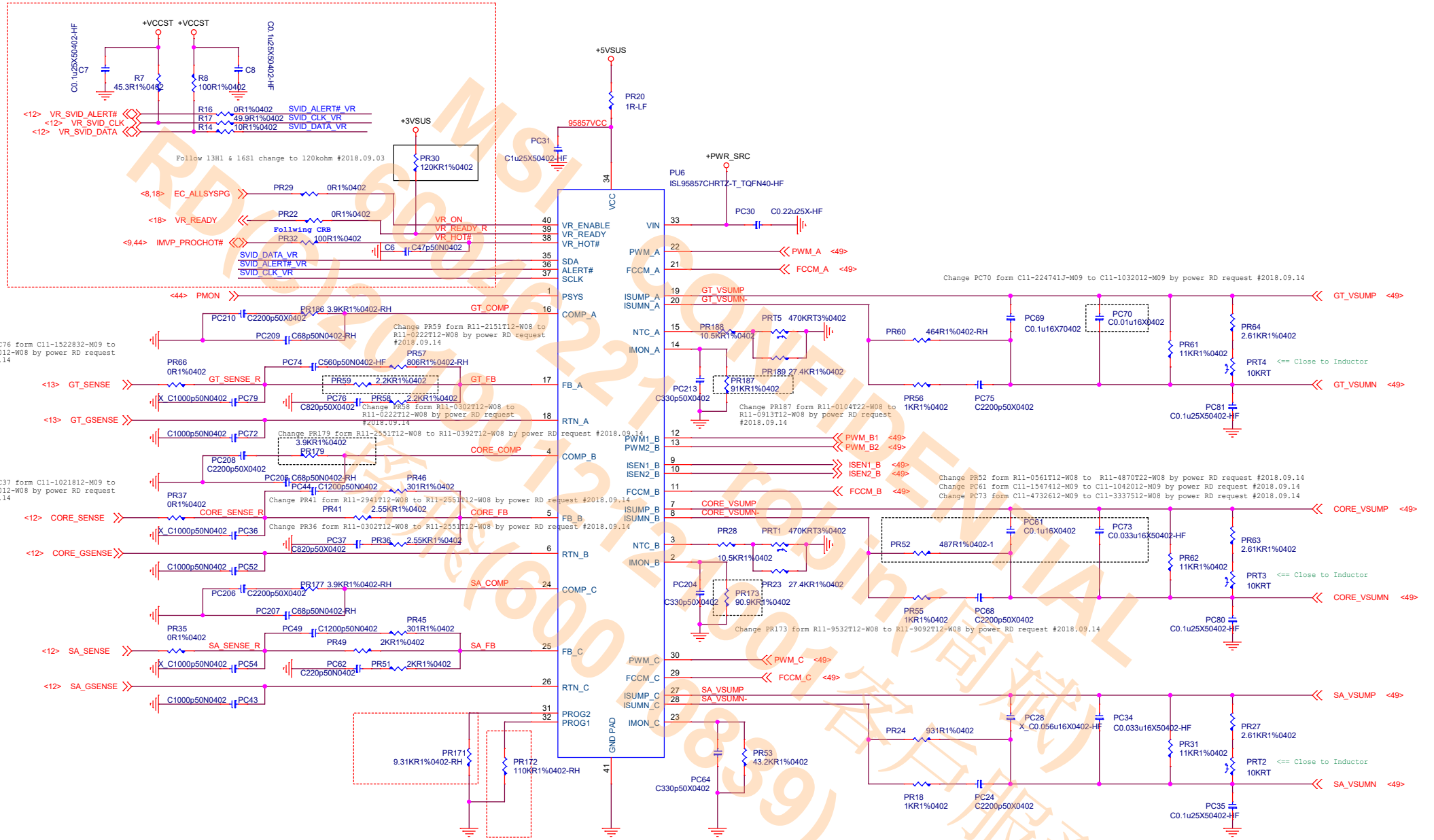
+VCCST +VCCST
C7 C0.1u25X50402-HF
C8 C0.1u25X50402-HF
R7 45.3R1%0402
R8 100R1%0402
<12> VR_SVID_ALERT#
<12> VR_SVID_CLK
<12> VR_SVID_DATA
R16 0R1%0402 SVID_ALERT# VR
R17 49.9R1%0402 SVID_CLK_VR
R14 10R1%0402 SVID_DATA_VR
+3VSUS
PR30 120KR1%0402
Follow 13H1 & 16S1 change to 120kohm #2018.09.03
+5VSUS
PR20 1R-LF
95857VCC
PC31 C1u25X50402-HF
+PWR_SRC
PU6 ISL95857CHRTZ-T_TQFN40-HF
PC30 C0.22u25X-HF
<8,18> EC_ALLSYSPG
PR29 0R1%0402
<18> VR_READY
PR22 0R1%0402
Follwing CRB
<9,44> IMVP_PROCHOT#
PR32 100R1%0402
C6 C47p50N0402
VR_ON
VR_READY_R
VR_HOT#
SVID_DATA_VR
SVID_ALERT# VR
SVID_CLK_VR
VR_ENABLE
VR_READY
VR_HOT#
SDA
ALERT#
SCLK
VCC
GND PAD
VIN
PWM_A
FCCM_A
ISUMP_A
ISUMN_A
NTC_A
IMON_A
PWM1_B
PWM2_B
ISEN1_B
ISEN2_B
FCCM_B
ISUMP_B
ISUMN_B
NTC_B
IMON_B
PWM_C
FCCM_C
ISUMP_C
ISUMN_C
IMON_C
PSYS
COMP_A
FB_A
RTN_A
COMP_B
FB_B
RTN_B
COMP_C
FB_C
RTN_C
PROG2
PROG1
<44> PMON
PR186 3.9KR1%0402-RH
GT_COMP
PC210 C2200p50X0402
PC209 C68p50N0402-RH
Change PR59 form R11-2151T12-W08 to R11-0222T12-W08 by power RD request #2018.09.14
Change PC76 form C11-1522832-M09 to C11-8212012-W08 by power RD request #2018.09.14
PR66 0R1%0402
PR57 806R1%0402-RH
PC74 C560p50N0402-HF
<13> GT_SENSE
GT_SENSE_R
PR59 2.2KR1%0402
GT_FB
X_C1000p50N0402 PC79
PC76 C820p50X0402
PR58 2.2KR1%0402
Change PR58 form R11-0302T12-W08 to R11-0222T12-W08 by power RD request #2018.09.14
<13> GT_GSENSE
C1000p50N0402 PC72
Change PR179 form R11-2551T12-W08 to R11-0392T12-W08 by power RD request #2018.09.14
3.9KR1%0402 PR179
CORE_COMP
PC208 C2200p50X0402
PC205 C68p50N0402-RH
PC44 C1200p50N0402
PR46 301R1%0402
Change PC37 form C11-1021812-M09 to C11-8212012-W08 by power RD request #2018.09.14
PR37 0R1%0402
Change PR41 form R11-2941T12-W08 to R11-2551T12-W08 by power RD request #2018.09.14
<12> CORE_SENSE
CORE_SENSE_R
PR41 2.55KR1%0402
CORE_FB
X_C1000p50N0402 PC36
PC37 C820p50X0402
PR36 2.55KR1%0402
Change PR36 form R11-0302T12-W08 to R11-2551T12-W08 by power RD request #2018.09.14
<12> CORE_GSENSE
C1000p50N0402 PC52
PR177 3.9KR1%0402-RH
SA_COMP
PC206 C2200p50X0402
PC207 C68p50N0402-RH
PR35 0R1%0402
PC49 C1200p50N0402
PR45 301R1%0402
<12> SA_SENSE
SA_SENSE_R
PR49 2KR1%0402
SA_FB
X_C1000p50N0402 PC54
PC62 C220p50N0402
PR51 2KR1%0402
<12> SA_GSENSE
C1000p50N0402 PC43
PR171 9.31KR1%0402-RH
PR172 110KR1%0402-RH
2017/07/19 750KHz
Change PU6 form I32-958572C-I11 to I32-958573C-I11 by power RD request #2018.09.14
Change PR172 form R11-0104T22-W08 to R11-0114T12-W08 by power RD request #2018.09.14
Change PR53 form R11-9762T12-W08 to R11-4322T12-W08 by power RD request #2018.09.14
PR53 43.2KR1%0402
PC64 C330p50X0402
Change PC70 form C11-224741J-M09 to C11-1032012-M09 by power RD request #2018.09.14
PR188 10.5KR1%0402
PR5 470KRT3%0402
PR189 27.4KR1%0402
PC213 C330p50X0402
PR187 91KR1%0402
Change PR187 form R11-0104T22-W08 to R11-0913T12-W08 by power RD request #2018.09.14
PR60 464R1%0402-RH
PC69 C0.1u16X70402
PC70 C0.01u16X0402
PR64 2.61KR1%0402
PR61 11KR1%0402
PRT4 10KRT
<== Close to Inductor
PR56 1KR1%0402
PC75 C2200p50X0402
PC81 C0.1u25X50402-HF
GT_VSUMP <49>
GT_VSUMN <49>
PWM_A <49>
FCCM_A <49>
PWM_B1 <49>
PWM_B2 <49>
ISEN1_B <49>
ISEN2_B <49>
FCCM_B <49>
Change PR52 form R11-0561T12-W08 to R11-4870T22-W08 by power RD request #2018.09.14
Change PC61 form C11-1547412-M09 to C11-1042012-M09 by power RD request #2018.09.14
Change PC73 form C11-4732612-M09 to C11-3337512-W08 by power RD request #2018.09.14
PR28 10.5KR1%0402
PRT1 470KRT3%0402
PR23 27.4KR1%0402
PC204 C330p50X0402
PR173 90.9KR1%0402
Change PR173 form R11-9532T12-W08 to R11-9092T12-W08 by power RD request #2018.09.14
PR52 487R1%0402-1
PC61 C0.1u16X0402
PC73 C0.033u16X50402-HF
PR63 2.61KR1%0402
PR62 11KR1%0402
PRT3 10KRT
PR55 1KR1%0402
PC68 C2200p50X0402
PC80 C0.1u25X50402-HF
CORE_VSUMP <49>
CORE_VSUMN <49>
PR24 931R1%0402
PC28 X_C0.056u16X0402-HF
PC34 C0.033u16X50402-HF
PR27 2.61KR1%0402
PR31 11KR1%0402
PRT2 10KRT
PR18 1KR1%0402
PC24 C2200p50X0402
PC35 C0.1u25X50402-HF
SA_VSUMP <49>
SA_VSUMN <49>
MICRO-STAR INT'L CO.,LTD.
Title
+VCC_CORE(1)
Size Custom
Document Number MS-14B3
Rev 0A
Date: Monday, October 01, 2018
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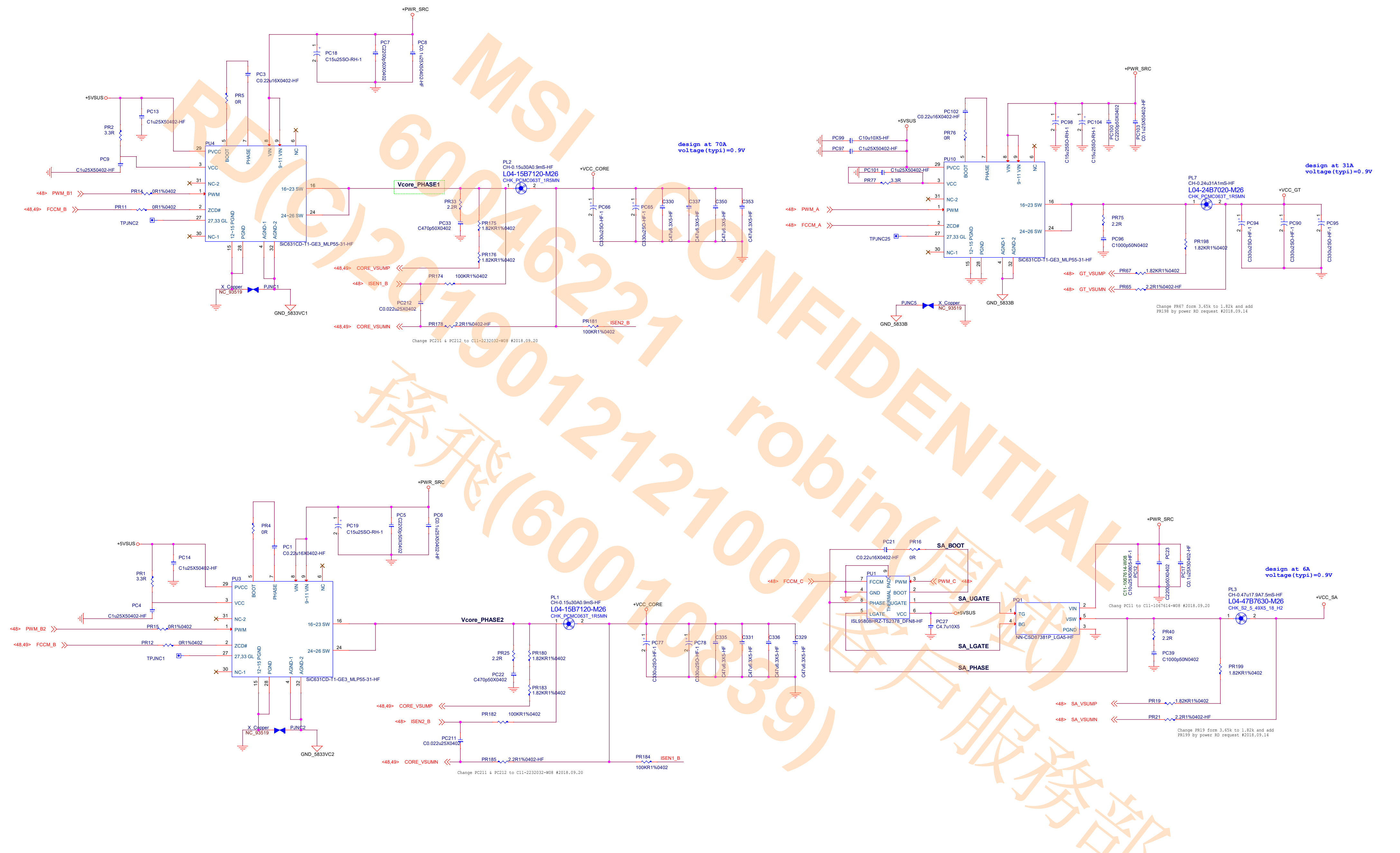
design at 70A
voltage(typi)=0.9V
design at 31A
voltage(typi)=0.9V
design at 6A
voltage(typi)=0.9V
Vcore_PHASE1
Vcore_PHASE2
SiC631CD-T1-GE3_MLP55-31-HF
ISL95808HRZ-TS2378_DFN8-HF
NN-CSD87381P_LGA5-HF
L04-15B7120-M26
L04-24B7020-M26
L04-47B7630-M26
+PWR_SRC
+5VSUS
+VCC_CORE
+VCC_GT
+VCC_SA
CORE_VSUMP
CORE_VSUMN
ISEN1_B
ISEN2_B
GT_VSUMP
GT_VSUMN
SA_VSUMP
SA_VSUMN
SA_BOOT
SA_UGATE
SA_LGATE
SA_PHASE
PWM_A
PWM_B1
PWM_B2
PWM_C
FCCM_A
FCCM_B
FCCM_C
Change PC211 & PC212 to C11-2232032-W08 #2018.09.20
Change PR67 form 3.65k to 1.82k and add PR198 by power RD request #2018.09.14
Chang PC11 to C11-1067614-W08 #2018.09.20
Change PR19 form 3.65k to 1.82k and add PR199 by power RD request #2018.09.14

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Title: +VCC_CORE(2)

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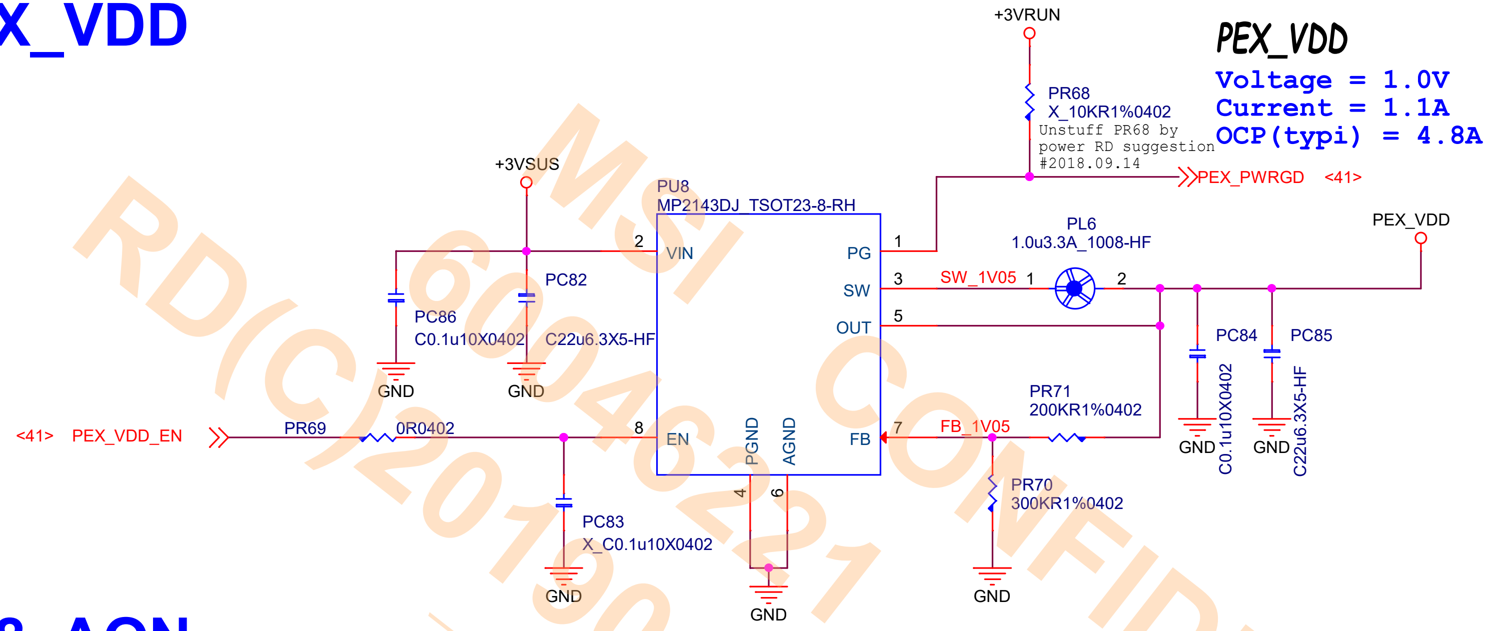
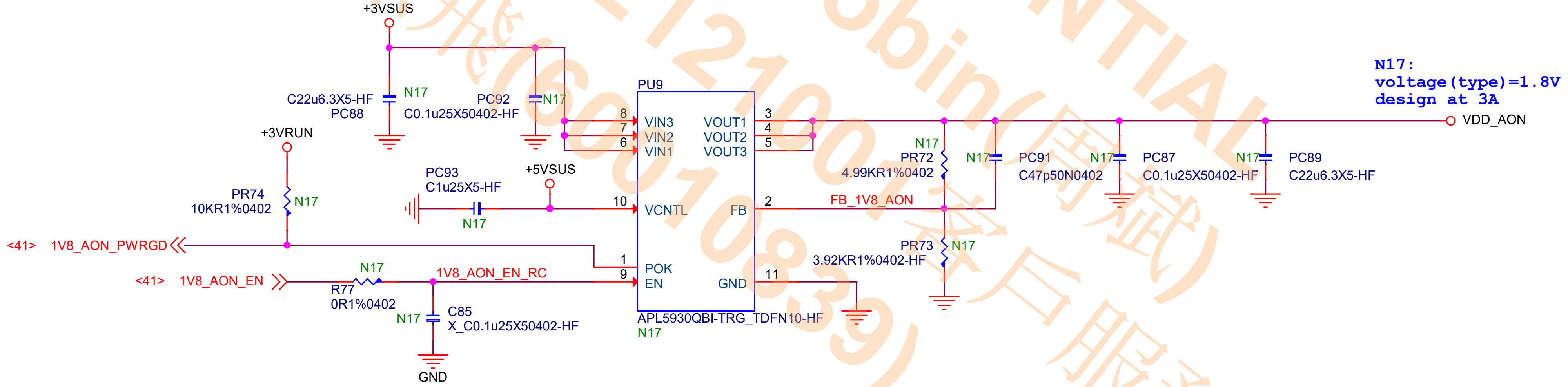
PEX_VDD


+3VRUN
PR68
X_10KR1%0402
Unstuff PR68 by power RD suggestion #2018.09.14
PEX_PWRGD <41>
PEX_VDD
Voltage = 1.0V
Current = 1.1A
OCP(typi) = 4.8A
+3VSUS
PU8
MP2143DJ_TSOT23-8-RH
VIN
PG
SW
OUT
EN
FB
PGND
AGND
PL6
1.0u3.3A_1008-HF
SW_1V05
PC82
C22u6.3X5-HF
PC86
C0.1u10X0402
PC84
C0.1u10X0402
PC85
C22u6.3X5-HF
PR71
200KR1%0402
FB_1V05
PR70
300KR1%0402
<41> PEX_VDD_EN
PR69
0R0402
PC83
X_C0.1u10X0402
GND

1V8_AON


+3VSUS
C22u6.3X5-HF
PC88
PC92
C0.1u25X50402-HF
N17
PU9
VIN3
VIN2
VIN1
VOUT1
VOUT2
VOUT3
VCNTL
FB
POK
EN
GND
APL5930QBI-TRG_TDFN10-HF
N17:
voltage(type)=1.8V
design at 3A
VDD_AON
PR72
4.99KR1%0402
PC91
C47p50N0402
PC87
C0.1u25X50402-HF
PC89
C22u6.3X5-HF
FB_1V8_AON
PR73
3.92KR1%0402-HF
+3VRUN
PR74
10KR1%0402
PC93
C1u25X5-HF
+5VSUS
<41> 1V8_AON_PWRGD
<41> 1V8_AON_EN
R77
0R1%0402
1V8_AON_EN_RC
C85
X_C0.1u25X50402-HF
GND

MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER PEX_VDD/1V8_AON

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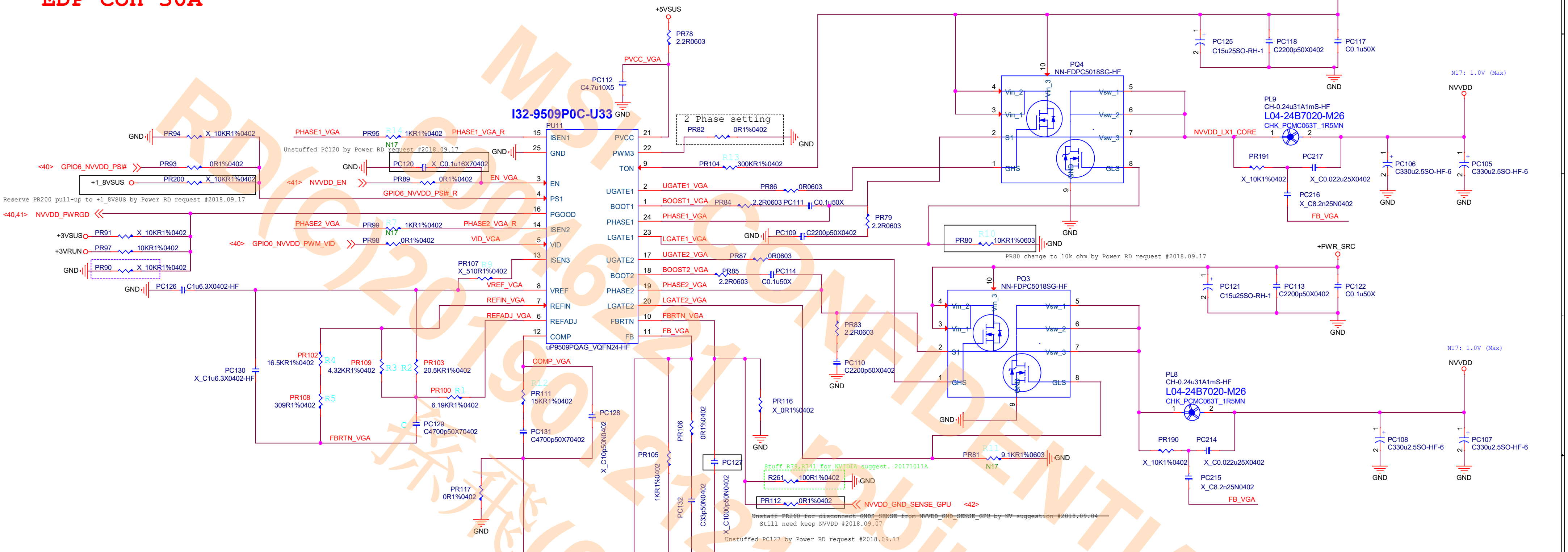
DGPU POWER NVVDD

CONFIG A
VBoot: N17S-0.8V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 60.4A
EDP-Con 30A



CONFIG	R1	R2	R3	R4	R5	C
N17S-G1	6.19KR1%	20.5KR1%	4.32KR1%	16.5KR1%	309R1%	4.7nF

CONFIG	R6	R7	R8	R9	R10	R11	R12	R13	R14
N17S-G1	NC	1KR1%	NC	NC	20KR1%	9.1KR1%	15KR1%	300KR1%	1KR1%

N17

- N17R1 **R1** X_6.19KR1%0402 R11-6191T12-W08 N17
- N17R2 **R2** X_20.5KR1%0402 R11-2052T12-W08 N17
- N17R3 **R3** X_4.32KR1%0402 R11-4321T12-W08 N17
- N17R4 **R4** X_16.5KR1%0402 R11-1652T12-W08 N17
- N17R5 **R5** X_309R1%0402 R11-3090T12-R01 N17
- CA **C** X_C4700p50X70402 C11-4722812-M09 N17
- PWM1 **PWM** X_uP9509PQAG_VQFN24-HF I32-9509P0C-U33 N17
- N17R12 **R12** X_15KR1%0402 R11-0153T12-W08 N17
- N17R13 **R13** X_300KR1%0402 R11-0304T12-W08 N17

190.Change R1A name to N17R1 for BOM. 20171127.
191.Change R1B name to N16R1 for BOM. 20171127.
192.Change R2A name to N17R2 for BOM. 20171127.
193.Change R2B name to N16R2 for BOM. 20171127.
194.Change R3A name to N17R3 for BOM. 20171127.
195.Change R3B name to N16R3 for BOM. 20171127.
190.Change R4A name to N17R4 for BOM. 20171127.
191.Change R4B name to N16R4 for BOM. 20171127.
192.Change R5A name to N17R5 for BOM. 20171127.
193.Change R5B name to N16R5 for BOM. 20171127.
194.Change R12A name to N17R12 for BOM. 20171127.
195.Change R12B name to N16R12 for BOM. 20171127.
194.Change R13A name to N17R13 for BOM. 20171127.
195.Change R13B name to N16R13 for BOM. 20171127.

234.Change N16R13 P/N from R11-0913T12-W08 to R11-0683T12-W08 for Power. 20180109

Remover N16 BOM option #2018.09.20

以後注意 Option 的 Location 不要跟其他 Location 撞到的，因為程式不會分 A/B。

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Title: DGPU POWER NVVDD

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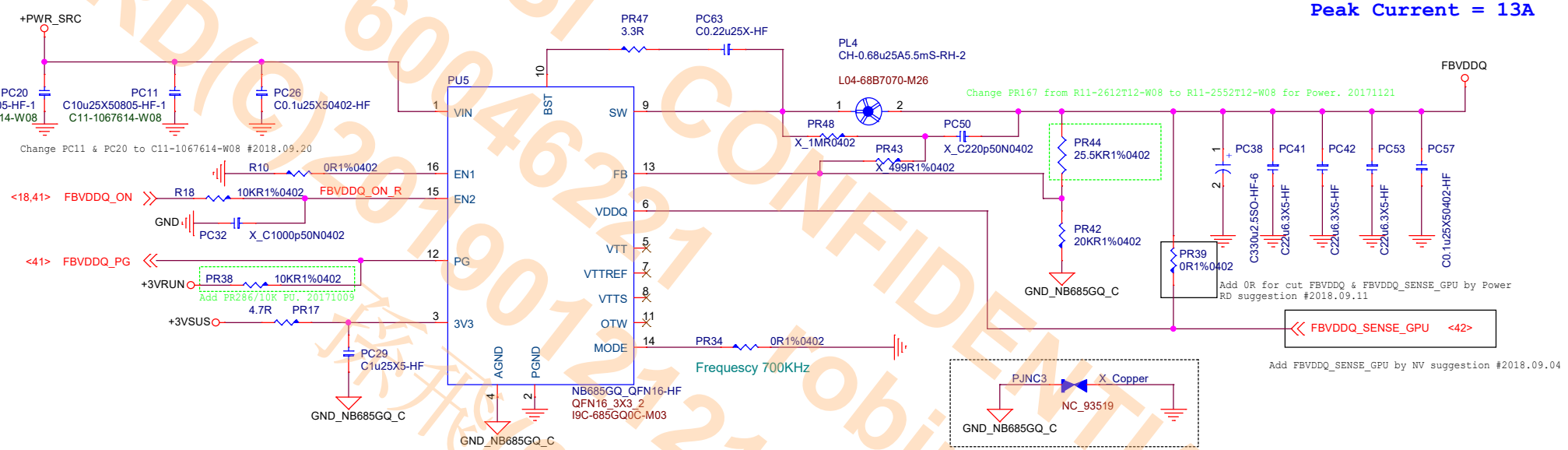
FBVDDQ POWER



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU POWER FBVDDQ		
Size: Custom	Document Number: MS-14B3	Rev: 0A
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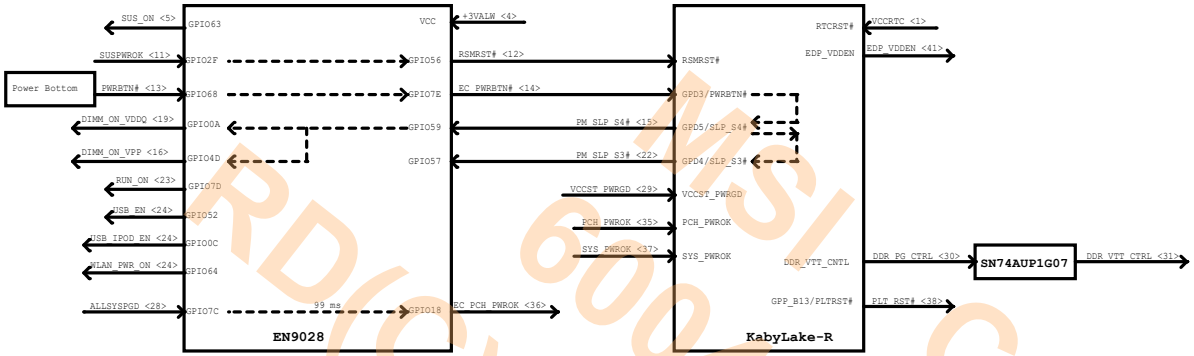
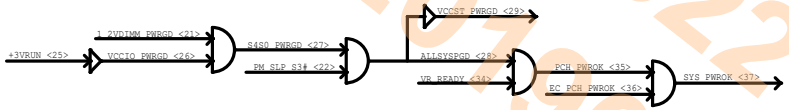
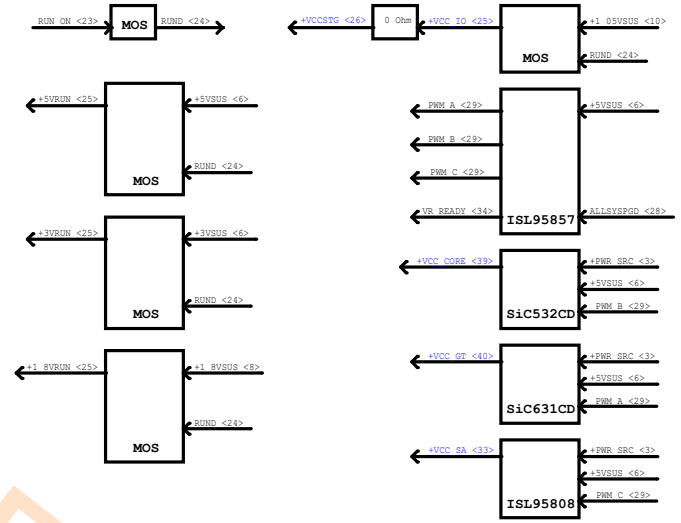
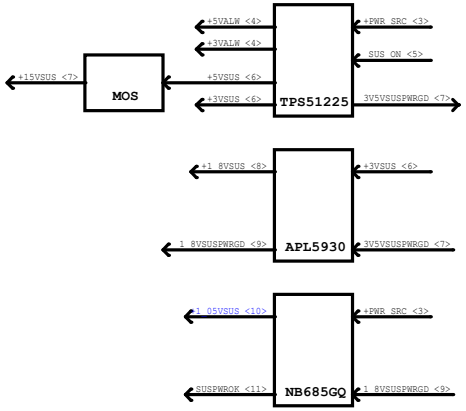




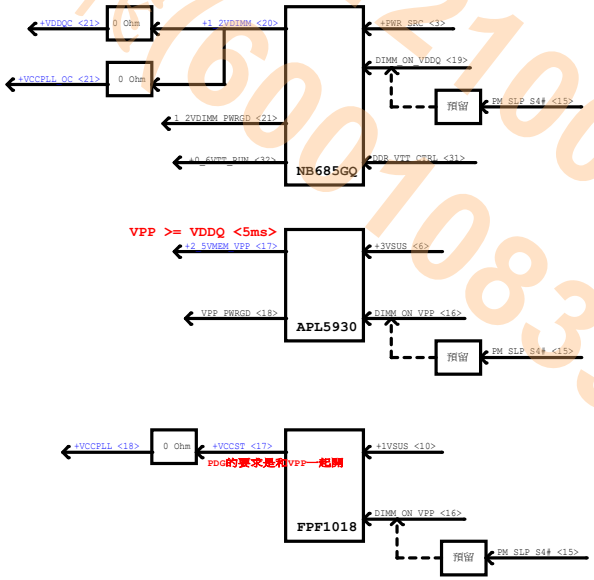
S0

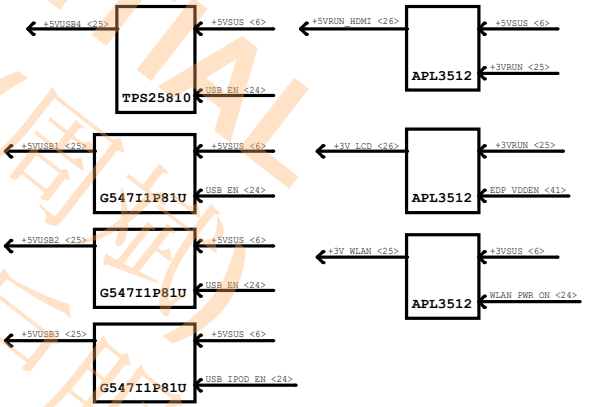


S4/S5



S3





MICRO-STAR INT'L CO.,LTD.

Title: Power on Block Diagram

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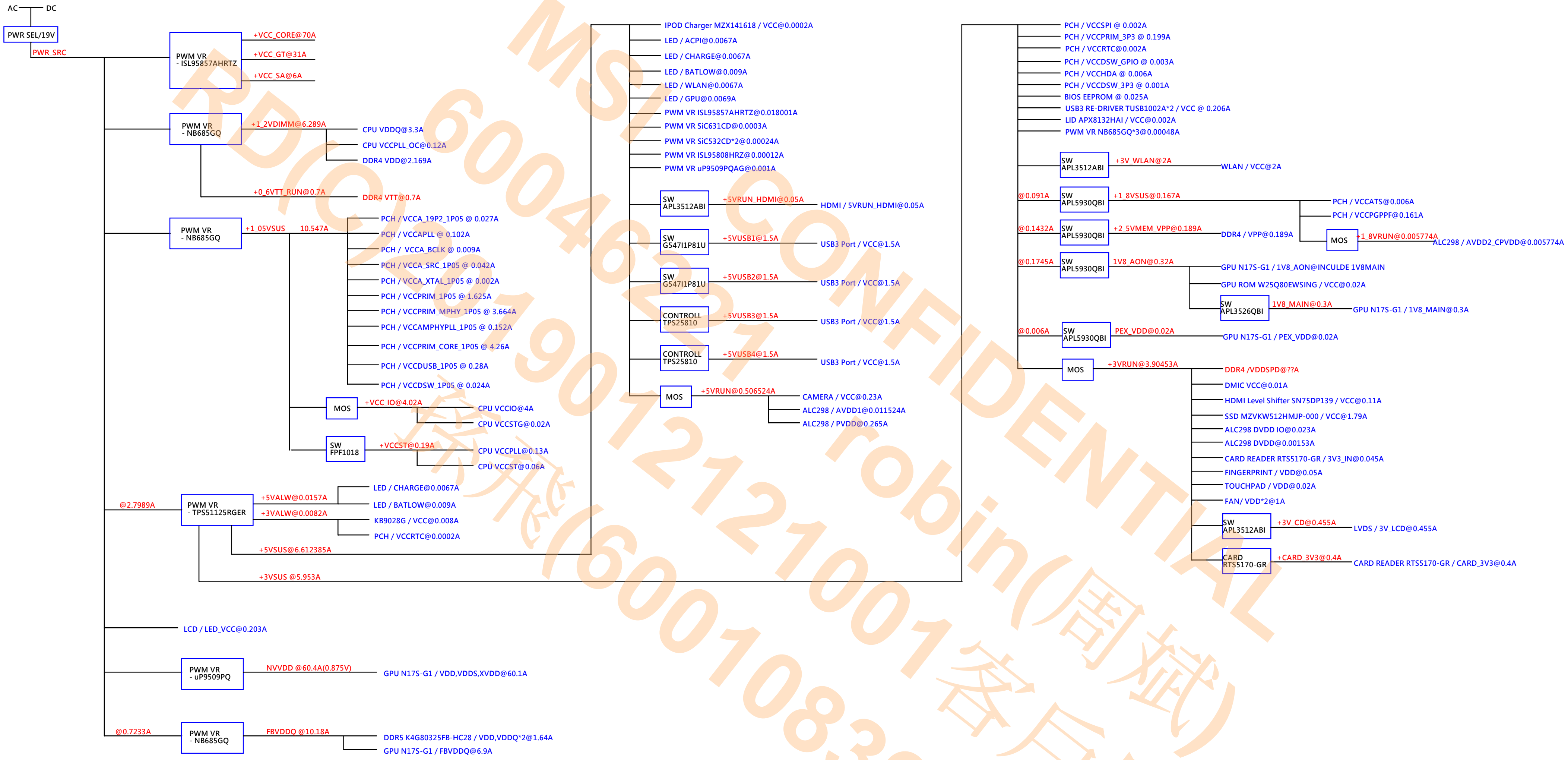
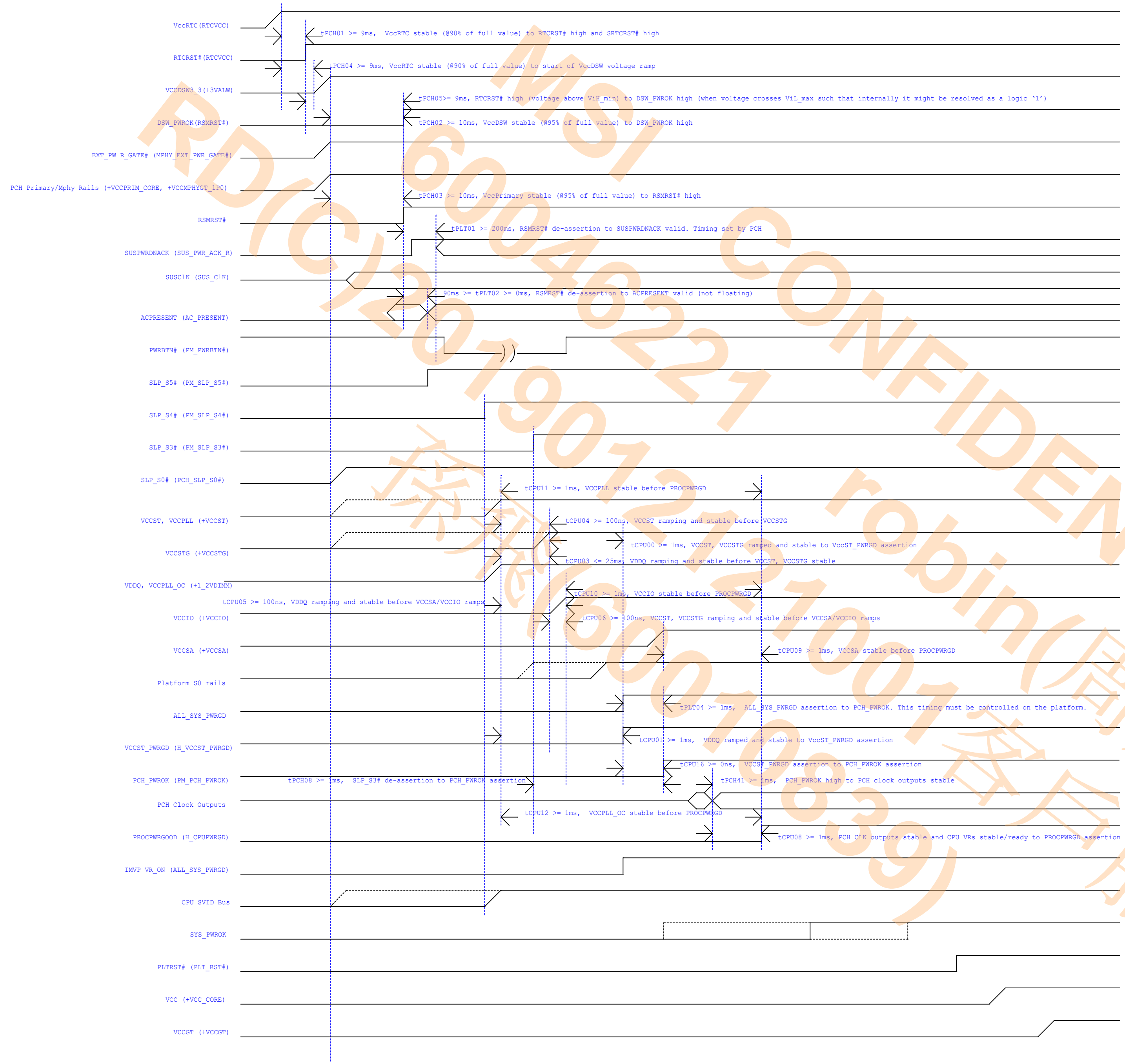
14B3 Power Delivery Chart


AC
DC
PWR SEL/19V
PWR_SRC
PWM VR - ISL95857AHRTZ
+VCC_CORE@70A
+VCC_GT@31A
+VCC_SA@6A
PWM VR - NB685GQ
+1_2VDIMM@6.289A
CPU VDDQ@3.3A
CPU VCCPLL_OC@0.12A
DDR4 VDD@2.169A
+0_6VTT_RUN@0.7A
DDR4 VTT@0.7A
PWM VR - NB685GQ
+1_05VSUS
10.547A
PCH / VCCA_19P2_1P05 @ 0.027A
PCH / VCCAPLL @ 0.102A
PCH / VCCA_BCLK @ 0.009A
PCH / VCCA_SRC_1P05 @ 0.042A
PCH / VCCA_XTAL_1P05 @ 0.002A
PCH / VCCPRIM_1P05 @ 1.625A
PCH / VCCPRIM_MPHY_1P05 @ 3.664A
PCH / VCCAMPHYPLL_1P05 @ 0.152A
PCH / VCCPRIM_CORE_1P05 @ 4.26A
PCH / VCCDUSB_1P05 @ 0.28A
PCH / VCCDSW_1P05 @ 0.024A
MOS
+VCC_IO@4.02A
CPU VCCIO@4A
CPU VCCSTG@0.02A
SW FPF1018
+VCCST@0.19A
CPU VCCPLL@0.13A
CPU VCCST@0.06A
@2.7989A
PWM VR - TPS51125RGER
+5VALW@0.0157A
+3VALW@0.0082A
LED / CHARGE@0.0067A
LED / BATLOW@0.009A
KB9028G / VCC@0.008A
PCH / VCCRTC@0.0002A
+5VSUS@6.612385A
+3VSUS @5.953A
LCD / LED_VCC@0.203A
PWM VR - uP9509PQ
NVVDD @60.4A(0.875V)
GPU N17S-G1 / VDD,VDDS,XVDD@60.1A
@0.7233A
PWM VR - NB685GQ
FBVDDQ @10.18A
DDR5 K4G80325FB-HC28 / VDD,VDDQ*2@1.64A
GPU N17S-G1 / FBVDDQ@6.9A
IPOD Charger MZX141618 / VCC@0.0002A
LED / ACPI@0.0067A
LED / CHARGE@0.0067A
LED / BATLOW@0.009A
LED / WLAN@0.0067A
LED / GPU@0.0069A
PWM VR ISL95857AHRTZ@0.018001A
PWM VR SiC631CD@0.0003A
PWM VR SiC532CD*2@0.00024A
PWM VR ISL95808HRZ@0.00012A
PWM VR uP9509PQAG@0.001A
SW APL3512ABI
+5VRUN_HDMI@0.05A
HDMI / 5VRUN_HDMI@0.05A
SW G547I1P81U
+5VUSB1@1.5A
USB3 Port / VCC@1.5A
SW G547I1P81U
+5VUSB2@1.5A
USB3 Port / VCC@1.5A
CONTROLL TPS25810
+5VUSB3@1.5A
USB3 Port / VCC@1.5A
CONTROLL TPS25810
+5VUSB4@1.5A
USB3 Port / VCC@1.5A
MOS
+5VRUN@0.506524A
CAMERA / VCC@0.23A
ALC298 / AVDD1@0.011524A
ALC298 / PVDD@0.265A
PCH / VCCSPI @ 0.002A
PCH / VCCPRIM_3P3 @ 0.199A
PCH / VCCRTC@0.002A
PCH / VCCDSW_GPIO @ 0.003A
PCH / VCCHDA @ 0.006A
PCH / VCCDSW_3P3 @ 0.001A
BIOS EEPROM @ 0.025A
USB3 RE-DRIVER TUSB1002A*2 / VCC @ 0.206A
LID APX8132HAI / VCC@0.002A
PWM VR NB685GQ*3@0.00048A
SW APL3512ABI
+3V_WLAN@2A
WLAN / VCC@2A
@0.091A
SW APL5930QBI
+1_8VSUS@0.167A
PCH / VCCATS@0.006A
PCH / VCCPGPPF@0.161A
@0.1432A
SW APL5930QBI
+2_5VMEM_VPP@0.189A
DDR4 / VPP@0.189A
MOS
+1_8VRUN@0.005774A
ALC298 / AVDD2_CPVDD@0.005774A
@0.1745A
SW APL5930QBI
1V8_AON@0.32A
GPU N17S-G1 / 1V8_AON@INCULDE 1V8MAIN
GPU ROM W25Q80EWSING / VCC@0.02A
SW APL3526QBI
1V8_MAIN@0.3A
GPU N17S-G1 / 1V8_MAIN@0.3A
@0.006A
SW APL5930QBI
PEX_VDD@0.02A
GPU N17S-G1 / PEX_VDD@0.02A
MOS
+3VRUN@3.90453A
DDR4 /VDDSPD@??A
DMIC VCC@0.01A
HDMI Level Shifter SN75DP139 / VCC@0.11A
SSD MZVKW512HMJP-000 / VCC@1.79A
ALC298 DVDD IO@0.023A
ALC298 DVDD@0.00153A
CARD READER RTS5170-GR / 3V3_IN@0.045A
FINGERPRINT / VDD@0.05A
TOUCHPAD / VDD@0.02A
FAN/ VDD*2@1A
SW APL3512ABI
+3V_CD@0.455A
LVDS / 3V_LCD@0.455A
CARD RTS5170-GR
+CARD_3V3@0.4A
CARD READER RTS5170-GR / CARD_3V3@0.4A

G3 to S0



VccRTC(RTCVCC)
tPCH01 >= 9ms, VccRTC stable (@90% of full value) to RTCRST# high and SRTCRST# high
RTCRST#(RTCVCC)
tPCH04 >= 9ms, VccRTC stable (@90% of full value) to start of VccDSW voltage ramp
VCCDSW3_3(+3VALW)
tPCH05>= 9ms, RTCRST# high (voltage above ViH_min) to DSW_PWROK high (when voltage crosses ViL_max such that internally it might be resolved as a logic '1')
DSW_PWROK(RSMRST#)
tPCH02 >= 10ms, VccDSW stable (@95% of full value) to DSW_PWROK high
EXT_PW R_GATE# (MPHY_EXT_PWR_GATE#)
PCH Primary/Mphy Rails (+VCCPRIM_CORE, +VCCMPHYGT_1P0)
tPCH03 >= 10ms, VccPrimary stable (@95% of full value) to RSMRST# high
RSMRST#
tPLT01 >= 200ms, RSMRST# de-assertion to SUSPWRDNACK valid. Timing set by PCH
SUSPWRDNACK (SUS_PWR_ACK_R)
SUSClK (SUS_ClK)
90ms >= tPLT02 >= 0ms, RSMRST# de-assertion to ACPRESENT valid (not floating)
ACPRESENT (AC_PRESENT)
PWRBTN# (PM_PWRBTN#)
SLP_S5# (PM_SLP_S5#)
SLP_S4# (PM_SLP_S4#)
SLP_S3# (PM_SLP_S3#)
SLP_S0# (PCH_SLP_S0#)
tCPU11 >= 1ms, VCCPLL stable before PROCPWRGD
VCCST, VCCPLL (+VCCST)
tCPU04 >= 100ns, VCCST ramping and stable before VCCSTG
tCPU00 >= 1ms, VCCST, VCCSTG ramped and stable to VccST_PWRGD assertion
VCCSTG (+VCCSTG)
tCPU03 <= 25ms, VDDQ ramping and stable before VCCST, VCCSTG stable
VDDQ, VCCPLL_OC (+1_2VDIMM)
tCPU10 >= 1ms, VCCIO stable before PROCPWRGD
tCPU05 >= 100ns, VDDQ ramping and stable before VCCSA/VCCIO ramps
VCCIO (+VCCIO)
tCPU06 >= 100ns, VCCST, VCCSTG ramping and stable before VCCSA/VCCIO ramps
VCCSA (+VCCSA)
tCPU09 >= 1ms, VCCSA stable before PROCPWRGD
Platform S0 rails
tPLT04 >= 1ms, ALL_SYS_PWRGD assertion to PCH_PWROK. This timing must be controlled on the platform.
ALL_SYS_PWRGD
tCPU01 >= 1ms, VDDQ ramped and stable to VccST_PWRGD assertion
VCCST_PWRGD (H_VCCST_PWRGD)
tCPU16 >= 0ns, VCCST_PWRGD assertion to PCH_PWROK assertion
PCH_PWROK (PM_PCH_PWROK)
tPCH08 >= 1ms, SLP_S3# de-assertion to PCH_PWROK assertion
tPCH41 >= 1ms, PCH_PWROK high to PCH clock outputs stable
PCH Clock Outputs
tCPU12 >= 1ms, VCCPLL_OC stable before PROCPWRGD
PROCPWRGOOD (H_CPUPWRGD)
tCPU08 >= 1ms, PCH CLK outputs stable and CPU VRs stable/ready to PROCPWRGD assertion
IMVP VR_ON (ALL_SYS_PWRGD)
CPU SVID Bus
SYS_PWROK
PLTRST# (PLT_RST#)
VCC (+VCC_CORE)
VCCGT (+VCCGT)

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Title	G3 into S0 without M	
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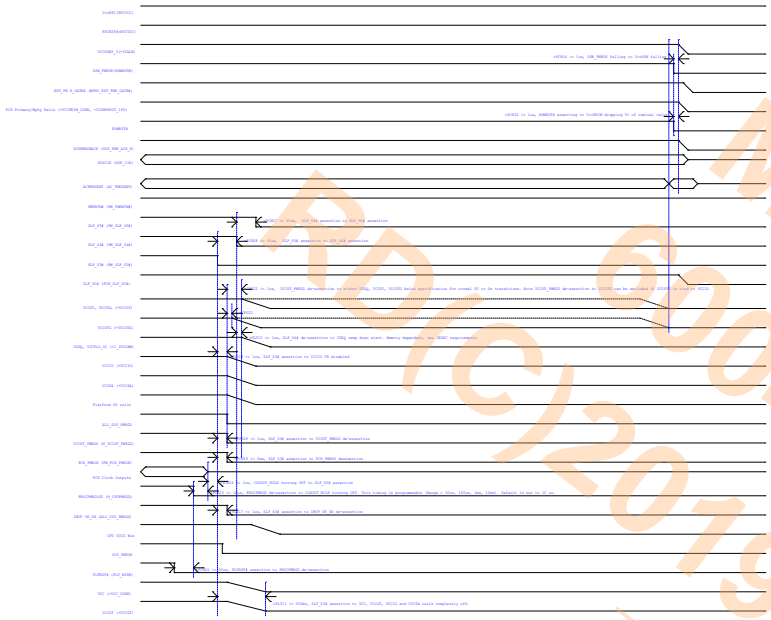
S0 to G3



MICRO-STAR INT'L CO.,LTD.		
Title: S0 into G3 without M		
Size: A	Document Number: MS-14B3	Rev: 0A
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1. Page.31 Change Charge_LED#/BATLOW_LED# pull up to +5VALW #2018.08.09
2. Page.8/12 Remove SLP_S0# function, 14B3 did not support #2018.08.09
3. Page.12 Remove RUN_ON_C10 control, 14B3 did not support #2018.08.09
4. Page.18 Follow 16S1 to change control logic with RUN_ON #2018.08.09
5. Page.18 Change netname from ACPI_LED# to POWER_LED# #2018.08.09

6. Page.29 Follow 16S1 reserve I2C SMbus for TP #2018.08.10
7. Page.8 Follow 14B1 reserve R657 for CFG_UMA sku. #2018.08.10
8. Page.8 Follow 13H1 reserve MB ID[0:3] #2018.08.10
9. Page.27/28 Follow 13H1 add short protection circuit on USB Type-C RX #2018.08.10
10.Page.45 Add +VCCSTG power combine with +VCC_IO (follow 13H1) #2018.08.10
11.Page.45 Reserve +VCCSTG power combine with +VCCST (follow 16S1) #2018.08.10
12.Page.45 Follow 13H1 reserve control signal RUN_ON for +VCCST #2018.08.10

13.Page.7 Add Pull-up R5318 for PCIE_CLK_WLAN_REQ# #2018.08.13
14.Page.23 Add TPM page #2018.08.13
15.Page.18 Change DGPU_PWRGD to GPIO5D #2018.08.13
16.Page.18 EC recommend remove EX-XTAL #2018.08.13

17.Page.25 Change USB3.1 re-driver from 1002 to 1002A(Follow13H1) #2018.08.14
18.Page.18 Add USB_1002_EN on GPIO5E #2018.08.14

19.Page.17 DP139 VCC side add bulk cap by vendor suggest #2018.08.15
20.Page.3 Remove Pull-Down R5153, page.17 have reserve same pull-down #2018.08.15
21.Page.18 Add Pull-up R102 for KBRST# (follow 13H1) #2018.08.15
22.Page.23 Add Pull-up Resistor for USB_1002_EN by EC suggestion #2018.08.15
23.Page.7 Follow PDG(P.294) reserve capacitor to GND for EMI issue #2018.08.15
24.Page.9 Follow 14B1 change HDA R/C value for SA #2018.08.15
25.Page.18 Remove PCH_PWROK pull-down resistor, page.8 have pull-down 10Kohm #2018.08.15
26.Page.19 Add OR0402 for SATA M.2 #2018.08.15
27.Page.20 Add AC coupling capacitor for PCIE GEN2 #2018.08.15

28.Page.44-52 Combine power change for improve power loadline #2018.08.16

29.Page.23 Add resistor 0ohm and place on T-routing via side #2018.08.20
30.Page.23 Reserve capacitance and place on TPM side for SA issue #2018.08.20

31.Page.6 Follow 14B1 to change location for placement #2018.08.22

32.Page.7 Follow PDG change BIAS R from 10M 5% to 10M 1% #2018.08.23
33.Page.12 Add Reserve Cap, refer to PDG 575412 Table 11-2 #2018.08.23

34.Page.8/9/11/20 Add CNVi function by PM request #2018.08.24
~~35.Page.7 Reserve RTC_RST# discharge circuit #2018.08.24~~

35. Combine layout team re-name location on CPU side #2018.08.28
36.Page.20 Change R5344 from 0805 to 1206 for CNVi GEN2 (2A) #2018.08.28

37.Page.08 Follow MOW Table 5-1 change R7042 & R7034 from 75 to 33ohm #2018.08.29

38.Page.20 Follow PDG add 10uF+0.01uF #2018.08.30
39.Page.33 Not Staff R5040 & staff R5039 by NV comment #2018.08.30
40.Page.33 Change to VDD_AON by NV comment #2018.08.30
41.Page.42 Add 22u for VRAM by NV comment #2018.08.30
42. Remove N16 co-design portion #2018.08.30

43.Page.20 Change R5344 connnect to +3V_WLAN #2018.09.03
44.Page.18 Follow 13H1 & 16S1 add buffer IC on VR_READY #2018.09.03

~~45.Page.51 Unstaff PR260 for disconnect GNDS_SENSE from MVVDD_GND_SENSE_GPU by NV suggestion #2018.09.04~~
~~46.Page.51 Unstaff PR248 for disconnect VDDS_SENSE from MVVDD_SENSE_GPU by NV suggestion #2018.09.04~~
47.Page.42/52 Add FBVDDQ_SENSE_GPU by NV suggestion #2018.09.04
48.Page.10 Change USB3.1 port1/2/3/4 order for layout #2018.09.04

49.Page.46 Follow 13H1 Add S3 # for shutdown timing TPLT18 #2018.09.05
50.Page.46 Reserve Cap for PM_S3_CNTRL time delay after RUND #2018.09.05
51.Page.27 Delete ESD18 and change USB3_RXN_TYPEC1_U_C/USB3_RXP_TYPEC1_U_C link ESD16 for Layout. #2018.09.05
52.Page.28 Delete ESD30 and change USB3_RXN_TYPEC3_C/USB3_RXP_TYPEC3_C link ESD28 for Layout. #2018.09.05
53.Page.28 Delete ESD31 and change USB3_RXN_TYPEC4_C/USB3_RXP_TYPEC4_C link ESD28 for Layout. #2018.09.05
54.Page.28 Swap USB3_RXP_TYPEC3_C/USB3_RXN_TYPEC3_C by layout request #2018.09.05
55.Page.28 Swap USB3_RXP_TYPEC4_C/USB3_RXN_TYPEC4_C by layout request #2018.09.05

56.Page.32 Delete UME1 for thermal solution change #2018.09.06

57.Page.42 Disconnect VDDS_SENSE/GNDS_SENSE link to VDD_SENSE/GND_SENSE by NV suggestion #2018.09.07
58.Page.14 Follow PDG Table11-4, add decoupling 1uF 020I for PCH power rail #2018.09.07

59.Page.52 Add 0R for cut FBVDDQ & FBVDDQ_SENSE_GPU by Power RD suggestion #2018.09.11

60.Page.38 Set NV_Strap 0xA as default for Hynix H5GC8H24AJR-R2C #2018.09.12

61. Layout Re-name by layout request #2018.09.13
62. Change R0402 PCB footprint to MOM type : EC14,R454,R201,R197,R192,R311,R463,PR30,R438,R305,R437
63.Page.7 Follow 16S1 0B add discharge circuit on SRTC_RST & RTC_RST #2018.09.13
64.Page.21 Add JNC5 by vender suggestion #2018.09.13

65.Page.49 Change PR67 form 3.65k to 1.82k and add PR198 by power RD request #2018.09.14
66.Page.49 Change PR19 form 3.65k to 1.82k and add PR199 by power RD request #2018.09.14
67.Page.48 Change PU6 form 132-958572C-I11 to 132-958573C-I11 by power RD request #2018.09.14
68.Page.48 Change PR59 form R11-2151T12-W08 to R11-0222T12-W08 by power RD request #2018.09.14
69.Page.48 Change PR187 form R11-0104T22-W08 to R11-0913T12-W08 by power RD request #2018.09.14
69.Page.48 Change PR58 form R11-0302T12-W08 to R11-0222T12-W08 by power RD request #2018.09.14
70.Page.48 Change PR179 form R11-2551T12-W08 to R11-0392T12-W08 by power RD request #2018.09.14
71.Page.48 Change PR41 form R11-2941T12-W08 to R11-2551T12-W08 by power RD request #2018.09.14
72.Page.48 Change PR36 form R11-0302T12-W08 to R11-2551T12-W08 by power RD request #2018.09.14
73.Page.48 Change PR52 form R11-0561T12-W08 to R11-4870T22-W08 by power RD request #2018.09.14
74.Page.48 Change PR173 form R11-9532T12-W08 to R11-9092T12-W08 by power RD request #2018.09.14
75.Page.48 Change PR172 form R11-0104T22-W08 to R11-0114T12-W08 by power RD request #2018.09.14
76.Page.48 Change PR53 form R11-9762T12-W08 to R11-4322T12-W08 by power RD request #2018.09.14
77.Page.48 Change PC70 form C11-224741J-M09 to C11-1032012-M09 by power RD request #2018.09.14
78.Page.48 Change PC76 form C11-1522832-M09 to C11-8212012-W08 by power RD request #2018.09.14
79.Page.48 Change PC61 form C11-1547412-M09 to C11-1042012-M09 by power RD request #2018.09.14
80.Page.48 Change PC73 form C11-4732612-M09 to C11-3337512-W08 by power RD request #2018.09.14
81.Page.48 Change PC37 form C11-1021812-M09 to C11-8212012-W08 by power RD request #2018.09.14
82.Page.50 Unstuff PR68 by power RD suggestion #2018.09.14
83.Page.25 Change USB3.1 Redriver to initial EQ/VOD setting by vender suggestion #2018.09.14

84.Page.32 Reserve +5VSUS 0402 0.1u cap *3 to GND by EMI request #2018.09.17
85.Page.32 Reserve +3VRUN 0402 0.1u cap *1 to GND by EMI request #2018.09.17
86.Page.51 PR80 change to 10k ohm by Power RD request #2018.09.17
87.Page.51 Unstuffed PC127 by Power RD request #2018.09.17
88.Page.51 Unstuffed PC120 by Power RD request #2018.09.17
89.Page.51 Reserve PR200 pull-up to +1_8VSUS by Power RD request #2018.09.17
90.Page.46 Change PC169, PC179, PC184 from 120uF to 150uF(C71-151061G-S03) by power RD request #2018.09.17

91.Page.32 Change CPU & GPU stand off to 16S1 type by ME request #2018.09.18

92.Page.51 Remover N16 BOM option #2018.09.20
93.Page.46/49 Change C238, PC211 & PC212 to C11-2232032-W08 #2018.09.20
94. Change PC11, PC12, PC20, PC150, PC178, PC190, PC191, PC192 to C11-1067614-W08 #2018.09.20
95.Page.38 Change Y2 to D04-1107400-F07 because main source was phase out #2018.09.20

96.Page.24 U9 change USB_EN to USB_IPOD_EN for IPOD charger by EC request #2018.09.21

97.Page.20 Staff R320 for PCIe module #2018.09.27
98.Page.20 Stuff U36 and unstuff R313 for PCIe module #2018.09.27

100.Page29. Stuff R503 & R505, unstuffed R502 & R504 to change TP protocal from I2C to SMBUS by vendor request #2018.10.01

271.Add E2P-4B12611-Y42 *1,E2P-4B12511-Y42*2
for UMA sku by ME. 20180712
272.Add E2B-13F2020-A89 *1 for UMA Sku by ME. 20180713

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