TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Control/MISC/CFG,CPU-Memory	3,4
CPU-PEG/Display/RSVD	5
CPU-Power,CPU-GND	6,7
DDR4 DIMM*4	8,9,10,11
PCH-LPC/SPI/SMBUS/MISC	12
PCH-DMI/PCIE/USB/SATA	13
PCH-Audio/Display/Clock	14
PCH-GPIO/RSVD	15
PCH-Power,PCH-GND,PCH-Strap	16,17,18
PCIE SLOT-CPU(X16)(X1)	19,20
SIO-NCT6687/NCT3933	21,22
LAN - RTL8125B / FAN	23,24,25
AUDIO - ALC897 - depop circuit	26,27
VGA/HDMI/DP	28,29,30
M.2/WIFI/CNVi	31,32,33
USB/PS2/USB Power	34,35,36,37
SATA/VBAT/BIOS	38,39,40
ACPI CONTROLLER/CURRENT SENSE-RT9553	41,42
5V COLAY/PWM-RT3609BE/VCORE/VGT	43,44,45,46,47
VCCSA-RT3651EF/VCCIO-SYM212	48,49,50
DDR PWR - RT8125H/DDR PWR VPP25/VTT	51,52
VCCST_PLL/VCCSTG/PCH Power - RT8125H/1P8_VSB	53,54
ATX Connector / F_Panel/PWR-Seqence/MCU	55,56,57
SILEGO /EZ DEBUG LED/EMI/Manual Parts	58,59,60,61,62
Power Map/GPIO MAP/Power Sequence/SMBus	63,64,65,66
Revision History	67

MS-7D18

mATX

Ver: 1.0

Intel -RKL-S plamform

CPU:

Rocket lake S 65W

PWM:

IMVP8 -RT3609BE

Onboard Chip:

HD Audio Codec:ALC897
LAN- RTL8125B colay RTL8111K
SIO:NTC6687
Flash ROM: SPI 256 MB X1

System Chipset:

B560 PCH_V

Display Output:

HDMI 2.0 Port

DP Port

VGA Port

Main Memory:

DDRIV (2933MHz) * 4 (Dual Channel)

ACPI:

LDO

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
M.2 Key M Slot * 2
M.2 Key E Slot * 1

Other:

SATA3.0 *6
PS2 * 1
REAL USB3.2 Gen1 *2
REAL USB3.2 Gen2 *2
REAL USB2.0*2
FRONT USB3.2 Gen1*1
FRONT USB2.0 *2

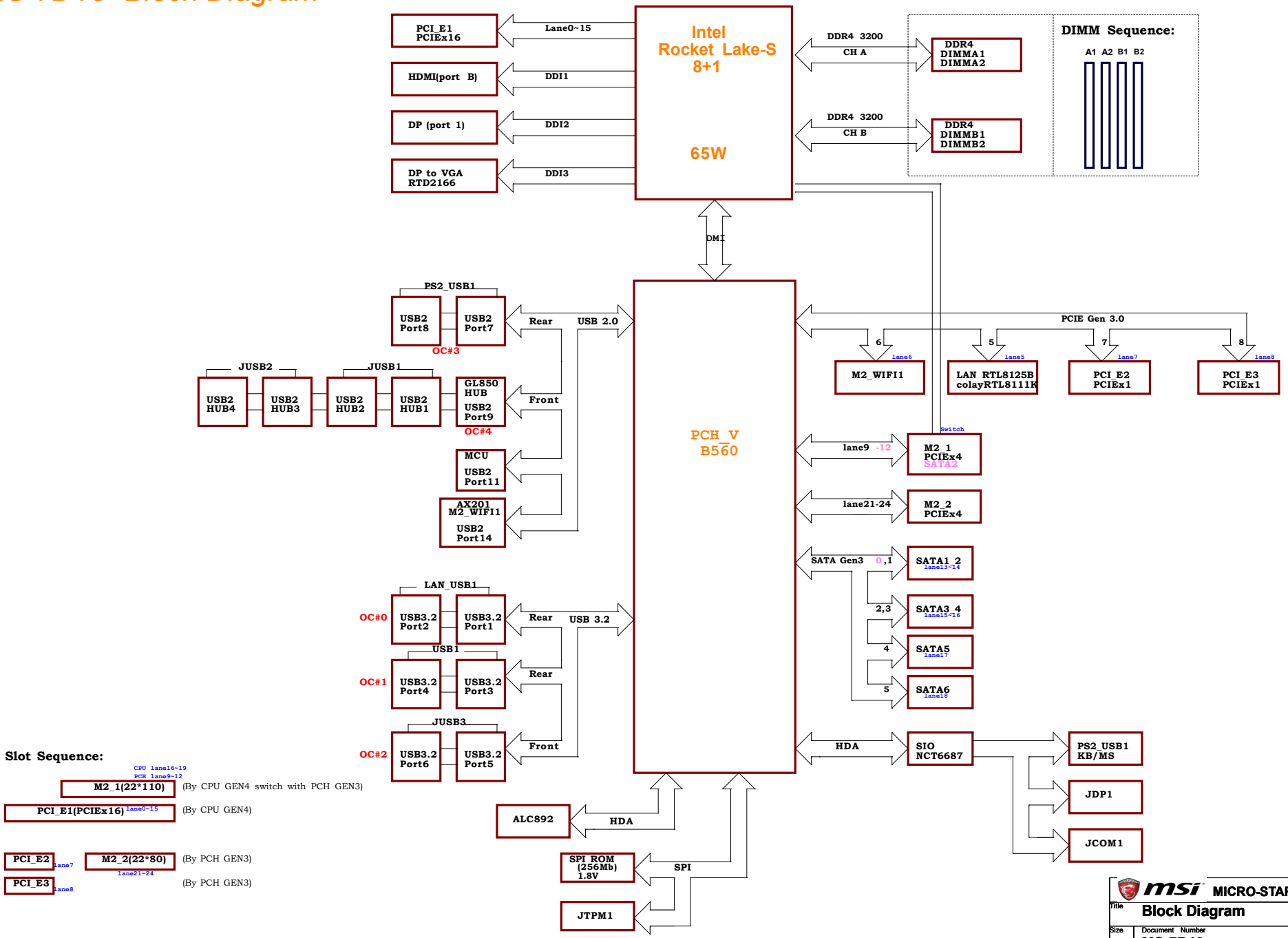
MICRO-STAR INT'L CO.,LTD.

Title: Cover Sheet

Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 1 of 67

MS-7D18 Block Diagram



Slot Sequence:

CPU lane16~19
PCH lane9~12
M2_1(22*110) (By CPU GEN4 switch with PCH GEN3)

PCI_E1(PCIEx16) lane0~15 (By CPU GEN4)

PCI_E2 lane7
M2_2(22*80) lane21~24 (By PCH GEN3)

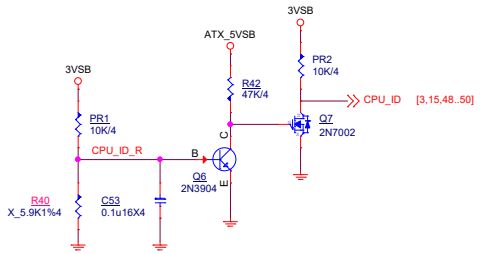
PCI_E3 lane8 (By PCH GEN3)

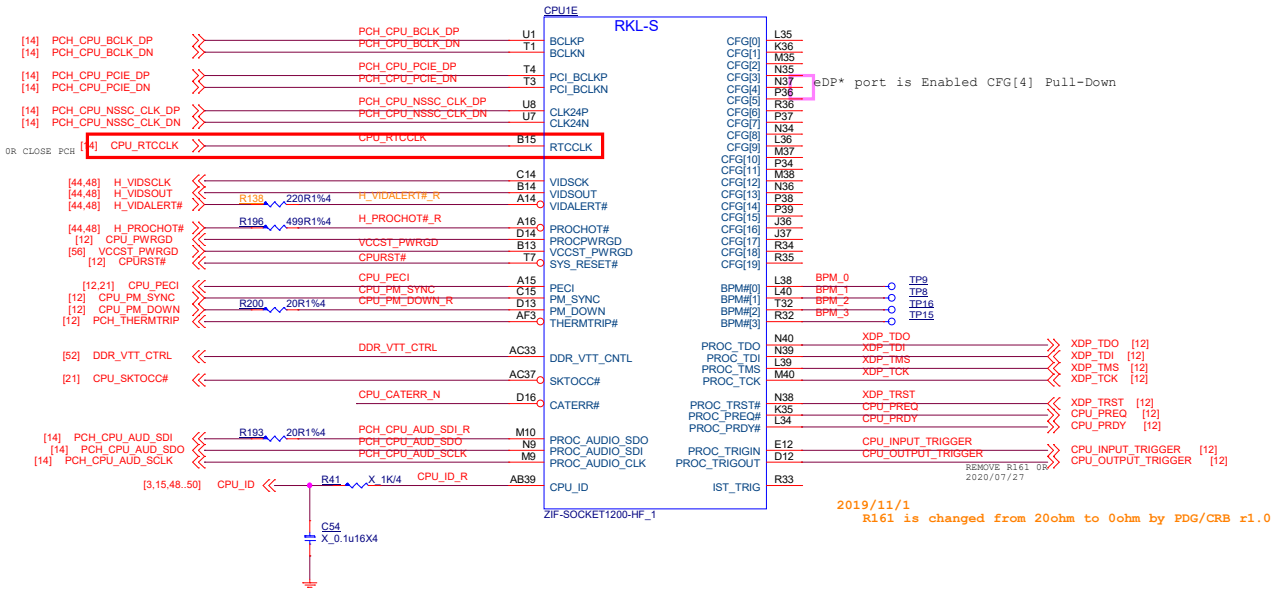
MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

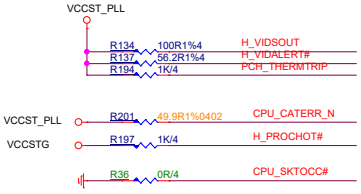
Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 2 of 67

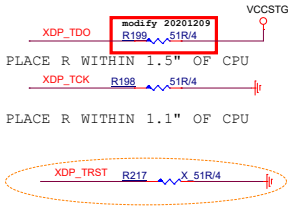




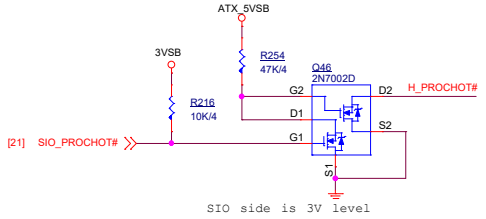
2019/11/1
R161 is changed from 20ohm to 0ohm by PDG/CRB r1.0



JTAG



H_PROCHOT Level shift



CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No stall	Stall	SCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5			PCIE Bifurcation
6			PCIE Bifurcation
7	Follow RESET#	Wait for BIOS	PEG TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

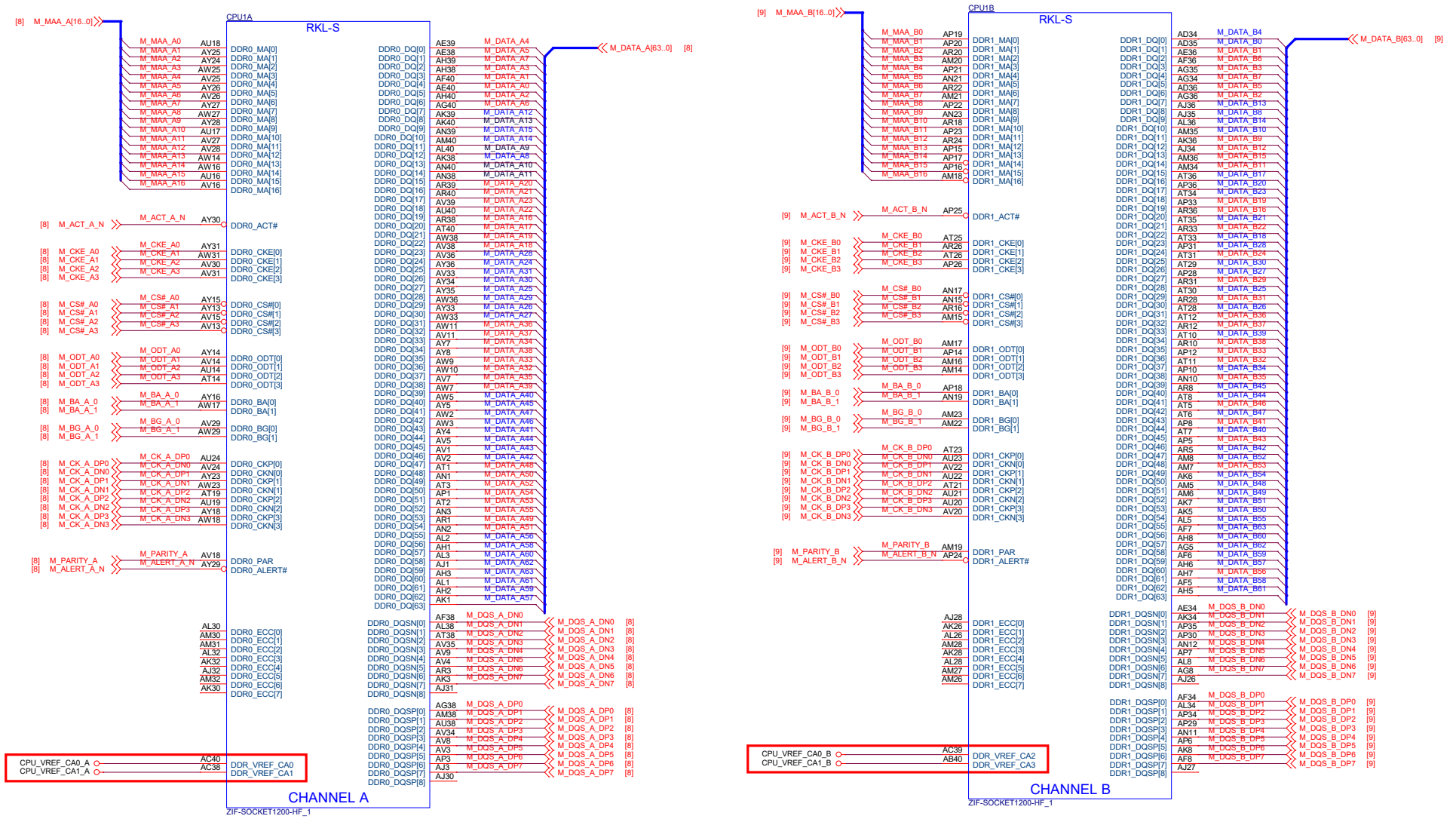
CFG5	CFG6			
ENABLE#		SLOT	SLOT	SLOT
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	RSVD	RSVD	RSVD
1	1	X16	X0	X0

MICRO-STAR INT'L CO.,LTD.

Title: CPU-Control/MISC/CFG

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 3 of 67

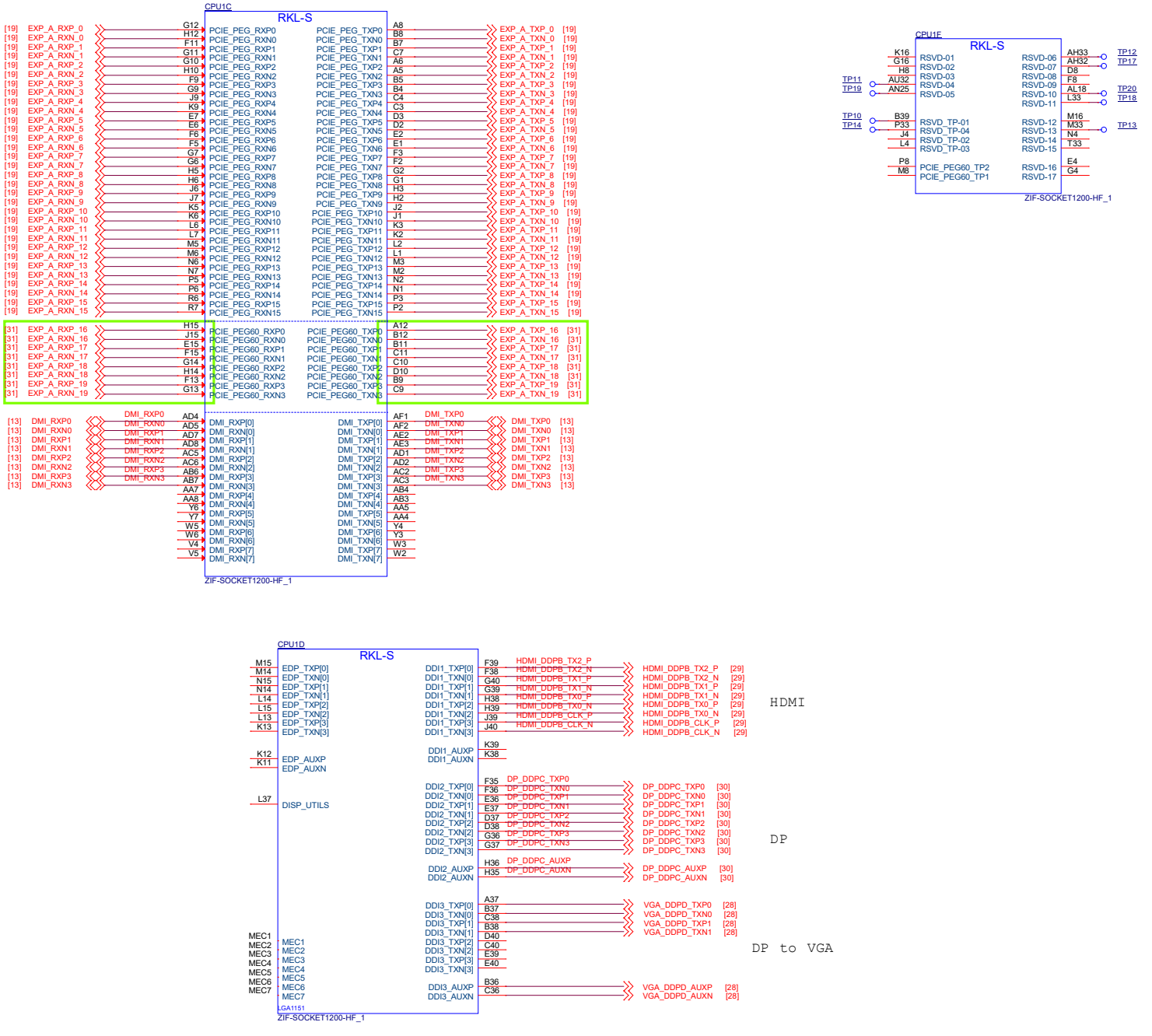


MICRO-STAR INT'L CO.,LTD.

Title: CPU-Memory

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 4 of 67

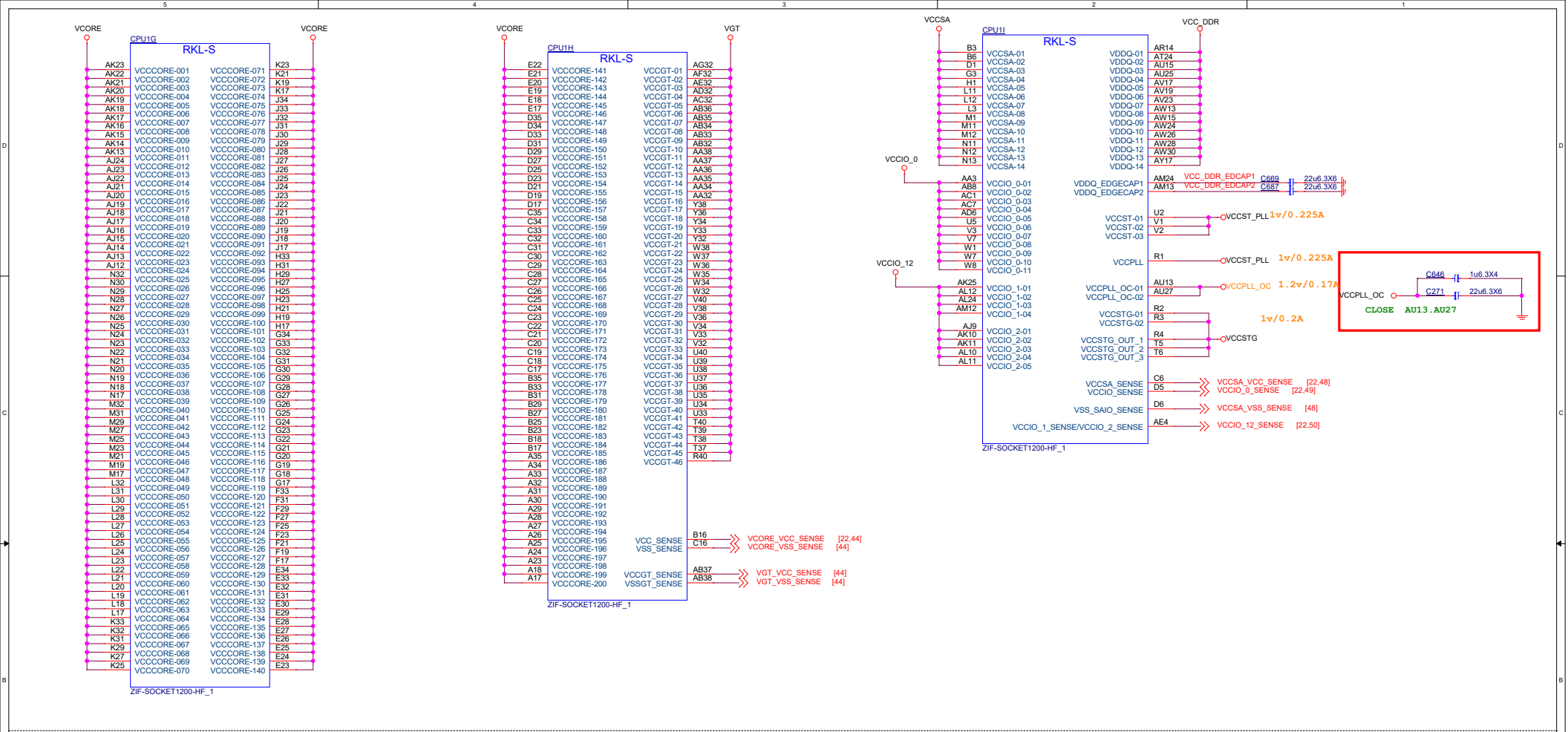


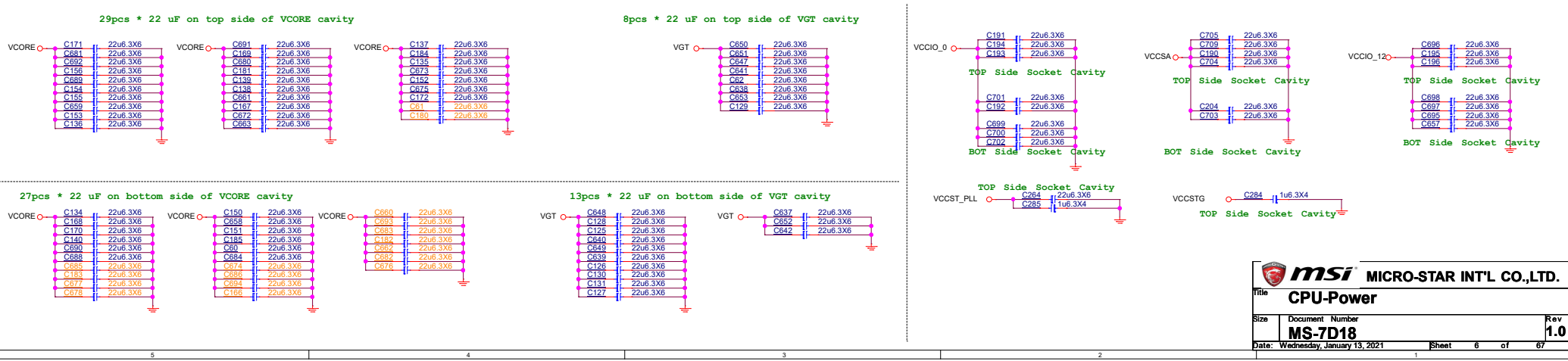
MICRO-STAR INT'L CO.,LTD.

Title: CPU-PEG/Display/RSVD

Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 5 of 67



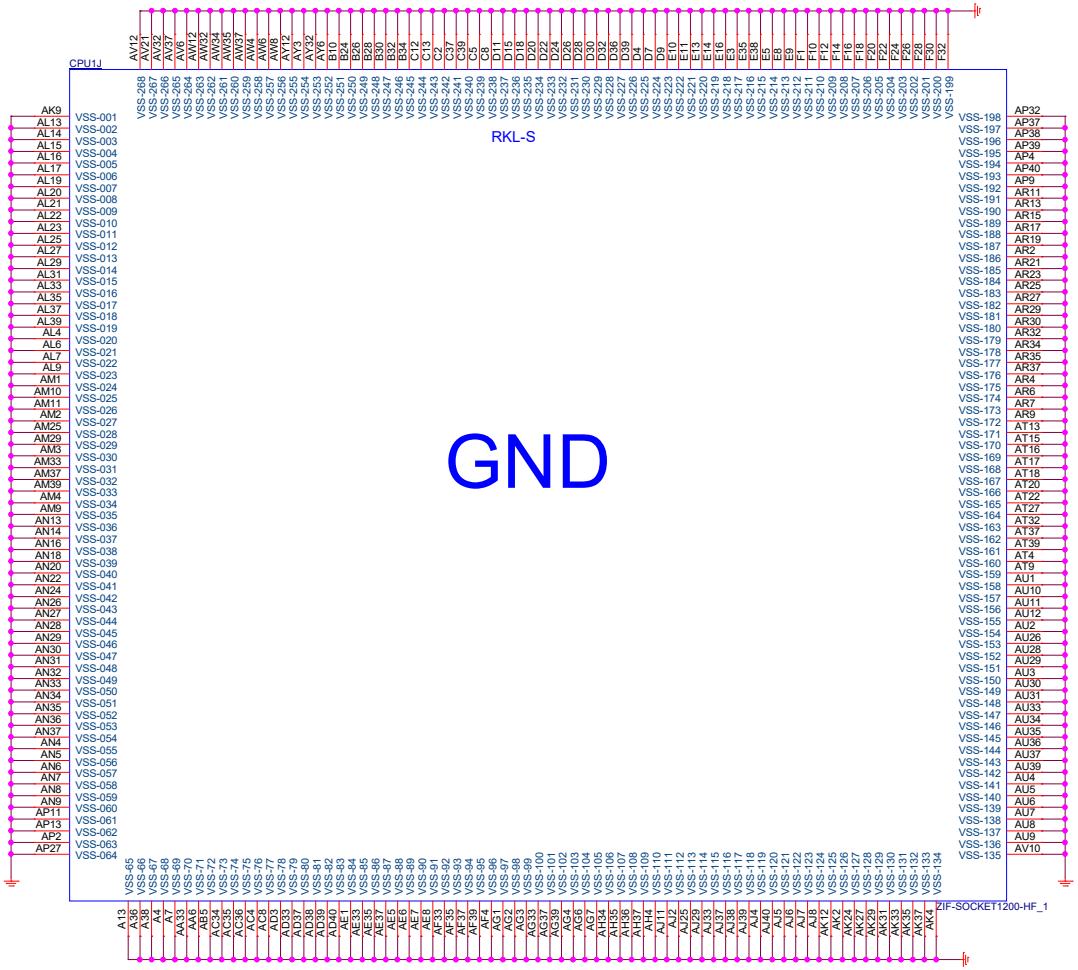


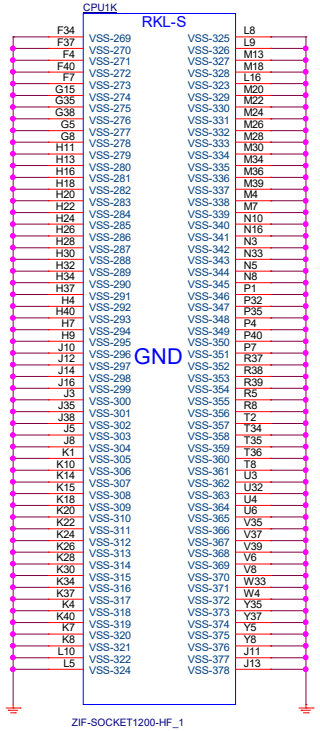
MICRO-STAR INT'L CO.,LTD.

Title: CPU-Power

Size | Document Number: MS-7D18 | Rev: 1.0

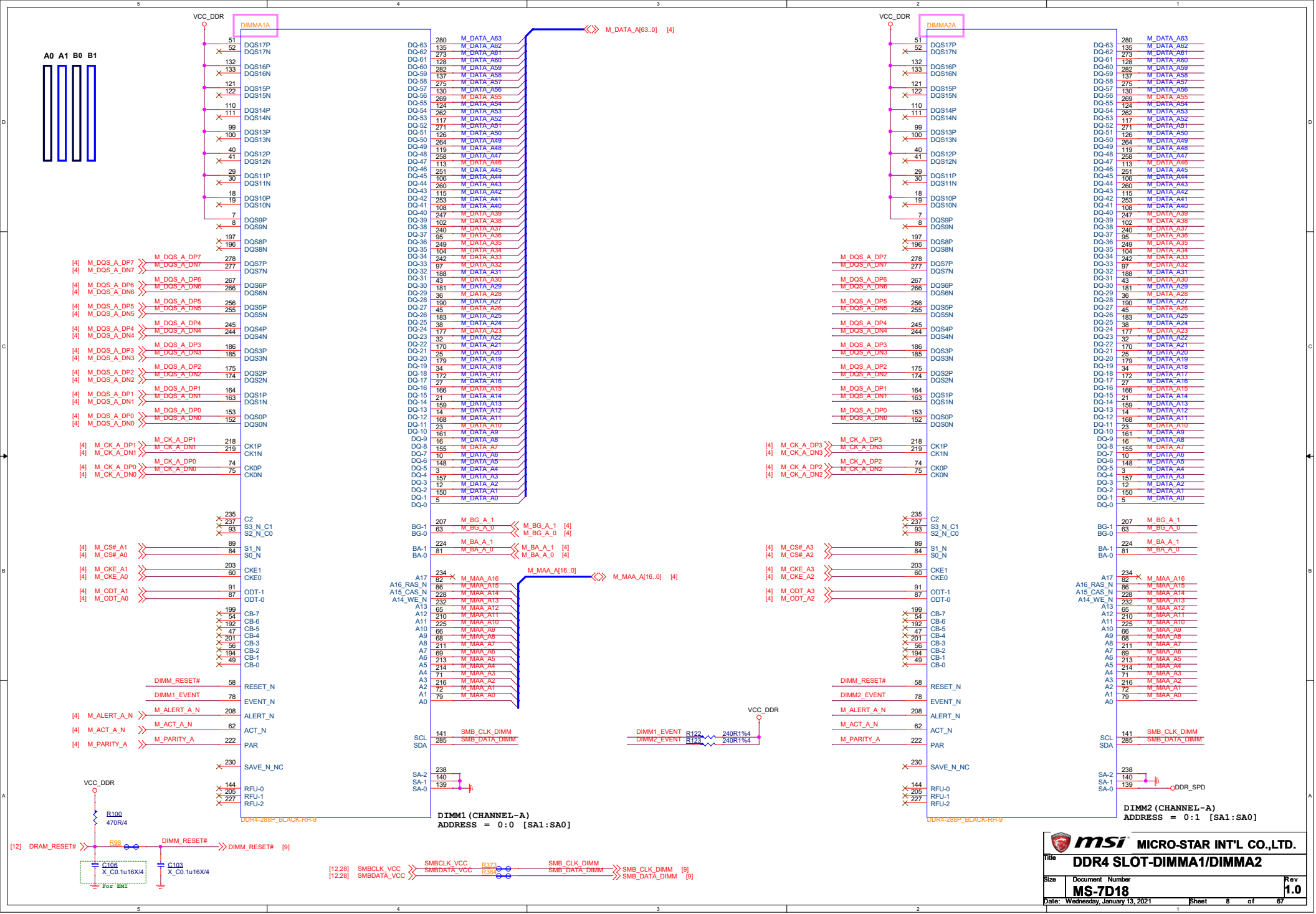
Date: Wednesday, January 13, 2021 | Sheet 6 of 67

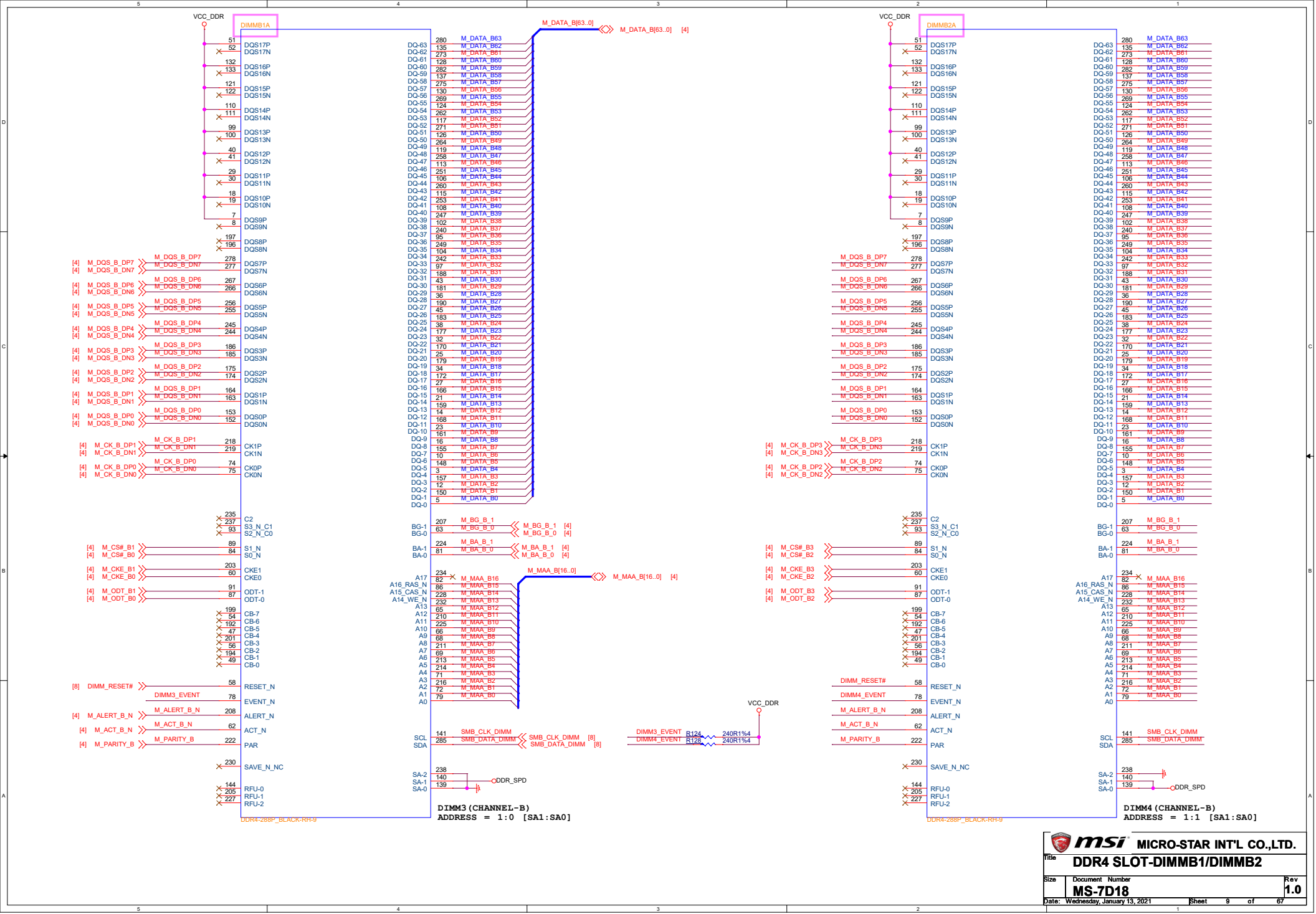




MICRO-STAR INT'L CO.,LTD.

Title	CPU-GND	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 7 of 67	


A0 A1 B0 B1
VCC_DDR
DIMMA1A
DIMMA2A
M_DATA_A[63..0] [4]
M_MAA_A[16..0]
M_MAA_A[16..0] [4]
M_BG_A_1
M_BG_A_0
M_BA_A_1
M_BA_A_0
DIMM_RESET#
DIMM1_EVENT
DIMM2_EVENT
M_ALERT_A_N
M_ACT_A_N
M_PARITY_A
SMB_CLK_DIMM
SMB_DATA_DIMM
DDR4-288P_BLACK-RH-9
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
DDR_SPD
R100
470R/4
R98
C106
X_C0.1u16X/4
C103
X_C0.1u16X/4
For EMI
DRAM_RESET# [12]
DIMM_RESET# [9]
SMBCLK_VCC [12,28]
SMBDATA_VCC [12,28]
R373
R364
SMB_CLK_DIMM [9]
SMB_DATA_DIMM [9]
MICRO-STAR INT'L CO.,LTD.
DDR4 SLOT-DIMMA1/DIMMA2
Size
Document Number
MS-7D18
Rev
1.0
Date: Wednesday, January 13, 2021
Sheet 8 of 67

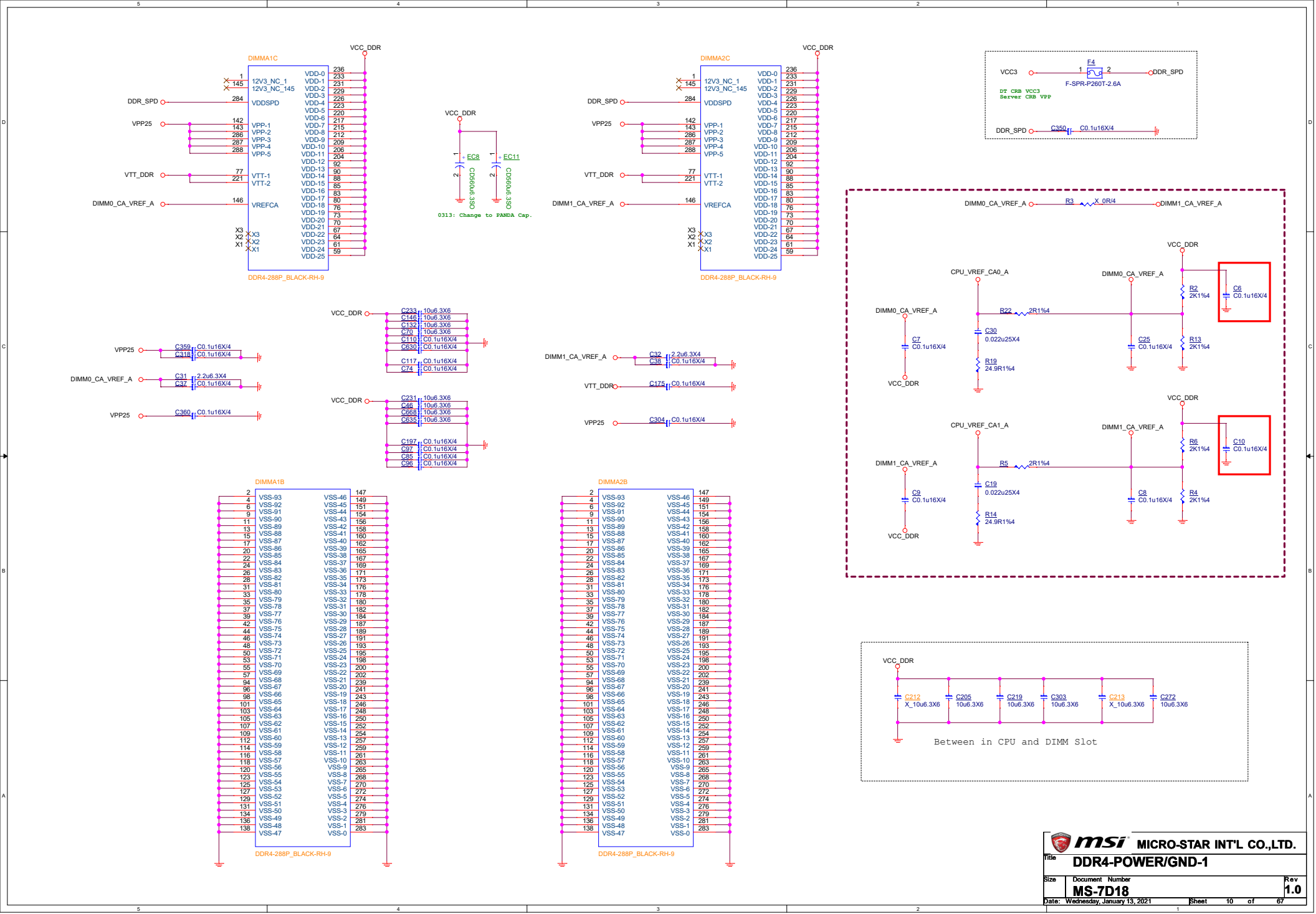


MICRO-STAR INT'L CO.,LTD.

Title: DDR4 SLOT-DIMMB1/DIMMB2

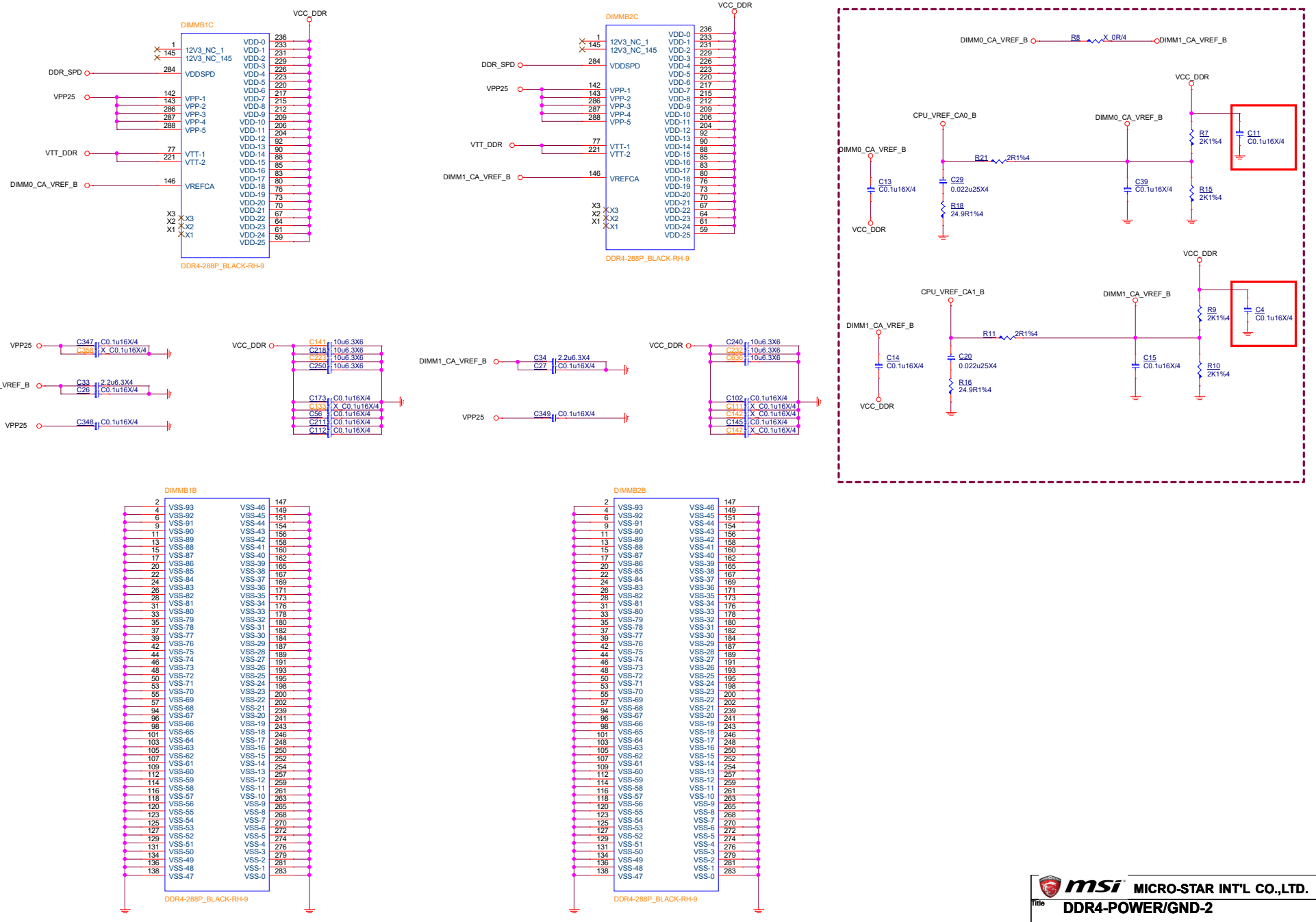
Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 9 of 67



MICRO-STAR INT'L CO.,LTD.

Title	DDR4-POWER/GND-1	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 10 of 67	

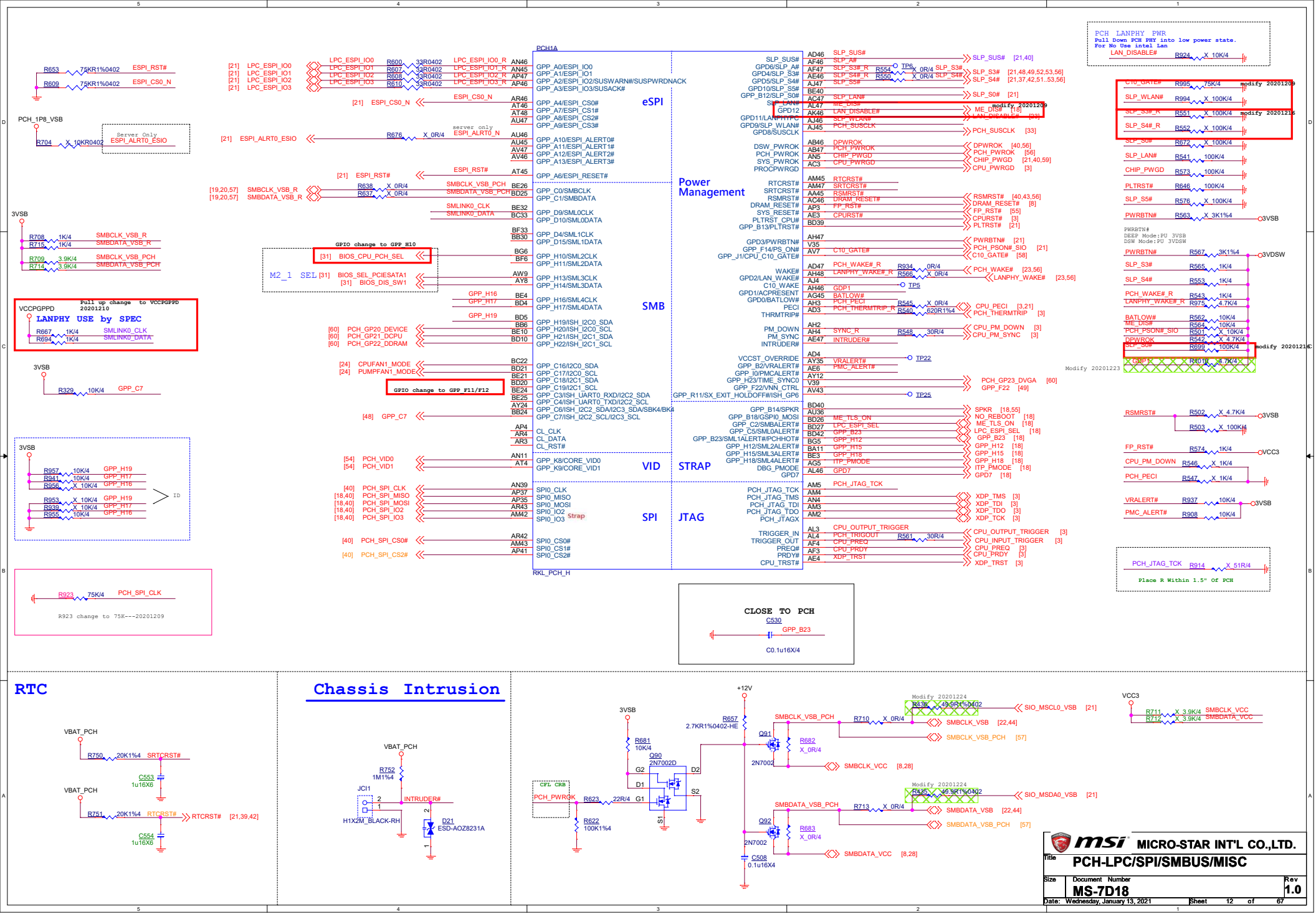


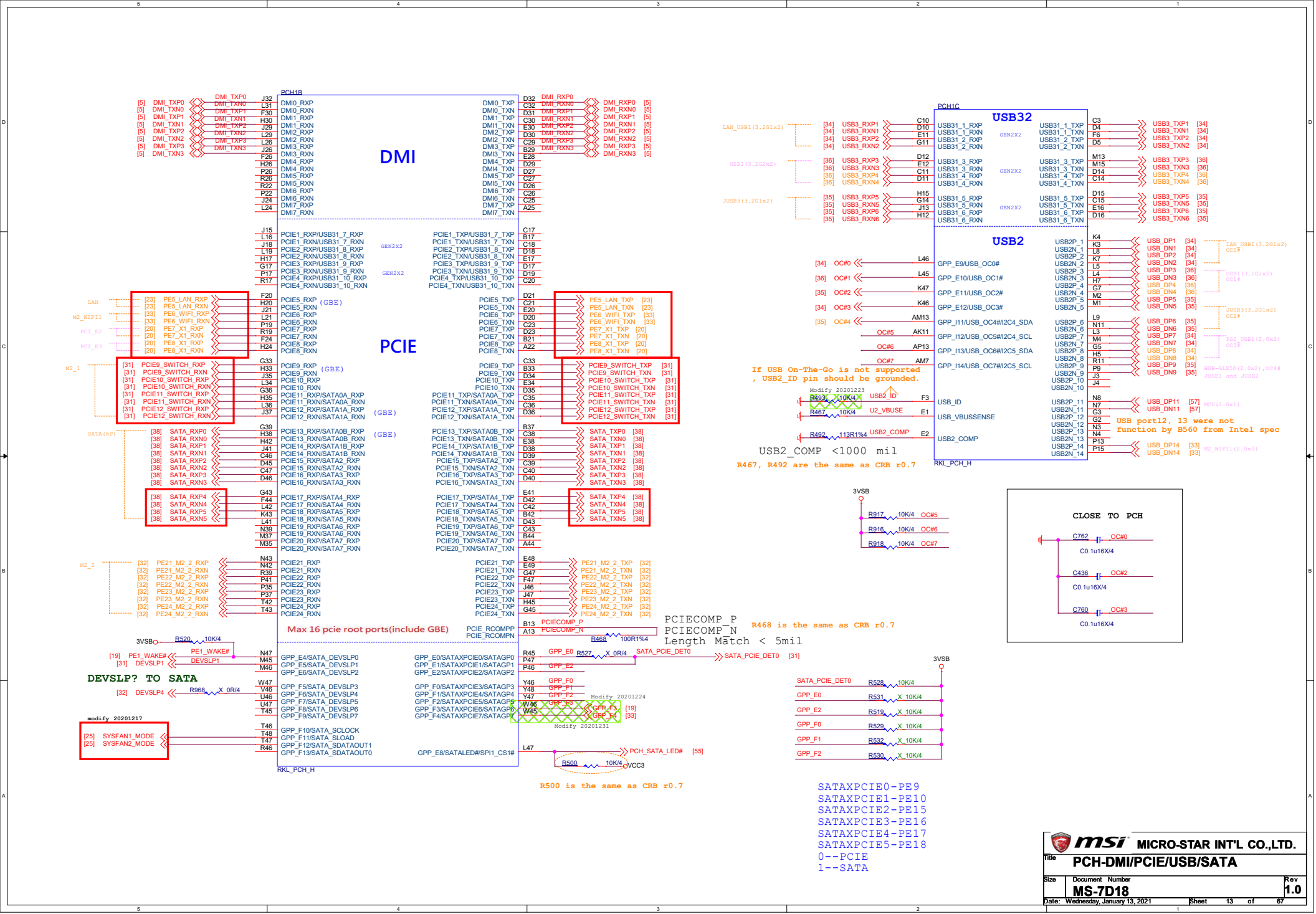
MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-2

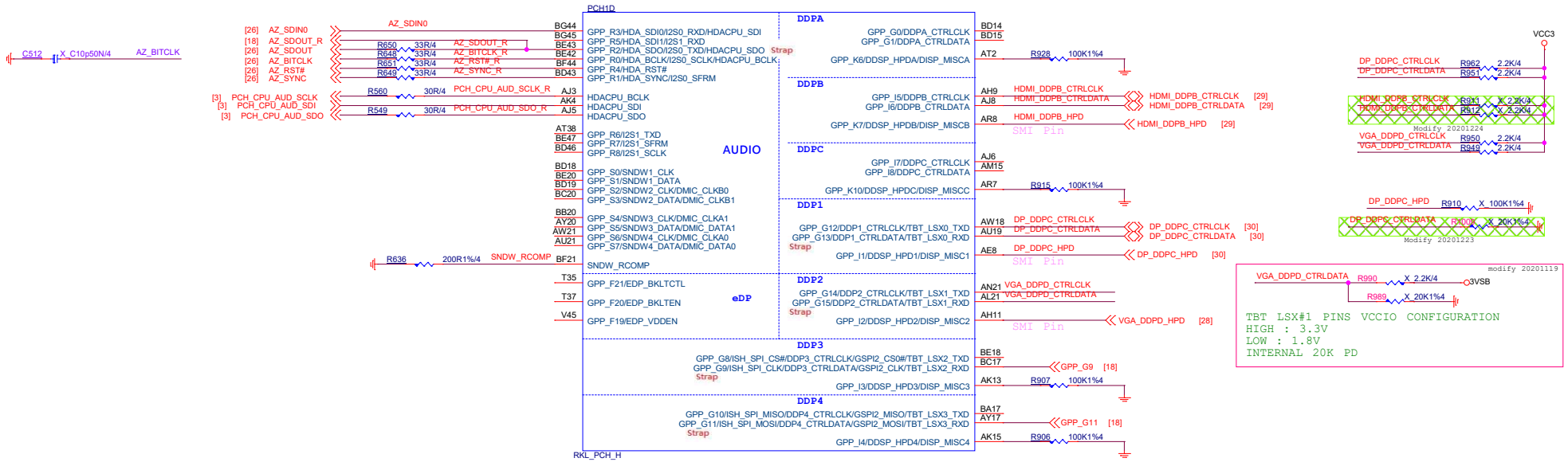
Size: | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 11 of 67

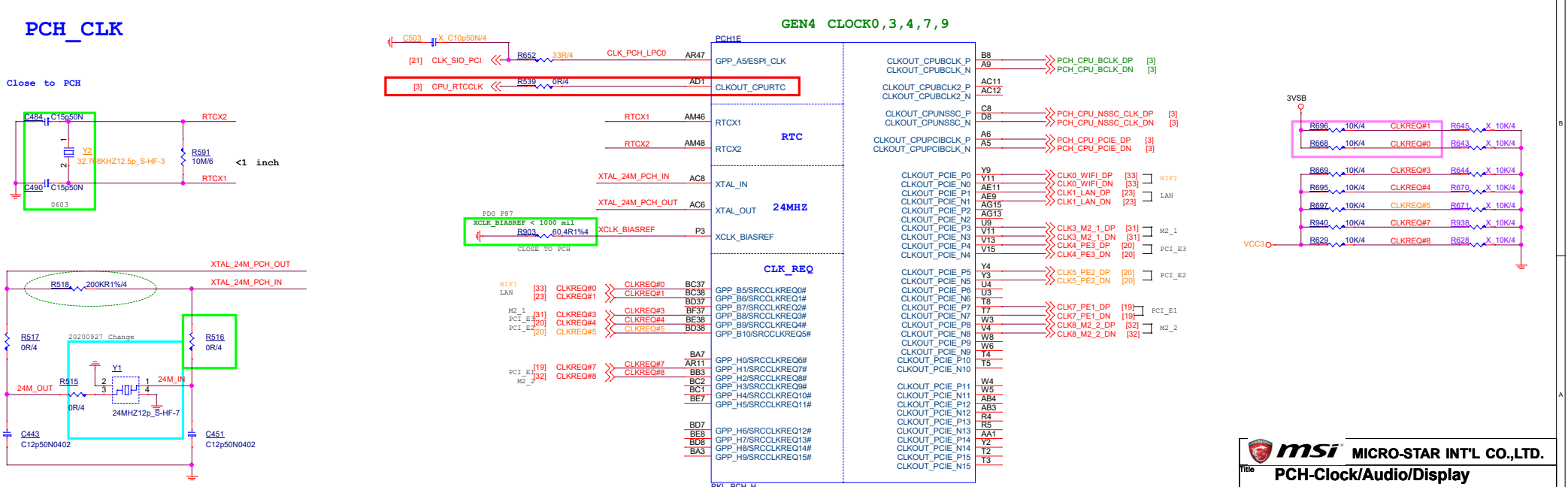

PCH1A
eSPI
SMB
VID
SPI
Power Management
STRAP
JTAG
RKL_PCH_H
LANPHY USE by SPEC
Full up change to VCCPGPPD 20201210
GPIO change to GPP_H10
GPIO change to GPP_F11/F12
M2_1 SEL
CLOSE TO PCH
PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
RTC
Chassis Intrusion
CFL CRB
MICRO-STAR INT'L CO.,LTD.
PCH-LPC/SPI/SMBUS/MISC
MS-7D18
Rev 1.0
Wednesday, January 13, 2021
Sheet 12 of 67


PCH1B
DMI
PCIE
Max 16 pcie root ports(include GBE)
RKL_PCH_H
PCH1C
USB32
USB2
RKL_PCH_H
If USB On-The-Go is not supported , USB2_ID pin should be grounded.
USB2_COMP <1000 mil
R467, R492 are the same as CRB r0.7
CLOSE TO PCH
C762 OC#0 C0.1u16X4
C436 OC#2 C0.1u16X4
C760 OC#3 C0.1u16X4
USB port12, 13 were not function by B560 from Intel spec
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
R468 is the same as CRB r0.7
DEVSLP? TO SATA
R500 is the same as CRB r0.7
SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA
MICRO-STAR INT'L CO.,LTD.
PCH-DMI/PCIE/USB/SATA
MS-7D18
Rev 1.0
Wednesday, January 13, 2021
Sheet 13 of 67

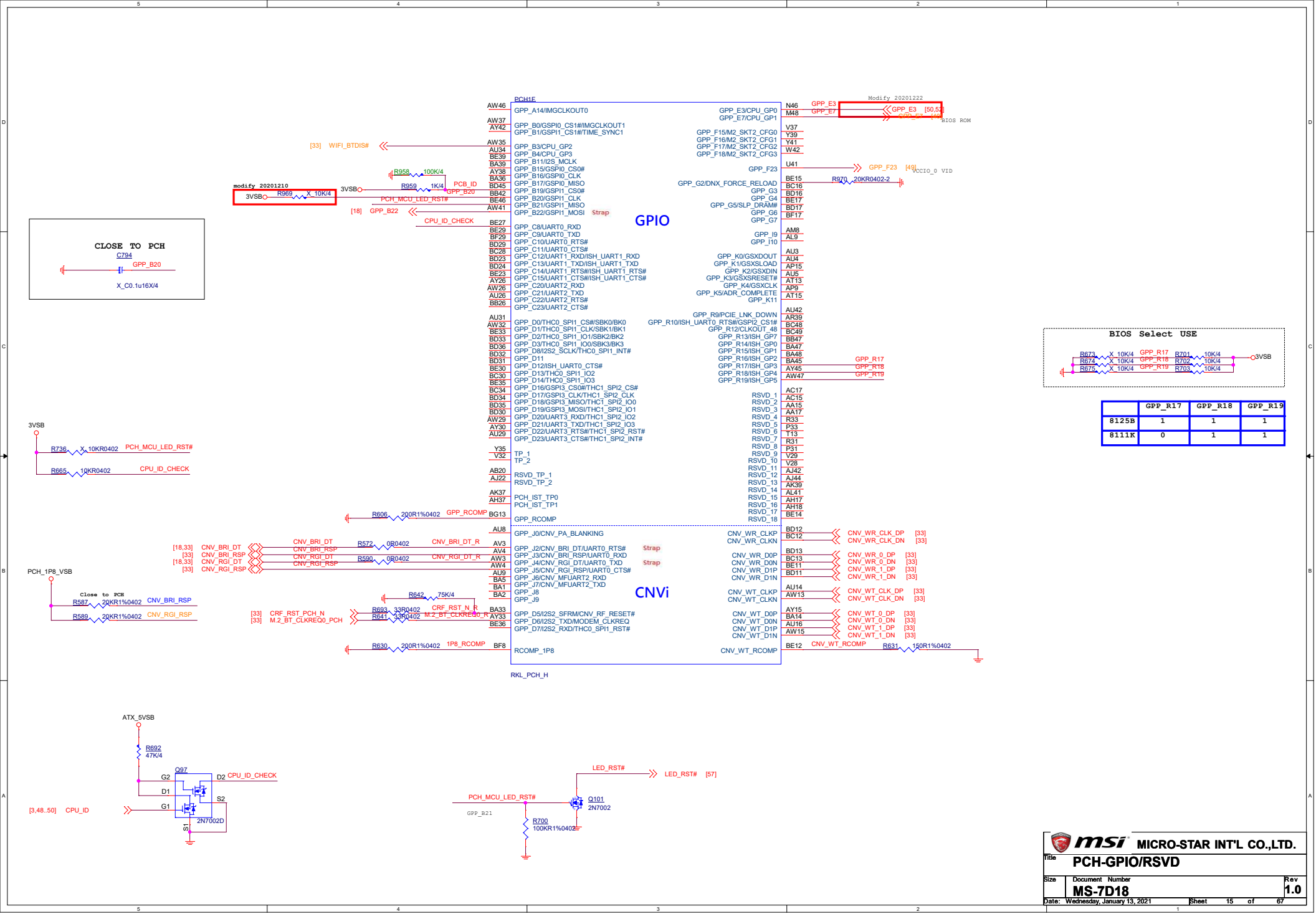
PCH_AUDIO



PCH_CLK

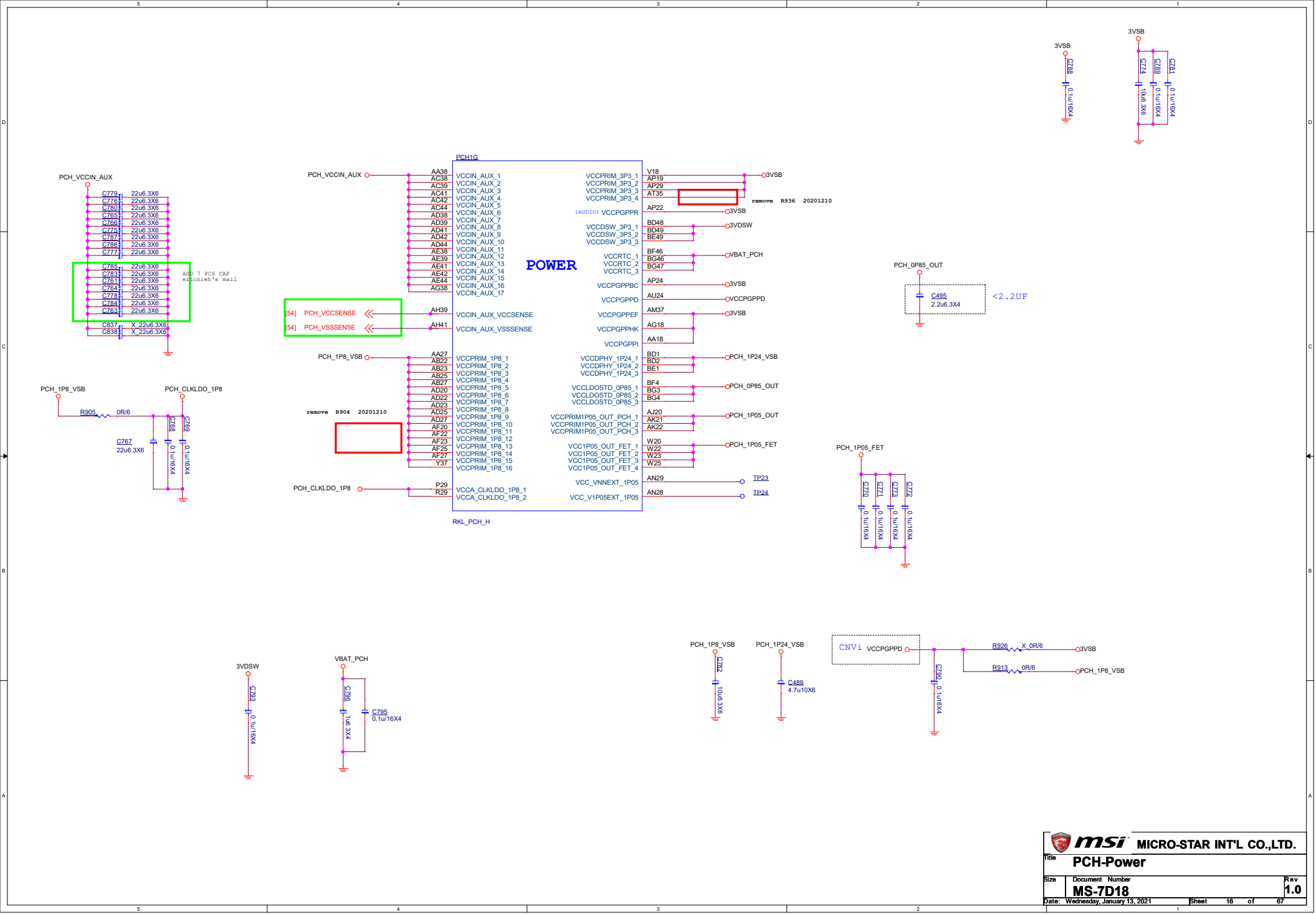


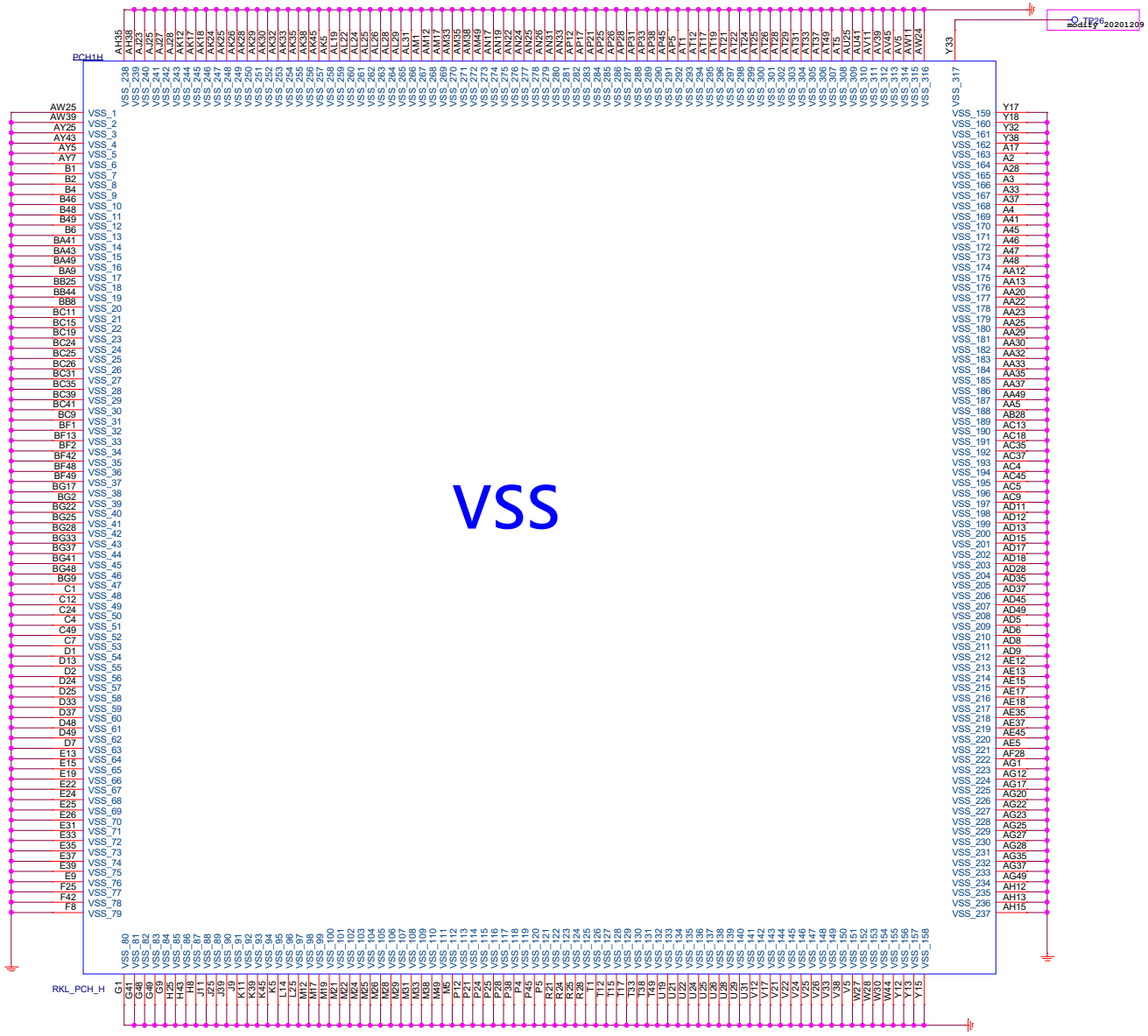
MSI MICRO-STAR INT'L CO.,LTD.			
Title: PCH-Clock/Audio/Display			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Thursday, January 14, 2021	Sheet 14 of 67		



Title	PCH-GPIO/RSVD		
Size	Document Number MS-7D18		Rev 1.0
Date: Wednesday, January 13, 2021	Sheet 15 of 67		

MICRO-STAR INT'L CO.,LTD.


PCH1G
POWER
RKL_PCH_H
PCH_VCCIN_AUX
PCH_1P8_VSB
PCH_CLKLDO_1P8
3VSB
3VDSW
VBAT_PCH
PCH_0P85_OUT
PCH_1P24_VSB
PCH_1P05_OUT
PCH_1P05_FET
[54] PCH_VCCSENSE
[54] PCH_VSSSENSE
VCCIN_AUX_VCCSENSE
VCCIN_AUX_VSSSENSE
remove R904 20201210
remove R936 20201210
ADD 7 PCS CAP ericnieh's mail
<2.2UF
CNVi VCCPGPPD
TP23
TP24
MICRO-STAR INT'L CO.,LTD.
PCH-Power
MS-7D18
1.0
Wednesday, January 13, 2021
Sheet 16 of 67

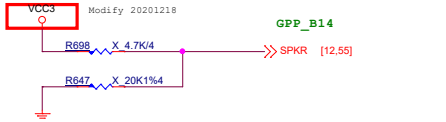


Title	PCH-GND
Size	Document Number: MS-7D18
Rev	1.0
Date:	Wednesday, January 13, 2021
Sheet	17 of 67

MICRO-STAR INT'L CO.,LTD.

TOP Swap

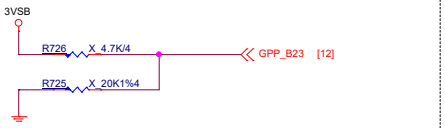
0 : DISABLE (Default)
1 : ENABLE



Internal Pull-down is disabled after PCH_PWROK is high.

DCI Enable

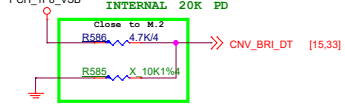
0 : DISABLE Intel DCI-OOB(Default)
1 : ENABLE intel DCI-OOB



Internal Pull-down is disabled after RSMRST# de-assert.

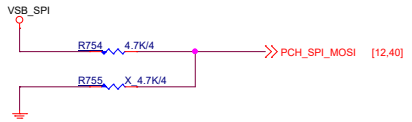
XTAL SEL1

1 = 24MHZ
0 = 38.4MHZ (default)
INTERNAL 20K PD



Internal Pull-down is disabled after RSMRST# de-assert.

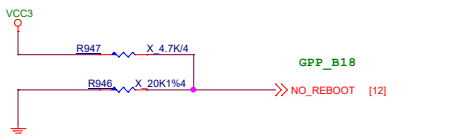
Reserved



Internal Pull-up

No Reboot

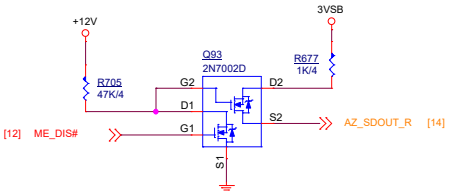
0 : DISABLE (Default)
1 : ENABLE



Internal Pull-down is disabled after PCH_PWROK is high.

Flash Descriptor Security Override

0 : ENABLE
1 : DISABLE

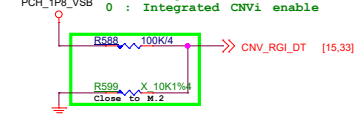


Internal Pull-down is disabled after PCH_PWROK is high.

0 : Enable security measures defined in the Flash Descriptor.
(Default)
1 : DISABLE:Flash Descritior Decurity(Override).

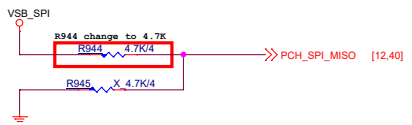
XTAL SEL2

1 : Integrated CNVi disable
0 : Integrated CNVi enable



When a RF companion chip is connected to the PCH CNVi interface,the device internal pull down resistor will pull the strap low to enable CNVi interface.

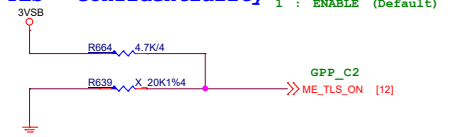
Reserved



Internal Pull-up

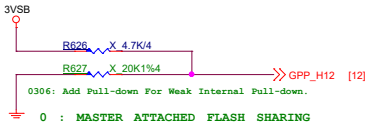
TLS confidentiality

0 : DISABLE
1 : ENABLE (Default)



Internal Pull-down is disabled after RSMRST# de-assert.

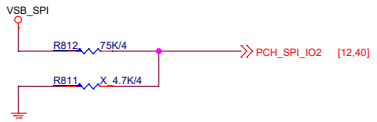
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

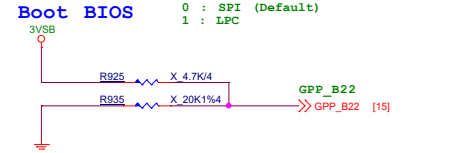
Internal Pull-down is disabled after RSMRST# de-assert.

DEBUG CONSENT STRAP



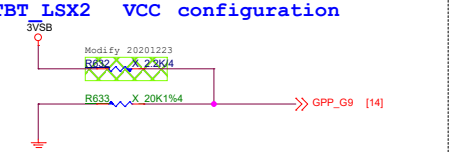
Boot BIOS

0 : SPI (Default)
1 : LPC



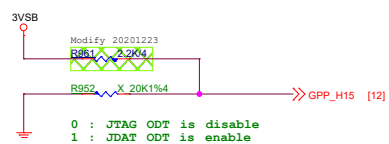
Internal Pull-down is disabled after PCH_PWROK is high.

TBT_LSX2 VCC configuration



0 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 1.8V
1 = DDP3 I2C / TBT_LSX2 / BBSB_LS2_TX pins at 3.3V

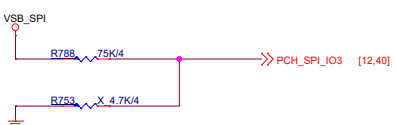
Internal Pull-down is disabled after RSMRST# de-assert.



0 : JTAG ODT is disable
1 : JDAT ODT is enable

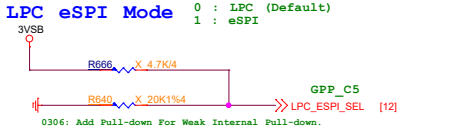
Internal Pull-down is disabled after RSMRST# de-assert.

PERSONALITY STRAP(A0 ONLY)



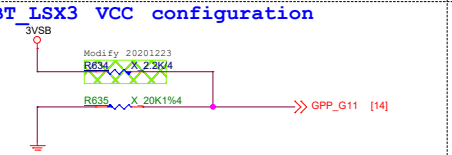
LPC eSPI Mode

0 : LPC (Default)
1 : eSPI



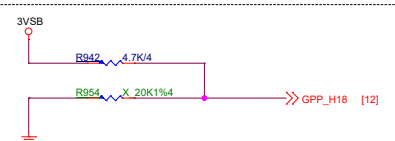
Internal Pull-down is disabled after RSMRST# de-assert.

TBT_LSX3 VCC configuration

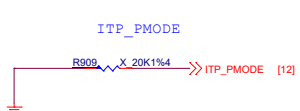


0 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V
1 = DDP4 I2C /TBT_LSX3 / BBSB_LS3 pins at 3.3V

Internal Pull-down is disabled after RSMRST# de-assert.



SPI VCCIO CONFIGURATION
HIGH:VCCPSPI=1.8V
LOW:VCCPSPI=3.3V
INTERNAL 20K PD



MICRO-STAR INT'L CO.,LTD.

Title	PCH-Strap	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 18 of 67	

12V - 5.5A

VCC3 - 3A

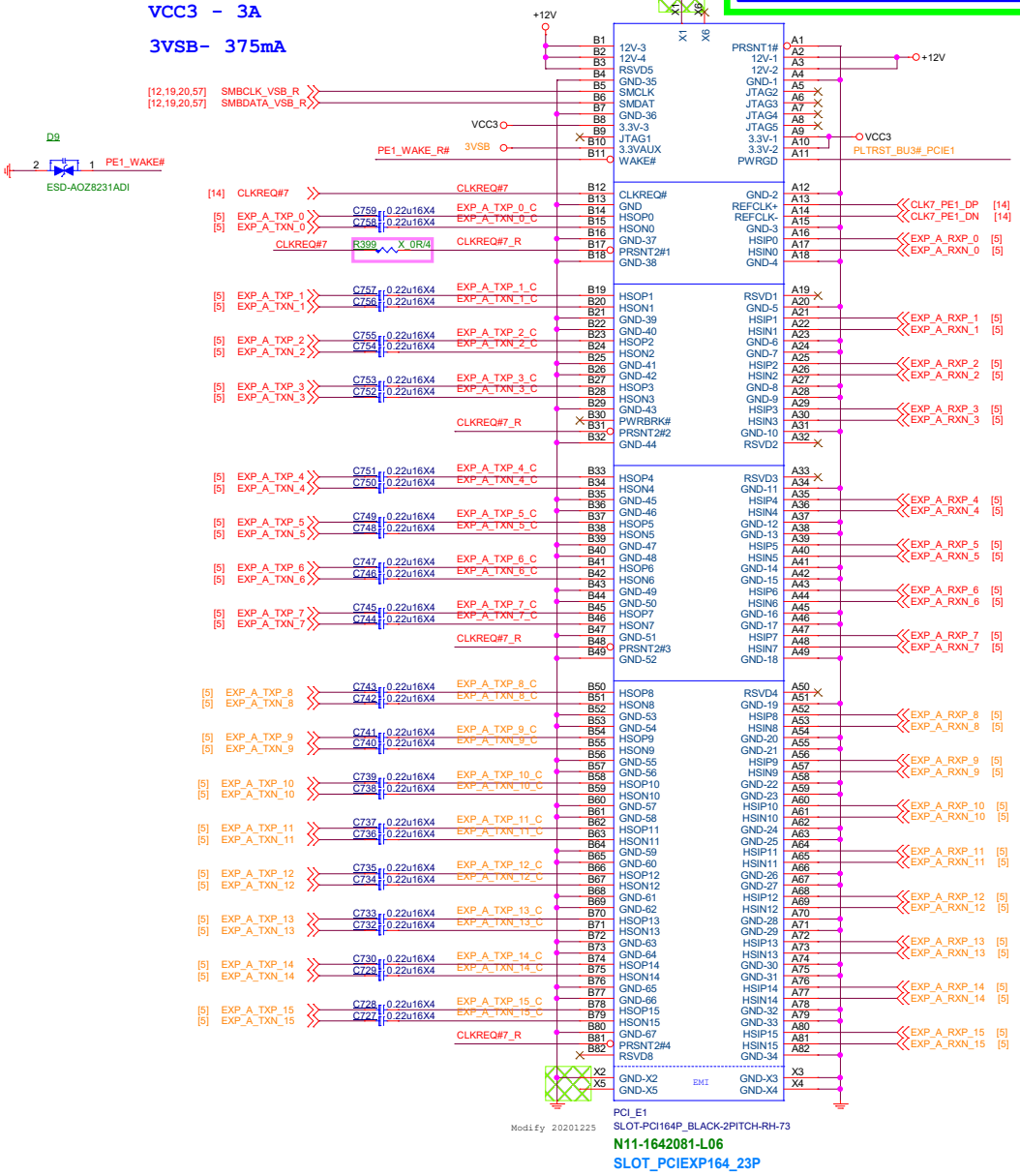
3VSB- 375mA

GEN4 X/X/20MIL

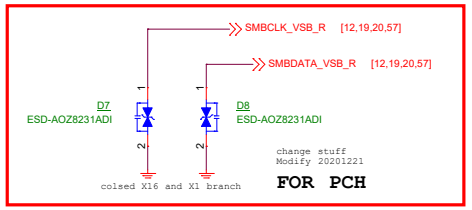
Modify 20201225

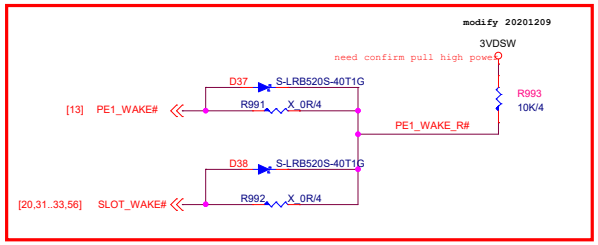
PCI Express X16 Slot

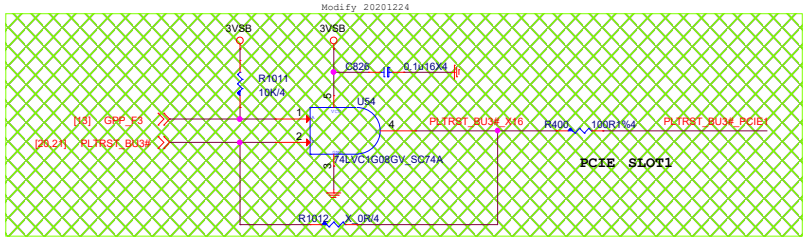
change new PN by PM spec

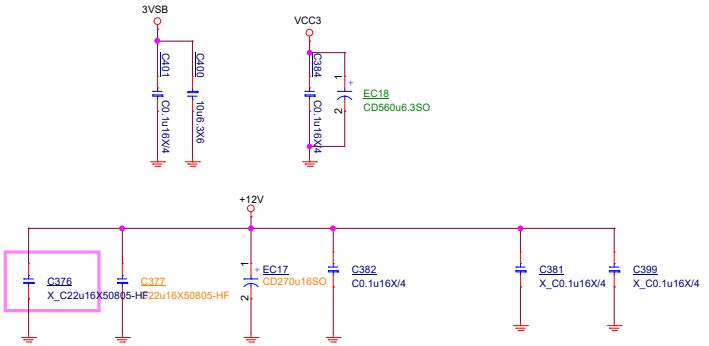


SMBus ESD

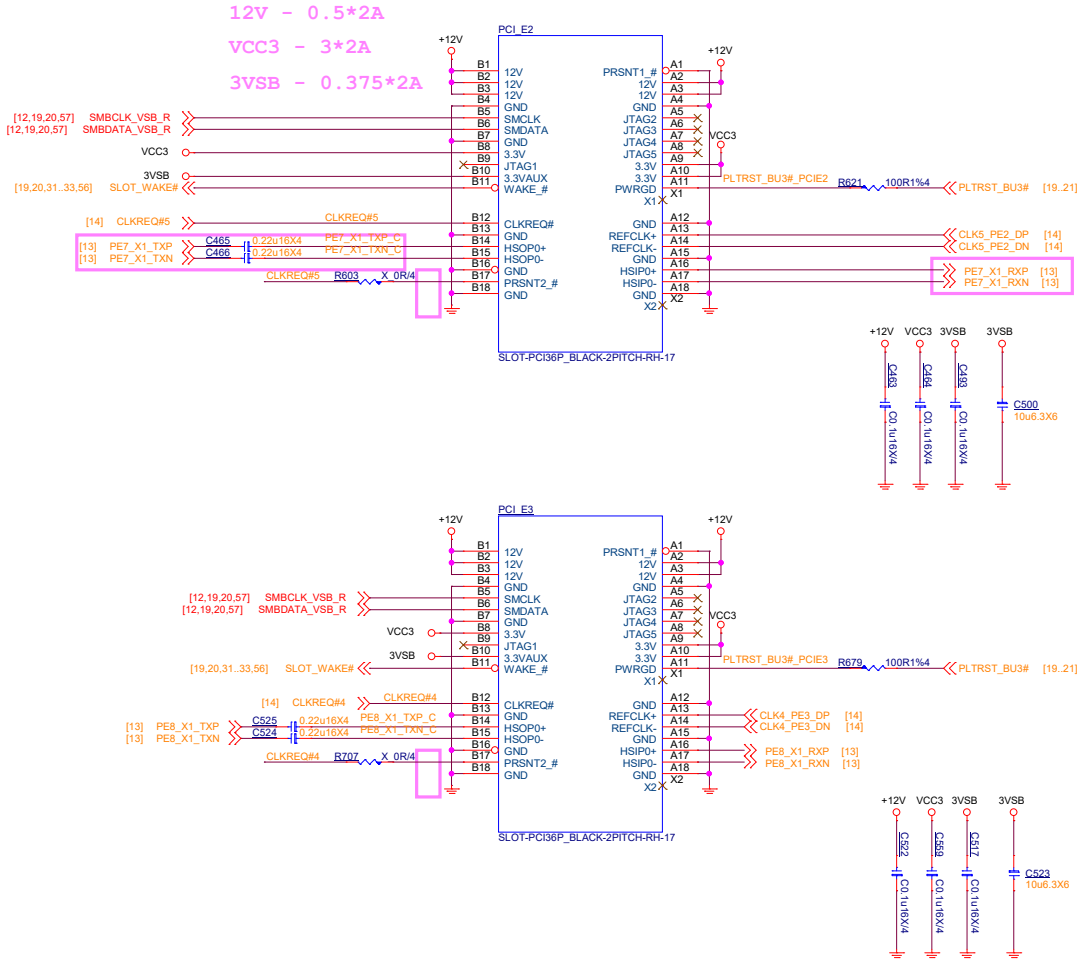




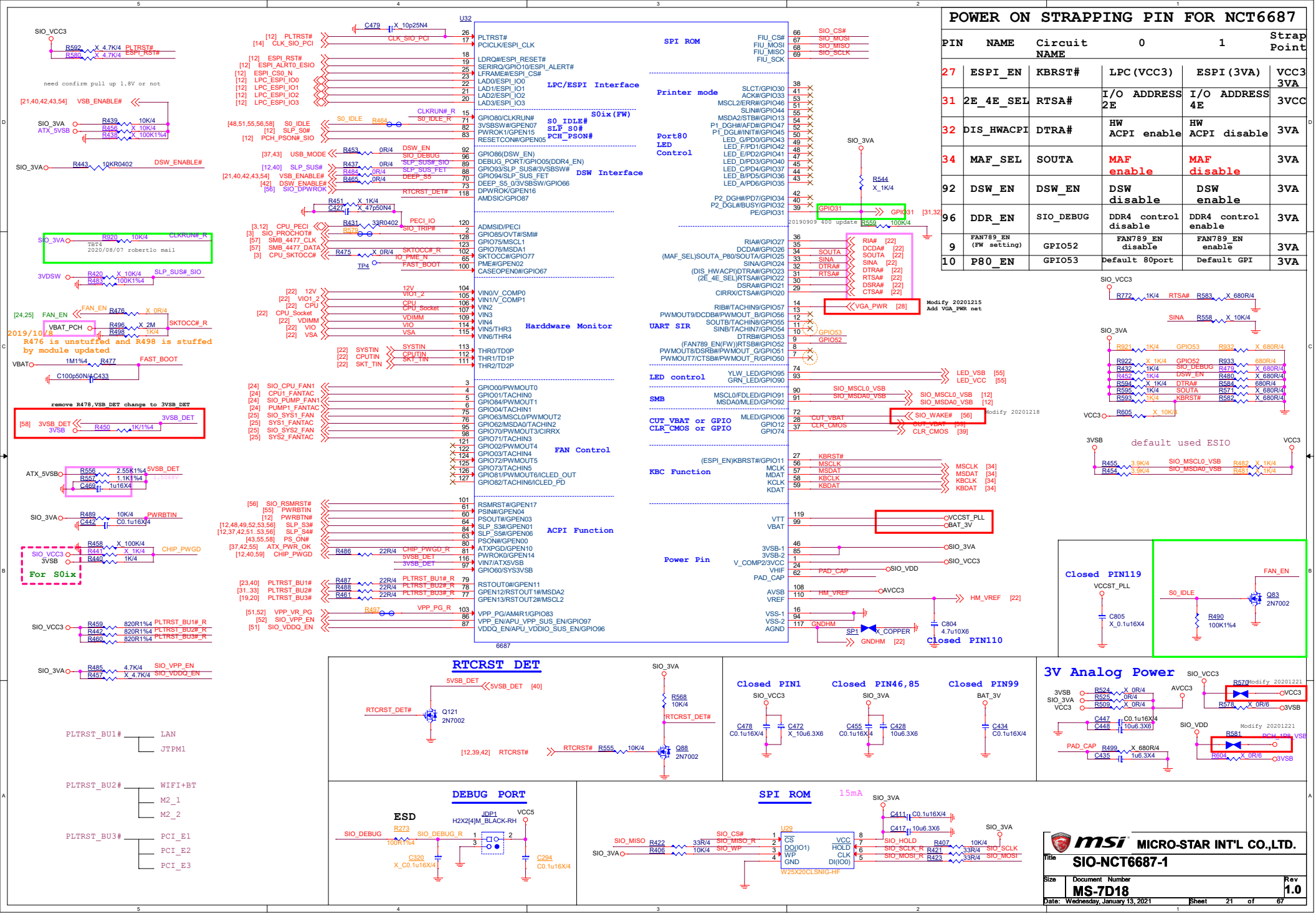




Title	MICRO-STAR INT'L CO.,LTD.		
	PCIE SLOT-CPU (X16)		
Size	Document Number		Rev
	MS-7D18		1.0
Date: Wednesday, January 13, 2021	Sheet 19 of 67		



MICRO-STAR INT'L CO.,LTD.			
Title: PCIE SLOT-PCH (X1)			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 20 of 67		



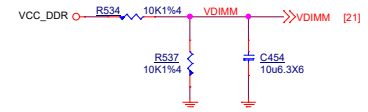
POWER ON STRAPPING PIN FOR NCT6687

PIN	NAME	Circuit NAME	0	1	Strap Point
27	ESPI_EN	KBRST#	LPC(VCC3)	ESPI(3VA)	VCC3 3VA
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789_EN disable	FAN789_EN enable	3VA
10	P80_EN	GPIO53	Default 80port	Default GPI	3VA

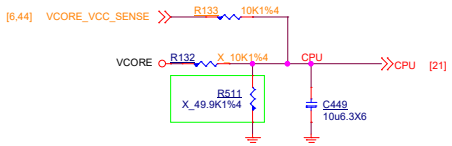
MSI	MICRO-STAR INT'L CO.,LTD.		
Title	SIO-NCT6687-1		
Size	Document Number MS-7D18		Rev 1.0
Date: Wednesday, January 13, 2021		Sheet 21 of 67	

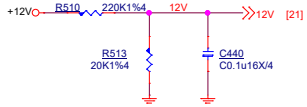
HW Monitor - Voltage

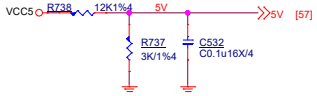
SIO HM Voltage Over 2V will Not Detect



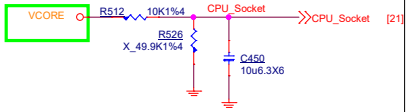
R132&R133 place together



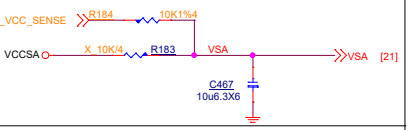




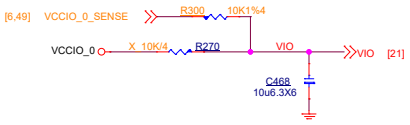
VCORE net need close to CPU socket plane.

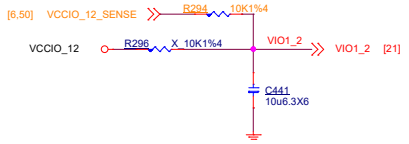


R184&R183 place together

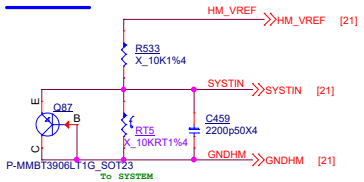


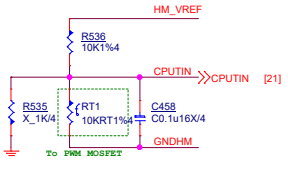
R300&R270 place together

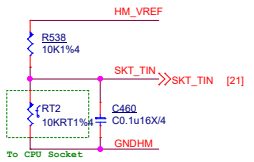




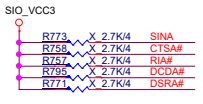
Thermal



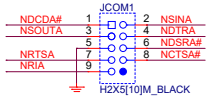




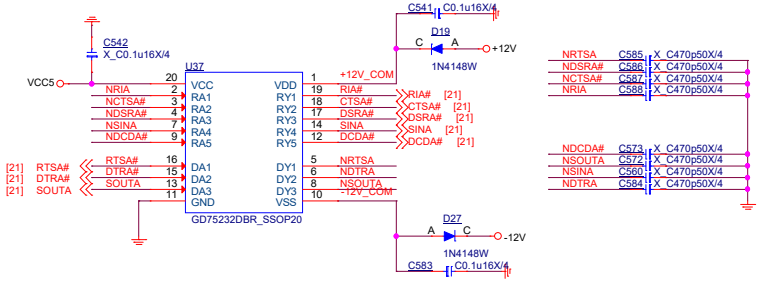
COM PORT



No Use UART Port1

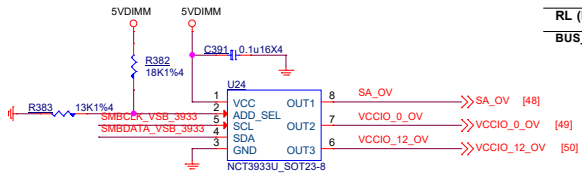


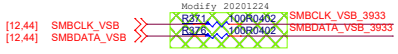
N31-2051331-H06



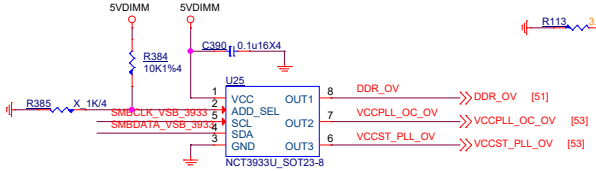
VOLTAGE CONSOLE

0x26:RH=18K,RL=13K





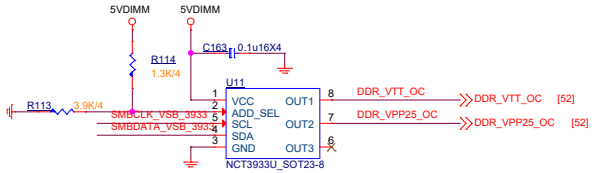
0x20:RH=10K,RL=OPEN



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%

0x22:RH=1.3K,RL=3.9K



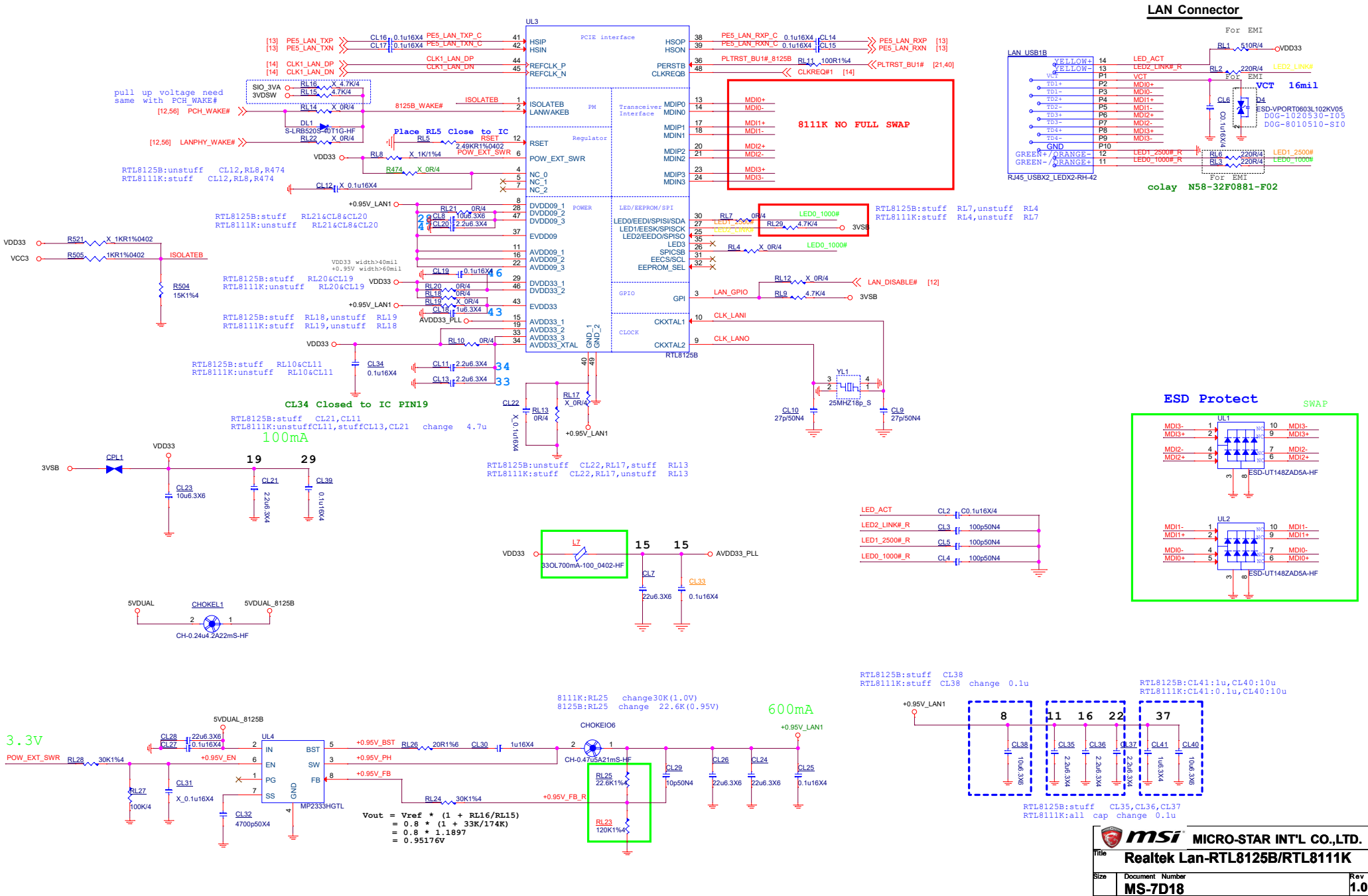
MICRO-STAR INT'L CO.,LTD.

Title: SIO-NCT6687-2

Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 22 of 67

Realtek Lan-RTL8125B/RTL8111K

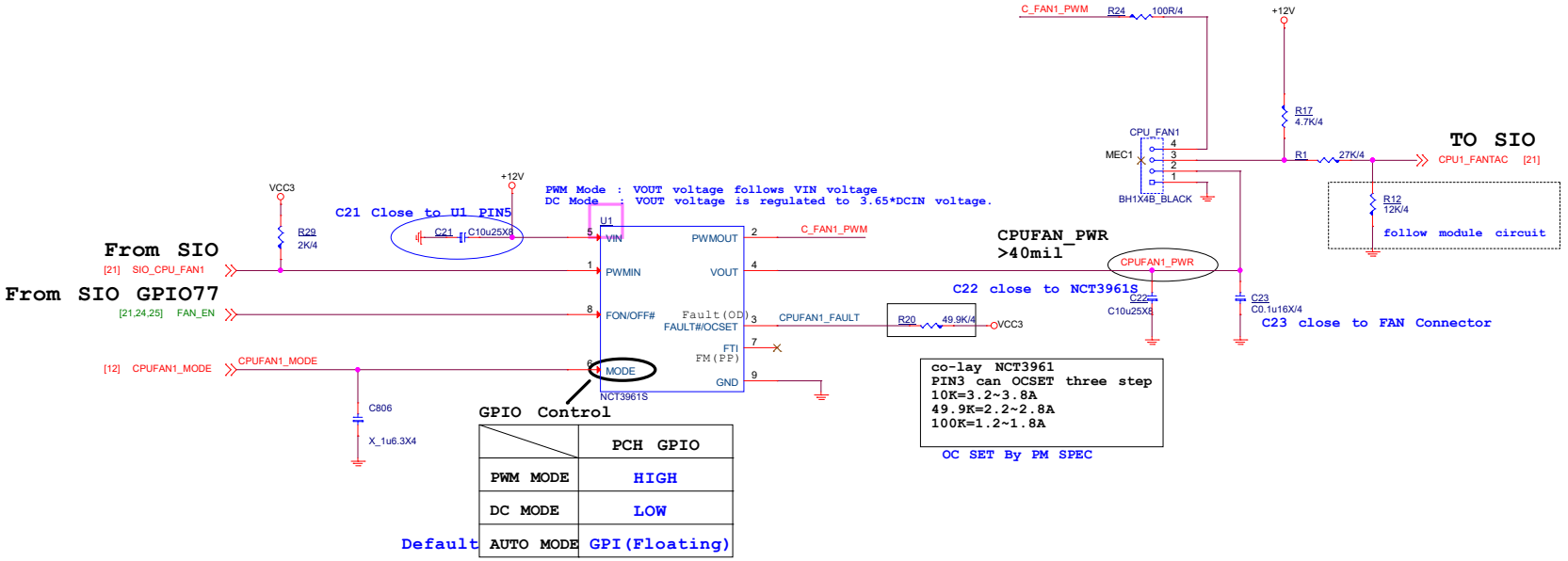


MICRO-STAR INT'L CO.,LTD.			
Title: Realtek Lan-RTL8125B/RTL8111K			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 23 of 67		

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

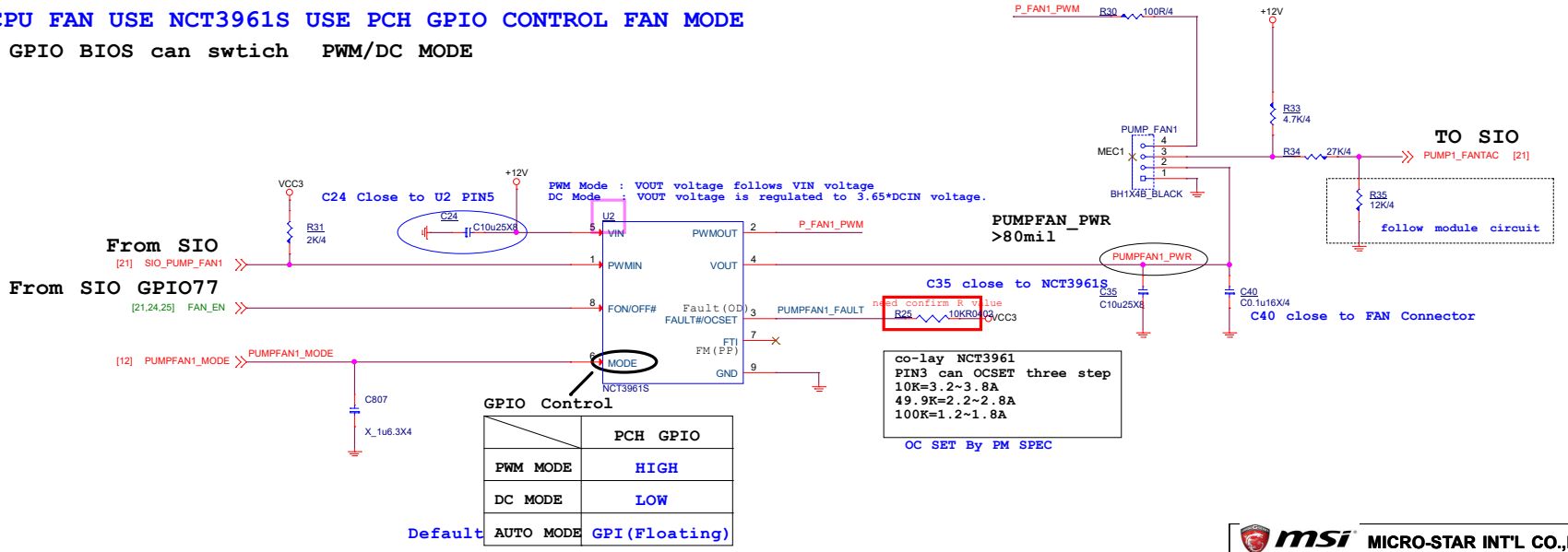
CPU FAN 2A



TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

PUMP FAN 3A



MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN1 + PUMP FAN1

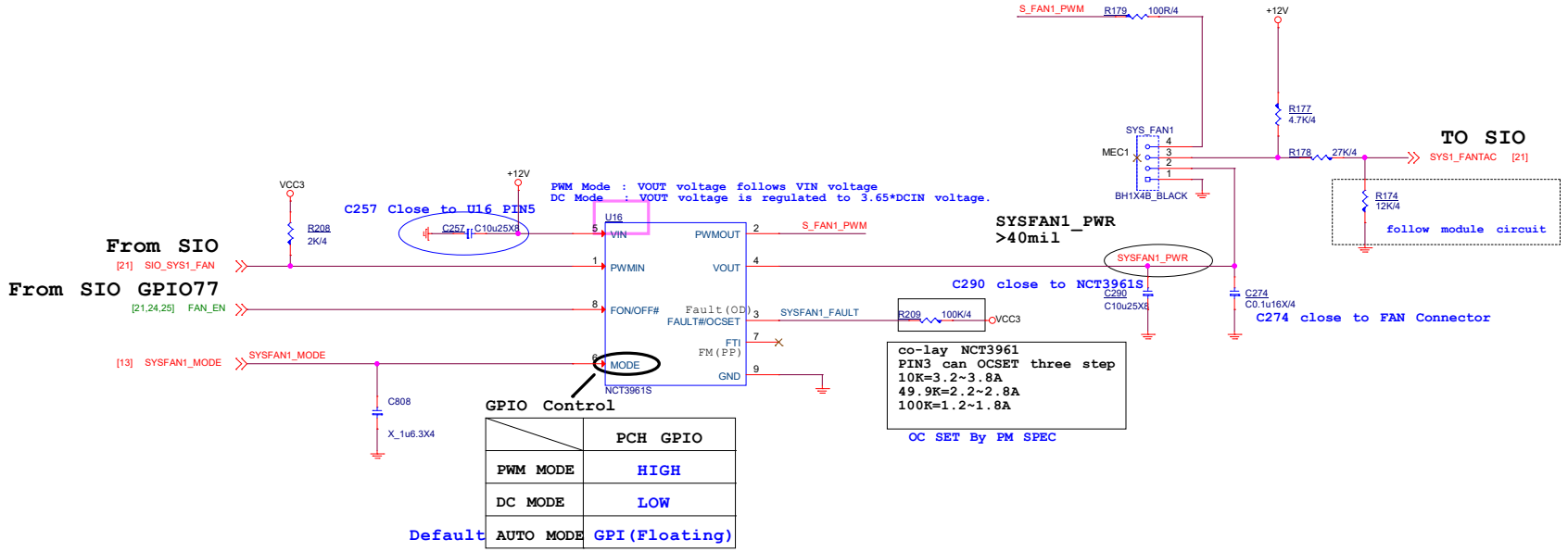
Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 24 of 67

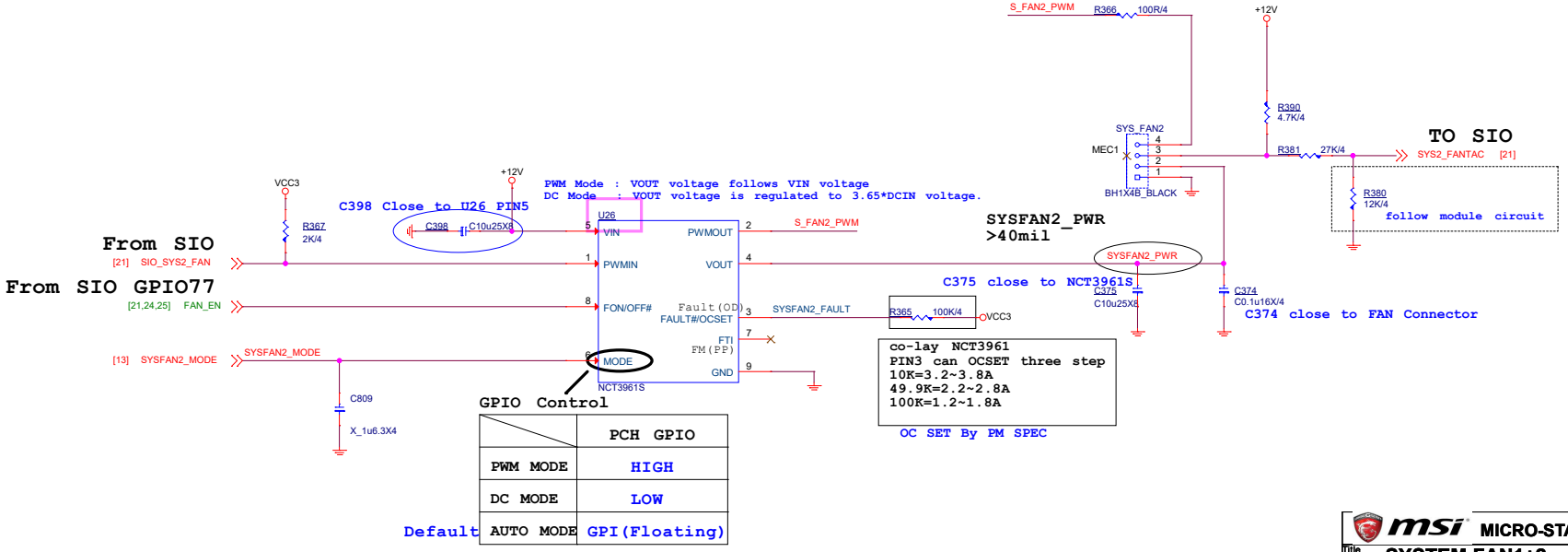
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

SYS FAN 1A



SYS FAN 1A

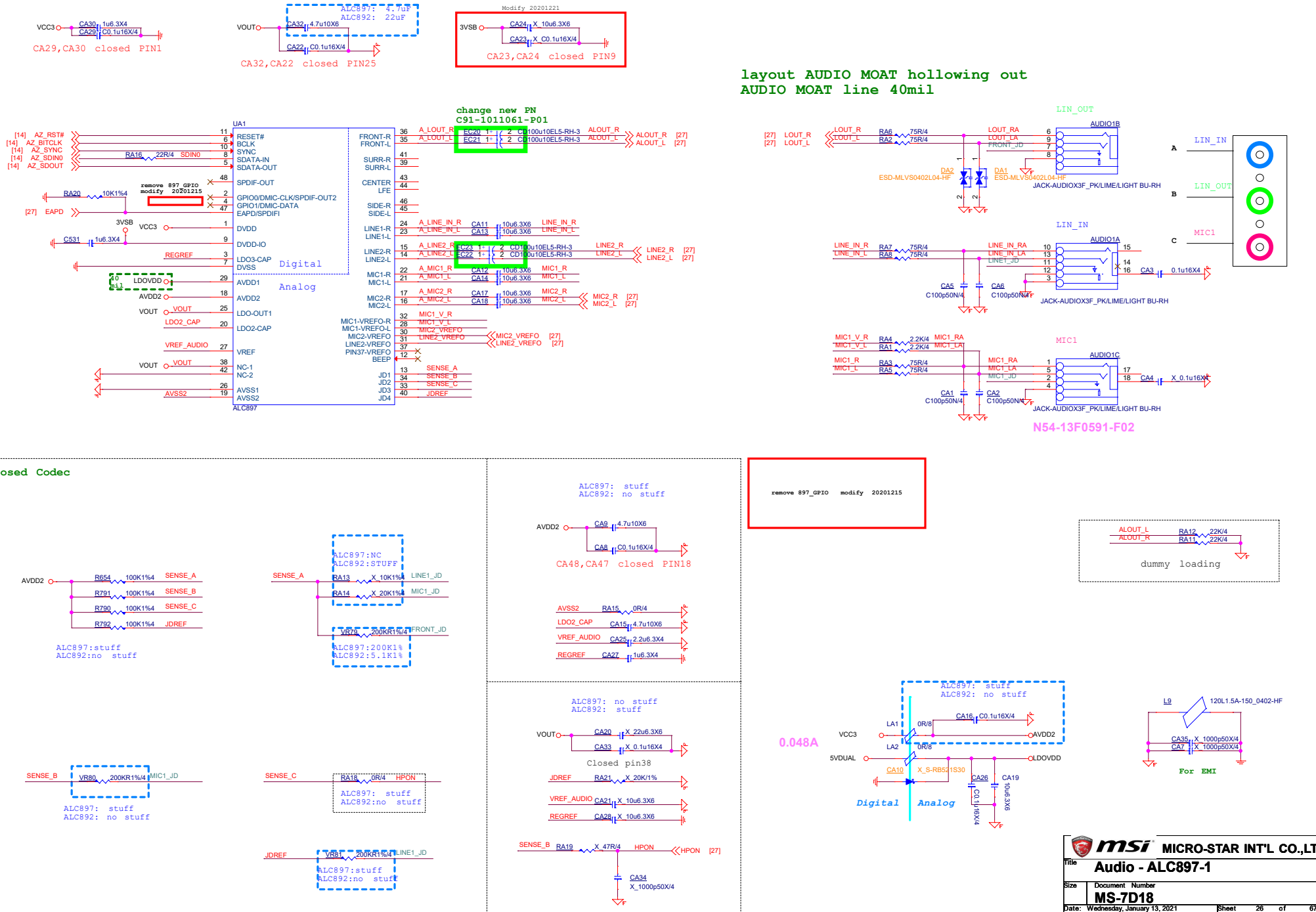


MICRO-STAR INT'L CO.,LTD.

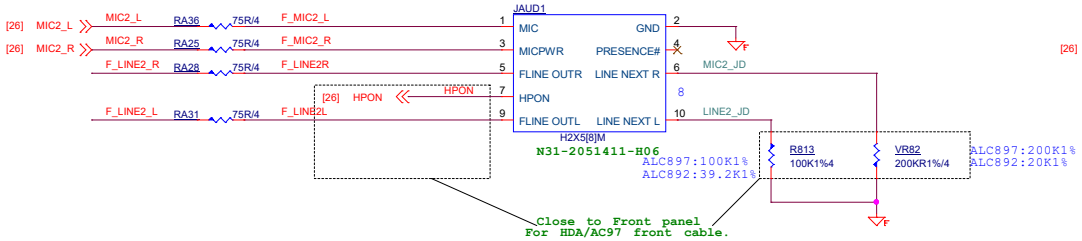
Title: SYSTEM FAN1+2

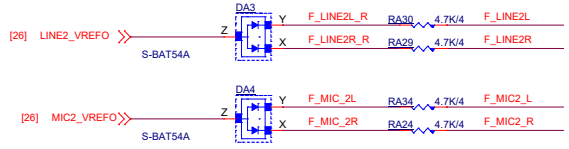
Size | Document Number: MS-7D18 | Rev: 1.0

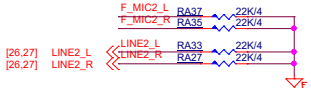
Date: Wednesday, January 13, 2021 | Sheet 25 of 67

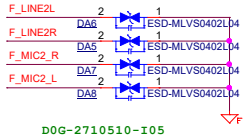


MICRO-STAR INT'L CO.,LTD.			
Title: Audio - ALC897-1			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 26 of 67		





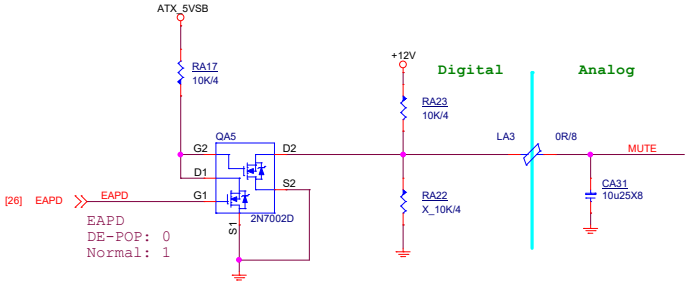




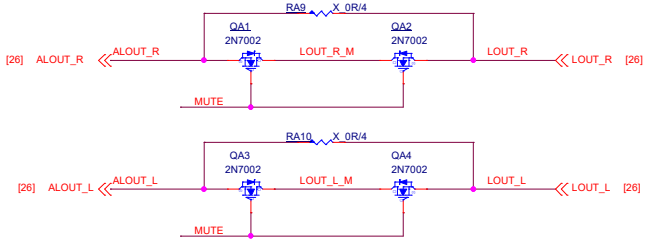
ESD protect

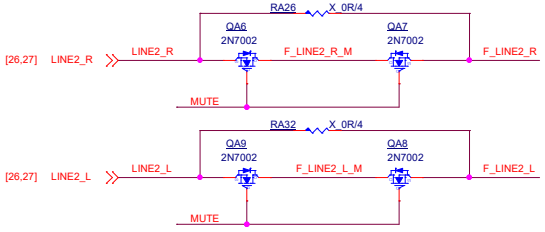
D0G-2710510-I05
AVL:D0G-2950500-SI0

De-POP circuit



LIN_OUT



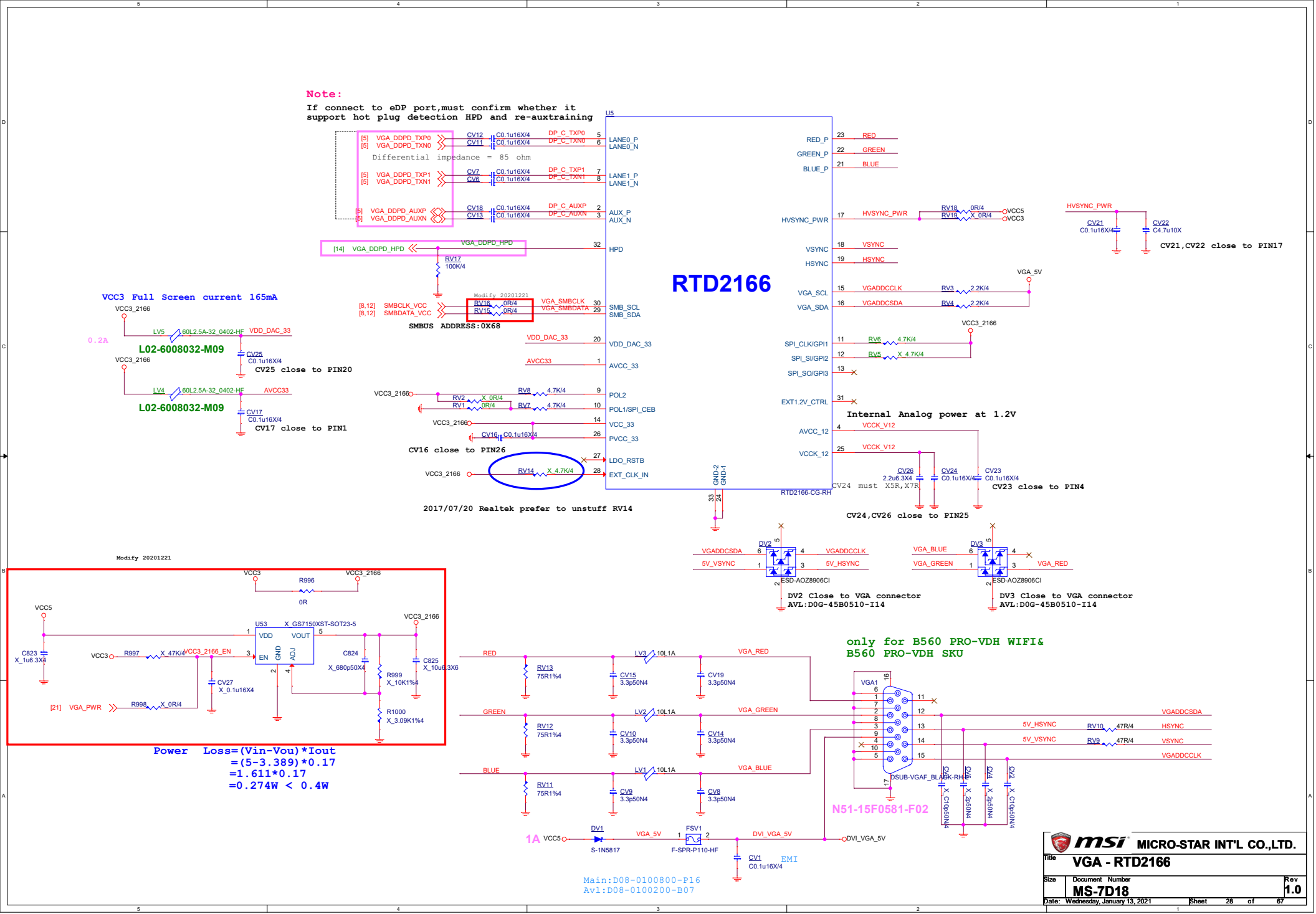


MICRO-STAR INT'L CO.,LTD.

Title	Audio - ALC897-2	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 27 of 67	

Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



Modify 20201221

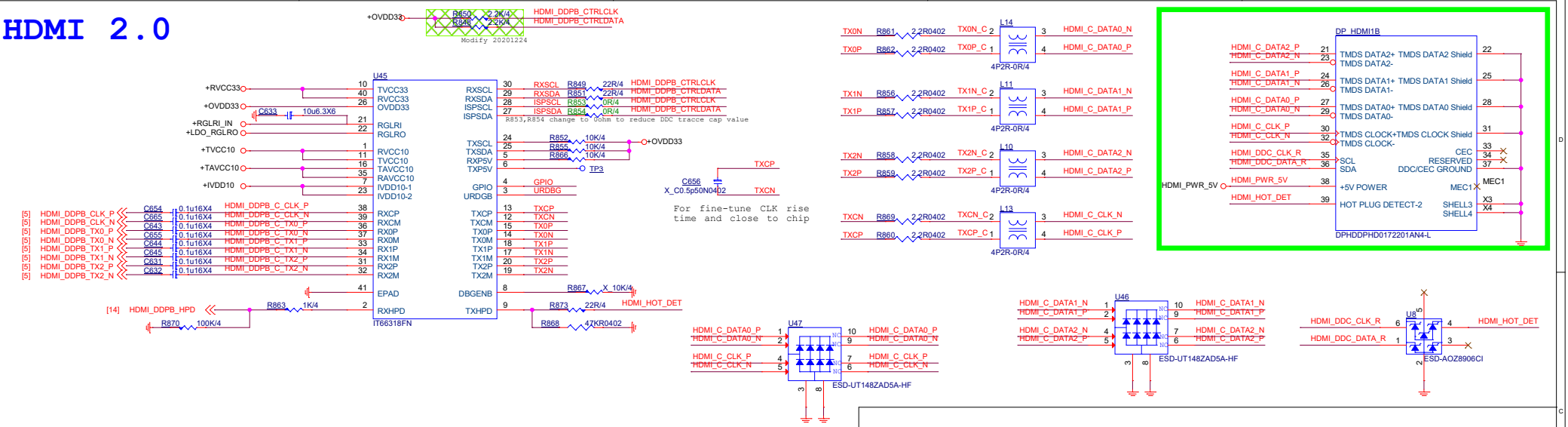
Power Loss=(Vin-Vou)*Iout
=(5-3.389)*0.17
=1.611*0.17
=0.274W < 0.4W

only for B560 PRO-VDH WIFI& B560 PRO-VDH SKU

Main:D08-0100800-P16
Avl:D08-0100200-B07

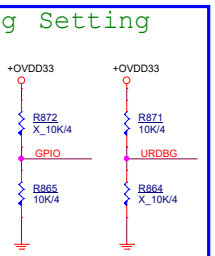
MICRO-STAR INT'L CO.,LTD.			
Title: VGA - RTD2166			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 28 of 67		

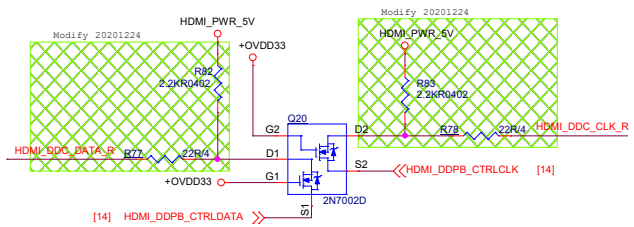
HDMI 2.0



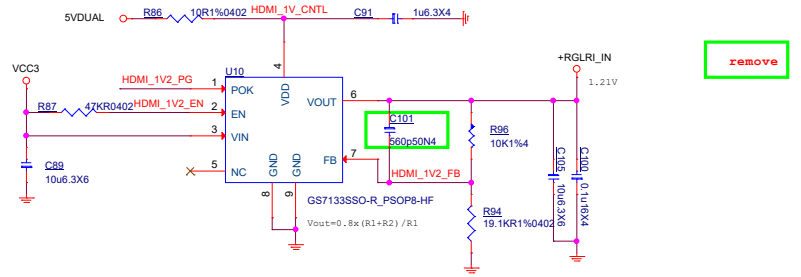
Reserved Trapping Setting

Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1



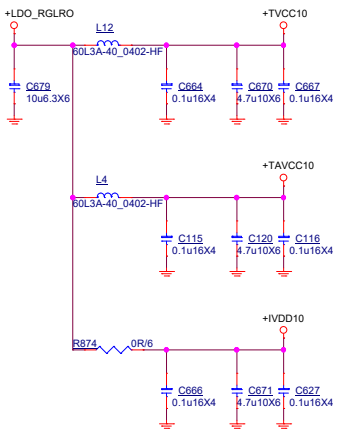


HDMI 1.2V



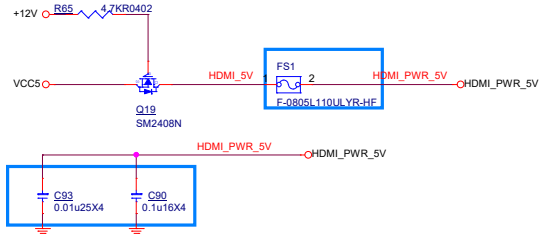
HDMI 1V

224mA

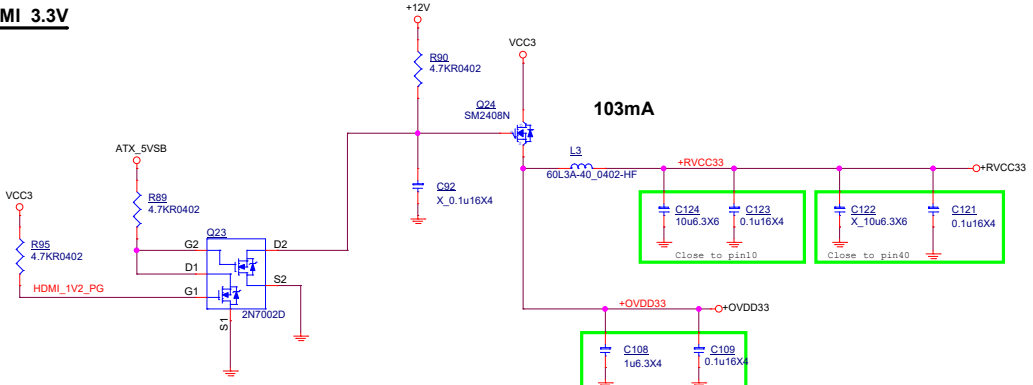


HDMI 5V

Add common-mode choke for EMI and close to connector



HDMI 3.3V

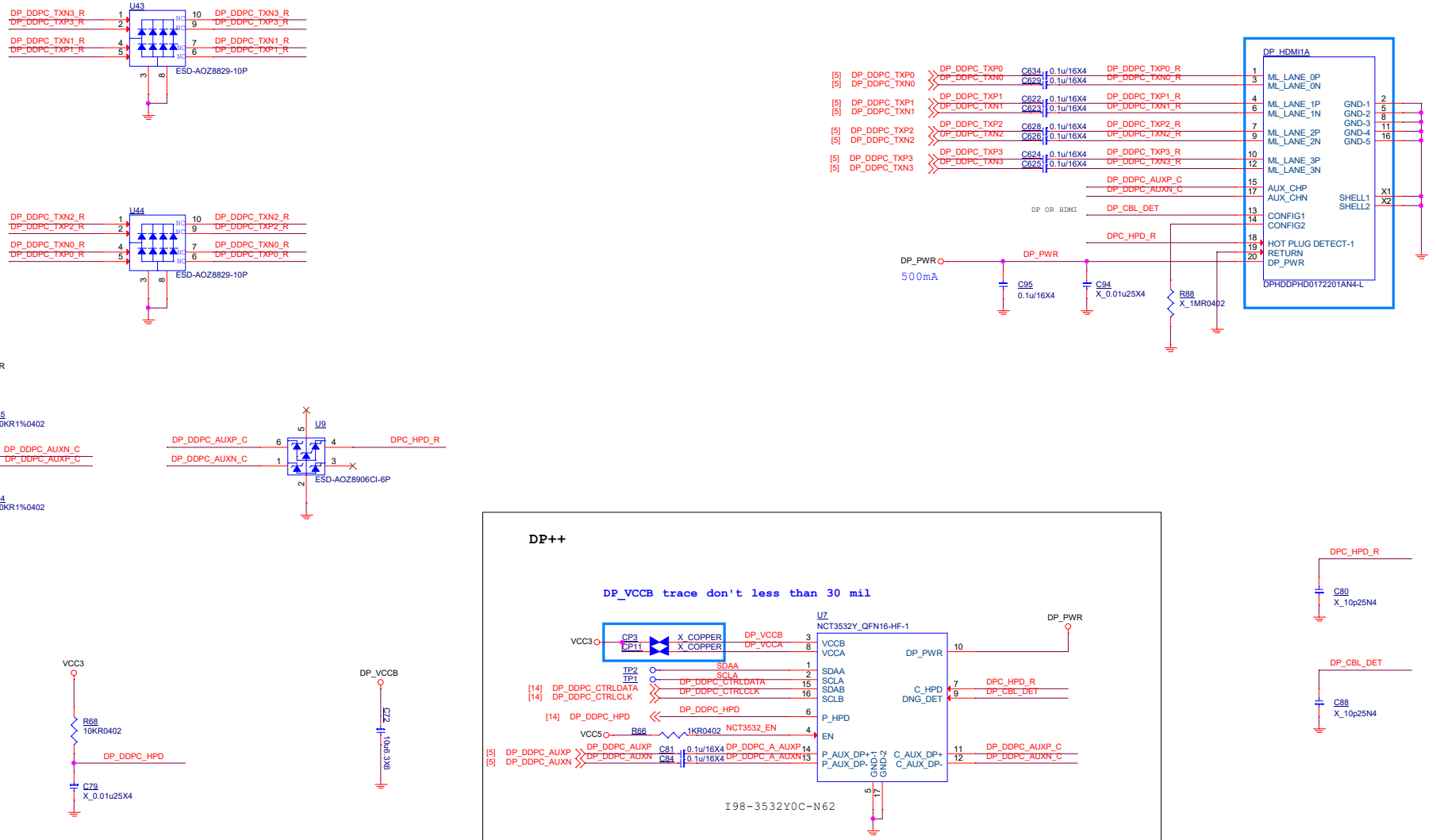


MICRO-STAR INT'L CO.,LTD.

Title: HDMI Connector

Size	Document Number	Rev
	MS-7D18	1.0

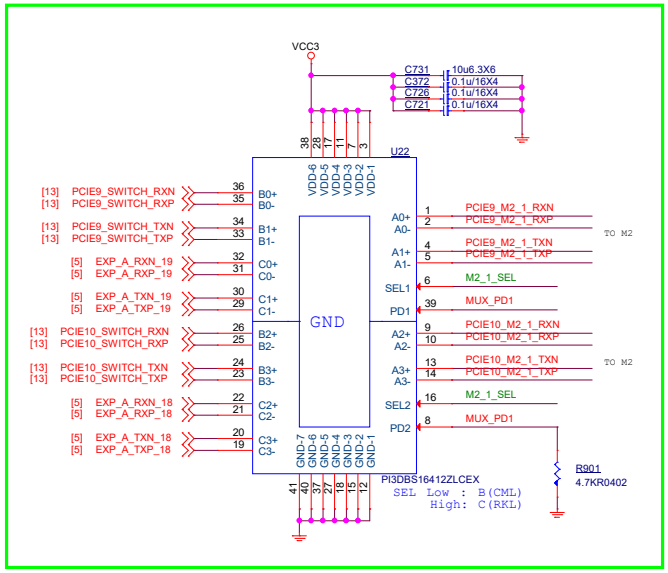
Date: Wednesday, January 13, 2021 Sheet 29 of 67

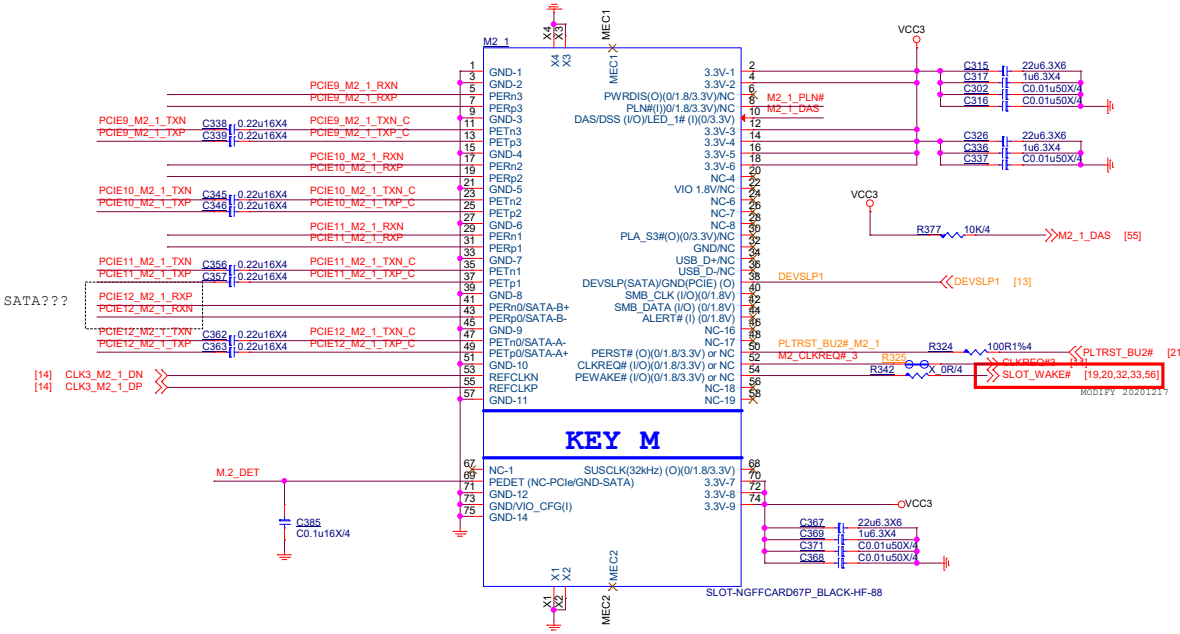


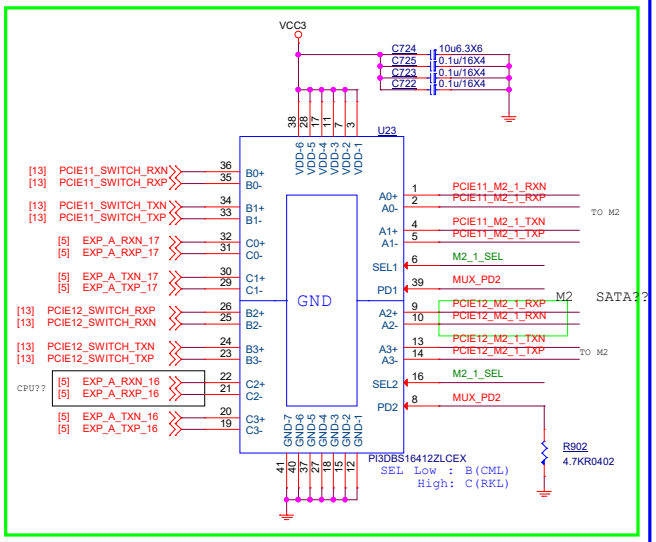
MICRO-STAR INT'L CO.,LTD.			
Title: DP Connector			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 30 of 67		

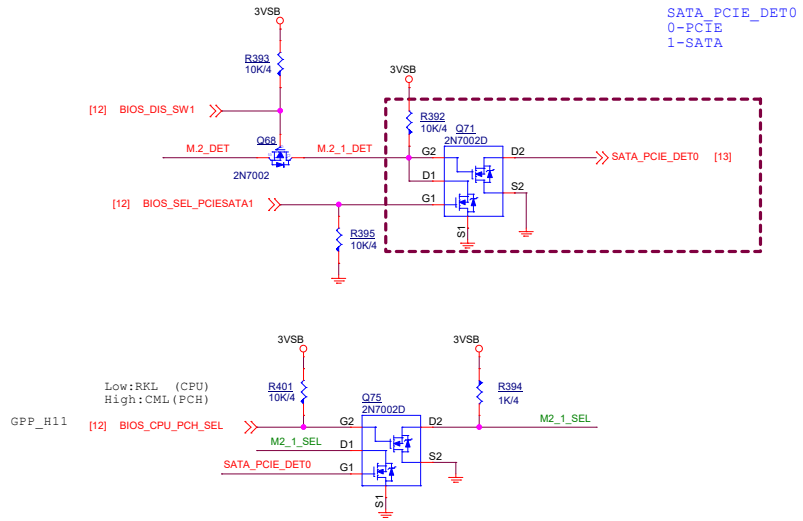
M.2 Connector

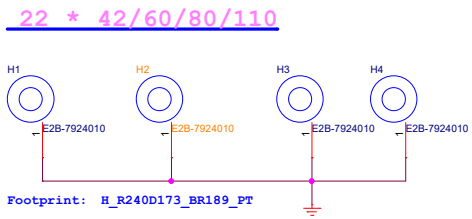
VCC3 - 2.5A

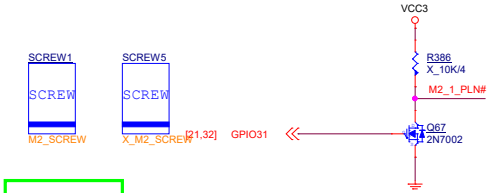


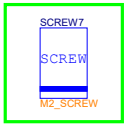












For HS Cover

BIOS_MODE

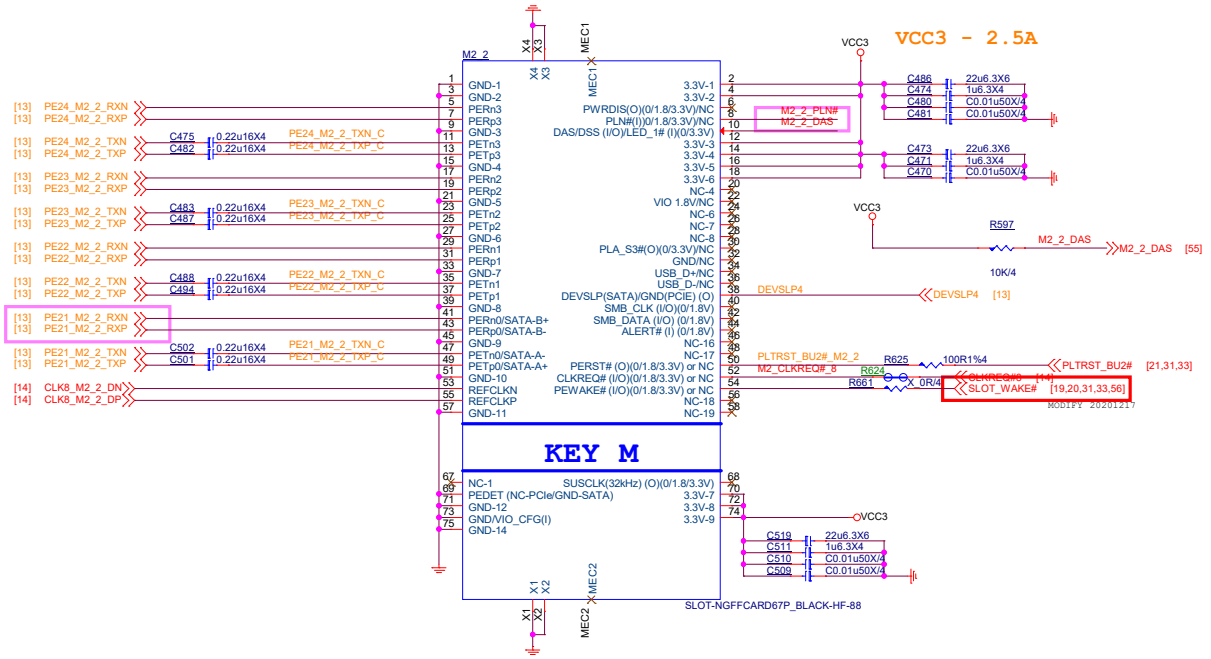
BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
GPO(0)	GPO(1)	M2-SATA
GPO(0)	GPO(0)	M2-PCIE
GPI	GPI	AUTO

BIOS_MODE

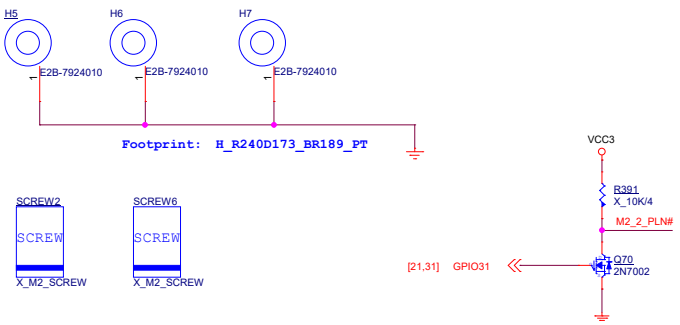
BIOS_CPU_PCH_SEL GPP_H11	
GPI(1)	CML(PCH)
GPO(0)	RKL(CPU)

MICRO-STAR INT'L CO.,LTD.

Title: M2_1		
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 31 of 67	

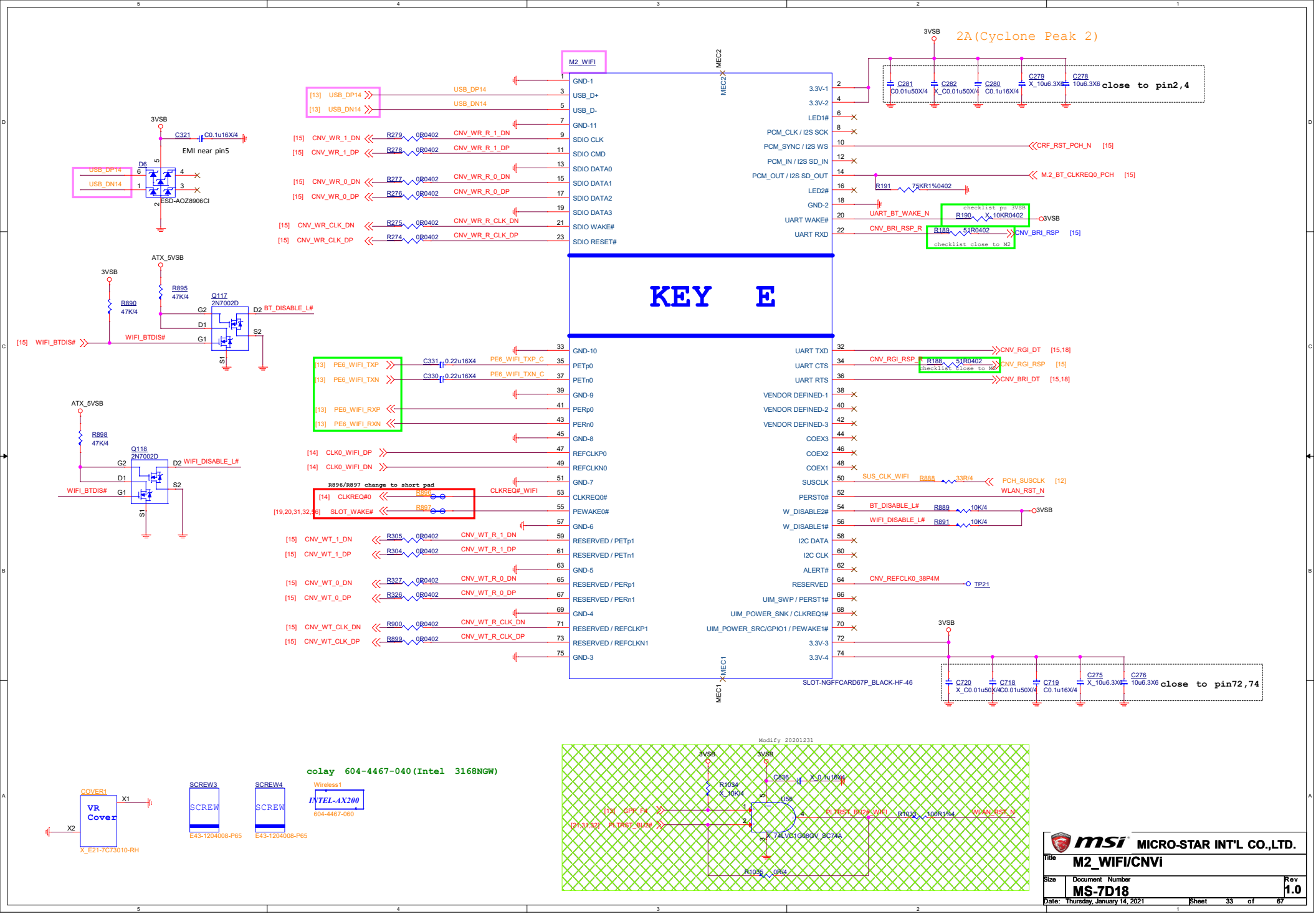


22 * 42/60/80

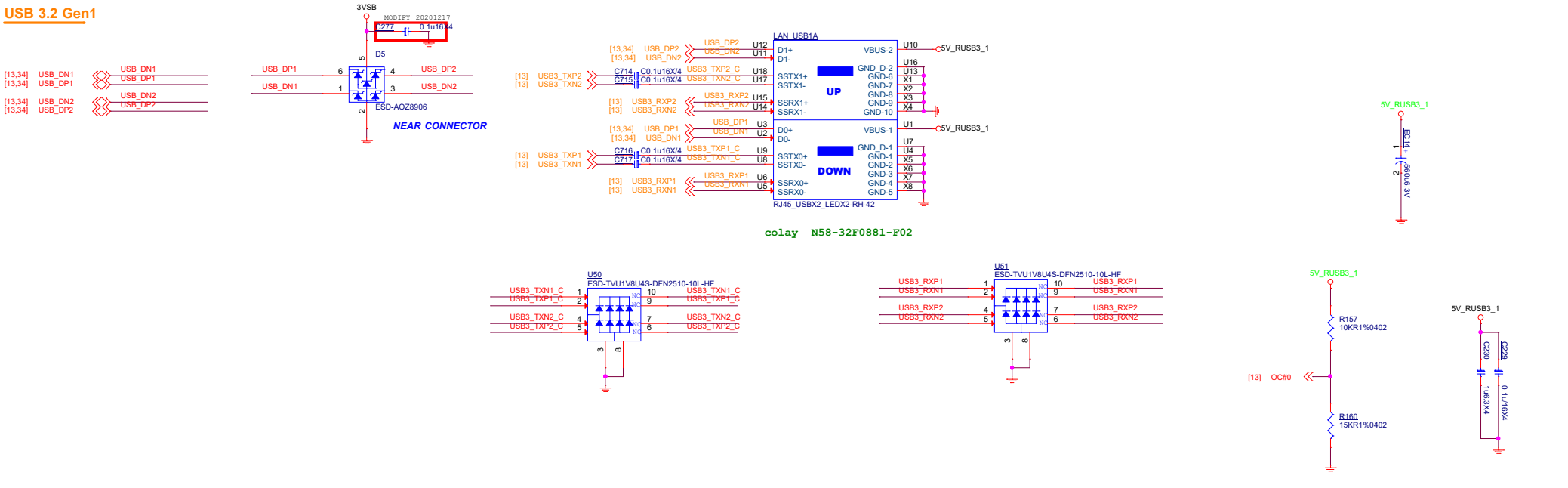


MICRO-STAR INT'L CO.,LTD.

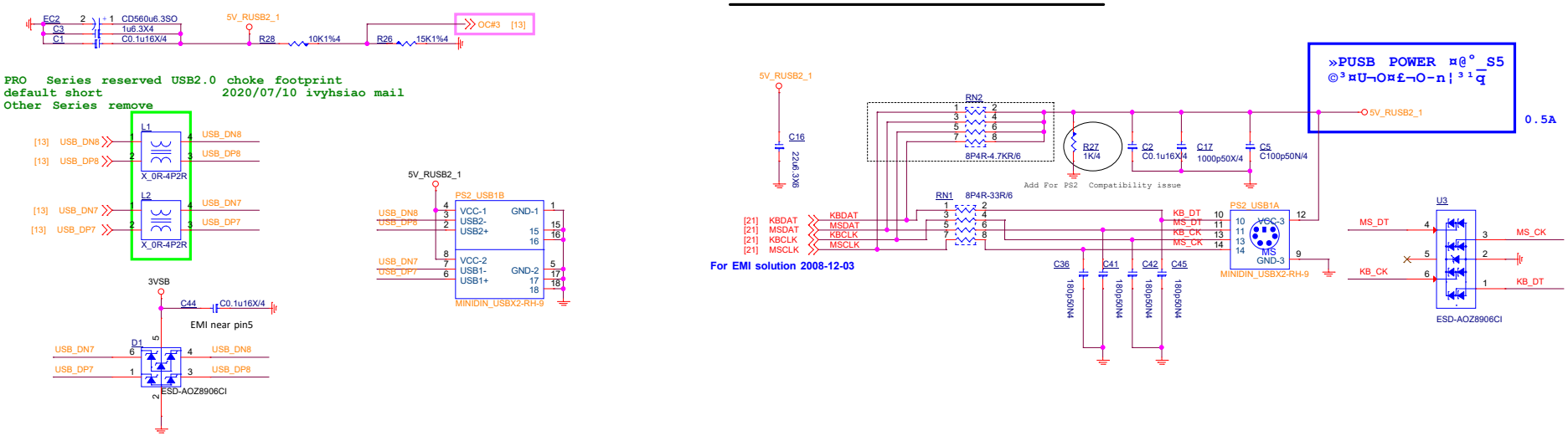
Title	M2_2	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 32 of 67	


2A(Cyclone Peak 2)
M2_WIFI
MEC2
KEY E
MEC1
SLOT-NGFFCARD67P_BLACK-HF-46
GND-1
USB_D+
USB_D-
GND-11
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
SDIO DATA2
SDIO DATA3
SDIO WAKE#
SDIO RESET#
GND-10
PETp0
PETn0
GND-9
PERp0
PERn0
GND-8
REFCLKP0
REFCLKN0
GND-7
CLKREQ0#
PEWAKE0#
GND-6
RESERVED / PETp1
RESERVED / PETn1
GND-5
RESERVED / PERp1
RESERVED / PERn1
GND-4
RESERVED / REFCLKP1
RESERVED / REFCLKN1
GND-3
3.3V-1
3.3V-2
LED1#
PCM_CLK / I2S SCK
PCM_SYNC / I2S WS
PCM_IN / I2S SD_IN
PCM_OUT / I2S SD_OUT
LED2#
GND-2
UART WAKE#
UART RXD
UART TXD
UART CTS
UART RTS
VENDOR DEFINED-1
VENDOR DEFINED-2
VENDOR DEFINED-3
COEX3
COEX2
COEX1
SUSCLK
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C DATA
I2C CLK
ALERT#
RESERVED
UIM_SWP / PERST1#
UIM_POWER_SNK / CLKREQ1#
UIM_POWER_SRC/GPIO1 / PEWAKE1#
3.3V-3
3.3V-4
close to pin2,4
close to pin72,74
checklist pu 3VSB
checklist close to M2
R896/R897 change to short pad
colay 604-4467-040(Intel 3168NGW)
Modify 20201231
INTEL-AX200
604-4467-060
ESD-AOZ8906CI
EMI near pin5
VR Cover
X_E21-7C73010-RH
E43-1204008-P65
MICRO-STAR INT'L CO.,LTD.
M2_WIFI/CNVi
MS-7D18
1.0
Thursday, January 14, 2021
33
67

USB 3.2 Gen1



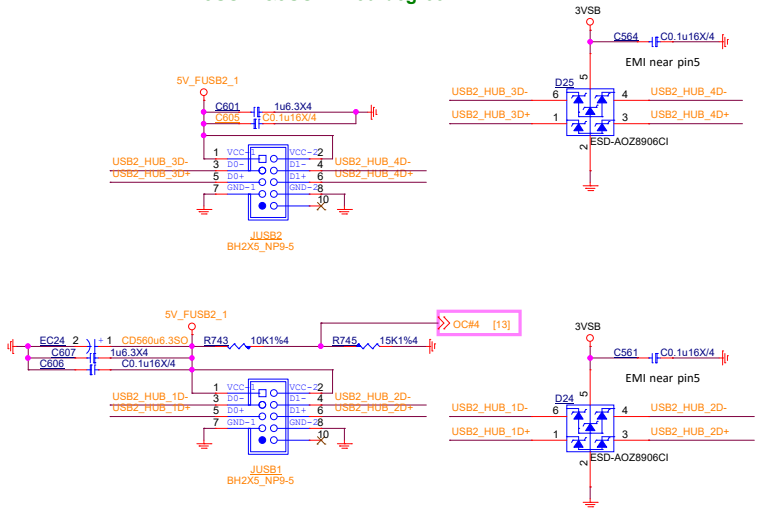
USB 2.0



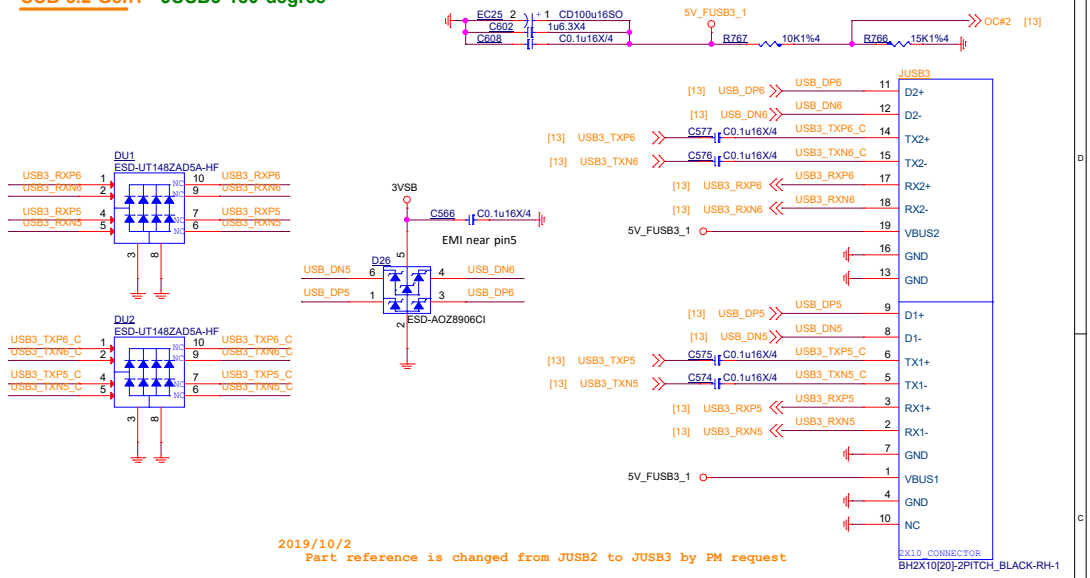
MICRO-STAR INT'L CO.,LTD.			
Title: Rear USB3.2/USB2.0/PS2			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Thursday, January 14, 2021	Sheet 34 of 67		

USB 2.0

JUSB1&JUSB2 180 degree

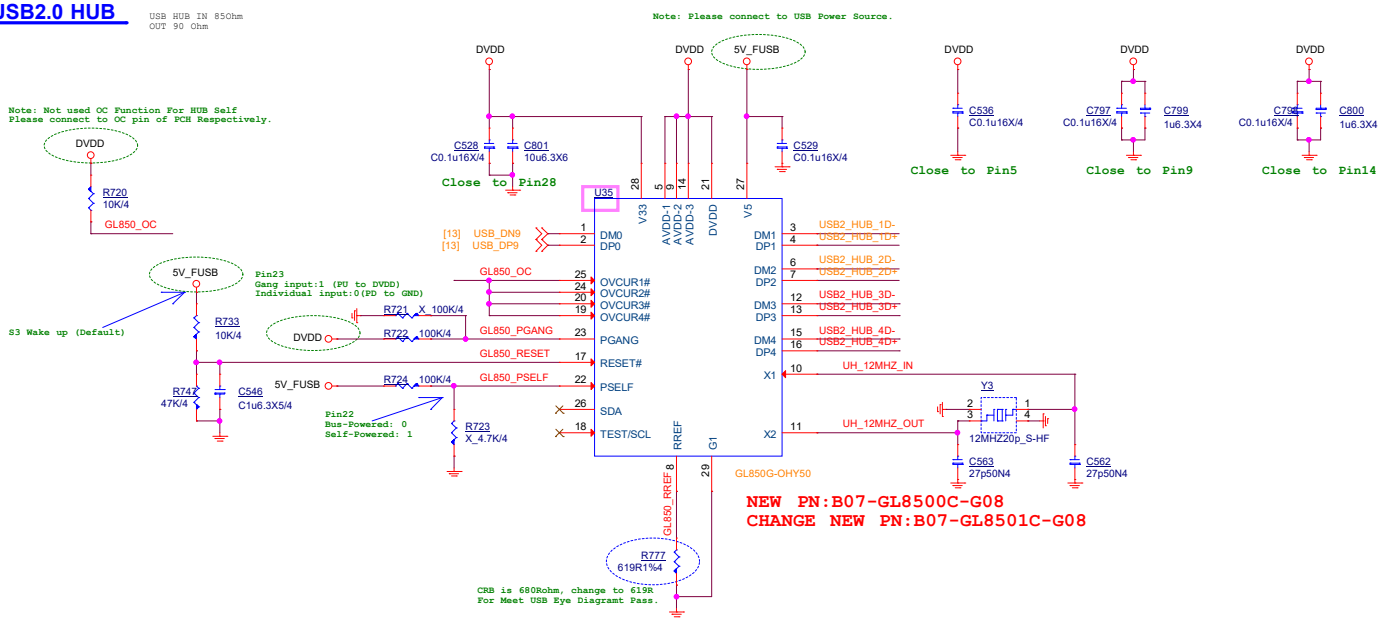


USB 3.2 Gen1 JUSB3 180 degree



2019/10/2
Part reference is changed from JUSB2 to JUSB3 by PM request

GL850G USB2.0 HUB



NEW PN:B07-GL8500C-G08
CHANGE NEW PN:B07-GL8501C-G08

MICRO-STAR INT'L CO.,LTD.

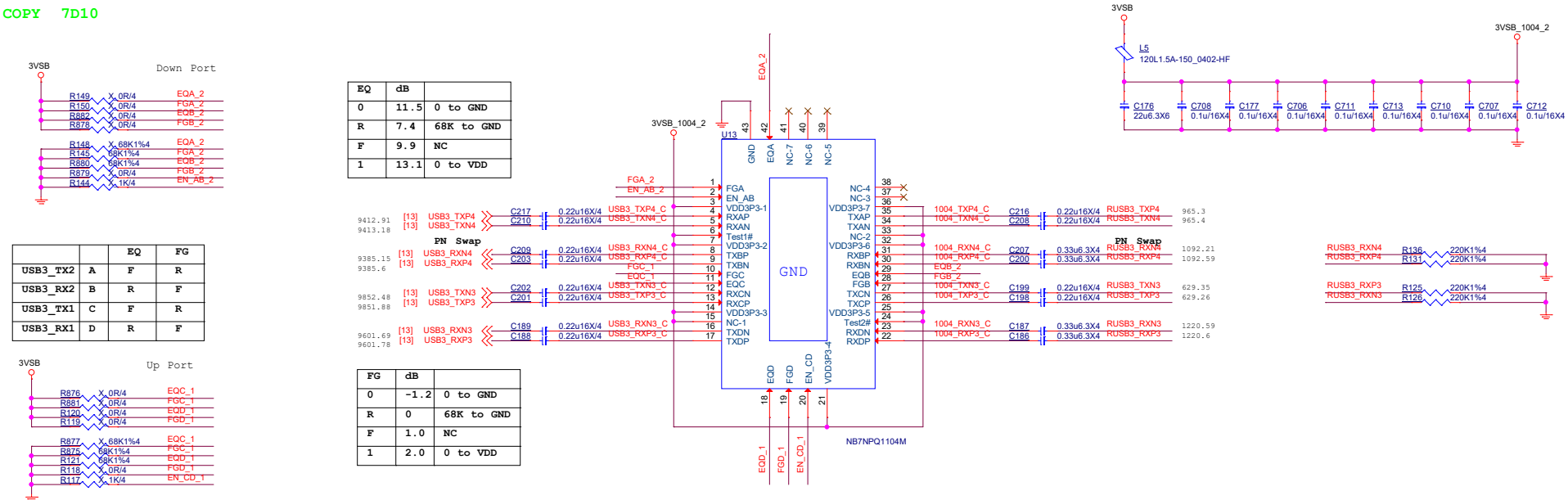
Title: Front USB3.2/USB2.0/GL850HUB

Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 35 of 67

Rear USB3.1 Redriver

COPY 7D10

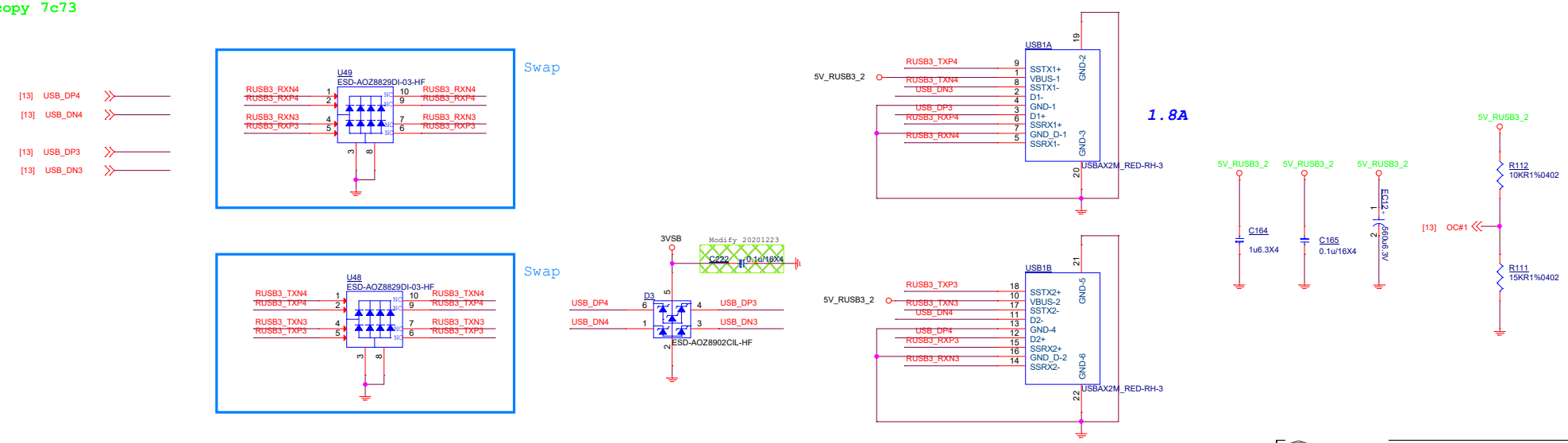


EQ	dB	
0	11.5	0 to GND
R	7.4	68K to GND
F	9.9	NC
1	13.1	0 to VDD

FG	dB	
0	-1.2	0 to GND
R	0	68K to GND
F	1.0	NC
1	2.0	0 to VDD

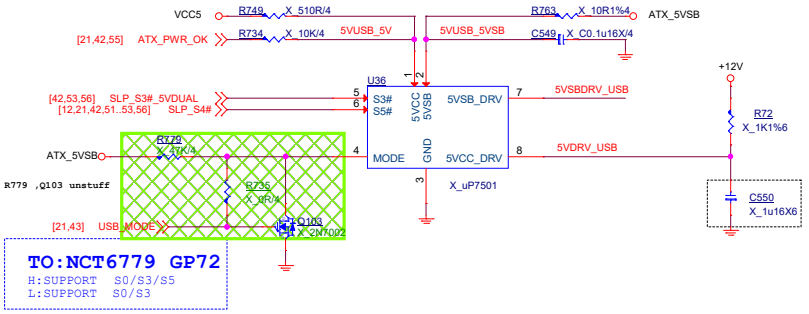
		EQ	FG
USB3_TX2	A	F	R
USB3_RX2	B	R	F
USB3_TX1	C	F	R
USB3_RX1	D	R	F

change
copy 7c73



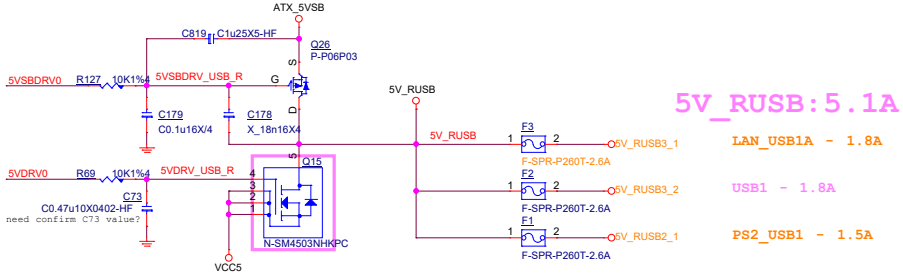
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	USB3.2 GEN2	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Thursday, January 14, 2021	Sheet 36 of 67	

USB POWER



5VSBDRV_DIMM, 5VCCDRV_DIMM width 12mil,
Do NOT route near the edge of a board.

REAR USB PORT POWER



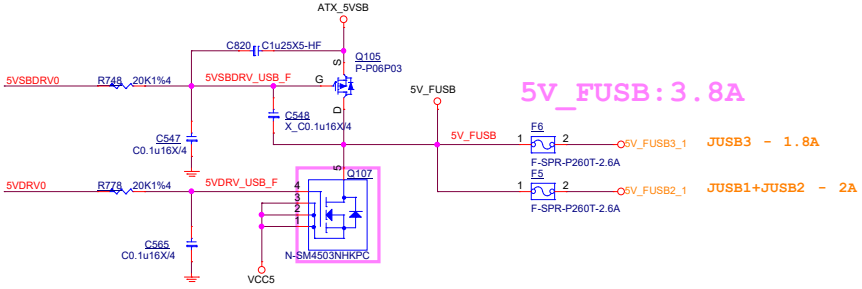
5V_RUSB:5.1A

LAN_USB1A - 1.8A

USB1 - 1.8A

PS2_USB1 - 1.5A

FRONT USB PORT POWER



5V_FUSB:3.8A

JUSB3 - 1.8A

JUSB1+JUSB2 - 2A

MICRO-STAR INT'L CO.,LTD.

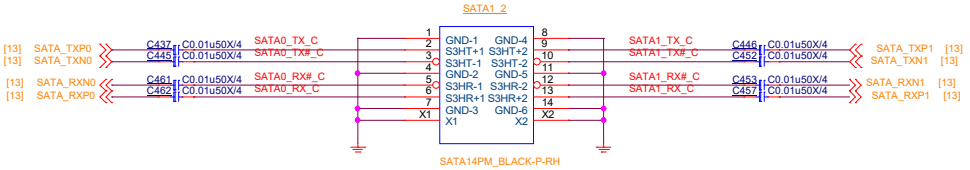
Title: USB /PS2 Power

Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 37 of 67

SATA PORT 0,1

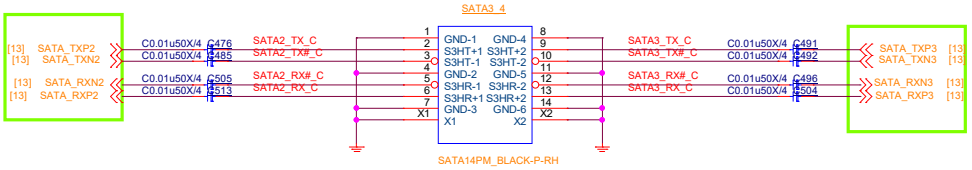
Black 90 degree



ADD SATA3_4

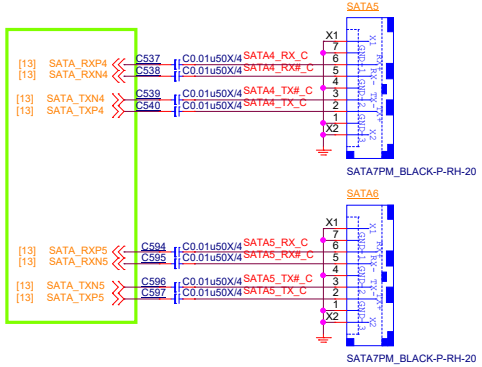
SATA PORT 2,3

Black 90 degree



SATA PORT 4,5

Black 180 degree



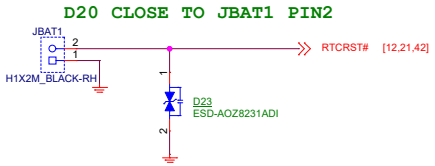
MICRO-STAR INT'L CO.,LTD.

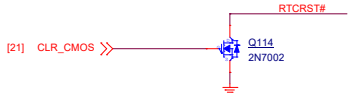
Title: SATA connector

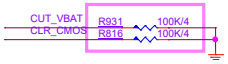
Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 38 of 67

CUT_VBAT/CLR_CMOS

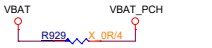


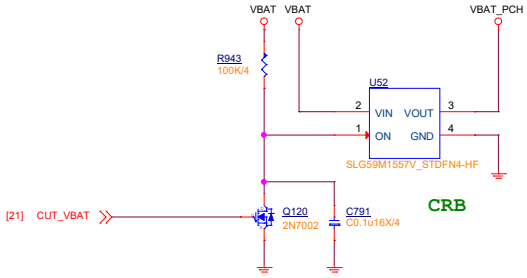


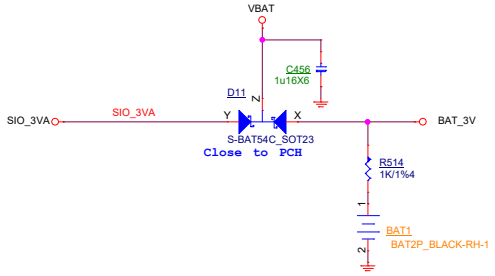


remove R930,R919,C792,Q119

VBAT







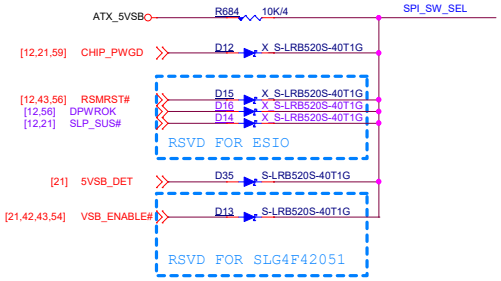
MICRO-STAR INT'L CO.,LTD.

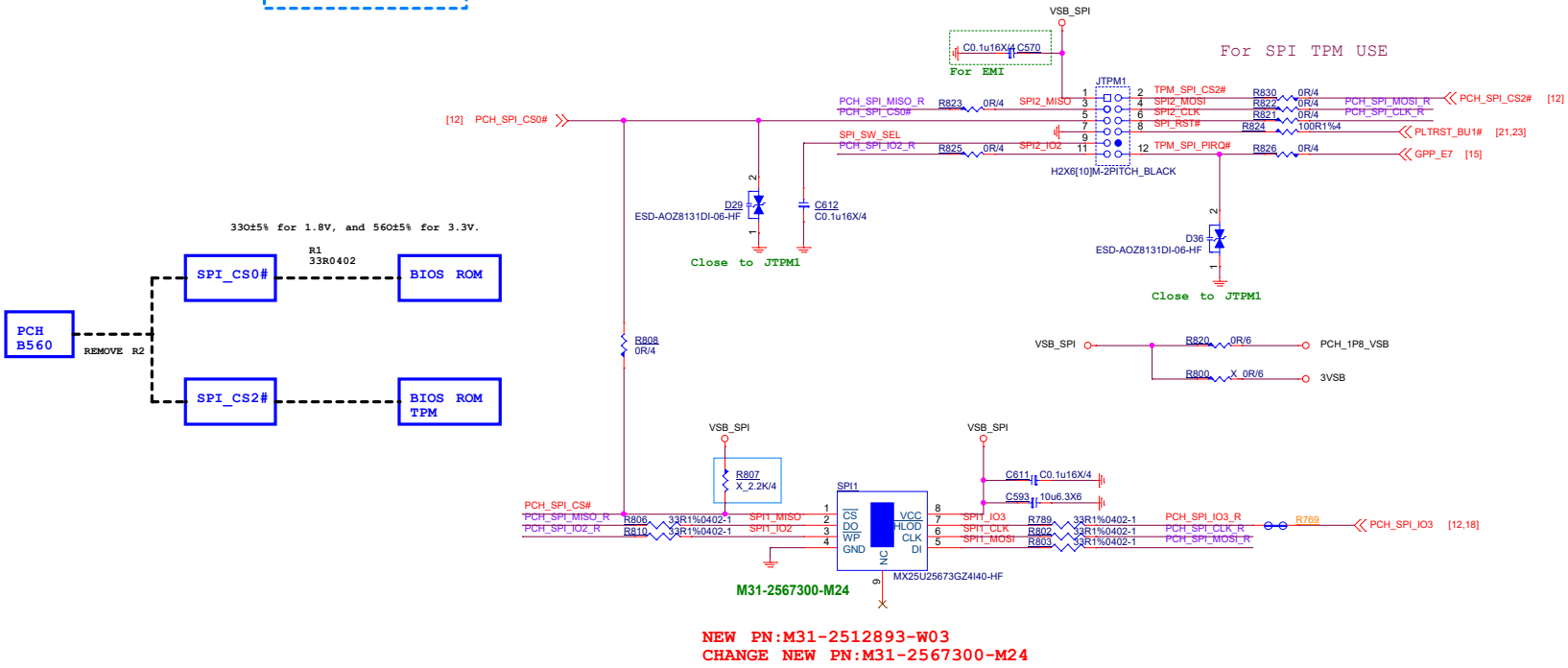
Title: VBAT Circuit

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 39 of 67

Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.





NEW PN:M31-2512893-W03
CHANGE NEW PN:M31-2567300-M24

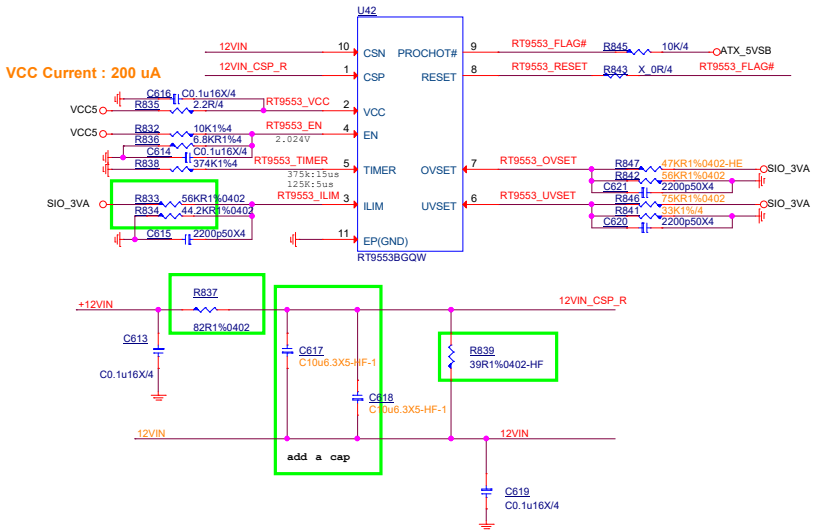
MICRO-STAR INT'L CO.,LTD.

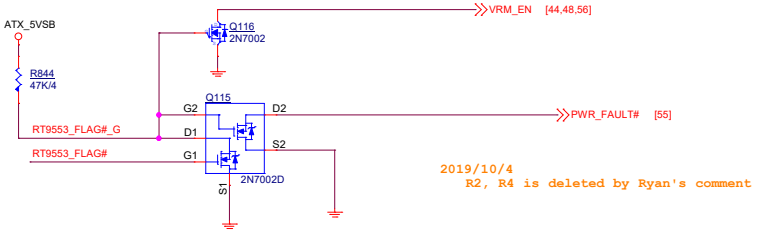
Title: BIOS ROM

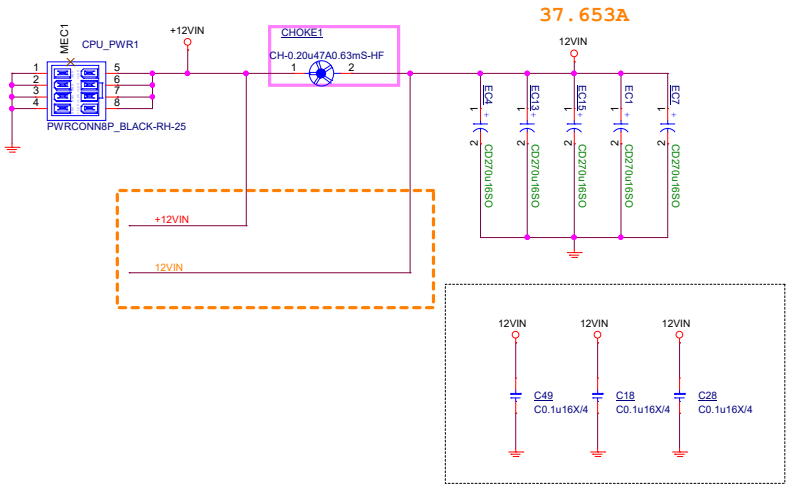
Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 40 of 67

OCP: 60A



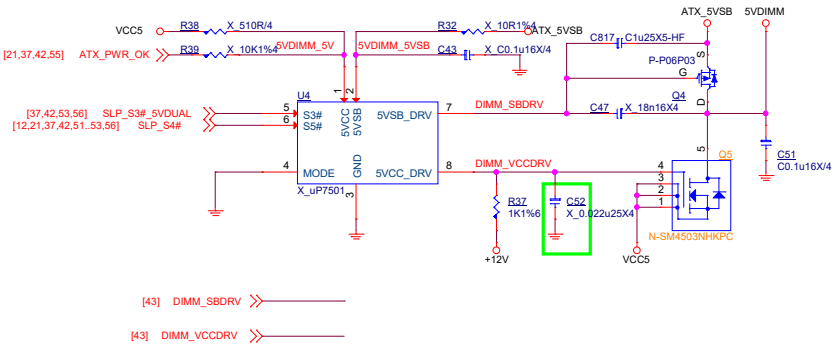




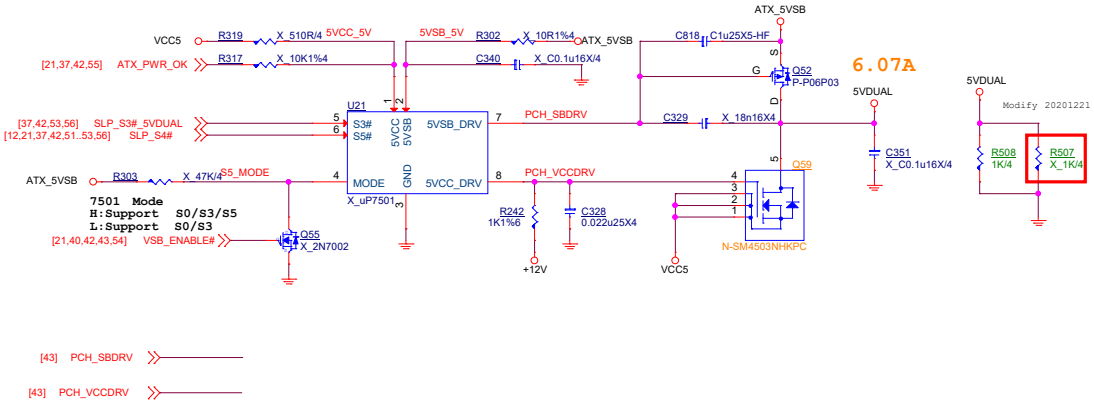
MICRO-STAR INT'L CO.,LTD.		
Title: 12VIN/CURRENT SENSE-RT9553		
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 41 of 67	

5VDIMM FOR DDR and USB Port

7.389A

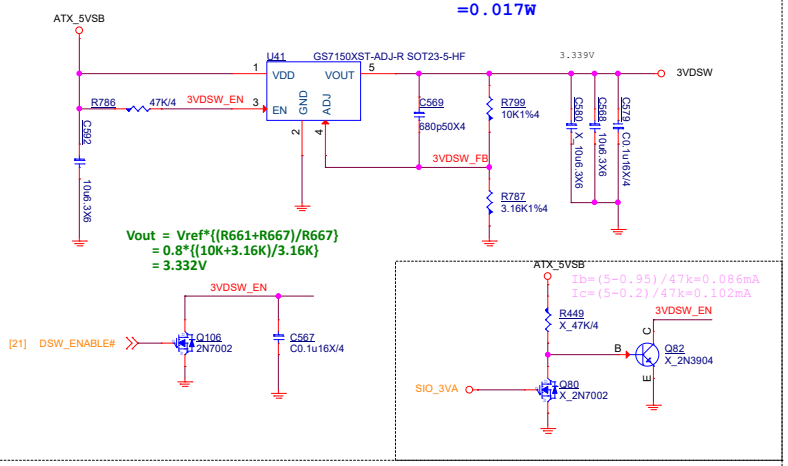


5VDUAL

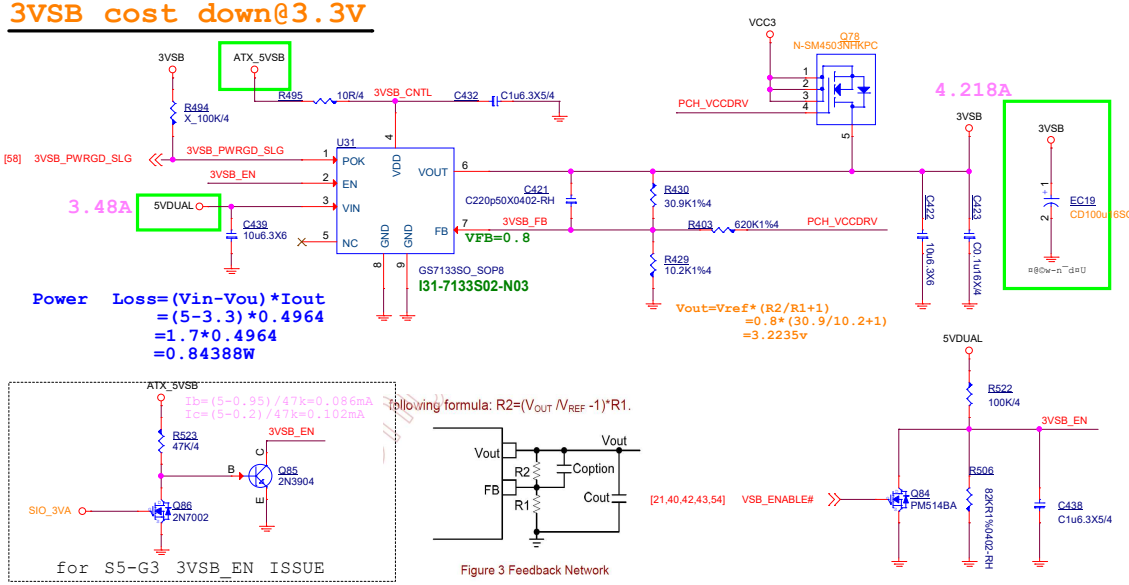


3VDSW

Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.01
=1.7*0.01
=0.017W



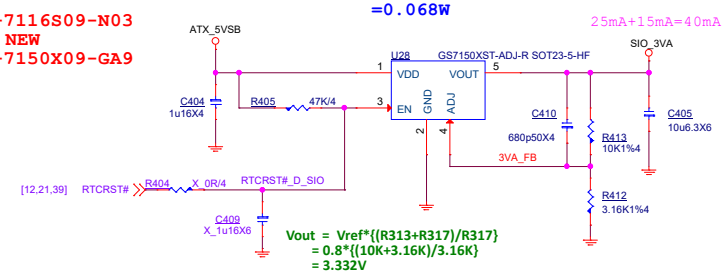
3VSB cost down@3.3V

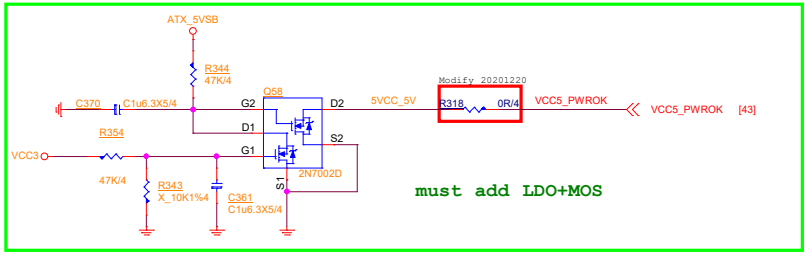


SIO 3VA

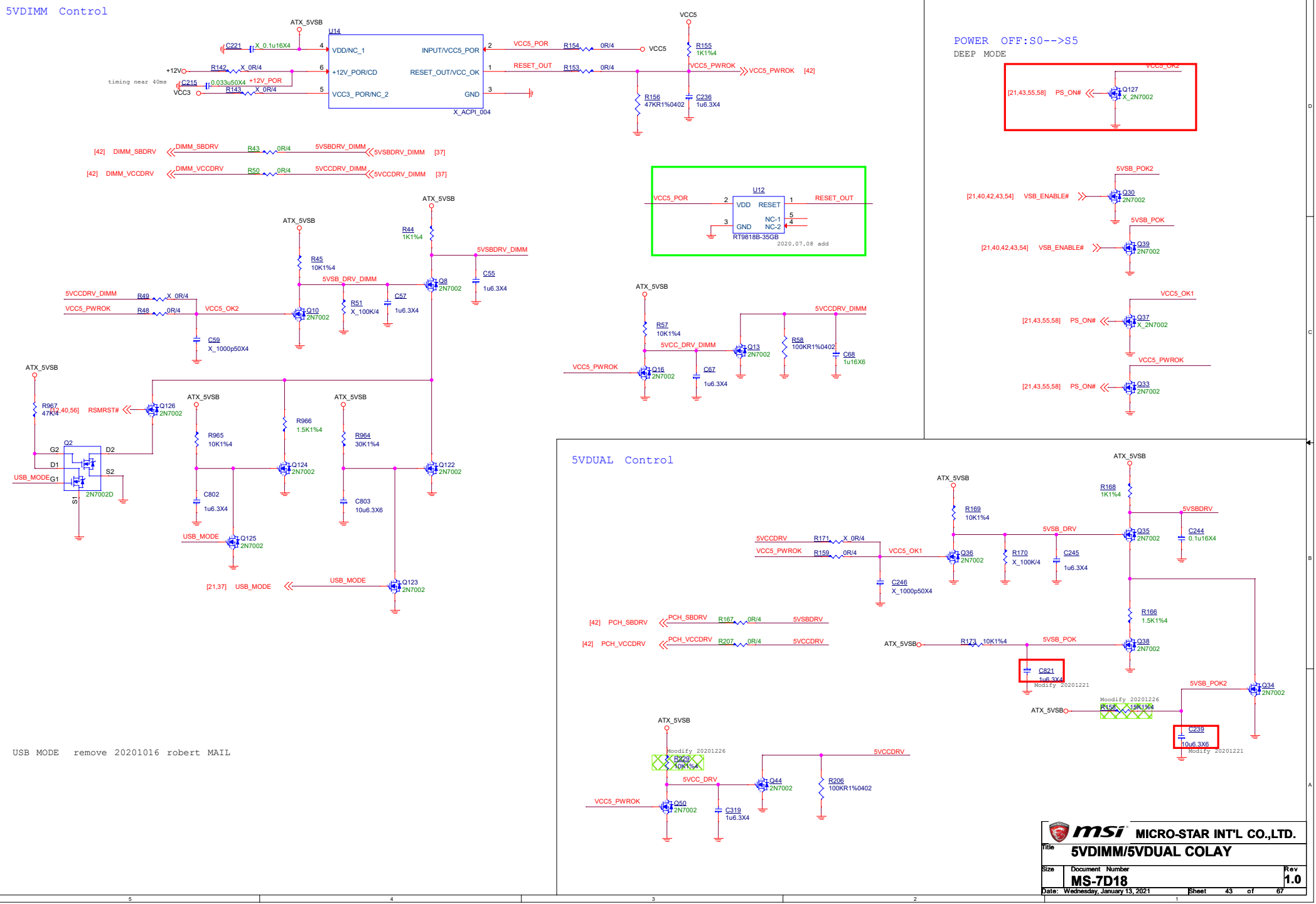
Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.04
=1.7*0.04
=0.068W

NEW
PN:I31-7116S09-N03
CHANGE NEW
PN:I31-7150X09-GA9



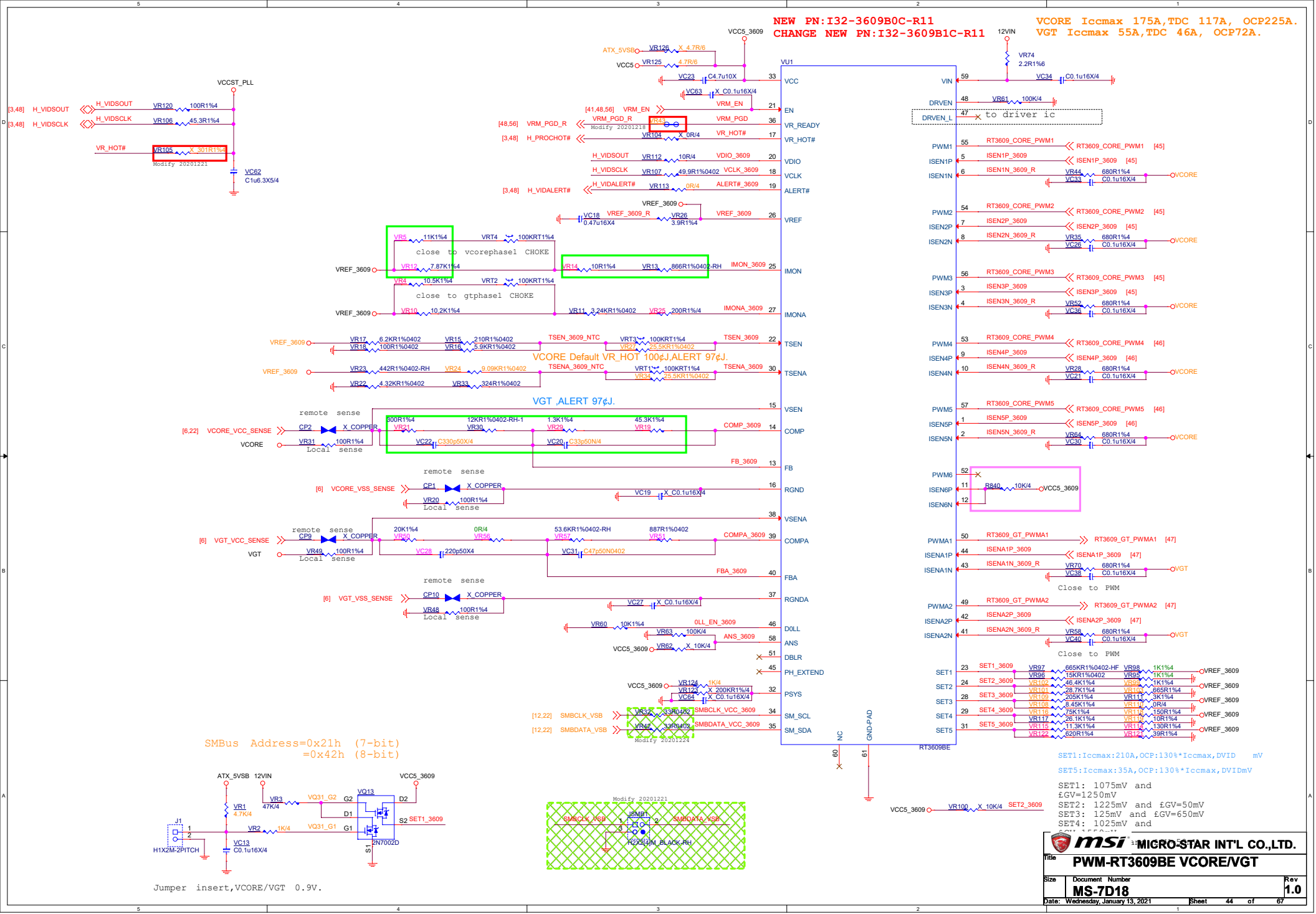


MSI MICRO-STAR INT'L CO.,LTD.		
Title: ACPI		
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 42 of 67	


5VDIMM Control
ATX_5VSB
U14
C221
X_0.1u16X4
VDD/NC_1
INPUT/VCC5_POR
VCC5_POR
R154
0R/4
VCC5
R155
1K1%4
+12V
R142
X_0R/4
+12V_POR/CD
RESET_OUT/VCC_OK
RESET_OUT
R153
0R/4
VCC5_PWROK
VCC5_PWROK [42]
timing near 40ms
C215
0.033u50X4
+12V_POR
VCC3
R143
X_0R/4
VCC3_ POR/NC_2
GND
X_ACPI_004
R156
47KR1%0402
C236
1u6.3X4
[42] DIMM_SBDRV
DIMM_SBDRV
R43
0R/4
5VSBDRV_DIMM
5VSBDRV_DIMM [37]
[42] DIMM_VCCDRV
DIMM_VCCDRV
R50
0R/4
5VCCDRV_DIMM
5VCCDRV_DIMM [37]
U12
VCC5_POR
VDD
RESET
RESET_OUT
NC-1
NC-2
GND
RT9818B-35GB
2020.07.08 add
R44
1K1%4
R45
10K1%4
5VSBDRV_DIMM
C55
1u6.3X4
5VSB_DRV_DIMM
Q8
2N7002
5VCCDRV_DIMM
R49
X_0R/4
VCC5_PWROK
R48
0R/4
VCC5_OK2
Q10
2N7002
R51
X_100K/4
C57
1u6.3X4
C59
X_1000p50X4
R57
10K1%4
5VCC_DRV_DIMM
Q13
2N7002
R58
100KR1%0402
C68
1u16X6
VCC5_PWROK
Q16
2N7002
C67
1u6.3X4
R967
47K/4
[21,40,56] RSMRST#
Q126
2N7002
Q2
G2
D2
D1
S2
G1
S1
2N7002D
USB_MODE
R965
10K1%4
R966
1.5K1%4
R964
30K1%4
Q124
2N7002
Q122
2N7002
C802
1u6.3X4
C803
10u6.3X6
USB_MODE
Q125
2N7002
[21,37] USB_MODE
USB_MODE
Q123
2N7002
POWER OFF:S0-->S5
DEEP MODE
VCC5_OK2
[21,43,55,58] PS_ON#
Q127
X_2N7002
5VSB_POK2
[21,40,42,43,54] VSB_ENABLE#
Q30
2N7002
5VSB_POK
[21,40,42,43,54] VSB_ENABLE#
Q39
2N7002
VCC5_OK1
[21,43,55,58] PS_ON#
Q37
X_2N7002
VCC5_PWROK
[21,43,55,58] PS_ON#
Q33
2N7002
5VDUAL Control
ATX_5VSB
R168
1K1%4
R169
10K1%4
5VSBDRV
C244
0.1u16X4
5VSB_DRV
5VCCDRV
R171
X_0R/4
VCC5_PWROK
R159
0R/4
VCC5_OK1
Q36
2N7002
R170
X_100K/4
C245
1u6.3X4
Q35
2N7002
C246
X_1000p50X4
R166
1.5K1%4
[42] PCH_SBDRV
PCH_SBDRV
R167
0R/4
5VSBDRV
[42] PCH_VCCDRV
PCH_VCCDRV
R207
0R/4
5VCCDRV
ATX_5VSB
R173
10K1%4
5VSB_POK
Q38
2N7002
C821
1u6.3X4
Modify 20201221
5VSB_POK2
Q34
2N7002
Moodify 20201226
R158
15K1%4
C239
10u6.3X6
Modify 20201221
Moodify 20201226
R329
10K1%4
5VCC_DRV
Q44
2N7002
R206
100KR1%0402
VCC5_PWROK
Q50
2N7002
C319
1u6.3X4
USB MODE remove 20201016 robert MAIL
MICRO-STAR INT'L CO.,LTD.
Title
5VDIMM/5VDUAL COLAY
Size
Document Number
MS-7D18
Rev
1.0
Date: Wednesday, January 13, 2021
Sheet 43 of 67

NEW PN:I32-3609B0C-R11
CHANGE NEW PN:I32-3609B1C-R11

VCORE Iccmax 175A,TDC 117A, OCP225A.
VGT Iccmax 55A,TDC 46A, OCP72A.

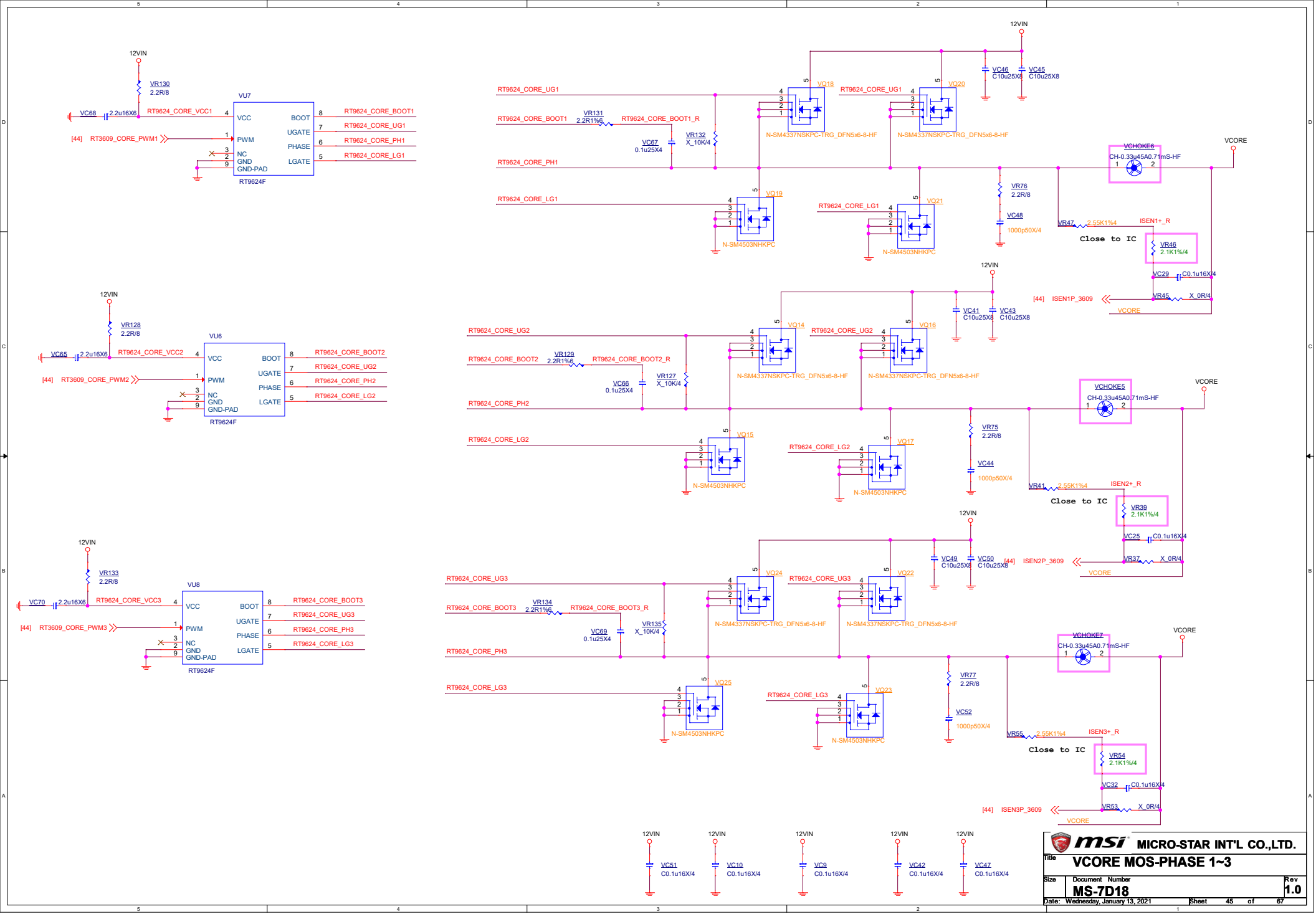


MICRO-STAR INT'L CO.,LTD.

Title: PWM-RT3609BE VCORE/VGT

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 44 of 67

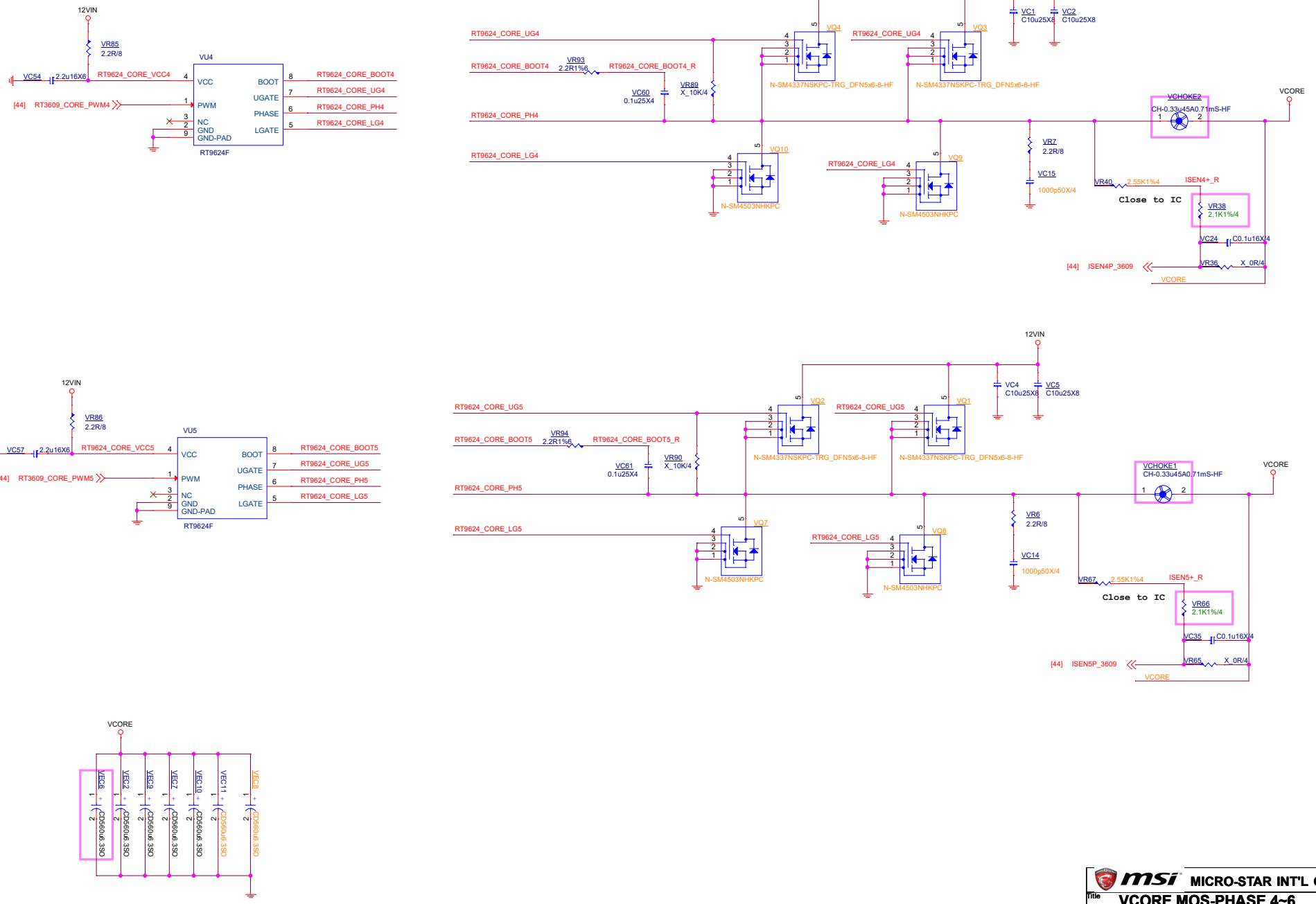


MICRO-STAR INT'L CO.,LTD.

Title: VCORE MOS-PHASE 1~3

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 45 of 67

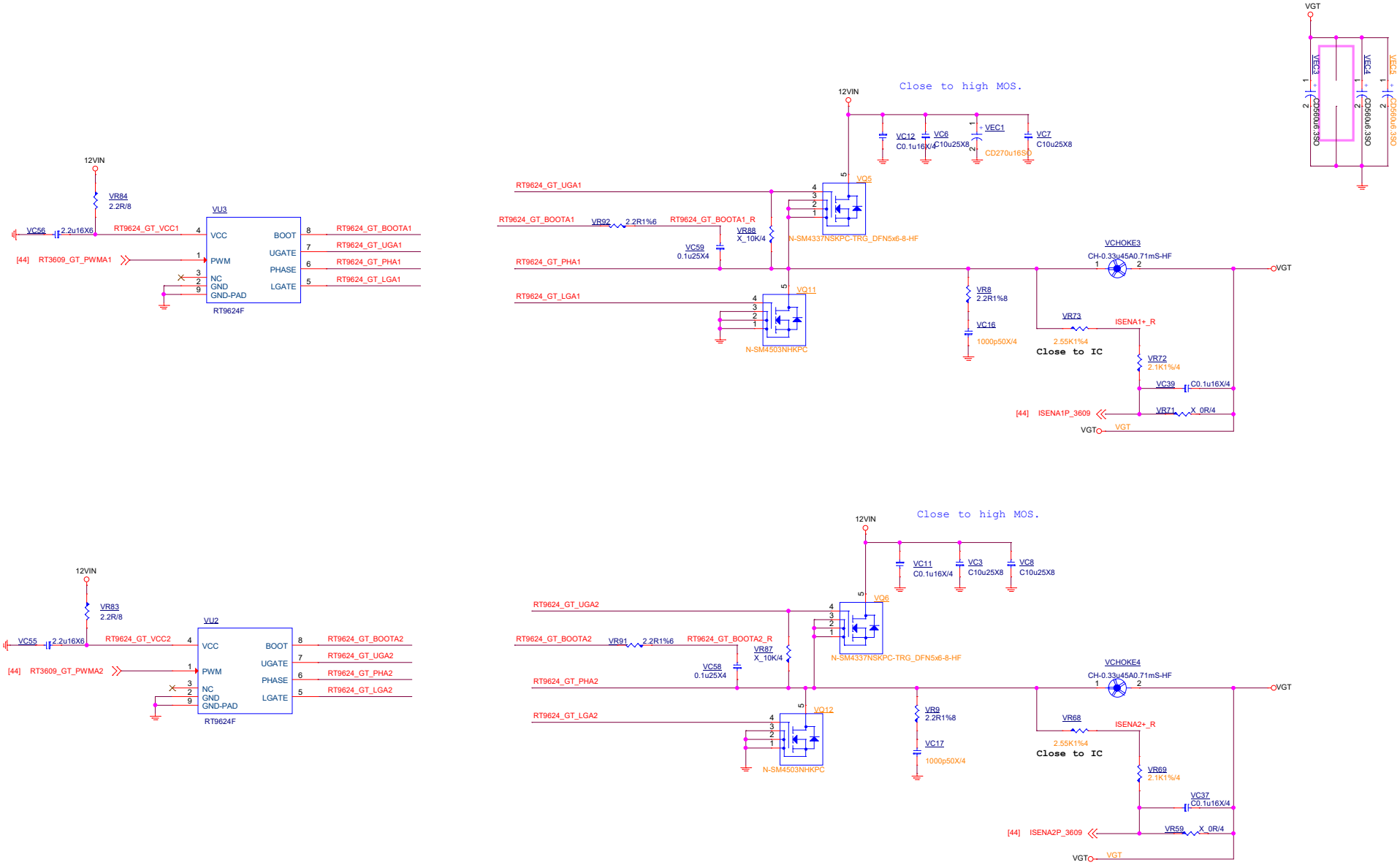


MICRO-STAR INT'L CO.,LTD.

Title: VCORE MOS-PHASE 4~6

Size	Document Number	Rev
	MS-7D18	1.0

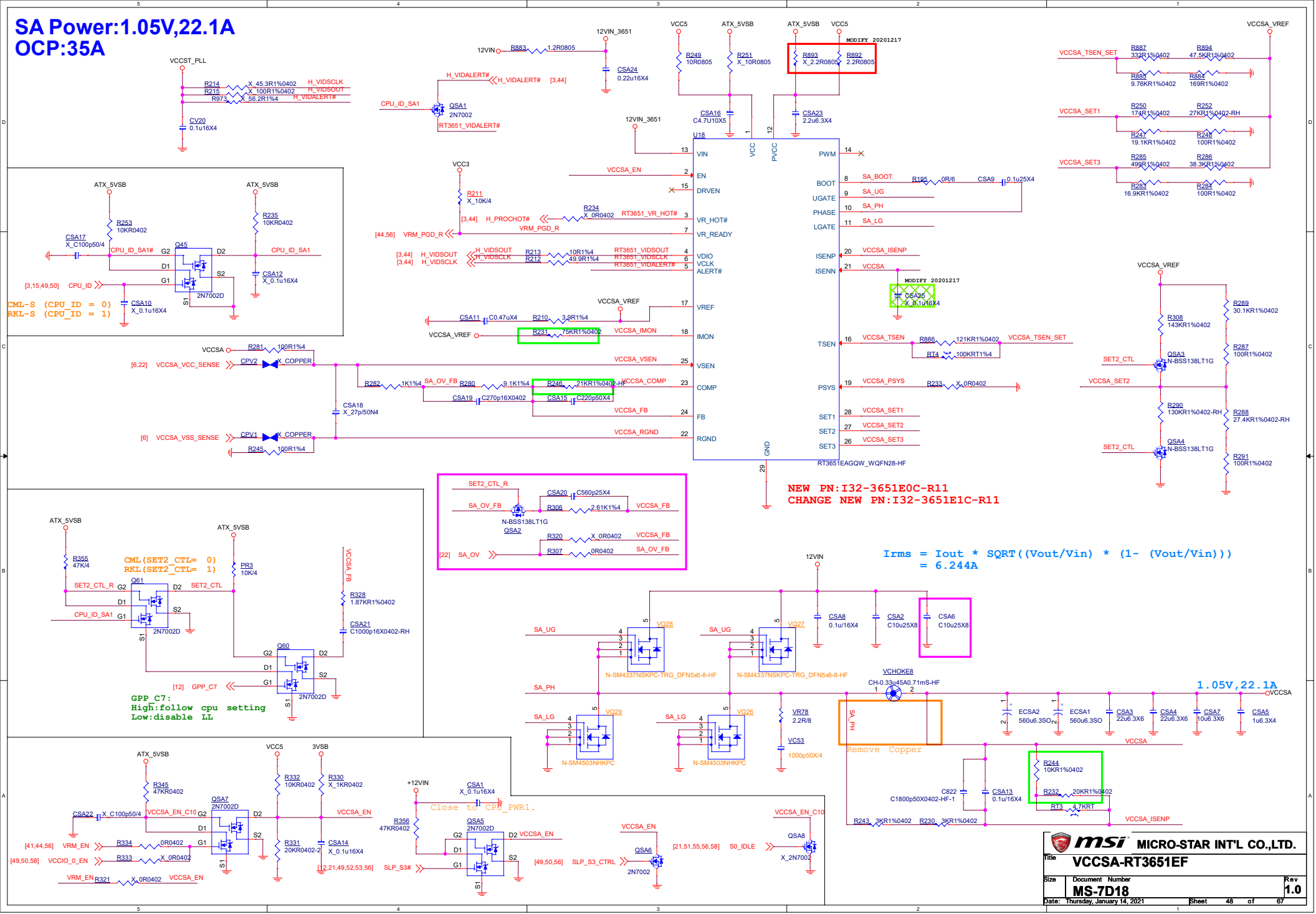
Date: Wednesday, January 13, 2021 Sheet 46 of 67



MICRO-STAR INT'L CO.,LTD.

Title	VGT MOS-PHASE 1~2	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 47 of 67	

SA Power:1.05V,22.1A
OCP:35A



MSI MICRO-STAR INT'L CO.,LTD.

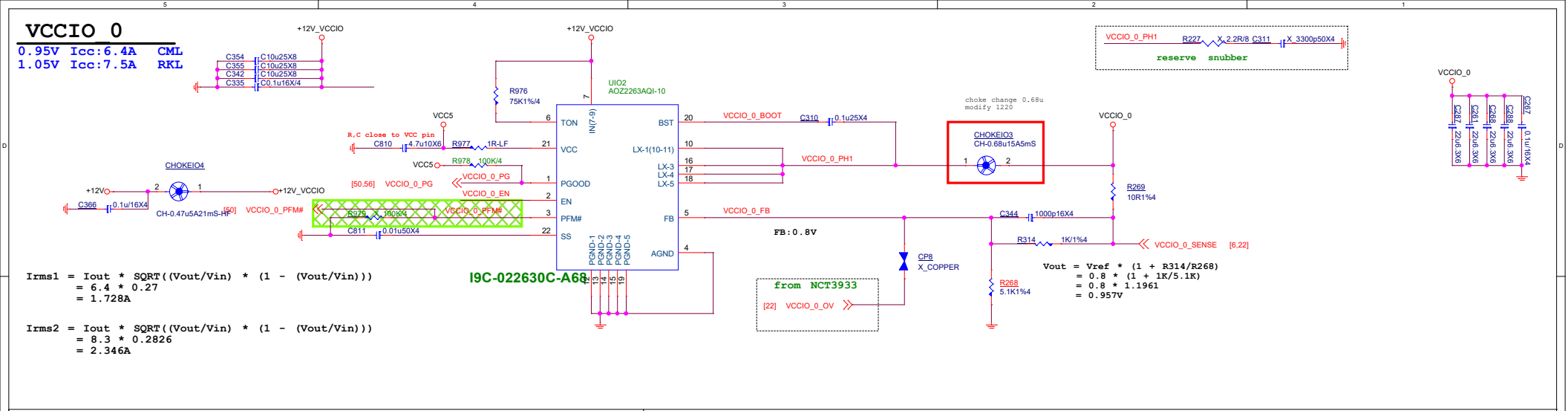
Title: VCCSA-RT3651EF

Size: | Document Number: MS-7D18 | Rev: 1.0

Date: Thursday, January 14, 2021 | Sheet 48 of 67

VCCIO_0

0.95V Icc:6.4A CML
1.05V Icc:7.5A RKL

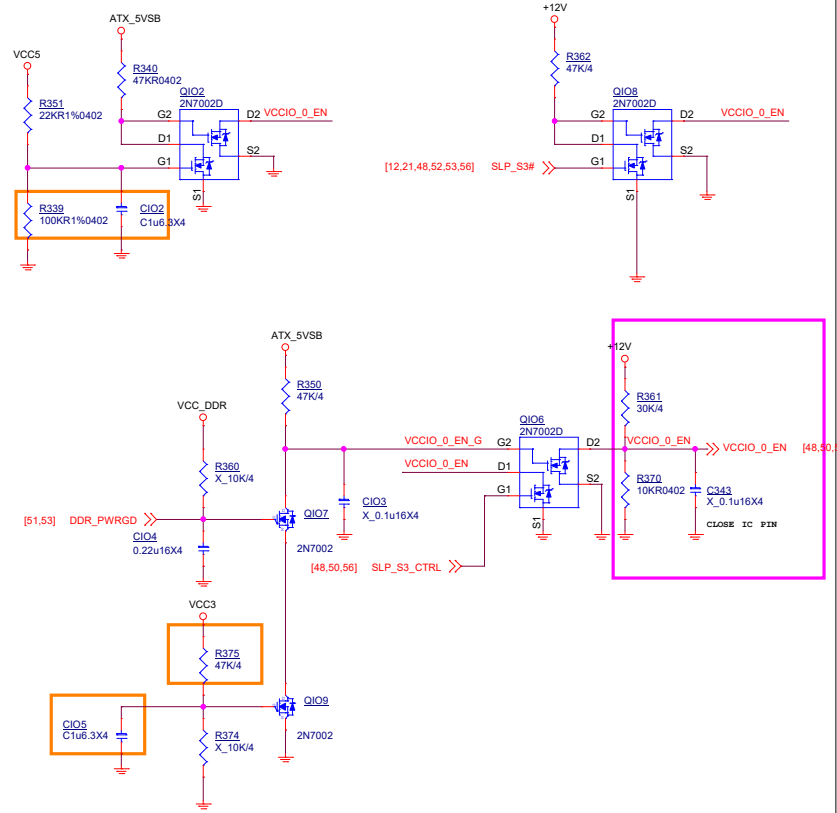


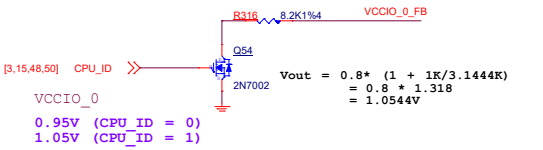
I9C-022630C-A68

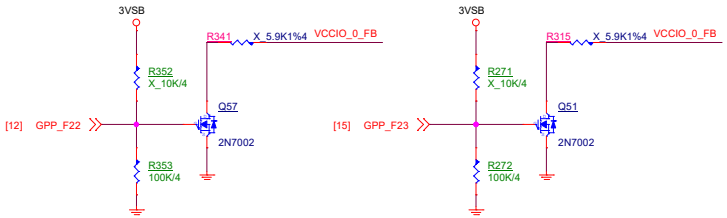
Irms1 = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 6.4 * 0.27
= 1.728A

Irms2 = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 8.3 * 0.2826
= 2.346A

Vout = Vref * (1 + R314/R268)
= 0.8 * (1 + 1K/5.1K)
= 0.8 * 1.1961
= 0.957V







information from PDG page686

GPP_F22	GPP_F23	CPU_ID	VCCIO_0
Low	Low	Low	0.95V
Low	Low	High	1.05V
High	Low	High	1.075V
Low	High	High	1.100V
High	High	High	1.125V

MICRO-STAR INT'L CO.,LTD.

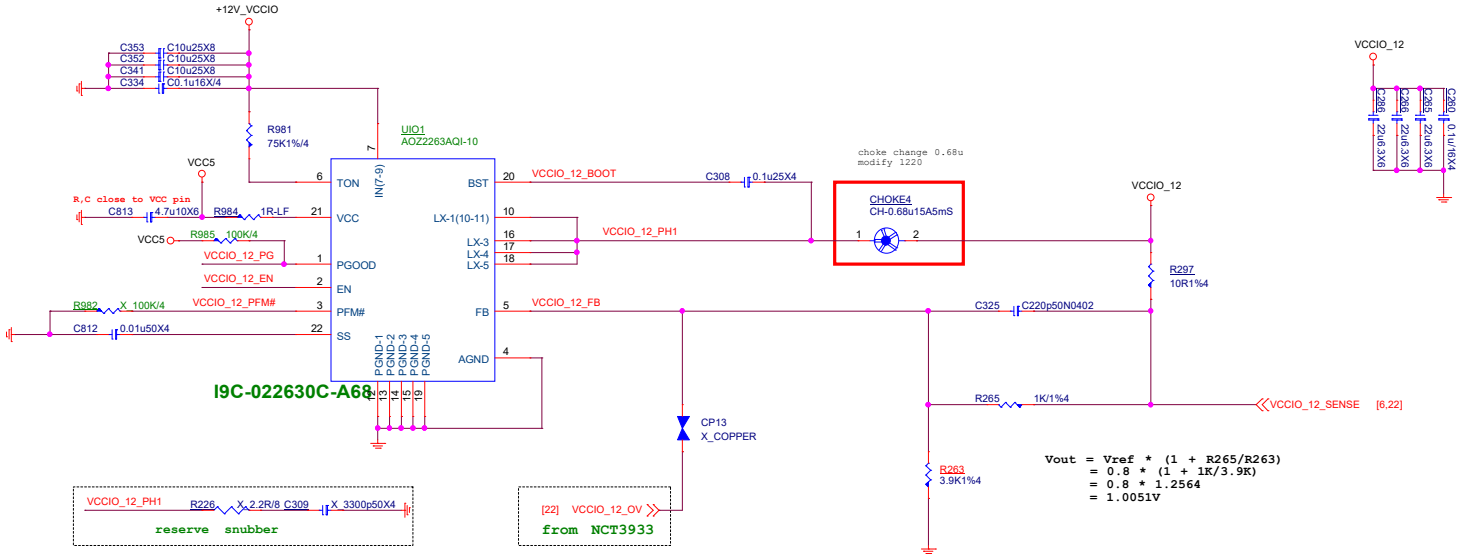
Title: VCCIO_0-AOZ2263AQI

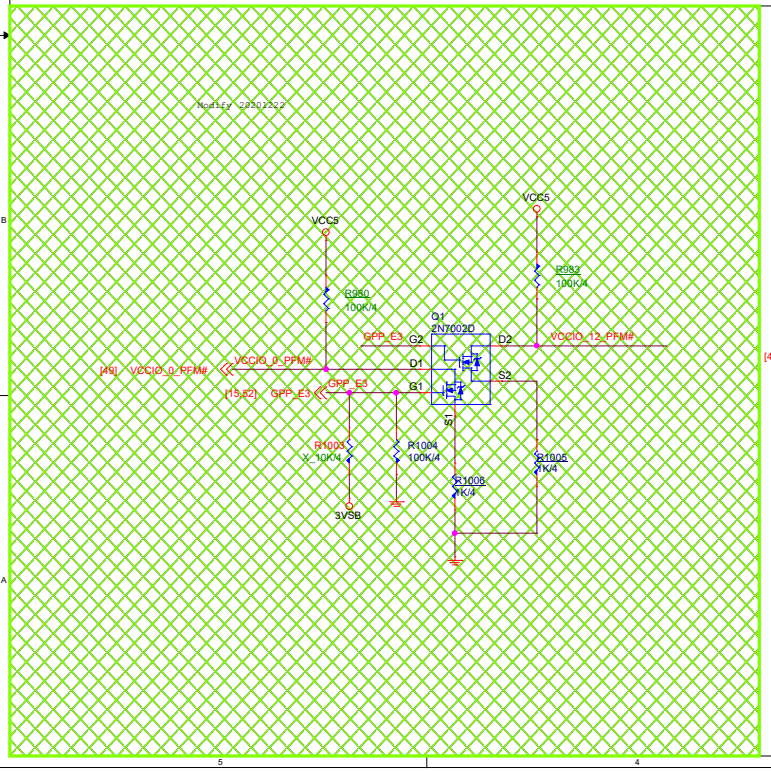
Size: | Document Number: MS-7D18 | Rev: 1.0

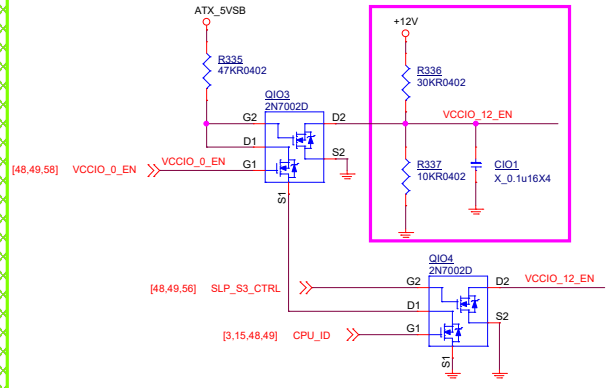
Date: Wednesday, January 13, 2021 | Sheet 49 of 67

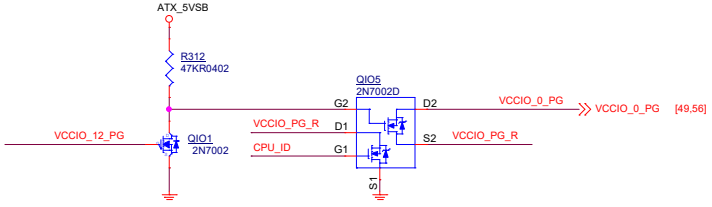
VCCIO_12

1.0V Icc:9.6A RKL









MICRO-STAR INT'L CO.,LTD.

Title: VCCIO_12-AOZ2263AQI

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 50 of 67

DDR4 Power:1.2V,14.15A

4.3A For CPU

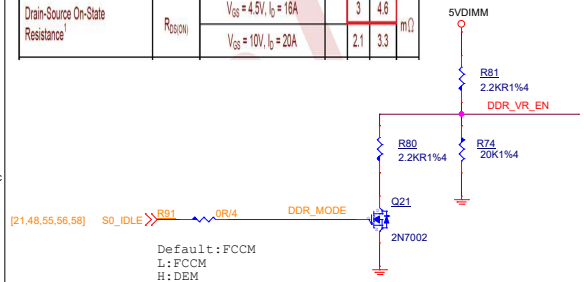
9.1A For 4DIMM

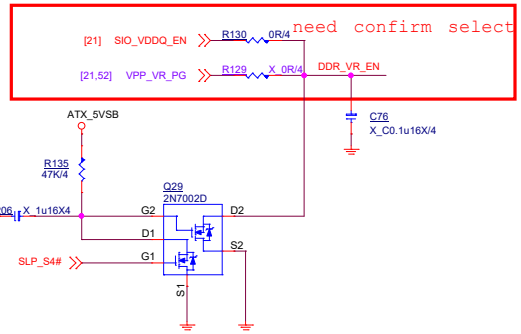
0.75A For VTT_DDR

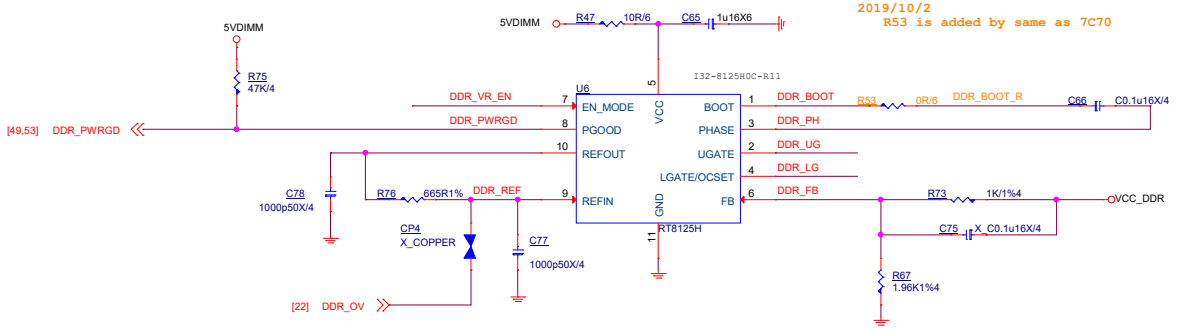
Iout = 4.3+9.1+0.75=14.15A

Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/4.6m
=15.913A
Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/3m
=24.4A

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 16A		3	4.6	mΩ
		V_{GS} = 10V, I_D = 20A		2.1	3.3	







2019/10/2
R53 is added by same as 7C70

$$V_{OUT} = \left[V_{REFOUT} \times \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \right] + \frac{\Delta V_{OUT}}{2}$$

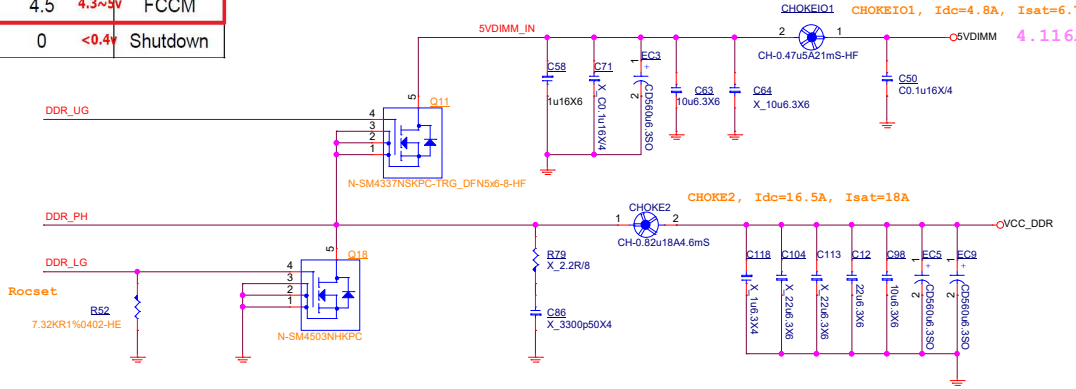
Vout=Vrefout*(1+R1/R2)
=0.794x(1+1/1.96)
=1.1991v

Table 1. States of EN_MODE Control Circuit

Q1	Q2	V_{EN_MODE} (V)	Mode
ON	OFF	2.37 2.1~2.7v	DEM
OFF	OFF	4.5 4.3~5v	FCCM
OFF	ON	0 <0.4v	Shutdown

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 14.15 * SQRT(0.1824)
= 6.043A



$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.2*13.67) * (1.2/5)
= 1.1119uH

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.4*13.67) * (1.2/5)
= 0.55596uH

So L range = 0.55596uH ~ 1.1119uH

£GIL=(Vin-Vout)/(L*Fsw) * Vout/Vin
=(5-1.2)/(0.82u*300K)*(1.2/5)
=3.7073A

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

Rocset = [(1.3* Iout) - (0.5 * £GIL)]*Rds(on)/
Iocset
= [(1.3*13.67) -(0.5*3.7073)]* 3m / 10u
= 4.7752Kohm
Rocset = [(1.3*Iout) - (0.5 * £GIL)]*Rds(on)/
Iocset
= ((1.3*13.67) - (0.5*3.7073)]* 4.6m / 10u
= 7.3219Kohm

2019/9/27
Q11 is changed to N-PK806BA and Q18 is changed to N-PK810BA by Ivy's comment

2019/12/17
Q11 is changed to SM4337NSKPC-TRG and Q18 is changed to SM4503NHKPC-TRG by Ivy's comment

MICRO-STAR INT'L CO.,LTD.

Title: DDR PWR - RT8125H

Size | Document Number: MS-7D18 | Rev: 1.0

Date: Wednesday, January 13, 2021 | Sheet 51 of 67

VPP2.5V Power:2.5V,6A(for dimm LED)

IC OCP:7.6A(6.6A~8.6A)

$$F_{SW}(kHz) = \frac{V_{OUT}(V)}{V_{IN}(V) \times T_{ON}(nS)} \times 10^6$$

3.75A

Ton=Vout/(Vin*Fsw)
=1000ns

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 6 * 0.5
= 3A

L04-01074U0-T15

2020/09/21
R161 ischange form 180Kohm to 220Kohm
R175 is added with 1.5ohm;
by vendor's suggstion

FB:0.8V

Vout = Vref * (1 + R4497/R4499)
= 0.8 * (1 + 1K/0.47K)
= 0.8 * 3.1277
= 2.50216V

EN:off threshold 0.5V
on threshold 1.6V

need confirm select

reserve snubber

from NCT3933

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

VREF Shutdown Mode						
Shutdown Threshold	V_{IH}	Enable	0.4			V
	V_{IL}	Disable			0.15	

Recommended Operating Conditions

ITEM	SYMBOL	MIN	MAX	UNITS
Input Voltage	VIN	1.0	5.5	V
	VCNTL	3.0	5.5	
	EN1 & EN2	0	3.3	
	VREF	0.5	3.3	V

NCT3103S co-lay NCT3102S/UP0109

0.75A

0.3*4=1.2A

R105/R106 change to 1K

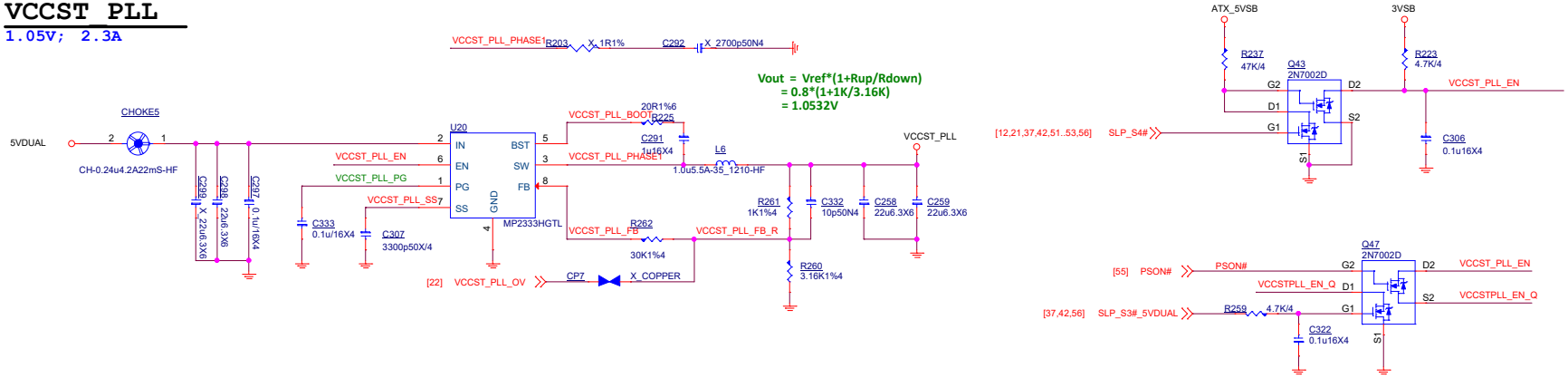
from NCT3933

Title	DDR PWR VPP25/VTT
Size	Document Number: MS-7D18
Rev	1.0
Date:	Wednesday, January 13, 2021
Sheet	52 of 67

MICRO-STAR INT'L CO.,LTD.

VCCST PLL

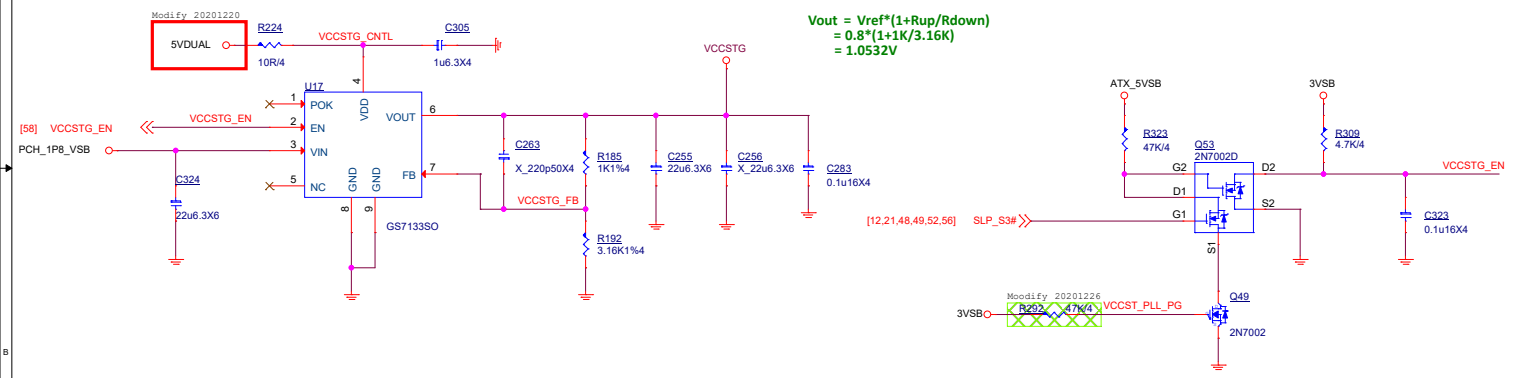
1.05V; 2.3A



VCCSTG

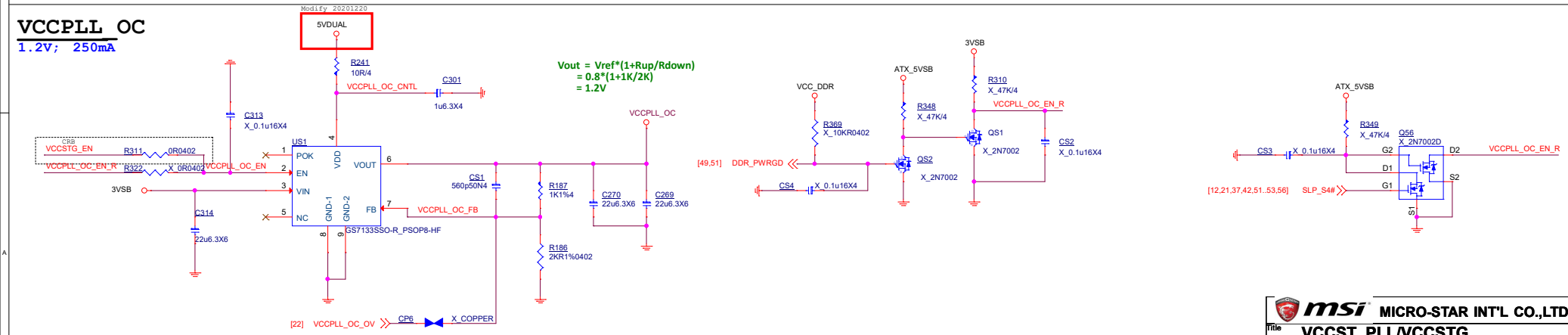
1.05V; 0.9A

Power Loss1=(Vin-Vout)*Iout
=(1.8-1.05)*0.95
=0.75*0.95
=0.7125W



VCCPLL_OC

1.2V; 250mA



MICRO-STAR INT'L CO.,LTD.

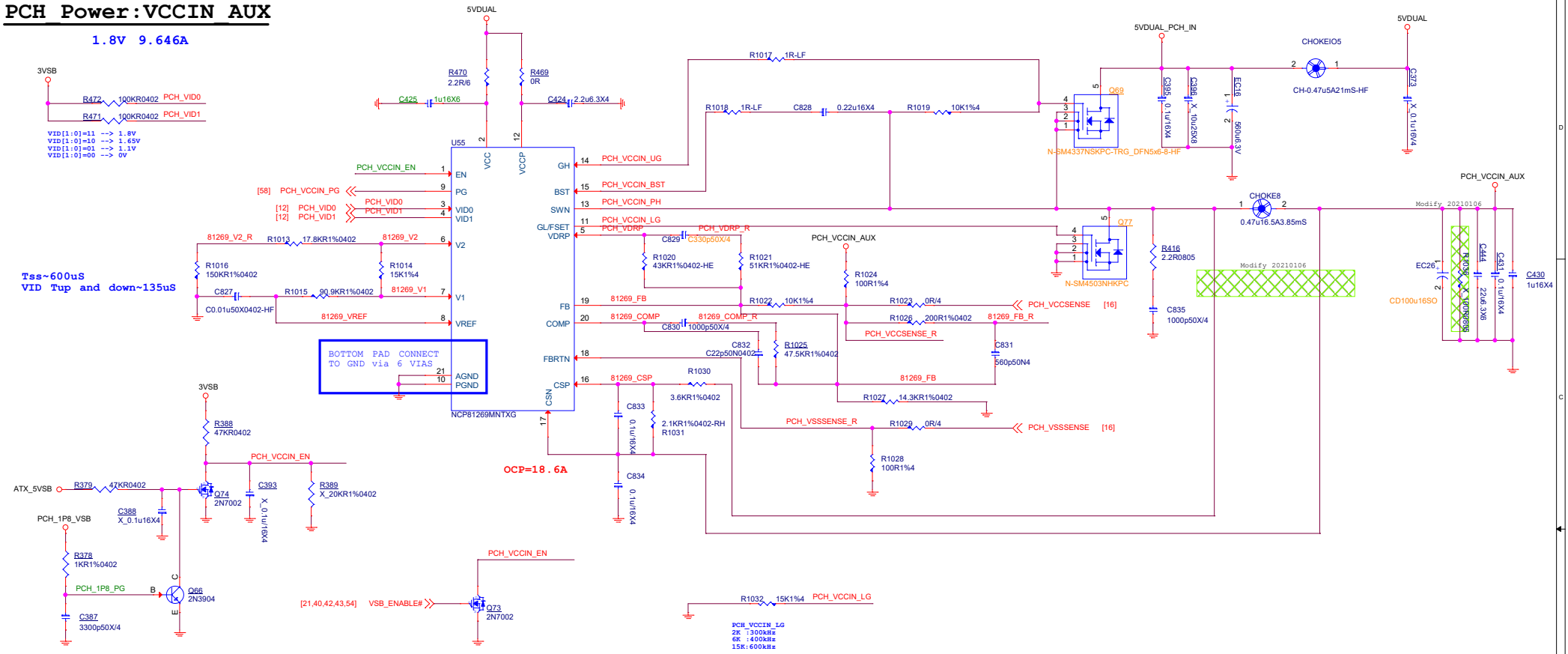
Title: VCCST_PLL/VCCSTG

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 53 of 67

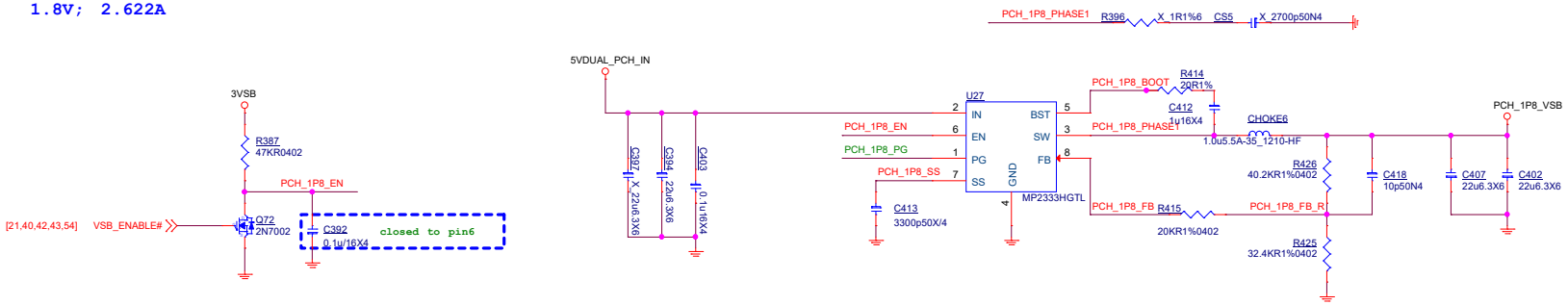
PCH_Power:VCCIN_AUX

1.8V 9.646A



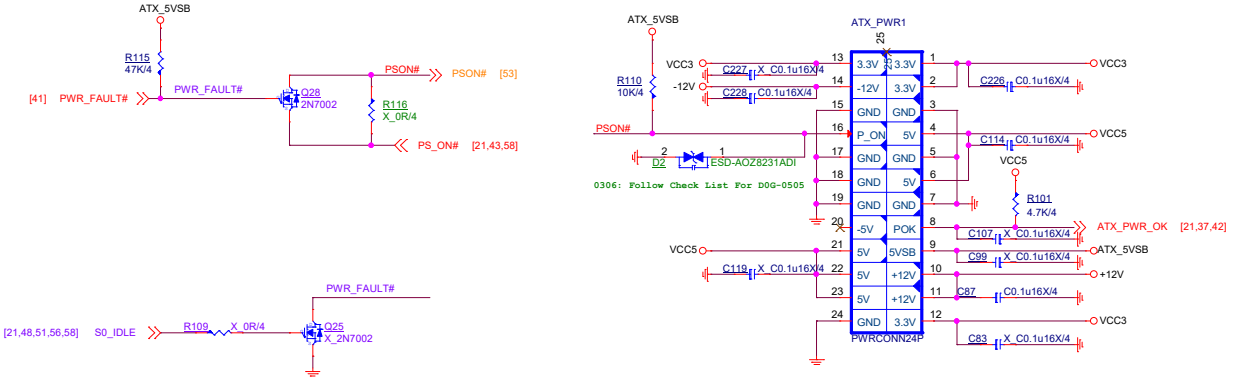
PCH_1P8_VSB

1.8V; 2.622A

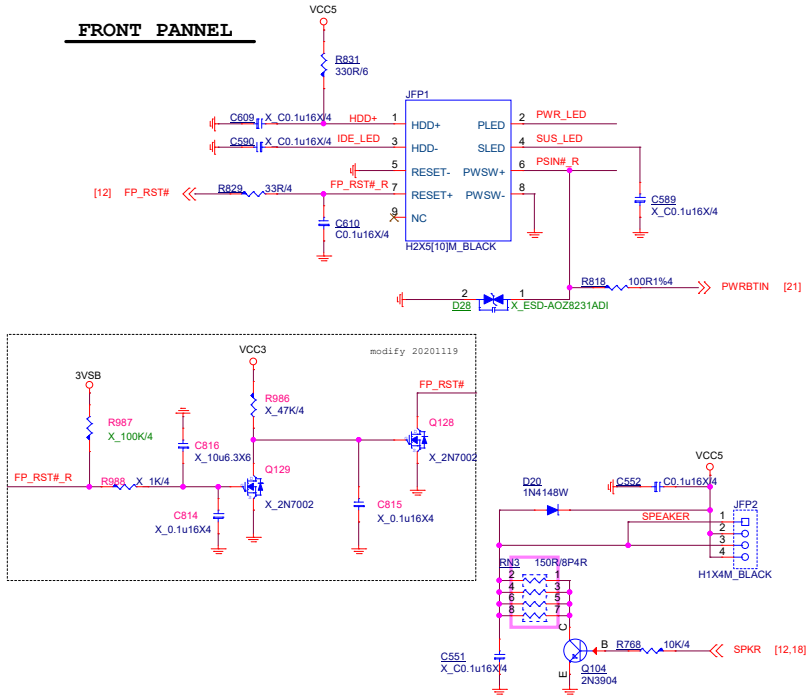


MSI MICRO-STAR INT'L CO.,LTD.			
Title: PCH Power - RT8125H			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Thursday, January 14, 2021	Sheet 54 of 67		

ATX POWER CONNECTOR



FRONT PANNEL



Thunderbolt card support

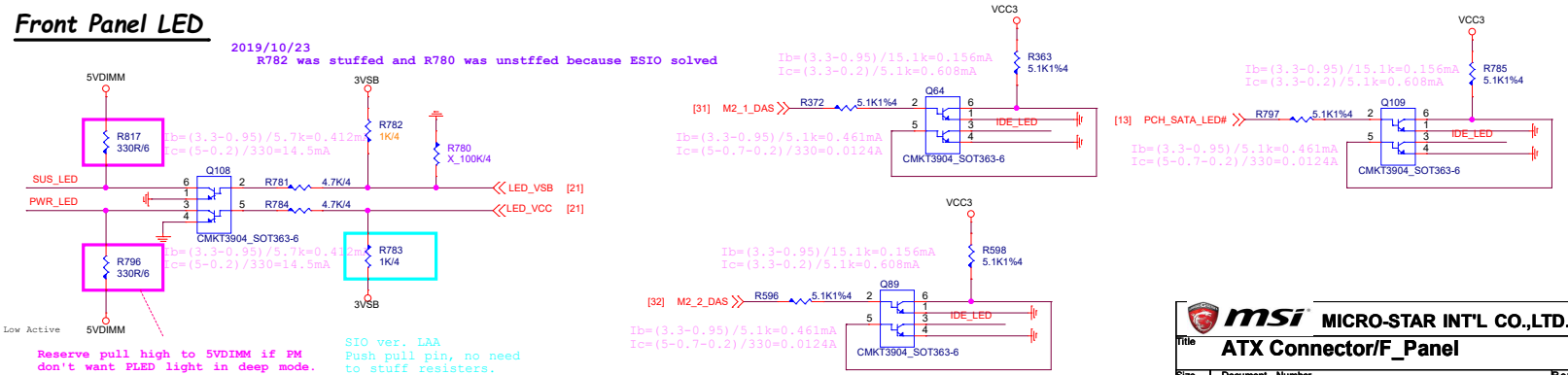
CRB use GPP_H15
need confirm

default use PCIE Slot Wake#

CRB use GPP_F2

Front Panel LED

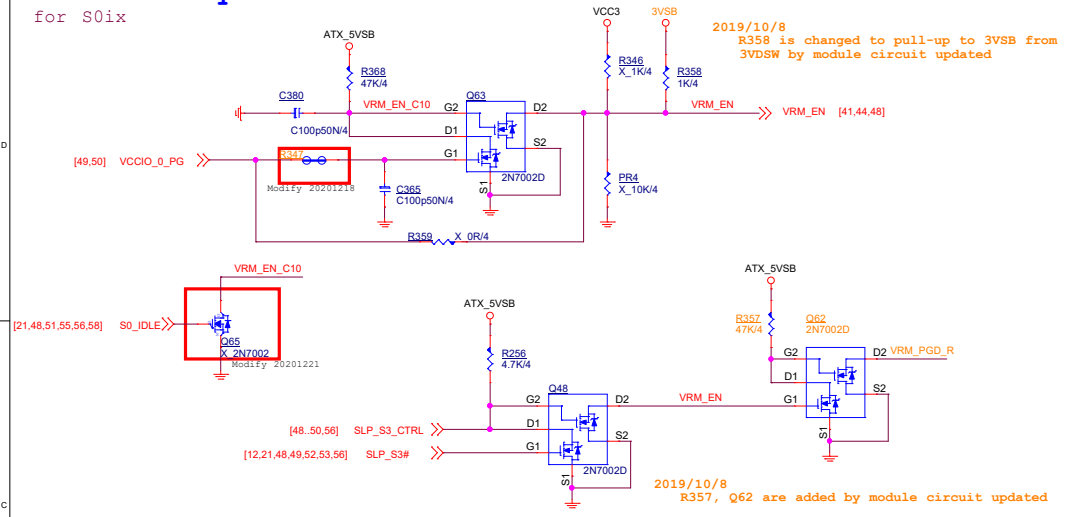
2019/10/23
R782 was stuffed and R780 was unstffed because ESIO solved



MICRO-STAR INT'L CO.,LTD.			
Title: ATX Connector/F_Panel			
Size	Document Number: MS-7D18		Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 55 of 67		

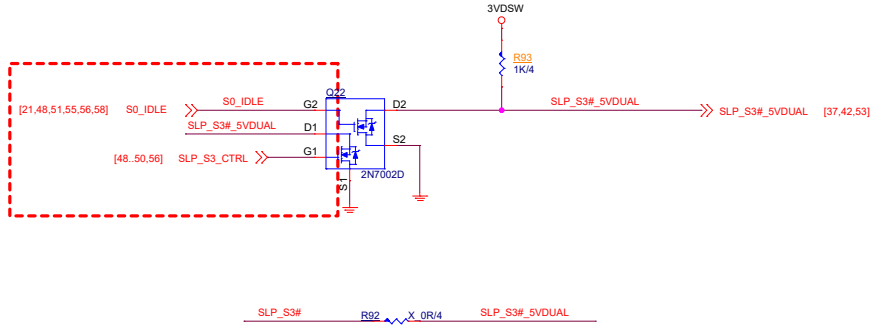
PWR-VRM-Seqence

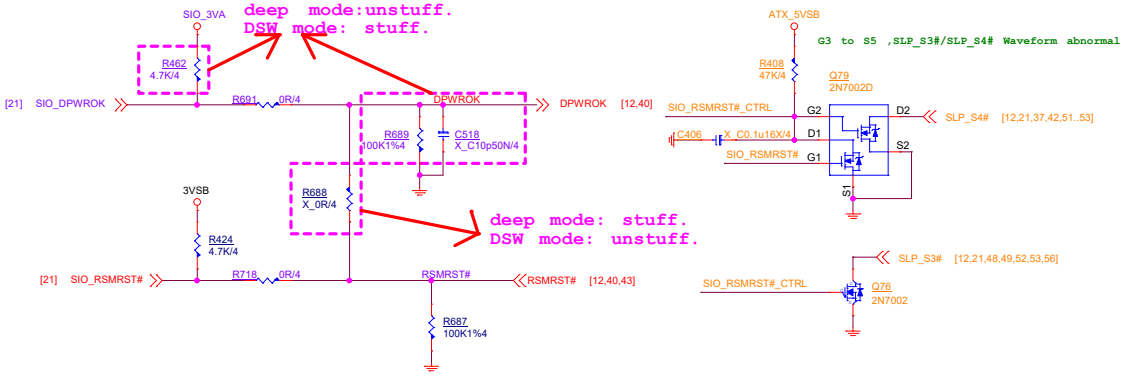
for S0ix



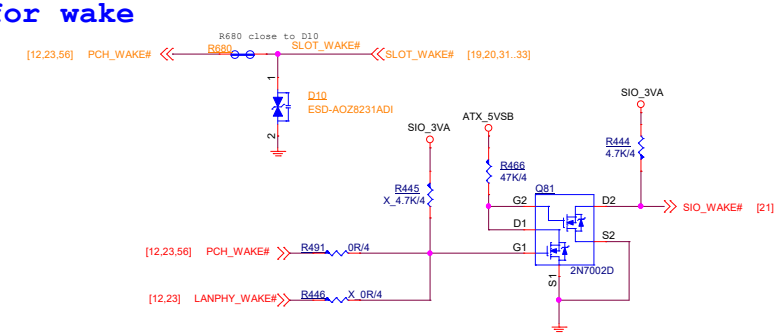
for 5VDIMM and 5VDUAL

for S0ix

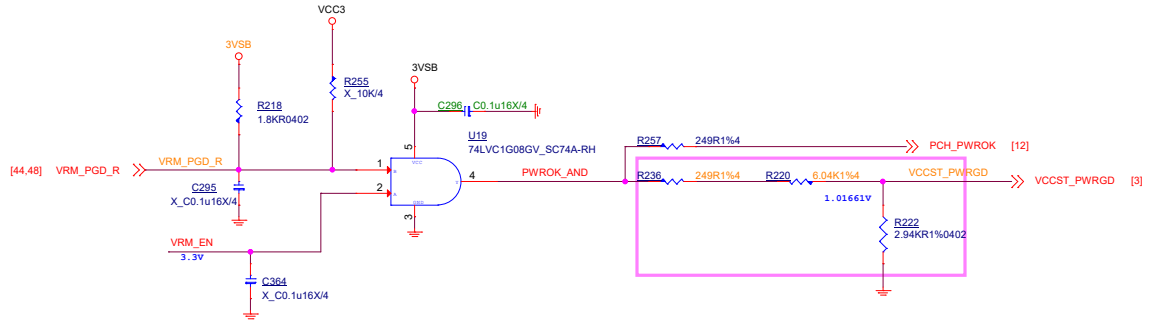


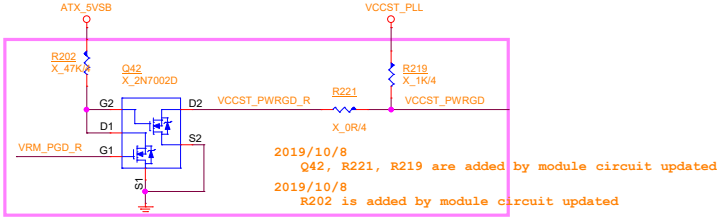


for wake



PCH_PWROK/VCCST_PWRGD





MICRO-STAR INT'L CO.,LTD.

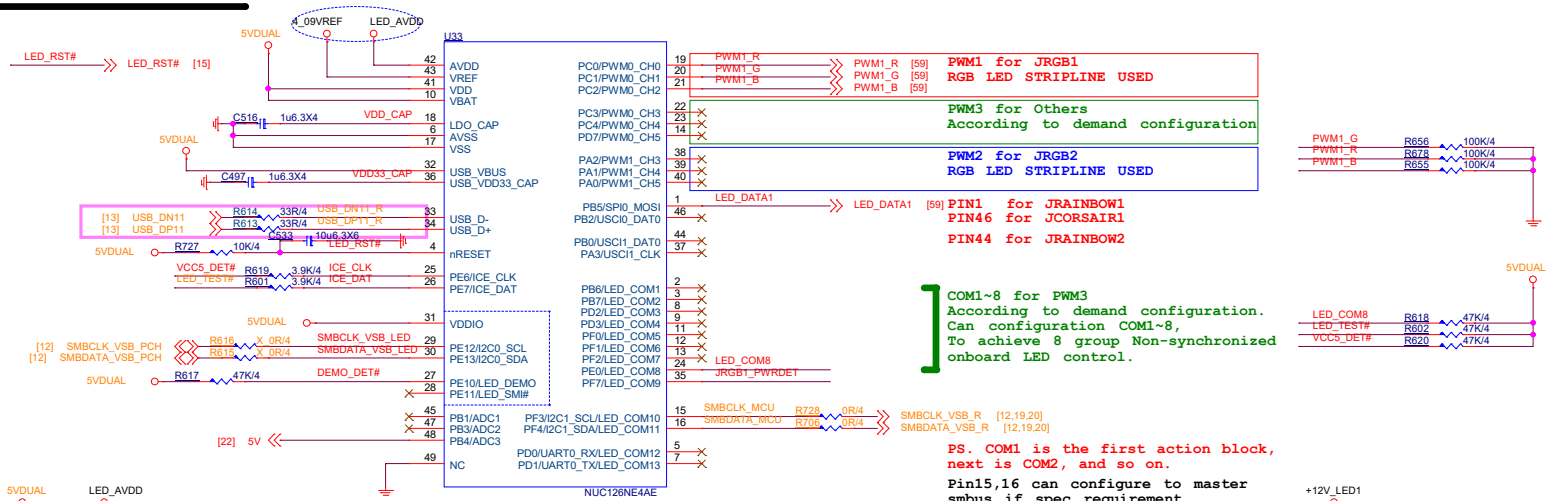
Title: POWER SEQUENCE

Size	Document Number	Rev
	MS-7D18	1.0

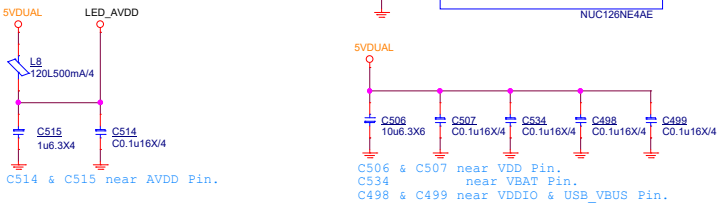
Date: Wednesday, January 13, 2021 Sheet 56 of 67

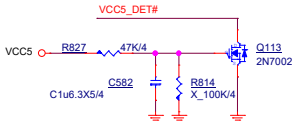
48 PIN LED MCU

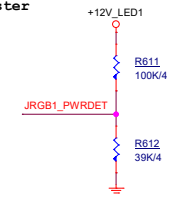
If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.



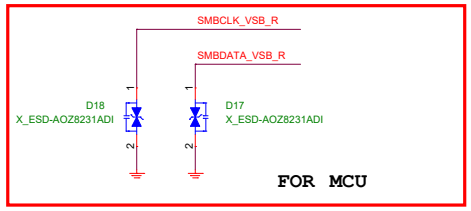
Control	Net Name	PWM USE
PCH	LED_DATA4	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_DATA1	No Use
JRAINBOW2	LED_DATA3	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	No Use
Board Side LED	COM 9~12	No Use







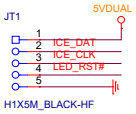
SMBus ESD



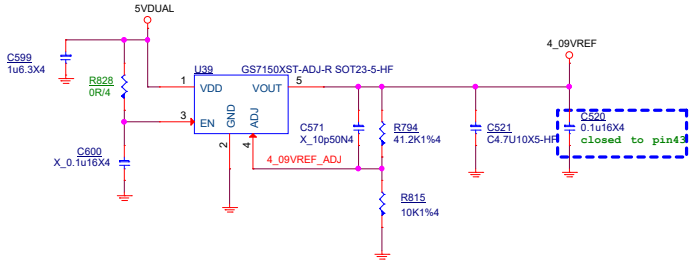
IF no JPWRLED1 & JPIPE_LED spec

MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JT1 for FW update

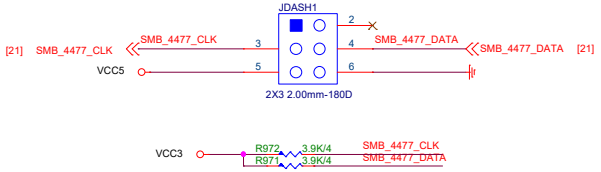


MCU Voltage Monitor



JDASH1

NEW PN:N31-2031431-H06



MICRO-STAR INT'L CO.,LTD.

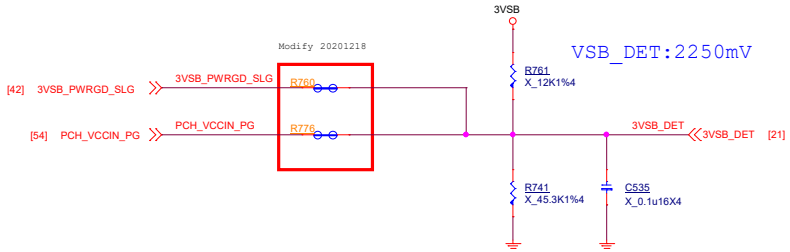
Title: LED MCU Control

Size	Document Number	Rev
	MS-7D18	1.0

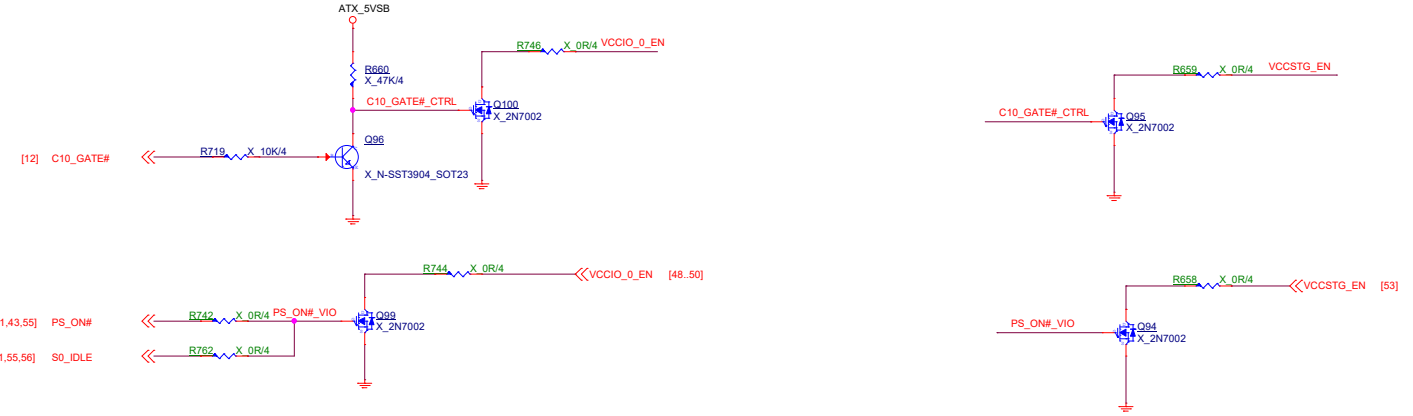
Date: Wednesday, January 13, 2021 Sheet 57 of 67

FOR RSMRST#/DPWROK/SLP_SUS# INTEL seqence request

Remove silego
500s update 1105



S0IX: VCCIO/VCCSTG OFF



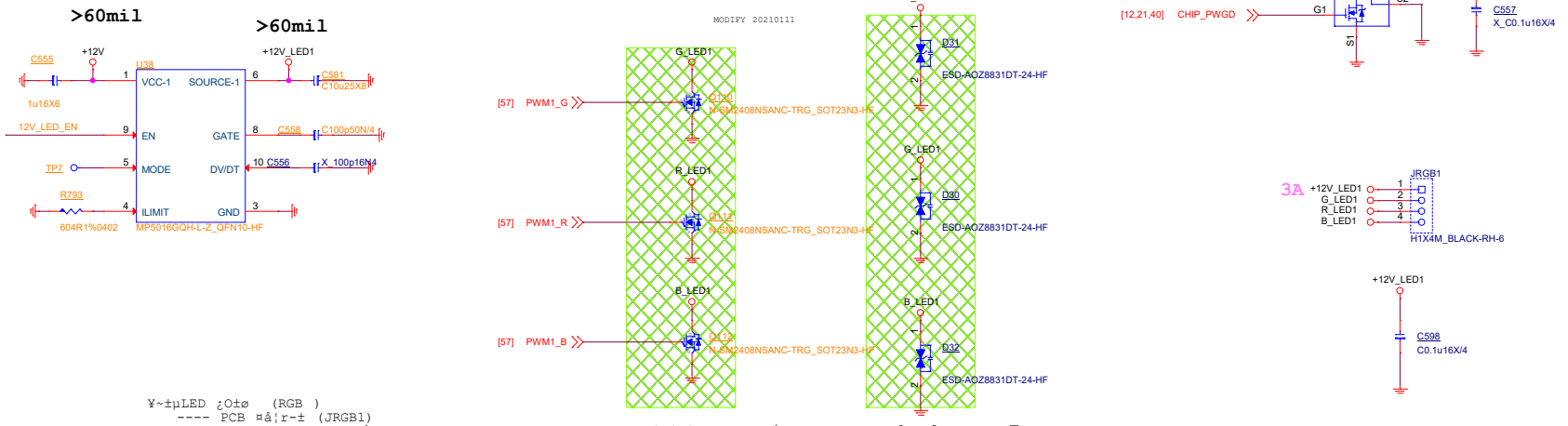
MICRO-STAR INT'L CO.,LTD.

Title: SILEGO Sequence

Size	Document Number	Rev
	MS-7D18	1.0

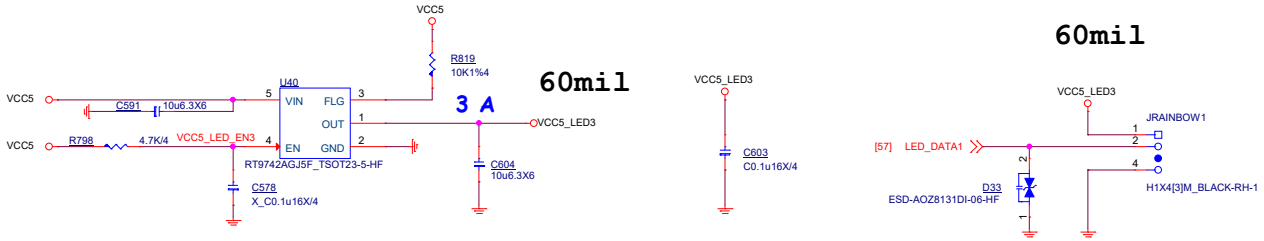
Date: Wednesday, January 13, 2021 Sheet 58 of 67

JRGB1



¥~‡µLED ¿O‡ø (RGB)
---- PCB ¤å¦r-‡ (JRGB1)
---- ¤â¥U µù©ú RGB ‡µÀY¤ä´©¼Ð·Ç 5050 RGB LED ¿O‡ø (12V/G/R/B) , ¿O‡øÁ`¿é¥X¹q¬y--¨î¬°3¦w°ö (12 ¥ñ¯S) , ªø«×--¨î¬°2¤½¤Ø

JRAINBOW1

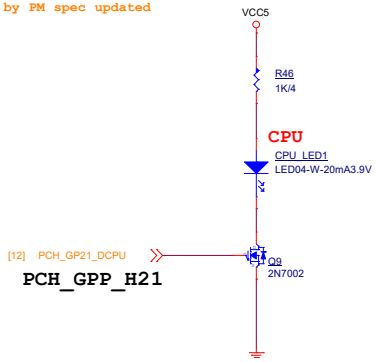


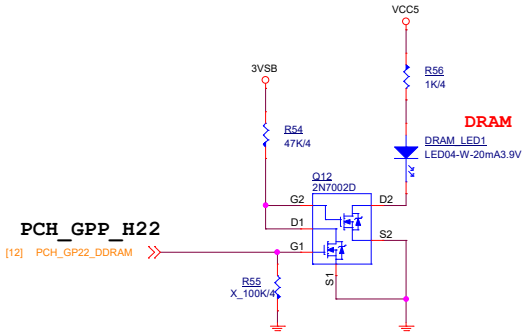
MICRO-STAR INT'L CO.,LTD.		
Title: LED PIN HEADER		
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 59 of 67	

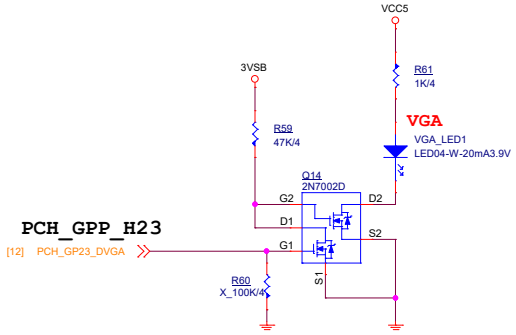
EZ DEBUG LED

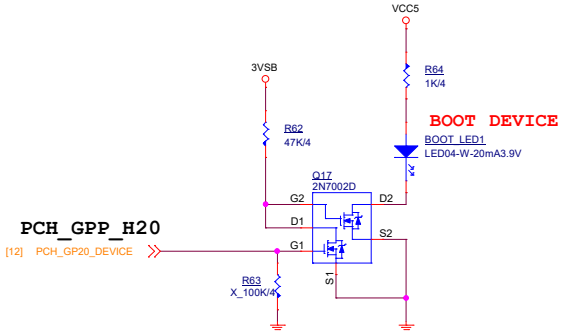
2019/10/3
This page is added by PM spec updated

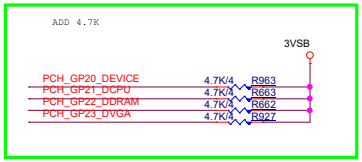
C:D0C-040P100-H91
D:D0C-040V800-H91
V:D0C-040T200-H91
B:D0C-040V700-H91











LED
¬õ : D0C-040P100-H91
AVL: D0C-040S500-E07

LED
¥Õ : D0C-040T200-H91
AVL: D0C-040S200-E07

GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
«G	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
·À	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

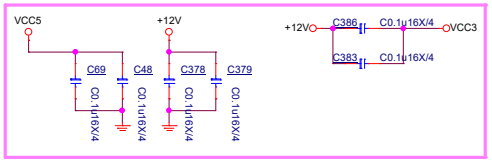
ÃÖ¾÷Â ¹qª¬°A¤U¡A4-ÓLED¥ý°û«ùdefault¥þ·t¡A¶}¾÷³q¹q«á¡G
1.-°¥ý¶i¦æCPU checkCPU LED «G¡Acheck PASS«á«hCPU LED·À±¼¡C
2.±µµÜ¨ì§Ç¶i¦æMemory /memory LED«Gcheck PASS«á«hmemory LED·À±¼¡C
3.VGAª°check/VGA LED«G¡Acheck PASS«á«hVGA LED·À±¼¡C
4. BOOT DEVICEª°check/BOOT LED«G¡Acheck PASS«á«hBOOT LED·À±¼¡C
5. ¦]¦¹³Ì«á¥¿±`¶¶§Q¶}¾÷«á¡A¥|-ÓLED¿O³£¬O·À±¼ª°¡C
¡]¨t²Î-«±Ò©Î¨ä¥L-ì¦]³y¦¨¨t²Î-«¶}¾÷¡A«hLED¤´«ö¤W-z¦æ¬°°ÊŞ@¡^

21ci203T

msi MICRO-STAR INT'L CO.,LTD.

Title	EZ DEBUG LED	
Size	Document Number MS-7D18	Rev 1.0
Date: Wednesday, January 13, 2021	Sheet 60 of 67	

Return path cap



21ci203T

MICRO-STAR INT'L CO.,LTD.

Title	EMI CAP	
Size	Document Number: MS-7D18	Rev: 1.0
Date: Wednesday, January 13, 2021	Sheet 61 of 67	

CPU_H1

CPU
ÅK®y

AZIF0208-P001C

Optical Fiducial Marks-120

FM2 FM1 FM5 FM8

X_FM X_FM X_FM X_FM

FM3 FM4 FM6 FM7

X_FM X_FM X_FM X_FM

PCH-HS1

PCH
H/S

HS-0409430

MOS-N-HS1

MOS
H/S

8554-65900-00A

MOS-W-HS1

MOS
H/S

8554-65901-00A

Mounting Holes

MH1 MH3 MH7

MH2 MH6 MH4

MH5 MH8

X_MH001

2020/07/22
ivyhsiao mail

C389
X_C100p50N/4

Audio layout guide

BAT1_X1

BAT-BCR2032P-RH

BIOS_LA1

AMI

OK

AMI

HDMI_LA1

HDMI_LABEL

LABLE3

CFOS
LABLE

CFOS_LABLE

Simulation

SIM2 SIM1 SIM3

SIM2 SIM1 SIM3

X_PIN1*2 X_PIN1*2 X_PIN1*2

MOS Heatsink Holes

HS_H4 HS_H3 HS_H1 HS_H2

X_FM X_FM X_FM X_FM

PCB FOOTPRINT H_R162D120_BR182_EMI
2020/07/30 PETER MAIL

1.0

MK_LA1

B560M PRO-VDH WIFI

PCB1

7D18-0A

21ci203T

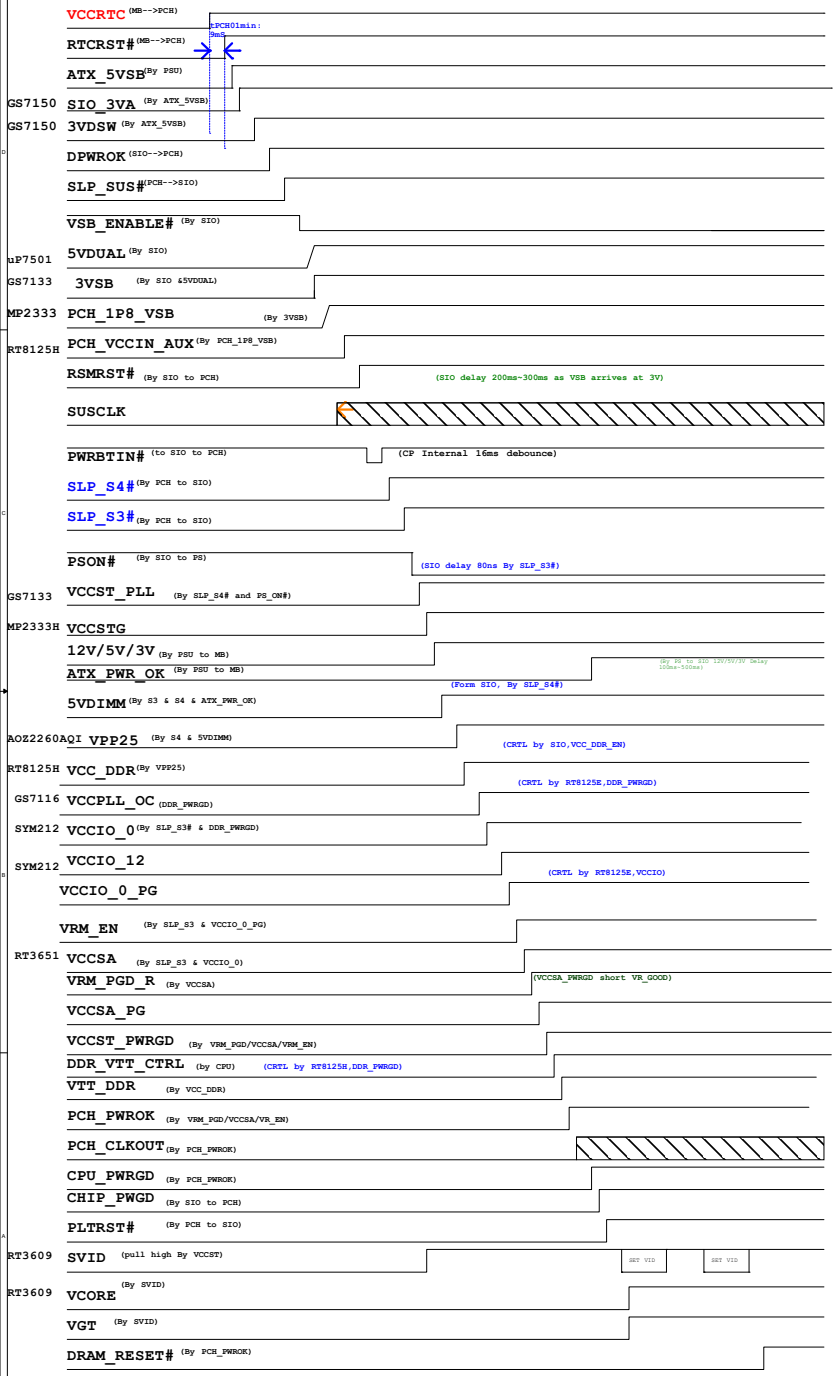
MICRO-STAR INT'L CO.,LTD.

Title: Manual Parts

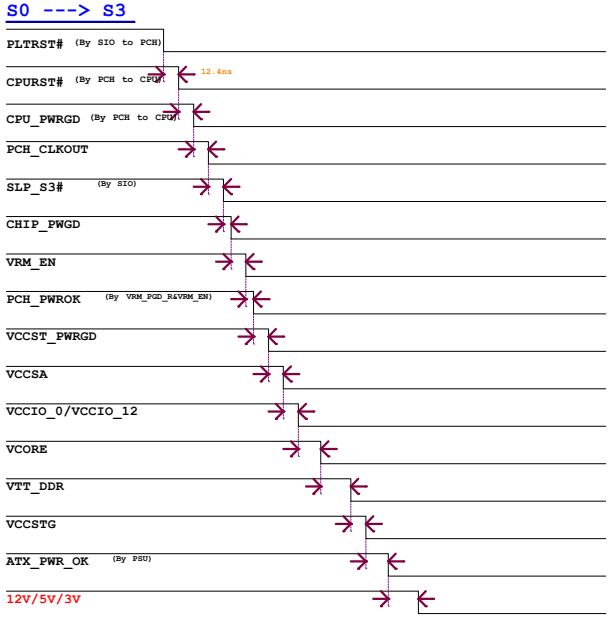
Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 62 of 67

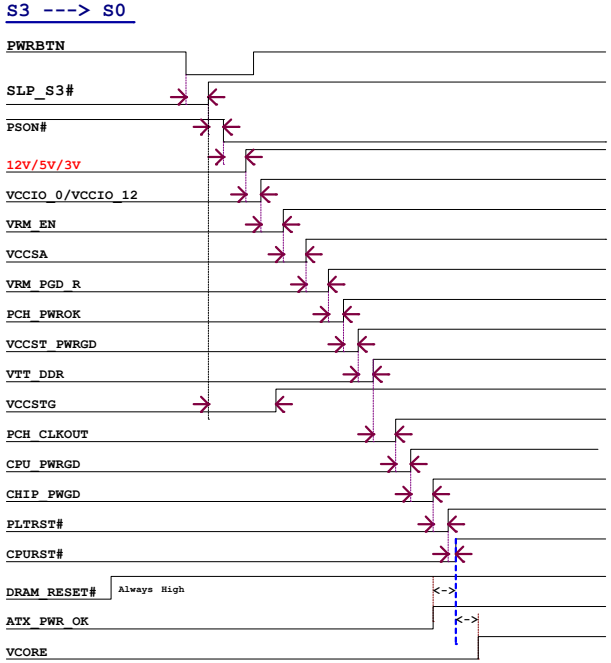
(G3)DS5 ---> S0



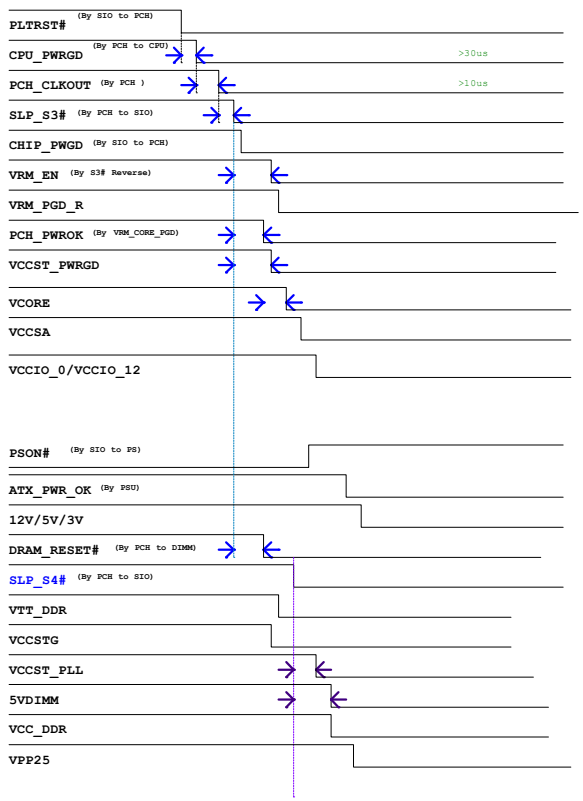
S0 ---> S3



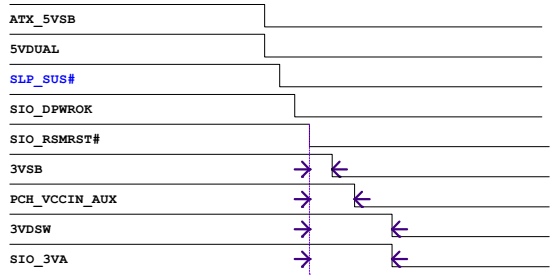
S3 ---> S0



S0 --> S5



S5 --> G3



MICRO-STAR INT'L CO.,LTD.

Title: Power Sequence

Size	Document Number	Rev
	MS-7D18	1.0

Date: Wednesday, January 13, 2021 Sheet 65 of 67