MS-7882

ATX

Ver: 1.0

Haswell-E Platform

CPU:

Haswell-E

System Chipset:

Wellsburg

Onboard Chip:

HD Audio Codec: ALC1150

LAN-Killer LAN

SIO:NTC6792D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

*DDRIV (1666MHz) * 8 (Dual Channel)*

ACPI:

ISL6388

PWM:

VRD12.5 -ISL6388

Expansion Slots:

PCI Express (X16) Slot1
PCI Express (X8) Slot2
PCI Express (X8) Slot3
PCI Express (X16) Slot4
PCI Express (X8) Slot5

Other:

*SATA3.0 *8*
*USB2.0 *8*
*USB3.1 *1*
*REAL USB3.0 *6*
*FRONT USB2.0 *4*
*FRONT USB3.0 *4*

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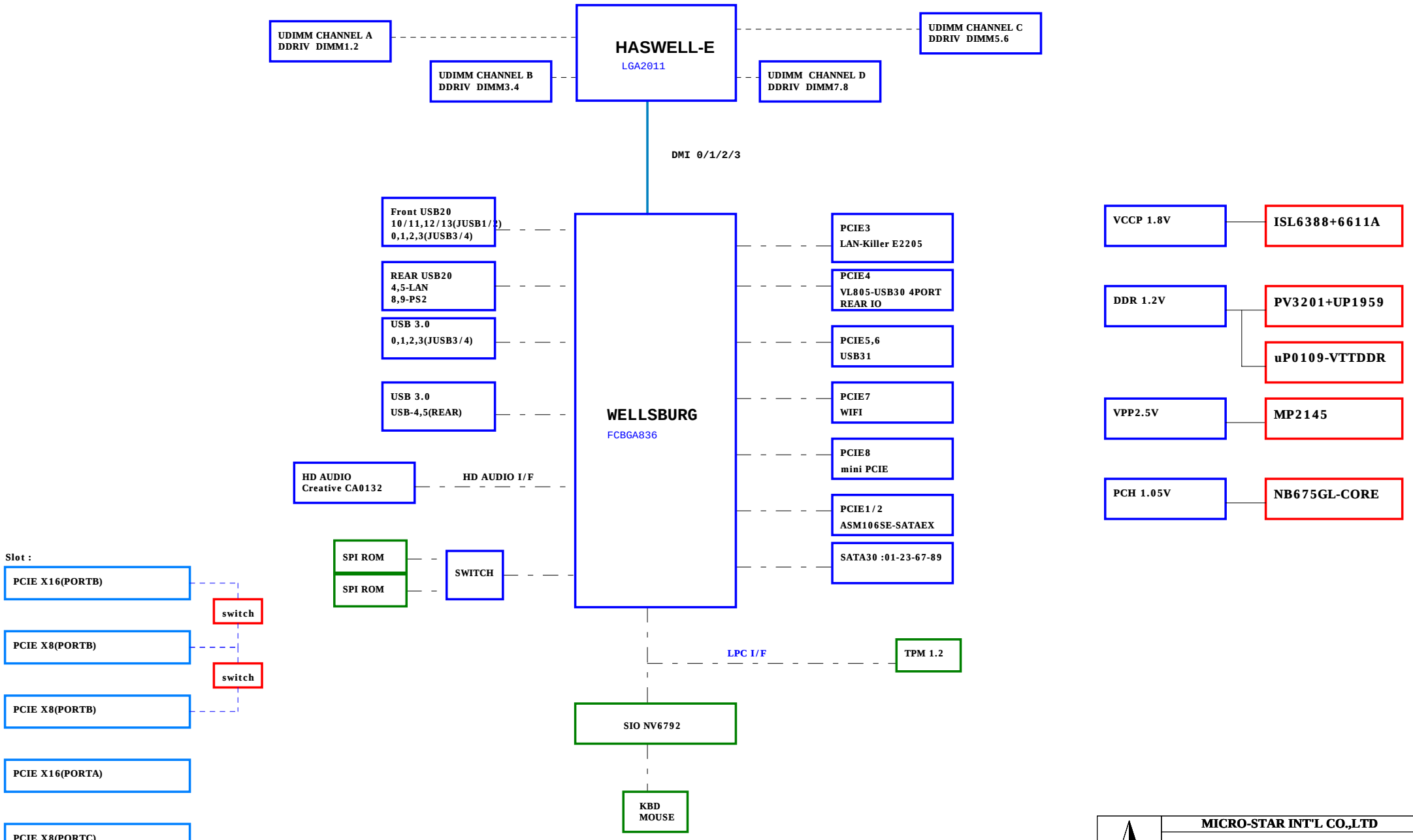
MS-7882 Block Diagram



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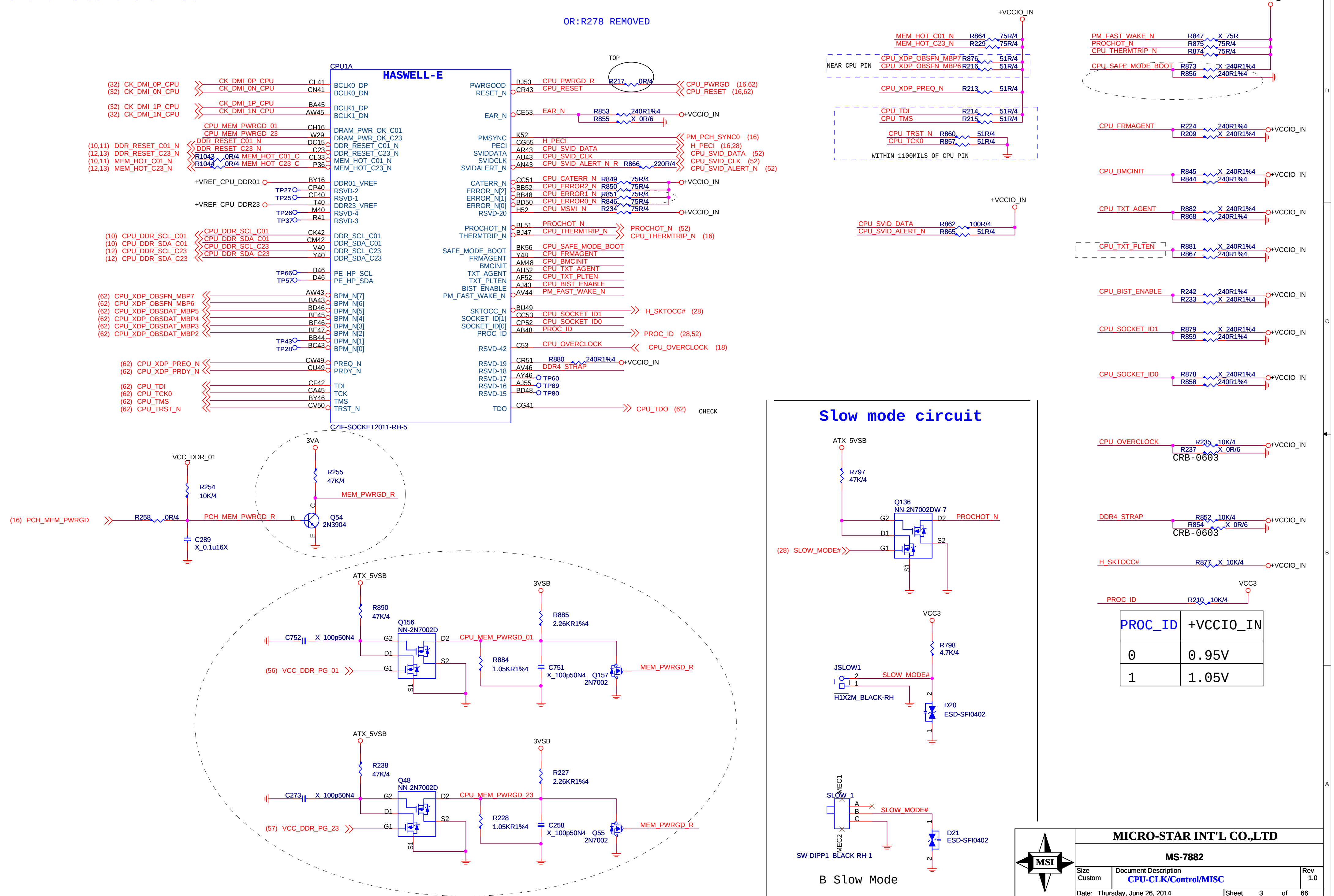
CPU-CLK/Control/MISC



PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V

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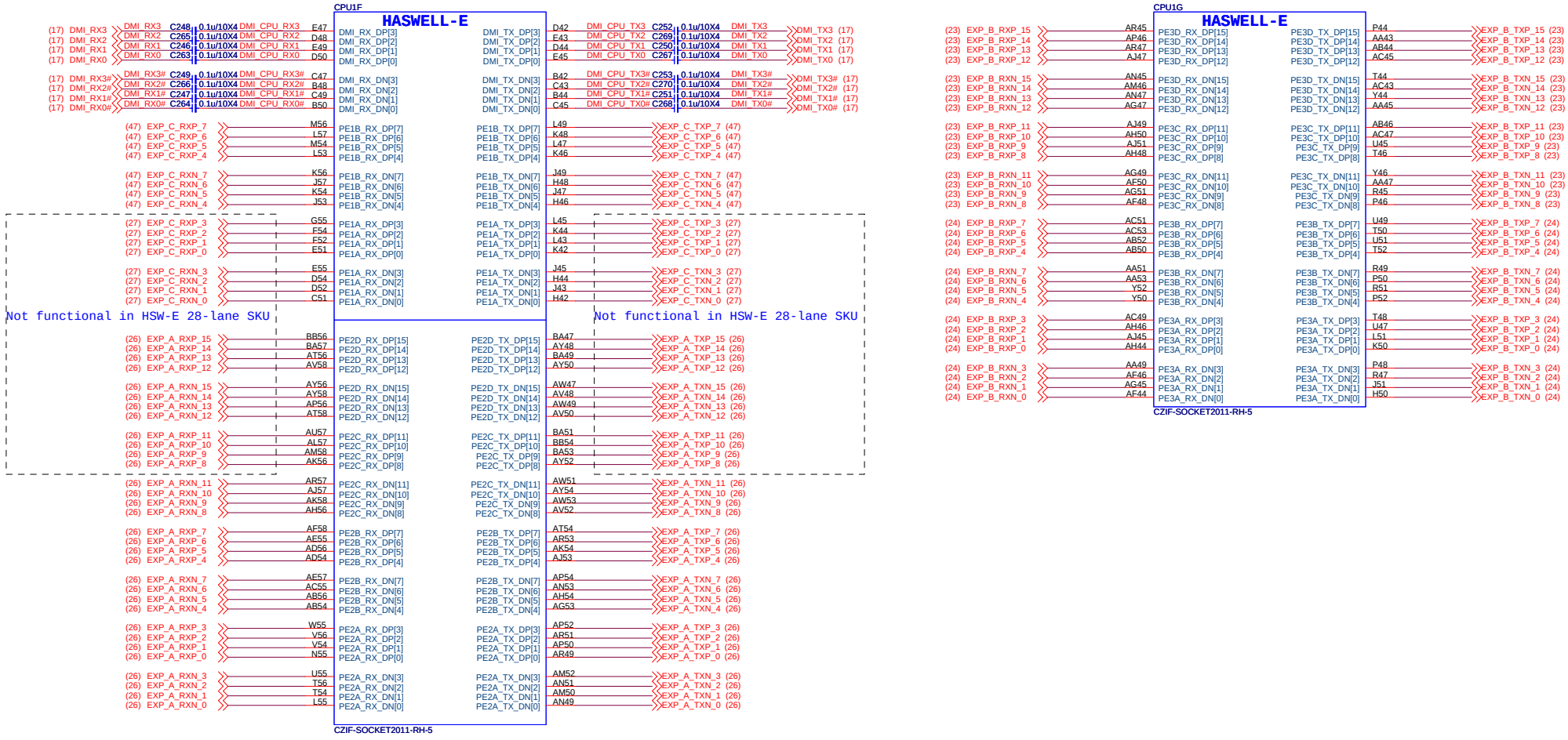
CPU-DMI/PEG



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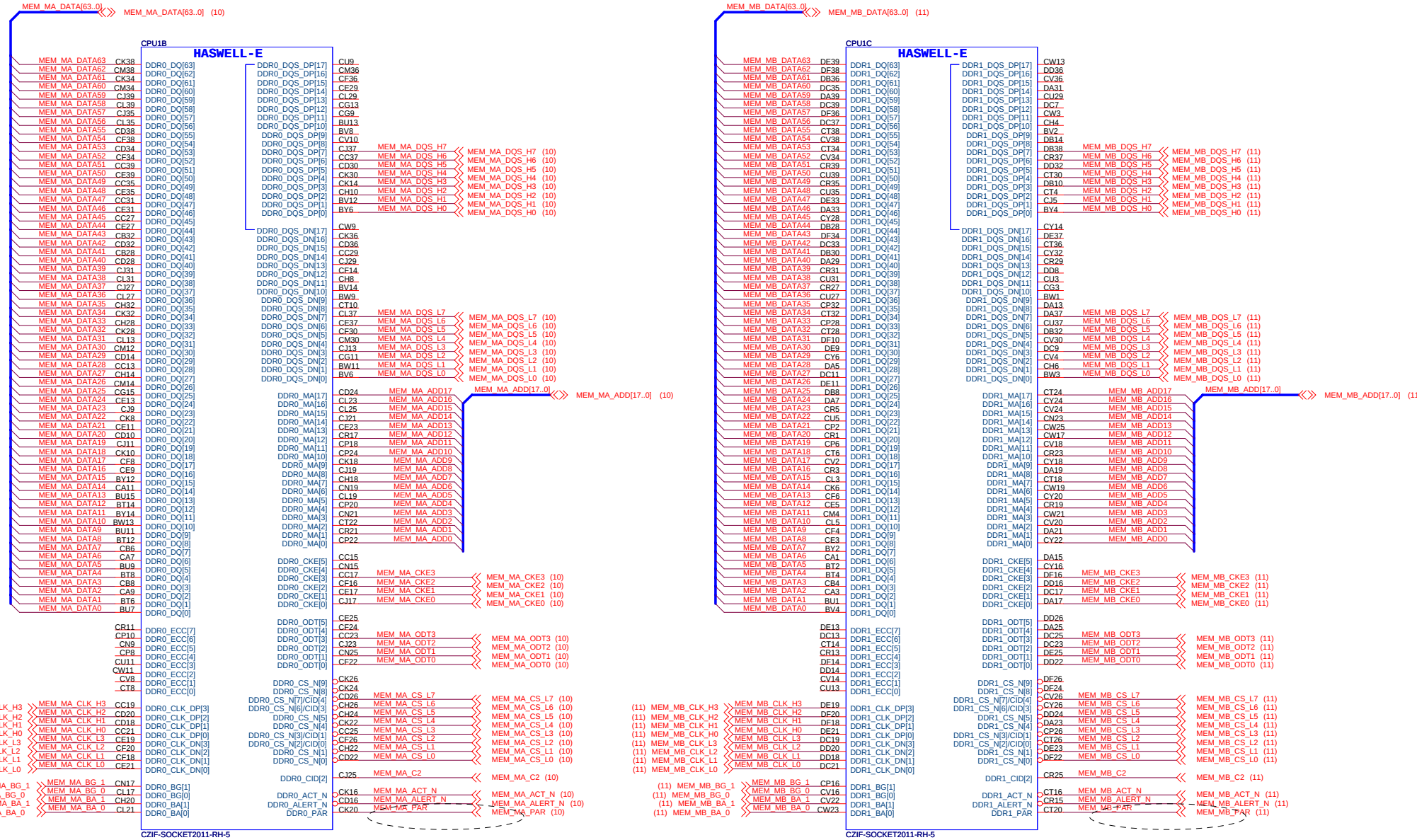
CPU-Memory0/1



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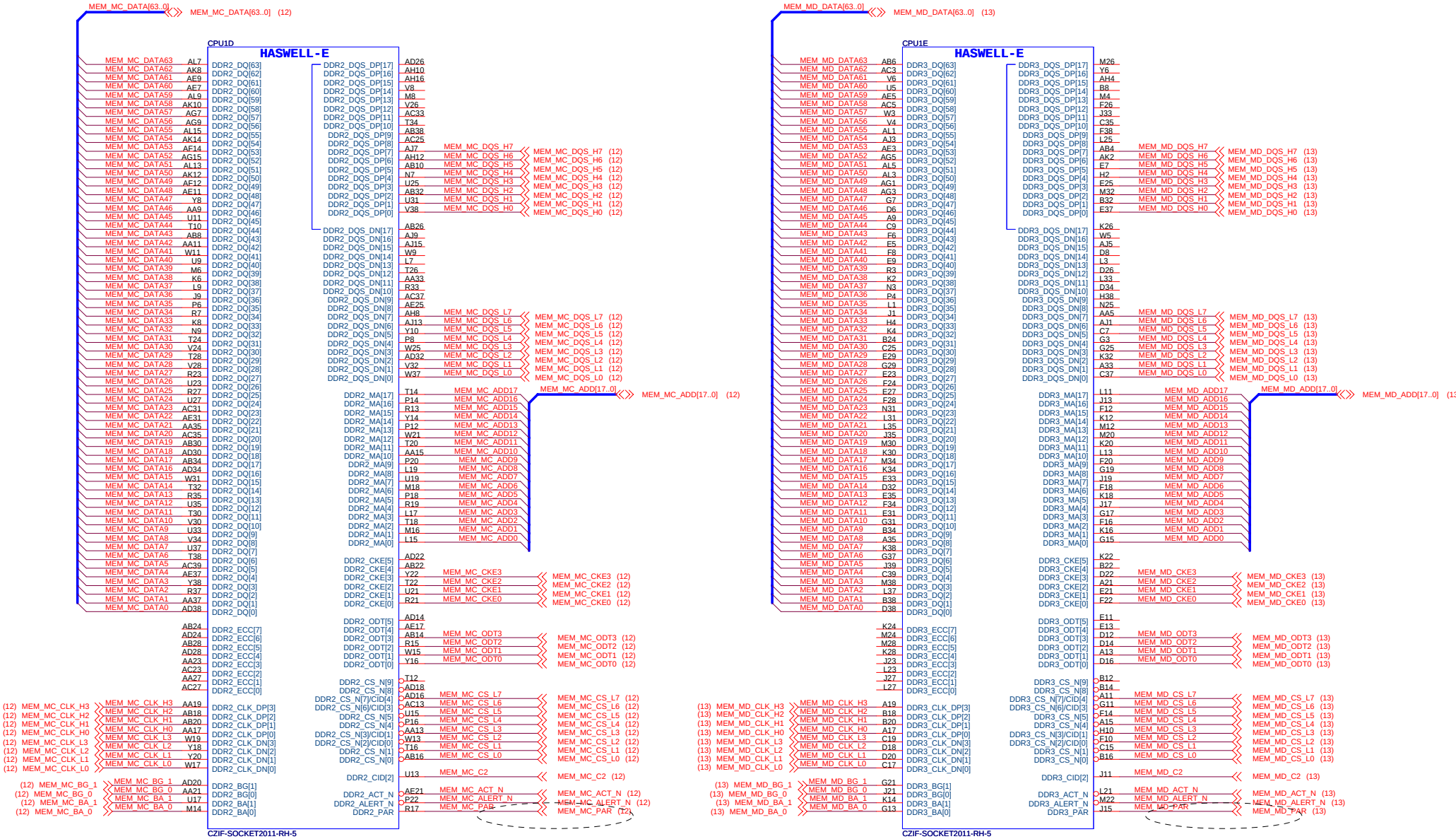
CPU-Memory2/3



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Size: Custom	Document Description: CPU-Memory2/3	Rev: 1.0
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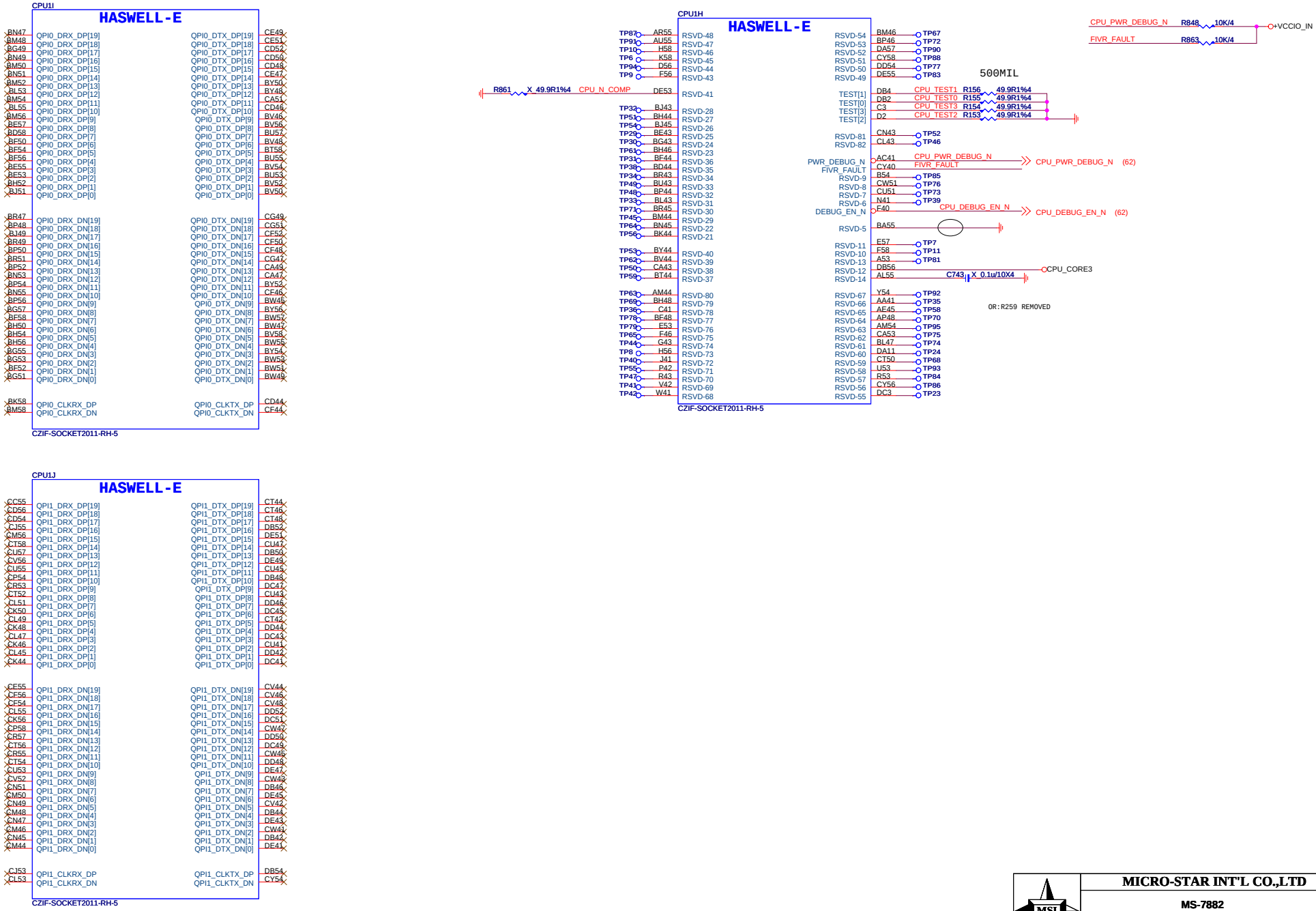
CPU-QPI/RESERVE



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Size: Custom	Document Description: CPU-QPI/RESERVE	Rev: 1.0
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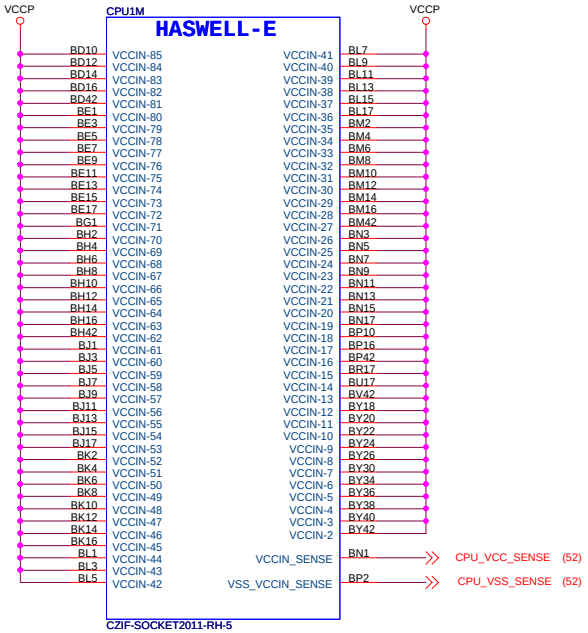
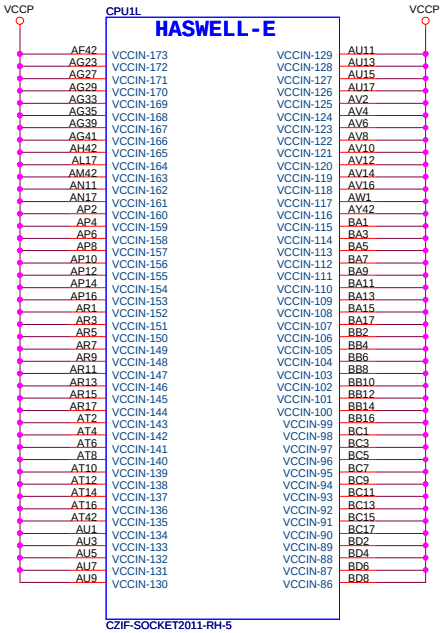
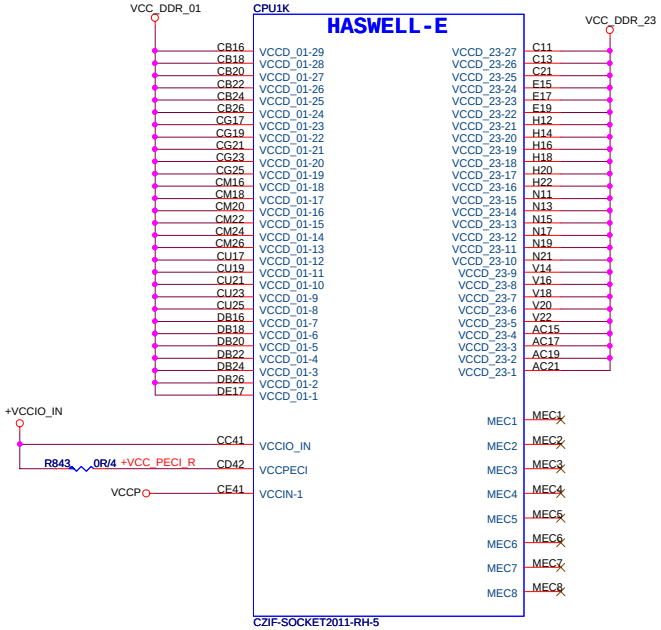
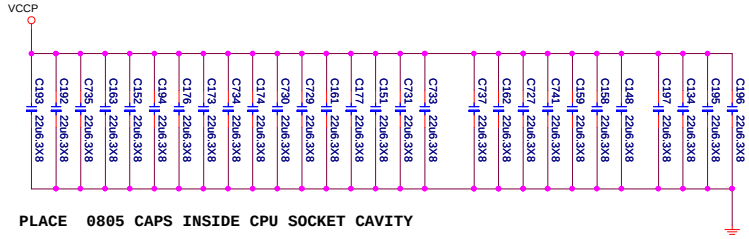
CPU-Power



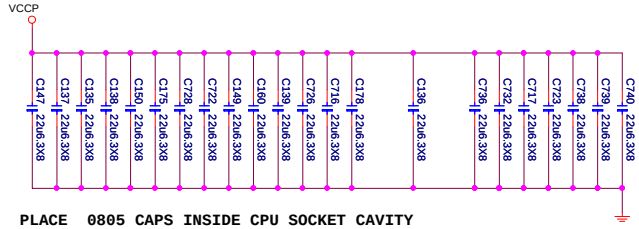




+CPU_VCCP-Decoupling



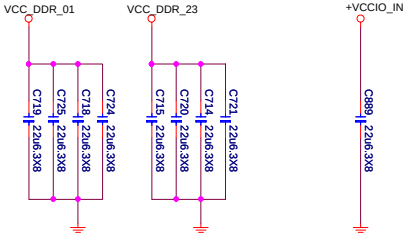
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

Skt cavity caps, place: 28 on top side & 26 on back side.

+CPU_DDR-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

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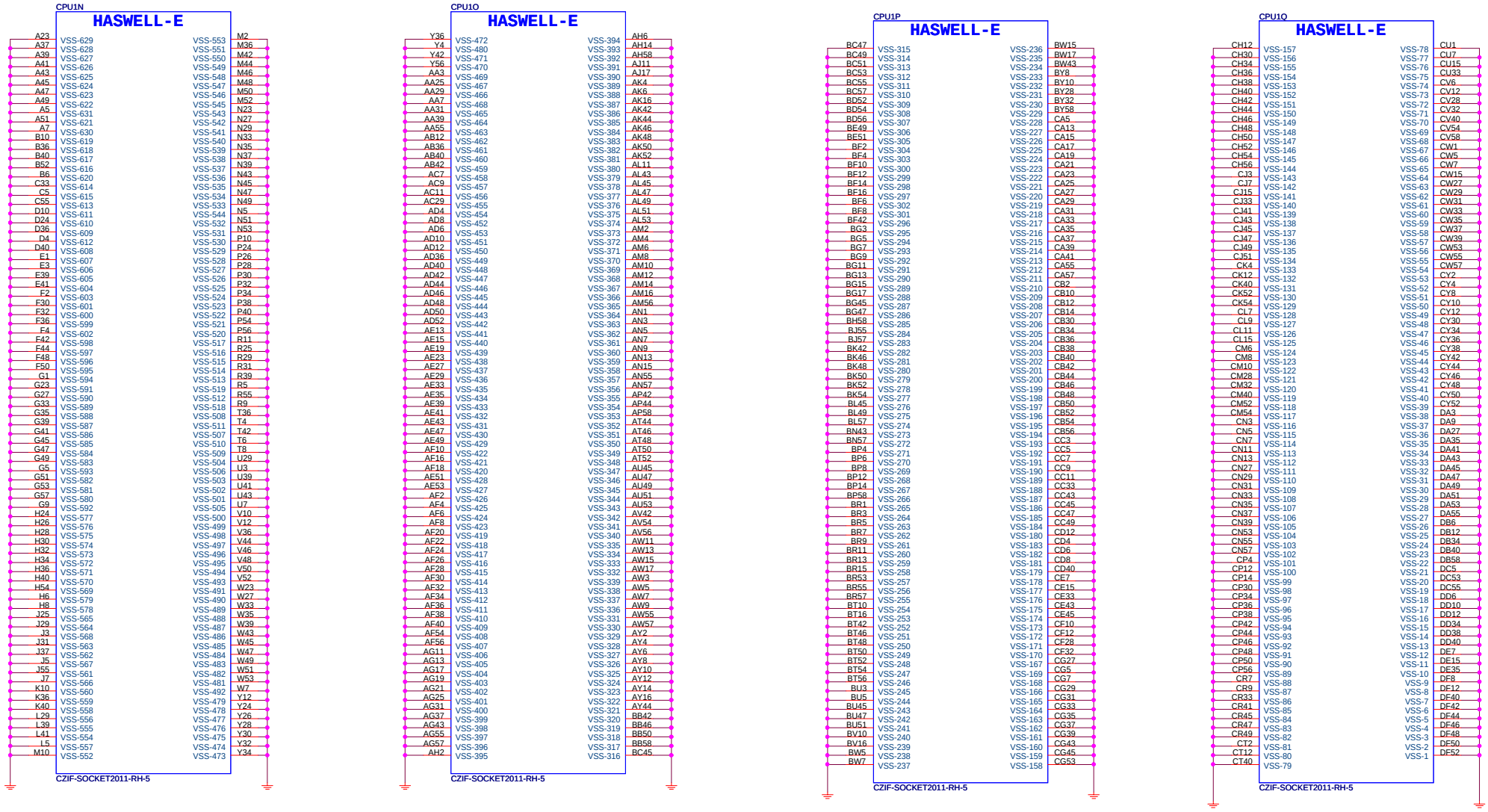
CPU-GND



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Size: Custom	Document Description: CPU-GND	Rev: 1.0
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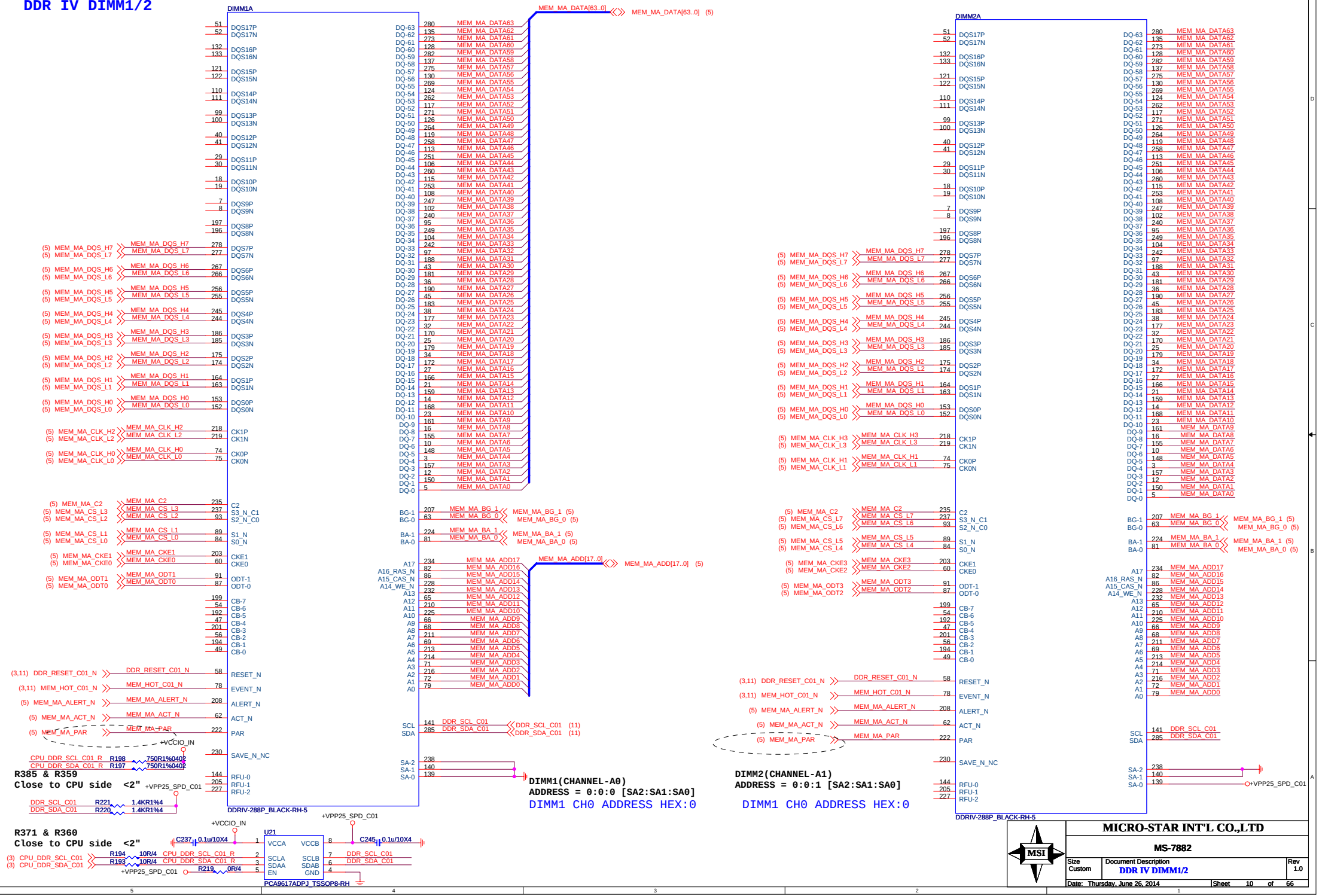
DDR IV DIMM1/2



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Size: Custom	Document Description: DDR IV DIMM1/2	Rev: 1.0
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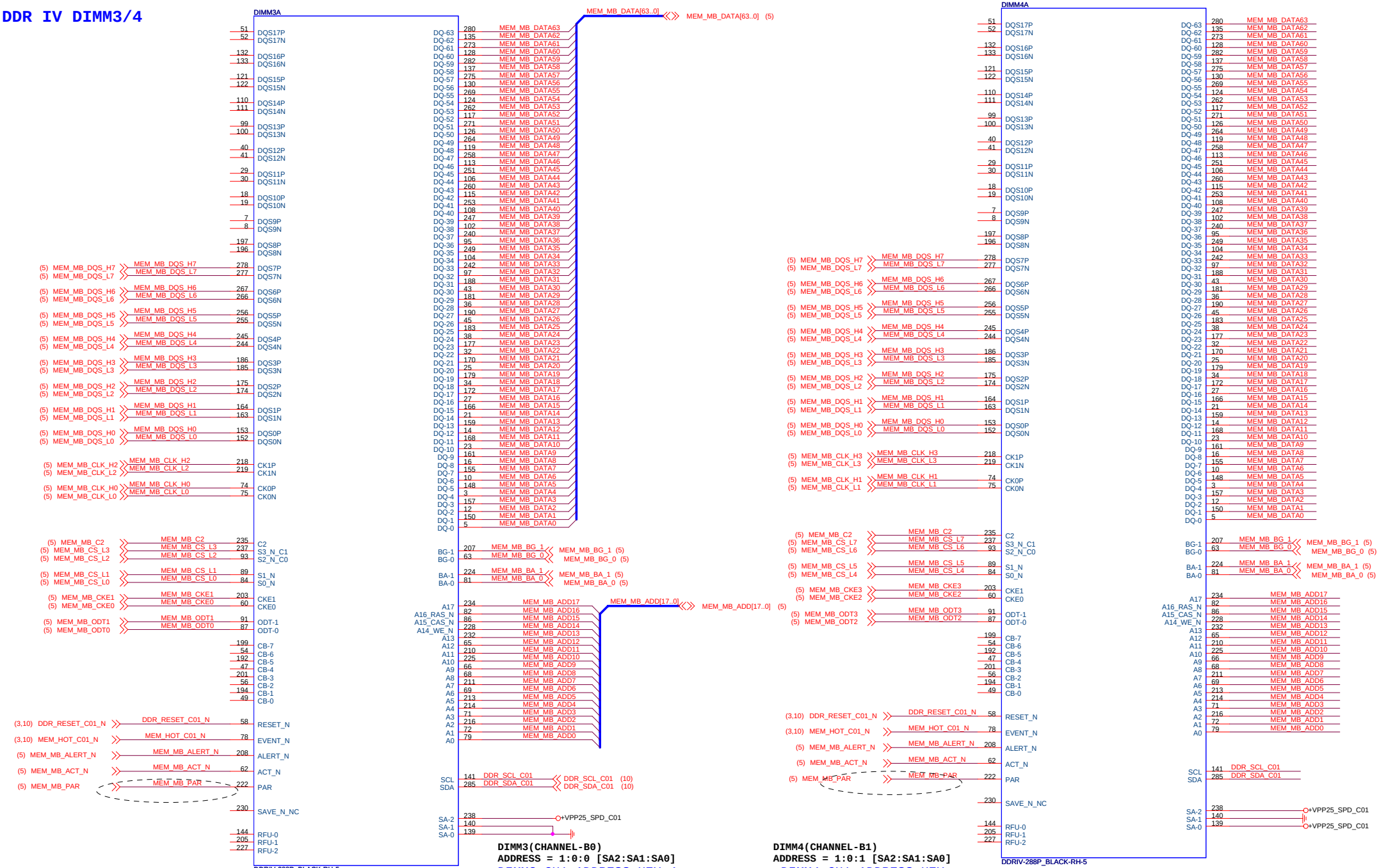
DDR IV DIMM3/4



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Size: Custom	Document Description: DDR IV DIMM3/4
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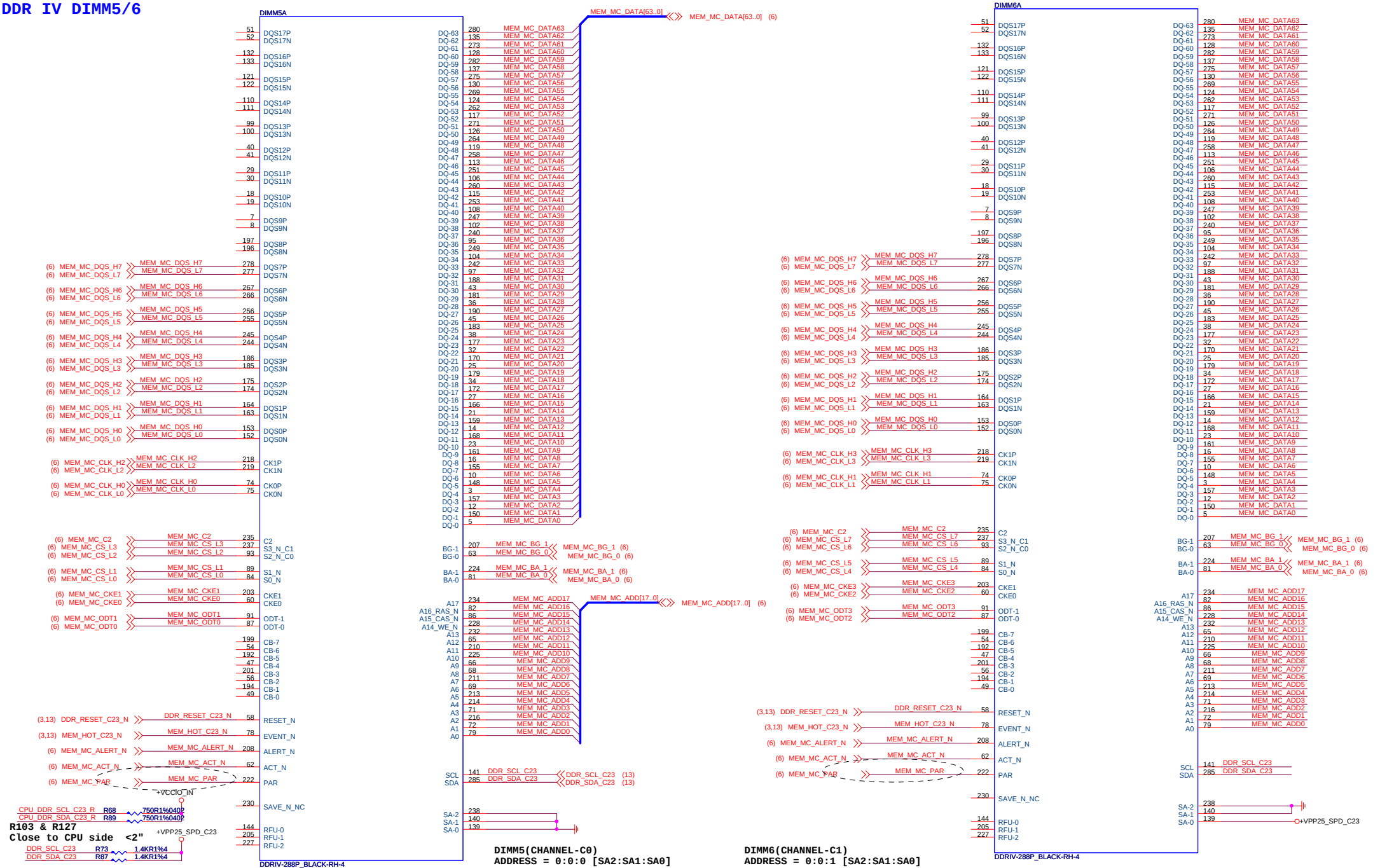
DDR IV DIMM5/6



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Size: Custom	Document Description: DDR IV DIMM5/6
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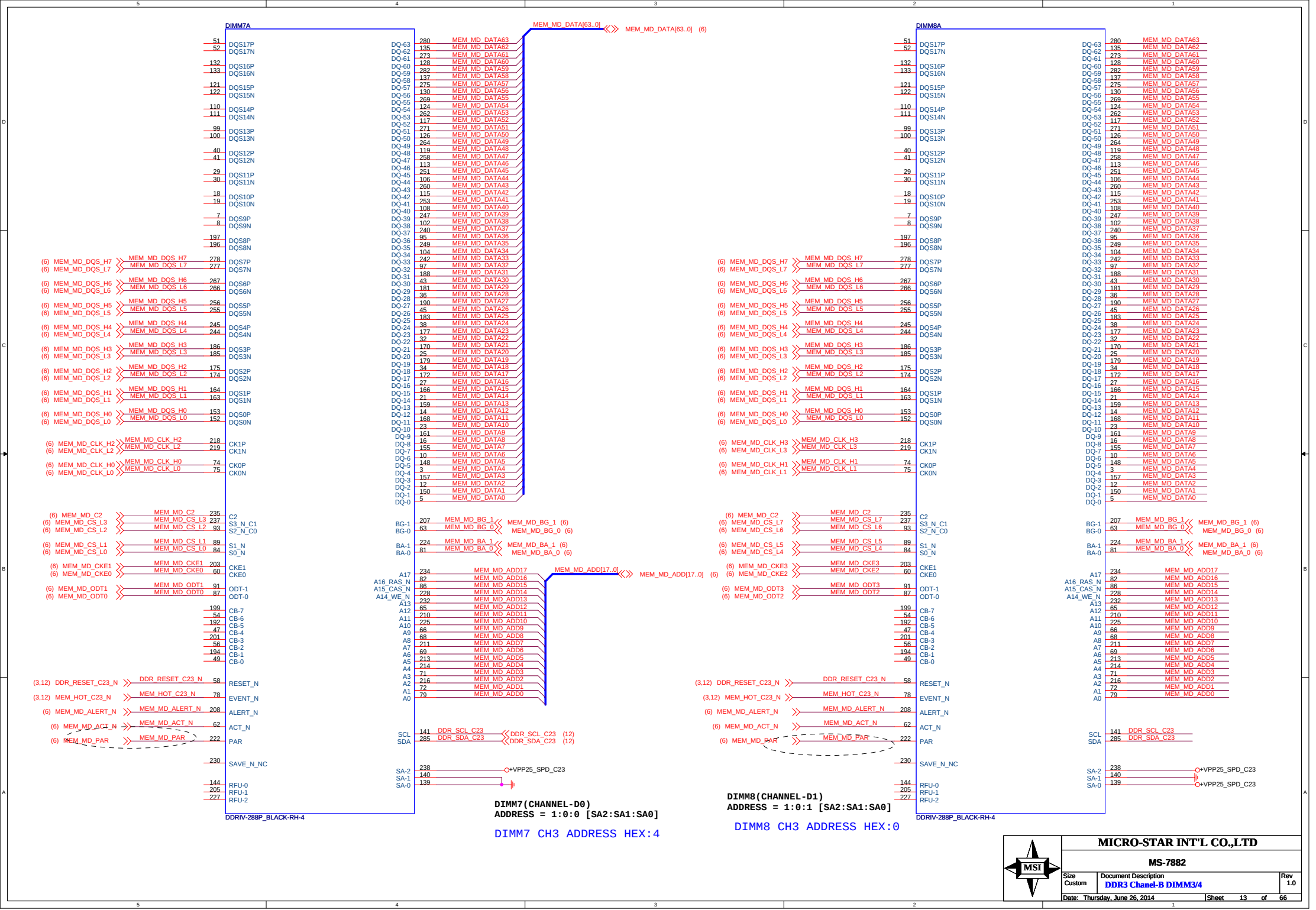

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Size	Document Description	Rev
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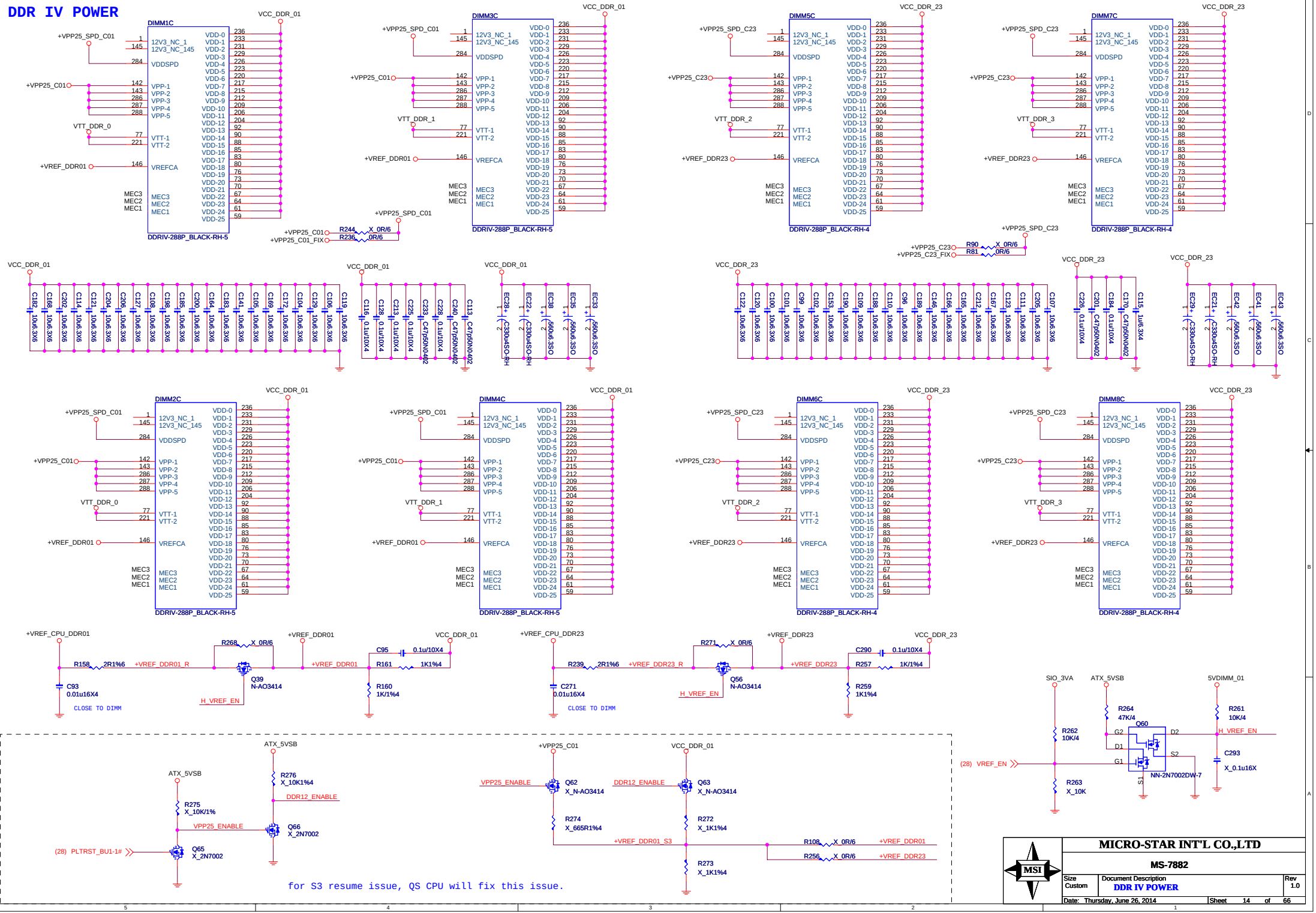
DDR IV POWER



MICRO-STAR INT'L CO.,LTD		
MS-7882		
Size: Custom	Document Description: DDR IV POWER	Rev: 1.0
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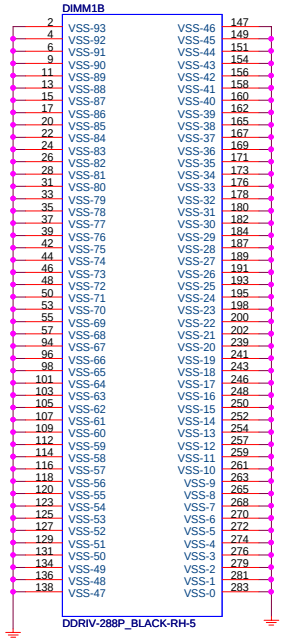
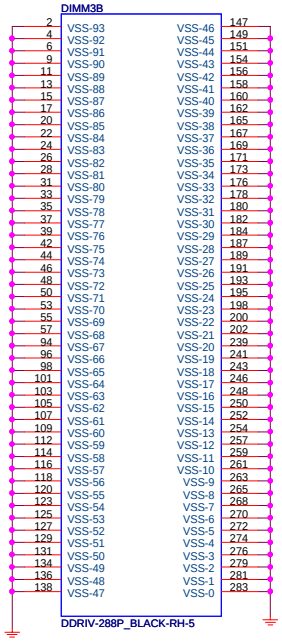
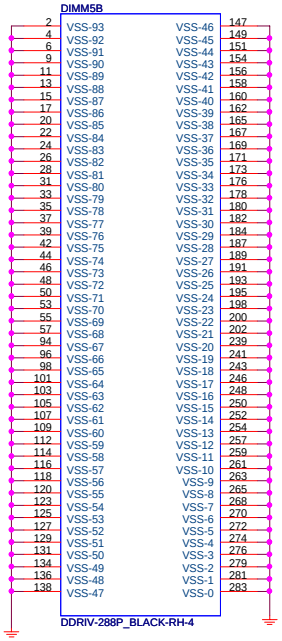
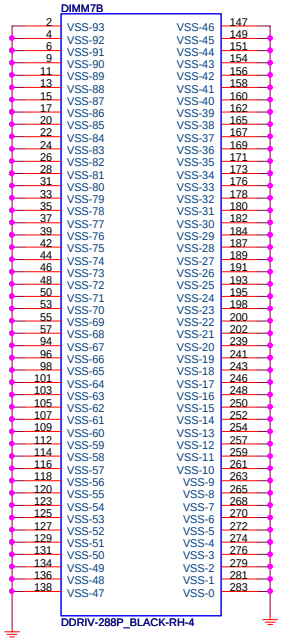
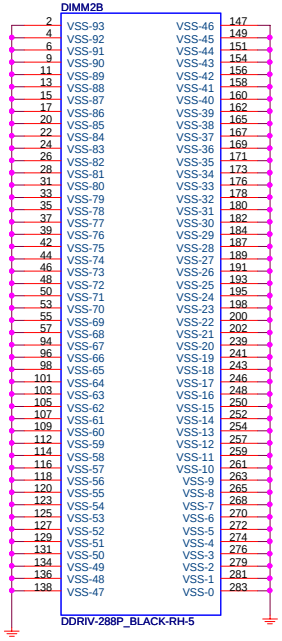
DDR IV GND

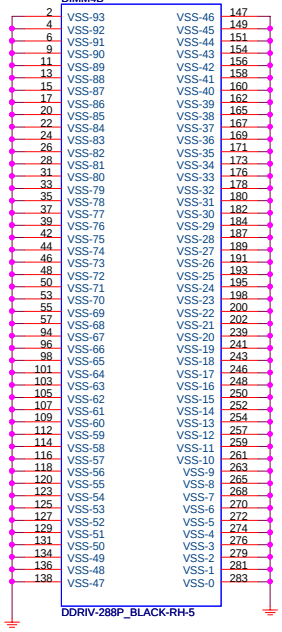


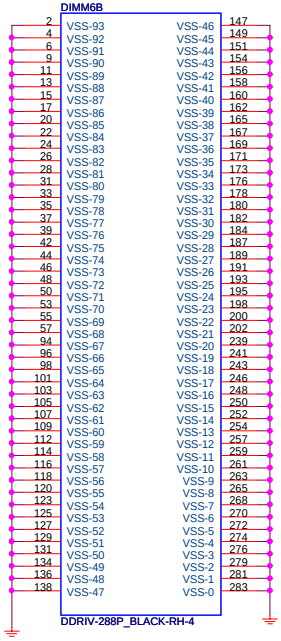


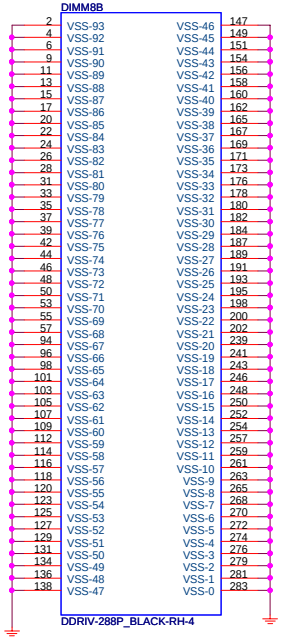












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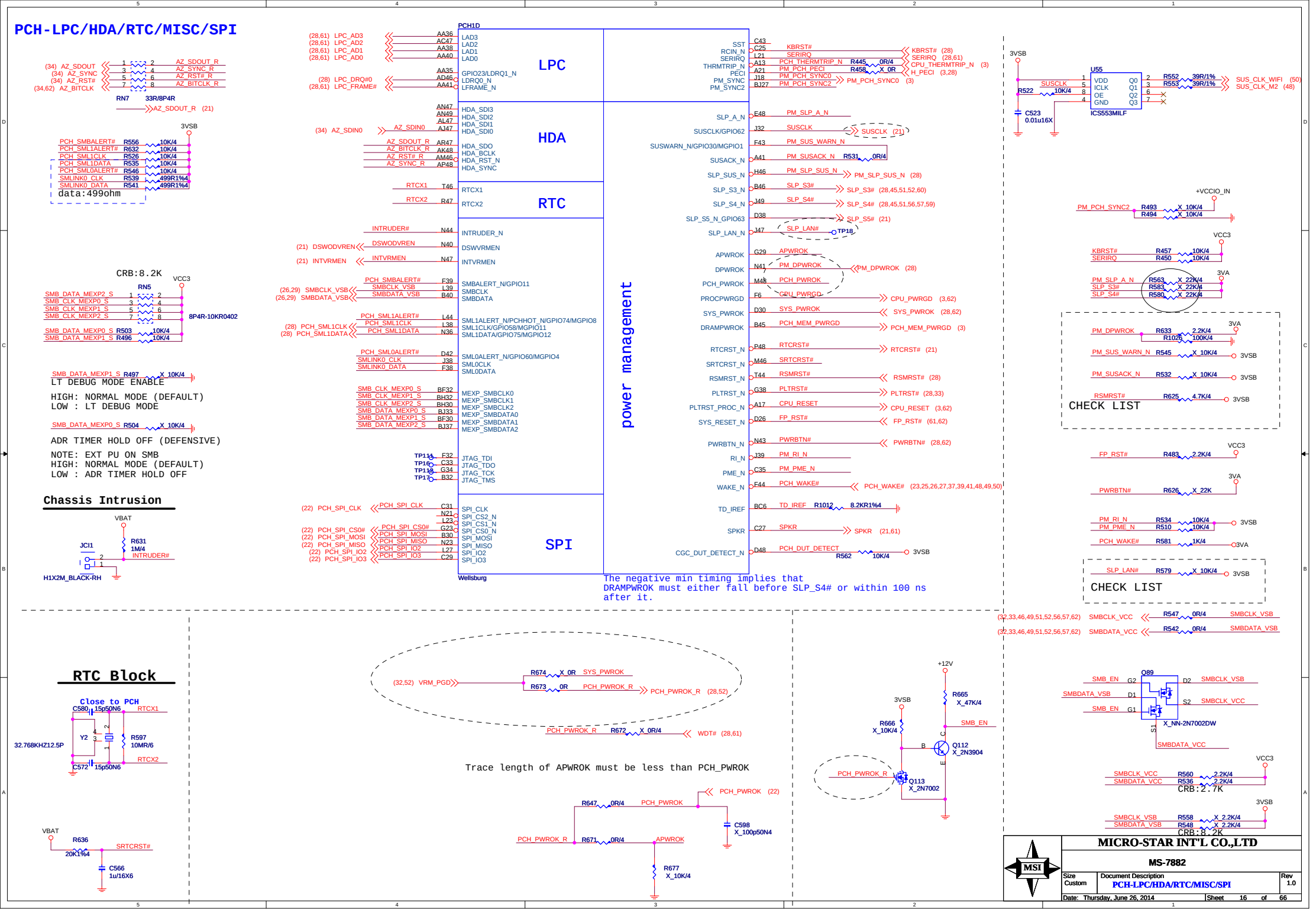
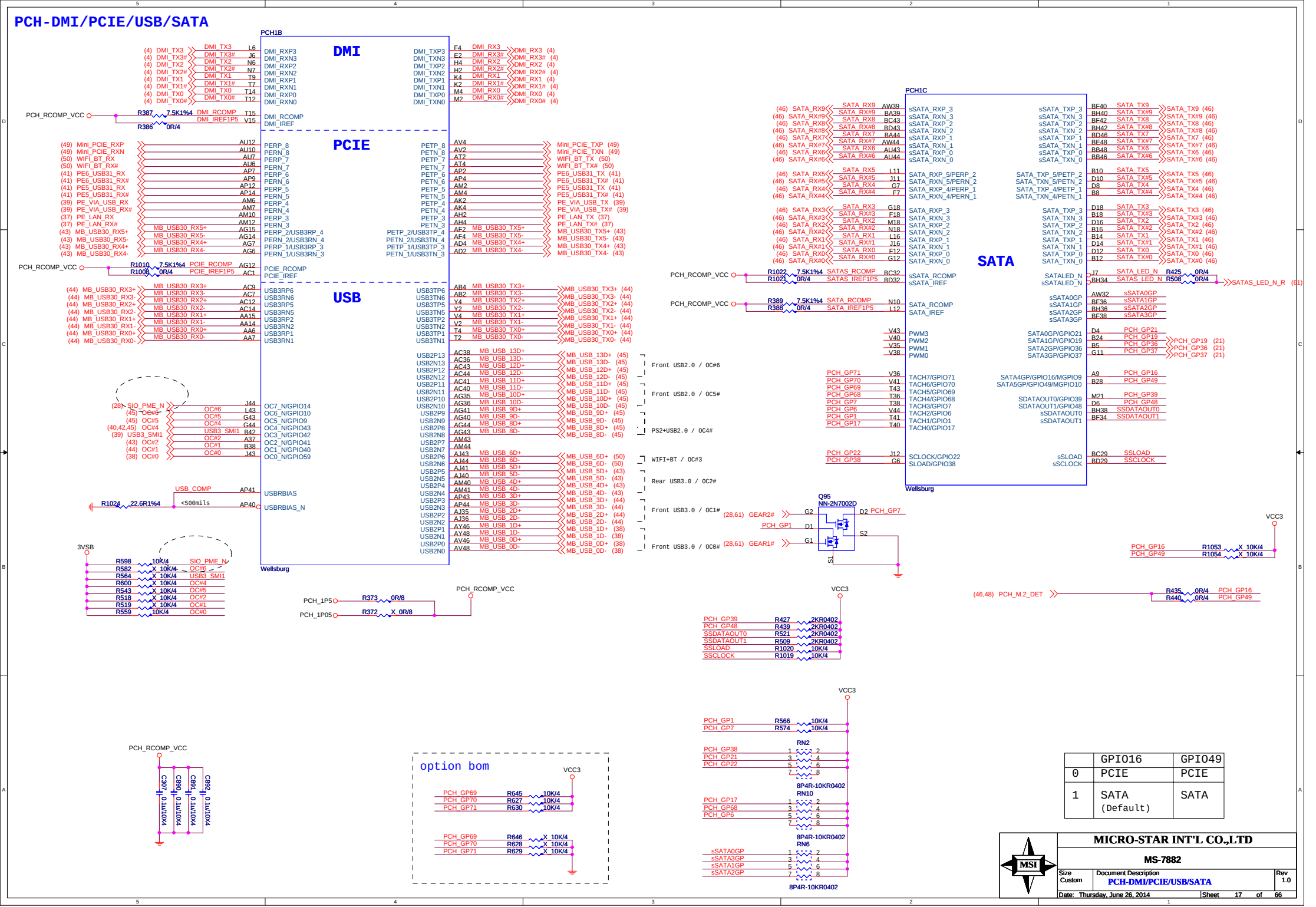
PCH-LPC/HDA/RTC/MISC/SPI



PCH-DMI/PCIE/USB/SATA



	GPIO16	GPIO49
0	PCIE	PCIE
1	SATA (Default)	SATA

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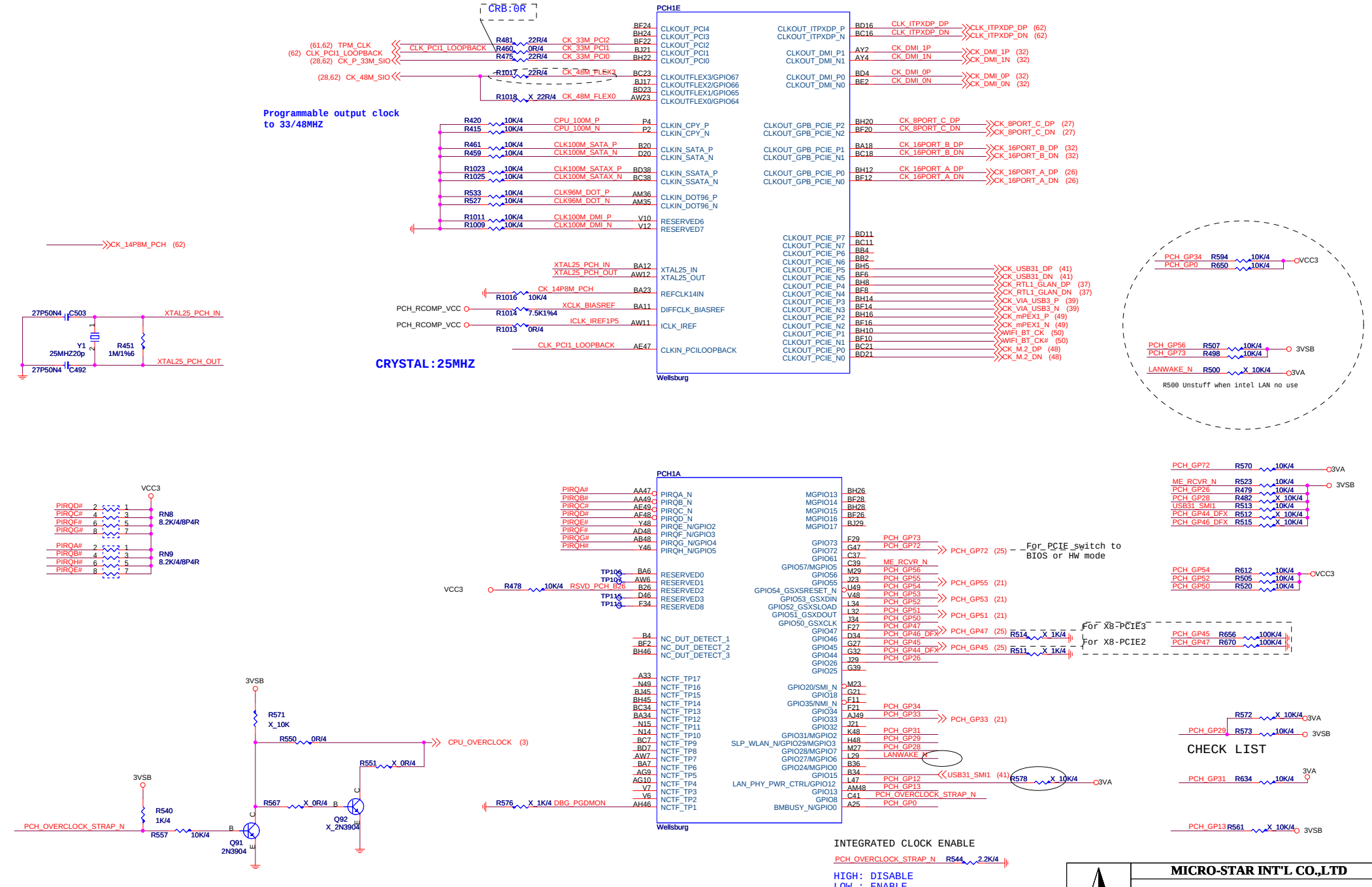
PCH-CLK/GPIO



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PCH-POWER

PCH_1P05:5.83A

+1P05V_ME:0.67A

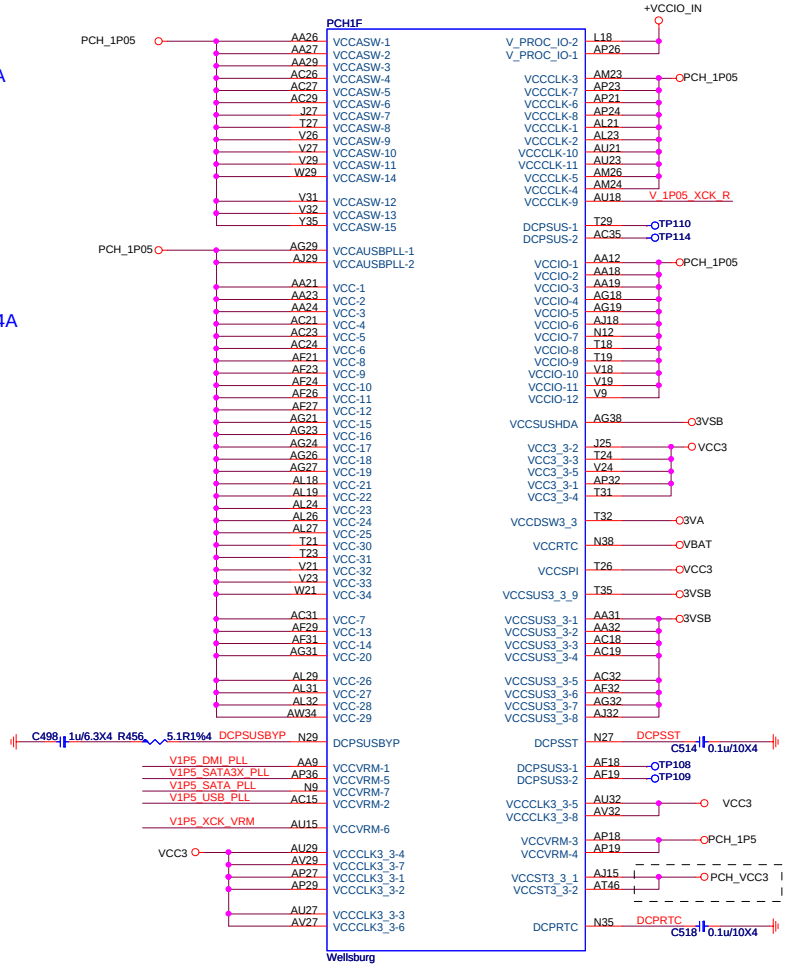
VCC3:0.2A

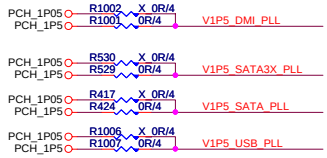
3VSB:0.27A

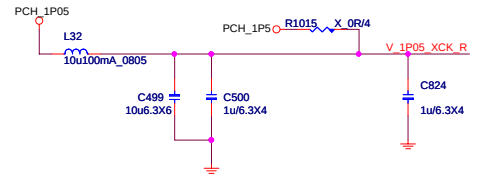
SPI_VCC3:0.02A

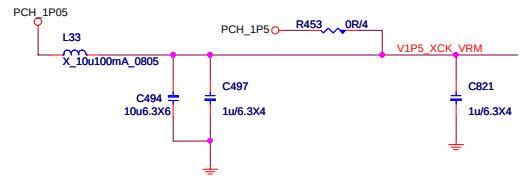
3VA:0.02A

+VCCIO_IN:0.004A

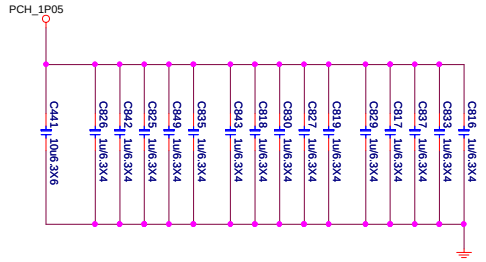


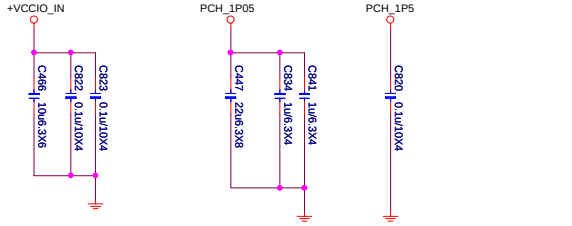


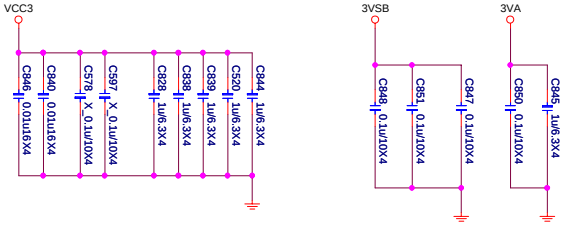


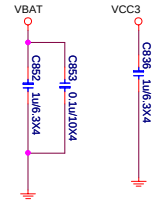


PCH decoupling cap









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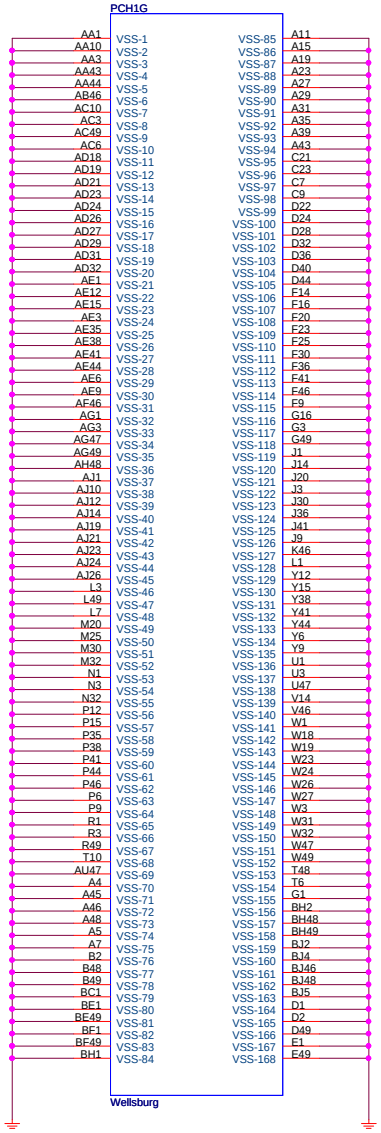
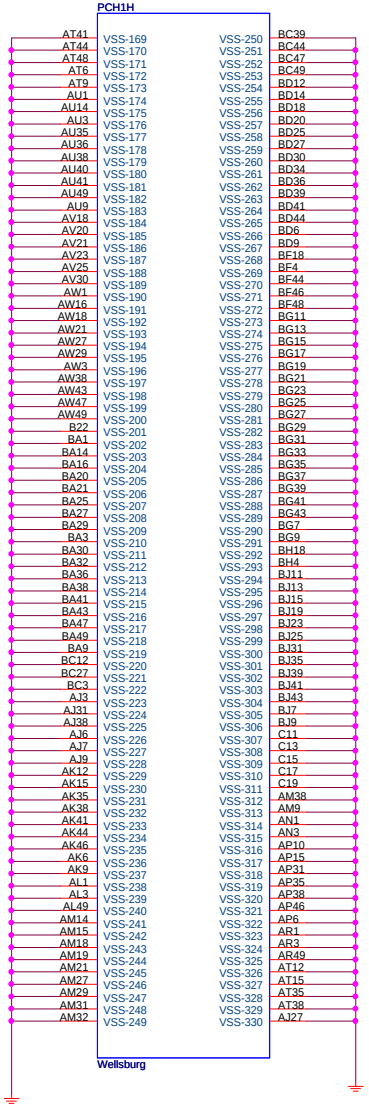
PCH - GND





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PCH Strap/Clear cMOS

	GP19	GP51
SPI	1	1
LPC	0	0

(17) PCH_GP19 — PCH_GP19 — R463 10K/4 — VCC3
R477 X_1K/4

(18) PCH_GP51 — PCH_GP51 — R524 10K/4 — VCC3
R525 X_1K/4

DMI RX Termination

(17) PCH_GP36 — PCH_GP36 — R434 X_1K/4 — R433 X_10K/4 — VCC3

This signal has a weak internal pull-down.
This signal only take effect if DMI is configured in AC-coupled mode.
0 = DMI RX is terminated to VSS.
1 = option not supported.

(17) PCH_GP37 — PCH_GP37 — R431 1K/4 — R430 X_10K/4 — VCC3

TLS CONFIDENTIALITY ENABLE STRAP

HIGH :TLS CONFIDENTIALITY ENABLE (DEFAULT)
LOW : RING OSCILLATOR BYPASS
LOW :TLS CONFIDENTIALITY DISABLE

ATX_5VSB — R590 47K/4
+12V — R565 47K/4
3VSB — R591 1K/4

Q94 (NN-2N7002DW-7): G2, D2, D1, S2, G1, S1
JME1: X_H1X2M-2PITCH_BLACK-HF
(28) ME_DIS#
AZ_SDOUT_R
AZ_SDOUT_R (16)

HIGH (1-2):SECURITY MEASURES OVERRIDEN
LOW (0-1) : SECURITY PER FLASH DESCRIPTOR (DEFAULT)

DEEP SLEEP WELL ON-DIE VRM ENABLE

VBAT — R599 390K/4 — DSWODVREN — DSWODVREN (16)

HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

INTEGRATED SUS 1.05V VRM ENABLE

VBAT — R635 390K/4 — INTVRMEN — INTVRMEN (16)

HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

PLL ON-DIE VR ENABLE

(16) SUSCLK — SUSCLK — R506 X_22K — R501 X_22K — 3VSB

HIGH :PLL ON-DIE VR ENABLE. INT PU. (DEFAULT)
LOW :PLL ON-DIE VR DISABLE

Top-Block Swap
Override

(18) PCH_GP55 — R462 10K/4 — R476 X_10K/4 — VCC3

DMI TX TERMINATION (DEFENSIVE)

(18) PCH_GP33 — PCH_GP33 — R585 X_10K/4 — R575 X_10K/4 — VCC3

This signal has a weak internal pull-down.
This signal only takes effect if DMI is configured in DC-coupled mode.
0 = DMI TX is terminated to VSS.
1 = DMI TX is terminated to VCC/2.

NO REBOOT OPTION STRAP

LOW : REBOOT
HIGH: NO-REBOOT

(16,61) SPKR — R495 1K/4 — VCC3

DMI AC Coupling

CHECK LIST

(18) PCH_GP53 — R586 X_10K/4 — R568 1K/4 — VCC3

This Signal has a weak internal pull-up.
0= Configures DMI for AC coupling mode.
1 = Configures DMI for DC coupling mode.

RTC and CLR_CMOS

SIO_3VA — R749 4.7K/4
SIO_3VA — R744 4.7K/4

(28) CLR_CMOS# — Q132 2N7002 — R750 0R/4 — RTCRST# — RTCRST# (16)
C668 0.1u/10X4
RTCRST# — R755 20K1%4 — VBAT
C665 1u/16X6

Only connector to PCH

RTCRST# — R763 X_0R/4 — RTCRST#_D
co-lay

VBAT — U70 NC7SP125P5X
RTCRST# — RTCRST#_D
RTCRST#_D — RTCRST#_D (28)
connector to other RTCRST#

3VA — D6 S-BAT54C-SOT23 — R316 1K1%4 — BAT1 BAT-2P-RH-1
20mil
Close to PCH

VBAT — JBAT1 H1X2M_BLACK-RH — R789 20K1%4 — C689 1u/16X6 — C396 1u/16X6

ATX_5VSB — R145 10K/1%4
CLR_CMOS1: RTCRST#_D (28), CCMOS_LED_R
CCMOS_LED — Q34 2N7002 — C90 X_0.1u16X — SW-TACTB1-RH-5
(16) SLP_S5# — SLP_S5#
(22,28,36,41,43,48,50,61,62) ALL_LED_OFF# — Q36 2N7002

LED LIGHTING RULE	
S0/S3/S4	: LED OFF
S5	: LED ON

tri-state

INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

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(16) PCH_SPI_CS0# PCH_SPI_CS0#

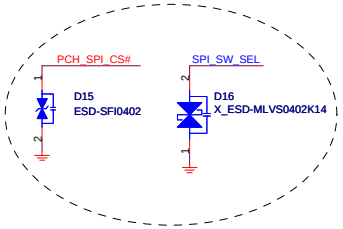
(16) PCH_SPI_MOSI PCH_SPI_MOSI

(16) PCH_SPI_MISO PCH_SPI_MISO

(16) PCH_SPI_CLK PCH_SPI_CLK

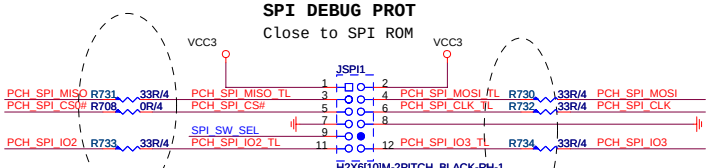
(16) PCH_SPI_IO2 PCH_SPI_IO2

(16) PCH_SPI_IO3 PCH_SPI_IO3



SPI DEBUG PROT

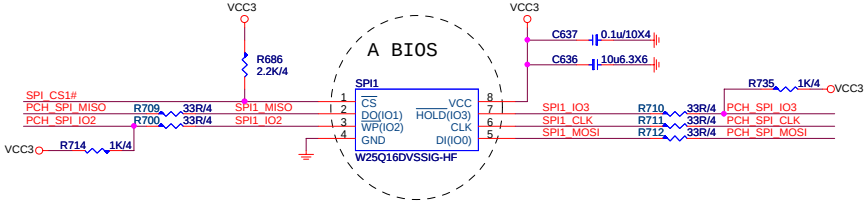
Close to SPI ROM



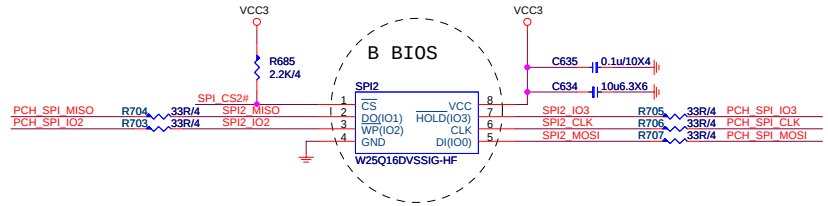
Part Number:N31-2061341-H06

(16) PCH_PWROK PCH_PWROK R1065 0R/4 SPI_SW_SEL

2014.06.05 Add for support TL624-1.1



16M ROM



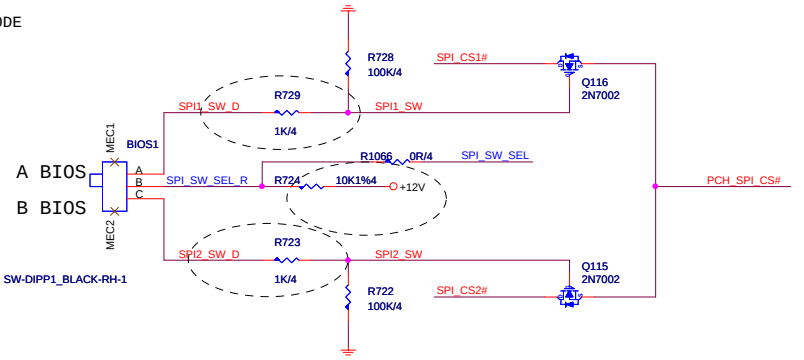
SPI FLASH ROM

Place close to SB.

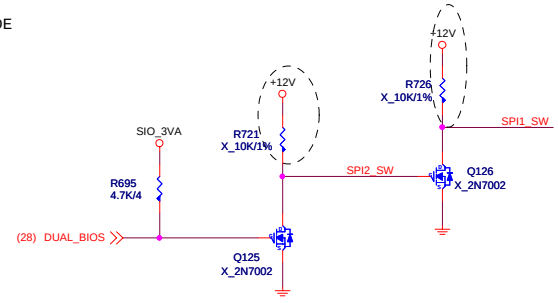
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.

OPTION BIOS

HW MODE



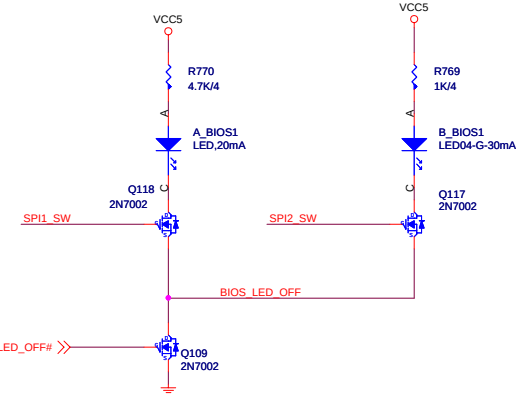
BIOS MODE

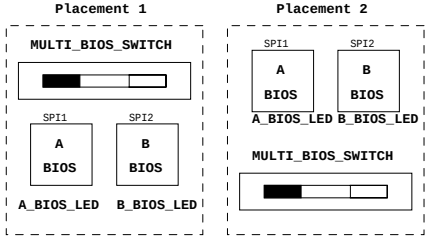


* if you not support Standby power in S5 Status, component "MULTI_BIOS_SWITCH1.B(PIN B) " Pull-high to +12V & Q12/Q13 MOS select 2N7002

* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset) , component "MULTI_BIOS_SWITCH1.B(PIN B)" pull-igh to ATX_5VSB , component Q12/Q13 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30





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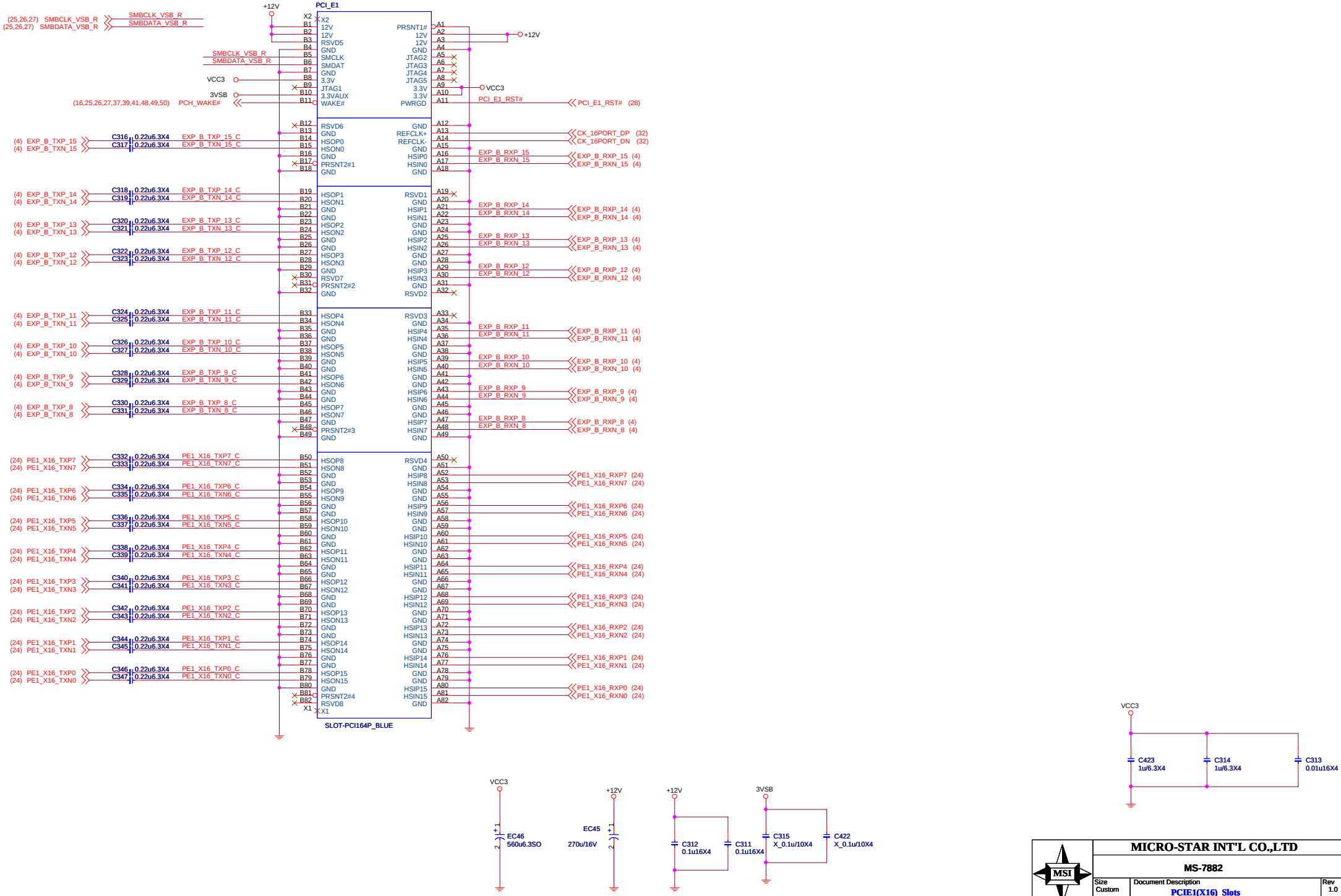
PCIE1(X16) & PCIE2(X1) Slots



MICRO-STAR INT'L CO.,LTD	
MS-7882	
Size: Custom	Document Description: PCIE1(X16) Slots
Rev: 1.0	
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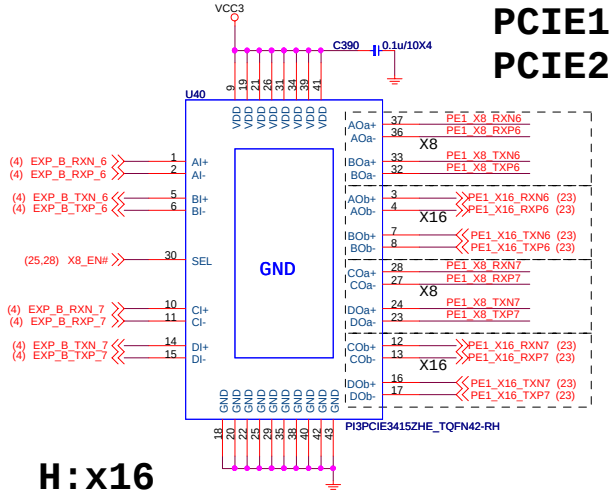
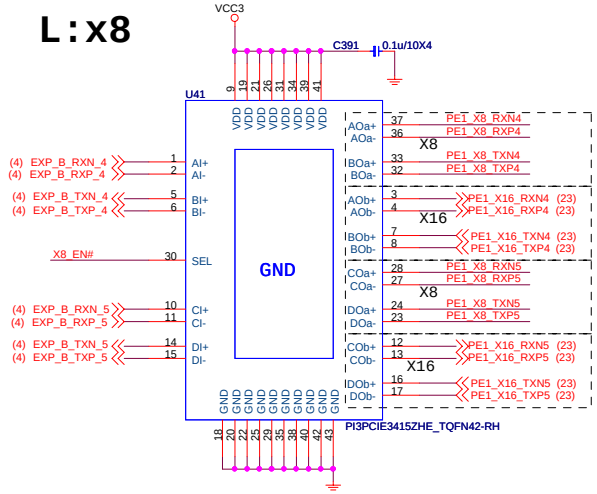
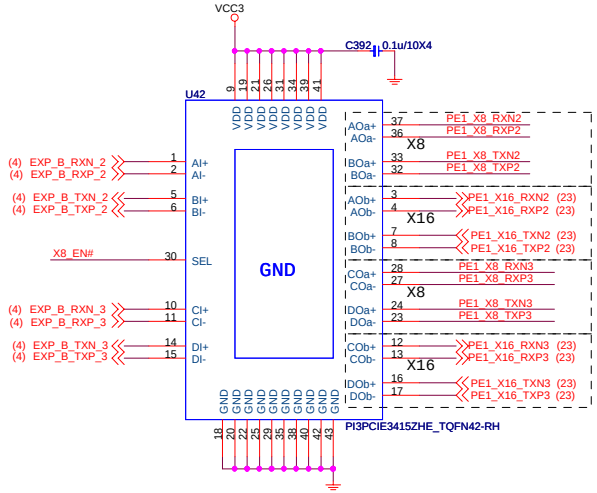
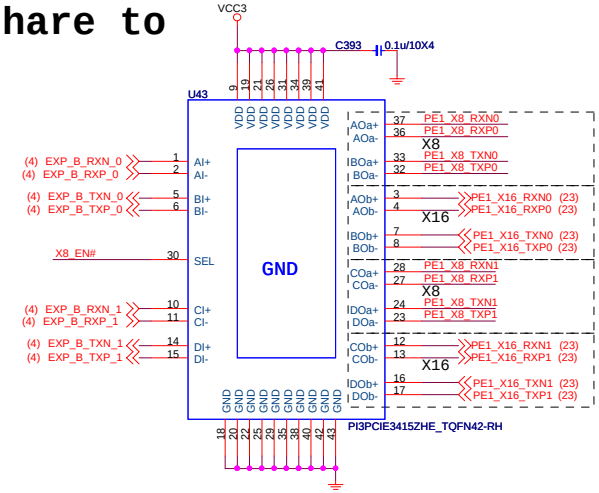
PCIE1(x16) share to PCIE2(x8)

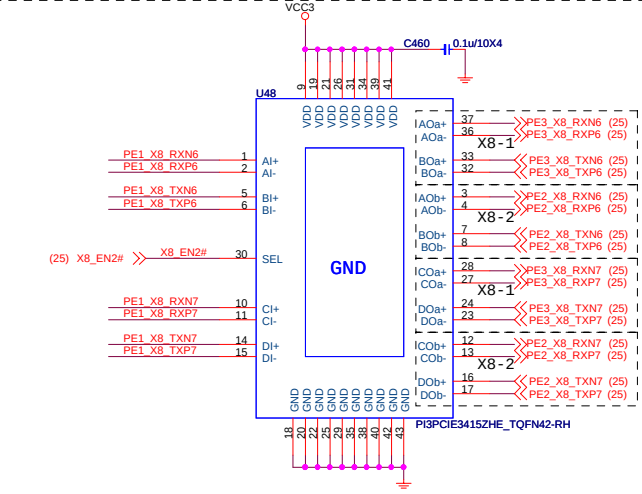
H:x16
L:x8

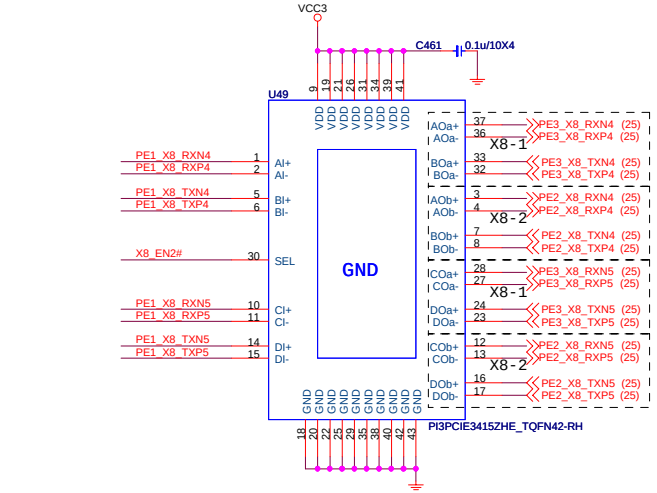




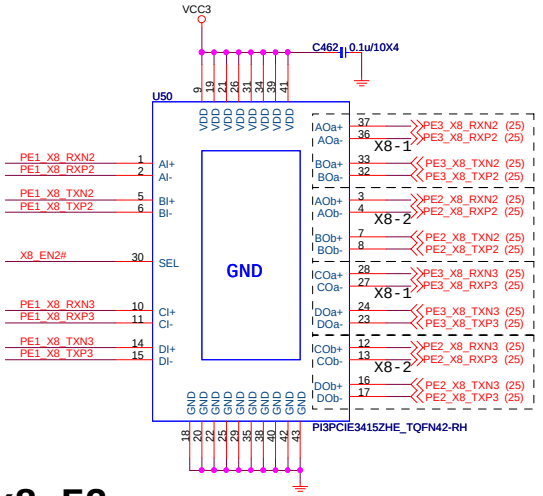




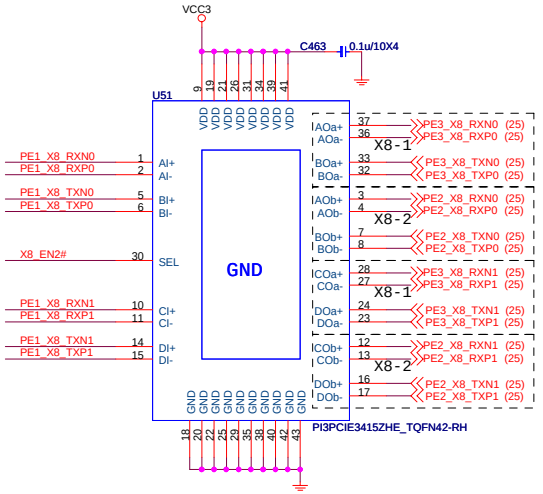




Switch PCIE(x8) for PCIE2 or PCIE3



H:x8-E2
L:x8-E3



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	MS-7882	
Size: Custom	Document Description: PCIE Switch 3415	Rev: 1.0
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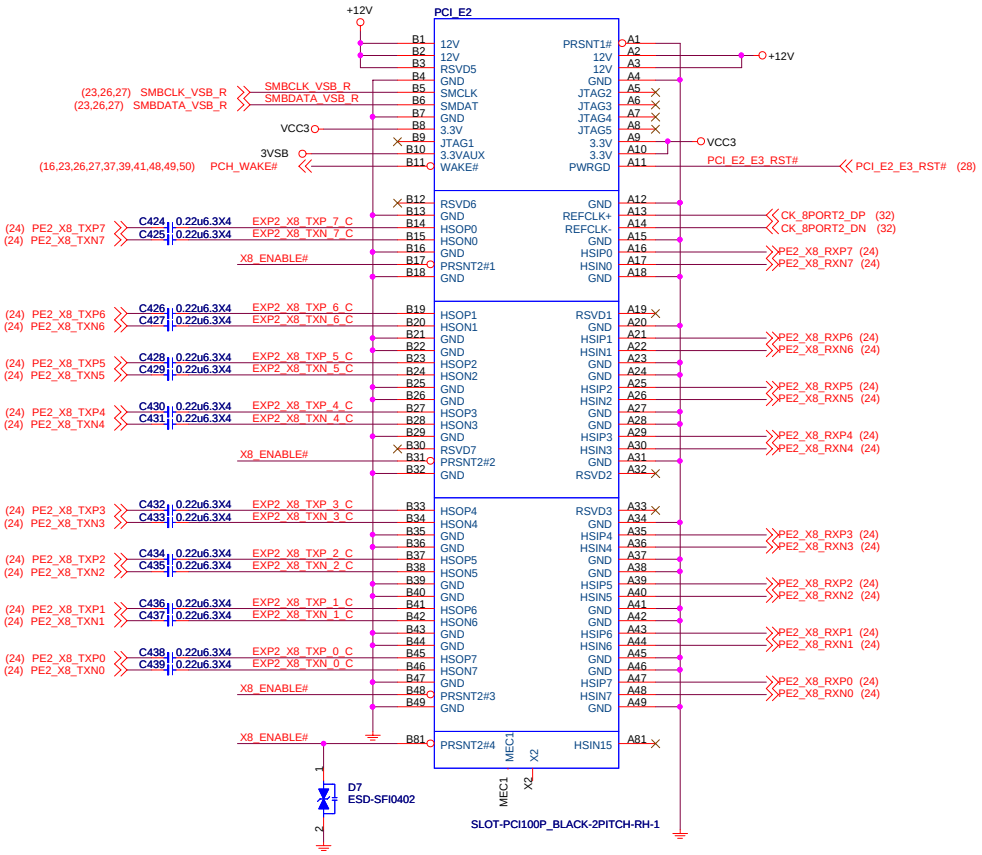
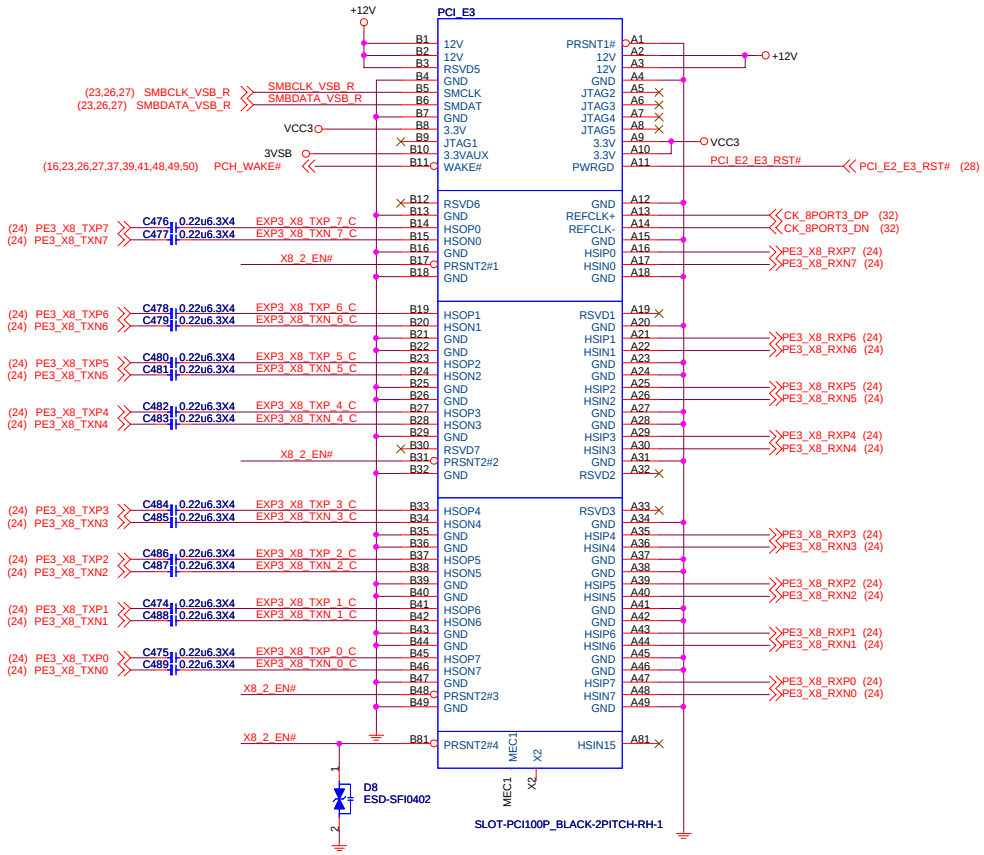
PCIE5(X8) /PCIE3415





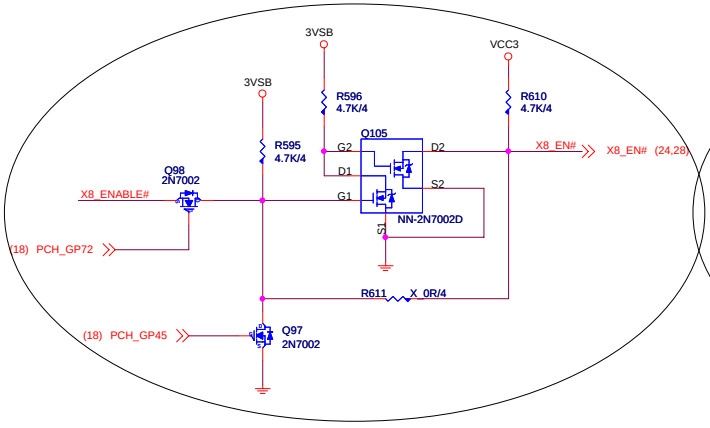
GPIO72

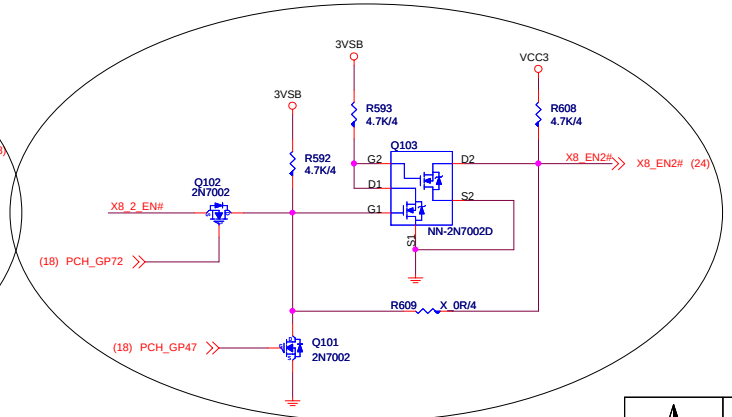
0: BIOS MODE
1: HW MODE

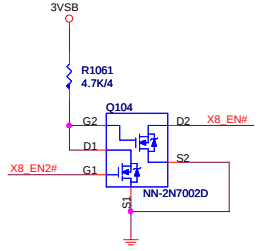
If USE HW MODE
PCH_GPIO45/47 programming to GPI
PCH_GPIO72 programming GPO

If USE BIOS MODE
PCH_GPIO45/47 programming to GPO

PCH Status	GPIO72	GPIO45	GPIO47
AUTO	1	GPI(def:0)	
16,0,0	0	X	X
8,8,0	0	1	0
8,0,8	0	0	1







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Custom	PCIE2&3(X8) /PCIE3415	1.0

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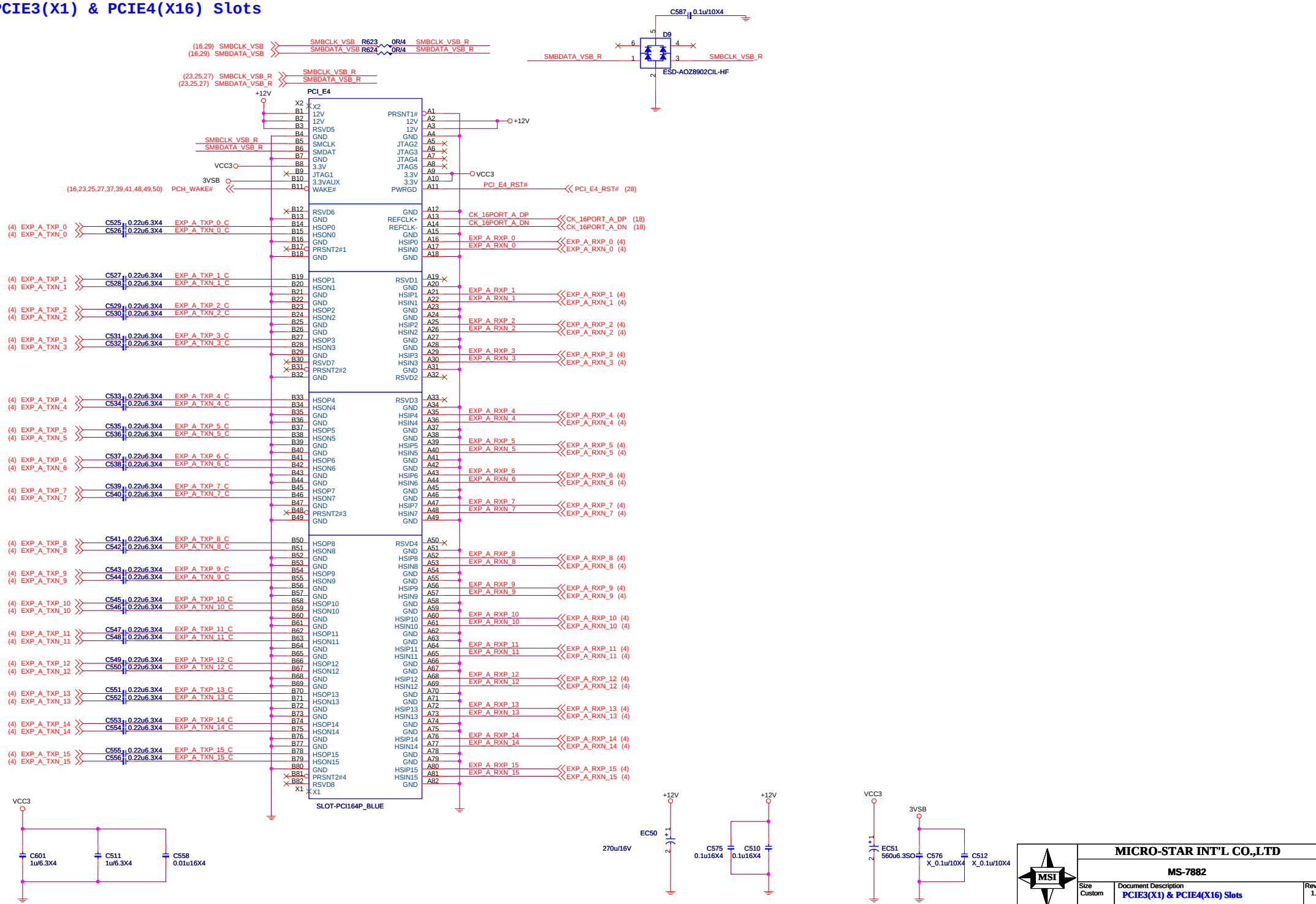
PCIE3(X1) & PCIE4(X16) Slots



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PCIE3(X1) & PCIE4(X16) Slots
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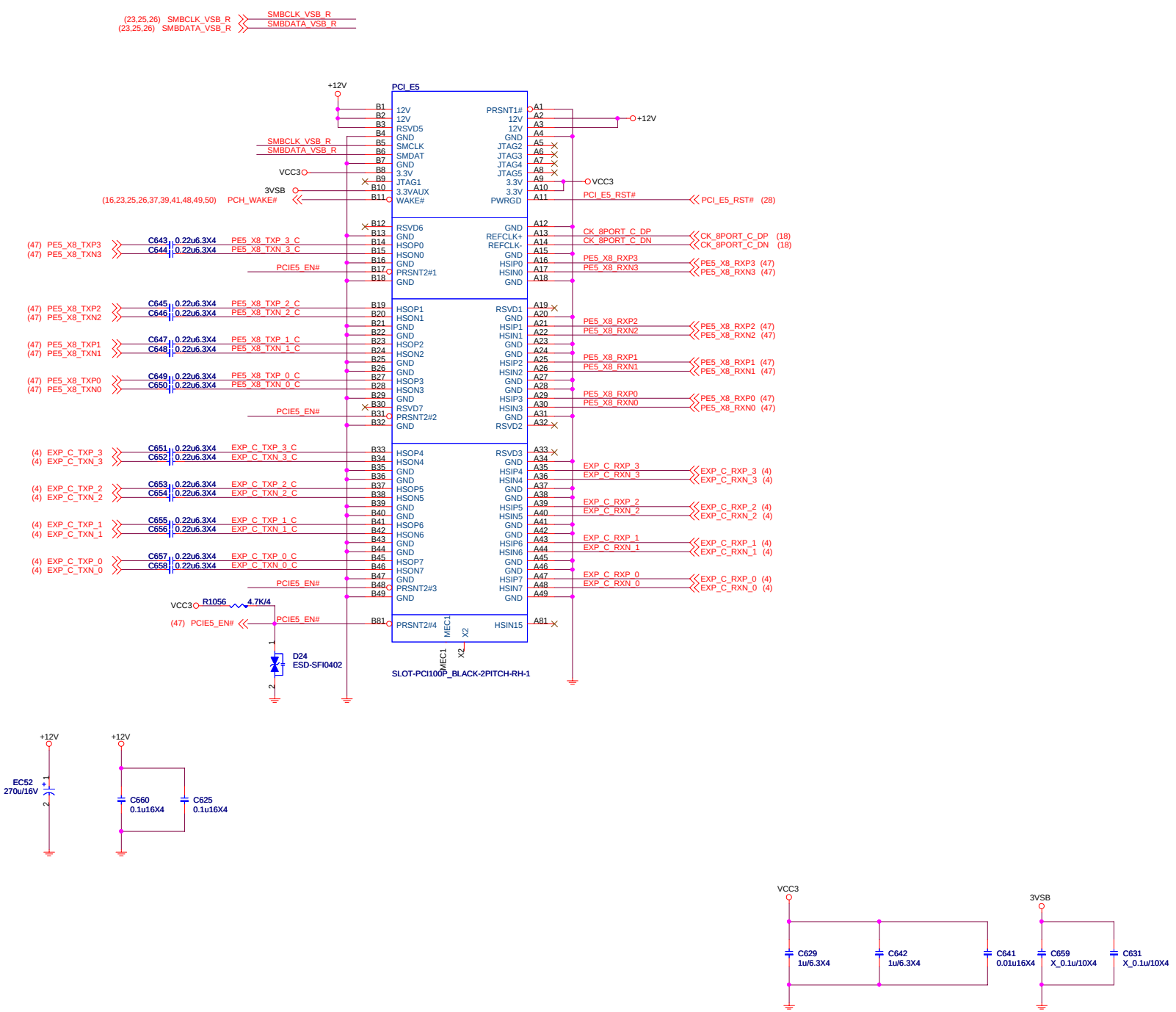
PCIE5(X8) Slots



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MS-7882	
Size: Custom	Document Description: PCIE6(X8) Slots
Rev: 1.0	
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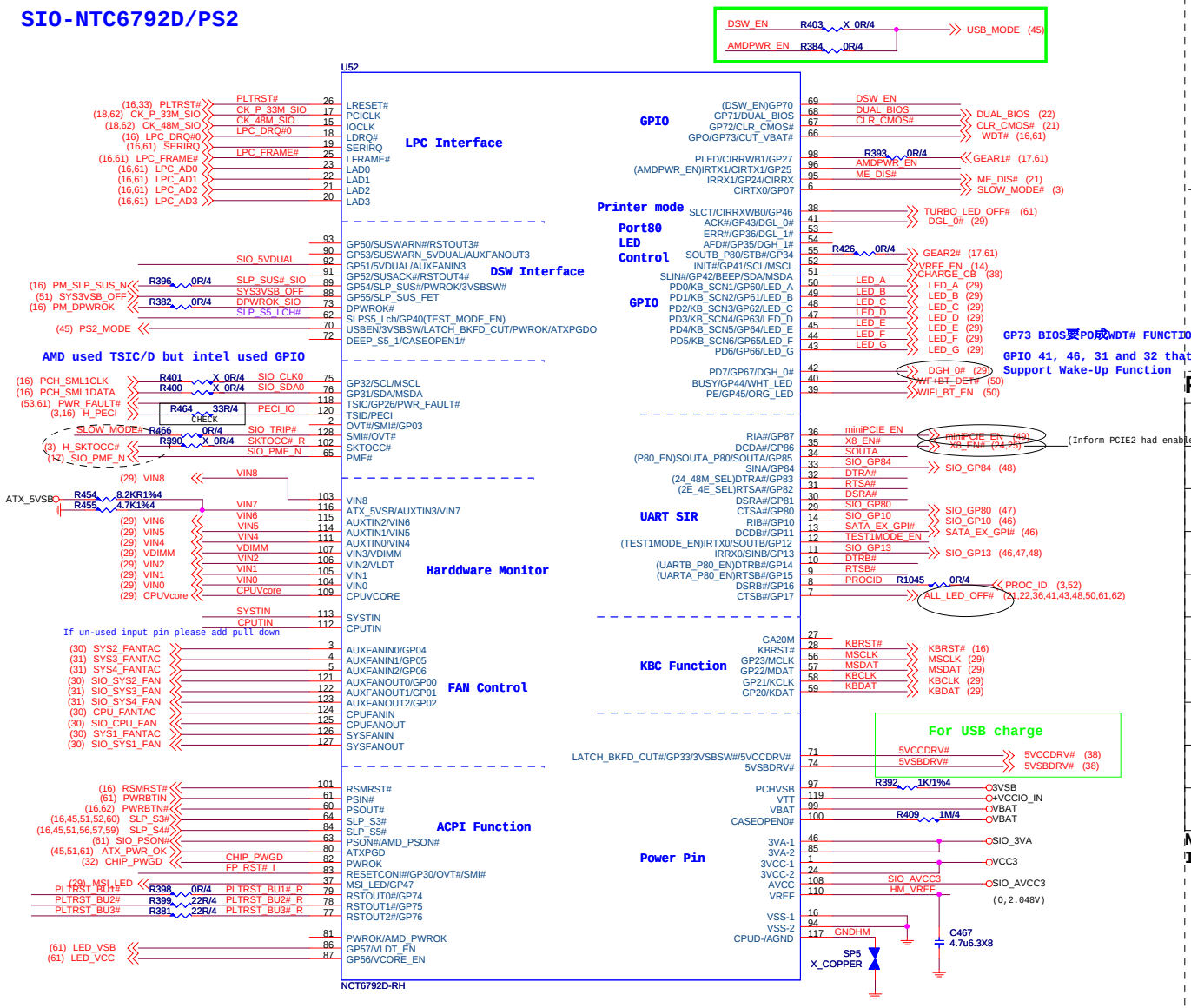
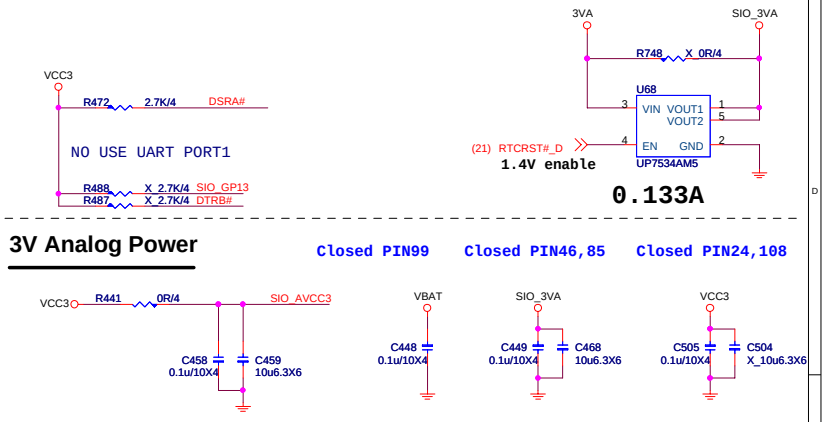
SIO-NTC6792D/PS2

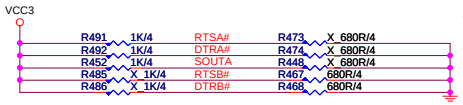


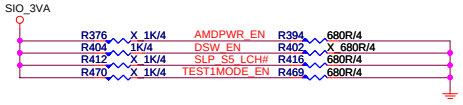


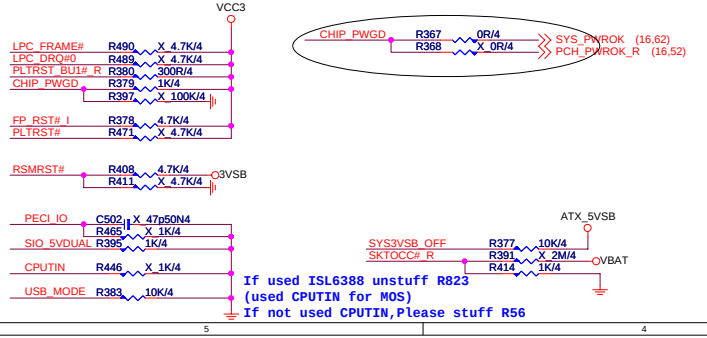
POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

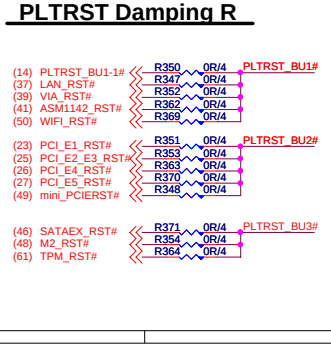
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO



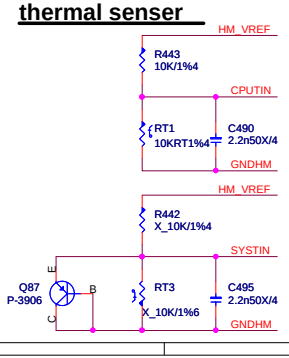


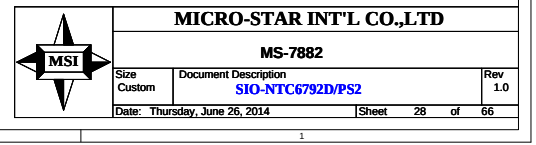


PLTRST Damping R

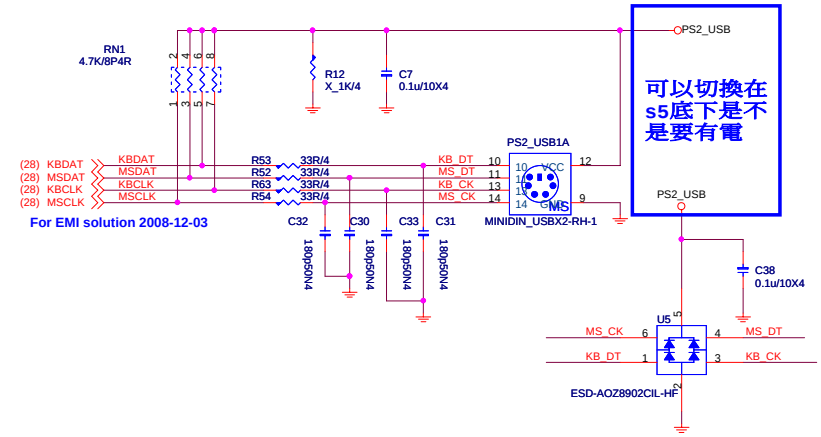


thermal senser

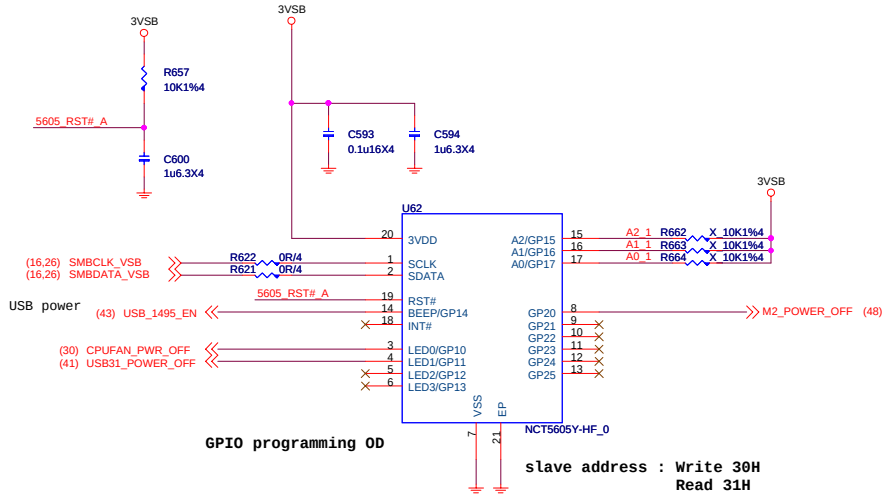




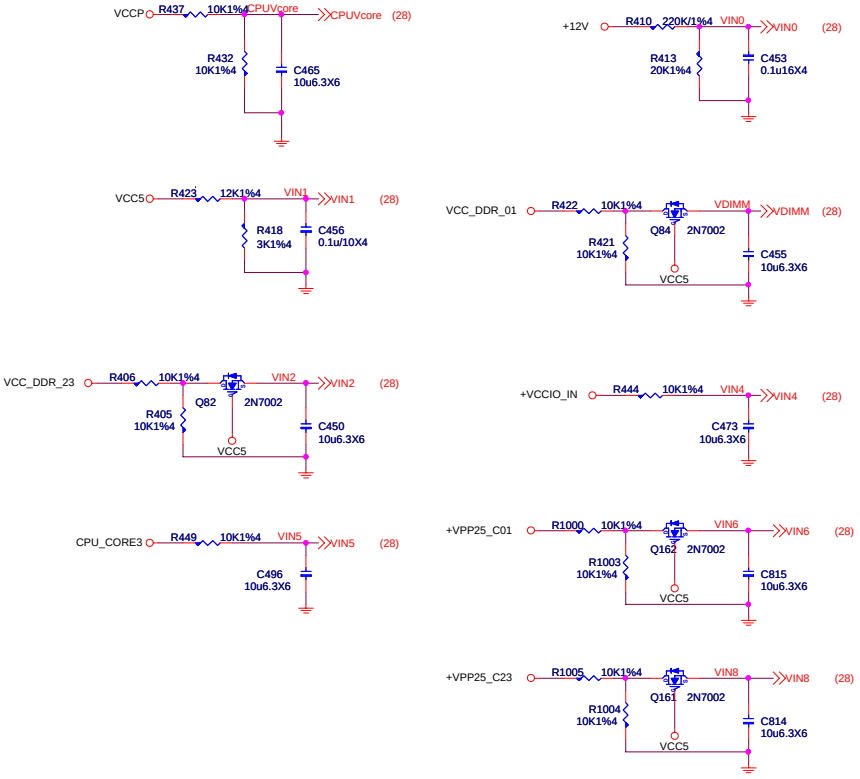
PS2 KEYBOARD & MOUSE CONNECTOR



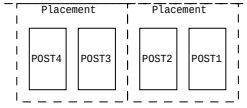
CUT POWER CHIP



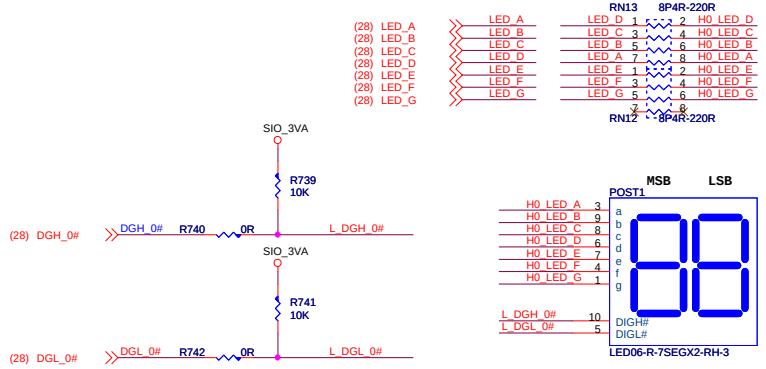
HW Monitor - Voltage



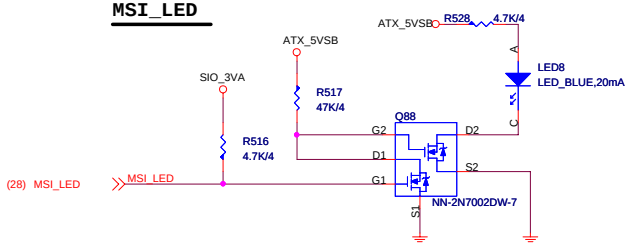
DEBUG LED



Placement一定要對
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)



MSI_LED



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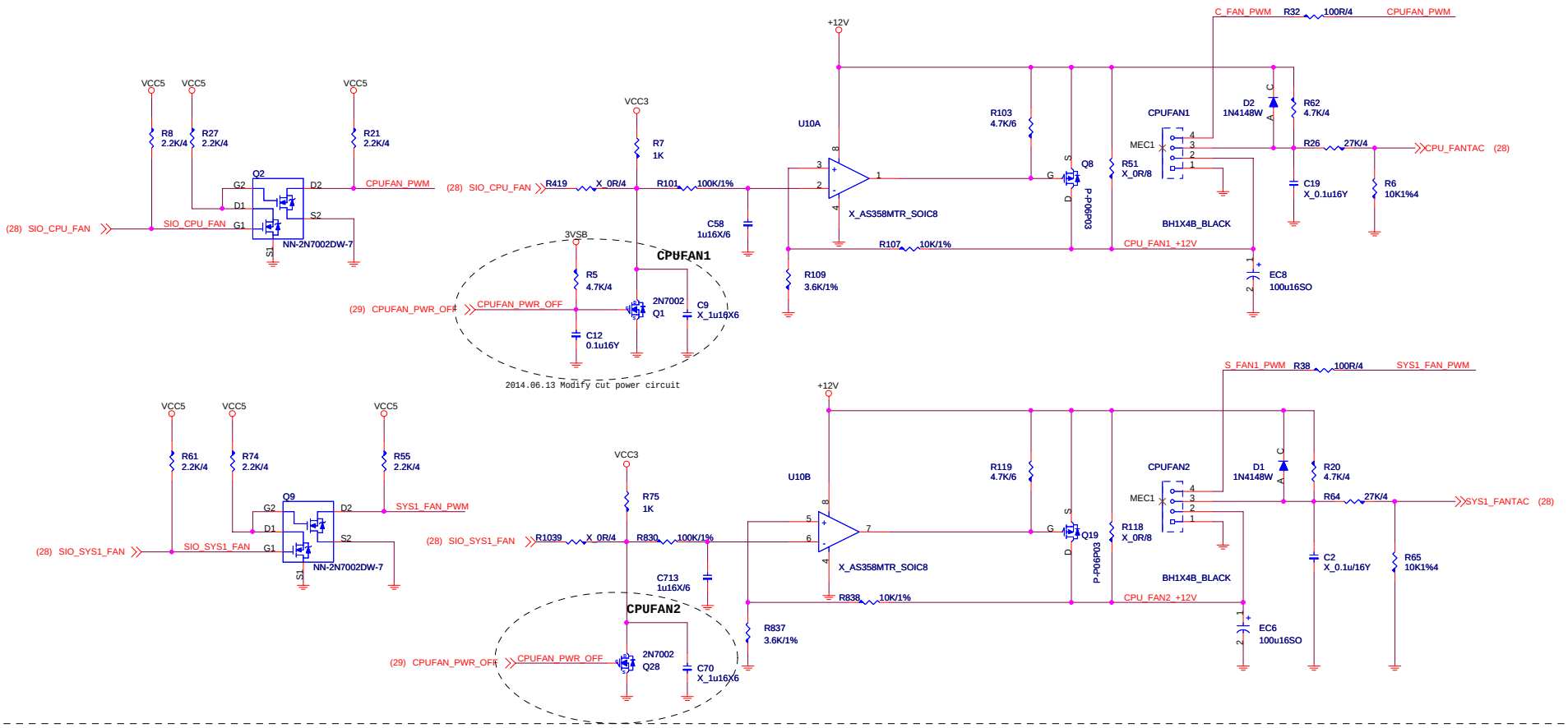
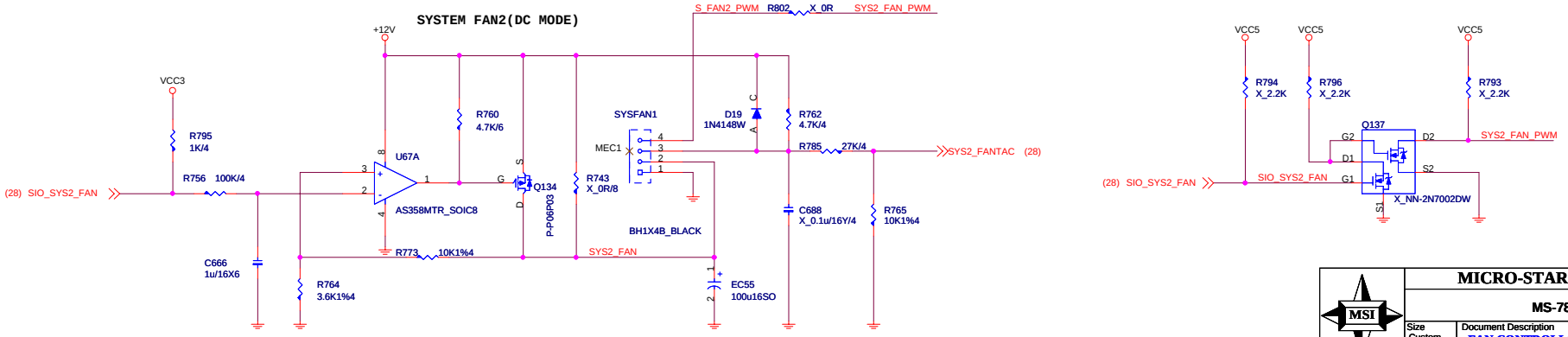
Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6792)



Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6792)



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Custom	FAN CONTROLLOR-1	1.0

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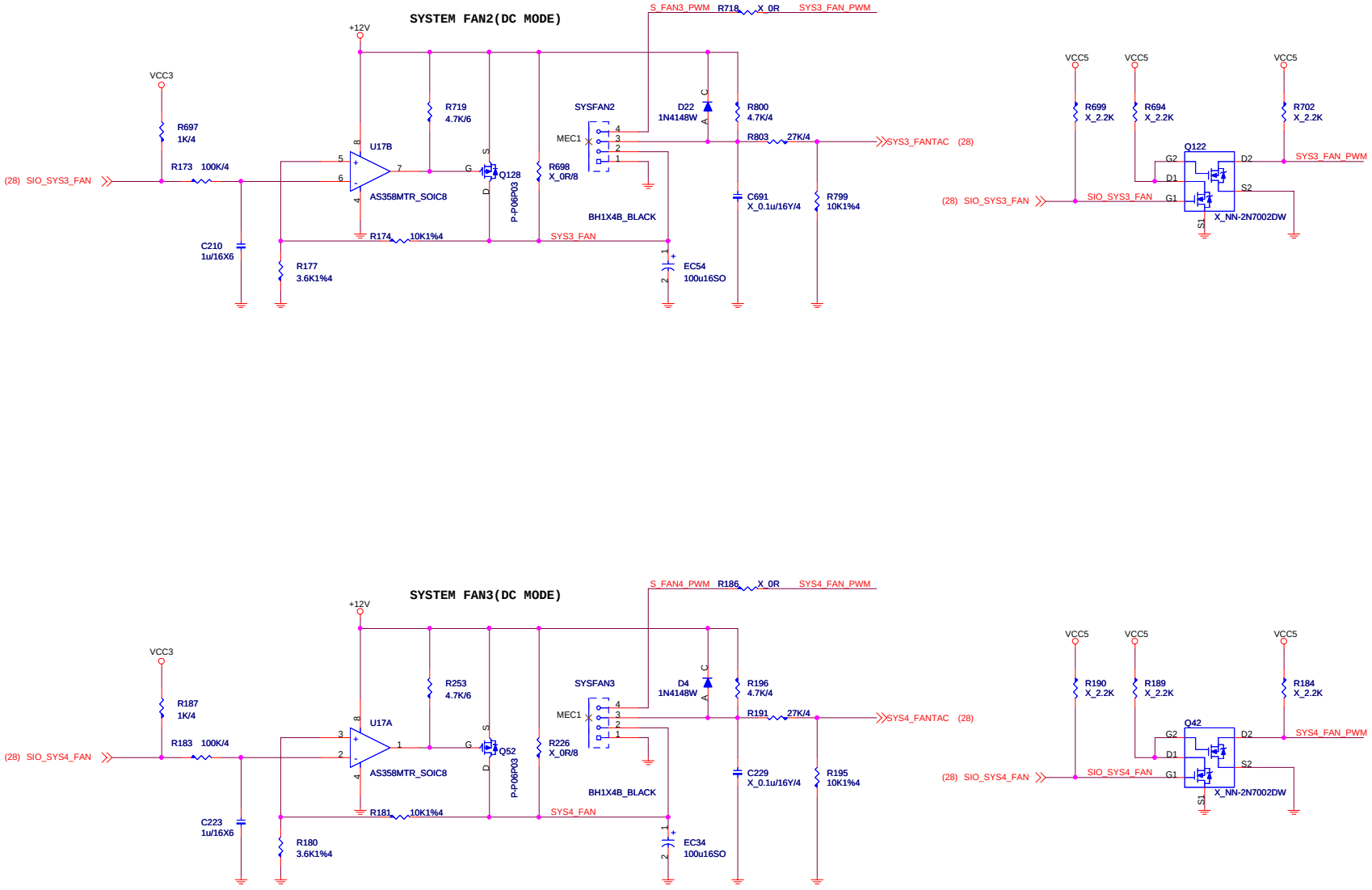
Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6792)



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	FAN CONTROLLOR-2	1.0

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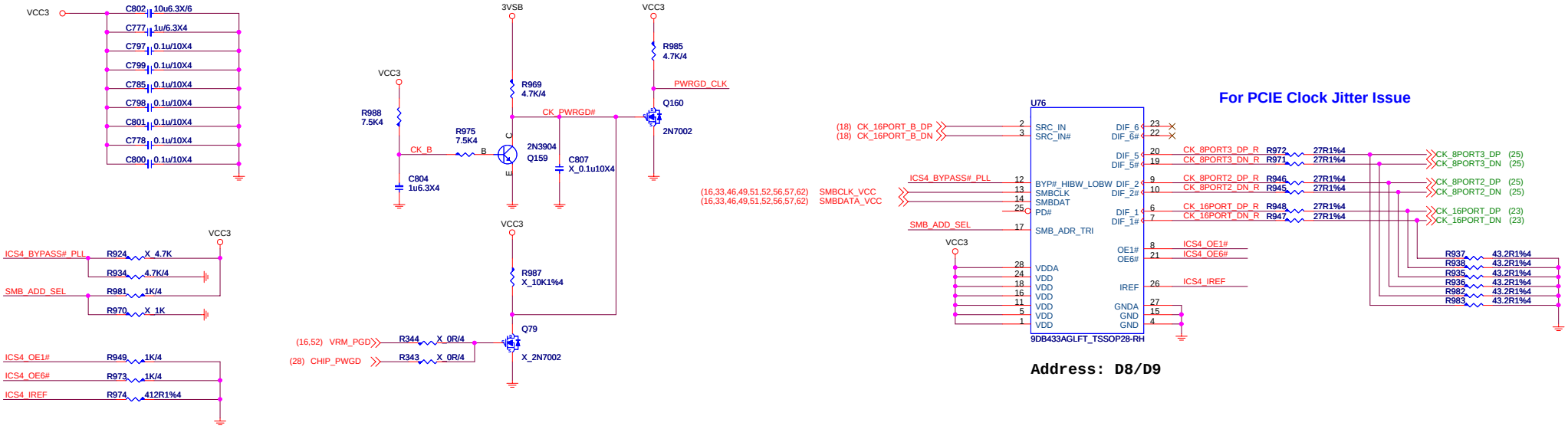
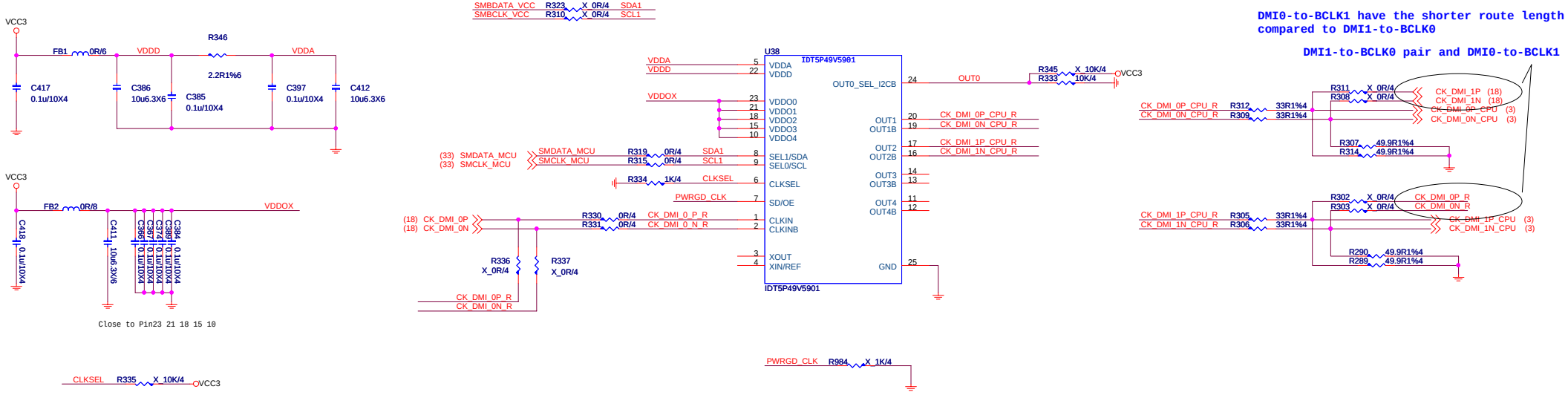
CLK Buffer_9DB433



For PCIE Clock Jitter Issue

Address: D8/D9

CLK GEN-IDT5P49V5901



DMI0-to-BCLK1 have the shorter route length compared to DMI1-to-BCLK0

DMI1-to-BCLK0 pair and DMI0-to-BCLK1

PIN:CLKSEL. Input clock select. Selects the active input reference source in manual switchover mode.
0 = XIN/REF, XOUT (default)
1 = CLKIN, CLKINB

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Size: Custom	Document Description: CLK Buffer_9DB433/IDT49325	Rev: 1.0
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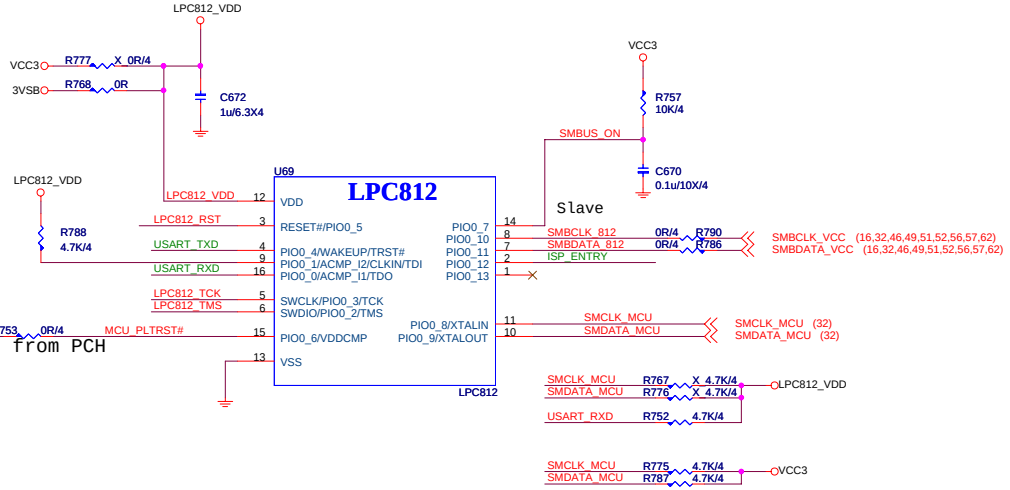
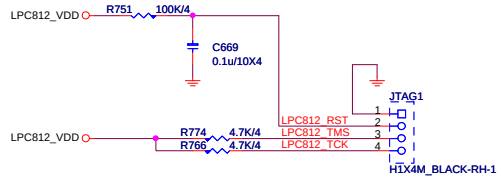
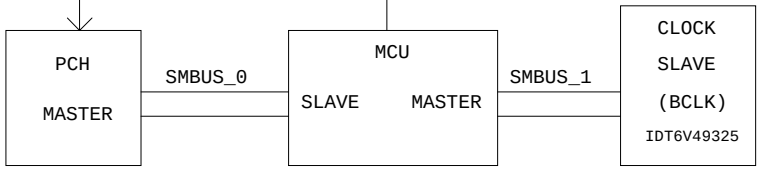
SIO 6792 , GPIO13
default low , active high



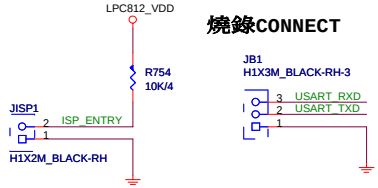
JTAG for SW DEBUG



Clear CMOS When System Boot Fail



燒錄CONNECT



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MS-7882	
Size: Custom	Document Description: MCU-LPC812
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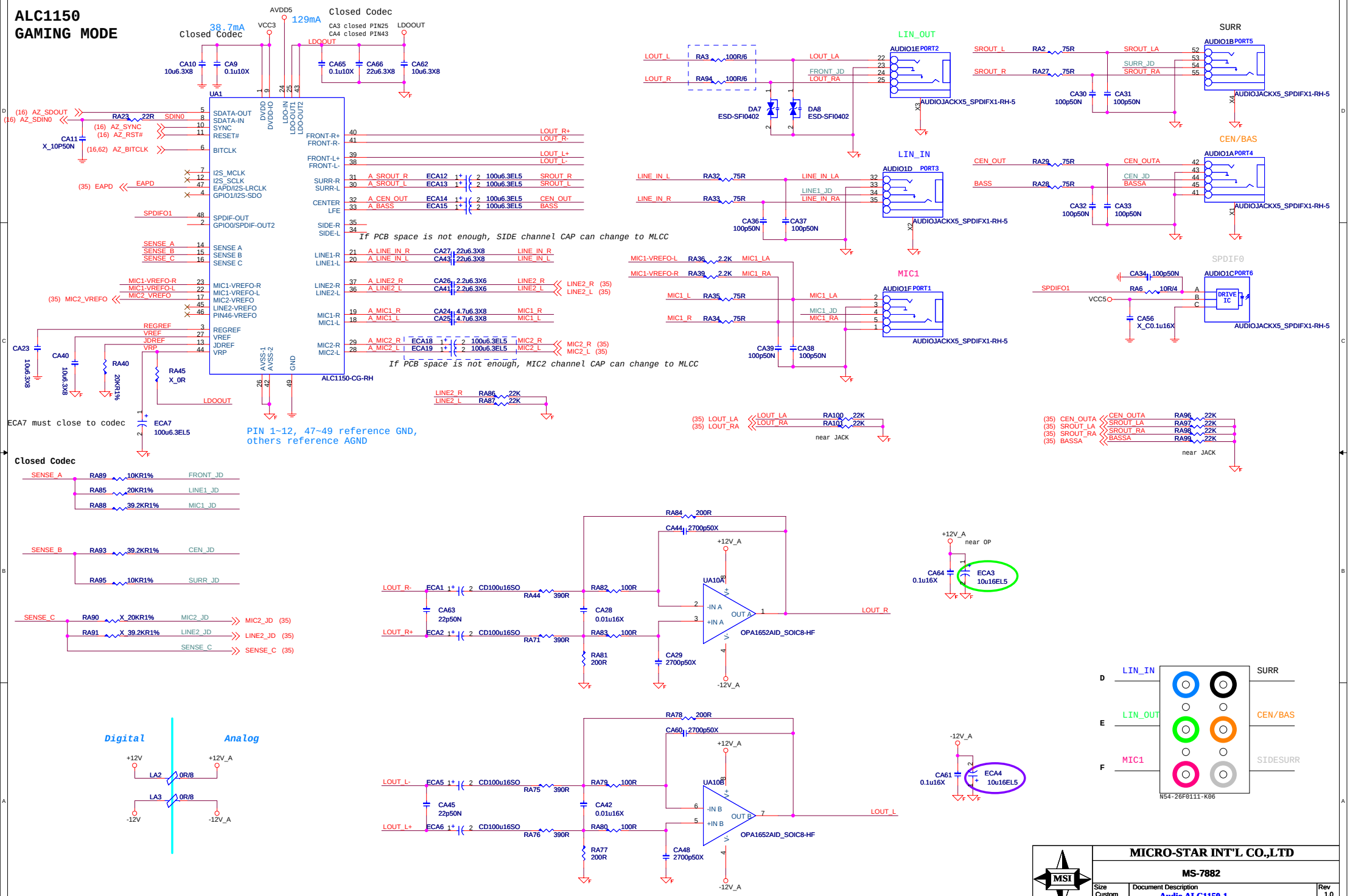
ALC1150
GAMING MODE



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MS-7882	
Size: Custom	Document Description: Audio ALC1150-1
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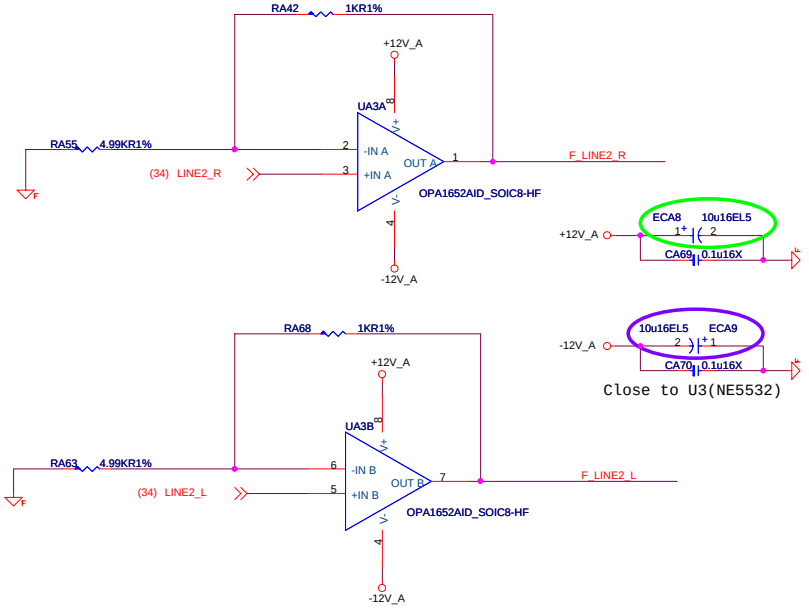
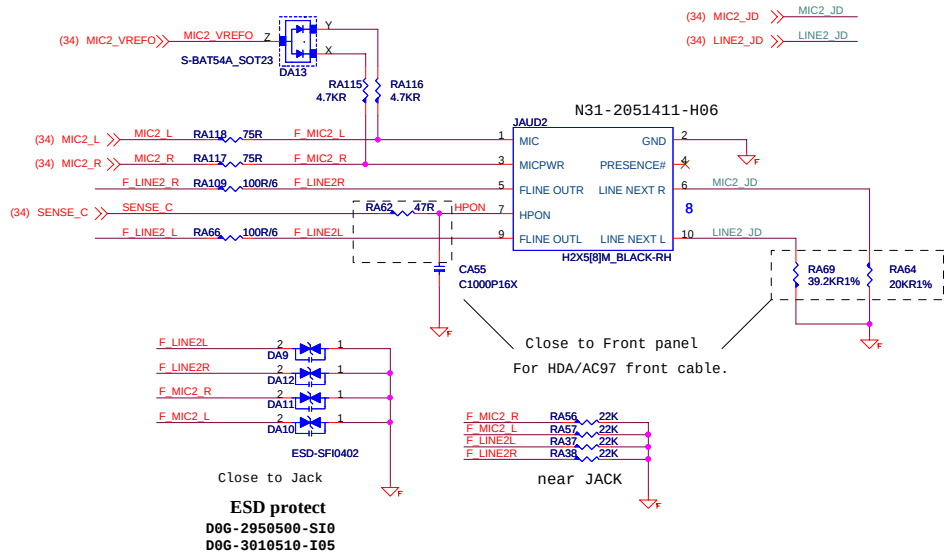
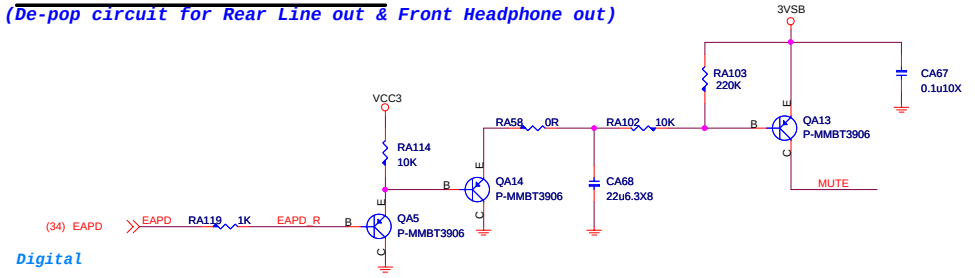
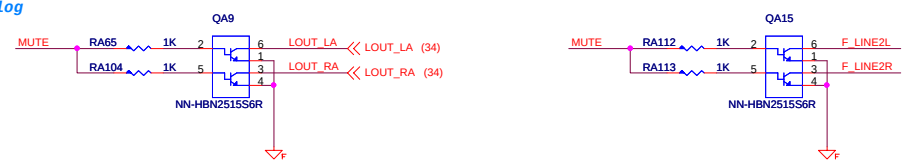




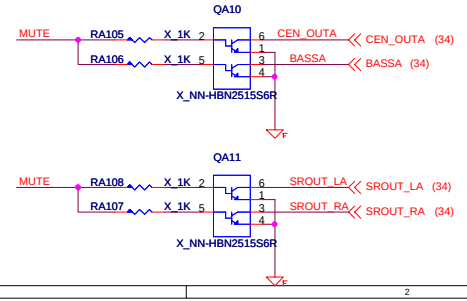
Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)

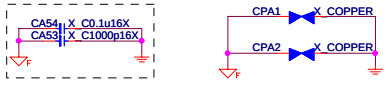




(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



EMI



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MS-7882		
Size: Custom	Document Description: Audio ALC1150-2	Rev: 1.0
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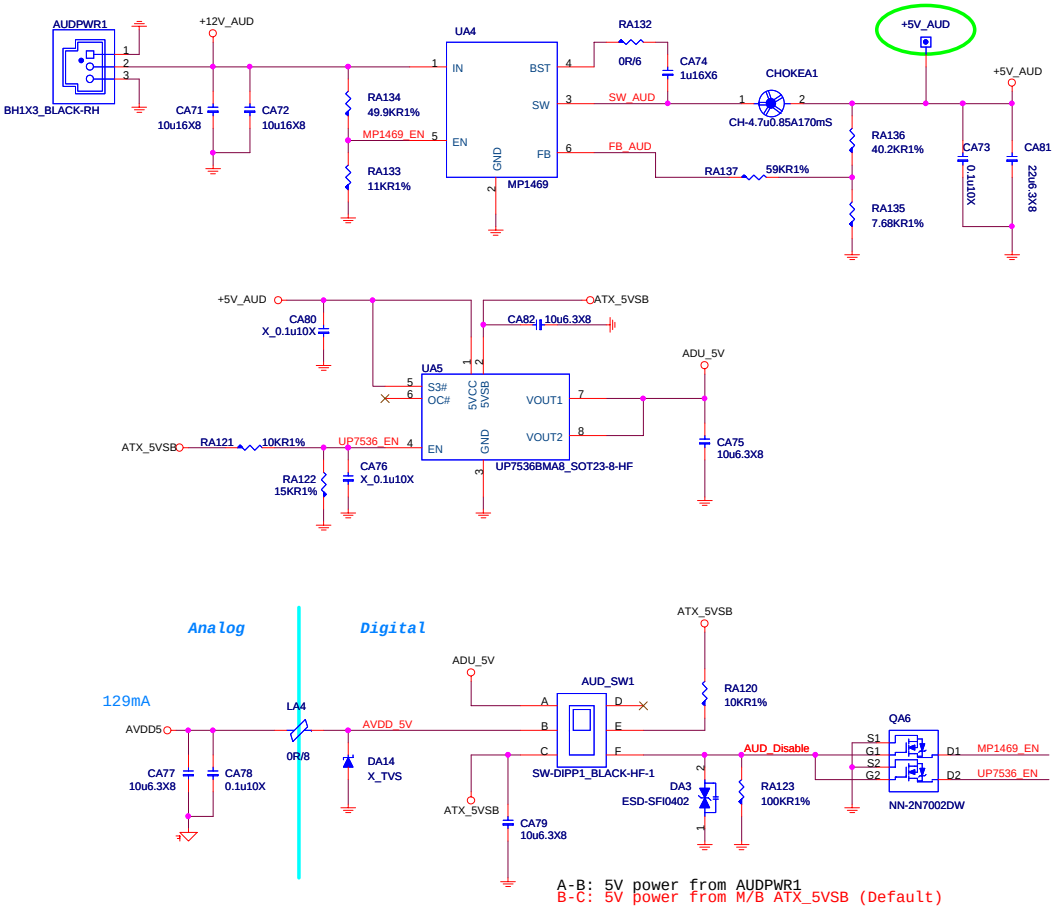
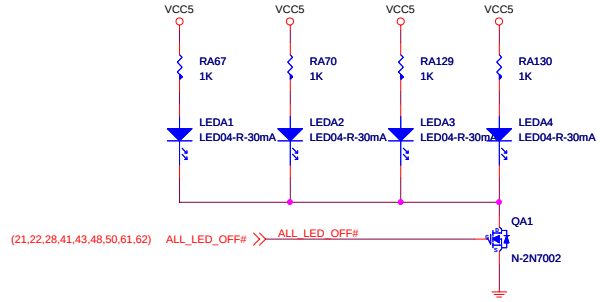
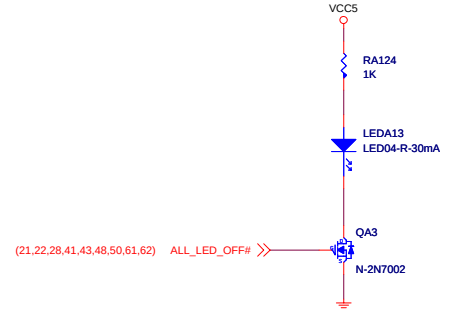
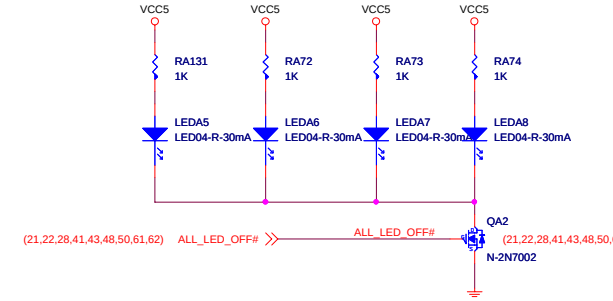
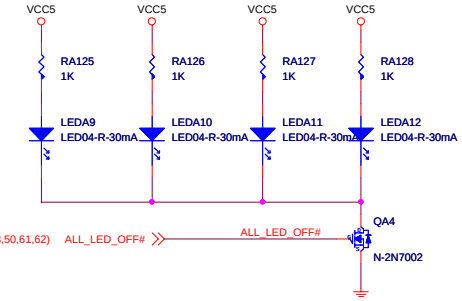


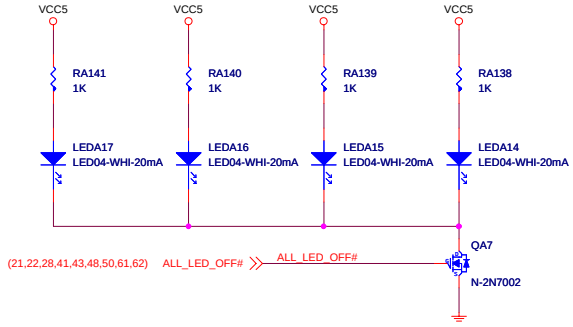
Audio moat is transparent and width 40mil

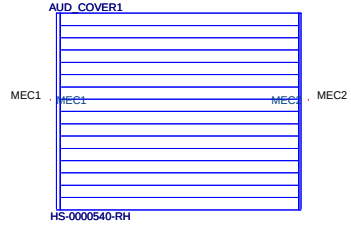












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E2205-B Giga LAN

Pull-up resister RL1 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

LED0:
1=hi core voltage(overclocking)
0=low core voltage (non-overclocking)

LED1:
1=SWR mode
0=LDO mode

LED3:
1=25MHz clock
0=48MHz clock

Reserve for strap hi

CHOKEL1:
L04-47A7310-C08
L04-47A7680-T15

LL1:
L02-3018023-C08
L02-3018023-T19

VDD33 power trace should be wider than 30mils;
AVDD33 power trace should be wider than 30mils;
VDD_IO power trace should be wider than 30mils;
VDDIO_REG power trace should be wider than 20mils;
AVDDH power trace should be wider than 20mils;
AVDDL power traces should be wider than 20mils.
DVDDL power traces should be wider than 20mils.

10:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRIO13.

D0G-1020510-I05
D0G-8010510-SI0

D0G-05A0300-I14
D0G-06A050C-A68

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MS-7882	
Size: Custom	Document Description: LAN RTL8111G/8106E
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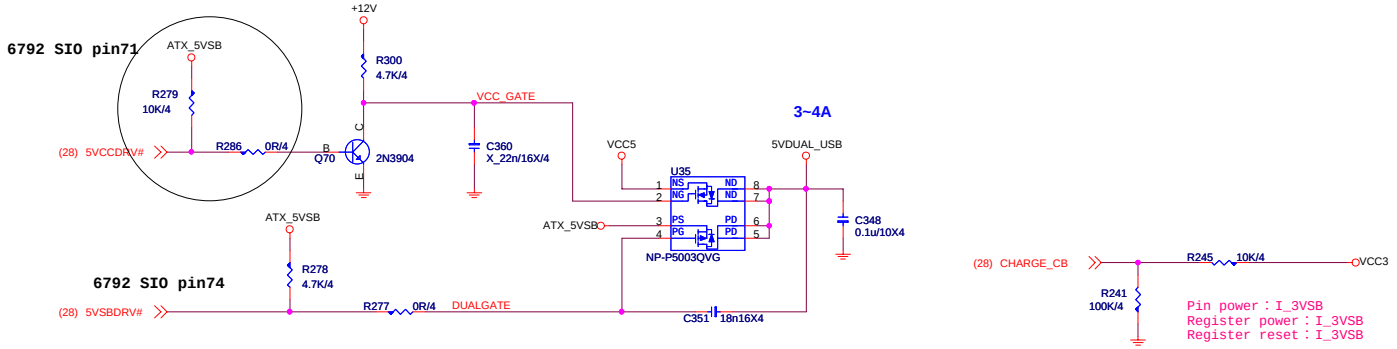
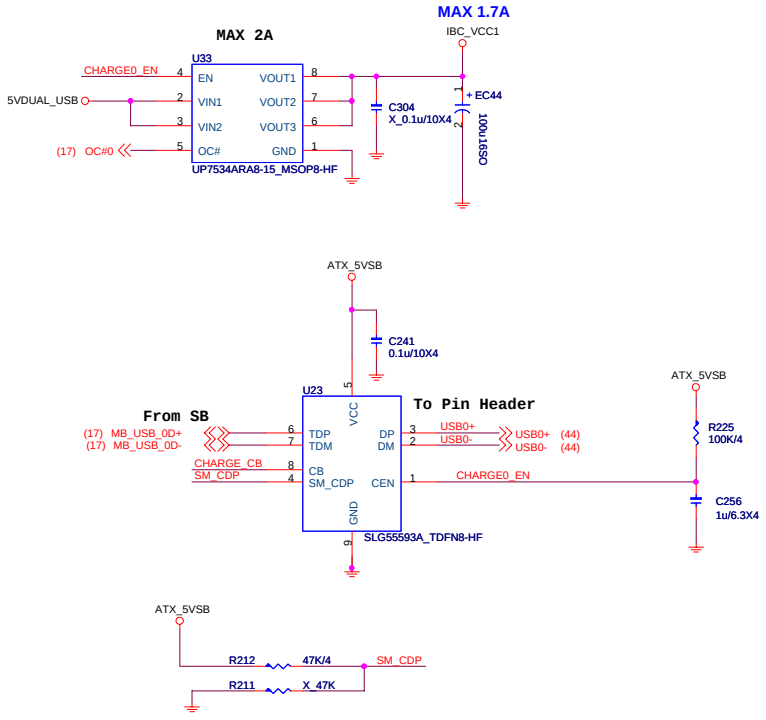
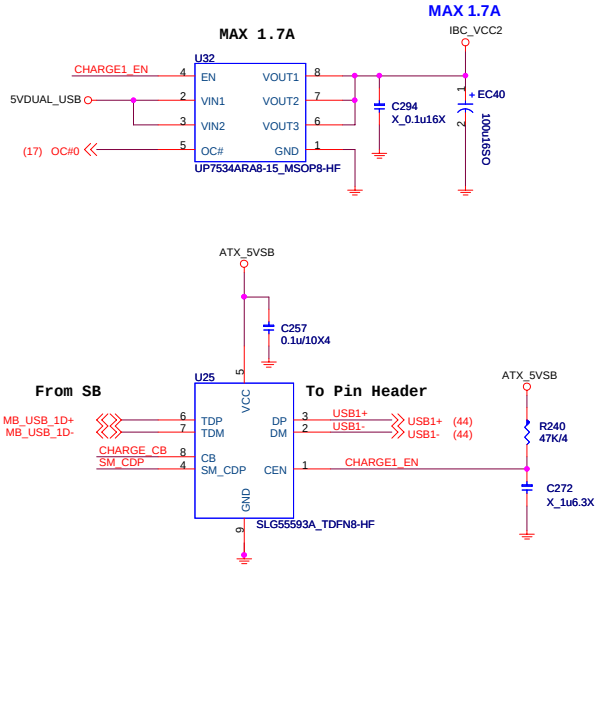
5VDUAL_USB



USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging



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MS-7882		
Size: Custom	Document Description: USB CHARGE_SLG55593A	Rev: 1.0
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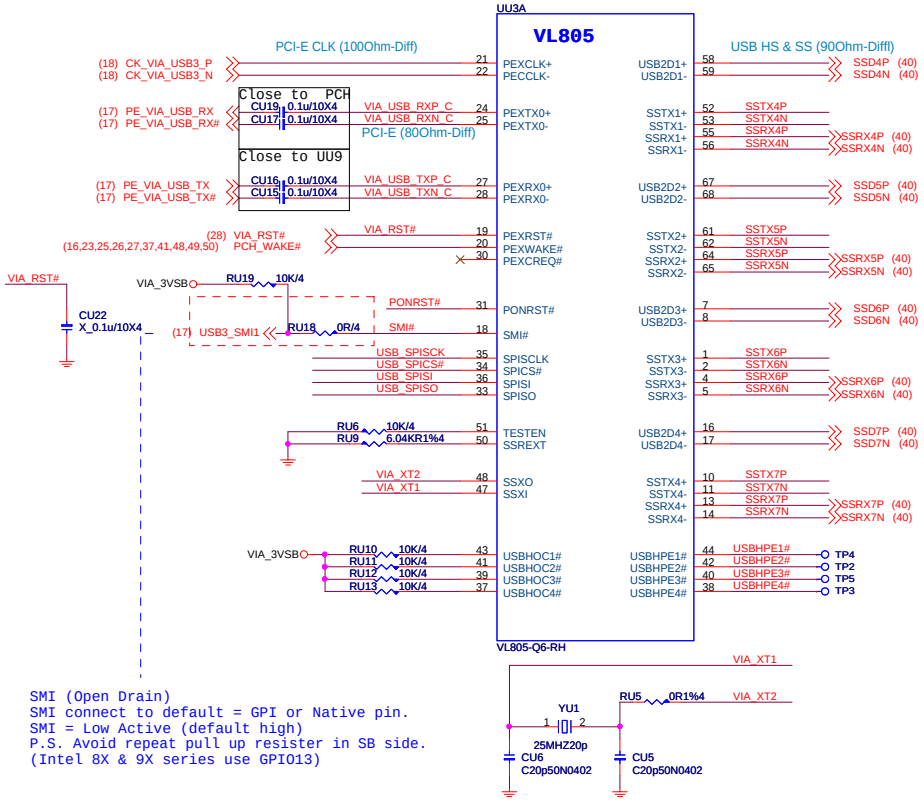
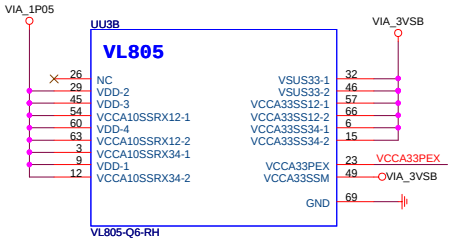
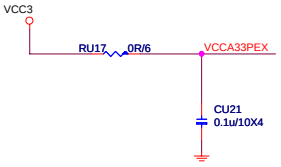
VL805-USB30-4PORT

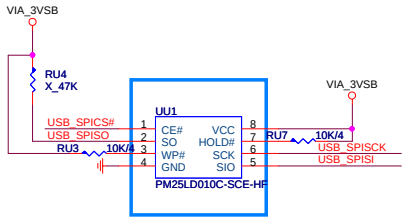


SMI (Open Drain)
SMI connect to default = GPI or Native pin.
SMI = Low Active (default high)
P.S. Avoid repeat pull up resister in SB side.
(Intel 8X & 9X series use GPIO13)

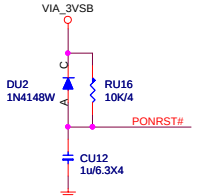




EEPROM

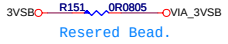


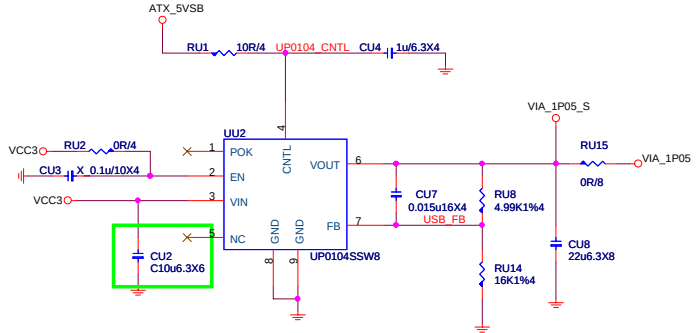
Change to 1M.

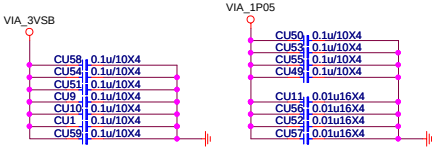


1.05V core Power

Max Power disspation: (3.3 V-1.05V)*0.247A=0.55575W
VIA Core Power: VIA_1P05 247mA







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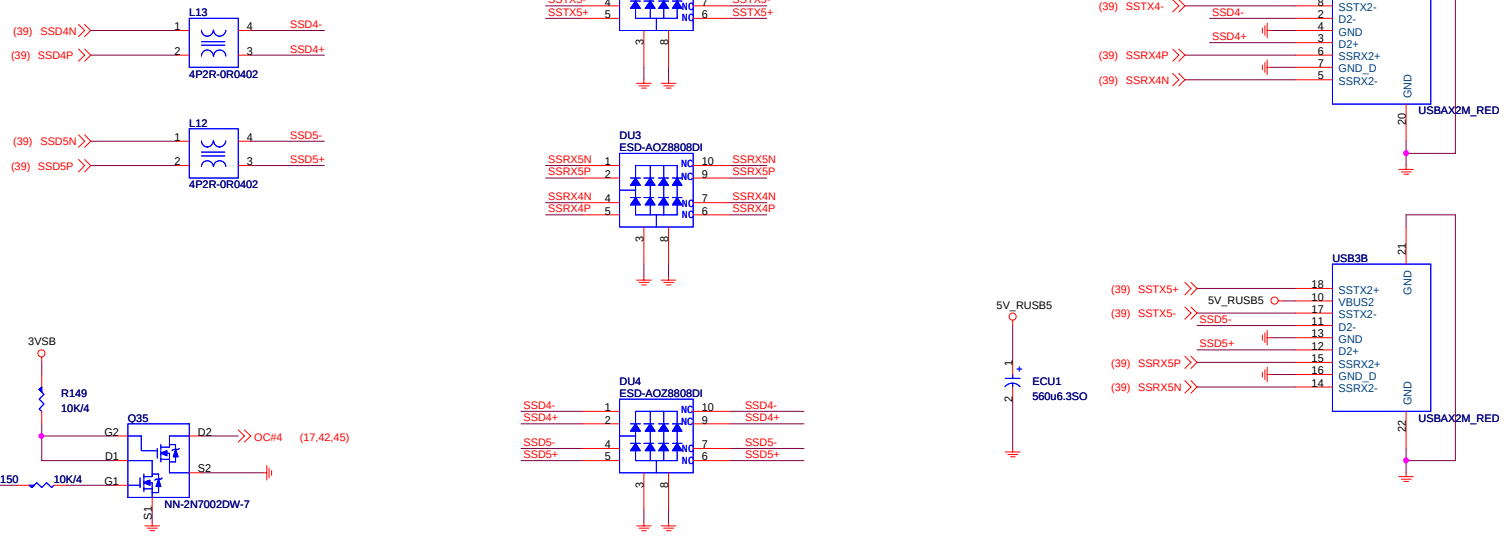
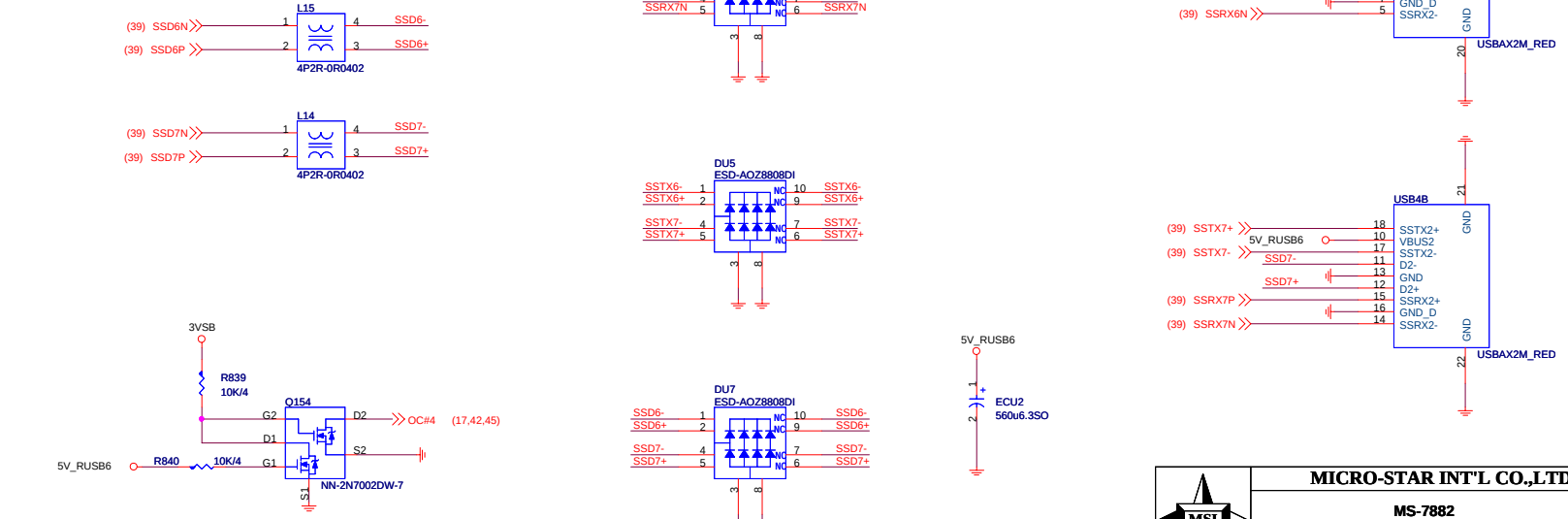
VL805-USB30-4PORT CONN

Rear I/O

Close to Connector





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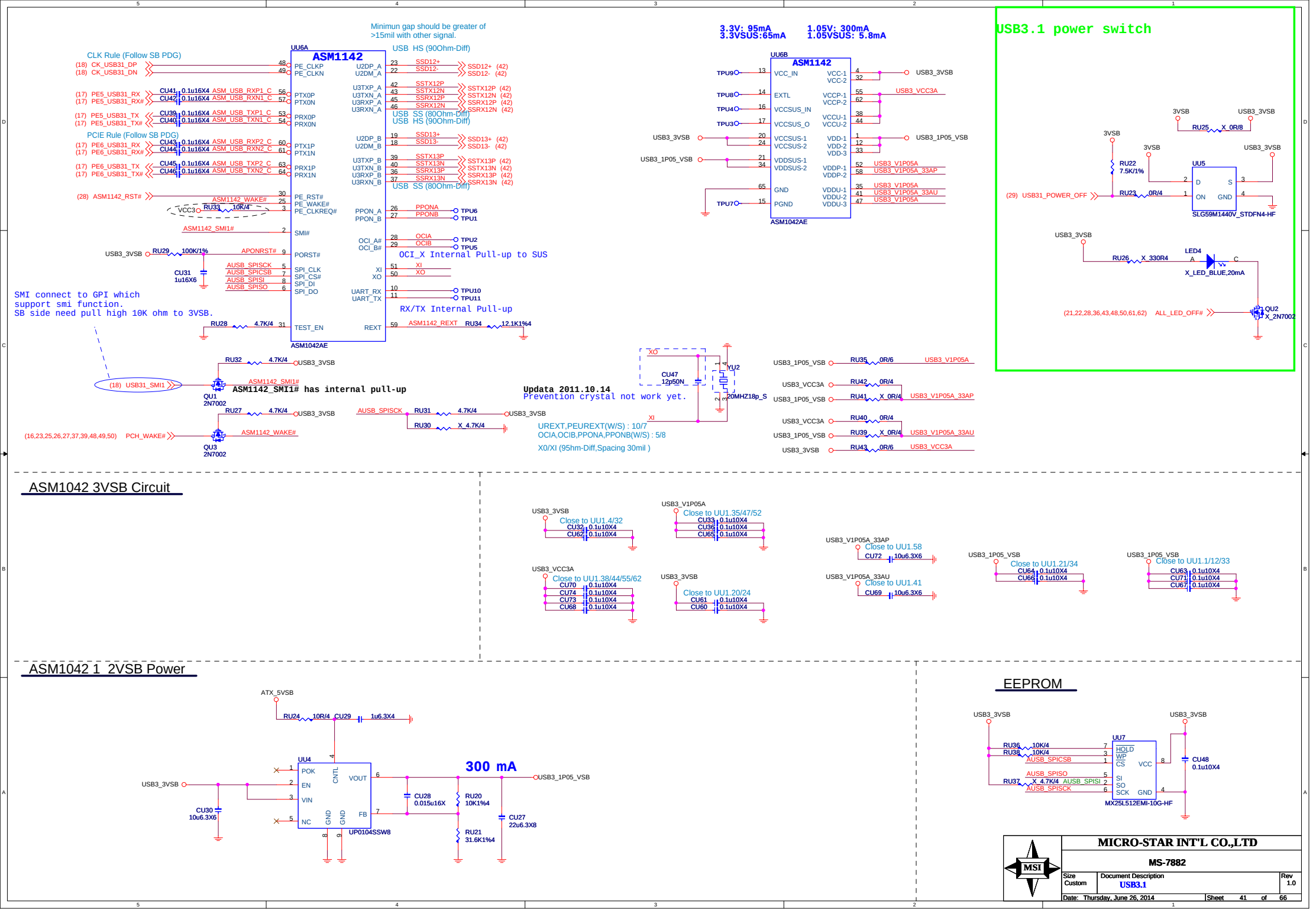

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Size: Custom	Document Description: USB3.1
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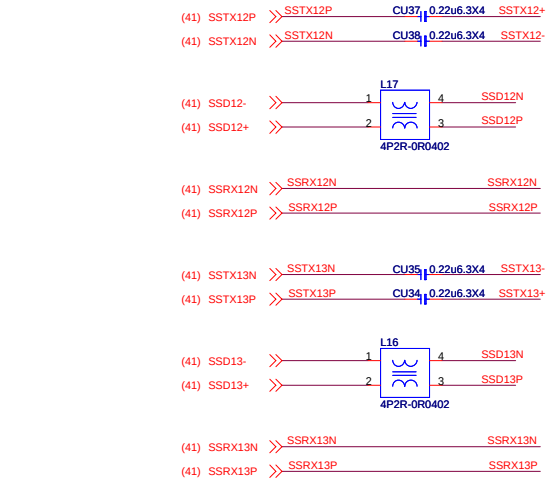
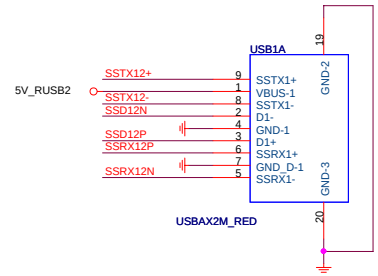
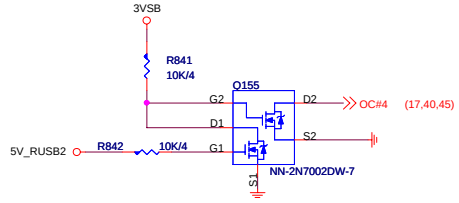
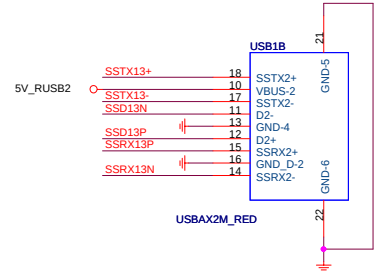


Rear USB3 CONN

Important~~
If USB3.0 signal conect to front pin header,
please must less than 0.6 inch,short trace
has better eye diagram with some bad fly cable by SI customer.

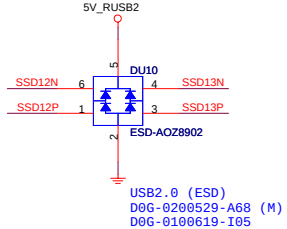


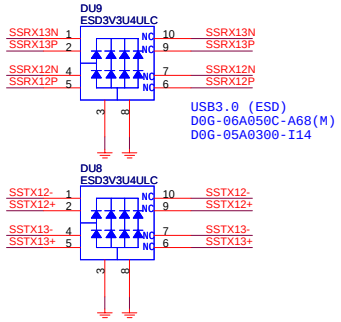


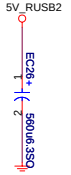


ESD Protection

NEAR CONNECTOR







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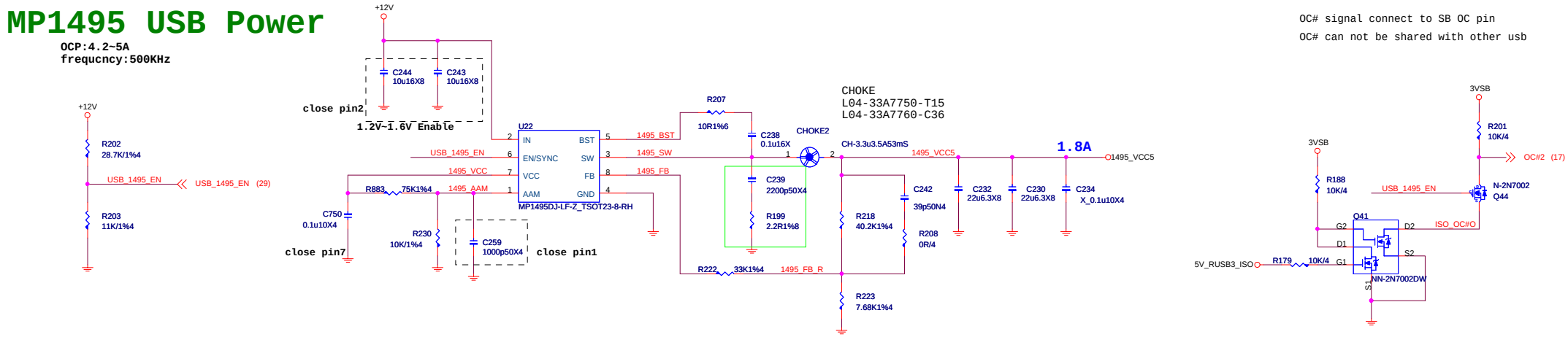
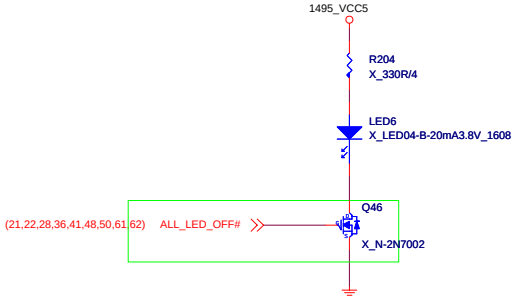
MP1495 USB Power

OCP:4.2~5A
frequcncy:500KHz

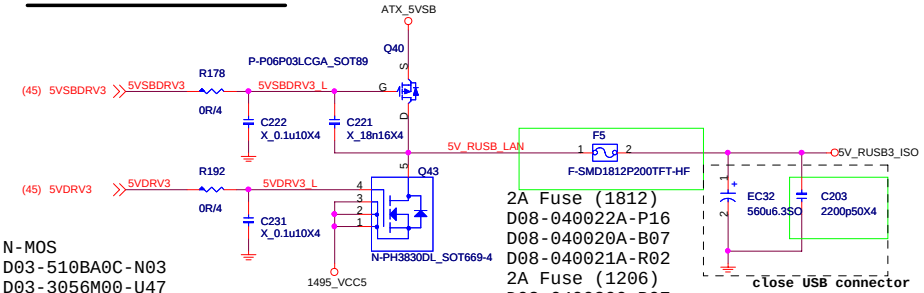
OC# signal connect to SB OC pin
OC# can not be shared with other usb



TO:NCT6792D GP17



REAR USB PORT POWER



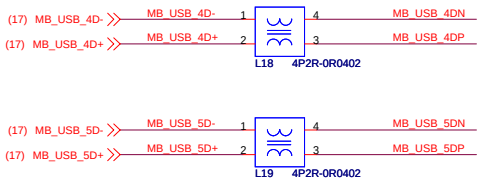
P-MOS
D03-06P0319-N03

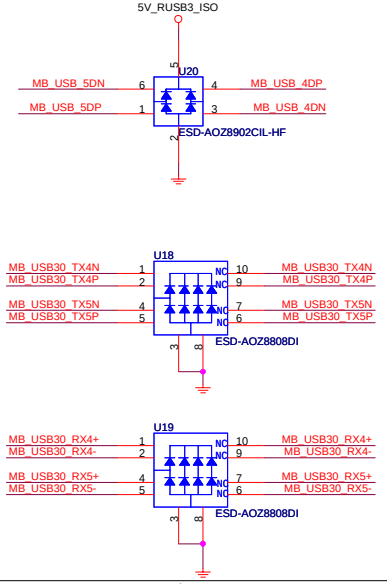
N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

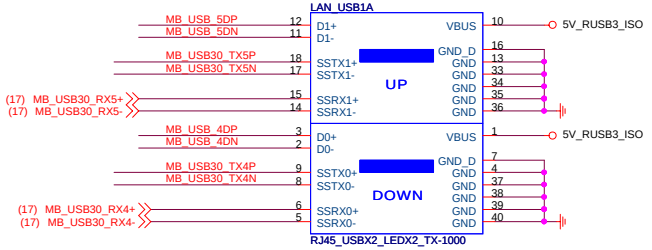
2A Fuse (1812)
D08-040022A-P16
D08-040020A-B07
D08-040021A-R02
2A Fuse (1206)
D08-0400800-B07
D08-0400900-L07

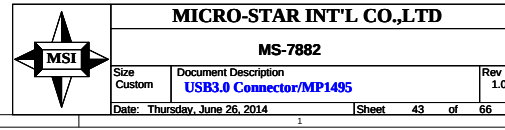
(D03-P500303-N03 N/P MOS can replace Q1/Q2)

USB3.0 Connector



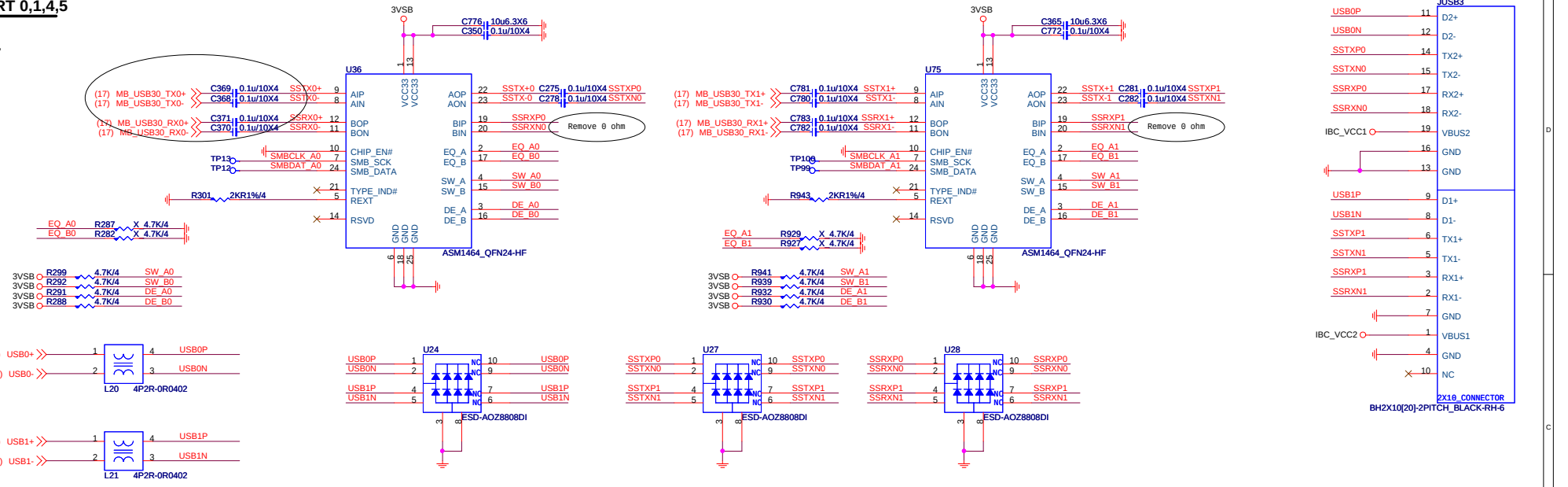






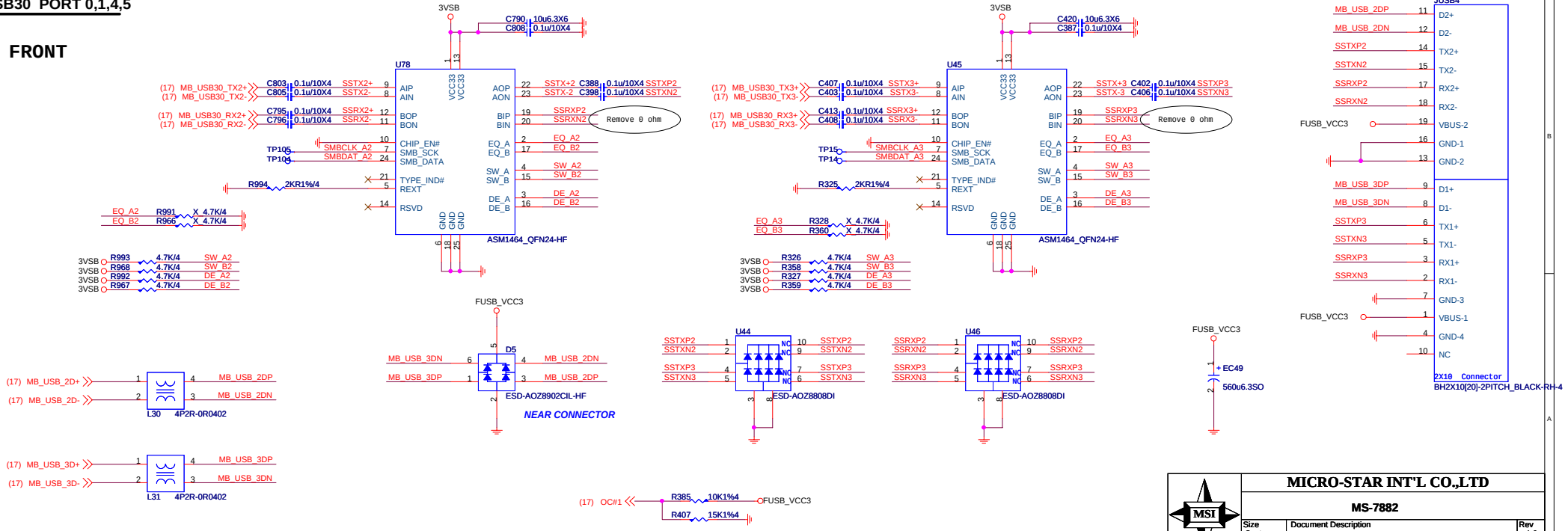
FRONT USB30 PORT 0,1,4,5

USB3.0 FRONT



FRONT USB30 PORT 0,1,4,5

USB3.0 FRONT



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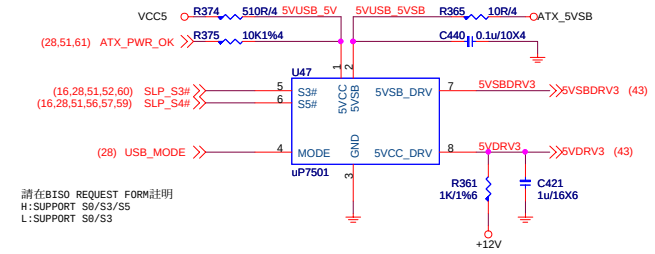
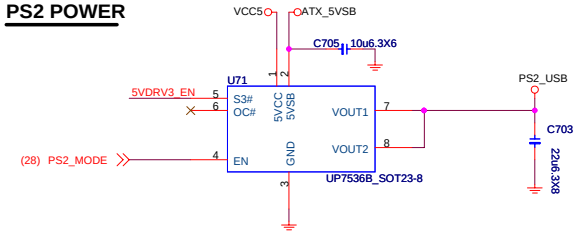
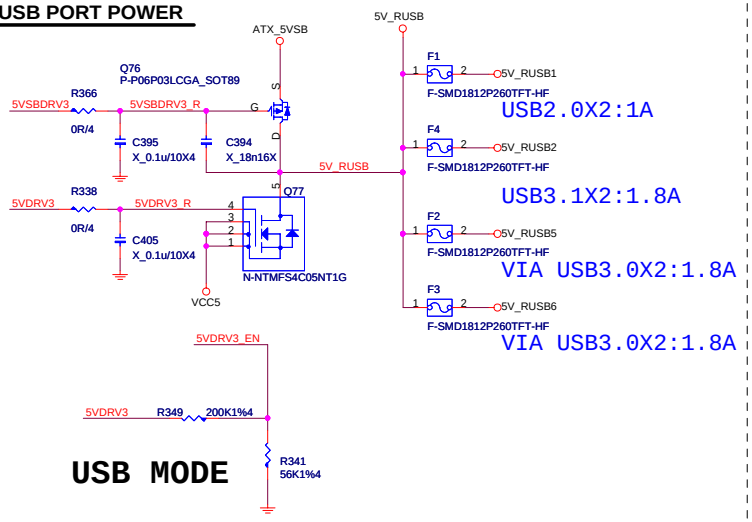
USB POWER



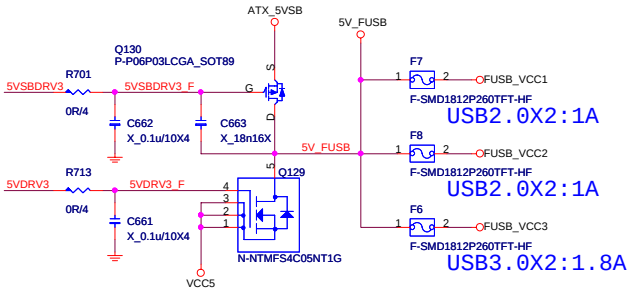
PS2 POWER



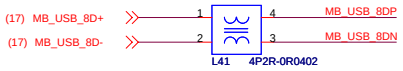
REAR USB PORT POWER

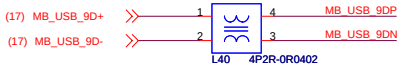


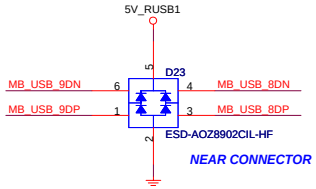
Front USB PORT POWER

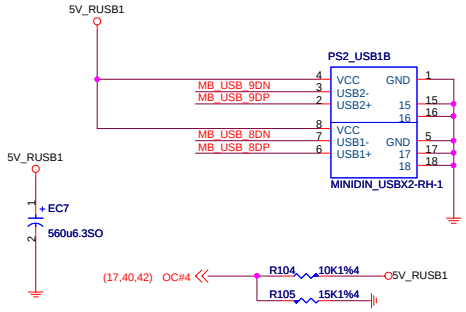


REAR USB PORT 8,9 (With PS2)

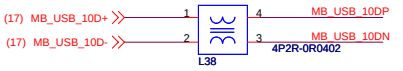


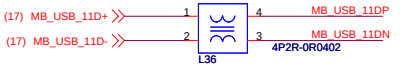


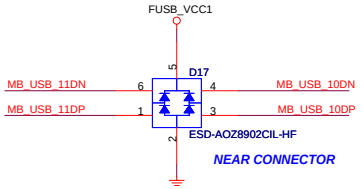


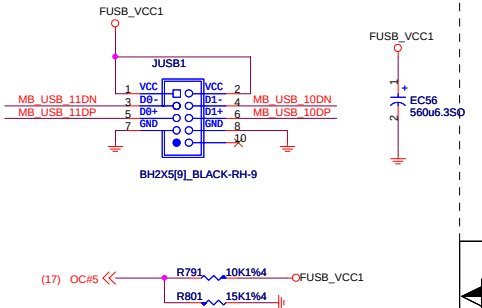


FRONT USB PORT 10.11

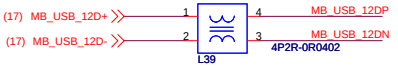


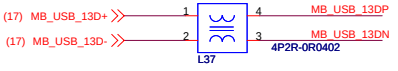


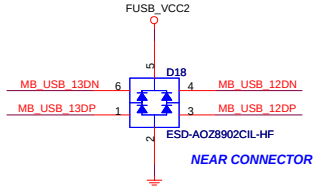


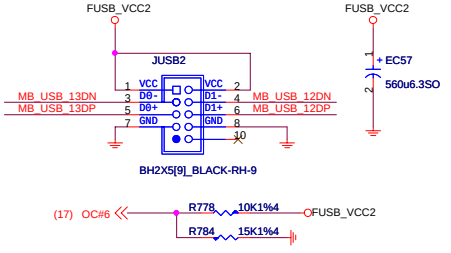


FRONT USB PORT 12,13









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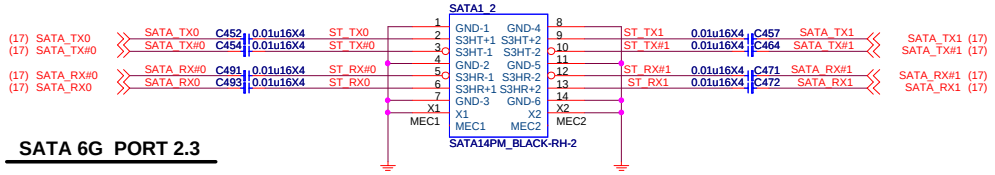
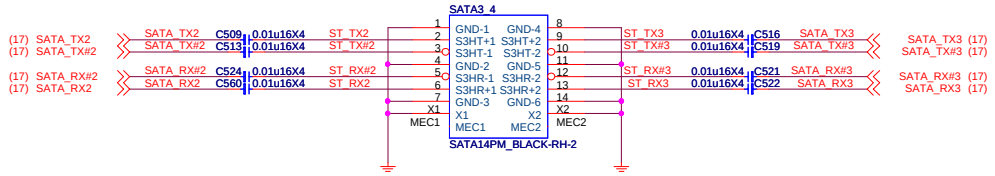
SATA & PCIE Re-driver

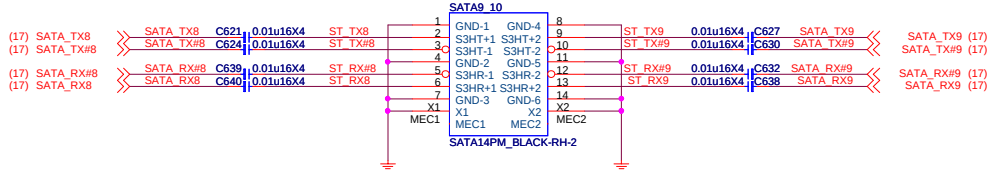
SATA 6G PORT 0.1



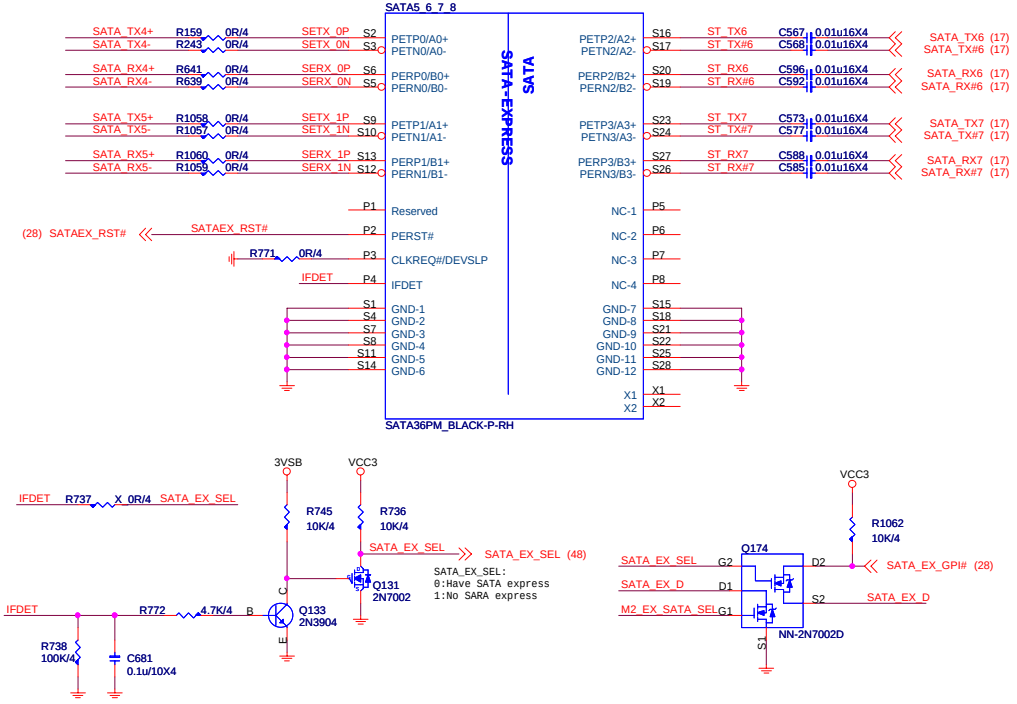
SATA 6G PORT 2.3

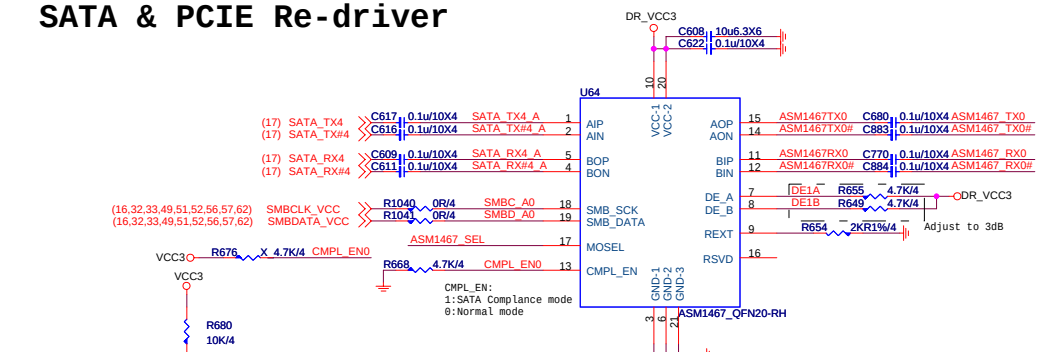


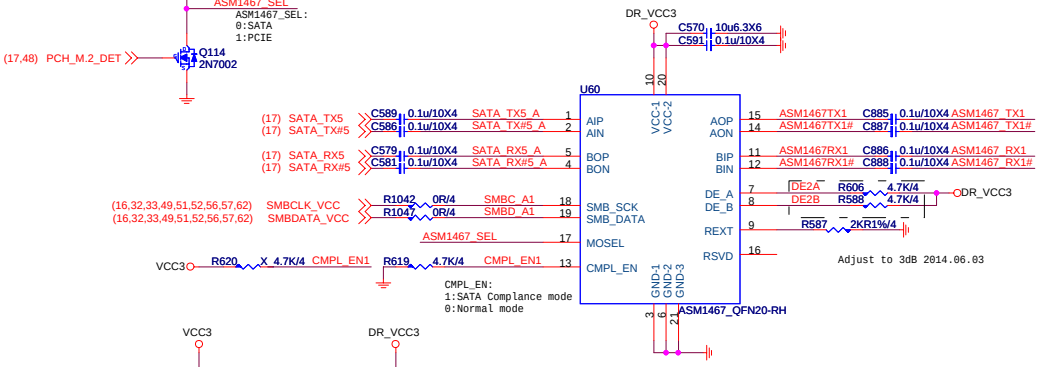
SATA 6G PORT 8.9

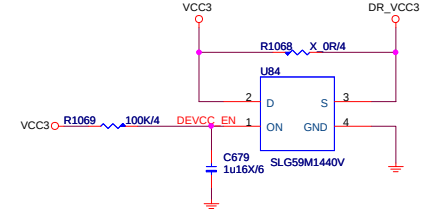


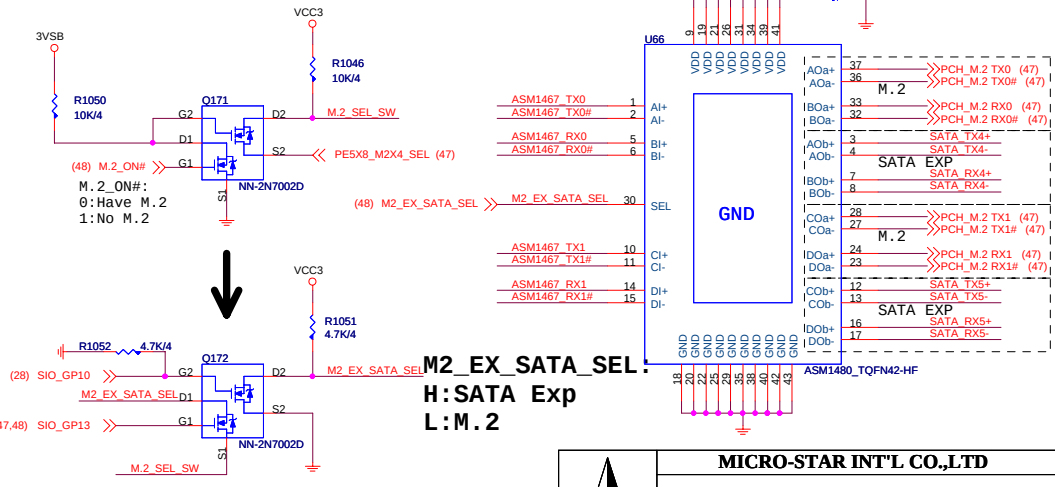
SATA 6G PORT 4.5.6.7 & SATA Express











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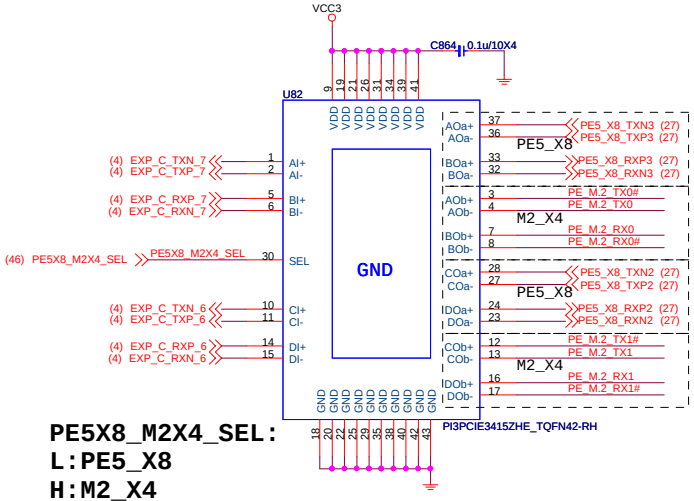
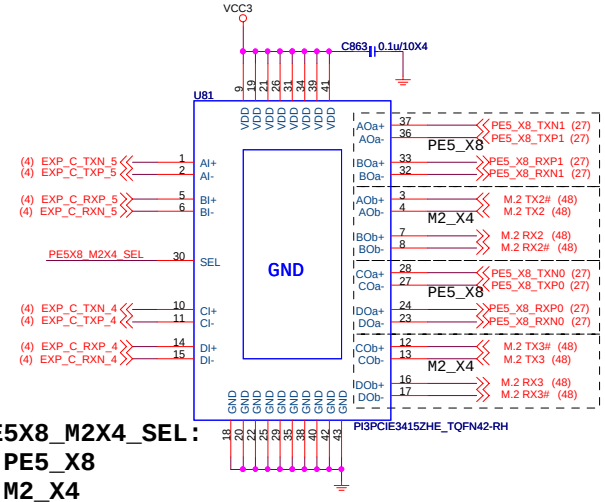
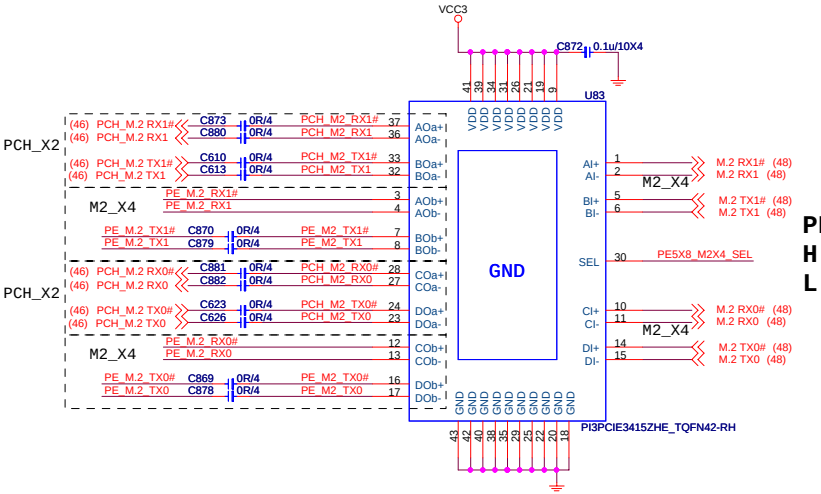
PCIE5 & M.2 Switch



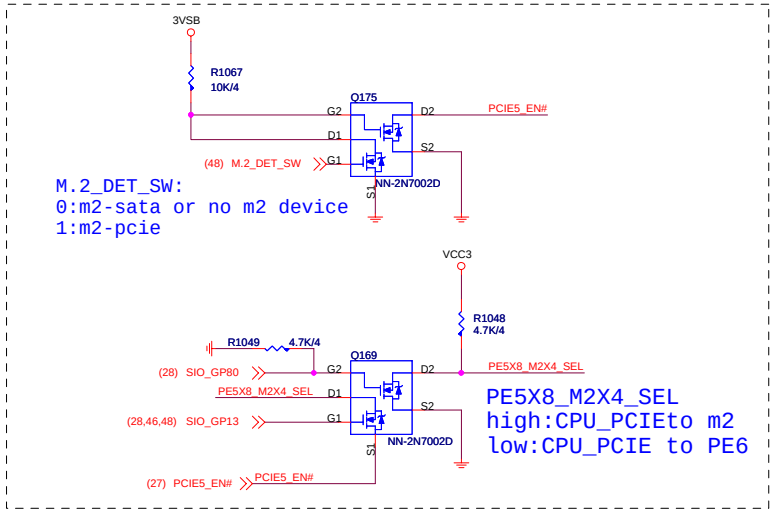
PE5X8_M2X4_SEL:
L:PE5_X8
H:M2_X4



PE5X8_M2X4_SEL:
L:PE5_X8
H:M2_X4



PE5X8_M2X4_SEL:
H:PCIE from CPU
L:PCIE from PCH



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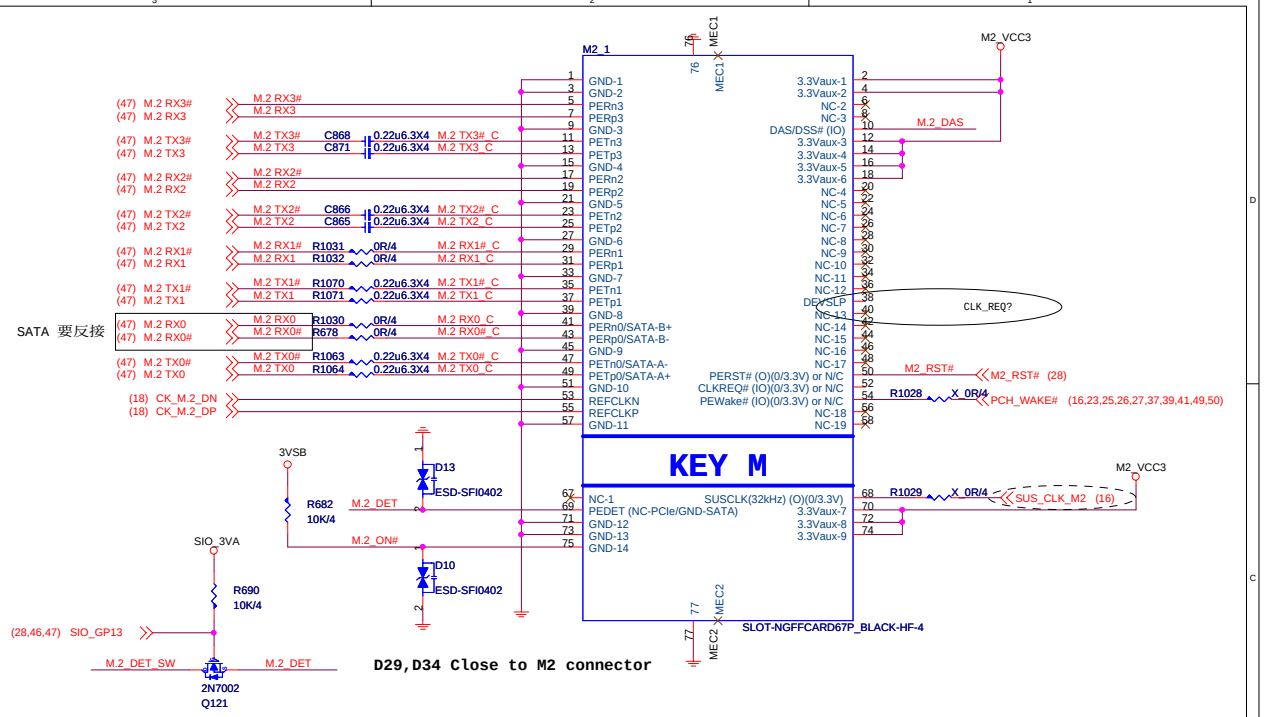
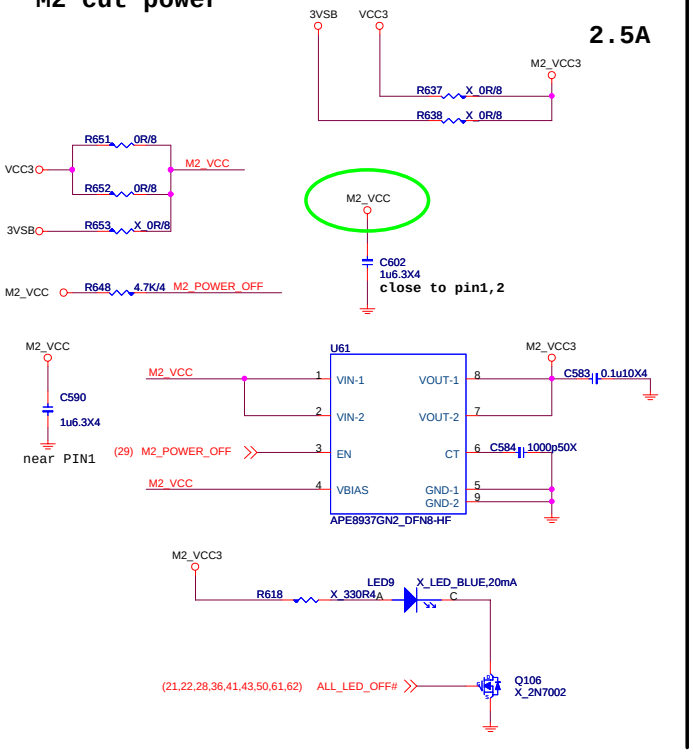
BIOS_MODE

SIO_GP10	SIO_GP80	SIO_GP84	SIO_GP13	Mode
1	0	1:PCIE 0:SATA	0	M2-PCH
X	1	X	0	PCIEX8
X	0	X	0	M2-X4
0	X	1:PCIE 0:SATA	X	SATA EXpress
GPI(:0)	GPI(:0)	GPI(:0)	1	AUTO

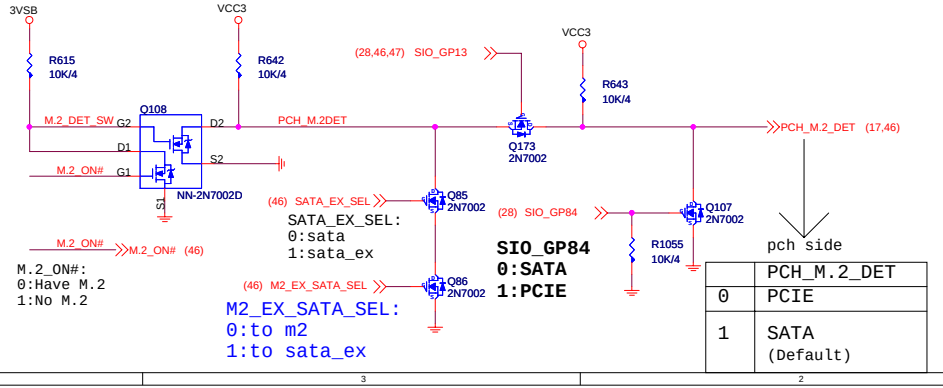


M2 cut power

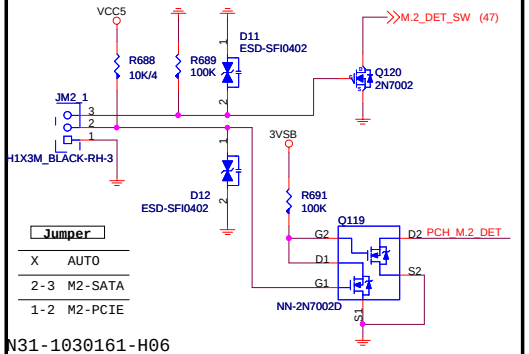
2.5A

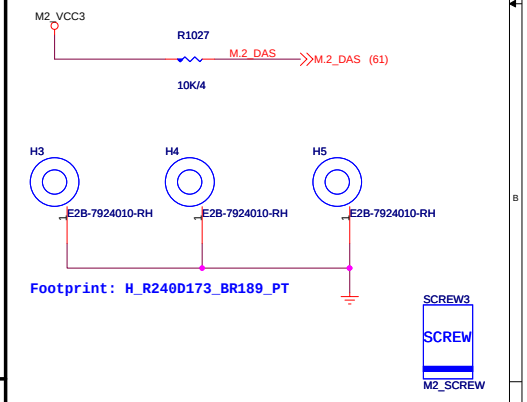


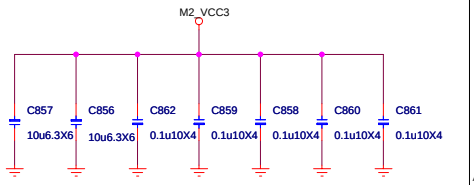
SATA & PCIE SWITCH



	PCH_M.2_DET
0	PCIE
1	SATA (Default)







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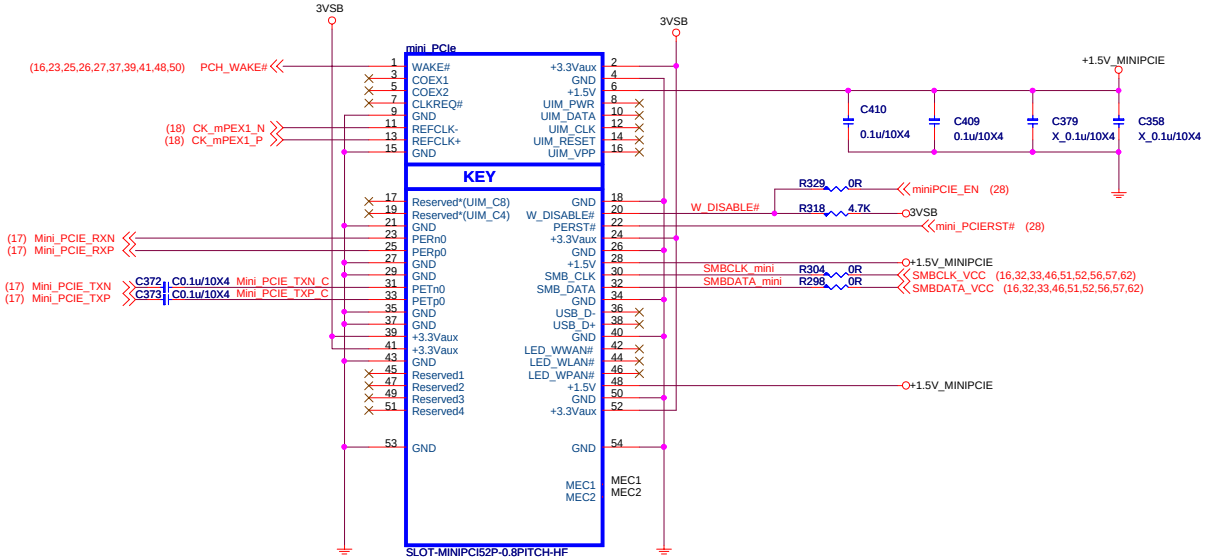
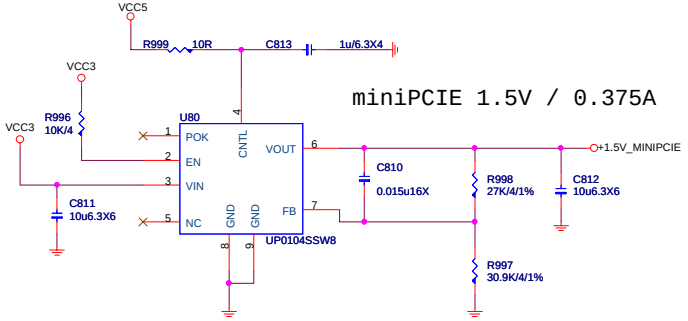
mini PCIE





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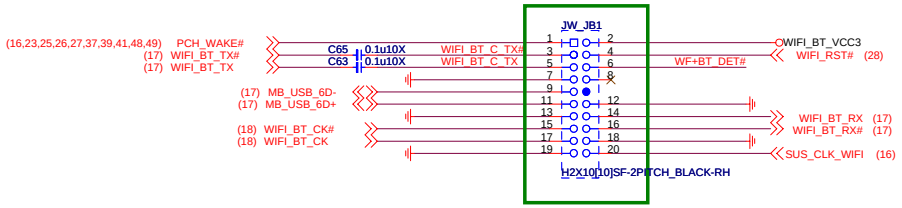
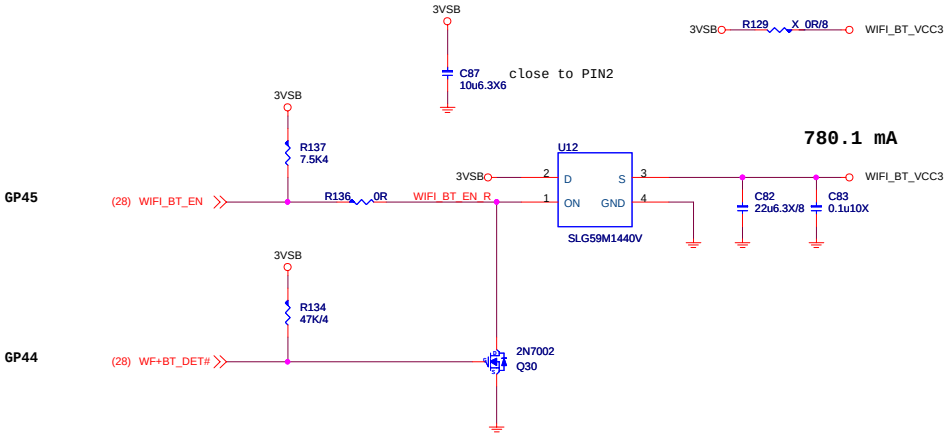
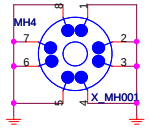
WIFI + Buletooth

2014.02.17

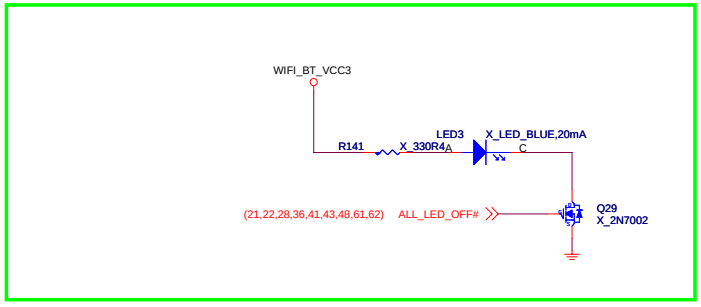


2014.04.02 Update footprint





2014.04.02 Update footprint



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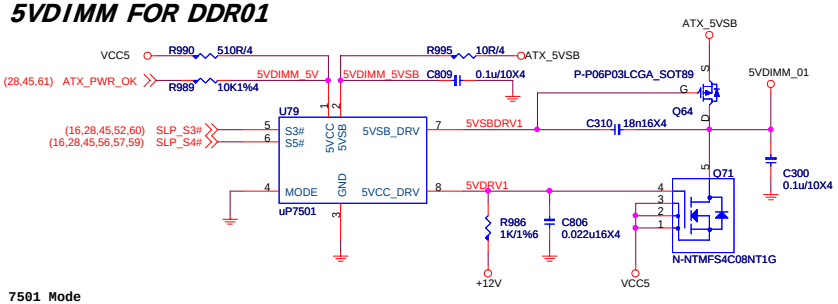
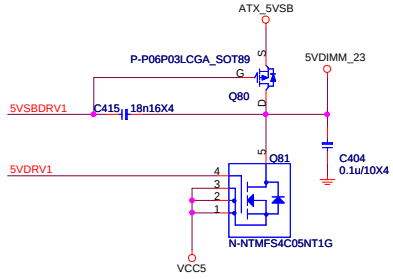
5VDIMM FOR DDR01



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

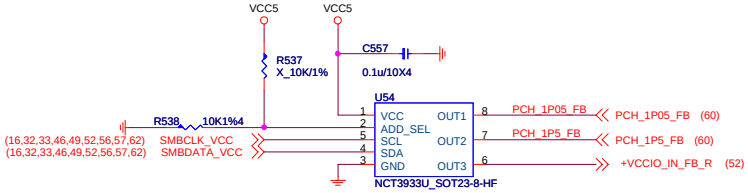
5VDRV1看VCC5起來6-10ms後起來,因為當初挑power

5VDIMM FOR DDR23

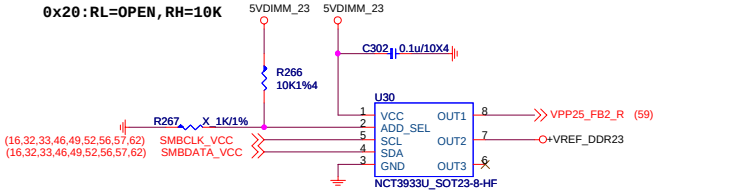


VOLTAGE CONSOLE

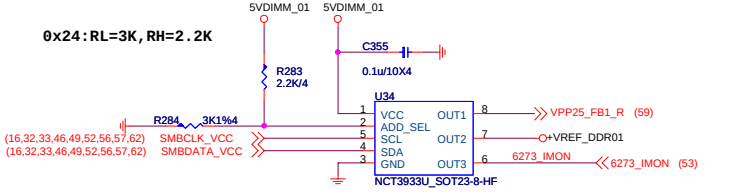
0x2A:RL=10K,RH=OPEN



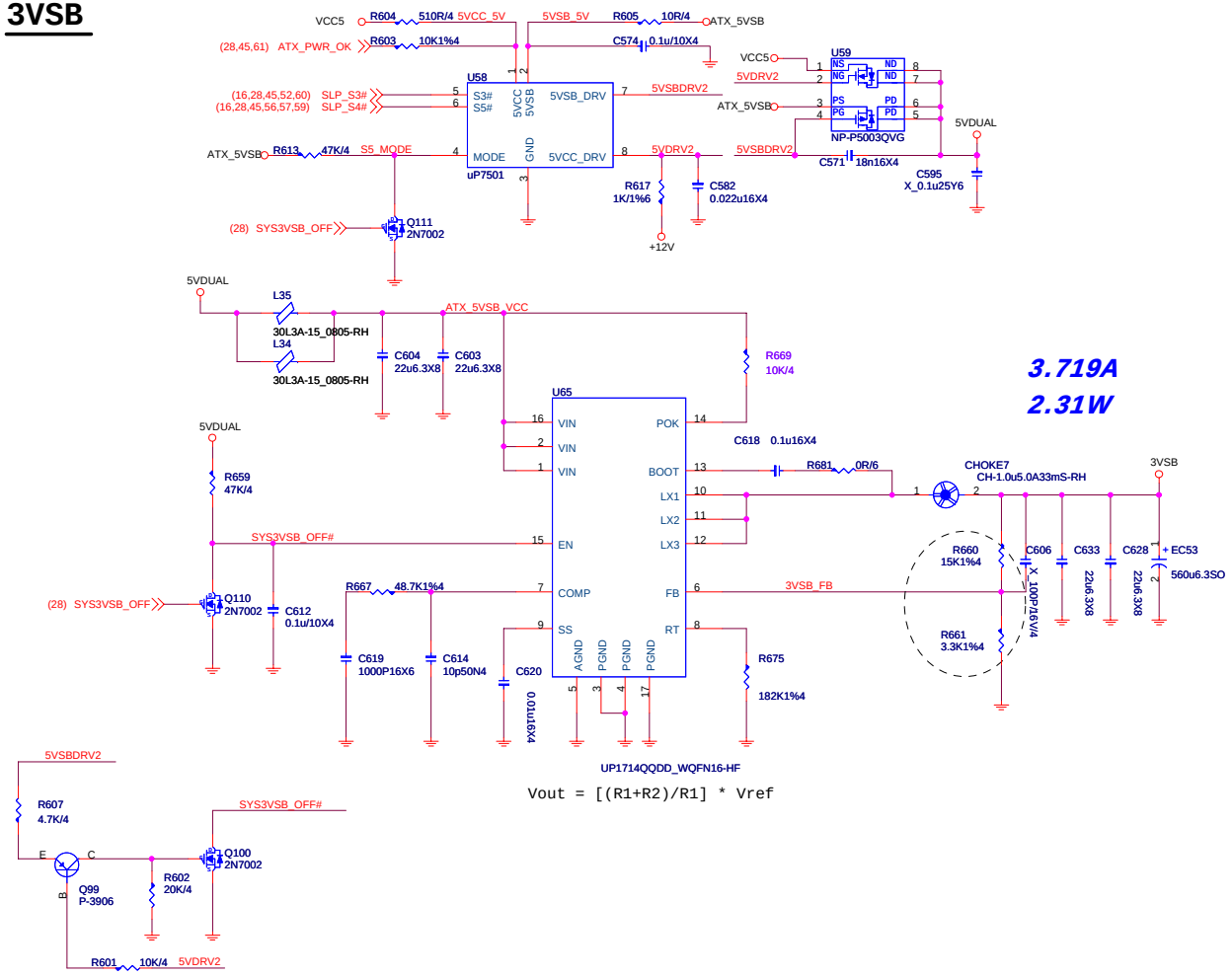
0x20:RL=OPEN,RH=10K



0x24:RL=3K,RH=2.2K

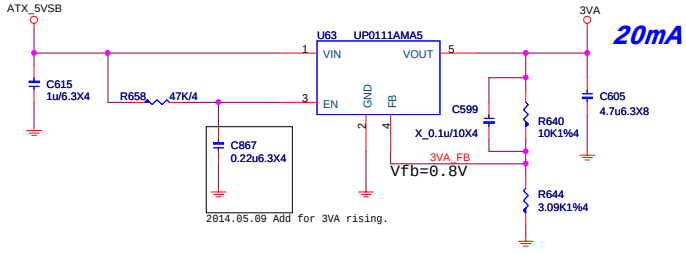


3VSB



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

3VA



2014.05.09 Add for 3VA rising.

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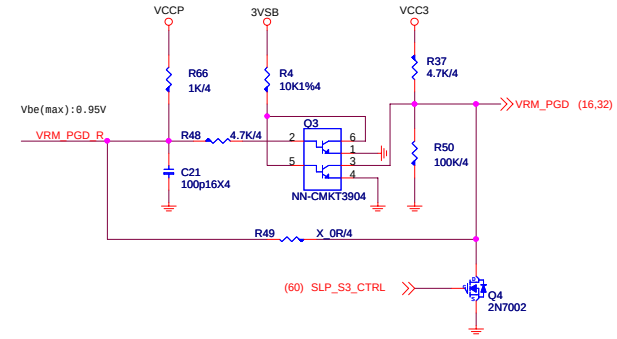
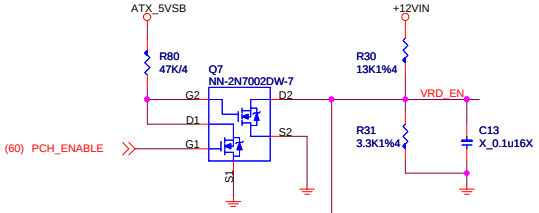
CPU Power-ISL6388-8Phase

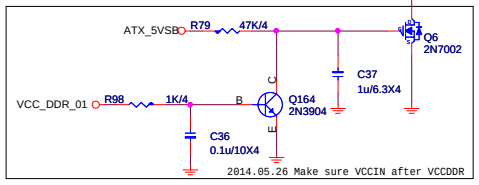
VCCP_1.8V 180A,OC margin 2.5V=240A

OCP:336A for 8Phase

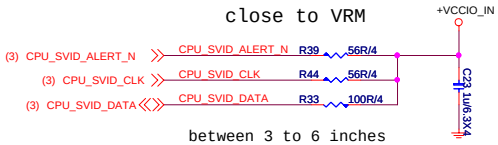
VRMPWRGD LEVEL SHIFT



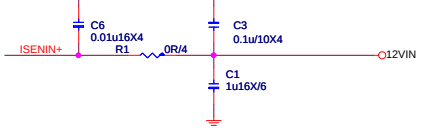




close to VRM



between 3 to 6 inches

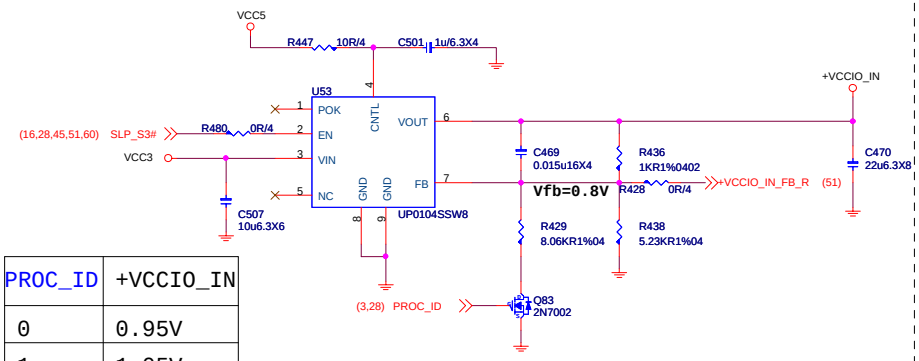


R811 stuff 154K for APS 20A per step.

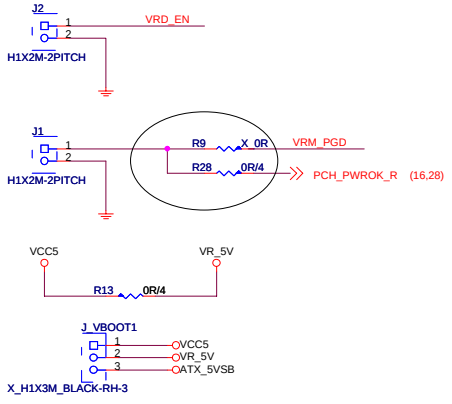
(240A / 12 Phase) * DCR / (Risen + Rset/64)
= 100uA
R753=4.64k ohm

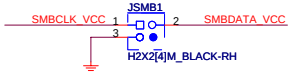
close phase sequence 6-3-5-2-4-1
address:8AH
Golden Point only for 7882

VCCIO_IN_1.05V 431mA,OC margin 1.6V=1A



PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V





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MS-7882		
Size: Custom	Document Description: VRD12.5 - PWM-uP1649	Rev: 1.0
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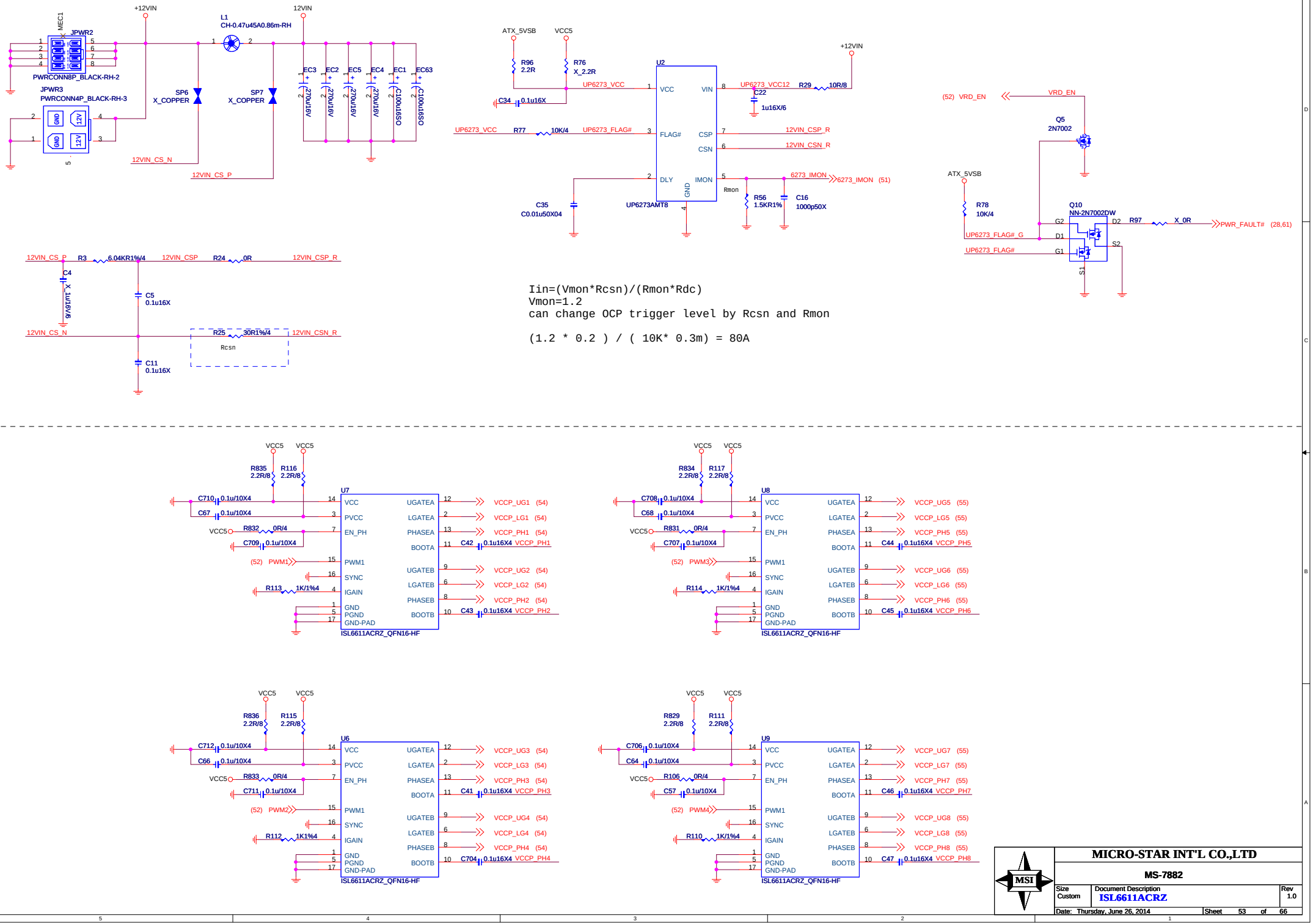
MEC1
JPWR2
PWRCONN8P_BLACK-RH-2
JPWR3
PWRCONN4P_BLACK-RH-3
+12VIN
L1
CH-0.47u45A0.86m-RH
12VIN
SP6
X_COPPER
SP7
X_COPPER
EC3
EC2
EC5
EC4
EC1
EC63
270u16V
C100u16SO
12VIN_CS_N
12VIN_CS_P
ATX_5VSB
VCC5
R96
2.2R
R76
X_2.2R
U2
UP6273_VCC
C34
0.1u16X
VCC
VIN
UP6273_VCC12
R29
10R/8
C22
1u16X/6
UP6273_VCC
R77
10K/4
UP6273_FLAG#
FLAG#
CSP
CSN
12VIN_CSP_R
12VIN_CSN_R
DLY
IMON
GND
6273_IMON
6273_IMON (51)
Rmon
R56
1.5KR1%
C16
1000p50X
C35
C0.01u50X04
UP6273AMT8
(52) VRD_EN
VRD_EN
Q5
2N7002
ATX_5VSB
R78
10K/4
Q10
NN-2N7002DW
G2
D2
R97
X_0R
PWR_FAULT# (28,61)
UP6273_FLAG# G
D1
UP6273_FLAG#
G1
S2
S1
12VIN_CS_P
R3
6.04KR1%/4
12VIN_CSP
R24
0R
12VIN_CSP_R
C4
X_1u16/6
C5
0.1u16X
12VIN_CS_N
R25
30R1%/4
12VIN_CSN_R
Rcsn
C11
0.1u16X
Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon
(1.2 * 0.2) / (10K* 0.3m) = 80A
U7
R835
2.2R/8
R116
2.2R/8
C710
0.1u/10X4
C67
0.1u/10X4
R832
0R/4
C709
0.1u/10X4
(52) PWM1
R113
1K/1%4
PVCC
EN_PH
PWM1
SYNC
IGAIN
GND
PGND
GND-PAD
UGATEA
LGATEA
PHASEA
BOOTA
UGATEB
LGATEB
PHASEB
BOOTB
VCCP_UG1 (54)
VCCP_LG1 (54)
VCCP_PH1 (54)
C42
0.1u16X4
VCCP_PH1
VCCP_UG2 (54)
VCCP_LG2 (54)
VCCP_PH2 (54)
C43
0.1u16X4
VCCP_PH2
ISL6611ACRZ_QFN16-HF
U8
R834
2.2R/8
R117
2.2R/8
C708
0.1u/10X4
C68
0.1u/10X4
R831
0R/4
C707
0.1u/10X4
(52) PWM3
R114
1K/1%4
VCCP_UG5 (55)
VCCP_LG5 (55)
VCCP_PH5 (55)
C44
0.1u16X4
VCCP_PH5
VCCP_UG6 (55)
VCCP_LG6 (55)
VCCP_PH6 (55)
C45
0.1u16X4
VCCP_PH6
ISL6611ACRZ_QFN16-HF
U6
R836
2.2R/8
R115
2.2R/8
C712
0.1u/10X4
C66
0.1u/10X4
R833
0R/4
C711
0.1u/10X4
(52) PWM2
R112
1K/1%4
VCCP_UG3 (54)
VCCP_LG3 (54)
VCCP_PH3 (54)
C41
0.1u16X4
VCCP_PH3
VCCP_UG4 (54)
VCCP_LG4 (54)
VCCP_PH4 (54)
C704
0.1u16X4
VCCP_PH4
ISL6611ACRZ_QFN16-HF
U9
R829
2.2R/8
R111
2.2R/8
C706
0.1u/10X4
C64
0.1u/10X4
R106
0R/4
C57
0.1u/10X4
(52) PWM4
R110
1K/1%4
VCCP_UG7 (55)
VCCP_LG7 (55)
VCCP_PH7 (55)
C46
0.1u16X4
VCCP_PH7
VCCP_UG8 (55)
VCCP_LG8 (55)
VCCP_PH8 (55)
C47
0.1u16X4
VCCP_PH8
ISL6611ACRZ_QFN16-HF
MSI
MICRO-STAR INT'L CO.,LTD
MS-7882
Size
Custom
Document Description
ISL6611ACRZ
Rev
1.0
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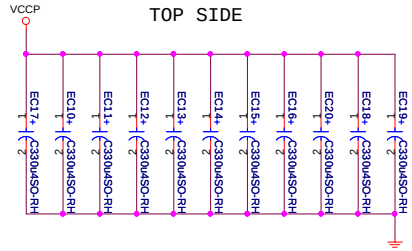
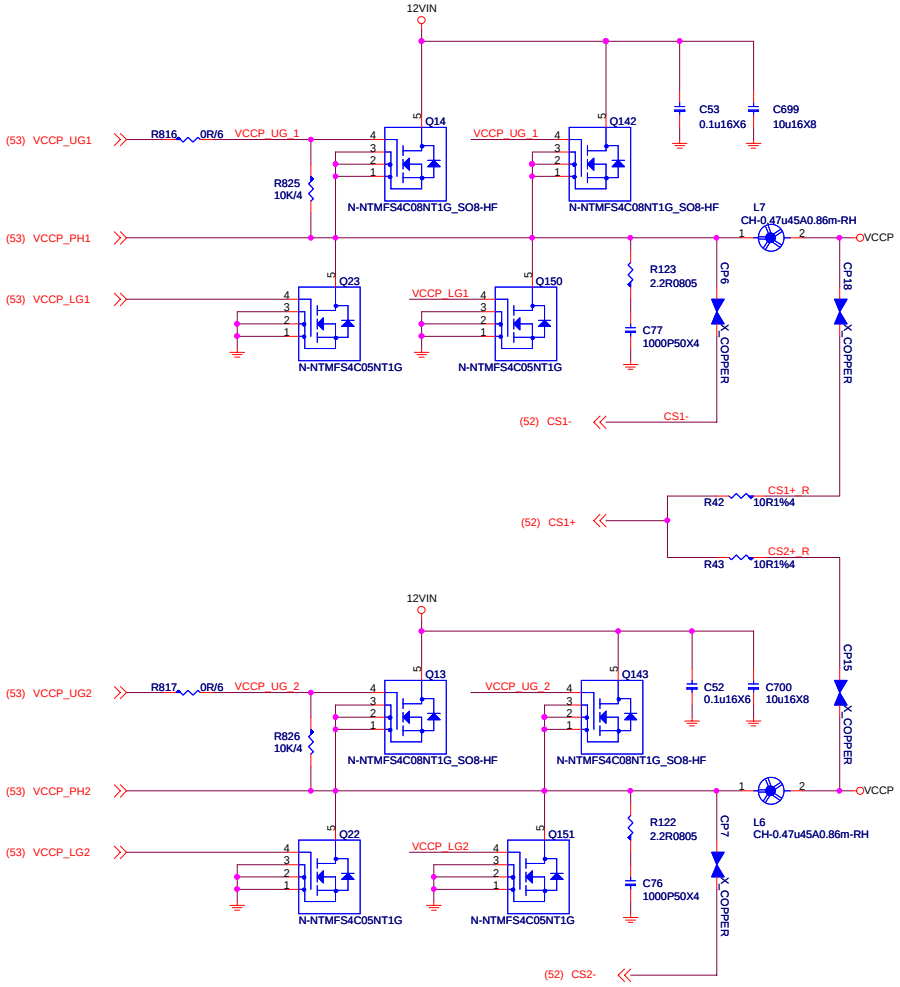
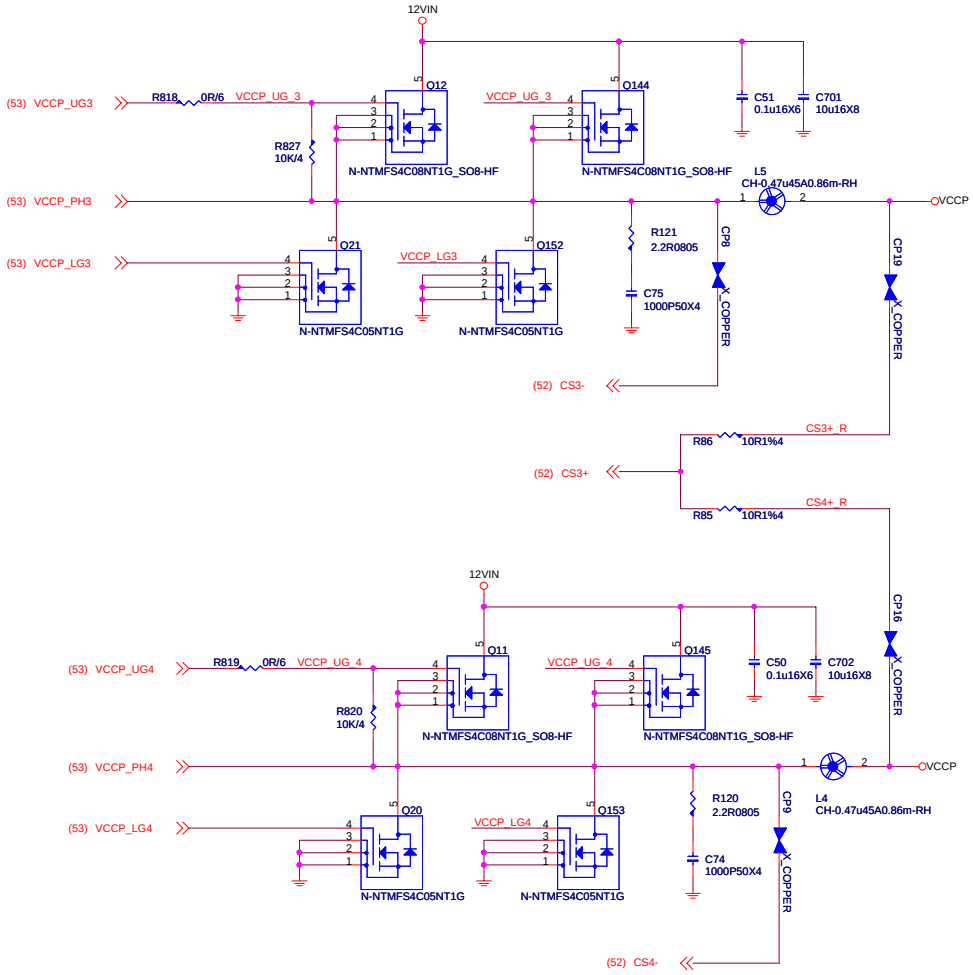
Irms= Iout $\sqrt{D/N-(D)^2}$ = 320 $\sqrt{0.02-(0.16)^2}$ = 23.94A

5000mA*5=25A>23.94A







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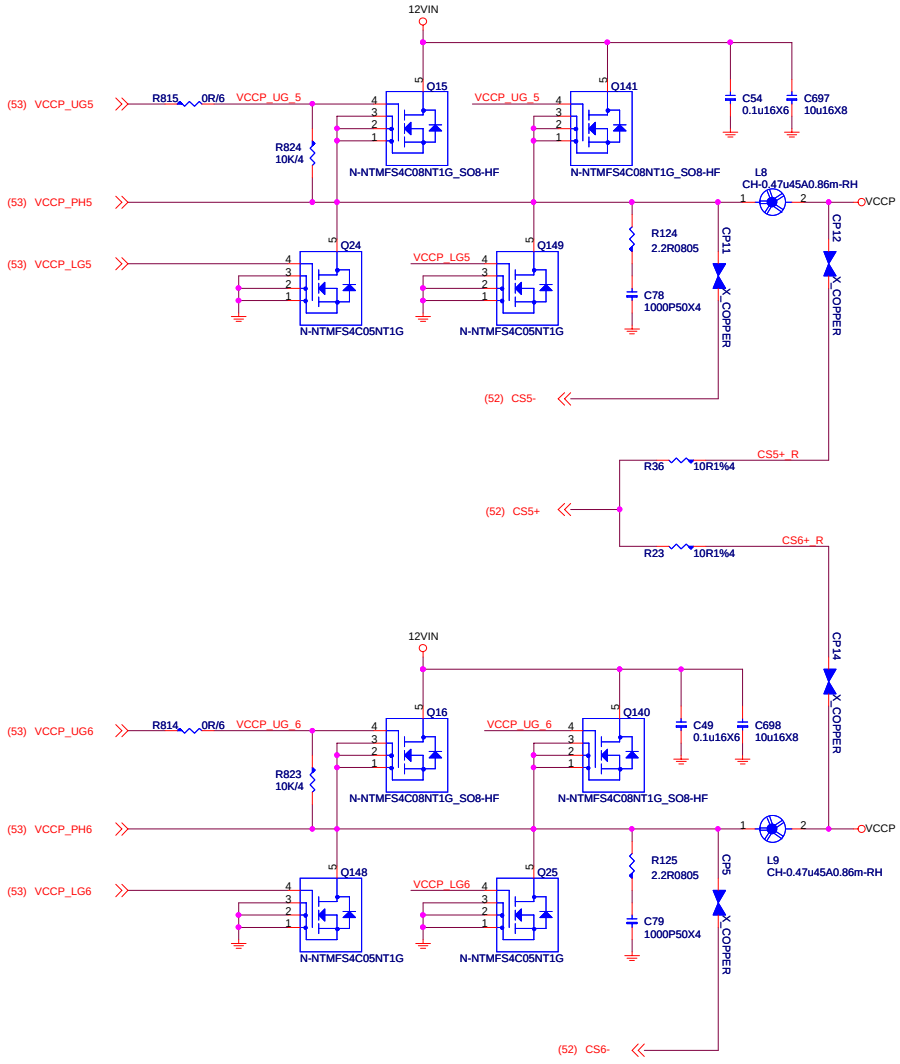

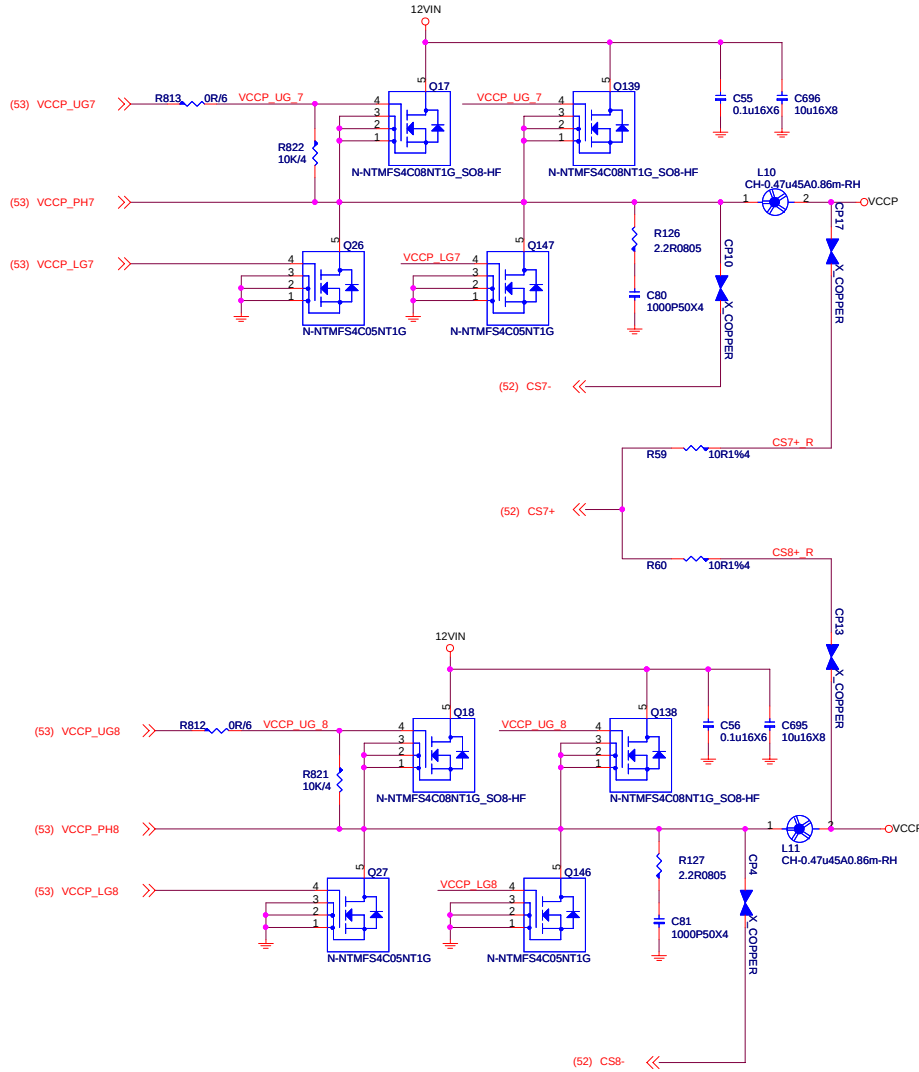

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MS-7882		
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DDR Power1-PV3203-2-Phase

DDR4_1.2V 11A,OC margin=44A

OCP:66A for 2Phase

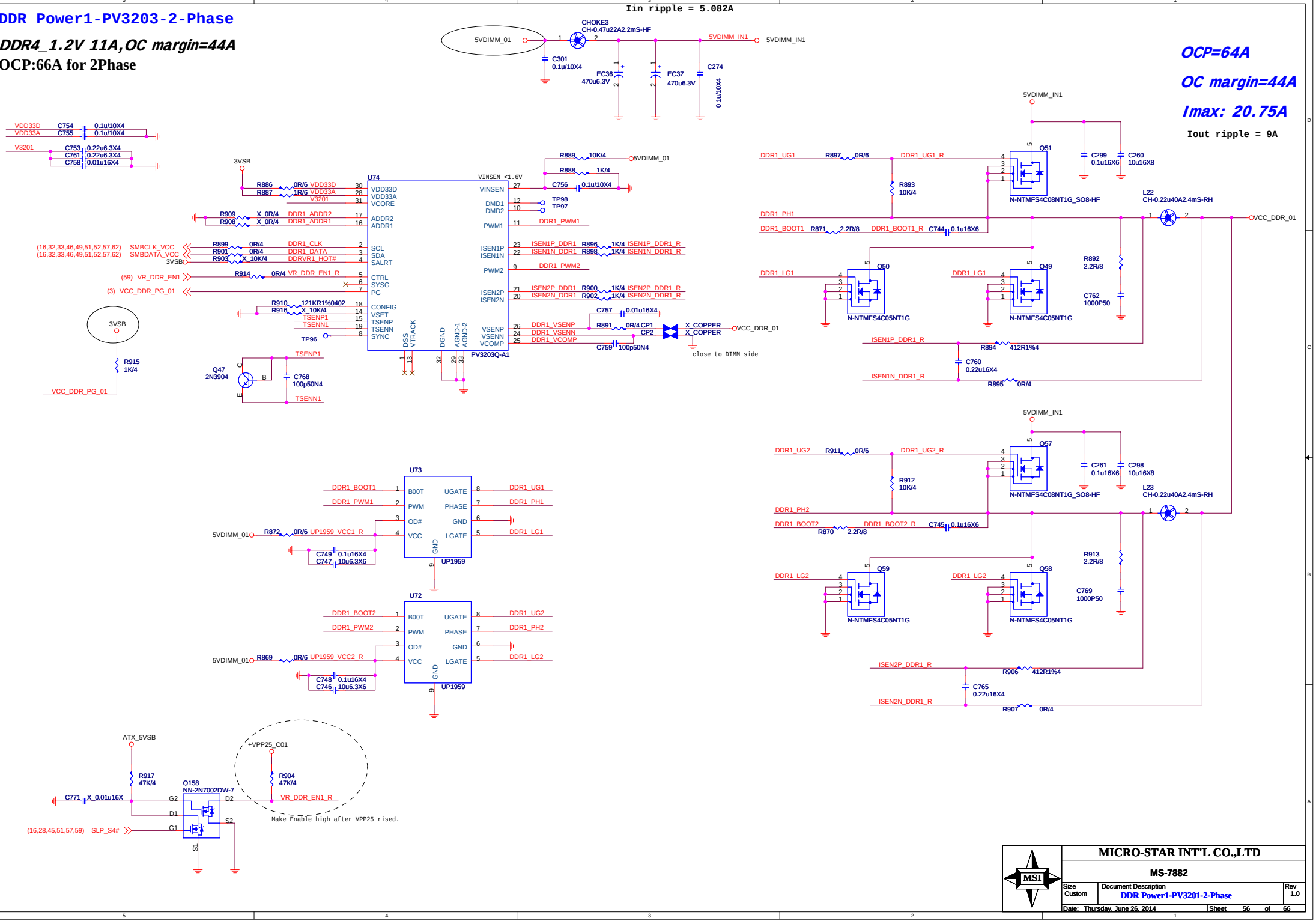
Iin ripple = 5.082A

OCP=64A

OC margin=44A

Imax: 20.75A

Iout ripple = 9A



MICRO-STAR INT'L CO.,LTD		
MS-7882		
Size: Custom	Document Description: DDR Power1-PV3201-2-Phase	Rev: 1.0
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DDR Power1-PV3203-2-Phase

DDR4_1.2V 11A,OC margin=44A

OCP:66A for 2Phase

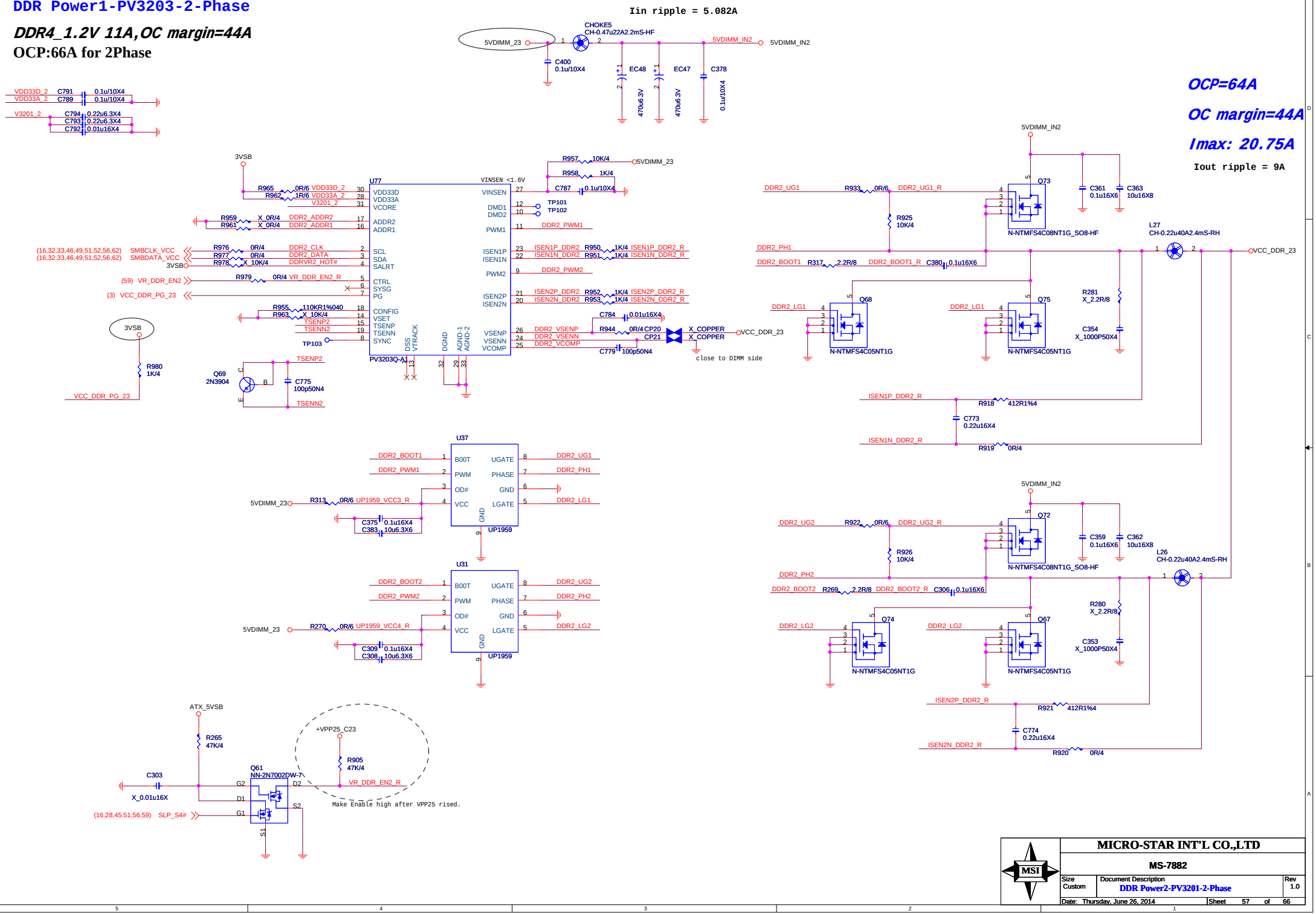
Iin ripple = 5.082A

OCP=64A

OC margin=44A

Imax: 20.75A

Iout ripple = 9A



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7882	
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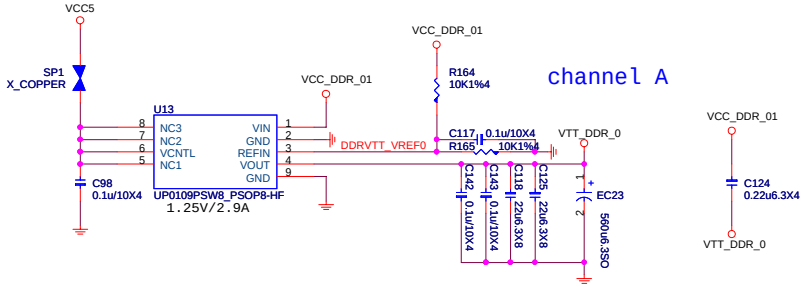
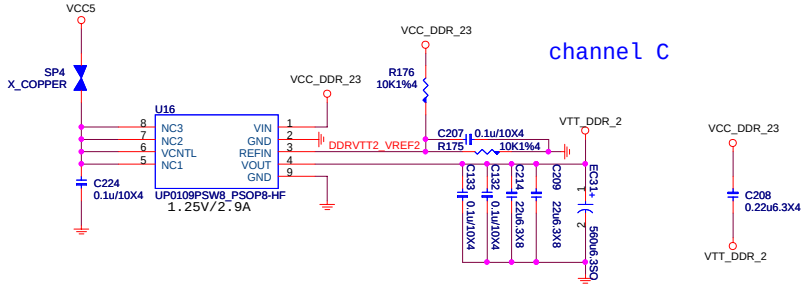
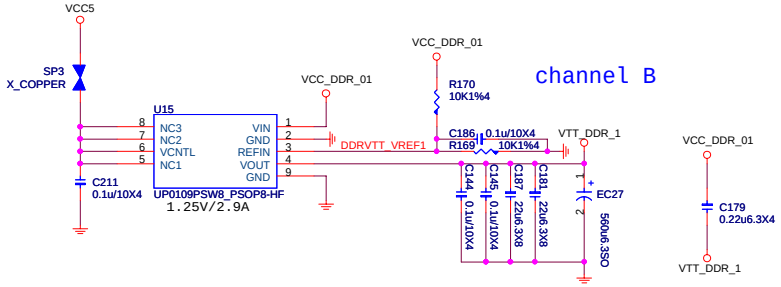
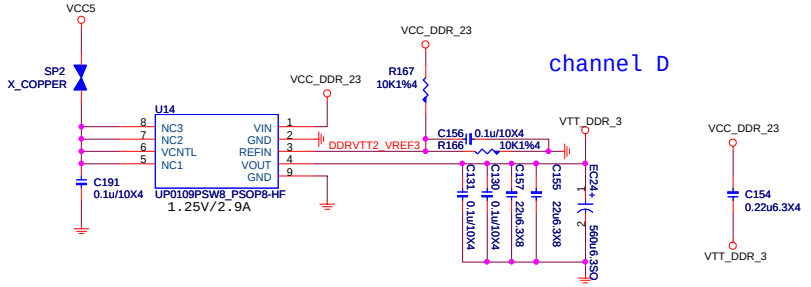
4DIMM :1.2A FOR DDR VTT

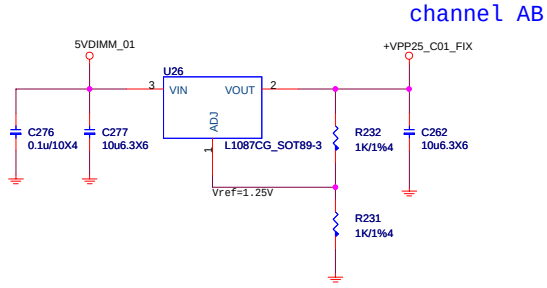
4DIMM :3A FOR OC margin

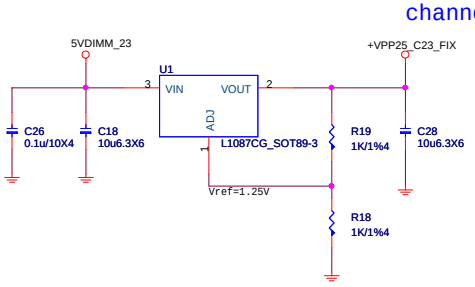












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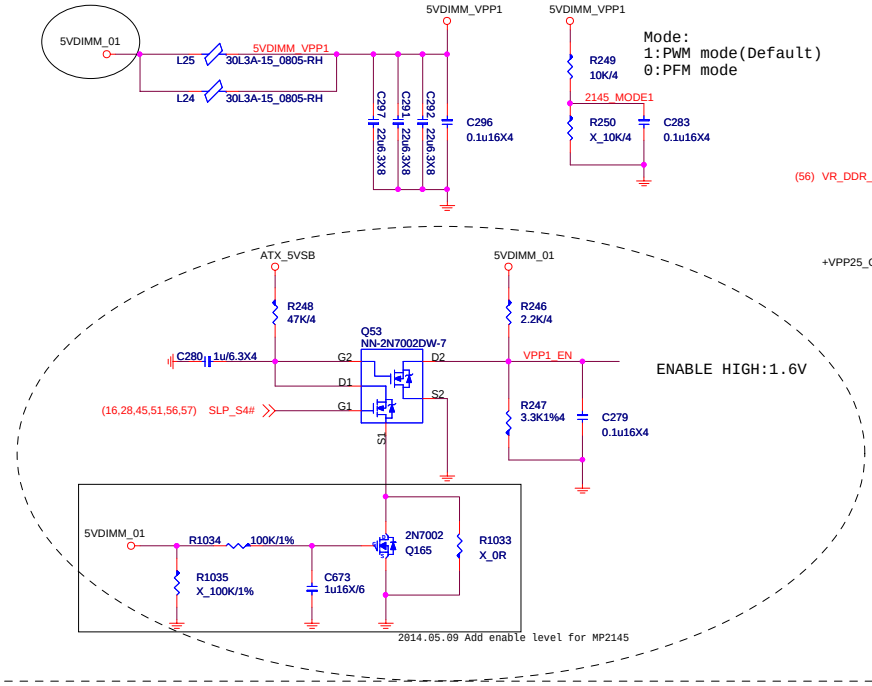
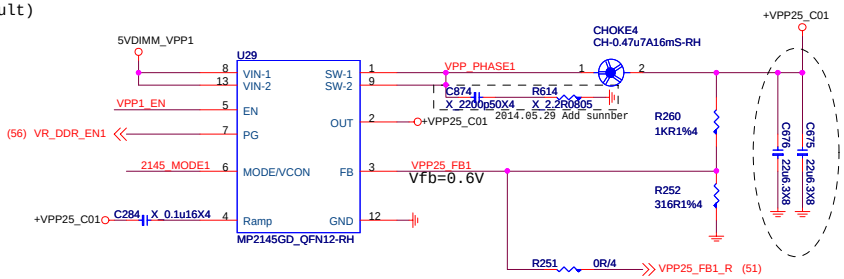
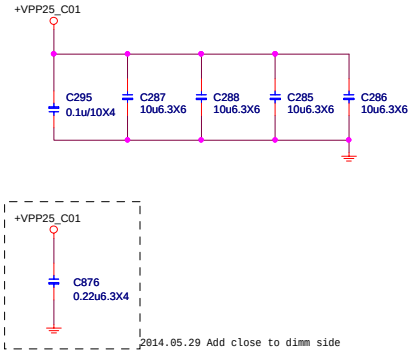
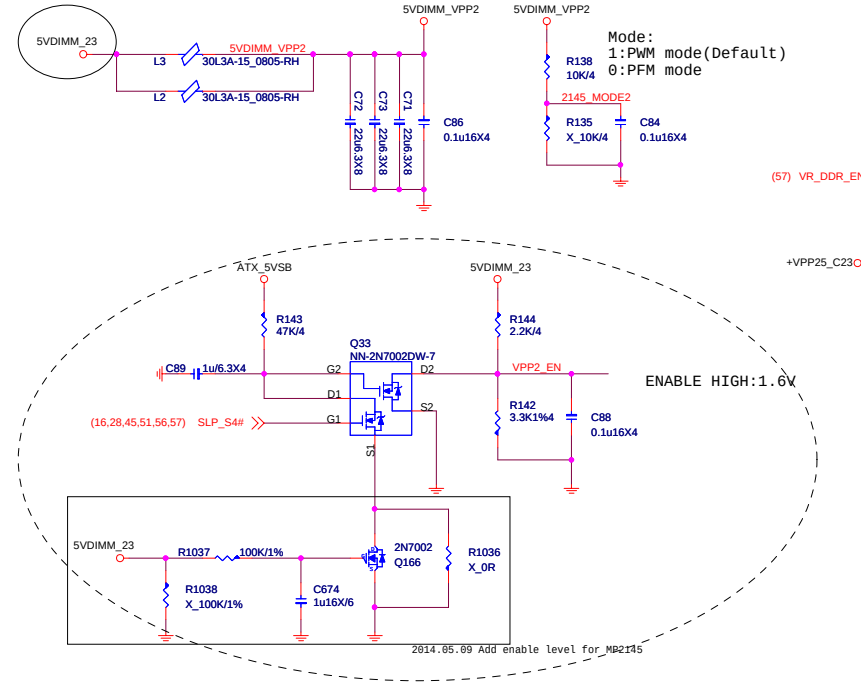
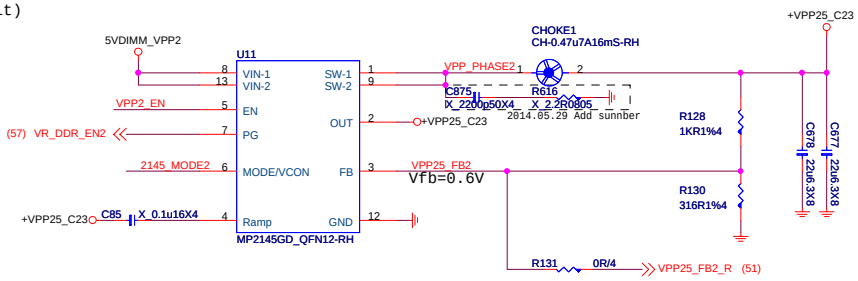
4DIMM :6A FOR DDR VPP

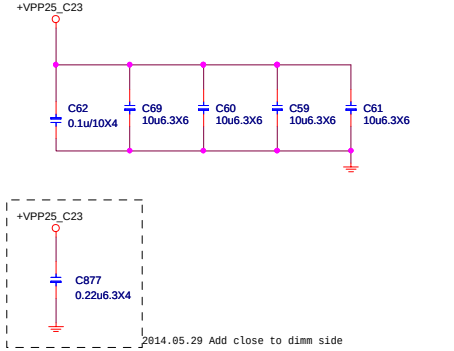












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PCH Power:1.05V

PCH Core 6.504A

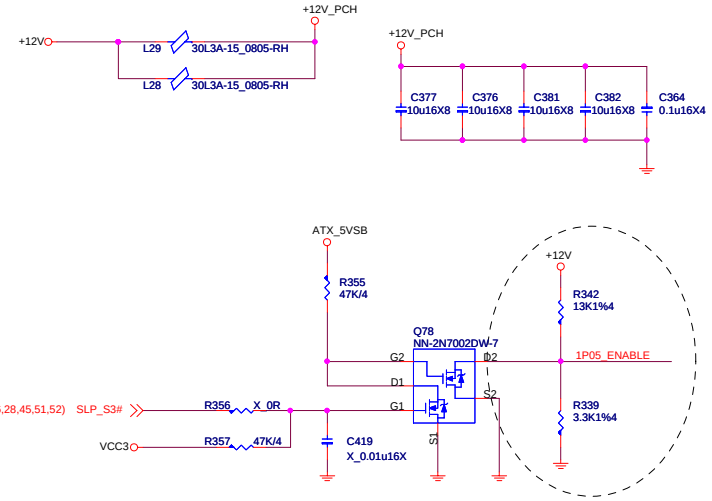
OCP calculate:

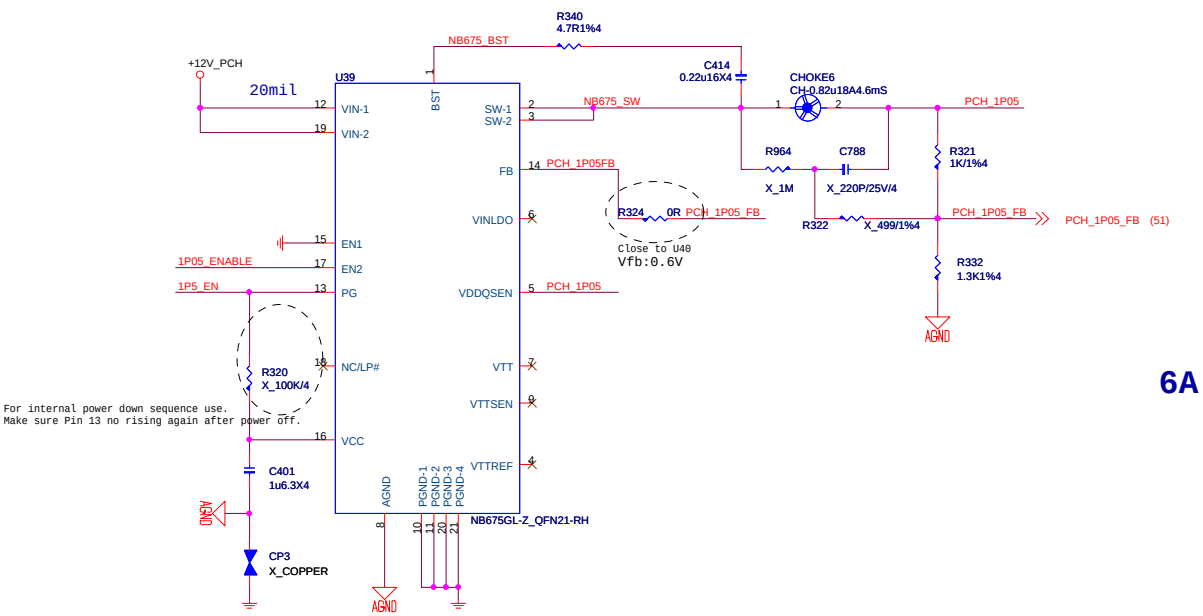
(20mA * Rocs) / 4 * Rds-on = IOCP

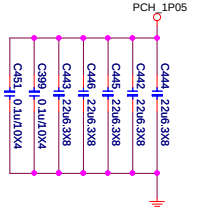
(20mA * 12.1K) / 4 * 4mohm = 15.5A

MAX 10A

ILIMIT=10A~12A 峰谷

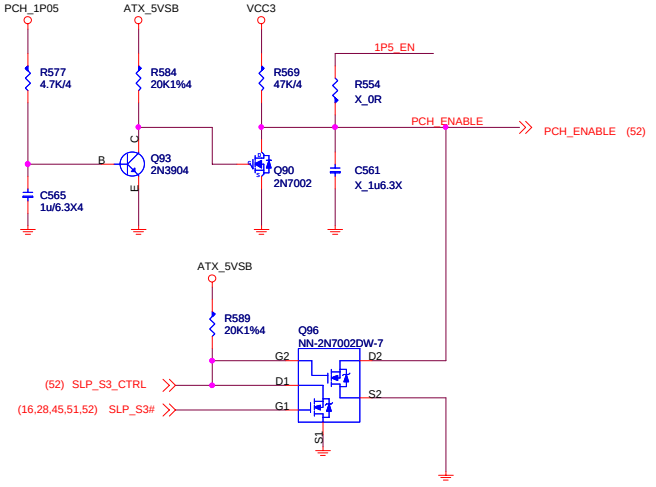


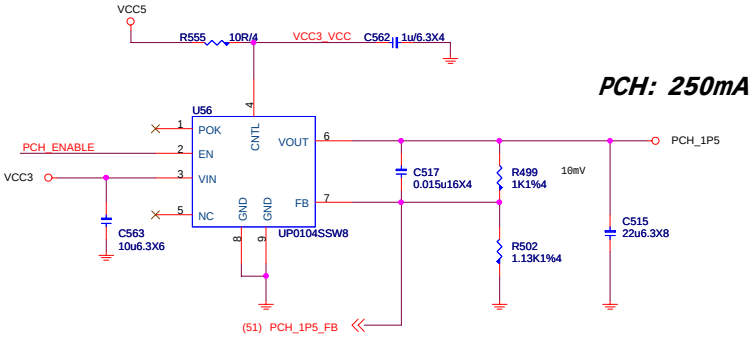




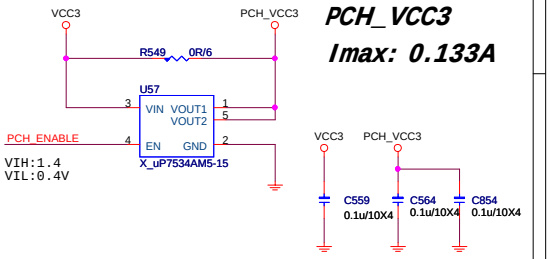
6A

Waitting PCH_1P05 Ready





PCH: 250mA



PCH_VCC3

Imax: 0.133A

C854 close to PCH

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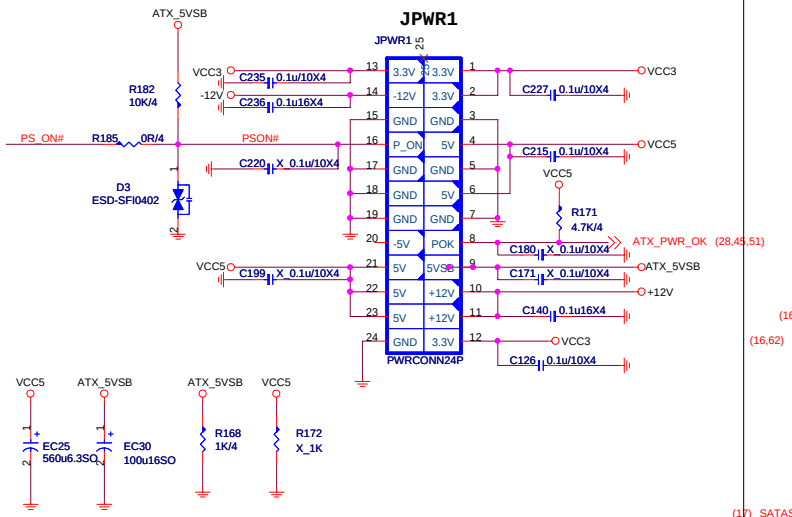
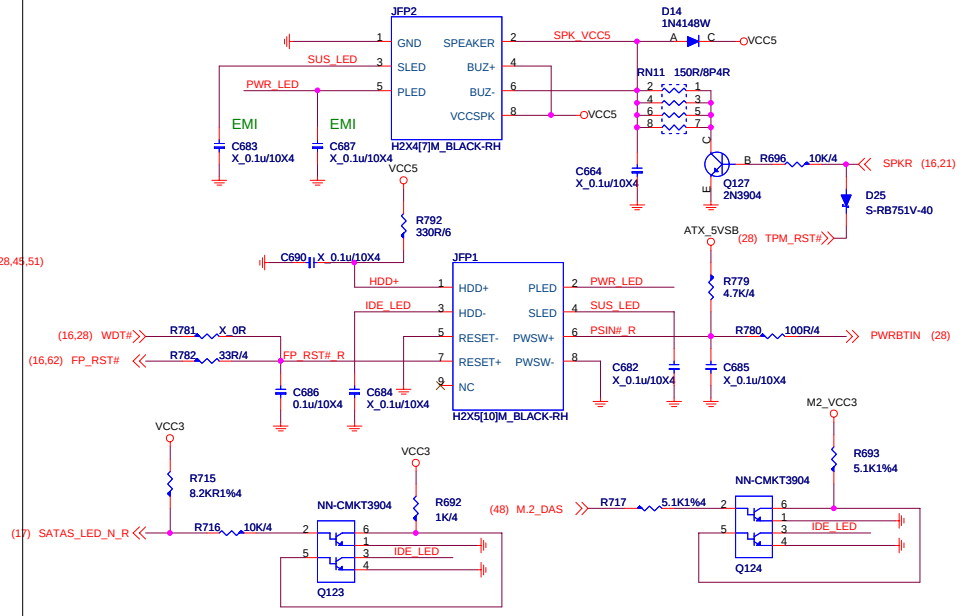
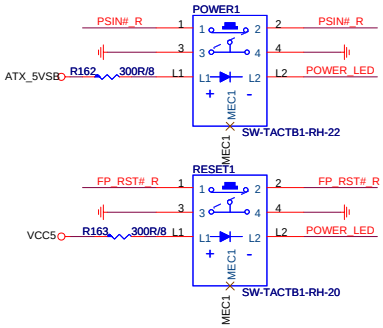
ATX POWER CONNECTOR

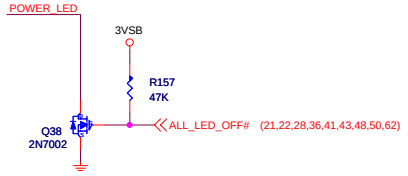


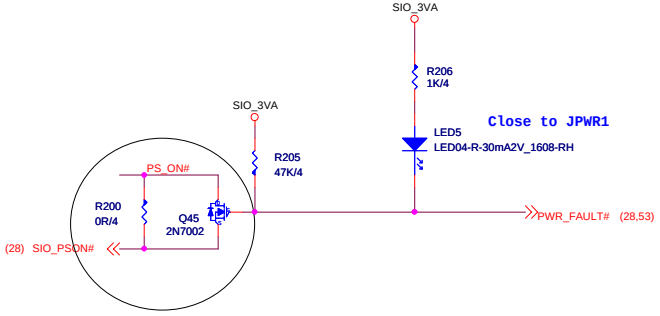
FRONT PANNEL



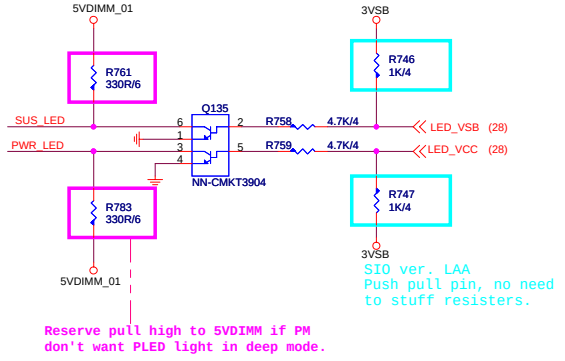
PWR/RST Botton



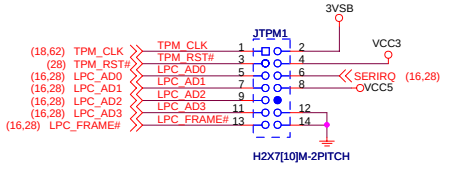


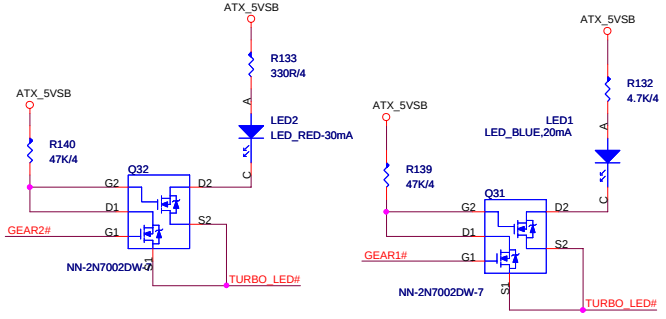


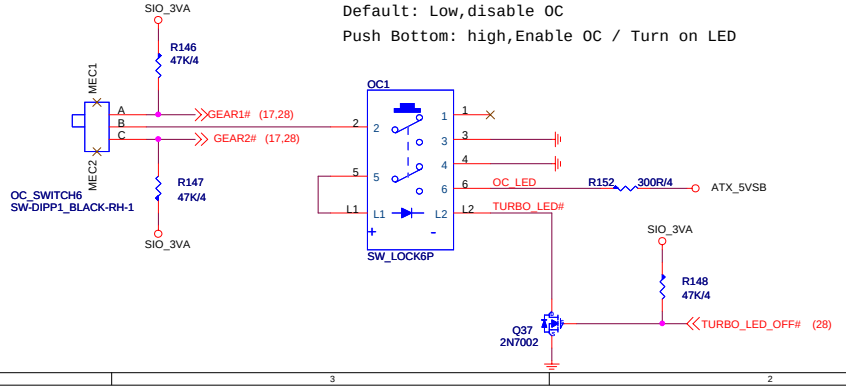
Front Panel LED



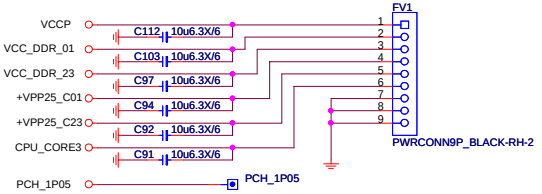
TPM







Voltage test point



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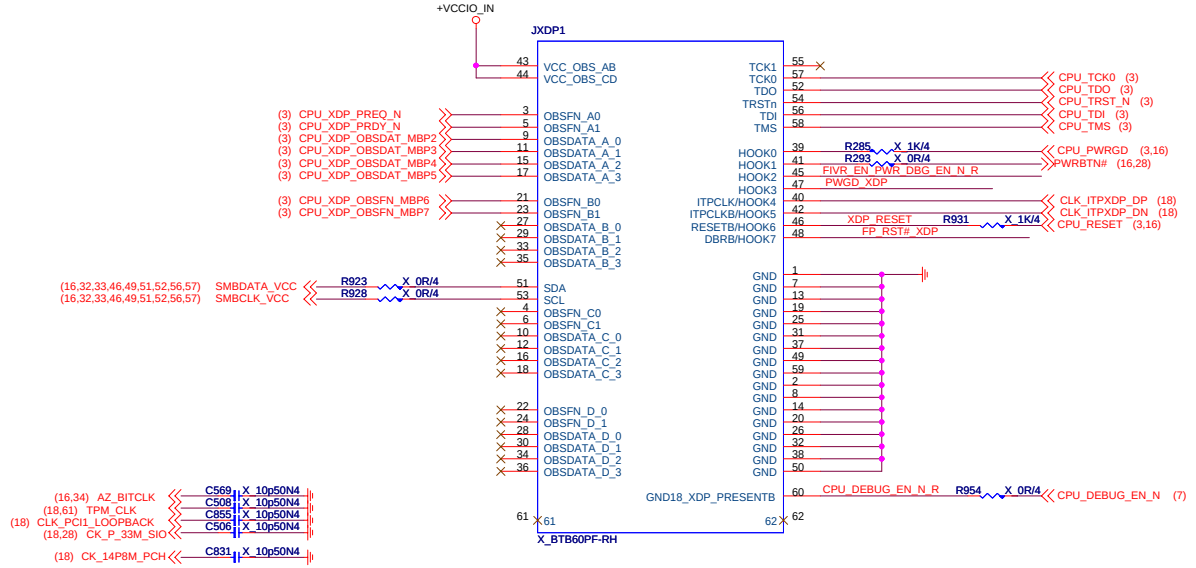
Reserve debug port 5020



(16,34) AZ_BITCLK
(18,61) TPM_CLK
(18) CLK_PCI1_LOOPBACK
(18,28) CK_P_33M_SIO
C569 X_10p50N4
C508 X_10p50N4
C855 X_10p50N4
C506 X_10p50N4
(18) CK_14P8M_PCH
C831 X_10p50N4
(18,28) CK_48M_SIO
C832 X_10p50N4

+VCCIO_IN
CPU_DEBUG_EN_N R942 976R1%4
CPU_TDO R940 75R/4

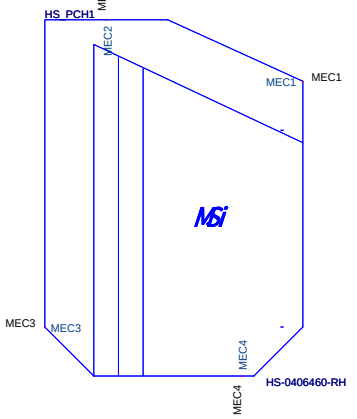
WITHIN 250MILS OF XDP CONNECTOR PIN

VCC_DDR_01
C766 0.1u/10X4
C764 0.1u/10X4
C763 0.1u/10X4
C767 0.1u/10X4

+VCCIO_IN
R294 X_150R1%4
(7) CPU_PWR_DEBUG_N
R295 X_0R/4
FIVR_EN_PWR_DBG_EN_N_R
C356 X_0.1u/10X4

VCC3
R960 X_4.7K/4
(16,61) FP_RST#
R956 X_0R/4
FP_RST#_XDP
C786 X_0.1u/10X4

VCC3
R296 X_4.7K
(16,28) SYS_PWROK
R297 X_0R/4
PWGD_XDP
C357 X_0.1u/10X4



CPU_H1
CPU 鎖座
CPU_H1

BAT1_X1
BAT-BCR2032P-RH

HS_MOS1
X_HS-0501760-RH

CPU_H2
CPU 鎖座
CPU_H1

mini_card1
mini PCIE Card
mini_PCIE_card

FM6 X_FM
FM3 X_FM
FM15 X_FM
FM16 X_FM

VCC5
U118
SLG59M1440V
ALL_LED_OFF#
(21,22,28,36,41,43,48,50,61) ALL_LED_OFF#
PIPE_5V
JPIPE_LED1
BH1X3HS-1.25PITCH_BLACK-RH

VCCP
VCC_DDR_01
VCC_DDR_23
+VPP25_C01
+VPP25_C23
PCH_1P5
3VSB
+VCCIO_IN
3VA
VTT_DDR_0
VTT_DDR_1
VTT_DDR_2
VTT_DDR_3

SIM2 X_PIN1*2
SIM1 X_PIN1*2

Mounting Holes

MH1 X_MH001
MH2 X_MH001
MH8 X_MH001
MH6 X_MH001
MH7 X_MH001
MH5 X_MH001
MH10 X_MH001
MH3 X_MH001
MH9 X_MH001
C671 0.1u/10X4
C667 0.1u/10X4
C349 0.1u/10X4
C305 0.1u/10X4

Optical Fiducial Marks-120

FM9 X_FM
FM10 X_FM
FM8 X_FM
FM7 X_FM
FM1 X_FM
FM4 X_FM
FM5 X_FM
FM2 X_FM

MICRO-STAR INT'L CO.,LTD

MS-7882

Size	Document Description	Rev
Custom	XDP / Manual Parts	1.0

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