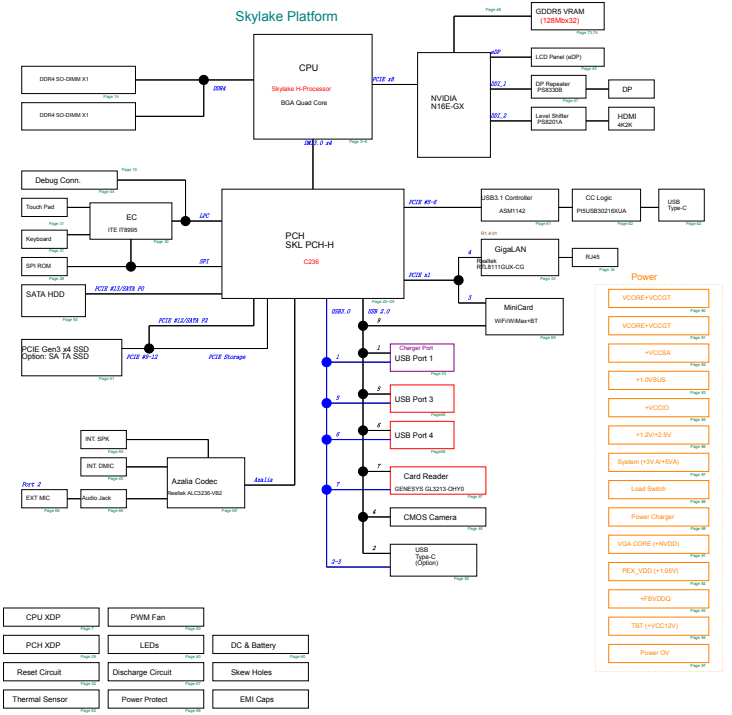
GL502VM Block Diagram



PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_PEGA_REQ0#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_GLAN#_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/GPUEVENT#_PCH		PU 10K(@)	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/GC6FBEN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	GPO	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	PCH_GPPC2			
GPP_C3	SML0CLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		+3VSUS
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(@)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(@)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PU 10K(@)	+3VSUS
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT			
GPP_D1	GPI	GPO	GPIO_3_FORCE_PWR			
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#		PD 100K(@)	
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCB_ID0		PD 10K	
GPP_D10	GPI	Strap	PCB_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID		PD 10K(@)	
GPP_D12	GPI	Strap	TOUCH_PANEL_ID		PD 10K(@)	
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(@)	+3VSUS
GPP_D14	GPI	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPI	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)		PU 10K(@)	+3V
GPP_E4	GPI	Native	NGFF0_DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	NGFF2_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(@)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	(N.C)			
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	SATA3_HDD_DEVSLP		PU 10K(@)	+3VS
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPI	(N.C)		(N.C)	
GPP_F20	GPI	GPI	(N.C)			
GPP_F21	GPI	GPI	(N.C)		(N.C)	
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPI	(N.C)			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H5	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H6	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H7	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H8	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H9	GPI	Native	(N.C)		(N.C)	(N.C)
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	(N.C)		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPI	(N.C)		(N.C)	
GPP_I1	GPI	GPI	(N.C)		(N.C)	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	GPI	(N.C)			
GPP_I4	GPI	GPI	GPP_I4		PD 100K	
GPP_I5	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I6	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)
GPP_I7	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I8	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)
GPP_I9	GPI	GPI	(N.C)		(N.C)	(N.C)
GPP_I10	GPO	GPO	(N.C)	(N.C)	(N.C)	(N.C)

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	PCH_GPD2#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUSB#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUSC#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	(N.C)	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	NKey_WRST	PD 10K	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4/INTR#	PU 10K (@)	+3VSUS
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN#_wCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	EC_GPE6		
GPE7	OD	GPO	THRO_CPU#	PU 10K(@) (N.C)	+3VA_EC (N.C)

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH	PD 10K (@)	
GPG4	GPI		EC_SI/EC_SI_PCH	PD 10K (@)	
GPG5	GPI		EC_SO/EC_SO_PCH	PD 10K (@)	
GPG6	O	GPO	USB30_5VSUS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K(@)	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	(N.C)	(N.C)
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	(N.C)	(N.C)
GPI7	Alt	AD	MB_MAX_POWER	PU 100K & PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	EC_GPJ6/KB_WAKE#	PU 100K(@)	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Ad dress	
on board memory CHA		
SO-DIMM B(0)	A4h	
EC Master (SMB1)	SM-Bus Ad dress	
SM-Bus Device		
VGA Thermal Sensor	96h	
CPU Thermal Sensor	90h	
Power Thermal Sensor	7Eh	

Device Identification

CPU Thermal Sensor		
1st	080023123010	NCT7717U
2nd		

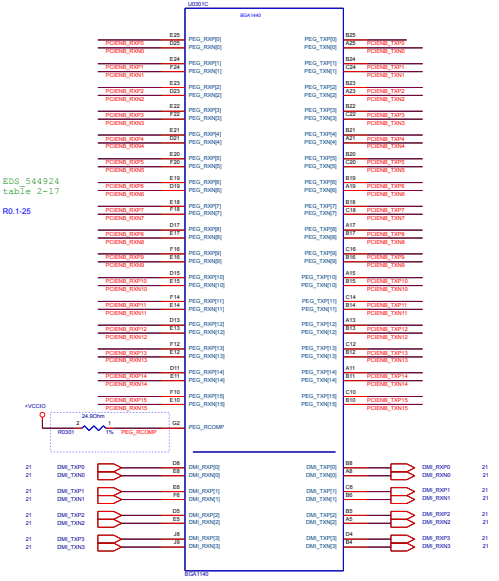
GL502VM PCIE & USB Function define

Skylake HM170

HSIO	HSIO Capabilies	Funcon	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01		
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06	USB3_IO	
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	SRC1
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN	SRC4
11	PCIE#05 / GBE	TBT	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	PCIE*4 SSD SATA SSD	SRC6
16	PCIE#10 / SATA#1		
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	1st HDD	
23			
24			
25			
26			

USB 2.0	Funcon
USB2_01	USB3.0 MB Port1
USB2_02	
USB2_03	
USB2_04	Camera
USB2_05	USB3.0 IO Port1
USB2_06	USB3.0 IO Port2
USB2_07	CardReader
USB2_08	N-Key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

PCIEG

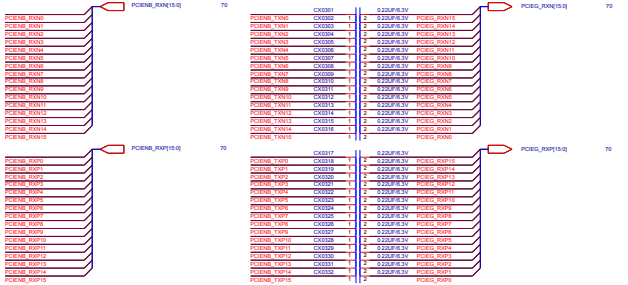


EDS_544924
table 2-17

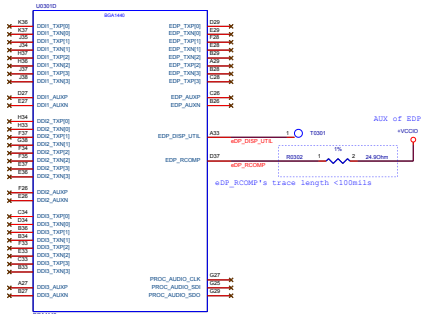
R0.1-25

R0301 close to CPU
PEG_COMP trace length <400mils

Main Board



Display



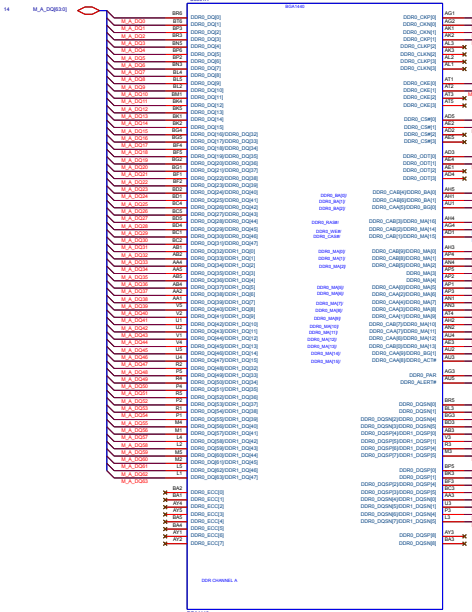
AUX of EDP

eDP_RCOMP's trace length <100mils

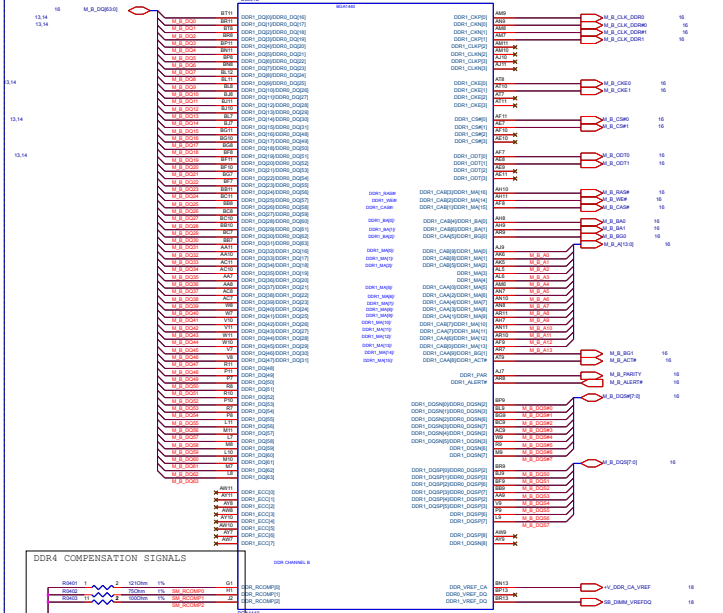
R0303 Place Near CPU

Main Board

Memory Channel A

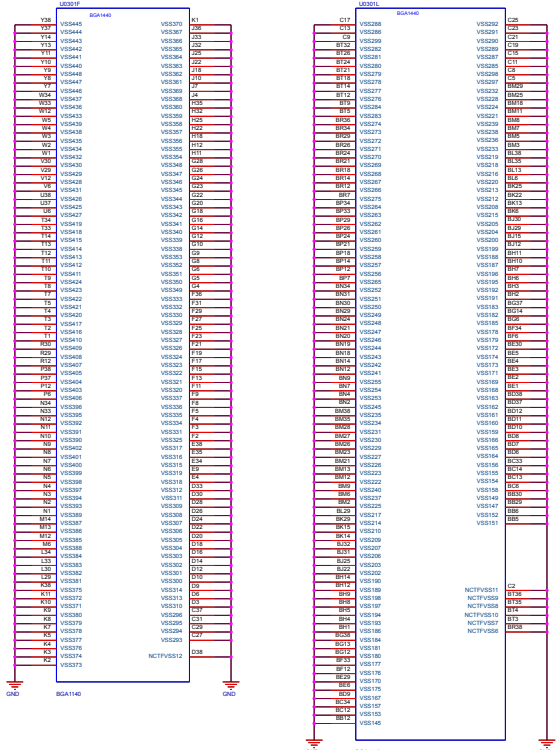


Memory Channel B



DDR4 COMPENSATION SIGNALS

Main Board


U3301F
BGA1440
Y38 VSS445
Y37 VSS444
Y14 VSS443
Y13 VSS442
Y11 VSS441
Y10 VSS440
Y9 VSS448
Y8 VSS447
Y7 VSS446
W34 VSS445
W33 VSS436
W12 VSS433
W5 VSS439
W4 VSS438
W3 VSS435
W2 VSS434
W1 VSS432
V30 VSS430
V29 VSS429
V12 VSS428
V6 VSS431
U38 VSS426
U37 VSS425
U8 VSS427
T34 VSS419
T33 VSS418
T14 VSS415
T13 VSS414
T12 VSS413
T11 VSS412
T10 VSS411
T9 VSS411
T8 VSS423
T7 VSS422
T5 VSS421
T4 VSS420
T3 VSS417
T2 VSS416
T1 VSS419
R30 VSS409
R29 VSS408
R12 VSS408
P38 VSS405
P37 VSS404
P12 VSS403
P6 VSS406
N34 VSS396
N33 VSS395
N12 VSS392
N11 VSS391
N10 VSS390
N9 VSS402
N8 VSS401
N7 VSS400
N6 VSS399
N5 VSS398
N4 VSS397
N3 VSS394
N2 VSS393
N1 VSS389
M14 VSS387
M13 VSS386
M12 VSS385
M6 VSS388
L34 VSS384
L33 VSS383
L30 VSS382
L29 VSS381
K38 VSS381
K11 VSS372
K10 VSS371
K9 VSS380
K8 VSS379
K7 VSS378
K5 VSS377
K4 VSS376
K3 VSS374
K2 VSS373
K1 VSS370
J36 VSS367
J33 VSS366
J32 VSS365
J25 VSS364
J22 VSS363
J18 VSS362
J10 VSS361
J7 VSS369
J4 VSS368
H35 VSS360
H32 VSS359
H25 VSS358
H22 VSS357
H18 VSS356
H12 VSS355
H11 VSS354
G28 VSS348
G26 VSS347
G24 VSS346
G23 VSS345
G22 VSS344
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G16 VSS341
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G10 VSS338
G9 VSS353
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G5 VSS350
G4 VSS349
F36 VSS333
F31 VSS332
F29 VSS330
F27 VSS329
F25 VSS328
F23 VSS327
F21 VSS326
F19 VSS324
F17 VSS323
F15 VSS322
F13 VSS321
F11 VSS320
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F6 VSS336
F4 VSS335
F3 VSS334
F2 VSS331
E38 VSS325
E35 VSS317
E34 VSS316
E9 VSS315
E4 VSS318
D33 VSS312
D30 VSS311
D28 VSS308
D26 VSS307
D24 VSS306
D22 VSS305
D20 VSS304
D18 VSS303
D16 VSS302
D12 VSS301
D10 VSS300
D9 VSS314
D6 VSS313
D3 VSS310
C37 VSS296
C31 VSS295
C29 VSS294
C27 VSS293
D38 NCTFVSS12
GND
BGA1140
GND
U3301L
BGA1440
C17 VSS288
D13 VSS286
C9 VSS299
BT32 VSS282
BT26 VSS281
BT24 VSS280
BT21 VSS279
BT18 VSS278
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BT12 VSS276
BT9 VSS284
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BM13 VSS223
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BM9 VSS221
BM8 VSS220
BM2 VSS257
BL29 VSS225
BK26 VSS217
BK15 VSS214
BK14 VSS210
BJ32 VSS209
BJ31 VSS207
BJ25 VSS206
BJ22 VSS203
BH14 VSS202
BH12 VSS190
BH9 VSS189
BH8 VSS198
BH5 VSS197
BH4 VSS194
BH1 VSS193
BG38 VSS186
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BG12 VSS180
BF33 VSS177
BF12 VSS176
BE29 VSS170
BE6 VSS175
BD9 VSS167
BC34 VSS157
BC12 VSS153
BB12 VSS145
C25 VSS292
C21 VSS291
C16 VSS290
C15 VSS289
C11 VSS287
C8 VSS285
C5 VSS286
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BM25 VSS232
BM16 VSS228
BM11 VSS224
BM8 VSS221
BL37 VSS239
BM5 VSS238
BM2 VSS236
BL38 VSS233
BL35 VSS218
BL13 VSS216
BL6 VSS220
BK25 VSS213
BK22 VSS212
BK13 VSS208
BK6 VSS215
BJ30 VSS205
BJ29 VSS204
BJ12 VSS200
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BH10 VSS188
BH7 VSS187
BH6 VSS196
BH3 VSS195
BG7 VSS192
BG37 VSS191
BG14 VSS183
BG6 VSS182
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BE4 VSS174
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BE2 VSS171
BE1 VSS169
BD38 VSS168
BD37 VSS163
BD12 VSS162
BD11 VSS161
BD10 VSS160
BC8 VSS159
BD7 VSS166
BD6 VSS165
BC33 VSS164
BC14 VSS156
BC13 VSS155
BC6 VSS154
BB30 VSS158
BB29 VSS149
BB6 VSS152
BB5 VSS151
NCTFVSS11
NCTFVSS9
NCTFVSS8
NCTFVSS10
NCTFVSS7
NCTFVSS6
C2
BT36 VSS298
BT35 VSS219
BT4 VSS217
BR58 VSS211
GND
BGA1140
GND
U3301M
BGA1440
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AW1 VSS122
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AU33 VSS114
AU12 VSS113
AU11 VSS112
AU10 VSS111
AU9 VSS119
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AU7 VSS117
AU6 VSS116
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AT29 VSS108
AT6 VSS110
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AR37 VSS104
AR14 VSS101
AR13 VSS100
AR5 VSS107
AR4 VSS106
AR3 VSS103
AR2 VSS102
AR1 VSS99
AP34 VSS96
AP33 VSS95
AP12 VSS94
AP11 VSS93
AP10 VSS92
AP9 VSS98
AP8 VSS97
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AN29 VSS88
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AN7 VSS90
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AM12 VSS80
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AM4 VSS85
AM3 VSS82
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AM1 VSS79
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AL7 VSS76
AL4 VSS75
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AK29 VSS67
AK4 VSS69
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AJ37 VSS62
AJ6 VSS66
AJ5 VSS65
AJ4 VSS64
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AJ2 VSS60
AJ1 VSS59
AH34 VSS57
AH33 VSS56
AH12 VSS55
AH6 VSS58
AG30 VSS51
AG29 VSS50
AG11 VSS49
AG10 VSS48
AG8 VSS54
AG7 VSS53
AG6 VSS52
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AF13 VSS43
AF12 VSS42
AF4 VSS47
AF3 VSS46
AF2 VSS45
AF1 VSS41
AE34 VSS40
AE33 VSS39
AE6 VSS38
AD30 VSS29
AD29 VSS32
AD12 VSS31
AD11 VSS30
AD10 VSS37
AD9 VSS36
AD8 VSS35
AD7 VSS34
AD6 VSS33
AC37 VSS27
AC14 VSS26
AC6 VSS28
AC5 VSS25
AC4 VSS24
AC3 VSS23
AC2 VSS22
AC1 VSS21
AB34 VSS20
AB33 VSS19
AB6 VSS18
AA30 VSS16
AA29 VSS15
AA12 VSS14
AA10 VSS11
AA9 VSS10
AA8 VSS9
AA7 VSS8
AA6 VSS7
AA5 VSS6
AA4 VSS5
AA3 VSS4
AA2 VSS3
AA1 VSS2
AA0 VSS12
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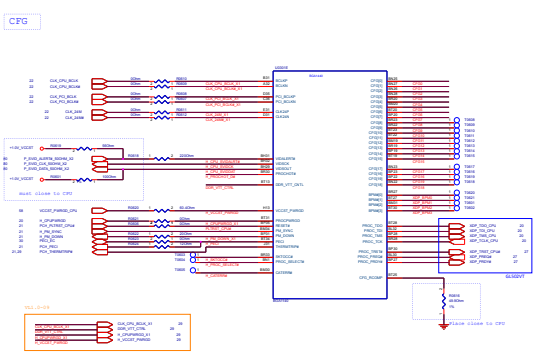
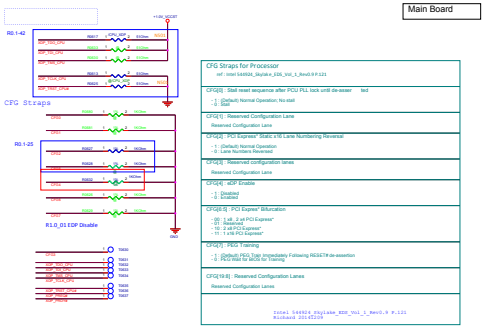
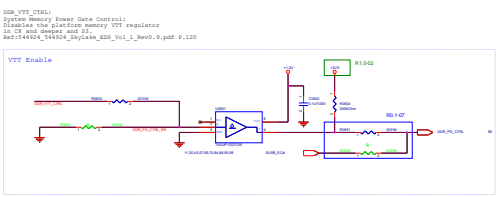
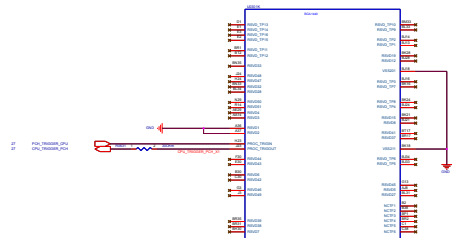
A4 NCTFVSS3
A3 NCTFVSS1
GND
BGA1140
GND


CFG
must close to CPU
Place close to CPU

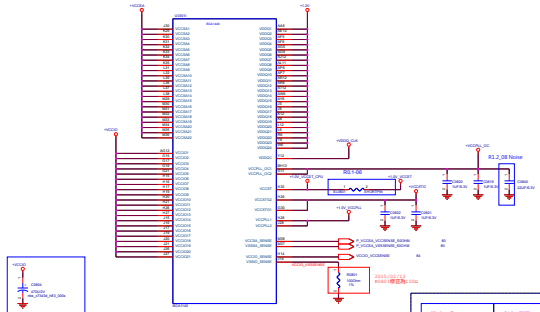

Main Board
CFG Straps
R1.0_01 EDP Disable
CFG Straps for Processor
ref : Intel 544924_Skylake_4S6_Vol_1_Rev0.9 P.121
CFG[0] : Stall reset sequence after PCU PLL lock until de-asser ted
- 1 : (Default) Normal Operation; No stall
- 0 : Stall
CFG[1] : Reserved Configuration Lane
Reserved Configuration Lane
CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed
CFG[3] : Reserved configuration lanes
Reserved Configuration Lane
CFG[4] : eDP Enable
- 1 : Disabled
- 0 : Enabled
CFG[6:5] : PCI Express* Bifurcation
- 00 : 1 x8, 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*
CFG[7] : PEG Training
- 1 : (Default) PEG Train immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training
CFG[19:8] : Reserved Configuration Lanes
Reserved Configuration Lanes
Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121
Released 2015/12/09

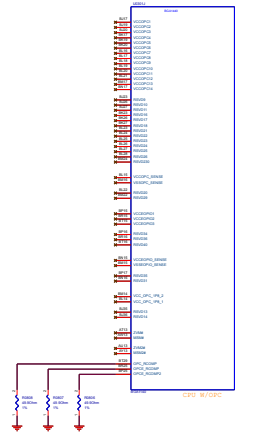

DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120
VTT Enable
R1.0-02
R1.1-27
CPU SIDEBAND SIGNALS
R1.1-11



Main Board

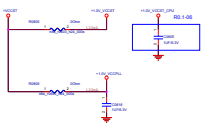
OPC Power Rails



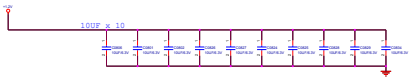


Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	+1.0V_VCCSFR
			+1.0V_VCCPLL
	+1.2V	+VDDQ_CLK	+VDDQ_CLK
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

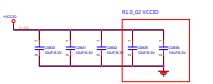
+1.0V_VCCST/+1.0V_VCCPLL
DECAPS Place Back Side (TOP)



+VDDQ DECAPS Place Back Side (TOP)

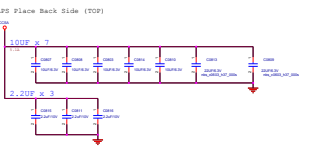


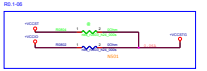
+VCCIO DECAPS Place Back Side (TOP)



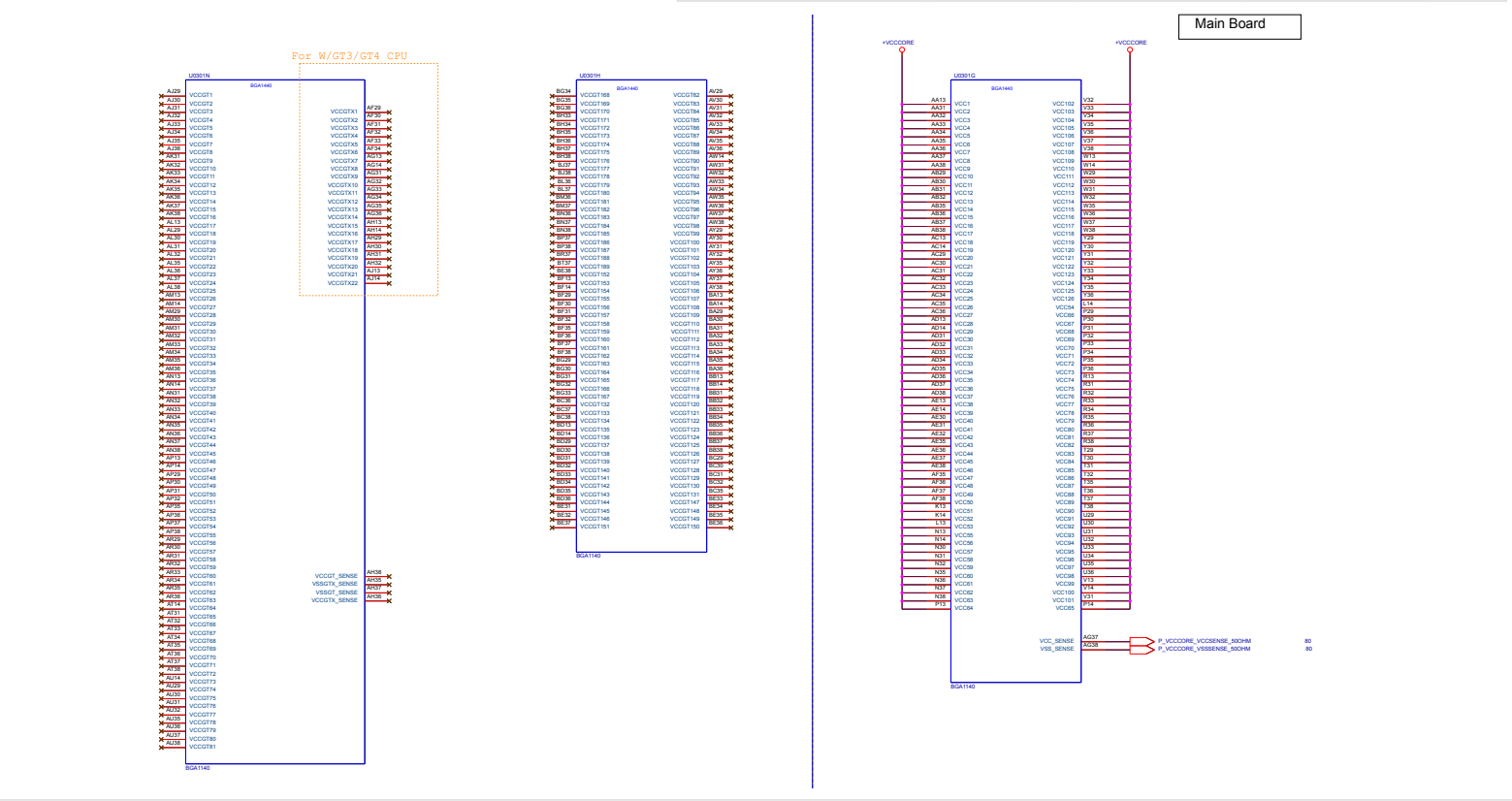
+VDDQ_CLK DECAPS Place Back Side (TOP)

+VCCSA DECAPS Place Back Side (TOP)



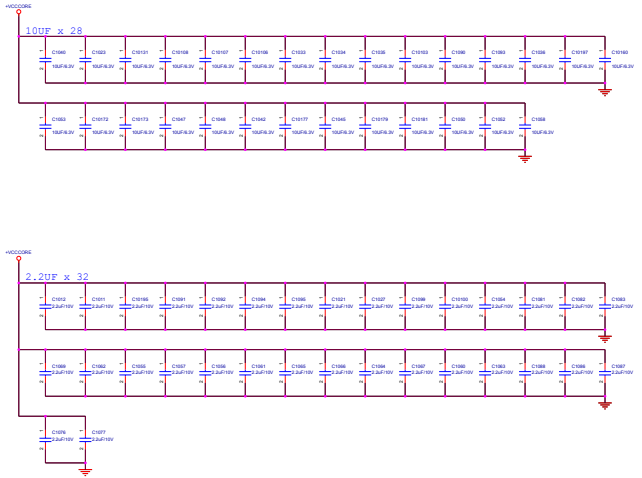


Volume Segment
+VCCIO is supplied +1.0V2 (shared with +VCCSTG)


Main Board
For W/GT3/GT4 CPU
U0301N
BGA1440
AJ29 VCCGT1
AJ30 VCCGT2
AJ31 VCCGT3
AJ32 VCCGT4
AJ33 VCCGT5
AJ34 VCCGT6
AJ35 VCCGT7
AJ36 VCCGT8
AK31 VCCGT9
AK32 VCCGT10
AK33 VCCGT11
AK34 VCCGT12
AK35 VCCGT13
AK36 VCCGT14
AK37 VCCGT15
AK38 VCCGT16
AL13 VCCGT17
AL29 VCCGT18
AL30 VCCGT19
AL31 VCCGT20
AL32 VCCGT21
AL35 VCCGT22
AL36 VCCGT23
AL37 VCCGT24
AL38 VCCGT25
AM13 VCCGT26
AM14 VCCGT27
AM29 VCCGT28
AM30 VCCGT29
AM31 VCCGT30
AM32 VCCGT31
AM33 VCCGT32
AM34 VCCGT33
AM35 VCCGT34
AM36 VCCGT35
AN13 VCCGT36
AN14 VCCGT37
AN31 VCCGT38
AN32 VCCGT39
AN33 VCCGT40
AN34 VCCGT41
AN35 VCCGT42
AN37 VCCGT43
AN38 VCCGT44
AP13 VCCGT45
AP14 VCCGT46
AP29 VCCGT47
AP30 VCCGT48
AP31 VCCGT49
AP32 VCCGT50
AP33 VCCGT51
AP35 VCCGT52
AP36 VCCGT53
AP37 VCCGT54
AP38 VCCGT55
AR29 VCCGT56
AR30 VCCGT57
AR31 VCCGT58
AR32 VCCGT59
AR33 VCCGT60
AR34 VCCGT61
AR35 VCCGT62
AR36 VCCGT63
AT14 VCCGT64
AT31 VCCGT65
AT32 VCCGT66
AT33 VCCGT67
AT34 VCCGT68
AT35 VCCGT69
AT36 VCCGT70
AT37 VCCGT71
AT38 VCCGT72
AU14 VCCGT73
AU29 VCCGT74
AU30 VCCGT75
AU31 VCCGT76
AU32 VCCGT77
AU35 VCCGT78
AU36 VCCGT79
AU37 VCCGT80
AU38 VCCGT81
BGA1140
AF29 VCCGTX1
AF30 VCCGTX2
AF31 VCCGTX3
AF32 VCCGTX4
AF33 VCCGTX5
AF34 VCCGTX6
AG11 VCCGTX7
AG14 VCCGTX8
AG31 VCCGTX9
AG32 VCCGTX10
AG33 VCCGTX11
AG34 VCCGTX12
AG35 VCCGTX13
AG36 VCCGTX14
AH11 VCCGTX15
AH14 VCCGTX16
AH29 VCCGTX17
AH30 VCCGTX18
AH31 VCCGTX19
AH32 VCCGTX20
AJ13 VCCGTX21
AJ14 VCCGTX22
AH38 VCCGT_SENSE
AH35 VSSGTX_SENSE
AH37 VSSGT_SENSE
AH36 VCCGTX_SENSE
U0301H
BGA1440
BG34 VCCGT168
BG35 VCCGT169
BG36 VCCGT170
BH33 VCCGT171
BH34 VCCGT172
BH35 VCCGT173
BH36 VCCGT174
BH37 VCCGT175
BH38 VCCGT176
BJ37 VCCGT177
BJ38 VCCGT178
BL36 VCCGT179
BL37 VCCGT180
BM36 VCCGT181
BM37 VCCGT182
BN36 VCCGT183
BN37 VCCGT184
BN38 VCCGT185
BP37 VCCGT186
BP38 VCCGT187
BR37 VCCGT188
BT37 VCCGT189
BE38 VCCGT152
BF13 VCCGT153
BF14 VCCGT154
BF25 VCCGT155
BF30 VCCGT156
BF31 VCCGT157
BF32 VCCGT158
BF33 VCCGT159
BF34 VCCGT160
BF35 VCCGT161
BF36 VCCGT162
BF37 VCCGT163
BG30 VCCGT164
BG31 VCCGT165
BG32 VCCGT166
BG33 VCCGT167
BC34 VCCGT132
BC37 VCCGT133
BC38 VCCGT134
BD13 VCCGT135
BD14 VCCGT136
BD25 VCCGT137
BD30 VCCGT138
BD31 VCCGT139
BD32 VCCGT140
BD33 VCCGT141
BD34 VCCGT142
BD35 VCCGT143
BD36 VCCGT144
BE31 VCCGT145
BE32 VCCGT146
BE37 VCCGT151
AV29 VCCGT82
AV30 VCCGT83
AV31 VCCGT84
AV32 VCCGT85
AV33 VCCGT86
AV34 VCCGT87
AV35 VCCGT88
AV36 VCCGT89
AW14 VCCGT90
AW31 VCCGT91
AW32 VCCGT92
AW33 VCCGT93
AW34 VCCGT94
AW35 VCCGT95
AW36 VCCGT96
AW37 VCCGT97
AW38 VCCGT98
AY30 VCCGT99
AY31 VCCGT100
AY32 VCCGT101
AY33 VCCGT102
AY35 VCCGT103
AY36 VCCGT104
AY37 VCCGT105
AY38 VCCGT106
BA13 VCCGT107
BA14 VCCGT108
BA30 VCCGT109
BA31 VCCGT110
BA32 VCCGT111
BA33 VCCGT112
BA34 VCCGT113
BA35 VCCGT114
BA36 VCCGT115
BB36 VCCGT116
BB37 VCCGT117
BB14 VCCGT118
BB31 VCCGT119
BB32 VCCGT120
BB33 VCCGT121
BB34 VCCGT122
BB35 VCCGT123
BB37 VCCGT124
BB38 VCCGT125
BC29 VCCGT126
BC30 VCCGT127
BC31 VCCGT128
BC32 VCCGT129
BC33 VCCGT130
BC35 VCCGT131
BE33 VCCGT147
BE34 VCCGT148
BE35 VCCGT149
BE36 VCCGT150
BGA1140
+VCCCORE
U0301G
BGA1440
AA13 VCC1
AA31 VCC2
AA32 VCC3
AA33 VCC4
AA34 VCC5
AA35 VCC6
AA36 VCC7
AA37 VCC8
AA38 VCC9
AB29 VCC10
AB30 VCC11
AB31 VCC12
AB32 VCC13
AB35 VCC14
AB36 VCC15
AB37 VCC16
AB38 VCC17
AC13 VCC18
AC14 VCC19
AC29 VCC20
AC30 VCC21
AC31 VCC22
AC32 VCC23
AC33 VCC24
AC34 VCC25
AC35 VCC26
AC36 VCC27
AD13 VCC28
AD14 VCC29
AD31 VCC30
AD32 VCC31
AD33 VCC32
AD34 VCC33
AD35 VCC34
AD36 VCC35
AD37 VCC36
AD38 VCC37
AE13 VCC38
AE14 VCC39
AE30 VCC40
AE31 VCC41
AE32 VCC42
AE35 VCC43
AE36 VCC44
AE37 VCC45
AE38 VCC46
AF35 VCC47
AF36 VCC48
AF37 VCC49
AF38 VCC50
K13 VCC51
K14 VCC52
L13 VCC53
N13 VCC55
N14 VCC56
N30 VCC57
N31 VCC58
N32 VCC59
N35 VCC60
N36 VCC61
N37 VCC62
N38 VCC63
P13 VCC64
VCC103 Y33
VCC104 Y34
VCC105 Y35
VCC106 Y36
VCC107 Y37
VCC108 Y38
VCC109 W13
VCC110 W14
VCC111 W29
VCC112 W30
VCC113 W31
VCC114 W32
VCC115 W35
VCC116 W36
VCC117 W37
VCC118 W38
VCC119 Y29
VCC120 Y30
VCC121 Y31
VCC122 Y32
VCC123 Y33
VCC124 Y34
VCC125 Y35
VCC126 Y36
VCC54 L14
VCC66 P29
VCC67 P30
VCC68 P31
VCC69 P32
VCC70 P33
VCC71 P34
VCC72 P35
VCC73 P36
VCC74 R13
VCC75 R31
VCC76 R32
VCC77 R33
VCC78 R34
VCC79 R35
VCC80 R36
VCC81 T29
VCC82 T30
VCC83 T31
VCC84 T32
VCC85 T35
VCC86 T36
VCC87 T37
VCC88 T38
VCC89 U29
VCC90 U30
VCC91 U31
VCC92 U32
VCC93 U33
VCC94 U34
VCC95 U35
VCC96 U36
VCC97 U37
VCC98 V13
VCC99 V14
VCC100 V31
VCC101 V32
VCC65
BGA1140
AG37
AG38
VCC_SENSE
VSS_SENSE
P_VCCCORE_VCCSENSE_50OHM
P_VCCCORE_VSSSENSE_50OHM
80
80

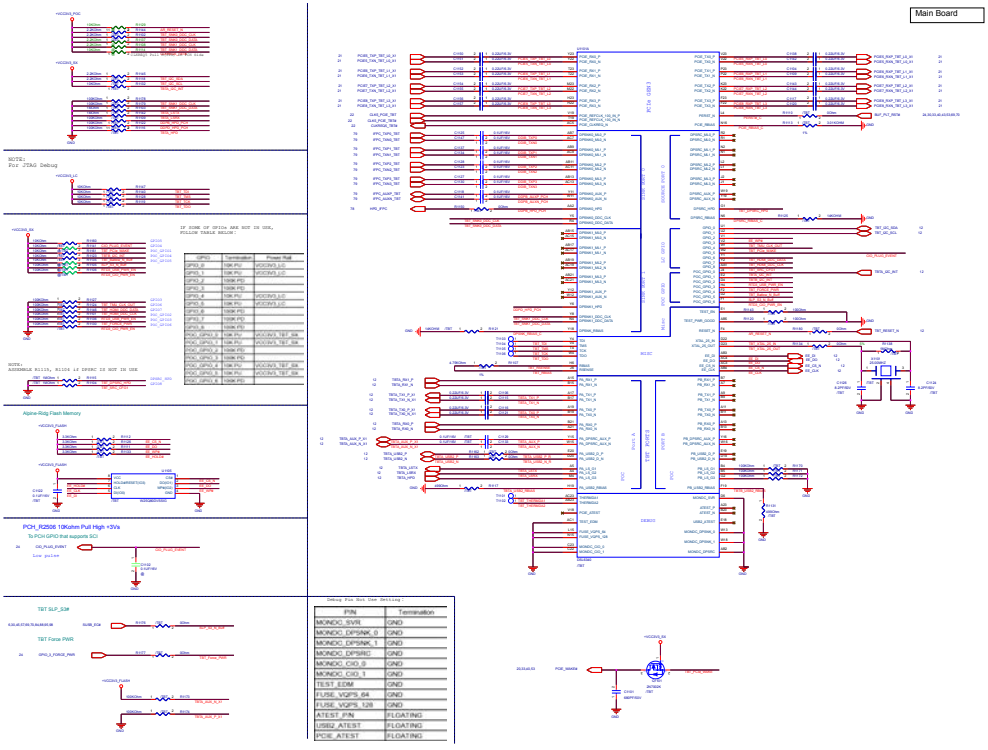
Main Board

+VCCORE DECAPS Place Back Side (TOP)

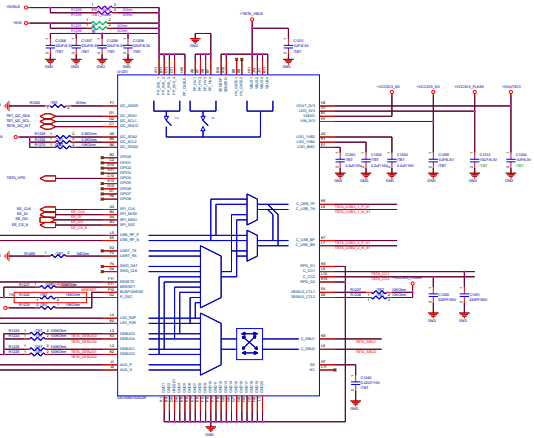


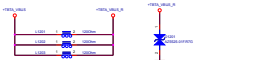
+VCCGT DECAPS Place Back Side (TOP)

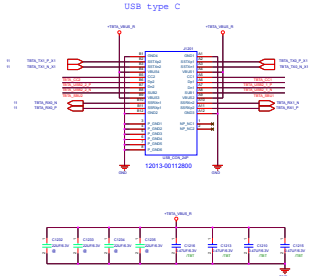
Main Board

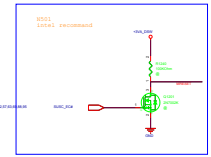

NOTE:
For JTAG Debug
IF SOME OF GPIOs ARE NOT IN USE, FOLLOW TABLE BELOW :
NOTE:
ASSEMBLE R1115, R1104 if DFXHC IS NOT IN USE
Alpine-Ridg Flash Memory
PCH_R2508 10Kohm Pull High +3Vs
To PCH GPIO that supports SCI
Low pulse
TBT SLP_S3#
TBT Force PWR
Debug Pin Not Use Setting :
PIN
Termination
MONDO_SVR
GND
MONDO_DPSNK_0
MONDO_DPSNK_1
MONDO_DPSRC
MONDO_CIO_0
MONDO_CIO_1
TEST_EDM
FUSE_VQPS_64
FUSE_VQPS_128
ATEST_PIN
FLOATING
USB2_ATEST
PCIE_ATEST

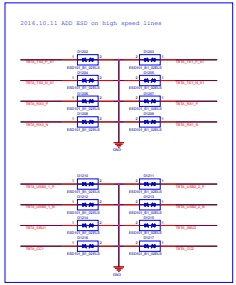
Main Board

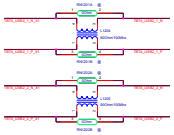


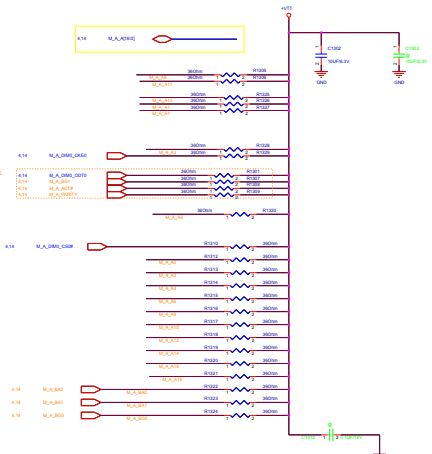


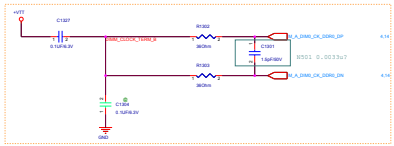

USB type C
12013-0011200


R501
Intel recommand

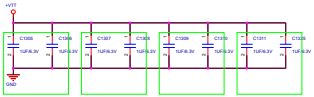

ESD-Protection
2016.10.11 ADD ESD on high speed lines

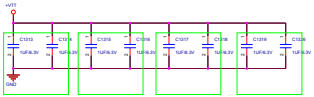


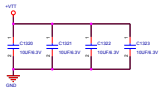


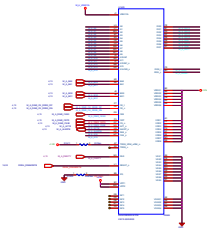


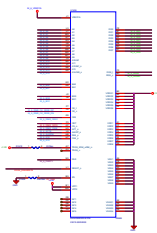
3.Page13.Delete C1309 and Clock Pull up power change from +1.2V to +0.6V -20121212

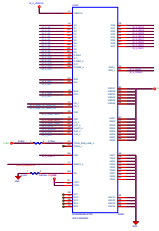


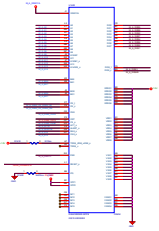


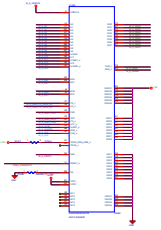


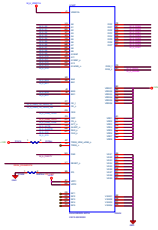


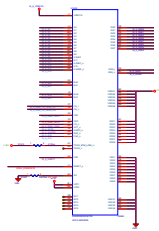


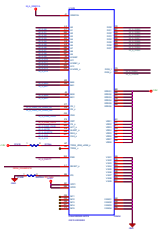


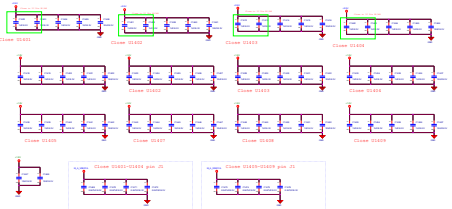


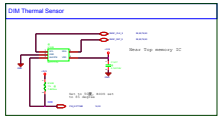


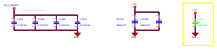






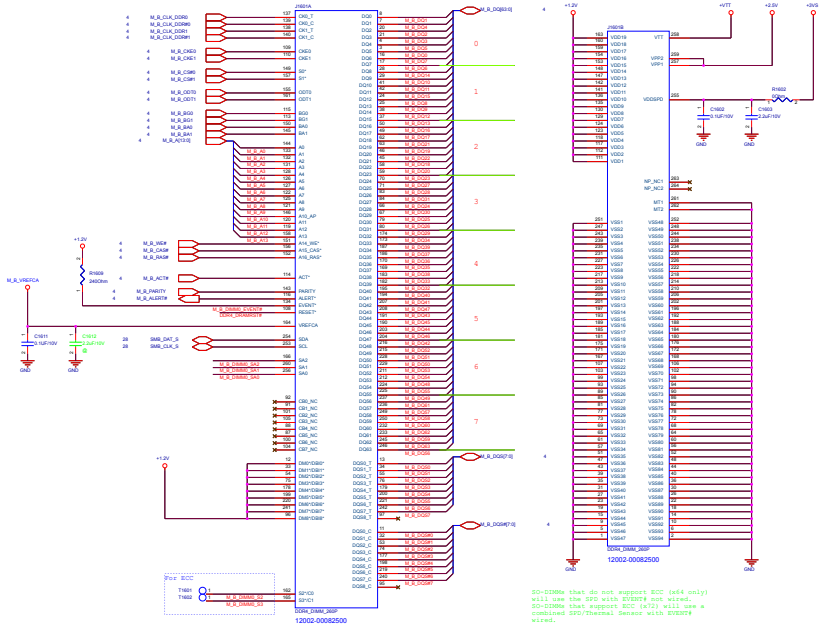


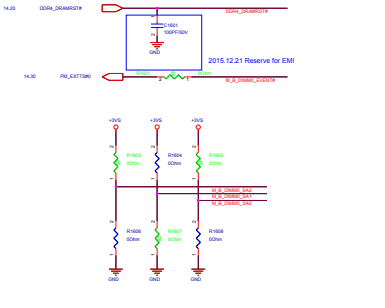

DIM Thermal Sensor
Near Top memory IC



SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

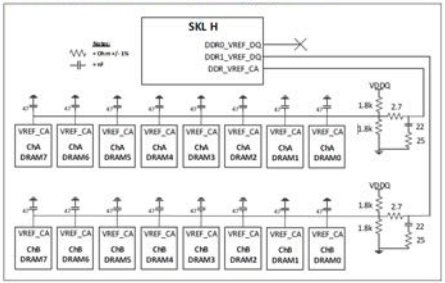
Main Board



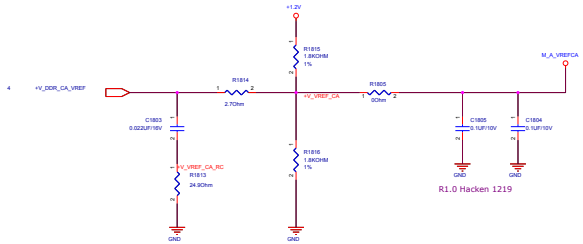


Main Board

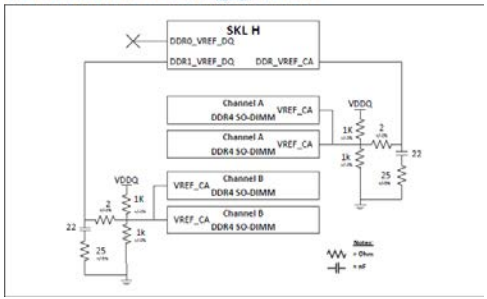
Figure 4-27. SKL H DDR4/DDR4-RS x8 Memory Down V_{REF-CA} Overview



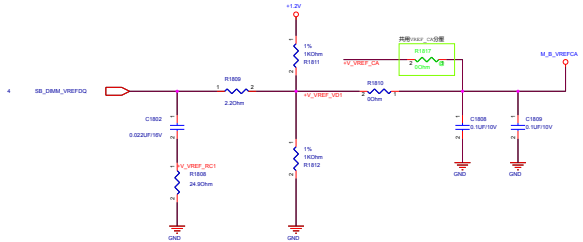
SO-DIMM0 Vref



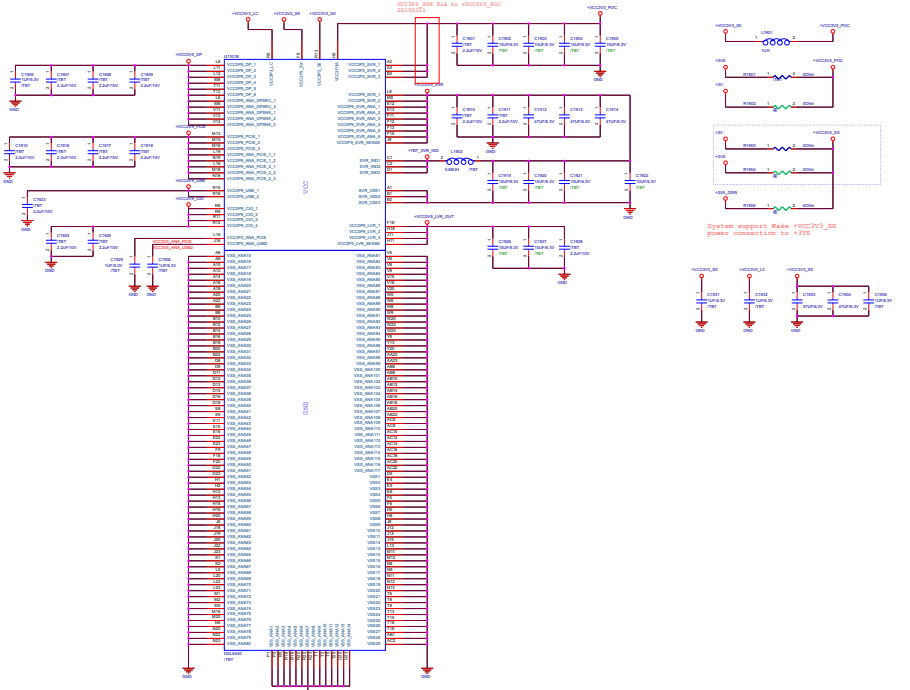
SKL H DDR4/DDR4-RS SO-DIMM V_{REF-CA} Overview

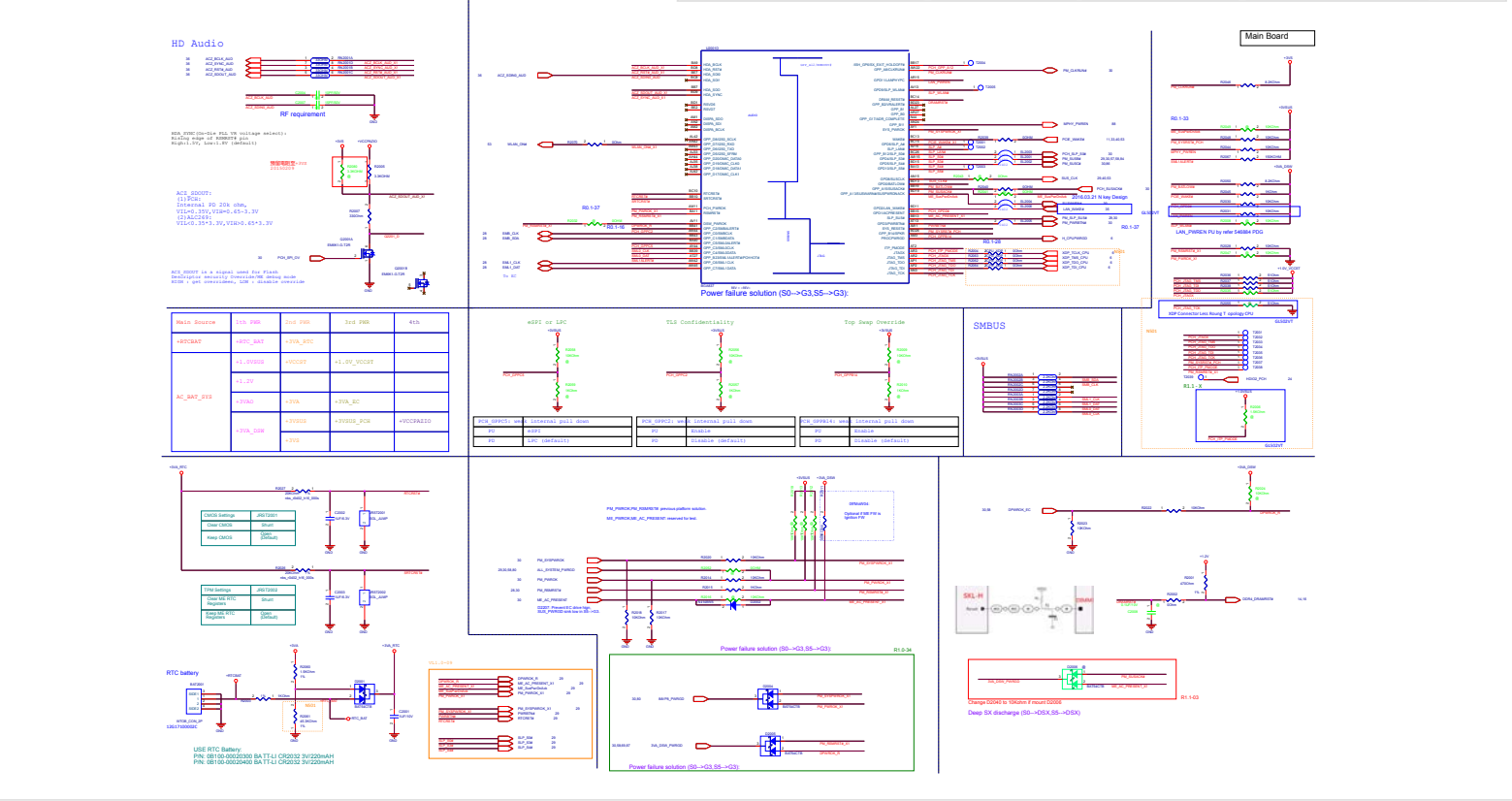


SO-DIMM1 Vref



Main Board


VCC3P3_SVR Fix to +VCC3V3_PDC
20150331
System support Make +VCC3V3_SX
power connection to +3VS

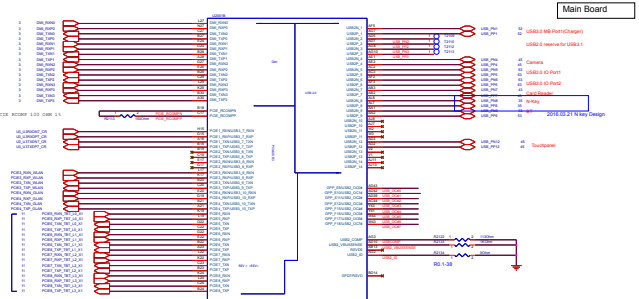

HD Audio
RF requirement
Power failure solution (S0-->G3,S5-->G3):
Main Board
Main Source
+VCCGAVT
AC_BAT_SYS
+3VA_DSW
+3VPCU
+3VA
+VCCSPI
+1.0VSUS
+1.2V
+3VSUS
+VCCSFRTC
+5VSUS
+3VSUS_PCH
eSPI or LPC
TLS Confidentiality
Top Swap Override
SMBUS
RTC battery
USE RTC Battery:
P/N: 0B100-00020300 BATT-LI CR2032 3V/220mAH
PIN: 0B100-00020400 BATT-LI CR2032 3V/220mAH
Power failure solution (S0-->G3,S5-->G3):
Deep SX discharge (S0-->DSX,S5-->DSX)

Main Board

PCIE Setting

GL502VM PCIE/SATA Function define
Skylake MM170

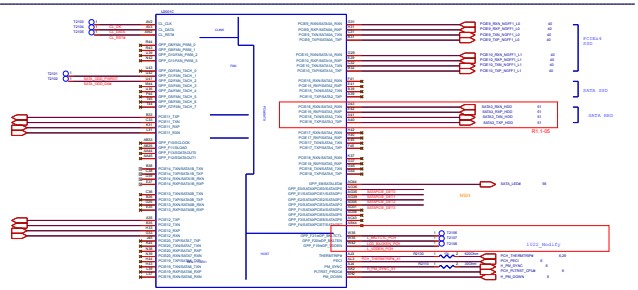
RSVD	MSVD Capabilities	Funcon	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_ID	
02	USB3#02 / SSIC#01		
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3_ID	
06	USB3#06	USB3_ID	
07	USB3#07 / PCIE#01	CardReader_USB3	SRC1
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN	SRC4
11	PCIE#05 / GBE	TBT	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	PCIE*4 SSD SATA SSD	SRC6
16	PCIE#10 / SATA#1		
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	1st HDD	
23			
24			
25			
26			



USB Setting

GL502VM USB Function define
Skylake MM170

USB 2.0	Funcon	USB 3.0	Funcon
USB2_01	USB3.0 MB Port1	USB3_01	MB USB3.0
USB2_02		USB3_02	
USB2_03		USB3_03	
USB2_04	Camera	USB3_04	
USB2_05	USB3.0 IO Port1	USB3_05	USB3.0 IO Port1
USB2_06	USB3.0 IO Port2	USB3_06	USB3.0 IO Port2
USB2_07	CardReader	USB3_07	Card reader
USB2_08	N-Key	USB3_08	
USB2_09	BT		
USB2_10			
USB2_11			
USB2_12			

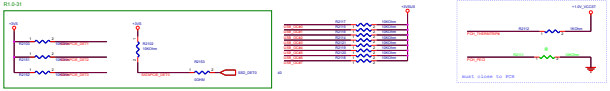


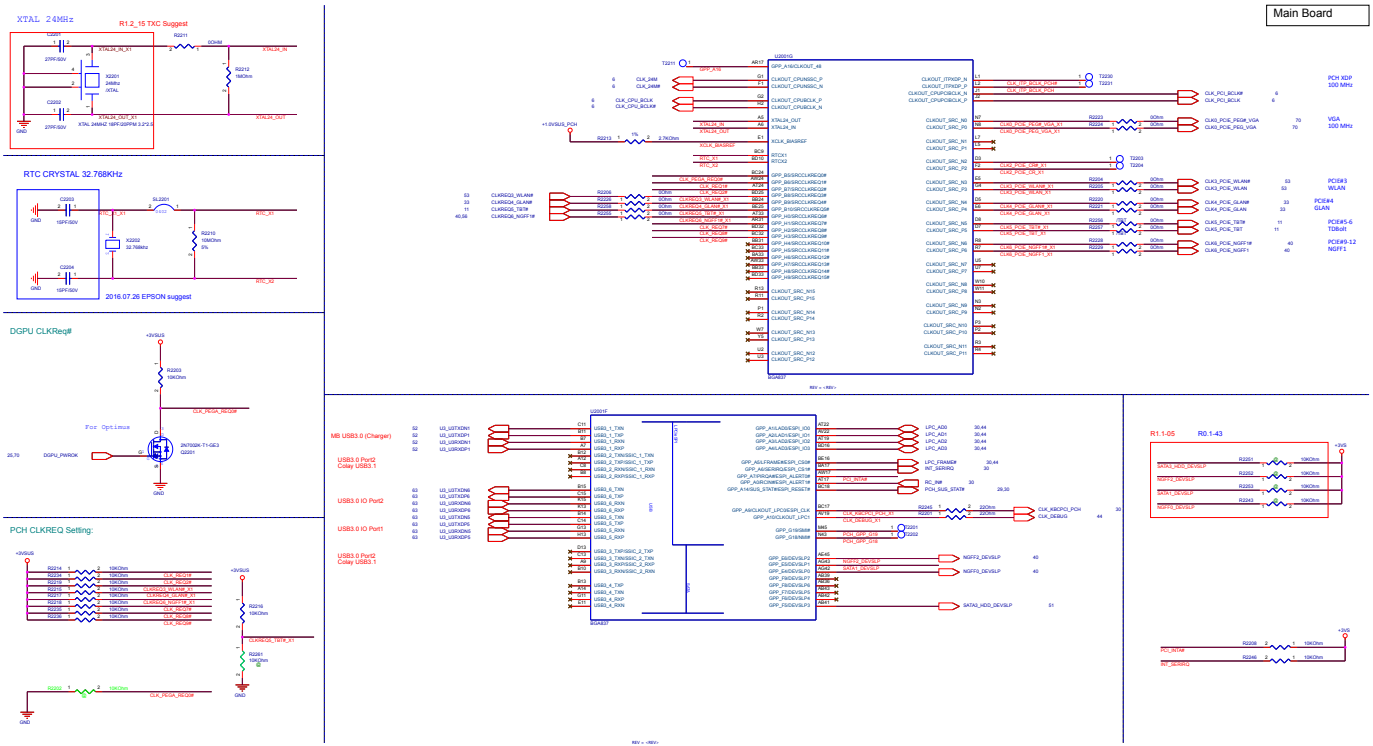
N501VW PCIE/SATA Function define

	Funcon
PCIE-01	
PCIE-02	
PCIE-03	WLAN
PCIE-04	GLAN
PCIE-05	TBT AR
PCIE-06	TBT AR
PCIE-07	TBT AR
PCIE-08	TBT AR
PCIE-09 (SATA-0A)	PCIE SSD
PCIE-10 (SATA-1A)	PCIE SSD
PCIE-11	PCIE SSD
PCIE-12	PCIE SSD

	Funcon
PCIE-13 (SATA-0B)	
PCIE-14 (SATA-1B)	
PCIE-15 (SATA-2)	
PCIE-16 (SATA-3)	HDD
PCIE-17 (SATA-4)	
PCIE-18 (SATA-5)	
PCIE-19 (SATA-6)	
PCIE-20 (SATA-7)	

	Funcon
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	
CLKREQ-3	WLAN
CLKREQ-4	GLAN
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	




Main Board
XTAL 24MHz
R1.2_15 TXC Suggest
RTC CRYSTAL 32.768KHz
2016.07.26 EPSON suggest
DGPU CLKReq#
PCH CLKREQ Setting:
U2001G
U2001F
U2001J
U2001K
U2001H
U2001E
U2001D
U2001C
U2001B
U2001A
Y2201
32.768KHz
R1-05
R0.1-43

Main Board

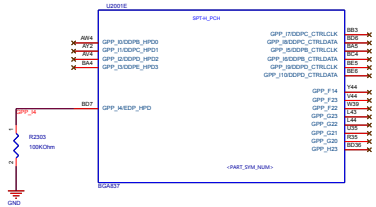
HPD0 to DP

HPD1 to HDMI

HPD2 to TBT

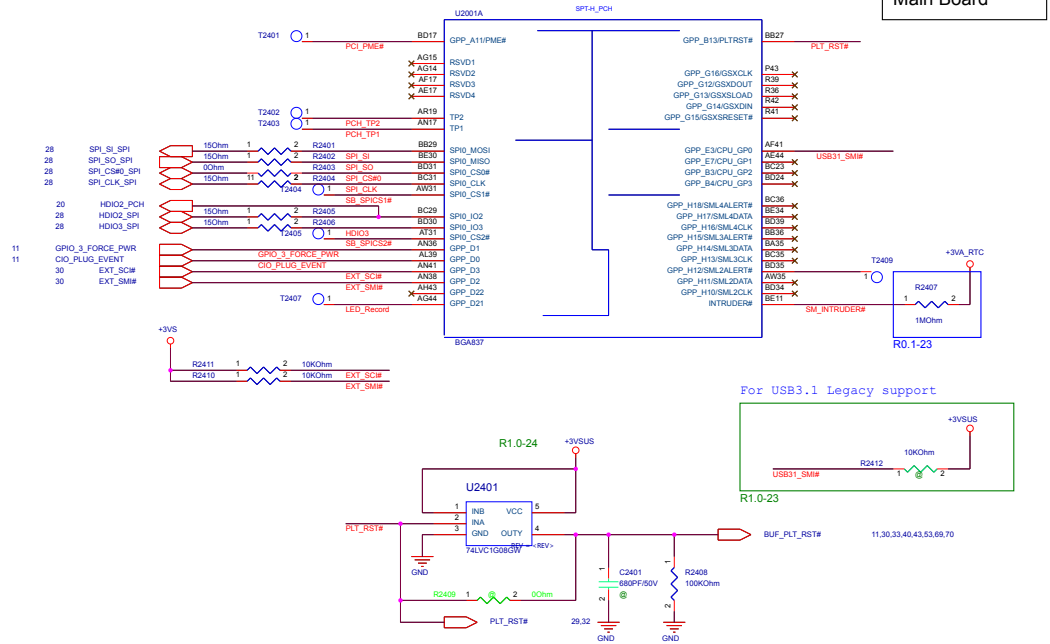
HPD3 to VGA

HPD4 to EDP Panel

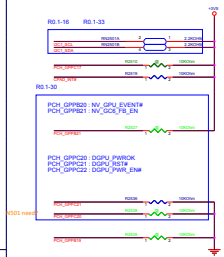


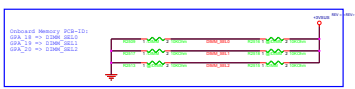
REV = <REV>

Main Board

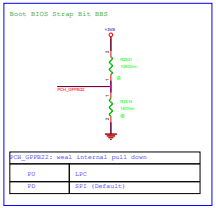

U2001A
SPT-H_PCH
T2401
PCI_PME#
BD17
GPP_A11/PME#
AG15
AG14
AF17
AE17
RSVD1
RSVD2
RSVD3
RSVD4
T2402
T2403
PCH_TP2
PCH_TP1
AR19
AN17
TP2
TP1
28 SPI_SI_SPI
28 SPI_SO_SPI
28 SPI_CS#0_SPI
28 SPI_CLK_SPI
15Ohm
15Ohm
0Ohm
15Ohm
R2401
R2402
R2403
R2404
SPI_SI
SPI_SO
SPI_CS#0
SPI_CLK
T2404
SB_SPICS1#
BB29
BE30
BD31
BC31
AW31
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
20 HDIO2_PCH
28 HDIO2_SPI
28 HDIO3_SPI
15Ohm
15Ohm
R2405
R2406
T2405
HDIO3
SB_SPICS2#
BC29
BD30
AT31
SPI0_IO2
SPI0_IO3
SPI0_CS2#
11 GPIO_3_FORCE_PWR
11 CIO_PLUG_EVENT
30 EXT_SCI#
30 EXT_SMI#
GPIO_3_FORCE_PWR
CIO_PLUG_EVENT
EXT_SCI#
EXT_SMI#
AN36
AL39
AN41
AN38
AH43
GPP_D1
GPP_D0
GPP_D3
GPP_D2
GPP_D22
T2407
LED_Record
AG44
GPP_D21
BGA837
GPP_B13/PLTRST#
PLT_RST#
BB27
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXSRESET#
P43
R39
R36
R42
R41
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
USB31_SMI#
AF41
AE44
BC23
BD24
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
SMI_INTRUDER#
BC36
BE34
BD39
BB36
BA35
BC35
BD35
AW35
BD34
BE11
T2409
+3VA_RTC
R2407
1MOhm
R0.1-23
+3VS
R2411
R2410
10KOhm
10KOhm
EXT_SCI#
EXT_SMI#
For USB3.1 Legacy support
+3VSUS
10KOhm
R2412
USB31_SMI#
R1.0-23
R1.0-24
+3VSUS
U2401
INB
INA
GND
VCC
OUTY
74LVC1G08GW
PLT_RST#
GND
R2409
0Ohm
PLT_RST#
29,32
GND
C2401
680PF/50V
GND
R2408
100KOhm
GND
BUF_PLT_RST#
11,30,33,40,43,53,69,70

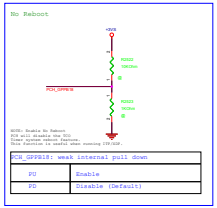
Main Board

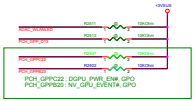


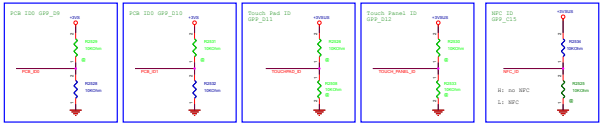


	Micron (8Gb)	Samsung (8Gb)		
	MT52L256M32D1PF-107 WT:B 2133MT/s 1.2V MO-276	K4Z80325BB-HC20 2133MT/s 1.2V FBGA178		
DIMM_SEL0	L	L		
DIMM_SEL1	L	L		
DIMM_SEL2	L	H		

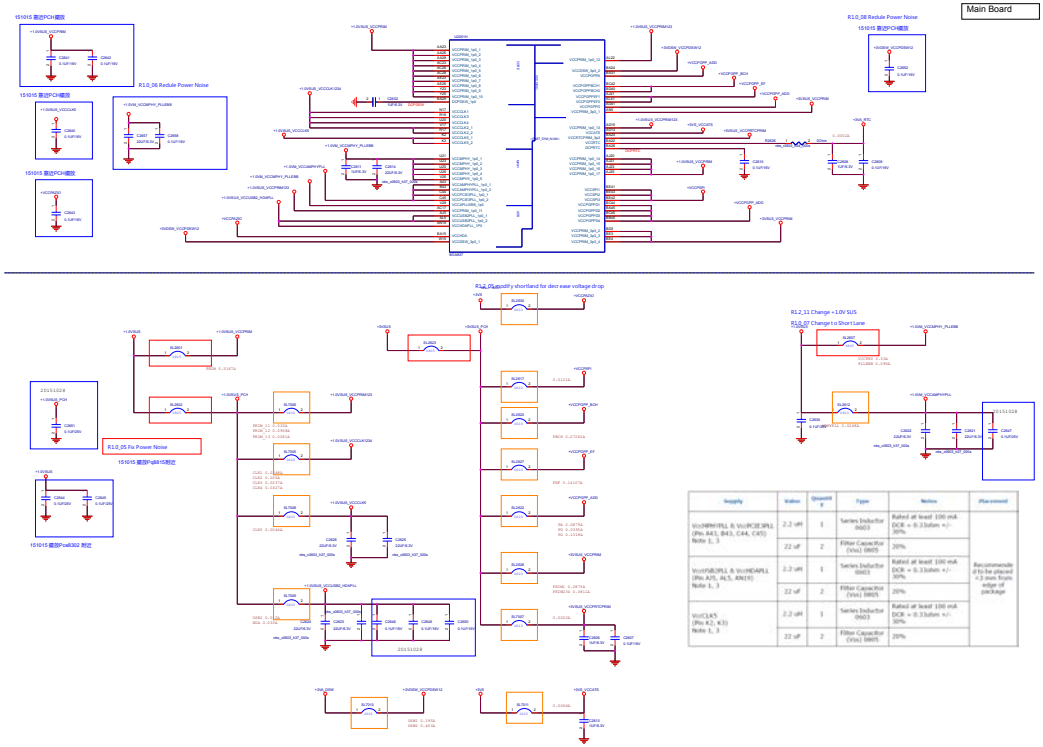






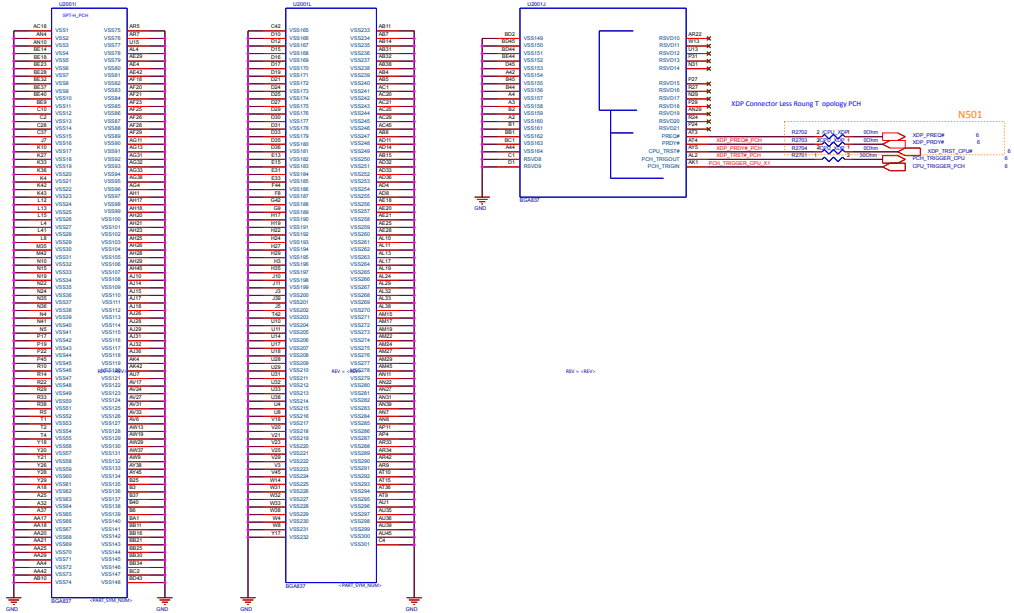


Main Board



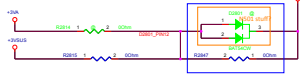
Supply	Value	Quantity	Type	Notes	Placement
VccHPM/PLL & VccPCIE3PLL (Pin A41, B43, C44, C45) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	Recommended to be placed <3 mm from edge of package
	22 uF	2	Filter Capacitor (Via) 0805	20%	
VccUSB3PLL & VccHDAPLL (Pin A75, AL5, AN19) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Via) 0805	20%	
VccCLK5 (Pin A2, K3) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Via) 0805	20%	

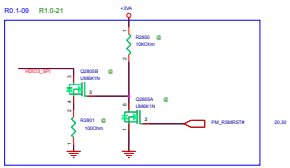
Main Board


U20011
SPT-H_PCH
U20011L
U20012
XDP Connector Less Roung T opology PCH
N501
XDP_PREQ#
XDP_PRDY#
XDP_TEST_CPU#
PCH_TRIGGER_CPU
CPU_TRIGGER_PCH
GND
BGA837

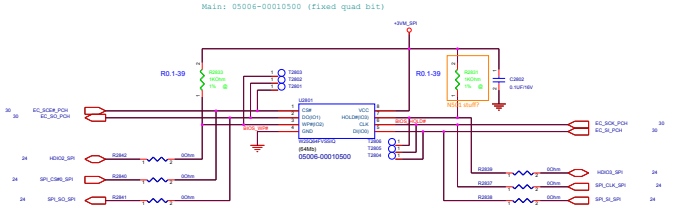
Main Board

SPI Power

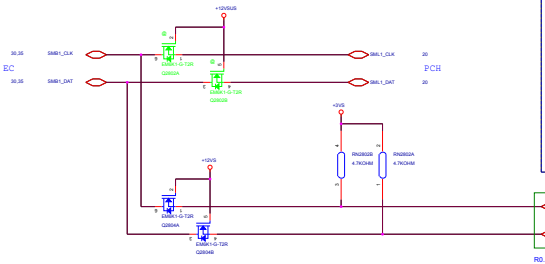




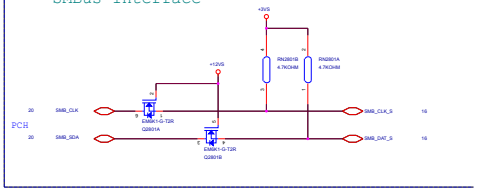
1st SPI ROM



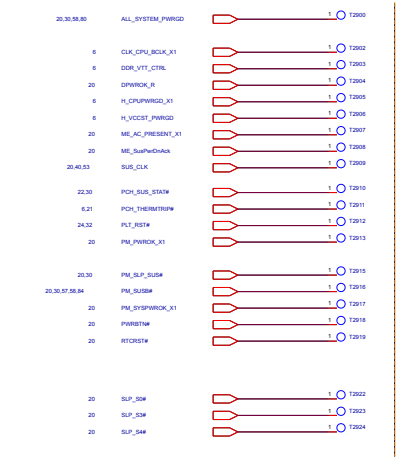
System Management Interface

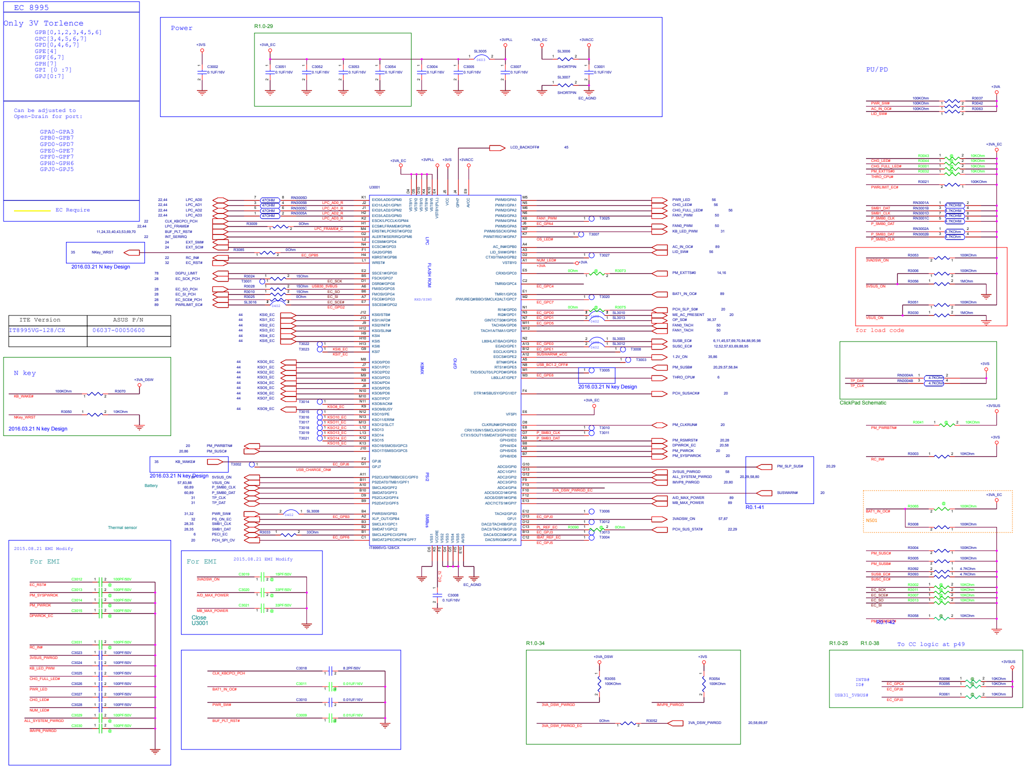


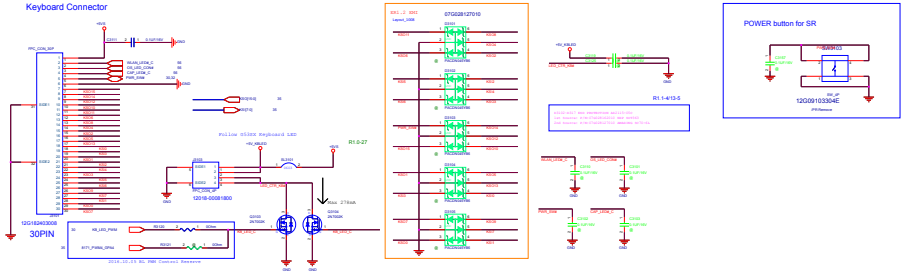
SMBus Interface

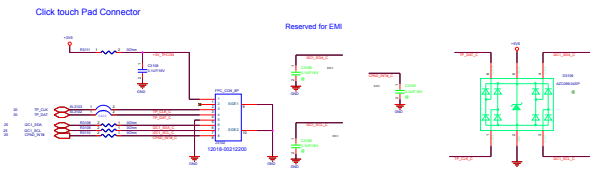


VL1.0-09


20,30,58,80
ALL_SYSTEM_PWRGD
1
T2900
6
CLK_CPU_BCLK_X1
T2902
6
DDR_VTT_CTRL
T2903
20
DPWROK_R
T2904
6
H_CPUPWRGD_X1
T2905
6
H_VCCST_PWRGD
T2906
20
ME_AC_PRESENT_X1
T2907
20
ME_SusPwrDnAck
T2908
20,40,53
SUS_CLK
T2909
22,30
PCH_SUS_STAT#
T2910
6,21
PCH_THERMTRIP#
T2911
24,32
PLT_RST#
T2912
20
PM_PWROK_X1
T2913
20,30
PM_SLP_SUS#
T2915
20,30,57,58,64
PM_SUSB#
T2916
20
PM_SYSPWROK_X1
T2917
20
PWRBTN#
T2918
20
RTCRST#
T2919
20
SLP_S0#
T2922
20
SLP_S3#
T2923
20
SLP_S4#
T2924

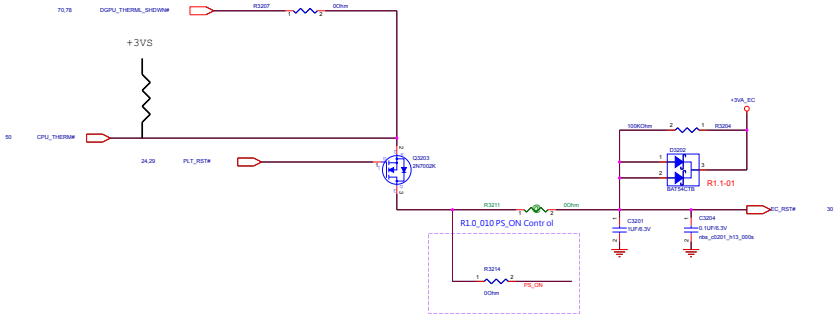

EC 8995
Only 3V Torlence
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
Can be adjusted to
Open-Drain for port:
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5
EC Require
Power
R1.0-29
ITE Version
ASUS P/N
IT8995VG-128/CX
06037-00050600
N key
2016.03.21 N key Design
U3001
IT8995VG-128/CX
LCD_BACKOFF#
2015.08.21 EMI Modify
For EMI
Close U3001
Thermal sensor
Battery
PU/PD
for load code
ClickPad Schematic
R0.1-41
R0.1-42
R1.0-34
R1.0-25
R1.0-38
To CC logic at p49


Keyboard Connector
12G18240308
30PIN
Follow 65300 Keyboard LED
R1.0-27
07G028127010
R1.1-413-5
POWER button for SR
12G09103304E

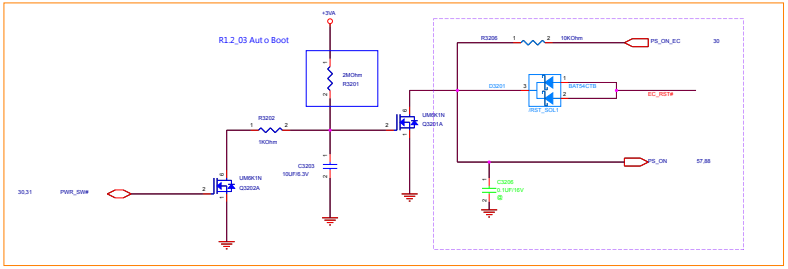

Click touch Pad Connector
Reserved for EMI
12018-0021200

Reset Circuit

Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



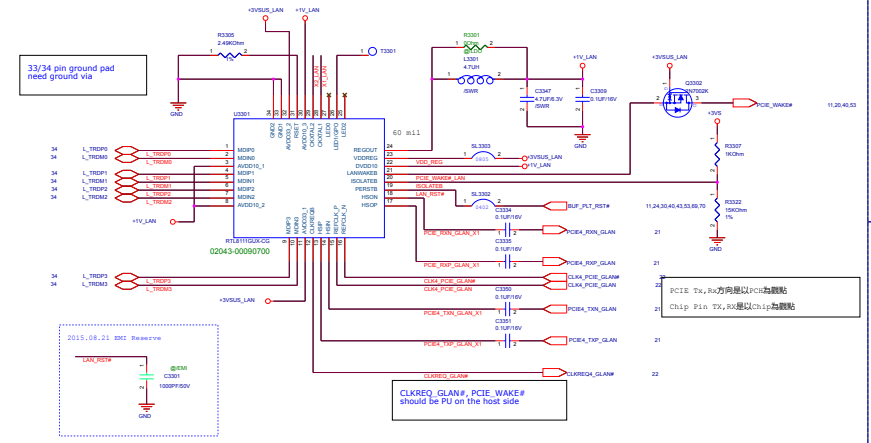
Battery embedded (press pwr_sw 10sec, then reset ec)

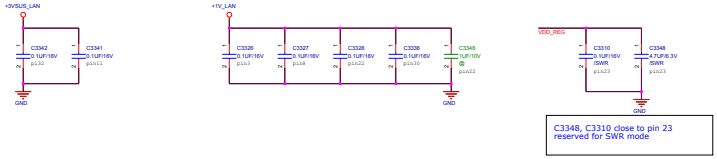


EC power off solution:
Solution1 Mount R3205, D3201/ Unmount R3216
Solution2 Mount R3206/R3216/ Unmount D3201- for reserved 0402 footprint

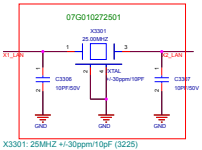
R1.2-65
<Variant Name>

Main Board





R1 2_15 TXC Suggest

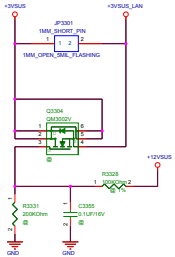


X3301: 25MHZ +/-30ppm/10pF (3225)

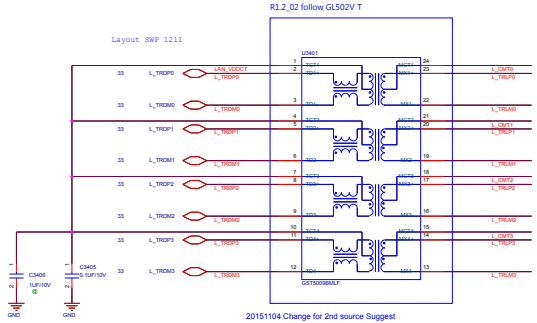
1st: P/N:07G010272501 TXC/7V2500001 1

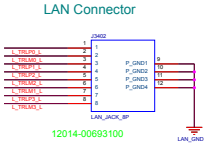
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms



Main Board

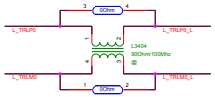


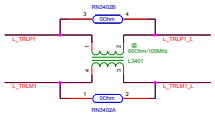


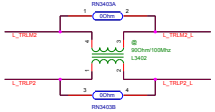
J3402 LAN Jack

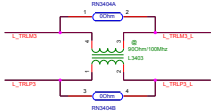
1st Source: P/N:12014-00161700 FOXCONN/JM361 1-NS640003-7H

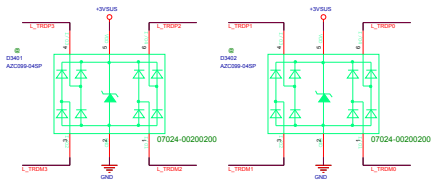
2nd Source: P/N:12014-00035500 SINGA TRON/2RJ1648-000111F







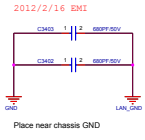


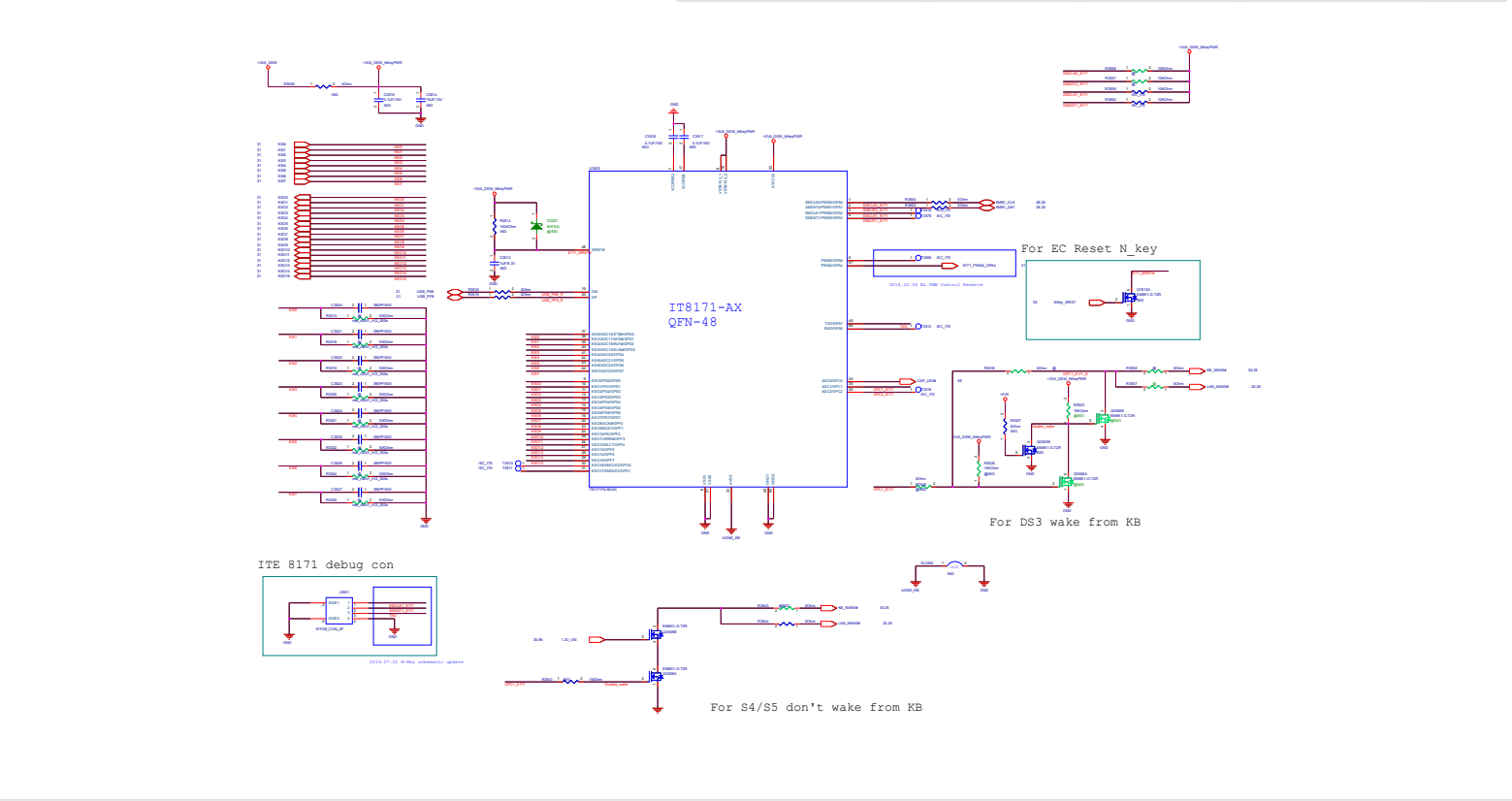


D3401,D3402 ESD Diode

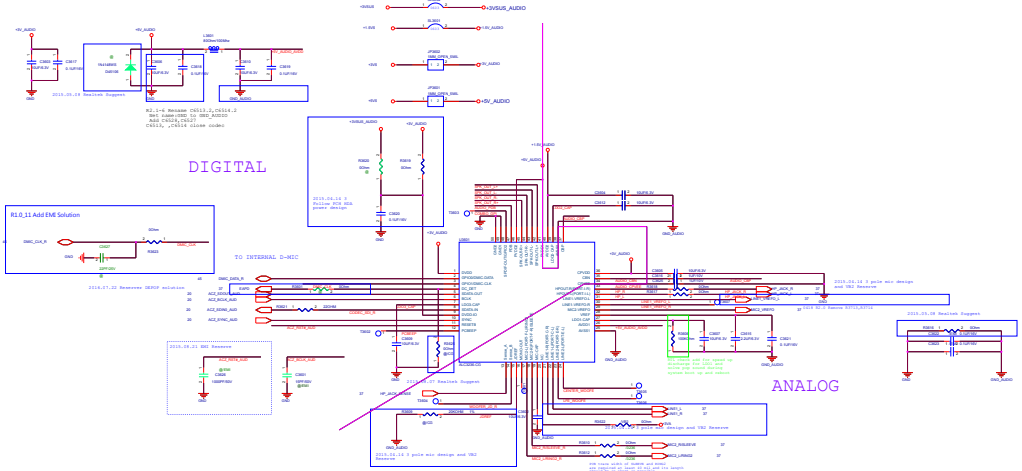
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP ..R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D




IT8171-AX
QFN-48
For EC Reset N_key
For DS3 wake from KB
ITE 8171 debug con
For S4/S5 don't wake from KB

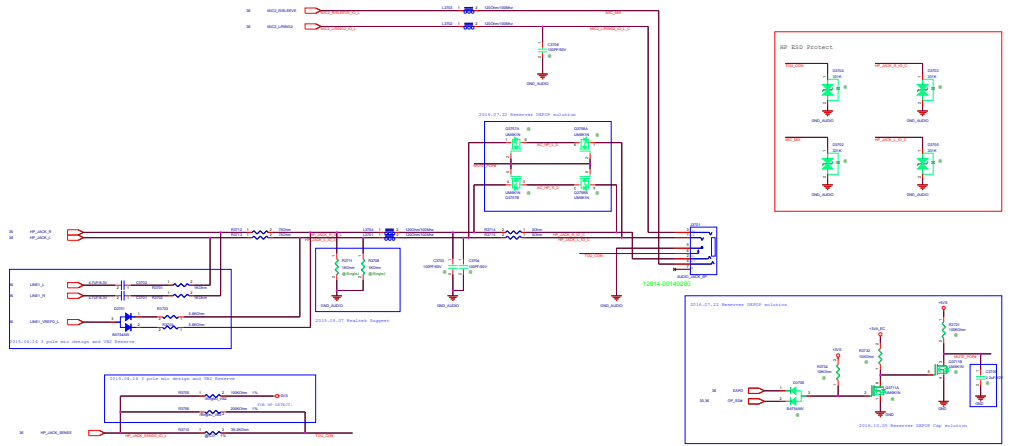
Main Board


DIGITAL
ANALOG
TO INTERNAL D-MIC
R1.0_11 Add EMI Solution
Mute & De-POP Control ??

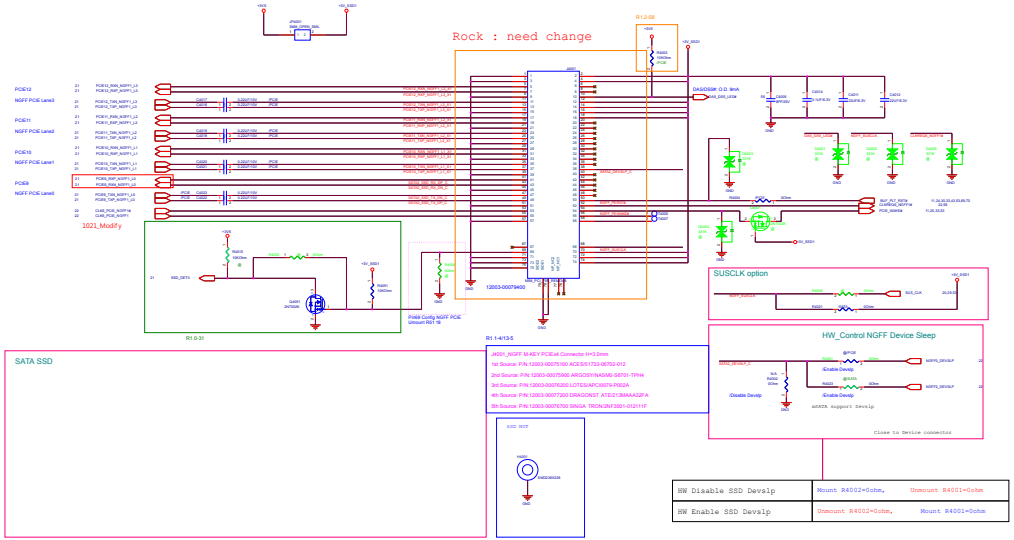
Main Board

Headphone&MIC

HP & MIC Connector

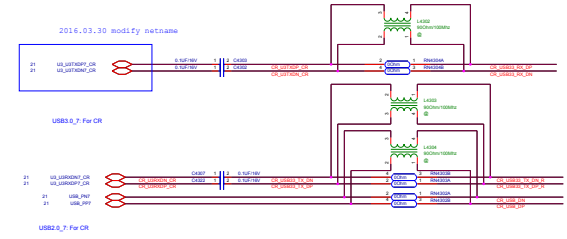


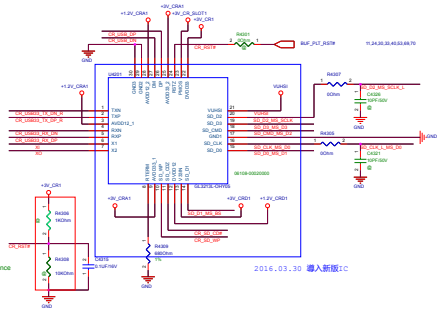
NGFF_SSD


Rock : need change
1021_Modify
SATA SSD
SUSCLK option
HW_Control NGFF Device Sleep
Close to Device connector
HW Disable SSD Devslp
Mount R4002=0ohm,
Unmount R4001=0ohm
HW Enable SSD Devslp
Unmount R4002=0ohm,
Mount R4001=0ohm

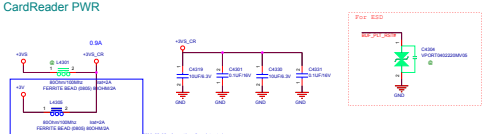
CR I/O Conn. (MB)

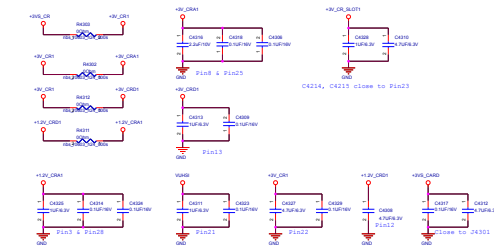
Main Board

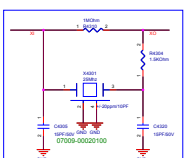




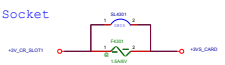
CardReader PWR

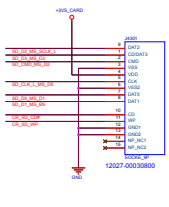




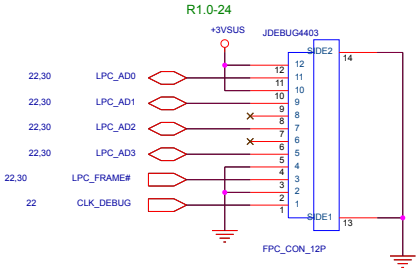


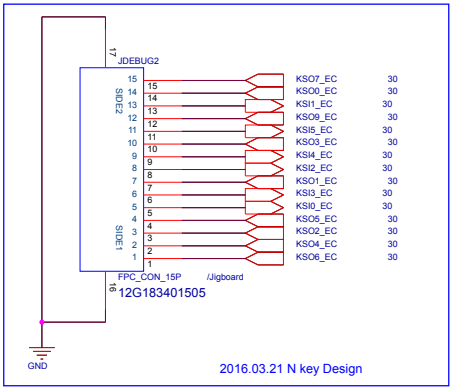
CR Socket

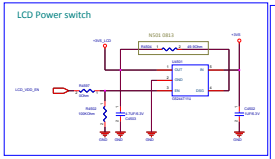


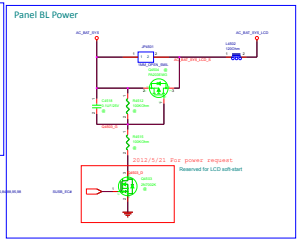


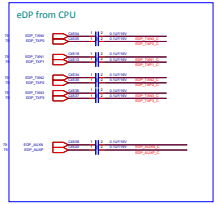
LPC Debug Port

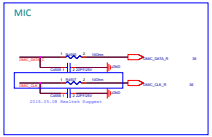


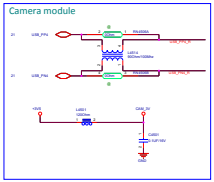


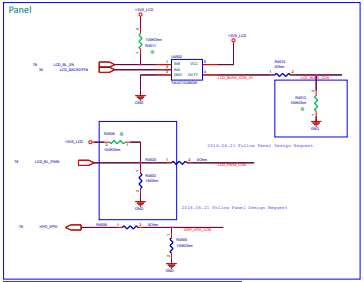

LCD Power switch
N501 0813
+3VS_LCD
+5VS
LCD_VDD_EN
Q502
AO3407
R4802
100KOhm
C4803
4.7UF/6.3V
C4802
0.1UF/6.3V
GND

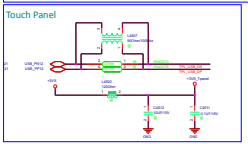

Panel BL Power
AC_BAT_SYS
AC_BAT_SYS_LCD
LX6301
PANEL_BKL_EN
Q4101
AO3400
R4103
100KOhm
C4104
0.1UF/50V
2012/5/21 For power request
Reserved for LCD soft-start
Q4102
AO3400
BLUE_SCA

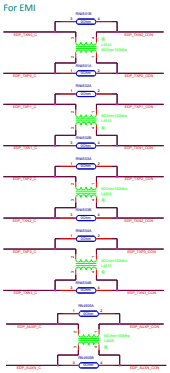

eDP from CPU
EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3
EDP_AUXN
EDP_AUXP
C4838
C4839
C4840
C4841
C4842
C4843
C4844
C4845
C4846
C4847
0.1UF/16V

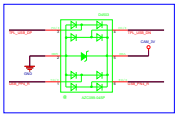

MIC
DMIC_DATA
DMIC_CLK
C4850
2.2UF/16V
L4501
600ohm
DMIC_DATA_R
DMIC_CLK_R
C4851
0.1UF/16V
2015.05.08 Modified Suggest

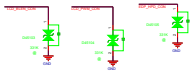

Camera module
USB_FP4
USB_FP4-
R4105BA
L4514
90Ohm/100MHz
R4106BA
USB_FP4_P
USB_FP4_N
+5VS
L4501
120Ohm
CAM_5V
C4852
0.1UF/16V
GND

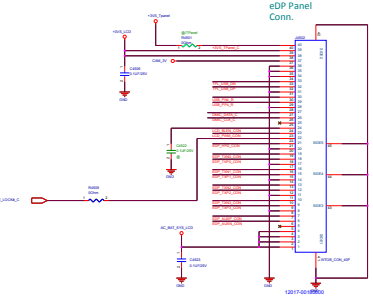

Panel
+3VS_LCD
R4099
100KOhm
R4101
0Ohm
LX6302
LCD_BL_EN
LCD_BACKOFF#
LCD_BKEN_CONN
R4102
100KOhm
R4103
100KOhm
R4098
0Ohm
LCD_BL_PWM
R4100
0Ohm
R4101
100Ohm
2016.06.21 Follow Panel Design Request
2016.06.21 Follow Panel Design Request
HPD_CONN
R4099
10KOhm
GND


Touch Panel
L4502
90Ohm/100MHz
USB_FP4-
USB_FP4+
R4105BA
R4106BA
L4503
120Ohm
+3VS
+3VS_Camer
C4852
0.1UF/16V
C4853
0.1UF/16V
GND


For EMI
R4401BA
R4402BA
R4403BA
R4404BA
R4405BA
R4406BA
R4407BA
R4408BA
R4409BA
R4410BA
R4411BA
R4412BA
L4511
L4512
L4513
L4514
L4515
L4516
L4517
L4518
L4519
L4520
L4521
L4522
600ohm/100MHz
EDP_TXN0_CONN
EDP_TXP0_CONN
EDP_TXN1_CONN
EDP_TXP1_CONN
EDP_TXN2_CONN
EDP_TXP2_CONN
EDP_TXN3_CONN
EDP_TXP3_CONN
EDP_AUXN_CONN
EDP_AUXP_CONN

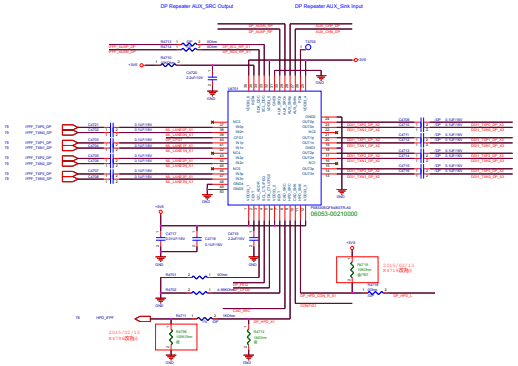

D4503
D4504
D4505
D4506
D4507
D4508
D4509
D4510
PCH_EDP_HPD
CAM_5V
EDP_AUXP_CONN
EDP_AUXN_CONN
2016.10.07. EMI Design Request

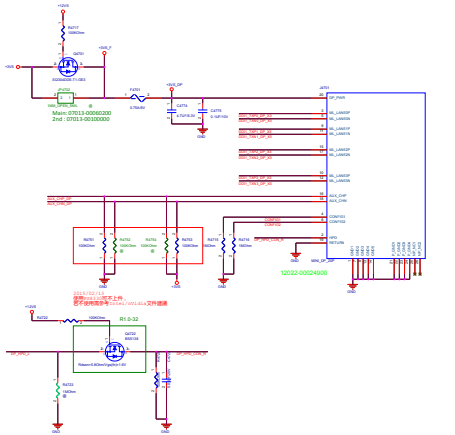

D4503
D4504
D4505
D4506
D4507
D4508
D4509
D4510
EDP_TXN0_CONN
EDP_TXP0_CONN
EDP_TXN1_CONN
EDP_TXP1_CONN
EDP_TXN2_CONN
EDP_TXP2_CONN
EDP_TXN3_CONN
EDP_TXP3_CONN
EDP_AUXN_CONN
EDP_AUXP_CONN
GND


eDP Panel Conn.
+3VS_LCD
+3VS_Tunnel
@Panel
R4801
0Ohm
CAM_5V
C4836
0.1UF/16V
C4837
0.1UF/16V
C4838
0.1UF/16V
LX6303
EDP_TXN0_CONN
EDP_TXP0_CONN
EDP_TXN1_CONN
EDP_TXP1_CONN
EDP_TXN2_CONN
EDP_TXP2_CONN
EDP_TXN3_CONN
EDP_TXP3_CONN
EDP_AUXN_CONN
EDP_AUXP_CONN
AC_BAT_SYS_LCD
C4839
0.1UF/25V
PANEL_LCDCM_C
R4808
0Ohm
CNTOR_CON_40P
12017-00180900
S:12017-00180900
GND

Main Board

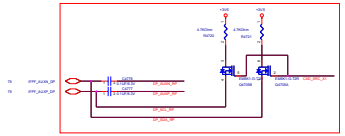
DP Repeater_PS8330B

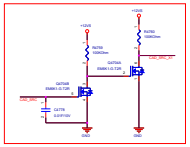


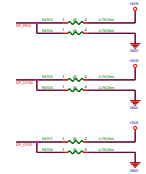


R2.0_30 reference Parade Design Circuit PS8330B

Fix MiniDP t o HDMI Dongle No Displa y Issue

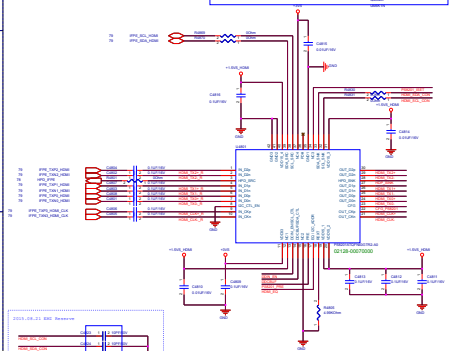




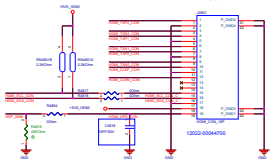


Main Board

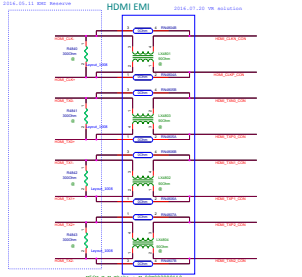
HDMI Active-Level Shift



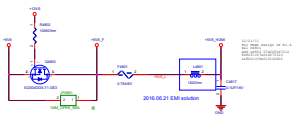
HDMI Conn.



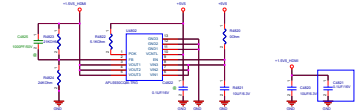
HDMI EMI

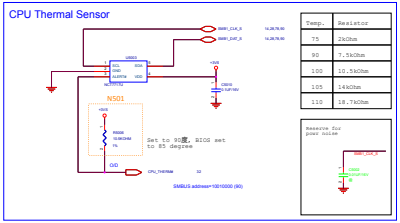


HDMI PWR_+5VS_HDMI

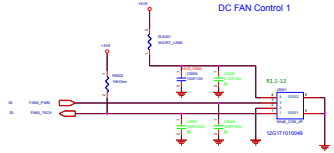


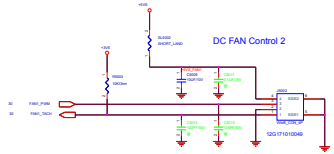
HDMI LDO 1.5VS

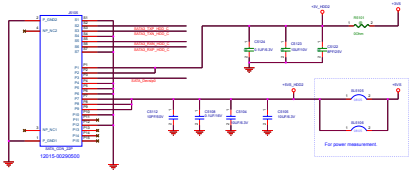




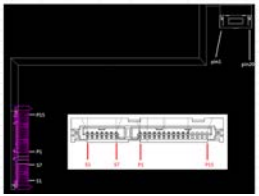
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm



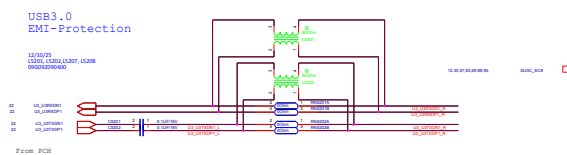


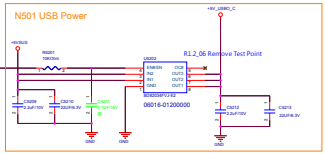


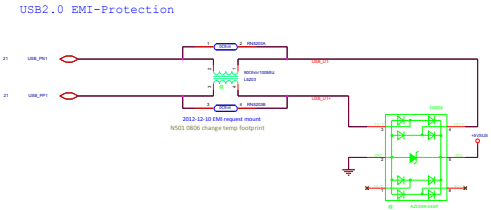
SATA Connector		
Pin	net	Note
P15	NC	
P14	NC	
P13	NC	
P12	Ground	
P11	NC	
P10	Ground	
P9	+5V	power
P8	+5V	
P7	+5V	
P6	Ground	
P5	Ground	
P4	Ground	
P3	Devslp	Impedance 50Ω
P2	+3V	power
P1	+3V	
S7	Ground	
S6	SATA_RX_P	Differential Pairs, impedance 85Ω
S5	SATA_RX_N	Differential Pairs, impedance 85Ω
S4	Ground	
S3	SATA_TX_N	Differential Pairs, impedance 85Ω
S2	SATA_TX_P	Differential Pairs, impedance 85Ω
S1	Ground	

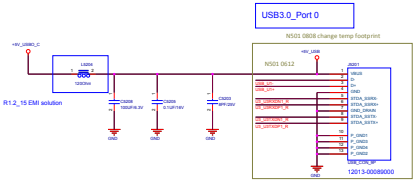


20 pin HDD Board connector		
Pin	net	Note
pin1	Ground	
pin2	NC	
pin3	+5V	power
pin4	+5V	
pin5	+5V	
pin6	+5V	
pin7	NC	
pin8	Ground	
pin9	Devslp	Impedance 50Ω
pin10	NC	
pin11	+3V	power
pin12	+3V	
pin13	NC	
pin14	Ground	
pin15	SATA_RX_P	Differential Pairs, impedance 85Ω
pin16	SATA_RX_N	Differential Pairs, impedance 85Ω
pin17	Ground	
pin18	SATA_TX_N	Differential Pairs, impedance 85Ω
pin19	SATA_TX_P	Differential Pairs, impedance 85Ω
pin20	Ground	


USB3.0
EMI-Protection
12/10/25
LS201, LS202,LS207, LS208
09x2702004430
From PCH

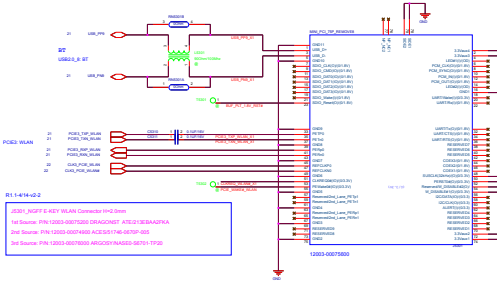

N501 USB Power
R1.2_06 Remove Test Point
06016-01200000


USB2.0 EMI-Protection
2012-12-10 EMI request mount
N501 0806 change temp footprint


USB3.0_Port 0
N501 0808 change temp footprint
N501 0612
R1.2_15 EMI solution
12013-00089000

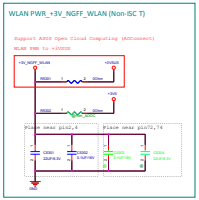
R1.1-02

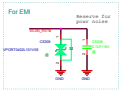
NGFF M.2 TYPE_E-KEY WIFI

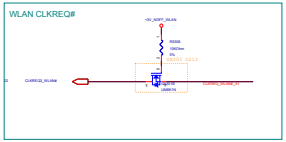


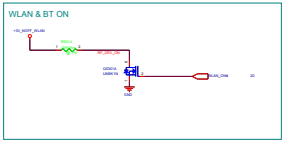
R1.1-4/14-v2-2

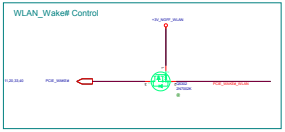
JS301_NGFF E-KEY WLAN Connector H=2.0mm
1st Source: P/N:12003-00075200 DRAGONIST ATE213EBAAZFKA
2nd Source: P/N:12003-00074900 ACES/51746-0670P-005
3rd Source: P/N:12003-00076000 ARCGSYINAS60-58701-TP20

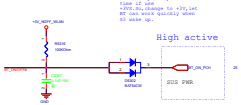




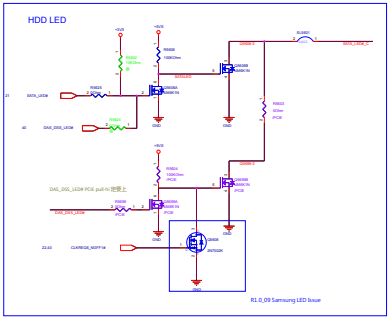


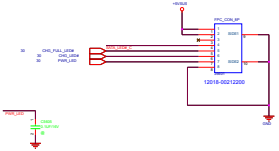


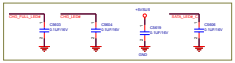


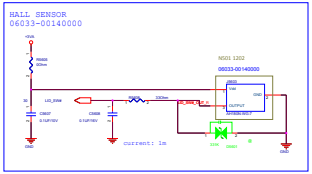


2014/05/29 Add HDD & SSD LED control circuit.

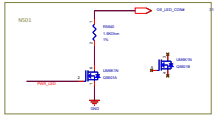


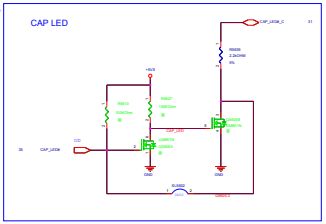


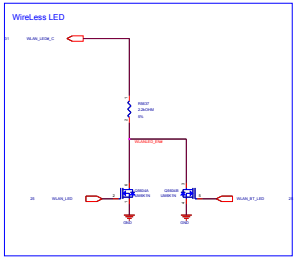




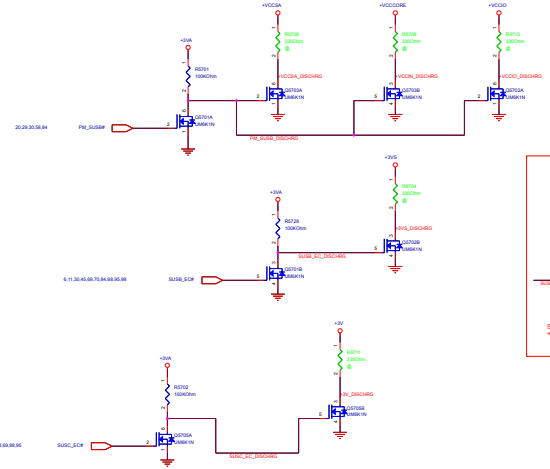
OS LED

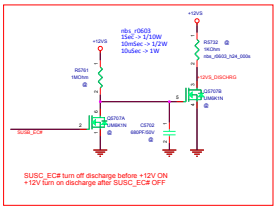


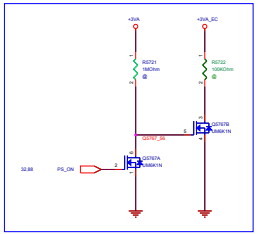


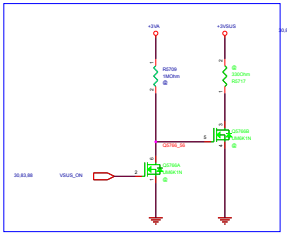


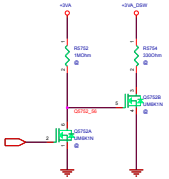
R0.1-02 R0.1-27 R1.0-17

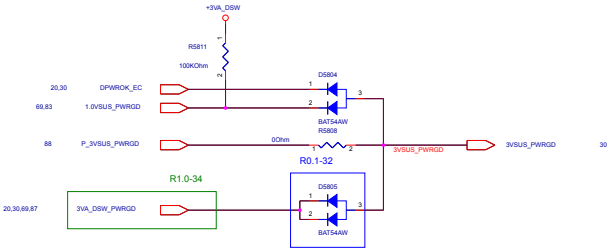


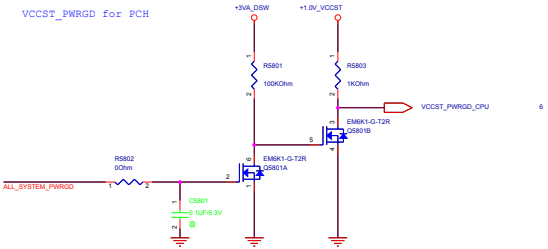


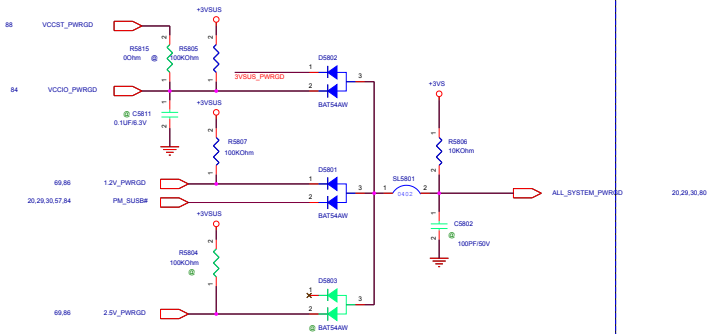


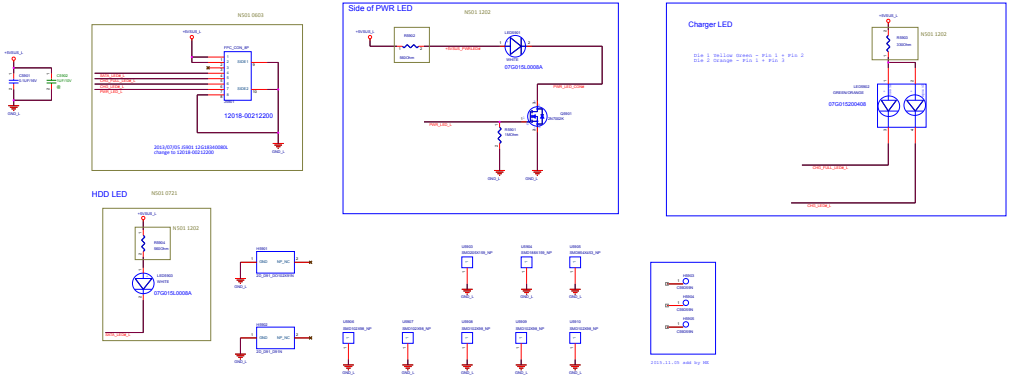




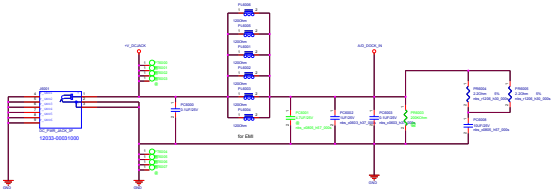

+3VA_DSW
RS811
100KOhm
20,30
DPWROK_EC
69,83
1.0VSUS_PWRGD
DS804
BAT54AW
88
P_3VSUS_PWRGD
0Ohm
RS808
3VSUS_PWRGD
3VSUS_PWRGD
30
R0.1-32
R1.0-34
20,30,69,87
3VA_DSW_PWRGD
DS805
BAT54AW


VCCST_PWRGD for PCH
+3VA_DSW
+1.0V_VCCST
RS801
100KOhm
RS803
1KOhm
VCCST_PWRGD_CPU
6
EM6K1-G-T2R
QS801B
EM6K1-G-T2R
QS801A
R5802
0Ohm
ALL_SYSTEM_PWRGD
C5801
0.1UF/6.3V

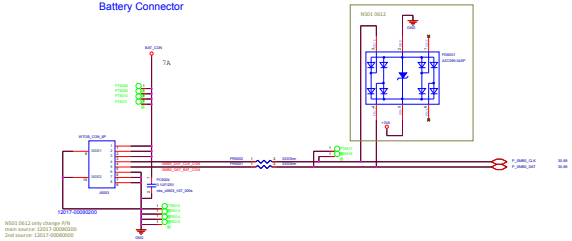

88
VCCST_PWRGD
+3VSUS
RS815
0Ohm
RS805
100KOhm
DS802
BAT54AW
3VSUS_PWRGD
84
VCCIO_PWRGD
C5811
0.1UF/6.3V
RS807
100KOhm
69,86
1.2V_PWRGD
20,29,30,57,84
PM_SUSB#
DS801
BAT54AW
SL5801
+3VS
RS806
10KOhm
ALL_SYSTEM_PWRGD
20,29,30,80
C5802
100PF/50V
RS804
100KOhm
69,86
2.5V_PWRGD
DS803
BAT54AW


Side of PWR LED
Charger LED
HDD LED
12018-00212200
07GD15L0008A
07GD15200408
H5901
H5902
U5905
U5906
U5907
U5908
U5909
U5910
U5903
U5904
H=1.3
H=0
H=0.2
H=0(to MB)

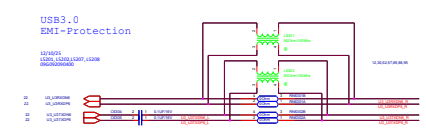
DC-IN Connector

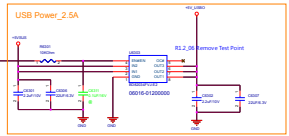


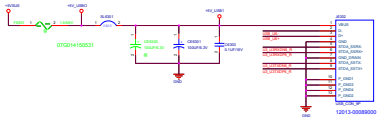
Battery Connector

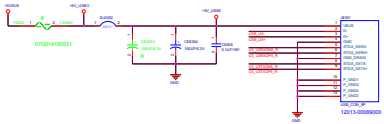


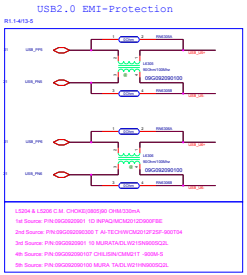
N501 0612 only change P/N
main source: 12017-00080200
2nd source: 12017-00080000

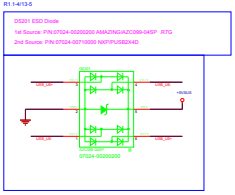

USB3.0
EMI-Protection
12/16/25
LS201, LS202 LS237, LS238
09G0920904000
From PCH

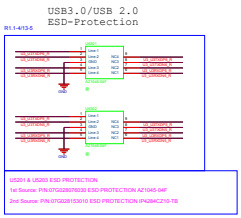

USB Power_2.5A
R1.2_06 Remove Test Point
06016-01200000

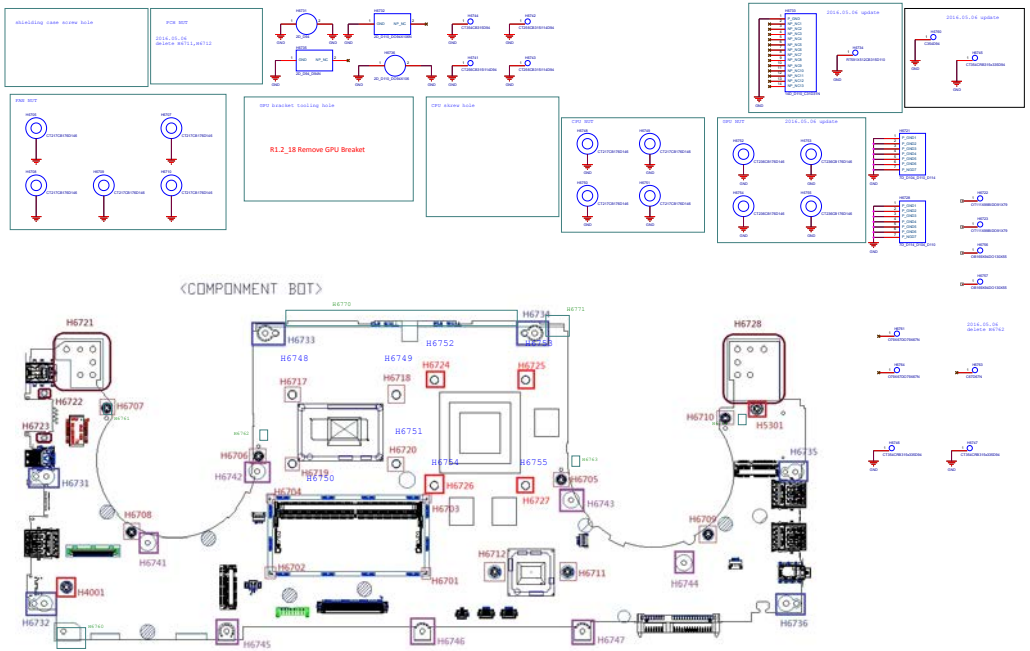

07G0141500531
12013-00089000


07G0141500531
12013-00089000

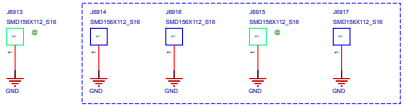

USB2.0 EMI-Protection
R1.1-4/13-5
09G0920900100
LS204 & LS206 C.M. CHOKE(1800)90 OHM/100mA
1st Source: P/N:09G0920900 1D-INPAC(HCM2012D900)FSE
2nd Source: P/N:09G0920900300 T At TECHWIC(M2012F2SF-900T04
3rd Source: P/N:09G0920901 1G MURATA(DLW21SN900SQ2)L
4th Source: P/N:09G0920901G7 CHILISIN(CMND1T -900M-S
5th Source: P/N:09G0920901G0 MURA TA(DLW21HN900SQ2)L

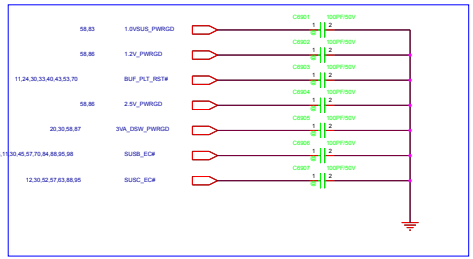

R1.1-4/13-5
DS201 ESD Diode
1st Source: P/N:07G24-002002200 AMAZING(AZC099-04SF .R7G
2nd Source: P/N:07G24-007100000 NXP/PUSE(D4)
07G24-002002200

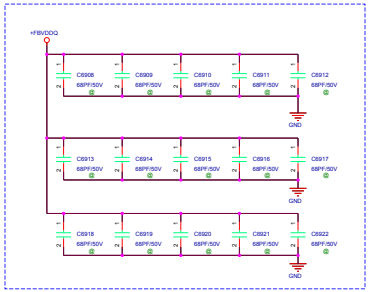

USB3.0/USB 2.0
ESD-Protection
R1.1-4/13-5
US201 & US203 ESD PROTECTION
1st Source: P/N:07G0280760330 ESD PROTECTION AZ1045-04F
2nd Source: P/N:07G0281530310 ESD PROTECTION IP4284CZ10-TB

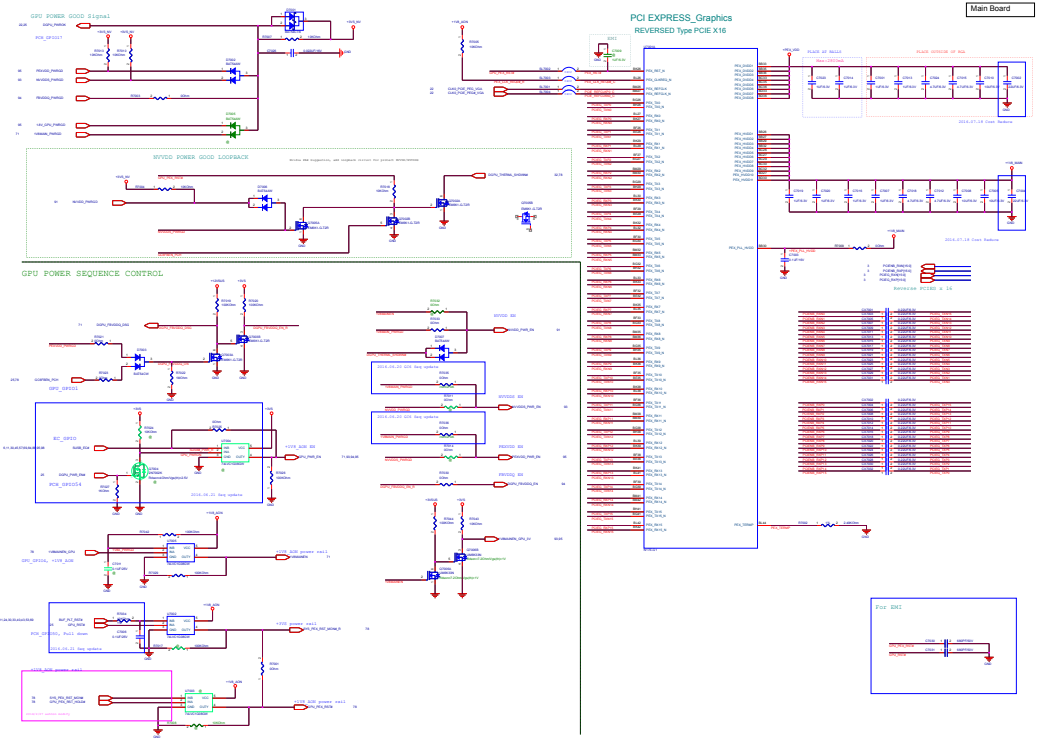

Shielding case screw hole
PCB HOT
2014.05.04
delete H6711,H6712
FAN HOT
CPU bracket tooling hole
R1.2_18 Remove GPU Breaket
CPU screw hole
CPU HOT
2014.05.04 update
<COMPONMENT BOT>
H6721
H6722
H6723
H6731
H6732
H6707
H6708
H6741
H4001
H6740
H6745
H6746
H6747
H6736
H6744
H6709
H6710
H5301
H6728
H6735
H6733
H6734
H6752
H6748
H6749
H6724
H6725
H6717
H6718
H6751
H6720
H6706
H6742
H6719
H6750
H6704
H6754
H6755
H6726
H6727
H6705
H6743
H6703
H6702
H6701
H6712
H6711

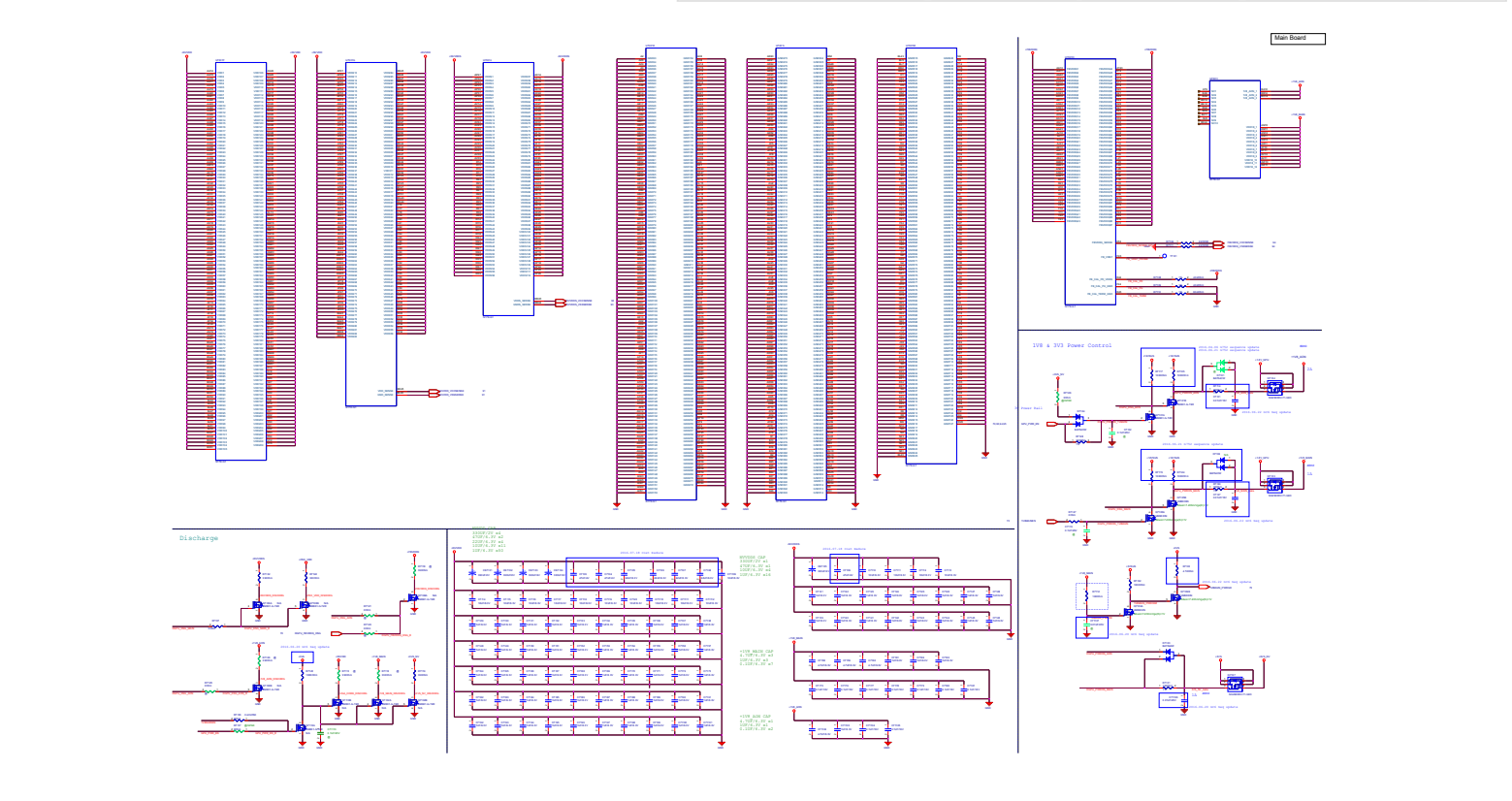
R1.2_17 EMI Reserve 100pf to Gnd





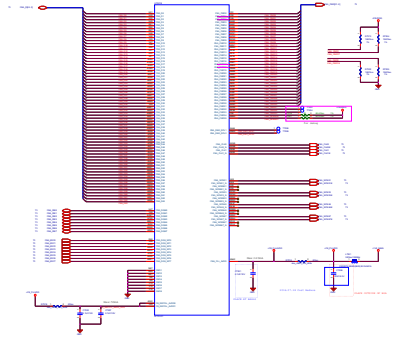



Main Board
PCI EXPRESS_Graphics
REVERSED Type PCIE X16
GPU POWER GOOD Signal
PCH_GPIO17
NVVDD POWER GOOD LOOPBACK
GPU POWER SEQUENCE CONTROL
GPU_GPIO1
EC_GPIO
PCH_GPIO54
GPU_GPIO2, +1V8_AON
PCH_GPIO50, Pull down
+3VS_AON power sail
+1V8_AON power sail
+1V05_AON power sail
+VCC_AON power sail
MVDD_EN
NVVDD_EN
FBVDDQ_EN
PEXVDD_EN
For EMI
Reserved Pin160 & 16

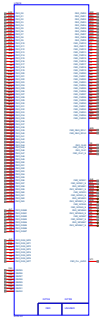

Main Board
Discharge
1V8 & 3V3 Power Control

Main Board

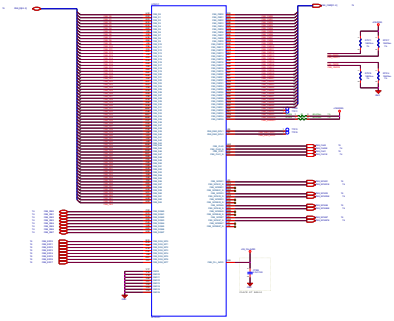
MEMORY: GPU FB Partition A



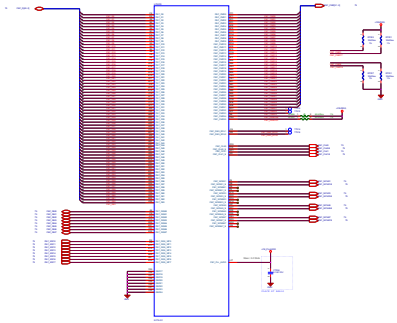
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B

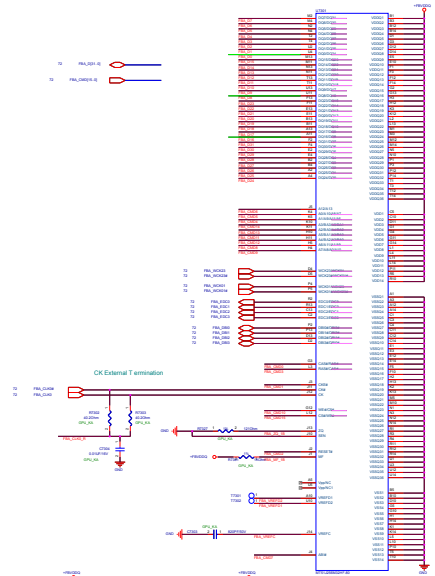


MEMORY: GPU FB Partition C



FBA Partition Memory (1 of 2)

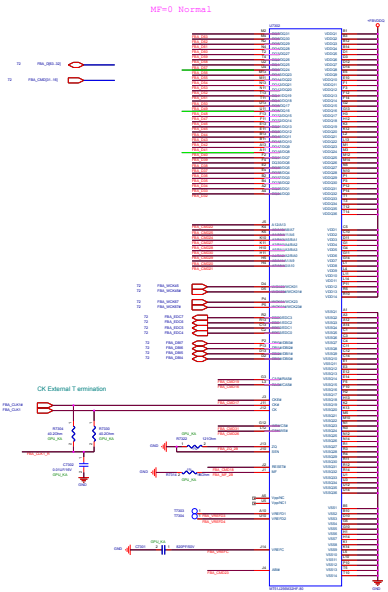
MF=1 Mirror



FBA Partition Memory (2 of 2)

Main Board

MF=0 Normal



R1.3-62 R1.2-25

USE GDDR5 V/RAM 128Mb x 32 (512MB)

1st: P/N:03008-00020100 HYNIX/H5GC4H24MFR-T2C (M-die), Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G4132SFC-HC03 ,Strap: 0x3

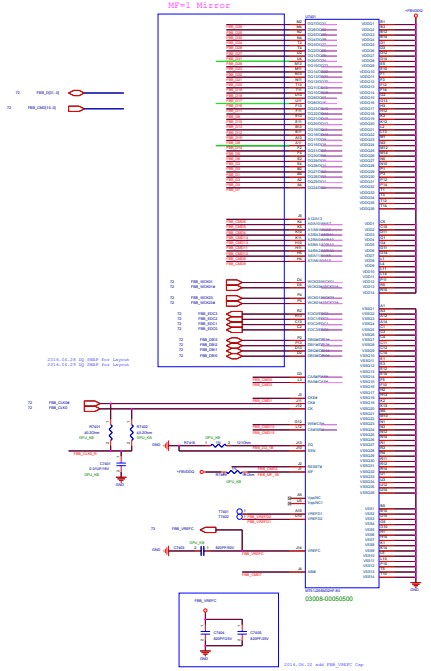
3rd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

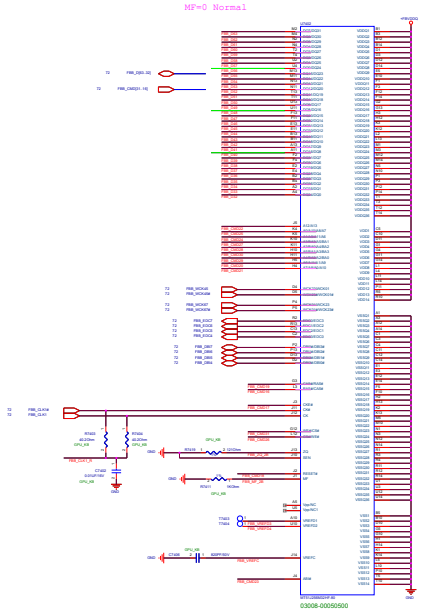
MA[10:0]	MF	BANK 1	BANK 0
x16	0	0	VDD
x32	0	VDD	VDD
x16, mirrored	VDD	VDD	0
x32, mirrored	VDD	VDD	VDD

Main Board

FBB Partition Memory (1 of 2)



FBB Partition Memory (2 of 2)



R1-3-02 R1-2-25

USE GDDR5 VRAM 128Mb x 32 (512MB):

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap :0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G4132SFC-HC03 ,Strap :0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

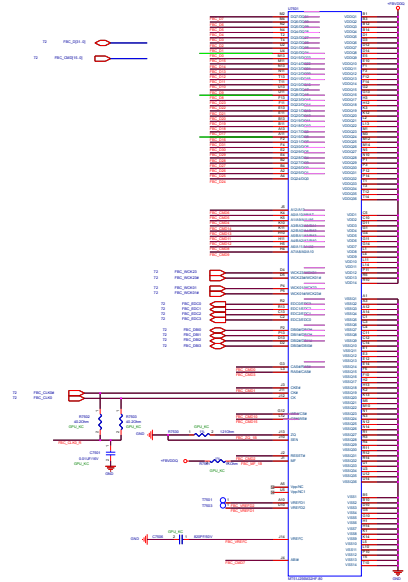
GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x32	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

Main Board

FBC Partition Memory (1 of 2)

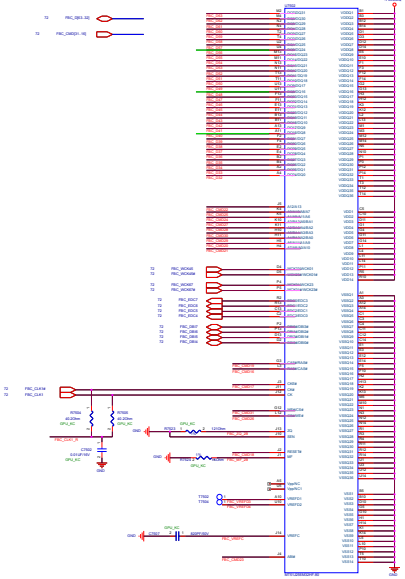
MF=1 Mirror



03008-00050500

FBC Partition Memory (2 of 2)

MF=0 Normal



03008-00050500

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX:H5GC4H24MFR-T2C (64-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G4132SFC-HC03 ,Strap: 0x3

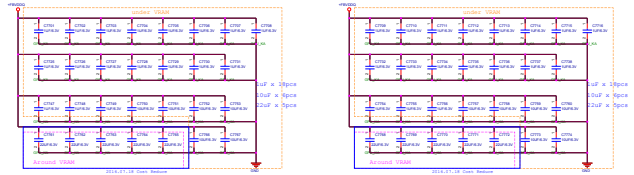
3nd: P/N:03008-00030400 Micron/EDW4032BABG-50-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

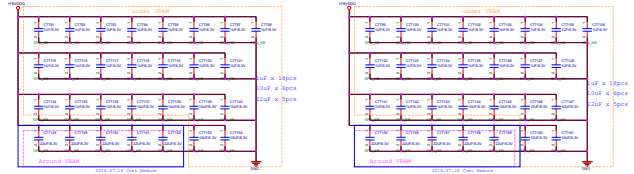
MA[4:0]	MF	EDC[1]	EDC[0]
x32	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	0	0
x32 mirrored	VDDQ	VDDQ	VDDQ

Main Board

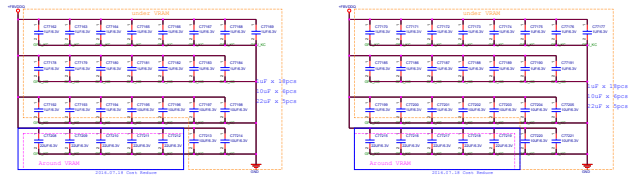
Chanel A



Chanel B

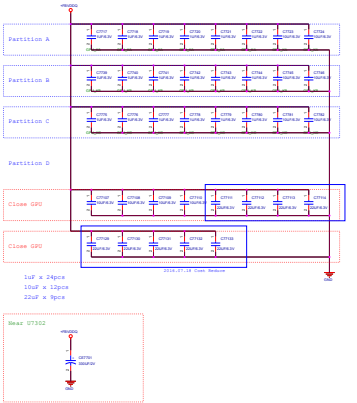


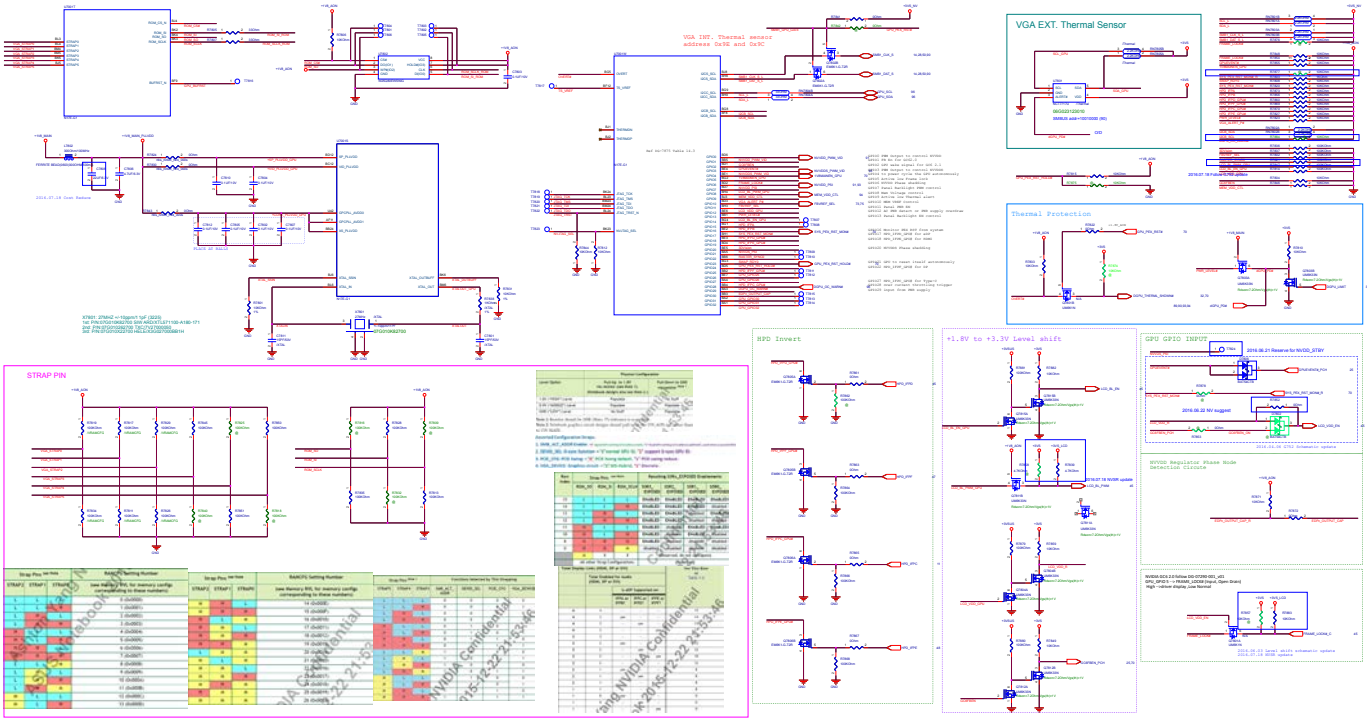
Chanel C

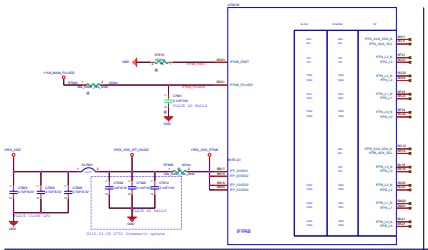


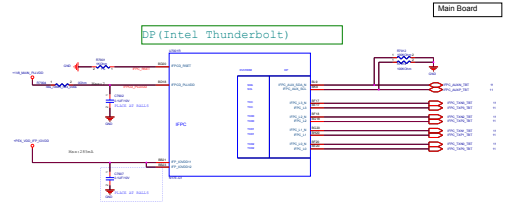
Chanel D

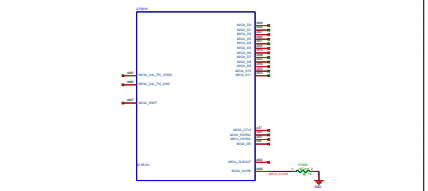
VRAM PWR_FBVDDQ

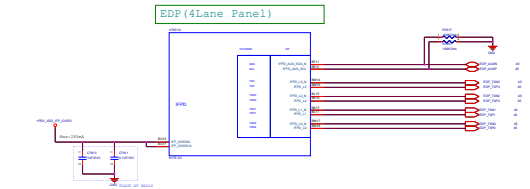


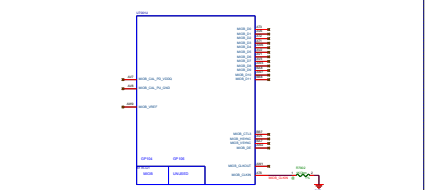

VGA IWT. Thermal sensor address 0x9E and 0x9C
VGA EXT. Thermal Sensor
Thermal Protection
STRAP PIN
HPD Invert
+1.8V to +3.3V Level shift
GPU GPIO INPUT
NVVDD Regulator Phase Node Detection Circuit
2016.06.21 Reserve for NVDD_STBY
2016.06.22 NV suggest
2016.07.18 NVDD update
2016.07.18 Level shift schematic update
2016.07.18 GPIO schematic update
NVIDIA Confidential

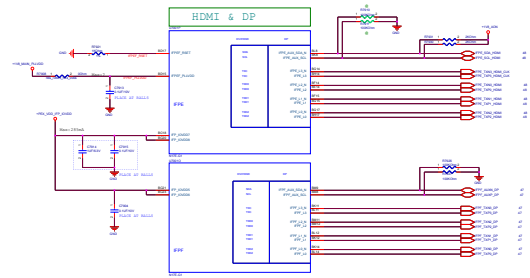








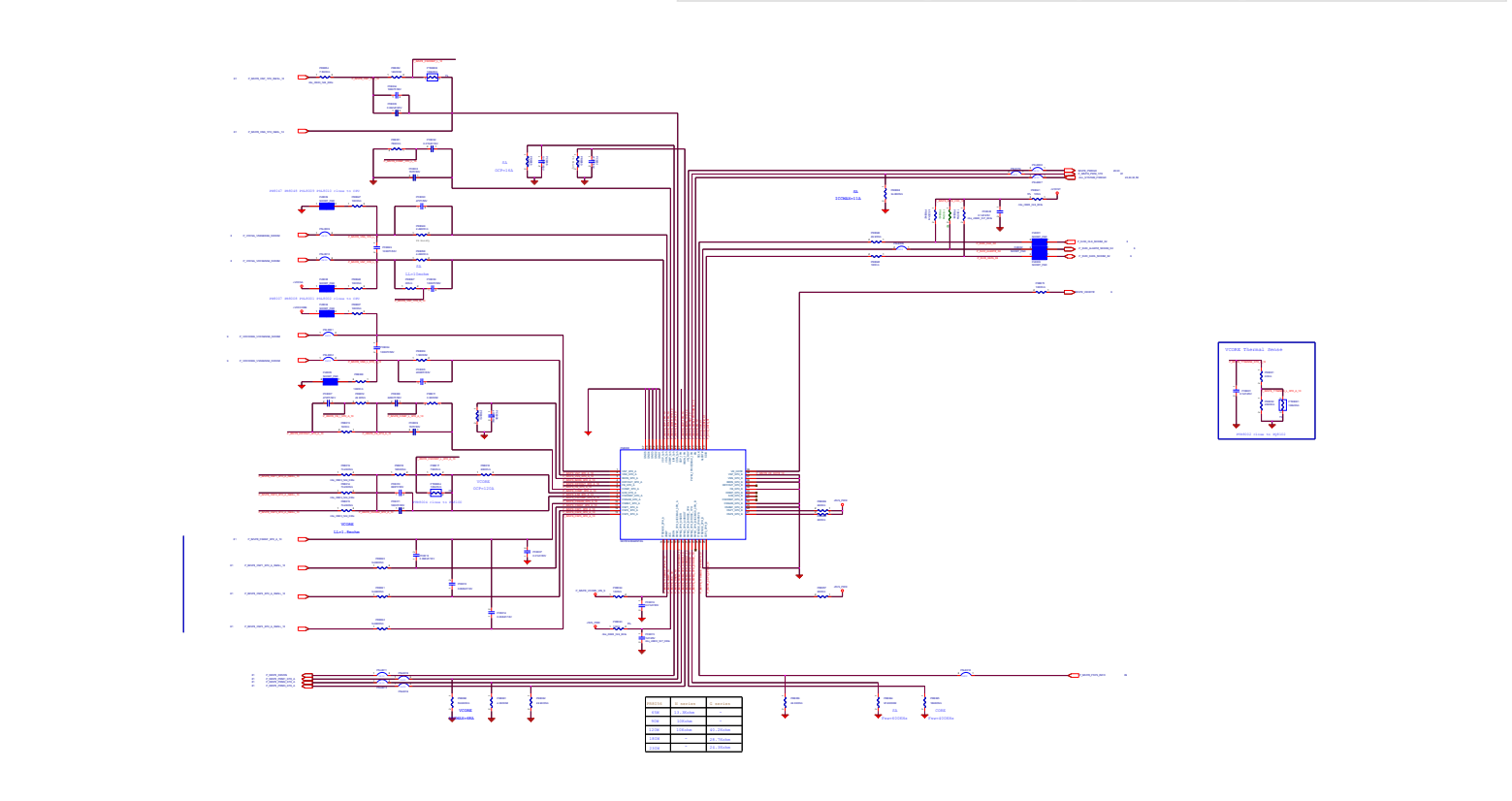




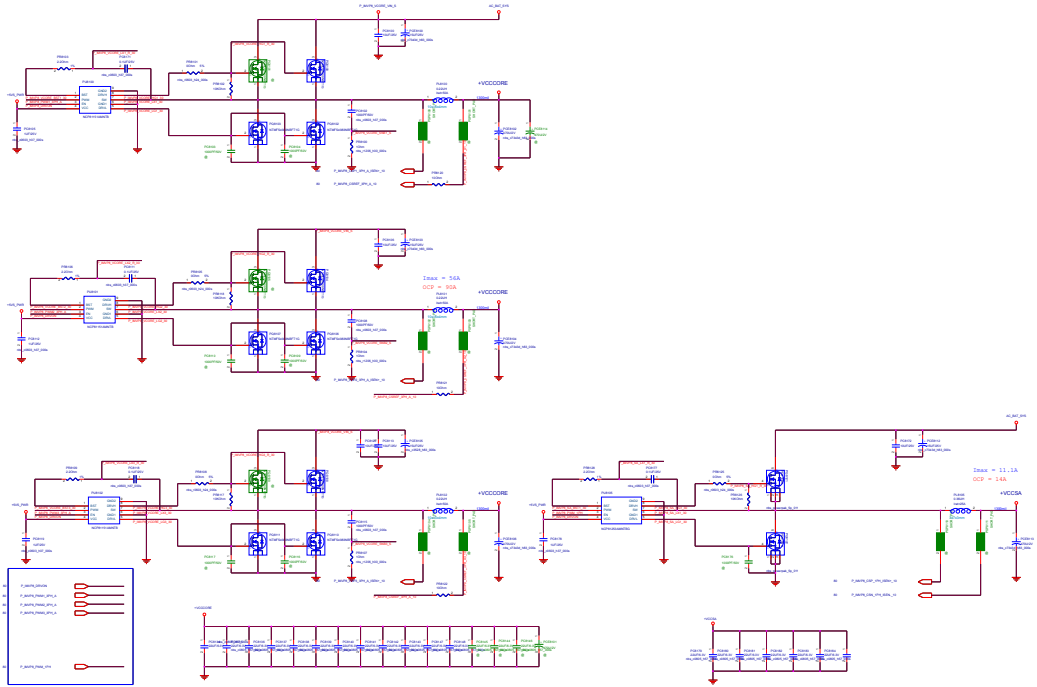
15.2.3 Unconnected Signals (NC)

The following guidelines apply to unused MIPI interfaces:

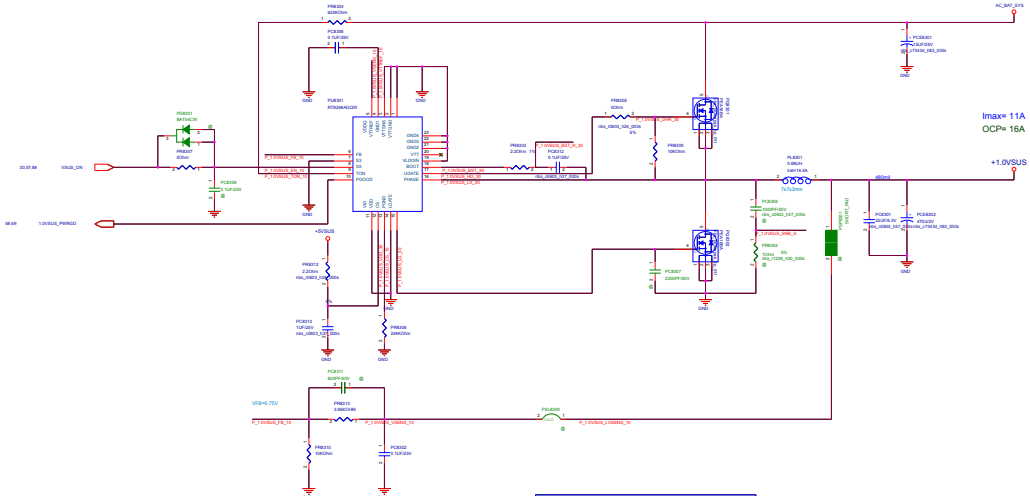
- Power up all VDD18 pins.
- Leave MIO data pins and clock pins floating.



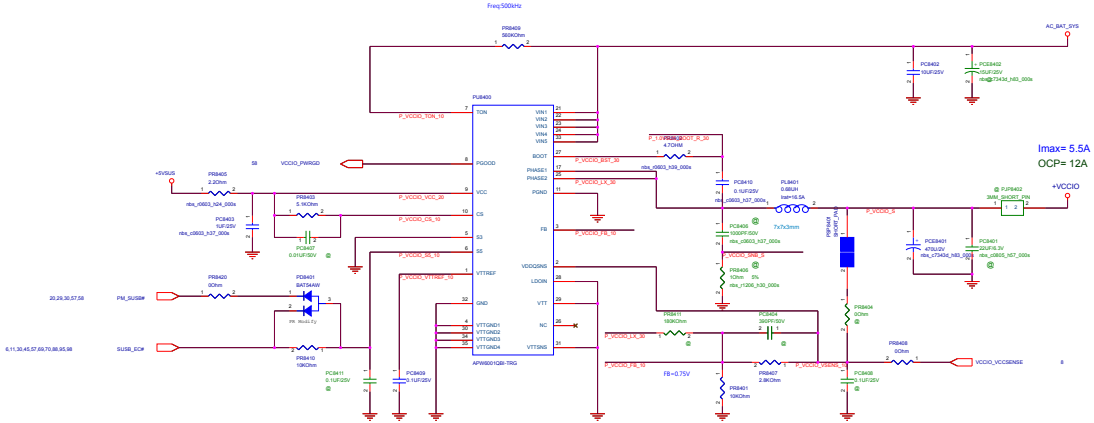
Skylake IMVP8 Power [For CPU]



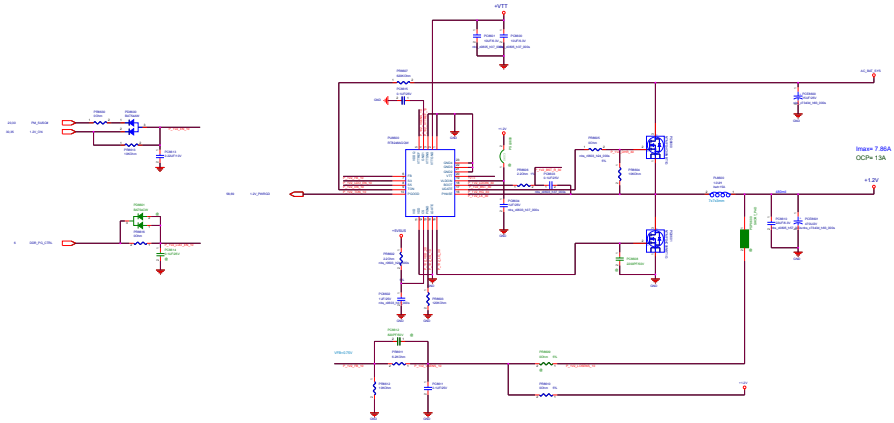
+1.0VSUS [For PCH]



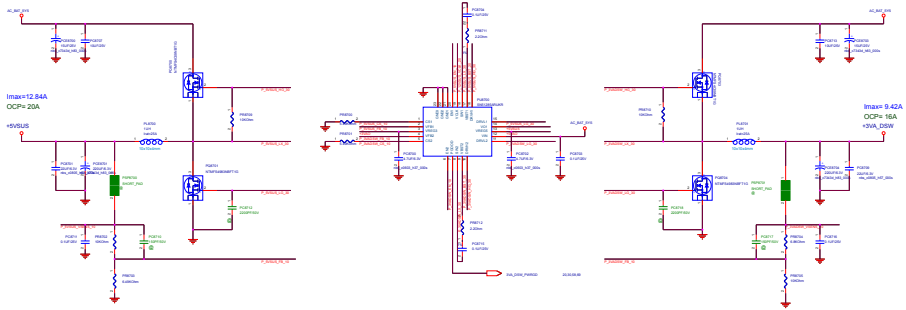
+VCCIO [For CPU]

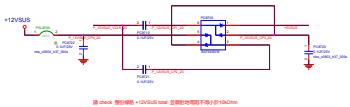


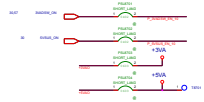
+1.2V / +VTT / +2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]







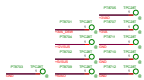
請 check 預防電阻 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (MVFR)

	M2	M1	M0	CHG	PH	PL	Bit with USB Charger=
PS_ON	0	0	0	1	0	0	0
SYSRUN_ON	0	0	1	1	0	0	1
SUS3_ON	0	1	0	1	0	0	0
SUS5_ON	0	1	1	1	0	0	1
1.5V_ON	1	0	0	1	0	0	0
SUS1_EC#	1	0	1	1	0	0	0
SUS6_EC#	1	1	0	1	0	0	0

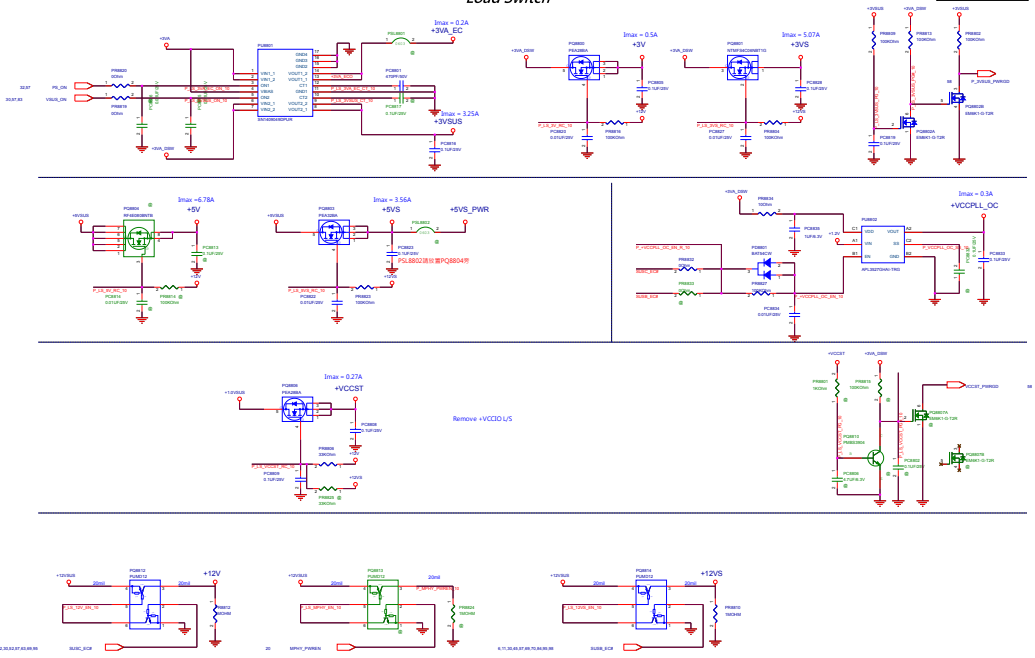
Battery Mode (MVFR)

	M2	M1	M0	CHG	PH	PL	Bit with USB Charger=
PS_ON	0	0	0	1	0	0	0
SYSRUN_ON	0	0	1	1	0	0	0
SUS3_ON	0	1	0	1	0	0	0
SUS5_ON	0	1	1	1	0	0	0
1.5V_ON	1	0	0	1	0	0	0
SUS1_EC#	1	0	1	1	0	0	0
SUS6_EC#	1	1	0	1	0	0	0

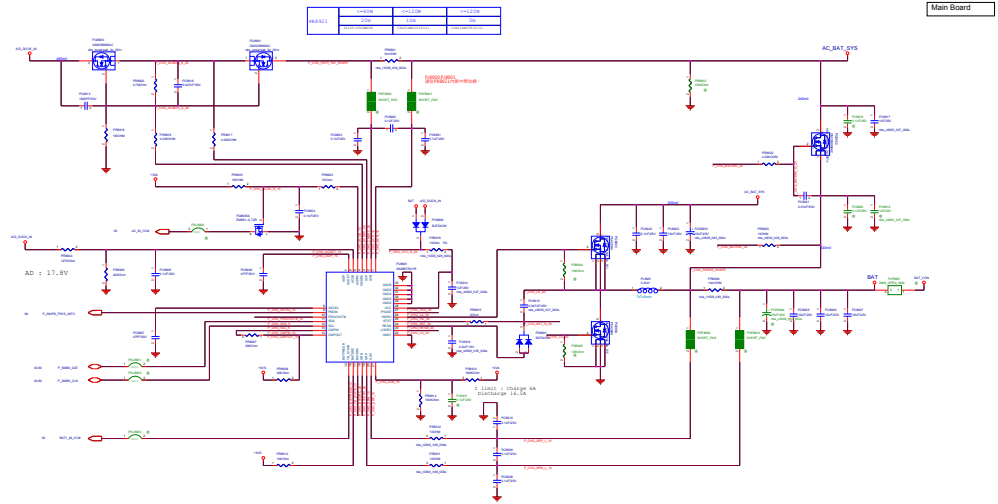


Main Board

Load Switch



Main Board



Adaptor select
total power = 90% ADP

Adaptor select			
	R Value	Wattage
968321	10m	65w
968936		
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	210W
150K	2.0V	75W	240W
270K	2.4V	90W	330W
560K	2.8V	120W	450W

HW_Throttle

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

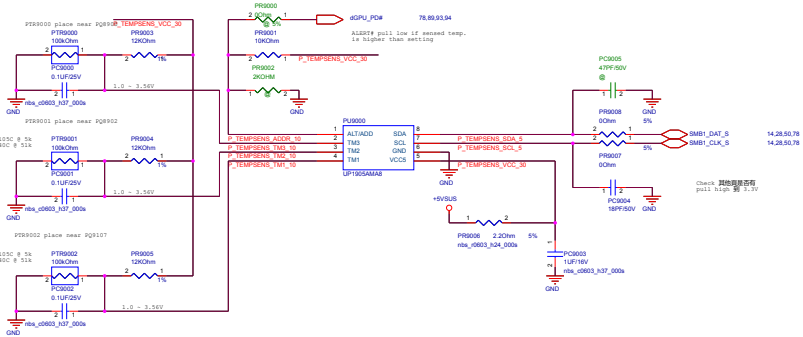
Main Board

Address Selection Table

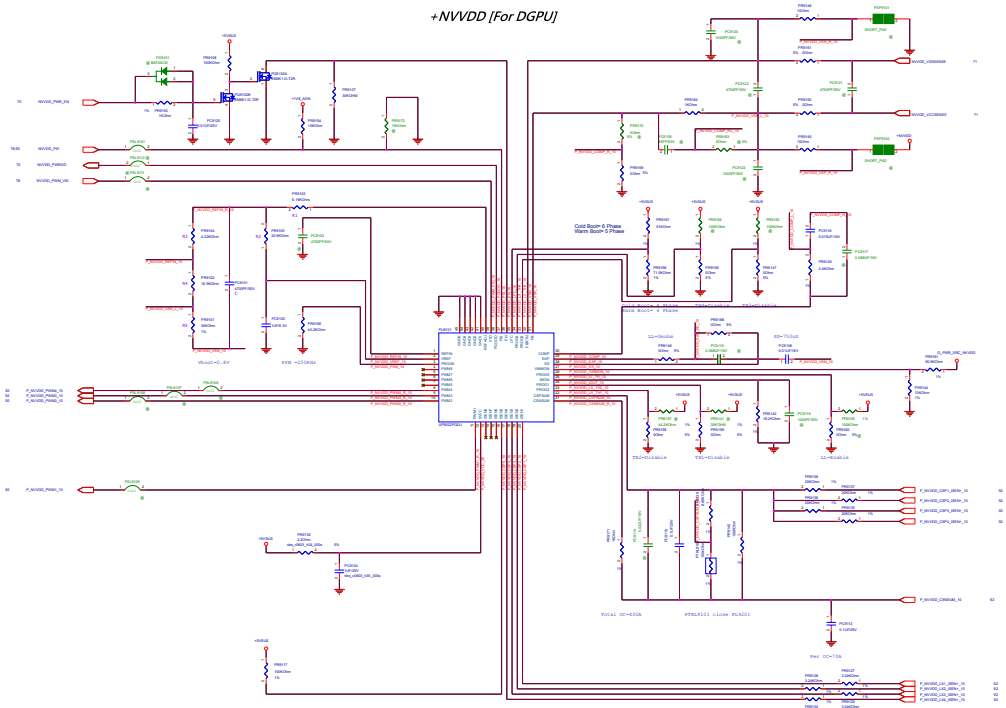
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	3.9k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

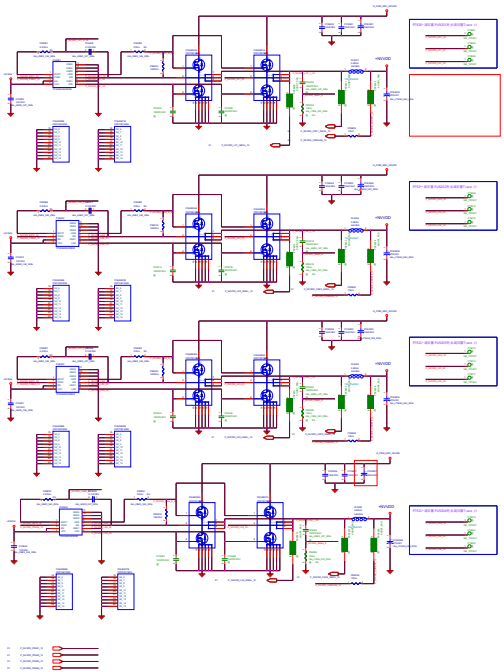
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



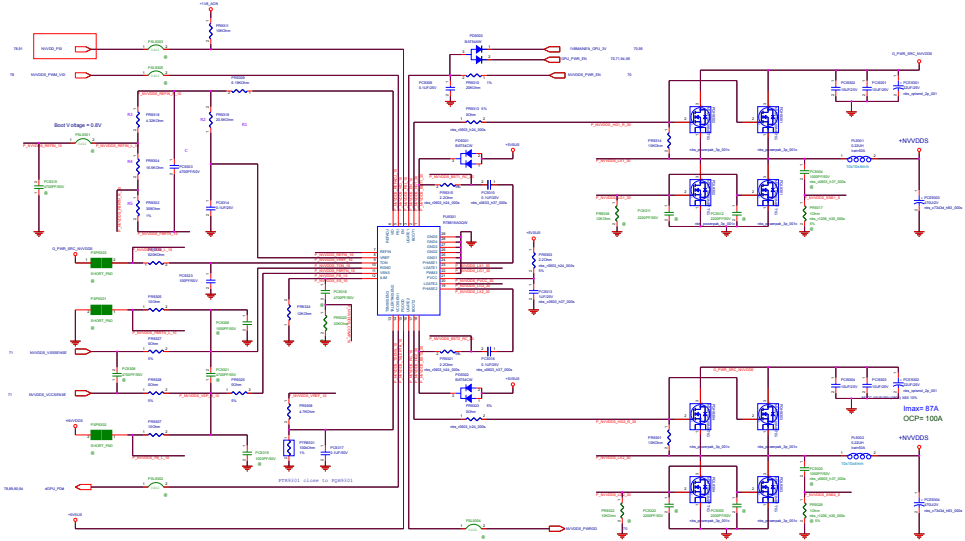
+NVVDD [For DGPU]



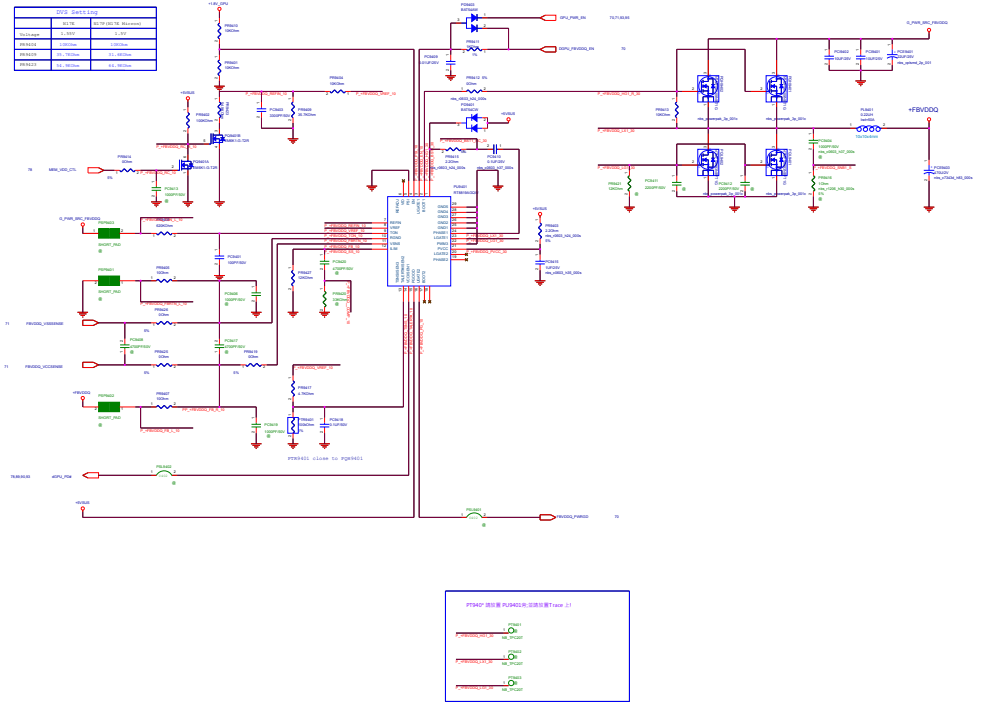
+NVVDD [For DGPU]

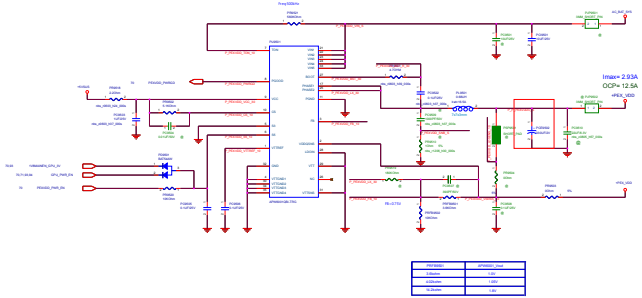


+NVVDDS [For DGPU]

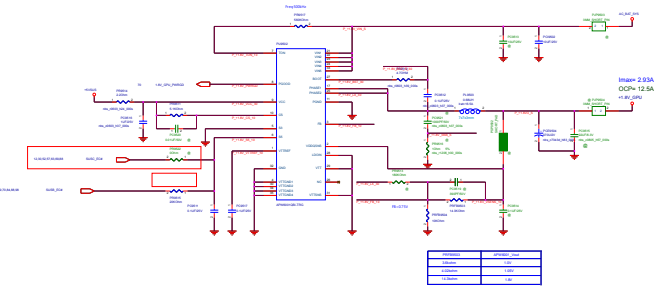


+FBVDDQ [For VRAM]

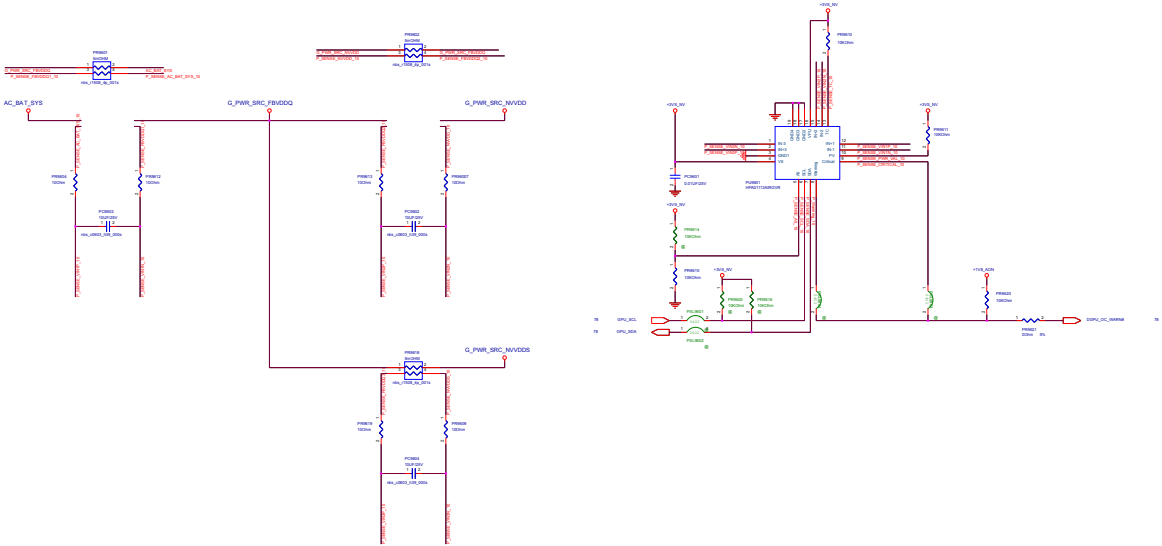




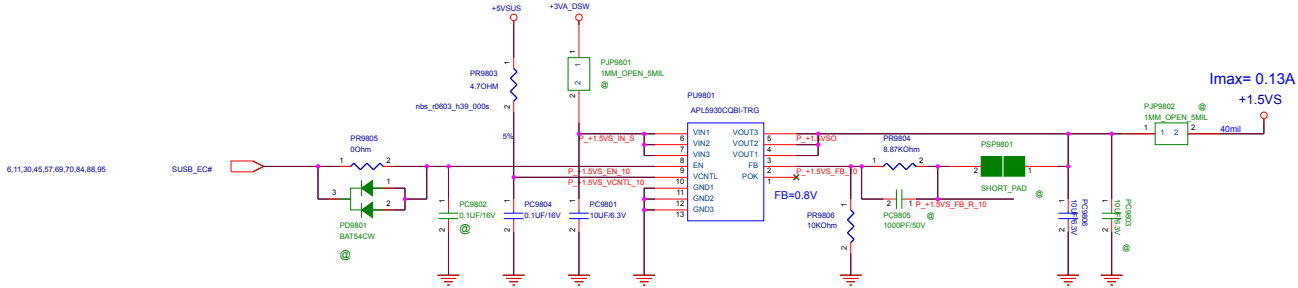
PMIC Enable	SPM8650_Vout
1.8Ohm/nm	1.8V
4.02kohm/nm	1.05V
10.2kohm/nm	1.8V

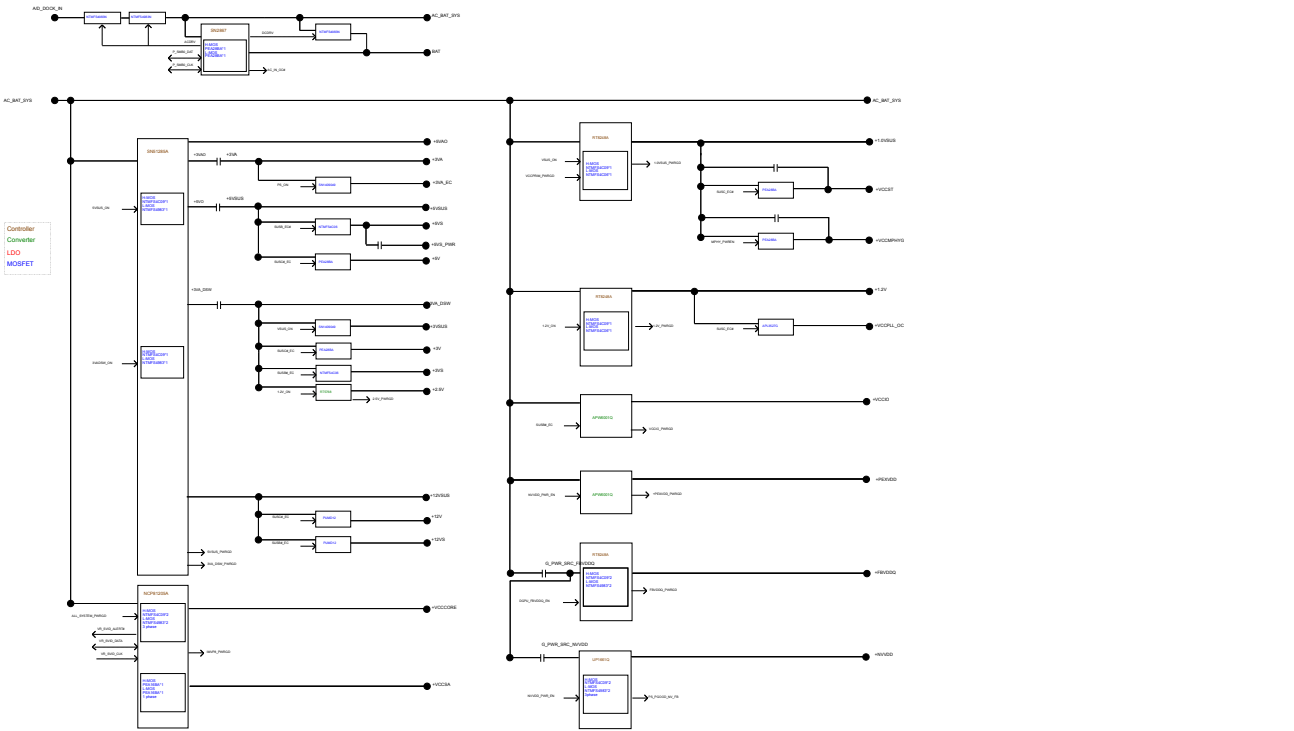


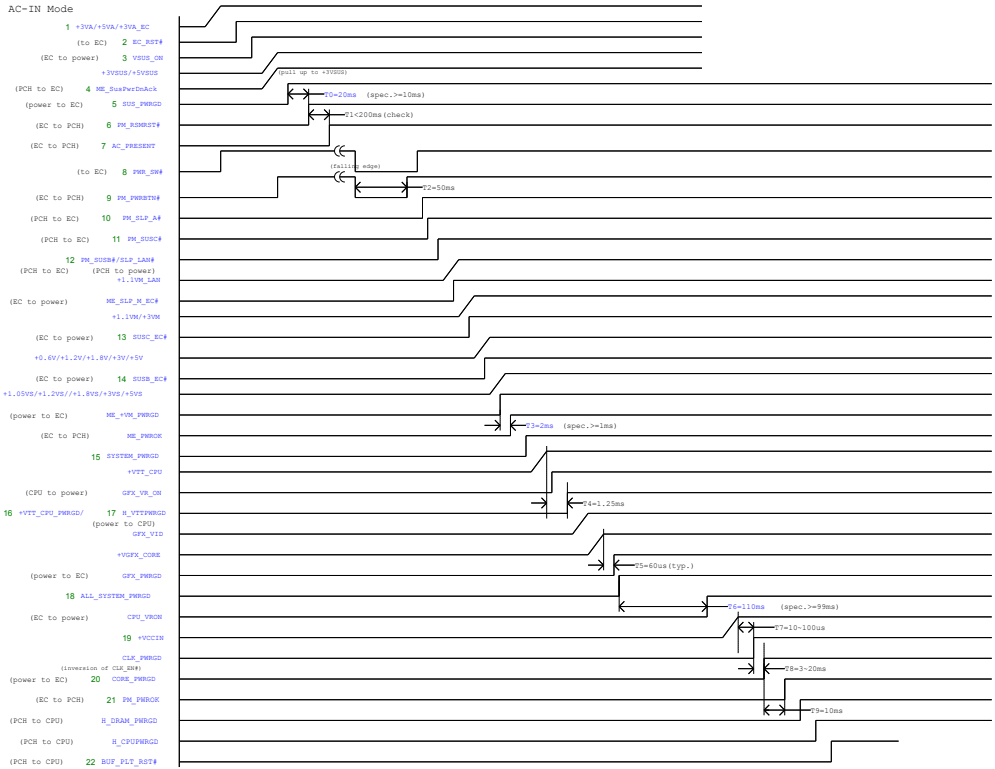
PMIC Enable	SPM8650_Vout
2.8kohm/nm	1.8V
4.02kohm/nm	1.05V
10.2kohm/nm	1.8V

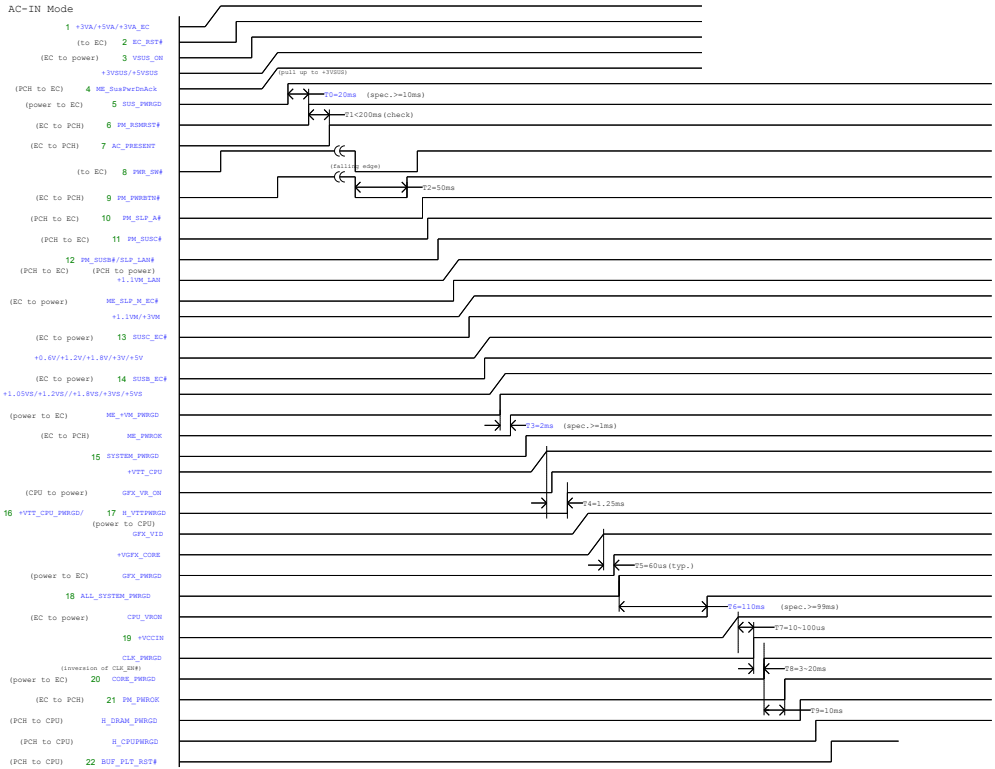

AC_BAT_SYS
G_PWR_SRC_FBVDDQ
G_PWR_SRC_NVVDD
G_PWR_SRC_NVVDDS
+3V3_NV
+1V8_AON
GPU_SCL
GPU_SDA
GPU_CC_WARN#

+1.5VS


+5VSUS
+3VA_DSW
PR9803
4.7OHM
nbs_r0603_h39_000s
5%
PJP9801
1MM_OPEN_5MIL
PU9801
APL5930CQBI-TRG
VIN1
VIN2
VIN3
EN
VCNTL
GND1
GND2
GND3
VOUT3
VOUT2
VOUT1
FB
POK
P_+1.5VS_IN_S
P_+1.5VS_EN_10
P_+1.5VS_VCNTL_10
P_+1.5VSO
P_+1.5VS_FB_10
FB=0.8V
PR9805
0Ohm
6,11,30,45,57,69,70,84,88,95
SUSB_EC#
PD9801
BAT54CW
PC9802
0.1UF/16V
PC9804
0.1UF/16V
PC9801
10UF/6.3V
PR9804
8.87KOhm
PR9806
10KOhm
PC9805
1000PF/50V
P_+1.5VS_FB_R_10
PSP9801
SHORT_PAD
PC9806
10UF/6.3V
PC9807
10UF/6.3V
PJP9802
1MM_OPEN_5MIL
40mil
Imax= 0.13A
+1.5VS


AC_DOCK_IN
AC_BAT_SYS
BAT
AC_BAT_SYS
Controller
Converter
LDO
MOSFET
+5VALW
+3VALW
+3VA_EC
+5VSUS
+3VSUS
+5VS_PWR
+5V
+3VA_DSW
+1V5SUS
+3V
+3VS
+2.5V
+12VSUS
+12V
+12VS
+VCCCORE
+VCC3A
+1.5VALW
+1.5V
+VCCPLL_IOC
+VCCIO
+PCIEVDD
+5VSODIO
+MVDD
AC_BAT_SYS


AC-IN Mode
1 +3VA/+5VA/+3VA_EC
(to EC) 2 EC_RST#
(EC to power) 3 VSUS_ON
+3VSUS/+5VSUS
(pull up to +3VSUS)
(PCH to EC) 4 ME_SusPwrDnAck
(power to EC) 5 SUS_PWRGD
T0=20ms (spec.>=10ms)
T1<200ms(check)
(EC to PCH) 6 PM_RSMRST#
(EC to PCH) 7 AC_PRESENT
(falling edge)
(to EC) 8 PWR_SW#
T2=50ms
(EC to PCH) 9 PM_PWRBTN#
(PCH to EC) 10 PM_SLP_A#
(PCH to EC) 11 PM_SUSC#
12 PM_SUSB#/SLP_LAN#
(PCH to EC) (PCH to power)
+1.1VM_LAN
(EC to power) ME_SLP_M_EC#
+1.1VM/+3VM
(EC to power) 13 SUSC_EC#
+0.6V/+1.2V/+1.8V/+3V/+5V
(EC to power) 14 SUSB_EC#
+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS
(power to EC) ME_+VM_PWRGD
T3=2ms (spec.>=1ms)
(EC to PCH) ME_PWROK
15 SYSTEM_PWRGD
+VTT_CPU
(CPU to power) GFX_VR_ON
T4=1.25ms
16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD
(power to CPU)
GFX_VID
+VGFX_CORE
T5=60us(typ.)
(power to EC) GFX_PWRGD
18 ALL_SYSTEM_PWRGD
T6=110ms (spec.>=99ms)
(EC to power) CPU_VRON
T7=10~100us
19 +VCCIN
CLK_PWRGD
(inversion of CLK_EN#)
T8=3~20ms
(power to EC) 20 CORE_PWRGD
(EC to PCH) 21 PM_PWROK
T9=10ms
(PCH to CPU) H_DRAM_PWRGD
(PCH to CPU) H_CPUPWRGD
(PCH to CPU) 22 BUF_PLT_RST#


AC-IN Mode
1 +3VA/+5VA/+3VA_EC
(to EC) 2 EC_RST#
(EC to power) 3 VSUS_ON
+3VSUS/+5VSUS
(pull up to +3VSUS)
(PCH to EC) 4 ME_SusPwrDnAck
(power to EC) 5 SUS_PWRGD
T0=20ms (spec.>=10ms)
T1<200ms(check)
(EC to PCH) 6 PM_RSMRST#
(EC to PCH) 7 AC_PRESENT
(falling edge)
(to EC) 8 PWR_SW#
T2=50ms
(EC to PCH) 9 PM_PWRBTN#
(PCH to EC) 10 PM_SLP_A#
(PCH to EC) 11 PM_SUSC#
12 PM_SUSB#/SLP_LAN#
(PCH to EC) (PCH to power)
+1.1VM_LAN
(EC to power) ME_SLP_M_EC#
+1.1VM/+3VM
(EC to power) 13 SUSC_EC#
+0.6V/+1.2V/+1.8V/+3V/+5V
(EC to power) 14 SUSB_EC#
+1.05VS/+1.2VS//+1.8VS/+3VS/+5VS
(power to EC) ME_+VM_PWRGD
T3=2ms (spec.>=1ms)
(EC to PCH) ME_PWROK
15 SYSTEM_PWRGD
+VTT_CPU
(CPU to power) GFX_VR_ON
T4=1.25ms
16 +VTT_CPU_PWRGD/ 17 H_VTTPWRGD
(power to CPU)
GFX_VID
+VGFX_CORE
T5=60us(typ.)
(power to EC) GFX_PWRGD
18 ALL_SYSTEM_PWRGD
T6=110ms (spec.>=99ms)
(EC to power) CPU_VRON
T7=10~100us
19 +VCCIN
CLK_PWRGD
(inversion of CLK_EN#)
T8=3~20ms
(power to EC) 20 CORE_PWRGD
(EC to PCH) 21 PM_PWROK
T9=10ms
(PCH to CPU) H_DRAM_PWRGD
(PCH to CPU) H_CPUPWRGD
(PCH to CPU) 22 BUF_PLT_RST#