Commercial AIO Chassis System

Project name: Woody
SCH Ver: SA
PCB Number: 15033-SA

PAGE	TITLE	Quantity
01	COVER PAGE	
02	BLOCK DIAGRAM	
03	CPU (PCIE/DMI)	
04	CPU_(THERMAL/CLOCK/PM/CFG)	
05	CPU_(DDR4 CHANNEL A)	
06	CPU_(DDR4 CHANNEL B)	
07	CPU (DDI/EDP)	
08	CPU (CPU Power)	
09	CPU (VSS)	
10	CPU (Power CAP)	
11	DDR4 DIMM_1	
12	DDR4 DIMM_2	
13	DDR4 DIMM_3_(R)	
14	DDR4 DIMM_4_(R)	
15	PCH (SPI/UART/I2C)	
16	PCH (DMI/PCI-E/USB)DDI GP	
17	PCH (PCI-E/SATA)	
18	PCH (CLOCK/CL)	
19	PCH (USB/ESPI)	
20	PCH(GPIO/CPU/SMBUS/IHDA/JTAG)	
21	PCH (POWER1)	
22	PCH (POWER2)_PCH Strap	
23	PCH Power CAP	
24	SIO ITE8732F_CX	
25	Flash&RTC	
26	Thermal&FAN	
27	Audio Codec_ALC269	
28	Audio_AMP	
29	Audio IO_Combo HP_MIC	
30	Audio IO_Side	
31	LAN_RTL8111EPV	
32	RJ45&Transformer	
33	Card reader_(R)	
34	USB Charger_TPS2544	
35	USB_Redrive_(R)	
36	USB20_REAR PORT	
37	USB20_FRONT HEADER	
38	USB30_REAR PORT	
39	USB30_(R)	
40	Power Plane EN Sequence	
41	Dual Power	
42	Switch power	
43	DCIN JACK(BATT Conn)	
44	OZ554A LED Converter	
45	RT8243_5V/3D3V	
46	VCORE & V_GT IC (NCP81203)	
47	VCORE OUTPUT (NCP81151)	
48	V_GT OUTPUT(NCP81151)	
49	DC to DC_12V (SY8246)	
50	MEM/MEMVTT (RT8207P)	
51	PCH_1P0V(RT8237C)	
52	VCC_SA(RT8237C)	
53	VCC_IO(RT8237C)	
54	LDO_1P5V_1P8V_2P5V	

PAGE	TITLE	Quantity
55	LVDS Connector	
56	HDMI IN	
57	HDMI OUT_(R)	
58	DVI/CRT	
59	Display port	
60	HDD/ODD	
61	Mini PCIE Card TV Tuner_(R)	
62	WLAN and BT--NGFF	
63	SSD-NGFF	
64	PWR BT/Side Key/LED	
65	Stand off&EMI Cap&DUMMY BOM	
66	IO Board	
67	COM	
68	Debug	
69	LPT_(R)	
70	G sensor	
71	Thunderbolt_(R)	
72	Thunderbolt_(R)	
73	Thunderbolt_(R)	
74	Thunderbolt_(R)	
75	Thunderbolt_(R)	
76	GPU_(R)	
77	GPU_(R)	
78	GPU_(R)	
79	GPU_(R)	
80	GPU_(R)	
81	GPU VRAM 1&2_(R)	
82	GPU VRAM 3&4_(R)	
83	GPU VRAM 5&6_(R)	
84	GPU VRAM 7&8_(R)	
85	GPU CORE_(R)	
86	GPU discrete power_(R)	
87	GPU Switch_(R)	
88	GPU Switch_(R)	
89	GPU others_(R)	
90	NFC_(R)	
91	TPM	
92	PS2_(R)	
93	Express Card:PCIE X16	
94	Smart Card_(R)	
95	Scalar-RTD2486VRD	
96	Scalar Power	
97	Inter LAN	
98	LAN Switch_(R)	
99	XDP&ITP	
100	Table of Content	
101	GPIO table	
102	POWER SEQUENCE	
103	Power Block Diagram	
104	SMBUS table	
105	CLOCK MAP	
106	RESET Flow CHART	
107	Change History	

PCB BOARD SIZE
6 Layers
200mmX240mm

BOM Configuration
Unmount:(R_)
Q170:(Q_)
H110:(H_)
VGA:(D_)
XDP:(X_)
3D WEBCAM:(W3_)
AMP:(A_)
SCALAR:(S_)
G-Sensor:(G_)
Non HDMI:(U_)
HDMI:(M)

<Core Design>

wistron

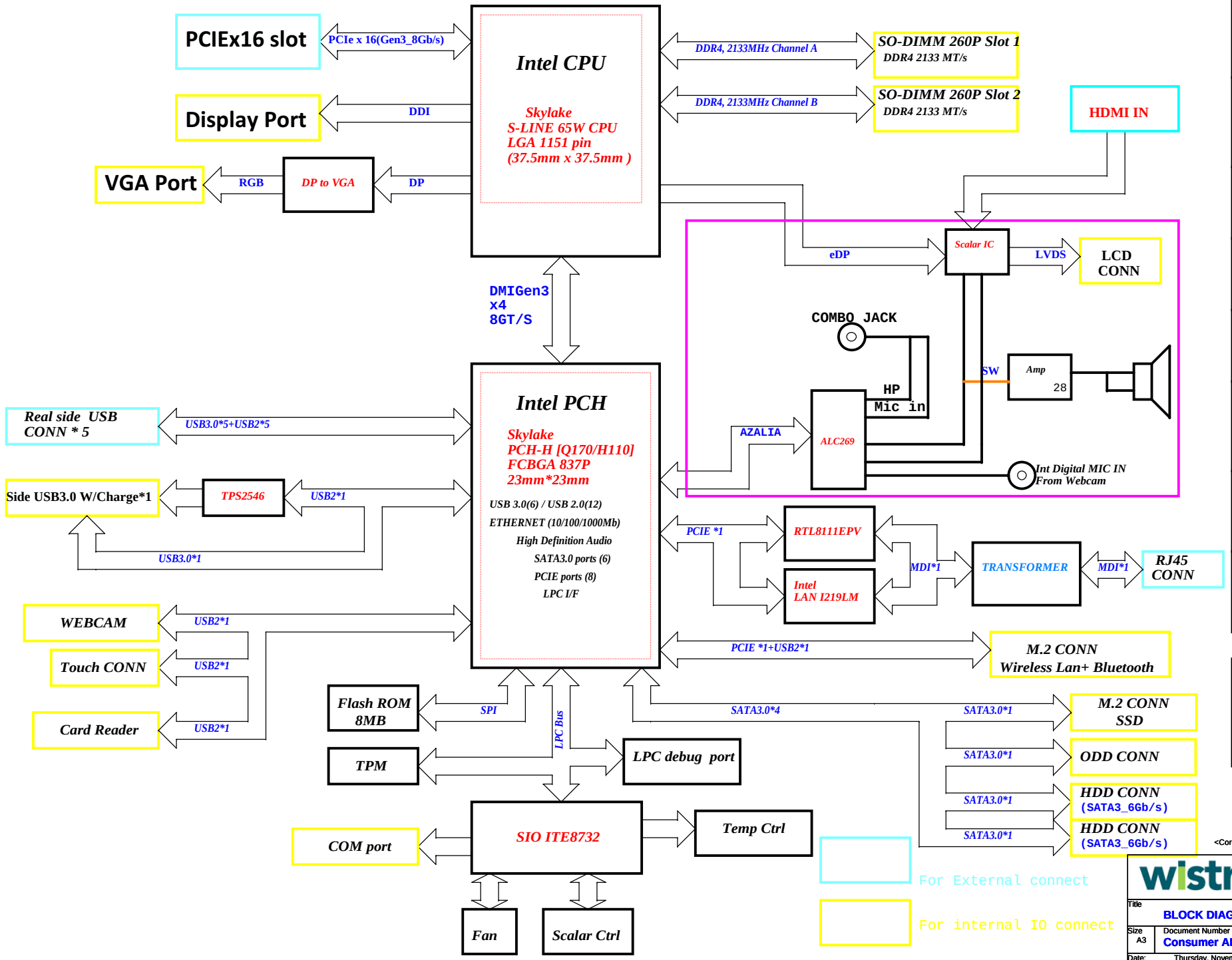
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: COVER PAGE

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 1 of 107

Woody Block Diagram



5V/3D3V DC/DC RT8243B	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_Charger 3D3V_A

CPU/GT DC/DC NCP81203	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE GFX_CORE

VCCSA DC/DC RT8237C	
INPUTS	OUTPUTS
DCBATOUT	VCC_SA

VCCIO DC/DC RT8237C	
INPUTS	OUTPUTS
DCBATOUT	VCC_IO

12V DC/DC RT8115C	
INPUTS	OUTPUTS
3D3V_S0	12V_S0

MEM/MEMVTT DC/DC RT8207P	
INPUTS	OUTPUTS
DCBATOUT	VDDQ 0D6V_VREF_S0

1D0V DC/DC RT8237C	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

VGA DC/DC NCP81172	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Bottom
L3:Signal	
L4:Signal	

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 2 of 107

2014/8/5
Change CPU P/N to 062.10015.0081

PEG

93 PEG_TX_CPU_P[0..15]
93 PEG_TX_CPU_N[0..15]
93 PEG_RX_CPU_P[0..15]
93 PEG_RX_CPU_N[0..15]

DMI

16 DMI_RX_CPU_P[0..3]
16 DMI_RX_CPU_N[0..3]
16 DMI_TX_CPU_P[0..3]
16 DMI_TX_CPU_N[0..3]

SKYLAKE-1

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU(PCIE/DMI)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 3 of 107

CPU XDP

4 XDP_PCUDEBUG3

20 H_TCK

65 H_TRST_N

SVID

46 VIDSCK_VR1

46 VIDSOUT_VR1

46 VIDALERT#_VR1

CLOCK

18 CPU_BCLK_PCH

18 CPU_BCLK_PCH#

18 CPU_PCIBCLK_PCH

18 CPU_PCIBCLK_PCH#

18 CPU_CLK24M_PCH

18 CPU_CLK24M_PCH#

CONTROL

65 CPU_VCCST_PWRGD_R

43,46 PROCHOT#_R

40,50 DDR_VTT_CNTL

40 CPU_VCCST_PWRGD

20,65 H_PWRGD

17,65 PLTRST_CPU_N

17 PM_SYNC_CPU

17 PM_DOWN_PCH

17,24 PECI_CPU

17 THERMTRIP#_CPU_R

16 H_SKTOCC_N

20 PCH_JTAG_TDO

20 PCH_JTAG_TDI

20 PCH_JTAG_TMS

21 H_TRST_N_R

VIDSCK
VIDSOUT
VIDALERT#
Need to add Pull UP on both CPU and VR side.

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{ser1} [Ω]	R_{mid2} [Ω]	R_{b1} [Ω]	R_{b2} [Ω]	VCC_{GT} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

2014/9/29
reserve R21 as Rosa D7

SKL_CNL_N — R402 2 (R) 1 — 10KR2J-3-GP — VCC_IO

This RES Value unconfirm.

1V_VCCST_VCCPLL_S3

VIDSCK_VR1 — R404 1 (R) 2 — 45D3R2F-L-GP
VIDALERT#_VR1 — R470 1 — 56R2F-1-GP
VIDSOUT_VR1 — R471 1 — 100R2J-2-GP
PROCHOT#_CPU — R421 1 — 2 75R2F-2-GP

Change R421 to 75ohm as CRB v1.0

3D3V_S5

H_SKTOCC_N — R477 1 — 10KR2J-3-GP

H_TCK TERMINATION
PLACE NEAR CPU WITHIN 1.1 INCH

H_TCK — R403 1 — 51R2F-2-GP

PLace Anywhere

H_TRST_N — R407 1 — 51R2F-2-GP

2014/8/5
Change CPU P/N to 062.10015.0081

CFG3 — R414 — 1KR2J-1-GP — XDP_PCUDEBUG3 — XDP_PCUDEBUG3 4

CPU1E — SKYLAKE — 5 OF 12 — LGA1151 — SKYLAKE-1

CPU_BCLK_PCH — W5 BCLKP
CPU_BCLK_PCH# — W4 BCLKN
CPU_PCIBCLK_PCH — W1 PCI_BCLKP
CPU_PCIBCLK_PCH# — W2 PCI_BCLKN
CPU_CLK24M_PCH — K9 CLK24P
CPU_CLK24M_PCH# — J9 CLK24N

VIDALERT#_VR1 — R469 1 — 220R2J-L2-GP — VIDALERT#_CPU — E39 VIDALERT#
VIDSCK_VR1 — E38 VIDSCK
VIDSOUT_VR1 — E40 VIDSOUT
PROCHOT#_R — R467 1 — 100R2J-2-GP — PROCHOT#_CPU — C39 PROCHOT#

Change R467 to 100ohm as CRB v1.0

DDR_VTT_CNTL — AC36 DDR_VTT_CNTL
TP_CPU_ZVM# — AC38 ZVM#
TP_CPU_AC37 — AC37 RSVD_AC37
TP37 — TP_CPU_AC37

CPU_VCCST_PWRGD — R433 — 0R0402-PAD-2-GP — CPU_VCCST_PWRGD_R — U2 VCCST_PWRGD

H_PWRGD — F8 PROCPWRGD
PLTRST_CPU_N — E7 RESET#
PM_SYNC_CPU — E8 PM_SYNC
PM_DOWN_PCH — R422 — 20R2F-GP — PM_DOWN_CPU — D8 PM_DOWN
PECI_CPU — G7 PECI
THERMTRIP#_CPU_R — R468 — 0R0402-PAD-2-GP — THERMTRIP#_CPU — D11 THERMTRIP#

H_SKTOCC_N — AB35 SKTOCC#
SKL_CNL_N — AB36 PROC_SELECT#
TP_CPU_AB37
TP_CPU_D14
CATERR#_CPU — D13 CATERR#

CFG0 H15 — R410 — 1KR2J-1-GP
CFG1 F15 — R418 — 1KR2J-1-GP
CFG2 F16 — R419 — 1KR2J-1-GP
CFG3 H16 — R420 — 1KR2J-1-GP
CFG4 F19 — R431 — 1KR2J-1-GP
CFG5 H18 — R429 — 1KR2J-1-GP
CFG6 G21 — R430 — 1KR2J-1-GP
CFG7 H20 — R411 — 1KR2J-1-GP
CFG8 G16 — R428 — 1KR2J-1-GP
CFG9 E16 — R432 — 1KR2J-1-GP
CFG10 F17 — R423 — 1KR2J-1-GP
CFG11 H17 — R425 — 1KR2J-1-GP
CFG12 G20 — R424 — 1KR2J-1-GP
CFG13 F20 — R426 — 1KR2J-1-GP
CFG14 F21 — R427 — 1KR2J-1-GP
CFG15 H19 — R454 — 1KR2J-1-GP

SKL_PCUSTB_0_DN — E14
SKL_PCUSTB_0_DP — F14
SKL_PCUSTB_1_DN — G18
SKL_PCUSTB_1_DP — F18
7/15 Alex Correct
For CPU XDP

BPM_CPU_N0 — D16 BPM#0
BPM_CPU_N1 — D17 BPM#1
TP_CPU_G14 — G14 BPM#2 — TP_CPU_G14
TP_CPU_H14 — H14 BPM#3 — TP_CPU_H14

PROC_TDO — H13 H_TDO
PROC_TDI — G12 H_TDI
PROC_TMS — F13 H_TMS
PROC_TCK — F11 H_TCK
PROC_TRST# — F12 H_TRST_N
PROC_PREQ# — B9 H_PREQ_N
PROC_PRDY# — B10 H_PRDY_N

CFG_RCOMP — M11 — CFG_RCOMP — R415 49D9R2F-GP

H_TRST_N — R406 — 0R0402-PAD-2-GP — H_TRST_N_R

H_TDO
H_TDI
H_TMS

2015/11/20 Rossi
Remove for Hang up

- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_(THERMAL/CLOCK/PM/CFG)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 4 of 107

CHANNEL A DIMM0

11 M_A_DQ[63..0]
11 M_A_A[13..0]
11 M_A_DQS_DP[7..0]
11 M_A_DQS_DN[7..0]
11 M_A_BA[1..0]
11 M_A_BG[1..0]

11 M_A_CLK0
11 M_A_CLK#0
11 M_A_CLK1
11 M_A_CLK#1
11 M_A_CS#[1..0]

11 M_A_ACT#
11 M_A_ODT0
11 M_A_ODT1
11 M_A_CKE0
11 M_A_CKE1
11 M_A_CAS#
11 M_A_WE#
11 M_A_RAS#
11 M_A_ALERT#
11 M_A_PAR

2014/8/5
Change CPU P/N to 062.10015.0081

CPU1A — SKYLAKE — 1 OF 12 — LGA1151

M_A_DQ0	AE38	DDR0_DQ0	
M_A_DQ1	AE37	DDR0_DQ1	
M_A_DQ2	AG38	DDR0_DQ2	
M_A_DQ3	AG37	DDR0_DQ3	
M_A_DQ4	AE39	DDR0_DQ4	
M_A_DQ5	AE40	DDR0_DQ5	
M_A_DQ6	AG39	DDR0_DQ6	
M_A_DQ7	AG40	DDR0_DQ7	
M_A_DQ8	AJ38	DDR0_DQ8	
M_A_DQ9	AJ37	DDR0_DQ9	
M_A_DQ10	AL38	DDR0_DQ10	
M_A_DQ11	AL37	DDR0_DQ11	
M_A_DQ12	AJ40	DDR0_DQ12	
M_A_DQ13	AJ39	DDR0_DQ13	
M_A_DQ14	AL39	DDR0_DQ14	
M_A_DQ15	AL40	DDR0_DQ15	
M_A_DQ16	AN38	DDR0_DQ16/DDR0_DQ32	
M_A_DQ17	AN40	DDR0_DQ17/DDR0_DQ33	
M_A_DQ18	AR38	DDR0_DQ18/DDR0_DQ34	
M_A_DQ19	AR37	DDR0_DQ19/DDR0_DQ35	
M_A_DQ20	AN39	DDR0_DQ20/DDR0_DQ36	
M_A_DQ21	AN37	DDR0_DQ21/DDR0_DQ37	
M_A_DQ22	AR39	DDR0_DQ22/DDR0_DQ38	
M_A_DQ23	AR40	DDR0_DQ23/DDR0_DQ39	
M_A_DQ24	AW37	DDR0_DQ24/DDR0_DQ40	
M_A_DQ25	AU38	DDR0_DQ25/DDR0_DQ41	
M_A_DQ26	AV35	DDR0_DQ26/DDR0_DQ42	
M_A_DQ27	AW35	DDR0_DQ27/DDR0_DQ43	
M_A_DQ28	AU37	DDR0_DQ28/DDR0_DQ44	
M_A_DQ29	AV37	DDR0_DQ29/DDR0_DQ45	
M_A_DQ30	AT35	DDR0_DQ30/DDR0_DQ46	
M_A_DQ31	AU35	DDR0_DQ31/DDR0_DQ47	
M_A_DQ32	AY8	DDR0_DQ32/DDR1_DQ0	
M_A_DQ33	AW8	DDR0_DQ33/DDR1_DQ1	
M_A_DQ34	AV6	DDR0_DQ34/DDR1_DQ2	
M_A_DQ35	AU6	DDR0_DQ35/DDR1_DQ3	
M_A_DQ36	AU8	DDR0_DQ36/DDR1_DQ4	
M_A_DQ37	AV8	DDR0_DQ37/DDR1_DQ5	
M_A_DQ38	AW6	DDR0_DQ38/DDR1_DQ6	
M_A_DQ39	AY6	DDR0_DQ39/DDR1_DQ7	
M_A_DQ40	AY4	DDR0_DQ40/DDR1_DQ8	
M_A_DQ41	AV4	DDR0_DQ41/DDR1_DQ9	
M_A_DQ42	AT1	DDR0_DQ42/DDR1_DQ10	
M_A_DQ43	AT2	DDR0_DQ43/DDR1_DQ11	
M_A_DQ44	AV3	DDR0_DQ44/DDR1_DQ12	
M_A_DQ45	AW4	DDR0_DQ45/DDR1_DQ13	
M_A_DQ46	AT4	DDR0_DQ46/DDR1_DQ14	
M_A_DQ47	AT3	DDR0_DQ47/DDR1_DQ15	
M_A_DQ48	AP2	DDR0_DQ48/DDR1_DQ32	
M_A_DQ49	AM4	DDR0_DQ49/DDR1_DQ33	
M_A_DQ50	AP3	DDR0_DQ50/DDR1_DQ34	
M_A_DQ51	AM3	DDR0_DQ51/DDR1_DQ35	
M_A_DQ52	AP4	DDR0_DQ52/DDR1_DQ36	
M_A_DQ53	AM2	DDR0_DQ53/DDR1_DQ37	
M_A_DQ54	AP1	DDR0_DQ54/DDR1_DQ38	
M_A_DQ55	AM1	DDR0_DQ55/DDR1_DQ39	
M_A_DQ56	AK3	DDR0_DQ56/DDR1_DQ40	
M_A_DQ57	AH1	DDR0_DQ57/DDR1_DQ41	
M_A_DQ58	AK4	DDR0_DQ58/DDR1_DQ42	
M_A_DQ59	AH2	DDR0_DQ59/DDR1_DQ43	
M_A_DQ60	AH4	DDR0_DQ60/DDR1_DQ44	
M_A_DQ61	AK2	DDR0_DQ61/DDR1_DQ45	
M_A_DQ62	AH3	DDR0_DQ62/DDR1_DQ46	
M_A_DQ63	AK1	DDR0_DQ63/DDR1_DQ47	
	AU33	DDR0_ECC0	
	AT33	DDR0_ECC1	
	AW33	DDR0_ECC2	
	AV31	DDR0_ECC3	
	AU31	DDR0_ECC4	
	AV33	DDR0_ECC5	
	AW31	DDR0_ECC6	
	AY31	DDR0_ECC7	

DDR CHANNEL A

	AW18	DDR0_CKP0	M_A_CLK0
	AV18	DDR0_CKN0	M_A_CLK#0
	AW17	DDR0_CKP1	M_A_CLK1
	AV17	DDR0_CKN1	M_A_CLK#1
	AW16	DDR0_CKP2	
	AV16	DDR0_CKN2	
	AT16	DDR0_CKP3	
	AU16	DDR0_CKN3	
	AY24	DDR0_CKE0	M_A_CKE0
	AW24	DDR0_CKE1	M_A_CKE1
	AV24	DDR0_CKE2	
	AV25	DDR0_CKE3	
	AW12	DDR0_CS#0	M_A_CS#0
	AU11	DDR0_CS#1	M_A_CS#1
	AV13	DDR0_CS#2	
	AV10	DDR0_CS#3	
	AW11	DDR0_ODT0	M_A_ODT0
	AU14	DDR0_ODT1	M_A_ODT1
	AU12	DDR0_ODT2	
	AV10	DDR0_ODT3	
	AY13	DDR0_BA0/DDR0_CAB4/DDR0_BA0	M_A_BA0
	AV15	DDR0_BA1/DDR0_CAB6/DDR0_BA1	M_A_BA1
	AW23	DDR0_BA2/DDR0_CAA5/DDR0_BG0	M_A_BG0
	AW13	DDR0_RAS#/DDR0_CAB3/DDR0_MA16	M_A_RAS#
	AV14	DDR0_WE#/DDR0_CAB2/DDR0_MA14	M_A_WE#
	AY11	DDR0_CAS#/DDR0_CAB1/DDR0_MA15	M_A_CAS#
	AW15	DDR0_MA0/DDR0_CAB9/DDR0_MA0	M_A_A0
	AU18	DDR0_MA1/DDR0_CAB8/DDR0_MA1	M_A_A1
	AU17	DDR0_MA2/DDR0_CAB5/DDR0_MA2	M_A_A2
	AV19	DDR0_MA3	M_A_A3
	AT19	DDR0_MA4	M_A_A4
	AU20	DDR0_MA5/DDR0_CAA0/DDR0_MA5	M_A_A5
	AV20	DDR0_MA6/DDR0_CAA2/DDR0_MA6	M_A_A6
	AU21	DDR0_MA7/DDR0_CAA4/DDR0_MA7	M_A_A7
	AT20	DDR0_MA8/DDR0_CAA3/DDR0_MA8	M_A_A8
	AT22	DDR0_MA9/DDR0_CAA1/DDR0_MA9	M_A_A9
	AY14	DDR0_MA10/DDR0_CAB7/DDR0_MA10	M_A_A10
	AU22	DDR0_MA11/DDR0_CAA7/DDR0_MA11	M_A_A11
	AV22	DDR0_MA12/DDR0_CAA6/DDR0_MA12	M_A_A12
	AV12	DDR0_MA13/DDR0_CAB0/DDR0_MA13	M_A_A13
	AV23	DDR0_MA14/DDR0_CAA9/DDR0_BG1	M_A_BG1
	AU24	DDR0_MA15/DDR0_CAA8/DDR0_ACT#	M_A_ACT#
	AY15	DDR0_PAR	M_A_PAR
	AT23	DDR0_ALERT#	M_A_ALERT#
	AF39	DDR0_DQSN0	M_A_DQS_DN0
	AK39	DDR0_DQSN1	M_A_DQS_DN1
	AP39	DDR0_DQSN2/DDR0_DQSN4	M_A_DQS_DN2
	AU36	DDR0_DQSN3/DDR0_DQSN5	M_A_DQS_DN3
	AW7	DDR0_DQSN4/DDR1_DQSN0	M_A_DQS_DN4
	AU3	DDR0_DQSN5/DDR1_DQSN1	M_A_DQS_DN5
	AN3	DDR0_DQSN6/DDR1_DQSN4	M_A_DQS_DN6
	AJ3	DDR0_DQSN7/DDR1_DQSN5	M_A_DQS_DN7
	AF38	DDR0_DQSP0	M_A_DQS_DP0
	AK38	DDR0_DQSP1	M_A_DQS_DP1
	AP38	DDR0_DQSP2/DDR0_DQSP4	M_A_DQS_DP2
	AV36	DDR0_DQSP3/DDR0_DQSP5	M_A_DQS_DP3
	AV7	DDR0_DQSP4/DDR1_DQSP0	M_A_DQS_DP4
	AU2	DDR0_DQSP5/DDR1_DQSP1	M_A_DQS_DP5
	AN2	DDR0_DQSP6/DDR1_DQSP4	M_A_DQS_DP6
	AJ2	DDR0_DQSP7/DDR1_DQSP5	M_A_DQS_DP7
	AV32	DDR0_DQSP8	
	AU32	DDR0_DQSN8	

SKYLAKE-1

<Core Design>

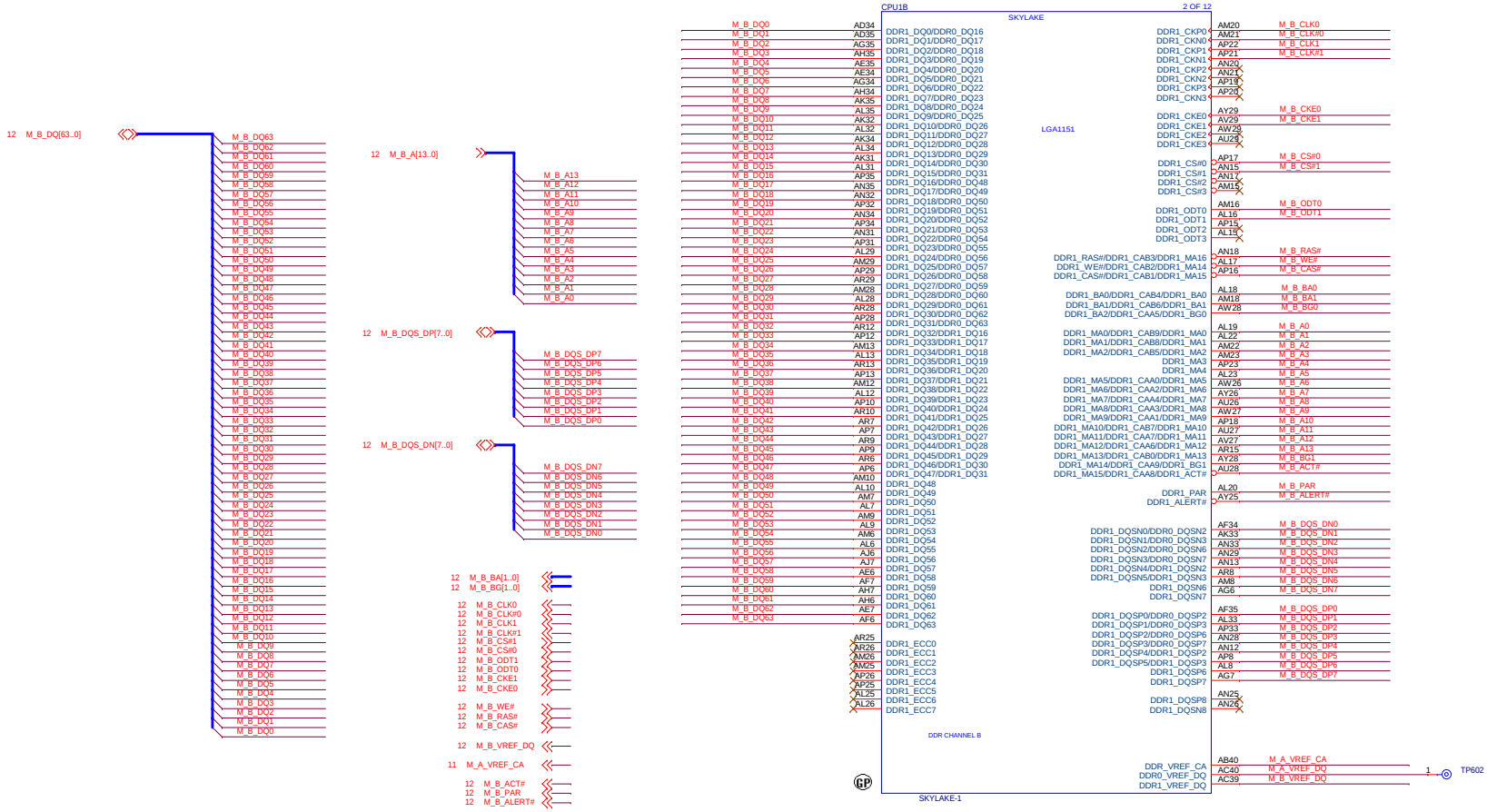
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_(DDR4 CHANNEL A)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

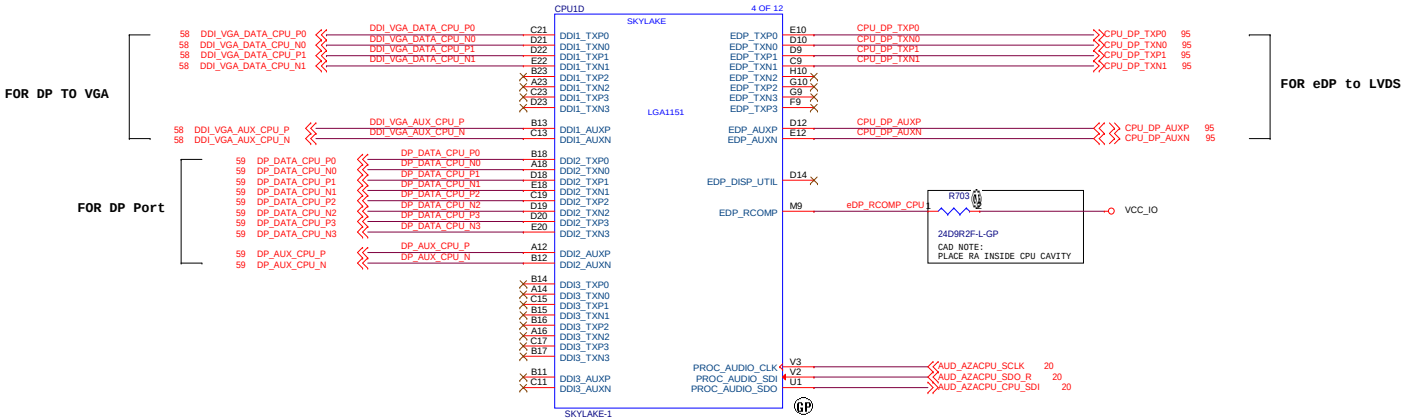
Date: Thursday, November 26, 2015 | Sheet 5 of 107



<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: CPU (DDR_CHB)		
Size: C	Document Number: Consumer AIO Woody	Rev: SA
Date: Thursday, November 26, 2015	Sheet 6 of 107	

2014/8/5
Change CPU P/N to 062.10015.0081



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU (DDI/EDP)

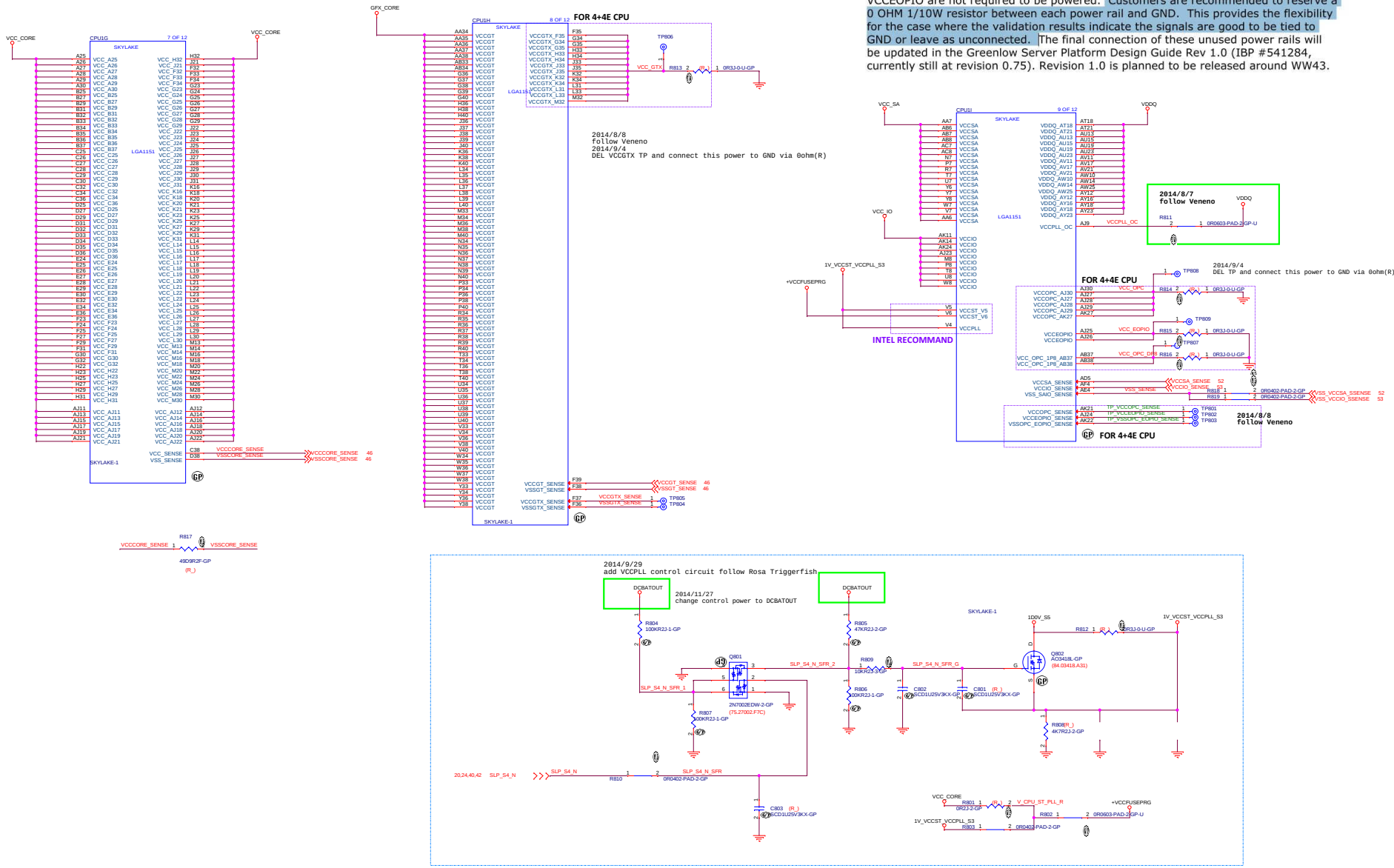
Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 7 of 107

Greenlow Server Reference Circuit: Unused Power Pins Handling

Greenlow Server Reference board Zumba Beach does not support pGFX and EDRAM, hence some of the power rails such as VCCGT, VCCGTX, VCC_OPC_1P8, VCCOPC and VCCEOPIO are not required to be powered. Customers are recommended to reserve a 0 OHM 1/10W resistor between each power rail and GND. This provides the flexibility for the case where the validation results indicate the signals are good to be tied to GND or leave as unconnected. The final connection of these unused power rails will be updated in the Greenlow Server Platform Design Guide Rev 1.0 (IBP #541284, currently still at revision 0.75). Revision 1.0 is planned to be released around WW43.

2014/8/5
Change CPU P/N to 062.10015.0081

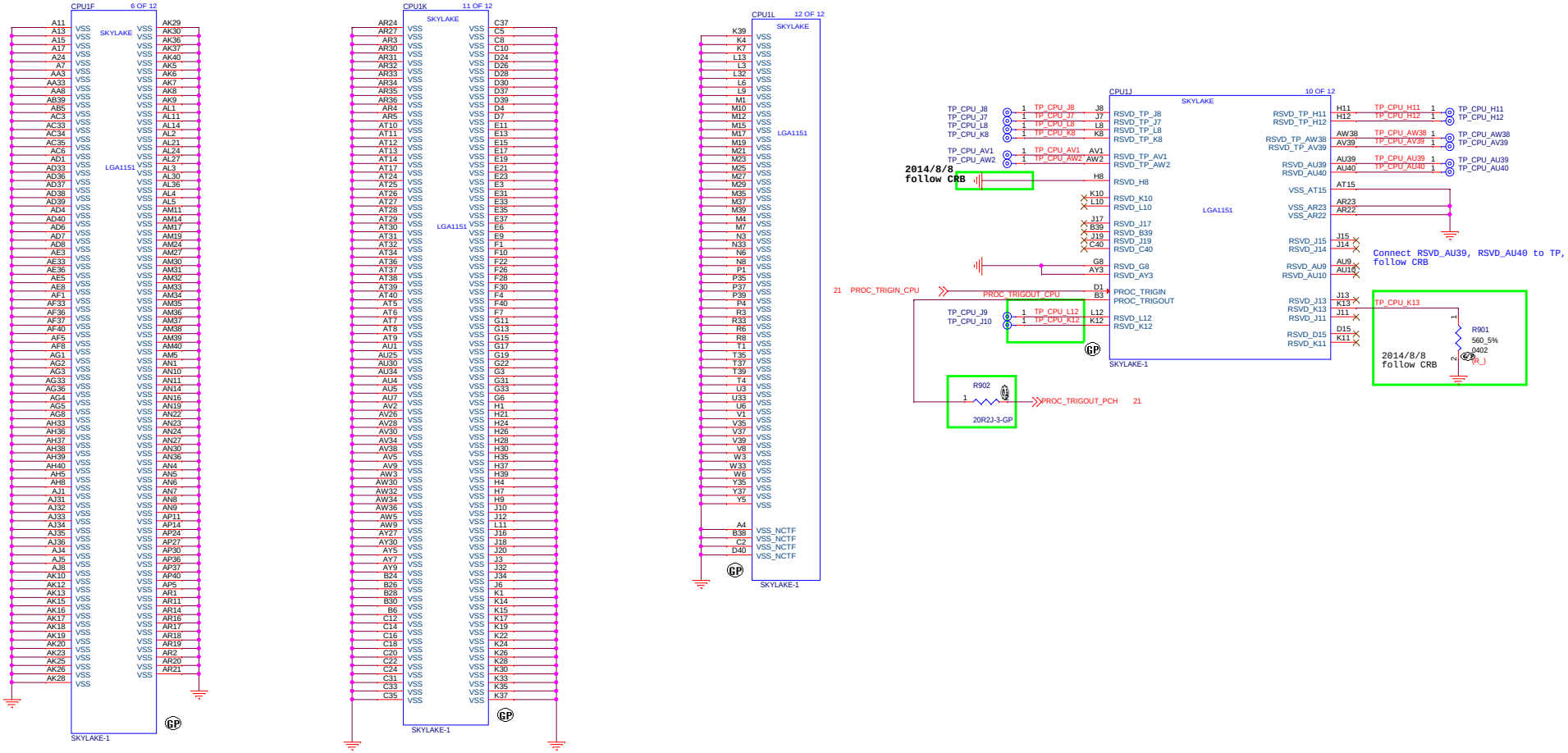


<Core Design>

wistron Wistron Incorporated
21F, 88, Sec.1 Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: CPU (CPU Power)
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA
Date: Thursday, November 26, 2015 | Sheet 8 of 107

2014/8/5
Change CPU P/N to 062.10015.0081



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU (VSS)

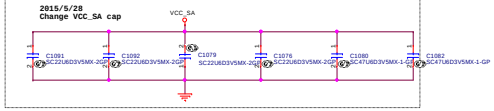
Size: C | Document Number: Consumer AIO Woody | Rev: SA

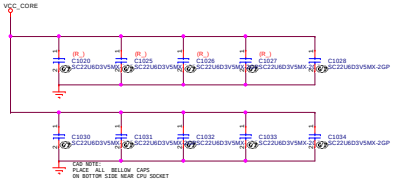
Date: Thursday, November 26, 2015 | Sheet 9 of 107

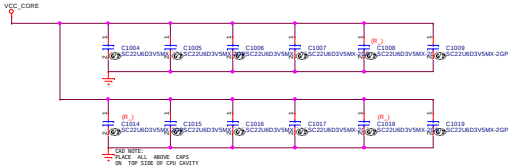
2014/8/8
DEL VCCOPC and VCCE0PIO power cap

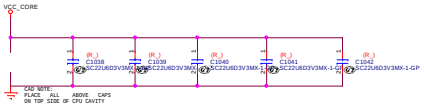
PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE

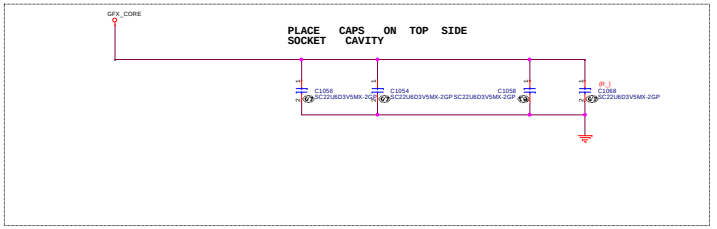
2015/5/28
Change VCC_SA cap

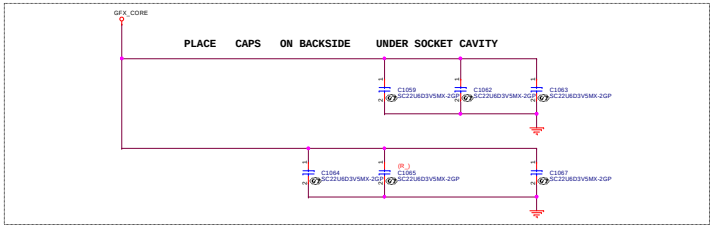


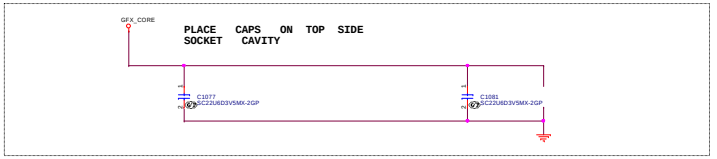






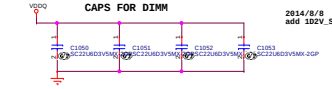




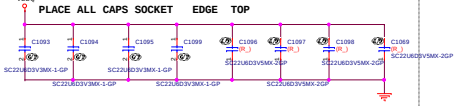


VDDQ
CAPS FOR DIMM

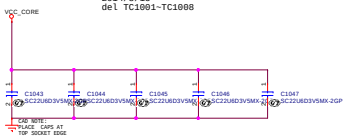
2014/8/8
add 1D2V_S3 cap



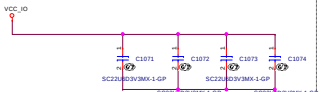
VDDQ
PLACE ALL CAPS SOCKET EDGE TOP



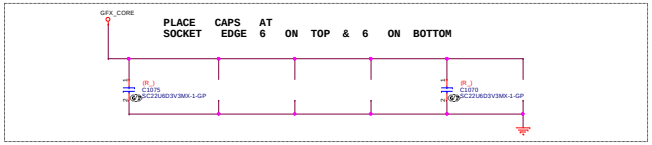
2014/8/15
del TC1001~TC1008

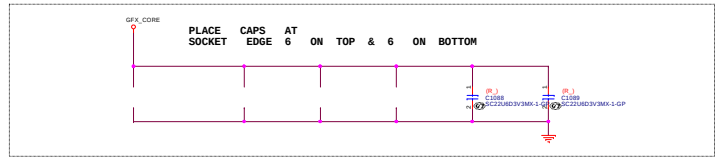


PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE

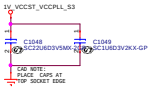


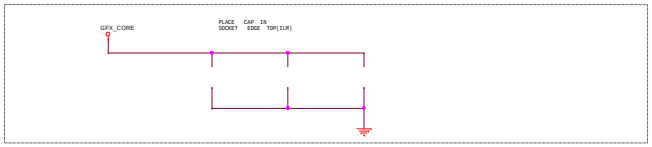
2014/8/8
add VCC_IO cap





PLACE ALL CAPS OUTSIDE CPU SOCKET CAVITY ON TOPSIDE





<Core Design>

wistron

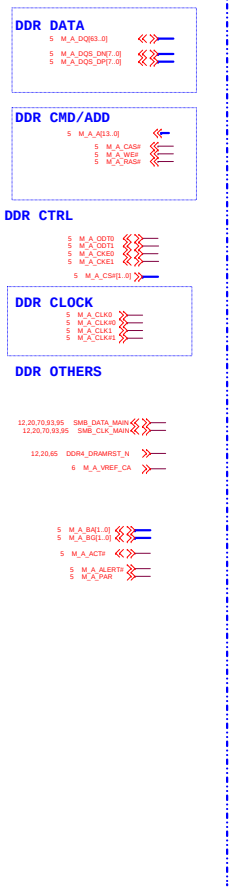
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

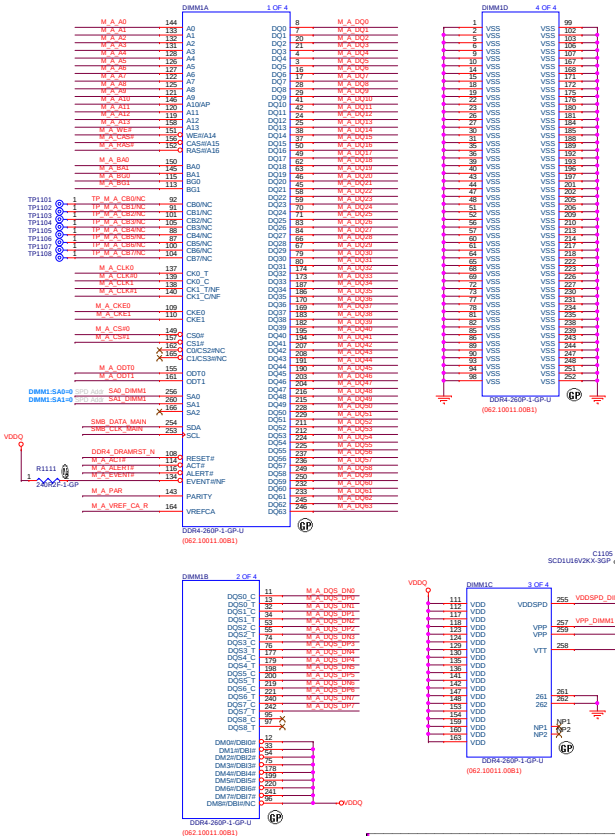
Title: CPU Power CAP

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 28, 2013 | Sheet 10 of 107

CHANNEL-A XMM1, A0, H=9.2mm

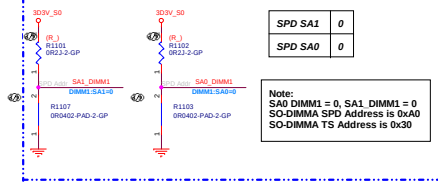




SM Bus 0							
Device	8-bit Address (hex)						
DIMM A0	A0						
DIMM A1	A4						
DIMM B0	A2						
DIMM B1	A6						
1	0	1	0	0	x	x	0

Note:0,3^7 Bit as default

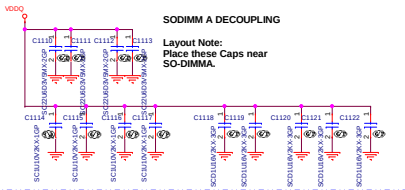
SPD Address of DIMM1



SPD SA1	0
SPD SA0	0

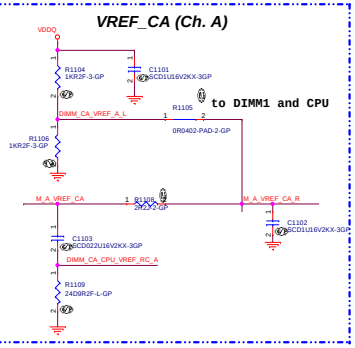
Note:
SA0 DIMM1 = 0, SA1_DIMM1 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

SODIMM A DECOUPLING



Layout Note:
Place these Caps near SO-DIMMA.

VREF_CA (Ch. A)



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File: DDR4 DIMM_1

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 11 of 107

CHANNEL-B DIMM2, A2, H=5.2mm

DDR DATA

6 M_B_DQ[63..0]
6 M_B_DQS_DN[7..0]
6 M_B_DQS_DP[7..0]

DDR CMD/ADD

6 M_B_A[13..0]
6 M_B_WE#
6 M_B_RAS#
6 M_B_CAS#
6 M_B_BA[1..0]
6 M_B_BG[1..0]

DDR CTRL

6 M_B_CS#1
6 M_B_CS#0
6 M_B_CKE1
6 M_B_CKE0
6 M_B_ODT0
6 M_B_ODT1

DDR CLOCK

6 M_B_CLK0
6 M_B_CLK#0
6 M_B_CLK1
6 M_B_CLK#1

DDR OTHERS

11,20,65 DDR4_DRAMRST_N
11,20,70,93,95 SMB_DATA_MAIN
11,20,70,93,95 SMB_CLK_MAIN

6 M_B_ACT#
6 M_B_PAR
6 M_B_ALERT#
6 M_B_VREF_DQ

DIMM2A 1 OF 4

M_B_RAS# 152 RAS#/A16 DQ63 246 M_B_DQ63
M_B_CAS# 150 CAS#/A15 DQ62 245 M_B_DQ62
M_B_WE# 151 WE#/A14 DQ61 233 M_B_DQ61
M_B_A13 108 A13 DQ60 232 M_B_DQ60
M_B_A12 119 A12 DQ59 250 M_B_DQ59
M_B_A11 120 A11 DQ58 249 M_B_DQ58
M_B_A10 146 A10/AP DQ57 236 M_B_DQ57
M_B_A9 121 A9 DQ56 237 M_B_DQ56
M_B_A8 125 A8 DQ55 225 M_B_DQ55
M_B_A7 122 A7 DQ54 224 M_B_DQ54
M_B_A6 127 A6 DQ53 212 M_B_DQ53
M_B_A5 126 A5 DQ52 211 M_B_DQ52
M_B_A4 128 A4 DQ51 229 M_B_DQ51
M_B_A3 131 A3 DQ50 228 M_B_DQ50
M_B_A2 132 A2 DQ49 215 M_B_DQ49
M_B_A1 133 A1 DQ48 216 M_B_DQ48
M_B_A0 144 A0 DQ47 204 M_B_DQ47
203 M_B_DQ46
M_B_BA1 145 BA1 DQ45 190 M_B_DQ45
M_B_BA0 150 BA0 DQ44 191 M_B_DQ44
M_B_BG1 113 BG1 DQ43 208 M_B_DQ43
M_B_BG0 115 BG0 DQ42 207 M_B_DQ42
194 M_B_DQ41
M_B_CLK1 138 CK1_T/NF DQ40 195 M_B_DQ40
M_B_CLK1# 140 CK1_C/NF DQ39 182 M_B_DQ39
M_B_CLK0 137 CK0_T DQ38 183 M_B_DQ38
M_B_CLK0# 139 CK0_C DQ37 169 M_B_DQ37
170 M_B_DQ36
M_B_CS#1 157 CS1# DQ35 186 M_B_DQ35
M_B_CS#0 148 CS0# DQ34 187 M_B_DQ34
173 M_B_DQ33
M_B_CKE1 110 CKE1 DQ32 174 M_B_DQ32
M_B_CKE0 109 CKE0 DQ31 80 M_B_DQ31
79 M_B_DQ30
M_B_ODT1 161 ODT1 DQ29 67 M_B_DQ29
M_B_ODT0 155 ODT0 DQ28 66 M_B_DQ28
64 M_B_DQ27
C1/CS3#/NC DQ26 83 M_B_DQ26
C0/CS2#/NC DQ25 71 M_B_DQ25
70 M_B_DQ24
CB7/NC DQ23 59 M_B_DQ23
CB6/NC DQ22 58 M_B_DQ22
CB5/NC DQ21 46 M_B_DQ21
CB4/NC DQ20 45 M_B_DQ20
CB3/NC DQ19 62 M_B_DQ19
CB2/NC DQ18 49 M_B_DQ18
CB1/NC DQ17 50 M_B_DQ17
CB0/NC DQ16 37 M_B_DQ16
38 M_B_DQ15
PARITY DQ14 25 M_B_DQ14
RESET# DQ13 24 M_B_DQ13
DQ12 42 M_B_DQ12
M_B_EVENT# 134 EVENT#/NF DQ11 41 M_B_DQ11
M_B_ALERT# 116 ALERT# DQ10 29 M_B_DQ10
M_B_ACT# 114 ACT# DQ9 28 M_B_DQ9
VDDSPD_DIMM2 255 VDDSPD DQ8 17 M_B_DQ8
DQ7 16 M_B_DQ7
SA2 DQ6 3 M_B_DQ6
SA1 DQ5 4 M_B_DQ5
SA0 DQ4 21 M_B_DQ4
DQ3 20 M_B_DQ3
SDA DQ2 7 M_B_DQ2
SCL DQ1 8 M_B_DQ1
VREFCA DQ0 6 M_B_DQ0

DDR4-260P-GP-U1
(062.10011.00C1)

DIMM2D 4 OF 4

VSS 1 99
VSS 2 102
VSS 5 103
VSS 6 106
VSS 9 107
VSS 10 167
VSS 14 168
VSS 15 171
VSS 18 172
VSS 19 175
VSS 22 176
VSS 23 180
VSS 26 181
VSS 27 184
VSS 30 185
VSS 31 188
VSS 35 189
VSS 36 192
VSS 39 193
VSS 40 196
VSS 43 197
VSS 44 201
VSS 47 202
VSS 48 205
VSS 51 206
VSS 52 209
VSS 56 210
VSS 57 213
VSS 60 214
VSS 61 217
VSS 64 218
VSS 65 222
VSS 68 223
VSS 69 226
VSS 72 227
VSS 73 230
VSS 77 231
VSS 78 234
VSS 81 235
VSS 82 238
VSS 85 239
VSS 86 243
VSS 89 244
VSS 90 247
VSS 93 248
VSS 94 251
VSS 98 252

DDR4-260P-GP-U1
(062.10011.00C1)

TP1210 TP_M_B_C1/CS3_N/NC
TP1209 TP_M_B_C0/CS2#/NC
TP1208 TP_M_B_CB7/NC
TP1207 TP_M_B_CB6/NC
TP1206 TP_M_B_CB5/NC
TP1205 TP_M_B_CB4/NC
TP1204 TP_M_B_CB3/NC
TP1203 TP_M_B_CB2/NC
TP1202 TP_M_B_CB1/NC
TP1201 TP_M_B_CB0/NC

VDDQ
3D3V_S0
R1205 240R2F-2-GP
R1207 0R0603-PAD-2-GP-U
C1206 SCD1U16V2KX-3GP
C1205 SCD1U16V2KX-3GP
DIMM2:SA1=1 SPD Addr SA1_DIMM2
DIMM2:SA0=0 SPD Addr SA0_DIMM2

DIMM2B 2 OF 4

DQS8_T 97
DQS8_C 95
DQS7_T 242
DQS7_C 240
DQS6_T 221
DQS6_C 219
DQS5_T 200
DQS5_C 198
DQS4_T 179
DQS4_C 177
DQS3_T 76
DQS3_C 74
DQS2_T 55
DQS2_C 53
DQS1_T 34
DQS1_C 32
DQS0_T 13
DQS0_C 11
96
DM8#/DBI#/NC 241
DM7#/DBI7# 220
DM6#/DBI6# 199
DM5#/DBI5# 178
DM4#/DBI4# 75
DM3#/DBI3# 54
DM2#/DBI2# 33
DM1#/DBI# 12
DM0#/DBI0# 9

M_B_DQS_DP7
M_B_DQS_DN7
M_B_DQS_DP6
M_B_DQS_DN6
M_B_DQS_DP5
M_B_DQS_DN5
M_B_DQS_DP4
M_B_DQS_DN4
M_B_DQS_DP3
M_B_DQS_DN3
M_B_DQS_DP2
M_B_DQS_DN2
M_B_DQS_DP1
M_B_DQS_DN1
M_B_DQS_DP0
M_B_DQS_DN0

VDDQ

DDR4-260P-GP-U1
(062.10011.00C1)

DIMM2C 3 OF 4

VDD 111
VDD 117
VDD 123
VDD 129
VDD 135
VDD 141
VDD 147
VDD 153
VDD 159
VDD 112
VDD 118
VDD 124
VDD 130
VDD 136
VDD 142
VDD 148
VDD 154
VDD 160
VDD 163
261
262
VPP 257
VPP 259
NP1 258
NP2
VTT

VDDQ
2D5V_VPP
R1206 0R0402-PAD-2-GP
C1201 SCD1U16V2KX-3GP
C1202 SCD1U16V2KX-3GP
0D6V_VTT_S0
C1203 SC4D7U6D3V3KX-GP
C1204 SCD1U16V2KX-3GP

Place these caps close to VTT1 and VTT2.

SPD Address of DIMM2

3D3V_S0
R1201 0R0402-PAD-2-GP
SPD Addr SA1_DIMM2
DIMM2:SA1=1
(R_)
R1203 0R2J-2-GP
3D3V_S0
(R_)
R1202 0R2J-2-GP
SPD Addr SA0_DIMM2
DIMM2:SA0=0
R1204 0R0402-PAD-2-GP

SPD SA1	1
SPD SA0	0

Note:
SA0 DIMM2 = 0, SA1_DIMM2 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM B DECOUPLING

VDDQ
C1213 SCD1U16V2KX-3GP
C1214 SCD1U16V2KX-3GP
C1215 SCD1U16V2KX-3GP
C1225 SCD1U16V2KX-3GP
C1216 SCD1U16V2KX-3GP
C1217 SCD1U16V2KX-3GP
C1218 SCD1U16V2KX-3GP
C1219 SCD1U16V2KX-3GP
C1220 SCD1U16V2KX-3GP
C1221 SCD1U16V2KX-3GP
C1222 SCD1U16V2KX-3GP
C1223 SCD1U16V2KX-3GP
C1224 SCD1U16V2KX-3GP

Layout Note:
Place these Caps near SO-DIMMA.

VREF_DQ (Ch. B)

VDDQ
R1211 1KR2F-3-GP
C1208 SCD1U16V2KX-3GP
DIMM_CA_VREF_B_L
R1212 0R0402-PAD-2-GP
to DIMM2 and CPU
R1208 1KR2F-3-GP
C1211 SCD1U16V2KX-3GP
M_B_VREF_DQ
R1209 240R2F-GP
M_B_VREF_CA_R
C1210 SCD022U16V2KX-3GP
C1209 SCD1U16V2KX-3GP
C1207 SCD1U16V2KX-3GP
DIMM_CA_CPU_VREF_RC_B
R1210 240R2F-L-GP

SMBus 0							
Device	8-bit Address (hex)						
DIMM A0	A0						
DIMM A1	A4						
DIMM B0	A2						
DIMM B1	A6						
1	0	1	0	0	x	x	0

Note:0,3~7 Bit as default

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DDR4 DIMM_2
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 12 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DDR4 DIMM_3_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 13 of 107

Reserved

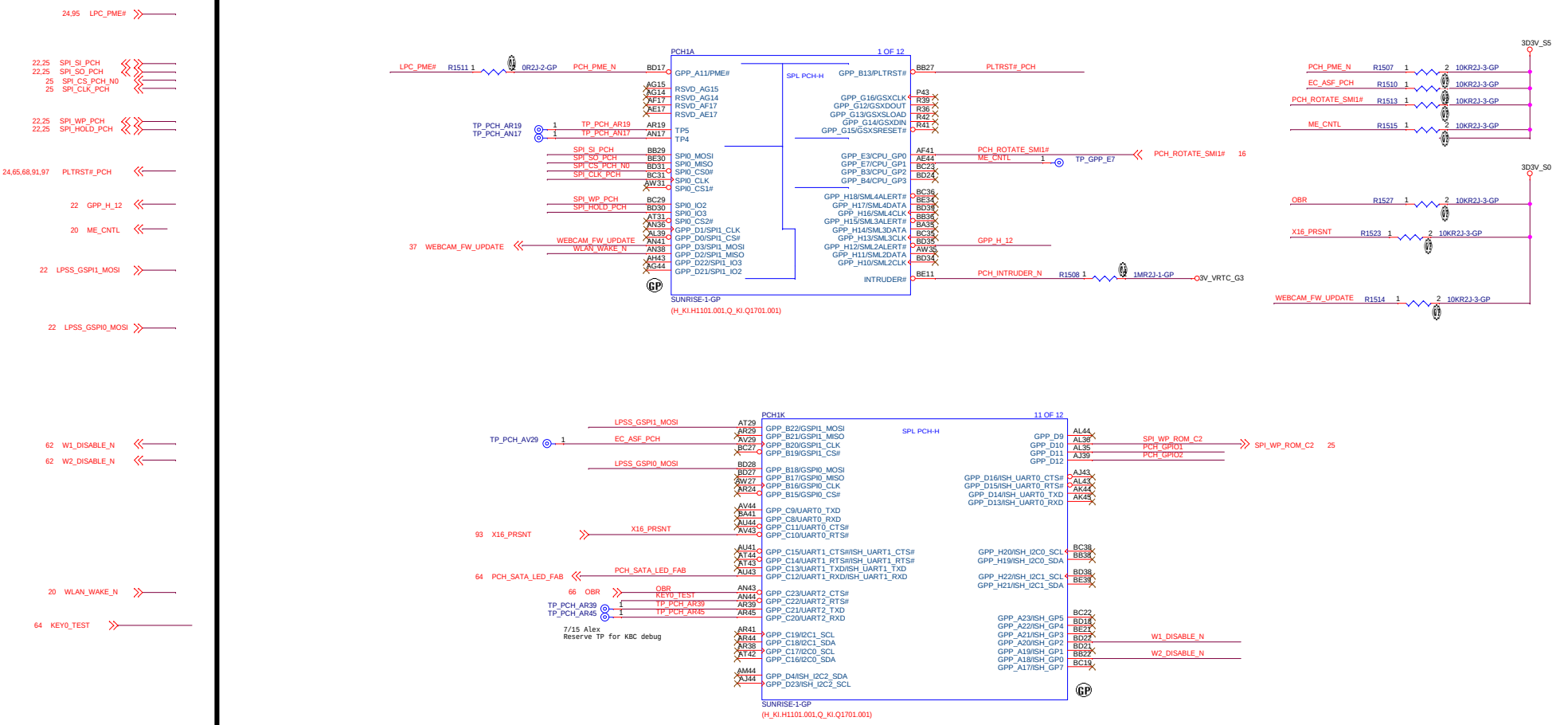
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DDR4 DIMM_4_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 14 of 107



<Core Design>

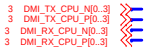
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (SPI/UART/I2C)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 15 of 107

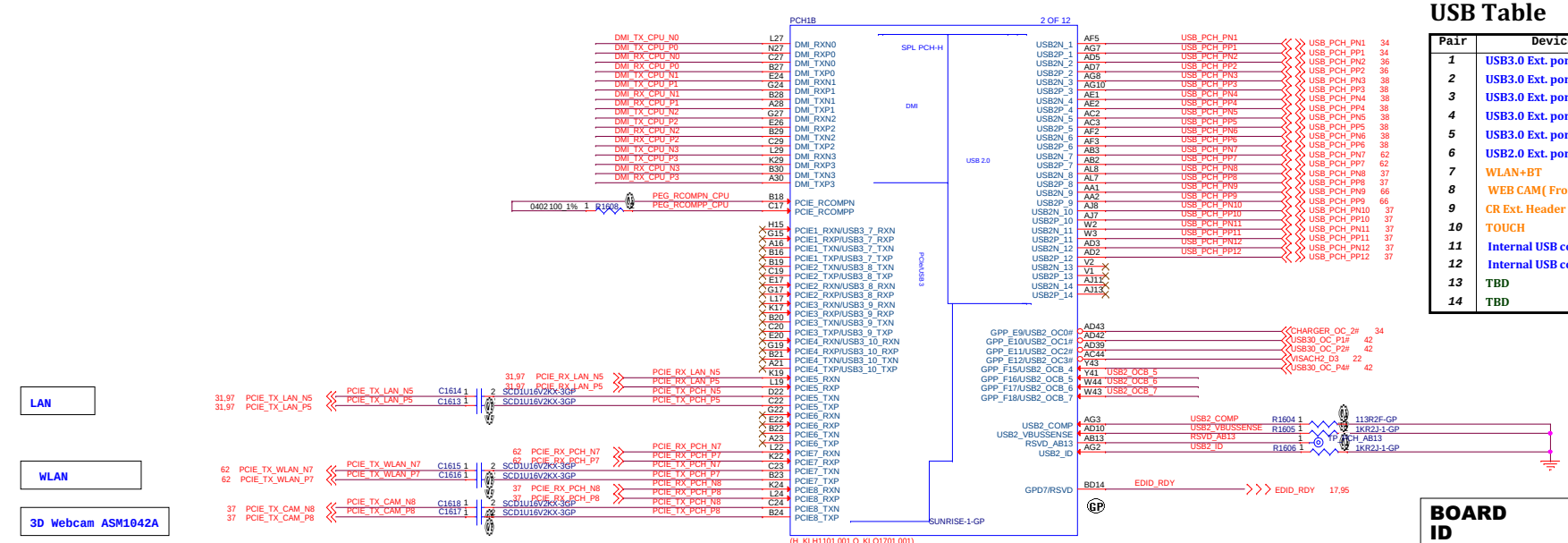
DMI



LAN

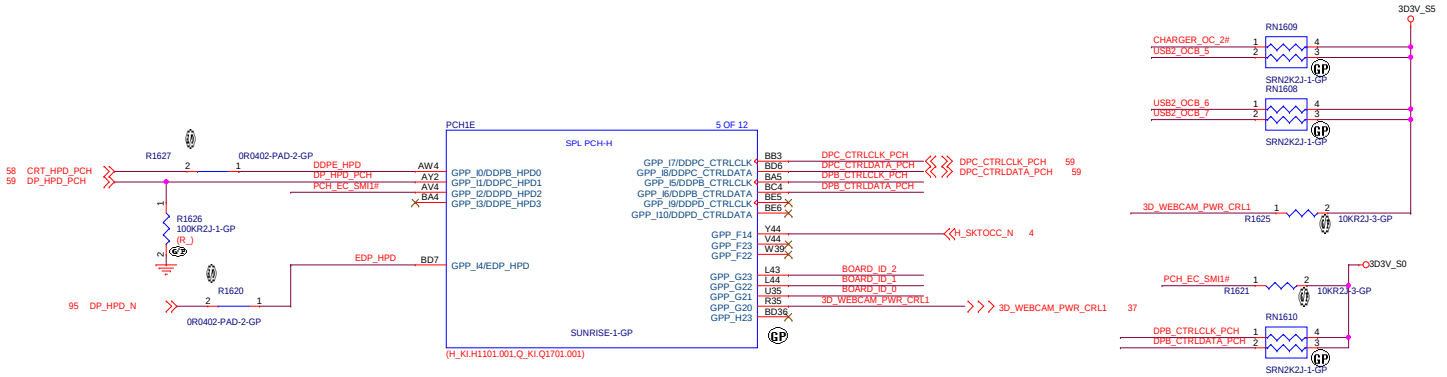
WLAN

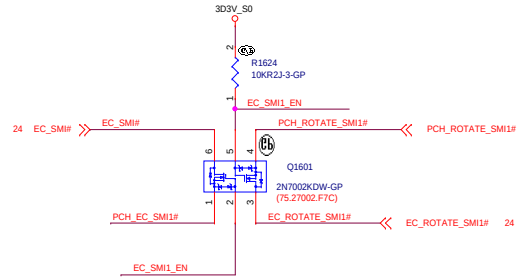
3D Webcam ASM1042A



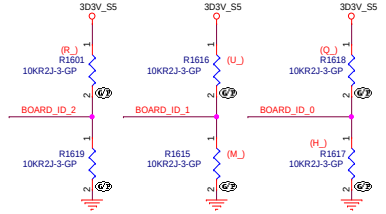
USB Table

Pair	Device
1	USB3.0 Ext. port 1 (Side)
2	USB3.0 Ext. port 2 (Rear)
3	USB3.0 Ext. port 3 (Rear)
4	USB3.0 Ext. port 4 (Rear)
5	USB3.0 Ext. port 5 (Rear)
6	USB2.0 Ext. port 5 (Rear)
7	WLAN+BT
8	WEB CAM(Front)
9	CR Ext. Header (Side)
10	TOUCH
11	Internal USB connector
12	Internal USB connector
13	TBD
14	TBD





BOARD ID



SB EC Board ID Description

H110	ID2 bit1	ID1 bit0
W/HDMI	0	0
W/O HDMI	0	1

	ID0
Q170	1
H110	0

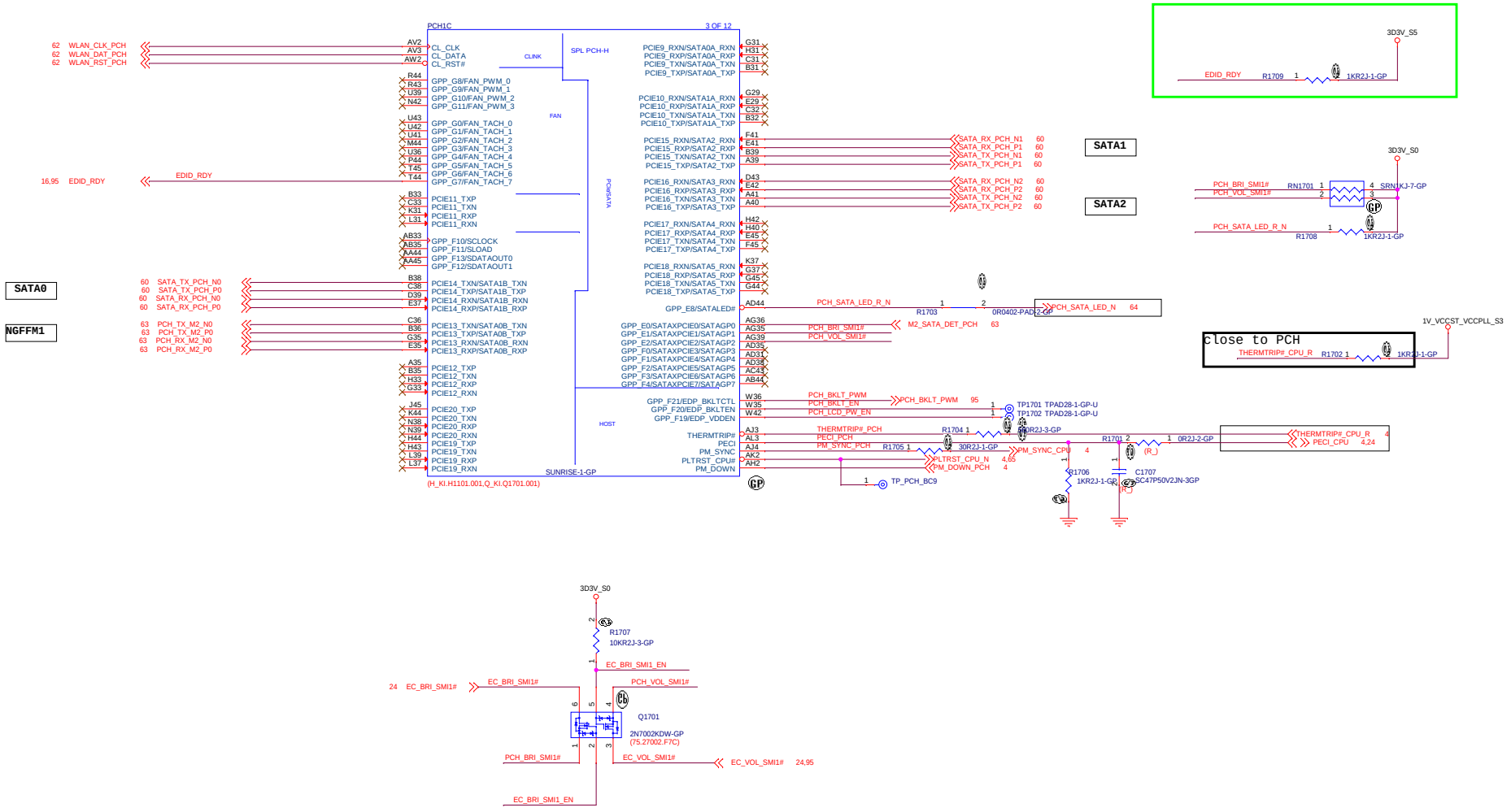
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (DMI/PCI-E/USB)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 16 of 107



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (PCI-E/SATA)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 17 of 107

6/21 Delete
CLKOUT_48 is only supported and enabled on SKL-H Server

2014/8/13 2.7K 1%
1V_VCCF24_Sx NEED CHECK
R1803 1 2K7R2F-GP
6/26 2.7K 0.5%
INTEL PDG: 2.71K 0.5%

TP_PCH_AR17 1
CLKOUT_48M_R
PCH1G 7 OF 12
AR17 GPP_A16/CLKOUT_48
SPL PCH-H

4 CPU_CLK24M_PCH
4 CPU_CLK24M_PCH#
G1 CLKOUT_CPUNSSC_P
F1 CLKOUT_CPUNSSC#

4 CPU_BCLK_PCH
4 CPU_BCLK_PCH#
G2 CLKOUT_CPUBCLK_P
H2 CLKOUT_CPUBCLK#

XTL_24M_OUT_PCH
XTL_24M_IN_PCH
A5 XTAL24_OUT
A6 XTAL24_IN

XCLK_BIASREF_PCH
E1 XCLK_BIASREF

XTL_32K_X1_PCH
XTL_32K_X2_PCH
BC9 RTCX1
BD10 RTCX2

62 PEG_CLKREQ1_WLAN#
31,97 PEG_CLKREQ2_LAN#
37 PEG_CLKREQ4_3D#
63 PEG_CLKREQ7_M2#
93 PEG_CLKREQ8_PCIE16#
PEG_CLKREQ7_M2#
PEG_CLKREQ8_PCIE16#

BC24 GPP_B5/SRCCLKREQ0#
AW24 GPP_B6/SRCCLKREQ1#
AT24 GPP_B7/SRCCLKREQ2#
BD25 GPP_B8/SRCCLKREQ3#
BB25 GPP_B9/SRCCLKREQ4#
BE25 GPP_B10/SRCCLKREQ5#
AT33 GPP_H0/SRCCLKREQ6#
AR31 GPP_H1/SRCCLKREQ7#
BD33 GPP_H2/SRCCLKREQ8#
BC32 GPP_H3/SRCCLKREQ9#
BB31 GPP_H4/SRCCLKREQ10#
BC33 GPP_H5/SRCCLKREQ11#
BA33 GPP_H6/SRCCLKREQ12#
AW33 GPP_H7/SRCCLKREQ13#
BB33 GPP_H8/SRCCLKREQ14#
BD33 GPP_H9/SRCCLKREQ15#

R13 R11 CLKOUT_PCIE_N15 CLKOUT_PCIE_P15
P1 R2 CLKOUT_PCIE_N14 CLKOUT_PCIE_P14
W7 Y5 CLKOUT_PCIE_N13 CLKOUT_PCIE_P13
U2 U3 CLKOUT_PCIE_N12 CLKOUT_PCIE_P12

SUNRISE-1-GP
(H_KI.H1101.001.Q_KI.Q1701.001)

CLKOUT_ITPXDP# L1
CLKOUT_ITPXDP_P L2
XDP_CLK_CON#
XDP_CLK_CON
CLK OUT for CPU XDP

CLKOUT_CPUPCIBCLK# J1
CLKOUT_CPUPCIBCLK_P J2
CPU_PCIBCLK_PCH# 4
CPU_PCIBCLK_PCH 4

CLKOUT_PCIE_N0 N7
CLKOUT_PCIE_P0 N8
CLKOUT_PCIE_N1 L7
CLKOUT_PCIE_P1 L5
PEG_CLK1_WLAN# 62
PEG_CLK1_WLAN 62
CLK OUT OF WLAN

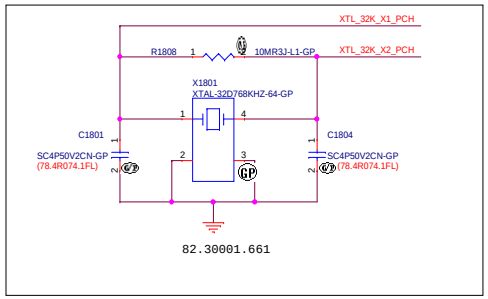
CLKOUT_PCIE_N2 D3
CLKOUT_PCIE_P2 F2
PEG_CLK2_LAN# 31,97
PEG_CLK2_LAN 31,97
CLK OUT OF PCIE for LAN

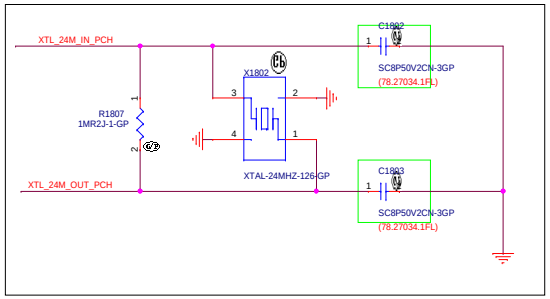
CLKOUT_PCIE_N3 E5
CLKOUT_PCIE_P3 G4
CLKOUT_PCIE_N4 D5
CLKOUT_PCIE_P4 E6
PEG_CLK4_3D# 37
PEG_CLK4_3D 37
CLK OUT OF PCIE for 3D WEBCAM

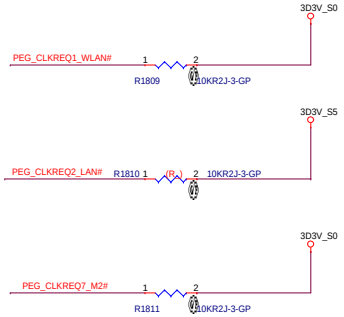
CLKOUT_PCIE_N5 D8
CLKOUT_PCIE_P5 D7
CLKOUT_PCIE_N6 R8
CLKOUT_PCIE_P6 R7
CLKOUT_PCIE_N7 U5
CLKOUT_PCIE_P7 U7
PEG_CLK7_M2# 63
PEG_CLK7_M2 63
CLK OUT OF NGFF for SSD

CLKOUT_PCIE_N8 W10
CLKOUT_PCIE_P8 W11
PEG_CLK8_PCH# 93
PEG_CLK8_PCH 93
CLK OUT OF PCIE for PCIEX16

CLKOUT_PCIE_N9 N3
CLKOUT_PCIE_P9 N2
CLKOUT_PCIE_N10 P3
CLKOUT_PCIE_P10 P2
CLKOUT_PCIE_N11 R3
CLKOUT_PCIE_P11 R4







<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH(CLOCK/CL)
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 18 of 107

PORT1 USB30 SIDE PORT

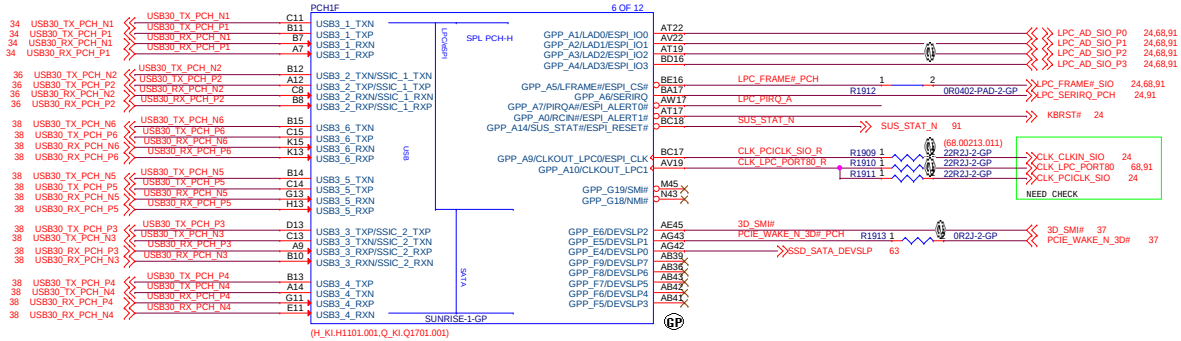
PORT2 USB30 REAR PORT

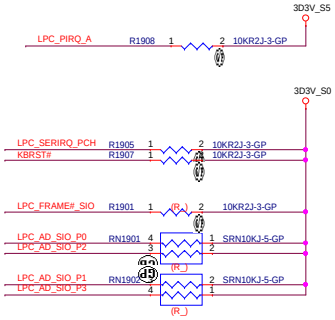
PORT6 USB30 REAR PORT

PORT5 USB30 REAR PORT

PORT3 USB30 REAR PORT

PORT4 USB30 REAR PORT





Integrated Pull-ups and Pull-downs

Signal	Resistor Type	Value	Notes
LAD[3:0]	Pull-up	15 - 40 KΩ	

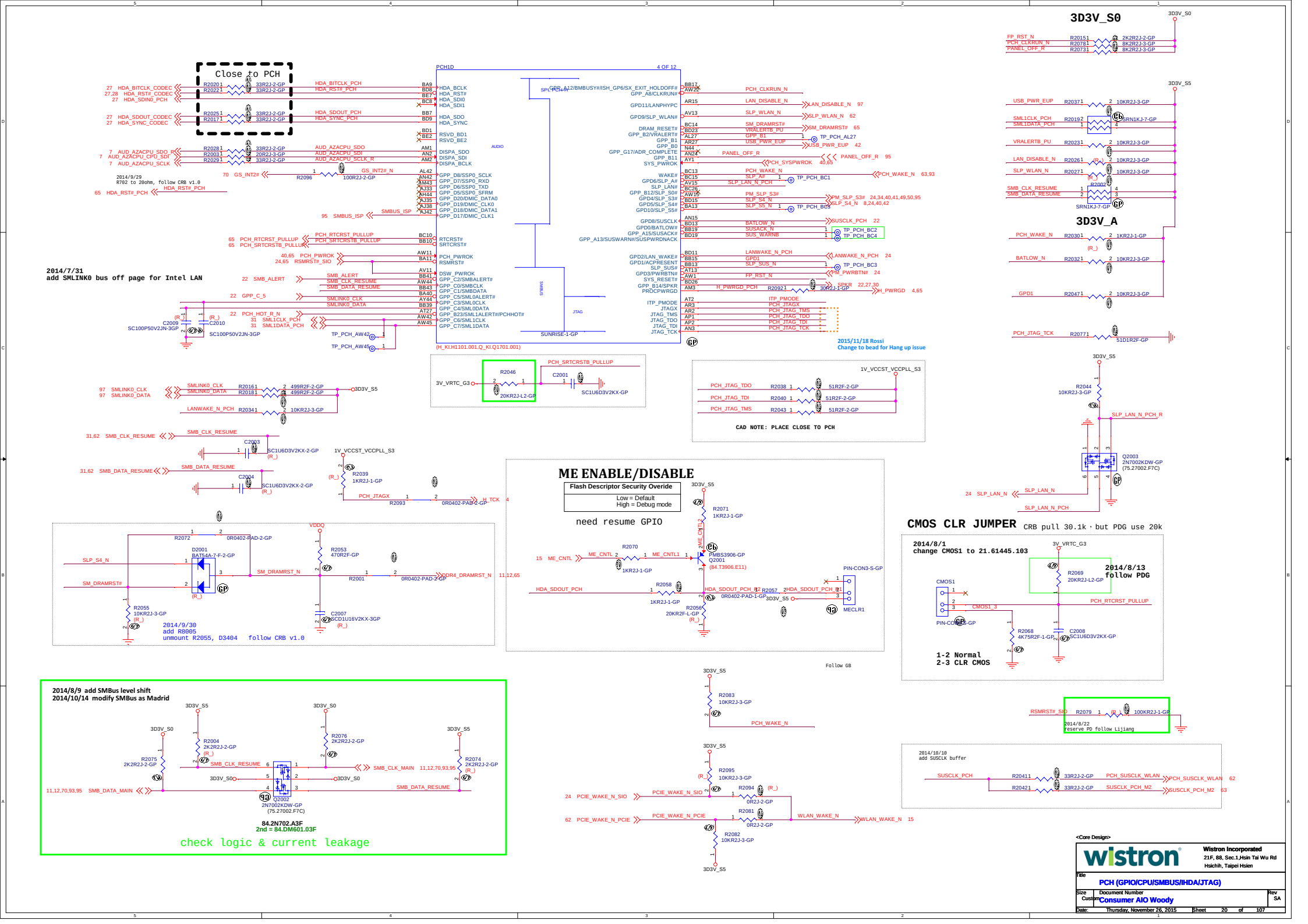
<Core Design>

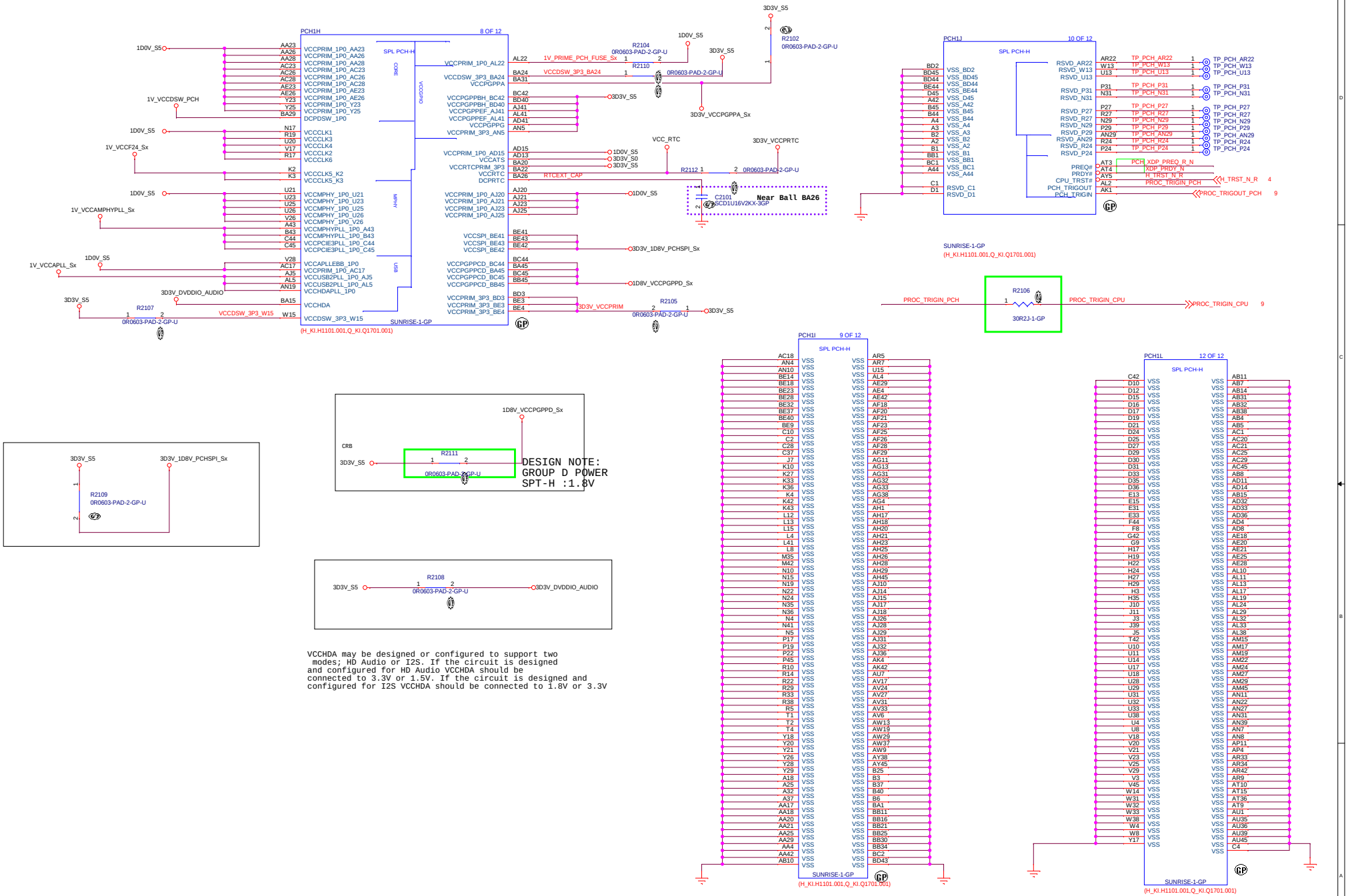
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (USB/ESPI

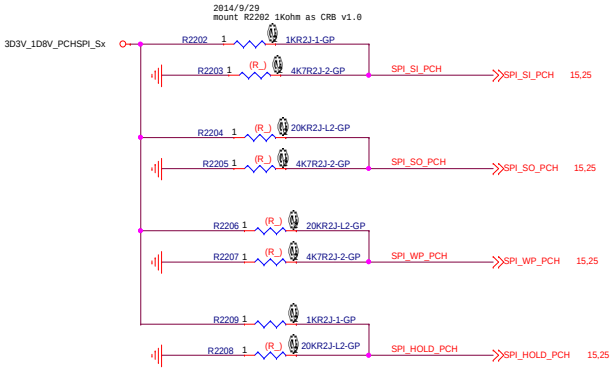
Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 19 of 107

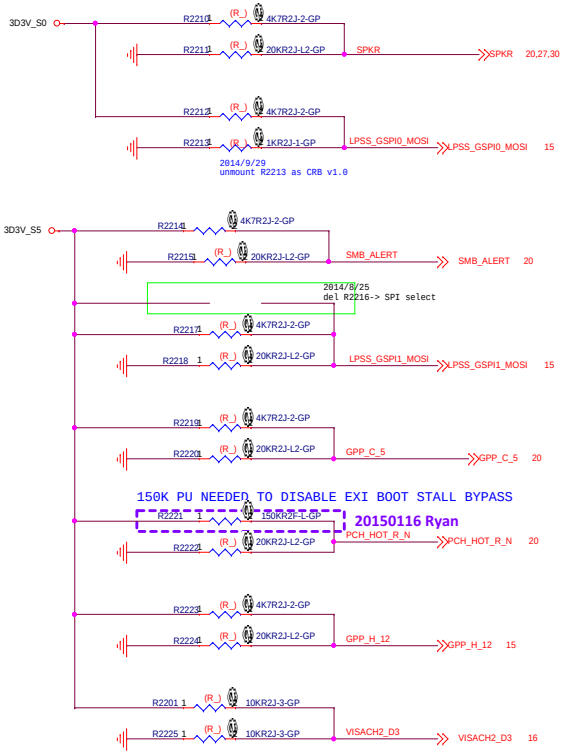

3D3V_S0
Close to PCH
PCH1D
4 OF 12
2014/7/31
add SMLINK0 bus off page for Intel LAN
2014/9/29
R702 to 20ohm, follow CRB v1.0
2015/11/18 Rossi
Change to bead for Hang up issue
1V_VCCST_VCCPLL_S3
CAD NOTE: PLACE CLOSE TO PCH
ME ENABLE/DISABLE
Flash Descriptor Security Overide
Low = Default
High = Debug mode
need resume GPIO
CMOS CLR JUMPER
CRB pull 30.1k , but PDG use 20k
2014/8/1
change CMOS1 to 21.61445.103
2014/8/13
follow PDG
1-2 Normal
2-3 CLR CMOS
2014/9/30
add R8005
unmount R2055, D3404 follow CRB v1.0
2014/8/9 add SMBus level shift
2014/10/14 modify SMBus as Madrid
84.2N702.A3F
2nd = 84.DM601.03F
check logic & current leakage
Follow GB
2014/8/22
reserve PD follow Lijiang
2014/10/10
add SUSCLK buffer
3D3V_S5
3D3V_A
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
PCH (GPIO/CPU/SMBUS/IHDA/JTAG)
Consumer AIO Woody
Thursday, November 26, 2015
Sheet 20 of 107


PCH1H
8 OF 12
SPL PCH-H
1D0V_S5
1V_VCCDSW_PCH
1V_VCCF24_Sx
1V_VCCAMPHYPLL_Sx
1V_VCCAPLL_Sx
3D3V_DVDDIO_AUDIO
3D3V_S5
VCCDSW_3P3_W15
SUNRISE-1-GP
(H_KI.H1101.001,Q_KI.Q1701.001)
R2107
0R0603-PAD-2-GP-U
R2102
R2104
R2110
R2112
R2105
C2101
SCD1U16V2KX-3GP
Near Ball BA26
VCC_RTC
3D3V_VCCPRTC
3D3V_VCCPGPPA_Sx
3D3V_1D8V_PCHSPI_Sx
1D8V_VCCPGPPD_Sx
3D3V_VCCPRIM
RTCEXT_CAP
PCH1J
10 OF 12
PROC_TRIGIN_PCH
PROC_TRIGIN_CPU
R2106
30R2J-1-GP
PCH1I
9 OF 12
PCH1L
12 OF 12
R2109
R2111
R2108
DESIGN NOTE:
GROUP D POWER
SPT-H :1.8V
VCCHDA may be designed or configured to support two modes; HD Audio or I2S. If the circuit is designed and configured for HD Audio VCCHDA should be connected to 1.8V or 3.3V
<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title
PCH (POWER1)
Size C
Document Number
Consumer AIO Woody
Rev SA
Date: Thursday, November 26, 2015
Sheet 21 of 107

PCH STRAP FUNCTIONS



SPI_SI_PCH (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_SO_PCH (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_WP_PCH (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_HOLD_PCH (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU



SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPI0_MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITP/XDP. The internal pull-down is disabled after PLTRST# deasserts.
PCH_PORT80_LED (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT SELECT STRAP 0: SPI select 1: LPC select The internal pull-down is disabled after PLTRST# deasserts.
GPP_C_5 (GPP_C5/SML0ALERT#)	ESPI/LPC SELECT STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disable after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistoris disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR

Need check
Though CRB use LPC to connect EC.
This pin doen't pull down

Follow ROSA / D7 trigerfish & Lily / M800 skylake project.

<Core Design>

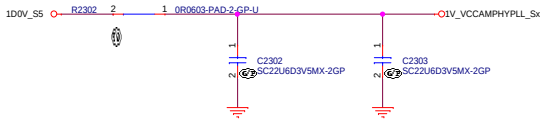
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

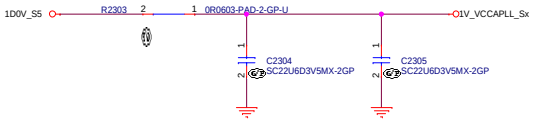
Title: PCH_(POWER2)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

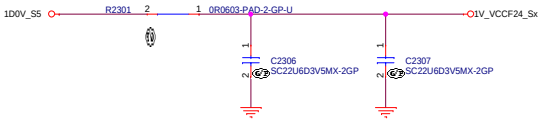
Date: Thursday, November 26, 2015 | Sheet 22 of 107



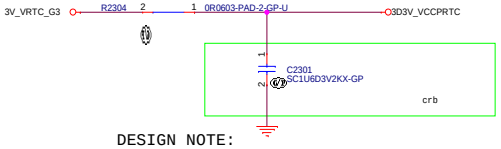
DESIGN NOTE:
PLACE HOLDER FOR VCCMPHYPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN A42,A43, AND B43



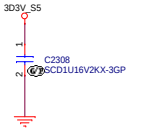
DESIGN NOTE:
PLACE HOLDER FOR VCCAUSB_1P0 AND VCCAAZPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN AJ5,AL5, AND AN19



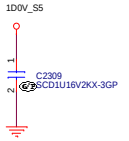
DESIGN NOTE:
PLACE HOLDER FOR VCCF24_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN K2 AND K3



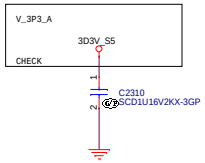
DESIGN NOTE:
BOARD CAP FOR VCCPRTC_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA22



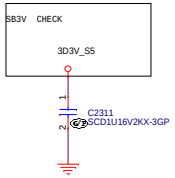
DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AJ41 AND AL41



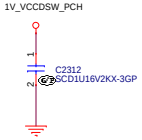
DESIGN NOTE:
BOAED CAP FOR VCCMPHY_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26



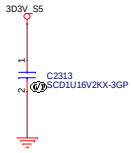
DESIGN NOTE:
EDGE CAP FOR VCCPUSBDSW_3P3
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
 PIN W15



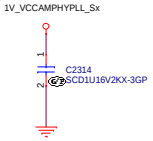
DESIGN NOTE:
BOAED CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA20



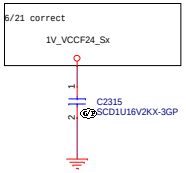
DESIGN NOTE:
BOAED CAP FOR VCCDSW_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA29



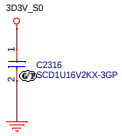
DESIGN NOTE:
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AD41



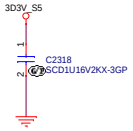
DESIGN NOTE:
BOAED CAP FOR VCCMPHYPLL_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN A42,A43 AND B43



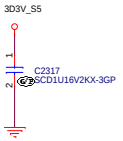
DESIGN NOTE:
BOAED CAP FOR VCCF24_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN K2,K3



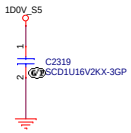
DESIGN NOTE:
BOAED CAP FOR VCCATS
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AD13



DESIGN NOTE:
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BC42 AND BD40



DESIGN NOTE:
BOAED CAP FOR VCCPHVC_3P3(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN15



DESIGN NOTE:
EDGE CAP FOR VCCMPHY_1P0 AND VCCDUSB_1P0
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26,AND AC17

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH Power CAP

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 23 of 107

AMP

LPC

Power Manager

CLOCK

SMBUS

PECI

OTHERS

COM Port

HW Monitor

VRD

PCH

REMINE LAYOUT

Reset signals

For AC OFF SEQUENCE

ECIO SPI ROM

Chassis Intrusion

IT8731 Power On Strapping Options

Symbol	value	Description
JP6	1	Disabled SVID Output pin
Pin 29	AMD SVID_EN	0 Enable SVID(Pin3)/SVC(Pin31) output pins
JP4	1	K8 power sequence function is disabled
Pin 124	K8PWR_EN	0 K8 power sequence function is enabled
JP3	1	The default value of EC Index 15h/16h/1Th is 80h
Pin 124	FAN_CTL_SEL	0 The default value of EC Index 15h/16h/1Th is 00h(Fan full speed)

PECI follow design guide--Kai 0319

SM Bus PH
SMB_DATA/CLK

For Power monitor function

Note
VREF follow Moussy

Mount R7978--Kai 0313

For OSD communication

AMP_PDN# from GP36 to GP17--Kai 0516

Note
From PCH SMB Link1

Case Open Detection

For EC domain, reset after power up

LPC I/F

Reserved EUP_DSW_SEL
JP1=1 EUP
JP1=0 DSW
--Kai 0315
Add pull down--Kai 0319

LPC groups need ex pull high--Kai 0319
RN7909 change to 3D3V_S0--Kai 0328

Add RN7911--Kai 0508

Delete SIO_PANEL_ON/OFF pull high--Kai 0514

To SB 3/5 EUP control

PWRBT Signal

HDMI IN DET

Connect High
Normal Low

Connect Low
Normal High

Power Good 3V

0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms

2012/12/12
1A change

20130910 Ryan

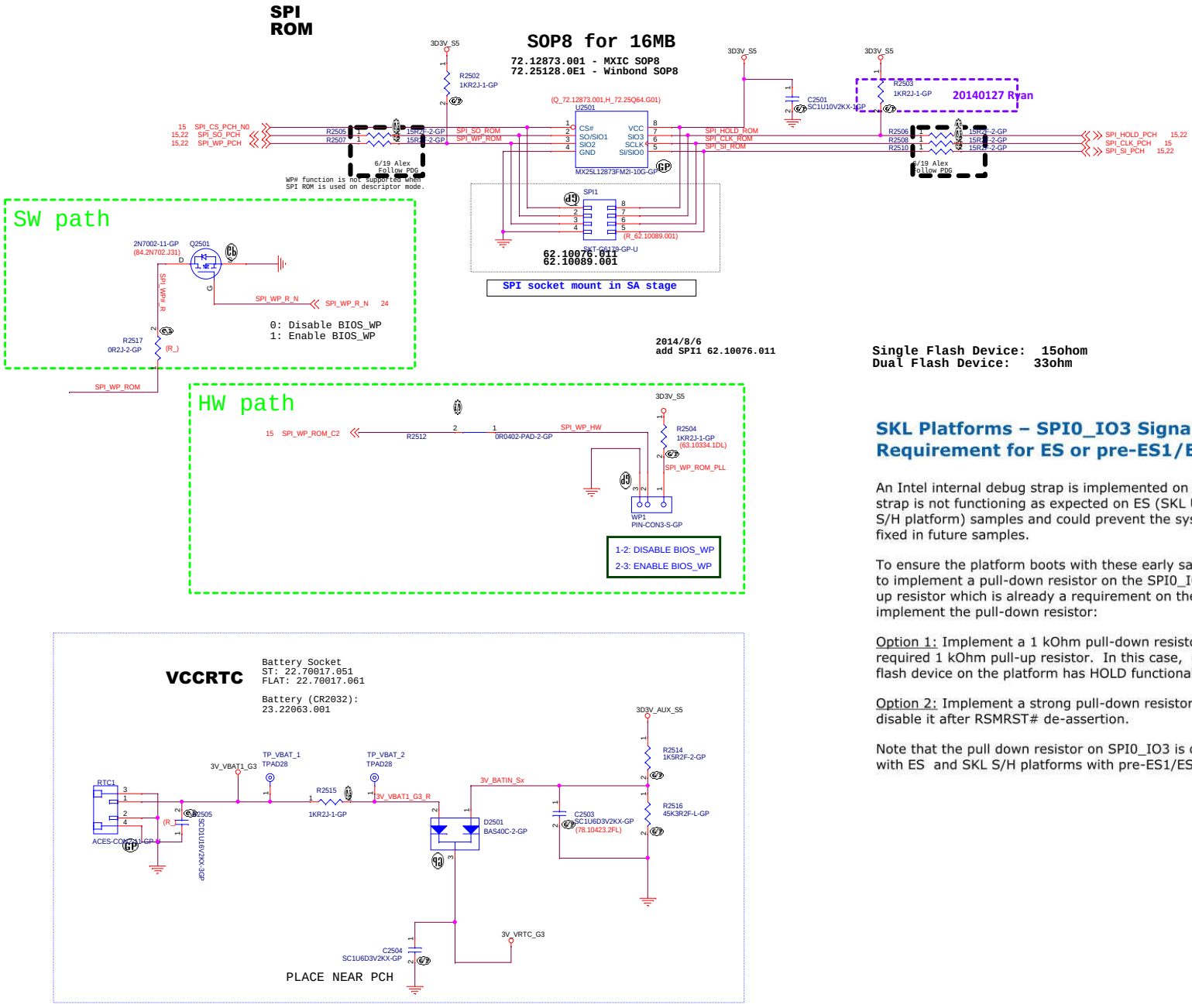
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: SIO ITE8732F-CX

Size: C | Document Number: Consumer AIO Woody | Rev: 0A

Date: Thursday, November 29, 2012 | Sheet 24 of 100



SKL Platforms – SPI0_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples

An Intel internal debug strap is implemented on the SPI0_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-ES1/ES1 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0_IO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

<Core Design>

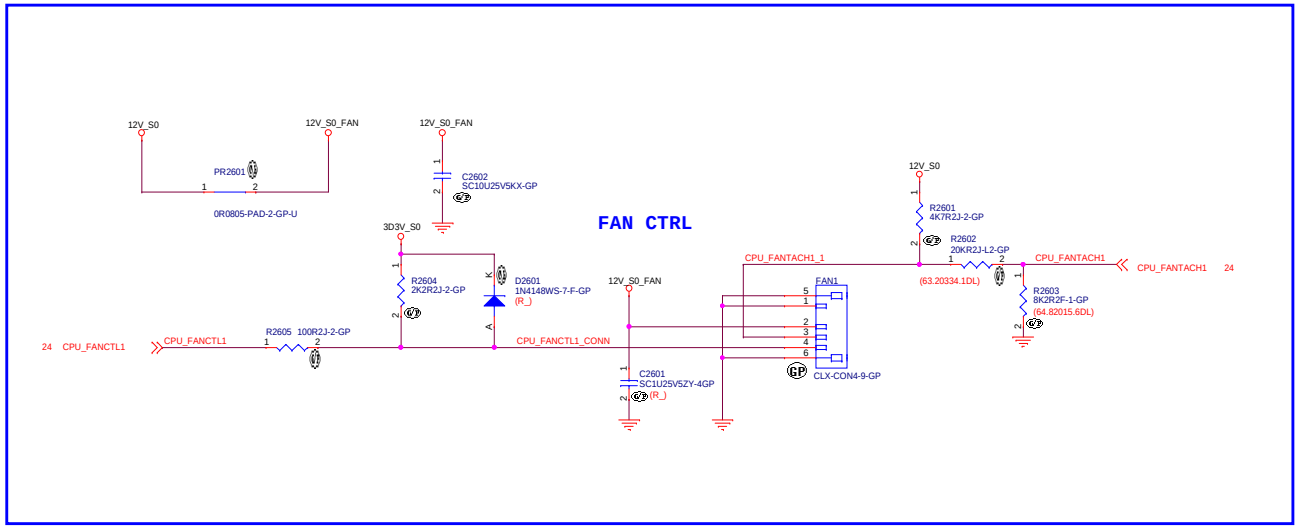
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Flash&RTC

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 25 of 107



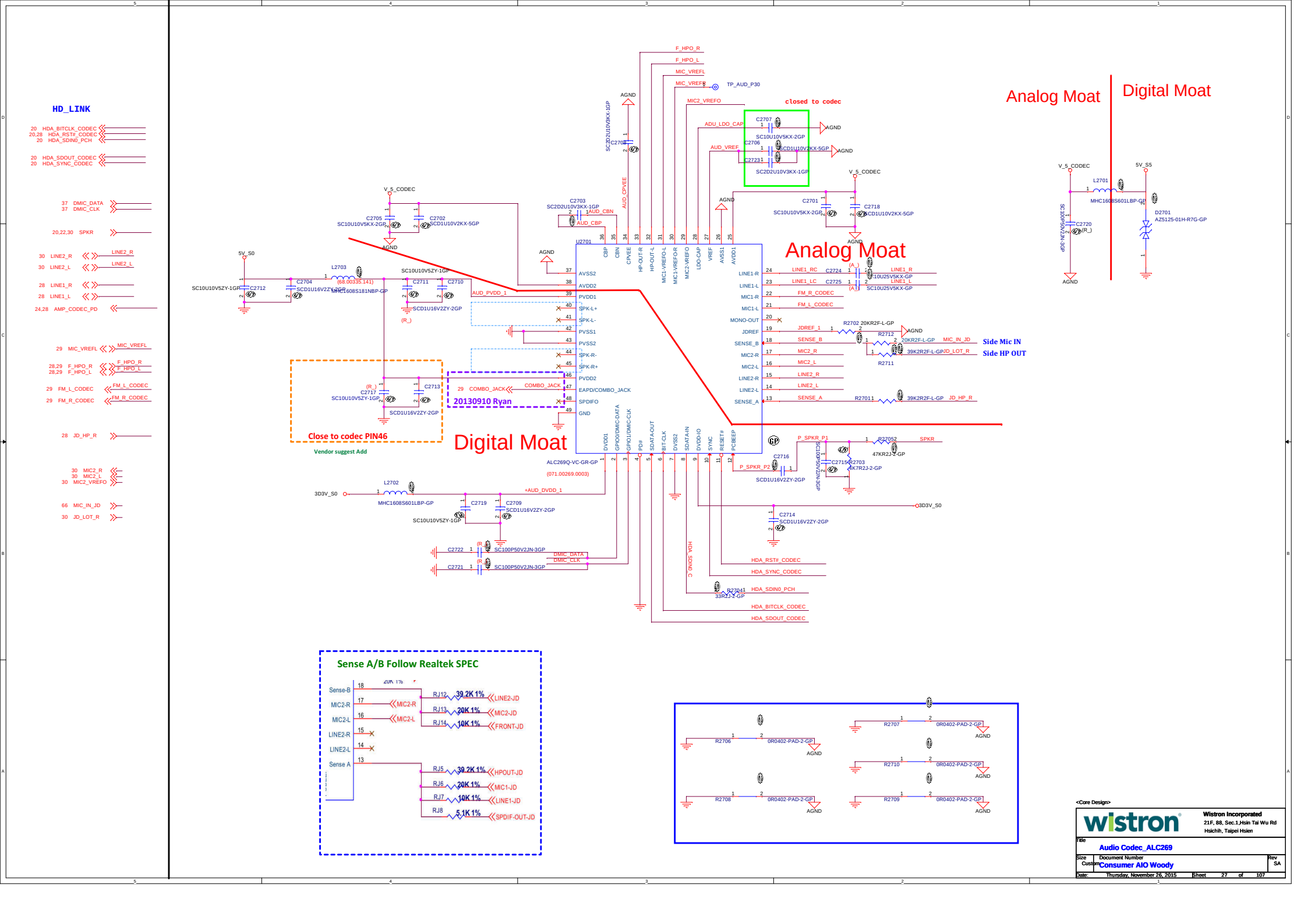
<Core Design>

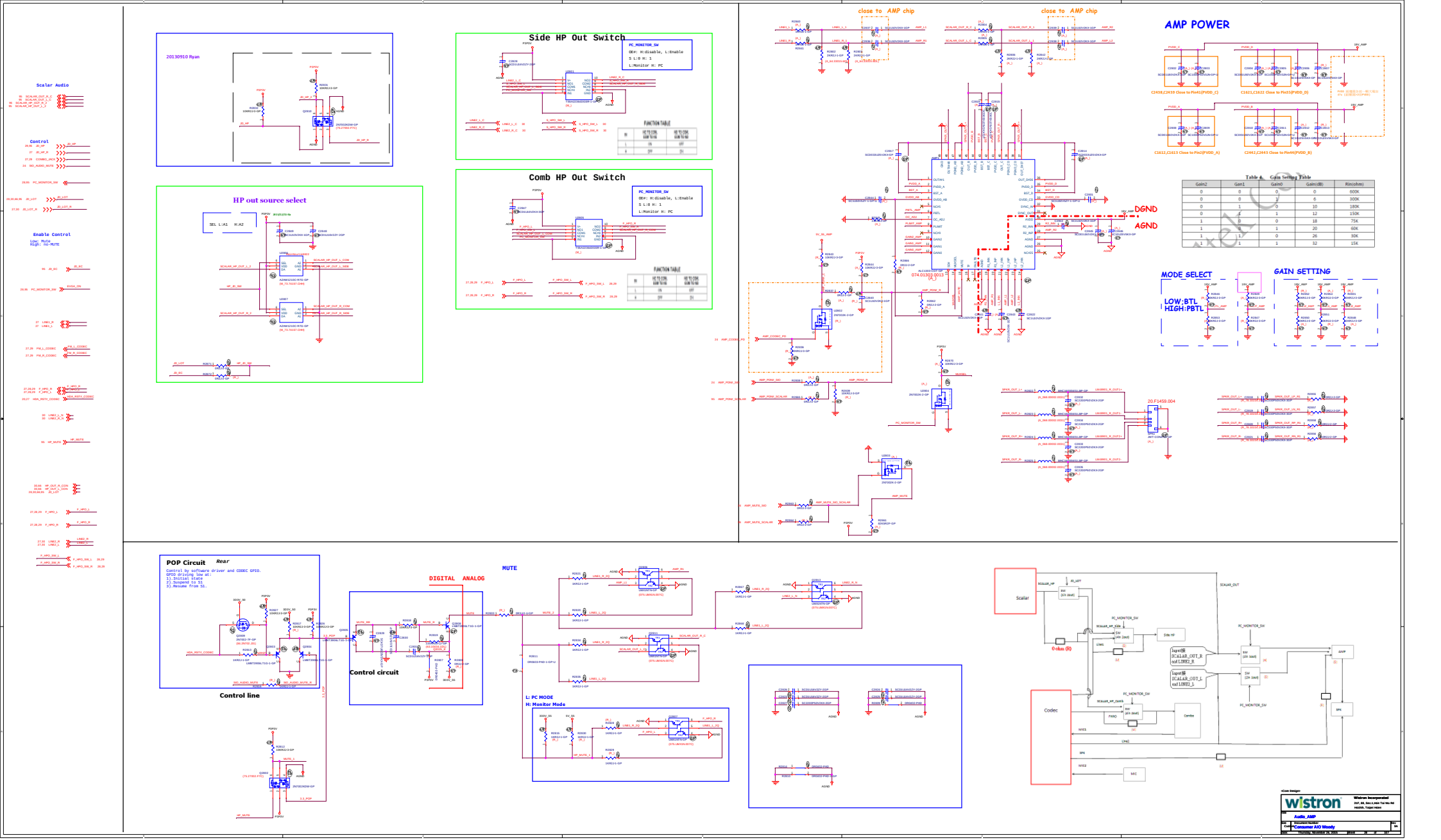
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thermal & FAN

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 26 of 107


HD_LINK
20 HDA_BITCLK_CODEC
20,28 HDA_RST#_CODEC
20 HDA_SDIN0_PCH
20 HDA_SDOUT_CODEC
20 HDA_SYNC_CODEC
37 DMIC_DATA
37 DMIC_CLK
20,22,30 SPKR
30 LINE2_R
30 LINE2_L
28 LINE1_R
28 LINE1_L
24,28 AMP_CODEC_PD
29 MIC_VREFL
28,29 F_HPO_R
28,29 F_HPO_L
29 FM_L_CODEC
29 FM_R_CODEC
28 JD_HP_R
30 MIC2_R
30 MIC2_L
30 MIC2_VREFO
66 MIC_IN_JD
30 JD_LOT_R
Analog Moat
Digital Moat
closed to codec
Close to codec PIN46
Vendor suggest Add
20130910 Ryan
Side Mic IN
Side HP OUT
Sense A/B Follow Realtek SPEC
RJ12 39.2K 1% LINE2-JD
RJ13 20K 1% MIC2-JD
RJ14 10K 1% FRONT-JD
RJ5 39.2K 1% HPOUT-JD
RJ6 20K 1% MIC1-JD
RJ7 10K 1% LINE1-JD
RJ8 5.1K 1% SPDIF-OUT-JD
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Audio Codec_ALC269
Consumer AIO Woody
Thursday, November 26, 2015


20130910 Ryan
Side HP Out Switch
PC_MONITOR_SW
OEM: H:disable, L:Enable
S L:0 H: 1
L:Monitor H: PC
Comb HP Out Switch
PC_MONITOR_SW
OEM: H:disable, L:Enable
S L:0 H: 1
L:Monitor H: PC
HP out source select
SEL L:A1 H:A2
close to AMP chip
close to AMP chip
AMP POWER
C2458,C2459 Close to Pin41(PVDD_C)
C1621,C1622 Close to Pin35(PVDD_D)
C1612,C1615 Close to Pin2(PVDD_A)
C2442,C2443 Close to Pin44(PVDD_B)
Table 4. Gain Setting Table
Gain2 Gain1 Gain0 Gain(dB) Rin(ohm)
0 0 0 0 600K
0 0 1 6 300K
0 1 0 10 180K
0 1 1 12 150K
1 0 0 18 75K
1 0 1 20 60K
1 1 0 26 30K
1 1 1 32 15K
DGND
AGND
MODE SELECT
LOW:BTL
HIGH:PBTL
GAIN SETTING
Scalar Audio
Control
Enable Control
Low: Mute
High: no-MUTE
POP Circuit
Rear
Control line
Control circuit
DIGITAL
ANALOG
MUTE
L: PC MODE
H: Monitor Mode
Scalar
Codec
0 ohm (R)
Wistron Incorporated
Audio_AMP
Consumer AIO Woody

27 MIC_VREFL <<>> MIC_VREFL

27,29 FM_L_CODEC <<>> FM_L_CODEC
27,29 FM_R_CODEC <<>> FM_R_CODEC

27,29 FM_L_CODEC <<>> FM_L_CODEC
27,29 FM_R_CODEC <<>> FM_R_CODEC

27 COMBO_JACK <<>> COMBO_JACK

28 F_HPO_SW_R <<>> F_HPO_SW_R

28,29 F_HPO_SW_L <<>> F_HPO_SW_L

28,29 F_HPO_SW_L <<>> F_HPO_SW_L

28,95 JD_HP >>> JD_HP

27,28 F_HPO_L >> F_HPO_L

27,28 F_HPO_R >> F_HPO_R

Combo Jack HP/MIC

CODEC

MIC_VREFL
R2901 2K2R2J-2-GP
FM_L_CODEC C2901 SC2D2U10V3KX-1GP
FM_R_CODEC C2903 MIC1 SC2D2U10V3KX-1GP
R2902 1KR2J-1-GP
MIC1_JACKL
L2901 FCM1608KFG-301T05-GP (68.00335.091)
MIC_IN_JACK
R2903 22KR2J-GP
C2902 SC100P50V2JN-3GP (78.10224.2FL)
AGND
AGND
COMBO_JACK
R2906 22KR2J-GP
C2906 SC10U10V5KX-2GP
AGND

F_HPO_SW_R
R2904 75R2J-1-GP
F_HPO_R_CL
L2902 FCM1608KFG-301T05-GP (63.00000.00L)
F_HPO_R_C
F_HPO_SW_L
R2905 75R2J-1-GP
F_HPO_L_CL
L2903 FCM1608KFG-301T05-GP (63.00000.00L)
F_HPO_L_C
JD_HP
C2904 (78.10224.2FL) SC100P50V2JN-3GP
C2905 (78.10224.2FL) SC100P50V2JN-3GP
AGND

AUDR1
NP2
NP1
AUDIO-JK540-GP

F_HPO_L
R2907 0R2J-2-GP (U_)
F_HPO_SW_L
F_HPO_R
R2908 0R2J-2-GP (U_)
F_HPO_SW_R

20130910 Ryan

ESD

MIC_IN_JACK
JD_HP
D2901 AZ5125-02S-R7G (R_)
F_HPO_R_C
F_HPO_L_C
D2902 AZ5125-02S-R7G (R_)

<Core Design>

wistron

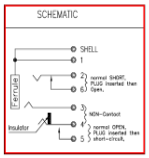
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

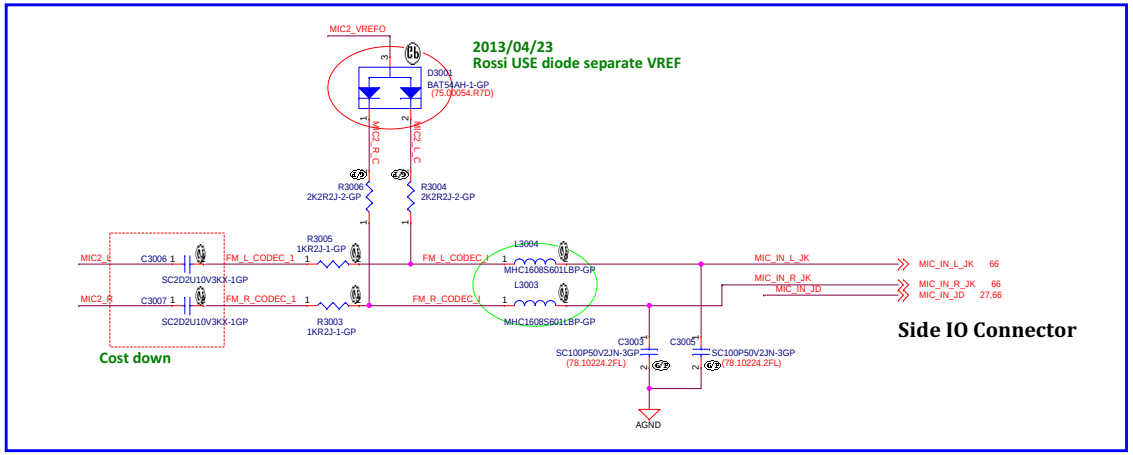
Title: Audio IO_Combo HP_MIC

Size: C | Document Number: Consumer AIO Woody | Rev: SA

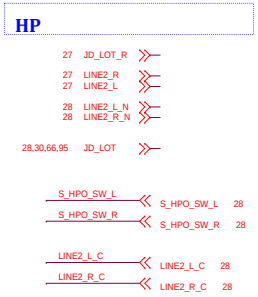
Date: Thursday, November 26, 2015 | Sheet 29 of 107

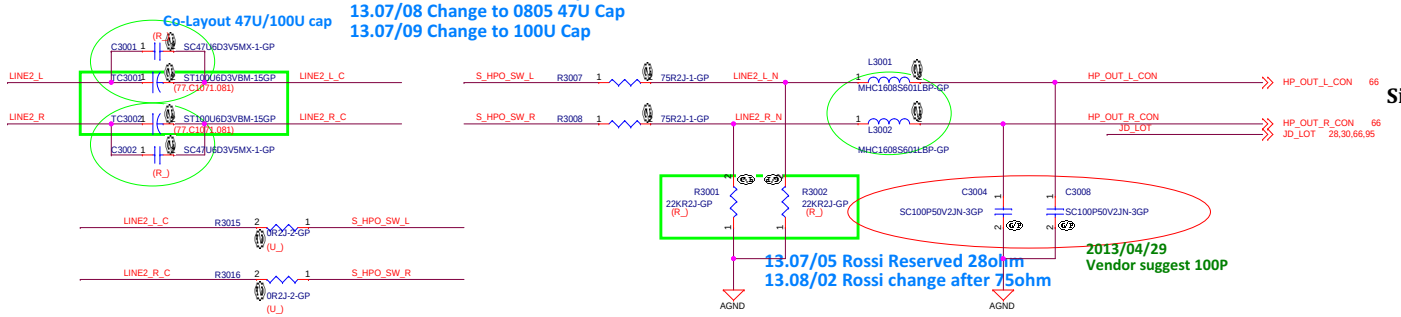
MIC

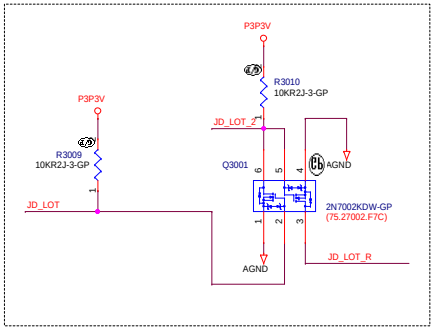


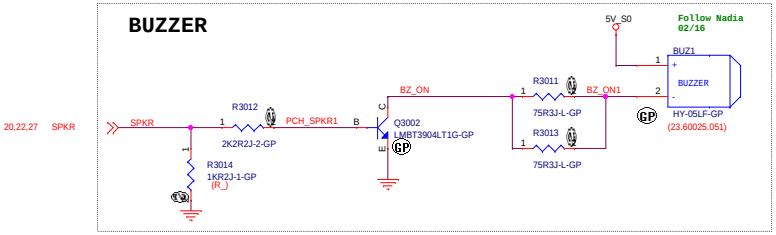


HP









<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: Audio IO_Side		
Size: C	Document Number: Consumer AIO Woody	Rev: SA
Date: Thursday, November 26, 2015	Sheet 30 of 107	

MDI

32,97 LAN_MDI_LAN_P0
32,97 LAN_MDI_LAN_N0
32,97 LAN_MDI_LAN_P1
32,97 LAN_MDI_LAN_N1
32,97 LAN_MDI_LAN_P2
32,97 LAN_MDI_LAN_N2
32,97 LAN_MDI_LAN_P3
32,97 LAN_MDI_LAN_N3

PCIE

18,97 PEG_CLK2_LAN
18,97 PEG_CLK2_LAN#
16,97 PCIE_TX_LAN_P5
16,97 PCIE_TX_LAN_N5
16,97 PCIE_RX_LAN_P5
16,97 PCIE_RX_LAN_N5

OTHERS

24 PLTRST_LAN
24,97 LANWAKE_N
18,97 PEG_CLKREQ2_LAN#

LAN LED

32,97 LAN_SPEED1000_LAN_N
32,97 LAN_SPEED100_LAN_N
32,66,97 LAN_LINKACTIVITY_LAN_N

SMBUS

20,62 SMB_CLK_RESUME
20,62 SMB_DATA_RESUME
20 SML1CLK_PCH
20 SML1DATA_PCH
24 SMB_CLK_LAN
24 SMB_DATA_LAN

10Mb: Green
100Mb: Green
1Gb: Orange
Active: Green Light flash

2015/1/14-SB Vita
del TP771,TP772,TP770,TP727,R275 for layout TP setting

2014/8/27-SA Vita
vendor suggestion mount R227 1K

2014/8/1-SA Vita
add R236(R) for 8111EP

2012/09/19
SPISK SPISI EECS
reserved connecot to EEPROM

2015/1/16-SB Vita
Change X3 to 82.30020.G71
Add R3138 470ohm for crystal
use F7 as (B_78.18034.1FL) for C238,C239

82.30020.G71
25MHZ X'tal with CL=12PF

2013/03/06
connect to PCH side SMBus
P/H EUP PWR instead of normal PWR

2014/8/1-SA Vita
connect to chipset SMBus

2014/8/1-SA Vita
mount R233 and unmount R235 for 8111EP

2011/06/23
LAN IC: 71.08111.K03 vBremen (support ASF)
71.08111.J03 aBremen (non support ASF)

2012/09/24
Change XTAL to SMT

2014/12/31-SB Vita
add dual MOS architecture to avoid LAN SMBus leakage

2014/8/1-SA Vita
mount R249 and unmount R247 for 8111EP

2014/8/1-SA Vita
mount R251 and unmount R250 for 8111EP

2014/8/1-SA Vita
mount R252 for 8111EP

4Mb ROM

72.25406.001

2014/12/18-SB Vita
Change L7 symbol to 068.4R710.1281

Close To U3201 Pin 3, 6, 9, 13, 29, 41, 45.

Close To U3201 Pin 21.

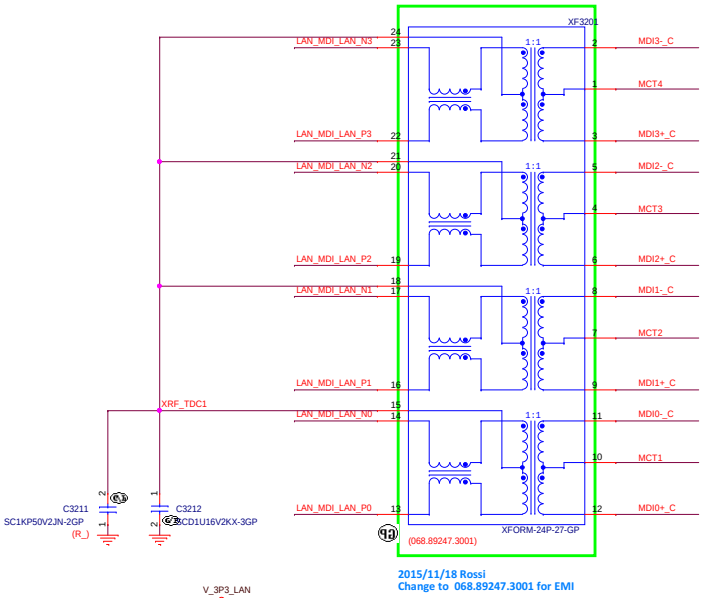
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

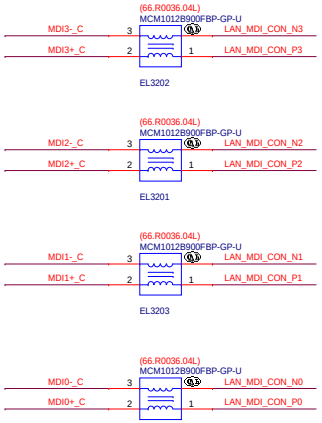
Title: RTL8111EPV
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA
Date: Thursday, November 26, 2015 | Sheet 31 of 107

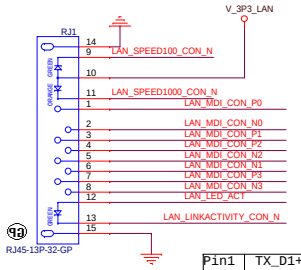
LAN

31,97 LAN_MDI_LAN_P0
31,97 LAN_MDI_LAN_N0
31,97 LAN_MDI_LAN_P1
31,97 LAN_MDI_LAN_N1
31,97 LAN_MDI_LAN_P2
31,97 LAN_MDI_LAN_N2
31,97 LAN_MDI_LAN_P3
31,97 LAN_MDI_LAN_N3
31,97 LAN_SPEED1000_LAN_N
31,97 LAN_SPEED100_LAN_N
31,66,97 LAN_LINKACTIVITY_LAN_N

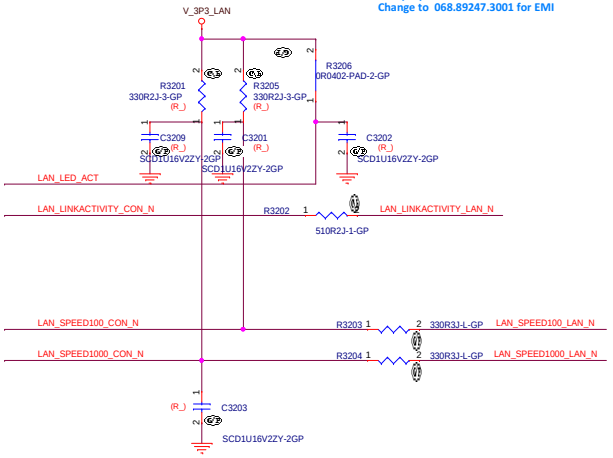


2015/11/18 Rossi
Change to 068.89247.3001 for EMI

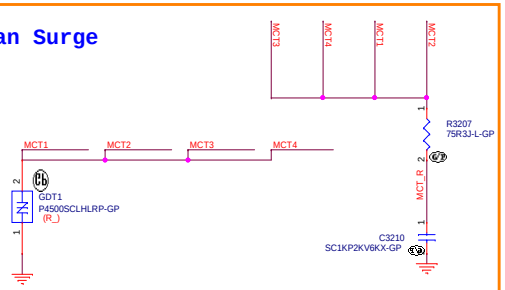




Pin1	TX_D1+	
Pin2	TX_D1-	
Pin3	RX_D2+	
Pin4	B1_D3+	
Pin5	B1_D3-	
Pin6	RX_D2-	
Pin7	B1_D4+	
Pin8	B1_D4-	
Pin10 +	Pin9 -	GREEN
Pin10 +	Pin11 -	ORANGE
Pin12 +	Pin13 -	Green



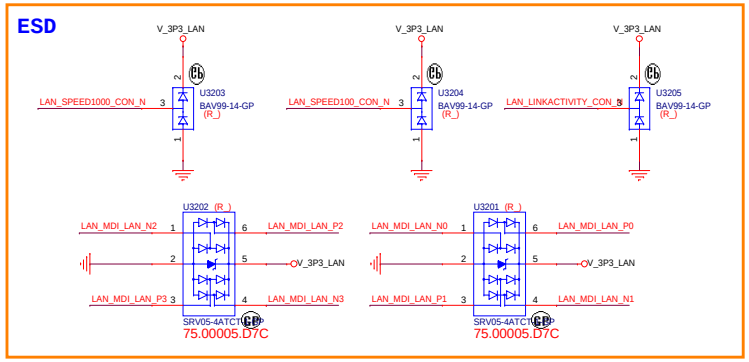
Lan Surge

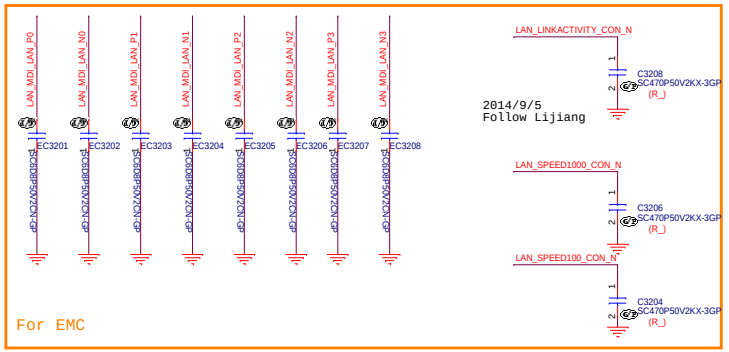


PCB

	Link	Act
	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

ESD





<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: RJ45&Transformer

Size	Document Number	Rev
C	Consumer AIO Woody	SA

Date: Thursday, November 26, 2015 Sheet 32 of 107

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

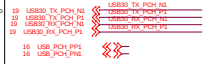
Title

Card reader_(R)

Size	Document Number	Rev
C	Consumer AIO Woody	SA

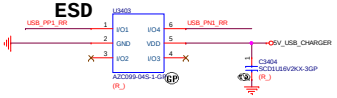
Date: Thursday, November 26, 2015 Sheet 33 of 107

USB3.0 SIDE CONNECTOR

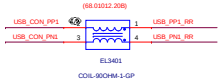


USB3.0's USB2 pair from PCH

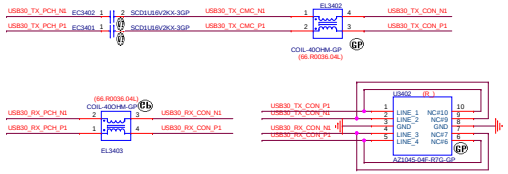
ESD



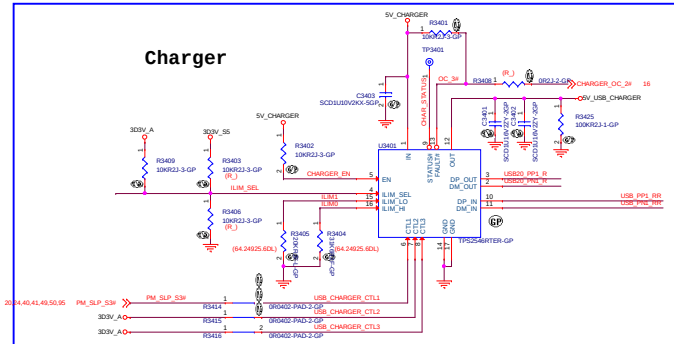
USB2.0 EMI



USB3.0 EMI



Charger



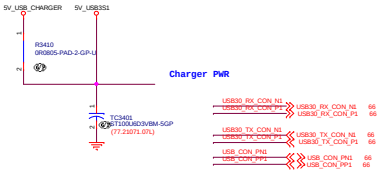
Truth Table for TPS2540A/TPS2543/TPS2546

ACPI Control	CTL1	CTL2	CTL3	ILIM_SEL	PWR	Control Mode
S0	1	1	1	1	+5V_MAIN	CDP
S1	1	1	1	1	+5V_MAIN	CDP
S3	0	1	1	1	ATX_5VSB	DCP
S4	0	1	1	1	ATX_5VSB	DCP
S5	0	1	1	1	ATX_5VSB	DCP
S5_EuP	0	1	1	1	ATX_5VSB	DCP
G3->S5	0	1	1	1	ATX_5VSB	DCP

Paid attantion to CTRL1 and CTRL3 GPIO pin selection

	CTRL1	CTRL2	CTRL3	ILIM_SEL
S0	High	High	High	High
S3	Low	High	High	High
S4	Low	High	High	High
S5	Low	High	High	High

Side IO BD



USB 3.0 Connector Pin definition	
1	*POWER*
2	*USB 2.0 D-*
3	*USB 2.0 D+*
4	*GND*
5	*StdA_SSRX- SuperSpeed RX*
6	*StdA_SSRX+*
7	*GND*
8	*StdA_SSTX- SuperSpeed TX*
9	*StdA_SSTX+*

<Core Design>

Wistron Incorporated
21F, 88, Sec.1 Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB Charger_TPS2544

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 34 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

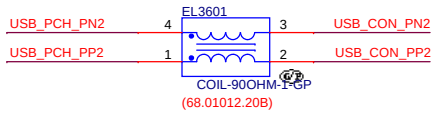
Title: USB_Redrive_(R)

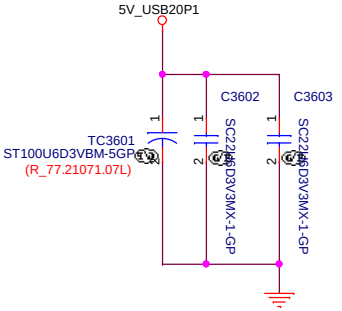
Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 35 of 107

16 USB_PCH_PN2
16 USB_PCH_PP2

USB2.0 EMI

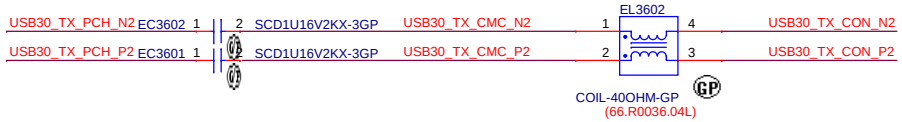


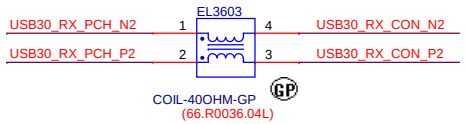


USB30_RX_CON_N2 → USB30_RX_CON_N2 38
USB30_RX_CON_P2 → USB30_RX_CON_P2 38
USB30_TX_CON_N2 → USB30_TX_CON_N2 38
USB30_TX_CON_P2 → USB30_TX_CON_P2 38
USB_CON_PN2 → USB_CON_PN2 38
USB_CON_PP2 → USB_CON_PP2 38

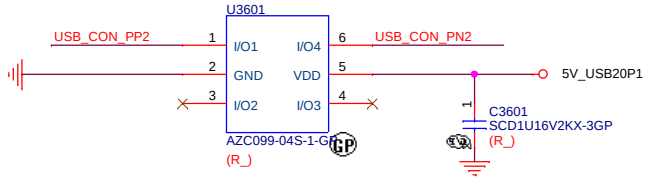
19 USB30_TX_PCH_N2
19 USB30_TX_PCH_P2
19 USB30_RX_PCH_N2
19 USB30_RX_PCH_P2

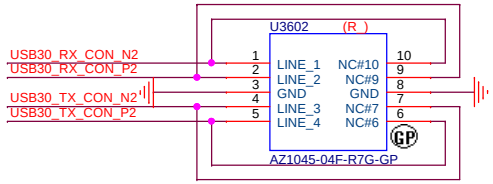
USB3.0 EMI





ESD





<Core Design>

wistron

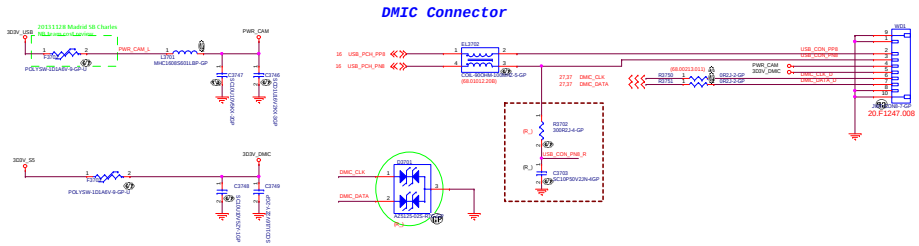
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB 30_REAR PORT

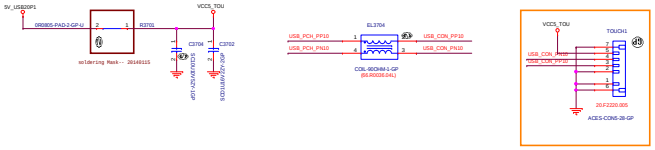
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 36 of 107

USB Port8 -> WEBCAM

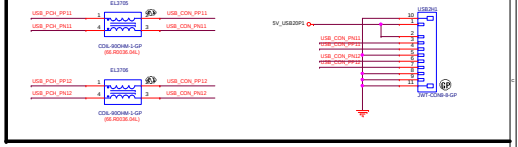


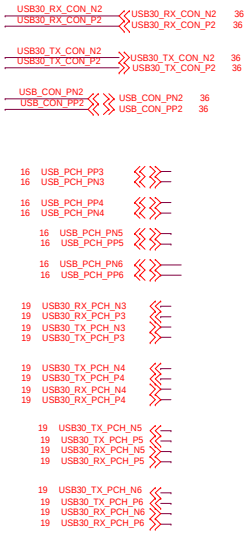
USB Port7 -> Touch



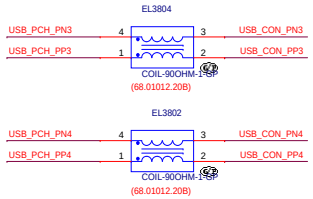
PCIE1->3D WEBCAM

09/06/2015 Add Internal USB connector
power use rear USB2.0 power

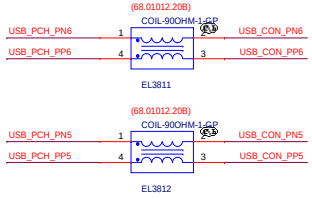




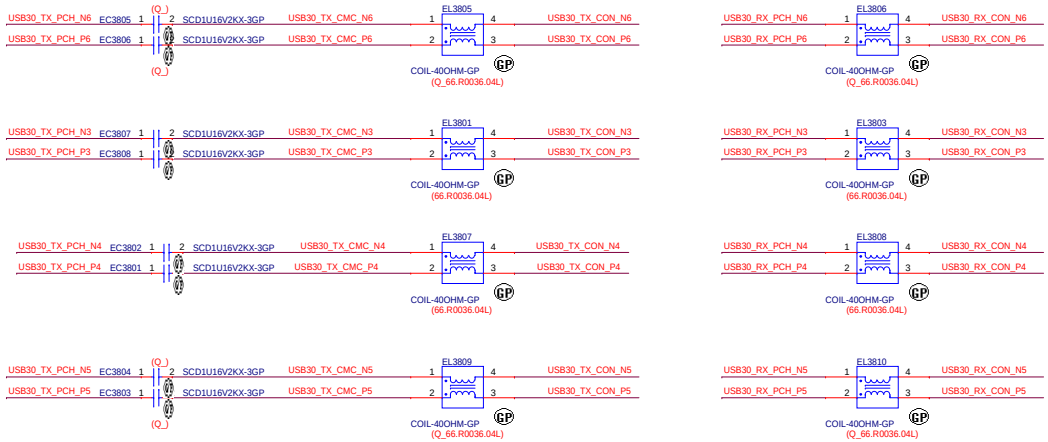
USB2.0 EMI



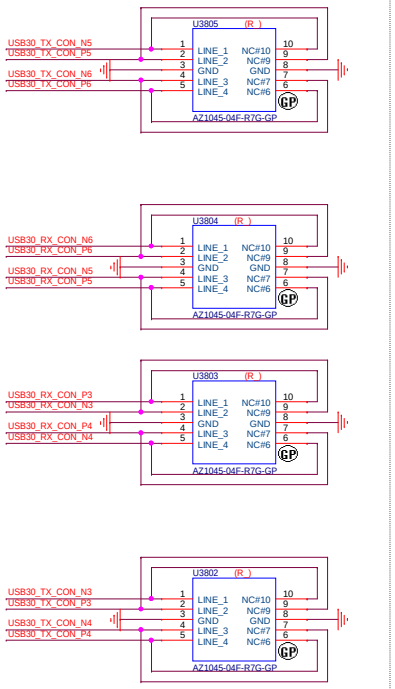
USB2.0 EMI



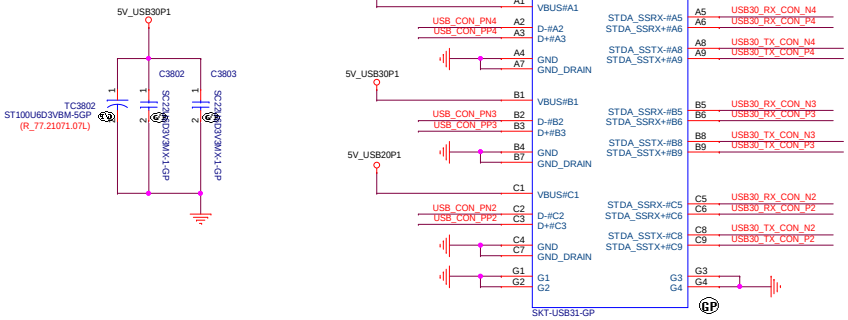
USB3.0 EMI



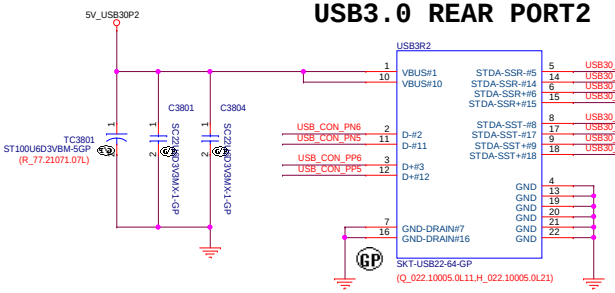
ESD



USB3.0 REAR PORT1

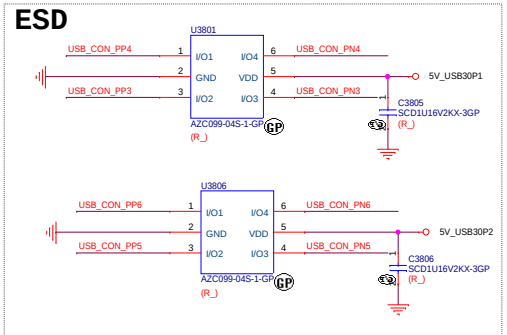


USB3.0 REAR PORT2



Q170:(USB 3.0*4)
H110:(USB3.0*2, USB2.0*2)

ESD



<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB30_REAR PORT

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 38 of 107

Reserved

<Core Design>

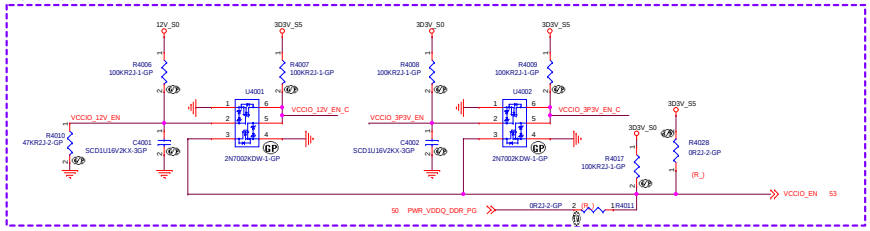
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB30_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 39 of 107

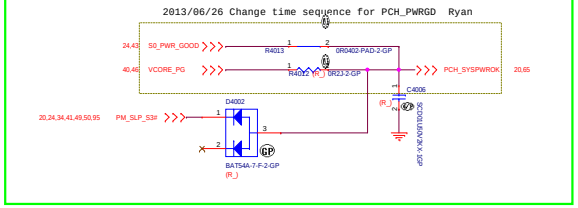
2014/9/23
VCCIO ENABLE
follow Yama D7



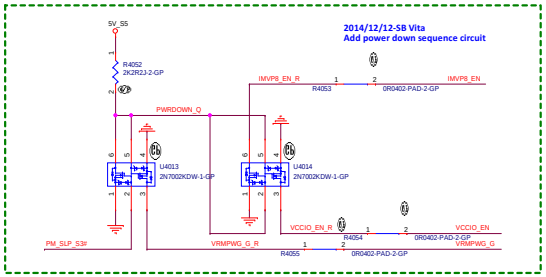
2014/8/7
follow Madrid

Power Sequence

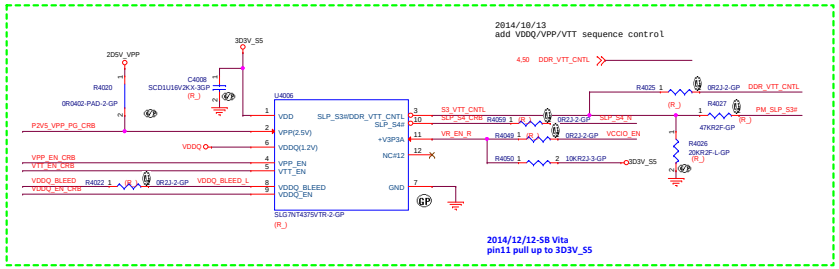
2013/06/26 Change time sequence for PCH_PWRGD Ryan



2014/12/12-SB Vita
Add power down sequence circuit



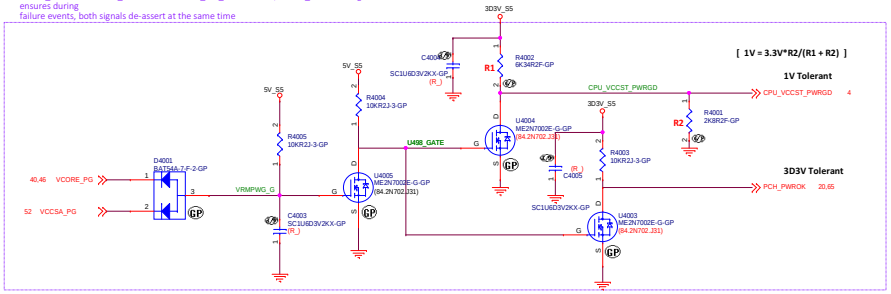
2014/10/13
add VDDQ/VPP/VTT sequence control

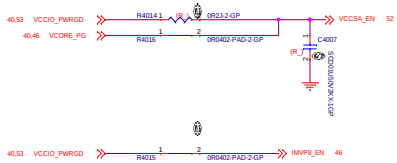


2014/12/12-SB Vita
pin11 pull up to 3D3V_S5

2014/8/7
Follow Veneno

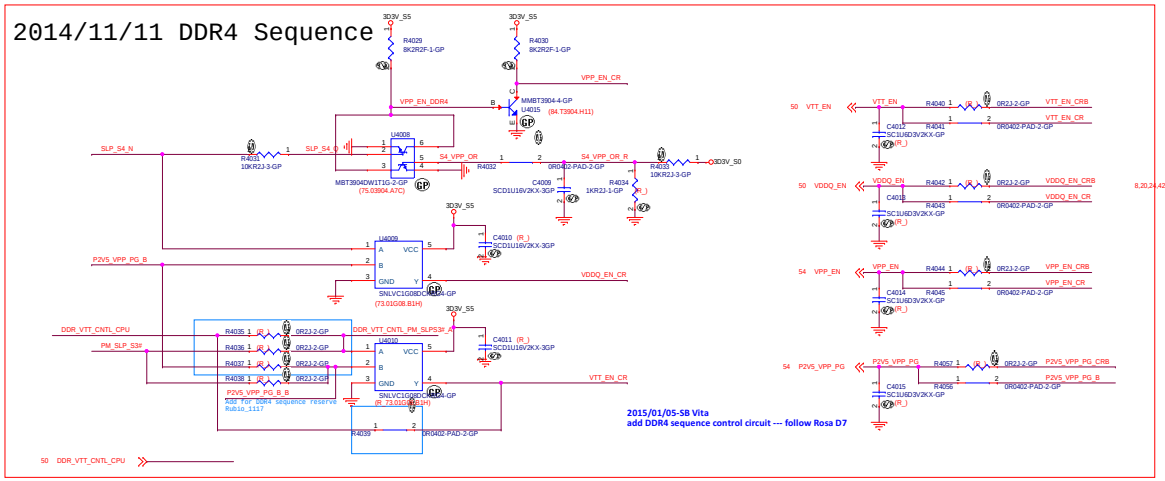
Note:
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both
VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during
failure events, both signals de-assert at the same time



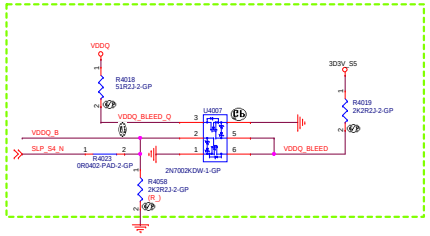


1> VCCIO -> VCORE -> VCCSA (current)
2> VCCIO -> VCORE/VCCSA both

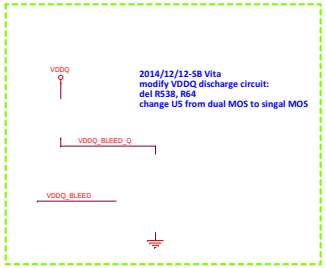
2014/11/11 DDR4 Sequence



2015/01/05-SB Vita
add DDR4 sequence control circuit --- follow Rosa D7



2015/01/07-SB Vita
change U2 F7 to (75.03904.A7C)



2014/12/12-SB Vita
modify VDDQ discharge circuit:
del R538, R64
change U5 from dual MOS to singal MOS

<Core Design>

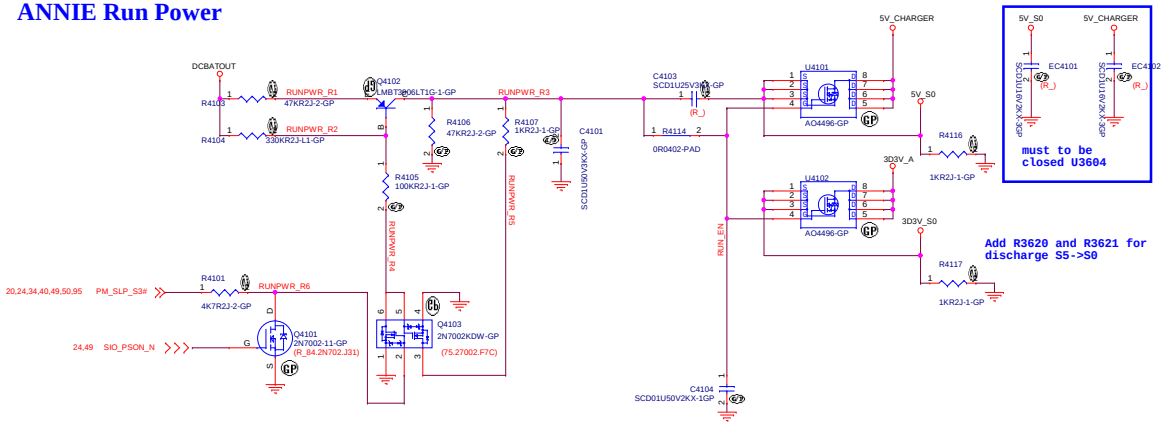
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Power Plane EN Sequence

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

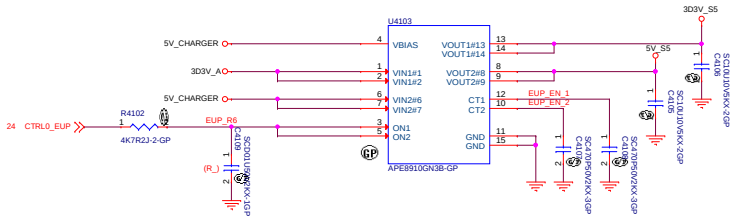
Date: Thursday, November 26, 2015 | Sheet 40 of 107

ANNIE Run Power



EUP Power

Modify 3V/5V Logic Control as Load Switch



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Switch power_DS3

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

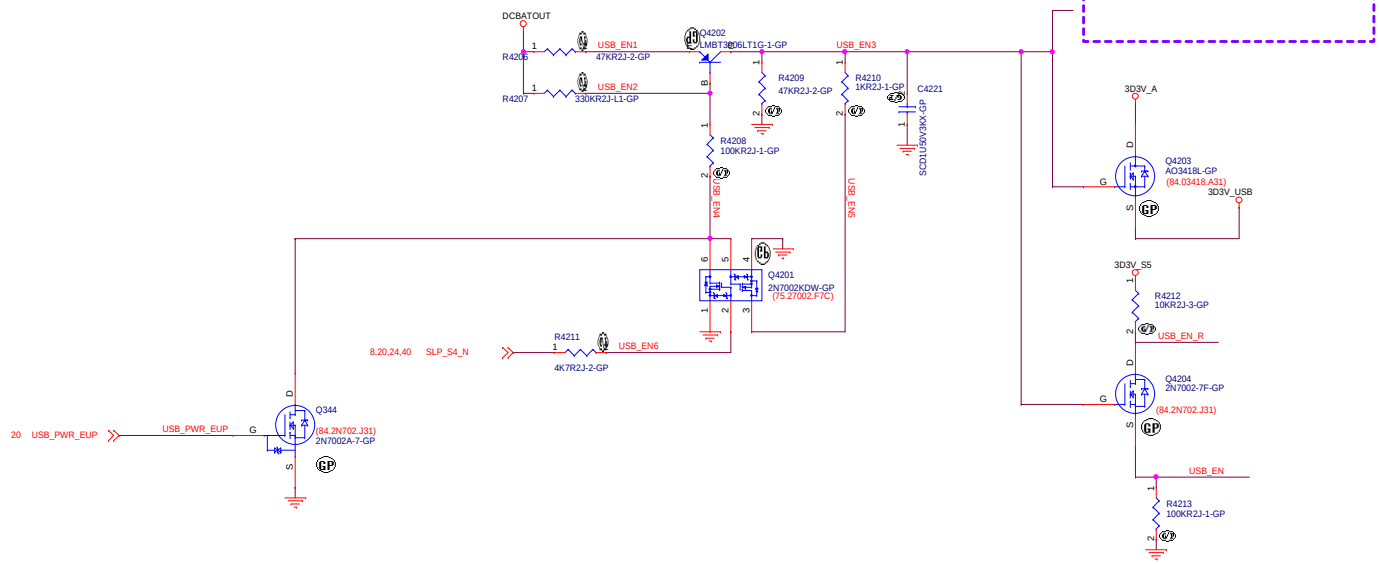
Date: Thursday, November 26, 2015 | Sheet 41 of 107

	S5	S4	S3-S0		S5	S4	S3-S0	Status
USB_PWR_SLP	L	L	L	USB_EN	L	L	H	No Support S4 USB wake up
USB_PWR_SLP	L	H	L	USB_EN	L	H	L	Support S4 USB wake up

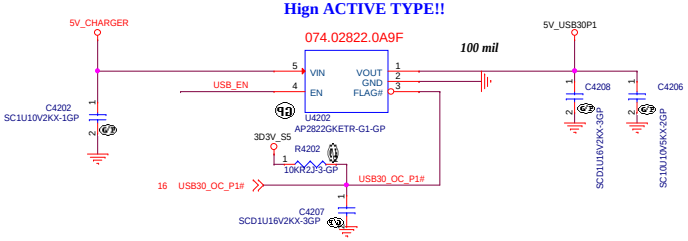
S4, S5 --> choice by USB_PWR_SLP
S3-S0 --> choice by SLP_S4#

VCC5_USB

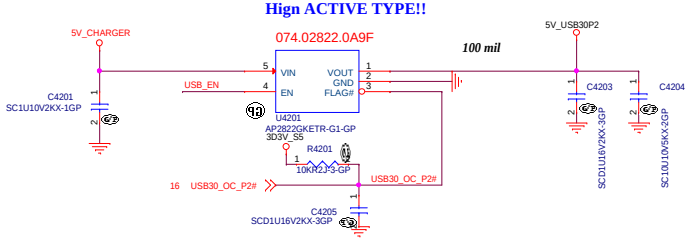
20130927 Ryan



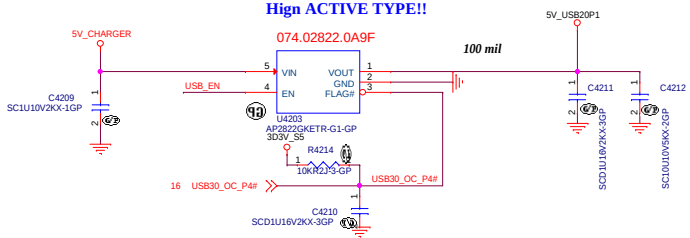
Hign ACTIVE TYPE!!



Hign ACTIVE TYPE!!



Hign ACTIVE TYPE!!

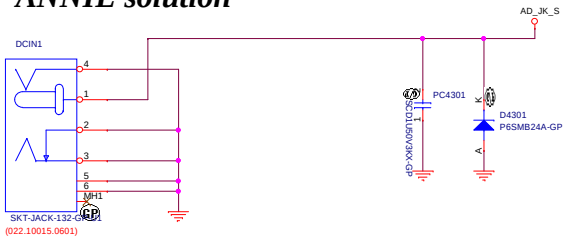


<Core Design>

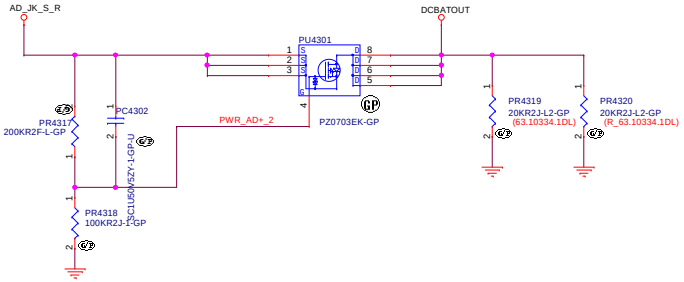
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Switch power
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 42 of 107

ANNIE solution



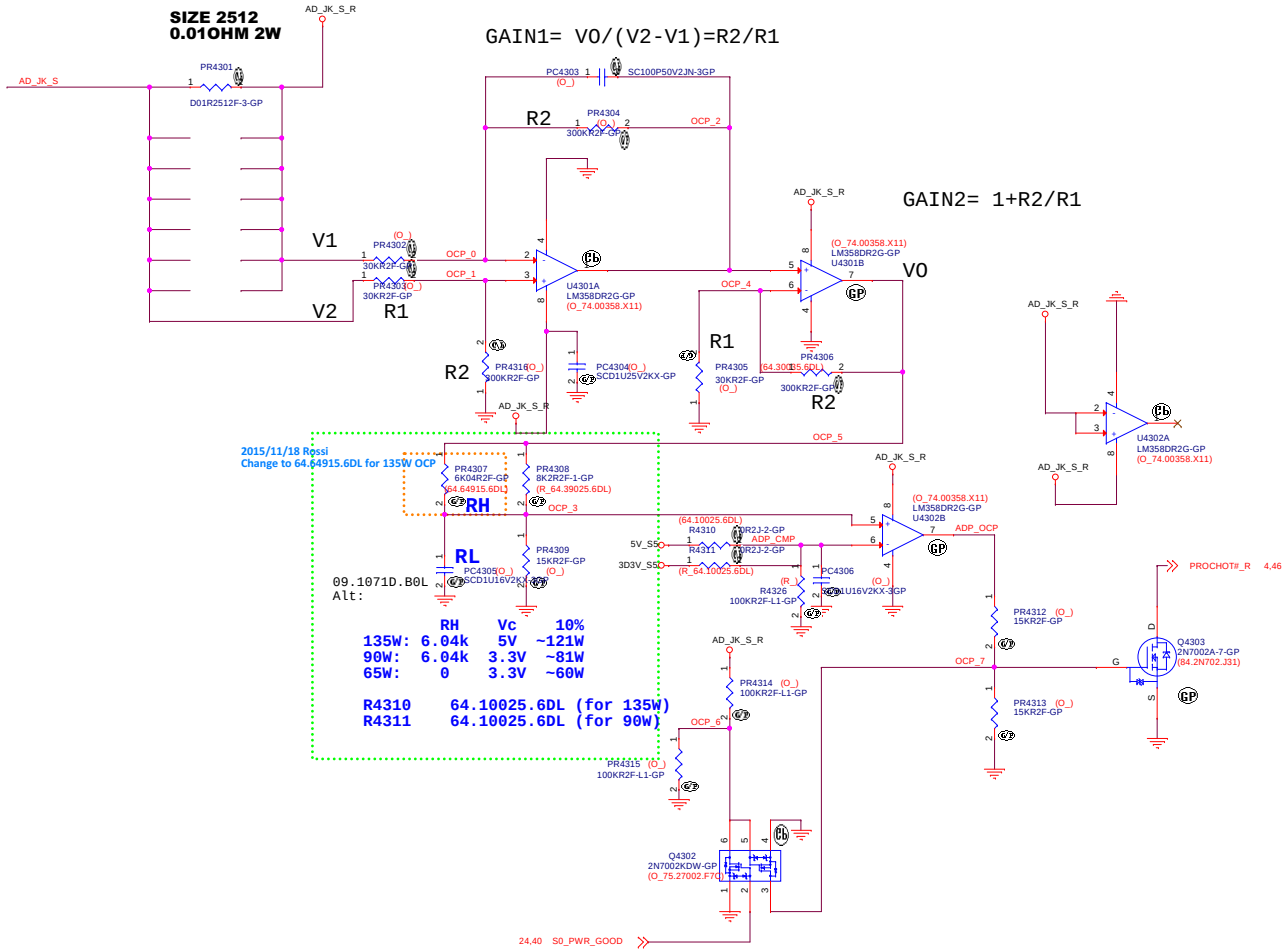
DCIN1 PN Change to 22.10037.A41



SIZE 2512
0.01OHM 2W

GAIN1= VO/(V2-V1)=R2/R1

GAIN2= 1+R2/R1



<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

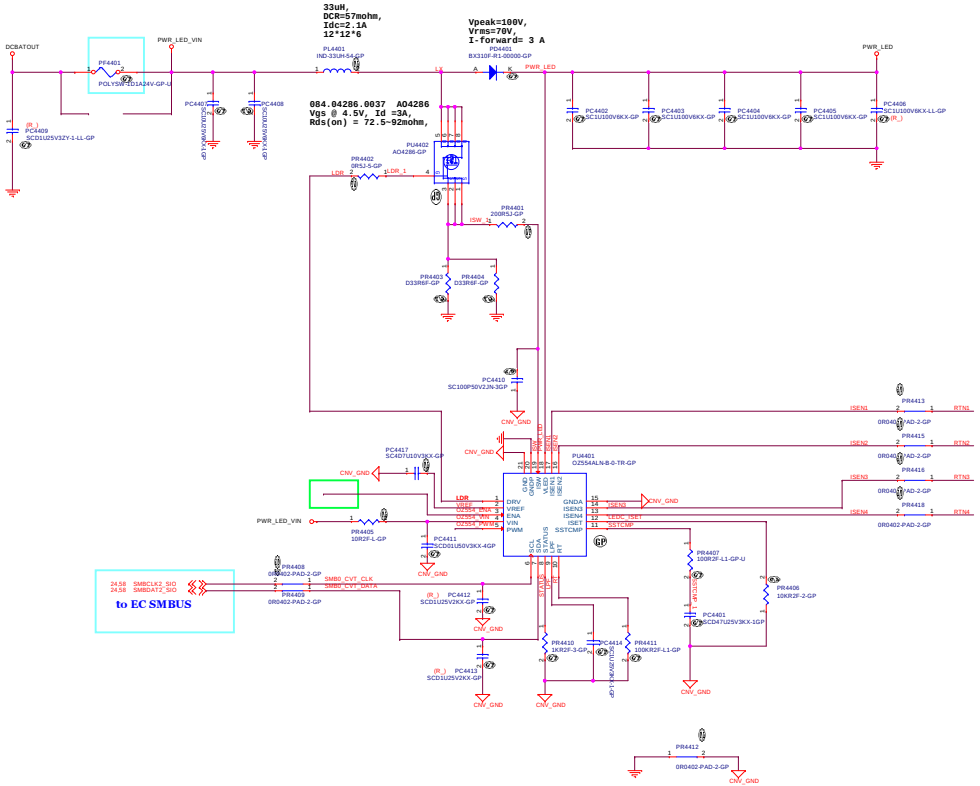
Title: DCIN JACK(BATT Conn)

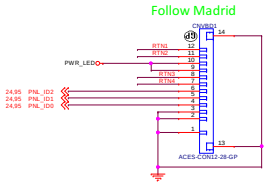
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 43 of 107

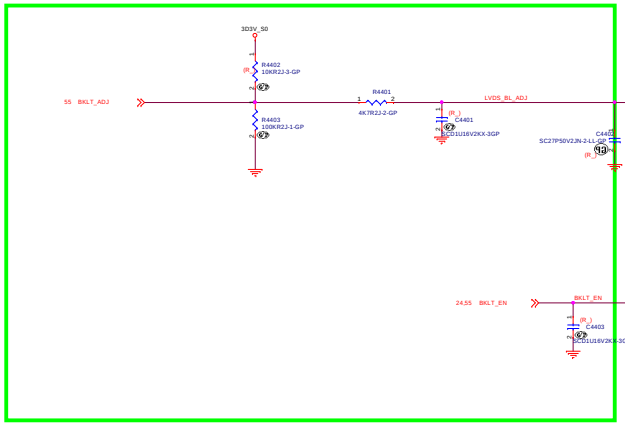
Converter Board

Cable detection			
PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Status
1	1	1	Panel unplug
X	X	X	Panel plug

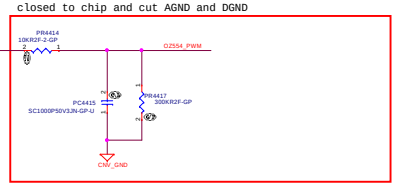


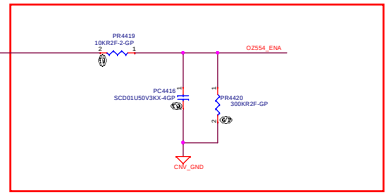


Need EE to check



closed to chip and cut AGND and DGND





Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
	0	0	0	
	0	0	1	
	0	1	0	
	1	0	0	
	1	1	0	
	1	1	1	

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: OZ554A LED Converter

Size: D | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 44 of 107

PWR_3D3V/PWR_5V

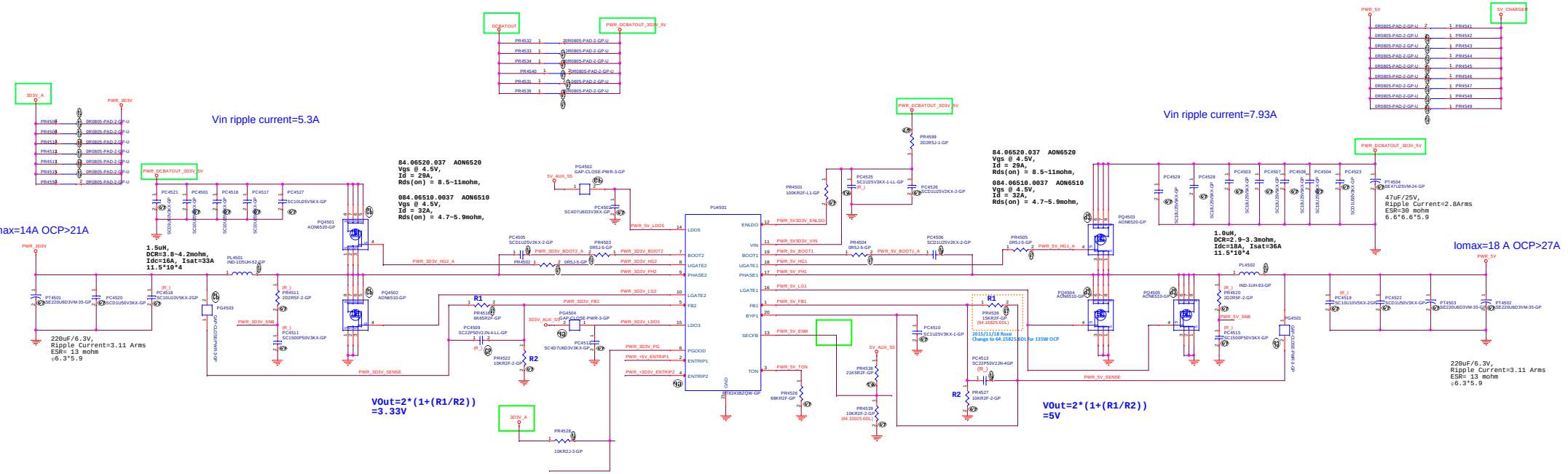


Table 2. Power Up Sequencing(RT8243A)							
ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

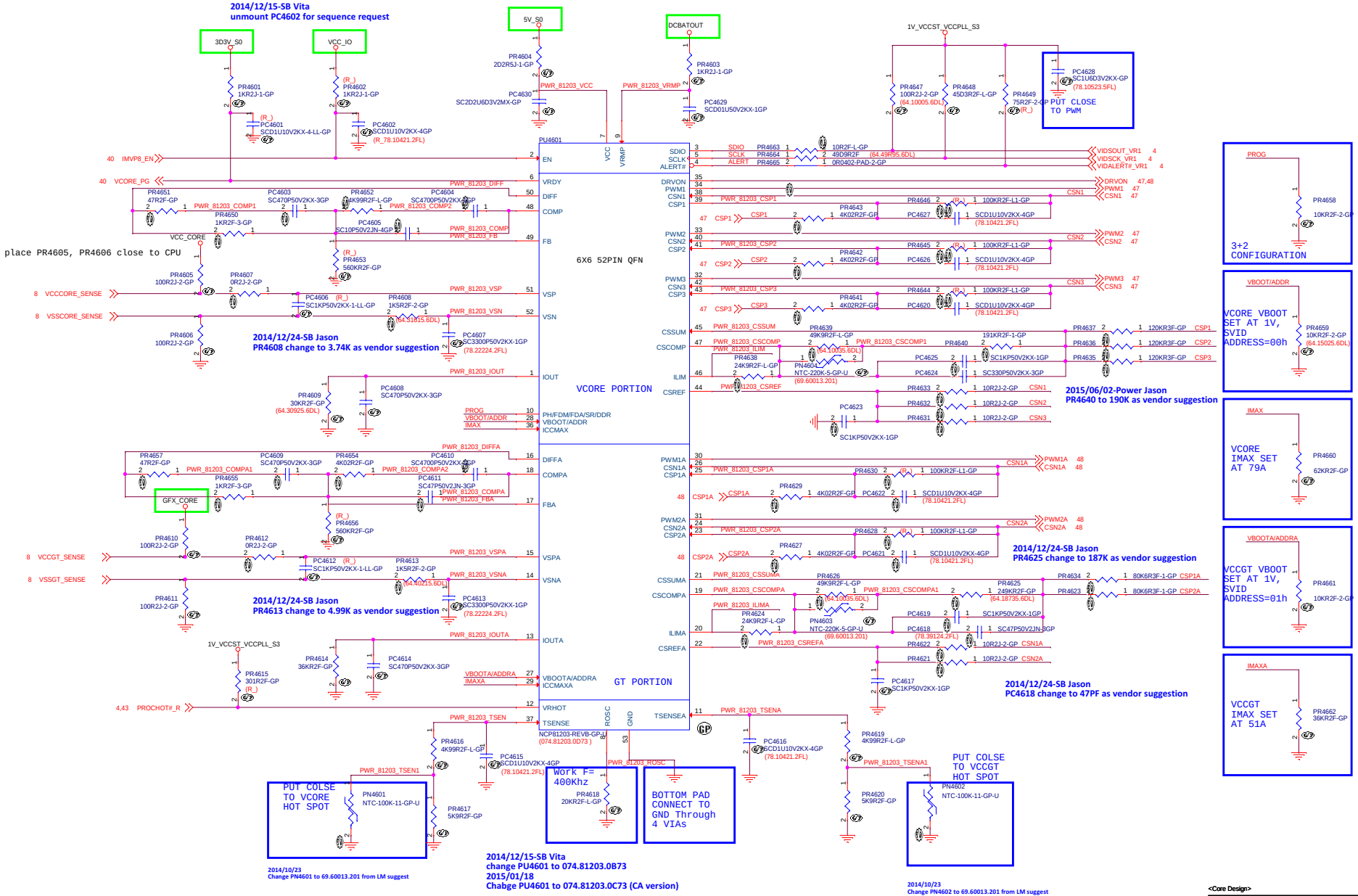
<Core Design>

wistron — Wistron Incorporated, 21F, 88, Sec.1,Hsin Tai Wu Rd, Hsichih, Taipei Hsien

Title	RT8243_5V/3D3V	
Size: Custom	Document Number: Consumer AIO Woody	Rev: 5A
Date: Tuesday, November 26, 2013	Sheet 45 of 107	

PWR_CORE/PWR_VCCGT

Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE 65Watt



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCORE & V_GT IC (NCP81203)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 46 of 107

PWR_CORE

84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

Vin ripple=7.9A

PWR_DCBATOUT_VCORE
DCBATOUT
PR4719 1 0R5J-5-GP (68.NC24.031)
PR4720 1 0R5J-5-GP (68.NC24.031)
PR4721 1 0R5J-5-GP (68.NC24.031)
PR4722 1 0R5J-5-GP (68.NC24.031)

PWR_81151_BST1R
PR4702 0R5J-5-GP
PC4703 SCD1U25V3KX-GP (78.10424.2BL)
PR4703 0R5J-5-GP
PWR_81151_H1R
PR4704 10KR2J-3-GP
PWR_81151_BST1
PWR_81151_DRVH1
PWR_81151_SW1
PWR_81151_DRVL1
PU4702 AON6552-GP
PU4703 AON6552-GP
PU4705 AON6508-GP
PU4706 AON6508-GP
PC4716 SCD01U50V2KX-1GP
PC4702 SC10U25V6KX-1GP
PT4702 SE47U25VM-13-GP
47uF/25V,
Ripple Current=2.8Arms
ESR=30 mohm
6.6*6.6*5.9
0.36uH,
DCR=1.03mohm,
Idc=32.5A, Isat=28.8A
11.5*10*4
PL4704 IND-D36UH-54-GP
PR4705 2D2R6J-3-GP
PWR_81151_SNB1
PC4705 SC1KP50V2KX-1GP
PG4702 COPPER-CLOSE-GP-U
PG4703 COPPER-CLOSE-GP-U
46 CSP1
46 CSN1
VCC_CORE
PT4703 SE560U2D5VM-7-GP
PT4701 SE560U2D5VM-7-GP
PT4704 SE560U2D5VM-7-GP
PT4705 SE560U2D5VM-7-GP
PT4706 SE560U2D5VM-7-GP
PT4709 SE330U2D5VDM-2GP (R_)
560uF/2.5V,
Ripple Current=3.5 Arms
ESR= 14 mohm
6.3*5.9
46 PWM1
46,47,48 DRVCN
PR4701 51R2J-2-GP
PWR_81151_EN1
PWR_81151_VCC1
PU4704 NCP81151MNTBG-GP
PR4706 2D2R5J-1-GP
PC4704 SC1U16V2KX-GP
5V_SS
BOTTOM PAD CONNECT TO GND Through 4 VIAs

PWR_81151_BST2R
PR4707 0R5J-5-GP
PC4706 SCD1U25V3KX-GP (78.10424.2BL)
PR4708 0R5J-5-GP
PWR_81151_H2R
PR4709 10KR2J-3-GP
PWR_81151_BST2
PWR_81151_DRVH2
PWR_81151_SW2
PWR_81151_DRVL2
PU4707 AON6552-GP
PU4708 AON6552-GP
PU4710 AON6508-GP
PU4711 AON6508-GP
PC4701 SCD01U50V2KX-1GP
PC4707 SC10U25V6KX-1GP
PT4707 SE47U25VM-13-GP
PL4705 IND-D36UH-54-GP
PR4712 2D2R5J-3-GP
PWR_81151_SNB2
PC4709 SC1KP50V2KX-1GP
PG4701 COPPER-CLOSE-GP-U
PG4704 COPPER-CLOSE-GP-U
46 CSP2
46 CSN2
46 PWM2
46,47,48 DRVCN
PR4710 51R2J-2-GP
PWR_81151_EN2
PWR_81151_VCC2
PU4709 NCP81151MNTBG-GP
PR4711 2D2R5J-1-GP
PC4708 SC1U16V2KX-GP
5V_SS
BOTTOM PAD CONNECT TO GND Through 4 VIAs

TDC=79A
ICCMAX=86A
OCP>118.5A

PWR_81151_BST3R
PR4713 0R5J-5-GP
PC4710 SCD1U25V3KX-GP (78.10424.2BL)
PR4714 0R5J-5-GP
PWR_81151_H3R
PR4715 10KR2J-3-GP
PWR_81151_BST3
PWR_81151_DRVH3
PWR_81151_SW3
PWR_81151_DRVL3
PU4701 AON6552-GP
PU4712 AON6552-GP
PU4714 AON6508-GP
PU4715 AON6508-GP
PC4717 SCD01U50V2KX-1GP
PC4711 SC10U25V6KX-1GP
PT4708 SE47U25VM-13-GP
PL4701 IND-D36UH-54-GP
PR4717 2D2R6J-3-GP
PWR_81151_SNB3
PC4713 SC1KP50V2KX-1GP
PG4705 COPPER-CLOSE-GP-U
PG4706 COPPER-CLOSE-GP-U
46 CSP3
46 CSN3
46 PWM3
46,47,48 DRVCN
PR4716 51R2J-2-GP
PWR_81151_EN3
PWR_81151_VCC3
PU4713 NCP81151MNTBG-GP
PR4718 2D2R5J-1-GP
PC4712 SC1U16V2KX-GP
5V_SS
BOTTOM PAD CONNECT TO GND Through 4 VIAs

<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCORE OUTPUT (NCP81151)
Size: Custom
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 47 of 107

PWR_VCCGT

84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

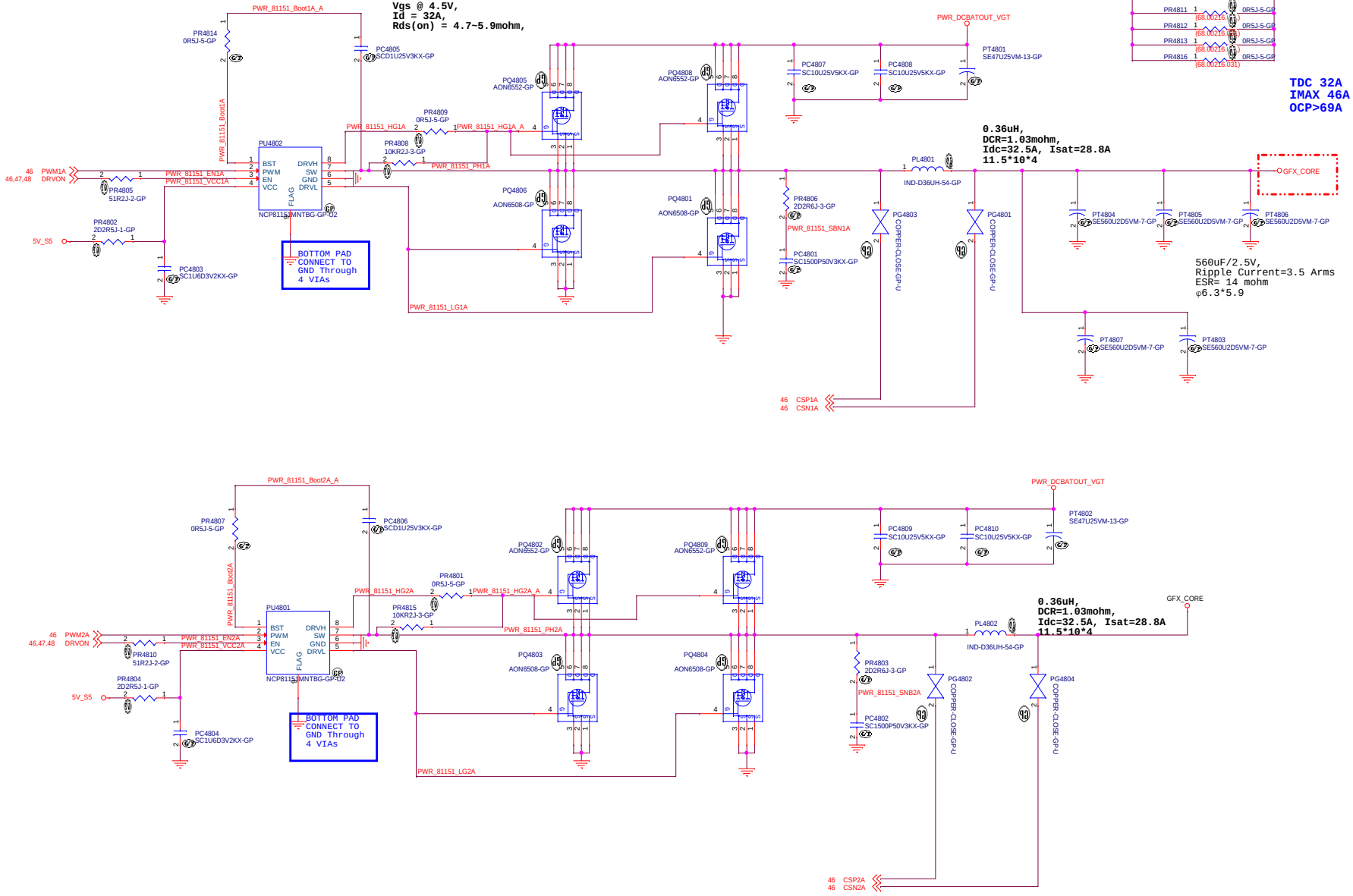
Input ripple current =6.39A
during Vout= 1.1V

47uF/25V,
Ripple Current=2.8Arms
ESR=30 mohm
6.6*6.6*5.9

TDC 32A
IMAX 46A
OCP>69A

0.36uH,
DCR=1.03mohm,
Idc=32.5A, Isat=28.8A
11.5*10*4

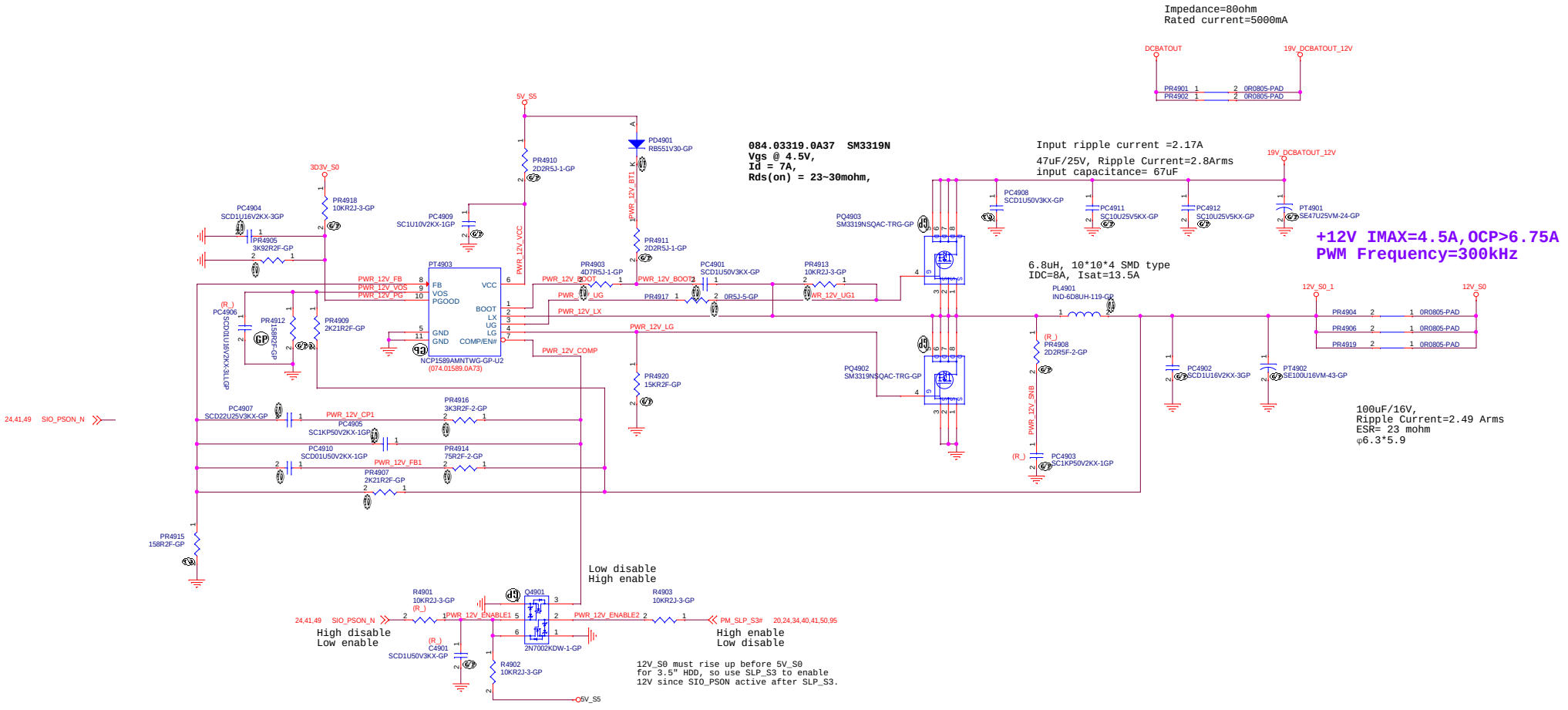
560uF/2.5V,
Ripple Current=3.5 Arms
ESR= 14 mohm
φ6.3*5.9



<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title	V_GT OUTPUT(NCP81151)	
Size C	Document Number: Consumer AIO Woody	Rev SA
Date: Thursday, November 26, 2015	Sheet 48 of 107	

PWR_12V



<Core Design>

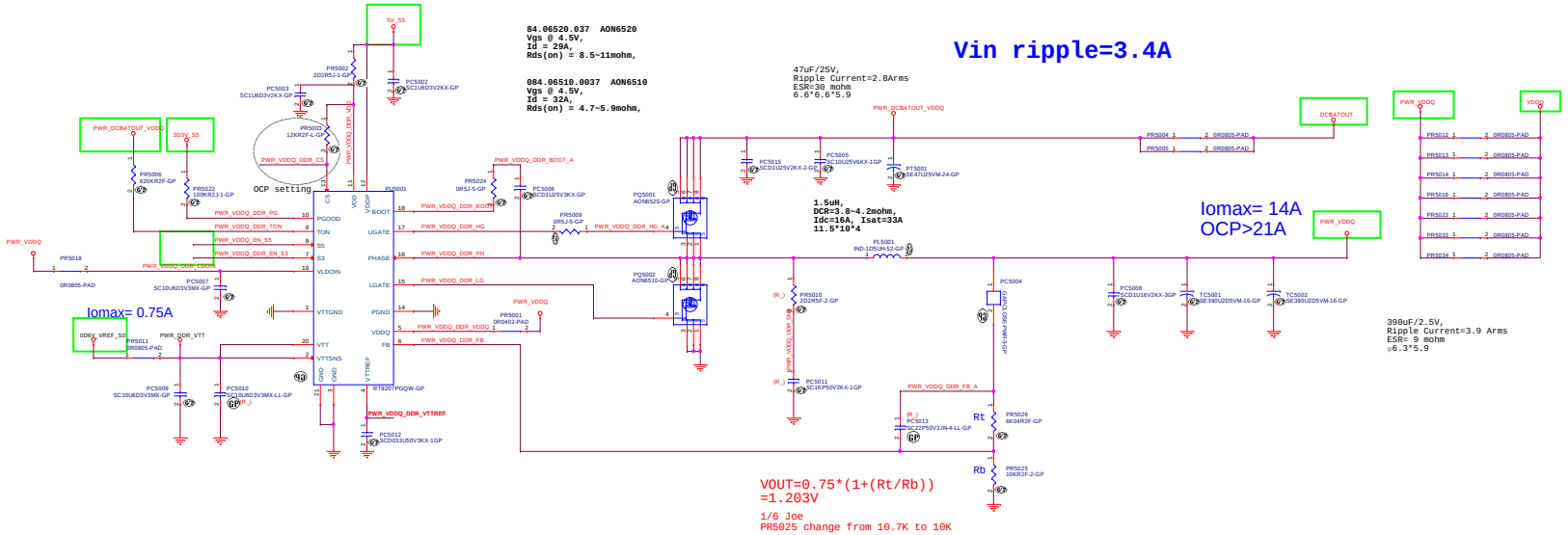
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DC to DC_12V (SY8246)

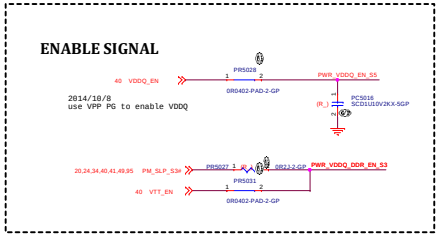
Size: C | Document Number: Consumer AIO Scotland | Rev: SA

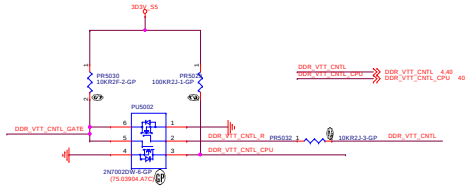
Date: Thursday, November 26, 2015 | Sheet 49 of 107

PWR_VDDQ

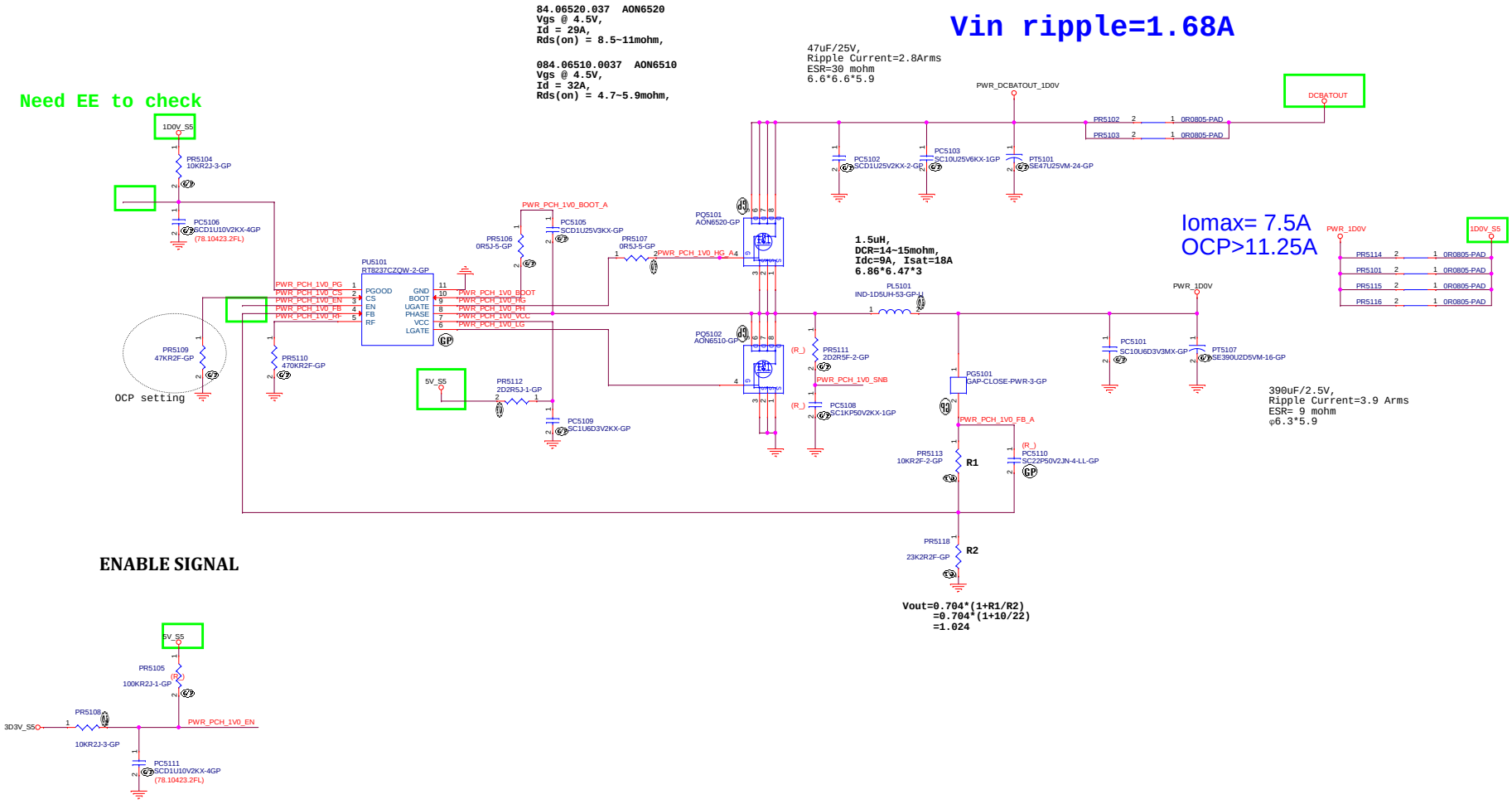


ENABLE SIGNAL





PWR_1D0V



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH_1P0V(RT8237C)

Size: Custom | Document Number: Consumer AIO Scotland | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 51 of 107

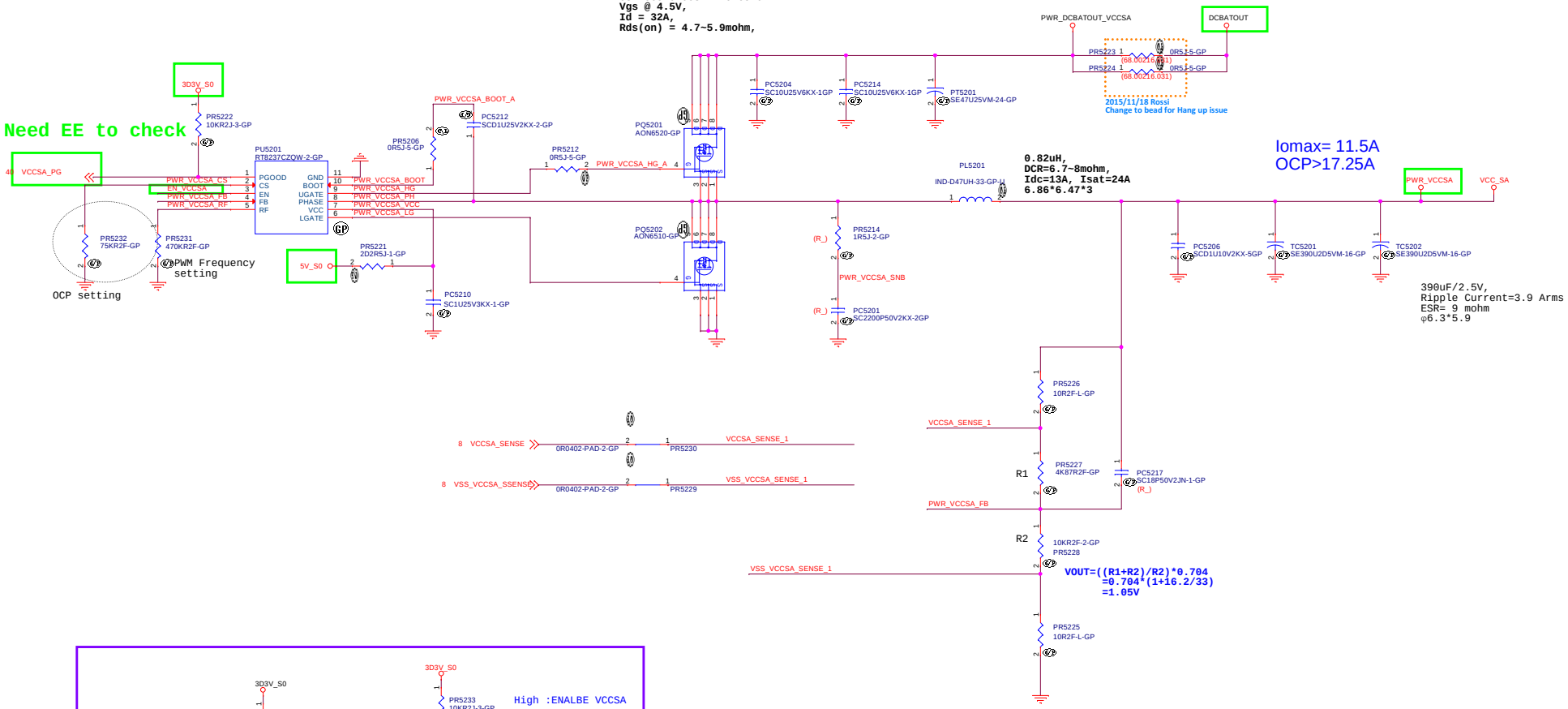
PWR_VCCSA

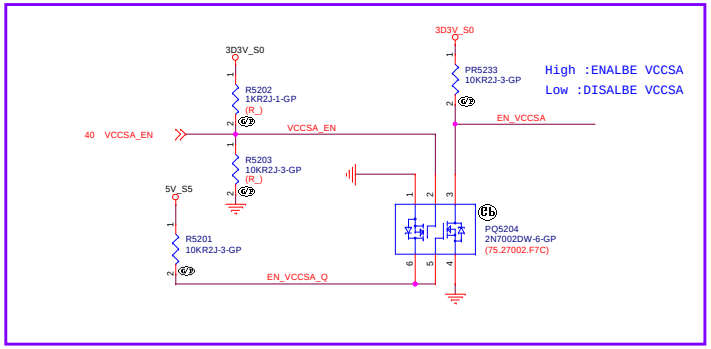
84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

Vin ripple=2.63A

Need EE to check





<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

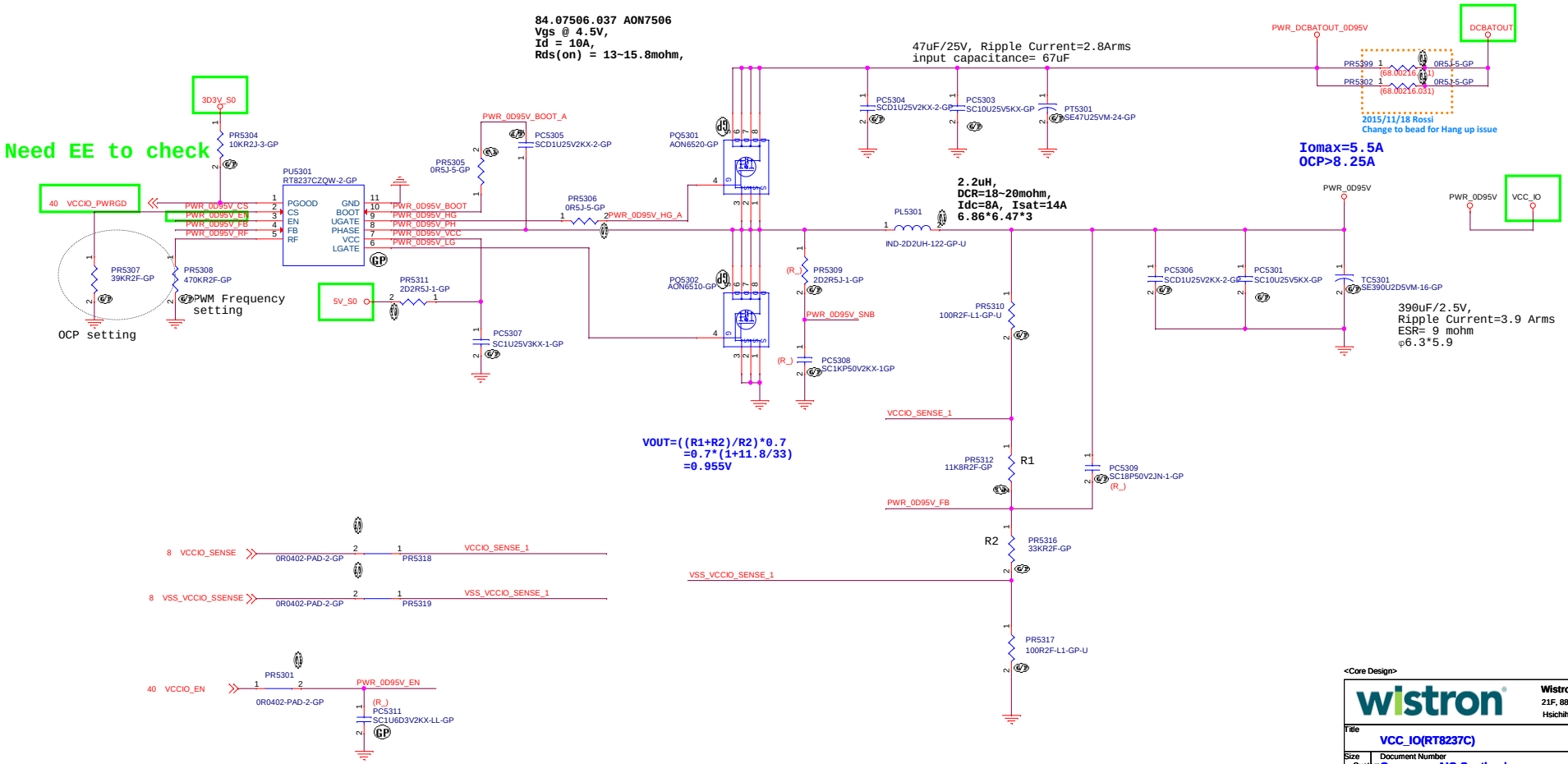
Title: VCC_SA(RT8237C)
Size: Custom
Document Number: Consumer AIO Scotland
Rev: SA
Date: Thursday, November 26, 2015
Sheet 52 of 107

PWR_VCCIO

84.07410.A37 SIS412DN
Vgs @ 4.5V,
Id = 7A,
Rds(on) = 24~29mohm,

84.07506.037 AON7506
Vgs @ 4.5V,
Id = 10A,
Rds(on) = 13~15.8mohm,

Vin ripple=1.2A



<Core Design>

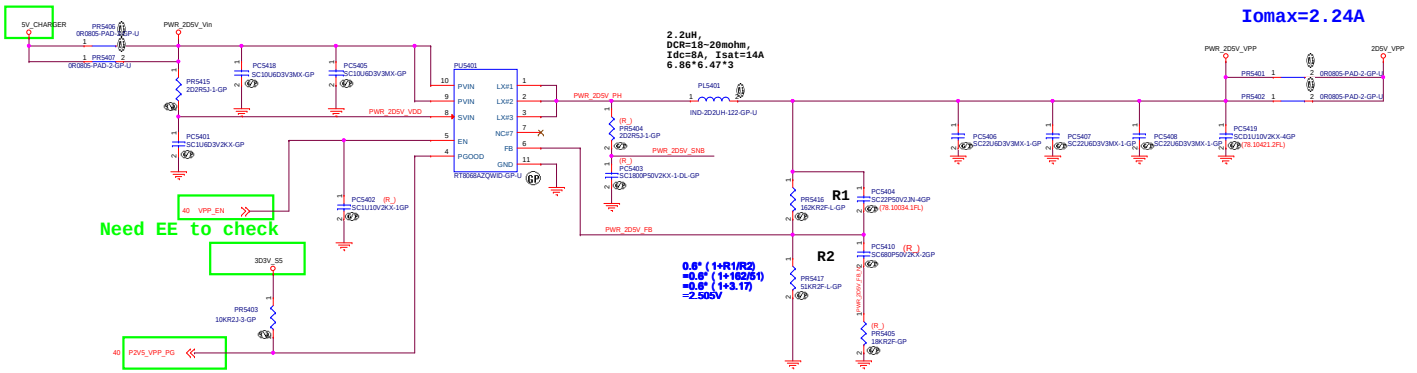
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCC_IO(RT8237C)

Size: Custom | Document Number: Consumer AIO Scotland | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 53 of 107

PWR_2D5V_VPP



<Core Design>

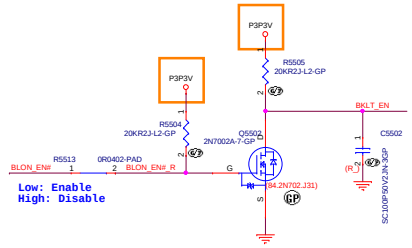
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

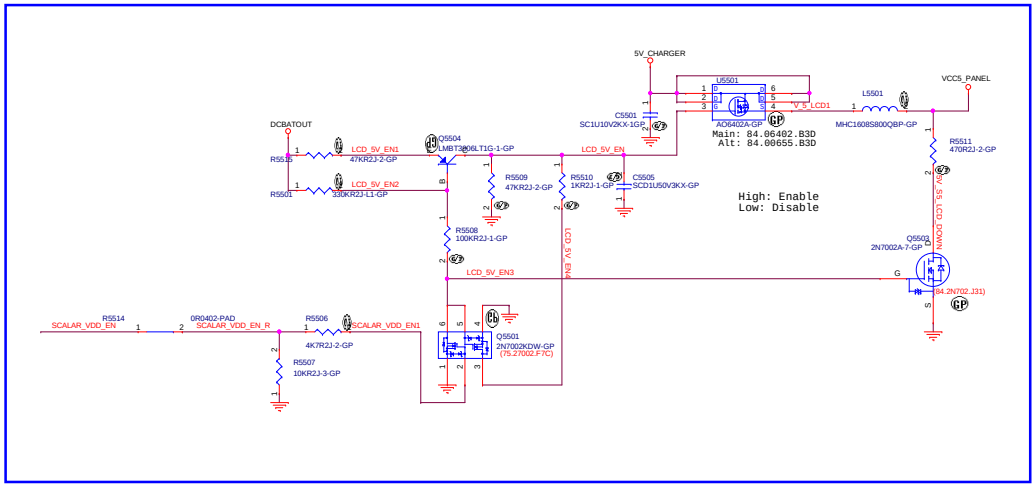
Title: LDO_1P5V_1P8V_2P5V

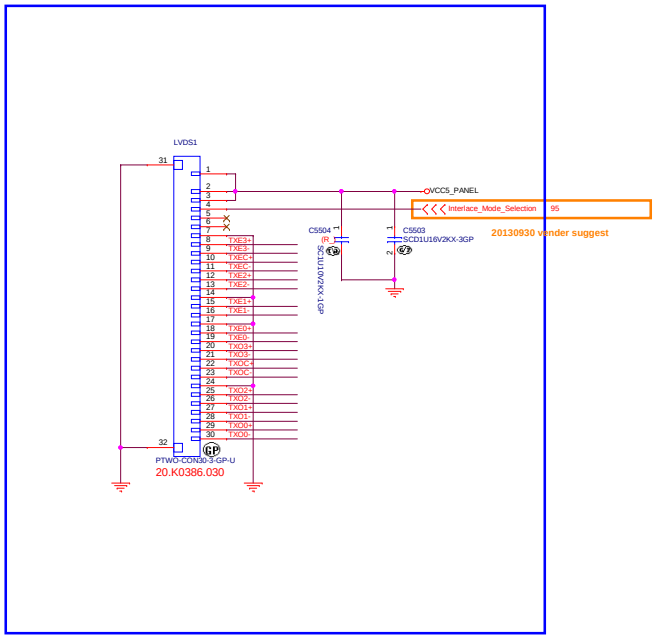
Size: Custom | Document Number: Consumer AIO Scotland | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 54 of 107

SSID = VIDEO







LVDS

95	TXO0-	TXO0-
95	TXO0+	TXO0+
95	TXO1-	TXO1-
95	TXO1+	TXO1+
95	TXO2-	TXO2-
95	TXO2+	TXO2+
95	TXOC-	TXOC-
95	TXOC+	TXOC+
95	TXO3-	TXO3-
95	TXO3+	TXO3+
95	TXE0-	TXE0-
95	TXE0+	TXE0+
95	TXE1-	TXE1-
95	TXE1+	TXE1+
95	TXE2-	TXE2-
95	TXE2+	TXE2+
95	TXEC-	TXEC-
95	TXEC+	TXEC+
95	TXE3-	TXE3-
95	TXE3+	TXE3+

95	SCALAR_BKLT_CTRL	SCALAR_BKLT_CTRL
95	SCALAR_VDD_EN	SCALAR_VDD_EN
95	BLON_EN#	BLON_EN#
24,44	BKLT_EN	BKLT_EN
44	BKLT_ADJ	BKLT_ADJ

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LVDS Connector

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 55 of 107

HDMI

56,95 HDMI1_D2+
56,95 HDMI1_D2-
56,95 HDMI1_D1+
56,95 HDMI1_D1-
56,95 HDMI1_D0+
56,95 HDMI1_D0-
56,95 HDMI1_CK+
56,95 HDMI1_CK-

24,56,95 DET_HDMI#

95 DDC_WP
56,95 HDMI1_SDA
56,95 HDMI1_SCL

95 HPD_SCA1

HDMI-IN Connector

HDIN1

HDMI1_D2+_C
HDMI1_D2-_C
HDMI1_D1+_C
HDMI1_D1-_C
HDMI1_D0+_C
HDMI1_D0-_C
HDMI1_CK+_C
HDMI1_CK-_C
DET_HDMI_C
HDMI_SCL_IN
HDMI_SDA_IN
HDMI_HPDET

24,56,95 DET_HDMI#
R5615 1KR2J-1-GP (M_)

HDMI_5V
HDMI_5V
C5604 SCD1U16V2ZY-2GP (R_)

SKT-HDMI19P-57-GP (M_)

HPD_SCA1
R5619 100R2J-2-GP (M_)

20130910 Ryan

EMI/ESD near Connector

D5603
HDMI1_D0+_C
HDMI1_D0-_C
HDMI1_CK+_C
HDMI1_CK-_C
SP3010-04UTG-GP (R_)

D5604
HDMI1_D1-_C
HDMI1_D1+_C
HDMI1_D2-_C
HDMI1_D2+_C
SP3010-04UTG-GP (R_)

EMI/ESD near Connector

HDMI_5V
3D3V_A
R5618 1KR2J-1-GP
20130930 vender suggest
R5616 10KR2J-3-GP (M_)
HPD_SCA1
DET_HDMI#
U5602 AZ23C6V2-1-GP

HDMI_SCL_IN
HDMI_SDA_IN
U5603 AZ23C6V2-1-GP

Reserved for HDMI re-Driver

V_1P5

08/11 Allen modify

U5605
INPUT
OUTPUT
ADJ/GND
AZ1117CR-ADJTRG1-GP-U (M_074.01117.0A38)

3D3V_A
C5608 SC10U10V5KX-2DLGP (M_78.10623.51L)
V_1P5_HDMI
C5607 SCD1U16V2KX-3DLGP (M_78.10421.2FL)
R2
R5627 180R3F-GP (M_)
1117_ADJ
R1
R5628 36R3F-GP (M_)

Vout = 1.25*(1+R1/R2)

3D3V_A
C5618 SCD1U16V2KX-3GP (M_)
C5617 SCD1U16V2KX-3GP (M_)

Change to oohm for Debug

HDMI1_D0+_C R5621 R2J-2-GP HDMI1_DATA_IC_P0
HDMI1_D0-_C R5622 R2J-2-GP HDMI1_DATA_IC_N0
HDMI1_D1+_C R5623 R2J-2-GP HDMI1_DATA_IC_P1
HDMI1_D1-_C R5624 R2J-2-GP HDMI1_DATA_IC_N1
HDMI1_D2+_C R5625 R2J-2-GP HDMI1_DATA_IC_P2
HDMI1_D2-_C R5639 R2J-2-GP HDMI1_DATA_IC_N2
HDMI1_CK+_C R5640 R2J-2-GP HDMI1_DATA_IC_P3
HDMI1_CK-_C R5641 R2J-2-GP HDMI1_DATA_IC_N3

TPAD24 TP3404 1HDMI_SCL_IN_U5604
TPAD24 TP3405 1HDMI_SDA_IN_U5604

V_1P5_HDMI
3D3V_A

U5604
VDD33 VDD33
VDDRX VDDRX
VDDTX VDDTX
VDDTA
I2C_CTL_EN
IN_D0P IN_D0N IN_D1P IN_D1N IN_D2P IN_D2N IN_CKP IN_CKN
EQ/I2C_ADDR0 CFG/I2C_ADDR1
PRE ISET PD#
DCIN_EN/SCL_CTL DDCBUF/SDA_CTL
SCL_SNK SDA_SNK
SCL_SRC SDA_SRC
HPD_SRC HPD_SNK
REXT
GND GND GND
OUT_D0P OUT_D0N OUT_D1P OUT_D1N OUT_D2P OUT_D2N OUT_CKP OUT_CKN
HDMI_LANE0_IC_DP HDMI_LANE0_IC_DN HDMI_LANE1_IC_DP HDMI_LANE1_IC_DN HDMI_LANE2_IC_DP HDMI_LANE2_IC_DN HDMI_LANE3_IC_DP HDMI_LANE3_IC_DN
EQ CFG PRE ISET U5604_PD_N DCIN_EN DDCBUF HDMI1_SCL_U5604 HDMI1_SDA_U5604
PS8407ATQFN40GTR2-A1-GP (M_)

TP3402 TPAD24
TP3403 TPAD24 (M_)

HDMI_HDCP_READY
REXT
R5626 4K99R2F-L-GP (M_63.56234.1DL)

24,96 SCALAR_EN
R5643 1 0R2J-2-GP U5604_PD_N (M_)

mount if use

R5630 4K7R2F-GP CFG (M_)
R5635 4K7R2F-GP DCIN_EN (M_)
R5629 4K7R2F-GP EQ (R_)
R5631 4K7R2F-GP ISET (R_)
R5632 4K7R2F-GP DDCBUF (M_)
R5636 4K7R2F-GP PRE (R_)
R5642 4K7R2F-GP HDMI_HDCP_READY (M_)

mount if use

V_1P5_HDMI
C5610 SCD01U50V2KX-1DLGP (M_78.10324.2FL)
C5609 SCD1U16V2KX-3DLGP (M_78.10421.2FL)
Near Pin 20, 31

V_1P5_HDMI
C5612 SCD01U50V2KX-1DLGP (M_78.10324.2FL)
C5611 SCD1U16V2KX-3DLGP (M_78.10421.2FL)
Near Pin 19

V_1P5_HDMI
C5614 SCD01U50V2KX-1DLGP (M_78.10324.2FL)
C5616 SCD1U16V2KX-3DLGP (M_78.10421.2FL)
Near Pin 19

V_1P5_HDMI
C5613 SCD01U50V2KX-1DLGP (M_78.10324.2FL)
C5615 SCD1U16V2KX-3DLGP (M_78.10421.2FL)
C5615: 11/14 BOM cost
Near Pin 20, 31

HDMI_CLK & DATA level shift

don't need from Scalar

5V_S0
R5617 0R0402-PAD (M_)

HDMI_5V
R5620 100KR2J-1-GP (M_)
D5602 BZX84-C6V8-GP (M_)

DDC5V_HDMI_R
D5601 BAT54C-12-GP (M_75.00054.T7D)
DDC5V_HDMI
DDC5V_HDMI

R5614 4K7R2J-2-GP
R5613 4K7R2J-2-GP
R5609 10KR2J-3-GP (M_)
C5603 SCD1U16V2ZY-2GP (R_)

HDMI_SCL_IN
HDMI_SDA_IN
R5610 47R2J-2-GP
R5611 47R2J-2-GP (M_)
(M_64.10015.60L)(M_64.10015.60L)
DDC_WP_1

U5601
VCC WC# SCL SDA
E0 E1 E2 VSS
M24C02-WMN6TP-1-GP (M_)

56,95 HDMI1_SDA
56,95 HDMI1_SCL

C5605 SC33P50V2JN-3GP (R_)
C5606 SC33P50V2JN-3GP (R_)
R5612 100R2J-2-GP (M_)
DDC_WP

C5601 DUMMY-C2
C5602 DUMMY-C2

TR5602
56,95 HDMI1_D0-
56,95 HDMI1_D0+
HDMI_LANE0_IC_DN
HDMI_LANE0_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

TR5604
56,95 HDMI1_CK-
56,95 HDMI1_CK+
HDMI_LANE3_IC_DN
HDMI_LANE3_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

TR5601
56,95 HDMI1_D2-
56,95 HDMI1_D2+
HDMI_LANE2_IC_DN
HDMI_LANE2_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

TR5603
56,95 HDMI1_D1-
56,95 HDMI1_D1+
HDMI_LANE1_IC_DN
HDMI_LANE1_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDMI IN
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 56 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDMI OUT_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

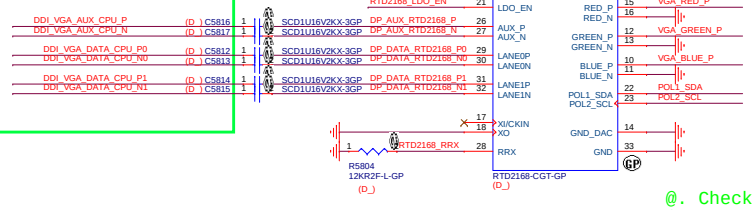
Date: Thursday, November 26, 2015 | Sheet 57 of 107

Pin#	Description	Type	Note
5	DVCC_33	Power	Digital power at 3.3V
9	VDD_DAC_33	Power	Analog power at 3.3V
19	VCCK_12	Power	Digital power at 1.2V
20	DVCC_33	Power	Digital power at 3.3V
24	AVCC_33	Power	Analog power at 3.3V
25	AVCC_12	Power	Analog power at 1.2V

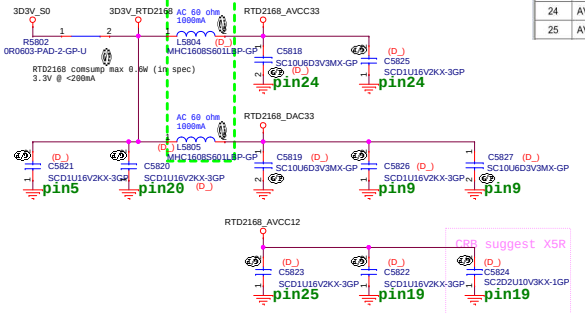
7 DDI_VGA_AUX_CPU_P
7 DDI_VGA_AUX_CPU_N
7 DDI_VGA_DATA_CPU_P0
7 DDI_VGA_DATA_CPU_N0
7 DDI_VGA_DATA_CPU_P1
7 DDI_VGA_DATA_CPU_N1
16 CRT_HPD_PCH
24,44 SMBCLK2_SIO
24,44 SMBDAT2_SIO

DP to VGA converter: RTD2168

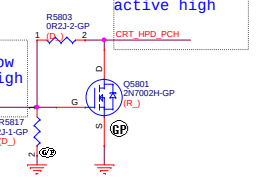
DDI EDP set DP INPUT by VBIOS



2013/10/23
Change L5312 & L5311 that follow Brian



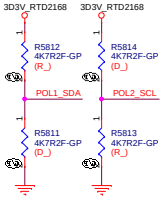
VGA cable
un-Plug: Low
Plug: High



@. Check if need level shift for all signals
@. ESD solution follow Rosa Tigris

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



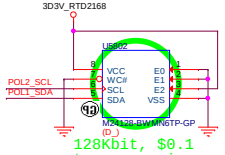
RTD2168 Supports three operation mode for system design. Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode: PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

EEPROM MODE

In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

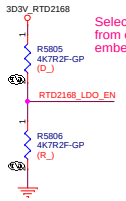


128Kbit, $0.1
too expensive

I2C address=0xA8

Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

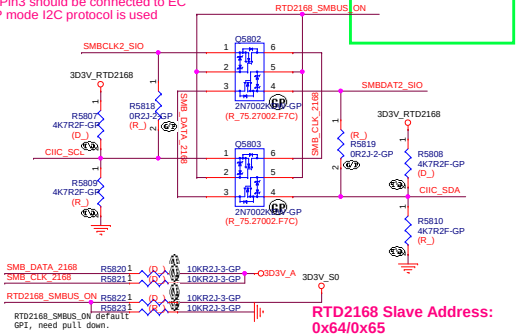


Select VCCK_V12 source from external 1.2V or embedded LDO

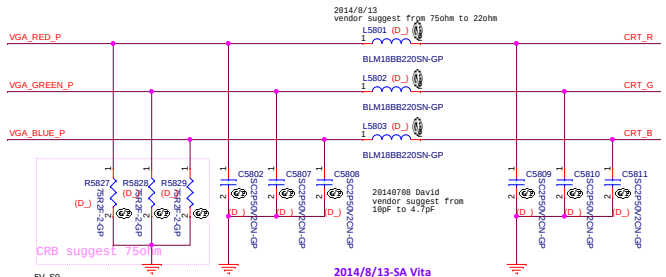
EP Mode

2014/7/30
need check

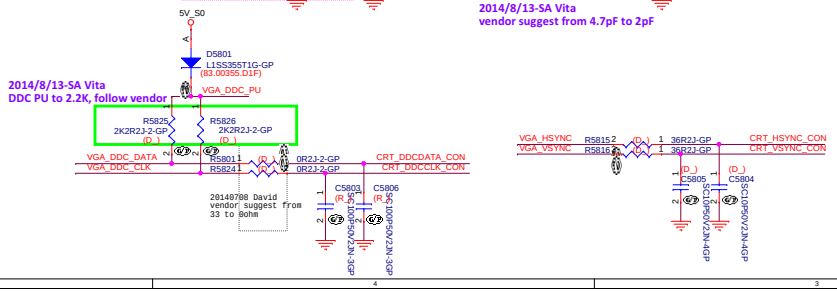
Pin2, Pin3 should be connected to EC for EP mode I2C protocol is used



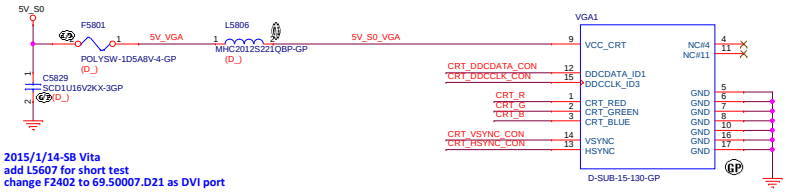
RTD2168 Slave Address: 0x64/0x65



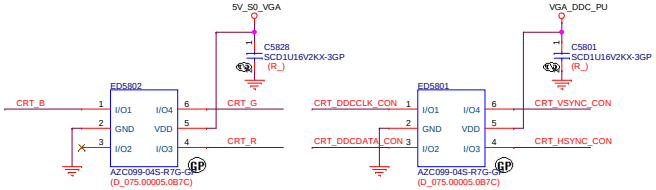
2014/8/13-SA Vita
vendor suggest from 4.7pF to 2pF



2014/8/13-SA Vita
DDC PU to 2.2K, follow vendor



2015/1/14-SB Vita
add L5607 for short test
change F2402 to 69.50007.D21 as DVI port



2015/01/18-SB Corree
add ED6520 / ED2 as 075.00005.0B7C (EMI request)
2015/01/23-SB Vita
change ED6520 / ED2 F7 to (D_075.00005.0B7C)

<Core Design>

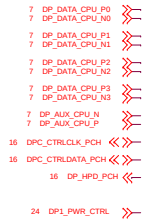
wistron

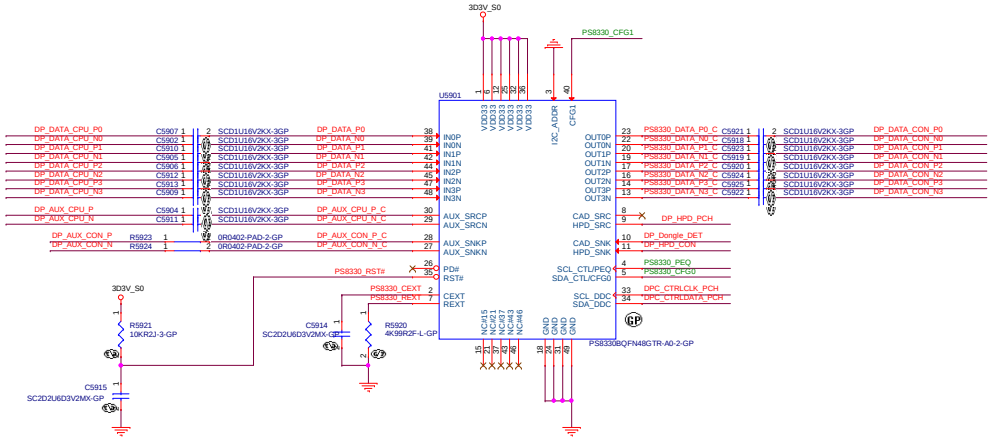
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

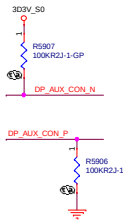
Title: DVI/CRT

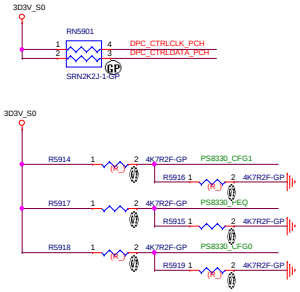
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

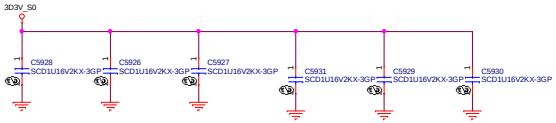
Date: Thursday, November 26, 2015 | Sheet 58 of 107

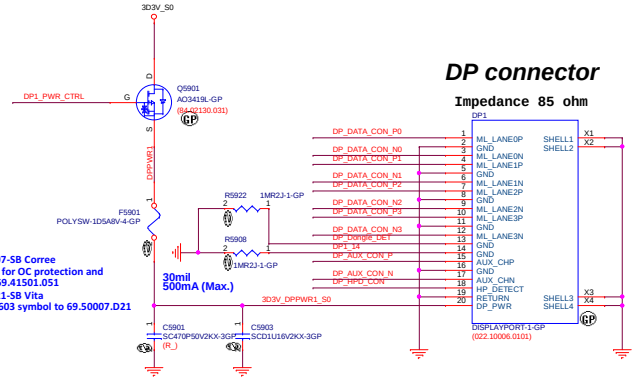










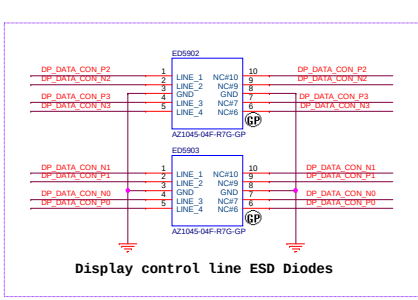


DP connector

Impedance 85 ohm

2015/01/07-SB Corree
add F5603 for OC protection and
use F7 as 69.41501.051
2015/01/21-SB Vita
change F5603 symbol to 69.50007.D21

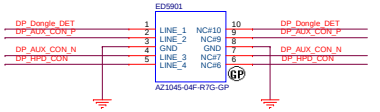
30mil
500mA (Max.)



Display control line ESD Diodes

ESD

2015/01/18-SB Corree
Add ED5701 / ED5702 / ED5703 as 75.01045.073 from EMI request



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Display port

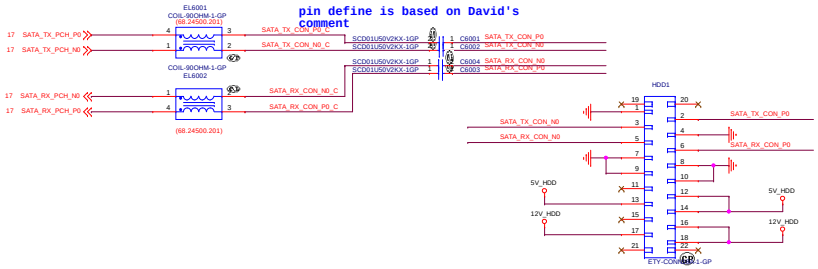
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

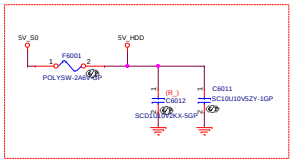
Date: Thursday, November 26, 2015 | Sheet 59 of 107

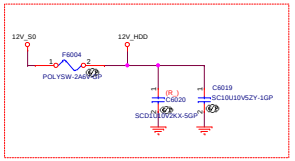
SATA Port 0

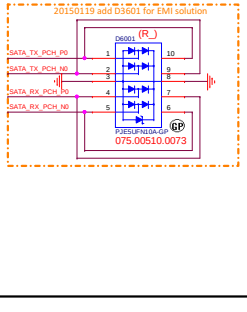
SATA HDD Connector

Michael 2012/01/03
pin define is based on David's comment



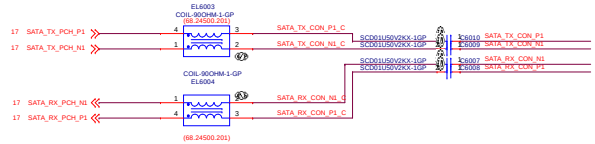


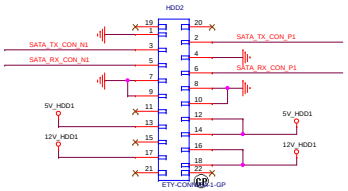


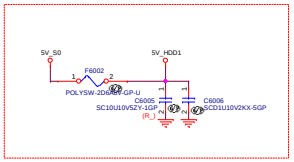


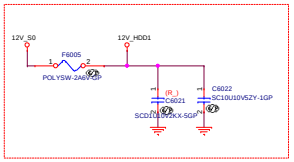
SATA Port 1

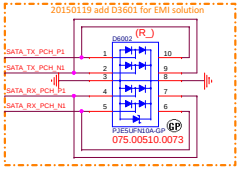
SATA HDD Connector





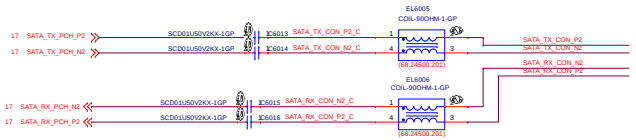


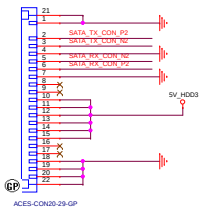


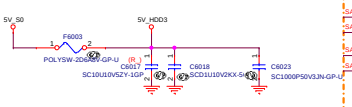


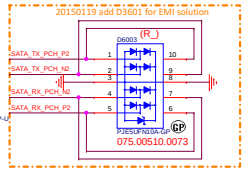
SATA Port 2

ODD Connector









<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDD/ODD

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 60 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Mini PCIE Card TV Tuner_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 61 of 107

M.2 2230 / 1630 Key E Type

Mini PCIE (WLAN)

15 USB_PCH_PP7
15 USB_PCH_PN7

PCIEX1

16 PCIE_RX_PCH_N7
16 PCIE_RX_PCH_P7
16 PCIE_TX_WLAN_N7
16 PCIE_TX_WLAN_P7

18 PEG_CLK1_WLAN
18 PEG_CLK1_WLAN#

OTHERS

20 PCIE_WAKE_N_PCIE
24,62,63 PLT_WLAN_RST#
18 PEG_CLKREQ1_WLAN#
15,62 W1_DISABLE_N
15,62 W2_DISABLE_N
17 WLAN_RST_PCH
17 WLAN_DAT_PCH
17 WLAN_CLK_PCH

20 SLP_WLAN_N → SLP_WLAN_N
24,97 LAN_EN_PWR_SIO → LAN_EN_PWR_SIO

3D3V_S5

R6208 10KR2J-3-GP
R6204 10KR2J-3-GP

V_3P3_WLAN

2014/10/1-Corree
Change to Key.E type

NGFFE1

76	3_3VAUX	77	GND
74	3_3VAUX	75	RESERVED#73
72	RESERVED#70	73	RESERVED#71
70	RESERVED#68	71	GND
68	RESERVED#66	69	RESERVED#67/2ND_LANE_PERN1
66	GPIO0_NFC_RESET#/MGPIO7	67	RESERVED#65/2ND_LANE_PERP1
64	NFC_I2C_IRQ/MGPIO5	65	GND
62	NFC_I2C_SM_CLK	63	RESERVED#61/2ND_LANE_PETN1
60	NFC_I2C_SM_DATA	61	RESERVED#59/2ND_LANE_PETP1
58	W_DISABLE#1	59	GND
56	RESERVED#54/W_DISABLE#2	57	PEWAKE0#
54	PERST0#	55	CLKREQ0#
52	SUSCLK_32KHZ	53	GND
50	COEX1	51	REFCLKN0
48	COEX2	49	REFCLKP0
46	COEX3	47	GND
44	CLINK_CLK	45	PERN0
42	CLINK_DATA	43	PERP0
40	CLINK_RESET	41	GND
38	UART_CTS	39	PETN0
36	UART_RTS	37	PETP0
34	UART_TX	35	GND
32		33	
22	UART_RX	23	SDIO_RESET
20	UART_WAKE	21	SDIO_WAKE
18	GND	19	SDIO_DAT3
16	LED#2	17	SDIO_DAT2
14	PCM_OUT	15	SDIO_DAT1
12	PCM_IN	13	SDIO_DAT0
10	PCM_SYNC	11	SDIO_CMD
8	PCM_CLK	9	SDIO_CLK
6	LED#1	7	GND
4	3_3VAUX	5	USB_D-
2	3_3VAUX	3	USB_D+
		1	GND
NP2	NP2	NP1	NP1

NGFF_KEY_E_75P
SKT-NGFF75P-91-GP
062.10003.0611

20,31 SMB_CLK_RESUME → R6209 0R2J-2-GP → SMB_CLK_MINI
20,31 SMB_DATA_RESUME → R6210 0R2J-2-GP → SMB_DATA_MINI
15,62 W1_DISABLE_N → W1_DISABLE_N
15,62 W2_DISABLE_N → W2_DISABLE_N
24,62,63 PLT_WLAN_RST# → R6207 0R0402-PAD-2GP → PLT_WLAN_RST_C
20 PCH_SUSCLK_WLAN → PCH_SUSCLK_WLAN

WLAN_CLK_PCH → R6201 0R2J-2-GP → WLAN_CLK_CON
WLAN_DAT_PCH → R6202 0R2J-2-GP → WLAN_DAT_CON
WLAN_RST_PCH → R6203 0R2J-2-GP → WLAN_RST_CON

Controller Link interface is the Management communication link between the Skylake PCH and Intel Wireless cards

PLT_WLAN_RST# → C6205 SCD1U25V2KX-2GP

MINI1_WAKE# → R6205 0R0402-PAD-2GP → MINI_CLKREQ#_WLAN_C
MINI_CLKREQ#_WLAN_C → R6206 0R0402-PAD-2GP → PEG_CLKREQ1_WLAN#
0R2J-2-GP → R6211 PCIE_WLAN_WAKE# → PCIE_WLAN_WAKE# 24
PCIE_WAKE_N_PCIE

PEG_CLK1_WLAN#
PEG_CLK1_WLAN

PCIE_RX_PCH_N7
PCIE_RX_PCH_P7
PCIE_TX_WLAN_N7
PCIE_TX_WLAN_P7

2014/10/7
TX connect to TX, RX connect to RX

2014/10/1-Corree
TX connect to RX , RX connect to TX

2014/9/16
add EL3605 for NGFFE1 (follow Rosa Tigris)

USB_CON_PN7 → EL6201 → USB_PCH_PP7
USB_CON_PP7 → EL6201 → USB_PCH_PN7
EL6201 COIL-900HM-1GP (66.R0036.04L)

USB_CON_PN7
USB_CON_PP7

Close to Pin2/4/72/74

V_3P3_WLAN
C6204 SCD1U25V2KX-2-GP
C6202 SC10U6D3V5KX-1GP
C6201 SCD1U25V2KX-2-GP
C6203 SCD1U25V2KX-2-GP

LAN Power

LAN PWR delay circuit --> Verify SA

3D3V_S5
2010/05/06
R6216 100KR2J-1-GP (R_)
R6213 10KR2J-3-GP (R_)
R6218 10KR2J-3-GP (R_)
LAN_EN_W2
LAN_EN_W3
5V_S5
R6217 100KR2J-1-GP (R_)
C6206 SCD1U16V2KX-3GP (R_)
3D3V_S5
Q6202 AO3419L-GP (R_84.02130.031)
A03419 PMOS 3.5A
R6214 0R5J-5-GP
V_3P3_WLAN
R6215 10KR2J-3-GP (R_)
Add for leveage prevent

LAN_EN_PWR_SIO → R6212 10KR2J-3-GP (R_) → LAN_EN_W1
SLP_WLAN_N → R6219 10KR2J-3-GP (R_)
LAN_EN_W1 → Q6201 MMBT3904-3-GP (R_84.T3904.H11)
C6207 SC10U10V3MX-GP (R_)

WLAN (M2 key E)

HS5 STF256R109H124-GP

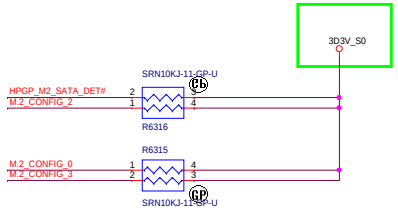
<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

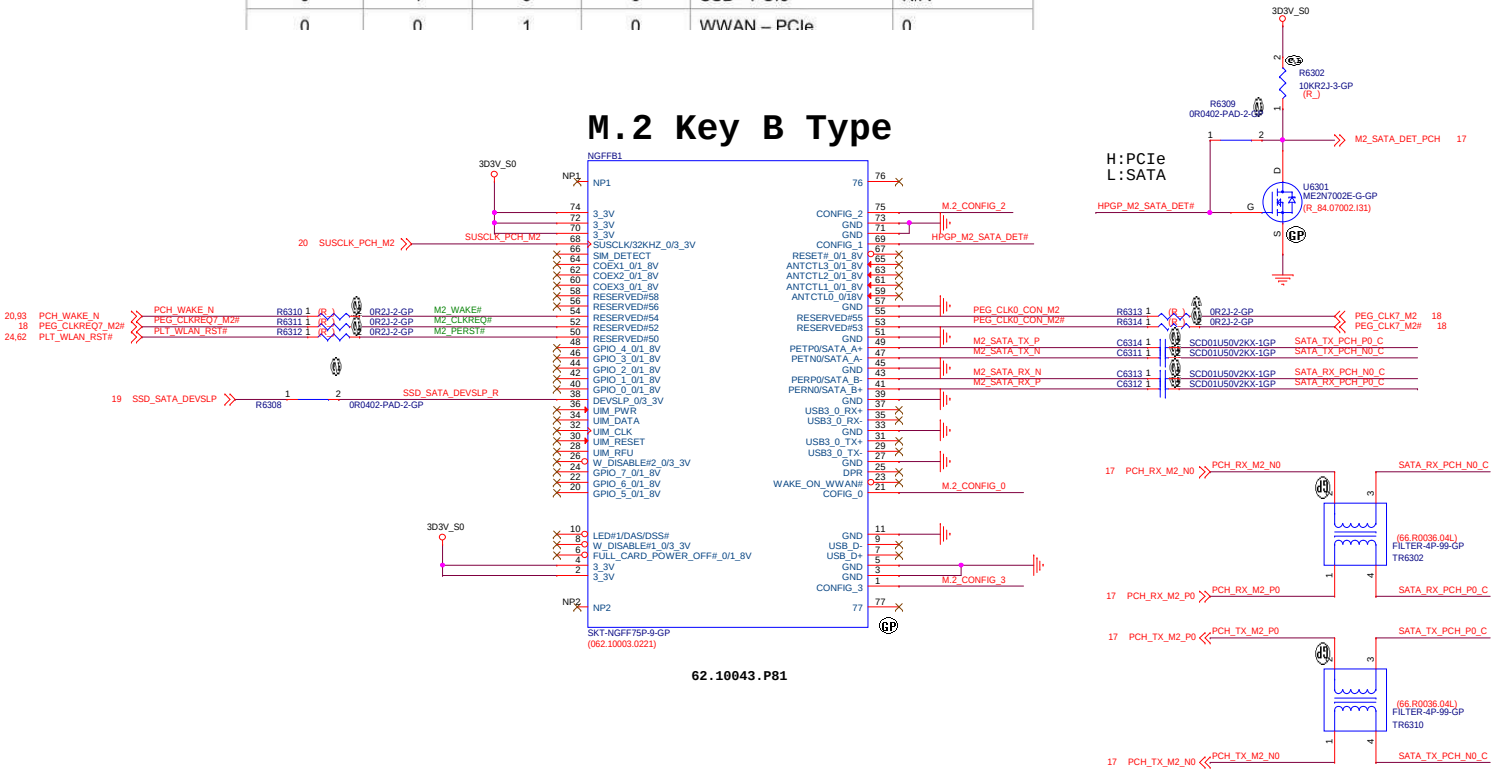
Title: WLAN and BT--NGFF
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 62 of 107

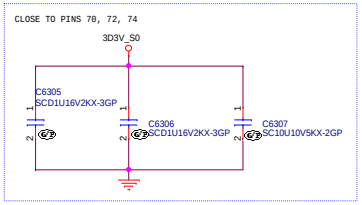
Table 46. Socket 2 Module Configuration Table

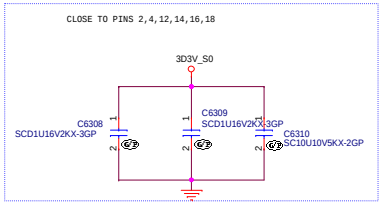
Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0



M.2 Key B Type







<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

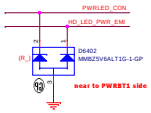
Title: SSD-NGFF

Size: C | Document Number: Consumer AIO Woody | Rev: SA

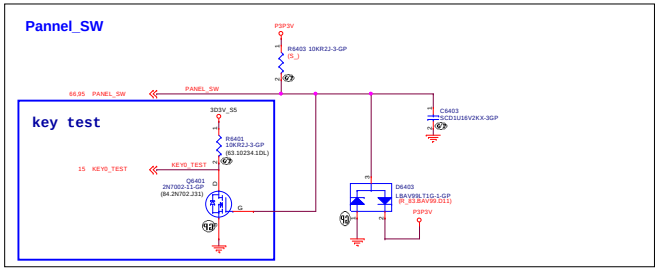
Date: Thursday, November 26, 2015 | Sheet 63 of 107

PWR BTN

20141203 Add D1 prevent ESD when Fab assembly



Pannel_SW



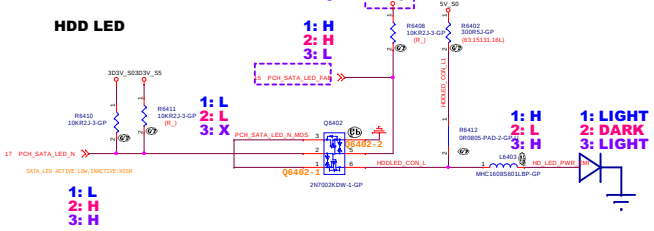
20141204 Modify HDDLED control logic

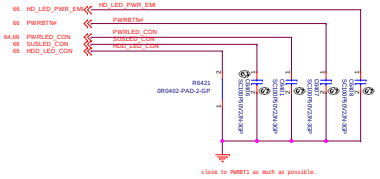
STATE	PCH_SATA_LED_N	PCH_SATA_LED_FAB	PCH_SATA_LED_N_MOS	Q6402-1	Q6402-2	HDDLED_CON	LED
1	L	H	L	OFF	ON	H	LIGHT
2	H	H	L	ON	ON	L	DARK
3	H	L	X	OFF	OFF	H	LIGHT

Note: 3. for FAB HDDLED test,
PCH_SATA_LED_FAB default is GPO High

20150115 Ryan

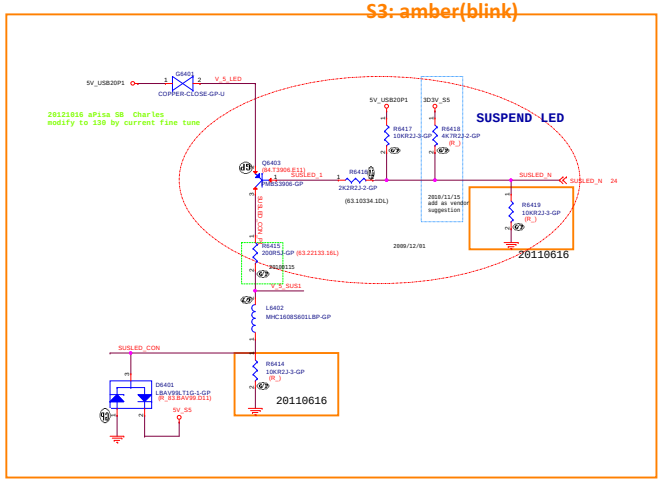
HDD LED



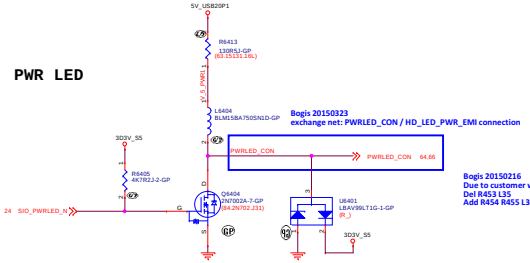


20150109 modify PWRLED behavior

~~S0: white(keep light)~~
~~S3: amber(blink)~~



PWR LED



System LED Definition

S0/S1(Blue), S3(amber), S4(off), S5(off)

	S0	S3	S4/S5
SUSLED_N	LOW	HIGH	HIGH
SIO_PWRLED_N	LOW	HIGH	HIGH

PC Health LED Definition

POWER/ SUSLED Warning LED

	Normal		Warning		OFF
	S0	S3	S0	S3	S4/S5
SUSLED_N	HIGH	H & L PWM (Breathing)	H & L (Blinking)	H & L (Blinking)	HIGH
SIO_PWRLED_N	LOW	HIGH	LOW	LOW	HIGH

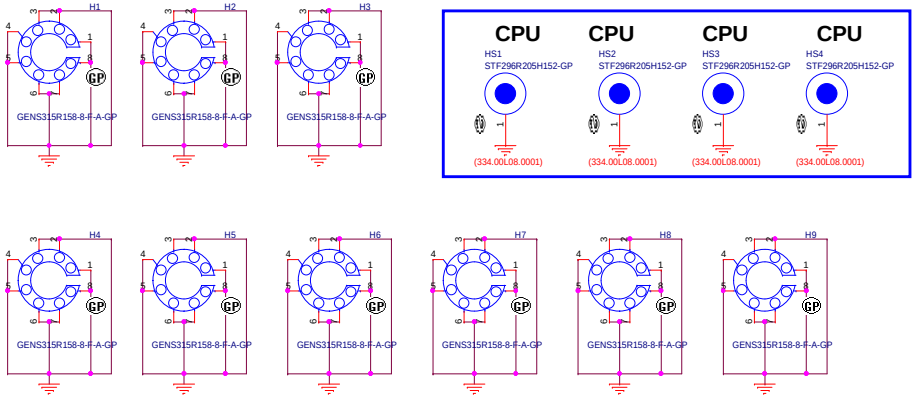
S0/Good (Blue)
S0/Warning (Blink Red)
S3/Good (Blink Blue)
S3/Warning (Blink Red)
S4/S5 (off)

<Core Design>

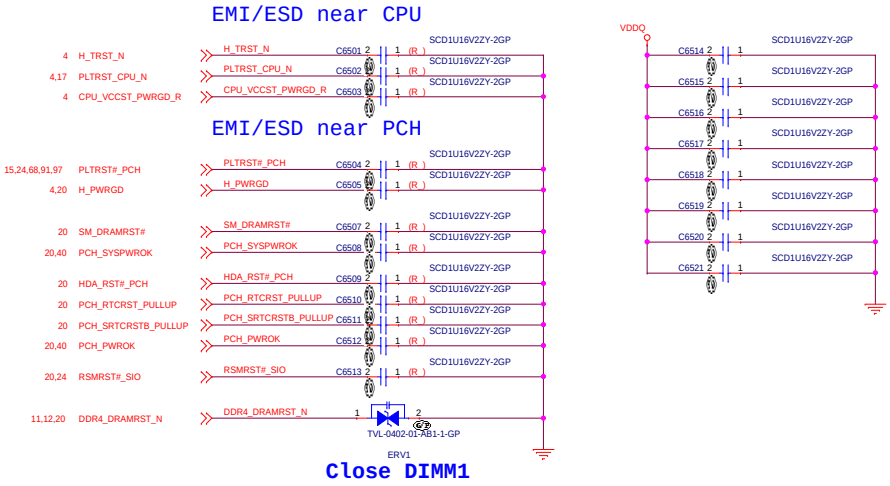
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PWR BT/Side Key/LED
Size: D
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 64 of 107

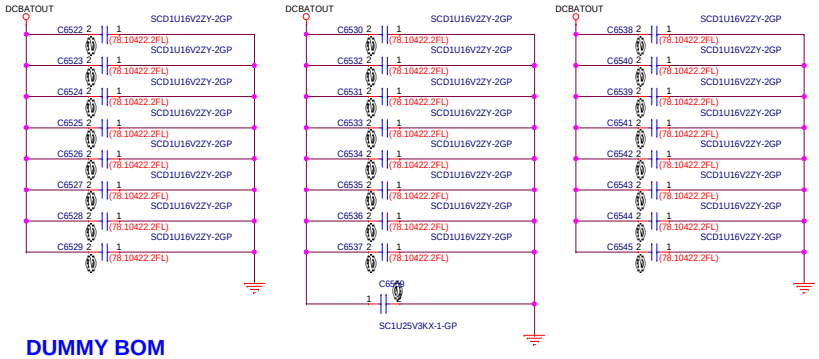
Stand off&Hole

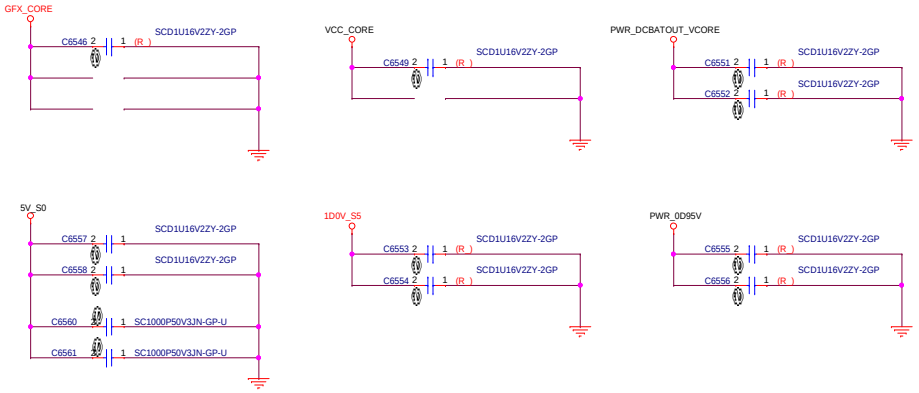


EMI CAP



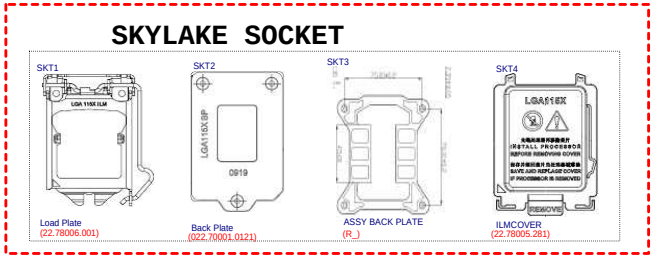
Close DIMM1





DUMMY BOM

Material part



GSKT1
GASKET
(R_334.03508.0001)

GASKET FOR WIESON HDMI

GSKT2
GASKET
(R_334.0350F.0001)

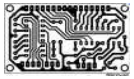
GASKET FOR TCONN HDMI

Battery Symbol

BAT3
BATTERY CR2032
(R_23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

PCB Symbol



PCB1
PCB
(R_)

HeatSink Symbol

Del PCHHS1 by Thermal--Ryan 0225

PCHHS1
HEATSINK
(60.3ET05.001)

Vendor
P/N:
60.3MN01.011(second source)
60.3MN01.001

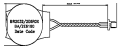
LABEL

LBL1
LABEL
(40.3BZ24.011)

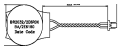
LBL6
LABEL
(R_45.3J904.011)

LBL5
LABEL
(R_40.3BZ24.001)

MB serial NO# and MAC address
40.3BZ24.011 -> 30 x 15mm
40.3KP03.011 -> 35 x 15mm
45.41107.021 -> 70 x 8mm
CARD
45.ACA01.0C1 -> 32 x 7mm
MIC CARD
45.41109.001 -> 20 x 5mm



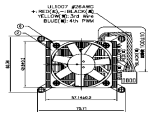
BAT2
BATTERY BR2032_60MM
(R_23.24220.612)
Wire Length:60mm
耐高溫>85C
Vendor
P/N:
23.21208.061
23.24220.612



BAT1
BATTERY CR2032_30MM
(23.21221.024)
Wire Length:30mm

Vendor
P/N:
23.21221.024
23.21212.031

HeatSink+FAN Symbol



HSFAN1
(R_60.3KN01.001)

Vendor
P/N:

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Stand off&EMI Cap&DUMMY BOM

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 65 of 107

USB3 Charger

USB30_RX_CON_N1 → USB30_RX_CON_N1 34, USB30_RX_CON_P1 → USB30_RX_CON_P1 34

USB30_TX_CON_N1 → USB30_TX_CON_N1 34, USB30_TX_CON_P1 → USB30_TX_CON_P1 34

USB_CON_PN1 → USB_CON_PN1 34, USB_CON_PP1 → USB_CON_PP1 34

Card Reader

16 USB_PCH_PP9

16 USB_PCH_PN9

Audio

30 HP_OUT_R_CON

30 HP_OUT_L_CON

28,30,95 JD_LOT

30 MIC_IN_L_JK

30 MIC_IN_R_JK

27 MIC_IN_JD

BTNBD

15 OBR

64 PWRBTN#

64 PWRLED_CON

64 SUSLED_CON

64 HDD_LED_CON

HDD/LAN LED

24 LAN_LED3_CTRL

31,32,97 LAN_LINKACTIVITY_LAN_N

ON/OFF

64,95 PANEL_SW

BRIGHTNESS

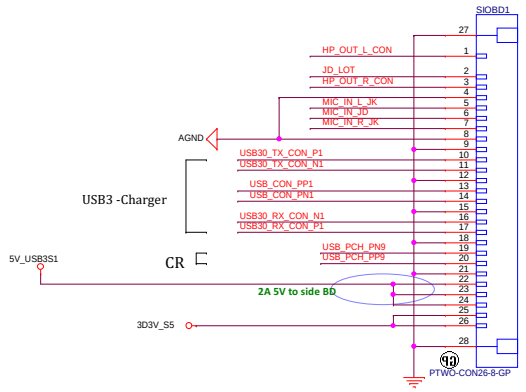
24 BRIGHTNESS_N

64 HD_LED_PWR_EMI → HD_LED_PWR_EMI

Side IO BD

2012/09/03

FFC1 (CR, USB3, Audio) 26pin



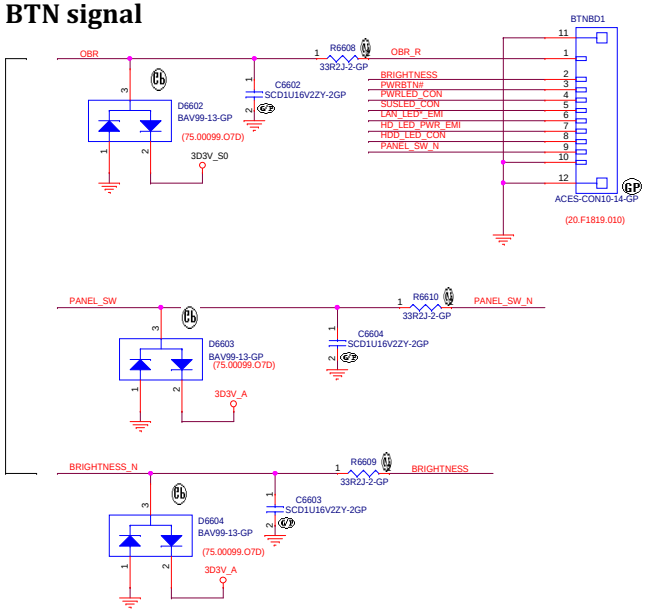
2013/04/21

Rossi delete FFC2

Button BD

OBR / BTN signal

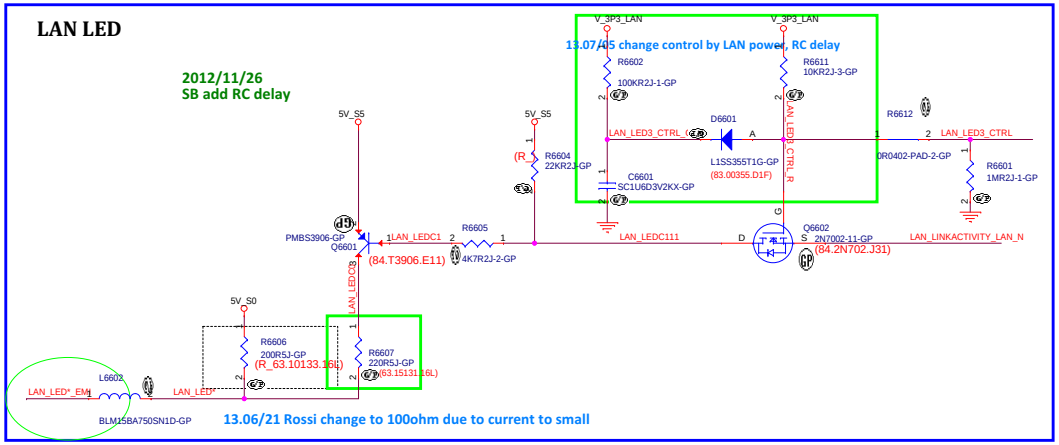
To PCH



LAN LED

2012/11/26

SB add RC delay



<Core Design>

wistron

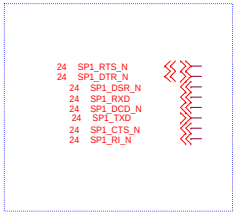
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: IO Board

Size: C | Document Number: Consumer AIO Woody | Rev: SA

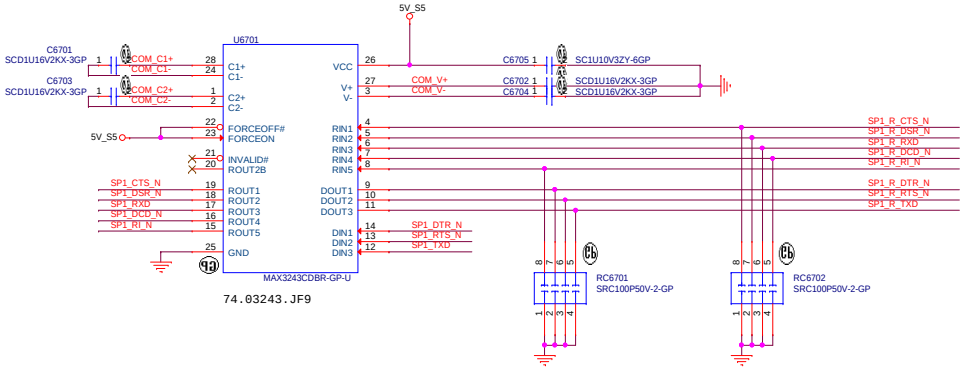
Date: Thursday, November 26, 2015 | Sheet 66 of 107

COM Port



2014/9/30-SA Vita
change COM2 power to +5V_AUX2

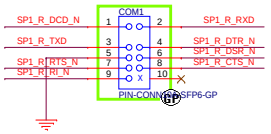
SERIAL PORT



74.03243.JF9

COM port header

13.07/05 Change comport to 2.0 pitch type



2014/8/7
change COM2 to 21.62884.205

2014/12/18-SB Vita
Change COM2 front header naming to COM1

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

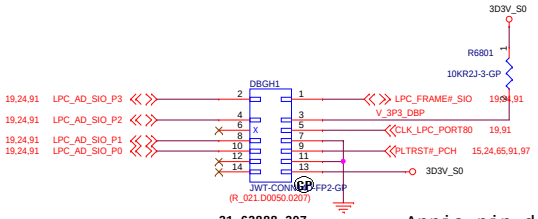
Title: COM

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 67 of 107

80 port

Layout close to SIO



21.62888.207

Annie pin define

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Debug

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 68 of 107

<Core Design>

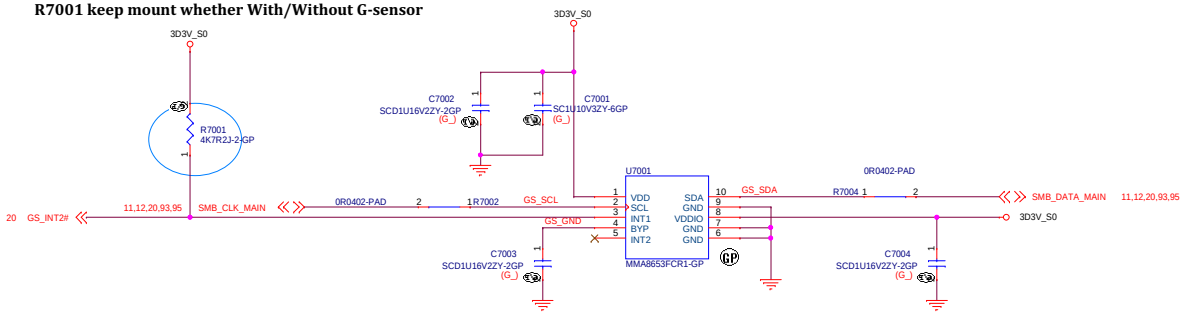
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LPT_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 69 of 107

R7001 keep mount whether With/Without G-sensor



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: G sensor

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 70 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 71 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 72 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 73 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 74 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 75 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 76 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 77 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 78 of 107

(R)

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: 5A

Date: Thursday, November 26, 2015 | Sheet 79 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 80 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 1&2_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 81 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 3&4_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: 5A

Date: Thursday, November 26, 2015 | Sheet 82 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 5&6_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: 5A

Date: Thursday, November 26, 2015 | Sheet 83 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 7&8_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 84 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU CORE_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 85 of 107

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU discrete power_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 86 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Switch

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 87 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Switch

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 88 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Others

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 89 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: NFC

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 90 of 107

19,24,68 LPC_FRAME#_SIO — LPC_FRAME#_SIO

19,68 CLK_LPC_PORT80 — CLK_LPC_PORT80

15,24,65,68,97 PLTRST#_PCH — PLTRST#_PCH

19,24,68 LPC_AD_SIO_P3 — LPC_AD_SIO_P3

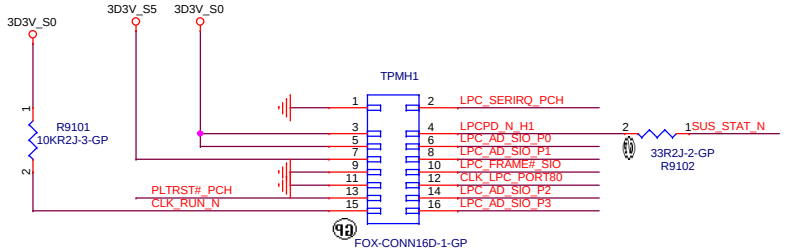
19,24,68 LPC_AD_SIO_P2 — LPC_AD_SIO_P2

19,24,68 LPC_AD_SIO_P1 — LPC_AD_SIO_P1

19,24,68 LPC_AD_SIO_P0 — LPC_AD_SIO_P0

19 SUS_STAT_N

19,24 LPC_SERIRQ_PCH



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: TPM

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 91 of 107

Reserved

<Core Design>

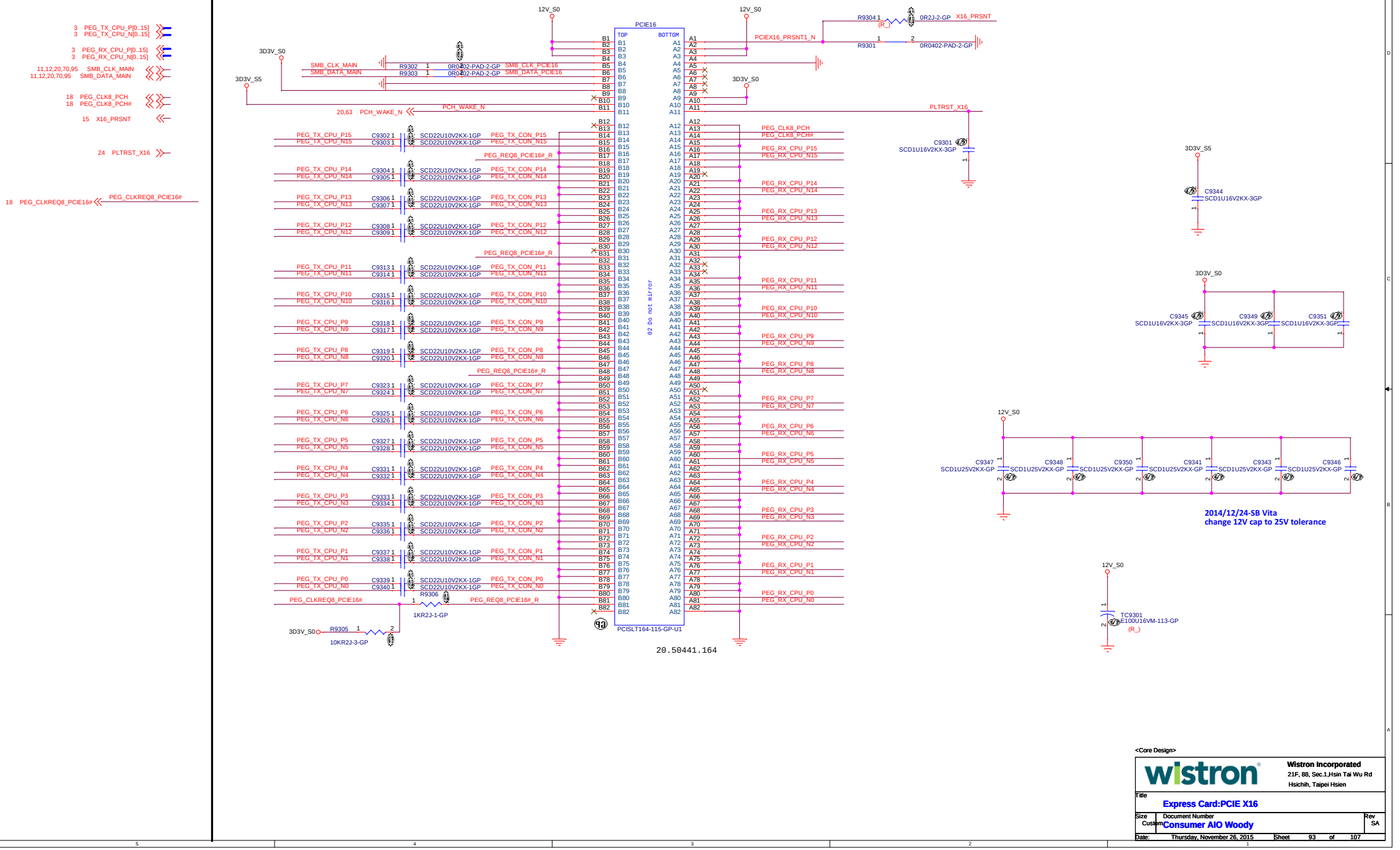
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PS2_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 92 of 107



20.50441.164

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Express Card:PCIE X16

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 93 of 107

Reserved

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Smart Card_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 94 of 107

SSID = Scalar

Audio Out

LVDS-OUT

DMMI-IN

COMRTOL

cDP-IN 20122018 Ryan

PC_MONITOR_SW

According to the IR decode or side key value to switch the satus of monitor mode and PC mode

Panel On Off CTRL

BEAD 要30ohm@100MHz(1A)

如果有使用OD，建議在這邊放10uF(MLCC)

Main EEPROM

Shielding

Need Check

Michael 2012/2/6

EEPROM for OSD

72.24C16.Y01. ATMEL
72.02416.B01. ST

LCD ON/OFF

Pin 118
PW ON Latch功能選項
Internal MCU :Pull High
External MCU :Pull Low

20130930 vender suggest

B-EVEN

A-ODD

Remove

SB add

20150115 Ryan

To AMP

Monitor mode

Monitor	DET_HDMI#	SCALAR_EN	Panel EN/PWM/CTRL
	0	1	Active

DET_HDMI# : connect to SIO and Scalar

To SIO: make scalar workable -> Scalar_EN 1(From SIO)

To Scalar: let scalar know HDMI IN, and make related signal active, Panel and AMP

20150409 swap HDMI PIN

HDMI side:
HDMI0 => RX2 pair
HDMI1 => RX1 pair
HDMI2 => RX0 pair
HDMICK => RC pair

Prevent leakage

Firmware update by SMBUS

Michael 2011/12/01
PC Mode + DVI使用SIO + 4個被用 3D3V_S0

SMBUS_ISP H : Simutaneous Mode
SMBUS_ISP L : Isolate Mode

Michael 2012/3/8 -A
R3205 is add for tune equal length

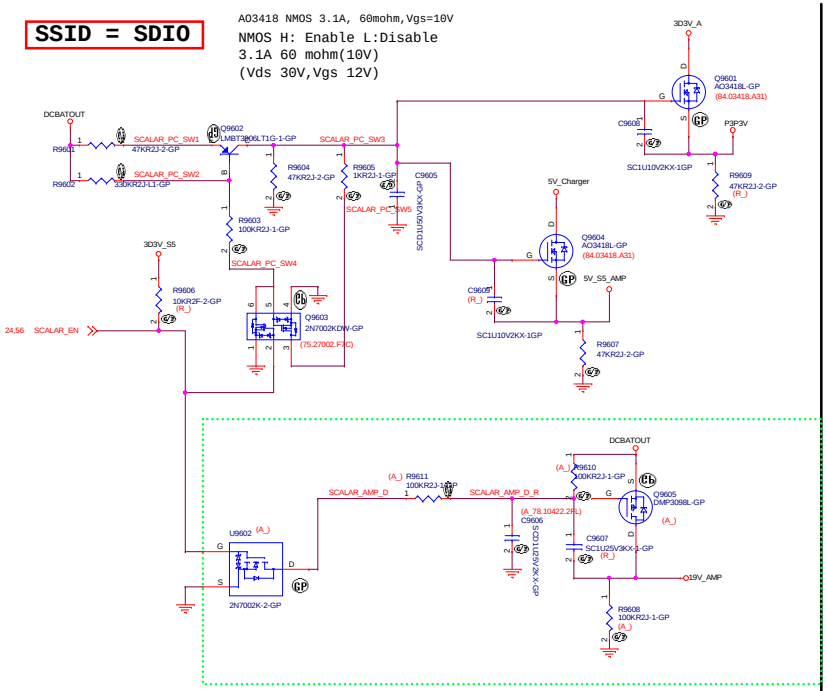
20150127 add 2N7002 logic for leakage

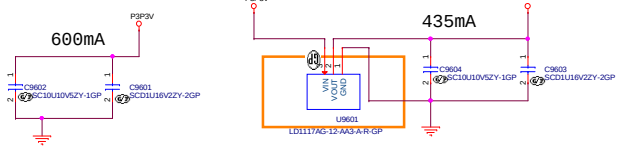
wistron
Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Scaler-RTD2486VRD
Size: C
Document Number: Consumer A/D Woody
Rev: 0A
Date: Thursday, November 29, 2012
Sheet: 66 of 107

SSID = SDIO

AO3418 NMOS 3.1A, 60mohm,Vgs=10V
NMOS H: Enable L:Disable
3.1A 60 mohm(10V)
(Vds 30V,Vgs 12V)





Scalar Spec Table

	GPI input	From	High	Low	Default
Pin69	GPI-1 PC Power ON → PM_SLP_S3# 20,24,34,40,41,49,50,95	SB	PC	Monitor	Monitor
Pin109	GPI-2 Mode change/ Panel OnOff	SW	Normal	Touch	PC: PC (PC->HDMI) Monitor: HDMI, VGA (HDMI)

GPO output

Pin55	GPO-2 Panel On/OFF → SCALAR_VDD_EN 55,95	Scalar	ON	OFF	PC: ON Monitor: Detect Signal
Pin104	GPO-3 PC/Monitor → PC_MONITOR_SW 28,95	Scalar	PC	Monitor	PC: PC, Monitor: HDMI, VGA
Pin101	GPO-5 Video → BLON_EN# 55,95	Scalar	Disable	Enable	Disable
	Delete AMP mute circuit, the mute function change to EC --Kai 0308				

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Scalar Power
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA
Date: Thursday, November 26, 2015 | Sheet 98 of 107

PCIE

18,31 PEG_CLK2_LAN
18,31 PEG_CLK2_LAN#
16,31 PCIE_TX_LAN_P5
16,31 PCIE_TX_LAN_N5
16,31 PCIE_RX_LAN_P5
16,31 PCIE_RX_LAN_N5

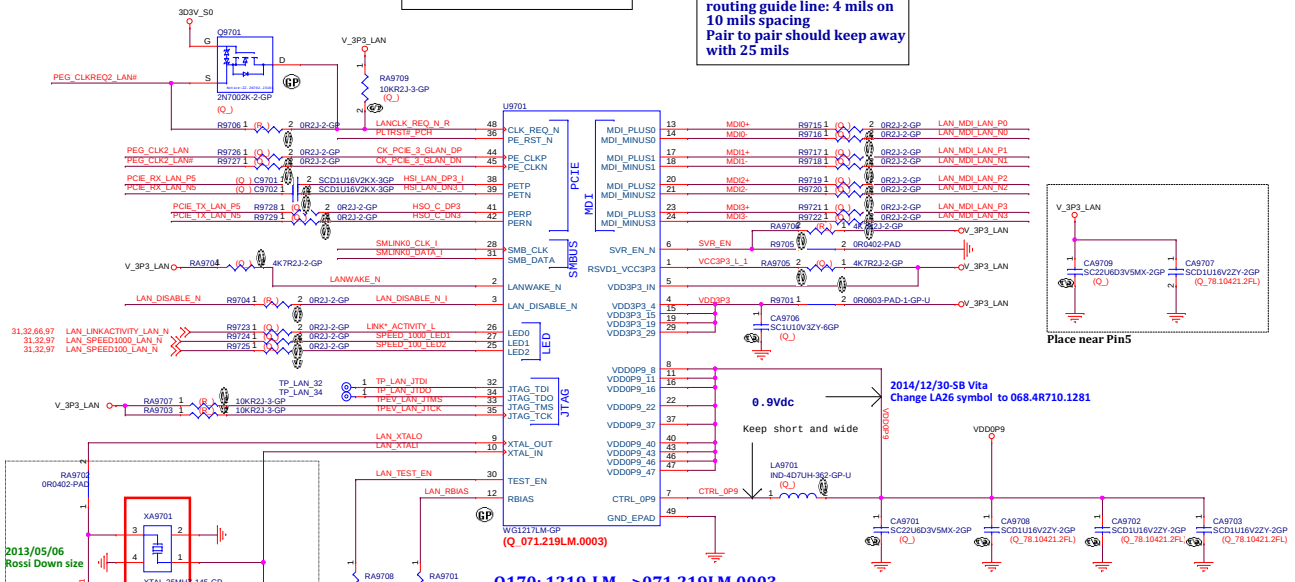
OTHERS

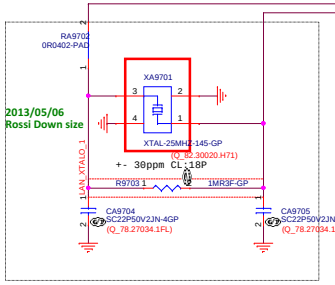
20 LAN_DISABLE_N
20 SMLINK0_CLK
20 SMLINK0_DATA
15,24,65,68,91 PLTRST#_PCH
24,31 LANWAKE_N
18,31 PEG_CLKREQ2_LAN#

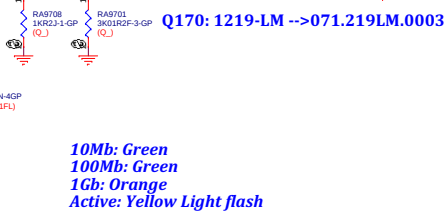
31,32 LAN_MDI_LAN_P0
31,32 LAN_MDI_LAN_N0
31,32 LAN_MDI_LAN_P1
31,32 LAN_MDI_LAN_N1
31,32 LAN_MDI_LAN_P2
31,32 LAN_MDI_LAN_N2
31,32 LAN_MDI_LAN_P3
31,32 LAN_MDI_LAN_N3
31,32,97 LAN_SPEED1000_LAN_N
31,32,97 LAN_SPEED100_LAN_N
31,32,66,97 LAN_LINKACTIVITY_LAN_N
24,62 LAN_EN_PWR_SIO

If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,the CLK_REQ_N pull-up resistor should be connected to +V3.3S.

LAN_MDI_P / LAN_MDI_N routing guide line: 4 mils on 10 mils spacing
Pair to pair should keep away with 25 mils





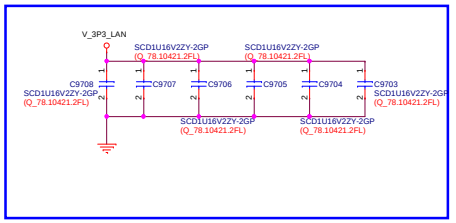


10Mb: Green
100Mb: Green
1Gb: Orange
Active: Yellow Light flash

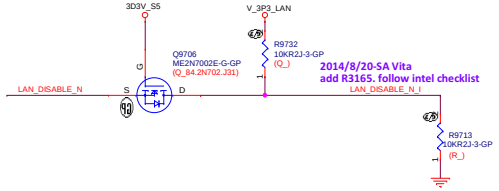
0.9Vdc POWER OPTIONS

Internal SRV	Shared with PCH's 1.05V SVR
LA36 : STUFF	LA36 : NO STUFF
RA1020 : NO STUFF	RA1020 : STUFF
R968 : STUFF	R968 : NO STUFF
RA886 : NO STUFF	RA886 : STUFF

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply (example sharing from PCH's 1.05V SVR). When sharing, make sure the 1.05V_SHARED is controlled by the SLP_LAN signal. Both +3.3V_LAN and 1.05V_SHARED rails are remained powered on during ALL Sx states, as required to support WOL.

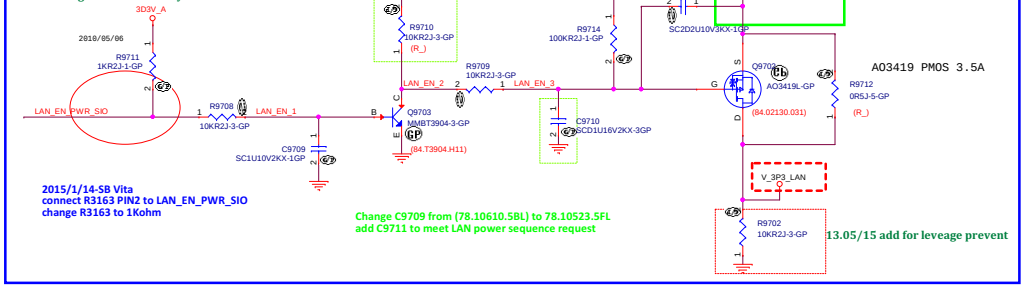


2015/3/19-1A Vita
add Q39, R9825 to control WOL under EUP

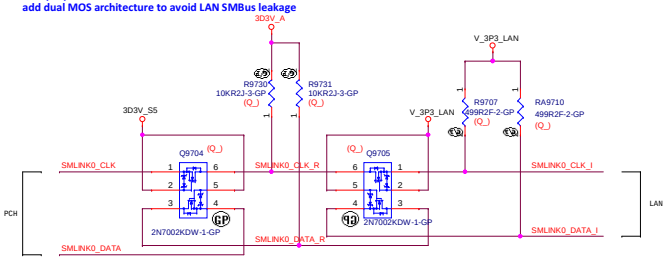


LAN Power

Mount LAN PWR delay circuit --> Verify SA
BOM change for control delay--> 0703



2014/12/31-SB Vita
add dual MOS architecture to avoid LAN SMBus leakage



<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Inter LAN
Size: Custom
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 97 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LAN Switch_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 98 of 107

2015/11/18 Rossi
Remove XDP connector

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
XDP&ITP

Size
A

Document Number
Consumer AIO Woody

Rev
SA

Date: Thursday, November 26, 2015

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Table of Content

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 100 of 107

(R)

<Core Design>

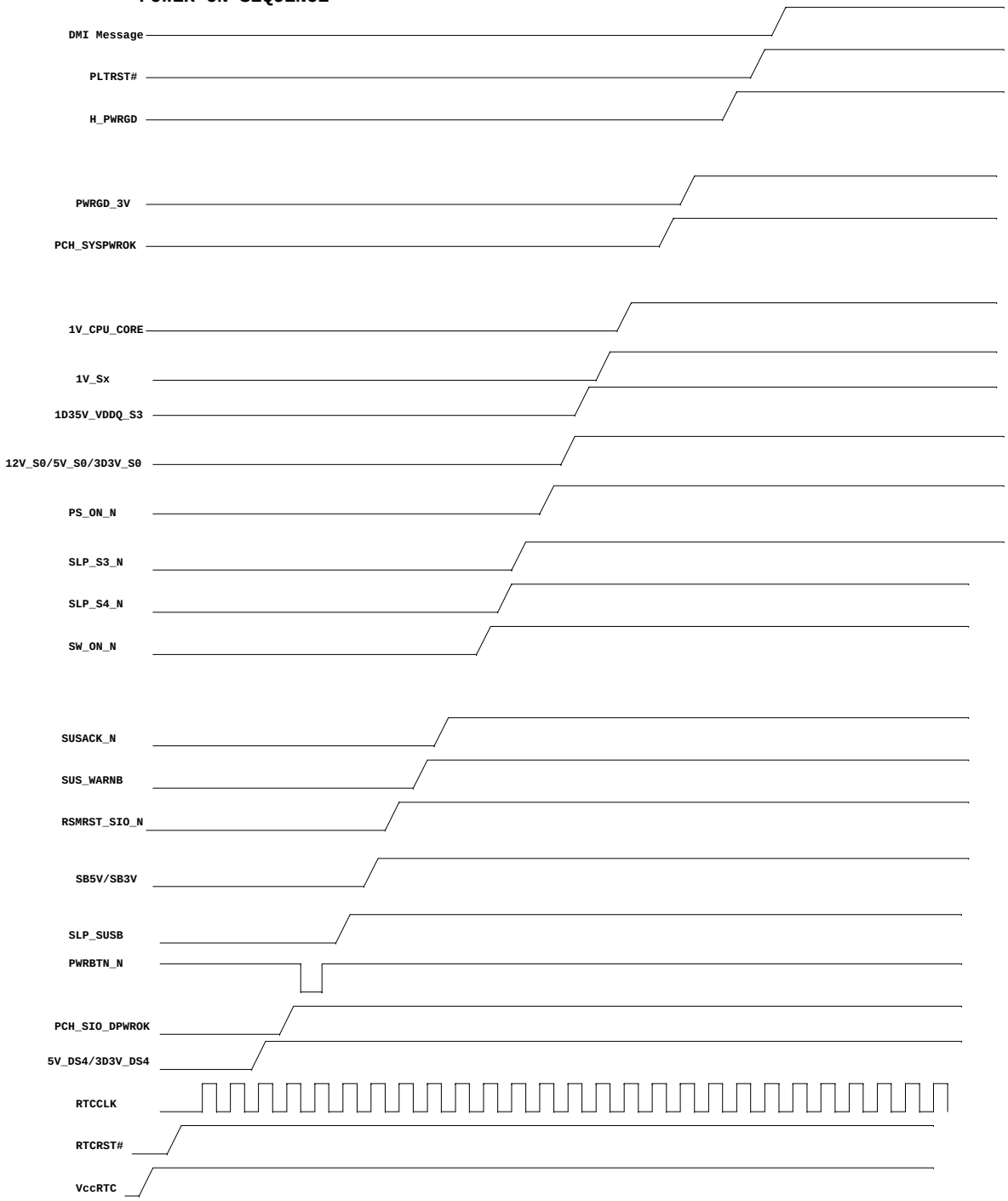
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPIO table

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 101 of 107

POWER ON SEQUENCE



<Core Design>

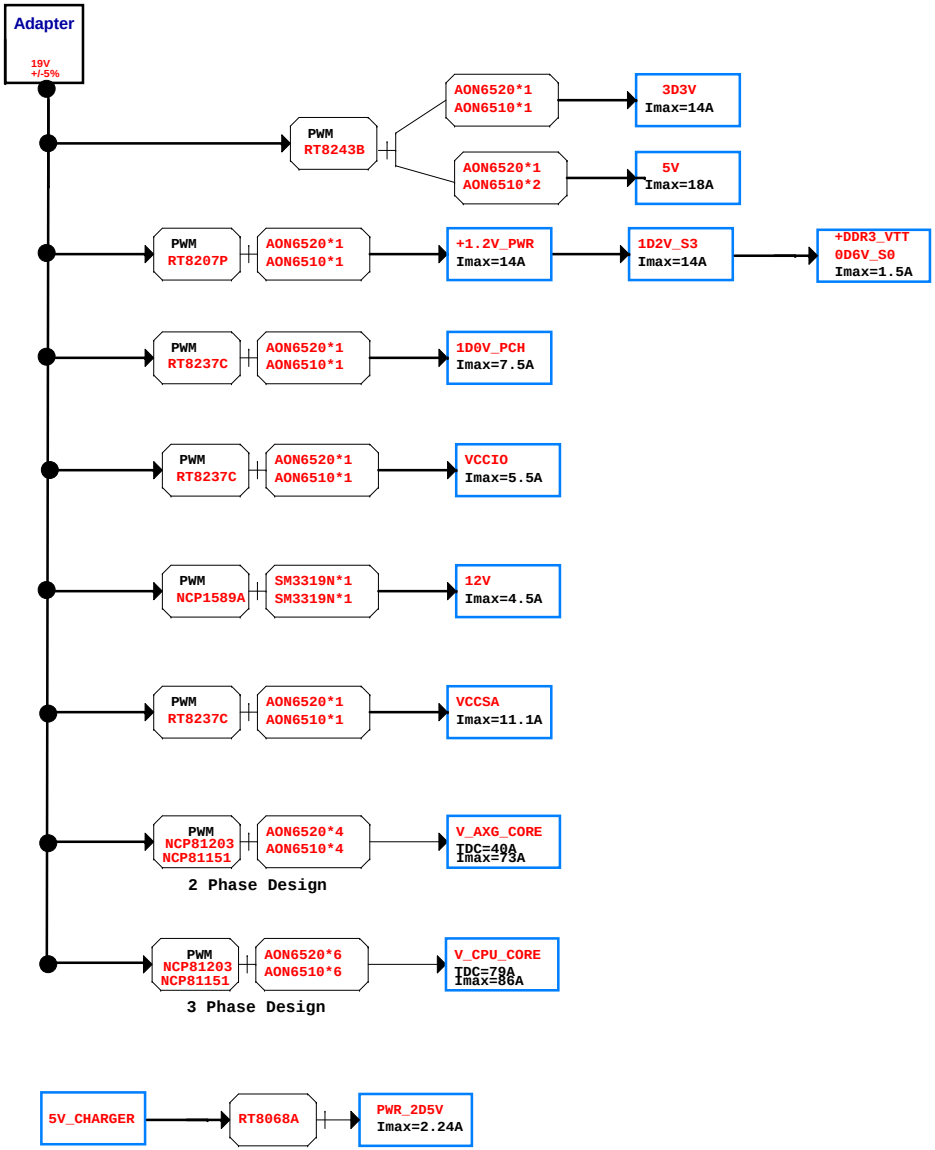
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Power sequence

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 102 of 107



<Core Design>

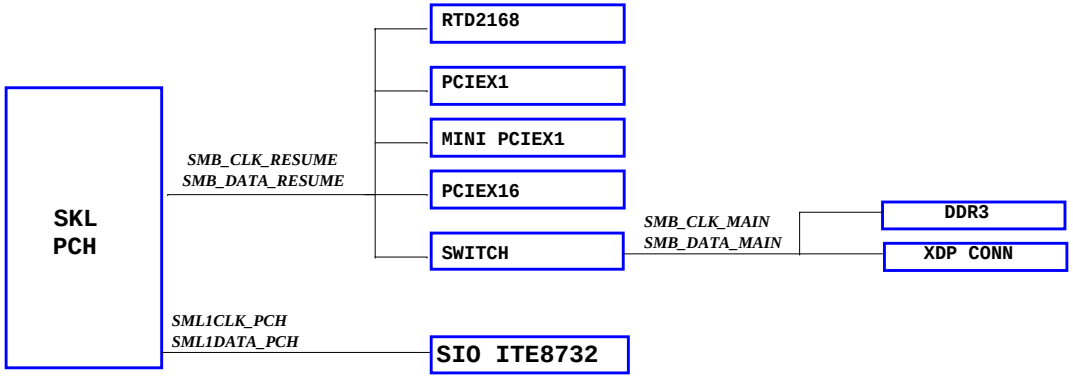
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Power Block Diagram

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 103 of 107



<Core Design>

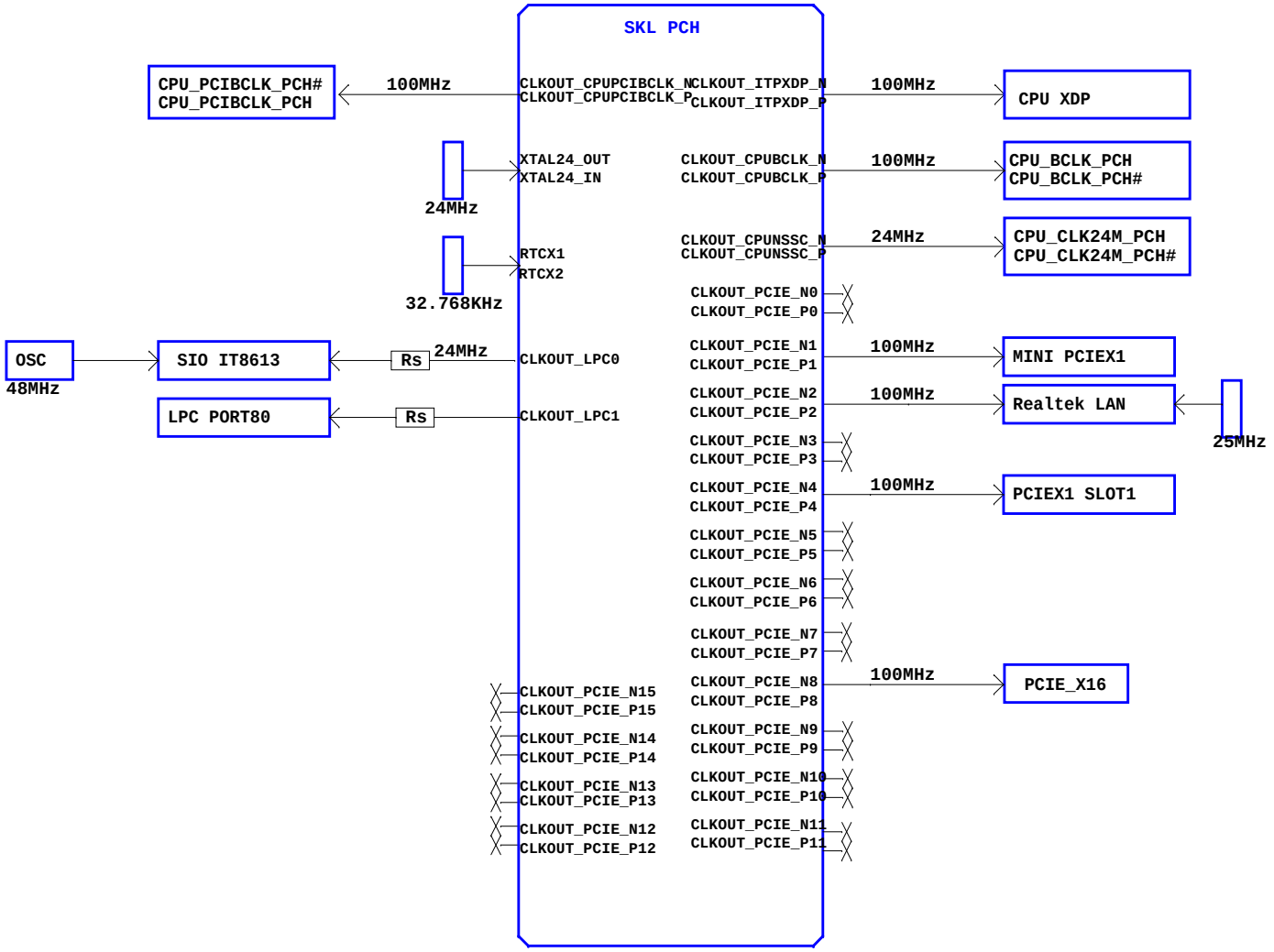
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: SMBUS Block Diagram

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 104 of 107



<Core Design>

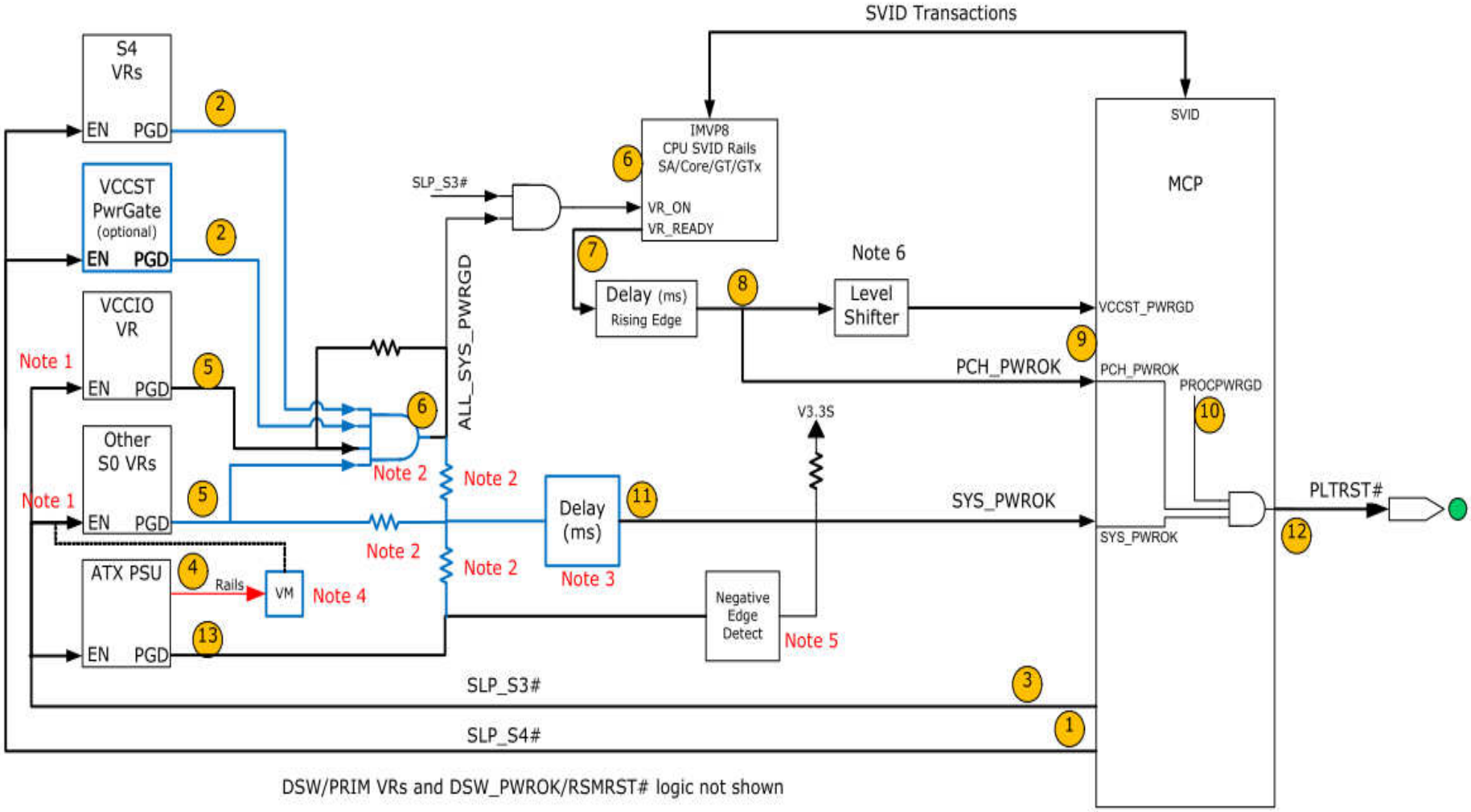
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Clock MAP

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 105 of 107



<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: RESET Flow Chart		
Size: C	Document Number: Consumer AIO Woody	Rev: SA
Date: Thursday, November 26, 2015	Sheet 106 of 107	

(R)

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Change History

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 107 of 107