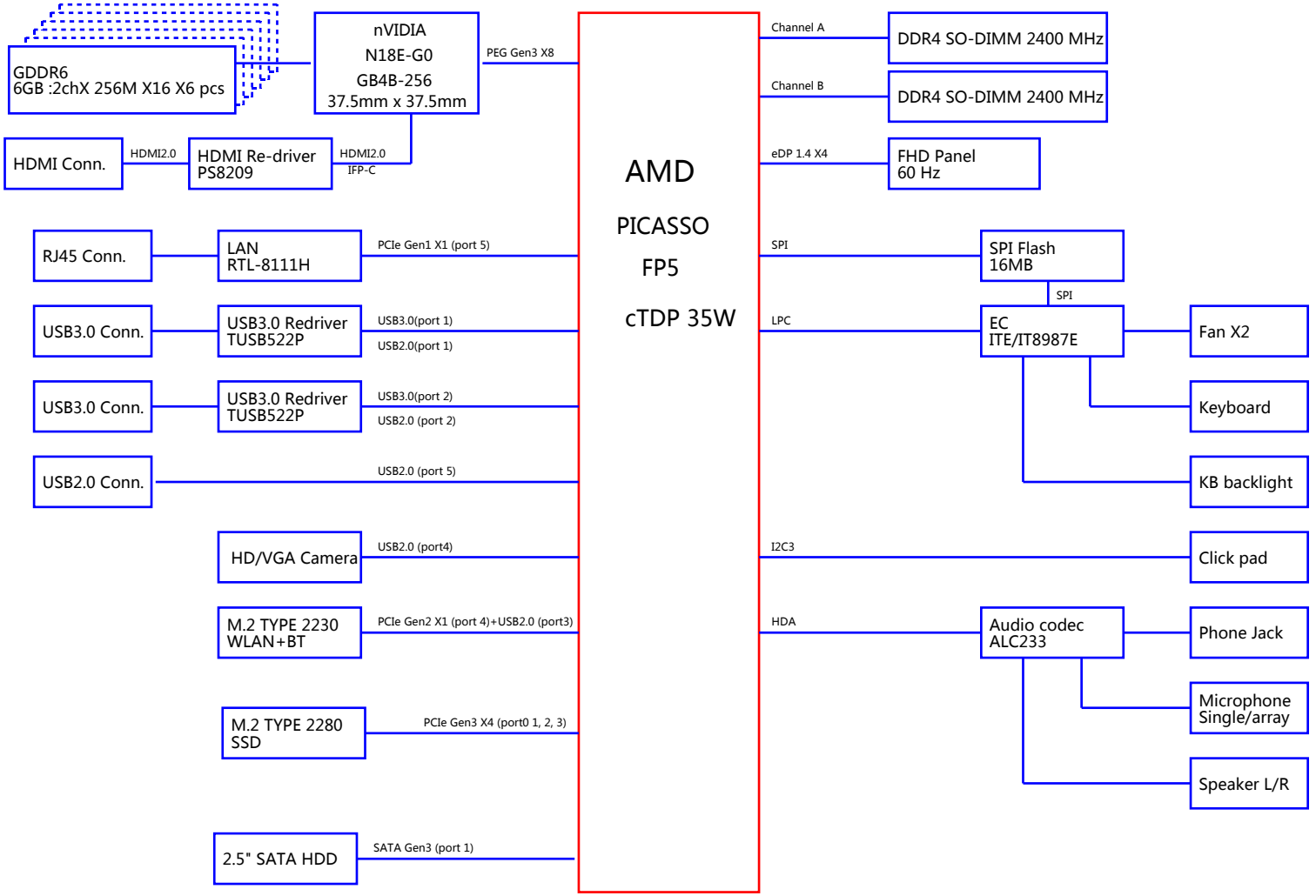
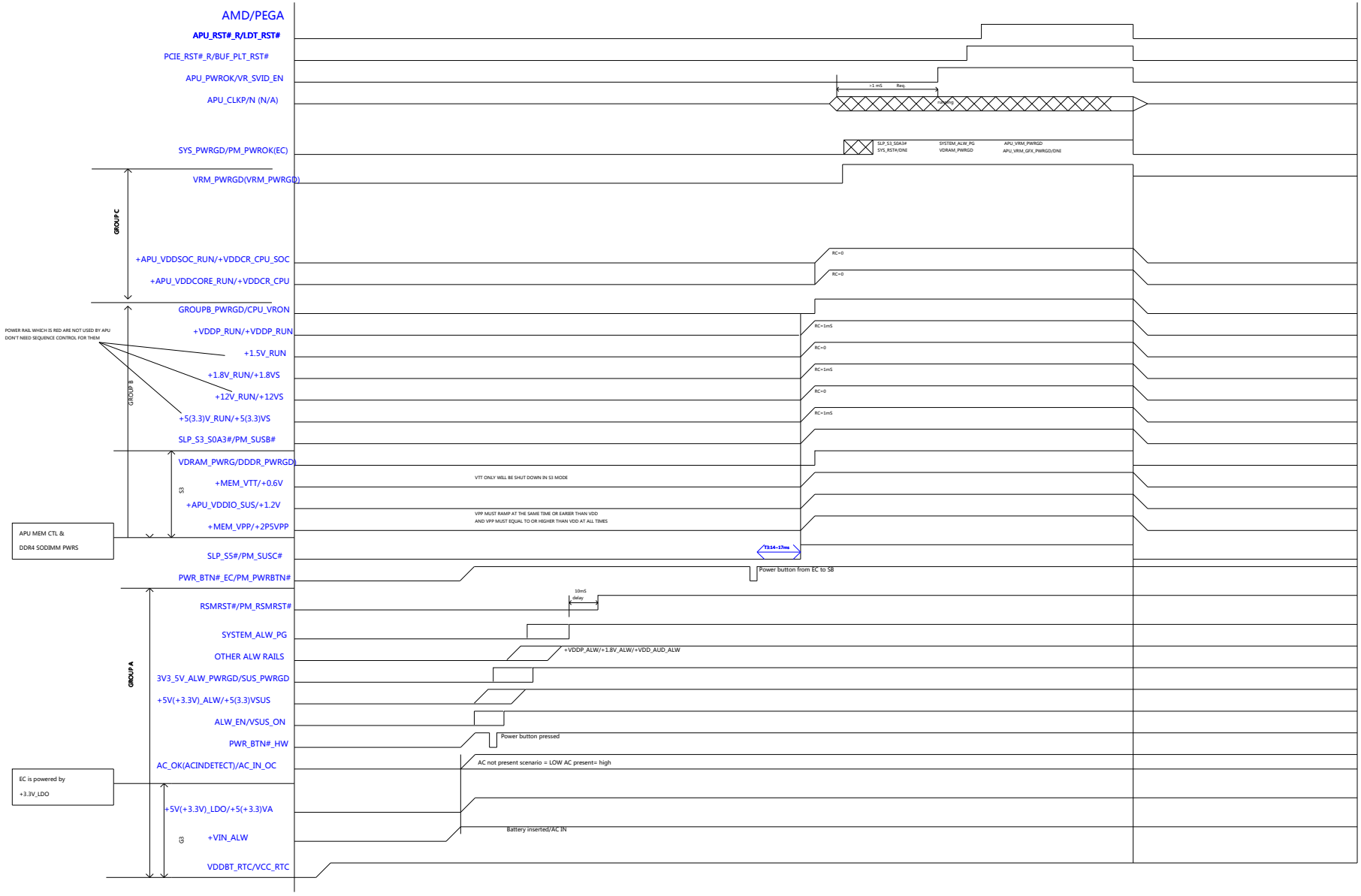
FX505DU Block Diagram



Power

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
RG1-HW3 RD

Title : Block Diagram
Engineer: Johnson Huang
Size: C | Project Name: FX505DU | Rev: 1.1
Date: Tuesday, March 12, 2019 | Sheet 1 of 99



PEGATRON PROPRIETARY AND CONFIDENTIAL

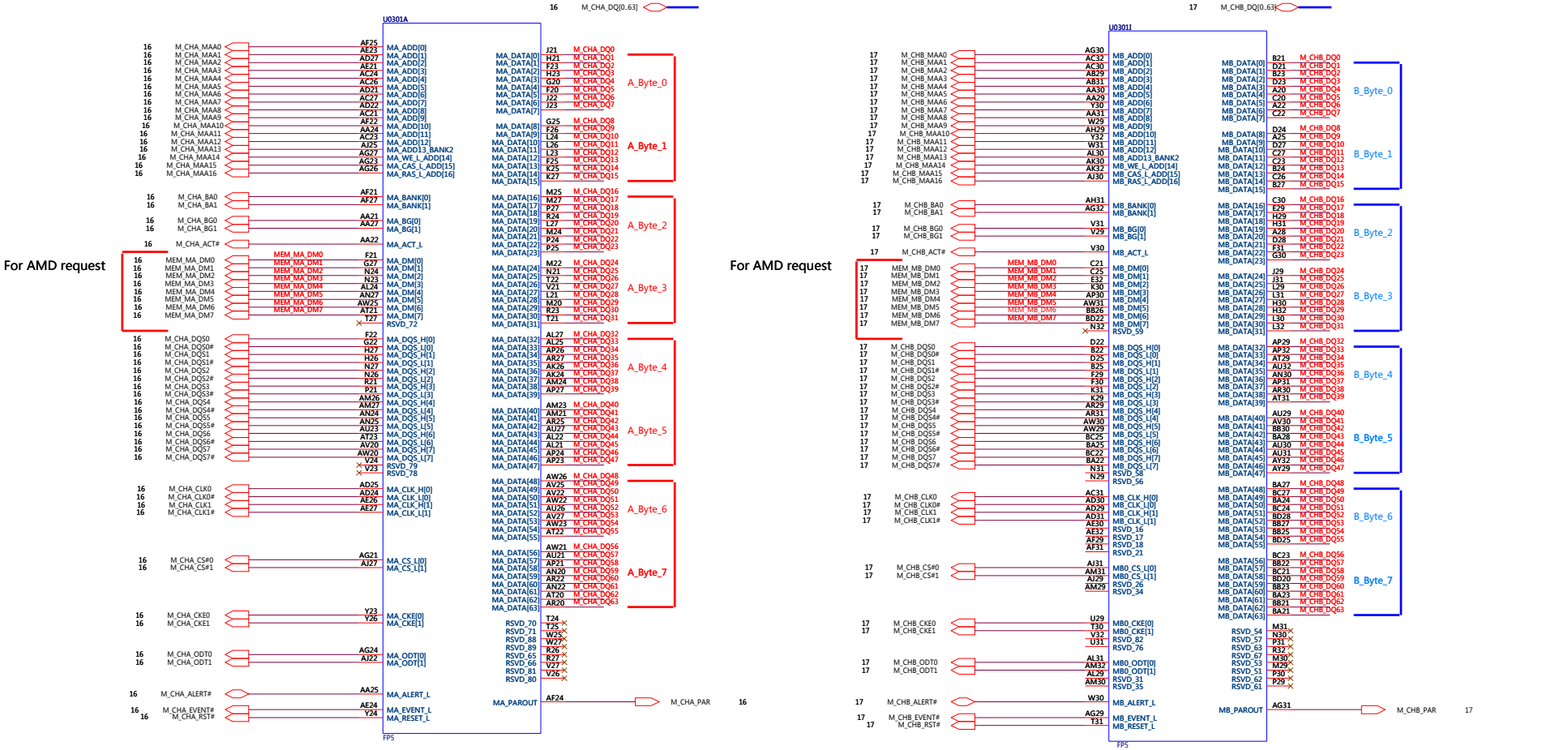
Title : Option

BG1-HW3 RD

Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.1

Date: Tuesday, March 12, 2019 Sheet 2 of 72



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

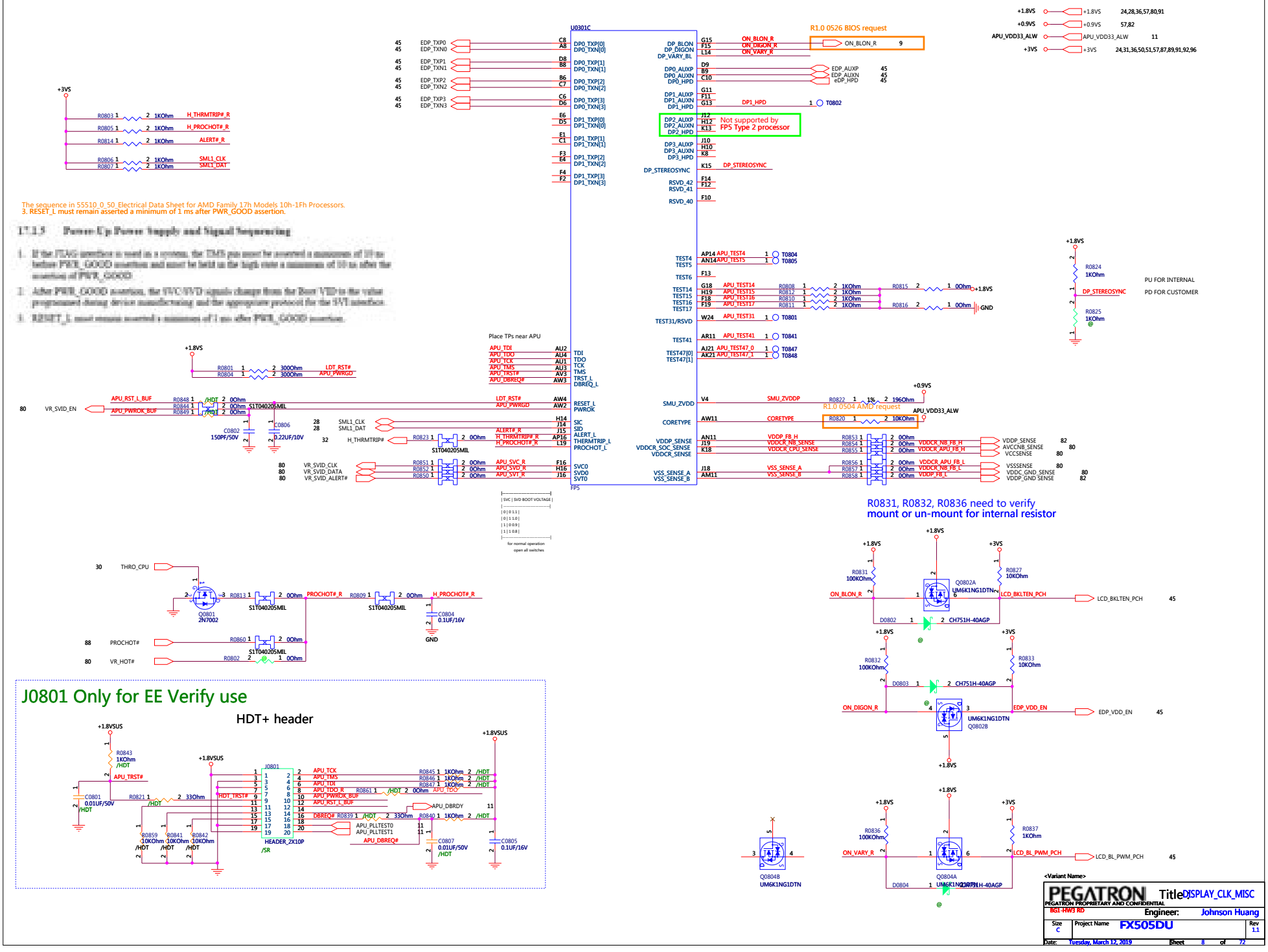
BG1-HW3 RD

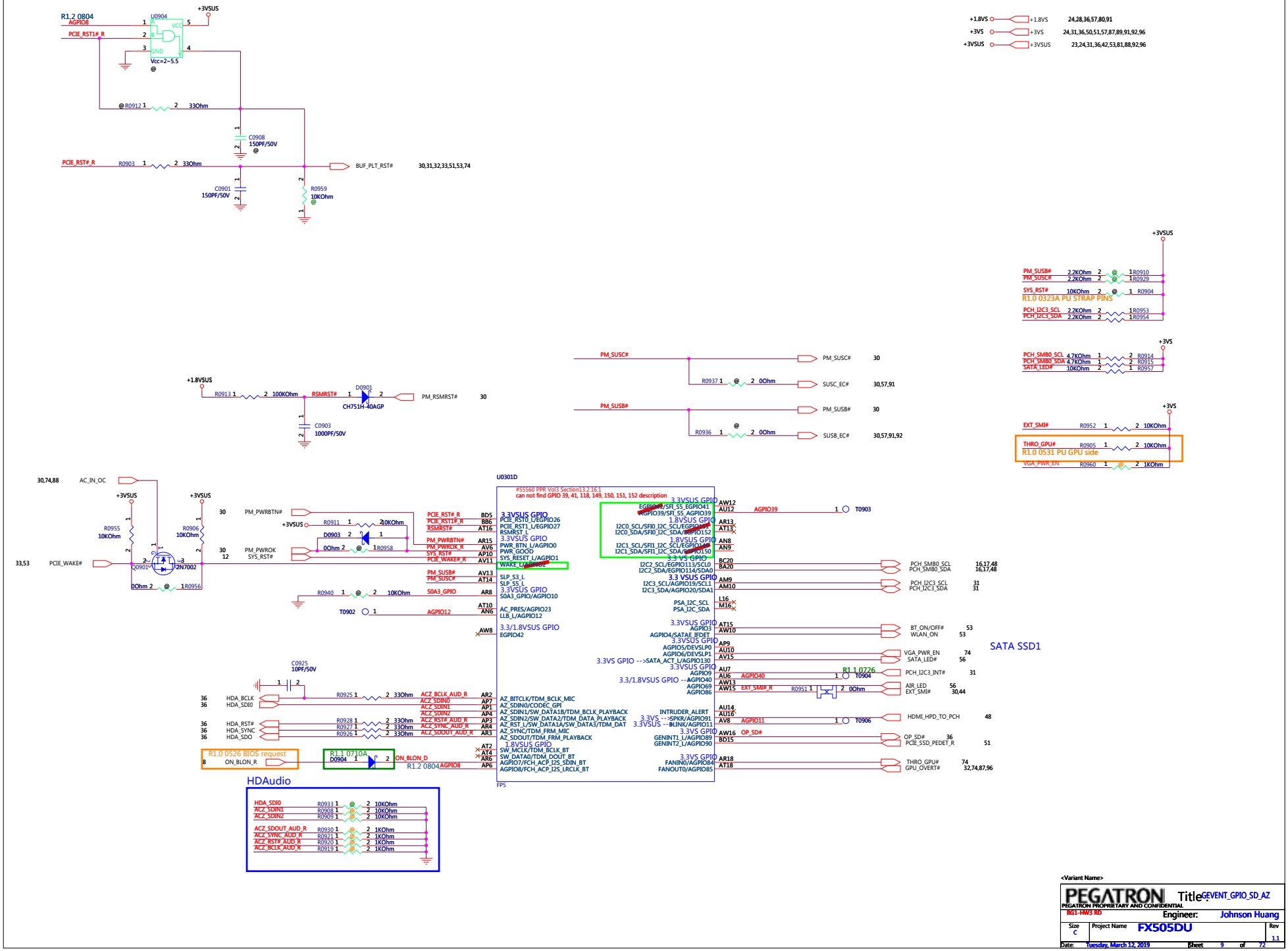
Title : MEM & PCIE I_F

Engineer:

Size	Project Name	Rev
C		1.1

Date: Tuesday, March 12, 2019 Sheet 7 of 72


U0301C
R1.0 0526 BIOS request
ON_BLON_R
Not supported by FPS Type 2 processor
DP_STEREOSYNC
Place TPs near APU
R1.0 0504 AMD request
APU_VDD33_ALW
PU FOR INTERNAL
PD FOR CUSTOMER
R0831, R0832, R0836 need to verify
mount or un-mount for internal resistor
J0801 Only for EE Verify use
HDT+ header
HEADER_2X10P
Q0801 2N7002
Q0802A UM6K1NG1DTN
Q0802B UM6K1NG1DTN
Q0804A UM6K1NG1DTN
Q0804B UM6K1NG1DTN
D0802 CH751H-40AGP
D0803 CH751H-40AGP
D0804 CH751H-40AGP
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title DISPLAY_CLK_MISC
Engineer: Johnson Huang
FX505DU
Tuesday, March 12, 2019
Sheet 8 of 72



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

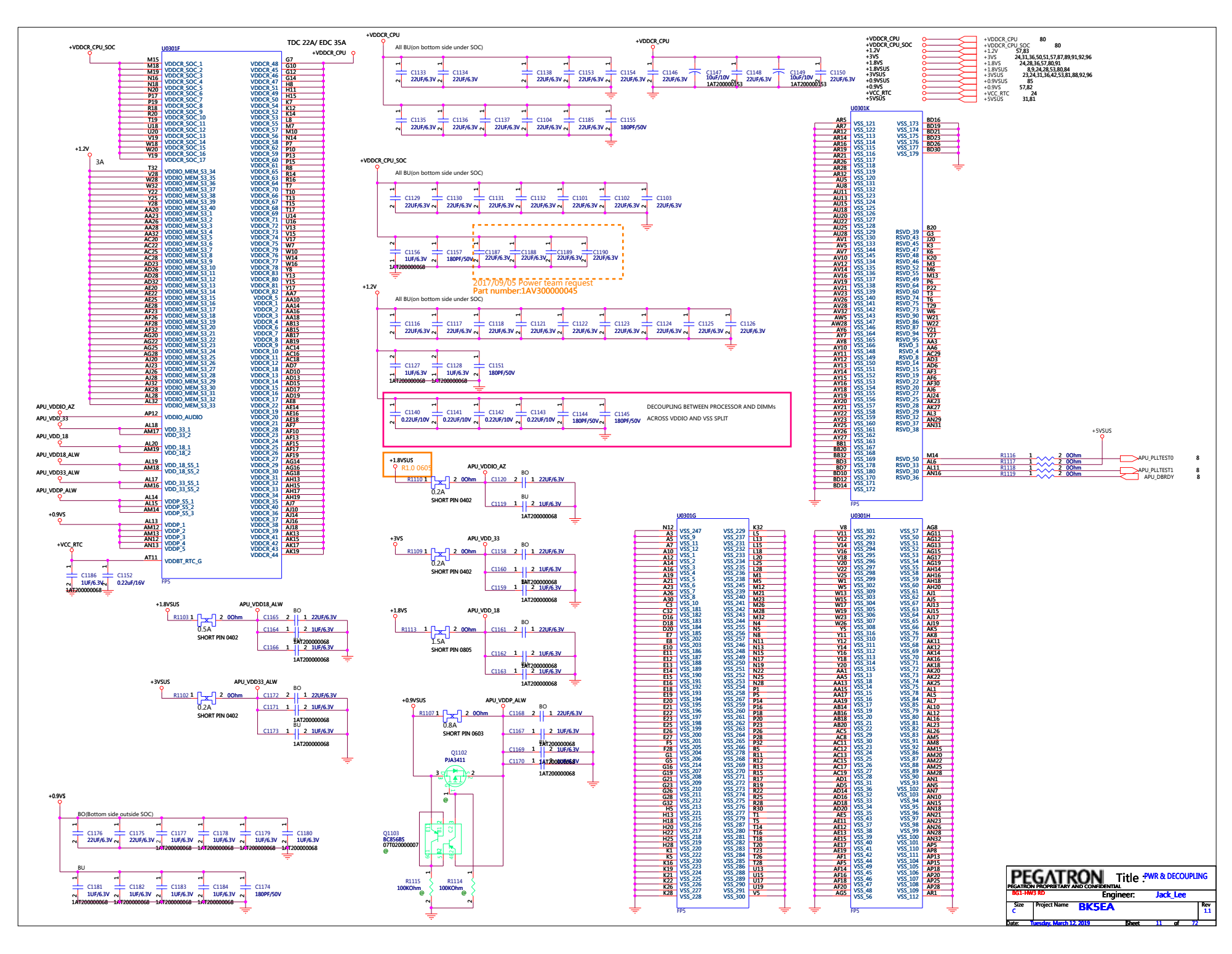
Title: GEVENT_GPIO_SD_AZ

BG1-HW3 RD

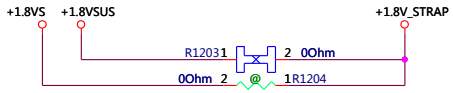
Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.1

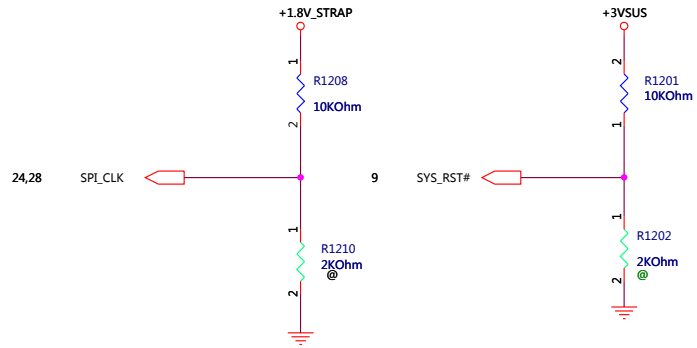
Date: Tuesday, March 12, 2019 Sheet 9 of 72


TDC 22A/ EDC 35A
U0301F
U0301K
U0301G
U0301H
All BU(on bottom side under SOC)
BO(Bottom side outside SOC)
BU
DECOUPLING BETWEEN PROCESSOR AND DIMMs
ACROSS VDDIO AND VSS SPLIT
2017/09/05 Power team request
Part number:1AV300000045
SHORT PIN 0402
SHORT PIN 0805
SHORT PIN 0603
PJA3411
BC856BS
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PWR & DECOUPLING
Engineer: Jack_Lee
Project Name BK5EA
Size C
Rev 1.1
Date: Tuesday, March 12, 2019
Sheet 11 of 72

+1.8VSUS +1.8VSUS 8,9,24,28,53,80,84
+1.8VS +1.8VS 24,28,36,57,80,91
+3VSUS +3VSUS 23,24,31,36,42,53,81,88,92,96



STRAP PINS



STRAP	FUNCTION	DEFINITION
SPI_CLK		1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

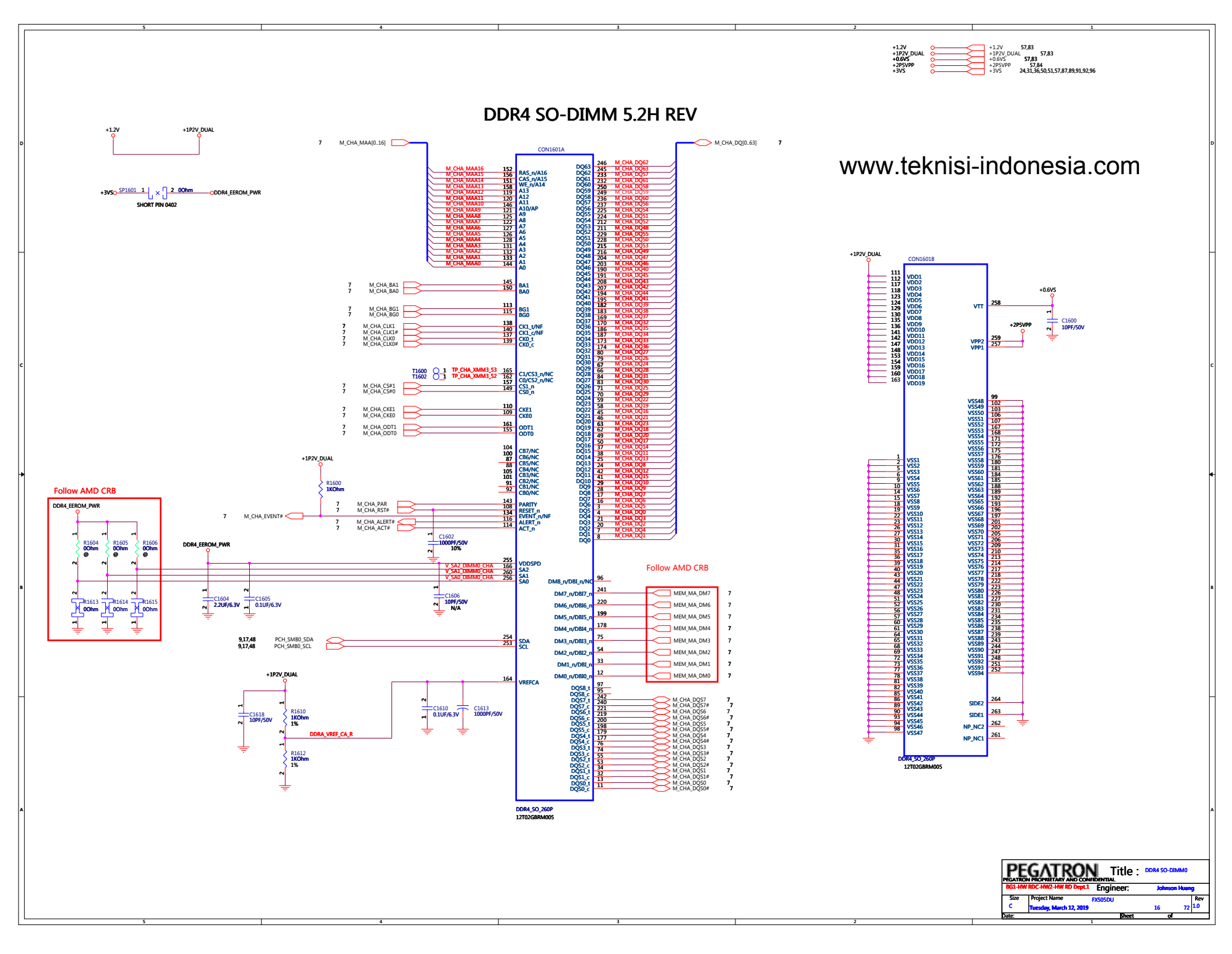
PEGATRON Title : STRAPS, SOCKET, HS

BG1-HW3 RD Engineer: Johnson Huang

Size B | Project Name FX505DU | Rev 1.1

Date: Tuesday, March 12, 2019 Sheet 12 of 72

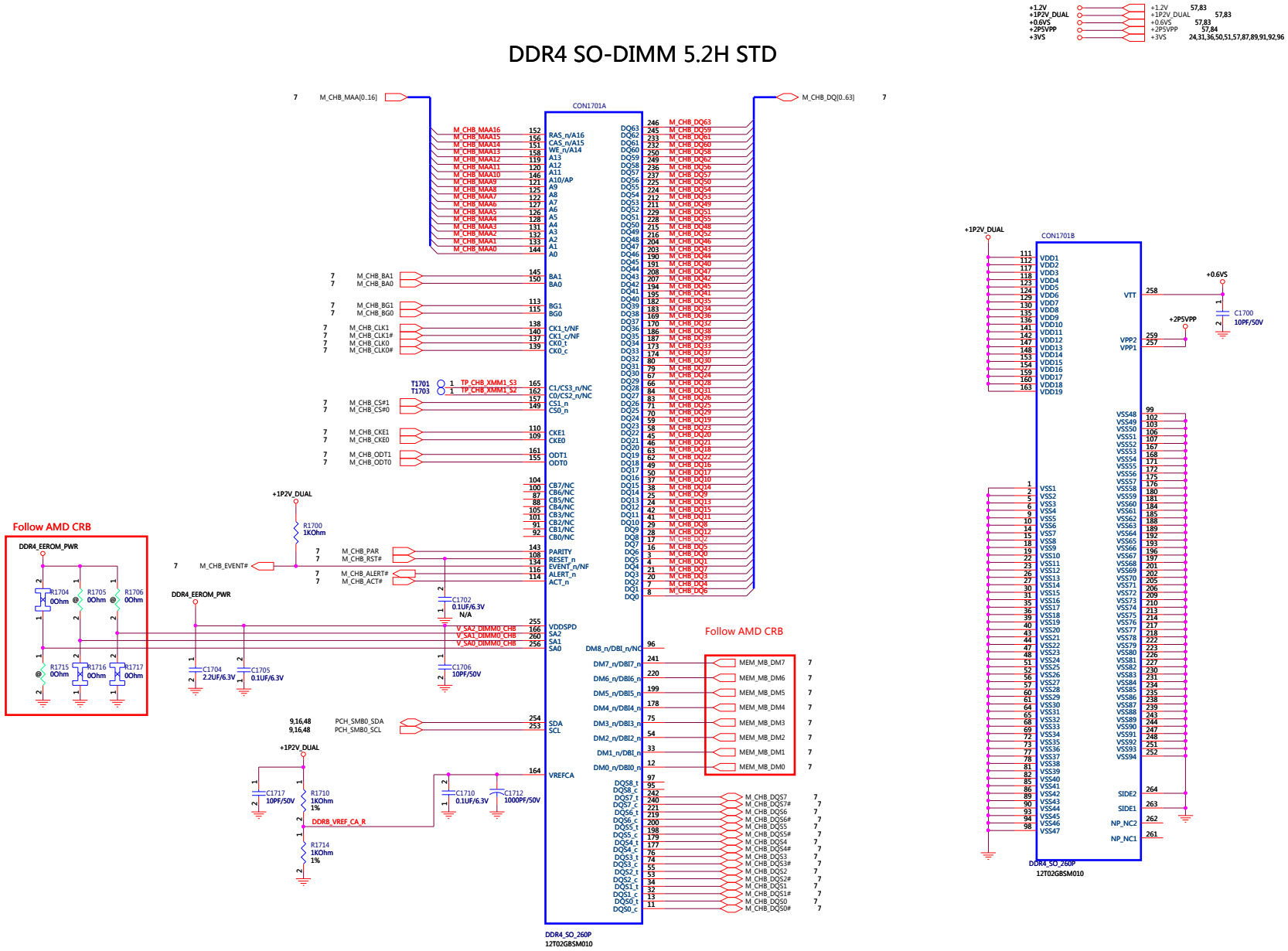
DDR4 SO-DIMM 5.2H REV



+1.2V	+1.2V	57,83	
+1P2V_DUAL	+1P2V_DUAL	57,83	
+0.6VS	+0.6VS	57,83	
+2P5VPP	+2P5VPP	57,84	
+3VS	+3VS	24,31,36,50,51,57,87,89,91,92,96	

PEGATRON	Title :	DDR4 SO-DIMM0	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.1	Engineer:	Johnson Huang	
Size: C	Project Name: FX505DU		Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet: 16	of: 72	

DDR4 SO-DIMM 5.2H STD



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DDR4 SO-DIMM1

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.0

Date: Tuesday, March 12, 2019 Sheet 17 of 72

+1.2V
+1P2V_DUAL
+0.6VS
+2P5VPP
+3VS

+1.2V 57,83
+1P2V_DUAL 57,83
+0.6VS 57,83
+2P5VPP 57,84
+3VS 24,31,36,50,51,57,87,89,91,92,96

+1P2V_DUAL

NOTE:
Place those cap close to CH A DIMM

R1.1 modify
EMC

C1805 10UF/6.3V
C1806 10UF/6.3V
C1807 10UF/6.3V
C1800 2.2UF/6.3V
C1801 2.2UF/6.3V
C1802 2.2UF/6.3V
C1803 2.2UF/6.3V
C1804 2.2UF/6.3V
C1843 0.1UF/6.3V
C1846 0.1UF/6.3V
C1851 0.1UF/6.3V
C1848 10PF/50V
C1852 2.2UF/6.3V

C1822 1UF/6.3V 0201 X5R/+/-20%
C1858 1UF/6.3V 0201 X5R/+/-20%
C1823 1UF/6.3V 0201 X5R/+/-20%
C1859 1UF/6.3V 0201 X5R/+/-20%
C1824 1UF/6.3V 0201 X5R/+/-20%
C1860 10UF/6.3V
C1825 1UF/6.3V 0201 X5R/+/-20%
C1861 10UF/6.3V
C1826 1UF/6.3V 0201 X5R/+/-20%
C1862 1UF/6.3V 0201 X5R/+/-20%
C1827 1UF/6.3V 0201 X5R/+/-20%
C1863 10UF/6.3V
C1828 1UF/6.3V 0201 X5R/+/-20%
C1864 10UF/6.3V
C1829 1UF/6.3V 0201 X5R/+/-20%
C1865 1UF/6.3V 0201 X5R/+/-20%

R1.1 modify EMC
R1.1 modify EMC
R1.1 modify EMC
R1.1 modify EMC

FX505 RF reserve @20180131

+0.6VS

C1808 2.2UF/6.3V
C1809 2.2UF/6.3V
C1818 2.2UF/6.3V
C1854 10PF/50V
C1855 2.2UF/6.3V
C1819 2.2UF/6.3V
C1820 2.2UF/6.3V
C1821 2.2UF/6.3V

NOTE:
Place those cap close to CH B DIMM

R1.1 modify
EMC

C1815 10UF/6.3V
C1816 10UF/6.3V
C1817 10UF/6.3V
C1810 2.2UF/6.3V
C1811 2.2UF/6.3V
C1812 2.2UF/6.3V
C1813 2.2UF/6.3V
C1814 2.2UF/6.3V
C1844 0.1UF/6.3V
C1845 0.1UF/6.3V
C1850 0.1UF/6.3V
C1847 10PF/50V
C1853 10UF/6.3V

R1.1 modify
EMC

C1832 1UF/6.3V 0201 X5R/+/-20%
C1866 1UF/6.3V 0201 X5R/+/-20%
C1833 1UF/6.3V 0201 X5R/+/-20%
C1867 1UF/6.3V 0201 X5R/+/-20%
C1834 1UF/6.3V 0201 X5R/+/-20%
C1868 1UF/6.3V 0201 X5R/+/-20%
C1835 1UF/6.3V 0201 X5R/+/-20%
C1869 1UF/6.3V 0201 X5R/+/-20%
C1836 1UF/6.3V 0201 X5R/+/-20%
C1870 1UF/6.3V 0201 X5R/+/-20%
C1837 1UF/6.3V 0201 X5R/+/-20%
C1871 1UF/6.3V 0201 X5R/+/-20%
C1838 1UF/6.3V 0201 X5R/+/-20%
C1872 1UF/6.3V 0201 X5R/+/-20%
C1839 1UF/6.3V 0201 X5R/+/-20%
C1873 1UF/6.3V 0201 X5R/+/-20%

FX505 RF reserve @20180131

+2P5VPP

C1840 10UF/6.3V
C1842 1UF/6.3V 0201 X5R/+/-20%
C1875 1UF/6.3V 0201 X5R/+/-20%
C1856 10PF/50V
C1857 2.2UF/6.3V
C1841 10UF/6.3V
C1849 1UF/6.3V 0201 X5R/+/-20%
C1874 1UF/6.3V 0201 X5R/+/-20%

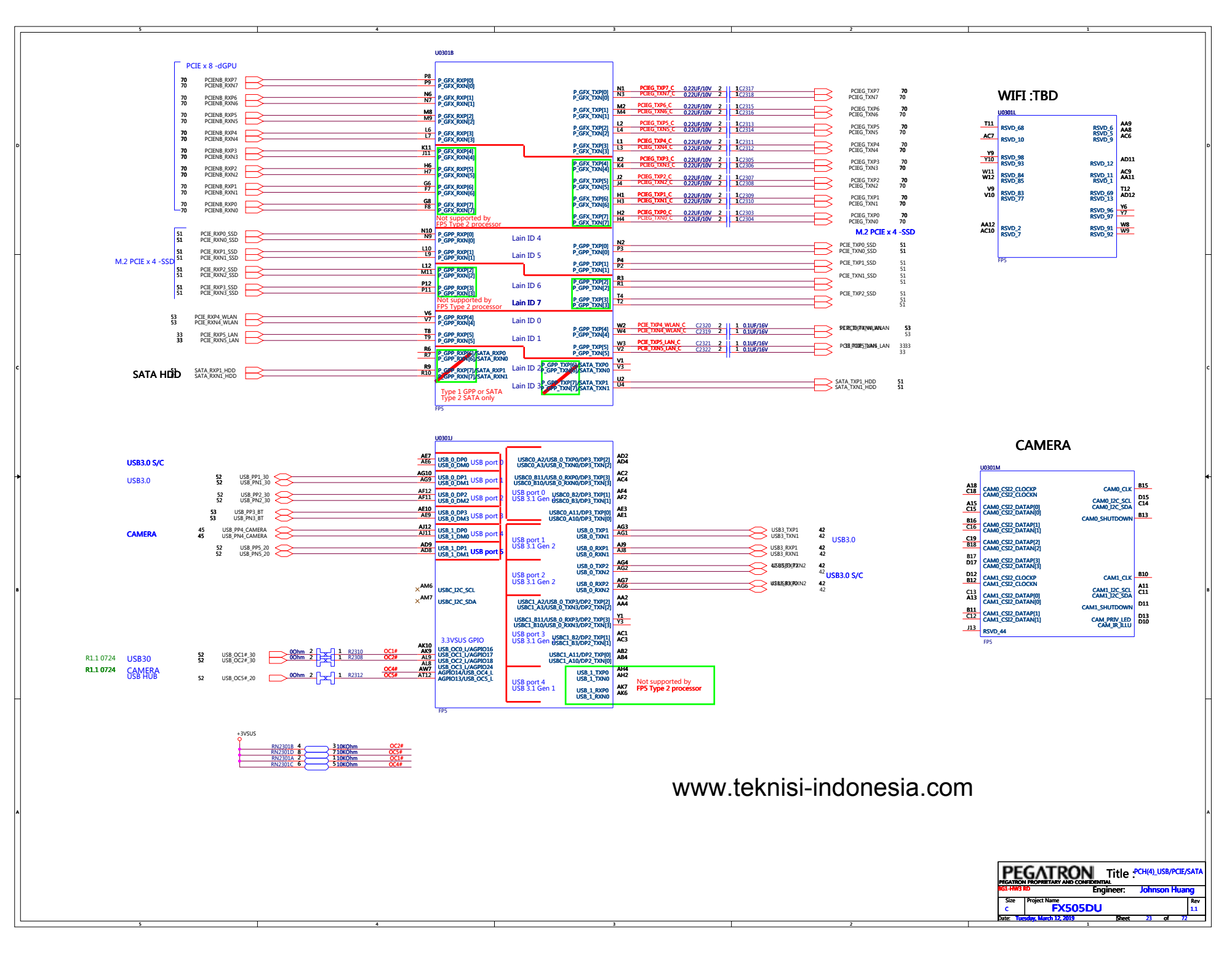
CE1800 330UF/2V @

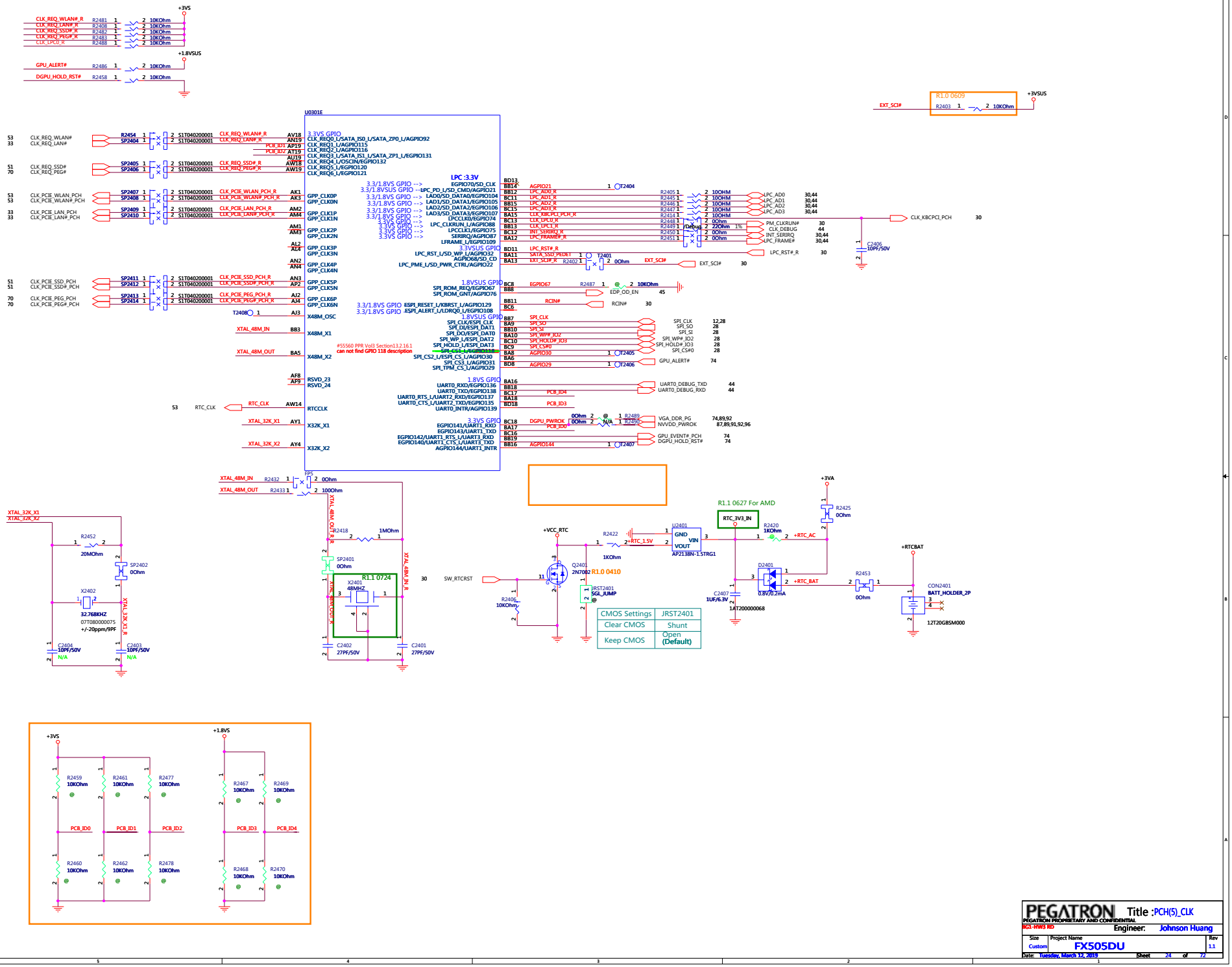
CFL-H DDR4 SODIMM Decoupling

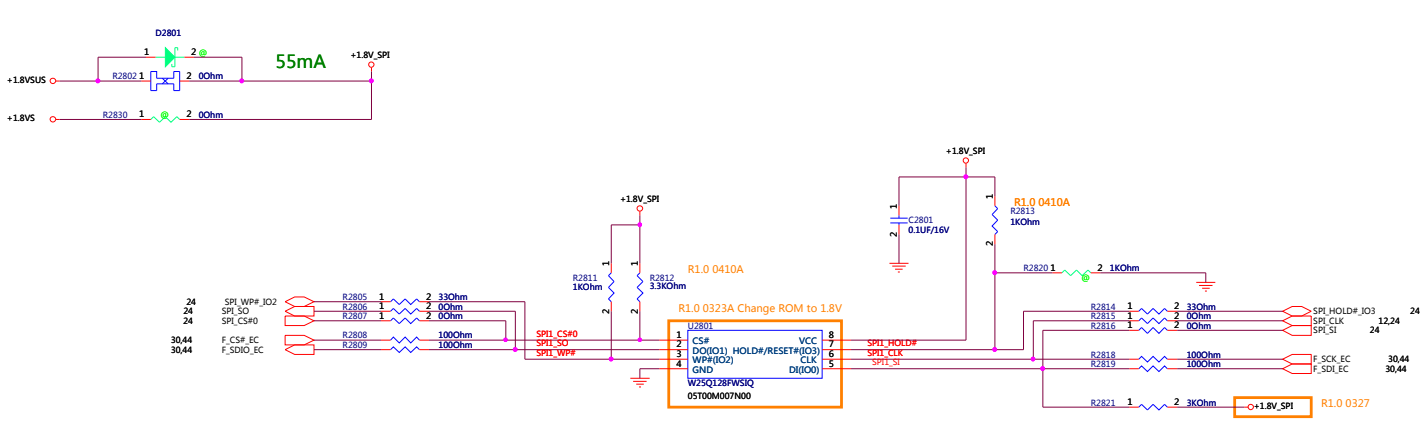
DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x pF (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DDR, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DDR	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

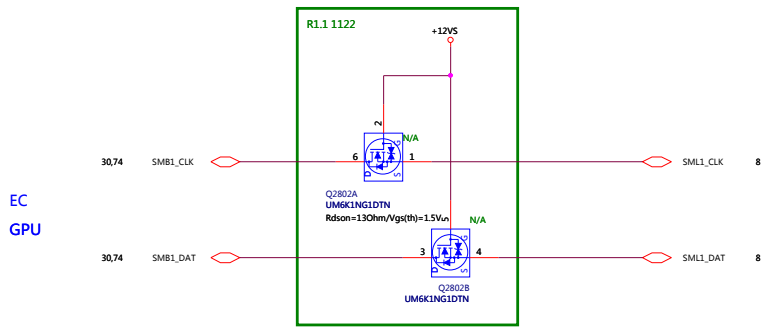
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4 Caps.
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size C | Project Name FX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 18 of 72


PCIE x 8 -dGPU
M.2 PCIE x 4 -SSD
SATA HDD
WIFI :TBD
CAMERA
USB3.0 S/C
USB3.0
CAMERA
R1.1 0724 USB30
R1.1 0724 CAMERA
USB HUB
Not supported by FP5 Type 2 processor
Type 1 GPP or SATA
Type 2 SATA only
3.3VSUS GPIO
www.teknisi-indonesia.com
PEGATRON
Title : PCH(4)_USB/PCIE/SATA
Engineer: Johnson Huang
Project Name FX505DU
Date: Tuesday, March 12, 2019
Sheet 23 of 72

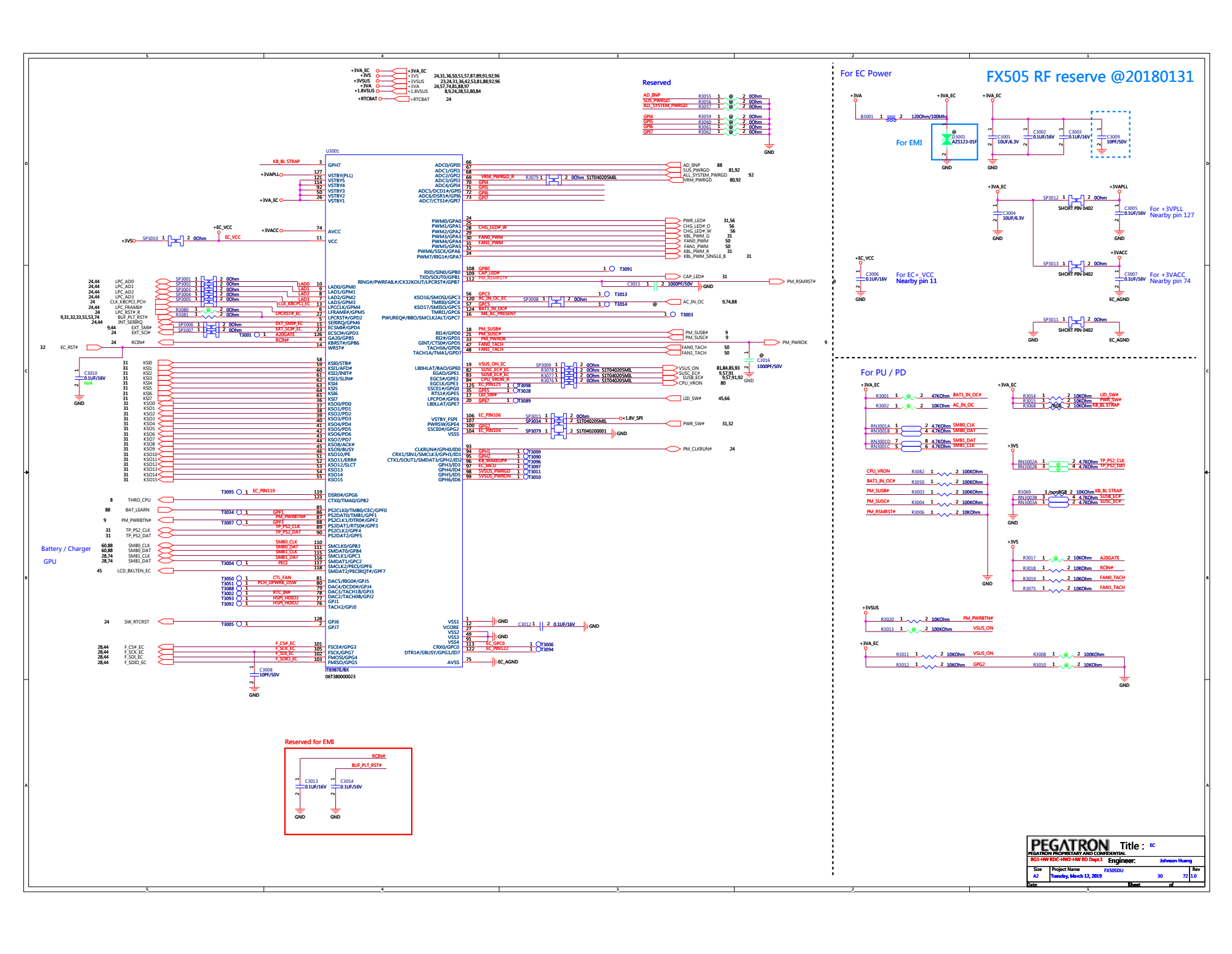

+3VS
+1.8VSUS
CLK_REQ_WLAN#_R
CLK_REQ_LAN#_R
CLK_REQ_SSD#_R
CLK_REQ_PEG#_R
CLK_LPC0_R
GPU_ALERT#
DGPU_HOLD_RST#
U0301E
3.3VS GPIO
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
CLK_REQ4_L/OSCIN/EGPIO132
CLK_REQ5_L/EGPIO120
CLK_REQ6_L/EGPIO121
LPC :3.3V
EGPIO70/SD_CLK
LPC_PD_L/SD_CMD/AGPIO21
LAD0/SD_DATA0/EGPIO104
LAD1/SD_DATA1/EGPIO105
LAD2/SD_DATA2/EGPIO106
LAD3/SD_DATA3/EGPIO107
LPCCLK0/EGPIO74
LPC_CLKRUN_L/AGPIO88
LPCCLK1/EGPIO75
SERIRQ/AGPIO87
LFRAME_L/EGPIO109
3.3VSUS GPIO
LPC_RST_L/SD_WP_L/AGPIO32
AGPIO68/SD_CD
LPC_PME_L/SD_PWR_CTRL/AGPIO22
1.8VSUS GPIO
SPI_ROM_REQ/EGPIO67
SPI_ROM_GNT/AGPIO76
ESPI_RESET_L/KBRST_L/AGPIO129
ESPI_ALERT_L/LDRQ0_L/EGPIO108
SPI_CLK/ESPI_CLK
SPI_DI/ESPI_DAT1
SPI_DO/ESPI_DAT0
SPI_WP_L/ESPI_DAT2
SPI_HOLD_L/ESPI_DAT3
SPI_CS1_L/EGPIO118
SPI_CS2_L/ESPI_CS_L/AGPIO30
SPI_CS3_L/AGPIO31
SPI_TPM_CS_L/AGPIO29
1.8VS GPIO
UART0_RXD/EGPIO136
UART0_TXD/EGPIO138
UART0_RTS_L/UART2_RXD/EGPIO137
UART0_CTS_L/UART2_TXD/EGPIO135
UART0_INTR/AGPIO139
3.3VS GPIO
EGPIO141/UART1_RXD
EGPIO143/UART1_TXD
EGPIO142/UART1_RTS_L/UART3_RXD
EGPIO140/UART1_CTS_L/UART3_TXD
AGPIO144/UART1_INTR
#55560 PPR Vol3 Section13.2.16.1
can not find GPIO 118 description
X48M_OSC
X48M_X1
X48M_X2
RSVD_23
RSVD_24
RTCCLK
X32K_X1
X32K_X2
XTAL_48M_IN
XTAL_48M_OUT
RTC_CLK
XTAL_32K_X1
XTAL_32K_X2
R1.0 0609
EXT_SCI#
R1.1 0724
R1.1 0627 For AMD
R1.0 0410
CMOS Settings
Clear CMOS
Keep CMOS
JRST2401
Shunt
Open
(Default)
RTC_3V3_IN
+VCC_RTC
+3VA
+RTCBAT
+RTC_AC
+RTC_BAT
+RTC_1.5V
SW_RTCRST
PCB_ID0
PCB_ID1
PCB_ID2
PCB_ID3
PCB_ID4
PEGATRON
Title :PCH(5)_CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
BGT-HW3 R0
Engineer: Johnson Huang
Size: Custom
Project Name: FX505DU
Rev: 1.1
Date: Tuesday, March 12, 2019
Sheet 24 of 72

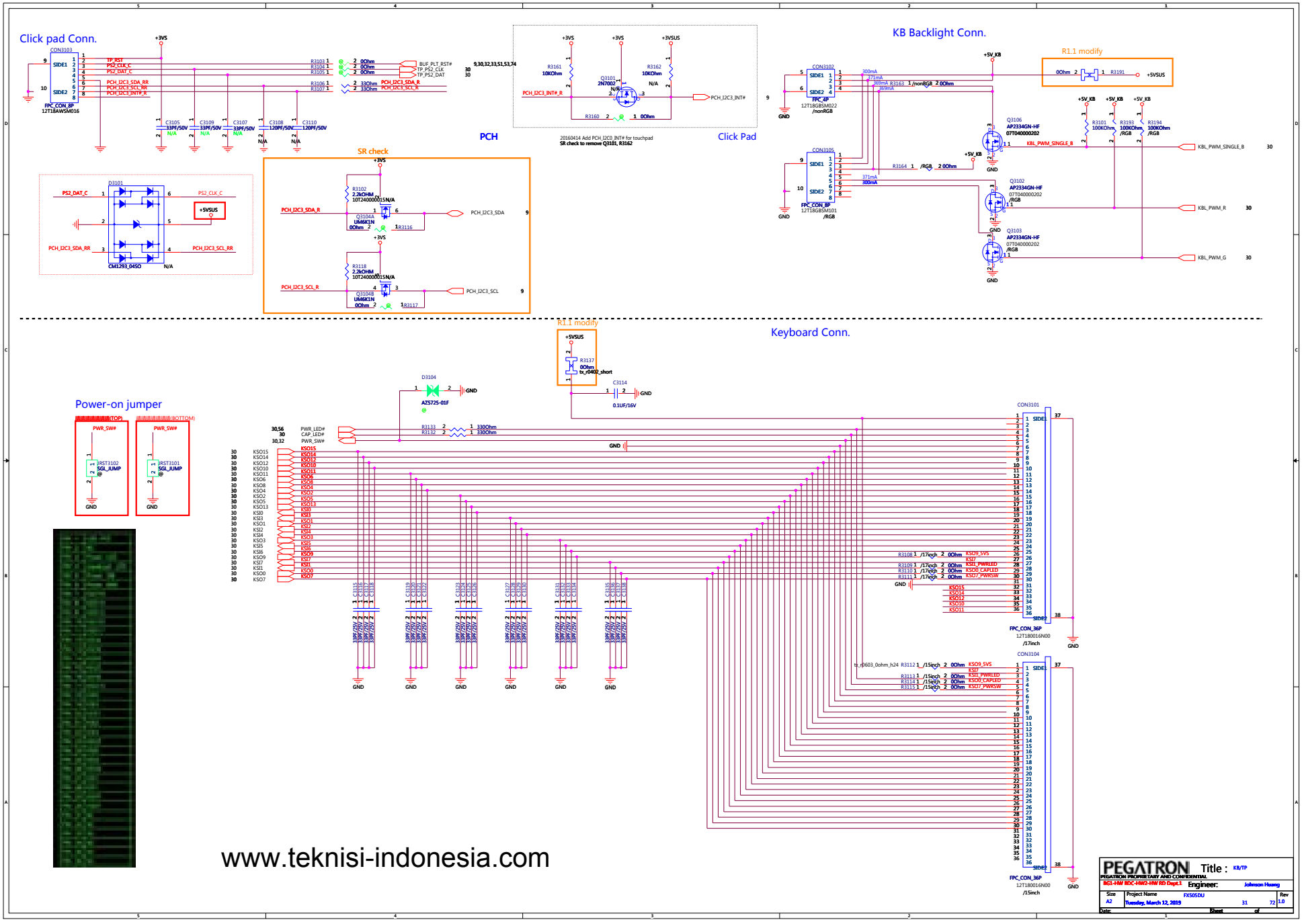


PCH SMBus



PEGATRON PROPRIETARY AND CONFIDENTIAL	Title :	PCH(9)_SPI_SMB
X51-HW3 RD	Engineer:	Johnson Huang
Size: Custom	Project Name: FX505DU	Rev: 1.1
Date: Tuesday, March 12, 2019	Sheet 28 of 72	

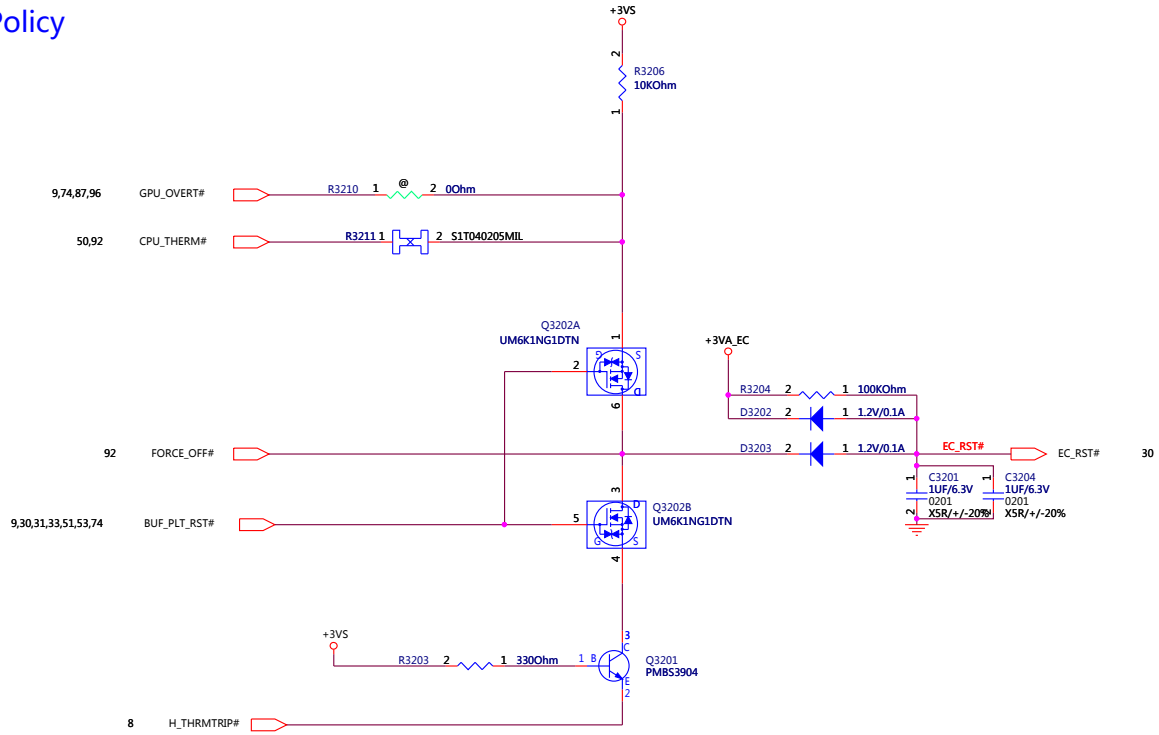

For EC Power
FX505 RF reserve @20180131
For EMI
For +3VPLL
Nearby pin 127
For EC+_VCC
Nearby pin 11
For +3VACC
Nearby pin 74
For PU / PD
Reserved
Reserved for EMI
Battery / Charger
GPU
U3001
IT8987E/BX
06T380000023
PEGATRON
Title : EC
PEGATRON PROPRIETARY AND CONFIDENTIAL
RC1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size A2
Project Name FX505DU
Rev 1.0
Tuesday, March 12, 2019
Sheet 30 of 72


Click pad Conn.
PCH
Click Pad
SR check
KB Backlight Conn.
R1.1 modify
Power-on jumper
Keyboard Conn.
www.teknisi-indonesia.com
PEGATRON
Title : KB/TP
Engineer:
Johnson Huang
FX505DU
Tuesday, March 12, 2019

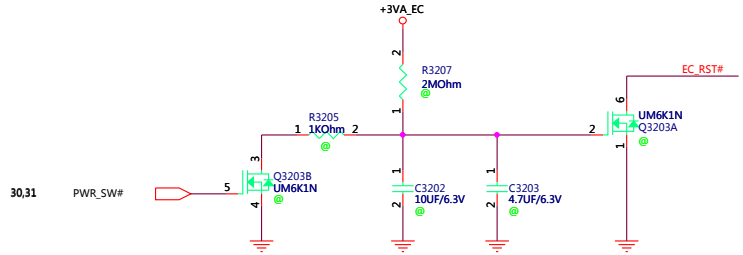
+3VA_EC +3VA_EC

+3VS +3VS 24,31,36,50,51,57,87,89,91,92,96

Thermal Policy



EC reset



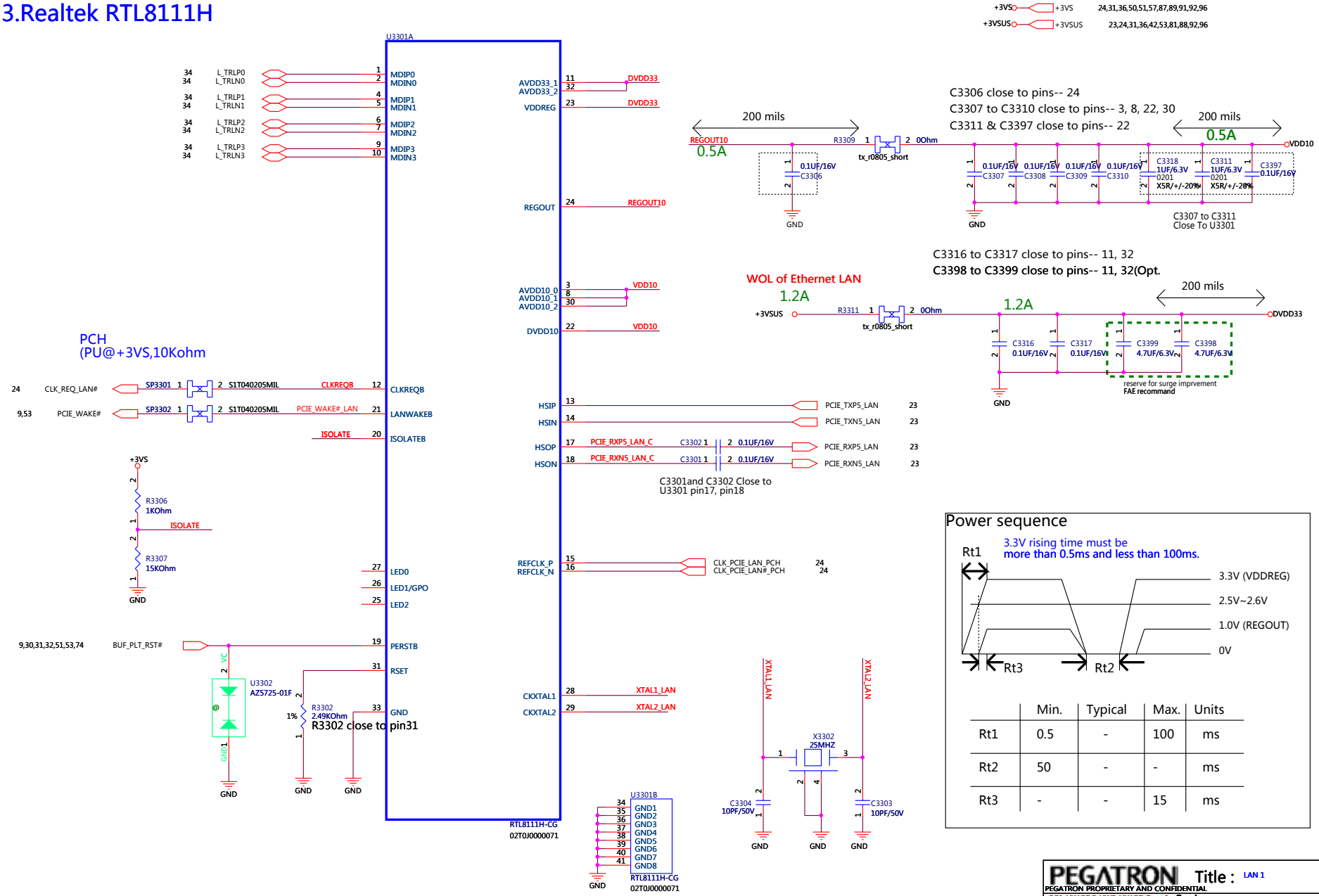
PEGATRON Title : RST

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 32 of 72	

33.Realtek RTL8111H

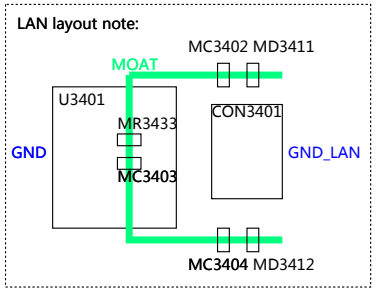


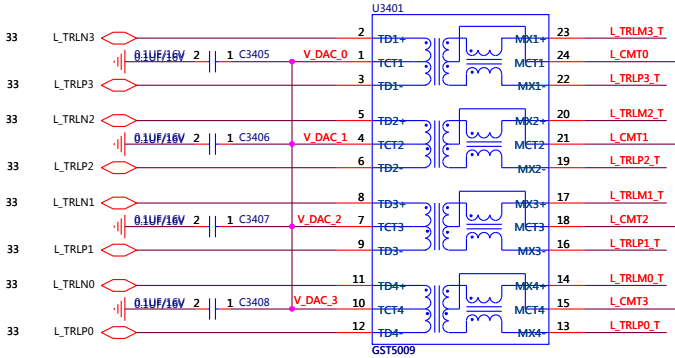
Power sequence

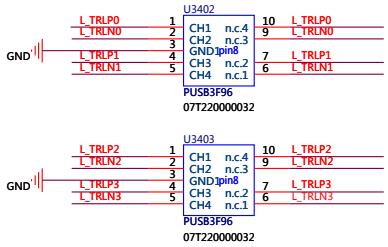
	Min.	Typical	Max.	Units
Rt1	0.5	-	100	ms
Rt2	50	-	-	ms
Rt3	-	-	15	ms

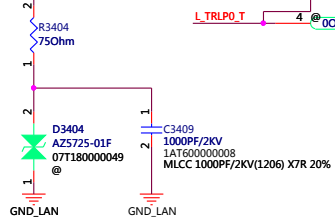
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : LAN 1
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size A3 | Project Name FX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 33 of 72

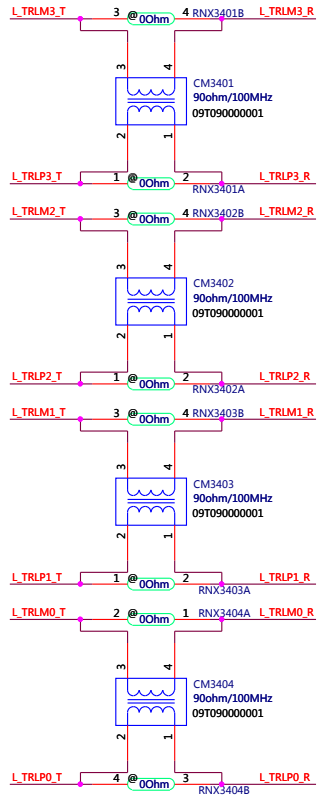
34.Transformer/RJ45



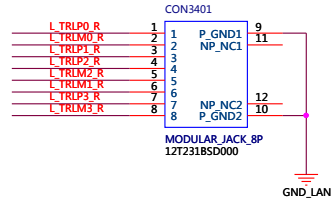


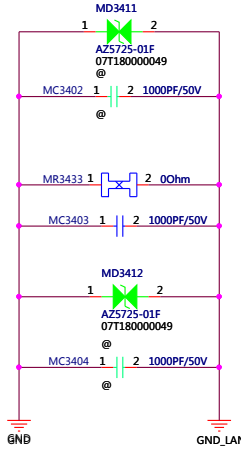






RJ45





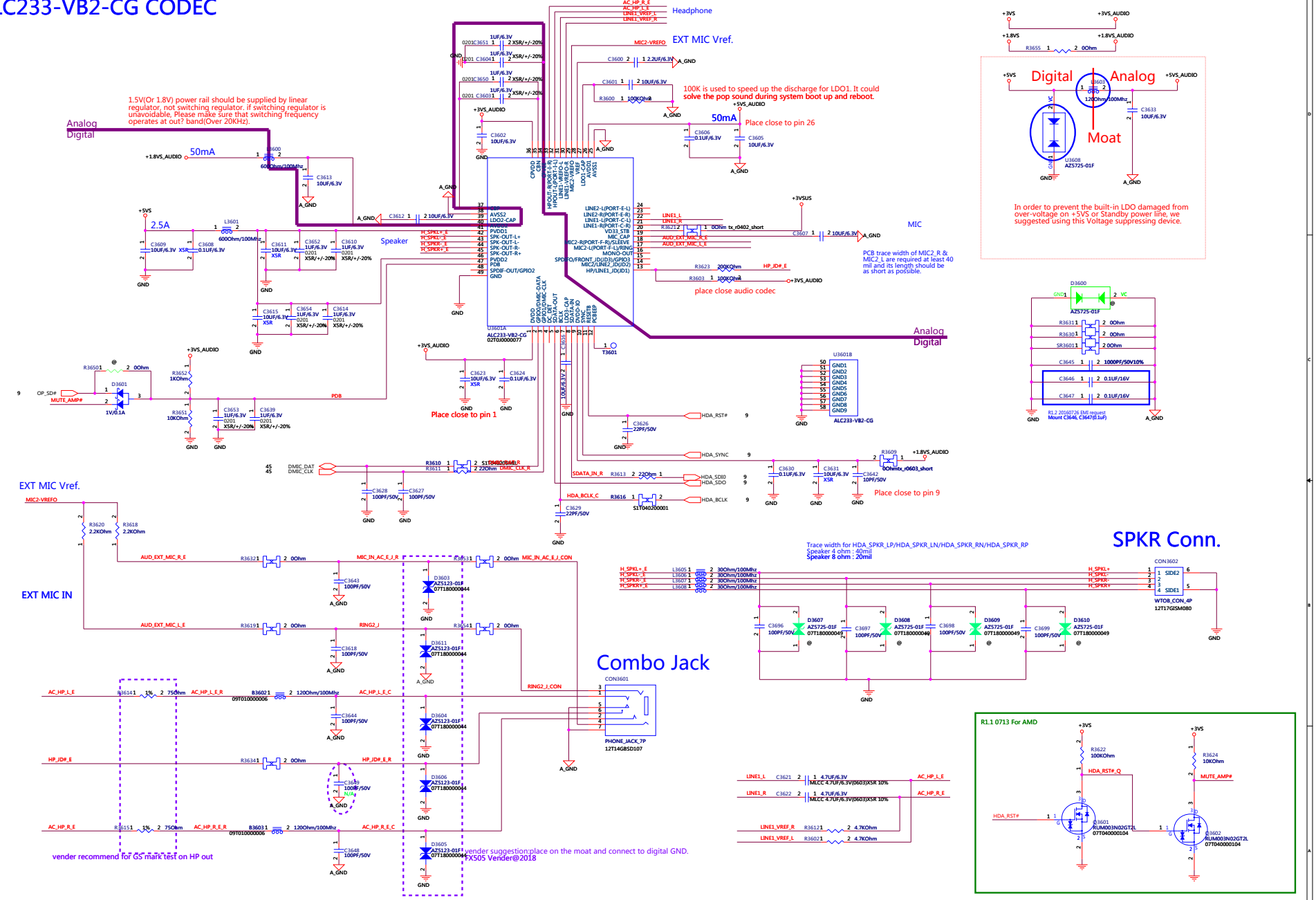
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LAN 2

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

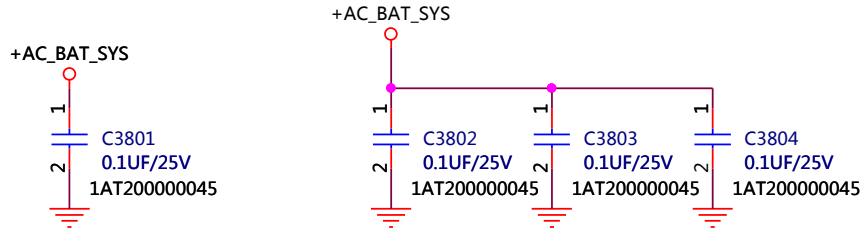
Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 34 of 72	

ALC233-VB2-CG CODEC



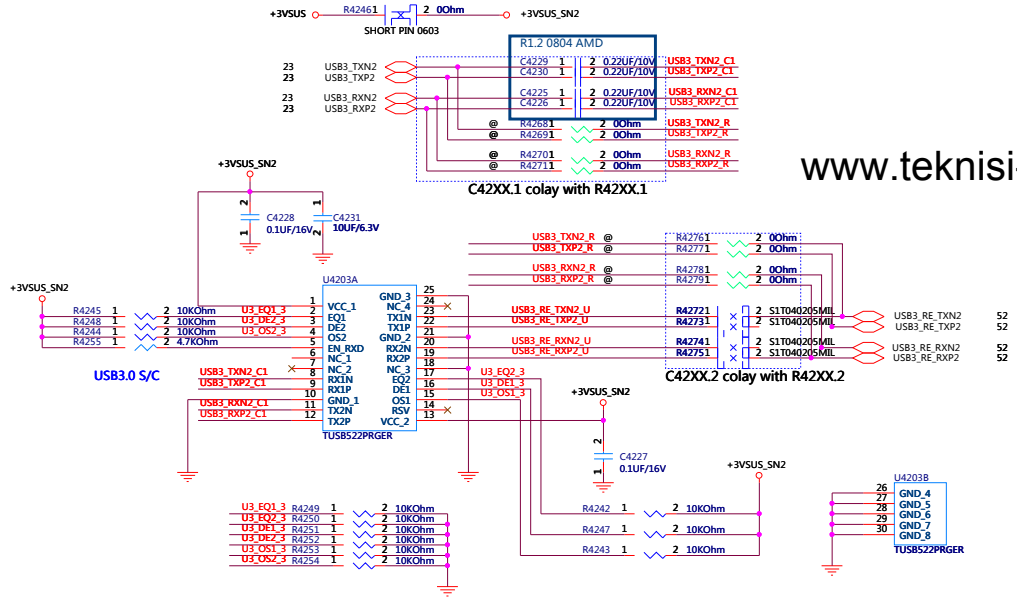
PEGATRON	Title :	AUDIO CODEC	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
RD1-HW RDC-MK2-HW RD Dept.	Engineer:	Johnson Huang	
Size	Project Name	FX505DU	Rev
Custom	Tuesday, March 12, 2019	36 72	1.0
Date:		Sheet of	

+AC_BAT_SYS +AC_BAT_SYS 80,81,82,83,84,88,97

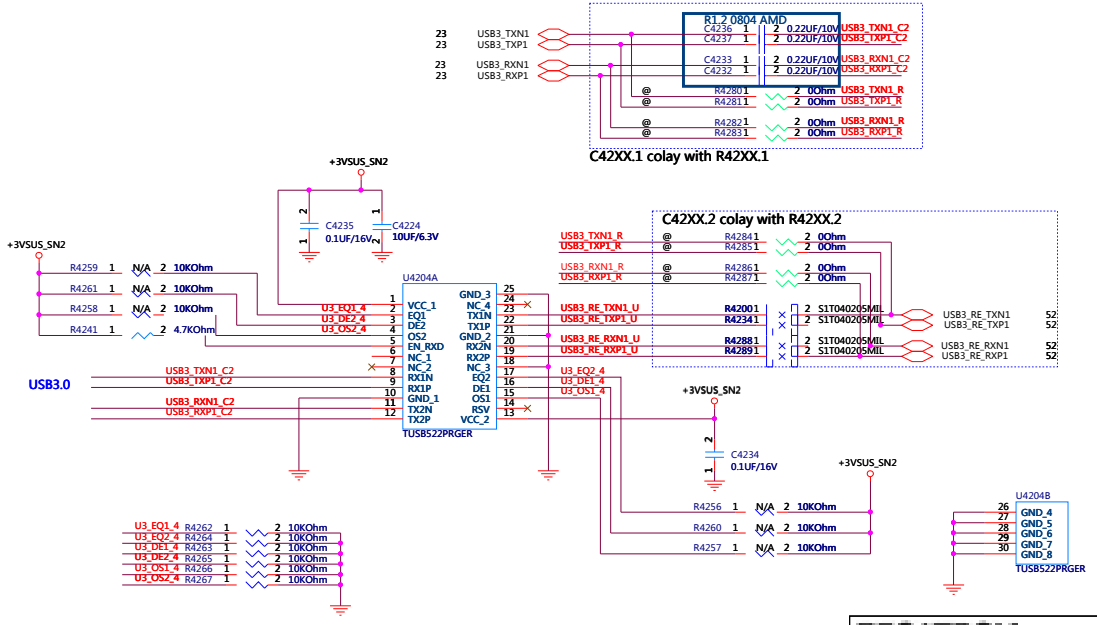


Title	<Title>	
Size A	Document Number FX505DU	Rev 1.1
Date: Tuesday, March 12, 2019	Sheet 38 of 72	

USB 3.0 PORT 0 S/C (Gen 1)



USB 3.0 PORT 1 (Gen 1)



PEGATRON Title : USB3 repeater

PEGATRON PROPRIETARY AND CONFIDENTIAL

BGT-HW3 RD

Engineer: Johnson Huang

Size	Project Name	Rev
Custom	FX505DU	1.1

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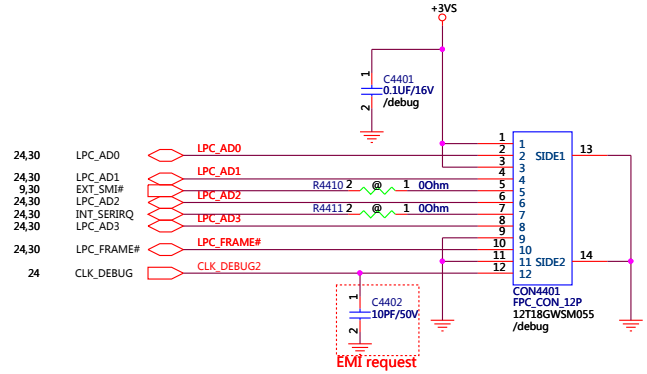
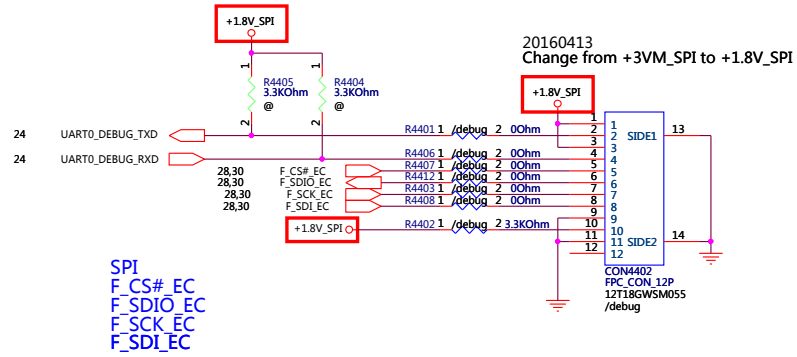
+3VS +3VS 24,31,36,50,51,57,87,89,91,92,96

+3VSUS +3VSUS 23,24,31,36,42,53,81,88,92,96

+3VM_SPI +3VM_SPI





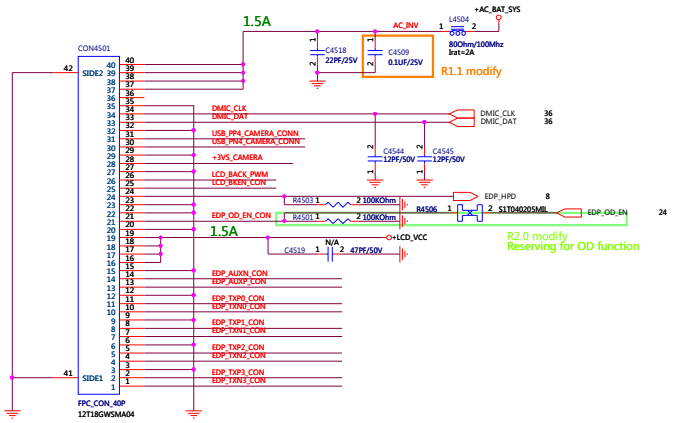
PEGATRON Title : DEBUG

PEGATRON PROPRIETARY AND CONFIDENTIAL

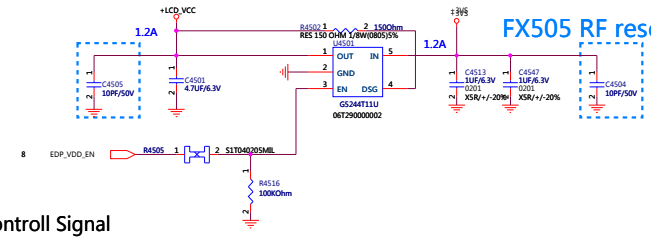
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 44 of 72	

eDP Conn.

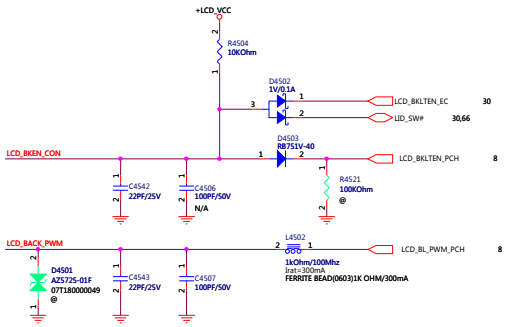


LCD VDDEN / +LED_VCC

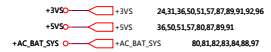


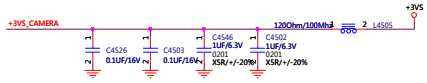
FX505 RF reserve @20180131

Controll Signal

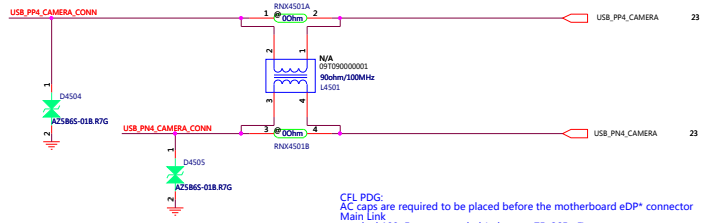


Camera Signal

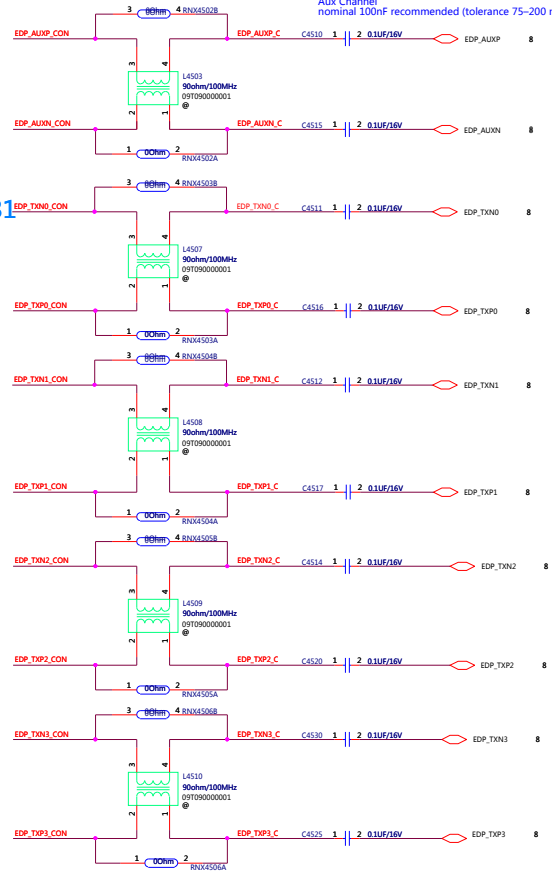




CAMERA

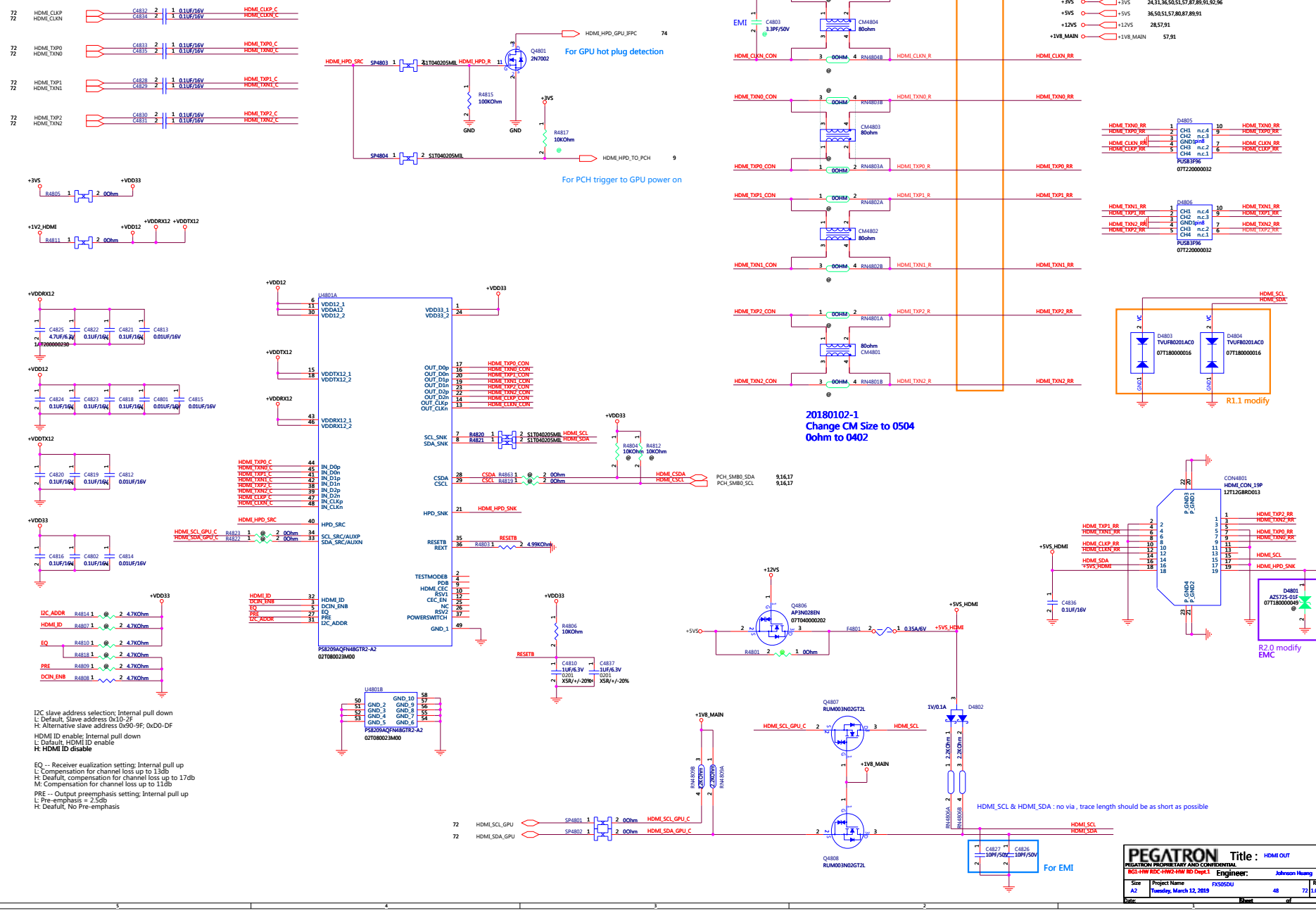


CFL PDG:
AC caps are required to be placed before the motherboard eDP* connector
Main Link
nominal 100nF recommended (tolerance 75~265 nF)
Aux Channel
nominal 100nF recommended (tolerance 75~200 nF)



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : EDP/MIC
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size A2
Project Name FX505DU
Rev 1.0
Date: Tuesday, March 12, 2019
Sheet 45 of 72

HDMI


R10_0727_EMI
Size change to 0201
R1.1 modify
Delete R4855~R4862
For GPU hot plug detection
For PCH trigger to GPU power on
20180102-1
Change CM Size to 0504
0ohm to 0402
R1.1 modify
R2.0 modify
EMC
For EMI
HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible
I2C slave address selection; Internal pull down
L: Default, Slave address 0x10-2F
H: Alternative slave address 0x90-9F; 0xD0-DF
HDMI ID enable: Internal pull down
L: Default, HDMI ID enable
H: HDMI ID disable
EQ -- Receiver eualization setting; Internal pull up
L: Compensation for channel loss up to 13db
H: Deafult, compensation for channel loss up to 17db
M: Compensation for channel loss up to 11db
PRE -- Output preemphasis setting; Internal pull up
L: Pre-emphasis = 2.5db
H: Deafult, No Pre-emphasis
PEGATRON
Title : HDMI OUT
PEGATRON PROPRIETARY AND CONFIDENTIAL
RC1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size A2
Project Name FX505DU
Rev 1.0
Tuesday, March 12, 2019
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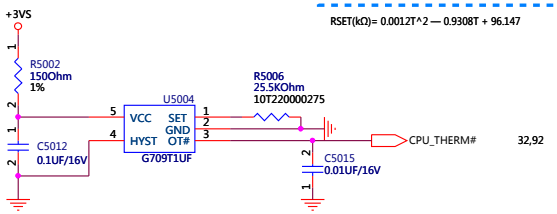
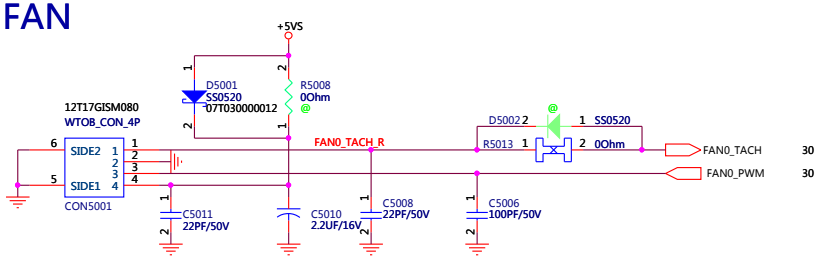
CPU Thermal Sensor

temperature set=85 C

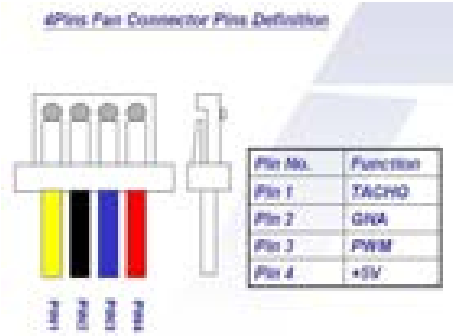
RSET(kΩ)= 0.0012T^2 — 0.9308T + 96.147



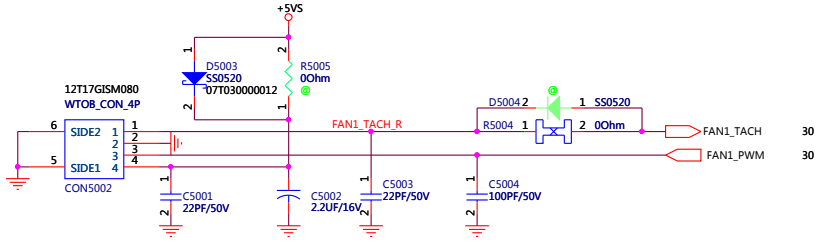
CPU FAN



EC(PU@+3VS,10Kohm



GPU FAN



EC(PU@+3VS,10Kohm

PEGATRON Title : FAN/THERMAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0

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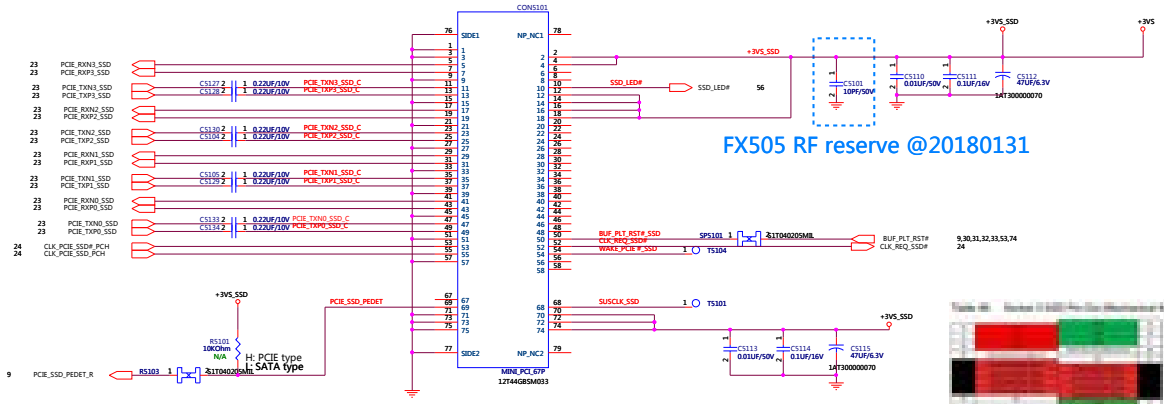
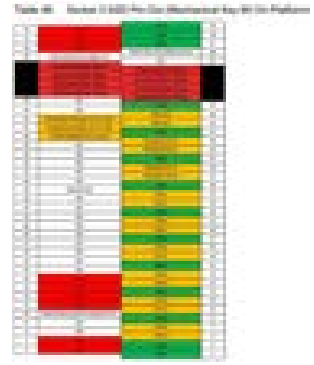
SSD/HDD

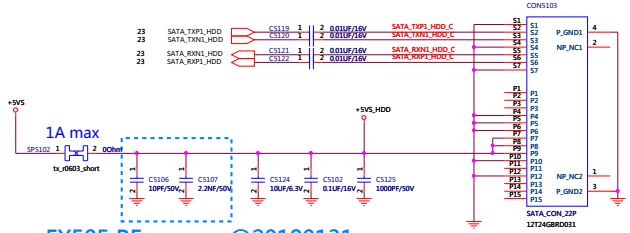
M.2 2280 KEY-M



FX505 RF reserve @20180131



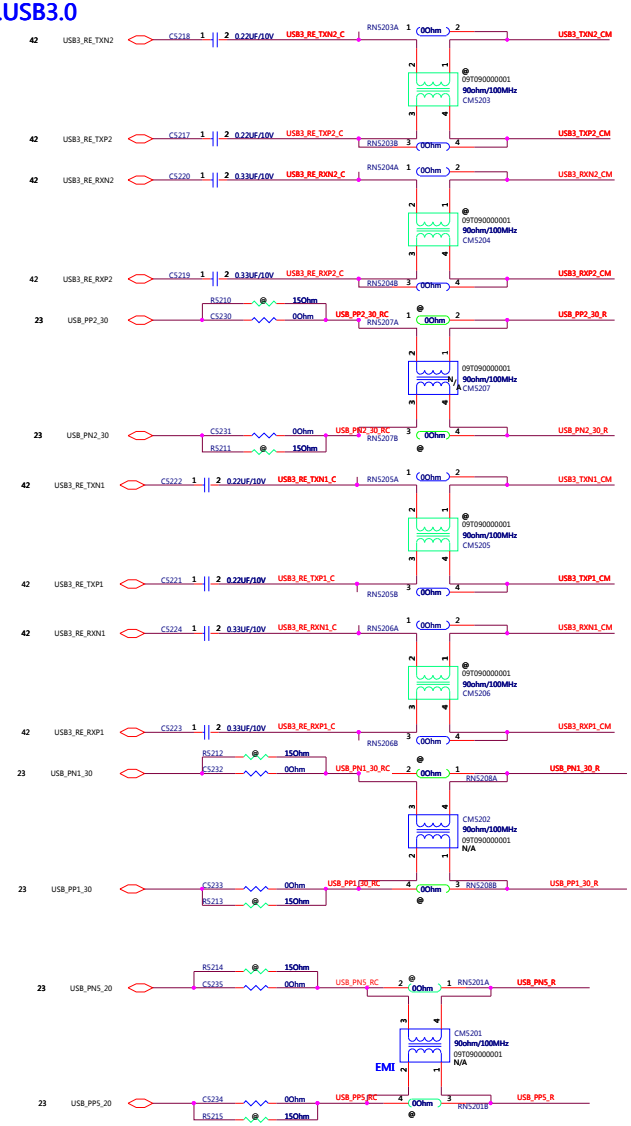
SATA Conn. 2.5"HDD

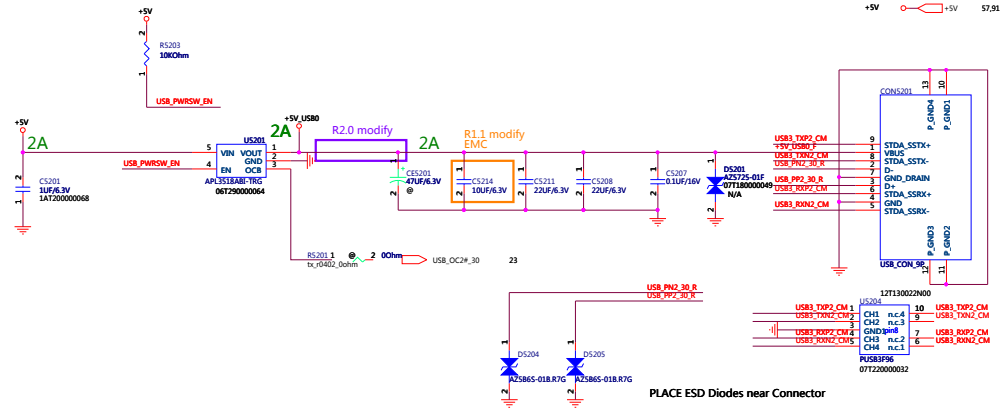


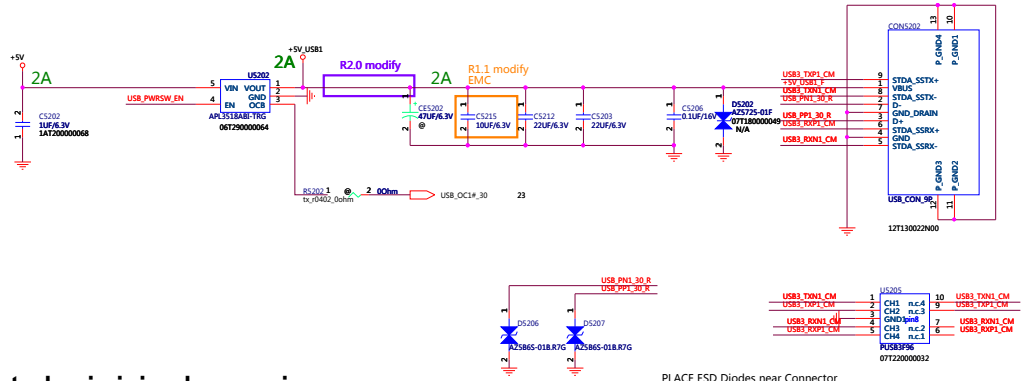
FX505 RF reserve @20180131

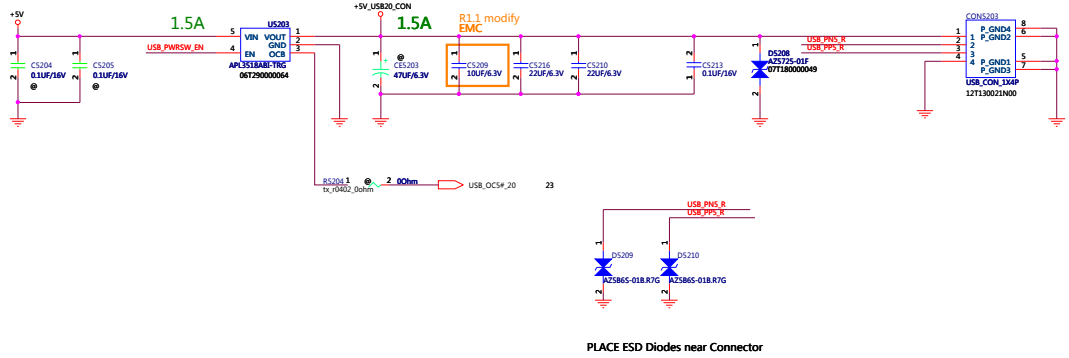
PEGATRON	Title : SSD/HDD		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
9G1-HW RDC-HMO-HW RD Dept.1	Engineer: Johnson Huang		
Size: Custom	Project Name: FX505DU	Rev: 1.0	
Date: Tuesday, March 12, 2019	Sheet: 51 of 72		

52.USB3.0









PEGATRON Title : USB JCAK

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW MDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A2	FX505GE	1.0

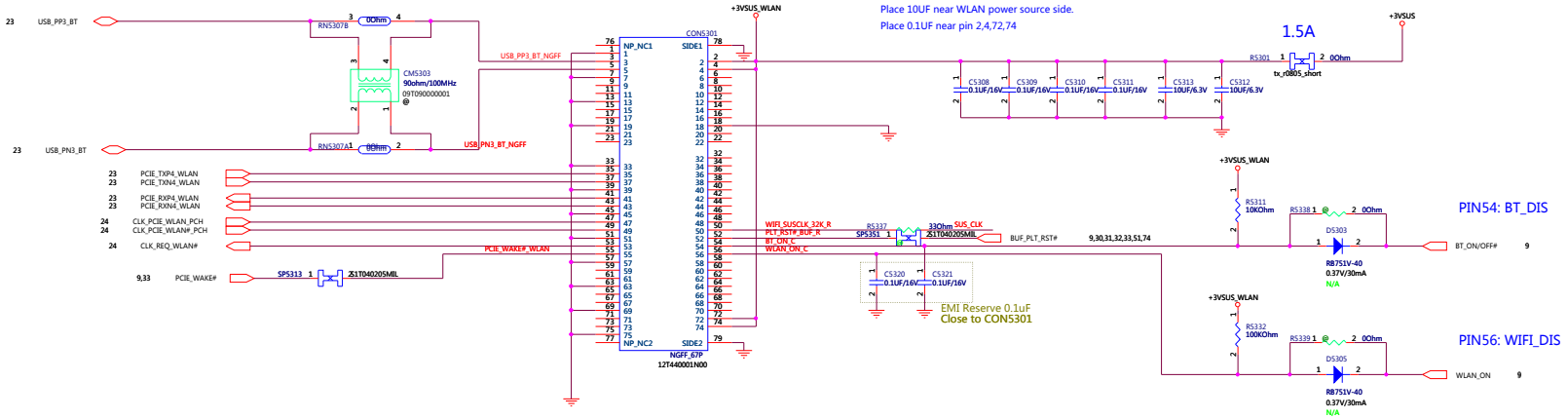
Date: Tuesday, March 12, 2019 Sheet 52 of 72

WLAN+BT

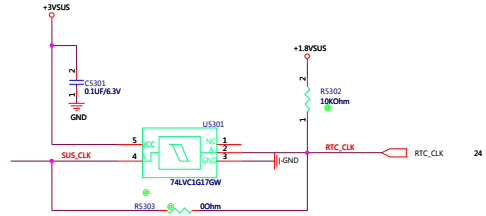
M.2 2230 KEY-E

WLAN bypass capactors:

Place 10UF near WLAN power source side.
Place 0.1UF near pin 2,4,72,74



WLAN_SUS_CLK Update



+3VSUS	+3VSUS	9,11,12,23,24,30,31,33,36,42,74,81,88,92,96
+1.8VSUS	+1.8VSUS	8,9,11,12,24,28,80,84

PEGATRON Title : WLAN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BCI-HW BDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A2	EX505DU	1.0
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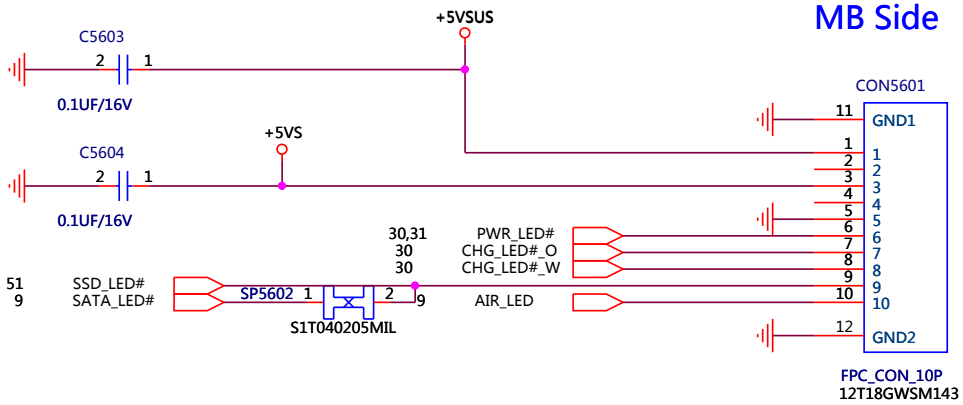


+5VSUS	+5VSUS	31,81
+5VS	+5VS	36,50,51,57,80,87,89,91

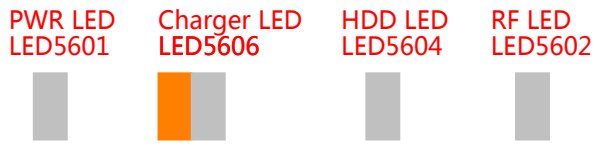
Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF

Charger LED

PCB/ID LOCATION



HDD LED

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LED

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A4	FX505DU	1.0

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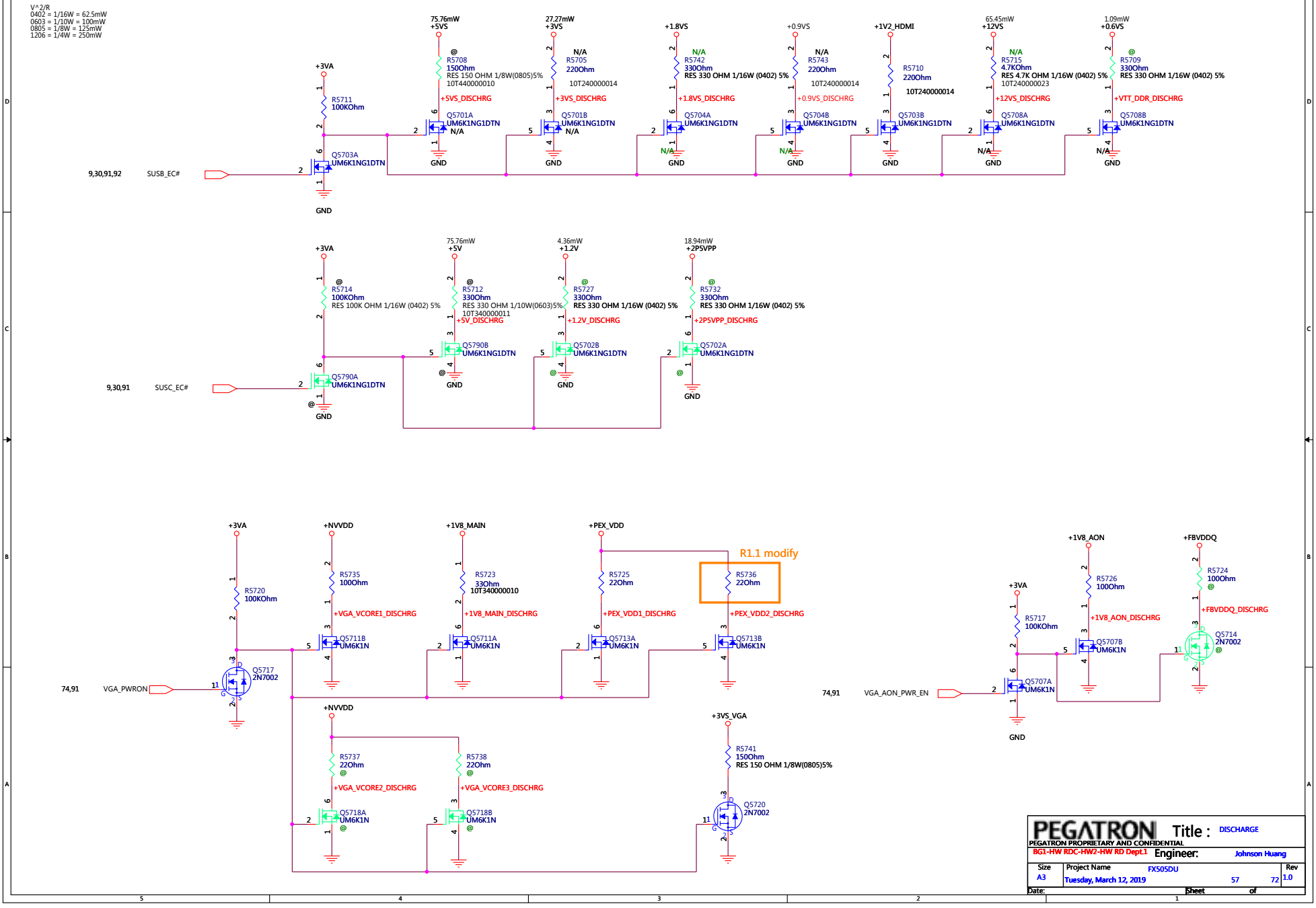
V^2/R
0402 = 1/16W = 62.5mW
0603 = 1/10W = 100mW
0805 = 1/8W = 125mW
1206 = 1/4W = 250mW
+3VA
R5711
100KOhm
Q5703A
UM6K1NG1DTN
9,30,91,92
SUSB_EC#
GND
75.76mW
+5VS
@
R5708
150Ohm
RES 150 OHM 1/8W(0805)5%
10T440000010
+5VS_DISCHRG
Q5701A
UM6K1NG1DTN
N/A
27.27mW
+3VS
N/A
R5705
220Ohm
10T240000014
+3VS_DISCHRG
Q5701B
UM6K1NG1DTN
+1.8VS
N/A
R5742
330Ohm
RES 330 OHM 1/16W (0402) 5%
+1.8VS_DISCHRG
Q5704A
UM6K1NG1DTN
+0.9VS
N/A
R5743
220Ohm
10T240000014
+0.9VS_DISCHRG
Q5704B
UM6K1NG1DTN
+1V2_HDMI
R5710
220Ohm
10T240000014
Q5703B
UM6K1NG1DTN
65.45mW
+12VS
N/A
R5715
4.7KOhm
RES 4.7K OHM 1/16W (0402) 5%
10T240000023
+12VS_DISCHRG
Q5708A
UM6K1NG1DTN
1.09mW
+0.6VS
@
R5709
330Ohm
RES 330 OHM 1/16W (0402) 5%
+VTT_DDR_DISCHRG
Q5708B
UM6K1NG1DTN
+3VA
@
R5714
100KOhm
RES 100K OHM 1/16W (0402) 5%
Q5790A
UM6K1NG1DTN
9,30,91
SUSC_EC#
75.76mW
+5V
@
R5712
330Ohm
RES 330 OHM 1/10W(0603)5%
10T340000011
+5V_DISCHRG
Q5790B
UM6K1NG1DTN
4.36mW
+1.2V
@
R5727
330Ohm
RES 330 OHM 1/16W (0402) 5%
+1.2V_DISCHRG
Q5702B
UM6K1NG1DTN
18.94mW
+2P5VPP
@
R5732
330Ohm
RES 330 OHM 1/16W (0402) 5%
+2P5VPP_DISCHRG
Q5702A
UM6K1NG1DTN
+3VA
R5720
100KOhm
Q5717
2N7002
74,91
VGA_PWRON
+NVVDD
R5735
100Ohm
+VGA_VCORE1_DISCHRG
Q5711B
UM6K1N
+1V8_MAIN
R5723
33Ohm
10T340000010
+1V8_MAIN_DISCHRG
Q5711A
UM6K1N
+PEX_VDD
R5725
22Ohm
+PEX_VDD1_DISCHRG
Q5713A
UM6K1N
R1.1 modify
R5736
22Ohm
+PEX_VDD2_DISCHRG
Q5713B
UM6K1N
+NVVDD
R5737
22Ohm
@
+VGA_VCORE2_DISCHRG
Q5718A
UM6K1N
@
R5738
22Ohm
@
+VGA_VCORE3_DISCHRG
Q5718B
UM6K1N
@
+3VS_VGA
R5741
150Ohm
RES 150 OHM 1/8W(0805)5%
Q5720
2N7002
+1V8_AON
R5726
100Ohm
+1V8_AON_DISCHRG
Q5707B
UM6K1N
+FBVDDQ
R5724
100Ohm
@
+FBVDDQ_DISCHRG
Q5714
2N7002
@
+3VA
R5717
100KOhm
Q5707A
UM6K1N
74,91
VGA_AON_PWR_EN
GND
PEGATRON
Title : DISCHARGE
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size
A3
Project Name
FX505DU
Rev
1.0
Tuesday, March 12, 2019
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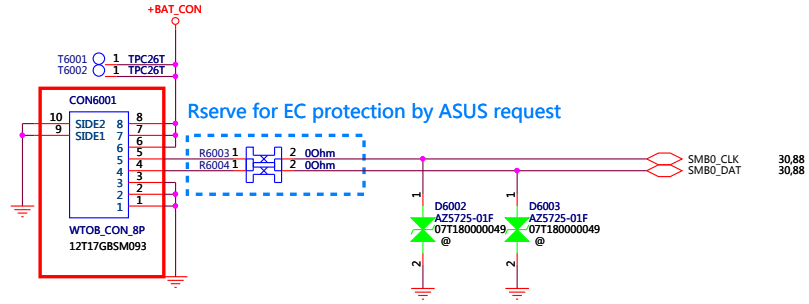
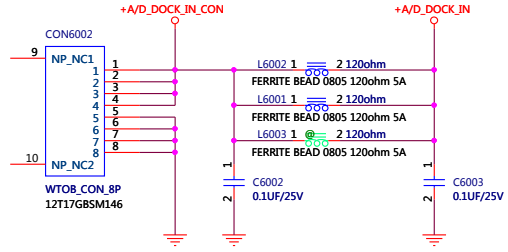
72

Battery Conn.



ABBA assign: 1217-01UG0AS(1217-017L000)，doesn't include 1217-01EG000 (the same pool)

AC in Conn.



FX505DD/DT N17P/N18P Adaptor: 120W (6.32A)
FX505DU N18E-G0 Adaptor: 180W (9.23A)

PEGATRON Title : BAT/AC IN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size A3 | Project Name FX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 60 of 99

65.NUT,Screw hole,Tooling hole

M.2 SSD NUT:

H6522
GND
CT236B176D146

Tooling hole

drill 3*3.5

H6518
1
O138x118DO138x118N

H6521
1
O138x118DO138x118N

drill 1.7

H6524
1
C67D67N

drill 2.2*1.7

H6526
1
O87X67DO87X67N

Screw hole

B group:
CPU GPU bracket hole

H6501
1
CT303CB185D146
H6502
1
CT303CB185D146
H6503
1
CT303CB185D146
H6504
1
CT303CB185D146
GND

H6505
1
CT303CB185D146
H6506
1
CT303CB185D146
H6507
1
CT303CB185D146
H6508
1
CT303CB185D146
GND

D group:

H6510
P_GND
NP_NC_1 ... NP_NC_48
NP_NC_2 ... NP_NC_47
NP_NC_3 ... NP_NC_46
NP_NC_4 ... NP_NC_45
NP_NC_5 ... NP_NC_44
NP_NC_6 ... NP_NC_43
NP_NC_7 ... NP_NC_42
NP_NC_8 ... NP_NC_41
NP_NC_9 ... NP_NC_40
NP_NC_10 ... NP_NC_39
NP_NC_11 ... NP_NC_38
NP_NC_12 ... NP_NC_37
NP_NC_13 ... NP_NC_36
NP_NC_14 ... NP_NC_35
NP_NC_15 ... NP_NC_34
NP_NC_16 ... NP_NC_33
NP_NC_17 ... NP_NC_32
NP_NC_18 ... NP_NC_31
NP_NC_19 ... NP_NC_30
NP_NC_20 ... NP_NC_29
NP_NC_21 ... NP_NC_28
NP_NC_22 ... NP_NC_27
NP_NC_23 ... NP_NC_26
NP_NC_24 ... NP_NC_25
GND
C315D118

E:
TOP: phi 7 drill 6
BOT: phi 7 drill 6

H6517
1
C276D236
GND

F:
TOP: phi 8 drill 3
BOT: phi 4 drill 3

H6511
1
CT315CB157D118
GND

C group:
TOP: phi 8 drill 2.5
BOT: phi 8 drill 2.5

H6514
1
C315D98
S1T1XDCCUY00
H6515
1
C315D98
S1T1XDCCUY00
H6516
1
C315D98
S1T1XDCCUY00
GND

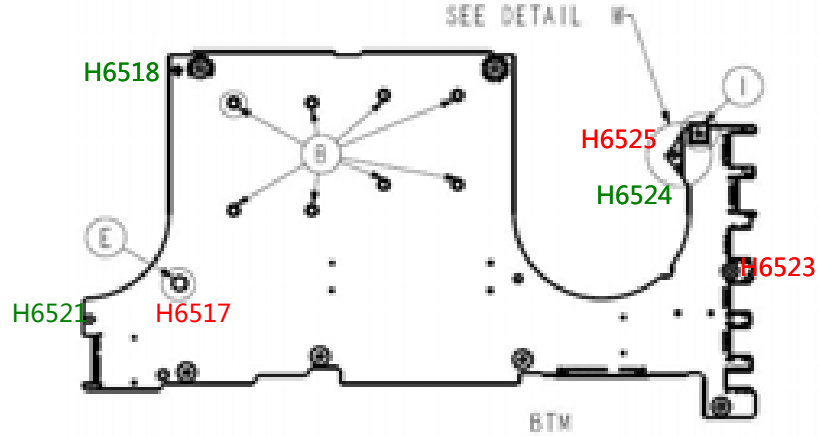
Near Audio Jack
TOP: square 8
BOT: phi 8 drill 3

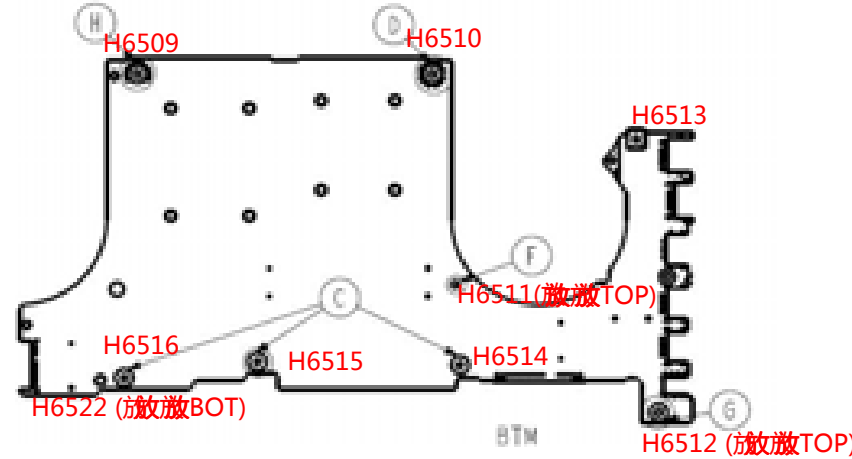
H6512
1
RT315X335B315D118
B_GND

R6501 1 @ 2 0Ohm
R6502 1 @ 2 0Ohm
B_GND
A_GND

H group:

H6509
P_GND
NP_NC1 ... NP_NC19
NP_NC2 ... NP_NC20
NP_NC3 ... NP_NC21
NP_NC4 ... NP_NC22
NP_NC5 ... NP_NC23
NP_NC6 ... NP_NC24
NP_NC7 ... NP_NC25
NP_NC8 ... NP_NC26
NP_NC9 ... NP_NC27
NP_NC10 ... NP_NC28
NP_NC11 ... NP_NC29
NP_NC12 ... NP_NC30
NP_NC13 ... NP_NC31
NP_NC14 ... NP_NC32
NP_NC15 ... NP_NC33
NP_NC16 ... NP_NC34
NP_NC17 ... NP_NC35
NP_NC18 ... NP_NC36
GND
C315D118





I group:
TOP: square8*8.5 drill 2.5
BOT: square8*8.5 drill 2.5

H6513
1
R315X335D98
GND

TOP: phi 7 drill 3
BOT: phi 7 drill 3

H6523
1
C276D118
GND

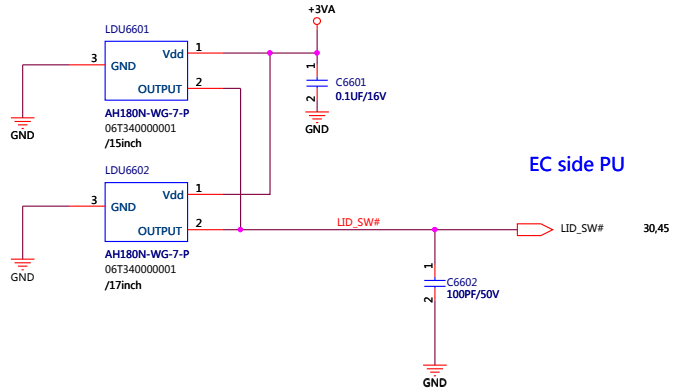
TOP: phi 3 drill 2.5
BOT: phi 3 drill 2.5

H6525
1
C118D98
GND

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : NUT/HOLE
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size: Custom | Project Name: FX505DU | Rev: 1.0
Date: Tuesday, March 12, 2019 | Sheet 65 of 72

+3VA +3VA 24,57,74,81,88,97

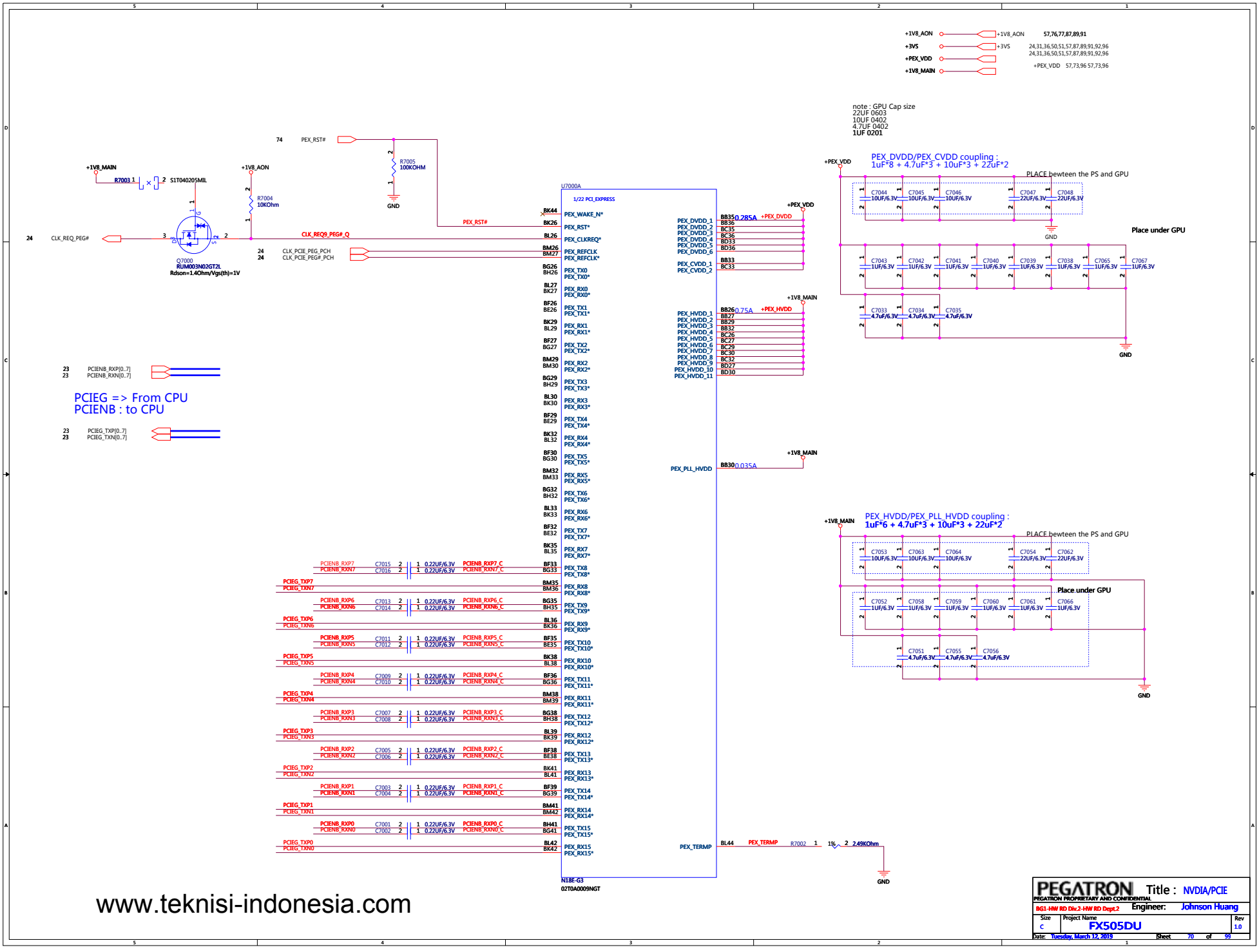
Hall sensor



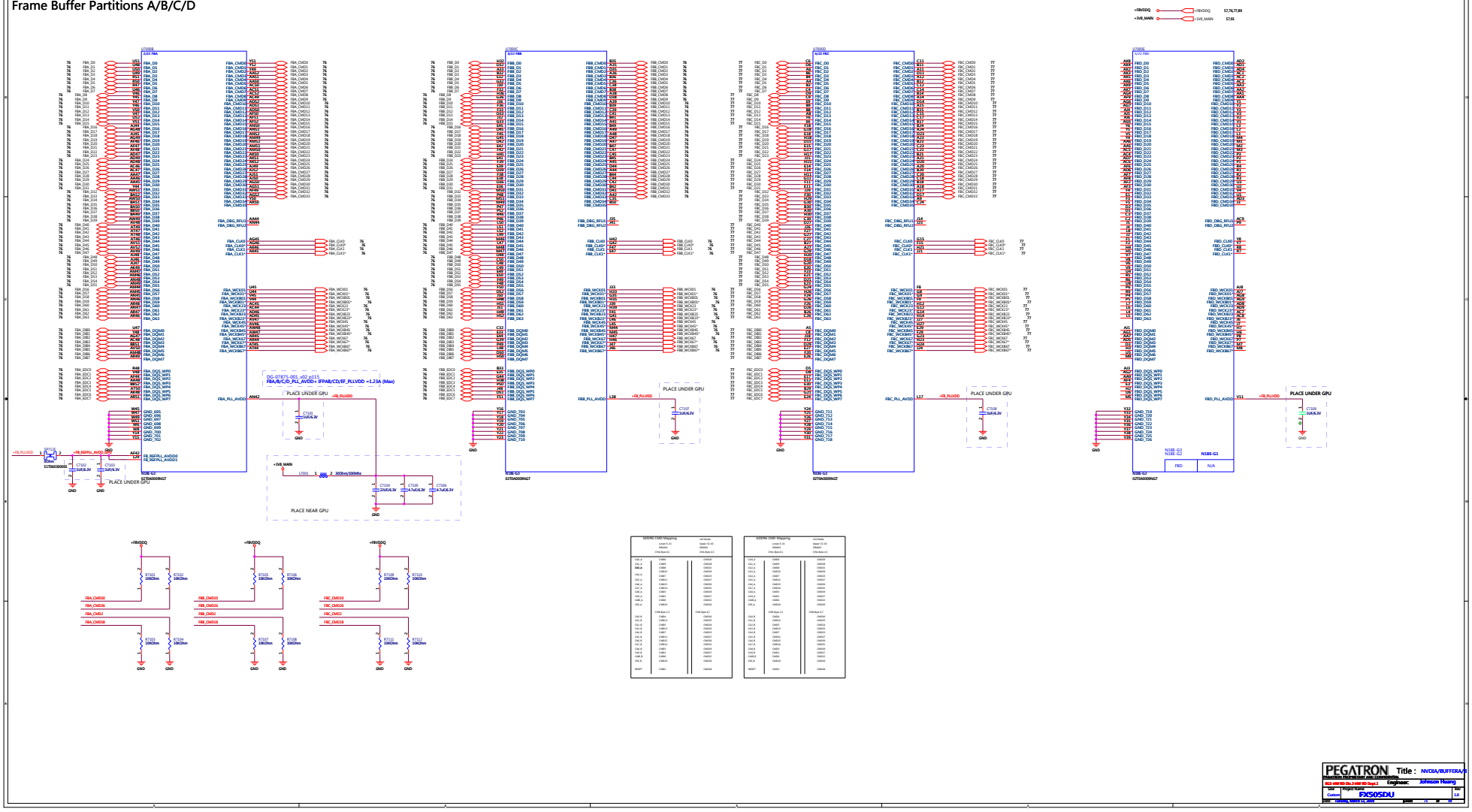
EC side PU

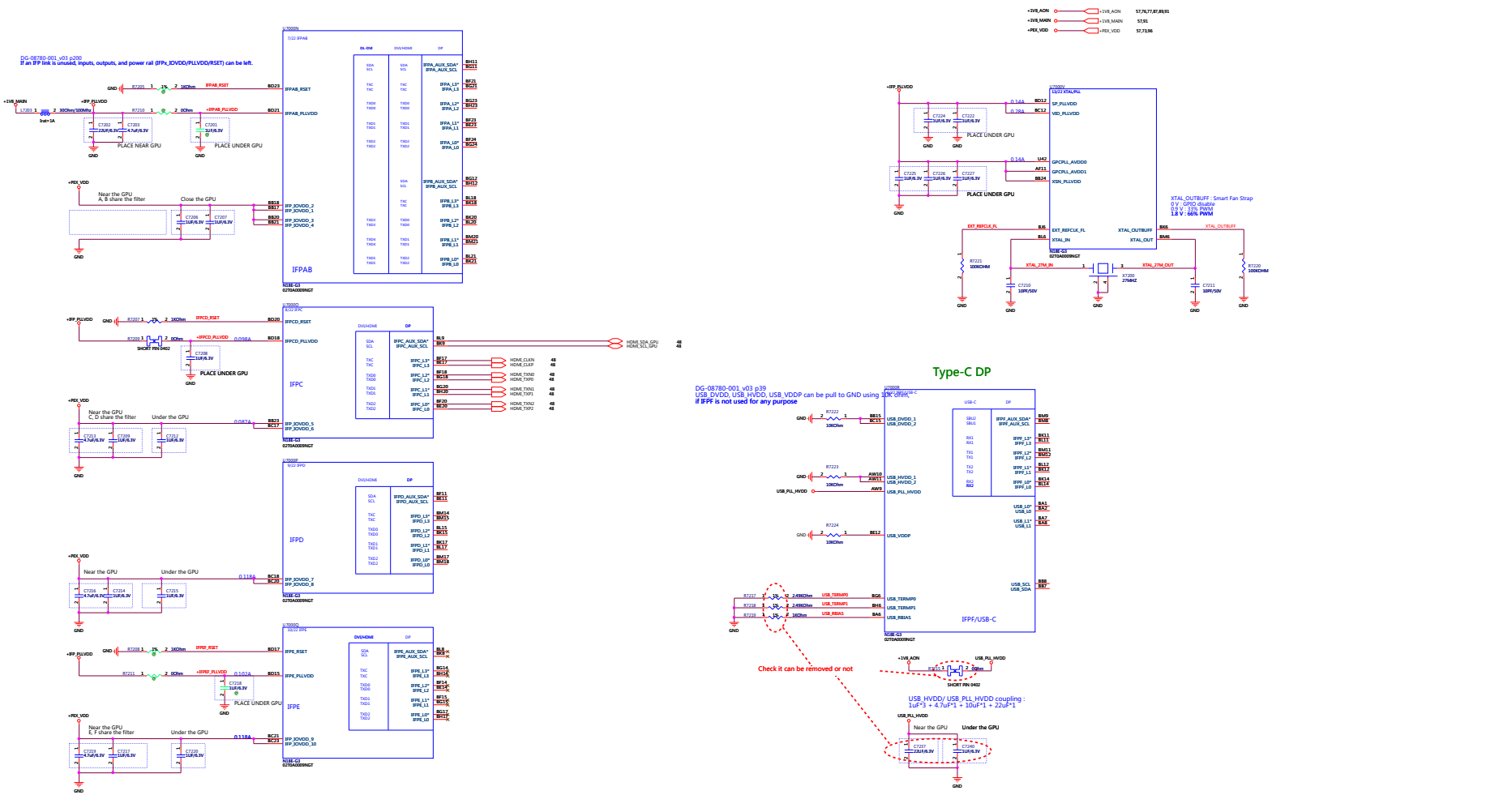
PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON	Title : TO DB	
BG1-HW RDC-HW2-HW RD Dept.1	Engineer: Johnson Huang	
Size A3	Project Name FX505DU	Rev 1.0
Date: Tuesday, March 12, 2019	Sheet 66 of 72	



Frame Buffer Partitions A/B/C/D





PEGATRON Title : NVDIA/DACA/XTAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Johnson Huang

Size	Project Name	Rev
D	FX505DU	1.0

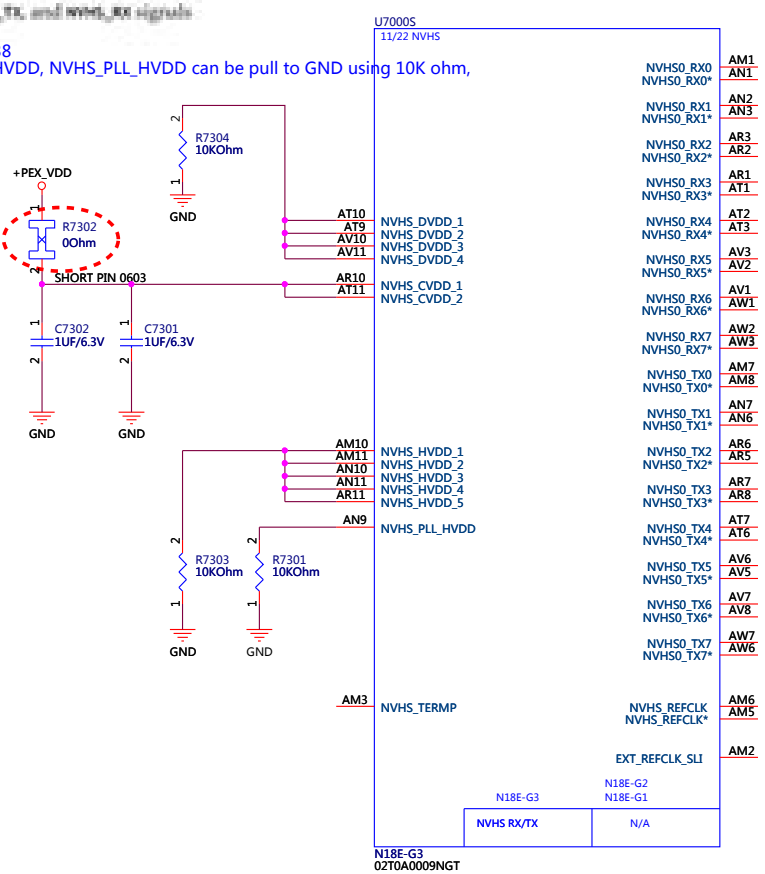
Date: Tuesday, March 12, 2019 Sheet 29 of 50

NVLINK

- N18E CPU does not support NVLink and SLI.
- Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, and NVHS_PLL_HVDD rails to GND with 10 K resistor
- Do not use any decoupling or filtering capacitor for NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, or NVHS_PLL_HVDD rails
- Leave NVHS_TESTMP, EXT_REFCLK_SLI, NVHS_REFCLK, NVHS_TS, and NVHS_RX signals floating (NC).

DG-08780-001_v03 p38
NVHS_DVDD, NVHS_HVDD, NVHS_PLL_HVDD can be pull to GND using 10K ohm, if no application

Check it can be removed or not



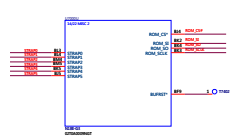
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

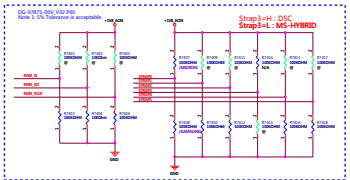
Title : NVDIA/Multi-use IO

BG1-HW RD Div.2-HW RD Dept.2 Engineer: Johnson Huang

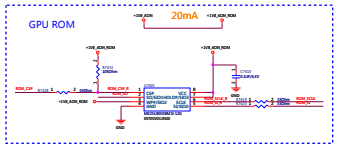
Size	Project Name	Rev
B	FX505DU	1.0

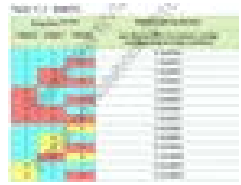
Date: Tuesday, March 12, 2019 Sheet 73 of 99

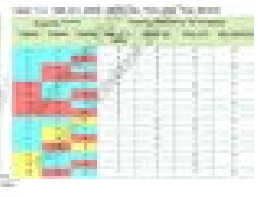




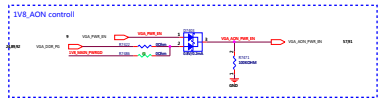
STRAP2	STRAP1	STRAP0	Vendor
0	0	0	Samsung
0	0	1	Micron

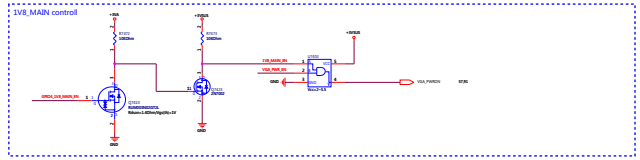


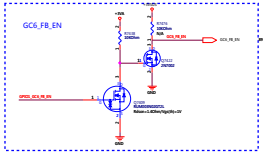


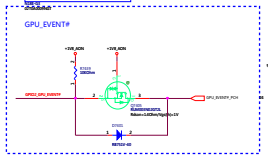


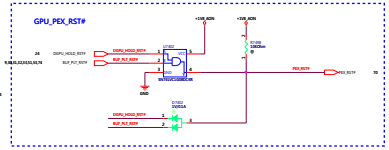
NV power sequence

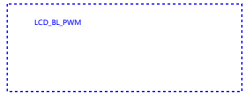


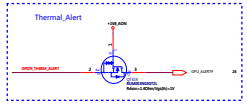


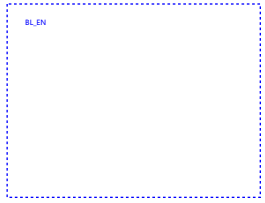


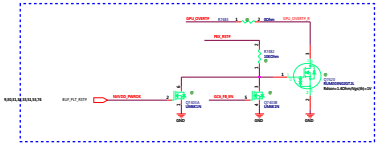


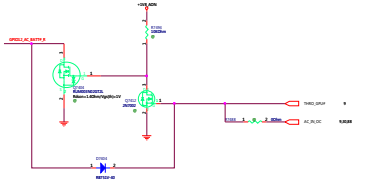




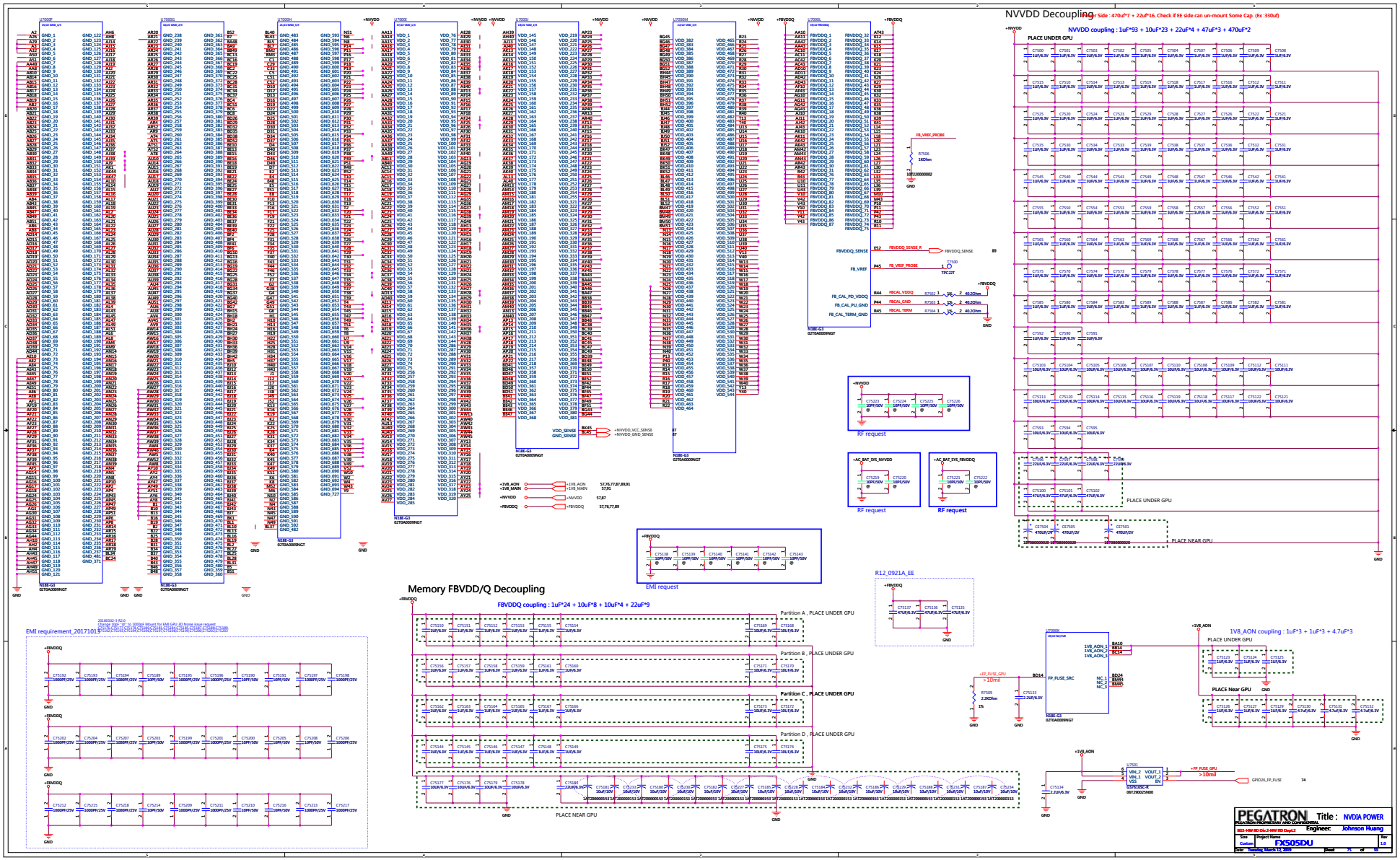


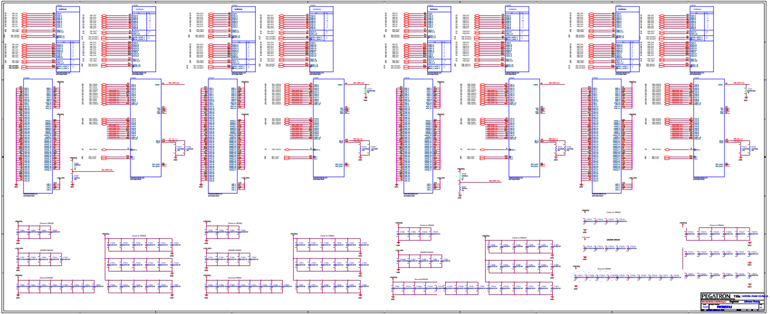




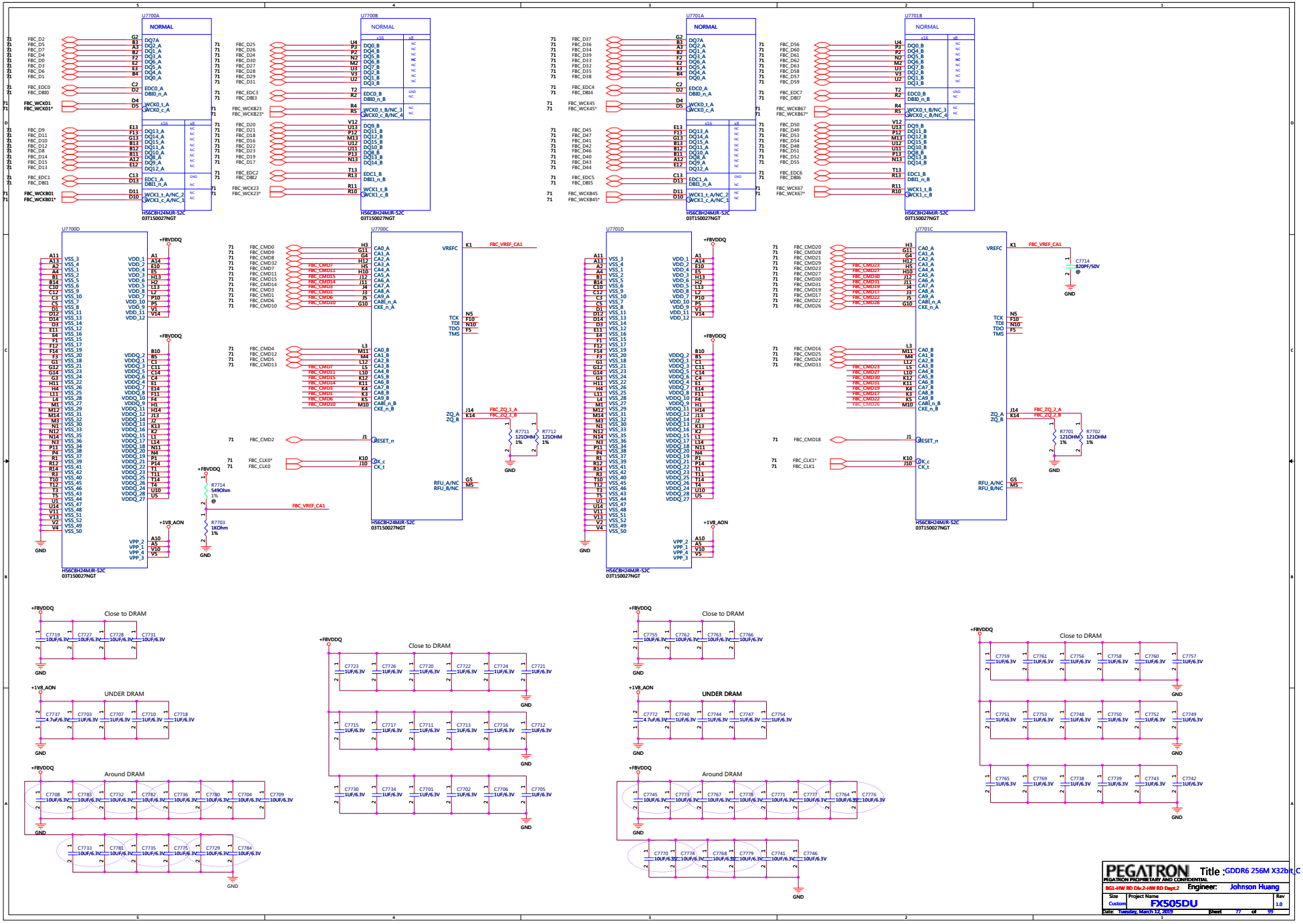


PEGATRON	Title : NVIDIA MISC/GPIO	
	Engineer: Johnson Huang	
Size	Project Name	Rev
Custom	FXSOSDU	1A
Date:	Sheet of	

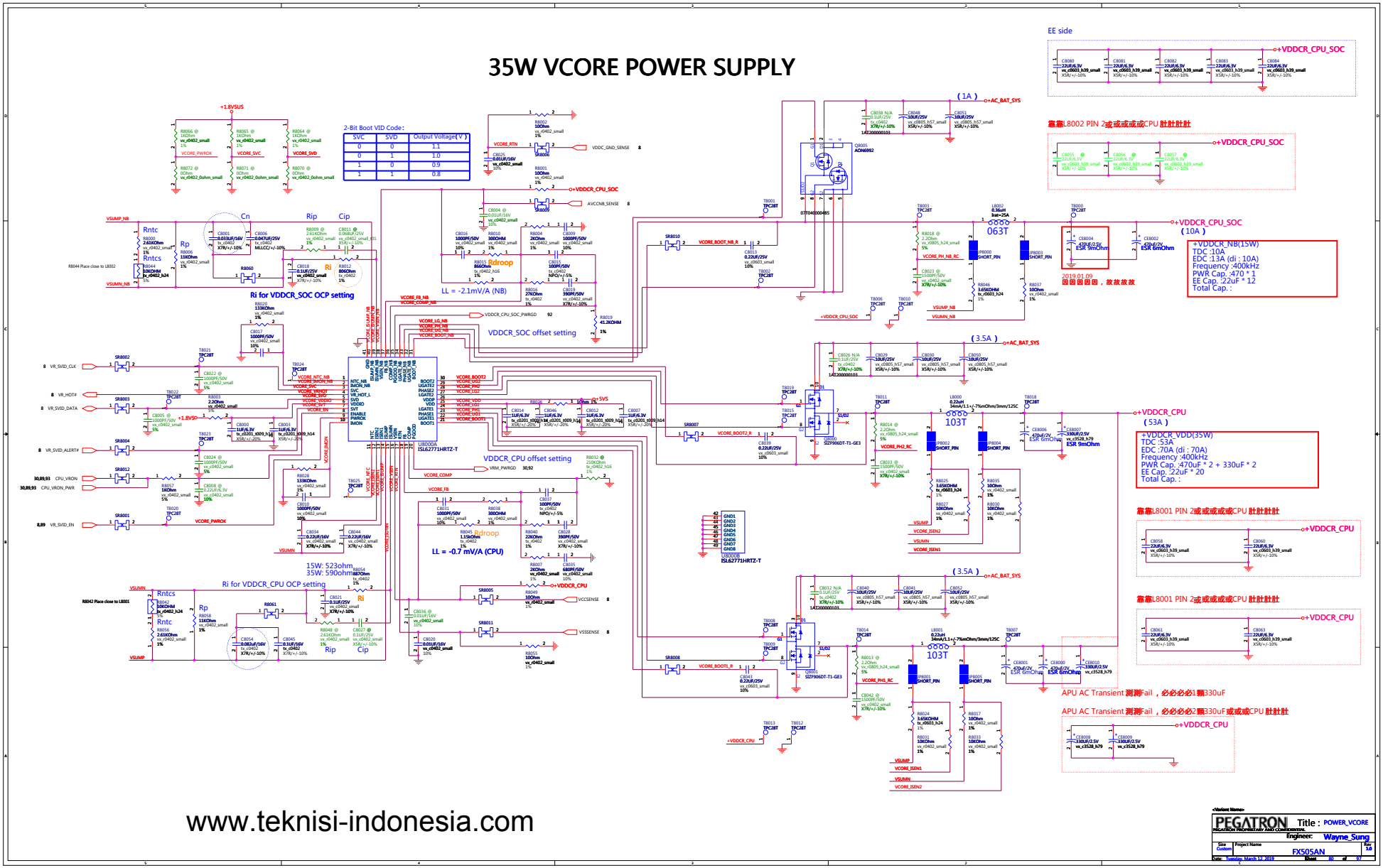

NVVDD Decoupling
NVVDD coupling : 1uF*93 + 10uF*23 + 22uF*4 + 47uF*3 + 470uF*2
PLACE UNDER GPU
PLACE NEAR GPU
Memory FBVDD/Q Decoupling
FBVDDQ coupling : 1uF*24 + 10uF*8 + 10uF*4 + 22uF*9
Partition A , PLACE UNDER GPU
Partition B , PLACE UNDER GPU
Partition C , PLACE UNDER GPU
Partition D , PLACE UNDER GPU
EMI requirement_20171011
1V8_AON coupling : 1uF*3 + 1uF*3 + 4.7uF*3
RF request
EMI request
PEGATRON
Title : NVDIA POWER
Engineer: Johnson Huang
Project Name: FX505DU
Rev: 1.0



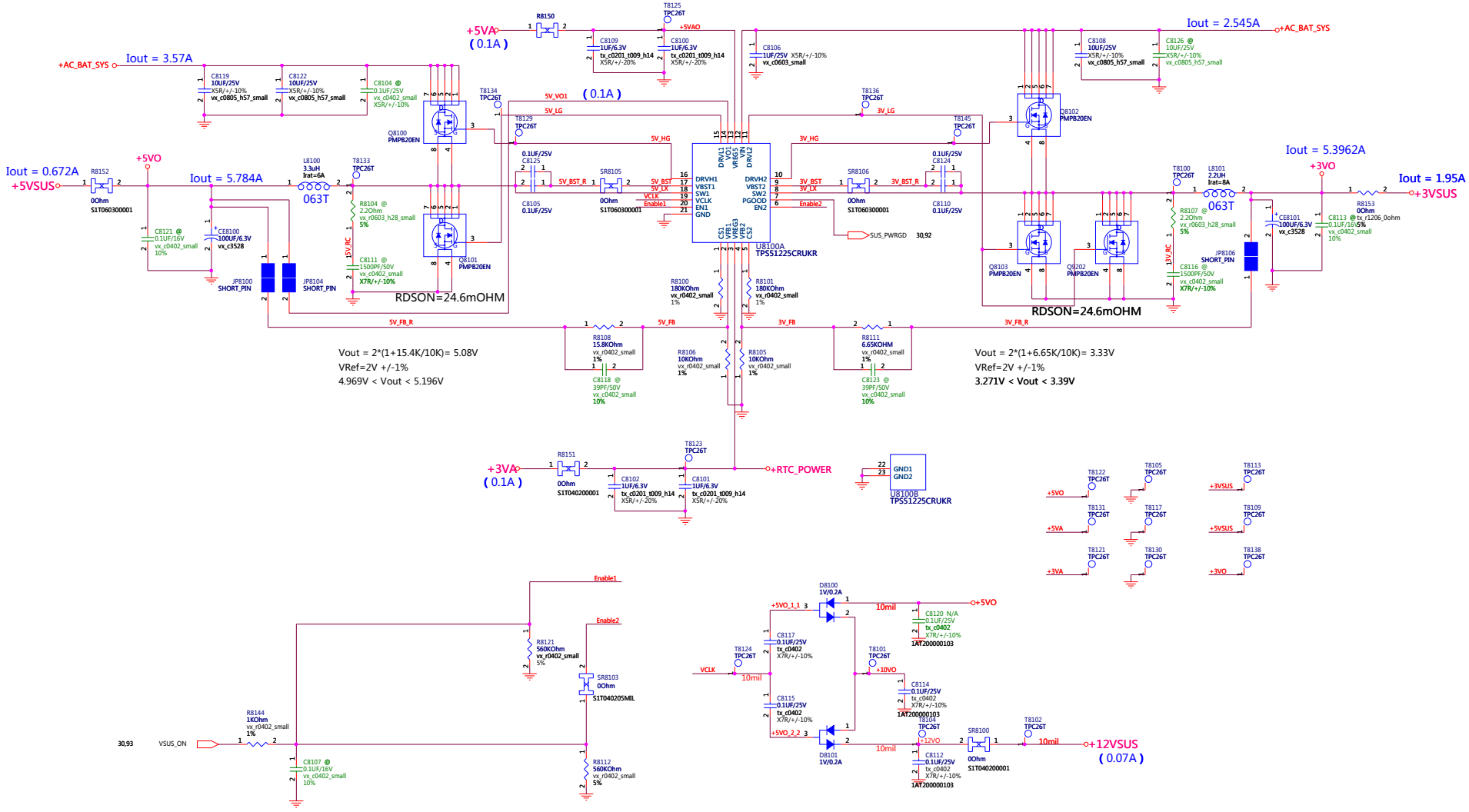
PEGATRON
Title : GDDR6 256M X32bit_A
Engineer: Johnson Huang


U7700A
NORMAL
U7700B
NORMAL
U7701A
NORMAL
U7701B
NORMAL
H56CBH24MJR-S2C
03T150027NGT
U7700D
U7700C
U7701D
U7701C
+FBVDDQ
+1V8_AON
VREFC
FBC_VREF_CA1
RESET_n
CK_c
CK_t
ZQ_A
ZQ_B
FBC_ZQ_1_A
FBC_ZQ_1_B
FBC_ZQ_2_A
FBC_ZQ_2_B
R7711 121OHM 1%
R7712 121OHM 1%
R7701 121OHM 1%
R7702 121OHM 1%
R7714 549Ohm 1%
R7703 1KOhm 1%
C7714 820PF/50V
GND
Close to DRAM
UNDER DRAM
Around DRAM
C7719 10UF/6.3V
C7727 10UF/6.3V
C7728 10UF/6.3V
C7731 10UF/6.3V
C7737 4.7UF/6.3V
C7703 1UF/6.3V
C7707 1UF/6.3V
C7710 1UF/6.3V
C7718 1UF/6.3V
C7708 10UF/6.3V
C7783 10UF/6.3V
C7732 10UF/6.3V
C7782 10UF/6.3V
C7736 10UF/6.3V
C7780 10UF/6.3V
C7704 10UF/6.3V
C7709 10UF/6.3V
C7733 10UF/6.3V
C7781 10UF/6.3V
C7735 10UF/6.3V
C7775 10UF/6.3V
C7729 10UF/6.3V
C7784 10UF/6.3V
C7723 1UF/6.3V
C7726 1UF/6.3V
C7720 1UF/6.3V
C7722 1UF/6.3V
C7724 1UF/6.3V
C7721 1UF/6.3V
C7715 1UF/6.3V
C7717 1UF/6.3V
C7711 1UF/6.3V
C7713 1UF/6.3V
C7716 1UF/6.3V
C7712 1UF/6.3V
C7730 1UF/6.3V
C7734 1UF/6.3V
C7701 1UF/6.3V
C7702 1UF/6.3V
C7706 1UF/6.3V
C7705 1UF/6.3V
C7755 10UF/6.3V
C7762 10UF/6.3V
C7763 10UF/6.3V
C7766 10UF/6.3V
C7772 4.7UF/6.3V
C7740 1UF/6.3V
C7744 1UF/6.3V
C7747 1UF/6.3V
C7754 1UF/6.3V
C7745 10UF/6.3V
C7773 10UF/6.3V
C7767 10UF/6.3V
C7778 10UF/6.3V
C7771 10UF/6.3V
C7777 10UF/6.3V
C7764 10UF/6.3V
C7776 10UF/6.3V
C7770 10UF/6.3V
C7774 10UF/6.3V
C7768 10UF/6.3V
C7779 10UF/6.3V
C7741 10UF/6.3V
C7746 10UF/6.3V
C7759 1UF/6.3V
C7761 1UF/6.3V
C7756 1UF/6.3V
C7758 1UF/6.3V
C7760 1UF/6.3V
C7757 1UF/6.3V
C7751 1UF/6.3V
C7753 1UF/6.3V
C7748 1UF/6.3V
C7750 1UF/6.3V
C7752 1UF/6.3V
C7749 1UF/6.3V
C7765 1UF/6.3V
C7769 1UF/6.3V
C7738 1UF/6.3V
C7739 1UF/6.3V
C7743 1UF/6.3V
C7742 1UF/6.3V
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :GDDR6 256M X32bit_C
BG1-HW RD Div-2-HW RD Dept.2
Engineer: Johnson Huang
Size Custom
Project Name FX505DU
Rev 1.0
Date: Tuesday, March 12, 2019
Sheet 77 of 99

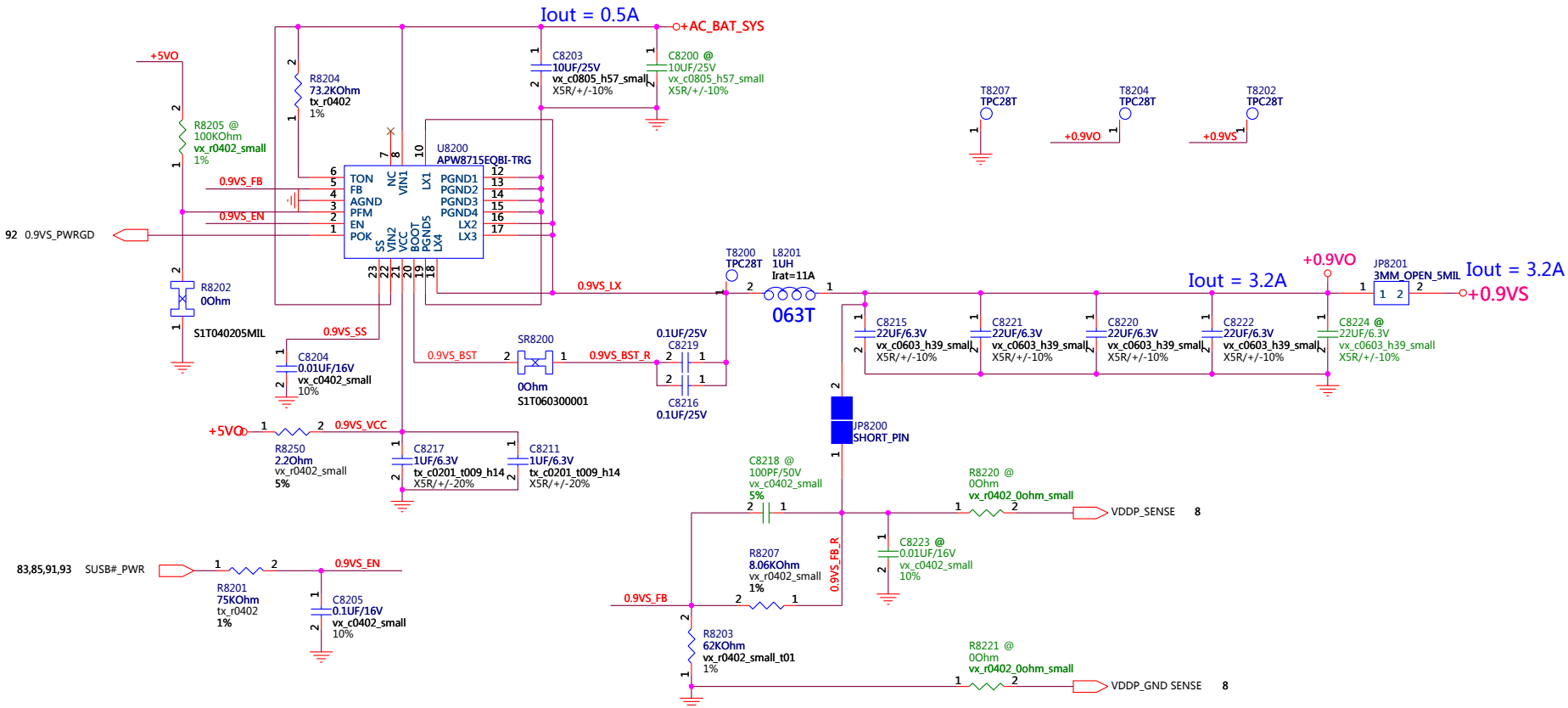
35W VCORE POWER SUPPLY



5VO & 3VO POWER SUPPLY



0.9VS POWER SUPPLY



<Variant Name>

PEGATRON Title : +0.9VS

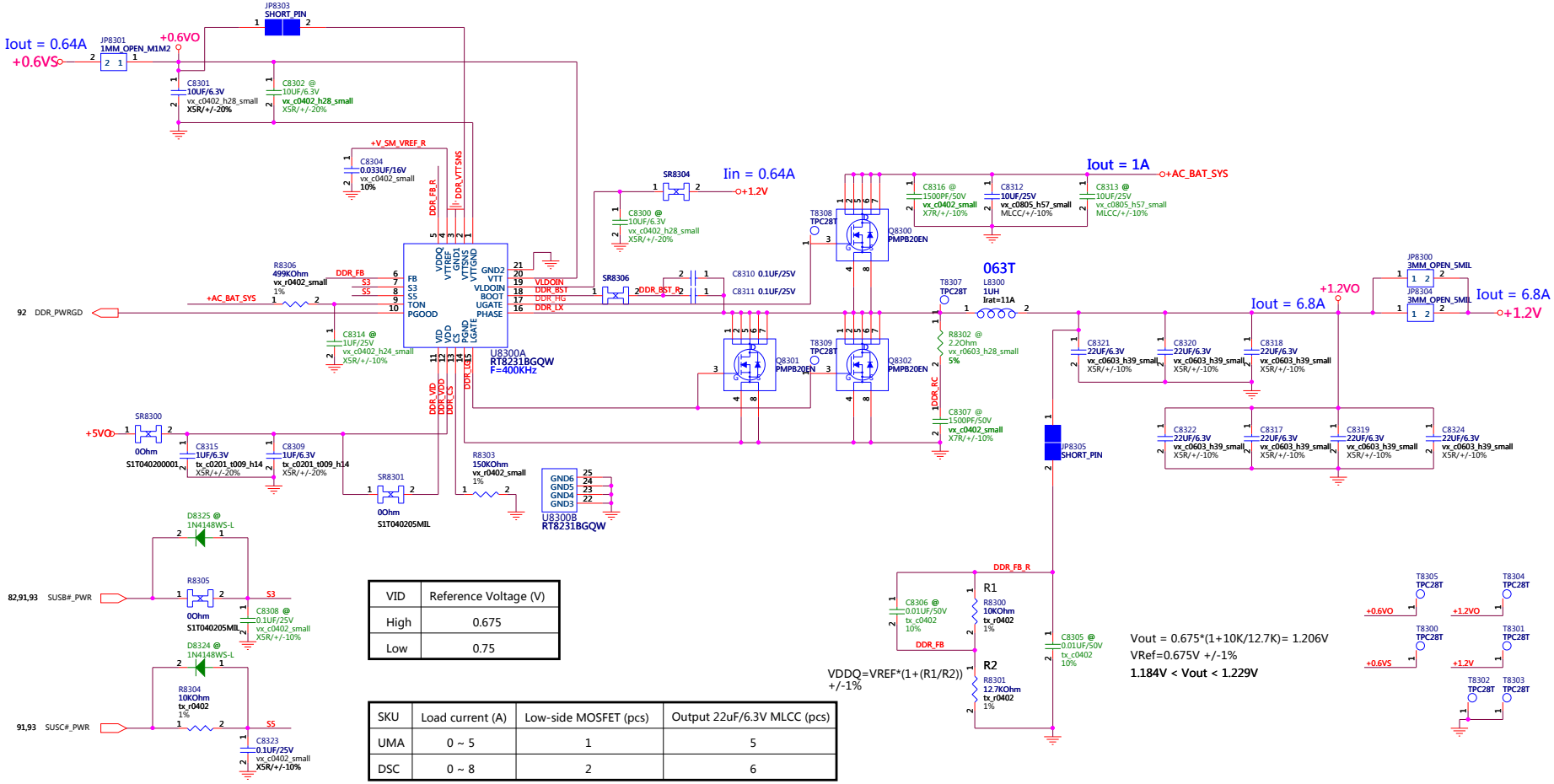
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Wayne_Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 82 of 97

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

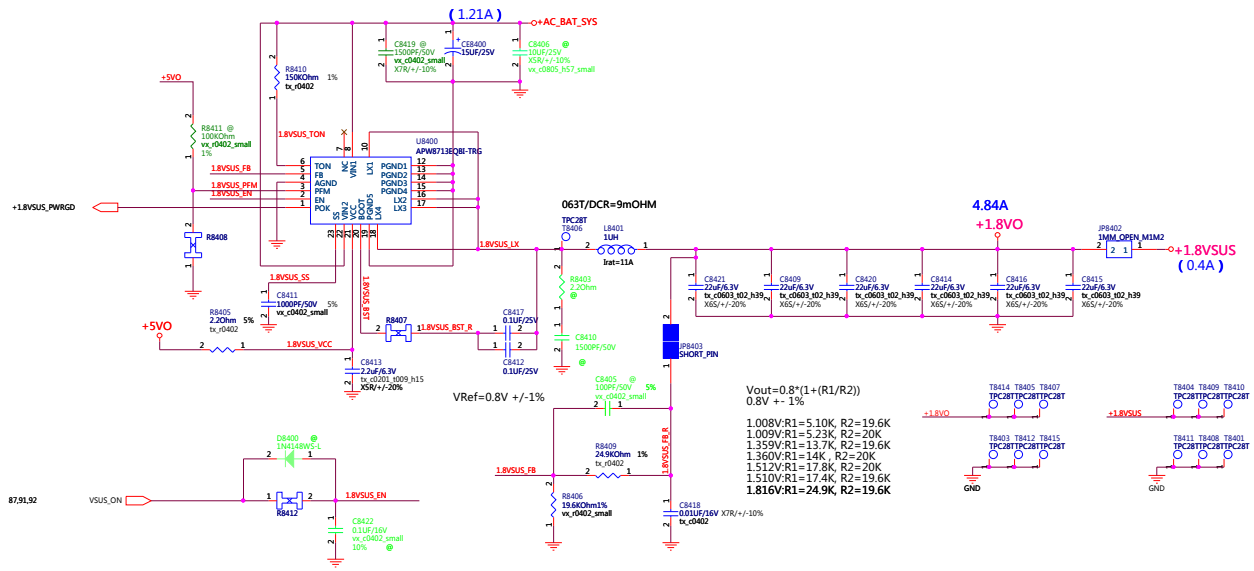
Title : POWER_DDR & VTT

Engineer: Wayne_Sung

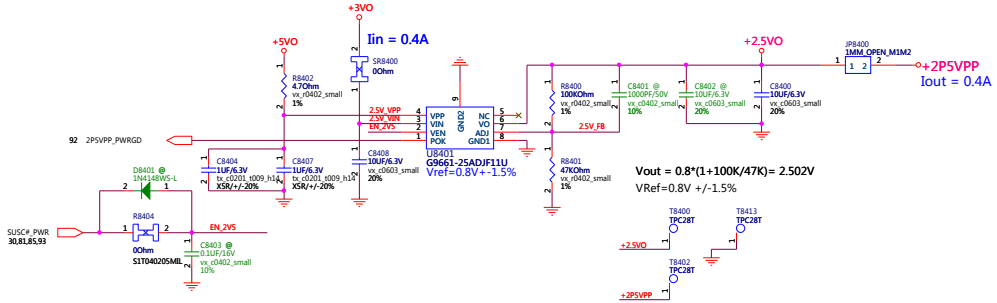
Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 83 of 97

1.8VSUS POWER SUPPLY



2.5VO POWER SUPPLY



PEGATRON Title : POWER_+1.8VSUS_2.5V
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp. Engineer: Wayne Sung
Size: C | Project Name: FX505AN | Rev: 1.0
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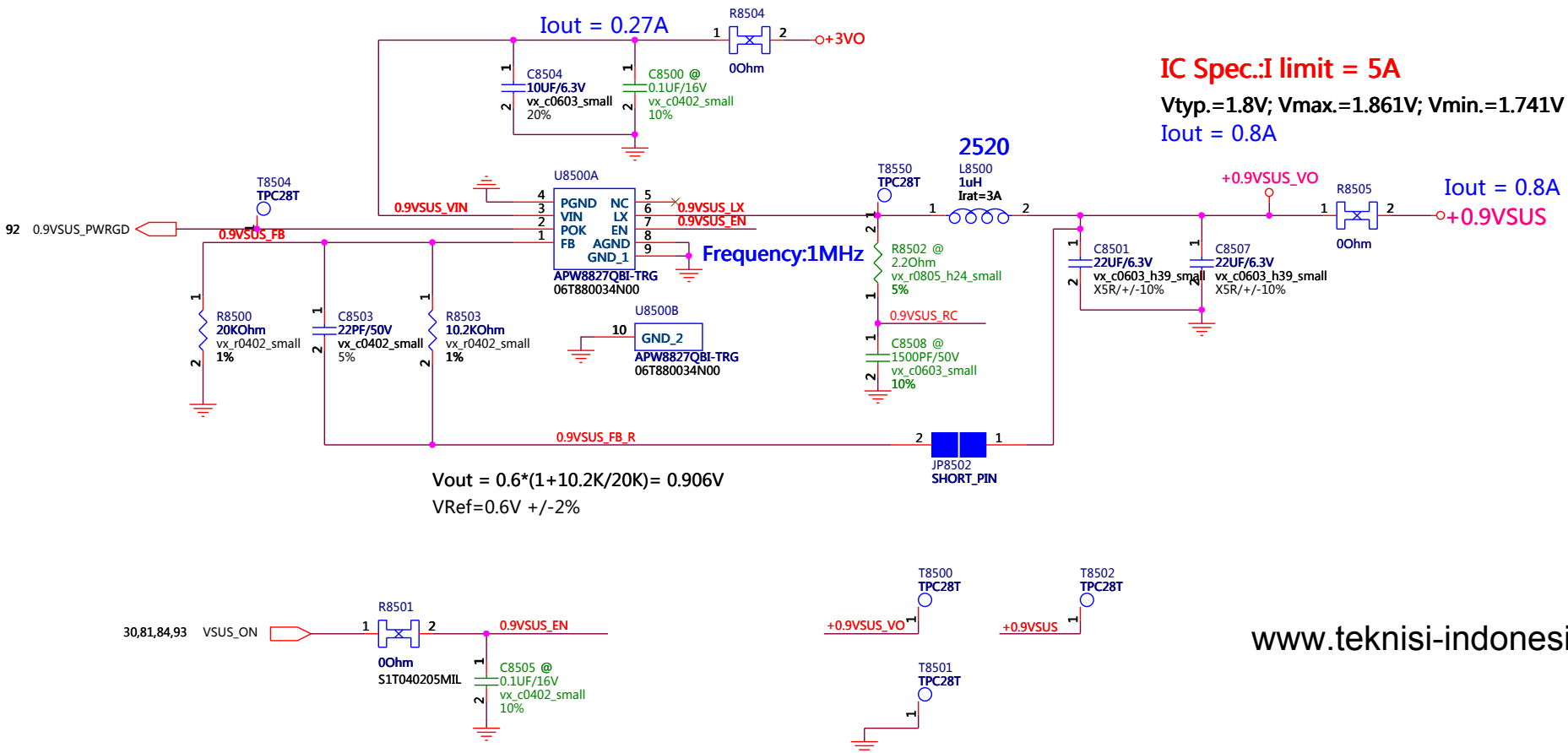
0.9VSUS POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_0.9VSUS

Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

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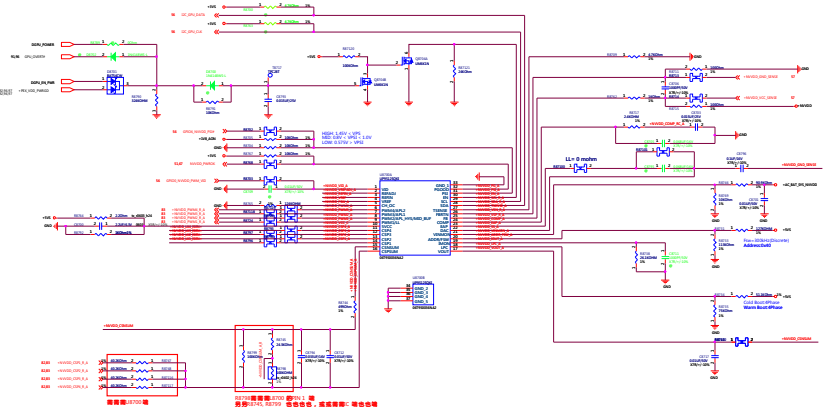
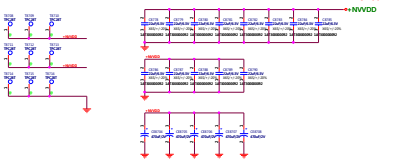
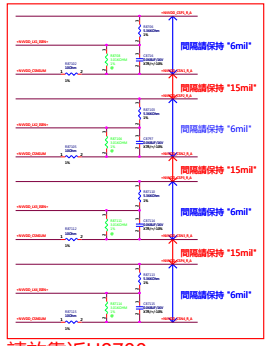


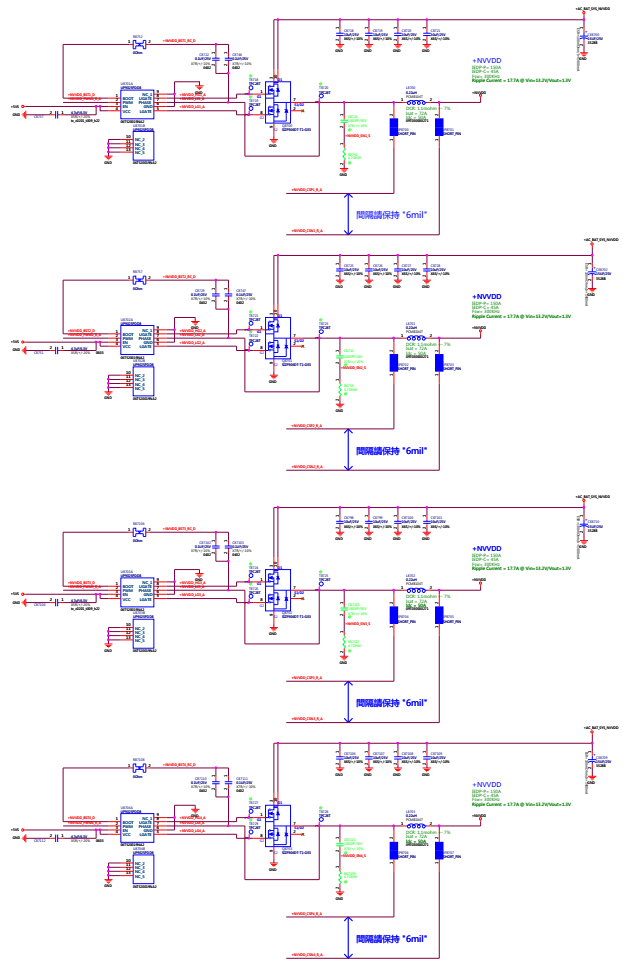
RB721	6.19K
RB718	20.5K
RB719	4.32K
RB722	16.5K
RB723	309
CB707	4.7nF
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV

EDP=225A 6uS
OCP:293A
TDC=80A

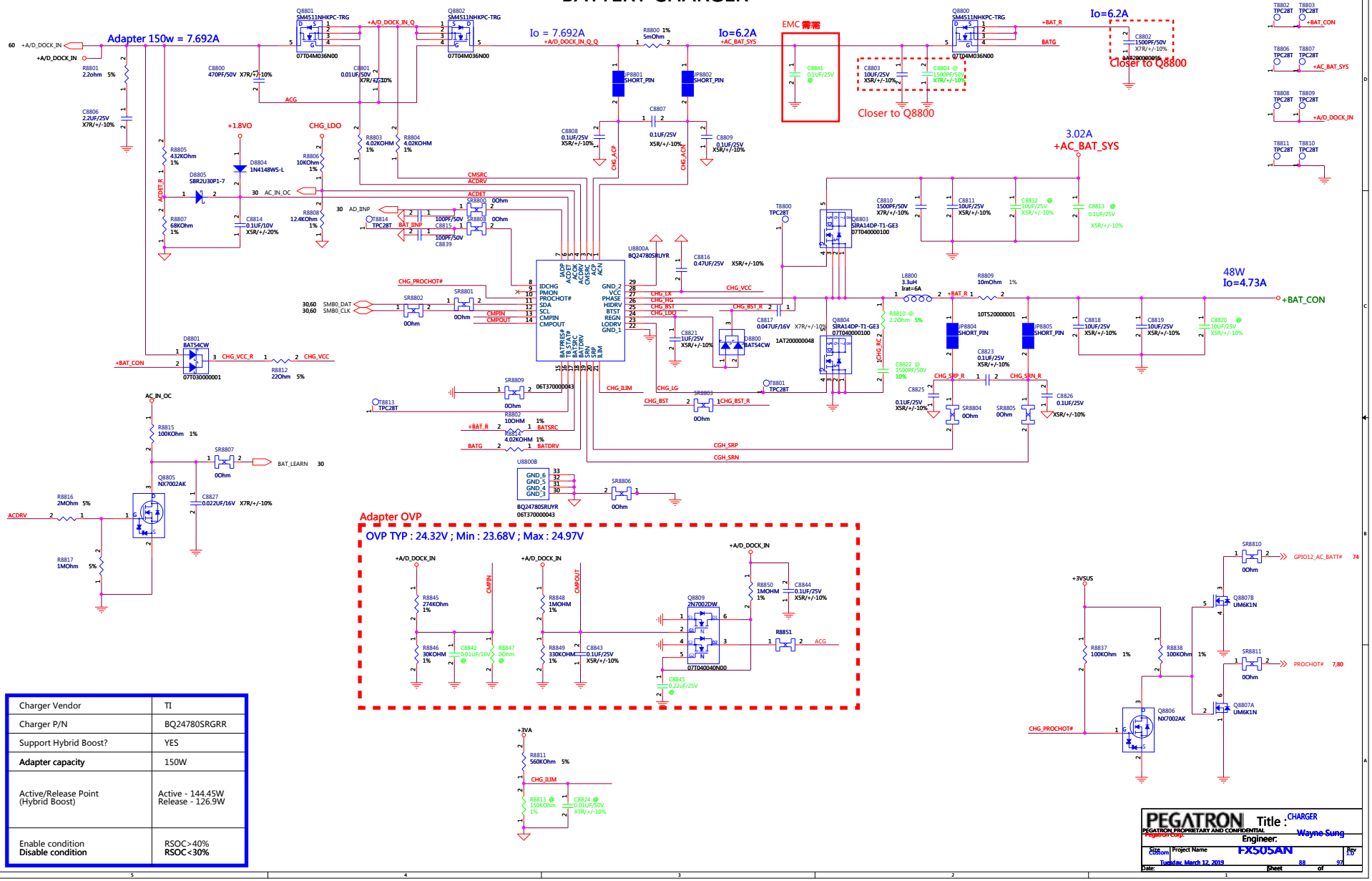




請放靠近U8700



BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	150W
Active/Release Point (Hybrid Boost)	Active - 144.45W Release - 126.9W
Enable condition **Disable condition**	RSOC>40% **RSOC<30%**

PEGATRON Title : CHARGER
PEGATRON CORP. PROPRIETARY AND CONFIDENTIAL
Engineer: Wayne Sung
Size: C Custom | Project Name: FX505AN | Rev: 1.0
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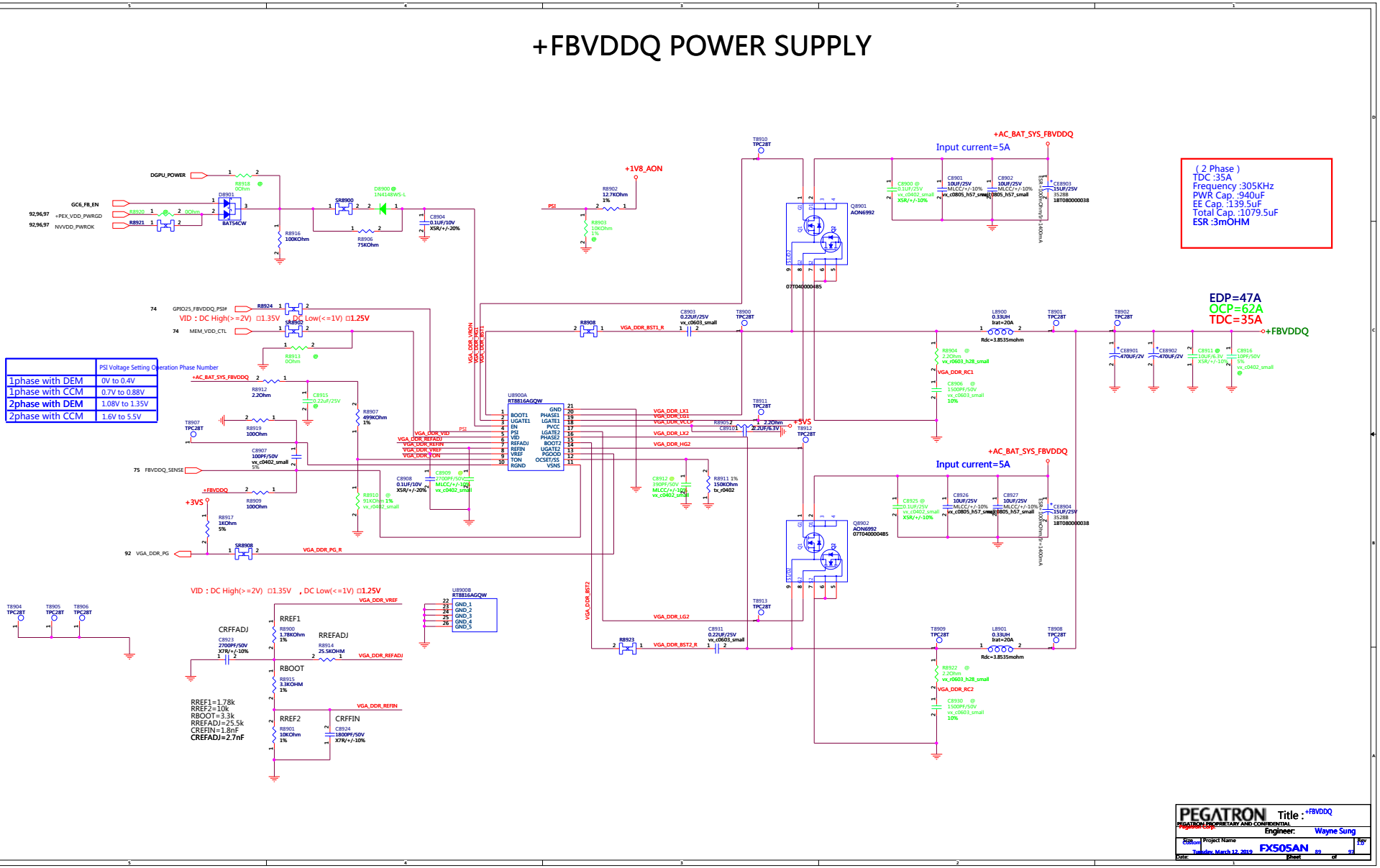
+FBVDDQ POWER SUPPLY



	PSI Voltage Setting Operation Phase Number
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : +FBVDDQ

Engineer: Wayne Sung

Size: Custom | Project Name: FX505AN | Rev: 1.0

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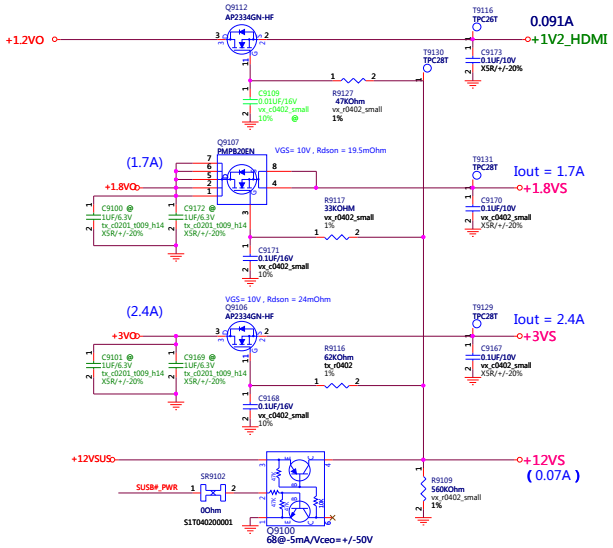
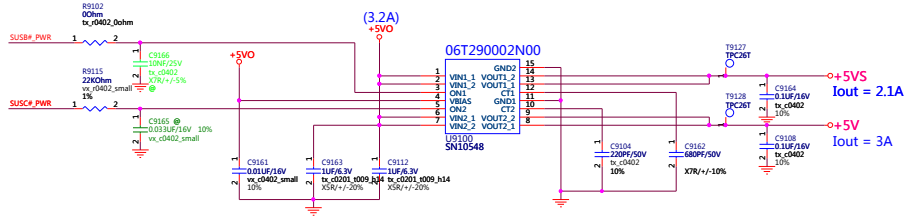
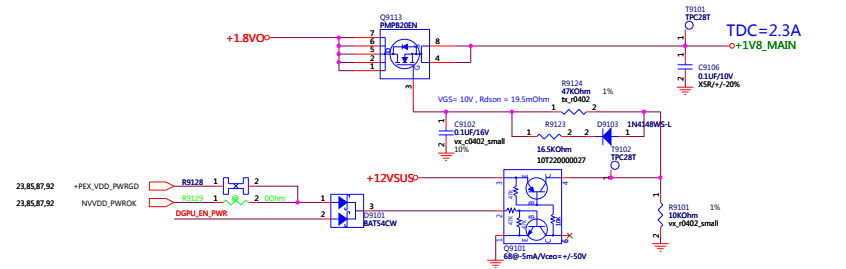
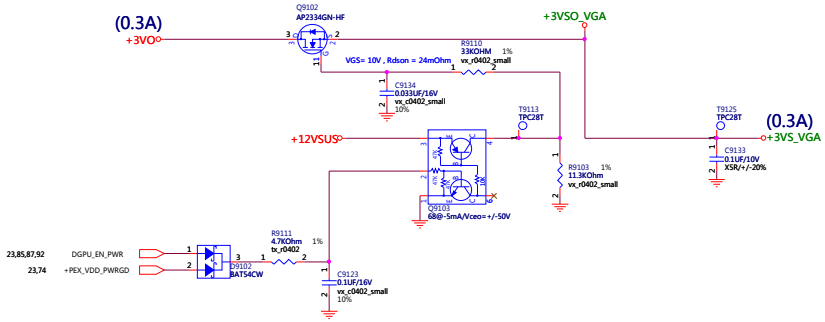
LOAD SWITCH

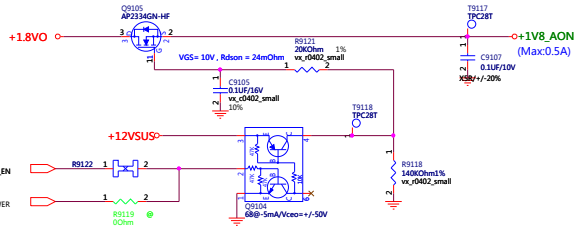




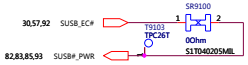


DSC_VGA_PWR POWER

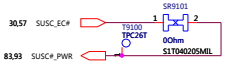




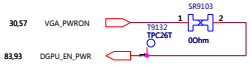
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_LOAD SWITCH

Pegatron Corp. Engineer: Wayne Sung

Size	Project Name	Rev
A2	FX505AN	1.0

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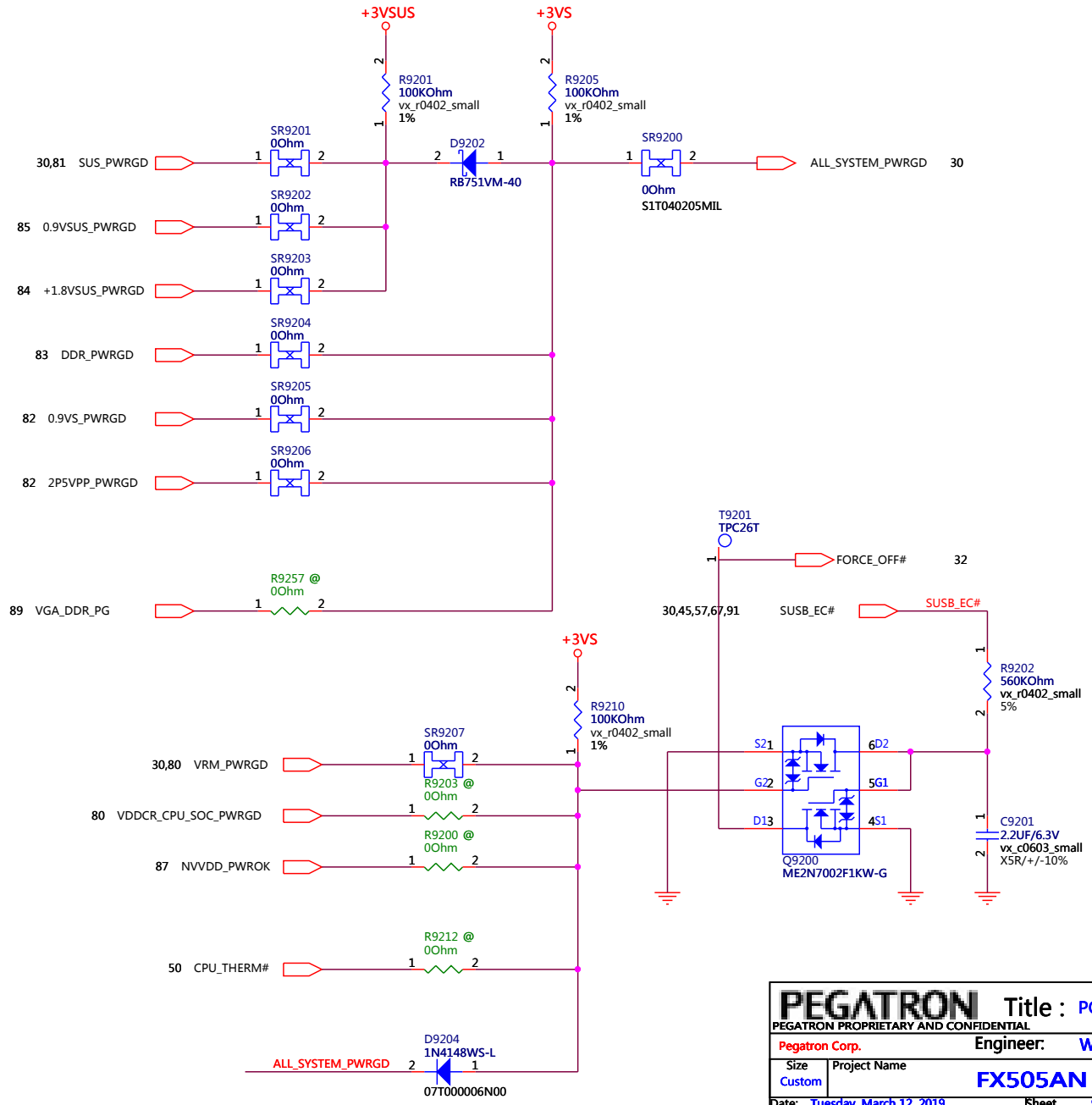
POWER GOOD DETECTER



PEGATRON Title : POWER_PROTECT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

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+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,88,89

+BAT_CON → +BAT_CON 60,88

+RTC_POWER → +RTC_POWER 81

+5VA → +5VA 56,66,81

+3VA → +3VA 11,28,30,56,57,60,66,81,88

+5VO → +5VO 81,83,85,89,91

+3VO → +3VO 81,84,85,89,91

+2.5VO → +2.5VO 83

+1.8VO → +1.8VO 84,85,91

+1.8VO_VGA → +1.8VO_VGA 83

+1.2VO → +1.2VO 83

+0.9VO → +0.9VO 83

+0.9VSUS_VO → +0.9VSUS_VO 83

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91

+5VSUS → +5VSUS 52,66,81

+3VSUS → +3VSUS 8,9,11,12,28,30,31,36,51,81,92

+1.8VSUS → +1.8VSUS 9,11,28,80,84,89

+0.9VSUS → +0.9VSUS 83

+12VS → +12VS 28,31,48,91

+5VS → +5VS 30,31,36,48,50,51,56,57,61,80,91

+3VS → +3VS 8,9,10,11,12,16,17,28,30,31,36,37,40,45,48,50,51,53,56,57,61,62,64,66,91,92

+1.8VS → +1.8VS 8,9,11,28,31,44,48,57,80,89,91

+0.6VS → +0.6VS 16,17,57,83

+3V → +3V 31,44,57,64,66,91

+1.2V → +1.2V 7,11,16,17,57,83

+2P5VPP → +2P5VPP 83

+1.8VS_VGA → +1.8VS_VGA 83

+1.35VS_VGA → +1.35VS_VGA 83

+VDDCI_VGA → +VDDCI_VGA 11,80,89

+VDDC_VGA → +VDDC_VGA 11,80,89

+VDDCR_CPU_SOC → +VDDCR_CPU_SOC 11,80

+VDDCR_CPU → +VDDCR_CPU 11,80

FOR POWER TEST

+3VA

JP9300 SGL_JUMP (1 2) → T9300 TPC28T → CPU_VRON_PWR 30,80,89

JP9301 SGL_JUMP (1 2) → T9301 TPC28T → SUSB#_PWR 82,83,85,91

JP9302 SGL_JUMP (1 2) → T9302 TPC28T → SUSC#_PWR 83,91

JP9303 SGL_JUMP (1 2) → T9303 TPC28T → VSUS_ON 30,81,84,85

JP9304 SGL_JUMP (1 2) → T9304 TPC28T → DGPU_POWER 89

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SIGNAL

Pegatron Corp.

Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

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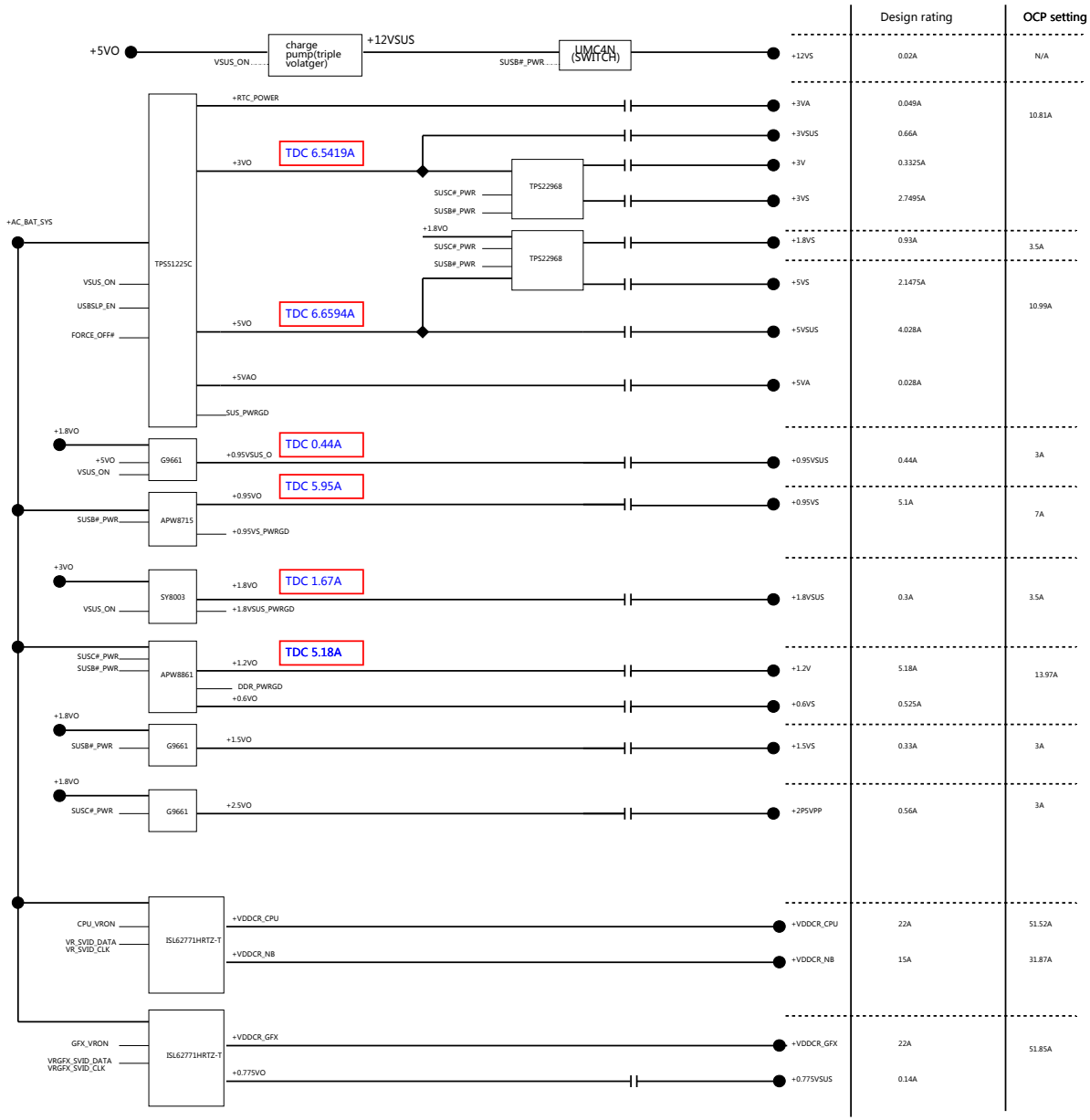
Design rating
OCP setting
+5VO
charge pump(triple volatger)
VSUS_ON
+12VSUS
SUSB#_PWR
LIMC4N (SWITCH)
+12VS
0.02A
N/A
+RTC_POWER
+3VA
0.049A
10.81A
+3VSUS
0.66A
TDC 6.5419A
+3VO
+3V
0.3325A
TPS22968
SUSC#_PWR
SUSB#_PWR
+3VS
2.7495A
+AC_BAT_SYS
+1.8VO
SUSC#_PWR
SUSB#_PWR
TPS22968
+1.8VS
0.93A
3.5A
TPS51225C
VSUS_ON
USBSLP_EN
FORCE_OFF#
+5VS
2.1475A
10.99A
TDC 6.6594A
+5VO
+5VSUS
4.028A
+5VAO
+5VA
0.028A
SUS_PWRGD
+1.8VO
TDC 0.44A
+0.95VSUS_O
+0.95VSUS
0.44A
3A
+5VO
VSUS_ON
G9661
TDC 5.95A
+0.95VO
+0.95VS
5.1A
7A
SUSB#_PWR
APW8715
+0.95VS_PWRGD
+3VO
TDC 1.67A
+1.8VO
+1.8VSUS
0.3A
3.5A
SY8003
VSUS_ON
+1.8VSUS_PWRGD
SUSC#_PWR
SUSB#_PWR
TDC 5.18A
+1.2VO
+1.2V
5.18A
13.97A
APW8861
DDR_PWRGD
+0.6VO
+0.6VS
0.525A
+1.8VO
SUSB#_PWR
G9661
+1.5VO
+1.5VS
0.33A
3A
+1.8VO
SUSC#_PWR
G9661
+2.5VO
+2P5VPP
0.56A
3A
CPU_VRON
VR_SVID_DATA
VR_SVID_CLK
ISL62771HRTZ-T
+VDDCR_CPU
+VDDCR_CPU
22A
51.52A
+VDDCR_NB
+VDDCR_NB
15A
31.87A
GFX_VRON
VRGFX_SVID_DATA
VRGFX_SVID_CLK
ISL62771HRTZ-T
+VDDCR_GFX
+VDDCR_GFX
22A
51.85A
+0.775VO
+0.775VSUS
0.14A
Title : POWER_SIGNAL
PEGATRON CONFIDENTIAL
Engineer: Wayne Sung
Pegatron Corp.
Size Custom
Project Name FX505AN
Rev 1.0
Date: Tuesday, March 12, 2019
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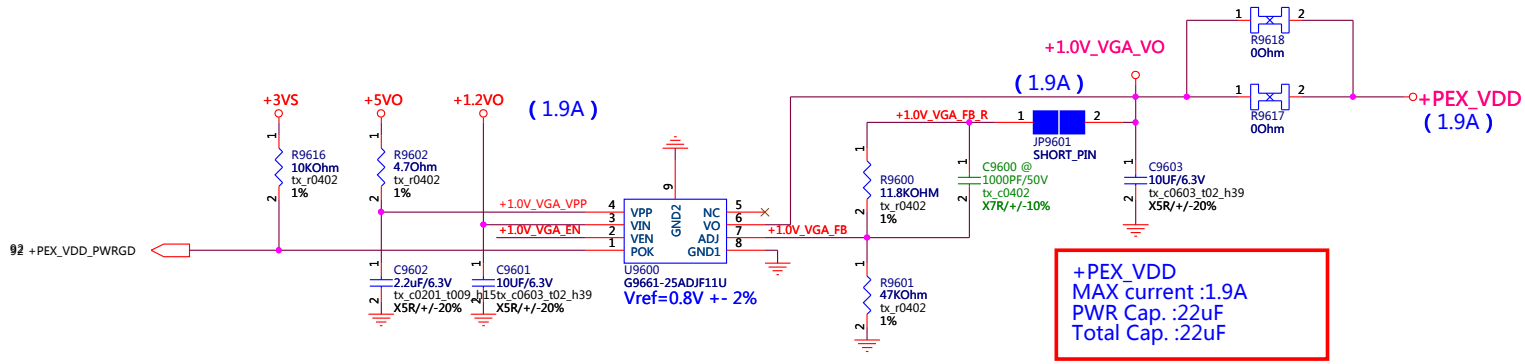
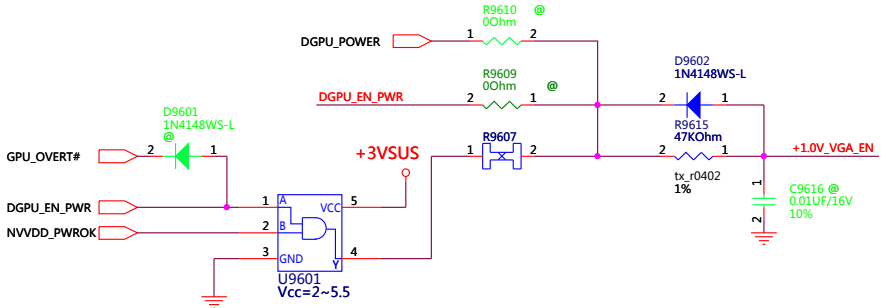
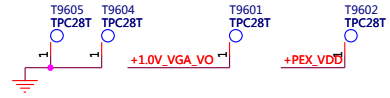
+PEX_VDD POWER SUPPLY







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +PEX_VDD

Engineer: Wayne Sung

Size	Project Name	Rev
B	FX505AN	1.0

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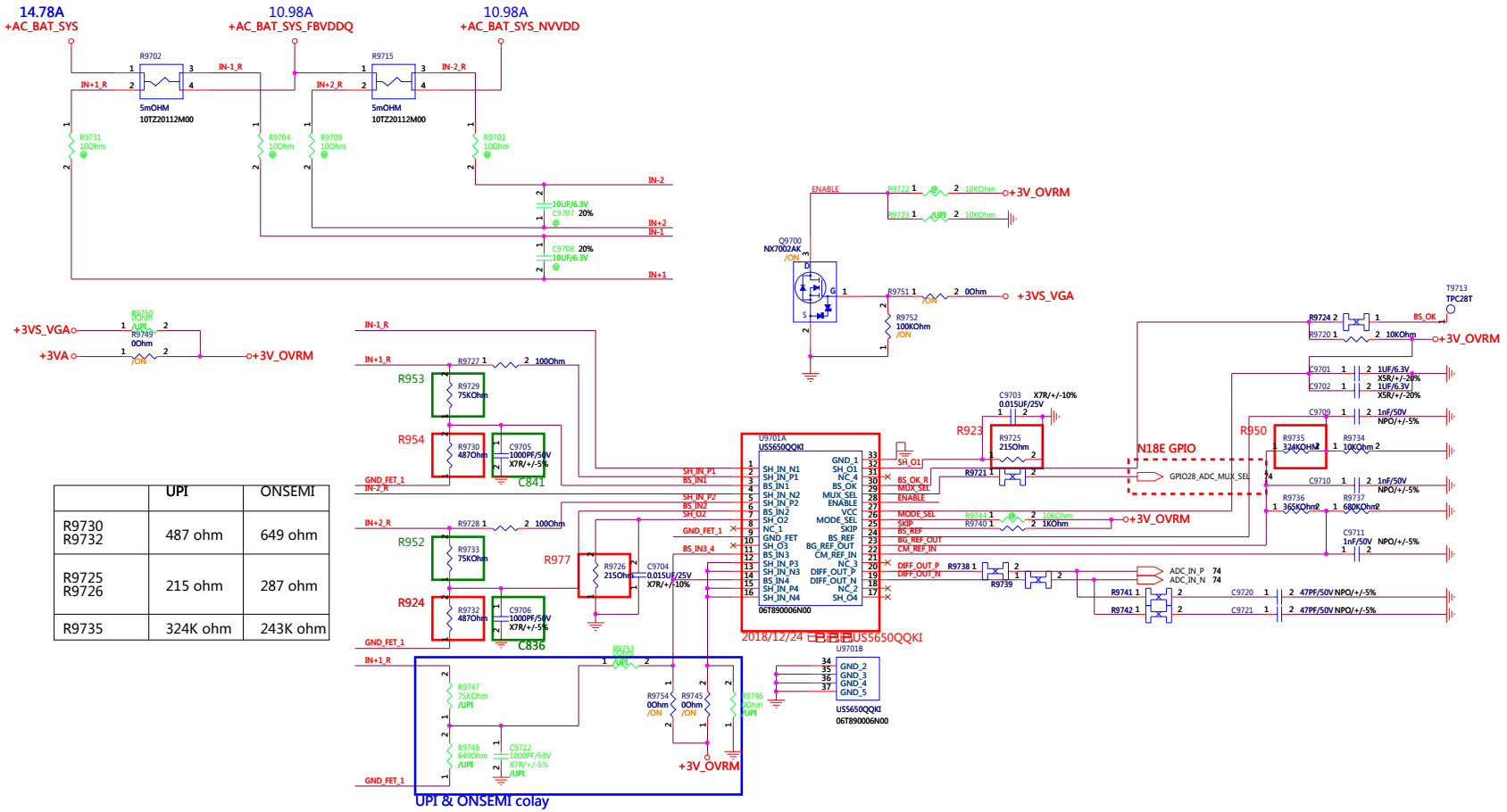
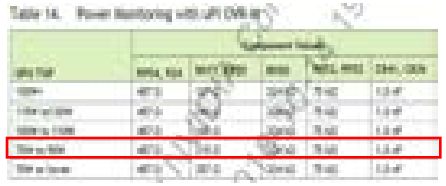


	UPI	ONSEMI
R9730 R9732	487 ohm	649 ohm
R9725 R9726	215 ohm	287 ohm
R9735	324K ohm	243K ohm



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +NVVDS
Engineer: Wayne Sung
Size: C
Project Name: FX505AN
Rev: 1.0
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20181026D

C0853~C0858 are changed to 0402

20181028A

Reserving R0960
PCIE_TX[N:P][9:11]_SSD_C are changed to PCIE_TX[N:P][1:3]_SSD_C

20181031C

Add R7113-R7118
Remove CE7502
Add R3653, R3654

20181101A
Add R4403, R4408, R4412
memory swap
Delete test point on CON5103

20181101B
Add R2454
Add C5142, C5141
Add SATA/PCIE redriver on Page 51
Change R3653, R3654 to 0402

20181102
Add R5104
Change JRST2401 to jumper
Delete R2409

20181105
Change R3634, R3632, R3619 to TX
Change C5144, C5145 to 0.47uF
Add R5116, R5117
Remove SATA signals to SSD

20181105
D3101 swap

20181106
Remove SATA_DEVSLP

20181107
Remove H6527
Add L6003; Change the sequence of parts on smbus of battery

20181108
Modify for the circuit of GPU sense
HDMI and USB signals swap

20181109
Change C8106 from 0402 to 0603
Change PEXVDD JP to 0805 0ohm

20181112
RN7403 swap
Update power segment

20181113
Delete FBx_VREF_CA related circuit
Add Q3601, Q3602

20181114
Change D3611 to AGND

20181122
Change Q2802 to 12VS and be unmount

20181207
Change U5301 to 0603-001J000
Change R5723 to 33 ohm
Mounting R1107
Unmounting Q1102、Q1103、R1114、R1115
Change R0837 to 1Kohm
Add R2489, R2490, R0861
Rename FP_FUSE_GPU to +FP_FUSE_GPU

20181207
Unmount U5301, R5337

20181211
Update power schemtic 1211

20181217
Mount Q5704、Q5708、R5705、R5715、R5742
Change RTC_3V3_IN to +RTC_3V3_IN
Change 0ohm to short pad
Remove R7421

20181219
Remove D7405
Add R5205~R5210、C5225~C5230

20181224
Mount R5705, Q5701

20181226
Change INT of I2C of toucpad to level shifter

20181227
Change 0603 MLCC *1 to 0402 MLCC *2 for EMI/ME request
Change C0903 to 1000pF

20181228
Unmount R7455
Reserve C3015
Change C1147, C1149 to 10uF 0402; Remove C1139
Change R7215 to shortpad
Change R2425, R2453 to shortpad
Change R0914, R0915 to 4.7Kohm
Mount C3108, C3110

20190103
Change R7113-R7118 to T7101-T7106

20190104
Change R0860 to shortpad
Change R3623, R3102, R3118 to 5% component
Reserve C3016
Change C8731, C8737, C87104, C87112 to lower package

20190107
Delete T7101-T7106
Unmount Q7401
Change R2806, R2807, R2815, R2816 to 0 ohm; R2808, R2809, R2818, R2819 to 100 ohm

20190214
Mount Q2802
Mount R7414, unmount R7413

20190219
Change C2403, C2404 to 10pF
Change R2454 to shortpad

Title	<Title>	
Size B	Document Number FX505DU	Rev <RevCode>
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