Compal Confidential

LA-F881P Schematics Document

Intel Coffee Lake S with DDR4 + CNP + AMD GPU (R17M-P1-70)

AIO M/B

REV : 1.0

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Title: *Cover Page*		
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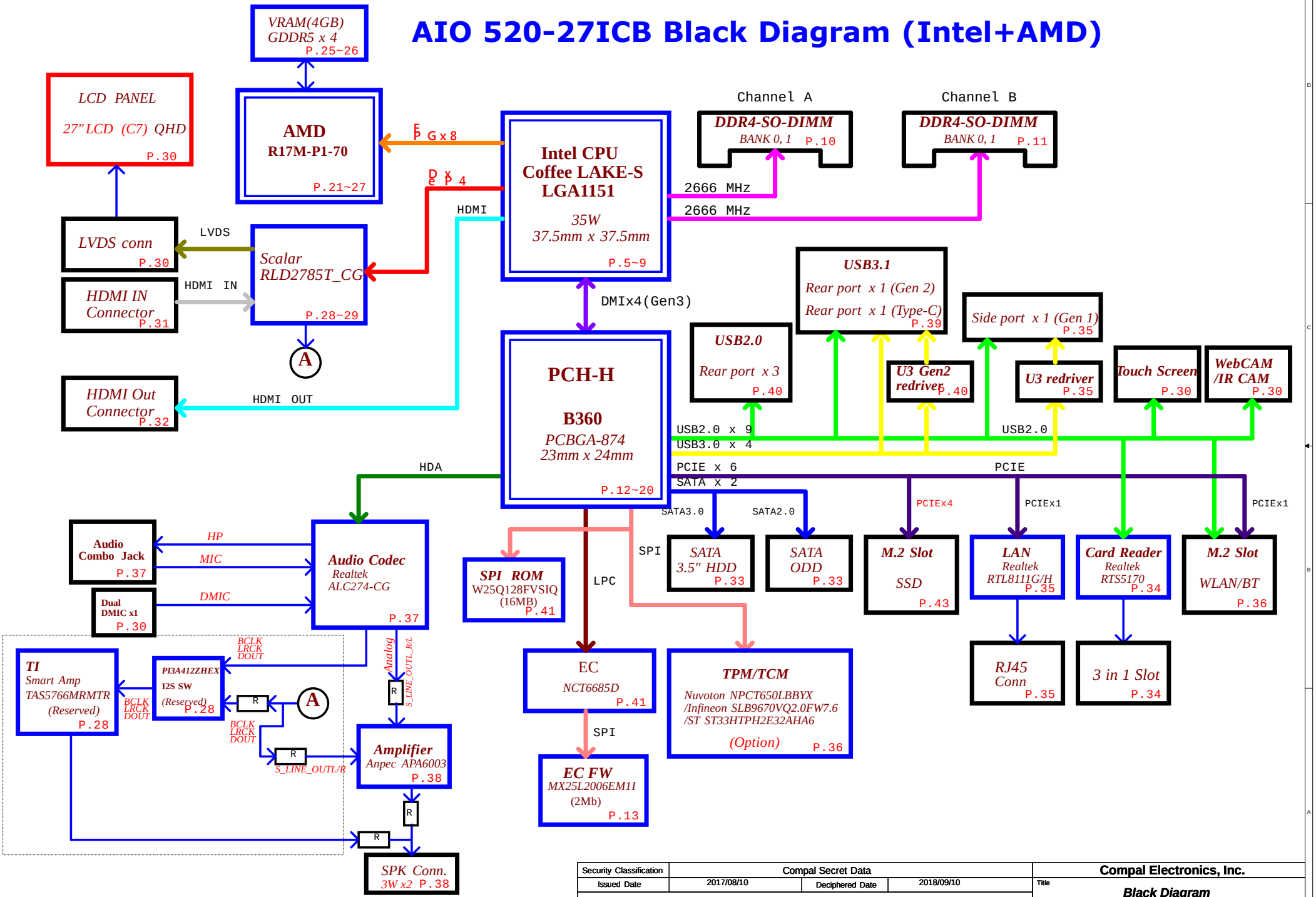
PCB Size : 201 mm x 240 mm

AIO 520-27ICB Black Diagram (Intel+AMD)



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Title	Black Diagram
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PCIE Port Table

No.	Port	Device
12	6	LAN
13	7	WLAN
27	21	SSD
28	22	SSD
29	23	SSD
30	24	SSD

SATA Port Table

No.	Port	Device
19	0	HDD
20	1	ODD

USB2.0 Port Table

Port	Device	OC# Pin
1	USB 2.0 Rear IO Port 2	OC#1
2		NA
3	USB 2.0 Rear IO Port 3	OC#1
4	USB 2.0/3.0 (Rear IO)	OC#2
5	USB 2.0/3.0 Rear IO(type C)	OC#2
6	USB 2.0/3.0 (IO Board)	OC#3
7	Web Camera	NA
8	Card Reader	NA
9	TOUCH	NA
10	WLAN/BT	NA

USB3.0 Port Table

No.	Port	Device
1	1	USB3.0 (Rear IO) (Gen2)
2	2	USB3.0 (IO Board)
3	3	USB 3.0 Rear IO (type C) (Gen1)
4	4	USB 3.0 Rear IO (type C) (Gen1)
5	5	NC
6	6	NC

DDI Port Table

No.	Port	Device
1	DDI1	HDMI OUT
2	DDI2	NC
3	DDI3	NC

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3 *
3	

SKU ID(Project) Table

SKU (UMA&DIS)	ECA70 (C7) 520-27IKL SIT BOM Configure Table
431ABJ38L01 (DIS) 451ABJ38L01 Micron_4G	
431ABJ38L02 (UMA) 451ABJ38L02	
431ABJ38L03 (DIS) 451ABJ38L03 Samsung_4G	
431ABJ38L04 (DIS) 451ABJ38L04 Hynix_4G	
X4EABJ38L01 (PS) (for LAN 8111G)	
X4EABJ38L02 (PS) (for LAN 8111H)	

BOM Structure Table

BOM Structure	Description

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DSW	3.3V DSW on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VALW_S5	12V always on power rail	ON	ON	ON
+1.8VS_S0	1.8V always on power rail	ON	OFF	OFF
+1.0VALW_S5	1.0V always on power rail	ON	ON	ON
+1.0V_VCCST_S3	1.0V power rail for CPU VCCST	ON	ON	OFF
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+CPU_VCCIO_S0	0.95V power rail for CPU VCCIO	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+1.05VS_S0	+1.5VS on power rail for CPU VCCSA	ON	OFF	OFF
+CPU_CORE	VCC Core voltage for CPU	ON	OFF	OFF
+VCC_GT_S0	Core voltage for CPU graphic	ON	OFF	OFF
+3VS_DGPU_S0	3.3V power rail for DIS graphic	ON	OFF	OFF
+VGA_CORE_S0	VCC Core voltage for GPU	ON	OFF	OFF
+1.05VS_DGPU_S0	1.05V power rail for DIS graphic	ON	OFF	OFF
+1.35VS_VGA_S0	1.35V power rail for VRAM	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus0 Address

Device	Address	HEX
Smart AMP DSP (TI)		0x9A
GPU (R17M-P1-70)		0x41

EC SM Bus2 Address

Device	Address	HEX
Scalar RTD2785T		0x94/0x95
LCD Backlight	0011 0001	31
Thermal Sensor	1001 101	4D

PCH SM Bus Address

Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

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Title: Notes List

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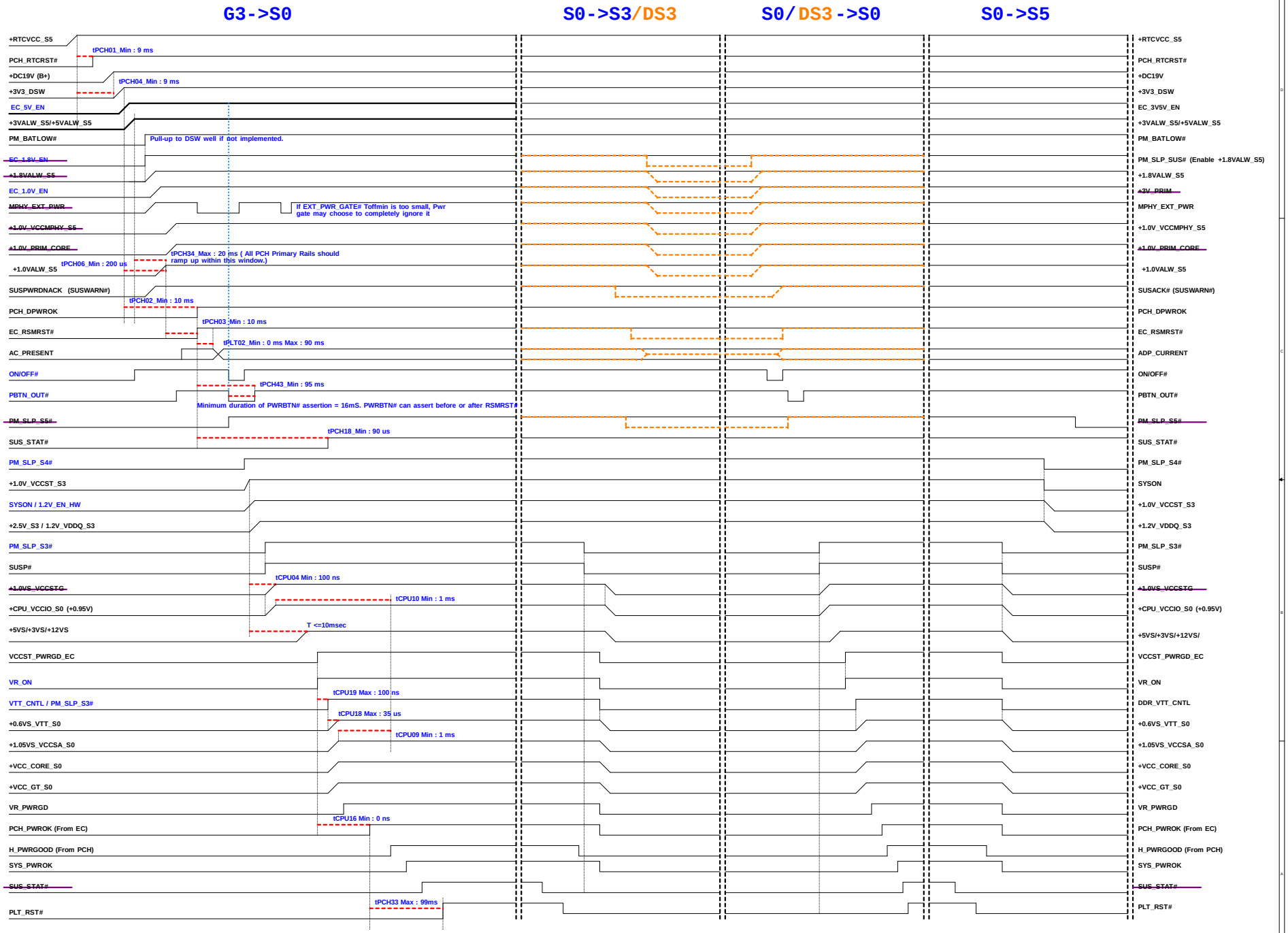
Power Sequence_SKL-S [Deep Sx Platform]



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Title: PWR Sequence

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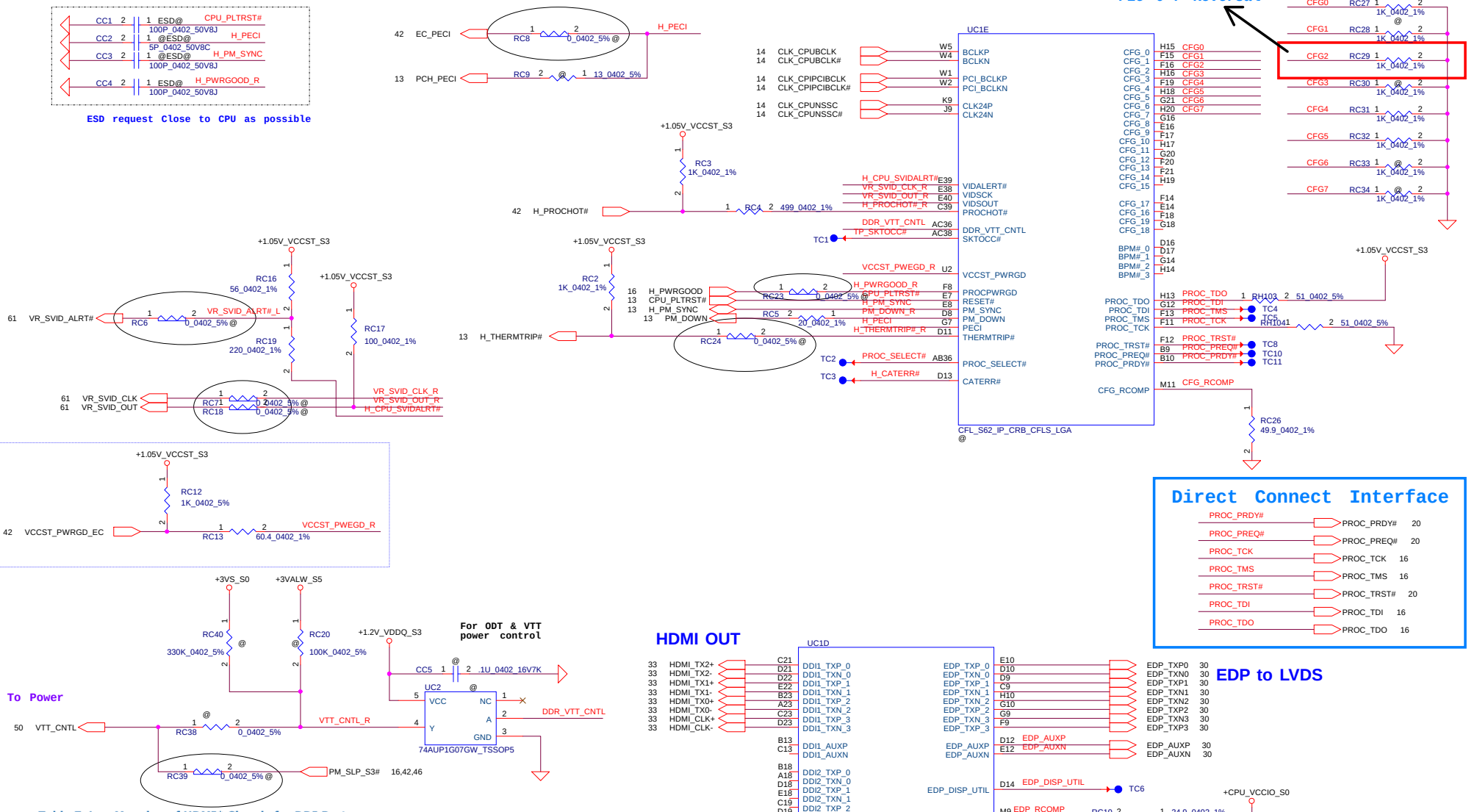

Table 7-1. Mapping of HDMI* Signals for DDI Ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA

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Title: *Skylake JTAG/XDP/DDI*

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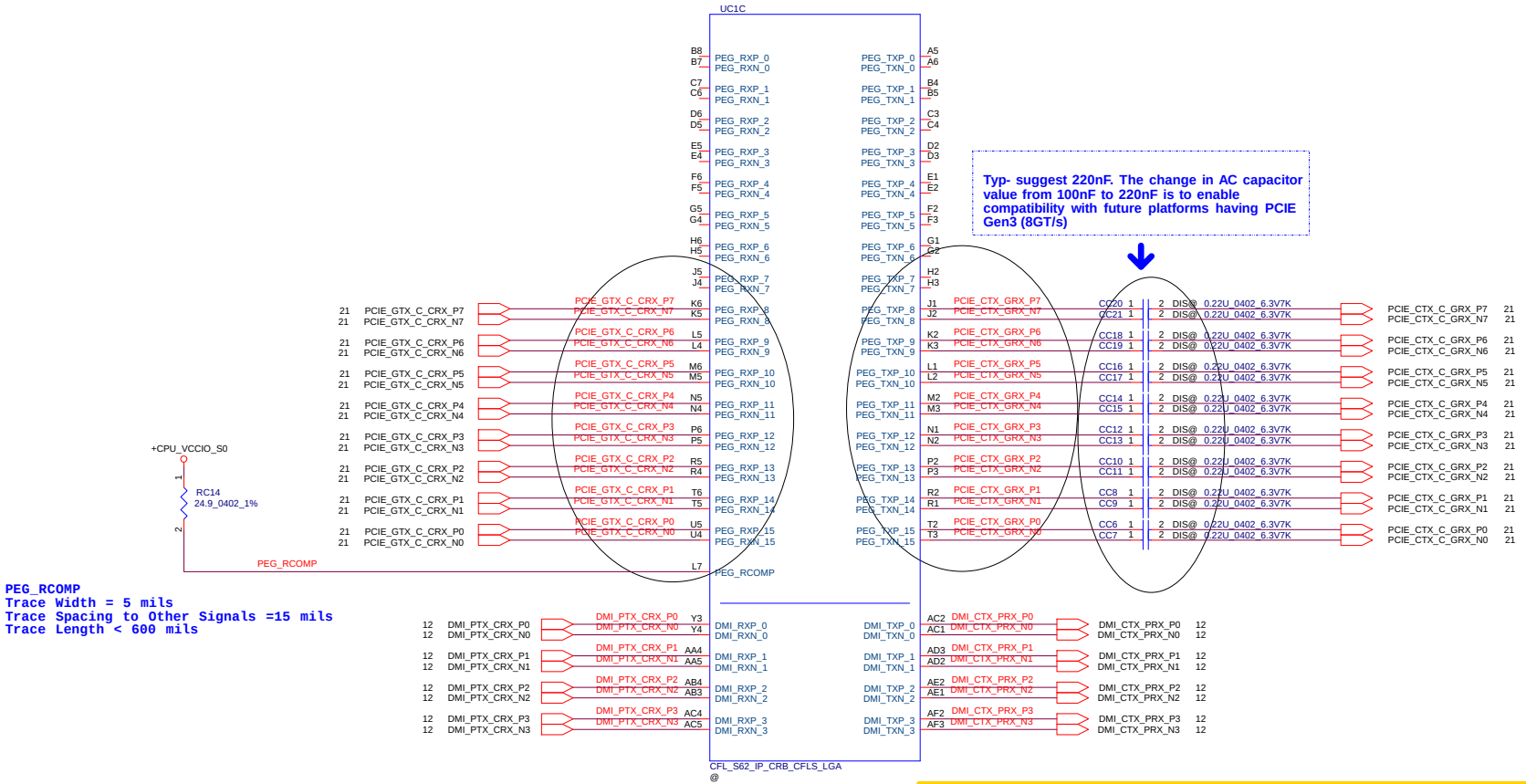
PCIE 8~15 LANE Reversal



Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

PEG_RCOMP
Trace Width = 5 mils
Trace Spacing to Other Signals =15 mils
Trace Length < 600 mils

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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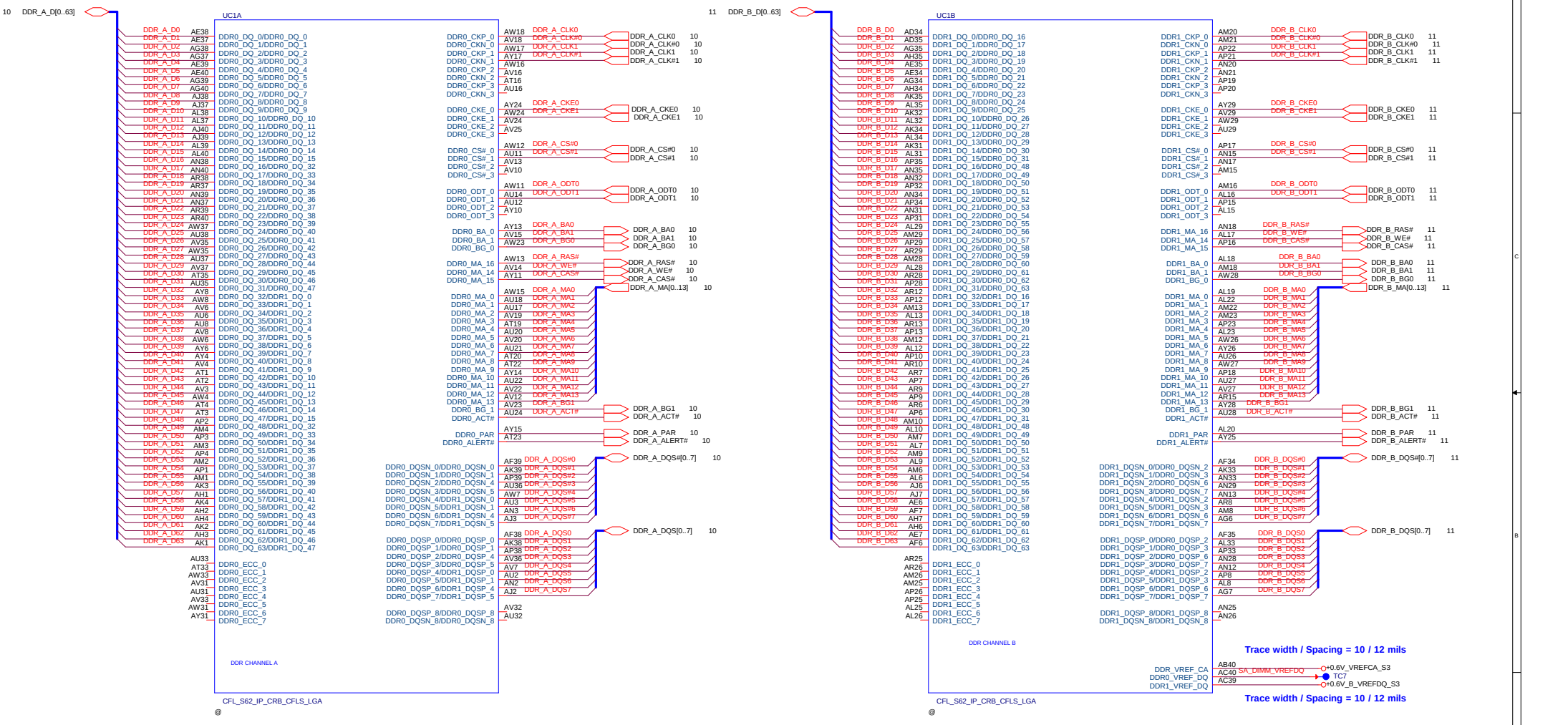

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Title: ***Skylake DDR4***

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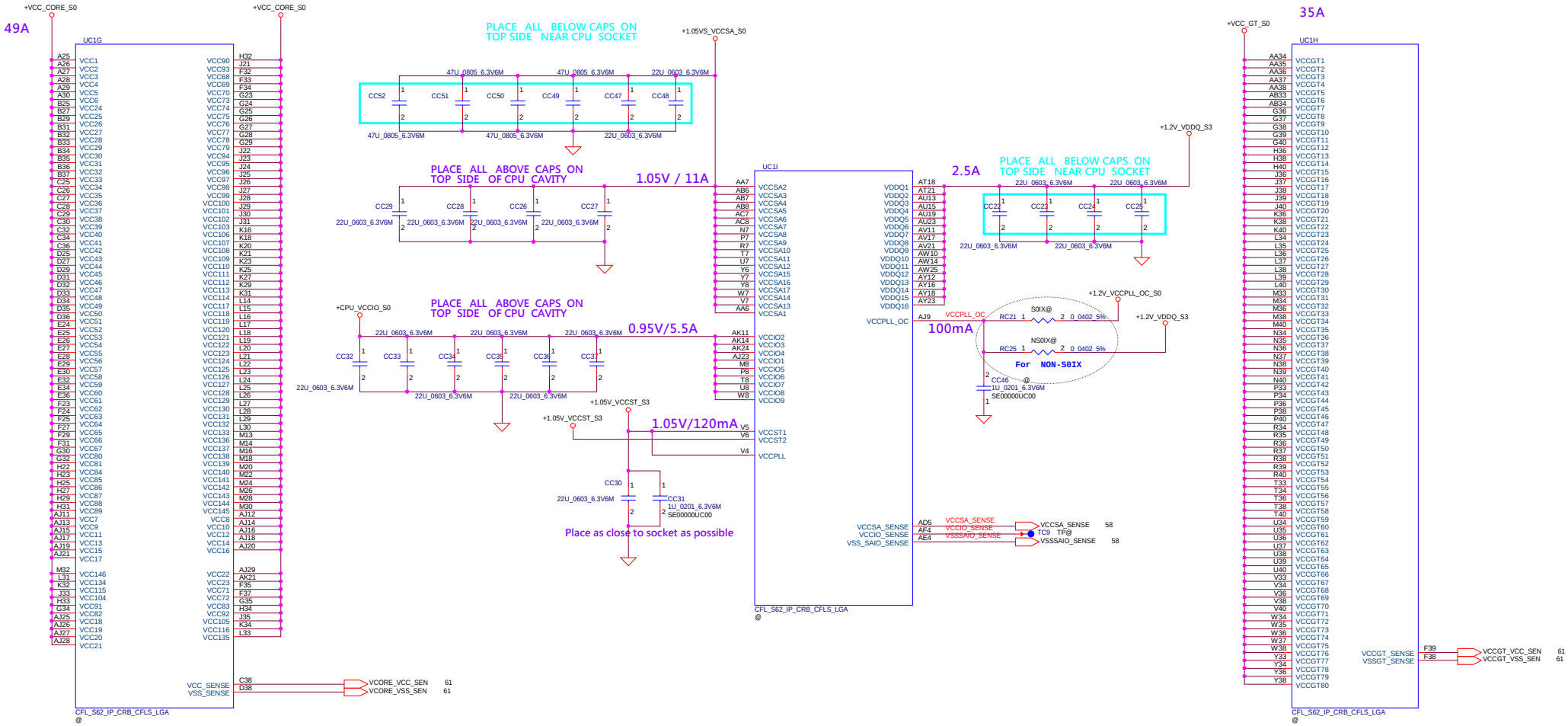
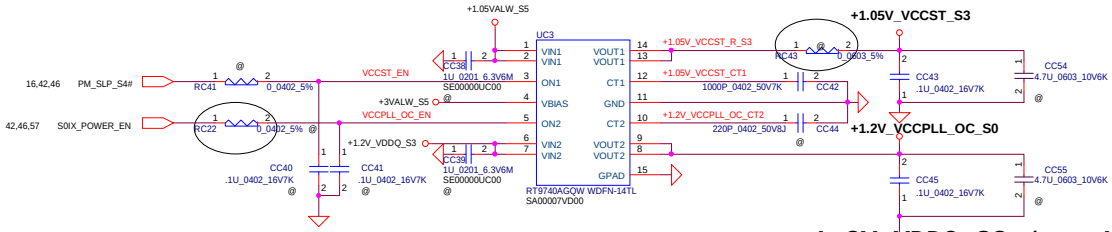


VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

+1.05VALW_S5 to +1.05V_VCCST



+1.2V_VDDQ_S3 to +1.2V_VCCPLL_OC

1st source : RT9740AGQW (SA00007VD00)
2nd source : xxxxxxx (xxxxxxx)

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Title	Skylake POWER
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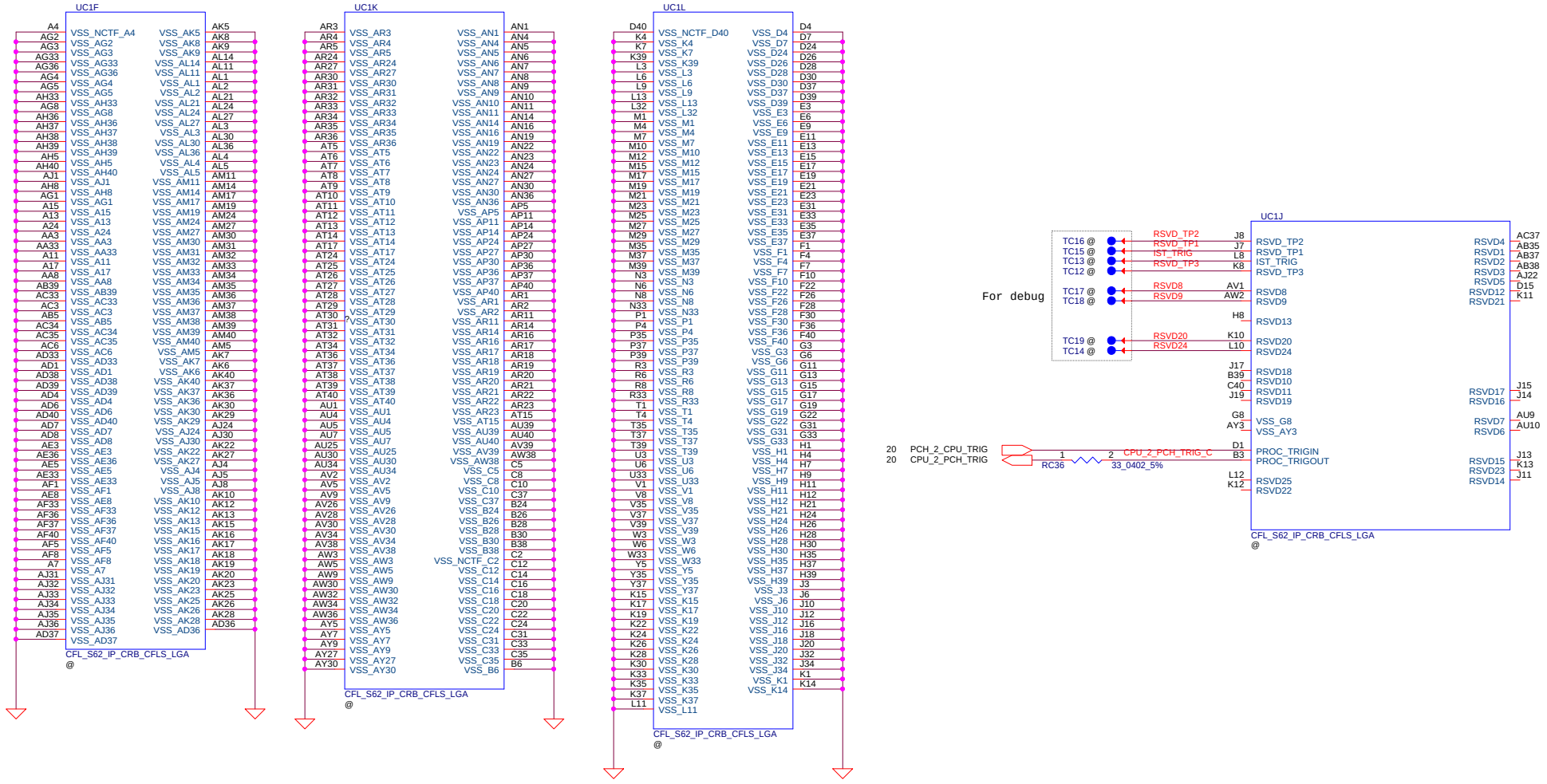

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Title: ***Skylake GND/RSVD***

Size	Document Number	Rev
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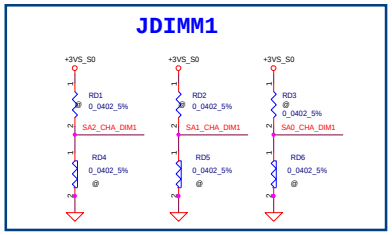
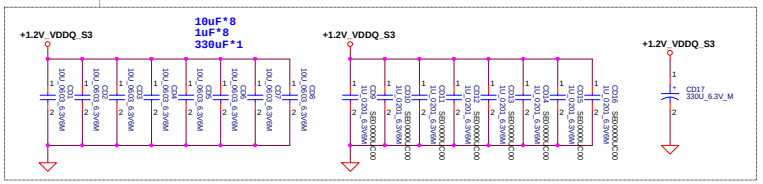
INTERLEAVE CHANNEL-A



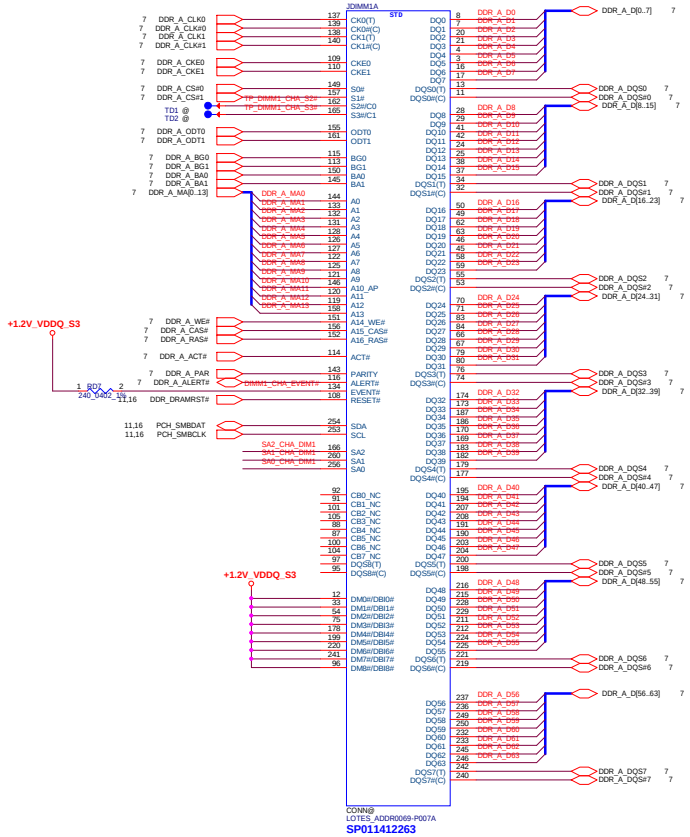
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

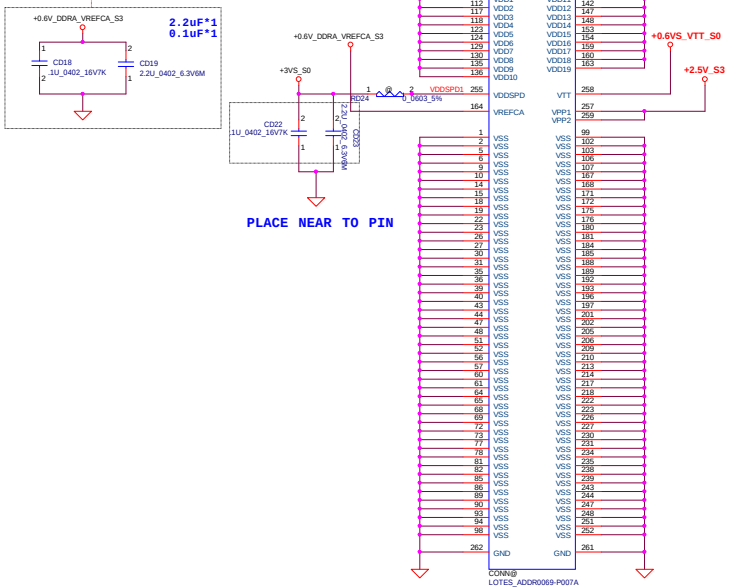
Layout Note:
Place near JDIMM1



(8.0 mm) STD

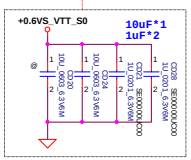


Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1

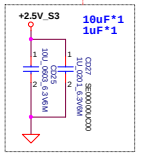


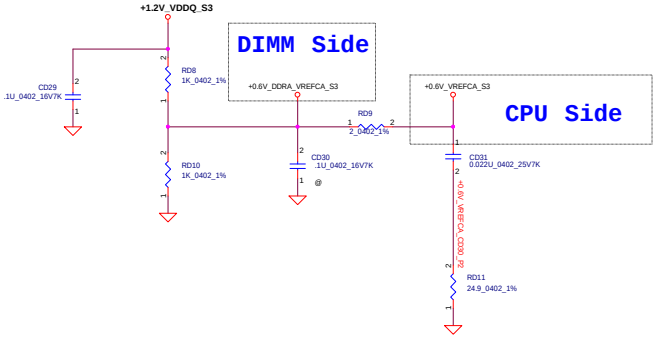
PLACE NEAR TO PIN

Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1





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Title: DDR4_DIMMA

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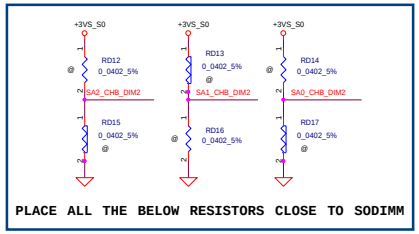
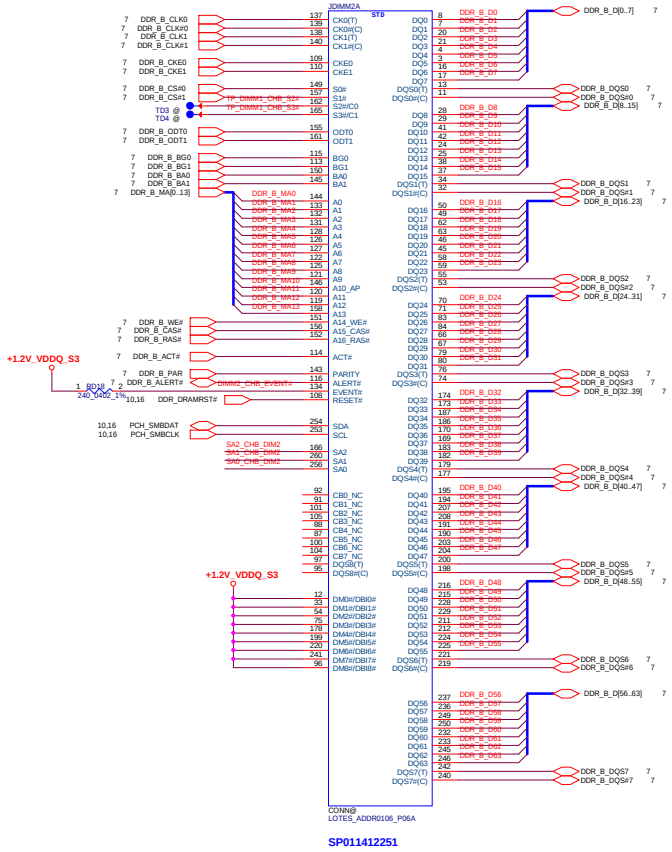
INTERLEAVE

CHANNEL-B



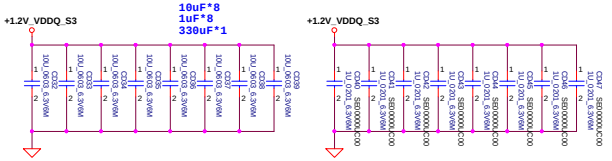
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:0xA4
READ ADDRESS: 0xA5
SA0 = 0, SA1 = 1. SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

(4.0 mm) STD

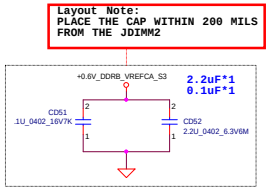


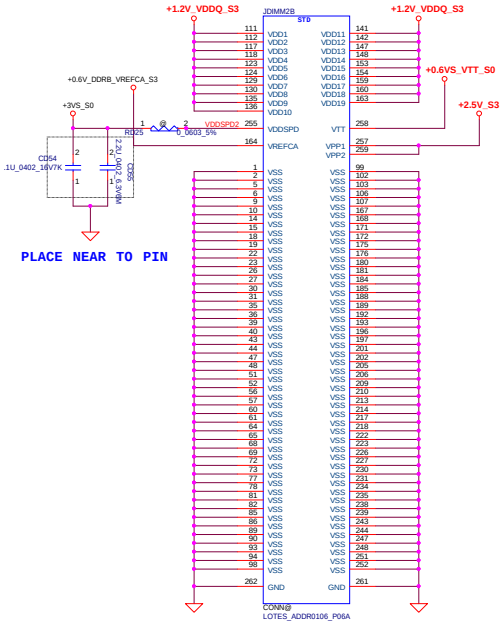
SP011412251

Layout Note:
Place near JDIMM2

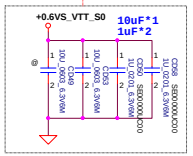


Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

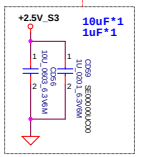


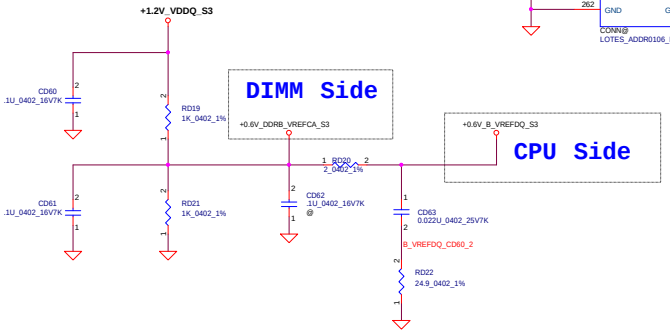


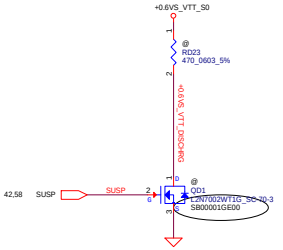
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2







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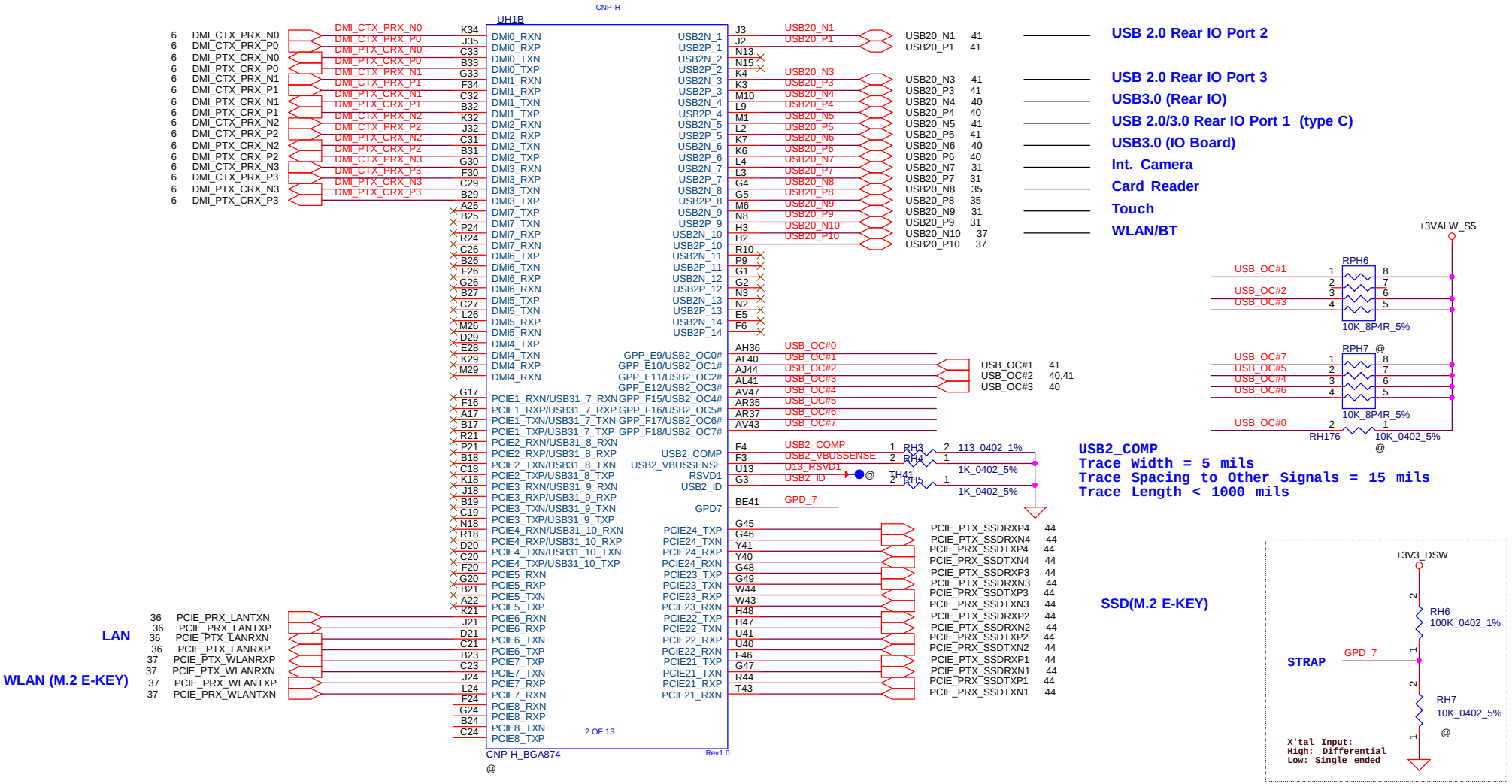

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Title: ***PCH_DMI/USB2/PCIE***

Size	Document Number	Rev
B	LA-F882P M/B	0.2

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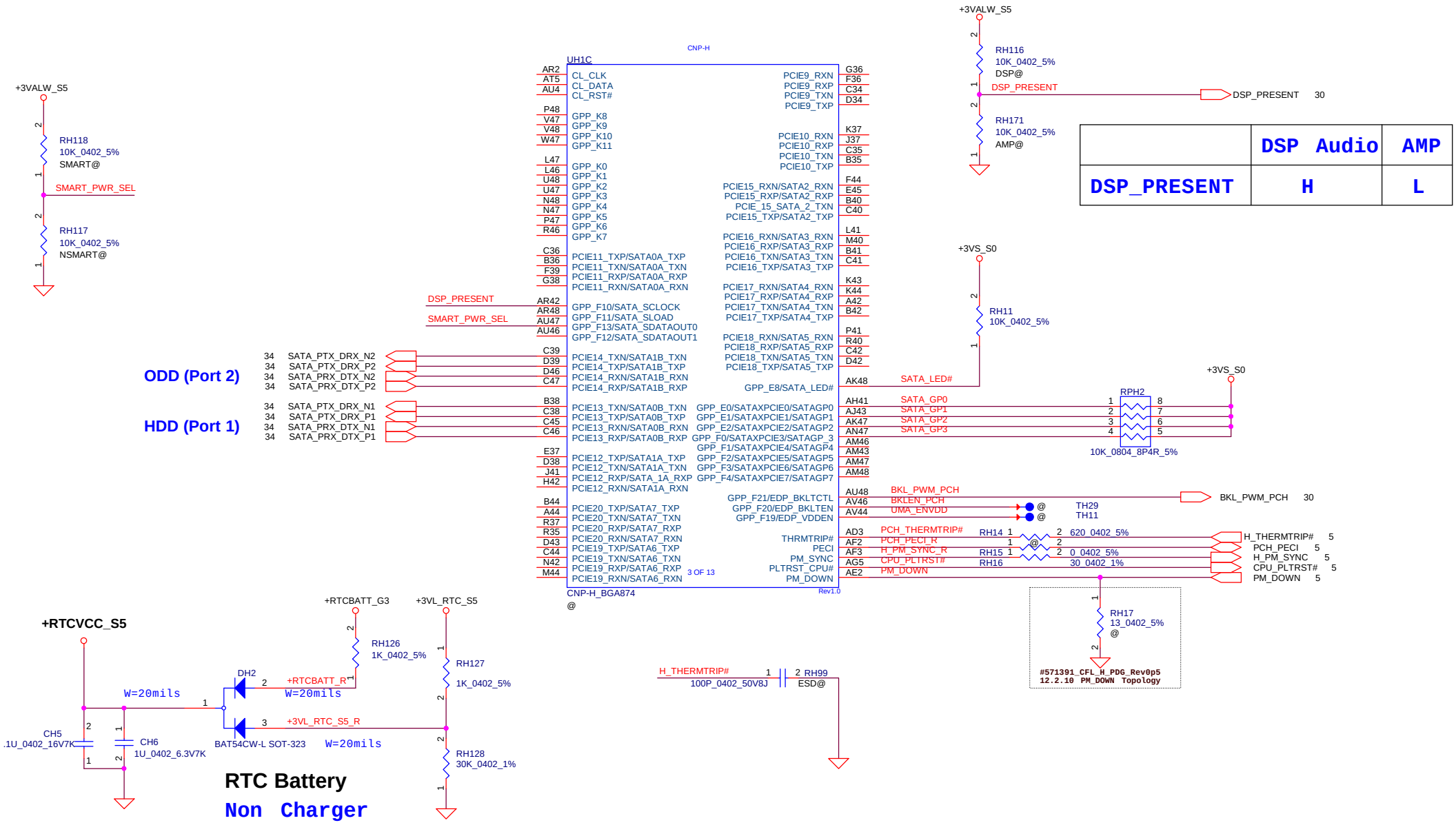

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Title: *PCH_HDA/JTAG/SATA*

Size	Document Number	Rev
B	LA-F882P M/B	0.2

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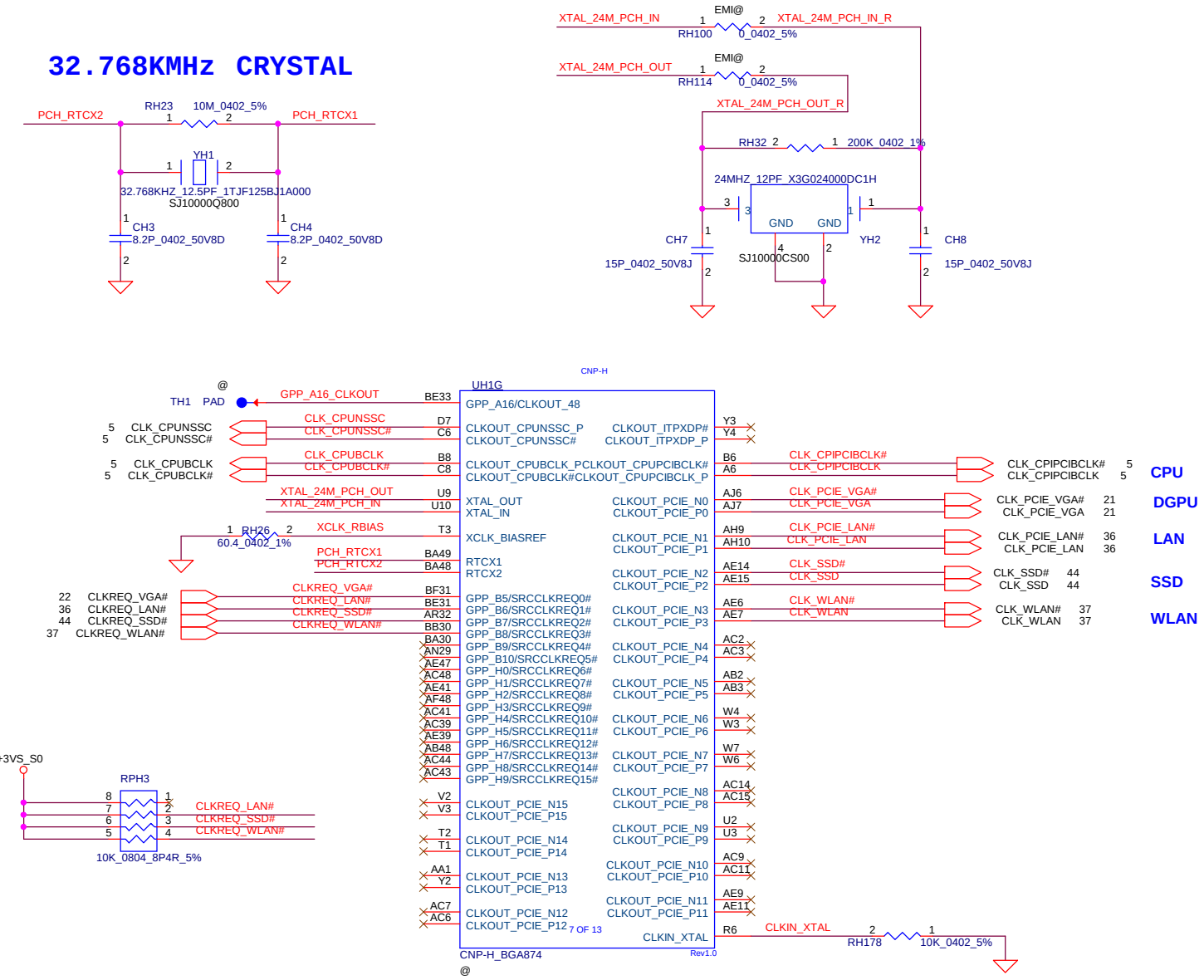

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Issued Date	2017/08/10	Deciphered Date	2018/09/10

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Title: ***PCH_CLK\LPC\SPI\SMBUS***

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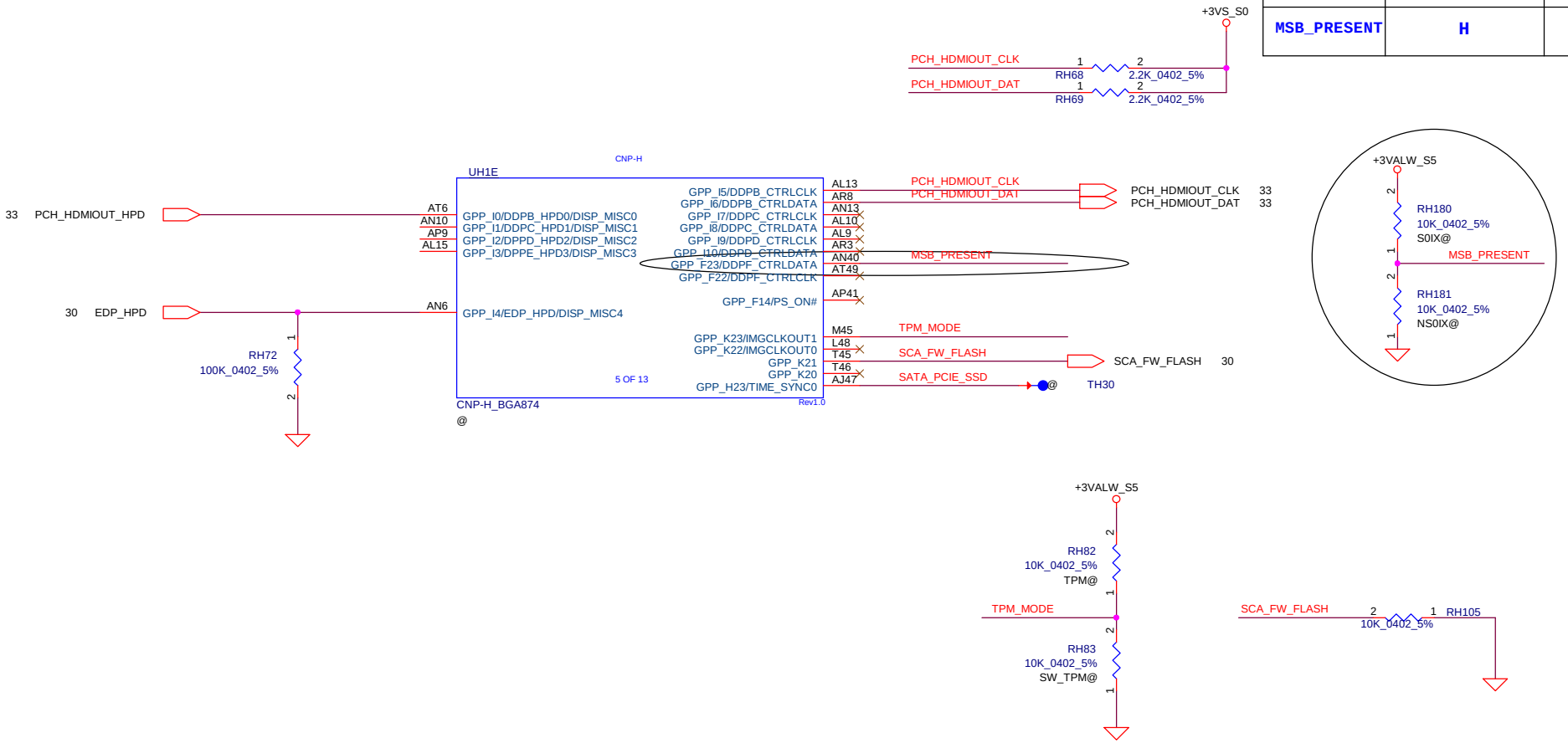
	Moderm standby	No Moderm standby
MSB_PRESENT	H	L



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Title: ***PCH_CRT/DDC***

Size	Document Number	Rev
B	LA-F882P M/B	0.2

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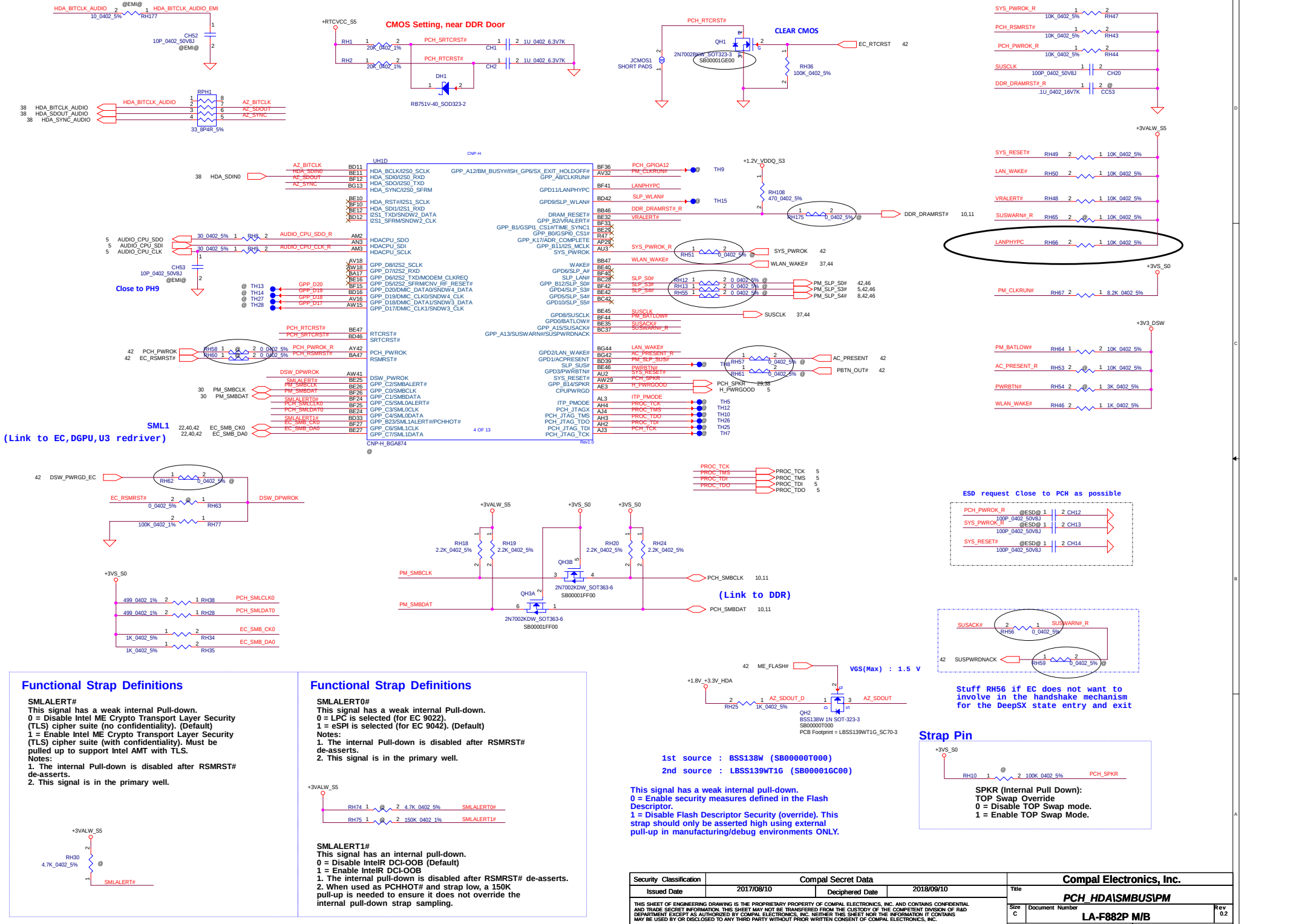
CMOS Setting, near DDR Door
CLEAR CMOS
SML1
(Link to EC,DGPU,U3 redriver)
Close to PH9
(Link to DDR)
ESD request Close to PCH as possible
VGS(Max) : 1.5 V
Stuff RH56 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit
1st source : BSS138W (SB00000T000)
2nd source : LBSS139WT1G (SB000001GC00)
Strap Pin
Functional Strap Definitions
SMLALERT#
This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.
Functional Strap Definitions
SMLALERT0#
This signal has a weak internal Pull-down.
0 = LPC is selected (for EC 9022).
1 = eSPI is selected (for EC 9042). (Default)
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.
SMLALERT1#
This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
SPKR (Internal Pull Down):
TOP Swap Override
0 = Disable TOP Swap mode.
1 = Enable TOP Swap Mode.
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Rev 0.2
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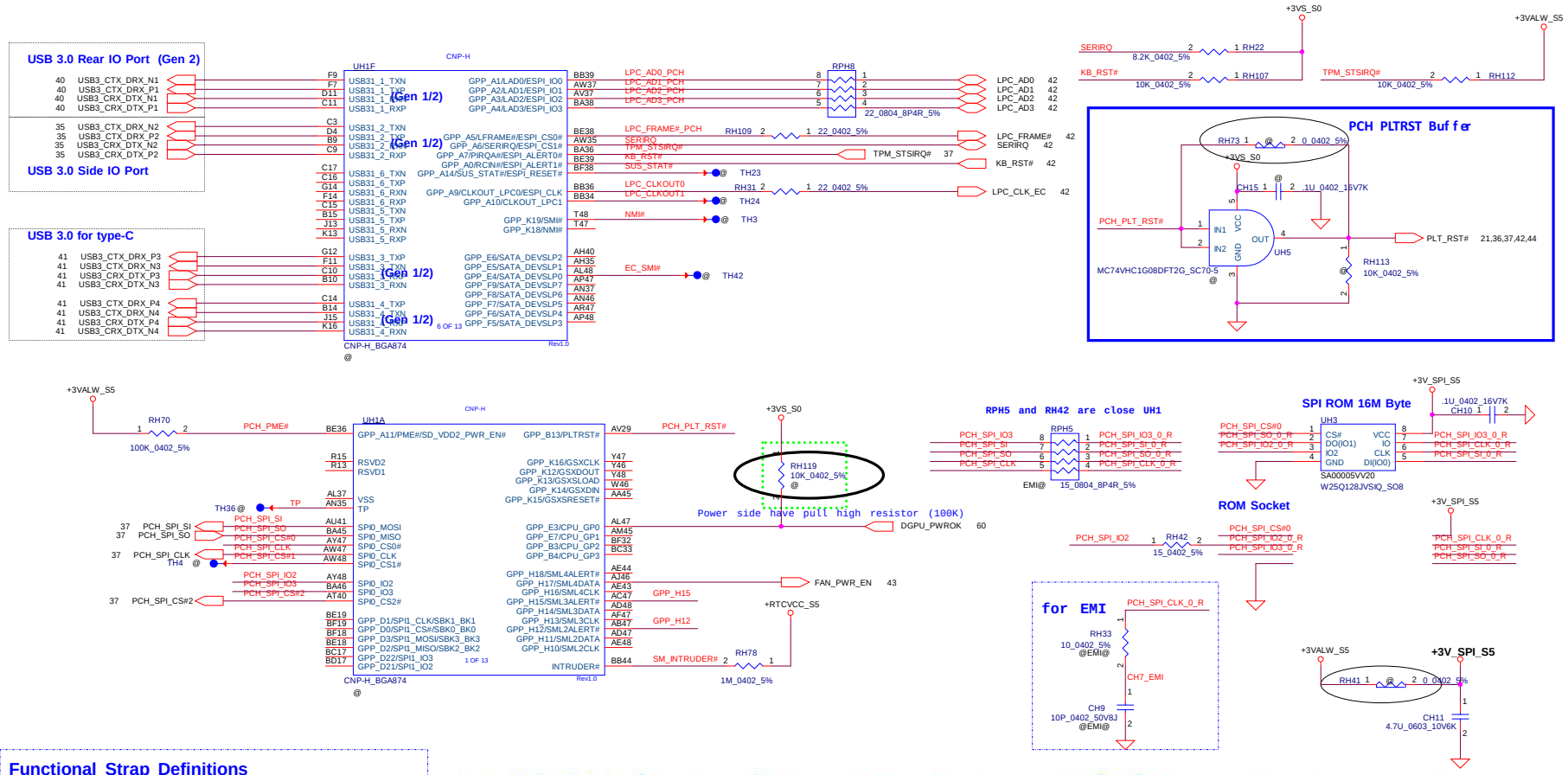
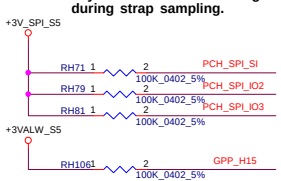


Functional Strap Definitions

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



Functional Strap Definitions

SML2ALERT# (Internal Pull Down):
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

Intel® 300 Series Chipset Preliminary HSIO Lane Assignments

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
USB 3.1 Gen 1 / Gen 2 #1	USB 3.1 Gen 1 / Gen 2 #2	USB 3.1 Gen 1 / Gen 2 #3	USB 3.1 Gen 1 / Gen 2 #4	USB 3.1 Gen 1 / Gen 2 #5	USB 3.1 Gen 1 / Gen 2 #6	USB 3.1 Gen 1 #7	USB 3.1 Gen 1 #8	USB 3.1 Gen 1 #9	USB 3.1 Gen 1 #10	PCIe 3.0 #5	PCIe 3.0 #6	PCIe 3.0 #7	PCIe 3.0 #8	PCIe 3.0 #9	PCIe 3.0 #10	PCIe 3.0 #11	PCIe 3.0 #12	PCIe 3.0 #13	PCIe 3.0 #14	PCIe 3.0 #15	PCIe 3.0 #16	PCIe 3.0 #17	PCIe 3.0 #18	PCIe 3.0 #19	PCIe 3.0 #20	PCIe 3.0 #21	PCIe 3.0 #22	PCIe 3.0 #23	PCIe 3.0 #24
						PCIe 3.0 #1	PCIe 3.0 #2	PCIe 3.0 #3	PCIe 3.0 #4	GbE (LAN)				GbE (LAN)		SATA #0[1]	SATA #1[1] GbE (LAN)	SATA #0 GbE (LAN)	SATA #1	SATA #2	SATA #3	SATA #4	SATA #5						
						x4				x4				x4				x4				x4				x4			
						x2		x2		x2		x2		x2		x2		x2		x2		x2				x2		x2	
						No Remapping				No Remapping				Intel® RST for PCIe Storage				No Remapping				Intel® RST for PCIe Storage				Intel® RST for PCIe Storage			

SKU

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
H310	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen1	N/A	N/A	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B360	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1	USB3.1 Gen 1	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	SATA LAN	SATA	SATA	SATA	SATA	SATA	N/A	N/A	PCIe	PCIe	PCIe	PCIe

[1] SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.

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Title	*PCH_PCI-E/USB*		
Size	Document Number		Rev
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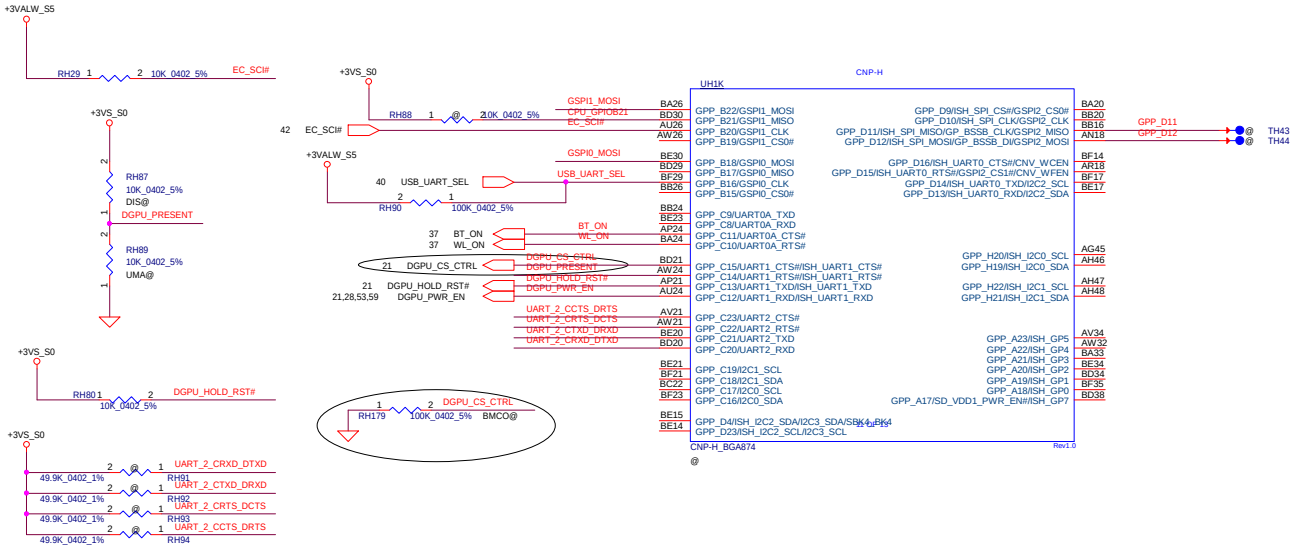
Date:	Monday, April 09, 2018	Sheet	17 of 66

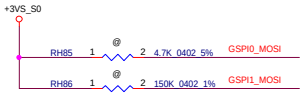


Functional Strap Definitions

GSPI0_MOSI (Internal Pull Down):
No Reboot
0 = Disable No Reboot mode. -->
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):
Boot BIOS Strap Bit
0 = SPI Mode -->
1 = LPC Mode

Strap Pin



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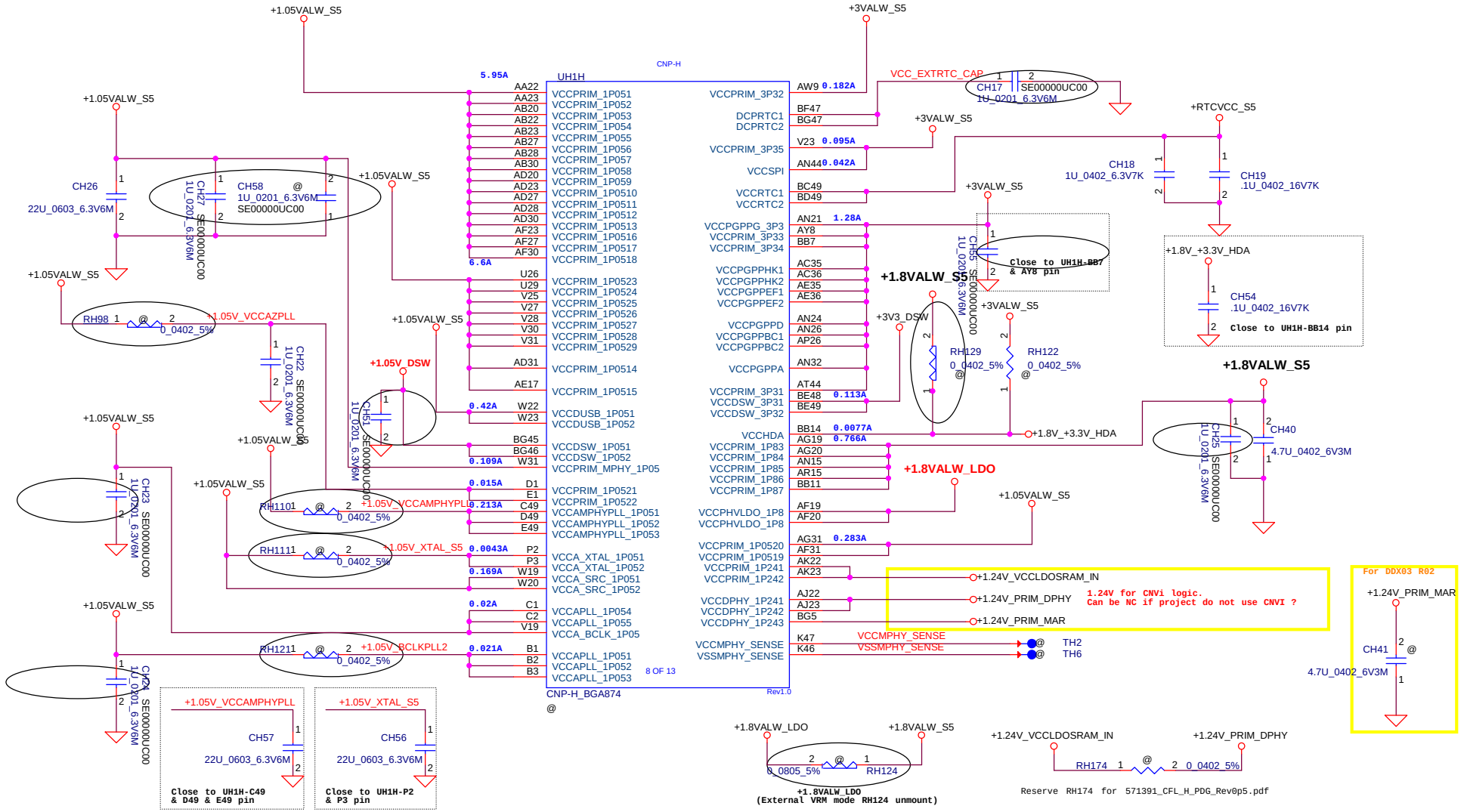

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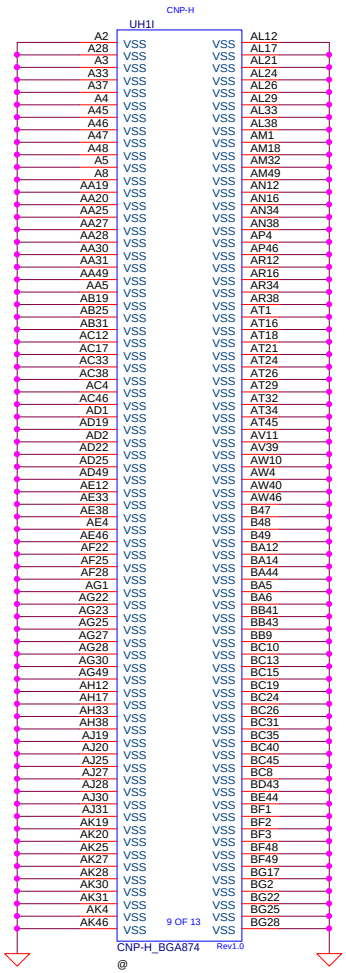
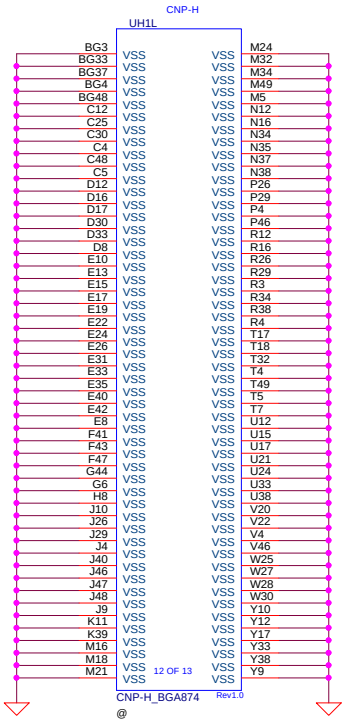
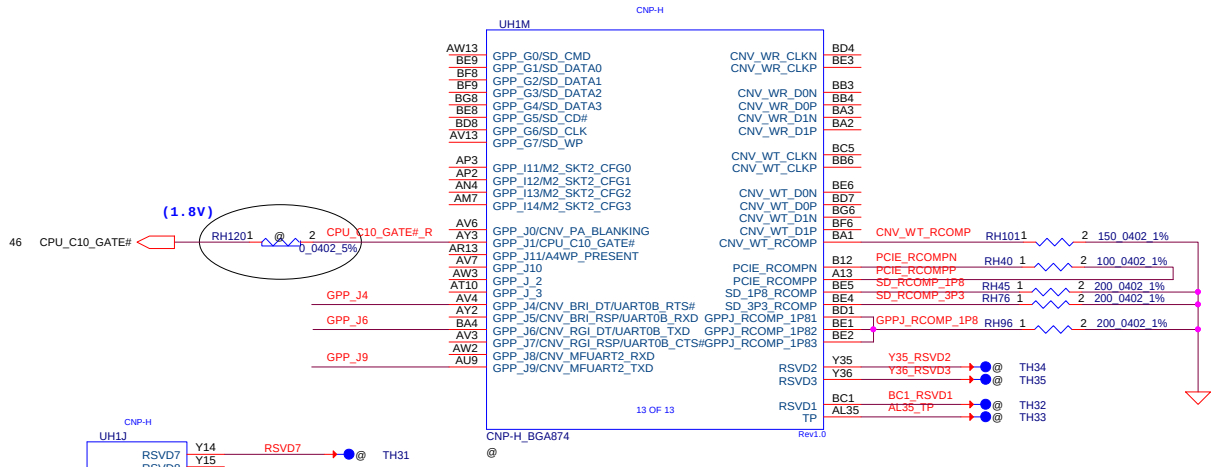






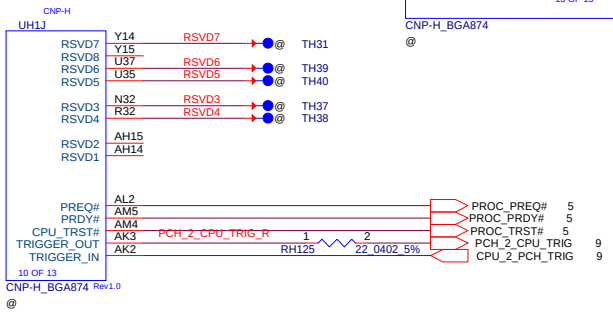
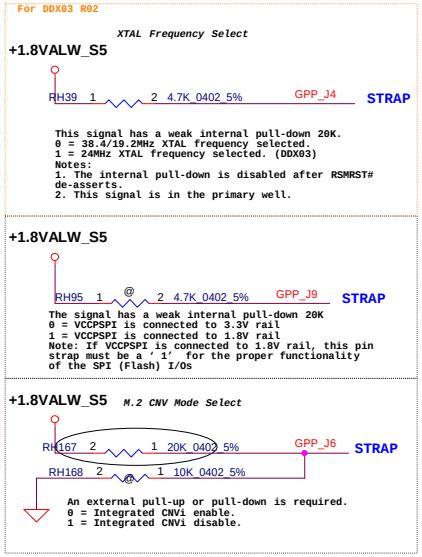


Table 18-1. GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.



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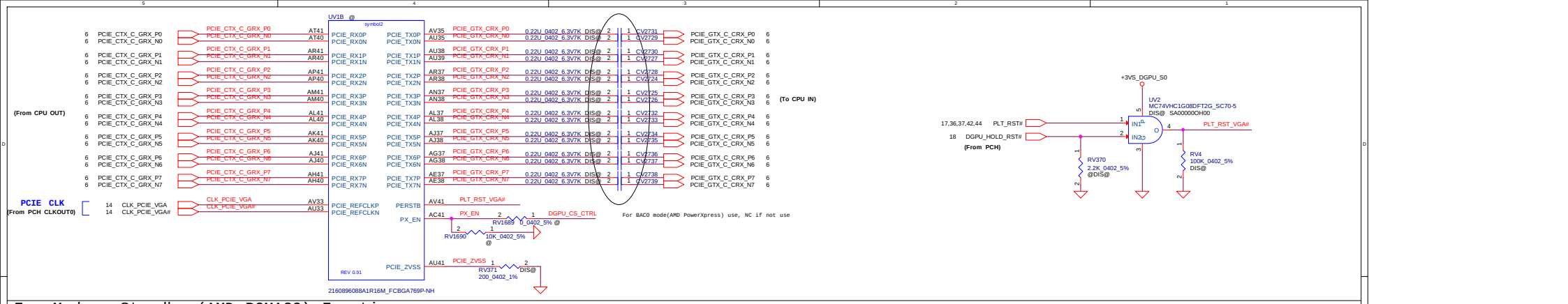
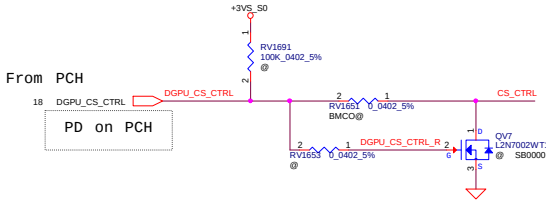
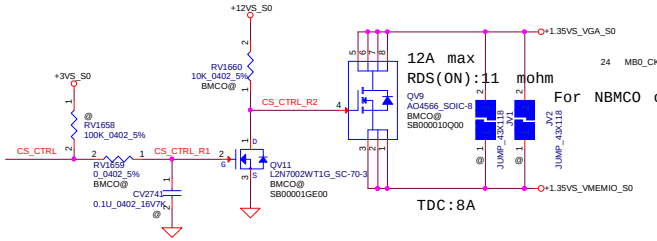
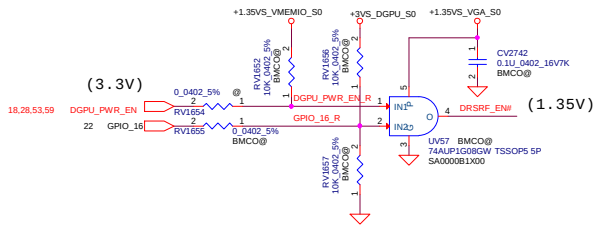
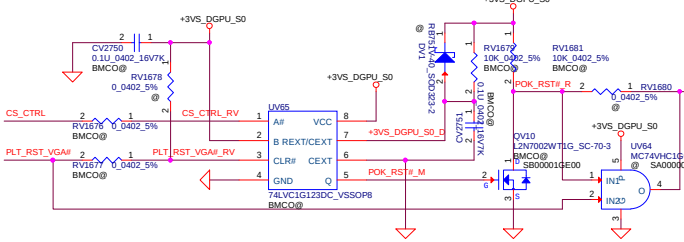


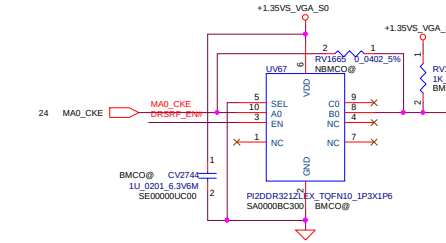
For Moderm Standby (AMD BOMACO) Function:

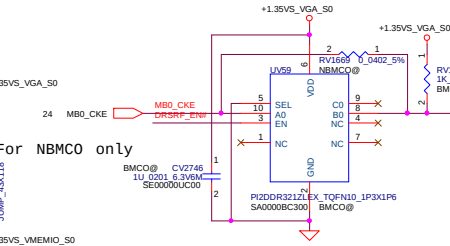


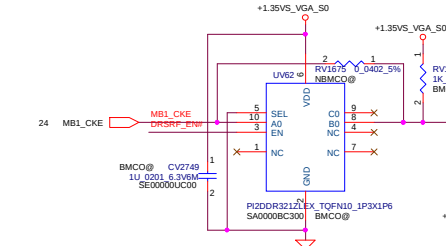


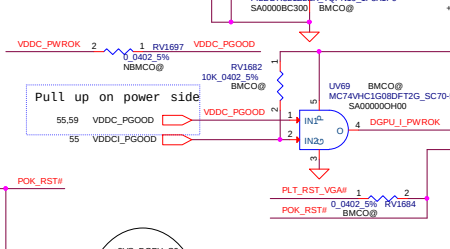


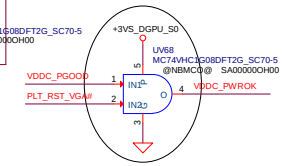


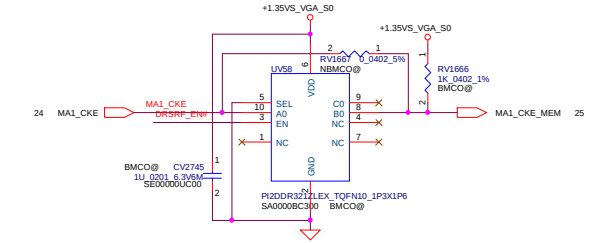


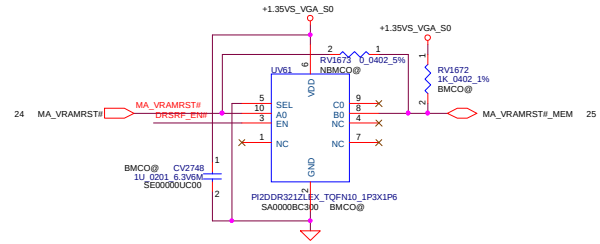


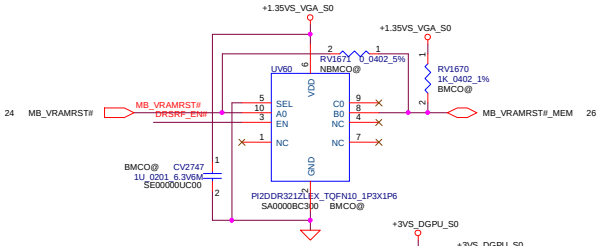


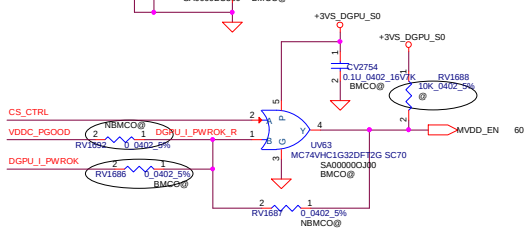












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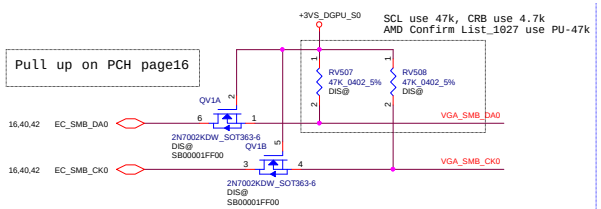
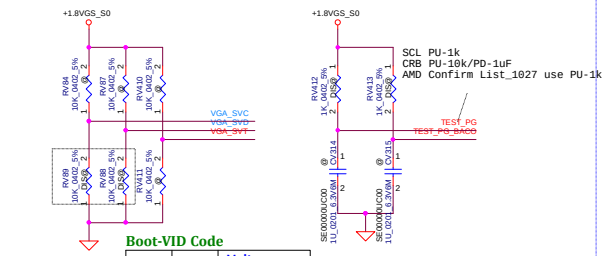




Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

to GPU power

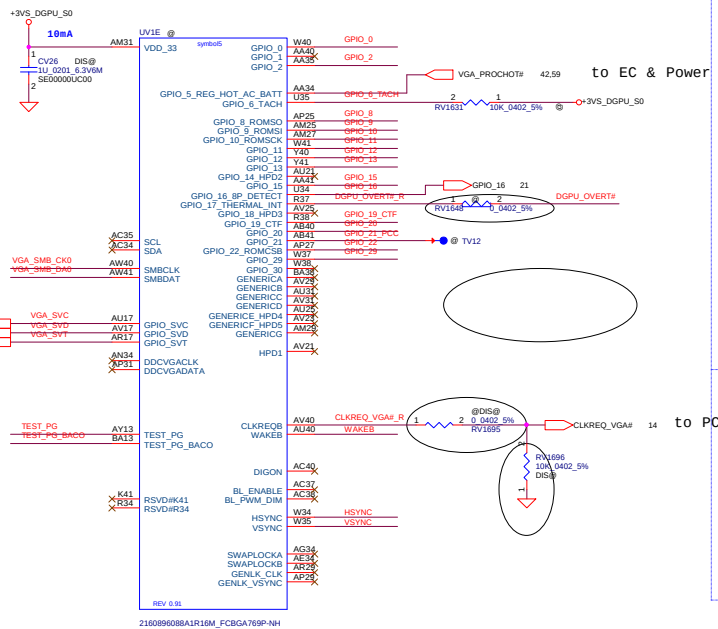
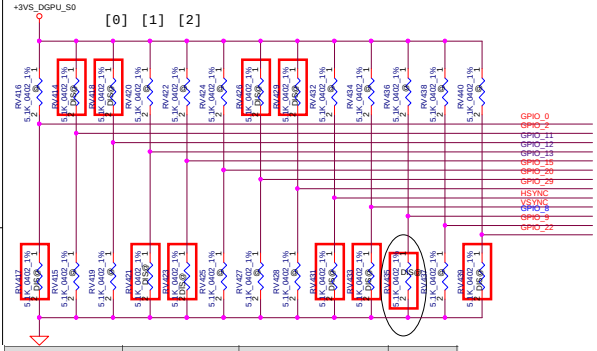


Table 5–2 Regulator Guidelines

Rail Name		Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDC	"R17M-P1-50" 18W	0.700 V to 0.887 V	VID_VDDCI VDDC × 0.6 mΩ ± 20 mV	Overshoot: 120 mV Undershoot: 90 mV	20 A (TDC) 50 A (EDC)	1, 4, 8
	"R17M-P1-50" 25W	0.700 V to 0.963 V			30 A (TDC) 60 A (EDC)	
	"R17M-P1-50" 35W	0.700 V to 1.075 V			40 A (TDC) 70 A (EDC)	
	"R17M-P1-70" 25W	0.700 V to 1.000 V			30 A (TDC) 70 A (EDC)	
	"R17M-P1-70" 40W	0.700 V to 1.144 V			45 A (TDC) 92 A (EDC)	
	"R17M-M2-70"	0.700 V to 0.800 V			16 A (TDC) 35 A (EDC)	



BIF_GEN3_EN_A	GPIO_2	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.	1 (Internal pull-up)	
BIF_CLK_PM_EN	GPIO_8_ROMSO	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.	0 (Internal pull-down)	1 Provide a pull-up resistor option to VDD_33 on the PCB.

Table 3–27 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

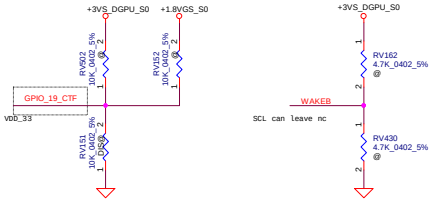
VRAM 4 pcs total 4GB

3.22.2 ROM Configurations

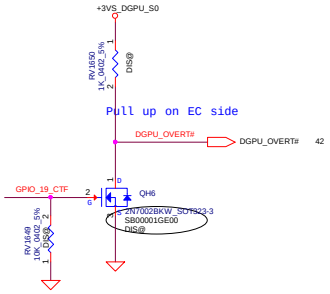
For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device. **Note:** When an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low).	1 (Internal pull-up)	



TX_HALF_SWING	GPIO_0	Controls the transmitter full/half swing mode. 0: The transmitter full-swing is enabled. 1: The transmitter half-swing is enabled.	0 (Internal pull-down)	
BIF_VGA_DIS	GPIO_29	Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).	0 (Internal pull-down)	



The CTF setpoint is 96℃ by default

TX_DEEMPH_EN	GPIO_20	PCI Express transmitter de-emphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.	0 (Internal pull-down)	1 Through pull-up resistor to VDD_33.

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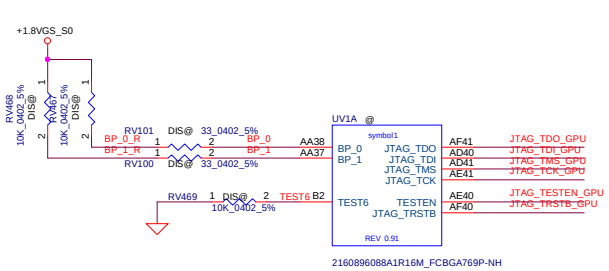

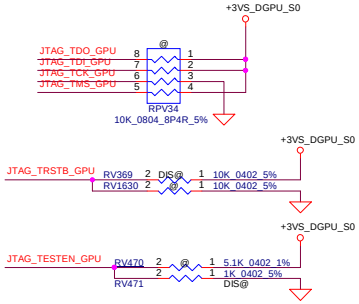

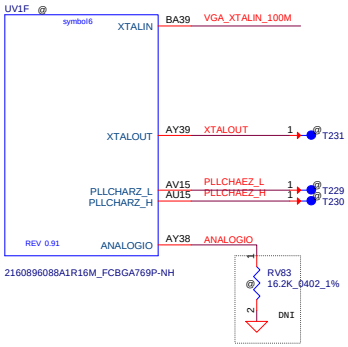

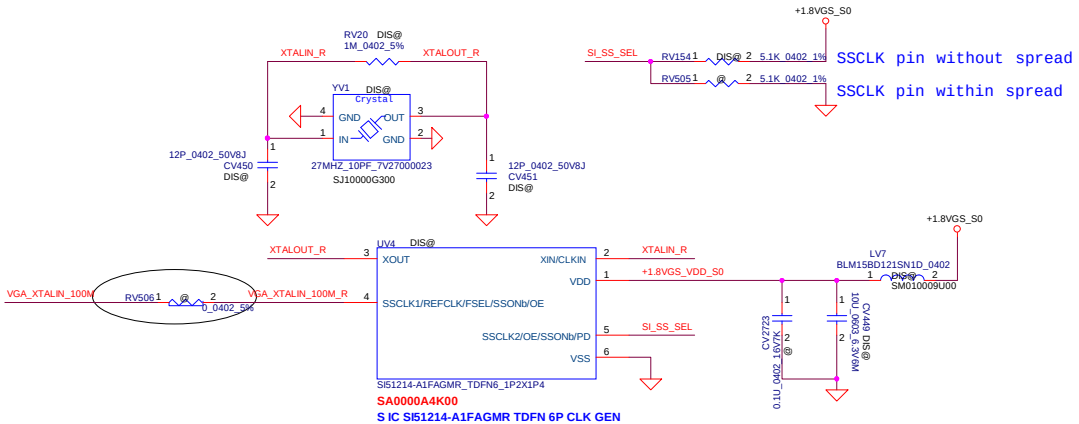

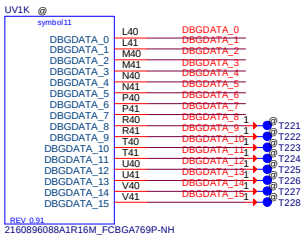

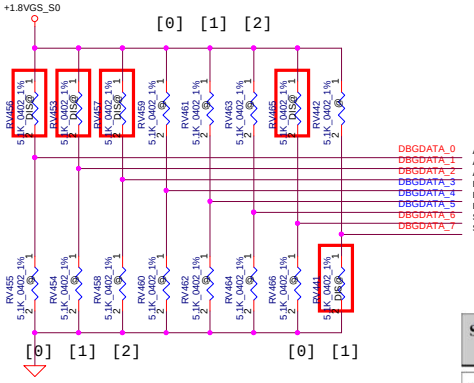

AUD_PORT_CONN[2:0]

111: No usable endpoints
110: One usable endpoint
101: Two usable endpoints
100: Three usable endpoints
011: Four usable endpoints
010: Five usable endpoints
001: Six usable endpoints
000: All endpoints are usable

BOARD_CONFIG[2:0]

000:SAM 128Mx32
001:HYN 128Mx32
010:MIC 256Mx32
011:SAM 256Mx32
100:HYN 256Mx32
101:MIC 128Mx32
110:
111:

DBGDATA_[7:6]

00: 0x 40
01: 0x 41
10: 0x 42
11: 0x 43

BOARD_CONFIG[2:0]

2	1	0
RV464 V4G_S@	RV461 V4G_S@	RV459 V4G_S@
S RES 1/16W 5.1K +-1% 0402 SD034510180	S RES 1/16W 5.1K +-1% 0402 SD034510180	S RES 1/16W 5.1K +-1% 0402 SD034510180
RV463 V4G_H@	RV462 V4G_H@	RV460 V4G_H@
S RES 1/16W 5.1K +-1% 0402 SD034510180	S RES 1/16W 5.1K +-1% 0402 SD034510180	S RES 1/16W 5.1K +-1% 0402 SD034510180
RV464 V4G_M@	RV461 V4G_M@	RV460 V4G_M@
S RES 1/16W 5.1K +-1% 0402 SD034510180	S RES 1/16W 5.1K +-1% 0402 SD034510180	S RES 1/16W 5.1K +-1% 0402 SD034510180

Strap Pins		GPU 7-bit Slave Address Field						
DBGDATA_7	DBGDATA_6	A6	A5	A4	A3	A2	A1	A0
LOW	LOW	1	0	0	0	0	0	0
LOW	HIGH	**1**	**0**	**0**	**0**	**0**	**0**	**1**
HIGH	LOW	1	0	0	0	0	1	0
HIGH	HIGH	1	0	0	0	0	1	1

Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: R17M-P1-50/70_(2/8)_MSIC-2

Size: Custom | Document Number: LA-F882P M/B | Rev: 0.2

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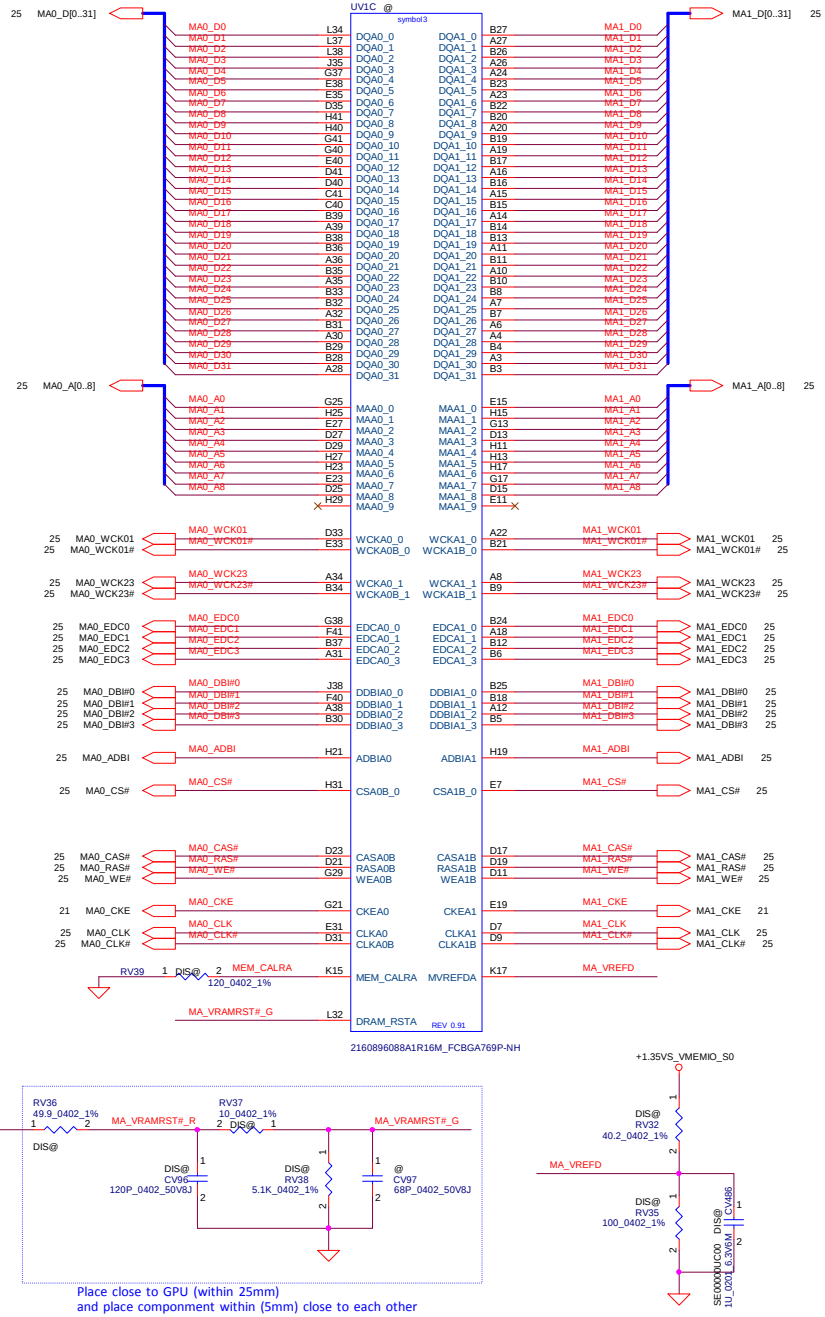
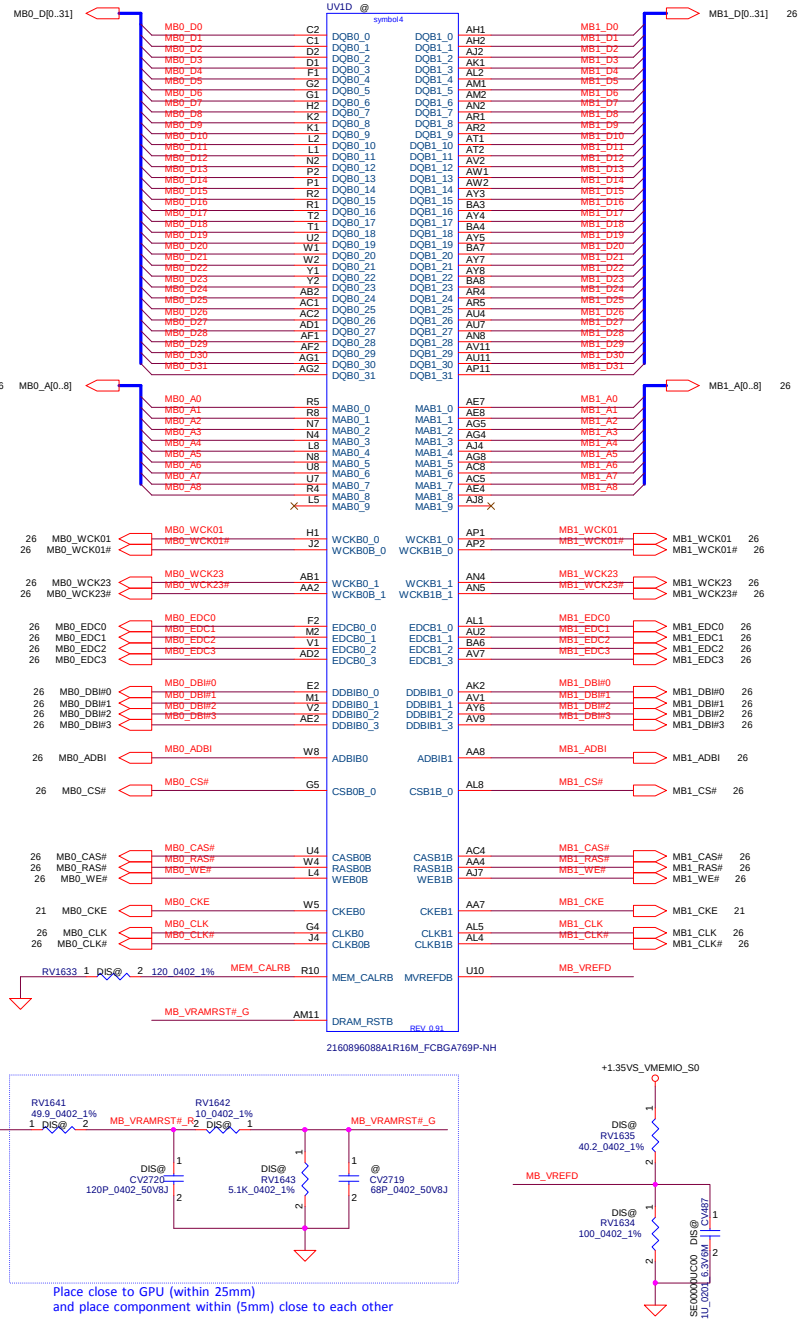
A0/1 Channel



B0/1 Channel



Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: R17M-P1-50/70_(4/9)_MEM

Size: Custom | Document Number: LA-F882P M/B | Rev: 0.2

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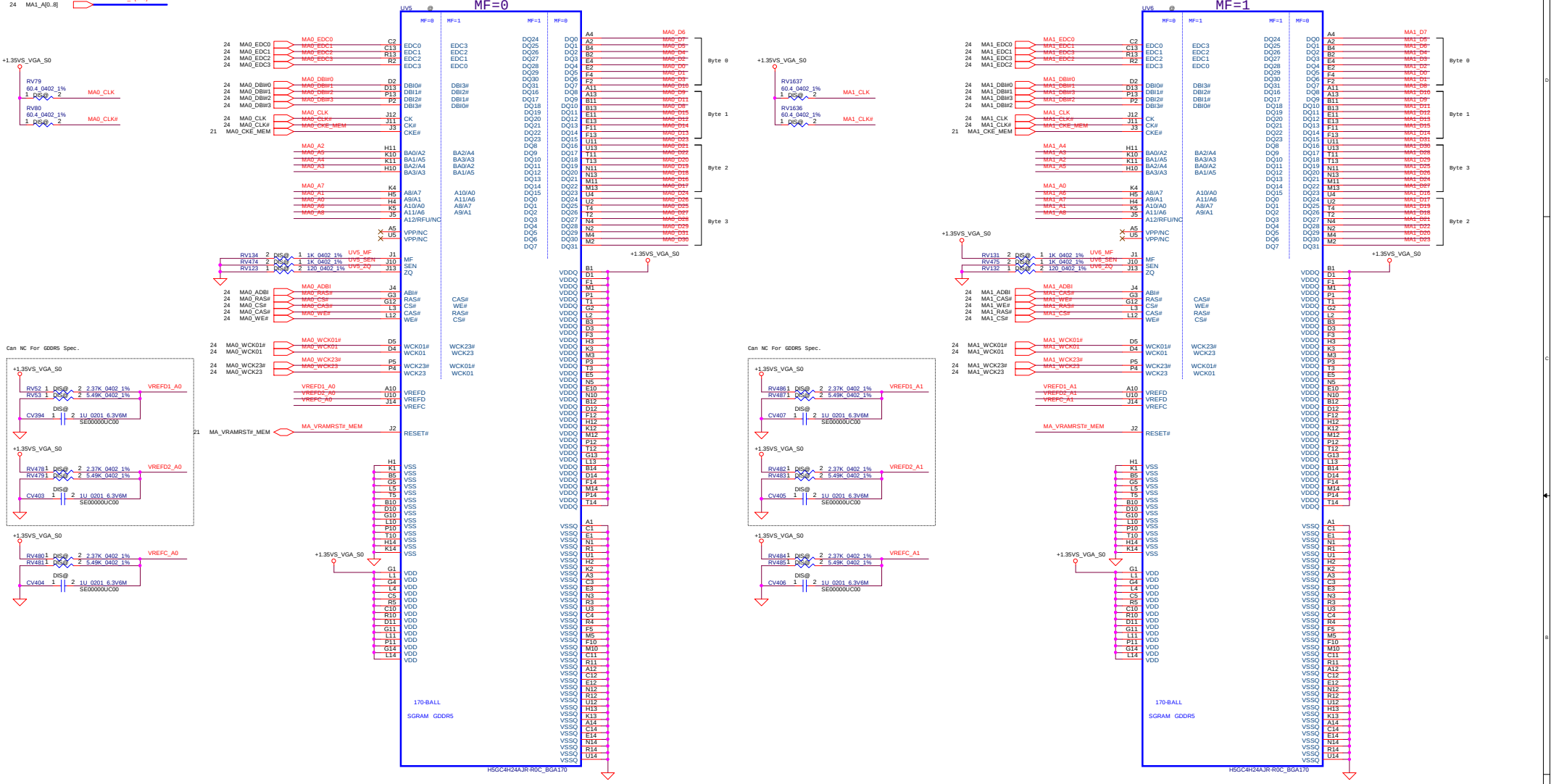
A0 Channel

A1 Channel



Compal Electronics, Inc.

Title: R17M-P1-50/70_(5/9)_CH A

Size: Custom | Document Number: LA-F882P M/B | Rev: 0.2

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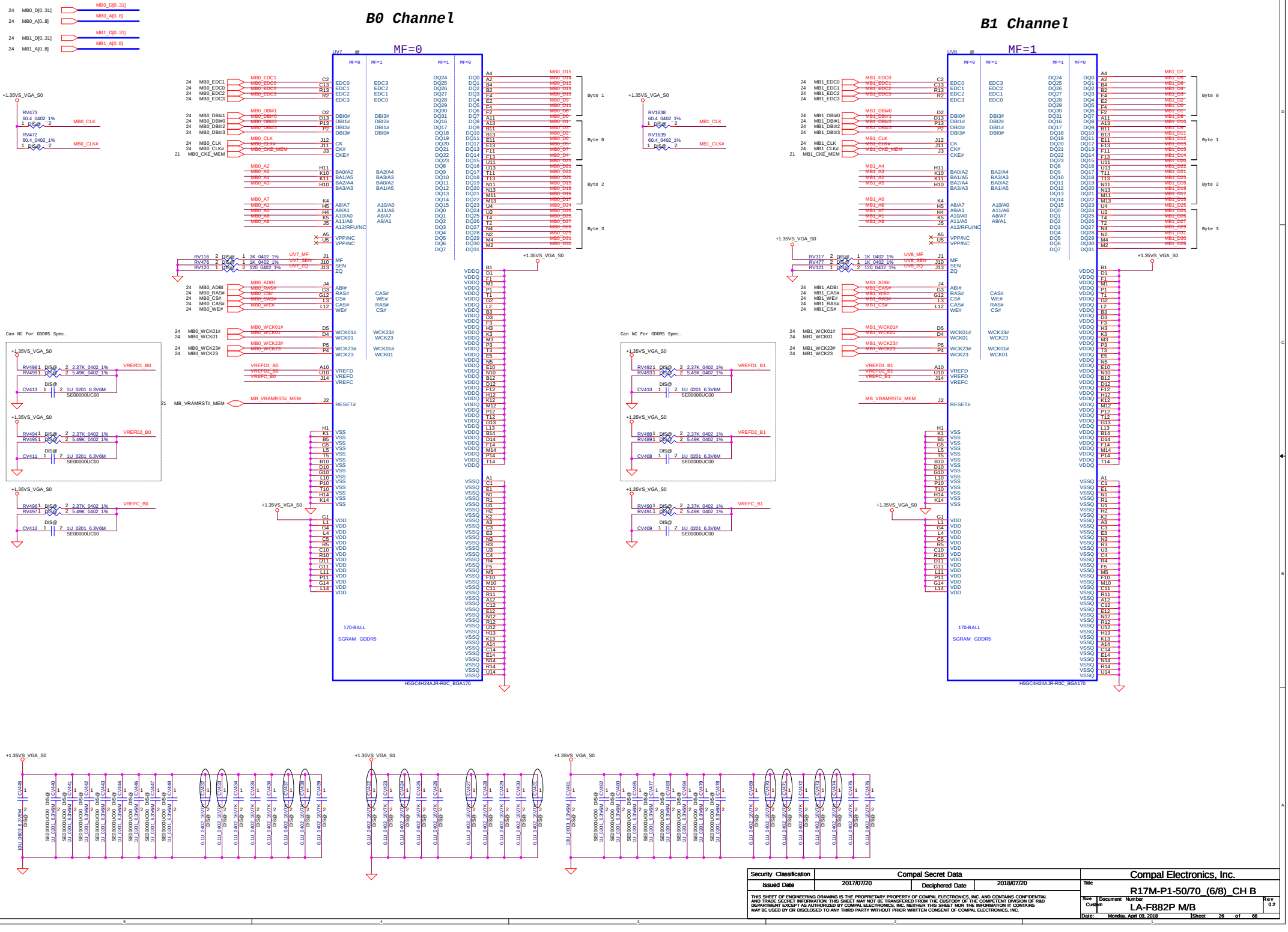
B0 Channel

B1 Channel



Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.	
Title	R17M-P1-50/70_(6/8)_CH B
Size: Custom	Document Number: LA-F882P M/B
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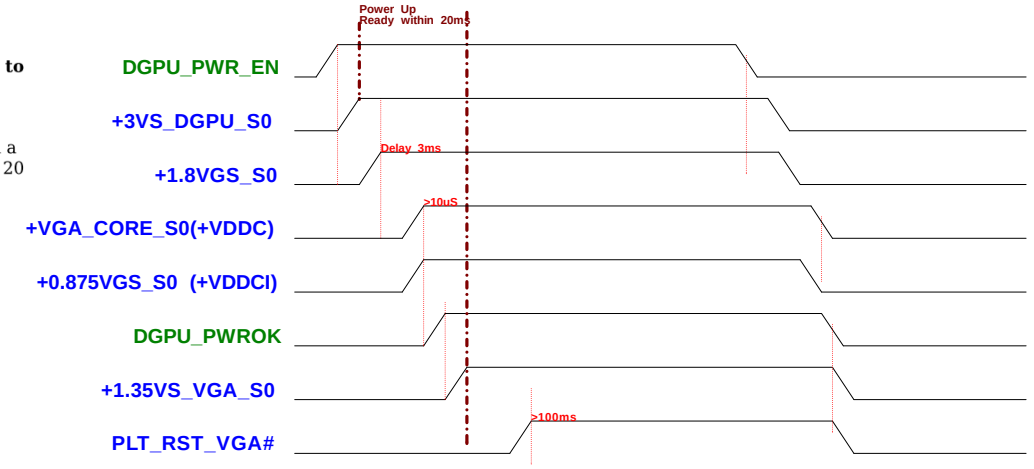
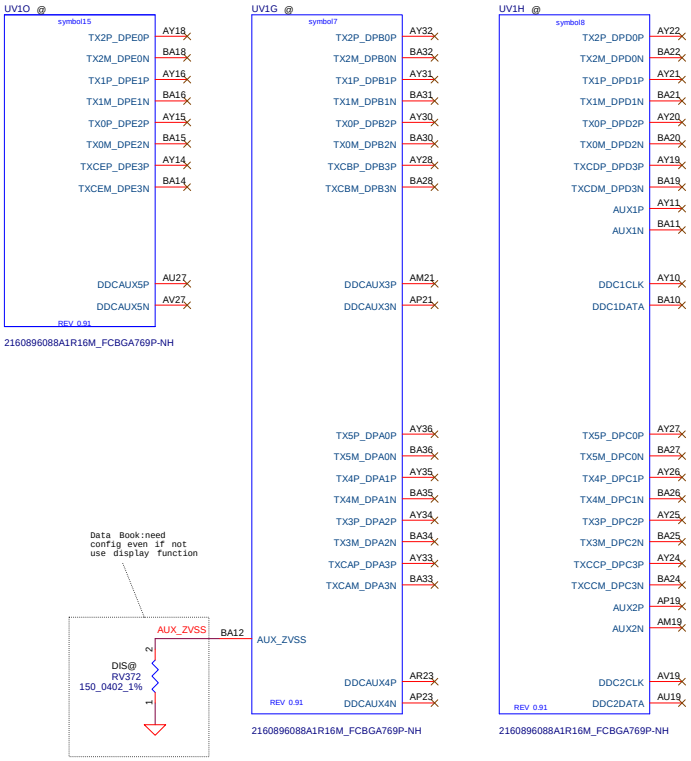
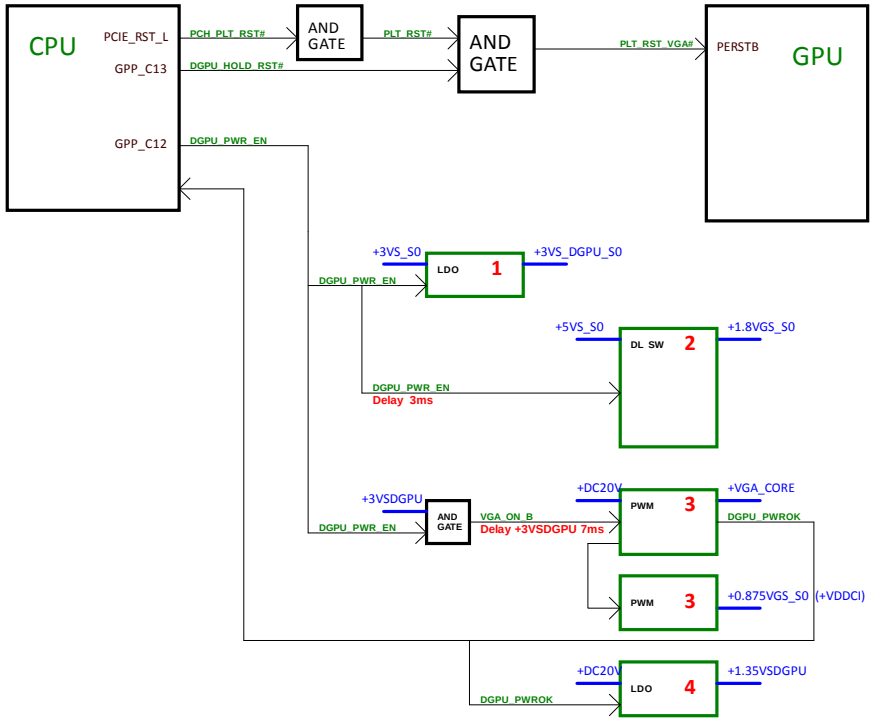
5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.







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Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.			
Title	R17M-P1-50/70_(7/8)_DISPLAY		
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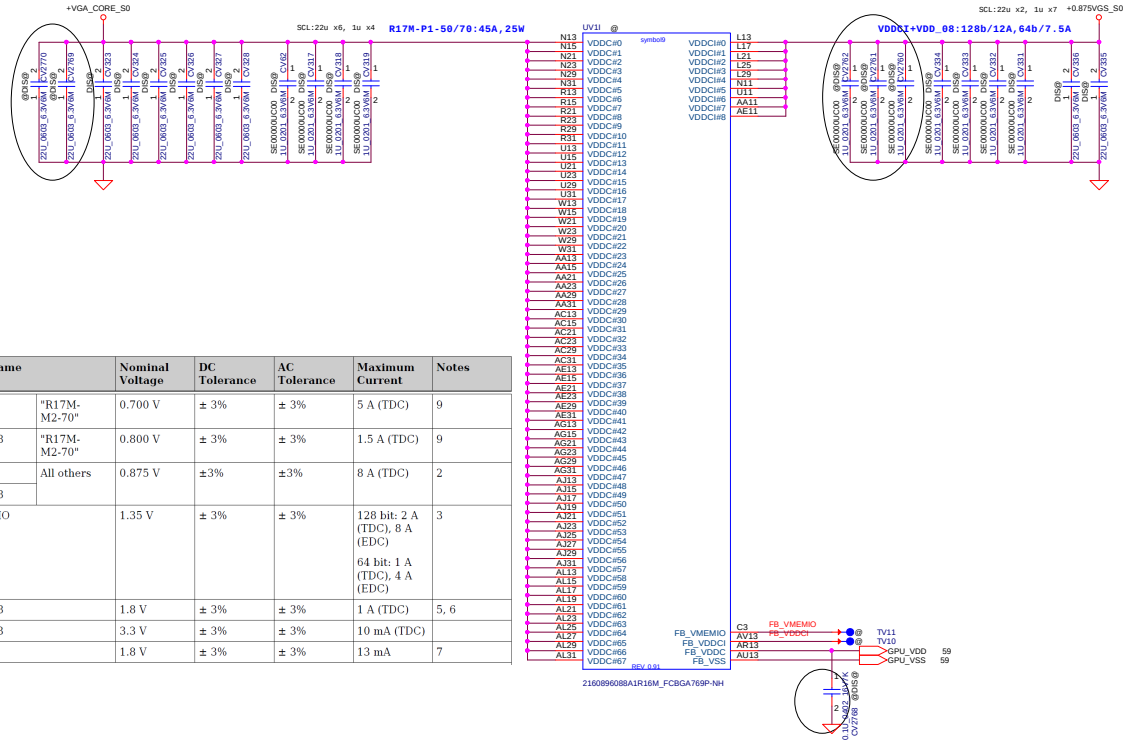
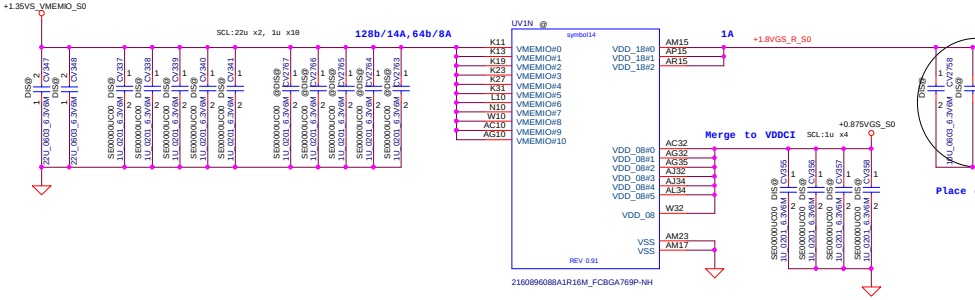
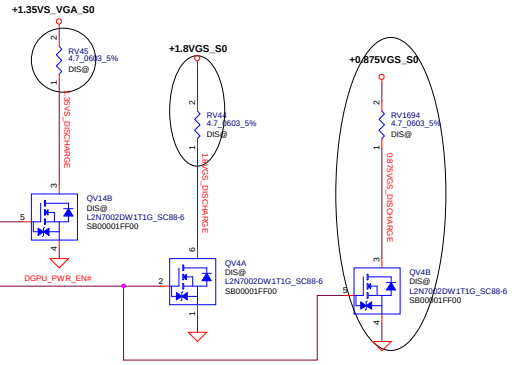
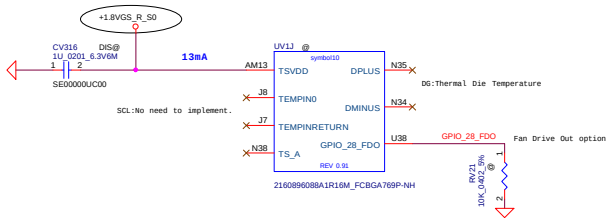
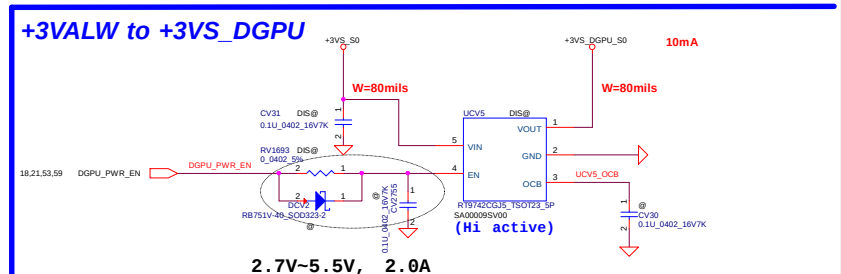


Rail Name		Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDCI	"R17M-M2-70"	0.700 V	± 3%	± 3%	5 A (TDC)	9
VDD_08	"R17M-M2-70"	0.800 V	± 3%	± 3%	1.5 A (TDC)	9
VDDCI	All others	0.875 V	±3%	±3%	8 A (TDC)	2
VDD_08						
VMEMIO		1.35 V	± 3%	± 3%	128 bit: 2 A (TDC), 8 A (EDC) 64 bit: 1 A (TDC), 4 A (EDC)	3
VDD_18		1.8 V	± 3%	± 3%	1 A (TDC)	5, 6
VDD_33		3.3 V	± 3%	± 3%	10 mA (TDC)	
TSVDD		1.8 V	± 3%	± 3%	13 mA	7









Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/10	Deciphered Date 2018/09/10	Title: R17M-P1-50/70_(8/8)_PWR/GND
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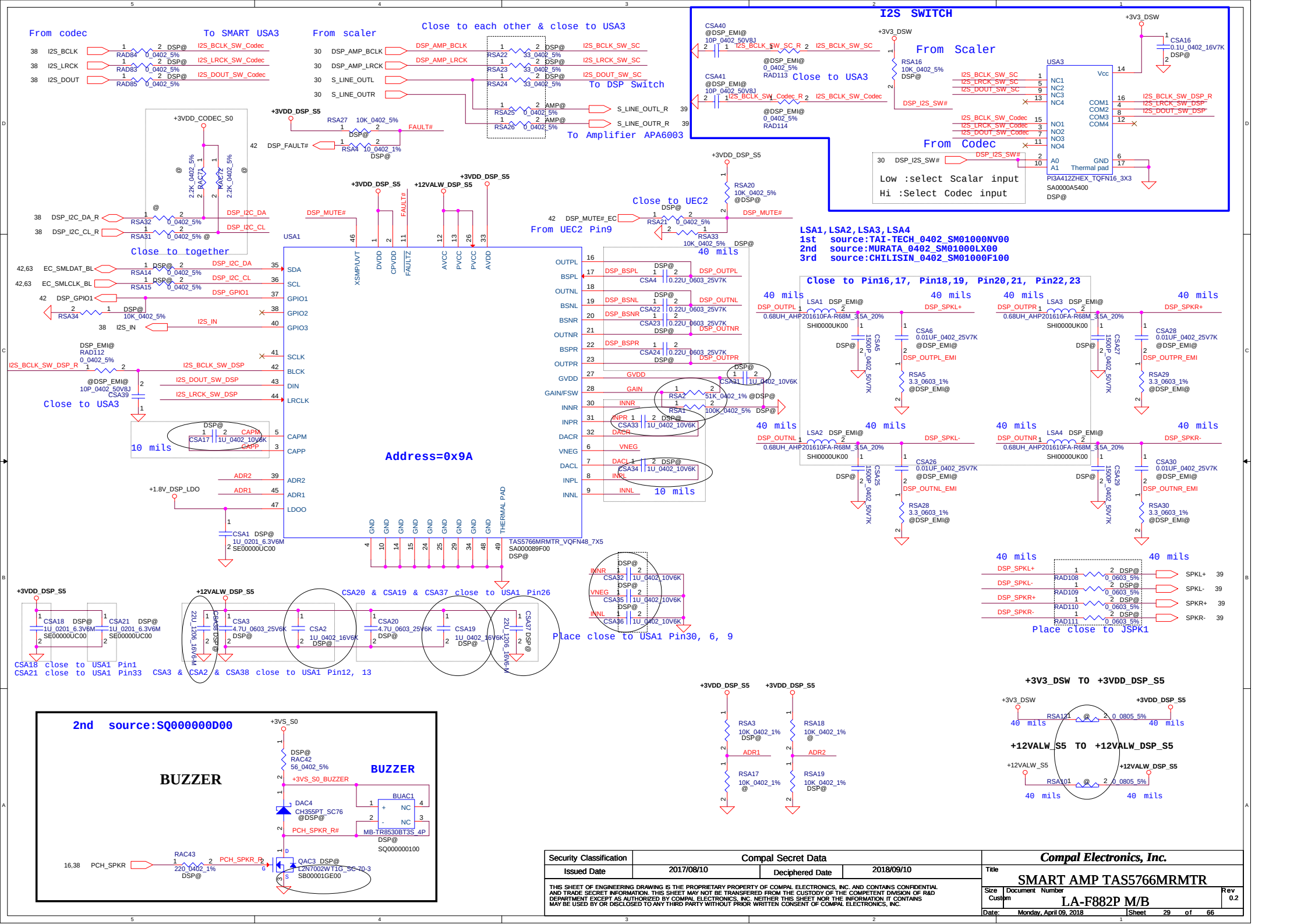
			Date: Monday, April 09, 2018; Sheet 28 of 66



Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: SMART AMP TAS5766MRMTR

Size: Custom | Document Number: LA-F882P M/B | Rev: 0.2

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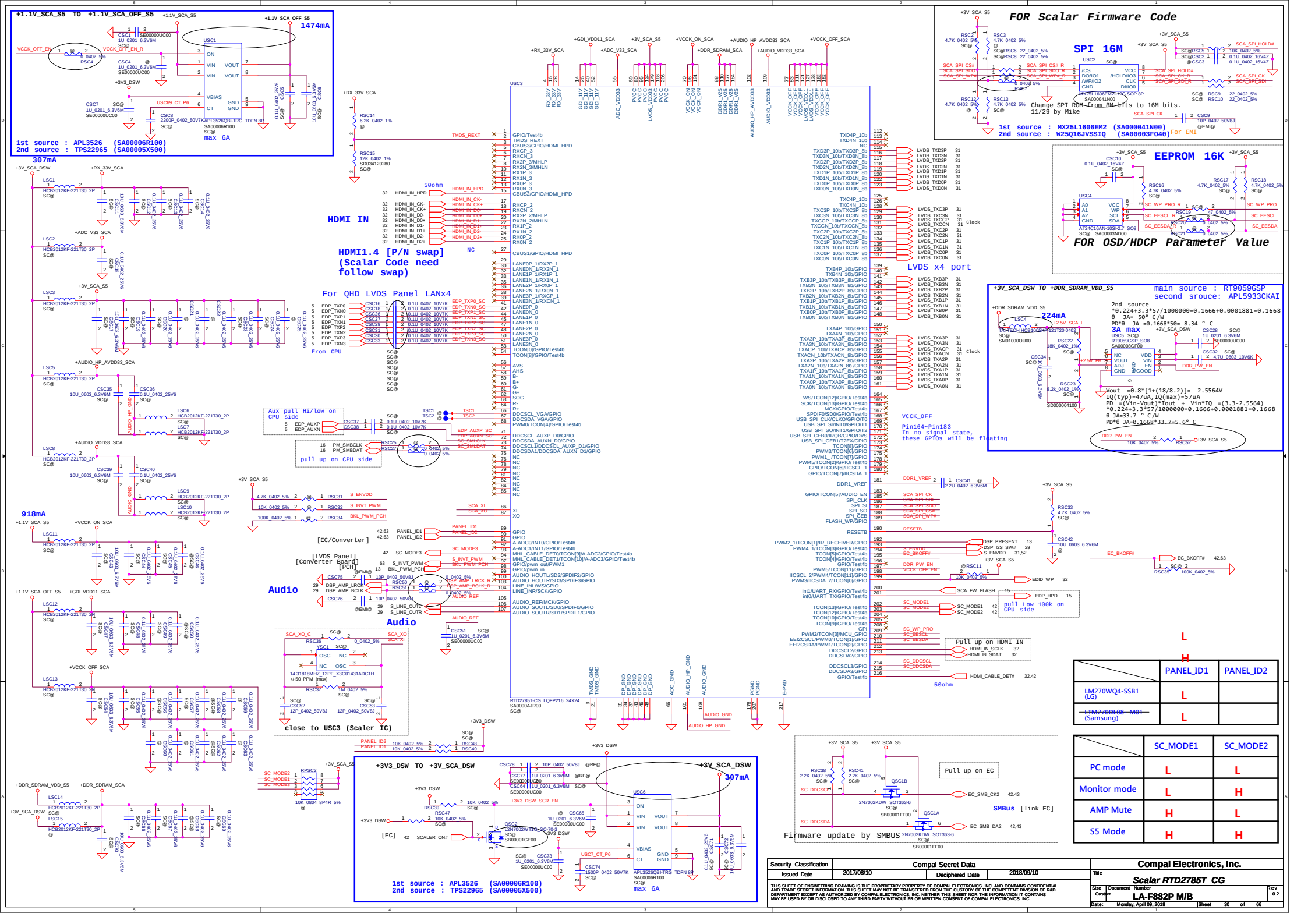

	PANEL_ID1	PANEL_ID2
LM270WQ4-SSB1 (LG)	L	
~~LTM270DL08 M01~~ (Samsung)	L	

	SC_MODE1	SC_MODE2
PC mode	L	L
Monitor mode	L	H
AMP Mute	H	L
S5 Mode	H	H

Security Classification	Compal Secret Data	
Issued Date	2017/08/10	Deciphered Date 2018/09/10

Compal Electronics, Inc.	
Title	Scalar RTD2785T_CG
Size / Document Number / Custom	LA-F882P M/B
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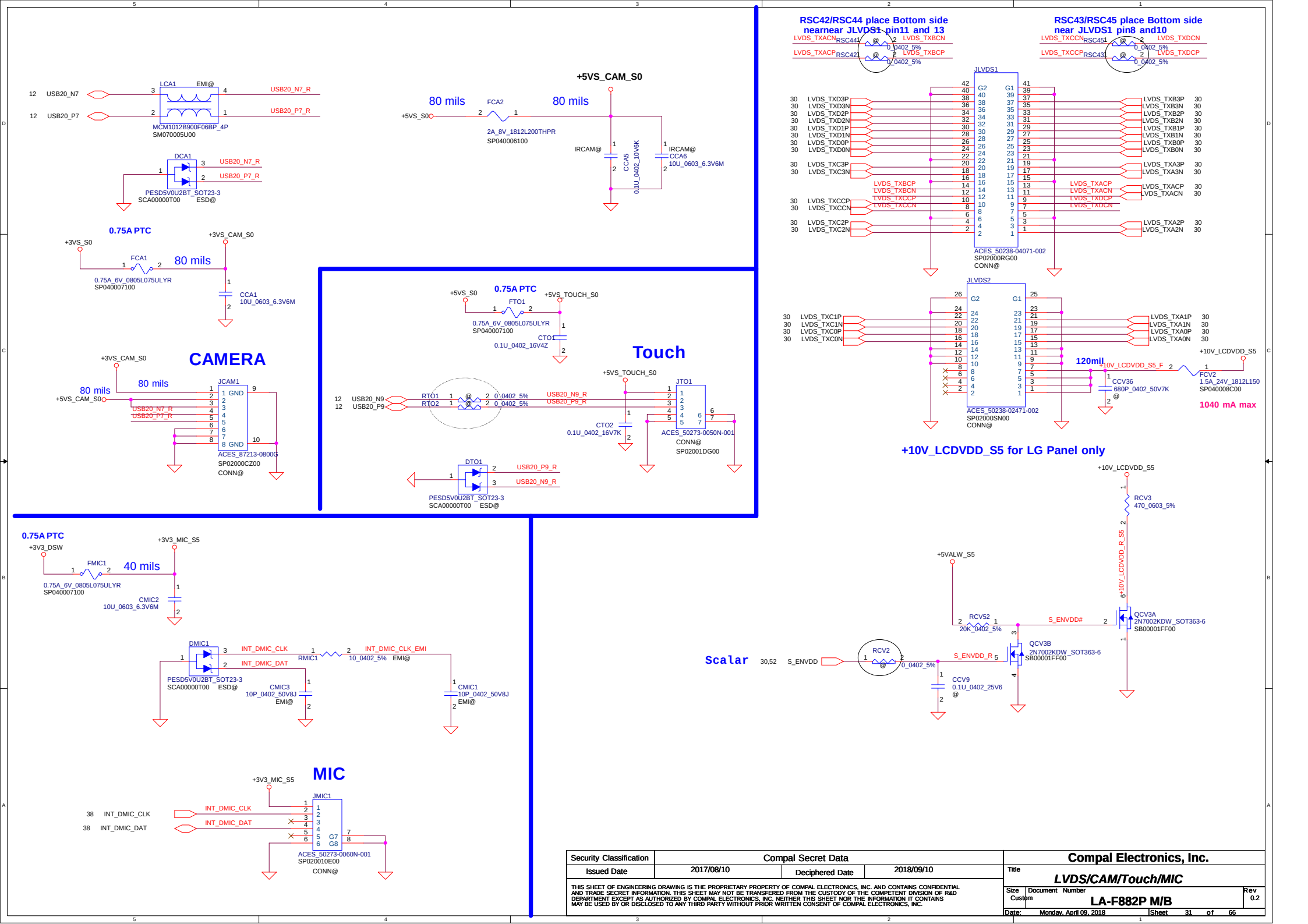

Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: ***LVDS/CAM/Touch/MIC***

Size	Document Number	Rev
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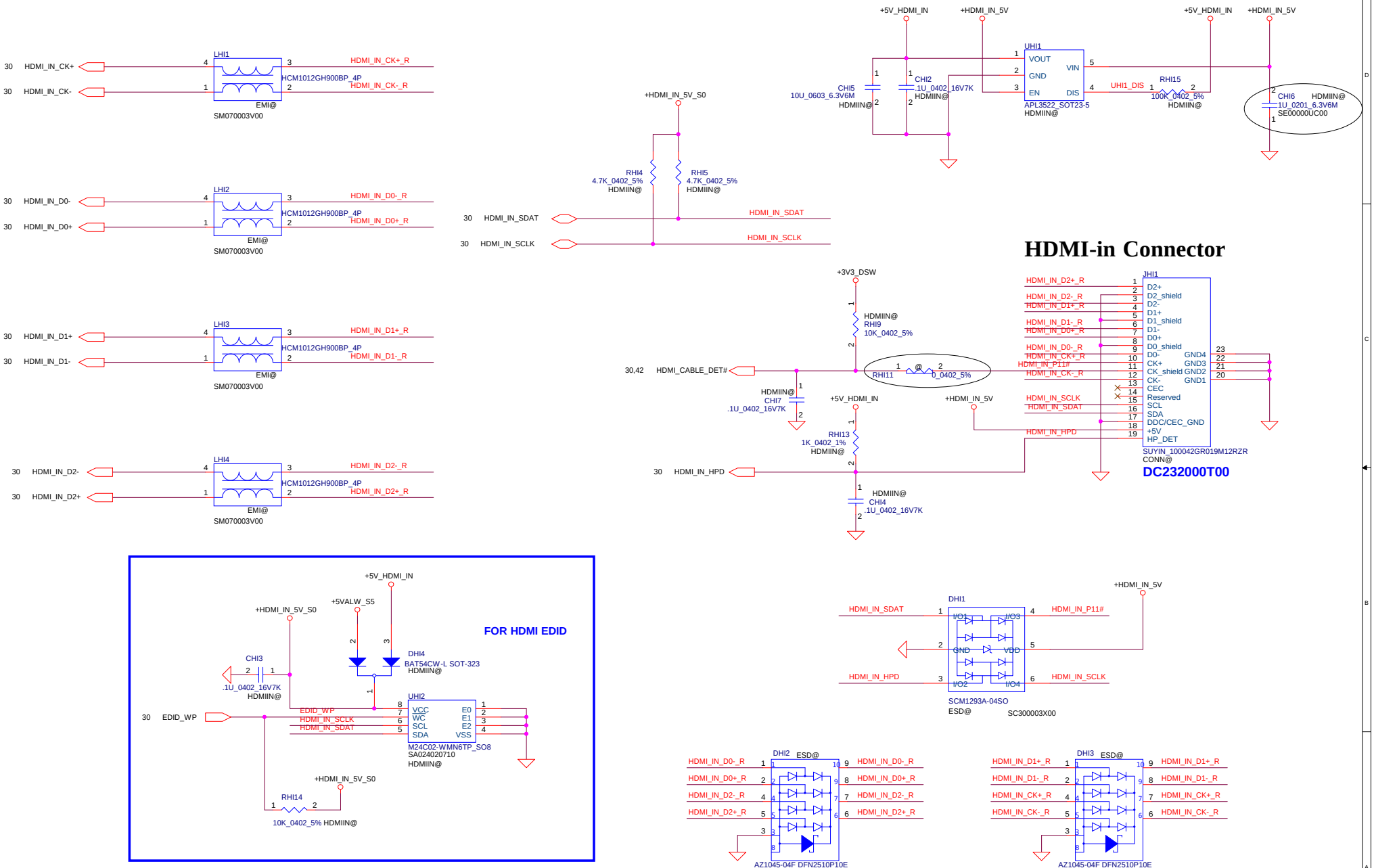
HDMI-in Connector



Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.	
Title	*HDMI-IN conn*
Size: Custom	Document Number: LA-F882P M/B
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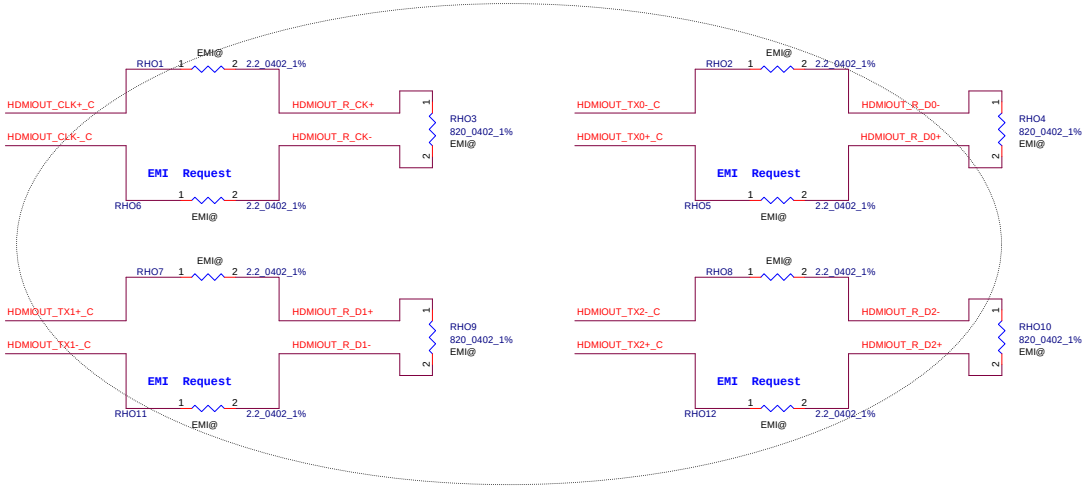
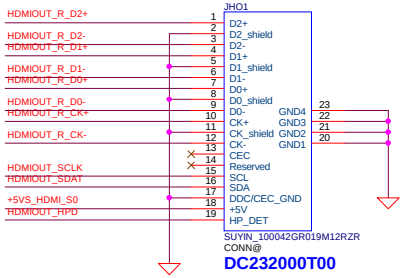
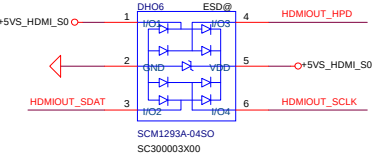
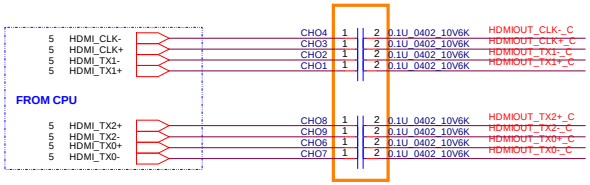
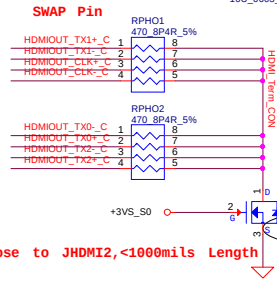
HDMI-OUT Connector

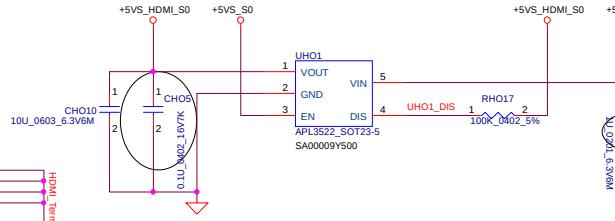


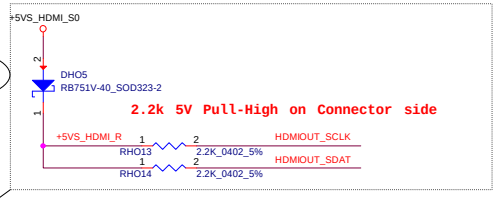


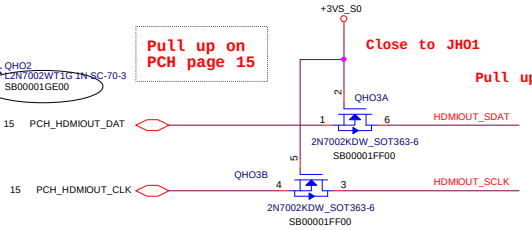


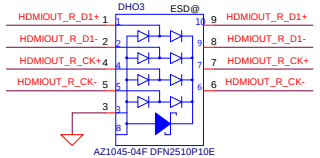


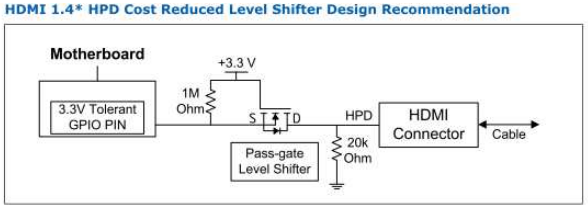


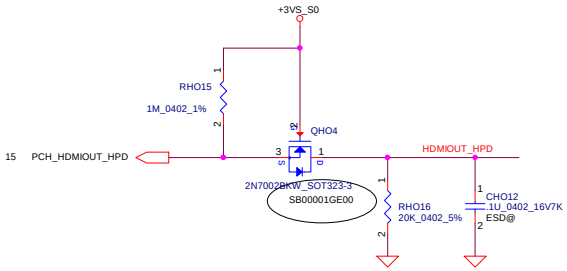


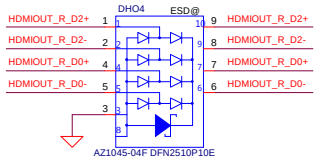












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Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: **HDMI IN**

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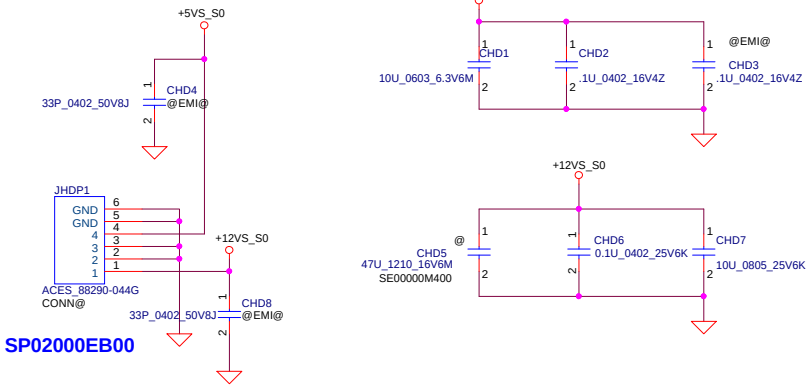
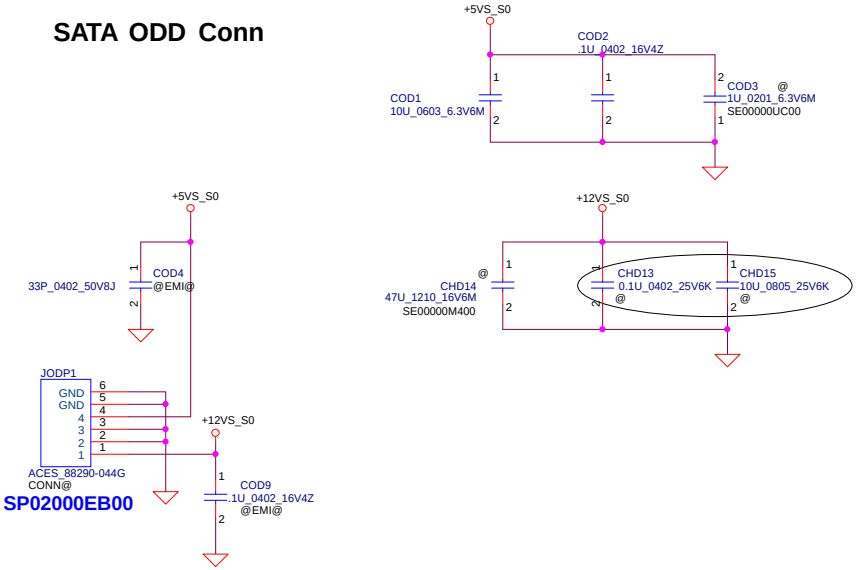
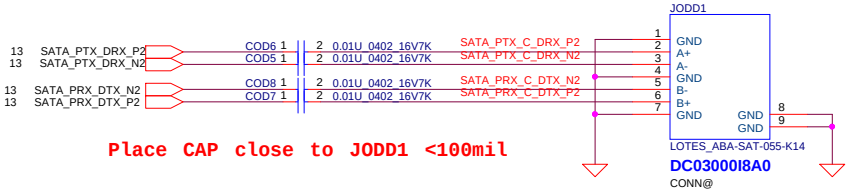
SATA HDD Conn.

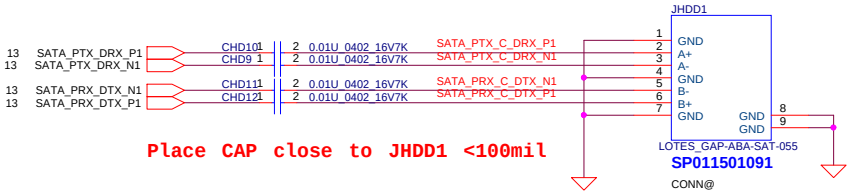


SATA ODD Conn





Place CAP close to JODD1 <100mil



Place CAP close to JHDD1 <100mil

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***HDD/ODD***

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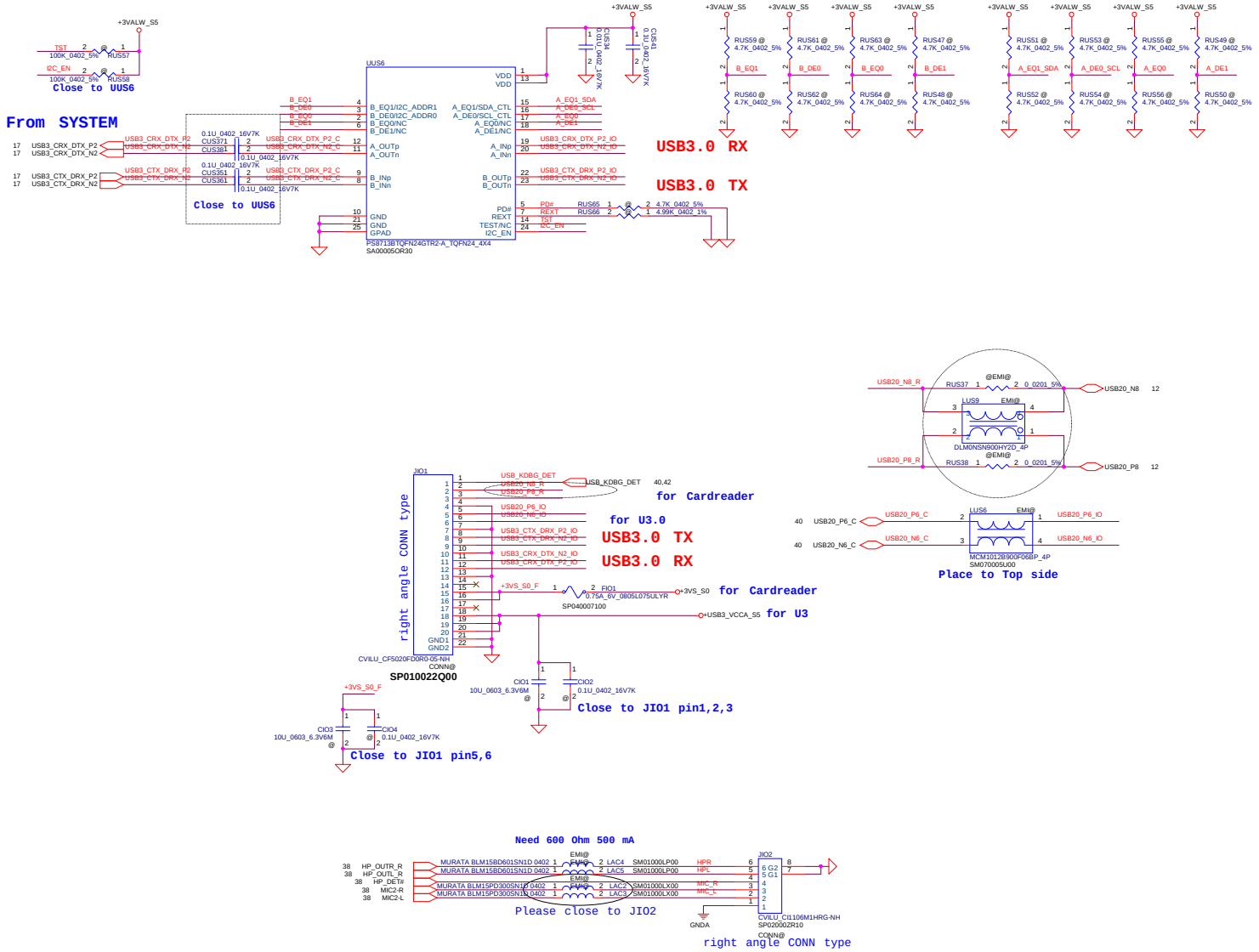

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Issued Date	2017/08/10	Deciphered Date 2018/09/10	Title: IO Board
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			Date: Monday, April 09, 2018; Sheet 35 of 66

WOL circuit (Connect +3V_LAN to +3VALW)

+3VALW_S5 — 60mil — JUML1 @ JUMP_43X39 — 60mil — +3.3V_LAN_S5

300mA,120ohm

+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

40 mils — Close to Pin 11,23

+3.3V_LAN_S5: CL1 .1U_0402_16V7K; CL2 .1U_0402_16V7K; @ CL5 4.7U_0603_6.3V6K; @ CL21 4.7U_0603_6.3V6K; @ CL8 4.7U_0603_6.3V6K; CL3 .1U_0402_16V7K — Close to Pin 32

60 mils — Close to pin 3,8,30,24

+LAN_VDDREG: CL4 .1U_0402_16V7K; CL6 .1U_0402_16V7K; CL7 .1U_0402_16V7K; CL9 .1U_0402_16V7K

close to UL1 pin11

LED Status

WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on

blinking

8111G resistor/8111H capacitor

RL14 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

RL17 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

RL20 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

RL15 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

RL18 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

RL21 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

RL16 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

RL19 NS0IX@ SD028000080 RTL8111G-CG_0ohm resistor

CL13~ CL16 need colse to UL1

Close to pin 22: @ CL12 SE00000UC00 1U_0201_6.3V6M; CL20 .1U_0402_16V7K

+3.3V_LAN_S5, +LAN_VDDREG

PCIE_PRX_LANTXP / PCIE_PRX_LANTXN — CL13 .1U_0402_16V7K; CL14 .1U_0402_16V7K — PCIE_PRX_C_LANTXP / PCIE_PRX_C_LANTXN

PCIE_PTX_LANRXP / PCIE_PTX_LANRXN — CL15 .1U_0402_16V7K; CL16 .1U_0402_16V7K — PCIE_PTX_C_LANRXP / PCIE_PTX_C_LANRXN

CLK_PCIE_LAN / CLK_PCIE_LAN# — CLK_PCIE_LAN / CLK_PCIE_LAN#

+3VS_S0, +3.3V_LAN_S5

RL1 10K_0402_5% — LAN_CLKREQ#_R

PCIE_WAKE#

RL3 1K_0402_5% — ISOLATE#

17,21,37,42,44 — PLT_RST#

RL6 15K_0402_5%

+3.3V_LAN_S5 — RL5 2.49K_0402_1% — UL1_RSET_P31

LAN_X2 / LAN_X1

UL1 (RTL8111H-CG QFN 32P_4X4, SA000080P00, S0IX@)

HSOP, HSON, HSIP, HSIN, REFCLK_P, REFCLK_N, CLKREQB, LANWAKEB, ISOLATEB, PERSTB, VDDREG, RSET, CKXTAL2, CKXTAL1

AVDD10, AVDD10, AVDD10, AVDD33, AVDD33, DVDD10

MDIP0, MDIN0, MDIP1, MDIN1, MDIP2, MDIN2, MDIP3, MDIN3

LAN_MIDI0+_R RL14 — LAN_MIDI0-_R RL15 — LAN_MIDI1+_R RL16 — LAN_MIDI1-_R RL17 — LAN_MIDI2+_R RL18 — LAN_MIDI2-_R RL19 — LAN_MIDI3+_R RL20 — LAN_MIDI3-_R RL21 — S0IX_EMI@ 0.1U_0402_25V6

LED2, LED1/GPIO, LED0

LAN_LED_ORG# — TL1; LAN_PHY_DIS# — TL2; LAN_LED_YEL# — TL3

LAN_PHY_DIS# 42

REGOUT — +LAN_VDDREG

GND

Pull up on PCH page14

+3VS_S0, +3.3V_LAN_S5 — RL8 10K_0402_5% — QL1 L2N7002WT1G_SC-70-3 SB00001GE00

14 CLKREQ_LAN# — LAN_CLKREQ#_R

UL1 NS0IX@ RTL8111G-CG SA00005V700

JRJ1

RL4 @ 0_0402_5% — CL17 .1U_0402_16V7K EMI@

LAN_MIDI0+ 1 TD1+ R1; LAN_MIDI0- 2 TD1- R2; LAN_MIDI1+ 3 TD2+ R3; LAN_MIDI1- 4 TD2- R4; JRJ1_CT_R5R6 5 CT R5; 6 CT R6; LAN_MIDI2+ 7 TD3+ R7; LAN_MIDI2- 8 TD3- R8; LAN_MIDI3+ 9 TD4+ R9; LAN_MIDI3- 10 TD4- R10

Yellow — RL7 510_0402_5% — LAN_LED_YEL# — LAN_LED_YEL#_R — 11 L1

20mils

+3.3V_LAN_S5 — 12 L2

GND 13, GND 14 — LAN_GND

CONN@ SP011312232

+3.3V_LAN_S5 — LAN_LED_YEL# — DCA3 PESD5V0U2BT_SOT23-3 SCA00000T00 ESD@

RL11 @ 0_0805_5%; RL12 @ 0_0805_5% — LAN_GND

+3.3V_LAN_S5 — RL13 @ 10K_0402_5% — LAN_PHY_DIS#

LAN_X1 — RL10 1M_0402_5% — LAN_X2

YL1 25MHZ_10PF_X3G025000DA1H-X SJ10000DE00 (OSC, NC, NC, OSC)

CL18 10P_0402_50V8J; CL19 10P_0402_50V8J

DL1 (ESD@ SC300001G00 AZC099-04S.R7G SOT23-6)

LAN_MIDI0+ — LAN_MIDI1- — LAN_MIDI1+ — LAN_MIDI0-

DL2 (ESD@ SC300001G00 AZC099-04S.R7G SOT23-6)

LAN_MIDI2+ — LAN_MIDI3- — LAN_MIDI3+ — LAN_MIDI2-

Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

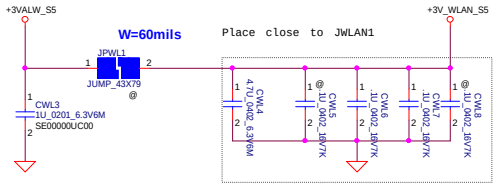
Compal Electronics, Inc.

Title: LAN RTL8111G/H

Size: Custom | Document Number: LA-F882P M/B | Rev: 0.2

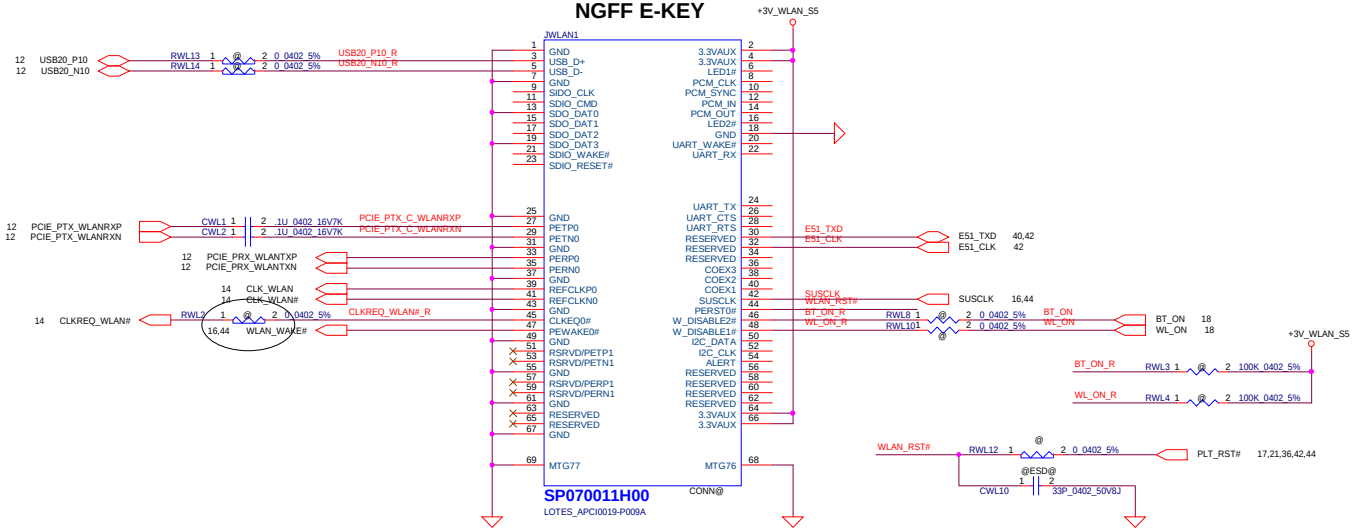
Date: Monday, April 09, 2018 | Sheet 36 of 66

WLAN (WIFI/BT Combo)



WLAN Conn.

NGFF E-KEY

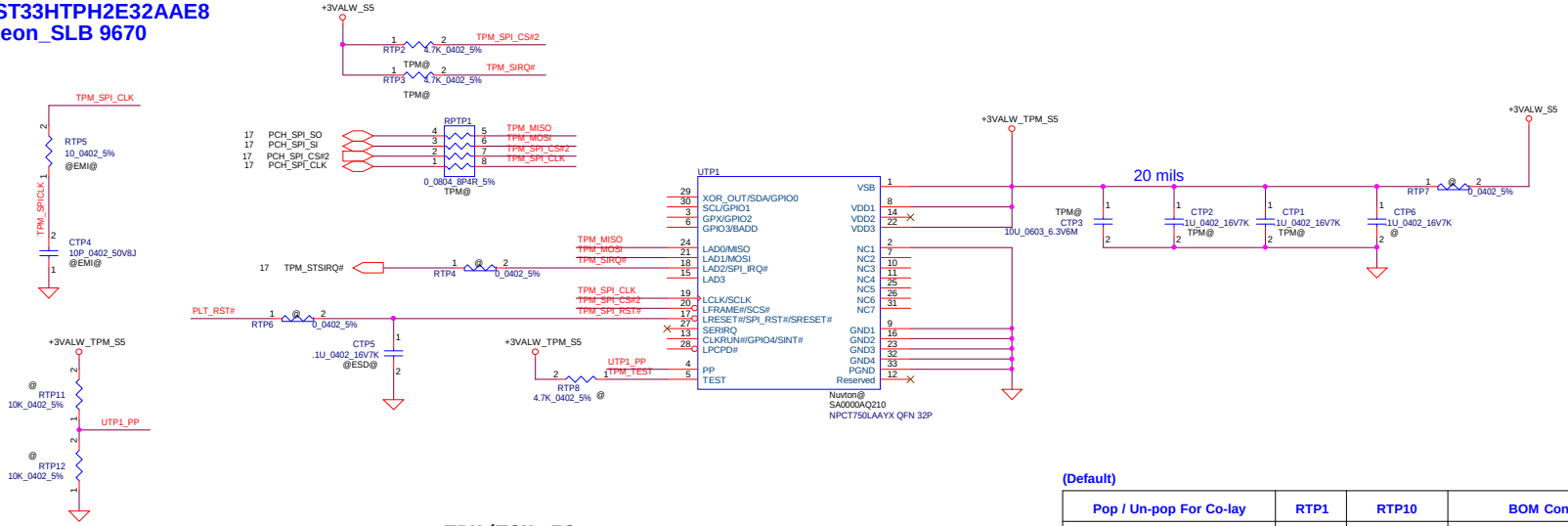


SP070011H00
LOTES_APCI0019-P009A

TPM 2.0 Co-lay

1.Nuvton_NPCT650LBAYX
2.ST_ST33HTPH2E32AAE8
3.Infineon_SLB 9670

NEW PART: Nuvoton NPCT650LBAYX (Default)
Infineon SLB 9670
ST ST33HTPH2E32AAE8



TPM/TCM IC

ST_ST33HTPH2E32AAE8(SPI)
SA00009SO40

Infineon_SLB 9670(SPI)
SA00009N230

(Default)

Pop / Un-pop For Co-lay	RTP1	RTP10	BOM Config
Nuvton_NPCT750LAAYX(SPI)	V	V	Nuvton@+TPM@
ST_ST33HTPH2E32AHB4(SPI)	X	X	ST@+TPM@
Infineon_SLB 9670VQ2(SPI)	X	X	Infineon@+TPM@

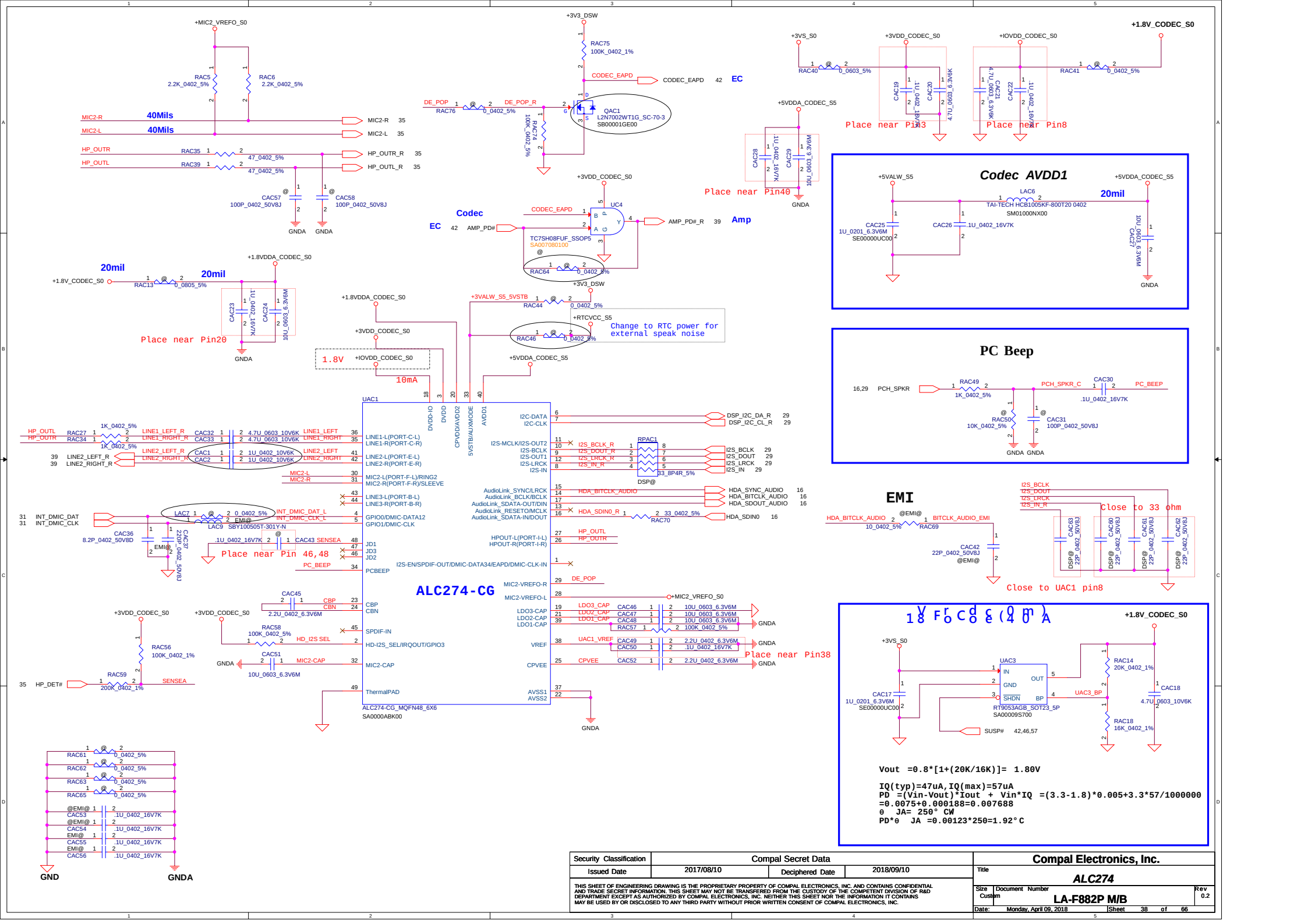
Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: **WLAN (NGFF) / TPM**

Size	Document Number	Rev
	LA-F882P M/B	0.2

Date: Monday, April 09, 2018 | Sheet 37 of 63


ALC274-CG
ALC274-CG_MQFN48_6X6
SA0000ABK00
UAC1
Codec AVDD1
PC Beep
EMI
Codec
Amp
EC
Place near Pin20
Place near Pin 46,48
Place near Pin38
Place near Pin40
Place near Pin33
Place near Pin8
Change to RTC power for external speak noise
Close to 33 ohm
Close to UAC1 pin8
Vout =0.8*[1+(20K/16K)]= 1.80V
IQ(typ)=47uA,IQ(max)=57uA
PD =(Vin-Vout)*Iout + Vin*IQ =(3.3-1.8)*0.005+3.3*57/1000000
=0.0075+0.000188=0.007688
θ JA= 250° CW
PD*θ JA =0.00123*250=1.92° C
Security Classification
Compal Secret Data
Issued Date
2017/08/10
Deciphered Date
2018/09/10
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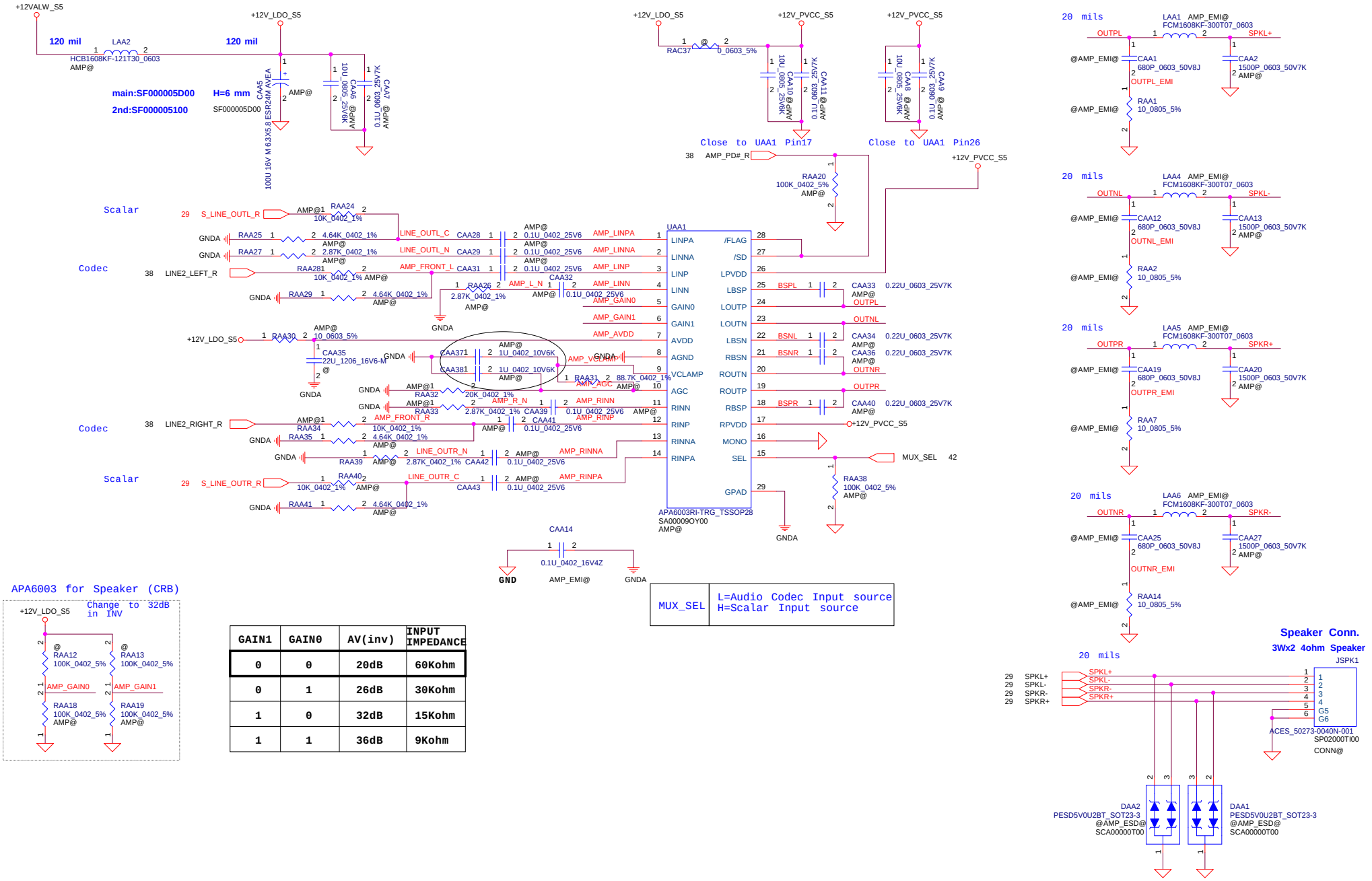
Compal Electronics, Inc.
Title
ALC274
Size
Custom
Document Number
LA-F882P M/B
Rev
0.2
Date:
Monday, April 09, 2018
Sheet
38
of
66



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

MUX_SEL	L=Audio Codec Input source H=Scalar Input source

Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: Amp ANPEC APA6003

Size	Document Number	Rev
Custom	LA-F882P M/B	0.2

Date: Monday, April 09, 2018 | Sheet 39 of 66

USB MUX Selection	
KDBG_MUX_SEL	Output
H	D = D2
L	D = D1

For WIN 7 Debug

Close to JIO1

USB D+/D- Swap

W=100mils 2.0A W=100mils

With Discharge Function

For U3 Side power

USB3.1 Gen2 Repeater

EQ setting of A(B) channel.
Default is Middle Level
L: TBD
M(Default): TBD
H: TBD

DE setting of A (B) channel.
Default is Middle Level.
L: TBD
M(Default): TBD
H: TBD

Chip Operation Mode Selection.
Default is Middle Level
L: Redriver Mode
M(Default): Redriver Mode for 5Gbps; Retimer Mode 10Gbps
H: Retimer Mode

To CPU

To Connector

TX

RX

Chip Enable. Active is high. Default is internal pull-down by 150K

SMBUS pull up on PCH side

PCH

I2C address setting. Internal pull down at 150kΩ , 3.3V
I/O.[ADDR1,ADDR0]=
LL: 0x50~0x53 (default)
LH: 0x54~0x57
HL: 0xE0~0xE3
HH: 0xE4~0xE7

Close to UUS9 IC

USB3.1 Gen 2 Conn.

RX

TX

W=80mil

For reserved EA fine ture redriver IC request

NXP

Place close to JUSB2

W=100mils 2.0A W=100mils

With Discharge Function

Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: Side USB3.0 x 1

Size	Document Number	Rev
C	LA-F882P M/B	0.2

Date: Monday, April 09, 2018 Sheet 40 of 66

Route	Width (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

USB3.1 Gen1 only

Type C conn

W = 200 mils

NPTH

Route	Width (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

Place close to JUSB2

Place close to JUSB2

SMART_PWRON#	Smart power on select
H	D = D2 No support Smart Power On
L	D = D1 Support Smart Power On

Place close to JUSB4

With Discharge Function

No Support BIOS recovery, EC debug only

USB2.0 Conn.

SP011412192

For USB2.0 debug port

With Discharge Function

2 port commen use part

Place close to JUSB5

USB2.0 Conn.

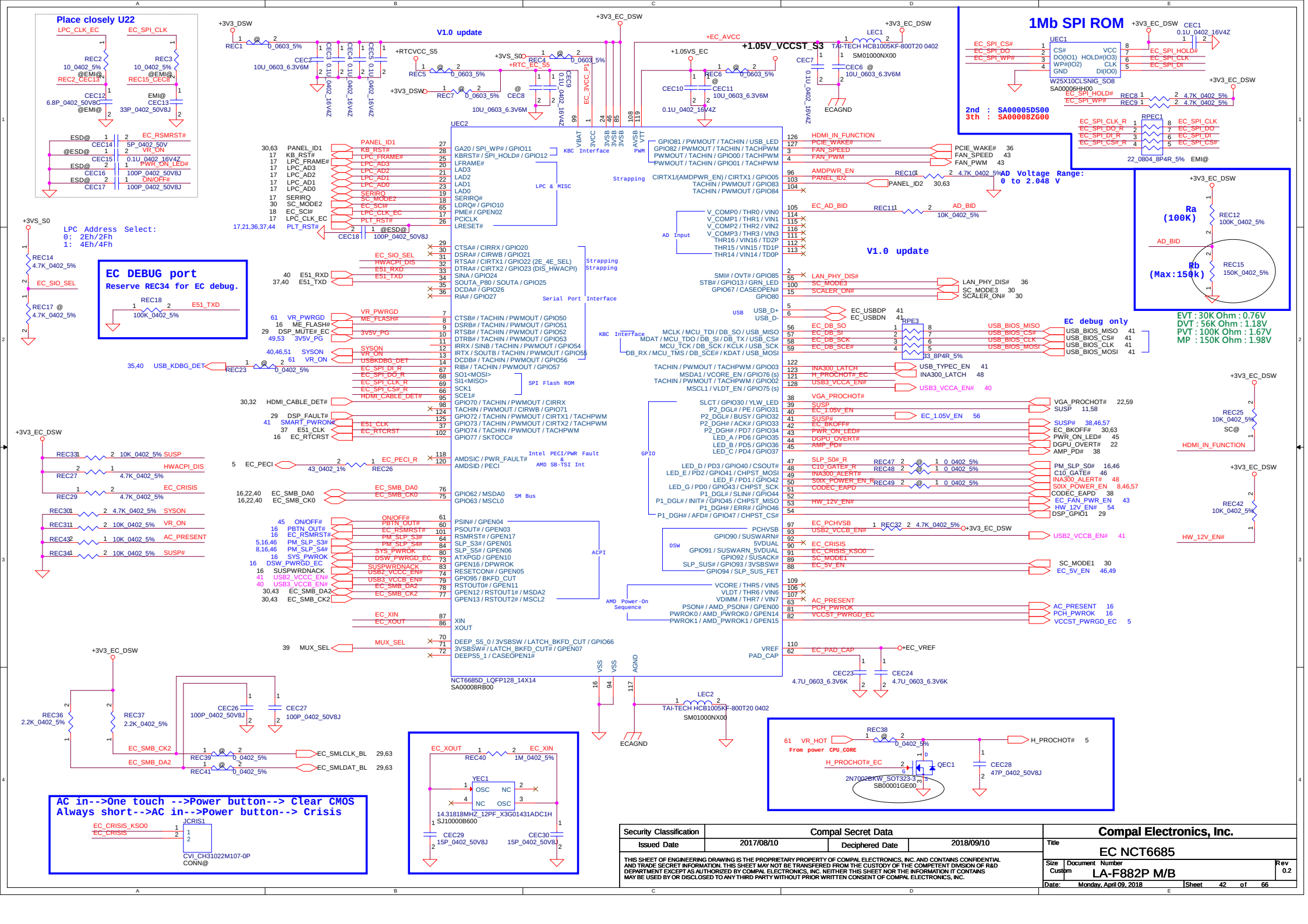
Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: Rear USB3.0 x 1

Size: Custom | Document Number: LA-F882P M/B | Rev: 0.2

Date: Monday, April 09, 2018 | Sheet 41 of 66


Place closely U22
LPC_CLK_EC
ESC_SPI_CLK
V1.0 update
+1.05V_VCCST_S3
1Mb SPI ROM
UEC1
W25X10CLSNIG_SO8
SA00006HH00
2nd : SA00005DS00
3th : SA00008ZG00
AD Voltage Range:
0 to 2.048 V
Ra
(100K)
Rb
(Max:150K)
EVT : 30K Ohm : 0.76V
DVT : 56K Ohm : 1.18V
PVT : 100K Ohm : 1.67V
MP : 150K Ohm : 1.98V
LPC Address Select:
0: 2Eh/2Fh
1: 4Eh/4Fh
EC DEBUG port
Reserve REC34 for EC debug.
EC debug only
V1.0 update
NCT6685D_LQFP128_14X14
SA00008RB00
AC in-->One touch -->Power button--> Clear CMOS
Always short-->AC in-->Power button--> Crisis
Security Classification
Compal Secret Data
Issued Date
2017/08/10
Deciphered Date
2018/09/10
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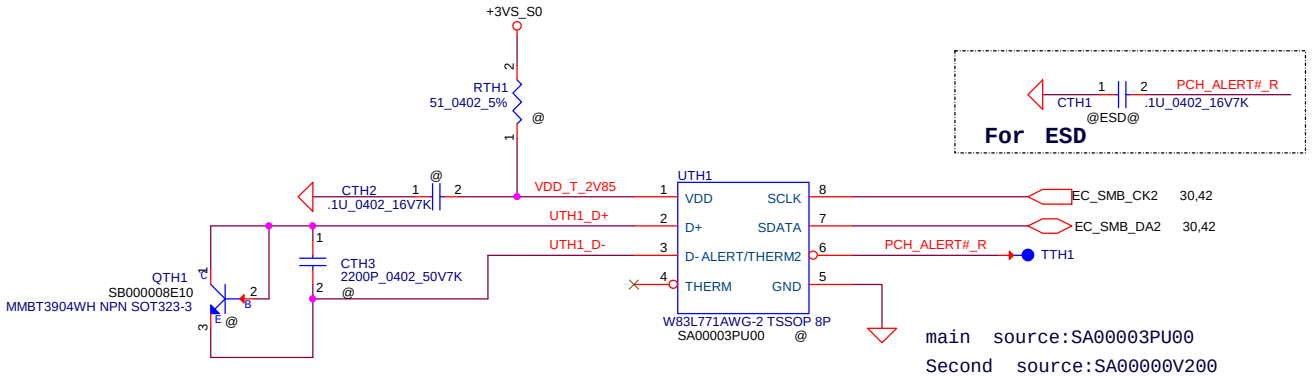
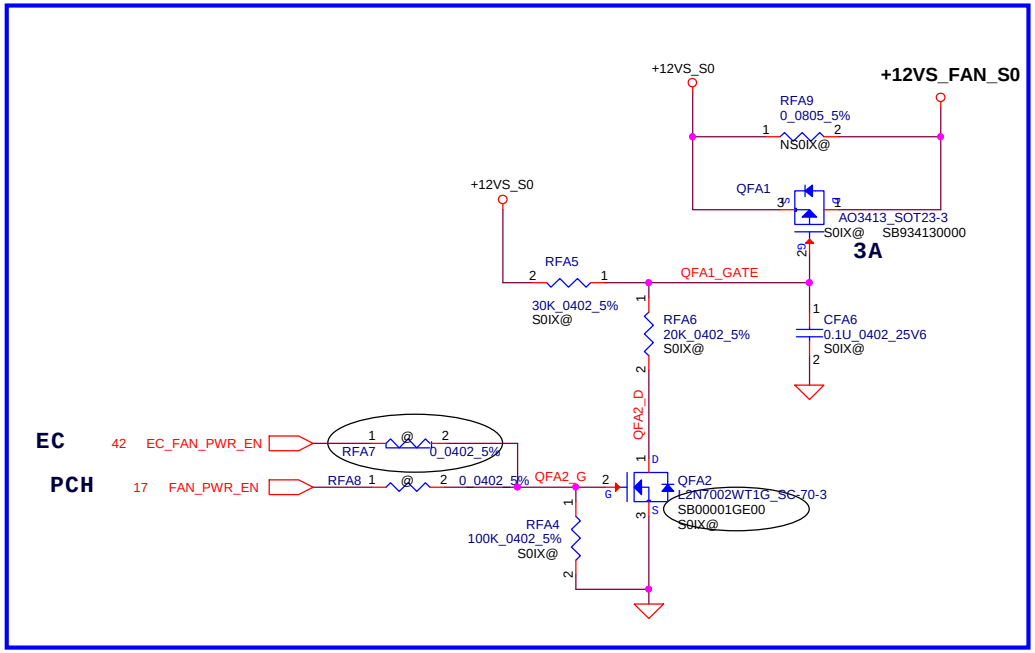
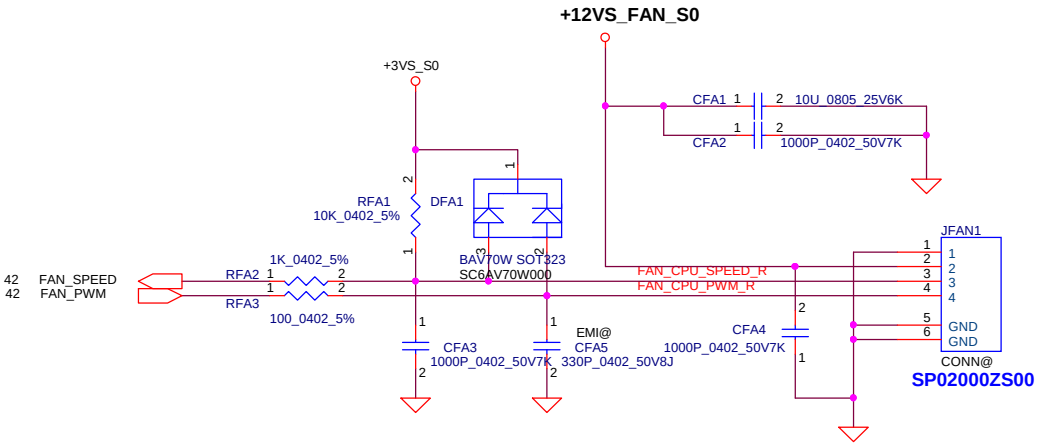
Compal Electronics, Inc.
Title
EC NCT6685
Size
Custom
Document Number
LA-F882P M/B
Rev
0.2
Date: Monday, April 09, 2018
Sheet 42 of 66

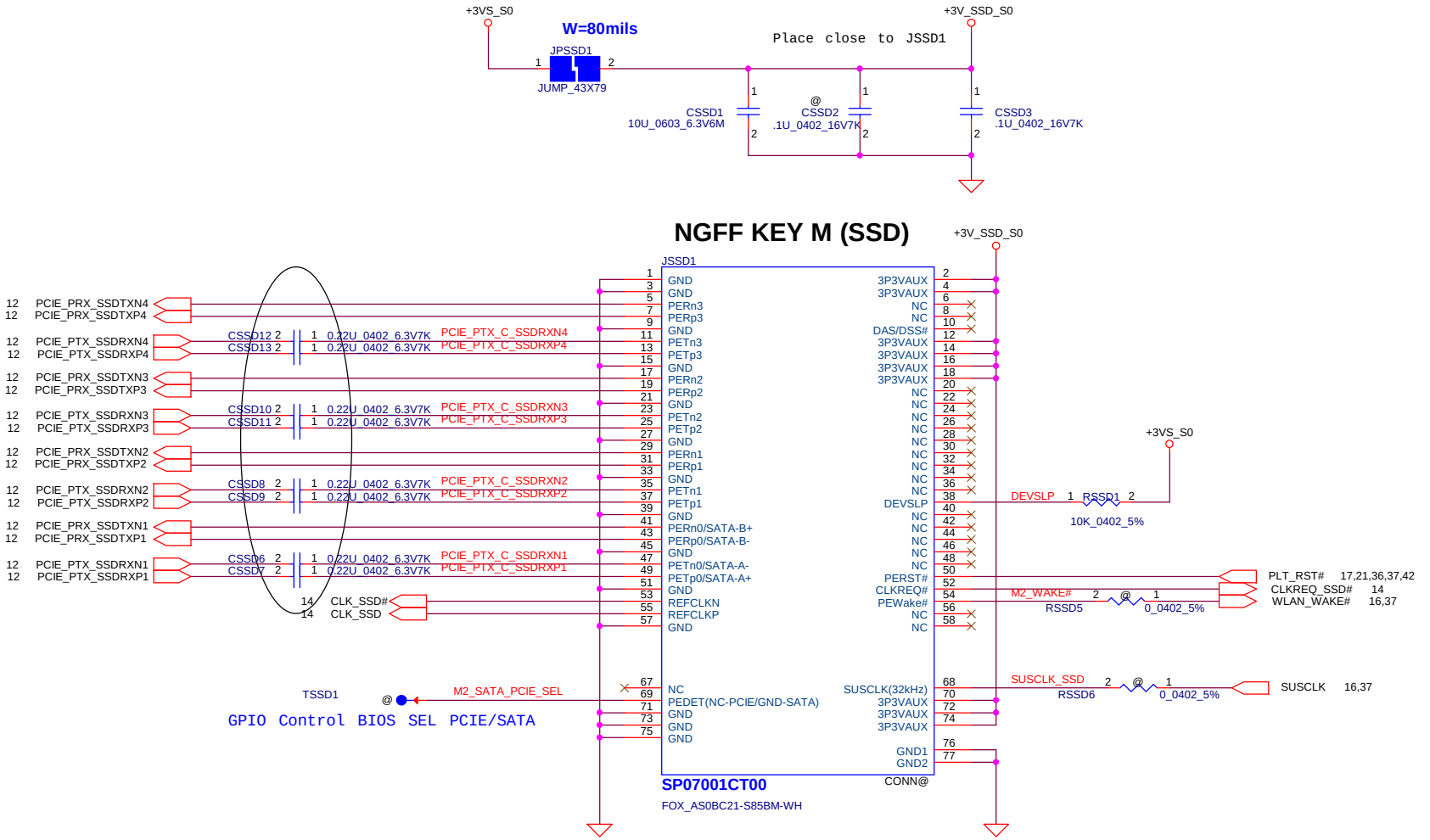






Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.	
Title	FAN/Thermal Sensor
Size	Document Number: LA-F882P M/B
Rev	0.2
Date: Monday, April 09, 2018	Sheet 43 of 66



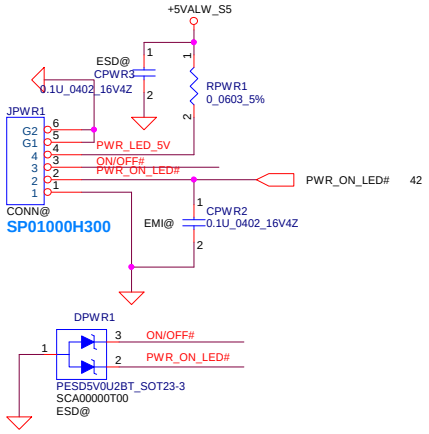
Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: ***SSD (M.2)***

Size	Document Number	Rev
B	LA-F882P M/B	0.2

Date: Monday, April 09, 2018 Sheet 44 of 66



BARCODE

ZZZ5 @ BARCODE_8X8

ZZZ6 @ BARCODE_12X4

ZZZ7 @ BARCODE_20X4

ZZZ8 @ BARCODE_10X10

VRAM GDDR5

ZZZ10 X76
Part Number = X7673838L53
X76_Micron4G@

ZZZ11 X76
Part Number = X7673838L52
X76_SAM4G@

ZZZ12 X76
Part Number = X7673838L51
X76_Hynix4G@

R3 part

CPU

UC1 IC CM8067702868416 QKHE B0 2.9G LGA 1151
AB000012900
i7-7700T @

UC1 IC CM8067702867915 QKHH B0 2.4G LGA 1151
AB000012600
i5-7400T @

UC1 IC CM8067703015810 QL3M S0 3.5G LGA 1151
AB000012J00
i3-7100T @

UC1 IC CM8067703016114 QL3T S0 2.9G LGA 1151
AB000012I00
G4560T @

PCH

R1 part

UH1 S IC FHSSKU01 QNDN A1 FCBGA 874P PCH-H
SA0000BXA00
B360_R1@

R3 part

UH1 S IC FHSSKU01 QNDN A1 FCBGA 874P PCH-H
SA0000BXA10
B360@

GPU

R1 part

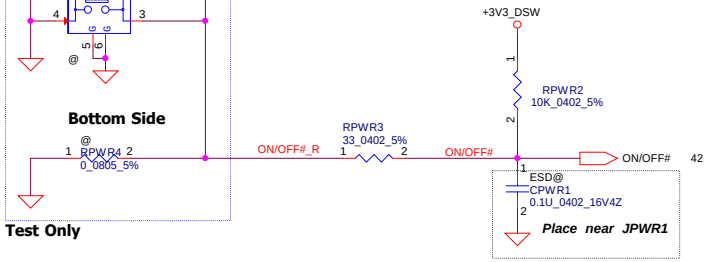
UV1 DIS_R1@
S IC 216-0905004 A1 R17M-P1-70 FCBGA 769P 0FA
SA0000ALX10

R3 part

UV1 DIS@
S IC 216-0905004 A1 R17M-P1-70 ABO!
SA0000ALX30

Power Button

ON/OFF switch
TOP Side
SW1
NTC017-DA1J-D160T_4P
SN100005J00
MP un-mount
Bottom Side
RPWR4
0_0805_5%
Test Only



WIFI Screw Hole

4.2mm x 1

H1 H_4P2

SSD Screw Hole

6.2mm x 2

H2 H_6P2
H3 H_6P2

PCB

ZZZ1 DAZ@
PCB LA-F882P
DAZ28O00301

IO board:DA6001UH010
power board:DA60020L010

PCB Screw Hole

4.2 mm x 1

H18 H_4P2X4P6-G

4.2 mm x 1

H17 H_4P2-G

4.0 mm x 6

H21 H_4P0-G
H22 H_4P0-G
H23 H_4P0-G
H24 H_4P0-G
H25 H_4P0-G
H19 H_4P0-G

CPU Screw Hole

5.4mm x 4

H4 H_5P4
H5 H_5P4
H7 H_5P4
H6 H_5P4

3.8 mm x 3

H8 H_3P8
H10 H_3P8
H9 H_3P8

GPU Screw Hole

3.3 mm x 4

H15 H_3P3
H11 H_3P3
H28 H_3P3
H16 H_3P3

Other

1.2 mm x 3

H29 H_1P2N
H30 H_1P2N
H31 H_1P2N

FD1 FD2 FD3 FD4

Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

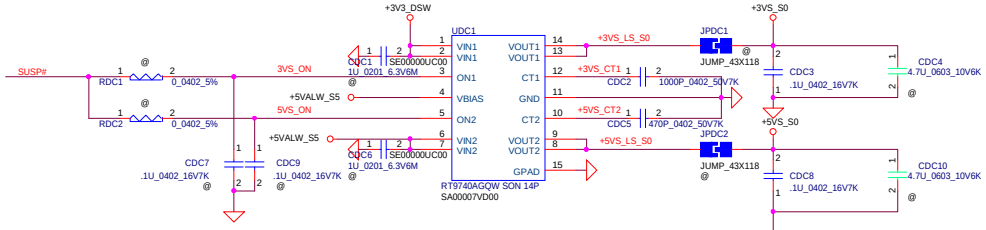
Compal Electronics, Inc.

Title: PWR SW/LED/SCREW

Size	Document Number	Rev
Custom	LA-F882P M/B	0.2

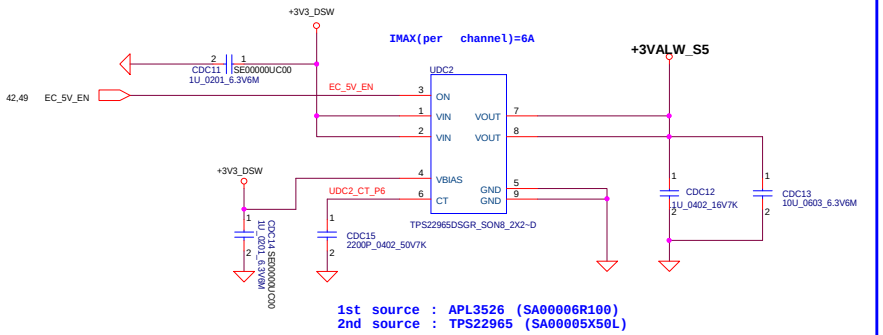
Date: Monday, April 09, 2018 Sheet 45 of 66

VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

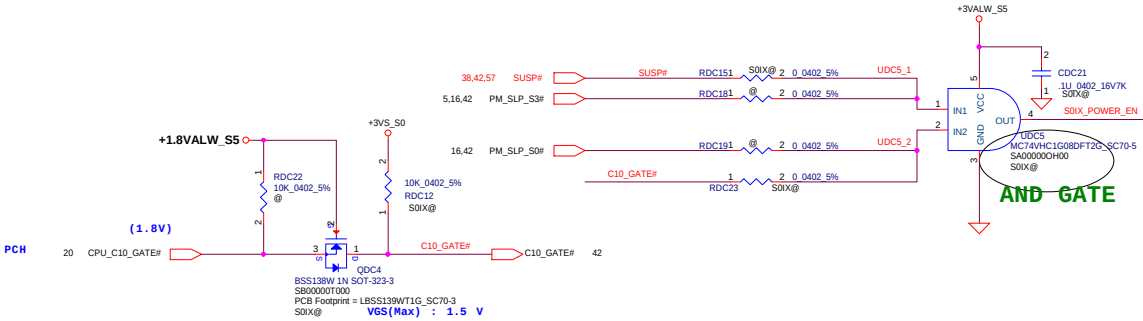


1st source : RT9740AGQW (SA00007VD00)
2nd source : xxxxxxx (xxxxxxx)

+3VDSW_S5 to +3VALW_S5 Transfer



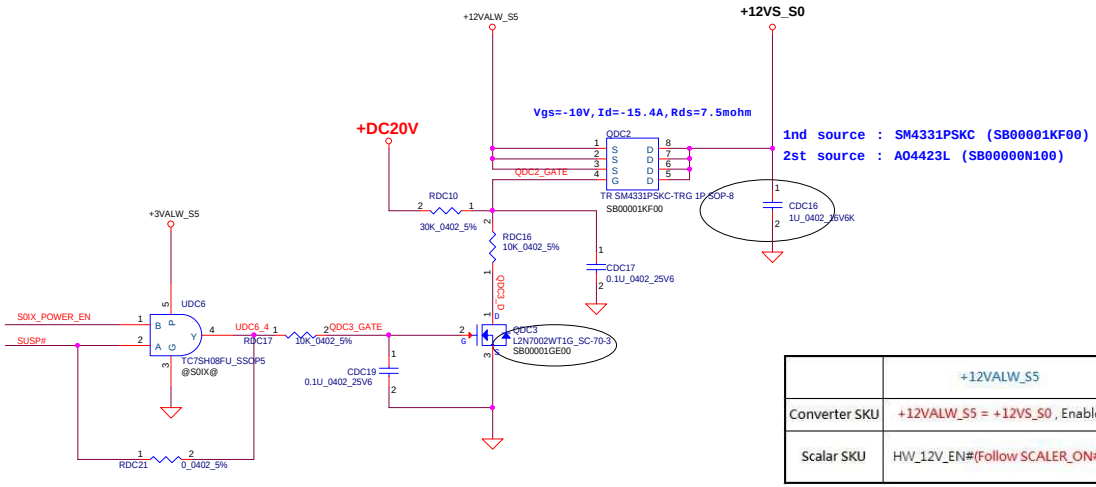
1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)

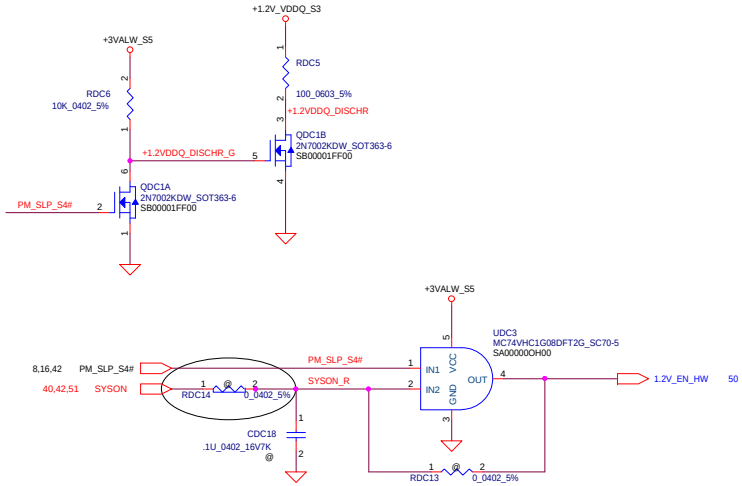


1st source : BSS138W (SB00000T000)
2nd source : LBSS139WT1G (SB00001GC00)
VGS(Max) : 1.5 V

Link to power & EC

+12VALW_S5 TO +12VS_S0 (PMOS)





	+12VALW_S5	+12VS_S0	BOM
Converter SKU	+12VALW_S5 = +12VS_S0 , Enable: HW_12V_EN# (Follow SPL_S3#)		RDC7,RDC8,RDC9
Scalar SKU	HW_12V_EN#(Follow SCALER_ON#)	SUSP# (Follow SPL_S3#)	QDC2,RDC10,RDC16,RDC17,CDC19,CDC17

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/10	Deciphered Date 2018/09/10	Title: DC INTERFACE
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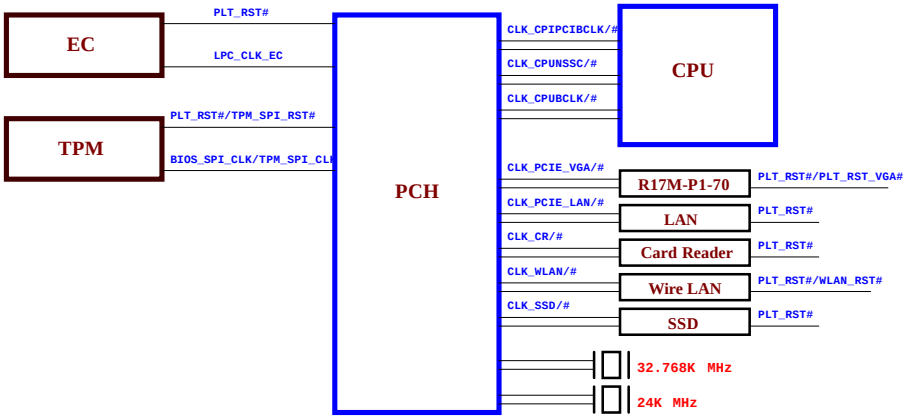
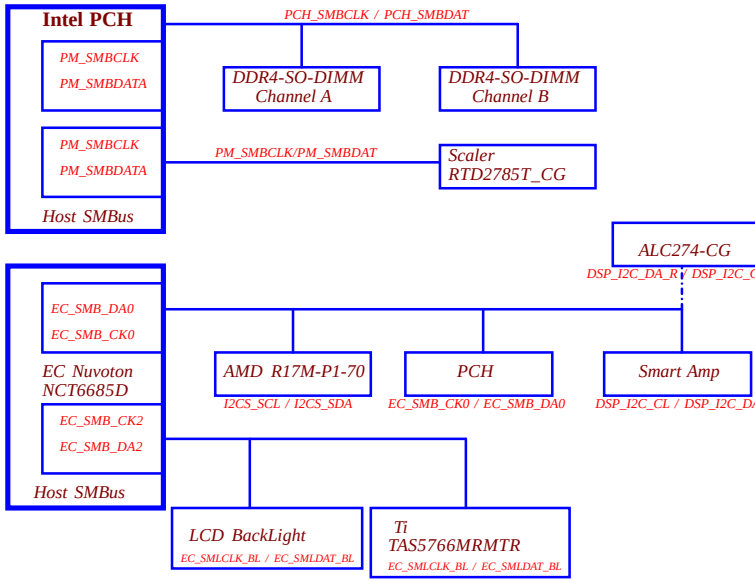
System clock and Reset map



SMBUS Block Diagram



Group	Pin	ULT SPEC	Power well	Default Internal Pull H / L	Strapping Usage	Default	SCI / SMI / NMI	BBA10	BBA10 Default Internal Pull H / L
GPD	BD13	GPD0 / BATLOW#	DSW			Native		PM_BATLOW#	PU 8.2K to +3VALW_DSW_S5
	BB15	GPD1 / ACPRESENT	DSW			Native		AC_PRESENT_R	PU 10K to +3VALW_DSW_S5(@)
	BD11	GPD2 / LAN_WAKE#	DSW			Native		LAN_WAKE#	PU 10K to +3VALW_DSW_S5
	AT13	GPD3 / PWRBTN#	DSW			Native		PBTN_OUT#_R	PU 100K to +3VALW_DSW_S5
	AW15	GPD4 / SLP_S3#	DSW			Native		PM_SLP_S3#	
	BD15	GPD5 / SLP_S4#	DSW			Native		PM_SLP_S4#	
	BC15	GPD6 / SLP_A#	DSW			Native		PM_SLP_A#	Testpoint
	BD14	GPD7 / RSVD	DSW			N/A			
	AN15	GPD8 / SUSCLK	DSW			Native		SUSCLK	PD 1K(@)
	AV13	GPD9 / SLP_WLAN#	DSW			Native		PM_SLP_LAN#	Testpoint
	BA13	GPD10 / SLP_S5#	DSW			Native		PM_SLP_S5#	Testpoint
	AR15	GPD11 / LANPHYPC	DSW			Native		LANPHYPC	Testpoint
GPP_A	AT17	GPP_A0 / RCIN#	Primary(3.3V/1.8V)			Native	SCI	KB_RST#	PU 10K to +3VS_S0
	AT22	GPP_A1 / LAD0 / ESPI_IO0	Primary(3.3V/1.8V)			Native	SCI	LPC_AD0	
	AY22	GPP_A2 / LAD1 / ESPI_IO1	Primary(3.3V/1.8V)			Native	SCI	LPC_AD1	
	AT19	GPP_A3 / LAD2 / ESPI_IO2	Primary(3.3V/1.8V)			Native	SCI	LPC_AD2	
	BD16	GPP_A4 / LAD3 / ESPI_IO3	Primary(3.3V/1.8V)			Native	SCI	LPC_AD3	
	BE16	GPP_A5 / LFRAME# / ESPI_CS#	Primary(3.3V/1.8V)			Native	SCI	LPC_FRAME#	
	BA17	GPP_A6/SERIRQ/ESPI_CS1#	Primary(3.3V/1.8V)			Native	SCI	SERIRQ	PU 10K to +3VS_S0
	AW17	GPP_A7/PIRQA#/ESPI_ALERT0#	Primary(3.3V/1.8V)			Native	SCI	LPC_PIRQA#	PU 10K to +3VALW_S5
	AW22	GPP_A8 / CLKRUN#	Primary(3.3V/1.8V)			Native	SCI	TPM_CLKRUN#	PU 8.2K to +3VS_TPM_S0
	BC17	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK	Primary(3.3V/1.8V)			Native	SCI	LPC_CLKOUT0	
	AV19	GPP_A10 / CLKOUT_LPC1	Primary(3.3V/1.8V)			Native	SCI	LPC_CLKOUT1	
	BD17	GPP_A11 /PME#	Primary(3.3V/1.8V)			Native	SCI	PCH_PME#	PU 100K to +3V_1.8V_PGPPA_S5
	BB17	GPP_A12/BM_BUSY#/ISH_GP6#/SX_EXIT_HOLDOFF#	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIOA12	Testpoint
	BD19	GPP_A13 / SUSWARN# / SUSPWRDNACK	Primary(3.3V/1.8V)			Native	SCI	SUSWARN#_R	
	BC18	GPP_A14/SUS_STAT#/ESPI_RESET#	Primary(3.3V/1.8V)			Native	SCI	SUS_STAT#	
	BB19	GPP_A15 / SUSACK#	Primary(3.3V/1.8V)			Native	SCI	SUSACK#	
	AR17	GPP_A16/CLKOUT_48	Primary(3.3V/1.8V)			GPI	SCI	GPP_A16_CLKOUT	Testpoint
	BC19	GPP_A17/ISH_GP7	Primary(3.3V/1.8V)			GPI	SCI		
	BB22	GPP_A18 / ISH_GP0	Primary(3.3V/1.8V)			GPI	SCI		
	BD21	GPP_A19 / ISH_GP1	Primary(3.3V/1.8V)			GPI	SCI		
	BD22	GPP_A20 / ISH_GP2	Primary(3.3V/1.8V)			GPI	SCI		
	BE21	GPP_A21 / ISH_GP3	Primary(3.3V/1.8V)			GPI	SCI		
	BD18	GPP_A22 / ISH_GP4	Primary(3.3V/1.8V)			GPI	SCI		
	BC22	GPP_A23 / ISH_GP5	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIOA23	Testpoint
GPP_B	AR27	GPP_B0	Primary(3.3V/1.8V)			GPO	SCI		
	AL27	GPP_B1	Primary(3.3V/1.8V)			GPO	SCI		
	BD22	GPP_B2 / VRALERT#	Primary(3.3V/1.8V)			GPI	SCI	VRALERT#	PU 10K to +3VALW_DSW_S5(@)
	BC23	GPP_B3 / CPU_GP2	Primary(3.3V/1.8V)			GPI	SCI		
	BD24	GPP_B4 / CPU_GP3	Primary(3.3V/1.8V)			GPI	SCI		
	BC24	GPP_B5 / SRCCLKREQ0#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_VGA#	PU 10K to +3VS+S0
	AW24	GPP_B6 / SRCCLKREQ1#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_LAN#	PU 10K to +3VS+S0
	AT24	GPP_B7 / SRCCLKREQ2#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_CR#	PU 10K to +3VS+S0
	BD25	GPP_B8 / SRCCLKREQ3#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_WLAN#	PU 10K to +3VS+S0
	BB24	GPP_B9 / SRCCLKREQ4#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#4	PU 10K to +3VS+S0
	BE25	GPP_B10 / SRCCLKREQ5#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#5	PU 10K to +3VS+S0
	AN24	GPP_B11	Primary(3.3V/1.8V)			GPO	SCI	MPHY_EXT_PWR	PU 200K to +2VALW_S5
	BC26	GPP_B12 / SLP_S0#	Native			Native	SCI	PM_SLP_S0#	
	BB27	GPP_B13 / PLTRST#	Primary(3.3V/1.8V)			Native	SCI	PCH_PLT_RST#	
	BD26	GPP_B14 / SPKR	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	Yes	PCH_SPKR	Strap for Top Swap override 0=Enable; L=Disable(Default) PU 100K to +3VS_S0(@) L(20K)
	AR24	GPP_B15 / GSPI0_CS#	Primary(3.3V/1.8V)			GPI	SCI		
	BD27	GPP_B16 / GSPI0_CLK	Primary(3.3V/1.8V)			GPI	SCI	USB_UART_SEL	PU 100K to +3VALW_S5
	BD27	GPP_B17 / GSPI0_MISO	Primary(3.3V/1.8V)			GPI	SCI		
	BD28	GPP_B18 / GSPI0_MOSI	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	SCI	GSPI0_MOSI	Strap for Re-Reboot 0=Disable(Default); L=Enable PU 4.7K to +3VS_S0(@) L(20K)
	BC27	GPP_B19 / GSPI1_CS#	Primary(3.3V/1.8V)			GPI	SCI	WCAM_PWREN	PD 100K(@)
	AV29	GPP_B20 / GSPI1_CLK	Primary(3.3V/1.8V)		Yes	GPO	SCI	WCAM_RST_CPU	
	AR29	GPP_B21 / GSPI1_MISO	Primary(3.3V/1.8V)			GPI	SCI	CPU_GP0021	PU 10K to +3VS
	AT29	GPP_B23 / GSPI1_MOSI	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	SCI	GSPI1_MOSI	Strap for BIOS Boot 0=LPC; L=SPI(Default) PU 10K to +3VS_S0 (@) L(20K)
	AT27	GPP_B25 / SMLALERT#B / PCHHOT#	Primary(3.3V/1.8V)	L(20K)		GPO	Yes	SMLALERT1#	Testpoint L(20K)
	AW44	GPP_C0 / SMBCLK	Primary(3.3V/1.8V)			Native	SCI	PM_SMBCLK	PU 2.2K to +2VALW_S5
	BB43	GPP_C1 / SMBDATA	Primary(3.3V/1.8V)			Native	SCI	PM_SMBDATA	PU 2.2K to +2VALW_S5
	BB41	GPP_C2 / SMBALERT#	Primary(3.3V/1.8V)	hpd	Yes	GPO	SCI	SMLALERT#	Strap for TLS Confidentiality 0=Enable; L=Disable(Default) PU 4.7K to +3VALW_S5 L(20K)
	AY44	GPP_C3 / SMLI2C0	Primary(3.3V/1.8V)			Native	SCI	PCH_SMLI2C0	PU 499 to +3VS_S0
	BB39	GPP_C4 / SMLI2DATA0	Primary(3.3V/1.8V)			Native	SCI	PCH_SMLI2DATA0	PU 499 to +3VS_S0
	BA40	GPP_C5 / SMLI0ALERT#	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	SCI	SMLALERT0#	Strap for eSPI/LPC mode selection 0=eSPI(Default); L=LPC PU 4.7K to +3VALW_S5(@) L(20K)
	AW42	GPP_C6 / SMLI1CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SMLI1CLK1	PU 1K to +3VS_S0
	AW45	GPP_C7 / SMLI1DATA	Primary(3.3V/1.8V)			GPO	SCI	PCH_SMLI2DATA1	PU 1K to +3VS_S0
	BA41	GPP_C8 / UART0_RXD	Primary(3.3V/1.8V)			GPI	SCI		
	BA42	GPP_C9 / UART0_TXD	Primary(3.3V/1.8V)			GPI	SCI		
GPP_C	AV43	GPP_C10 / UART0_RTS#	Primary(3.3V/1.8V)			GPI	SCI		
	AU44	GPP_C11 / UART0_CTS#	Primary(3.3V/1.8V)			GPI	SCI	BT_ON	+3VS_WLAN_S5
	AU43	GPP_C12 / UART1_RXD / ISH_UART1_RXD	Primary(3.3V/1.8V)			GPI	SCI	DGPU_PWR_EN	
	AT43	GPP_C13 / UART1_TXD / ISH_UART1_TXD	Primary(3.3V/1.8V)			GPI	SCI	DGPU_HOLD_RST#	
	AT44	GPP_C14 / UART1_RTS# / ISH_UART1_RTS#	Primary(3.3V/1.8V)			GPI	SCI		
	AU41	GPP_C15 / UART1_CTS# / ISH_UART1_CTS#	Primary(3.3V/1.8V)			GPI	SCI		Enable Pull H
	AT42	GPP_C16 / I2C0_SDA	Primary(3.3V/1.8V)			GPI	SCI		
	AR39	GPP_C17 / I2C0_SCL	Primary(3.3V/1.8V)			GPI	SCI		
	AR44	GPP_C18 / I2C1_SDA	Primary(3.3V/1.8V)			GPI	SCI		
	AR41	GPP_C19 / I2C1_SCL	Primary(3.3V/1.8V)			GPI	SCI		
	AR45	GPP_C20 / UART2_RXD	Primary(3.3V/1.8V)			GPI	SCI	UART_2_CRXD_DTXD	PU 49.9K to +3VS_S0
GPP_D	AR39	GPP_C21 / UART2_TXD	Primary(3.3V/1.8V)			GPI	SCI	UART_2_CTXD_DRXD	PU 49.9K to +3VS_S0
	AN44	GPP_C22 / UART2_RTS#	Primary(3.3V/1.8V)			GPI	Yes	UART_2_CRTS_DCTS	PU 49.9K to +3VS(@)
	AN43	GPP_C23 / UART2_CTS#	Primary(3.3V/1.8V)			GPI	Yes		
	AL39	GPP_D0 / SPI1_CS#	Primary(3.3V/1.8V)			GPI	Yes		
	AN39	GPP_D1 / SPI1_CLK	Primary(3.3V/1.8V)			GPI	Yes		
	AN38	GPP_D2 / SPI1_MISO	Primary(3.3V/1.8V)			GPI	Yes		
	AN41	GPP_D3 / SPI1_MOSI	Primary(3.3V/1.8V)			GPI	Yes		
	AM44	GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA	Primary(3.3V/1.8V)			GPI	Yes		
	AJ33	GPP_D5/SX_SFR#	Primary(3.3V/1.8V)			GPI	SCI		
	AM43	GPP_D6/I2S_TXD	Primary(3.3V/1.8V)			GPI	SCI		
	AN42	GPP_D7/I2S0_RXD	Primary(3.3V/1.8V)			GPI	SCI		
	AL42	GPP_D8/I2S0_SCLK	Primary(3.3V/1.8V)			GPI	SCI		
	AL44	GPP_D9	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIOD9	Testpoint
	AL36	GPP_D10	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIOD10	Testpoint
	AL35	GPP_D11	Primary(3.3V/1.8V)			GPI	SCI	CPU_GPIOD11	Testpoint
	AJ39	GPP_D12	Primary(3.3V/1.8V)			GPI	SCI	CPU_GPIOD12	Testpoint
	AK45	GPP_D13/ISH_UART0_RXD/SML0BDAT	Primary(3.3V/1.8V)			GPI	SCI	CPU_GPIOD13	Testpoint
	AK46	GPP_D14/ISH_UART0_TXD/SML0BCLK	Primary(3.3V/1.8V)			GPI	SCI	CPU_GPIOD14	Testpoint
	AL43	GPP_D15 / ISH_UART0_RTS#	Primary(3.3V/1.8V)			GPI	SCI	CPU_GPIOD15	Testpoint
	AJ43	GPP_D16 / ISH_UART0_CTS# / SML0BALERT#	Primary(3.3V/1.8V)			GPI	SCI	CPU_GPIOD16	Testpoint
	AJ42	GPP_D17 / DMIC_CLK1	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICCLK1	Testpoint
	AJ38	GPP_D18 / DMIC_DATA1	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICDAT1	Testpoint
	AJ35	GPP_D19 / DMIC_CLK0	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICCLK0	Testpoint
	AH44	GPP_D20 / DMIC_DATA0	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICDAT0	Testpoint
	AG44	GPP_D21 / SPI1_IO2	Primary(3.3V/1.8V)			GPI	SCI		
	AH43	GPP_D22 / SPI1_IO3	Primary(3.3V/1.8V)			GPI	SCI		
	AJ44	GPP_D23 / PM_SYNC_ACK/ISH_GP8/SX_EXIT_HOLDOFF_ACK	Primary(3.3V/1.8V)			GPI	SCI		
GPP_E	AG35	GPP_E0 / SATAXPCIE0 / SATAGP0	Native			Native	Yes	SATA_GP0	PU 10K to +3VS_S0
	AG35	GPP_E1 / SATAXPCIE1 / SATAGP1	Primary(3.3V/1.8V)			Native	Yes	SATA_GP1	PU 10K to +3VS_S0
	AG39	GPP_E2 / SATAXPCIE2 / SATAGP2	Primary(3.3V/1.8V)			Native	Yes	SATA_GP2	PU 10K to +3VS_S0
	AF41	GPP_E3 / CPU_GP0	Primary(3.3V/1.8V)			GPI	Yes	DGPU_PWROK	PU 10K to +3VS_S0
	AG43	GPP_E4 / DEVSLP0	Primary(3.3V/1.8V)			GPI	Yes		
	AG43	GPP_E5 / DEVSLP1	Primary(3.3V/1.8V)			GPI	Yes		
	AE45	GPP_E6 / DEVSLP2	Primary(3.3V/1.8V)			GPI	Yes		
	AE44	GPP_E7 / CPU_GP1	Primary(3.3V/1.8V)			GPI	Yes		
	AD44	GPP_E8 / SATALED#	Primary(3.3V/1.8V)			GPI	Yes	SATA_LED#	PU 10K to +3VS_S0
	AD43	GPP_E9 / USB2_OC0#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC0#	PU 10K to +3VALW_S5 L(20K)
	AD42	GPP_E10 / USB2_OC1#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC1#	PU 10K to +3VALW_S5 L(20K)
	AD39	GPP_E11 / USB2_OC2#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC2#	PU 10K to +3VALW_S5 L(20K)
GPP_F	AC44	GPP_E12 / USB2_OC3#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC3#	PU 10K to +3VALW_S5 L(20K)
	AD35	GPP_F0/SATAXPCIE3/SATAGP3	Primary(3.3V/1.8V)			Native	SCI	SATA_GP3	PU 10K to +3VS _S0
	AD31	GPP_F1/SATAXPCIE4/SATAGP4	Primary(3.3V/1.8V)			Native	SCI	SATA_GP4	Testpoint
	AD38	GPP_F2/SATAXPCIE5/SATAGP5	Primary(3.3V/1.8V)			Native	SCI	SATA_GP5	Testpoint
	AC43	GPP_F3/SATAXPCIE6/SATAGP6	Primary(3.3V/1.8V)			Native	SCI	SATA_GP6	Testpoint
	AB44	GPP_F4/SATAXPCIE7/SATAGP7	Primary(3.3V/1.8V)			Native	SCI	SATA_GP7	Testpoint
	AB41	GPP_F5/DEVSLP3	Primary(3.3V/1.8V)			GPI	SCI		
	AB42	GPP_F6/DEVSLP4	Primary(3.3V/1.8V)			GPI	SCI		
	AB43	GPP_F7/DEVSLP5	Primary(3.3V/1.8V)			GPI	SCI		
	AB36	GPP_F8/DEVSLP6	Primary(3.3V/1.8V)			GPI	SCI		
	AB39	GPP_F9/DEVSLP7	Primary(3.3V/1.8V)			GPI	SCI		
	AB33	GPP_F10/SCLOCK	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F10	Testpoint
	AB35	GPP_F11/SLOAD	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F11	Testpoint
	AA45	GPP_F12/SDATAOUT1	Primary(3.3V/1.8V)			GPI	SCI		
	AA44	GPP_F13/SDATAOUT0	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F13	Testpoint
	Y44	GPP_F14	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F14	Testpoint
	Y43	GPP_F15/USB2_OC8_4	Primary(3.3V/1.8V)			GPI	SCI	USB_OC#4	Testpoint
	Y41	GPP_F16/USB2_OC9_5	Primary(3.3V/1.8V)			GPI	SCI	USB_OC#5	Testpoint
	W44	GPP_F17/USB2_OC8_6	Primary(3.3V/1.8V)			GPI	SCI	USB_OC#6	Testpoint
	W43	GPP_F18/USB2_OC9_7	Primary(3.3V/1.8V)			GPI	SCI	USB_OC#7	Testpoint
	W42	GPP_F19/EDP_VDDEN	Primary(3.3V/1.8V)			GPI	SCI	LIMA_ENVDD	Testpoint
	W35	GPP_F20/EDP_BKLTEN	Primary(3.3V/1.8V)			GPI	SCI	BKLTN_PCH	
	W36	GPP_F21/EDP_BKLTCTL	Primary(3.3V/1.8V)			GPI	SCI	BKL_PWM_PCH	
	W39	GPP_F22	Primary(3.3V/1.8V)			GPI	SCI		
	V44	GPP_F23	Primary(3.3V/1.8V)			GPI	SCI		
GPP_G	U43	GPP_G0/FAN_TACH_0	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G0	Testpoint
	U42	GPP_G1/FAN_TACH_1	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G1	Testpoint
	U41	GPP_G2/FAN_TACH_2	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G2	Testpoint
	M44	GPP_G3/FAN_TACH_3	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G3	Testpoint
	U36	GPP_G4/FAN_TACH_4	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G4	Testpoint
	P44	GPP_G5/FAN_TACH_5	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G5	Testpoint
	T45	GPP_G6/FAN_TACH_6	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G6	Testpoint
	T44	GPP_G7/FAN_TACH_7	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G7	Testpoint
	R44	GPP_G8/FAN_PWM_0	Native			Native	SCI	PCH_GPP_G8	Testpoint
	R43	GPP_G9/FAN_PWM_1	Native			Native	SCI	PCH_GPP_G9	Testpoint
	U39	GPP_G10/FAN_PWM_2	Native			Native	SCI	PCH_GPP_G10	Testpoint
GPP_H	N42	GPP_G11/FAN_PWM_3	Native			Native	SCI	PCH_GPP_G11	Testpoint
	R39	GPP_G12/GSXDOUT	Primary(3.3V/1.8V)			GPI	SCI		
	R36	GPP_G13/GSXSLOAD	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G13	Testpoint
	R42	GPP_G14/GSXDIN	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G14	Testpoint
	R41	GPP_G15/GSXRESET#	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G15	
	P43	GPP_G16/GSXCLK	Primary(3.3V/1.8V)			GPI	SCI		
	N44	GPP_G17/ADR_COMPLETE	Primary(3.3V/1.8V)			GPI	SCI	GPP_G17	Testpoint
	N43	GPP_G18/NMI#	Primary(3.3V/1.8V)			GPI	SCI	NMI#	Testpoint
	M45	GPP_G19/SMI#	Primary(3.3V/1.8V)			GPI	SCI	EC_SMI#	
	R35	GPP_G20	Primary(3.3V/1.8V)			GPI	SCI		
	U35	GPP_G21	Primary(3.3V/1.8V)			GPI	SCI	SUS_32CAM_EN	
	L44	GPP_G22	Primary(3.3V/1.105V)			GPI	SCI		
	L43	GPP_G23	Primary(3.3V/1.11V)			GPI	SCI		
GPP_I	AT33	GPP_H0/SRCCLKREQ6#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#6	PU 10K to +3VS_S0
	AR31	GPP_H1/SRCCLKREQ7#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#7	PU 10K to +3VS_S0
	BD32	GPP_H2/SRCCLKREQ8#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#8	PU 10K to +3VS_S0
	BC32	GPP_H3/SRCCLKREQ9#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#9	PU 10K to +3VS_S0
	BB31	GPP_H4/SRCCLKREQ10#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#10	PU 10K to +3VS_S0
	BC33	GPP_H5/SRCCLKREQ11#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#11	PU 10K to +3VS_S0
	BA33	GPP_H6/SRCCLKREQ12#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#12	PU 10K to +3VS_S0
	AW33	GPP_H7/SRCCLKREQ13#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#13	PU 10K to +3VS_S0
	BB33	GPP_H8/SRCCLKREQ14#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#14	PU 10K to +3VS_S0
	BD33	GPP_H9/SRCCLKREQ15#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#15	PU 10K to +3VS_S0
	BD34	GPP_H10/SML2CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML2CLK2	Testpoint
	AW35	GPP_H11/SML2DATA	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML2DAT42	Testpoint
	BD35	GPP_H12/SML2ALERT#	Primary(3.3V/1.8V)	L(20K)		GPO	SCI	SMLALERT0#	Testpoint L(20K)
	BC35	GPP_H13/SML3CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML3CLK3	Testpoint
	BA35	GPP_H14/SML3DATA	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML3DAT43	Testpoint
	BB36	GPP_H15/SML3ALERT#	Primary(3.3V/1.8V)			GPI	SCI	SMLALERT0#	Testpoint
	BD39	GPP_H16/SML4CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML4CLK4	Testpoint
	BE34	GPP_H17/SML4DATA	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML4DAT44	Testpoint
	BC36	GPP_H18/SML4ALERT#	Primary(3.3V/1.8V)			GPI	SCI	SMLALERT0#4	Testpoint
	BB38	GPP_H19/ISH_I2C0_SDA	Primary(3.3V/1.8V)			GPI	SCI	ISH_I2C_0_SDA	Testpoint
	BC38	GPP_H20/ISH_I2C0_SCL	Primary(3.3V/1.8V)			GPI	SCI	ISH_I2C_0_SCL	Testpoint
	BE39	GPP_H21/ISH_I2C1_SDA	Primary(3.3V/1.9V)			GPI	SCI	ISH_I2C1_SCL	Testpoint
	BD38	GPP_H22/ISH_I2C1_SCL	Primary(3.3V/1.105V)			GPI	SCI	ISH_I2C1_SDA	Testpoint
	BD36	GPP_H23	Primary(3.3V/1.11V)			GPI	SCI	3DCAM_PW	
GPP_J	AW4	GPP_J0/DDPB_HPD0	Primary(3.3V/1.8V)			GPI	SCI	PCH_HDMIOUT_HPD	PU 1M to +3VS_S0
	AY2	GPP_J1/DDPC_HPD1	Primary(3.3V/1.8V)			GPI	SCI	DDPC_HPD	Testpoint
	AU4	GPP_J2/DDPD_HPD2	Primary(3.3V/1.8V)			GPI	SCI	DDPD_HPD	Testpoint
	BA4	GPP_J3/DDPE_HPD3	Primary(3.3V/1.8V)			GPI	SCI	EC_SCI#	
	BD7	GPP_J4/EDP_HPD	Primary(3.3V/1.8V)			GPI	SCI	EDP_HPD_R	PD 100K
	BA5	GPP_J5/DDPB_CTRLCLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_HDMIOUT_CLK	PU 2.2K to +3VS_S0
	BC4	GPP_J6/DDPB_CTRLDATA	Primary(3.3V/1.8V)	L(20K)		GPO	SCI	PCH_HDMIOUT_DATA	PU 2.2K to +3VS_S0 L(20K)
	BB3	GPP_J7/DDPC_CTRLCLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_DPC_CLK	PU 2.2K to +3VS_S0

Security Classification	Compal Secret Data		
Issued Date	2017/08/10	Deciphered Date	2018/09/10

Compal Electronics, Inc.

Title: **GPIO Table & SMBUS BD**

Size: | Document Number: **LA-F882P M/B** | Rev: 0.2

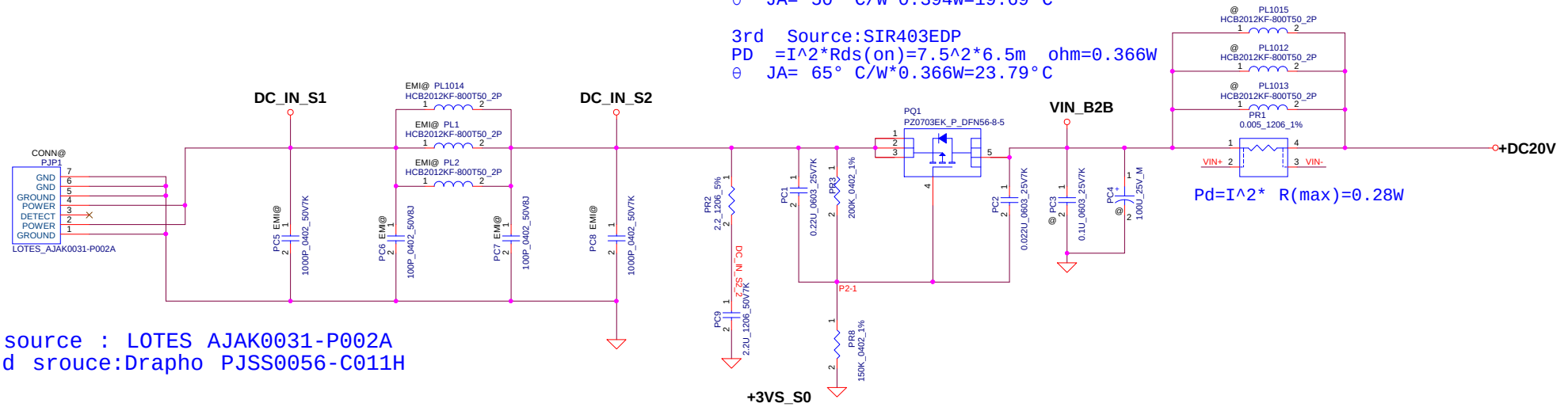
Date: Monday, April 09, 2018 | Sheet 47 of 66

Main source:PZ0703EK
PD =I^2*Rds(on)=7.5^2*7m ohm=0.394W
θ JA= 50° C/W*0.394W=19.69°C

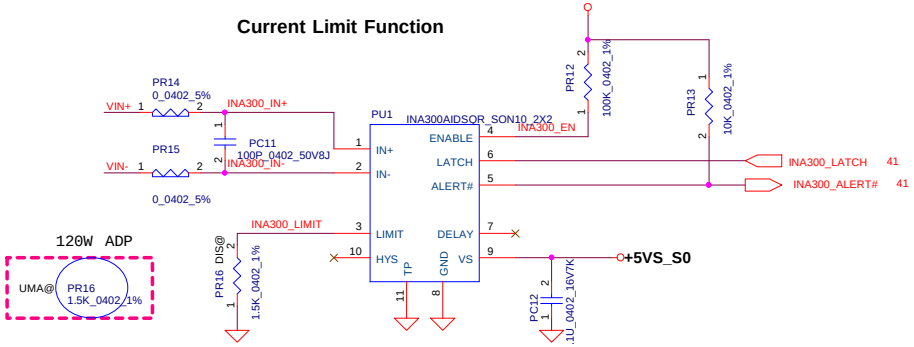
Second source:AON6405
PD =I^2*Rds(on)=7.5^2*7m ohm=0.394W
θ JA= 50° C/W*0.394W=19.69°C

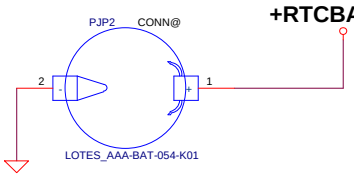
3rd Source:SIR403EDP
PD =I^2*Rds(on)=7.5^2*6.5m ohm=0.366W
θ JA= 65° C/W*0.366W=23.79°C

BOM Control



main source : LOTES AJAK0031-P002A
second srouce:Drapho PJSS0056-C011H





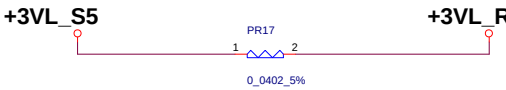
RTC BATT CONNECTER

UMA SKU 120W:
Full Load(100%) --> 6A
Vtrip=6*5m=30mV
VLimit=Vtrip; Rlimit=(30mV+0.5mV)/20uA= 1.525K

Trigger(112.5%) --> 6.75A (@135W)
Vtrip=6.75*5m=33.75mV
Rlimit=(33.75mV+0.5mV)/20uA=1.7125K
Select Rlimit=1.5K
I_Trigger-->6.75A

DIS SKU 150W:
Full Load(100%) --> 7.5A
Vtrip=7.5*5m=37.5mV
VLimit=Vtrip; Rlimit=(37.5mV+0.5mV)/20uA= 1.9K

Trigger(120%) --> 9A (@180W)
Vtrip=9*5m=45mV
Rlimit=(45mV+0.5mV)/20uA=2.275K
Select Rlimit=2K
I_Trigger-->9A



Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: ***DCIN/CONN***

Size	Document Number	Rev
Custom		0.1

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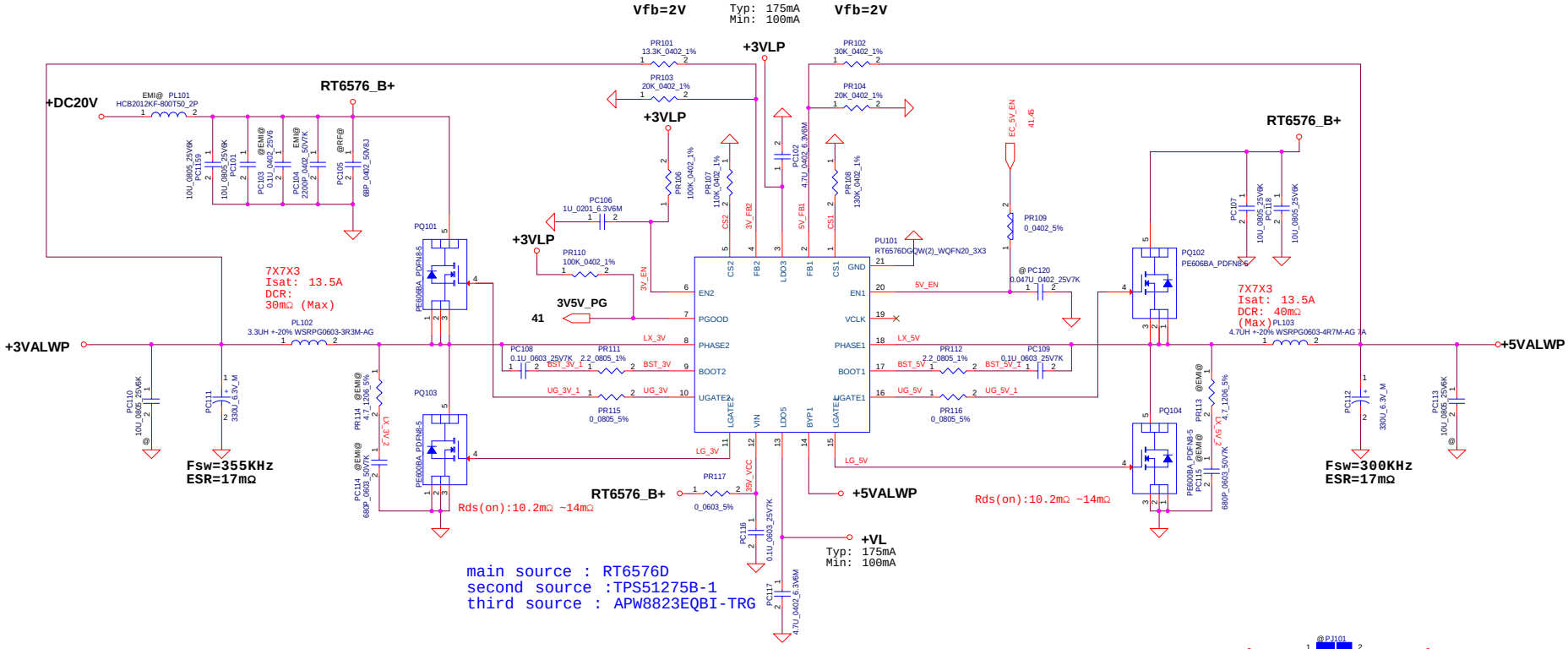



```
+3VALWP
Vin = 20V
Iin  =3.3*6.8/0.85/20
     = 1.32A
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      = 2*[1+(13.3K/20K)]
      = 3.3V
```

```
+3VALWP
Imax=4.48A  ;  Ipeak=6.8A  ;Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds  :  L/S  -->  typ:10.2mohm  ;  max:  14mohm
Itrip=9~11  uA
Iocp(set)=10A~13.5A
Iin_ripple=1.66A
Output  Cap.  ESR=17mohm
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.352A
LIR=Delta  IL/Ipeak=0.367
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=240.02uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.87uF
```

```
+5VALWP
Vin = 20V
Iin  =5*8.44/0.85/20
     = 2.48A
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      = 2*[1+(30K/20K)]
      =5V
```

```
+5VALWP
Imax=5.9A,Ipeak=8.44A   ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds  :  L/S  -->  typ:10.2ohm  ;  max:  14mohm
Itrip=9~11  uA
Iocp(set)=12.66A~13.5A
Iin_ripple=2.56A
Output  Cap.  ESR=17mohm
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.660A
LIR=Delta  IL/Ipeak=0.315
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=243.73uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.85uF
```

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/15	Deciphered Date	2013/08/29

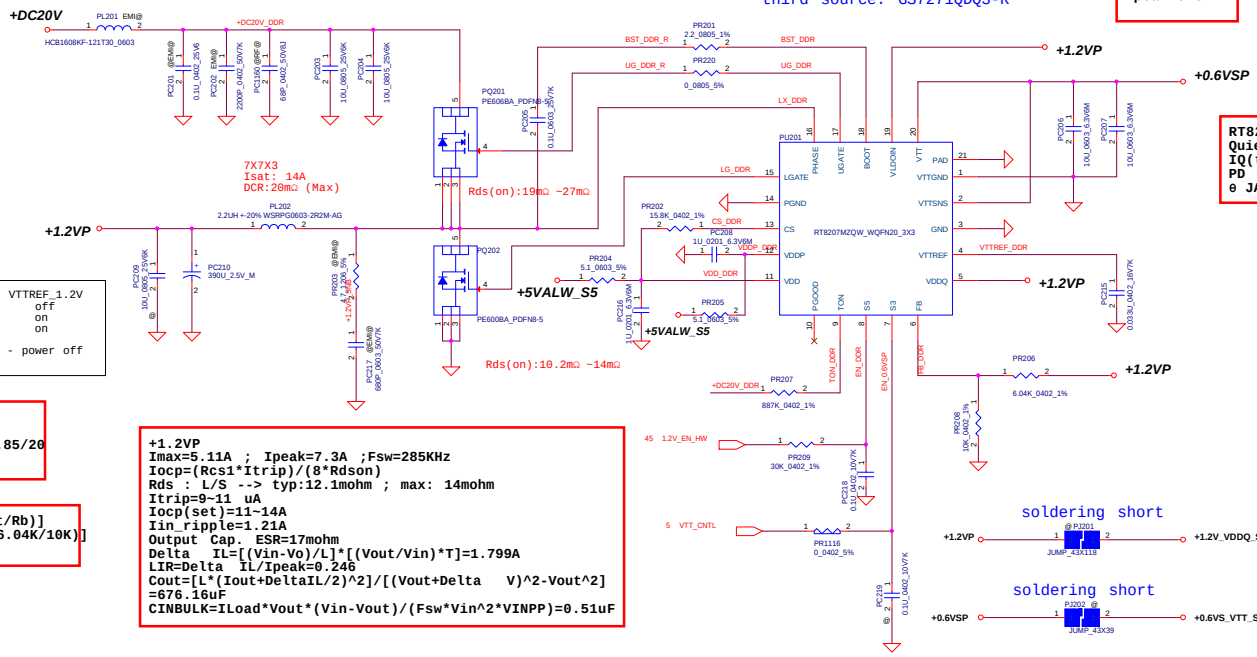
Title	3V/5V (RT6576D)		
Size C	Document Number		Rev 0.1
Date: Monday, April 09, 2018		Sheet 49 of 66	

main source : RT8207MZQW
second srouce:UP1566PQKF
third source: GS7271QDQ3-R

+0.6VSP
TDC=0.42A
Ipeak=0.6A

Vo	0.6	
Vin	1.2	
Io	0.75	
PD	0.455	
θ JA(main)	52	° C/W
θ JA(2nd)	68	

RT8207M:
Quiescent Current (GND Current)
IQ(typ)=0.47mA,IQ(max)=1mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.455W
θ JA= 33.7° C/W*0.903=23.66°C



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.2VP
Vin = 20V
Iin = 7.3*1.2/0.85/20
= 0.51A

Vout = Vfb*[1+(Rt/Rb)]
= 0.75*[1+(6.04K/10K)]
= 1.203V

+1.2VP
Imax=5.11A ; Ipeak=7.3A ;Fsw=285KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:12.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11~14A
Iin_ripple=1.21A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.799A
LIR=Delta IL/Ipeak=0.246
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=676.16uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.51uF

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

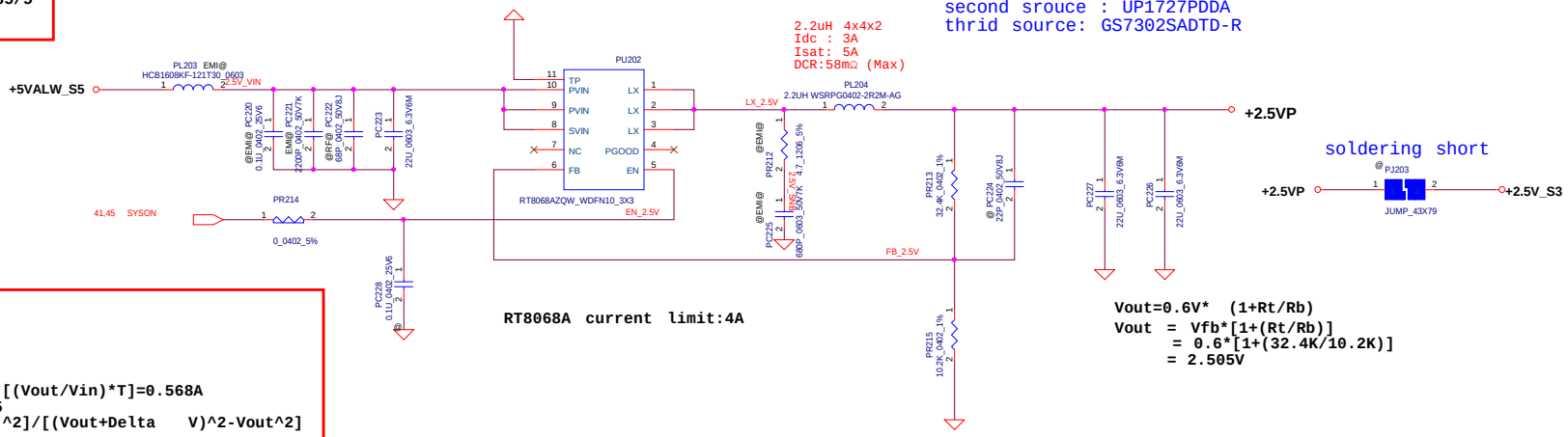
Compal Electronics, Inc.

Title: 1.2VP/0.6VSP(RT8207M)

Size	Document Number	Rev
Custom		0.1

Date: Monday, April 09, 2018 Sheet 50 of 66

+2.5VP
Vin =5V
Iin = 2.5*2.24/0.85/5
=1.32A



+2.5VP
Ipeak=2.24A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.75A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta IL/Ipeak=0.25
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.78uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/15	Deciphered Date	2013/08/29

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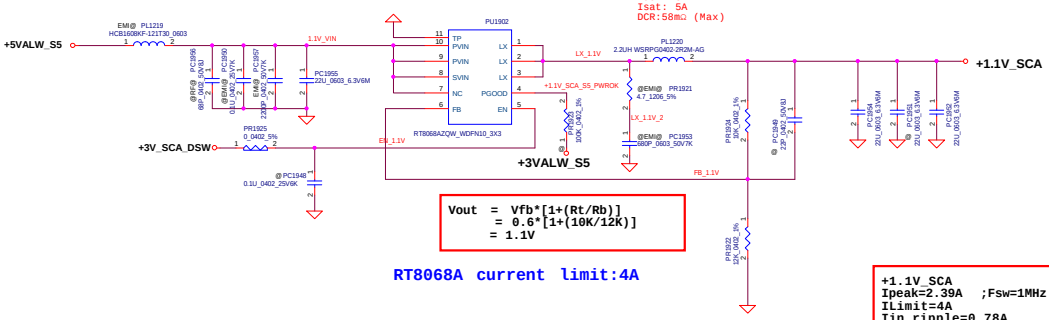
Title: 2.5VP(RT8068)
Size: C | Document Number | Rev: 0.1
Date: Monday, April 09, 2018 | Sheet 51 of 66

+1.1V_SCA
Vin =5V
Iin =1.1*1.94/0.9/5
=0.58A

main source : RT8068AZQW
second srouce : UP1727PDDA
thrid source: GS7302SADTD-R

2.2uH 4x4x2
Idc : 3A
Isat: 5A
DCR:58mΩ (Max)



Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(10K/12K)]
= 1.1V

RT8068A current limit:4A

+1.1V_SCA ——— @PJ902 JUMP_43X79 ——— +1.1V_SCA_S5

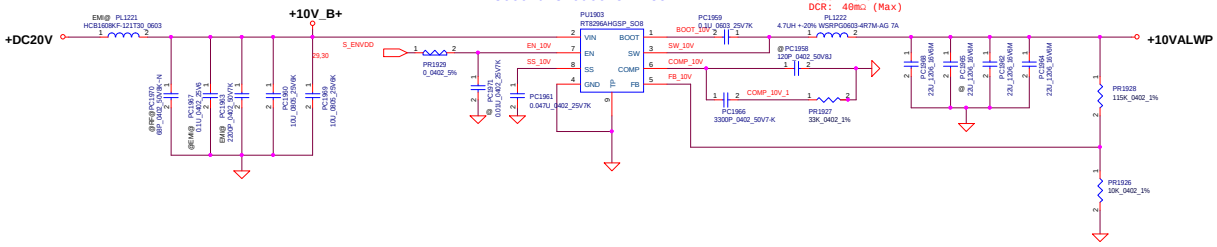
soldering short

+1.1V_SCA
Ipeak=2.39A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.78A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.39A
LIR=Delta IL/Ipeak=0.163
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=77.75uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

+10VALWP
Vin =20V
Iin = 10*1.04/0.85/20
=0.61A

main source : RT8296A
second srouce:UP1735P

7X7X3
Isat: 13.5A
DCR: 40mΩ (Max)



Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(115K/10K)]
= 10V

+10VALWP ——— @PJ906 JUMP_43X79 ——— +10V_LCDVDD_S5

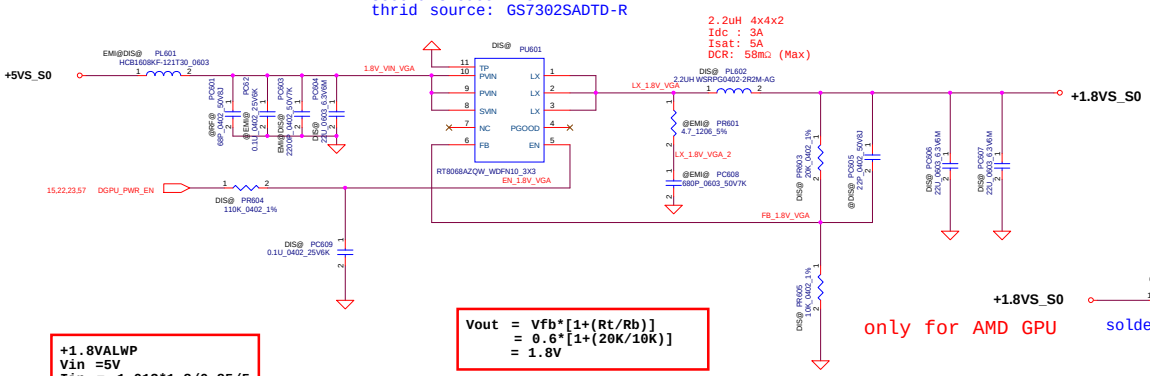
Soldering Short

+10VALWP
Imax=0.73A,Ipeak=1.04A ; Fsw=340KHz
Current Limit=4.1A(Min)
in_ripple=0.78A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.12A
LIR=Delta IL/Ipeak=3
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=6.11uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.27uF

Security Classification	Compal Secret Data		
Issued Date	2013/08/15	Deciphered Date	<Deciphered_Date>

Title	1V1(RT8068)/10V(RT8296)	
Size: Custom	Document Number	Rev 0.1
Date: Monday, April 08, 2019	Sheet 52 of 66	

main source : RT8068AZQW
second srouce : UP1727PDDA
thrid source: GS7302SADTD-R

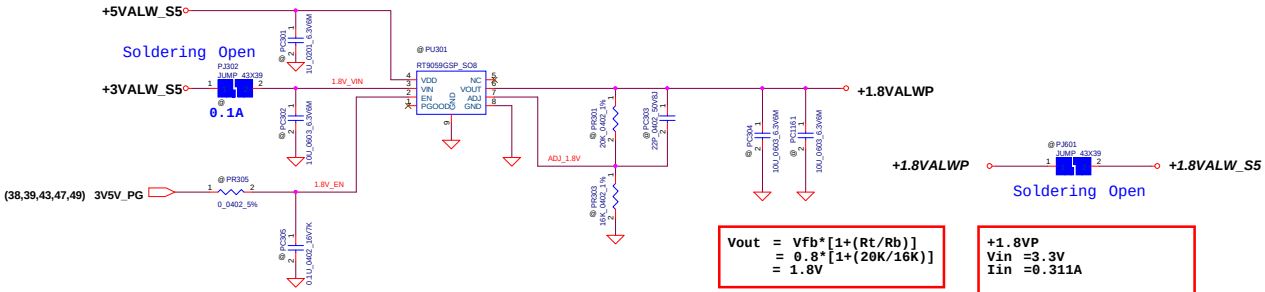



```
+1.8VALWP
Vin =5V
Iin = 1.013*1.8/0.85/5
    =0.429A
```

```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.6*[1+(20K/10K)]
     = 1.8V
```

```
+1.8VALWP
Ipeak=1.013A  ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.4A
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.745A
LIR=Delta  IL/Ipeak=0.372
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta   V)^2-Vout^2]
=20.81uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.06uF
```

main source : RT9059GSP
second souce: APL5933CKAI
third source : GS7166




```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.8*[1+(20K/16K)]
     = 1.8V
```

```
+1.8VP
Vin =3.3V
Iin =0.311A
```

Vo	1.8	V
Vin	3.3	V
Io	0.65	A
PD	0.456	W
θ JA(main) θ JA(2nd)	33.7 50	° C/W

```
+1.8VS
Ipeak=0.311A  ;
Current   Limit=3.1A(min)~3.6A(Typ)~4.2A(Max)

RT9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA,IQ(max)=1.2mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.978W
θ JA= 33.7° C/W*0.903=32.99°C
```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Title: 1.8V(RT8068/RT9059)

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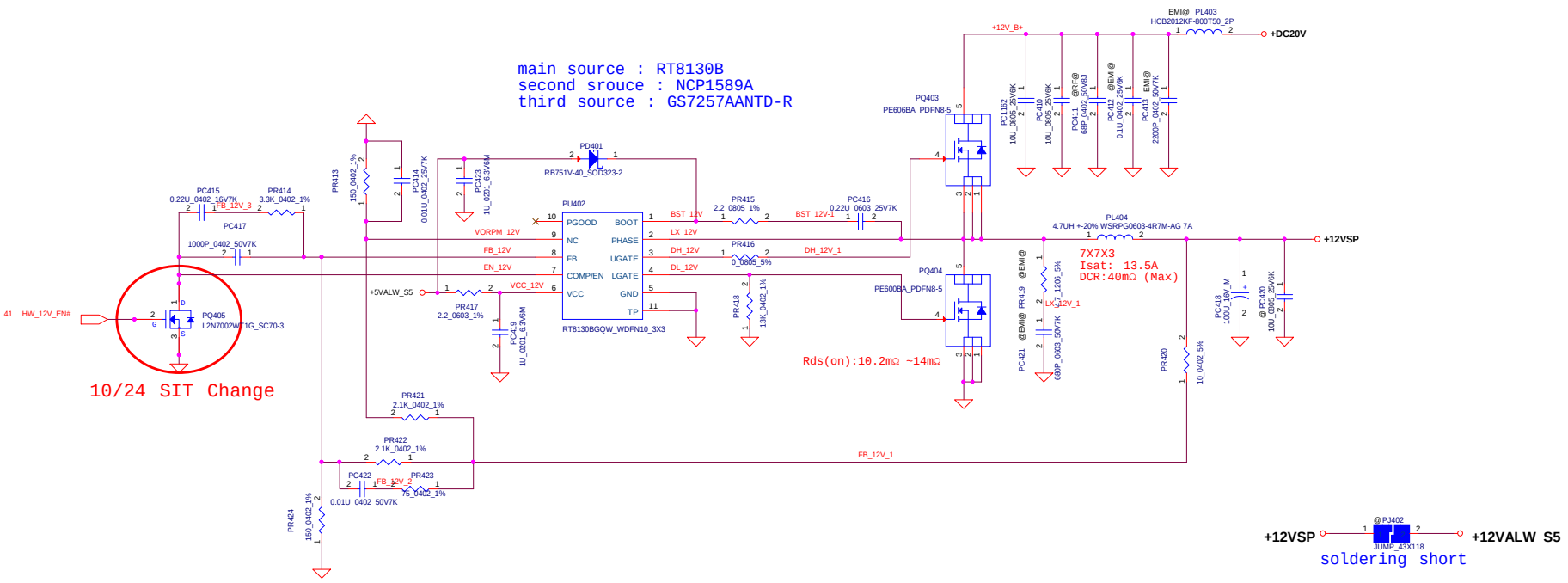


+12VSP
Imax=2.607,Ipeak=3.724A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:12.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10~13.5A
Iin_ripple=0.97A
Output Cap. ESR=24mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.404A
LIR=Delta IL/Ipeak=0.914
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =15uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.04uF

Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(2.1K/150)]
= 12V

+12VSP
Vin = 20V
Iin = 12*2.1/0.85/20
= 2.63A

Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: 12V(RT8130B)

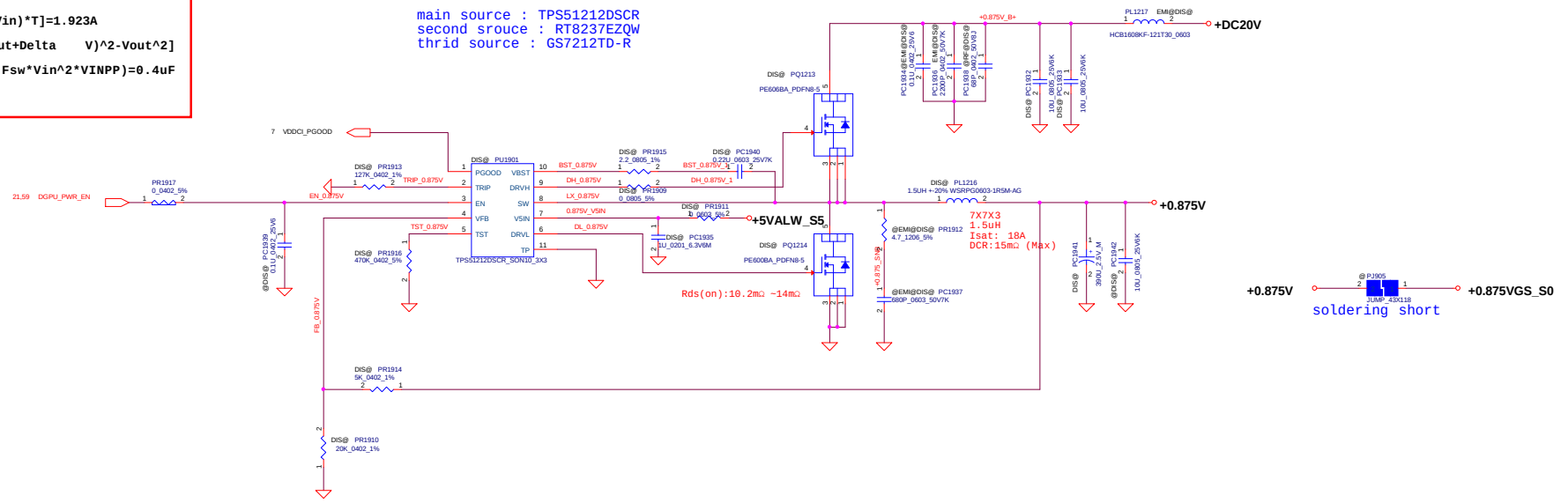
Size	Document Number	Rev
C		0.1

Date: Monday, April 09, 2018 Sheet 54 of 66

+0.875V
Imax=5.6,Ipeak=8A ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=12~16A
Iin_ripple=1.15A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.923A
LIR=Delta IL/Ipeak=0.24
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=822.98uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.4uF

+0.875V
Vin = 20V
Iin = 8*0.875/0.85/20
= 0.412A

main source : TPS51212DSCR
second srouce : RT8237EZQW
thrid source : GS7212TD-R



Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(5K/20K)]
= 0.875V

Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: 0.875V(TPS51212)

Size	Document Number	Rev
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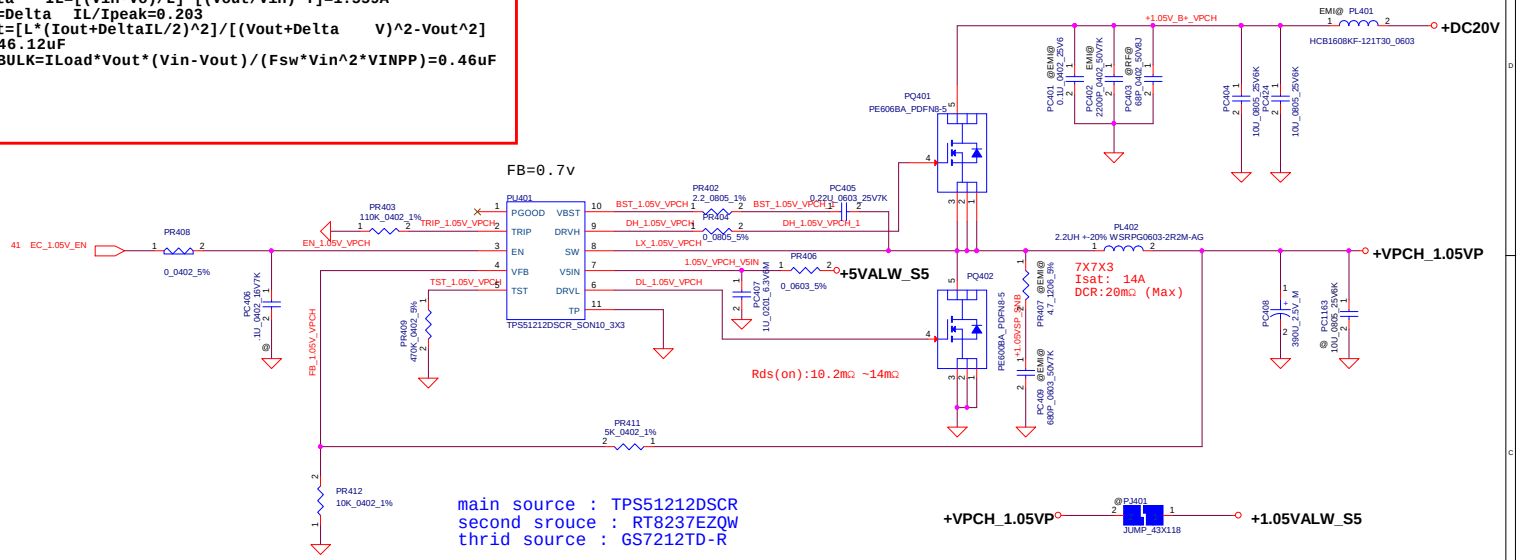
```
+VPCH_1.05VP
Ipeak=7.696A,Imax=5.387A  ;  Iocp=11.6A~14A
Fsw=290K
Iin_ripple=  1.28A
Output  Cap.  ESR=17mohm
Rds   L/S --> typ: 12.1mohm ; max: 14mohm
Delta    IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.559A
LIR=Delta   IL/Ipeak=0.203
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=1246.12uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.46uF
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      = 0.7*[1+(5K/10K)]
      = 1.05V
```

```
+VPCH_1.05VP
Vin  = 20V
Iin  =  1.0*10.24/0.85/20
     = 0.602A
```



Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: VPCH1.05V(TPS51212)

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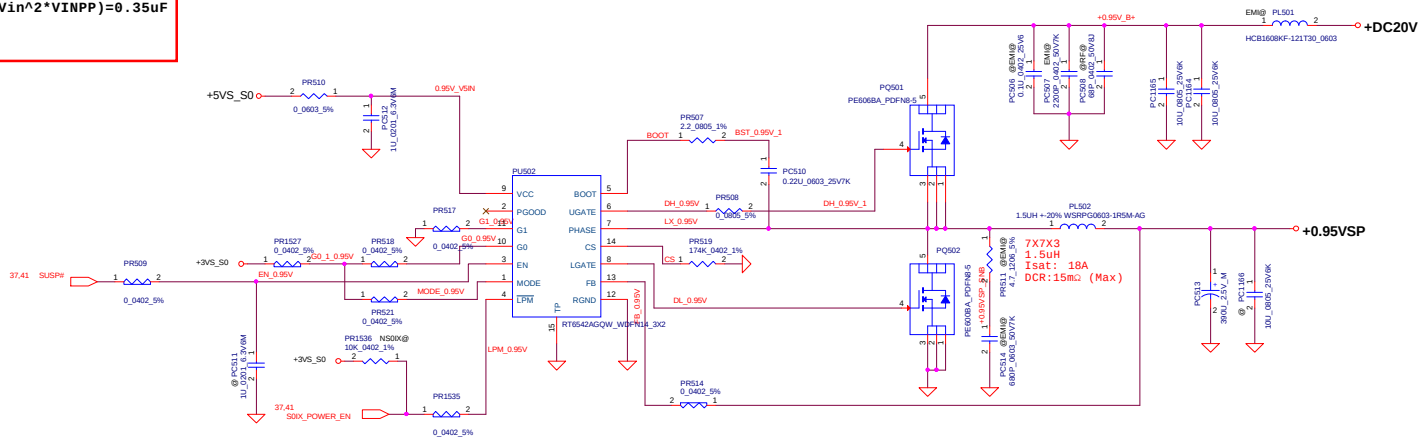
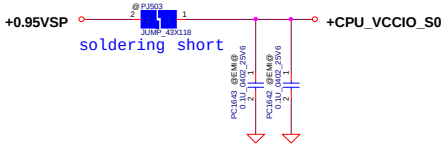
```
+0.95VSP
Imax=4.48,Ipeak=6.4A   ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.3~13.6A
Iin_ripple=0.95A
Output Cap. ESR=17mohm
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.08A
LIR=Delta  IL/Ipeak=0.325
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=831.61uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.35uF
```

```
+0.95VSP
Vin = 20V
Iin  =  6.4*0.95/0.85/20
     = 0.357A
```



NS0IX@ for non-morden standby



Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: **VCCIO_0.95V(RT6542AGQW))**

Size	Document Number	Rev
Custom		0.1

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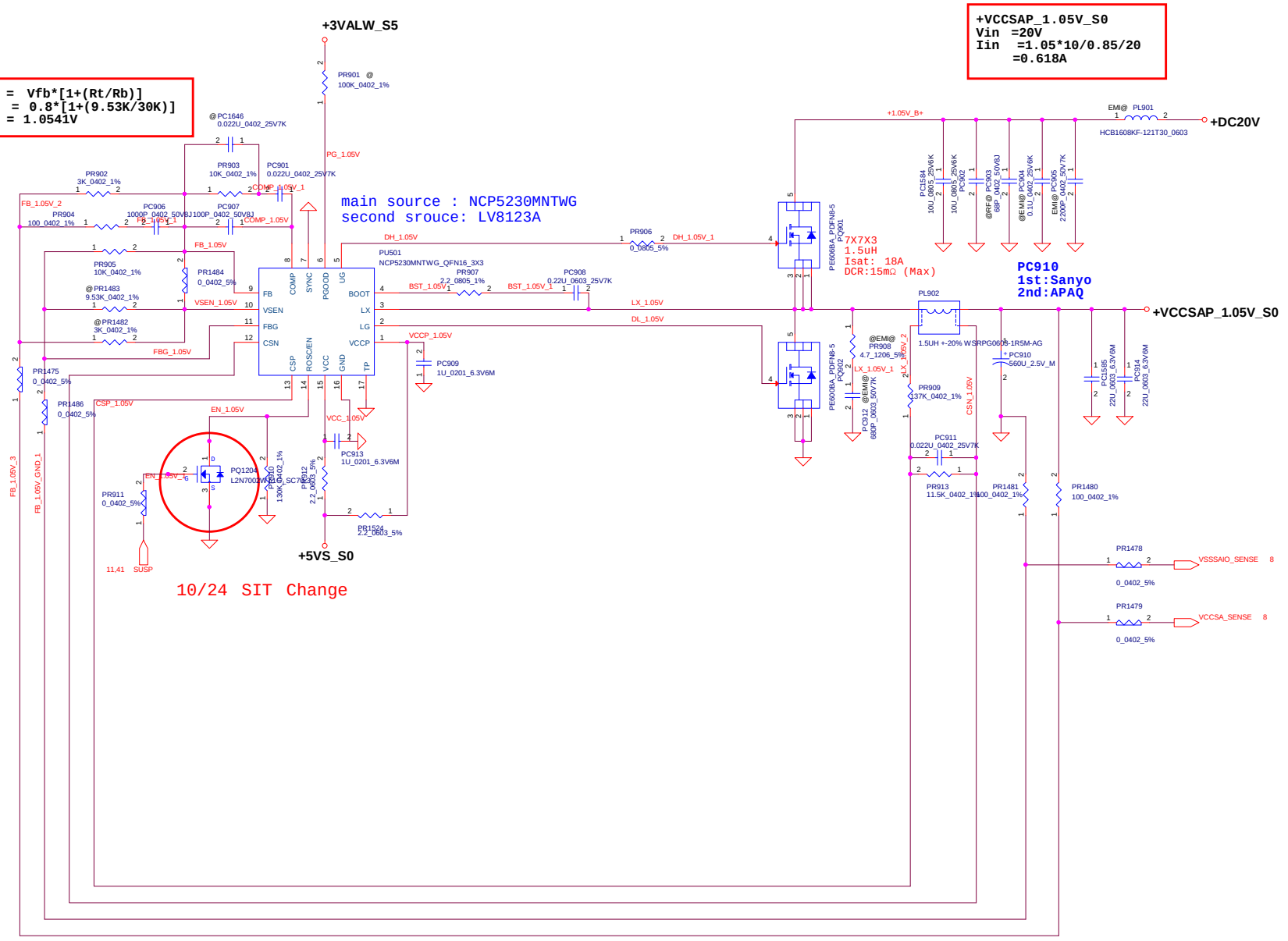

Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(9.53K/30K)]
= 1.0541V

+VCCSAP_1.05V_S0
Vin =20V
Iin =1.05*10/0.85/20
=0.618A

+1.05VSP
Imax=7.826A,Ipeak=11.18A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:11mohm ; max: 17.5mohm

Iocp(set):~17.2A
Iin_ripple=1.72A
Output Cap. ESR=9mohm
Delta Il=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.21A
LIR=Delta Il/Ipeak=0.201
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1029.17uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.64uF

Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: VCCSA_1.05VSP(NCP5230M)

Size: Custom | Document Number | Rev: 1.0

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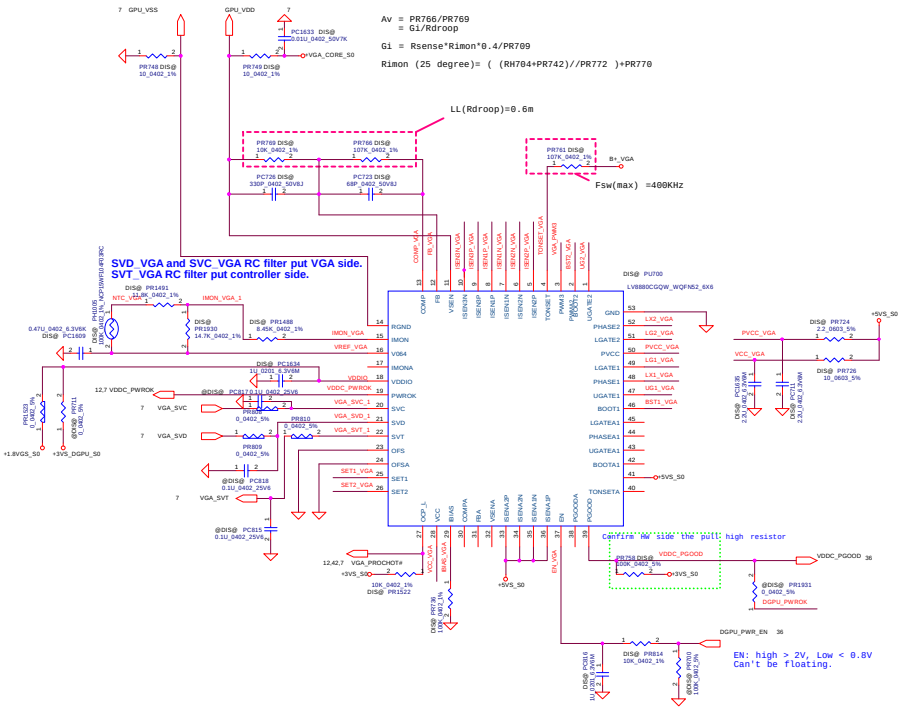
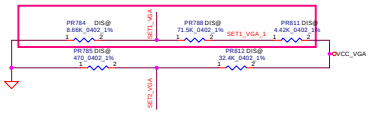
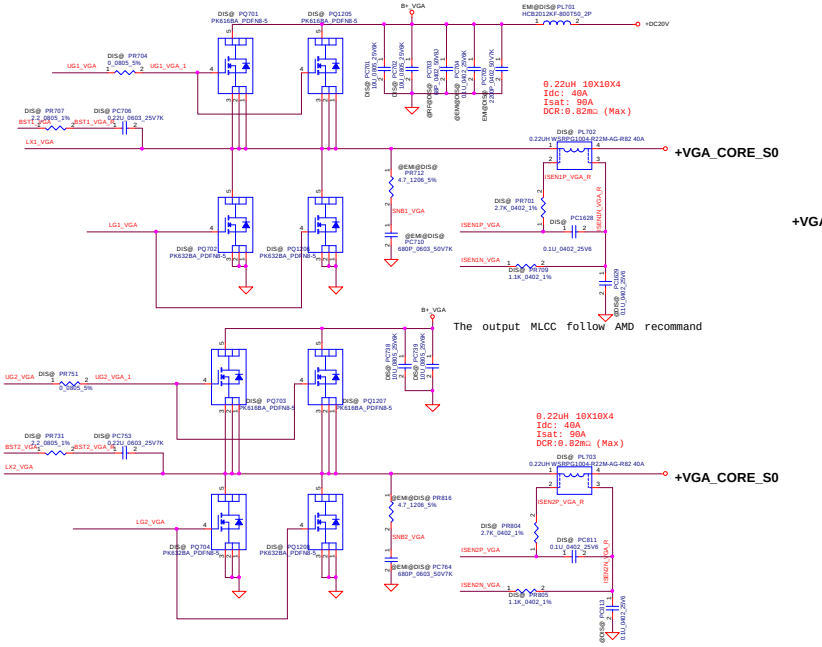
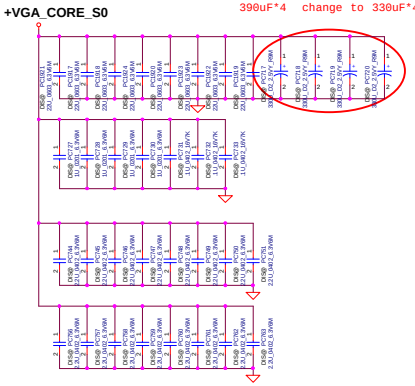




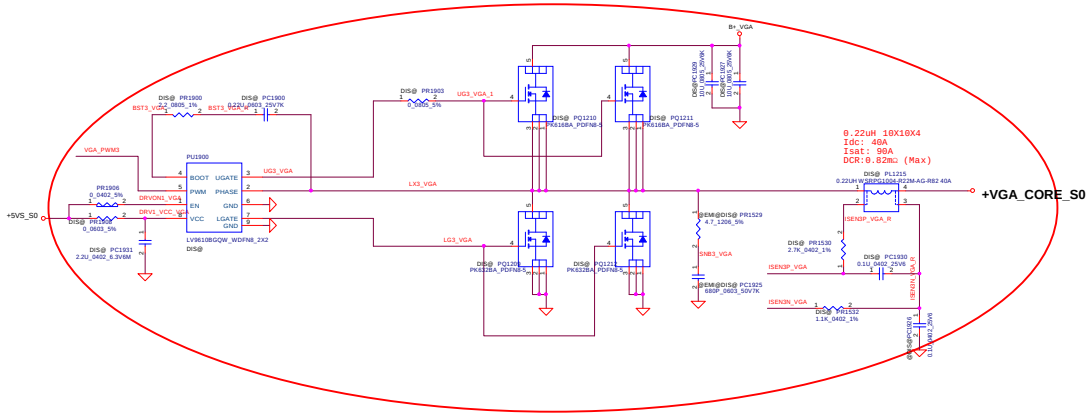
+VGA_CORE [AMD R17M-P1-70]
TDC=45A ; Ipeak=92A ; Iocp>=120A
Fsw=400K
Inductor DCR=1mohm
Output Cap. ESR=9mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=8.727A
LIR=Delta IL/Ipeak=0.388
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1356.75uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.76uF

+VGA_CORE
Vin = 20V
Iin = 45*1/0.8/20
= 2.8125A





VGA_CORE
330uF*4 + 22uF*8 + 1uF*7 + 2.2uF*16
1538.2uF



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Issued Date	2013/08/29	Deciphered Date	2013/08/29
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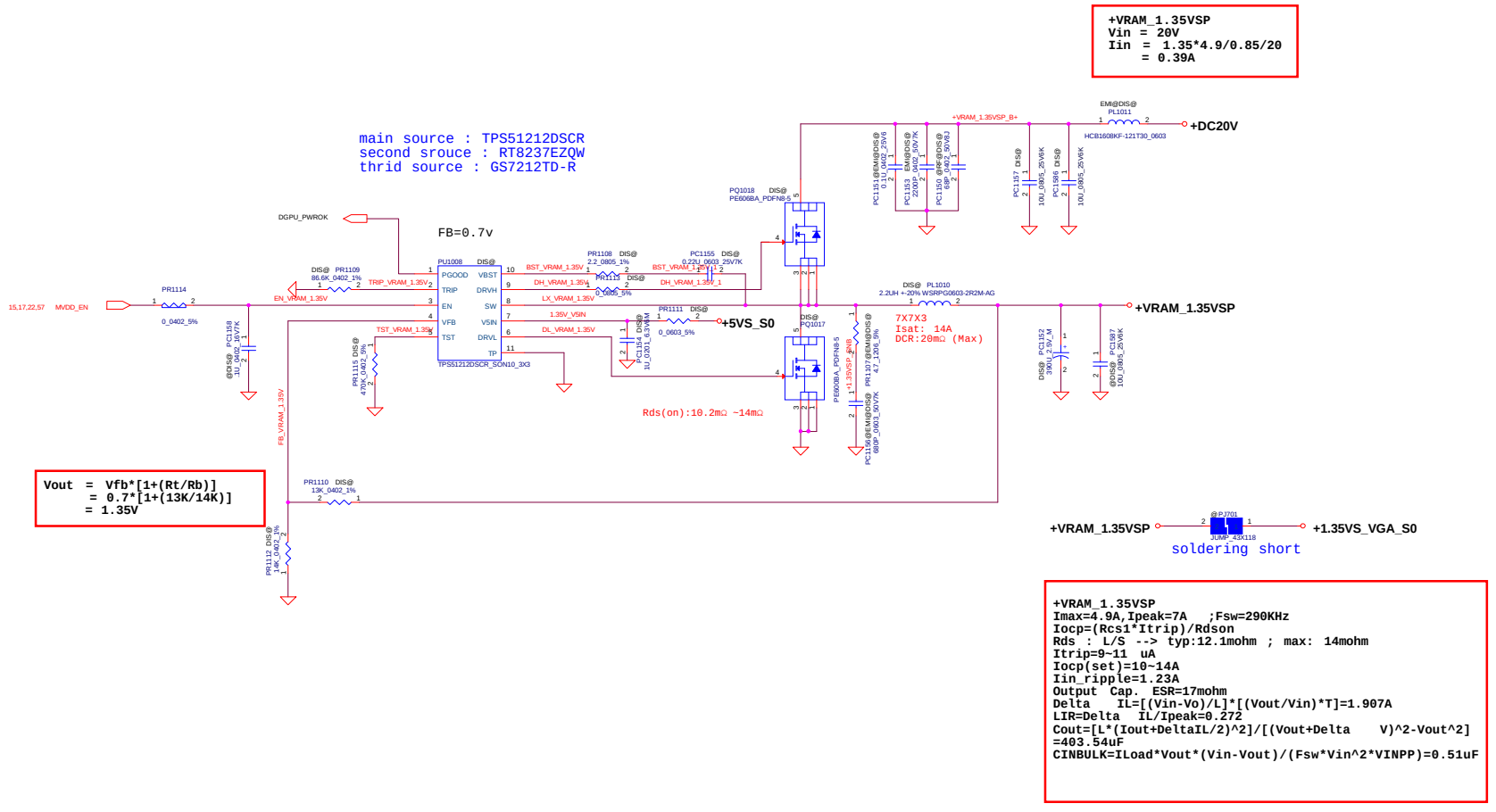
			Size: Document Number: Rev: 0.1
			Date: Monday, April 09, 2018 Sheet 59 of 66



Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: ***VRAM_1.35V(TPS51212)***

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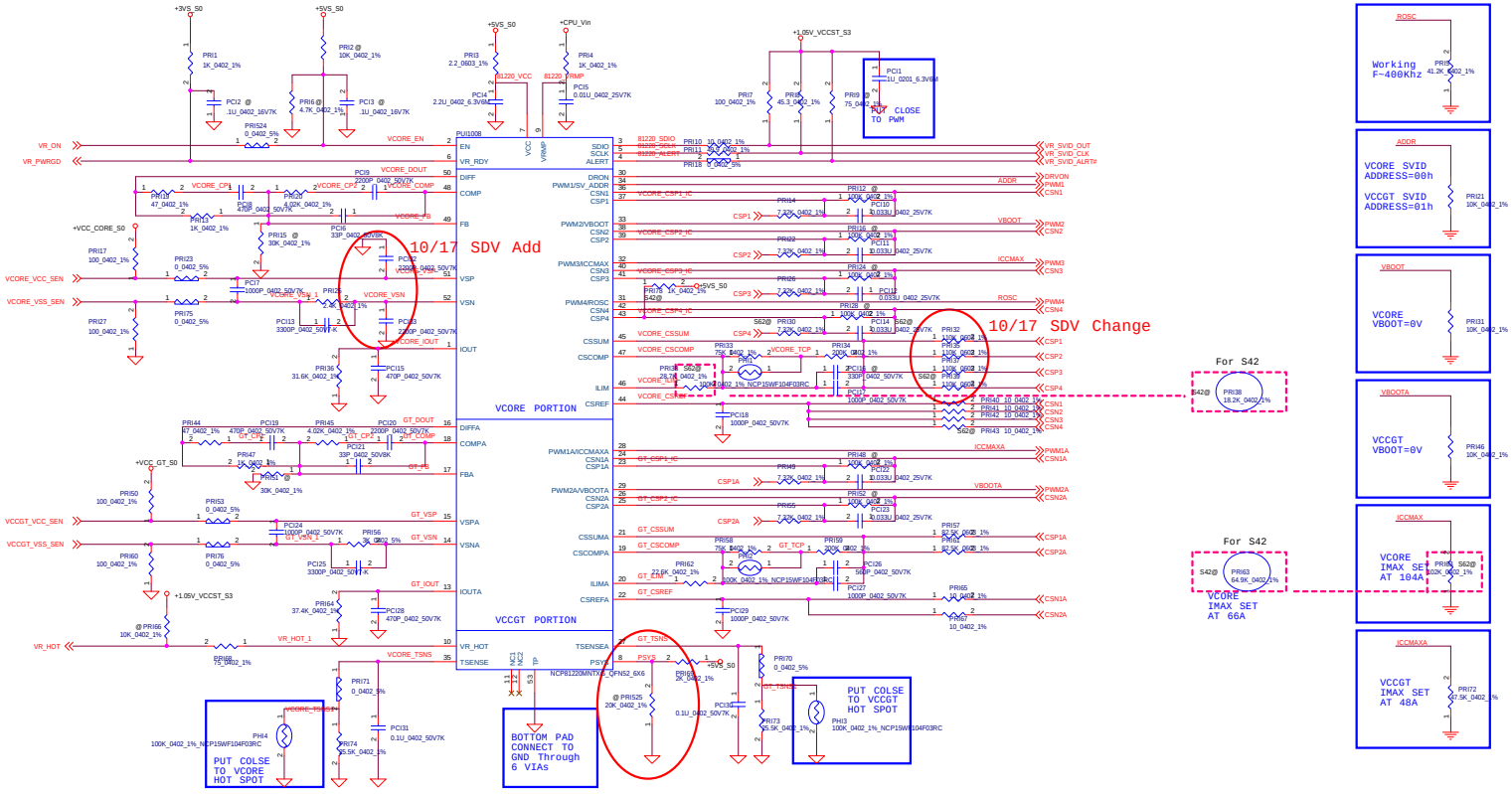
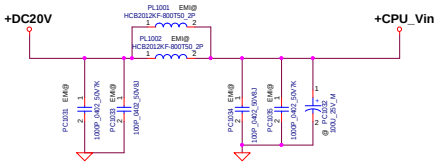
Intel Coffeelake IMVP8 POWER CFL - S-LINE 62 / 42 / 22 35W 4+2 PHASE





CFL - S-LINE 62 / 42 / 22 35W

+CPU_CORE
TDC=74A,Ipeak=104A Fsw=400K,OCP=135~176.8A
Inductor DCR=0.98mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.255A
LIR=Delta IL/Ipeak=0.394
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =811.08
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.03uF

+GFX_CORE
TDC=34A,Ipeak=48A Fsw=400K,OCP=62.4~81.6A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=6.267A
LIR=Delta IL/Ipeak=0.358
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =577.19uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

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Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Title: **CPU_CORE (NCP81220M)**

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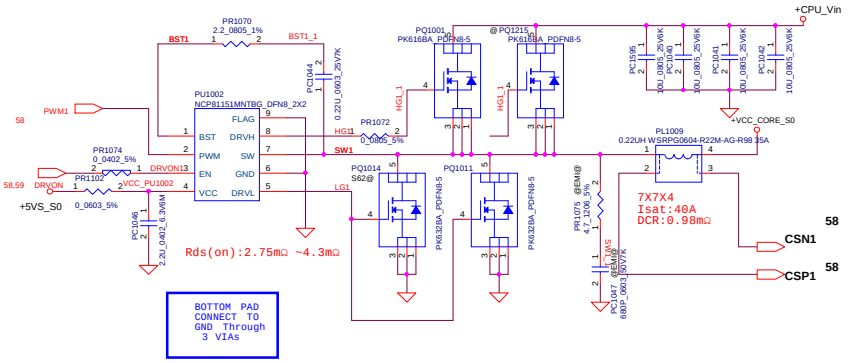

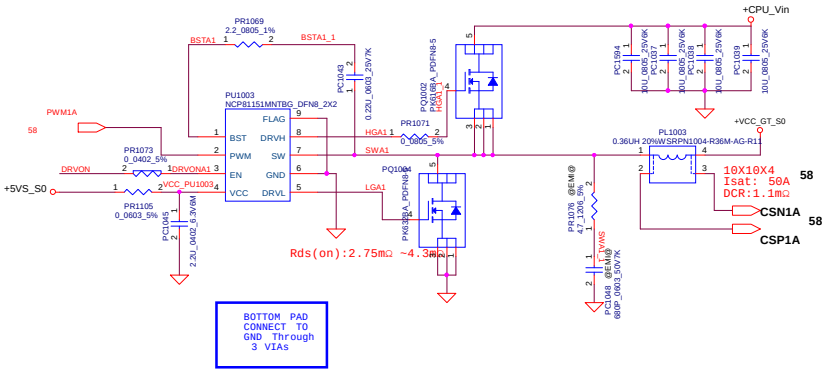

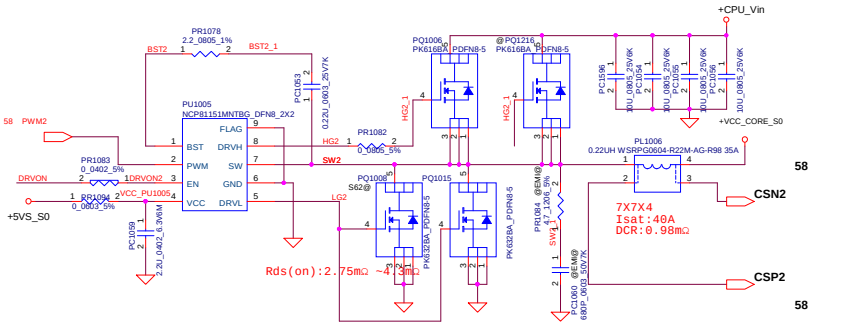

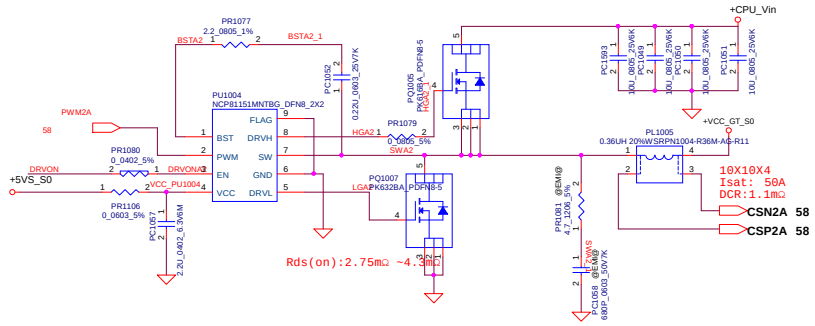

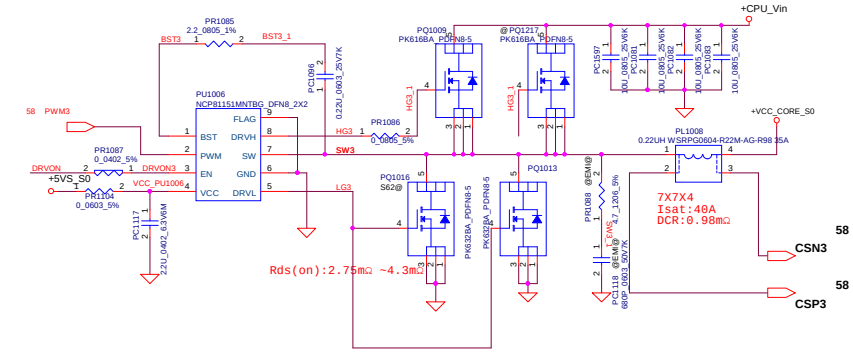

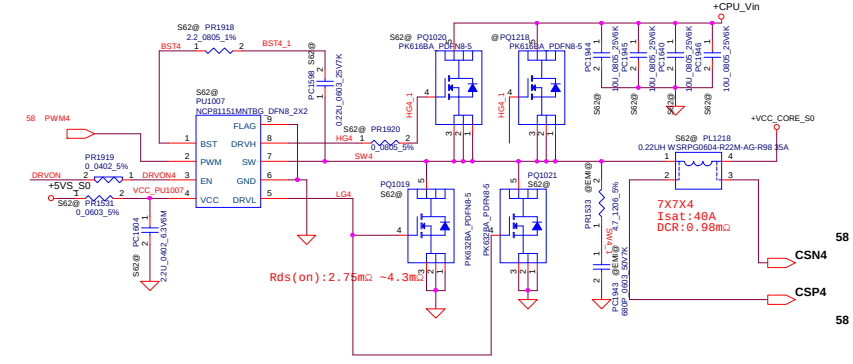

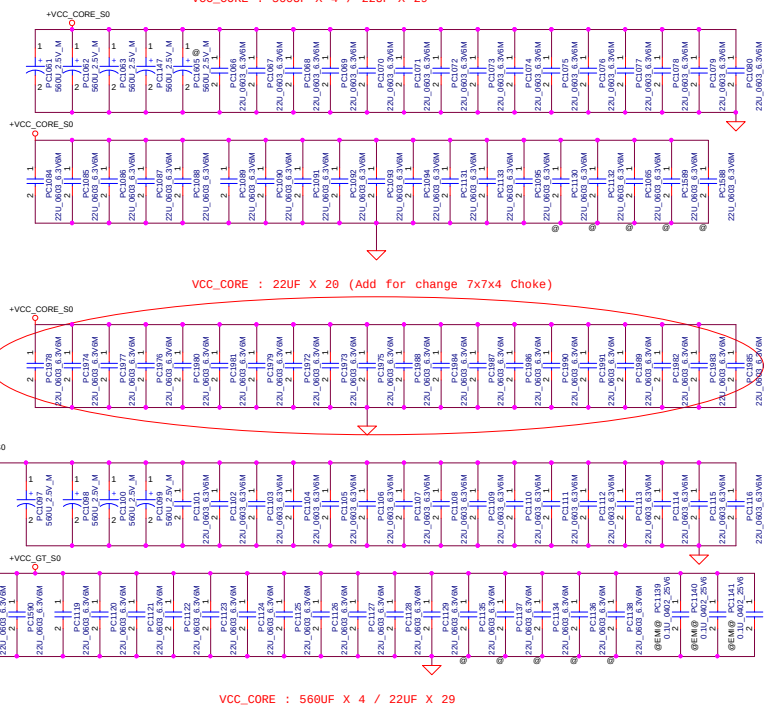

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Title: CPU_CORE 1

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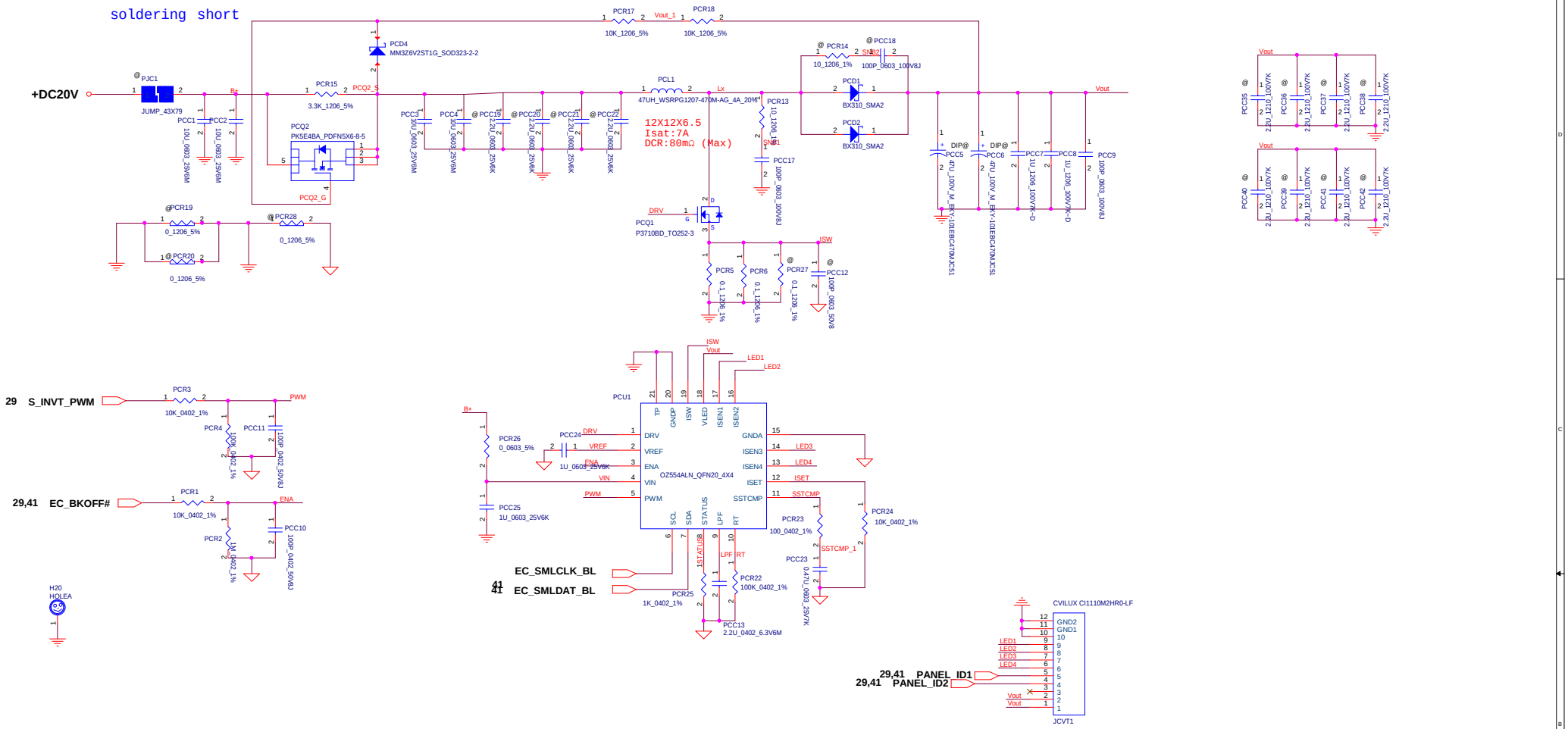

Security Classification	Compal Secret Data		
Issued Date	2015/11/30	Deciphered Date	2015/11/30

Compal Electronics, Inc.

Title: CONVERTER/B

Size	Document Number	Rev
C	C7 Converter/B	0.2

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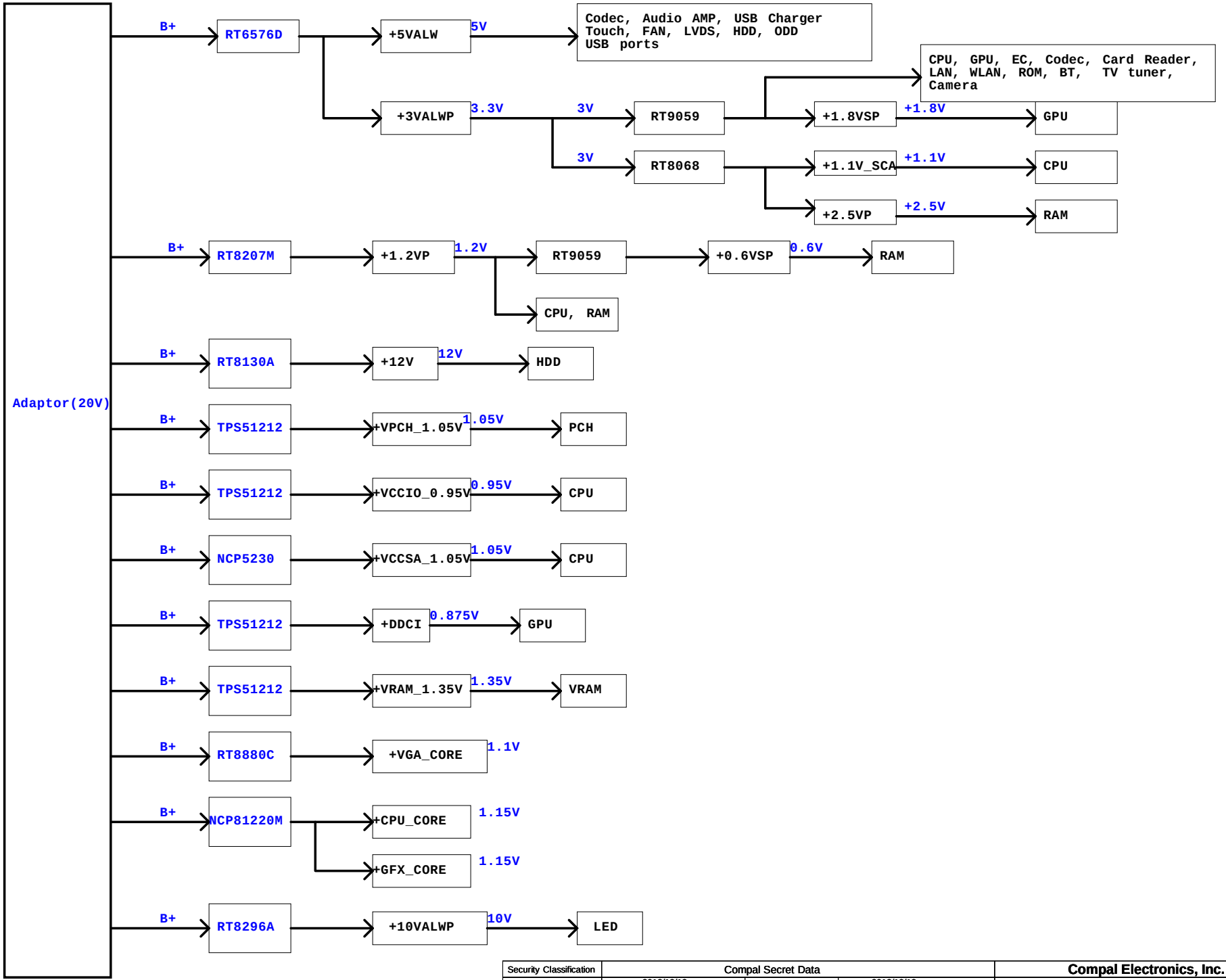

Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: ***Power Rail***

Size	Document Number	Rev
Custom		0.1

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