C550 ICL Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DY	***DUMMY, NOT ASM***
DDP/ SDP	***Memory down BOM Control***
DDR4_CTRL	***Memory down BOM Control***
MEM_IDx_x	***Memory ID for SW Team (BOM Control)***
PCB_ID	***PCB ID for SW Team (PCB version)***
SKU_ID	***SKU ID for SW Team (Model ID)***
DIS	***GPU***
PSL/ Non PSL	***Support / Non Support KBC Power Switched Logic***
AOU/Non AOU	***USB port AOU function***
EMC/DY-EMC	***EMI team suggest***
Wlan PS/ Wlan Non-ps	***Support WLAN type***
SHARE NON_SHARE	***SPI ROM BOM Control***

C550

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Title: ***COVER PAGE***

Size: A3 | Document Number: **C550-ICL** | Rev: **SC**

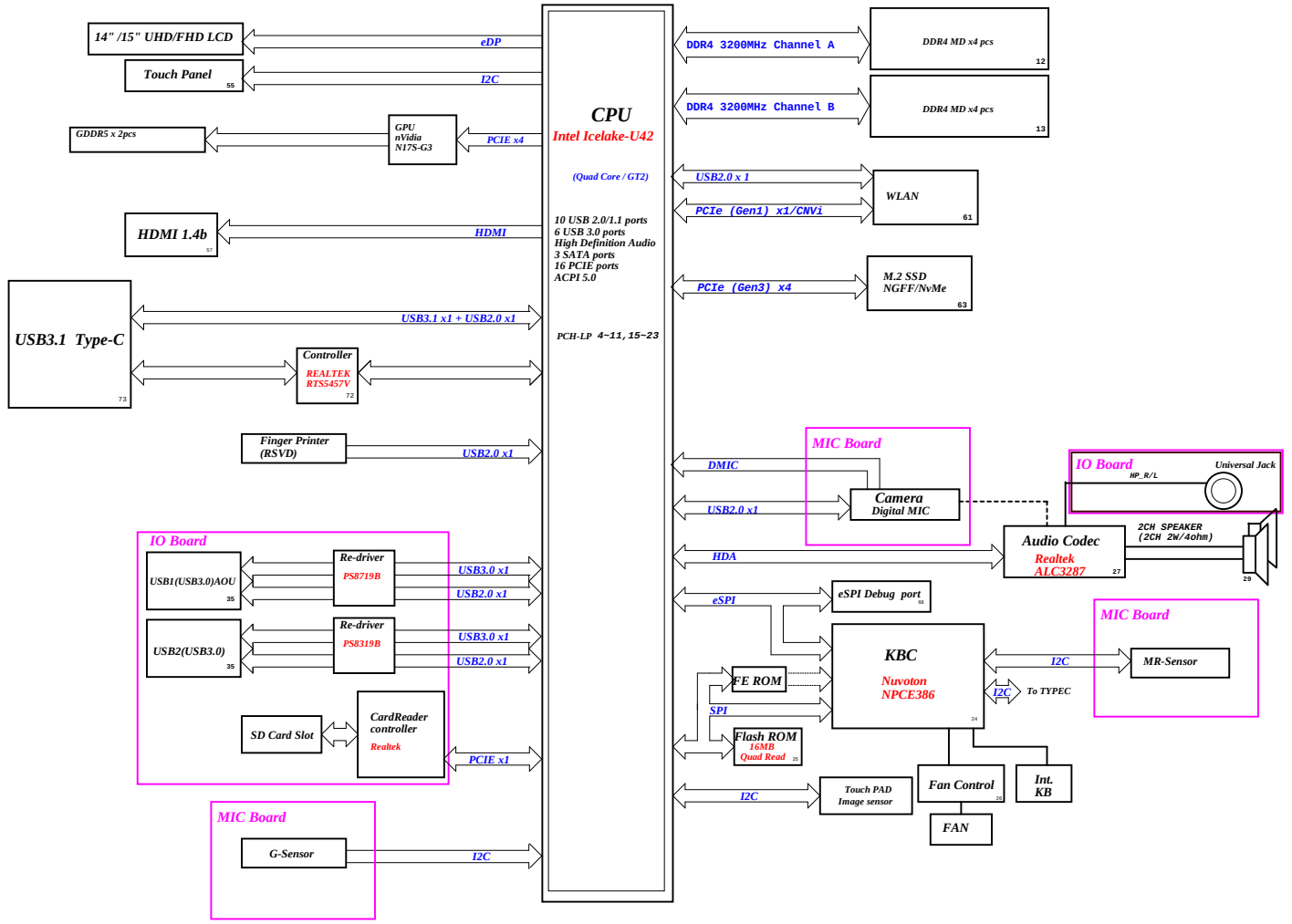
Date: Thursday, March 05, 2020 | Sheet 1 of 106

C550 ICL Block Diagram

Project code: LC55-14C
4PD0K1010001
LC55-15C
4PD0K101B001

PCB P/N: 19792
Revision: SC

IO/Sensor BD



PCB Layer Stackup

L1: Signal
L2: GND/POWER
L3: Signal
L4: Signal
L5: GND/POWER
L6: Signal
L7: GND/POWER
L8: Signal

Battery Charger/Selector BQ25710RSNR-GP 44	
20V_IN	19V_DCBATOUT BT+
System DC/DC TPS51393PRJER-GP TPS51395PRJER-GP 45	
19V_DCBATOUT	PWR_5V PWR_3D3V
CPU_VCORE RT3612EBGQW-1-GP 46	
1V_CPU_CORE AOE6936 47	
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCAUX MP2941BGL-C669-Z-GP 50	
19V_DCBATOUT	1D8V_VCCIN_AUX
DC/DC 1D2V_S3 TPS51486RJER-GP 51	
19V_DCBATOUT	1D2V_S3
DC/DC 0D6V_VREF_S0 TPS51486RJER-GP 51	
5V_S5	0D6V_VREF_S0
DC/DC 1D8V_S5 RT5797ALGQW-GP 53	
19V_DCBATOUT	1D8V_S5
DC/DC 1D05V_S5 APW8738AQBI-TRG-1-GP 54	
5V_S5	1D05V_VNN_BYPASS 1D05V_S5_BYPASS

C550

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
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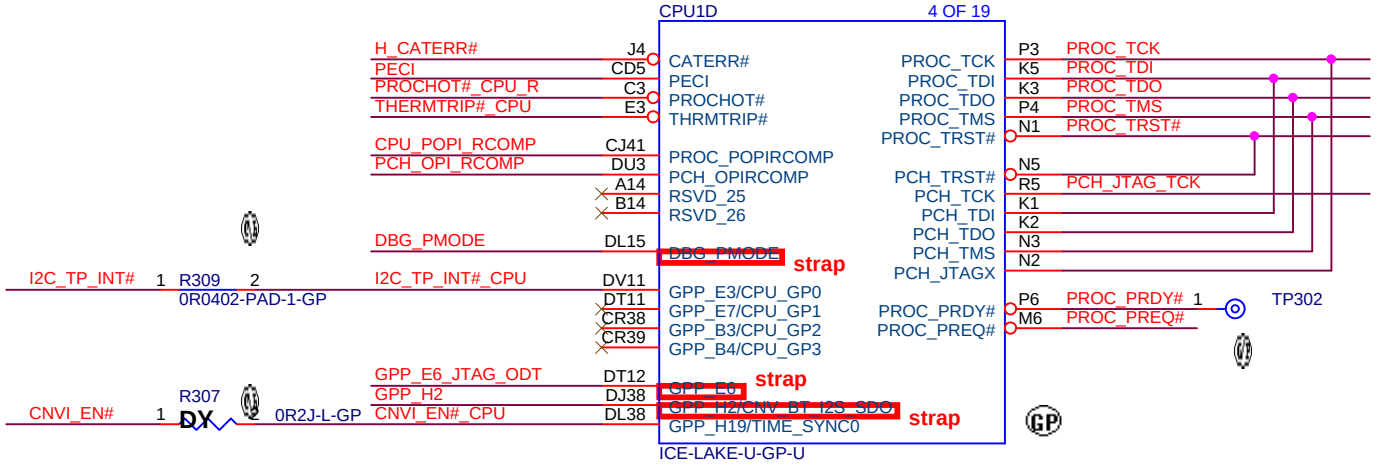
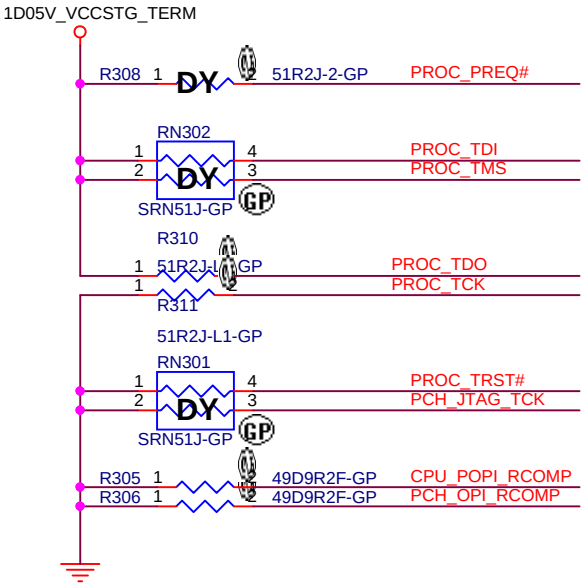
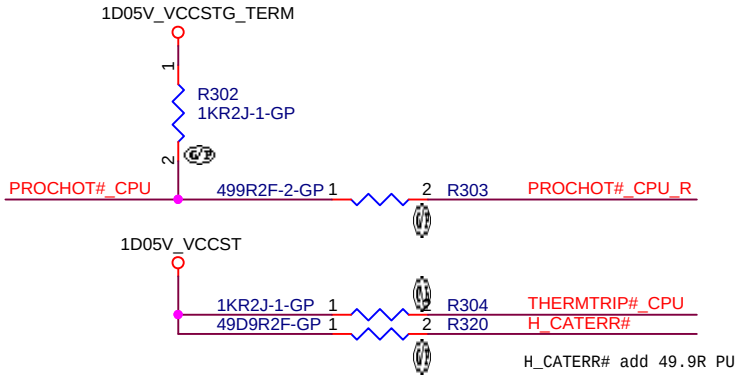
24 PECI
15 DBG_PMODE
24,44,46,72 PROCHOT#_CPU
26 THERMTRIP#_CPU
15 GPP_E6_JTAG_ODT

61 CNVI_EN#
24,65 I2C_TP_INT#
15 GPP_H2

99 PROC_TCK
99 PROC_TDI
99 PROC_TDO
99 PROC_TMS
99 PROC_TRST#
99 PROC_PREQ#
99 PROC_PRDY#
99 PCH_JTAG_TCK







C550

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Title: CPU (THML/JTAG)		
Size: A4	Document Number: C550-ICL	Rev: SC
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eDP

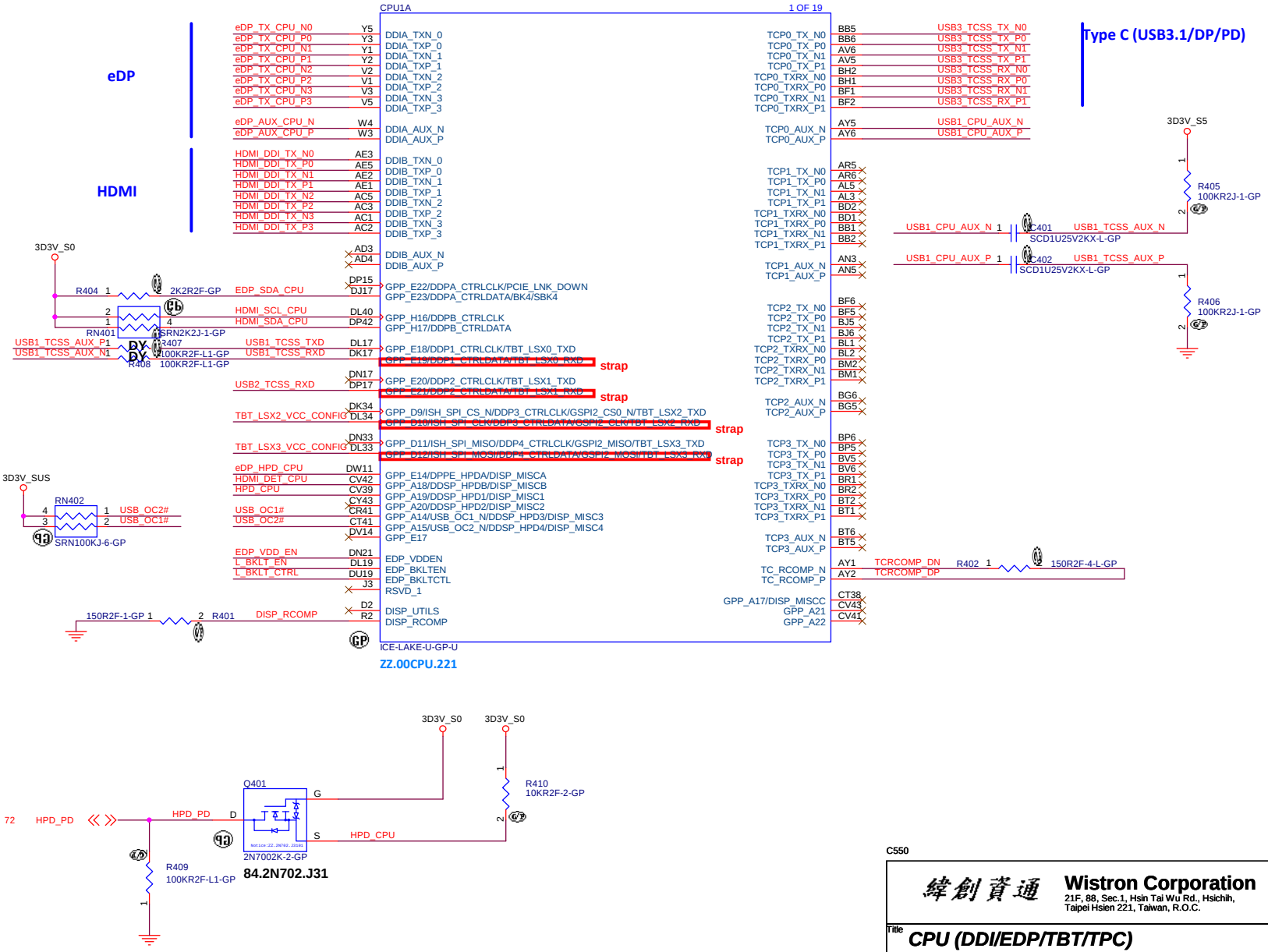
55	eDP_TX_CPU_N0
55	eDP_TX_CPU_P0
55	eDP_TX_CPU_N1
55	eDP_TX_CPU_P1
55	eDP_TX_CPU_N2
55	eDP_TX_CPU_P2
55	eDP_TX_CPU_N3
55	eDP_TX_CPU_P3
55	eDP_AUX_CPU_N
55	eDP_AUX_CPU_P
55	L_BKLT_EN
55	EDP_VDD_EN
55	L_BKLT_CTRL
55	eDP_HPD_CPU

Type C (USB3.1/DP/PD)

73	USB3_TCSS_TX_P0
73	USB3_TCSS_TX_N0
73	USB3_TCSS_RX_P0
73	USB3_TCSS_RX_N0
73	USB3_TCSS_TX_P1
73	USB3_TCSS_TX_N1
73	USB3_TCSS_RX_P1
73	USB3_TCSS_RX_N1
72	USB1_TCSS_AUX_P
72	USB1_TCSS_AUX_N
15	USB1_TCSS_RXD
15	USB2_TCSS_RXD
15	TBT_LSX2_VCC_CONFIG
15	TBT_LSX3_VCC_CONFIG

HDMI

57	HDMI_DDI_TX_N0
57	HDMI_DDI_TX_P0
57	HDMI_DDI_TX_N1
57	HDMI_DDI_TX_P1
57	HDMI_DDI_TX_N2
57	HDMI_DDI_TX_P2
57	HDMI_DDI_TX_N3
57	HDMI_DDI_TX_P3
57	HDMI_SCL_CPU
57	HDMI_SDA_CPU
57	HDMI_DET_CPU



C550

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Title: **CPU (DDI/EDP/TBT/TPC)**

Size	Document Number	Rev
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DDR4

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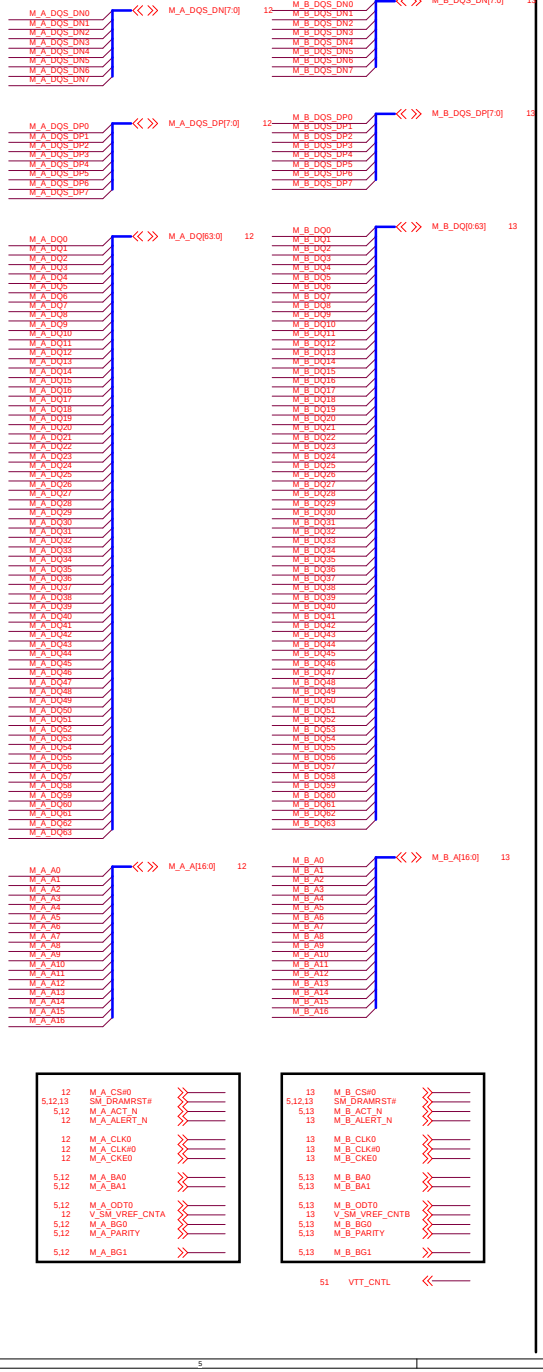

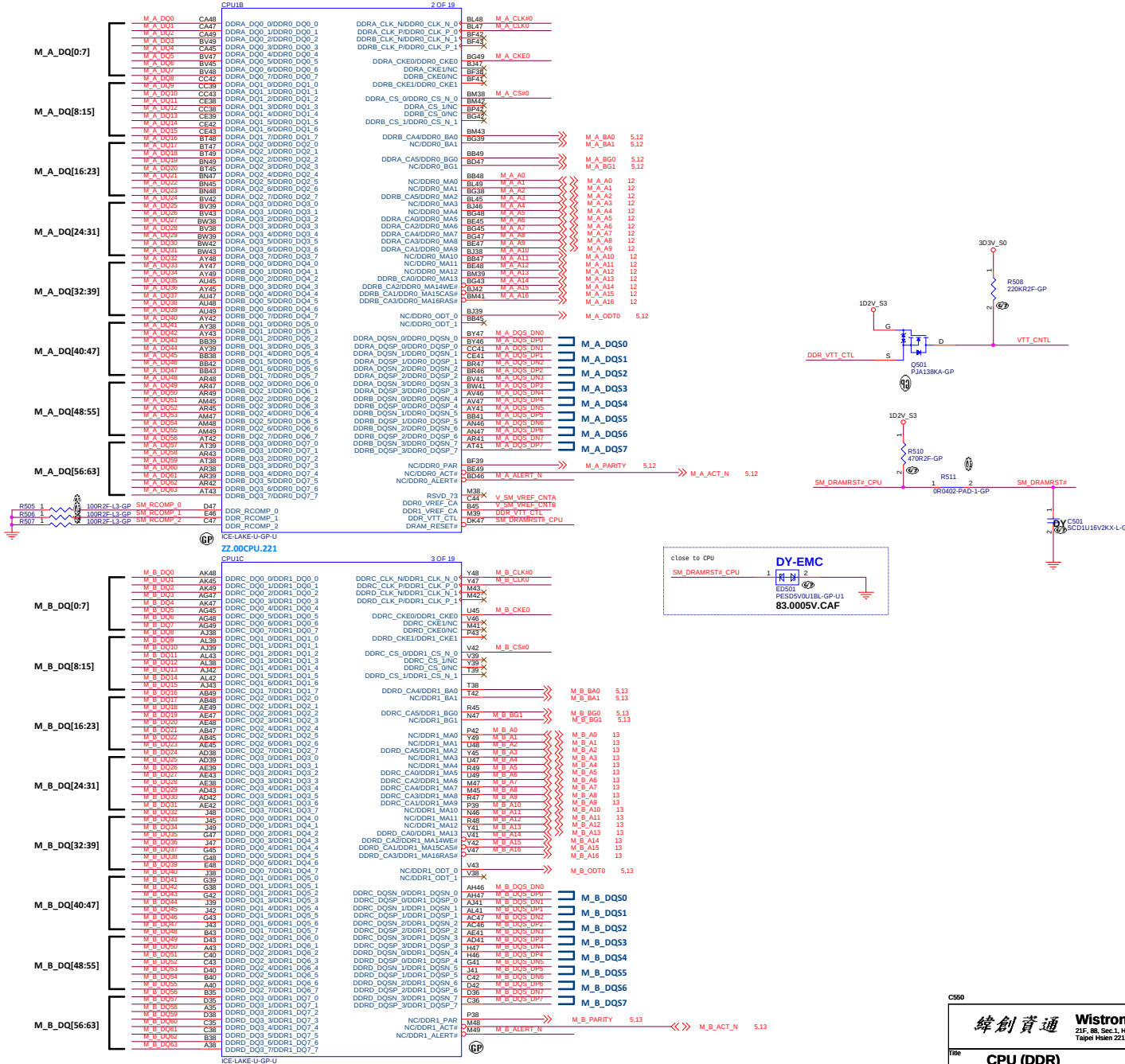

C550

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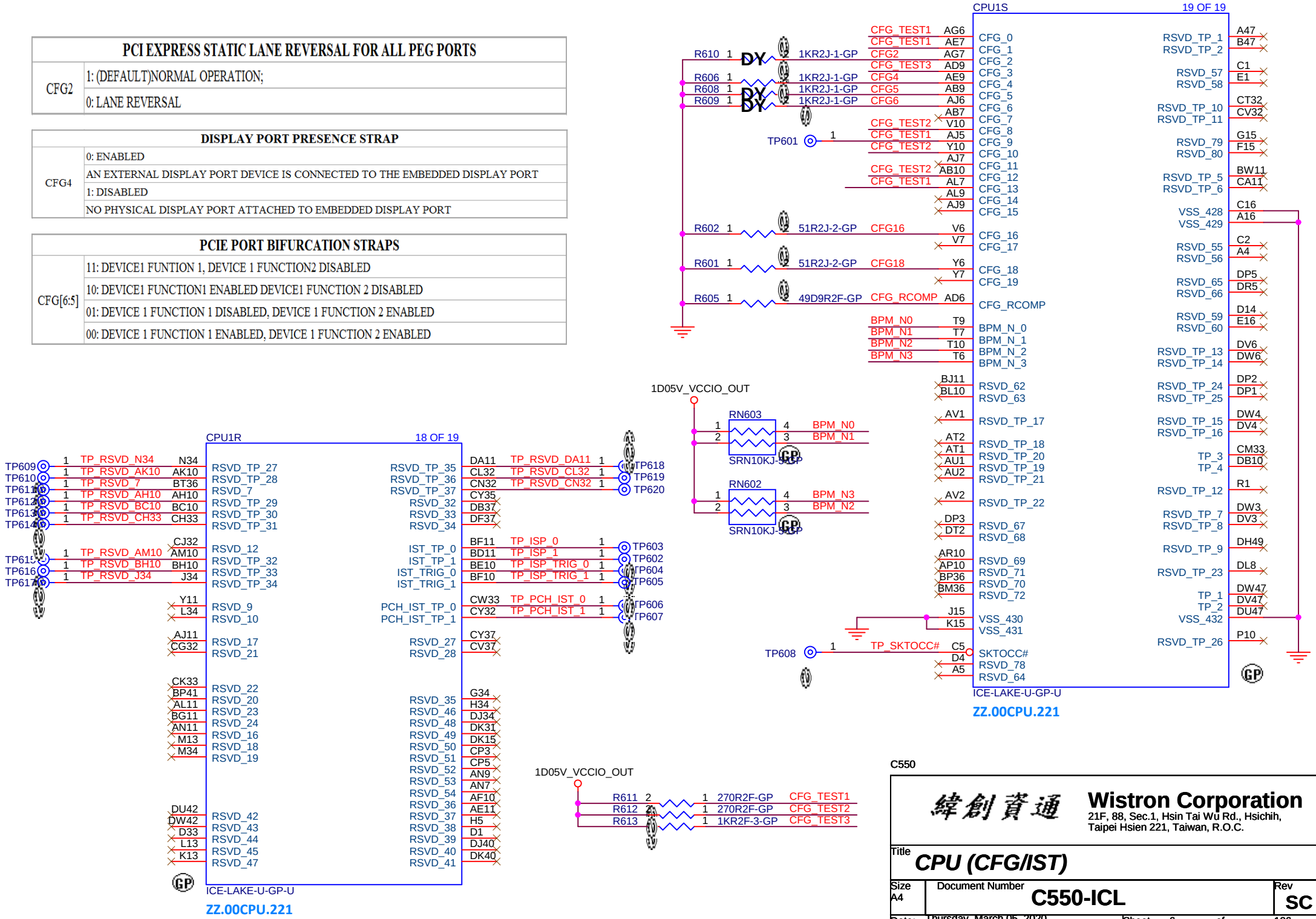
Title	**CPU (DDR)**	
Size A2	Document Number **C550-ICL**	Rev **SC**
Date: Thursday, March 05, 2020	Sheet 5 of 106	

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION;
	0: LANE REVERSAL

DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED
	AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1: DISABLED
	NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
	10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
	01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED



C550

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Title	***CPU (CFG/IST)***	
Size A4	Document Number **C550-ICL**	Rev **SC**
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46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_CLK_CPU
46 SVID_DATA_CPU
46 SVID_ALERT#_CPU

SVID ALERT

1D05V_VCCST

R701
56R2J-4-GP

SVID_ALERT#_CPU — 1 R706 2 — SVID_ALERT#_CPU_R
0R0402-PAD-1-GP

SVID CLK

1D05V_VCCST

R730 1 — DY — 2 100R2J-L-GP — SVID_CLK_CPU

SVID_CLK_CPU reserve 100 Ohm PU

SVID DATA

1D05V_VCCST

R703 1 — 2 100R2F-L-GP-U — SVID_DATA_CPU

1V_CPU_CORE

CPU1L 12 OF 19

A19	VCCIN_1	VCCIN_52	CJ35
AC12	VCCIN_2	VCCIN_53	CK10
V13	VCCIN_3	VCCIN_54	J32
W12	VCCIN_4	VCCIN_55	CL34
Y13	VCCIN_5	VCCIN_56	CL35
K29	VCCIN_6	VCCIN_57	CN34
K31	VCCIN_7	VCCIN_58	CN35
B19	VCCIN_8	VCCIN_59	CP33
B23	VCCIN_9	VCCIN_60	CR34
B27	VCCIN_10	VCCIN_61	A29
B29	VCCIN_11	VCCIN_62	CR35
BN10	VCCIN_12	VCCIN_63	CT33
BP11	VCCIN_13	VCCIN_64	CT34
BP9	VCCIN_14	VCCIN_65	CT35
BR10	VCCIN_15	VCCIN_66	CU33
BT11	VCCIN_16	VCCIN_67	D19
A21	VCCIN_17	VCCIN_68	D21
BT9	VCCIN_18	VCCIN_69	D23
BU10	VCCIN_19	VCCIN_70	D24
BV36	VCCIN_20	VCCIN_71	D27
BV9	VCCIN_21	VCCIN_72	AA12
BW10	VCCIN_22	VCCIN_73	D29
BW36	VCCIN_23	VCCIN_74	F19
BW9	VCCIN_24	VCCIN_75	F21
BY10	VCCIN_25	VCCIN_76	F23
C19	VCCIN_26	VCCIN_77	F24
C23	VCCIN_27	VCCIN_78	F27
A23	VCCIN_28	VCCIN_79	F29
C27	VCCIN_29	VCCIN_80	G1
C29	VCCIN_30	VCCIN_81	G19
CA36	VCCIN_31	VCCIN_82	G23
CA9	VCCIN_32	VCCIN_83	AB1
CB10	VCCIN_33	VCCIN_84	G27
CC11	VCCIN_34	VCCIN_85	G29
CC36	VCCIN_35	VCCIN_86	H19
CC9	VCCIN_36	VCCIN_87	H23
CD10	VCCIN_37	VCCIN_88	H27
CE11	VCCIN_38	VCCIN_89	H29
A24	VCCIN_39	VCCIN_90	J18
CE34	VCCIN_40	VCCIN_91	J20
CE35	VCCIN_41	VCCIN_92	J22
CF10	VCCIN_42	VCCIN_93	J23
CF33	VCCIN_43	VCCIN_94	AB13
CG11	VCCIN_44	VCCIN_95	J26
CG34	VCCIN_45	VCCIN_96	J28
CG35	VCCIN_46	VCCIN_97	K17
CH10	VCCIN_47	VCCIN_98	K19
J30	VCCIN_48	VCCIN_99	K21
CJ11	VCCIN_49	VCCIN_100	K23
A27	VCCIN_50	VCCIN_101	K24
CJ34	VCCIN_51	VCCIN_102	K27
		VCCIN_103	M1
		VCCIN_104	U1
SVID_ALERT#_CPU_R H1	VIDALERT#		
SVID_CLK_CPU H2	VIDSCK	VCCIN_SENSE	F17 VCCCORE_SENSE
SVID_DATA_CPU H3	VIDSOUT	VSSIN_SENSE	G17 VSSCORE_SENSE

ICE-LAKE-U-GP-U

ZZ.00CPU.221

1V_CPU_CORE

R704 1 — 2 100R2F-L-GP-U — VCCCORE_SENSE

R705 1 — 2 100R2F-L-GP-U — VSSCORE_SENSE

Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

C550

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Title: **CPU (VCCIN/VID)**

Size	Document Number	Rev
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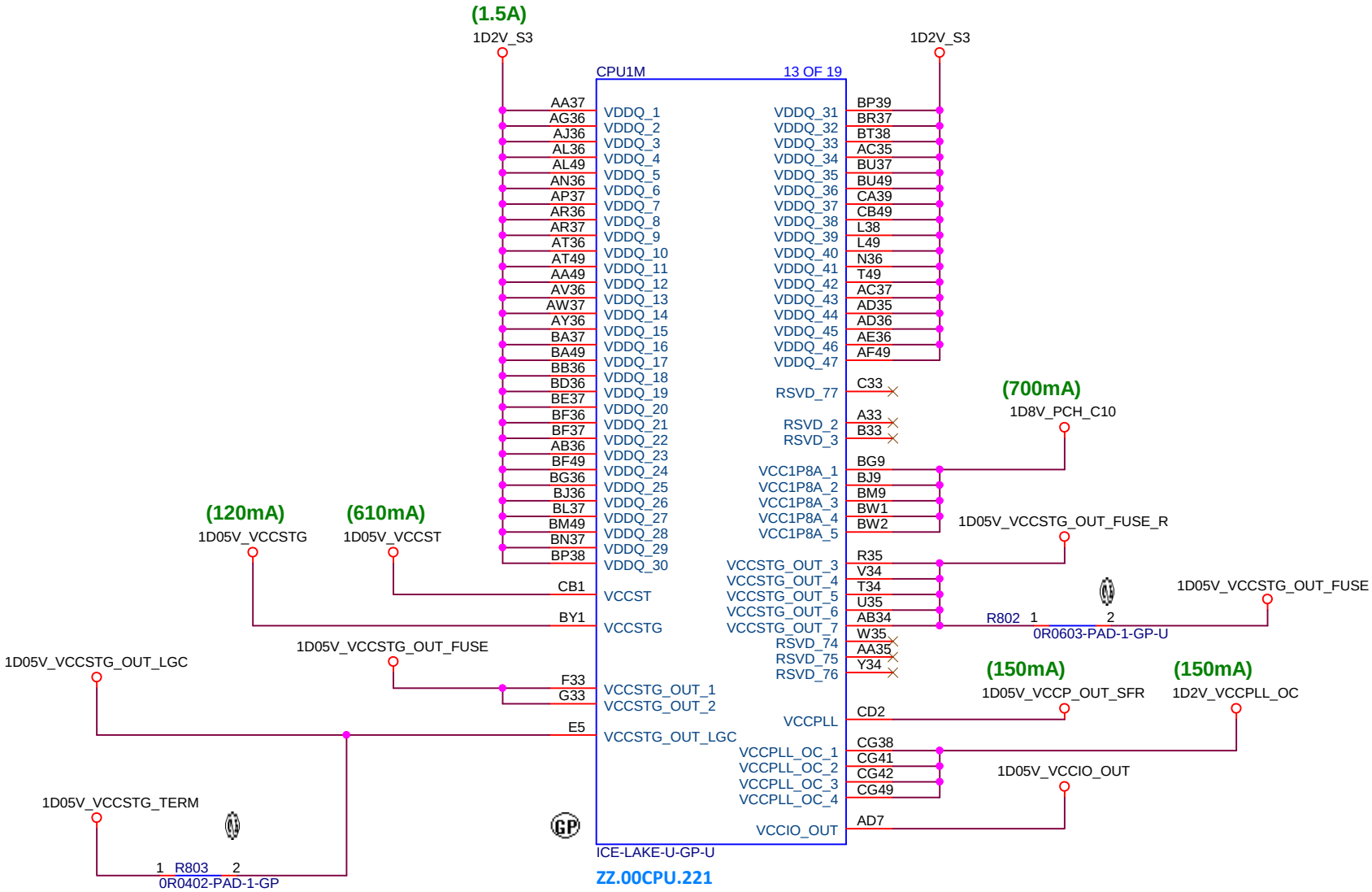

C550

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Title: CPU (VDDQ/VCC/VCCST)

Size	Document Number	Rev
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C550

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Title: ***CPU (RSVD)***

Size	Document Number	Rev
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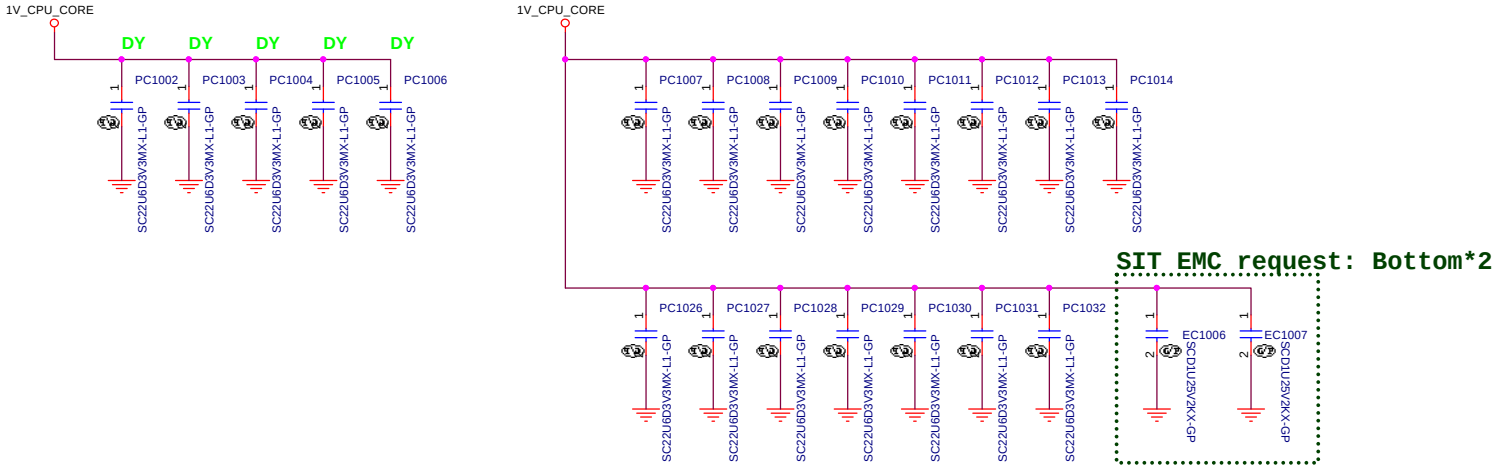
Main Func = CPU

ICL_U42

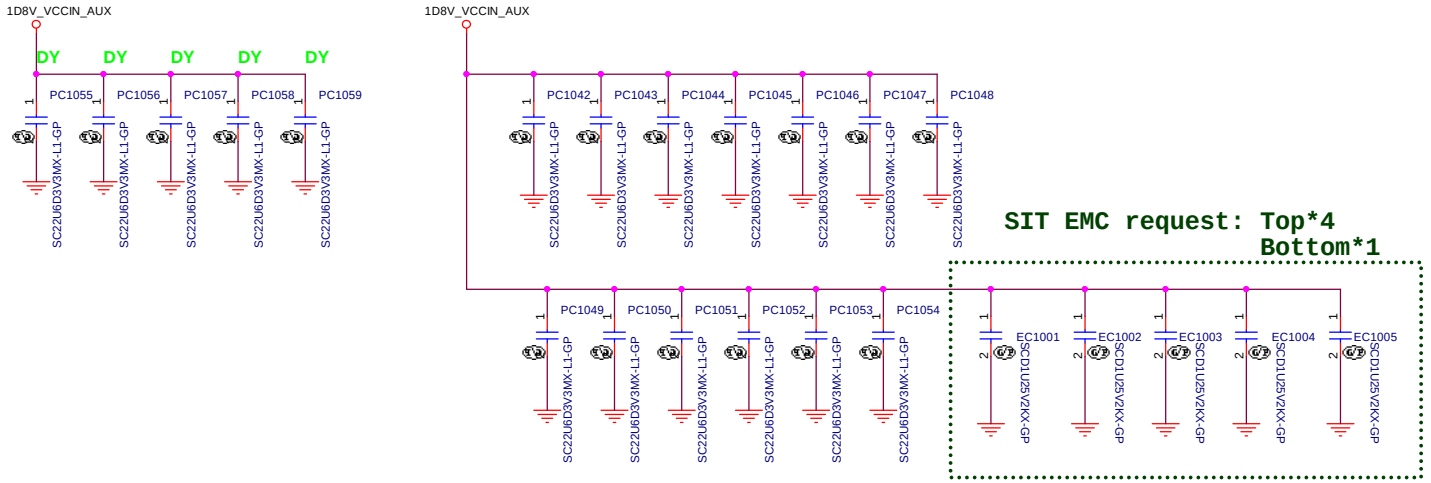
U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	15	220uF*2

VCORE



1D8V_VCCIN_AUX



C550

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Title: CPU (POWER CAP1)

Size: A3 | Document Number: C550-ICL | Rev: SC

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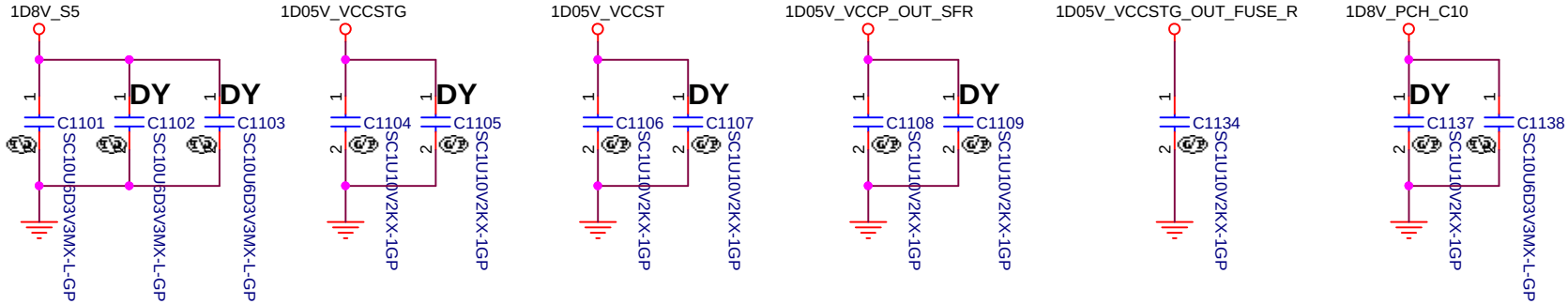
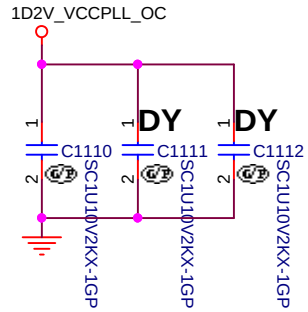
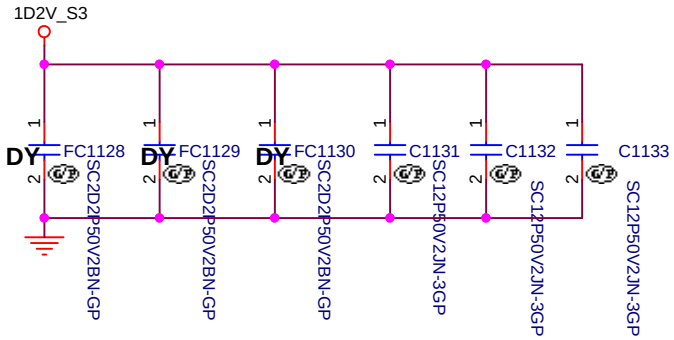


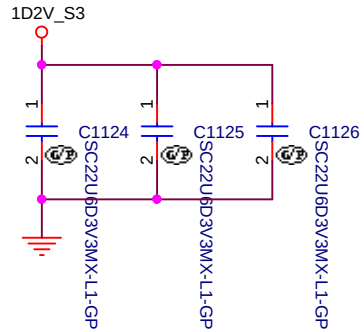
For VCCPLL_OC pin-CG38,CG41,CG42,CG49



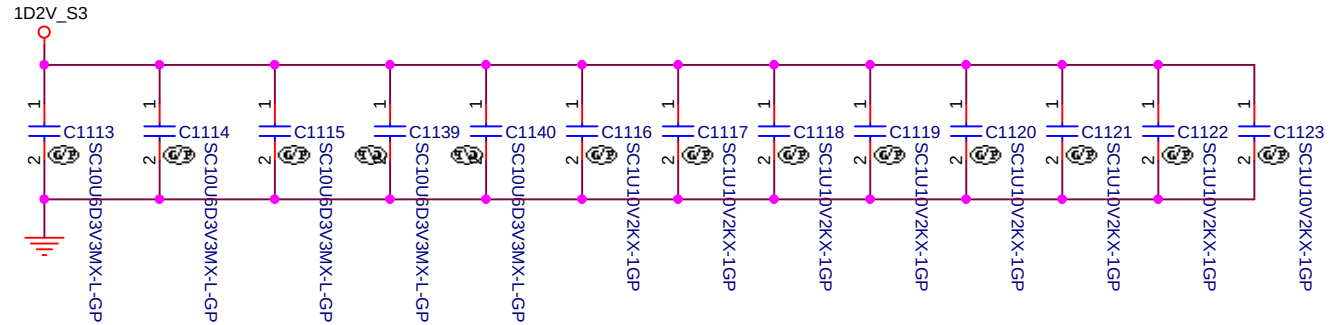
EMC CAPS - PLACE <4mm FROM SOC VDDQ, WITH EACH PAIR <12mm APART



PLACE on CPU Same Side



PLACE on BACK SIDE



C550

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Title: *CPU (POWER CAP2)*		
Size: A4	Document Number: C550-ICL	Rev: SC
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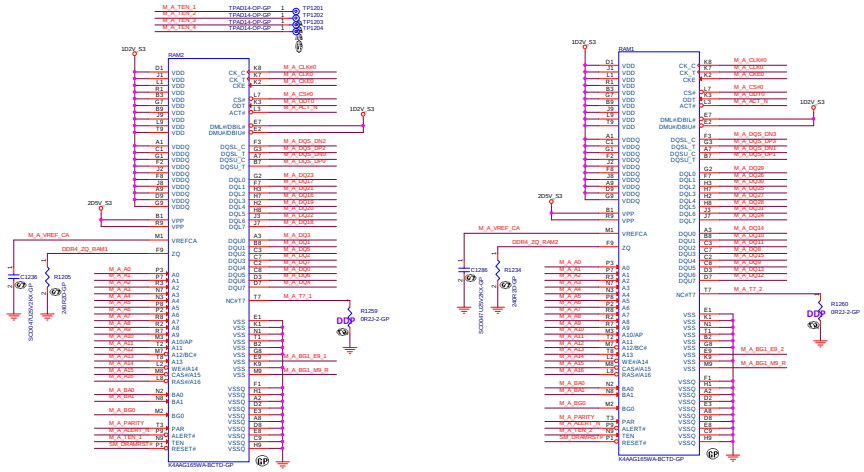
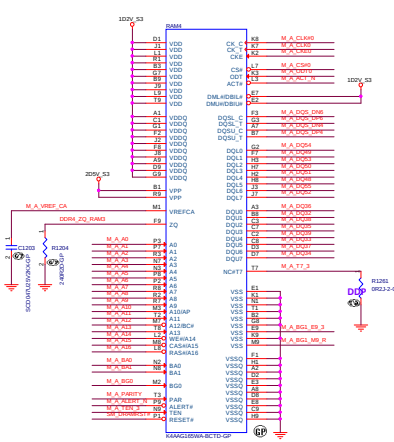
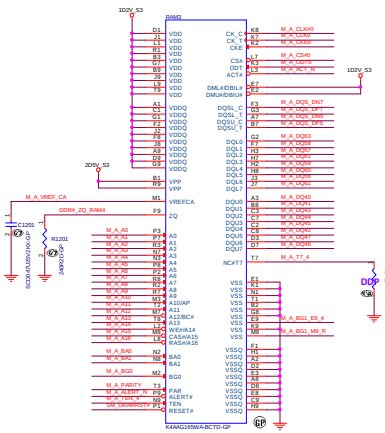
Main Func = DIMM1

Layout Note:Place as pic..







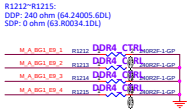
SDP and DDP BOM Control Table

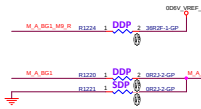
		SDPx16 8Gb	SDPx16 16Gb	SDPx16 8Gb	SDPx16 8Gb	SDPx16 16Gb	DDPx16 16Gb
		SM30N76632 Samsung K4A8G165WC-BCWE	SM30N76633 Samsung K4AAG165WA-BCWE	SM30N76639 SK Hynix H5AN8G6NCJR-VKC	SM30N76570 Micron MT40A512M16TB-062E	SM30N76641 Micron MT40A1G16KD-062E:E	SM30N76640 SK Hynix H5ANAG6NCJR-XNC
DDR4_CTRL	R1212	0R	0R	0R	0R	0R	240R 1%
	R1213	0R	0R	0R	0R	0R	240R 1%
	R1214	0R	0R	0R	0R	0R	240R 1%
	R1215	0R	0R	0R	0R	0R	240R 1%
SDP	R1221	ASM	ASM	ASM	ASM	ASM	DY
DDP	R1220	DY	DY	DY	DY	DY	ASM
	R1224	DY	DY	DY	DY	DY	ASM

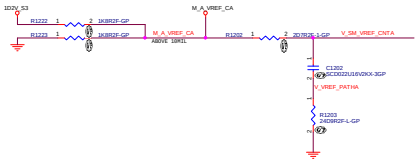
BOM control

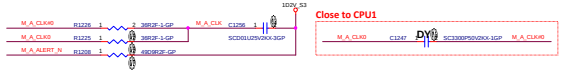
SDP & DDP SETTING

R1212~R1215:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.80034.1DL)

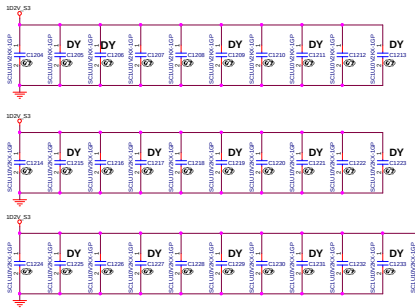




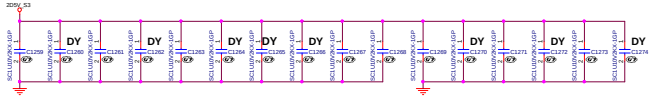




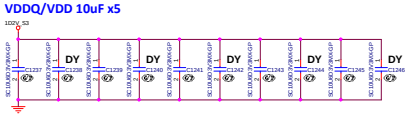
VDDQ/VDD 1uF x16



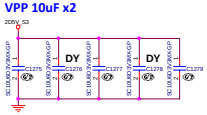
VPP 1uF x8



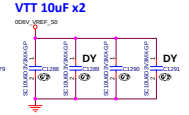
VDDQ/VDD 10uF x5



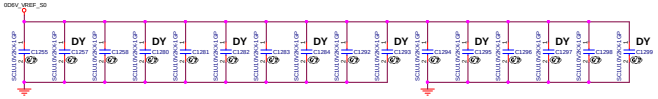
VPP 10uF x2

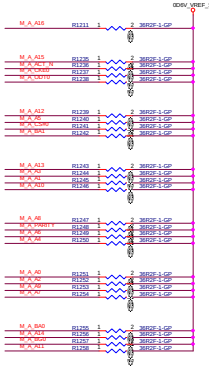


VTT 10uF x2



VTT 1uF x8





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Title	DDR (DDR4-CHA)
Size: A1	Document Number: C550-ICL
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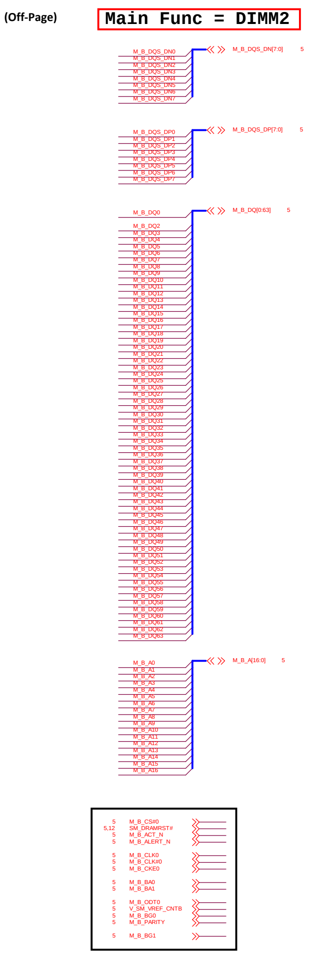
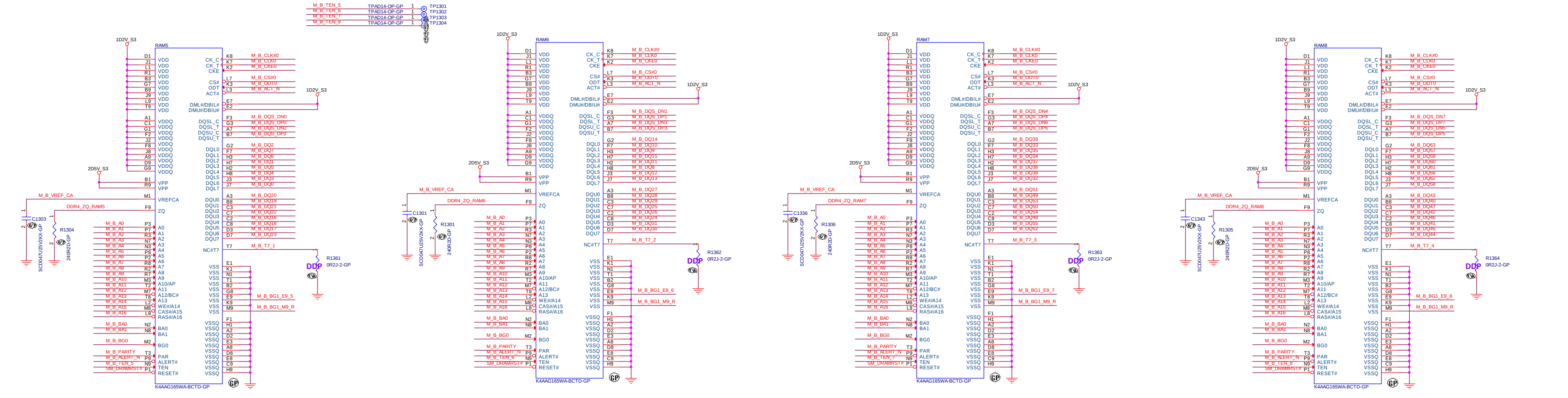
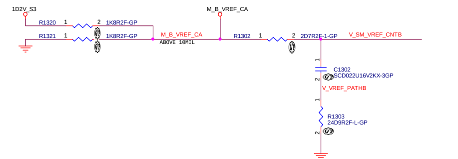






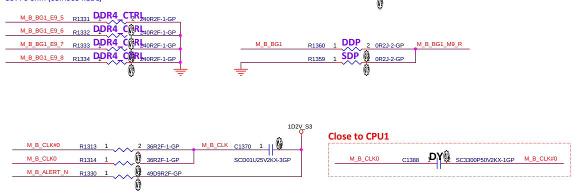
SDP and DDP BOM Control Table

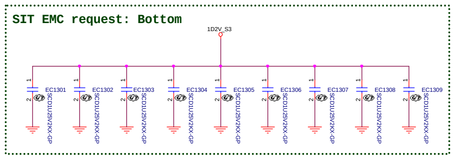
		SDPx16 8Gb	SDPx16 16Gb	SDPx16 8Gb	SDPx16 8Gb	SDPx16 16Gb	DDPx16 16Gb
		SM30N76632 Samsung K4A8G165WC-BCWE	SM30N76633 Samsung K4AAG165WA-BCWE	SM30N76639 SK Hynix H5AN8G6NCJR-VKC	SM30N76570 Micron MT40A512M16TB-062E	SM30N76641 Micron MT40A1G16KD-062E:E	SM30N76640 SK Hynix H5ANAG6NCJR-XNC
DDR4_CTRL	R1331 R1332 R1333 R1334	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%
SDP	R1359	ASM	ASM	ASM	ASM	ASM	DY
DDP	R1312 R1360	DY DY	DY DY	DY DY	DY DY	DY DY	ASM ASM

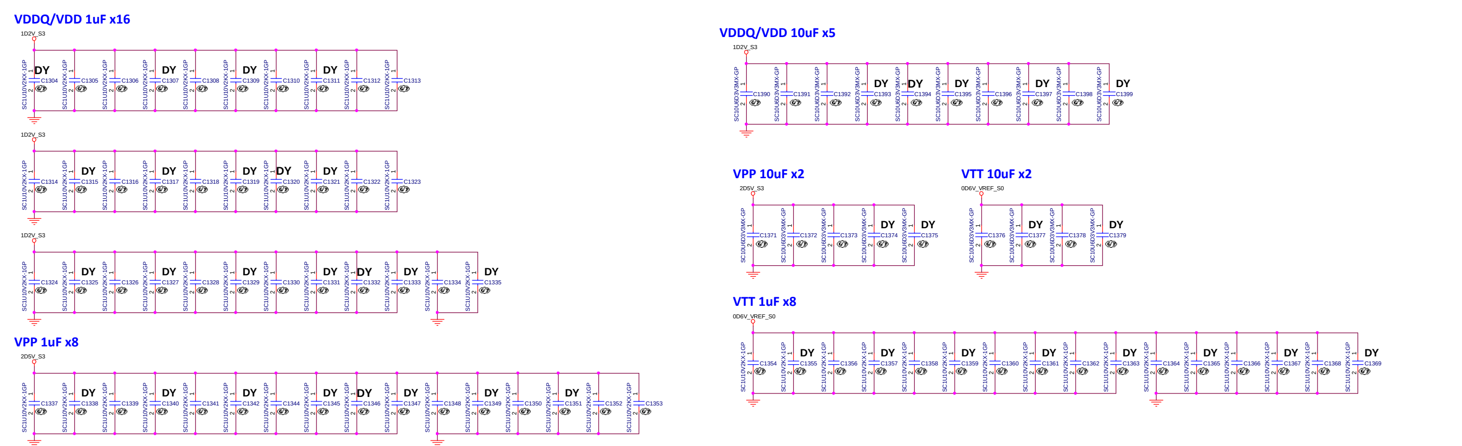
BOM control

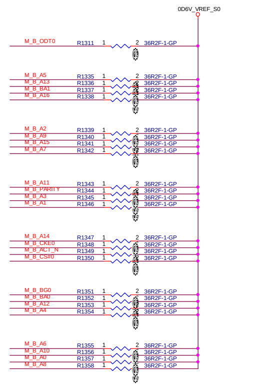
SDP & DDP SETTING

R1331~R1334:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)









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Title	DDR (DDR4-CHB)	
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Title: ***DDR (RSVD)***

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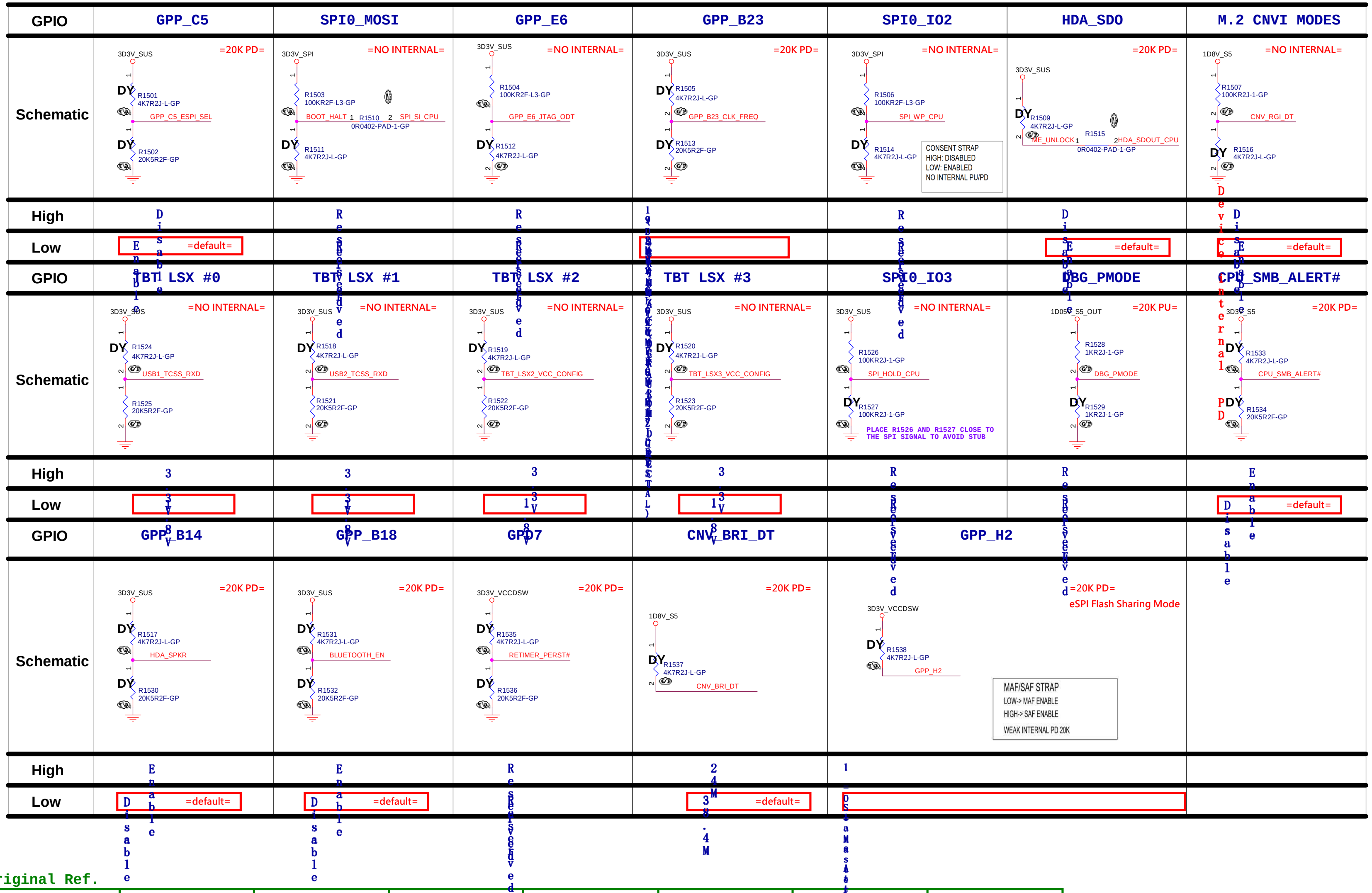
3	DBG_PMODE
18,25	SPI_WP_CPU
18,25	SPI_HOLD_CPU
21,61	CNV_RGI_DT
18	GPP_C5_ESPI_SEL
3	GPP_E6_JTAG_ODT
20	GPP_B23_CLK_FREQ
15,19	HDA_SDOUT_CPU
18,25	SPI_SI_CPU
4	TBT_LSX2_VCC_CONFIG
4	TBT_LSX3_VCC_CONFIG
4	USB1_TCSS_RXD
4	USB2_TCSS_RXD
15,19	HDA_SDOUT_CPU
20,27	HDA_SPKR
20,61	BLUETOOTH_EN
18	CPU_SMB_ALERT#
17	RETIMER_PERST#
21,61	CNV_BRI_DT
3	GPP_H2



Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	HDA_SDO	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**CPU_SMB_ALERT#**	**GPP_B14**	**GPP_B18**	**GPD7**	**CNV_BRI_DT**
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TLS CONFIDENTIALITY LOW - TLS CONFIDENTIALITY DISABLE HIGH - TLS CONFIDENTIALITY ENABLE WEAK INTERNAL PD 20K	TOP SWAP OVERRIDE HIGH- TOP SWAP ENABLED LOW-DISABLED WEAK INTERNAL PD 20K	NO REBOOT HIGH - NO REBOOT LOW- REBOOT ENABLED WEAK INTERNAL PD 20K	XTAL INPUT MODE LOW: XTAL IS ATTACHED HIGH: XTAL INPUT IS SINGLE ENDED WEAK INTERNAL PD 20K	XTAL SEL LOW: 38.4/19.2MHZ (DEFAULT) HIGH = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO) WEAK INTERNAL PD 20K

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Title: **CPU (STRAP)**

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M.2 PCIe SSD

63 SSD_PCIE_RX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_TX_P3
63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P2
63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P1
63 SSD_SATA_RX_N
63 SSD_SATA_RX_p
63 SSD_SATA_TX_N
63 SSD_SATA_TX_p

GFX

76 GFX_PCIE_TX_P0
76 GFX_PCIE_TX_N0
76 GFX_PCIE_TX_P1
76 GFX_PCIE_TX_N1
76 GFX_PCIE_TX_P2
76 GFX_PCIE_TX_N2
76 GFX_PCIE_TX_P3
76 GFX_PCIE_TX_N3
76 GFX_PCIE_RX_P0
76 GFX_PCIE_RX_N0
76 GFX_PCIE_RX_P1
76 GFX_PCIE_RX_N1
76 GFX_PCIE_RX_P2
76 GFX_PCIE_RX_N2
76 GFX_PCIE_RX_P3
76 GFX_PCIE_RX_N3

USB3.0 Port1

66 USB1_USB30_RX_N
66 USB1_USB30_RX_P
66 USB1_USB30_TX_N
66 USB1_USB30_TX_P

USB3.0 Port2

66 USB2_USB30_RX_N
66 USB2_USB30_RX_P
66 USB2_USB30_TX_N
66 USB2_USB30_TX_P

Card Reader

66 CARD_PCIE_RX_N
66 CARD_PCIE_RX_P
66 CARD_PCIE_TX_N
66 CARD_PCIE_TX_P

WLAN

61 WLAN_PCIE_TX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_RX_N

USB2.0 TYPE-C

72 TYPEC_USB20_N
72 TYPEC_USB20_P

RGB Camera

56 CCD_USB20_N
56 CCD_USB20_P

BT

61 BT_USB20_P
61 BT_USB20_N

USB2.0 AOU

36 USB1_USB20_N
36 USB1_USB20_P

USB2.0

66 USB2_USB20_N
66 USB2_USB20_P

Finger Printer

92 FP_USB20_N
92 FP_USB20_P

36 USB_OC0#
36 USB_OC3#
63 SSD_DET#
63 SSD_DEVSLP

CPU1H

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Card Reader

CARD_PCIE_RX_N CV7
CARD_PCIE_RX_P CV6
CARD_PCIE_TX_N DD3
CARD_PCIE_TX_P DD5

WLAN

WLAN_PCIE_RX_N CT6
WLAN_PCIE_RX_P CT7
WLAN_PCIE_TX_N DA3
WLAN_PCIE_TX_P DA5

M.2 PCIe SSD

SSD_PCIE_RX_N3 CP7
SSD_PCIE_RX_P3 CP6
SSD_PCIE_TX_N3 DA2
SSD_PCIE_TX_P3 DA1
SSD_PCIE_RX_N2 CM7
SSD_PCIE_RX_P2 CM6
SSD_PCIE_TX_N2 CY3
SSD_PCIE_TX_P2 CY4
SSD_PCIE_RX_N1 CK7
SSD_PCIE_RX_P1 CK6
SSD_PCIE_TX_N1 CW2
SSD_PCIE_TX_P1 CW1
SSD_SATA_RX_N CJ6
SSD_SATA_RX_P CJ7
SSD_SATA_TX_N CW5
SSD_SATA_TX_P CW3

PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP
PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP
PCIE11_RXN/SATA0_RXN
PCIE11_RXP/SATA0_RXP
PCIE11_TXN/SATA0_TXN
PCIE11_TXP/SATA0_TXP
PCIE12_RXN/SATA1A_RXN
PCIE12_RXP/SATA1A_RXP
PCIE12_TXN/SATA1A_TXN
PCIE12_TXP/SATA1A_TXP

TP1601 1 DCI_1 CG7
TP1602 1 DCI_2 CG6
TP1603 1 DCI_3 CT3
TP1604 1 DCI_4 CT5

PCIE13_RXN
PCIE13_RXP
PCIE13_TXN
PCIE13_TXP
PCIE14_RXN CE6
PCIE14_RXP CE7
PCIE14_TXN CT2
PCIE14_TXP CT1
PCIE15_RXN/SATA1B_RXN CC5
PCIE15_RXP/SATA1B_RXP CC6
PCIE15_TXN/SATA1B_TXN CR3
PCIE15_TXP/SATA1B_TXP CR4
PCIE16_RXN/SATA2_RXN CA6
PCIE16_RXP/SATA2_RXP CA5
PCIE16_TXN/SATA2_TXN CP1
PCIE16_TXP/SATA2_TXP CP2

GPP_E0/SATAXPCIE0/SATAGP0 DW12
GPP_A12/SATAXPCIE1/SATAGP1 CR42
GPP_A13/SATAXPCIE2/SATAGP2 CR43
GPP_E9/USB_OC0# DW14
GPP_A16/USB_OC3# CT43
GPP_E4/DEVSLP0 DU12
GPP_E5/DEVSLP1 DU11
GPP_A11/SATA_DEVSLP2 CV48
GPP_H12/M2_SKT2_CFG0 DT38
GPP_H13/M2_SKT2_CFG1 DW38
GPP_H14/M2_SKT2_CFG2 DV38
GPP_H15/M2_SKT2_CFG3 DU38
PCIE_RCOMPN DN1
PCIE_RCOMPP DN3

ICE-LAKE-U-GP-U

ZZ.00CPU.221

PCIE1_RXN/USB31_1_RXN DJ8
PCIE1_RXP/USB31_1_RXP DJ6
PCIE1_TXN/USB31_1_TXN DJ2
PCIE1_TXP/USB31_1_TXP DJ1
PCIE2_RXN/USB31_2_RXN DG9
PCIE2_RXP/USB31_2_RXP DG7
PCIE2_TXN/USB31_2_TXN DJ3
PCIE2_TXP/USB31_2_TXP DJ5
PCIE3_RXN/USB31_3_RXN DE7
PCIE3_RXP/USB31_3_RXP DE9
PCIE3_TXN/USB31_3_TXN DF3
PCIE3_TXP/USB31_3_TXP DF5
PCIE4_RXN/USB31_4_RXN DC7
PCIE4_RXP/USB31_4_RXP DC9
PCIE4_TXN/USB31_4_TXN DF2
PCIE4_TXP/USB31_4_TXP DF1
PCIE5_RXN/USB31_5_RXN DA6
PCIE5_RXP/USB31_5_RXP DA7
PCIE5_TXN/USB31_5_TXN DE4
PCIE5_TXP/USB31_5_TXP DE3
PCIE6_RXN/USB31_6_RXN CY7
PCIE6_RXP/USB31_6_RXP CY6
PCIE6_TXN/USB31_6_TXN DD1
PCIE6_TXP/USB31_6_TXP DD2

USBN2P_1 DN8
USBN2P_2 DK11
USBN2P_3 DP13
USBN2P_4 DK10
USBN2P_5 DL5
USBN2P_6 DP11
USBN2P_7 DK13
USBN2P_8 DN6
USBN2P_9 DL2
USBN2P_10 DP10
USB_ID DL6
USB_VBUSSENSE DL11
USB2_COMP DN5
RSVD_81 CD3

GFX

GFX_PCIE_RX_N0
GFX_PCIE_RX_P0
GFX_PCIE_TX_N0
GFX_PCIE_TX_P0
GFX_PCIE_RX_N1
GFX_PCIE_RX_P1
GFX_PCIE_TX_N1
GFX_PCIE_TX_P1
GFX_PCIE_RX_N2
GFX_PCIE_RX_P2
GFX_PCIE_TX_N2
GFX_PCIE_TX_P2
GFX_PCIE_RX_N3
GFX_PCIE_RX_P3
GFX_PCIE_TX_N3
GFX_PCIE_TX_P3

USB3.0 Port1

USB1_USB30_RX_N
USB1_USB30_RX_P
USB1_USB30_TX_N
USB1_USB30_TX_P

USB3.0 Port2

USB2_USB30_RX_N
USB2_USB30_RX_P
USB2_USB30_TX_N
USB2_USB30_TX_P

USB2.0 TYPE-C

TYPEC_USB20_N
TYPEC_USB20_P

RGB Camera

CCD_USB20_N
CCD_USB20_P

USB2.0 AOU

USB1_USB20_N
USB1_USB20_P

USB2.0

USB2_USB20_N
USB2_USB20_P

Finger Printer

FP_USB20_N
FP_USB20_P

BT

BT_USB20_N
BT_USB20_P

USB_ID
USB_VBUSSENSE
USB2_COMP

USB_OC#

USB_OC0#	USB3.0 Power
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	USB3.0 Power

3D3V_SUS
3D3V_S0
R1606 1 100KR2F-L1-GP 1 USB_OC0#
R1607 100KR2F-L1-GP 1 USB_OC3#
SSD_DET#
SSD_DEVSLP
DY
R1605 10KR2F-L1-GP
R1601 1 100R2F-L3-GP PCIE_RCOMPN PCIE_RCOMPP

R1604 1 10KR2F-L1-GP
R1602 1 10KR2F-L1-GP
R1603 1 113R2F-GP

PCIe Port Assignment		Share BUS
Port1	GFX	USB3.0
Port2		
Port3		USB3.0
Port4		
Port5	USB3.0 Port1	
Port6	USB3.0 Port2	
Port7	Card reader	
Port8	WLAN	
Port9	M.2 SSD	SATA
Port10		
Port11		
Port12		
Port13	N/A	
Port14	N/A	
Port15	N/A	
Port16	N/A	

USB2.0 Port Assignment	
Port1	USB2.0 TYPE-C
Port2	RGB Camera
Port3	N/A
Port4	USB2.0 AOU
Port5	USB2.0
Port6	Finger Printer
Port7	N/A
Port8	N/A
Port9	N/A
Port10	Bluetooth

Place TOP Side

USB1_USB20_N 1 AFTP1601
USB1_USB20_P 1 AFTP1602
USB2_USB20_N 1 AFTP1603
USB2_USB20_P 1 AFTP1604
1 AFTP1605

C550

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

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40,53 PM_SLP_SUS#
99 PM_SLP_S5#
24,40,51 PM_SLP_S4#
24,40,54,86 PM_SLP_S3#
99 PM_SLP_A#
55 PM_SLP_S0#
61 PM_SLP_WLAN#

99 SYS_RESET#
24,26,61,63,66,76 PLT_RST#
24 PCH_RSMRST#
15 RETIMER_PERST#

24 PM_PWRBTN#
24 AC_PRESENT

40 C10_PWR_GATE#
40 VCCST_OVERRIDE

24,40 ALL_SYS_PWRGD
45 3V_5V_PWRGD
40 PCH_PWROK
24 SYS_PWROK

61 PCIE_WAKE#

72 CPU_SMB_INT#

24 DSW_PWROK

CPU1K 11 OF 19

PM_SLP_SUS# DM49 SLP_SUS#
PM_SLP_S5# DF45 GPD10/SLP_S5#
PM_SLP_S4# DC48 GPD5/SLP_S4#
PM_SLP_S3# DF47 GPD4/SLP_S3#
PM_SLP_A# DH47 GPD6/SLP_A#
PM_SLP_S0# CL45 GPP_B12/SLP_S0#
PM_SLP_WLAN# DE49 GPD9/SPL_WLAN#
DN48 SLP_LAN#
PM_RSMRST# DG49 RSMRST#
SYS_RESET# DK19 SYS_RESET#
PLT_RST# CM49 GPP_B13/PLTRST#
INPUT3VSEL DN49 INPUT3VSEL
RTC_INTRUDER# DR47 INTRUDER#

GPD3/PWRBTN# CY42 PM_PWRBTN#
GPD1/ACPRESENT DE46 AC_PRESENT
GPD0/BATLOW# DH48 PM_BATLOW#
GPP_B11/PMCALERT CL39 CPU_SMB_INT#
GPP_H18/CPU_C10_GATE# DU40 C10_PWR_GATE#
GPP_H3/SX_EXIT_HOLDOFF_N/CNV_BT_I2S_SDO DG40
WAKE# DL45 PCIE_WAKE#
GPD_2/LAN_WAKE# DE47 LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON DF48 TP_RSVD_DSWLDO
VCCST_OVERRIDE CE4 VCCST_OVERRIDE_R
VCCST_PWRGD CF2 VCCST_PWRGD_R
VCCSTPWRGOOD_TCSS CE3 VCCSTPWRGOOD_TCSS
PROCPWRGD CF1 TP_VCORE_PWRGD
GPD7 DC47 RETIMER_PERST#

strap
strap

ICE-LAKE-U-GP-U

ZZ.00CPU.221

R1732 1 DY 2 75KR2J-GP
TP1701
R1728 1 2 VCCST_OVERRIDE
0R0402-PAD-1-GP
R1731 1 2 VCCST_OVERRIDE
0R0402-PAD-1-GP
TP1702

PM_RSMRST# R1723 1 DY 2 0R2J-L-GP DSW_PWROK_R DR48
PCH_PWROK R1720 1 0R0402-PAD-1-GP PCH_PWROK_R DN47
SYS_PWROK R1724 1 0R0402-PAD-1-GP SYS_PWROK_R DP19

close to CPU

PM_RSMRST#
DY
ED1702
PESD5V0U1BL-GP-U1
83.0005V.CAF

3D3V_S0
R1701 1 2 1KR2F-3-GP SYS_RESET#
R1712 1 2 100KR2J-1-GP C10_PWR_GATE#

3D3V_S5
R1713 1 2 100KR2J-1-GP AC_PRESENT
R1714 1 2 10KR2J-3-GP LAN_WAKE#
R1715 1 2 10KR2J-3-GP PM_BATLOW#
R1740 1 DY 2 20KR2F-L-GP DSW_PWROK_R

3D3V_SUS
R1716 1 2 10KR2J-3-GP PCIE_WAKE#
R1730 1 2 100KR2J-1-GP VCCST_OVERRIDE_R
R1735 1 DY 2 100KR2J-1-GP PM_SLP_S4#
R1736 1 DY 2 100KR2J-1-GP PM_SLP_S3#
R1737 1 DY 2 100KR2J-1-GP PM_SLP_A#
R1733 1 DY 2 100KR2J-1-GP PM_SLP_WLAN#

SPI Voltage STRAP

3V SELECT STRAP
LOW → 3.3V +/-5%
HIGH → 3.0V +/-5%

3D3V_RTC_AUX
DY R1704 1MR2F-GP
RTC_INTRUDER#
R1750 10KR2J-L-GP

3D3V_S5
DY R1705 4K7R2J-L-GP
INPUT3VSEL
R1706 100KR2J-1-GP

add RTC_INTRUDER# 10K PD_20181129_Thomas

The VCCSPI voltage (3.3V or 1.8V) is selected via a hard strap on the INTRUDER#.
0 = SPI interface operation voltage is 3.3V (ground through a 10 kohm resistor)
1 = SPI interface operation voltage is 1.8V (pulled up with 1 Mohm to VCCRTC)

3D3V_AUX_S5
R1707 1 2 100KR2J-GP
R1708 10KR2J-3-GP
Q1701
3V_5V_POK#
2N7002KDW-1-GP
75.27002.F7C

PM_RSMRST# R1711 1 2 100KR2J-1-GP
R1709 1 2 1KR2J-1-GP PCH_RSMRST#
3V_5V_POK_C R1710 1 2 3V_5V_PWRGD
0R0402-PAD-1-GP
R1722 1 DY 2 0R2J-2-GP PM_SLP_SUS#

3D3V_SUS
1D05V_VCCST
U1701
ALL_SYS_PWRGD
NC#1 VCC
A
GND Y
74LVC1G07GW-GP
73.01G07.0HG
C1702 SCD1U16V2KX-L-GP
R1719 1KR2F-3-GP
VCCST_PWRGD
R1721 60D4R2F-GP
VCCST_PWRGD_R
Volatge Level 1V

DSW_PWROK_R 1 R1725 2 DSW_PWROK
0R0402-PAD-1-GP
R1726 1MR2J-1-GP DY
C1703 SC1U10V2KX-L1-GP
Delay 3D3V_S5 over 10ms.

C550

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: Custom
Document Number: C550-ICL
Rev: SC
Date: Thursday, March 05, 2020
Sheet 17 of 106

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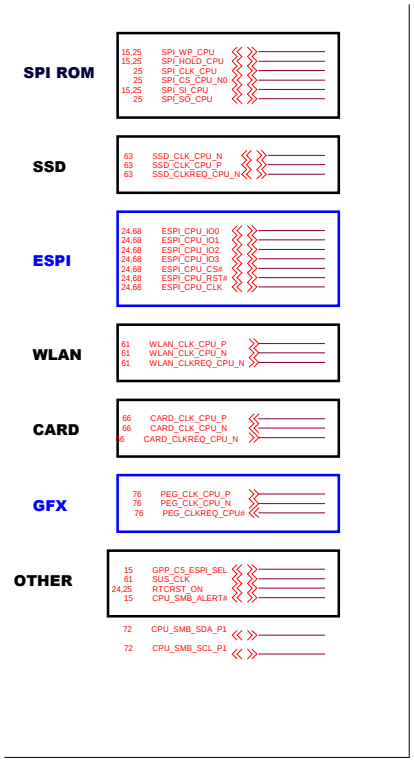

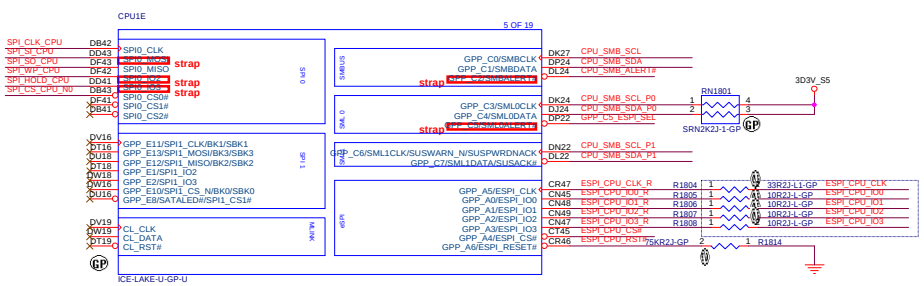

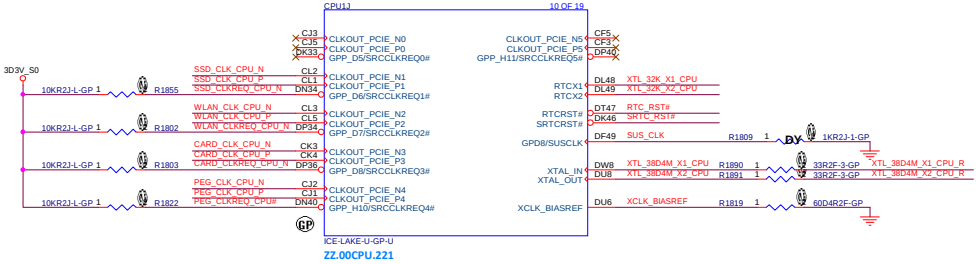

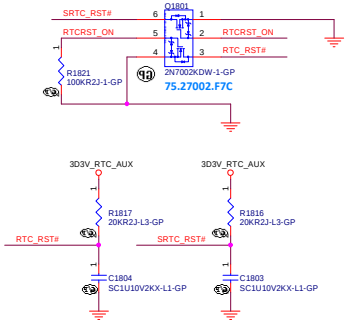

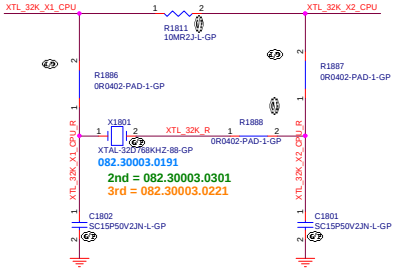

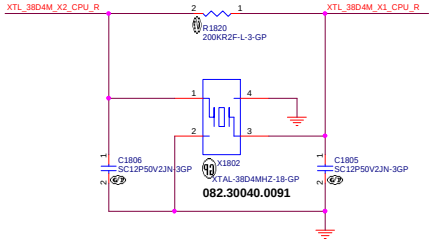

BOM Control

X1801 (32.768KHz)	C1801(Cd)	C1802(Cg)
EPSON 082.30003.0191	15pF	15pF
SEIKO 082.30003.0301	15pF	15pF
NDK 082.30003.0221	15pF	15pF

X1802 (38.4MHz)	C1806	C1805	
HARMONY 082.30040.0091	12pF	12pF	FVT verify
HOSONIC 082.30040.0161	12pF	12pF	FVT verify
TXC 082.30040.0171	12pF	12pF	FVT shortage

C550

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)

Size: A2 | Document Number: C550-ICL | Rev: SC

Date: Thursday, March 05, 2020 | Sheet 18 of 106

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Codec

27 HDA_BITCLK_CODEC
27 HDA_SYNC_CODEC
27 HDA_SDOUT_CODEC
27 HDA_SDIN0_CPU
27 HDA_RST_CODEC
15 HDA_SDOUT_CPU

CNVi

61 CNV_CLKREQ
61 CNV_RF_RESET

Dmic

55 DMIC_SCL_CODEC_EDP
55 DMIC_SDA_CODEC_EDP

Other

24 CPU_MS
24 ME_FWP

1D8V_S5

RN1901
DMIC_SCL_CODEC_EDP 1 4
DMIC_SDA_CODEC_EDP 2 3
SRN2K2J-3-GP

EL1901 68.00358.031 -> 0ohm 63.R0034.1DL 0402
20200225_SVT_EC

HDA_BITCLK_CODEC — EL1901 1 2 0R2J-L-GP — HDA_BITCLK_CPU — CY46
HDA_SYNC_CODEC — R1901 1 2 0R2J-L-GP — HDA_SYNC_CPU — CV49
HDA_SDOUT_CODEC — R1905 1 2 0R2J-L-GP — HDA_SDOUT_CPU — CY47
HDA_SDIN0_CPU — CV45
HDA_RST_CODEC — R1911 1 2 33R2J-2-GP — HDA_RST_N_CPU — DA47
ME_FWP — R1920 1 2 1K1R2F-GP — DP33

DY EC1901 SC10P50V2JN-L1-GP

CNV_RF_RESET — CT48
CNV_CLKREQ — CV47 / CT47

CPU1G

GPP_R0/HDA_BCLK/I2S0_SCLK
GPP_R1/HDA_SYNC/I2S0_SFRM
GPP_R2/HDA_SDO/I2S0_TXD — strap
GPP_R3/HDA_SDI0/I2S0_RXD
GPP_R4/HDA_RST#
GPP_D19/I2S_MCLK
GPP_A23/I2S1_SCLK — DC45
GPP_R5/HDA_SDI1/I2S1_SFRM — DA49
GPP_R6/I2S1_TXD — DA45
GPP_R7/I2S1_RXD — DA48
GPP_A7/I2S2_SCLK — CT49
GPP_A8/I2S2_SFRM/CNV_RF_RESET# — CT48
GPP_A10/I2S2_RXD — CV47
GPP_A9/I2S2_TXD/MODEM_CLKREQ — CT47
GPP_S0/SNDW1_CLK — CY39
GPP_S1/SNDW1_DATA — CY38
GPP_S2/SNDW2_CLK — DB39
GPP_S3/SNDW2_DATA — DD38
GPP_S4/SNDW3_CLK/DMIC_CLK1 — DF38
GPP_S5/SNDW3_DATA/DMIC_DATA1 — DD39

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GPP_G6/SD_CLK — CE46
GPP_G1/SD_DATA0 — CC48
GPP_G2/SD_DATA1 — CC49 — CPU_MS
GPP_G3/SD_DATA2 — CC47
GPP_G4/SD_DATA3 — CF45
GPP_G0/SD_CMD — CC45
GPP_G7/SD_WP — CF49
GPP_G5/SD_CD# — CE47
SD3.0
GPP_H0/CNV_BT_I2S_SDO — DK38
GPP_H1/SD_PWR_EN_N/CNV_BT_I2S_SDO — DG38
SD3_RCOMP — CJ43 — SD3_RCOMP — R1902 1 2 200R2F-L-GP
R1904 33R2J-2-GP
GPP_S6/SNDW4_CLK/DMIC_CLK0 — DG36 — DMIC_SCL_CPU — 1 2 — DMIC_SCL_CODEC_EDP
GPP_S7/SNDW4_DATA/DMIC_DATA0 — DG34 — DMIC_SDA_CPU — 1 2 — DMIC_SDA_CODEC_EDP
R1906
SNDW_RCOMP — CV38 — SNDW_RCOMP — 33R2J-2-GP
R1903 200R2F-L-GP
AUDIO

ICE-LAKE-U-GP-U

ZZ.00CPU.221

C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (HAD/I2S/SD/DMIC)**

Size	Document Number	Rev
A4	C550-ICL	SC

Date: Thursday, March 05, 2020 Sheet 19 of 106

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15 GPP_B23_CLK_FREQ
25 RTC_DET#
15,27 HDA_SPKR
15,61 BLUETOOTH_EN
24,61 WIFI_RF_EN
24,55 LID_CLOSE#

68 CPU_UART2_TXD
68 CPU_UART2_RXD

24 EC_SM#
24 EC_SC#

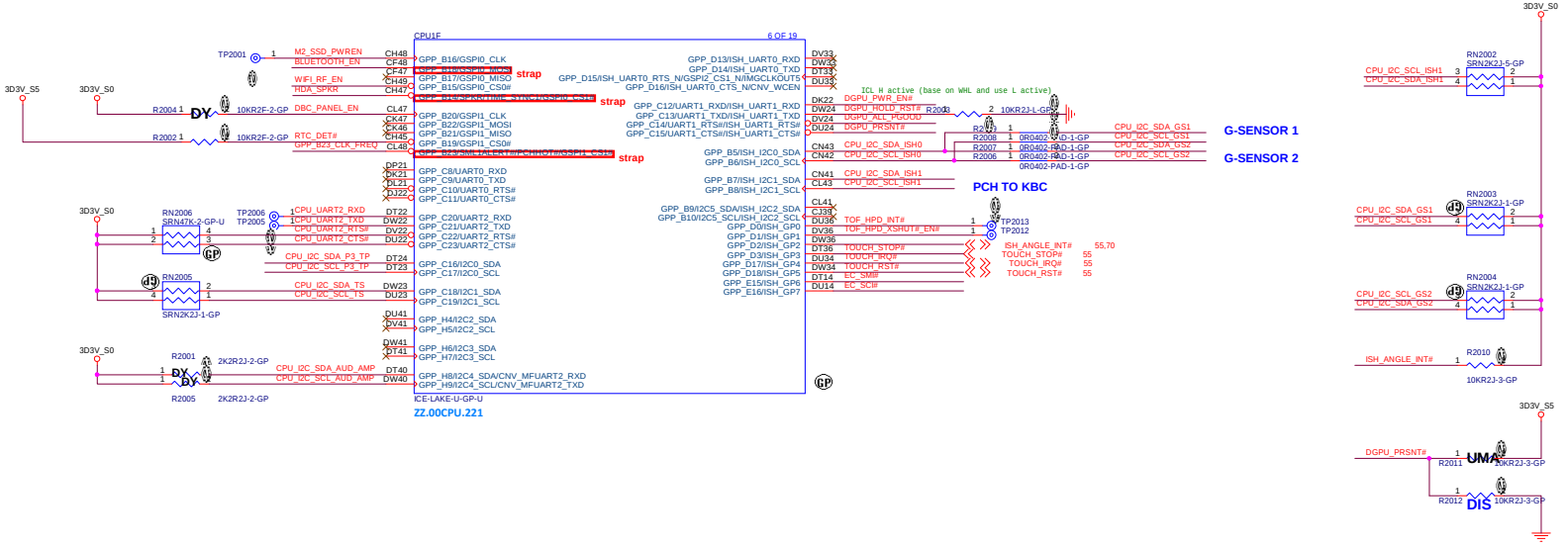
55 CPU_I2C_SCL_TS
55 CPU_I2C_SDA_TS

65 CPU_I2C_SCL_P3_TP
65 CPU_I2C_SDA_P3_TP

70 CPU_I2C_SDA_GS1
70 CPU_I2C_SCL_GS1
55 CPU_I2C_SDA_GS2
55 CPU_I2C_SCL_GS2

24 CPU_I2C_SDA_ISH1
24 CPU_I2C_SCL_ISH1

88 DGPU_PWR_EN#
76 DGPU_HOLD_RST#
88 DGPU_ALL_PGOOD



C550		
緯創資通	Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (UART/I2C/ISH)	
Size A2	Document Number C550-ICL	Rev SC
Date: Thursday, March 05, 2020	Sheet 20 of 106	

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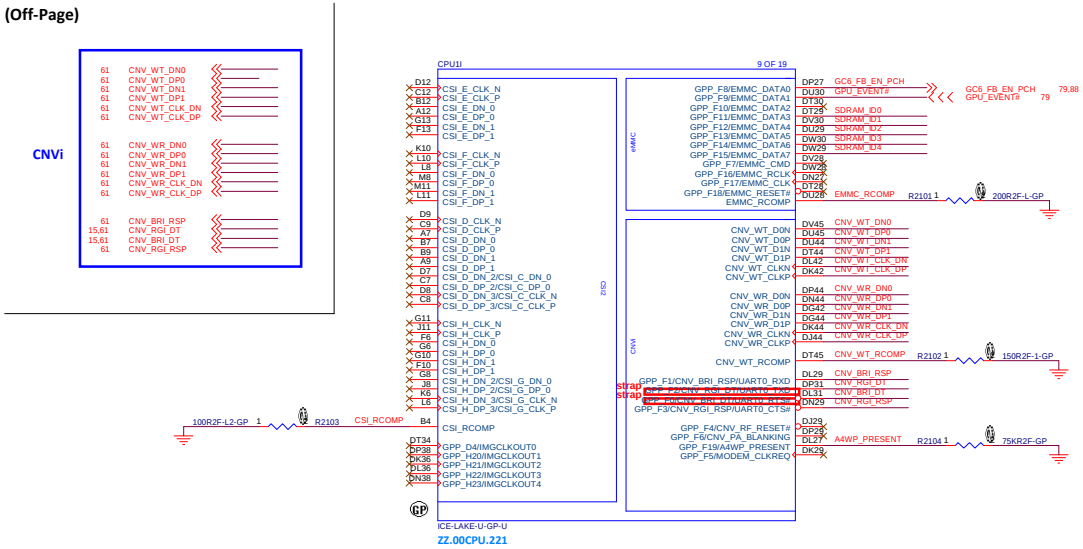
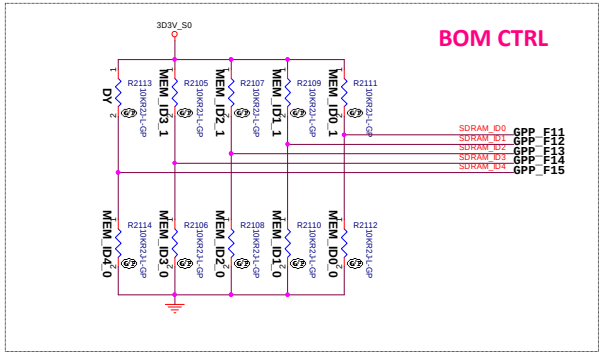




SVT Stage

SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Wisrton PN	Vendor	Density	Chanel		
0	0	0	0	0	SM30N76633	Samsung	8GB+8GB	A+B	SDP	SKU6,SKU12
0	0	0	0	1	SM30N76641	Micron	8GB+8GB	A+B	SDP	SKU14
0	0	0	1	0	SM30N76640	SK hynix	8GB+8GB	A+B	DDP	SKU13
0	0	0	1	1	SM30T12056	SMART	4GB+4GB	A+B	SDP	
0	0	1	0	0	SM30N76632	Samsung	4GB+4GB	A+B	SDP	SKU2
0	0	1	0	1	SM30N76570	Micron	4GB+4GB	A+B	SDP	SKU4,SKU5,SKU9,SKU11
0	0	1	1	0	SM30N76639	SK hynix	4GB+4GB	A+B	SDP	SKU3,SKU8,SKU10
0	0	1	1	1						
0	1	0	0	0	SM30N76633	Samsung	8GB+8GB	A+B	SDP	
0	1	0	0	1						
0	1	0	1	0	SM30N76640	SK hynix	8GB+8GB	A+B	DDP	
0	1	0	1	1	SM30N76632	Samsung	4GB	A	SDP	SKU1,SKU7
0	1	1	0	0	SM30U97726	HT Micron	4GB	A	SDP	
0	1	1	0	1	SM30N76570	Micron	4GB	A	SDP	
0	1	1	1	0	SM30N76639	SK hynix	4GB	A	SDP	
0	1	1	1	1	SM30N76640	SK hynix	8GB	A	DDP	

SDRAM_ID4 R2113 R2114	SDRAM_ID3 R2105 R2106	SDRAM_ID2 R2107 R2108	SDRAM_ID1 R2109 R2110	SDRAM_ID0 R2111 R2112	Memory ID	Wisrton PN	Vendor	Density
DY 10K	2.2M 2.2K	2M 2K	1.2M 1.2K	1M 1K	00000	SM30N76633	Samsung	8GB+8GB
DY 10K	2.2M 2.2K	2M 2K	1.2M 1.2K	1K 1M	00001	SM30N76641	Micron	8GB+8GB
DY 10K	2.2M 2.2K	2M 2K	1.2K 1.2M	1M 1K	00010	SM30N76640	SK hynix	8GB+8GB
DY 10K	2.2M 2.2K	2M 2K	1.2K 1.2M	1K 1M	00011	SM30T12056	SMART	4GB+4GB
DY 10K	2.2M 2.2K	2K 2M	1.2M 1.2K	1M 1K	00100	SM30N76632	Samsung	4GB+4GB
DY 10K	2.2M 2.2K	2K 2M	1.2M 1.2K	1K 1M	00101	SM30N76570	Micron	4GB+4GB
DY 10K	2.2M 2.2K	2K 2M	1.2K 1.2M	1M 1K	00110	SM30N76639	SK hynix	4GB+4GB
					00111			
DY 10K	2.2K 2.2M	2M 2K	1.2M 1.2K	1M 1K	01000	SM30N76633	Samsung	8GB+8GB
					01001			
DY 10K	2.2K 2.2M	2M 2K	1.2K 1.2M	1M 1K	01010	SM30N76640	SK hynix	8GB+8GB
DY 10K	2.2K 2.2M	2M 2K	1.2K 1.2M	1M 1K	01011	SM30N76632	Samsung	4GB
DY 10K	2.2K 2.2M	2K 2M	1.2M 1.2K	1M 1K	01100	SM30U97726	HT Micron	4GB
DY 10K	2.2K 2.2M	2K 2M	1.2M 1.2K	1K 1M	01101	SM30N76570	Micron	4GB
DY 10K	2.2K 2.2M	2K 2M	1.2K 1.2M	1M 1K	01110	SM30N76639	SK hynix	4GB
DY 10K	2.2K 2.2M	2K 2M	1.2K 1.2M	1K 1M	01111	SM30N76640	SK hynix	8GB

Value	Part Number
1K	63.10234.L0L
1M	63.10534.L1L
1.2K	63.12234.1DL
1.2M	63.12534.1DL
2K	63.20234.1DL
2M	63.20534.1DL
2.2K	63.22234.L0L
2.2M	63.22534.1DL
10K	63.10334.L0L
10M	63.10634.1DL

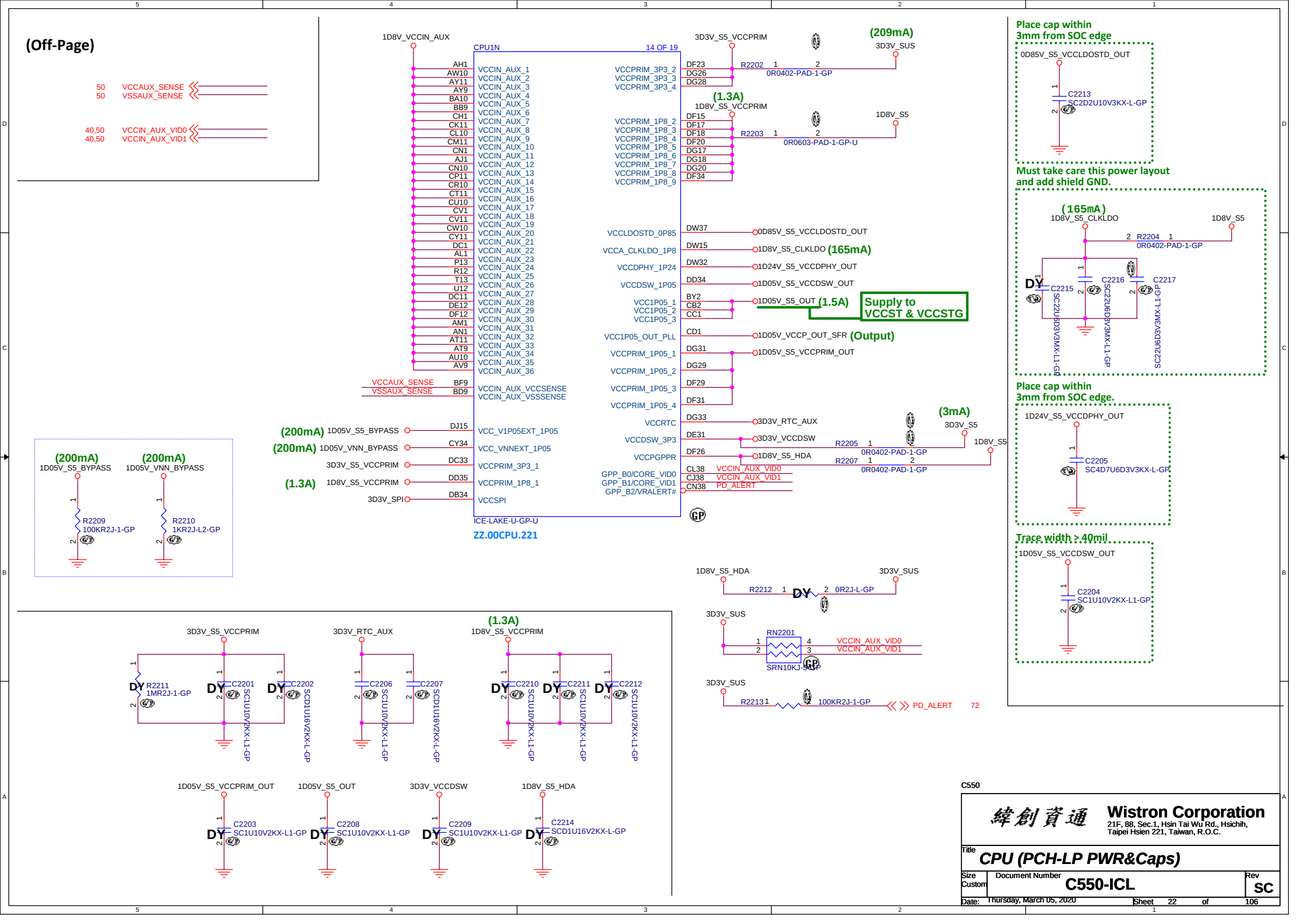
C550

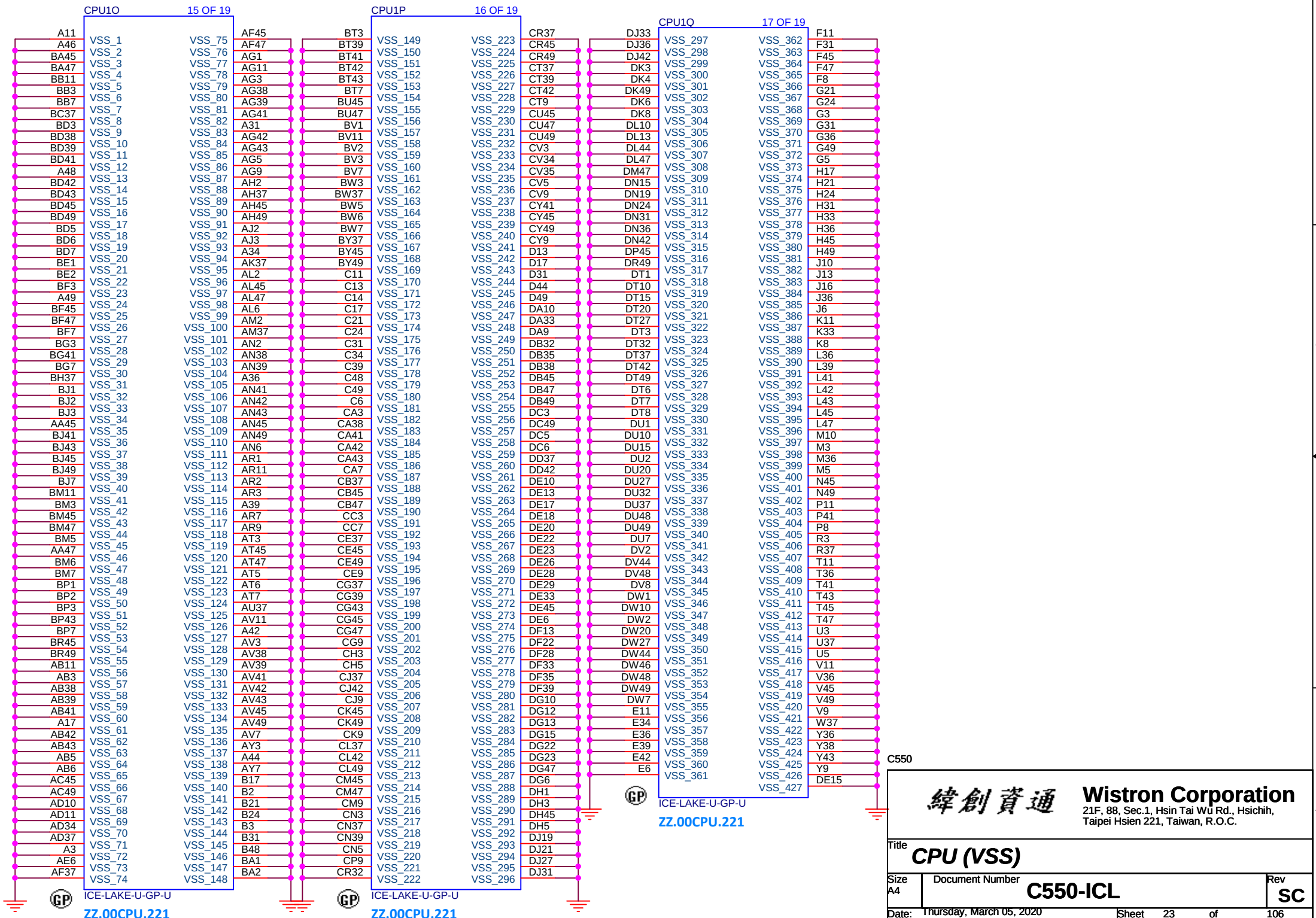
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVi)

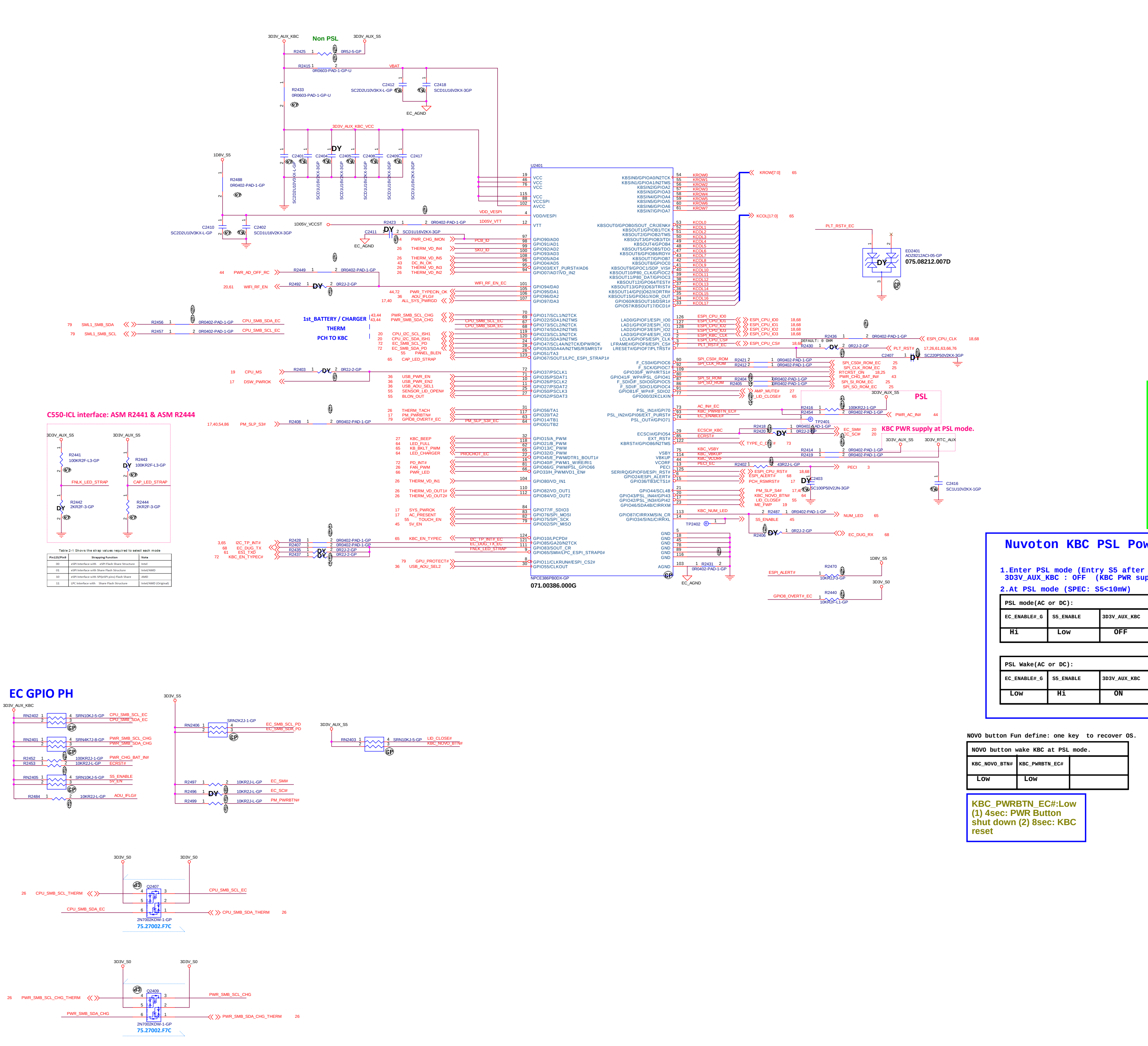
Size: A2 | Document Number: C550-ICL | Rev: SC

Date: Thursday, March 05, 2020 | Sheet 21 of 106


(Off-Page)
50 VCCAUX_SENSE
50 VSSAUX_SENSE
40,50 VCCIN_AUX_VID0
40,50 VCCIN_AUX_VID1
1D8V_VCCIN_AUX
CPU1N
14 OF 19
ICE-LAKE-U-GP-U
ZZ.00CPU.221
3D3V_S5_VCCPRIM
(209mA)
3D3V_SUS
R2202 0R0402-PAD-1-GP
(1.3A)
1D8V_S5_VCCPRIM
1D8V_S5
R2203 0R0603-PAD-1-GP-U
0D85V_S5_VCCLDOSTD_OUT
1D8V_S5_CLKLDO (165mA)
1D24V_S5_VCCDPHY_OUT
1D05V_S5_OUT (1.5A)
Supply to VCCST & VCCSTG
1D05V_VCCP_OUT_SFR (Output)
1D05V_S5_VCCPRIM_OUT
3D3V_RTC_AUX
3D3V_VCCDSW
1D8V_S5_HDA
(3mA)
3D3V_S5
R2205 0R0402-PAD-1-GP
R2207 0R0402-PAD-1-GP
VCCIN_AUX_VID0
VCCIN_AUX_VID1
PD_ALERT
1D05V_S5_BYPASS (200mA)
1D05V_VNN_BYPASS (200mA)
R2209 100KR2J-1-GP
R2210 1KR2J-L2-GP
3D3V_S5_VCCPRIM
1D8V_S5_VCCPRIM (1.3A)
3D3V_SPI
VCCSPI
VCCAUX_SENSE
VSSAUX_SENSE
VCCIN_AUX_VCCSENSE
VCCIN_AUX_VSSSENSE
Place cap within 3mm from SOC edge
Must take care this power layout and add shield GND.
Place cap within 3mm from SOC edge.
Trace width > 40mil
1D05V_S5_VCCDSW_OUT
1D8V_S5_HDA
3D3V_SUS
R2212 0R2J-L-GP
RN2201
SRN10KJ-3-GP
R2213 100KR2J-1-GP
PD_ALERT 72
3D3V_S5_VCCPRIM
3D3V_RTC_AUX
1D8V_S5_VCCPRIM (1.3A)
1D05V_S5_VCCPRIM_OUT
1D05V_S5_OUT
3D3V_VCCDSW
1D8V_S5_HDA
C550
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PCH-LP PWR&Caps)
Size Custom
Document Number C550-ICL
Rev SC
Date: Thursday, March 05, 2020
Sheet 22 of 106


CPU1O
15 OF 19
A11 A46 BA45 BA47 BB11 BB3 BB7 BC37 BD3 BD38 BD39 BD41 A48 BD42 BD43 BD45 BD49 BD5 BD6 BD7 BE1 BE2 BF3 A49 BF45 BF47 BF7 BG3 BG41 BG7 BH37 BJ1 BJ2 BJ3 AA45 BJ41 BJ43 BJ45 BJ49 BJ7 BM11 BM3 BM45 BM47 BM5 AA47 BM6 BM7 BP1 BP2 BP3 BP43 BP7 BR45 BR49 AB11 AB3 AB38 AB39 AB41 A17 AB42 AB43 AB5 AB6 AC45 AC49 AD10 AD11 AD34 AD37 A3 AE6 AF37
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74
VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128 VSS_129 VSS_130 VSS_131 VSS_132 VSS_133 VSS_134 VSS_135 VSS_136 VSS_137 VSS_138 VSS_139 VSS_140 VSS_141 VSS_142 VSS_143 VSS_144 VSS_145 VSS_146 VSS_147 VSS_148
AF45 AF47 AG1 AG11 AG3 AG38 AG39 AG41 A31 AG42 AG43 AG5 AG9 AH2 AH37 AH45 AH49 AJ2 AJ3 A34 AK37 AL2 AL45 AL47 AL6 AM2 AM37 AN2 AN38 AN39 A36 AN41 AN42 AN43 AN45 AN49 AN6 AR1 AR11 AR2 AR3 A39 AR7 AR9 AT3 AT45 AT47 AT5 AT6 AT7 AU37 AV11 A42 AV3 AV38 AV39 AV41 AV42 AV43 AV45 AV49 AV7 AY3 A44 AY7 B17 B2 B21 B24 B3 B31 B48 BA1 BA2
GP
ICE-LAKE-U-GP-U
ZZ.00CPU.221
CPU1P
16 OF 19
BT3 BT39 BT41 BT42 BT43 BT7 BU45 BU47 BV1 BV11 BV2 BV3 BV7 BW3 BW37 BW5 BW6 BW7 BY37 BY45 BY49 C11 C13 C14 C17 C21 C24 C31 C34 C39 C48 C49 C6 CA3 CA38 CA41 CA42 CA43 CA7 CB37 CB45 CB47 CC3 CC7 CE37 CE45 CE49 CE9 CG37 CG39 CG43 CG45 CG47 CG9 CH3 CH5 CJ37 CJ42 CJ9 CK45 CK49 CK9 CL37 CL42 CL49 CM45 CM47 CM9 CN3 CN37 CN39 CN5 CP9 CR32
VSS_149 VSS_150 VSS_151 VSS_152 VSS_153 VSS_154 VSS_155 VSS_156 VSS_157 VSS_158 VSS_159 VSS_160 VSS_161 VSS_162 VSS_163 VSS_164 VSS_165 VSS_166 VSS_167 VSS_168 VSS_169 VSS_170 VSS_171 VSS_172 VSS_173 VSS_174 VSS_175 VSS_176 VSS_177 VSS_178 VSS_179 VSS_180 VSS_181 VSS_182 VSS_183 VSS_184 VSS_185 VSS_186 VSS_187 VSS_188 VSS_189 VSS_190 VSS_191 VSS_192 VSS_193 VSS_194 VSS_195 VSS_196 VSS_197 VSS_198 VSS_199 VSS_200 VSS_201 VSS_202 VSS_203 VSS_204 VSS_205 VSS_206 VSS_207 VSS_208 VSS_209 VSS_210 VSS_211 VSS_212 VSS_213 VSS_214 VSS_215 VSS_216 VSS_217 VSS_218 VSS_219 VSS_220 VSS_221 VSS_222
VSS_223 VSS_224 VSS_225 VSS_226 VSS_227 VSS_228 VSS_229 VSS_230 VSS_231 VSS_232 VSS_233 VSS_234 VSS_235 VSS_236 VSS_237 VSS_238 VSS_239 VSS_240 VSS_241 VSS_242 VSS_243 VSS_244 VSS_245 VSS_246 VSS_247 VSS_248 VSS_249 VSS_250 VSS_251 VSS_252 VSS_253 VSS_254 VSS_255 VSS_256 VSS_257 VSS_258 VSS_259 VSS_260 VSS_261 VSS_262 VSS_263 VSS_264 VSS_265 VSS_266 VSS_267 VSS_268 VSS_269 VSS_270 VSS_271 VSS_272 VSS_273 VSS_274 VSS_275 VSS_276 VSS_277 VSS_278 VSS_279 VSS_280 VSS_281 VSS_282 VSS_283 VSS_284 VSS_285 VSS_286 VSS_287 VSS_288 VSS_289 VSS_290 VSS_291 VSS_292 VSS_293 VSS_294 VSS_295 VSS_296
CR37 CR45 CR49 CT37 CT39 CT42 CT9 CU45 CU47 CU49 CV3 CV34 CV35 CV5 CV9 CY41 CY45 CY49 CY9 D13 D17 D31 D44 D49 DA10 DA33 DA9 DB32 DB35 DB38 DB45 DB47 DB49 DC3 DC49 DC5 DC6 DD37 DD42 DE10 DE13 DE17 DE18 DE20 DE22 DE23 DE26 DE28 DE29 DE33 DE45 DE6 DF13 DF22 DF28 DF33 DF35 DF39 DG10 DG12 DG13 DG15 DG22 DG23 DG47 DG6 DH1 DH3 DH45 DH5 DJ19 DJ21 DJ27 DJ31
GP
ICE-LAKE-U-GP-U
ZZ.00CPU.221
CPU1Q
17 OF 19
DJ33 DJ36 DJ42 DK3 DK4 DK49 DK6 DK8 DL10 DL13 DL44 DL47 DM47 DN15 DN19 DN24 DN31 DN36 DN42 DP45 DR49 DT1 DT10 DT15 DT20 DT27 DT3 DT32 DT37 DT42 DT49 DT6 DT7 DT8 DU1 DU10 DU15 DU2 DU20 DU27 DU32 DU37 DU48 DU49 DU7 DV2 DV44 DV48 DV8 DW1 DW10 DW2 DW20 DW27 DW44 DW46 DW48 DW49 DW7 E11 E34 E36 E39 E42 E6
VSS_297 VSS_298 VSS_299 VSS_300 VSS_301 VSS_302 VSS_303 VSS_304 VSS_305 VSS_306 VSS_307 VSS_308 VSS_309 VSS_310 VSS_311 VSS_312 VSS_313 VSS_314 VSS_315 VSS_316 VSS_317 VSS_318 VSS_319 VSS_320 VSS_321 VSS_322 VSS_323 VSS_324 VSS_325 VSS_326 VSS_327 VSS_328 VSS_329 VSS_330 VSS_331 VSS_332 VSS_333 VSS_334 VSS_335 VSS_336 VSS_337 VSS_338 VSS_339 VSS_340 VSS_341 VSS_342 VSS_343 VSS_344 VSS_345 VSS_346 VSS_347 VSS_348 VSS_349 VSS_350 VSS_351 VSS_352 VSS_353 VSS_354 VSS_355 VSS_356 VSS_357 VSS_358 VSS_359 VSS_360 VSS_361
VSS_362 VSS_363 VSS_364 VSS_365 VSS_366 VSS_367 VSS_368 VSS_369 VSS_370 VSS_371 VSS_372 VSS_373 VSS_374 VSS_375 VSS_376 VSS_377 VSS_378 VSS_379 VSS_380 VSS_381 VSS_382 VSS_383 VSS_384 VSS_385 VSS_386 VSS_387 VSS_388 VSS_389 VSS_390 VSS_391 VSS_392 VSS_393 VSS_394 VSS_395 VSS_396 VSS_397 VSS_398 VSS_399 VSS_400 VSS_401 VSS_402 VSS_403 VSS_404 VSS_405 VSS_406 VSS_407 VSS_408 VSS_409 VSS_410 VSS_411 VSS_412 VSS_413 VSS_414 VSS_415 VSS_416 VSS_417 VSS_418 VSS_419 VSS_420 VSS_421 VSS_422 VSS_423 VSS_424 VSS_425 VSS_426 VSS_427
F11 F31 F45 F47 F8 G21 G24 G3 G31 G36 G49 G5 H17 H21 H24 H31 H33 H36 H45 H49 J10 J13 J16 J36 J6 K11 K33 K8 L36 L39 L41 L42 L43 L45 L47 M10 M3 M36 M5 N45 N49 P11 P41 P8 R3 R37 T11 T36 T41 T43 T45 T47 U3 U37 U5 V11 V36 V45 V49 V9 W37 Y36 Y38 Y43 Y9 DE15
GP
ICE-LAKE-U-GP-U
ZZ.00CPU.221
C550
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (VSS)
Size A4
Document Number
C550-ICL
Rev SC
Date: Thursday, March 05, 2020
Sheet 23 of 106

SSID = KBC



Model_ID_BOM Ctrl

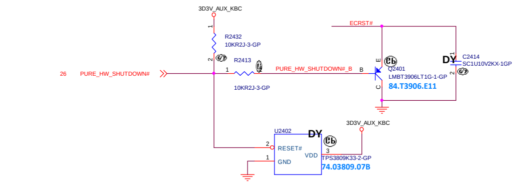
PCB VERSION A/D(PIN100)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LC55-14C	100.0K	10.0K 64.10025.L0L	3.0V
LC55-15C	100.0K	20.0K 64.20025.L0L	2.75V
NA	100.0K	33.0K 64.33025.L0L	2.48V
NA	100.0K	47.0K 64.47025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-1M	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

Prevent BIOS data loss solution

Q2401 84.03906.G11->84.T3906.E11(main)



Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

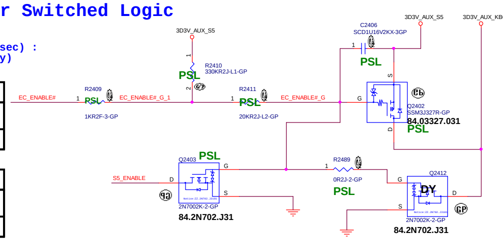
2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):

EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):

EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON



NOVO button Fun define: one key to recover OS.

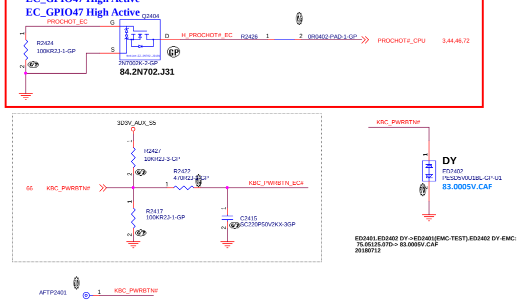
NOVO button wake KBC at PSL mode.

KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low (1) 4sec: PWR Button shut down (2) 8sec: KBC reset

EC_GPIO47 High Active

EC_GPIO47 High Active



C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ECIO (NUVOTON NPCE386)

Size: A1 | Document Number: C550-ICL | Rev: SC

Date: Thursday, March 05, 2020 | Sheet 24 of 106

SSID = Flash.ROM

SPI ROM

15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU
18 SPI_CLK_CPU
18 SPI_CS_CPU_N0
15,18 SPI_SI_CPU
18 SPI_SO_CPU

SPI_CLK_CPU R2517 1 10R0D9R2F-GP SPI_CLK_EC
SPI_SO_CPU R2518 1 10R0D9R2F-GP SPI_SO_EC
SPI_SI_CPU R2519 1 10R0D9R2F-GP SPI_SI_EC
SPI_WP_CPU R2520 1 10R0D9R2F-GP SPI_WP_EC
SPI_HOLD_CPU R2521 1 10R0D9R2F-GP SPI_HOLD_EC
SPI_CS_CPU_N0 R2516 1 10R0D9R2F-GP SPI_CS_EC

3D3V_SPI
R2501 1 10KR2J-3-GP SPI_SO_EC
R2502 1 10KR2J-3-GP SPI_CS_EC
R2503 1 10KR2J-3-GP SPI_WP_EC
R2504 1 10KR2J-3-GP SPI_HOLD_EC

DY
C2501 SC10U25V5KX-GP
C2503 SC1U10V2KX-1GP

3D3V_SPI
C2502 SC1U10V2KX-1GP

SPI_CS_EC
SPI_SO_EC
SPI_WP_EC

SHARE_ROM
R2539 1 0R2J-2-GP SPI_CS0#_ROM_EC
SPI_WP_EC 1 4 SRN0J-6-GP SPI_WP_ROM_EC
SPI_SO_EC 2 3 SPI_SO_ROM_EC
SHARE_ROM
RN2502

BIOS1 16MByte
CS# VCC
SO/SIO1 SIO3
SIO2 SCLK
GND SI/SIO0
MX25L12872FM2I-10G-GP
072.25128.0D61
VCC接3.3V

SPI_HOLD_EC
SPI_CLK_EC
SPI_SI_EC
SHARE_ROM
R2542 1 0R2J-2-GP SPI_HOLD_ROM_EC
RN2505 1 4 SRN0J-6-GP SPI_CLK_ROM_EC
2 3 SPI_SI_ROM_EC
SHARE_ROM

BOM CTRL

BOM CTRL

TABLE of SPI BIOS1		
VENDOR	P/N	Wistron P/N
MXIC	MX25L12872FM2I-10G	072.25128.0D61
WINBOND	W25Q128JVSIQ	072.25128.0B71

3D3V_SPI
3D3V_S5
R2505 1 2 0R0402-PAD-1-GP
C2509 SCD1U16V2KX-3GP
C2506 SCD1U25V2KX-L-GP

128k byte for FEROM

3D3V_SPI
BIOS2
VCC CS#
HOLD# SO/SIO1
SCLK WP#
SI/SIO0 GND
DY
MX25L1006EMI-10G-GP
72.25106.001

SPI_HOLD_ROM_EC
SPI_CLK_ROM_N
SPI_SI_ROM_N
SPI_CS0#_ROM_N
SPI_SO_ROM_N
SPI_WP_ROM_EC

24 SPI_CLK_ROM_EC
24 SPI_SI_ROM_EC
RN2503
SRN33J-5-GP-U
NON_SHARE

RN2504
SRN33J-5-GP-U
NON_SHARE
SPI_CS0#_ROM_EC 24
SPI_SO_ROM_EC 24

3D3V_SPI
SPI_HOLD_ROM_EC
SPI_WP_ROM_EC
RN2506
SRN10KJ-5-GP
NON_SHARE

FEROM

TABLE of SPI BIOS2		
VENDOR	P/N	Wistron P/N
MACRONIX	MX25L1006EMI-10G	72.25106.001
GIGADEVICE	GD25D10BTIGR	072.25D10.0A0D
WINBOND	W25X10CLSNIG	72.02510.001

SSID = RBAT

18,24 RTCRST_ON
20 RTC_DET#

3D3V_RTCVCC_CONN
3D3V_AUX_S5
3D3V_RTC_AUX
D2502 LBAT54CLT1G-1-GP
075.00054.0B7D
C2505 SCD47U25V3KX-1GP
RTC_PWR
R2507 1KR2J-1-GP
R2509 10MR2J-L-GP
RTC_DET#
Q2505 PJA7002H-R1-00001-2-GP
084.07002.M010

3D3V_RTC_AUX
R2510 1 2 0R0603-PAD-1-GP-U
U2501 GND VIN DY VOUT
AP2138N-1D5TRG1-GP
1st = 74.02138.03B
C2511 SC1U10V2KX-1GP
C2512 SC1U10V2KX-1GP
VBAT_SB_N
R2511 1KR2F-L1-GP
1D5V_VDDBT_RTC
C2513 SC1U10V2KX-1GP
G2501 GAP-OPEN
R25121 DY 20R2J-2-GP
Q2511 2N7002K-2-GP
RTCRST_ON
Q2511_S
R2513 100R2J-L-GP
1st = 84.2N702.J31
2nd = 84.2N702.031

C550

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title FLASH/RTC
Size A2 Document Number C550-ICL Rev SC
Date: Thursday, March 05, 2020 Sheet 25 of 106

Main Func = Thermal Sensor

Close to Thermal sensor

@CPU — Close to CPU chips
@Ambient — Close to KBC chips
@SSD — Close to SSD chips
@Charger — Close to Charger chips
@GPU — Close to GPU

Close to Charger
Ch2 — 84.T3904.H11 — Close to thermal sensor
Close to GPU
Ch1 — 84.T3904.H11 — Close to thermal sensor

Close to DIMM — 74.07718.089
Close to SSD Bottom side — 74.07718.089

Software Control
Hardware Control

ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

NCT7718W Table:

R2627 \ R2639 R2635 \ R2640	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

FAN CONN

FAN1 — ACES-CON4-17-DP-U2 — 20.F1621.004

Q2602 — 2N7002K-2-GP — 84.2N702.J31
Q2603 — LBAW56LT1G-GP — 83.00056.Y11

Layout Note:Place Close to PCH1.
To 3V/ 5V Power IC S5 ENABLE
Q2601 — MMBT2222ALT1G-GP — 84.02222.X11

PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

5V *100K/(100K+40K) = 3.57V

Q2603 — 2N7002K-2-GP — 84.2N702.J31
U2601 — LMV331IDCKRG4-GP — 74.09331.A2F

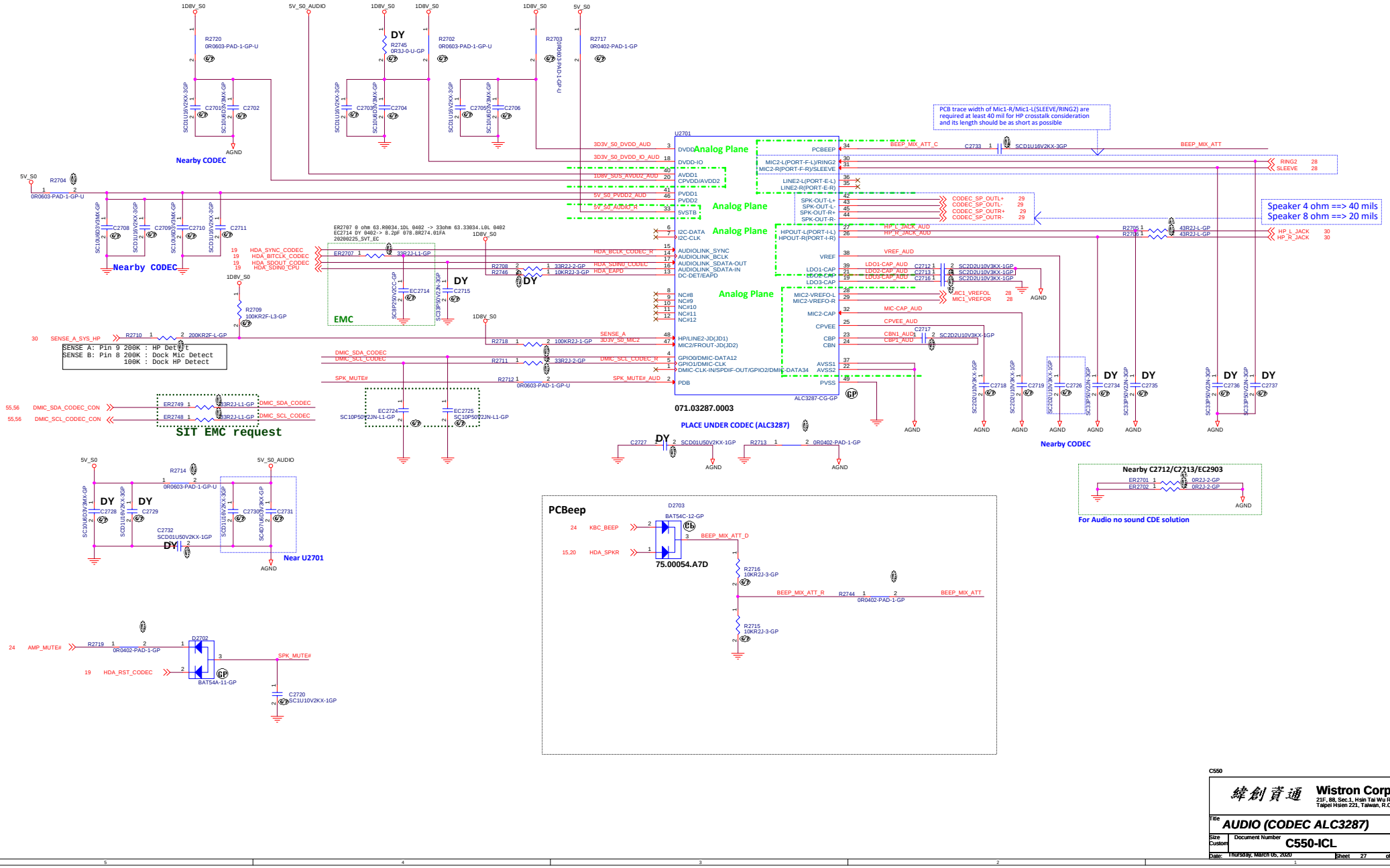
TABLE:

ID	Target	Function
RT2601	PU5101	1D2V_S3
RT2602	PU4801	1V_VCCGT
RT2603	PQ5201	1D05V_SUS
RT2604	PU4701	1V_CPU_CORE
RT2605	PQ4505	5V_S5
RT2606	PQ4506	3D3V_S5
RT2607	PU4404	Charger-Buck
RT2608	PU4406	Charger-Boost

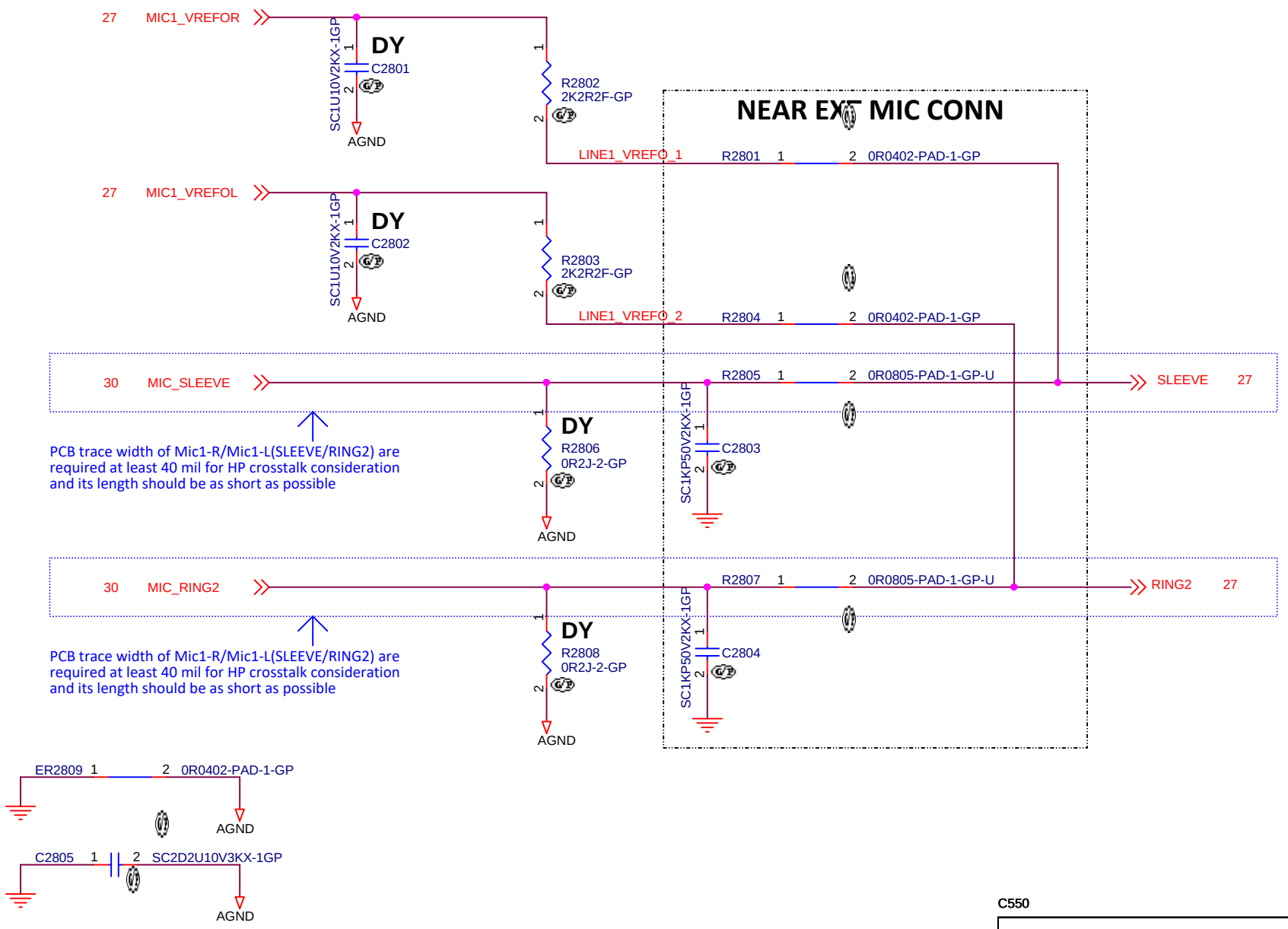
C550

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (THERMAL/FAN)
Size: A1 | Document Number: C550-ICL | Rev: SC
Date: Thursday, March 06, 2008 | Sheet 28 of 35



C550	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO (CODEC ALC3287)
Size: Custom	Document Number: C550-ICL
Rev	SC
Date: Thursday, March 05, 2020	Sheet 27 of 106



C550

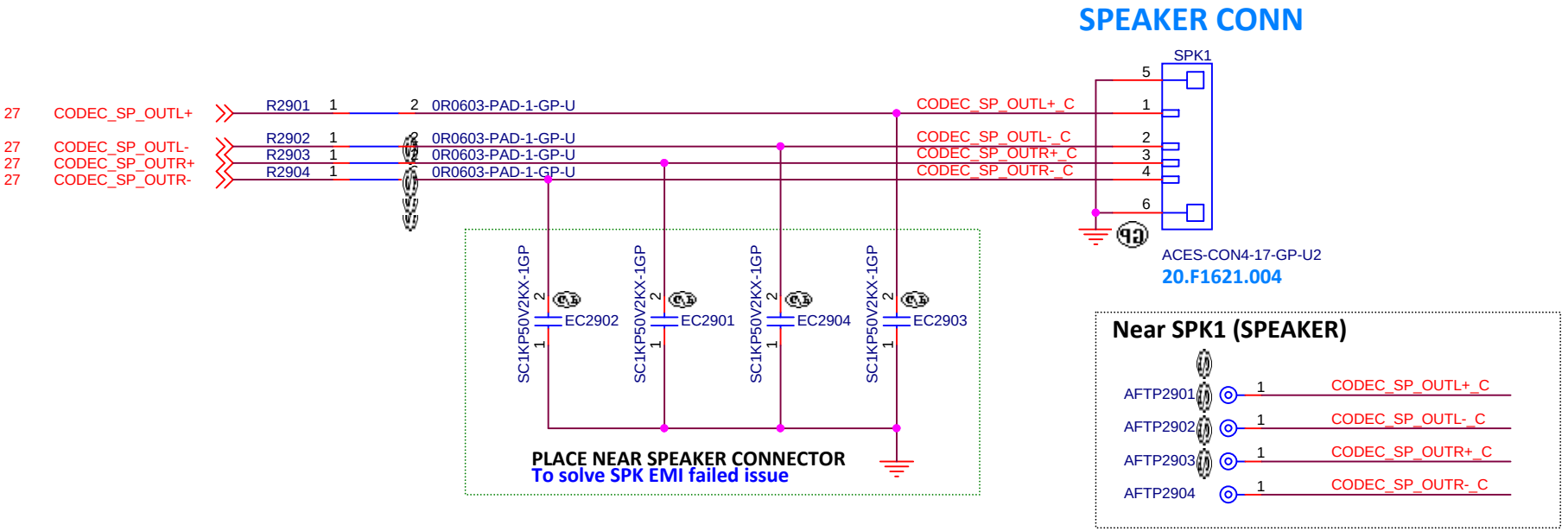
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (MIC I/F)***

Size	Document Number	Rev
A4	C550-ICL	SC

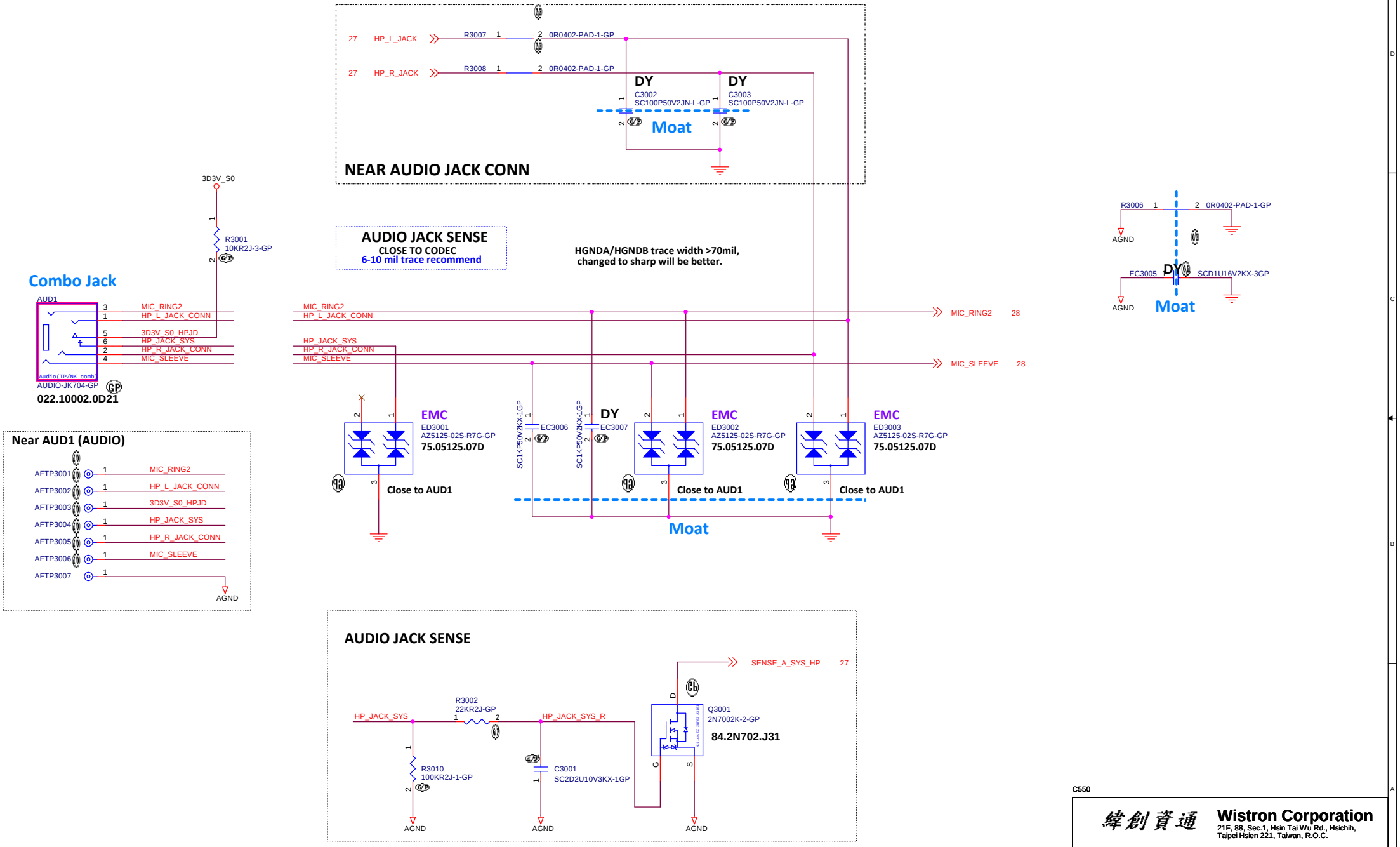
Date: Thursday, March 05, 2020 Sheet 28 of 106

Main Func = AUDIO



C550

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO (SPEAKER)*		
Size: A4	Document Number: C550-ICL	Rev: SC
Date: Thursday, March 05, 2020	Sheet 29 of 106	



C550

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AUDIO (AUDIO JACK)***	
Size A3	Document Number **C550-ICL**	Rev **SC**
Date: Thursday, March 05, 2020	Sheet 30 of 106	

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C550

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Taipei Hsien 221, Taiwan, R.O.C.

Title ***LAN (RSVD)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

Date: Thursday, March 05, 2020 Sheet 31 of 106

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C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***LAN (RSVD)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

Date: Thursday, March 05, 2020 Sheet 32 of 106

(Blanking)

C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***CARDREADER (SDIO/SD CONN)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

Date: Thursday, March 05, 2020 Sheet 33 of 106

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C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

Date: Thursday, March 05, 2020 Sheet 34 of 106

(Blanking)

C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

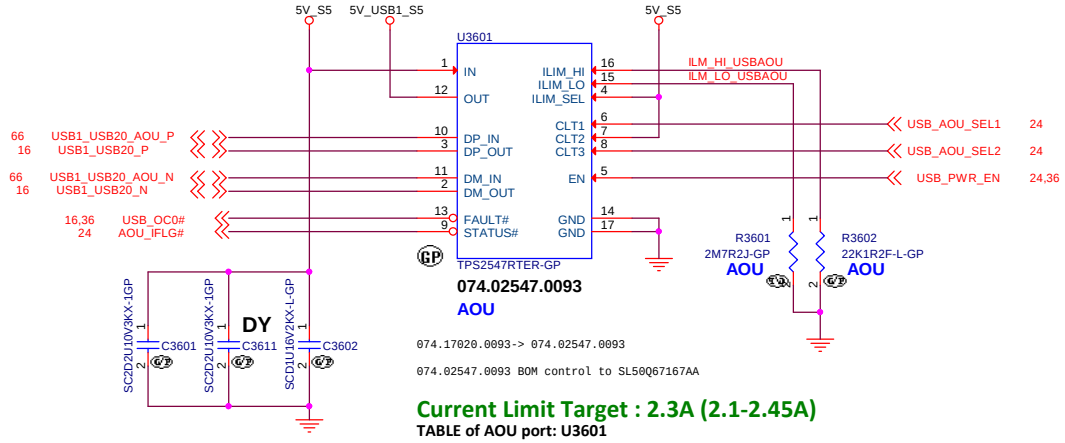
Title: ***USB (CHARGER/SWITCH)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

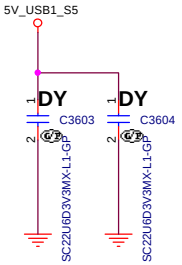
Date: Thursday, March 05, 2020 Sheet 35 of 106

Main Func = USB Charger

For USB3.0 System Port1 (For AOU)



Layout Note: Close 5V_USB1_S5

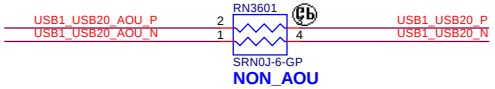


Current Limit Target : 2.3A (2.1-2.45A)

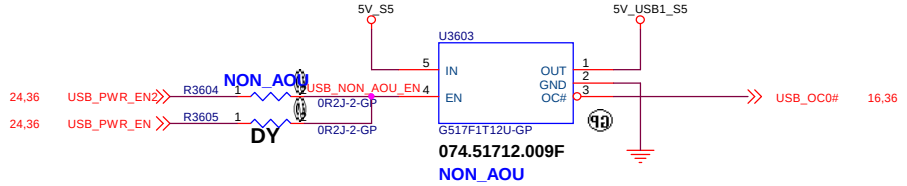
TABLE of AOU port: U3601

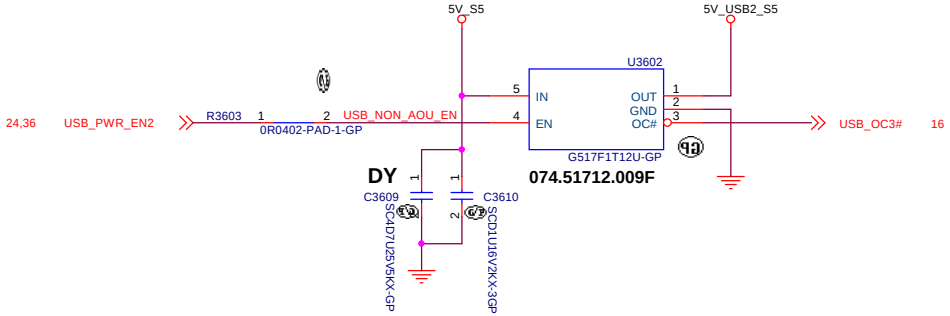
	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER	SL50Q67167AA
2nd	TI	TPS2547RTER	074.02547.0093

SN1702001RTER is not equivalent device of TPS2546RTER

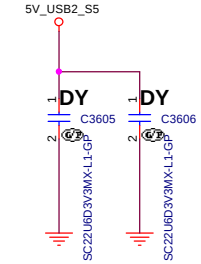


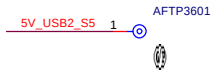
For USB3.0 System Port2





Layout Note: Close 5V_USB2_S5





C550

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB(USB Charger)***	
Size A3	Document Number **C550-ICL**	Rev **SC**
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C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

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C550

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)(USB Redriver/Hub)***

Size	Document Number	Rev
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C550

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SEQUENCE (RSVD)***

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17,24,54,86 PM_SLP_S3#
17,53 PM_SLP_SUS#
17 VCCST_OVERRIDE
17,24 ALL_SYS_PWRGD
22,50 VCCIN_AUX_VID0
22,50 VCCIN_AUX_VID1
17 PCH_PWROK
17 C10_PWR_GATE#
46 PWR_VCORE_VR_READY
46 PWR_VCORE_VR_EN
51 PWR_VDDQ_PG

RUN Power 5V_S0/3D3V_S0

5V_S5 → U4007 VBIAS; C4013 DY, C4014 SC1U10V2KX-L1-GP
3D3V_S5 → C4017 DY, C4018 SC1U10V2KX-L1-GP, C4021 DY
PM_SLP_S3# → R4008 0R0402-PAD-1-GP → 3V_5V_S0_EN
SW_5V_S0_CT, SW_3D3V_S0_CT → C4015 DY SC470P50V2KX-L-GP, C4016 DY SC1KP50V2KX-L-GP
U4007 G2898KD1U-GP
5V_S0 (2.5A)
3D3V_S0 (2A)
C4019 SC1U10V2KX-L1-GP, C4020 SC1U10V2KX-L1-GP
074.02898.0093
2nd = 074.22976.0091

1D8V_S0 2018/12/21 add

1D8V_S5 → Q4004 PJA3413-1-GP → 1D8V_S0
150mA
C4044 SCD1U16V2KX-L-GP, R4034 10KR2J-3-GP, C4045 SC1U10V2KX-1GP, R4035 20KR2J-L2-GP
1D8V_EN_R#
common part
084.03413.0031
C4046 SCD1U25V2KX-GP
R4059 0R0402-PAD-1-GP → 1D8V_PM_SLP_S3#
Q4003 2N7002K-2-GP
1D8V_EN#
84.2N702.J31

Layout Note:Close to CPU Side.

1D2V_S3 → 1D2V_VCCPLL_OC

R4404 0R0402-PAD-1-GP
1D2V_VCCPLL_OC_FIP (150mA)
C10_PWR_GATE# → R4012 0R2J-L-GP → 2VCCPLL_OC_GATE#
U4011 APE8939GN3-GP 074.08939.0093
R4013 0R0603-PAD-1-GP-U
C4004 SC1U10V2KX-L-GP, C4005 SC1U10V2KX-L-GP, C4006 SC10U6D3V3MX-L-GP

3D3V_S5 → 3D3V_SUS

R4099 0R0603-PAD-1-GP-U
3D3V_SUS_FIP (1A)
PM_SLP_SUS# → R4010 0R2J-L-GP → 3D3V_SUS_EN
U4009 APE8939GN3-GP 074.08939.0093
R4011 D01R3F-L-GP
C4029 SC1U10V2KX-L-GP, C4030 SC1U10V2KX-L-GP, C4031 SC1U10V2KX-L-GP, C4032 SC10U6D3V3MX-L-GP

VCORE_PWRGD → R4050 0R0402-PAD-1-GP → PWR_VCORE_VR_READY

TOP

5V_S5 → AFTP4001, AFTP4002
5V_S0 → AFTP4003
3D3V_S5 → AFTP4004, AFTP4005, AFTP4006, AFTP4007
3D3V_S0 → AFTP4008, AFTP4009

1D05V_S5 → 1D05V_VCCSTG

17,24,51 PM_SLP_S4# → C10_PWR_GATE# → U4004 74LVC1G08GW-1-GP 73.01G08.L04
R4003 0R0402-PAD-1-GP
VCCSTG_EN → C4007 SC1U10V2KX-L-GP
R4026 1KR2J-3-GP → VCCSTG_EN_R → C4008 SCD1U25V2KX-3GP
6A/Rds(on):4.5mOhm/Tr:7~20us
U4005 APE8939GN3-GP 074.08939.0093
1D05V_VCCSTG_FIP (120mA)
R4028 0R0402-PAD-1-GP
C4009 SC1U10V2KX-L-GP, C4010 SC1U10V2KX-L-GP

1D8V_S5 → 1D8V_PCH_C10_FIP → 1D8V_PCH_C10

6A/Rds(on):4.5mOhm/Tr:7~20us
R4014 0R3J-0-U-GP, R4027 0R0603-PAD-1-GP-U
C10_PWR_GATE# → R4015 0R2J-L-GP → 1D8V_GATE#
PM_SLP_S3# → R4019 0R0402-PAD-1-GP
U4003 APE8939GN3-GP 074.08939.0093
C4037 SC1U10V2KX-L-GP, C4038 SC1U10V2KX-L-GP, C4039 SC1U10V2KX-L-GP, C4047 SC1U10V2KX-L-GP

1D05V_S5 → 1D05V_VCCST_FIP

6A/Rds(on):4.5mOhm/Tr:7~20us (700mA)
U4002 APE8939GN3-GP 074.08939.0093
R4026 0R0603-PAD-1-GP-U
(610mA)
VCCIN_AUX_VID0 → D4003 BAT54C-12-GP 75.00054.A7D
VCCIN_AUX_VID1 → D4003 BAT54C-12-GP 75.00054.A7D
PM_SLP_S3# → D4004 BAT54C-12-GP 75.00054.A7D
VCCST_OVERRIDE_3D3V → D4004 BAT54C-12-GP 75.00054.A7D
C4002 SC1U10V2KX-L-GP, C4003 SC1U10V2KX-L-GP

VCORE_PWRGD / ALL_SYS_PWRGD → U4001 SN74AUP1G08DCKR-GP 73.01G08.DHH

R4001 0R0402-PAD-1-GP
PCH_PWROK → R4002 10KR2F-2-GP → 3D3V_S0
C4001 SCD1U16V2KX-L-GP

PM_SLP_S3# / PWR_VDDQ_PG → ALL_SYS_PWRGD

D4002 RB551V30-GP 83.R5003.H8H
R4018 1KR2J-1-GP (3D3V_S0)
R4016 0R0402-PAD-1-GP
R4017 0R0402-PAD-1-GP → PWR_VCORE_VR_EN

VCCST_OVERRIDE

3D3V_SUS → R4005 100KR2J-1-GP → VCCST_OVERRIDE_Q1
Q4002 LSI1012LT1G-GP 084.01012.0031
Q4001 2N7002K-2-GP 84.2N702.J31
R4006 100KR2J-1-GP → VCCST_OVERRIDE_3D3V

C550

Wistron Corporation
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Title: SEQUENCE (POWER PLANE EN)
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C550

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SEQUENCE (RSVD)***

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C550

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)*

Size	Document Number	Rev
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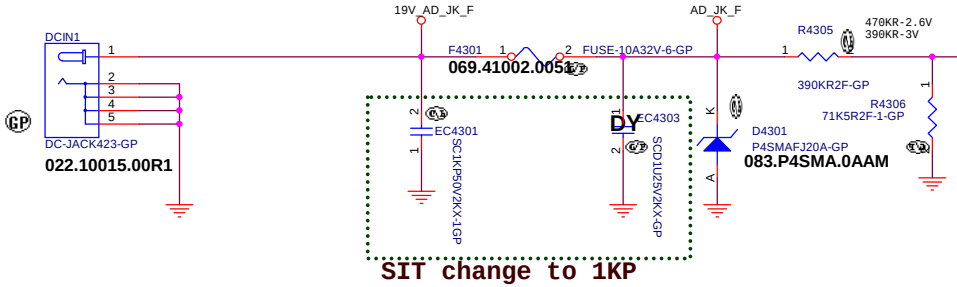
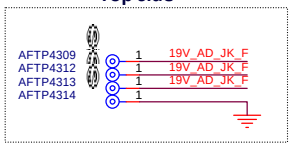
Total MLCC capacitance at DCIN connector
is smaller than 1000pf to avoid LC resonance

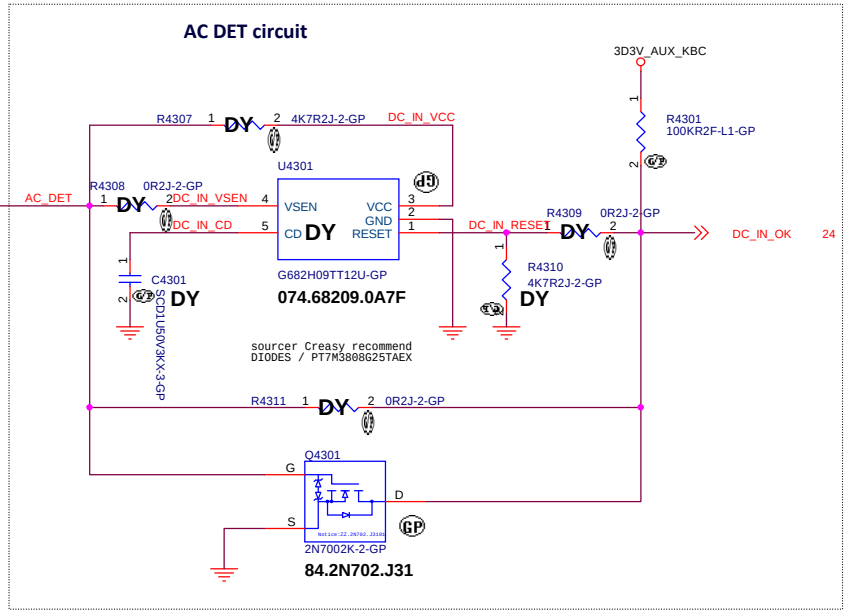
DCIN CONN



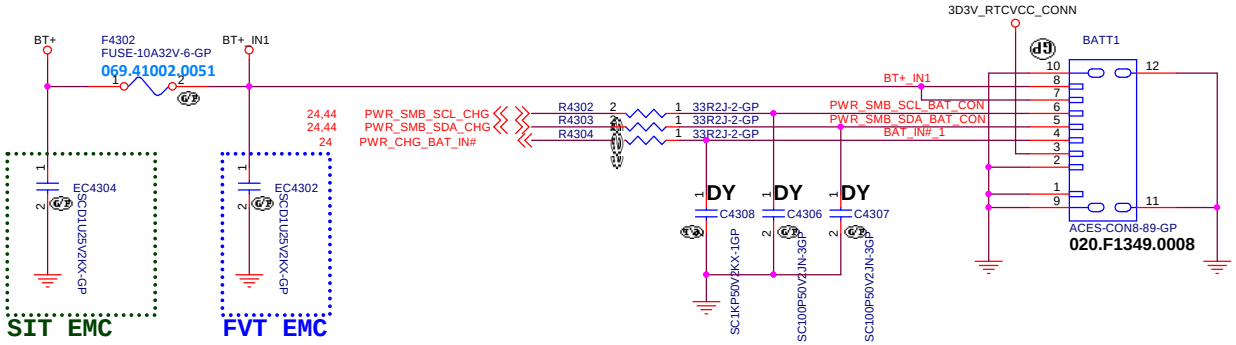
Top side



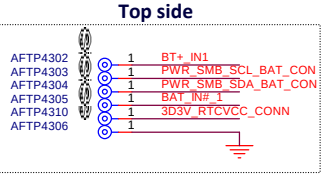
AC DET circuit



Main Battery Connector



Top side



C550

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Title: *INT IO (DCIN/BATT CONN)*		
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OFFPAGE - PIC - EE

PH on EE Side

PH on EE Side

for typeC

Device will be transition from normal Buck-Boost operation to PTM operation by:
- Set REG0x07[7] = 0 to disable the EN_EXITSLM.
- Set REG0x09[6] = 1.
- Set REG0x09[2] = 1.
- Ground ILIM_HIZ pin.

Device will transition out of PTM mode with host control by:
- Set REG0x09[2] = 0.
- Pull ILIM_HIZ pin to high.
- Device exits PTM to buck-boost operation if tripping VinDPM or IbDPM.
- Device exits PTM to buck-boost operation under fault conditions (ACOC; TSHUT; BATOC).

SIT EMC request

For Adapter IN
Confirm with EE

Id= -10A
Qg= -22nC
Rdson=14-22mohm

AD+_2 trace width > 8mil
Length < 500mil

84.05112.001K

84.05212.B11

FVT EMC

2.2uH,
DCR=80ohm,
Idc=14A, Isat=16A
10*10*3mm

FVT EMC request

	VILIM	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

Reserve for Power test

Reserve for PTM
If it hasn't more GPIO

# of CELL	VCELL_PREG	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

84.2N702.J31

0505
buyer: 7"

C550

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (CHARGER_BQ25710R)

Size: Custom | Document Number: C550-ICL | Rev: SC

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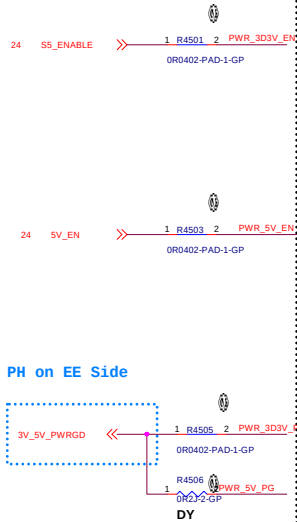
OFFPAGE-Signal



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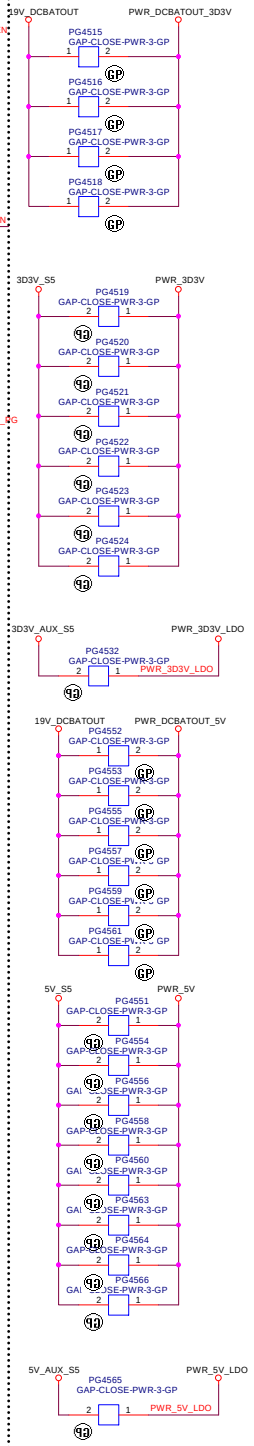

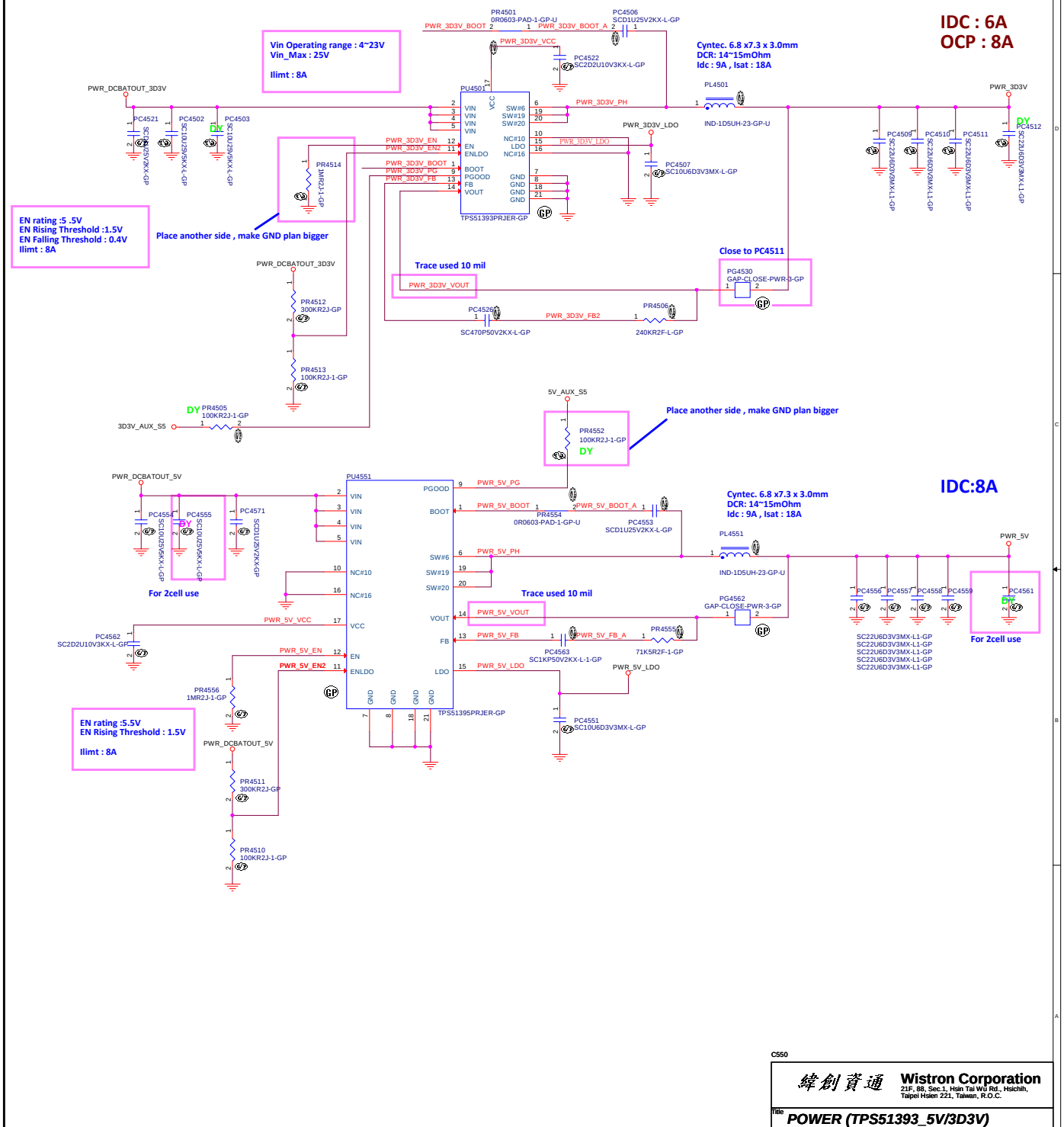

C550

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	POWER (TPS51393_5V/3D3V)	
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PH on CPU side
PROCHOT#_CPU
SVID_CLK_CPU
SVID_DATA_CPU
SVID_ALERT#_CPU
PWR_VCORE_VR_EN
VCORE_PG
PH on CPU side
PWR_VCORE_VR_READY
VSSCORE_SENSE
VCCCORE_SENSE
CHGR_PSYS_IMVP
EE side Link
SVID Pull High V
1D05V_VCCST
PWR_VCORE_VCCST

Reserve for Power test

PWR_VCORE_VCCST
3D3V_S0
PR4607 10KR2F-L1-GP
PR4613 75R2F-2-GP
PR4688 0R0402-PAD-1-GP
PWR_VCORE_VR_READY
PROCHOT#_CPU
CHGR_PSYS_IMVP
PWR_VCORE_PSYS

RT3612EB

PU4601
RT3612EBGQW-1-GP

PWR_VCORE_VREF
PR4619 3K57R2F-GP
PR4620 1K21R2F-2-GP
PR4621 9K09R2F-GP
PR4622 17K8R2F-GP
PWR_VCORE_SET1_A
PWR_VCORE_SET2_A
PWR_VCORE_SET3_A
PR4666 357R2F-GP
PR4660 100R2F-L1-GP-U
PR4661 100R2F-L1-GP-U
PR4624 3K48R2F-GP
PR4625 1K18R2F-GP
PR4626 8K25R2F-1-GP
PR4627 36K5R2F-GP
PWR_VCORE_SET1_B
PWR_VCORE_SET2_B
PWR_VCORE_TSEN_A_A
PWR_VCORE_SET3_B
PR4669 100R2F-L1-GP-U
PR4668 10R2F-L-GP
PR4667 100R2F-L1-GP-U
PR4659 200R2F-L-GP
PWR_VCORE_VCCST
PR4631
PR4632 100R2F-L3-GP
PR4630 75R2F-2-GP
DY
PR4634 49D9R2F-GP
PR4609 SCD1U25V2KX-L-GP
PR4636 10R2F-L-GP
SVID_CLK_CPU
SVID_DATA_CPU
SVID_ALERT#_CPU
PR4674 0R0402-PAD-1-GP
LL/IMON Compesation
NCP15XH103F03RC
Need confirm with RT If you change Chock
Close to PL4701
PR4639 NTC-100K-12-GP-U
B = 4250
PWR_VCORE_NTC1N
PR4665 2K94R2F-GP
PWR_VCORE_VREF
PR4677 0R0402-PAD-1-GP
PR4643 17K8R2F-GP
PWR_VCORE_NTC1N_A
PWR_VCORE_NTC1P
PR4601 23K2R2F-GP
PWR_VCORE_IMON
PR4624 SCD1U25V2KX-L-GP
PR4637 10KR2F-L1-GP
PWR_VCORE_PSYS
PWR_VCORE_VR_READY

5V_S5
PR4604 6D2R2F-GP
PWR_VCORE_VCC
PC4602 SC10U6D3V3MX-L-GP
PR4609 2D2R3-1-U-GP
PWR_VCORE_PVCC
PC4603 SC2D2U10V3KX-L-GP
PR4650 0R0402-PAD-1-GP
PROCHOT#_CPU
PROCHOT#_CPU_A
PR4615 3D9R2F-GP
PWR_VCORE_VREF_A
PWR_VCORE_VREF
PC4606 SCD47U25V3KX-1GP
PWR_VCORE_TSEN
PWR_VCORE_TSEN_A
PWR_VCORE_SET1
PWR_VCORE_SET2
PWR_VCORE_SET3

VCC
PVCC
VR_HOT#
VREF06
TSEN
SET1
SET2
SET3
VCLK
VDIO
ALERT#
VR_READY
PSYS
IMON

19V_DCBATOUT
PR4605 2D2R3F-L-GP
PC4605 SCD22U25V3KX-GP
PWR_VCORE_VIN
PWR_VCORE_VR_EN
PR4612 2D2R3F-L-GP
PWR_VCORE_BOOTA
PWR_VCORE_BOOTA_A
PC4604 SCD1U25V2KX-L-GP
PR4616 2D2R3F-L-GP
PWR_VCORE_BOOTB
PWR_VCORE_BOOTB_A
PC4607 SCD1U25V2KX-L-GP

VIN
VRON
BOOT1
UGATE1
PHASE1
LGATE1
BOOT2
UGATE2
PHASE2
LGATE2

PWR_VCORE_HGA
PWR_VCORE_PHA
PWR_VCORE_LGA
PWR_VCORE_HGB
PWR_VCORE_PHB
PWR_VCORE_LGB

0603 Size
PR4628 2K4R3F-GP
PR4655 2K4R3F-GP
PWR_VCORE_ISEN1P_B
PWR_VCORE_ISEN1P_A
PR4662 2K94R2F-GP
PC4601 SCD1U25V2KX-L-GP
PR4629 680R2F-GP
PC4608 SCD1U25V2KX-L-GP
PWR_VCORE_ISEN1N_B
PWR_VCORE_ISEN1N_A
0603 Size
PR4633 2K4R3F-GP
PR4646 2K4R3F-GP
PWR_VCORE_ISEN2P_B
PWR_VCORE_ISEN2P_A
PR4663 2K94R2F-GP
PC4610 SCD1U25V2KX-L-GP
PR4635 680R2F-GP
PC4611 SCD1U25V2KX-L-GP
PWR_VCORE_ISEN2N_B
PWR_VCORE_ISEN2N_A

ISEN1P
ISEN1N
ISEN2P
ISEN2N

PWR_VCORE_ISEN1P
PWR_VCORE_ISEN1N
PWR_VCORE_ISEN2P
PWR_VCORE_ISEN2N

1V_CPU_CORE
PR4638 100R2F-L1-GP-U
DY
PC4612 SC100P50V2JN-L-GP
PC4613 SC220P50V2KX-3GP
PR4640 31K6R2F-GP
PR4641 10K2R2-2-GP
PR4671 0R0402-PAD-1-GP
VCCCORE_SENSE
PR4644 100R2F-L1-GP-U
PR4672 0R0402-PAD-1-GP
VSSCORE_SENSE

VSEN
COMP
FB
RGND
GND

PWR_VCORE_VSEN
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_RGND

C550

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT3612EB_VCORE(1/2))
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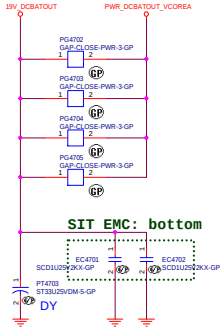

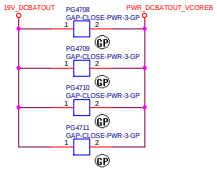

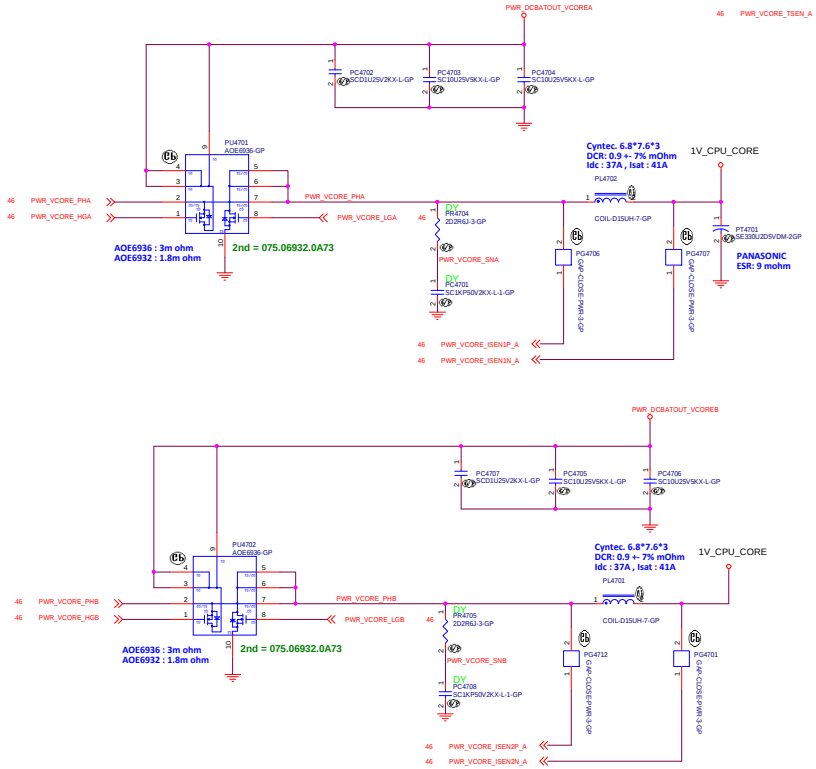

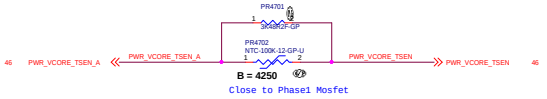

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER (AOE6936_VCORE(2/2))		
Size: Custom	Document Number: C550-ICL	Rev: SC
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER (RSVD)***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***POWER (RSVD)***

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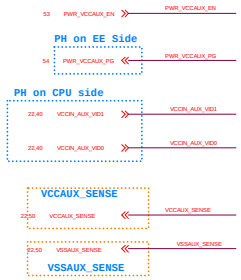

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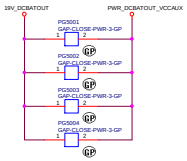

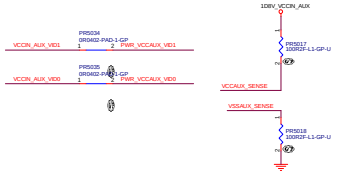

TABLE: MP2941 VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

LOGIC

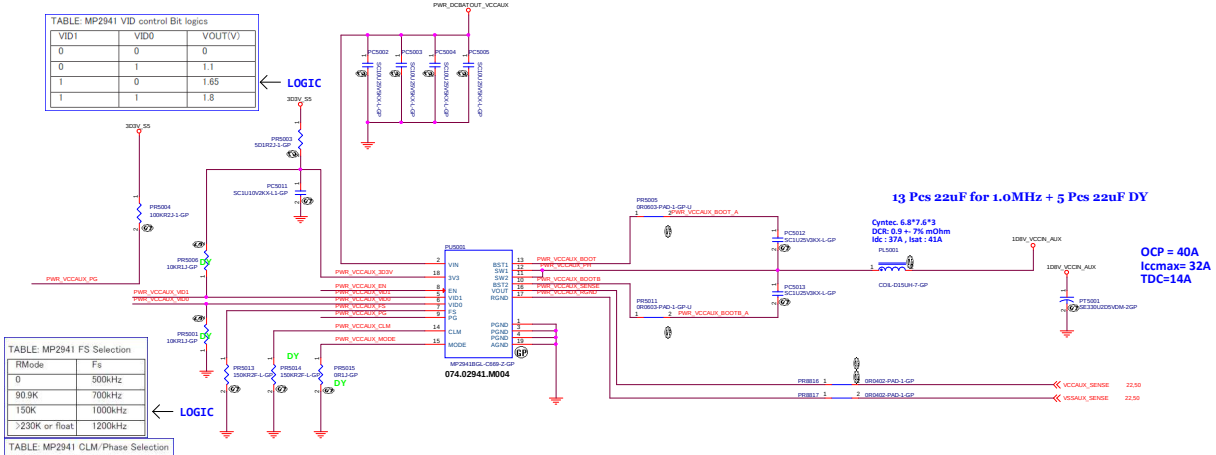

TABLE: MP2941 FS Selection

RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

LOGIC

TABLE: MP2941 CLM/Phase Selection

RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

LOGIC

TABLE: MP2941 Mode Selection

RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay

LOGIC

TABLE : MP2941

Item	R0 sample	R1 sample
VOUT	1.65V fixed	Defined by VCCPCHCORE_VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary

C550

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Title: POWER (VCCINAUX_MP2941)

Size: A1 | Document Number: C550-ICL | Rev: SC

Date: Thursday, March 06, 2008 | Sheet 50 of 105

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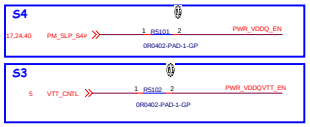

PH on EE Side

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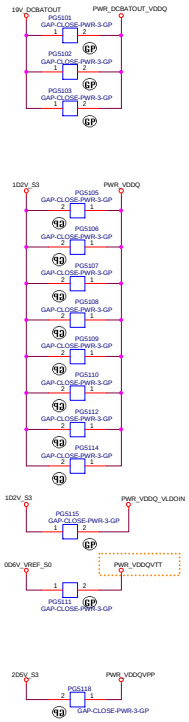

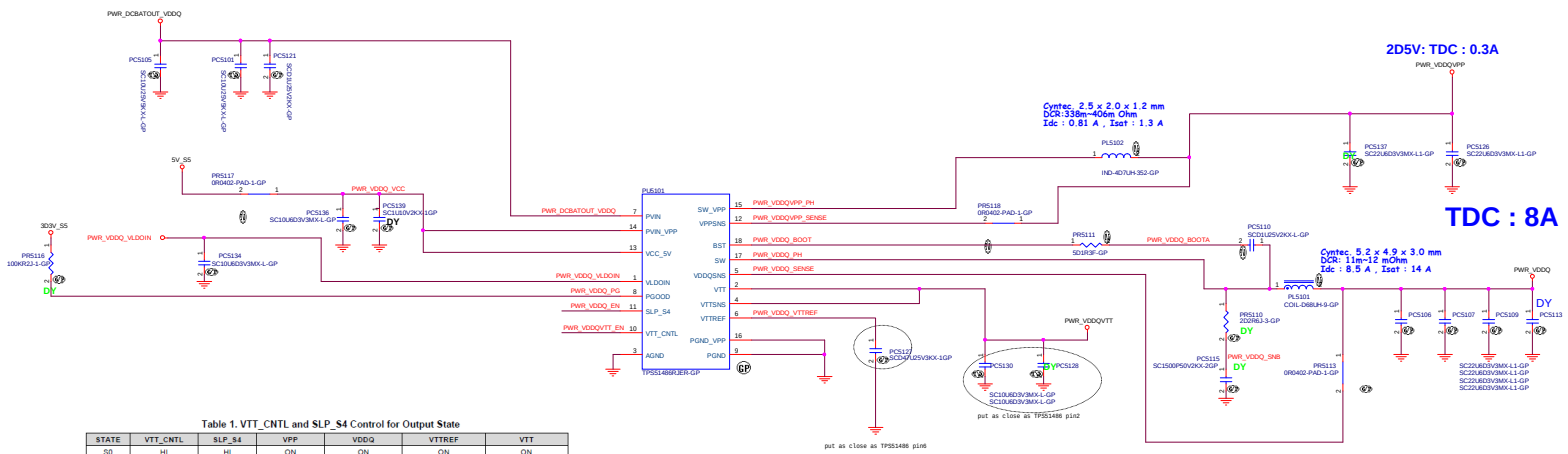

Table 1. VTT_CNTL and $LP_S4 Control for Output State

STATE	VTT_CNTL	$LP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

C550

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File: POWER (TPS51486R_VDDQ/VTT)

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C550

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER (RSVD)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

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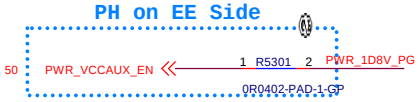
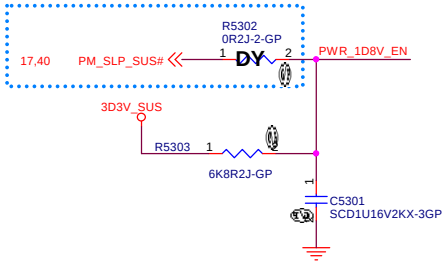


PH on EE Side



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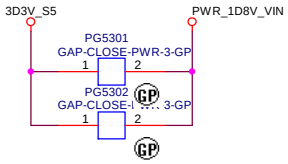
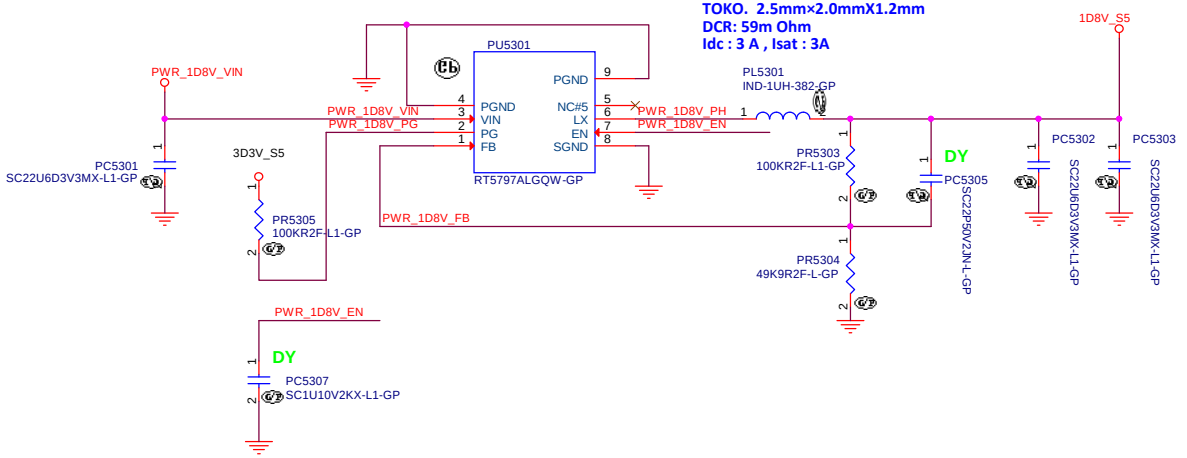


TDC=2A
Imax= 3A

TOKO. 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A



C550

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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT5797_1D8V)

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PH on EE Side

VCCIN_AUX_PWRGD

50 PWR_VCCAUX_PG >> 1 R5450 2 PWR_VNN_EN

0R0402-PAD-1-GP

PM_SLP_S3#

17,24,40,86 PM_SLP_S3# >> 1 R5452 2 PWR_VNN1D05V_VID

0R0402-PAD-1-GP

PWR_VNN1D05V_PG1 1 R5453 2 PWR_1D05V_EN

0R0402-PAD-1-GP

OFFPAGE-GAP

1D05V_VNN_BYPASS — PG5401 GAP-CLOSE-PWR-3-GP — PWR_VNN

1D05V_S5_BYPASS — PG5402 GAP-CLOSE-PWR-3-GP — PWR_1D05V

3D3V_S5

PR5420 1 100KR2J-1-GP 2 PWR_VNN1D05V_PG1

PR5421 1 100KR2J-1-GP 2 PWR_VNN1D05V_PG2

PC5401 1 SC1U10V2KX-L1-GP

5V_S5 — PR5413 1 2D2R2J-3-GP

PC5402 1 SC10U6D3V3MX-L-GP

5V_S5 — PR5422 1 0R0402-PAD-1-GP 2 PWR_VNN1D05V_VINA

PR5410 1 0R0402-PAD-1-GP 2 PWR_VNN1D05V_VINB

PC5403 1 SC10U6D3V3MX-L-GP

PWR_VNN1D05V_VID

PWR_VNN1D05V_BOOTA_A PC5404 1 SCD1U25V2KX-L-GP PWR_VNN1D05V_BOOTA

PWR_VNN1D05V_BOOTB_A PC5405 1 SCD1U25V2KX-L-GP PWR_VNN1D05V_BOOTB

DY PC5406 1 SCD1U16V2KX-L-GP PWR_VNN1D05V_PG1

DY PC5407 1 SCD1U16V2KX-L-GP PWR_VNN1D05V_PG2

PR5423 1 0R0402-PAD-1-GP 2 PWR_VNN1D05V_PHB

PWR_VNN1D05V_PHA

PR5401 0R0402-PAD-1-GP

PU5401

VCC	8	EN1	15 PWR_VNN_EN
VIN1	11	EN2	6 PWR_1D05V_EN
VIN2	10	LX1	1 PWR_VNN1D05V_PHA
VID	13	LX2	4 PWR_VNN1D05V_PHB
BOOT1	2	FB2	5 PWR_VNN1D05V_FB2
BOOT2	3	VOUT1	16 PWR_VNN1D05V_VOUT1
POK1	14	AGND	17
POK2	7	PGND	9
		PGND	12

APW8738AQBI-TRG-1-GP

074.08738.0073

Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A

PL5401 IND-1UH-382-GP

PWR_VNN

PC5411 SC10U6D3V3MX-L-GP

PC5412 SC10U6D3V3MX-L-GP

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A

PL5402 IND-10UH-330-GP

PWR_1D05V

PR5408 7K5R2F-1-GP

PR5407 10KR2F-2-GP

PC5410 SC10U6D3V3MX-L-GP

PR5419 1 0R0402-PAD-1-GP 2 PWR_VNN

C550

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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (APW8738A_VNN1D05)

Size	Document Number	Rev
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Main Func = LCD

LCD Connector

INVERTER POWER

F5501 69.50007.A31->69.42402.001 (main)_20180718

69.42402.001

SIT EMC request:Top

074.51712.009F

1) DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

20.K0678.050

Test point

Touch Connector

Touch

074.51712.009F

PLACE NEAR MIC1

20.F2191.010

C550	
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Title: DISPLAY (LCD/TOUCH)	
Size: A1	Document Number: C550-ICL
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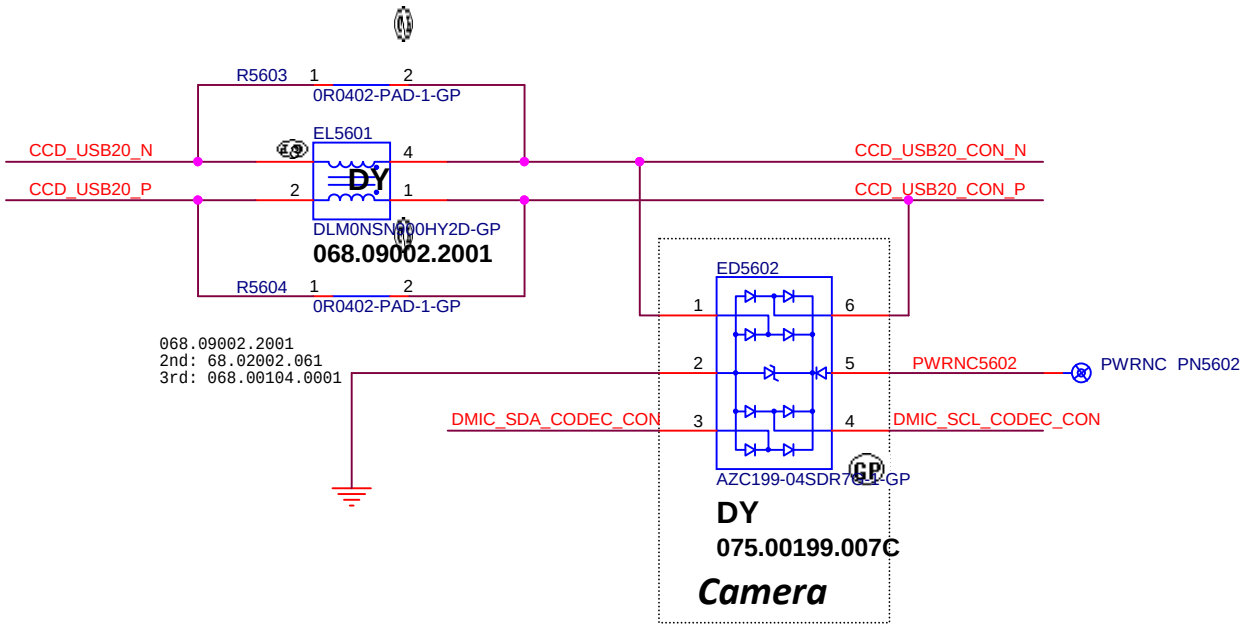
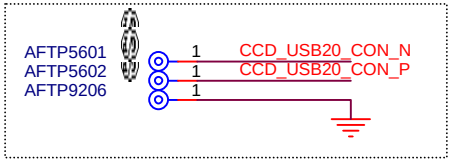
16 CCD_USB20_N
16 CCD_USB20_P
55 CCD_USB20_CON_N
55 CCD_USB20_CON_P
27,55 DMIC_SCL_CODEC_CON
27,55 DMIC_SDA_CODEC_CON

CCD CONN



BOT side



C550

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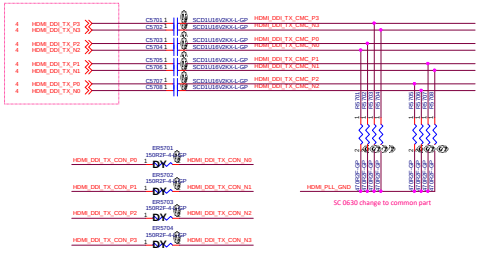
Title: ***DISPLAY (CAMERA)***		
Size: A4	Document Number: **C550-ICL**	Rev: **SC**
Date: Thursday, March 05, 2020	Sheet 56 of 106	

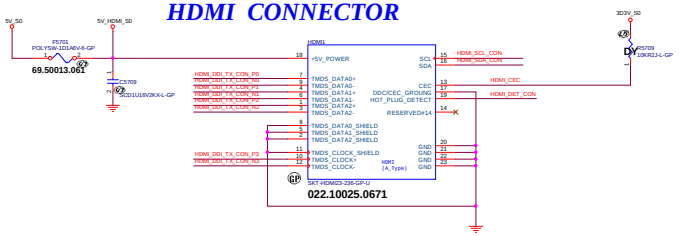
HDMI

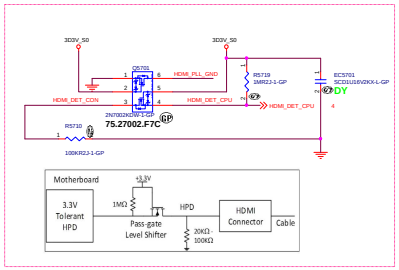
HDMI Passive Level Shifter

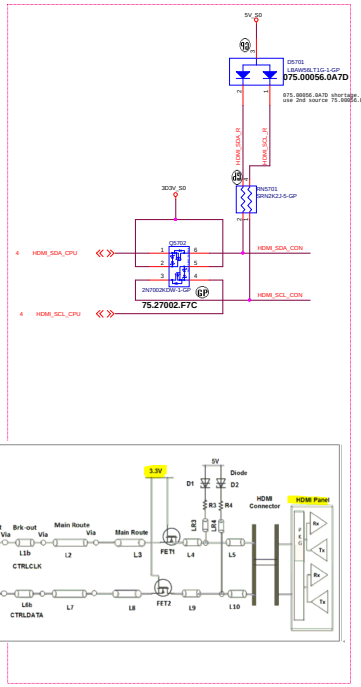
Close to HDMI Connector

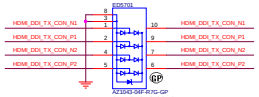


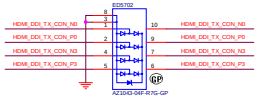
HDMI CONNECTOR

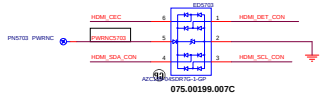


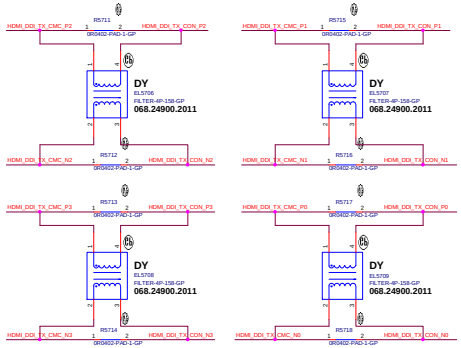












C550

Wistron Corporation
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Title: DISPLAY (HDMI CONN/RETIMER)

Size: A1 | Document Number: C550-ICL | Rev: SC

Date: Thursday, March 06, 2008 | Sheet 57 of 105

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Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
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Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

Date: Thursday, March 05, 2020 Sheet 59 of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)*

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Main Func = WLAN

(Off-Page)

17 PM_SLP_WLAN#
3 CNVI_EN#
20,24 WIFI_RF_EN
15,20 BLUETOOTH_EN
17,24,26,63,66,76 PLT_RST#
18 SUS_CLK
19 CNV_CLKREQ
19 CNV_RF_RESET
21 CNV_BRI_RSP
15,21 CNV_BRI_DT
21 CNV_RGI_RSP
15,21 CNV_RGI_DT
21 CNV_WT_CLK_DP
21 CNV_WT_CLK_DN
21 CNV_WT_DP0
21 CNV_WT_DN0
21 CNV_WT_DP1
21 CNV_WT_DN1
21 CNV_WR_CLK_DP
21 CNV_WR_CLK_DN
21 CNV_WR_DP0
21 CNV_WR_DN0
21 CNV_WR_DP1
21 CNV_WR_DN1
16 BT_USB20_P
16 BT_USB20_N
16 WLAN_PCIE_TX_P
16 WLAN_PCIE_TX_N
16 WLAN_PCIE_RX_P
16 WLAN_PCIE_RX_N
18 WLAN_CLK_CPU_P
18 WLAN_CLK_CPU_N
18 WLAN_CLKREQ_CPU_N
17 PCIE_WAKE#

3D3V_S5
WLAN-NonPS
R6130 1 0R5J-5-GP
3D3V_WLAN
1A
C6103 SCD1U16V2KX-3GP WLAN-PS
R6111 10KR2J-3-GP WLAN-PS
C6102 SCD1U16V2KX-3GP WLAN-PS
WLAN_EN_R#
Q6101 PJA3415-GP WLAN-PS
084.03415.0031
C6101 SCD1U16V2KX-3GP WLAN-PS
FC6101 SC10P50V2JN-L1-GP WLAN-PS
R6112 20KR2J-L2-GP WLAN-PS
R6110 0R2J-2-GP WLAN-PS
CNVI_EN# CNVI_EN#_R
R6123 10KR2J-3-GP WLAN-PS
Q6102 2N7002K-3-GP
WLAN_EN#
PM_SLP_WLAN#
84.2N702.J31 WLAN-PS

BOM Control

TOP side
PLT_RST# WLAN_CLK_CPU_P WLAN_CLK_CPU_N BT_USB20_CON_P BT_USB20_CON_N
AFTE14P-GP AFTP6101 AFTP6102 AFTP6103 AFTP6104 AFTP6105

3D3V_S0 WLAN: 1080mA 3D3V_WLAN
R6101 DY 0R3J-0-U-GP
R6102 DY 0R3J-0-U-GP
3D3V_WLAN
C6107 DY C6108 DY C6109 DY C6104 C6105 C6106
SCD1U16V2KX-3GP

M.2 Key-E FOR WLAN / BT

WLAN1 NGFF_KEY_E_75P
BT_USB20_P R6108 0R0402-PAD-1-GP BT_USB20_CON_P
BT_USB20_N R6109 0R0402-PAD-1-GP BT_USB20_CON_N
CNV_WR_DN1 CNV_WR_DP1 CNV_WR_DN0 CNV_WR_DP0 CNV_WR_CLK_DN CNV_WR_CLK_DP
WLAN_PCIE_TX_P C6110 SCD1U16V2KX-L-GP WLAN_PCIE_TX_CON_P
WLAN_PCIE_TX_N C6111 SCD1U16V2KX-L-GP WLAN_PCIE_TX_CON_N
WLAN_PCIE_RX_P WLAN_PCIE_RX_N WLAN_CLK_CPU_P WLAN_CLK_CPU_N WLAN_CLKREQ_CPU_N
PCIE_WAKE# R6117 0R0402-PAD-1-GP PCIE_WAKE#_CON
CNV_WT_DN1 CNV_WT_DP1 CNV_WT_DN0 CNV_WT_DP0 CNV_WT_CLK_DN CNV_WT_CLK_DP
SKT-NGFF75P-164-GP
062.10003.0B11 062.10007.0371-> 062.10003.0B11/ 062.10007.0511_FVT

3D3V_WLAN
CNV_RF_RESET CNV_CLKREQ
CNV_BRI_RSP_R R6118 22R2J-2-GP CNV_BRI_RSP
CNV_RGI_DT_R R6121 22R2J-2-GP CNV_RGI_DT
CNV_RGI_RSP_R R6104 22R2J-2-GP CNV_RGI_RSP
CNV_BRI_DT_R R6122 22R2J-2-GP CNV_BRI_DT
E51_TXD_WLAN R6103 DY 0R2J-2-GP E51_TXD 24
WLAN_COEX2 WLAN_COEX1 TP6102 Test_Point_20MIL TP6103 Test_Point_20MIL
SUSCLK_32K_N R6113 33R2J-2-GP SUS_CLK
PLT_RST#
BLUETOOTH_EN
WIFI_RF_EN
RESERVED#66 TP6104

1D8V_S5
CNV_BRI_DT R6124 DY 10KR2J-3-GP
CNV_RGI_RSP R6125 DY 20KR2F-L-GP
CNV_BRI_RSP R6126 DY 20KR2F-L-GP

ED6101 DY-EMC
BT_USB20_N BT_USB20_P
PWRNC6101 PWRNC PN6101
AZC099-04S-2-GP
075.09904.0A7C
PLACE NEAR WLAN1

CNV_CLKREQ R6119 71K5R2F-1-GP
CNV_RF_RESET R6107 75KR2J-GP

3D3V_WLAN
WIFI_RF_EN BLUETOOTH_EN R6105 DY 10KR2J-3-GP R6106 DY 10KR2J-3-GP
WIFI_RF_EN BLUETOOTH_EN R6120 DY 100KR2J-1-GP R6114 DY 100KR2J-1-GP

C550
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: INT IO (WLAN/CNVi)
Size: A2 | Document Number: C550-ICL | Rev: SC
Date: Thursday, March 05, 2020 | Sheet 61 of 106

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)*

Size	Document Number	Rev
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SSD CONN

(Off-Page)

16 SSD_PCIE_RX_N3
16 SSD_PCIE_RX_P3
16 SSD_PCIE_TX_N3
16 SSD_PCIE_TX_P3

16 SSD_PCIE_RX_N2
16 SSD_PCIE_RX_P2
16 SSD_PCIE_TX_N2
16 SSD_PCIE_TX_P2

16 SSD_PCIE_RX_N1
16 SSD_PCIE_RX_P1
16 SSD_PCIE_TX_N1
16 SSD_PCIE_TX_P1

16 SSD_SATA_RX_N
16 SSD_SATA_RX_p
16 SSD_SATA_TX_N
16 SSD_SATA_TX_p

18 SSD_CLK_CPU_N
18 SSD_CLK_CPU_P
18 SSD_CLKREQ_CPU_N

17,24,26,61,66,76 PLT_RST#

16 SSD_DEVSLP

SSD_DET	
1	SATA
0	PCIe

M2_SSD_PEDET	
1	PCIe
0	SATA

SSD_PCIE_TX_N3 C6301 1 — SCD22U10V2KX-L1-GP — SSD_PCIE_TX_N3_C
SSD_PCIE_TX_P3 C6302 1 — SCD22U10V2KX-L1-GP — SSD_PCIE_TX_P3_C
SSD_PCIE_TX_N2 C6303 1 — SCD22U10V2KX-L1-GP — SSD_PCIE_TX_N2_C
SSD_PCIE_TX_P2 C6304 1 — SCD22U10V2KX-L1-GP — SSD_PCIE_TX_P2_C
SSD_PCIE_TX_N1 C6305 1 — SCD22U10V2KX-L1-GP — SSD_PCIE_TX_N1_C
SSD_PCIE_TX_P1 C6306 1 — SCD22U10V2KX-L1-GP — SSD_PCIE_TX_P1_C
SSD_SATA_TX_N C6307 1 — SCD22U10V2KX-L1-GP — SSD_SATA_TX_N_C
SSD_SATA_TX_p C6308 1 — SCD22U10V2KX-L1-GP — SSD_SATA_TX_p_C

SSD1 — SKT-MINI67P-32-GP — NGFF_KEY_M 75P

1	GND	2	3_3VAUX
3	GND	4	3_3VAUX
5	SSD_PCIE_RX_N3	PETN3	6 NC#6
7	SSD_PCIE_RX_P3	PETP3	8 NC#8
9	PETN3		10 DAS/DSS#
11	GND		12 3_3VAUX
13	PERN3		14 3_3VAUX
15	PERP3		16 3_3VAUX
17	GND	PETN2	18 3_3VAUX
19	SSD_PCIE_RX_N2	PETP2	20 NC#20
21	SSD_PCIE_RX_P2		22 NC#22
23	PETN2		24 NC#24
25	GND		26 NC#26
27	PERN2		28 NC#28
29	PERP2		30 NC#30
31	GND		32 NC#32
33	SSD_PCIE_RX_N1		34 NC#34
35	SSD_PCIE_RX_P1		36 NC#36
37	PETN1		38 DEVSLP
39	PETP1		40 NC#40
41	GND		42 NC#42
43	PERN1		44 NC#44
45	PERP1		46 NC#46
47	GND		48 NC#48
49	SSD_SATA_RX_p		50 PERST#/NC#50
51	SSD_SATA_RX_N		52 CLKREQ#/NC#52
53	GND		54 PEWAKE#/NC#54
55	PETN0/SATA_B+		56 NC#56
57	PETP0/SATA_B-		58 NC#58
67	GND		68 SUSCLK_32KHZ
69	PERN0/SATA_A-		70 3_3VAUX
71	PERP0/SATA_A+		72 3_3VAUX
73	GND		74 3_3VAUX
75	SSD_CLK_CPU_N		76
77	SSD_CLK_CPU_P		NP2
NP1	REFCLKN		
	REFCLKP		
	GND		
	NC#67		
	M2_SSD_PEDET		
	GND		
	GND		
	GND		
	77		
	NP1		

062.10003.0841

3D3V_NGFF_SSD — R6304 0R0805-PAD-1-GP-U — 3D3V_S0
R6305 0R0805-PAD-1-GP-U
DAS2 — R6307 — 0R2J-2-GP — DY
SSD_DEVSLP
SSD_CLKREQ# — R6306 0R0402-PAD-1-GP — PLT_RST# — SSD_CLKREQ_CPU_N

3D3V_NGFF_SSD — DY
C6326 SCD1U16V2KX-L-GP
C6327 SC1U10V2KX-L1-GP
C6328 SC10U6D3V3MX-L-GP

C6329 SCD01U25V2KX-3GP
C6330 SC1U25V3KX-3GP
C6331 SCD22U25V3KX-GP
Close to SSD2 pin 2, 4

C6332 SCD01U25V2KX-3GP
C6333 SC1U25V3KX-3GP
C6334 SCD22U25V3KX-GP
Close to SSD2 pin 70, 72, 74

3D3V_S0 — R6308 100KR2J-1-GP
16 SSD_DET# — R6309 — DY — 0R2J-2-GP
2N7002K-2-GP Q6301
M2_SSD_PEDET
84.2N702.J31

PLT_RST# — D6303 AOZ8212ACI-05-GP
075.08212.007D
DY

close to SSD1
main: 075.08212.007D AOS
2nd: 075.52215.007D NXP
3rd: 75.05125.07D Amazing

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Title: INT IO (SSD M.2/eMMC)

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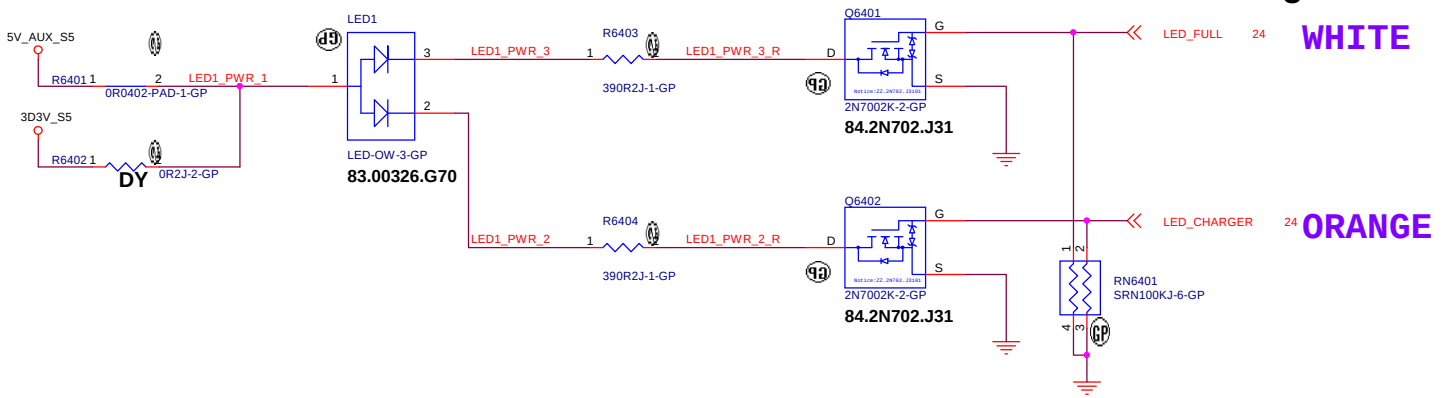
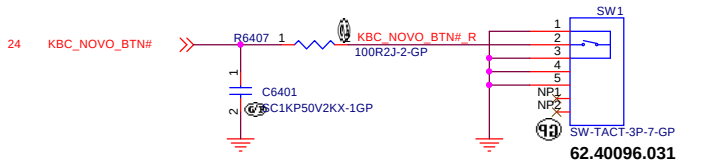
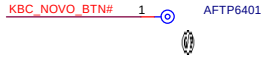
LED

DC-IN



NOVO BUTTON





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Title: *LED/NOVO BUTTON*		
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24 KCOL[7:0]

24 KROW[7:0]

CLOSE keyboard connector

KB CONN for 14C

KB1 20.K0849.034/ 20.K0724.034-> 020.K0013.0034_SC

020.K0013.0034
LC55_14C

KB CONN for 15C

KB2 20.K0849.034/ 20.K0724.034-> 020.K0013.0034_SC

020.K0013.0034
LC55_15C

Follow LS1511A

I2C Port3

Follow Raichu

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

TPAD CONN

020.K0376.0008

TOP side

KBD BL CONN FOR 14C

020.K0206.0004
LC55_14C

KBBL1 change to 020.K0206.0004 from 020.K0305.0004

KBD BL CONN FOR 15C

020.K0206.0004
LC55_15C

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Title: INT IO (KB/TP)

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USB3.0 Port1

16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
16 USB1_USB30_TX_N
16 USB1_USB30_TX_P

36 USB1_USB20_AOU_N
36 USB1_USB20_AOU_P

USB3.0 Port2

16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB30_TX_N
16 USB2_USB30_TX_P

16 USB2_USB20_N
16 USB2_USB20_P

CARD

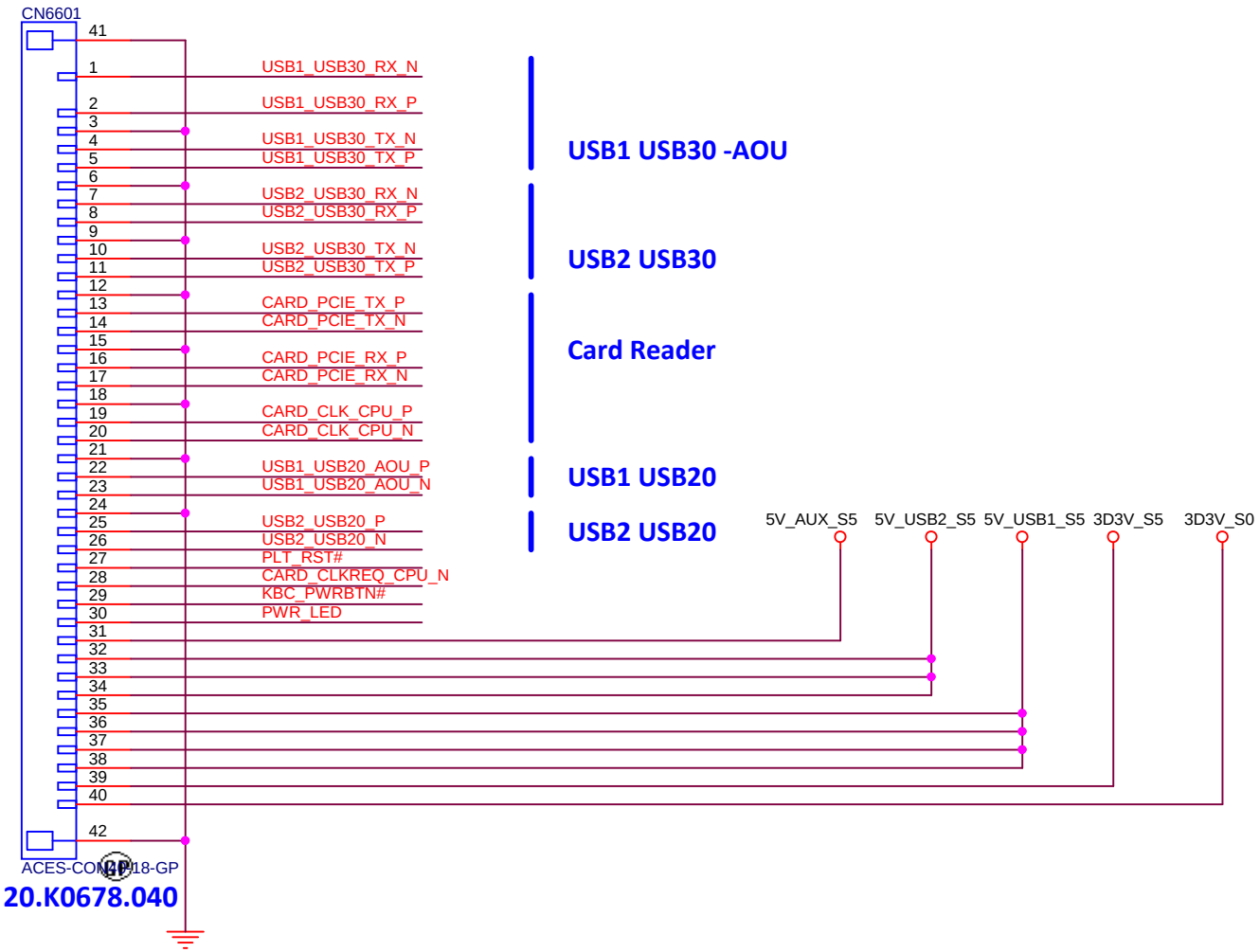
16 CARD_PCIE_RX_N
16 CARD_PCIE_RX_P
16 CARD_PCIE_TX_N
16 CARD_PCIE_TX_P

18 CARD_CLK_CPU_P
18 CARD_CLK_CPU_N
18 CARD_CLKREQ_CPU_N

Others

17,24,26,61,63,76 PLT_RST#
24 KBC_PWRBTN#
24 PWR_LED

MB to IO Board



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Title: ***IO BOARD CONN***

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Title ***SENSOR (RSVD)(HALL-SENSOR)***

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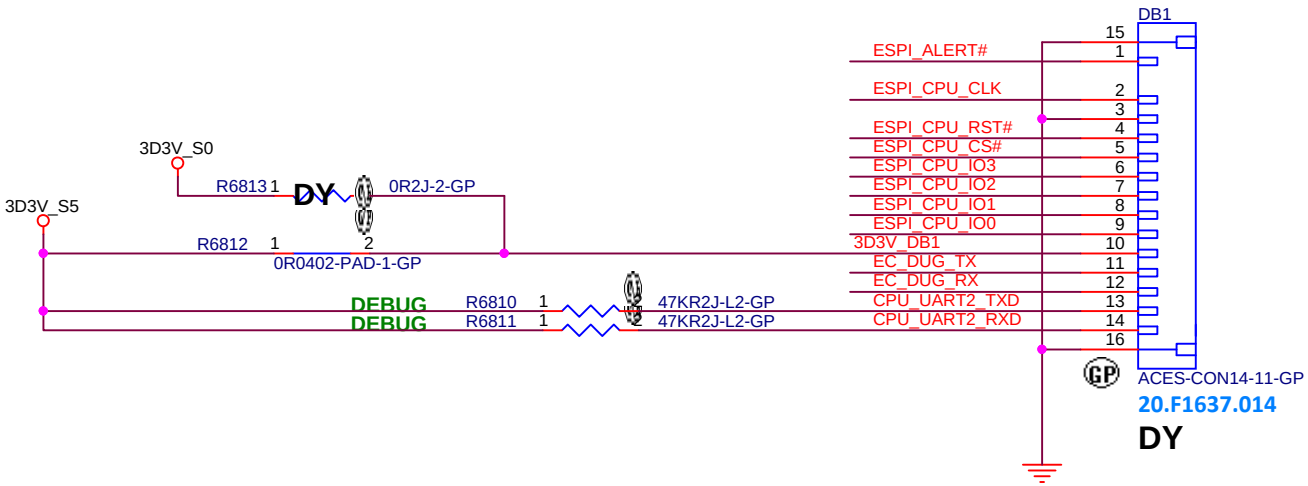
20 CPU_UART2_TXD
20 CPU_UART2_RXD
24 ESPI_ALERT#
18,24 ESPI_CPU_CLK

18,24 ESPI_CPU_RST#
24 EC_DUG_RX
24 EC_DUG_TX

18,24 ESPI_CPU_CS#
18,24 ESPI_CPU_IO3
18,24 ESPI_CPU_IO2
18,24 ESPI_CPU_IO1
18,24 ESPI_CPU_IO0



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Title: ***DEBUG (ESPI DEBUG)***

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Title: ***SENSOR (RSVD)***

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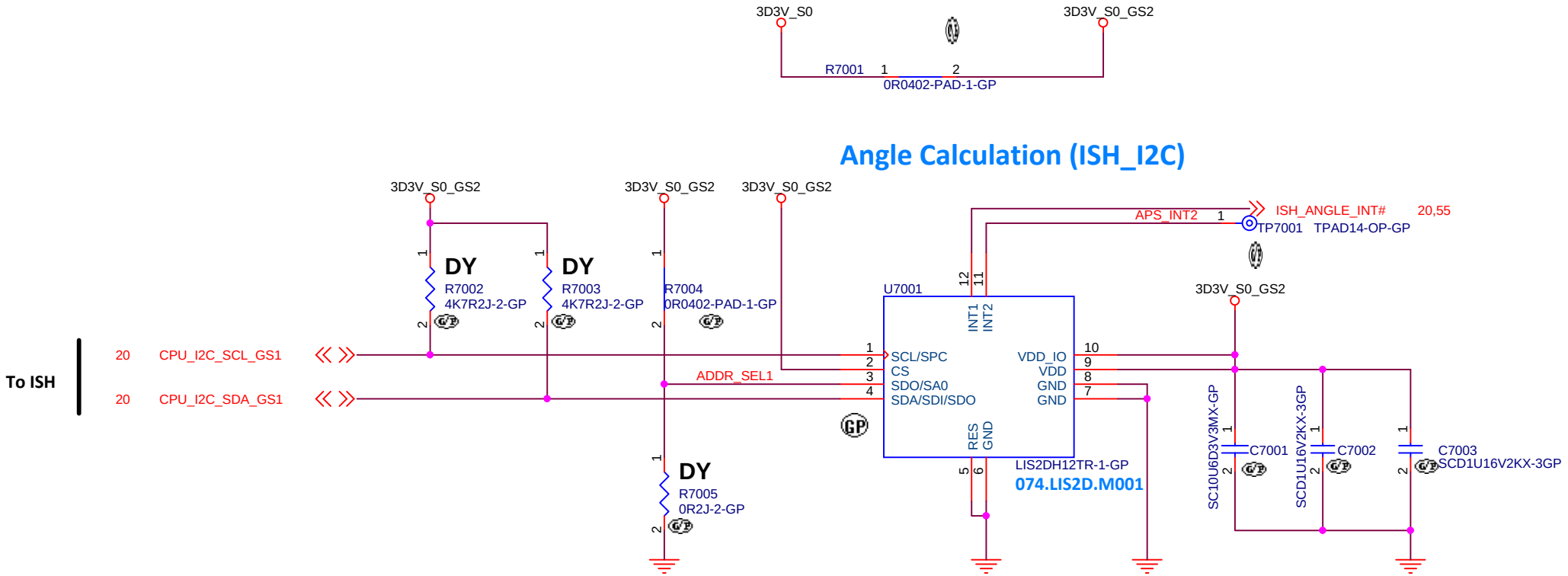

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address
LIS2DH12TR	H L	32h(W) & 33h(R) 30h(W) & 31h(R)

← Logic

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001

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Title: **SENSOR (G-SENSOR)**

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Title ***EXT IO (RSVD)***

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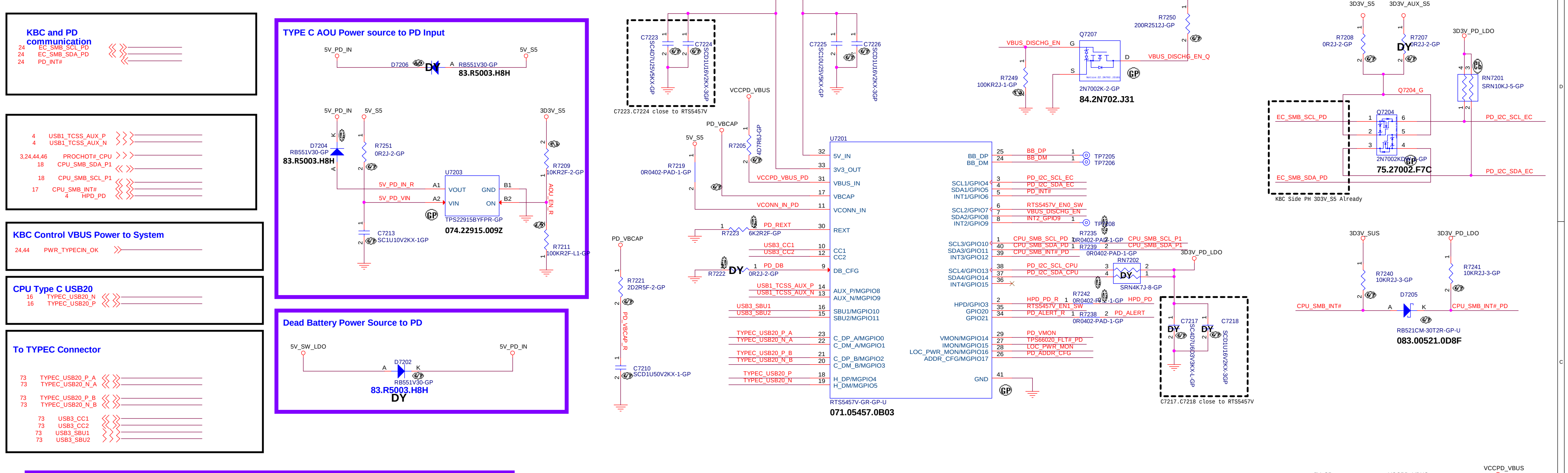
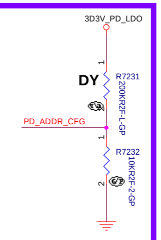
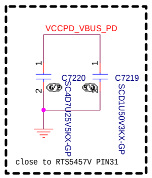
USB Port3, Type C_USB3.0, PD

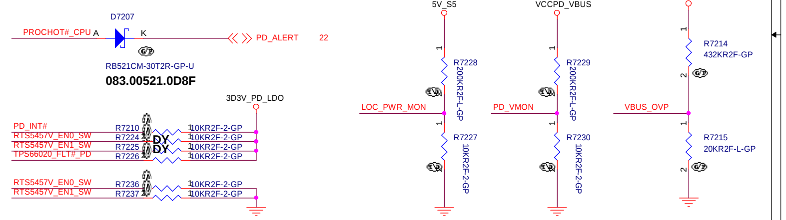


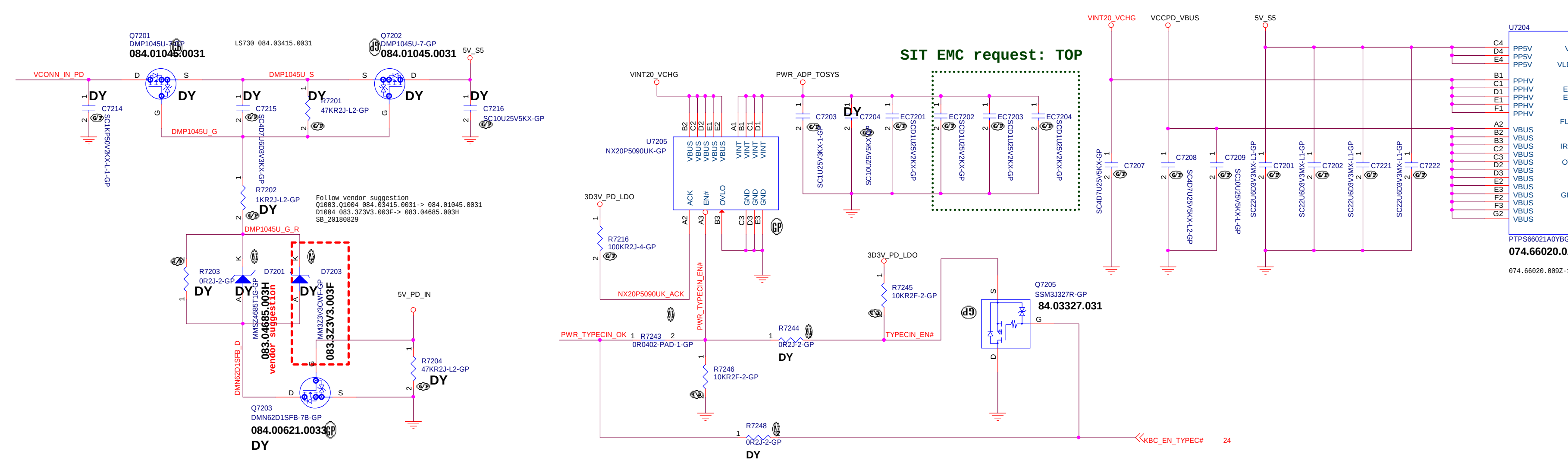
Slave Addr	PULL-HIGH RESISTOR (R7231)	PULL-LOW RESISTOR (R7232)	VOLTAGE
addr0: 0xCC	NC	10.0K	< 0.2V
addr1: 0xCE	75K	10.0K	>= 0.2V && < 0.6V
addr2: 0xD0	33.0K	10.0K	>= 0.6V && < 1.0V
addr3: 0xD2	10.0K	10.0K	>= 1.0V





Function Table		
EN1	EN0	Device State
0	0	Source and Sink paths disabled.
0	1	Sink path enabled.
1	0	Source path enabled, 1.5A
1	1	Source path enabled, 3.0A





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Title: ***EXT IO (RSVD)***

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KBC

24 TYPE_C_DET#

From PD Controller

72 TYPEC_USB20_P_A
72 TYPEC_USB20_N_A
72 TYPEC_USB20_P_B
72 TYPEC_USB20_N_B
72 USB3_CC1
72 USB3_CC2
72 USB3_SBU1
72 USB3_SBU2

CPU TCSS Port

4 USB3_TCSS_TX_P0
4 USB3_TCSS_TX_N0
4 USB3_TCSS_RX_P0
4 USB3_TCSS_RX_N0
4 USB3_TCSS_TX_P1
4 USB3_TCSS_TX_N1
4 USB3_TCSS_RX_P1
4 USB3_TCSS_RX_N1

VCCPD_VBUS_CONN
EC7301 SCD1U16V2KX-1-GP
EC7302 SCD1U16V2KX-1-GP

VCCPD_VBUS_CONN
R7301 0R0805-PAD-1-GP-U
R7302 0R0805-PAD-1-GP-U
VCCPD_VBUS

3D3V_AUX_KBC
R7310 100KR2J-1-GP
TYPE_C_DET#
Q7301 2N7002K-2-GP
84.2N702.J31
Q7301_G
VCCPD_VBUS
R7311 76K8R2F-GP
R7318 100KR2F-L1-GP
D7305 MM3Z3V3CWF-GP
DY

USB3_CC1
USB3_CC2
C7312 SC220P50V2KX-3GP
C7313 SC220P50V2KX-3GP
FROM TYPE C PD

3D3V_PD_LDO
3D3V_PD_LDO
R7303 0R2J-2-GP DY
R7304 10KR2J-3-GP DY

CC PROTECTION

U7301 SN1710033RUKR-1-GP
074.17100.0073
DY

USB3_CC1 USB3_CC2 USB3_SBU1 USB3_SBU2
USB3_CC_VBIAS USB3_CC_VPWR
USB3_CC_FLT#
C7301 SCD1U16V2KX-1-GP DY
C7302 SCD1U16V2KX-3GP DY
USBC_CC_GND R7309 0R3J-0-U-GP DY

The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.

R7312 R7313 0R0402-PAD-1-GP
R7314 R7315 0R0402-PAD-1-GP

TOP side

AFTP7301 AFTP7302 AFTP7303 AFTP7304 AFTP7305
AFTP7306 AFTP7307 AFTP7308 AFTP7309

USB Port3
Type C_USB3.0, PD

ED7303 AZ1043-04F-R7G-GP
075.01043.0073
075.01043.0073
075.00810.0A73
075.PUSB3.0A73

ED7304 AZ1043-04F-R7G-GP
075.01043.0073

VCCPD_VBUS_CONN
D7304 P4SMAFJ20A-GP
083.P4SMA.0AAM
DY

USB3
SKT-USB28-18-GP
SCA0L72570AA

VCCPD_VBUS_CONN

Close USB3

ED7301 AZ5125-02S-R7G-GP
75.05125.07D

ED7302 AZC199-04SDR7G-GP
075.00199.007C
PWRNC7301 PWRNC PN7301

Close USB3

C7304 C7305 SCD22U10V2KX-1GP
C7306 C7307 SCD33U6D3V2KX-1GP
R7305 R7306 220KR2J-L2-GP
C7308 C7309 SCD22U10V2KX-1GP
C7310 C7311 SCD33U6D3V2KX-1GP
R7307 R7308 220KR2J-L2-GP

R7316 R7317 R7319 R7320 0R2J-2-GP DY
EL7301 EL7302 DLM0NSN900HY2D-GP
068.09002.2001

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Title: EXT IO (TYPEC CONN)
Size: A2 | Document Number: C550-ICL | Rev: SC
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Title: ***EXT IO (TYPEC PD)***

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Title ***EXT IO (RSVD)***

Size	Document Number	Rev
A4	**C550-ICL**	**SC**

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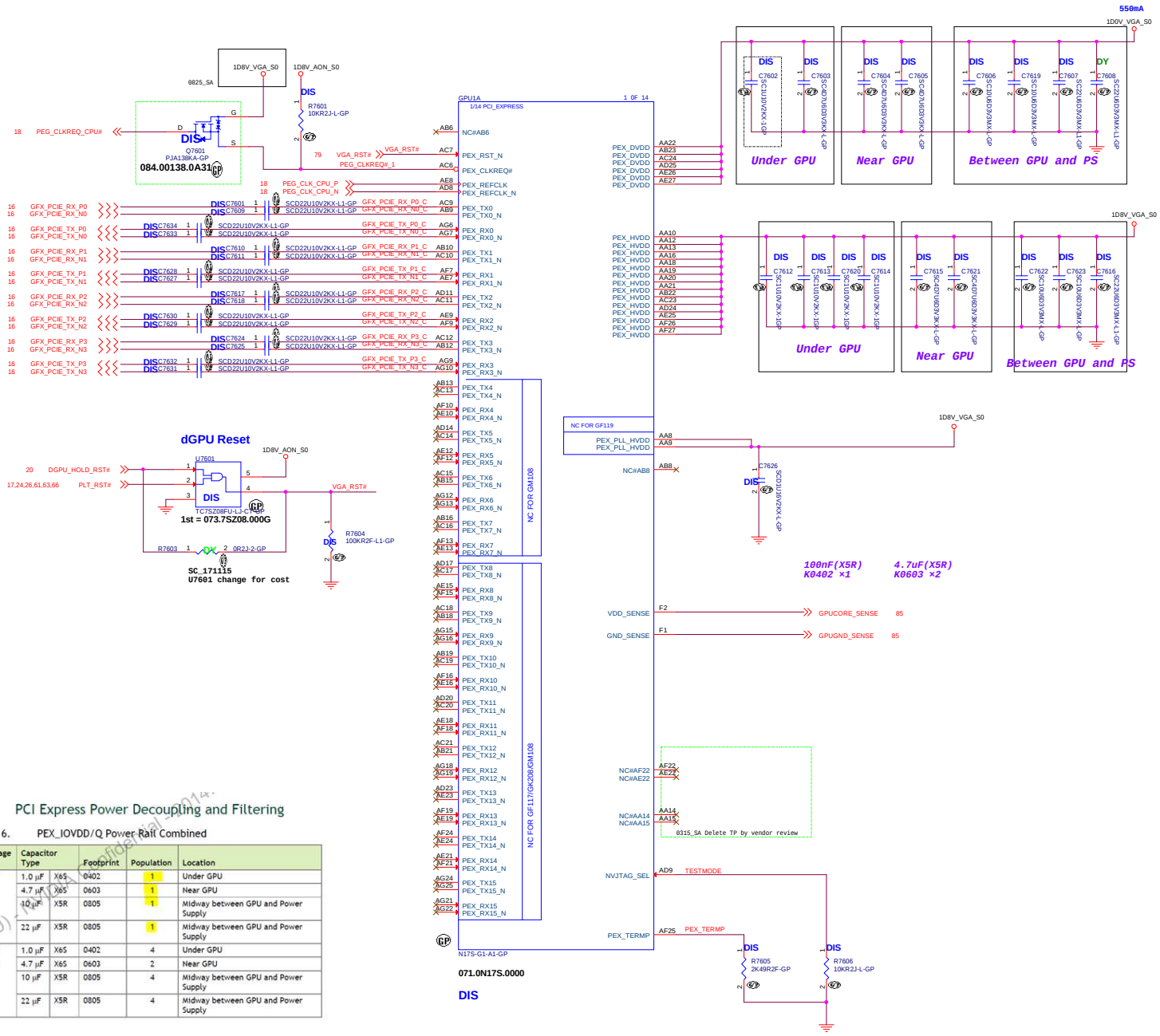

3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3B-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

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Title: GPU (PEG 1/5)

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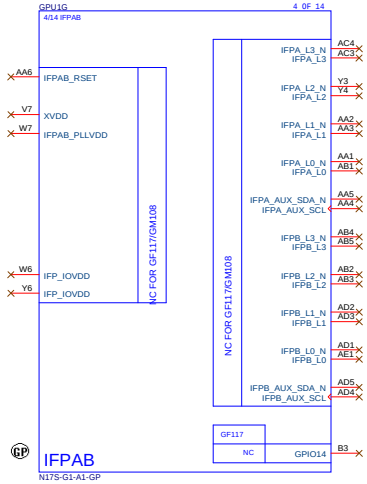

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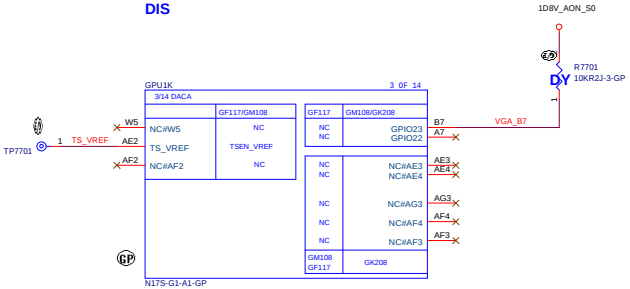

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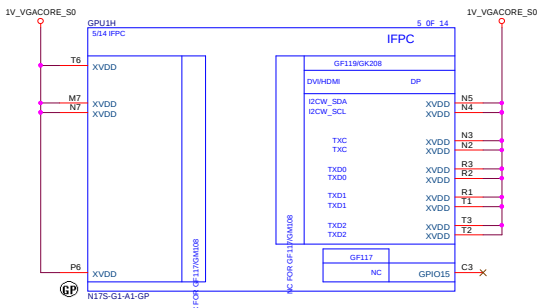

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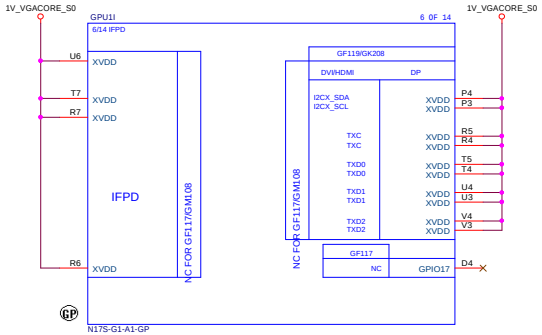

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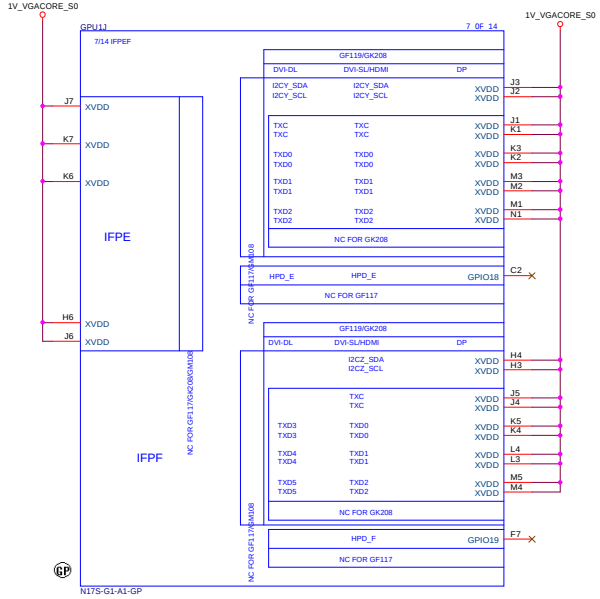

DIS

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Title: GPU (DIGITAL 2/5)		
Size: A2	Document Number: C550-ICL	Rev: SC
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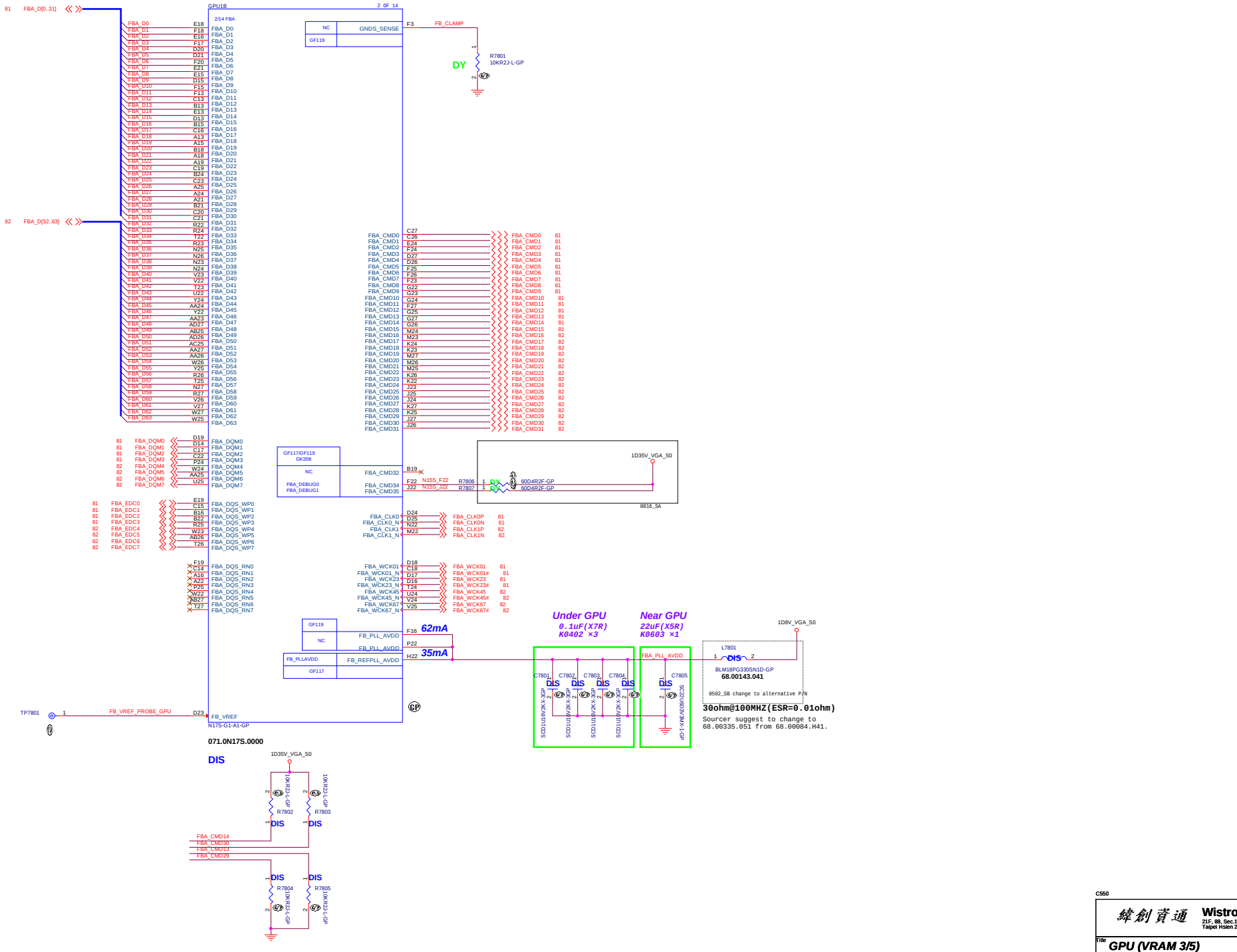

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Title: GPU (VRAM 3/5)

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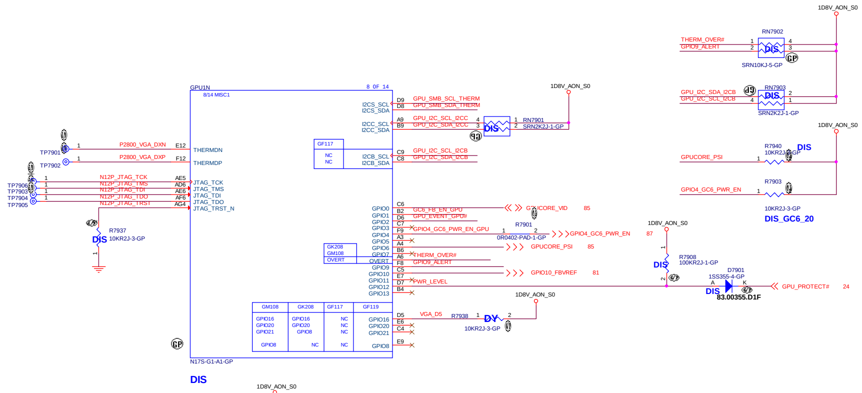
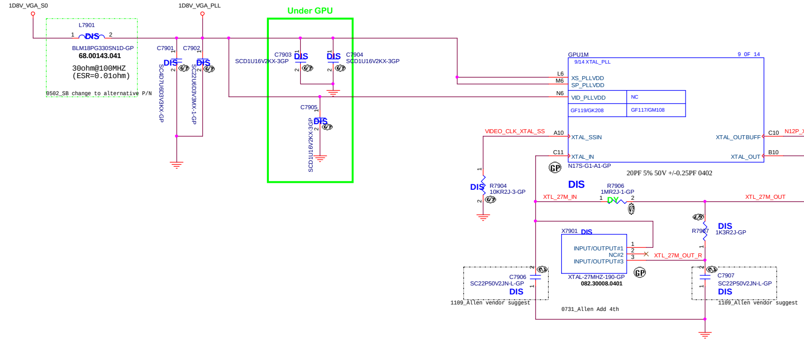
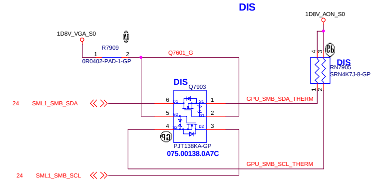
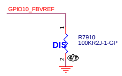
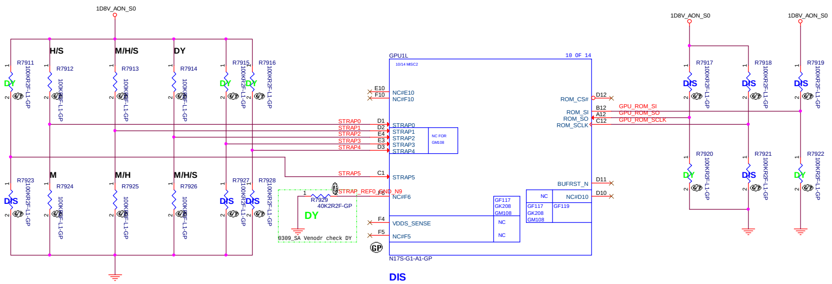
Main Func = dGPU

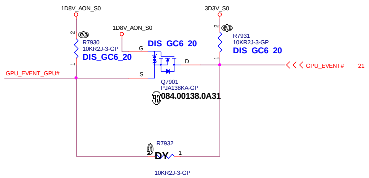


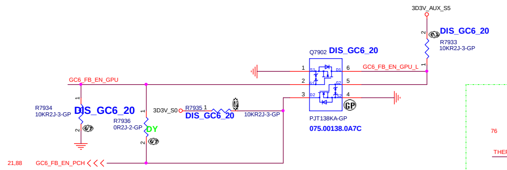












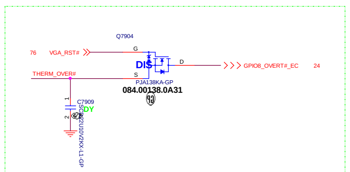


Table 4. N17S-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

GDDR5 - 256Mx32/512Mx16, 1.5V/1.55V 8Gbps / 1.35V 7Gbps		Hynix	900851-372	H5GC8H24AJR-R2C	A	19nm
GDDR5 - 256Mx32/512Mx16, 1.55V 8Gbps / 1.35V 6.5Gbps	195092	Samsung	900851-971	K4G80325FB-HC25	B	20nm
GDDR5 - 256Mx32/512Mx16, 1.5V/1.55V 8Gbps / 1.35V 7Gbps		Micron	900851-672	MT51J256M32HF-80:B	B	17nm

GDDR5 RAM_CFG

GPU SKU	GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Number	Die Revision	Memory Speed CK Grad	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
	N17S-G0/G2/G3/G4	GDDR5	1.35V	8Gb	256Mx32 512Mx16	Micron	MT51J256M32HF-80:B	B-die	8 Gbps	N/A	0x9	L	M	L	Prodution ready
						Hynix	H5GC8H24AJR-R2C	A-die	8 Gbps	N/A	0xA	L	M	H	Prodution ready
						Samsung	K4G80325FC-HC25	C-die	8 Gbps	N/A	0x3	L	H	H	Post-Prodution ready

STRAP0	STRAP1	STRAP2	Wisrton PN	Vendor
L	M	L	SV20R09096	Micron
H	M	L	SV20R09095	Hynix
H	H	L	SV20T35751	Sumsung

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

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Title: GPU (GPIO 4/5)

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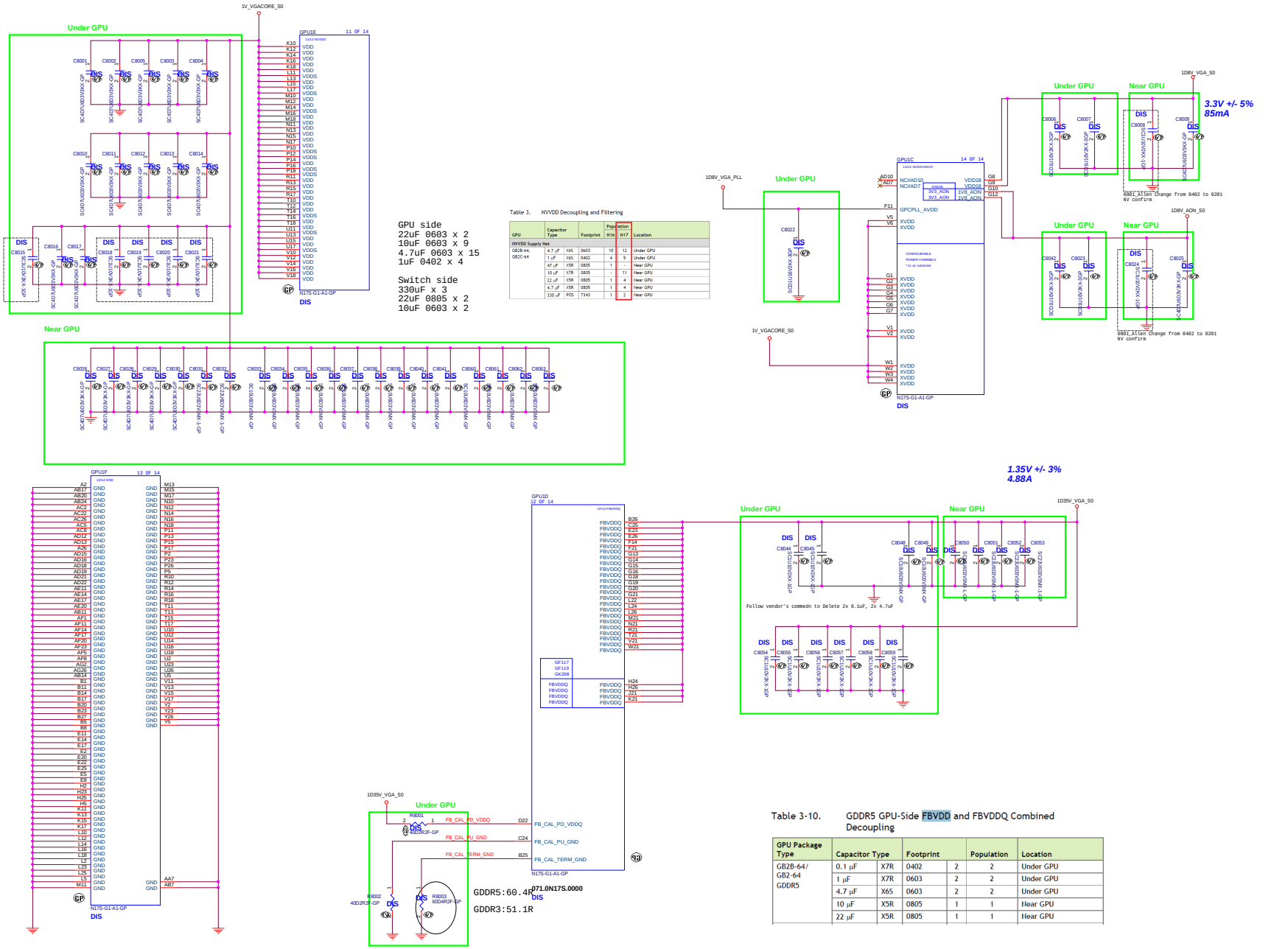

GPU side
22uF 0603 x 2
10uF 0603 x 9
4.7uF 0603 x 15
1uF 0402 x 4

Switch side
330uF x 3
22uF 0805 x 2
10uF 0603 x 2

Table 3. NVVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
NVVDD Supply Net					
GB2B-64, G82C-64	4.7 µF	X6S	0603	10	12	Under GPU
	1 µF	X6S	0402	4	5	Under GPU
	47 µF	X5R	0805	1	-	Near GPU
	10 µF	X7R	0805	-	11	Near GPU
	22 µF	X5R	0805	1	4	Near GPU
	4.7 µF	X5R	0805	1	4	Near GPU
	330 µF	POS	7343	1	2	Near GPU

Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint		Population	Location
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

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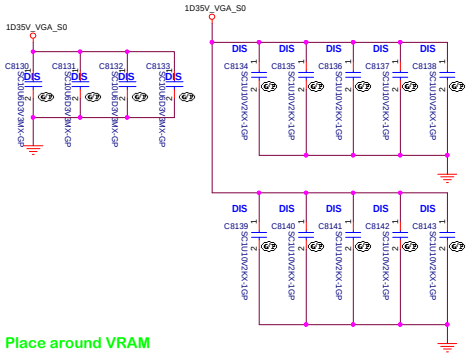
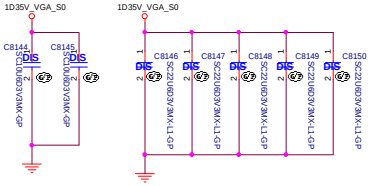
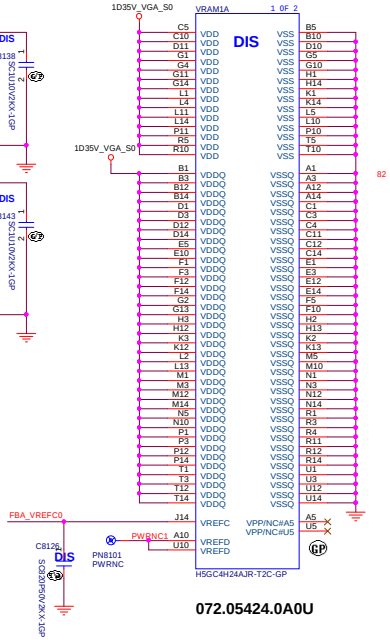
Place under VRAM VDD and VDDQ ball



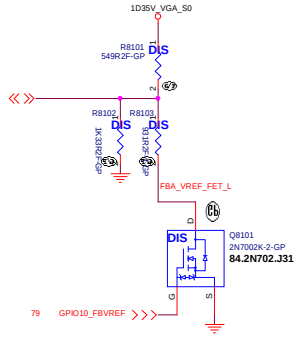
Place around VRAM





072.05424.0A0U

Frame Buffer Patition A-Lower Half

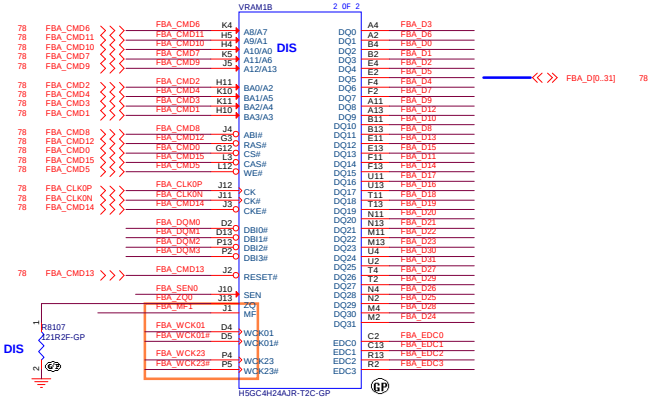


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Place close to each VRAM

Normal(MF=0)



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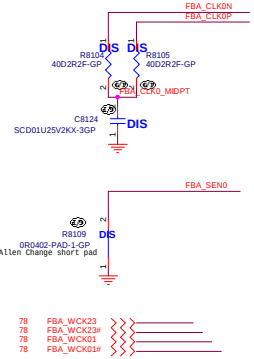

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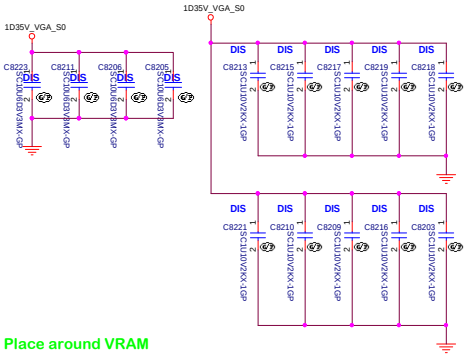
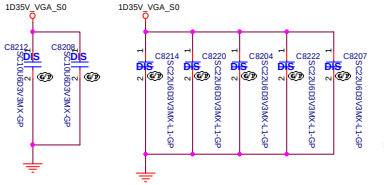
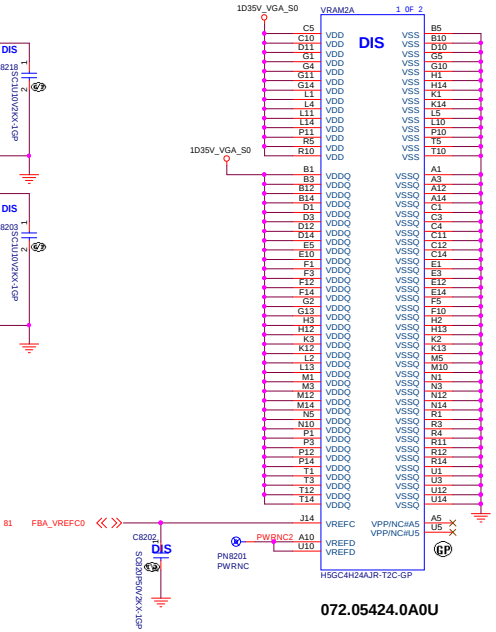
Place under VRAM VDD and VDDQ ball



Place around VRAM





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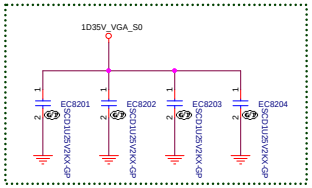
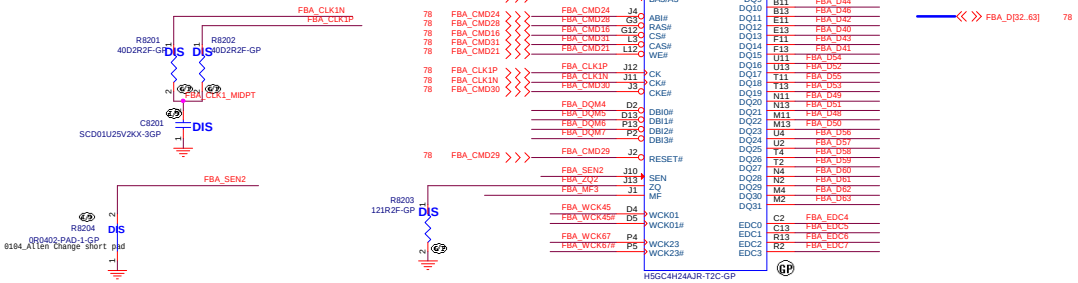
SIT EMC request: Bottom



Place close to each VRAM

Normal(MF=0)



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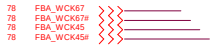

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Title: GPU (VRAM2 2/2)

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Title: ***GPU (RSVD)***

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Title: *GPU (RSVD)*

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OFFPAGE

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PH on EE side

79 GPUCORE_VID

79 GPUCORE_PSI

NVDDSGND_SENSE

76 GPUGND_SENSE

76 GPUCORE_SENSE

NVVDDS_SENSE

87,88 PWR_VGA_NVVDD_PG

87,88 PWR_DGPU_VR_EN

RT8816B For VGACORE

VGA : N17S-G0/1
EDP-Continuous : 28A
EDP-Peak : 60.4A

Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

VGA : N17S-G0/G1
EDP-Continuous : 28A
EDP-Peak : 60.4A

ID:31/54A ,
Rdson: 6.8~8.6/2.8~3.5m (Q1/Q2)

1st = 075.36354.0073

Cyntec. 6.86 x 6.47 x 3.0mm
DCR: 0.66 +- 7% mOhm
Idc : 36A , Isat : 41A

OCP setting

73.2K -> OCP = 90A

SS setting

Place Near GPU (NVVDD5)
1X330uF (Poscap) - PT8511 (Page85)

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Title	GPU (RT8816B_VGA)
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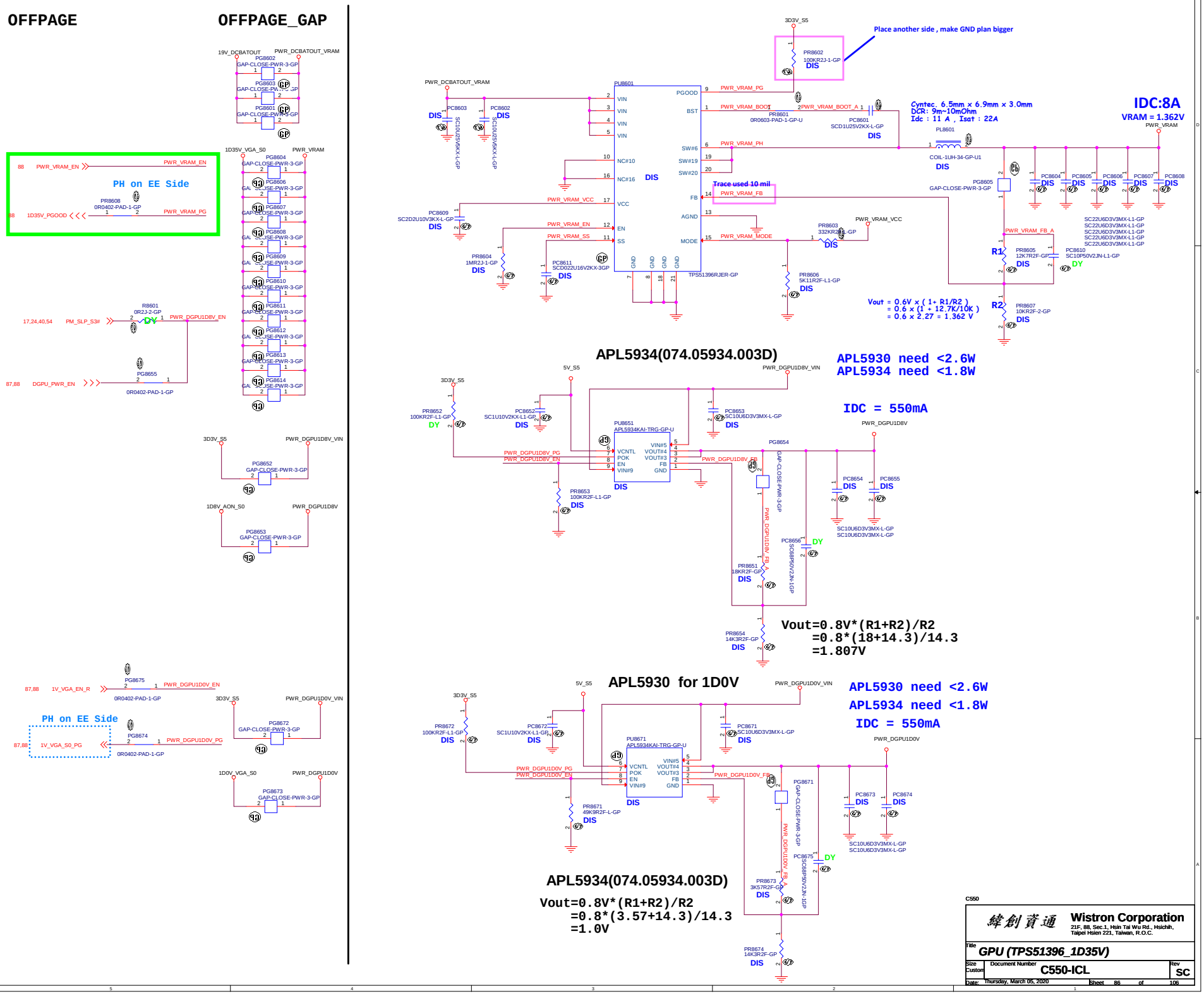
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19V_DCBATOUT
PWR_DCBATOUT_VRAM
PG8602
PG8603
PG8601
GAP-CLOSE-PWR-3-GP
1D35V_VGA_S0
PWR_VRAM
PG8604
PG8606
PG8607
PG8608
PG8609
PG8610
PG8611
PG8612
PG8613
PG8614
88
PWR_VRAM_EN
PH on EE Side
PR8608
0R0402-PAD-1-GP
1D35V_PGOOD
PWR_VRAM_PG
R8601
0R2J-2-GP
DY
17,24,40,54
PM_SLP_S3#
PWR_DGPU1D8V_EN
PG8655
87,88
DGPU_PWR_EN
0R0402-PAD-1-GP
3D3V_S5
PWR_DGPU1D8V_VIN
PG8652
1D8V_AON_S0
PWR_DGPU1D8V
PG8653
PG8675
1V_VGA_EN_R
PWR_DGPU1D0V_EN
PG8672
PG8674
1V_VGA_S0_PG
PWR_DGPU1D0V_PG
1D0V_VGA_S0
PWR_DGPU1D0V
PG8673
Place another side , make GND plan bigger
PR8602
100KR2J-1-GP
DIS
PWR_DCBATOUT_VRAM
PC8603
PC8602
SC10U25V5KX-L-GP
PU8601
VIN
NC#10
NC#16
VCC
EN
SS
AGND
MODE
PGOOD
BST
SW#6
SW#19
SW#20
FB
GND
TPS51396RJER-GP
PWR_VRAM_PG
PWR_VRAM_BOOT_A
PR8601
0R0603-PAD-1-GP-U
PC8601
SCD1U25V2KX-L-GP
PWR_VRAM_PH
PL8601
COIL-1UH-34-GP-U1
Cyntec, 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A
IDC:8A
VRAM = 1.362V
PWR_VRAM
Trace used 10 mil
PWR_VRAM_FB
PWR_VRAM_VCC
PWR_VRAM_EN
PWR_VRAM_SS
PWR_VRAM_MODE
PC8609
SC2D2U10V3KX-L-GP
PR8604
1MR2J-1-GP
PC8611
SCD022U16V2KX-3GP
PR8603
332KR2F-L-GP
PR8606
5K11R2F-L-L1-GP
PG8605
GAP-CLOSE-PWR-3-GP
PC8604
PC8605
PC8606
PC8607
PC8608
SC22U6D3V3MX-L1-GP
PWR_VRAM_FB_A
R1
PR8605
12K7R2F-GP
PC8610
SC10P50V2JN-L1-GP
R2
PR8607
10KR2F-2-GP
Vout = 0.6V x (1+ R1/R2)
= 0.6 x (1 + 12.7K/10K)
= 0.6 x 2.27 = 1.362 V
APL5934(074.05934.003D)
APL5930 need <2.6W
APL5934 need <1.8W
IDC = 550mA
5V_S5
PWR_DGPU1D8V_VIN
PR8652
100KR2F-L1-GP
PC8652
SC1U10V2KX-L1-GP
PC8653
SC10U6D3V3MX-L-GP
PU8651
APL5934KAI-TRG-GP-U
VCNTL
POK
EN
VIN#9
VIN#5
VOUT#4
VOUT#3
FB
GND
PWR_DGPU1D8V_PG
PWR_DGPU1D8V_EN
PWR_DGPU1D8V_FB
PR8653
100KR2F-L1-GP
PG8654
GAP-CLOSE-PWR-3-GP
PWR_DGPU1D8V
PC8654
PC8655
SC10U6D3V3MX-L-GP
PC8656
SC680P50V2JN-1GP
PR8651
18KR2F-GP
PR8654
14K3R2F-GP
Vout=0.8V*(R1+R2)/R2
=0.8*(18+14.3)/14.3
=1.807V
APL5930 for 1D0V
PR8672
100KR2F-L1-GP
PC8672
SC1U10V2KX-L1-GP
PC8671
SC10U6D3V3MX-L-GP
PU8671
APL5934KAI-TRG-GP-U
PWR_DGPU1D0V_PG
PWR_DGPU1D0V_EN
PWR_DGPU1D0V_FB
PR8671
49K9R2F-L-GP
PG8671
GAP-CLOSE-PWR-3-GP
PWR_DGPU1D0V
PC8673
PC8674
SC10U6D3V3MX-L-GP
PC8675
SC680P50V2JN-1GP
PR8673
3K57R2F-GP
PR8674
14K3R2F-GP
APL5930 need <2.6W
APL5934 need <1.8W
IDC = 550mA
APL5934(074.05934.003D)
Vout=0.8V*(R1+R2)/R2
=0.8*(3.57+14.3)/14.3
=1.0V
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Title
GPU (TPS51396_1D35V)
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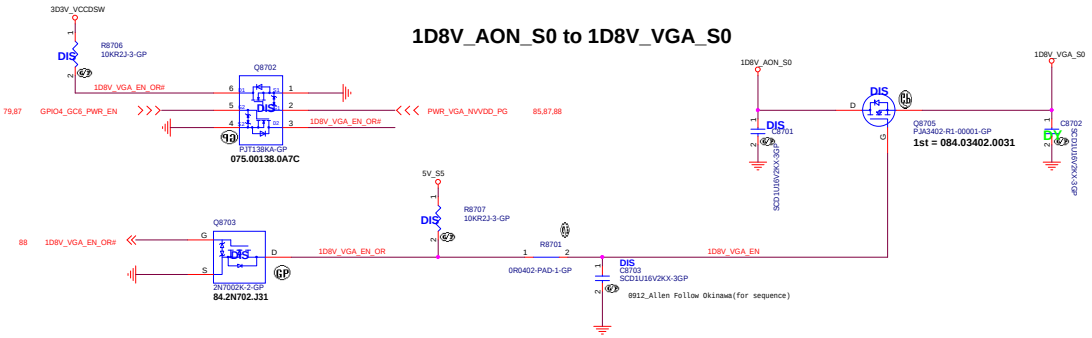

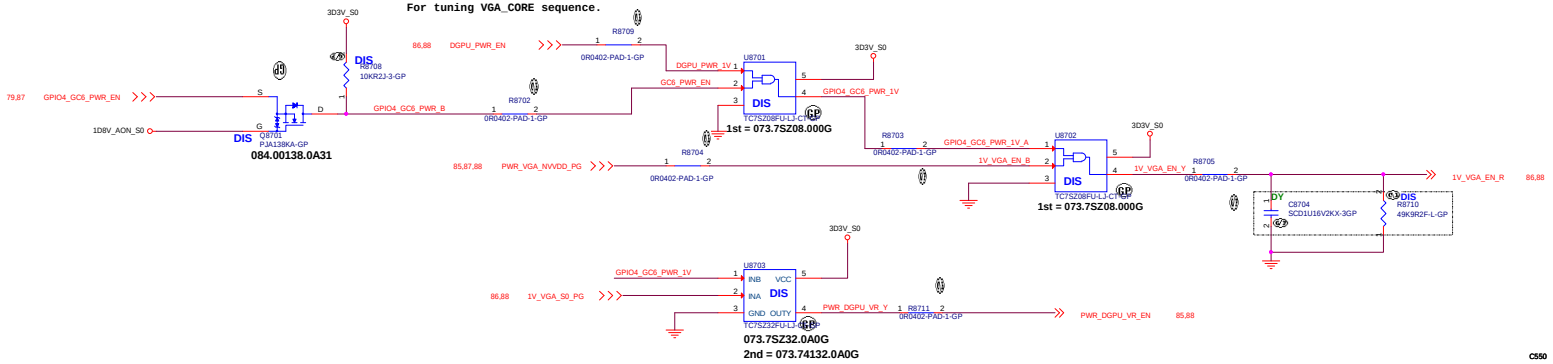

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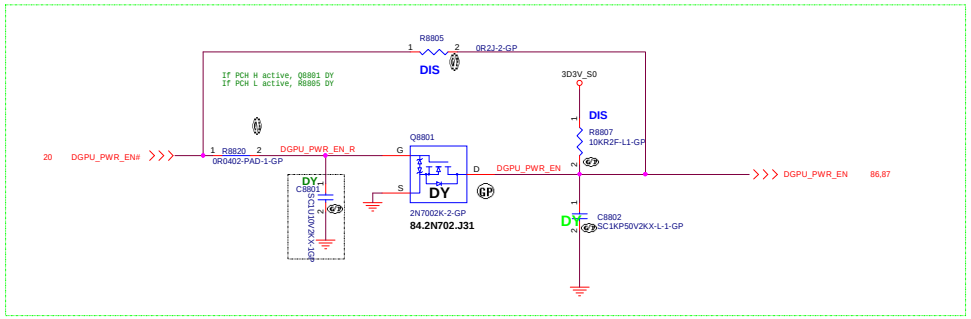
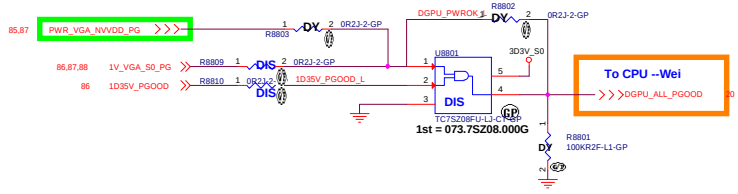
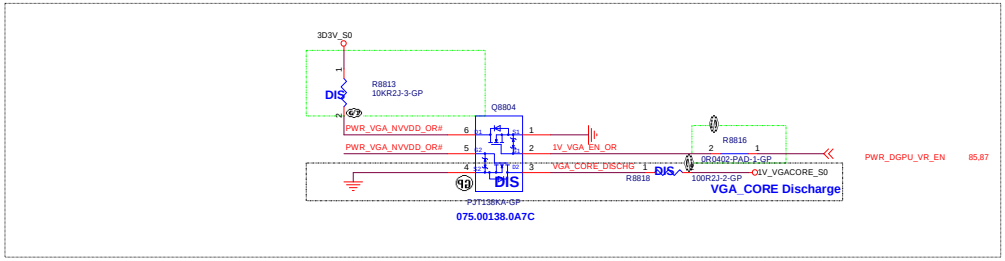
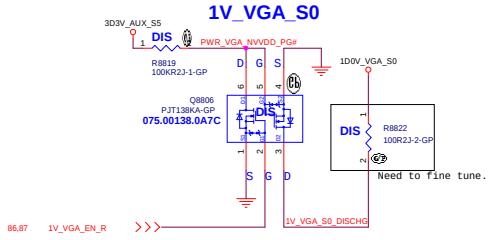
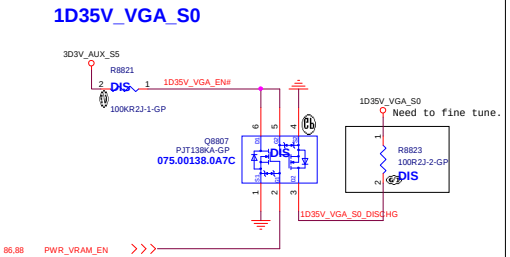


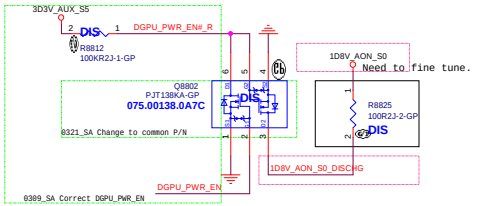


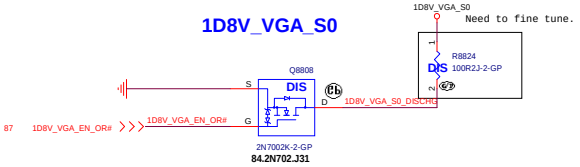


dGPU Power Discharge Circuit









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Title: GPU (DISCHARGE/SEQUENCE)		
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ZZ.00PAD.EJ1 H1 HOLE237R103-GP

ZZ.00PAD.QN1 H2 HOLE158R103-GP

ZZ.00PAD.EJ1 H3 HOLE237R103-GP

ZZ.00PAD.EJ1 H4 HOLE237R103-GP

ZZ.00PAD.EJ1 H5 HOLE237R103-GP

ZZ.00PAD.QN1 H6 HOLE158R103-GP

ZZ.SCREW.1A1 H8 HOLE197R111-GP

ZZ.SCREW.1A1 H9 HOLE197R111-GP

ZZ.00PAD.QN1 H12 HOLE158R103-GP

ZZ.00PAD.6N1 H13 HOLE197R67-GP

ZZ.00PAD.6N1 H14 HOLE197R67-GP

434.07K0E.0001 HS1 STF237R113H86-GP

34.4EO02.001 HS2 STFT236B142R128H43-1-GP

34.4SE26.001 HS3 STF237R113H62-4-GP

34.4SE26.001 HS4 STF237R113H62-4-GP

34.4SE26.001 HS5 STF237R113H62-4-GP

34.4SE26.001 HS6 STF237R113H62-4-GP

34.4SE26.001 HS7 STF237R113H62-4-GP

FVT EMC request: change to 0.1U

PWR_DCBATOUT_VCCAUX: EC8901, EC8902 SCD1U25V2KX-GP

PWR_DCBATOUT_5V: EC8903 SCD1U25V2KX-GP

PWR_DCBATOUT_3D3V: EC8904 SCD1U25V2KX-GP

PWR_DCBATOUT_VGACOREB: EC8905, EC8907 SCD1U25V2KX-GP

PWR_DCBATOUT_VGACOREA: EC8906, EC8908 SCD1U25V2KX-GP

PWR_DCBATOUT_VRAM: EC8911 SCD1U25V2KX-GP

19V_DCBATOUT: EC8909, EC8910, EC8912, EC8913, EC8914, EC8915, EC8916, EC8917, EC8918, EC8919, EC8920, EC8921, EC8922, EC8923 SCD1U25V2KX-GP

SIT EMC request: TOP

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Title: UNUSED PARTS (RF/EMI CAP)

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Title: ***INT IO (RSVD)***

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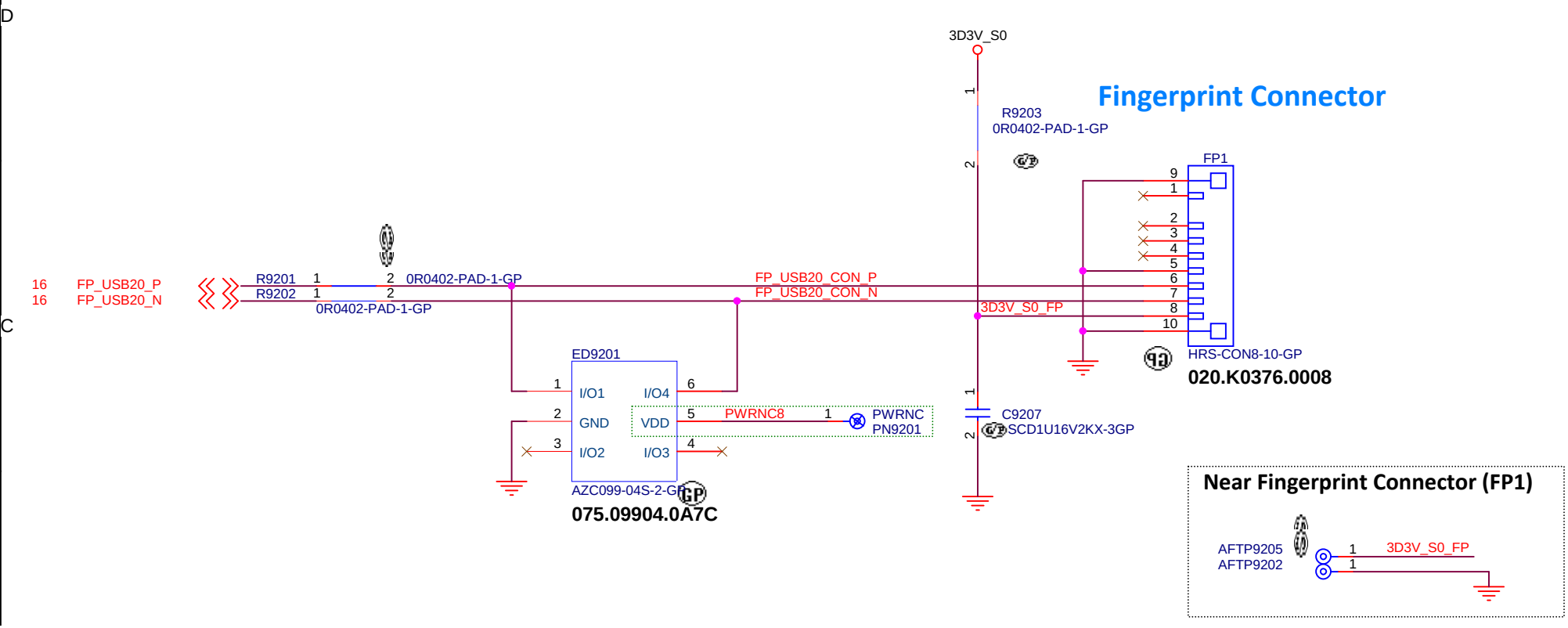

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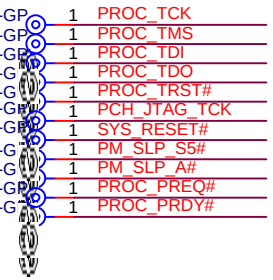
3	PROC_TCK
3	PROC_TDI
3	PROC_TDO
3	PROC_TMS
3	PROC_TRST#
3	PCH_JTAG_TCK
17	SYS_RESET#
17	PM_SLP_S5#
17	PM_SLP_A#
3	PROC_PREQ#
3	PROC_PRDY#



TP9901	TPAD14-OP-GP	1	PROC_TCK
TP9902	TPAD14-OP-GP	1	PROC_TMS
TP9903	TPAD14-OP-GP	1	PROC_TDI
TP9904	TPAD14-OP-G	1	PROC_TDO
TP9905	TPAD14-OP-G	1	PROC_TRST#
TP9906	TPAD14-OP-GP	1	PCH_JTAG_TCK
TP9907	TPAD14-OP-GP	1	SYS_RESET#
TP9908	TPAD14-OP-G	1	PM_SLP_S5#
TP9909	TPAD14-OP-G	1	PM_SLP_A#
TP9910	TPAD14-OP-GP	1	PROC_PREQ#
TP9911	TPAD14-OP-G	1	PROC_PRDY#

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Title: ***DEBUG (XDP/DCI)***

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Title **CHANGE HISTORY**

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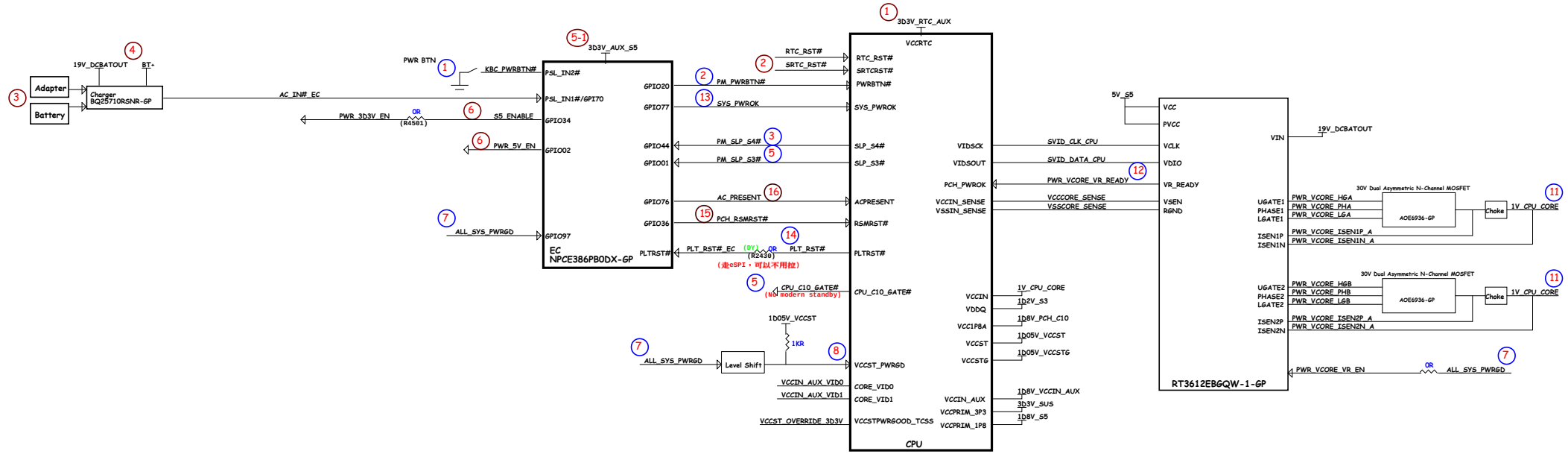
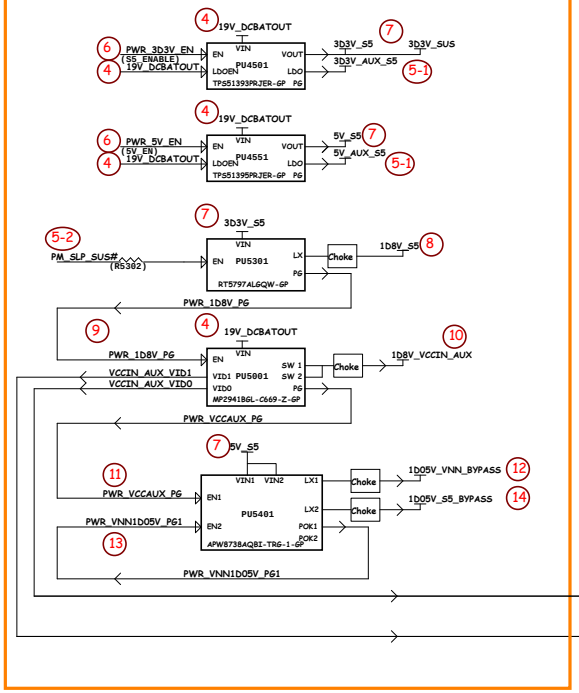
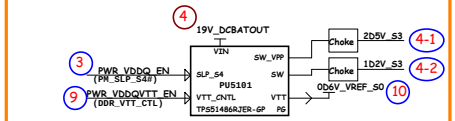
LC55 ICL SEQUENCE & BLOCK DIAGRAM



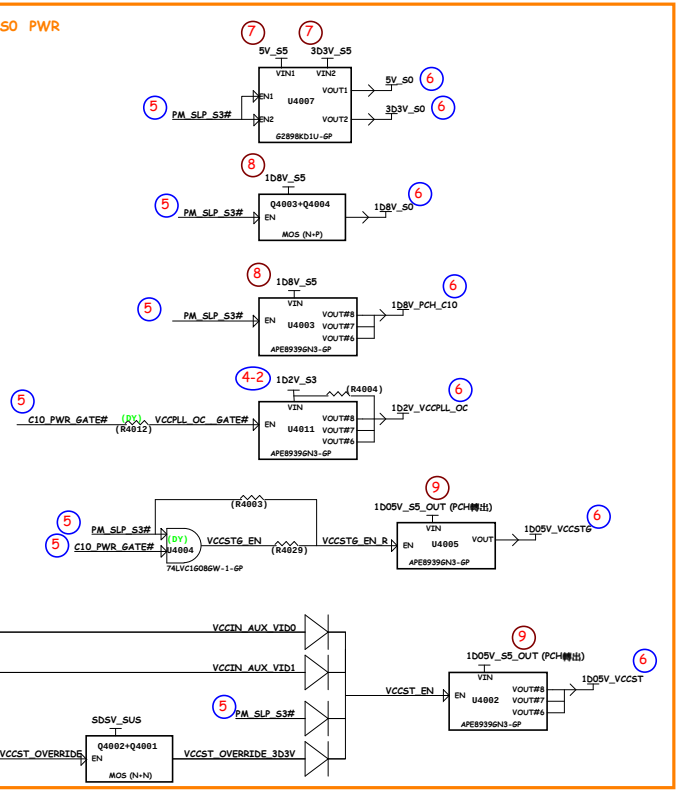
S5 PWR

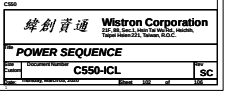


S3 PWR

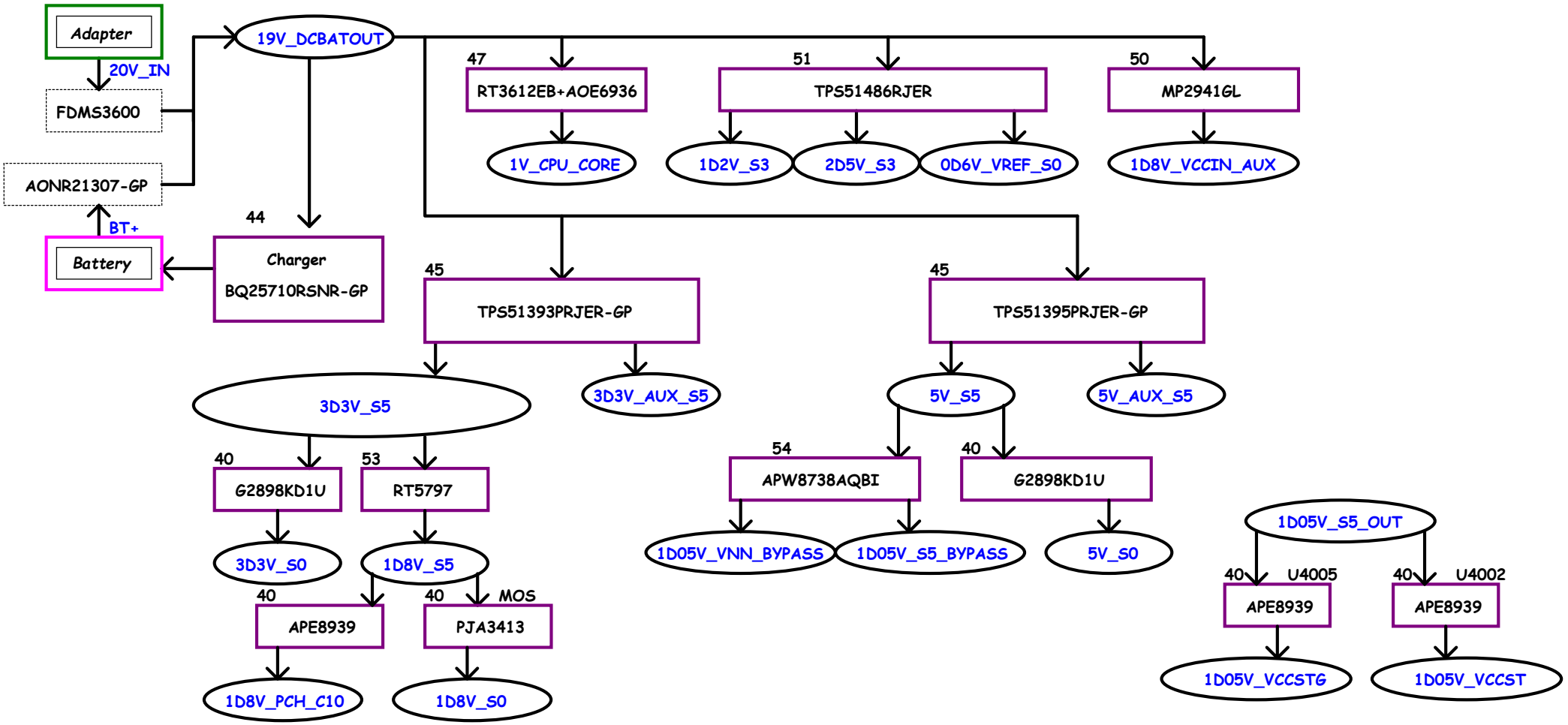


S0 PWR





LC55 ICL Power Block Diagram



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Title: POWER BLOCK DIAGRAM

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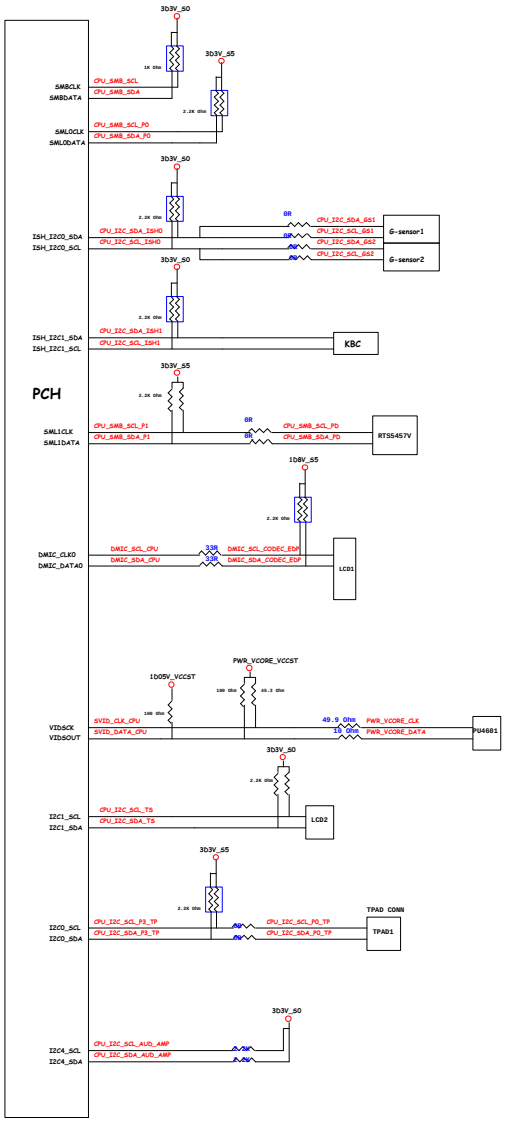
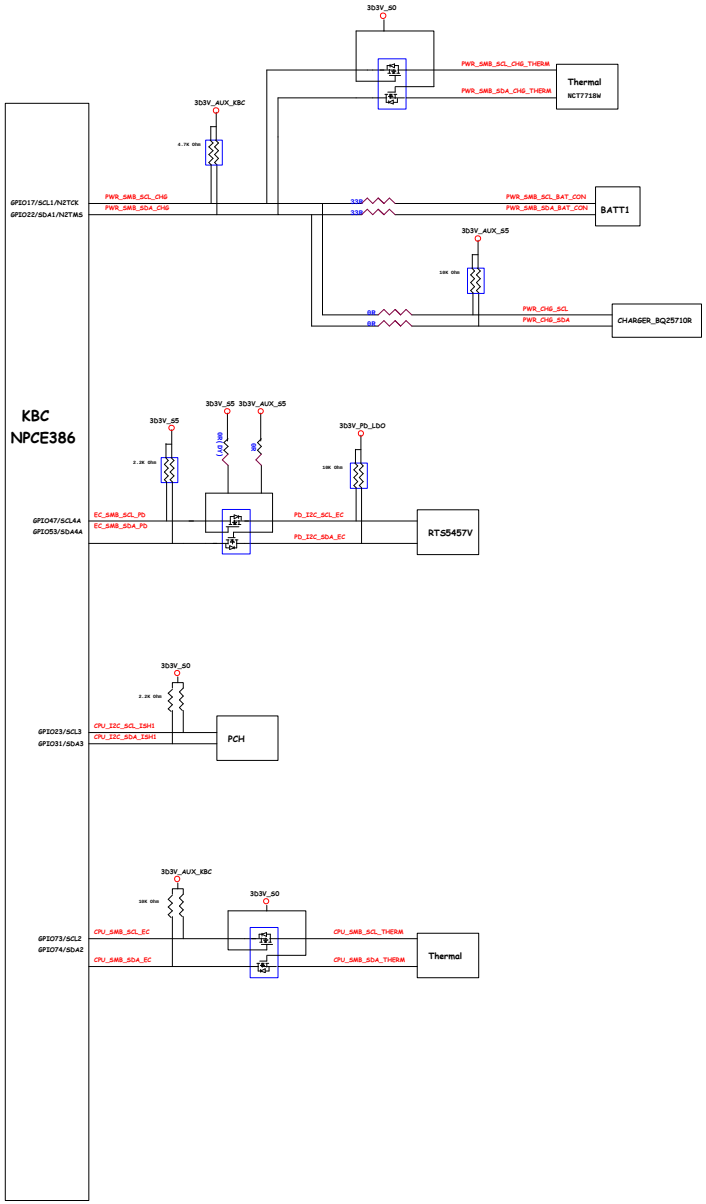
LC55 ICL SMBUS/I2C BLOCK DIAGRAM

PCH SMBus Block Diagram



KBC SMBus Block Diagram



Wistron Corporation	SMBUS/I2C BLOCK DIAGRAM		
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Title: ***THERMAL/AUDIO BLOCK DIAGRAM***

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Title **CLK BLOCK**

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