SYSTEM PAGE REF.

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	002_System Setting
	003_CPU_DISPLAY
	004_CPU_DDR4
	005_CPU_LPC,SPI,SMB,CLINK
	006_CPU_POEWR
	008_CPU_MISC,JTAG
	009_CPU_CFG,RSVD
	010_CPU_POWER_CAP
	016_DDR4_SO-DIMM_A_REV
	017_DDR4_SO-DIMM_B_STD
	018_DDR4_CA_DQ_VOLTAGE
	019_DDR4
	020_CPU_PCH_CSI2,EMMC
	021_CPU_PCH_CGPIO, LPIO, MISC
	022_CPU_PCH_AUDIO,SDIO,SDXC
	023_CPU_PCH_PCIE,USB,SATA
	024_CPU_PCH_CLOCK SIGNALS,RTC
	025_CPU_PCH_SYS_POWER
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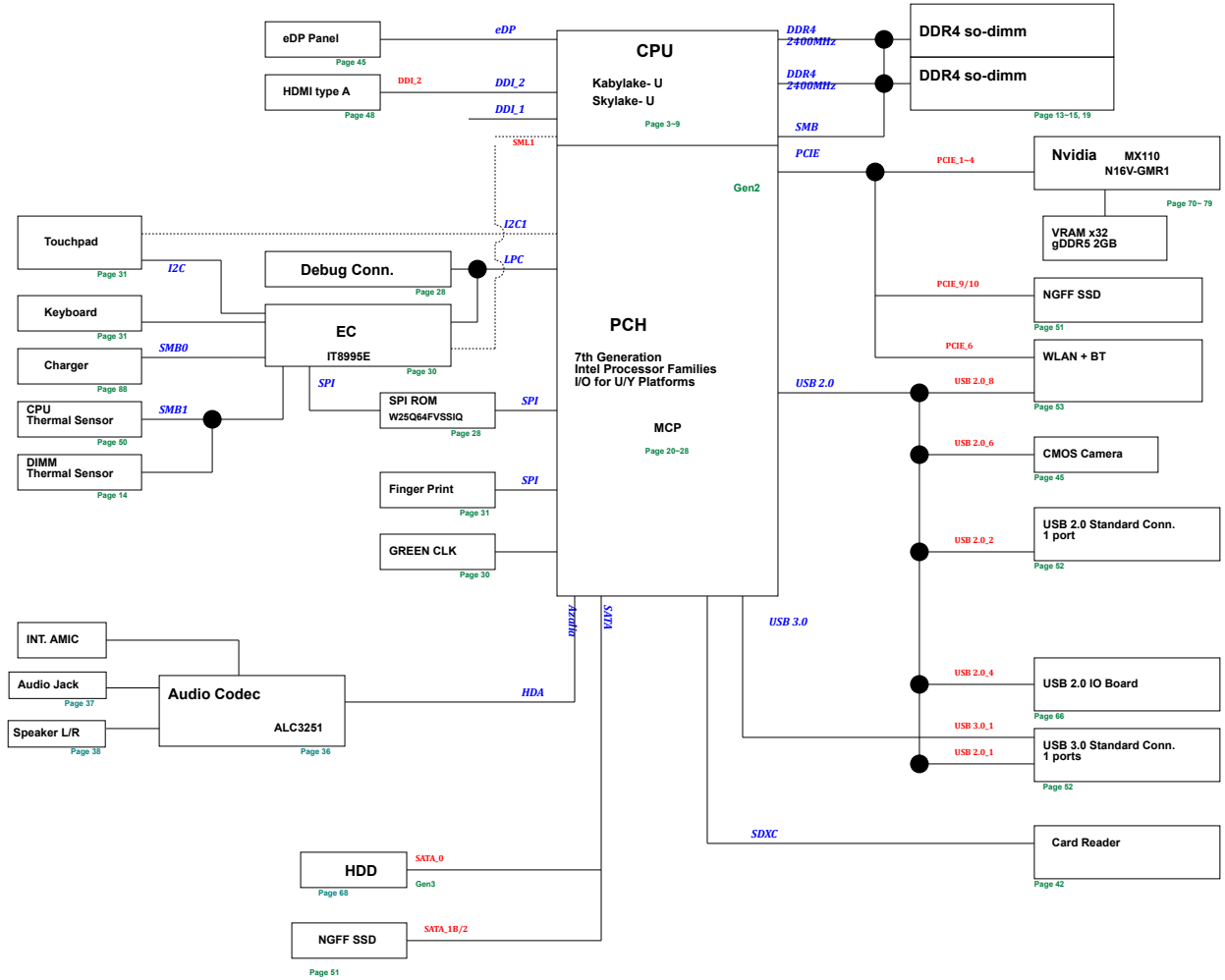
	027_CPU_PCH_POEWR,GND
	028_PCH-SPI ROM,OTH /DEBUG PORT
	029_Silego_Green_CLK_Gen
	030_KBC_IT8995E-128/DX
	031_KBC_KB,TP,KB-light,FP
	032_RST_Reset Circuit
	036_AUD-ALC3251
	037_AUD-HEADPHONE JACK
	038_AUD_SPEAKER
	042_CardReader Connector
	045_eDP Connector
	048_HDMI-type A
	050_FAN_Thermal Seneor
	051_NGFF(KEY-M)_SSD
	052_USB 3.0 + 2.0 CONN
	053_NGFF(KEY-E)_WLAN
	057_DSG_Discharge
	058_PRO_Protect
	059_Power & WIFI & CAP LED&LID
	060_DC_DC & BAT IN
	064_
	065_ME_Conn & Skew Hole
	066_USB IO Board
	067_
	068_HDD B2BConnector
	069_EMI
	070_VGA_nVIDIA_N16V/S_PCIE
	071_VGA_nVIDIA_N16V/S_FB-IF
	072_VGA_nVIDIA_N16V/S_FB-GDDR5
	073_VGA_nVIDIA_N16V/S_VDD
	074_VGA_nVIDIA_N16V/S_DISPLAY
	075_VGA_nVIDIA_N16V/S_ROM,XTAL
	076_VGA_nVIDIA_N16V/S_GPIO
	077_VGA_nVIDIA_N16V/S_POWER

080_PW_IMVP8 (1) (RT3601BCGQW)
081_PW_IMVP8 (2) (RT3601BCGQW)
083_PW_+1.0VSUS / +1.8VSUS
086_PW_1.2V/+VTT/+2.5
087_PW_+3VADSW/+5VSUS (RT8249C)
088_PW_LOAD SWITCH
089.PW_CHARGER(BQ24780)
090_PW_PROTECTION
091_PW_+NVVDD
093_PW_+FBVDDQ

BLOCK DIAGRAM

X507 UAR/UBR SCHEMATIC Revision1.0

Non Connected Standby



Power

+VCCGT +VCCSA
+VCCCORE
+VCCST
Page 80 & 81

+1.0VSUS / +1.8VSUS
Page 83

+0.95VSG
+VCCPRIM_CORE
Page 84

+1.2V / +VTT / +2.5V
Page 86

+3VADSW/+5VSUS
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Load Switch
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Charger
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+VDDC
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+FBVDDQ
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CPU XDP
Page 7

Discharge Circuit
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DC & BATT. Conn.
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Reset Circuit
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Skew Holes
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BOM

ASUS Project Name: X507UA/UV
Rev: R1.0
Title : Block Diagram
Size: Custom
Dept.: ASUSTeK COMPUTER INC
Engineer: Bull Tsai
Date: Friday, April 13, 2018
Sheet 1 of 102

PCH_CPT GPIO

	PCH_IHBX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	
	GPP_A0	Native1	BC_INT		EXT PU 10K	+3VS	PU at EC
	GPP_A1	Native1	LPC_AD0				
	GPP_A2	Native1	LPC_AD1				
	GPP_A3	Native1	LPC_AD2				
	GPP_A4	Native1	LPC_AD3				
	GPP_A5	Native1	LPC_FRAME#				
	GPP_A6	Native1	INT_SERIRQ		EXT PU 10K	+3VS	
	GPP_A7	GPO	PCI_INTA#		EXT PU 10K	+3VS	
	GPP_A8	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS	
	GPP_A9	Native1	CLK_KBCPCI_PCH				
	GPP_A10	Native	CLK_DEBUG				
For 555 N/A	GPP_A11	GPI	N/A	需確認是否具wake 功能			
	GPP_A12	GPO	N/A				
	GPP_A13	Native1	SUSWARN#		EXT PU 10K	+3VSUS	
	GPP_A14	Native1	PCH_SUS_STAT#				
Need Add EC	GPP_A15	Native1	PCH_SUSACK#				
For 555 N/A	GPP_A16	Native1	N/A (SD_1P8_SEL)		PD 49.9K		
For 555 N/A	GPP_A17	Native1	N/A (SD_PWR_EN#)				
	GPP_A18	GPO	N/A				
	GPP_A19	GPO	N/A				
	GPP_A20	GPO	N/A				
	GPP_A21	GPO	N/A				
	GPP_A22	GPO	N/A				
	GPP_A23	GPO	N/A				
For 555 N/A	GPP_B0	Native	N/A (VCCPRIM_VID0)		EXT PU 10K	+3VS	
For 555 N/A	GPP_B1	Native	N/A (VCCPRIM_VID1)		EXT PU 10K	+3VS	
	GPP_B2	GPO	N/A				
	GPP_B3	GPO	N/A				
	GPP_B4	GPO	N/A				
	GPP_B5	Native	CK_REQ_P0# DGPU		EXT PU 10K	+3VS	
	GPP_B6	Native	CK_REQ_P1#				
	GPP_B7	Native	CK_REQ_P2# SSD		EXT PU 10K	+3VS	
	GPP_B8	Native	CK_REQ_P3#				
	GPP_B9	Native	CK_REQ_P4#				
	GPP_B10	Native	CK_REQ_P5# WLAN		EXT PU 10K	+3VS	
	GPP_B11	Native	MPHY_PWREN (N/A)		EXT PU 20K	+3VSUS	
	GPP_B12	Native	PCH_SLP_SO_R#				
	GPP_B13	Native	PLT_RST#				
	GPP_B14	GPO	PCH_GPPB14				
For 555 N/A	GPP_B15	Native	FP_GSPI0_CS#				
For 555 N/A	GPP_B16	Native	FP_GSPI0_CLK				
For 555 N/A	GPP_B17	Native	FP_GSPI0_MISO				
	GPP_B18	Native	FP_GSPI0_MOSI				
	GPP_B19	GPO	BT_ON/OFF# GSPI1_CS_R#				
	GPP_B20	GPO	GPU_EVENT#		EXT PU 10K	+3VSG	
	GPP_B21	GPI	DGPU_FB_CLAMP_GPIO		EXT PD 10K	PU at DGPU	
	GPP_B22	GPO	PCH_GPPB22				
	GPP_B23	Native	SML1ALERT#		EXT PU 150K	+3VSUS	
	GPP_C0	Native	SMB_CK		EXT PU 2.2K	+3VSUS	
	GPP_C1	Native	SMB_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C2	GPO	GPP_C2				
For 555 N/A	GPP_C3	Native	SML0_CK		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C4	Native	SML0_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C5	GPO	GPP_C5				
	GPP_C6	Native	SML1_CK		EXT PU 2.2K	+3VSUS	
	GPP_C7	Native	SML1_DATA		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C8	GPO	N/A (PCH_GPPC8)				
For 555 N/A	GPP_C9	GPO	N/A (PCH_GPPC9)				
For 555 N/A	GPP_C10	GPO	N/A (PCH_GPPC10)				
For 555 N/A	GPP_C11	GPO	N/A (PCH_GPPC11)				
	GPP_C12	GPI	DIMM_SEL0		EXT PU 10K/ PD 10K	+3VSUS	
	GPP_C13	GPI	DIMM_SEL1		EXT PU 10K/ PD 10K	+3VSUS	
	GPP_C14	GPI	DIMM_SEL2		EXT PU 10K/ PD 10K	+3VSUS	
	GPP_C15	GPI	FP_RST#_GPIO				
	GPP_C16	GPO	I2C2_SDA_TCHPANEL(N/A)		EXT PU 4.7K	+3VS	
For 555 N/A	GPP_C17	GPO	I2C2_SCL_TCHPANEL(N/A)		EXT PU 4.7K	+3VS	
For X5410V N/A	GPP_C18	Native	I2C1_SDA_TCH_PAD		PU 4.7K	+3VS	
For X5410V N/A	GPP_C19	Native	I2C1_SCL_TCH_PAD		PU 4.7K	+3VS	
	GPP_C20	GPI	DGPU_PWROK		EXT PU 10K	+3VS	PU at DGPU
	GPP_C21	GPO	GPU_RST#				
	GPP_C22	GPO	DGPU_PWR_EN#		EXT PU 10K	+3VSUS	
	GPP_C23	GPI	TPanel_INT#		EXT PU 10K	+3VS	
	GPP_D0	GPO	N/A				
	GPP_D1	GPO	N/A				
	GPP_D2	GPO	N/A				
	GPP_D3	GPO	N/A				
For 555 N/A	GPP_D4	GPI	N/A				
	GPP_D5	GPO	SATA_ODD_PWRGT				
	GPP_D6	GPI	SATA_ODD_DA#				
	GPP_D7	GPO	N/A				
	GPP_D8	GPO	N/A				
	GPP_D9	GPI	PCB_ID0		EXT PD 10K		
For X5410V N/A	GPP_D10	GPI	SMIC_ID		EXT PD 10K		
	GPP_D11	GPI	TOUCHPAD_ID		EXT PD 10K		
	GPP_D12	GPI	TOUCH_PANEL_ID		EXT PD 10K		
	GPP_D13	GPI	TOUCHPAD_INTR#		EXT PU 10K	+3VS	
	GPP_D14	GPO	WLAN_LED_R				
X5410V Change	GPP_D15	GPO	SNSR_HUB_PWREN				
	GPP_D16	GPO	FP_INT#				
	GPP_D17	GPO	N/A				
	GPP_D18	GPO	N/A				
For 555 N/A	GPP_D19	Native	N/A				
For 555 N/A	GPP_D20	Native	N/A				
	GPP_D21	GPO	N/A				
	GPP_D22	GPO	N/A				

	PCH_IHBX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	
	GPP_D23	GPO	N/A				
	GPP_E0	NATIVE	DIRECT_ESATA_DETECT_R#		EXT PU 10K	+3VS	
	GPP_E1	NATIVE	SATA_ODD_PRSNT_R#		EXT PU 10K	+3VS	
	GPP_E2	NATIVE	MSATA_MPCIE_DET#		EXT PU 10K	+3VS	
	GPP_E3	GPO	N/A				
	GPP_E4	NATIVE	SATA0_DEVSLP				
	GPP_E5	GPO	N/A				
	GPP_E6	GPO	SATA2_DEVSLP				
	GPP_E7	GPO	N/A				
	GPP_E8	NATIVE	PCH_SATA_LED#		EXT PU 10K	+3VS	
	GPP_E9	GPIO	USB_OC_1_2#_R		EXT PU 10K	+3VSUS	
	GPP_E10	GPI	USB_OC_3_4#		EXT PU 10K	+3VSUS	
	GPP_E11	GPI	USB_OC_5_6#		EXT PU 10K	+3VSUS	
	GPP_E12	GPI	USB_OC_7_8#		EXT PU 10K	+3VSUS	
	GPP_E13	GPIO	N/A				
	GPP_E14	NATIVE	HDMI_HP		EXT PU 1M	+3VS	PD at HDMI conn
	GPP_E15	GPO	EXT_SMI#		EXT PU 10K	+3VS	
	GPP_E16	GPI	EXT_SCI# / EXT_SCI#_X1		EXT PU 10K	+3VS	
	GPP_E17	NATIVE	EDP_HPD_CON				
	GPP_E18	GPIO	DDPB_SCL_PCH				
	GPP_E19	GPIO	DDPB_SDA_PCH				
	GPP_E20	NATIVE	DDPC_SCL_PCH		EXT PU 2.2K	+3VS	PU at HDMI conn
	GPP_E21	NATIVE	DDPC_SDA_PCH		EXT PU 2.2K	+3VS	PU at HDMI conn
	GPP_E22	GPO	N/A				
	GPP_E23	GPO	N/A				
	GPP_F0	GPO	N/A				
	GPP_F1	GPO	N/A				
	GPP_F2	GPO	N/A				
	GPP_F3	GPO	N/A				
For X5410V ADD	GPP_F4	GPO	N/A				
For X5410V ADD	GPP_F5	GPO	N/A				
	GPP_F6	GPO	N/A				
	GPP_F7	GPO	N/A				
	GPP_F8	GPO	N/A				
	GPP_F9	GPO	N/A				
	GPP_F10	GPO	N/A				
	GPP_F11	GPO	N/A				
	GPP_F12	GPO	N/A				
	GPP_F13	GPO	N/A				
	GPP_F14	GPO	N/A				
	GPP_F15	GPO	N/A				
	GPP_F16	GPO	N/A				
	GPP_F17	GPO	N/A				
	GPP_F18	GPO	N/A				
	GPP_F19	GPO	N/A				
	GPP_F20	GPO	N/A				
	GPP_F21	GPO	N/A				
	GPP_F22	GPO	N/A				
	GPP_F23	GPO	N/A				
For 555 N/A	GPP_G0	Native	SDCMD		EXT PU 49.9K	+3VS	
For 555 N/A	GPP_G1	Native	SD-DATA0		EXT PU 49.9K	+3VS	
For 555 N/A	GPP_G2	Native	SD-DATA1		EXT PU 49.9K	+3VS	
For 555 N/A	GPP_G3	Native	SD-DATA2		EXT PU 49.9K	+3VS	
For 555 N/A	GPP_G4	Native	SD-DATA3		EXT PU 49.9K	+3VS	
For 555 N/A	GPP_G5	Native	SDCDN		EXT PU 49.9K	+3VS	
For 555 N/A	GPP_G6	Native	SDCLK		EXT PU 49.9K		
For 555 N/A	GPP_G7	Native	SDWP				
For 555 ADD	GPD0	Native	PM_BATLOW_R#		EXT PU 8.2K	+3VA_DSW	
	GPD1	Native	ME_AC_PRESENT_PCH		EXT PU 100K	+3VA_DSW	
	GPD2	GPI	PCH_GPD2#		EXT PU 10K	+3VA_DSW	
	GPD3	Native	PM_PWRBTN#				
For 555 ADD	GPD4	Native	PM_SUSB#		EXT PD 100K	PD at EC	
	GPD5	Native	PM_SUSC#		EXT PD 100K	PD at EC	
For 555 ADD	GPD6	Native	PM_SLP_A_R#				
	GPD7	GPO	WLAN_ON#				
For 555 N/A	GPD8	Native	NA (SUS_CK)				
	GPD9	Native	PCH_SLP_WLAN# (N/A)				
	GPD10	Native	SLP_S5# (N/A)				
	GPD11	Native	LAN_PWREN (N/A)				

EC IT8995 GPIO

	Pin Name	Config	Signal Name	Default status	Ext Pull up / down	Power
	GPA0	O	PWR_LED	LOW		
	GPA1	O	CHG_LED#	HIGH		
	GPA2	O	CHG_FULL_LED#	HIGH		
For 555 N/A	GPA3	O		LOW		
For 555 N/A	GPA4	O		LOW		
	GPA5	O	FAN1_PWM	LOW		
	GPA6	O		LOW		
For 555 N/A	GPA7	O		HIGH		
	GPB0	ADT ACIN#	AC_IN_OC#	LOW	EXT 10K PU	+3VA
	GPB1	I	LID_SW#	LOW	EXT 10K PU	+3VA
For 555 N/A	GPB2	O	(N/A)	LOW	EXT 10K PU	+3VA_EC
	GPB3	ADT PWRSW	PWR_SW#	LOW	EXT 10K PU	+3VA
	GPB4	I	PS_ON	HIGH		
For 555 N/A	GPB5	I	(N/A)	LOW		
	GPB6	O	BC_INT	LOW	EXT 10K PU	+3VS
For 555 N/A	GPC0	O	(N/A)	LOW		
	GPC1	ADT SMBCLK	SMB1_CLK	LOW	EXT 4.7K PU	+3VA_EC
	GPC2	ADT SMBDAT	SMB1_DAT	LOW	EXT 4.7K PU	+3VA_EC
	GPC3	O	PM_PWRBTN#	LOW		
For 555 N/A	GPC4	I	(N/A)	LOW	EXT 10K PU	+3VS
	GPC5	I	PM_SUSC#	LOW	EXT 100K PD	
	GPC6	Alt	BAT1_IN_OC#	LOW	EXT 10K PU	
For 555 N/A	GPC7	I	(N/A)	LOW		
	GPD0	O	PCH_SLP_S0#	LOW		
	GPD1	O	ME_AC_PRESENT	LOW	EXT 100K PU	+3VA_DSW
	GPD2	ADT LPCRST#	EC_RST_R#	LOW	EXT 100K PD	
	GPD3	O	EXT_SCI#	LOW	EXT 10K PU	+3VS
	GPD4	O	EXT_SMI#	LOW	EXT 10K PU	+3VS
	GPD5	O	GP_SCI#	HIGH		
	GPD6	ADT TACH	FAN2_TACH	LOW		
For 555 N/A	GPD7	O	(N/A)	LOW		
	GPE0	O	SUSB_EC#	LOW		
	GPE1	O	SUSC_EC#	LOW		
	GPE2	O	1.2V_ON	LOW		
	GPE3	O	N/A	LOW		
For 555 N/A	GPE4	O	(N/A)	HIGH		
	GPE5	O	PM_SUS3#	LOW	EXT 100K PD	
For 555 N/A	GPE6	O	(N/A)	HIGH		
	GPE7	O	THRO_CPU#	HIGH	EXT 1K PU	+VCCSTG
	GPF0	O	THRO_ON	LOW	EXT 10K PU/ 1M PD	+3VA_EC
	GPF1	O	VHUB_ON	LOW	EXT 100K PU	+3VA_EC
	GPF2	ADT SMBCLK	SMB2_CLK	LOW	EXT 4.7K PU	+3VA_EC
	GPF3	ADT SMBDAT	SMB2_DATA	LOW	EXT 4.7K PU	+3VA_EC
	GPF4	O	(N/A)	HIGH		
	GPF5	O	(N/A)	HIGH		
	GPF6	ADT PECI	PECI_EC	LOW		
	GPF7	O	PCH_SPI_OV	HIGH		
	GPG0	O	DGPU_LIMIT	LOW		
	GPG1	O	PCH_SUSACK#	HIGH		
	GPG2	I	PWRLIMIT_EC#	HIGH	EXT 100K PU	+3VA_EC
	GPG6	O	(N/A)	LOW		
	GPH0	ADT CLKRUN#	PM_CLKRUN#	LOW	EXT 8.2K PU	+3VS
For 555 N/A	GPH1	O	N/A	LOW		
For 555 N/A	GPH2	O	N/A	LOW		
	GPH3	O	PM_RSMRST#	LOW		
	GPH4	O	SUSWOK_EC	LOW	EXT 10K PD	
	GPH5	O	PM_PWROK	LOW	EXT 100K PD	
	GPH6	O	PM_SYSPWROK	LOW		
	GPH7	O	LCD_BACKOFF#	HIGH		
	GPI0	O	PM_SLP_S03#	LOW	EXT 10K PU/ PD 1K	+3VS
	GPI1	O	3VSUS_PWRGD	LOW		
	GPI2	O	ALL_SYSTEM_PWRGD	LOW	EXT 10K PU	+3VS
	GPI3	O	INVPB_PWRGD	LOW	EXT 10K PU	+3VS
	GPI4	O	3VA_DSW_PWRGD	LOW	EXT 100K PU	+3VA_DSW
	GPI5	O	SUSWARN#	LOW		
	GPI6	ADT ADC	A/D_MAX_POWER	LOW	EXT 0 PU	
	GPI7	ADT ADC	MB_MAX_POWER	LOW	EXT 100K PD/93.1K PU	+3VACC
	GPJ0	I	N/A	LOW		
VC lose	GPJ1	O	3VADSW_ON	LOW	EXT 100K PU	+3VA_EC
For 555 N/A	GPJ2	O	N/A	LOW		
	GPJ3	O	N/A	LOW		
For 555 N/A	GPJ4	O	N/A	LOW		
For 555 N/A	GPJ5	I	N/A	LOW		
For 555 N/A	GPJ6	O	N/A	LOW		
For 555 N/A	GPJ7	O	N/A	LOW		

*1: EC config GPI; Function output

Design IP Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
DIMM TEMP.	9Ah
CPU Thermal Sensor	90h

USB3 Port

USB3_1	USB 3.0 Port 0
USB3_2	
USB3_3	
USB3_4	

PCI Express

PCIE 1	DGPU
PCIE 2	
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	WLAN
PCIE 9	SSD
PCIE 10	
PCIE 11	
PCIE 12	

SATA Port

SATA 0	HDD
SATA 1	
SATA 2	SSD

PCI CLK

CLK0	DGPUx4
CLK1	
CLK2	SSD
CLK3	
CLK4	
CLK5	WLAN

USB Port

USB 1	USB 2.0 Port	USB 3.0 Port 0
USB 2	USB 2.0 Port	
USB 3		
USB 4	USB 2.0 Port	
USB 5		
USB 6	CAMERA	
USB 7	TOUCH_PANEL	
USB 8	WLAN/BT	
USB 9		
USB 10		

Device Identification

CPU Thermal Senser		
1st	060023123010	NCT7717U
2nd		

For X5400PR ADD

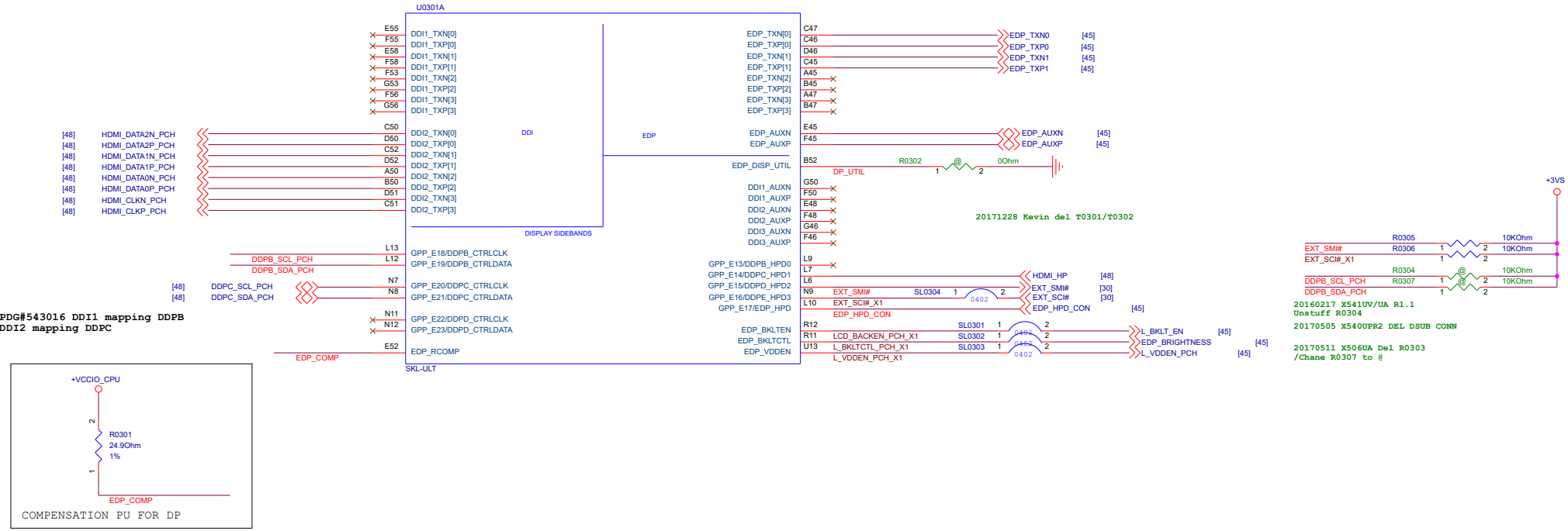
BOM

ASUS	Project Name: X507UA/UV	Rev: AH.1
Title :	System Setting	
Size: A	Dept.: AsiaSW.COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 2 of 102	

Display Port

A	EDP
B	
C	HDMI

Intel Version	ASUS P/N



PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPC

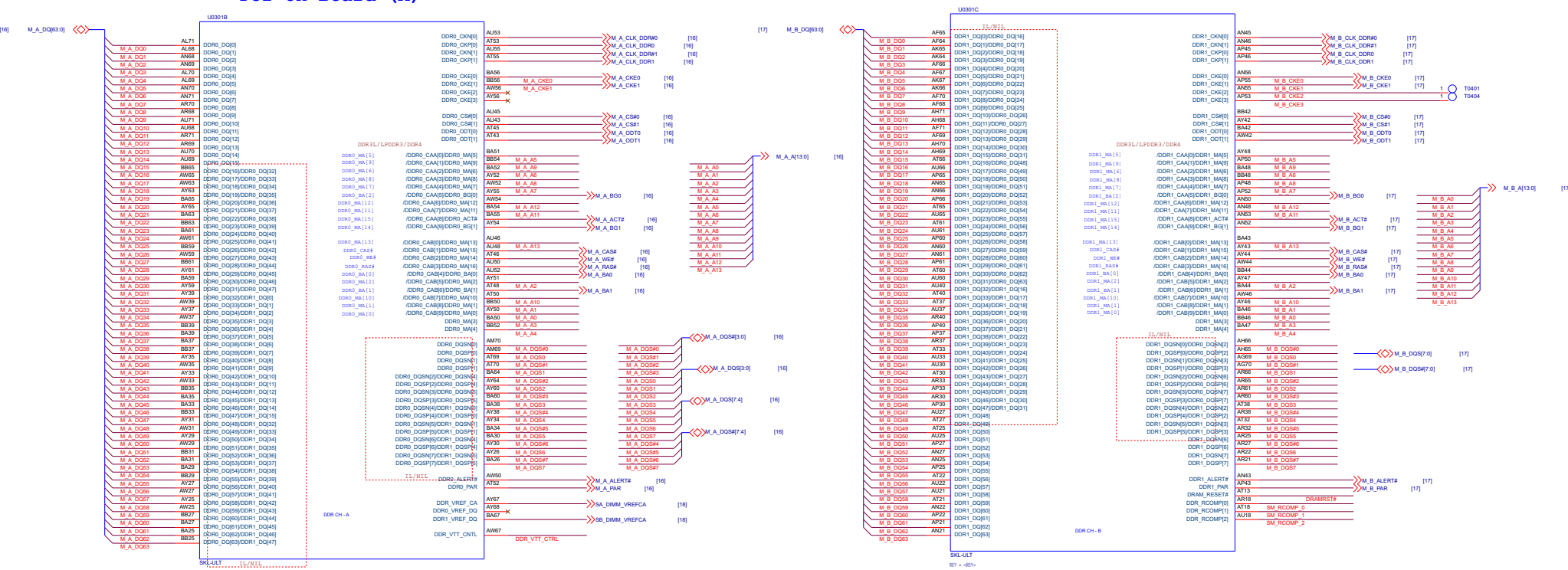
BOM

Project Name: X507UA/UV		Rev: R1.0
Title : CPU_DISPLAY		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 3 of 102	

512M x 8bit x 8

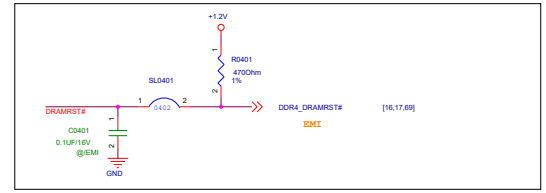
For On Board (A)

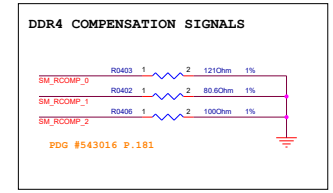
For SO-DIMM (B)



DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

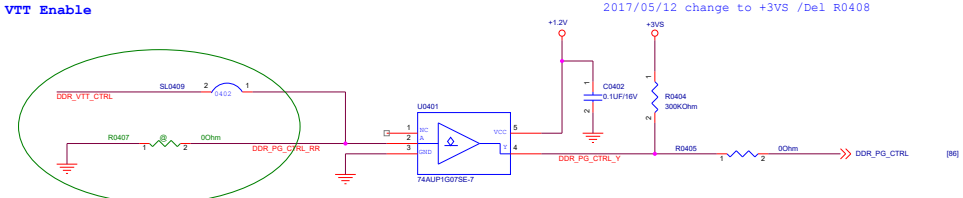
DDR0_Vref_DQ = Not in use in DDR4,
DDR1_Vref_DQ = DDR4_CA_ch1,
DDR_Vref_CA = DD4_CA_ch0





VTT Enable

2017/05/12 change to +3VS /Del R0408



20171228 Kevin Change U0401 PN

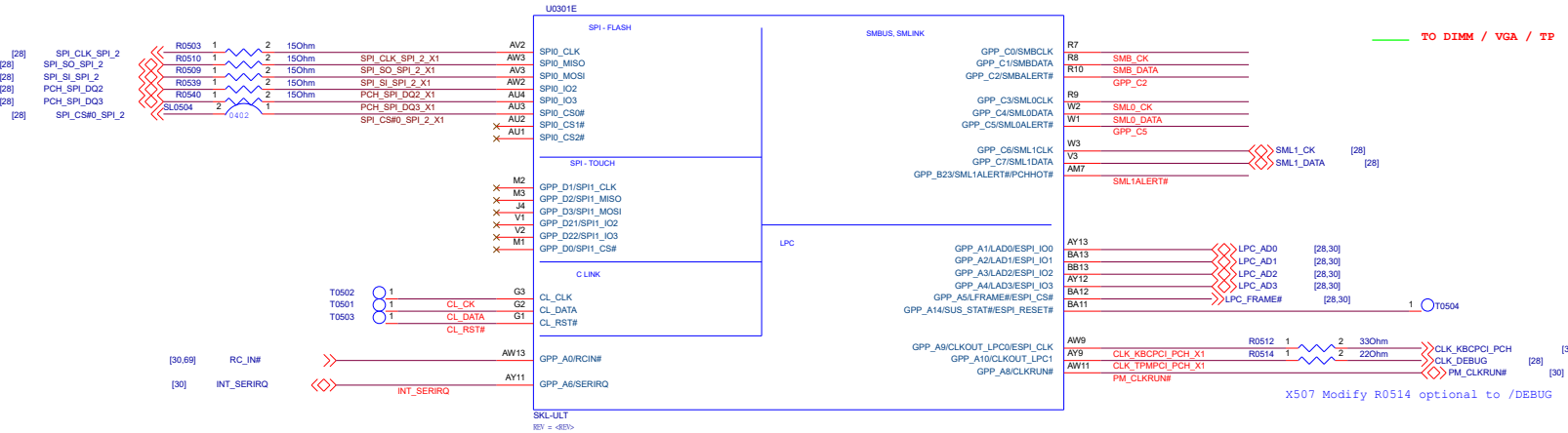
20160216 X541UV R1.1
R0407->R7739,R0408->R7740,R0409->R7741
20160218 X541UV R1.1
R0409->SL0409 for cost

Table 4-44. SKL U DDR4/-RS x8 Memory Down Routing Guideline (Sheet 3 of 3)

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)			Max (mils) Length			R (0±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group[1&2]	Byte [1&2]	Region	Breakout	Total	
RCOMP[0]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	121	
RCOMP[1]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	80.6	
RCOMP[2]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	100	

BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_DDR3		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 4 of 102	



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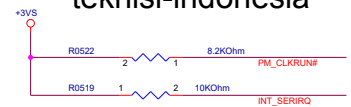
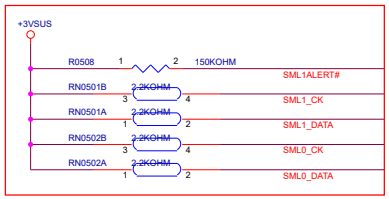
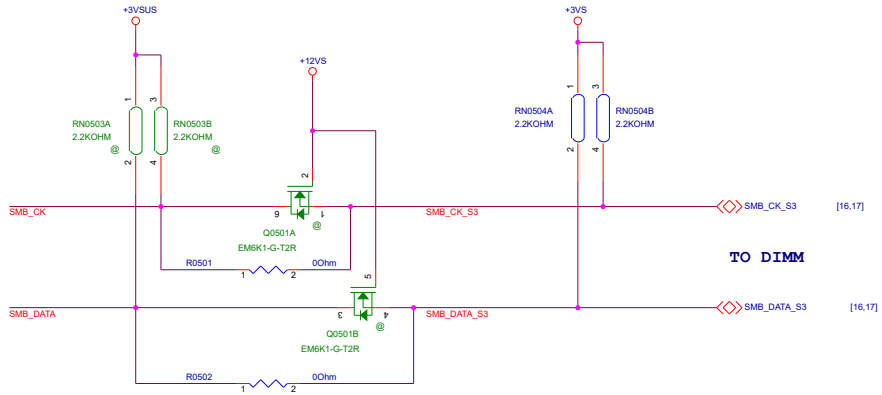
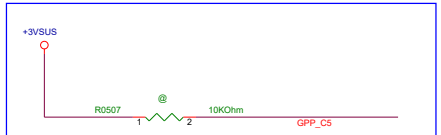


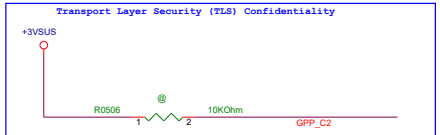




20171228 Kevin add R0501 & R0502 and set RN0503 & Q0501 as unstuff



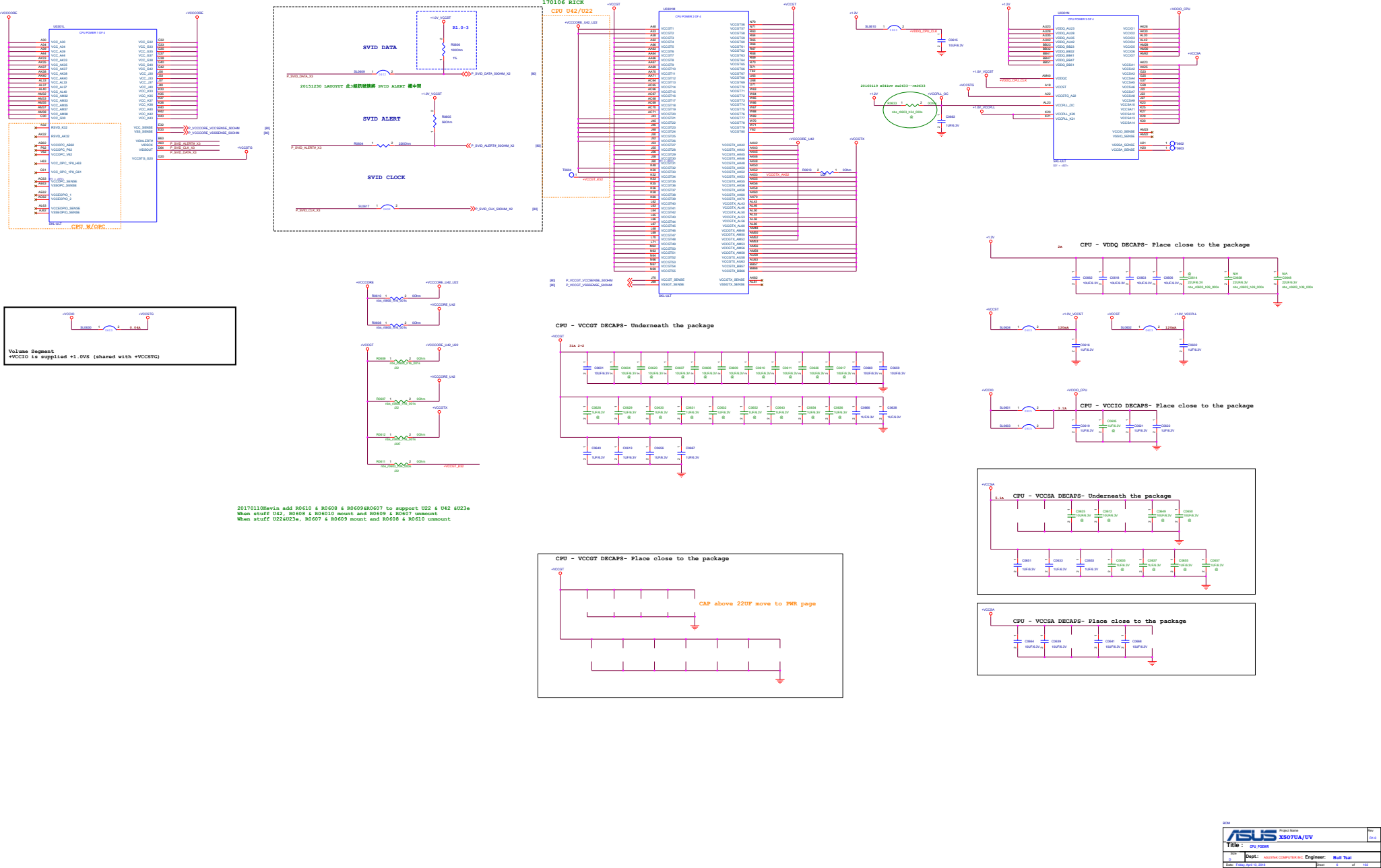
GPP_C5: weak internal pull down	
PU	SPI BUS
PD	LPC is selected for EC (Default)

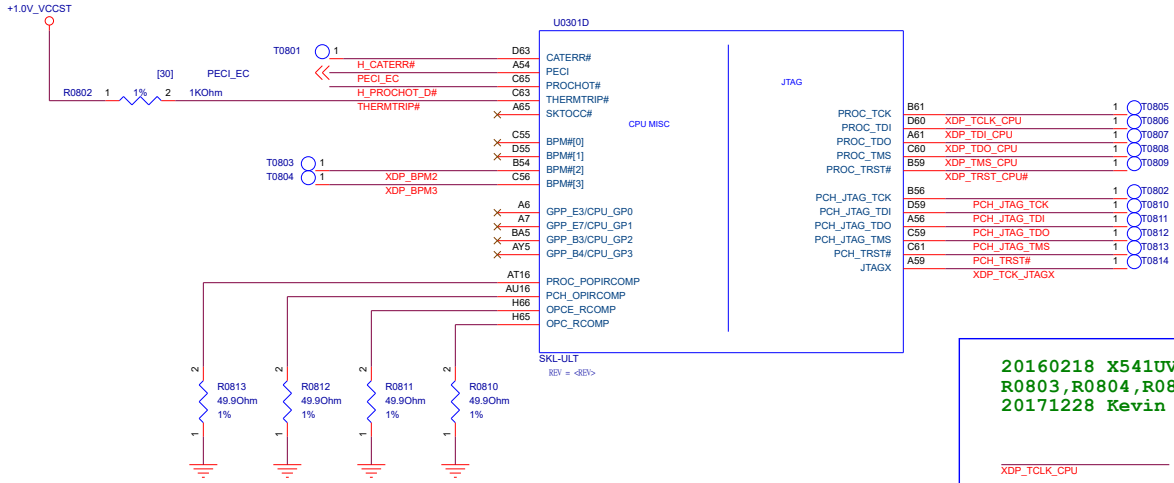


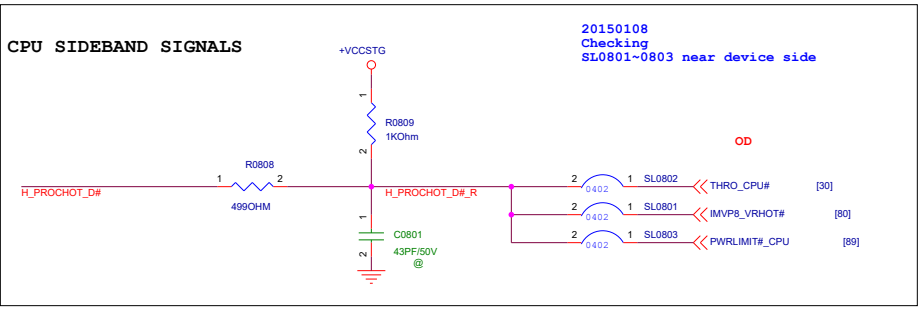
GPP_C2: weak internal pull down	
PU	Enable
PD	Disable Intel ME TLS ipher suite (no confodentiality)(Default)

BOM

Project Name: X507UA/UV		Rev: R1.0
Title : CPU_LPC,SPI,SMB,CLINK		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 5 of 102	

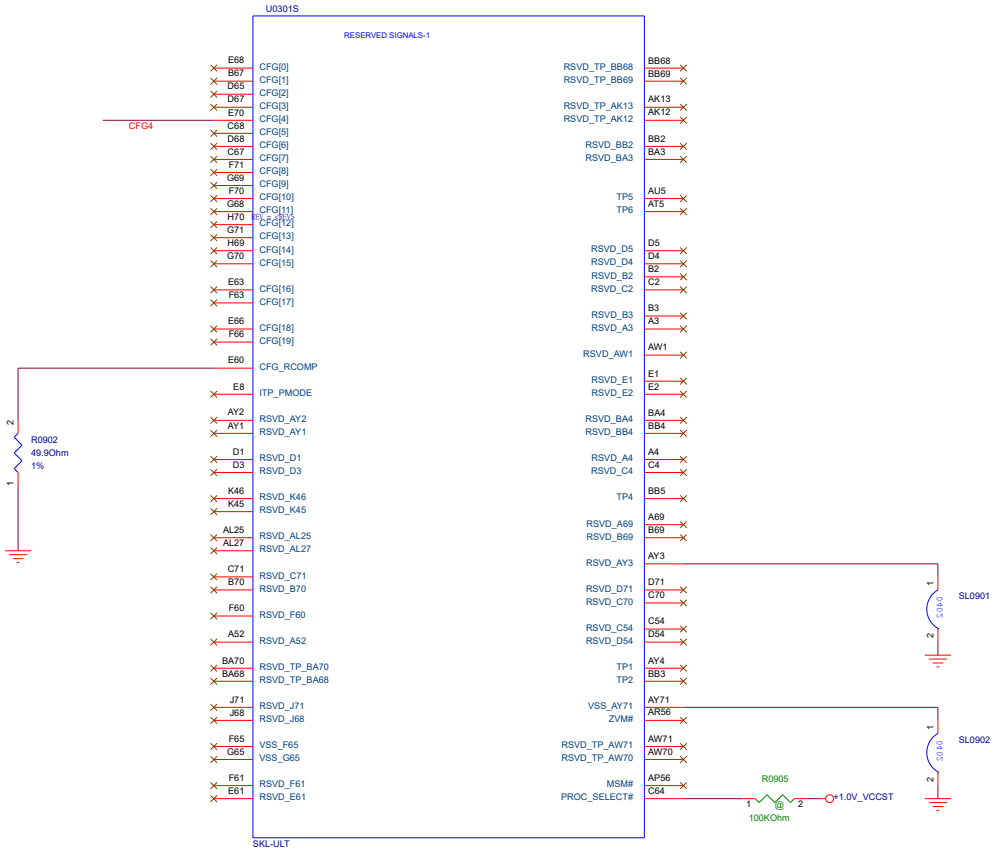

170106 RICK
CPU U42/U22
SVID DATA
SVID ALERT
SVID CLOCK
R1.0-3
20151230 LAOYOUT 此3組訊號請將 SVID ALERT 擺中間
CPU W/ GFC
Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)
20170110Kevin add R0610 & R0608 & R0609&R0607 to support U22 & U42 &U23e
When stuff U42, R0608 & R06010 mount and R0609 & R0607 unmount
When stuff U224023e, R0607 & R0609 mount and R0608 & R0610 unmount
CPU - VCCGT DECAPS- Underneath the package
CPU - VCCGT DECAPS- Place close to the package
CAP above 22UF move to PWR page
CPU - VDDQ DECAPS- Place close to the package
CPU - VCCIO DECAPS- Place close to the package
CPU - VCCSA DECAPS- Underneath the package
CPU - VCCSA DECAPS- Place close to the package
ASUS
X507UA/UV
Title : CPU_POWR
Engineer: Bull Tsai
Date: Friday, April 19, 2019

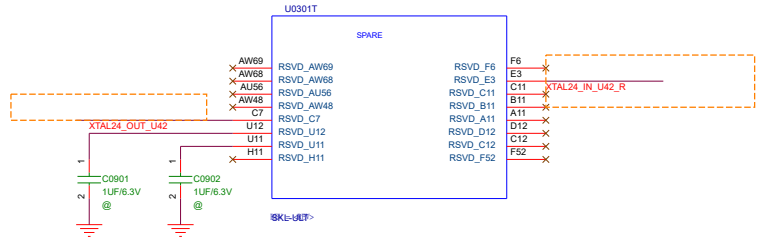




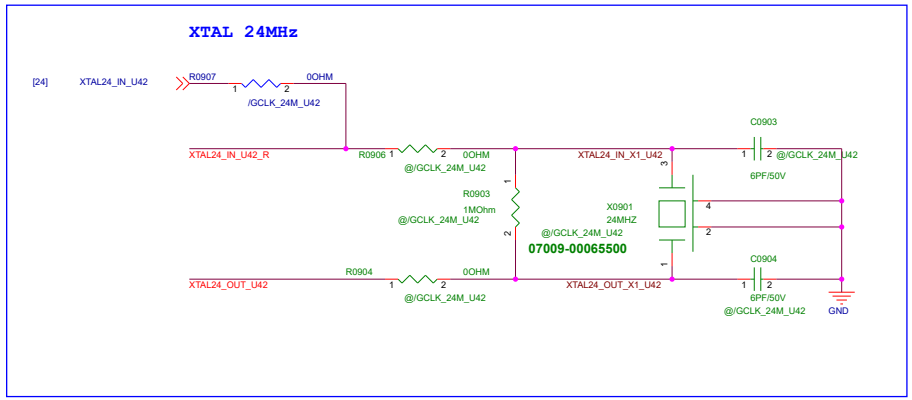
BOM

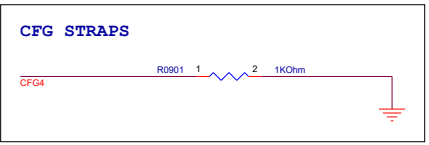
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_MISC,JTAG,CLK		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 8 of 102	





20171228 Kevin add X0901 and related component to support U42 CPU
20180104 Kevin change X0901 PN for system notice



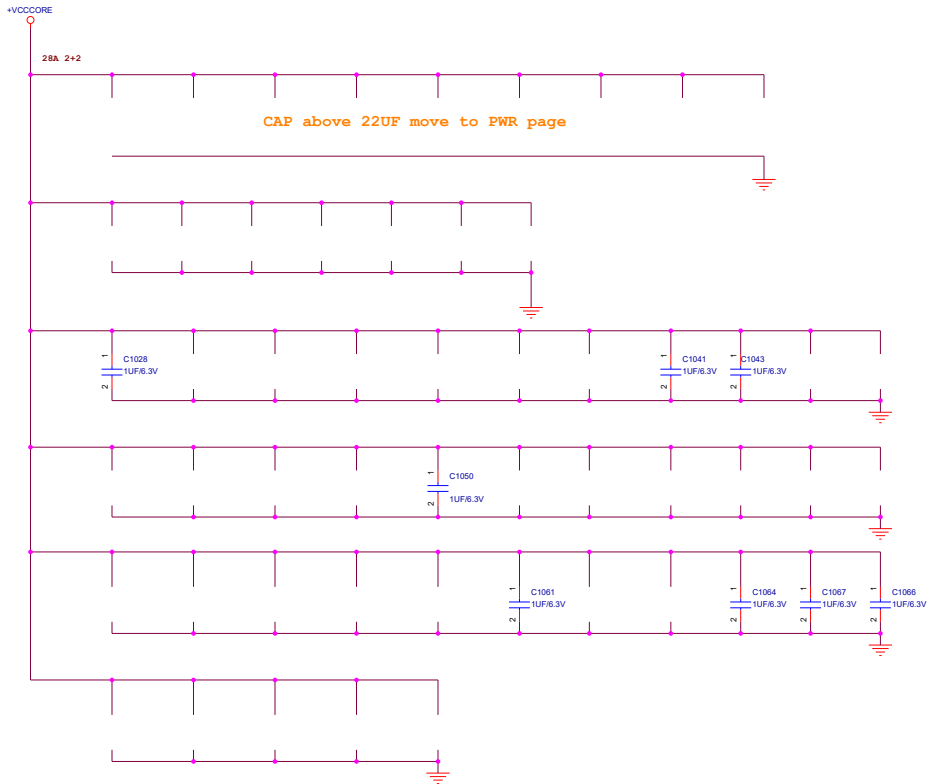


	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

BOM

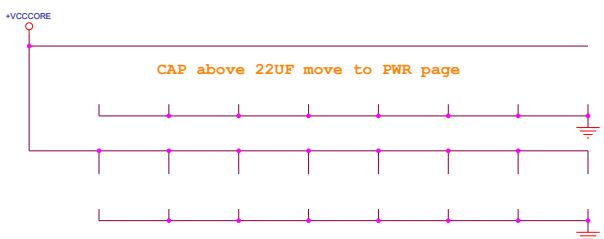
Project Name: X507UA/UV		Rev: R1.0
Title : CPU_CFG,RSVD		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 9 of 102	

CPU - VCC DECAPS- Underneath the package



2018/01/03 Kevin Del for placement space
C1034
C1049
C1046
C1062
C1068
C1065
C1044
C1063
C1031
C1045
C1048
C1030

CPU - VCC DECAPS- Place close to the package



BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_POWER_CAP		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 10 of 102	

2016/12/05 X542UA_R1.0 #98, DDR SWAP
2016/12/07 X542UA_R1.0 #A3, DDR SWAP

SWAP

J1601A

DDR4_DIMM_260P

12002-00080100

'EVENT_N': INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

J1601B

DDR4_DIMM_260P

2017/02/02 X542UA_R1.1 #24, 0ohm modify to SL

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2017/02/02 X542UA_R1.1 #24, 0ohm modify to SL
2017/03/16 X542UA_R2.0 #03, Modify SA0 to pull down

Place close to SO-DIMM

WRITE ADDRESS: 0X

Place close to SO-DIMM Socket (+VTT Pin)

2017/02/06 X542UA_R1.1 #26, EMI solution

Place close to SO-DIMM Socket (+VPP Pin)

2017/02/06 X542UA_R1.1 #26, EMI solution

2018/01/09 delete CE1601 for layout

Place close to SO-DIMM Socket (VDD Pin)

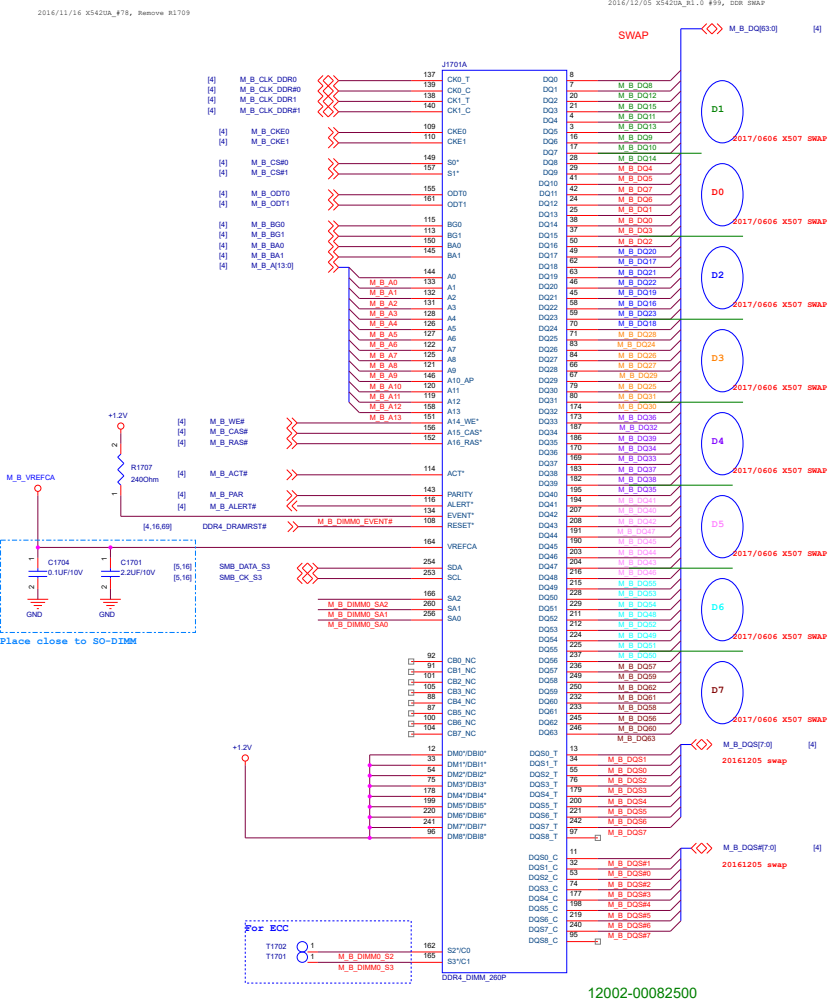
2017/02/06 X542UA_R1.1 #26, EMI solution

BOM

Project Name	X507UA/UV	Rev R1.0
Title :	DDR3_ON-BOARD_B_L32	
Size C	Dept.: NB2_RD1_EE1	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 16 of 102	

2016/11/16 X542UA_#78, Remove R1709

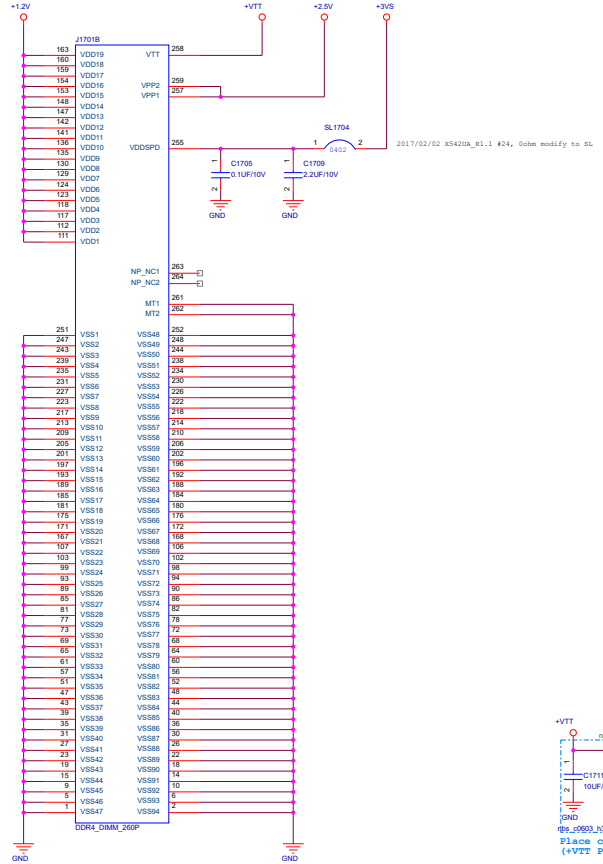
2016/12/05 X542UA_R1.0 #99, DDR SWAP

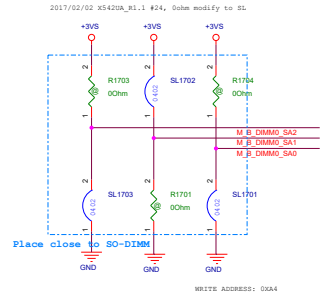


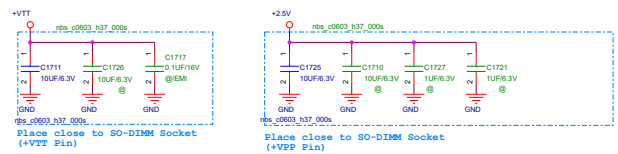
12002-00082500

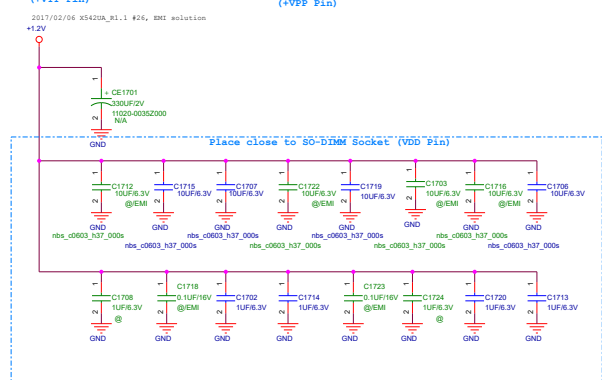
'EVENT_N': INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH







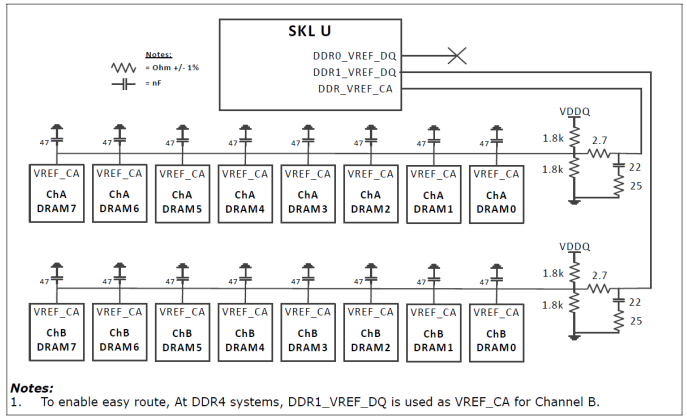


2017/02/06 X542UA_R1.1 #26, EMI solution

<Variant Name>

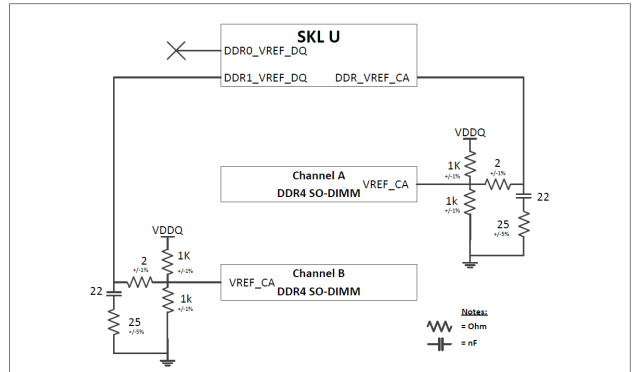
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title :	DDR4_SO-DIMM_1	
Size: C	Dept.:	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 17 of 102	

Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V_{REF-CA} Overview



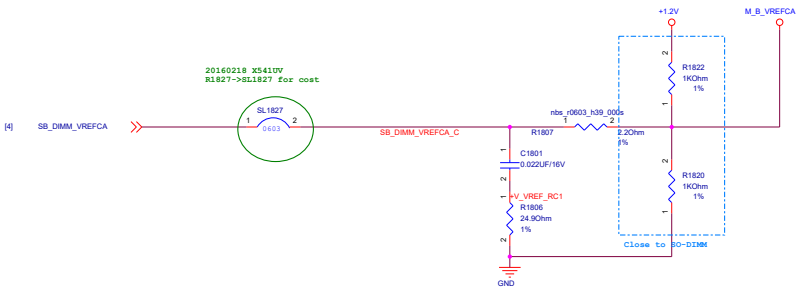
Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

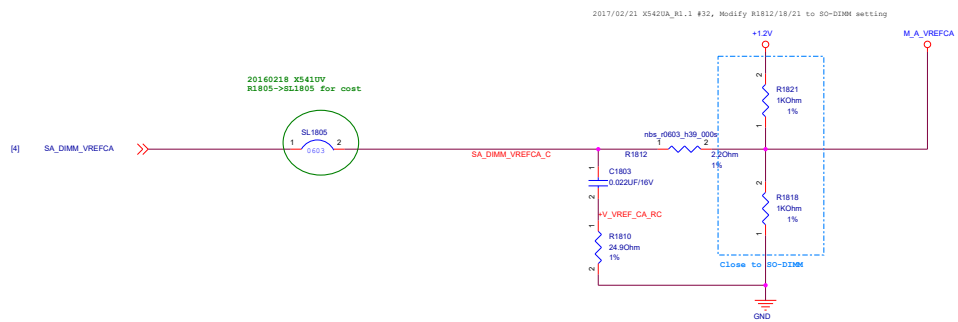
Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

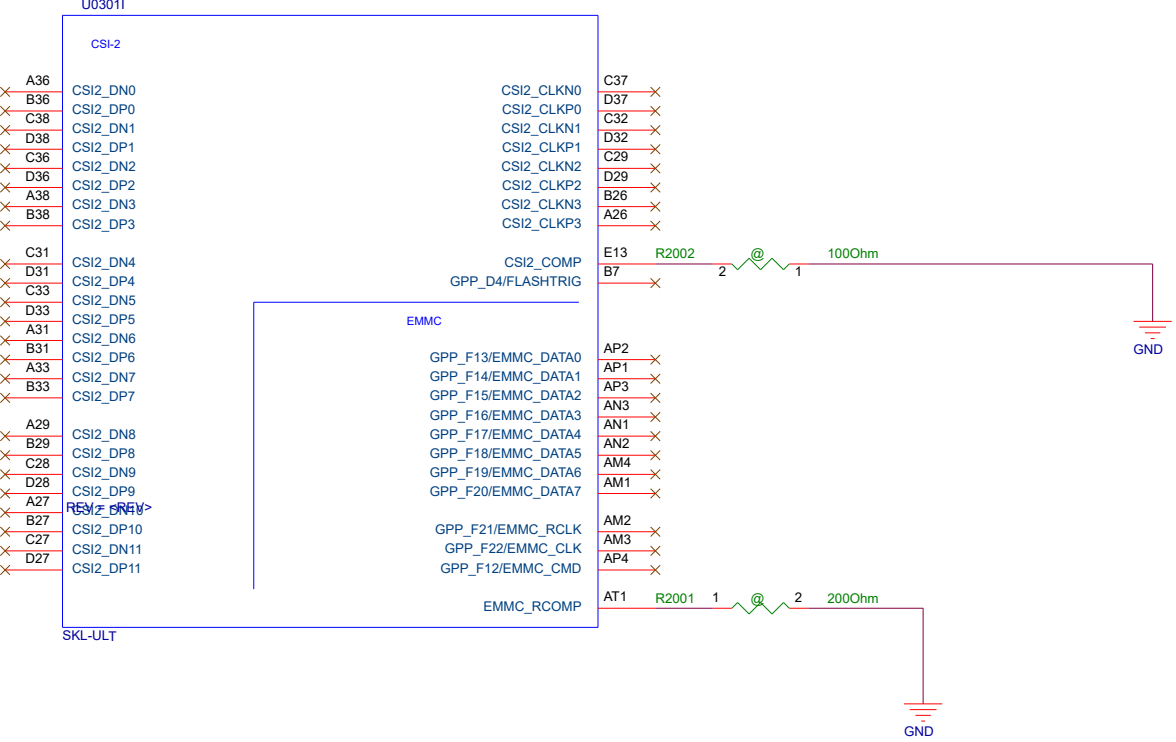
All Vref trace must be 20 mils width





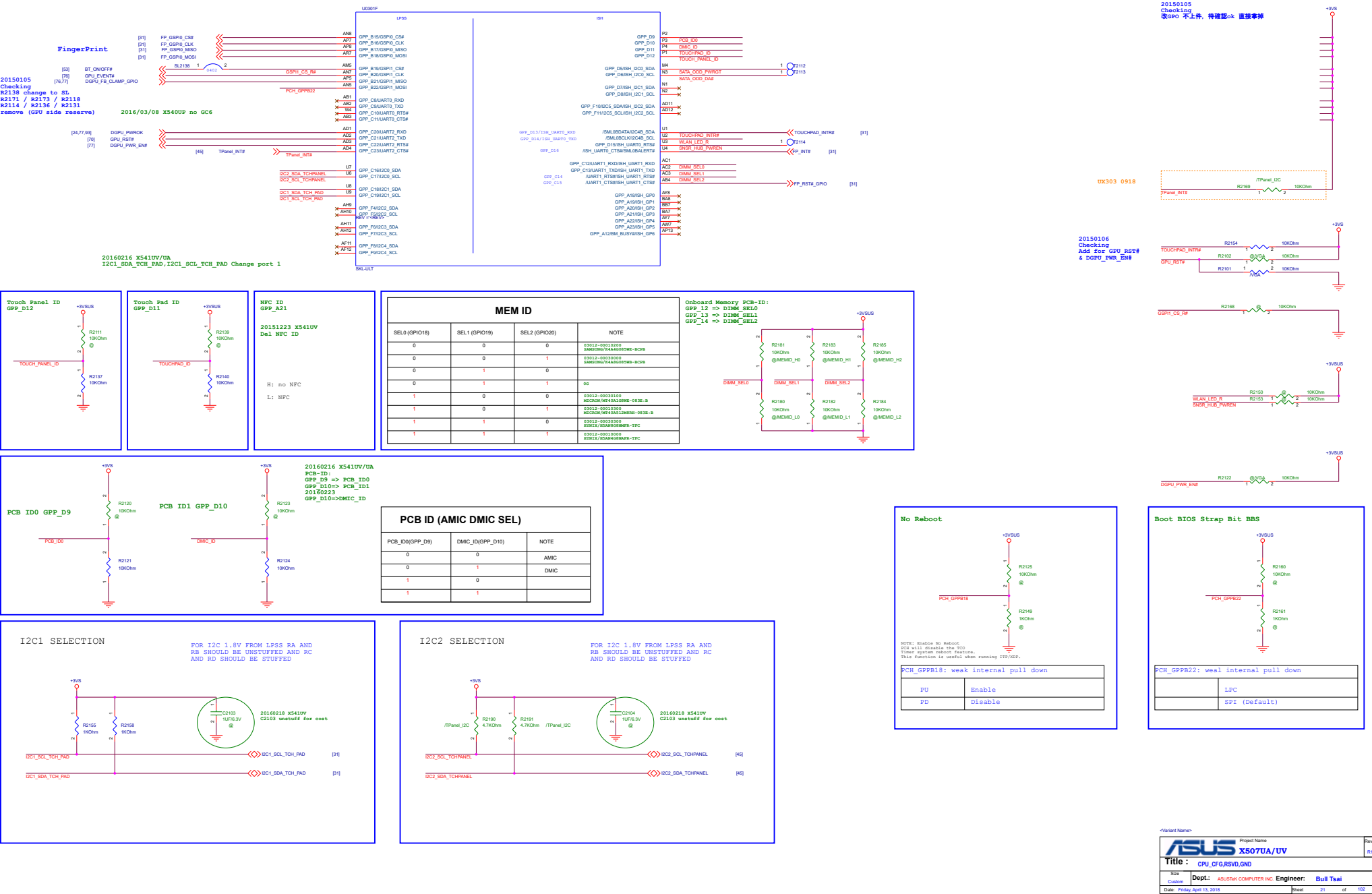
<Variant Name>

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : DDR4 CA VOLTAGE		
Size: C	Dept.:	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 18 of 102	



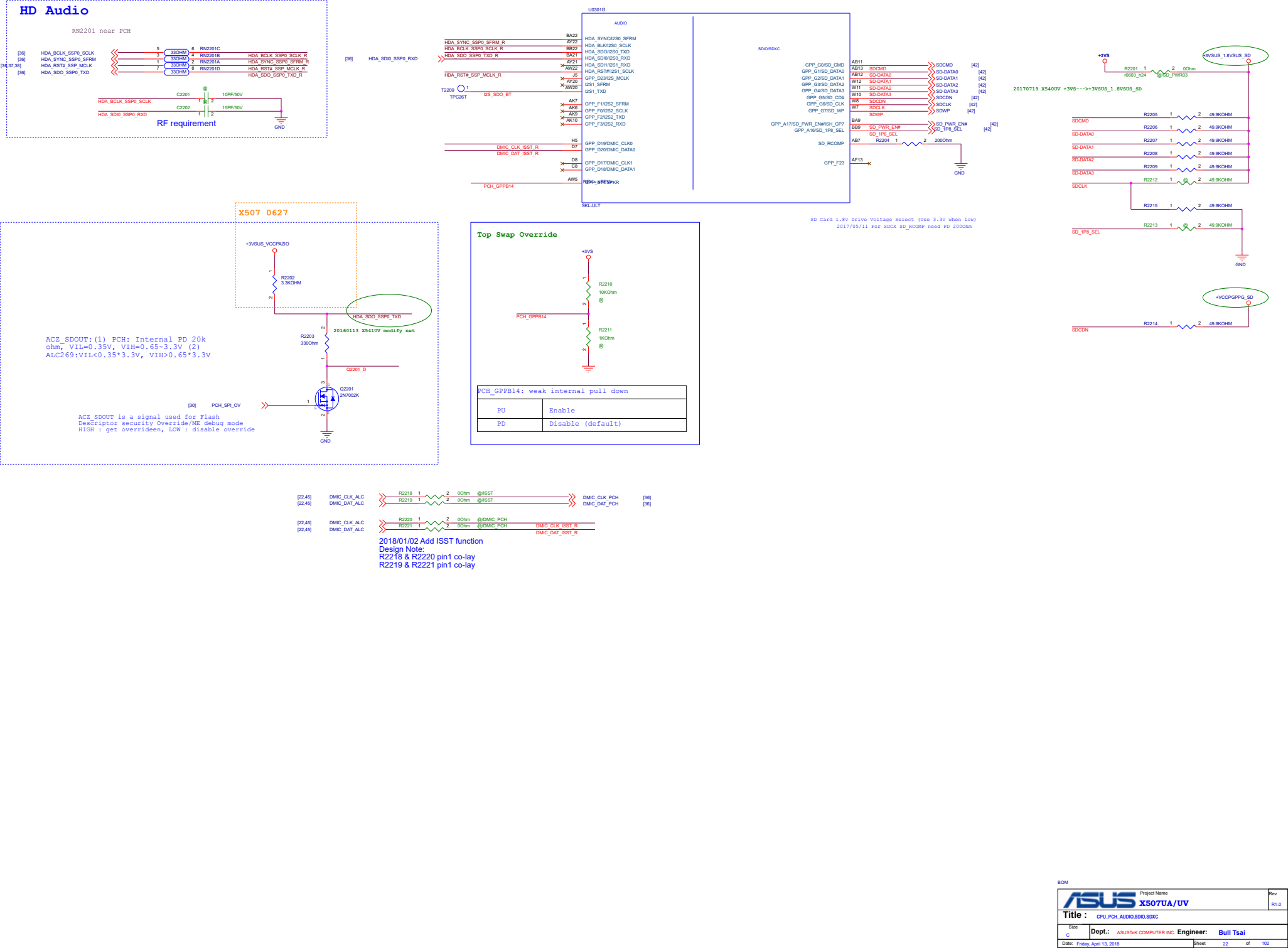
BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_PCH_CSI2,EMMC		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 20 of 102	



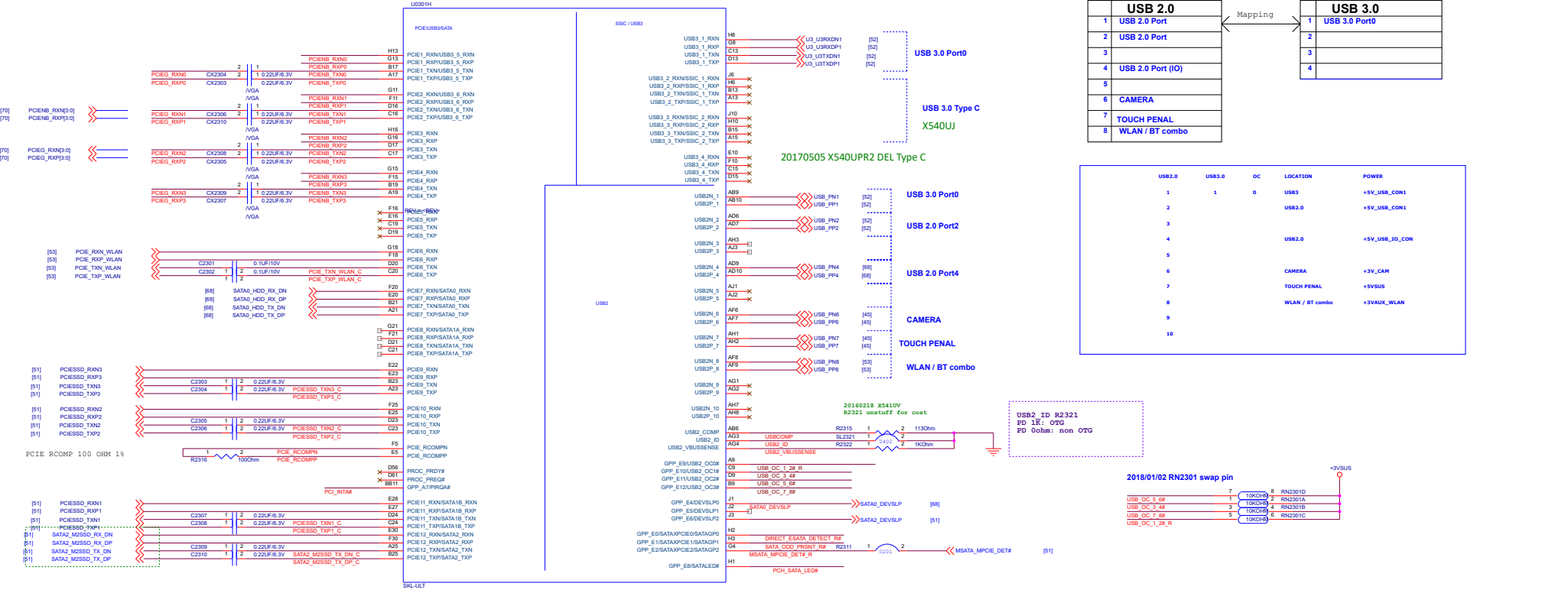
<variant_name>

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title :	CPU_CFG,RSVD,GND	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 21 of 102	



BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_PCH_AUDIO,SDIO,SDXC		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 22 of 102	



USB 2.0		Mapping	USB 3.0	
1	USB 2.0 Port		1	USB 3.0 Port0
2	USB 2.0 Port		2	
3			3	
4	USB 2.0 Port (IO)		4	
5				
6	CAMERA			
7	TOUCH PENAL			
8	WLAN / BT combo			

USB2.0	USB3.0	OC	LOCATION	POWER
1	1	0	USB3	+5V_USB_CON1
2			USB2.0	+5V_USB_CON1
3				
4			USB2.0	+5V_USB_IO_CON
5				
6			CAMERA	+3V_CAM
7			TOUCH PENAL	+5VSUS
8			WLAN / BT combo	+3VAUX_WLAN
9				
10				

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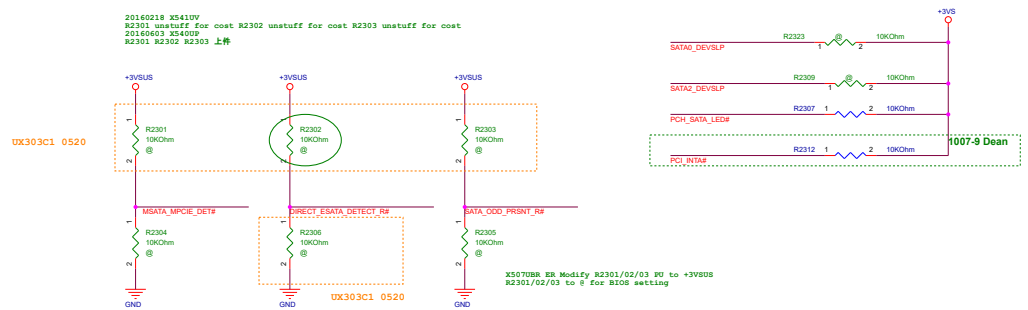
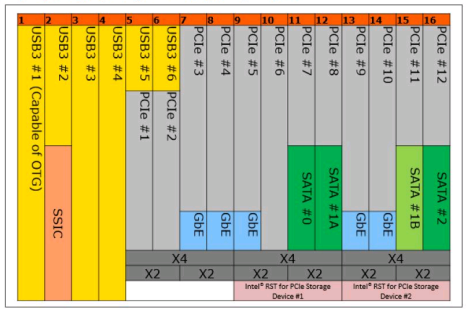


PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 1	DGPU		Port0
PCIE 2	DGPU		
PCIE 3	DGPU		
PCIE 4	DGPU		
PCIE 5			
PCIE 6	WLAN		Port5
PCIE 7/SATA 0	HDD		
PCIE 8/SATA 1A			
PCIE 9	SSD		Port2
PCIE 10	SSD		
PCIE 11/SATA 1B	SSD		
PCIE 12/SATA 2	SSD		

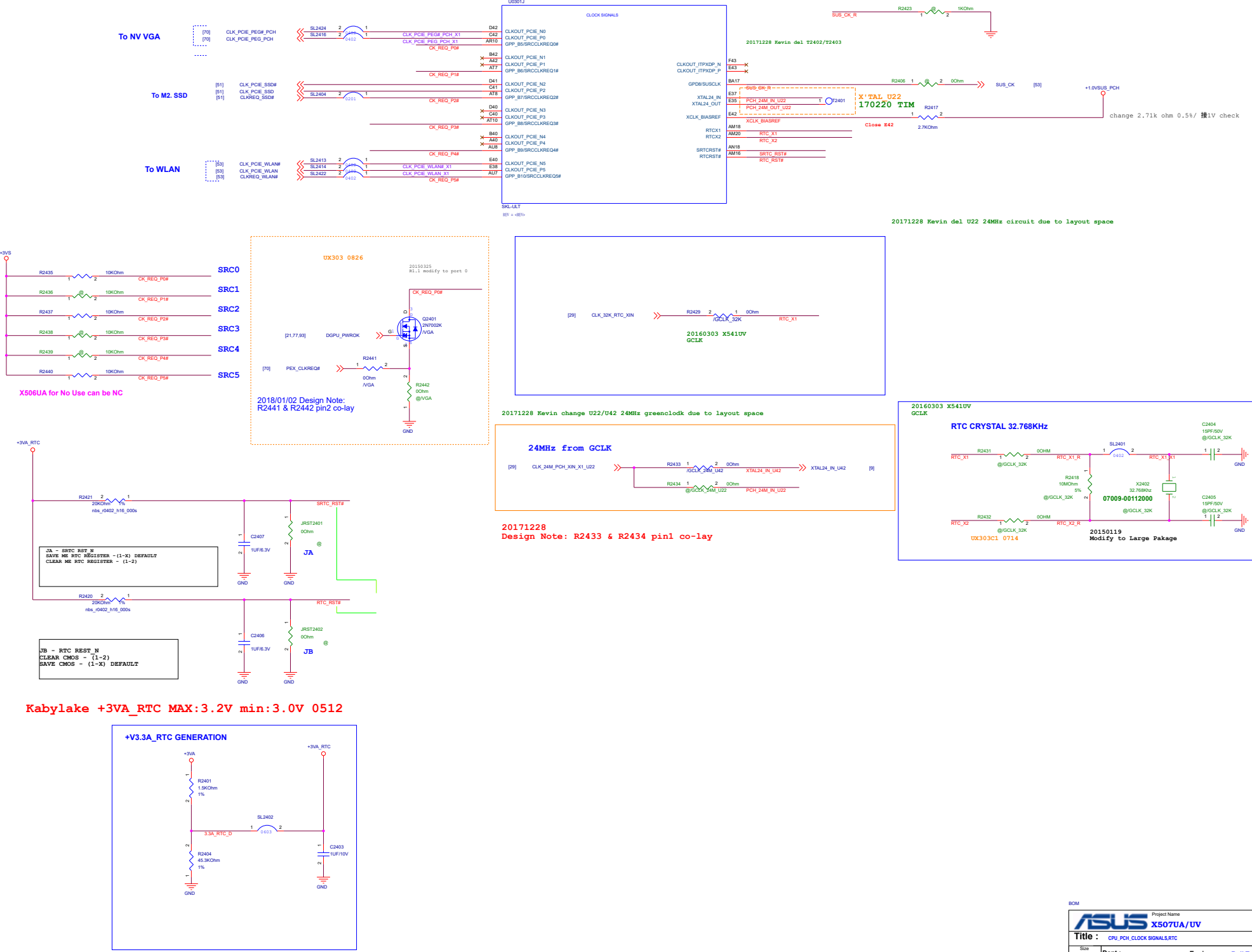
Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in SKL U

SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	N/A
PORT 2	SSD OPTION PCIE
PORT 3	N/A OPTION PCIE



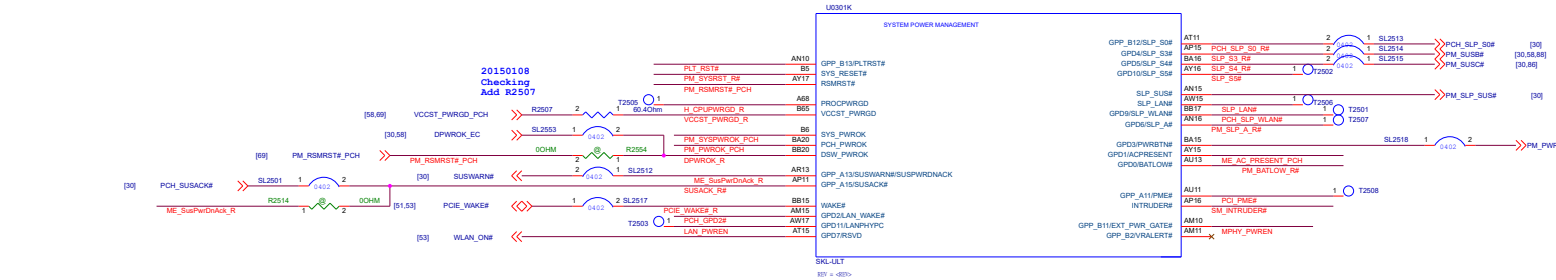
BOM

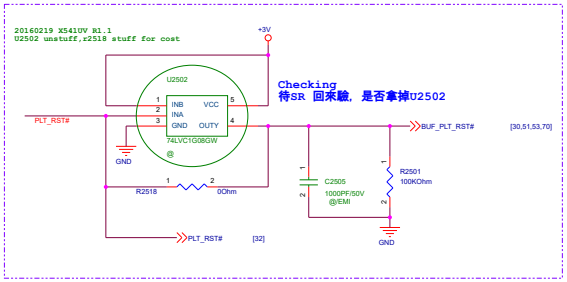
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title :	CPU_PCH_PCIE,USB,SATA	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 23 of 102	

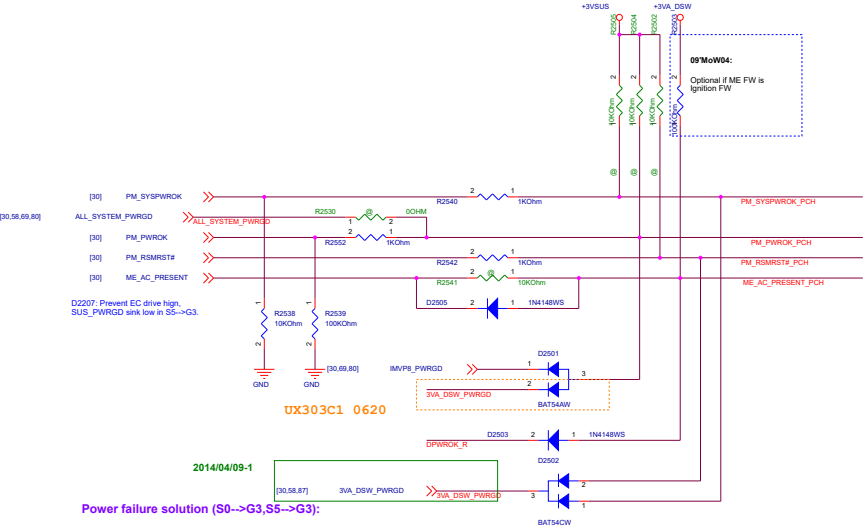


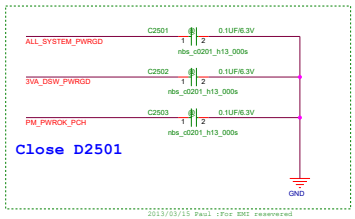
BOM

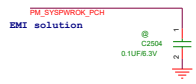
Project Name: X507UA/UV		Rev: R1.0
Title : CPU_PCH_CLOCK SIGNALS,RTC		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 24 of 102	

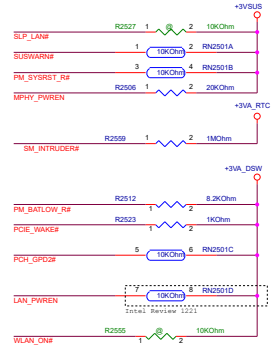


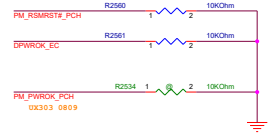










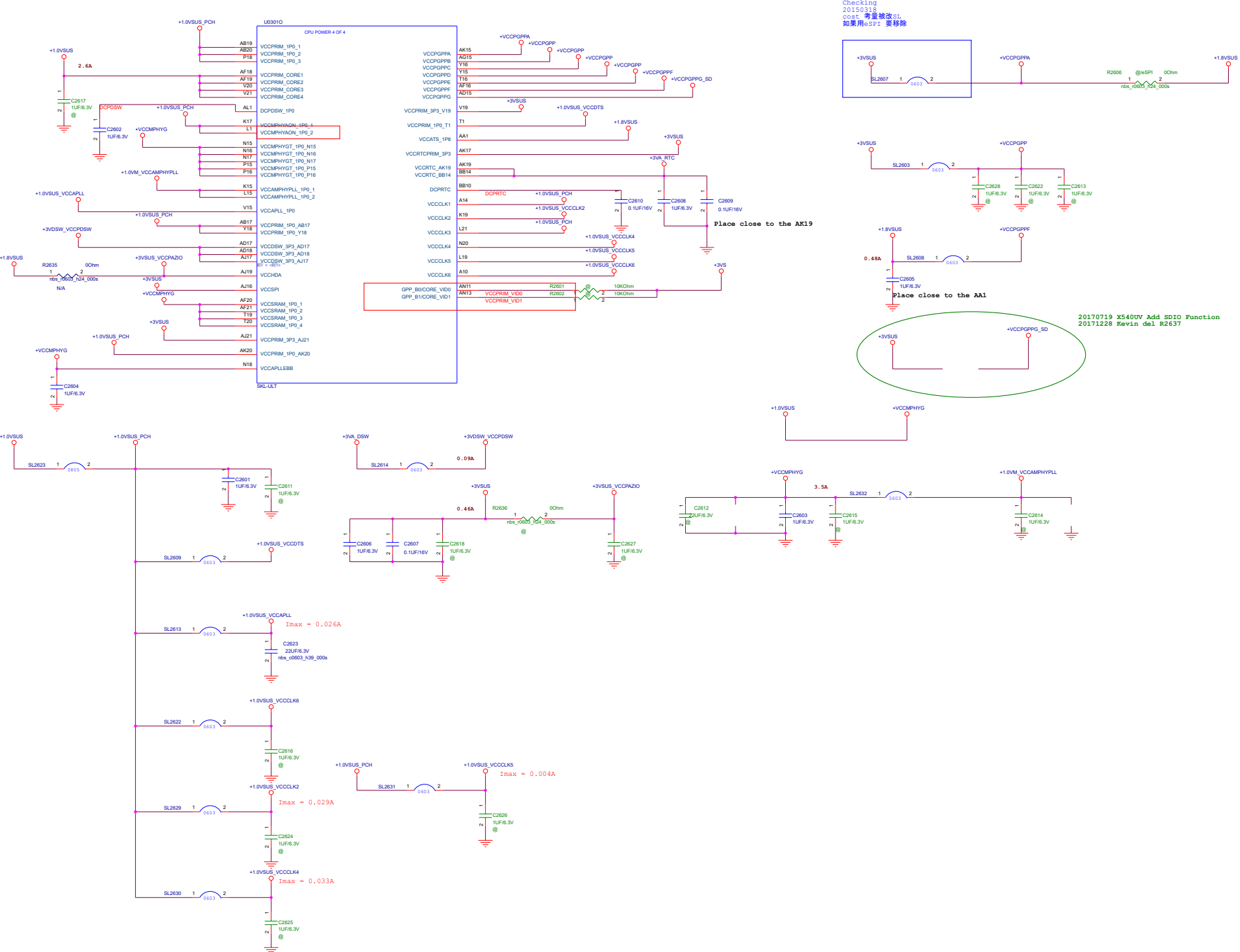


2017/05/12 remove R2505 ,power sequence will be check

BOM

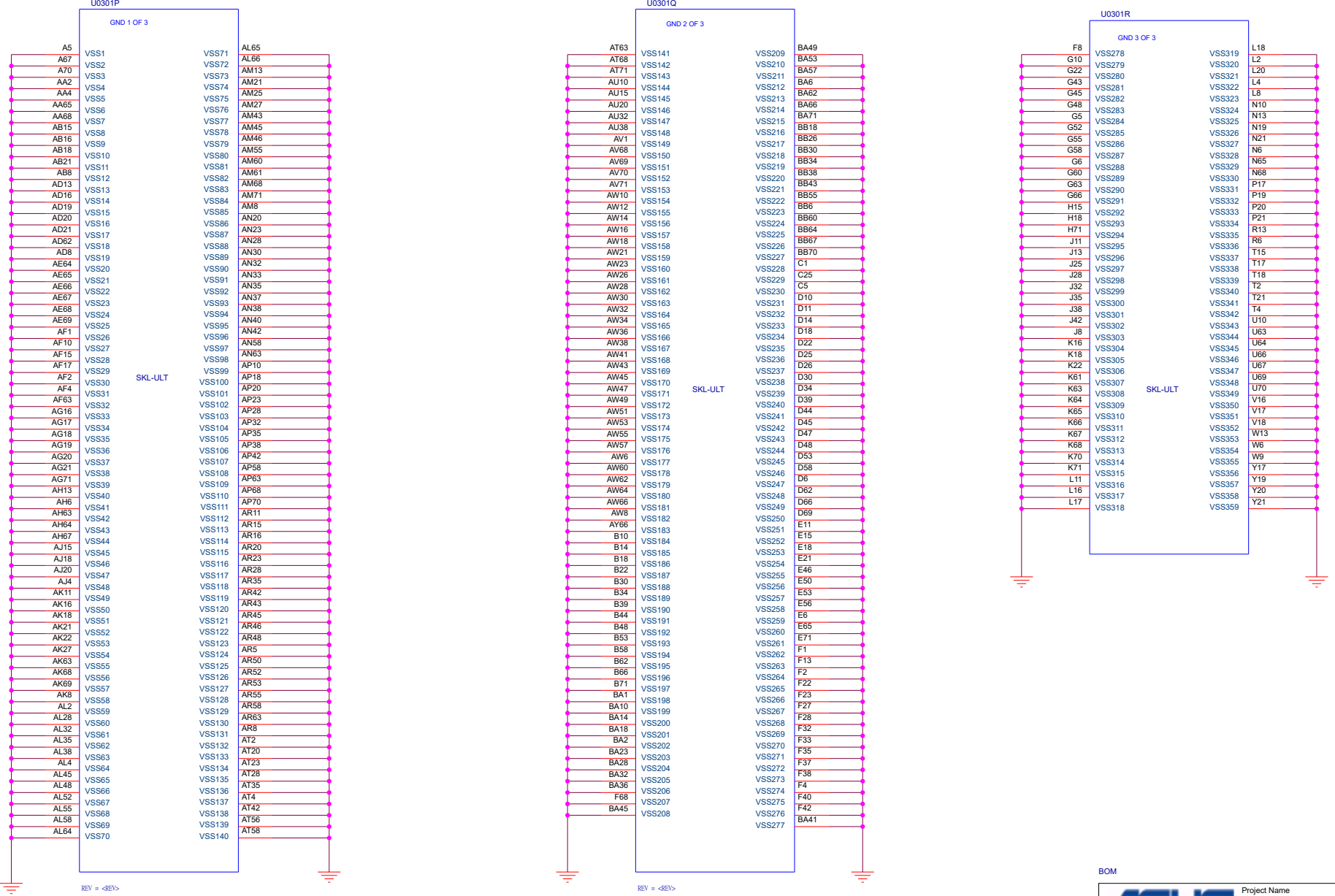
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_PCH_SYS_POWER		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 25 of 102	

Checking
20150318
cost 考量被改SL
如果用eSPI 要移除



BOM

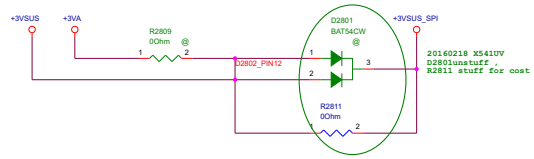
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_PCH_POEWR,GND		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 26 of 102	



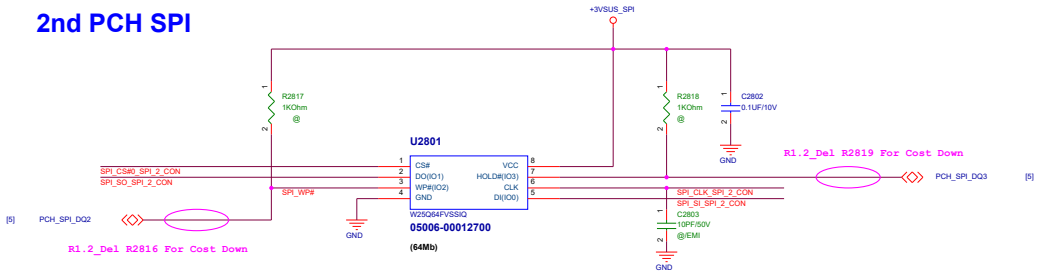
BOM

Project Name: X507UA/UV		Rev: R1.0
Title : CPU_PCH_POEWR,GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 27 of 102	

SPI PCH Power



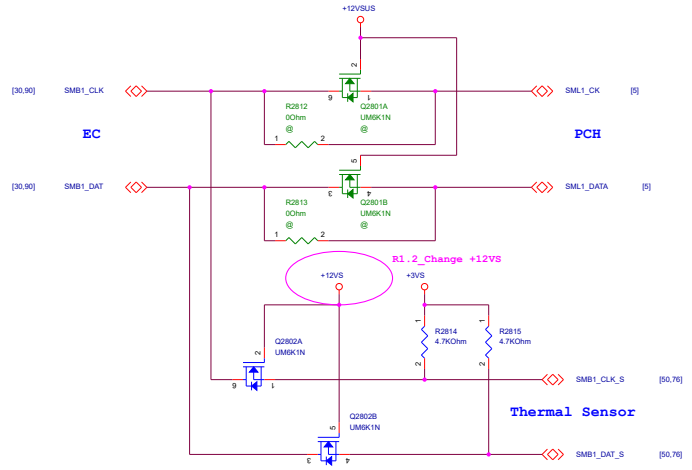
2nd PCH SPI



2nd : 05006-00012700 GIGADEVICE
X540LJ/LA add
X541UV/UA add 20160223
X540UPR BOM change_20170419
M: 05006-00013600
05006-00013400
05006-00012700

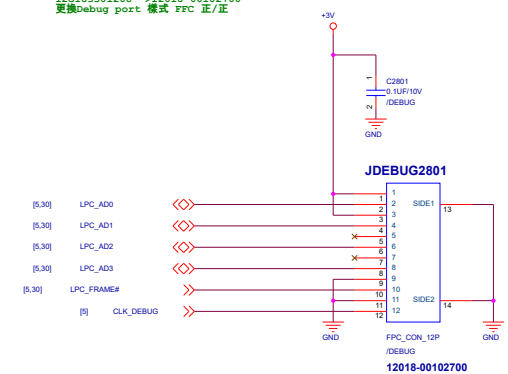
20170505 X540UPR2 BOM
M: 05006-00012700
05006-00013700
05006-00013600

System Management Interface



LPC Debug Port

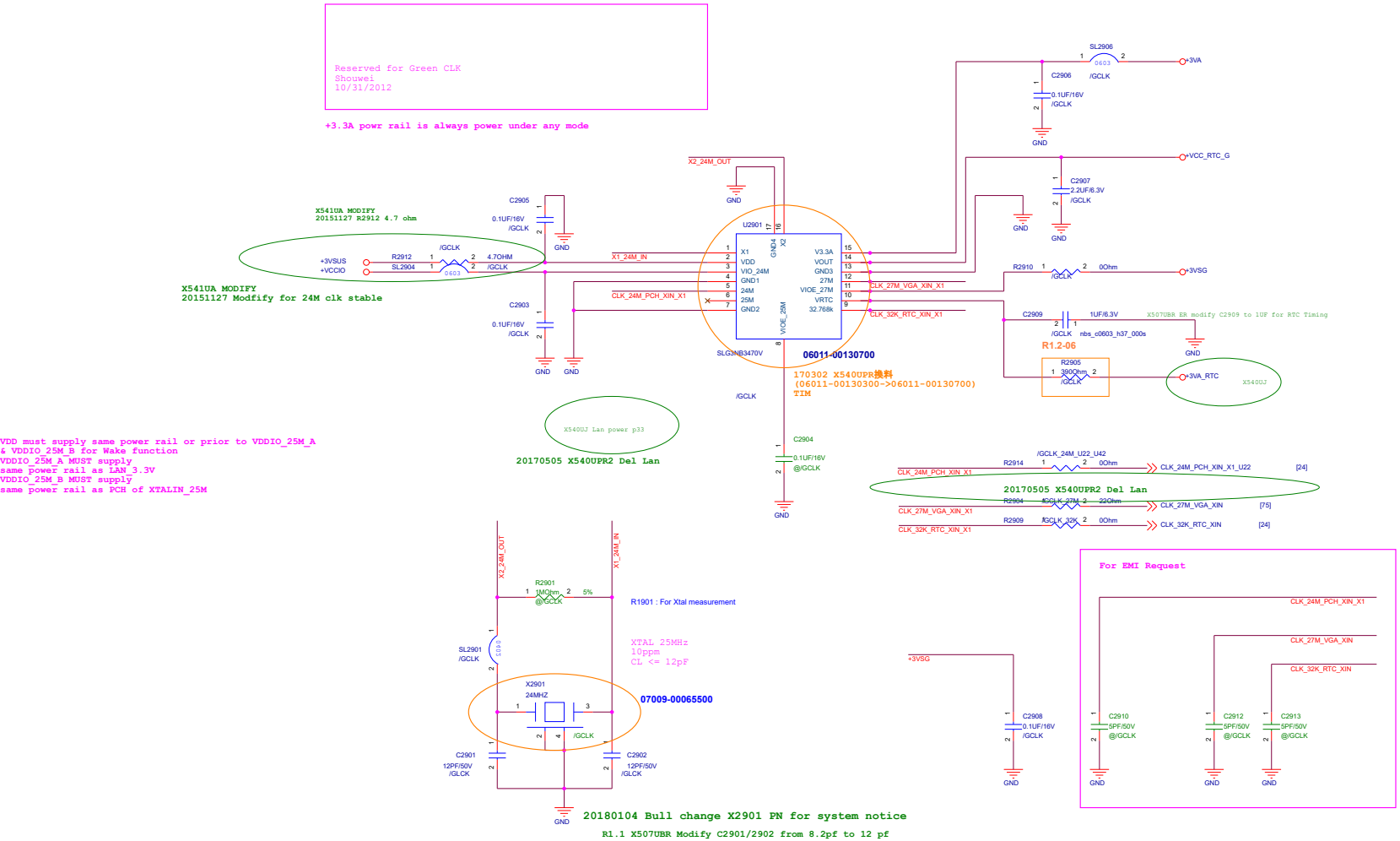
20151225
12G183301208-->12018-00102700
更換Debug port 樣式 FFC 正/正



<Variant Name>

ASUSTeK COMPUTER INC.	Title :	28_PCH-SPI ROM,OTH
	Engineer:	Bull Tsai
Size: C	Project Name: X507UA/UV	Rev: R1.0
Date: Friday, April 13, 2018	Sheet 28 of 102	

Silego Green CLK



ASUSTeK COMPUTER INC. NB1	Title :	Green CLK Gen	
	Engineer:	Bull Tsai	
Size: C	Project Name: X507UA/UV		Rev: R1.0
Date: Friday, April 13, 2018	Sheet 29 of 102		

EC 8585

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

Power

+3VS C3002 0.1UF/16V
+3VA_EC C3003 10UF/6.3V nbs_c0603_h37_000s C3006 10UF/6.3V nbs_c0603_h37_000s C3004 0.1UF/16V C3005 0.1UF/16V
SL3005 0603 +3VPLL C3007 0.1UF/16V
+3VA_EC SL3006 SHORTPIN nbs_r0603_shorted_000s C3001 0.1UF/16V
SL3007 SHORTPIN nbs_r0603_shorted_000s EC_AGND
+3VACC

20160104 X541UV del +1.8VS

U3001 IT8995E

LPC: LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 CLK_KBCPCI_PCH LPC_FRAME# BUF_PLT_RST# INT_SERIRQ EXT_SMI# EXT_SCI# A20GATE RC_IN# EC_RST#
FLASH ROM: DGPU_LIMIT EC_SCK_PCH EC_SO_PCH EC_SI_PCH EC_SCE#_PCH PWRLIMIT_EC# EC_SCK_PCH_X1 EC_SO_PCH_X1 EC_SI_PCH_X1 EC_SCE#_PCH_X1
KBMX: KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
GPIO: PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/RIG1#/GPA7 AC_IN#/GPB0 LID_SW#/GPB1 CTX0/TMA0/GPB2 CRX0/GPC0 TMRI0/GPC4 TMRI1/GPC6 /PWUREQ#/BBO/SMCLK2ALT/GPC7 RI1#/GPD0 RI2#/GPD1 GINT/CTS0#/GPD5 TACH0A/GPD6 TACH1A/TMA1/GPD7 L80HLAT/BAO/GPE0 EGALO/GPE1 EGCLK/GPE3 EGCS#/GPE2 GPE4/BTN# RTS1#/GPE5 TXD/SOUT0/LPCPD#/GPE6 L80LLAT/GPE7 DTR1#/SBUSY/GPG1/ID7 VFSPI CLKRUN#/GPH0/ID0 CRX1/SIN1/SMCLK3/GPH1/ID1 CTX1/SOUT1/SMDAT3/GPH2/ID2 GPH3/ID3 GPH4/ID4 GPH5/ID5 GPH6/ID6 ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 GPH4/GPI4 ADC5/DCD1#/GPI5 ADC6/DSR1#/GPI6 ADC7/CTS1#/GPI7 TACH2/GPJ0 GPU1 DAC2/TACH0B/GPJ2 DAC3/TACH1B/GPJ3 DAC4/DCD0#/GPJ4 DAC5/RIG0#/GPJ5
FS/2: PS2CLK0/TMB0/CEC/GPF0 PS2DAT0/TMB1/GPF1 SMCLK0/GPF2 SMDAT0/GPF3 PS2CLK2/GPF4 PS2DAT2/GPF5
SMBus: PWRSW/GPB3 XLP_OUT/GPB4 SMCLK1/GPC1 SMDAT1/GPC2 SMCLK2/PECI/GPF6 SMDAT2/PECIRQT#/GPF7
GPIO: GPJ6/THERMTRIP_SHUTDOWN# GPJ7

LCD_BACKOFF# [45]
+3VACC
PWR_LED [59] CHG_LED# [59] CHG_FULL_LED# [59] T3010 T3011
EC_GPM3 EC_GPM4 FAN0_PWM [50] T3013
EC_GPA7
AC_IN#_OC# [76,89] LID_SW# [59] T3003
EC_GPB2 3VA_ALW SL3017 +3VA
EC_GPC0 T3026
20170510 follow X5420A_R1.0 #79, Remove PM_EXTTS#0 & R3091
EC_GPC4 T3022
EC_GPC6 SL3018 BAT1_IN_OC# [89] T3018
EC_GPC7
EC_GPD0 SL3009 PCH_SLP_S0# [25]
EC_GPD1 SL3010 ME_AC_PRESENT [25]
EC_GPD5 SL3013 DP_SD# [37,38]
EC_GPD7 FAN0_TACH [50] T3019
EC_GPE0 SL3003 SUSB_EC# [45,57,77,88]
EC_GPE1 SL3012 SUSC_EC# [52,57,68,88]
1.2V_ON [86] T3020
PM_SUSB# [25,58,88] T3021
CAP_LED# THRO_CPU# [8]
PCH_SUSACK# [25]
SL3019 +3VA_EC R1.2-8
PM_CLKRUN# [5] T3004 T3007
SMB3_CLK SMB3_DAT
PM_RSMRST# [25]
DPWROK_EC [25,58]
PM_PWROK [25]
PM_SYSPWROK [25]
PM_SLP_SUS# [25]
3VSUS_PWRGD [58]
ALL_SYSTEM_PWRGD [25,58,69,80]
IMVP8_PWRGD [25,69,80]
3VA_DSW_PWRGD [25,58,87]
IMVP8_PWRGD = CORE_PWRGD
5VSUS_PWRGD remove
ME_SusPwrDnAck_EC
A/D_MAX_POWER [89]
MB_MAX_POWER [89]
3VADSW_ON [87]
GPJ0 [65] T3015
PL_REF_EC T3016
EC_GPJ3 T3014
iBAT_REF_EC
EC_GPJ5 T3025
2014/02/06-3

20160218 X541UV
R3025->SL3025 for cost

2013/03/15 Fwui :For EMI reserved

ITE Version	ASUS P/N
IT8995E-128/DX	06037-00050700

X507 Update

EMBEDDED CONTRO IT8995E-128/DX
06037-00050700

EMI solution

1220 Kevin del RN3002

PWR_SW# R3007 10KOhm
LID_SW# R3008 10KOhm
AC_IN_OC# R3009 10KOhm
+3VA
TP_DAT TP_CLK RN3004A RN3004B 4.7KOhm +5VS

X541UA MODIFY

1220 Kevin del R3021/R3022/R3016

SMB1_DAT SMB1_CLK SMB0_DAT SMB0_CLK RN3003B RN3003A RN3003C RN3003D 4.7KOhm
PWRLIMIT_EC# R3001 10KOhm R3063 100KOhm
EC-GPB2 UX303 0826
3VADSW_ON R3017 100KOhm
5VSUS_ON R3015 10KOhm R3061 1MOhm
VSUS_ON R3060 100KOhm R3036 1MOhm
CHG_FULL_LED# CHG_LED# THRO_CPU# R3018 10KOhm
PM_SLP_SUS# R3020 100KOhm

R1.0-6

PM_PWRBTN# R3019 10KOhm +3VSUS
IMVP8_PWRGD UX303 0714 R3085 10KOhm
R3074 10KOhm
A20GATE R3075 10KOhm
RC_IN#
UX303 0520 R3032 10KOhm
PM_RSMRST# UX303 0918 R3065 10KOhm
SUSB_EC# R3066 10KOhm
SUSC_EC#
EC_SCK_PCH_X1 EC_SCE#_PCH_X1 EC_SO_PCH_X1 EC_SI_PCH_X1
MB_MAX_POWER R3006 100KOhm
R3002 100KOhm
PM_SUSC# R3003 100KOhm
PM_SUSB#

1220 Kevin del R3069/R3068/R3030/R3031

+3VA_EC Checking BAT1_IN_OC# 時為-BAT 不時為-PD
R3047 lin-BAT R3048 10KOhm
BAT1_IN_OC# lin-BAT
for X455 internal battery always PD

EC_SCK_PCH C3019 15PF/50V
EC_SI_PCH C3020 33PF/50V
EC_SCE#_PCH C3021 33PF/50V
CLK_KBCPCI_PCH C3018 10PF/50V
BAT1_IN_OC# C3011 0.01UF/16V
UX303 1002
PWR_SW# C3012 0.01UF/16V
BUF_PLT_RST# C3009 1000PF/50V

UX303 0826
[25] SUSWARN# SL3001 ME_SusPwrDnAck_EC

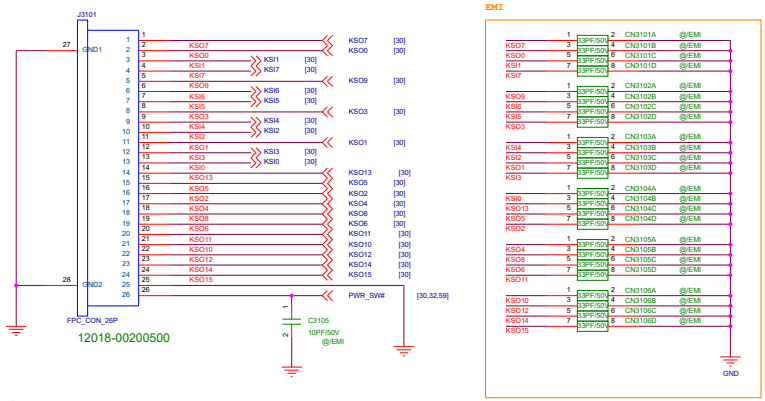
EMI
3VA_DSW_PWRGD C3010 1000PF/50V @EMI
SUSB_EC# C3013 0.1UF/10V @EMI
SUSC_EC# C3014 0.1UF/10V @EMI
LID_SW# C3015 0.1UF/10V @EMI

EMI solution
PM_SYSPWROK C3023 0.1UF/6.3V
PM_PWROK C3024 0.1UF/6.3V
DPWROK_EC C3025 1000PF/50V
ALL_SYSTEM_PWRGD C3026 0.1UF/6.3V
3VSUS_PWRGD C3027 1000PF/50V

BOM

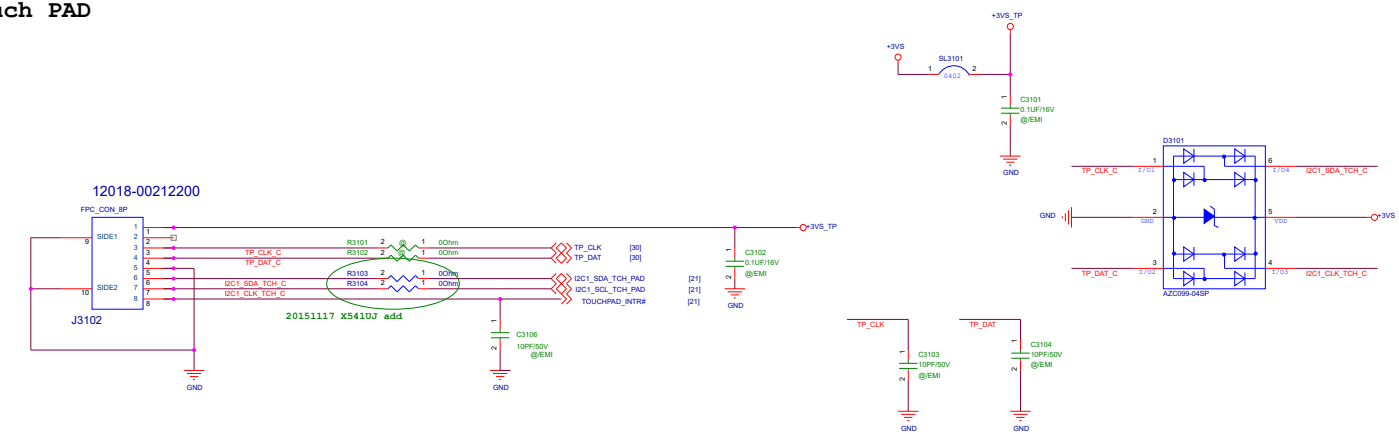
ASUS	Project Name: X507UA/UV		Rev: R1.0
Title : IT8995E-128/CX			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 30 of 102		

Internal Keyboard

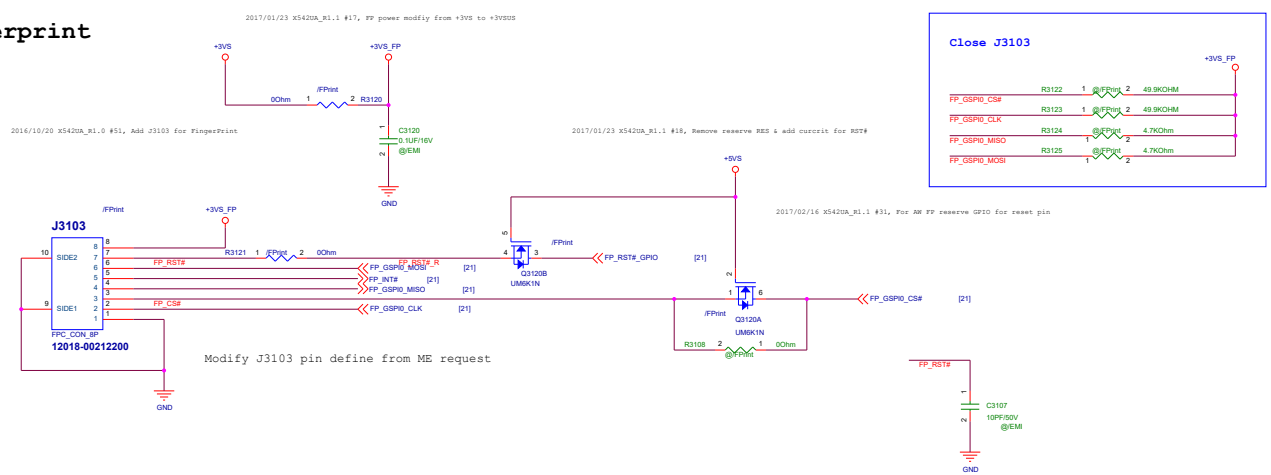


2017/05/16 modify PN to 12018-00200500

Touch PAD



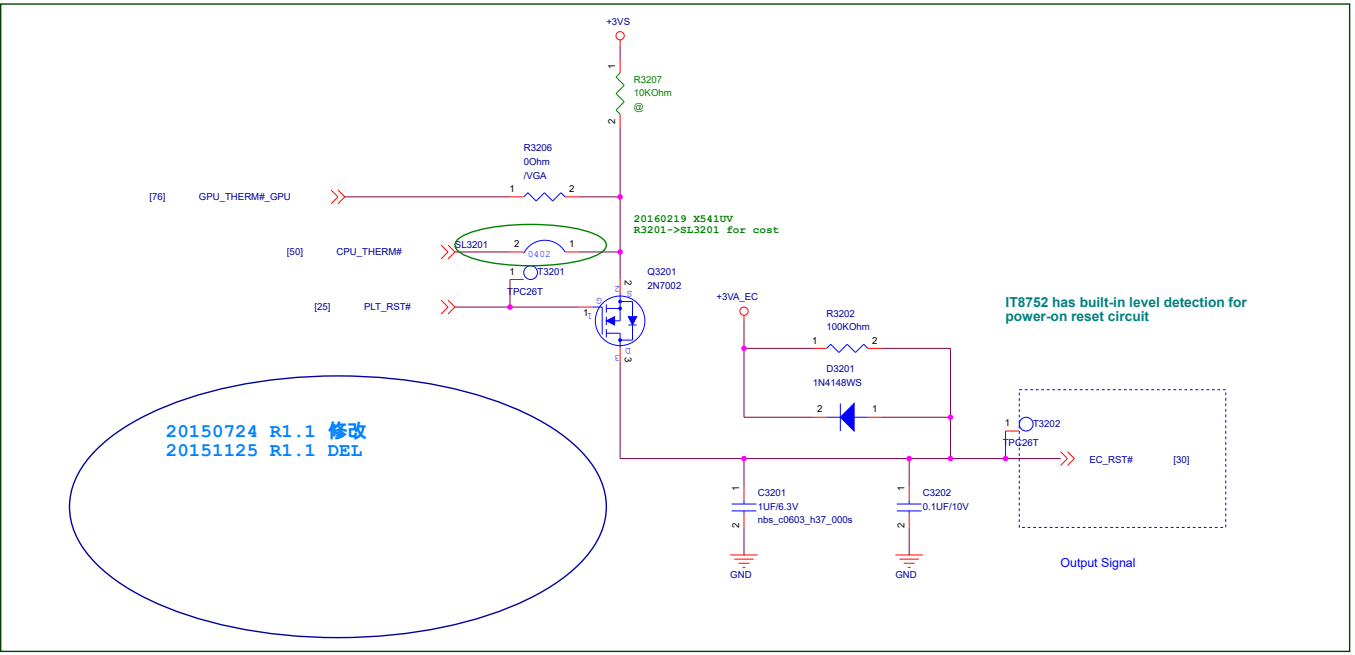
Fingerprint



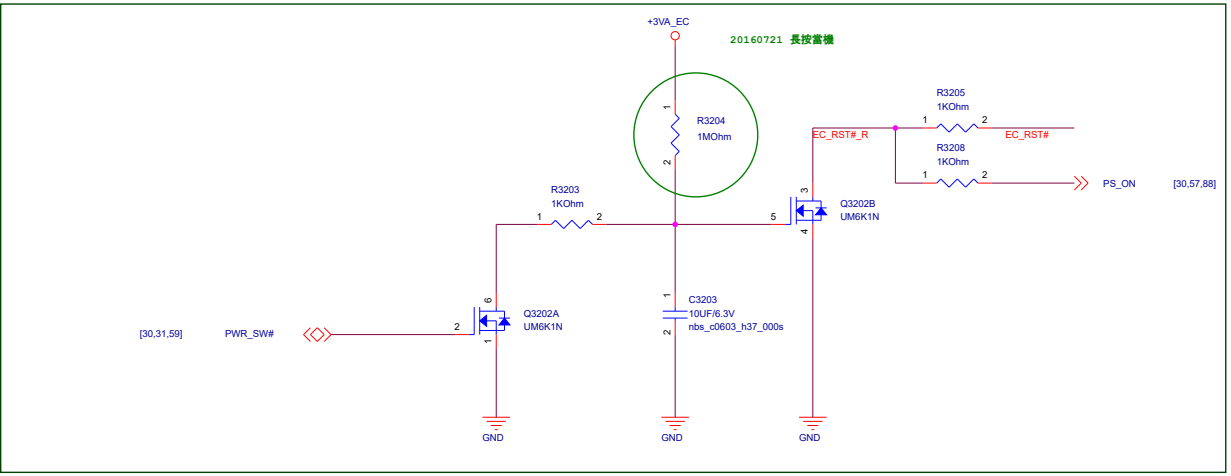
BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : EC-IT8995_KB,TP		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 31 of 102	

Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)



<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title : 32_RST_Reset Circuit	
	Engineer: Bull Tsai	
Size: B	Project Name: X507UA/UV	Rev: R1.0
Date: Friday, April 13, 2018	Sheet 32 of 102	

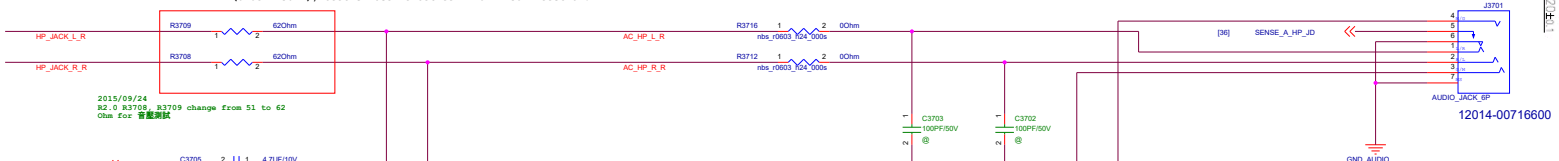
Universal Jack (Normal open type)

- 尺寸：一般分三種規格，2.5mm、3.5mm、6.35mm。
- 種類：一般分也三種規格，TS 端子 (Mono)、TRS 端子 (Stereo)、TRRS 端子 (Stereo + Mic/Video)。

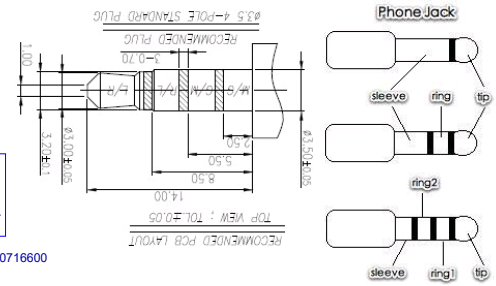
R1.3. Item 12.
Add 4 pole headset jack normal
open type for project demand.

R1.4. Item 13.
Recommand the HP damping resistance 56 ohm for CB certification.
Depend on your project, you can change the resistance value to meet CB certification
(under 150mV), best chioce is between 140mV~150mV section.

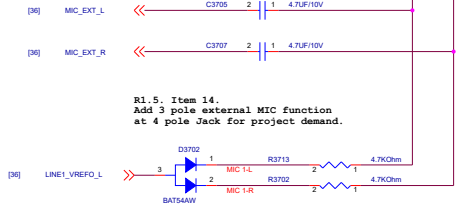
Global Headset
Normal Open
Supported iPhone/Nokia headset, headphone

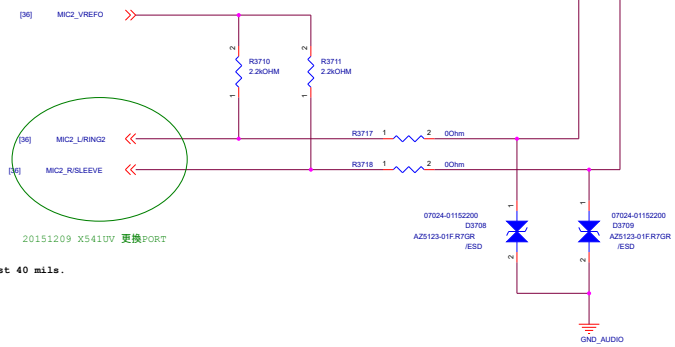


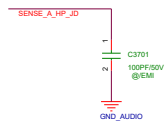
12014-00716600



R1.5. Item 14.
Add 3 pole external MIC function
at 4 pole Jack for project demand.







R0.93. Item 3.
Realtek suggest PCB trace width of RING2 & SLEEVE at least 40 mils.

CITA：國際標準

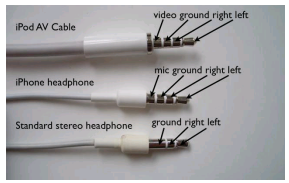
Apple iPhone/HTC/小米 的 Phone Jack 定義：

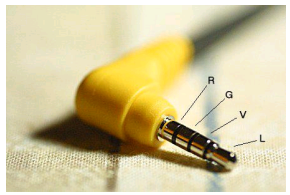
Apple	iPad (Stereo)	iPod (Stereo)	iPhone (Mic)	iPod (AV)
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring2	-	-	Ground	Ground
4. Sleeve	Ground	Ground	Mic	Video

OMTP：國家標準

Nokie Type 的 Phone Jack 定義：

Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring2	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel

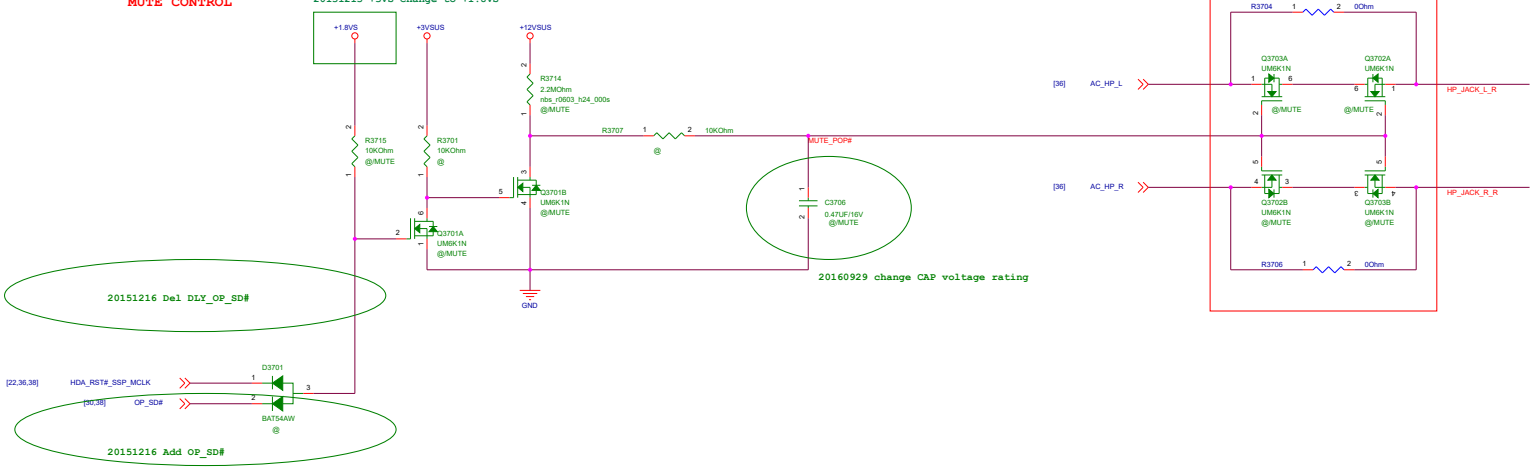




耳機pop noise mute線路

MUTE CONTROL

20151215 +3VS Change to +1.8VS

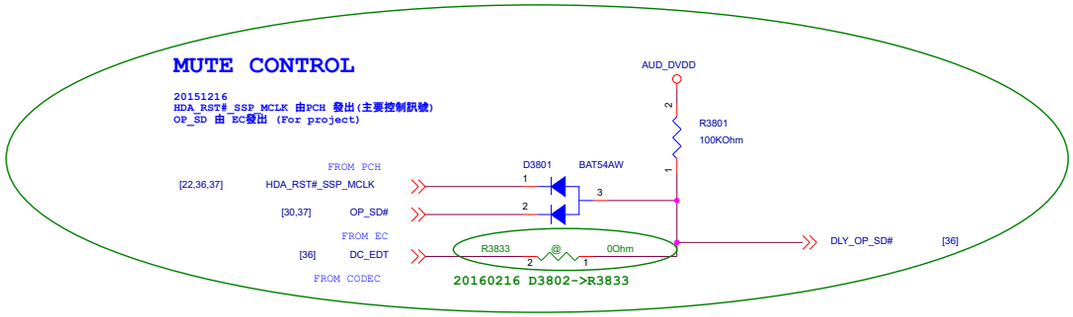


MUTE CONTROL

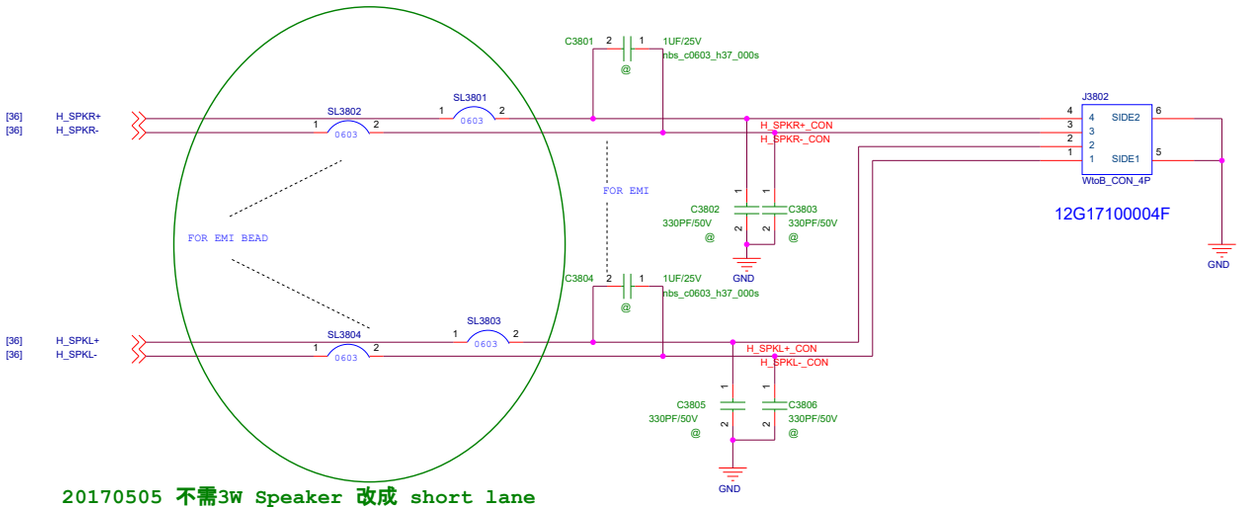
BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : IO Board-Audio Jack		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 37 of 102	

20160530
1. Del R3833 & Add D3801
2. AUD_DVDD_IO--->AUD_DVDD



Trace width for
H_SPKL+_O/H_SPKL-_O/H_SPKR+_O/H_SPKR-_OSpeaker
Speaker :4 ohm : 40mil ;8 ohm : 20mil



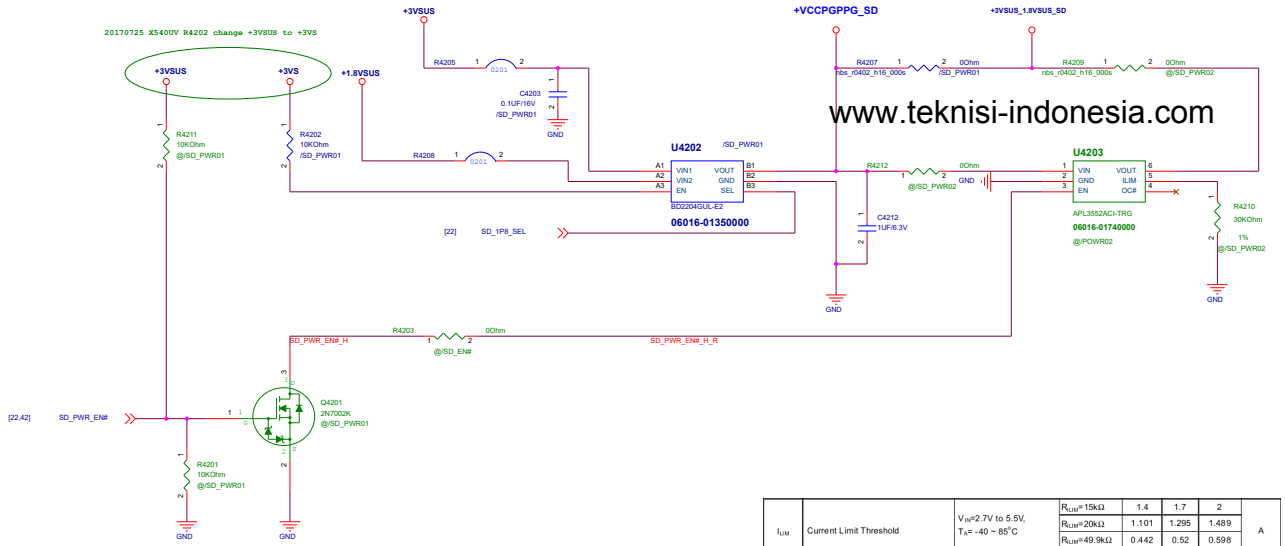
20170505 不需3W Speaker 改成 short lane

BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : HDD Board-Speaker		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 38 of 102	

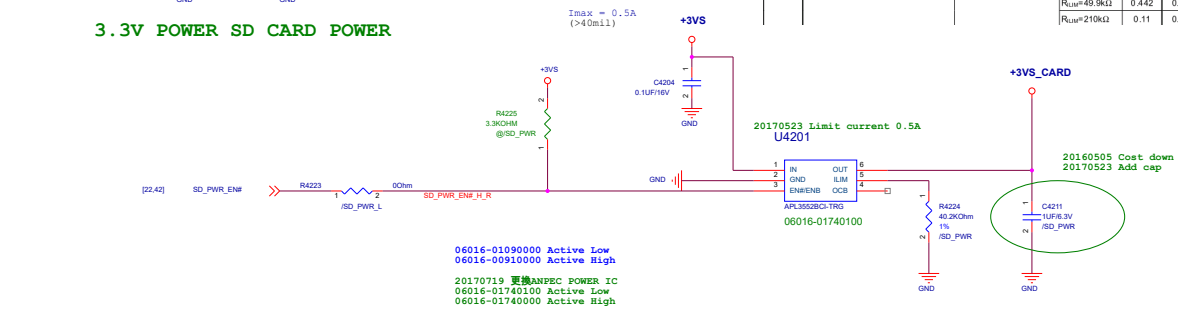
3.3V or 1.8V POWER SD CARD IO POWER

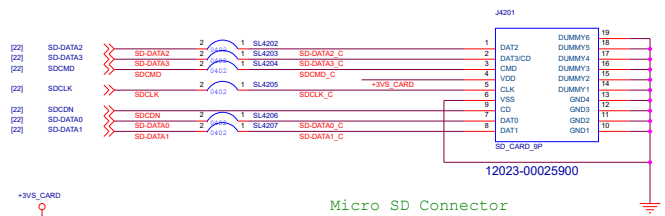
20170725 X540UV SD Power Condition
1./SD_PWR+/SD_PWR01
2./SD_PWR+/SD_PWR01-R4207+/SD_PWR02
3./SD_PWR+/SD_PWR03(@/SD_PWR03) ONLY 3.3V



I_{LIM}	Current Limit Threshold	V_{IN}=2.7V to 5.5V, T_A= -40 ~ 85°C	R_{LIM}=15kΩ	1.4	1.7	2	A
			R_{LIM}=20kΩ	1.101	1.295	1.489	
			R_{LIM}=49.9kΩ	0.442	0.52	0.598	
			R_{LIM}=210kΩ	0.11	0.13	0.15	

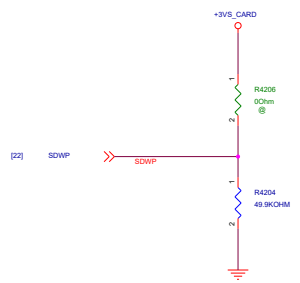
3.3V POWER SD CARD POWER

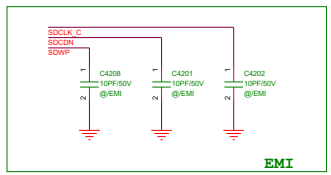


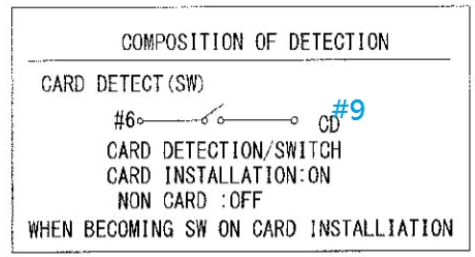


Micro SD Connector

PIN	SD mode
#1	DAT2
#2	DAT3/CD
#3	CMD
#4	V_{DD}
#5	CLK
#6	Vss
#7	DAT0
#8	DAT1
CD	CARD DETECT



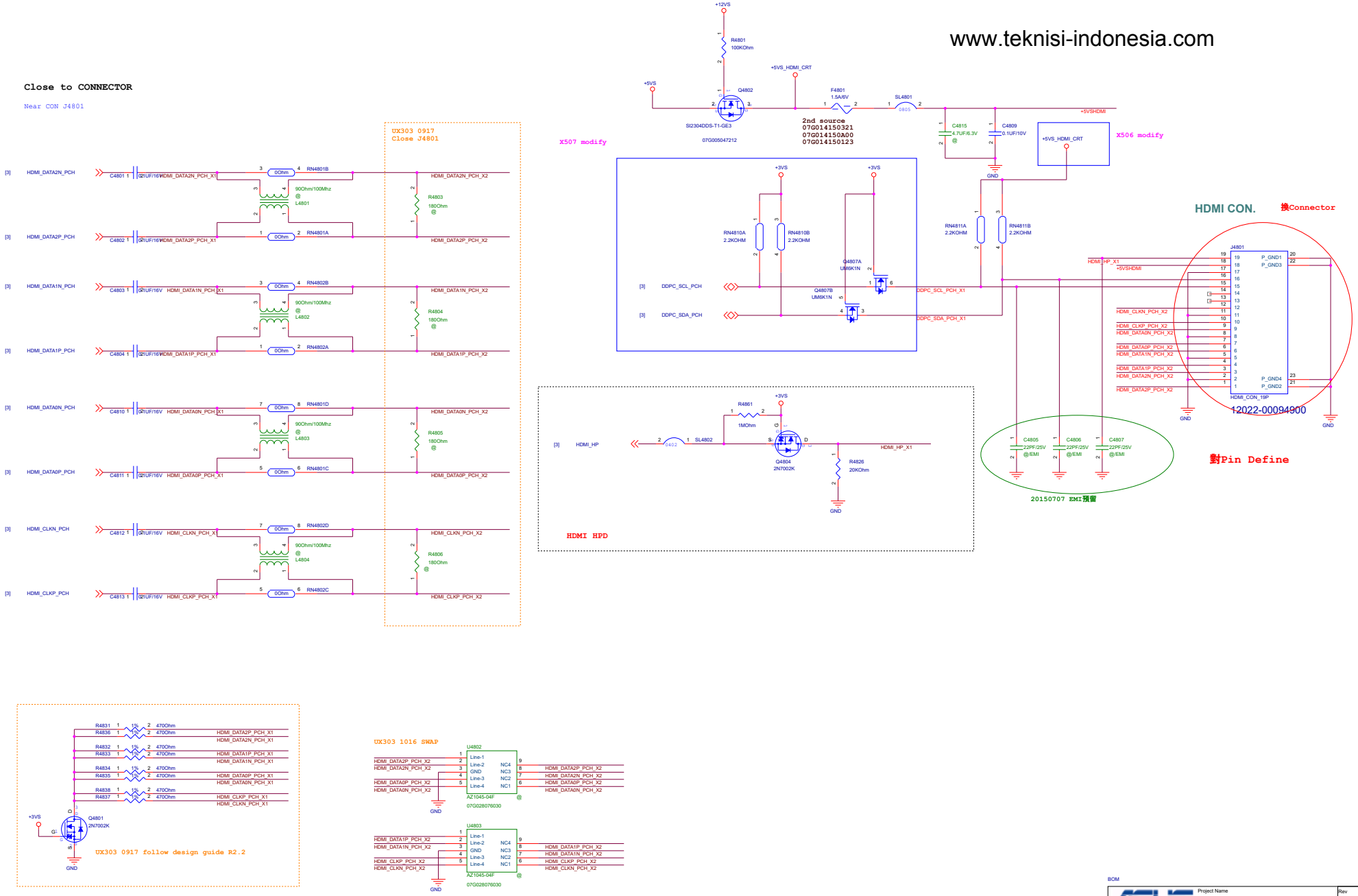




BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title :	CARD READER CONNECTOR	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 42 of 102	

HDMI type-A



BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : HDMI-type D		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 48 of 102	

eDP (LVDS) Panel

LCD +3VS_LCD Power

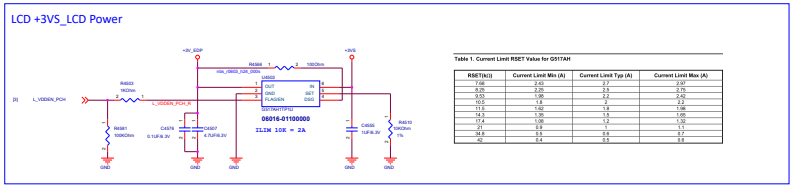
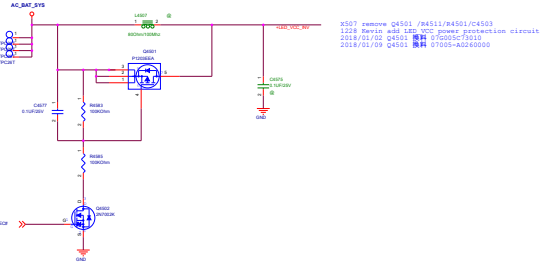


Table 1. Current Limit RSET Value for G51TAH

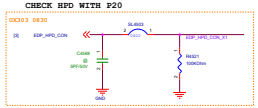
RSET(kΩ)	Current Limit Min (A)	Current Limit Typ (A)	Current Limit Max (A)
7.68	2.45	2.7	2.97
8.06	2.25	2.5	2.75
9.53	1.96	2.2	2.42
10.5	1.8	2	2.2
11.5	1.62	1.8	1.98
14.3	1.35	1.5	1.65
17.4	1.08	1.2	1.32
21	0.9	1	1.1
34.8	0.5	0.6	0.7
42	0.4	0.5	0.6



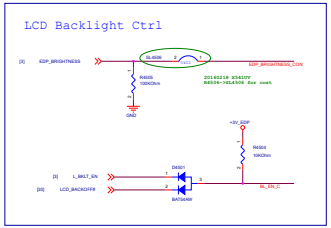
X507 remove Q4501 /R4511/R4501/C4503
1228 Kevin add LED VCC power protection circuit
2018/01/02 Q4501 換料 07G005C73010
2018/01/09 Q4501 換料 07005-A0260000

CHECK HPD WITH P20

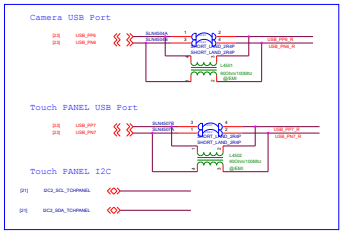
SW303 0830



LCD Backlight Ctrl



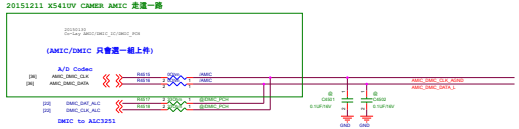
Camera USB Port



Touch PANEL USB Port

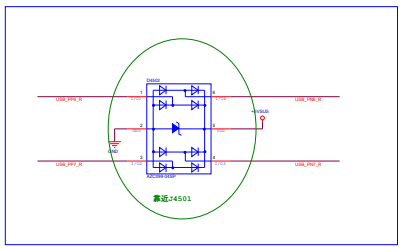
Touch PANEL I2C

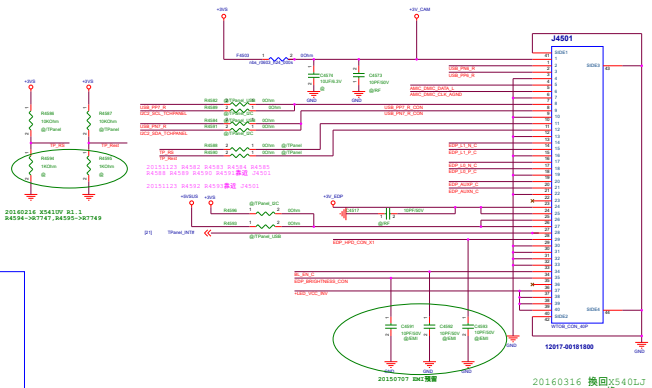
20151211 X541UV CAMER AMIC 走這一路



eDP Panel differential signals

X507 after SR modify to Shortland

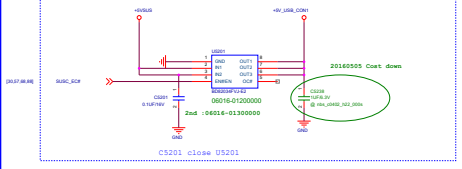




20160316 換回X540LJ
20160701 LBS換footprint

20160503
#1.1 Add USB power SW for power protect

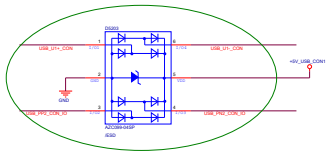
USB3.0 port 0 Power SW for Power Protect



X507UBA ER Change C5238 pakage for placement

USB3.0 ESD-Protection

USB 2.0 ESD-Protection

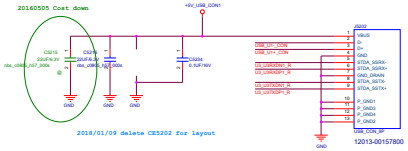


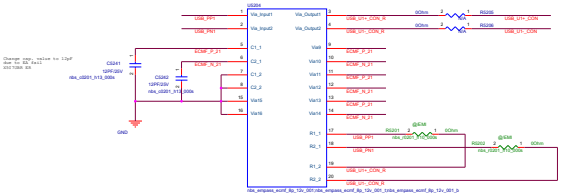
X540UPR merge 2 USB port to 1ESD component_20170331

USB3.0_Port 0

20160505 Cost down

2018/01/09 delete CE5202 for layout



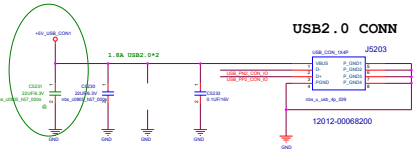


USB2.0_Port 2

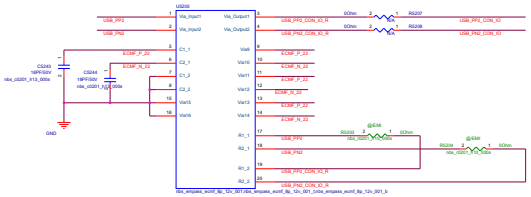
X540UJ DEL

20170505 X540UPR2 Add USB2.0

USB2.0 CONN



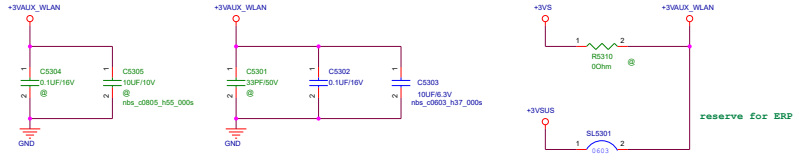
2018/01/09 delete CE5231 for layout



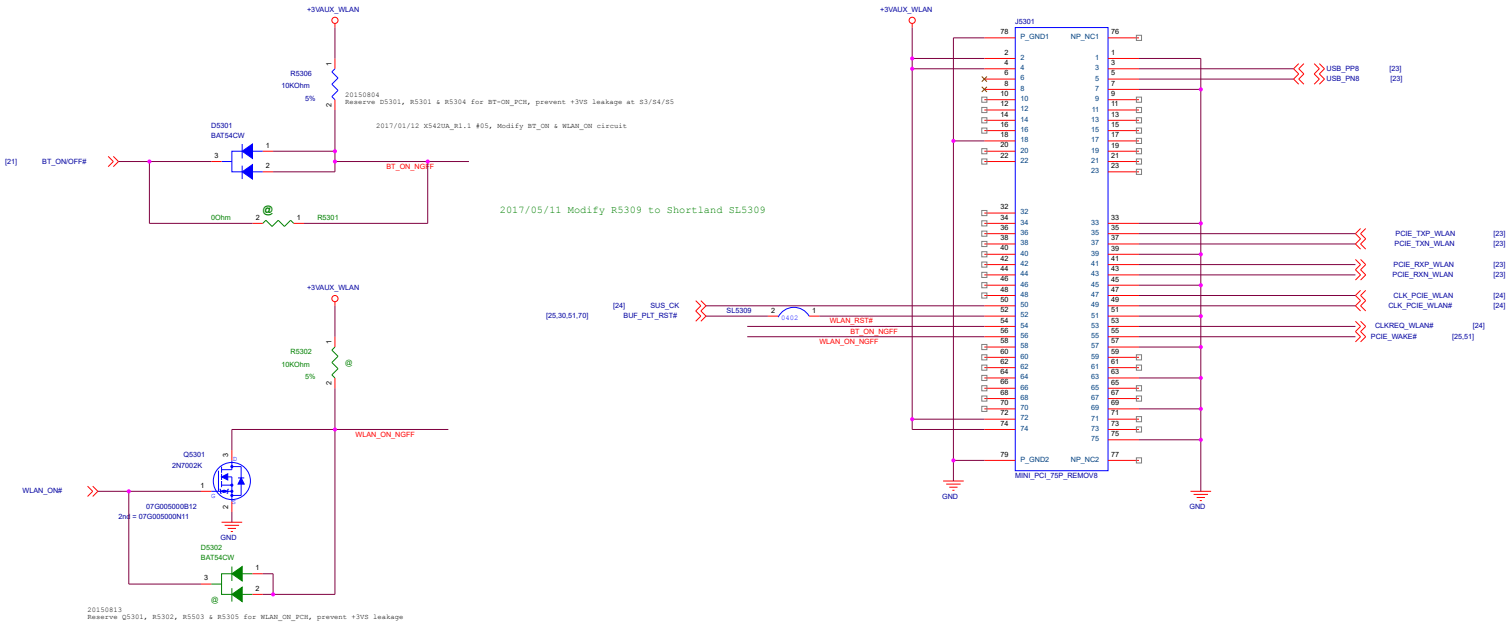
BOM

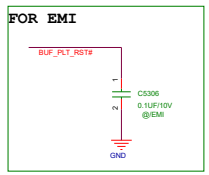
ASUS	Project Name: X507UA/UV		Rev: 49.0
Title : USB 3.0 + 2.0 CONN.			
Size: D	Dept.: ASUSTeK COMPUTER INC	Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet: 52	of: 102	

0520-11 Dean Merge BOM L3000 L5301 L2603 L2604 L2707
=> 1200HM/2A 09G013120802



0309-11 Dean_cost check keypart list上的WLAN均無+1.5V的需求
=> unstuff C5304, C5305



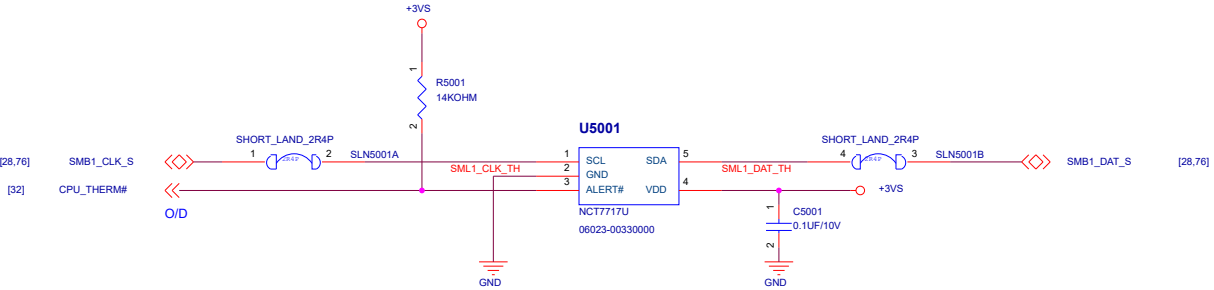


2017/05/11 BT/WLAN ON OFF Follow X452UQ PR

<Variant Name>

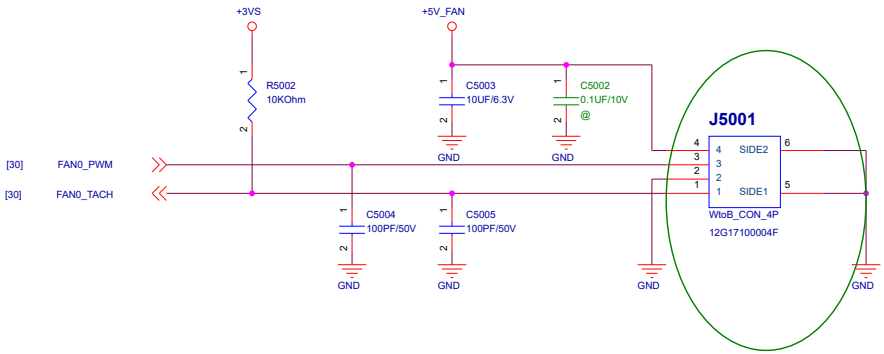
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : MINICARD(WLAN)		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 53 of 102	

CPU Thermal Sensor



2018/01/15 U5001 change 06023-00330000 for BOM Builder System

DC FAN Control



20160316 換回X540LJ

5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

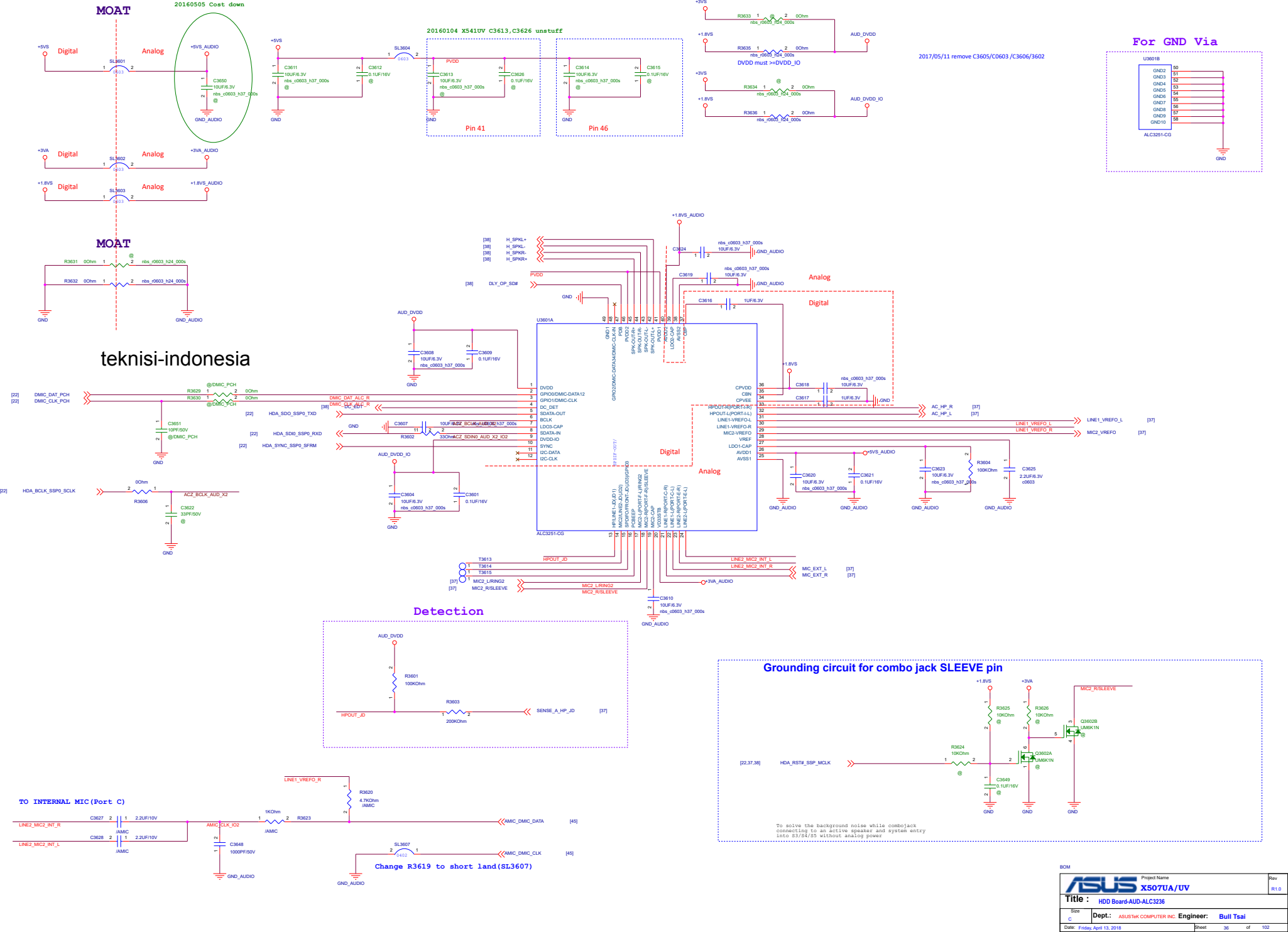
PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

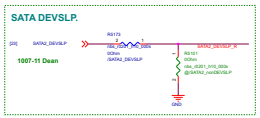
----------OTHER SIGNALS
10 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
10 mils
----------OTHER SIGNALS
Avoid FSB,Power

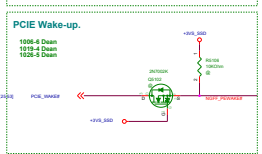
<Variant Name>

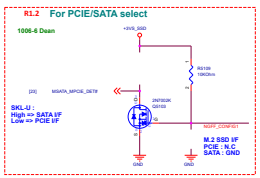
ASUSTeK COMPUTER INC. NB3	Title : 50_FAN_Thermal Sensor	
	Engineer: Bull Tsai	
Size: B	Project Name: X507UA/UV	Rev: R1.0
Date: Friday, April 13, 2018	Sheet 50 of 102	


MOAT
20160505 Cost down
+5VS
Digital
Analog
+5VS_AUDIO
SL3601
C3650
10UF/6.3V
nbs_c0603_h37_000s
GND_AUDIO
+3VA
+3VA_AUDIO
SL3602
+1.8VS
+1.8VS_AUDIO
SL3603
20160104 X541UV C3613,C3626 unstuff
C3611
10UF/6.3V
C3612
0.1UF/16V
SL3604
PVDD
C3613
C3626
Pin 41
C3614
C3615
Pin 46
+3VS
R3633
0Ohm
nbs_r0603_h24_000s
AUD_DVDD
R3635
DVDD must >=DVDD_IO
R3634
AUD_DVDD_IO
R3636
2017/05/11 remove C3605/C0603 /C3606/3602
For GND Via
U3601B
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
ALC3251-CG
MOAT
R3631
R3632
teknisi-indonesia
U3601A
DVDD
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
DC_DET
SDATA-OUT
BCLK
LDO3-CAP
SDATA-IN
DVDD-IO
SYNC
I2C-DATA
I2C-CLK
CPVDD
CBN
CPVEE
HPOUT-R(PORT-I-R)
HPOUT-L(PORT-I-L)
LINE1-VREFO-L
LINE1-VREFO-R
MIC2-VREFO
VREF
LDO1-CAP
AVDD1
AVSS1
ALC3251-CG
Analog
Digital
DMIC_DAT_PCH
DMIC_CLK_PCH
R3629
R3630
C3651
10PF/50V
HDA_SDO_SSP0_TXD
HDA_SDI0_SSP0_RXD
HDA_SYNC_SSP0_SFRM
HDA_BCLK_SSP0_SCLK
R3606
C3622
33PF/50V
ACZ_BCLK_AUD_X2
R3602
33OhmACZ_SDIN0_AUD_X2_IO2
C3604
C3601
C3607
C3608
C3609
C3610
C3616
C3617
C3618
C3619
C3620
C3621
C3623
C3624
C3625
2.2UF/6.3V
R3604
100KOhm
AC_HP_R
AC_HP_L
LINE1_VREFO_L
LINE1_VREFO_R
MIC2_VREFO
H_SPKL+
H_SPKL-
H_SPKR-
H_SPKR+
DLY_OP_SD#
HPOUT_JD
T3613
T3614
T3615
MIC2_L/RING2
MIC2_R/SLEEVE
LINE2_MIC2_INT_L
LINE2_MIC2_INT_R
MIC_EXT_L
MIC_EXT_R
Detection
R3601
100KOhm
R3603
200KOhm
SENSE_A_HP_JD
Grounding circuit for combo jack SLEEVE pin
R3625
10KOhm
R3626
10KOhm
Q3602B
UM6K1N
Q3602A
R3624
C3649
0.1UF/16V
HDA_RST#_SSP_MCLK
To solve the background noise while combojack connecting to an active speaker and system entry into 83/84/85 without analog power
TO INTERNAL MIC(Port C)
C3627
C3628
2.2UF/10V
/AMIC
AMIC_CLK_IO2
R3620
4.7KOhm
R3623
1KOhm
C3648
1000PF/50V
AMIC_DMIC_DATA
AMIC_DMIC_CLK
SL3607
Change R3619 to short land(SL3607)
BOM
Project Name
X507UA/UV
Rev
R1.0
Title :
HDD Board-AUD-ALC3236
Size
C
Dept.:
ASUSTeK COMPUTER INC.
Engineer:
Bull Tsai
Date:
Friday, April 13, 2018
Sheet
36
of
102

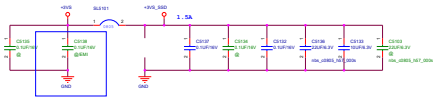
SSD CONN.



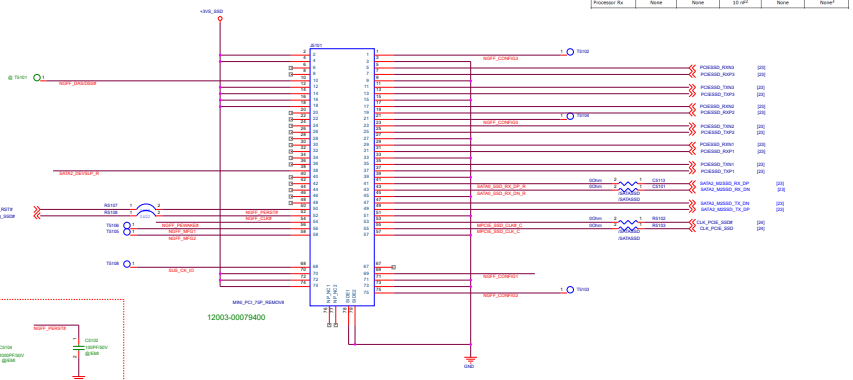


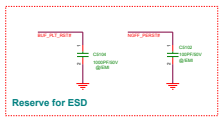


0310-1 Dean
0314-2 Dean



6/8 Jacky add 0.1UF for ESD





36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

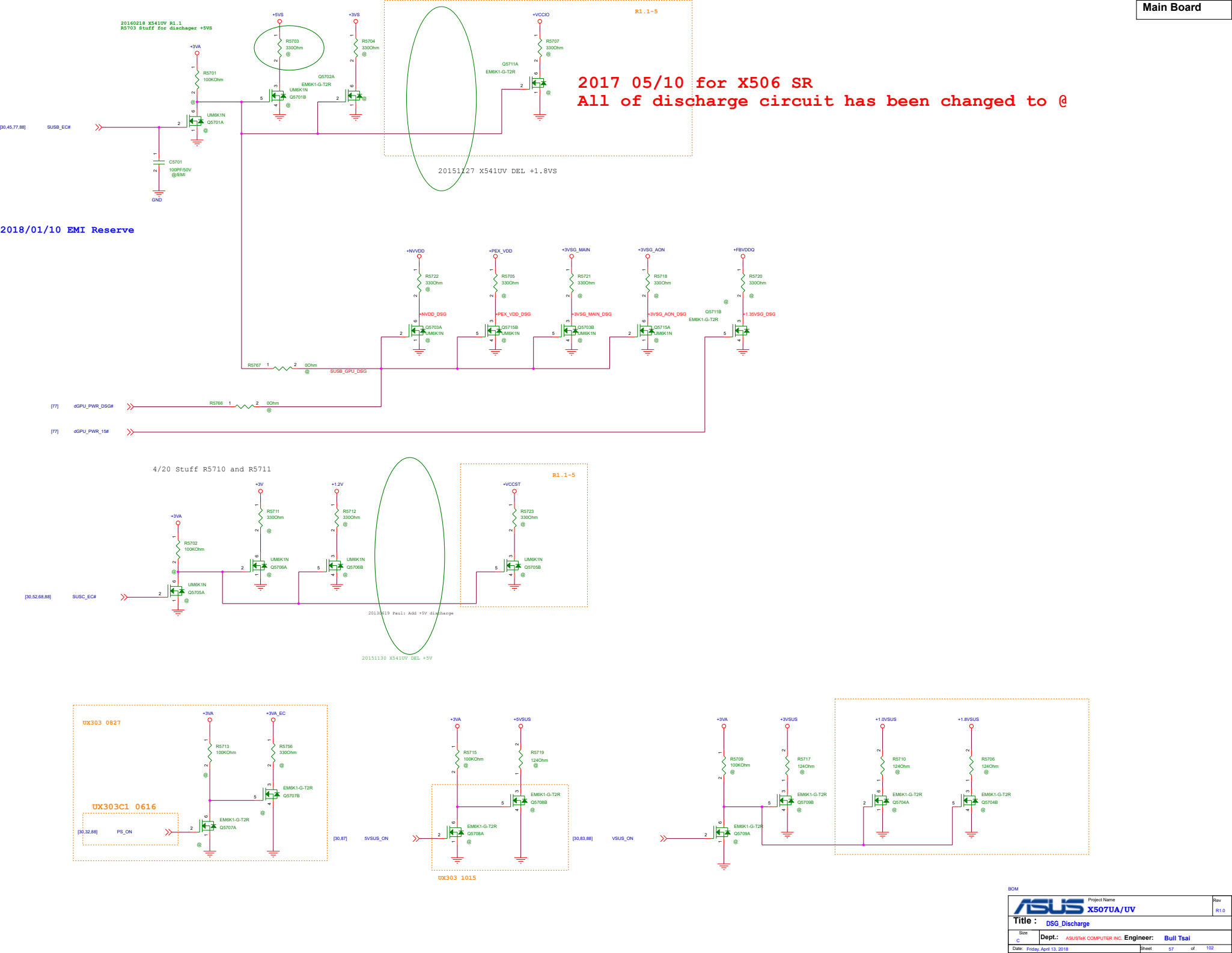
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

Table 36-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

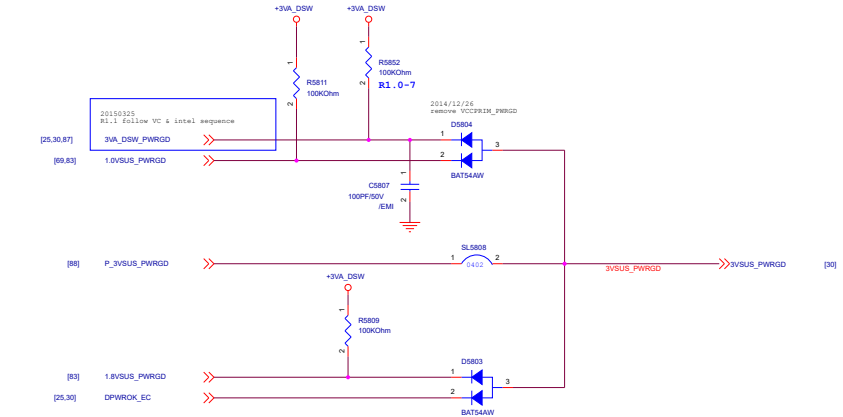
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

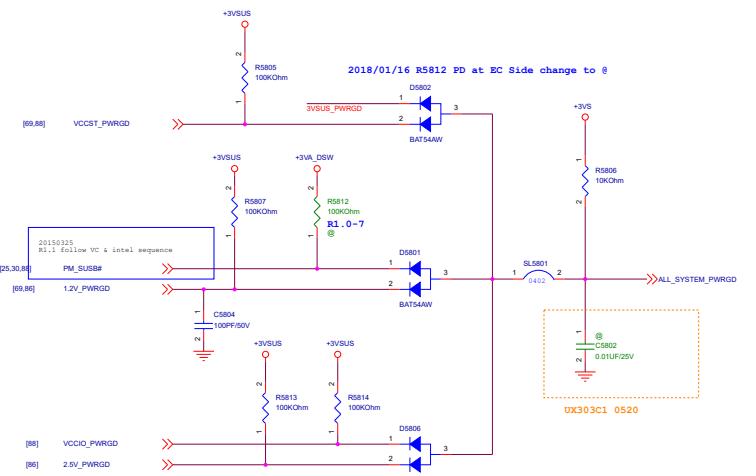
BOM						
ASUS	Project Name: X507UA/UV				Rev: 40.0	
Title : SATA HDD & ODD						
Size: A3	Dept.: ASUSTeK COMPUTER INC	Engineer: Bull Tsai				
Date: Friday, April 19, 2019		Sheet: 101	of: 103			

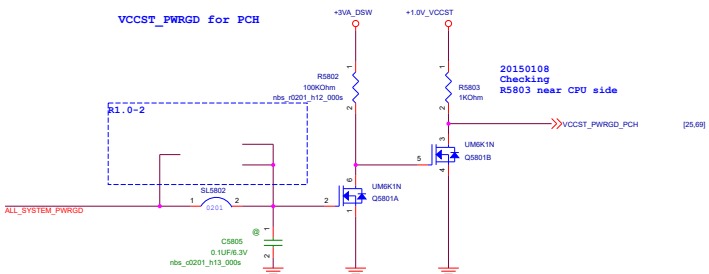


BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : DSG_Discharge		
Size: C	Dept.: ASUSTeK COMPUTER INC	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 57 of 102	



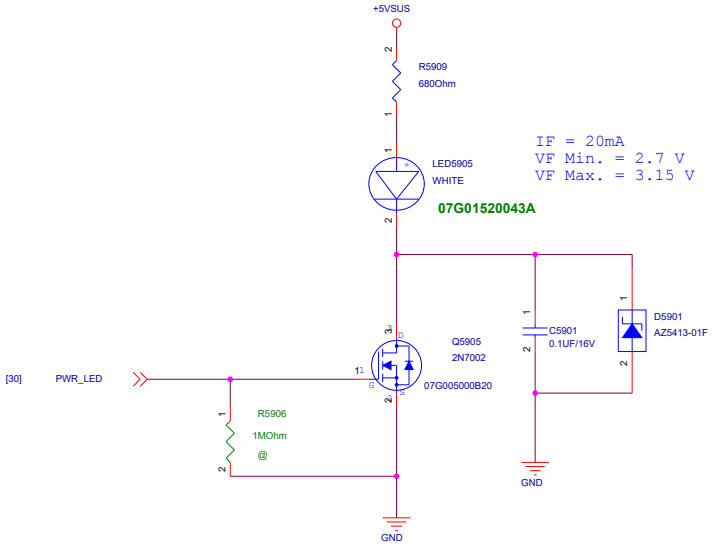




BOM

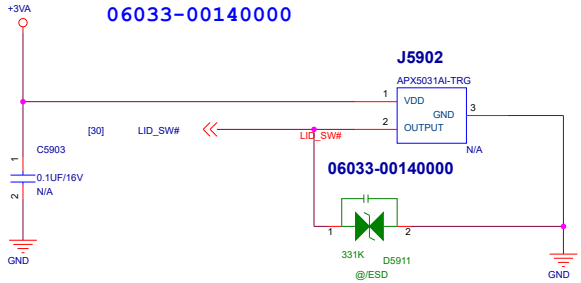
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : PRO_Protect		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 58 of 102	

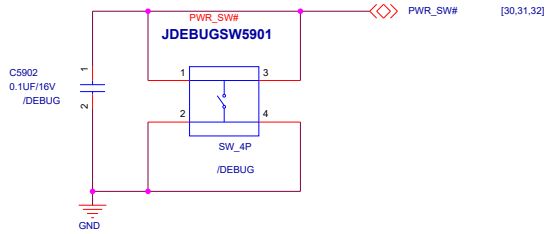
POWER LED



HALL SENSOR
06033-00140000

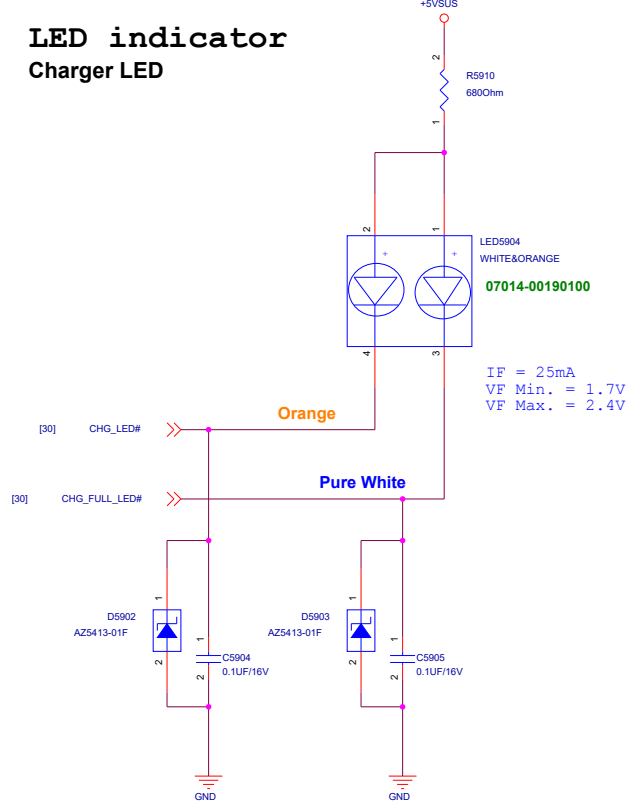
current: 1m





LED indicator

Charger LED

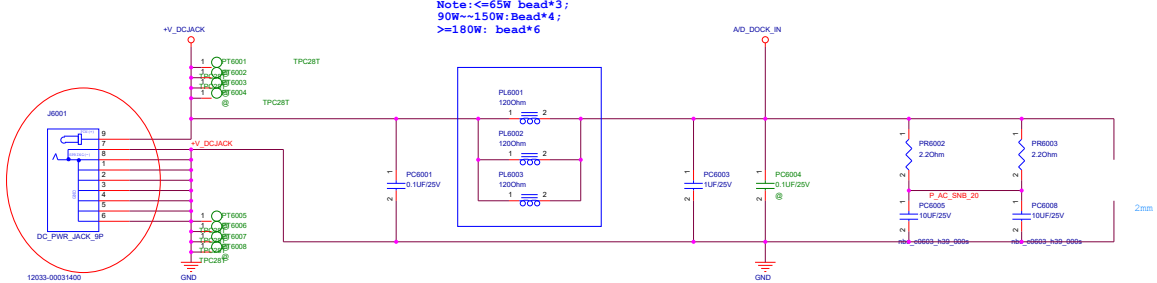


CAP Lock LED

WIRELESS/ BT LED

<Variant Name>

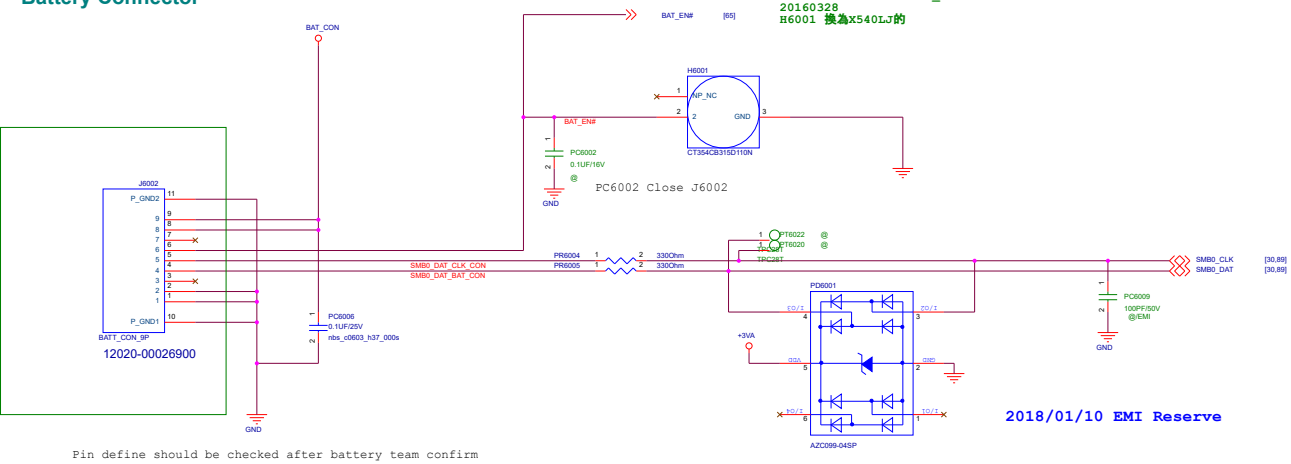
ASUSTeK COMPUTER INC. NB8	Title : 59_Power & WIFI & CAP LED	
	Engineer: Bull Tsai	
Size: B	Project Name: X507UA/UV	Rev: R1.0
Date: Friday, April 13, 2018	Sheet 59 of 102	



換Connector　　整個 GND Shape 都要跟PIN腳連起來

Battery Connector

20150706
H6001為一顆螺絲接通 BAT_EN# 和 GND,電池才開始送電
20160328
H6001 換為X540LJ的



2018/01/10 EMI Reserve

Pin define should be checked after battery team confirm

X507UBR ER change to 12020-00026900

<Variant Name>

Project Name: X507UBR		Rev: R1.0
Title : 60_DC_DC & BAT IN		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: SS	
Date: Friday, April 13, 2018	Sheet 60 of 102	

TOP CPU NUTF

TOP CPU NUT C

H6507 nbs_nut_1p_475 CT236CB176D146 13020-03890400 GND

H6514 CT189B180D150 nbs_nut_1p_403 13020-03890300 GND

H6508 nbs_nut_1p_415 CT236CB176D146 13020-03890400 GND

TOP CPU NUT B

H6509 CT256BRID146 nbs_nut_1p_402 13020-03890200 GND

TOP VGA NUT C

H6515 CT189B180D150 nbs_nut_1p_407 /VGA 13020-03890300 GND

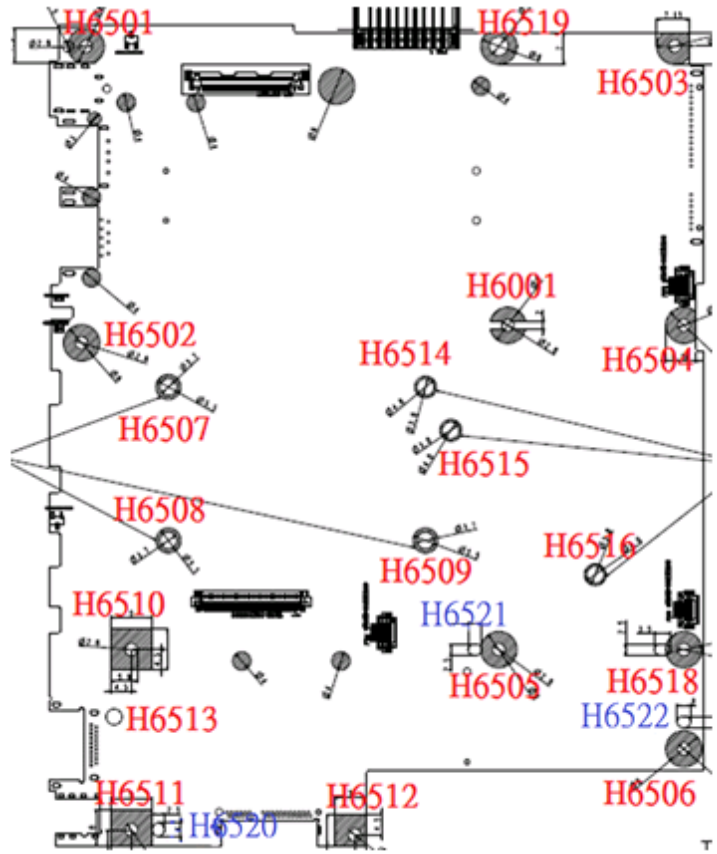
H6516 CT189B180D150 nbs_nut_1p_409 /VGA 13020-03890300 GND

BOT NUT A

H6513 CT236CB168D138 13020-03890100 GND

BOT NUT D

H6519 CT236CB195D165 13020-03890000 GND



H6510 ST354CB315D110 GND

H6511 ST354CB315D110 GND

H6512 ST354CB315D110 GND_AUDIO

H6501 GND NP_NC 2D_D98N_D110 GND

H6518 GND NP_NC 2D_D110_D138X98N GND

H6502 C315D94 GND

H6505 C315D110 GND

H6506 C315D110 GND

H6503 CRT281X276RB276X286D110 GND

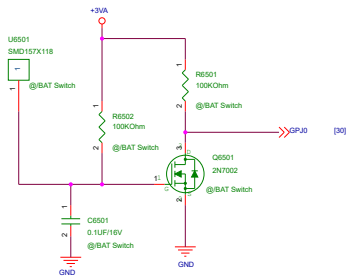
H6504 CRT259X315RB293X354D110 GND

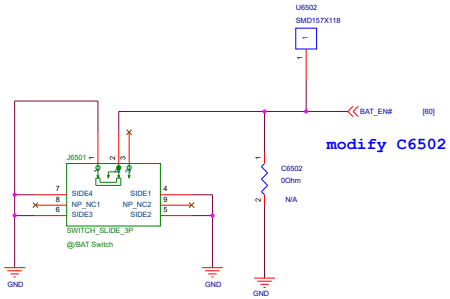
NPTH

H6520 O118X98DO118X98N

H6521 O118X98DO118X98N

H6522 O122X98DO122X98N





modify C6502 to 0 Ohm for BAT_EN# always low

<Variant Name>

ASUSTeK COMPUTER INC. NB4

Title : 65_ME_Conn & Skew Hole

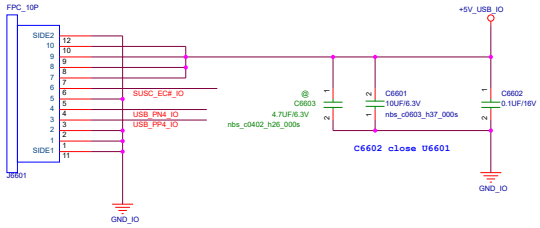
Engineer: Bull Tsai

Size	Project Name	Rev
C	X507UA/UV	R1.0

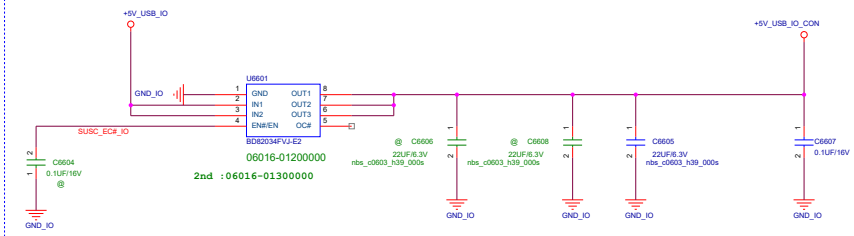
Date: Friday, April 13, 2018 Sheet 65 of 102

20150513
R1.1 Add USB power SW for power protect

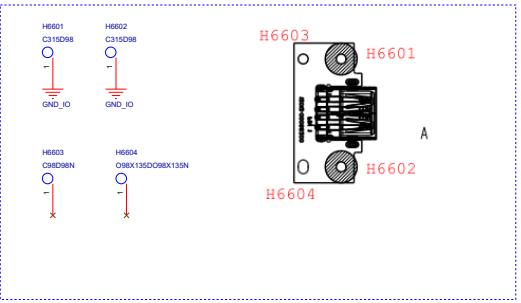
12018-00072600

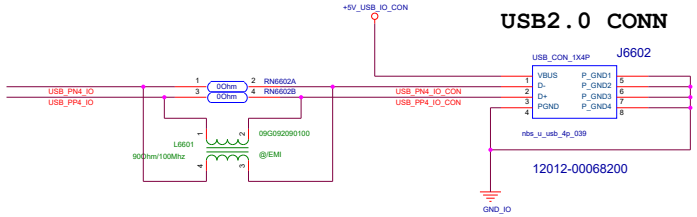


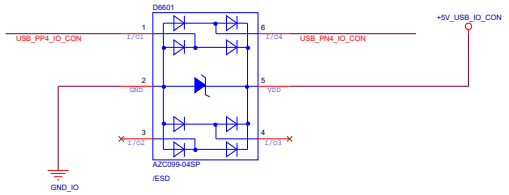
USB2.0_Port 4



HOLE



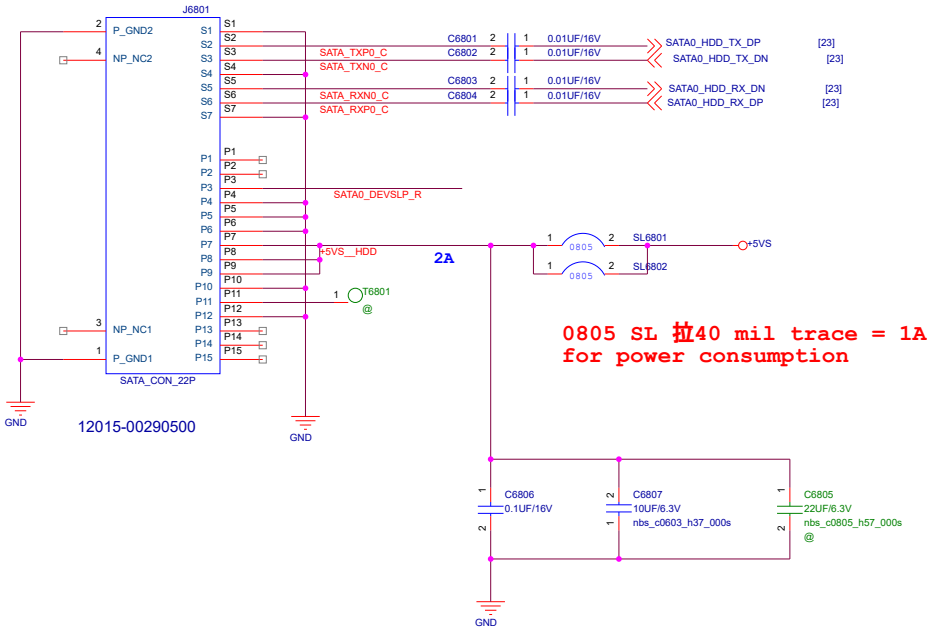




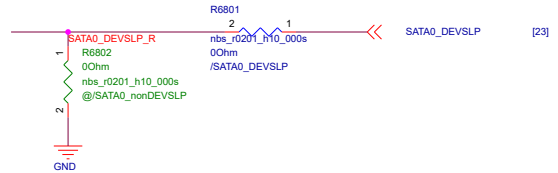
BOM

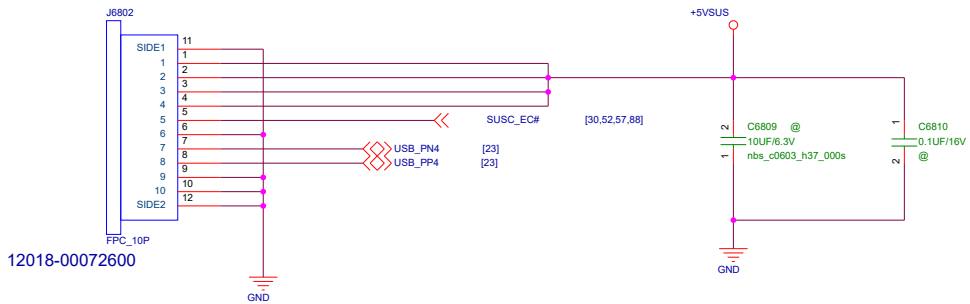
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : IO_USB		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 66 of 102	

SATA HDD



SATA DEVSLP.

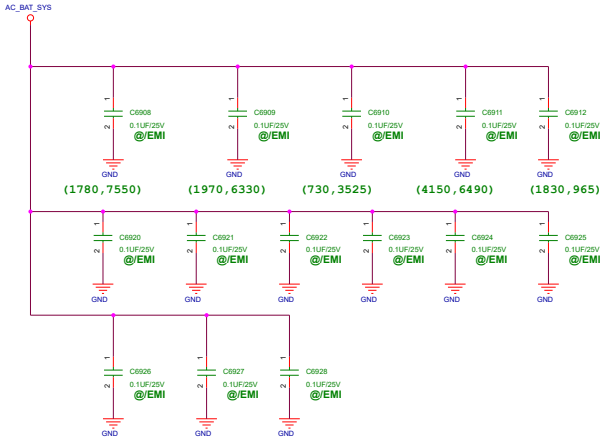




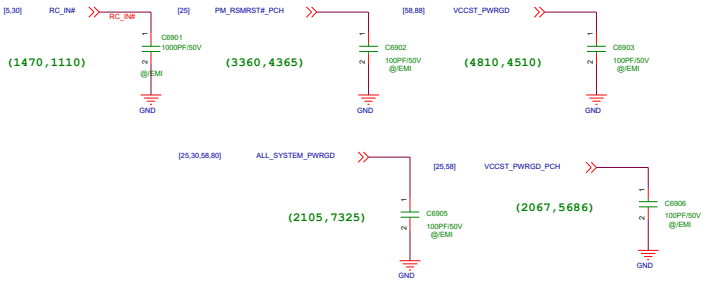
BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : B TO B CONNECTOR		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 68 of 102	

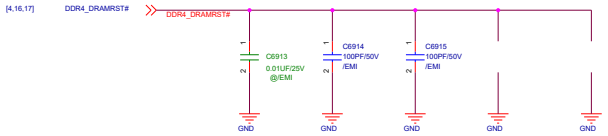
EMI AC_BAT_SYS CAP

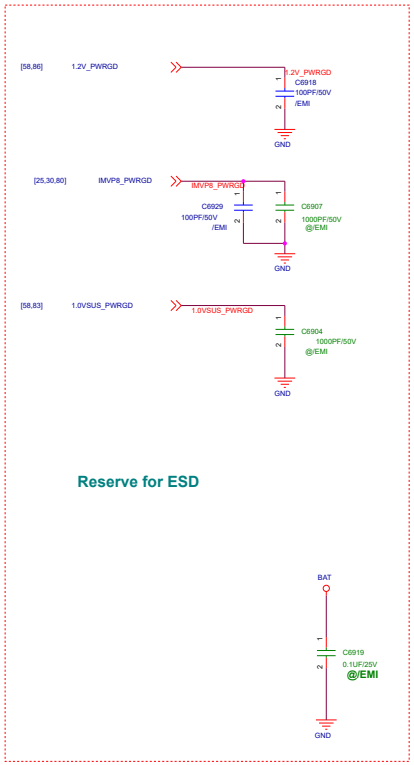


EMI CAP

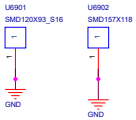


DDR4 CAPs



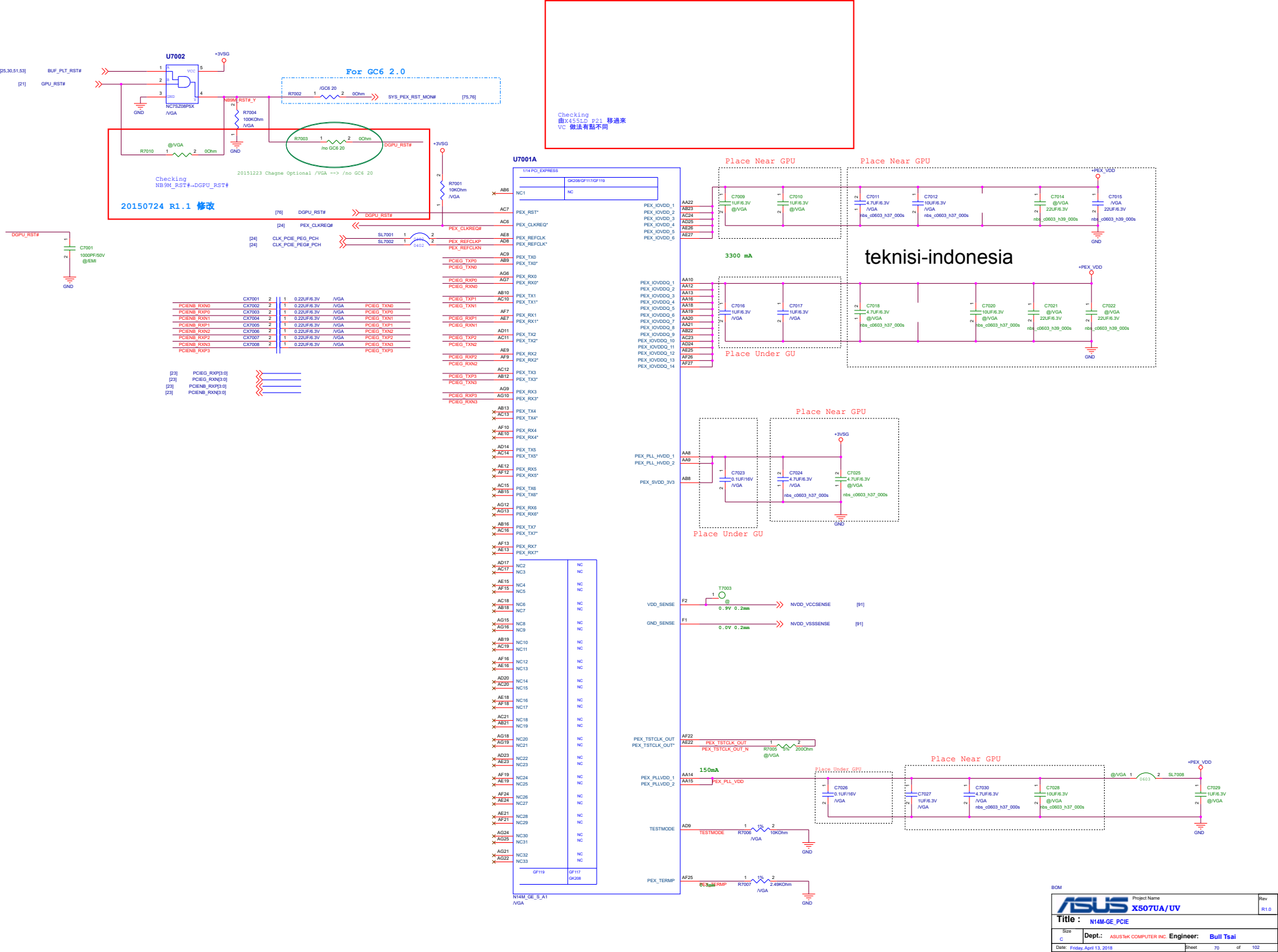


GASKET



BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : EMI		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 69 of 102	


U7002
For GC6 2.0
/GC6 20
R7002
0Ohm
SYS_PEX_RST_MON#
[75,76]
BUF_PLT_RST#
GPU_RST#
NB9M_RST#_Y
R7004
100KOhm
/VGA
R7003
/no GC6 20
DGPU_RST#
R7010
@/VGA
Checking
NB9M_RST#→DGPU_RST#
20150724 R1.1 修改
20151223 Chagne Optional /VGA --> /no GC6 20
Checking
由X455LD P21 移過來
VC 做法有點不同
U7001A
R7001
10KOhm
/VGA
PEX_CLKREQ#
PEX_REFCLKP
PEX_REFCLKN
C7001
1000PF/50V
@/EMI
Place Near GPU
Place Under GU
3300 mA
teknisi-indonesia
+PEX_VDD
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDD_6
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_PLL_HVDD_1
PEX_PLL_HVDD_2
PEX_SVDD_3V3
+3VSG
VDD_SENSE
GND_SENSE
NVDD_VCCSENSE
NVDD_VSSSENSE
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*
150mA
PEX_PLLVDD_1
PEX_PLLVDD_2
TESTMODE
PEX_TERMP
2.49KOhm
N14M_GE_S_A1
/VGA
BOM
Project Name
X507UA/UV
Rev
R1.0
Title :
N14M-GE_PCIE
Size
C
Dept.:
ASUSTeK COMPUTER INC.
Engineer:
Bull Tsai
Date:
Friday, April 13, 2018
Sheet
70
of
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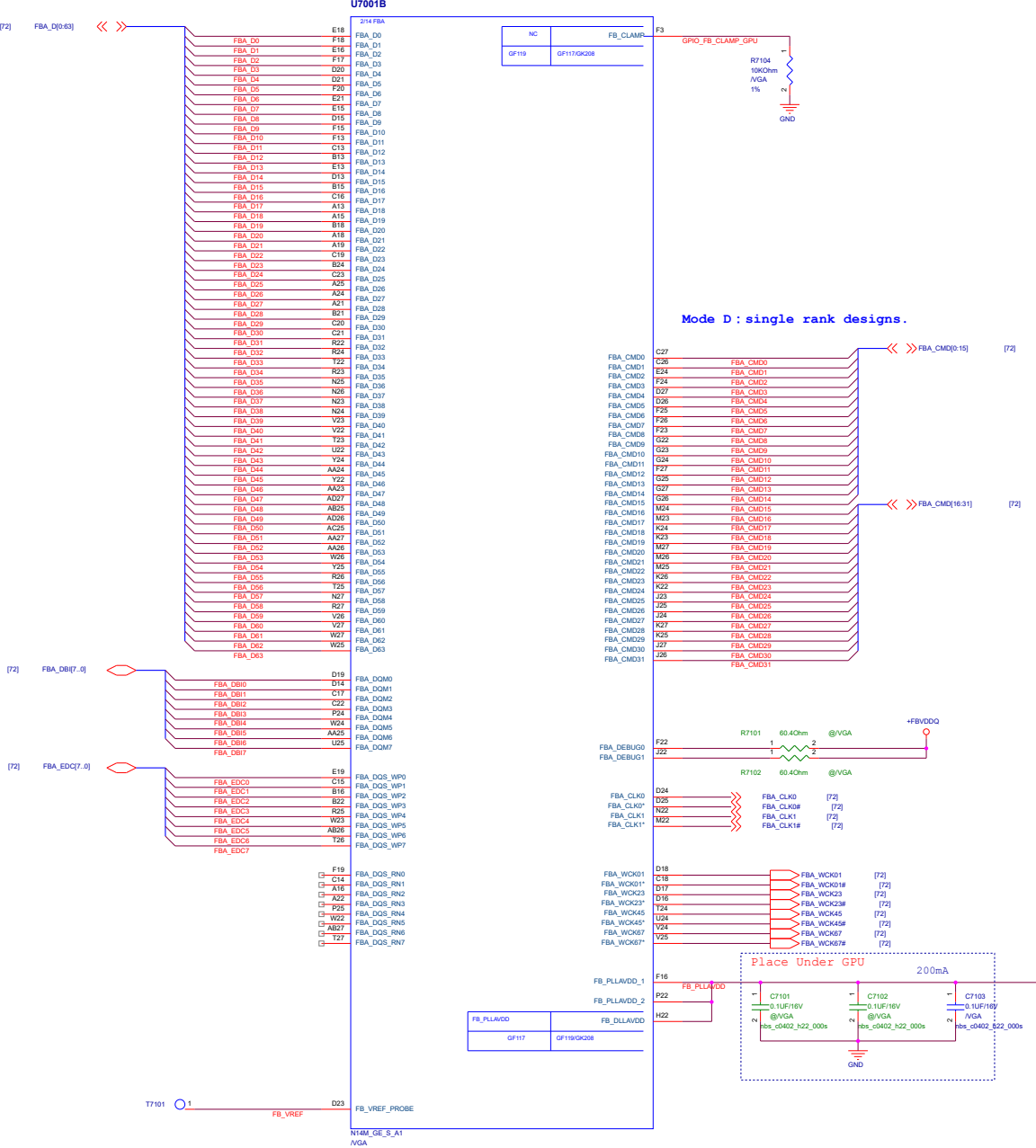


Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.

<Variant Name>

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : N14M-GE_FB-IF		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 71 of 102	

N15與N14不一樣。
3V3_AON

U7001C

Place Near Balls
150mA
C7301 0.1UF/16V /VGA
C7302 0.1UF/16V /VGA
C7303 0.1UF/16V @/VGA
Place Near GPU
+3VSG
C7304 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
GND

Place Near Balls
150mA
C7331 0.1UF/16V /VGA
C7305 0.1UF/16V /VGA
C7329 0.1UF/16V @/VGA
Place Near GPU
+3VSG_MAIN
C7330 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
GND

LD, GC6 20

CONFIGURABLE POWER CHANNELS
* nc on substrate

N14M_GE_S_A1

/VGA

U7001D

+FBVDDQ 2.5A

Place Under GPU
C7306 0.1UF/16V /VGA
C7308 1UF/6.3V /VGA
C7310 4.7UF/6.3V /VGA nbs_c0603_h37_000s
C7307 1UF/6.3V @/VGA
C7309 1UF/6.3V @/VGA
C7311 /VGA 10UF/6.3V nbs_c0603_h37_000s
5/16 C7311-10uF C7312-22uF for PWR Noise
GND

Place Near GPU
C7312 /VGA 22UF/6.3V nbs_c0603_h39_000s
C7313 /VGA 22UF/6.3V nbs_c0603_h39_000s
GND

N14M_GE_S_A1

/VGA

+FBVDDQ
/VGA R7301 40.2Ohm FB_CAL_PD_VDDQ
/VGA R7302 40.2Ohm FB_CAL_PU_GND
/VGA R7303 60.4Ohm FB_CAL_TERM_GND
GND

GDDR5 = 40.2 ohm
DDR3 = 42.2 ohm

GDDR5 = 60.4 ohm
DDR3 = 51.1 ohm

U7001F

N14M_GE_S_A1

/VGA

U7001E

+NVVDD 21.22A

Place Near Balls and Under GPU
C7314 0.1UF/16V /VGA
C7317 0.1UF/16V @/VGA
C7318 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7321 10UF/6.3V /VGA
C7324 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7327 4.7UF/6.3V /VGA nbs_c0603_h37_000s
C7315 0.1UF/16V /VGA
C7319 10UF/6.3V /VGA
C7322 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7325 10UF/6.3V /VGA
C7328 4.7UF/6.3V /VGA nbs_c0603_h37_000s
C7316 0.1UF/16V /VGA
C7320 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7323 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7326 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
GND

C7334 10UF/6.3V /VGA
GND

Optional caps Place Near GPU

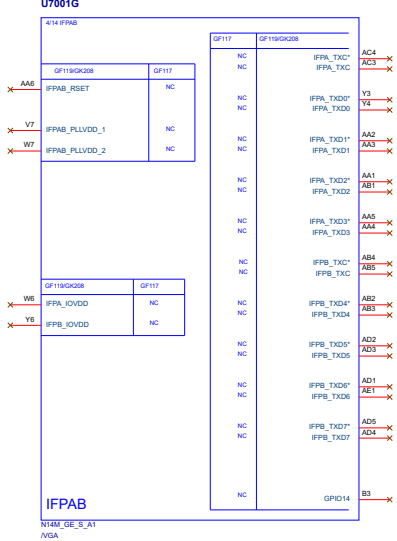
N14M_GE_S_A1

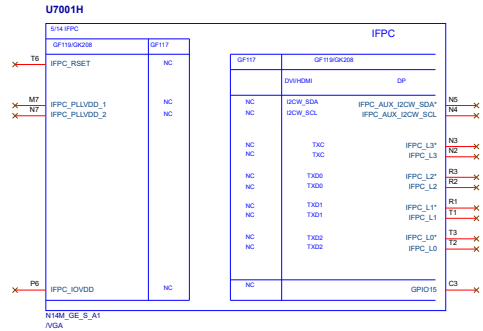
/VGA

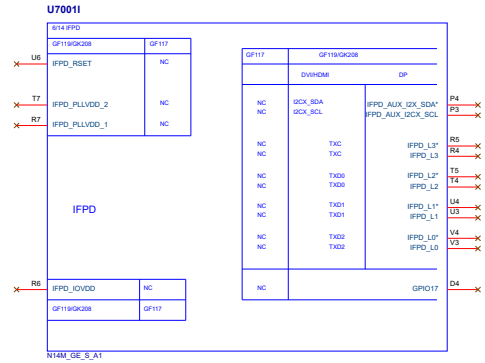
BOM

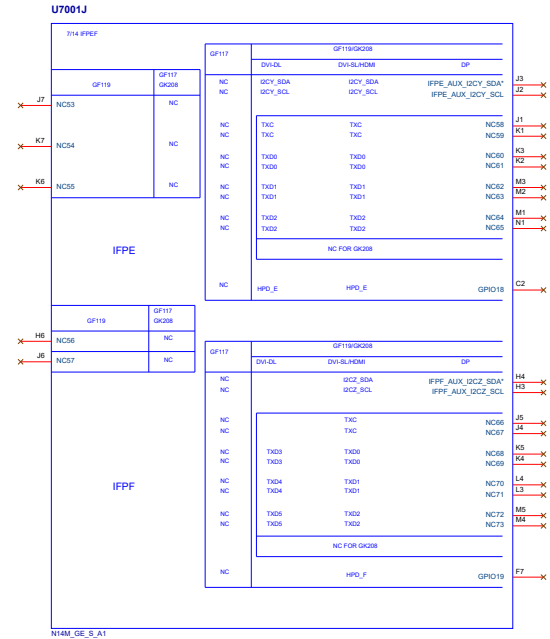
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : N14M-GE-VDD		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 73 of 102	

LVDS

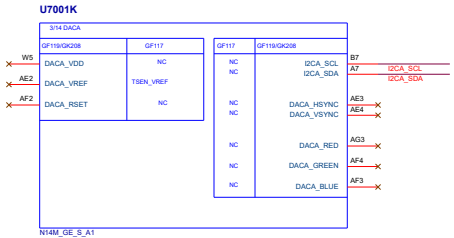


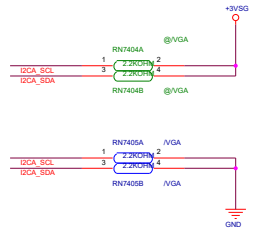






CRT



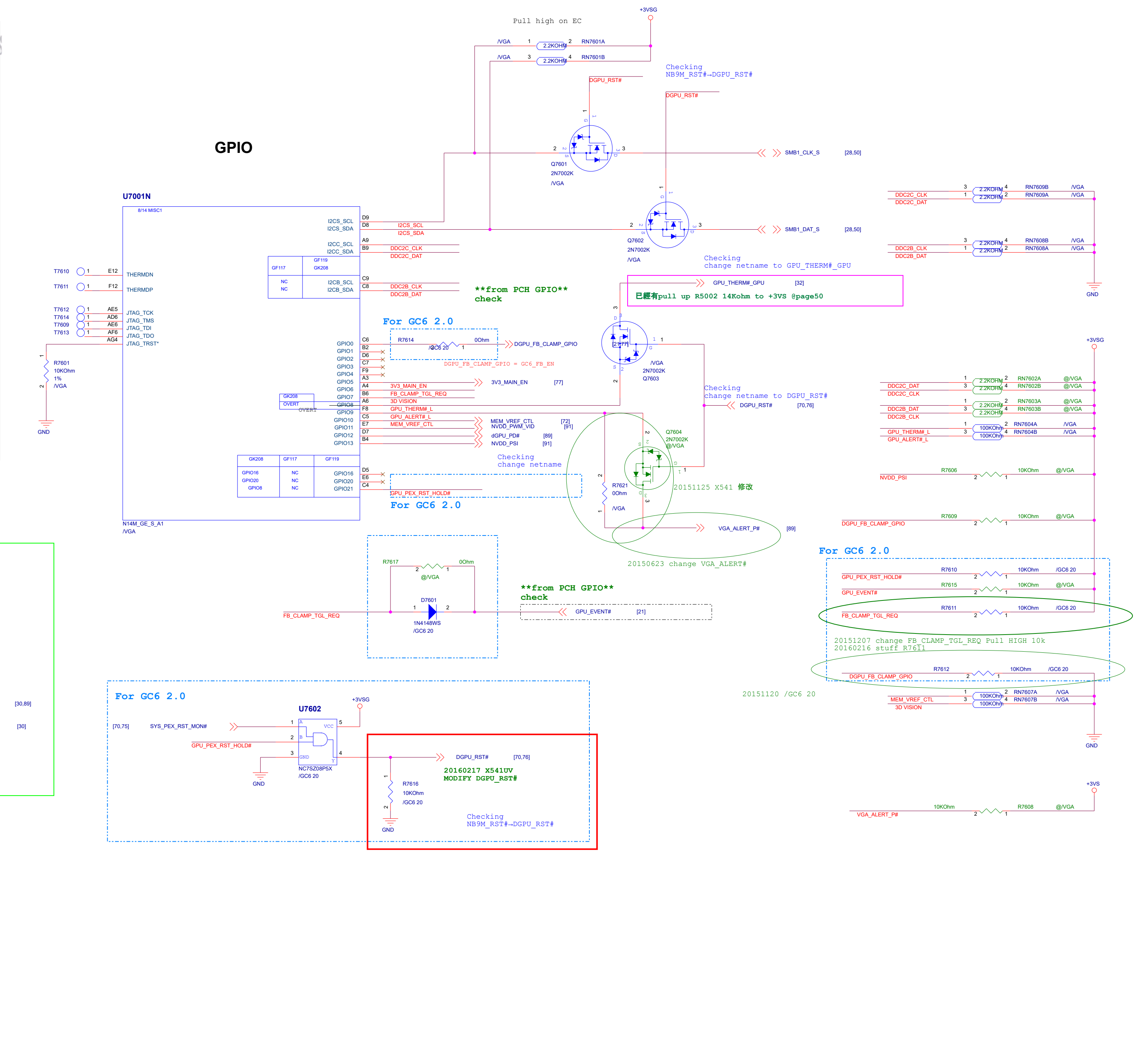


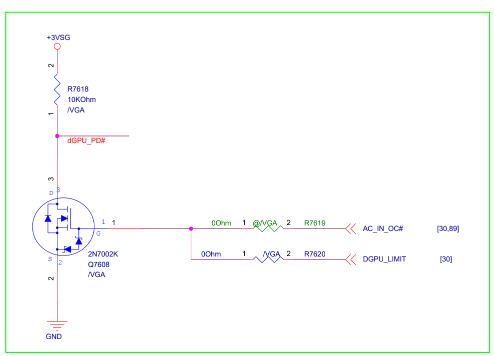
BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : N14M-GE_DISPLAY		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 74 of 102	

Table 12-1. GB2B-64 and GB4B-128 GPIO Description

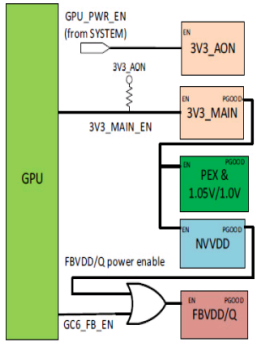
Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON





BOM

Project Name	X507UA/UV	Rev R1.0
Title :	N14M-GE_GPIO	
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 76	of 102



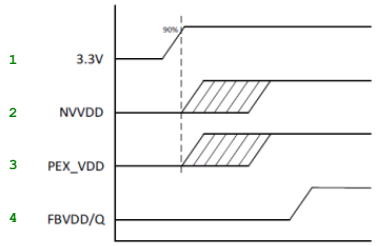
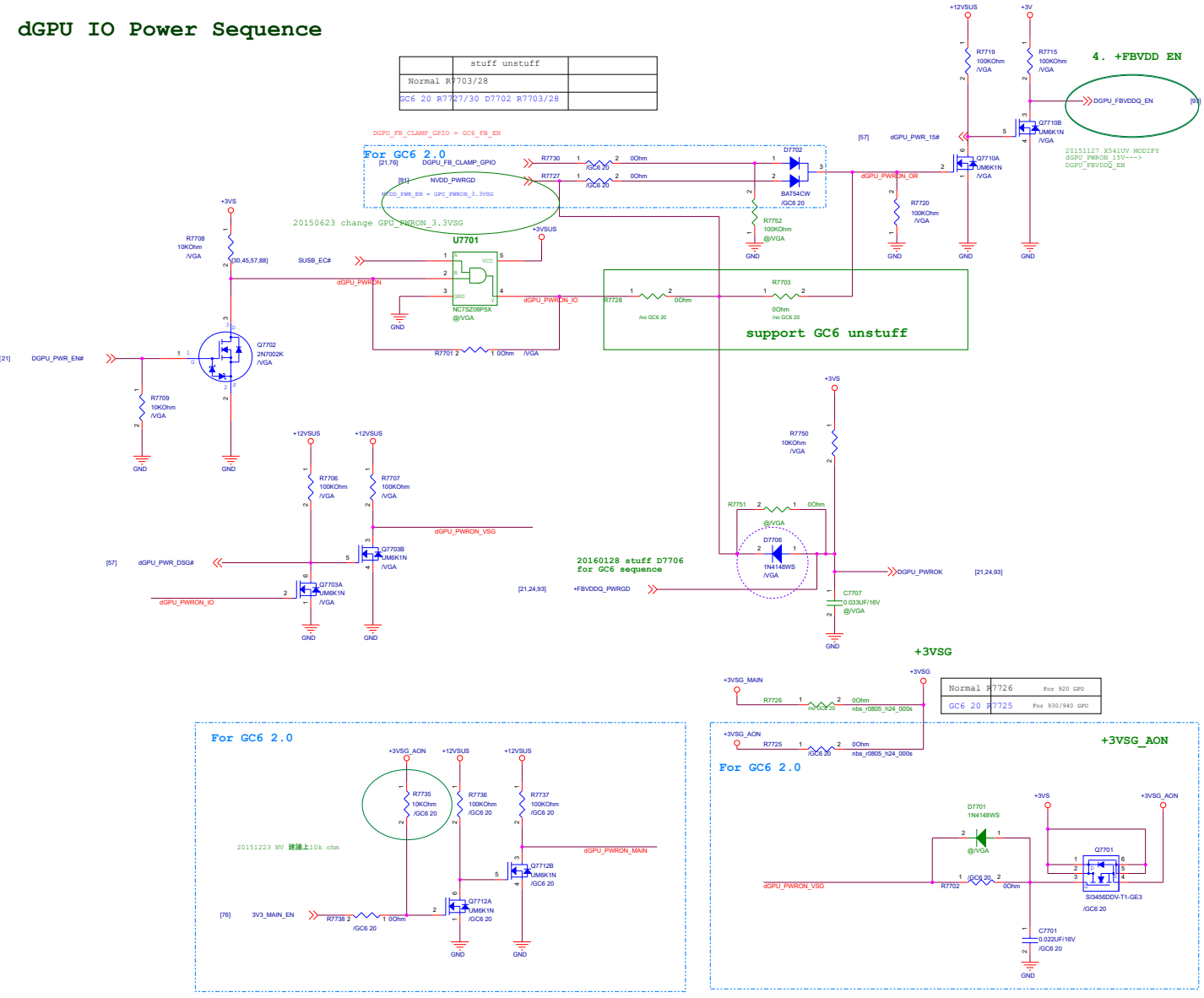
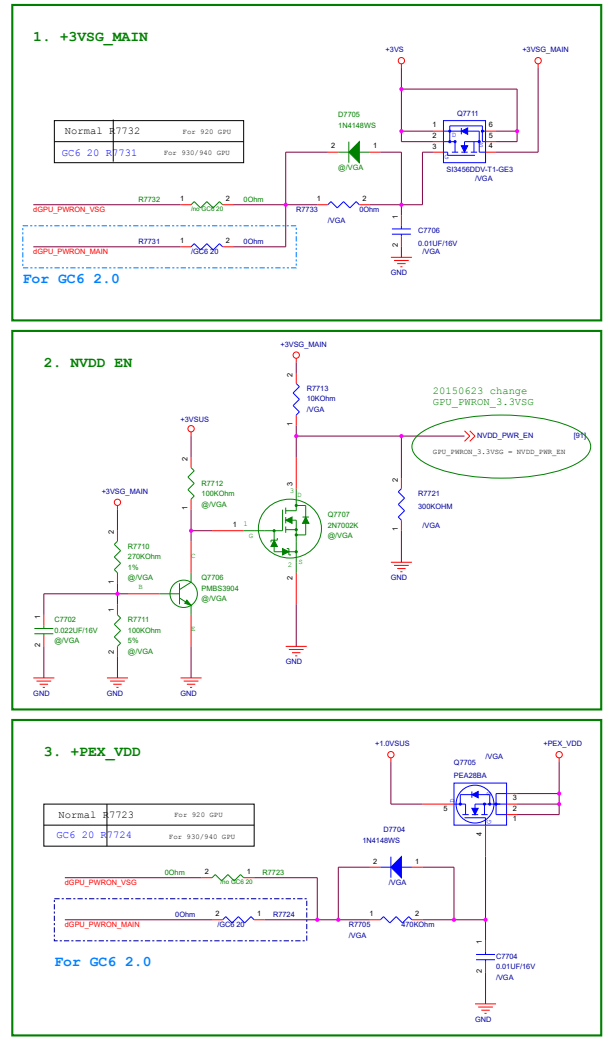


Figure 3-7. Example of Power-Up Sequencing Order

dGPU IO Power Sequence



dGPU Core Power Sequence



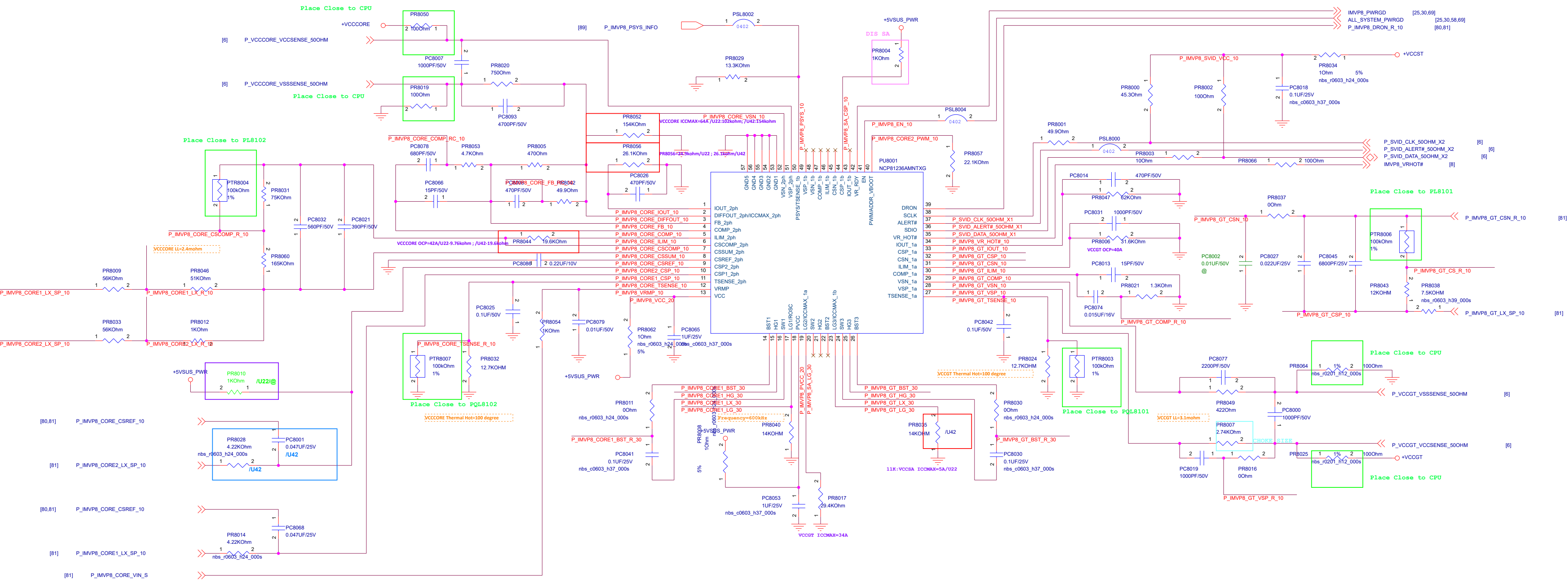
ASUS	Project Name: X507UA/UV	Rev: R1.0
Title :	N14M-GE_POWER	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 77 of 102	

KBLAKE IMVP8 (1) Power [For U22 CPU]

[81] P_IMVP8_GT_HG_30
[81] P_IMVP8_GT_LX_30
[81] P_IMVP8_GT_LG_30

[81] P_IMVP8_CORE1_HG_30
[81] P_IMVP8_CORE1_LX_30
[81] P_IMVP8_CORE1_LG_30

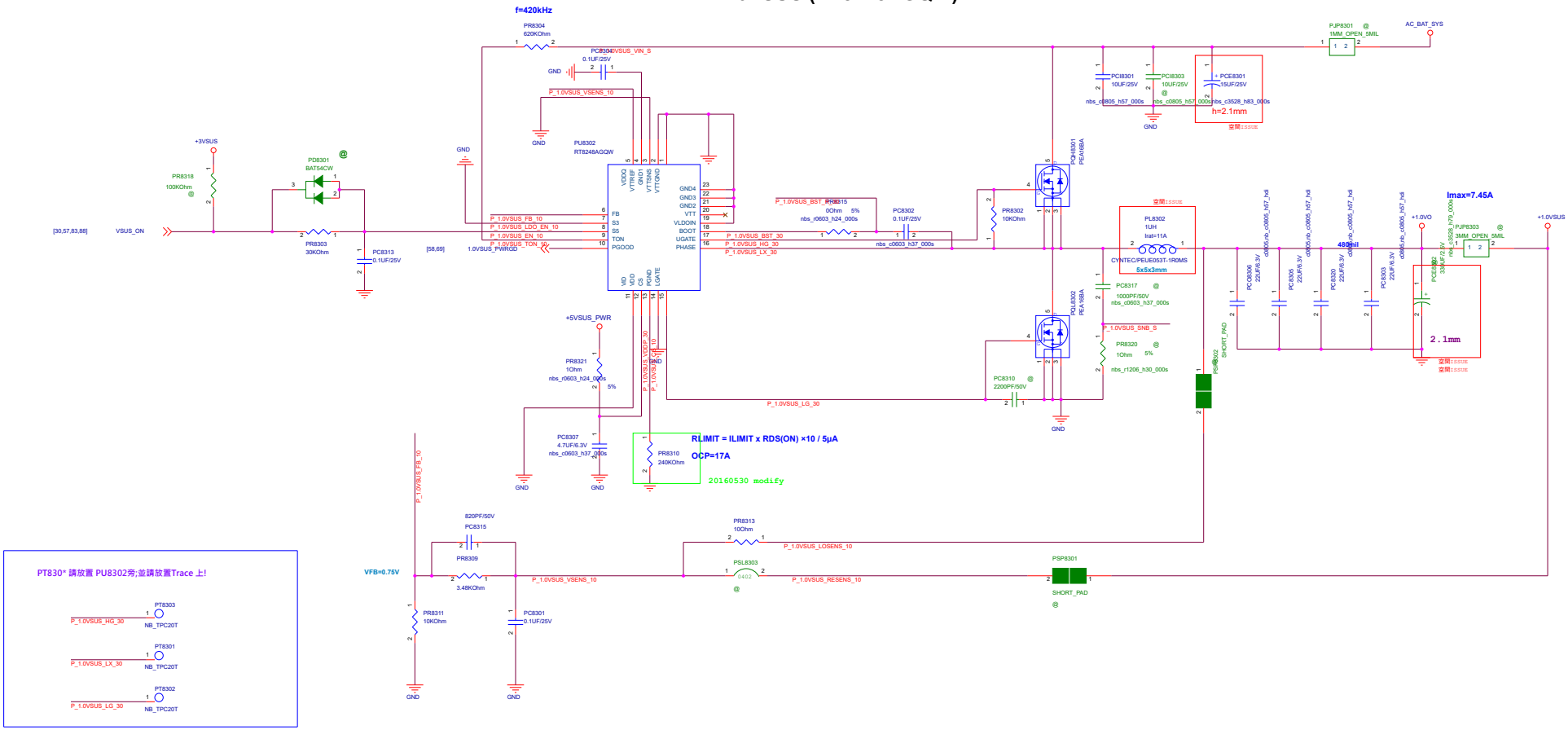
[81] P_IMVP8_CORE2_PWM_10
[80,81] P_IMVP8_DRON_R_10



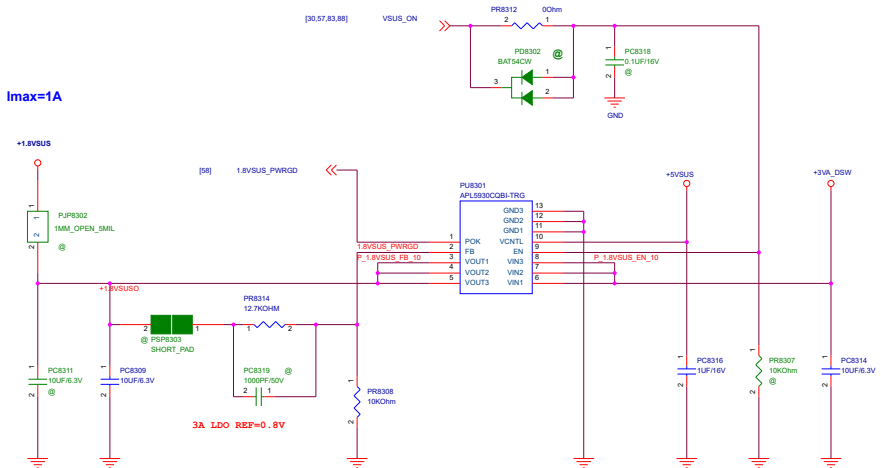
<Variant Name>

Project Name: X507UBR		Rev: R1.0
Title: PW_KBLAKE-U (1)		
Size: A2	Dept.: NB Power Team	Engineer: SS
Date: Friday, April 13, 2018	Sheet 80	of 102

+1.0VSUS (RT8248AGQW)



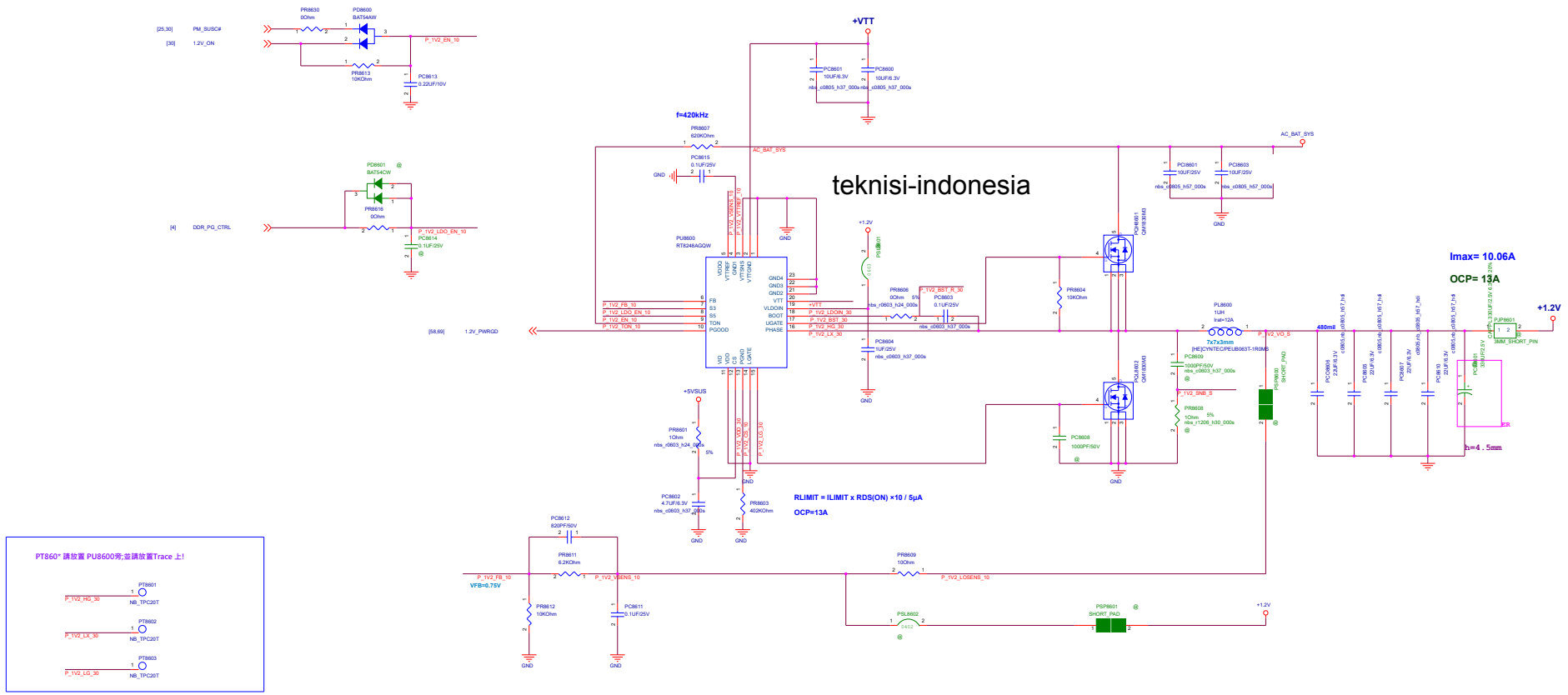
+1.8VSUS [For PCH]



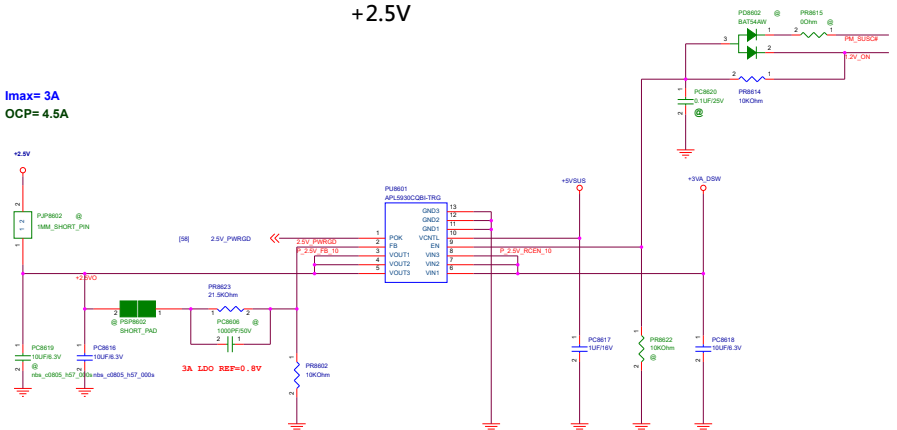
<Variant Name>

ASUS	Project Name: X507UBR	Rev: R1.0
Title : PW_+1.0VSUS / +1.8VSUS		
Size: C	Dept.: NB Power Team	Engineer: SS
Date: Friday, April 13, 2018	Sheet 83 of 102	

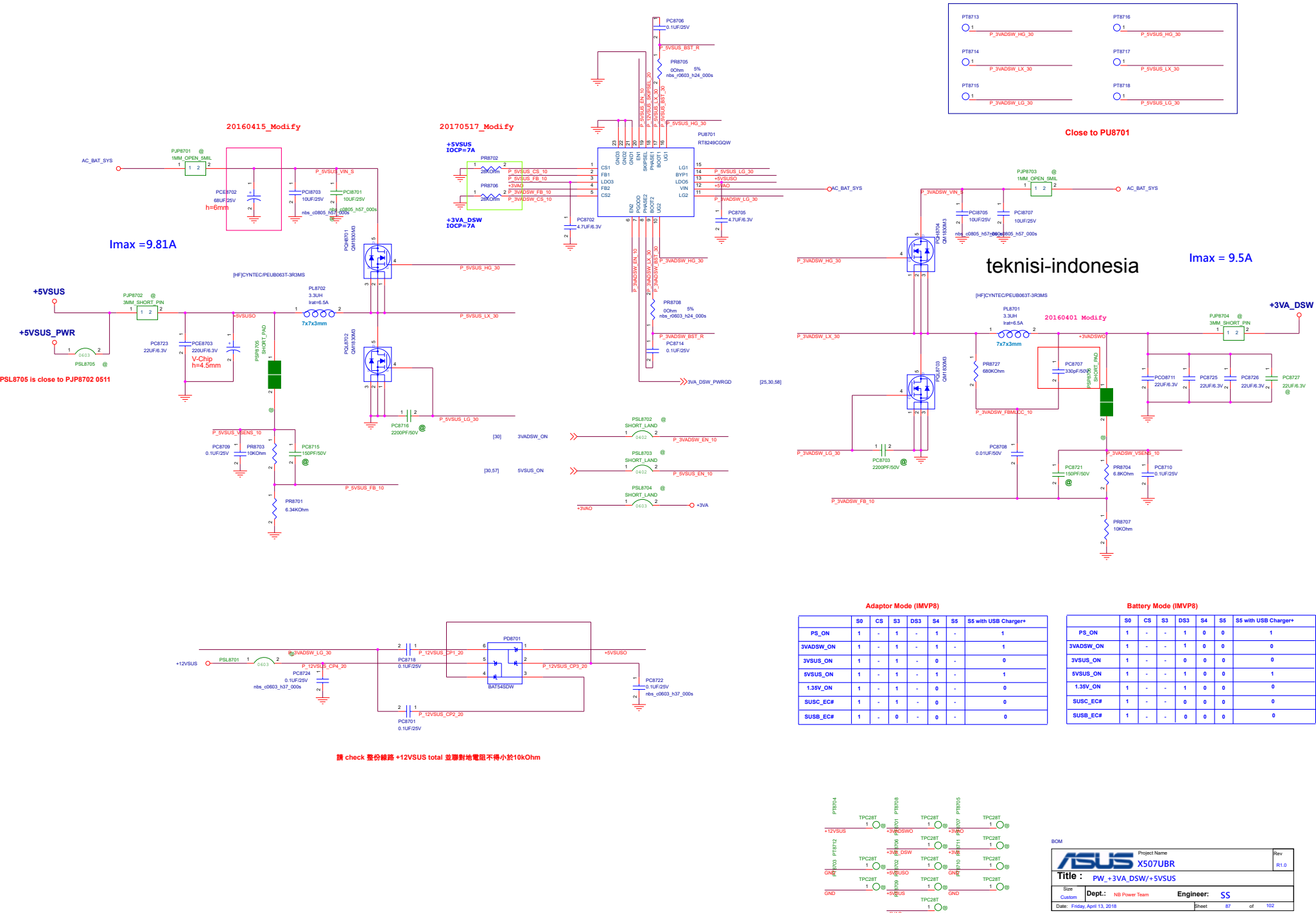
+1.2V / +VTT / +2.5V[For Memory]



+2.5V



+3VA_DSW / +5VSUS [System Power]



Adaptor Mode (IMVP8)

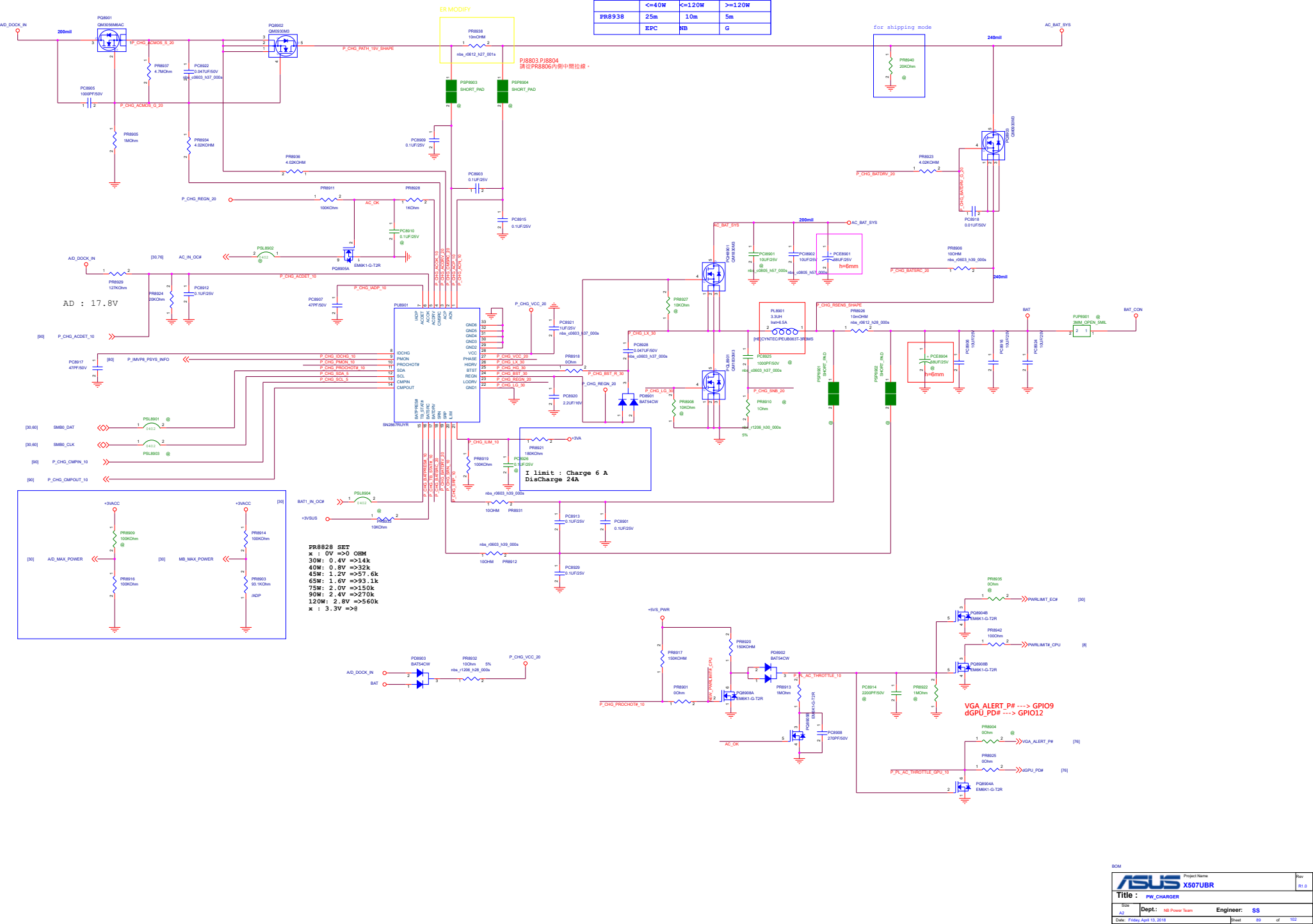
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

BOM

ASUS	Project Name: X507UBR	Rev: R1.0
Title :	PW_+3VA_DSW/+5VSUS	
Size: Custom	Dept.: NB Power Team	Engineer: SS
Date: Friday, April 13, 2018	Sheet 87 of 102	

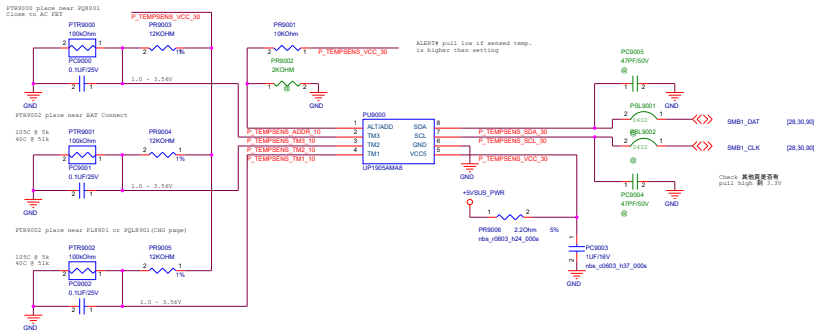

ER MODIFY
<=40W <=120W >=120W
PR8938 25m 10m 5m
EPC NB G
PJ8803,PJ8804
請從PR8806內側中間拉線。
for shipping mode
AC_BAT_SYS
A/D_DOCK_IN
200mil
240mil
PQ8901 QM3056M6AC
PQ8902 QM0930M3
PR8938 10mOHM
PSP8903 SHORT_PAD
PSP8904 SHORT_PAD
PR8940 20KOhm
PC8905 1000PF/50V
PR8905 1MOhm
PR8934 4.02KOHM
PR8936 4.02KOHM
PC8909 0.1UF/25V
PC8903 0.1UF/25V
PC8915 0.1UF/25V
PR8923 4.02KOHM
PQ8903 QM3930M3
PC8918 0.01UF/50V
PR8906 100HM
PR8911 100KOhm
PR8928 1KOhm
PC8910 0.1UF/25V
PSL8902
PQ8905A EM6K1-G-T2R
PC8901 10UF/25V
PC8902 10UF/25V
PC8903 + 68UF/25V h=6mm
PC8904 + 68UF/25V h=6mm
AD : 17.8V
PR8929 127KOhm
PR8924 20KOhm
PC8912 0.1UF/25V
PC8907 47PF/50V
PU8901
PC8917 47PF/50V
PSL8901
PSL8903
PC8921 1UF/25V
PR8918 0Ohm
PC8920 2.2UF/16V
PR8927 10KOhm
PL8901 3.3UH Isat=6.5A
PC8925 1000PF/50V
PR8926 10mOHM
PR8908 10KOhm
PR8910 1Ohm
PSP8901 SHORT_PAD
PSP8902 SHORT_PAD
PC8928 0.047UF/50V
PD8901 BAT54CW
PC8906 10U/F/25V
PC8916 10U/F/25V
PC8924 10U/F/25V
BAT
BAT_CON
PJP8901 3MM_OPEN_SMIL
PR8919 100KOhm
PC8926 0.1UF/25V
PR8921 180KOhm
PR8931 10OHM
PC8913 0.1UF/25V
PC8901 0.1UF/25V
PC8929 0.1UF/25V
PR8912 10OHM
PSL8904
PR8933 10KOhm
+3VSUS
+3VA
I limit : Charge 6 A
DisCharge 24A
PR8829 SET
x : 0V =>0 OHM
30W: 0.4V =>14k
40W: 0.8V =>32k
45W: 1.2V =>57.6k
65W: 1.6V =>93.1k
75W: 2.0V =>150k
90W: 2.4V =>270k
120W: 2.8V =>560k
x : 3.3V =>∞
+3VACC
PR8909 100KOhm
PR8916 100KOhm
PR8914 100KOhm
PR8903 93.1KOhm
A/D_MAX_POWER
MB_MAX_POWER
/ADP
+5VS_PWR
PR8917 150KOHM
PR8901 0Ohm
PR8920 150KOHM
PD8902 BAT54CW
PR8913 1MOhm
PQ8908A EM6K1-G-T2R
PQ8908B EM6K1-G-T2R
PC8908 270PF/50V
PC8914 2200PF/50V
PR8922 1MOhm
PR8935 0Ohm
PR8942 100Ohm
PR8904 0Ohm
PR8925 0Ohm
PQ8904A EM6K1-G-T2R
PWRLIMIT_EC#
PWRLIMIT#_CPU
VGA_ALERT_P#
dGPU_PD#
VGA_ALERT_P# ---> GPIO9
dGPU_PD# ---> GPIO12
PD8903 BAT54CW
PR8932 10Ohm 5%
BOM
ASUS
Project Name X507UBR
Rev R1.0
Title : PW_CHARGER
Size A2
Dept.: NB Power Team
Engineer: SS
Date: Friday, April 13, 2018
Sheet 89 of 102

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

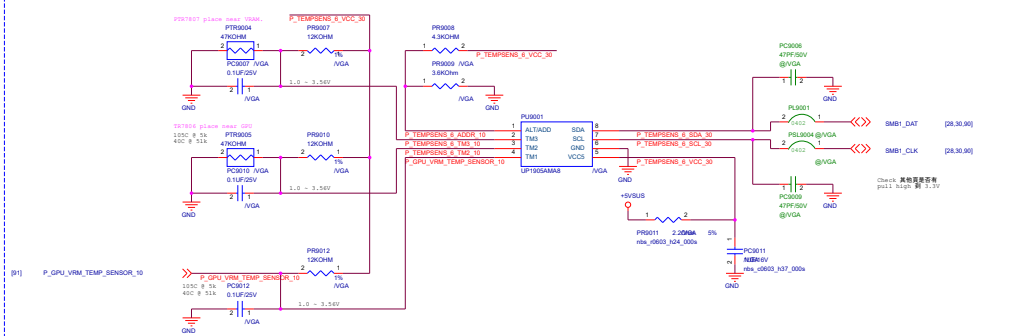
Register Address

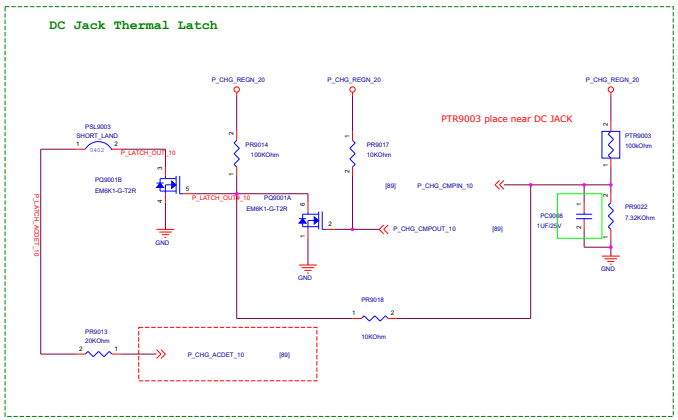
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9008	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9009	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k



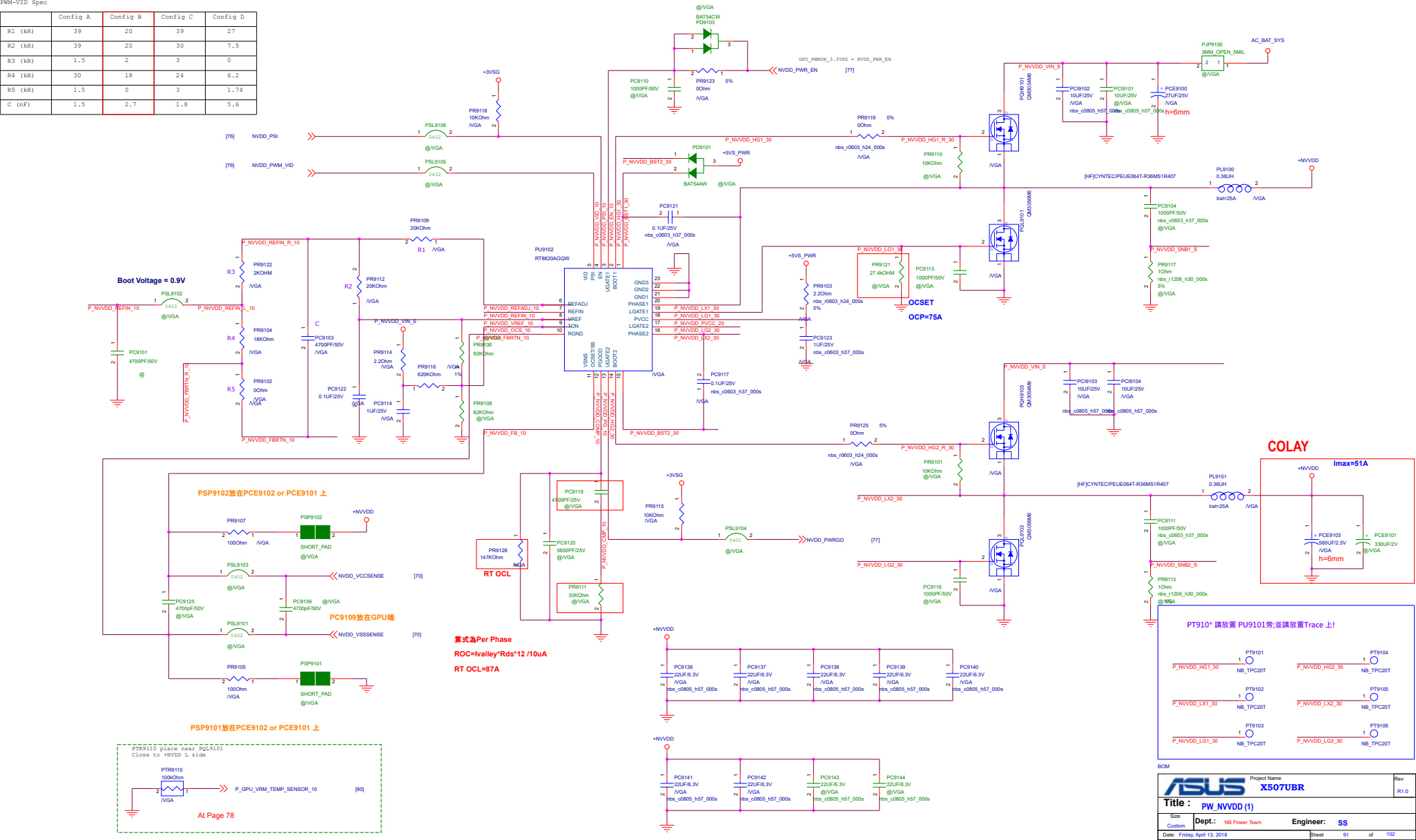


<variant_name>

ASUS	Project Name: X507UBR	Rev: R1.0
Title : PW_PROTECTION		
Size: A2	Dept.: NB Power Team	Engineer: SS
Date: Friday, April 13, 2018	Sheet 90 of 102	

PWM-VID Spec

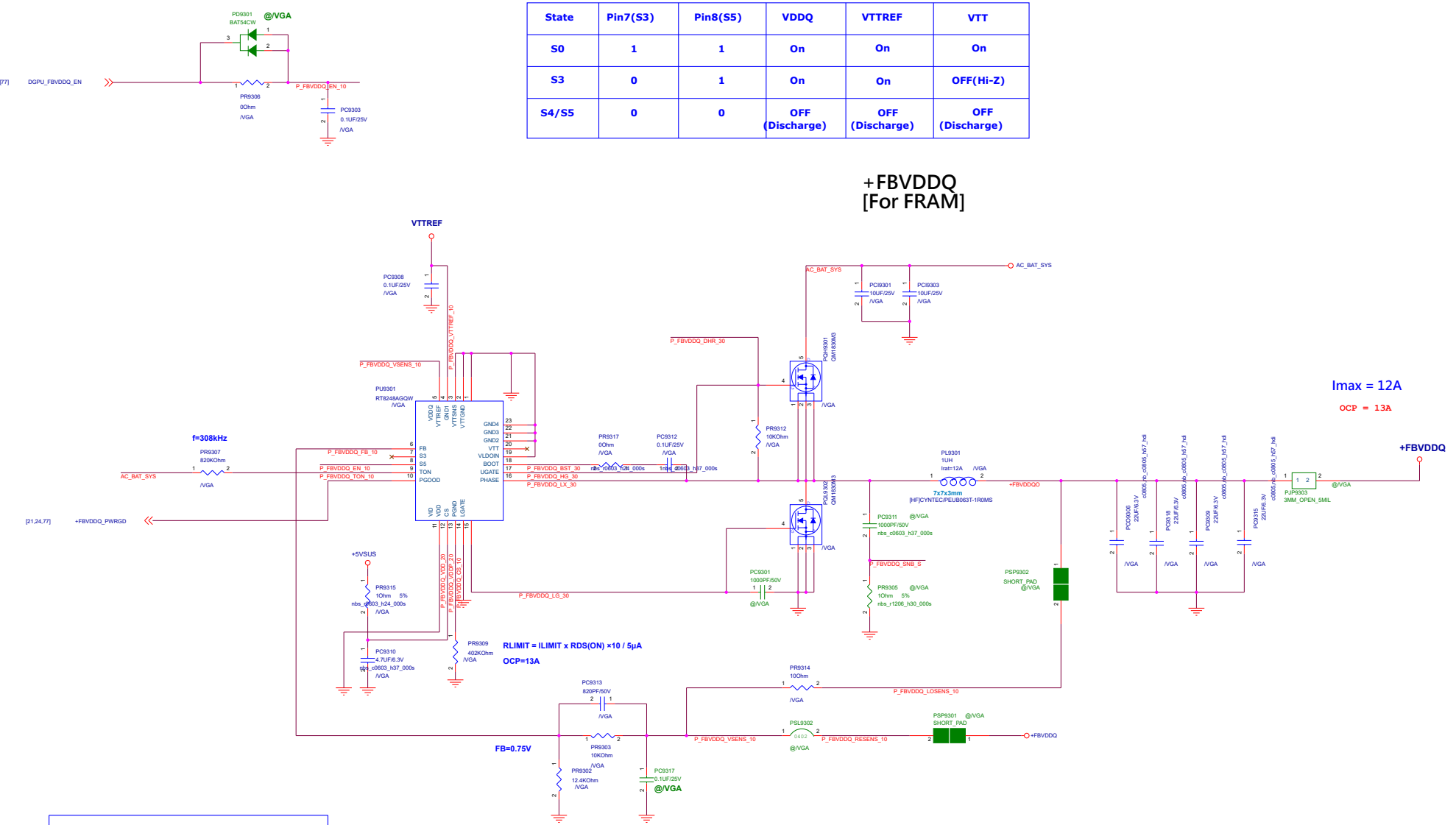
	Config A	Config B	Config C	Config D
R1 (kR)	39	20	39	27
R2 (kR)	39	20	30	7.5
R3 (kR)	1.5	2	3	0
R4 (kR)	30	18	24	6.2
R5 (kR)	1.5	0	3	1.74
C (nF)	1.5	2.7	1.8	5.6



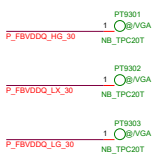
S3 And S5 Truth Table

State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+FBVDDQ [For FRAM]

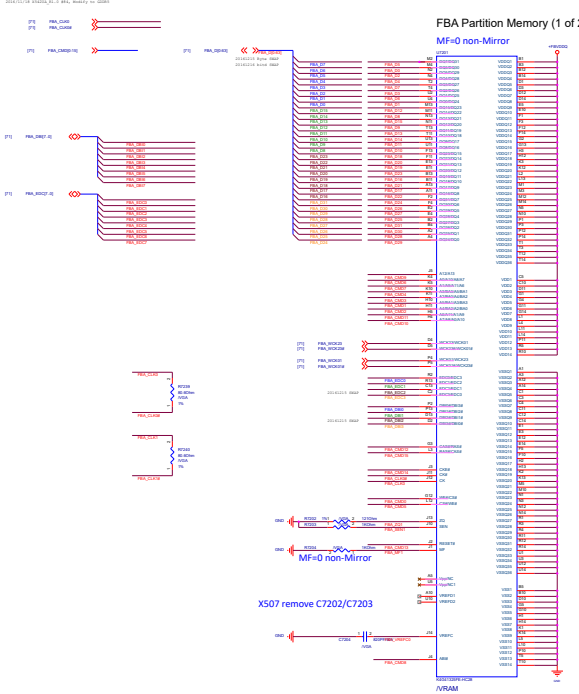


PT930* 請放置 PU9301旁;並請放置Trace 上!



<Variant Name>

ASUS	Project Name: X507UBR	Rev: R1.0
Title : PW_+FBVDDQ		
Size: Custom	Dept.: NB Power Team	Engineer: SS
Date: Friday, April 13, 2018	Sheet 93 of 102	

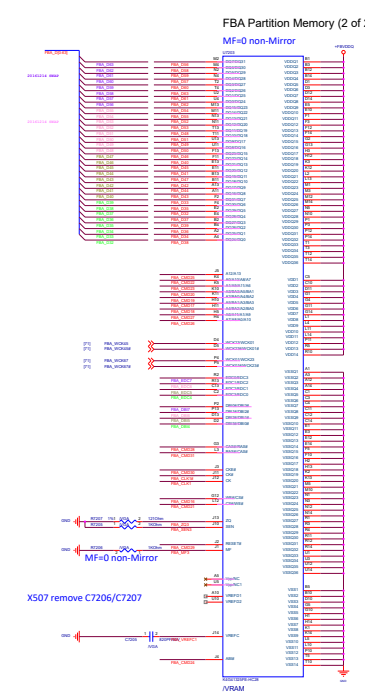


GDDR5 X32

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.



7.1.12.1 VREF-D

VREF-D pins can be left floating.

7.1.12.2 VREF-C

VREF-C connections for the ×16 mode are shown in Figure 7-8.

Table 7-14. VREF Configuration

Configuration	Requirement	Notes
×32	Share one Vref-C circuit for two memory parts.	GDDR5 DRAMs have internal VREF for DQ, EDC (VREF-D).
×16	Share one VREF-C circuit for four memory parts.	Command, Address VREF (VREF-C) needs to be externally supplied since DRAMs do NOT internally generate VREF for these signals.

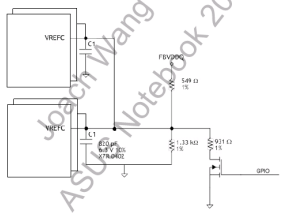
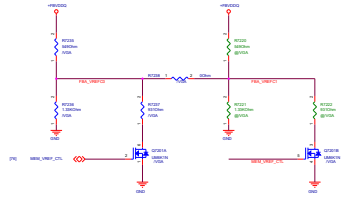
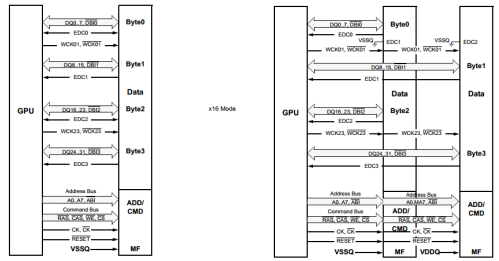
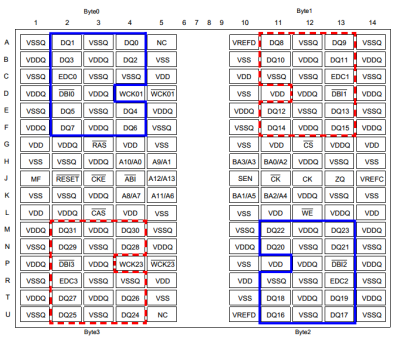


Figure 7-8. VREF-C Connections for ×16 Mode

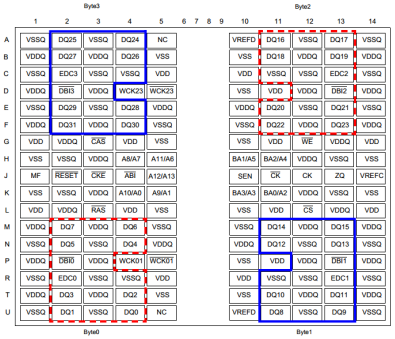




5.1 GDDR5 SGRAM 170ball BGA Ball-out MF=0



5.2 GDDR5 SGRAM 170ball BGA Ball-out MF=1



Signal Assignment in MF=0 and MF=1

Mirror Function Signal Mapping Columns 1 to 5

PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1
A1	VSSQ		A2	DQ1	DQ25	A3	VSSQ		A4	DQ0	DQ24	A5	NC	
B1	VDDQ		B2	DQ3	DQ27	B3	VDDQ		B4	DQ2	DQ26	B5	VSS	
C1	VSSQ		C2	EDC0	EDC3	C3	VSSQ		C4	VSSQ		C5	VDD	
D1	VDDQ		D2	DBI0	DBI3	D3	VDDQ		D4	WCK01	WCK23	D5	WCK01	WCK23
E1	VSSQ		E2	DQ5	DQ29	E3	VSSQ		E4	DQ4	DQ28	E5	VDDQ	
F1	VDDQ		F2	DQ7	DQ31	F3	VDDQ		F4	DQ6	DQ30	F5	VSSQ	
G1	VDD		G2	VDDQ		G3	RAS	CAS	G4	VDD		G5	VSS	
H1	VSS		H2	VSSQ		H3	VDDQ		H4	A10/A0	A8/A7	H5	A8/A7	A11/A6
J1	MF		J2	RESET		J3	CKE		J4	ABI		J5	A12/A13	
K1	VSS		K2	VSSQ		K3	VDDQ		K4	A8/A7	A10/A0	K5	A11/A6	A9/A1
L1	VDD		L2	VDDQ		L3	CAS	RAS	L4	VDD		L5	VSS	
M1	VDDQ		M2	DQ31	DQ7	M3	VDDQ		M4	DQ30	DQ6	M5	VSSQ	
N1	VSSQ		N2	DQ29	DQ5	N3	VSSQ		N4	DQ28	DQ4	N5	VDDQ	
P1	VDDQ		P2	DBI3	DBI0	P3	VDDQ		P4	WCK23	WCK01	P5	WCK23	WCK01
R1	VSSQ		R2	EDC3	EDC0	R3	VSSQ		R4	VSSQ		R5	VDD	
T1	VDDQ		T2	DQ27	DQ3	T3	VDDQ		T4	DQ26	DQ2	T5	VSS	
U1	VSSQ		U2	DQ25	DQ1	U3	VSSQ		U4	DQ24	DQ0	U5	NC	

Mirror Function Signal Mapping Columns 10 to 14

PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1
A10	VREFD		A11	DQ8	DQ16	A12	VSSQ		A13	DQ9	DQ17	A14	VSSQ	
B10	VSS		B11	DQ10	DQ18	B12	VDDQ		B13	DQ11	DQ19	B14	VDDQ	
C10	VDD		C11	VSSQ		C12	VSSQ		C13	EDC1	EDC2	C14	VSSQ	
D10	VSS		D11	VDD		D12	VDDQ		D13	DBI1	DBI2	D14	VDDQ	
E10	VDDQ		E11	DQ12	DQ20	E12	VSSQ		E13	DQ13	DQ21	E14	VSSQ	
F10	VSSQ		F11	DQ14	DQ22	F12	VDDQ		F13	DQ15	DQ23	F14	VDDQ	
G10	VSS		G11	VDD		G12	CS	WE	G13	VDDQ		G14	VDD	
H10	BA3/A3	BA1/A5	H11	BA0/A2	BA2/A4	H12	VDDQ		H13	VSSQ		H14	VSS	
J10	SEN		J11	CK		J12	CK		J13	ZQ		J14	VREFC	
K10	BA1/A5	BA3/A3	K11	BA2/A4	BA0/A2	K12	VDDQ		K13	VSSQ		K14	VSS	
L10	VSS		L11	VDD		L12	WE	CS	L13	VDDQ		L14	VDD	
M10	VSSQ		M11	DQ22	DQ14	M12	VDDQ		M13	DQ23	DQ15	M14	VDDQ	
N10	VDDQ		N11	DQ20	DQ12	N12	VSSQ		N13	DQ21	DQ13	N14	VSSQ	
P10	VSS		P11	VDD		P12	VDDQ		P13	DBI2	DBI1	P14	VDDQ	
R10	VDD		R11	VSSQ		R12	VSSQ		R13	EDC2	EDC1	R14	VSSQ	
T10	VSS		T11	DQ16	DQ10	T12	VDDQ		T13	DQ19	DQ11	T14	VDDQ	
U10	VREFD		U11	DQ16	DQ8	U12	VSSQ		U13	DQ17	DQ9	U14	VSSQ	

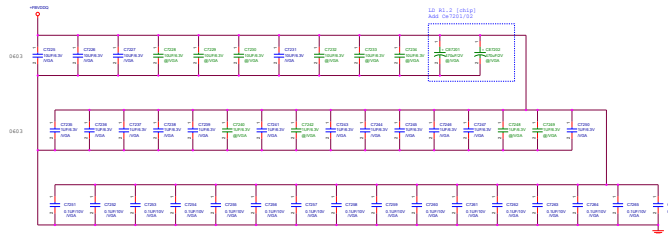


Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

GPU (for X507UV)	920MX(N16V-GMR1)	02004-00430400	C.S N16V-GMR1-S-A2 FCBGA595	NVIDIA GB2B-64 GM108-626-A2	STRAP	R7516	R7519
VRAM	256*32*2pcs	03008-00050000	GDDR5 256*32 5.0 1.35V FBGA170	SAMSUNG/K4G80325FB-HC28	0X0	NC	4.99K
		03008-00050400	GDDR5 256M*32 6.0 1.5V FBGA170	MICRON/MT51J256M32HF-70:A	0X1	NC	10K

15.5.13 SORx_EXPOSED Straps

SORx_EXPOSED is used to define audio capability on each digital display link.

Display links with audio capability should have the corresponding SORx_EXPOSED bit set to one. These include links used for HDMI, DisplayPort, and DVI ports that can be used with a DVI-to-HDMI dongle or routed to the HDMI or DisplayPort connector on a docking station.

Display links with no audio capability should have the corresponding SORx_EXPOSED bit set to 0. These include LVDS, eDP, or unused links.

Table 15-15 shows the correlation between display configurations and the SORx_EXPOSED strap settings.

Table 15-15. SORx_EXPOSED - Display Link to Usage Bit Mapping

Displays		HDMI/DP	DVI	LVDS	eDP	Not in Use
Standard Mode	IFPAB		SOR0_EXP = 1	SOR0_EXP = 0		SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPET	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
Split Mode AB	IFPA	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	IFPB	SOR0_EXP = 1	SOR0_EXP = 1			SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPET					
Split Mode EF	IFPAB					
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPE	SOR3_EXP = 1	SOR3_EXP = 1		SOR3_EXP = 0	SOR3_EXP = 0
	IFPF	SOR0_EXP = 1	SOR0_EXP = 1		SOR0_EXP = 0	SOR0_EXP = 0

15.5.14 DEVID_SEL Strap

This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVID straps. This strap only exists in the GB2B-64, GB4B-128, and GB3B-256 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* document for the latest configuration.

15.5.15 PCIE_CFG Strap

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing 3G3O_PADCFG. This strap only exists in the GB2B-64, GB4B-128, and GB3B-256 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* document for the latest configuration.

15.5.6 SMB_ALT_ADDR Strap

This strap is used to configure the address of the I²C slave device on the GPU's PCS interface.

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

15.5.5 VGA_DEVICE Strap

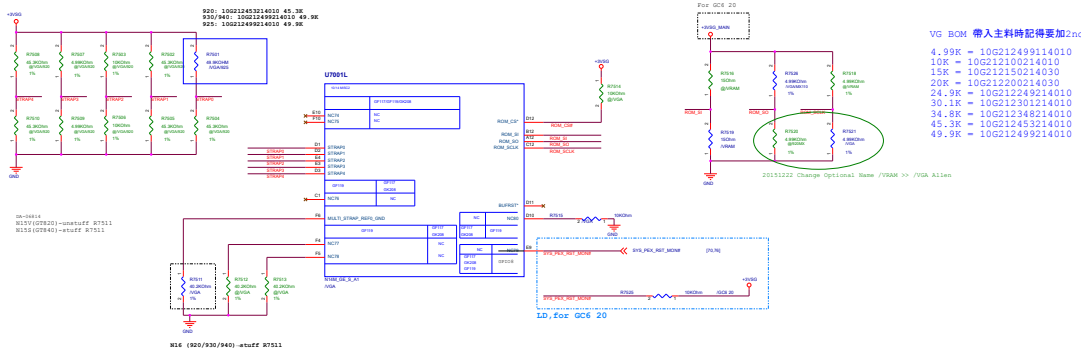
The VGA_DEVICE strap is used to identify the device type (or class code) of the GPU within the PCI configuration space. Set 3D Acceleration Device for GPU in Optimus configuration or secondary GPU in SLI configuration.

Table 15-7. VGA_DEVICE Settings

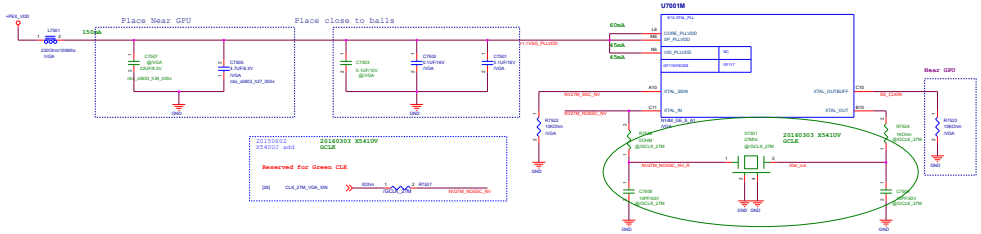
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device (Class Code 0302h)
1	Primary Display or VGA Device (Class Code 0300h)

Table 15-1. Device Specific Strap Mode Selection

	All N16x GPUs
MultiStrap_RefG_GND	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff N/GN 1% to GND



Xtal



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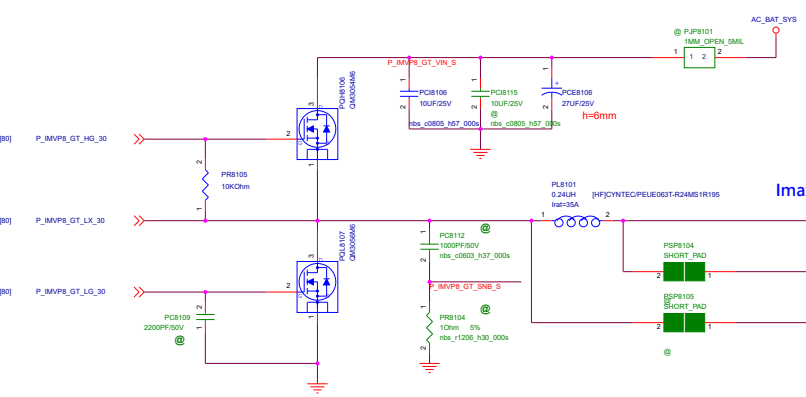
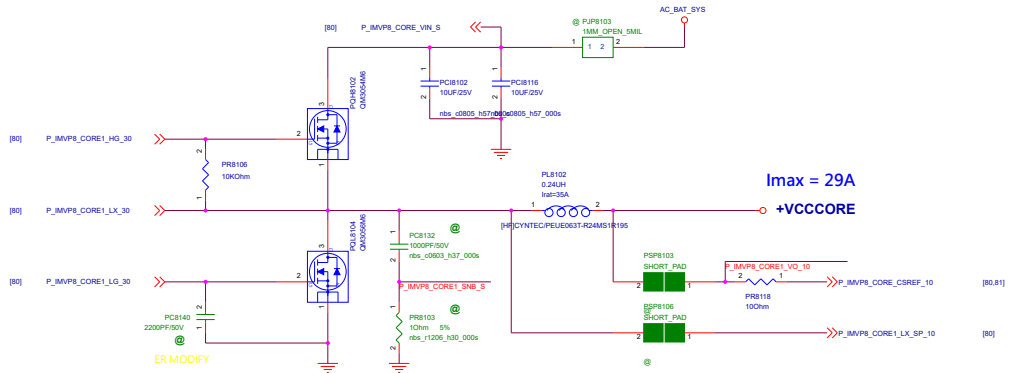
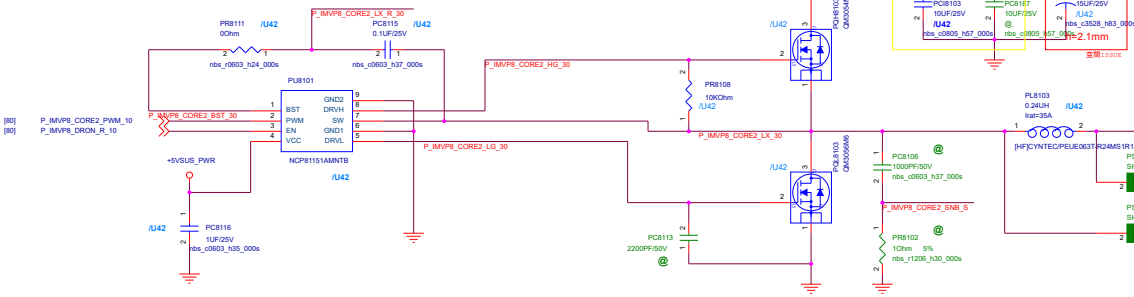
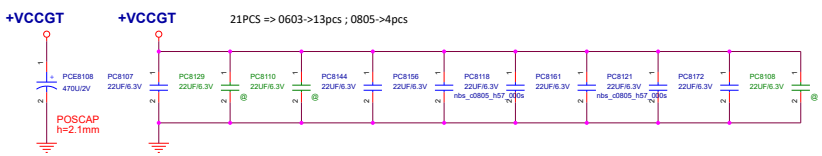
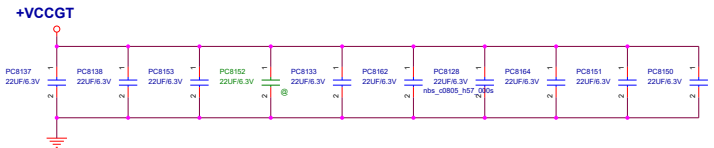
Skylake IMVP8 Power (2) [For CPU]

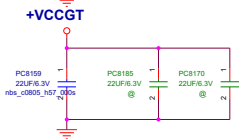


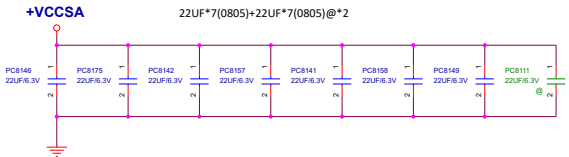


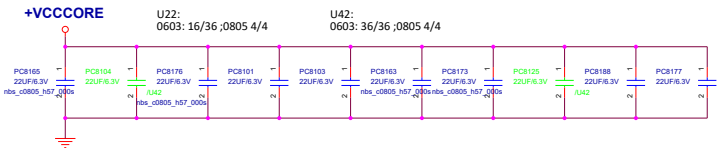


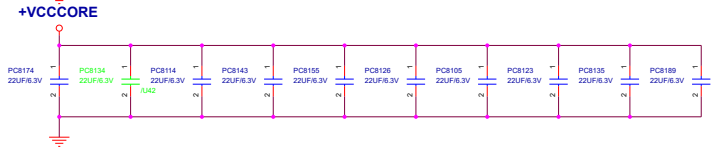


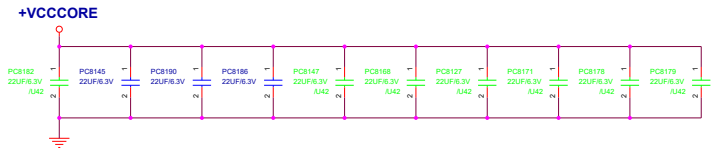


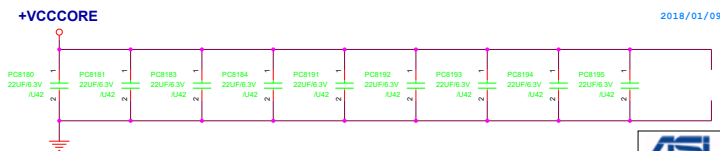


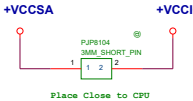












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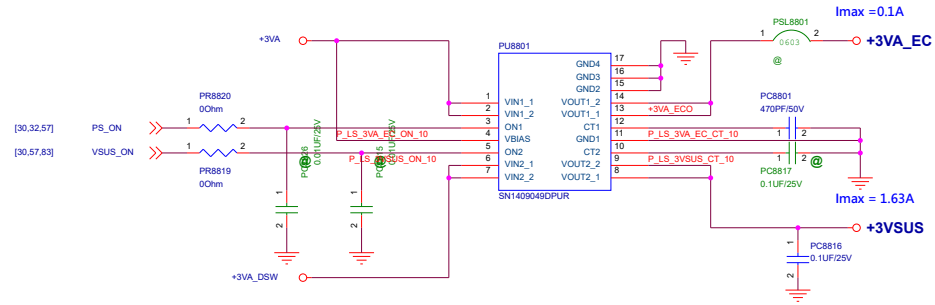
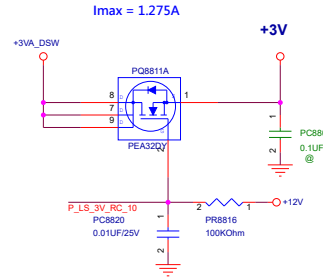
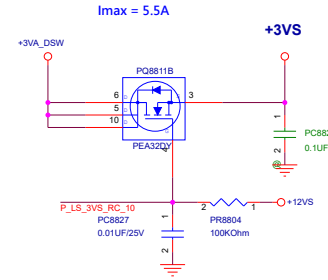
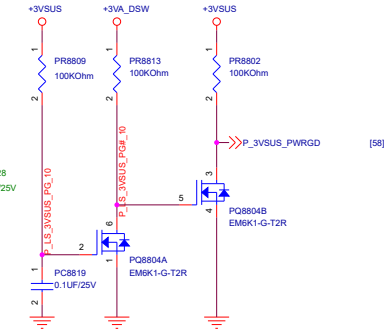
Load Switch

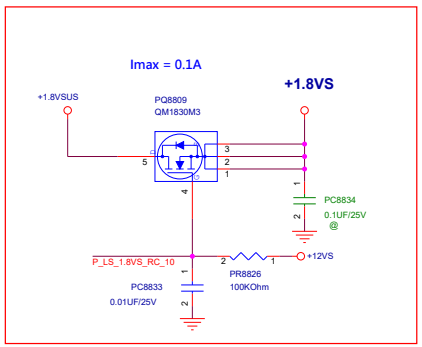


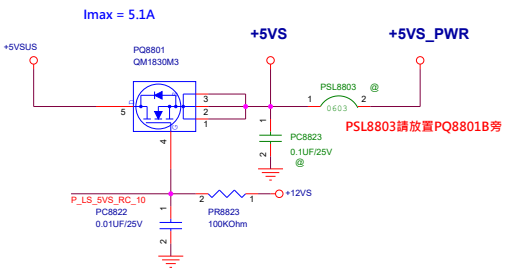


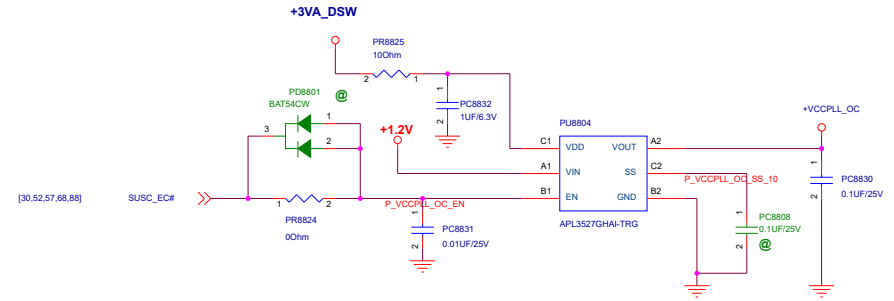


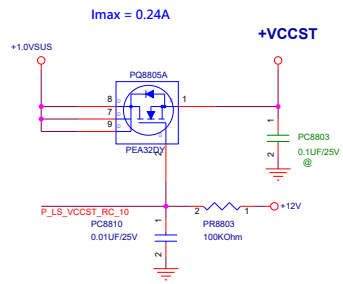


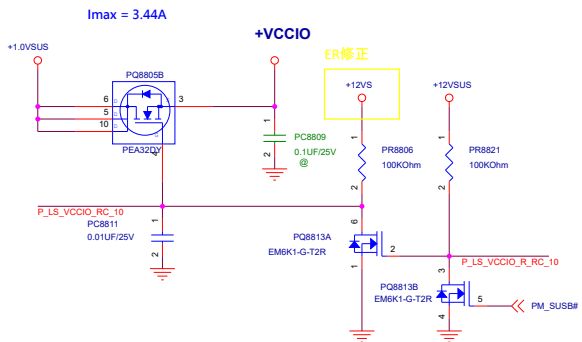
20151204 Modify

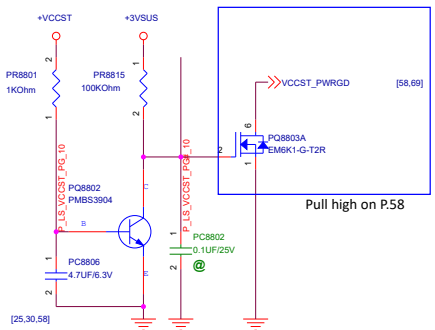


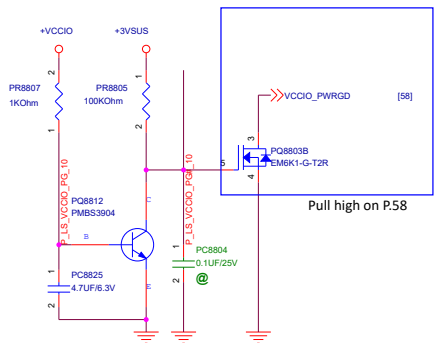


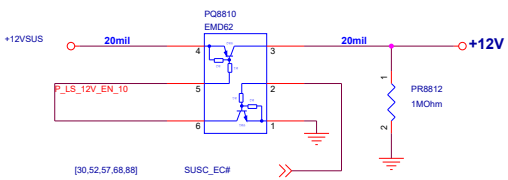


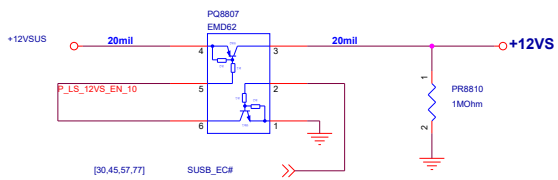












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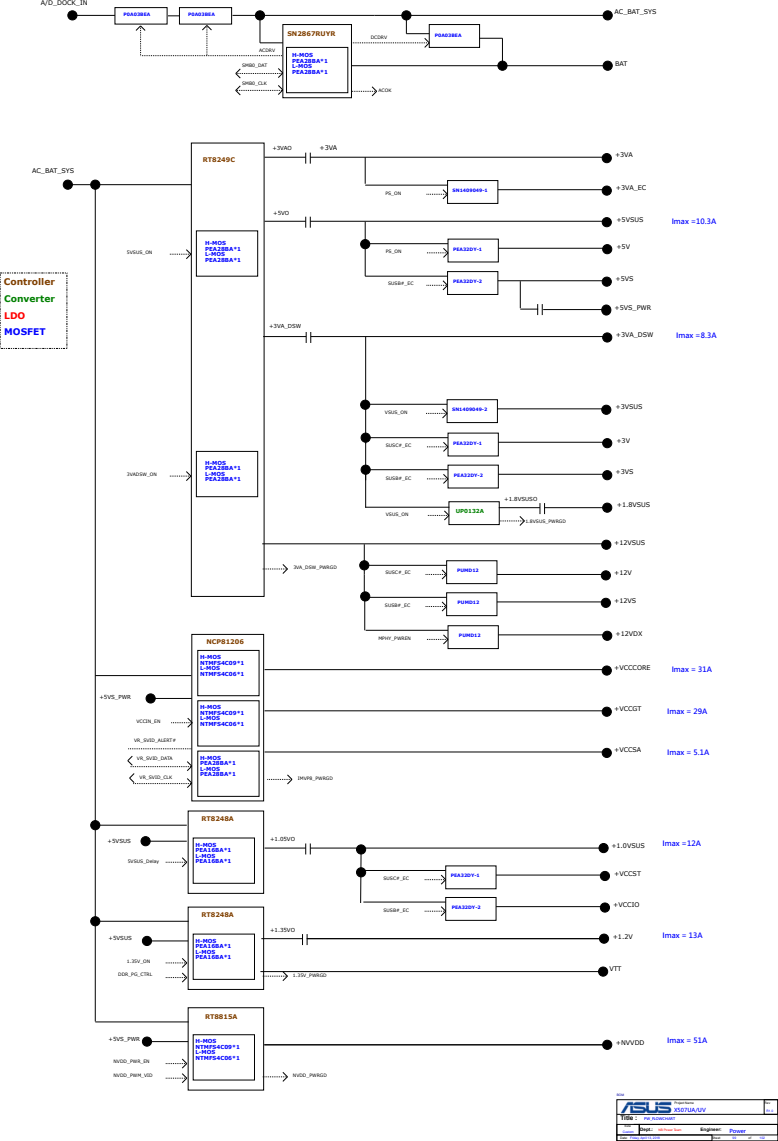
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L-MOS
PEA28BA*1
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ACOK
AC_BAT_SYS
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+3VA
+3VA
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+5VO
+5VSUS
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L-MOS
PEA28BA*1
SUSUS_ON
PS_ON
PEA320Y-1
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SUS8#_EC
PEA320Y-2
+5VS
+5VS_PWR
+3VA_DSW
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PEA320Y-2
+3VS
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PEA28BA*1
L-MOS
PEA28BA*1
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+1.8VSUSO
VSUS_ON
UP0132A
+1.8VSUS
1.8VSUS_PWRGD
+12VSUS
3VA_DSW_PWRGD
SUSC#_EC
PUMD12
+12V
SUS8#_EC
PUMD12
+12VS
MPHY_PWREN
PUMD13
+12VDX
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L-MOS
NTMFS4C06*1
+VCCCORE
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+5VS_PWR
N-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
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+VCCGT
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L-MOS
PEA28BA*1
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+5VSUS
+1.05VO
+1.0VSUS
Imax =12A
N-MOS
PEA18BA*1
L-MOS
PEA18BA*1
SVSUS_Delay
SUSC#_EC
PEA320Y-1
+VCCST
SUS8#_EC
PEA320Y-2
+VCCIO
RT8248A
+5VSUS
+1.35VO
+1.2v
Imax = 13A
N-MOS
PEA18BA*1
L-MOS
PEA18BA*1
1.35V_ON
VTT
DDR_PG_CTRL
1.35V_PWRGD
RT8815A
+5VS_PWR
+NVVDD
Imax = 51A
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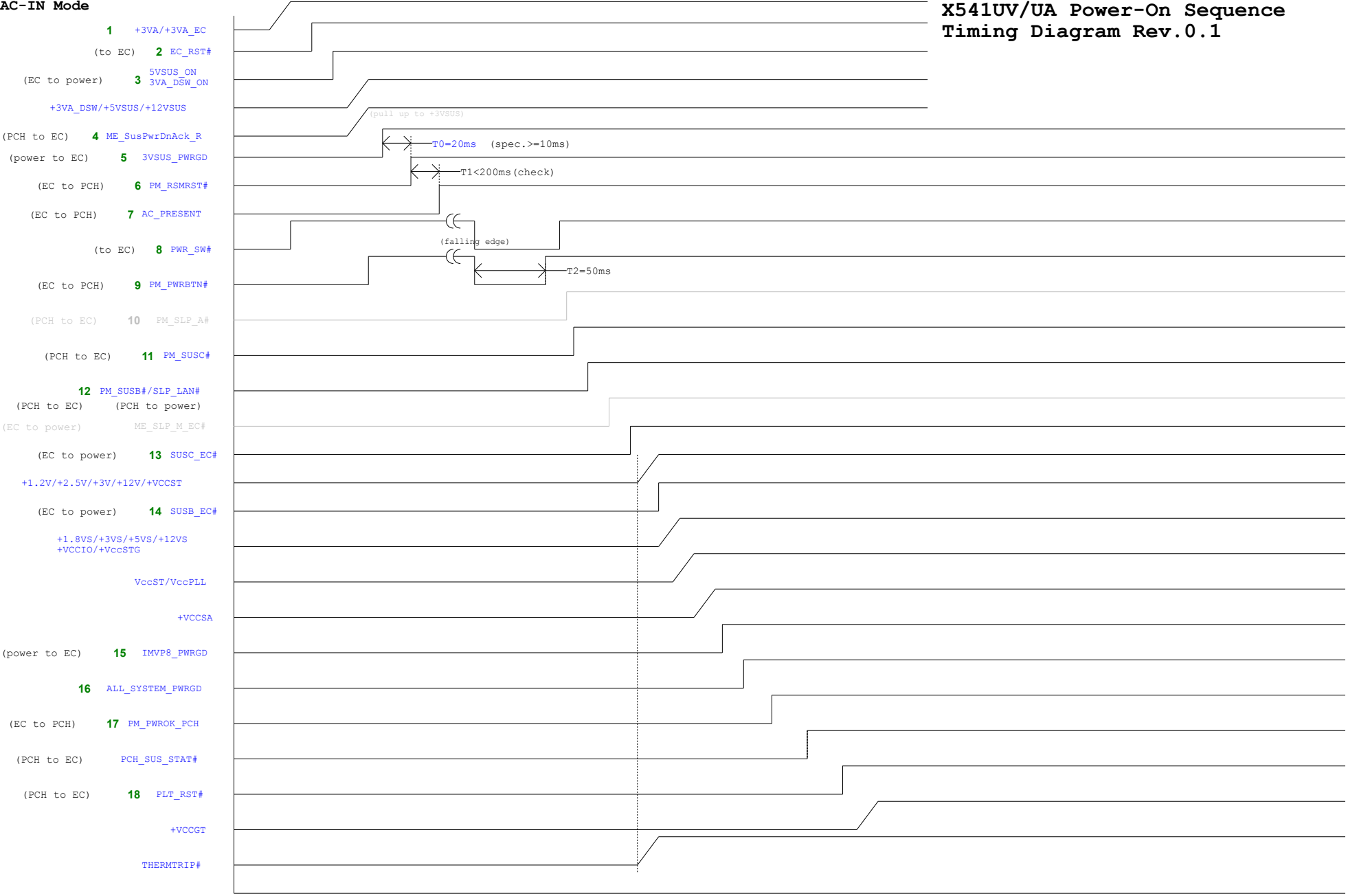
NTMFS4C09*1
L-MOS
NTMFS4C06*1
NVDD_PWR_EN
NVDD_PWM_VID
NVDD_PWRGD
Controller
Converter
LDO
MOSFET

X541UV/UA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode



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ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : Power On Timing		
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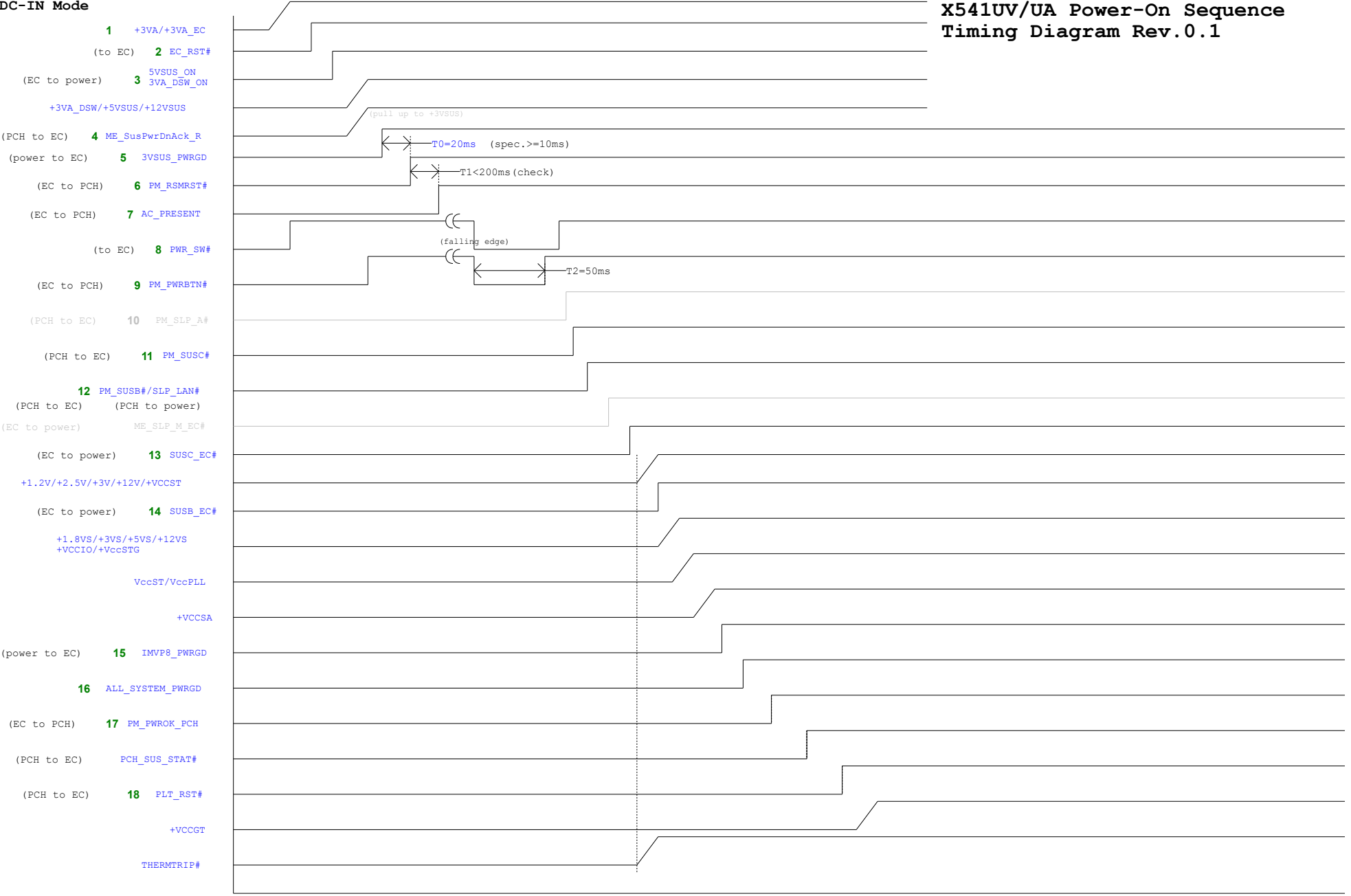
X541UV/UA Power-On Sequence Timing Diagram Rev.0.1



BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : Power On Timing		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 101 of 102	

Rev	Date	Description
R1.0	2016/05/26	1. Remove Q5706 2. 改U3101 R/B CON8 footprint 3. R7505數值10ok改為10k 4. Remove R7121, R7122改為4.7k
	2016/05/30	1. updated power 線路 2. Del R3833 & Add D3801 3. P.38 ADD DVDD IO~~~VAID_DVDD 4. 更換P.55 Type-C Short Pin
	2016/06/03	1. updated power 線路 (p.88) 2. R7505 改回10ok (for +1.8vag power up smooth) 3. R2301 R2302 R2303 上件
	2016/06/08	1. updated power 線路 (p.87) 2. updated power 線路 (p.80) - change option
R2.0	2016/07/01	1. J4501 LED換footprint 2. C2901 換 12 pF 3. C2505 for power sequence 4. Updated page 68, page 24 remove net
	2016/07/12	1. Change page 68 pin defined
	2016/07/13	1. Change 7/12 EMI 更動
	2016/07/21	1. updated power 線路 (p.84, p.88) 2. GPU PCIE change for Gen 2 3. Remove R7114 , R7505 change 10k 4. R3204 換 1M, R3207上件
	2016/09/29	1. change CAP voltage rating (p.37)
X540UPR R1.0	2017/03/28	• 更新Block Diagram (page 1) • 新增U42 / U22 ODLDO power plane(+VCCCORE/+VCCGT)切換線路 (page 6) • 新增 24M XTAL 預留線路 for U42 (page 9) • SCLK generation 改料 (page 29) • PCH 24M clock 改由 SCLK輸入 (page 9, 29) • power更新線路for U42 (page 78, 80, 81, 91) • ESD pool 線路與料更換 (page 55)
	2017/03/29	• 更新SVID / VCCCORE / VCCGT / VCCSA sense pin name (page6)
	2017/03/30	• power移除+VCCSA線路, 將+VCCSA 改為 +VCCIO_CPU (page 6, 80, 81)
	2017/03/31	• merge 2 USB port to 1ESD component (page 52)
	2017/04/05	• 新增wake on WAN預留線路 (page 30, 53)
	2017/04/07	• P_SVID_DATA_X2(Page 6) 改為P_SVID_DATA_50OHM_X2
	2017/04/11	• C1067 改為上件 C1065 改為不上件 (Page 10)
X506MA X506UA R1.0	2017/05/08	• Remove ODD (moidify IO) (Page 68) • Remove Carder Reader /direct connect from PCH (Page 42) • ADD M.2 SSD Schematic refer UX310UV (Page 51) • Modify Wlan connector / Schematic refer UX310UV (Page 53)
	2017/05/09	• Modify R2430,R3079,R2635,R2810 from 0 Ohm to Shortland for cost • Reduce Wake on WLAN Solution (Page 53) • Modify DDR to 2SO DIMM refer X542UQ_PR_0327
	2017/05/10	• Follow X542UA_R1.0 #79, Remove PM_EXTTS#0 & R3091 (page 30) • Remove D3602 (Page 36) • All Discharge BOM to 0 (Page 57) • Audio A/D GND left one 0 ohm at SR (Page 36)
	2017/05/11	• remove C3605/C0603/C3606/3602 these cap already had near Pin side (Page 36) • Change R4515/R4516 to shortland(SL4507/SL4508) (Pahe45) • Change R3619 to short land SL3607 (Page 36) • Modify R5309 to Shortland SL5309 (Page 53) • BT/WLAN ON OFF Follow X452UQ PR (Pae 53) • For SDCX; SD_RCOMP need PD 200Ohm(Page22)
	2017/05/12	• ADD Cardreader power solution, and FU/PD resistor move to PCH side • Del R2303 for better placement /Change R2307 to 0 for No Port B at X506UA • DDR_PG_CTRL FU change to +3VS /Del R2408 refer UX310 X452UQ (Page 4) • Modify R4803/R4804/R4805/R4806 to 0 R04801/R04802 to 0ohm (Page 48) • Change RN2401/RN2402 to R2435-R2440 No use CLK REQ be 0 (Page 24) • Change RN2502 to R2560/R2561(Page 25) for Cost • remove R2505 ,power sequence will be check in X506 SR (page 25) • ADD FingerPrint Function • Remove RN2104 /RN2103 refer UX310/X542UQ/2450. • Remove R2196 for X506 No oDD • Remove R2135 refer X542UQ • Remove R2161/R2161 • Remove C6920 & NET:SATAO_DEVSLP (Page23/69) • Remove R2310/R2308 • Change R2301 to SL2321 , • Add P4502 reserve (Page 45)
	2017/05/15	• Add USB EMCF (Page 52) • Remove C6920 for X506UA/UV no ODD • Remove EDP TX2/TX3 (Page 45) • Add Touch panel I2C • Change J4201 PN to 12023-00015200 /add R4203 (page 42) • UPADTE Power SCH (BAY MAX_20170515)
	2017/05/16	• modify J3101 PN to 12018-00200500 J3102 to 12018-00211200 J3701 to 12014-00711900 J6001 to 12033-00030700 J6002 to 12020-00025600 J6002 to 12065-00072200
	2017/05/17	• modify U4503/U4201 to 06016-01100000 • Add TPanel_INT# in J4501.33 • Add R4505 for SD_PWR_EN_# • Modify R0607/R0608 to JP0607/JP0608
	2017/05/18	• Update power SCH (X540UVK_MB_20170517_U22)
		• Modify Q4807 to 07G005107010 (N-MOSFET EM6K1GT2R EM76)
	2017/05/19	• Remove L5233 /L5204 /L5210 /SLN5213 /RN5203 /RN5201 for EMCF had reserve
	2017/05/24	• Modify Edp trace shortland location
		• Modify RN4811 PU to +5VS_HDMI_CRT
	2017/05/25	• Update Power SCH (X540UVK_MB_20170525_1350_U22)
	2017/05/26	• Remove R0602/R0603 JP0607/JP0608 / modify VCCSA power net
	2017/05/31	• Update Power SCH (X507_MB_20170531_1350_U22)
	2017/06/01	• Modify D6901 to D4502
		• ADD SATA0 DEVSLP function
		• remove U42 XTAL@ page 9
	2017/06/05	• remove Q4501 /R4511/R4501/C4503
	2017/06/06	• DDR SWAP follow Layout : ddr_swap_1404
		• ADD J6802/C6809/C6810 for USB IO Board
	2017/06/07	• Update X507_MB_20170607_1050_U22
		• Modify GPU Power CAP
		• Modify L4504/4509/4510 L5206/L5209 to temp_7_021687
		• Modify C2623 : 22UF from 11G2352226625390 to 11G2332226625320
	2017/06/08	• ADD USB IO Board Page_66
	2017/06/09	• X507_MB_20170609_1426_U22
	2017/06/12	• Change VRAM to GDDR5 256M X32 refer X542UQ
		• X507_MB_20170612_1856_U22
	2017/06/13	• X507_MB_20170613014_U22
		• Change connector follow connector list
	2017/06/14	• Modify TPanel_INT# to J4501 pin28
	2017/06/15	• MOVE I2C2_SDA_TCHPANEL/I2C2_SCL_TCHPANEL from GPP_F4/5 to GPP_C16/17
		• Remove R2142
		• Remove C1730
	2017/06/16	• Update J4201 to 12023-00025900
	2017/06/20	• Remove USB2.0 port 3
	2017/06/21	• Change EC(035011) PN to 06037-00050700
		• LED5904 to 07014-00190100 /LED 5905 to 07G01520043A
		• ADD C5104/C2505 ;C3010 ;C3105/C3106/C3107; C6904 /C6907/C6918 ;C7001 reserve for EMI
		• IO remove CE6601 C6603 EMCF change to bead solution
	2017/06/22	• Change SD card power solution to 06016-01090000 (U4201)
		• R4504 from 1K to 10K
		• Change Q4802 to SI2304DDS-T1-GE3
		• Change Q5905 to 2N7002
	2017/06/26	• Change C6605/C6606 to 0603
		• Update power sch x507_mb_20170626111B_u22
		• J6802 pin1/2/3 modify to +5VSUS
	2017/06/28	SR Gerber Out : X507UV_MB_6L_R10_20170628183O
	2017/06/30	• ADD USB IO ESD protect D6601
	2017/07/12	• Modify J3103 pin define from ME request
	2017/07/24	• Update X507UV_MB_6L_R11_20170724143O
	2017/07/26	• J5901/C5901 to 0 ;J5902/C5903 to N/A
	2017/07/27	• Bat connector
		• Update SD Solution base on X540UV_MB_ER_20170726-01_U22GDDR5
		• Update R4566 from 330 ohm改成100 ohm
		• R2122 change to 0,R7709 to N/A , PC9303change to 0
	2017/07/31	• JRST2401/JRST2402 modify to 0402 0ohm
		• USB Power Switch (U5201.4/J6802.4) enable pin from +3V to SUSC_EC#
	2017/08/01	• modify R4208 /R4205 /R4207 /R4209 footprint to 0402
X507UBR R1.0	2017/12/28	• change U2401 to 06004-00511800 for cost issue (page 4)
		• add R0501 & R0502 and set RN0503 & Q0501 as unstuff (page 5)
		• add R0610 & R0608 & R0609 to support U22 & U42 and change U0301M power net (page 6)
		• del unstuff resistors of XDP reserved in schematic (page 8)
		• add X0901 and related component to support U42 CPU (page 9)
		• modify green clock output connection to support U22 & U42, modify component include R2429 & R2433 & R2434 (page 24)
		• del U22 24MHz crystal solution(only support green clock input) due to layout space (page 24)
		• del R2637 due to SD controller power cannot connect to +3VSUS (page 26)
		• add panel LED_VCC power protection circuit (page 45)
		• modify Q5101 dual package MOS to Q5102(unstuff) & Q5103 as single package MOS for cost effective (page 51)
	2018/01/02	• add ISST function R2218 & R2220 & R2219 & R2221 (page 22)
		• add CLK_REQ# to GPU for N17(MX130) debug (page 24)
		• change Q4501 P/N to 07G005C73010 (page 45)
		• add PEX_CLK_REQ# to Q2401 for N17(MX130) debug (page 70)
	2018/01/03	• del C1034 C1049 C1046 C1062 C1068 C1065 C1044 C1063 C1031 C1045 C1048 C1030 for layout placement (page 10)
		• modify R2201.2 net name (page 22)
		• change U5204 & 5205 ECMF symbol due to PCB stack up change (page 52)
	2018/01/04	• change X0902 PN for system notice (page 9)
		• Update Power Schematic X507UBR_MB_6L_R10_20180103183O
		• change X2901 PN for system notice
	2018/01/05	• add R0907 for 24M XTAL Coley
	2018/01/09	• Q4501Change to 07005-A0260000
		• Delete CE1601/PC8196 /CE5202/CE5231
X507UBR R1.1	2018/02/27	• Modify W6507 Footprint to nbs_nut_1p_475
		• +VCCIO MOS Change PU +12VS
		• Change U7201/U7203 PN to 03008-00050000
		• modify C2909 to 1UF for RTC Timing
		• modify C2901/2902 from 8.2pf to 12 pf
		• modify C6502 to 0 Ohm for BAT_EN# always low
	2018/03/02	• Update Power Schematic
		• Change C5238 pakage for placement
		• Modify R2301/02/03 PU to +3VSUS
		• Modify C3708/3709 to D3708/3709 : 07024-01152200

BOM

ASUS	Project Name: X507UA/UV	Rev
Title : System History		
Size: D	Dept.: ASUSTeK COMPUTER INC	Engineer:
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Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0],ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQS[7:0], DQS#[7:0]
ECC strobe	DQSP[8], DQSN[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

eDP to LVDS

BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : LVDS CONNECTOR		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 46 of 102	

CPU XDP connector

BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : CPU_XDP		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Bull Tsai
Date: Friday, April 13, 2018	Sheet 7 of 102	

LPC DEBUG PORT

BOM

ASUS	Project Name: X507UA/UV	Rev: R1.0
Title : DEBUG PORT		
Size: A	Dept.: ASUSTeK COMPUTER INC. Engineer: Bull Tsai	
Date: Friday, April 13, 2018	Sheet 44 of 102	

<Variant Name>

	Title : DDR4_ON-BOARD_A_H32	
	Engineer: Bull Tsai	
Size: C	Project Name: X507UA/UV	Rev: R1.0
Date: Friday, April 13, 2018	Sheet 15 of 102	

BOM

/ISUS	Project Name **X507UA/UV**	Rev R1.0

Title :

Size D	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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/ISUS	Project Name **X507UA/UV**	Rev R1.0

Title :

Size C	**Dept.:** ASUSTeK COMPUTER INC. **Engineer:**	
Date: Friday, April 13, 2018	Sheet 12 of 102	

BOM

/ISUS	Project Name **X507UA/UV**	Rev R1.0

Title :

Size C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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	Project Name **X507UA/UV**	Rev R1.0

Title : RTL8402 (LAN+CR)

Size D	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai
Date: Friday, April 13, 2018	Sheet 33 of 102	

/ISUS	Project Name **X507UA/UV**	Rev R1.0

Title : RTL8402_RJ45

Size		
C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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BOM

/ISUS	Project Name **X507UA/UV**	Rev R1.0

Title :

Size C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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/ISUS	Project Name **X507UA/UV**	Rev R1.0

Title : HDD Board_HDD Conn_FPC

Size		
C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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BOM

	Project Name **X507UA/UV**	Rev R1.0

Title : SDIO_CR

Size		
A	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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	Project Name **X540UVK**	Rev R1.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Andy

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BOM

/ISUS	Project Name **X540UVK**	Rev R1.0

Title : **POWER_+VGFX_CORE**

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** **Andy**

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	Project Name **X540UVK**	Rev R1.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Andy

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	Project Name **X507UA/UV**	Rev R1.0

Title : CB-****

Size C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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BOM

/SUS	Project Name **X507UA/UV**	Rev R1.0

Title : CB-****

Size C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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	Project Name **X507UA/UV**	Rev R1.0

Title : CRT D-SUB

Size		
D	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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BOM

	Project Name **X507UA/UV**	Rev R1.0

Title : TV_****

Size C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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	Project Name **X507UA/UV**	Rev R1.0

Title : ASM1142_USB3.1_TYPEC

Size		
C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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Project Name

X507UA/UV

Rev

R1.0

Title : USB 3.1 MB Type-C

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER INC. NB1	Bull Tsai

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Project Name

X507UA/UV

Rev

R1.0

Title : PWR_SW&HALL_SW

Size	Dept.:	Engineer:
A	ASUSTeK COMPUTER INC.	Bull Tsai

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	Project Name **X507UA/UV**	Rev R1.0

Title : Sensors

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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/SUS	Project Name **X507UA/UV**	Rev R1.0

Title : ****

Size		
C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** **Bull Tsai**

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/ISUS	Project Name **X507UA/UV**	Rev R1.0

Title : NFC

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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BOM

Project Name

X507UA/UV

Rev

R1.0

Title : IO_SATA HDD & SPEAKER

Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER INC.	Bull Tsai

Date: Friday, April 13, 2018

BOM

	Project Name **X507UA/UV**	Rev R1.0

Title : IO_USB*2 & CR & LED

Size C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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	Project Name **X507UA/UV**	Rev R1.0

Title : VGA_****

Size		
C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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	Project Name **X507UA/UV**	Rev R1.0

Title : VGA_****

Size		
C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Bull Tsai

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/SUS	Project Name **X507UBR**	Rev R1.0

Title : PW_

Size Custom	**Dept.:** NB Power Team	**Engineer:** SS

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	Project Name X507UBR	Rev R1.0

Title : PW_

Size		
A3	**Dept.:** NB Power Team	**Engineer:** SS

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BOM

	Project Name **X507UBR**	Rev R1.0

Title : PW_

Size Custom	**Dept.:** NB Power Team	**Engineer:** SS

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BOM

	Project Name **X507UBR**	Rev R1.0

Title : PW_

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** SS

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	Project Name **X540UVK**	Rev R1.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Andy

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	Project Name **X540UVK**	Rev R1.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Andy

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