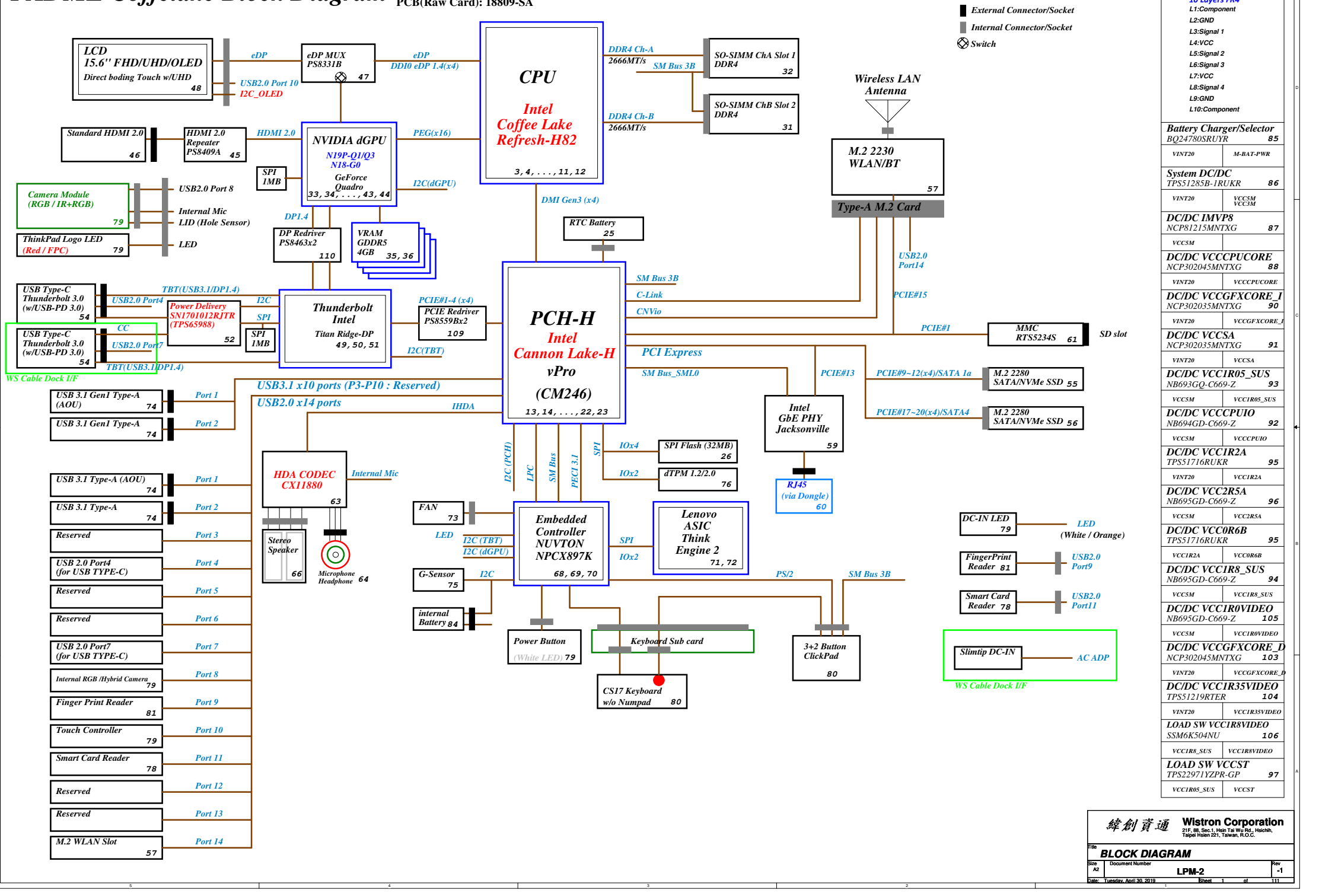
PADME Coffelake Block Diagram

Project Code: 4PD0GU010001
PCB(Raw Card): 18809-SA



PCB Layer Stackup

10 Layers FR4

L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:VCC
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector	BQ24780SRUYR	85
VINT20	M-BAT-PWR	
System DC/DC	TPS51285B-1RUKR	86
VINT20	VCC5M VCC3M	
DC/DC IMVP8	NCP81215MNTXG	87
VCC5M		
DC/DC VCCCPUCORE	NCP302045MNTXG	88
VINT20	VCCCPUCORE	
DC/DC VCCGFXCORE_I	NCP302035MNTXG	90
VINT20	VCCGFXCORE_I	
DC/DC VCCSA	NCP302035MNTXG	91
VINT20	VCCSA	
DC/DC VCC1R05_SUS	NB693GQ-C669-Z	93
VCC5M	VCC1R05_SUS	
DC/DC VCCCPUIO	NB694GD-C669-Z	92
VCC5M	VCCCPUIO	
DC/DC VCC1R2A	TPS51716RUKR	95
VINT20	VCC1R2A	
DC/DC VCC2R5A	NB695GD-C669-Z	96
VCC5M	VCC2R5A	
DC/DC VCC0R6B	TPS51716RUKR	95
VCC1R2A	VCC0R6B	
DC/DC VCC1R8_SUS	NB695GD-C669-Z	94
VCC5M	VCC1R8_SUS	
DC/DC VCC1R0VIDEO	NB695GD-C669-Z	105
VCC5M	VCC1R0VIDEO	
DC/DC VCCGFXCORE_D	NCP302045MNTXG	103
VINT20	VCCGFXCORE_D	
DC/DC VCC1R35VIDEO	TPS51219RTER	104
VINT20	VCC1R35VIDEO	
LOAD SW VCC1R8VIDEO	SSM6K504NU	106
VCC1R8_SUS	VCC1R8VIDEO	
LOAD SW VCCST	TPS22971YZPR-GP	97
VCC1R05_SUS	VCCST	

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Title: BLOCK DIAGRAM
Size: A2 | Document Number: LPM-2 | Rev: -1
Date: Tuesday, April 30, 2019 | Sheet 1 of 111

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

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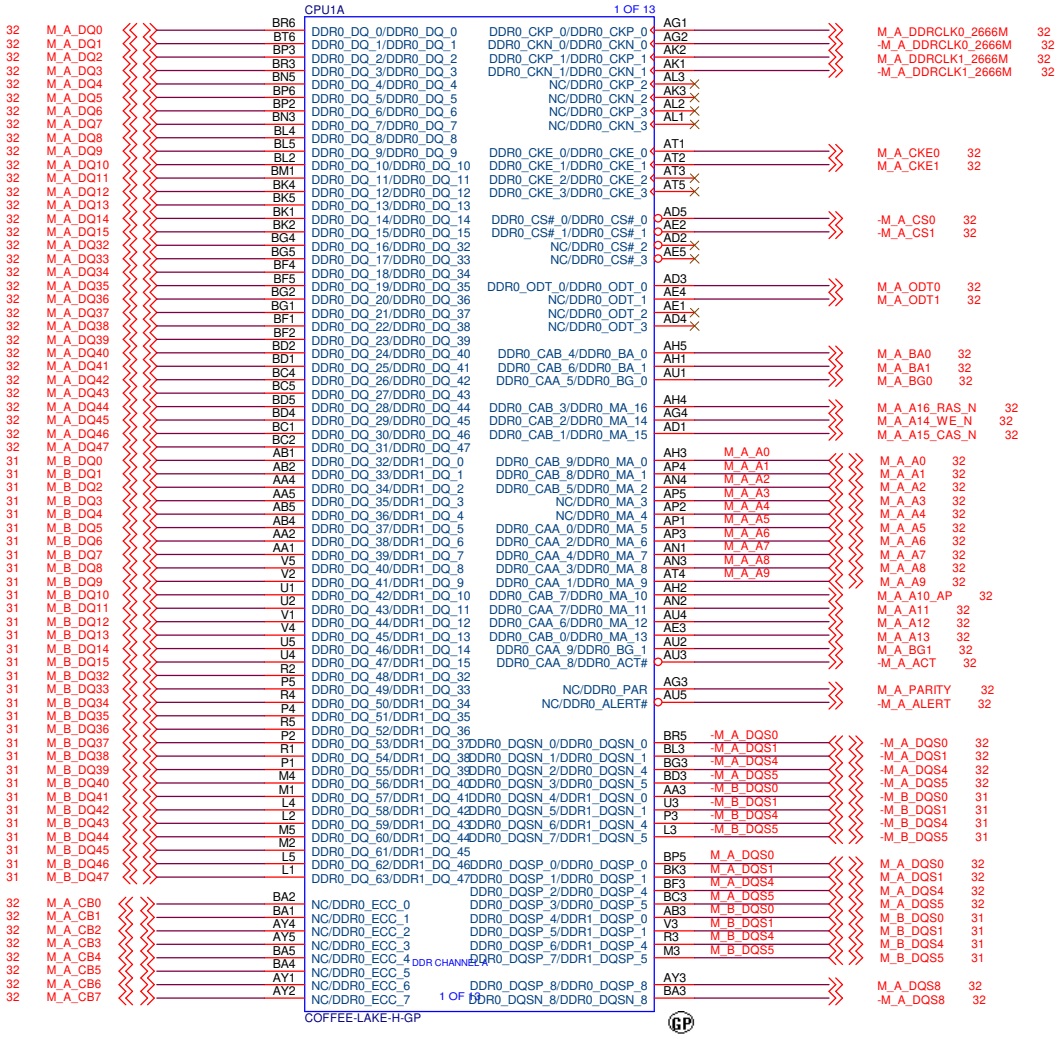
Title ***DESCRIPTION***

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 2 of 111

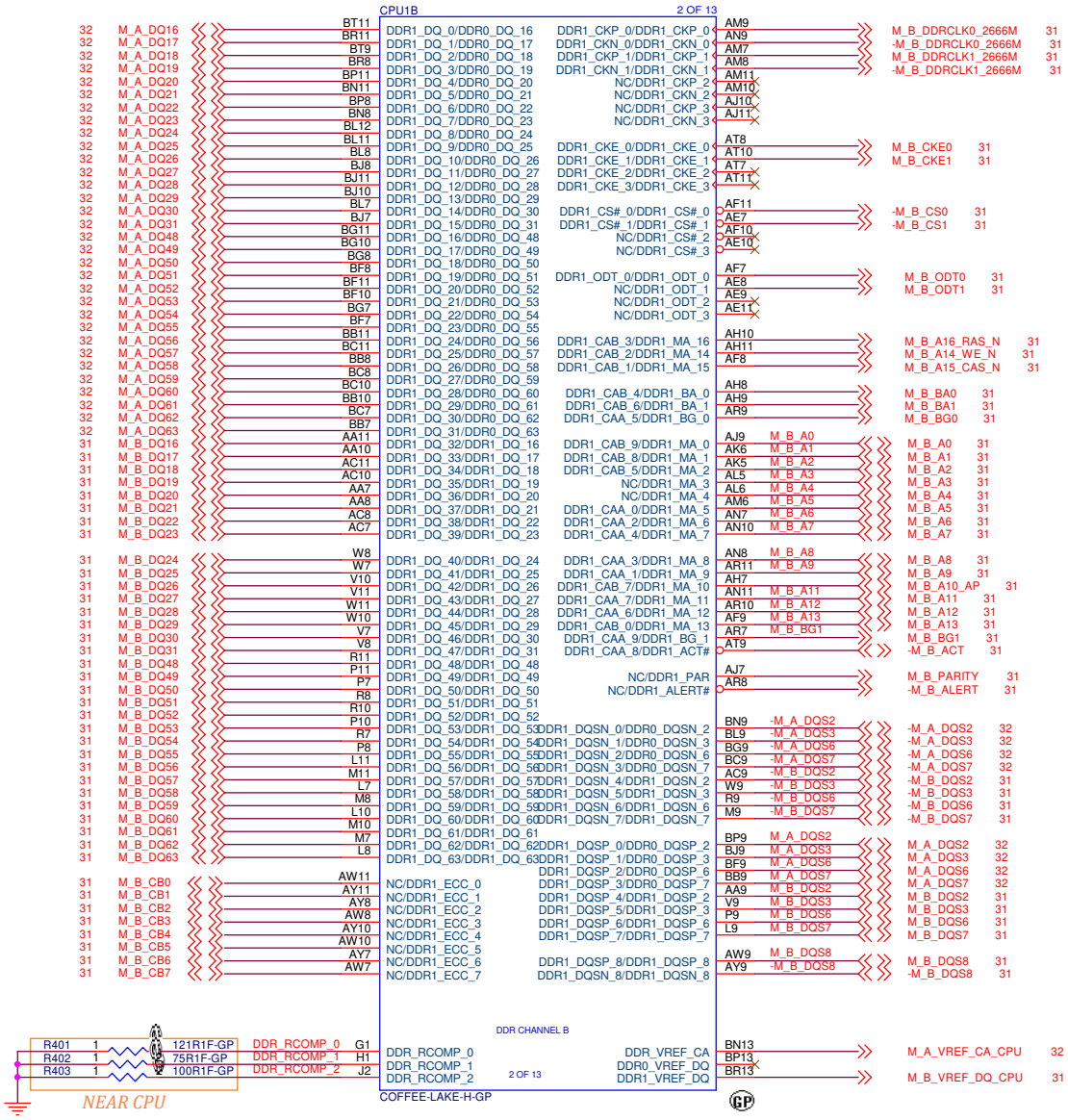


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU CFL-H DDR4 CH-A**

Size	Document Number	Rev
A3	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 3 of 111



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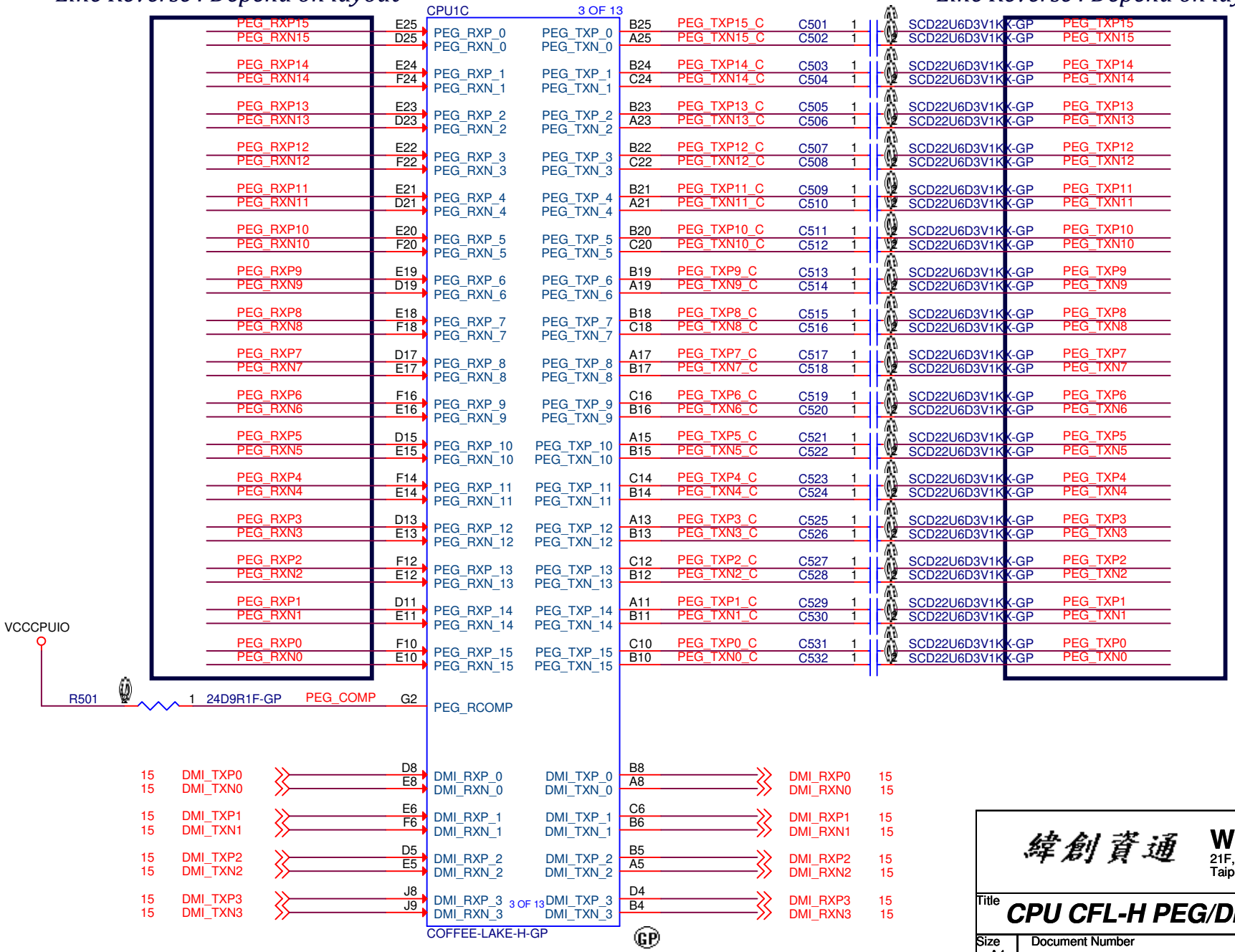
Title	***CPU CFL-H DDR4 CH-B***
Size: A3	Document Number: **LPM-2**
Rev: -1	
Date: Tuesday, April 30, 2019	Sheet 4 of 111

33 PEG_RXP[15:0]
33 PEG_RXN[15:0]
33 PEG_TXP[15:0]
33 PEG_TXN[15:0]

Line Reverse : Depend on layout

Line Reverse : Depend on layout



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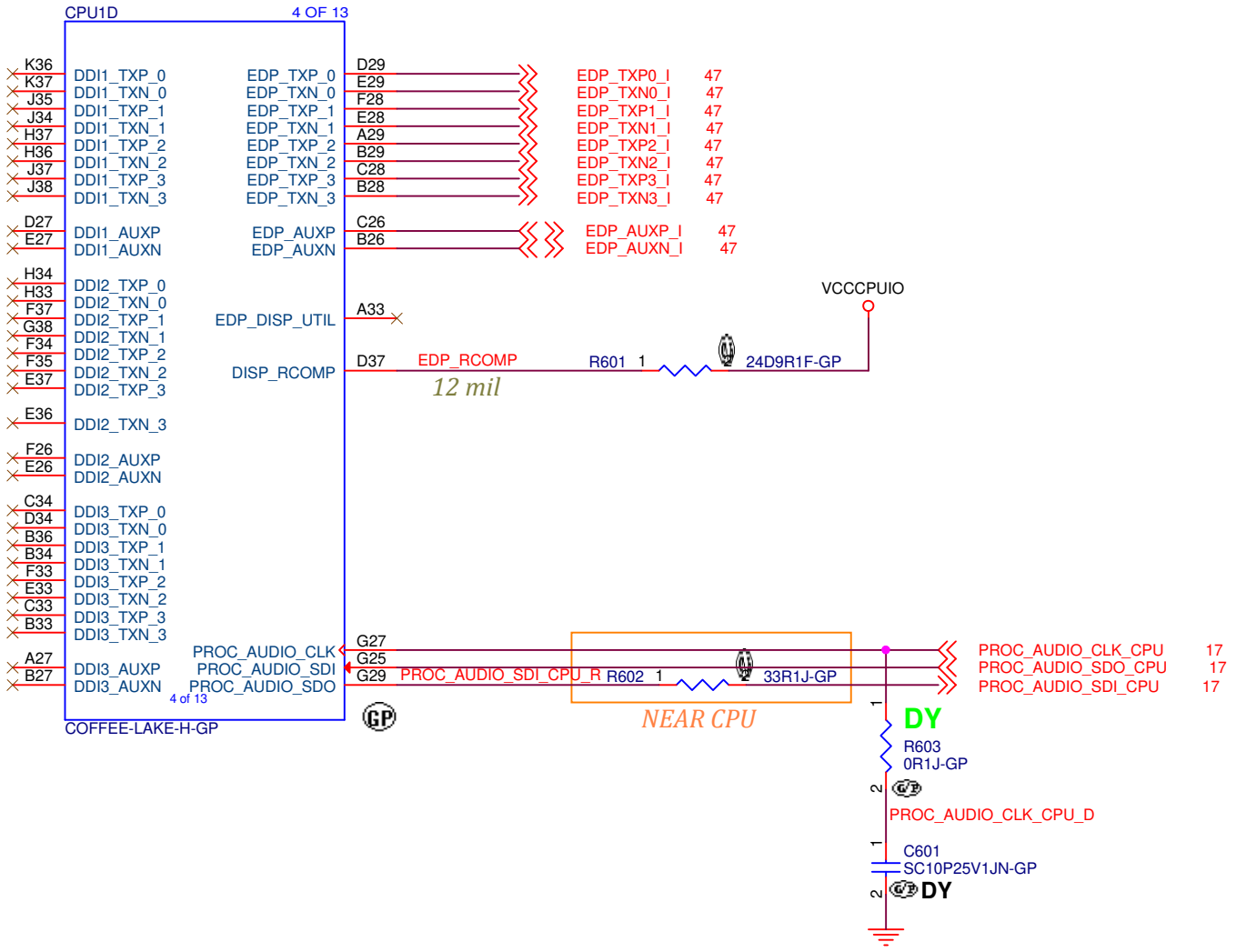
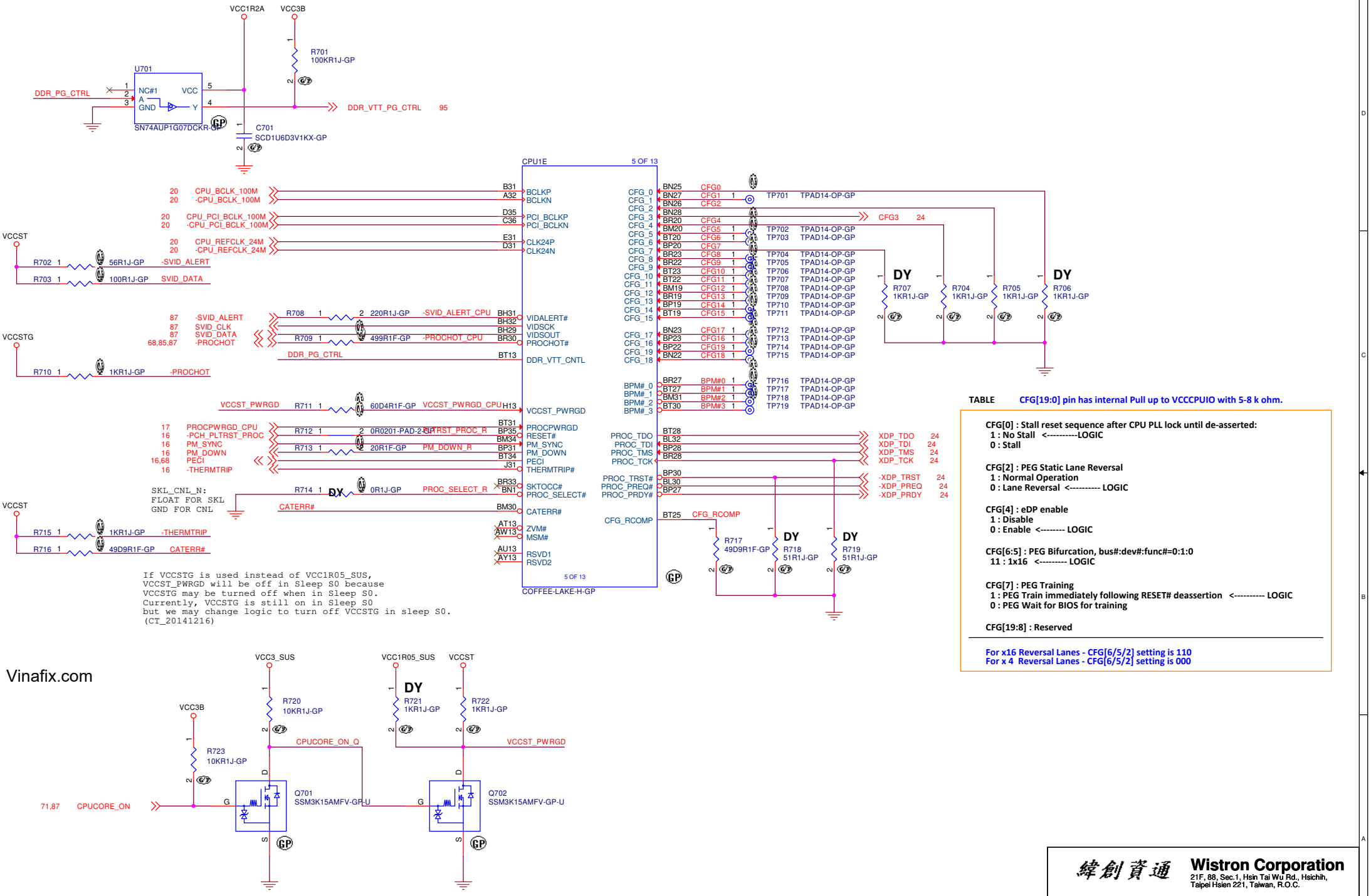
Title **CPU CFL-H PEG/DMI**

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 5 of 111



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU CFL-H DDI/EDP***	
Size A4	Document Number **LPM-2**	Rev **-1**
Date: Tuesday, April 30, 2019	Sheet 6 of 111	



緯創資通 **Wistron Corporation**
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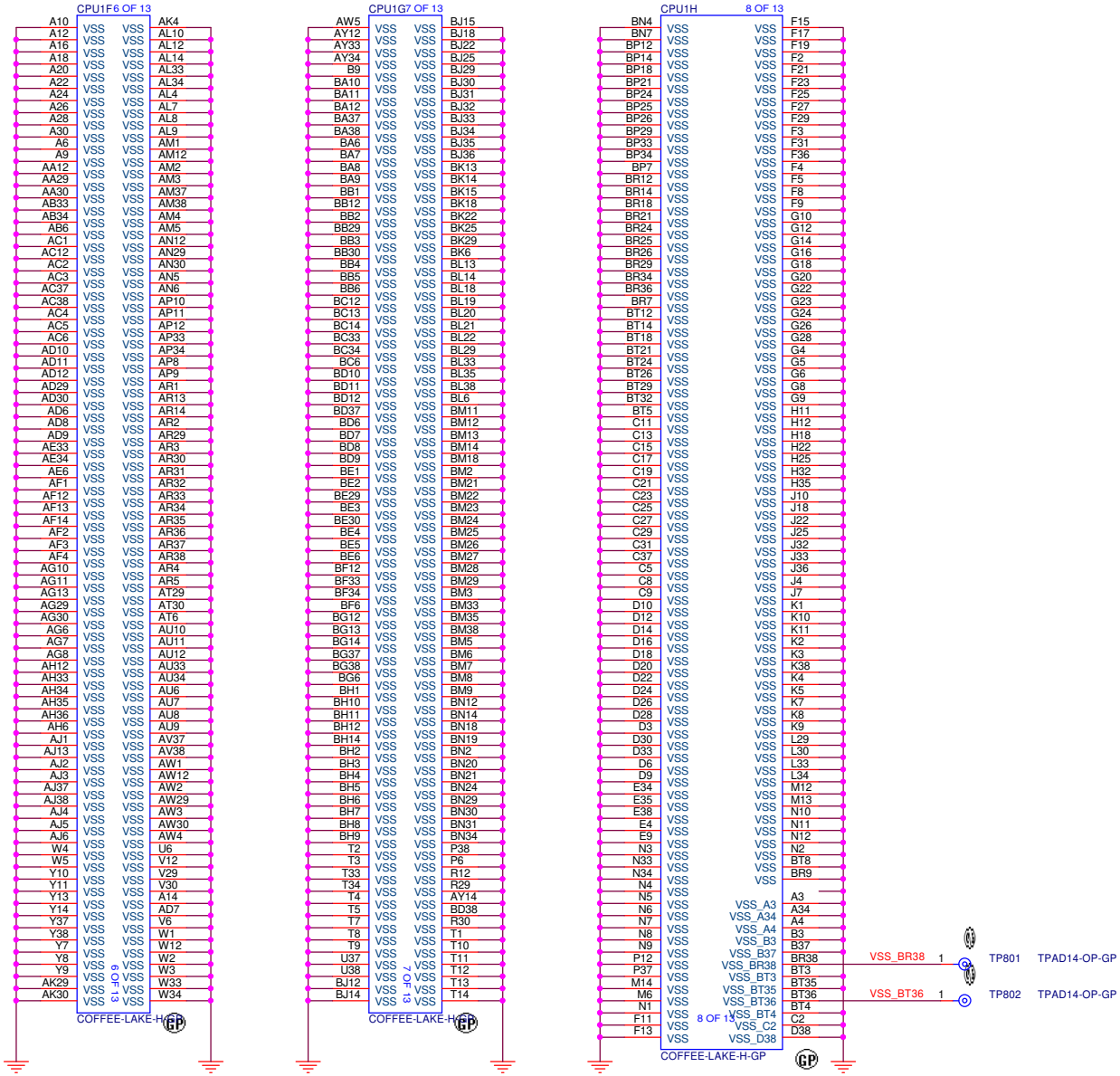
Taipei Hsien 221, Taiwan, R.O.C.

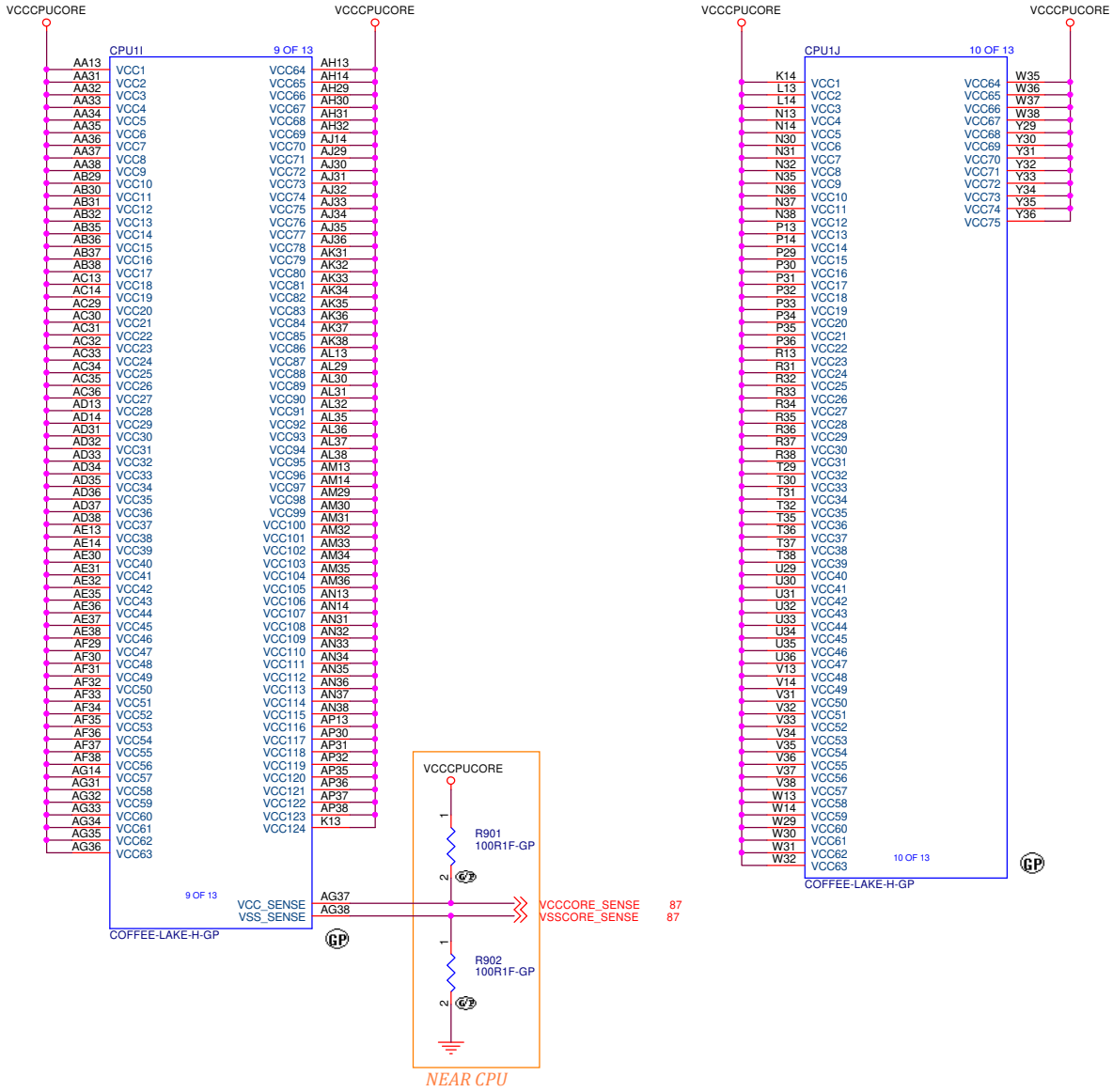
Title: **CPU CFL-H MISC/CLK/JTAG/CFG**

Size	Document Number	Rev
A3	LPM-2	-1

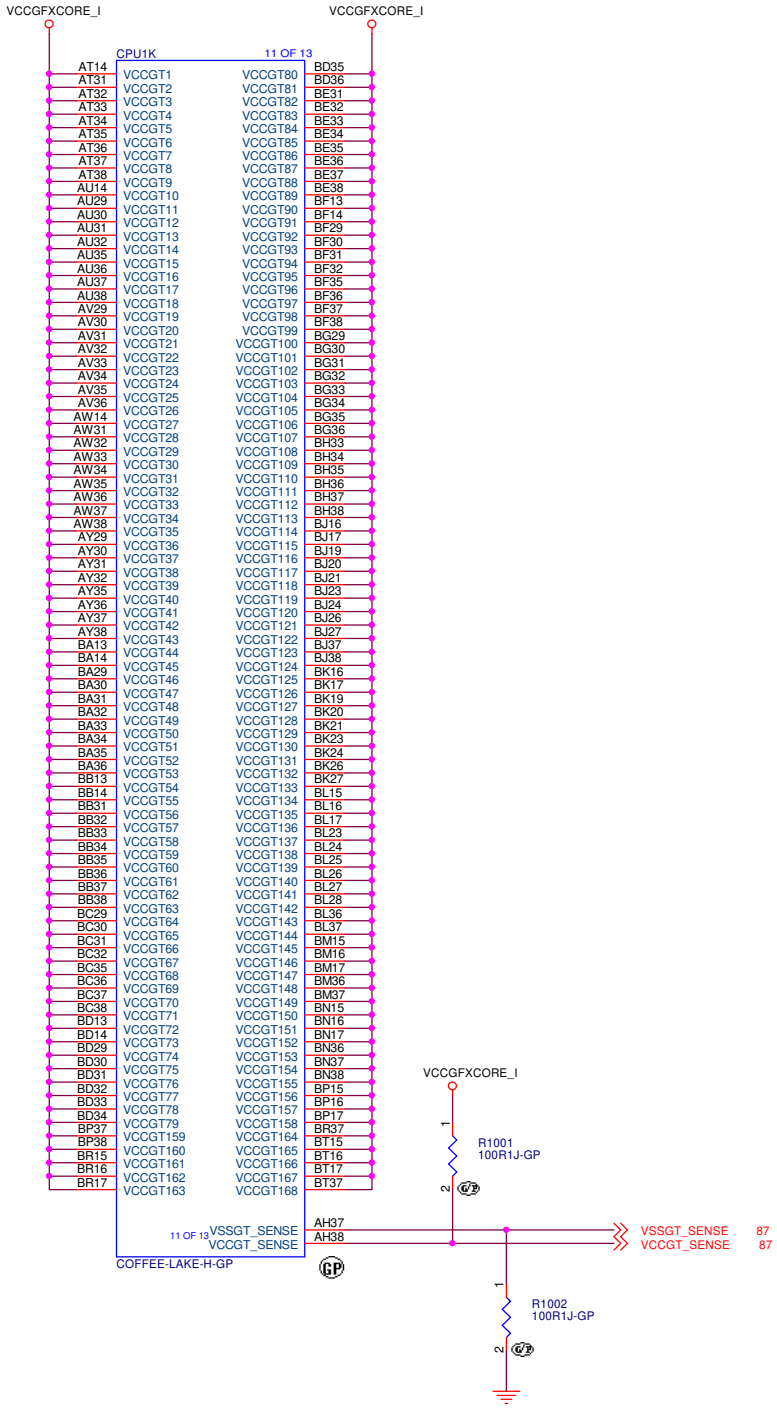
Date: Tuesday, April 30, 2019 Sheet 7 of 111



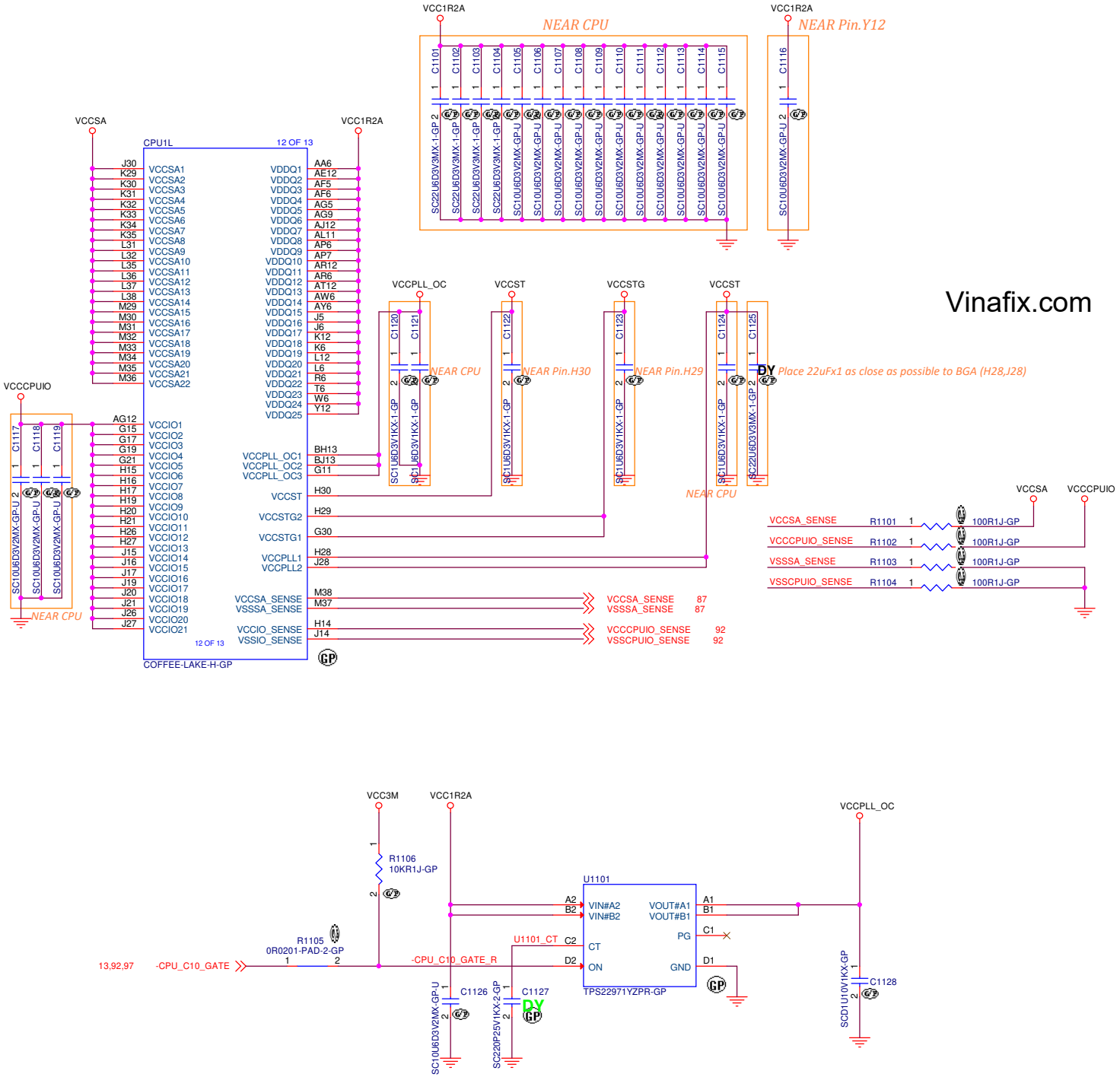
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU CFL-H GND***	
Size: A3	Document Number: **LPM-2**	Rev: -1
Date: Tuesday, April 30, 2019	Sheet 8 of 111	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***CPU CFL-H VCC***		
Size A3	Document Number **LPM-2**		Rev -1
Date: Tuesday, April 30, 2019		Sheet 9 of 111	



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU CFL-H VCCGT		
Size: A3	Document Number: LPM-2	Rev: -1
Date: Tuesday, April 30, 2019	Sheet 10 of 111	



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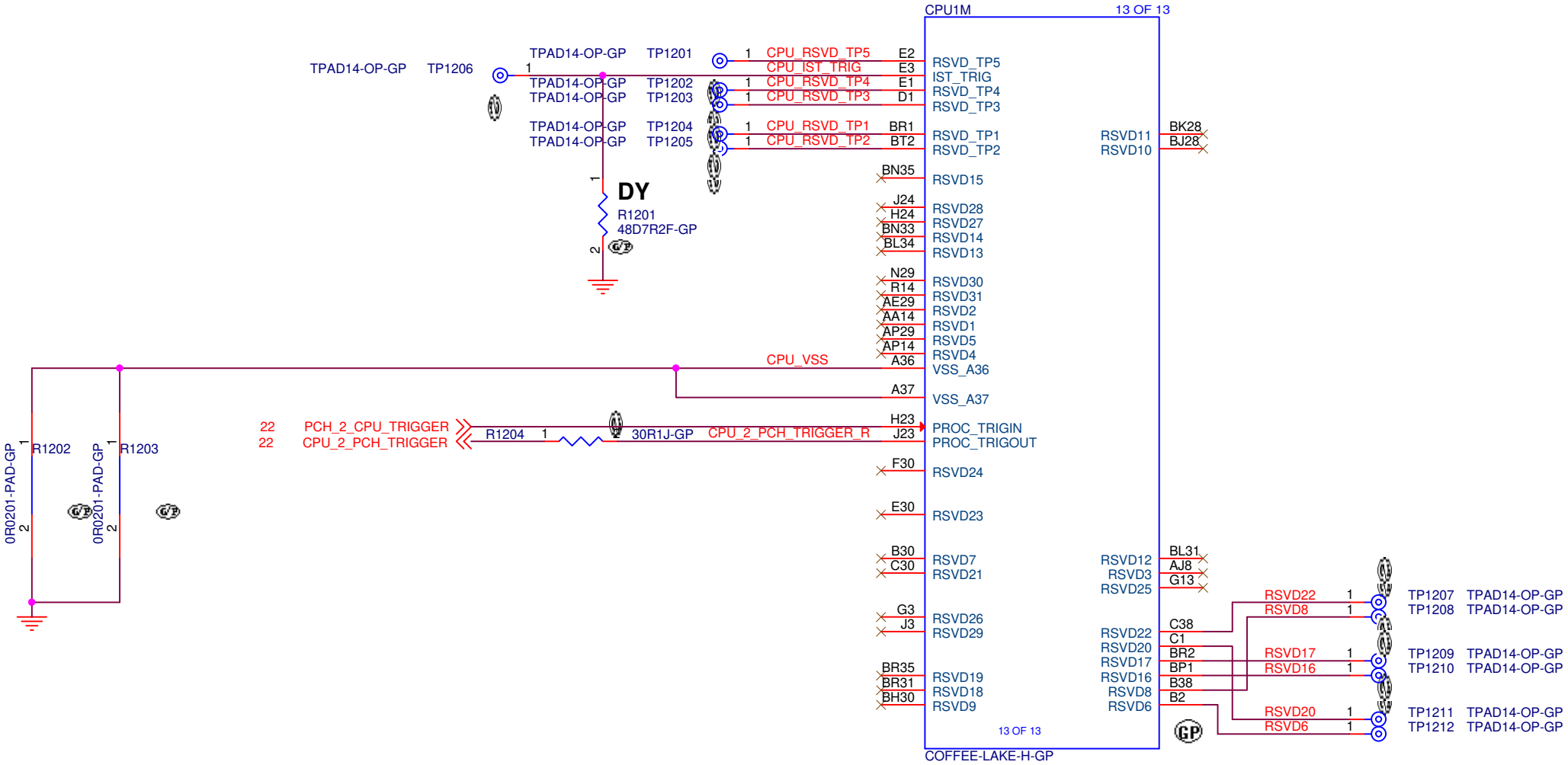
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU CFL-H VCCSA/VCCIO/VDD***
Size: A3	Document Number: **LPM-2**
Rev: -1	
Date: Tuesday, April 30, 2019	Sheet 11 of 111



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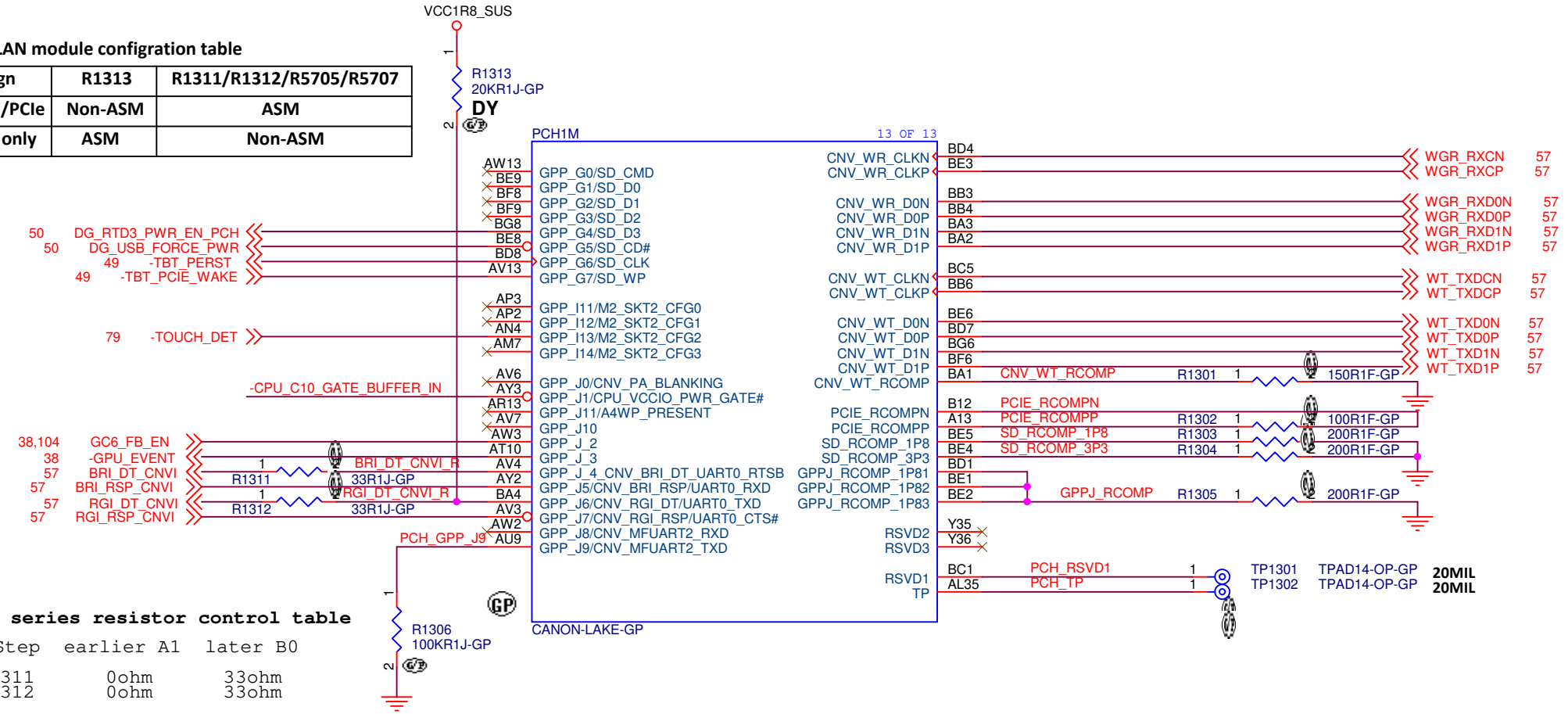
Title: ***CPU CFL-H RSVD***

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 12 of 111

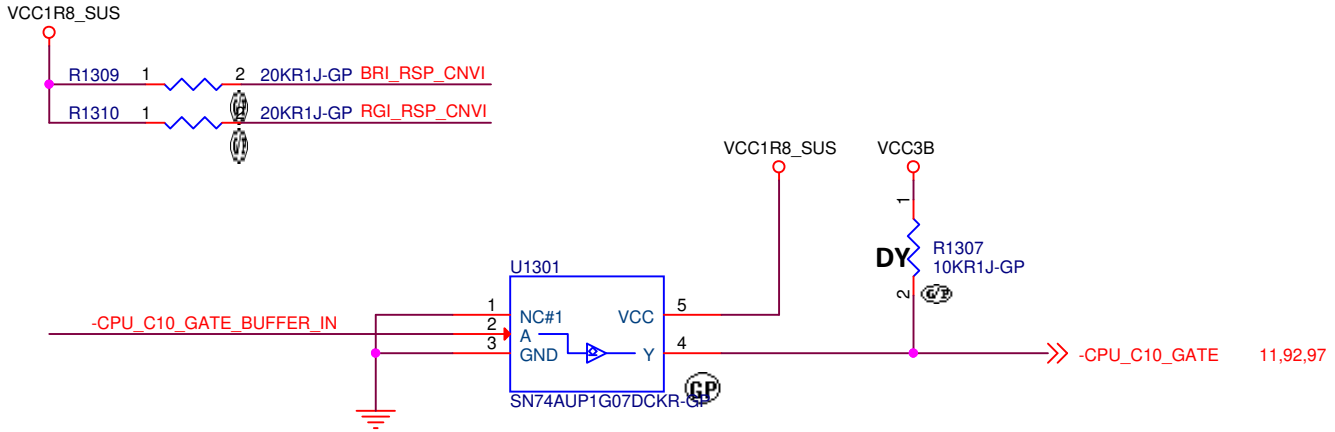
WLAN module configration table

Design	R1313	R1311/R1312/R5705/R5707
CNVi/PCIe	Non-ASM	ASM
PCIe only	ASM	Non-ASM



CNVi BT series resistor control table

PCH Step	earlier A1	later B0
R1311	0ohm	33ohm
R1312	0ohm	33ohm



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Title: **PCH CNL-H CNV**

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 13 of 111

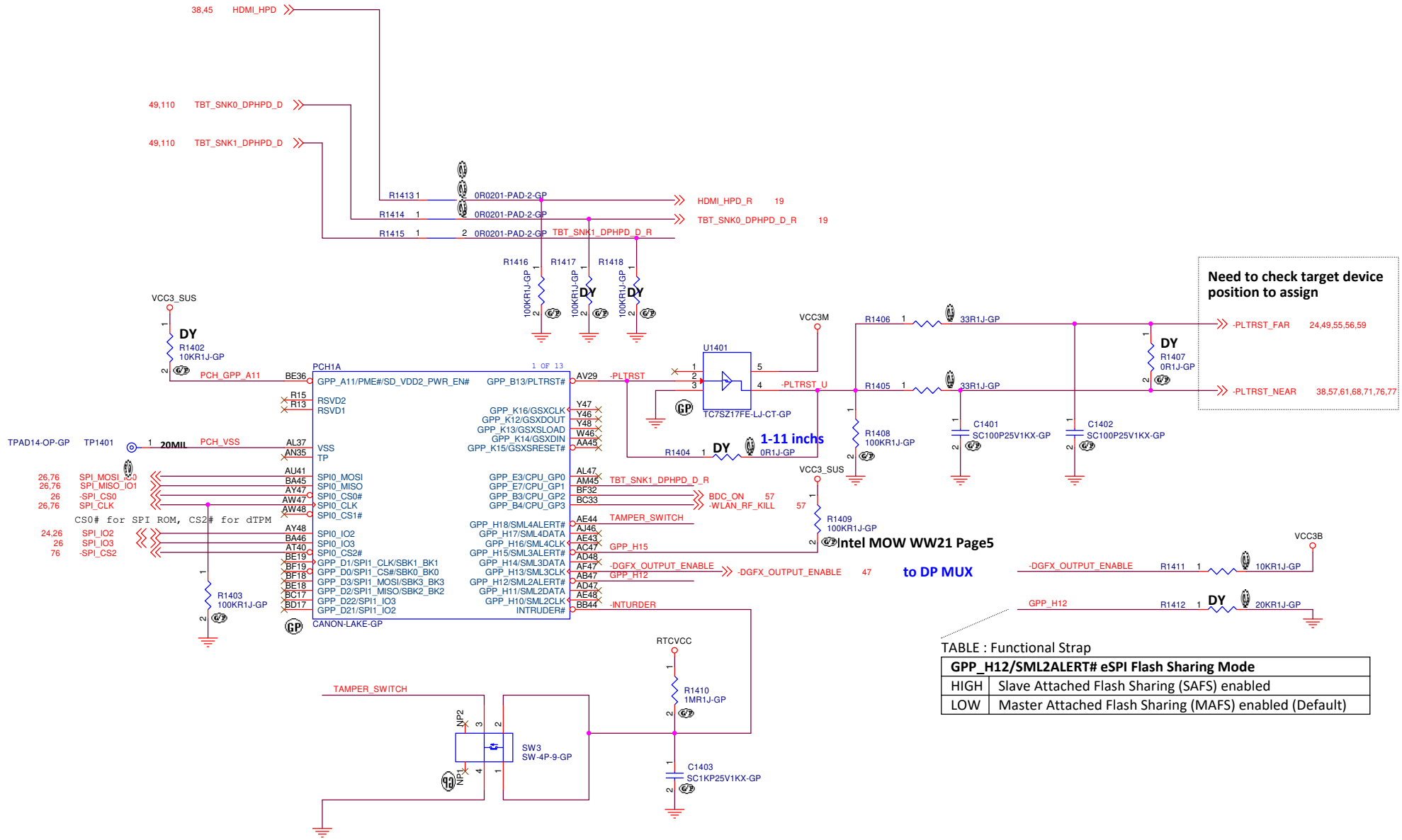

TABLE : Functional Strap

GPP_H12/SML2ALERT# eSPI Flash Sharing Mode	
HIGH	Slave Attached Flash Sharing (SAFS) enabled
LOW	Master Attached Flash Sharing (MAFS) enabled (Default)

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Title: **PCH CNL-H SPI**

Size	Document Number	Rev
A3	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 14 of 111

HSIO Port	CM246	Net Name
Port0	USB3.1 #1	USB3P1
Port1	USB3.1 #2	USB3P2
Port2	USB3.1 #3	N/A
Port3	USB3.1 #4	N/A
Port4	USB3.1 #5	N/A
Port5	USB3.1 #6	N/A
Port6	USB3.1 #7 / PCIe #1	PCIE1
Port7	USB3.1 #8 / PCIe #2	N/A
Port8	USB3.1 #9 / PCIe #3	N/A
Port9	USB3.1 #10 / PCIe #4	N/A
Port10	PCIe #5 / GbE	N/A
Port11	PCIe #6	N/A
Port12	PCIe #7	N/A
Port13	PCIe #8	N/A
Port14	PCIe #9 / GbE	PCIE12L3
Port15	PCIe #10	PCIE12L2
Port16	PCIe #11 / SATA #0a	PCIE12L1
Port17	PCIe #12 / SATA #1a / GbE	PCIE12L0_SATA1A
Port18	PCIe #13 / SATA #0b / GbE	PCIE13
Port19	PCIe #14 / SATA #1b	N/A
Port20	PCIe #15	PCIE15
Port21	PCIe #16	N/A
Port22	PCIe #17 / SATA #4	PCIE17L0_SATA4
Port23	PCIe #18 / SATA #5	PCIE17L1
Port24	PCIe #19 / SATA #6	PCIE17L2
Port25	PCIe #20 / SATA #7	PCIE17L3
Port26	PCIe #21	PCIE21L0
Port27	PCIe #22	PCIE21L1
Port28	PCIe #23	PCIE21L2
Port29	PCIe #24	PCIE21L3

USB2.0 Port Assignment	
Port1	System Port (AOU)
Port2	System Port
Port3	N/A
Port4	USB Type-C #1
Port5	N/A
Port6	N/A
Port7	USB Type-C #2
Port8	2D CAMERA
Port9	Fingerprint Reader
Port10	Touch Panel
Port11	Smart Card Reader
Port12	Reserved
Port13	N/A
Port14	WLAN (Bluetooth)

PCIe Port Assignment	
Port1	Media Card Controller
Port9	M.2 SSD0 (PCIe L3)
Port10	M.2 SSD0 (PCIe L2)
Port11	M.2 SSD0 (PCIe L1)
Port12	M.2 SSD0 (PCIe L0)
Port13	GbE PHY
Port14	N/A
Port15	WLAN
Port16	WWAN
Port17	M.2 SSD1 (PCIe L0)
Port18	M.2 SSD1 (PCIe L1)
Port19	M.2 SSD1 (PCIe L2)
Port20	M.2 SSD1 (PCIe L3)
Port21	Thunderbolt (PCIe L0)
Port22	Thunderbolt (PCIe L1)
Port23	Thunderbolt (PCIe L2)
Port24	Thunderbolt (PCIe L3)

PCH1B — 2 OF 13 — CANON-LAKE-GP

Media Card

USB2_COMP RES : Place within 1 inch
USB2_VBUSSENSE / USB2_ID
USB OTG FUNCTION SUPPORT

Phase	ID2	ID1	ID0
EVT	0	0	1
FVT	0	1	0
SIT	0	1	1
SIT-R	1	0	0
SVT	1	0	1

Planar ID Table

EC :PD2_SIT_001

Core	ID3
6 core	0
8 core	1

CPU Configration Table

ID4	
0	SYNC
1	ASYNC

PLANARID4

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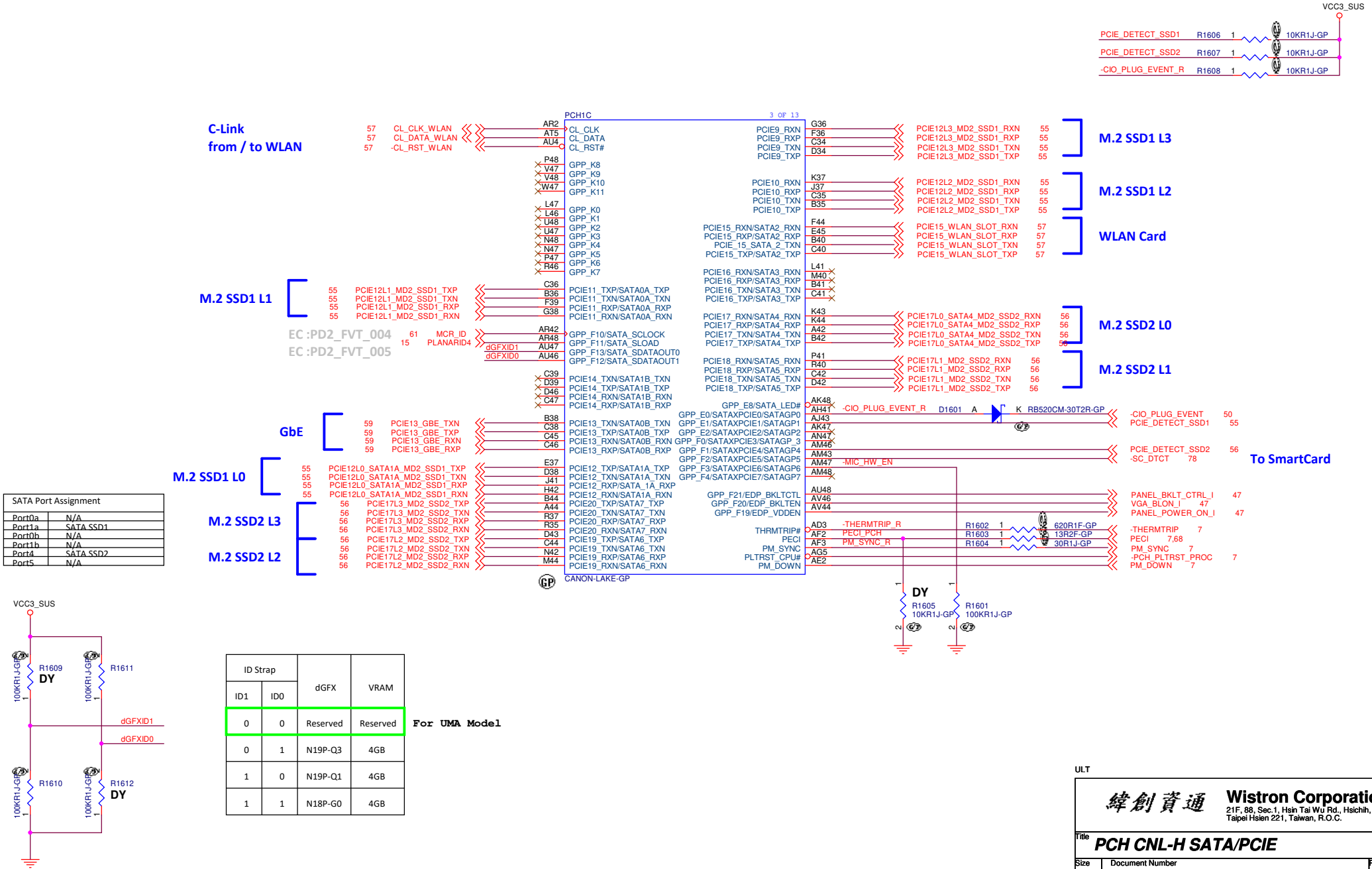
Title: PCH CNL-H DMI/PCIE/USB
Size: A3 | Document Number: LPM-2 | Rev: -1
Date: Thursday, June 06, 2019 | Sheet 15 of 111



SATA Port Assignment	
Port0a	N/A
Port1a	SATA SSD1
Port0b	N/A
Port1b	N/A
Port4	SATA SSD2
Port5	N/A

ID Strap		dGFX	VRAM
ID1	ID0		
0	0	Reserved	Reserved
0	1	N19P-Q3	4GB
1	0	N19P-Q1	4GB
1	1	N18P-G0	4GB

For UMA Model

ULT

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Title: **PCH CNL-H SATA/PCIE**

Size	Document Number	Rev
A3	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 16 of 111

TABLE : Functional Strap

HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descritor and/or the ME regions of the SPI after MFG Done bit is set.

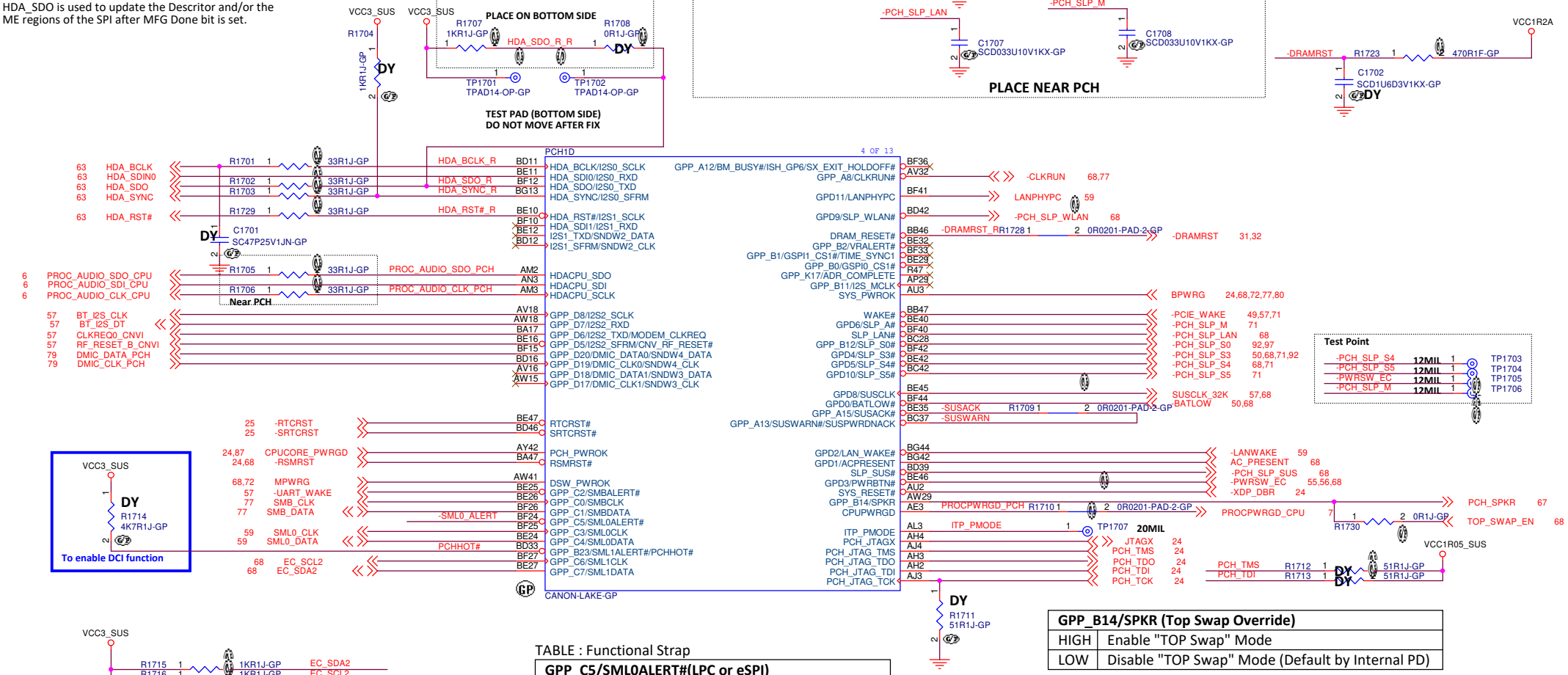

TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confldentlality
LOW	Disable ME Crypto TLS(Default)

TABLE : Functional Strap

GPP_B23/SML1ALERT#/PCHHOT#(Intel DCI-OOB)	
HIGH	Enable Intel DCI-OOB
LOW	Disable Intel DCI-OOB (Default)

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

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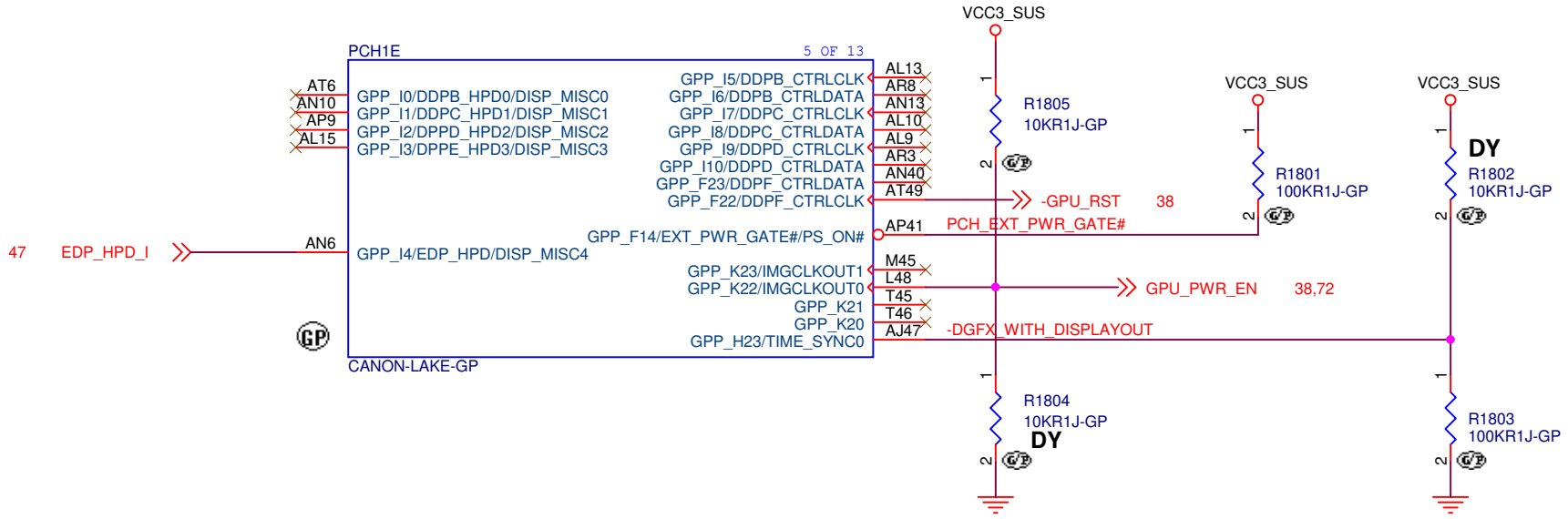
Title: PCH CNL-H AUDIO/SMBUS/JTAG

Size	Document Number	Rev
A3	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 17 of 111



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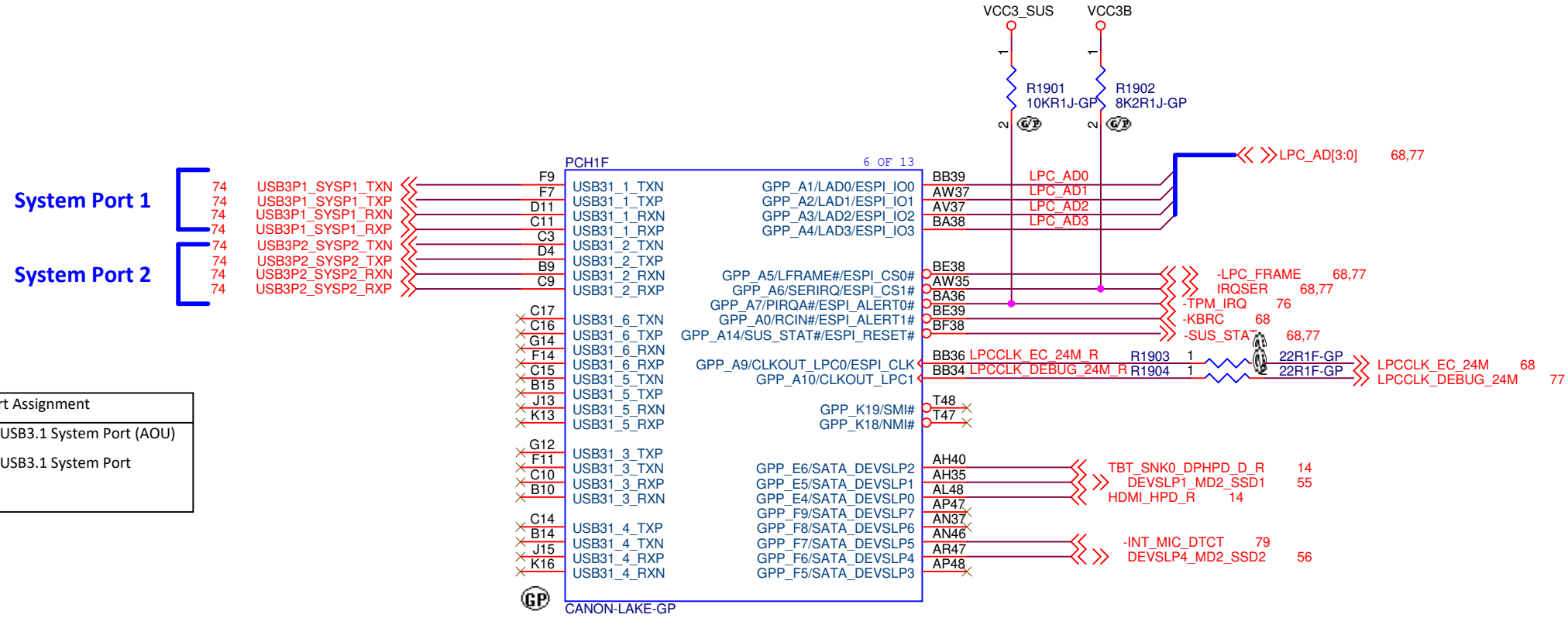
Title	***PCH CNL-H DDI CONTROL***	
Size A4	Document Number **LPM-2**	Rev **-1**
Date: Tuesday, April 30, 2019	Sheet 18 of 111	



USB 3.1 Port Assignment	
Port1	USB3.1 System Port (AOU)
Port2	USB3.1 System Port

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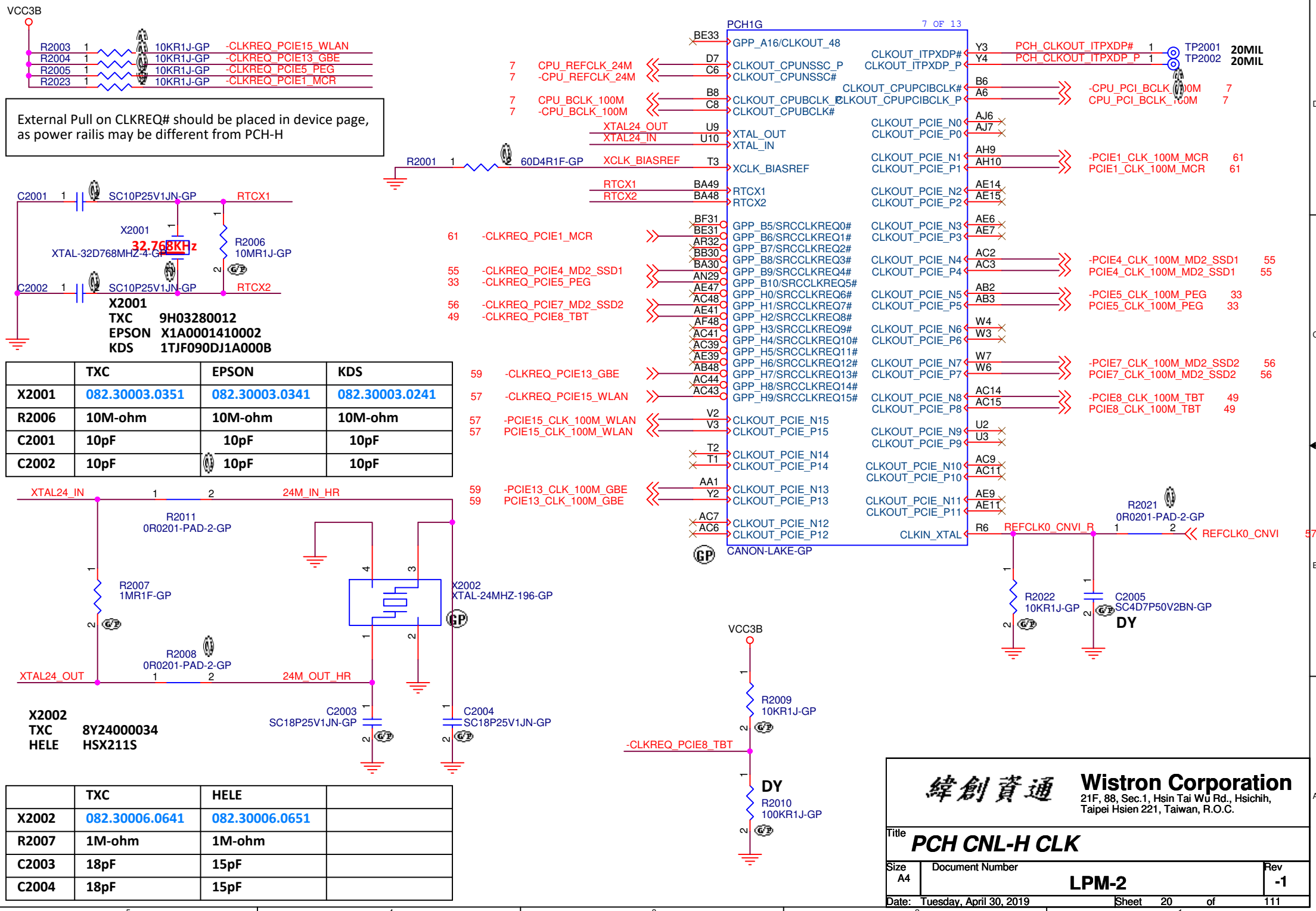
Title: **PCH CNL-H USB3/LPC**

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 19 of 111



	TXC	EPSON	KDS
X2001	082.30003.0351	082.30003.0341	082.30003.0241
R2006	10M-ohm	10M-ohm	10M-ohm
C2001	10pF	10pF	10pF
C2002	10pF	10pF	10pF

	TXC	HELE	
X2002	082.30006.0641	082.30006.0651	
R2007	1M-ohm	1M-ohm	
C2003	18pF	15pF	
C2004	18pF	15pF	

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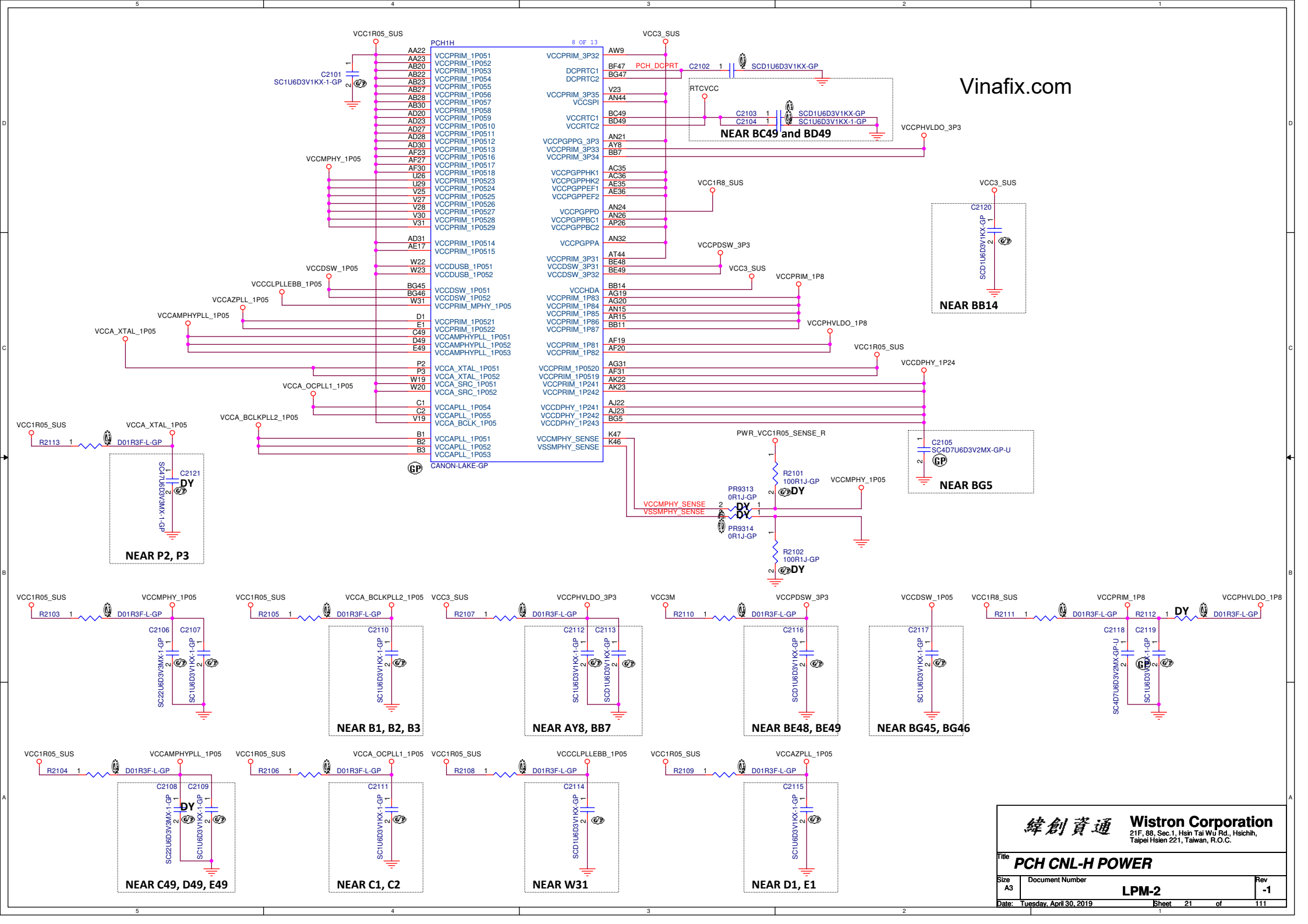
Title **PCH CNL-H CLK**

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 20 of 111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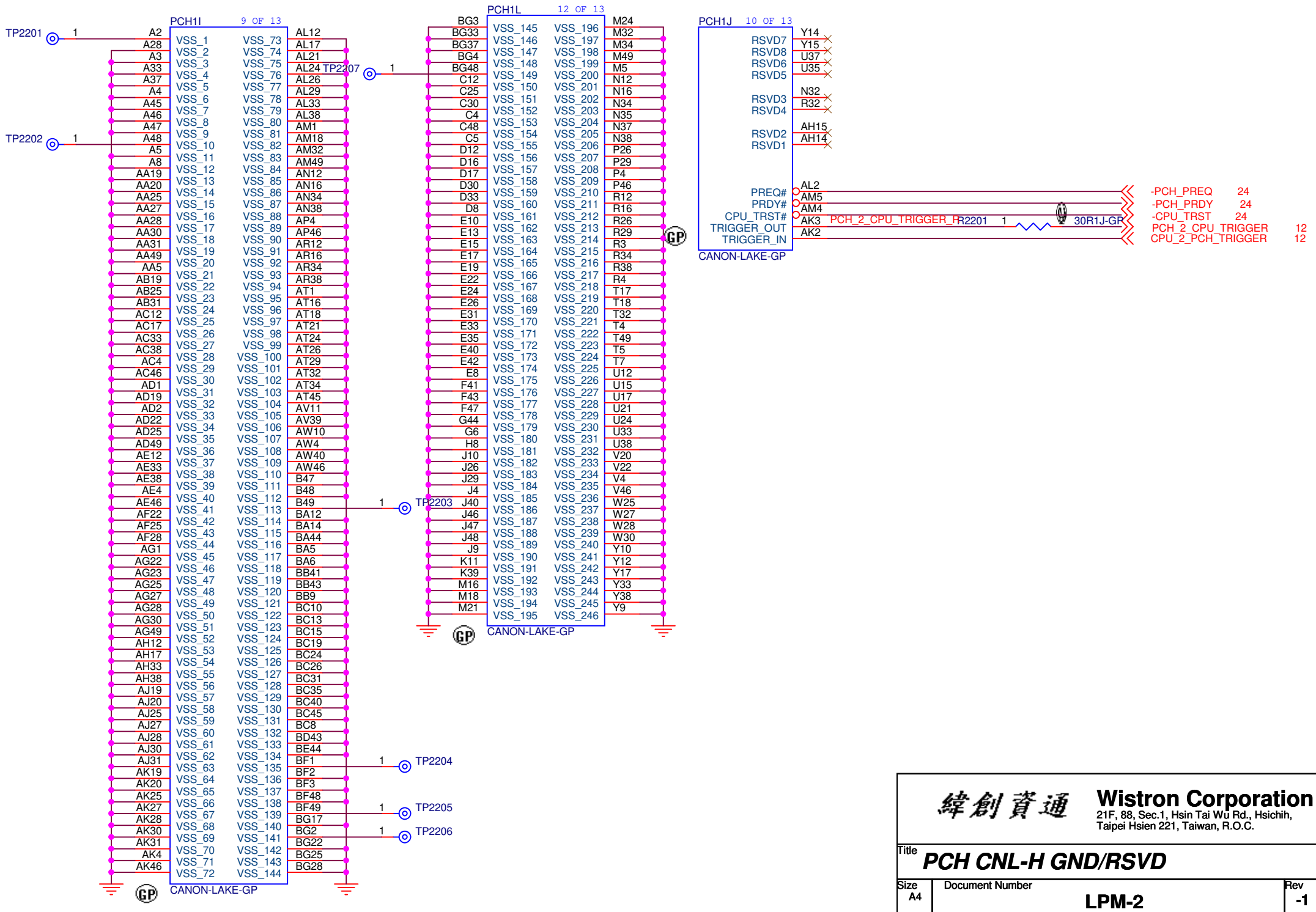
PCH1H
8 OF 13
CANON-LAKE-GP
VCC1R05_SUS
VCC3_SUS
VCCMPHY_1P05
VCCDSW_1P05
VCCCLPLLEBB_1P05
VCCAZPLL_1P05
VCCAMPHYPLL_1P05
VCCA_XTAL_1P05
VCCA_OCPLL1_1P05
VCCA_BCLKPLL2_1P05
VCC1R8_SUS
VCCPDSW_3P3
VCCPRIM_1P8
VCCPHVLDO_1P8
VCCPHVLDO_3P3
VCCDPHY_1P24
PCH_DCPRT
RTCVCC
PWR_VCC1R05_SENSE_R
VCCMPHY_SENSE
VSSMPHY_SENSE
NEAR BC49 and BD49
NEAR BB14
NEAR BG5
NEAR P2, P3
NEAR B1, B2, B3
NEAR AY8, BB7
NEAR BE48, BE49
NEAR BG45, BG46
NEAR C49, D49, E49
NEAR C1, C2
NEAR W31
NEAR D1, E1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH CNL-H POWER
LPM-2
Size A3
Rev -1
Date: Tuesday, April 30, 2019
Sheet 21 of 111



緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH CNL-H GND/RSVD**

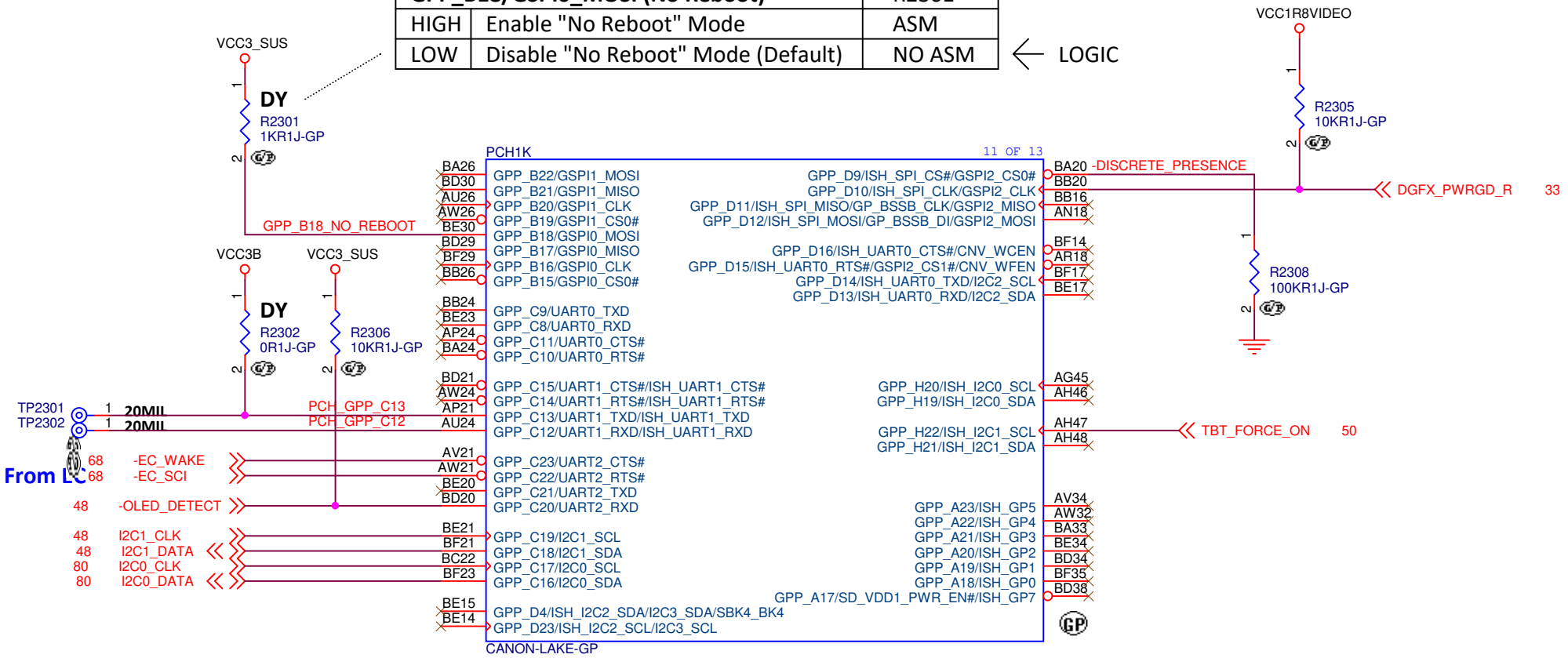
Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 22 of 111

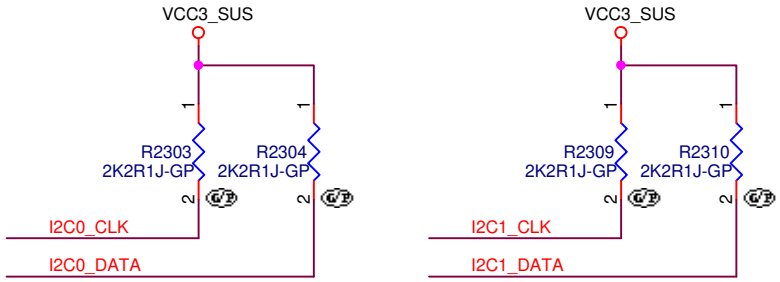
TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R2301
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

← LOGIC



Vinafix.com



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH CNL-H GSPI/UART/I2C**

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 23 of 111

XDP

TABLE : CPU ITP DEBUG REPORT

		NO Use	Individual Port	DCI 2.0 w/o connector
XDPR1	R2401	NO ASM	NO ASM	ASM
XDPR27	R2428	NO ASM	ASM	NO ASM
XDPR28	R2408	NO ASM	ASM	NO ASM
XDPR11	R2413	NO ASM	ASM	ASM
XDPC1	C2401	NO ASM	ASM	NO ASM
PCHR142	R2411	ASM	ASM	ASM
XDPR23	R2424	NO ASM	ASM	NO ASM
XDPR14	R2418	NO ASM	ASM	ASM
XDPR16	R2416	NO ASM	ASM	ASM
XDPR19	R2420	NO ASM	ASM	ASM
XDPR20	R2421	NO ASM	ASM	ASM
XDPR17	R2417	NO ASM	ASM	ASM
XDPR18	R2419	NO ASM	ASM	ASM
XDPR22	R2423	NO ASM	ASM	ASM
XDPR24	R2425	NO ASM	ASM	ASM
XDPR25	R2426	NO ASM	ASM	ASM
XDPR26	R2427	NO ASM	ASM	ASM

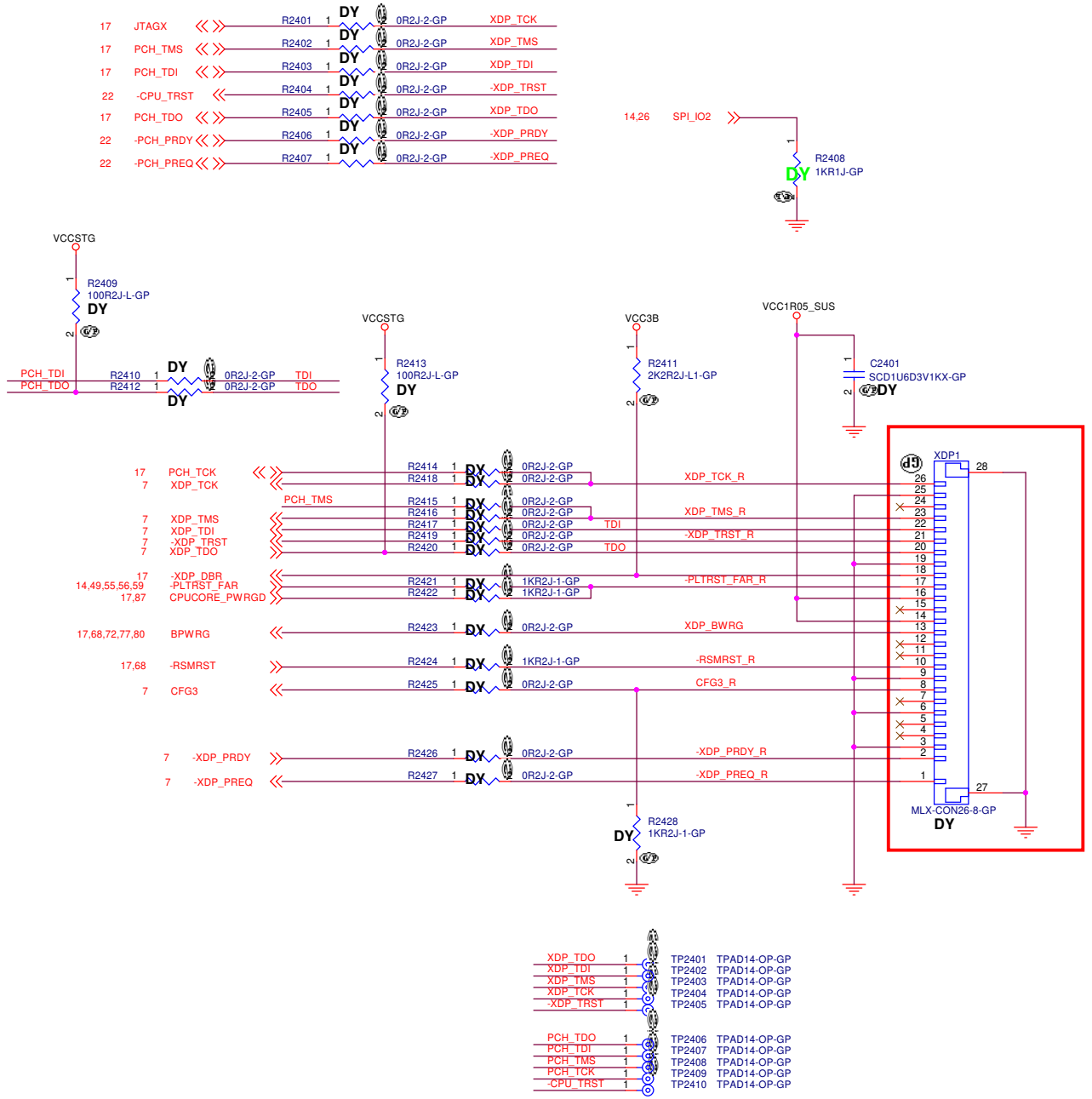
LOGIC

TABLE : PCH ITP DEBUG REPORT

		NO Use	Individual Port	DCI 2.0 w/o connector
XDPR8	R2409	NO ASM	ASM	NO ASM
XDPR21	R2422	NO ASM	ASM	NO ASM
XDPR23	R2424	NO ASM	ASM	NO ASM
XDPR13	R2414	NO ASM	ASM	NO ASM
XDPR15	R2415	NO ASM	ASM	NO ASM
XDPR9	R2410	NO ASM	ASM	NO ASM
XDPR10	R2412	NO ASM	ASM	NO ASM

LOGIC

PCHR31	R1711	NO ASM	ASM	NO ASM
PCHR32	R1712	NO ASM	ASM	NO ASM
PCHR33	R1713	NO ASM	ASM	NO ASM



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP CONNECTOR***

Size	Document Number	Rev
A3	LPM-2	-1

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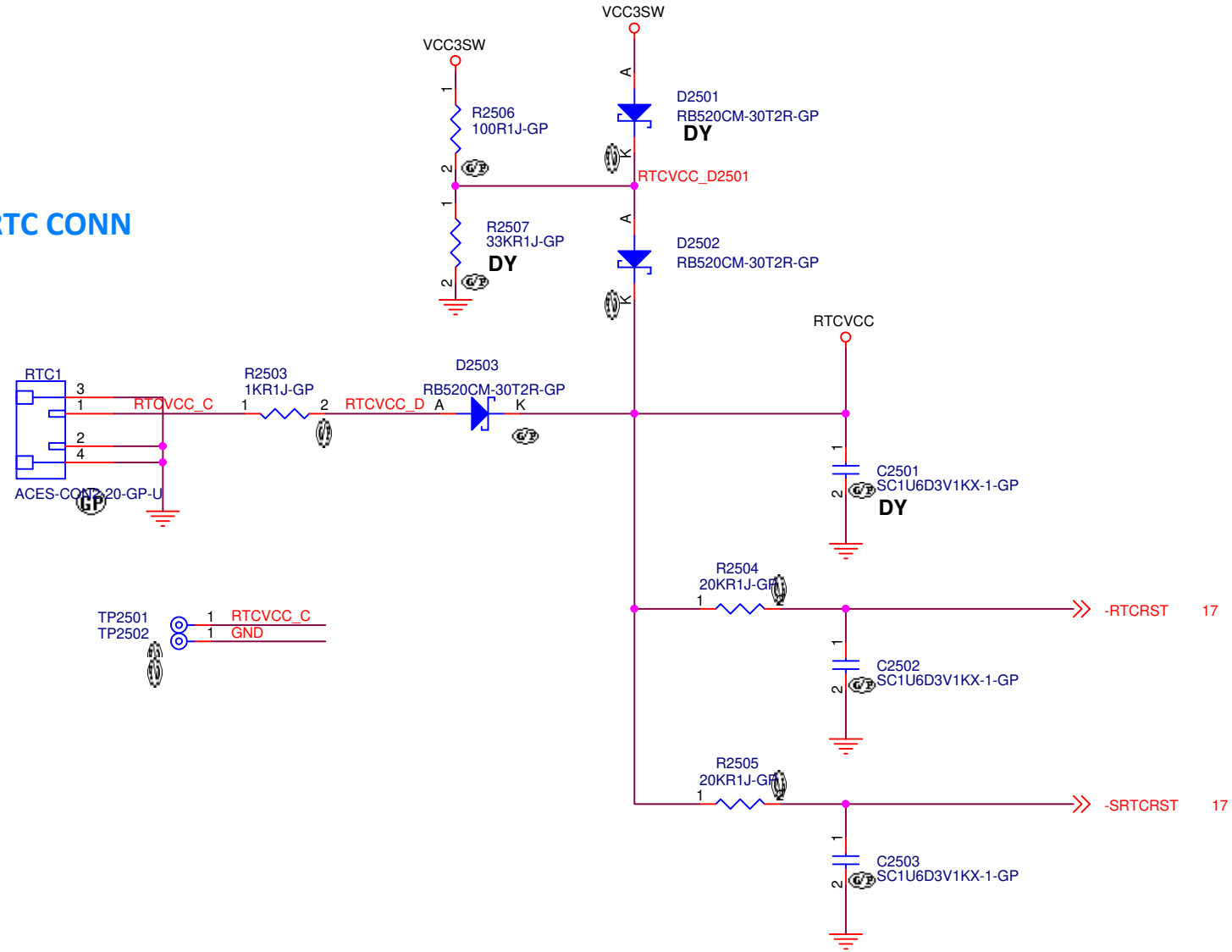
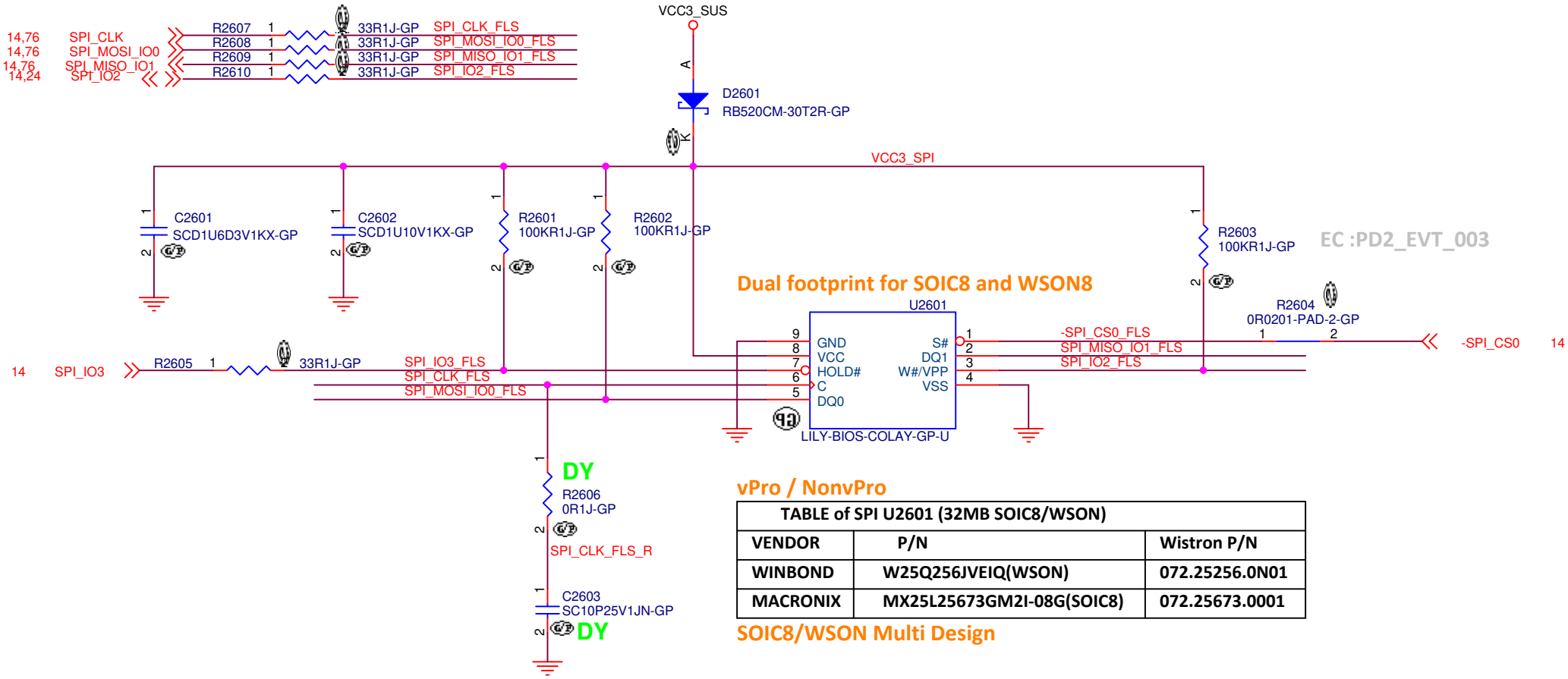
RTC

RTC CONN



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTC BATTERY***		
Size: A4	Document Number: **LPM-2**	Rev: **-1**
Date: Tuesday, April 30, 2019	Sheet 25 of 111	



vPro / NonvPro

TABLE of SPI U2601 (32MB SOIC8/WSON)		
VENDOR	P/N	Wistron P/N
WINBOND	W25Q256JVEIQ(WSON)	072.25256.0N01
MACRONIX	MX25L25673GM2I-08G(SOIC8)	072.25673.0001

SOIC8/WSON Multi Design

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SPI FLASH**

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 26 of 111

Reserved

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

Size	Document Number	Rev
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Date: Tuesday, April 30, 2019 Sheet 27 of 111

Reserved

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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Date: Tuesday, April 30, 2019 Sheet 28 of 111

Reserved

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Reserved***	
Size A4	Document Number **LPM-2**	Rev **-1**
Date: Tuesday, April 30, 2019	Sheet 29 of 111	

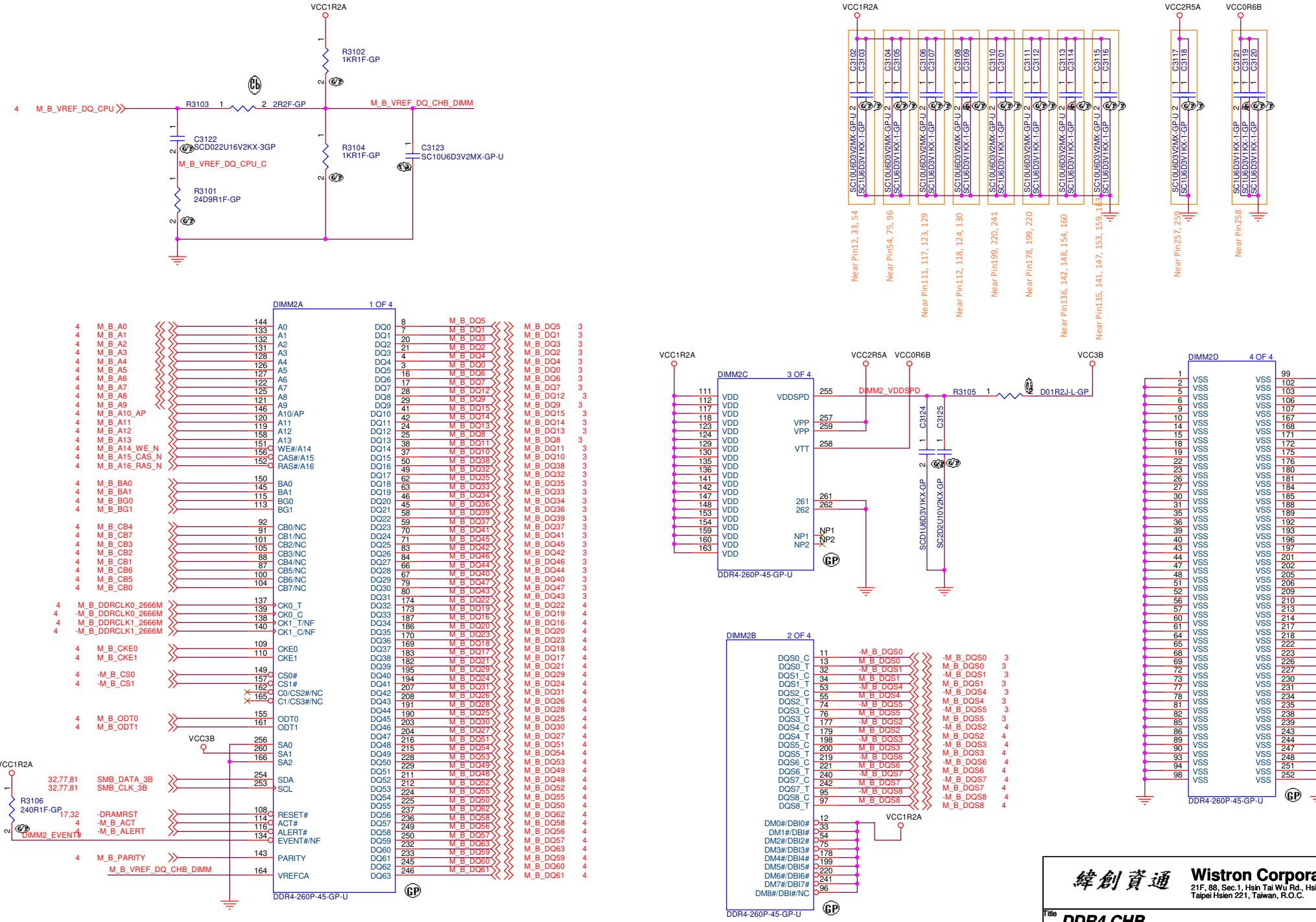
Reserved

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 30 of 111



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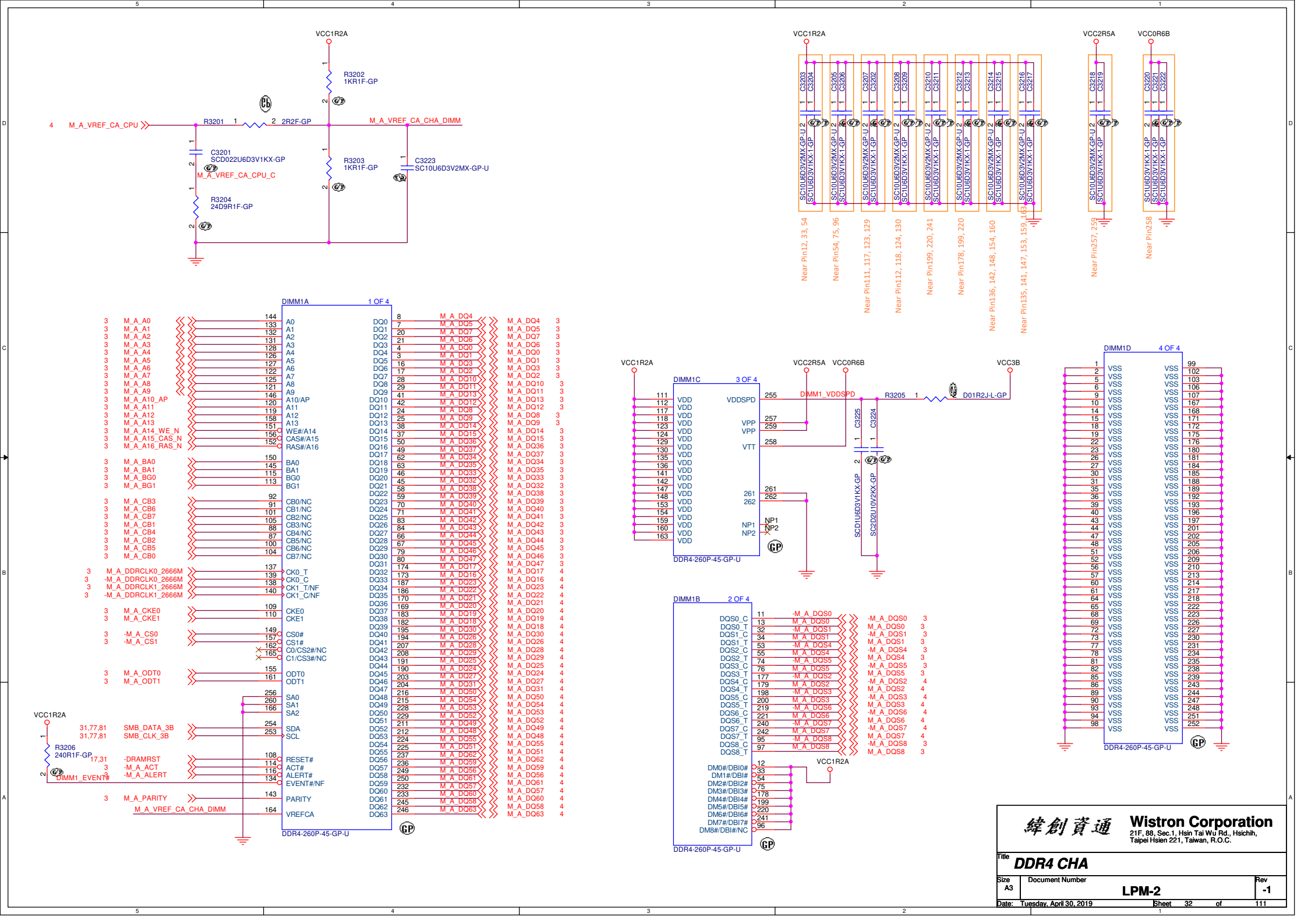
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR4 CHB			
Size: A3	Document Number: LPM-2		Rev: -1
Date: Tuesday, April 30, 2019		Sheet 31 of 111	


VCC1R2A
R3202
1KR1F-GP
M_A_VREF_CA_CPU
R3201
2R2F-GP
M_A_VREF_CA_CHA_DIMM
C3201
SCD022U6D3V1KX-GP
M_A_VREF_CA_CPU_C
R3203
1KR1F-GP
C3223
SC10U6D3V2MX-GP-U
R3204
24D9R1F-GP
VCC1R2A
VCC2R5A
VCC0R6B
C3203
C3204
C3205
C3206
C3207
C3208
C3209
C3210
C3211
C3212
C3213
C3214
C3215
C3216
C3217
C3218
C3219
C3220
C3221
C3222
SC10U6D3V2MX-GP-U
SC10U6D3V1KX-1-GP
Near Pin12, 33, 54
Near Pin54, 75, 96
Near Pin111, 117, 123, 129
Near Pin112, 118, 124, 130
Near Pin199, 220, 241
Near Pin178, 199, 220
Near Pin136, 142, 148, 154, 160
Near Pin135, 141, 147, 153, 159, 163
Near Pin257, 259
Near Pin258
DIMM1A
1 OF 4
DDR4-260P-45-GP-U
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10_AP
M_A_A11
M_A_A12
M_A_A13
M_A_A14_WE_N
M_A_A15_CAS_N
M_A_A16_RAS_N
M_A_BA0
M_A_BA1
M_A_BG0
M_A_BG1
M_A_CB3
M_A_CB6
M_A_CB7
M_A_CB1
M_A_CB4
M_A_CB2
M_A_CB5
M_A_CB0
M_A_DDRCLK0_2666M
-M_A_DDRCLK0_2666M
M_A_DDRCLK1_2666M
-M_A_DDRCLK1_2666M
M_A_CKE0
M_A_CKE1
-M_A_CS0
-M_A_CS1
M_A_ODT0
M_A_ODT1
M_A_PARITY
M_A_VREF_CA_CHA_DIMM
M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
M_A_DQ6
M_A_DQ7
M_A_DQ8
M_A_DQ9
M_A_DQ10
M_A_DQ11
M_A_DQ12
M_A_DQ13
M_A_DQ14
M_A_DQ15
M_A_DQ16
M_A_DQ17
M_A_DQ18
M_A_DQ19
M_A_DQ20
M_A_DQ21
M_A_DQ22
M_A_DQ23
M_A_DQ24
M_A_DQ25
M_A_DQ26
M_A_DQ27
M_A_DQ28
M_A_DQ29
M_A_DQ30
M_A_DQ31
M_A_DQ32
M_A_DQ33
M_A_DQ34
M_A_DQ35
M_A_DQ36
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M_A_DQ38
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M_A_DQ40
M_A_DQ41
M_A_DQ42
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M_A_DQ45
M_A_DQ46
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M_A_DQ48
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M_A_DQ54
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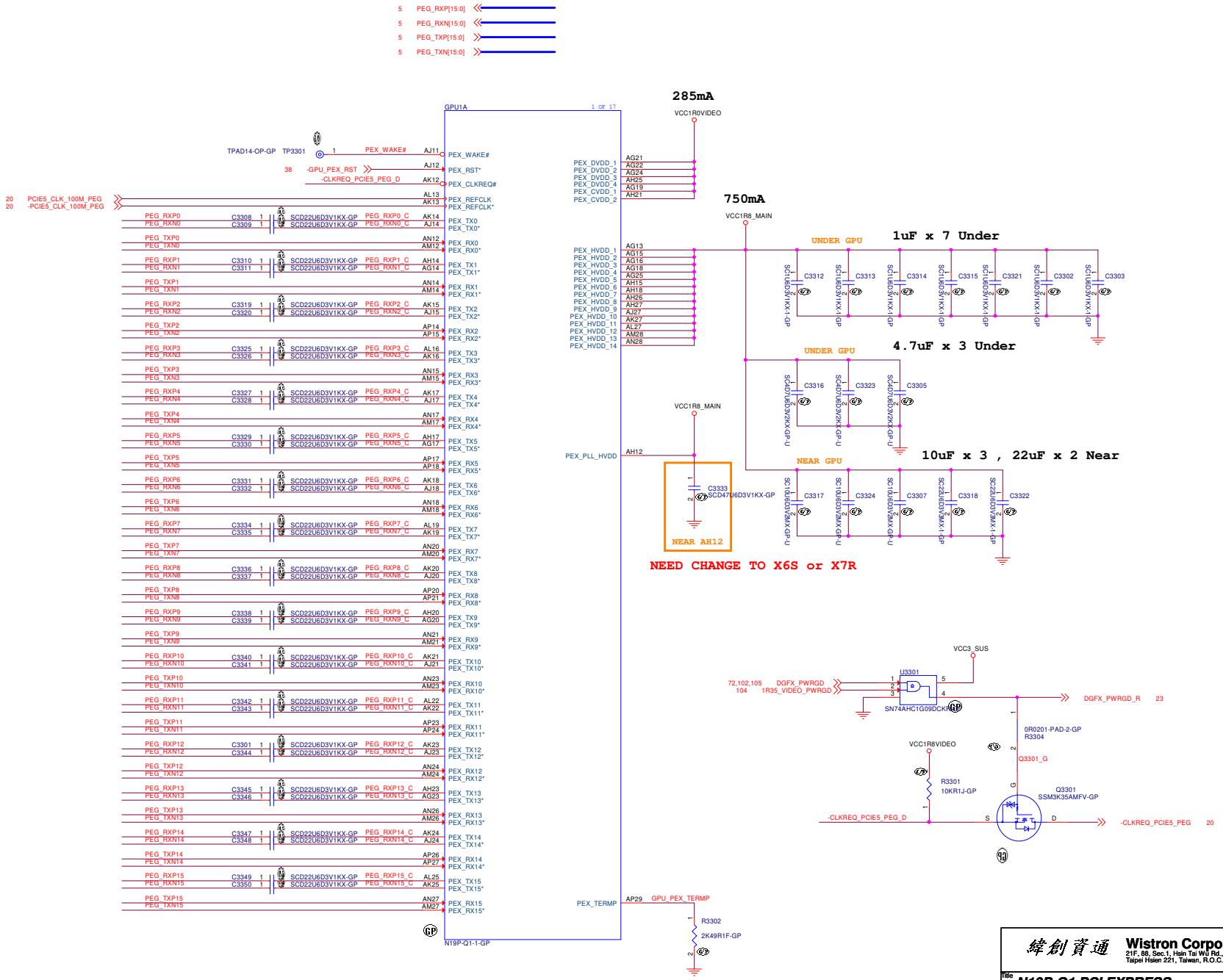
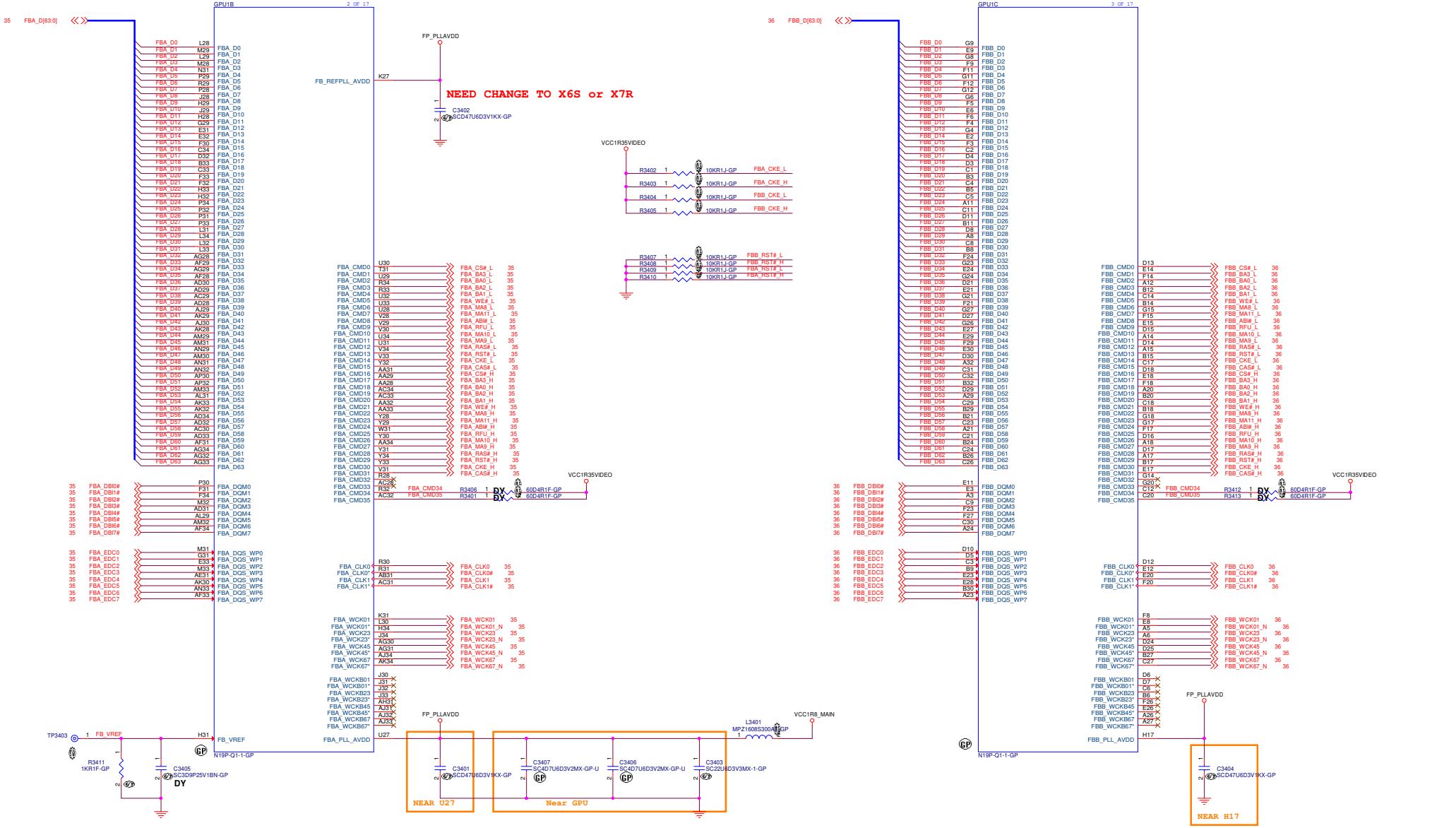
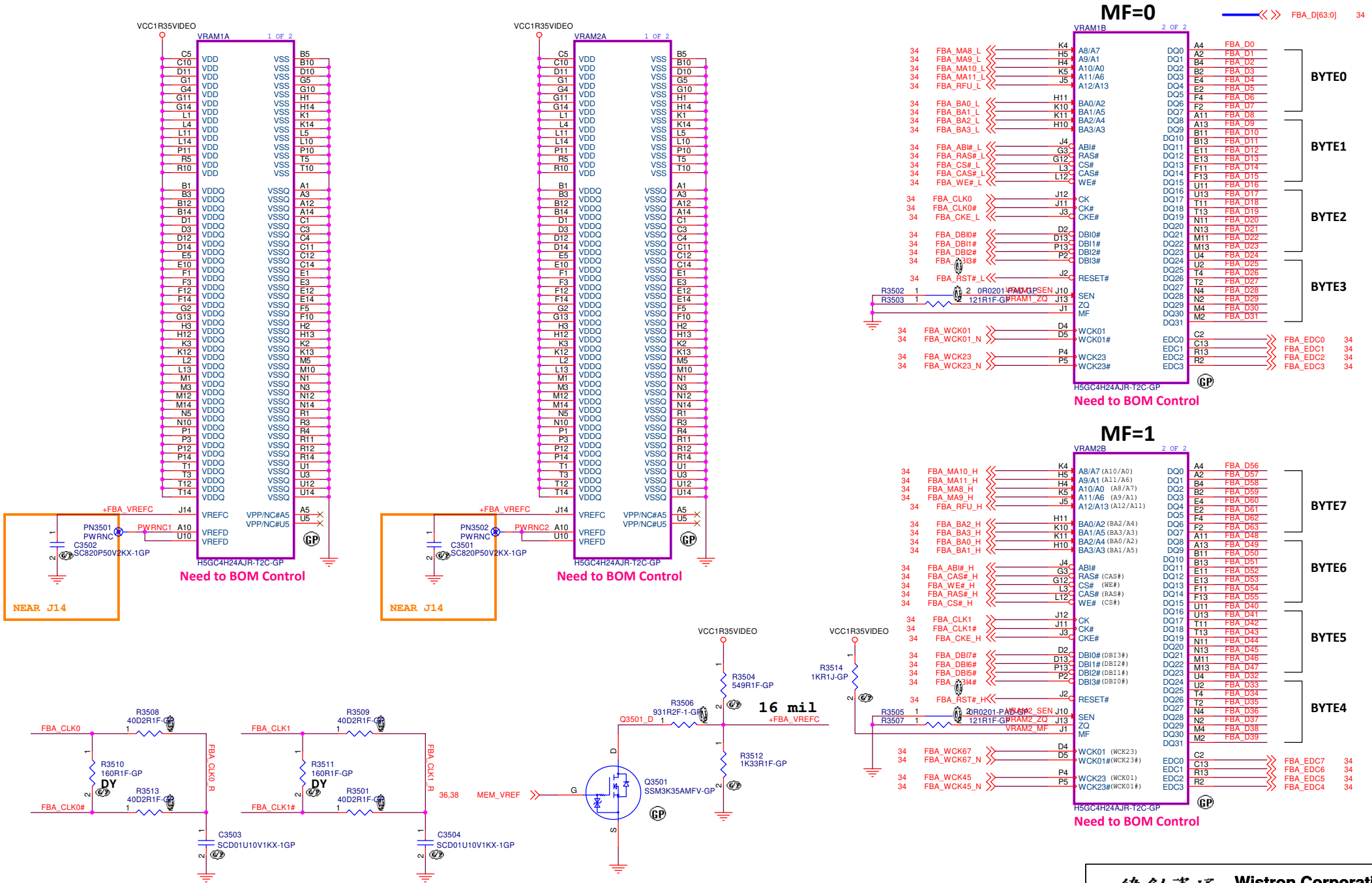
M_A_DQ56
M_A_DQ57
M_A_DQ58
M_A_DQ59
M_A_DQ60
M_A_DQ61
M_A_DQ62
M_A_DQ63
VCC1R2A
R3206
240R1F-GP
SMB_DATA_3B
SMB_CLK_3B
-DRAMRST
-M_A_ACT
-M_A_ALERT
DIMM1_EVENT#
VCC1R2A
VCC2R5A
VCC0R6B
VCC3B
DIMM1C
3 OF 4
DDR4-260P-45-GP-U
VDDSPD
VPP
VTT
NP1
NP2
DIMM1_VDDSPD
R3205
D01R2J-L-GP
C3225
C3224
SCD1U6D3V1KX-GP
SC2D2U10V2KX-GP
DIMM1B
2 OF 4
DDR4-260P-45-GP-U
-M_A_DQS0
M_A_DQS0
-M_A_DQS1
M_A_DQS1
-M_A_DQS4
M_A_DQS4
-M_A_DQS5
M_A_DQS5
-M_A_DQS2
M_A_DQS2
-M_A_DQS3
M_A_DQS3
-M_A_DQS6
M_A_DQS6
-M_A_DQS7
M_A_DQS7
-M_A_DQS8
M_A_DQS8
DM0#/DBI0#
DM1#/DBI#
DM2#/DBI2#
DM3#/DBI3#
DM4#/DBI4#
DM5#/DBI5#
DM6#/DBI6#
DM7#/DBI7#
DM8#/DBI#/NC
VCC1R2A
DIMM1D
4 OF 4
DDR4-260P-45-GP-U
VSS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR4 CHA
Size
A3
Document Number
LPM-2
Rev
-1
Date: Tuesday, April 30, 2019
Sheet 32 of 111

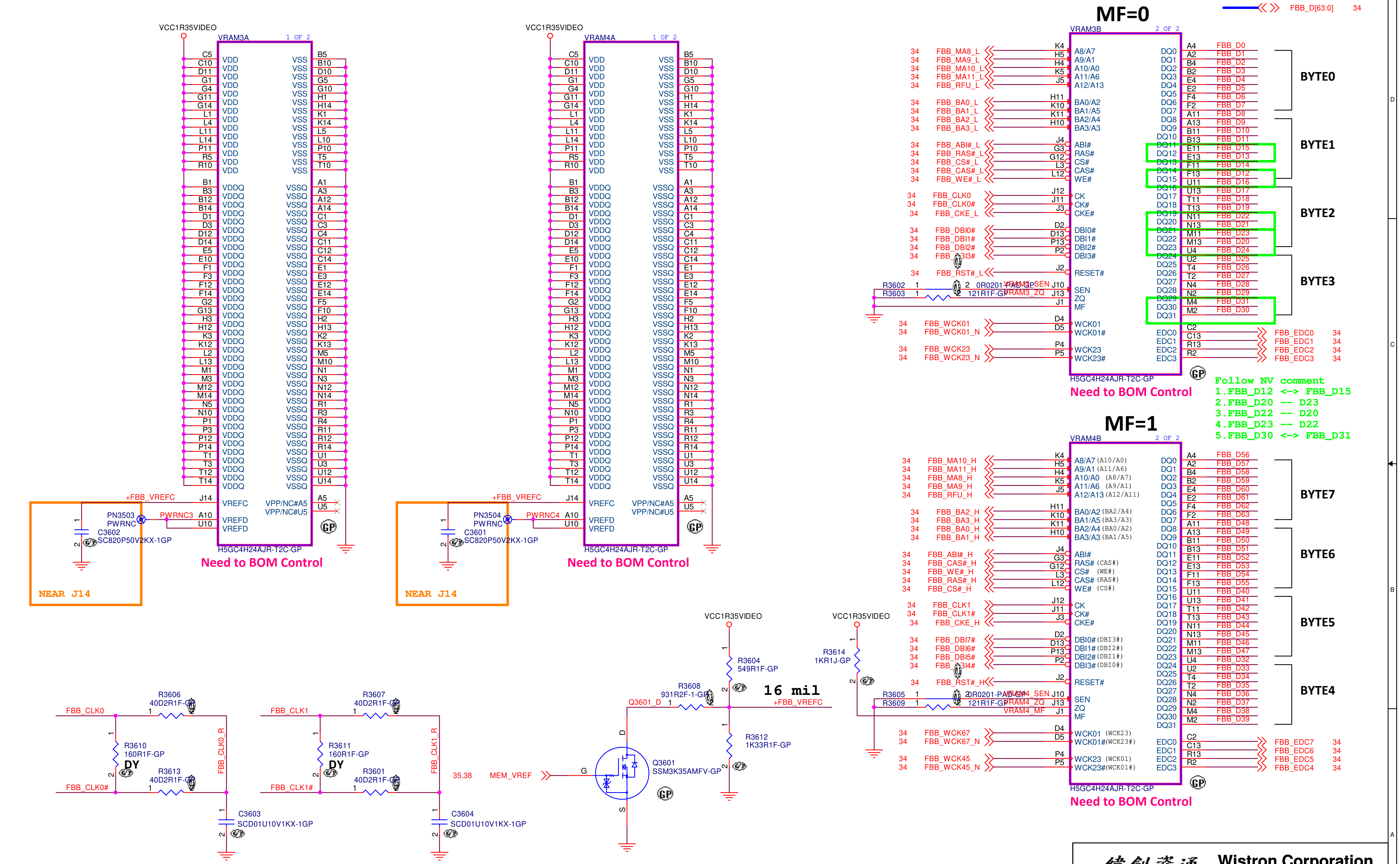


Wistron Corporation	Title: N19P-Q1 PCI EXPRESS		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size: Custom	Document Number: LPM-2	Rev: -1
	Date: Tuesday, April 30, 2019	Sheet 33 of 111	



緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	N19P-Q1 FB A/B	
Size A2	Document Number LPM-2	Rev -1
Date: Tuesday, April 30, 2019	Sheet 34 of 111	


MF=0
MF=1
VRAM1A
VRAM2A
VRAM1B
VRAM2B
H5GC4H24AJR-T2C-GP
Need to BOM Control
NEAR J14
BYTE0
BYTE1
BYTE2
BYTE3
BYTE4
BYTE5
BYTE6
BYTE7
16 mil
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
N19P-Q1 VRAM CH-A
LPM-2
Tuesday, April 30, 2019



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **N19P-Q1 VRAM CH-B**

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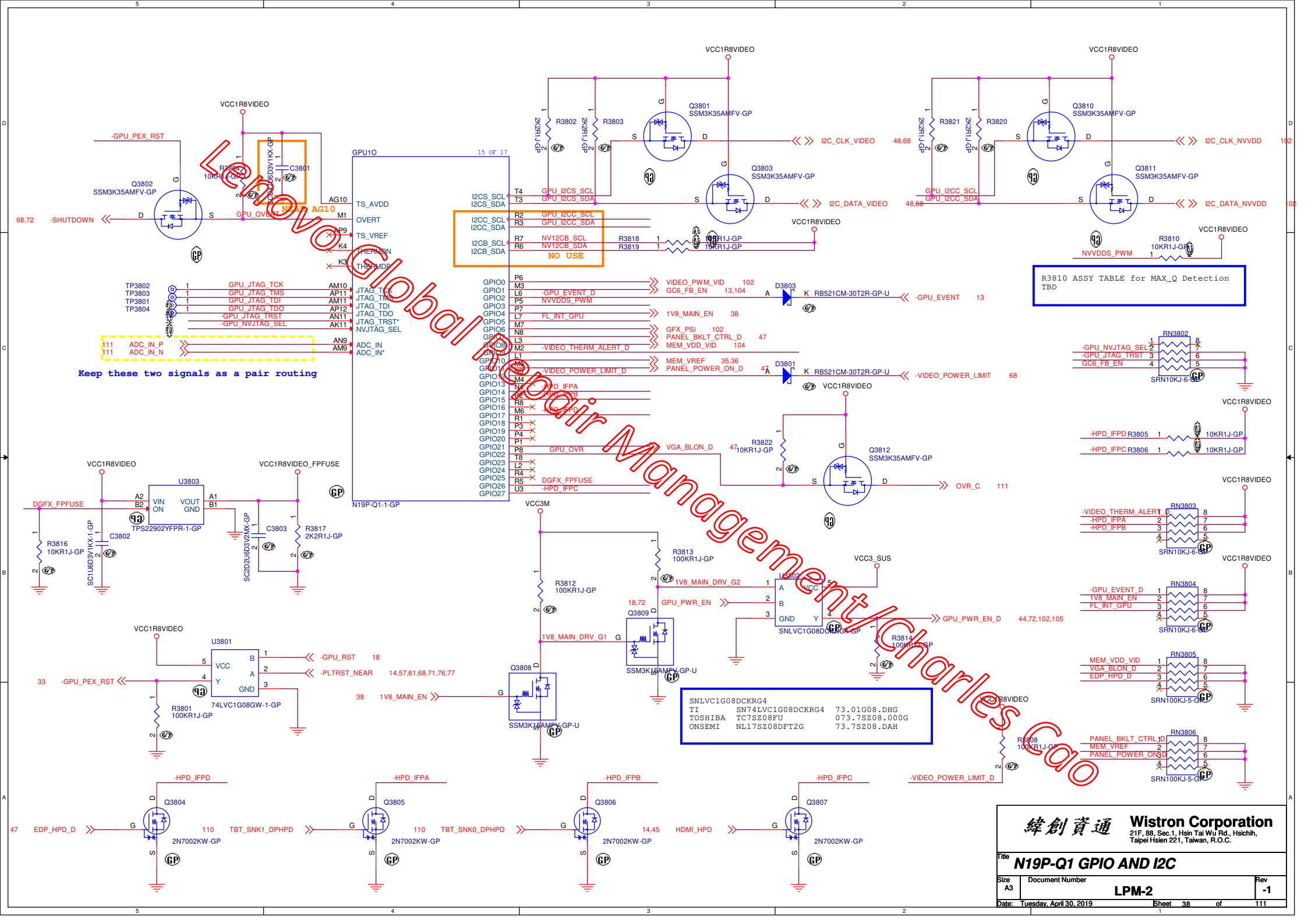
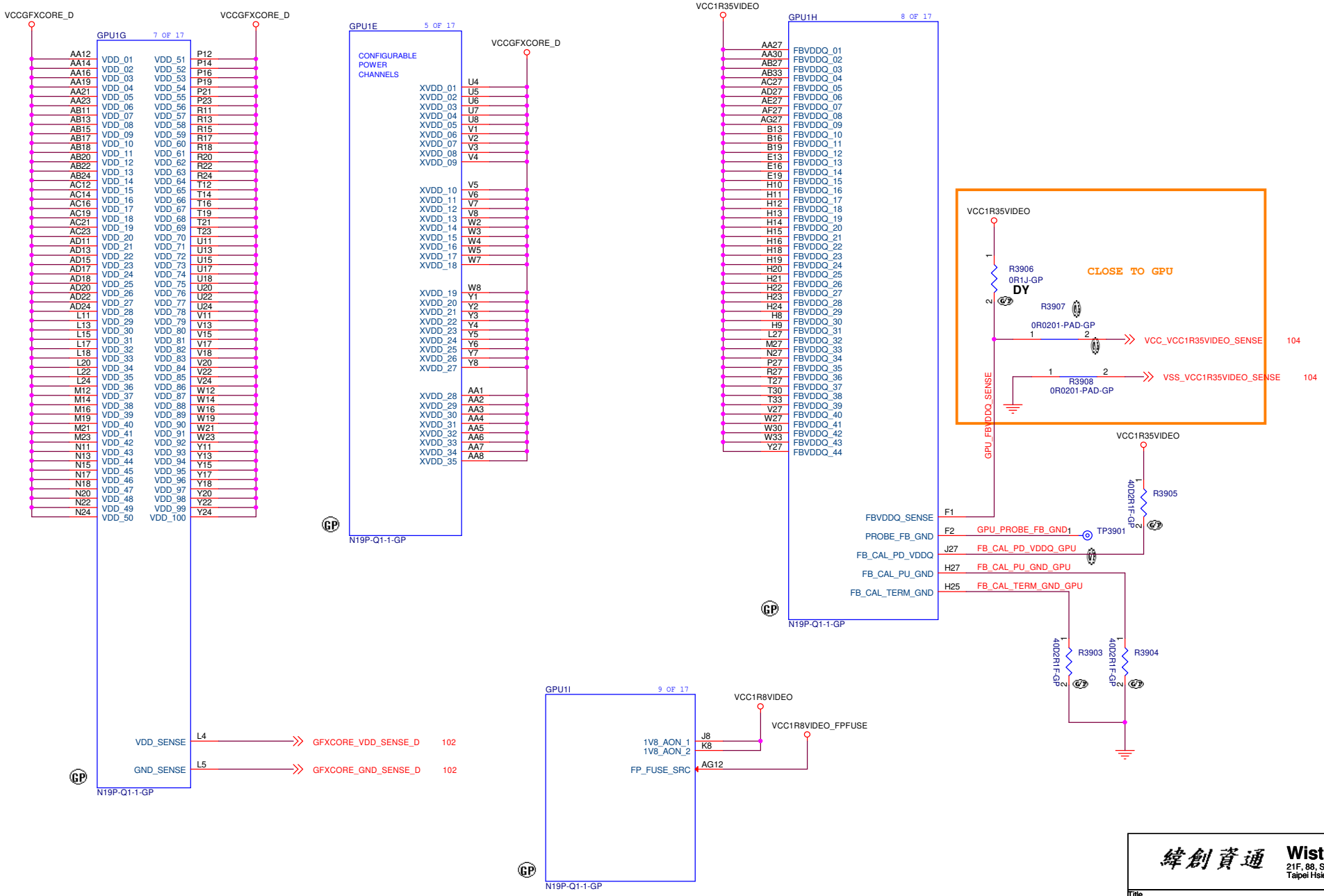
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **N19P-Q1 VRAM DECOUPING**

Size	Document Number	Rev
A2	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 57 of 111


GPU1O
N19P-Q1-1-GP
15 OF 17
NEAR AG10
NO USE
Keep these two signals as a pair routing
R3810 ASSY TABLE for MAX_Q Detection
TBD
SNLVC1G08DCKRG4
TI SN74LVC1G08DCKRG4 73.01G08.DHG
TOSHIBA TC7SZ08FU 073.7SZ08.000G
ONSEMI NL17SZ08DFT2G 73.7SZ08.DAH
Lenovo Global Repair Management/Charles Cao
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N19P-Q1 GPIO AND I2C
Size A3
Document Number LPM-2
Rev -1
Date: Tuesday, April 30, 2019
Sheet 38 of 111

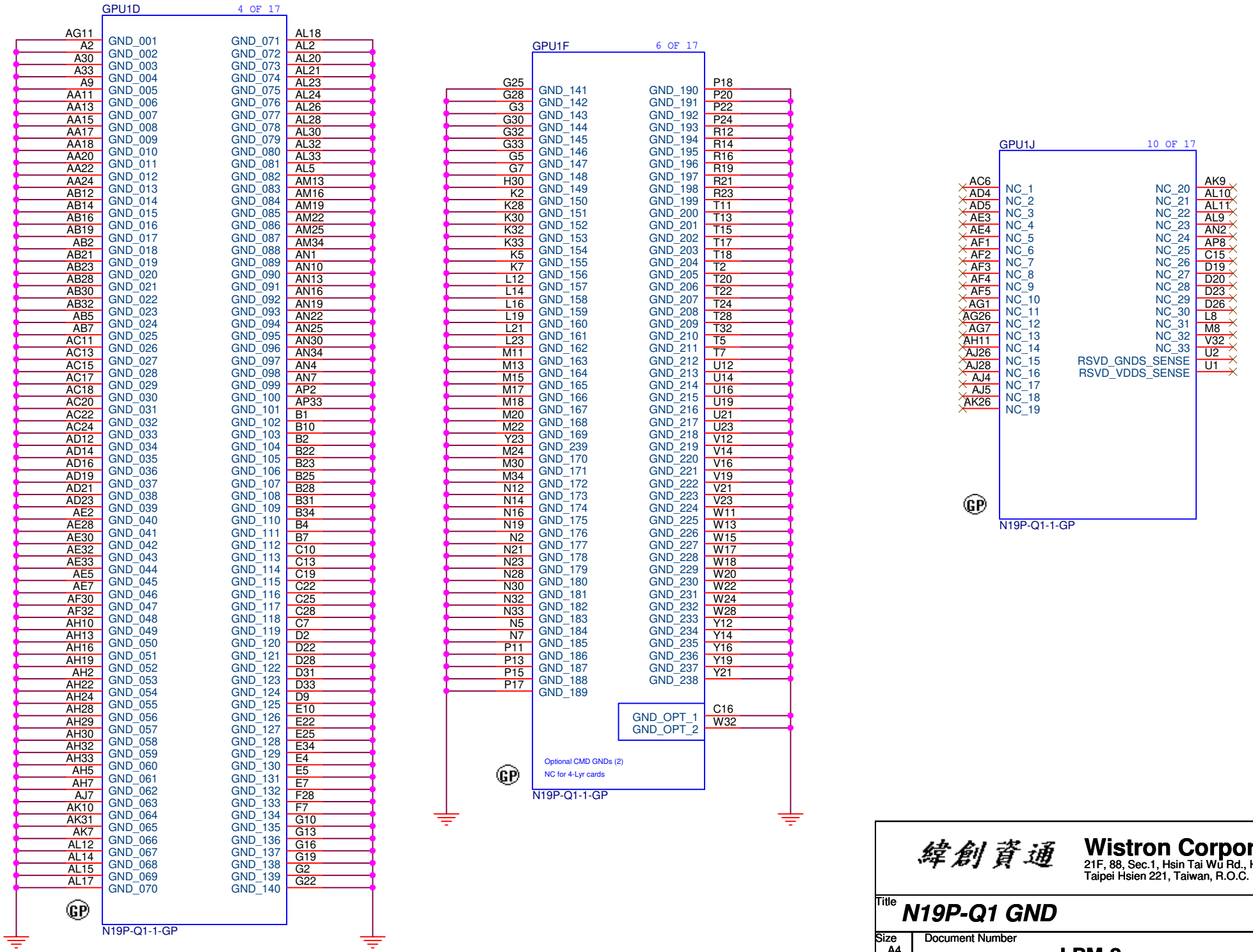


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N19P-Q1 POWER

Size	Document Number	Rev
A3	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 39 of 111



緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N19P-Q1 GND***

Size	Document Number	Rev
A4	**LPM-2**	-1

Date: Tuesday, April 30, 2019 Sheet 40 of 111

VCC1R35VIDEO

For FBVDDQ

UNDER GPU — 1uF x 12 Under

C4102 C4103 C4104 C4105 C4106 C4107

UNDER GPU

C4115 C4116 C4117 C4118 C4119 C4120

UNDER GPU — 10uF x 4 Under

C4135 C4136 C4137 C4138

NEAR GPU — 10uF x 2 Near

C4153 C4154

NEAR GPU — 22uF x 5 Near

C4163 C4164 C4165 C4166 C4167

VCCGFXCORE_D

For NVVDD

Place near to GPU — 22uF x 15 Near

C4121 C4122 C4123 C4124 C4125 C4126 C4127

Place near to GPU

C4139 C4140 C4141 C4142 C4143 C4157 C4158 C4159

VCC1R0VIDEO

For PEX_DVDD

UNDER GPU — 1uF x 6 Under

C4174 C4175 C4176 C4177 C4155 C4156

UNDER GPU — 4.7uF x 3 Under

C4190 C4191 C4192

NEAR GPU — 10uF x 3 , 22uF x 2 Near

C41A3 C41A4 C41A5 C4193 C4194

VCC1R8VIDEO

For 1V8_AON

4.7uF x 3 , 1uF x 3 Near — 0.47uF x 4 Under

C4101 C4178 C4179 C4180 C4196 C4197 C4198 C4199 C41A1 C41A2

Need Change X6S or X7R

VCCGFXCORE_D

For NVVDD

Place under to GPU — 10uF x 34 Under

C4108 C4109 C4110 C4111 C4112 C4113 C4114

Place under to GPU

C4128 C4129 C4130 C4131 C4132 C4133 C4134

Place under to GPU

C4144 C4145 C41A7 C41A6 C41A8 C41A9 C41A10

Place under to GPU

C4146 C4147 C4148 C4149 C4150 C4151 C4152

Place under to GPU

C4160 C4161 C4162 C4168 C4169 C4170

Place under to GPU — 1uF x 13 Under

C4171 C4172 C4173 C4181 C4182 C4183 C4195

Place under to GPU

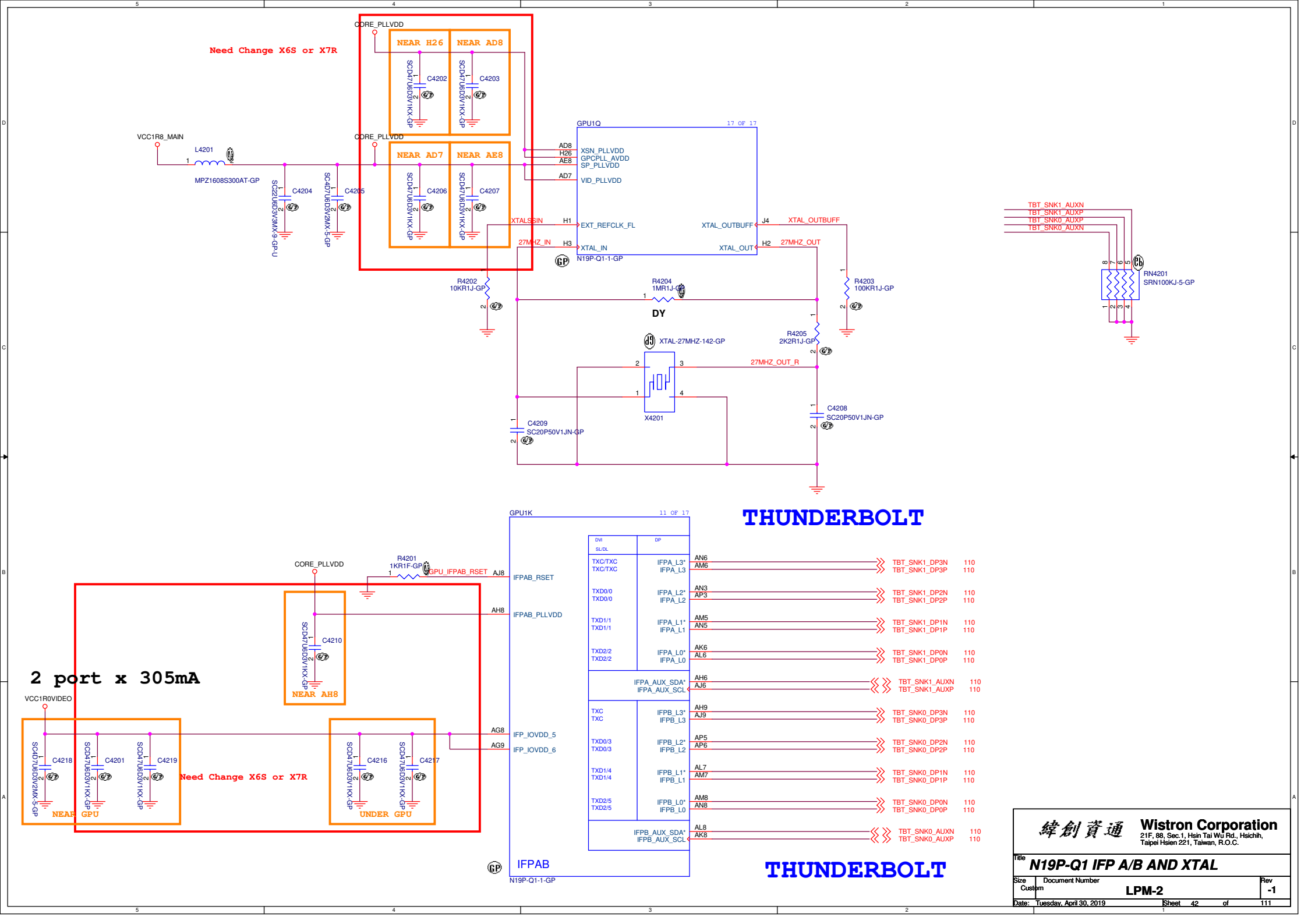
C4184 C4185 C4186 C4187 C4188 C4189

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

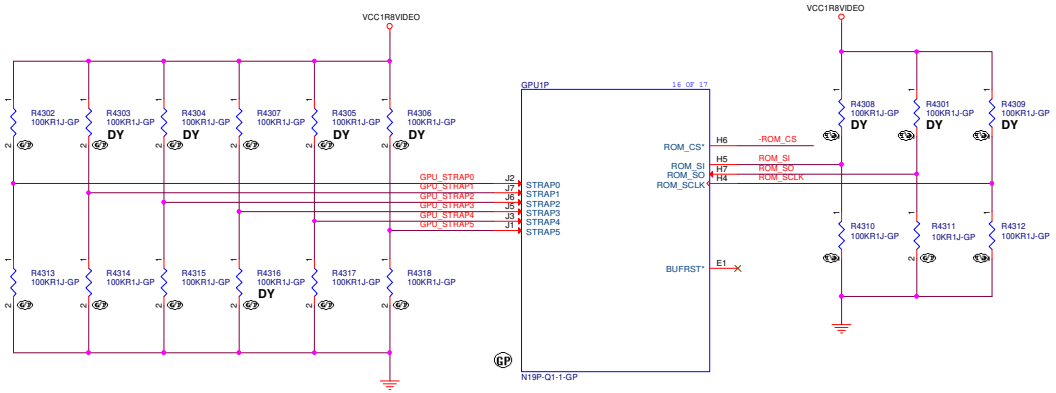
Title: N18P-Q3 DECOUPING

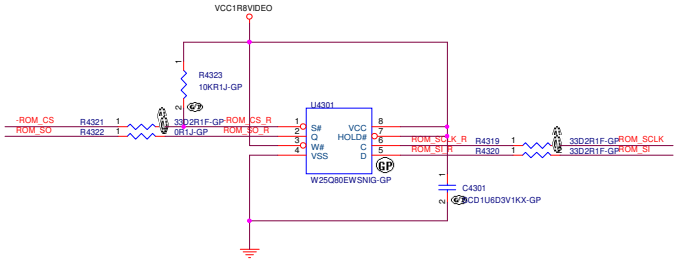
Size	Document Number	Rev
Custom	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 41 of 111



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	N19P-Q1 IFP A/B AND XTAL		
Size: Custom	Document Number: LPM-2	Rev: -1	
Date: Tuesday, April 30, 2019	Sheet 42 of 111		





Strap0 table for VRAM vendor		
Vendor	**R4302**	**R4313**
Micron MT51J256M32HF-80:B	**100K 1%**	**NO ASM**
Hynix H5GC8H24AJR-R2C	**NO ASM**	**100K 1%**

Strap1 table for VRAM vendor		
Vendor	**R4303**	**R4314**
Micron MT51J256M32HF-80:B	**NO ASM**	**100K 1%**
Hynix H5GC8H24AJR-R2C	**100K 1%**	**NO ASM**

Strap2 table for VRAM vendor		
Vendor	**R4304**	**R4315**
Micron MT51J256M32HF-80:B	**NO ASM**	**100K 1%**
Hynix H5GC8H24AJR-R2C	**NO ASM**	**100K 1%**

5.2.2.3 Assorted Configuration Straps

The following configurable characteristics of the graphics circuit share three physical strap pins:

- **SMB_ALT_ADDR Enable**: This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits. (see Section 13.3.2.1 for the SMBus address.)
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG**: This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N17x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits.

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0
No other configurations are supported.			

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

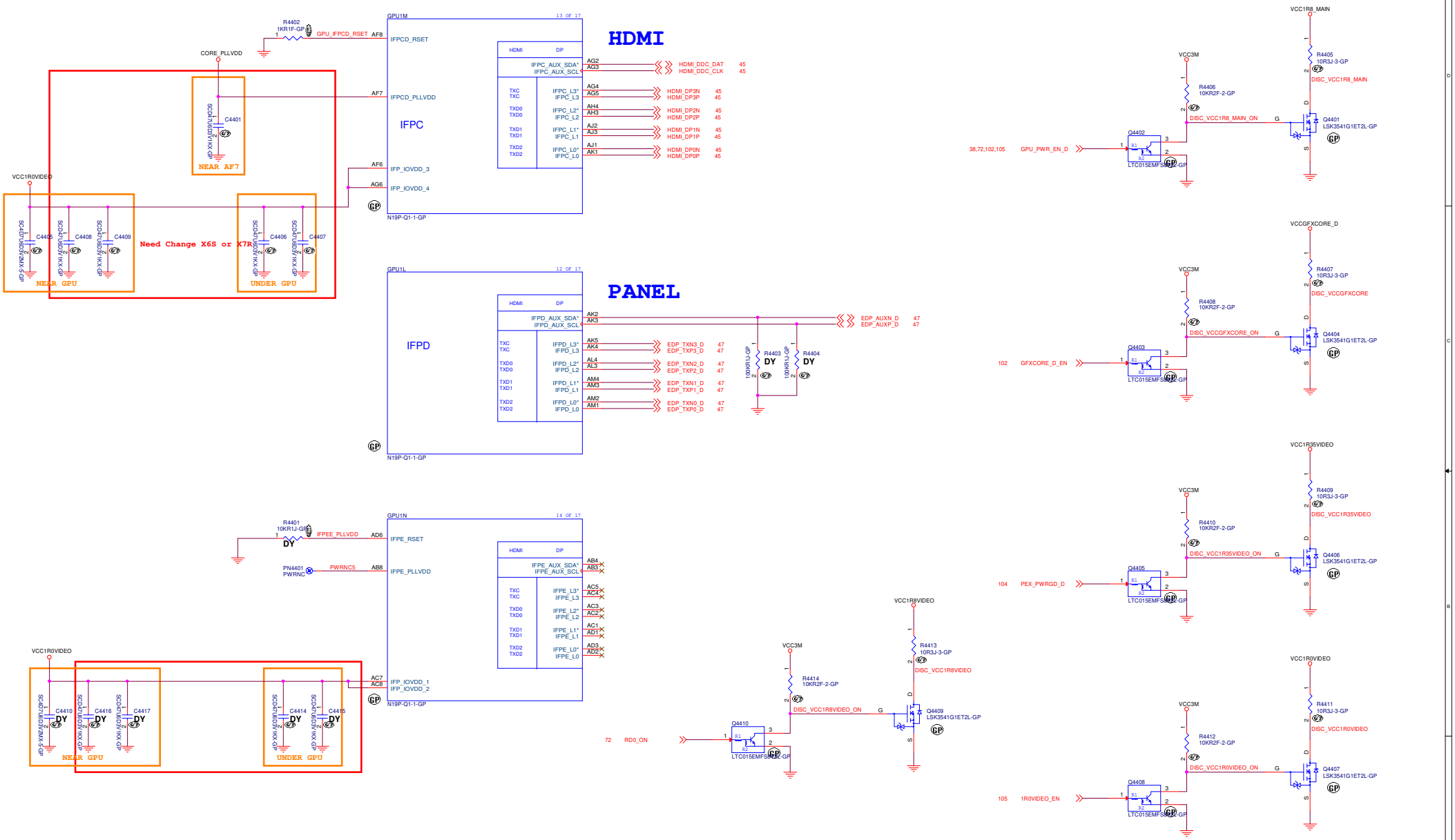
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

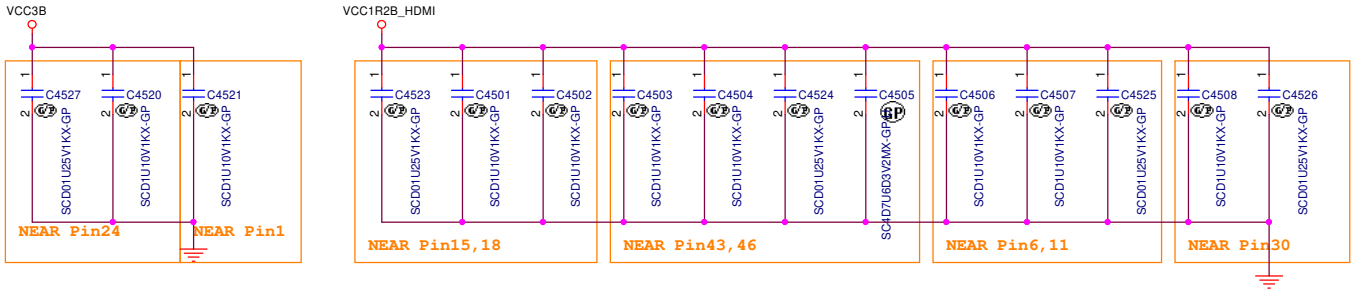
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

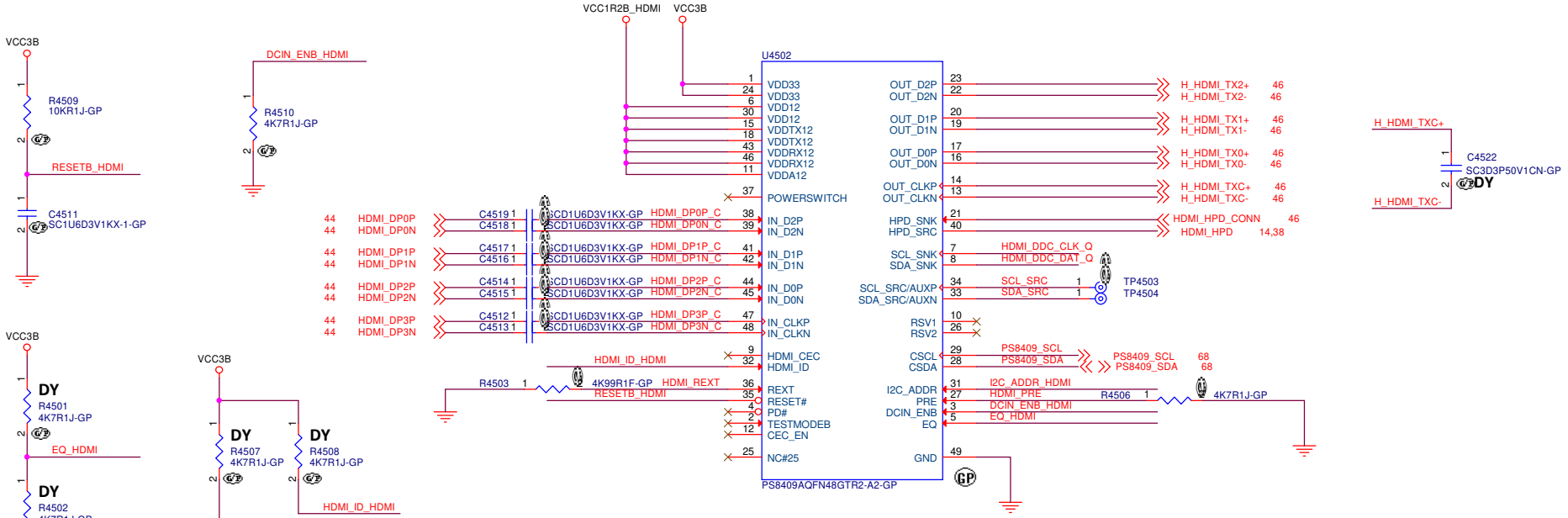
Title: N19P-Q1 MIO AND ROM
Size: A2 | Document Number: LPM-2 | Rev: -1
Date: Tuesday, April 30, 2019 | Sheet 43 of 111

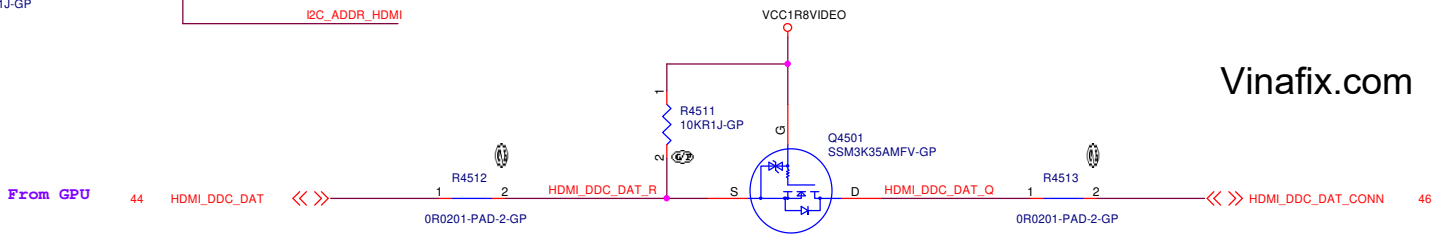


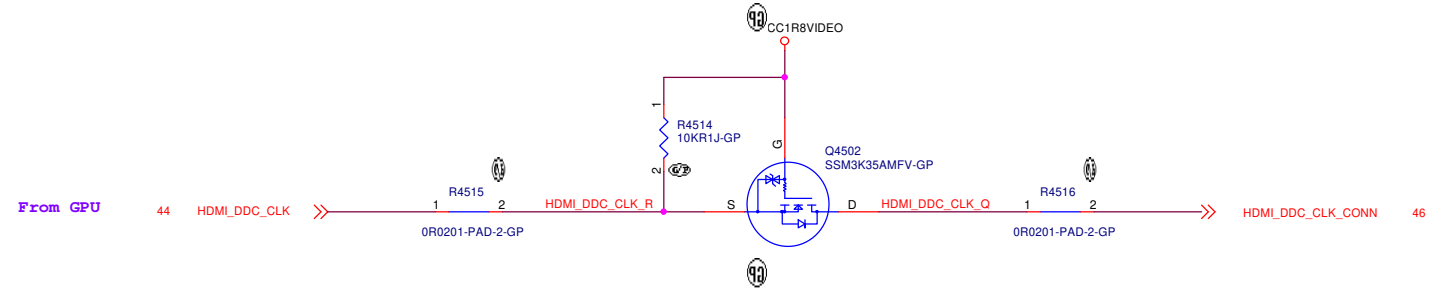
緯創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	N19P-Q1 IFP C/D AND E/F
Size: A2	Document Number: LPM-2
Rev: -1	
Date: Tuesday, April 30, 2019	Sheet 44 of 111

HDMI Re driver









緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI RE-DRIVER**

Size	Document Number	Rev
A3	LPM-2	-1

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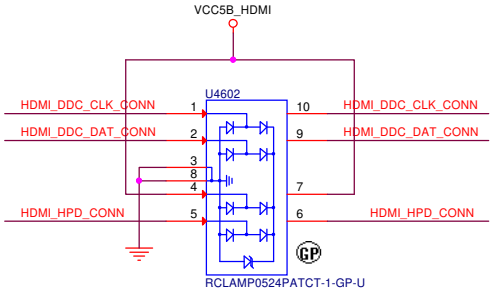
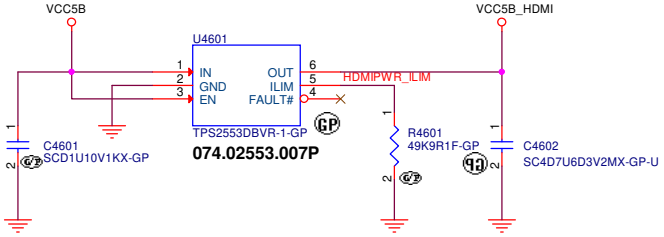
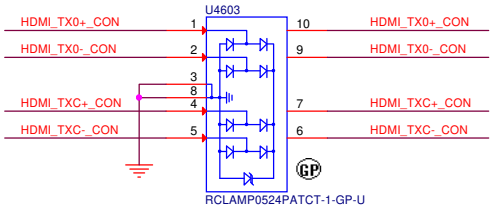
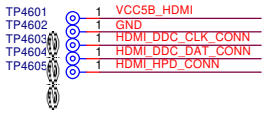
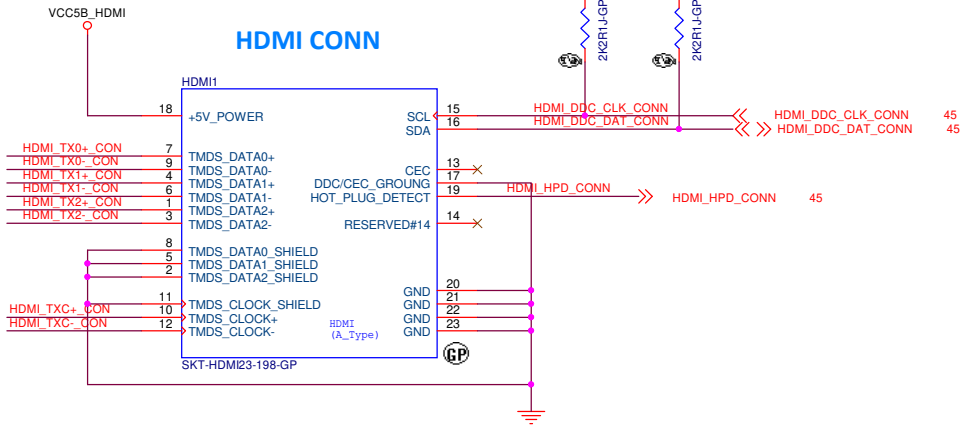
HDMI

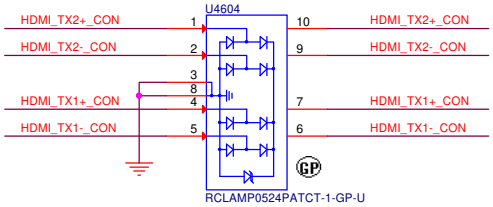


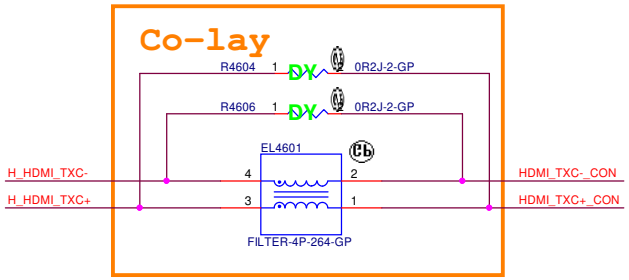


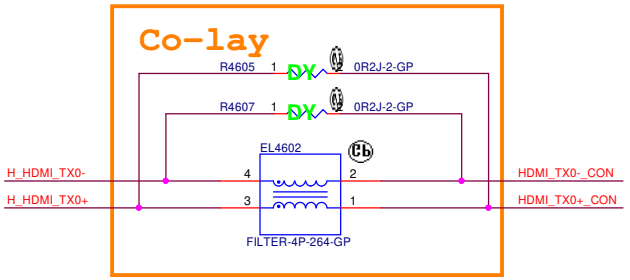


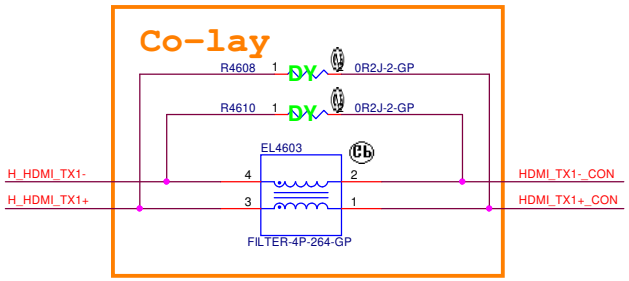


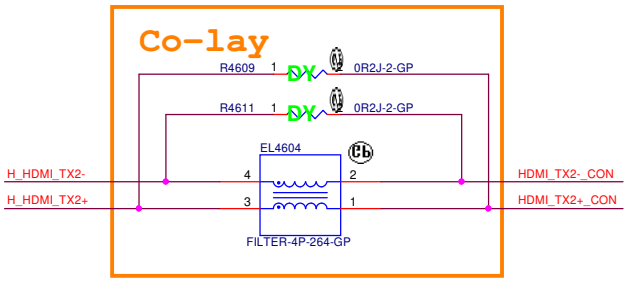












45 H_HDMI_TXC- → H_HDMI_TXC-
45 H_HDMI_TXC+ → H_HDMI_TXC+
45 H_HDMI_TX0- → H_HDMI_TX0-
45 H_HDMI_TX0+ → H_HDMI_TX0+
45 H_HDMI_TX1- → H_HDMI_TX1-
45 H_HDMI_TX1+ → H_HDMI_TX1+
45 H_HDMI_TX2- → H_HDMI_TX2-
45 H_HDMI_TX2+ → H_HDMI_TX2+

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Title: HDMI CONNECTOR

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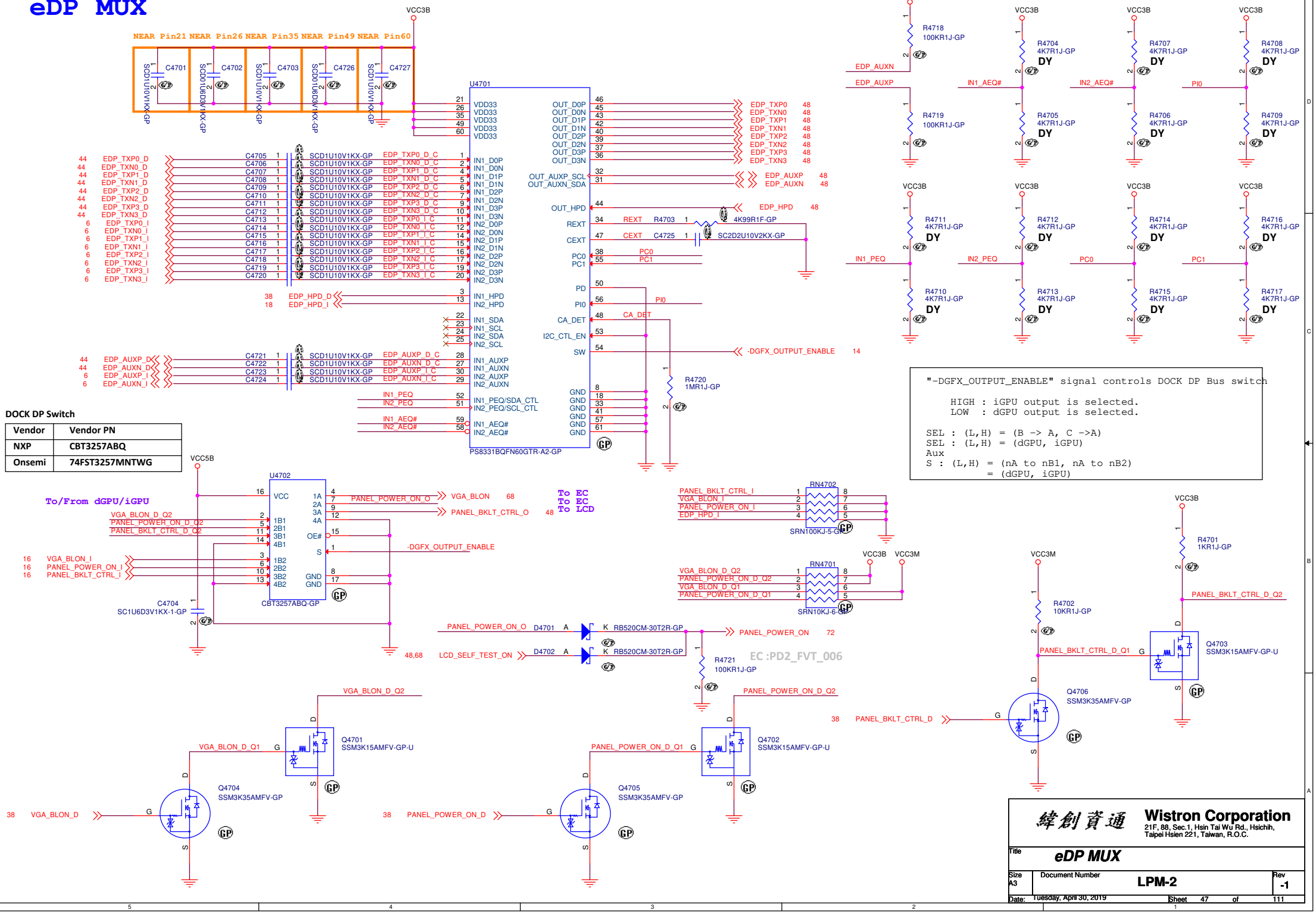
eDP MUX



DOCK DP Switch

Vendor	Vendor PN
NXP	CBT3257ABQ
Onsemi	74FST3257MNTWG

"-DGFX_OUTPUT_ENABLE" signal controls DOCK DP Bus switch

HIGH : iGPU output is selected.
LOW : dGPU output is selected.

SEL : (L,H) = (B -> A, C ->A)
SEL : (L,H) = (dGPU, iGPU)
Aux
S : (L,H) = (nA to nB1, nA to nB2)
= (dGPU, iGPU)

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Title	eDP MUX
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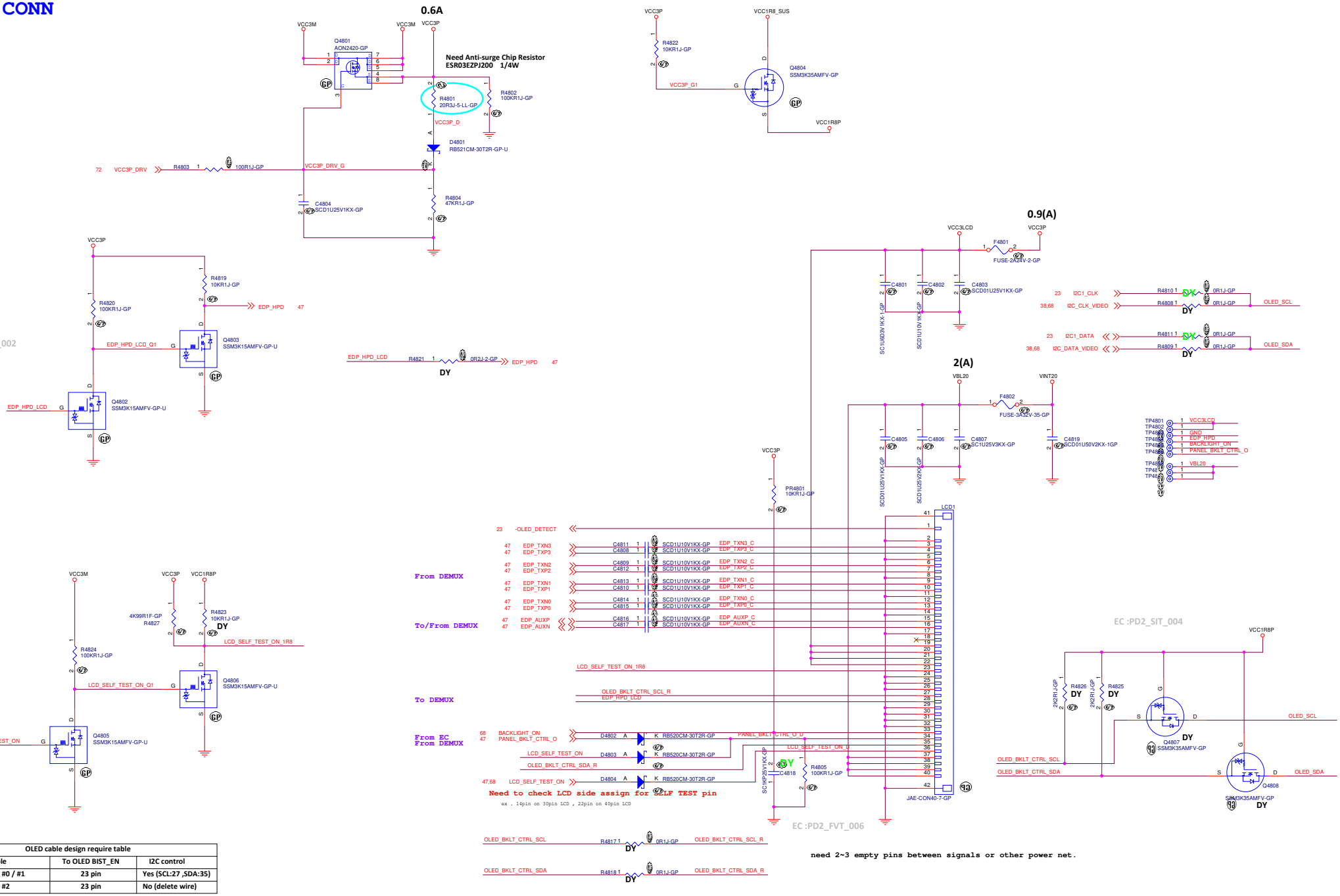
LCD CONN



OLED cable design require table		
OLED cable	To OLED BIST_EN	I2C control
For Track #0 / #1	23 pin	Yes (SCL:27 ,SDA:35)
For Track #2	23 pin	No (delete wire)

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Title: **LCD CONNECTOR**

Size	Document Number	Rev
A2	LPM-2	-1

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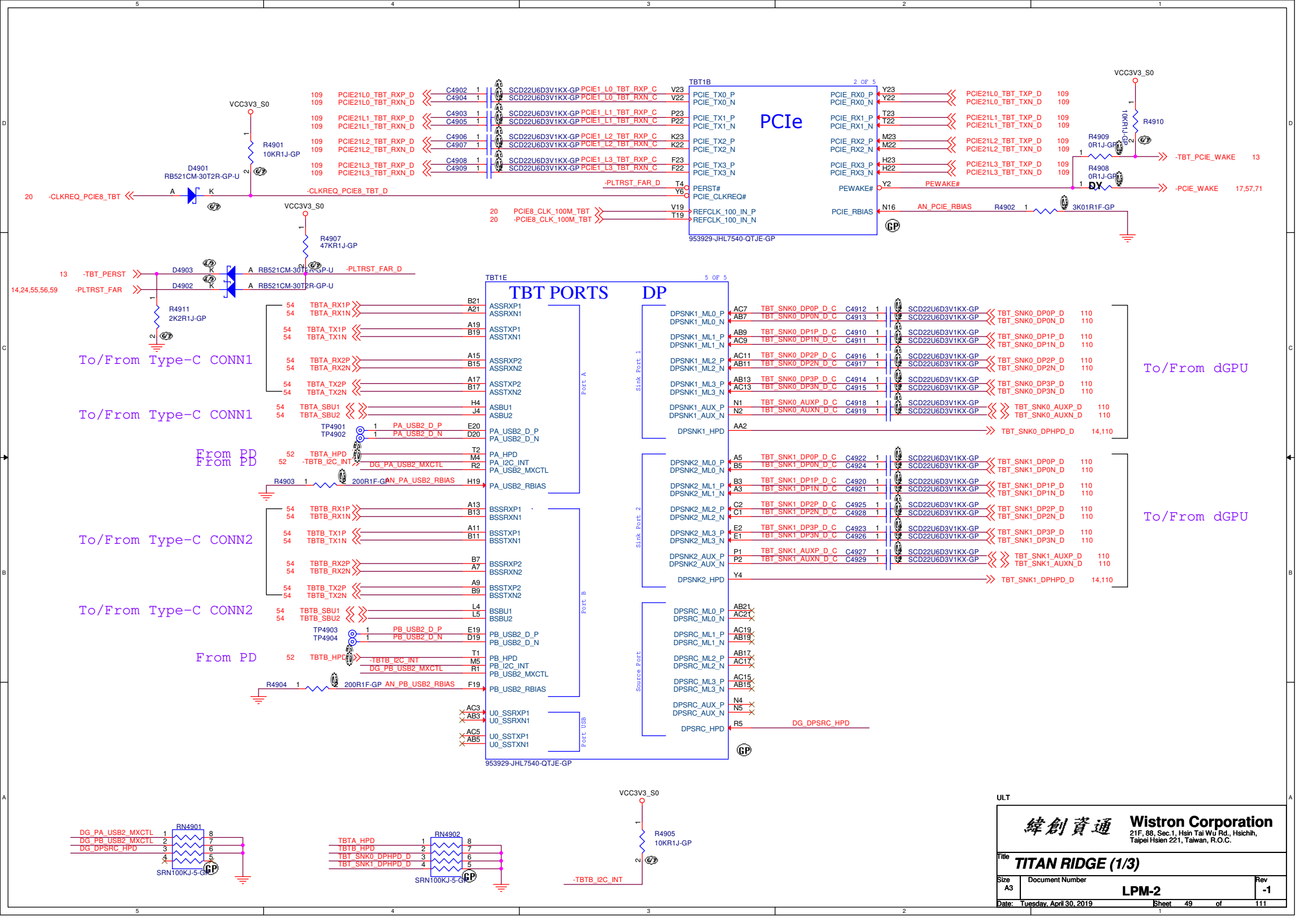
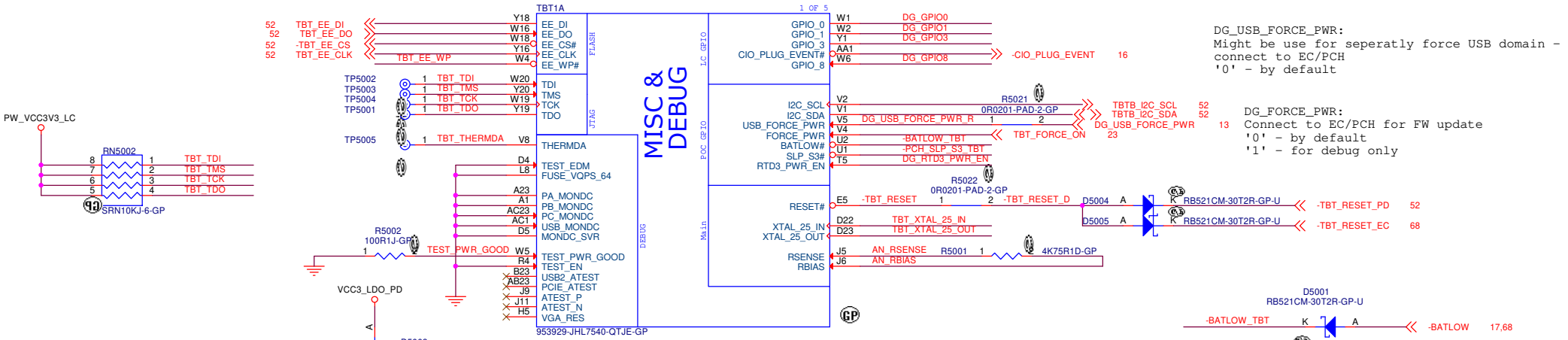


ULT

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TITAN RIDGE (1/3)		
Size: A3	Document Number: LPM-2	Rev: -1
Date: Tuesday, April 30, 2019	Sheet 49 of 111	



DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain - connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

P1

TABLE of SPI U5001		
VENDOR	P/N	Wistron P/N
WINBOND	W25Q80DVSNIG	072.25Q80.0C01
MACRONIX	MX25L8006EM1I-12G	072.25806.0A01

X1E

TABLE of SPI U5001		
VENDOR	P/N	Wistron P/N
Micron	W25Q80JVNIQ	072.25Q80.0F01
MACRONIX	MX25V8035FM1I	072.25835.0001

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TITAN RIDGE (2/3)

Size: A3 | Document Number: LPM-2 | Rev: -1

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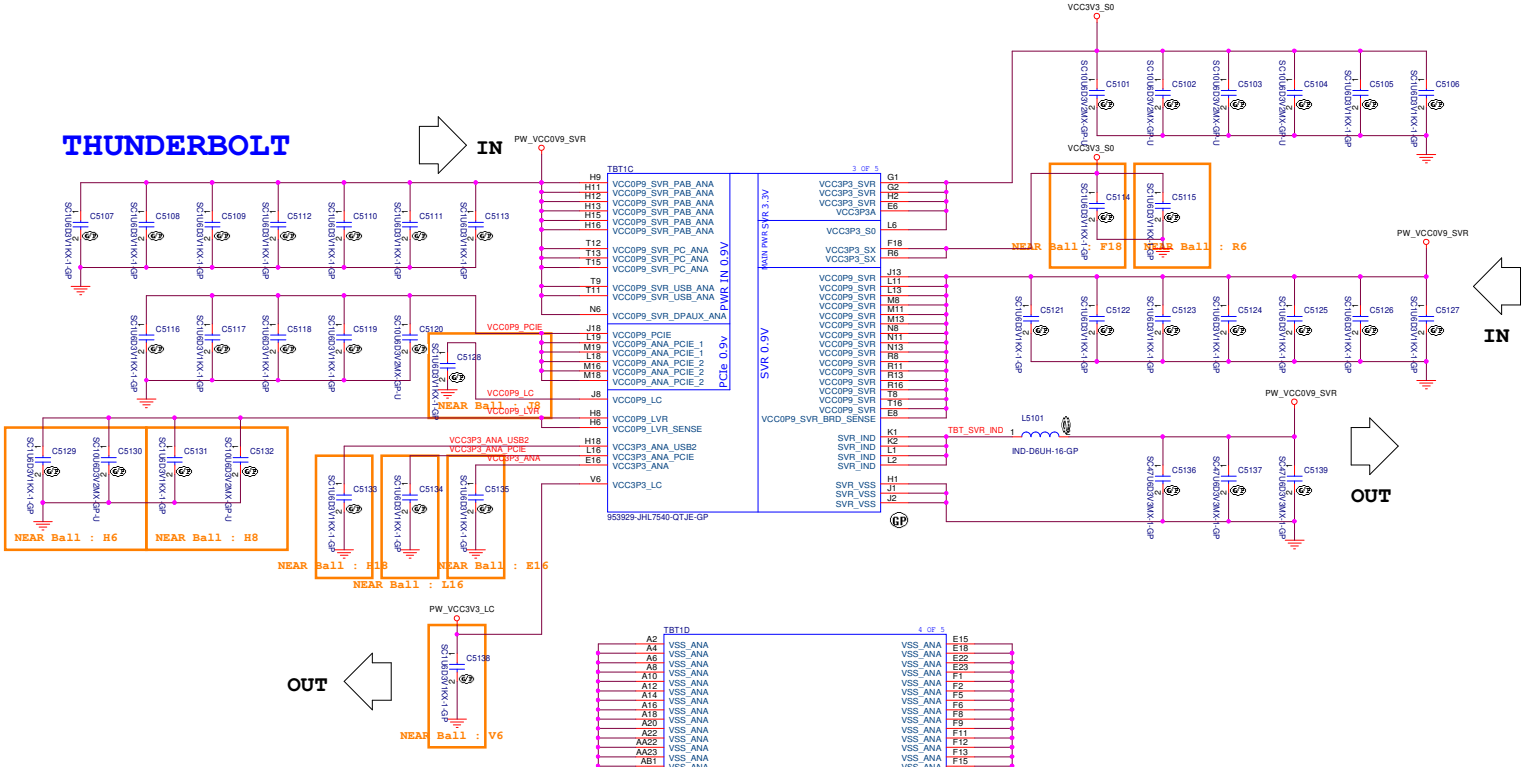


Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

緯創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TITAN RIDGE (3/3)
Size: A2	Document Number: LPM-2
Rev	-1
Date: Tuesday, April 30, 2019	Sheet 51 of 111

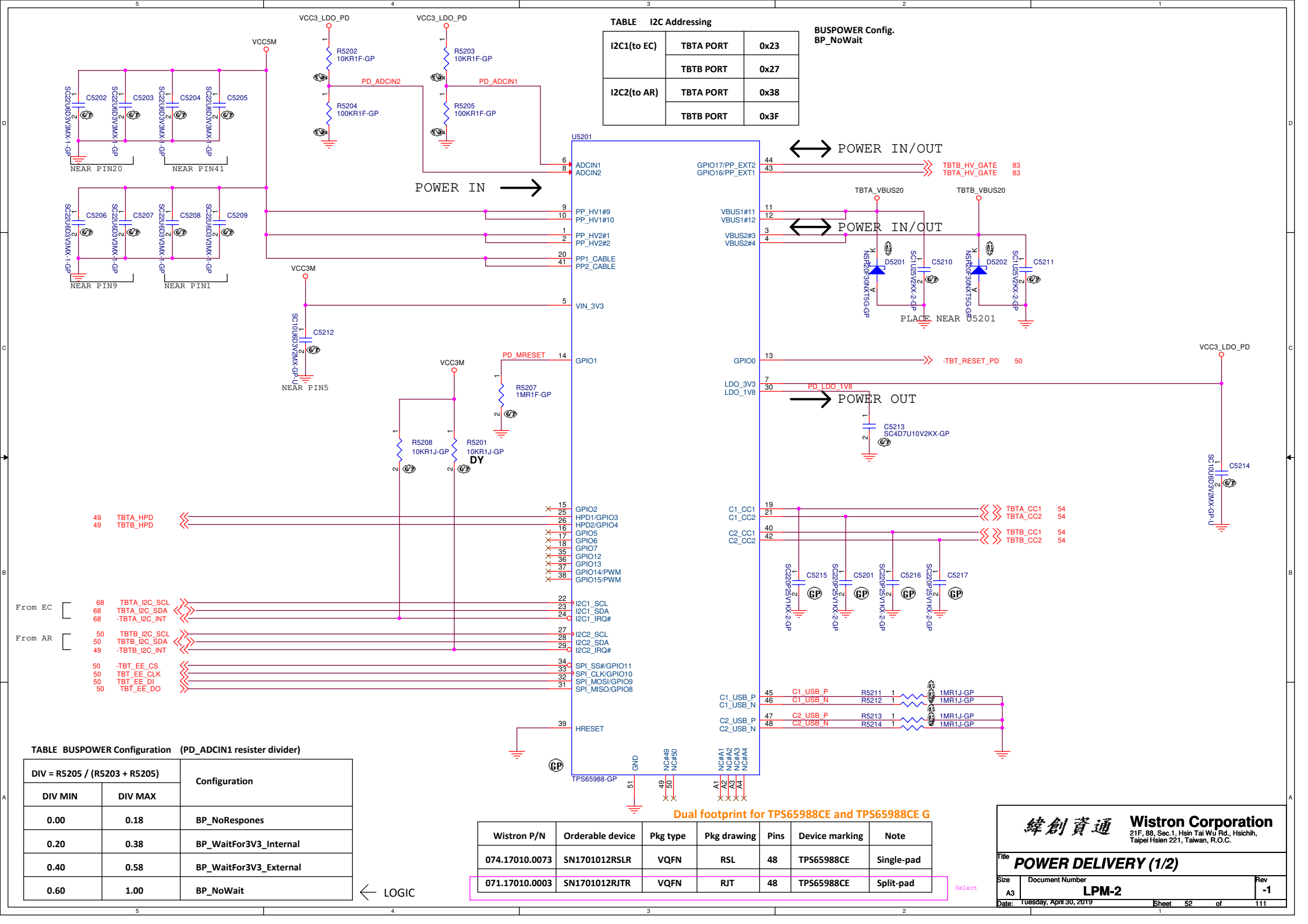
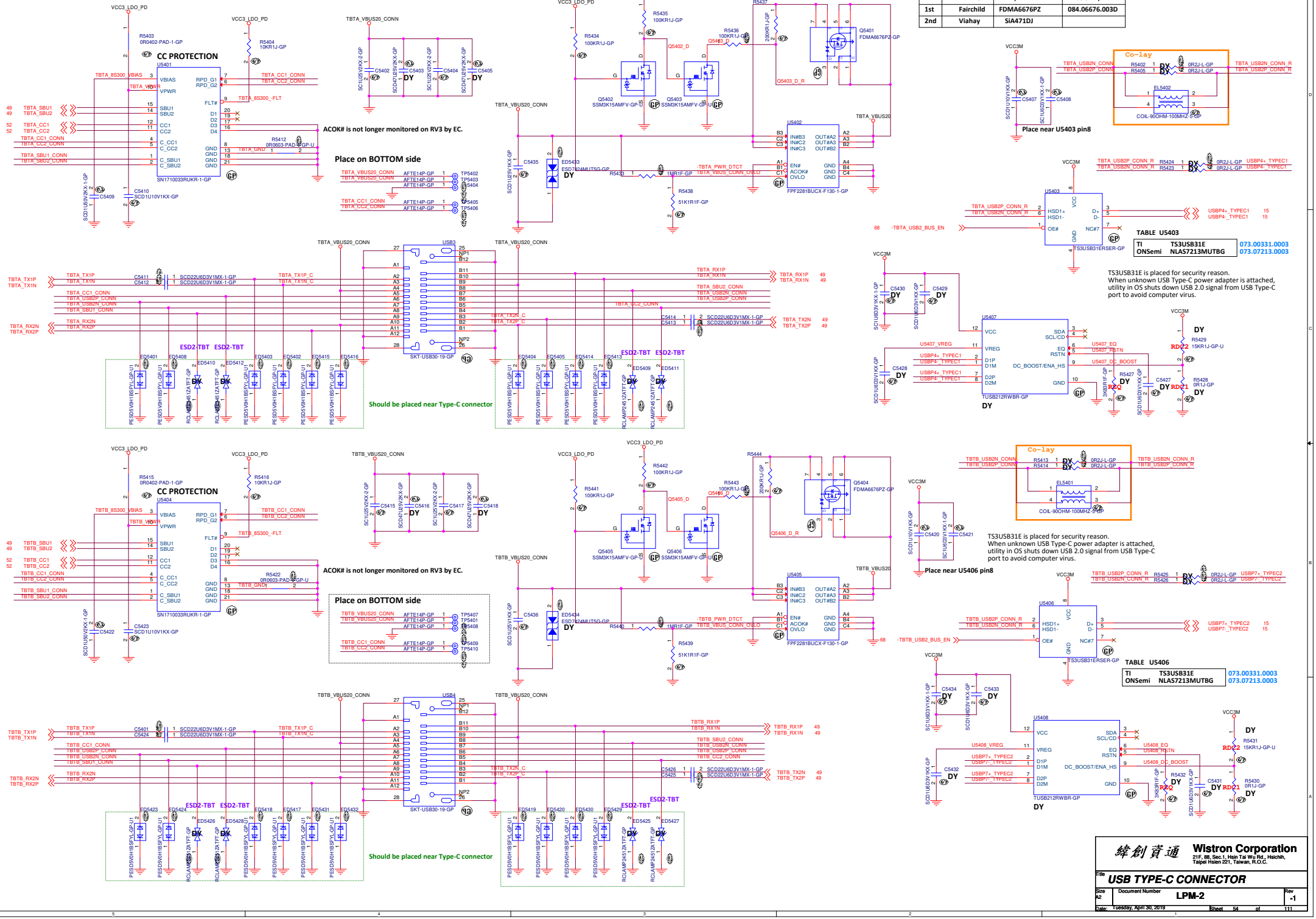


TABLE I2C Addressing
I2C1(to EC) TBTA PORT 0x23
TBTB PORT 0x27
I2C2(to AR) TBTA PORT 0x38
TBTB PORT 0x3F
BUSPOWER Config.
BP_NoWait
POWER IN
POWER IN/OUT
POWER OUT
PLACE NEAR U5201
NEAR PIN20
NEAR PIN41
NEAR PIN9
NEAR PIN1
NEAR PIN5
DY
From EC
From AR
U5201
TPS65988-GP
Dual footprint for TPS65988CE and TPS65988CE G
TABLE BUSPOWER Configuration (PD_ADCIN1 resister divider)
DIV = R5205 / (R5203 + R5205)
DIV MIN
DIV MAX
Configuration
0.00 0.18 BP_NoRespones
0.20 0.38 BP_WaitFor3V3_Internal
0.40 0.58 BP_WaitFor3V3_External
0.60 1.00 BP_NoWait
LOGIC
Wistron P/N
Orderable device
Pkg type
Pkg drawing
Pins
Device marking
Note
074.17010.0073 SN1701012RSLR VQFN RSL 48 TPS65988CE Single-pad
071.17010.0003 SN1701012RJTR VQFN RJT 48 TPS65988CE Split-pad
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER DELIVERY (1/2)
Size A3
Document Number LPM-2
Rev -1
Date: Tuesday, April 30, 2019
Sheet 52 of 111

Reserved

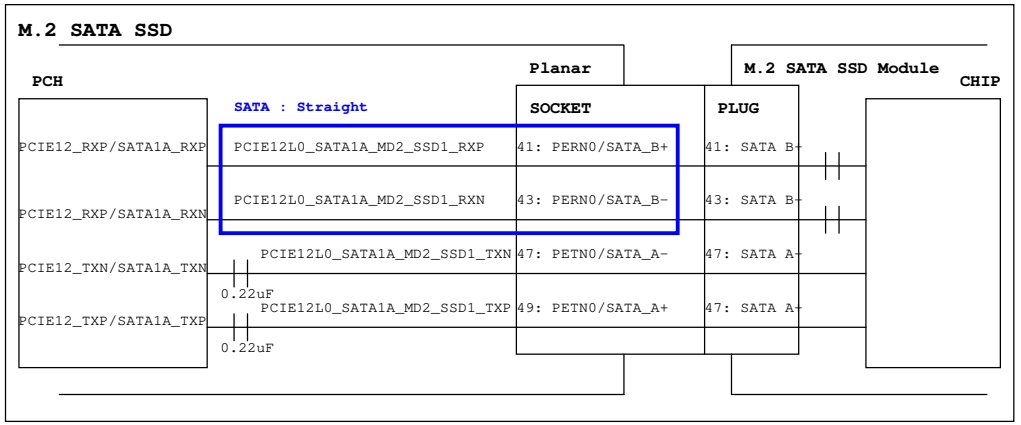
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **LPM-2**	Rev: **-1**
Date: Tuesday, April 30, 2019	Sheet 53 of 111	

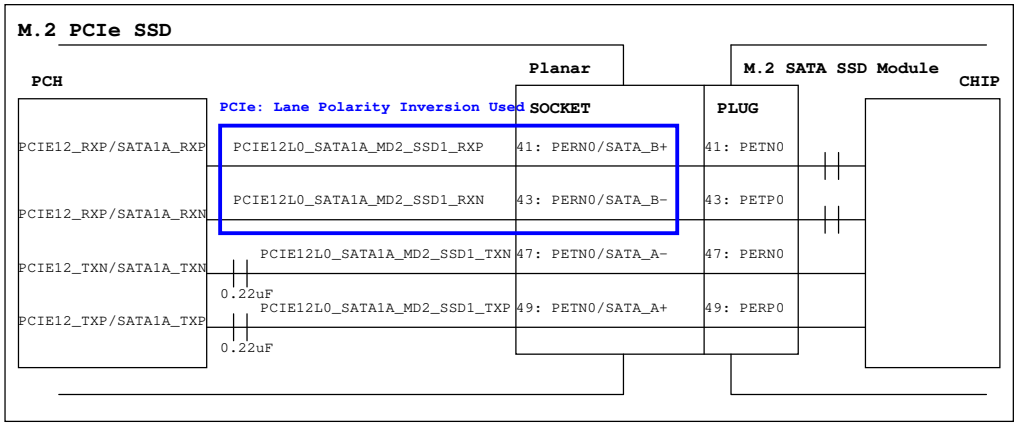
TABLE of Q5401 Q5404			
	VENDOR	P/N	Wistron P/N
1st	Fairchild	FDMA6676PZ	084.06676.003D
2nd	Viahay	SiA471DJ	



緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	USB TYPE-C CONNECTOR		
Size A2	Document Number LPM-2	Rev -1	
Date: Tuesday, April 30, 2019	Sheet 54 of 111		

M.2 SSD





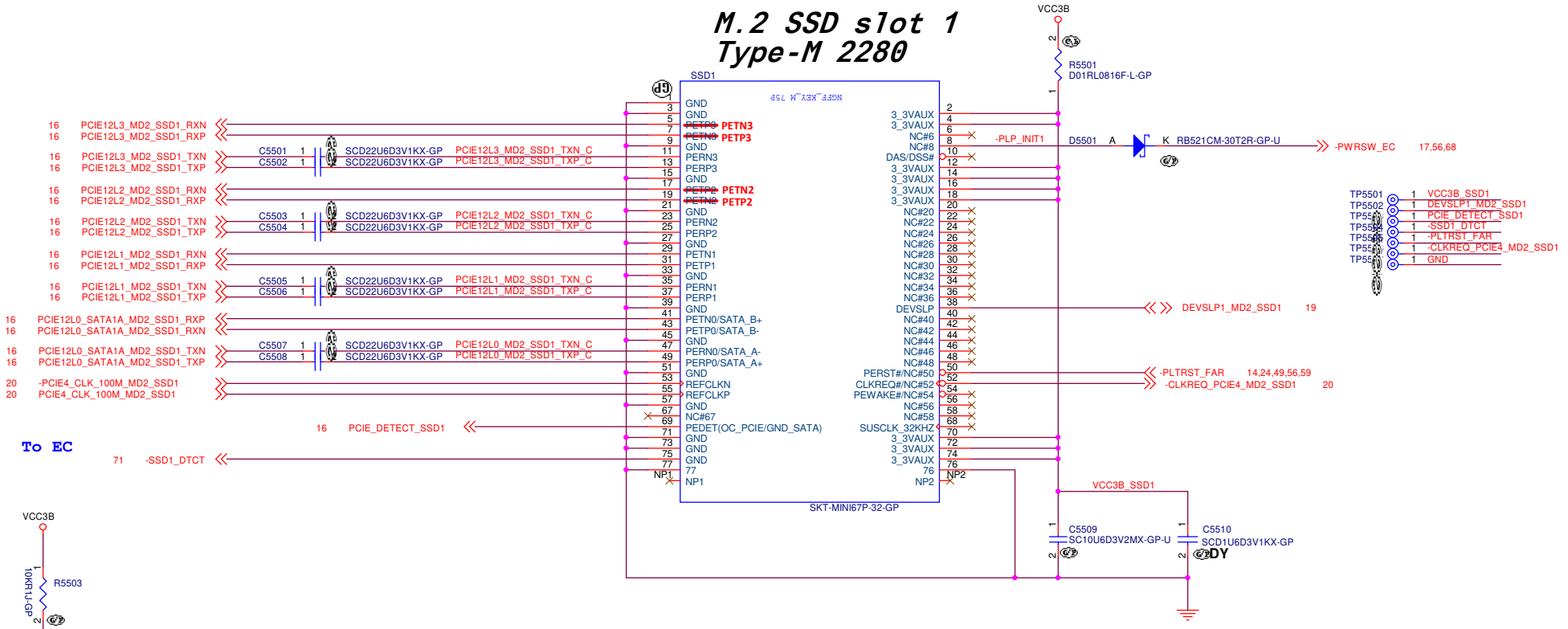
M.2 SSD slot 1
Type-M 2280

M.2 SSD1 L3

M.2 SSD1 L2

M.2 SSD1 L1

M.2 SSD1 L0



TABLE

PCIE_DETECT_SSD1	Device
LOW	SATA SSD
High	PCIe SSD

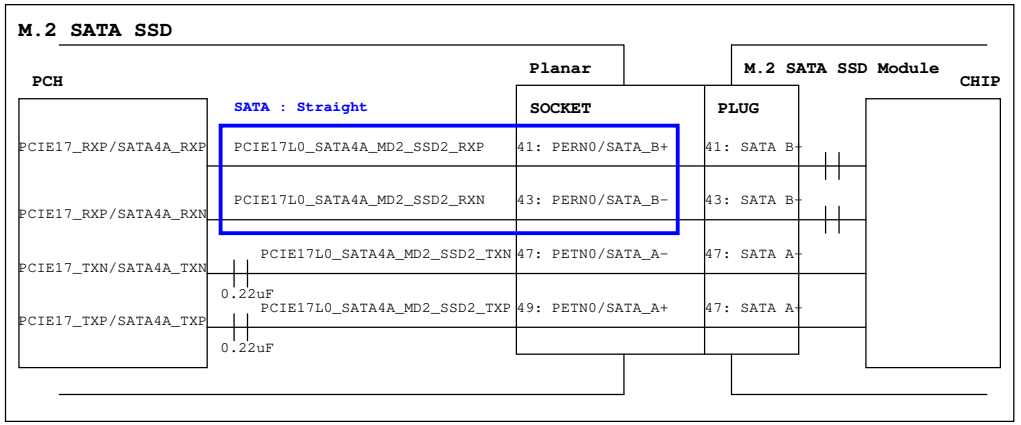
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

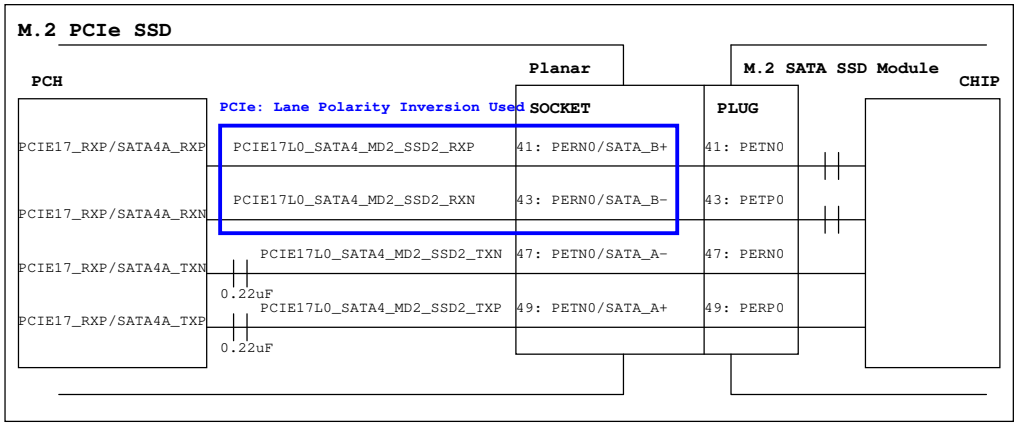
Title: M.2 SATA/PCIE SSD CARDSLOT1

Size: A3 | Document Number: LPM-2 | Rev: -1

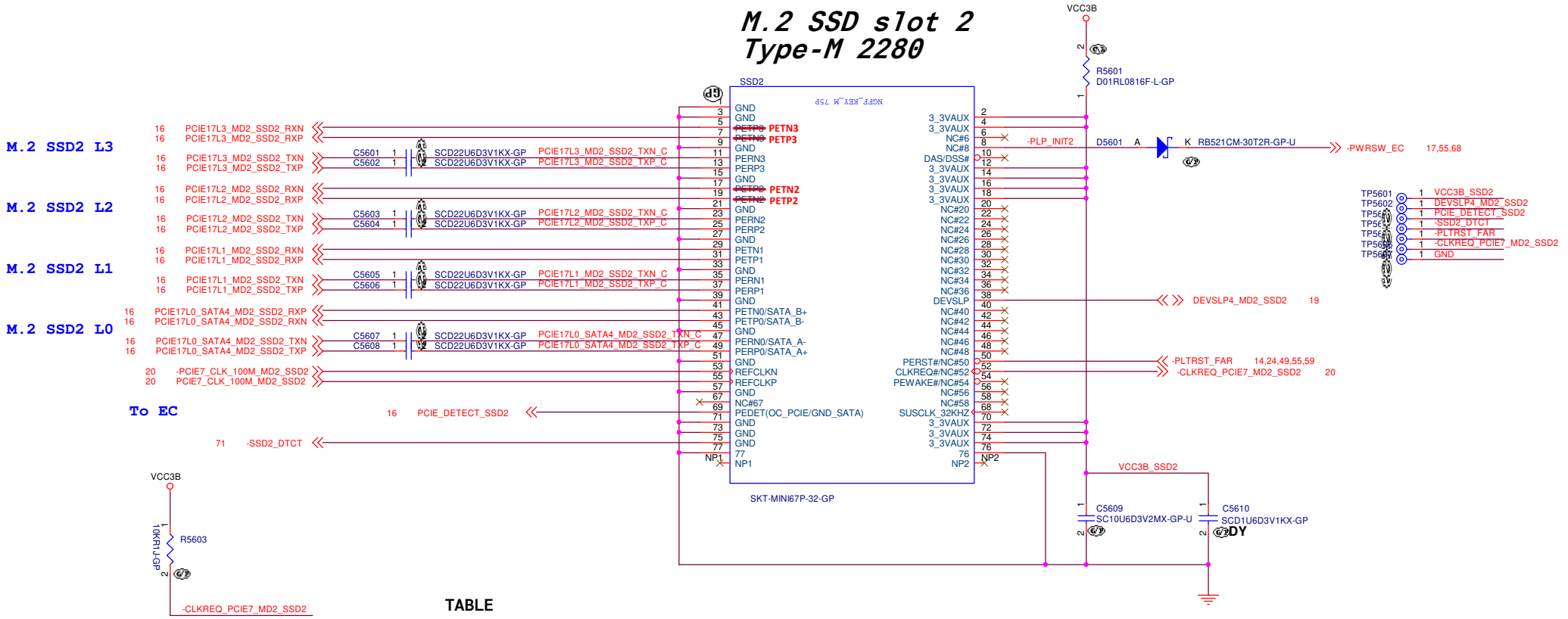
Date: Tuesday, April 30, 2019 | Sheet 55 of 111

M.2 SSD





M.2 SSD slot 2
Type-M 2280

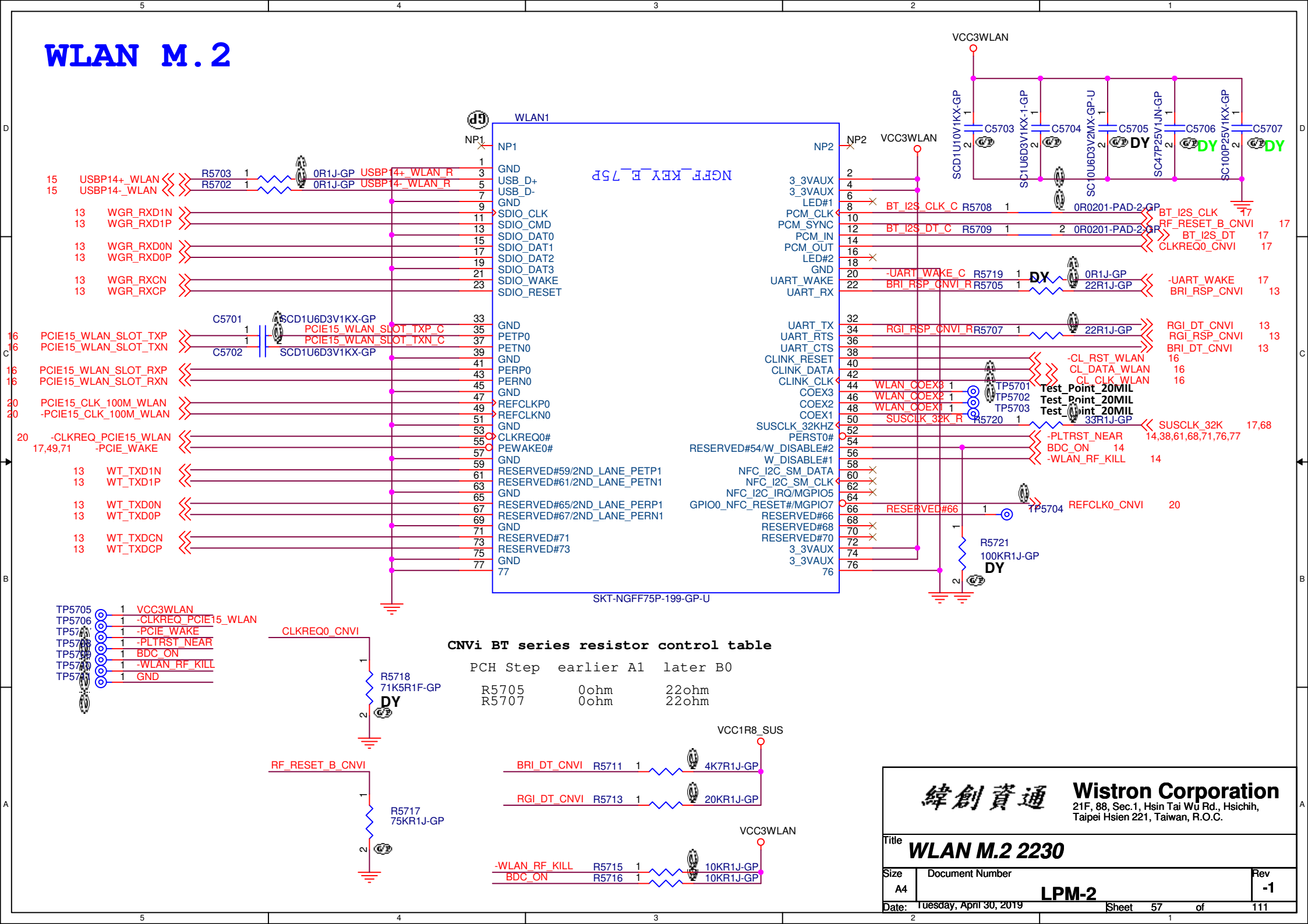


TABLE

PCIE_DETECT_SSD1	Device
LOW	SATA SSD
High	PCIe SSD

緯創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	M.2 SATA/PCIE SSD CARDSLOT2
Size	A3
Document Number	LPM-2
Rev	-1
Date:	Tuesday, April 30, 2019
Sheet	56 of 111

WLAN M.2



CNVi BT series resistor control table

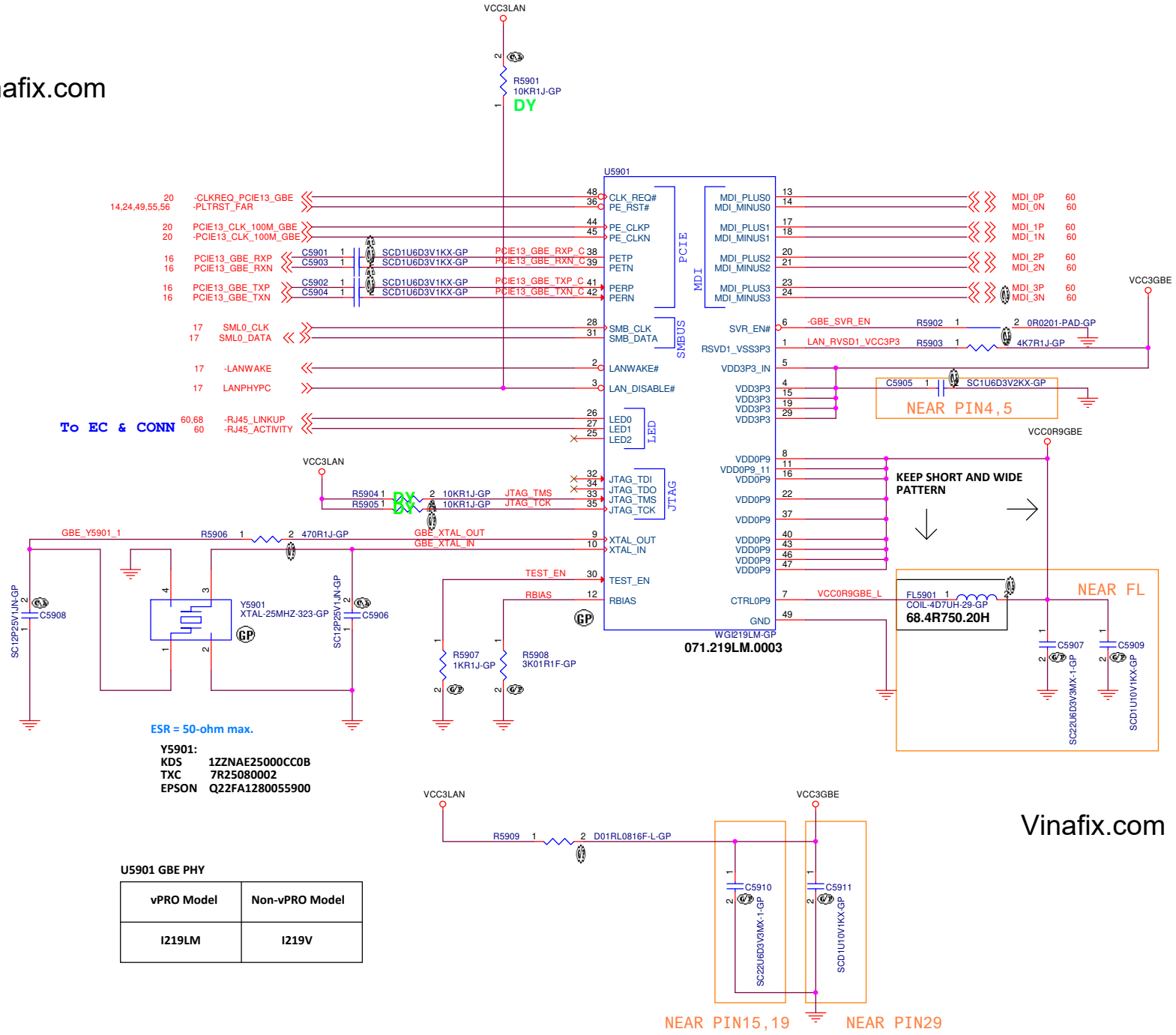
PCH Step	earlier A1	later B0
R5705	0ohm	22ohm
R5707	0ohm	22ohm

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***WLAN M.2 2230***
Size: A4	Document Number: **LPM-2** Rev: -1
Date: Tuesday, April 30, 2019	Sheet 57 of 111

Reserved

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***M.2 WWAN CARD SLOT***	
Size A4	Document Number **LPM-2**	Rev **-1**
Date: Tuesday, April 30, 2019	Sheet 58 of 111	

LAN



U5901 GBE PHY

vPRO Model	Non-vPRO Model
I219LM	I219V

ULT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

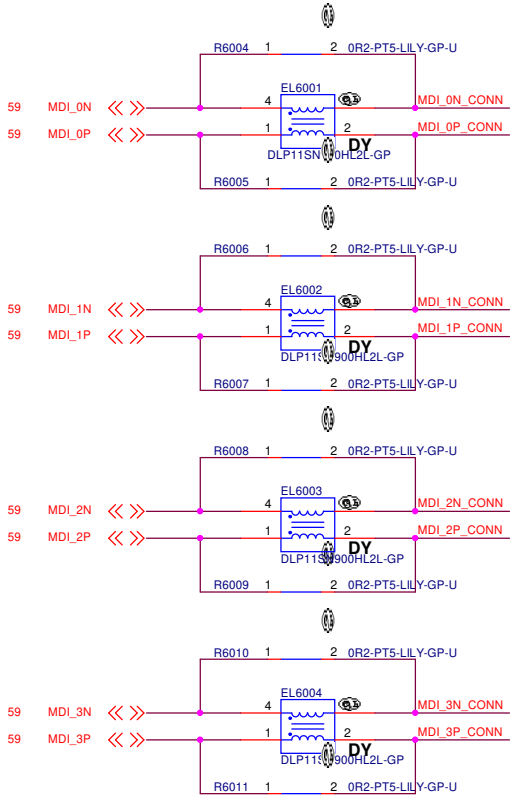
Title: **GBE JACKSONVILLE**

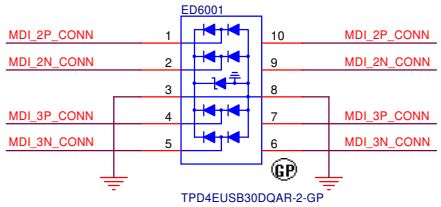
Size	Document Number	Rev
A3	LPM-2	-1

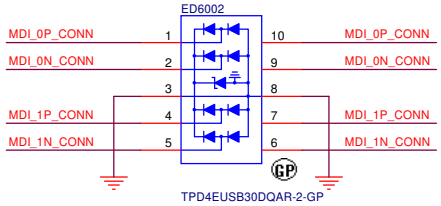
Date: Tuesday, April 30, 2019 Sheet 59 of 111

TABLE FL85-FL88

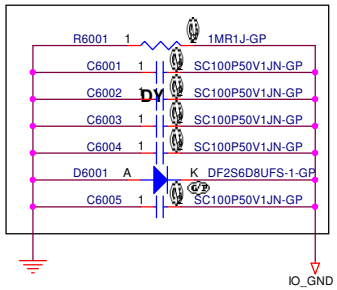
1st: Murata, DLP11SN900HL2
2nd: TDK, MCZ1210AH900L2TA0G



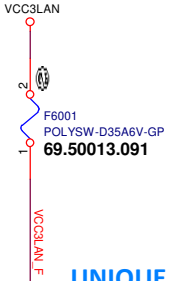




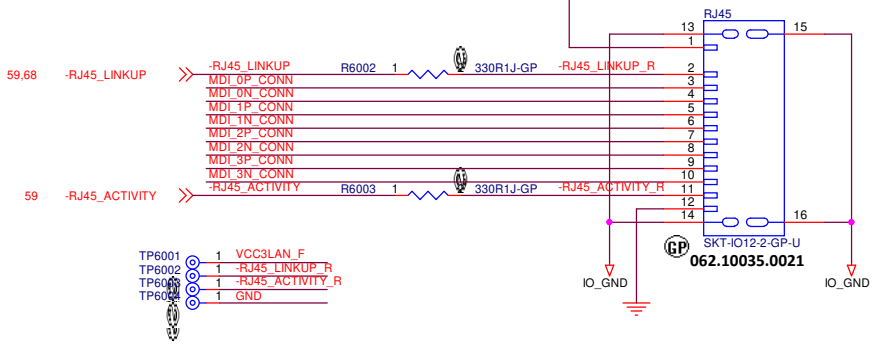
075.00430.0070



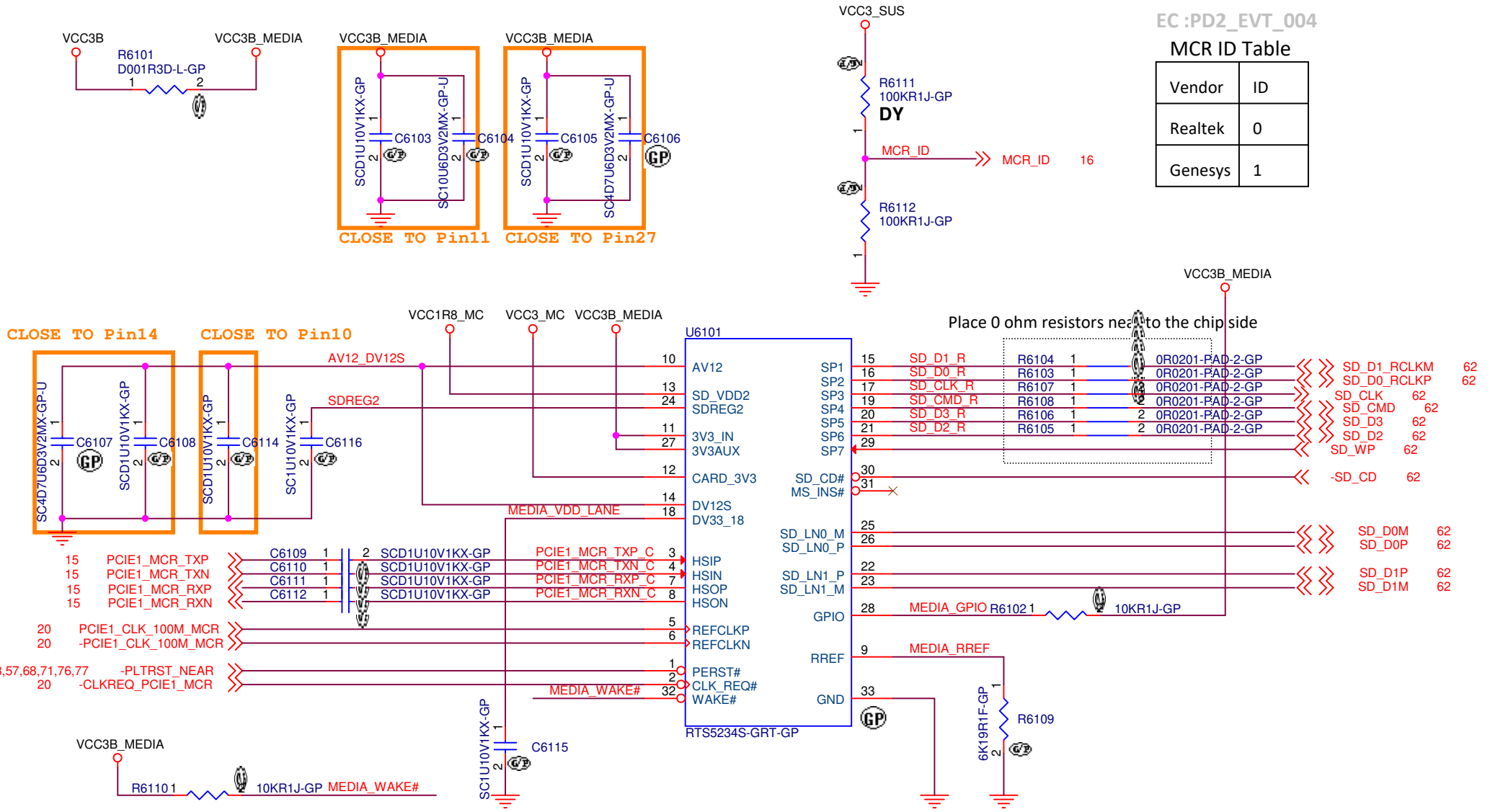
	Vendor	Description	Wistron PN
1st	LITTELFUSE	0603L035YR	069.4R350.0001
2nd	BOURNS	MF-FSMF035X-2	69.50013.091
3rd	AEM	PMS0603-035	XXX.



UNIQUE RJ45 CONN (LAN1)



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	GBE RJ45 CONNECTOR		
Size A3	Document Number LPM-2		Rev -1
Date: Tuesday, April 30, 2019		Sheet 60 of 111	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

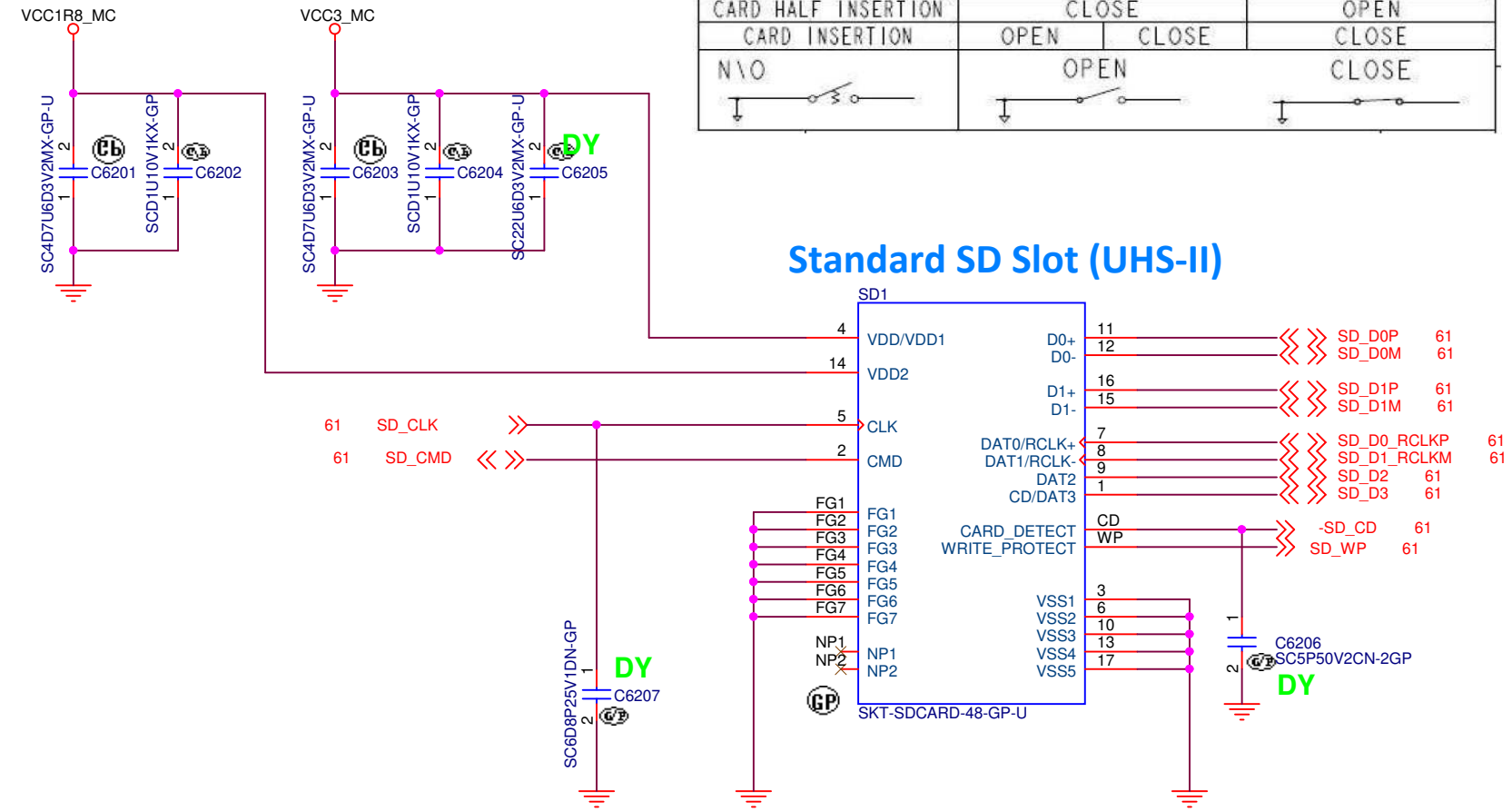
Title: ***MEDIA CARD CONTROLLER UHS-2***

Size	Document Number	Rev
A4	**LPM-2**	-1

Date: Tuesday, April 30, 2019 Sheet 61 of 111

	WRITE PROTECT SWITCH		CARD DETECT SWITCH
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	OPEN		OPEN
CARD HALF INSERTION	CLOSE		OPEN
CARD INSERTION	OPEN	CLOSE	CLOSE
N\O	OPEN		CLOSE

From RTS5348



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MEDIA CARD INTERFACE UHS-2**

Size	Document Number	Rev
A4	LPM-2	-1

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AUDIO

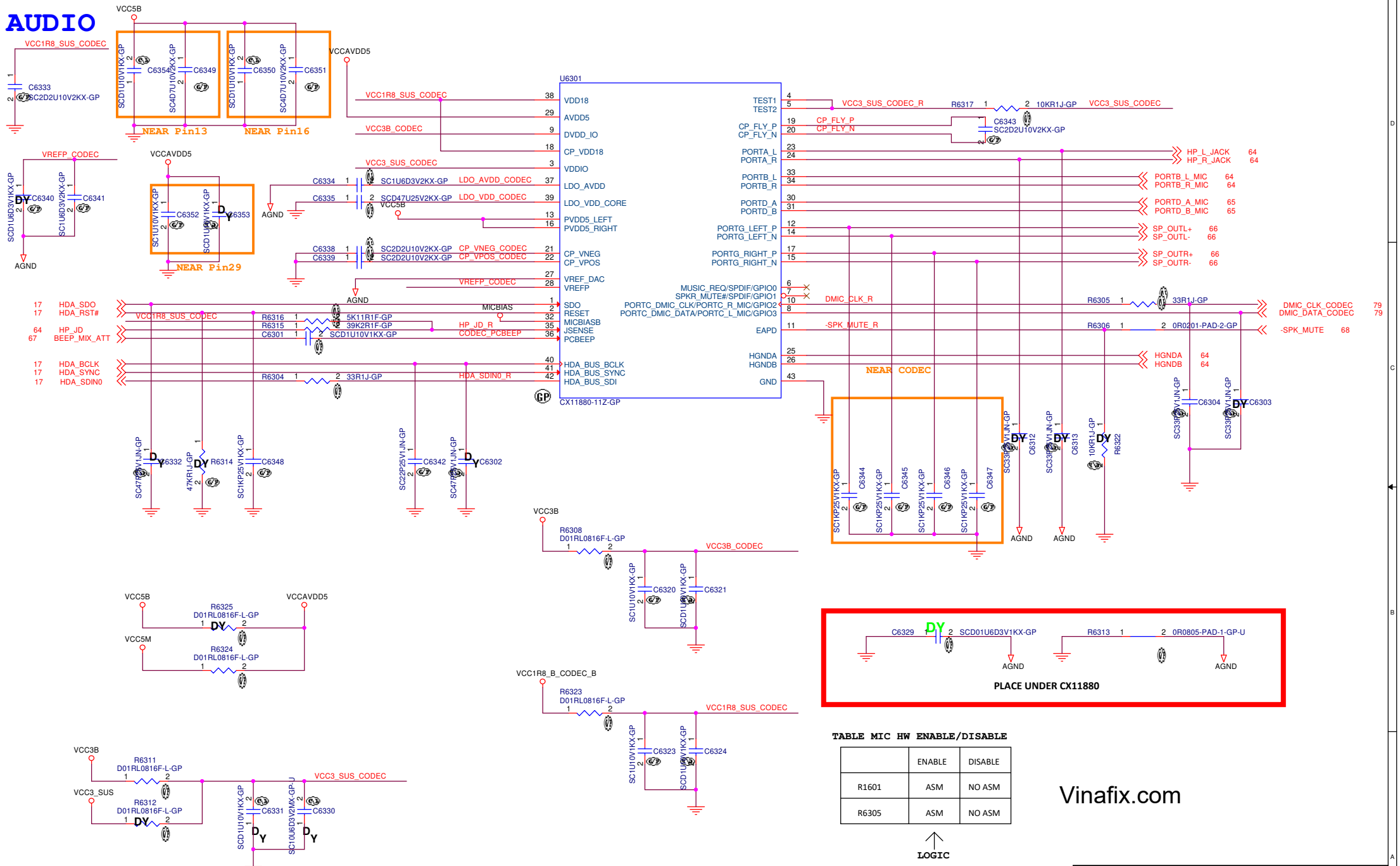


TABLE MIC HW ENABLE/DISABLE

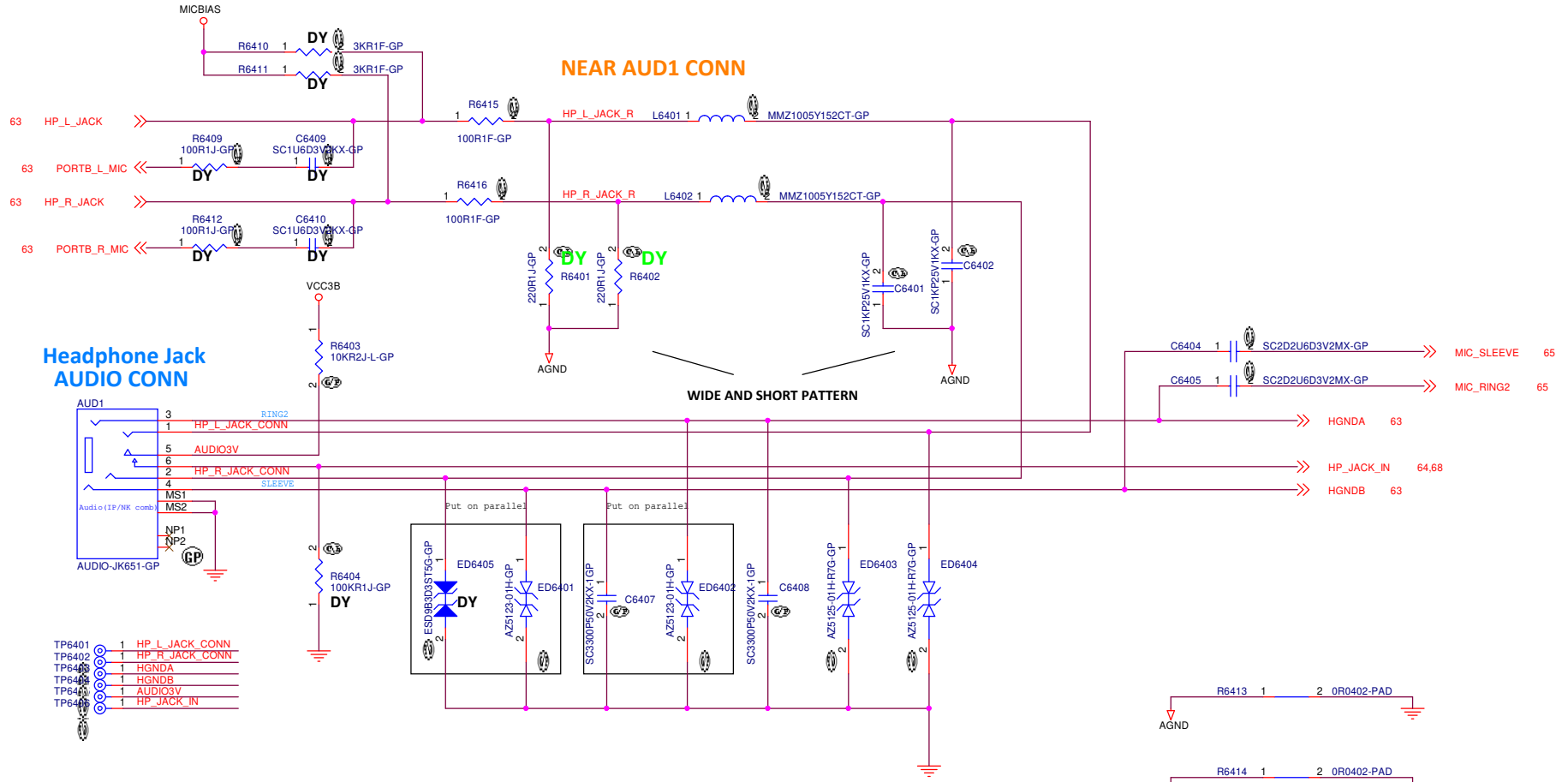
	ENABLE	DISABLE
R1601	ASM	NO ASM
R6305	ASM	NO ASM

LOGIC

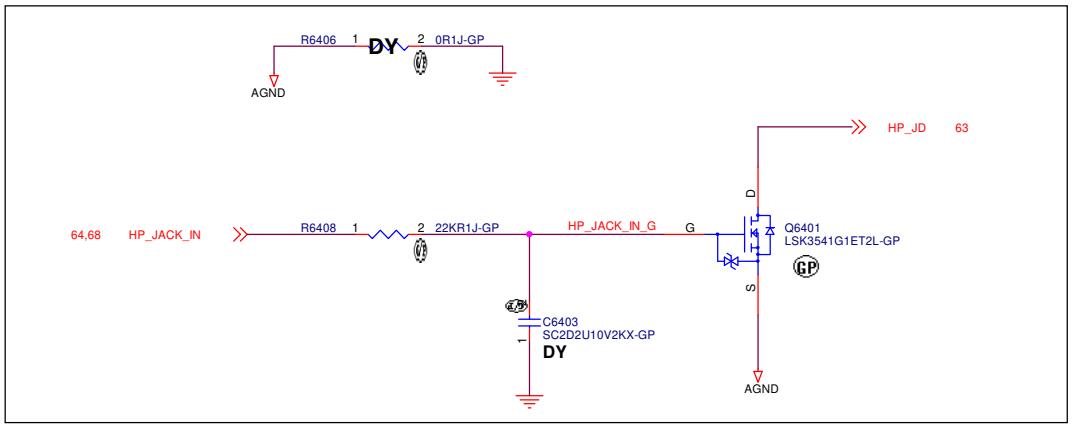
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CX11880-11Z
Size: A3 | Document Number: LPM-2 | Rev: -1
Date: Tuesday, April 30, 2019 | Sheet 63 of 111

AUDIO



AUDIO JACK SENSE



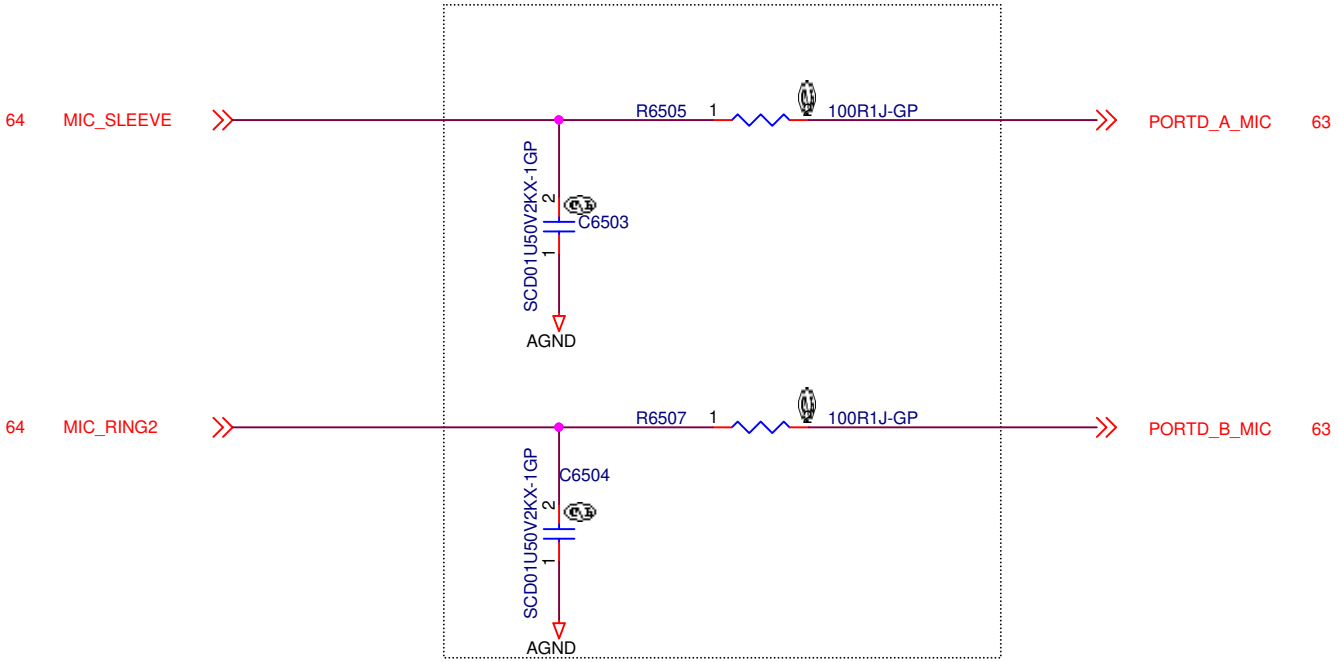
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CONNECTOR/SENSE**

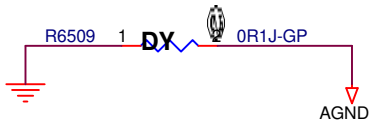
Size	Document Number	Rev
A3	LPM-2	-1

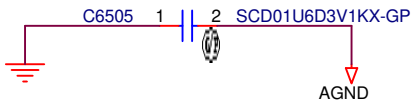
Date: Tuesday, April 30, 2019 Sheet 64 of 111

AUDIO



NEAR EXT MIC CONN





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO EXT MIC I/F***

Size	Document Number	Rev
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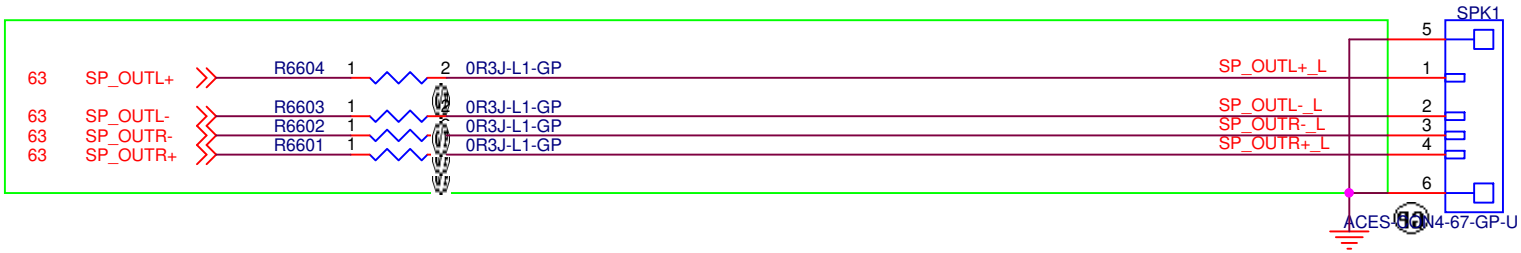
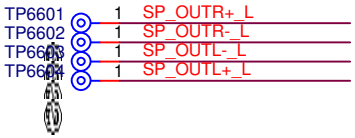
AUDIO

Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils





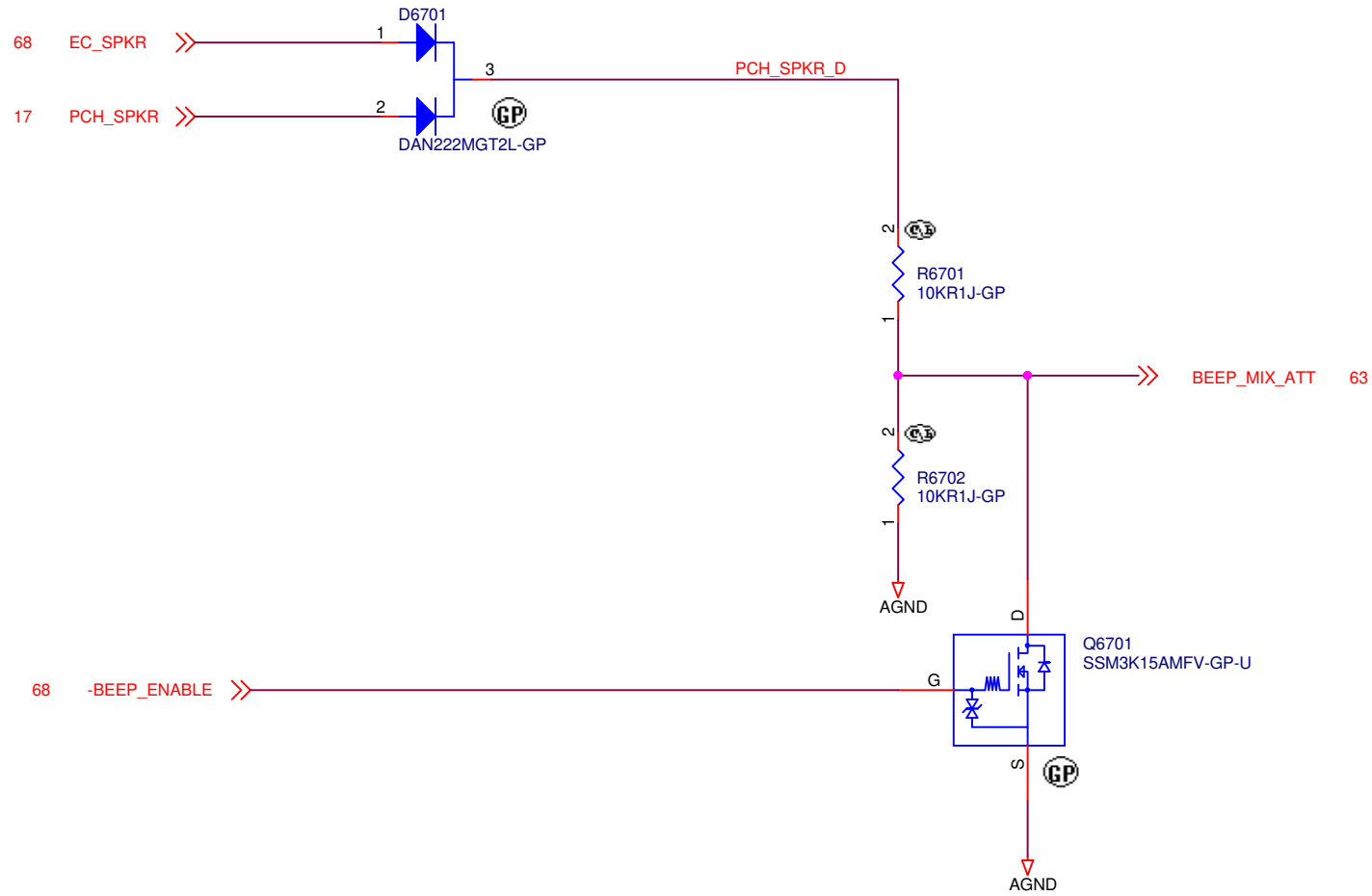
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO SPEAKER***

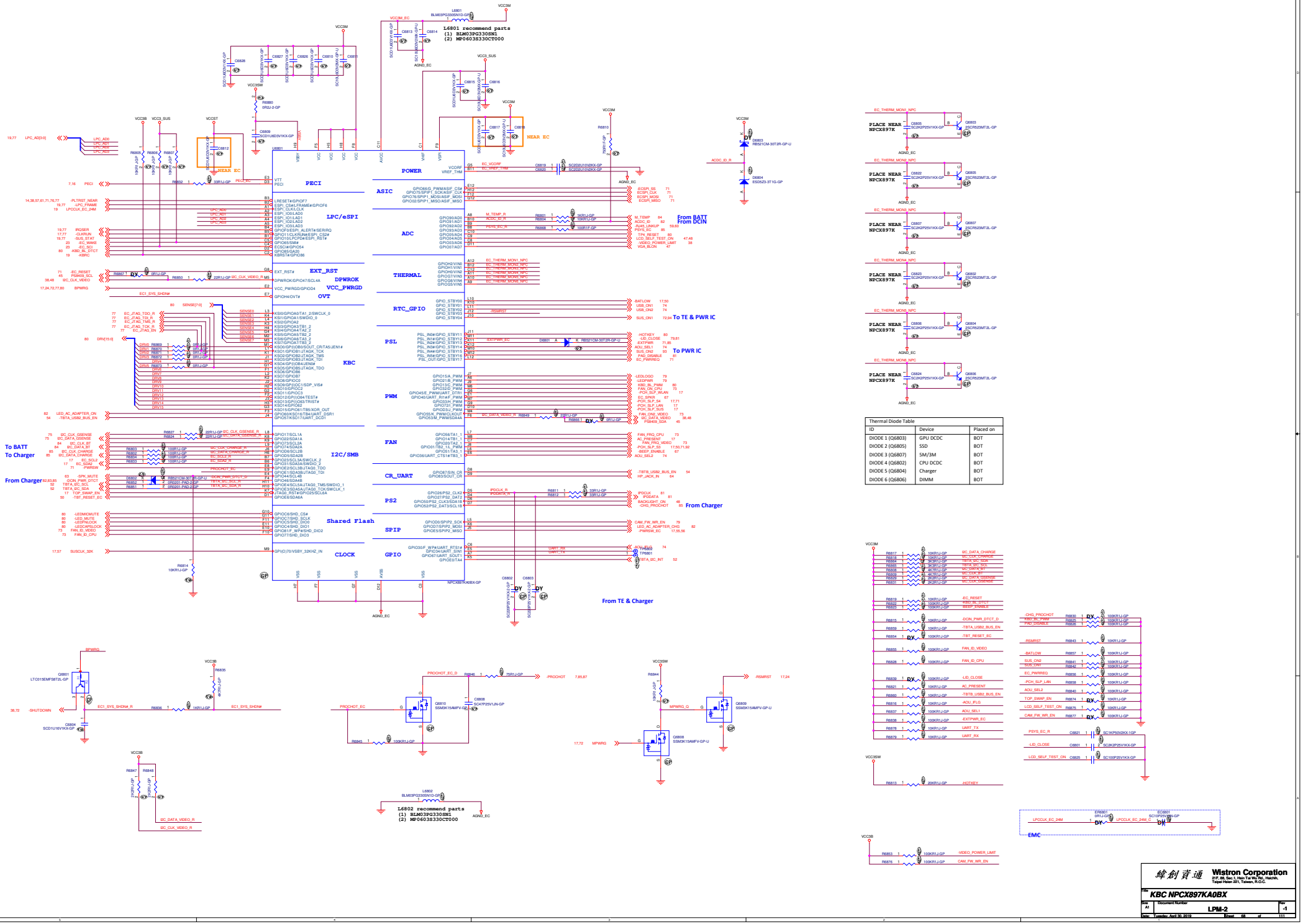
Size	Document Number	Rev
A4	LPM-2	-1

Date: Tuesday, April 30, 2019 Sheet 66 of 111

AUDIO



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO BEEP		
Size: A4	Document Number: LPM-2	Rev: -1
Date: Tuesday, April 30, 2019	Sheet 67 of 111	


L6801 recommend parts
(1) BLM03PG3308N1
(2) MPO6038330CT000
L6802 recommend parts
(1) BLM03PG3308N1
(2) MPO6038330CT000
KBC NPCX897KA0BX
POWER
PECI
LPC/eSPI
EXT_RST
DPWROK
VCC_PWRGD
OVT
KBC
I2C/SMB
Shared Flash
CLOCK
ASIC
ADC
THERMAL
RTC_GPIO
PSL
PWM
FAN
CR_UART
PS2
SPIP
GPIO
To BATT
To Charger
From Charger
From BATT
From DCIN
To TE & PWR IC
To PWR IC
From TE & Charger
From Charger
NEAR EC
PLACE NEAR NPCX897K
EMC
Thermal Diode Table
ID | Device | Placed on
DIODE 1 (Q6803) | GPU DCDC | BOT
DIODE 2 (Q6805) | SSD | BOT
DIODE 3 (Q6807) | 5M/3M | BOT
DIODE 4 (Q6802) | CPU DCDC | BOT
DIODE 5 (Q6804) | Charger | BOT
DIODE 6 (Q6806) | DIMM | BOT
Wistron Corporation
KBC NPCX897KA0BX
LPM-2
Tuesday, April 30, 2019

Reserved

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

Size	Document Number	Rev
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Reserved

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

Size	Document Number	Rev
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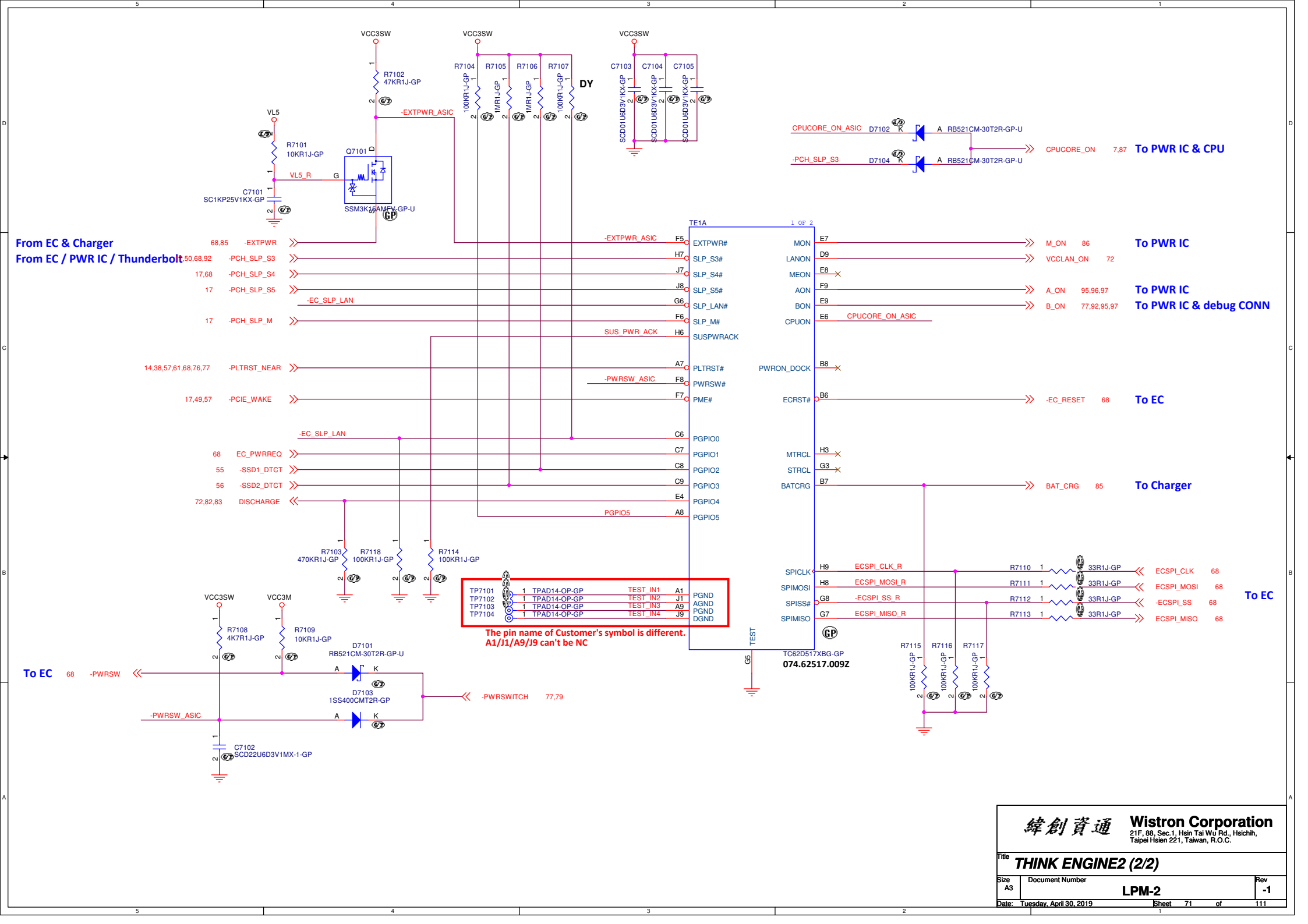
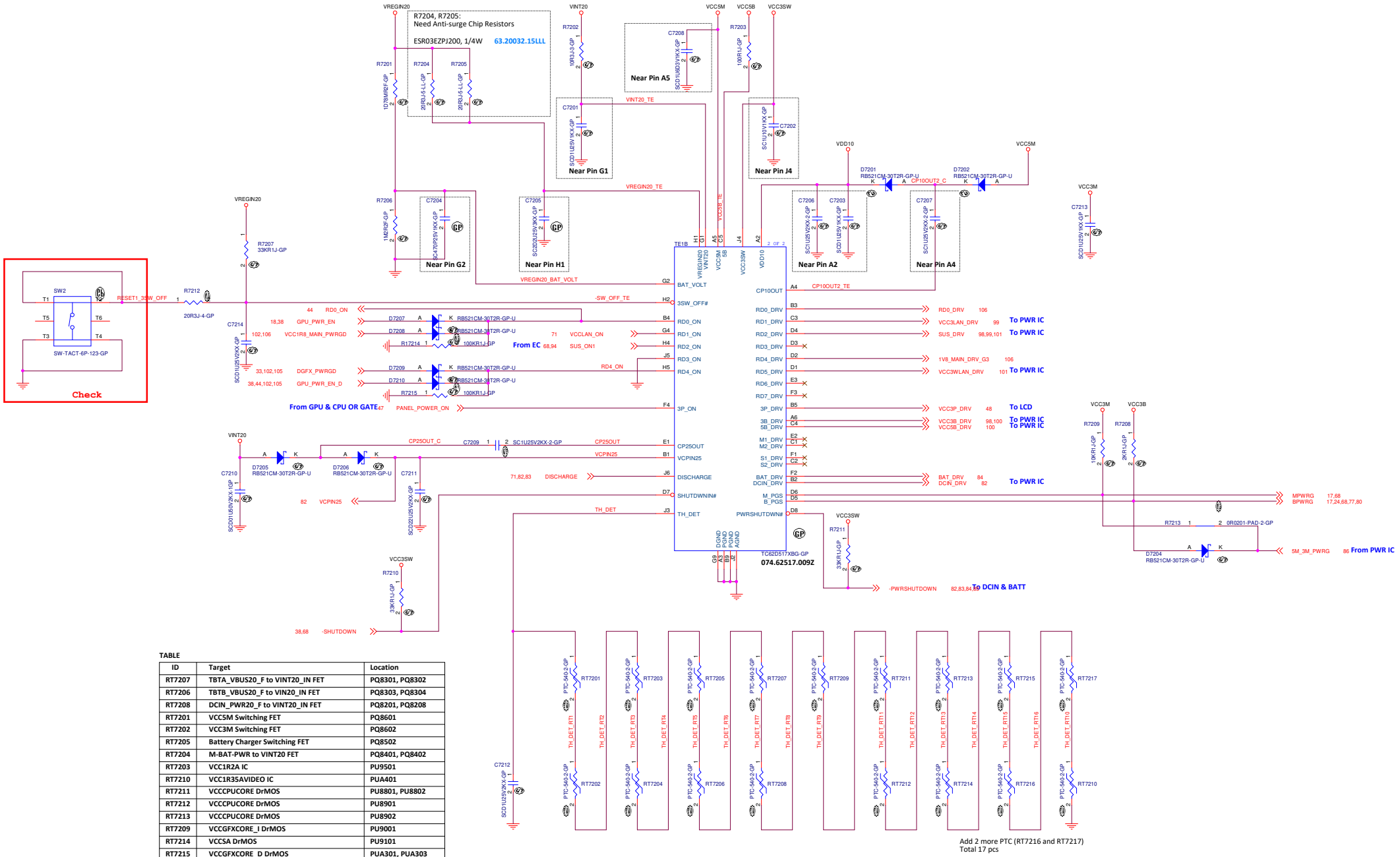


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *THINK ENGINE2 (2/2)*		
Size: A3	Document Number: LPM-2	Rev: -1
Date: Tuesday, April 30, 2019	Sheet 71 of 111	

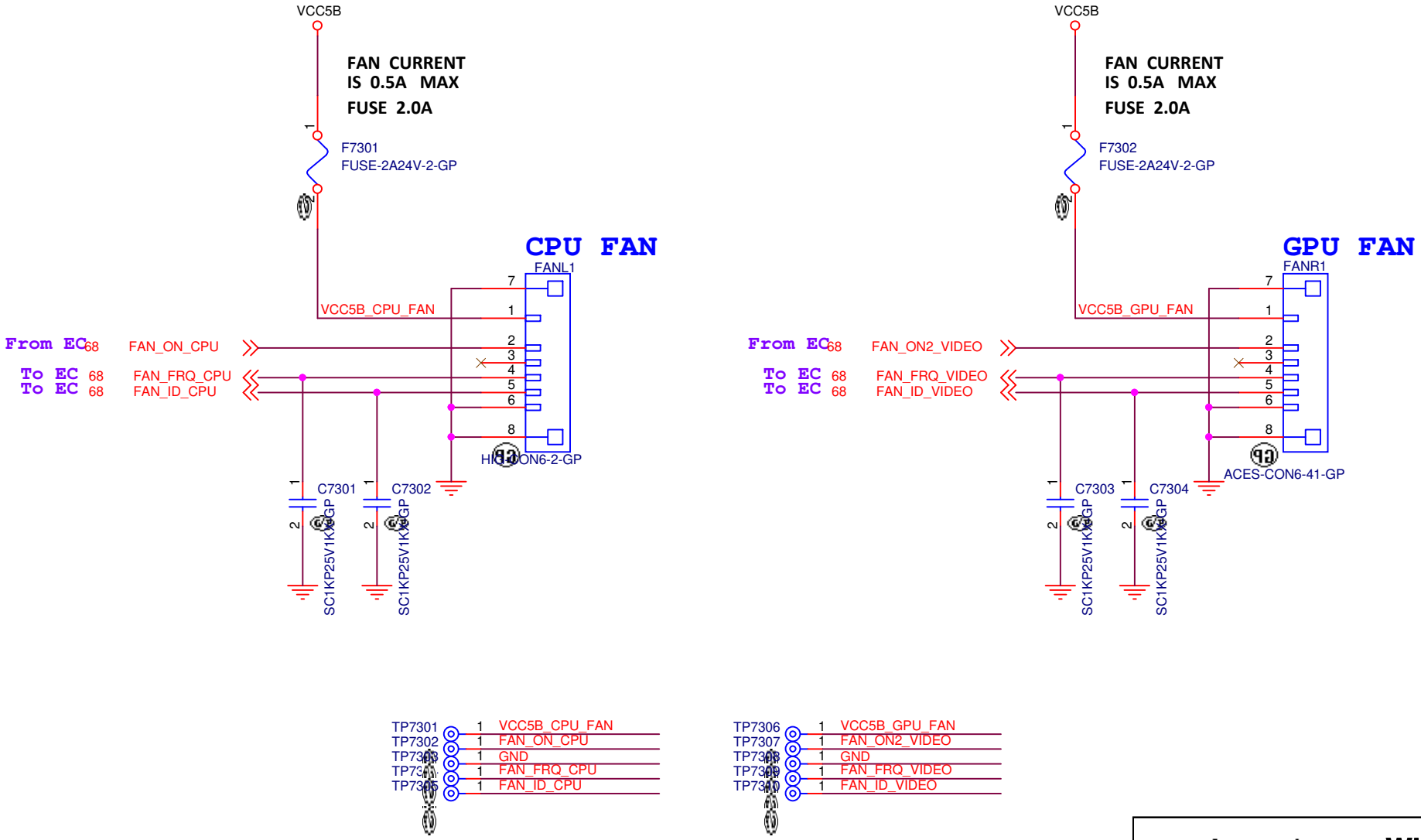


TABLE

ID	Target	Location
RT7207	TBTA_VBUS20_F to VINT20_IN FET	PQ8301, PQ8302
RT7206	TBTB_VBUS20_F to VIN20_IN FET	PQ8303, PQ8304
RT7208	DCIN_PWR20_F to VINT20_IN FET	PQ8201, PQ8208
RT7201	VCC5M Switching FET	PQ8601
RT7202	VCC3M Switching FET	PQ8602
RT7205	Battery Charger Switching FET	PQ8502
RT7204	M-BAT-PWR to VINT20 FET	PQ8401, PQ8402
RT7203	VCC1R2A IC	PU9501
RT7210	VCC1R35AVIDEO IC	PUA401
RT7211	VCCCPUCORE DrMOS	PU8801, PU8802
RT7212	VCCCPUCORE DrMOS	PU8901
RT7213	VCCCPUCORE DrMOS	PU8902
RT7209	VCCGFXCORE_I DrMOS	PU9001
RT7214	VCCSA DrMOS	PU9101
RT7215	VCCGFXCORE_D DrMOS	PUA301, PUA303
RT7216	VCCGFXCORE_D DrMOS	PUA302
RT7217	CPU Die	CPU1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	THINK ENGINE3 (2/2)		
Size A2	Document Number LPM-2	Rev -1	
Date: Tuesday, April 30, 2019	Sheet 72 of 111		

FAN



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***FAN CONNECTOR***	
Size A4	Document Number **LPM-2**	Rev **-1**
Date: Tuesday, April 30, 2019	Sheet 73 of 111	

TABLE of USB Charge	
TI	SN1702001RTER (PG1.1)
Pericom	PI5USB2546HZHEX

TABLE of USB3.0 Single	
GMT	G548A1F51U
TI	TPS2069CDGNR-2

USB_PWR_S1
WIDE PATTERN(MIN 500mA)
C7402 SCD1U10V1KX-GP
C7403 SCD1U6D3V1KX-GP
TC7402 ST150U6D3VBM-GP
TP7401 USB_PWR_S1
TP7402 GND
TP7403 USB_PWR_S2
TP7404 GND

U7402
USB3P1_RXN_CONN
USB3P1_RXP_CONN
USB3P1_TXN_CONN
USB3P1_TXP_CONN
RCLAMP0524PATCT-1-GP-U

Co-lay
R7402 0R2J-L-GP DY
R7403 0R2J-L-GP DY
EL7402 COIL-90OHM-100MHZ-5-GP
USBP1-_AOU
USBP1+_AOU
USBP1-_CONN
USBP1+_CONN

AOZ8105CI-1-GP
U7403

USB1
VBUS
D-
D+
STDA_SSRX-
STDA_SSRX+
STDA_SSTX-
STDA_SSTX+
GND_DRAIN
GND
SKT-USB15-9-GP-U
DY

EL7401 DY
EL7403 DY
R7404 0R2J-L-GP
R7401 0R2J-L-GP
R7405 0R2J-L-GP
R7406 0R2J-L-GP
C7405 SCD1U6D3V1KX-GP
C7406 SCD1U6D3V1KX-GP
USB3P1_SYSP1_RXN
USB3P1_SYSP1_RXP
USB3P1_SYSP1_TXN
USB3P1_SYSP1_TXP
USB3P1_RXN_CONN
USB3P1_RXP_CONN
USB3P1_TXN_CONN
USB3P1_TXP_CONN
Co-lay

PAD1 PAD-SLIDE-1P-GP USB_PWR_S1
PAD2 PAD-SLIDE-1P-GP USBP1-_CONN
PAD3 PAD-SLIDE-1P-GP USBP1+_CONN
PAD4 PAD-SLIDE-1P-GP

VCC5M
USB_PWR_S1
C7404 SCD1U10V1KX-GP
U7404
IN
OUT
ILIM_HI
ILIM_LO
ILIM_SEL
CLT1
CLT2
CLT3
DP_IN
DP_OUT
DM_IN
DM_OUT
EN
FAULT#
STATUS#
GND
SN1702001RTER-GP
USB1_ILIM_HI
USB1_ILIM_LO
AOU_SEL1
AOU_SEL2
USB_ON1
USBP1+_SYSP1
USBP1-_SYSP1
-USB_PORT0_OC0
-AOU_IFLG
R7407 22K1R1F-GP
R7408 2M7R1J-GP

USB_PWR_S2
WIDE PATTERN(MIN 500mA)
C7407 SCD1U10V1KX-GP
C7408 SCD1U6D3V1KX-GP
TC7401 ST150U6D3VBM-GP

U7401
USB3P2_RXN_CONN
USB3P2_RXP_CONN
USB3P2_TXN_CONN
USB3P2_TXP_CONN
RCLAMP0524PATCT-1-GP-U

Co-lay
R7409 0R2J-L-GP DY
R7410 0R2J-L-GP DY
EL7404 COIL-90OHM-100MHZ-5-GP
USBP2-_SYSP2
USBP2+_SYSP2
USBP2-_CONN
USBP2+_CONN

AOZ8105CI-1-GP
U7405

USB2
VBUS
D-
D+
STDA_SSRX-
STDA_SSRX+
STDA_SSTX-
STDA_SSTX+
GND_DRAIN
GND
SKT-USB15-9-GP-U
DY

EL7405 DY
EL7406 DY
R7411 0R2J-L-GP
R7412 0R2J-L-GP
R7413 0R2J-L-GP
R7414 0R2J-L-GP
C7410 SCD1U6D3V1KX-GP
C7401 SCD1U6D3V1KX-GP
USB3P2_SYSP2_RXN
USB3P2_SYSP2_RXP
USB3P2_SYSP2_TXN
USB3P2_SYSP2_TXP
USB3P2_RXN_CONN
USB3P2_RXP_CONN
USB3P2_TXN_CONN
USB3P2_TXP_CONN
Co-lay

PAD5 PAD-SLIDE-1P-GP USB3P1_RXN_CONN
PAD6 PAD-SLIDE-1P-GP USB3P1_RXP_CONN
PAD7 PAD-SLIDE-1P-GP USB3P1_TXN_CONN
PAD8 PAD-SLIDE-1P-GP USB3P1_TXP_CONN
PAD9 PAD-SLIDE-1P-GP

VCC5M
C7409 SCD1U10V1KX-GP
U7406
GND
IN#2
IN#3
EN/EN#
OUT#8
OUT#7
OUT#6
FLT#
TPS2069CDGNR-GP
USB_PWR_S2
USB_ON2
-USB_PORT1_OC1

PAD10 PAD-SLIDE-1P-GP USB_PWR_S2
PAD11 PAD-SLIDE-1P-GP USBP2-_CONN
PAD12 PAD-SLIDE-1P-GP USBP2+_CONN
PAD13 PAD-SLIDE-1P-GP

PAD14 PAD-SLIDE-1P-GP USB3P2_RXN_CONN
PAD15 PAD-SLIDE-1P-GP USB3P2_RXP_CONN
PAD16 PAD-SLIDE-1P-GP
PAD17 PAD-SLIDE-1P-GP USB3P2_TXN_CONN
PAD18 PAD-SLIDE-1P-GP USB3P2_TXP_CONN

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB POWER/CONNECTOR

Size	Document Number	Rev
A3	LPM-2	-1

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TABLE

P/N	ADDR_SEL	Address
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)
LIS2DWLTR	H L	

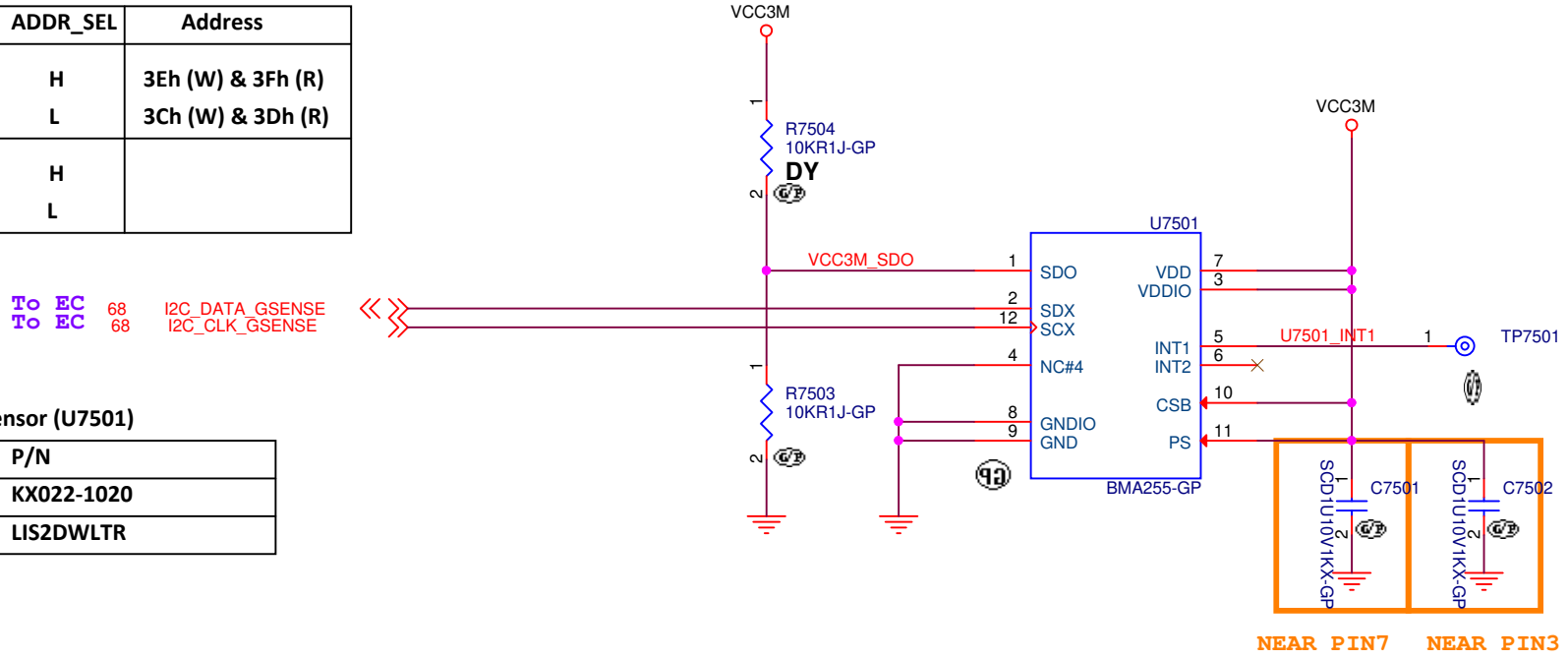

TABLE of G-Sensor (U7501)

Vendor	P/N
Kionix	KX022-1020
ST Micro	LIS2DWLTR

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***APS G-SENSOR P-SENSOR***

Size	Document Number	Rev
A4	LPM-2	-1

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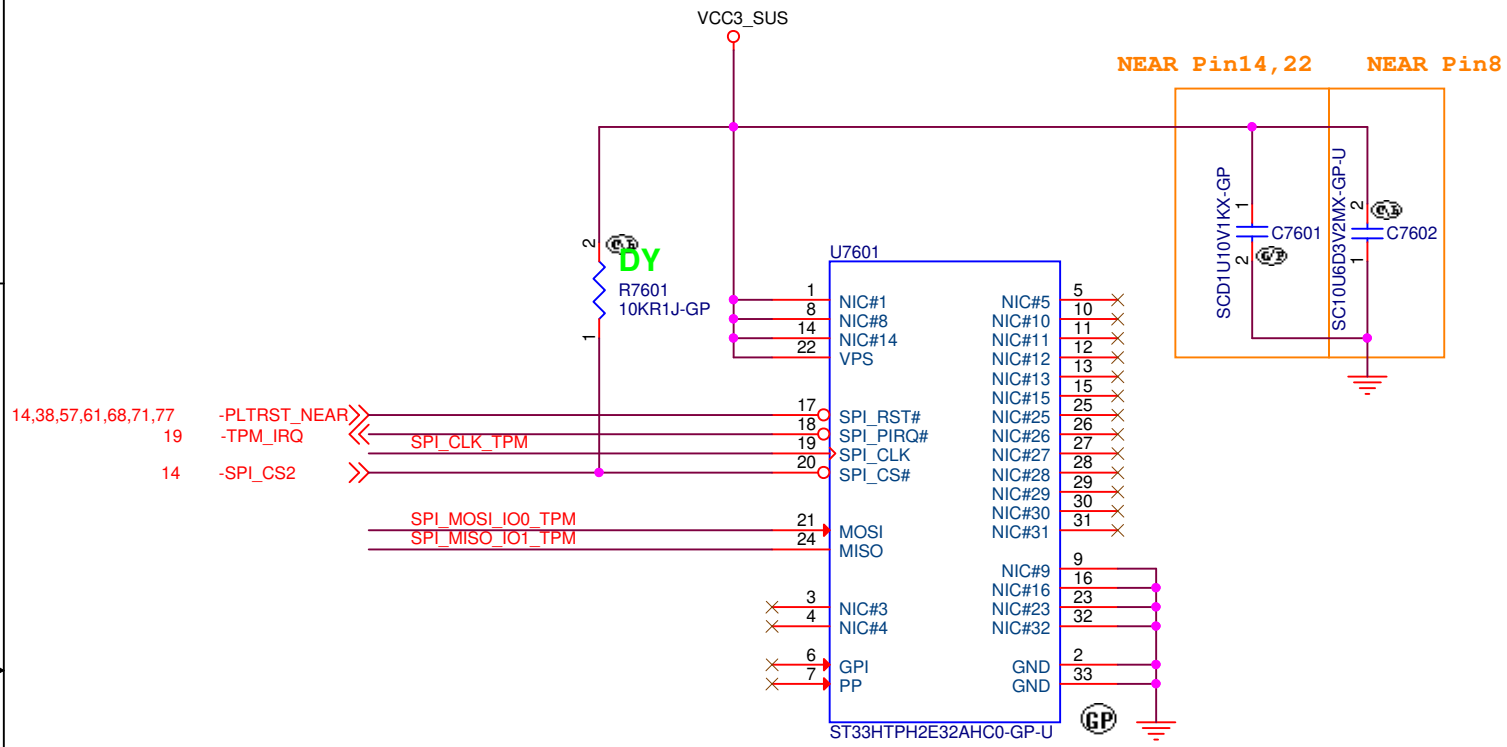
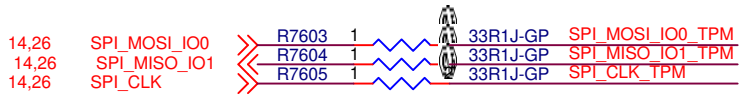
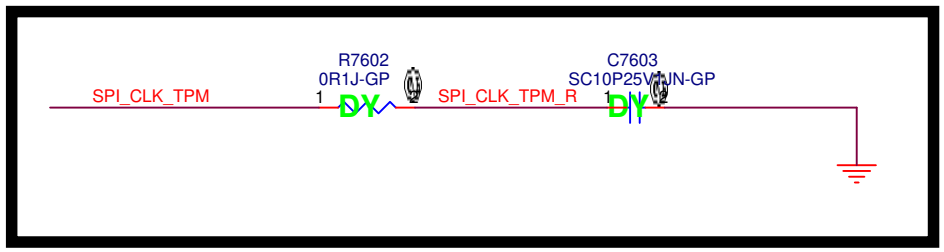
TPM







U7601	Vendor P/N	Lenovo P/N	Wistron P/N
Nuvoton	NPCT750LABYX FW 7.2.1.0	TBD	SL80R40158AA
ST Micro	ST33HTPH2E32AHC0	TBD	071.33232.0H03

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Title: ***DISCRETE TPM 2.0***

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A4	LPM-2	-1

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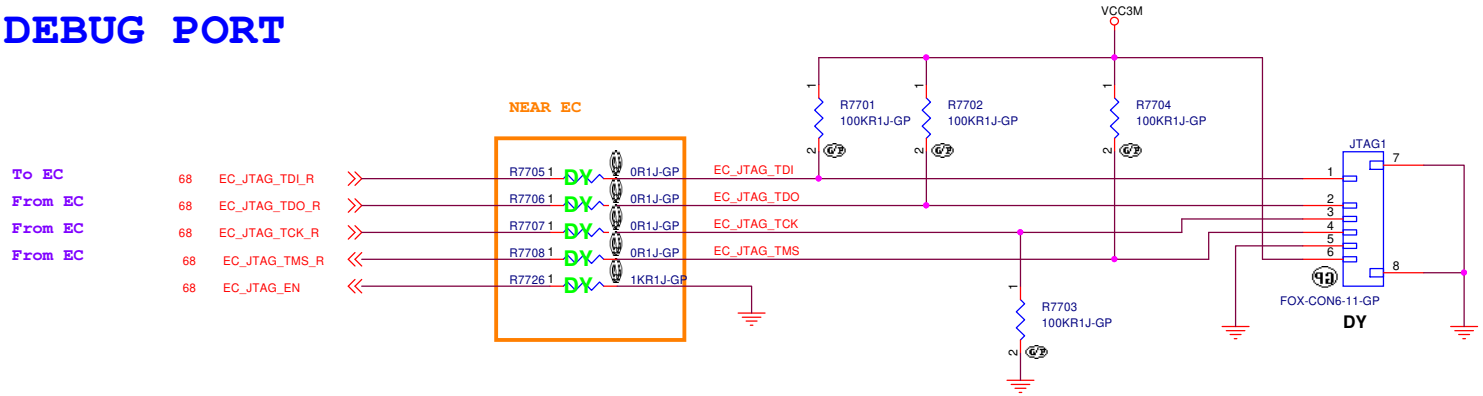
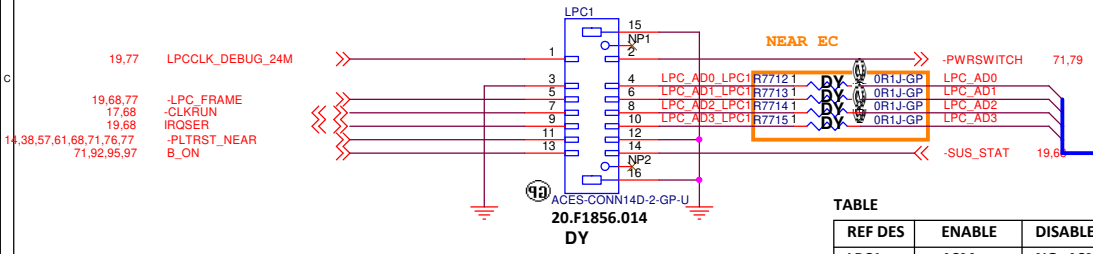
LPC DEBUG PORT



Lenovo Debug Tool I/F

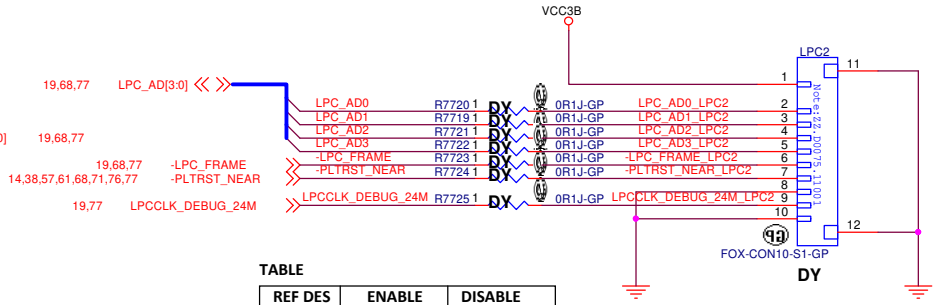


TABLE

REF DES	ENABLE	DISABLE
LPC1	ASM	NO_ASM
R7712	ASM	NO_ASM
R7713	ASM	NO_ASM
R7714	ASM	NO_ASM
R7715	ASM	NO_ASM

LOGIC

Wistron LPC for Debug Card CONN

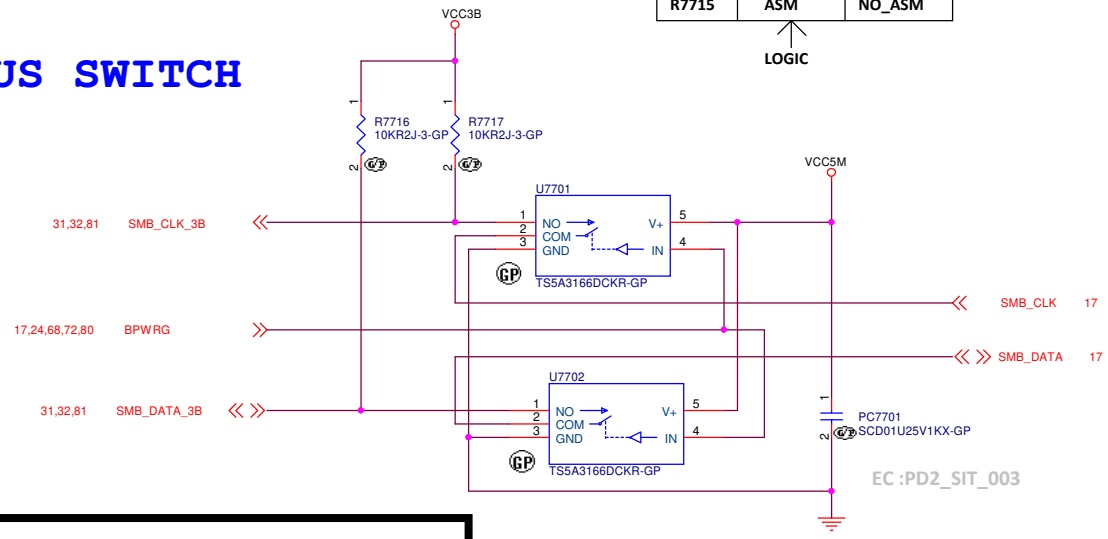


TABLE

REF DES	ENABLE	DISABLE
R7719	ASM	NO_ASM
R7720	ASM	NO_ASM
R7721	ASM	NO_ASM
R7722	ASM	NO_ASM
R7723	ASM	NO_ASM
R7724	ASM	NO_ASM
R7725	ASM	NO_ASM

LOGIC

SMBUS SWITCH



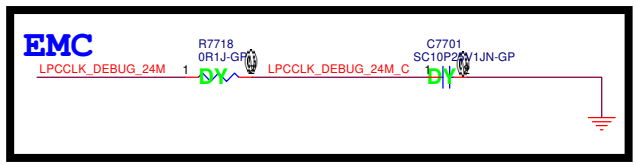


TABLE of U7701 U7702		
VENDOR	P/N	Wistron P/N
TI	TS5A3166DCKR-GP	073.53166.0A0G
ON	7SB385DFT2G	073.7S385.000G

緯創資通 Wistron Corporation
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Title: SMBUS SWITCH/LPC DEBUG PORT

Size: A3 | Document Number: LPM-2 | Rev: -1

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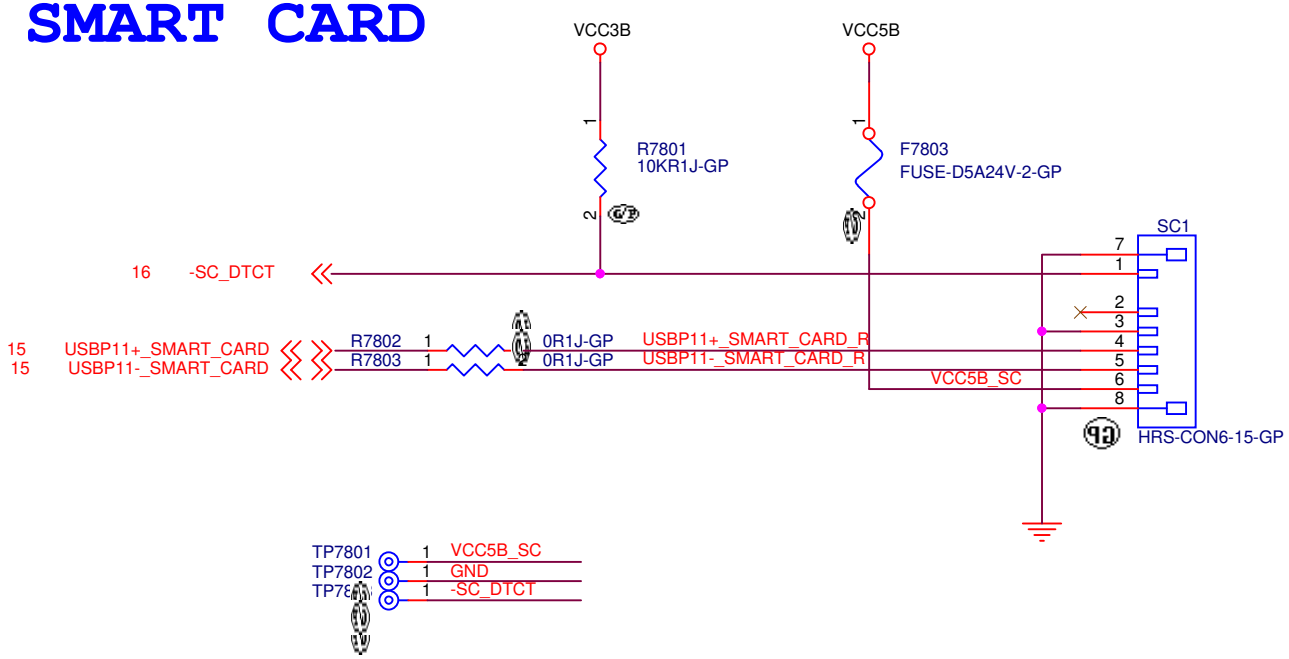
SMART CARD



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Title: ***SMART CARD***		
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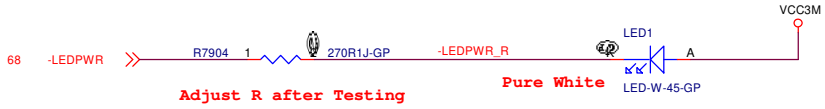
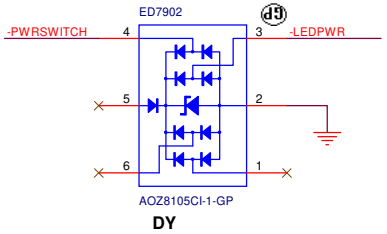
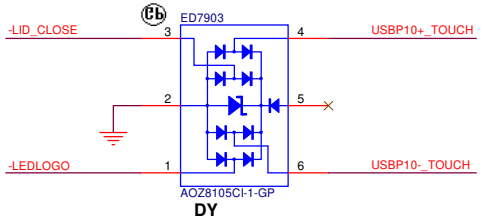
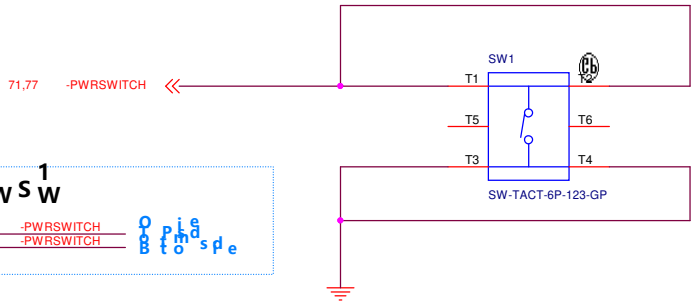
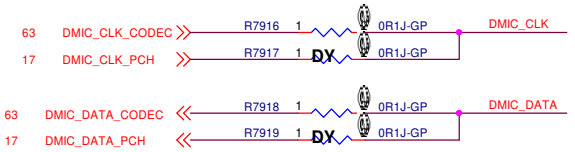
PWR BUTTON

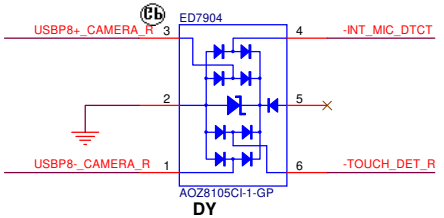


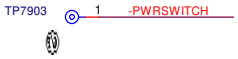




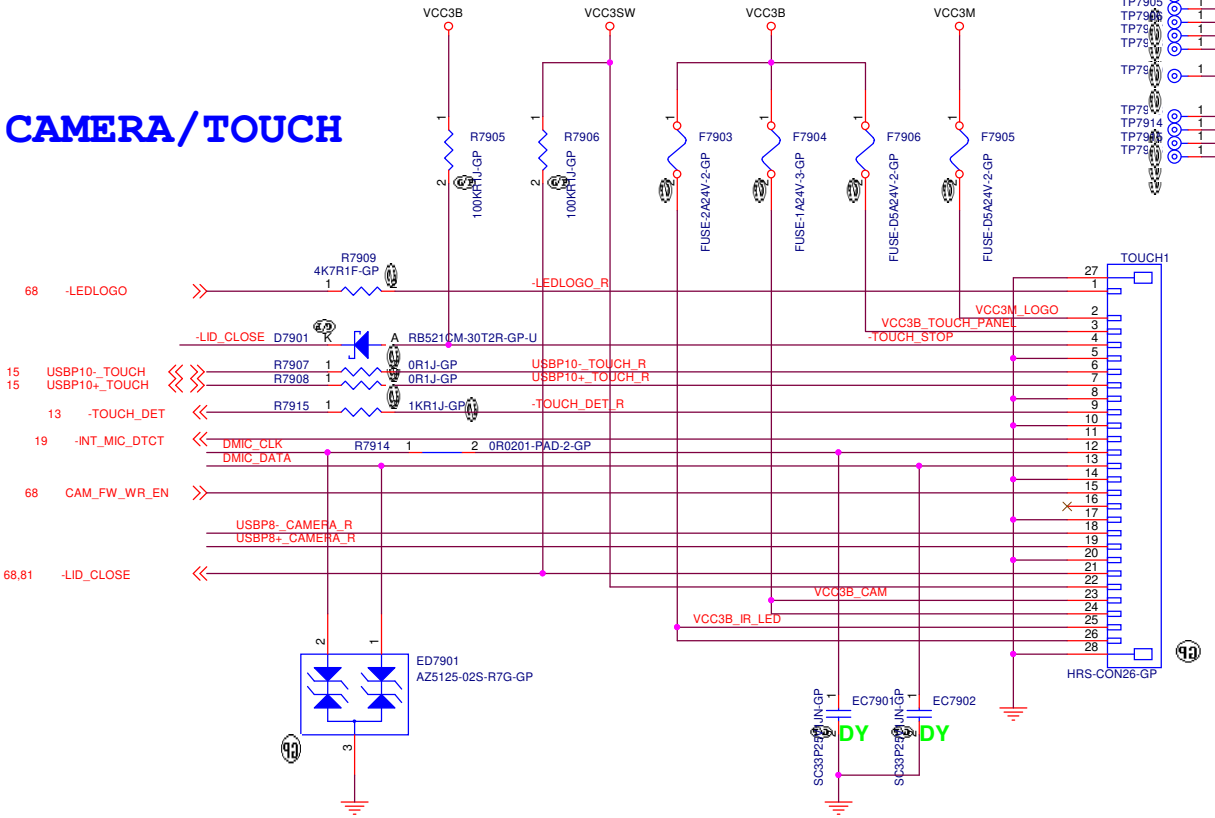


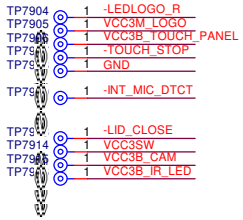


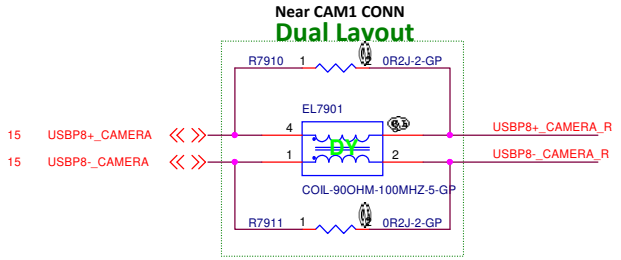




CAMERA/TOUCH







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Title: CAMERA/TOUCH/PWR BUTTON

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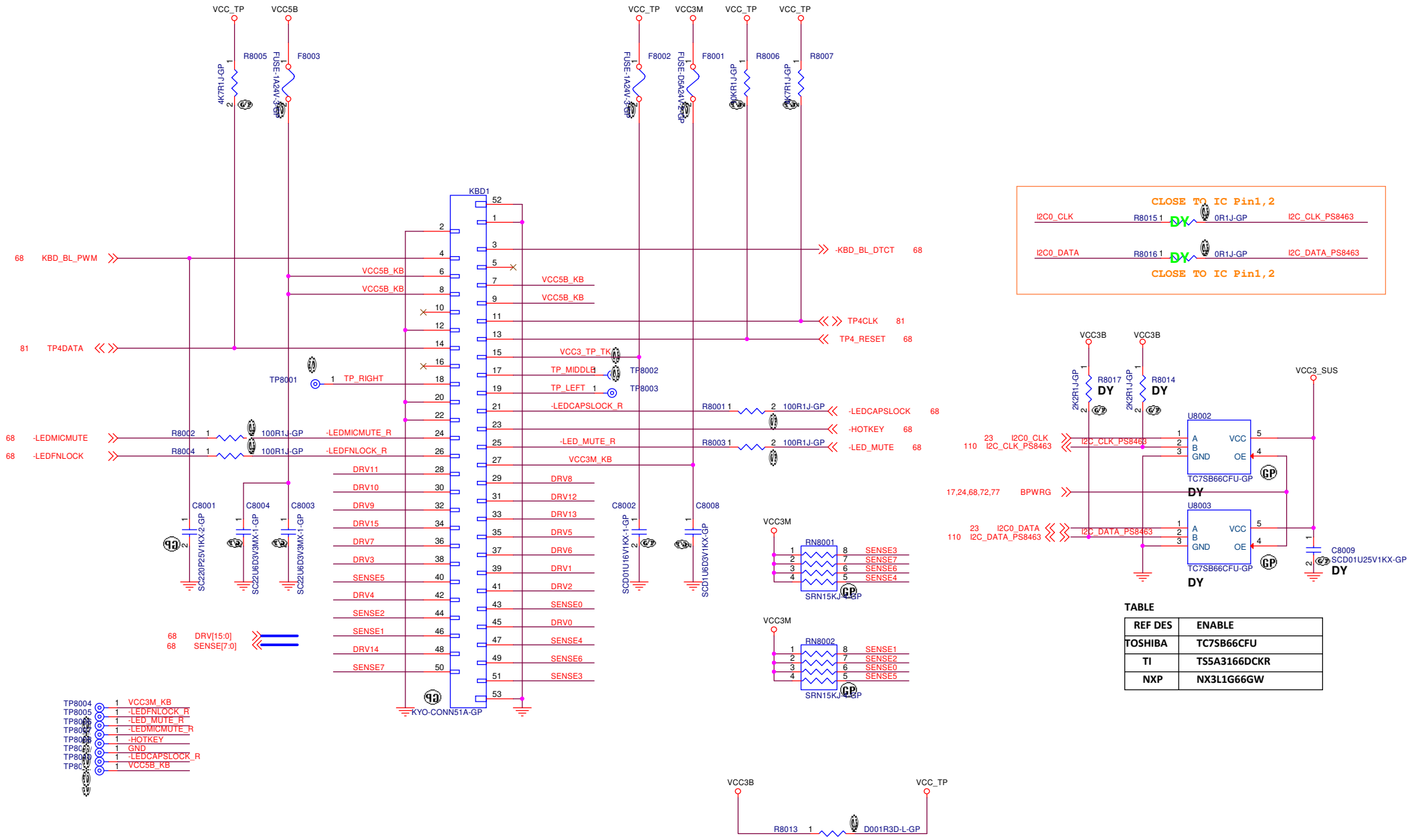

TABLE

REF DES	ENABLE
TOSHIBA	TC7SB66CFU
TI	TS5A3166DCKR
NXP	NX3L1G66GW

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Title: **KEYBOARD/TRACK POINT**

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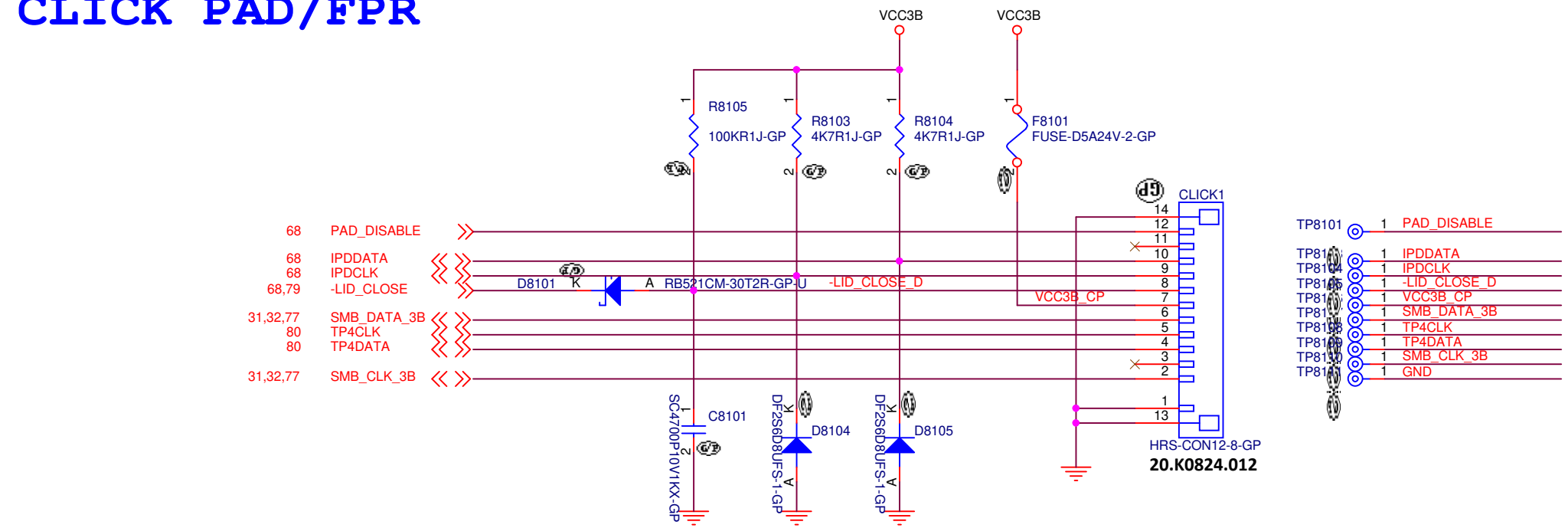
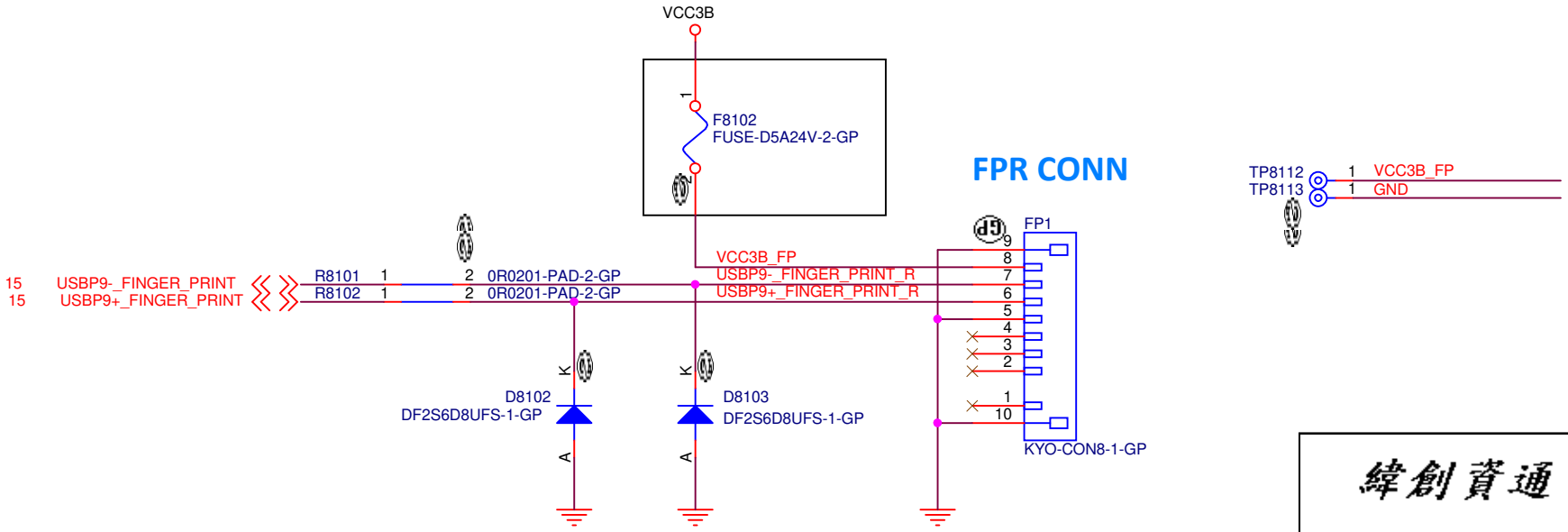
CLICK PAD/FPR





緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CLICK PAD/FPR***

Size	Document Number	Rev
A4	**LPM-2**	-1

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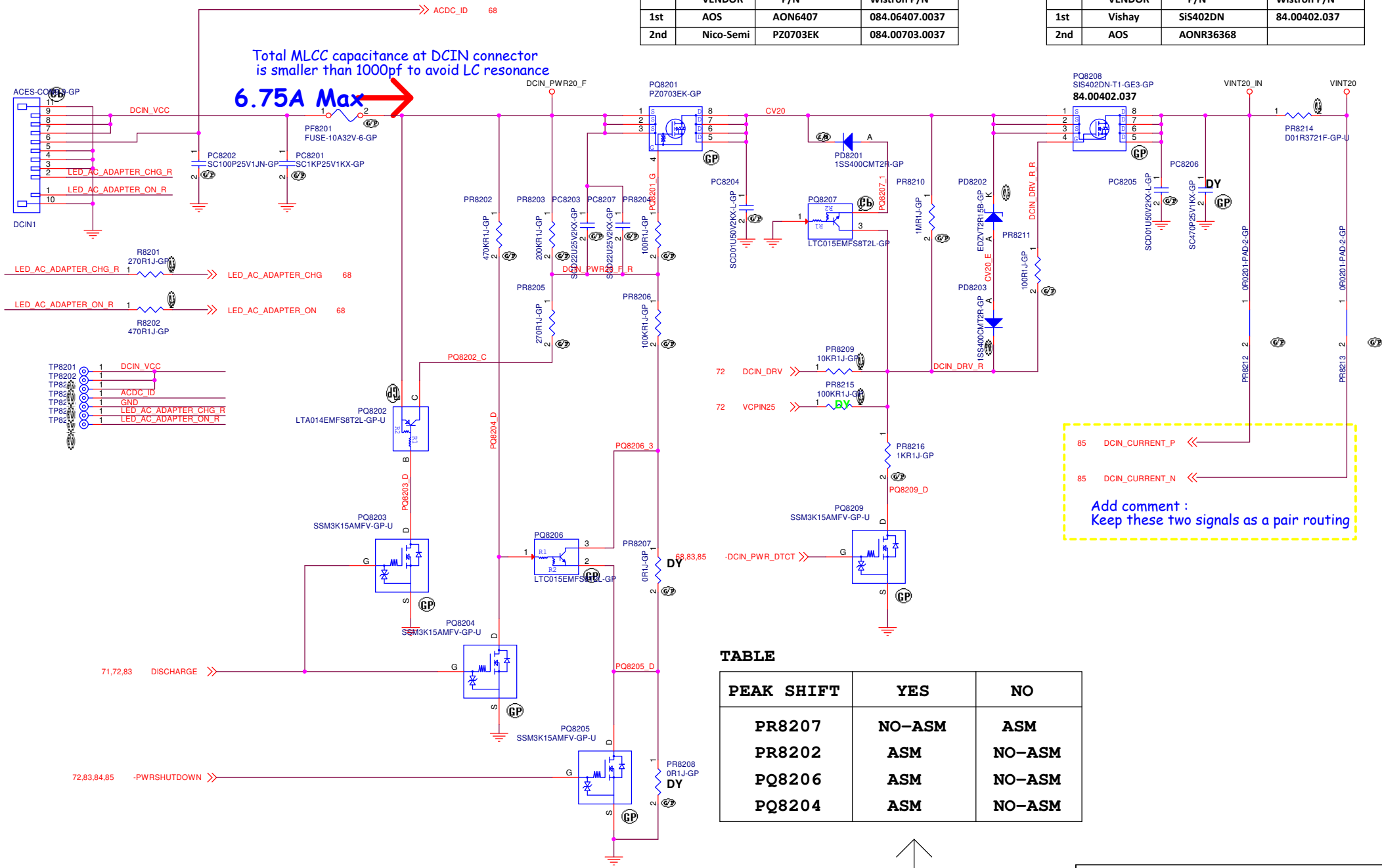
TABLE of PQ8201			
	VENDOR	P/N	Wistron P/N
1st	AOS	AON6407	084.06407.0037
2nd	Nico-Semi	PZ0703EK	084.00703.0037

TABLE of PQ8208			
	VENDOR	P/N	Wistron P/N
1st	Vishay	SiS402DN	84.00402.037
2nd	AOS	AONR36368	



TABLE

PEAK SHIFT	YES	NO
PR8207	NO-ASM	ASM
PR8202	ASM	NO-ASM
PQ8206	ASM	NO-ASM
PQ8204	ASM	NO-ASM

LOGIC

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Title: DC-IN

Size: A3 | Document Number | Rev

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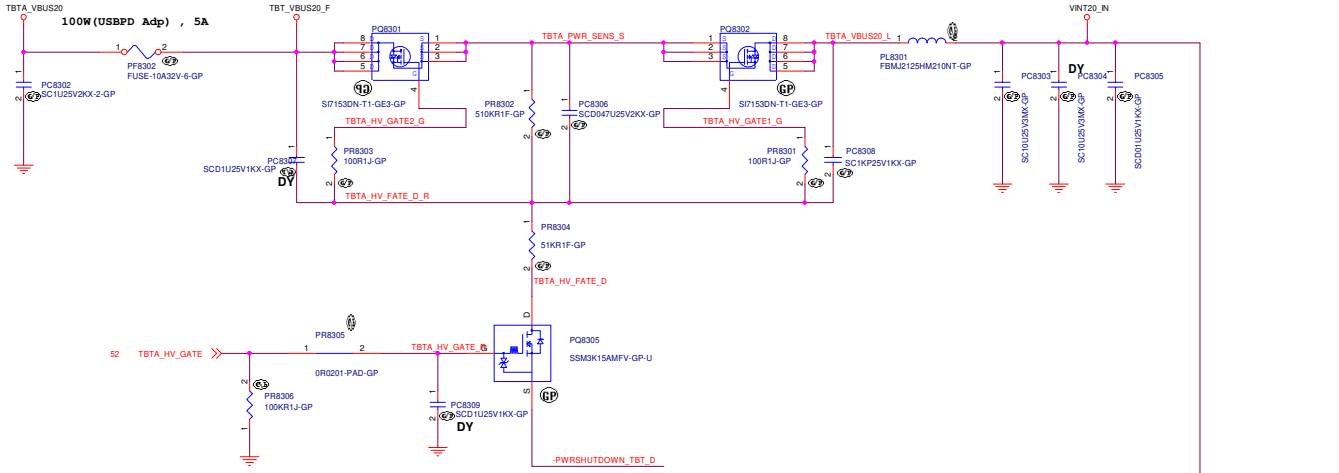
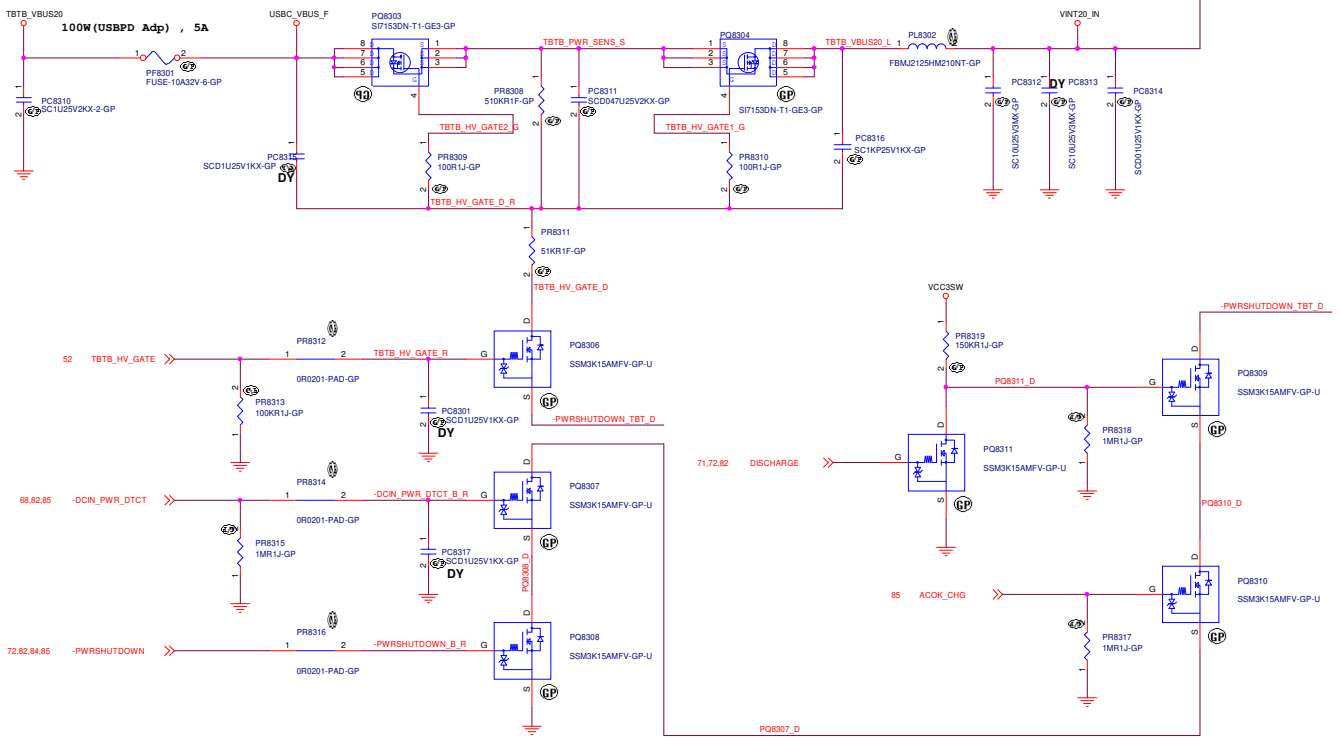
	PQ8301, PQ8302, PQ8303, PQ8304		
1st	Vishay	SI7153DN	084.07153.0037
2nd	AOS	AONR21357	084.21357.0A37

	PL8301, PL8302
1st	FBMJ2125HM210NT 068.00046.0061
2nd	





緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DC-IN		
Size A2	Document Number		Rev
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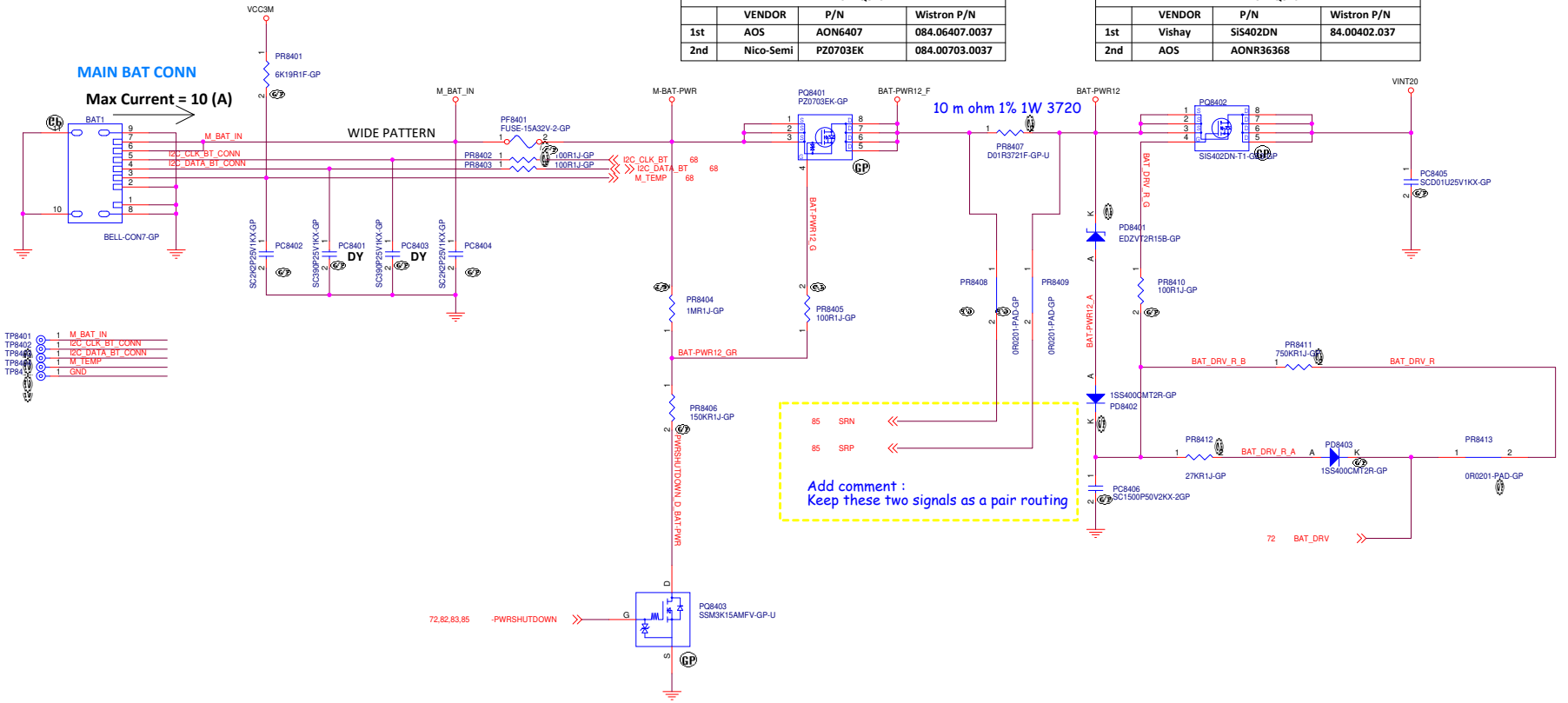
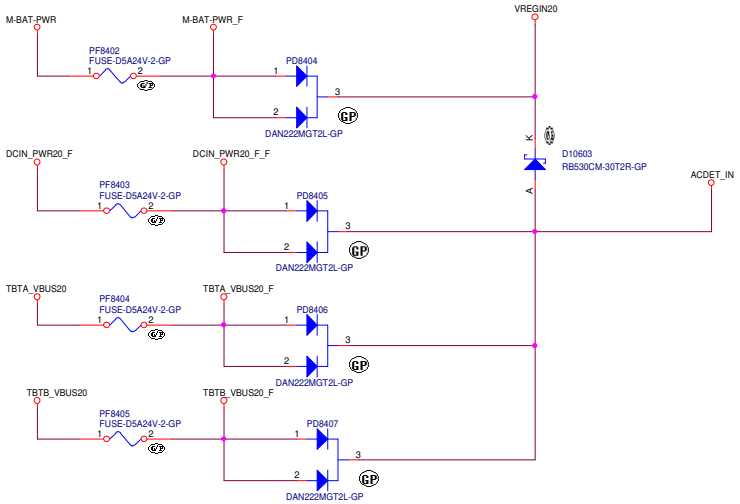
TABLE of PQ8401			
	VENDOR	P/N	Wistron P/N
1st	AOS	AON6407	084.06407.0037
2nd	Nico-Semi	PZ0703EK	084.00703.0037

TABLE of PQ8402			
	VENDOR	P/N	Wistron P/N
1st	Vishay	SiS402DN	84.00402.037
2nd	AOS	AONR36368	





Title	BATTERY INPUT
Size	C
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Rev	
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Taipei Hsien 221, Taiwan, R.O.C.

TABLE of PQ8507			
	VENDOR	P/N	Wistron P/N
1st	AOS	AON6407	084.06407.0037
2nd	Nico-Semi	PZ0703EK	084.00703.0037

PQ8502		
1st	Infineon BSC0923NDI 075.00923.M001	
2nd	AOS	AONY36354

MLCCs (input capacitors at charger)
must placed symmetrically on TOP and BOTTOM side

PL8501
CYNTEC CMLE063T-2R2MS 0.68.2R210.1881
TOKO FDSD0630-H-2R2M

MLCCs (output capacitors as charger) must placed symmetrically on TOP and BOTTOM side

Charge Current Max 5.0A

Add comment :
Keep these two signals as a pair routing

Put PC8510, PC8511, PC8512, PC8514, PR8504, PR8506, PR8501 and PR8505 close to IC side

Add comment :
Keep these two signals as a pair routing

EC86

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BATTERY CHARGER
Size	A2
Document Number	LPM-2
Rev	-1
Date:	Tuesday, April 30, 2019
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keep more than 2.0mm height for
if acoustic noise suppression MLCC use

Add comment :
MLCCs (Input capacitiors at charger)
must placed symmetrically on TOP and BOTTOM side

	PQ8601
1st	Infineon BSC0923NDI 75.00923.073
2nd	AOS AONY36354

Dual-N standard symbol to colay

VCC5M
Cont 11.1A
Max 12.6A
Peak 13.3A

Table PL8601
TDK SPM6530T-1R0M120 68.1R01A.11A
CYNTEC CMLE063T-1R0MS 068.R1010.1081

	PT8601 PT8602 PT8603
1st	Panasonic 6TPE220MAPB 77.22271.39L
2nd	KEMET T520B227M006ATE025 077.C2271.0041
3rd	TOKIN PSLB20J227M25LQ

PR8621	VCC5M
154K Ohm	5.08 V
158K Ohm	5.16 V
162K Ohm	5.24 V

Add comment :
Current Limit1
25.1A (17.5A - 38.1A)

Add comment :
Current Limit2
23.7A (16.9A - 35A)

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

	PQ8602
1st	Infineon BSC0923NDI 75.00923.073
2nd	AOS AONY36354

Add comment :
MLCCs (Input capacitiors at charger)
must placed symmetrically on TOP and BOTTOM side

Dual-N standard symbol to colay

VCC3M
Cont 9.6A
Max 11.2A
Peak14.6A

Table PL8602
TDK SPM6530T-1R0M120 68.1R01A.11A
CYNTEC CMLE063T-1R0MS 068.R1010.1081

	PT8604 PT8605 PT8606
1st	Panasonic 6TPE220MAPB 77.22271.39L
2nd	KEMET T520B227M006ATE025 077.C2271.0041
3rd	TOKIN PSLB20J227M25LQ

PR8622	VCC3M
130K Ohm	3.30 V
133K Ohm	3.33 V
137K Ohm	3.37 V

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Title: DC/DC VCC5M/VCC3M
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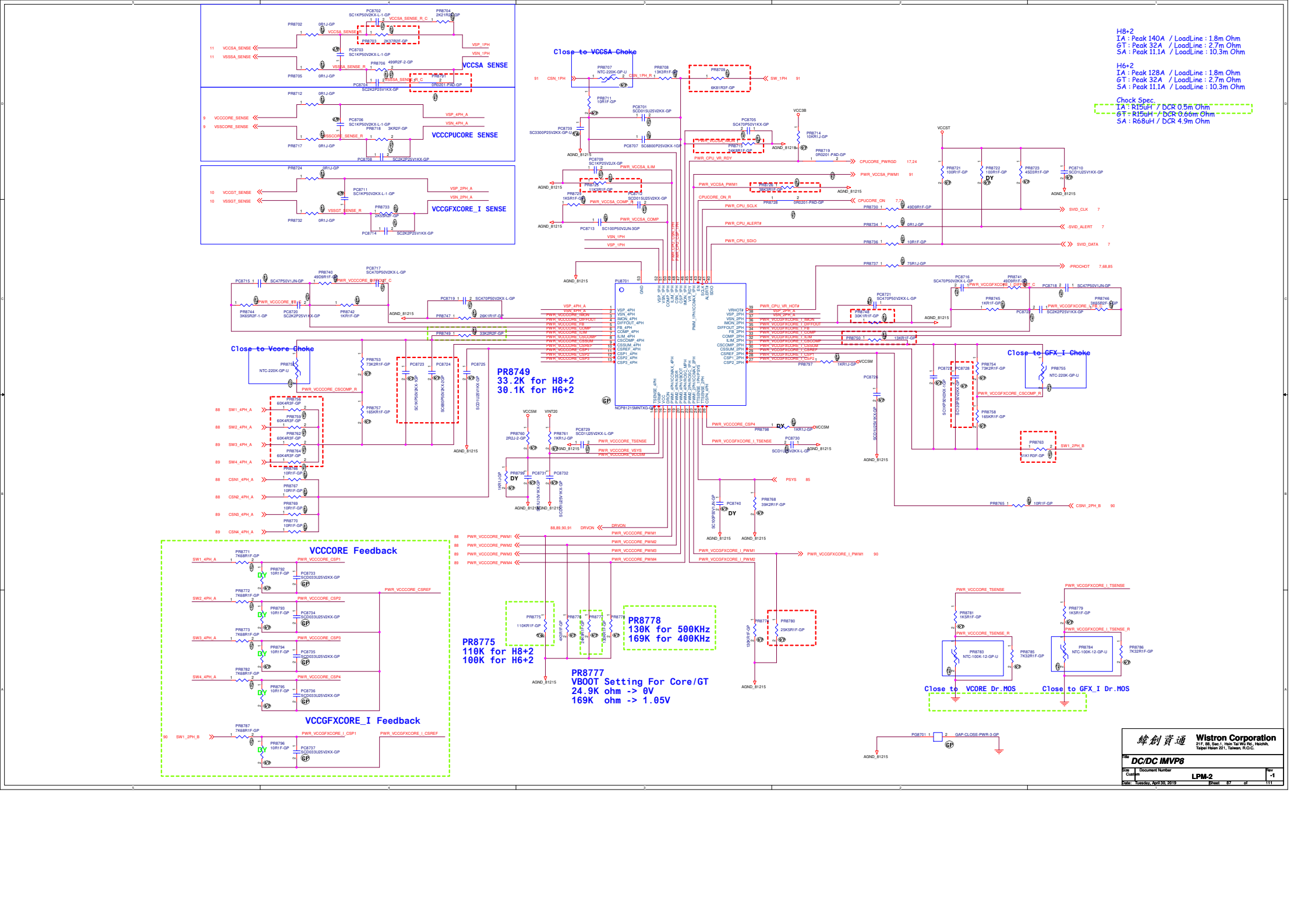
H8+2
IA : Peak 140A / LoadLine : 1.8m Ohm
GT : Peak 32A / LoadLine : 2.7m Ohm
SA : Peak 11.1A / LoadLine : 10.3m Ohm
H6+2
IA : Peak 128A / LoadLine : 1.8m Ohm
GT : Peak 32A / LoadLine : 2.7m Ohm
SA : Peak 11.1A / LoadLine : 10.3m Ohm
Chock Spec.
IA : R15uH / DCR 0.5m Ohm
GT : R15uH / DCR 0.66m Ohm
SA : R68uH / DCR 4.9m Ohm
VCCSA SENSE
VCCCPUCORE SENSE
VCCGFXCORE_I SENSE
Close to VCCSA Choke
Close to Vcore Choke
Close to GFX_I Choke
PR8749
33.2K for H8+2
30.1K for H6+2
PR8775
110K for H8+2
100K for H6+2
PR8778
130K for 500KHz
169K for 400KHz
PR8777
VBOOT Setting For Core/GT
24.9K ohm -> 0V
169K ohm -> 1.05V
VCCCORE Feedback
VCCGFXCORE_I Feedback
Close to VCORE Dr.MOS
Close to GFX_I Dr.MOS
NCP81215MNTXG-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC/DC IMVP8
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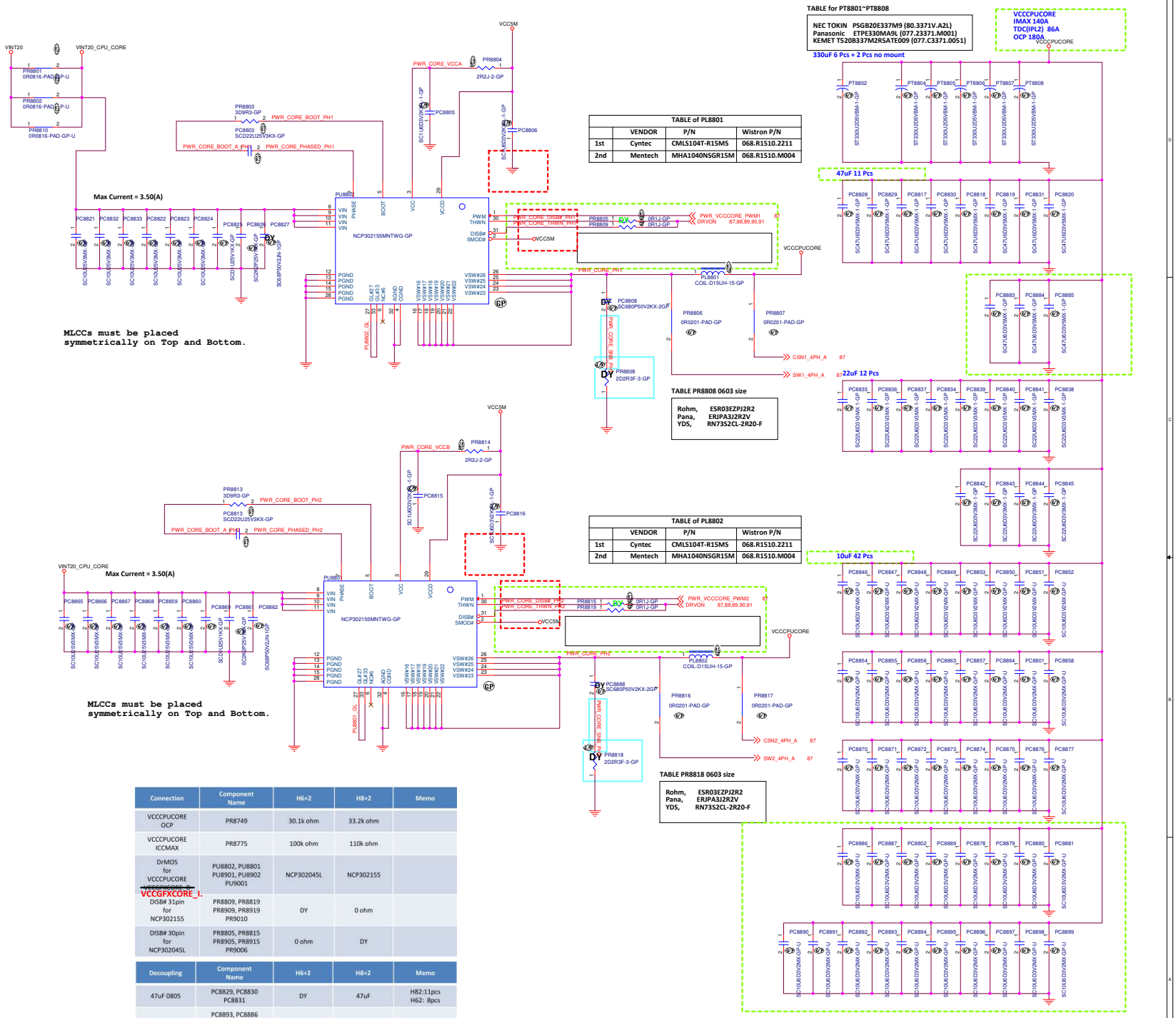

Connection	Component Name	H6+2	H8+2	Memo
VCCCPUCORE OCP	PR8749	30.1k ohm	33.2k ohm	
VCCCPUCORE ICCMAX	PR8775	100k ohm	110k ohm	
DrMOS for VCCCPUCORE ~~VCCGFXCORE_0~~ VCCGFXCORE_I.	PU8802, PU8801 PU8901, PU8902 PU9001	NCP302045L	NCP302155	
DISB# 31pin for NCP302155	PR8809, PR8819 PR8909, PR8919 PR9010	DY	0 ohm	
DISB# 30pin for NCP302045L	PR8805, PR8815 PR8905, PR8915 PR9006	0 ohm	DY	

Decoupling	Component Name	H6+2	H8+2	Memo
47uF 0805	PC8829, PC8830 PC8831	DY	47uF	H82:11pcs H62: 8pcs
10uF 0402	PC8893, PC8886 PC8895, PC8887 PC8890, PC8897 PC8891, PC8802 PC8899, PC8896 PC8894, PC8892 PC8889, PC8898	DY	10uF	H82:42pcs H62:28pcs

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Title: DC/DC VCCCPUCORE (1/2)

Size: Custom | Document Number | Rev

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VCCCPUCORE
IMAX 140A
TDC(IPL2) 86A
OCP 180A

1uF 63 Pcs

TABLE of PL8901			
	VENDOR	P/N	Wistron P/N
1st	Cyntec	CMLS104T-R15MS	068.R1510.2211
2nd	Mentech	MHA1040NSGR15M	068.R1510.M004

Max Current = 3.50(A)

MLCCs must be placed symmetrically on Top and Bottom.

TABLE PR8906 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

TABLE of PL8902			
	VENDOR	P/N	Wistron P/N
1st	Cyntec	CMLS104T-R15MS	068.R1510.2211
2nd	Mentech	MHA1040NSGR15M	068.R1510.M004

Max Current = 3.50(A)

MLCCs must be placed symmetrically on Top and Bottom.

TABLE PR8916 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

This circuit is for Hexa core.
Please refer to the table in next page.

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Title: DC/DC VCCCPUCORE (2/2)
Size: C | Document Number: LPM-2 | Rev: -1
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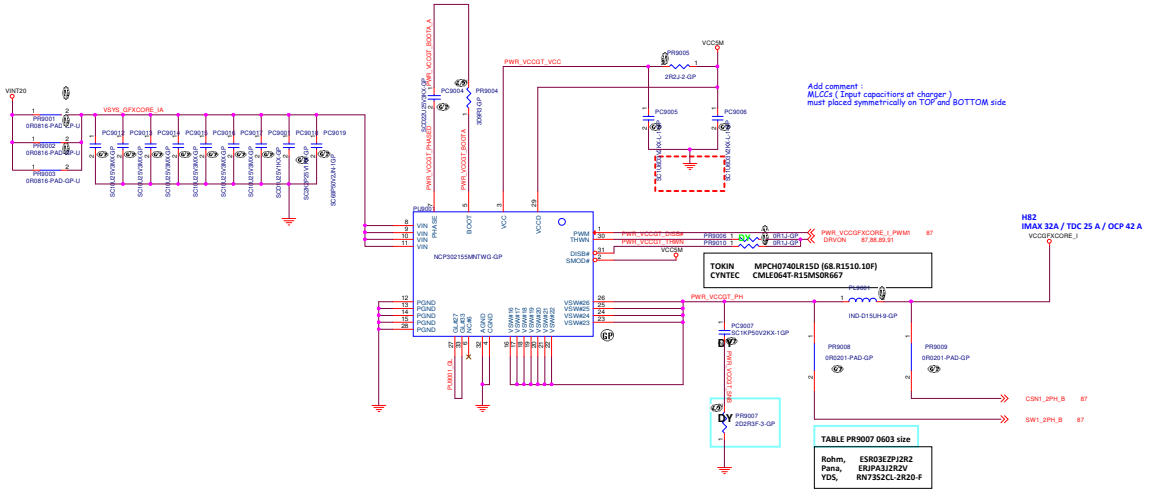


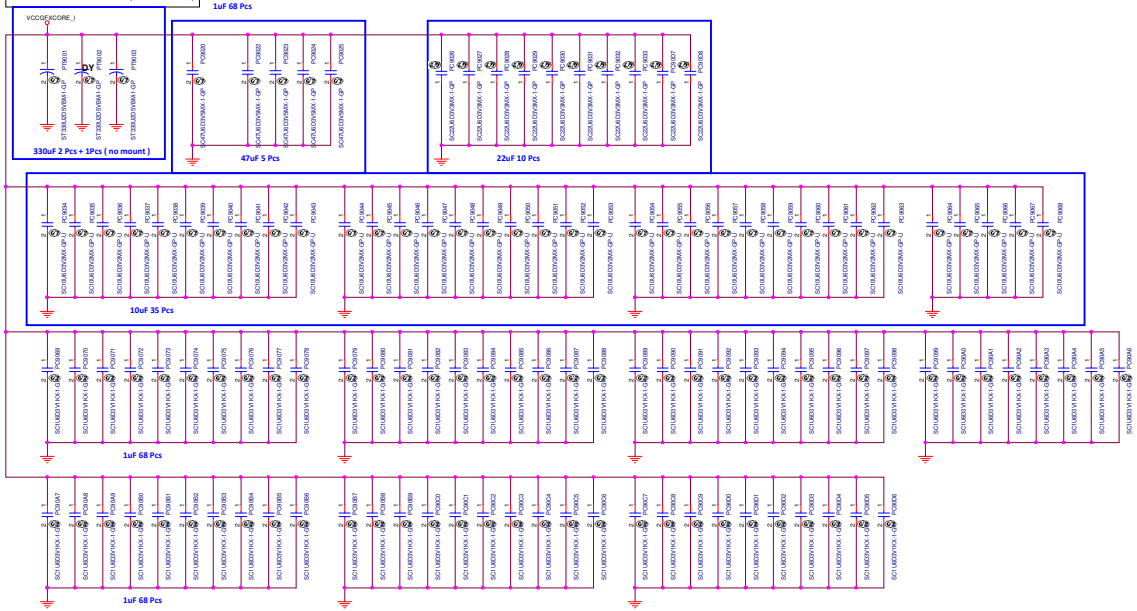
TABLE

Connection	Component Name	CPU-H Hexa	CPU-H Quad	Unit	memo
PWR_VCCCORE_ILIM to PWR_VCCCORE_CSCOMP	PR8749	30.1	20.0	Kohm	128Ax1.3 v.s 86Ax1.3
PWR_VCCCORE_PWM1 to AGND_81215	PR8775	100	68.1	Kohm	128A v.s 86A
SW4_4PH_A to PWR_VCCCORE_CSSUM	PR8764	60.4	No asm	Kohm	4phase v.s 3phase
CSN4_4PH_A to PWR_VCCCORE_CSREF	PR8770	10	No asm	ohm	4phase v.s 3phase
SW4_4PH_A to PWR_VCCCORE_CSP4	PR8782	7.68	No asm	Kohm	4phase v.s 3phase
PWR_VCCCORE_CSP4 to PWR_VCCCORE_CSREF	PC8736	0.033	No asm	uF	4phase v.s 3phase
PWR_VCCCORE_CSP4 to VCCSM	PR8798	No asm	1	Kohm	4phase v.s 3phase
PWR_VCCCORE_PWM4	PU8902	asm	No asm	____	4phase v.s 3phase
VCCSM to PWR_CORE_VCCD	PR8914	2.2	No asm	ohm	4phase v.s 3phase
PWR-CORE_VCCD to GND	PC8911	1	No asm	uF	4phase v.s 3phase
VCCSM to AGND_81215	PC8912	1	No asm	uF	4phase v.s 3phase
PWR_CORE_BOOT_PH4 to PWR_CORE_BOOT_A_PH4	PR8913	3.9	No asm	ohm	4phase v.s 3phase
PWR_CORE_BOOT_A_PH4 to PWR_CORE_PHASED_PH	PC8913	0.22	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8993	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8994	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8995	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8996	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8997	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8998	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8990	0.1	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8991	2200	No asm	pF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8992	2200	No asm	pF	4phase v.s 3phase
PWR_CORE_DISB#_PH4 to DRVON	PR8915	0	No asm	ohm	4phase v.s 3phase
VCCCPUCORE to PWR_CORE_PH4	PL8902	0.15	No asm	uH	4phase v.s 3phase
PWR_CORE_PH4 to SW4_4PH_A	PR8917	0	No asm	ohm	4phase v.s 3phase
VCCCPUCORE to CSN4_4PH_A	PR8918	0	No asm	ohm	4phase v.s 3phase

TABLE for PT9001, PT9002, PT9003

NEC TOKIN PSGB20E337M9 (80.3371V.A2L)
Panasonic ETPE330MA9L (No Wistron P/N)
KEMET T520B337M2R5ATE009 (077.C3371.0051)

330uF 2 Pcs + 1Pcs (no mount)
47uF 6 Pcs
22uF 8 Pcs
10uF 35 Pcs
1uF 68 Pcs



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Title: DC/DC VCCGFXCORE_I(NCP302045)

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MLCCs must be placed
symmetrically on Top and Bottom.

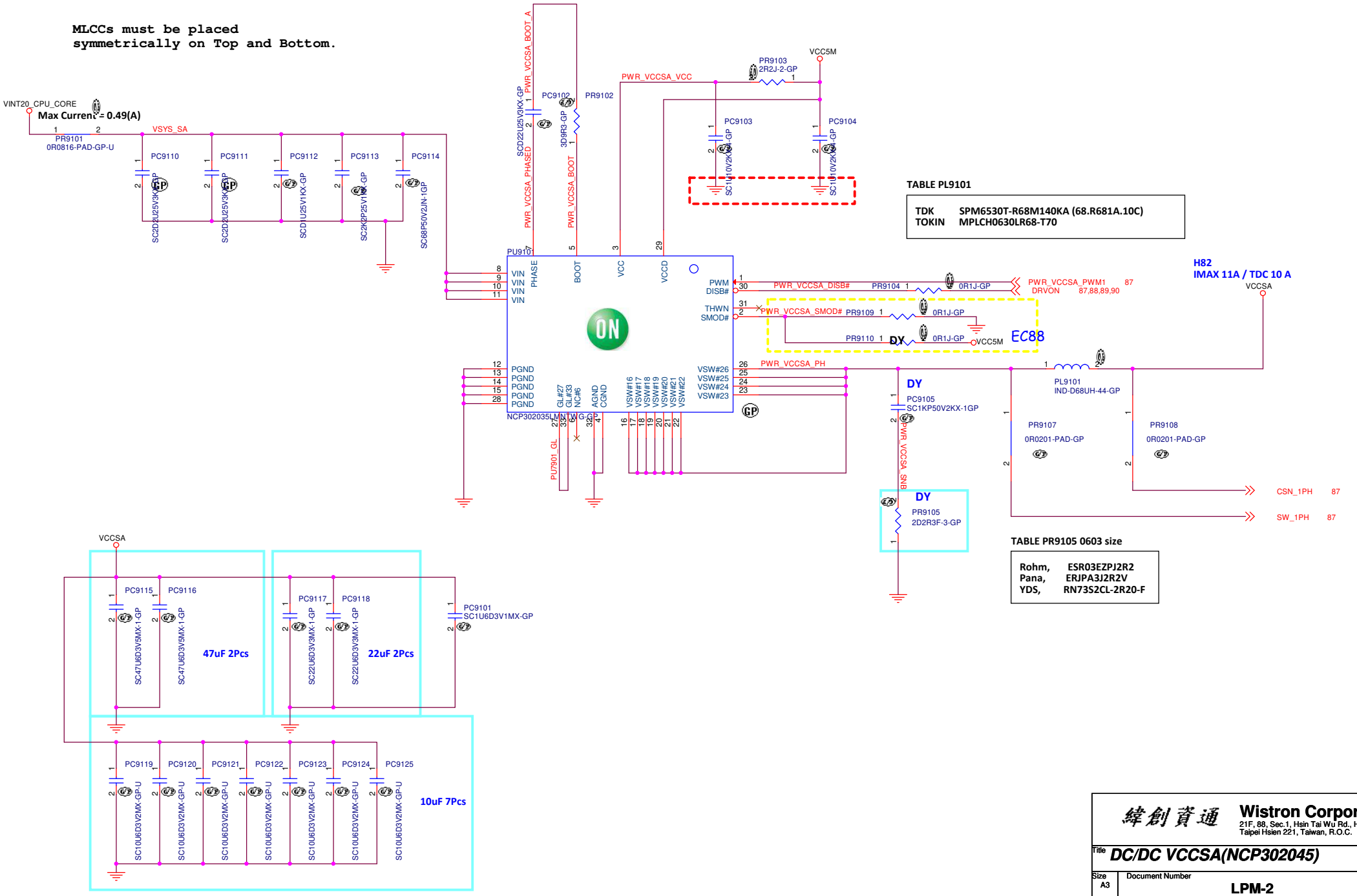

TABLE PL9101

TDK	SPM6530T-R68M140KA (68.R681A.10C)
TOKIN	MPLCH0630LR68-T70

TABLE PR9105 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

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Title: *DC/DC VCCSA(NCP302045)*

Size	Document Number	Rev
A3	LPM-2	-1

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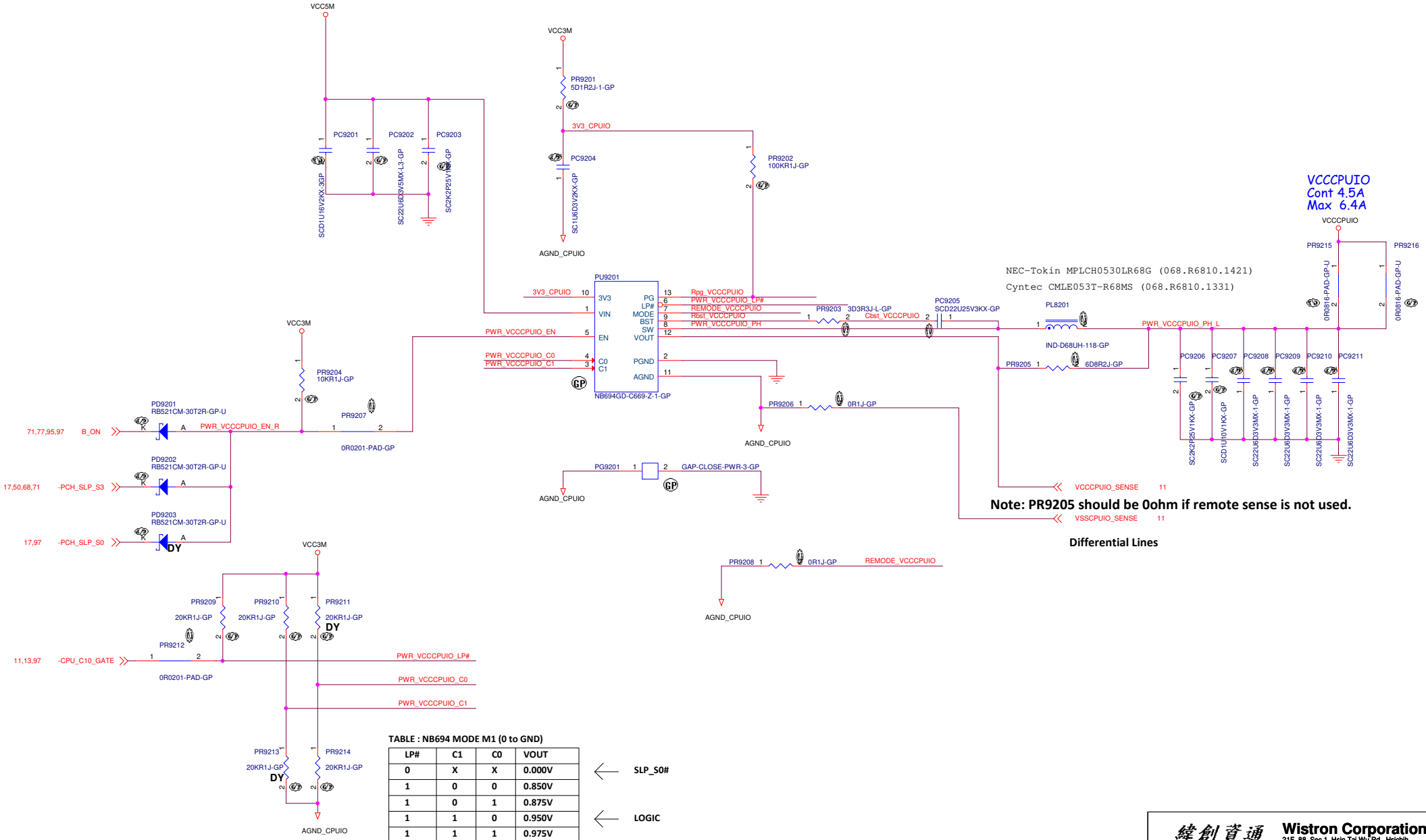

TABLE : NB694 MODE M1 (0 to GND)

LP#	C1	C0	VOUT	
0	X	X	0.000V	← SLP_S0#
1	0	0	0.850V	
1	0	1	0.875V	
1	1	0	0.950V	← LOGIC
1	1	1	0.975V	

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Title: **DC/DC VCCCPUIO**

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VCC1R05_SUS
Cont 5.7A
Max 8.1A

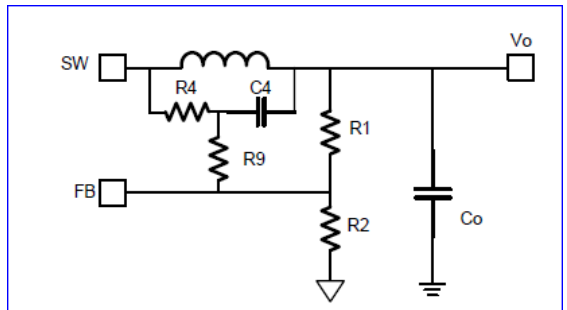
NEC-Tokin MPLCH0530LR68G (068.R6810.1421)
Cyntec CMLE053T-R68MS (068.R6810.1331)

EC 20181002

EC 20181002

EC 20181002

EC 20181002



Vo = 1.05V

R1 = 15K / R2=20K / R9=DY / Vref=0.6V
Vout = Vref x (1+R1/R2)
=0.6 x (1+15/20)
=1.05

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \cdot R_2 \qquad (4)$$

To get a pole for better noise immunity, set R9 with Equation (5):

$$R_9 \le \frac{1}{2\pi \times C_4 \times 2F_{SW}} \qquad (5)$$

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Title	DC/DC VCC1R05_SUS
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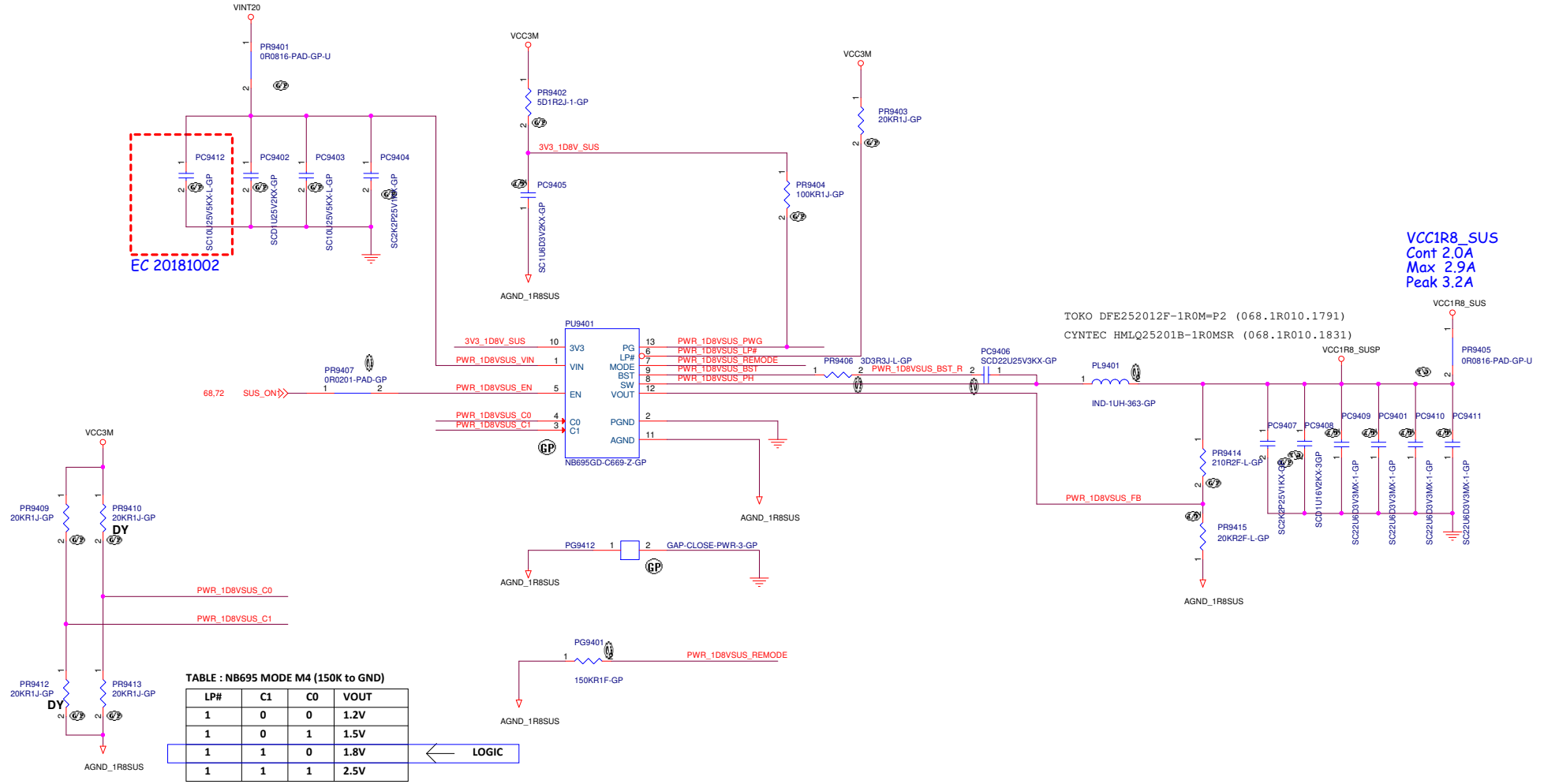

TABLE : NB695 MODE M4 (150K to GND)

LP#	C1	C0	VOUT	
1	0	0	1.2V	
1	0	1	1.5V	
1	1	0	1.8V	← LOGIC
1	1	1	2.5V	

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Title: ***DC/DC VCC1R8_SUS***

Size	Document Number	Rev
Custom	LPM-2	-1

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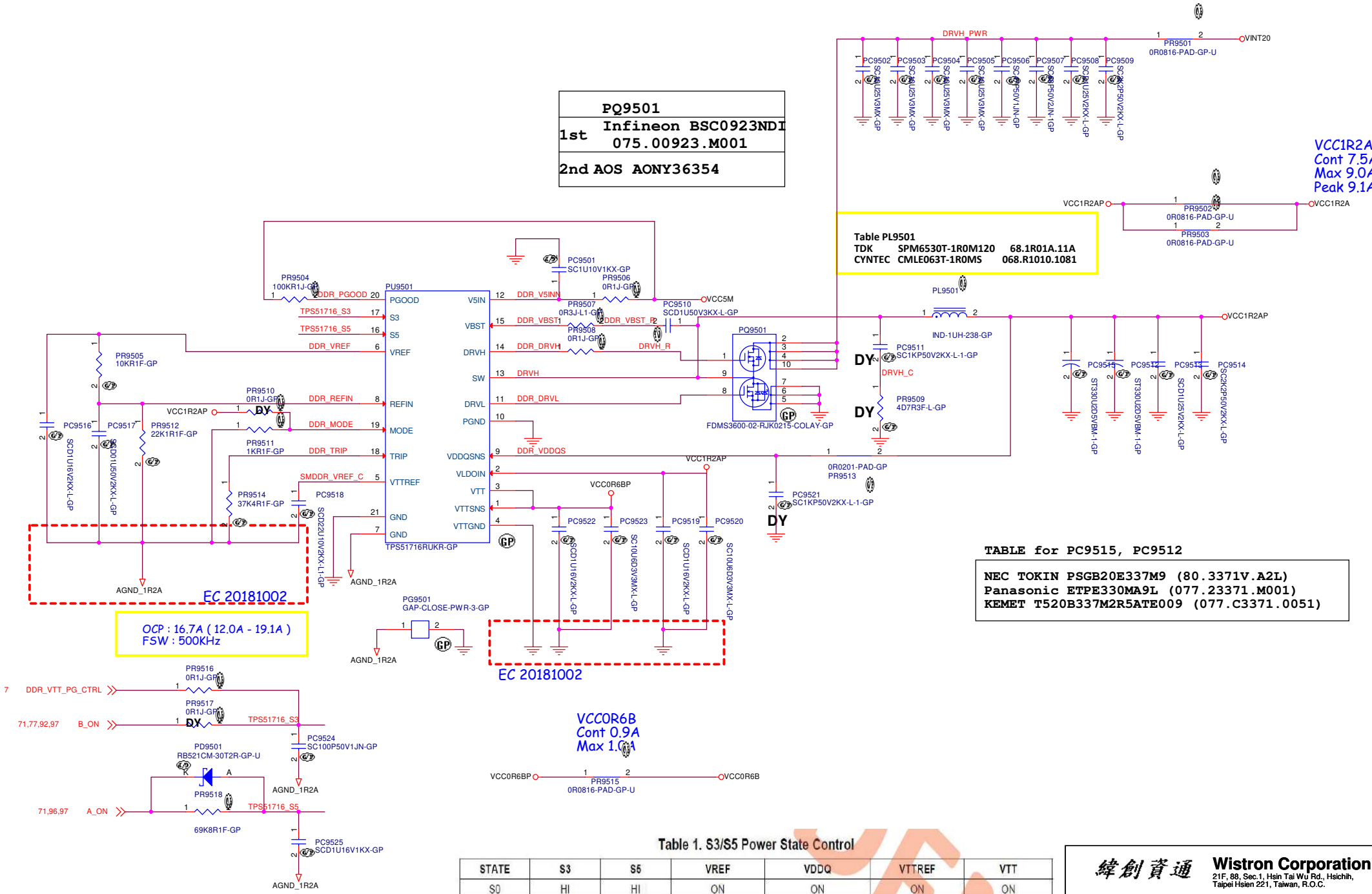

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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Title: DC/DC VCC1R2A/VCC0R6B
Size: A3 | Document Number: LPM-2 | Rev: -1
Date: Tuesday, April 30, 2019 | Sheet 95 of 111

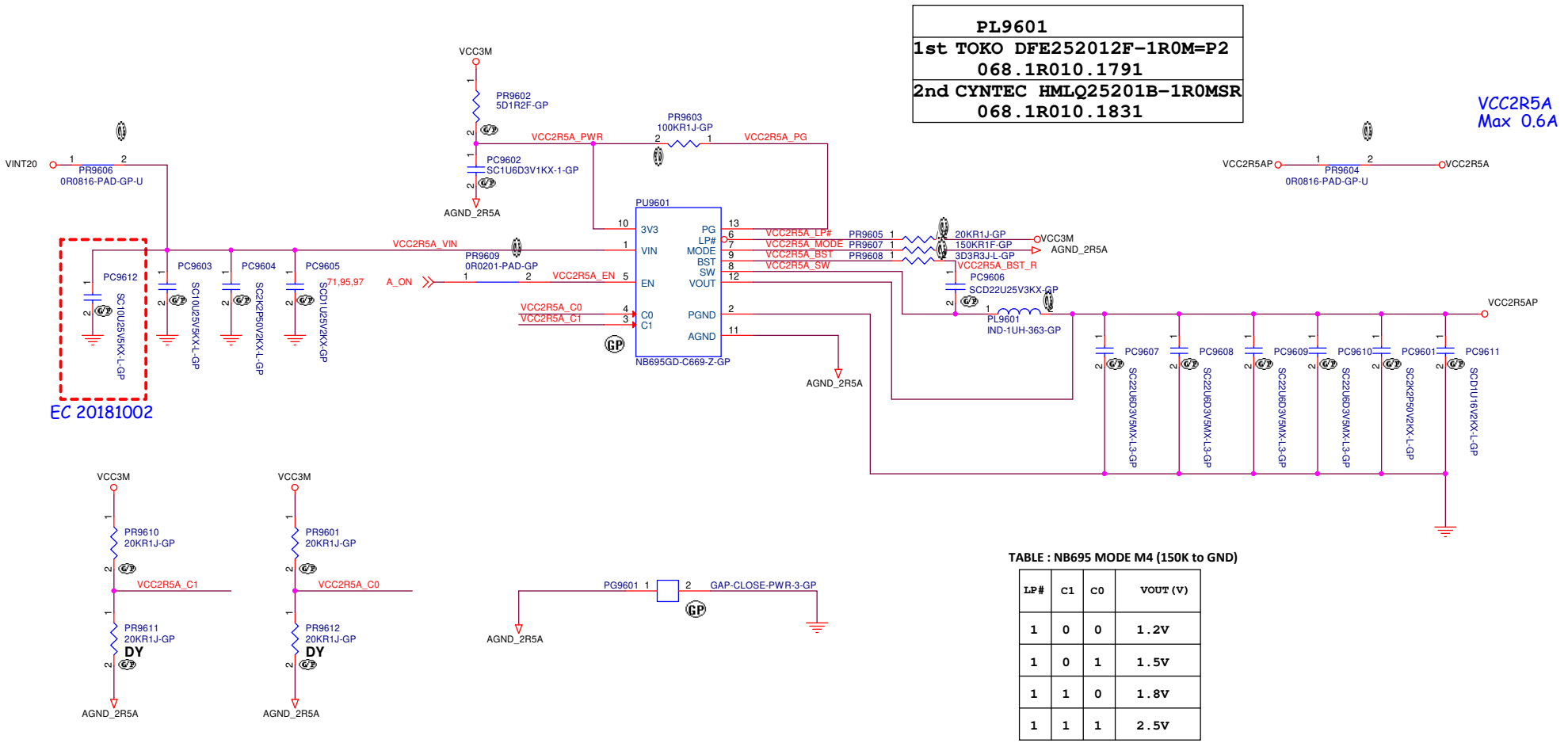

TABLE : NB695 MODE M4 (150K to GND)

LP#	C1	C0	VOUT (V)
1	0	0	1.2V
1	0	1	1.5V
1	1	0	1.8V
1	1	1	2.5V

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Title: ***DC/DC VCC2R5A***

Size	Document Number	Rev
A3	LPM-2	-1

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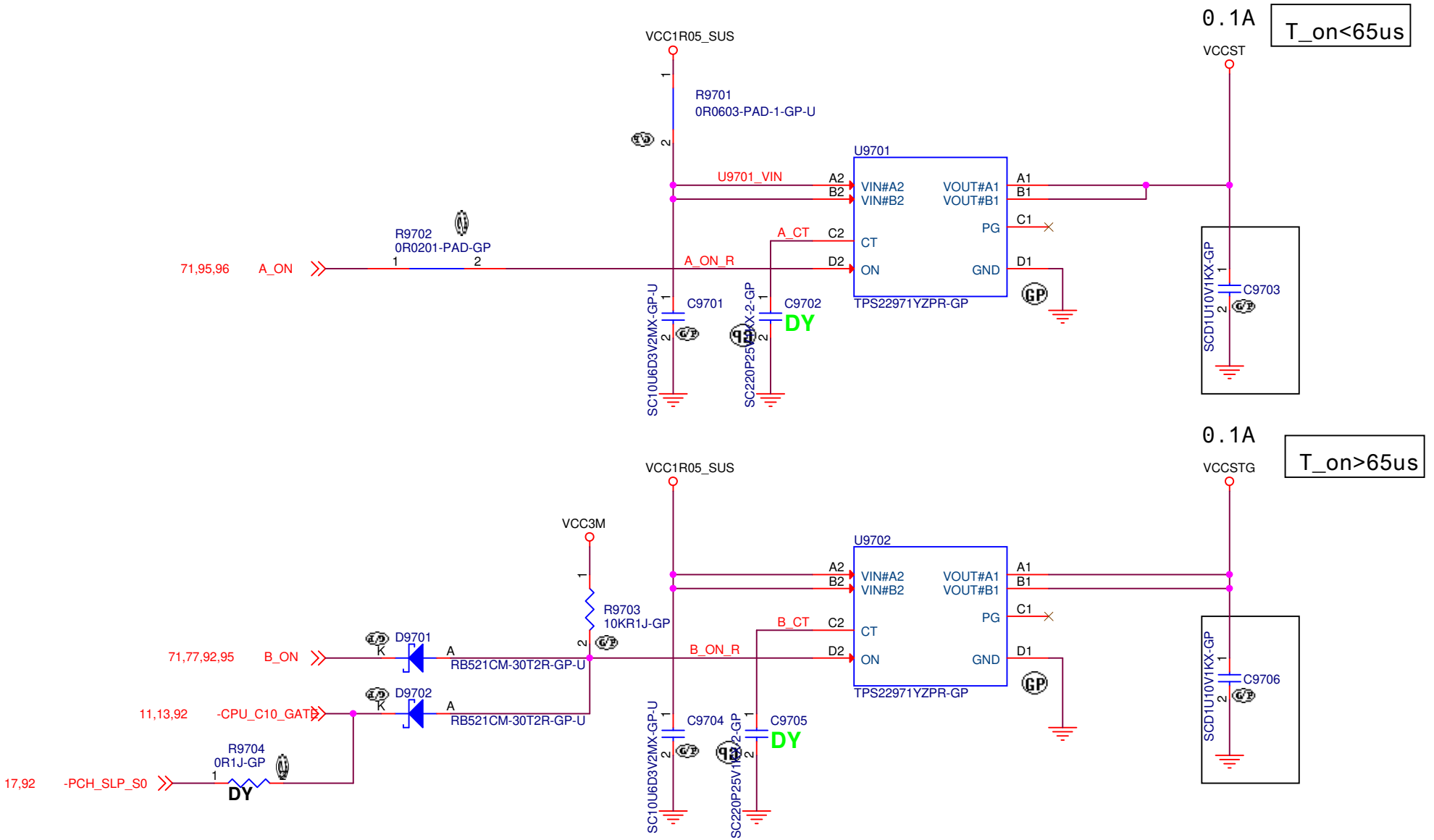

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Title: **LOAD SW VCCST/VCCSTG**

Size	Document Number	Rev
A4	LPM-2	-1

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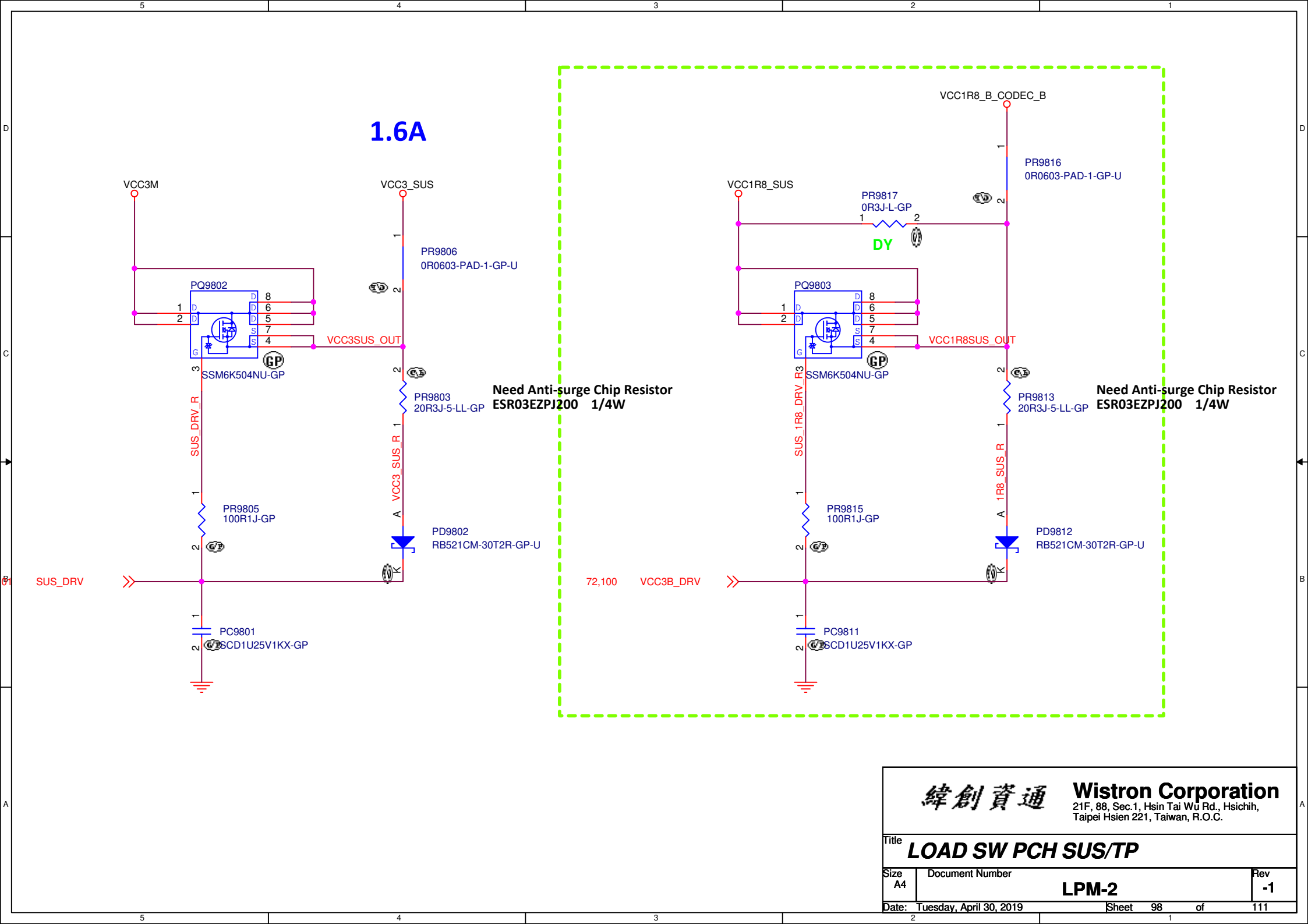

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LOAD SW PCH SUS/TP***	
Size: A4	Document Number: **LPM-2**	Rev: **-1**
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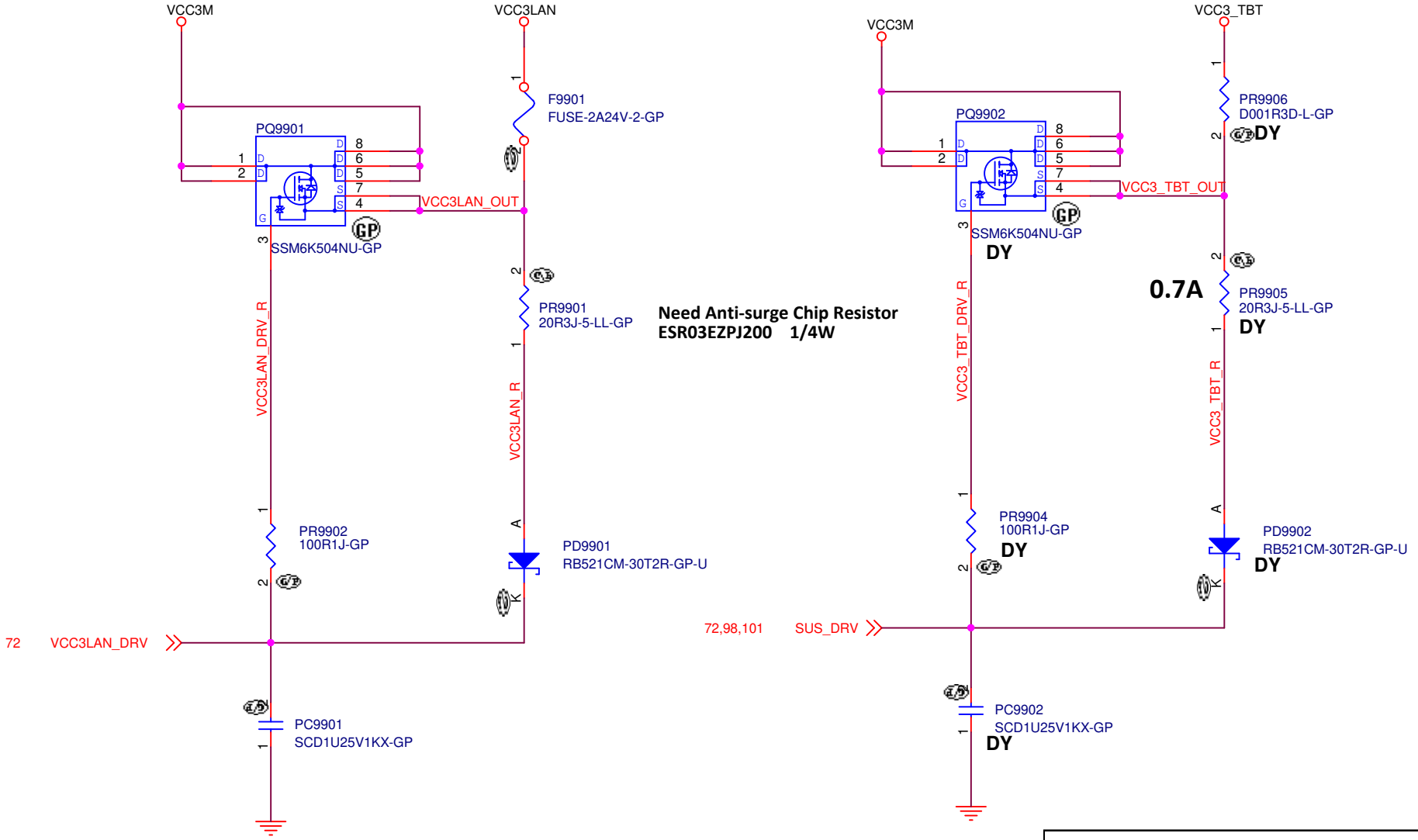
VCC3LAN

0.25A



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LOAD SW LAN/VCC3_TBT***	
Size: A4	Document Number: **LPM-2**	Rev: **-1**
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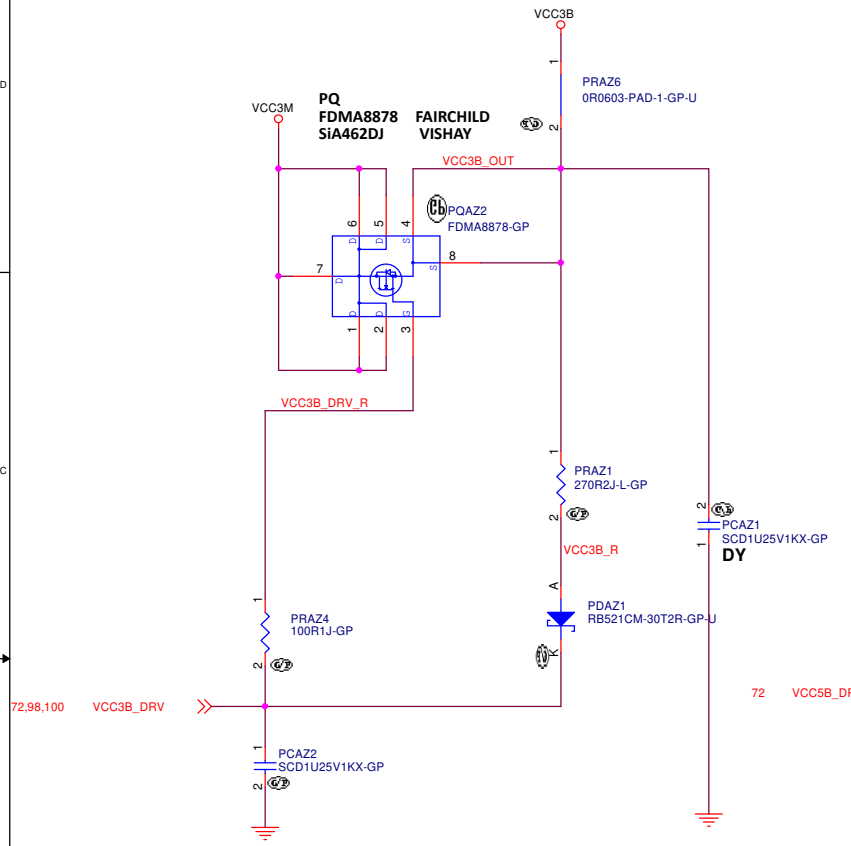
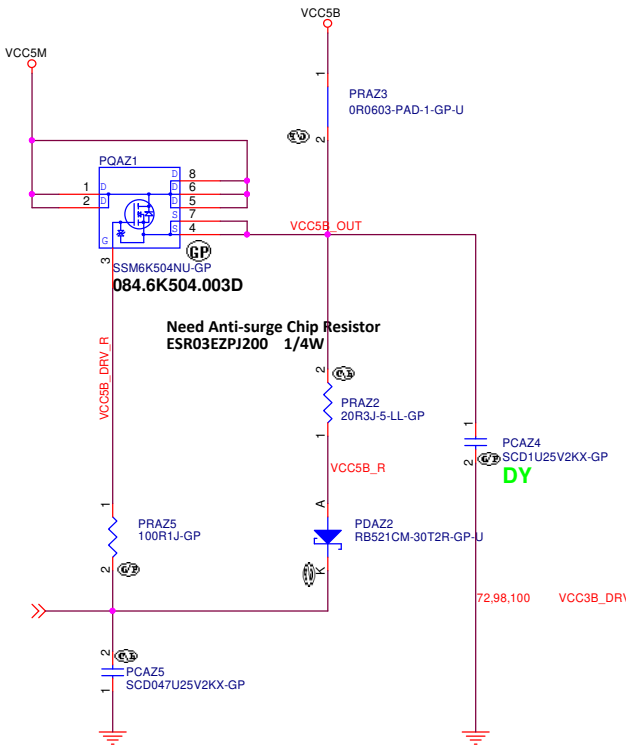
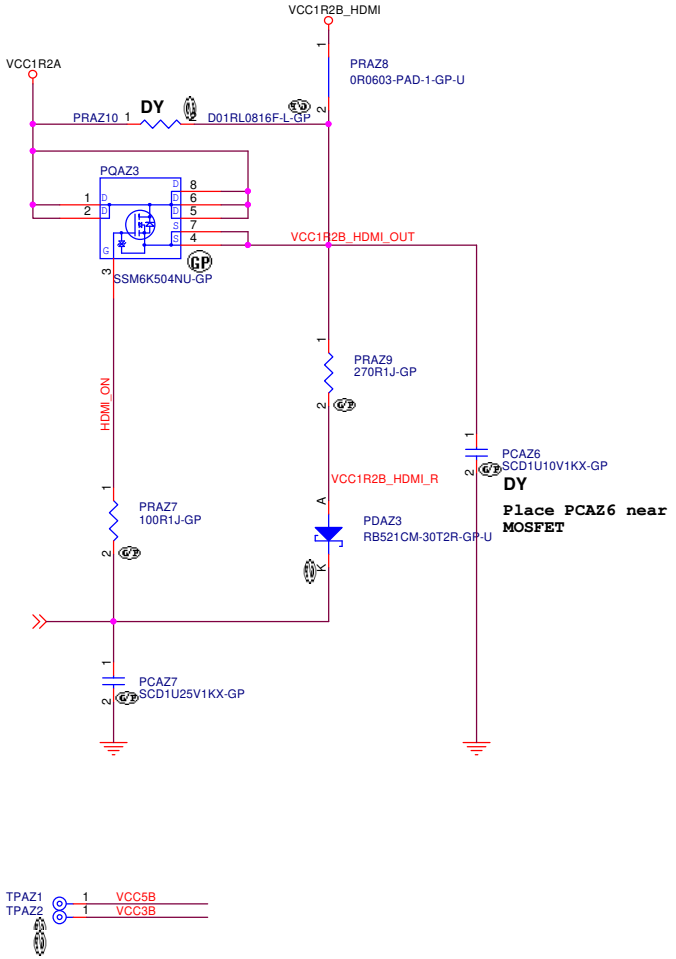
VCC3B
Max Current = 7.4 (A)



VCC5B
Max Current = 1.9 (A)



HDMI
Max Current = 1.7 (A)



TPAZ1 1 VCC5B
TPAZ2 1 VCC3B

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Title	LOAD SW B	
Size: A3	Document Number: LPM-2	Rev: -1
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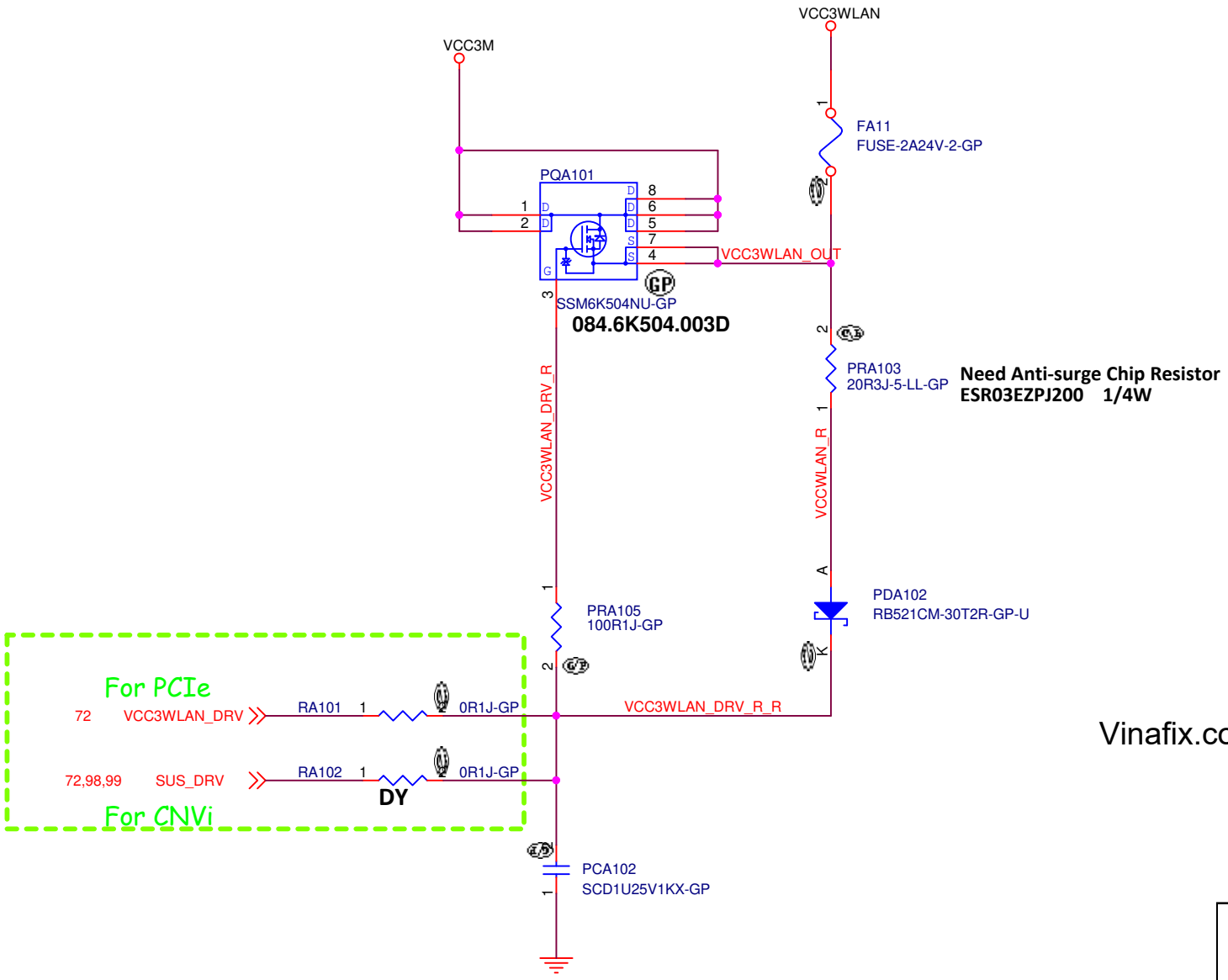
WLAN

1.1A



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Title	***LOAD SW WLAN***	
Size: A4	Document Number: **LPM-2**	Rev: **-1**
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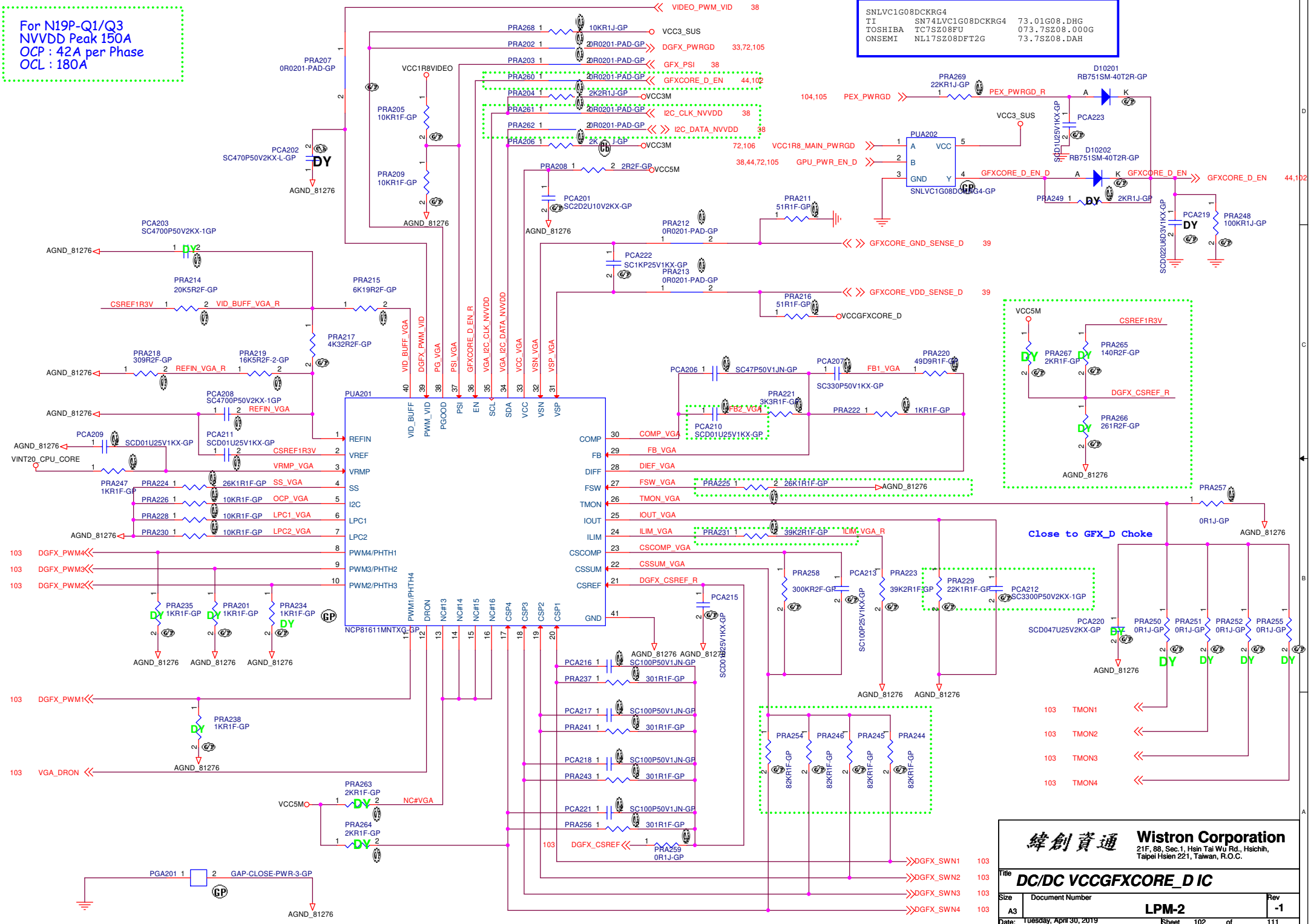
For N19P-Q1/Q3
NVVDD Peak 150A
OCP : 42A per Phase
OCL : 180A

SNLVC1G08DCKRG4		
TI	SN74LVC1G08DCKRG4	73.01G08.DHG
TOSHIBA	TC7SZ08FU	073.7SZ08.000G
ONSEMI	NL17SZ08DFT2G	73.7SZ08.DAH



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Title: DC/DC VCCGFXCORE_D IC

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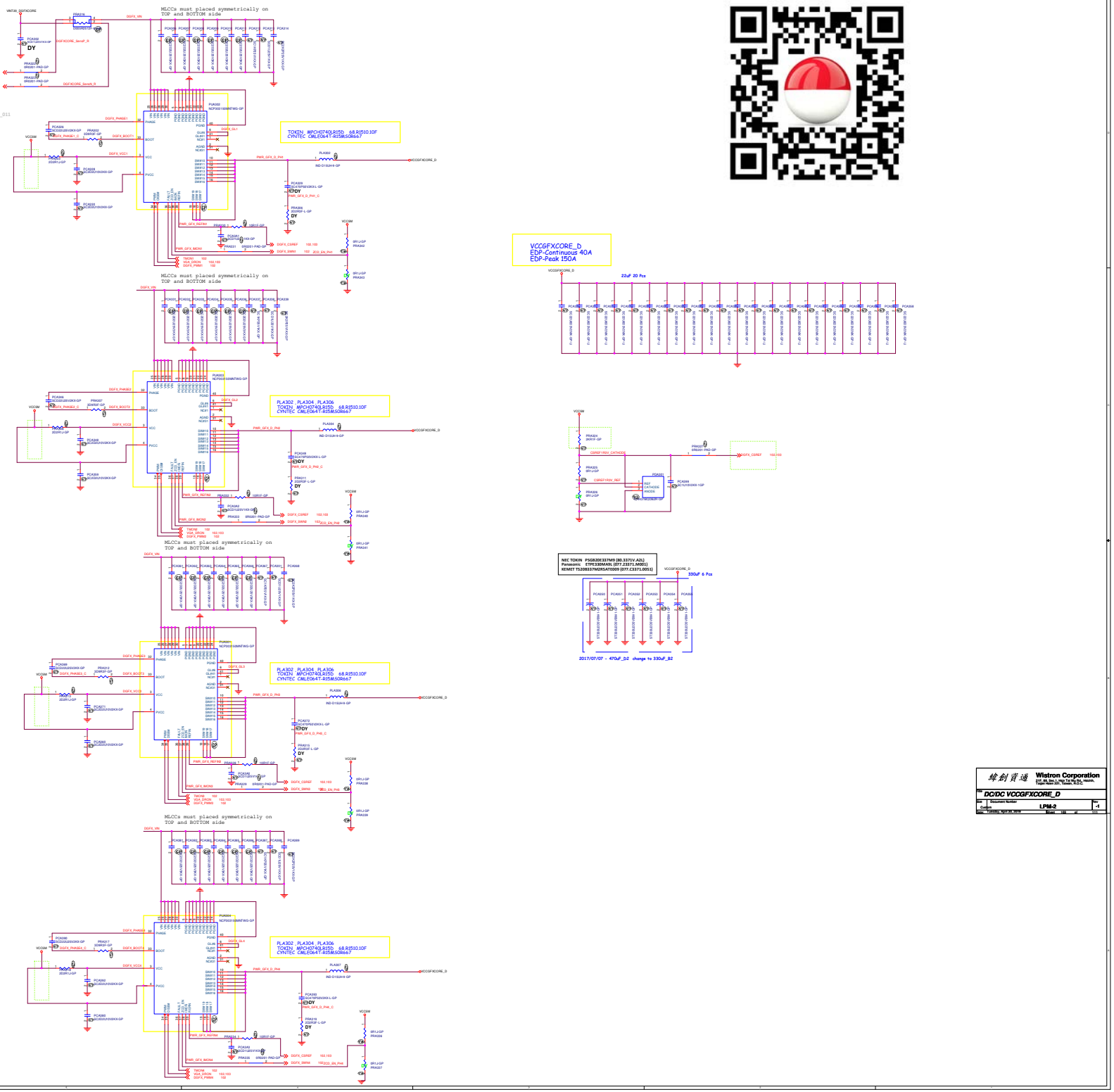
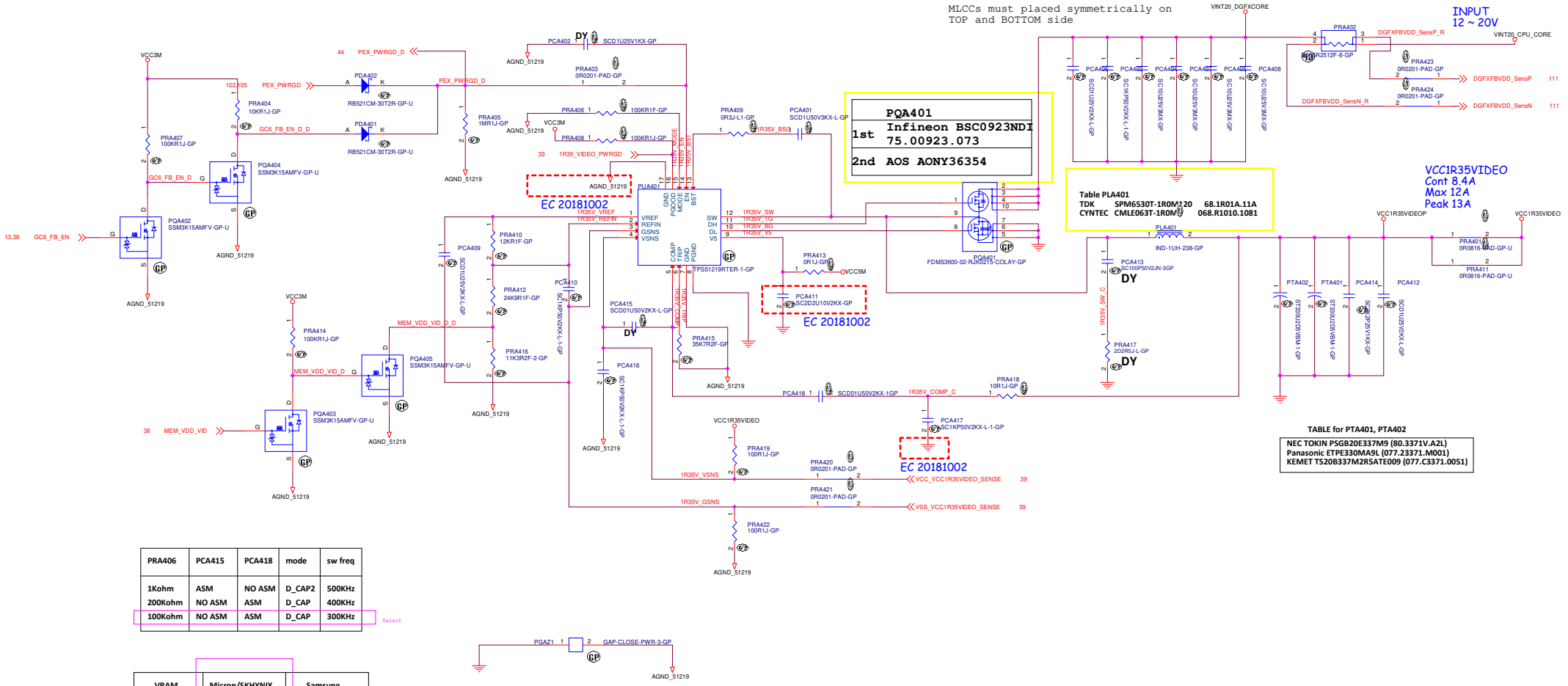

MLCCs must placed symmetrically on TOP and BOTTOM side
TOKIN_MPCH0740LR15D_ 68.R1510.10F
CYNTEC_CML E0647-R15M-S08x67
PL4302 , PL4304 , PL4306
VCCGFXCORE_D
EDP-Continuous 40A
EDP-Peak 150A
22uF 20 Pcs
NEC TOKIN_PSGB20E337M9 (80.3371V.A2L)
Panasonic_ETP.E330MA9L (077.23371.M001)
KEMET T520B337M2R5ATE009 (077.C3371.0051)
330uF 6 Pcs
2017/07/07 - 470uF_D2 change to 330uF_B2
Wistron Corporation
DC/DC VCCGFXCORE_D
LPM-2



PRA406	PCA415	PCA418	mode	sw freq
1Kohm	ASM	NO ASM	D_CAP2	500KHz
200Kohm	NO ASM	ASM	D_CAP	400KHz
100Kohm	NO ASM	ASM	D_CAP	300KHz

Select

VRAM	Micron/SKHYNIX	Samsung
MEM_VDD_VID	PRA416 = 11.3K 1%	PRA416 = 16.5K 1%
0	1.35V	1.35V
1	1.5V	1.55V

Select

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Title: DC/DC VCC1R35VIDEO

Size	Document Number	Rev
A2	LPM-2	-1

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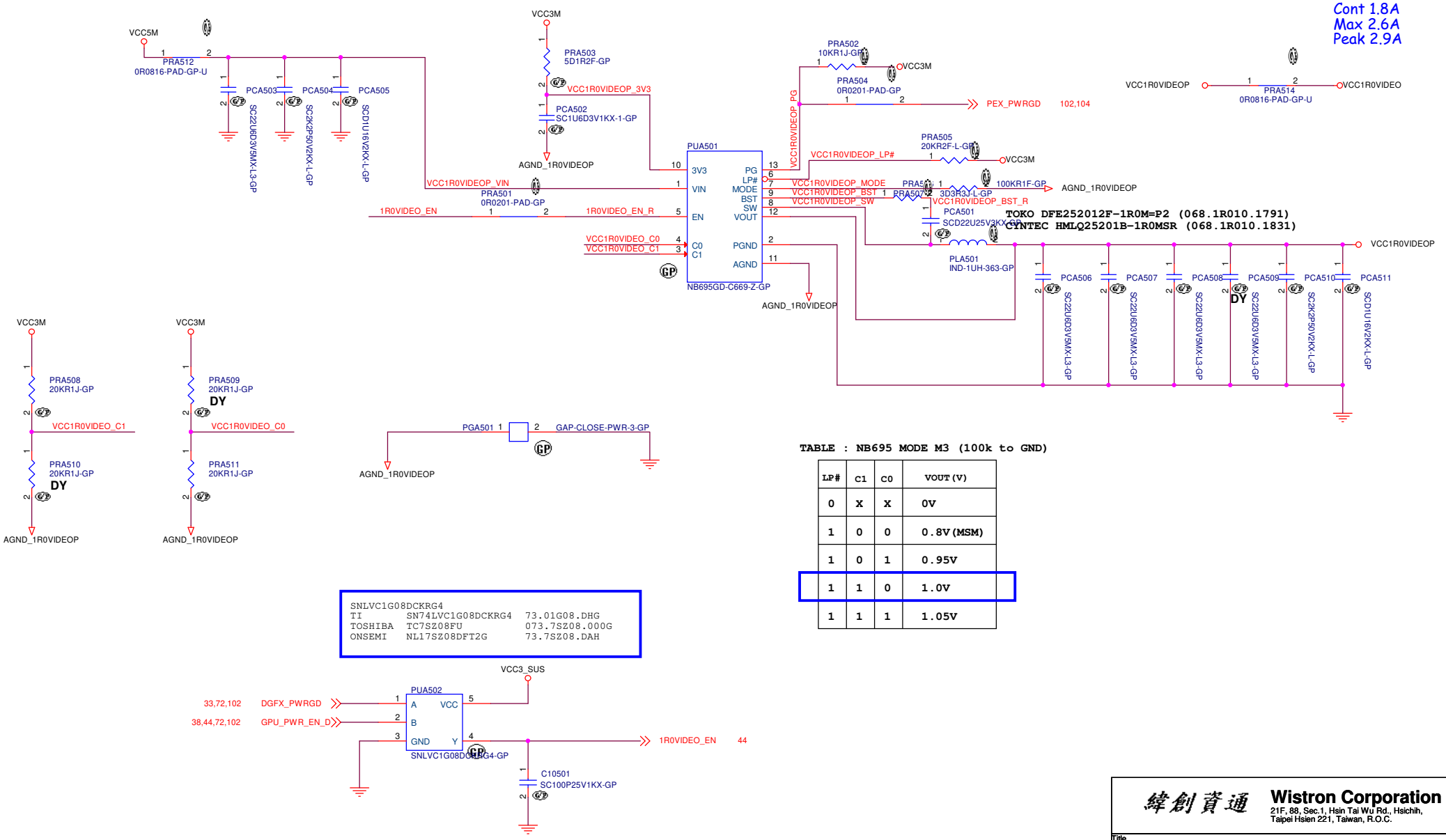

TABLE : NB695 MODE M3 (100k to GND)

LP#	C1	C0	VOUT (V)
0	X	X	0V
1	0	0	0.8V (MSM)
1	0	1	0.95V
1	1	0	1.0V
1	1	1	1.05V

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Title: ***DC/DC VCC1R0VIDEO***

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A3	LPM-2	-1

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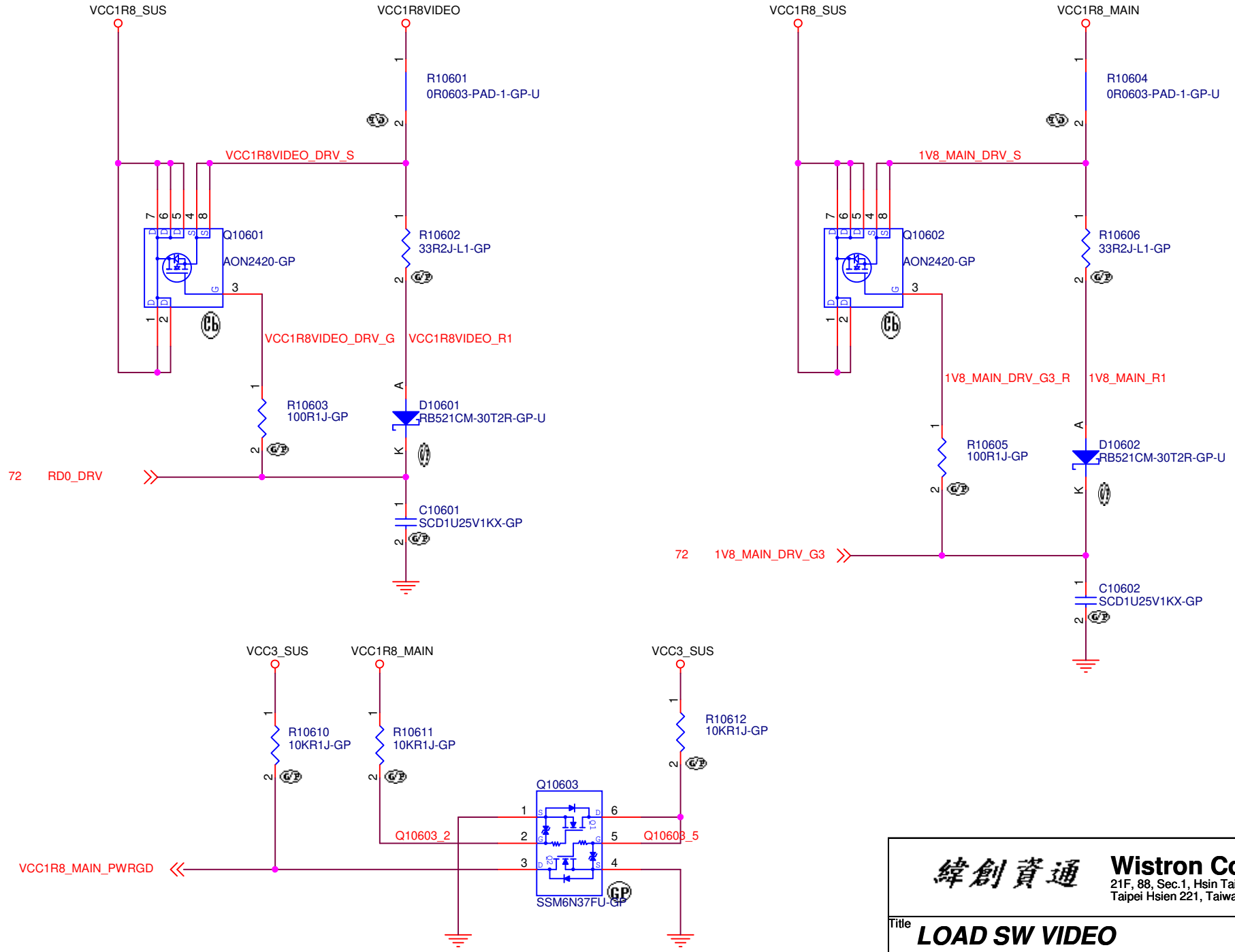
VCC1R8VIDEO & VCC1R8MAIN Total Max Current = 3.3 (A)



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Title: **LOAD SW VIDEO**

Size	Document Number	Rev
A4	LPM-2	-1

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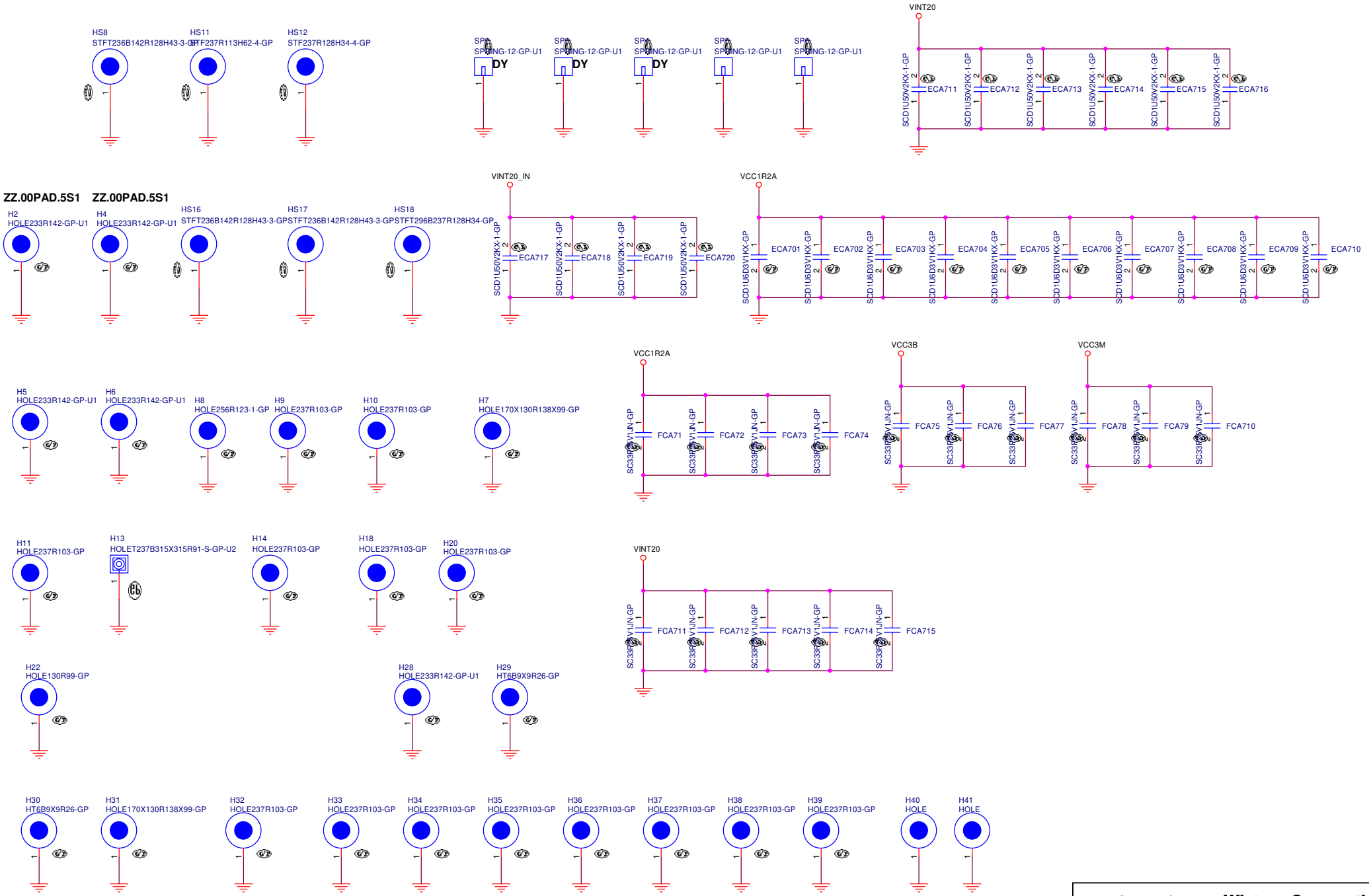

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Title: ***HOLE/EMC/RF***

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Title ***LOAD BOM ONLY***

Size	Document Number	Rev
A4	**LPM-2**	-1

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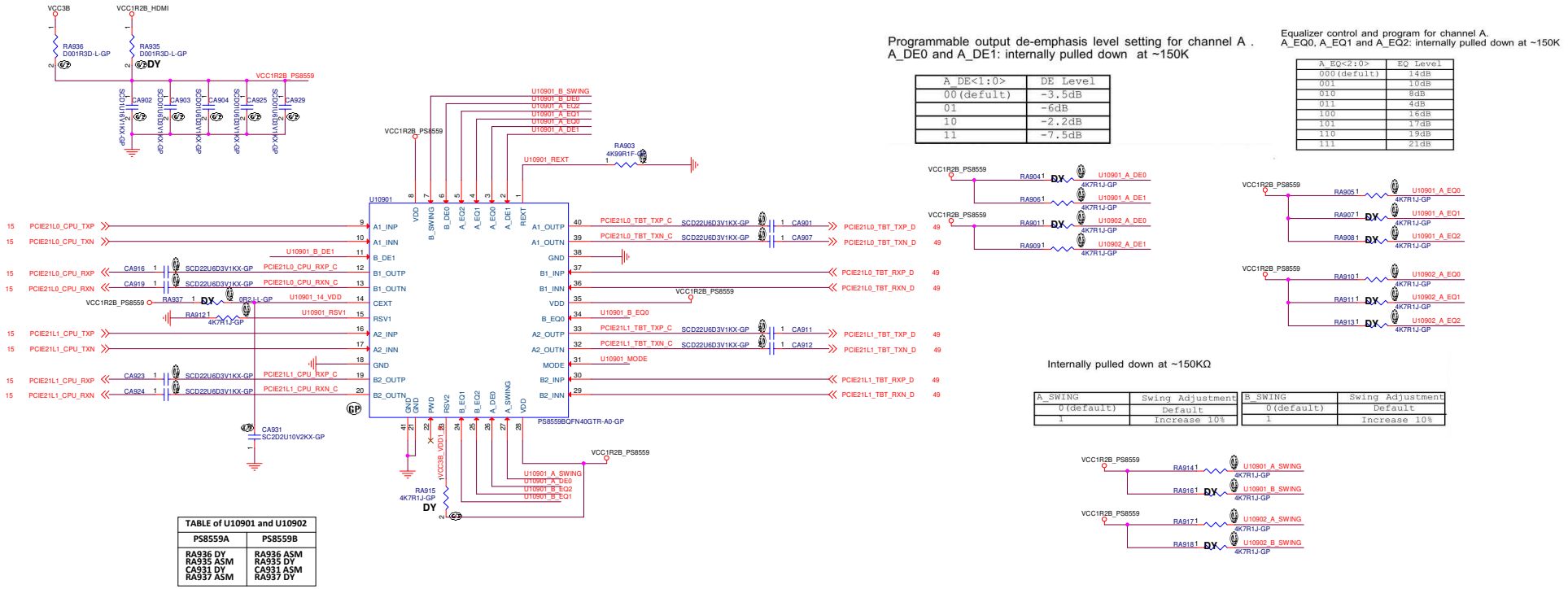

TABLE of U10901 and U10902	
PS8559A	PS8559B
RA936 DY RA935 ASM CA931 DY RA937 ASM	RA936 ASM RA935 DY CA931 ASM RA937 DY

Programmable output de-emphasis level setting for channel A .
A_DE0 and A_DE1: internally pulled down at ~150K

A_DE<1:0>	DE Level
00(default)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

A_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

Internally pulled down at ~150KΩ

A_SWING	Swing Adjustment
0(default)	Default
1	Increase 10%

B_SWING	Swing Adjustment
0(default)	Default
1	Increase 10%

Programmable output de-emphasis level setting for channel B .
B_DE0 and B_DE1: internally pulled down at ~150K

B_DE<1:0>	DE Level
00(default)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

B_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

Internally pulled down at ~150KΩ

MODE	Operation Mode
0(default)	SATA
1	PCIe

ULT

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCIE RE-DRIVER

Size: A2 | Document Number: LPM-2 | Rev: -1

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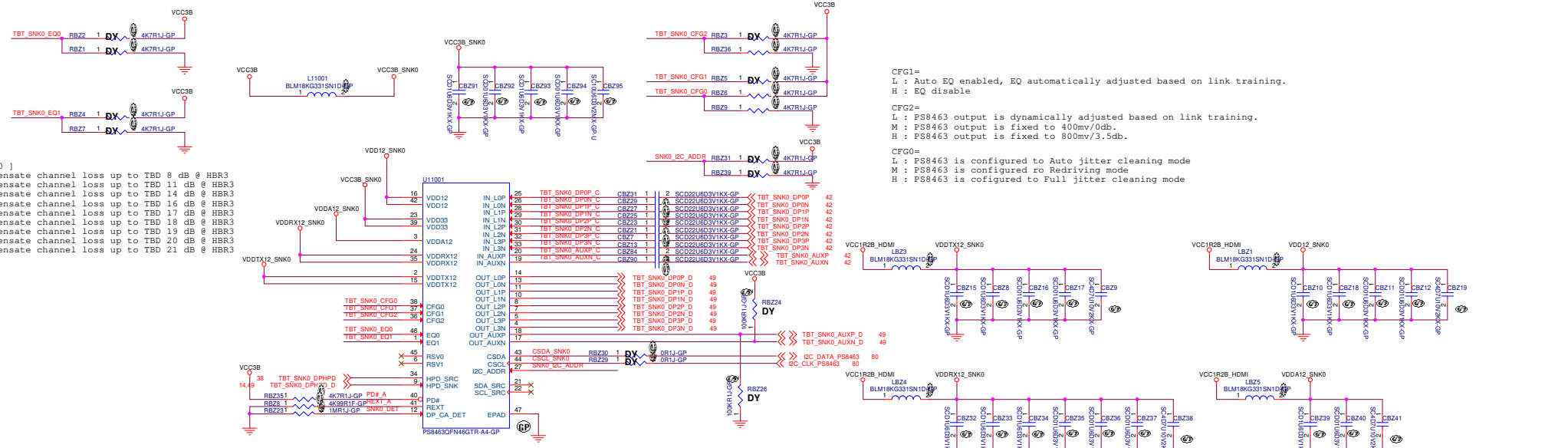

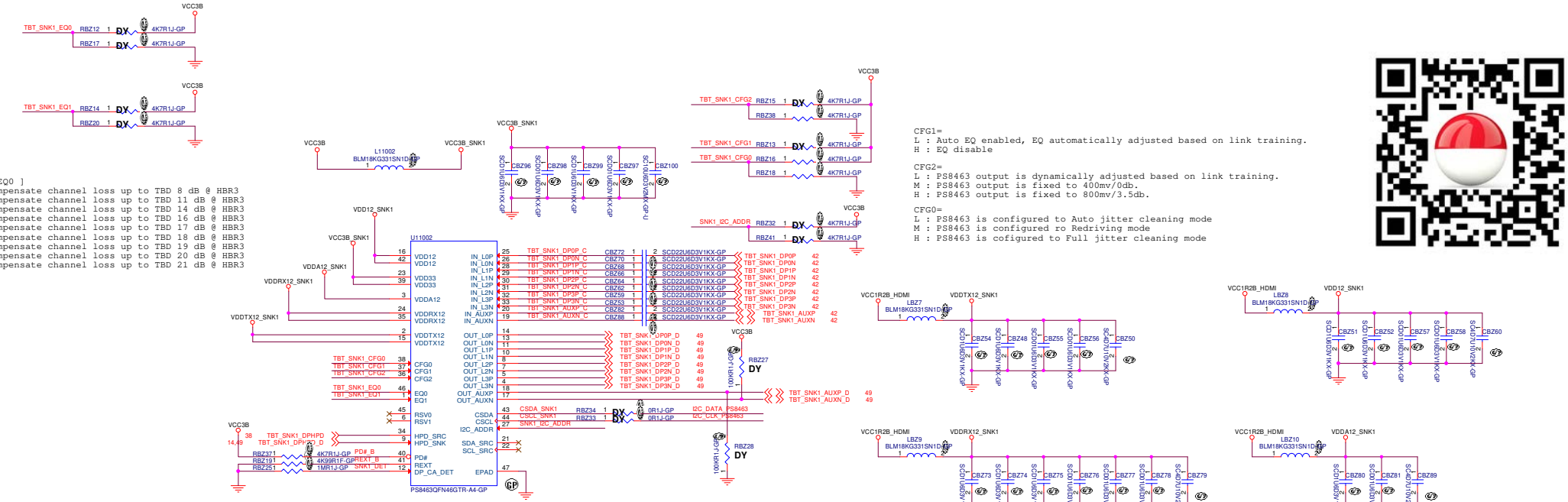

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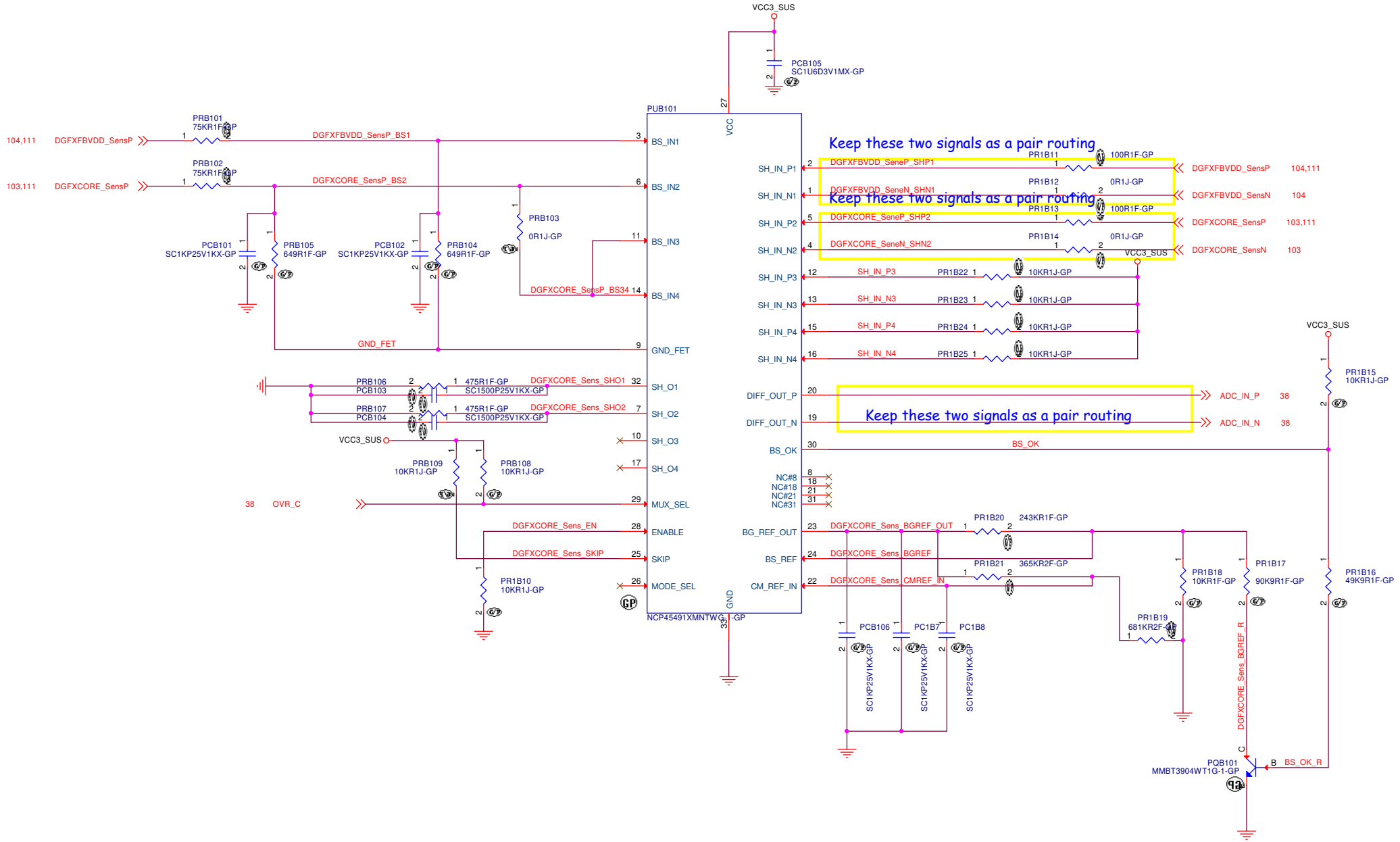

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