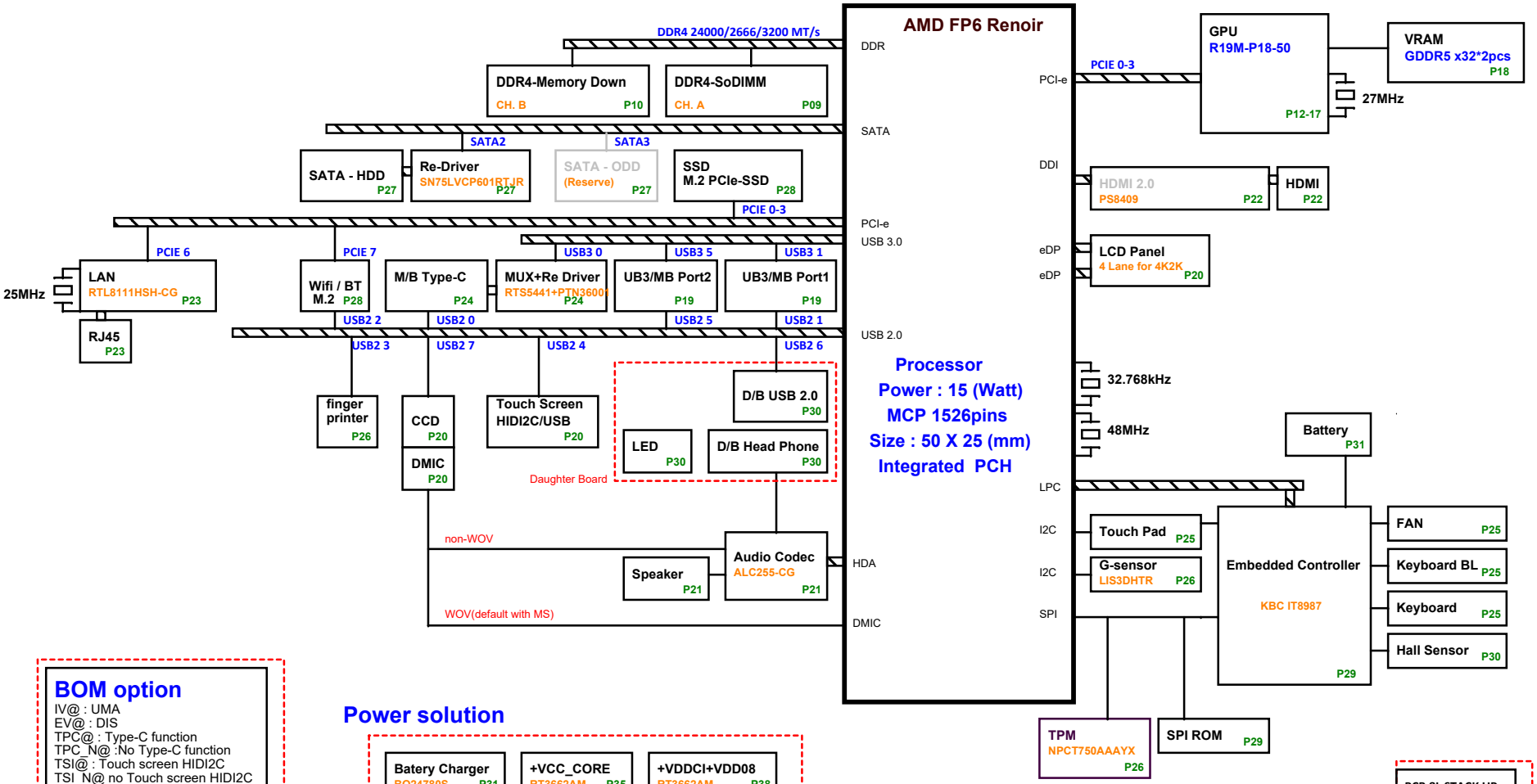
ZAUR AMD Renoir Platform Block Diagram

01



BOM option

IV@ : UMA
EV@ : DIS
TPC@ : Type-C function
TPC_N@ :No Type-C function
TSI@ : Touch screen HIDI2C
TSI_N@ no Touch screen HIDI2C
TPM@ : Trusted Platform Module
TPM_N@ no TPM
PBA@ : Finger Print on touch pad
KBL@ : Keyboard back light
GS@ : G-Sensor function
GS_N@ : No G-Sensor function
SSD@ : Solid State Disk
ODD@ : Optical Disc Drive
RAM@ : On Board Memory
DBG@ : for Debug Card
*255@ : Codec 255
256@ : Codec 256
FOR15_17@ : Panel 15 or 17 inch
*FOR14@ : Panel 14 inch
HDT@:AMD HDT
MID@:Memory ID
*MS@:Modern standby

G2@ for WW
G3@ for MGF
G3S@ MGF wo HDD connector

Power solution

Batery Charger BQ24780S P31	+VCC_CORE RT3662AM P35	+VDDCI+VDD08 RT3662AM P38
+3VPCU/+5VPCU RT6256/6258 P32	+VDDCR_SOC RT3662AM P35	+VGPU_CORE RT3662AM P39
+3V/+5V JW7110DFNC P32	+1.8V_S5 JW5213DFND P37	+1.35V_GFX G5335QT2U P41
VDDP_S5_S0 G5334CQT1 P33	+1.5V JW5222RSOTB P37	+1.8V_GFX UP8801SSW8 P41
+1.2VSUS TPS51486R P34	Thermal protection P37 TMP708AIDBVR	+3V_GFX P41

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

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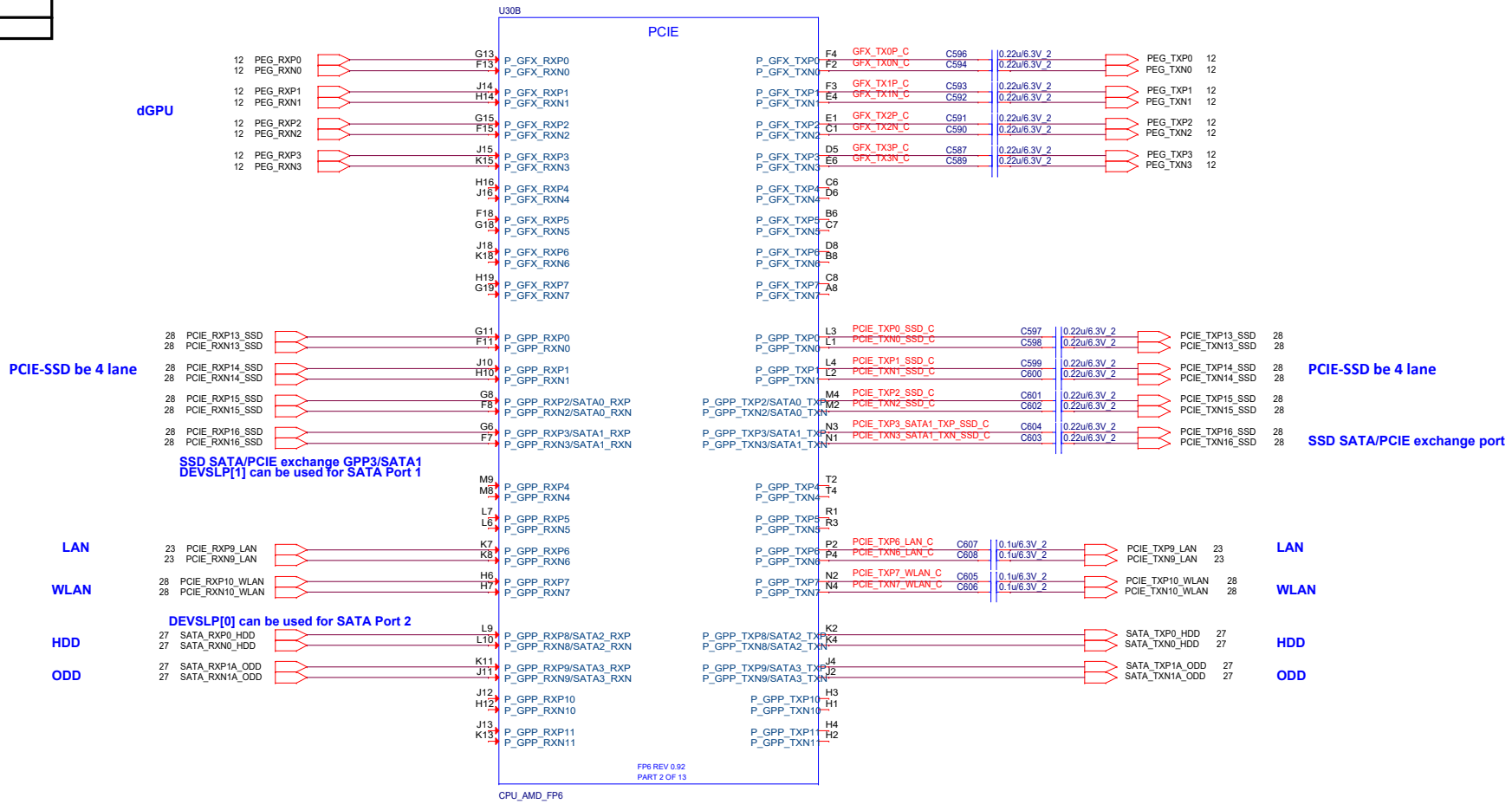
APU PCIE

AMD APU	TOP BSQ	QBCON

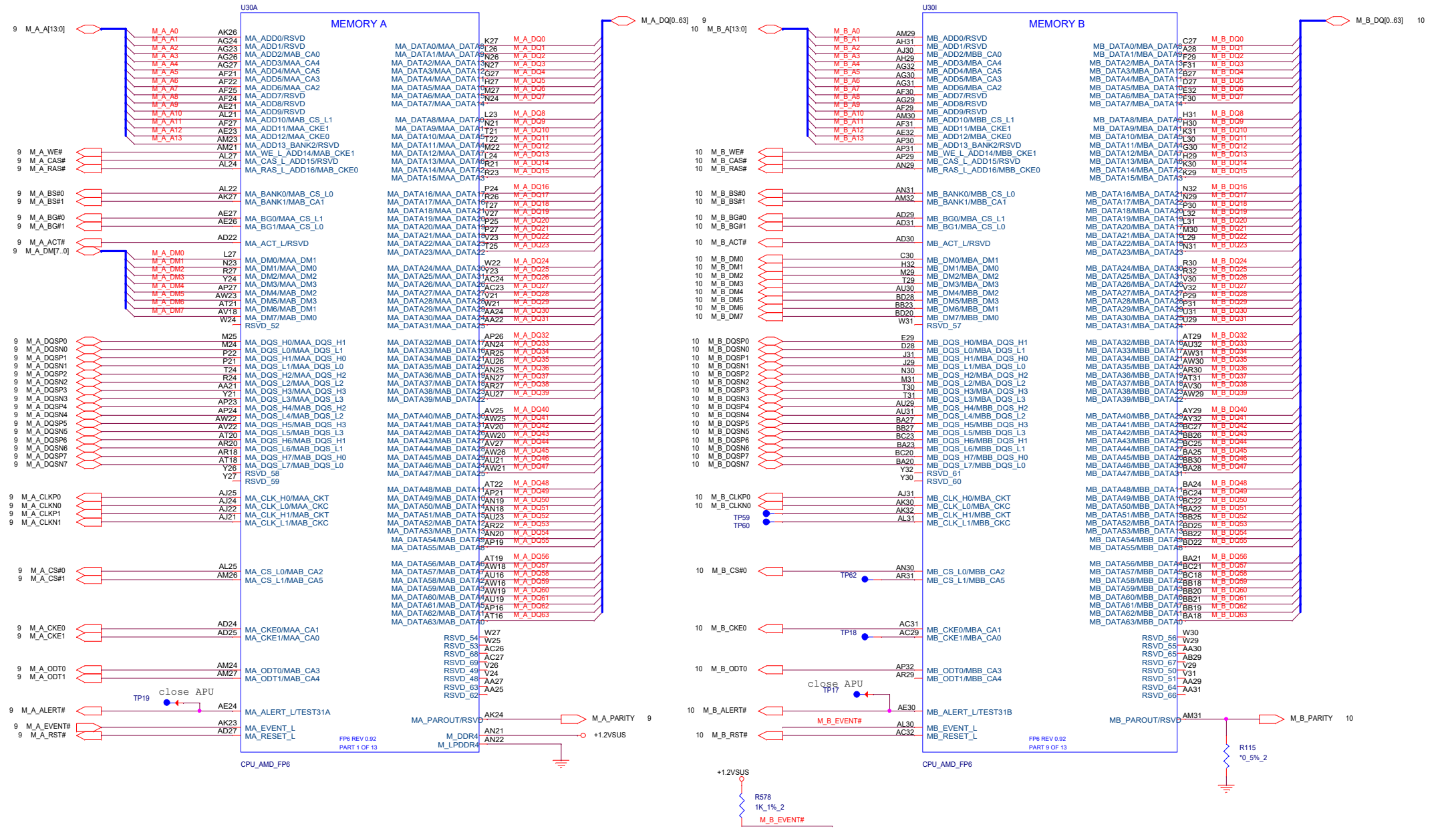
PCIE Port	Function
PCIE_0	SSD_PCIE
PCIE_1	SSD_PCIE
PCIE_2	SSD_PCIE
PCIE_3	SSD_PCIE
PCIE_4	NA
PCIE_5	NA
PCIE_6	LAN
PCIE_7	WLAN

SATA Port	Function
SATA_1	M.2_SSD
SATA_2	HDD
SATA_3	ODD



APU MEMORY

05



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	RR 2/7(MEM)		1A
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APU DISPLAY and MISC

06

eDP Panel

HDMI

U30C

DISPLAY/SVI2/JTAG/TEST

CPU_AMD_FP6

install R556/un-install R559 for the Audio output from HDMI

1118 :change to 4.7 k for the power saving

for ESD

cpu core powerok

check APU_THERMTRIP# connection

SI :change to 1K for LG Panel PWM

APU Serial VID

2018/08/27 :
SVC and SVD change to 22ohm

Boot-VID code

SVC	SVD	VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

HDT+ Connector for Debug only

FP6 PU to +1.8V_RUN

*HDT@HDT CONN

PLACE HDT CONNECTOR ON BOT
FP6 do not support pin 14/18/20 as CRB

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APU GPIO/AZ/UART

07

LAN/WLAN/NVMe

HDA INTERFACE

MIC@WOV
1227 remove WOV

no used on CRB

ACPI/AUDIO/I2C/GPIO/MISC

CLK/LPC/EMMC/SD/SPI/eSPI/UART

touch pad

I2C touch screen

DIMM, Gsensor

If unused, enable internal pull up or pull down by software

1224 RSVD R748 to +3V_S5

For SSD_DET
High: SSD SATA IF
Low: SSD PCIE IF

LPC interface, connected to a 10k pull-up resistor to 3.3V

STRAPS PINS connection

Multiple SPI Device Routing / remove it if no used TPM
PU to TPMPWR @ TPM page

PU to TPM power @ device page

10 kΩ optional buffer after pulldown depending on system loading

SPI_CLK not tri-stated for rom sharing
VGS MAX 1.06V

used EC_SCI#, PU 3.3_S5 as CRB

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	RR 4/7(GPIO/HDA/SPI/I2C)	1A
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USB3 and USB2 Port Mapping

TYPE-C meet USB3_0

U3 MB port A meet USB3_1

BT

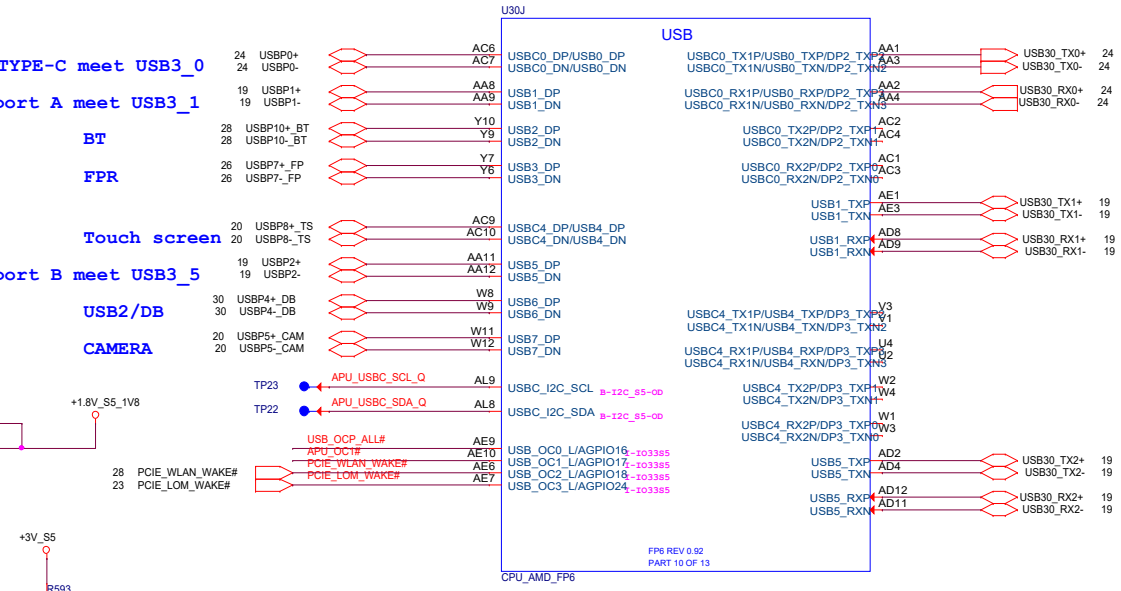
FPR

Touch screen

U3 MB port B meet USB3_5

USB2/DB

CAMERA

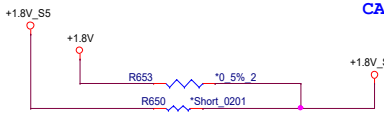


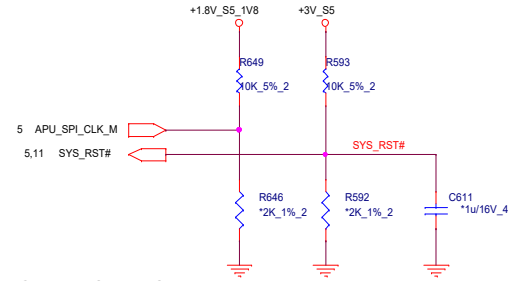
USB TYPE C

U3 MB port A

U3 MB port B

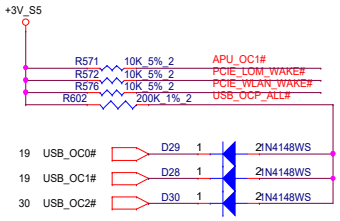
STRAPS PINS

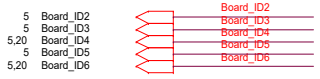


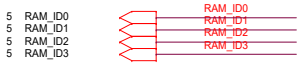


REQUIRED STRAPS

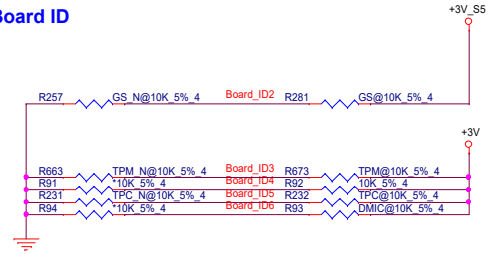
	APU_SPI_CLK	SYS_RST# (Int Pull-up)
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	normal reset mode (DEFAULT)
PULL LOW	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode







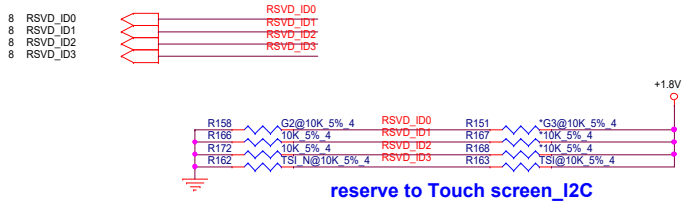
Board ID



default

	Low	High	
BOARD_ID2	Non G-sensor(GS_N@)	G-sensor(GS@)	S5
BOARD_ID3	Non TPM(TPM_N@)	TPM(TPM@)	S0
cable BOARD_ID4	Non Touch panel	Touch panel-USB (Control by Cable)	S0
BOARD_ID5	Non Type-C(TPC_N@)	Type-C(TPC@)	S0
cable BOARD_ID6	Single MIC(Cable control)	Dual MIC (DMIC@)	S0
RSVD_ID3	Non I2C Touch screen	I2C touch screen	S0

1217 reserved



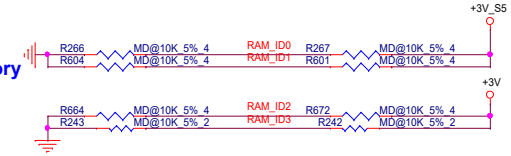
reserve to Touch screen_I2C

RAM ID

channel A is so-DIMM

channel B is on board memory

1217 adjust RAMID



ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	Hynix 8Gb	H5AN8G6NCJR-VKC	AKD5QGSTW13
0	0	0	1	Micron 8Gb	MT40A512M16LY-075:E	AKD5LZSTL24
0	0	1	0	Samsung 8Gb	K4A8G165WC-BCTD	AKD5QGST512
0	0	1	1	Hynix 16Gb	H5ANAG6NCMR-VKC	AKD5RGUTW08
1	1	1	1	With out on board memory		

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	RR 5/7(USB/STRAP)	1A

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APU POWER

09

3,9,10,34 +1.2VSUS
4,5,6,21,24,26,35,37 +1.8V
4,5,6,9,11,12,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,41 +3V
35,36 +VCC_CORE
4,5,6,11,21,24,26,29,37 +1.8V_S5
5,6,11,20,21,23,25,27,28,29,32,37,38 +3V_S5
33 VDDP_S5
4,33,37 VDDP
35,36 +VDDCR_SOC

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 7*22UF+1*1UF+1*180PF

+VDDCR_SOC

C217 180p/50V_4
C245 1u/6.3V_4
C249 22U/6.3V_6
C222 22U/6.3V_6
C256 22U/6.3V_6
C250 22U/6.3V_6
C253 22U/6.3V_6
C227 22U/6.3V_6
C246 22U/6.3V_6

RR DG: 9*22UF+2*1UF+4*0.22uf+3*180PF

BOTTOM SIDE DECOUPLING UNDER APU

VDDIO_MEM-DDR4:6A

+1.2VSUS

C314 22u/6.3V_6
C305 22u/6.3V_6
C315 22u/6.3V_6
C219 22u/6.3V_6
C287 22u/6.3V_6
C323 22u/6.3V_6
C234 22u/6.3V_6
C300 22u/6.3V_6
C233 22u/6.3V_6
C291 1u/6.3V_4
C296 1u/6.3V_4
C218 180p/50V_4

C321 0.22U/10V_4
C271 0.22U/10V_4
C320 0.22U/10V_4
C319 0.22U/10V_4
C265 180p/50V_4
C318 180p/50V_4

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

U30F

POWER

N16	VDDCR_SOC_1		
N18	VDDCR_SOC_2	13A	70A
N20	VDDCR_SOC_3		
P17	VDDCR_SOC_4		
P19	VDDCR_SOC_5		
R18	VDDCR_SOC_6		
R20	VDDCR_SOC_7		
T19	VDDCR_SOC_8		
U18	VDDCR_SOC_9		
U20	VDDCR_SOC_10		
V19	VDDCR_SOC_11		
W18	VDDCR_SOC_12		
W20	VDDCR_SOC_13		
Y19	VDDCR_SOC_14		
AC20	VDDIO_MEM_S3_1		
AC28	VDDIO_MEM_S3_2		
AD23	VDDIO_MEM_S3_3		
AD26	VDDIO_MEM_S3_4		
AD28	VDDIO_MEM_S3_5		
AD32	VDDIO_MEM_S3_6		
AE20	VDDIO_MEM_S3_7		
AE22	VDDIO_MEM_S3_8		
AE25	VDDIO_MEM_S3_9		
AE28	VDDIO_MEM_S3_10		
AF23	VDDIO_MEM_S3_11		
AF26	VDDIO_MEM_S3_12		
AF28	VDDIO_MEM_S3_13		
AF32	VDDIO_MEM_S3_14		
AG20	VDDIO_MEM_S3_15		
AG22	VDDIO_MEM_S3_16		
AG25	VDDIO_MEM_S3_17		
AG28	VDDIO_MEM_S3_18		
AJ20	VDDIO_MEM_S3_19		
AJ23	VDDIO_MEM_S3_20		
AJ26	VDDIO_MEM_S3_21		
AJ28	VDDIO_MEM_S3_22		
AJ32	VDDIO_MEM_S3_23		
AK22	VDDIO_MEM_S3_24		
AK25	VDDIO_MEM_S3_25		
AK28	VDDIO_MEM_S3_26		
AL23	VDDIO_MEM_S3_27		
AL26	VDDIO_MEM_S3_28		
AL28	VDDIO_MEM_S3_29		
AL32	VDDIO_MEM_S3_30		
AM22	VDDIO_MEM_S3_31		
AM25	VDDIO_MEM_S3_32		
AM28	VDDIO_MEM_S3_33		
AN28	VDDIO_MEM_S3_34		
AN32	VDDIO_MEM_S3_35		
AP28	VDDIO_MEM_S3_36		
AR32	VDDIO_MEM_S3_37		
AC21	VDDIO_VPH_1		
AD21	VDDIO_VPH_2		
AP9	VDDIO_AUDIO	0.2A	
AL18	VDD_33_1	0.25A	
AM17	VDD_33_2		
AL20	VDD_18_1	2.5A	
AM19	VDD_18_2		
AL19	VDD_18_S5_1	1A	
AM18	VDD_18_S5_2		
AL17	VDD_33_S5_1	0.25A	
AM16	VDD_33_S5_2		
AL11	VDDP_S5_1	2A	
AL12	VDDP_S5_2		
AM12	VDDP_S5_3		
M15	VDDP_1	2A	
M16	VDDP_2		
M18	VDDP_3		
AJ11	VDDBT_RTC_G		
G7	VDDCR_1		
G10	VDDCR_2		
G12	VDDCR_3		
G14	VDDCR_4		
H8	VDDCR_5		
H11	VDDCR_6		
H15	VDDCR_7		
K6	VDDCR_8		
K12	VDDCR_9		
K14	VDDCR_10		
L8	VDDCR_11		
M7	VDDCR_12		
M10	VDDCR_13		
N14	VDDCR_14		
P7	VDDCR_15		
P10	VDDCR_16		
P13	VDDCR_17		
P15	VDDCR_18		
R8	VDDCR_19		
R14	VDDCR_20		
R16	VDDCR_21		
T7	VDDCR_22		
T10	VDDCR_23		
T13	VDDCR_24		
T15	VDDCR_25		
T17	VDDCR_26		
U14	VDDCR_27		
U16	VDDCR_28		
V13	VDDCR_29		
V15	VDDCR_30		
V17	VDDCR_31		
W7	VDDCR_32		
W10	VDDCR_33		
W14	VDDCR_34		
W16	VDDCR_35		
Y8	VDDCR_36		
Y13	VDDCR_37		
Y15	VDDCR_38		
Y17	VDDCR_39		
AA7	VDDCR_40		
AA10	VDDCR_41		
AA14	VDDCR_42		
AA16	VDDCR_43		
AA18	VDDCR_44		
AB13	VDDCR_45		
AB15	VDDCR_46		
AB17	VDDCR_47		
AB19	VDDCR_48		
AC14	VDDCR_49		
AC16	VDDCR_50		
AC18	VDDCR_51		
AD7	VDDCR_52		
AD10	VDDCR_53		
AD13	VDDCR_54		
AD15	VDDCR_55		
AD17	VDDCR_56		
AD19	VDDCR_57		
AE8	VDDCR_58		
AE14	VDDCR_59		
AE16	VDDCR_60		
AE18	VDDCR_61		
AF7	VDDCR_62		
AF10	VDDCR_63		
AF13	VDDCR_64		
AF15	VDDCR_65		
AF17	VDDCR_66		
AF19	VDDCR_67		
AG14	VDDCR_68		
AG16	VDDCR_69		
AG18	VDDCR_70		
AH13	VDDCR_71		
AH15	VDDCR_72		
AH17	VDDCR_73		
AH19	VDDCR_74		
AJ7	VDDCR_75		
AJ10	VDDCR_76		
AJ14	VDDCR_77		
AJ16	VDDCR_78		
AJ18	VDDCR_79		
AK13	VDDCR_80		
AK15	VDDCR_81		
AK17	VDDCR_82		
AK19	VDDCR_83		

CPU_AMD_FP6

FP6 REV 0.92
PART 6 OF 13

+VCC_CORE

C254 22U/6.3V_6
C264 22U/6.3V_6
C263 22U/6.3V_6
C302 22U/6.3V_6
C295 22U/6.3V_6

RR DG: 16*22UF+1*180PF

C270 22U/6.3V_6
C309 22U/6.3V_6
C294 22U/6.3V_6
C276 22U/6.3V_6

C290 22U/6.3V_6
C251 22U/6.3V_6
C303 22U/6.3V_6
C275 22U/6.3V_6
C269 22U/6.3V_6
C252 22U/6.3V_6
C304 22U/6.3V_6
C247 180p/50V_4

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+3*1UF

VDDP_S5 +0.75V_S5

R288 *Short_0603
R280 *Short_0603

2A

C383 22u/6.3V_6
C368 1u/6.3V_4
C359 1u/6.3V_4
C385 1u/6.3V_4

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+1*1UF

R182 *Short_0603

C268 22u/6.3V_6

RR DG: 1*22UF+2*1UF

+1.8V_S5 +APU_VDDIO_AZ

R240 *Short_0603

0.2A

C350 1u/6.3V_4
C351 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+3V +APU_VDD_33

R295 *Short_0603

0.25A

C392 1u/6.3V_4
C388 1u/6.3V_4
C399 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+2*1UF

+3V_S5 +APU_VDD_33_S5

R291 *Short_0603

0.25A

C382 1u/6.3V_4
C389 1u/6.3V_4
C396 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+1.8V +VDD_18

R666 *Short_0603
R665 *Short_0603

2.5A

RR DG: 1*22UF+2*1UF

C307 1u/6.3V_4
C316 1u/6.3V_4
C649 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+1.8V_S5 +VDD_18_S5

R297 *Short_0603

1A

RR DG: 1*22UF+2*1UF

C391 1u/6.3V_4
C327 1u/6.3V_4
C398 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 2*22UF+8*1UF+1*180PF

VDDP +0.75V

R545 *Short_0603
R544 *Short_0603

2A

BOTTOM SIDE DECOUPLING UNDER APU

C588 1u/6.3V_4
C585 180p/50V_4
C584 1u/6.3V_4
C231 1u/6.3V_4
C243 1u/6.3V_4

C186 22u/6.3V_6
C226 22u/6.3V_6
C232 1u/6.3V_4

C586 1u/6.3V_4
C578 1u/6.3V_4
C583 1u/6.3V_4

+3VPCU

C404 *0.1u/6.3V_2

R290 1.5K_5%_4
R289 45.3K_1%_4

+3V_RTC_0

CN20 50281-00201-001

+3V_RTC_0 R277 *Short_0402 +3V_RTC_1

+3V_RTC_2 D7 BAT54CW +3V_RTC

20mils

C375 1u/6.3V_2

RTC Circuitry(RTC)

RTC Power trace width 20mils.
Coin Battery: Connected to a +3.3V from coin battery through a series resistor of: 1K

VDDBT_RTC

4.5uA

C311 0.22U/10V_4
C347 1u/6.3V_4

J1 *JUMP

R261 1K_1%_4 +3V_RTC

Q16 2N7002K

R262 100K_5%_4

CLR_CMOS 29

EC reset RTC

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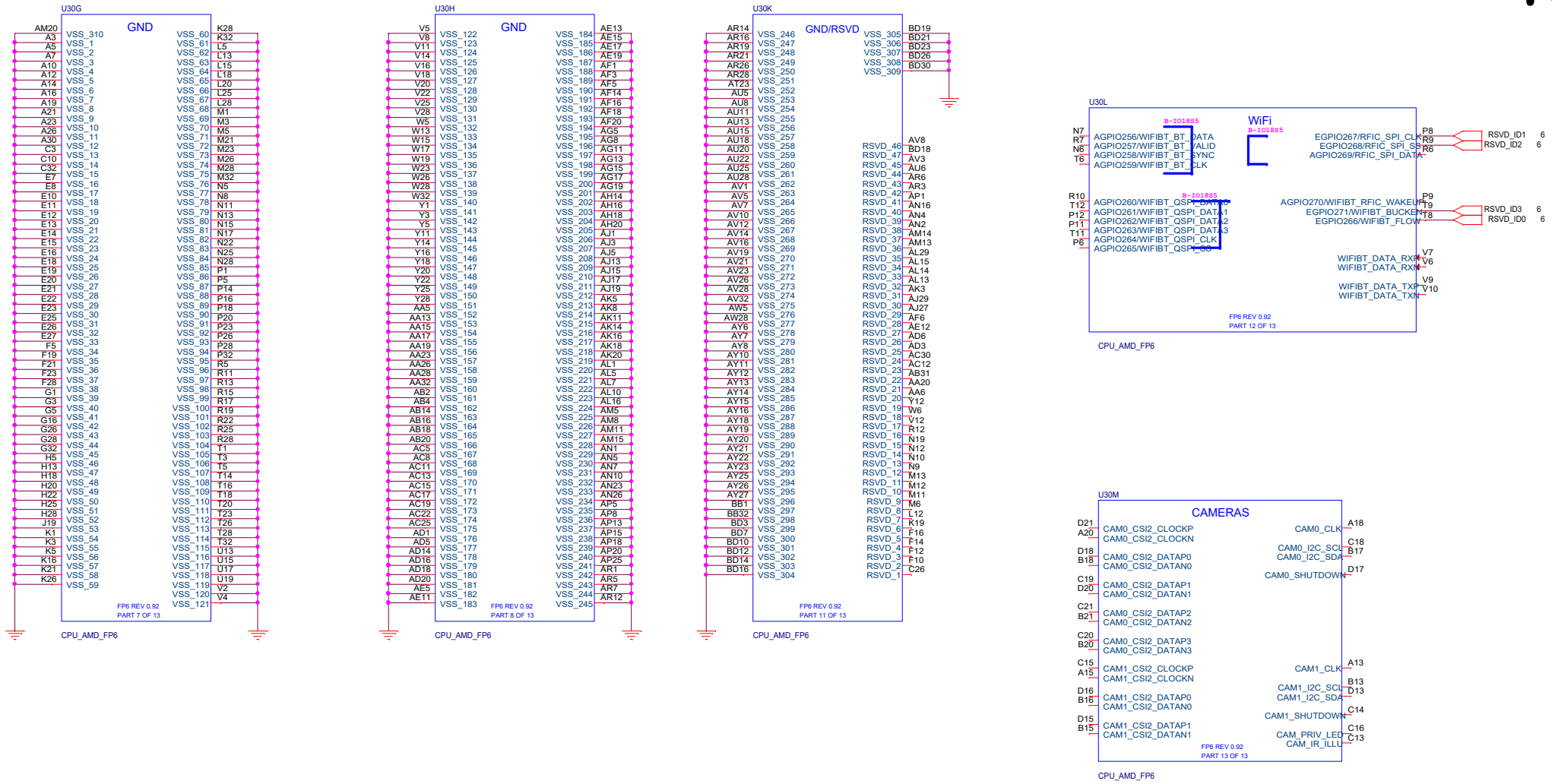
APU GND



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	RR 7/7(GND/RSVD)	1A

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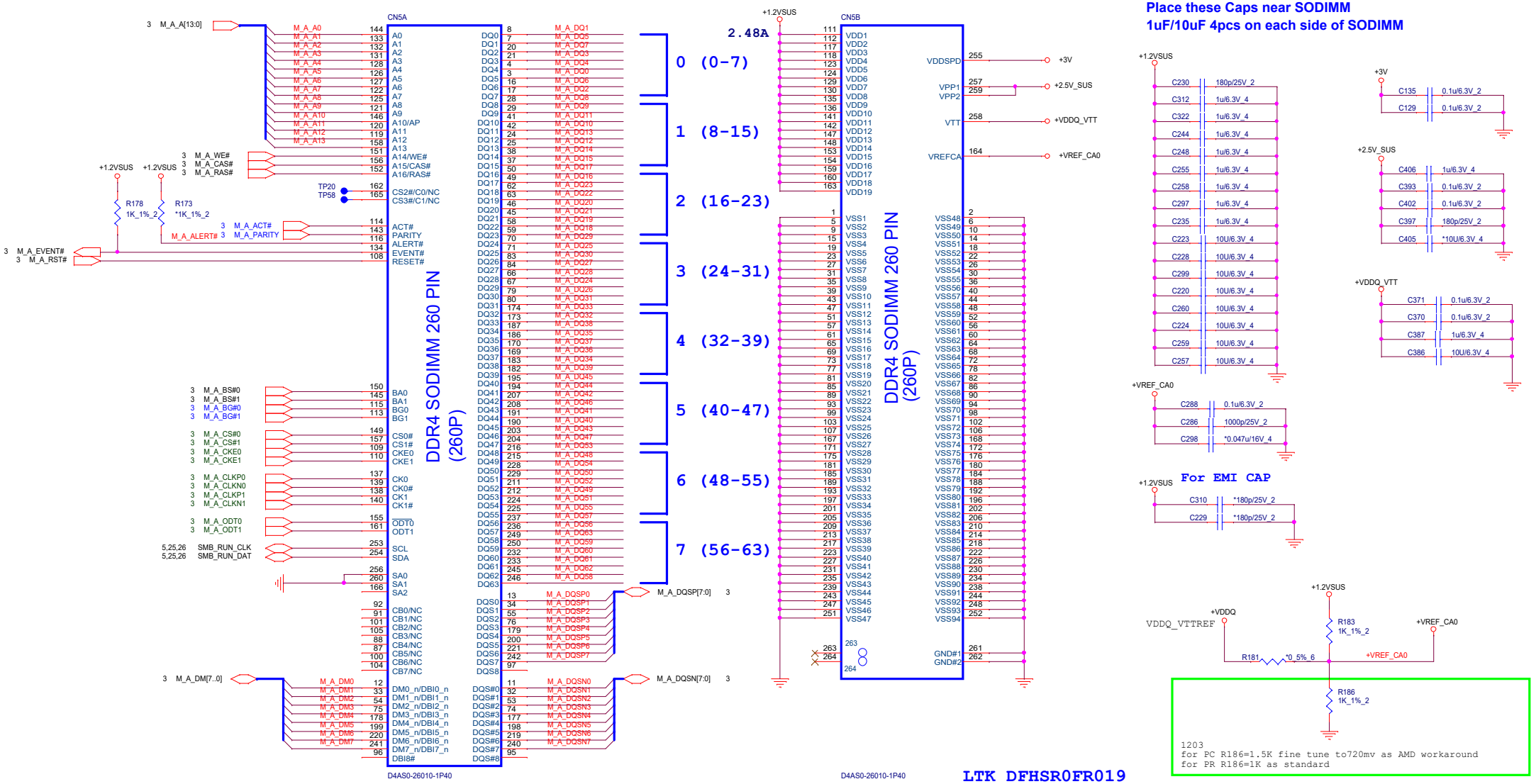
CHA0 DDR4

09

3 M_A_ALERT#
3 M_A_DQ[63:0]

4,5,6,7,11,12,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,41 10,34 +VDDQ
10,34 +3V
10,34 +2.5V_SUS
10,34 +VDDQ_VTT



Place these Caps near SODIMM
1uF/10uF 4pcs on each side of SODIMM

For EMI CAP

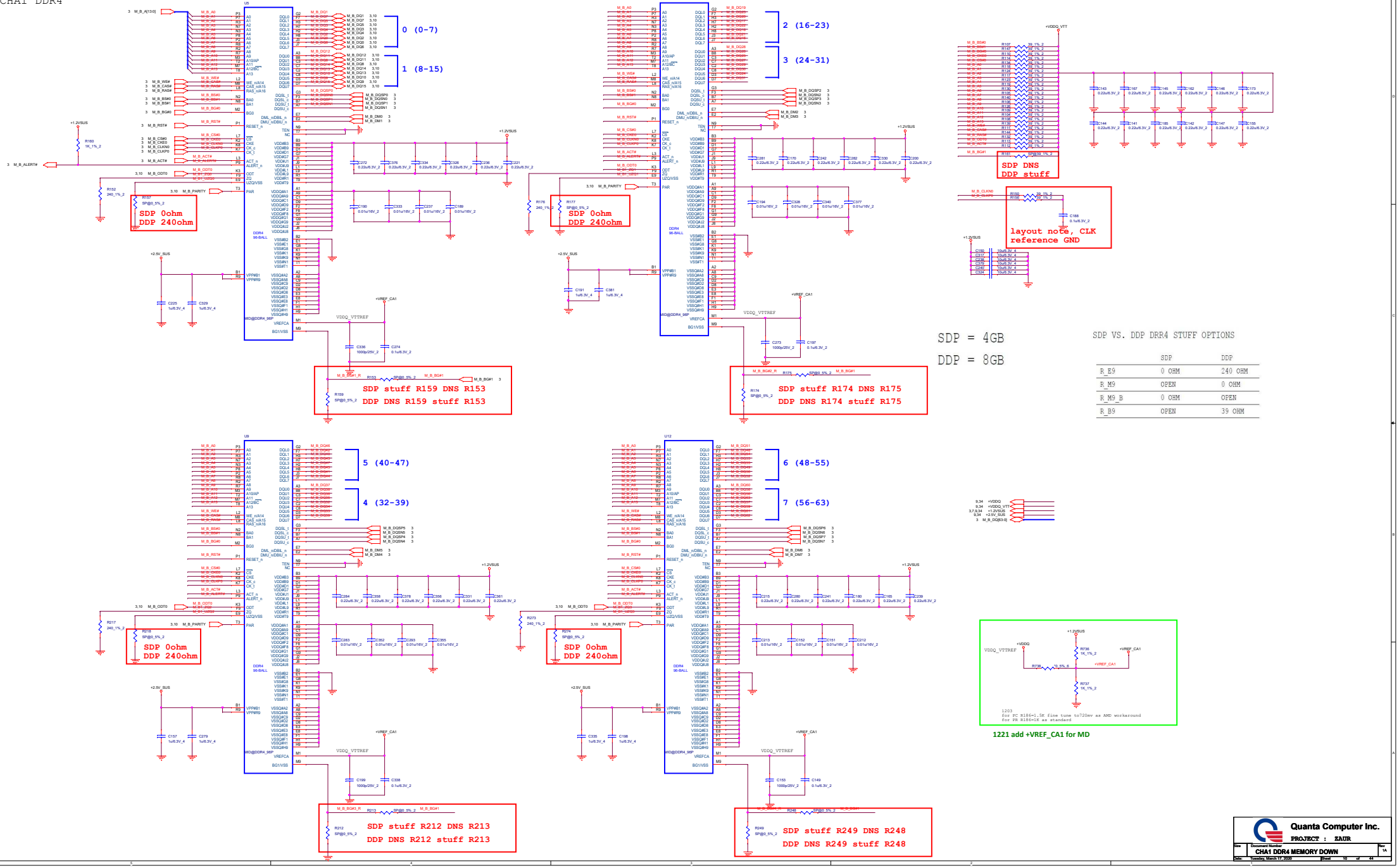
1203
for PC R186=1.5K fine tune to720mv as AMD workaround
for PR R186=1K as standard

LTK DFHSR0FR019
FOX DFHSR0FR199
DRE DFHSR0FR102

Quanta Computer Inc.
PROJECT : ZAUR

Size	Document Number	Rev
	CHA0 DDR4 DIMM0-RVS(4.0H)	1A
Date: Tuesday, March 17, 2020	Sheet 9 of 44	

CHA1 DDR4



SDP VS. DDP DRR4 STUFF OPTIONS

	SDP	DDP
R_E9	0 OHM	240 OHM
R_M9	OPEN	0 OHM
R_M9_B	0 OHM	OPEN
R_B9	OPEN	39 OHM

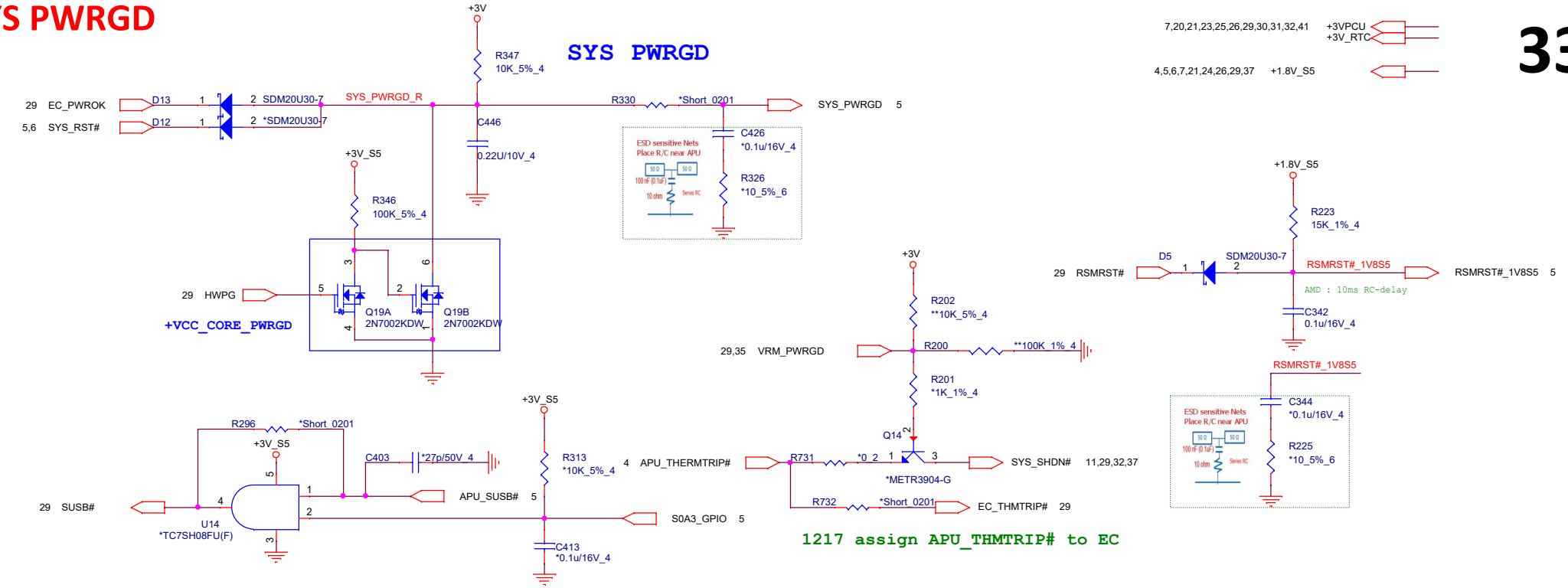
Quanta Computer Inc.

PROJECT : ZAUR

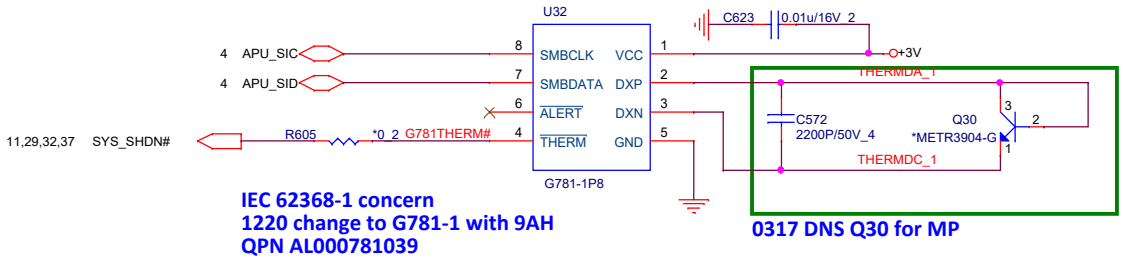
Size | Document Number: CHA1 DDR4 MEMORY DOWN | Rev: 1A

Date: Tuesday, March 17, 2020 | Sheet 10 of 44

SYS PWRGD



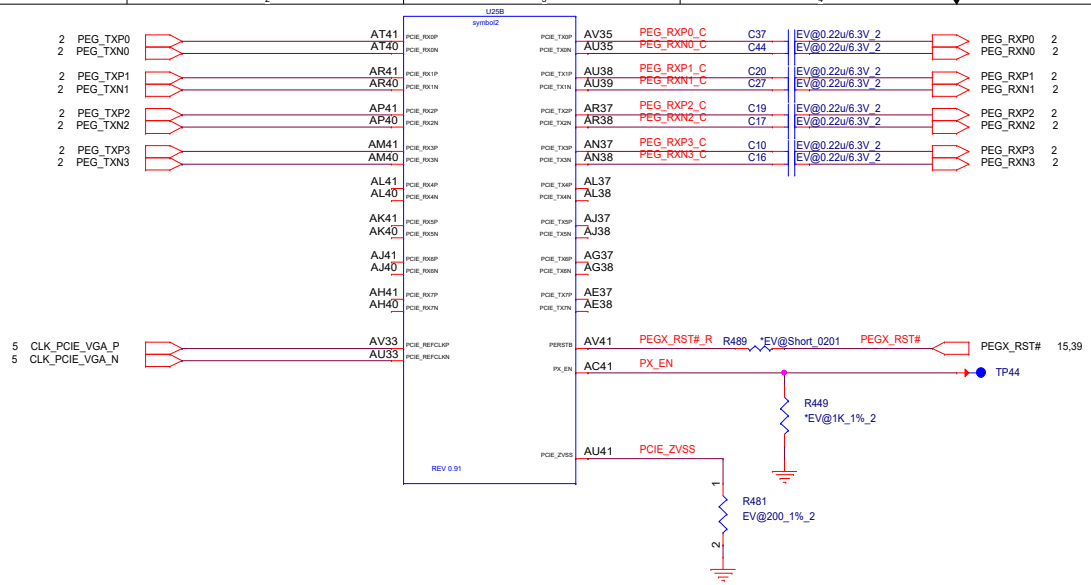
Address 9AH



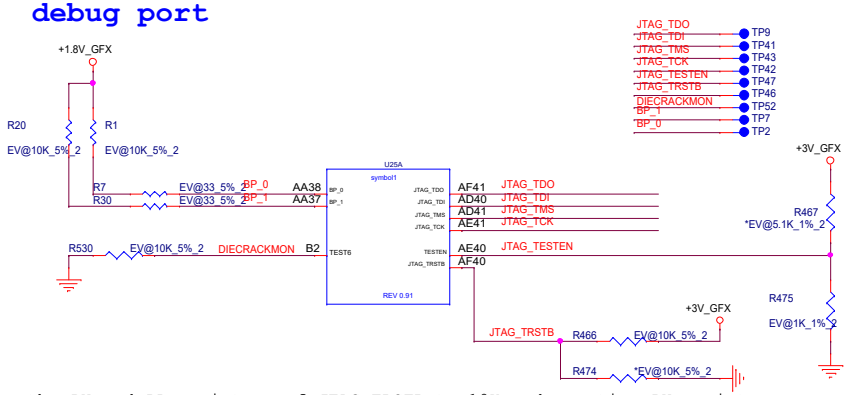
IEC 62368-1 concern
1220 change to G781-1 with 9AH
QPN AL000781039

0317 DNS Q30 for MP

Quanta Computer Inc.		
PROJECT : ZAUR		
Size	Document Number: RR SYSPWRGD/ThermalSensor	Rev: 1A
Date: Tuesday, March 17, 2020	Sheet 11 of 44	



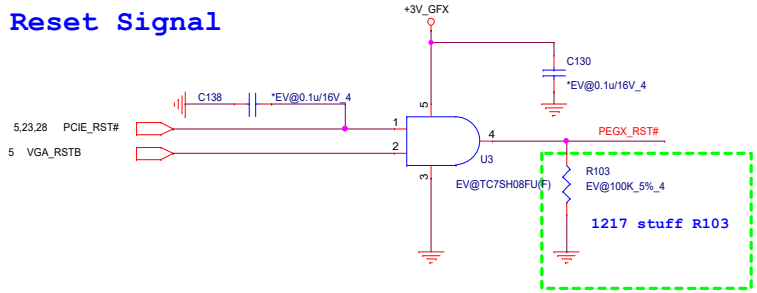
debug port

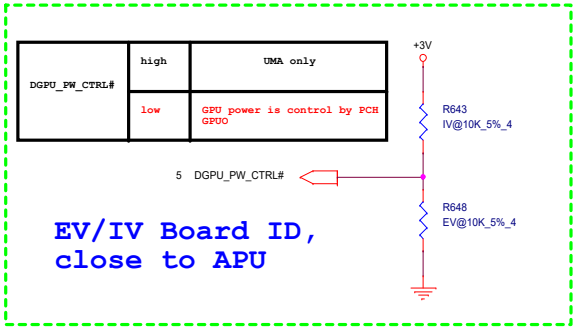


JTAG

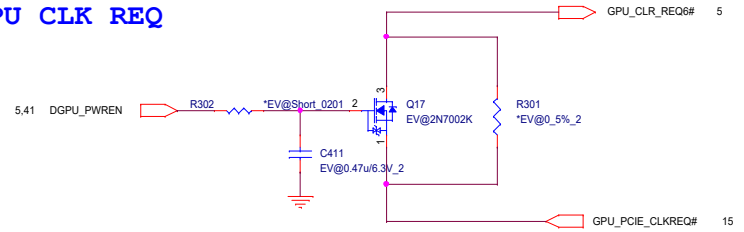
AMD Change the PU and PD resistors of JTAG_TRSTB to 10K and mounting PU resistor
AMD change the PU resistor of JTAG_TESTEN to 5.1K and keeping reserved.

GPU Reset Signal





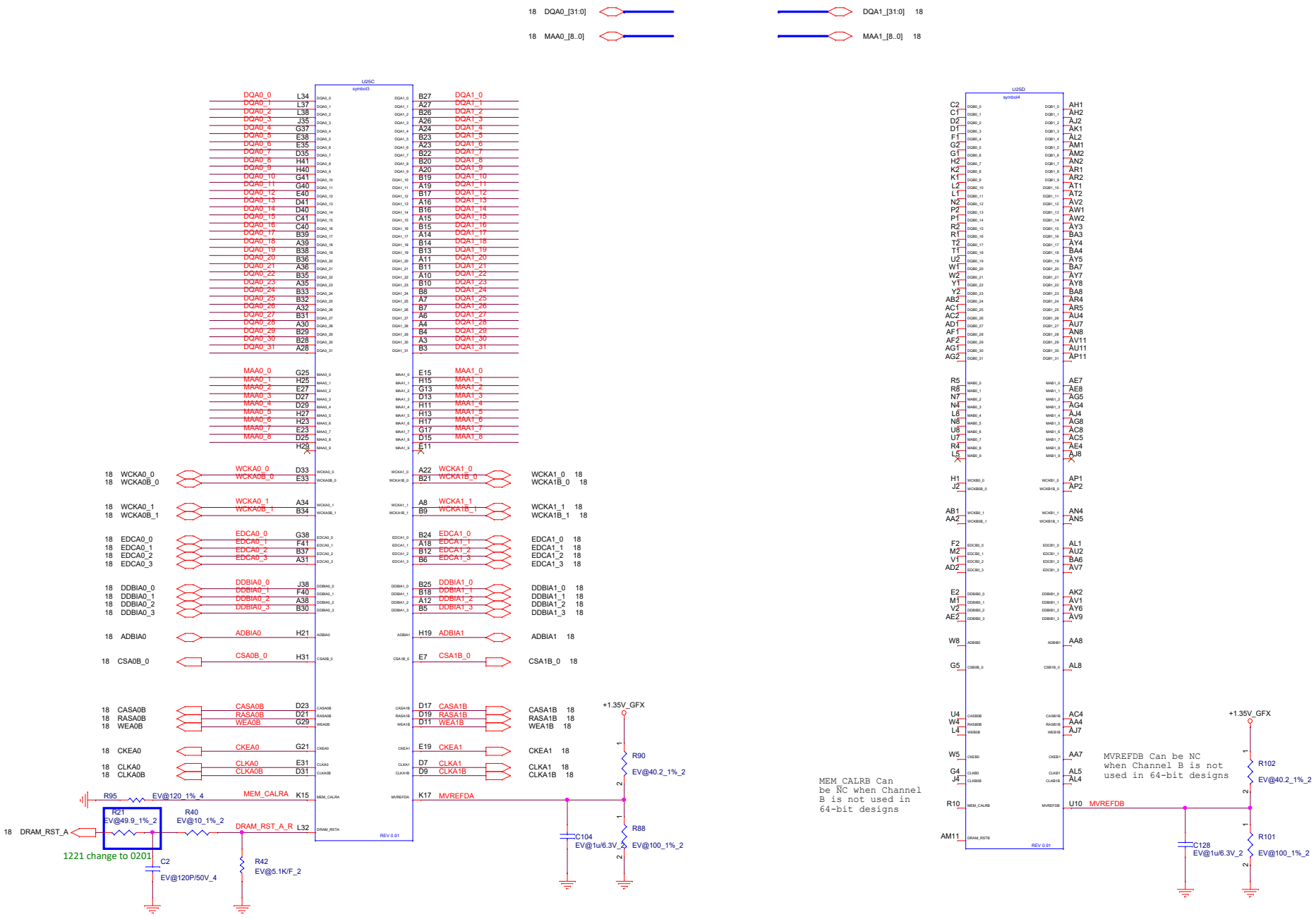
GPU CLK REQ



NB5

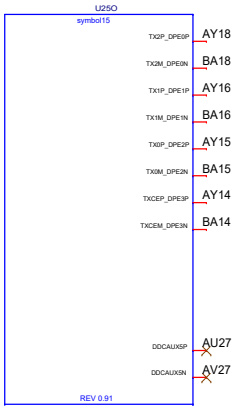
PROJECT : G3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R17M-P1-70 - 1/5 (PCIE)	1A
Date: Tuesday, March 17, 2020	Sheet 12 of 44	

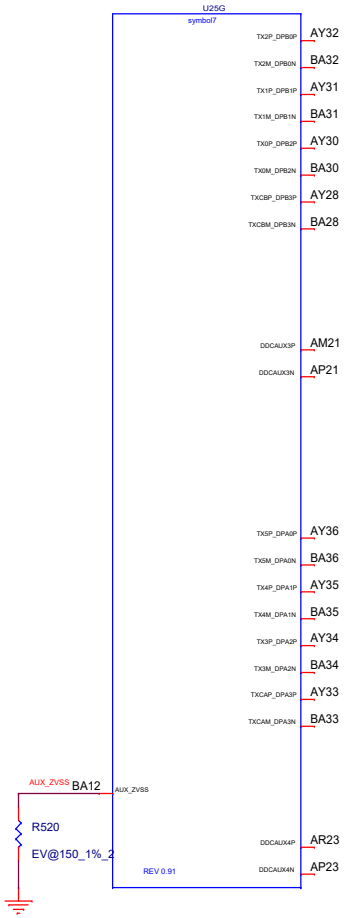


NB5	PROJECT : G3AC Quanta Computer Inc.	
Size: Custom	Document Number: R17M-P1-70 - 2/5 (Memory)	Rev: 1A
Date: Tuesday, March 17, 2020	Sheet 13 of 44	

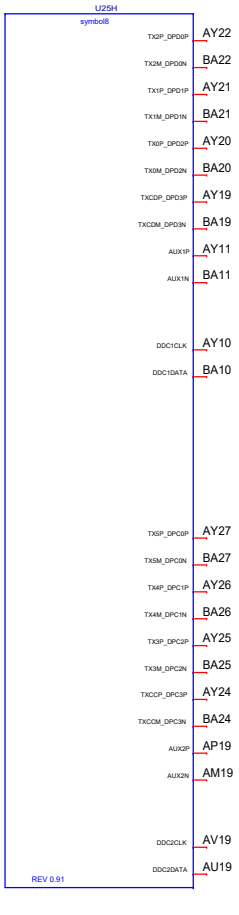
ASIC - TMDP (E)



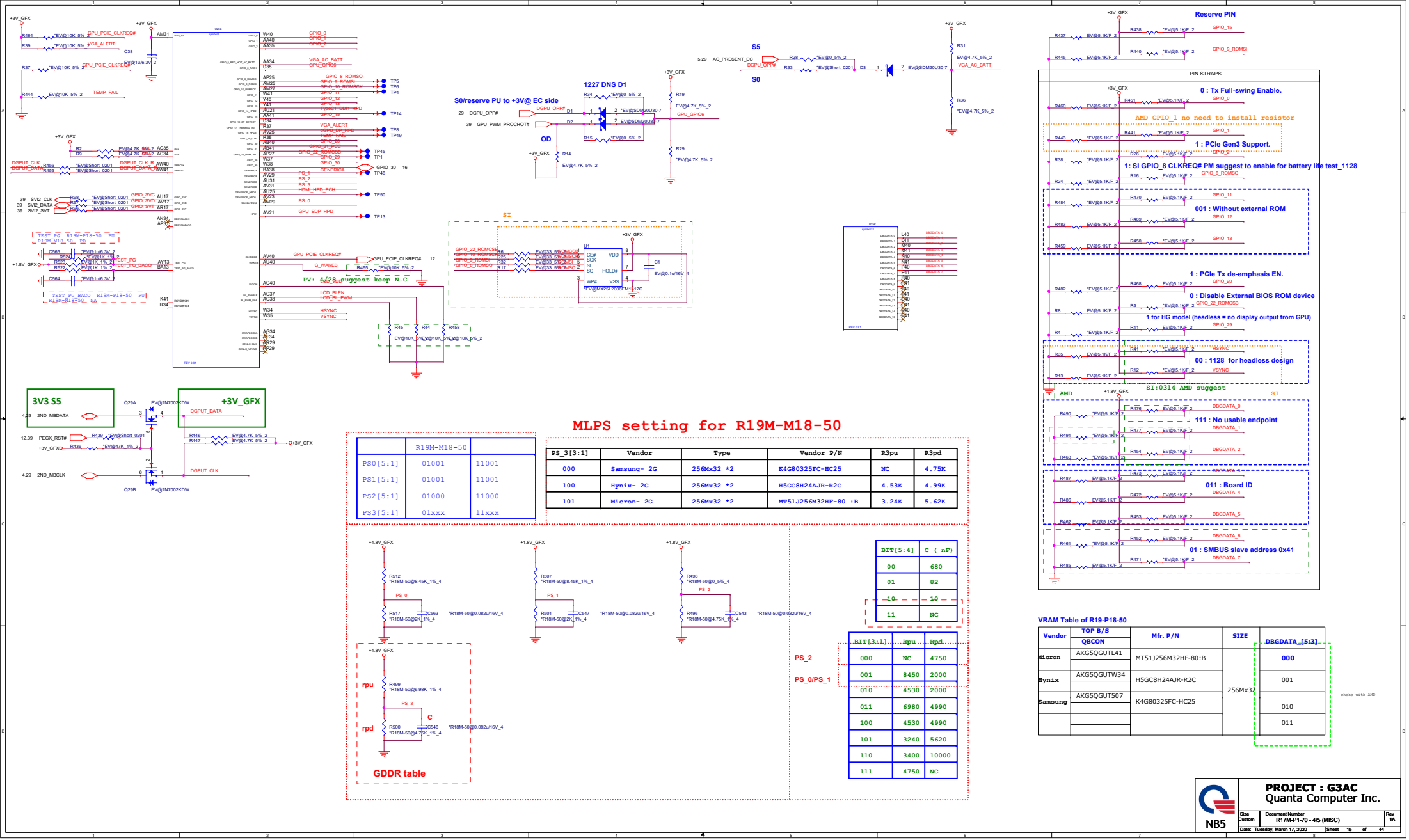
ASIC - TMDP (A/B)



ASIC - TMDP (C/D)



NB5	**PROJECT : G3AC** Quanta Computer Inc.	
Size A3	Document Number R17M-P1-70- 3/5 (Display)	Rev 1A
Date: Tuesday, March 17, 2020	Sheet 14 of 44	



MLPS setting for R19M-M18-50

	R19M-M18-50	
PS0[5:1]	01001	11001
PS1[5:1]	01001	11001
PS2[5:1]	01000	11000
PS3[5:1]	01xxx	11xxx

PS_3[3:1]	Vendor	Type	Vendor P/N	R3pu	R3pd
000	Samsung- 2G	256Mx32 *2	K4G80325FC-HC25	NC	4.75K
100	Hynix- 2G	256Mx32 *2	H5GC8H24AJR-R2C	4.53K	4.99K
101	Micron- 2G	256Mx32 *2	MT51J256M32HF-80 :B	3.24K	5.62K

BIT[5:4]	C (nF)
00	680
01	82
10	10
11	NC

PS_2 / PS_0/PS_1

BIT[3:1]	Rpu	Rpd
000	NC	4750
001	8450	2000
010	4530	2000
011	6980	4990
100	4530	4990
101	3240	5620
110	3400	10000
111	4750	NC

VRAM Table of R19-P18-50

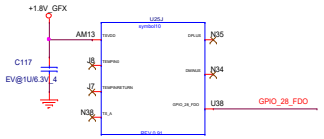
Vendor	TOP B/S QBCON	Mfr. P/N	SIZE	DBGDATA_[5:3]
Micron	AKG5QGUTL41	MT51J256M32HF-80:B	256Mx32	000
Hynix	AKG5QGUTW34	H5GC8H24AJR-R2C		001
Samsung	AKG5QGUT507	K4G80325FC-HC25		010
				011

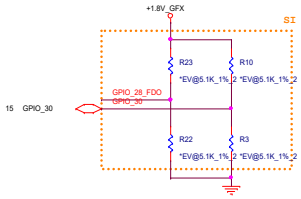
check with AMD

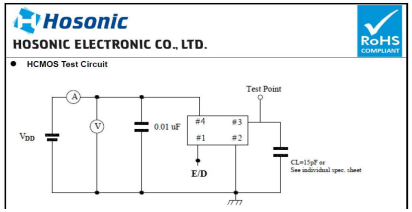
PROJECT : G3AC
Quanta Computer Inc.

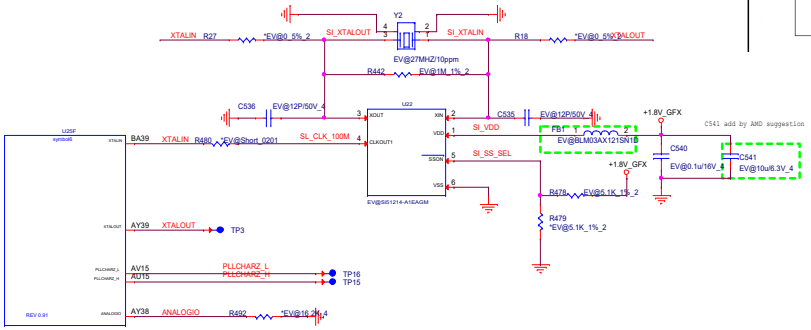
NB5

Size: Custom | Document Number: R17M-P1-70 - 4/5 (MISC) | Rev: 1A
Date: Tuesday, March 17, 2020 | Sheet 15 of 44





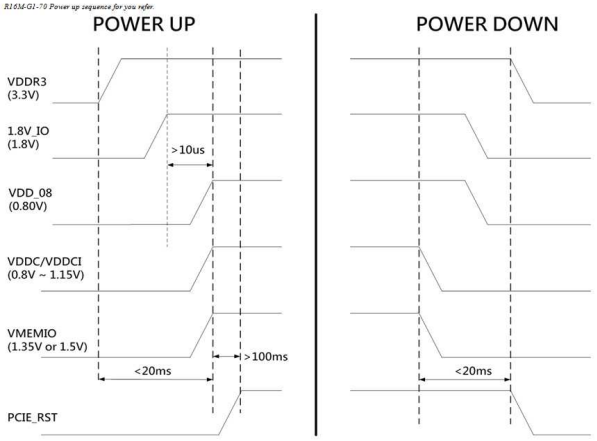




AMD GPIO Straping	Setting	Name	Description
GPIO 29	Pull low 10K ohm	BIF_VGA_DIS	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).
GPIO 20	Pull up 10K ohm	TX_DEEMPH_EN	PCI Express transmitter deemphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.
GPIO 0	Pull up 10K ohm	TX_HALF_SWING	Controls the transmitter full/half swing mode. 0: The transmitter full swing is enabled. 1: The transmitter half swing is enabled.
GPIO 22	Pull low 10K ohm	BIOS_ROM_EN	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.
GPIO 11	Pull up 10K ohm	ROM_CONFIG[2:0]	b) If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. GPIO_[13:12:11]=001=256MB
GPIO 12	Pull low 10K ohm		
GPIO 13	Pull low 10K ohm		
Hysnc	NC	Reserve	Reserve
Vsync	NC		

DBGDATA2	Pull up 10K ohm	AUD_PORT_CONN [2:0]	Determine the maximum number of digital display audio endpoints 101: Two usable endpoints
DBGDATA1	Pull low 10K ohm		
DBGDATA0	Pull up 10K ohm		
GPIO 1	Pull up 10K ohm	SMBUS_ADDR	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0x40 1: 0x41
GPIO 2	Pull up 10K ohm	BIF_GEN3_EN_A	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.
GPIO 8	connect CLKREQ#_GPU and add pull up / down resistor	BIF_CLK_PM_EN (Reserve)	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.
WAKEB	Pull low 10K ohm	OBFF	0: Disable
SVI2_SVC	Pull up 1Kohm	Boot up voltage	SVC:SVD=[1:0]=0.90V
SVI2_SVD	Pull low 1K ohm		

R16M-G1-70 Power up sequence for you refer.

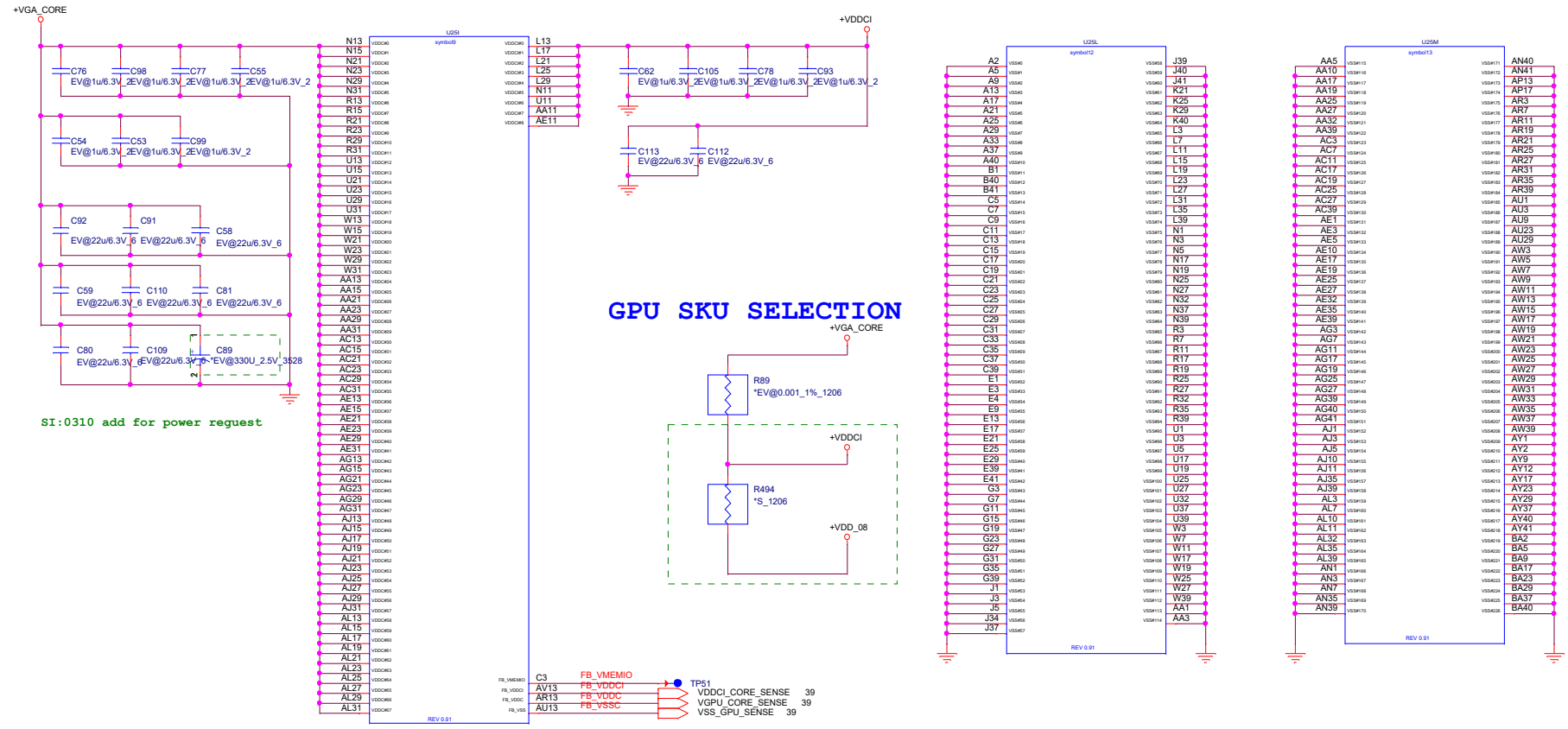


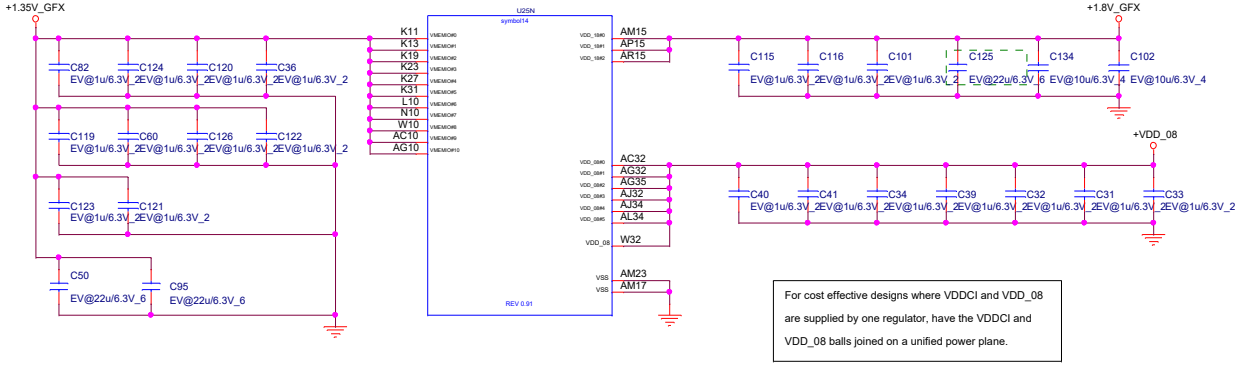
NB5

PROJECT : G3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R17M-P1-70 - 4/5 (MISC-2)	1A

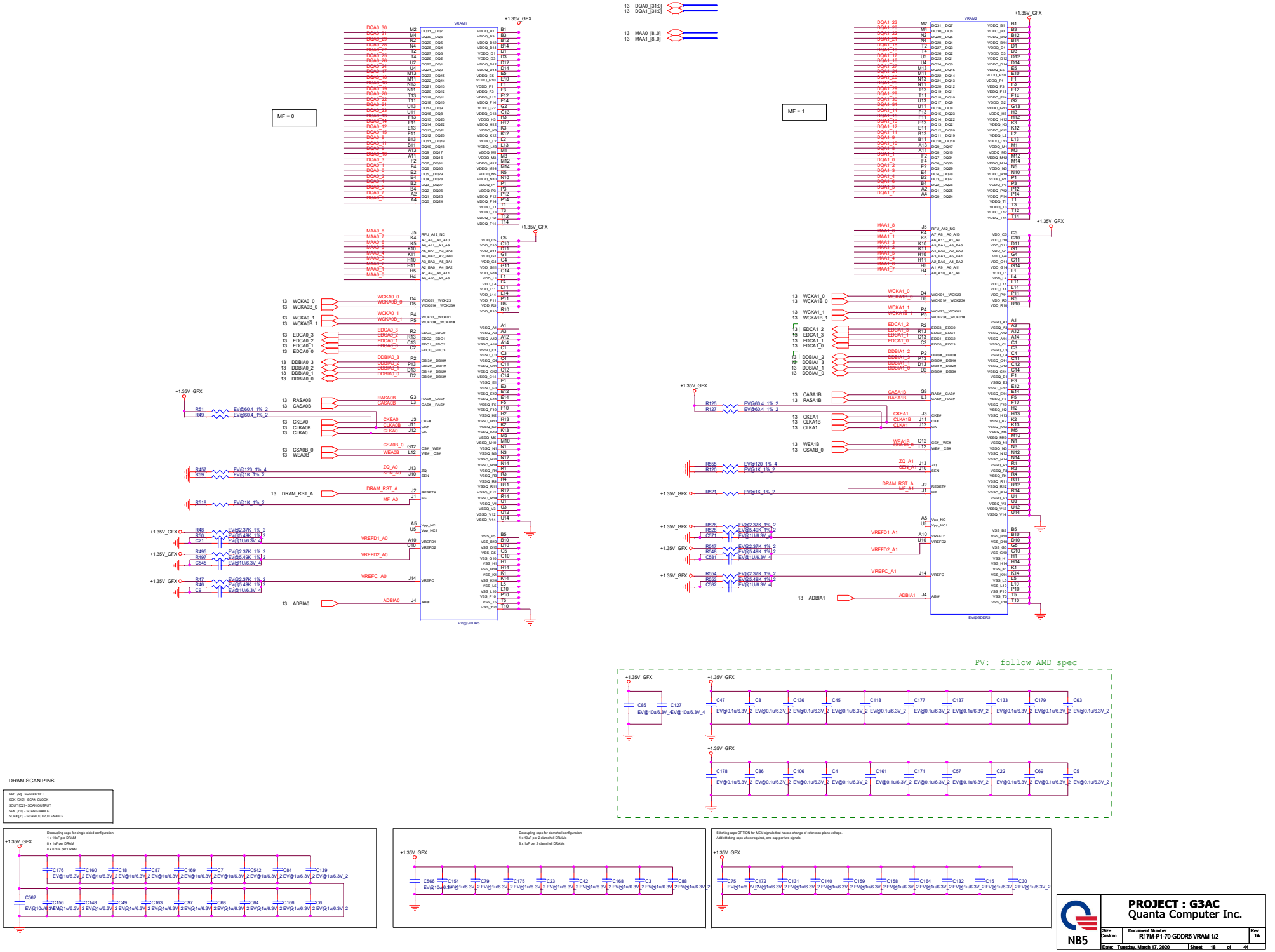
Date: Wednesday, March 18, 2020 Sheet 16 of 44



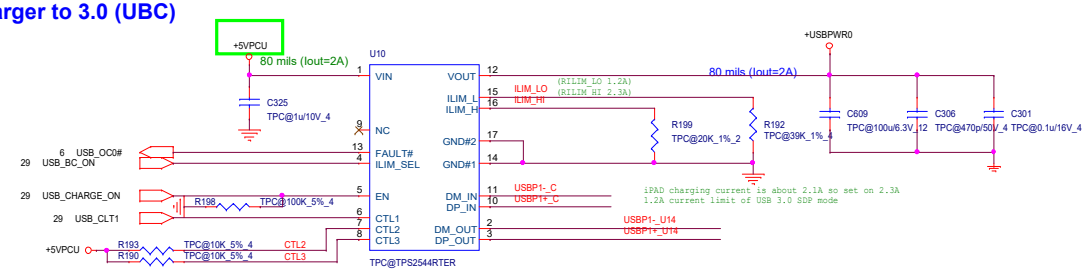


For cost effective designs where VDDCI and VDD_08 are supplied by one regulator, have the VDDCI and VDD_08 balls joined on a unified power plane.

NB5	**PROJECT : G3AC** Quanta Computer Inc.	
Size: Custom	Document Number: R17M-P1-70 - 5/5 (Power)	Rev: 1A
Date: Tuesday, March 17, 2020	Sheet 17 of 44	


MF = 0
MF = 1
VRAM1
VRAM2
+1.35V_GFX
DQA0_30
DQA0_31
DQA0_29
DQA0_28
DQA0_27
DQA0_25
DQA0_26
DQA0_24
DQA0_17
DQA0_16
DQA0_18
DQA0_19
DQA0_20
DQA0_22
DQA0_21
DQA0_23
DQA0_13
DQA0_14
DQA0_12
DQA0_15
DQA0_9
DQA0_11
DQA0_8
DQA0_10
DQA0_3
DQA0_1
DQA0_0
DQA0_2
DQA0_4
DQA0_5
DQA0_7
DQA0_6
DQA1_23
DQA1_20
DQA1_22
DQA1_21
DQA1_18
DQA1_19
DQA1_17
DQA1_16
DQA1_27
DQA1_24
DQA1_28
DQA1_25
DQA1_29
DQA1_26
DQA1_30
DQA1_31
DQA1_14
DQA1_15
DQA1_13
DQA1_12
DQA1_11
DQA1_9
DQA1_10
DQA1_8
DQA1_1
DQA1_0
DQA1_2
DQA1_3
DQA1_6
DQA1_5
DQA1_4
DQA1_7
13 DQA0_[31:0]
13 DQA1_[31:0]
13 MAA0_[8..0]
13 MAA1_[8..0]
MAA0_8
MAA0_7
MAA0_6
MAA0_5
MAA0_4
MAA0_3
MAA0_2
MAA0_1
MAA0_0
MAA1_8
MAA1_7
MAA1_6
MAA1_5
MAA1_4
MAA1_3
MAA1_2
MAA1_1
MAA1_0
WCKA0_0
WCKA0B_0
WCKA0_1
WCKA0B_1
WCKA1_0
WCKA1B_0
WCKA1_1
WCKA1B_1
EDCA0_3
EDCA0_2
EDCA0_1
EDCA0_0
EDCA1_2
EDCA1_3
EDCA1_1
EDCA1_0
DDBIA0_3
DDBIA0_2
DDBIA0_1
DDBIA0_0
DDBIA1_2
DDBIA1_3
DDBIA1_1
DDBIA1_0
RASA0B
CASA0B
RASA1B
CASA1B
CKEA0
CLKA0B
CLKA0
CKEA1
CLKA1B
CLKA1
CSA0B_0
WEA0B
WEA1B_0
CSA1B_0
ZQ_A0
SEN_A0
ZQ_A1
SEN_A1
DRAM_RST_A
MF_A0
MF_A1
VREFD1_A0
VREFD2_A0
VREFC_A0
VREFD1_A1
VREFD2_A1
VREFC_A1
ADBIA0
ADBIA1
EV@GDDR5
PV: follow AMD spec
DRAM SCAN PINS
SSN [J2] - SCAN SHIFT
SCK [G12] - SCAN CLOCK
SOUT [C2] - SCAN OUTPUT
SEN [J15] - SCAN ENABLE
SOEB [J1] - SCAN OUTPUT ENABLE
Decoupling caps for single-sided configuration
1 x 10uF per DRAM
8 x 1uF per DRAM
8 x 0.1uF per DRAM
Decoupling caps for clamshell configuration
1 x 10uF per 2 clamshell DRAMs
8 x 1uF per 2 clamshell DRAMs
Stitching caps OPTION for MEM signals that have a change of reference plane voltage.
Add stitching caps when required, one cap per two signals.
PROJECT : G3AC
Quanta Computer Inc.
NB5
Size: Custom
Document Number: R17M-P1-70-GDDR5 VRAM 1/2
Rev: 1A
Date: Tuesday, March 17, 2020
Sheet 18 of 44

USB Charger to 3.0 (UBC)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

iPAD charging current is about 2.1A so set on 2.3A
1.2A current limit of USB 3.0 SDP mode

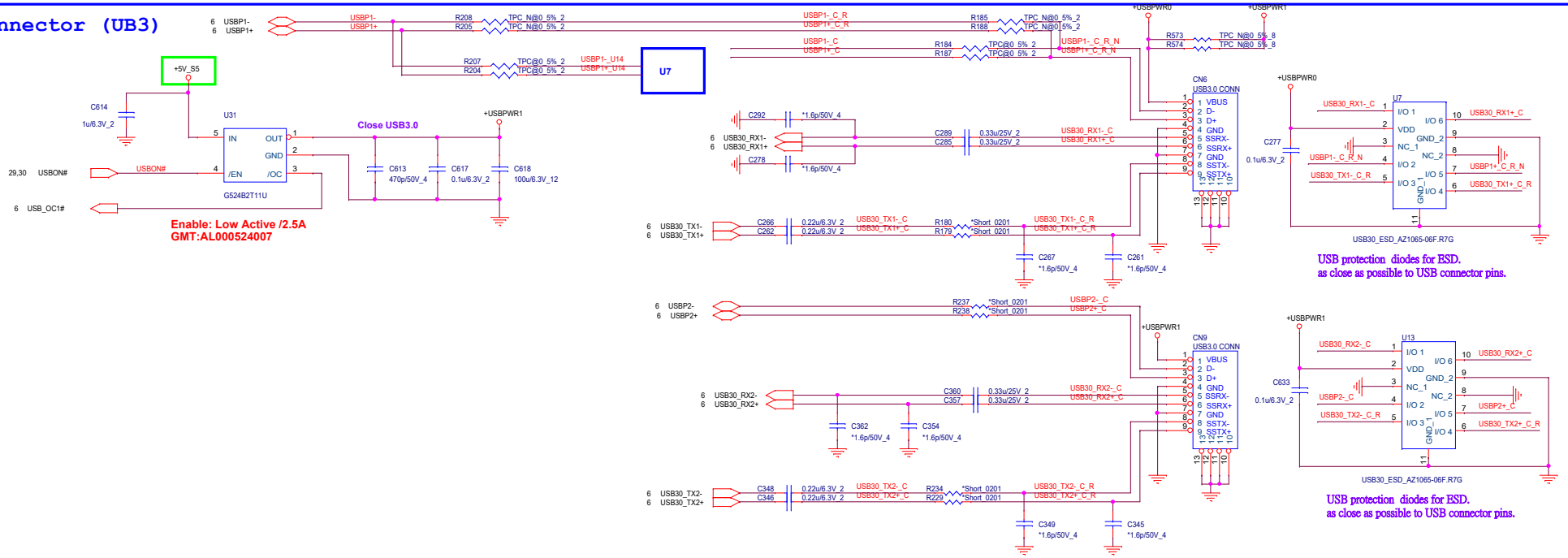
0326 TI AL002544001 (TPS2544RTER)

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

+5VPCU 21,27,32,33,37,41
+5V_S5 21,24,30,32,34,35,39
+3V 4,5,6,7,9,11,12,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,41

USB 3.0 Connector (UB3)



CAP close to different CONN

Quanta Computer Inc.
PROJECT : ZAUR

Size	Document Number	Rev
	USB3/Charger	1A

Date: Thursday, March 26, 2020 Sheet 19 of 44

eDP Conn.

2A / 80mils

2A/80mils

CCD DMIC POWER

TouchScreen POWER

1220 reserve for MS
1227 remove MS CCD/TS power rail=S0
stuff R508, R80

CCD-USB

TS-USB

TP_SCL, TP_SDA
Open Drain,
Pull high 2.2Kohm

From APU WOV

1227 remove WOV, stuff R52, R53

LCD back light

PCH

EC

2.5A / 100mils

Enable:High Active /2.5A
SGY : AL006288003
GMT: AL00524004

HID-I2C Touch screen

TP_SCL, TP_SDA
Open Drain,
Pull high 2.2Kohm

I2C Touch Panel interrupt

S5

S0

Quanta Computer Inc.	
PROJECT : ZAUR	
Size	Document Number: eDP CONN/LID/CAM/D-MIC/TS — Rev: 1A
Date: Wednesday, March 18, 2020	Sheet 20 of 44

Codec(ADO)

CPVDD PWR

Codec PWR 1.8V(ADO)

Codec PWR 5V(ADO)

Mute(ADO)

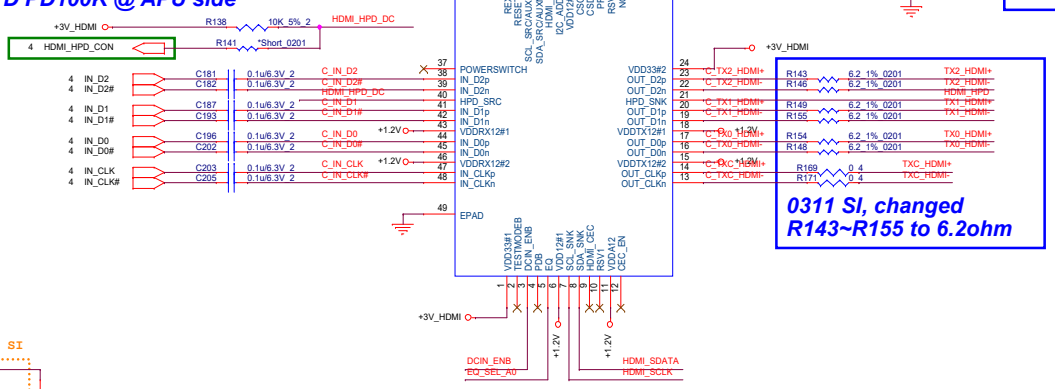
Internal Speaker

Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

WW G2 @ ALC256 : AL000256009
MGF G3 @ ALC3256M:
ALC255 : AL000255000- Design reserved

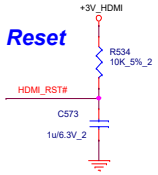
Quanta Computer Inc.
PROJECT : ZAUR
Size | Document Number: Audio Codec/HP/SPK/Hole | Rev 1A
Date: Tuesday, March 17, 2020 | Sheet 21 of 44

HDMI_HPD PD100K @ APU side

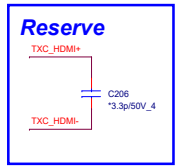


0311 SI, changed R143~R155 to 6.2ohm

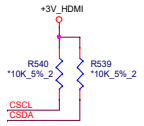
Reset

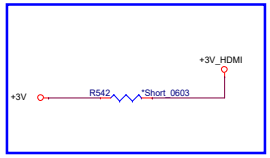


Reserve

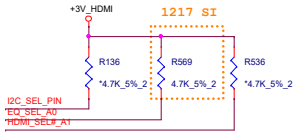


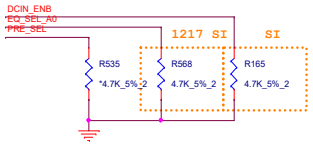
Optional





PS8409 strap pin





DCIN_ENB
DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default,AC coupling input

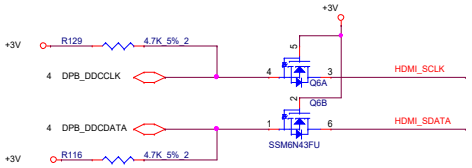
EQ_SEL_A0
Receiver equalization setting; Internal pull up , 3.3V I/O.
L: Compensaton for channel loss up to 13dB
H: Default , Compensation for channel loss up to 17dB
M: Compensation for channel loss up to 11dB

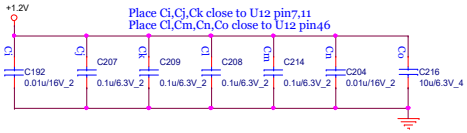
PRE_SEL
Output pre-emphasis setting; Internal pull up, 3.3V I/O.
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis

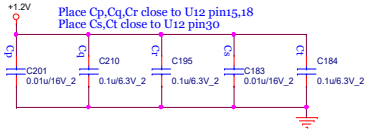
HDMI_SEL#_A1
HDMI_ID enable ; Internal pull down , 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable

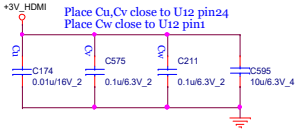
I2C_SEL_PIN
I2C Slave Address selection; Internal pull down, 3.3V I/O.
L: Default, Slave address 0x10-0x2F.
H: Alternative salve address 0x90-0x9F, 0xD0-0xDF.

0311 SI, changed R129, R116 to 4.7K

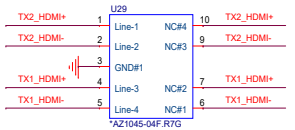


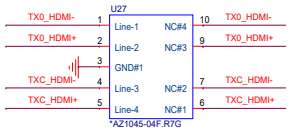




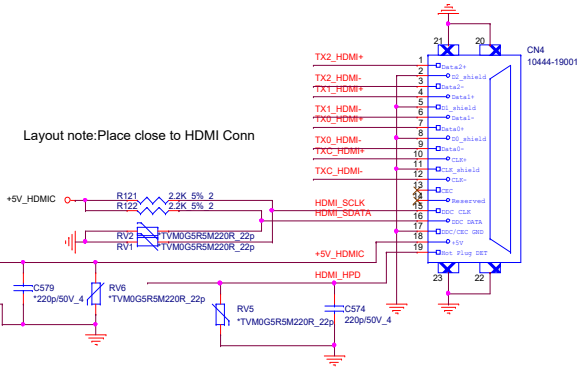


For ESD
Layout note:Place close to HDMI Conn





Layout note:Place close to HDMI Conn



40 mils

LAN RTL8111H-CG

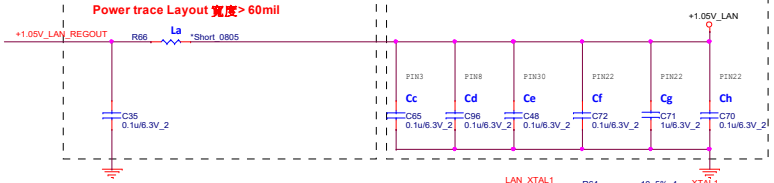
For LDO mode support

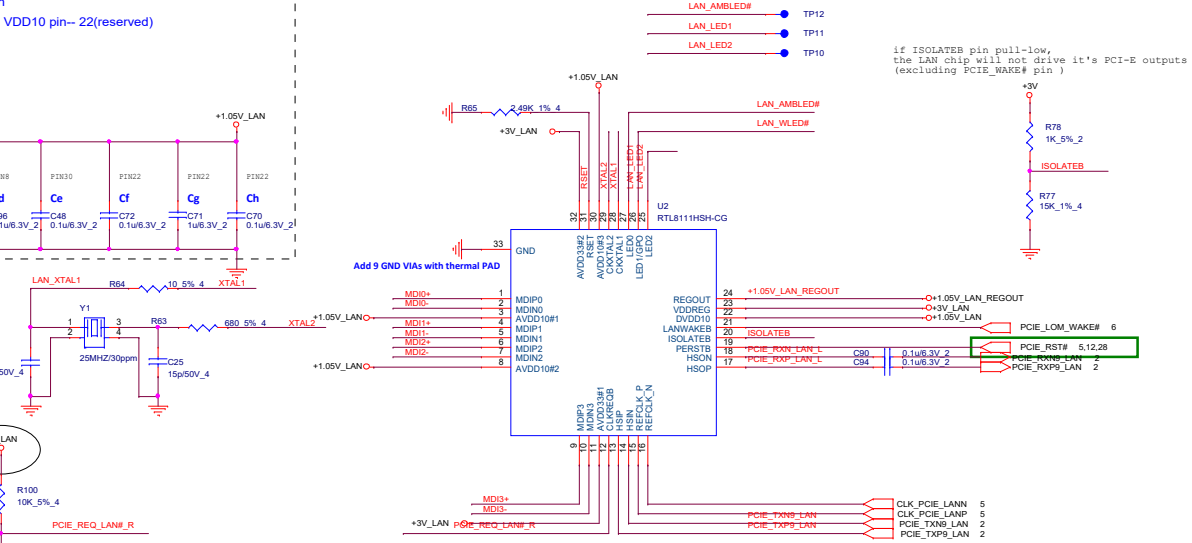
Stuff: La, Ca ,Cb

* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30

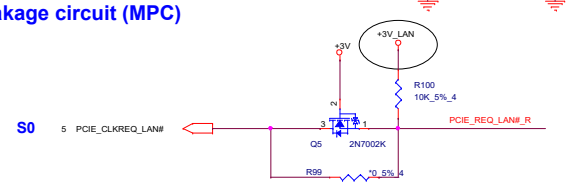
* Place Cg,Ch
close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬度> 60mil



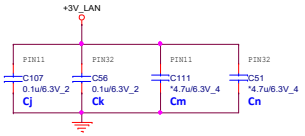


Leakage circuit (MPC)

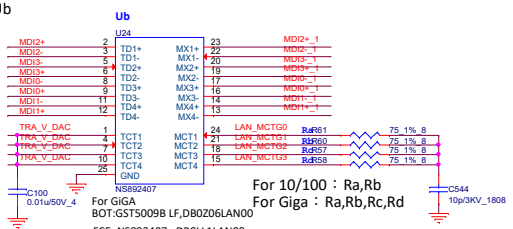


* Place Cj and Ck, close to each VDD33 pin-- 11, 32

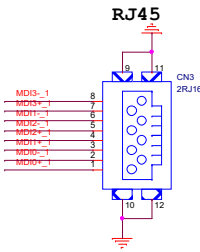
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



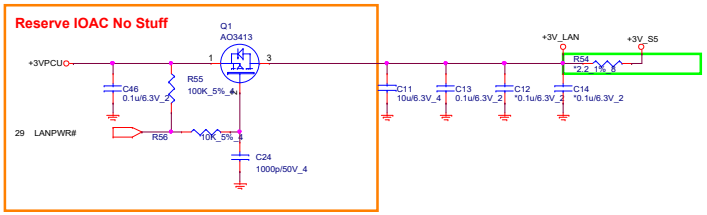
For Giga：Ub



RJ45



Reserve IOAC No Stuff



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	LAN RTL8111H	1A
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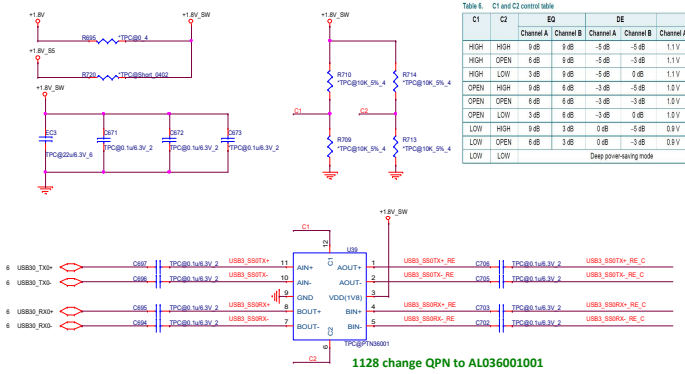
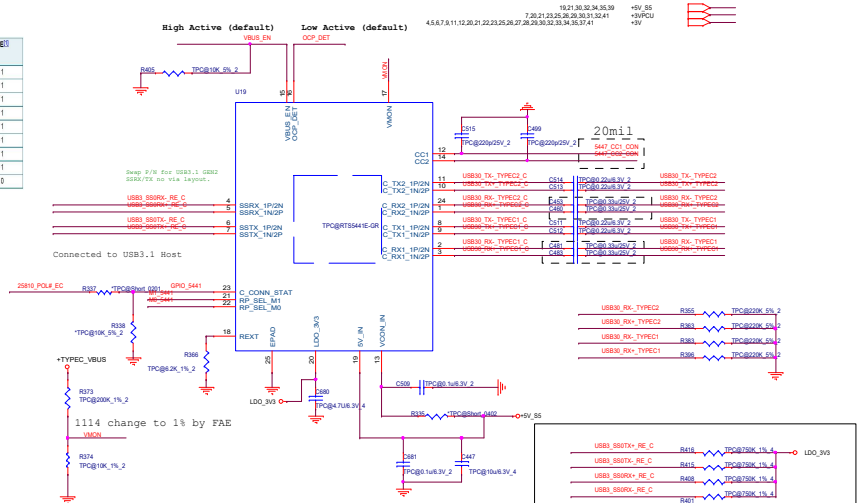
TYPE C and MUX PI2EQX632EXUBE

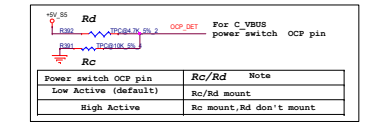
8.4 C1 and C2 overall control table

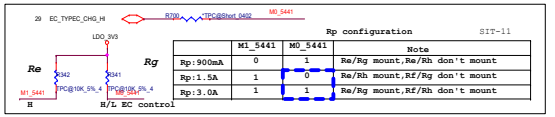
Table 6. C1 and C2 control table

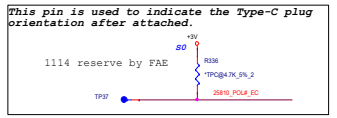
C1	C2	EQ		DE		OS		CBT
		Channel A	Channel B	Channel A	Channel B	Channel A	Channel B	
HIGH	HIGH	9 dB	9 dB	-5 dB	-5 dB	1.1 V	1.1 V	1
HIGH	OPEN	6 dB	9 dB	-5 dB	-3 dB	1.1 V	1.0 V	1
HIGH	LOW	3 dB	9 dB	-5 dB	0 dB	1.1 V	0.9 V	1
OPEN	HIGH	9 dB	6 dB	-3 dB	-5 dB	1.0 V	1.1 V	1
OPEN	OPEN	6 dB	6 dB	-3 dB	-3 dB	1.0 V	1.0 V	1
OPEN	LOW	3 dB	6 dB	-3 dB	0 dB	1.0 V	0.9 V	1
LOW	HIGH	9 dB	3 dB	0 dB	-5 dB	0.9 V	1.1 V	1
LOW	OPEN	6 dB	3 dB	0 dB	-3 dB	0.9 V	1.0 V	1
LOW	LOW	Deep power-saving mode						0



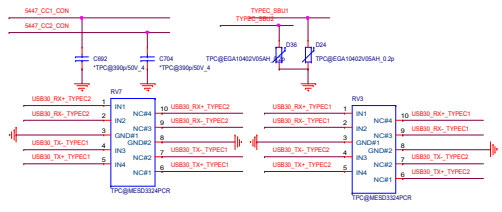


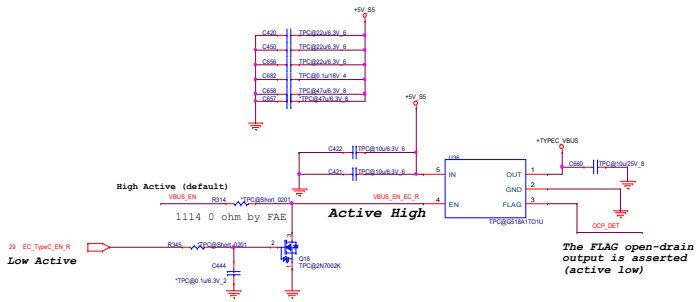


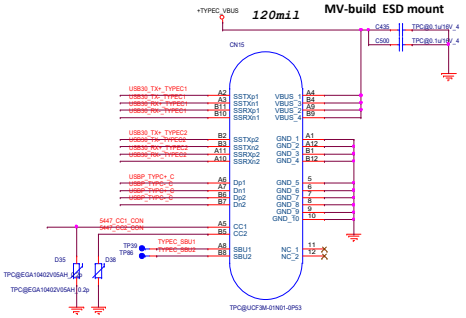




TYPE C USB3.0 ESD







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	USB SW/TYPE-C RT5447 & Re-driver		1A
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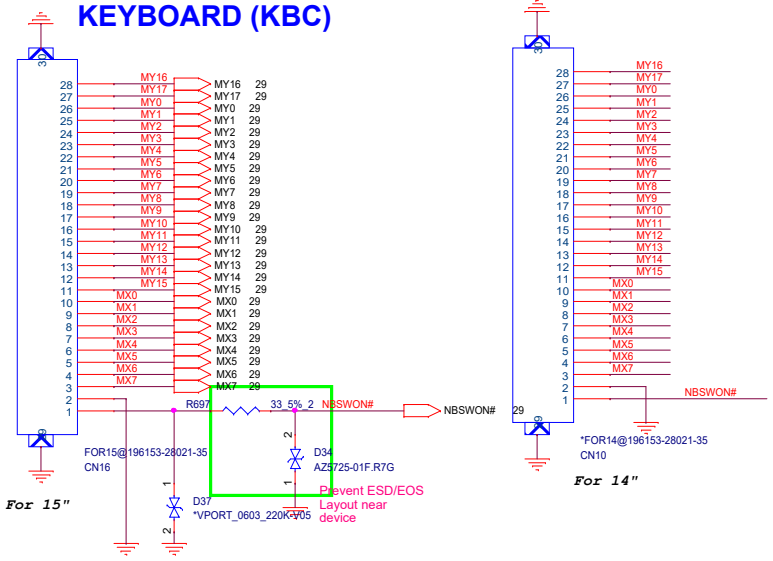
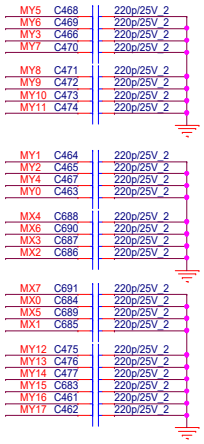
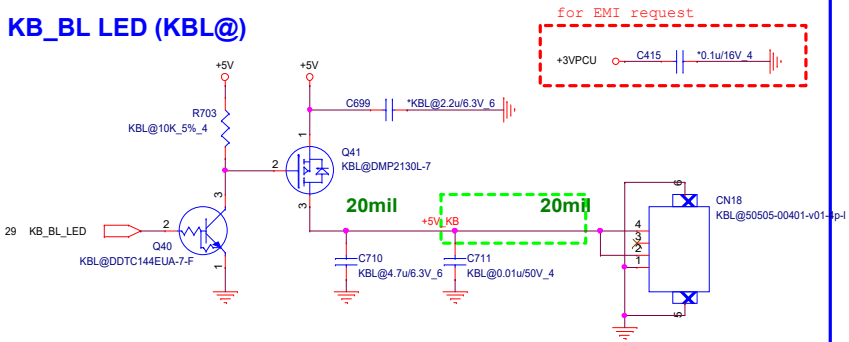
KEYBOARD (KBC)

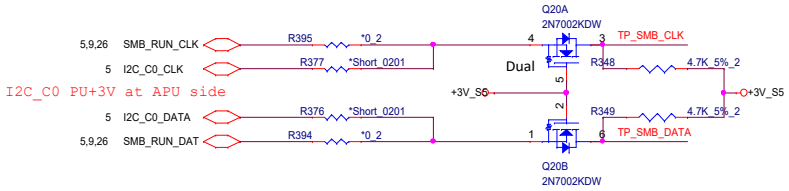


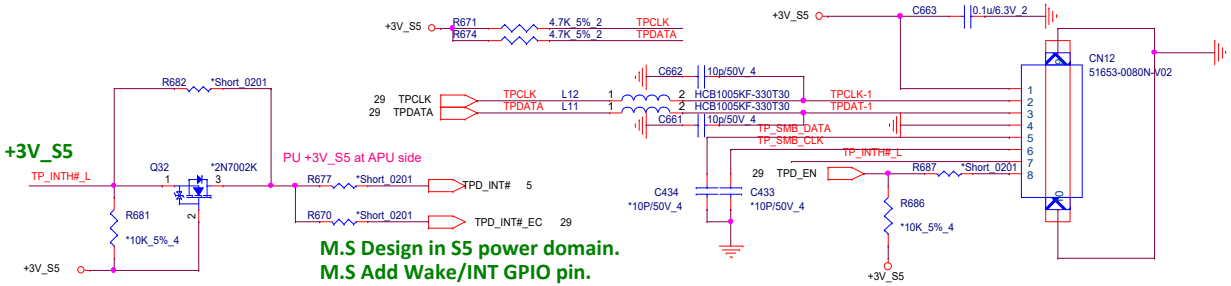


KB_BL LED (KBL@)

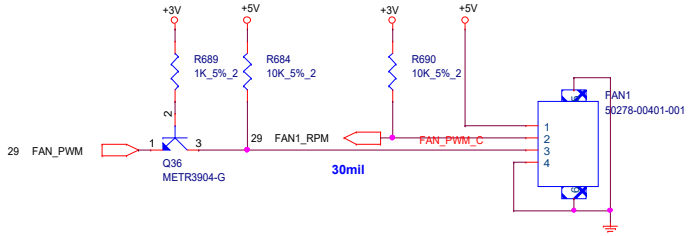


Touch Pad





FAN



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	KB/TP/FAN	1A

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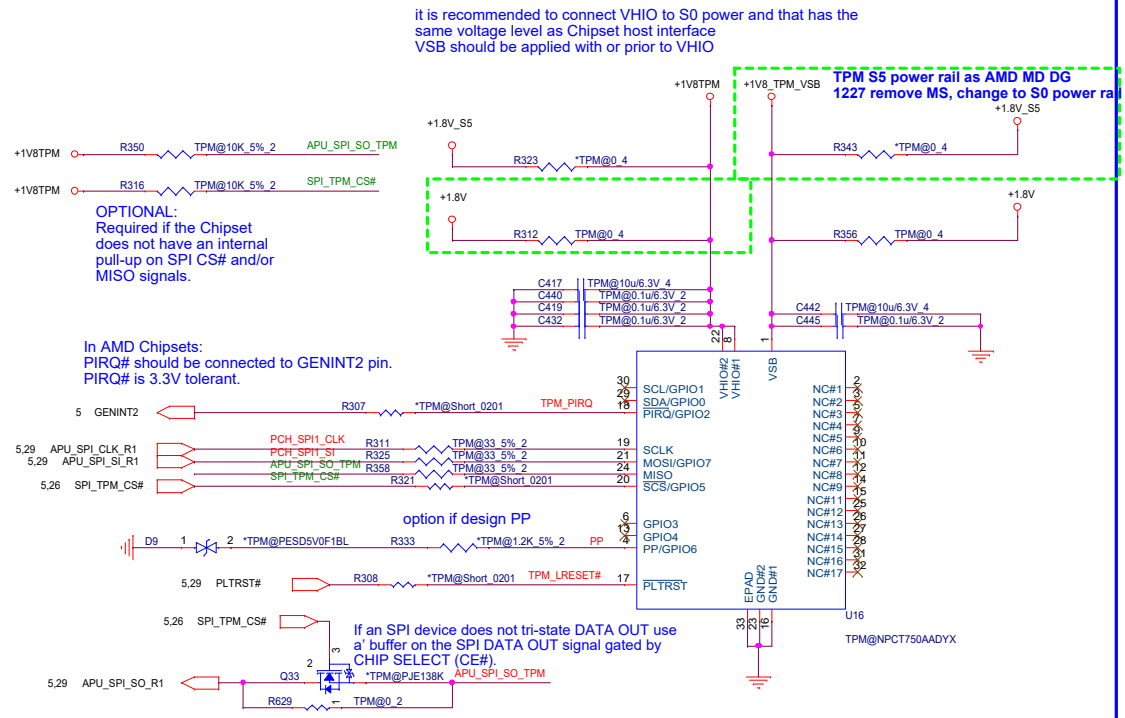
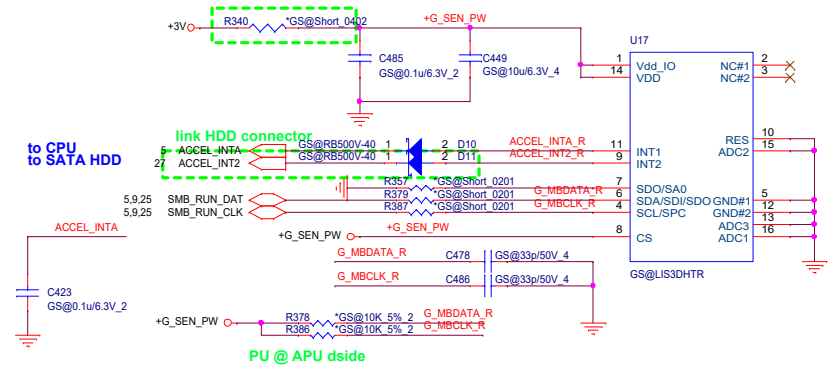
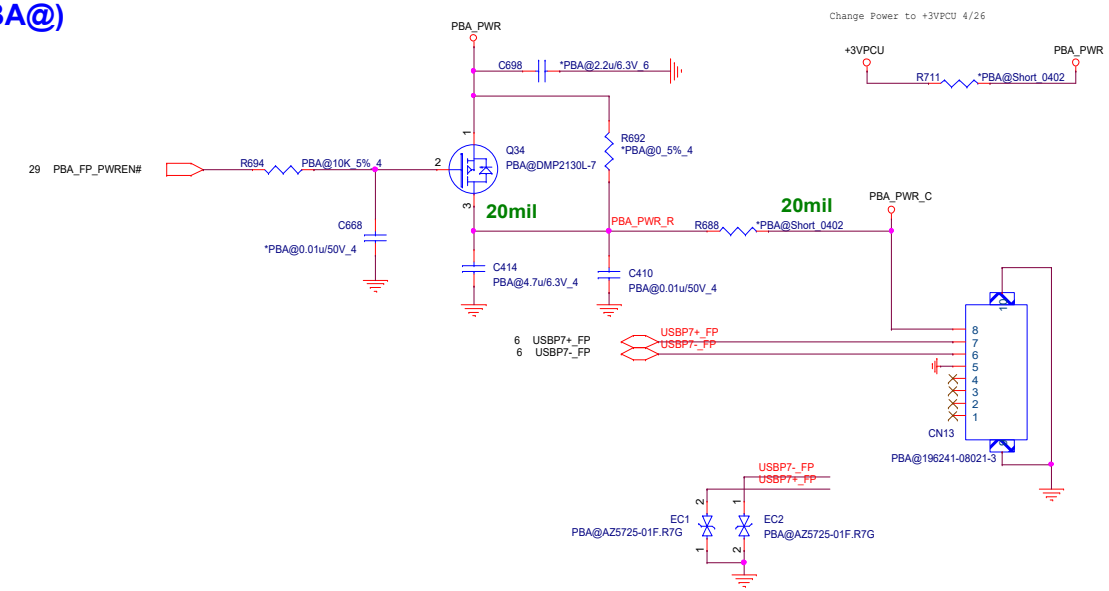
TPM NPCT750



G-sensor (GS@)



PBA (PBA@)



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	TPM/G-Sensor/PBA		1A
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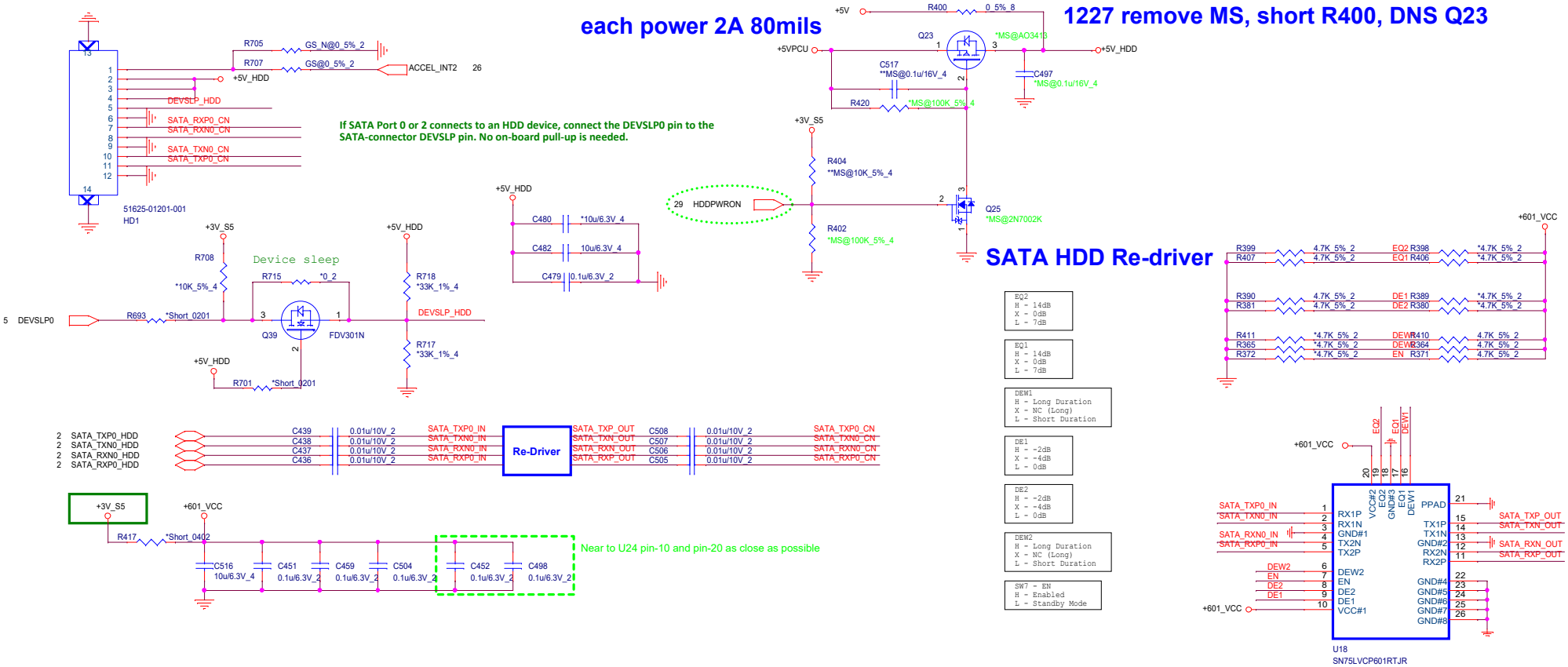
SATA HDD

M.S SATA SSD devices should be powered from S5 rail during S0i3, and should support DEVSLP as well as HIPM functionality. The SATA SSD power should be gated by EC GPIO during S3, S4, and S5.

19,21,24,30,32,34,35,39 +5V_S5
20,21,22,25,32,37 +5V
4,5,6,7,9,11,12,20,21,22,23,24,25,26,28,29,30,32,33,34,35,37,41 +3V
5,6,7,11,20,21,23,25,28,29,32,37,38 +3V_S5

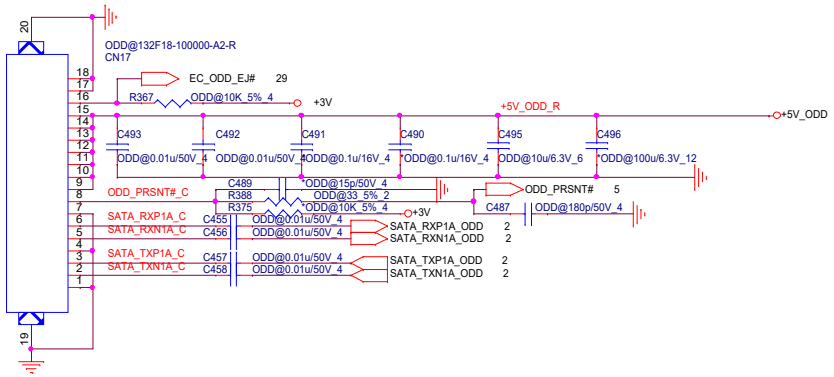
each power 2A 80mils

1227 remove MS, short R400, DNS Q23

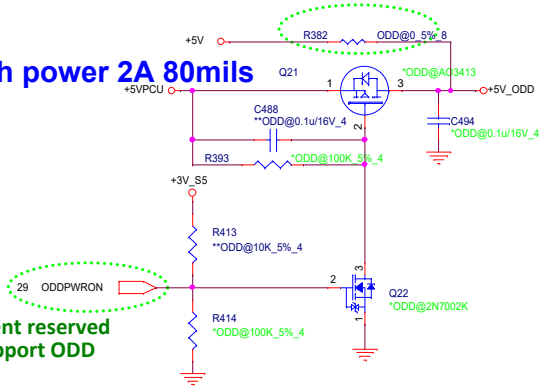


SATA HDD Re-driver

SATA ODD (ODD@)



each power 2A 80mils



M.S EC assignment reserved
A3/A5 do not support ODD

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	HDD/ ODD	1A
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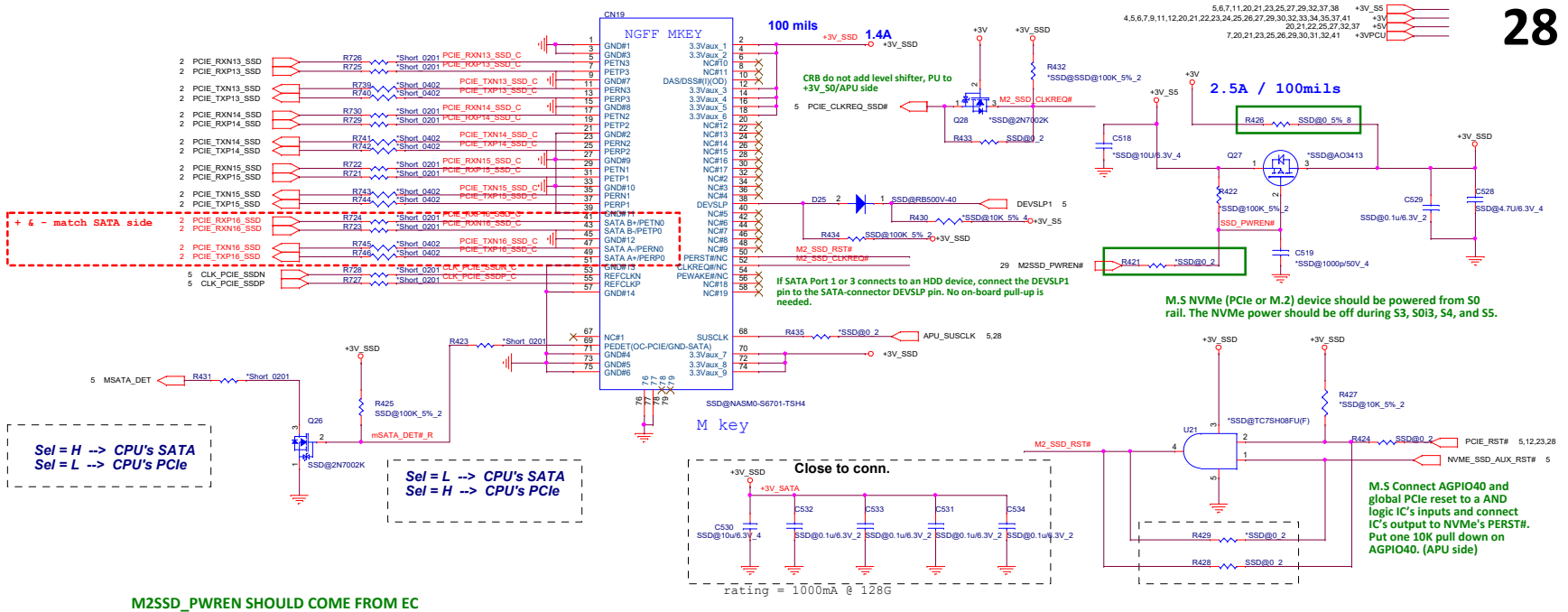
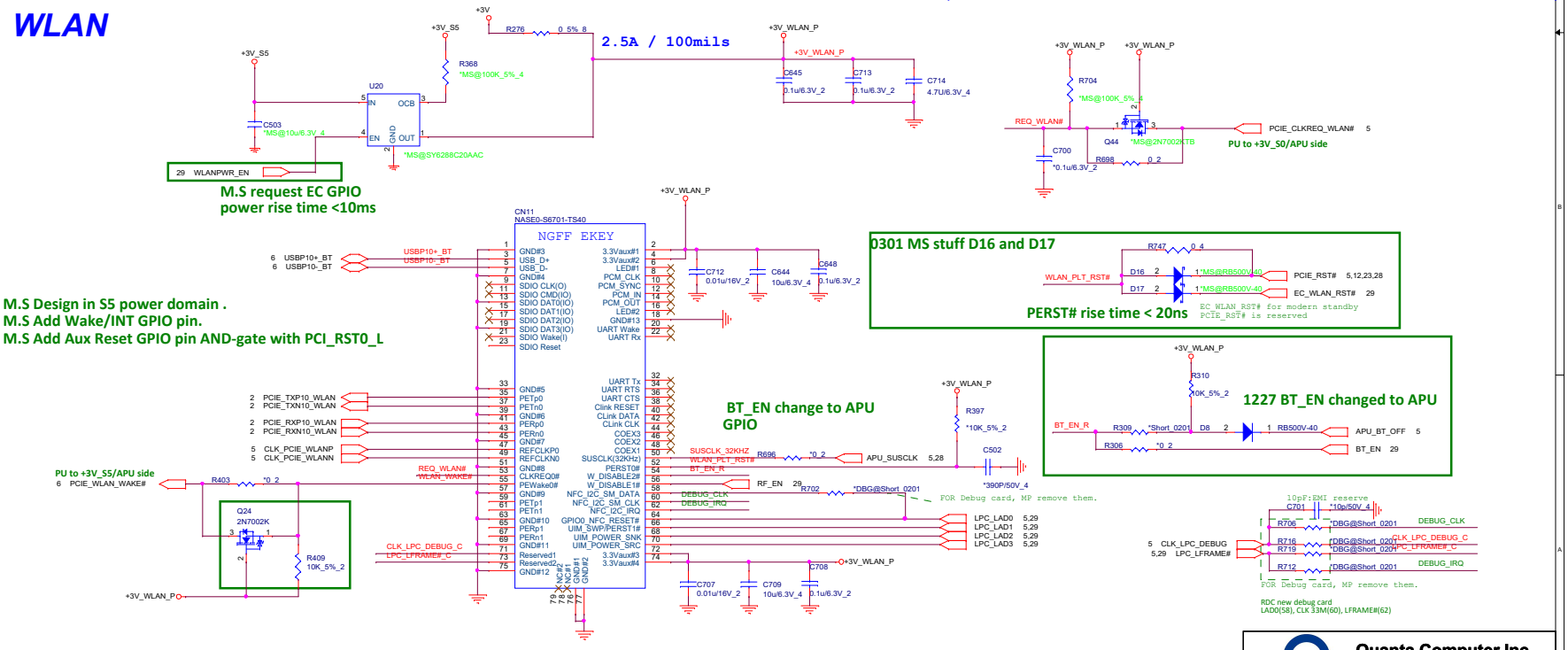


WLAN



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	HDD/WLAN(NGFF)		1A
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EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

12 mils

(For PLL Power)

IT8987E/BX LQFP

AJ089870F01 IT8987E/BX

1217 new GPIO

Output for type-c Apling ridge reset timming"Low " Active

Pin 80 EC_APWROK reserve TP

1218 HY add 2ND_S5ON for +3V_S5

Prevent ESD/EOS Layout near device

Near EC

dGPU PROCHOT

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA/DDR
SM Bus 3	
SM Bus 4	

1203 SIO_RCIN# have to stuff PU

reserve SERIRQ PU at APU side

PLTRST# PD as ZAS

1202 ITE suggest stuff RSMRST# PD

TVS PN:
Priority1: CY000220Z00
Priority2: CY402220B00

SM BUS PU(KBC)

Battery module

UMA& VGA, thermal IC

HWPG(KBC)

+VCC_CORE_PWRGD

Reset SW (FSW)

R233 should be always keep 0-ohm for option to switch Battery Detect Switch

Reserve switch for test (MP remove)

Reserve switch for test (MP remove)

BIOS/EC shared ROM(16MB)

share rom

1.8V_16MB
MX AKE5DFN0Z02
WND AKE5DF-0N00

SPI NOR FLASH(128KB) (KBC)
reserve for EC debug
3V3 SPI rom, check PN

for EC rom only

MX25U12835FM2I-10G

BIOS every pin need add TP2675(First)/TP2650 for ICT test test pad must place in TOP side

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	KBC IT8987	1A
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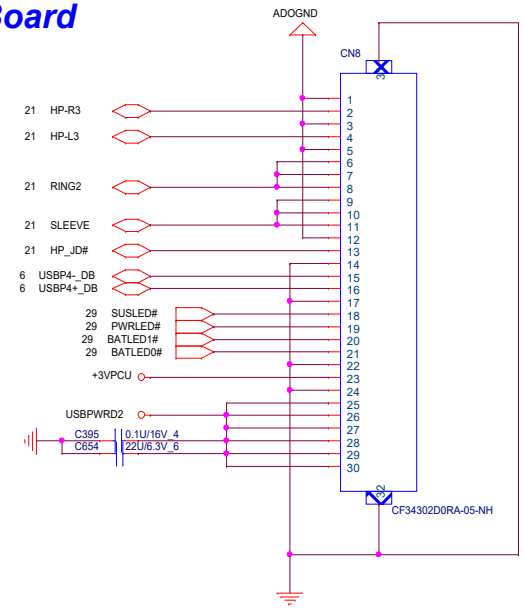
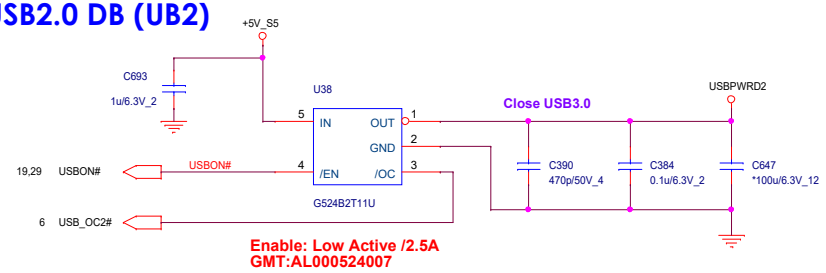
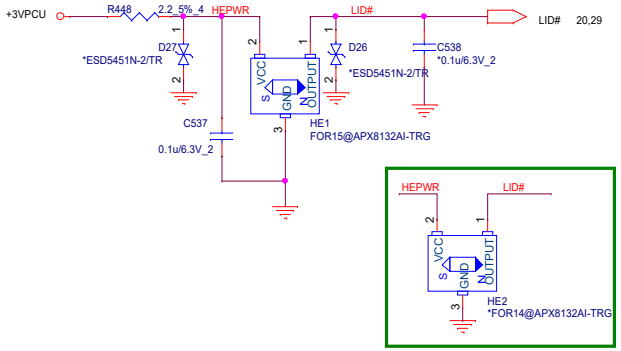
USB Board



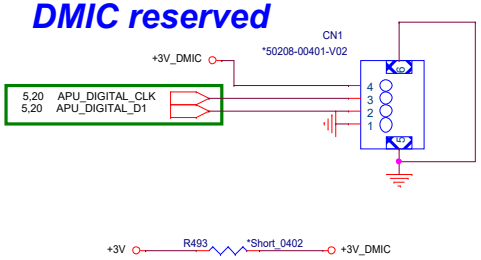
USB2.0 DB (UB2)



Hall Sensor



DMIC reserved



Quanta Computer Inc.

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	USB DB/Hall sensor/DMIC	1A
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PJ11 note:
45W black DFPJ03MR149, DFPJ03MR154
65W yellow DFPJ03MR148, DFPJ03MR155

PJ11 30706-00042-001

[11/11] change PJ11 from DFPJ03MR143 to DFPJ03MR149

12/25 Change PQ1&PQ3 to AONS32306 for shortage

12/18 PR352 modify by TI comment

12/18 PR85 modify by TI comment

12/18 PC267 modify by TI comment

12/18 PR328 modify by TI comment

12/18 PR336,PR339 modify by TI comment

ACDET=16.4V

BQ24780S : 1 µA/W (default)

*AMD CPU DOESN'T NEED TO REPORT PMON

Double Check if BI pin PU Low

1. PROCHOT Pin : Active Low
2. Double Check PU High with HW

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

ILIM=0.793V
Rsr = 0.01ohm

10/24 change netname to VRHOT

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+3V 4,5,6,7,9,11,12,20,21,22,23,24,25,26,27,28,29,30,33,34,35,37,41
+5V_S5 19,21,24,30,34,35,39
+5V 20,21,22,25,27,37
+3V_S5 5,6,7,11,20,21,23,25,27,28,29,37,38

+VIN 20,31,33,34,35,36,37,38,39,40,41
+3VPCU 7,20,21,23,25,26,29,30,31,41
+5VPCU 19,21,27,33,37,41
VL 37

+3VPCU
3.3 Volt +/- 5%
TDC : 6A
Width : 240mil
FSW : 500KHZ

+5VPCU
5 Volt +/- 5%
TDC : 8A
Width : 320mil
FSW : 750KHZ

To Thermal Protection

High frequency noise eliminate circuit

Power Auto Recovery

VCC=5V
(DON'T Connect to External Load)

(1) USM : 0.8V-1.7V
(2) Normal Mode : >2.3V

LDO=3.3V/100mA

LDO= 5V/100mA

C-[12/23] delet PJ16

C-[12/23] delet PJ19

C-[12/23] 0603->0402

PU13 RT6256BGQUF

PU15 RT6258CGQUF

PU4 AOZ1331ADI

PU5 AOZ1331ADI

PQ10 2N7002K

PQ11 2N7002K

TDC : 4.58A
PEAK : 6.1A
Width : 200mil

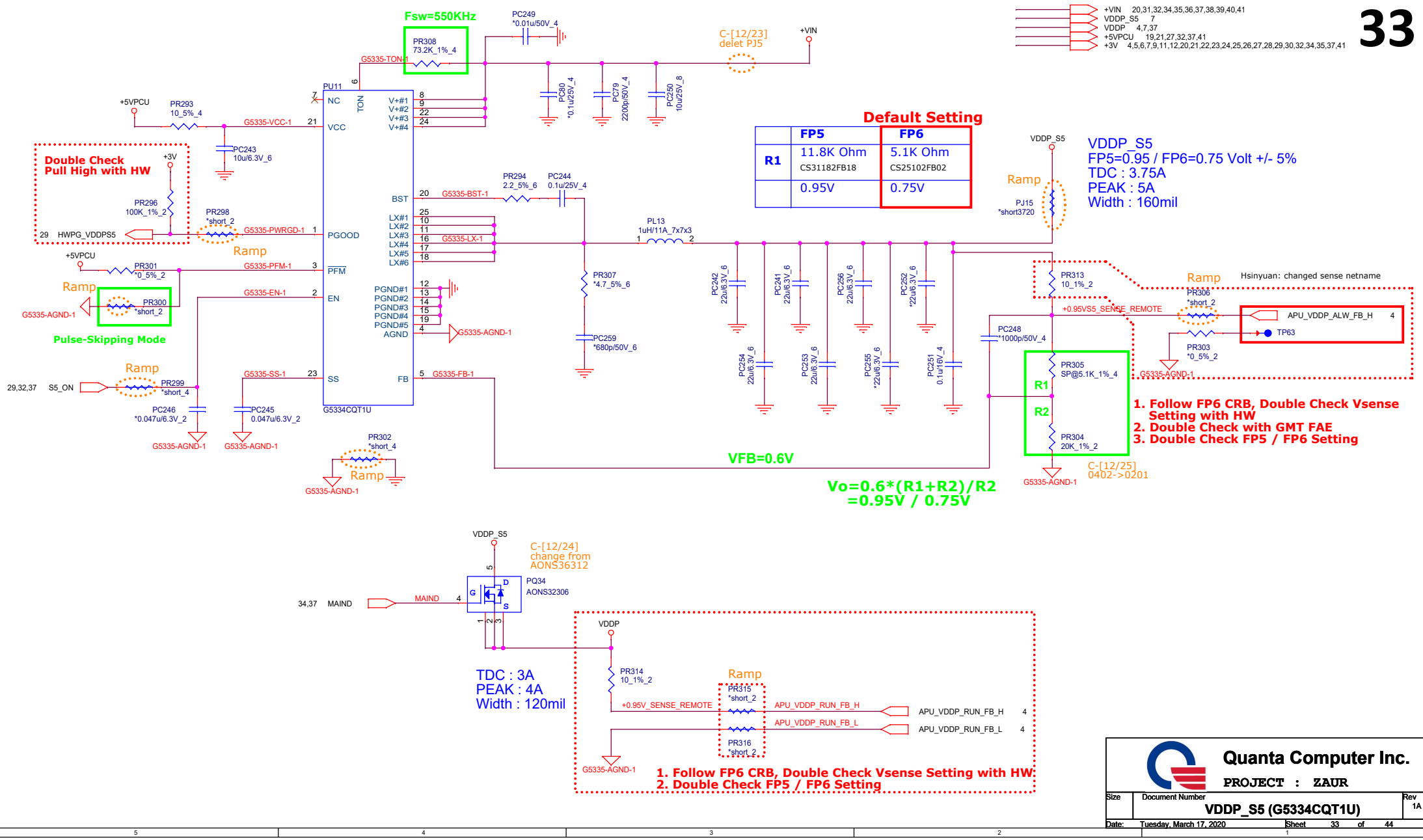
TDC : 3.43A
PEAK : 4.6A
Width : 160mil

TDC : 4.54A
PEAK : 6A
Width : 200mil

TDC : 3.53A
PEAK : 4.7A
Width : 160mil

1218 HY

Quanta Computer Inc.	
PROJECT : ZAUR	
Size	Document Number: SYSTEM 5V/3V (RT6256B/RT6258C) — Rev 1A
Date: Tuesday, March 17, 2020	Sheet 32 of 44


Fsw=550KHz
PR308 73.2K_1%_4
PC249 *0.01u/50V_4
C-[12/23] delet PJ5
+VIN
G5335-TON-1
PU11
NC
TON
V+#1
V+#2
V+#3
V+#4
VCC
BST
LX#1
LX#2
LX#3
LX#4
LX#5
LX#6
PGOOD
PFM
EN
PGND#1
PGND#2
PGND#3
PGND#4
PGND#5
AGND
SS
FB
G5334CQT1U
PC80 *0.1u/25V_4
PC79 2200p/50V_4
PC250 10u/25V_8
+5VPCU
PR293 10_5%_4
G5335-VCC-1
PC243 10u/6.3V_6
Double Check Pull High with HW
+3V
PR296 100K_1%_2
PR298 *short_2
29 HWPG_VDDPS5
G5335-PWRGD-1
Ramp
PR294 2.2_5%_6
PC244 0.1u/25V_4
G5335-BST-1
PL13 1uH/11A_7x7x3
G5335-LX-1
PR307 *4.7_5%_6
PC259 *680p/50V_6
PC242 22u/6.3V_6
PC241 22u/6.3V_6
PC256 22u/6.3V_6
PC252 *22u/6.3V_6
PC254 22u/6.3V_6
PC253 22u/6.3V_6
PC255 *22u/6.3V_6
PC251 0.1u/16V_4
PC248 *1000p/50V_4
+5VPCU
PR301 *0_5%_2
G5335-PFM-1
Ramp
PR300 *short_2
G5335-AGND-1
G5335-EN-1
Pulse-Skipping Mode
29,32,37 S5_ON
Ramp
PR299 *short_4
G5335-SS-1
PC246 *0.047u/6.3V_2
PC245 0.047u/6.3V_2
G5335-AGND-1
G5335-AGND-1
PR302 *short_4
Ramp
G5335-AGND-1
G5335-FB-1
VFB=0.6V
Vo=0.6*(R1+R2)/R2
=0.95V / 0.75V
Default Setting
FP5
FP6
R1
11.8K Ohm
CS31182FB18
5.1K Ohm
CS25102FB02
0.95V
0.75V
VDDP_S5
Ramp
PJ15 *short3720
VDDP_S5
FP5=0.95 / FP6=0.75 Volt +/- 5%
TDC : 3.75A
PEAK : 5A
Width : 160mil
PR313 10_1%_2
+0.95VS5_SENSE_REMOTE
PR305 SP@5.1K_1%_4
R1
R2
PR304 20K_1%_2
G5335-AGND-1
C-[12/25] 0402->0201
Ramp
Hsinyuan: changed sense netname
PR306 *short_2
APU_VDDP_ALW_FB_H 4
TP63
PR303 *0_5%_2
G5335-AGND-1
1. Follow FP6 CRB, Double Check Vsense Setting with HW
2. Double Check with GMT FAE
3. Double Check FP5 / FP6 Setting
+VIN 20,31,32,34,35,36,37,38,39,40,41
VDDP_S5 7
VDDP 4,7,37
+5VPCU 19,21,27,32,37,41
+3V 4,5,6,7,9,11,12,20,21,22,23,24,25,26,27,28,29,30,32,34,35,37,41
33
VDDP_S5
C-[12/24] change from AONS36312
34,37 MAIND
MAIND 4
PQ34 AONS32306
TDC : 3A
PEAK : 4A
Width : 120mil
VDDP
PR314 10_1%_2
Ramp
PR315 *short_2
PR316 *short_2
+0.95V_SENSE_REMOTE
APU_VDDP_RUN_FB_H
APU_VDDP_RUN_FB_L
APU_VDDP_RUN_FB_H 4
APU_VDDP_RUN_FB_L 4
G5335-AGND-1
1. Follow FP6 CRB, Double Check Vsense Setting with HW
2. Double Check FP5 / FP6 Setting
Quanta Computer Inc.
PROJECT : ZAUR
Size
Document Number
VDDP_S5 (G5334CQT1U)
Rev 1A
Date: Tuesday, March 17, 2020
Sheet 33 of 44

+5V_S5 19,21,24,30,32,35,39
+3V 4,5,6,7,9,11,12,20,21,22,23,24,25,26,27,28,29,30,32,33,35,37,41

+VIN 20,31,32,33,35,36,37,38,39,40,41
+1.2VSUS 3,7,9,10
+1.2V 22,37
+2.5V_SUS 9,10
+VDDQ_VTT 9,10
+VDDQ 9,10

+2.5V_SUS
2.5Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+1.2VSUS
1.2 Volt +/- 5%
TDC : 8A
Width : 320mil

TDC : 0.45A
PEAK : 0.6A
Width : 20mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

TDC : 0.23A
PEAK : 0.3A
Width : 20mil

Double Check Pull High with HW

	VTT_CNTL	SLP_S4	+1.2VSUS	+2.5VSUS	REF	VTT
S0	1	1	ON	ON	ON	ON
S3	0	1	ON	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZAUR

Size	Document Number	Rev
	DDR4_+1.2VSUS (TPS51486R)	1A

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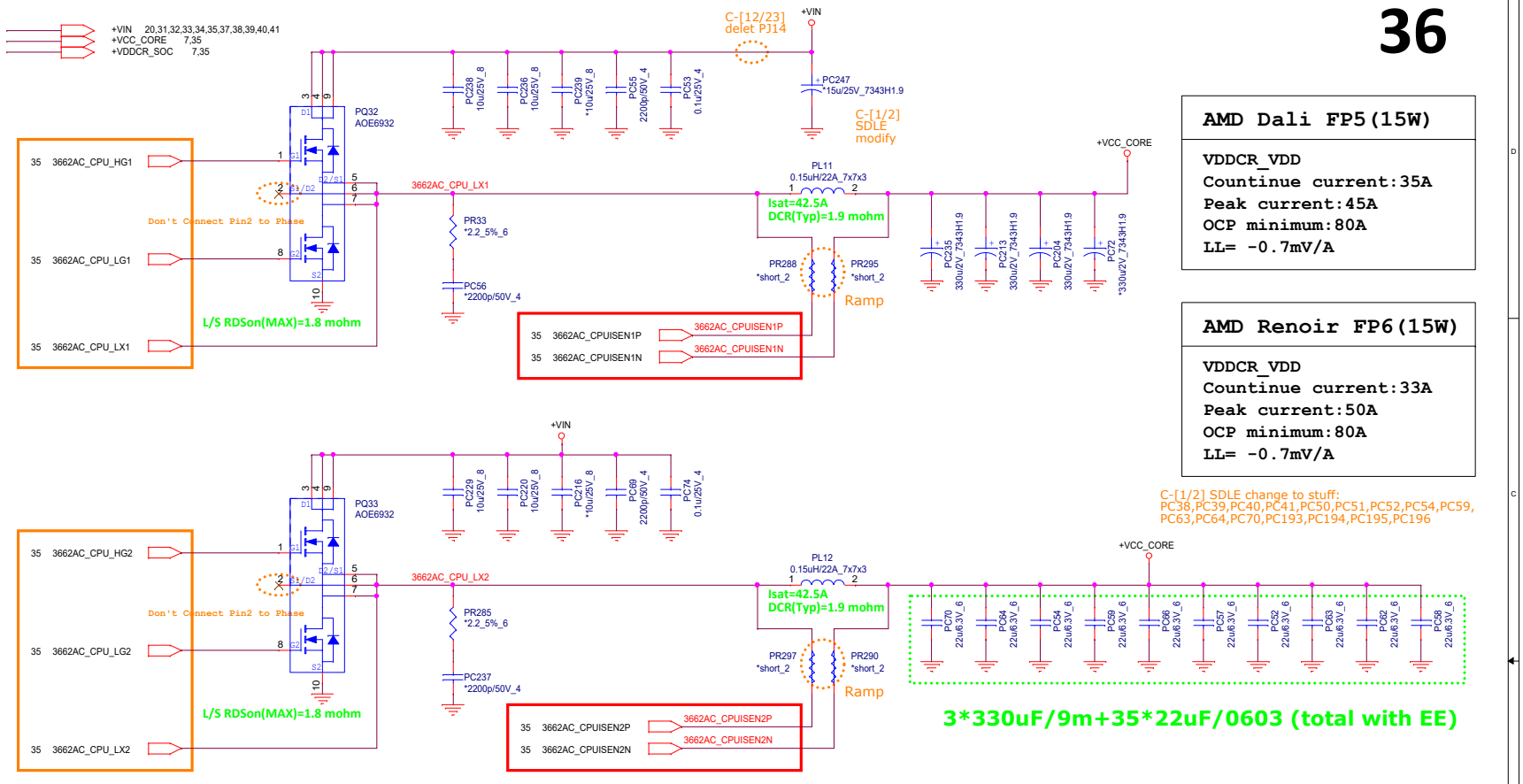
+VDDCR_SOC 7,36
+VCC_CORE 7,36
+5V_S5 19,21,24,30,32,34,39
+1.8V 4,5,6,7,21,24,26,37
+3V 4,5,6,7,9,11,12,20,21,22,23,24,25,26,27,28,29,30,32,33,34,37,41

Vset1	474mV
Delta Vset1	348mV
Vtsen	1074mV
Vtsen_NB	274mV

C-[1/2] SDLE modify
PR264: 10.2K->9.09K
PR259: 13K->10.5K
PC221,PC240: 150p->220p

Quanta Computer Inc.	
PROJECT : ZAUR	
Size	Document Number: VCORE (RT3662AMGQW) Rev 1A
Date: Tuesday, March 17, 2020	Sheet 35 of 44



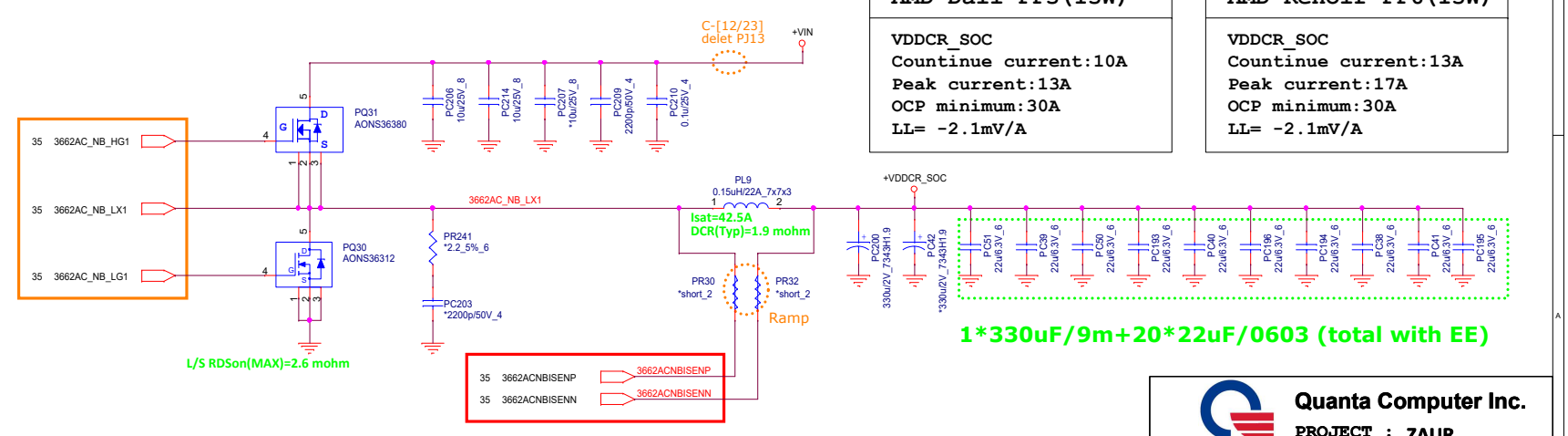
AMD Dali FP5(15W)

VDDCR_VDD
Countinue current:35A
Peak current:45A
OCP minimum:80A
LL= -0.7mV/A

AMD Renoir FP6(15W)

VDDCR_VDD
Countinue current:33A
Peak current:50A
OCP minimum:80A
LL= -0.7mV/A

C-[1/2] SDLE change to stuff:
PC38,PC39,PC40,PC41,PC50,PC51,PC52,PC54,PC59,
PC63,PC64,PC70,PC193,PC194,PC195,PC196



AMD Dali FP5(15W)

VDDCR_SOC
Countinue current:10A
Peak current:13A
OCP minimum:30A
LL= -2.1mV/A

AMD Renoir FP6(15W)

VDDCR_SOC
Countinue current:13A
Peak current:17A
OCP minimum:30A
LL= -2.1mV/A

Quanta Computer Inc.
PROJECT : ZAUR

Size	Document Number	Rev
	VCORE (RT3662ACGQW)	1A
Date: Tuesday, March 17, 2020	Sheet 36 of 44	

+3V_S5 5,6,7,11,20,21,23,25,27,28,29,32,38
+1.8V_S5 4,5,6,7,11,21,24,26,29
+1.8V 4,5,6,7,21,24,26,35
+1.5V 21
+1.2V 22,34

VL 32
+VIN 20,31,32,33,34,35,36,38,39,40,41
+3V 4,5,6,7,9,11,12,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,41
+5V 20,21,22,25,27,32
VDDP 4,7,33

+1.8V_S5
1.8 Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 160mil

Double Check PU high with HW

PR96 100K_1%_2
PR94 *short_2
PJ8 *short3720
PC105 0.01u/50V_4
PC104 10u/6.3V_4
PC125 *2200p/50V_6
PR98 *2.2_5%_6
PU7 JW5213DFND_TRPBF
PC120 *0.1u/6.3V_2
PL4 1uH/3.35A_2.5x2.0x1.2
PR99 *Short_0201
PC124 *22p/50V_4
R1 PR100 20K_1%_2
R2 PR101 10K_1%_4
PC122 0.1u/6.3V_2
PC110 22u/6.3V_6
PC111 22u/6.3V_6
PC123 *22u/6.3V_6
PJ7 *short3720
PR103 *short_4

29 HWPG_1.8VS5
+5VPCU
1218 HY
5213PG_1.8V
5213LX_1.8V
5213FB_1.8V_S
5213FB_1.8V
5213EN_1.8V
S5_ON 29,32,33

C-[12/25] 0402->0201

Vo=0.6*(R1+R2)/R2
=1.8V

+1.5V
1.5Volt +/- 5%
TDC : 0.08A
PEAK : 0.1A
Width : 20mil

Double Check PU high with HW

PR75 100K_1%_2
PR79 *short_2
PR102 *short_4
PC92 4.7u/6.3V_4
PR76 *short_6
PU6 JW5222RSOTB_TRPBF
PC118 0.47u/6.3V_4
PL5 2.2uH/1.67A_2.5x2.0x1.2
PR104 *Short_0201
PC109 *22p/50V_4
R1 PR82 22.6K_1%_4
R2 PR78 15K_1%_2
PC130 10u/6.3V_6
PC131 10u/6.3V_6
PC129 0.1u/16V_4

29 HWPG_1.5V
MAINON
JW5222LX1.5V
C-[12/23] delet PJ9

C-[12/25] 0402->0201

Vo=(0.6(R1+R2)/R2)
=1.504V

Thermal Protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85.27'C

VL
PR326 150_5%_4
PC270 0.1u/16V_4
0317 changed to 25.5K
PR311 25.5K_1%_4
PU12 TMP708AIDBVR
PR310 *short_2
SYS_SHDN# 11,29,32

Rset(Kohm)=0.0012T*T-0.9308T+96.147
=25.503 K ohm

HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

MAIND PQ8 AOSS32334C

TDC : 1.88A
PEAK : 2.5A
Width : 100mil

PQ21 DDTC144EUA-7-F
MAINON_ON_G
29,32,34 MAINON
PR205 *100K_1%_6
PR210 1M_5%_6
PR212 1M_5%_6
PR219 22_5%_8
PR204 *220_5%_8
PR213 22_5%_8
PR226 22_5%_8
PR58 22_5%_8
PR211 1M_5%_6
PQ23 2N7002K
PQ19 *2N7002K
PQ20 2N7002K
PQ25 2N7002K
PQ6 2N7002K
PQ24 2N7002K
PC184 *2200p/50V_4
MAIND 33,34

Quanta Computer Inc.
PROJECT : ZAUR

Size	Document Number	Rev
	+1.8V_S5/+1.5V/Thermal	1A
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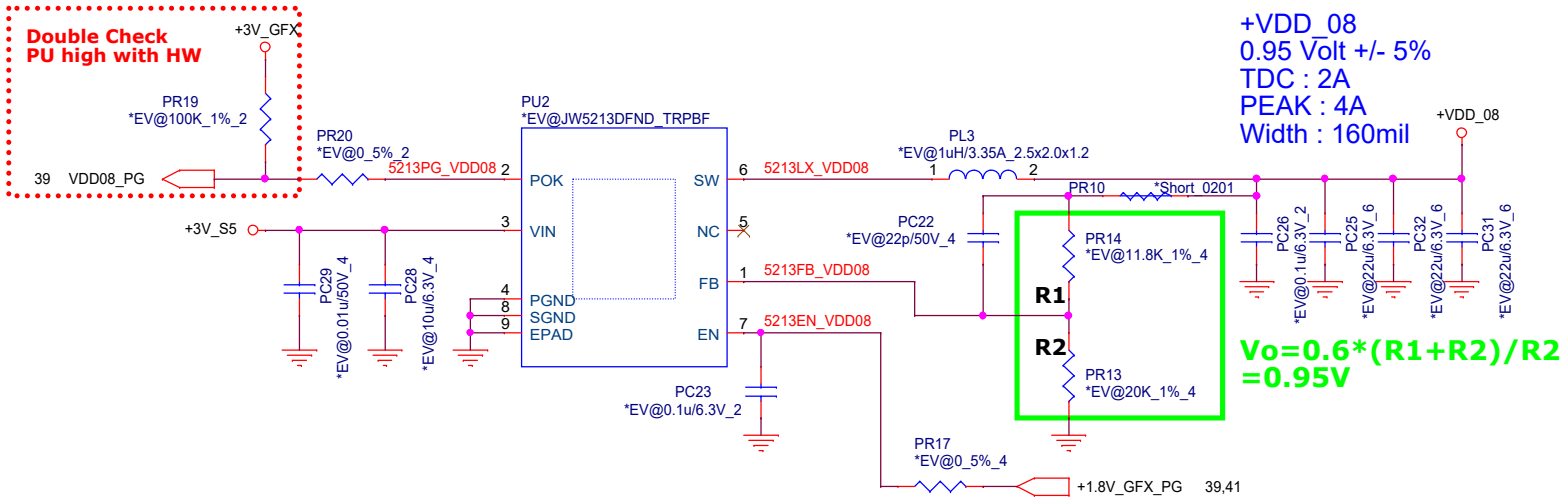
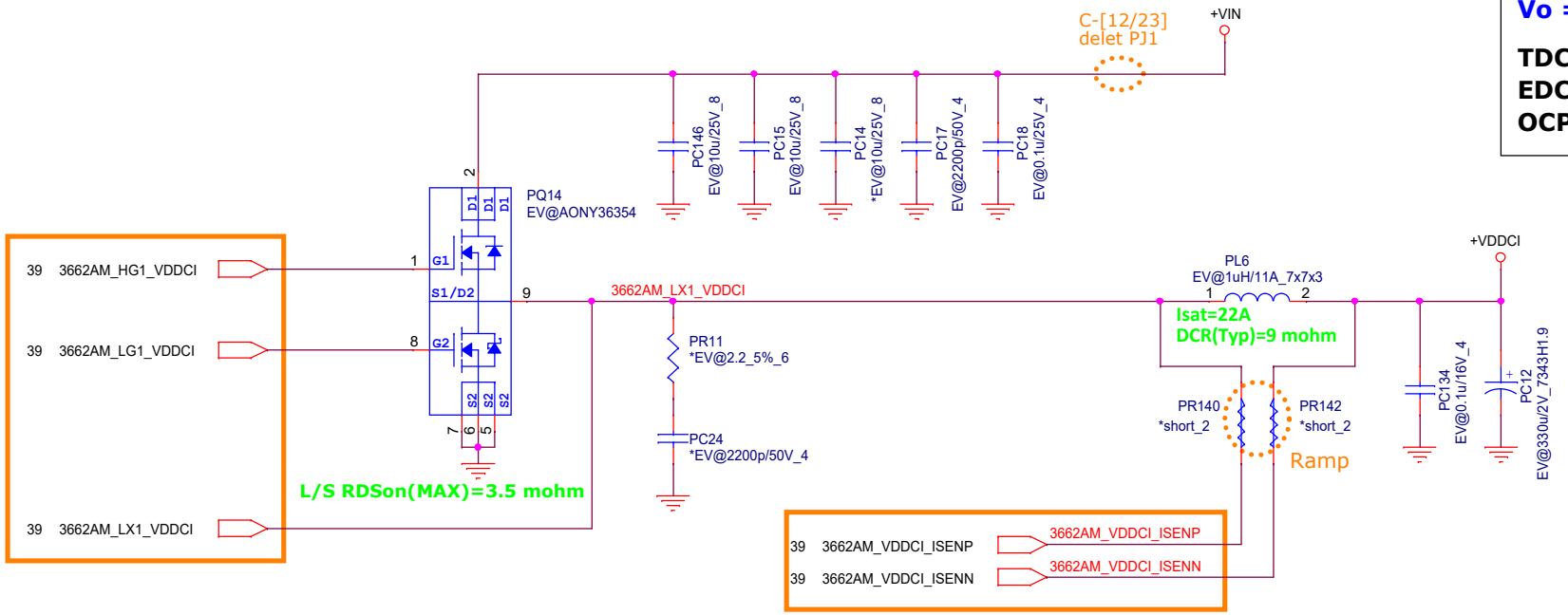
Design Reserved





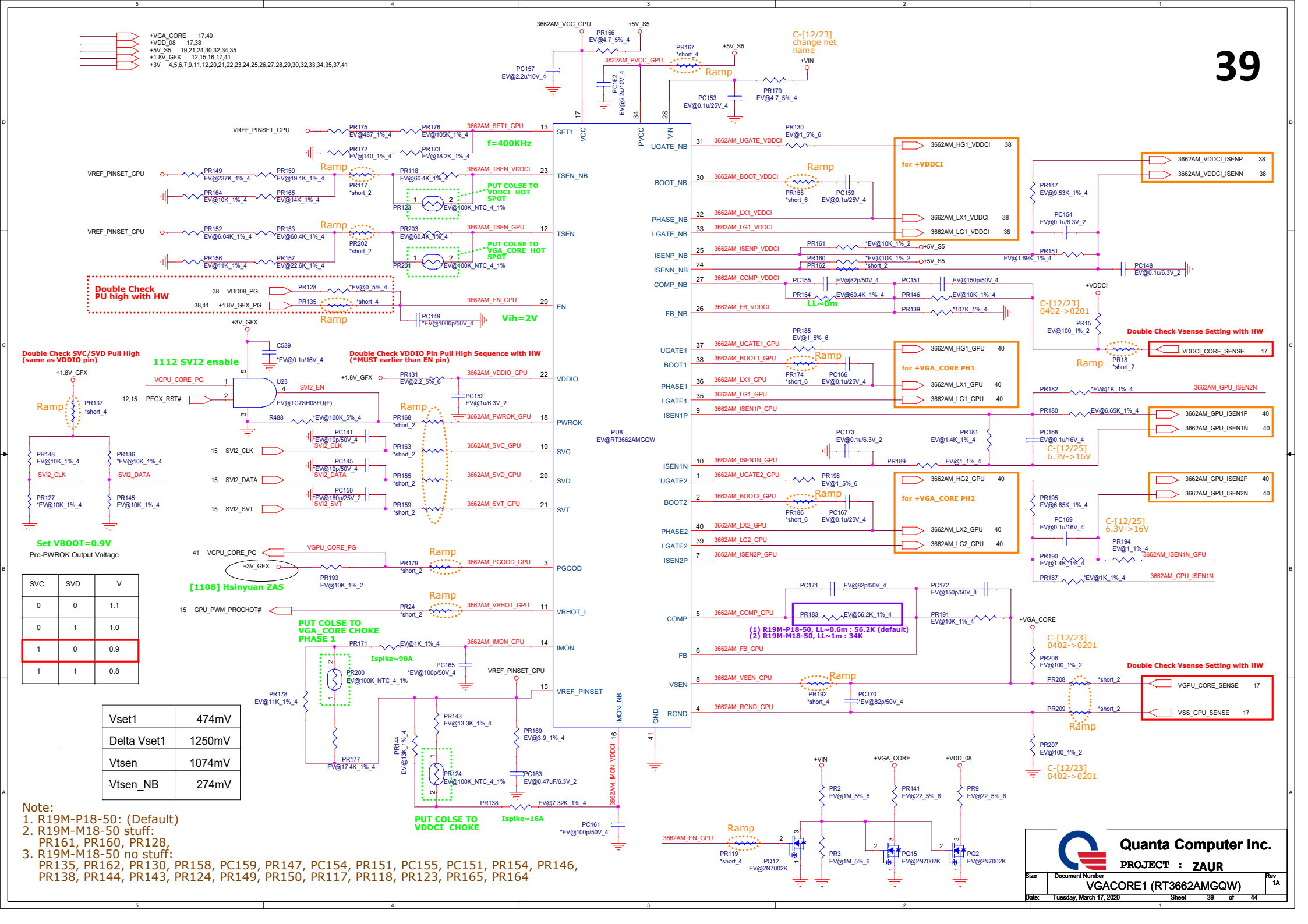
+VDDCI (R19M-P18-50) _18W
VDDCI + VDD_08 (merged)
Vo = 0.875V (Fix)
TDC : 8A EDC : 12A OCP : 16A

+VDDCI (R19M-M18-50)_18W
VDD_08
Vo = 0.95V (Fix)
TDC : 2A EDC : 3A OCP : 16A

Note:
1. R19M-P18-50: (Default)
2. R19M-M18-50 stuff:
   PR19, PR20, PC29, PC28, PU2, PL3, PR14, PR13, PR17, PC26, PC25, PC32
3. R19M-M18-50 no stuff:
   PJ1, PC18, PC17, PC15, PC146, PQ14, PL6, PR140, PR142, PC134, PC12

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	VDDCI&VDD_08	1A
Date: Tuesday, March 17, 2020	Sheet 38 of 44	



SVC	SVD	V
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vset1	474mV
Delta Vset1	1250mV
Vtsen	1074mV
Vtsen_NB	274mV

Note:
1. R19M-P18-50: (Default)
2. R19M-M18-50 stuff:
   PR161, PR160, PR128,
3. R19M-M18-50 no stuff:
   PR135, PR162, PR130, PR158, PC159, PR147, PC154, PR151, PC155, PC151, PR154, PR146, PR138, PR144, PR143, PR124, PR149, PR150, PR117, PR118, PR123, PR165, PR164

Quanta Computer Inc.
PROJECT : ZAUR

Size	Document Number	Rev
	VGACORE1 (RT3662AMGQW)	1A

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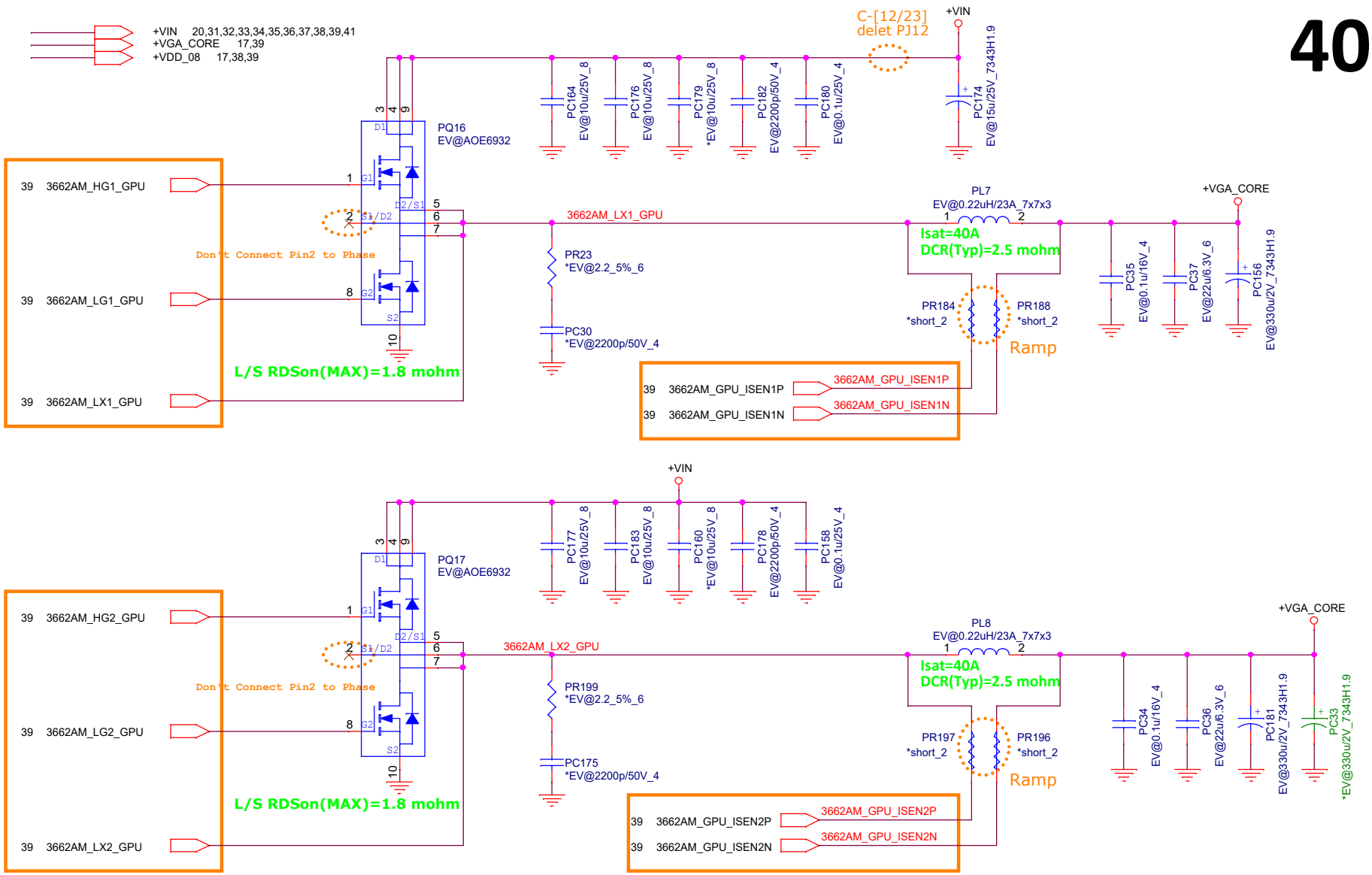


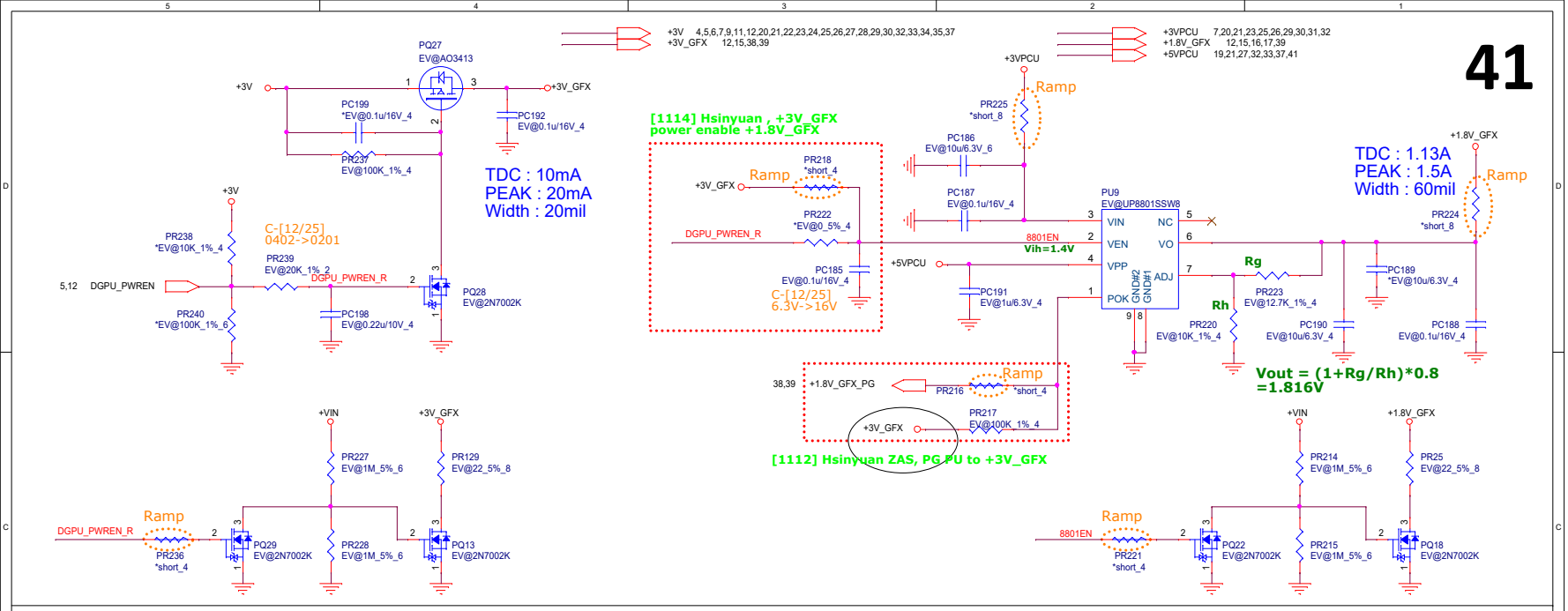
+VGA_CORE(R19M-P18-50) _18W
VDDC
TDC : 22A
EDC : 60A
OCP : 90A
LL=-0.6m

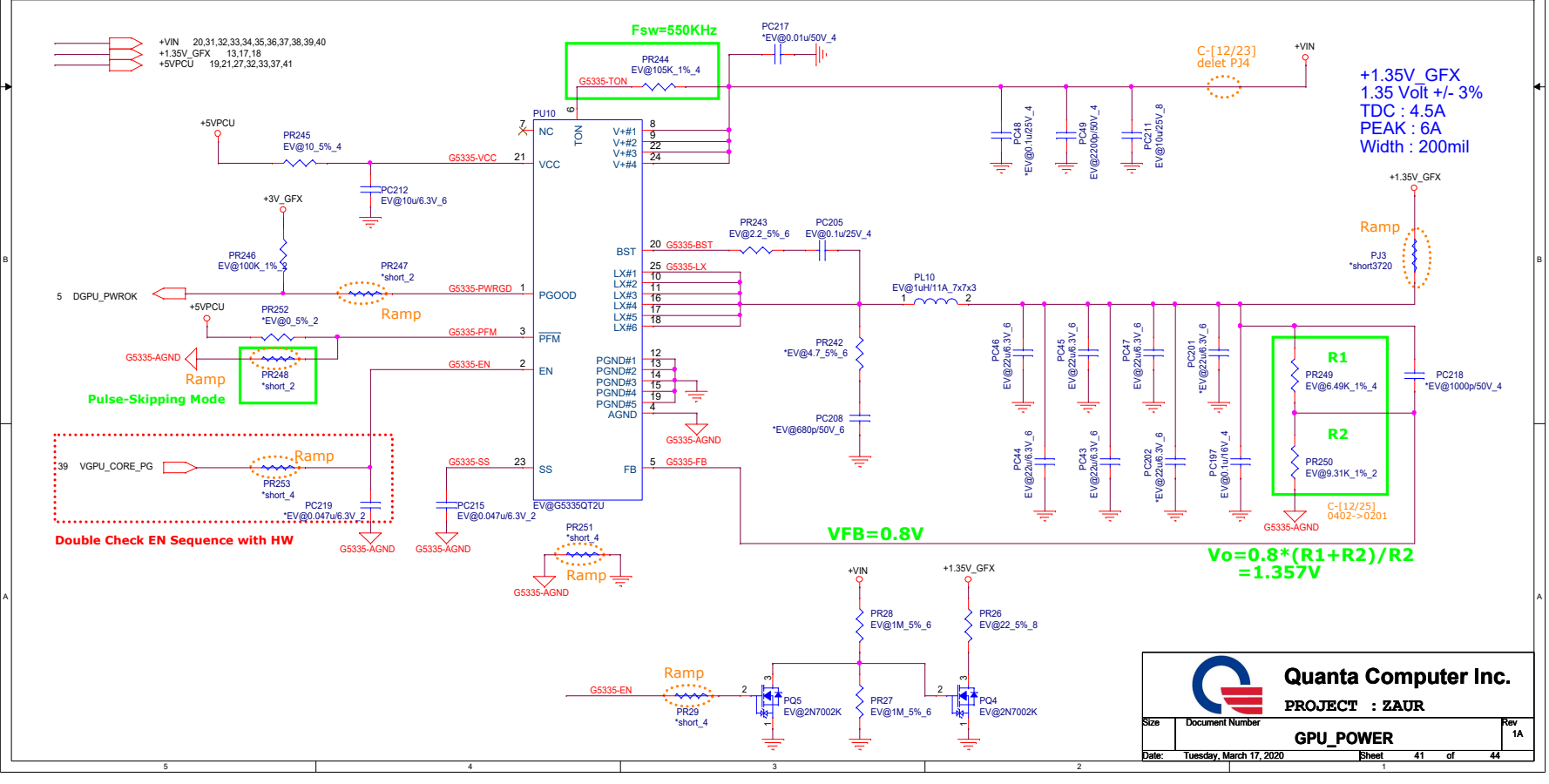
+VGA_CORE(R19M-M18-50)_18W
VDDC + VDDCI (merged)
TDC : 18A
EDC : 60A
OCP : 90A
LL=-1m

Quanta Computer Inc.

PROJECT : ZAUR

Size	Document Number	Rev
	VGACORE2 (RT3662AMGQW)	1A
Date: Tuesday, March 17, 2020	Sheet 40 of 44	





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Size	Document Number	Rev
	GPU_POWER	1A
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Hole

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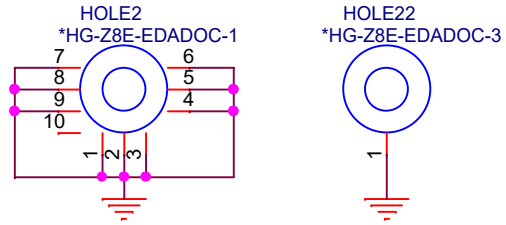
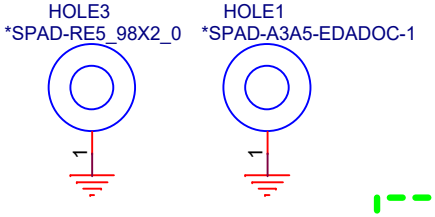
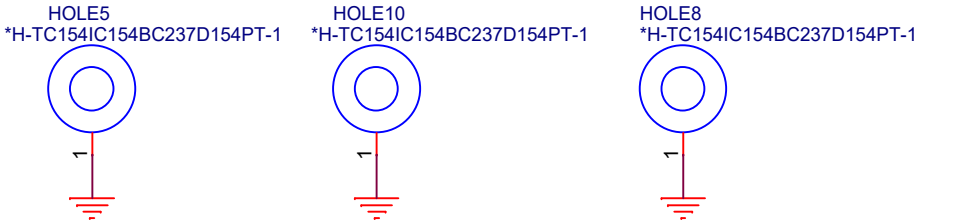
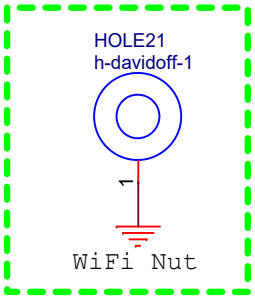
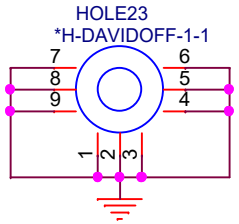
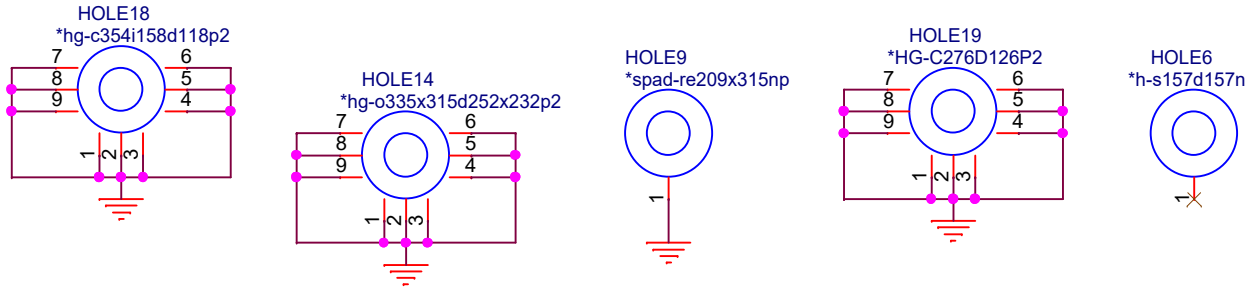


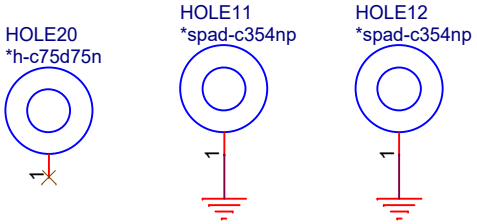


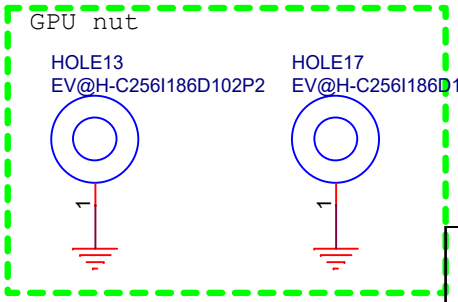


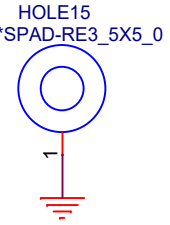


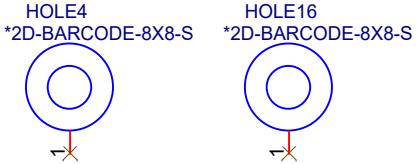








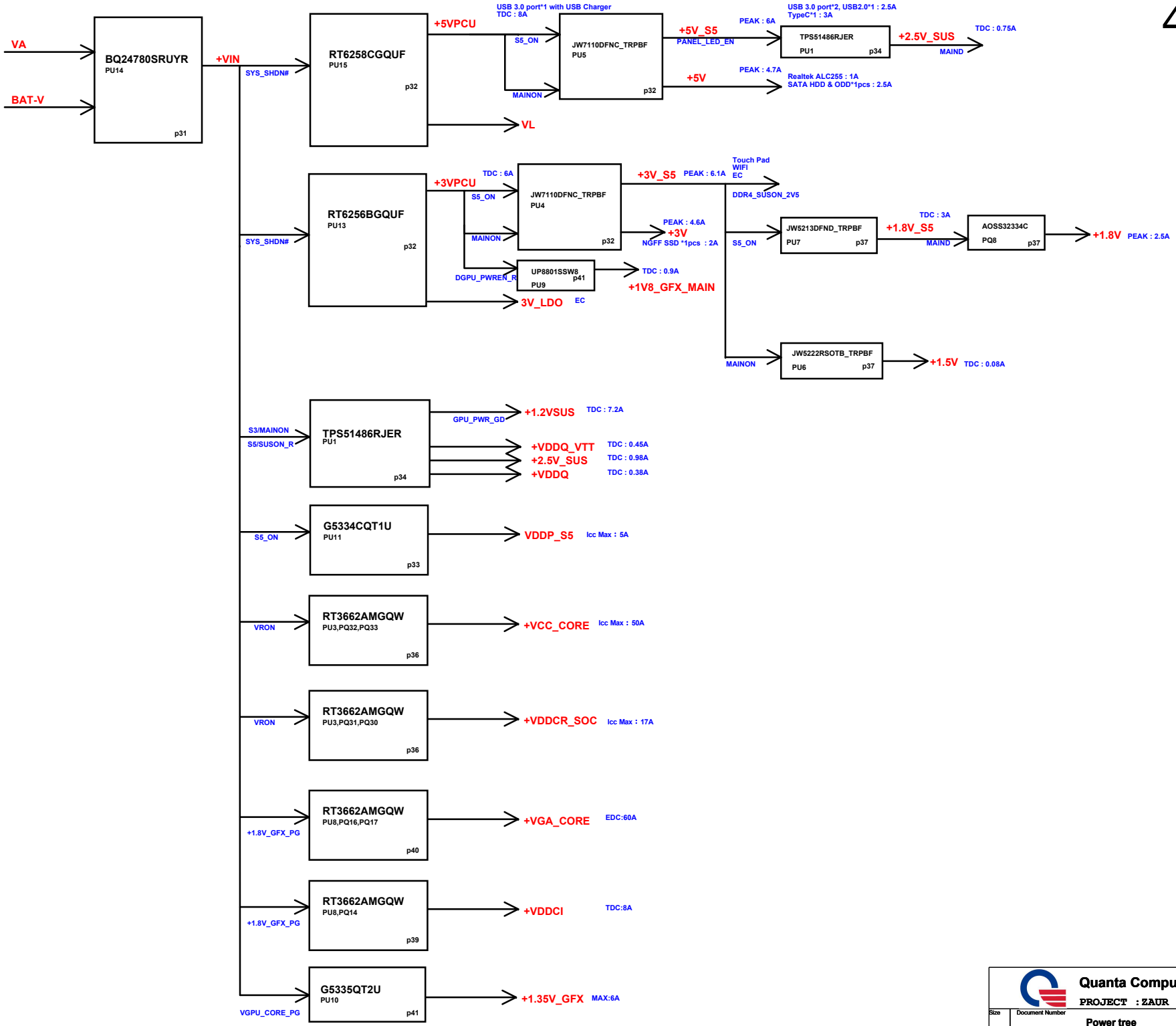




Quanta Computer Inc.

PROJECT : ZAUR

Size	Document Number	Rev
	Hole	3A
Date: Tuesday, March 17, 2020	Sheet 42 of 44	



Quanta Computer Inc.

PROJECT : ZAUR

Size	Document Number	Rev
	Power tree	1A

Date: Tuesday, March 17, 2020 Sheet 43 of 44

Stage	Date	CHANGE LIST
A	20191125	1. first released
C	20191217	adjust RAMID by AMD suggestion
		removed hole7
		Stuff R103 make a deault low on PEGX_RST#
		Stuff R569 4.7k and R568 4.7k for HDMI2 Eye test pass
		add SDP/DDP bom option
		APU_THERMTRIP# connect to EC new GPIO GPG0 as default, DNS SYS_SHDN# path
		change +1.8V_S5 source to +5VPCU & change +3V_S5 enable to 2ND_S5_ON for Rom sharing
		change U32 to G781-1P8 with slave address 9AH AL000781039
		reserved CCD/DMIC, TSI power gate
		change USB2 ESD protection to BC5V0F1BZ02 *2
		add +VREF_CA1 for MD
	20190317	most 0ohm modified to short pad
		R607/R608 changed to 47 ohm
		PR311 changed to 25.5K
MP		