MS-7276 uATX Version: 10

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe family processors in LGA775 Package.

System Chipset:

Intel BroadwaterG965/Q965 (North Bridge)
Intel ICH8DO / DH (South Bridge)

On Board Device:

BIOS -- SPI Flash 8M
Azalia Codec -- ALC883
LPC Super I/O -- W83627DHG
LAN -- NINEVEH/EKRON
CLOCK Gen -- ICS 9LPR502 (56pin)
1394 Controller -- VT6307 (2-port)
Hi-USB to PATA Bridge -- JM20335

Main Memory:

Dual-channel DDR-II * 4 (Max 4GB)

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

Intersil PWM:

Controller: Intersil ISL6312 (4 Phases)
Driver: Intersil ISL6612

Option	Function	Orcad Configure	BOM
STD	Broadwater/ICH8/W83627DHG/ALC883/82566DM/USB to IDE	cfg-STD	601-7276-A10
OPT:B	Broadwater/ICH8/W83627DHG/ALC883/82562V/USB to IDE	cfg-82562V	601-7276-A20
OPT:C	G965/ICH8DH/W83627DHG/ALC883/82566DC/JM20335	cfg-82566DC	601-7276-01S
OPT:D	Q965/ICH8DO/W83627DHG/ALC883/82566DM/JM20335	cfg-STD	601-7276-03S

MICRO-STAR INT'L CO.,LTD
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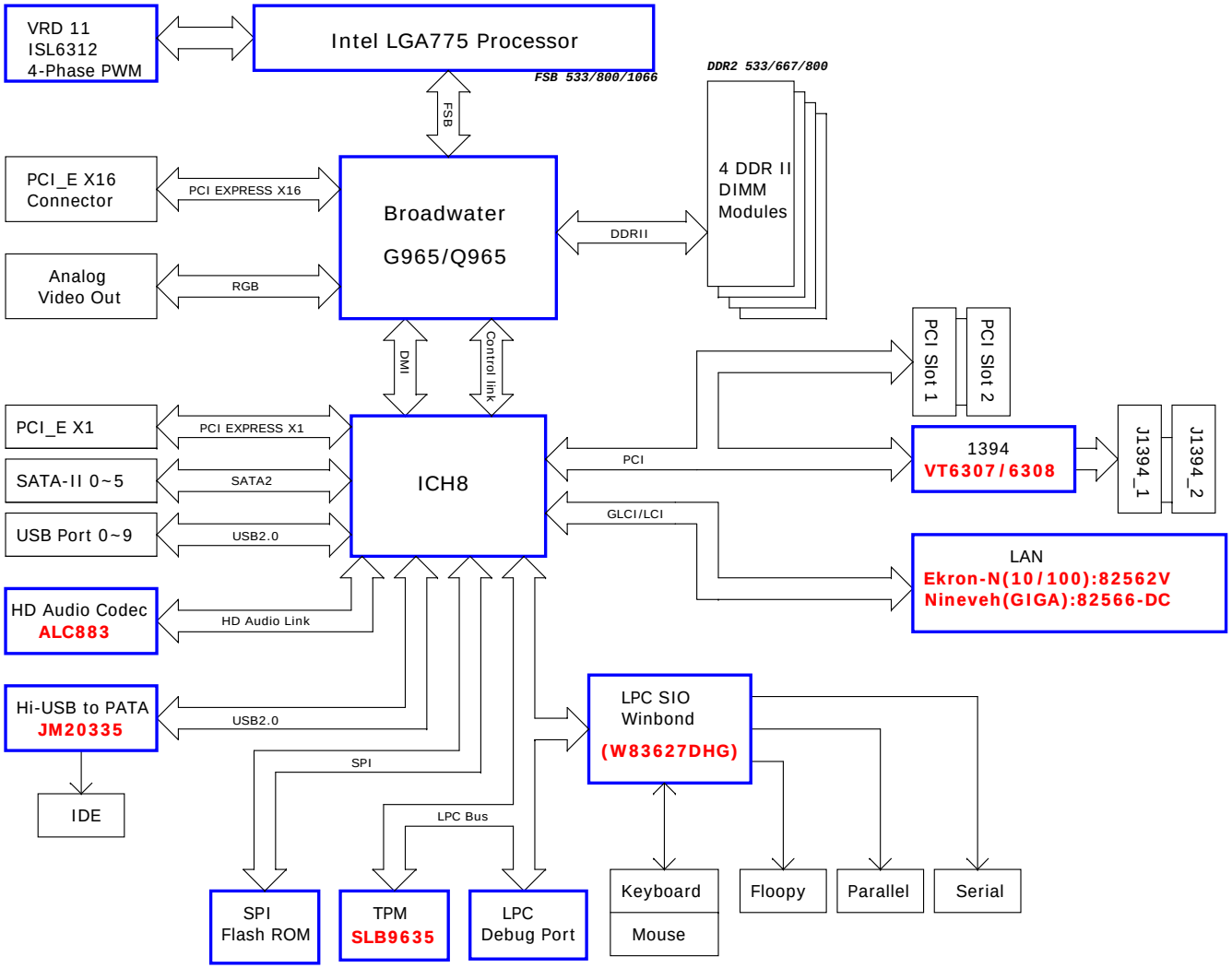
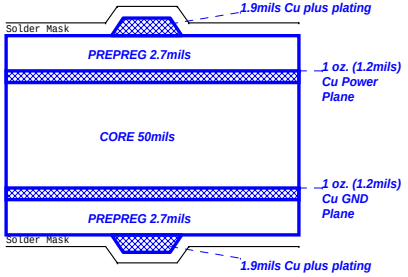
Block Diagram



Board Stack-up

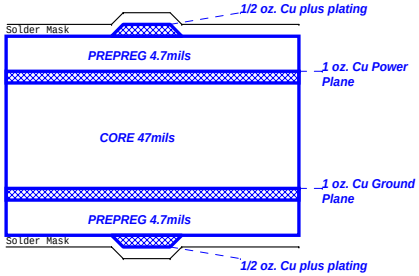
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

Board Stack-up

(2116 Prepreg Considerations)



Single End 60ohm Top/Bottom : 5mils
IEEE1394 - 110ohm Top : 5/7/5
PCIE, LAN, SATA - 100ohm Top : 5/6/5
USB2.0 - 90ohm Top : 7.5/7.5/7.5

MSI	MICRO-STAR INT'L CO.,LTD	
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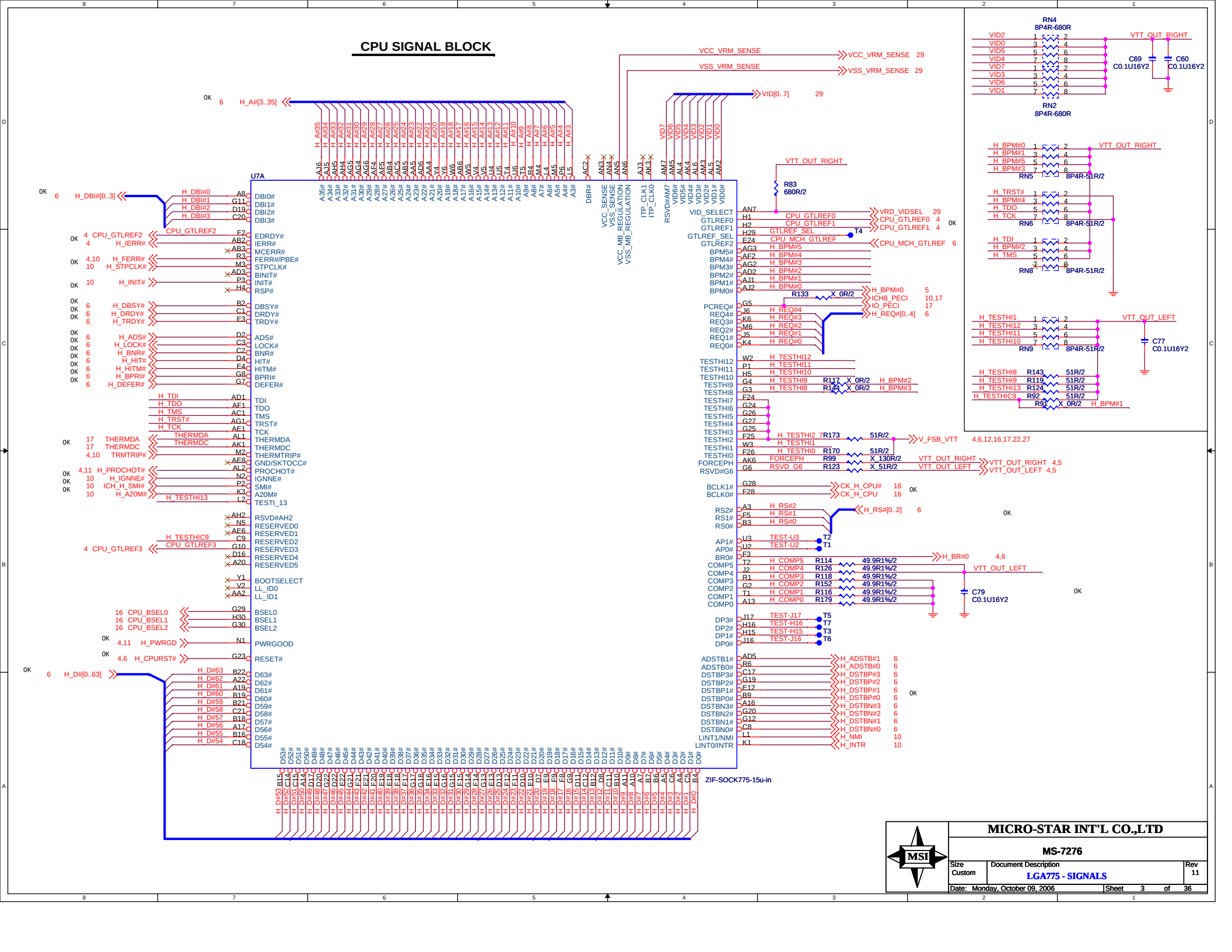
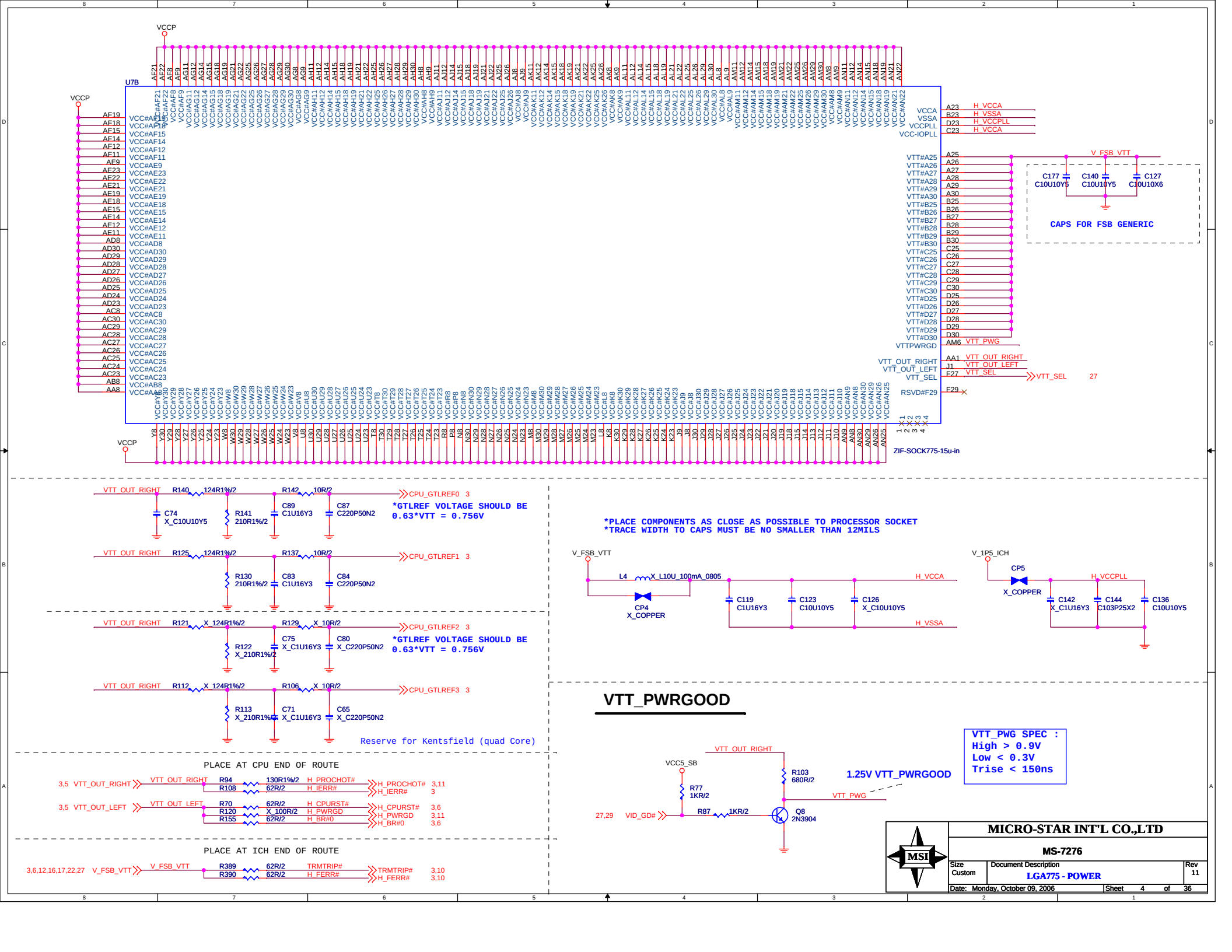
CPU SIGNAL BLOCK




U7B
VCCP
ZIF-SOCK775-15u-in
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
VTT_PWG
RSVD#F29
H_VCCA
H_VSSA
H_VCCPLL
H_VCCA
V_FSB_VTT
C177 C10U10Y5
C140 C10U10Y5
C127 C10U10X6
CAPS FOR FSB GENERIC
R140 124R1%/2
R142 10R/2
C74 X_C10U10Y5
R141 210R1%/2
C89 C1U16Y3
C87 C220P50N2
CPU_GTLREF0
*GTLREF VOLTAGE SHOULD BE 0.63*VTT = 0.756V
R125 124R1%/2
R137 10R/2
R130 210R1%/2
C83 C1U16Y3
C84 C220P50N2
CPU_GTLREF1
R121 X_124R1%/2
R129 X_10R/2
R122 X_210R1%/2
C75 X_C1U16Y3
C80 X_C220P50N2
CPU_GTLREF2
*GTLREF VOLTAGE SHOULD BE 0.63*VTT = 0.756V
R112 X_124R1%/2
R106 X_10R/2
R113 X_210R1%/2
C71 X_C1U16Y3
C65 X_C220P50N2
CPU_GTLREF3
Reserve for Kentsfield (quad Core)
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS
V_FSB_VTT
L4 X_L10U_100mA_0805
CP4 X_COPPER
C119 C1U16Y3
C123 C10U10Y5
C126 X_C10U10Y5
V_1P5_ICH
CP5 X_COPPER
C142 X_C1U16Y3
C144 C103P25X2
C136 C10U10Y5
VTT_PWRGOOD
VCC5_SB
R77 1KR/2
R87 1KR/2
R103 680R/2
Q8 2N3904
1.25V VTT_PWRGOOD
VTT_PWG
VID_GD#
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
PLACE AT CPU END OF ROUTE
R94 130R1%/2 H_PROCHOT#
R108 62R/2 H_IERR#
R70 62R/2 H_CPURST#
R120 X_100R/2 H_PWRGD
R155 62R/2 H_BR#0
PLACE AT ICH END OF ROUTE
R389 62R/2 TRMTRIP#
R390 62R/2 H_FERR#
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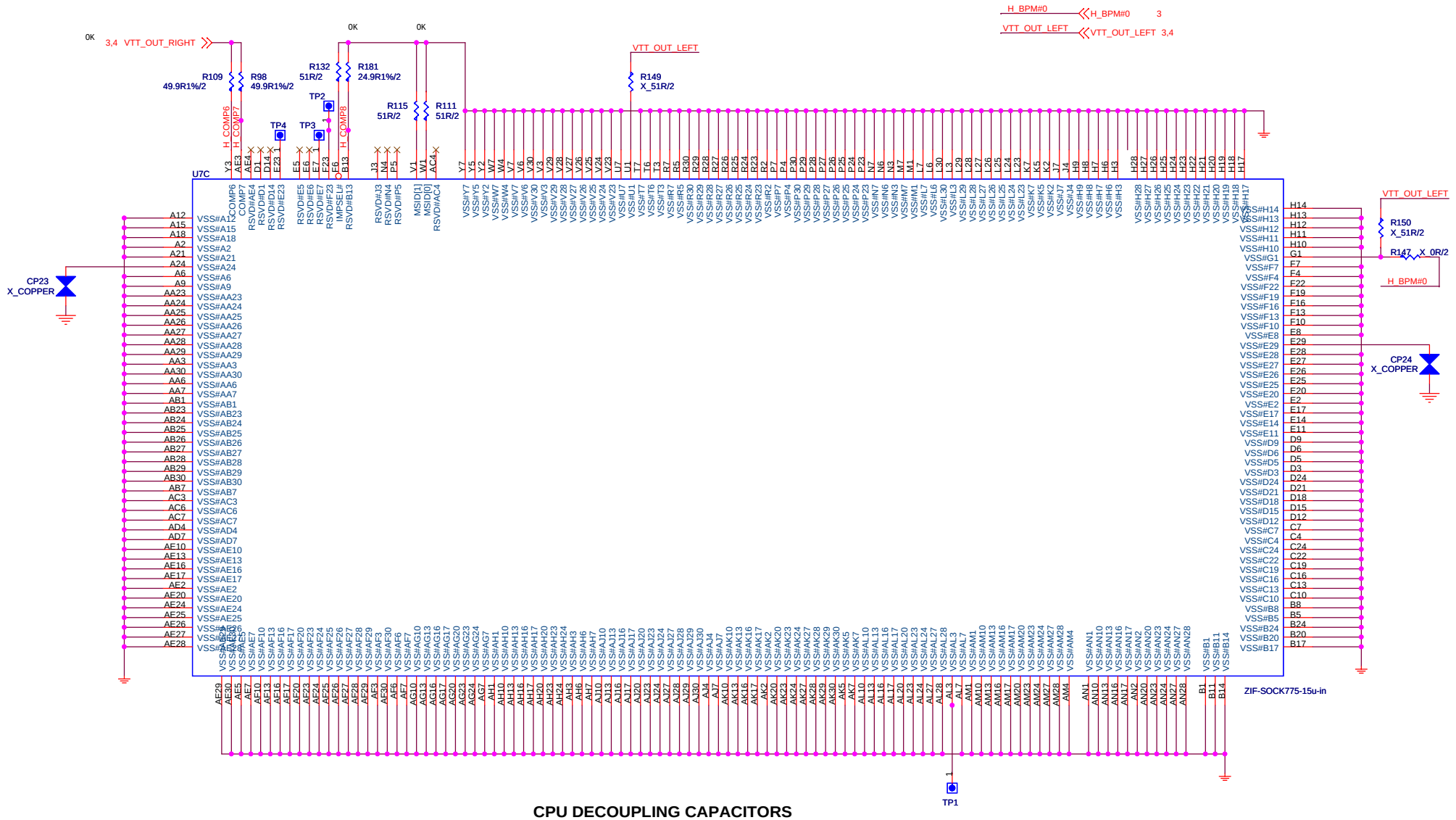
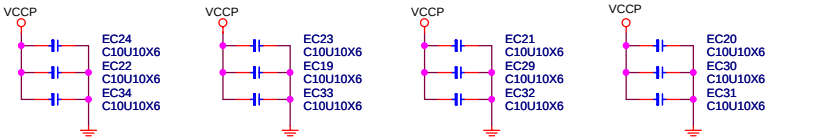


CPU DECOUPLING CAPACITORS



Place these caps within socket cavity

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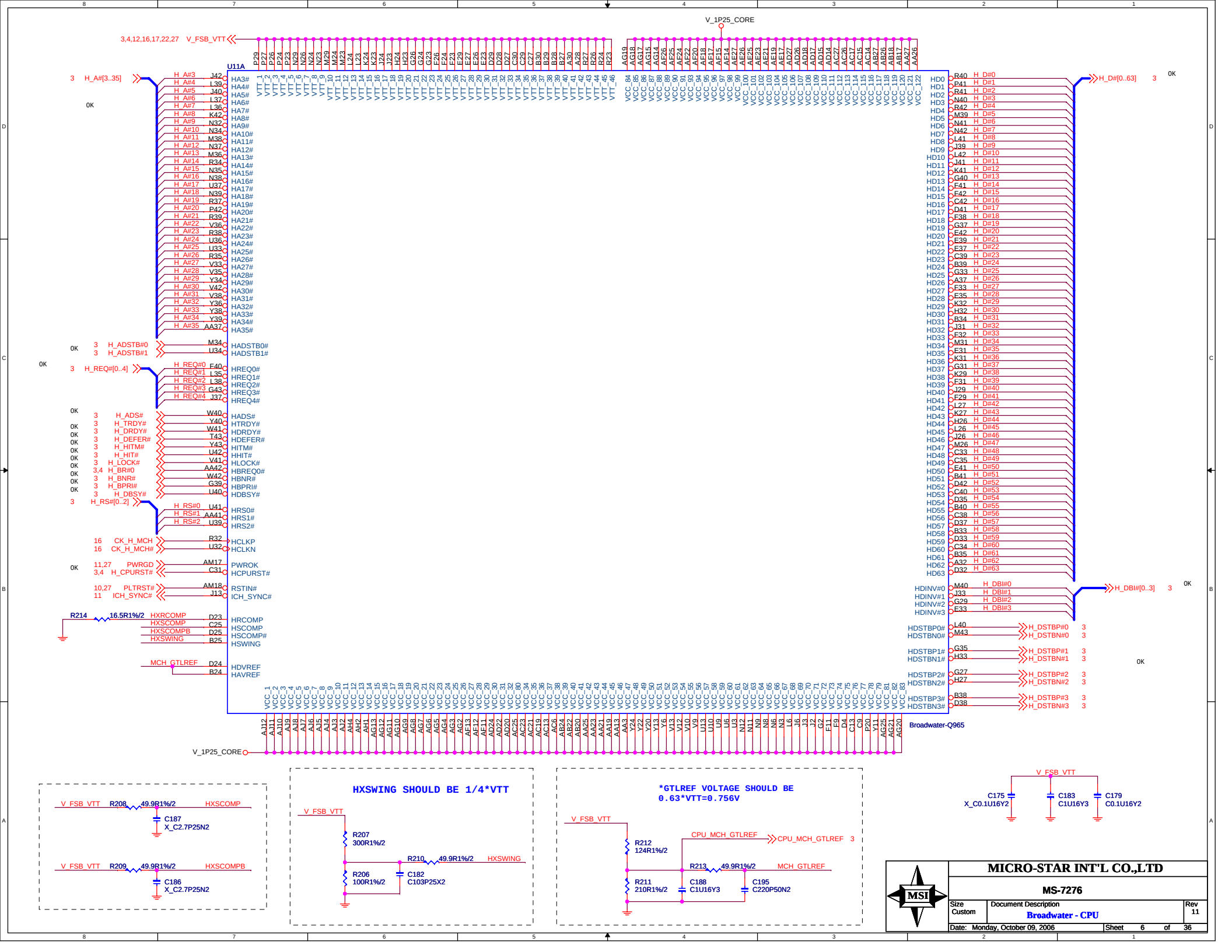
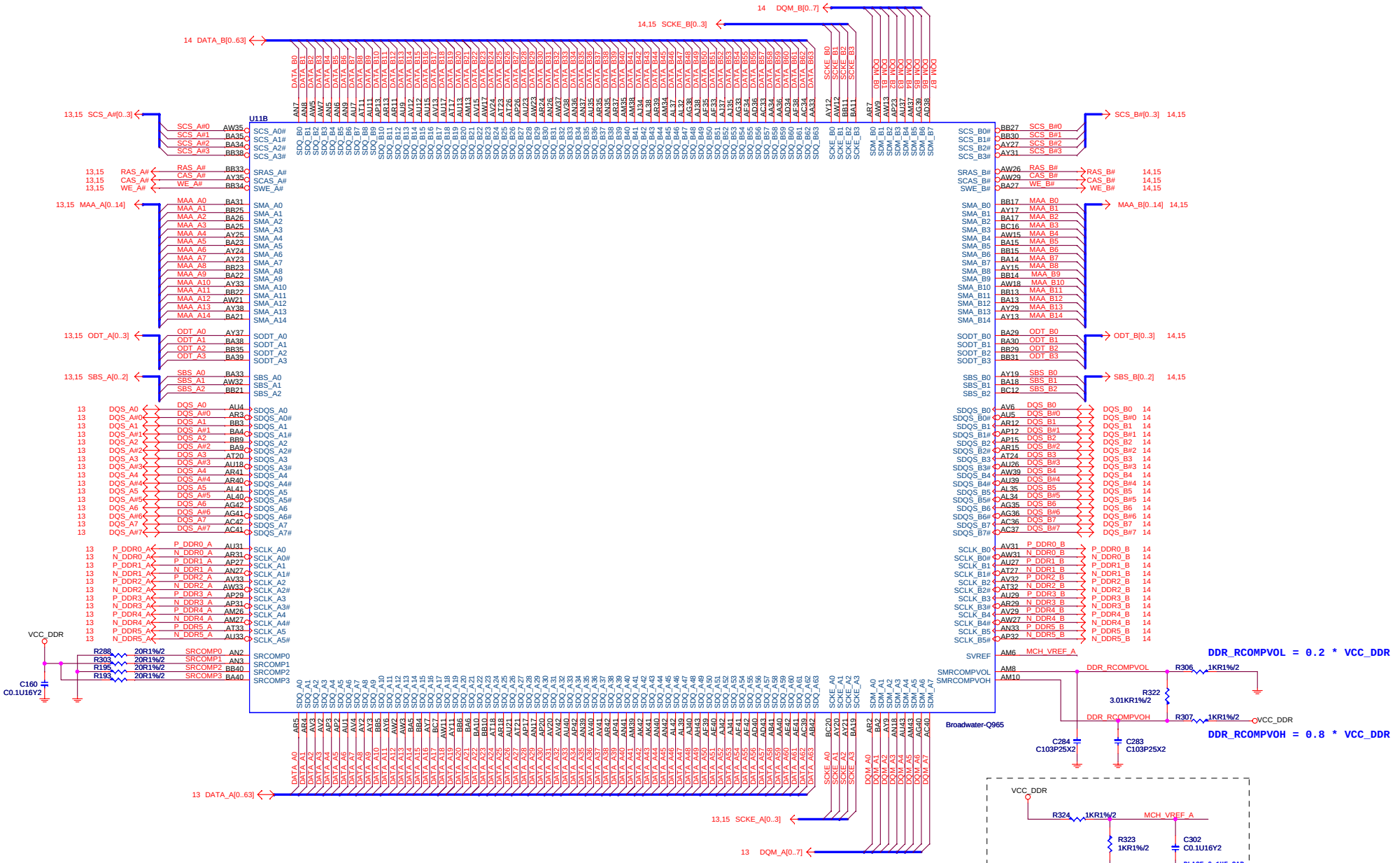

V_1P25_CORE
3,4,12,16,17,22,27 V_FSB_VTT
U11A
Broadwater-Q965
HXSWING SHOULD BE 1/4*VTT
*GTLREF VOLTAGE SHOULD BE 0.63*VTT=0.756V
MICRO-STAR INT'L CO.,LTD
MS-7276
Broadwater - CPU
Monday, October 09, 2006



MICRO-STAR INT'L CO.,LTD

MS-7276

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Custom	Broadwater - Memory	11

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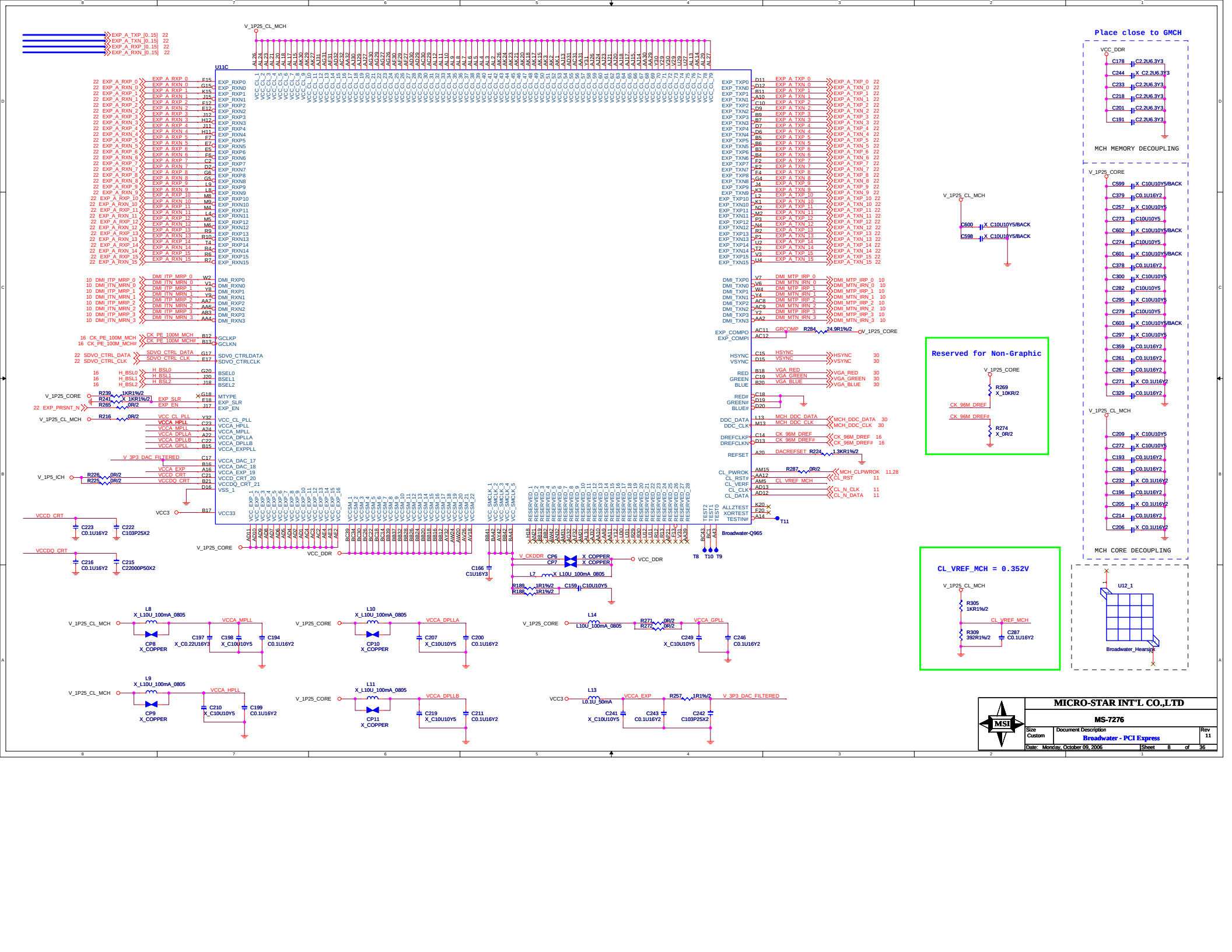
Place close to GMCH
MCH MEMORY DECOUPLING
MCH CORE DECOUPLING
Reserved for Non-Graphic
CL_VREF_MCH = 0.352V
Broadwater-Q965
Broadwater_Hearsink
MICRO-STAR INT'L CO.,LTD
MS-7276
Broadwater - PCI Express
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ICH8 H/W STRAPS

SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERIDE
INTVRMEN/ LAN100_SLP	EN	DIS	INT VRM (VccSus1_05,1_5,VccCL1_5) (VccLAN1_05,VccCL1_05)
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/ PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

PGNT#2 R464 X_1KR/2
PGNT#3 R486 X_1KR/2 VCC3_SB
11 ACSDOUT ACSDOUT R477 X_1KR/2
11 ACSYNC ACSYNC R478 X_1KR/2
11,24 SPKR R489 X_1KR/2 VCC3

RN41
VCC3 2 1 SERIRQ
4 3 A20GATE
6 5 KBRST#
8 7
8P4R-10KR/2

BOOT SELECT STRAPS

BOOT DEVICE	GNT0	SPI_CS1#	
FWH	1	1	
SPI	0	X	
PCI	1	0	

R511 1KR/2 PGNT#0
R467 X_1KR/2 SPI_CS1#

SPI DEBUG PROT
Place close to SPI ROM

VCC3_SB
JSPI1
SPI_MISO_F 3 4 SPI_MOSI_F
SPI_CS0_F# 5 6 SPI_CLK_F
SPI_HOLD# 7 8
9
H2X5(10)_black-RH

Part Number : N31-2051451-H06

U23A

ICH 8
PART 1/3

PCI INTERFACE
PCI EXPRESS
DIRECT MEDIA
LAN
INTERRUPT SPI
CPU

23,26 AD[31..0] AD0 E18 AD1 A16 AD2 A14 AD3 A17 AD4 B13 AD5 F18 AD6 E17 AD7 C17 AD8 A13 AD9 C14 AD10 E14 AD11 C13 AD12 E15 AD13 F16 AD14 A11 AD15 D10 AD16 C11 AD17 E13 AD18 E12 AD19 D13 AD20 F14 AD21 E11 AD22 D8 AD23 D7 AD24 C7 AD25 F13 AD26 B7 AD27 C6 AD28 B5 AD29 E12 AD30 F8 AD31 E7

23,26 C_BE#[3..0] C_BE#0 G16 C_BE#1 A10 C_BE#2 C12 C_BE#3 A12

23,26 DEVSEL# B12 FRAME# E16 IRDY# B6 TRDY# A7 STOP# D15 PAR D9 LOCK# D11 SERR# E6 PERR# C9 PCI_PME# D3

16 ICH_PCLK B10
23,26 PCIRST_ICH8# R505 33R/2 E3

23 PREQ#0 E8 PREQ#1 C16 PREQ#2 B16 PREQ#3 A9

23 PGNT#0 A4 PGNT#1 C15 PGNT#2 D17 PGNT#3 B9

23 PIRQ#A C4 PIRQ#B C5 PIRQ#C A3 PIRQ#D A8 PIRQ#E D5 PIRQ#F F10 PIRQ#G G11 PIRQ#H F9

17 SERIRQ SERIRQ AG9

SPI_MOSI_F R427 15R/2 SPI_MOSI D21
SPI_MISO B19
SPI_CS0_F# R434 15R/2 SPI_CS0# C21
SPI_CLK_F R466 15R/2 SPI_CLK A19
SPI_CS1# A18

RN34
V_3P3_CL 2 1 SPI_MOSI
4 3 SPI_CS0#
6 5 SPI_MISO
8 7
8P4R-10KR/2

VSS_001 A5 VSS_002 A24 VSS_003 A28 VSS_004 B2 VSS_005 B8 VSS_006 B11 VSS_007 B14 VSS_008 B17 VSS_009 B20 VSS_010 C22 VSS_011 C23 VSS_012 C24 VSS_013 D2 VSS_014 D4 VSS_015 D6 VSS_016 D12 VSS_017 D16 VSS_018 D19 VSS_019 D22 VSS_020 D25 VSS_021 D26 VSS_022 E9 VSS_023 E21 VSS_024 E24 VSS_025 E27 VSS_026 E28 VSS_027 F2 VSS_028 F7 VSS_029 F15 VSS_030 F22 VSS_031 F24 VSS_032 F25 VSS_033 F26 VSS_034 G1 VSS_035 G4 VSS_036 G6 VSS_037 G10 VSS_038 G13 VSS_039 G18 VSS_040 ICH8-DO

A20M# AD23 H_A20M# 3
CPUSLP# AC24
FERR# AB22 H_FERR# 3,4
IGNNE# AC22 H_IGNNE# 3
INIT# AB19 H_INIT# 3
INIT3_3V# AC12
INTR AH28 H_INTR 3
NMI AC23 H_NMI 3
SMI# AB20 ICH_H_SMI# 3
STPCLK# AB23 H_STPCLK# 3
RCIN# AE10 KBRST# 17
A20GATE AG10 A20GATE 17
THRMTRIP# AG28 TRMTRIP# 3,4 0K
PECI AF26 ICH8_PECI ICH8_PECI 3,17

PLTRST# AF23 PLTRST_L R423 33R/2 PLTRST# PLTRST# 6,27

PERN_1 N25 PE_RXN1
PERP_1 N26 PE_RXP1
PETN_1 M28 PE_TXN1_C C414 C0.1U16Y2 PE_TXN1 22
PETP_1 M27 PE_TXP1_C C424 C0.1U16Y2 PE_TXP1 22

PERN_2 L25
PERP_2 L26
PETN_2 K28
PETP_2 K27

PERN_3 J26
PERP_3 J25
PETN_3 H28
PETP_3 H27

PERN_4 G26
PERP_4 G25
PETN_4 E28
PETP_4 E27

PERN_5 E26
PERP_5 E25
PETN_5 D28
PETP_5 D27

Stuff for NINEVEH
Empty for EKRON

PERN_6/GLAN_RXN C26 GLAN_RXN
PERP_6/GLAN_RXP C25 GLAN_RXP
PETN_6/GLAN_TXN B28 GLAN_TXN_C C412 C0.1U16Y2 GLAN_TXN 20
PETP_6/GLAN_TXP B27 GLAN_TXP_C C404 C0.1U16Y2 GLAN_TXP 20

DMI_0RXN U26 DMI_0RXP U25 DMI_0TXN T28 DMI_0TXP T27
DMI_MTN_IRN_0 8 DMI_MTP_IRP_0 8 DMI_ITN_MRN_0 8 DMI_ITP_MRP_0 8

DMI_1RXN W26 DMI_1RXP W25 DMI_1TXN V28 DMI_1TXP V27
DMI_MTN_IRN_1 8 DMI_MTP_IRP_1 8 DMI_ITN_MRN_1 8 DMI_ITP_MRP_1 8

DMI_2RXN AA25 DMI_2RXP AA24 DMI_2TXN Y28 DMI_2TXP Y27
DMI_MTN_IRN_2 8 DMI_MTP_IRP_2 8 DMI_ITN_MRN_2 8 DMI_ITP_MRP_2 8

DMI_3RXN AC26 DMI_3RXP AC25 DMI_3TXN AB28 DMI_3TXP AB27
DMI_MTN_IRN_3 8 DMI_MTP_IRP_3 8 DMI_ITN_MRN_3 8 DMI_ITP_MRP_3 8

DMI_CLKN R25 DMI_CLKP R24
CK_PE_100M_ICH# 16 CK_PE_100M_ICH 16
V_1P5_ICH

DMICOMPI AD27 DMI_BIAS R388 24.9R1%/2
DMI_IRCOMPO AD28 <200mils

GLAN_CLK E22 ELAN_CLK ELAN_CLK 20
LAN_RSTSYNC E20 ELAN_SYNC ELAN_SYNC 20
LAN_RST# AF17 LAN_PWROK
LAN_RXD0 E19 ELAN_RXD0 ELAN_RXD0 20
LAN_RXD1 C19 ELAN_RXD1 ELAN_RXD1 20
LAN_RXD2 D20 ELAN_RXD2 ELAN_RXD2 20

LAN_TXD0 C20 ELAN_TXD0 ELAN_TXD0 20
LAN_TXD1 C18 ELAN_TXD1 ELAN_TXD1 20
LAN_TXD2 D18 ELAN_TXD2 ELAN_TXD2 20

LAN_PWROK R471 10KR/2 V_3P3_CL
R470 X_0R/2 RSMRST# RSMRST# 11,27
C478 C1U16Y3

SPI FLASH ROM
Place close to SB.

V_3P3_CL
C426 C0.1U16Y2
R384 2.2KR/2
U17
SPI_MISO R357 15R/2 SPI_CS0_F# 1 CE# VDD 8
SPI_MISO_F 2 SO HOLD# 7 SPI_HOLD#
11 SPI_WP# SPI_WP# 3 WP# SCK 6 SPI_CLK_F
From South-Bridge GPIO32 4 VSS SI 5 SPI_MOSI_F
V_3P3_CL R356 2.2KR/2
MX25L1605AM2C-15G
R375 X_0R/2
SPI_HOLD_GPO# 11
From South-Bridge GPIO33
Reserved for BIOS control used

MICRO-STAR INT'L CO.,LTD
MS-7276
Size: Custom
Document Description: ICH8 - PCI, DMI, CPU, SPI
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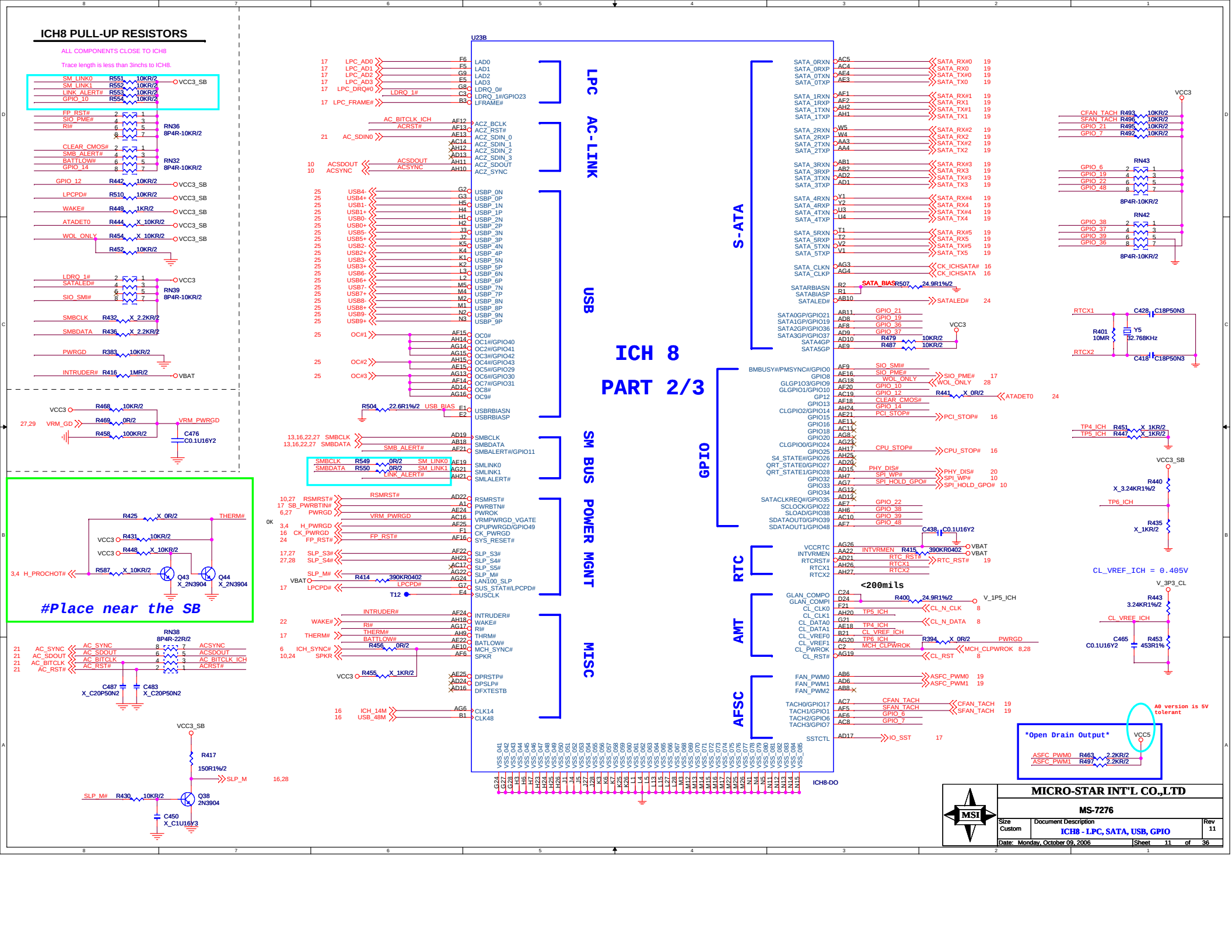
ICH8 PULL-UP RESISTORS
ALL COMPONENTS CLOSE TO ICH8
Trace length is less than 3inchs to ICH8.
#Place near the SB
ICH 8
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
S-ATA
GPIO
RTC
AMT
AFSC
ICH8-DO
<200mils
CL_VREF_ICH = 0.405V
Open Drain Output
A0 version is 5V tolerant
MICRO-STAR INT'L CO.,LTD
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ICH8 - LPC, SATA, USB, GPIO
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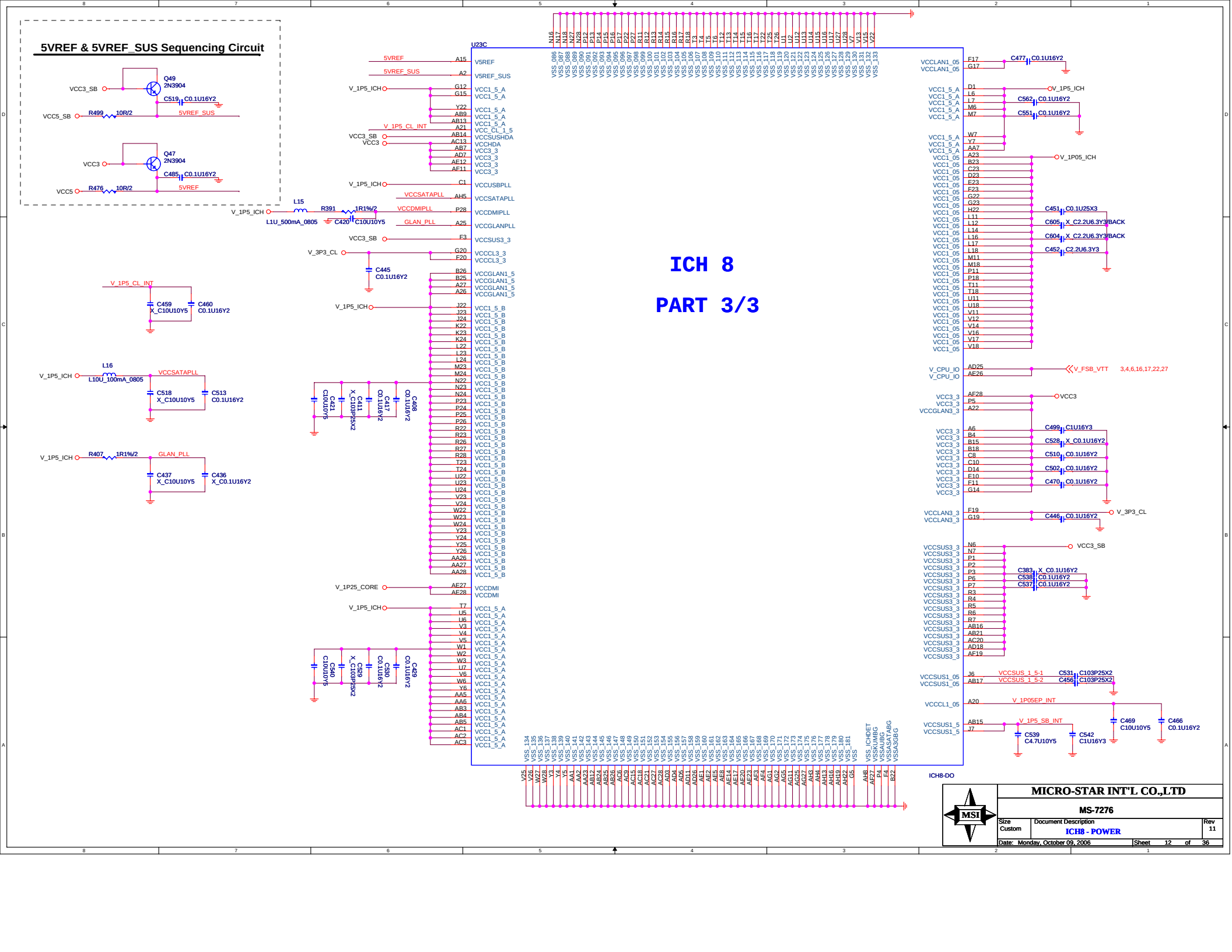
5VREF & 5VREF_SUS Sequencing Circuit
Q49
2N3904
VCC3_SB
C519
C0.1U16Y2
VCC5_SB
R499
10R/2
5VREF_SUS
Q47
2N3904
VCC3
C485
C0.1U16Y2
VCC5
R476
10R/2
5VREF
U23C
ICH 8
PART 3/3
5VREF
5VREF_SUS
V_1P5_ICH
V_1P5_CL_INT
VCC3_SB
VCC3
L15
R391
1R1%/2
C420
C10U10Y5
L1U_500mA_0805
VCCDMIPLL
GLAN_PLL
VCCSATAPLL
C445
C0.1U16Y2
C459
X_C10U10Y5
C460
C0.1U16Y2
L16
L10U_100mA_0805
C518
X_C10U10Y5
C513
C0.1U16Y2
R407
1R1%/2
C437
X_C10U10Y5
C436
X_C0.1U16Y2
V_1P25_CORE
C421
C10U10Y5
C411
X_C103P25X2
C417
C0.1U16Y2
C408
C0.1U16Y2
C540
C10U10Y5
C529
X_C103P25X2
C530
C0.1U16Y2
C429
C0.1U16Y2
C477
C0.1U16Y2
C562
C0.1U16Y2
C551
C0.1U16Y2
V_1P05_ICH
C451
C0.1U25X3
C605
X_C2.2U6.3Y3/BACK
C604
X_C2.2U6.3Y3/BACK
C452
C2.2U6.3Y3
V_CPU_IO
V_FSB_VTT
3,4,6,16,17,22,27
VCC3
C499
C1U16Y3
C528
X_C0.1U16Y2
C510
C0.1U16Y2
C502
C0.1U16Y2
C470
C0.1U16Y2
V_3P3_CL
C446
C0.1U16Y2
VCC3_SB
C383
X_C0.1U16Y2
C536
C0.1U16Y2
C537
C0.1U16Y2
VCCSUS_1_5-1
VCCSUS_1_5-2
C531
C103P25X2
C456
C103P25X2
V_1P05EP_INT
V_1P5_SB_INT
C539
C4.7U10Y5
C542
C1U16Y3
C469
C10U10Y5
C466
C0.1U16Y2
ICH8-DO
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MS-7276
Size
Custom
Document Description
ICH8 - POWER
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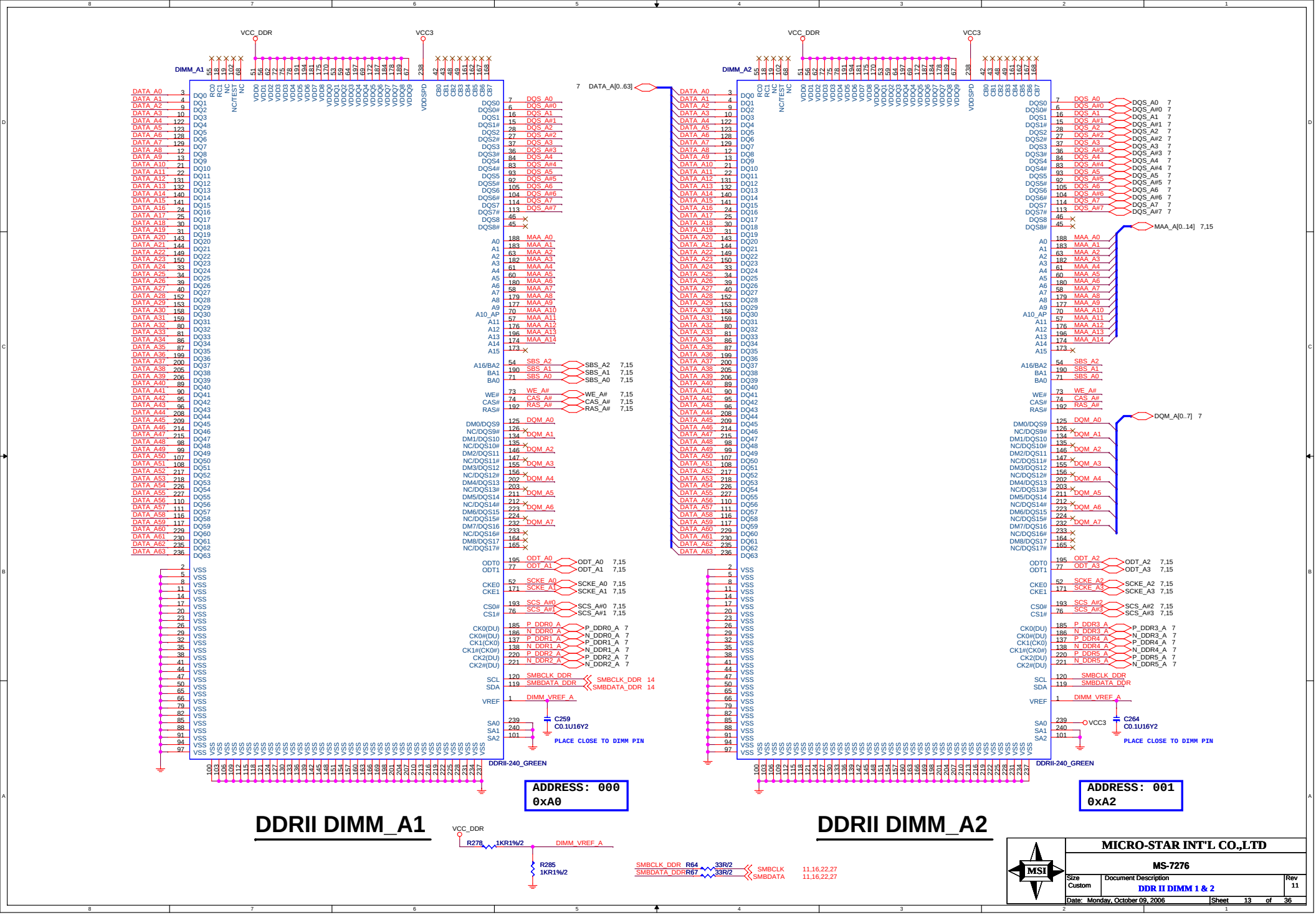

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR II DIMM 1 & 2
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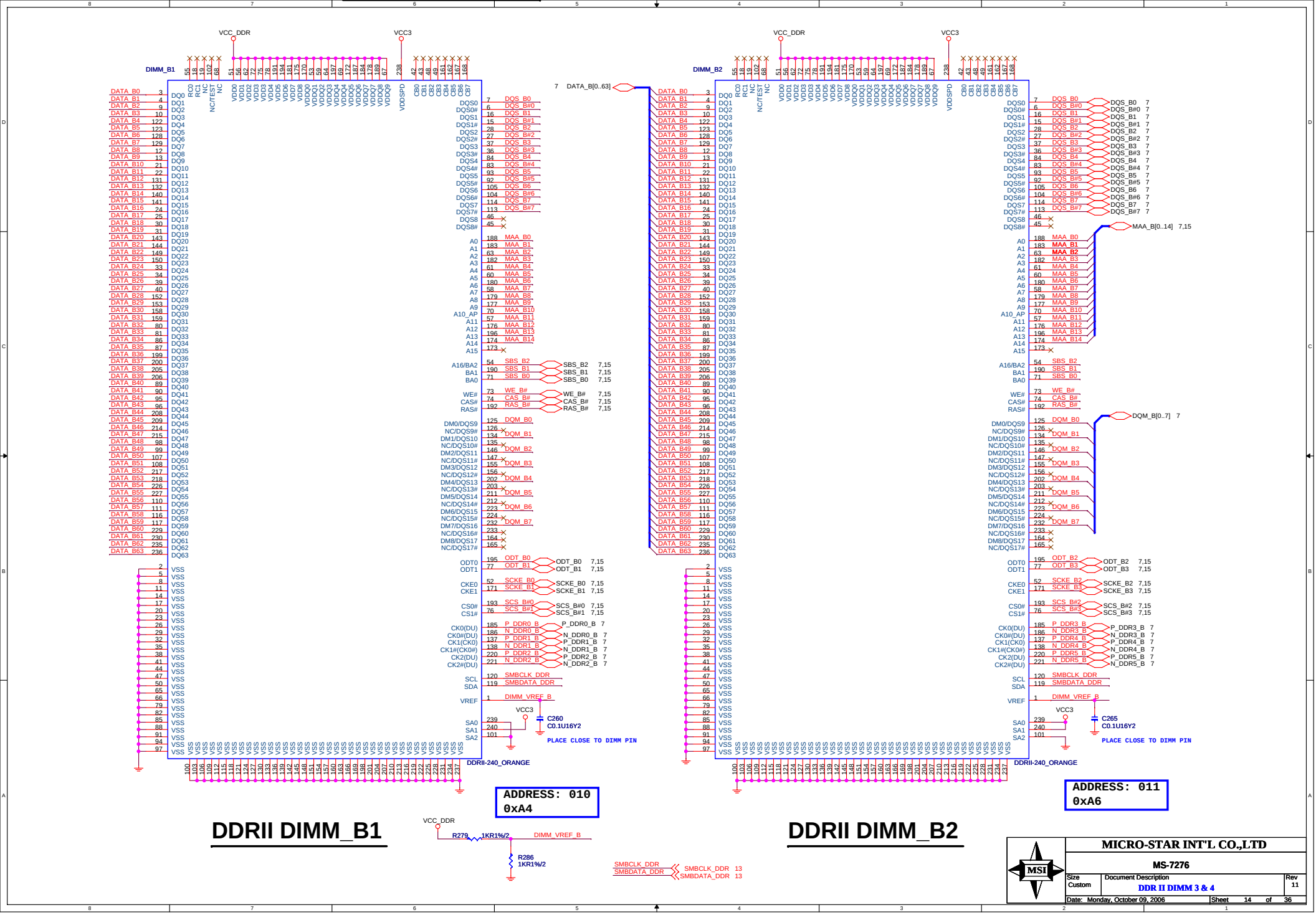

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Size: Custom	Document Description: DDR II DIMM 3 & 4
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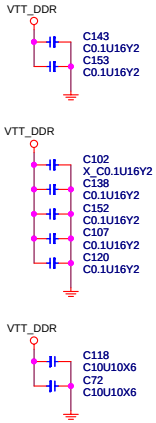
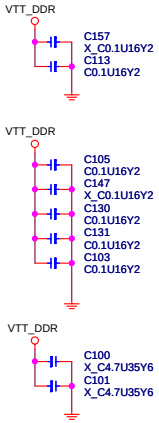
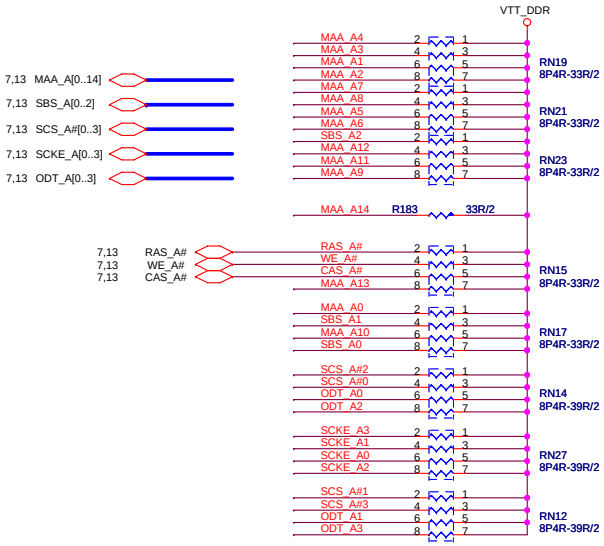
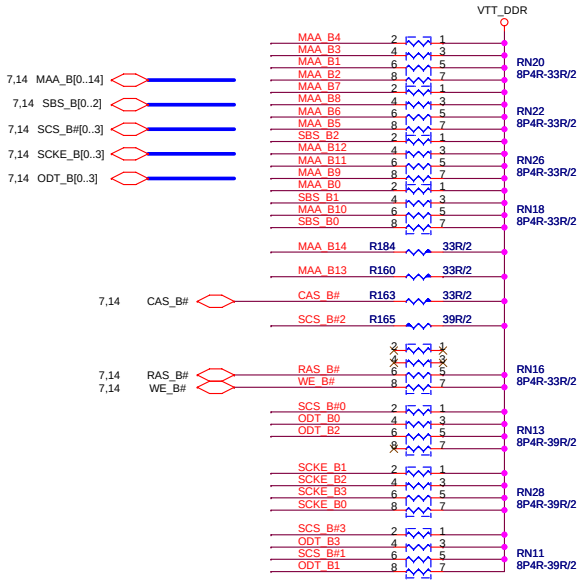
CHANNEL A V_SM_VTT DECOULPING CAPS

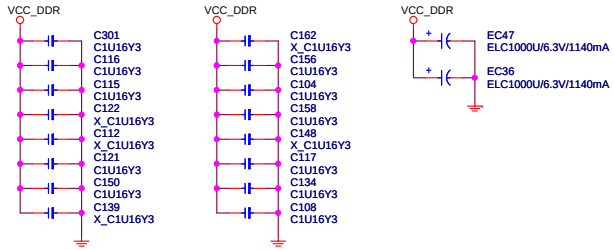


CHANNEL B V_SM_VTT DECOULPING CAPS









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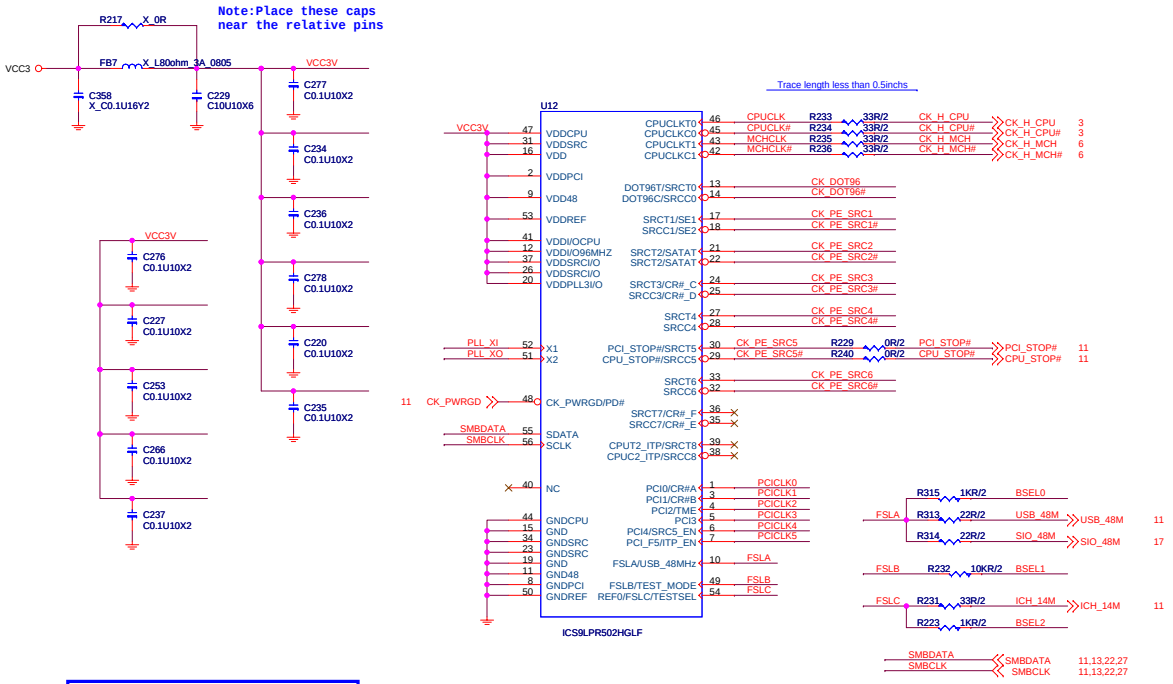
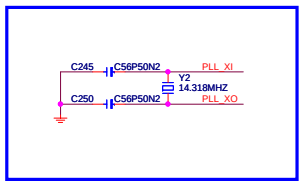
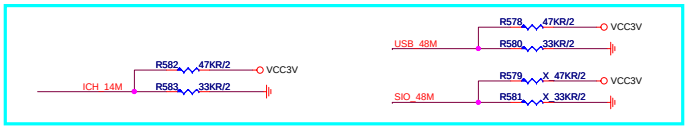
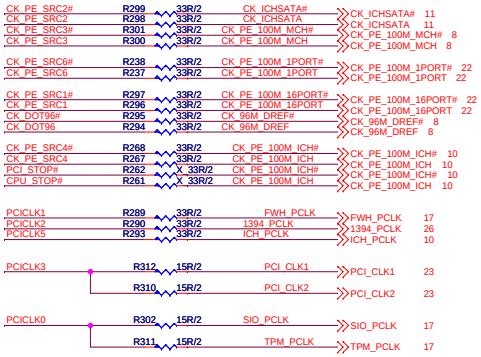
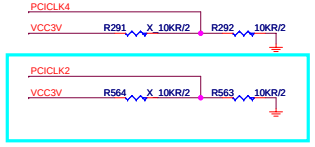
Clock Generator - ICS9LPR502

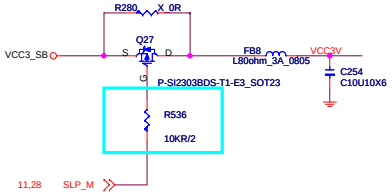




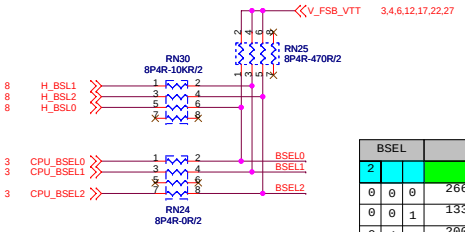




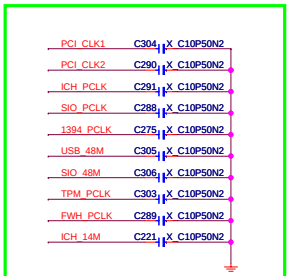




BSEL[0..2] Level Shift



BSEL			TABLE
2			
0	0	0	266 MHz (1066)
0	0	1	133 MHz (533)
0	1	0	200 MHz (800)



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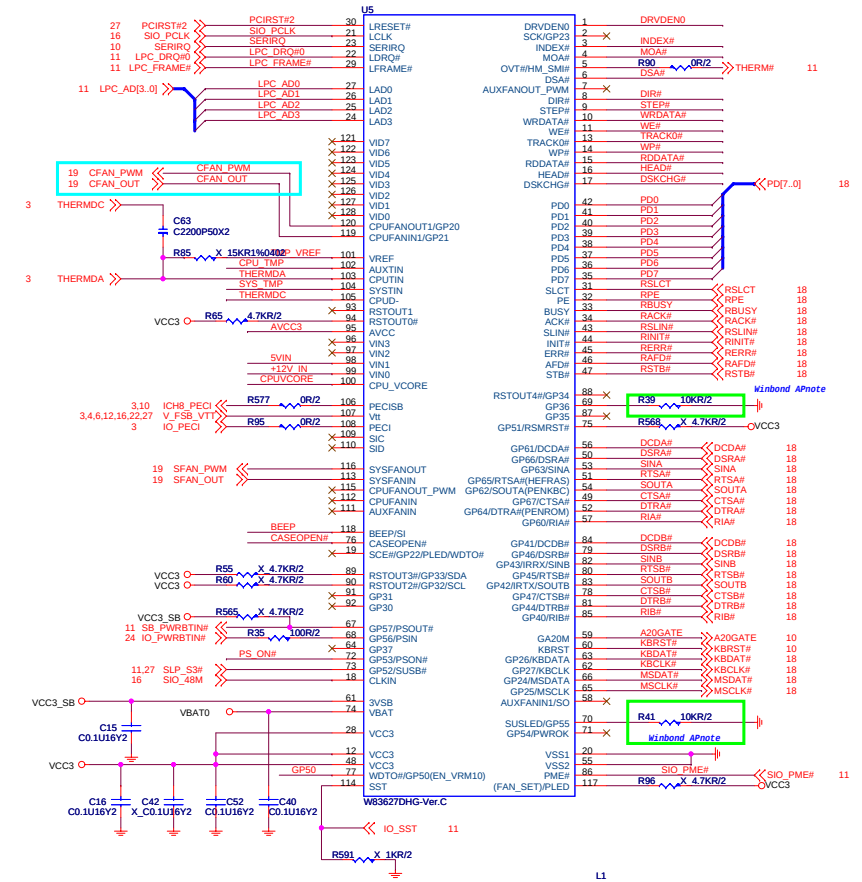
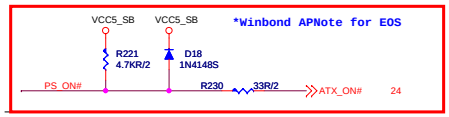
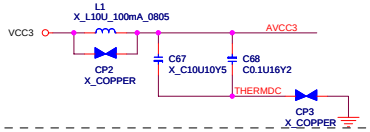
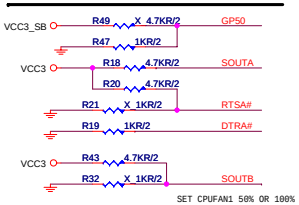
LPC SUPER I/O W83627DHG





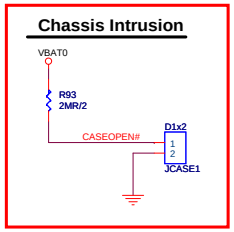


LPC I/O STRAPPING RESISTOR

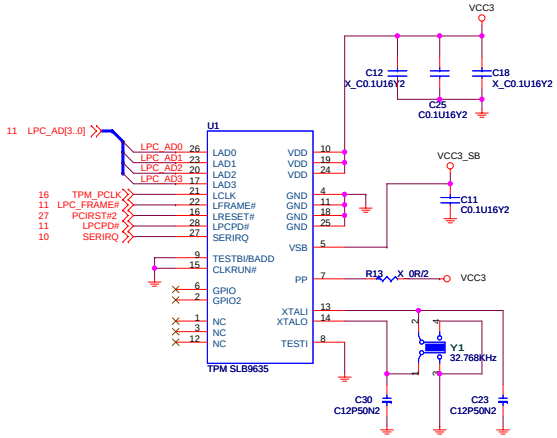


RTSA#	L: CFAD=2E	H: CFAD=4E
GP50	L: TTL LEVEL	H: VRM10 LEVEL
SOUTA	L: KBC DISABLE	H: KBC ENABLE
DTRA#	L: DISABLE SPI	H: ENABLE SPI

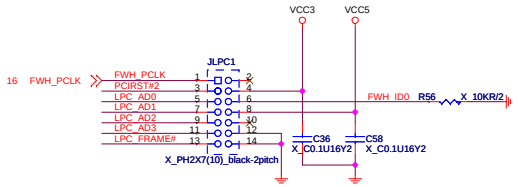
Chassis Intrusion



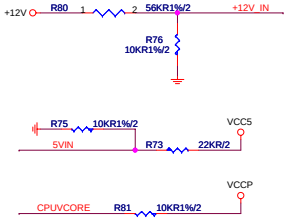
TPM - Security Controller



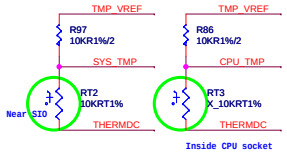
LPC Debug Port



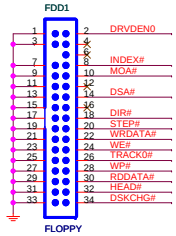
Voltage Detect

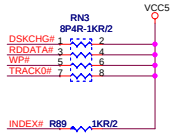


Temperature Senser

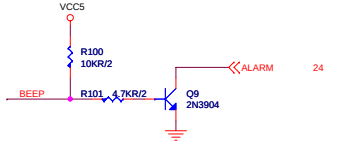


FLOPPY CONNECTOR





Beep



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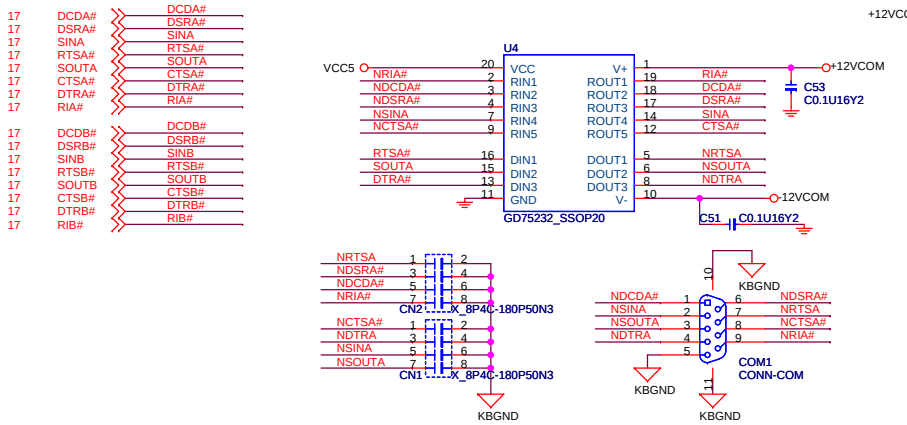
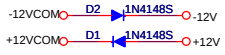
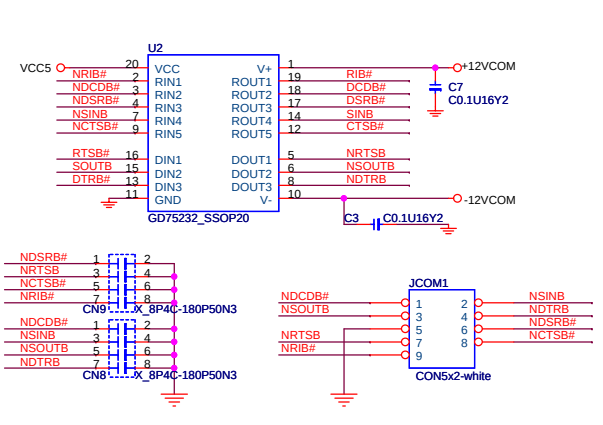
SERIAL PORT 1

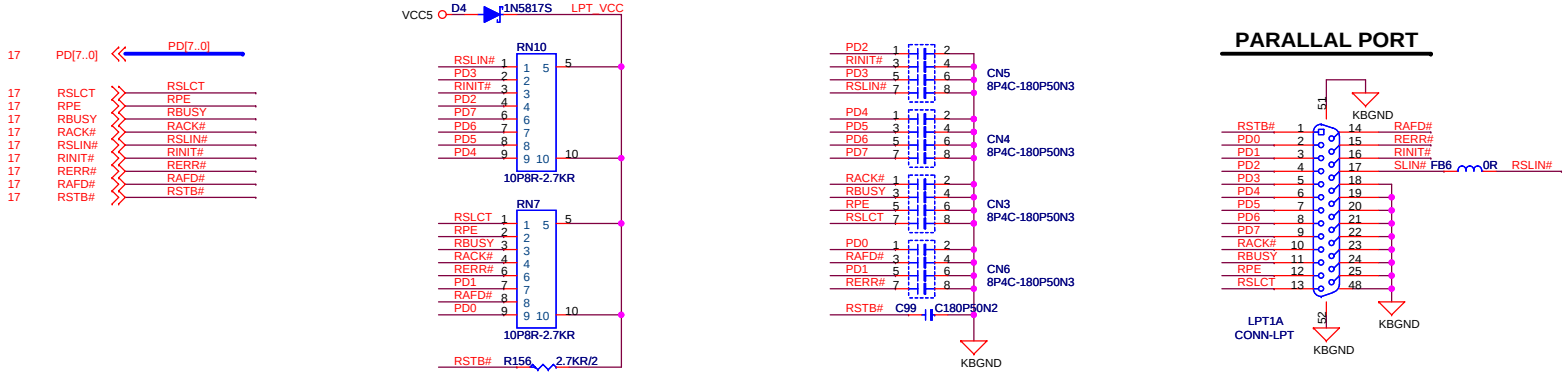




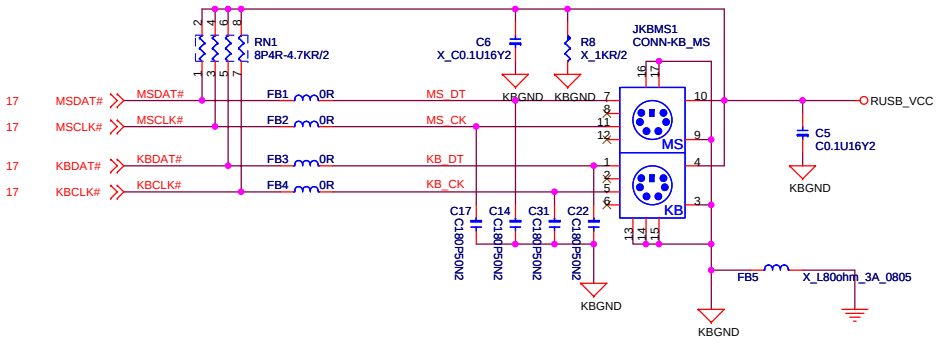
SERIAL PORT 2



PARALLAL PORT

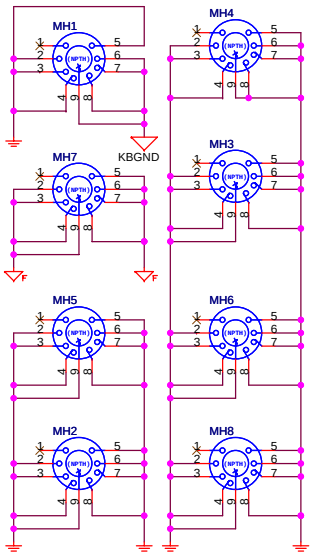


PS2 KEYBOARD & MOUSE CONNECTOR

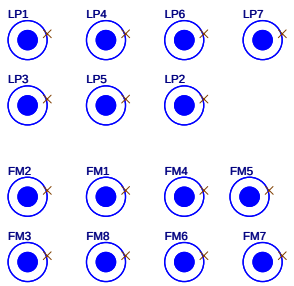


layout時應注意：將KBGND與GND，在第三層用三個50mil的通道相連

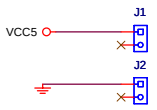
Mounting Holes



Optics Orientation Holes



Simulation



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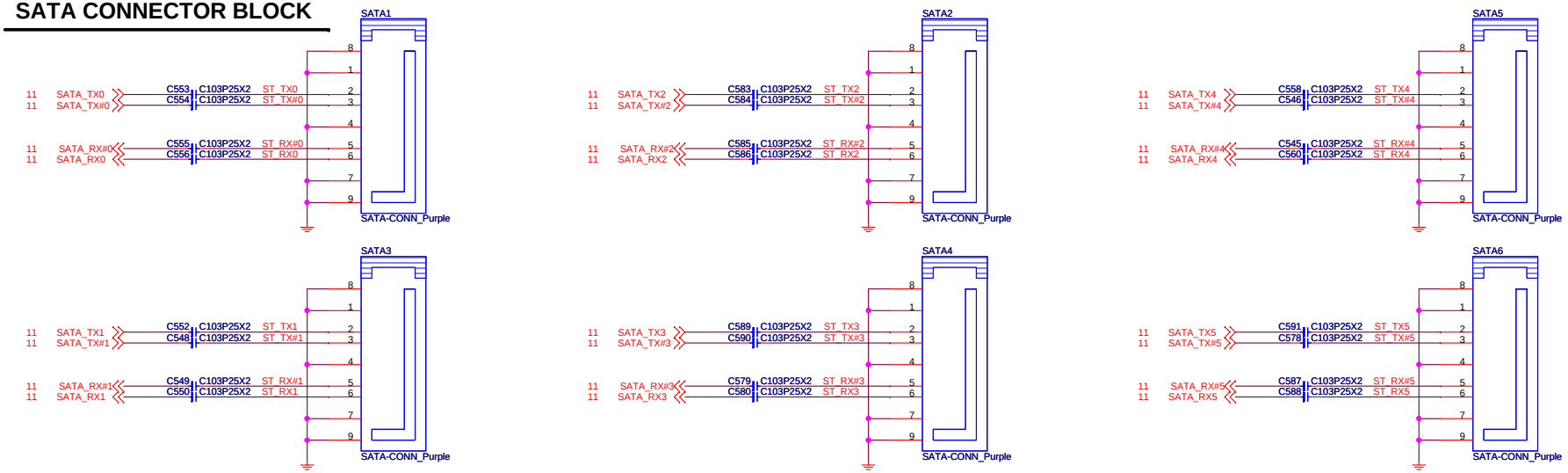
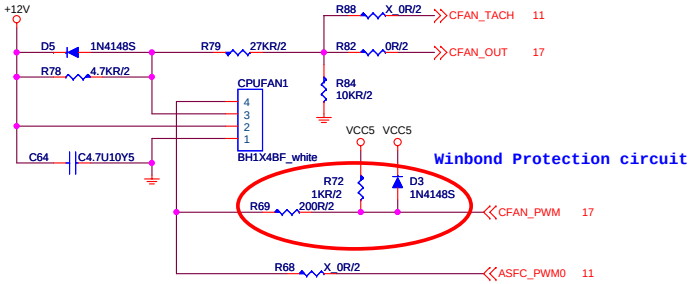
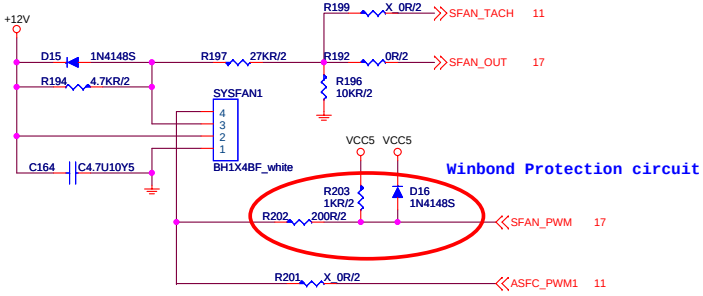
SATA CONNECTOR BLOCK



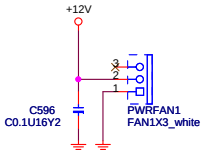
CPU FAN



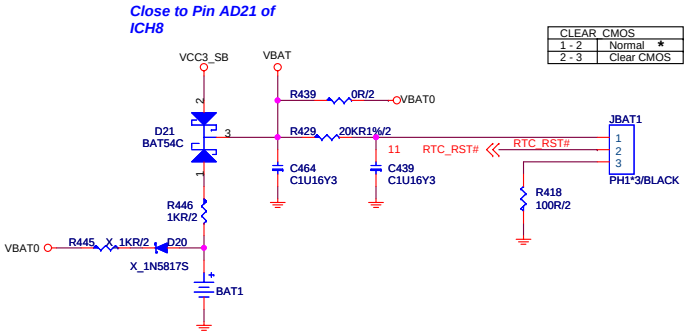
SYSTEM FAN



POWER FAN



RTC BLOCK



CLEAR_CMOS	
1 - 2	Normal
2 - 3	Clear CMOS

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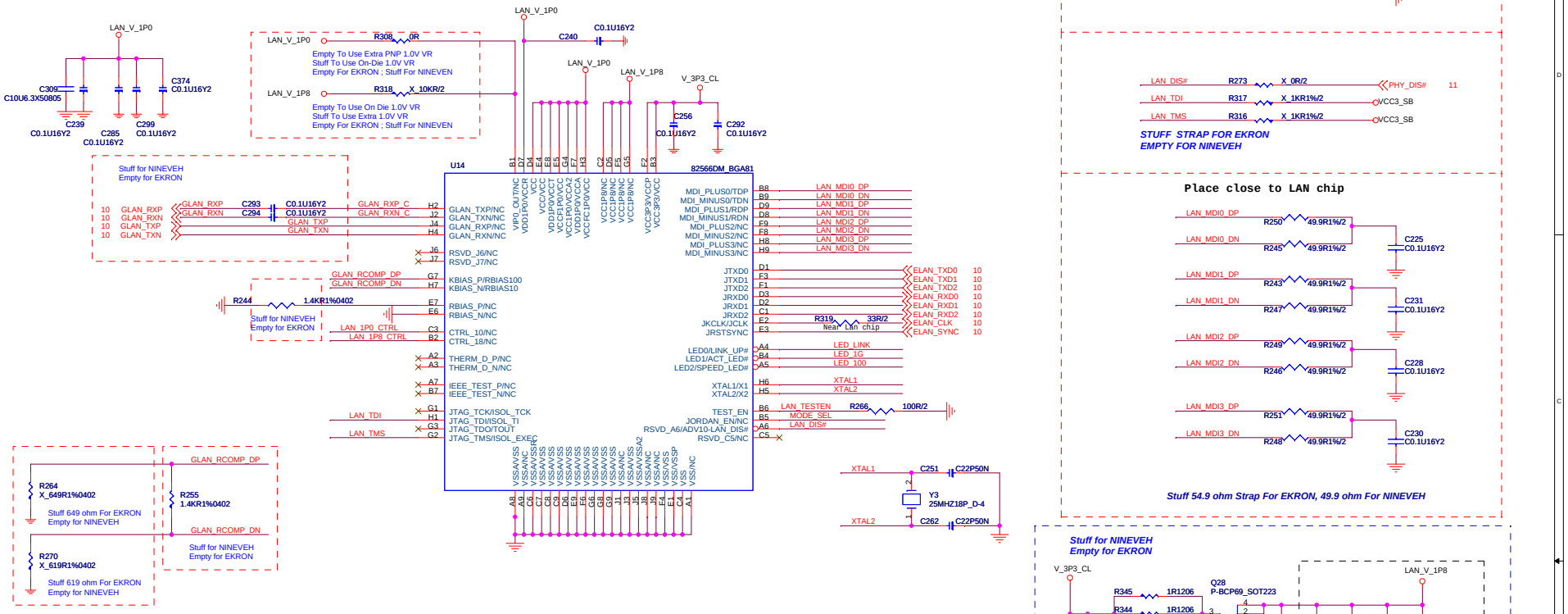
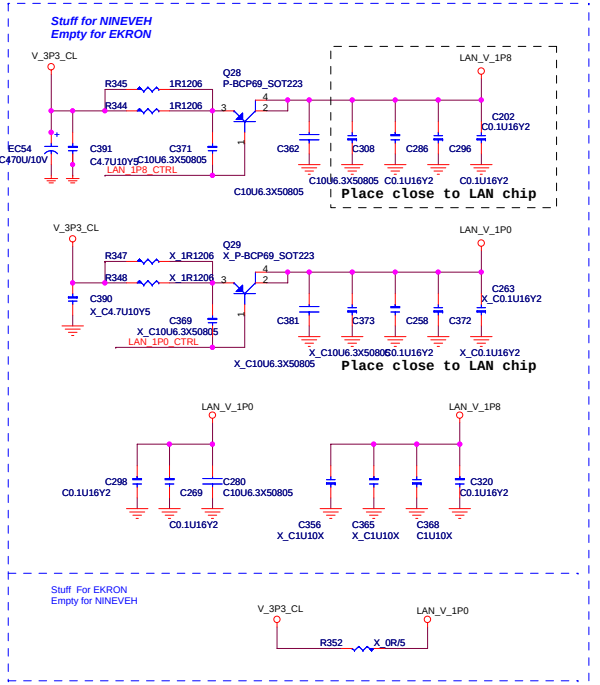
LAN - NINEVEH/EKRON





Intel 82556DM
For business desktop PCs.Support Intel AMT2 or ASF 2.0 alerting,Circuit Breaker,WoL,PXE,Multiport teaming,RSS,Intel Stable Image Platform Program drivers.
Intel 82556DC
For consumer desktop PC.Support Digital Home capabilities,WoL,PXE.
Intel 82562V
Basic 10/100 Ethernet connection.

B06-8256605-IY6
FOR NECP CONSIGN,CHIP LAN,INTEL/82566DM,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

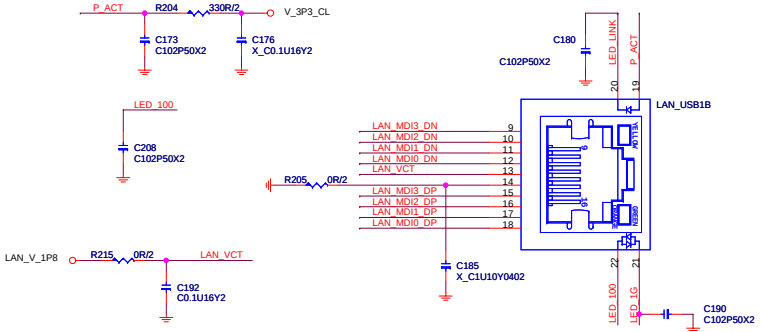
B06-8256615-I06
,CHIP LAN,INTEL/82566DC,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

B06-8256205-I06
,CHIP LAN,INTEL/82562V,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

Speed LED Type
1000Mbps : Orange
100Mbps : Green
10Mbps : LED off

YELLOW : For Active/Link

LAN CONNECTOR



ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

Giga-Lan	10/100-Lan
N58-22F0181-S42	N58-22F0061-S42 N58-22F0061-F02
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None
19 20 Yellow 21 Orange 22 Green	19 20 Yellow 21 22 Green

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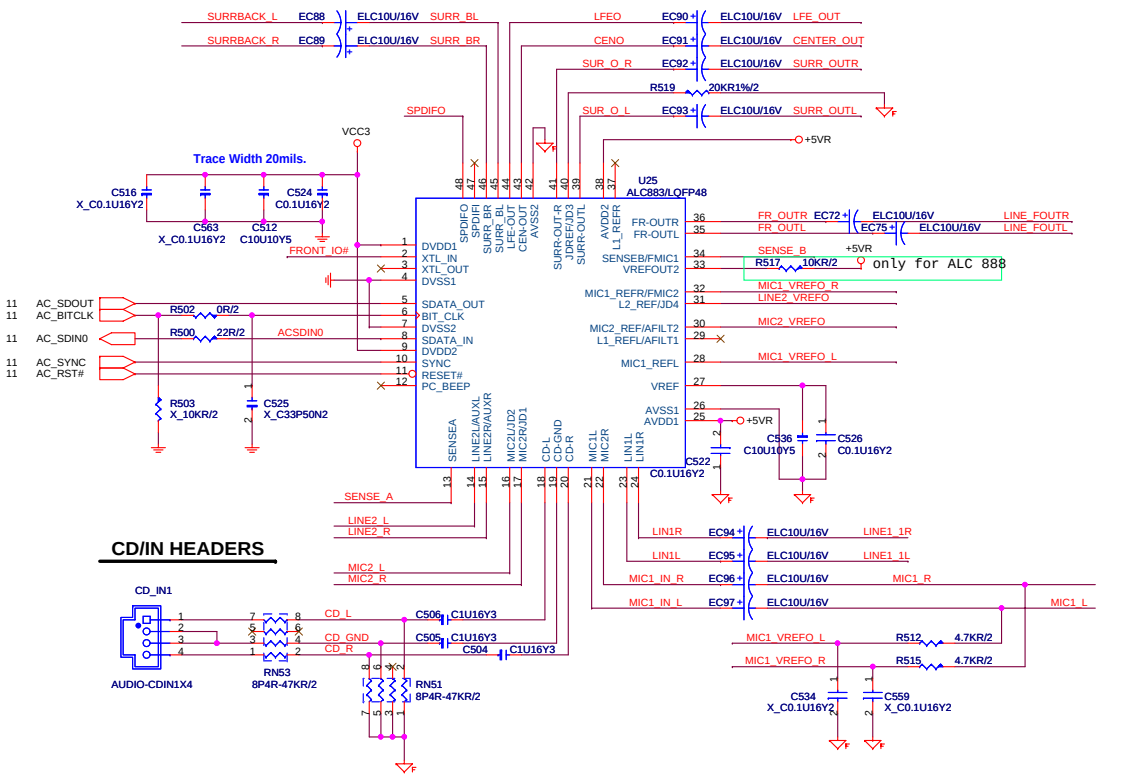
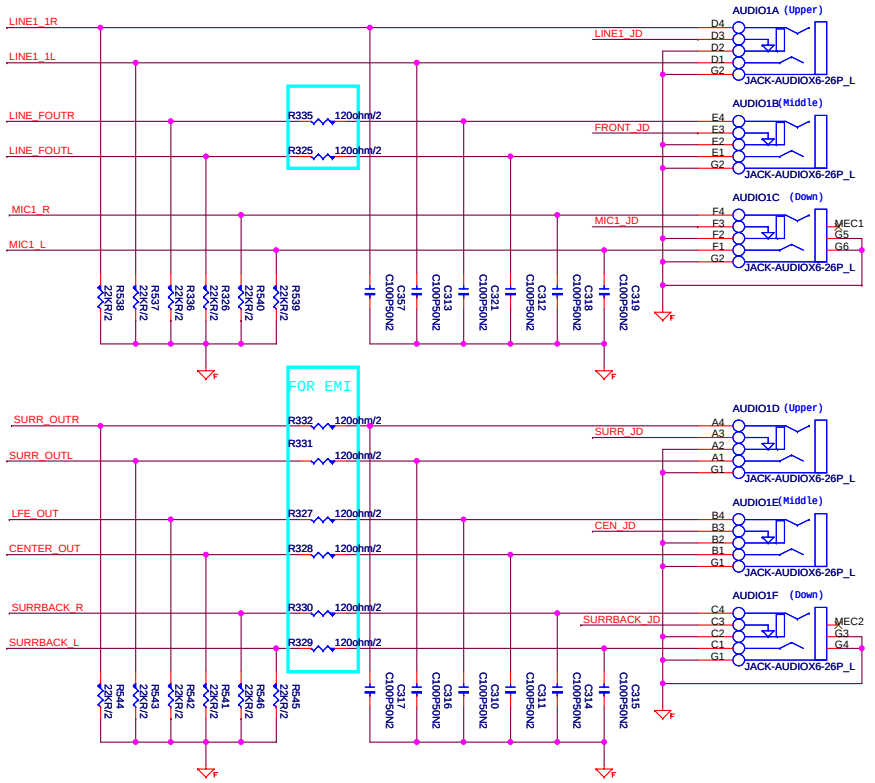
ALC883 CODEC

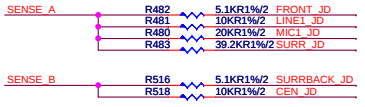


CD/IN HEADERS

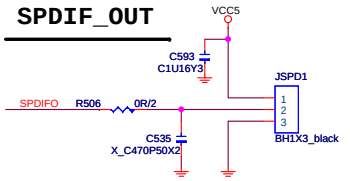
ALC883 JACK



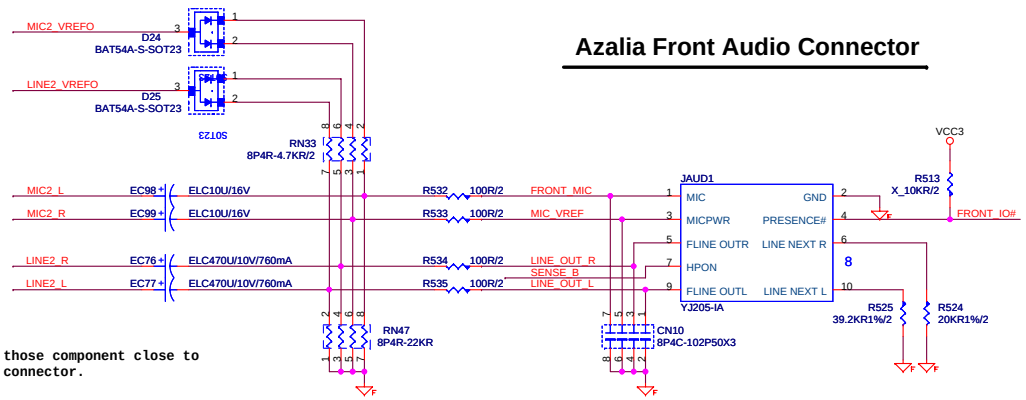
ALC883 JACK DETECT



SPDIF_OUT

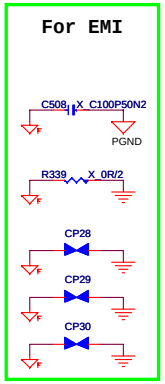


Azalia Front Audio Connector

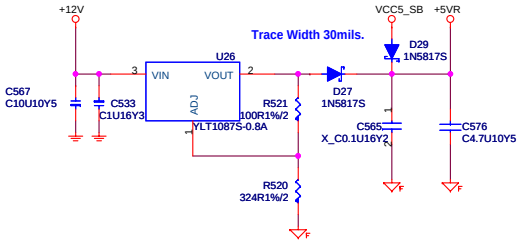


Place those component close to audio connector.

For EMI



AUDIO CODE REGULATORS



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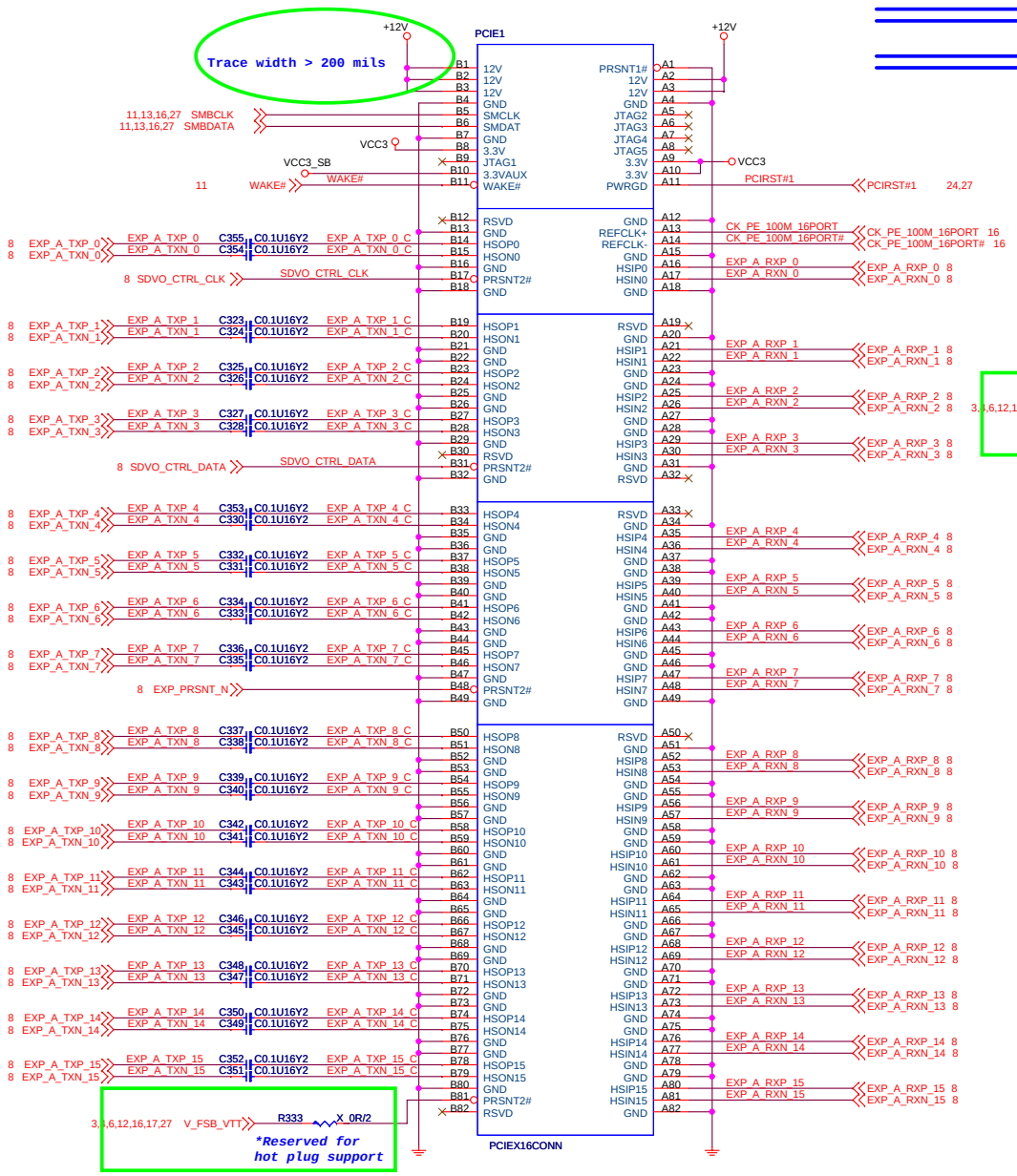
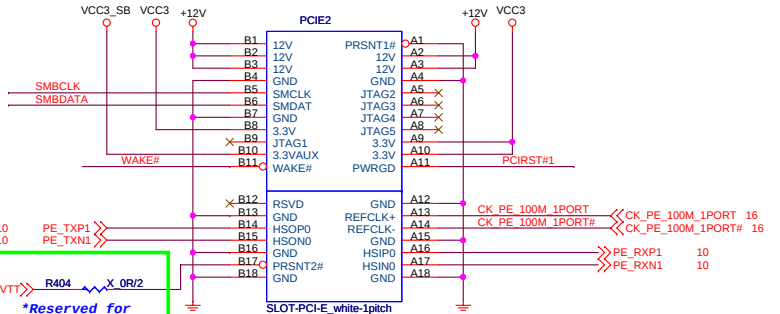
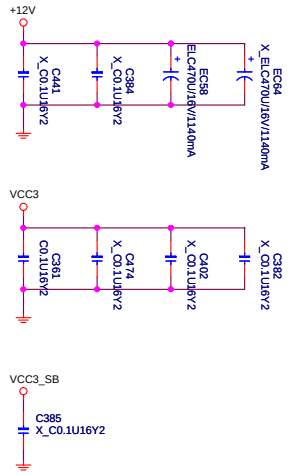
PCI EXPRESS 16-PORT



PCI EXPRESS 1-PORT





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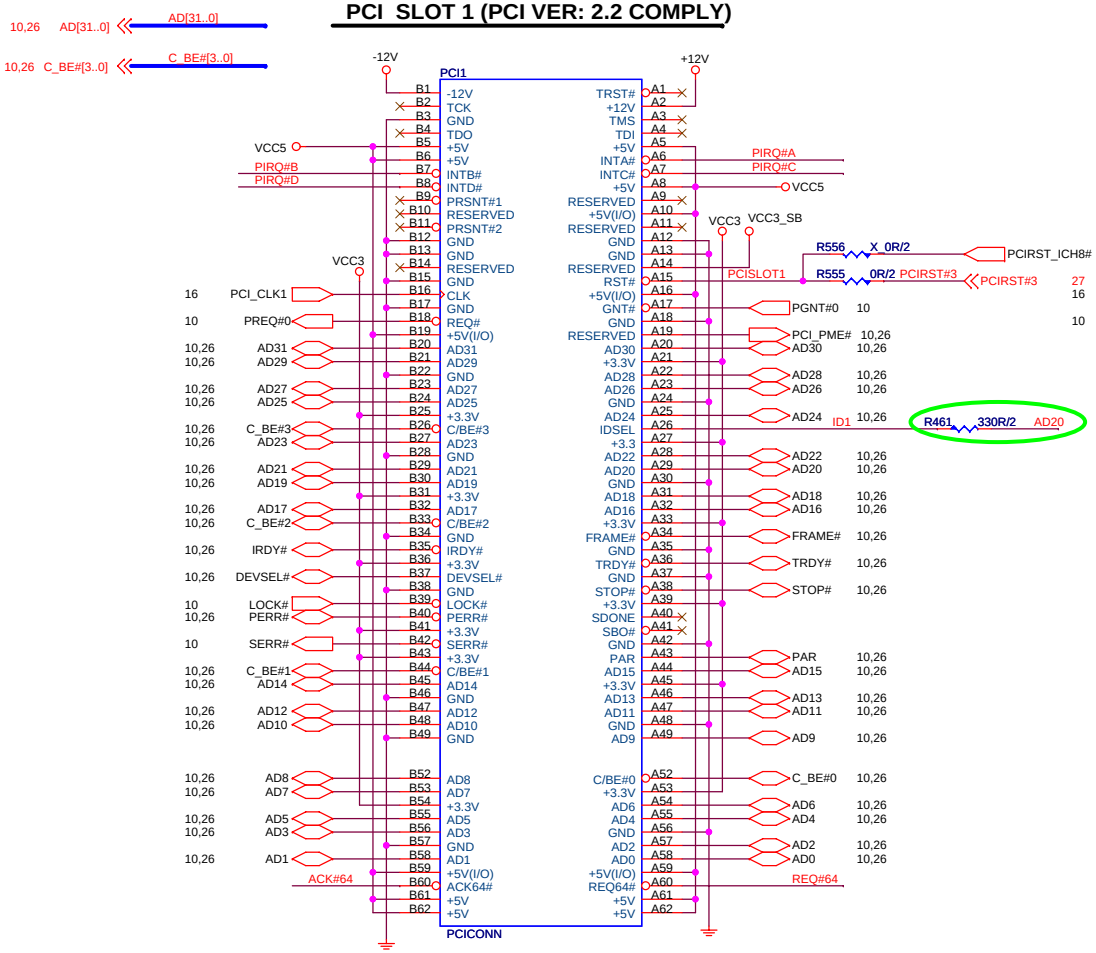
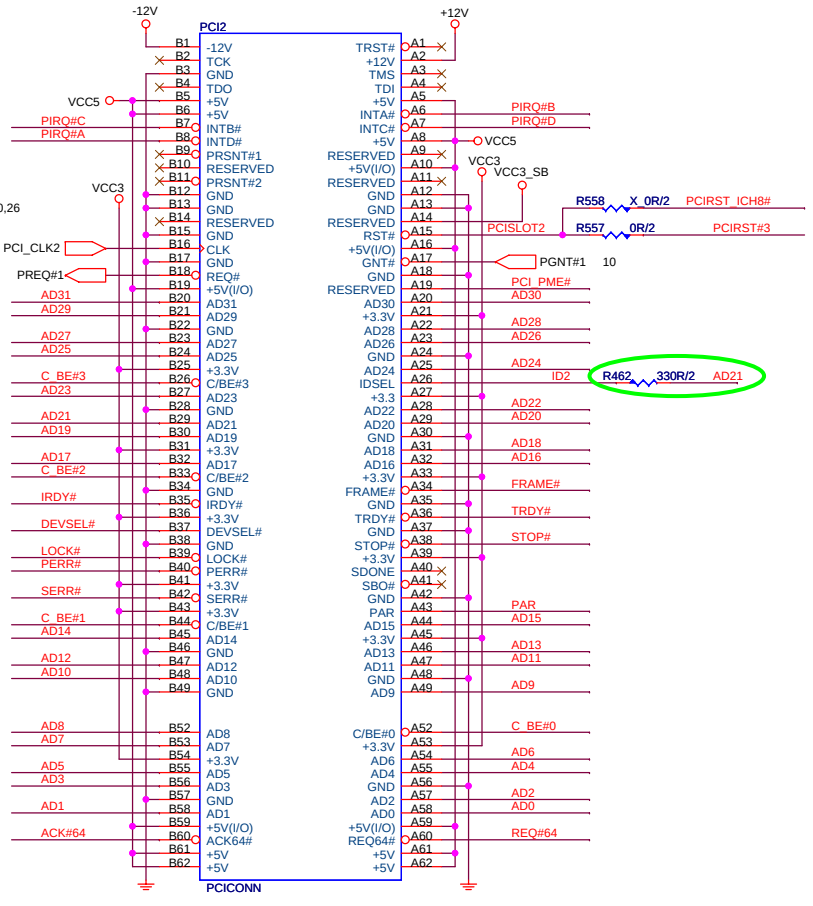
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



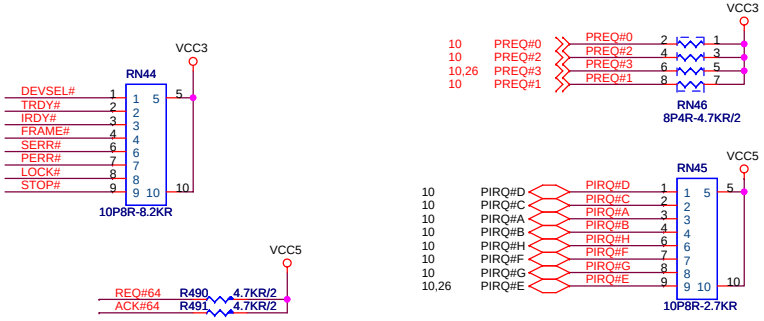
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

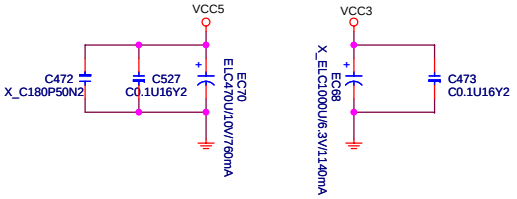


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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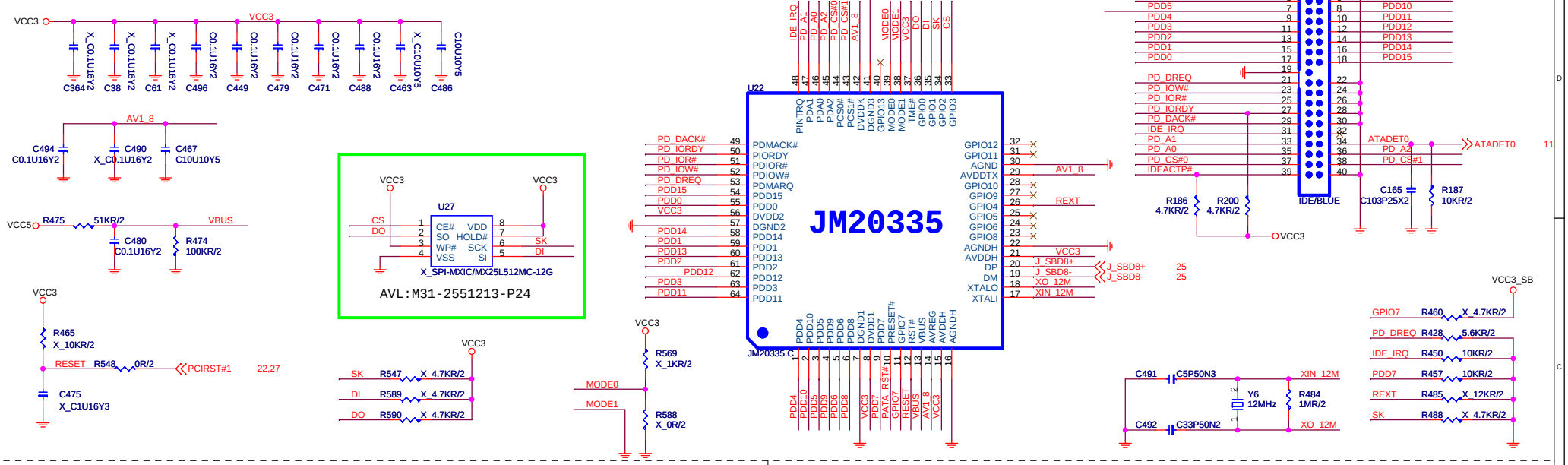
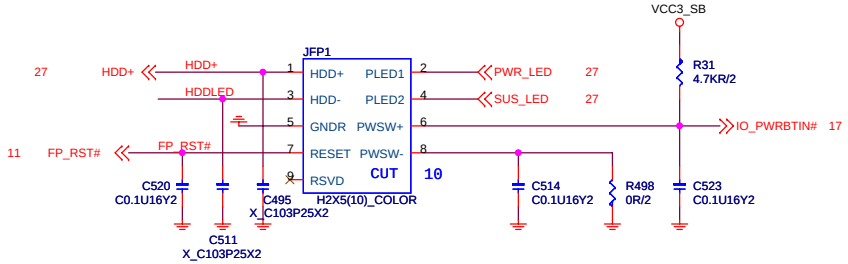
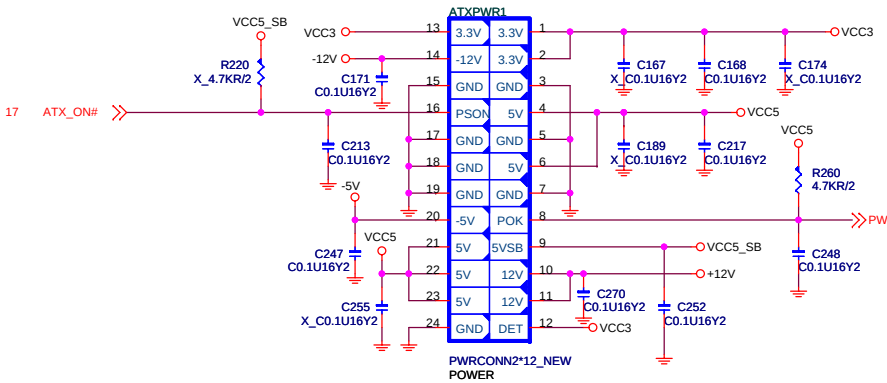
Hi-Speed USB to PATA Bridge



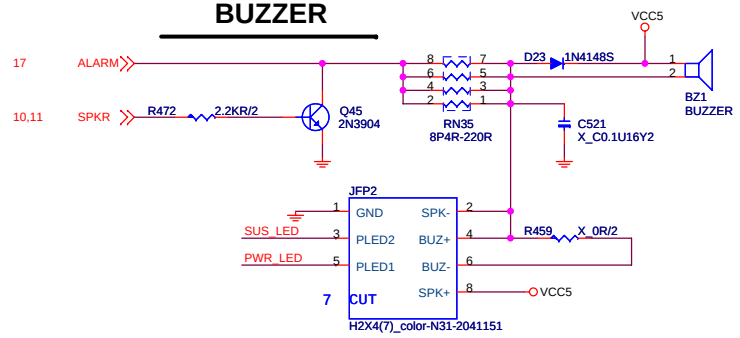
Front Panel



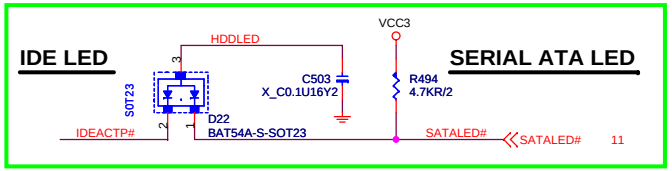
ATX CONNECTOR



BUZZER



IDE LED / SERIAL ATA LED



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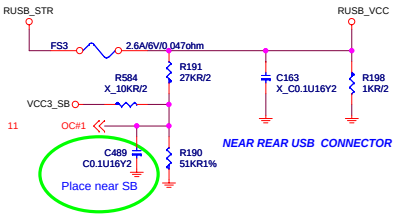
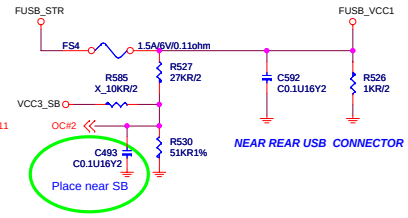
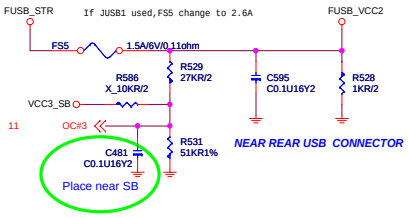
POWER CIRCUIT FOR USB PORT 0,1,2,3



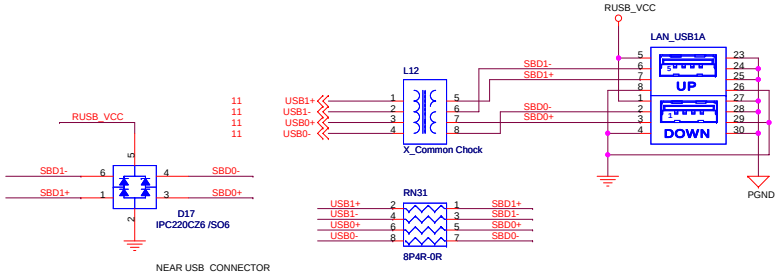
POWER CIRCUIT FOR USB PORT 4,5



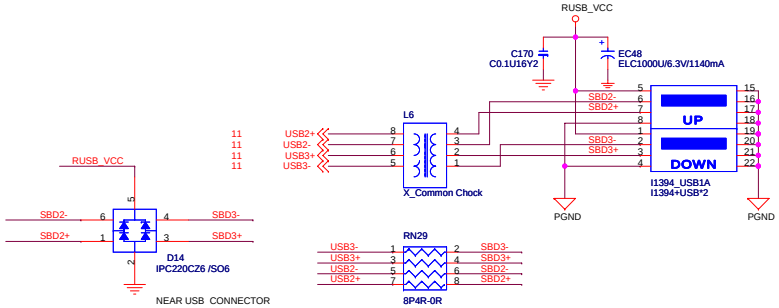
POWER CIRCUIT FOR USB PORT 6,7



REAR USB CONNECTOR FOR USB PORT 0,1

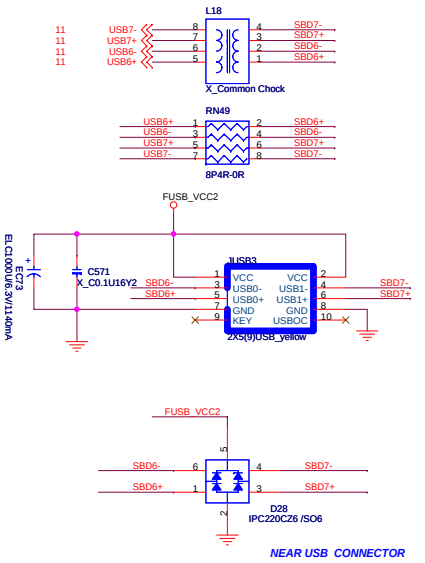


REAR USB CONNECTOR FOR USB PORT 2,3

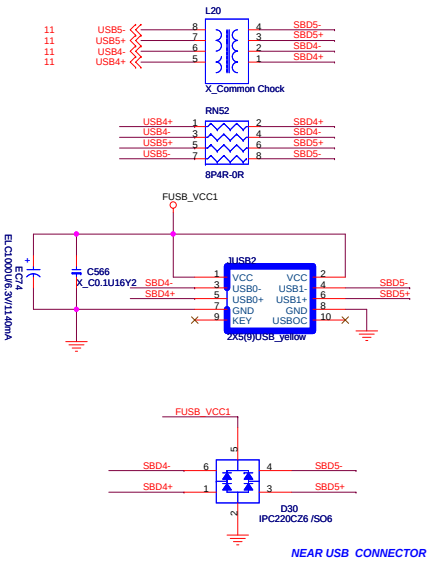


layout時應注意：將PGND與GND，在第三層用兩個50mil的通道相連

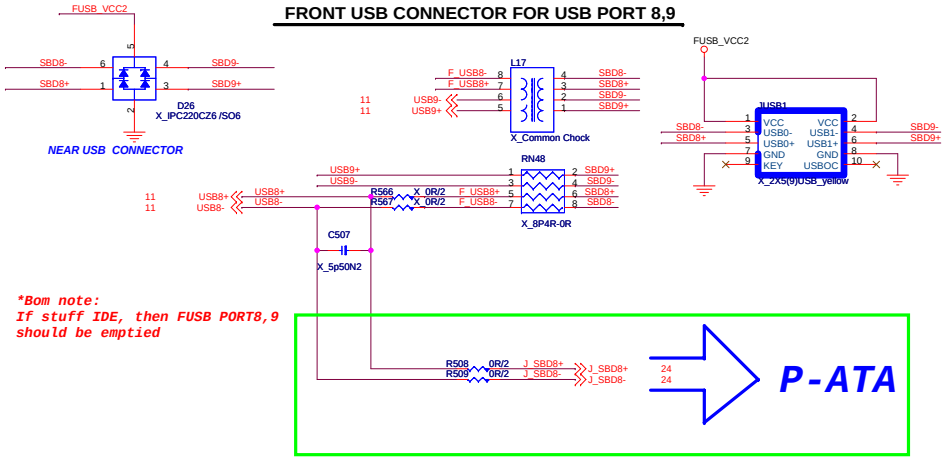
FRONT USB CONNECTOR FOR USB PORT 6,7



FRONT USB CONNECTOR FOR USB PORT 4,5



FRONT USB CONNECTOR FOR USB PORT 8,9



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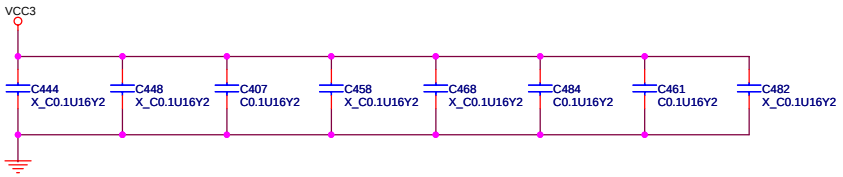
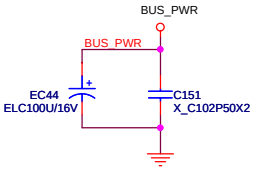
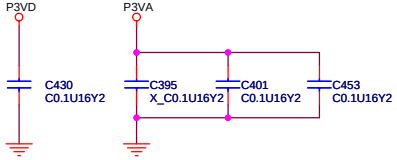
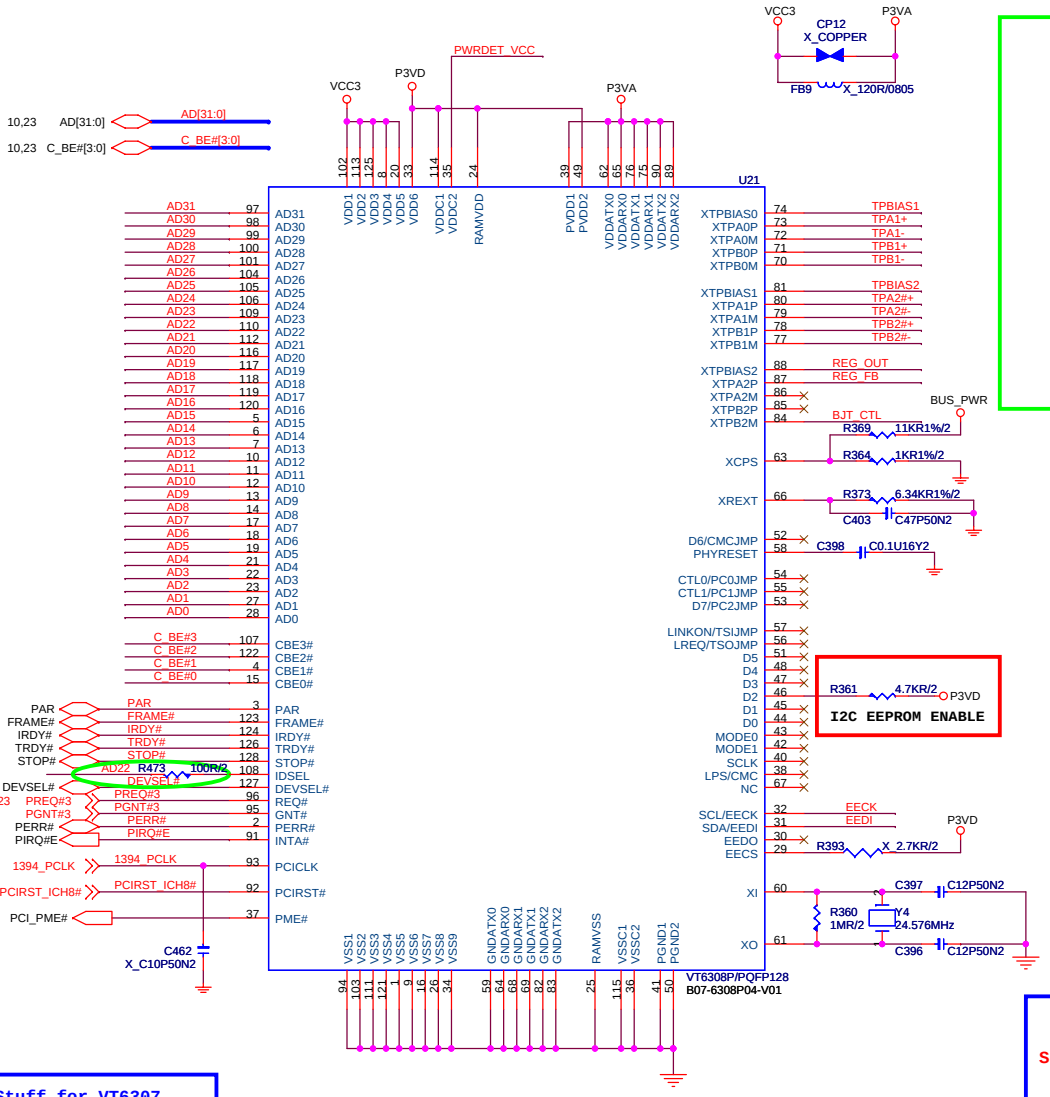
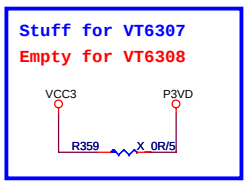


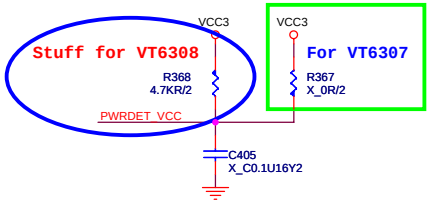


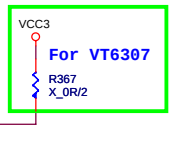


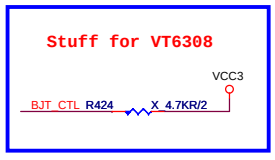
NEAR EACH POWER PIN

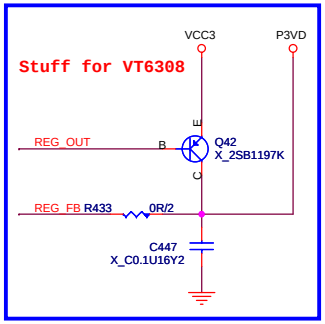




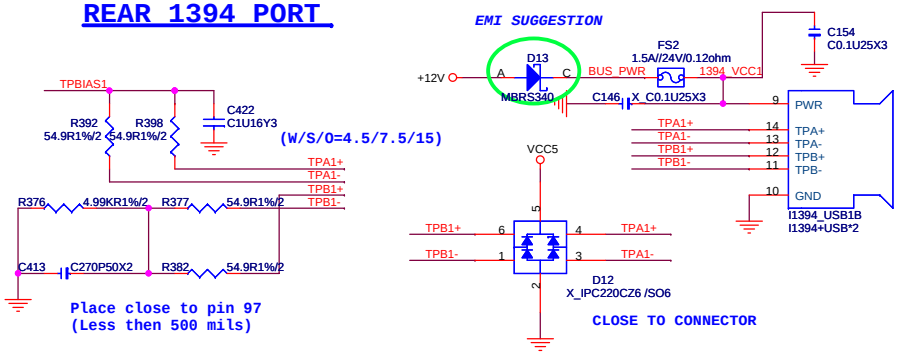




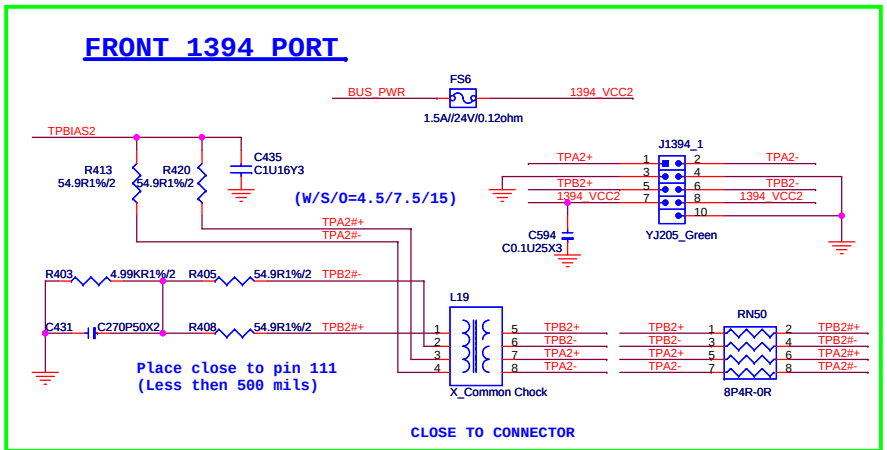


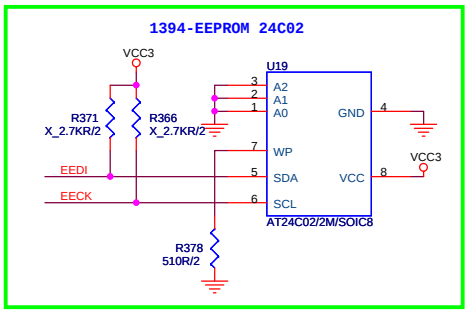


REAR 1394 PORT



FRONT 1394 PORT





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ACPI Controller MS-7

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

DDR I & DDR II VOLT SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

V_FSB_VTT 6.2A

Reserved for KENTSFIELD Processor.
(FSB1333, Quad-Core, Low Power)

THIS PIN IS OPEN DRAIN OUTPUT

Wide Trace

Close to MS11

VTT_SEL = H	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = L	V_FSB_VTT=1.2V	For normal processors.

5V DUAL Power 5A

FRONT USB

REAR USB

VCC3_SB Power

5VDIMM

V_1P25_CORE POWER...21.34A + 3.8A

*Short to V_1P25_CL if no iAMT support

Note:Iripple=Iout*[D/N-(D*D)]^0.5...D=Vout/Vin

Iripple=25*0.48=12A
(2.35*2)*1.7=7.99A<12A

CLOSE TO DEVICE FB

CONNECT TO CHOKE OUTPUT

DCR=1.68mohm

Layout Note:
1.Add more and more via at MS11's GND
2.All small signal shoule be referenced to GND

V_1P5_ICH...2A + 1.17A

V_1P05_ICH...1.17A

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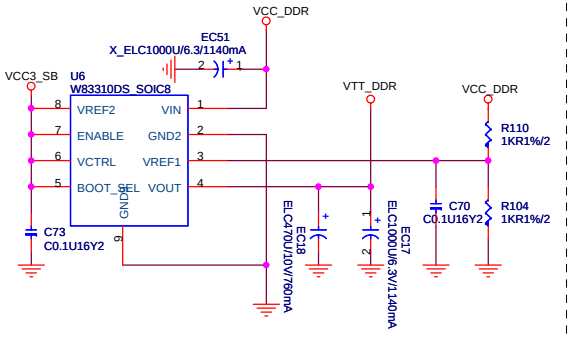
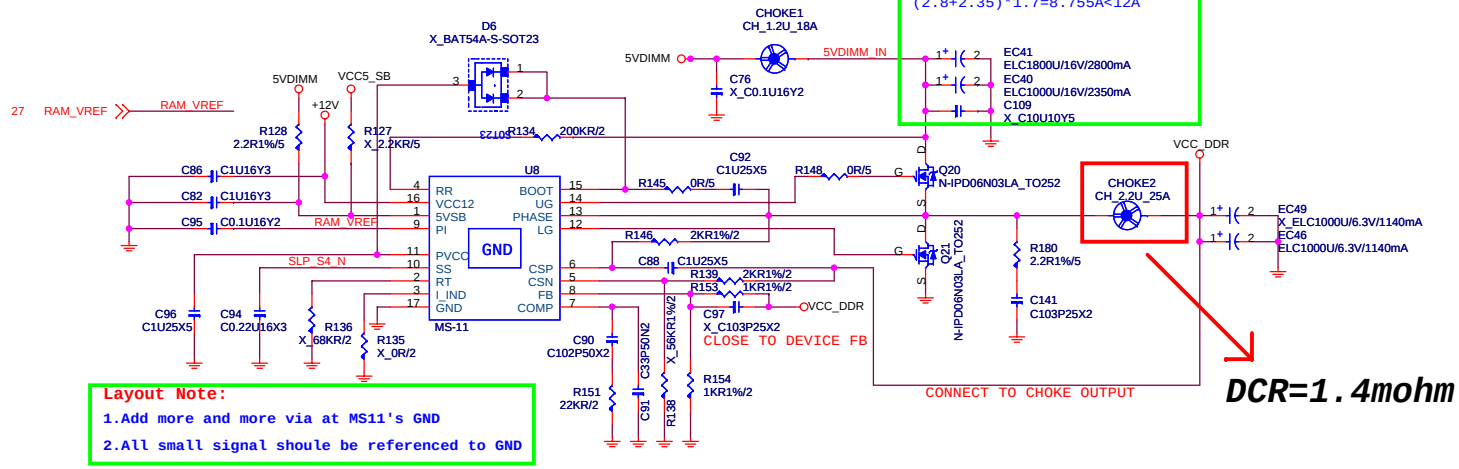
DDR II VTT POWER



DDR II 1.8V POWER...25A

Note:Iripple=Iout*[D/N-(D*D)]^0.5...D=Vout/Vin

Iripple=25*0.48=12A
(2.8+2.35)*1.7=8.755A<12A

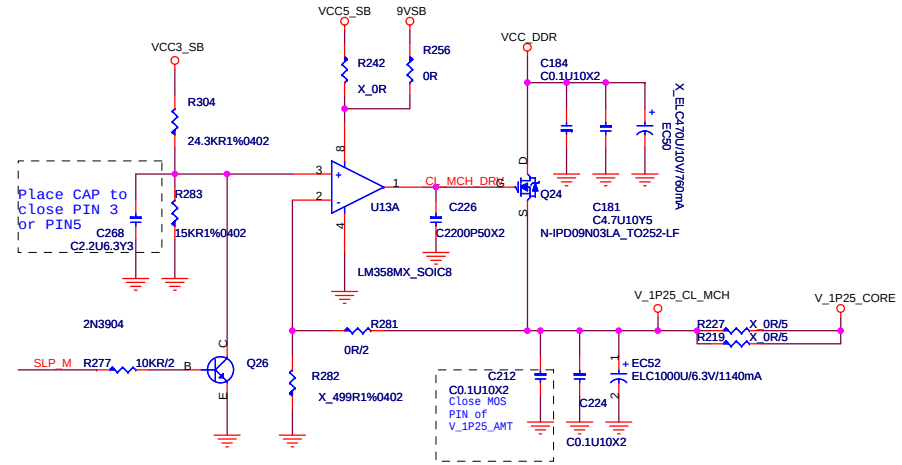


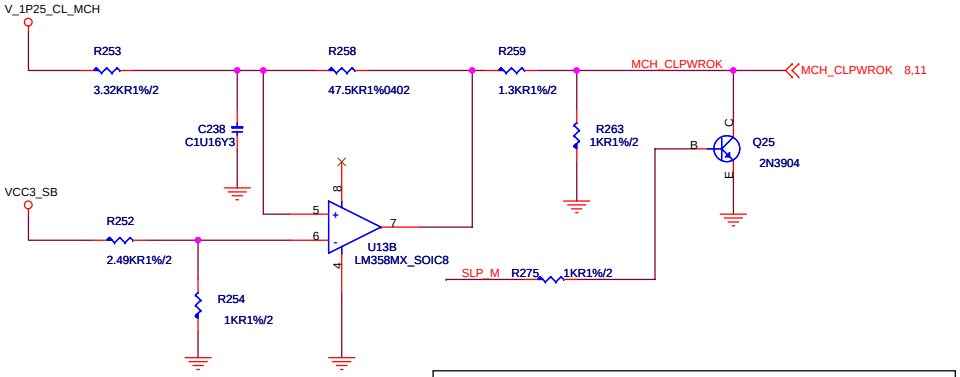
DCR=1.4mohm

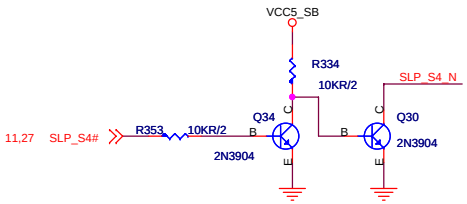
Layout Note:
1.Add more and more via at MS11's GND
2.All small signal shoule be referenced to GND

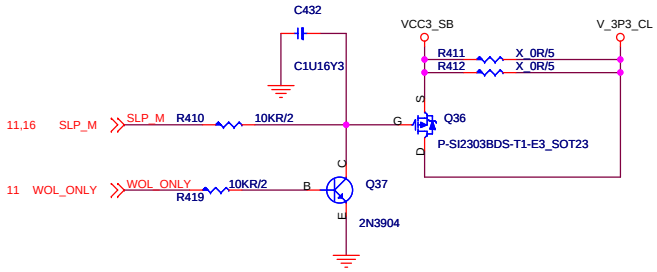
V_1P25_CL_MCH (3.8A)

For AMT power









S4_SATE#
AMT Enable-->indication of ACPI S4 state
SLP_S4#
AMT Disable-->indicate ACPI S4 state,DRAM power off.
AMT Enable-->not be assered ACPI S4 state,DRAM power ON
AMT Enable SLP_M#-->Control the overall power to Intel
AMT during ACPI S3-S5.

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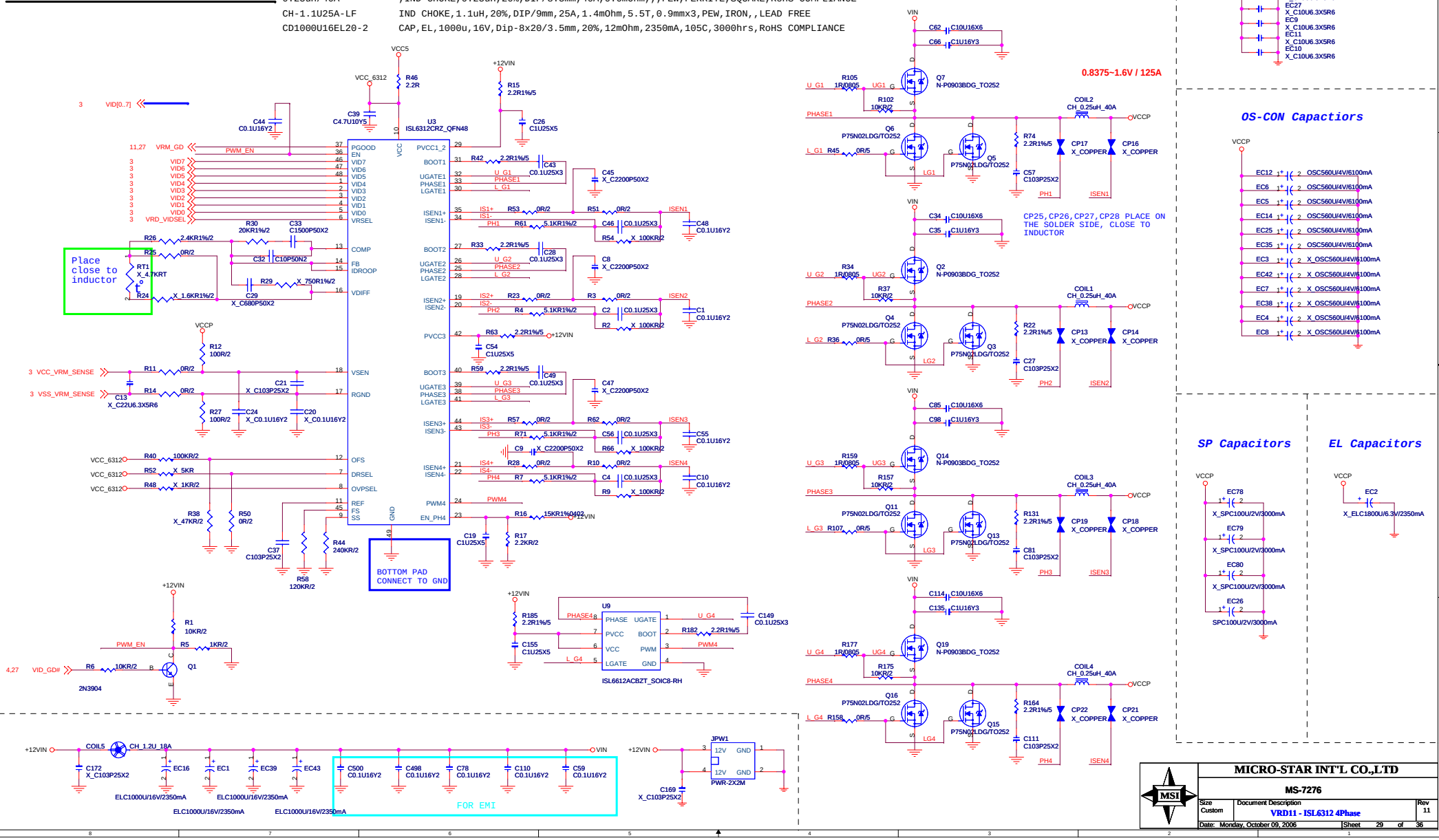
Voltage Regular Module

N-P0903BDG_TO252	mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=9.5m (10V/25A),Vgs(on) =1~3V,Id=50A,Ciss=1800pf,Qg=50nC,Vds=25V,Vgs=±20V,RoHS compliance
P75N02LDG/TO252	mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7m (@10V,30A),Vgs(on)=1~3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs=±20V,RoHS compliance
C100U2SP	ESR<15m ,Ripple cur<2.7A,LC<12uA,105C
CD560U4OS-2	CAP,OS-CON,560u/4V,Dip-2/8*9/3.5mm,ESR<7mohm, Ripplecur.=6100mA ,Lc. <500uA,SPEC series,RoHS compliance
1800UF/6.3V	ESR<12m , Ripplecur<2350mA,105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.25uH/40A	,IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,,,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
CH-1.1U25A-LF	IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CD1000U16EL20-2	CAP,EL,1000u,16V,Dip-8x20/3.5mm,20%,12mOhm,2350mA,105C,3000hrs,RoHS COMPLIANCE



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Model	MS-7276
Size	Custom
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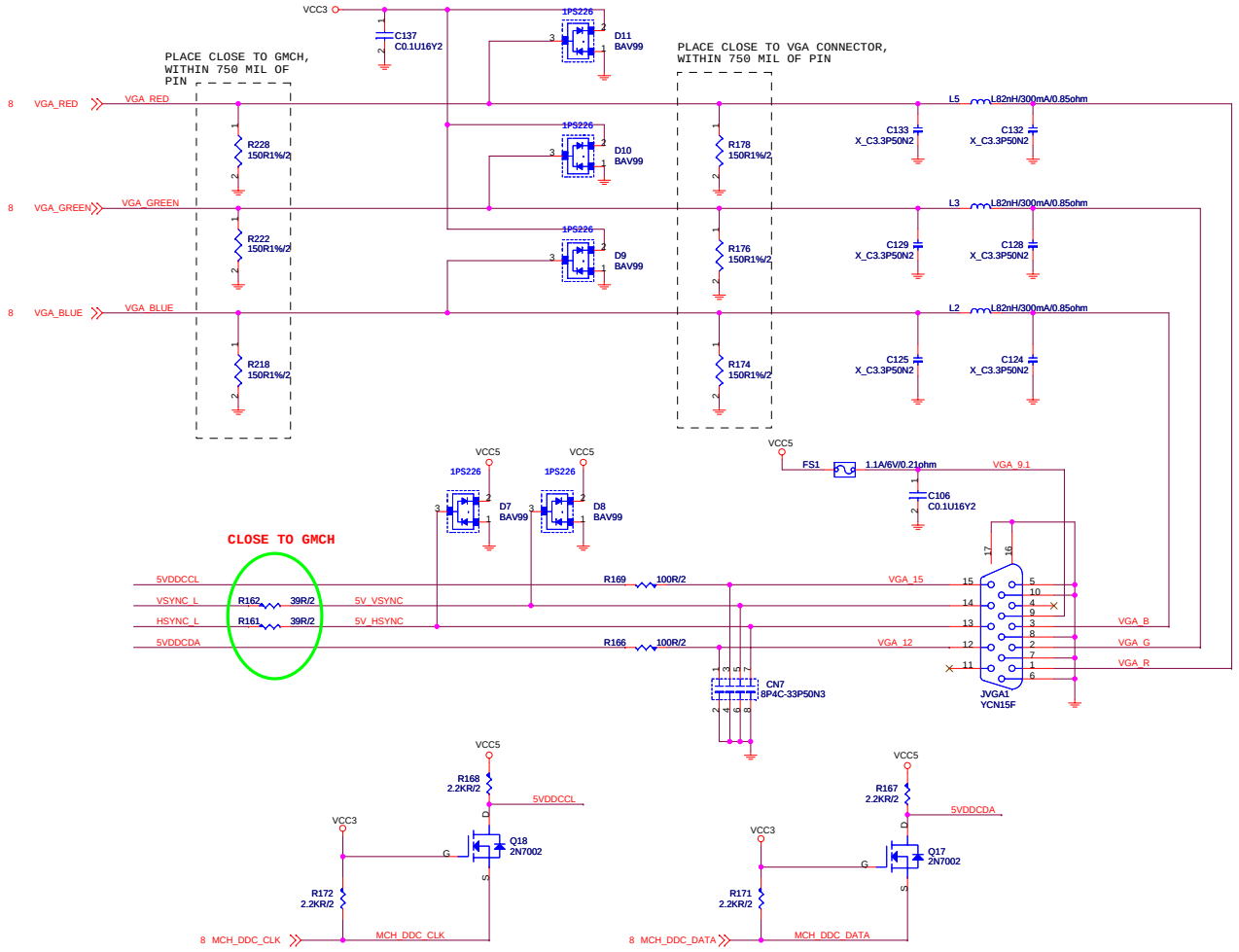
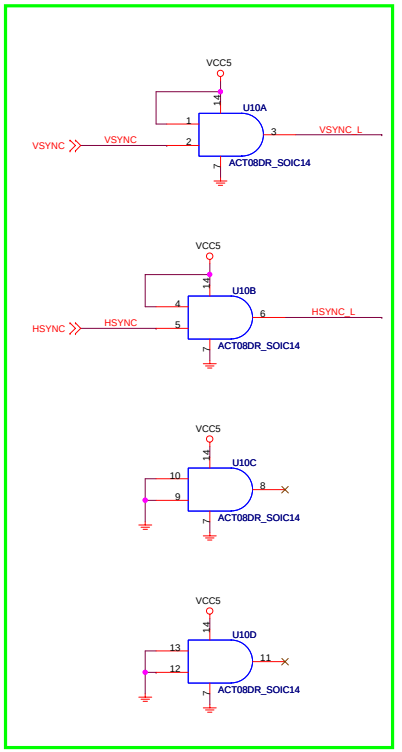
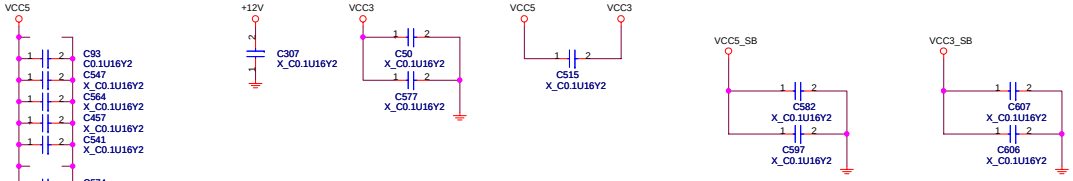
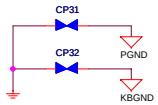
Video Connector





EMI Reserved





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ICH8

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	unmuxed		I/O	Core	Y	Y	3.3V	GPI	SIO_SMI#
GPIO[1]	TACH1		I/O	Core	Y	Y	3.3V	GPI	SFAN_TACH
GPIO[5:2]	PIRQ[H:E]#		I/OD	Core	Y	Y	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]		I/O	Core	Y	Y	3.3V	GPI	GPIO_[7:6]
GPIO[8]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	SIO_PME#
GPIO[9]	WOL_EN		I/O	Resume	Y	Y	3.3V	Native	GPIO_9
GPIO[10]	CLGPIO1		I/O	Resume	Y	Y	3.3V	GPI	GPIO_10
GPIO[11]	SMBALERT#		I/O	Resume	Y	Y	3.3V	Native	SMB_ALERT#
GPIO[12]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	ATADET0
GPIO[13]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	CLEAR_CMOS#
GPIO[14]	CLGPIO2		I/O	Resume	Y	Y	3.3V	GPI	GPIO_14
GPIO[15]	unmuxed		I/O	Resume			3.3V	GPO	
GPIO[16]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[17]	TACH0		I/O	Core	Y		3.3V	GPI	CFAN_TACH
GPIO[18]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[19]	SATA1GP		I/O	Core	Y		3.3V	GPI	GPIO_19
GPIO[20]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[21]	SATA0GP		I/O	Core	Y		3.3V	GPI	GPIO_21
GPIO[22]	SCLOCK		I/O	Core	Y		3.3V	GPI	GPIO_22
GPIO[23]	LDRQ1#		I/O	Core	Y		3.3V	Native	LDRQ_1#
GPIO[24]	CLGPIO0		I/O	Resume			3.3V	GPO	
GPIO[25]	unmuxed		I/O	Resume			3.3V	Native	FRONT_IO#
GPIO[26]	S4_STATE#		I/O	Resume			3.3V	GPO	
GPIO[27]	EL_STATE0		I/O	Resume			3.3V	GPO	
GPIO[28]	EL_STATE1		I/O	Resume			3.3V	GPO	
GPIO[29]	OC5#		I/O	Resume	Y		3.3V	Native	OC#2
GPIO[30]	OC6#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[31]	OC7#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[32]	unmuxed		I/O	Core			3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed		I/O	Core			3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[35]	SATACLKREQ#		I/O	Core			3.3V	GPO	
GPIO[36]	SATA2GP		I/O	Core	Y		3.3V	GPI	GPIO_36
GPIO[37]	SATA3GP		I/O	Core	Y		3.3V	GPI	GPIO_37
GPIO[38]	SLOAD		I/O	Core	Y		3.3V	GPI	GPIO_38
GPIO[39]	SDATAOUT0		I/O	Core	Y		3.3V	GPI	GPIO_39
GPIO[43:40]	OC[4:1]#		I/O	Resume	Y		3.3V	Native	OC#1;OC#2
GPIO[47:44]	NA		NA	NA			NA	NA	Not implemented
GPIO[48]	SDATAOUT1		I/O	Core	Y		3.3V	GPI	GPIO_48
GPIO[49]	CPUPWRGD		I/O	V_CPU_IO			CPU	Native	H_PWRGD
GPIO[50]	REQ1#		I/O	Core	Y		5.5V	Native	PREQ#1
GPIO[51]	GNT1#		I/O	Core			3.3V	Native	PGNT#1
GPIO[52]	REQ2#		I/O	Core	Y		5.5V	Native	PREQ#2
GPIO[53]	GNT2#		I/O	Core			3.3V	Native	PGNT#2
GPIO[54]	REQ3#		I/O	Core	Y		5.5V	Native	PREQ#3
GPIO[55]	GNT3#		I/O	Core			3.3V	Native	PGNT#3

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	PCI_CLK1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD21	PCI_CLK2
1394	PIRQ#D	PREQ#3 PGNT#3	AD22	1394_PCLK

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI_E X16 & PCI_E X1
PCIRST#2	SIO, 1394, FWH, TPM
PCIRST#3	PCI SLOT1&2,
PCIRST_ICH8#	MS7
HD_RST#	Primary IDE

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A1H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A3H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

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0A modify 10 change list

1. Add R536 for SLP_M
2. Q30.C connect to U8.10
3. change VTT_DDR drived from VCC_DDR
4. modify ALC883 circuit to meet the Vista "premium" SPEC
5. 1394 circuit modify, change net name from "VDD" to "P3VD" (page 26)
4. modify ALC883 circuit to meet the Vista "premium" SPEC
5. modify JM20335 circuit (page 24)
6. modify SMBLINK and SMBCLK/DATA circuit (page 11)
7. add C469 C539 for margin (page 12)
8. add R564 and R563 for ICS (page 16)
9. CPU FAN mornitor from AUXFANOUT change to CPUFANOUT1 (page 17)
10. add R566 and R567 for JM20335 (page 25)
11. modify V_FSB_VTT circuit (page 27)
12. change R51 R3 R62 R10 to 0ohm for power team solution (page 29)
13. modify V_1P5_ICH circuit from Vcc3 change to VCC_DDR (page 27)
14. Add Q54 and Q53 for S3 sequence (page 27)
15. reserve R522 R523 R575 R576 預防逆向電流 (page 27)
16. add R578 R579 R580 R581 R582 R583 for 48M and 14M pull high and pull down (page 16)
17. Add C606 C607 for EMI (page 30)
18. Add R584 R585 R586 for option USB OC# function (page 25)
19. change C369 and C371 footprint to 0805 (page 20)
20. change 1394`s PCIREST to PCIREST_ICH8 (page 26)

10 modify 11 change list

1. change 1394`s IRQ to PIRQ#E (page 26)
2. modify JM20335 circiut (page 24)
3. Add C498 and C500 for EMI (pang 29)
4. change R578 R579 R582 pull high to VCC3V (page 16)
5. Add C507 between USB8+ and USB8- (pang 25)
6. Add C508 between GNDF and PGND for EMI (pang 21)
7. Add R591 for winbond AP note (pang 17)

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