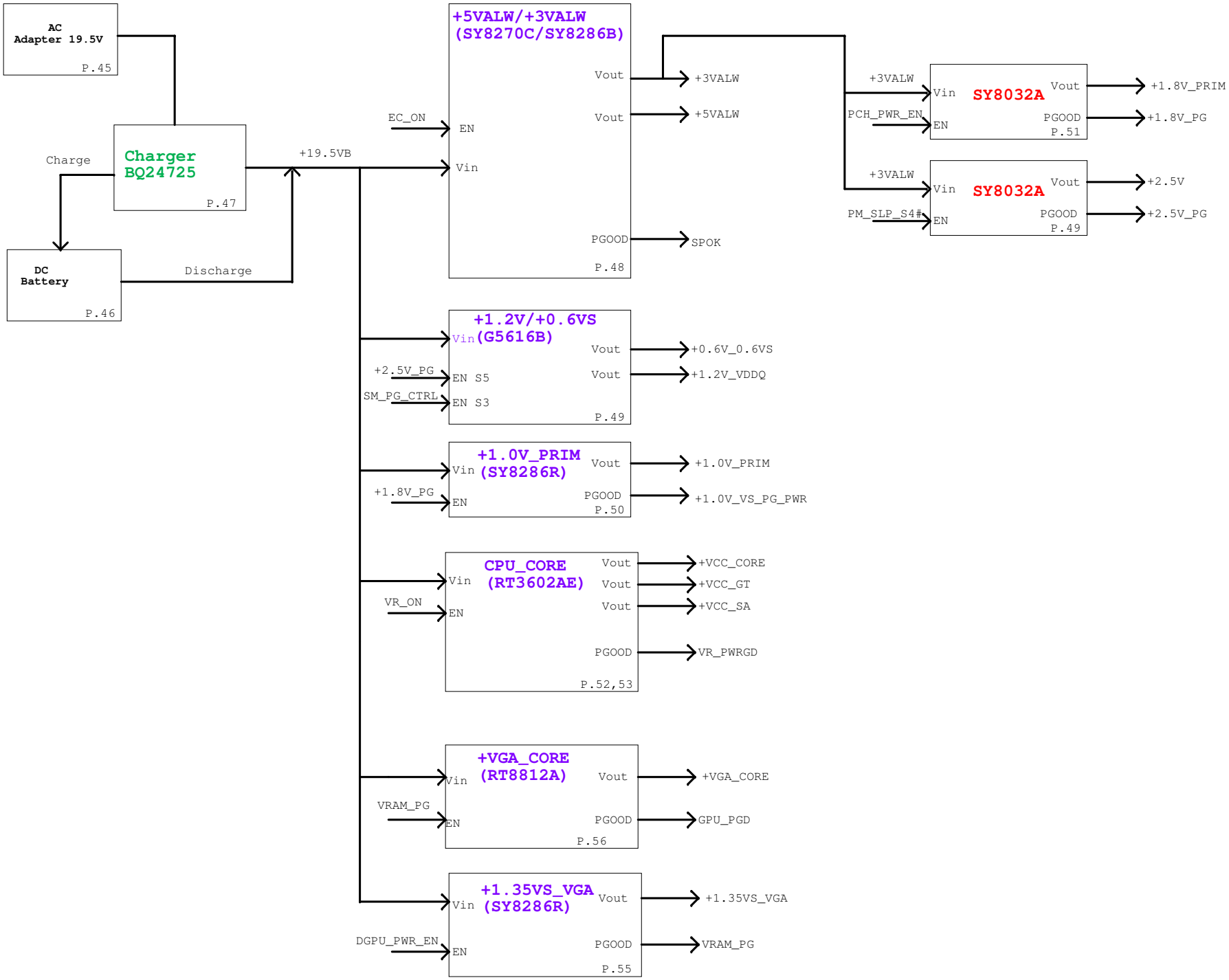

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Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title: *Power Block Diagram*

Size: | Document Number: LAH323P | Rev: v0.3

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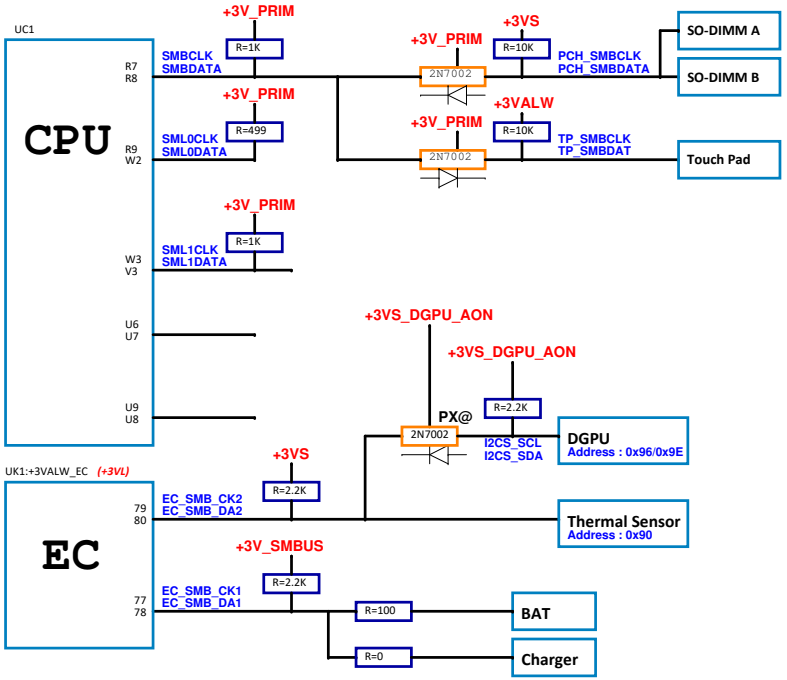

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/05/17	Deciphered Date 2021/05/17	Title: Notes List

Size: Custom	Document Number: LA-H323P		Rev: V0.1
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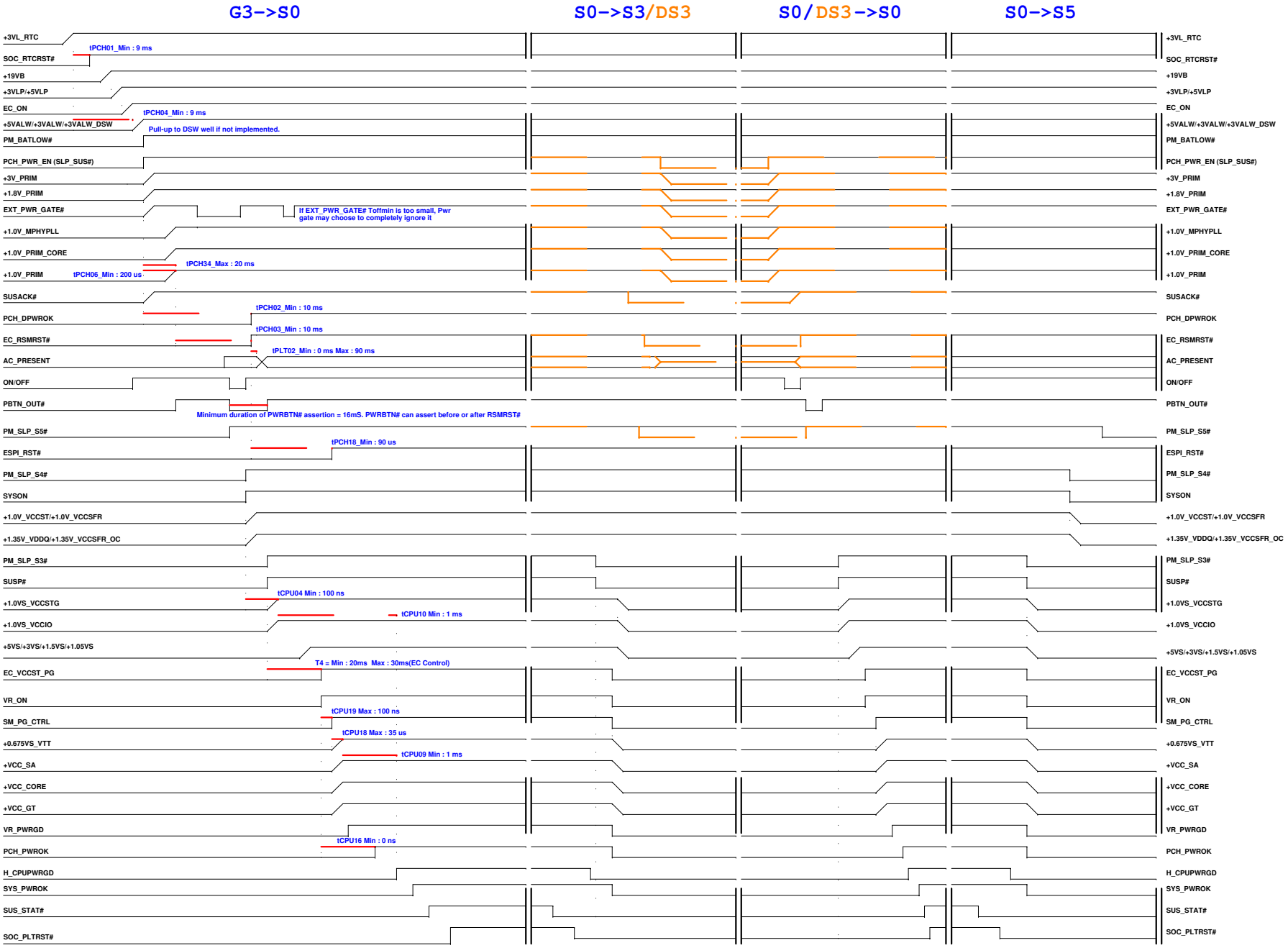
[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



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Issued Date		Deciphered Date	Title: HW Reserve

Size	Document Number	Rev
Custom	LA-H323P	Vo.1

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DDPB_CTRLDATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

1 = Port B is detected.

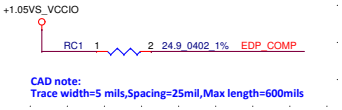
DDPC_CTRLDATA(Internal Pull Down):

Display Port C Detected

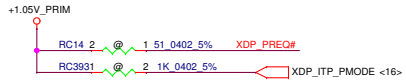
0 = Port C is not detected.

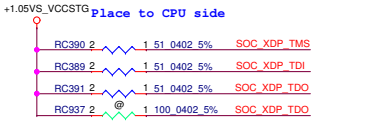
1 = Port C is detected.

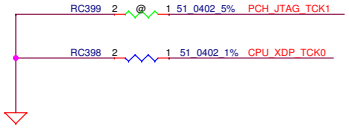
COMPENSATION PU FOR eDP

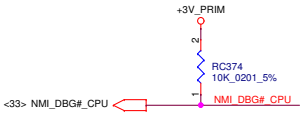


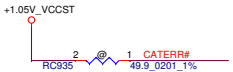
CAD note:
Trace width=5 mils,Spacing=25mil,Max length=600mils

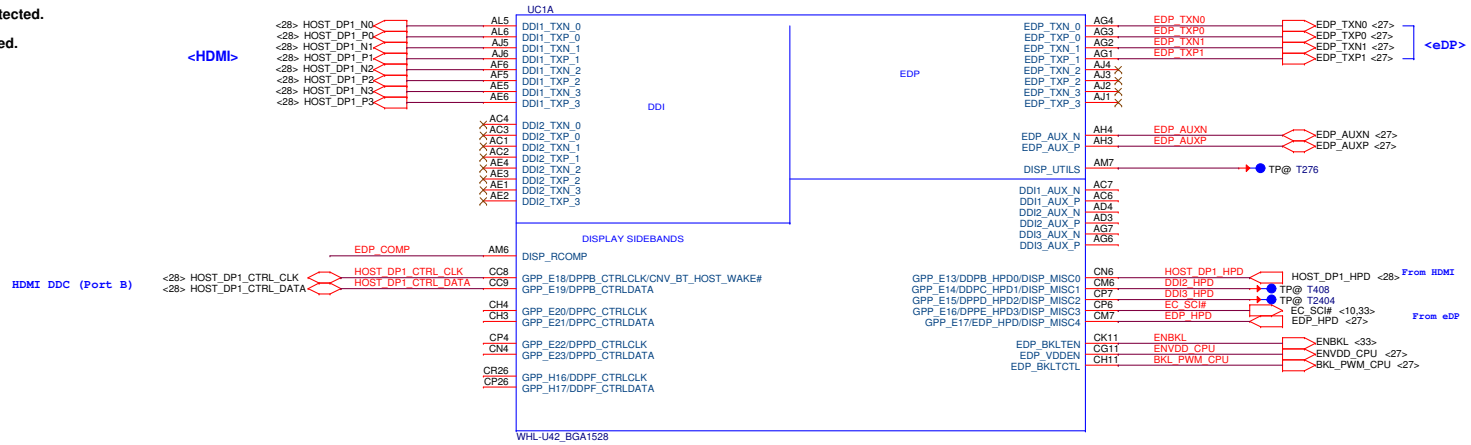


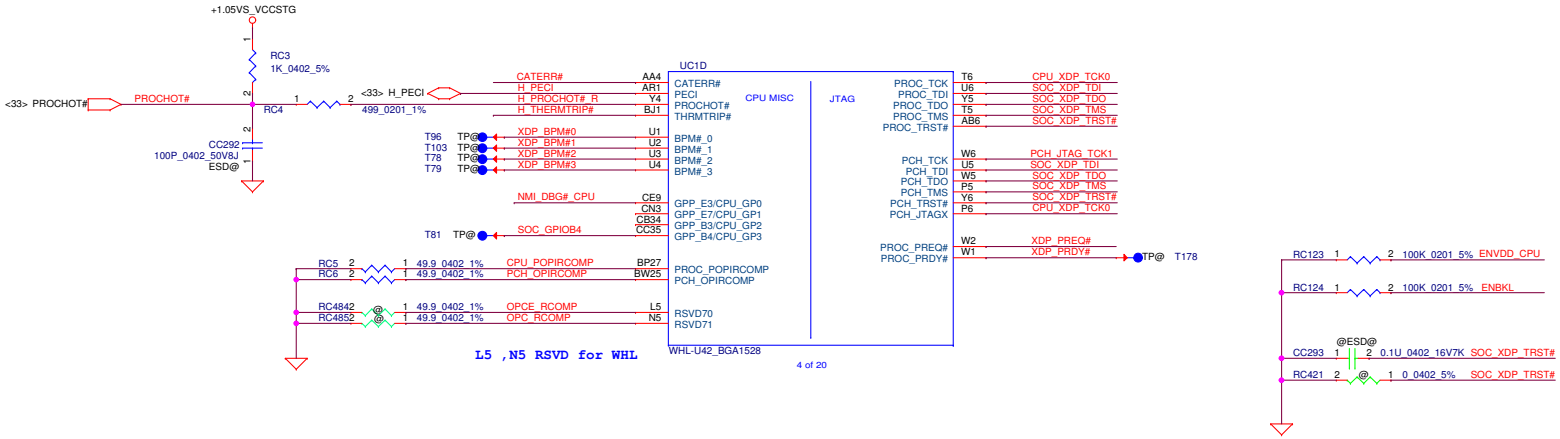












Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: **WHL-U(1/12))DDI,MSIC,XDP,EDP**

Size: Custom | Document Number: LA-H323P | Rev: V0.1

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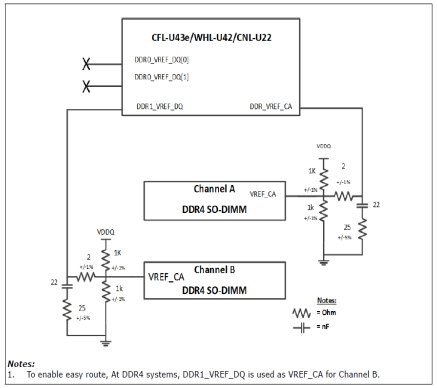
Interleaved Memory

Interleaved Memory

Figure 4-1. WHL U DDR4 SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

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			Date: Thursday, November 15, 2018 / Sheet 6 of 59

SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

<5,8,9,11,13,17,18,87> +3V_PRIM → +3V_PRIM
<6,9,10,11,17,18,19,22,23,24,27,28,29,31,32,33,35,36,40,41,88,94> +3VS → +3VS
<13> +3V_SPI → +3V_SPI

UC1E

<35> HOST_SPI_0_CLK
<35> HOST_SPI_0_SO
<35> HOST_SPI_0_SI
HOST_SPI_0_CS0# RC1160 1 2 49.9_0402_1%
<35> HOST_SPI_0_CS2#

HOST_SPI_0_CLK CH37
HOST_SPI_0_SO CF37
HOST_SPI_0_SI CF36
HOST_SPI_0_SIO2 CF34
HOST_SPI_0_SIO3 CG34
HOST_SPI_0_CS0#_R CG36
CG35
HOST_SPI_0_CS2# CH34

SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
SPI - FLASH

CF20
CG22
CF22
CG23
CH23
CG20

GPP_D1/SPI1_CLK/BK1/SBK1
GPP_D2/SPI1_MISO_IO1/BK2/SBK2
GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS0#/BK0/SBK0
SPI - TOUCH

T327 TP@ CL_CK_R CH7
T328 TP@ CL_DATA_R CH8
T329 TP@ CL_RST_N_R CH9

CL_CLK
CL_DATA
CL_RST#
C LINK

To TPM
<33> EC_KBRST# EC_KBRST# BV29
<33,35> SERIRQ SERIRQ BV28

GPP_A0/RCIN#/TIME_SYNC1
GPP_A6/SERIRQ

LPC Mode

WHL-U42_BGA1528

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SMBUS , SMLINK

GPP_C0/SMBCLK CK14 SMBCLK
GPP_C1/SMBDATA CH15 SMBDATA
GPP_C2/SMBALERT# CJ15 SMBALERT#
SMBALERT# <34>

Touch Pad

GPP_C3/SML0CLK CH14 SML0CLK
GPP_C4/SML0DATA CF15 SML0DATA
GPP_C5/SML0ALERT# CG15 SML0ALERT#
TP@ T305

GPP_C6/SML1CLK CN15 SML1CLK
GPP_C7/SML1DATA CM15 SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# CC34 SML1ALERT#
TP@ T90

LPC , ESPI

GPP_A1/LAD0/ESPI_IO0 CA29 LPC_AD0
GPP_A2/LAD1/ESPI_IO1 BY29 LPC_AD1
GPP_A3/LAD2/ESPI_IO2 BY27 LPC_AD2
GPP_A4/LAD3/ESPI_IO3 BV27 LPC_AD3
GPP_A5/LFRAME#/ESPI_CS# CA28 LPC_FRAME#
GPP_A14/SUS_STAT#/ESPI_RESET# CA27

LPC_AD0 <33>
LPC_AD1 <33>
LPC_AD2 <33>
LPC_AD3 <33>
LPC_FRAME# <33>

GPP_A9/CLKOUT_LPC0/ESPI_CLK BV32 CLK_PCI0 RC457 1 EMI@ 2 33_0402_5%
GPP_A10/CLKOUT_LPC1 BV30
GPP_A8/CLKRUN# BV30 PM_CLKRUN#
PM_CLKRUN# <33>

CLK_PCI_LPC <33>

EMI@ CC256 22P 50V J NPO 0402

+3V_PRIM
SMBALERT# RC380 1 2 10K_0201_5%
SML1ALERT# RC379 1 2 150K_0201_5%
SML0ALERT# RC360 1 @ 2 10K_0201_5%
RC218 1 @ 2 1K_0201_5%

+3VS
EC_KBRST# RC381 1 2 10K_0201_5%

+3V_PRIM
SML0CLK RC49 1 2 499_0201_1%
SML0DATA RC50 1 2 499_0201_1%
SML1CLK RC467 1 2 1K_0201_5%
SML1DATA RC468 1 2 1K_0201_5%
SMBDATA RC469 1 2 1K_0201_5%
SMBCLK RC470 1 2 1K_0201_5%
I2C0_SDA_TP RC1159 1 TPI2C@ 2 1K_0201_5%
I2C0_SCL_TP RC1158 1 TPI2C@ 2 1K_0201_5%

+3VS +3VS
RC216 10K_0402_5% RC215 10K_0402_5%
QC1
SMBCLK 6 1
SMBDATA 3 4
QC1 5
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
PCH_SMBCLK <17,18>
PCH_SMBDATA <17,18>

<10> I2C0_SCL_TP
<10> I2C0_SDA_TP
SMBCLK
SMBDATA
TPI2C@ R52651 2 0_0201_5%
TPSMB@ R52661 2 0_0201_5%
TPSMB@ R52671 2 0_0201_5%
TPI2C@ R52681 2 0_0201_5%

+3V_PRIM +3VALW
@ RC81 10K_0402_5%
@ RC82 10K_0402_5%
@ QC7 SB00001FF00 L2N7002SDW1T1G 2N SC88-6
TP_SMBCLK <34>
TP_SMBDATA <34>
R5271 1 2 0_0201_5%
R5272 1 2 0_0201_5%

Close to UC2

Single SPI ROM_CS0#

From CPU
HOST_SPI_0_SIO3 RC942 1 2 49.9_0402_1% HOST_SPI_0_HOLD#
HOST_SPI_0_SI RC943 1 2 49.9_0402_1% HOST_SPI_0_SI_R
HOST_SPI_0_SIO2 RC944 1 2 49.9_0402_1% HOST_SPI_0_WP#
HOST_SPI_0_SO RC945 1 2 49.9_0402_1% HOST_SPI_0_SO_R
To SPI ROM

SPI0 2 load with EC Flash sharing topology:
R1 is required 50 ohm for 3.3V and 15 ohm for 1.8V

From EC
(For share ROM)
<33> EC_SPI_SO EC_SPI_SO RC946 1 2 49.9_0402_1% HOST_SPI_0_SO_R
<33> EC_SPI_SI EC_SPI_SI RC947 1 2 49.9_0402_1% HOST_SPI_0_SI_R
<33> EC_SPI_CS0# EC_SPI_CS0# RC948 1 2 49.9_0402_1% HOST_SPI_0_CS0#
<33> HOST_SPI_0_CLK_R HOST_SPI_0_CLK_R 2 EMI@ 1 49.9_0402_1% HOST_SPI_0_CLK
CC295 10P_0402_50V8J @EMI@
RC456

+3V_SPI
HOST_SPI_0_SI RC941 1 2 100K_0201_5%
HOST_SPI_0_SIO2 RC383 1 2 100K_0201_5%
HOST_SPI_0_SIO3 RC384 1 2 100K_0201_5%
HOST_SPI_0_CS0# RC357 1 2 1K_0201_5%

For EC Auto Load Code

HOST_SPI_0_SIO3 RC51 1 @ 2 1K_0201_5%
HOST_SPI_0_CLK RC986 1 @ 2 100K_0201_5%

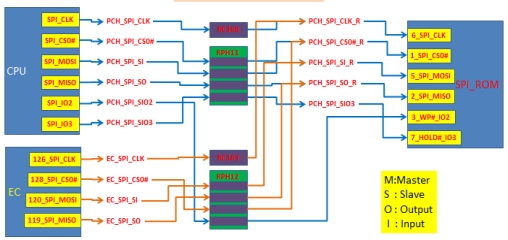
+3VS
PM_CLKRUN# RC107 1 2 8.2K_0201_5%
SERIRQ RC122 1 2 8.2K_0201_5%

+3V_SPI
CC8 1 2 0.1U_0201_10V6K

UC2
HOST_SPI_0_CS0# 1 CS# VCC 8
HOST_SPI_0_SO_R 2 DO(IO1) HOLD#(IO3) 7 HOST_SPI_0_HOLD#
HOST_SPI_0_WP# 3 WP#(IO2) CLK 6 HOST_SPI_0_CLK_R
4 GND DI(IO0) 5 HOST_SPI_0_SI_R
W25Q128JVSIQ SOP 8P
SA00005VV20
ACES_91960-0084L_8P-T
Use socket footprint

HOST_SPI_0_CS0#
@ CC9 68P_0201_25V8

ENE Fixed Code Block Diagram



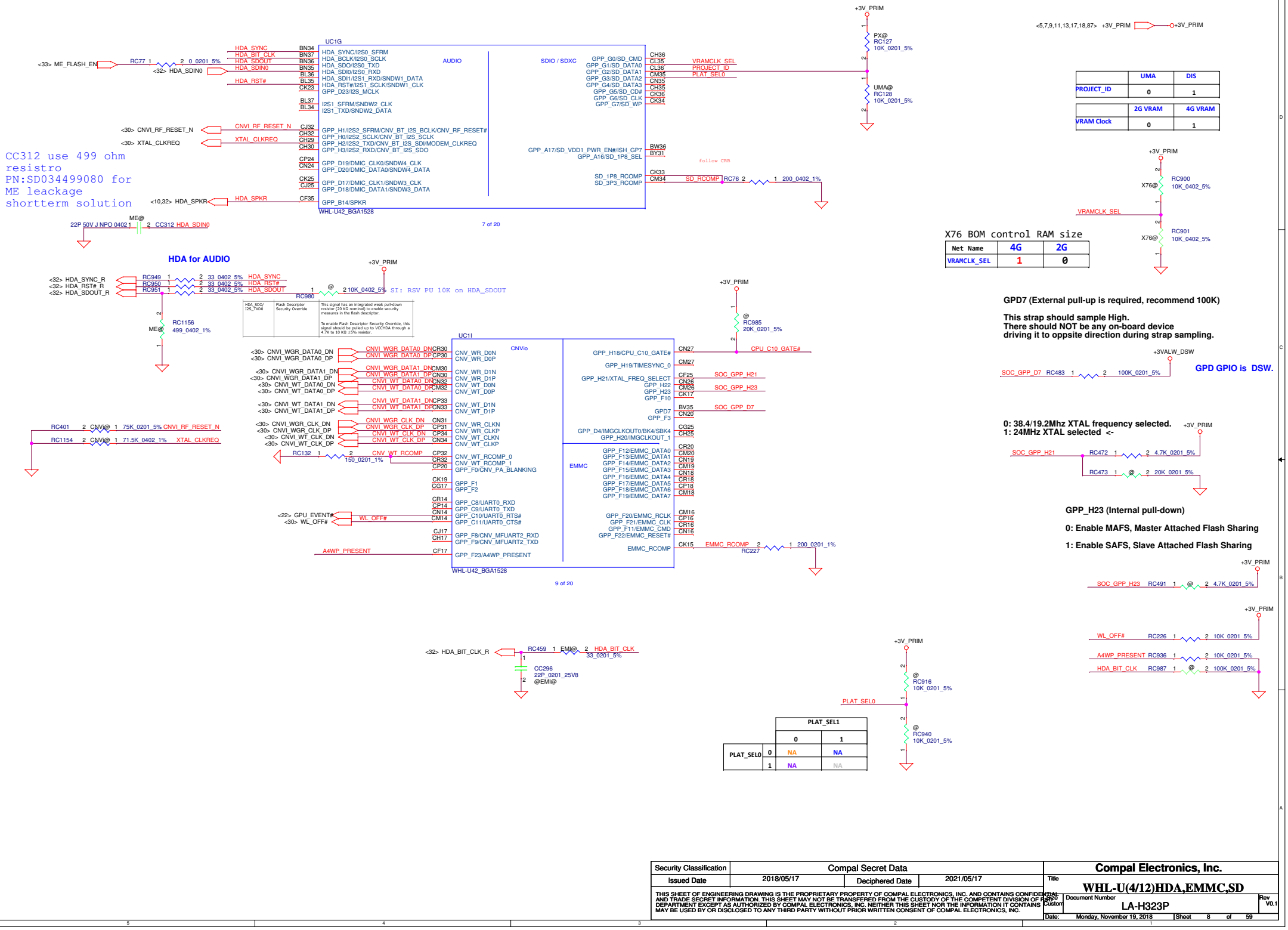
Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: **WHL-U(3/12)SPI,ESPI,SMB,LPC**

Size: Custom | Document Number: LA-H323P | Rev: V0.1

Date: Monday, November 19, 2018 | Sheet 7 of 59


UC1G
AUDIO
HDA_SYNC/I2S0_SFRM
HDA_BCLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST#/I2S1_SCLK/SNDW1_CLK
GPP_D23/I2S_MCLK
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_B14/SPKR
SDIO / SDXC
GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_1P8_RCOMP
SD_3P3_RCOMP
WHL-U42_BGA1528
7 of 20
CC312 use 499 ohm resistro PN:SD034499080 for ME leackage shortterm solution
HDA for AUDIO
UC1I
CNVio
CNV_WR_D0N
CNV_WR_D0P
CNV_WR_D1N
CNV_WR_D1P
CNV_WT_D0N
CNV_WT_D0P
CNV_WT_D1N
CNV_WT_D1P
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WT_CLKN
CNV_WT_CLKP
CNV_WT_RCOMP_0
CNV_WT_RCOMP_1
GPP_F0/CNV_PA_BLANKING
GPP_F1
GPP_F2
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_F8/CNV_MFUART2_RXD
GPP_F9/CNV_MFUART2_TXD
GPP_F23/A4WP_PRESENT
GPP_H18/CPU_C10_GATE#
GPP_H19/TIMESYNC_0
GPP_H21/XTAL_FREQ_SELECT
GPP_H22
GPP_H23
GPP_F10
GPD7
GPP_F3
GPP_D4/IMGCLKOUT0/BK4/SBK4
GPP_H20/IMGCLKOUT_1
EMMC
GPP_F12/EMMC_DATA0
GPP_F13/EMMC_DATA1
GPP_F14/EMMC_DATA2
GPP_F15/EMMC_DATA3
GPP_F16/EMMC_DATA4
GPP_F17/EMMC_DATA5
GPP_F18/EMMC_DATA6
GPP_F19/EMMC_DATA7
GPP_F20/EMMC_RCLK
GPP_F21/EMMC_CLK
GPP_F11/EMMC_CMD
GPP_F22/EMMC_RESET#
EMMC_RCOMP
WHL-U42_BGA1528
9 of 20
X76 BOM control RAM size
Net Name | 4G | 2G
VRAMCLK_SEL | 1 | 0
PROJECT_ID | 0 | 1
VRAM Clock | 0 | 1
GPD7 (External pull-up is required, recommend 100K)
This strap should sample High.
There should NOT be any on-board device driving it to oppsite direction during strap sampling.
GPD GPIO is DSW.
0: 38.4/19.2Mhz XTAL frequency selected.
1: 24MHz XTAL selected <-
GPP_H23 (Internal pull-down)
0: Enable MAFS, Master Attached Flash Sharing
1: Enable SAFS, Slave Attached Flash Sharing
PLAT_SEL1
PLAT_SEL0
Security Classification | Compal Secret Data
Issued Date | 2018/05/17 | Deciphered Date | 2021/05/17
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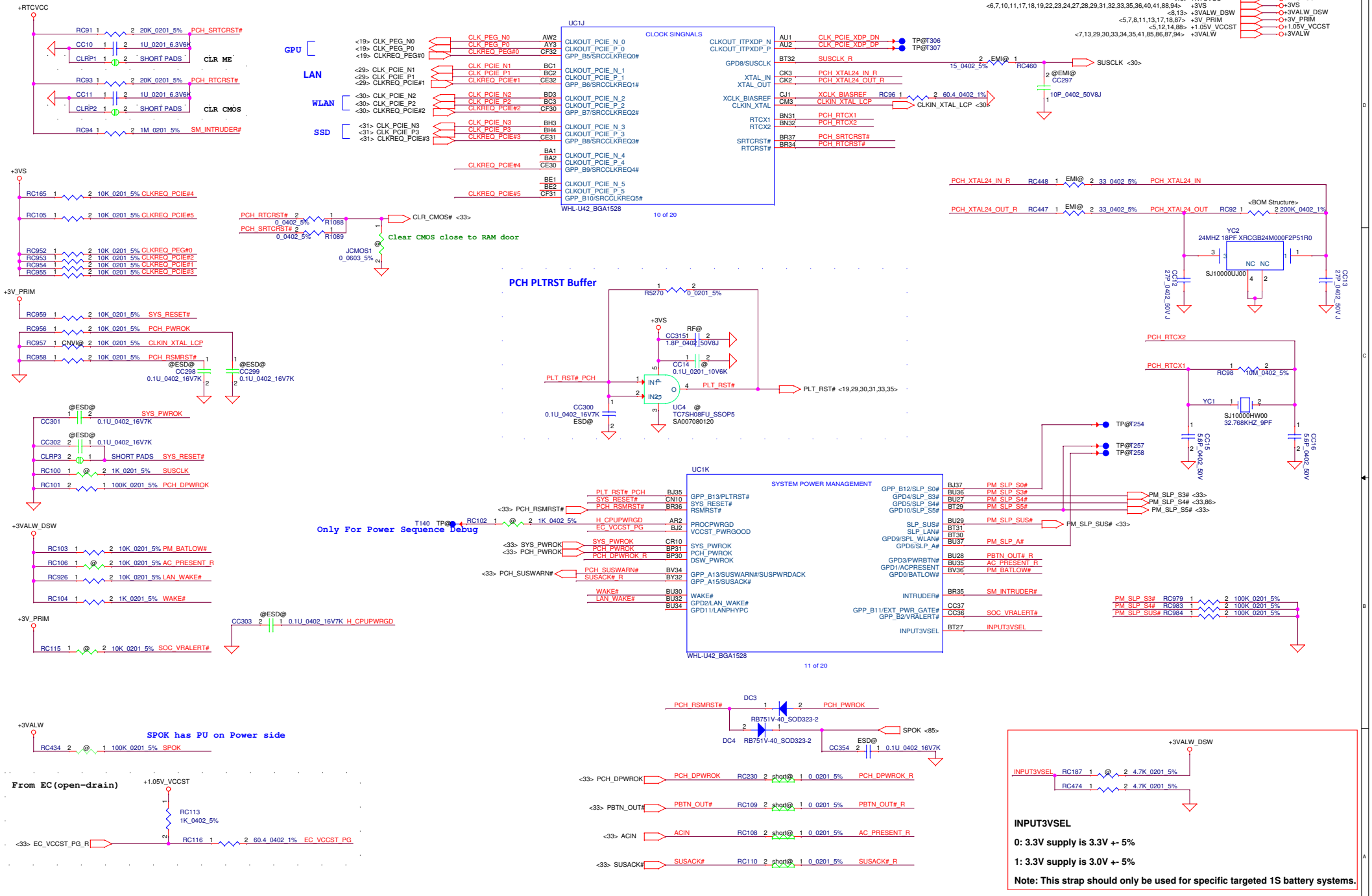
Title: WHL-U(4/12)HDA,EMMC,SD
Size: Custom | Document Number: LA-H323P | Rev: V0.1
Date: Monday, November 19, 2018 | Sheet 8 of 59



Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.			
Title	WHL-R(5/12)CLK,GPIO		
Size: Custom	Document Number: LA-H323P		Rev: V0.1
Date: Monday, November 19, 2018	Sheet 9 of 59		

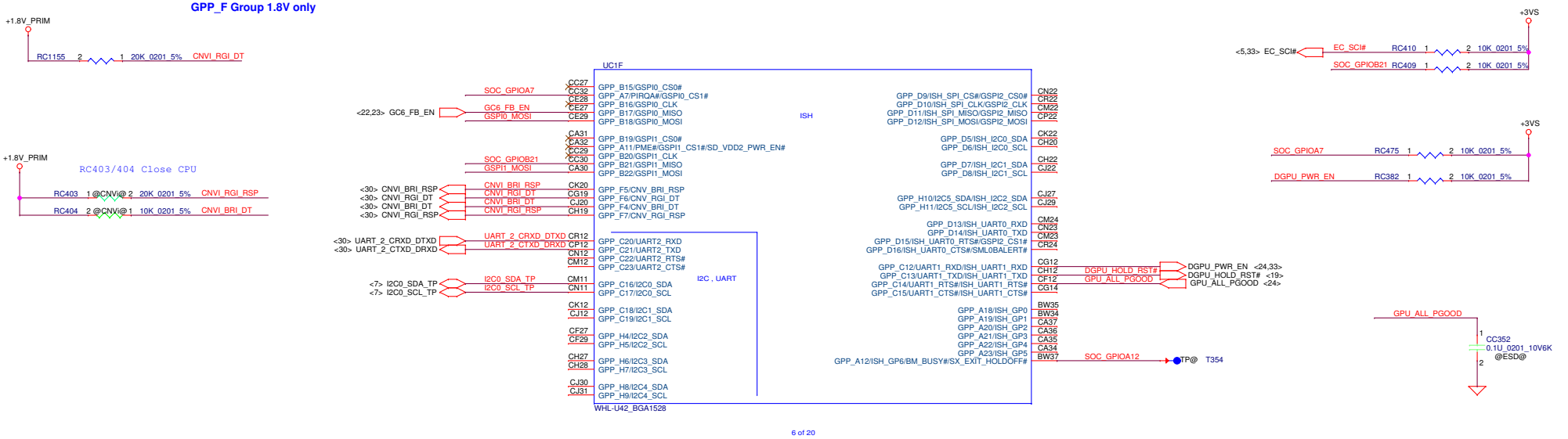
PCH EDS : M.2 CNV Mode Select

GPP_F6/CNV_RGI_DT

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.

GPP_F Group 1.8V only



Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> EPW30 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> EPW30 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

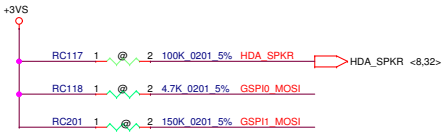
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

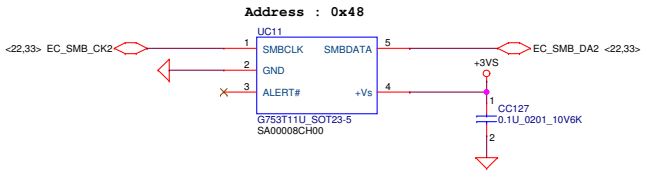
0 = SPI Mode --> EPW30 Use

1 = LPC Mode

Strap Pin

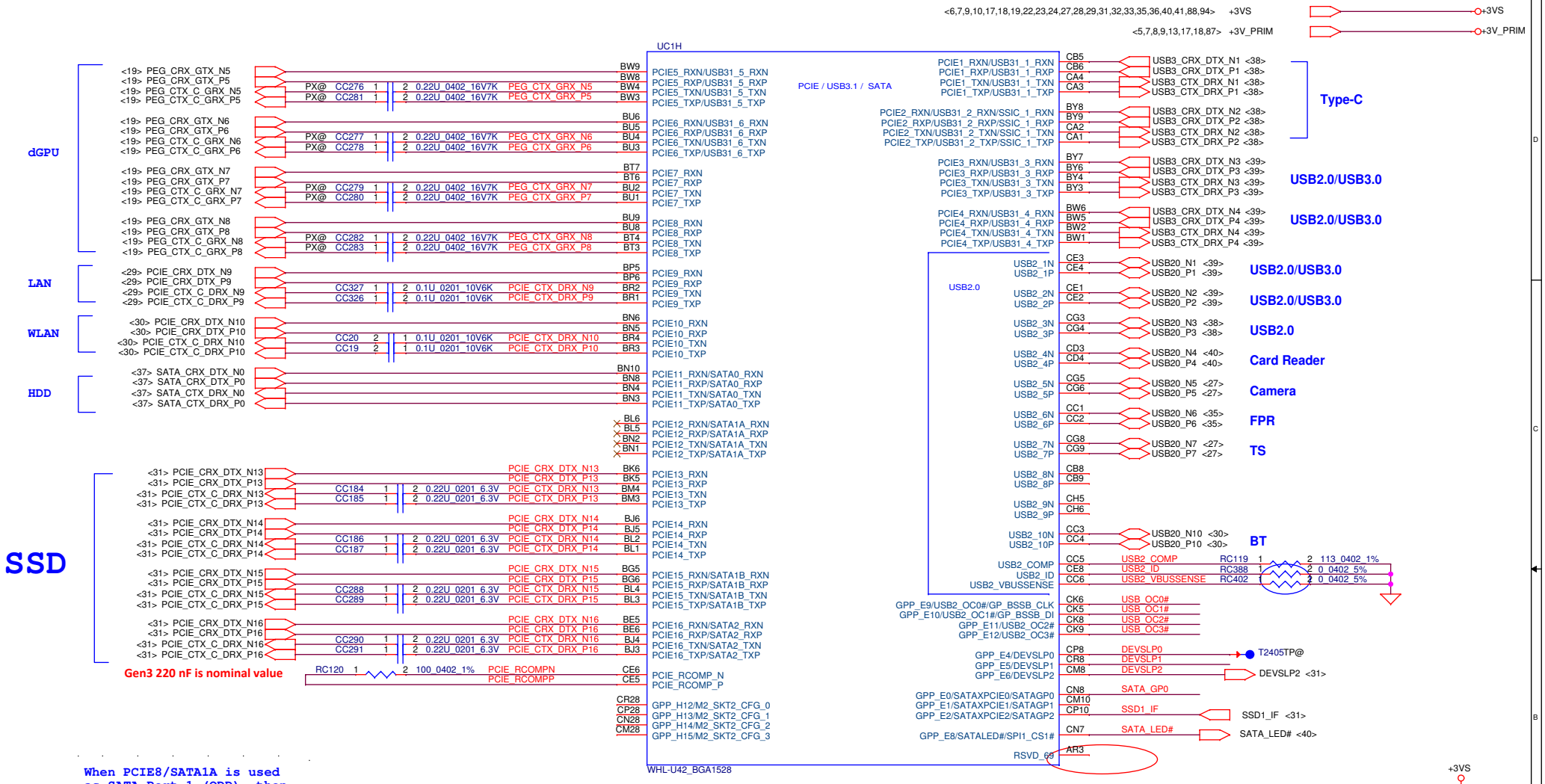


CPU THERMAL SENSOR



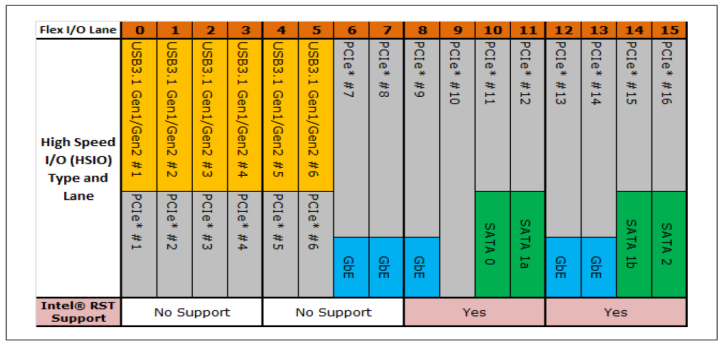
Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.			
Title	WHL-U(6/12)GPIO		
Size: Custom	Document Number: LA-H323P		Rev: V0.1
Date: Thursday, November 15, 2018	Sheet 10 of 59		



GPIO	DEVICE CONTROL
USB_OC0#	NA
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	M.2 SSD
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	SSD1_IF

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP



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Compal Electronics, Inc.

Title: WHL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: LA-H323P | Rev: V0.1

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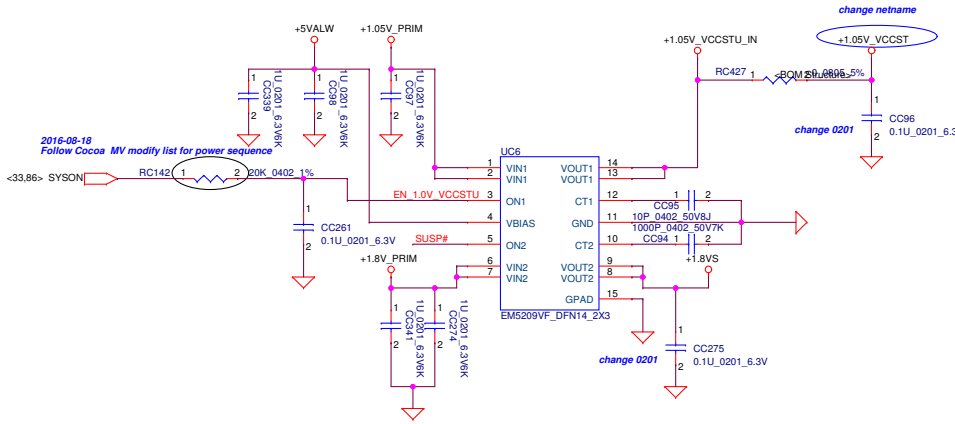
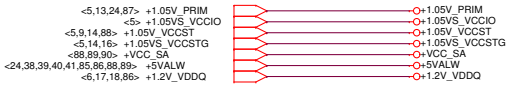
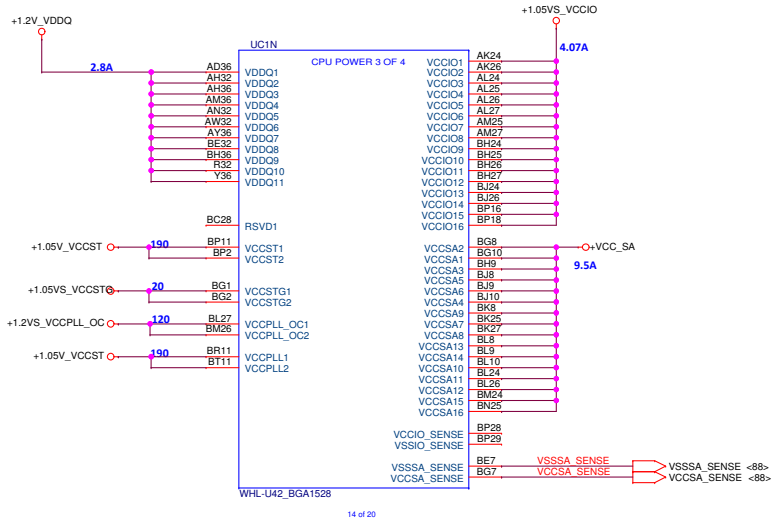
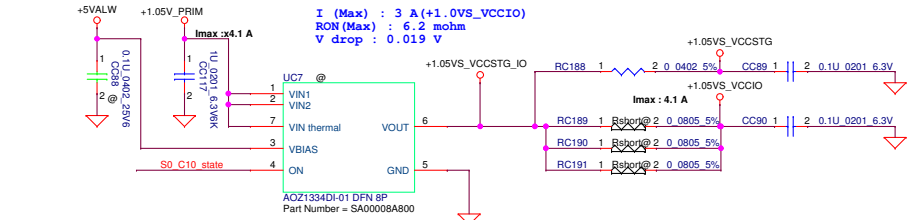
+1.05V_PRIM TO +1.05V_VCCST

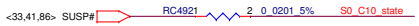






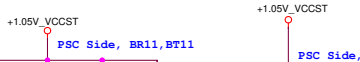
+1.05V_PRIM TO +1.05VS_VCCSTG / +1.05VS_VCCIO

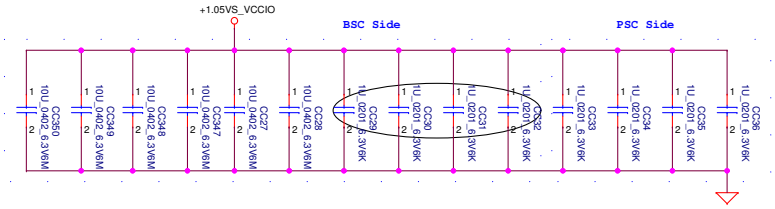




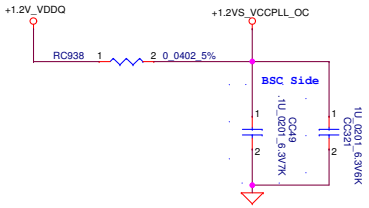
VccIO	**	V1.05A	15.5 mΩ	VccIO
VccST	SLP_S4#	V1.05A	55.3 mΩ	VccST/VccPLL
VccSTG	SLP_S3# && CPU_C10_GATE#	V1.05A	525.0 mΩ	VccSTG

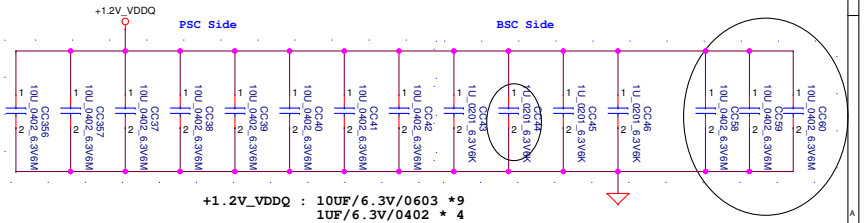
**Do not combine with VccSTG; 1.05V-10% allowed only on VCCIO; 5% additional Vdroop factored into LS RdsON





+1.2V_VDDQ TO +1.2VS_VCCPLL_OC





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Title	WHL-U(8/12)POWER
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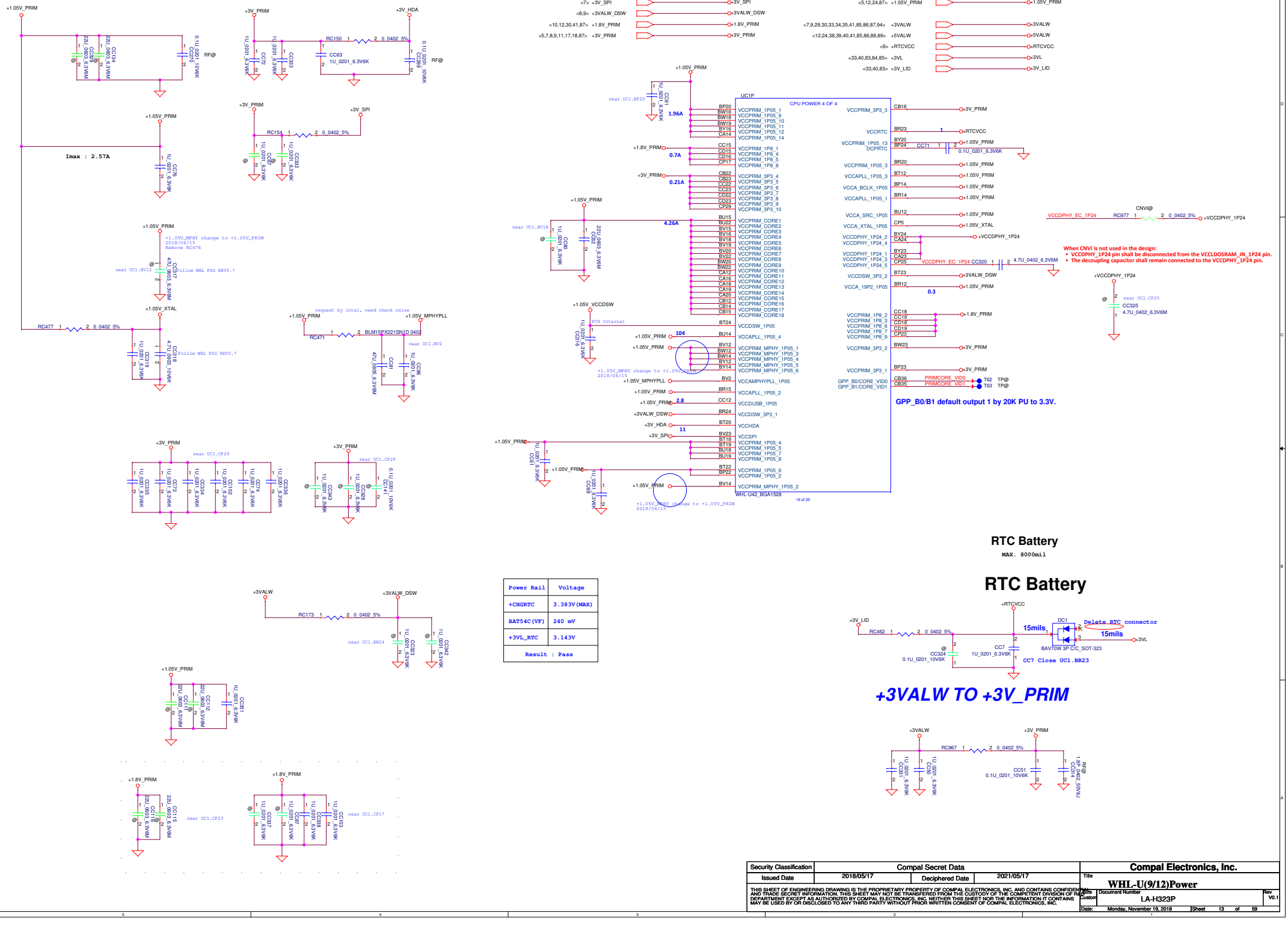

Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+3VL_RTC	3.143V
Result : Pass	

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Size Custom	Document Number LA-H323P		Rev V0.1
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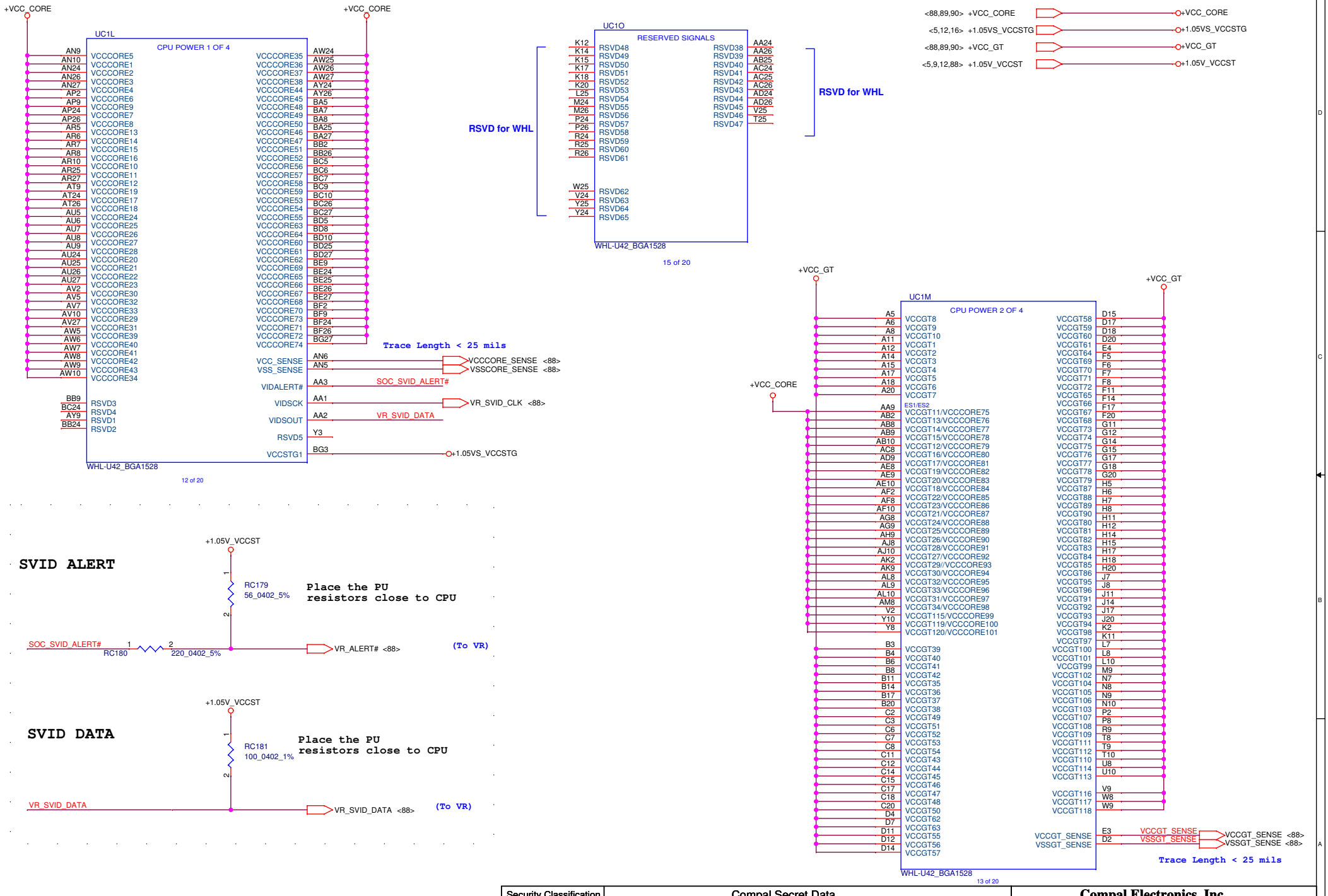

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: WHL-R(10/12)POWER,SVID

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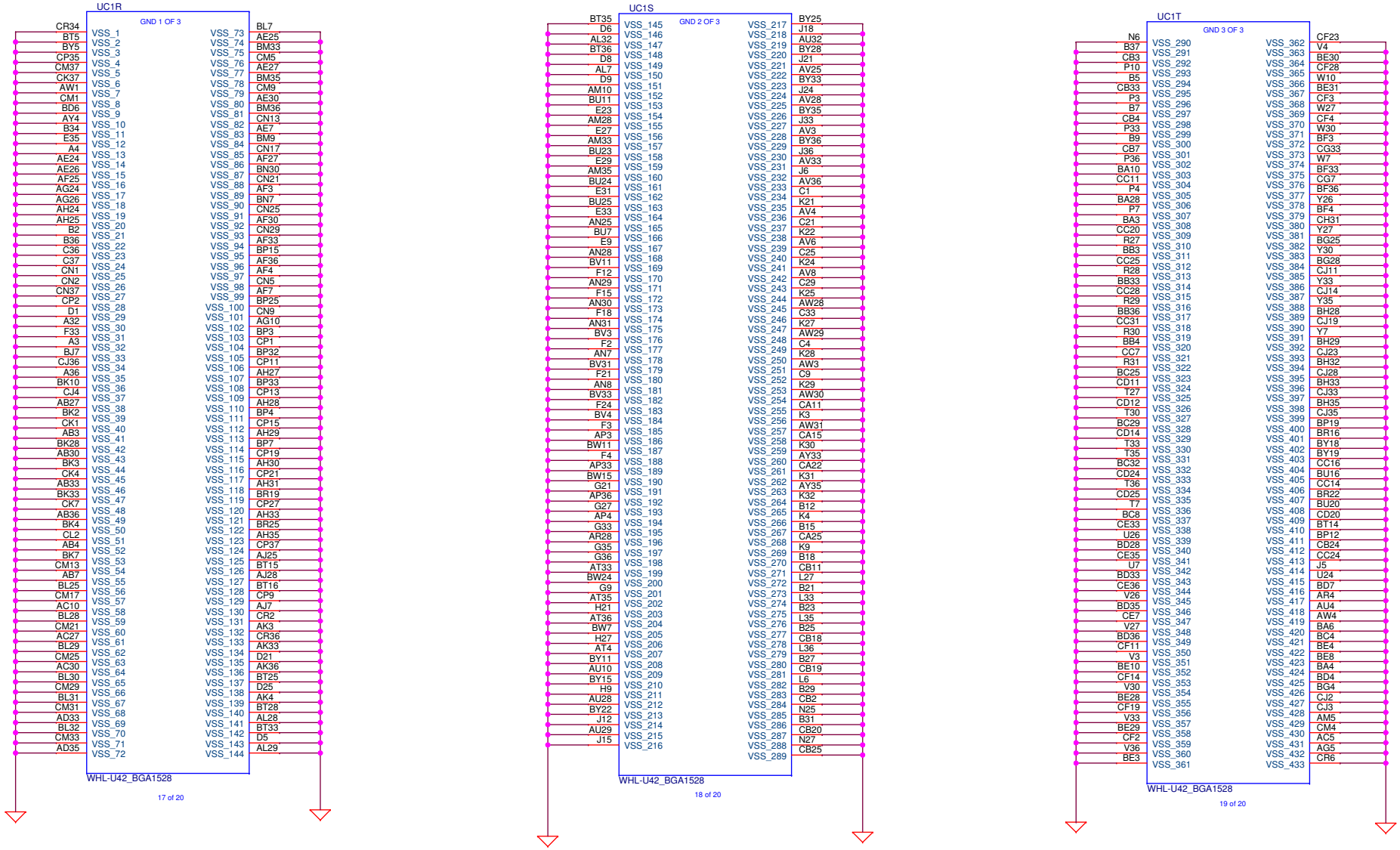

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Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: **WHL-U(11/12)GND**

Size: B | Document Number: LA-H323P | Rev: V0.1

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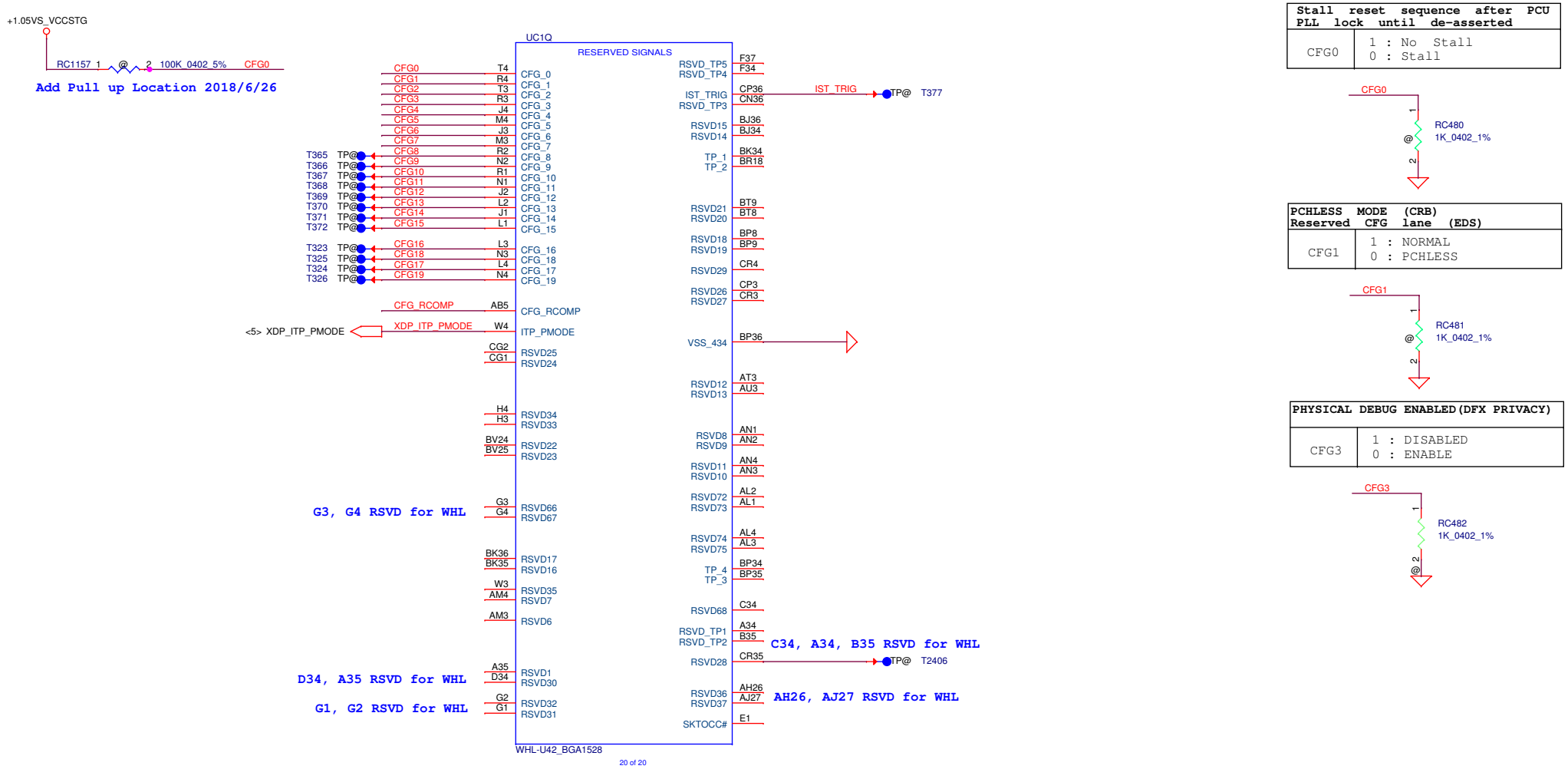

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Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: WHL-U(12/12)RSVD

Size: D | Document Number: LA-H323P | Rev: V0.1

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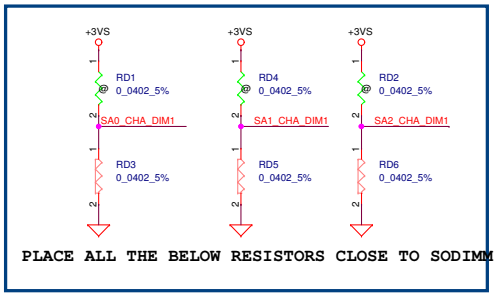
CHANNEL-A

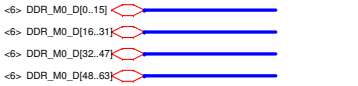
REVERSE TYPE

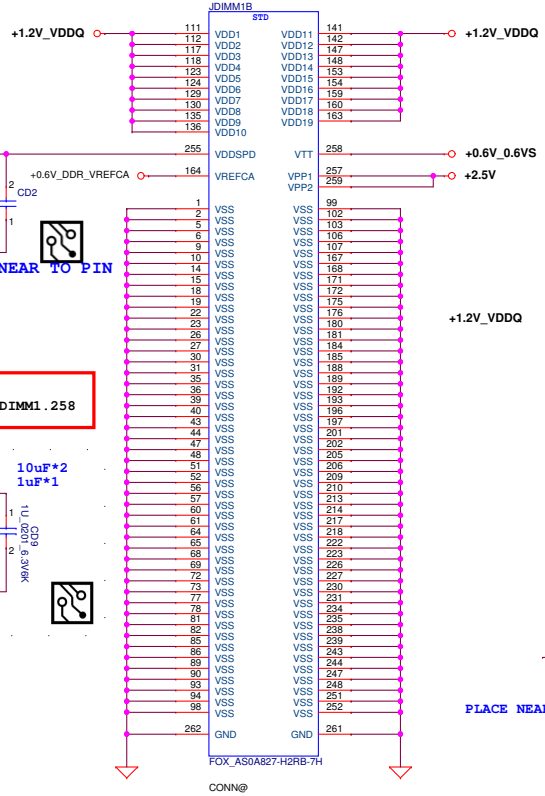
Interleaved Memory

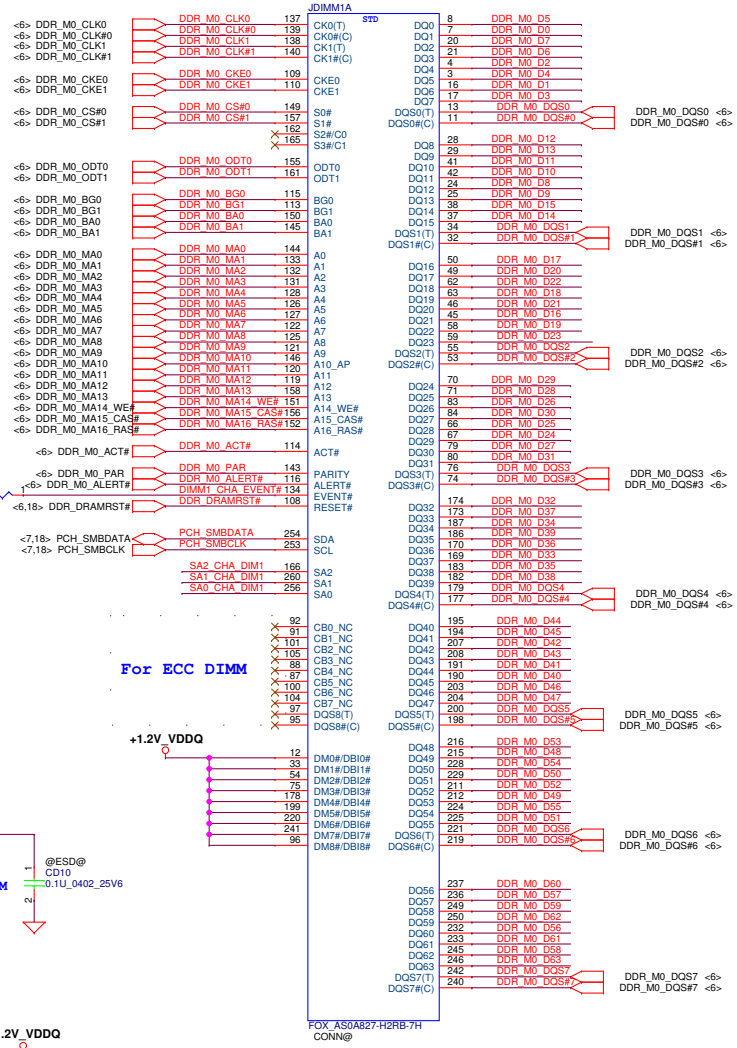
TOP: JDIMM1 CONN Non-ECC DIMM



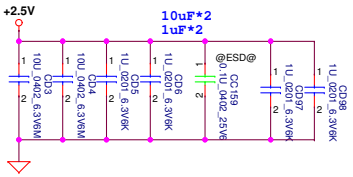
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



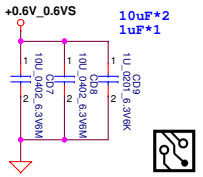




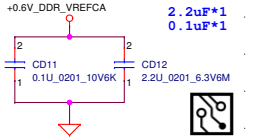
Layout Note:
Place near JDIMM1.257,259

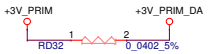


Layout Note:
Place near JDIMM1.258



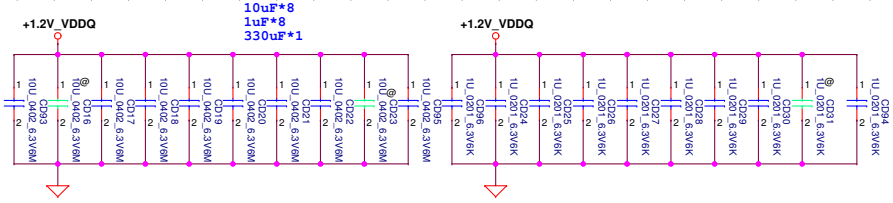
Layout Note:
PLACE THE CAP near JDIMM1. 164

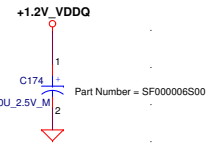


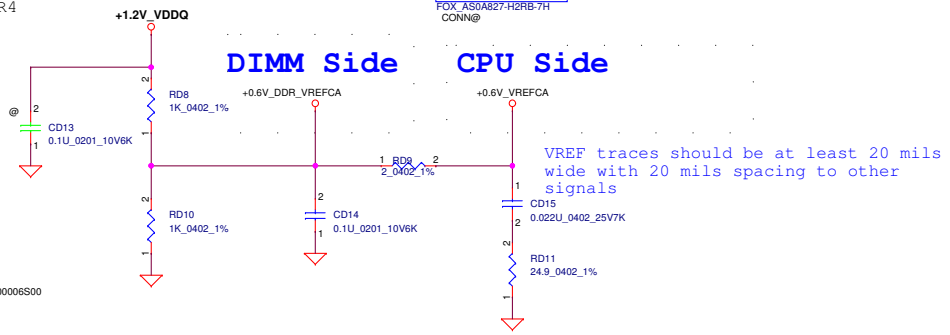


Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

Layout Note:
Place near JDIMM1







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Compal Electronics, Inc.	
Title	P18-DDRIV_CHA: DIMM0
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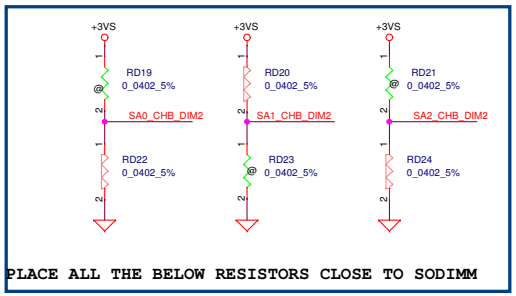
CHANNEL-B

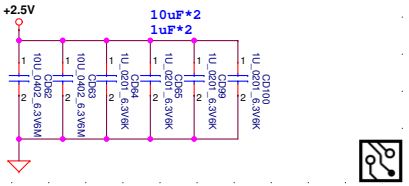
TOP: JDIMM2 CONN Non-ECC DIMM



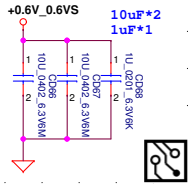
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

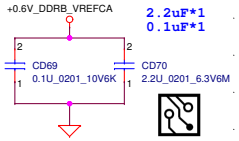
Layout Note:
Place near JDIMM2.257,259

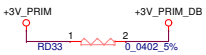


Layout Note:
Place near JDIMM2.258



Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2





Layout Note:
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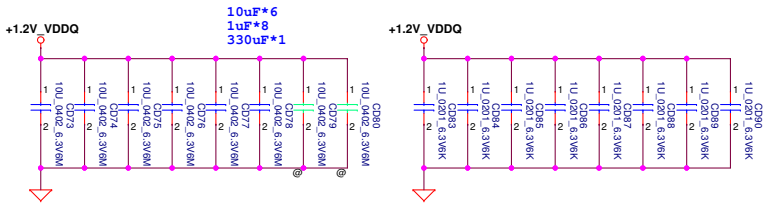
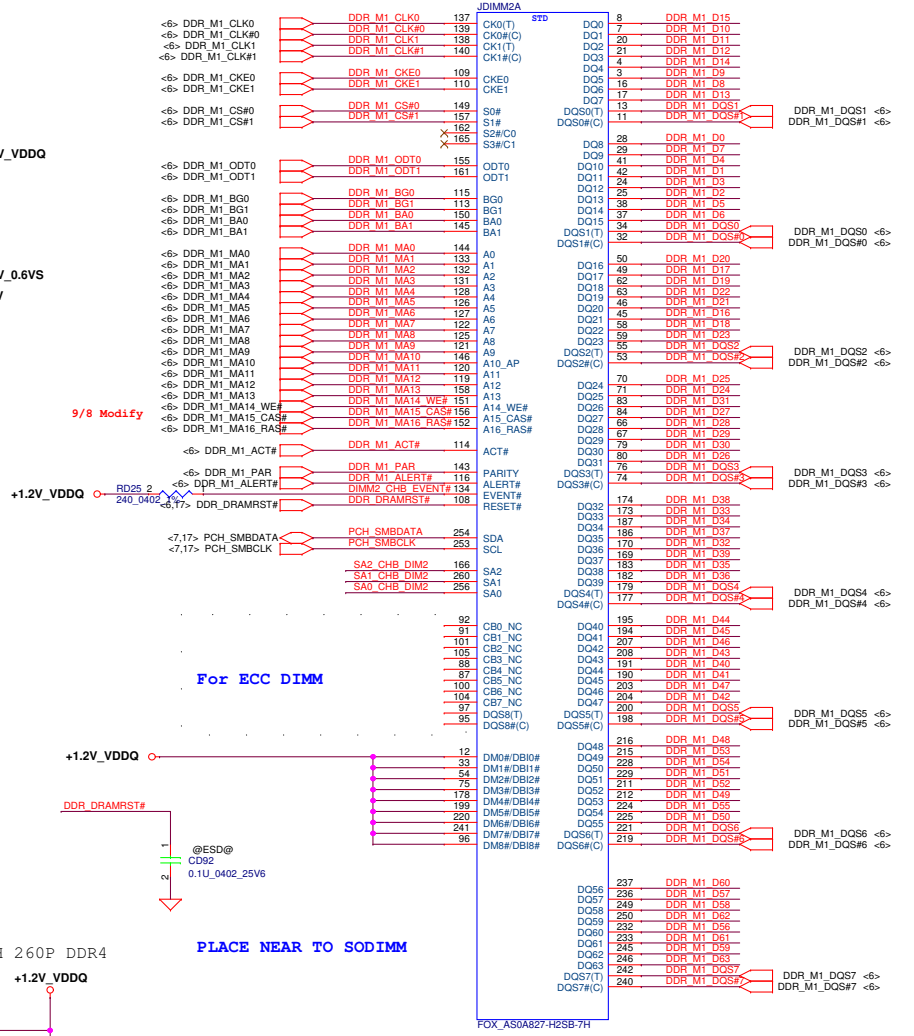
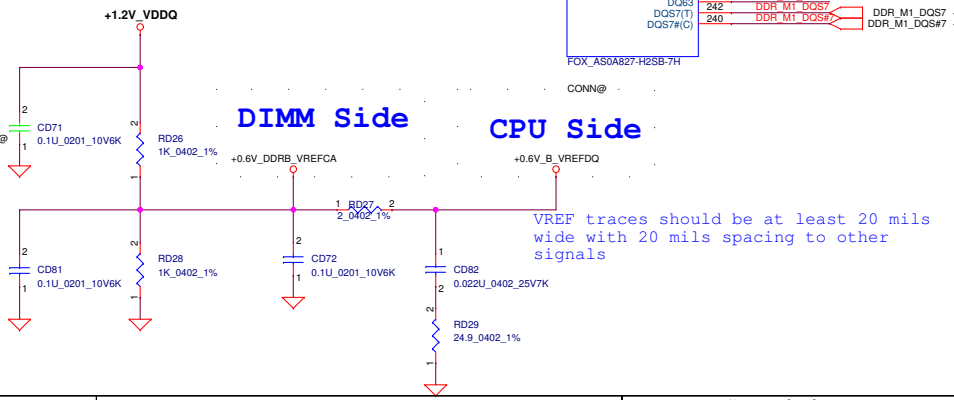


Interleaved Memory

Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4

STD (5.2 mm)





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Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: P19-DDRIV_CHB: DIMM0

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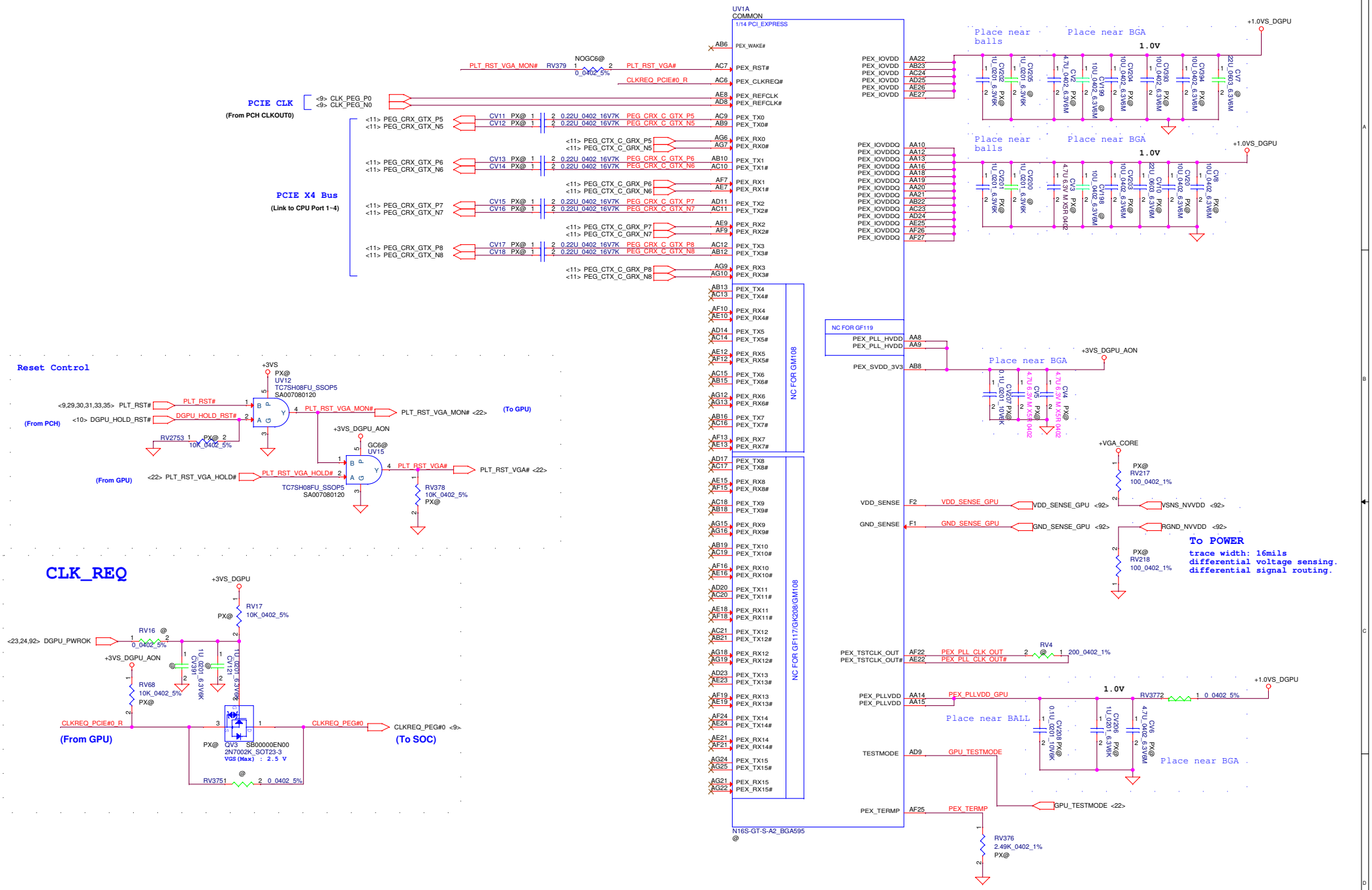

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.			
Title: NV(1/5)-PCIE			
Size: Custom	Document Number: LA-H323P		Rev: V0.1
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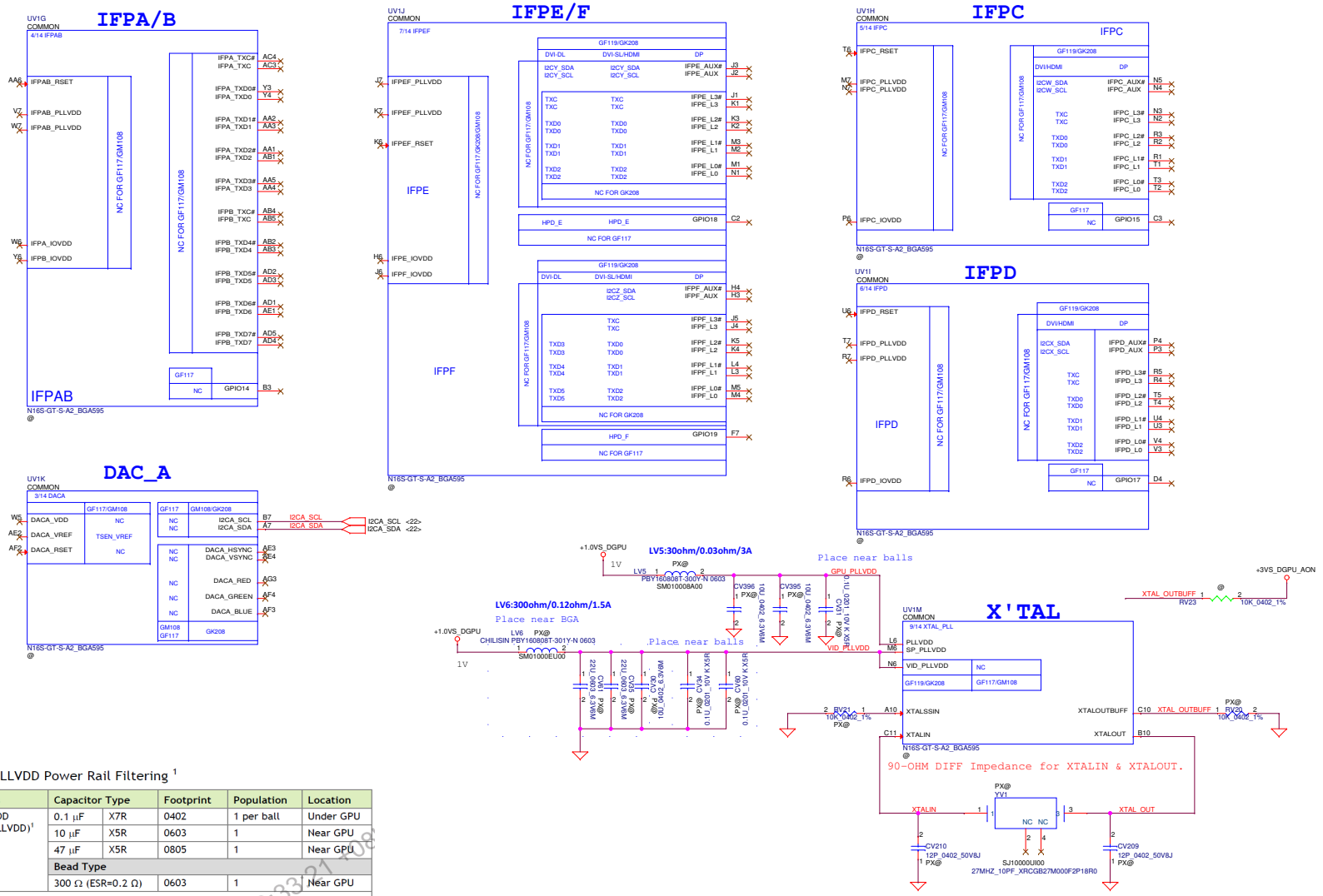

Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

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Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.	
Title	NV(2/5)-IFP_ABCDEF_DAC_XTAL
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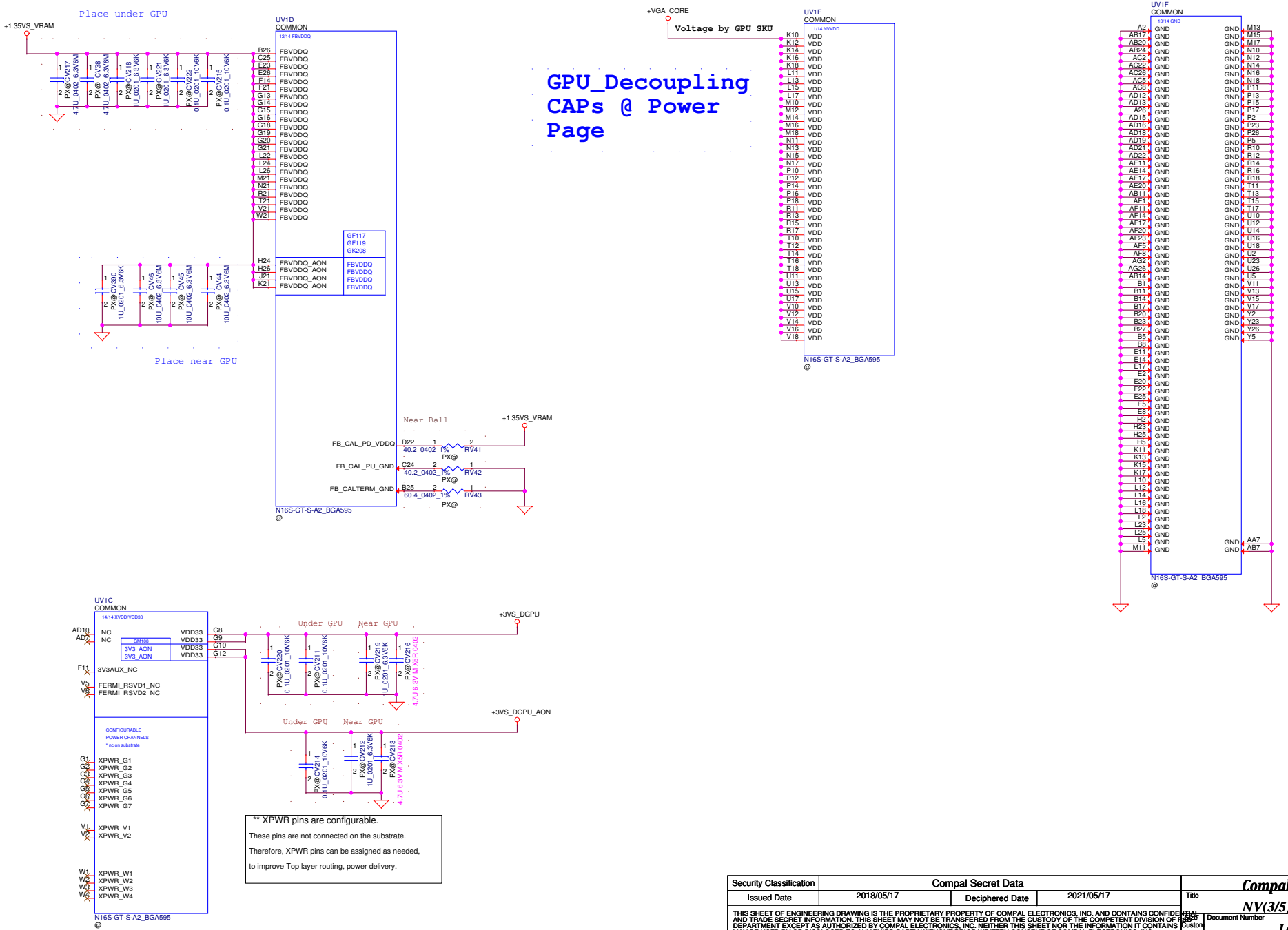
GPU_Decoupling CAPs @ Power Page



** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed,

to improve Top layer routing, power delivery.

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Issued Date	2018/05/17	Deciphered Date	2021/05/17

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Title: NV(3/5)-POWER

Size: Custom | Document Number: LA-H323P | Rev: V0.1

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VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

GPIO

I2CS SMBUS: 0x96 and 0x9E(Default)

For GC6 2.0

10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful FCS Slave addresses can be used with SMB_ALT_ADDR strapping.

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

Internal Thermal Sensor

Link to PCH SML1
PU @ PCH SIDE

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

+3VS Reserve for leakage issue

GPU side / EC side

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

STRAP

RV65 X76 BOM control

*2017-09-21:
Change RV64 to RV81 for MX130 strapping
2017-09-27:
Change RV81 from 10K to 4.99K for NV request

STRAP

STRAP0 : PU 49.9K (50K)
STRAP[1:5] : Reserved

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN		Pull-Down to GND	
4.99 kΩ	1000	0x08 M2G	0000	0x00
10.0 kΩ	1001	0x09 H2G	0001	0x01
15.0 kΩ	1010	0x0A	0010	0x02
20.0 kΩ	1011	0x0B	0011	0x03
24.9 kΩ	1100	0x0C	0100	0x04
30.1 kΩ	1101	0x0D	0101	0x05
34.8 kΩ	1110	0x0E	0110	0x06
45.3 kΩ	1111	0x0F	0111	0x07

N17S-G0/G2 GDDR5 Recommended Memories

Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade
Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps
Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009) M2G
L	M	H	10 (0x000A) H2G
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories

Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
Micron	MT51J256M32HF-80:B	B-die	0x8	3000	N/A	Substitution allowed with waiver²
Hynix	H5GC8H24AJR-R2C	A-die	0x9	3000	N/A	Substitution allowed with waiver²

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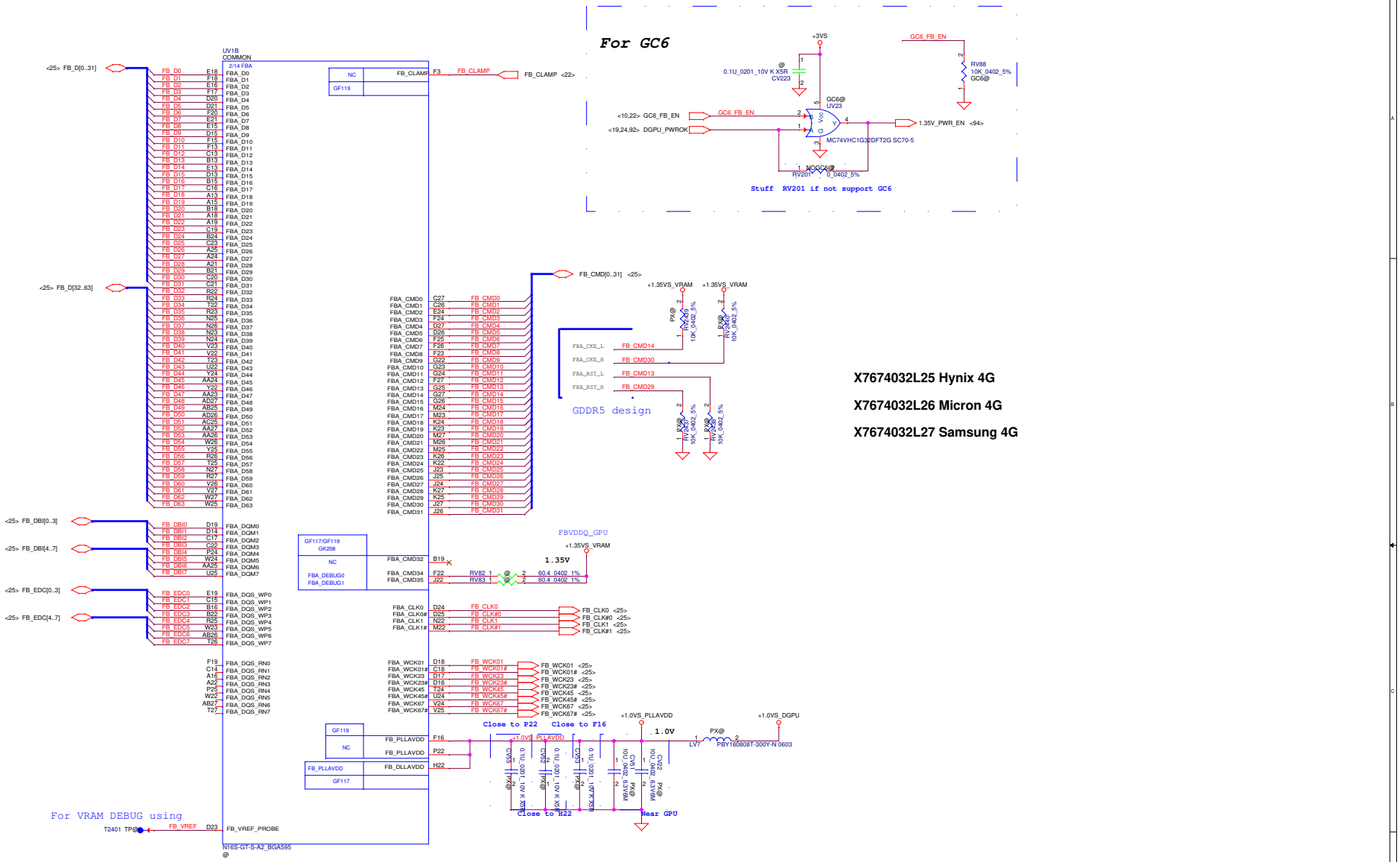

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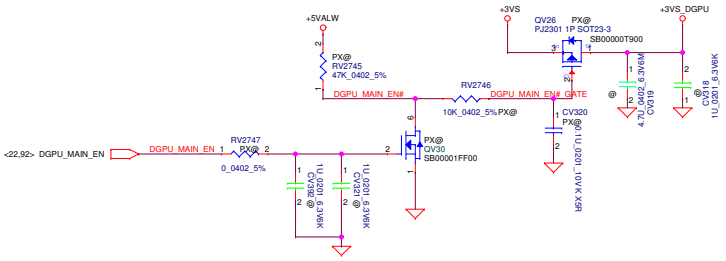
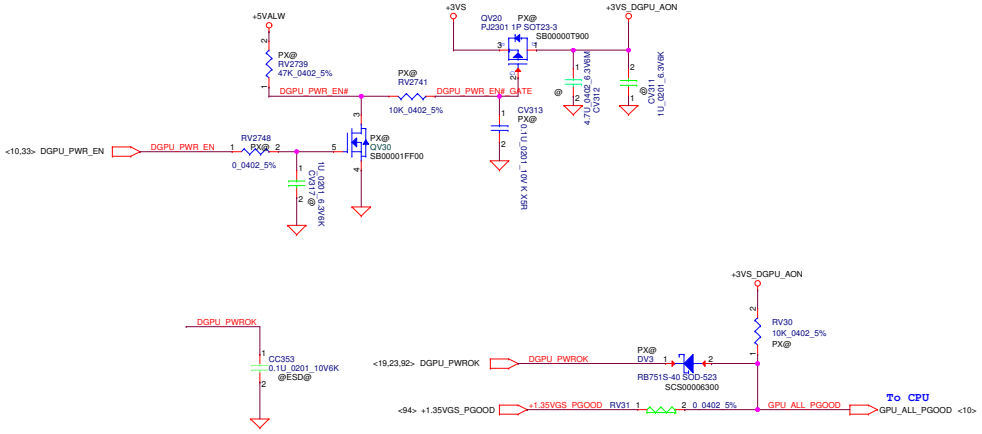
+3VS to +3VS_DGPU



+3VS to +3VS_DGPU_AON



Only For N16S-GT(GB2B-64)

+1.05V_PRIM to +1.0VS_DGPU

I_Continuous(Max) : 0.79 A(+1.0VS_DGPU)
RON(Max) : 22 mohm
V drop : 0.0175 V
Rising : ~ 208us

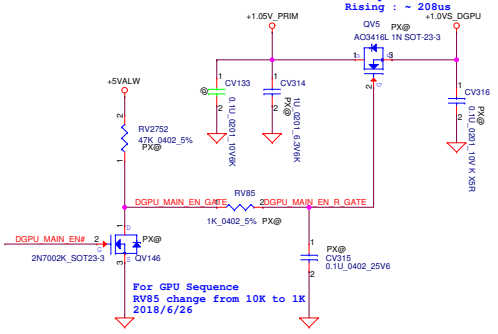


Table 5. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]	3.3V Total
		–	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5	26.5	–	2.0	–	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 3-15. PCI Express Power Rails Specification

GPU Package	Power Rails	Voltage	Transient Noise
GB2-64/ GB2B-64	PEX_IOVDD/Q and	1.05 V ± 30 mV or	100 mV pk-pk within 20 MHz (1.05V) or
	PEX_PLLVDD	1.0 V ± 15mV	70 mV pk-pk within 20 MHz (1.0V)

Table 3-7. Power Rail Specification for DDR3 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDDQ/FBVDD	1.5 V (DDR3) or 1.35V (DDR3L)
DC tolerance	± 3%
AC tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW

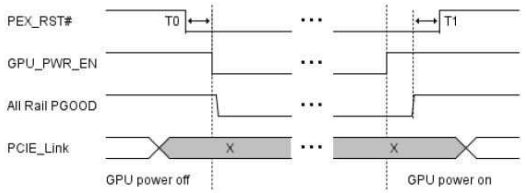
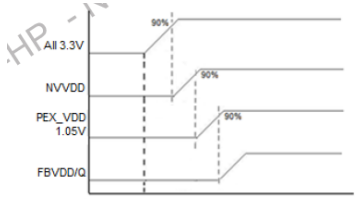


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

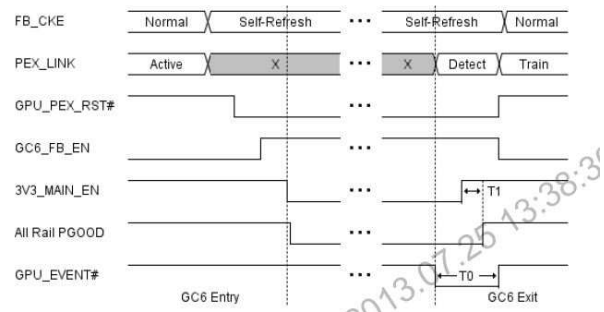


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

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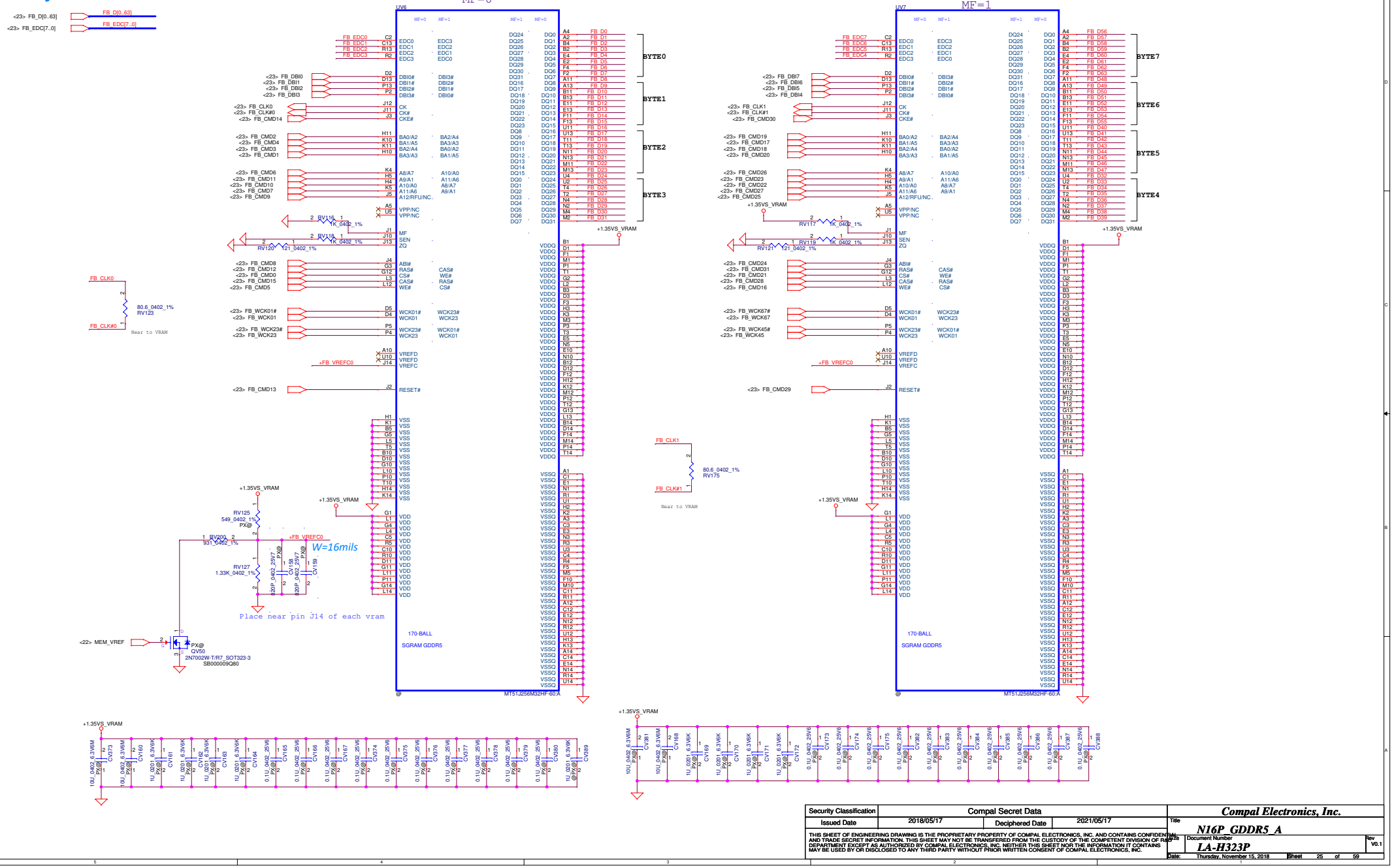
Memory Partition A



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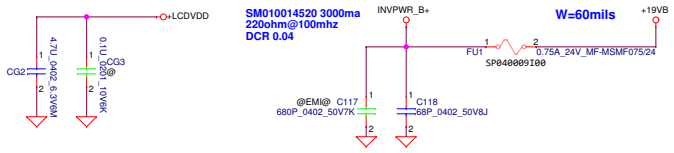
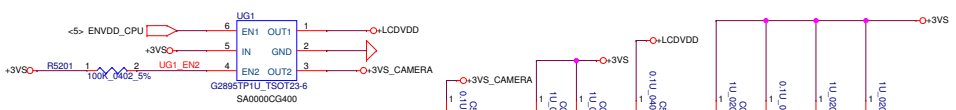
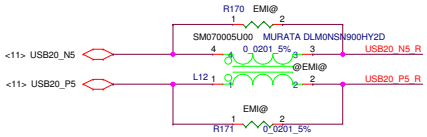
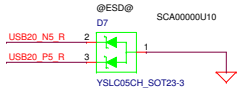
eDP Power

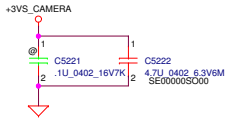


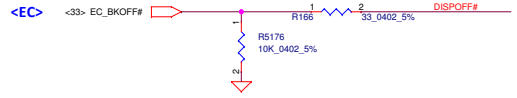


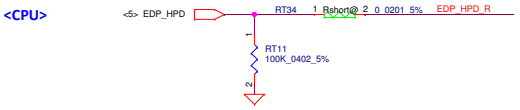
Camera

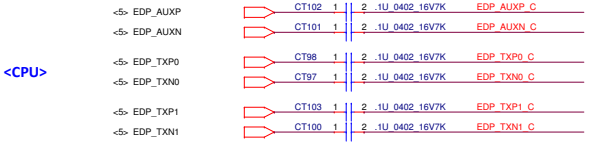


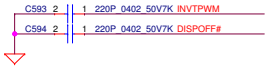




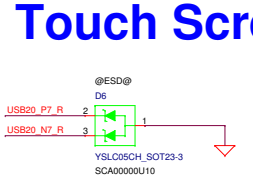


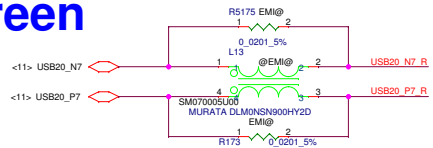


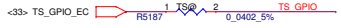




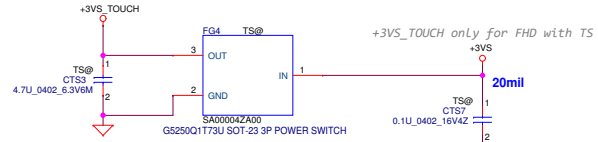
Touch Screen

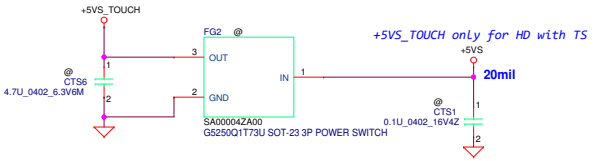




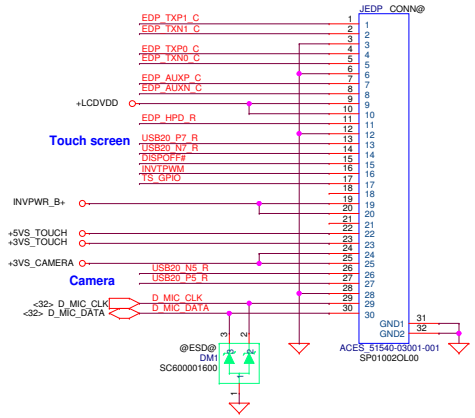


Touch Screen Power Selection:





eDP



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1.3.2 Digital Display Interface Signal Mapping

Table 1-4. Digital Display Interface Signal Mapping

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA

DDI_0 → HDMI_2; DDI_3 → CLK; DDI_1 → HDMI_0

<CPU>

<5> HOST_DP1_P0 / HOST_DP1_N0 → HOST_DP1_P0 / HOST_DP1_N0 0.1U_0402_16V7K → CG8 / CG9 → HDMI_TX_P2 / HDMI_TX_N2

<5> HOST_DP1_P1 / HOST_DP1_N1 → HOST_DP1_P1 / HOST_DP1_N1 0.1U_0402_16V7K → CG10 / CG11 → HDMI_TX_P1 / HDMI_TX_N1

<5> HOST_DP1_P2 / HOST_DP1_N2 → HOST_DP1_P2 / HOST_DP1_N2 0.1U_0402_16V7K → CG12 / CG13 → HDMI_TX_P0 / HDMI_TX_N0

<5> HOST_DP1_P3 / HOST_DP1_N3 → HOST_DP1_P3 / HOST_DP1_N3 0.1U_0402_16V7K → CG14 / CG15 → HDMI_CLKP / HDMI_CLKN

RG12 / RG13 / RG14 / RG15 / RG16 / RG17 / RG18 / RG19 470_0201_5%

QG1 SB00001FF00
L2N7002SDW1T1G 2N SC88-6

+3VS

<6,7,9,10,11,17,18,19,22,23,24,27,29,31,32,33,35,36,40,41,88,94> +3VS

<27,32,33,34,36,37,41,92> +5VS

+3VS

RG47 1M_0402_5%

<5> HOST_DP1_HPD → HDMI_HPD → RG108 10K_0402_5% → HP_DETECT

QG1 SB00001FF00
L2N7002SDW1T1G 2N SC88-6

RG56 20K_0402_5%

5V Level

@ CM17 220P_0402_50V7K

*DDA30_LA-F292PR02: RS_8.2ohm_RP_360ohm

HDMI_CLKP	RG59 EMI@	15 +-1% 0402	HDMI_R_CLKP	CG71 EMI@ 180 +-5% 0402 SD028180080
HDMI_CLKN	RG60 EMI@	15 +-1% 0402	HDMI_R_CLKN	
HDMI_TX_N2	RG63 EMI@	15 +-1% 0402	HDMI_R_TX_N2	CG72 EMI@ 180 +-5% 0402 SD028180080
HDMI_TX_P2	RG61 EMI@	15 +-1% 0402	HDMI_R_TX_P2	
HDMI_TX_P1	RG65 EMI@	15 +-1% 0402	HDMI_R_TX_P1	CG73 EMI@ 180 +-5% 0402 SD028180080
HDMI_TX_N1	RG10 EMI@	15 +-1% 0402	HDMI_R_TX_N1	
HDMI_TX_P0	RG12 EMI@	15 +-1% 0402	HDMI_R_TX_P0	CG74 EMI@ 180 +-5% 0402 SD028180080
HDMI_TX_N0	RG13 EMI@	15 +-1% 0402	HDMI_R_TX_N0	

@ESD@ D21

HDMI_R_TX_N0 / HDMI_R_TX_P0 / HDMI_R_CLKN / HDMI_R_CLKP → HDMI_R_TX_N0 / HDMI_R_TX_P0 / HDMI_R_CLKN / HDMI_R_CLKP

AZ1045-04F.R7G DFN2510P10E ESD
SC300001Y00

@ESD@ D22

HDMI_R_TX_N1 / HDMI_R_TX_P1 / HDMI_R_TX_N2 / HDMI_R_TX_P2 → HDMI_R_TX_N1 / HDMI_R_TX_P1 / HDMI_R_TX_N2 / HDMI_R_TX_P2

AZ1045-04F.R7G DFN2510P10E ESD
SC300001Y00

@ESD@ DG1

HP_DETECT / HDMI_CTRL_DAT / HDMI_CTRL_CLK → HP_DETECT / HDMI_CTRL_DAT / HDMI_CTRL_CLK

AZ1045-04F.R7G DFN2510P10E ESD
SC300001Y00

<5> HOST_DP1_CTRL_CLK → HOST_DP1_CTRL_CLK → HDMI_CTRL_CLK

QG2 SB00001FF00
L2N7002SDW1T1G 2N SC88-6

+3VS

<5> HOST_DP1_CTRL_DATA → HOST_DP1_CTRL_DATA → HDMI_CTRL_DAT

QG2 SB00001FF00
L2N7002SDW1T1G 2N SC88-6

+HDMI_CRT_5V

+3VS

RG105 2.2K_0402_5% HDMI_CTRL_CLK
RG109 2.2K_0402_5% HDMI_CTRL_DAT
RG110 2.2K_0402_5% HOST_DP1_CTRL_CLK
RG111 2.2K_0402_5% HOST_DP1_CTRL_DATA

W=40mils

FG1 AP2330W-7_SC59-3 SA00004ZA00

+5VS → IN; OUT → +HDMI_CRT_5V

CG46 0.1U_0402_16V7K

CG47 4.7U_0402_6.3V6M

HDMI Conn.

JHDMI CONN@ LOTES_AHDM0064-P001A DC232007B00

HP_DETECT	19	HP_DET	
+HDMI_CRT_5V	18	+5V	
	17	DDC/CEC_GND	
HDMI_CTRL_DAT	16	SDA	
HDMI_CTRL_CLK	15	SCL	
	14	Reserved	
	13	CEC	
HDMI_R_CLKN	12	CK-	
	11	CK_shield	GND 23
HDMI_R_CLKP	10	CK+	GND 22
HDMI_R_TX_N0	9	D0-	GND 21
	8	D0_shield	GND 20
HDMI_R_TX_P0	7	D0+	
HDMI_R_TX_N1	6	D1-	
	5	D1_shield	
HDMI_R_TX_P1	4	D1+	
HDMI_R_TX_N2	3	D2-	
	2	D2_shield	
HDMI_R_TX_P2	1	D2+	

@ CM26 10P_0402_50V8J

@ CM27 10P_0402_50V8J

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+LAN_VDD_3V3 Rising time
need>0.5mS and <100mS

CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

RTL8107ESH-CG/RTL8111HSH-CG Co-Lay

UL1

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32

CL10& CL16 close to UL1: Pin 23

(SA000084T00) RTL8111HSH-CG Giga

powe rail need to check

powe rail need to check

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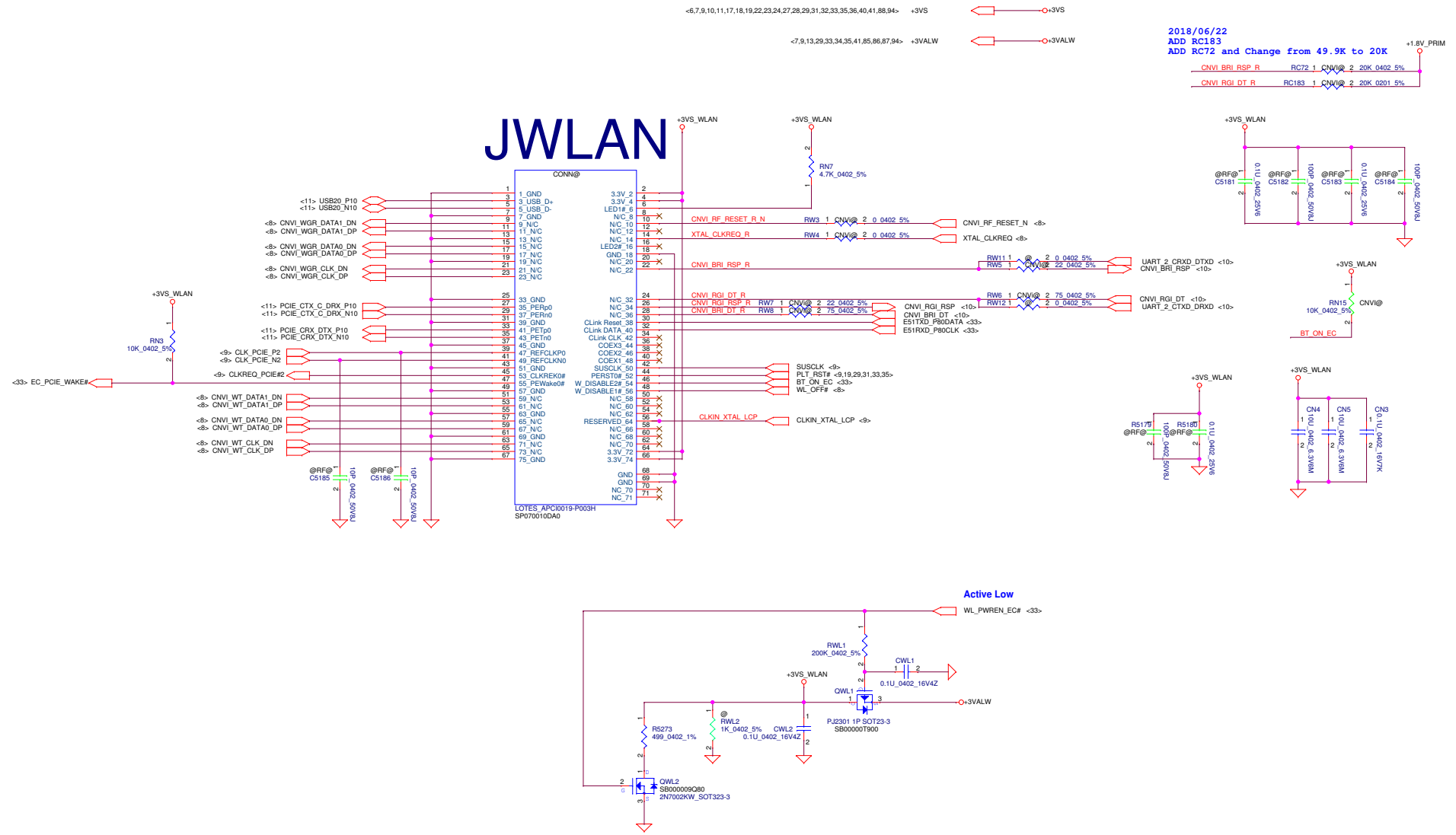
JWLAN



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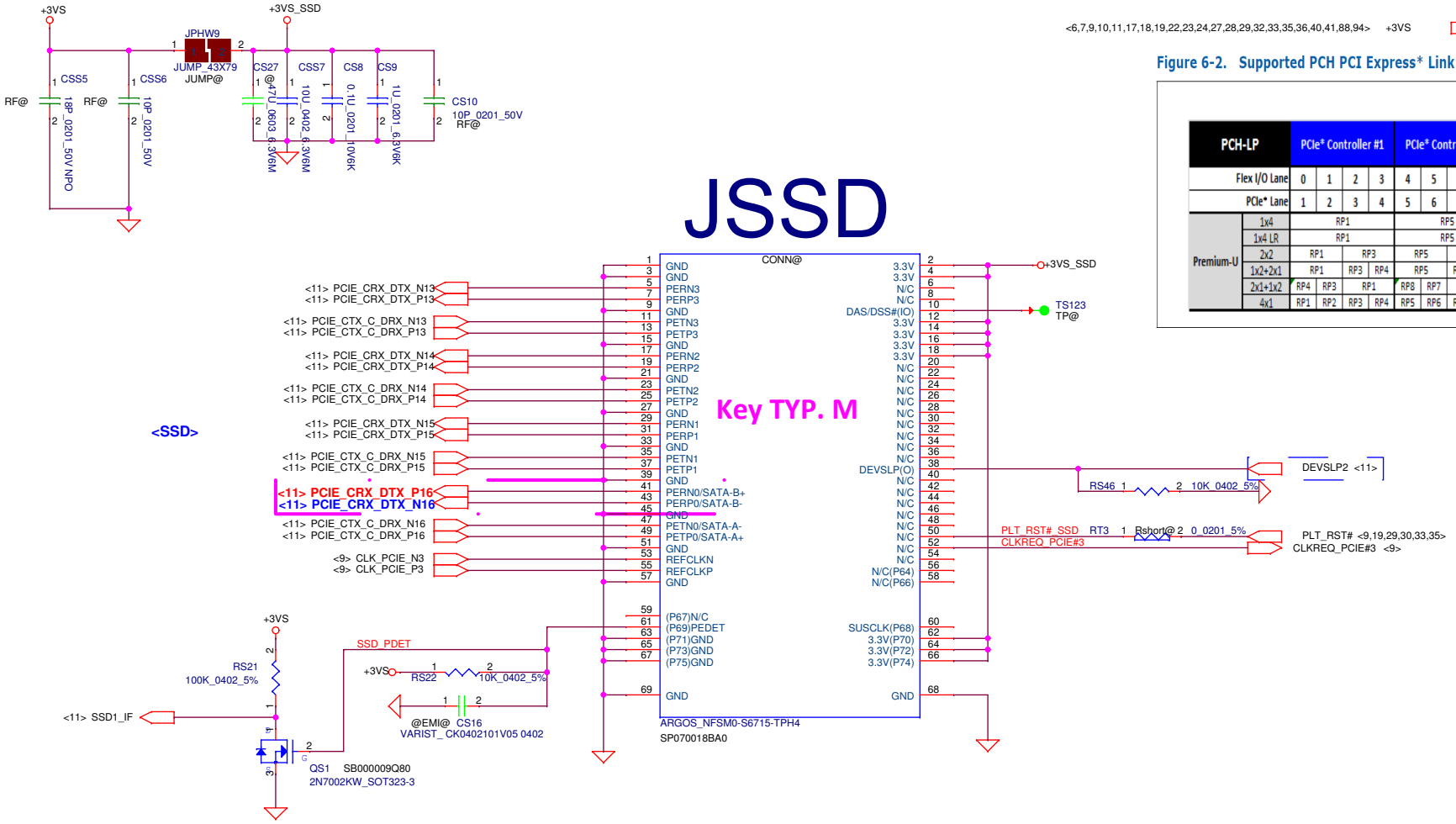


Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

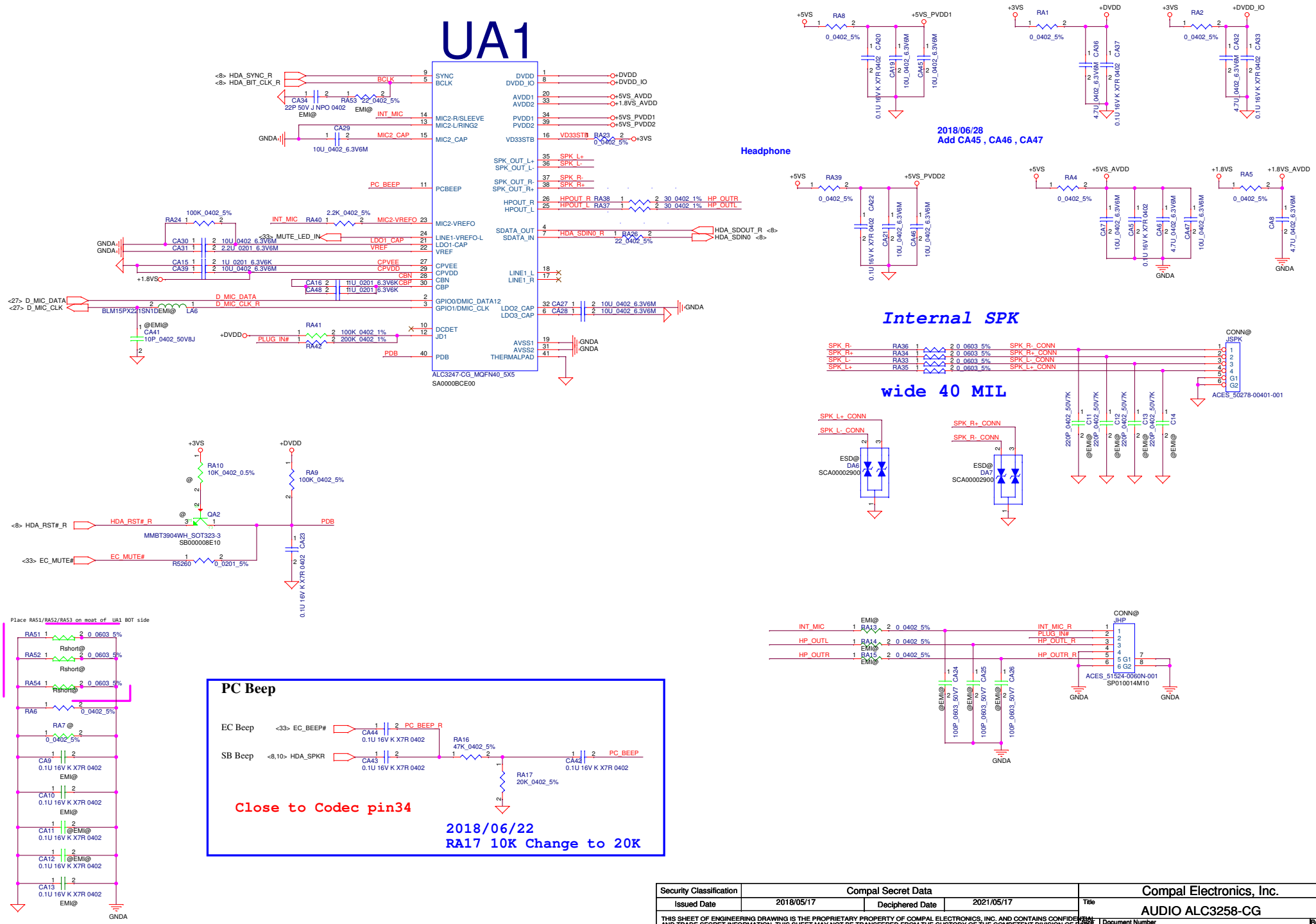
Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH	42	N/C
41	PETn0	PCIe TX	44	N/C
43	PETp0	PCIe TX	46	N/C
45	GND	Return current path	48	N/C
47	PERn0	PCIe Rx	50	PERST#
49	PERp0	PCIe Rx	52	CLKREQ#
51	GND	Return current path		

39	GND	Return Current Path	40
41	+B / TXP	Transmitter Differential Signal Pair	42
43	-B / TXN	Transmitter Differential Signal Pair	44
45	GND	Return Current Path	46
47	-A / RXN	Receiver Differential Signal Pair	48
49	+A / RXP	Receiver Differential Signal Pair	50
51	GND	Return Current Path	52

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.			
Title	*M.2 SSD*		
Size	Document Number LA-H323P		Rev V0.1
Date: Monday, November 19, 2018	Sheet 31 of 59		



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Issued Date	2018/05/17	Deciphered Date 2021/05/17	Title: AUDIO ALC3258-CG
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EC Board ID (UMA, DIS, phase) control table

RK4	WHL-U			
	DB	SI	PV	MV
UMA	0 (0ohm)	15K (0ohm)	27K (0ohm)	43K (0ohm)
DIS	12K (0ohm)	20K (0ohm)	33K (0ohm)	56K (0ohm)

2018/06/11
Close to UK1 Pin 111

Reserve EC_CLR_CMOS for clear CMOS
(2016-03-04 : Confirm Intel platform not support EC Clear CMOS function)
(2017-10-05 : 20180PP Add EC Clear CMOS function)

For Solve tPCH04(Min 9ms) Sequence Timing

CC128 RC369 place near EC Side

EMI request

UK1 KB9022QD_LQFP128_14X14
SA000075S30

20mil

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Compal Electronics, Inc.

Title: EC ENE-KB9022

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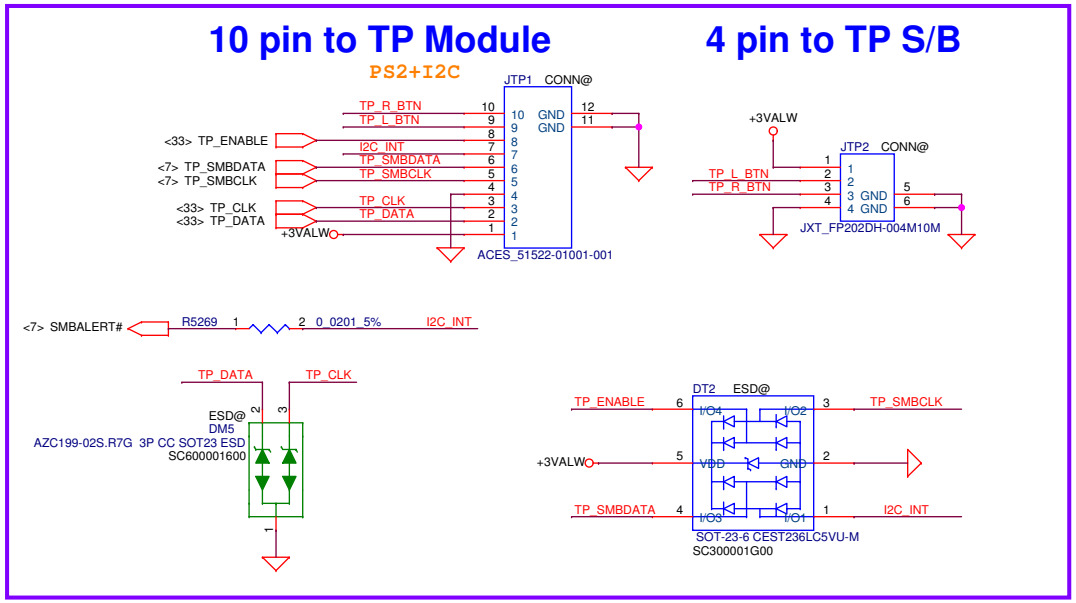

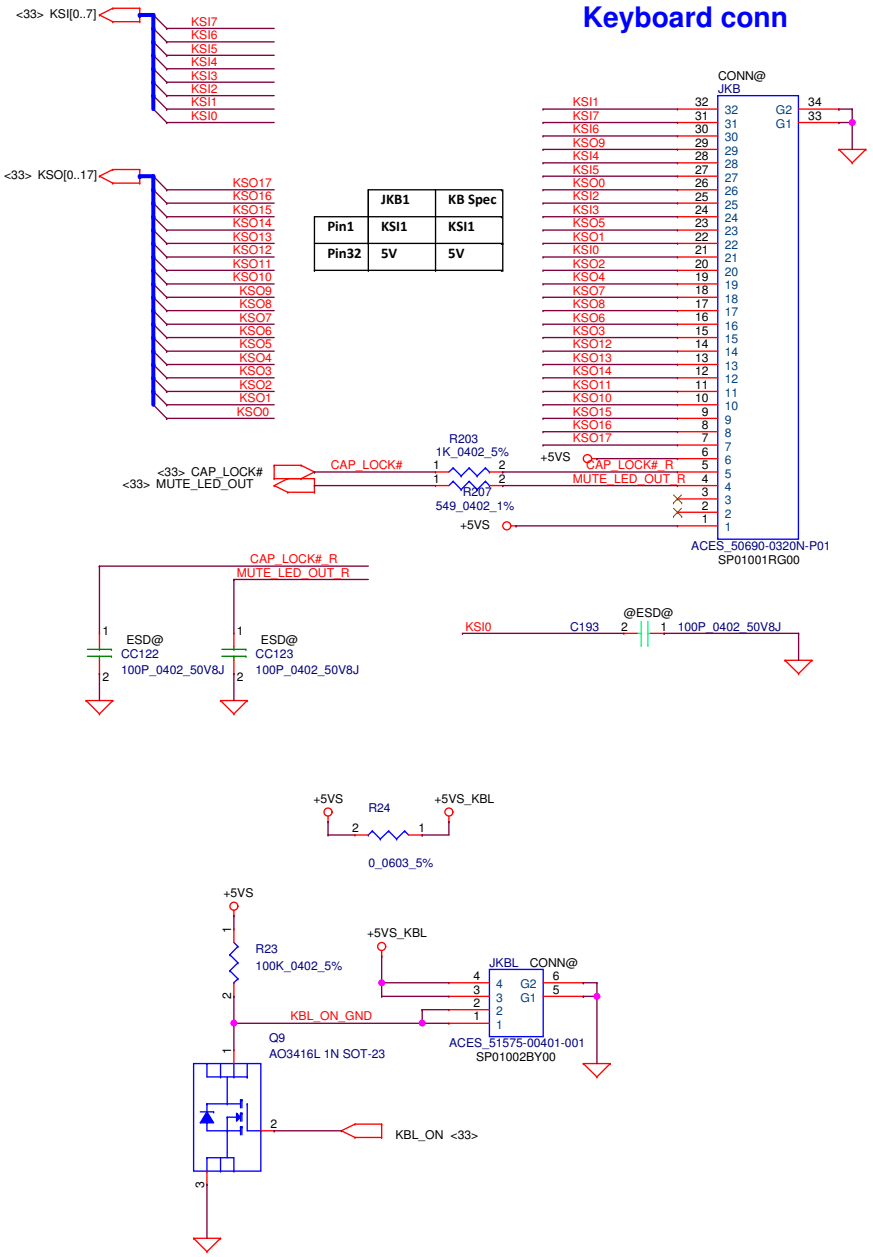

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Compal Electronics, Inc.

Title: KB/TP

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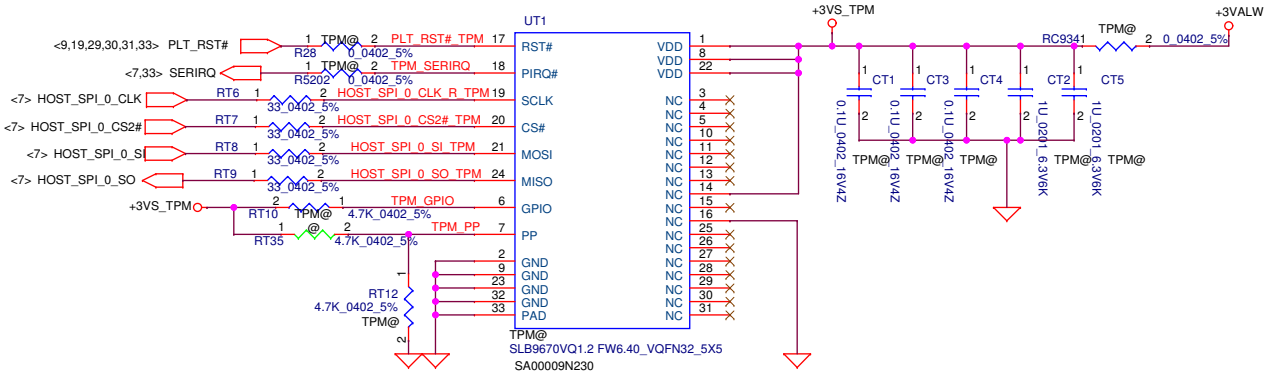
+3VALW <7,9,13,29,30,33,34,41,85,86,87,94>

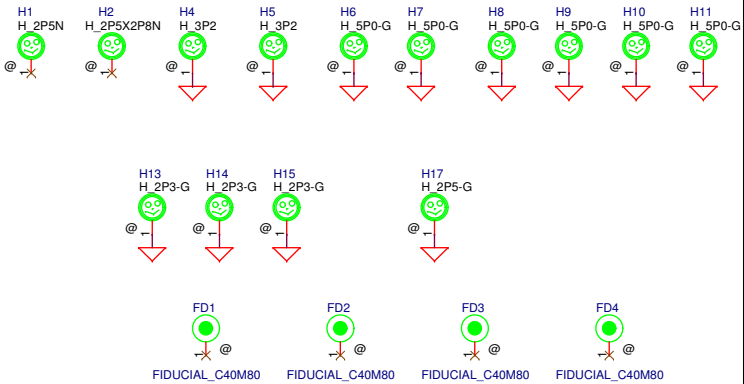
+3VS <6,7,9,10,11,17,18,19,22,23,24,27,28,29,31,32,33,36,40,41,88,94>

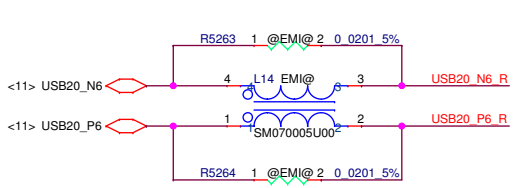
TPM2.0

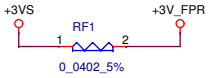


Screw Hole

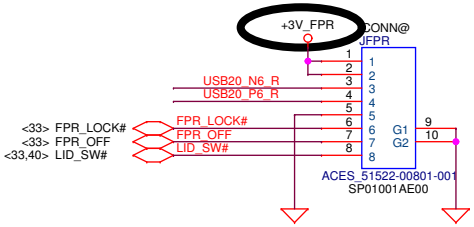
SSD WLAN GPU CPU

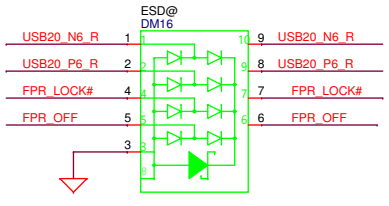






Finger Printer





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Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: TPM/Screw

Size: D | Document Number: LA-H323P | Rev: V0.1

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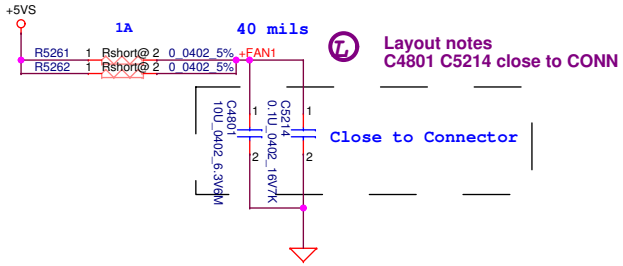

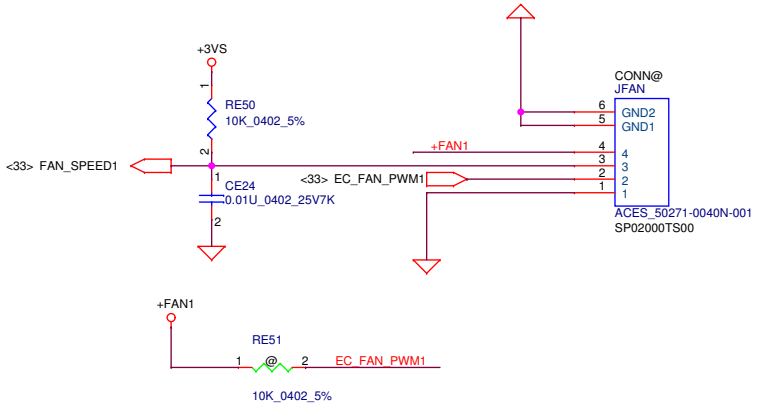

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Compal Electronics, Inc.

Title: FAN

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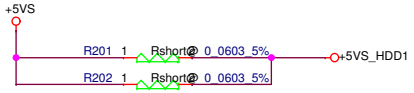
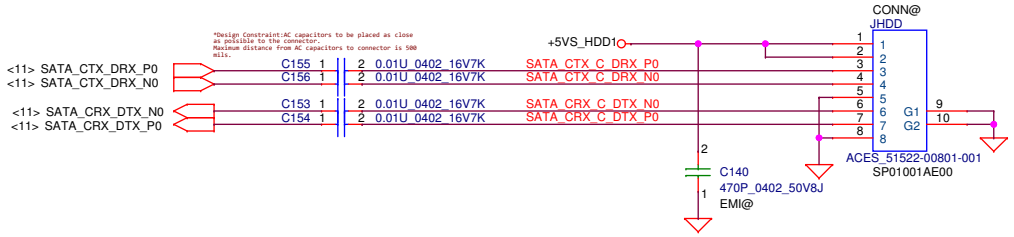
2.5" SATA HDD

<27,28,32,33,34,36,41,92> +5VS
<12,24,38,39,40,41,85,86,88,89> +5VALW
<7,9,13,29,30,33,34,35,41,85,86,87,94> +3VALW

+5VS
+5VALW
+3VALW

<PV> change short pad





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Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: HDD/ODD Conn

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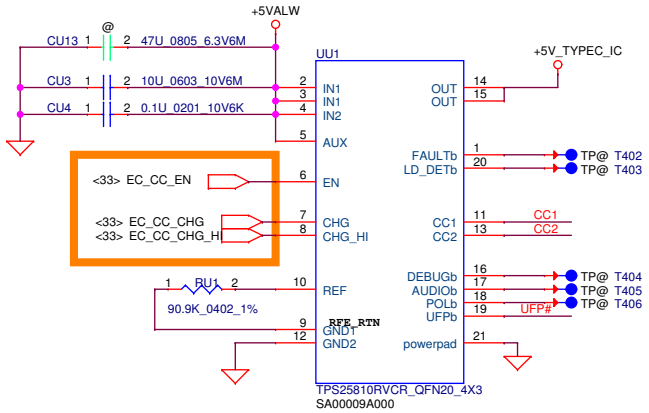
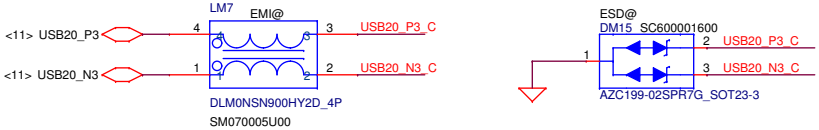
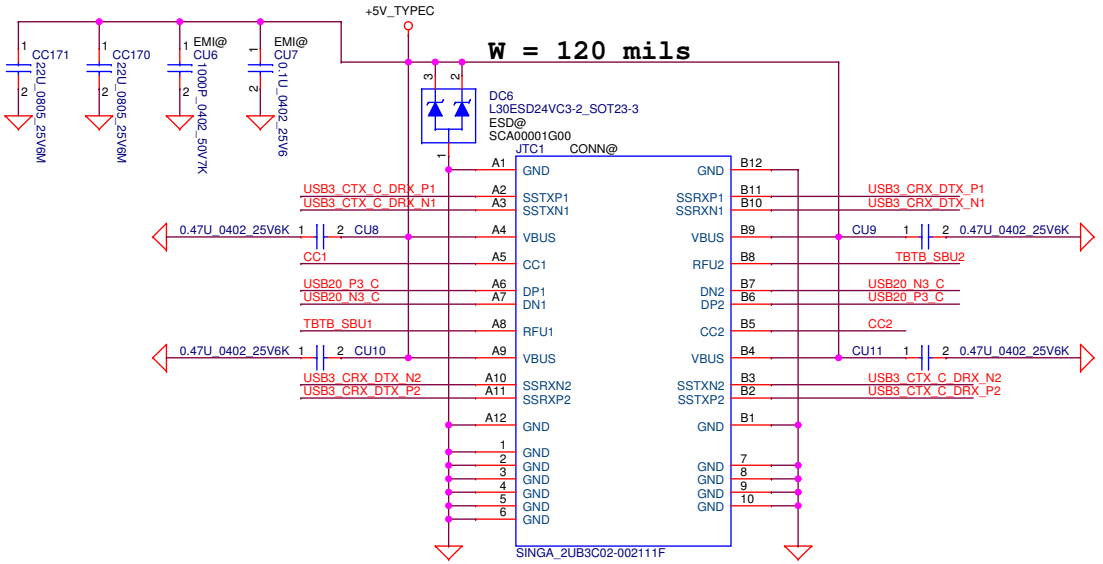
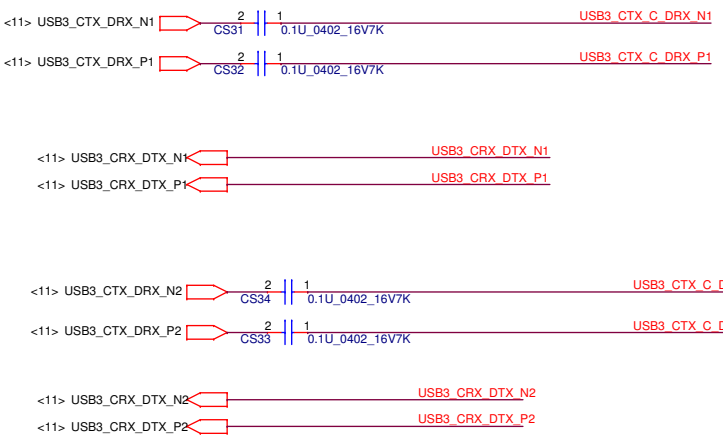
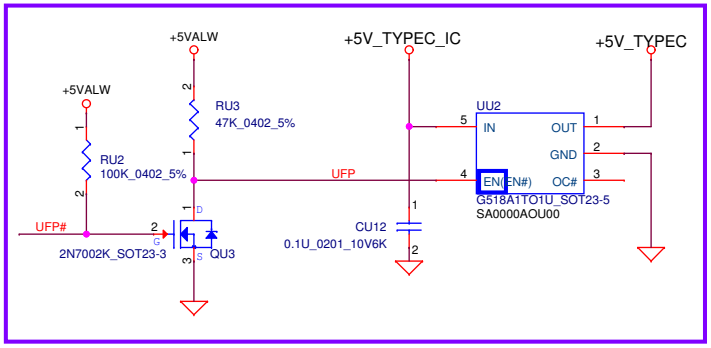
Type-C - USB only

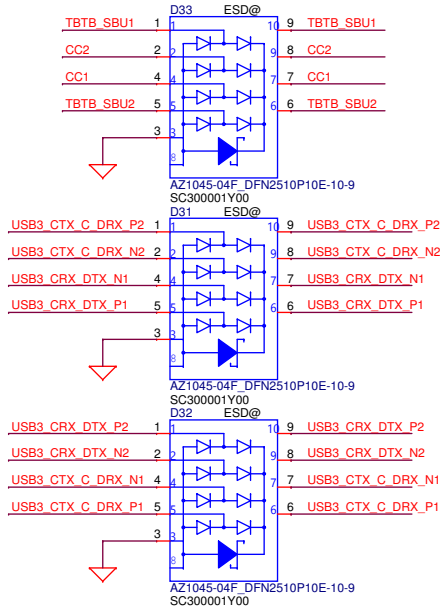












Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: Type-C Conn

Size: Custom | Document Number: LA-H323P | Rev: V0.1

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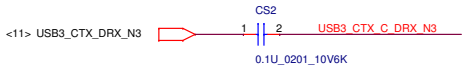
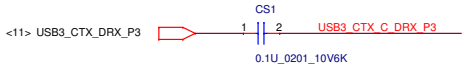
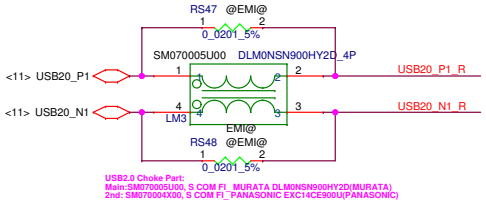
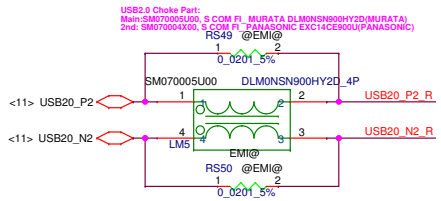


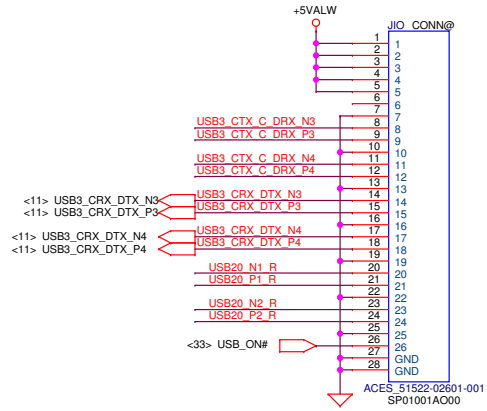




USB2.0 Choke Part:
Main:SM070005U00, S COM FI_MURATA DLM0NSN900HY2D(MURATA)
2nd: SM070004X00, S COM FI_PANASONIC EXC14CE900U(PANASONIC)

USB2.0 Choke Part:
Main:SM070005U00, S COM FI_MURATA DLM0NSN900HY2D(MURATA)
2nd: SM070004X00, S COM FI_PANASONIC EXC14CE900U(PANASONIC)





Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

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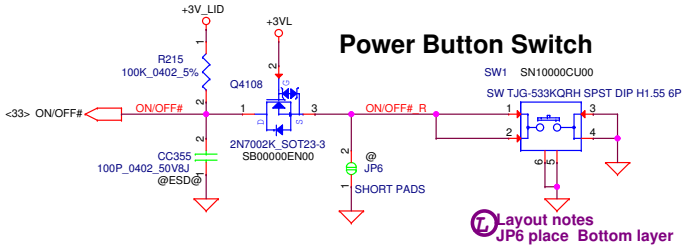
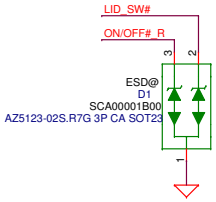
Power Button Switch

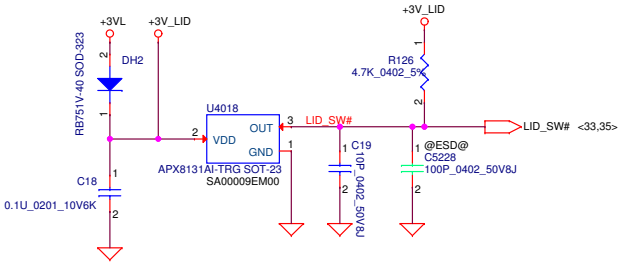


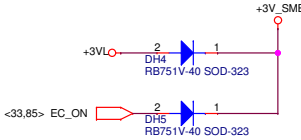
Layout notes
JP6 place Bottom layer

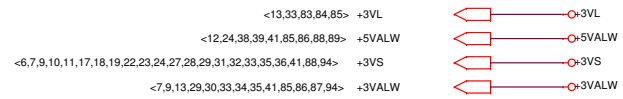
ESD Diode

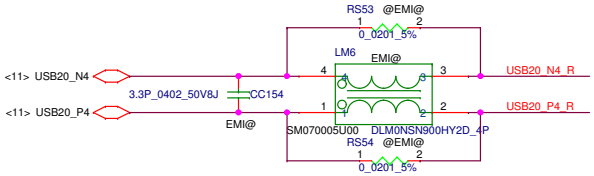


Lid Switch (Hall Effect Sensor)



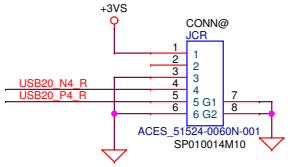




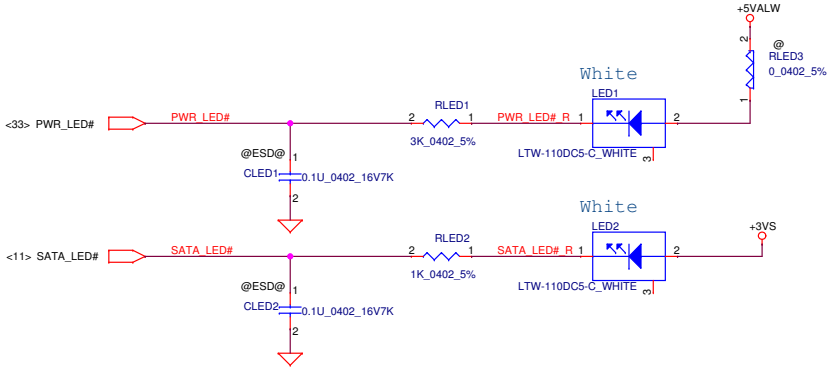


CR/B

Card reader



HDD LED/ POWER LED



Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: IO CON

Size: Custom | Document Number: LA-H323P | Rev: V0.1

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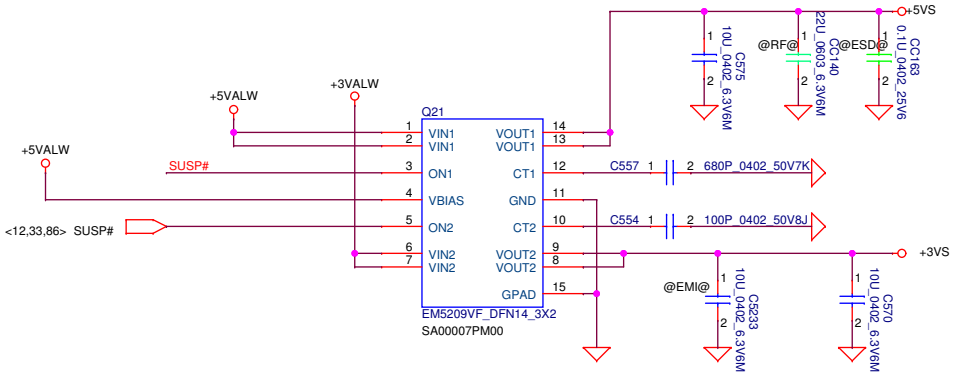
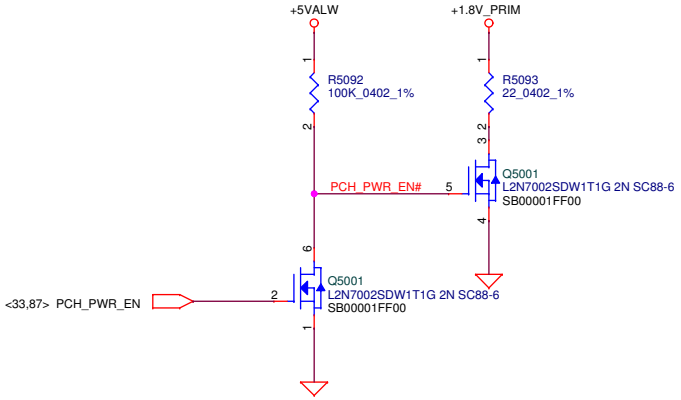


For +1.8V_PRIM Discharge



Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-H323P	V0.1

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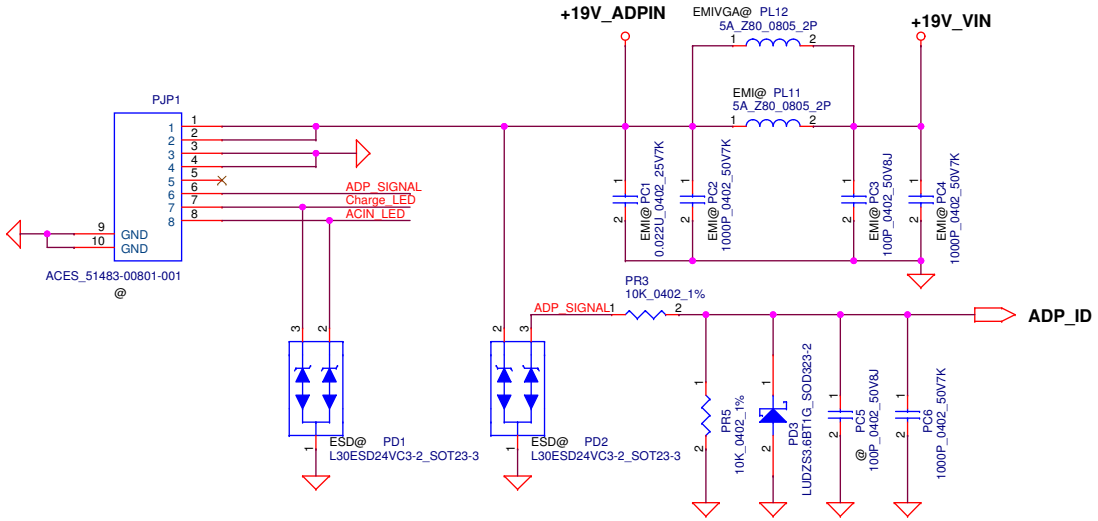

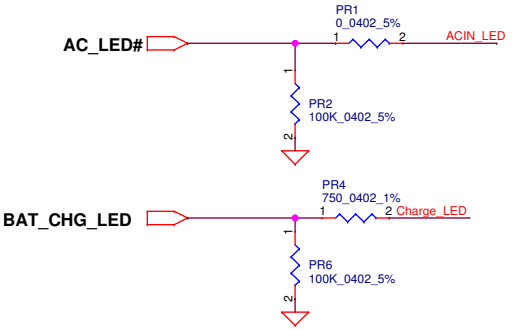

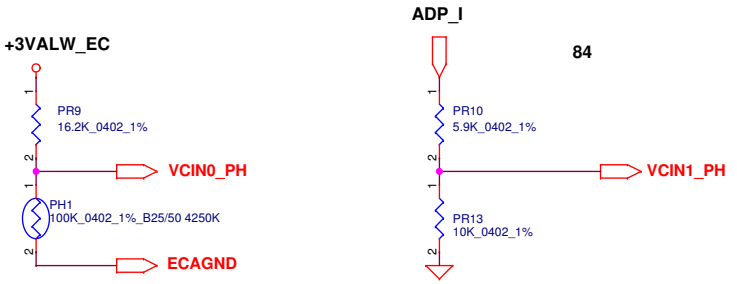

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	DC Conn		
Size	Document Number		Rev
	LAH323P		v0.3
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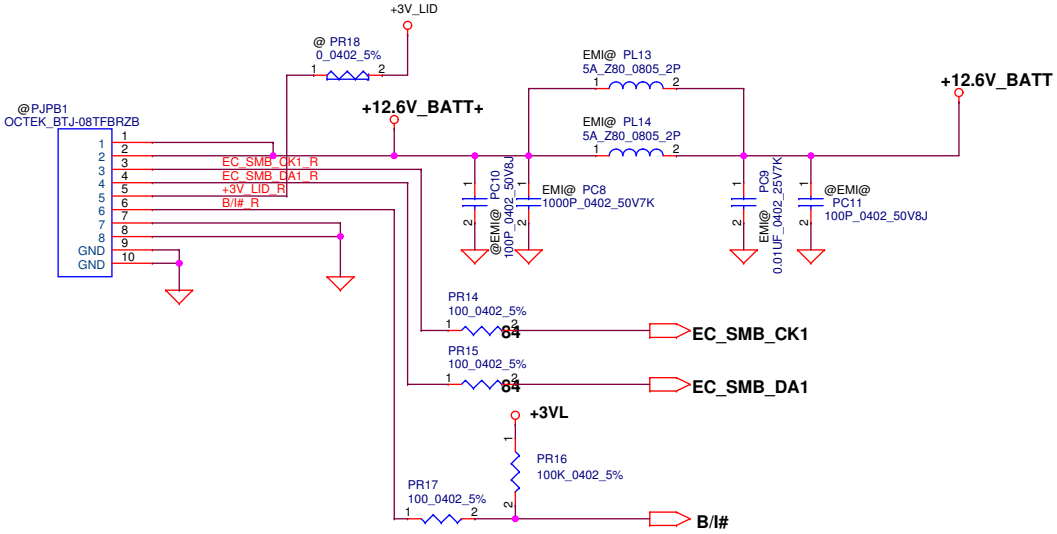

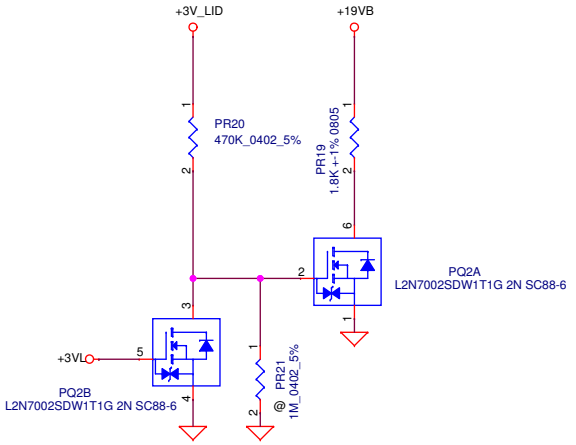

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: ***BATT Conn***

Size: C | Document Number: **LAH323P** | Rev: v0.3

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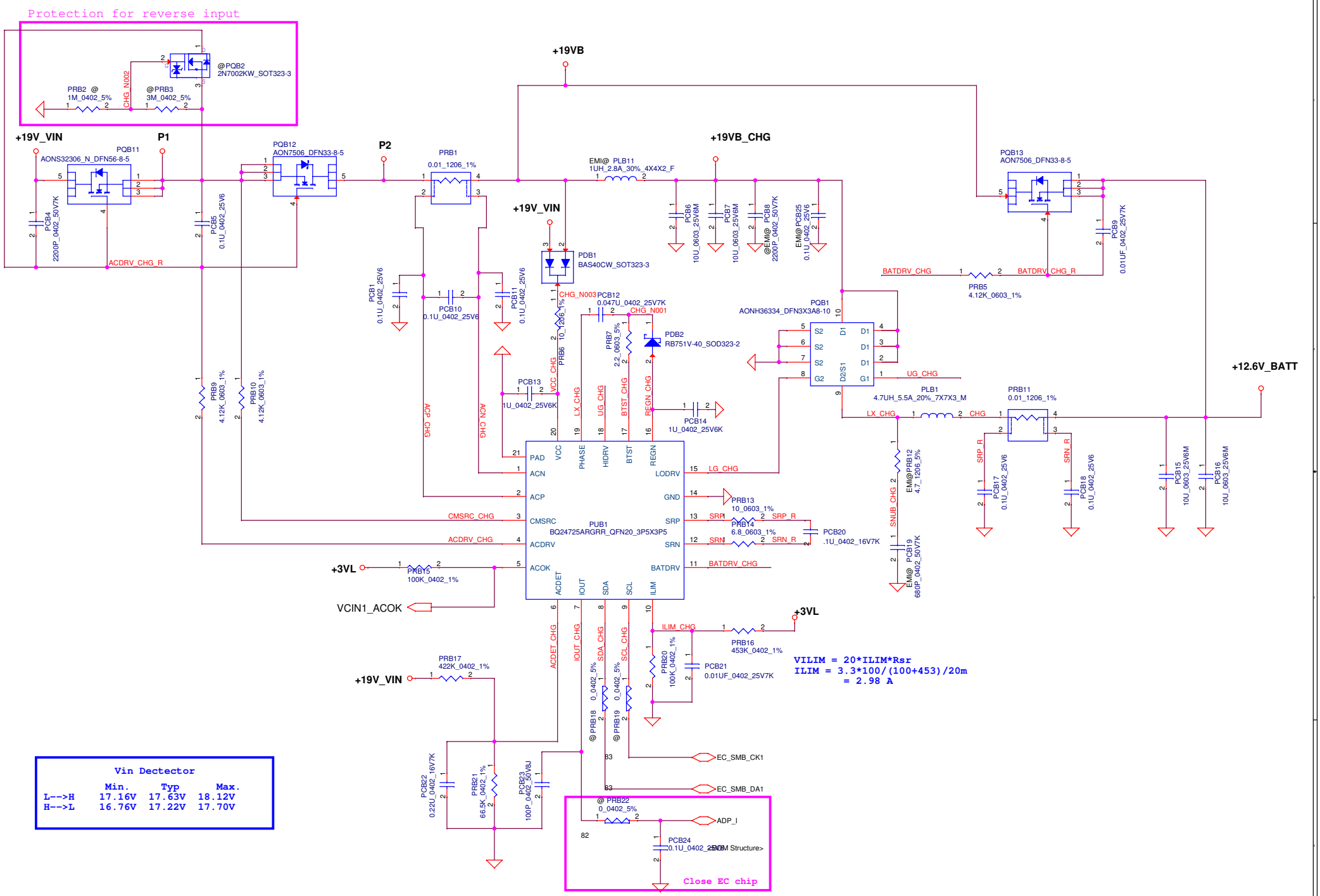

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: **CHARGER**

Size: D | Document Number | Rev: v0.3

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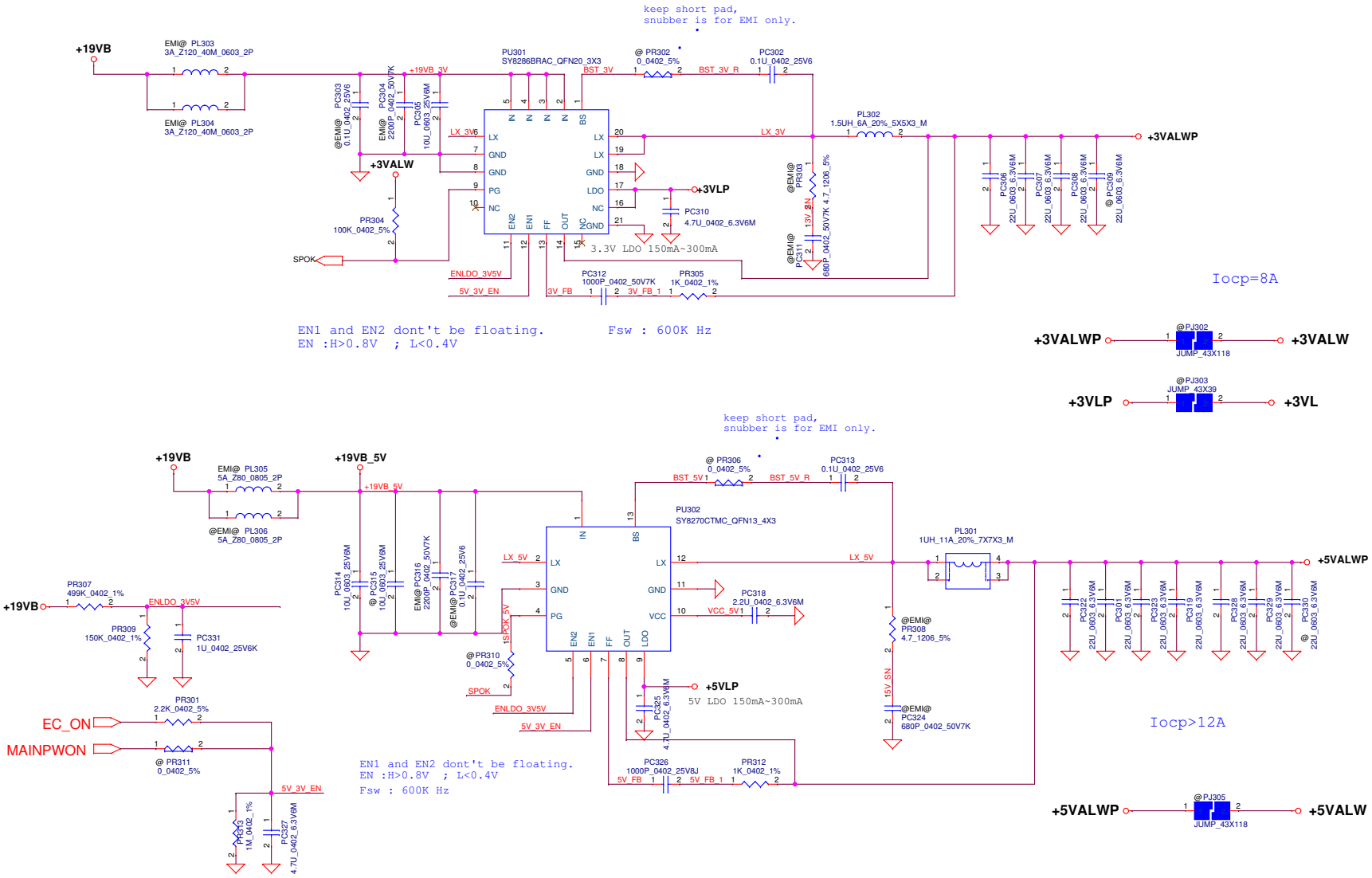
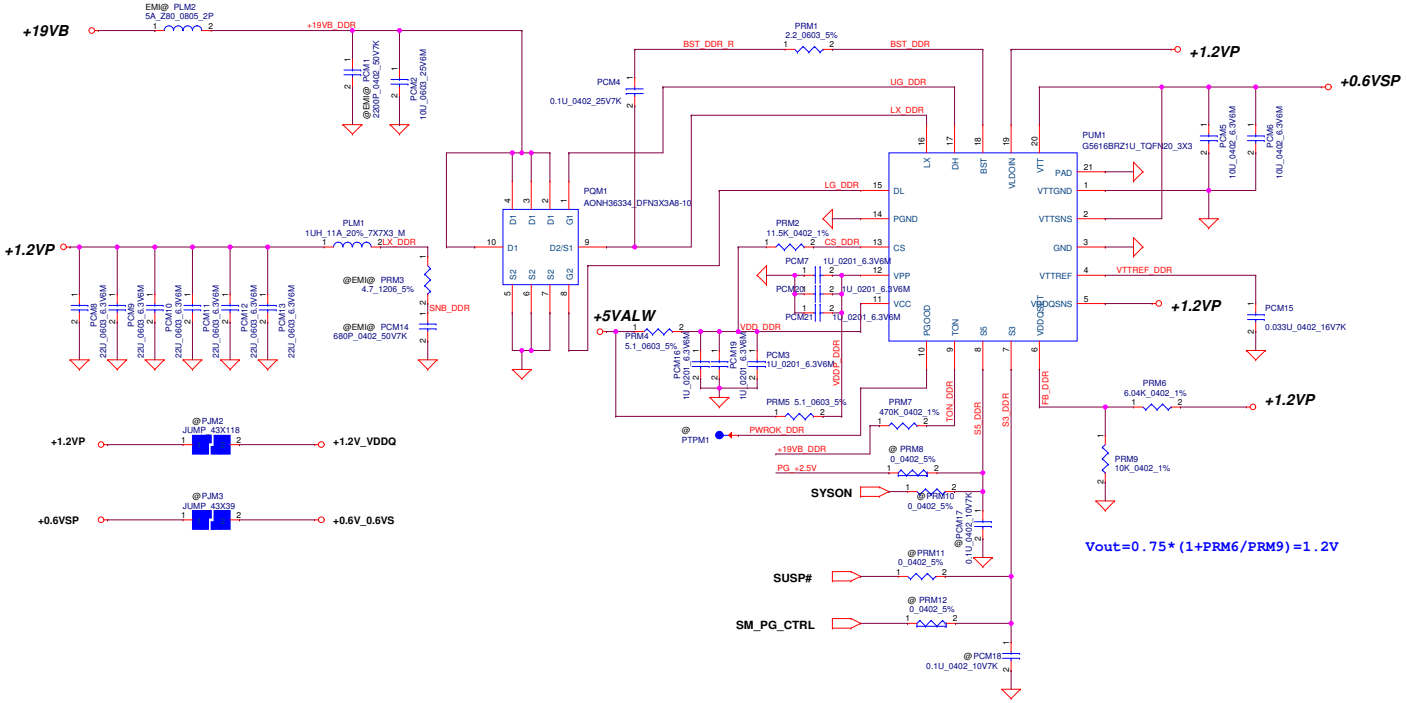
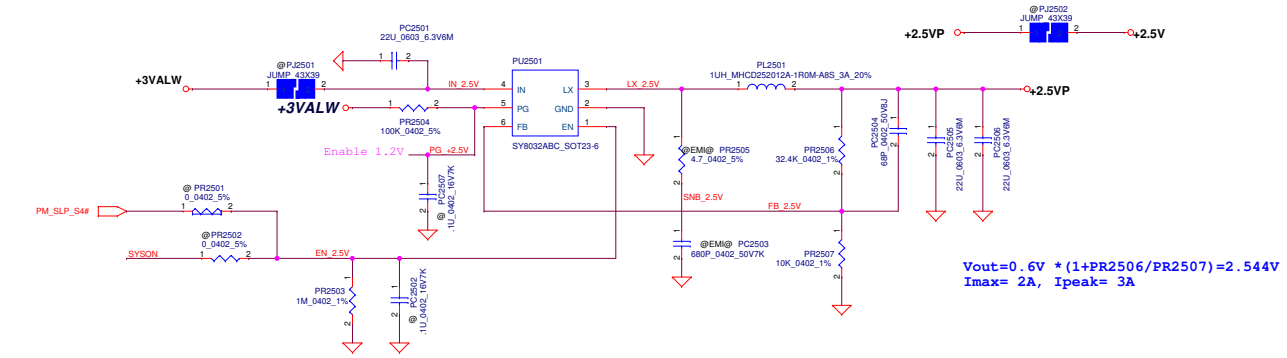


Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.			
Title	3VALW/5VALW		
Size: Custom	Document Number: LAH323P		Rev: v0.3
Date: Monday, November 19, 2018	Sheet 85 of 99		





Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5V

Size: Custom | Document Number | Rev: v0.3

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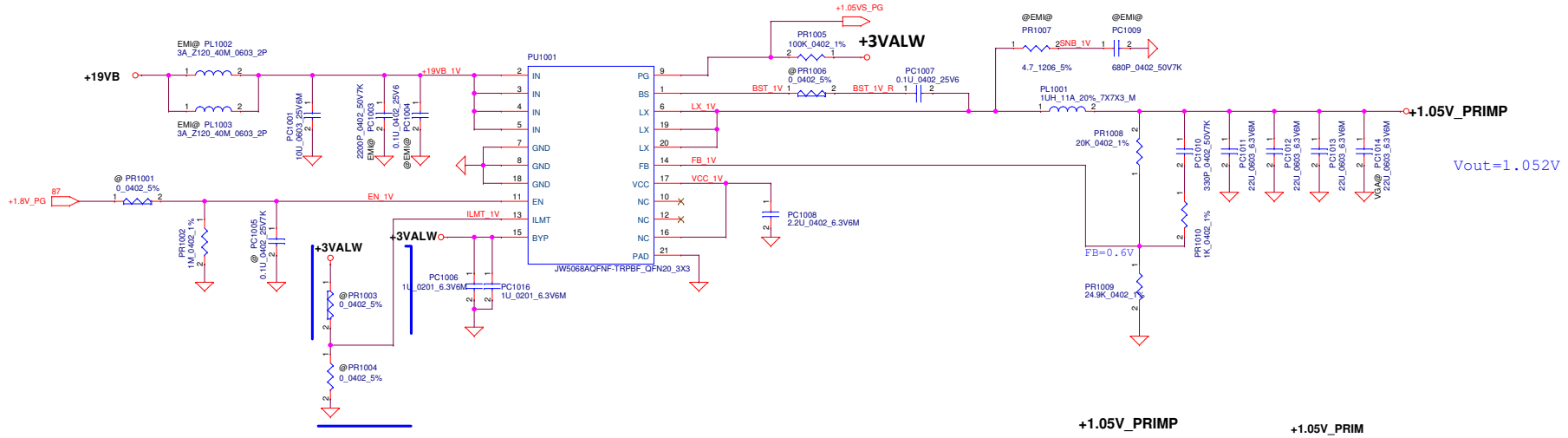
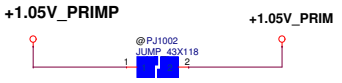
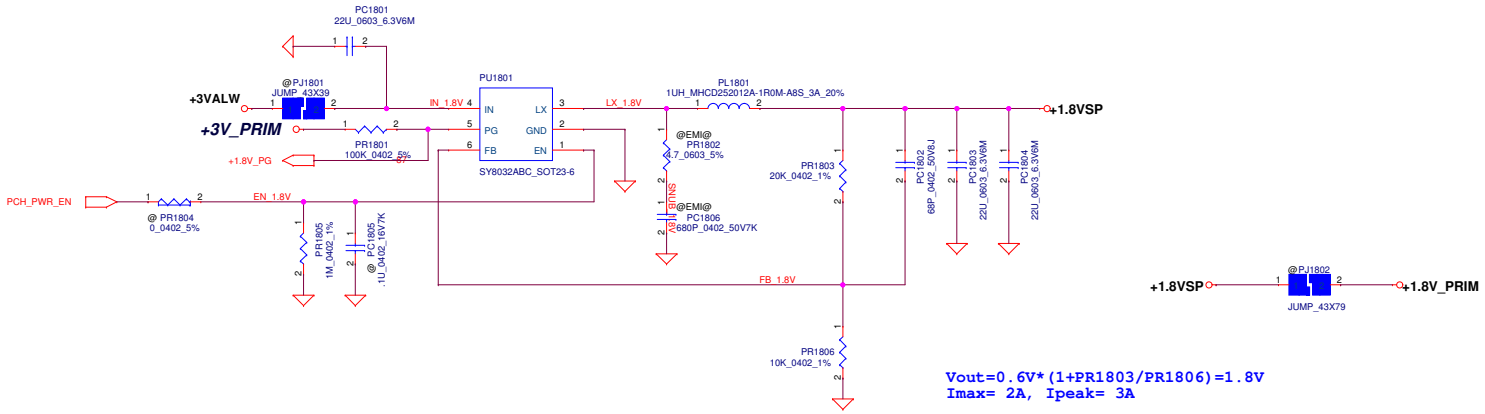


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.



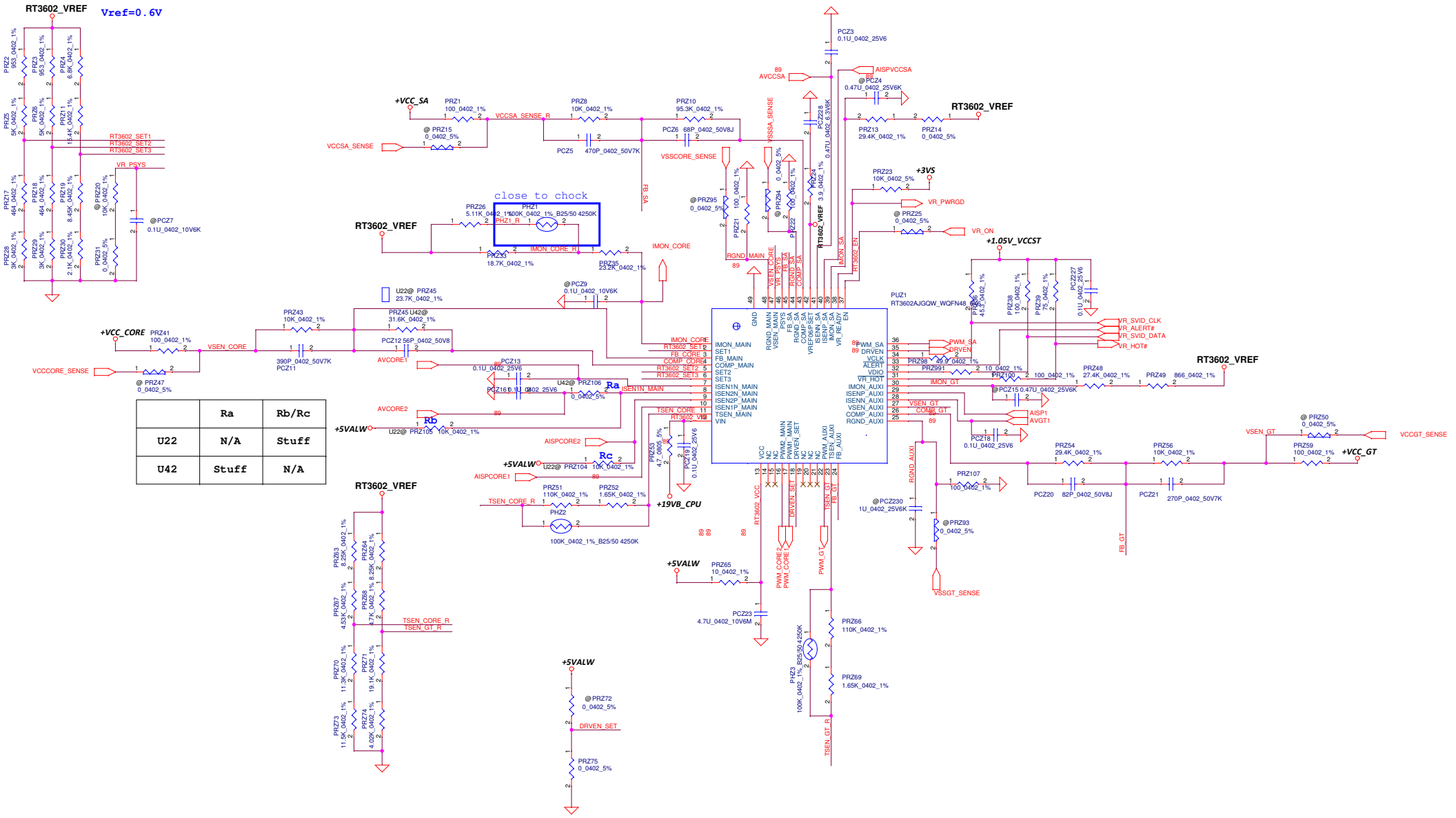


Vout=0.6V*(1+PR1803/PR1806)=1.8V
Imax= 2A, Ipeak= 3A

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title: 1.0V_PRIM and +1.8V_PRIM

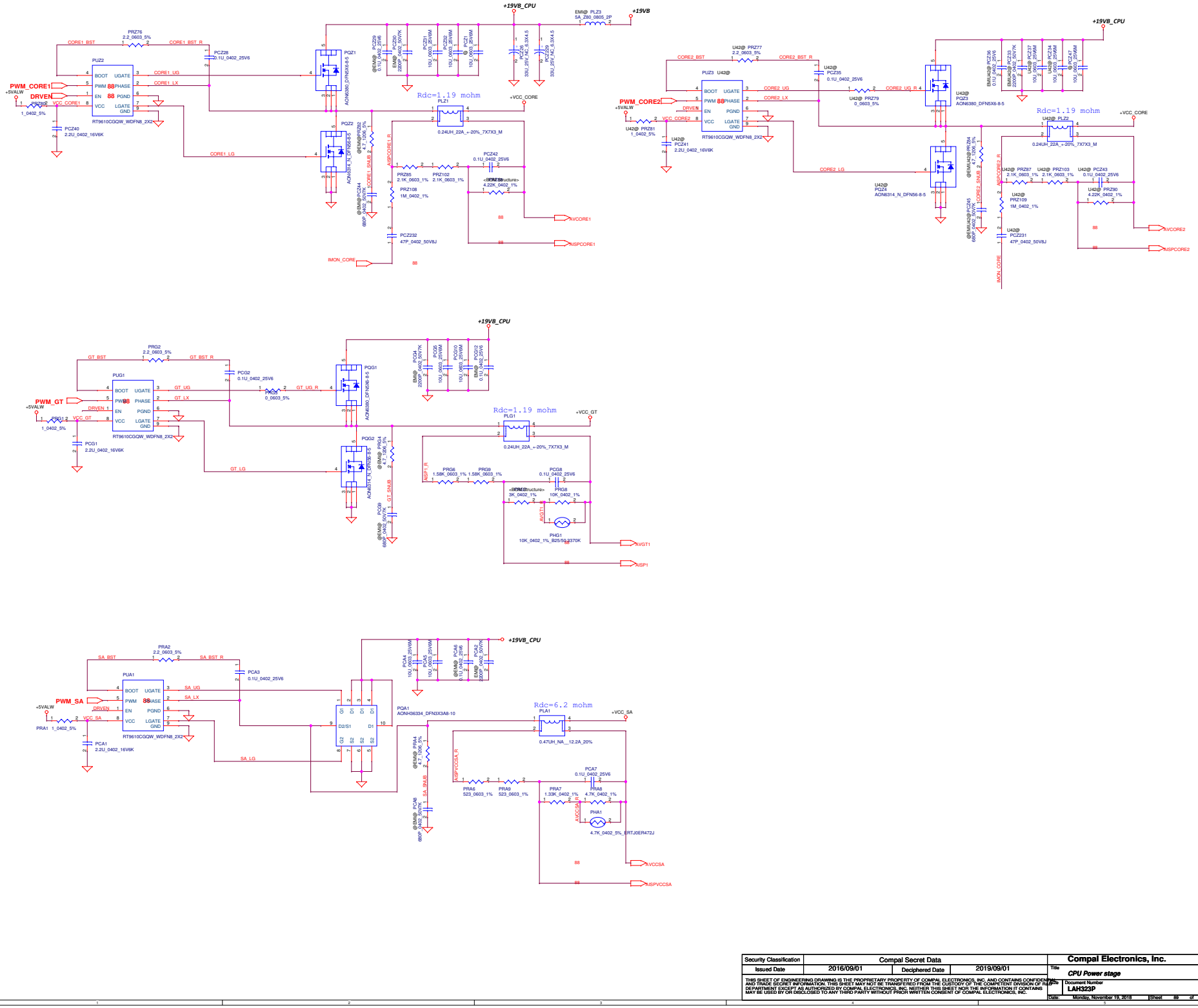
Size: C	Document Number	Rev: v0.3
Date: Monday, November 19, 2018	Sheet 87 of 99	



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.			
Title: CPU_CORE			
Size:	Document Number: LAH323P		Rev: v0.3
Date: Monday, November 19, 2018	Sheet 88 of 99		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date 2019/09/01	Title: CPU Power stage
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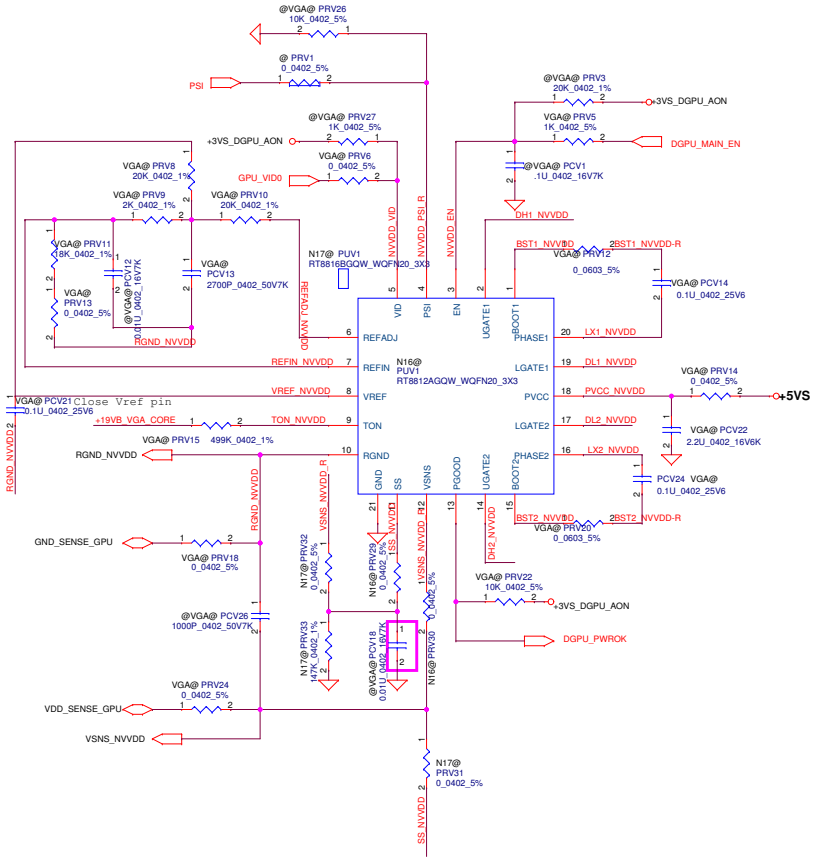
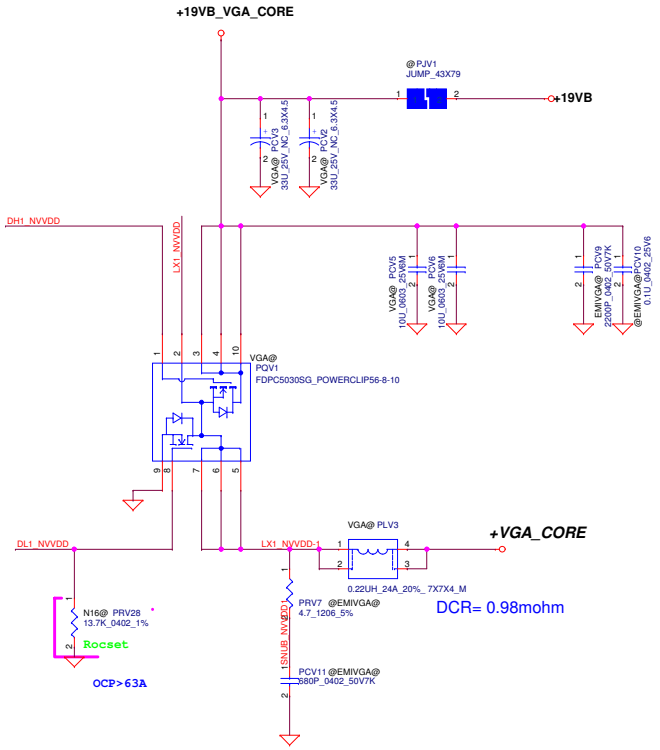
			Date: Monday, November 19, 2018; Sheet 89 of 99

PWM-VID Spec and component Values

PWM-VID Spec		Config B
Vmin		0.6V
Vmax		1.2V
Vboot		0.9V
Voltage step		6.25mV
N of Voltage level		96
Rrefadj	PRV10	20K
Rref1	PRV8	20K
Rboot	PRV9	2K
Rref2=PRV8+PRV11	PRV11	18K
	PRV13	0
C	PCV13	2.7nf

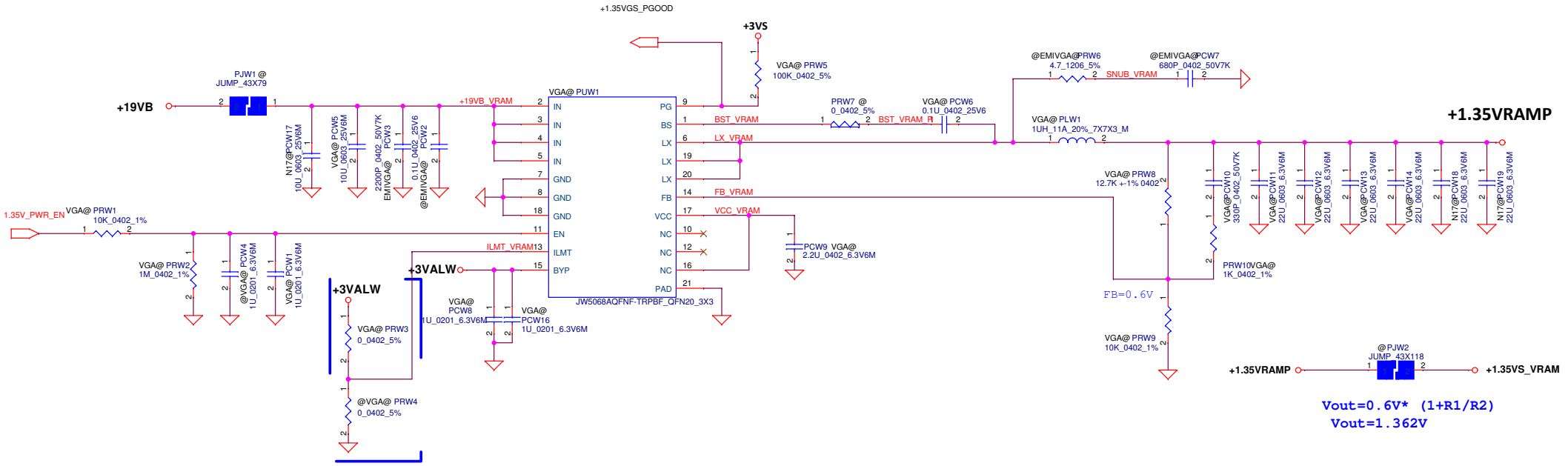
VGA Chip	N16S-GTR
OpenVReg Configurations	Config B
Rated TDP Power at Tj=102C	18W
Boosted GPU Total at Tj=102C	23W
EDP-Continuous at Tj=102C	26A
EDP-Peak at Tj=102C	51A
Istep max (Evaluation)	36.36A
OCP Setting	61A
Rcset	9.76K
Recommendation	2phase





Security Classification	Compal Secret Data		
Issued Date	2015/09/01	Deciphered Date	2018/09/01

Compal Electronics, Inc.			
Title	VGA_CORE		
Size	Document Number		Rev
			v0.3
Date:	Thursday, November 15, 2018	Sheet	92 of 99



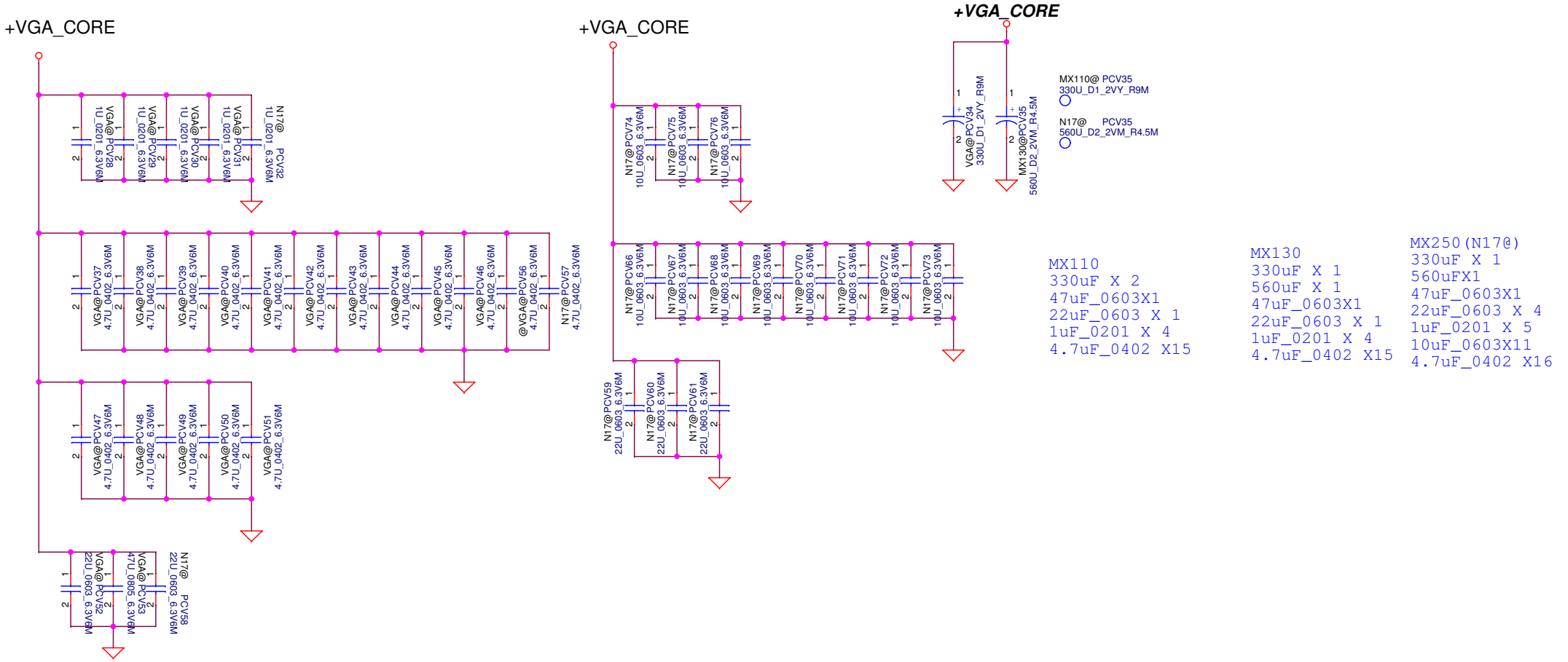
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *+1.35VS_VRAM*

Size: | Document Number: LAH323P | Rev: v0.3

Date: Thursday, November 15, 2018 | Sheet 94 of 99



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: ***VGA CHIP DECOUPLING***

Size | Document Number | Rev: v0.3

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+VCC_CORE

VCC_CORE :
U22
330uF*1
22uF*25
1uF*35

U42
330uF*2
22uF*35
1uF*35

+VCC_GT

VCC_GT :
U22&U42
330uF*1
22uF*24
1uF*13

+VCC_SA

VCC_SA :
U22 & U42
22uF*9
1uF*7

BOM option
by JU22(for GT) and JU42A (for IA)

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size: B | Document Number: LAH323P | Rev: v0.3

Date: Thursday, November 15, 2018 | Sheet 90 of 99

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

Power State

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x2C	0x58	0x59

<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0(S/B)
2	USB3.0(S/B)
3	USB3.0 Type-C
4	Card Reader
5	Camera
6	FPR
7	TS
8	X
9	X
10	BT

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION		CLK
0	1		1	USB3.0 Type-C		X
1	2		2			
2	3		3	USB3.0(S/B)		X
3	4		4	USB3.0(S/B)		X
4	5		5	GPU(DIS only)		CLK0
5	6		6			
6	7					
7	8					
8	9			LAN		CLK1
9	10			WLAN		CLK2
10	11	0		HDD		X
11	12	1a		X		X
12	13			PCIe x4	X	CLK3
13	14					
14	15	1b*			SATA SSD	X
15	16	2				

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

I3_8145U_R1@
UC1
i3-8145U
SA0000C8R50
S IC A32 FJ8068404064702 QQK9 W0 2.1G BGA 1528

I5_8265U_R1@
UC1
i5-8265U
SA0000C8Q50
S IC A32 FJ8068404064604 QQTG W0 1.6G BGA 1528

I7_8565U_R1@
UC1
i7_8550U
SA0000C8P50
S IC A32 FJ8068404064403 QQK6 W0 1.8G BGA 1528

MX110@
UV1
N16V-GMR1-S-A2
SA00009T00
S IC N16V-GMR1-S-A2 BGA 595PS

MX130@
UV1
N16S-GTR-S-A2
SA00009FP00
S IC N16S-GTR-S-A2 BGA 595P GPU

MX250@
UV1
N16S-GTR-S-A2
SA0000C2B00
S IC N17S-G2-A1 CS BGA 595P GPU

ZZZ
2G Micron
M2G_R1@
X7681332L02

ZZZ
2G Hynix
H2G_R1@
X7681332L01

ZZZ
2G Samsung
S2G_R1@
NA

ZZZ
WHL-2G
PCB_2G@
DA60023X000
PCB 2DM LA-G07FP REV0 M/B 3

ZZZ
WHL-2G
PCB_4G@
DA8001HS000
PCB 2H8 LA-H324P REV0 M/B 5

ZZZ
EMC for EE
2G_X4E@
X4EAFU32L01
SMT EMC FOR EE AH323 FPW50

ZZZ
EMC for EE
4G_X4E@
X4EAGK32L01
SMT EMC FOR EE AH324 FPW50

45@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

RO0000003HM

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/05/17	Deciphered Date 2021/05/17	Title: Notes List
Size: Custom	Document Number: LA-H323P		Rev: V0.1
Date: Thursday, November 15, 2018	Sheet 3 of 59		