Table of Contents

CAD Note:

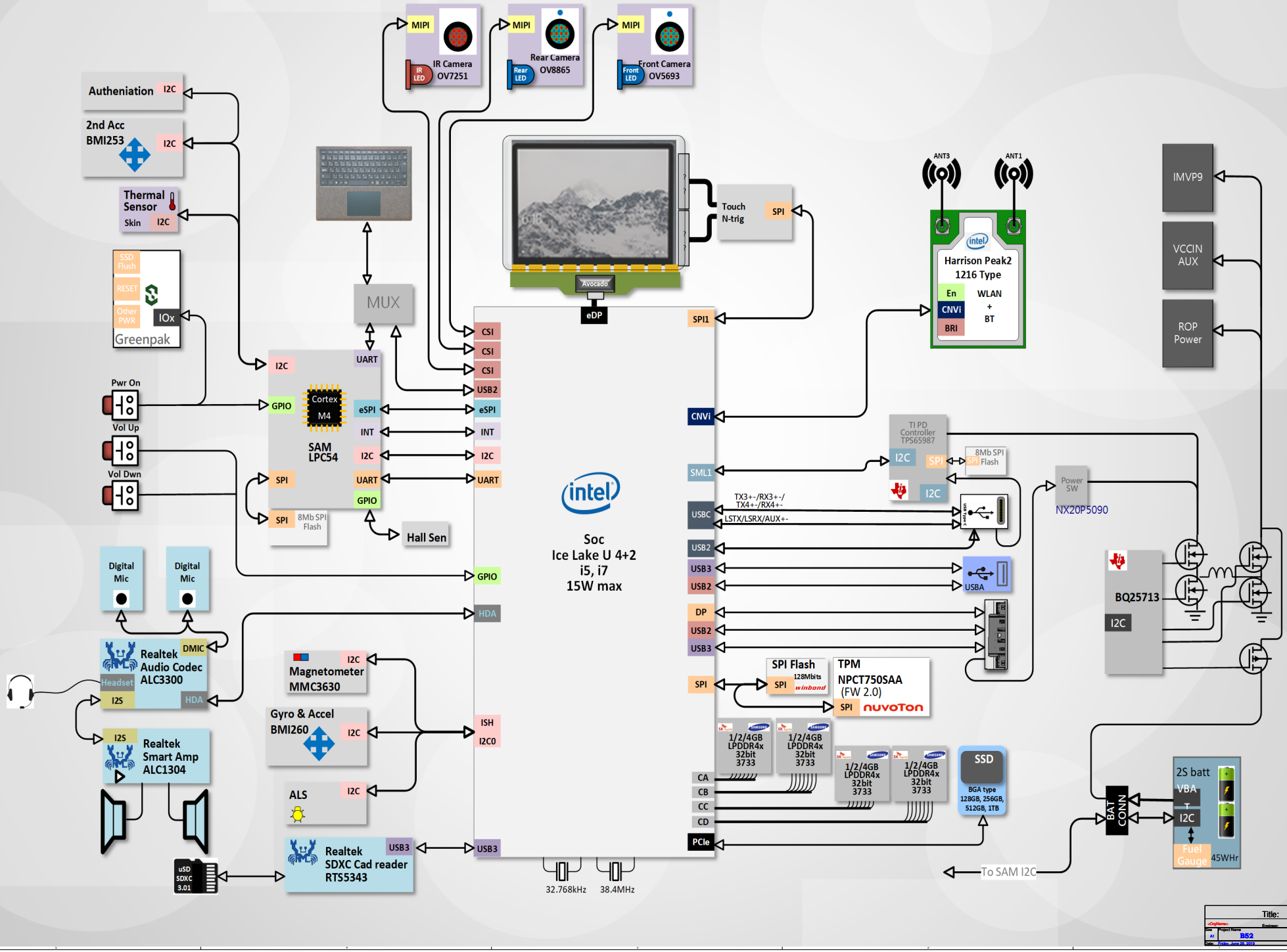
Property: BUILD-OPT
DNP = Do Not Place

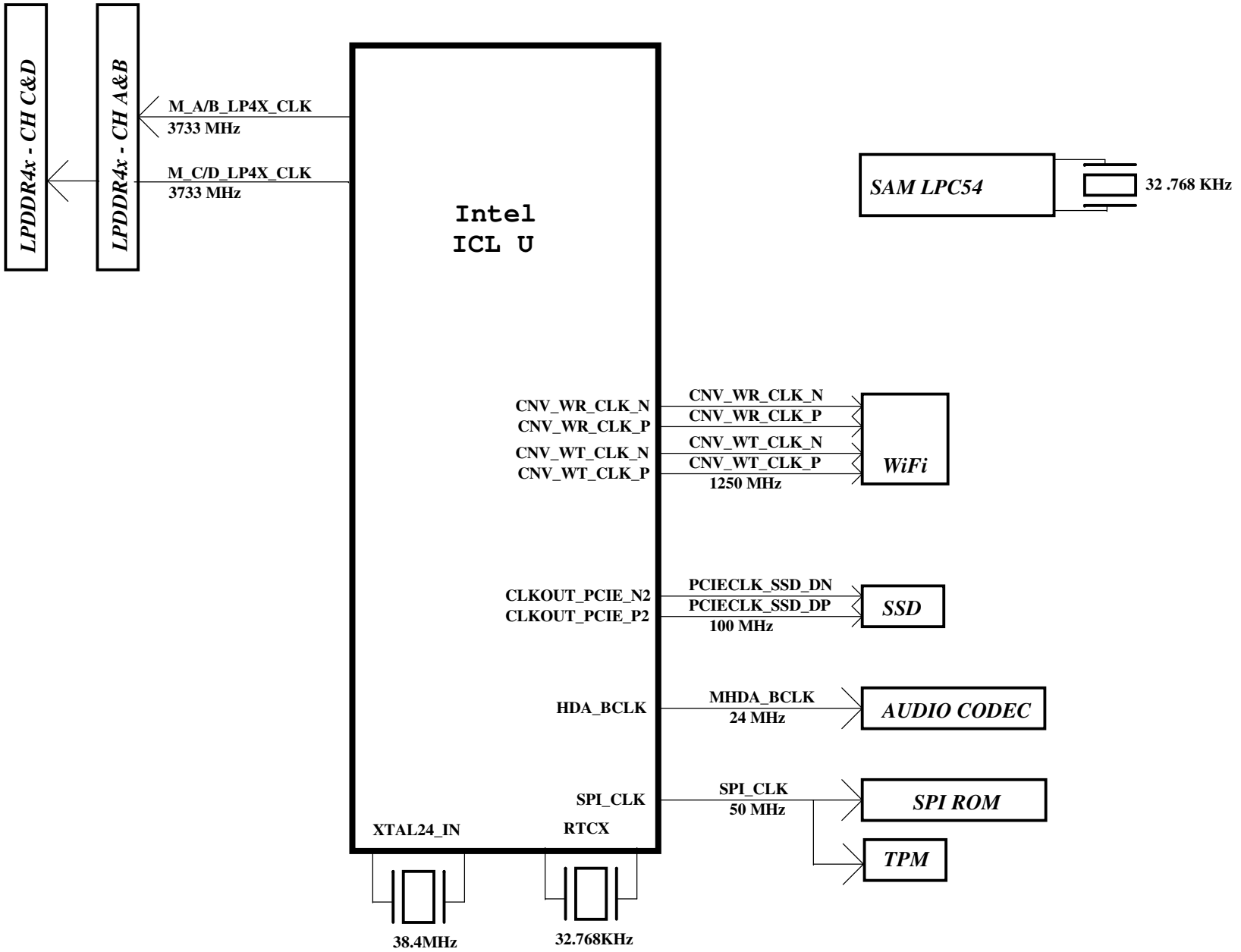
DBG_S – Replace with board short for MP
DBG_R – Replace with lower cost component for MP
DBG_N – Install for Non-Debug Builds
DBG_D – Remove from BOM (Depopulate) for MP
DBG_T – Used for Telemetry in MP as needed
DBG_TS – Used for Telemetry in MP as needed. This part needs to be replaced with a short if telemetry is not needed.

<Core Design>

Title:	Table of Contents
Engineer:	<OrgAddr1>
Size: A3	Project Name: B52
Rev:	<RevCode>
Date: Friday, June 28, 2019	Sheet 1 of 82

Item	Date	SCH Page/Title/Function	PCB Rev.	Designator (Reference)	Reason	Notes	Action/Details of change	Status (open/close)	Change Impact		
									BOM	SCH	PCB/Layout
1	2019/1/11	34. SAM Power, ADC, & Debug	R1.01	Microsoft	A SAM's GPIO missed for Blade detection.		Connect U3400 PIO1_21 (BLADE_RX) to PIO1_0	CLOSE		V	
2	2019/1/11	32. On Board-Sensors	R1.01	Microsoft	I2C port selection miss-alignment with SW team on Ambient Color Sensor.		Move I2C connection from ISH to PCH I2C4 EV0.9 design ALS_SCL/SDL were connect to PCH_SENSOR_ISH_SCL/ PCH_SENSOR_ISH_SDA, now is connect to I2C4_SDA/ I2C4_SCL and reserved PU RES.	CLOSE		V	
3	2019/1/11	10. CPU(1)_Disp,Type-C,MISC	R1.01	Microsoft	Wrong connection on chipset DDC, SL docking DP ++(HDMI) won't be functional.		TCPC port 4 for SL40, so we should use DDP4. SLDP_CTRL_CLK change from U1001.DK34 to DN33 (DDP3 DDP4) SLDP_CTRL_DATA change from U1001.DL34 to DL33 (DDP3 DDP4)	CLOSE		V	
4	2019/1/23	51. eDP connector	R1.01	Microsoft	HW & SW miss-alignment on LCD backlight control. If no change, instant on LOGO will become darker.		Have some BOM change for this item on Page 51. non-stuff: R5180、R5118、R5120、R5123、R5122、R5121、C5101、U5102 stuff: U5103、C5115、R5116、R5114、R5117、R5110、R5115	CLOSE		V	
5	2019/1/23	71. SL1 SIGNALS	R1.01	Microsoft	Wrong connection on DP lane connection on SL. Low resolution panel will malfunction with SL dock + DP monitor.		U7910 DP input and output lane swap from DATA0- DATA2- DATA1- DATA3 to DATA0- DATA1- DATA2- DATA3 Swap U7910 AUX P/N connection: from SL_AUX_DP--> AUXn, SL_AUX_DN--> AUXp to SL_AUX_DP--> AUXp, SL_AUX_DN--> AUXn	CLOSE		V	
6	2019/1/23	49. Camera IR	R1.01	Microsoft	Wrong connection on camera crystal control signal.		Change CAM_IR_PWR_EN from X4901.4 to X4901.1	CLOSE		V	
7	2019/1/24	48. SDXC	R1.01	Microsoft	Since SDXC BtoB connector will EOL, we change connector to (MOLEX/503772-1620).		7. Since SDXC BtoB connector (J4801) will be EOL, we change another connector to (MOLEX/503772-1620)	CLOSE		V	
8	2019/1/24	25. PCH(6)_CPU,GPIO,MISC	R1.01	Microsoft	DNP U2505 on page 25(FCU is no need in EV1 stage)		C2501、U2502、R2554、R2558 BOM change to DNP	CLOSE		V	
9	2019/1/24	32. On Board-Sensors	R1.01	Microsoft	BOM change of hall sensor		R3202、R3204、R3205、R3206 BOM change from DNP to DBG_D for debug easier.	CLOSE		V	
10	2019/1/25	38. TPM	R1.01	Microsoft	Add PU for TPM from Vander request.		1.U1001.DP15 (PCH_SERIRQ) add PU 10K to +1P8VSB. 2.U3801.20 (SPI_TPM_CS#) add PU 10K to +1P8V_TPM.	CLOSE		V	
11	2019/1/25	21. PCH(2)_CLK,SMB,eSPI, SPI	R1.01	Microsoft	Remove Debug component		1.Remove J2102 portiom R2166、R2712、R2168、R2171、R2165、R2170、R2167、R2164、R2169 2.Remove R2157、R2114、R2131、R2116、R2165、R2136、R2139、R2159、R2160、R2161、R2162、R2156 3.Remove J2101 portion R2163、R21272、R2173 Q2101	CLOSE		V	
12	2019/1/25	43. SSD BGA Type	R1.01	Microsoft	Samsung SSD circuit need to improve to schematic.		1.add Voltage Detector ciriuit and connected to W17 (U4303) 2.Add Test Point for TCK and TMS(TP4329/TP4330) 3.add 10uF for internal LDO U16/R16(C4342) 4.add test point for L16 (TP4328) 5.add Pull-up Resistor for N16 (R4352) 6.change cap and resistor value R4335 from 0ohm to 243ohm、C4340/C4341 from 5.6pf to 10pf	CLOSE		V	
13	2019/1/29	59. +5VSB & +3P3VSB	R1.01	Microsoft	eparate the EN pin of +5VSB from +3P3VSB		To connect SAM PIO4_11 to EN of +5VSB and PIO0_0 to +5VSB power good signal. And in case something wrong, please keep 0R option to go back solution	CLOSE		V	
14	2019/1/30	79. Type C PD controller	R1.01	Microsoft	Apple charger failing to work under dead battery condition		DNP the PU R7916 to SAM_3P3V_PD_EN and add a PD instead.	CLOSE		V	


MIPI
IR Camera
OV7251
IR LED
MIPI
Rear Camera
OV8865
Rear LED
MIPI
Front Camera
OV5693
Front LED
Autheniation
I2C
2nd Acc
BMI253
I2C
Thermal
Sensor
Skin
I2C
SSD Flush
RESET
Other PWR
IOx
Greenpak
MUX
Touch
N-trig
SPI
Avocado
eDP
ANT3
ANT1
Harrison Peak2
1216 Type
En
WLAN
+
BT
CNVi
BRI
IMVP9
VCCIN
AUX
ROP
Power
Pwr On
Vol Up
Vol Dwn
I2C
GPIO
UART
Cortex
M4
eSPI
INT
I2C
SPI
UART
GPIO
SAM
LPC54
SPI
8Mb SPI
Flash
Hall Sen
CSI
CSI
CSI
USB2
eSPI
INT
I2C
UART
GPIO
HDA
ISH
I2C0
USB3
SPI1
CNVi
SML1
USBC
USB2
USB3
USB2
DP
USB2
USB3
SPI
CA
CB
CC
CD
PCIe
Soc
Ice Lake U 4+2
i5, i7
15W max
32.768kHz
38.4MHz
TI PD
Controller
TPS65987
I2C
SPI
8Mb SPI
Flash
I2C
TX3+-/RX3+-/
TX4+-/RX4+-
LSTX/LSRX/AUX+-
USBA
Power
SW
NX20P5090
BQ25713
I2C
SPI Flash
128Mbits
winbond
SPI
TPM
NPCT750SAA
(FW 2.0)
SPI
nuvoTon
1/2/4GB
LPDDR4x
32bit
3733
1/2/4GB
LPDDR4x
32bit
3733
1/2/4GB
LPDDR4x
32bit
3733
1/2/4GB
LPDDR4x
32bit
3733
SSD
BGA type
128GB, 256GB,
512GB, 1TB
BAT
CONN
2S batt
VBA
T
I2C
Fuel
Gauge
45WHr
To SAM I2C
Digital
Mic
Digital
Mic
Realtek
Audio Codec
ALC3300
DMIC
Headset
I2S
HDA
I2C
Magnetometer
MMC3630
Gyro & Accel
BMI260
I2C
ALS
I2C
I2S
Realtek
Smart Amp
ALC1304
uSD
SDXC
3.01
Realtek
SDXC Cad reader
RTS5343
USB3
Title:
BLOCK DIAGRAM
B52



<Core Design>

Title: CLCOK DISTRIBUTION

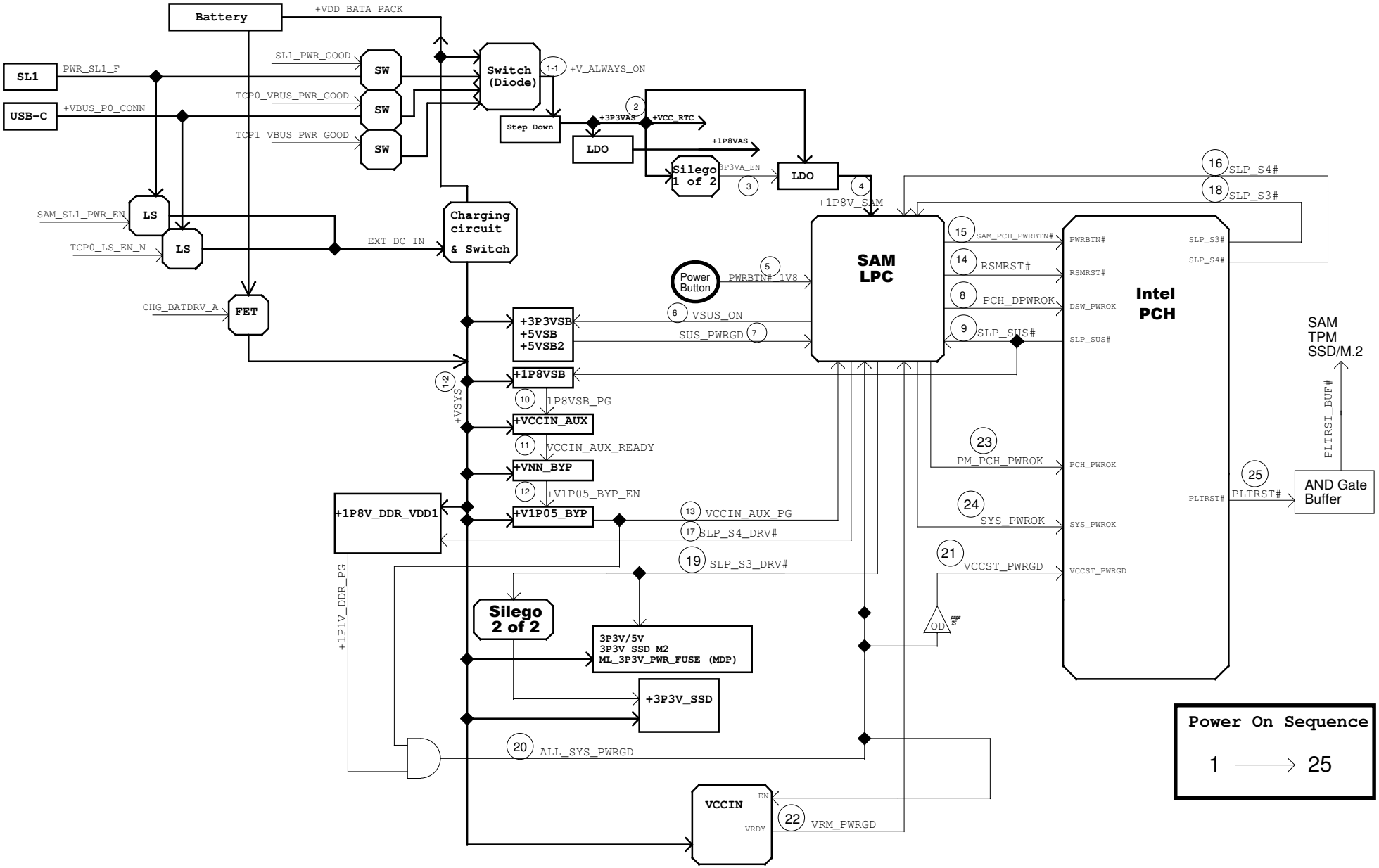
<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
A3	B52	2.89.6

Date: Friday, June 28, 2019 Sheet 4 of 82

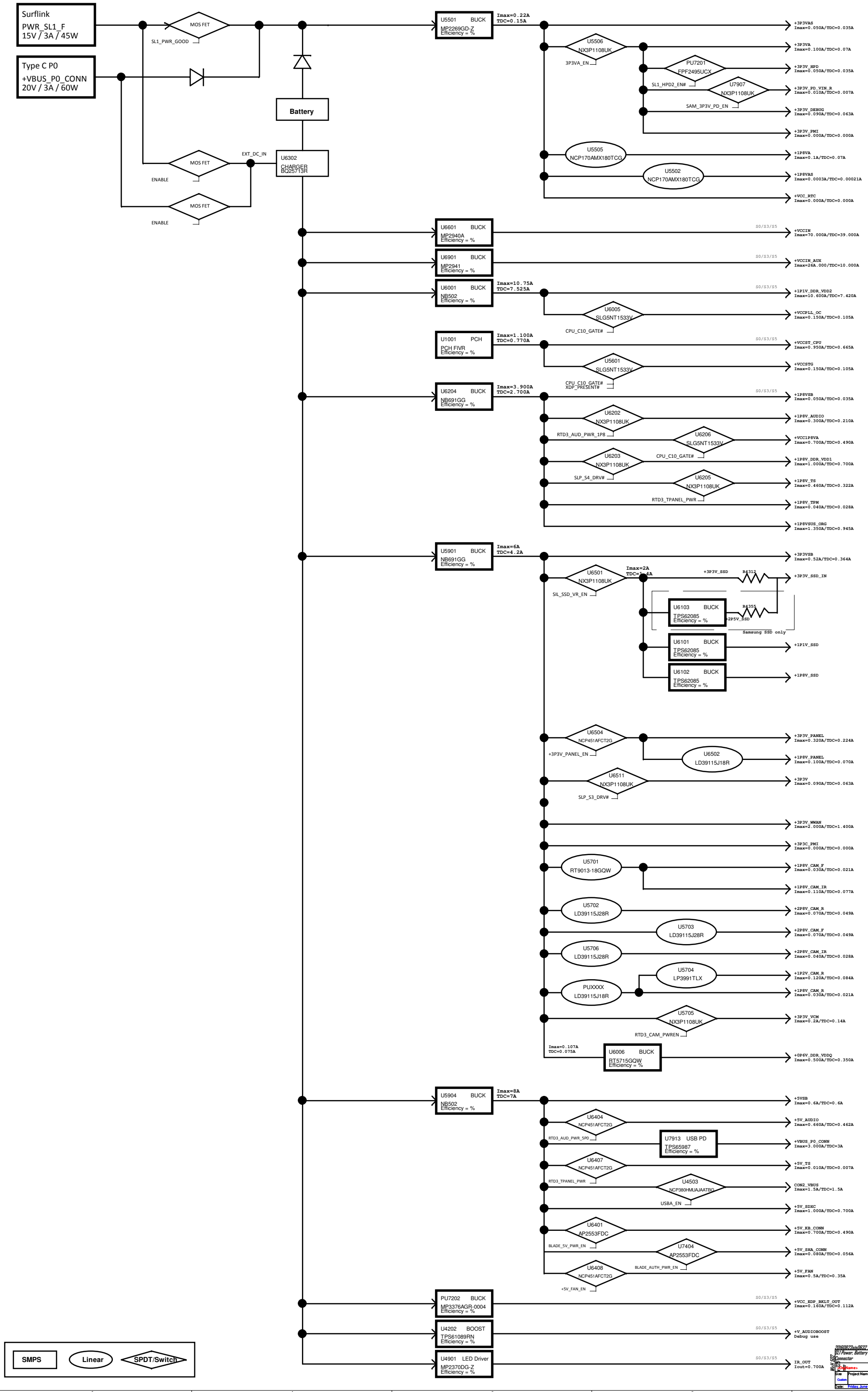
SIGNAL & RESET MAP

Last Update - Feb 13 2018



<Core Design>

Title:	SIGNAL&RESET MAP
<OrgName>	Engineer: <OrgAddr1>
Size: A2	Project Name: B52
Rev: 1.00	
Date: Friday, June 28, 2019	Sheet 5 of 52



Surflink
PWR_SL1_F
15V / 3A / 45W
Type C P0
+VBUS_P0_CONN
20V / 3A / 60W
MOS FET
SL1_PWR_GOOD
Battery
EXT_DC_IN
U6302
CHARGER
BQ25713R
ENABLE
U5501 BUCK
MP2269GD-Z
Efficiency = %
Imax=0.22A
TDC=0.15A
U5506
NX3P1108UK
3P3VA_EN
PU7201
FPF2495UCX
SL1_HPD2_EN#
U7907
NX3P1108UK
SAM_3P3V_PD_EN
U5505
NCP170AMX180TCG
U5502
NCP170AMX180TCG
+3P3VAS
Imax=0.050A/TDC=0.035A
+3P3VA
Imax=0.100A/TDC=0.07A
+3P3V_HPD
Imax=0.050A/TDC=0.035A
+3P3V_PD_VIN_R
Imax=0.010A/TDC=0.007A
+3P3V_DEBUG
Imax=0.090A/TDC=0.063A
+3P3V_PMI
Imax=0.000A/TDC=0.000A
+1P8VA
Imax=0.1A/TDC=0.07A
+1P8VAS
Imax=0.0003A/TDC=0.00021A
+VCC_RTC
Imax=0.000A/TDC=0.000A
U6601 BUCK
MP2940A
Efficiency = %
S0/S3/S5
+VCCIN
Imax=70.000A/TDC=39.000A
U6901 BUCK
MP2941
Efficiency = %
S0/S3/S5
+VCCIN_AUX
Imax=26A.000/TDC=10.000A
U6001 BUCK
NB502
Efficiency = %
Imax=10.75A
TDC=7.525A
S0/S3/S5
+1P1V_DDR_VDD2
Imax=10.600A/TDC=7.420A
U6005
SLG5NT1533V
CPU_C10_GATE#
+VCCPLL_OC
Imax=0.150A/TDC=0.105A
U1001 PCH
PCH FIVR
Efficiency = %
Imax=1.100A
TDC=0.770A
S0/S3/S5
+VCCST_CPU
Imax=0.950A/TDC=0.665A
U5601
SLG5NT1533V
CPU_C10_GATE#
XDP_PRESENT#
+VCCSTG
Imax=0.150A/TDC=0.105A
U6204 BUCK
NB691GG
Efficiency = %
Imax=3.900A
TDC=2.700A
S0/S3/S5
+1P8VSB
Imax=0.050A/TDC=0.035A
U6202
NX3P1108UK
+1P8V_AUDIO
Imax=0.300A/TDC=0.210A
RTD3_AUD_PWR_1P8
U6206
SLG5NT1533V
+VCC1P8VA
Imax=0.700A/TDC=0.490A
U6203
NX3P1108UK
CPU_C10_GATE#
+1P8V_DDR_VDD1
Imax=1.000A/TDC=0.700A
SLP_S4_DRV#
U6205
NX3P1108UK
+1P8V_TS
Imax=0.460A/TDC=0.322A
RTD3_TPANEL_PWR
+1P8V_TPM
Imax=0.040A/TDC=0.028A
+1P8VSUS_ORG
Imax=1.350A/TDC=0.945A
U5901 BUCK
NB691GG
Efficiency = %
Imax=6A
TDC=4.2A
+3P3VSB
Imax=0.52A/TDC=0.364A
U6501
NX3P1108UK
SIL_SSD_VR_EN
Imax=2A
+3P3V_SSD
R4312
+3P3V_SSD_IN
U6103 BUCK
TPS62085
Efficiency = %
R4355
+2P5V_SSD
Samsung SSD only
U6101 BUCK
TPS62085
Efficiency = %
+1P1V_SSD
U6102 BUCK
TPS62085
Efficiency = %
+1P8V_SSD
U6504
NCP451AFCT2G
+3P3V_PANEL_EN
+3P3V_PANEL
Imax=0.320A/TDC=0.224A
U6502
LD39115J18R
+1P8V_PANEL
Imax=0.100A/TDC=0.070A
U6511
NX3P1108UK
SLP_S3_DRV#
+3P3V
Imax=0.090A/TDC=0.063A
+3P3V_WWAN
Imax=2.000A/TDC=1.400A
+3P3C_PMI
Imax=0.000A/TDC=0.000A
U5701
RT9013-18GQW
+1P8V_CAM_F
Imax=0.030A/TDC=0.021A
+1P8V_CAM_IR
Imax=0.110A/TDC=0.077A
U5702
LD39115J28R
+2P8V_CAM_R
Imax=0.070A/TDC=0.049A
U5703
LD39115J28R
+2P8V_CAM_F
Imax=0.070A/TDC=0.049A
U5706
LD39115J28R
+2P8V_CAM_IR
Imax=0.040A/TDC=0.028A
U5704
LP3991TLX
+1P2V_CAM_R
Imax=0.120A/TDC=0.084A
PUXXXX
LD39115J18R
+1P8V_CAM_R
Imax=0.030A/TDC=0.021A
U5705
NX3P1108UK
RTD3_CAM_PWREN
+3P3V_VCM
Imax=0.2A/TDC=0.14A
Imax=0.107A
TDC=0.075A
U6006 BUCK
RT5715GQW
Efficiency = %
+0P6V_DDR_VDDQ
Imax=0.500A/TDC=0.350A
U5904 BUCK
NB502
Efficiency = %
Imax=8A
TDC=7A
+5VSB
Imax=0.6A/TDC=0.6A
U6404
NCP451AFCT2G
RTD3_AUD_PWR_5P0
+5V_AUDIO
Imax=0.660A/TDC=0.462A
U7913 USB PD
TPS65987
Efficiency = %
+VBUS_P0_CONN
Imax=3.000A/TDC=3A
U6407
NCP451AFCT2G
RTD3_TPANEL_PWR
+5V_TS
Imax=0.010A/TDC=0.007A
U4503
NCP380HMUAJAATBG
USBA_EN
CON2_VBUS
Imax=1.5A/TDC=1.5A
+5V_SDXC
Imax=1.000A/TDC=0.700A
U6401
AP2553FDC
BLADE_5V_PWR_EN
+5V_KB_CONN
Imax=0.700A/TDC=0.490A
U7404
AP2553FDC
BLADE_AUTH_PWR_EN
+5V_SHA_CONN
Imax=0.080A/TDC=0.056A
U6408
NCP451AFCT2G
+5V_FAN_EN
+5V_FAN
Imax=0.5A/TDC=0.35A
PU7202 BUCK
MP3376AGR-0004
Efficiency = %
S0/S3/S5
+VCC_EDP_BKLT_OUT
Imax=0.160A/TDC=0.112A
U4202 BOOST
TPS61089RN
Efficiency = %
S0/S3/S5
+V_AUDIOBOOST
Debug use
U4901 LED Driver
MP2370DG-Z
Efficiency = %
S0/S3/S5
IR_OUT
Iout=0.700A
SMPS
Linear
SPDT/Switch

20160823sis0632 :
SL1 Power, Battery
Connector

Report errors to Steven

W x H 502 x 326

Title: POWER FLOW (1 OF 2)

<OrgName>

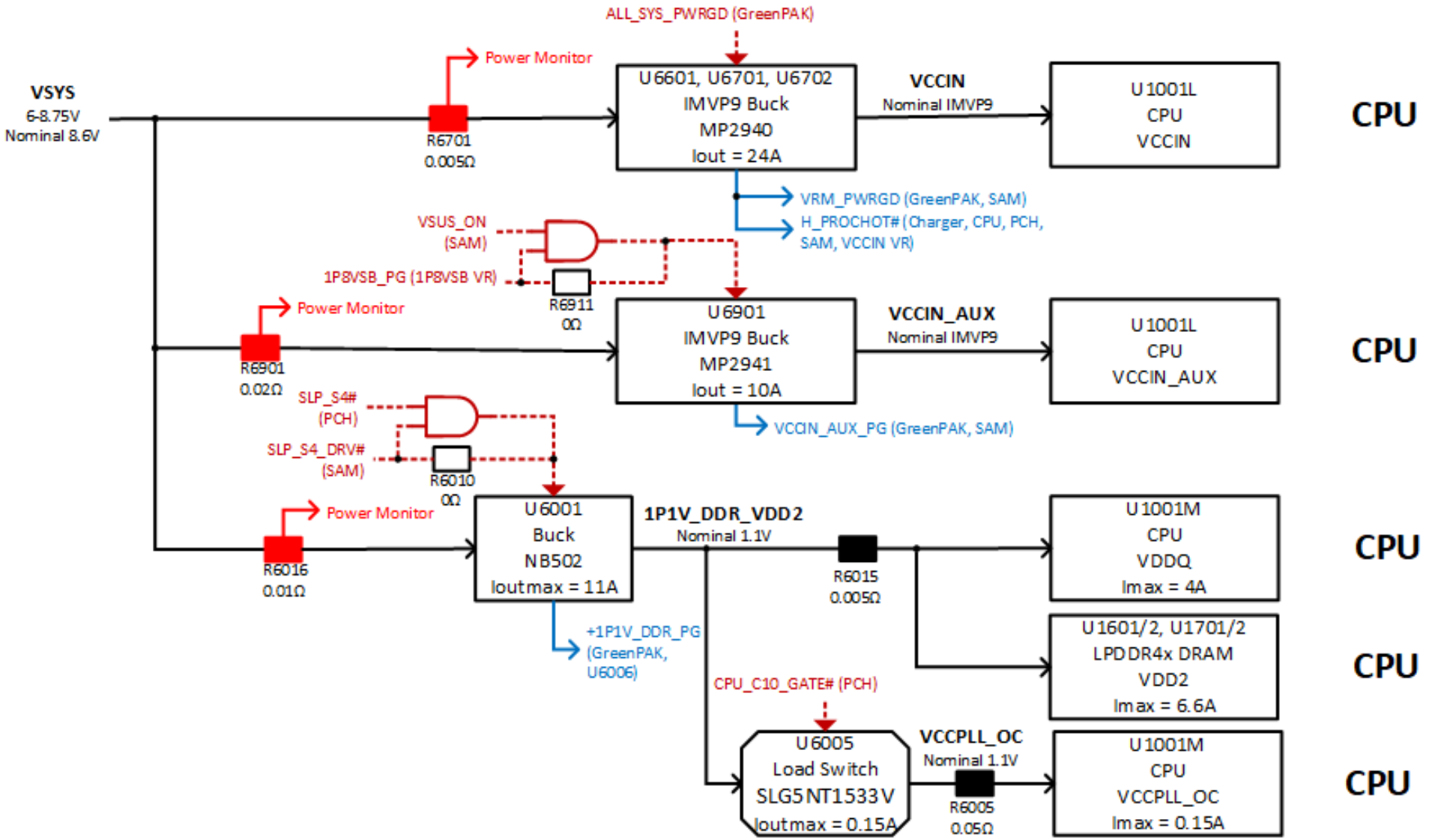
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	B52	1.00

Date: Friday, June 28, 2019 Sheet 6 of 82

LAST UPDATE – SEPT. 13 2018

CPU Power Delivery



<Core Design>

Title:	POWER FLOW(2 OF 2)		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 7 of 82		

CAD Note:

Defaults: Footprint SMD 0201, Cap tmp Coeff X5R, 1% resistors

Title:	Power States		
Engineer:	<OrgAddr1>		
Size: A3	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 8 of 82		

For battery and charger IC, 100K
For sensors connection 400K
For PD controller 400K
For temp sensor, acc chip for pro line, 400K
For ISH, pass the sensor information to ISH, 400K

I2C & SMBUS Map

7bit Address

PCH U1001 Master

I2C5, I2C4, I2C3, I2C2, I2C1, I2C0, SML0, SML1, SMB, ISH I2C1, ISH I2C0

- I2C4_SDA / I2C4_CLK → R3253 / R3254 → ALS_SDA / ALS_SCL → **Ambient Light (ACS) J3202** 0x39
- I2C4_SDA / I2C4_CLK → **64K EEPROM U2502** 0x??
- I2C3 → I2C_SDA_REAR_IR_CAM / I2C_SCL_REAR_IR_CAM → R2527 / R2528 → I2C_SDA_IRCAM / I2C_SCL_IRCAM → **IRCam Connector J4901** 0xC1
- I2C3 → I2C_SDA_REAR_IR_CAM / I2C_SCL_REAR_IR_CAM → R2520 / R2521 → I2C_SDA_RCAM / I2C_SCL_RCAM → **RCam Connector J5301** CAM: 0x10 VCM: 0X0C
- I2C2 → I2C_SDA_FCAM_R / I2C_SCL_FCAM_R → R2522 / R2523 → I2C_SDA_FCAM / I2C_SCL_FCAM → **FCam Connector J5401** 0x36
- I2C1 → PMI_I2C_SDA / PMI_I2C_SCL → R2854 / R2855 → PMI1_I2C_SDA_R / PMI1_I2C_SCL_R → **PwrMonitor0 U2813** 0x10; **PwrMonitor1 U2802** 0x12; **PwrMonitor2 U2803** 0x14
- I2C0 → PANEL_I2C_SDA / PANEL_I2C_SCL → R2597 / R2598 → EDP_I2C_SDA / EDP_I2C_SCL → **EDP Connector P5101** 0x3E&0x44&0x66
- SML1 → **Backlight PU7202** 0x28 → PR7220 / PR7222
- SMB: SMBDAT / SMBCLK → R2103 / R2102

Debug Conn J3302

- SAMTX_PCHRX / PCHTX_SAMRX
- SAM_PD_SDA / SAM_PD_SCL
- PANEL_I2C_SDA / PANEL_I2C_SCL
- SAM_SEN_SDA / SAM_SEN_SCL
- PMI_I2C_SDA / PMI_I2C_SCL
- POWER_SMB_SDA / POWER_SMB_SCL
- PCH_SAM_SNSR_SDA / PCH_SAM_SNSR_SCL

ISH I2C1 / ISH I2C0 → PCH_ISH_I2C0_SDA / PCH_ISH_I2C0_SCL → Q3205A / Q3205B → PCH_SAM_SNSR_SDA / PCH_SAM_SNSR_SCL → R2503 / R2506

- R3519 / R3520 → **Accel & Gyro U3207** 0x68 (R3227 / R3229)
- R3522 / R3524

PD Controller U7902: I2C2 0x38 / I2C1 0x20

PD_I2C2_SDA / PD_I2C2_SCL

SAM U3400: FC7, FC8, FC3, FC9, FC6, FC2

- FC7 → R3511 / R3512 → SAM_PD_SDA / SAM_PD_SCL
- FC3 → BAT_SDAr / BAT_SCLr → R3502 / R3503 → POWER_SMB_SDA / POWER_SMB_Scl → L7003 / L7004 → BAT_SMCLK / BAT_SMDATA → **Battery J7001** 0x0B
- FC6 → R3534 / R3535 → CHARGER_SDA / CHARGER_SCL → **Charger U6302** 0x6b
- FC2 → R3517 / R3525 → IMVP_SDA_P / IMVP_SCL_P → **IMVP9 U6601** 0xE1

SAM_SEN_SDA / SAM_SEN_SCL → R3515 / R3516

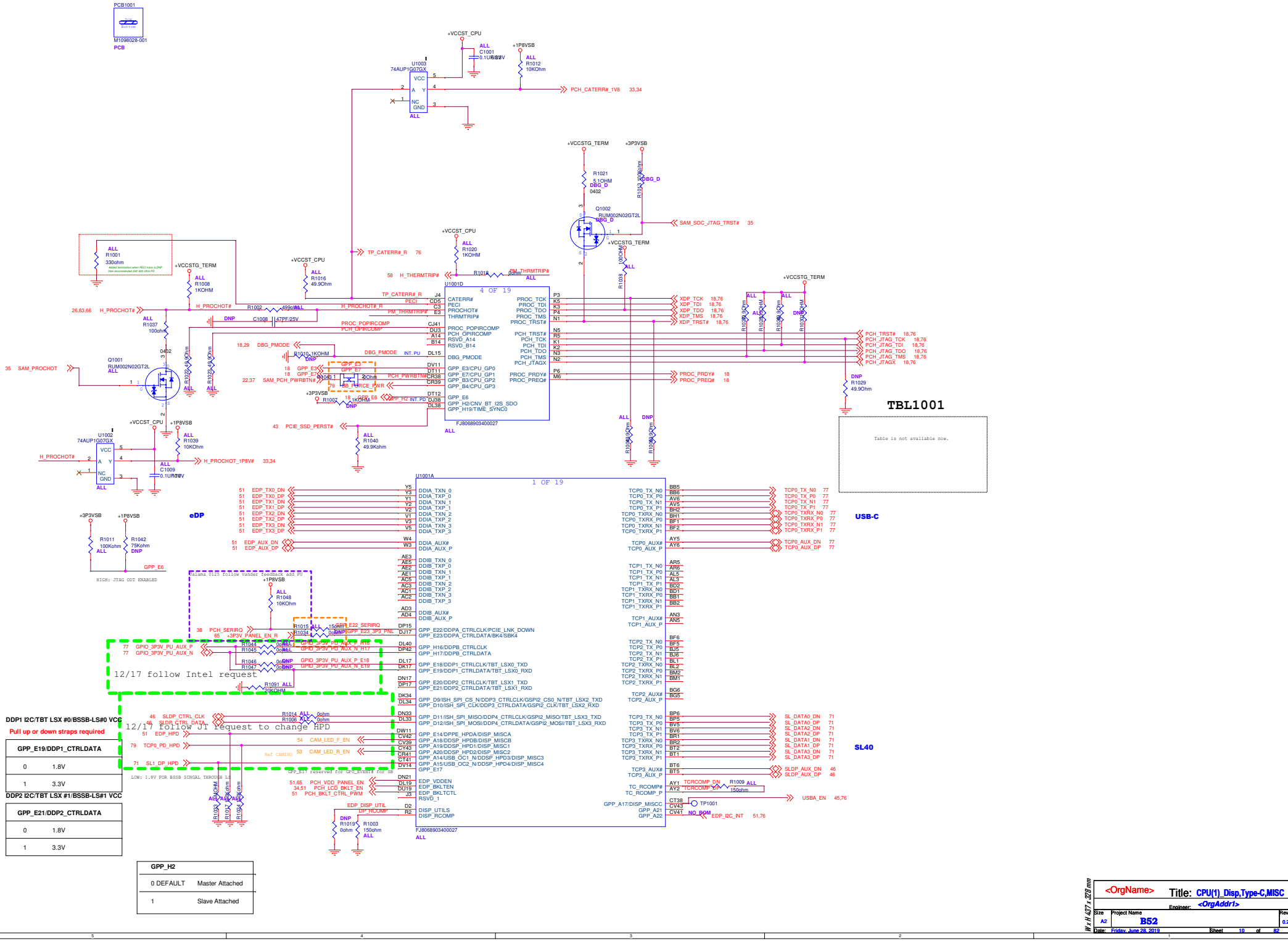
- **Magnetometer U3208** 0x30 (R3230 / R3228)
- **Ambient Light (ALS) J3202** 0x44 (R3224 / R3226)
- **Skin Temp U3904** 0x4B
- **Skin Temp U3903** 0x4A
- **Skin Temp U3902** 0x49
- **Skin Temp U3901** 0x48

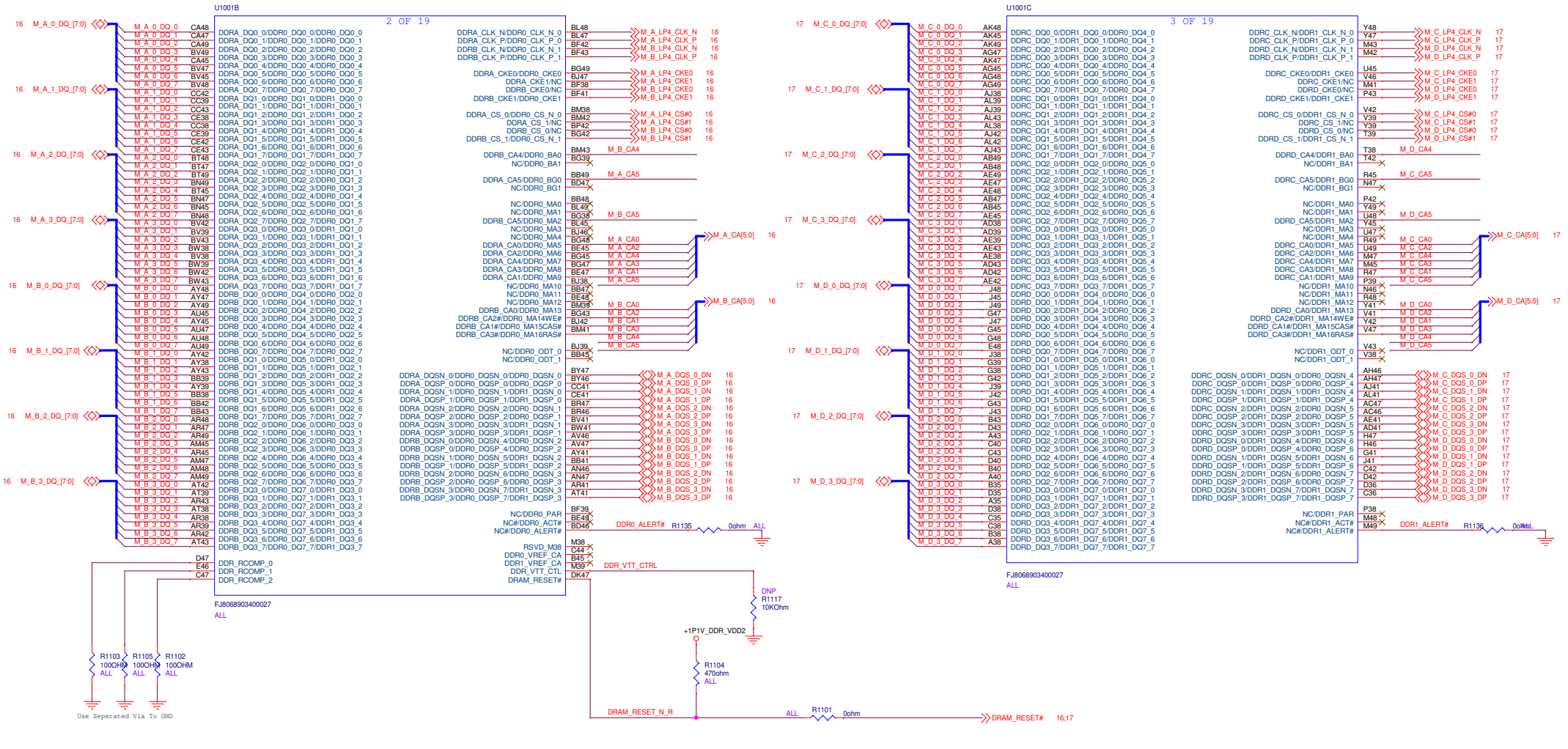
R7401 / R7403 → **Blade Accel U7408** 0x18

Authentication U3101 0x60

TS_A_I2C_SDA_CON_NC / TS_A_I2C_SCL_CON_NC → **Touch Conn J3001** 0x60

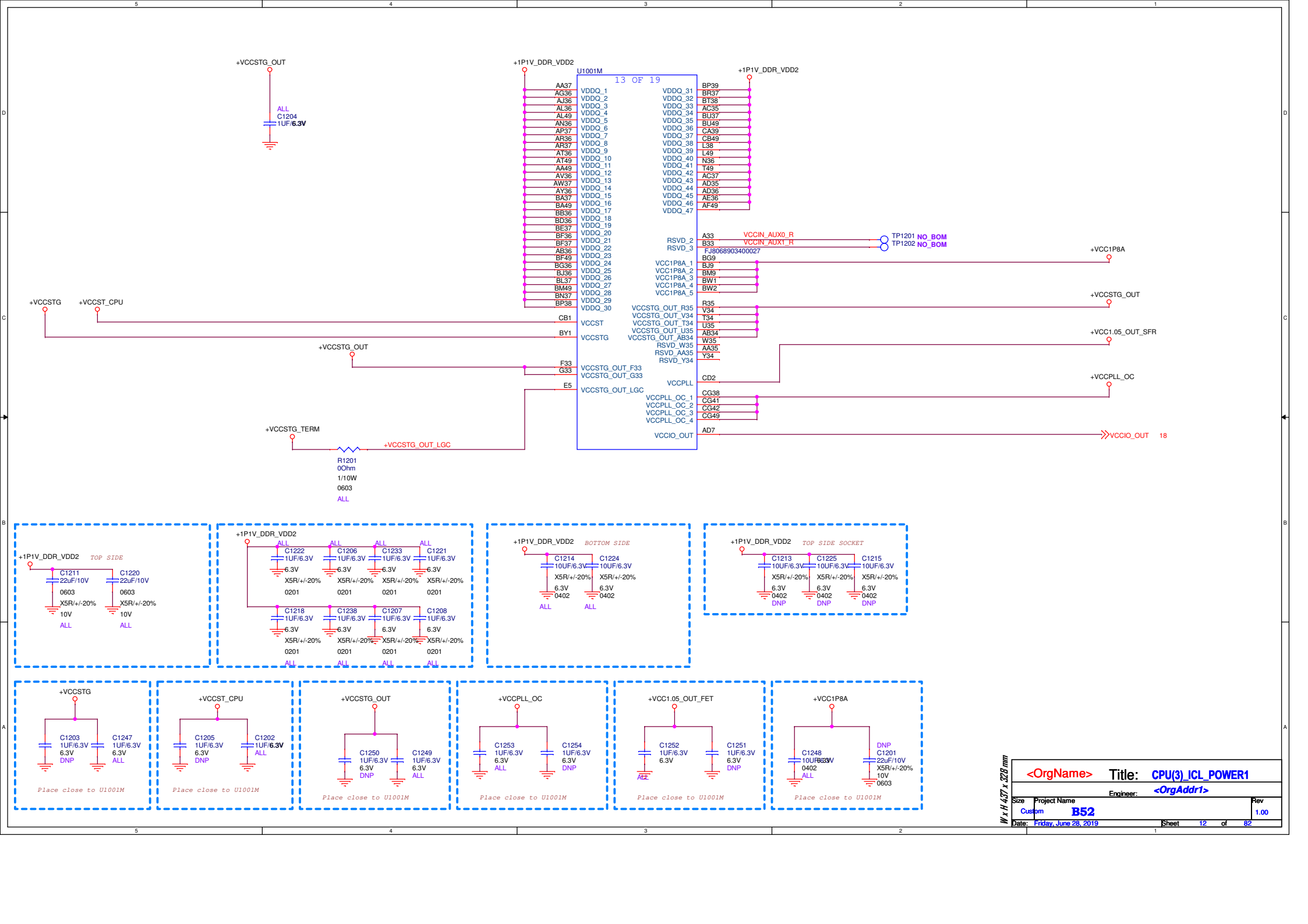
Title:	09. I2C MAP
Engineer:	<OrgAddr1>
Size: A2	Project Name: B52
Rev:	1.00
Date:	Friday, June 28, 2019
Sheet	9 of 82

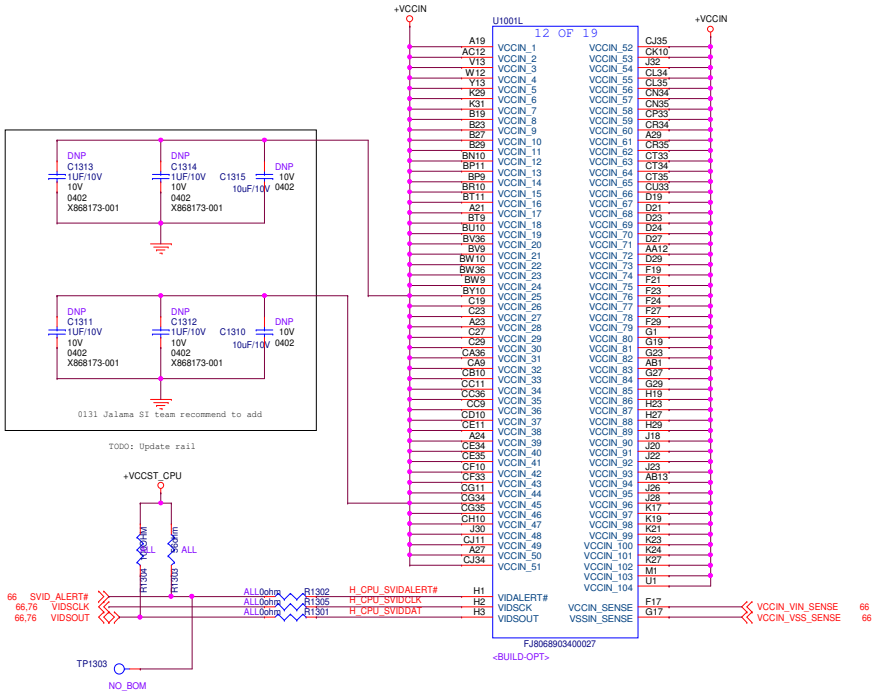

PCB1001
M1098028-001
PCB
U1003
74AUP1G07GX
+VCCST_CPU
+1P8VSB
C1001
0.1UF/6.3V
R1012
10KOhm
PCH_CATERRB#_1V8 33,34
+VCCSTG_TERM
+3P3VSB
R1021
5.1OHM
DBG_D
0402
R1043 100KOhm
Q1002
RUM002N02GT2L
SAM_SOC_JTAG_TRST# 35
TP_CATERR#_R 76
R1020
1KOHM
58 H_THERMTRIP#
R1018
0ohm
PM_THRMTRIP#
ALL
R1001
330ohm
Added termination when PECI trans is DNP
Use recommended 200~60 Ohm PD
R1008
1KOHM
R1016
49.9Ohm
H_PROCHOT#
R1002
499ohm
H_PROCHOT#_R
TP_CATERR#_R
PECI
PM_THRMTRIP#
C1008
47PF/25V
DNP
R1037
100ohm
0402
R1022 49.9Ohm
R1023 49.9Ohm
Q1001
RUM002N02GT2L
35 SAM_PROCHOT
18,29 DBG_PMODE
R1010 1KOHM
DBG_PMODE
INT.PU
18 GPP_E3
18 GPP_E7
R1040
2Ohm
22,37 SAM_PCH_PWRBTN#
PCH_PWRBTN#
79 EC_FORCE_PWR
R1007
1KOHM
GPP_E6
GPP_H2 INT_PD
43 PCIE_SSD_PERST#
R1040
49.9Kohm
U1001D
4 OF 19
CATERR#
PECI
PROCHOT#
THRMTRIP#
PROC_POPIRCOMP
PCH_OPIRCOMP
RSVD_A14
RSVD_B14
DBG_PMODE
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_E6
GPP_H2/CNV_BT_I2S_SDO
GPP_H19/TIME_SYNC0
FJ8068903400027
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_TRST#
PCH_TCK
PCH_TDI
PCH_TDO
PCH_TMS
PCH_JTAGX
PROC_PRDY#
PROC_PREQ#
XDP_TCK 18,76
XDP_TDI 18,76
XDP_TDO 18,76
XDP_TMS 18,76
XDP_TRST# 18,76
R1032 0ohm
R1034 0ohm
R1036 0ohm
R1030 0ohm
PCH_TRST# 18,76
PCH_JTAG_TCK 18,76
PCH_JTAG_TDI 18,76
PCH_JTAG_TDO 18,76
PCH_JTAG_TMS 18,76
PCH_JTAGX 18,76
R1029
49.9Ohm
TBL1001
Table is not available now.
R1035 0ohm
R1038 0ohm
U1002
74AUP1G07GX
H_PROCHOT#
H_PROCHOT_1P8V# 33,34
C1009
0.1UF/6.3V
U1001A
1 OF 19
eDP
51 EDP_TX0_DN
51 EDP_TX0_DP
51 EDP_TX1_DN
51 EDP_TX1_DP
51 EDP_TX2_DN
51 EDP_TX2_DP
51 EDP_TX3_DN
51 EDP_TX3_DP
51 EDP_AUX_DN
51 EDP_AUX_DP
DDIA_TXN_0
DDIA_TXP_0
DDIA_TXN_1
DDIA_TXP_1
DDIA_TXN_2
DDIA_TXP_2
DDIA_TXN_3
DDIA_TXP_3
DDIA_AUX#
DDIA_AUX_P
USB-C
TCP0_TX_N0 77
TCP0_TX_P0 77
TCP0_TX_N1 77
TCP0_TX_P1 77
TCP0_TXRX_N0 77
TCP0_TXRX_P0 77
TCP0_TXRX_N1 77
TCP0_TXRX_P1 77
TCP0_AUX_DN 77
TCP0_AUX_DP 77
R1011
100Kohm
R1042
75Kohm
DNP
GPP_E6
HIGH: JTAG ODT ENABLED
Liliana 0125 follow Vander feedback add PU
+1P8VSB
R1048
10KOhm
38 PCH_SERIRQ
R1015 150ohm
R1034 0ohm
GPP_E22_SERIRQ
65 +3P3V_PANEL_EN_R
GPP_E23_3P3_PNL
77 GPIO_3P3V_PU_AUX_P
77 GPIO_3P3V_PU_AUX_N
R1044 0ohm
R1045 0ohm
GPIO_3P3V_PU_AUX_P_H17
GPIO_3P3V_PU_AUX_N_H17
R1046 0ohm
R1047 0ohm
GPIO_3P3V_PU_AUX_P_E18
GPIO_3P3V_PU_AUX_N_E19
12/17 follow Intel request
R1091
20KOHM
GPP_E22/DDPA_CTRLCLK/PCIE_LNK_DOWN
GPP_E23/DDPA_CTRLDATA/BK4/SBK4
GPP_H16/DDPB_CTRLCLK
GPP_H17/DDPB_CTRLDATA
GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD
GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD
GPP_D9/ISH_SPI_CS_N/DDP3_CTRLCLK/GSPI2_CS0_N/TBT_LSX2_TXD
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/GSPI2_CLK/TBT_LSX2_RXD
GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/GSPI2_MISO/TBT_LSX3_TXD
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/GSPI2_MOSI/TBT_LSX3_RXD
GPP_E14/DPPE_HPDA/DISP_MISCA
GPP_A18/DDSP_HPDB/DISP_MISCB
GPP_A19/DDSP_HPD1/DISP_MISC1
GPP_A20/DDSP_HPD2/DISP_MISC2
GPP_A14/USB_OC1_N/DDSP_HPD3/DISP_MISC3
GPP_A15/USB_OC2_N/DDSP_HPD4/DISP_MISC4
GPP_E17
GPP_E21 reserved for SPI_AVAIL for 35
EDP_VDDEN
EDP_BKLTEN
EDP_BKLTCTL
RSVD_I
DISP_UTILS
DISP_RCOMP
FJ8068903400027
SL40
SL_DATA0_DN 71
SL_DATA0_DP 71
SL_DATA2_DN 71
SL_DATA2_DP 71
SL_DATA1_DN 71
SL_DATA1_DP 71
SL_DATA3_DN 71
SL_DATA3_DP 71
SLDP_AUX_DN 46
SLDP_AUX_DP 46
TCRCOMP_DN
TCRCOMP_DP
R1009 150ohm
USBA_EN 45,76
TP1001
NO_POM
EDP_I2C_INT 51,76
DDP1 I2C/TBT LSX #0/BSSB-LS#0 VCC
Pull up or down straps required
GPP_E19/DDP1_CTRLDATA
0 1.8V
1 3.3V
DDP2 I2C/TBT LSX #1/BSSB-LS#1 VCC
GPP_E21/DDP2_CTRLDATA
0 1.8V
1 3.3V
46 SLDP_CTRL_CLK
46 SLDP_CTRL_DATA
R1014 0ohm
R1006 0ohm
12/17 follow J1 request to change HPD
51 EDP_HPD
79 TCP0_PD_HPD
54 CAM_LED_F_EN
53 CAM_LED_R_EN
71 SL1_DP_HPD
LOW: 1.8V FOR BSSB SINGAL THROUGH LS
51,65 PCH_VDD_PANEL_EN
34,51 PCH_LCD_BKLT_EN
51 PCH_BKLT_CTRL_PWM
EDP_DISP_UTIL
DP_RCOMP
R1019 0ohm
R1003 150ohm
GPP_H2
0 DEFAULT Master Attached
1 Slave Attached
<OrgName>
Title: CPU(1)_Disp,Type-C,MISC
Engineer:
<OrgAddr1>
Size A2
Project Name B52
Rev 0.23
Date: Friday, June 28, 2019
Sheet 10 of 82
W x H 437 x 325 mm

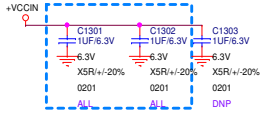


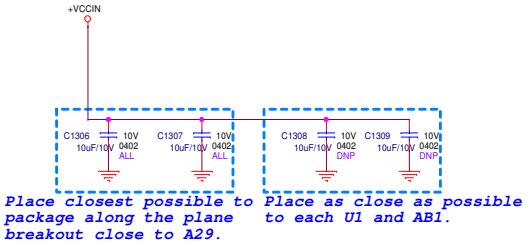
<OrgName>	Title:	CPU(2)_LPDDR4
	Engineer:	<OrgAddr1>
Size: Custom	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 11 of 82	

W x H 502 x 331 mm


+VCCSTG_OUT
ALL
C1204
1UF/6.3V
+1P1V_DDR_VDD2
U1001M
13 OF 19
VDDQ_1
VDDQ_2
VDDQ_3
VDDQ_4
VDDQ_5
VDDQ_6
VDDQ_7
VDDQ_8
VDDQ_9
VDDQ_10
VDDQ_11
VDDQ_12
VDDQ_13
VDDQ_14
VDDQ_15
VDDQ_16
VDDQ_17
VDDQ_18
VDDQ_19
VDDQ_20
VDDQ_21
VDDQ_22
VDDQ_23
VDDQ_24
VDDQ_25
VDDQ_26
VDDQ_27
VDDQ_28
VDDQ_29
VDDQ_30
VDDQ_31
VDDQ_32
VDDQ_33
VDDQ_34
VDDQ_35
VDDQ_36
VDDQ_37
VDDQ_38
VDDQ_39
VDDQ_40
VDDQ_41
VDDQ_42
VDDQ_43
VDDQ_44
VDDQ_45
VDDQ_46
VDDQ_47
+1P1V_DDR_VDD2
RSVD_2
RSVD_3
VCCIN_AUX0_R
VCCIN_AUX1_R
TP1201 NO_BOM
TP1202 NO_BOM
FJ8068903400027
VCC1P8A_1
VCC1P8A_2
VCC1P8A_3
VCC1P8A_4
VCC1P8A_5
+VCC1P8A
+VCCSTG
+VCCST_CPU
VCCST
VCCSTG
CB1
BY1
VCCSTG_OUT_R35
VCCSTG_OUT_V34
VCCSTG_OUT_T34
VCCSTG_OUT_U35
VCCSTG_OUT_AB34
RSVD_W35
RSVD_AA35
RSVD_Y34
+VCCSTG_OUT
+VCCSTG_OUT
VCCSTG_OUT_F33
VCCSTG_OUT_G33
VCCSTG_OUT_LGC
VCCPLL
+VCC1.05_OUT_SFR
+VCCPLL_OC
VCCPLL_OC_1
VCCPLL_OC_2
VCCPLL_OC_3
VCCPLL_OC_4
+VCCSTG_TERM
+VCCSTG_OUT_LGC
R1201
0Ohm
1/10W
0603
ALL
VCCIO_OUT
VCCIO_OUT 18
+1P1V_DDR_VDD2 TOP SIDE
C1211 22uF/10V 0603 X5R/+/-20% 10V ALL
C1220 22uF/10V 0603 X5R/+/-20% 10V ALL
+1P1V_DDR_VDD2
C1222 C1206 C1233 C1221 1UF/6.3V 6.3V X5R/+/-20% 0201 ALL
C1218 C1238 C1207 C1208 1UF/6.3V 6.3V X5R/+/-20% 0201 ALL
+1P1V_DDR_VDD2 BOTTOM SIDE
C1214 C1224 10UF/6.3V X5R/+/-20% 6.3V 0402 ALL
+1P1V_DDR_VDD2 TOP SIDE SOCKET
C1213 C1225 C1215 10UF/6.3V X5R/+/-20% 6.3V 0402 DNP
+VCCSTG
C1203 1UF/6.3V 6.3V DNP
C1247 1UF/6.3V 6.3V ALL
Place close to U1001M
+VCCST_CPU
C1205 1UF/6.3V 6.3V DNP
C1202 1UF/6.3V ALL
Place close to U1001M
+VCCSTG_OUT
C1250 1UF/6.3V 6.3V DNP
C1249 1UF/6.3V 6.3V ALL
Place close to U1001M
+VCCPLL_OC
C1253 1UF/6.3V 6.3V ALL
C1254 1UF/6.3V 6.3V DNP
Place close to U1001M
+VCC1.05_OUT_FET
C1252 1UF/6.3V 6.3V ALL
C1251 1UF/6.3V 6.3V DNP
Place close to U1001M
+VCC1P8A
C1248 10UF/6.3V 0402 ALL
DNP
C1201 22uF/10V X5R/+/-20% 10V 0603
Place close to U1001M
W x H 437 x 328 mm
<OrgName>
Title: CPU(3)_ICL_POWER1
Engineer: <OrgAddr1>
Size Custom
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 12 of 82

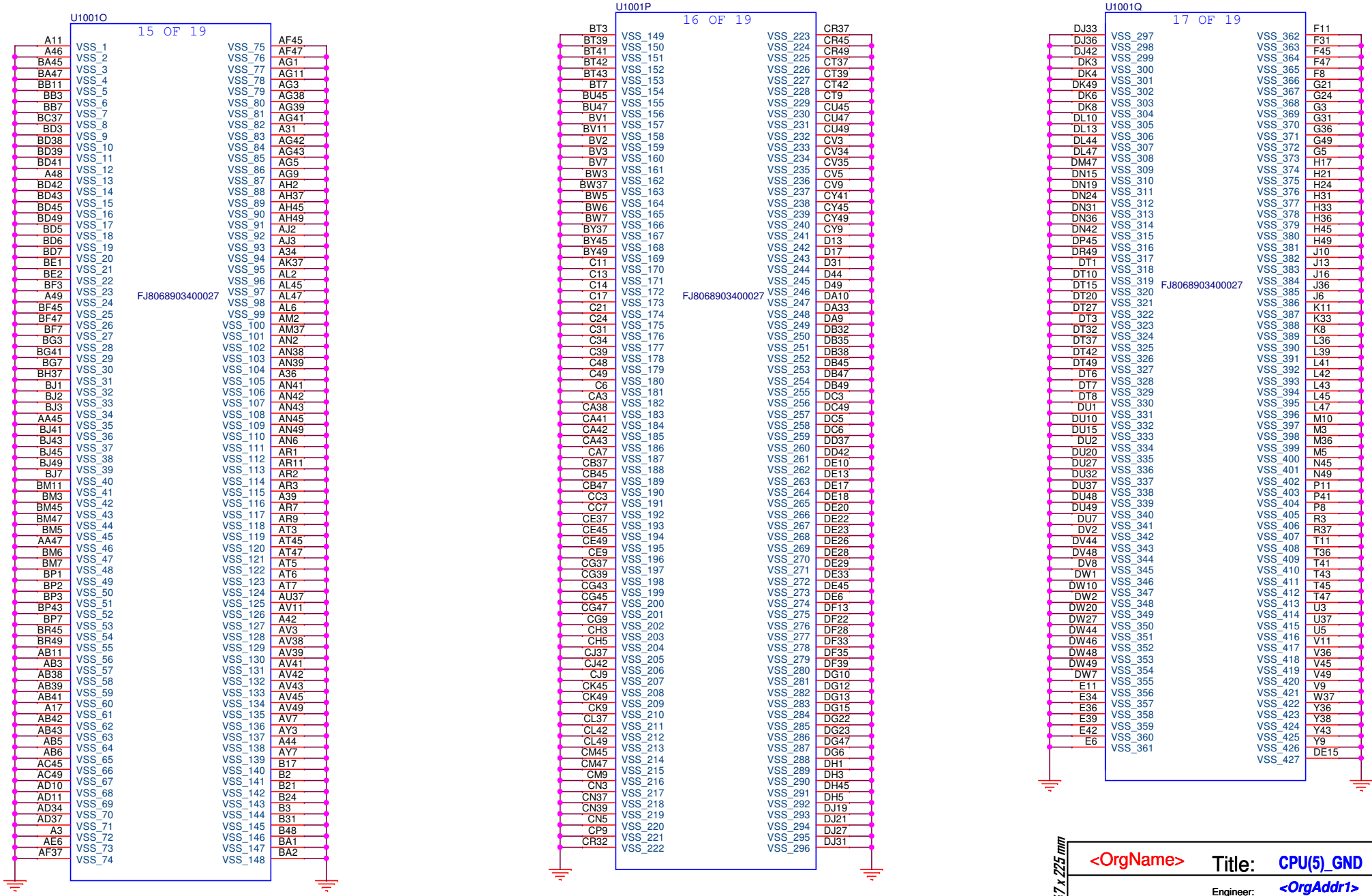




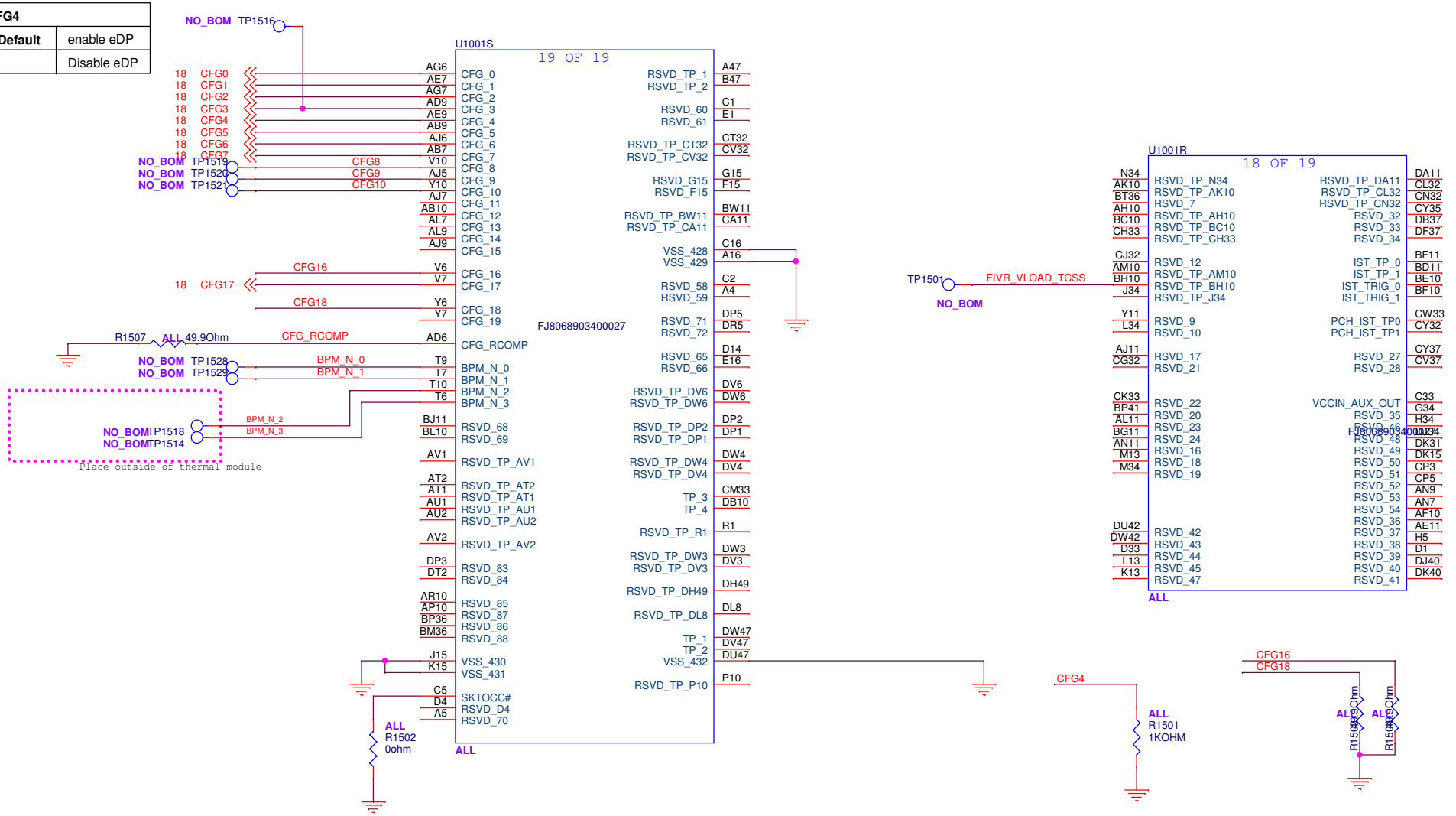


W = H.502 x .339 mm

<OrgName>	Title: CPU(4)_ICL_POWER2	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 13 of 82	


U1001O
15 OF 19
U1001P
16 OF 19
U1001Q
17 OF 19
FJ8068903400027
FJ8068903400027
FJ8068903400027
<OrgName>
Title: CPU(5)_GND
Engineer: <OrgAddr1>
Size Custom
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 14 of 82
W x H 347 x 225 mm

CFG4	
0 **Default**	enable eDP
1	Disable eDP



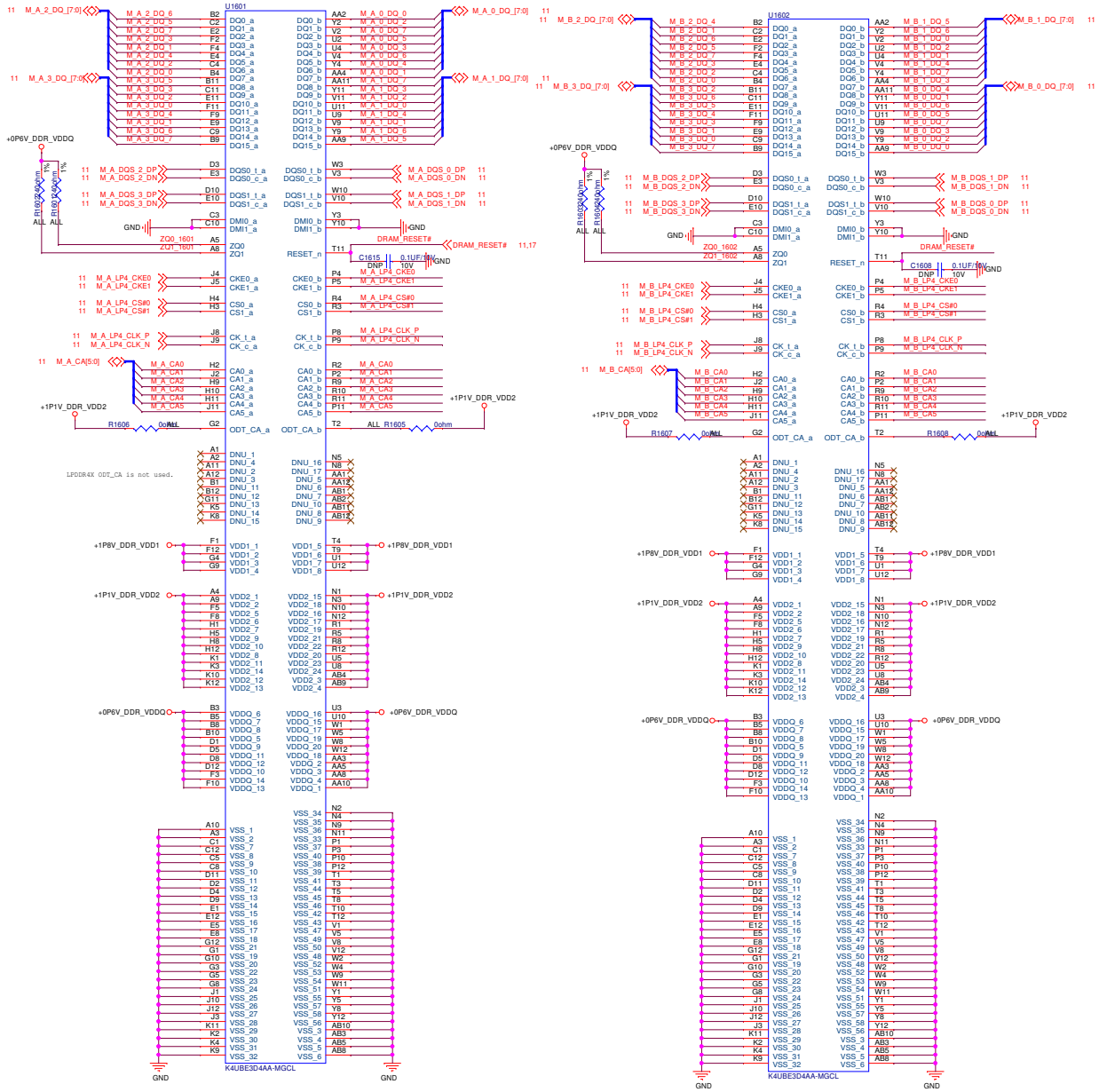
<OrgName>
Engineer: <OrgAddr1>

Title: CPU(6)_CFG,RESERVED

Size	Project Name	Rev
Custom	B52	1.00

Date: Friday, June 28, 2019 Sheet 15 of 82

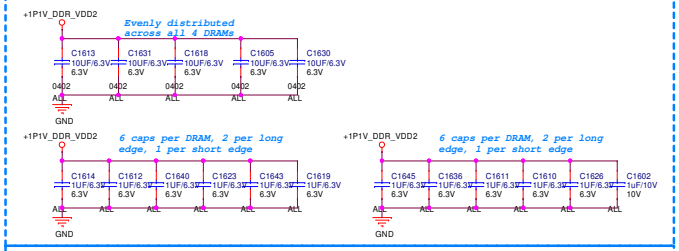
W x H 367 x 237 mm



LPDDR4X x32 **Performance**			
	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1μF (0402)
		evenly distribute among all drams	5x 10μF (0603)
	VDDQ	4 per Dram, 2 per short edge	16x 1μF (0402)
		evenly distribute among all drams	5x 10μF (0603)
	VDD1	4 per dram, 1 per corner (connected to edge and inner BGA)	16x 1μF (0402)
		Evenly distribute	5x 10μF (0603)

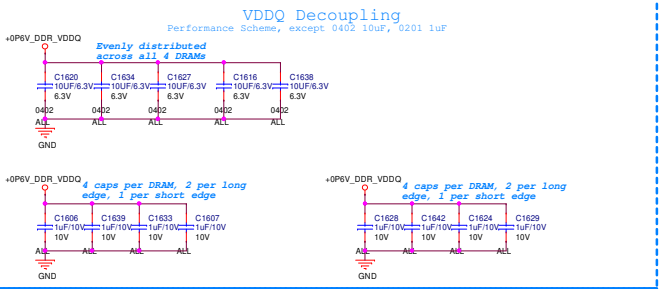
VDD2 Decoupling

Performance Scheme, except 0402 10uF, 0201 1uF



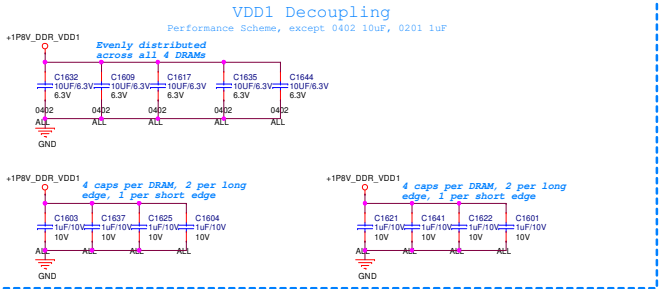
VDDQ Decoupling

Performance Scheme, except 0402 10uF, 0201 1uF



VDD1 Decoupling

Performance Scheme, except 0402 10uF, 0201 1uF



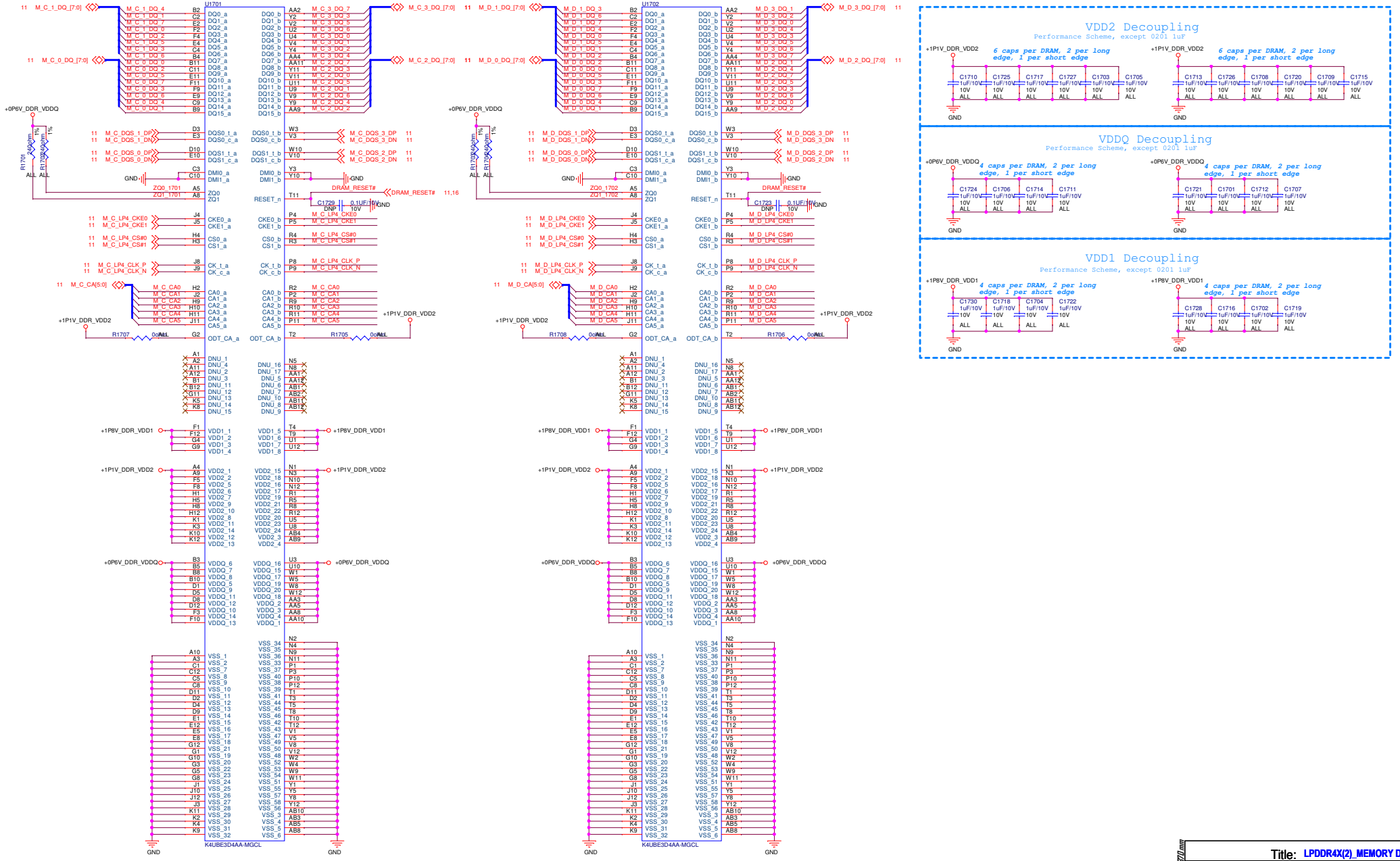
MEMORY TABLE 1601			
Manufacturer	MPN	Size	MSPN
Samsung	K4U6E3S4AA-MGCL	16Gb (2GB)	M1100585-001
Samsung	K4UBE3D4AA-MGCL	32Gb(4GB)	M1100590-001
Hynix	H9HCNNNBKMALHR-NEE	16Gb (2GB)	M1102096-001
Hynix	H9HCNNNCPMALHR-NEE	32Gb(4GB)	M1102097-001

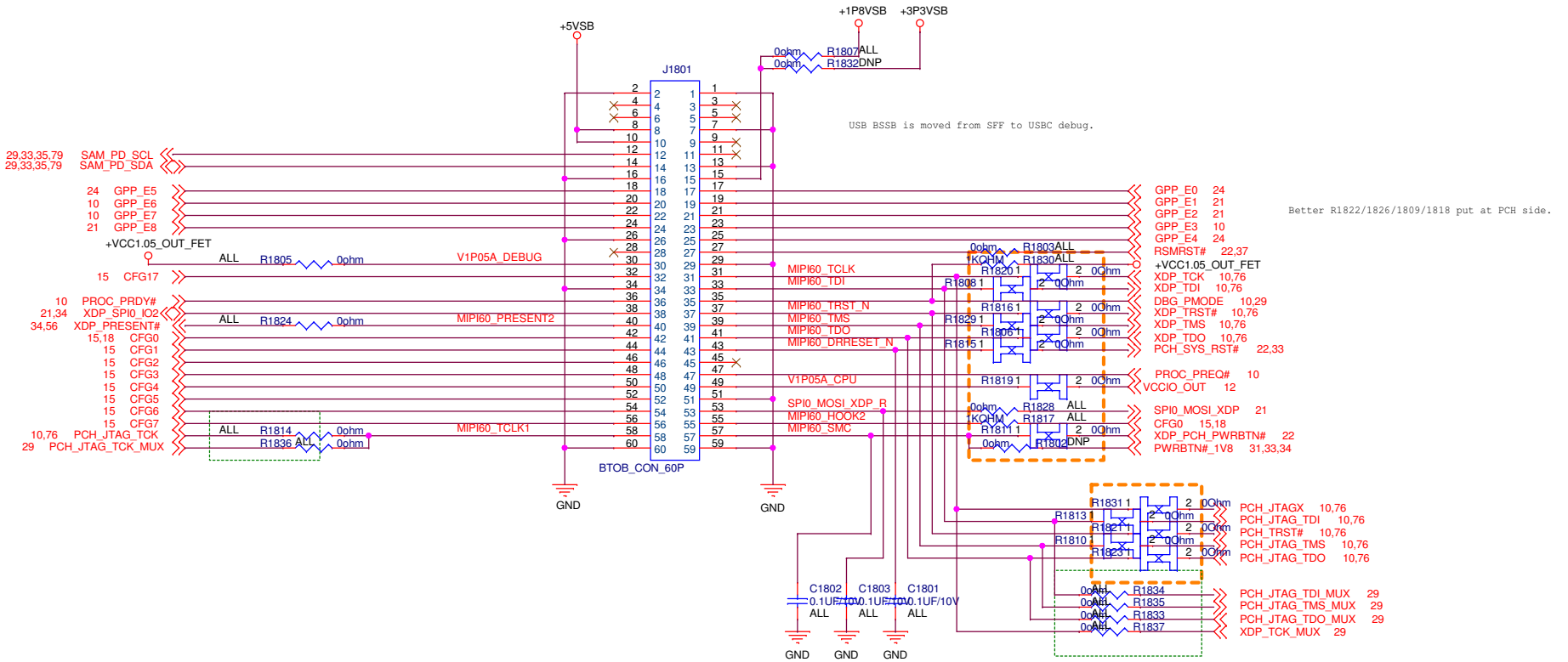
Title: LPDDR4X(1)_MEMORY DOWN

<OrgName> Engineer: <OrgAddr1>

Size: Custom | Project Name: B52 | Rev: 1.00

Date: Friday, June 28, 2019 | Sheet 16 of 82


U1701
U1702
K4UBE3D4AA-MGCL
VDD2 Decoupling
Performance Scheme, except 0201 1uF
6 caps per DRAM, 2 per long edge, 1 per short edge
VDDQ Decoupling
Performance Scheme, except 0201 1uF
4 caps per DRAM, 2 per long edge, 1 per short edge
VDD1 Decoupling
Performance Scheme, except 0201 1uF
4 caps per DRAM, 2 per long edge, 1 per short edge
Title: LPDDR4X(2)_MEMORY DOWN
<OrgName>
Engineer:
<OrgAddr1>
Size: Custom
Project Name: B52
Rev: 1.00
Date: Friday, June 28, 2019
Sheet 17 of 82



Signal	Pin #	Interface	Pin #	Signal
GND	1		2	GND
USB2_DP	3		4	USB0_TX_DP
USB2_DN	5		6	USB0_TX_DN
VBUS	7		8	GND
VBUS	9		10	USB0_RX_DP
I2C_SCL	11		12	USB0_RX_DN
I2C_SDA	13	PCH-VISA, USB2OC	14	GND
GND	15		16	+V1P5A_PCH_VREF_TRACE
MIPI60_FN13	17		18	MIPI60_FN8
MIPI60_FN14	19		20	MIPI60_FN9
MIPI60_FN15	21		22	MIPI60_FN10
MIPI60_FN_CLK2	23		24	MIPI60_FN11
GND	25		26	MIPI60_FN12
I2C_2_SCL	27		28	PM_RSMRST_N*
+V1.05A_VREF_DEBUG	29		30	GND
MIPI60_NDA_STRB_DP	31		32	MIPI60_TCLK
GND	33		34	MIPI60_TDI
MIPI60_PRDY_N	35		36	DBG_PMODE_MIPI60_RST_B_N
MIPI60_PREQ#/TI_N	37		38	MIPI60_TRST_N
MIPI60_DVEW/IDE	39		40	MIPI60_TMS
MIPI60_NDA0_N	41		42	MIPI60_TDO
MIPI60_NDA1_N	43		44	MIPI60_DBRESET_N
MIPI60_NDA2_N	45	CPU-VISA	46	I2C_2_SDA
MIPI60_NDA3_N	47		48	MIPI60_PREQ_N
MIPI60_NDA4_N	49		50	+V1.05A_CPU_VREF_TRACE
MIPI60_NDA5_N	51		52	GND
MIPI60_NDA6_N	53		54	SPI0_MOSI_SYS_PWROK_MIPI60
MIPI60_NDA7_N	55		56	MIPI60 HOOK2 CPU BOOT STRAP
MIPI60_TCLK1	57		58	SMC_ONOFF_MIPI60_N
GND	59		60	GND

Title:	SFF		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 18 of 82		

W x H 382 x 254 mm

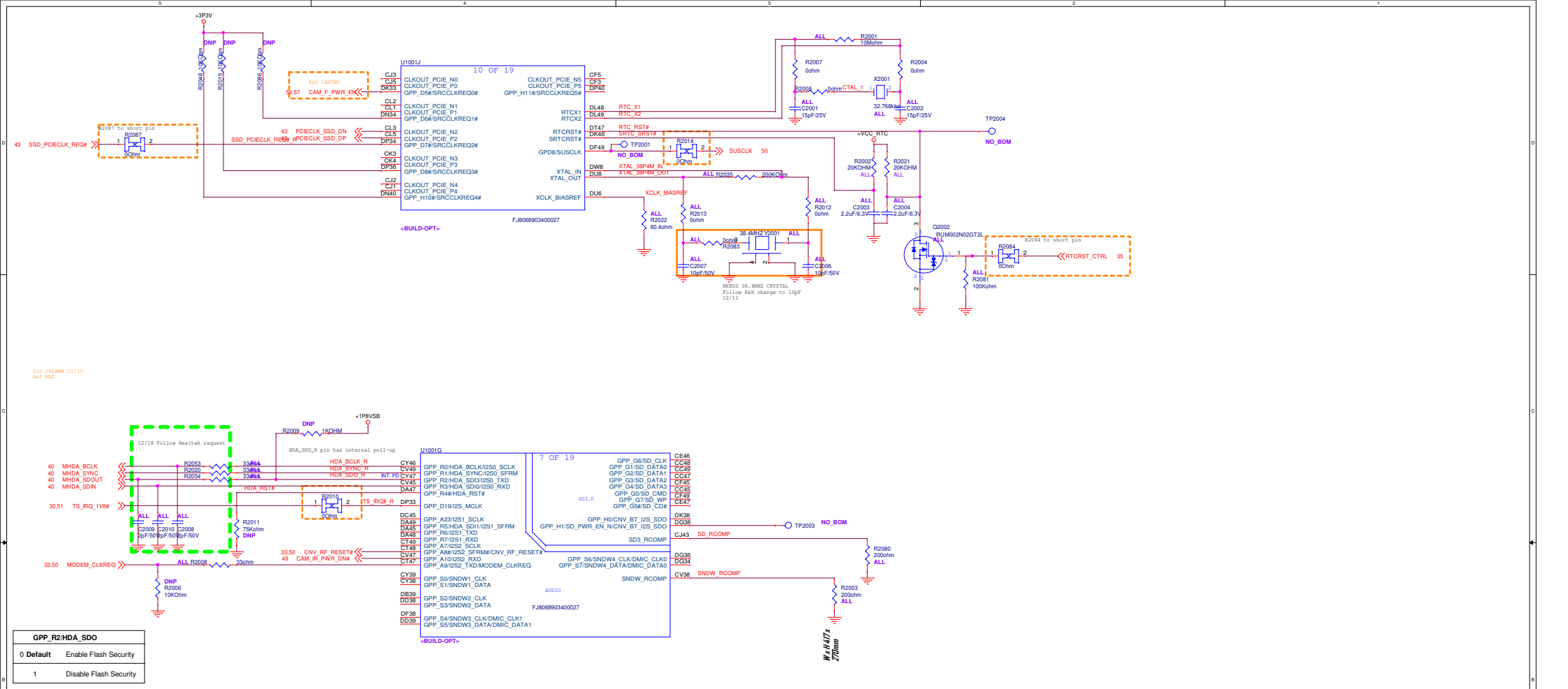
W x H 372 x 241 mm

Title:

<OrgName> Engineer: <OrgAddr1>

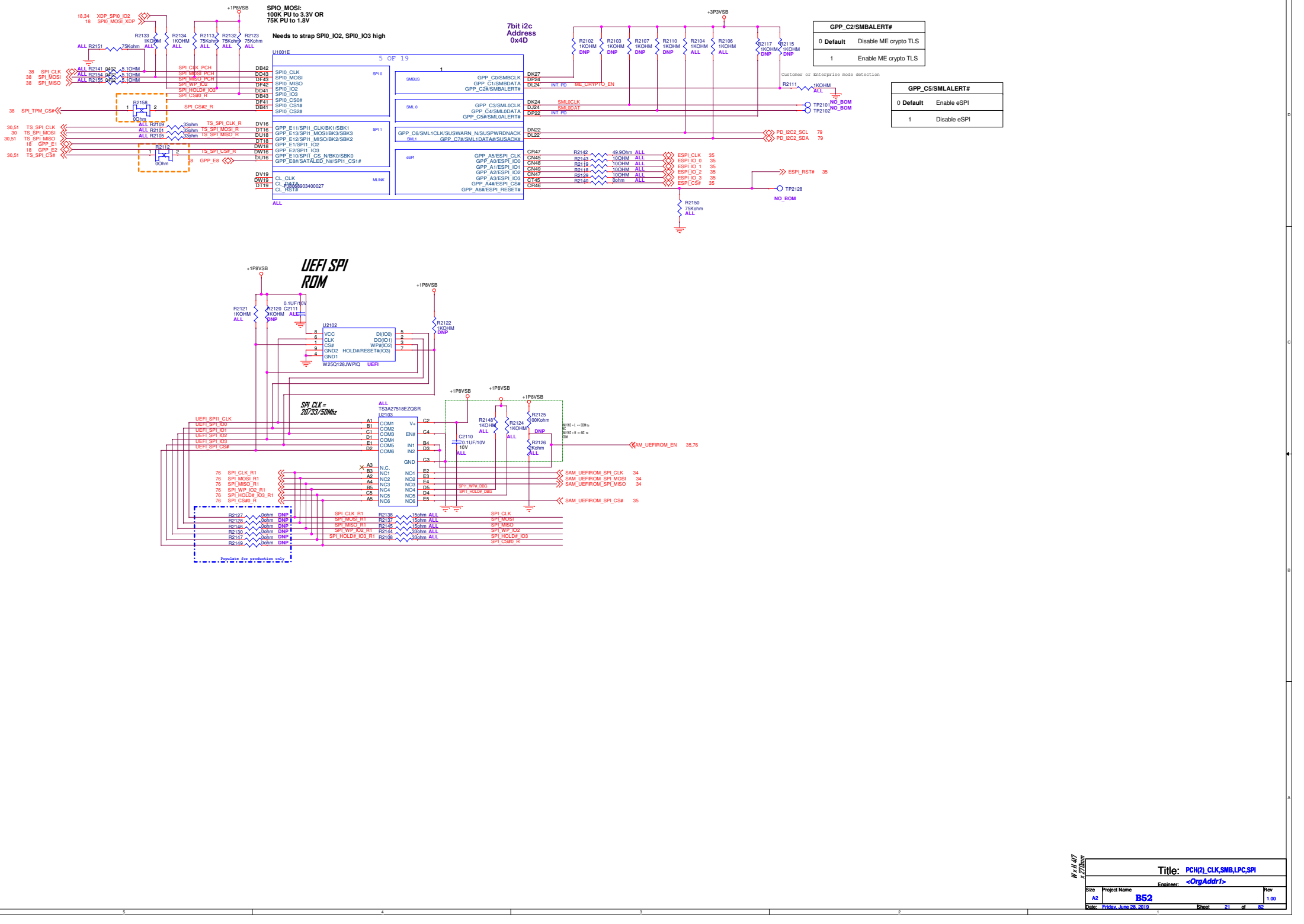
Size: Custom | Project Name: B52 | Rev: 1.00

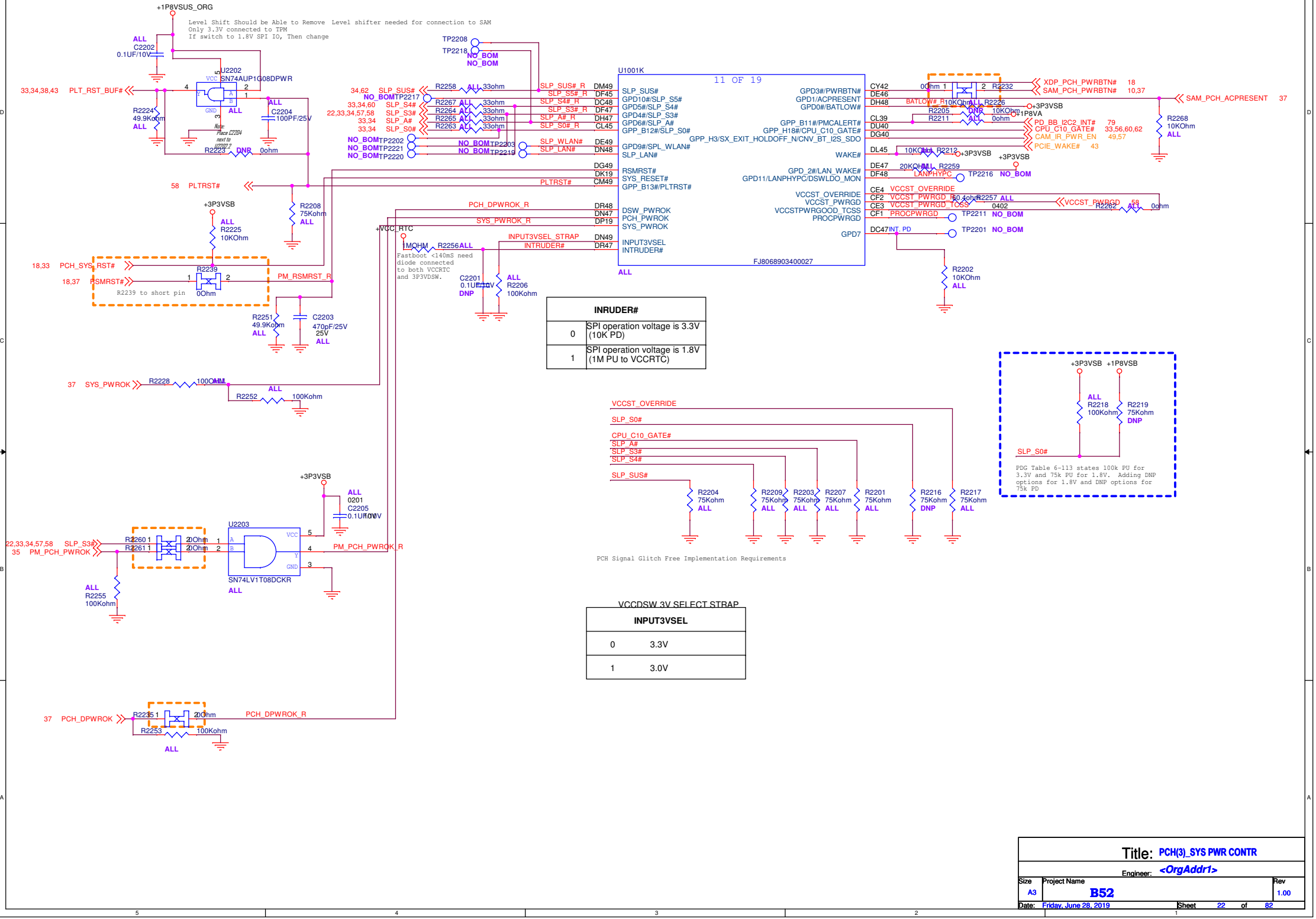
Date: Friday, June 28, 2019 | Sheet 19 of 82



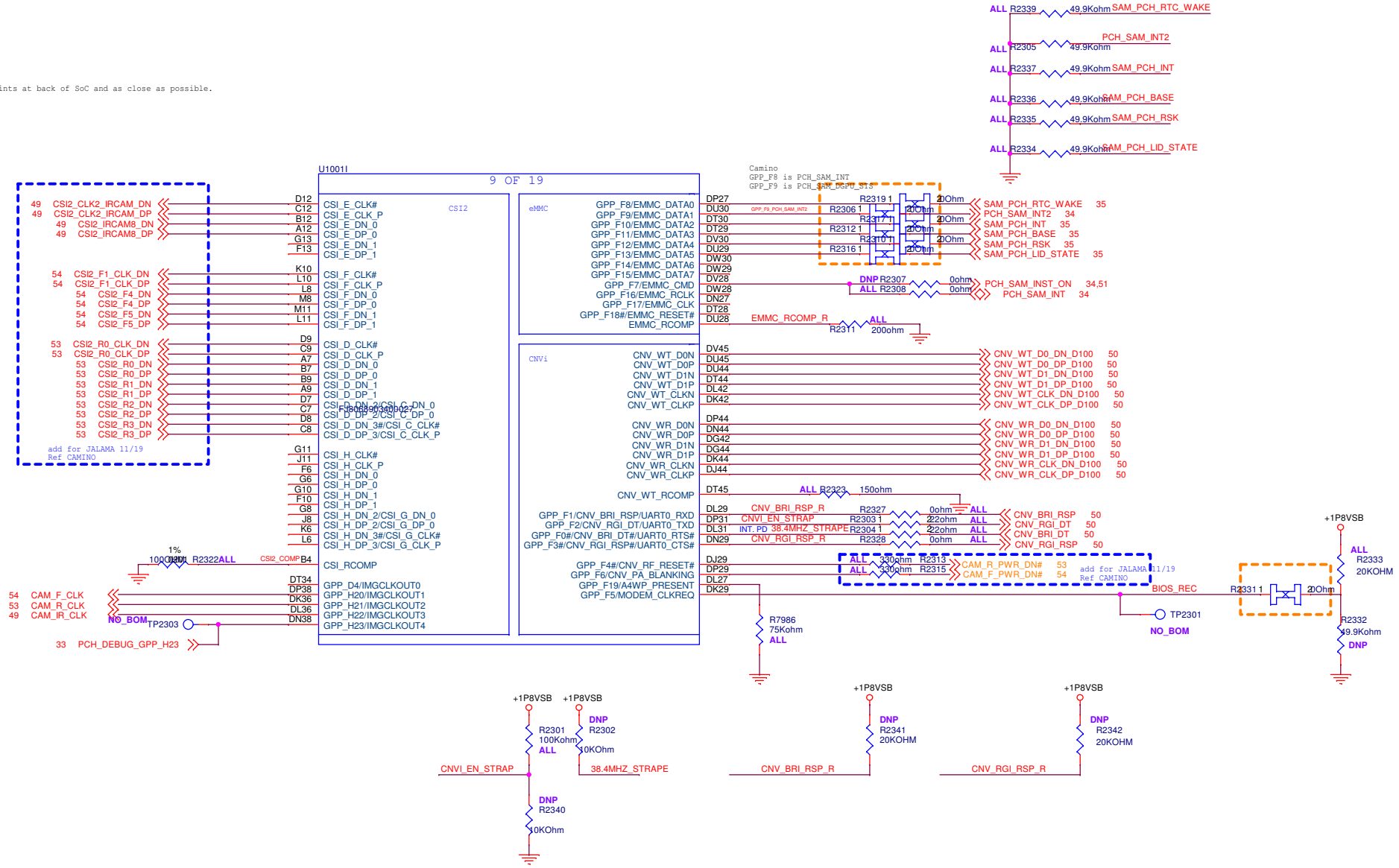
GPP_R2/HDA_SDO	
0 **Default**	Enable Flash Security
1	Disable Flash Security

Title:	PCH(1)_SD,HDA,RTC,CLK		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 20 of 82		


SPI0_MOSI:
100K PU to 3.3V OR
75K PU to 1.8V
Needs to strap SPI0_IO2, SPI0_IO3 high
7bit i2c
Address
0x4D
GPP_C2/SMBALERT#
0 Default Disable ME crypto TLS
1 Enable ME crypto TLS
GPP_C5/SMLALERT#
0 Default Enable eSPI
1 Disable eSPI
Customer or Enterprise mode detection
UEFI SPI
ROM
SPI_CLK =
20/33/50Mhz
Populate for production only
Title: PCH(2)_CLK,SMB,LPC,SPI
Engineer: <OrgAddr1>
Size A2
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 21 of 82


+1P8VSUS_ORG
Level Shift Should be Able to Remove Only 3.3V connected to TPM If switch to 1.8V SPI IO, Then change
Level shifter needed for connection to SAM
U2202 SN74AUP1G08DPWR
C2202 0.1UF/10V
C2204 100PF/25V
R2224 49.9Kohm
R2223 DNR 0ohm
33,34,38,43 PLT_RST_BUF#
Note: Place C2204 next to U2202
TP2208
TP2218
NO_BOM
U1001K
11 OF 19
SLP_SUS#
GPD10#/SLP_S5#
GPD5#/SLP_S4#
GPD4#/SLP_S3#
GPD6#/SLP_A#
GPP_B12#/SLP_S0#
GPD9#/SPL_WLAN#
SLP_LAN#
RSMRST#
SYS_RESET#
GPP_B13#/PLTRST#
DSW_PWROK
PCH_PWROK
SYS_PWROK
INPUT3VSEL
INTRUDER#
GPD3#/PWRBTN#
GPD1/ACPRESENT
GPD0#/BATLOW#
GPP_B11#/PMCALERT#
GPP_H18#/CPU_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF_N/CNV_BT_I2S_SDO
WAKE#
GPD_2#/LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON
VCCST_OVERRIDE
VCCST_PWRGD
VCCSTPWRGOOD_TCSS
PROCPWRGD
GPD7
FJ8068903400027
58 PLTRST#
+3P3VSB
R2208 75Kohm
R2225 10KOhm
18,33 PCH_SYS_RST#
18,37 PSMRSTT#
R2239 0Ohm
R2239 to short pin
PM_RSMRST_R
R2251 49.9Kohm
C2203 470pF/25V
37 SYS_PWROK
R2228 100OHM
R2252 100Kohm
+VCC_RTC
1MOHM R2256
Fastboot <140mS need diode connected to both VCCRTC and 3P3VDSW.
C2201 0.1UF/10V DNP
R2206 100Kohm
INPUT3VSEL_STRAP
INTRUDER#
PCH_DPWROK_R
SYS_PWROK_R
PLTRST#
INTRUDER#
R2202 10KOhm
XDP_PCH_PWRBTN# 18
SAM_PCH_PWRBTN# 10,37
SAM_PCH_ACPRESENT 37
R2268 10KOhm
R2205 DNR 10KOhm
R2211 ALL 0ohm
+1P8VA
PD_BB_I2C2_INT# 79
CPU_C10_GATE# 33,56,60,62
CAM_IR_PWR_EN 49,57
PCIE_WAKE# 43
R2232
R2226
R2212 10KOhm
R2259 20KOhm
LANPHYPC
TP2216 NO_BOM
VCCST_OVERRIDE
VCCST_PWRGD_TCSS
PROCPWRGD
TP2211 NO_BOM
INT_PD
TP2201 NO_BOM
R2257 50.4ohm
R2262 0402
VCCST_PWRGD 58
INPUT3VSEL_STRAP
INTRUDER#
INPUT3VSEL
0 SPI operation voltage is 3.3V (10K PD)
1 SPI operation voltage is 1.8V (1M PU to VCCRTC)
VCCST_OVERRIDE
SLP_S0#
CPU_C10_GATE#
SLP_A#
SLP_S3#
SLP_S4#
SLP_SUS#
R2204 75Kohm
R2209 75Kohm
R2203 75Kohm
R2207 75Kohm
R2201 75Kohm
R2216 75Kohm DNP
R2217 75Kohm
PCH Signal Glitch Free Implementation Requirements
R2218 100Kohm
R2219 75Kohm DNP
PDG Table 6-113 states 100k PU for 3.3V and 75k PU for 1.8V. Adding DNP options for 1.8V and DNP options for 75k PD
U2203 SN74LV1T08DCKR
22,33,34,57,58 SLP_S3#
35 PM_PCH_PWROK
R2260 20Ohm
R2261 20Ohm
PM_PCH_PWROK_R
R2255 100Kohm
37 PCH_DPWROK
R2235 20Ohm
R2253 100Kohm
PCH_DPWROK_R
VCCDSW 3V SELECT STRAP
INPUT3VSEL
0 3.3V
1 3.0V
Title: PCH(3)_SYS PWR CONTR
Engineer: <OrgAddr1>
Size A3
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 22 of 82

Please place testpoints at back of SoC and as close as possible.



CNVI ENABLE

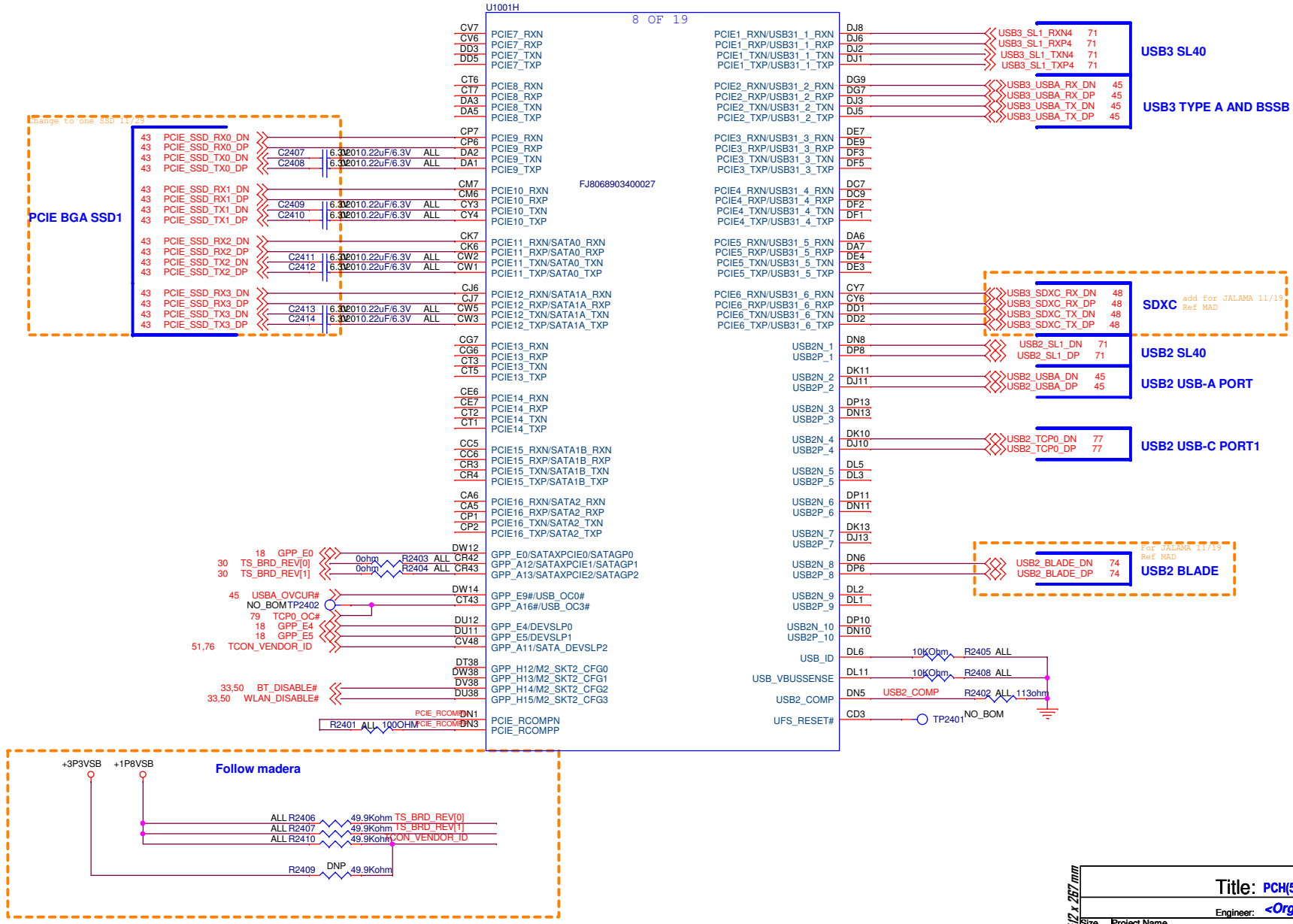
GPP_F2	
0 **Default**	Integrated CNVi Enabled
1	Integrated CNVi Disabled

XTAL FREQUENCY SELECTION

GPP_F0	
0 **Default**	38.4MHZ
1	24MHZ

Title:	PCH(4)_CSI,eMMC,CNVi,IDs		
Engineer:	<OrgAddr1>		
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 23 of 82		

W x H 422 x 273 mm



Title: PCH(5)_PCIE,USB			
Engineer: <OrgAddr1>			
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019		Sheet 24 of 82	

W x H 412 x 267 mm

SAM NEED DECIDE TO SET UEFI_TOP_SWAP HIGH OR LOW BEFORE ASSERT PCH_PWROK

35 SAM_PCH_TOP_SWAP

R2518 100Kohm DNP

No reboot strap
Low: Disable (Default)
High:Enable

GPP_B18:
No reboot strap
Low: Disable (Default)
High:Enable

GPP_B14	
0 (default)	Disable "Top Swap" mode
1	Enable "Top Swap" mode

+1P8VSB

R2533 R2534 R2535 R2536 R2539 100Kohm ALL ALL ALL ALL ALL

add for JALAMA 11/19
remove 2/12 base on
KORE request

48 SD_CD#_PCH

INT. PD

U1001F

6 OF 19

GPP_B16/GSPI0_CLK CH48
GPP_B18/GSPI0_MOSI CF48
GPP_B17/GSPI0_MISO CF47
GPP_B15#/GSPI0_CS0# CH49
GPP_B14#/SPKR#/TIME_SYNC1#/GSPI0_CS1# CH47

GPP_B20/GSPI1_CLK CL47
GPP_B22/GSPI1_MOSI CK47
GPP_B21/GSPI1_MISO CK46
GPP_B19#/GSPI1_CS0# CH45
GPP_B23#/SML1ALERT_N#/PCHHOT_N#/GSPI1_CS1# CL48

GPP_C8/UART0_RXD DP21
GPP_C9/UART0_TXD DK21
GPP_C10#/UART0_RTS# DL21
GPP_C11#/UART0_CTS# DJ22

GPP_C20/UART2_RXD DT22
GPP_C21/UART2_TXD DW22
GPP_C22#/UART2_RTS# DV22
GPP_C23#/UART2_CTS# DU22

GPP_C16/I2C0_SDA DT24
GPP_C17/I2C0_SCL DT23

GPP_C18/I2C1_SDA DW23
GPP_C19/I2C1_SCL DU23

GPP_H4/I2C2_SDA DU41
GPP_H5/I2C2_SCL DV41

GPP_H6/I2C3_SDA DW41
GPP_H7/I2C3_SCL DT41

GPP_H8/I2C4_SDA/CNV_MFUART2_RXD DT40
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD DW40

GPP_D13/ISH_UART0_RXD
GPP_D14/ISH_UART0_TXD
GPP_D15/ISH_UART0_RTS_N/GSPI2_CS1_N/IMGCLKOUT5
GPP_D16/ISH_UART0_CTS_N/CNV_WCEN

GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14#/UART1_RTS_N#/ISH_UART1_RTS#
GPP_C15#/UART1_CTS_N#/ISH_UART1_CTS#

GPP_B5/ISH_I2C0_SDA
GPP_B6/ISH_I2C0_SCL

GPP_B7/ISH_I2C1_SDA
GPP_B8/ISH_I2C1_SCL

GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL

GPP_D0/ISH_GP0
GPP_D1/ISH_GP1
GPP_D2/ISH_GP2
GPP_D3/ISH_GP3
GPP_D17/ISH_GP4
GPP_D18/ISH_GP5
GPP_E15/ISH_GP6
GPP_E16/ISH_GP7

<Should really be a space here in the symbol >

29,33,34 SAMTX_PCHRX
29,33,34 PCHTX_SAMRX
29,33,34,76 PCHRTS_SAMCTS
29,33,34,76 SAMRTS_PCHCTS

62 RTD3_AUD_PWR_1P8
64 RTD3_AUD_PWR_5P0
31,33 VOL_UP#
31,33 VOL_DOWN#

FJ8068903400027

PANEL_I2C_SDA_R
PANEL_I2C_SCL_R

+1P8V_PANEL

R2584 1KOHM ALL
R2583 1KOHM ALL

33,51,72 PANEL_I2C_SDA
33,51,72 PANEL_I2C_SCL

28,33,76 PMI_I2C_SDA
28,33,76 PMI_I2C_SCL

R2598 2.0Ohm
R2597 2.0Ohm

NO_BOM MTP2533
NO_BOM MTP2532

54 I2C_SDA_FCAM
54 I2C_SCL_FCAM

R2522 2.0Ohm
R2523 2.0Ohm

I2C_SDA_FCAM_R
I2C_SCL_FCAM_R

53 I2C_SDA_RCAM
53 I2C_SCL_RCAM

R2520 0ohm ALL
R2521 0ohm ALL

I2C_SDA_REAR_IR_CAM
I2C_SCL_REAR_IR_CAM

NO_BOM MTP2537
NO_BOM MTP2536

49 I2C_SDA_IRCAM
49 I2C_SCL_IRCAM
49 ALS_I2C3_SDA
49 ALS_I2C3_SCL

0ohm R2527 ALL
0ohm R2528 ALL
0ohm R2562 DBG_D_ALS
0ohm R2563 DBG_D_ALS

add for JALAMA 11/19
Ref CAMINO

32 I2C4_SDA
32 I2C4_SCL

CPUNSSC Clock Frequency

GPP_B23/SML1ALERT#/ PCHHOT#/GSPI1_CS1#	
Default	38.4MHz (crystal)
1	19.2MHz (internal divider)

TP2523 NO_BOM
TP2518 NO_BOM

DV33 TPANEL_RST#_R
DW33
DT33 RTD3_CAM_PWREN_R
DU33 FLASH_PROTECT#_R

0Ohm 1 2R2511
R2517 ALL 1KOHM
0Ohm 1 2R2515

TPANEL_RST# 30,33,35
RTD3_TPANEL_PWR 62,64
RTD3_CAM_PWREN 57,76
FLASH_PROTECT# 30

DK22 0Ohm 1 2R2513
DW24 0Ohm 1 2R2505
DU24 ALS_ACS_CONFIG
MEM_CONFIG

Debug UART
PCH_DBG_RX 29,33,76
PCH_DBG_TX 29,33,76

+3P3VSB
R2590 ALL 100Kohm
ALL R2589 100Kohm

CN43 PCH_ISH_I2C0_SDA 0Ohm 1 2R2501
CN42 PCH_ISH_I2C0_SCL 0Ohm 1 2R2502

PCH_SAM_SNSR_S0_SDA 32
PCH_SAM_SNSR_S0_SCL 32

CN41 PCH_ISH_I2C1_SDA ALL R2503 33ohm
CL43 PCH_ISH_I2C1_SCL ALL R2506 33ohm

PCH_SENSOR_ISH_SDA 32
PCH_SENSOR_ISH_SCL 32

CL41
CJ39
DU36 AGYRO_INT1#_R R2507 0ohm ALL
DV36 ALS_IRQ# 32
DW36 R2532
DT36 GPP_D5
DU34
DW34
DT14
DU14

Jalama EV1 change

NO_BOM +1P8VSB
TP2527
NO_BOM
CAM_R_PWR_EN 53,57
Ref CAMINO
ALL R2510 10KOhm
AGYRO_INT1# 32

MAG_INT 32
ISH_SAM_INT 34

+3P3VSB
DNP R2525 1KOHM
LED2501 RED DNP

-4mA sync capability on 3.3V GPIO

R2599 DNP 0ohm ISH_DBG

+1P8VSB
R2537 10KOhm DNP
MEM_CONFIG
LOW: A,B,C,D CHANNEL ENABLE
HIGH: A,C CHANNEL ENABLE
ALL R2526 10KOhm

+1P8VSB
R2560 10KOhm DNP
ALS_ACS_CONFIG
LOW: ACS
HIGH: ALS
DNP R2561 10KOhm

Jalama 0125 DNP FCU U2502

Do we need this FCU for log store

+1P8VSUS_ORG
DNP R2554 2Kohm
DNP R2558 2Kohm

+1P8VSUS_ORG
DNP C2501 0.1UF/6.3V
U2502
VCC SCL A2
VSS SDA B1
A1 B2
M24C64S-FCU6T/T
DNP
GND GND

I2C4_SCL
I2C4_SDA

NO_BOM TP2531
NO_BOM TP2530

R2508 ALL 49.9Kohm ISH_SAM_INT
R2572 ALL 49.9Kohm RTD3_AUD_PWR_1P8
R2595 ALL 49.9Kohm RTD3_AUD_PWR_5P0
R2559 ALL 49.9Kohm RTD3_TPANEL_PWR
R2596 DNP 10KOhm TPANEL_RST#
R2592 ALL 49.9Kohm RTD3_CAM_PWREN

+1P8VSB +1P8VSB
R2504 2Kohm ALL
R2512 2Kohm ALL
R2514 2Kohm ALL
R2516 2Kohm ALL

PCH_SENSOR_ISH_SCL
PCH_SENSOR_ISH_SDA
PCH_SAM_SNSR_S0_SCL
PCH_SAM_SNSR_S0_SDA

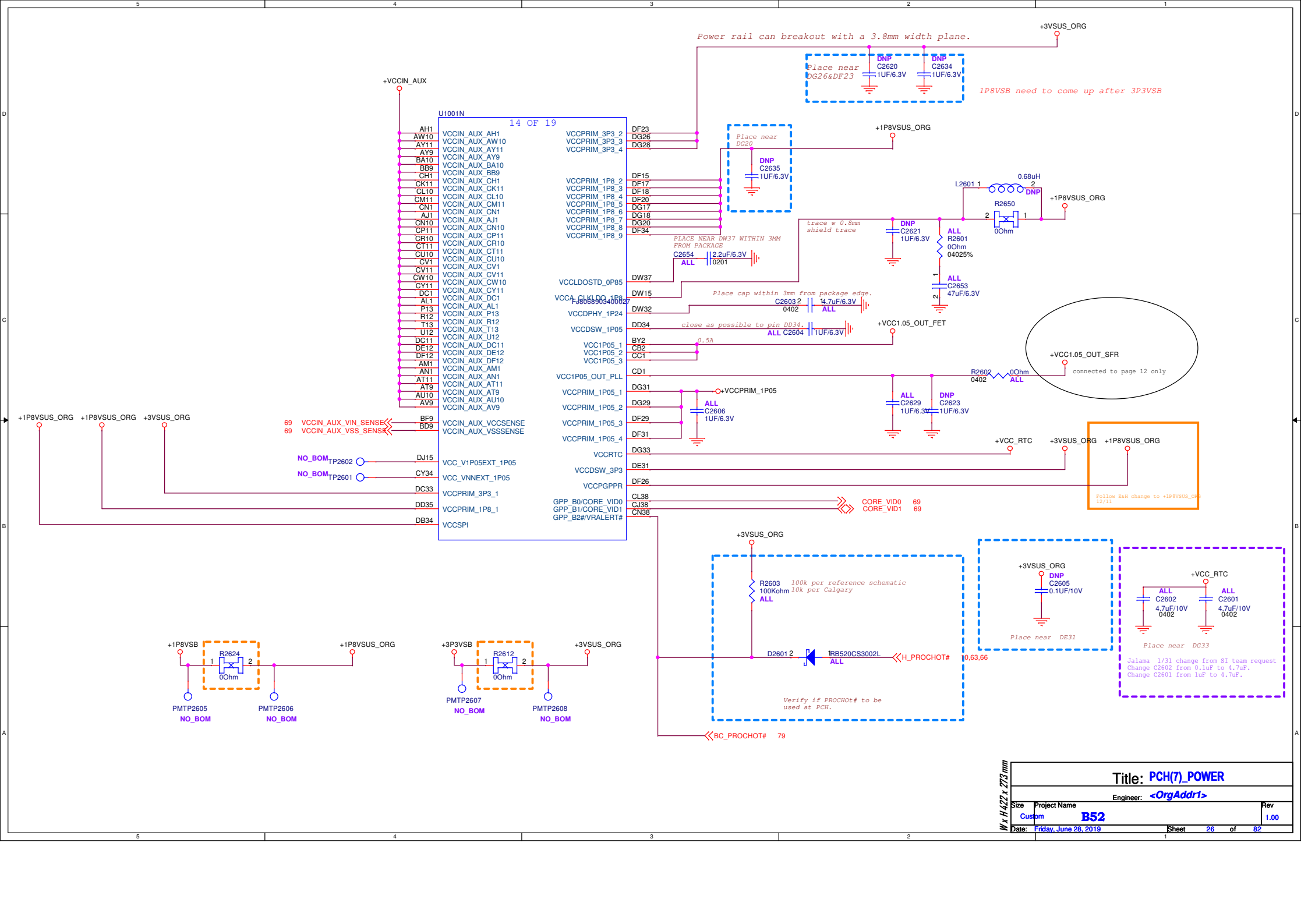
C2502 33pF/25V ALL
C2503 33pF/25V ALL

Wx114/7x 270ohm

Title: PCH(6)_CPU,GPIO,MISC
Engineer: <OrgAddr1>

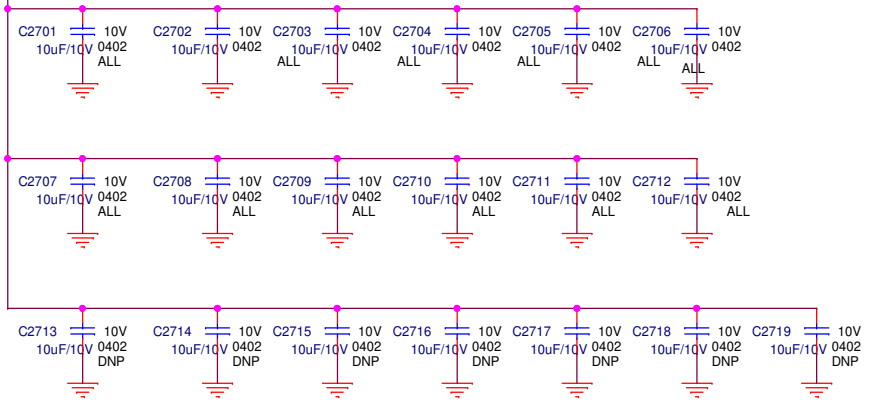
Size	Project Name	Rev
Custom	B52	1.00

Date: Friday, June 28, 2019 Sheet 25 of 82


Power rail can breakout with a 3.8mm width plane.
+3VSUS_ORG
Place near DG26&DF23
DNP C2620 1UF/6.3V
DNP C2634 1UF/6.3V
1P8VSB need to come up after 3P3VSB
+VCCIN_AUX
U1001N
14 OF 19
VCCIN_AUX_AH1
VCCIN_AUX_AW10
VCCIN_AUX_AY11
VCCIN_AUX_AY9
VCCIN_AUX_BA10
VCCIN_AUX_BB9
VCCIN_AUX_CH1
VCCIN_AUX_CK11
VCCIN_AUX_CL10
VCCIN_AUX_CM11
VCCIN_AUX_CN1
VCCIN_AUX_AJ1
VCCIN_AUX_CN10
VCCIN_AUX_CP11
VCCIN_AUX_CR10
VCCIN_AUX_CT11
VCCIN_AUX_CU10
VCCIN_AUX_CV1
VCCIN_AUX_CV11
VCCIN_AUX_CW10
VCCIN_AUX_CY11
VCCIN_AUX_DC1
VCCIN_AUX_AL1
VCCIN_AUX_P13
VCCIN_AUX_R12
VCCIN_AUX_T13
VCCIN_AUX_U12
VCCIN_AUX_DC11
VCCIN_AUX_DE12
VCCIN_AUX_DF12
VCCIN_AUX_AM1
VCCIN_AUX_AN1
VCCIN_AUX_AT11
VCCIN_AUX_AT9
VCCIN_AUX_AU10
VCCIN_AUX_AV9
VCCPRIM_3P3_2
VCCPRIM_3P3_3
VCCPRIM_3P3_4
VCCPRIM_1P8_2
VCCPRIM_1P8_3
VCCPRIM_1P8_4
VCCPRIM_1P8_5
VCCPRIM_1P8_6
VCCPRIM_1P8_7
VCCPRIM_1P8_8
VCCPRIM_1P8_9
VCCLDOSTD_0P85
VCCA_CLKLDO_1P8
VCCDPHY_1P24
VCCDSW_1P05
VCC1P05_1
VCC1P05_2
VCC1P05_3
VCC1P05_OUT_PLL
VCCPRIM_1P05_1
VCCPRIM_1P05_2
VCCPRIM_1P05_3
VCCPRIM_1P05_4
VCCRTC
VCCDSW_3P3
VCCPGPPR
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
GPP_B2#/VRALERT#
VCCSPI
VCC_V1P05EXT_1P05
VCC_VNNEXT_1P05
VCCPRIM_3P3_1
VCCPRIM_1P8_1
VCCIN_AUX_VCCSENSE
VCCIN_AUX_VSSSENSE
+1P8VSUS_ORG
Place near DG20
DNP C2635 1UF/6.3V
PLACE NEAR DW37 WITHIN 3MM FROM PACKAGE
C2654 ALL 2.2uF/6.3V 0201
trace w 0.8mm shield trace
DNP C2621 1UF/6.3V
L2601 0.68uH DNP
R2650 0Ohm
ALL R2601 0Ohm 04025%
ALL C2653 47uF/6.3V
Place cap within 3mm from package edge.
C2603 0402 4.7uF/6.3V ALL
close as possible to pin DD34.
ALL C2604 1UF/6.3V
+VCC1.05_OUT_FET
0.5A
+VCC1.05_OUT_SFR
connected to page 12 only
R2602 0402 0Ohm ALL
+VCCPRIM_1P05
ALL C2606 1UF/6.3V
ALL C2629 1UF/6.3V
DNP C2623 1UF/6.3V
+VCC_RTC
+3VSUS_ORG
+1P8VSUS_ORG
Follow E&H change to +1P8VSUS_ORG 12/11
+1P8VSUS_ORG
+1P8VSUS_ORG
+3VSUS_ORG
69 VCCIN_AUX_VIN_SENSE
69 VCCIN_AUX_VSS_SENSE
NO_BOM TP2602
NO_BOM TP2601
CORE_VID0 69
CORE_VID1 69
+3VSUS_ORG
R2603 100Kohm ALL
100k per reference schematic
10k per Calgary
D2601 RB520CS3002L ALL
H_PROCHOT# 10,63,66
Verify if PROCHOt# to be used at PCH.
BC_PROCHOT# 79
+3VSUS_ORG
DNP C2605 0.1UF/10V
Place near DE31
+VCC_RTC
ALL C2602 4.7uF/10V 0402
ALL C2601 4.7uF/10V 0402
Place near DG33
Jalama 1/31 change from SI team request
Change C2602 from 0.1uF to 4.7uF.
Change C2601 from 1uF to 4.7uF.
+1P8VSB
R2624 0Ohm
+1P8VSUS_ORG
PMTP2605 NO_BOM
PMTP2606 NO_BOM
+3P3VSB
R2612 0Ohm
+3VSUS_ORG
PMTP2607 NO_BOM
PMTP2608 NO_BOM
Title: PCH(7)_POWER
Engineer: <OrgAddr1>
Size: Custom
Project Name: B52
Rev: 1.00
Date: Friday, June 28, 2019
Sheet 26 of 82
W x H 422 x 273 mm

+VCCIN_AUX

Place them as directly below the BGAs as possible



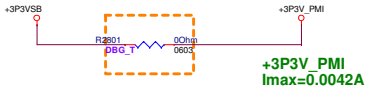
W x H 377 x 244 mm

Title: PCH(8)_decoupling

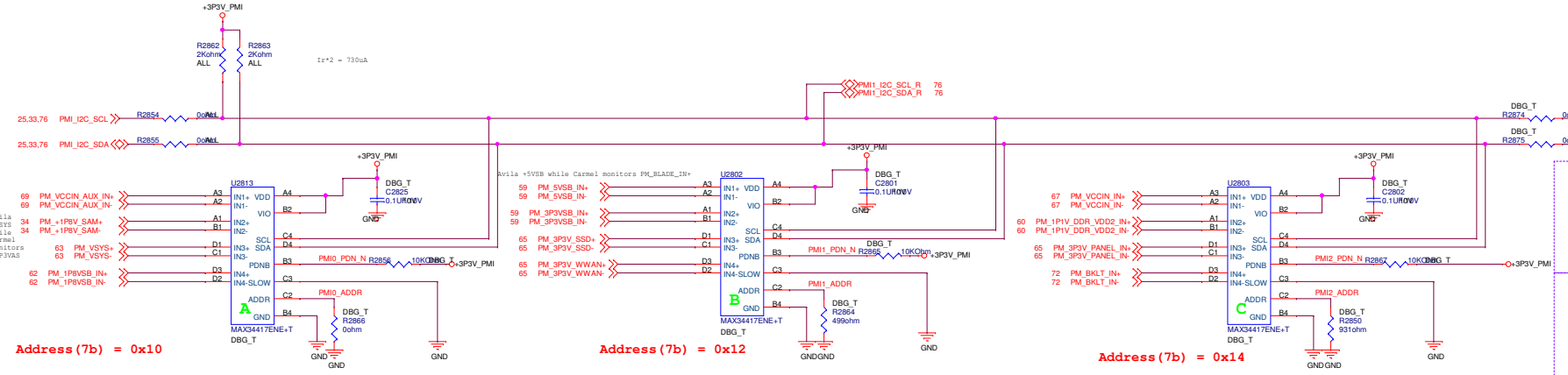
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	B52	1.00

Date: Friday, June 28, 2019 Sheet 27 of 82



+3P3V_PMI
Imax=0.0042A



MAX34417 VDD Average Supply Current
700uA PDNB=VIO and SLOW=GND
10uA PDNB=VIO and SLOW=VIO
2uA PDNB=GND

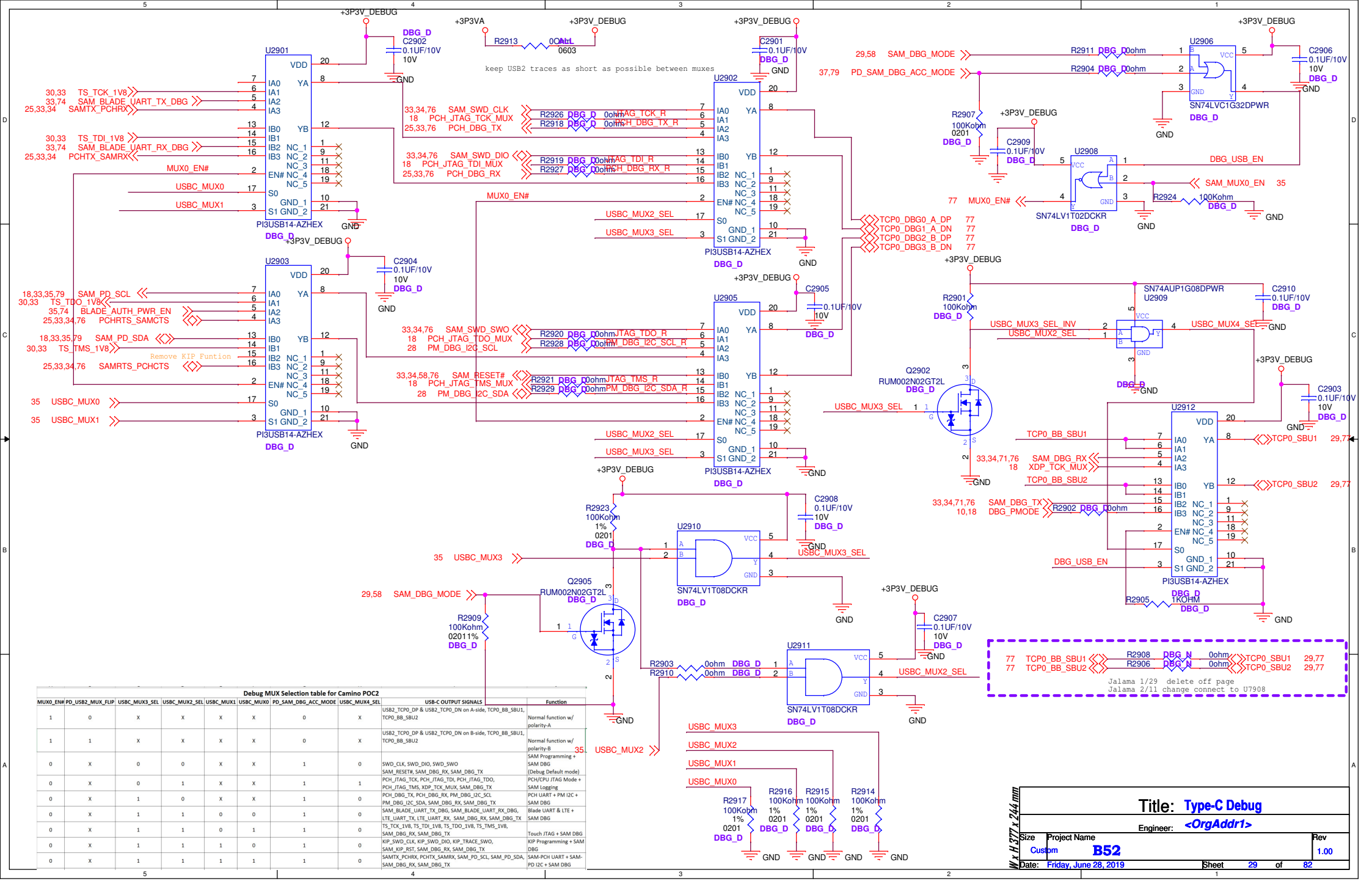
6x700uA=4.2mA
3.3Vx4.2mA=13.86mW

Part B
5VSB
3P3 VSB
1P8 VSB
3P3V WWAN

Part C
3P3 Panel
Display Backlight
3P3V SSD

Title:	Power Monitor	
Engineer:	<OrgAddr1>	
Size: A	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 28 of 82	

W=11.577, H=8.273, mm



Debug MUX Selection table for Camino POC2

MUX0_EN#	PD_USB2_MUX_FLIP	USBC_MUX3_SEL	USBC_MUX2_SEL	USBC_MUX1	USBC_MUX0	PD_SAM_DBG_ACC_MODE	USBC_MUX4_SEL	USB-C OUTPUT SIGNALS	Function
1	0	X	X	X	X	0	X	USB2_TCP0_DP & USB2_TCP0_DN on A-side, TCP0_BB_SBU1, TCP0_BB_SBU2	Normal function w/ polarity-A
1	1	X	X	X	X	0	X	USB2_TCP0_DP & USB2_TCP0_DN on B-side, TCP0_BB_SBU1, TCP0_BB_SBU2	Normal function w/ polarity-B
0	X	0	0	X	X	1	0	SWD_CLK, SWD_DIO, SWD_SWO SAM_RESET#, SAM_DBG_RX, SAM_DBG_TX	SAM Programming + SAM DBG (Debug Default mode)
0	X	0	1	X	X	1	1	PCH_JTAG_TCK, PCH_JTAG_TDI, PCH_JTAG_TDO, PCH_JTAG_TMS, XDP_TCK_MUX, SAM_DBG_TX	PCH/CPU JTAG Mode + SAM Logging
0	X	1	0	X	X	1	0	PCH_DBG_TX, PCH_DBG_RX, PM_DBG_I2C_SCL PM_DBG_I2C_SDA, SAM_DBG_RX, SAM_DBG_TX	PCH UART + PM I2C + SAM DBG
0	X	1	1	0	0	1	0	SAM_BLADE_UART_TX_DBG, SAM_BLADE_UART_RX_DBG, LTE_UART_TX, LTE_UART_RX, SAM_DBG_RX, SAM_DBG_TX	Blade UART & LTE + SAM DBG
0	X	1	1	0	1	1	0	TS_TCK_1V8, TS_TDI_1V8, TS_TDO_1V8, TS_TMS_1V8, SAM_DBG_RX, SAM_DBG_TX	Touch JTAG + SAM DBG
0	X	1	1	1	0	1	0	KIP_SWD_CLK, KIP_SWD_DIO, KIP_TRACE_SWO, SAM_KIP_RST, SAM_DBG_RX, SAM_DBG_TX	KIP Programming + SAM DBG
0	X	1	1	1	1	1	0	SAMTX_PCHRX, PCHTX_SAMRX, SAM_PD_SCL, SAM_PD_SDA, SAM_DBG_RX, SAM_DBG_TX	SAM-PCH UART + SAM-PD I2C + SAM DBG

Title: Type-C Debug

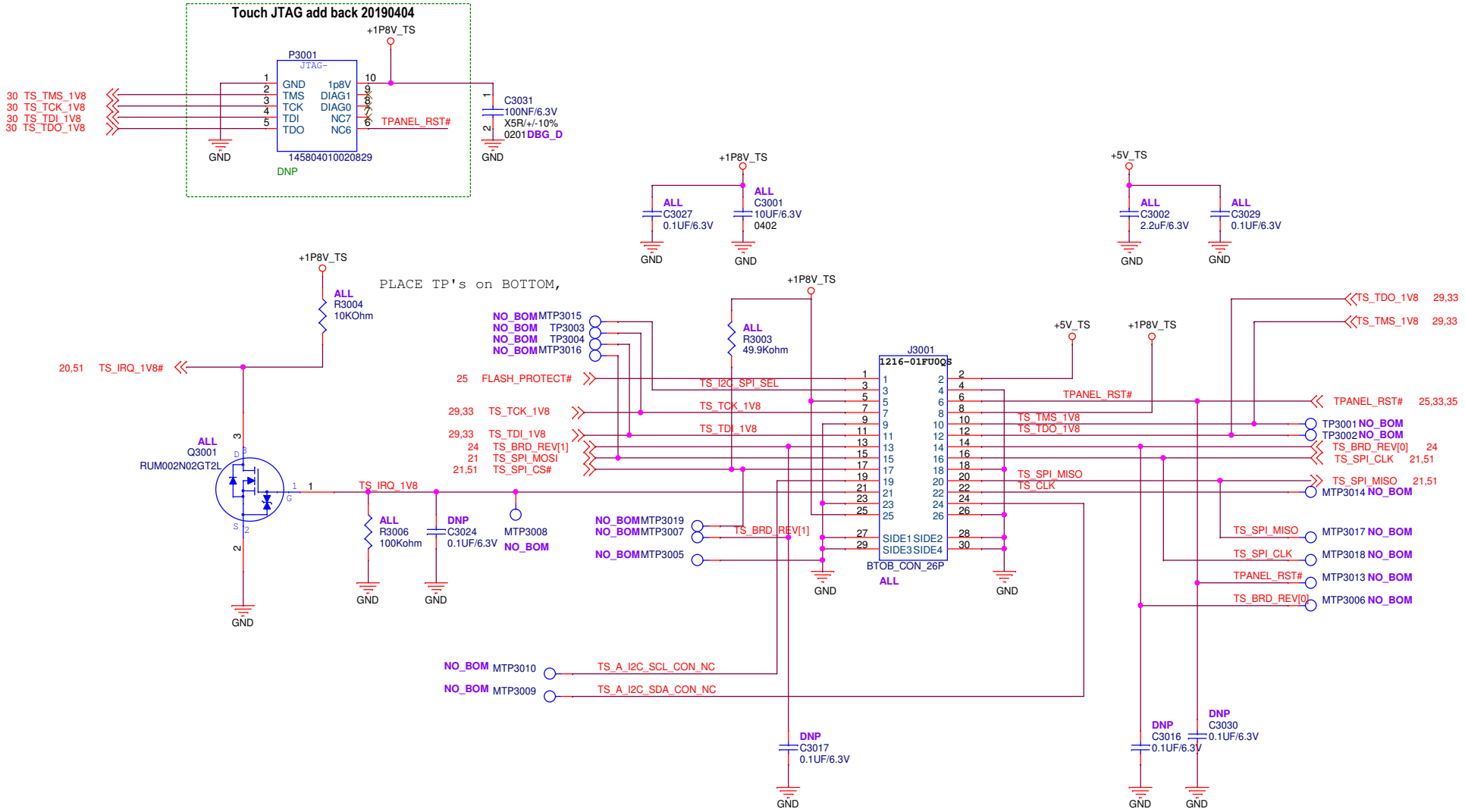
Engineer: <OrgAddr1>

Size: Custom | Project Name: B52 | Rev: 1.00

Date: Friday, June 28, 2019 | Sheet 29 of 82

W x H 377 x 244 mm

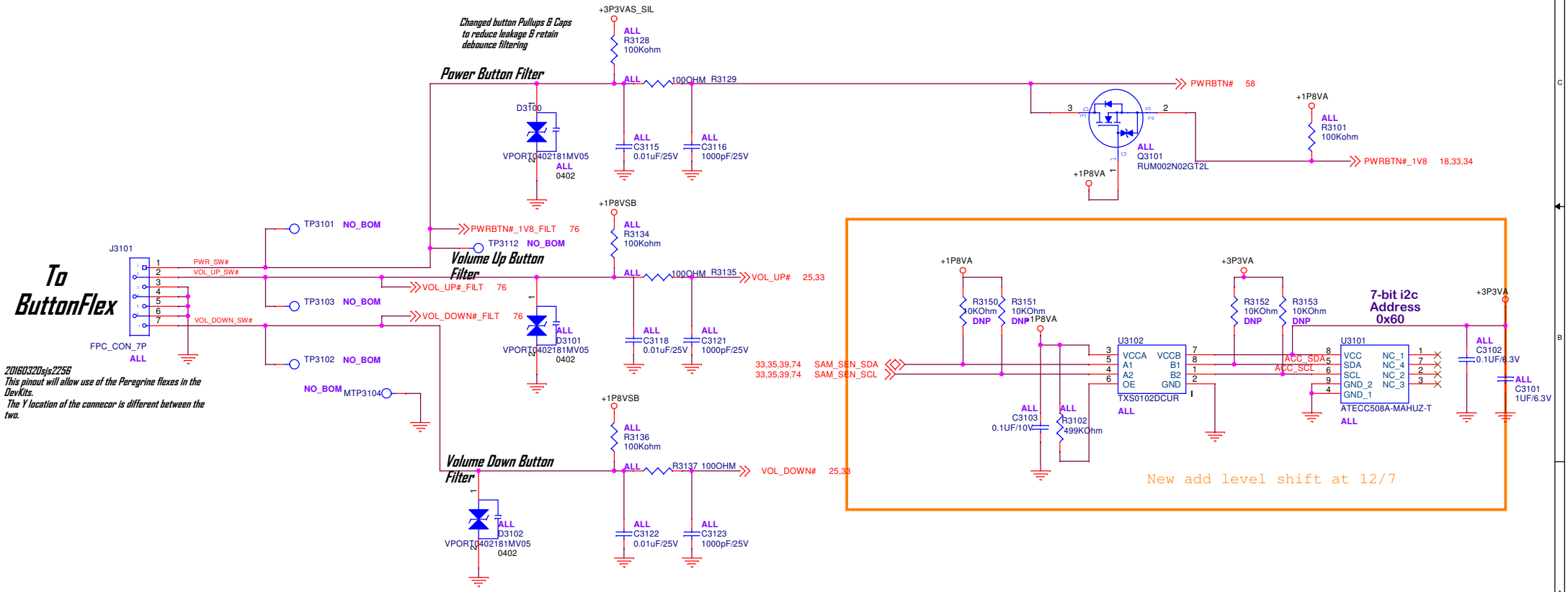
This Page reference Marada



Title:	Touch Con & Key	
Engineer:	<OrgAddr1>	
Size: Custom	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 30 of 82	

W x H 277 x 244 mm

This Page reference Marada



20160822sjs1414
Title is: Button & Diagnostic Conn

Report errors to Steven

Size: Custom	Project Name	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 31 of 82	

Title: Button & Diagnostic Conn

Engineer: <OrgAddr1>

WxH 422 x 273

12/19 change to Molex 1216-02KY0QS
2/12 Add ACS_IRQ# signal to connect to GPP_D1 per cross platform power team feedback

Hall Lockout 1

Hall Lockout 2

Hall Switch

Blade Closed Backside Lockout Logic

Hall South2	Hall North2	Lockout	Hall South	Blade Hall#
0	0	1	1	1
0	1	1	1	1
1	1	0	1	1
1	0	1	1	1
1	0	1	0	1
0	1	1	0	1
0	0	1	0	1
1	1	0	0	0

Jalama 0125 BOM change
DNP-->DBG_D

Jalama 0125 BOM change
DNP-->DBG_D --> short pin

Output LOW
...when lid
is closed

Remove at EV1 stage

Imax = 990uA at 3.3V

Changed from +3P3VSB

Ambient Light Sensor & Front Mic

7-bit i2c
Address
0x44

Imax = 150uA
for color ALS

Jalama change for EV1

I2C Pullup to 1.8V

Re-design for both ALS and ACS on MB side for JALAMA EV1.5

R3256	R3255	R3248	R3249	R3254	R3253	R3226	R3224	ALS/ACS
DNP	DNP	ALL	ALL	ALL	ALL	DNP	DNP	ACS (I2C4) I2C4_SCL I2C4_SDA
DNP	DNP	DNP	DNP	DNP	DNP	ALL	ALL	ALS ISH1 PCH_SENSOR_ISH_SCL PCH_SENSOR_ISH_SDA
ALL	ALL	DNP	DNP	DNP	DNP	DNP	DNP	ALS I2C3 ALS_I2C3_SCL ALS_I2C3_SDA

Acc/Gyro

Critical Layout Note for Mems devices:
- No traces under part,
- No vias in pads or directly under part,
- All traces entering pads to to be same width,
- All traces to enter pads at zero angle.
- All pads to have a trace, even if it is a stub

Clocking rotation controlled by MEdrawing.
(+X Device & +X Surface vectors must be parallel w/same direction

7-bit I2C Address = 0x68

Changed from +3P3VSB

Removed DND connection on OCSB

Removes "backdoor" i2c bus. R3222 & R3223

To ISH
AGYRO_INT1# 25
AGYRO_SAM_INT# 34

To SAM

To ISH
when in S0

To SAM
full time

Magnetometer

12/19 Vander request change to 0

7-bit i2c
Address
0x30

12/19 Vander request change to DNP

Added series jumper to TCAP

Near PinA1

Gyro and Magnetometer reference Hobart

Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm
... on any layer.
Clocking rotation controlled by MEdrawing.

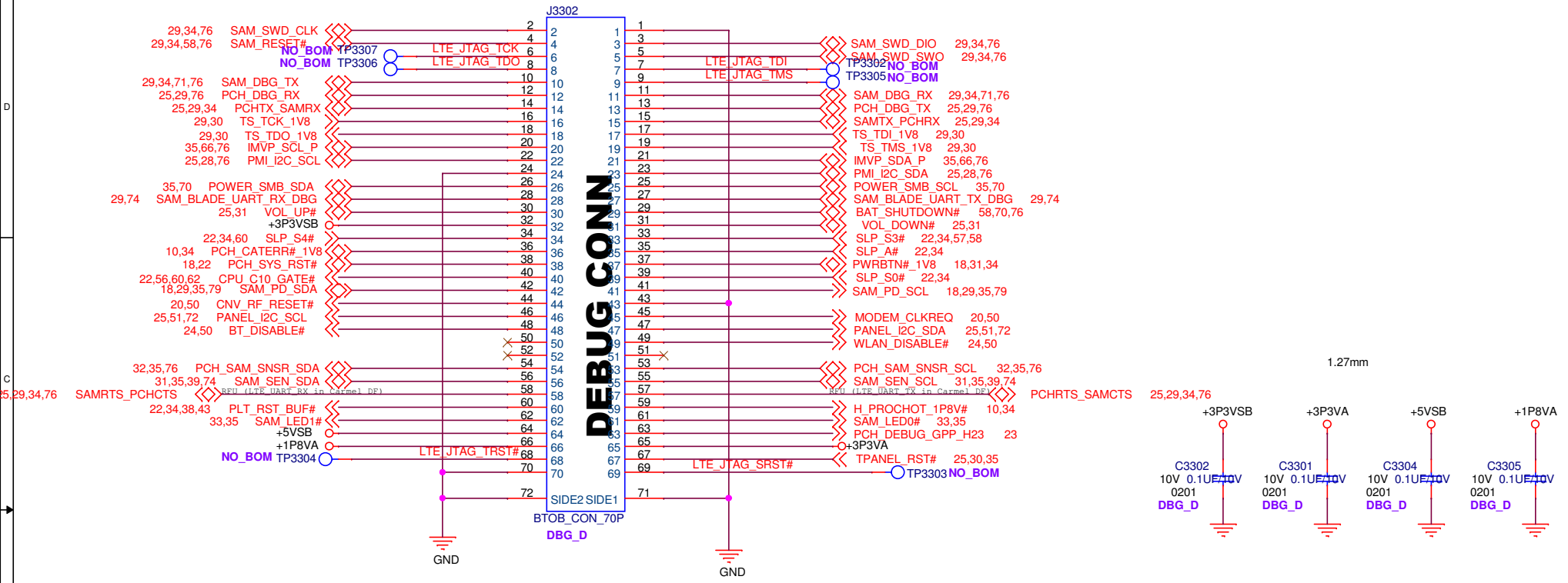
Power-Down
To put the ISL29033 into a power-down state, the user can set [7 to 5] bits to 0 in Register 0. Or more simply, set all of Register 0 to 0x00. This should be the default when the screen is off.

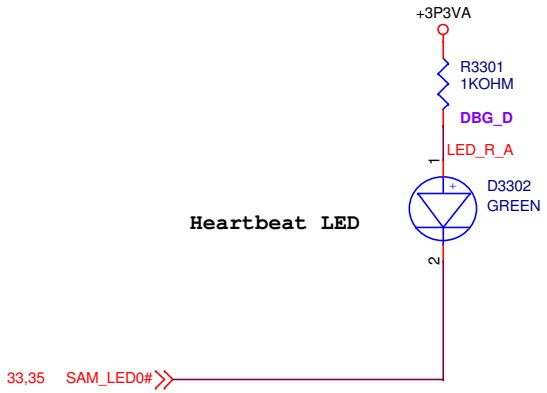
ALS field of view to be >55 degrees Half Angle Half Power
To acheive this FOV
- assuming a 48+/-6um uhole array on 150um centers contained in 4.3mm aperture,
- the top of the ALS chip should reside 1100um below the glass.

This should provide transmisivity [6% >%T(lambda) > 10.5% for [390nm < lambda <1000nm].
It would be prudent to control the uhole array using 30 random samples of 5 uholes measured by CMM/OMM

Report errors to Steven

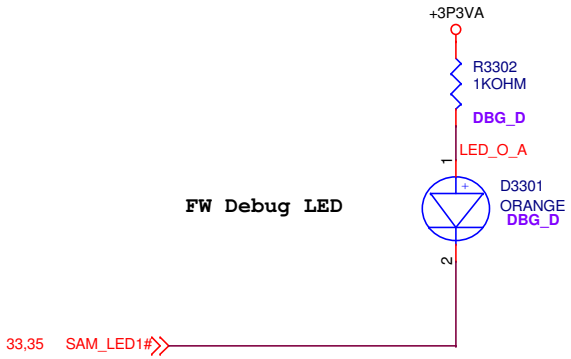
Title: On Board-Sensors
Engineer: <OrgAddr1>
Size: Custom | Project Name: B52 | Rev: 1.00
Date: Friday, June 28, 2019 | Sheet 32 of 82
W x H 462 x 299 mm





Heartbeat LED

LOW = LED ON



FW Debug LED

LOW = LED ON

<Core Design>

Title: Debug Conn

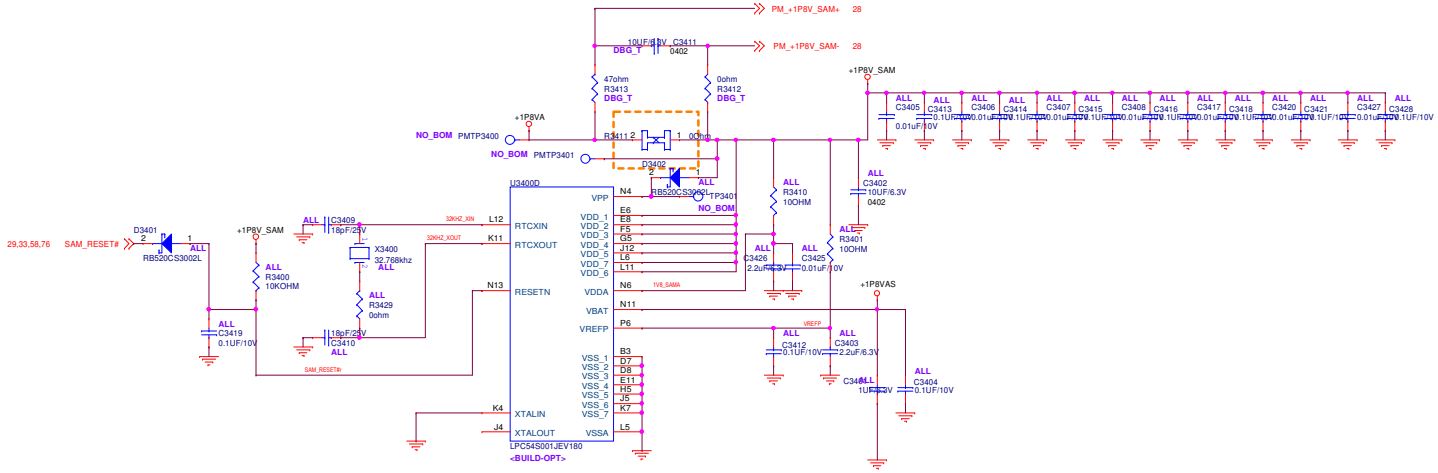
<OrgName> Engineer: <OrgAddr1>

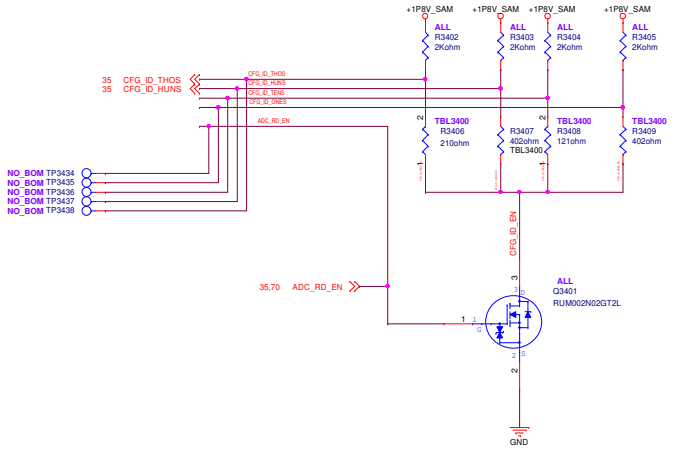
Size	Project Name	Rev
Custom	B52	1.00

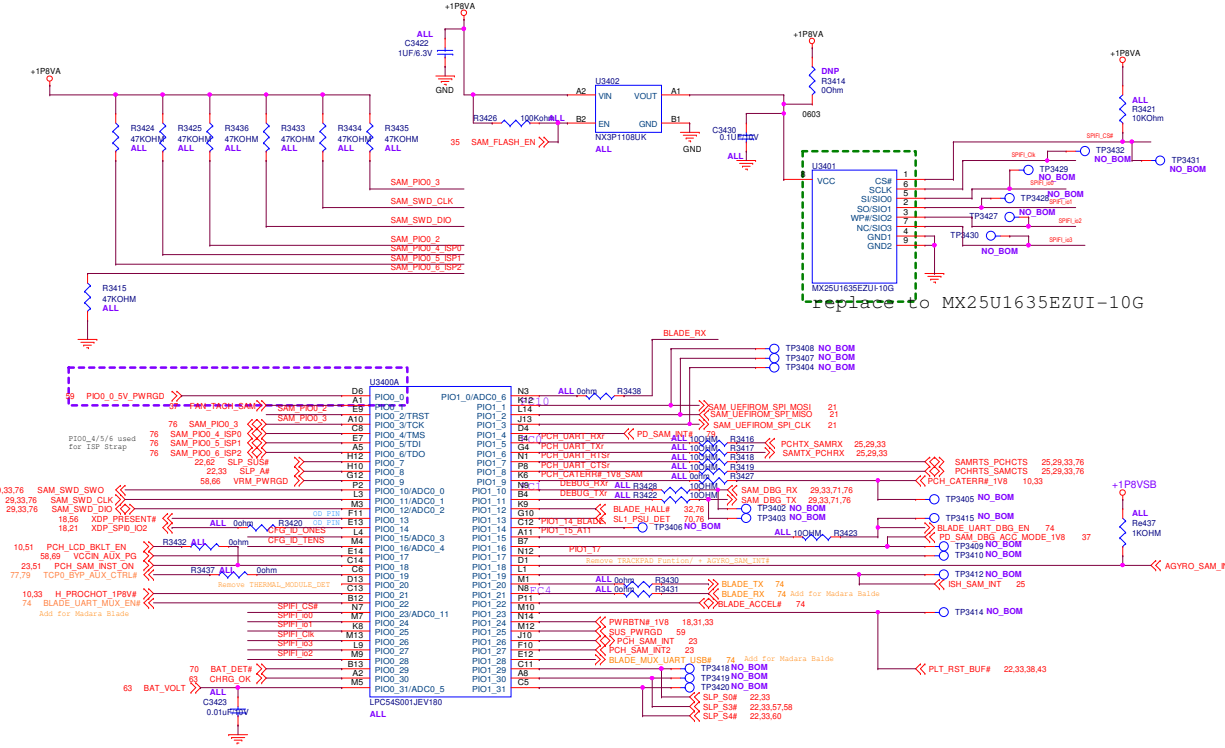
Date: Friday, June 28, 2019 Sheet 33 of 82

W x H 337 x 218 mm

System Aggregator Module







Which Sku Program ID for JALAMA TBL 3400

TBL 3400

SKU ID -ADC0-CFG_ID_ONES_PIO0 _15/ADC0_3

HEX number	binary	Decimal	R3409(ohm)	ADC count lower limit	ADC count upper limit	Jalama
0	0000	0	1	0	114	
1	0001	1	121	115	309	
2	0010	2	210	310	464	
3	0011	3	301	465	607	
4	0100	4	402	608	755	ACS+NUVOTON TPM+wifi 1216
5	0101	5	510	756	904	ACS+NATIONZ TPM+wifi 1216
6	0110	6	634	905	1078	ACS+fTPM+dual MEM
7	0111	7	806	1079	1271	ACS+fTPM+single MEM
8	1000	8	1000	1272	1485	ALS+NUVOTON TPM+wifi 1216
9	1001	9	1300	1486	1756	ALS+NATIONZ TPM+wifi 1216
A	1010	10	1740	1757	2060	ALS+fTPM+dual MEM
B	1011	11	2370	2061	2398	ALS+fTPM+single MEM
C	1100	12	3400	2399	2765	
D	1101	13	4990	2766	3166	
E	1110	14	10000	3167	3676	
F	1111	15	100000	3672	4096	

Memory_ID_ADC1-CFG_ID_TENS-PIO0 _16/ADC0_4

HEX number	binary	Decimal	R3408(ohm)	ADC count lower limit	ADC count upper limit	Jalama
0	0000	0	1	0	114	LP4x_2GB_K4U6E3S4AA-MGCL_SAMSUNG_M1100585-001
1	0001	1	121	115	309	LP4x_4GB_K4UBE3D4AA-MGCL_SAMSUNG_M1100590-001
2	0010	2	210	310	464	LP4x_2GB_MT53E512M32D2NP-046 WT:E_Micron
3	0011	3	301	465	607	LP4x_4GB_MT53E1G32D4NQ-046 WT:E_Micron
4	0100	4	402	608	755	
5	0101	5	510	756	904	LP4x_2GB_H9HCNNNBKMALHR-NEE_Hynix_M1102096-001
6	0110	6	634	905	1078	LP4x_4GB_H9HCNNNCPMALHR-NEE_Hynix_M1102097-001

Build_ID_ADC2-CFG_ID_HUNS-PIO2 _0/ADC0_7

HEX number	binary	Decimal	R3407(ohm)	ADC count lower limit	ADC count upper limit	Jalama
0	0000	0	1	0	114	Jalama Pre EV0.9
1	0001	1	121	115	309	Jalama EV1.0A
2	0010	2	210	310	464	Jalama EV1.0B
3	0011	3	301	465	607	Jalama EV1.5
4	0100	4	402	608	755	Jalama DV0.9
5	0101	5	510	756	904	Jalama DV1.0
6	0110	6	634	905	1078	Jalama DV1.0B Debug
7	0111	7	806	1079	1271	Jalama DV1.0B Retl
8	1000	8	1000	1272	1485	Jalama DV1.0C Debug
9	1001	9	1300	1486	1756	Jalama DV1.0C Retl

Program_ID_ADC3-CFG_ID_THOS-PIO2 _1/ADC0_8

HEX number	binary	Decimal	R3406(ohm)	ADC count lower limit	ADC count upper limit	Jalama
0	0000	0	1	0	114	
1	0001	1	121	115	309	
2	0010	2	210	310	464	Jalama
3	0011	3	301	465	607	

replace to MX25U1635EZUI-10G

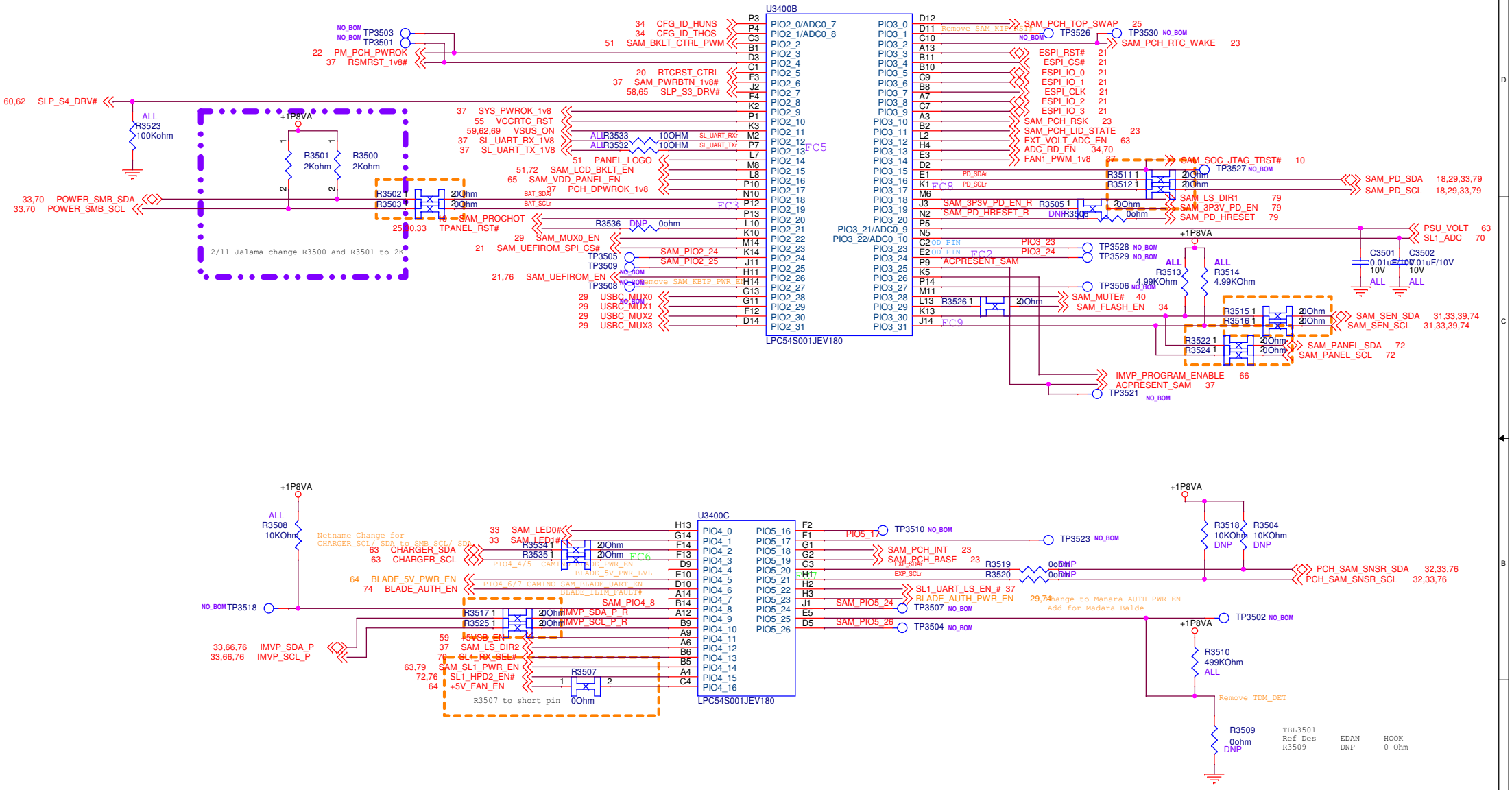
W x H 482 x 318 mm

Title: SAM Power, ADC, & Debug

<OrgName> Engineer: <OrgAddr1>

Size: A2 | Project Name: B52 | Rev: 1.00

Date: Friday, June 28, 2019 | Sheet 34 of 82


U3400B
LPC54S001JEV180
U3400C
LPC54S001JEV180
+1P8VA
2/11 Jalama change R3500 and R3501 to 2K
R3507 to short pin 0Ohm
Remove SAM_KBTP_PWR_EN
Remove TDM_DET
Netname Change for CHARGER_SCL/SDA to SMB_SCL/SDA
Change to Manara AUTH PWR EN
Add for Madara Balde
TBL3501
Ref Des EDAN HOOK
R3509 DNP 0 Ohm
Title: SAM Buses
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 35 of 82
W x H:387 x 257 mm
PCH

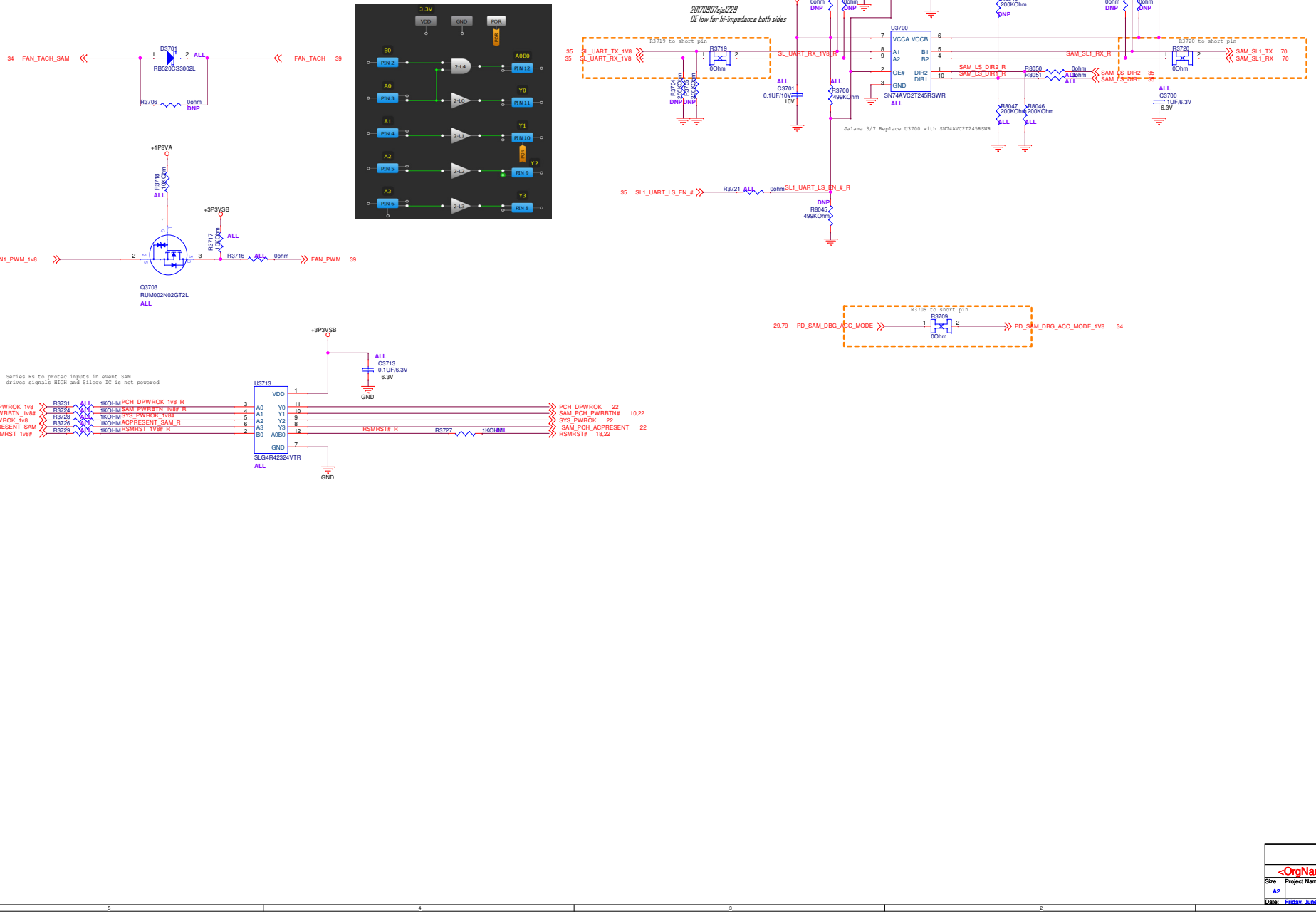
Title: Blank

<OrgName>

Enclosure: <OrgAddr1>

Size: A1 | Project Name: B52 | Rev: 1.00

Date: Friday, June 28, 2013 | Sheet: 36 of 52



Title: SAM Level Shifters

<OrgName> Engineer: <OrgAddr1>

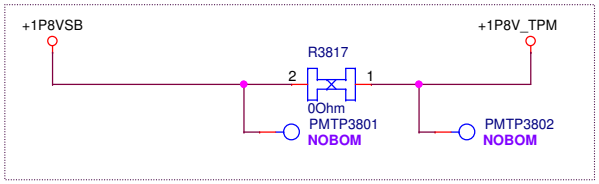
Size	Project Name	Rev
A2	B52	1.00

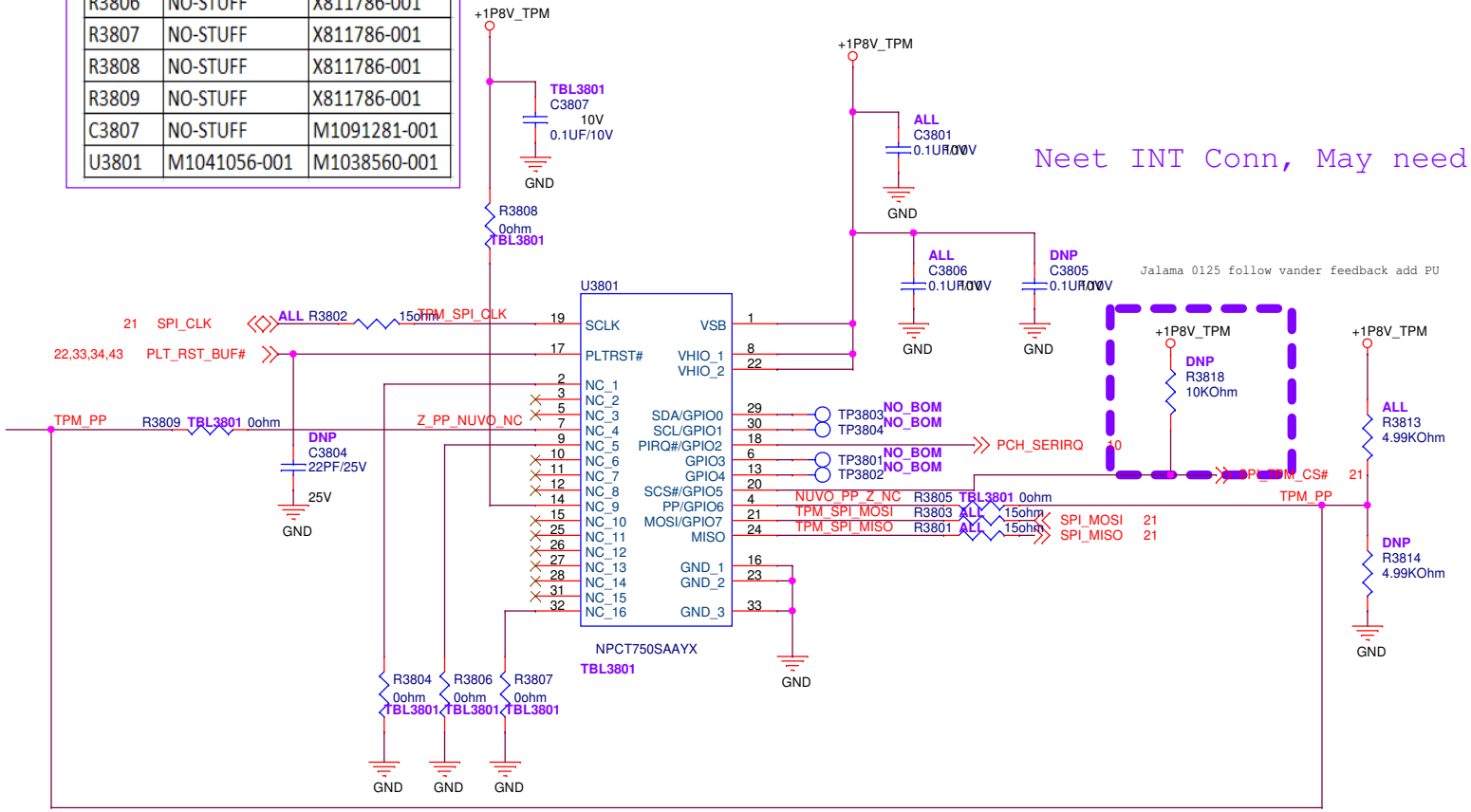
Date: Friday, June 28, 2019 Sheet 37 of 82

Trusted Platform Module

TBL3801

TBL3801		
Ref	Nuvoton	NationZ
R3804	NO-STUFF	X811786-001
R3805	X811786-001	NO-STUFF
R3806	NO-STUFF	X811786-001
R3807	NO-STUFF	X811786-001
R3808	NO-STUFF	X811786-001
R3809	NO-STUFF	X811786-001
C3807	NO-STUFF	M1091281-001
U3801	M1041056-001	M1038560-001



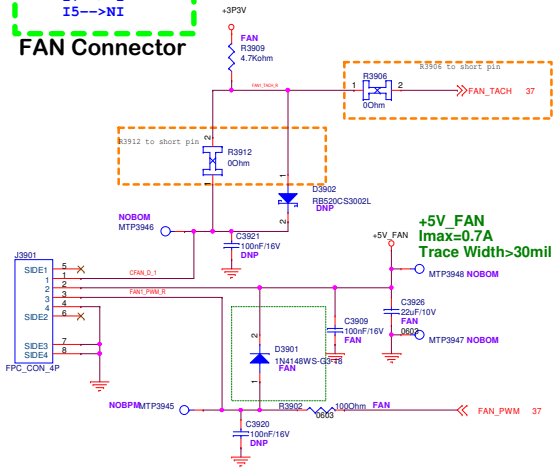


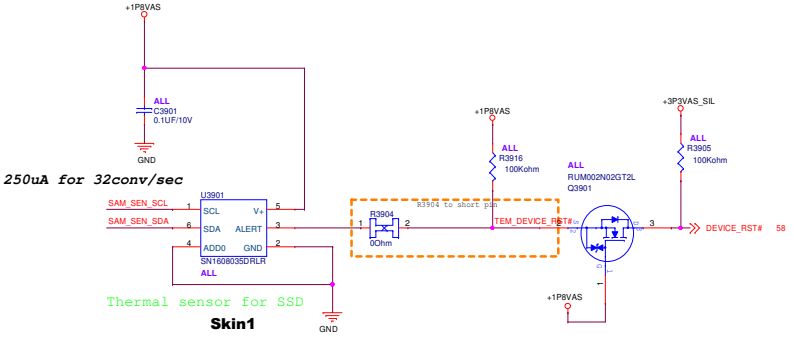
Title: TPM			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 38 of 82		

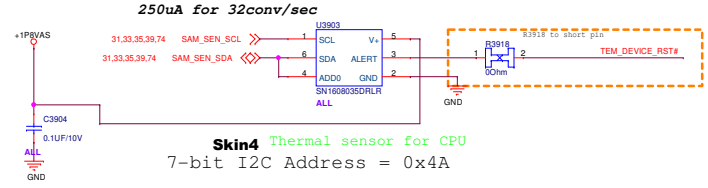
W x H 357 x 231 mm

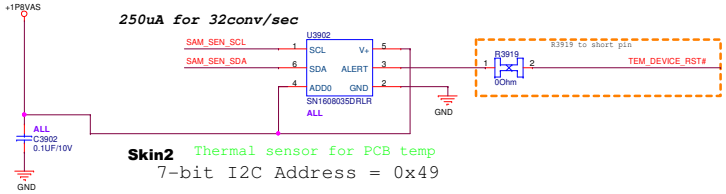
2018/12/27
FAN Table
I7--> I
I5-->NI

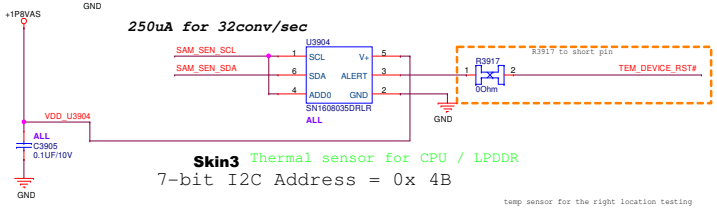
FAN Connector











temp sensor for the right location testing

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

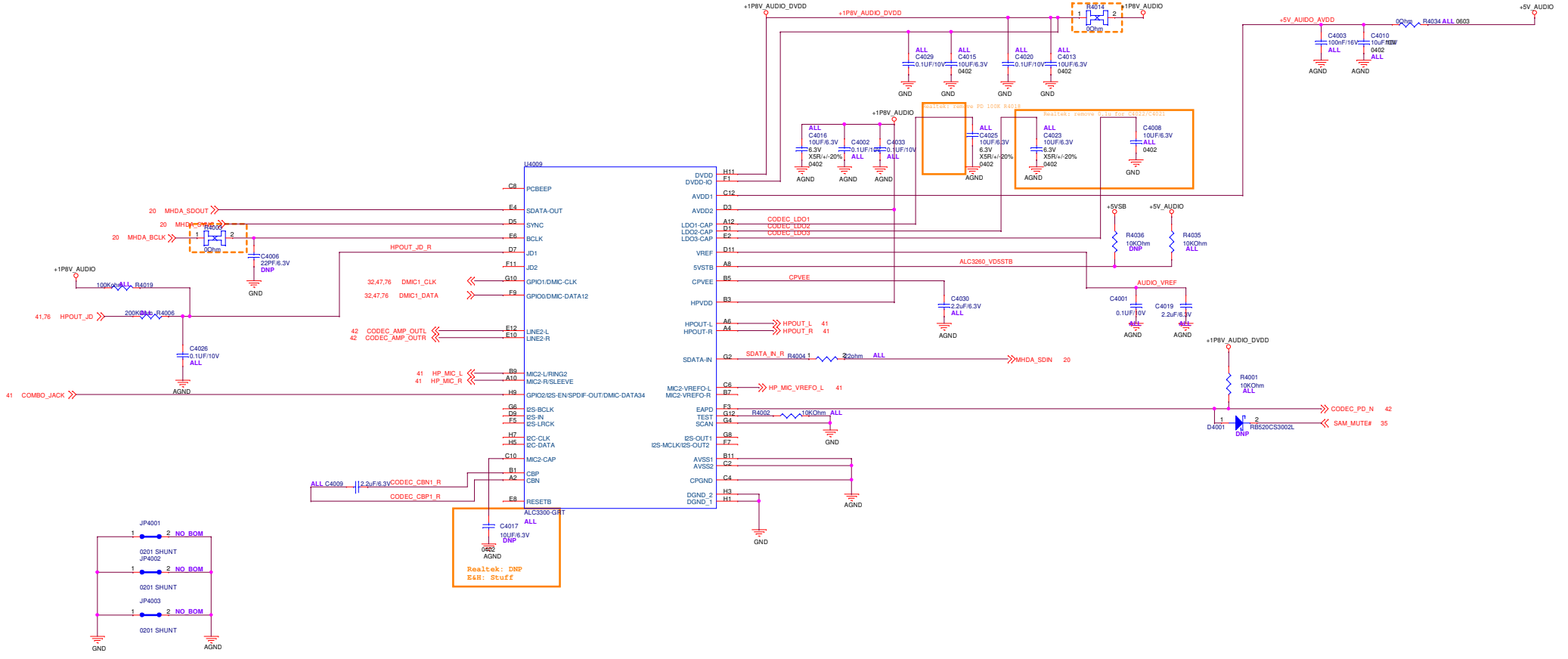
SAM_SEN_SCL — SAM_SEN_SCL 31,33,35,39,74
SAM_SEN_SDA — SAM_SEN_SDA 31,33,35,39,74

20160827sjs0527: Temp Sensor/System Fan

Report errors to Steven

W x H 387.1 x 258 mm

Title:	Temp Sensor/System Fan	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 39 of 82	

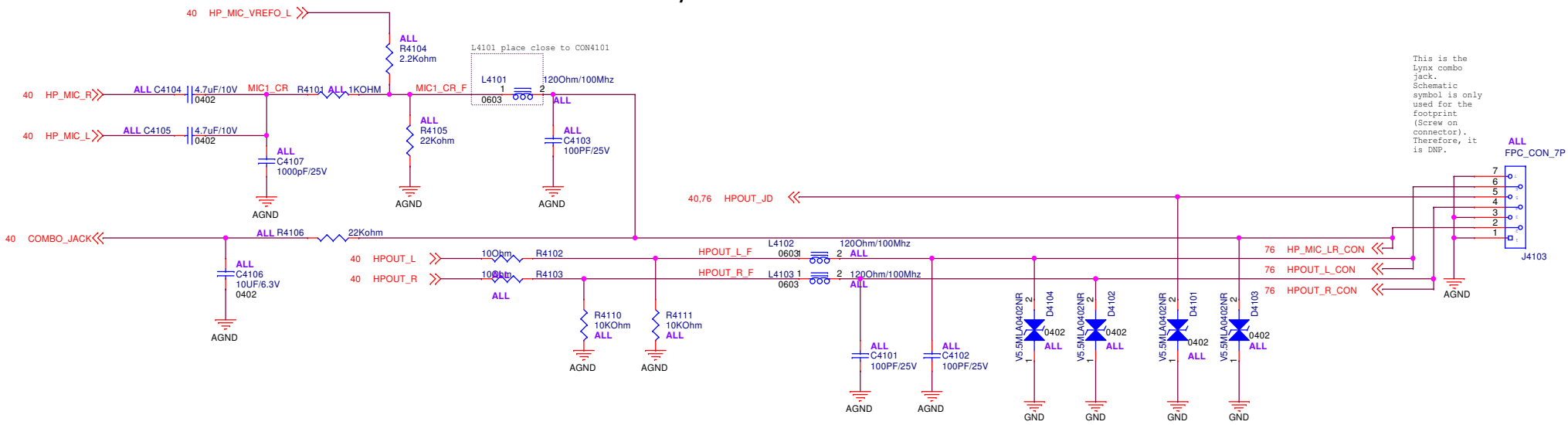


Title:	REALTEK ALC3269C_81BGA		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: B52		Rev: 1.0.0.1
Date: Friday, June 28, 2019	Sheet 40 of 82		

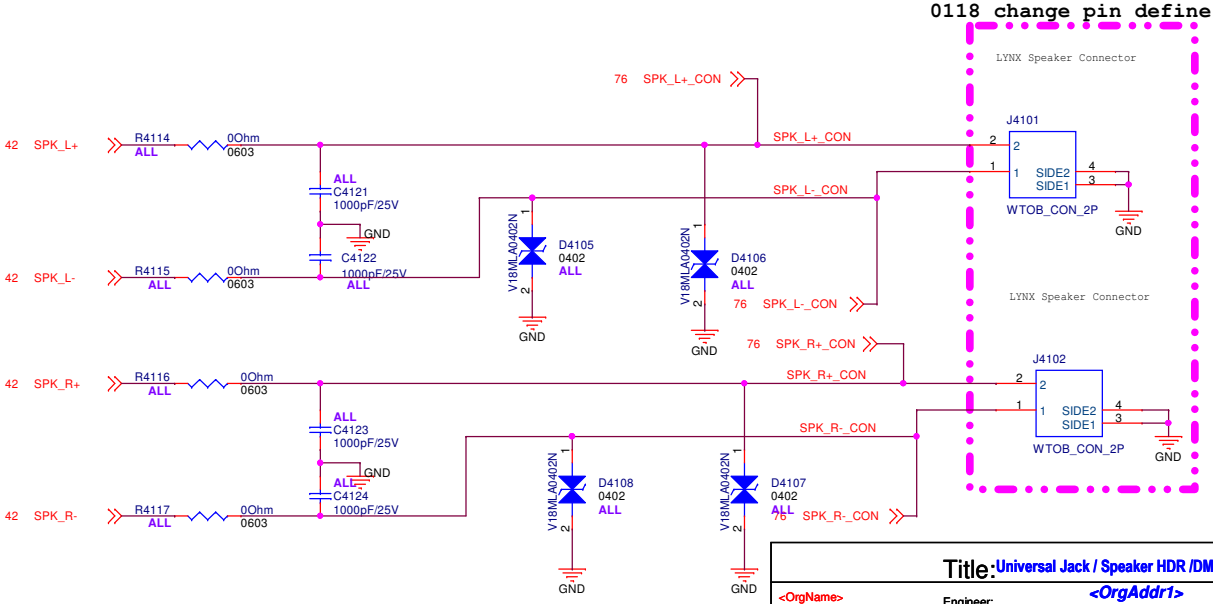
W x H 427 x 275 mm

HP/MIC1 Combo Jack

This Page reference Marada



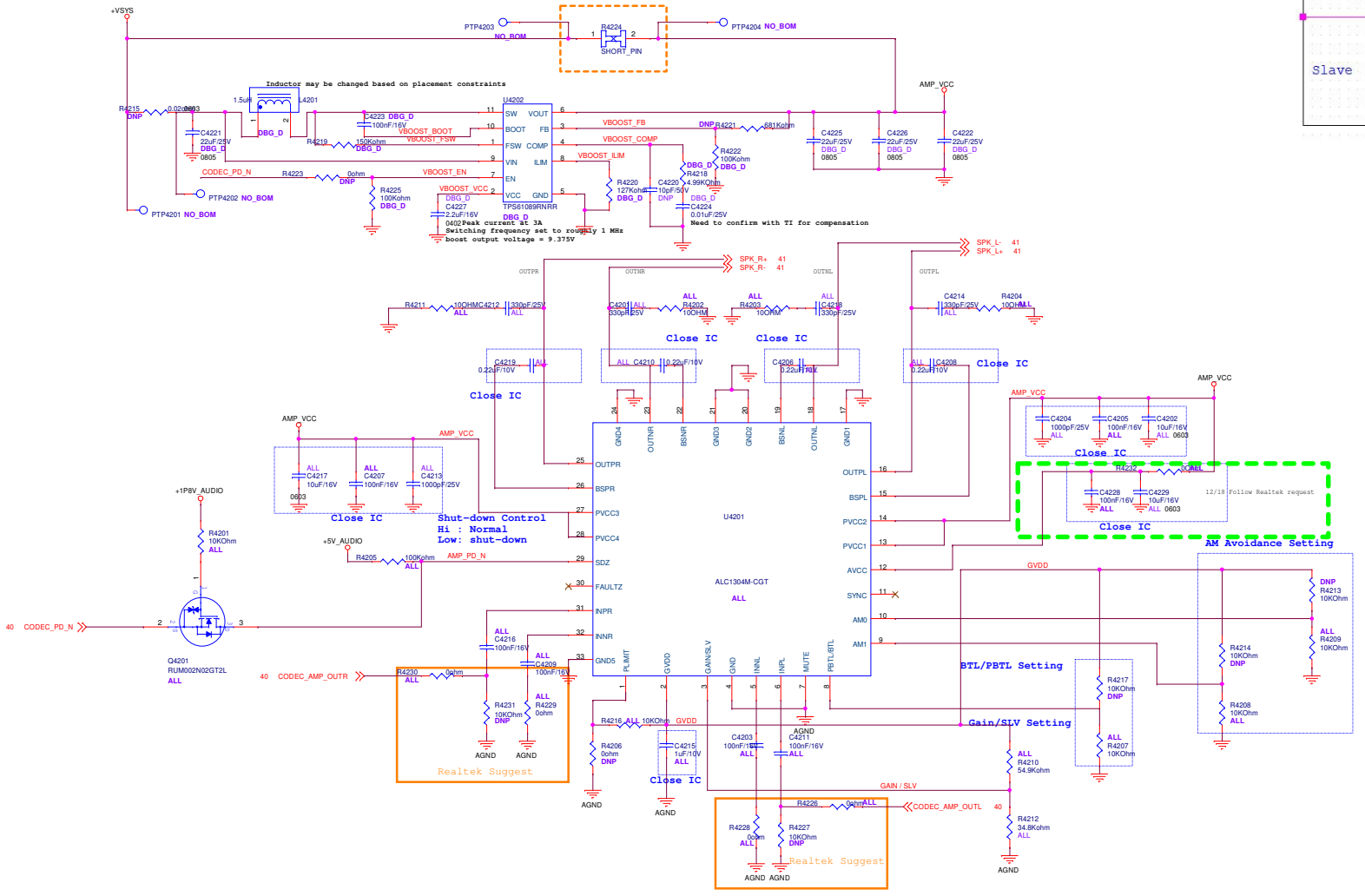
0118 change pin define



Title:	Universal Jack / Speaker HDR /DMIC HDR		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 41 of 82		

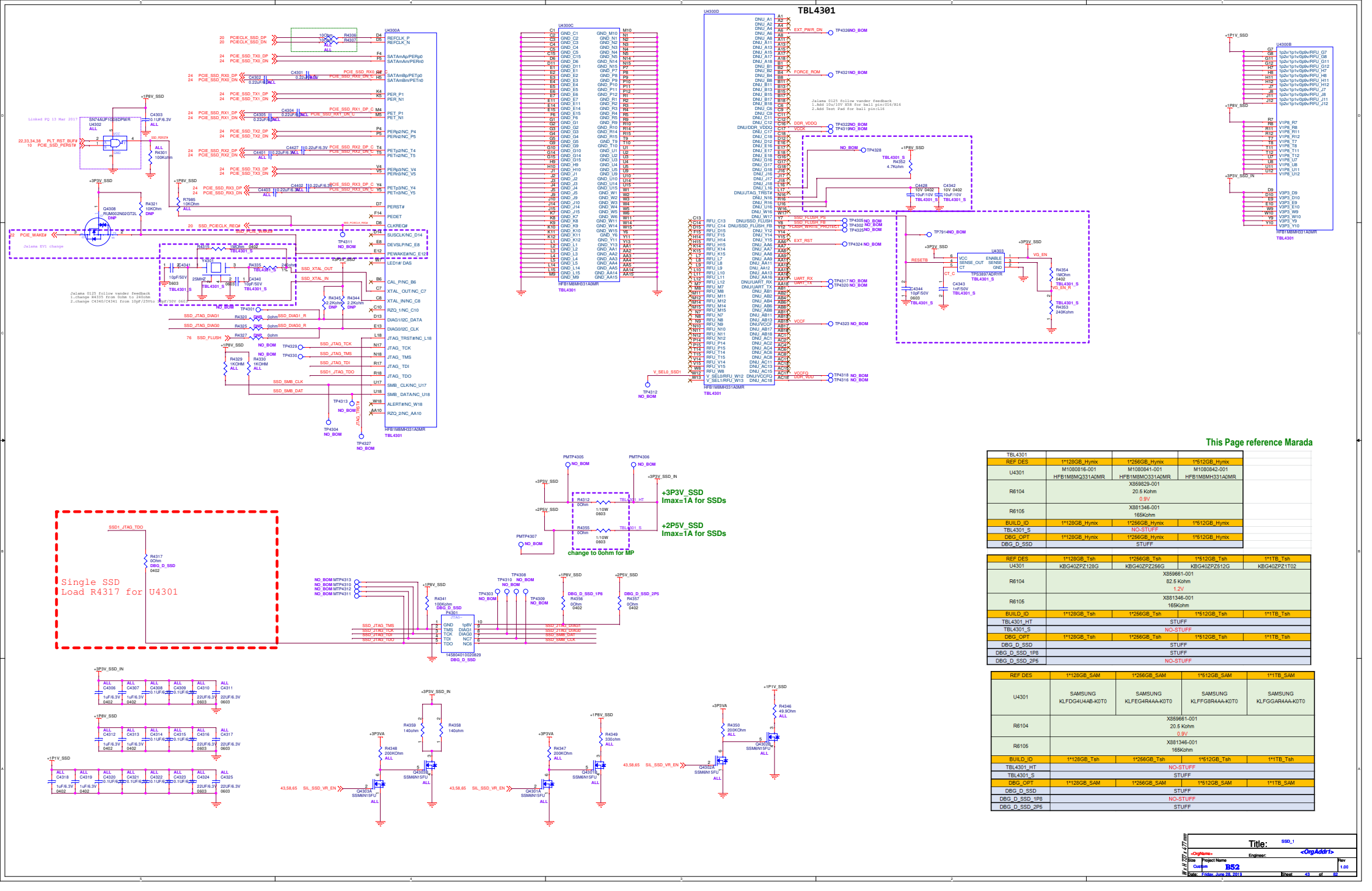
R4210 R4212

Mode	Gain	RX(ohm)	RY(ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	15dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	15dB	0	NC



AM1	AM0	PWM SW Frequency (KHz)		
		Min.	Typical	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250

Title: ALC1304 AMP			
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 42 of 82		



TBL4301			
REF DES	1*128GB_Hynix	1*256GB_Hynix	1*512GB_Hynix
U4301	M1080816-001 HFB1M8MQ331A0MR	M1080841-001 HFB1M8MO331A0MR	M1080842-001 HFB1M8MH331A0MR
R6104	X859829-001 20.5 Kohm 0.9V		
R6105	X881346-001 165Kohm		
BUILD_ID	1*128GB_Hynix	1*256GB_Hynix	1*512GB_Hynix
TBL4301_S	NO-STUFF		
DBG_OPT	1*128GB_Hynix	1*256GB_Hynix	1*512GB_Hynix
DBG_D_SSD	STUFF		

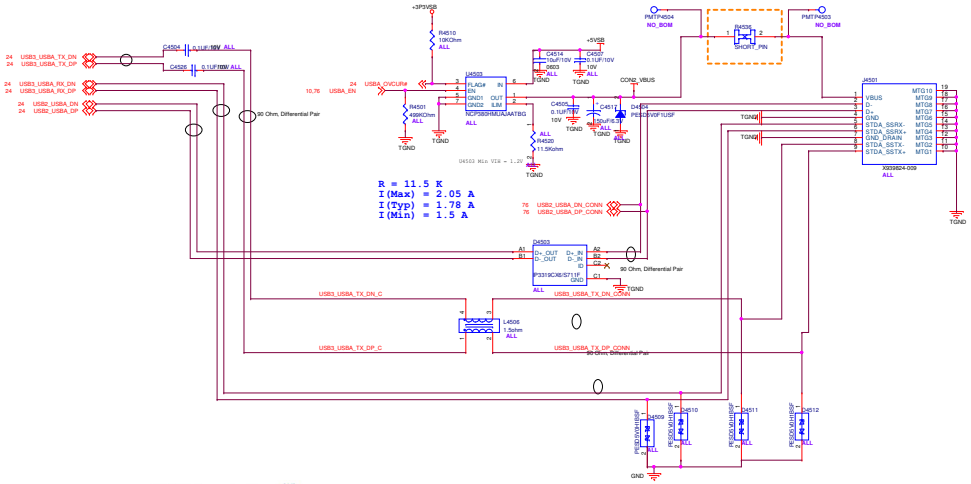
REF DES	1*128GB_Tsh	1*256GB_Tsh	1*512GB_Tsh	1*1TB_Tsh
U4301	KBG40ZPZ128G	KBG40ZPZ256G	KBG40ZPZ512G	KBG40ZPZ1T02
R6104	X859661-001 82.5 Kohm 1.2V			
R6105	X881346-001 165Kohm			
BUILD_ID	1*128GB_Tsh	1*256GB_Tsh	1*512GB_Tsh	1*1TB_Tsh
TBL4301_HT	STUFF			
TBL4301_S	NO-STUFF			
DBG_OPT	1*128GB_Tsh	1*256GB_Tsh	1*512GB_Tsh	1*1TB_Tsh
DBG_D_SSD	STUFF			
DBG_D_SSD_1P8	STUFF			
DBG_D_SSD_2P5	NO-STUFF			

REF DES	1*128GB_SAM	1*256GB_SAM	1*512GB_SAM	1*1TB_SAM
U4301	SAMSUNG KLFDG4U4AB-K0T0	SAMSUNG KLFEG4R4AA-K0T0	SAMSUNG KLFFG8R4AA-K0T0	SAMSUNG KLFGGAR4AA-K0T0
R6104	X859661-001 20.5 Kohm 0.9V			
R6105	X881346-001 165Kohm			
BUILD_ID	1*128GB_Tsh	1*256GB_Tsh	1*512GB_Tsh	1*1TB_Tsh
TBL4301_HT	NO-STUFF			
TBL4301_S	STUFF			
DBG_OPT	1*128GB_SAM	1*256GB_SAM	1*512GB_SAM	1*1TB_SAM
DBG_D_SSD	STUFF			
DBG_D_SSD_1P8	NO-STUFF			
DBG_D_SSD_2P5	STUFF			

Title: SSD_1
<OrgName> Engineer: <OrgAddr1>
Size: Custom | Project Name: B52 | Rev: 1.00
Date: Friday, June 28, 2019 | Sheet 43 of 82

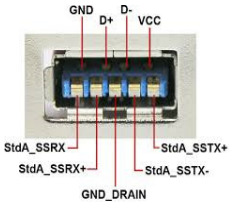
Title:	Blank				
<OrgName>	Engineer:	<OrgAddr1>			
Size: Custom	Project Name: B52				Rev: 1.00
Date: Friday, June 28, 2019		Sheet 44 of 82			

W x H 557.4 x 425 mm

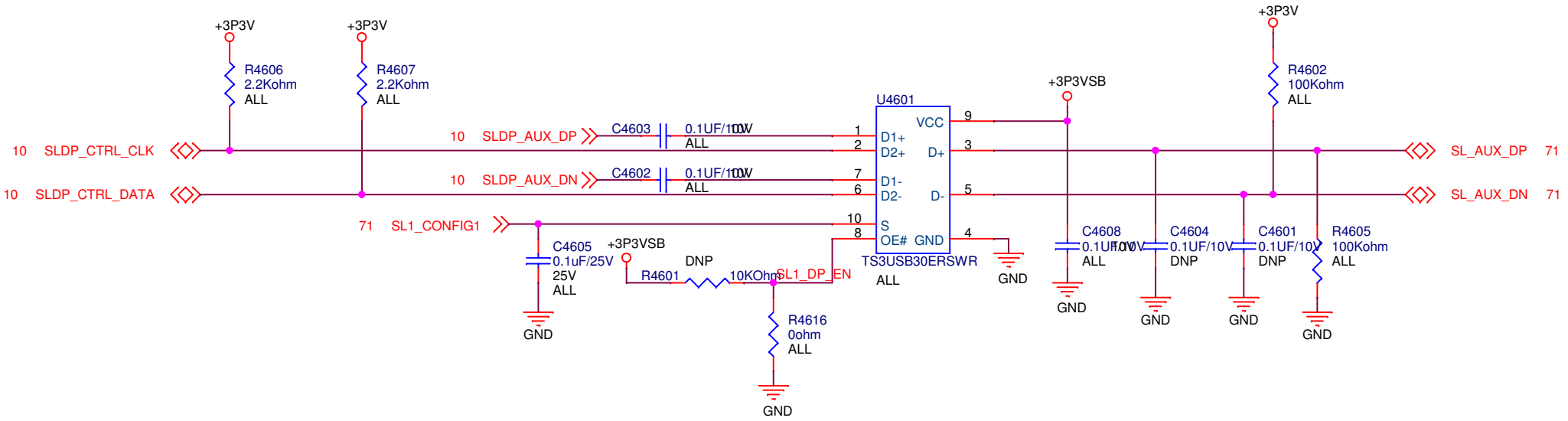


USB 3.0 Connector Pinouts[44]

Pin	Color	Signal name ("A" Connector)	Signal name ("B" Connector)	Description
Shell	N/A	Shield		Metal housing
1	Red	VBUS		Power
2	White	D−		USB 2.0 differential pair
3	Green	D+		
4	Black	GND		Ground for power return
5	Blue	StdA_SSRX−	StdB_SSTX−	SuperSpeed transmitter differential pair
6	Yellow	StdA_SSRX+	StdB_SSTX+	
7	N/A	GND_DRAIN		Ground for signal return
8	Purple	StdA_SSTX−	StdB_SSRX−	SuperSpeed receiver differential pair
9	Orange	StdA_SSTX+	StdB_SSRX+	



Title:	USB3.0 Port
<OrgName>	Engineer: <OrgAddr1>
Size: A1	Project Name: B52
Rev: 1.00	
Date: Friday, June 28, 2019	Sheet 48 of 82



TS3USB30E

EN	S	Connection
L	**L**	AUX for DP [D1 to D]
L	**H**	DDC for HDMI [D2 to D]
H	X	HI-Z

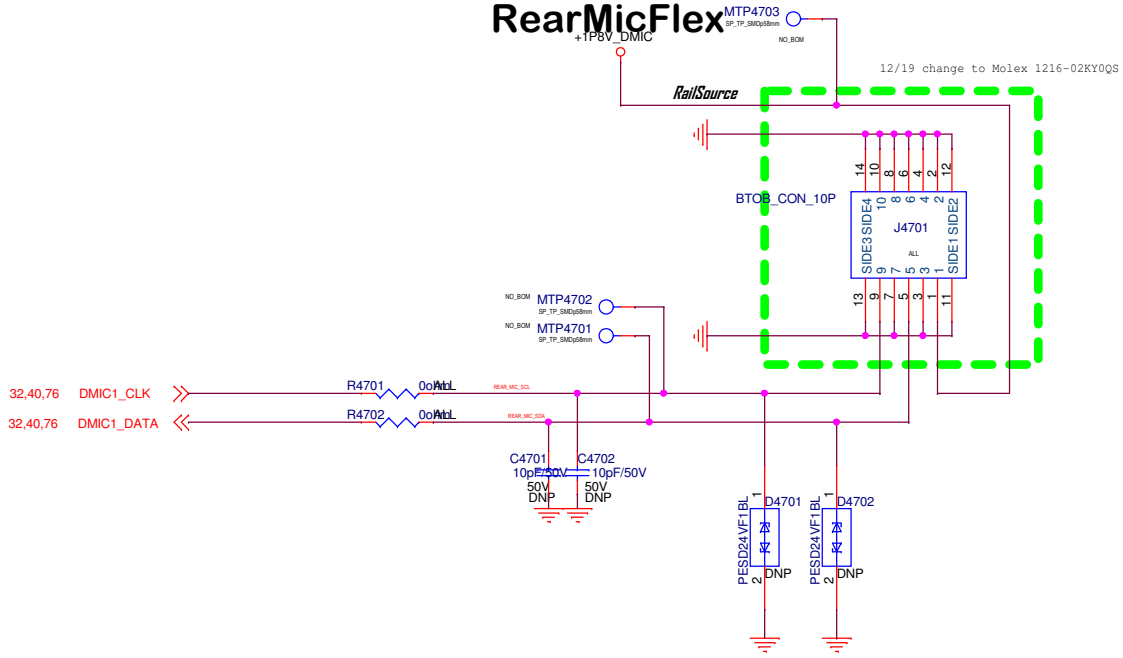
W x H 337 x 218 mm

Title:	DP Dongle Control	
<OrgName>	Engineer:	<OrgAddr1>
Size: A4	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 46 of 82	

This Page reference Marada

To

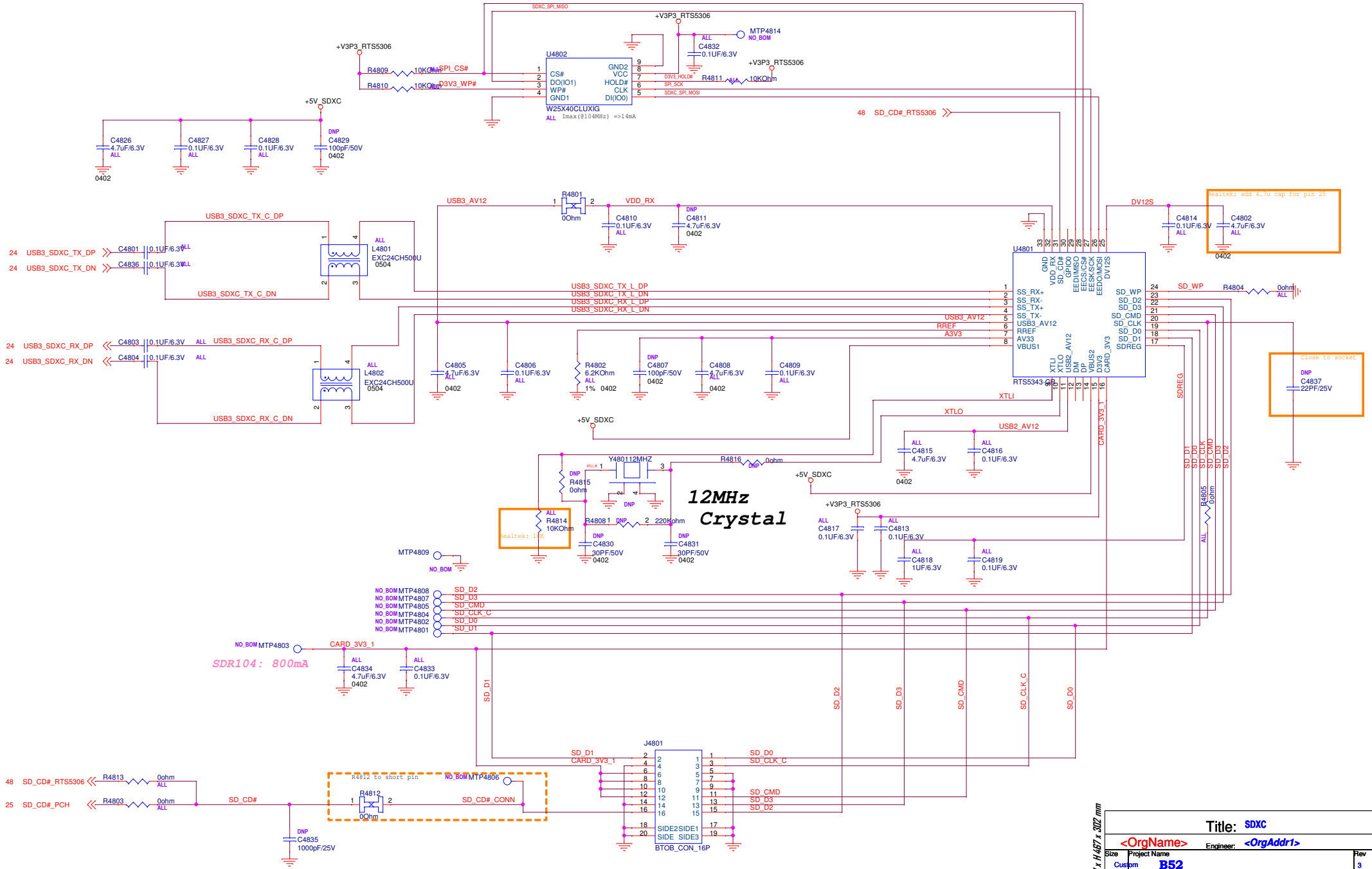
RearMicFlex



Title:	Microphone_rear		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019		Sheet 47 of 82	

W x H, 392 x 256 mm

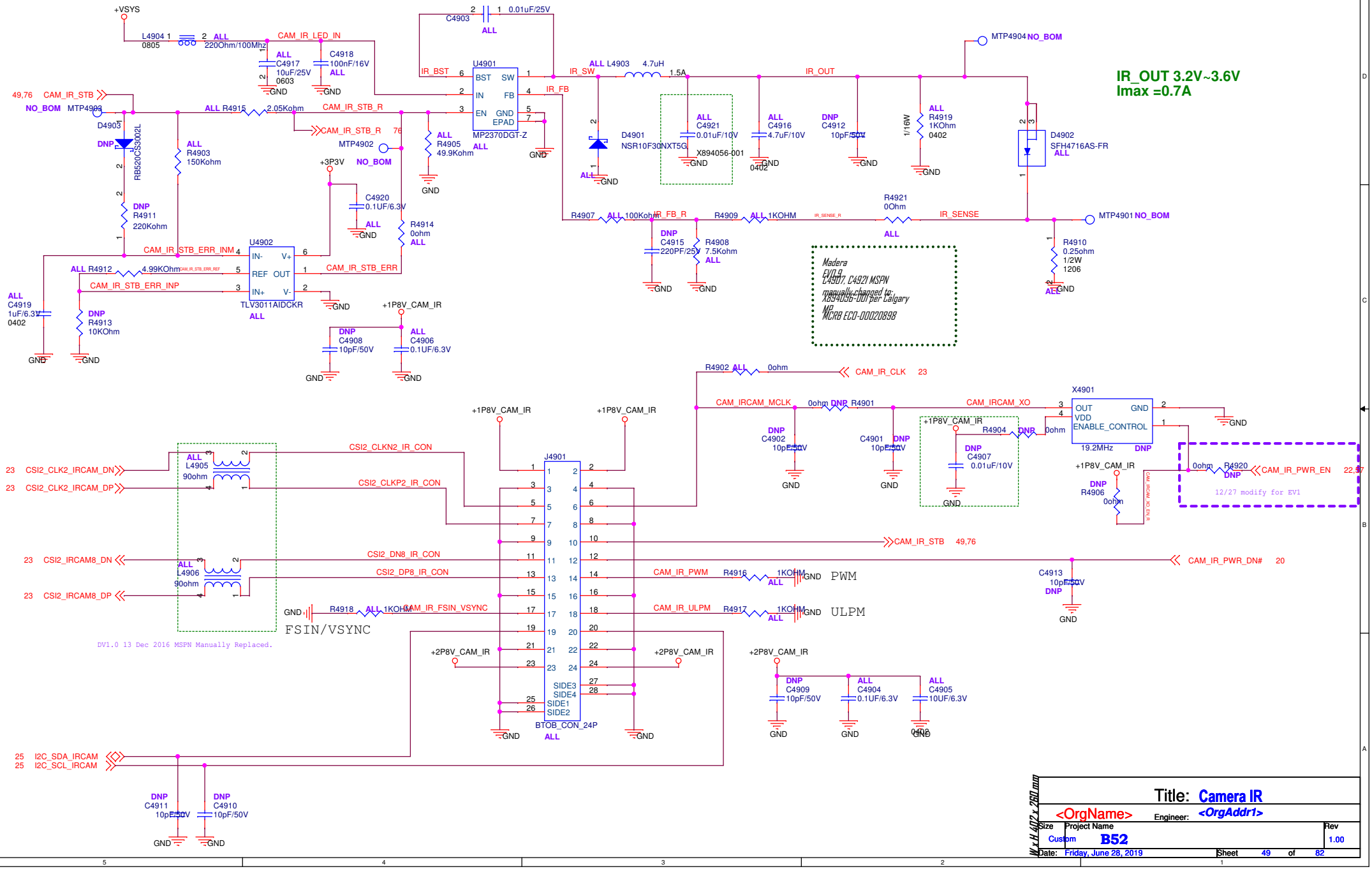
This Page reference Marada



Title:	SDXC		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: B52		Rev: 3
Date: Friday, June 28, 2019	Sheet 48 of 82		

W x H 467 x 302 mm

This Page reference Marada

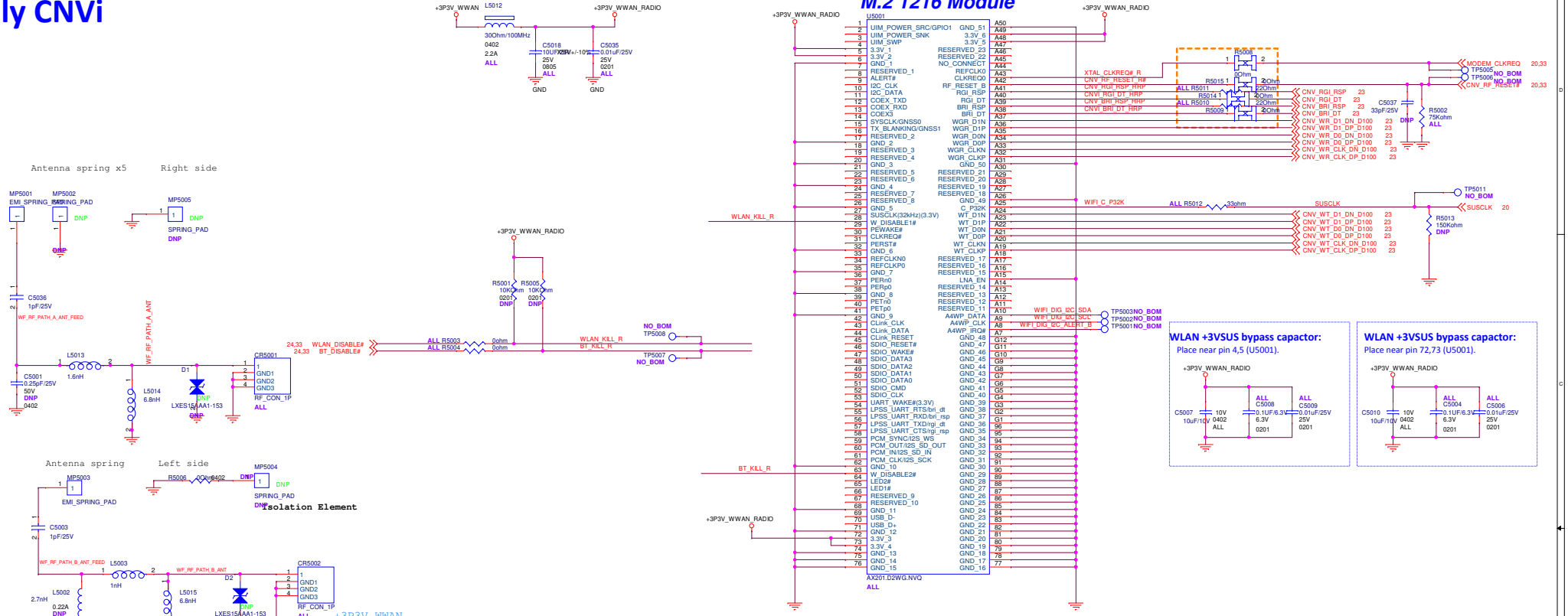


New 1216 Type

WLAN+BT (M.2 1216)
Only CNVi

M.2 1216 Module

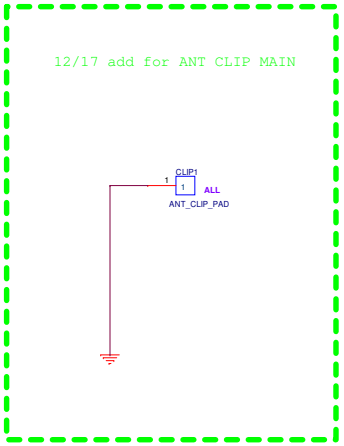
REFCLK not used by ICL-HrP

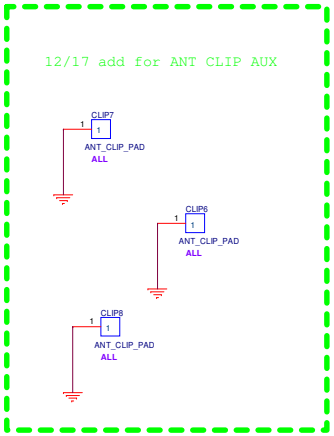


+3P3V_WWAN
3.3V +/- 0.165V
200 mVPP, 10-500kHz
300 mVpp -- allowed power rail noise
TRISE (0-3.3V) < 10mSec
RISING EDGE SHALL BE WITHOUT GLITCHES OR STEPS
RIPPLE SHALL NOT DIP MORE THAN 0.3V; OTHERWISE MAY BE INTERPRETED AS POR

LAYOUT NOTE:
CNV*D100 nets routed as 85-Ohm differential pairs

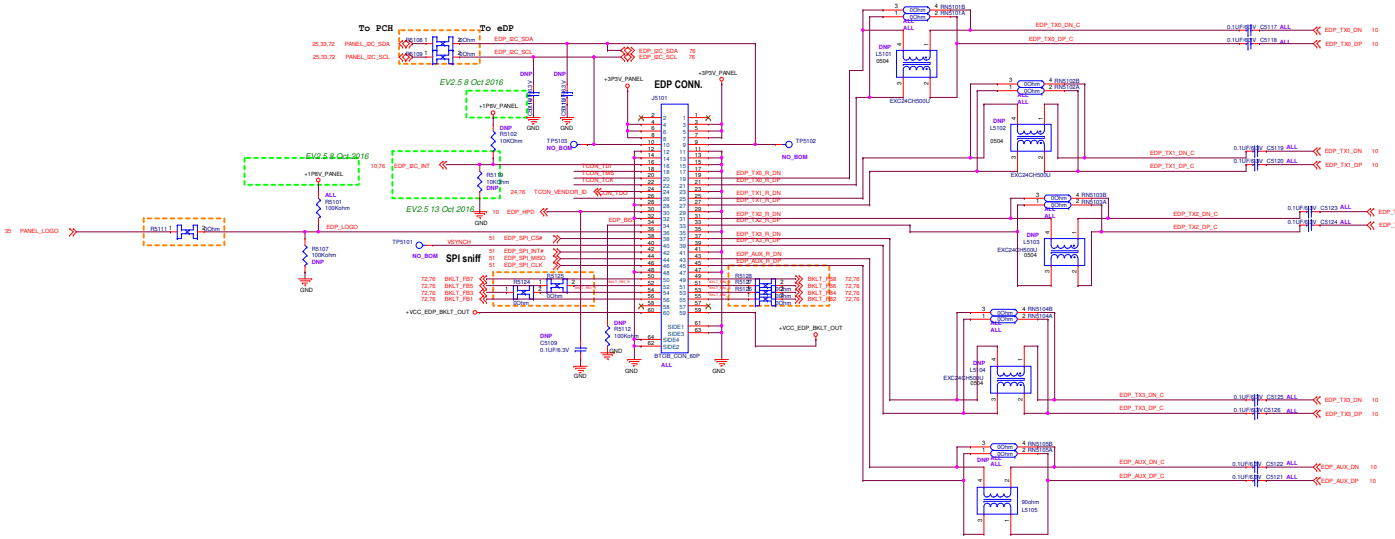
LAYOUT NOTE:
PLACE CNV_WT* TPS NEAR U5001;
Stubbs should be minimized and limited to just a VIA for access
Consider removing CNV_WT* TPs in later builds

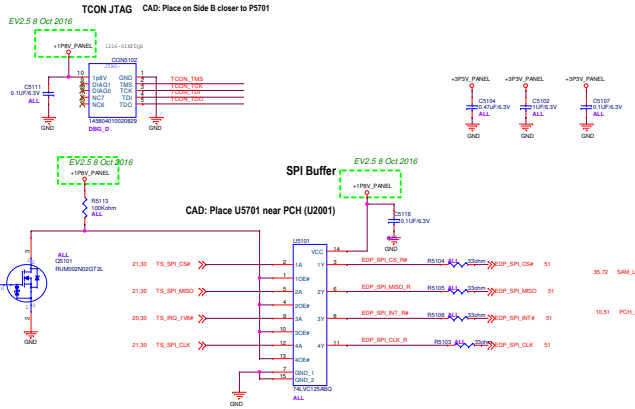


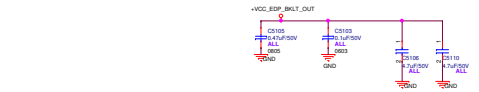


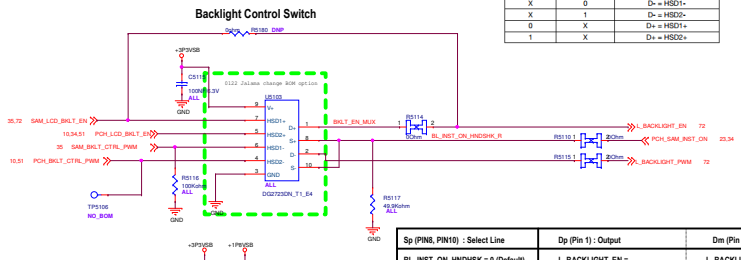
Title:	WI-FI_BT Coex	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 50 of 82	

This Page reference Marada

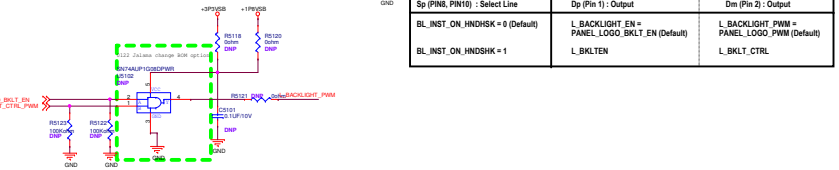








TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+



Sp (PIN8, PIN10) : Select Line	Dp (Pin 1) : Output	Dm (Pin 2) : Output
BL_INST_ON_HNDHSK = 0 (Default)	L_BACKLIGHT_EN = PANEL_LOGO_BKLT_EN (Default)	L_BACKLIGHT_PWM = PANEL_LOGO_PWM (Default)
BL_INST_ON_HNDSHK = 1	L_BKLTEN	L_BKLT_CTRL

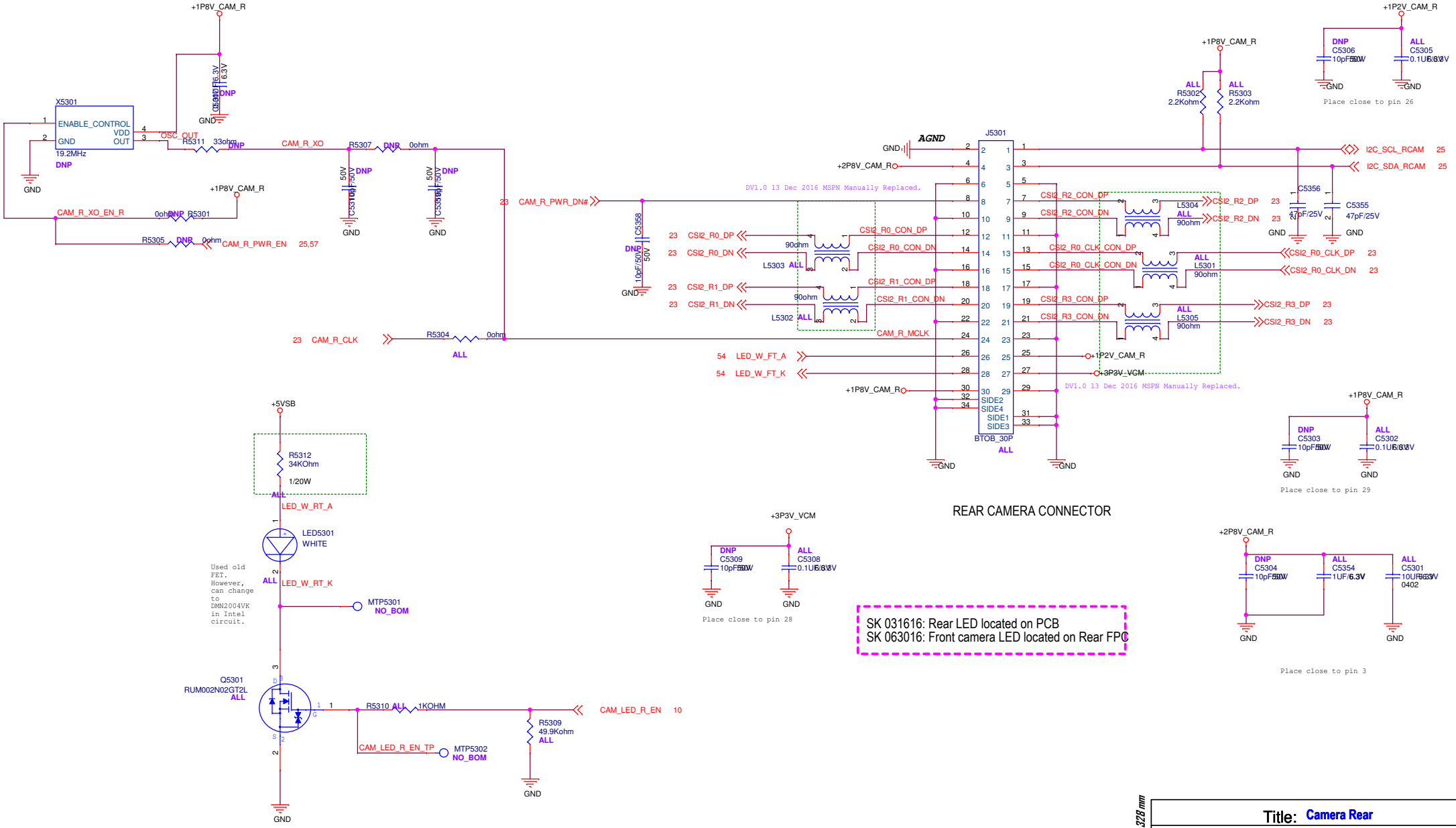
W = H 6972 x 7897 mm

Title:	eDP connector		
<OrgName>		Engineer:	<OrgAddr1>
Size: A3	Project Name: B52		Rev: 1.00
Date: Friday, June 09, 2023		Sheet: 51 of 82	

W: H: 432 x 368 mm

Title: PECI			
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 52 of 82		

This Page reference Marada

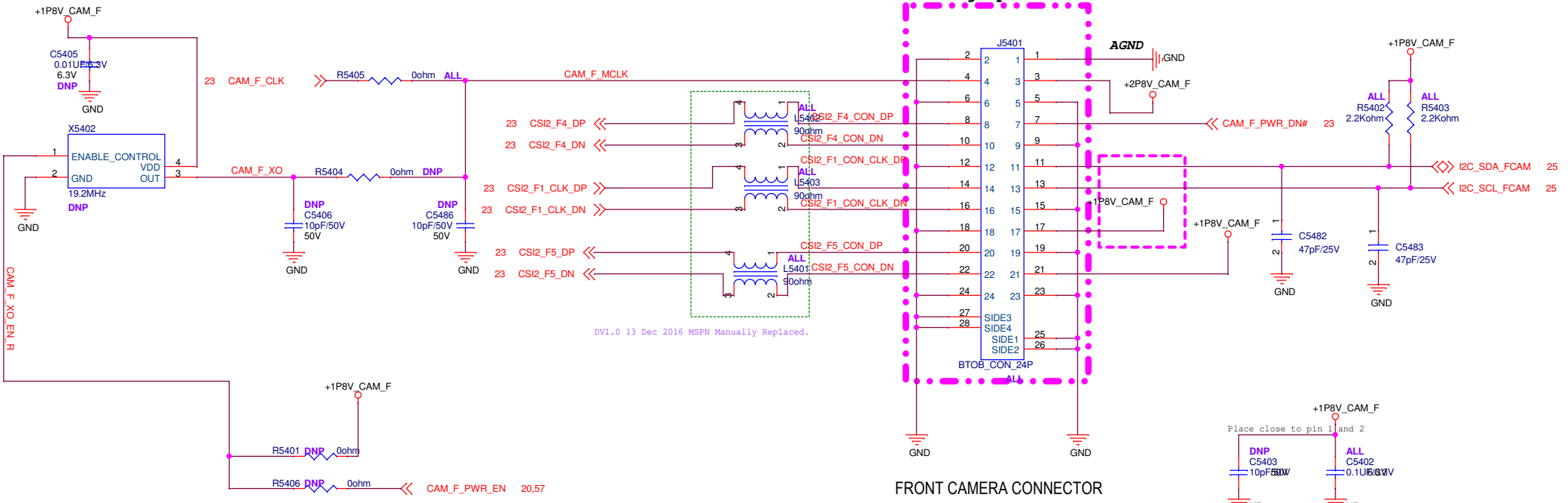


Title: Camera Rear			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 53 of 82		

W x H 437 x 328 mm

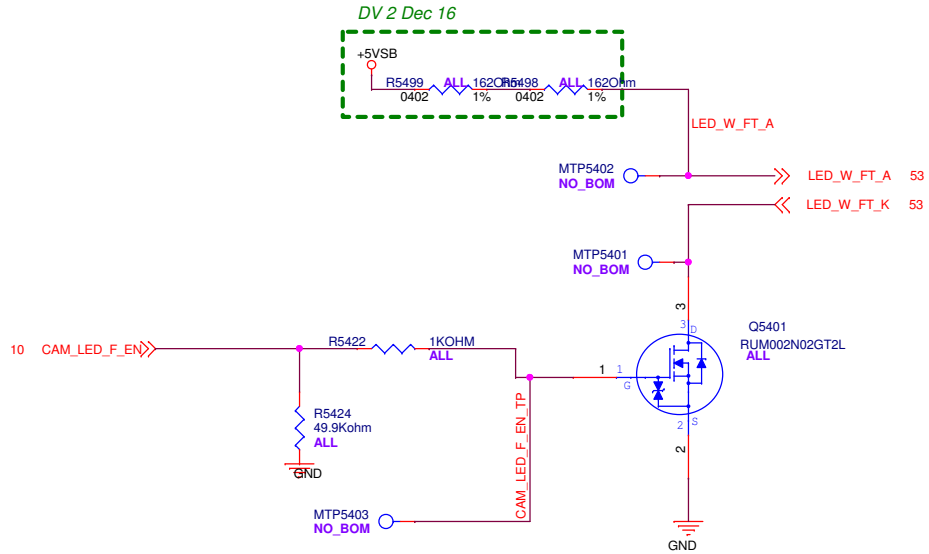
This Page reference Marada

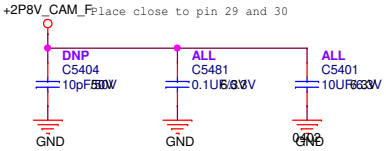
0118 change pin define



FRONT CAMERA CONNECTOR

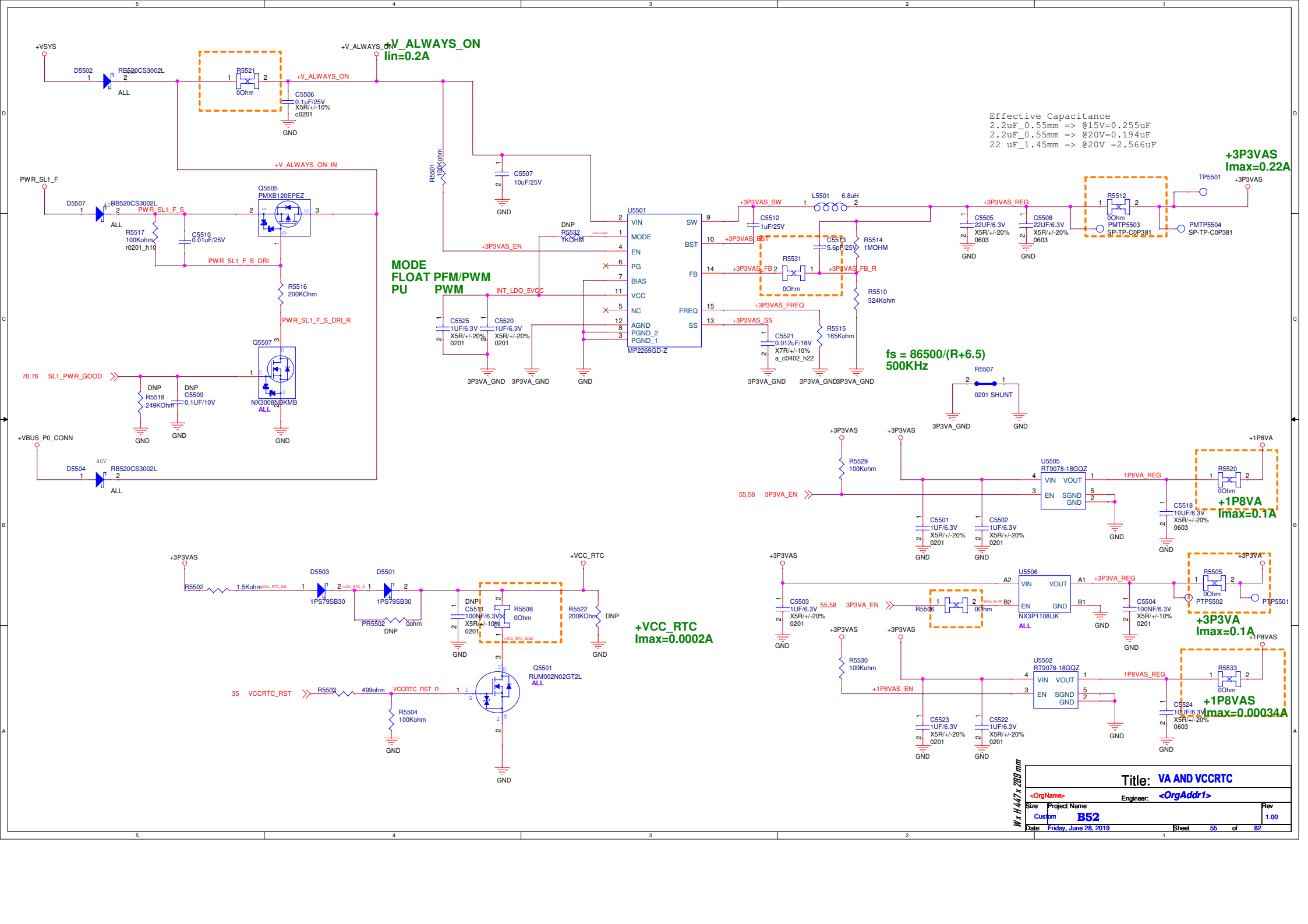
DV 2 Dec 16

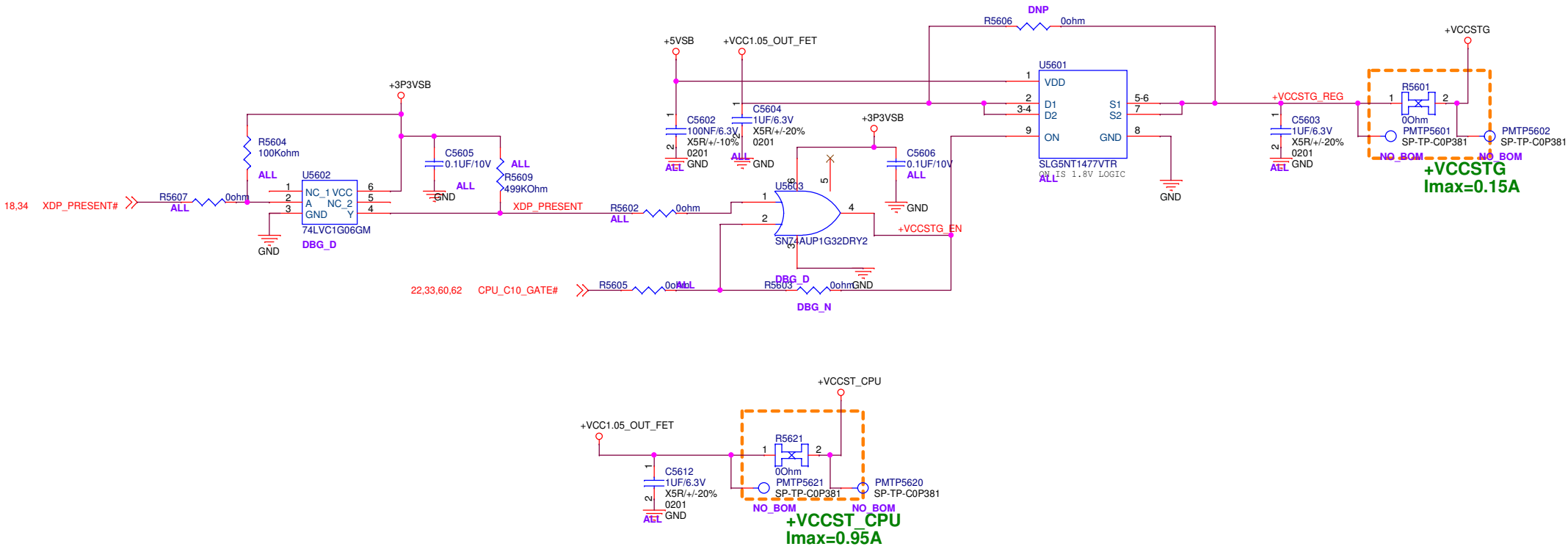




Title: Camera Front		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 54 of 82	

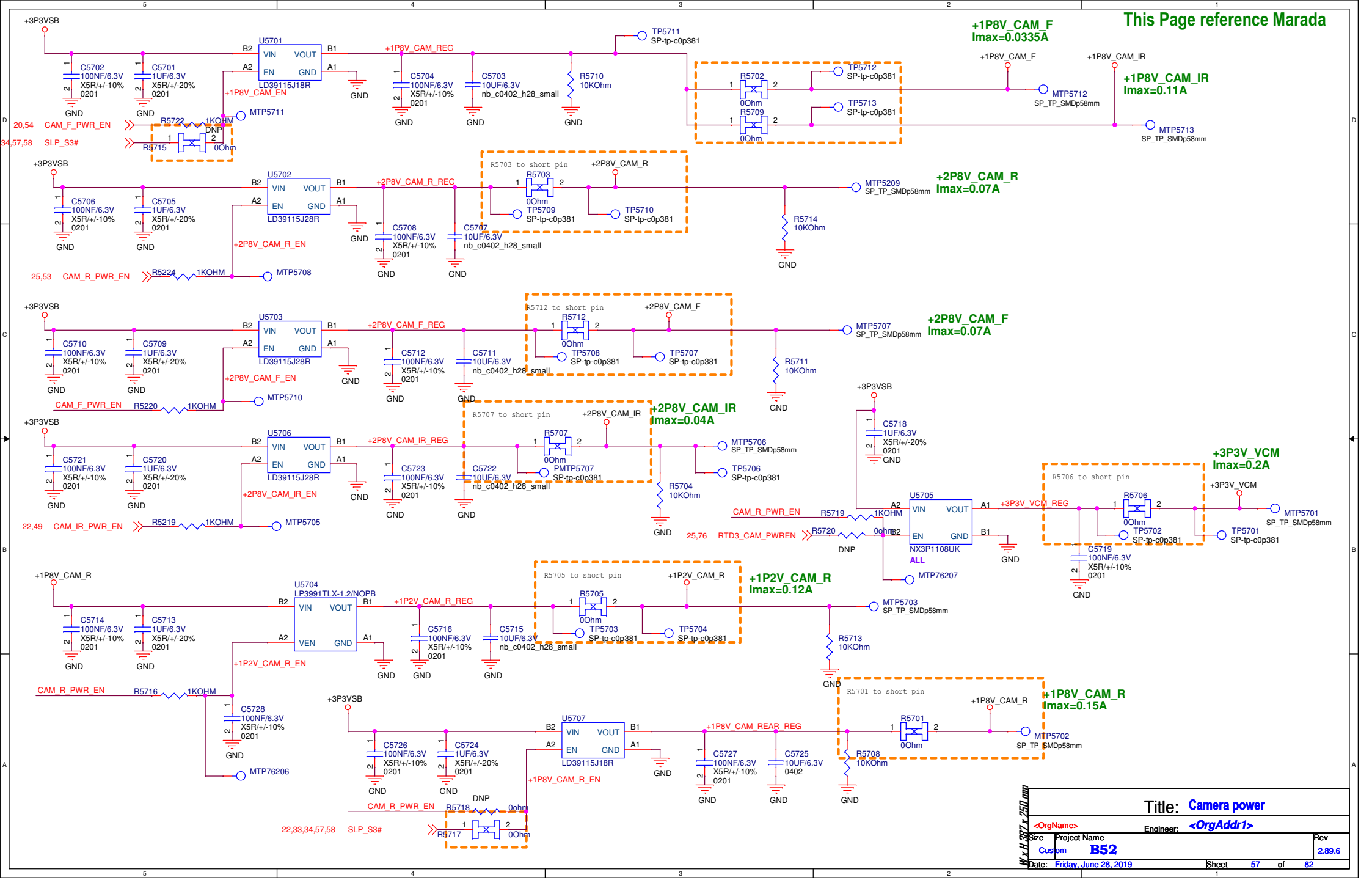
11 x 17 792 x 254 mm


+V_ALWAYS_ON
Iin=0.2A
Effective Capacitance
2.2uF_0.55mm => @15V=0.255uF
2.2uF_0.55mm => @20V=0.194uF
22 uF_1.45mm => @20V =2.566uF
+3P3VAS
Imax=0.22A
MODE
FLOAT PFM/PWM
PU PWM
fs = 86500/(R+6.5)
500KHz
+1P8VA
Imax=0.1A
+3P3VA
Imax=0.1A
+1P8VAS
Imax=0.00034A
+VCC_RTC
Imax=0.0002A
Title: VA AND VCCRTC
<OrgName>
Engineer: <OrgAddr1>
Project Name B52
Size Custom
Rev 1.00
Date: Friday, June 28, 2019
Sheet 55 of 82
W x H 447 x 289 mm

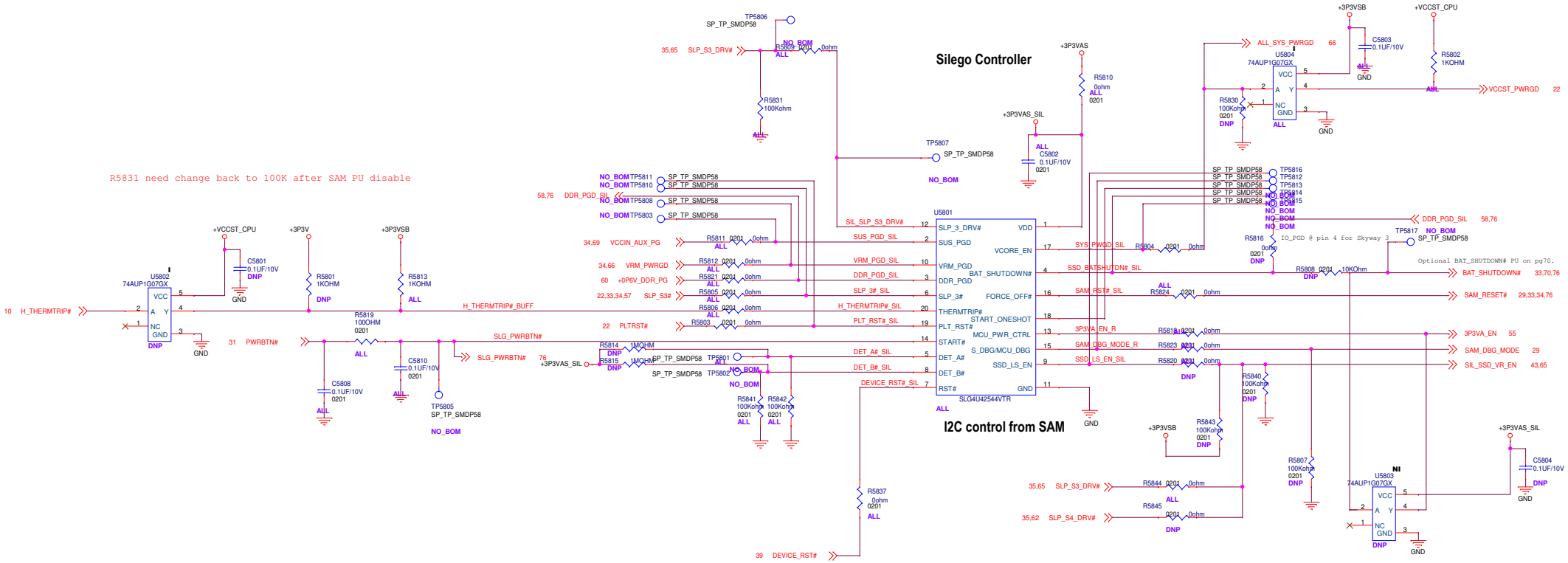


Title: +VCCSTG			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 56 of 82		

W x H 377 x 244 mm


This Page reference Marada
+1P8V_CAM_F
Imax=0.0335A
+1P8V_CAM_IR
Imax=0.11A
+2P8V_CAM_R
Imax=0.07A
+2P8V_CAM_F
Imax=0.07A
+2P8V_CAM_IR
Imax=0.04A
+3P3V_VCM
Imax=0.2A
+1P2V_CAM_R
Imax=0.12A
+1P8V_CAM_R
Imax=0.15A
+3P3VSB
U5701
LD39115J18R
U5702
LD39115J28R
U5703
LD39115J28R
U5706
LD39115J28R
U5704
LP3991TLX-1.2/NOPB
U5707
LD39115J18R
U5705
NX3P1108UK
ALL
+1P8V_CAM_REG
+2P8V_CAM_R_REG
+2P8V_CAM_F_REG
+2P8V_CAM_IR_REG
+1P2V_CAM_R_REG
+1P8V_CAM_REAR_REG
+3P3V_VCM_REG
+1P8V_CAM_EN
+2P8V_CAM_R_EN
+2P8V_CAM_F_EN
+2P8V_CAM_IR_EN
+1P2V_CAM_R_EN
+1P8V_CAM_R_EN
CAM_F_PWR_EN
CAM_R_PWR_EN
CAM_IR_PWR_EN
SLP_S3#
RTD3_CAM_PWREN
R5703 to short pin
R5712 to short pin
R5707 to short pin
R5705 to short pin
R5706 to short pin
R5701 to short pin
MTP5711
MTP5712
MTP5713
MTP5708
MTP5710
MTP5705
MTP5707
MTP5706
MTP5709
MTP5703
MTP5701
MTP5702
MTP76207
PMTP5707
TP5711
TP5712
TP5713
TP5709
TP5710
TP5708
TP5707
TP5706
TP5703
TP5704
TP5702
TP5701
SP-tp-c0p381
SP_TP_SMDp58mm
nb_c0402_h28_small
DNP
Title: Camera power
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: B52
Rev: 2.89.6
Date: Friday, June 28, 2019
Sheet 57 of 82

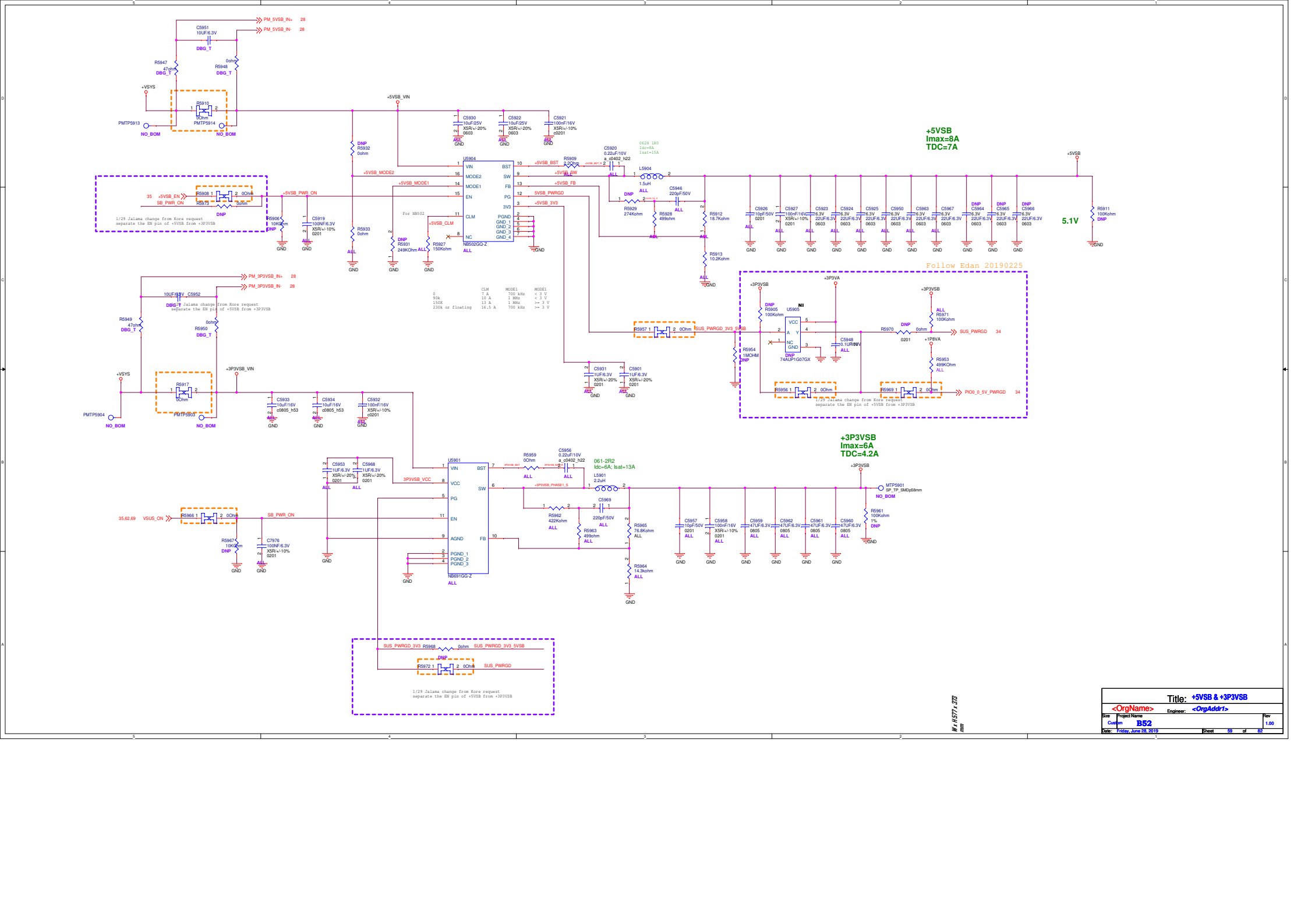
PIN17=PIN2*PIN12*PIN3*PIN6

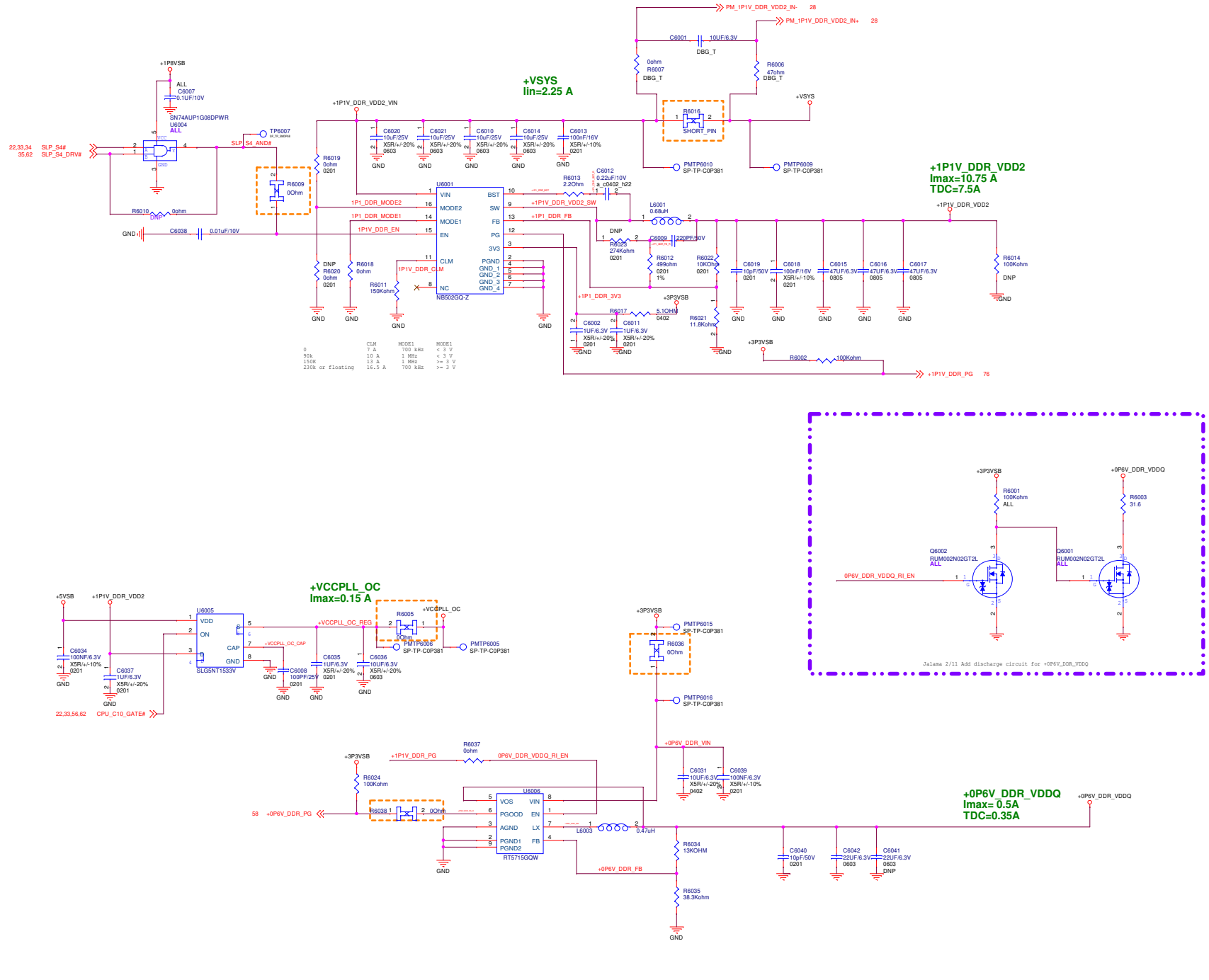


20160727sjs0530
title is: Silego Controller

Size: Custom	Project Name: B52	Rev: 1.00	
Date: Friday, June 28, 2019	Sheet 58 of 82		

Title: Silego Controller
<OrgName>
Engineer: <OrgAddr1>


+5VSB
Imax=8A
TDC=7A
5.1V
+3P3VSB
Imax=6A
TDC=4.2A
Follow Edan 20190225
Title: +5VSB & +3P3VSB
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: B52
Rev: 1.00
Date: Friday, June 28, 2019
Sheet 59 of 82
1/29 Jalama change from Kore request
separate the EN pin of +5VSB from +3P3VSB



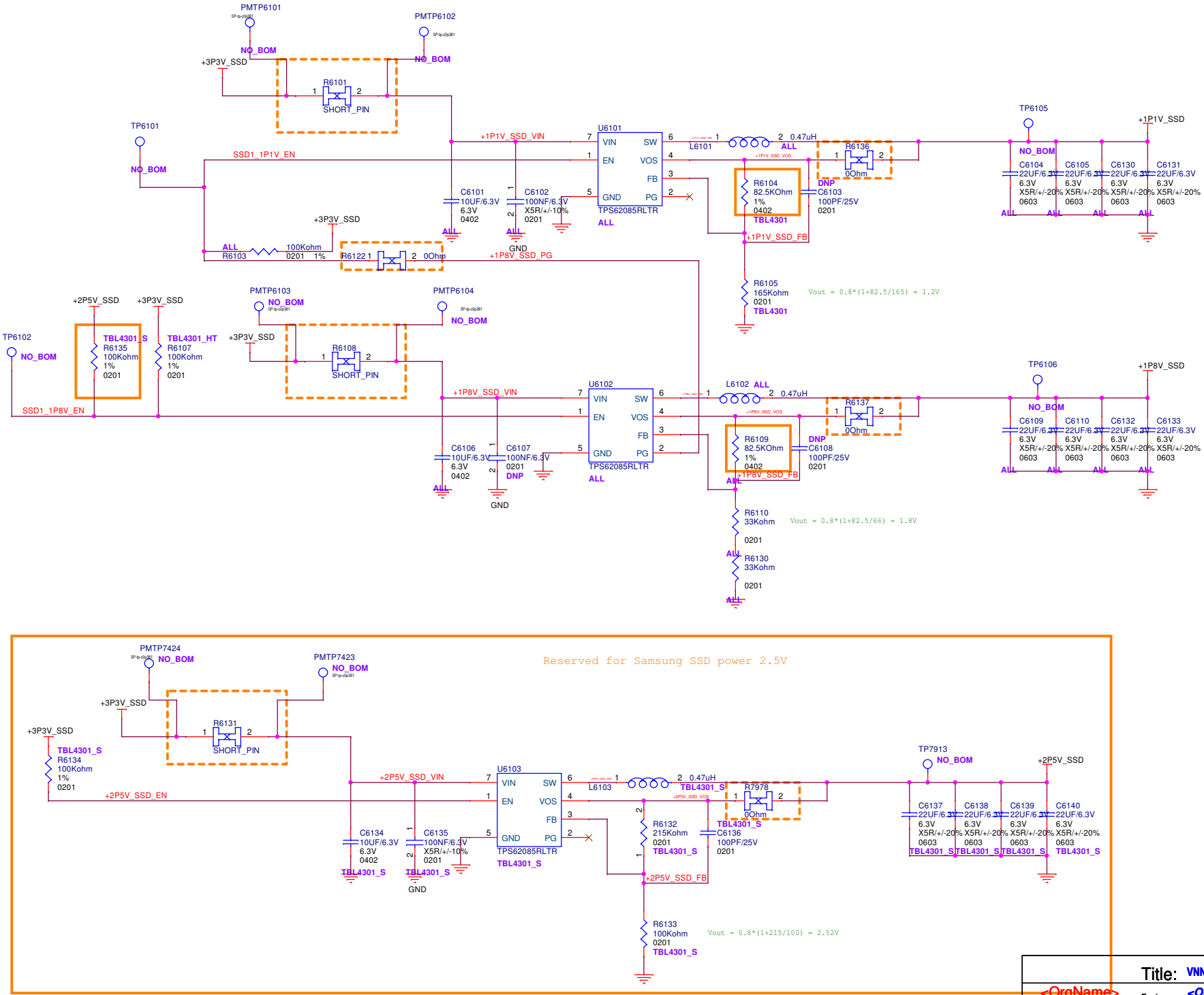
CLM	MODE1	MODE1
0	7 A	700 kHz	< 3 V
90k	10 A	1 MHz	< 3 V
150K	13 A	1 MHz	>= 3 V
230k or floating	16.5 A	700 kHz	>= 3 V

Title: +1P2V_DUAL&+VTT

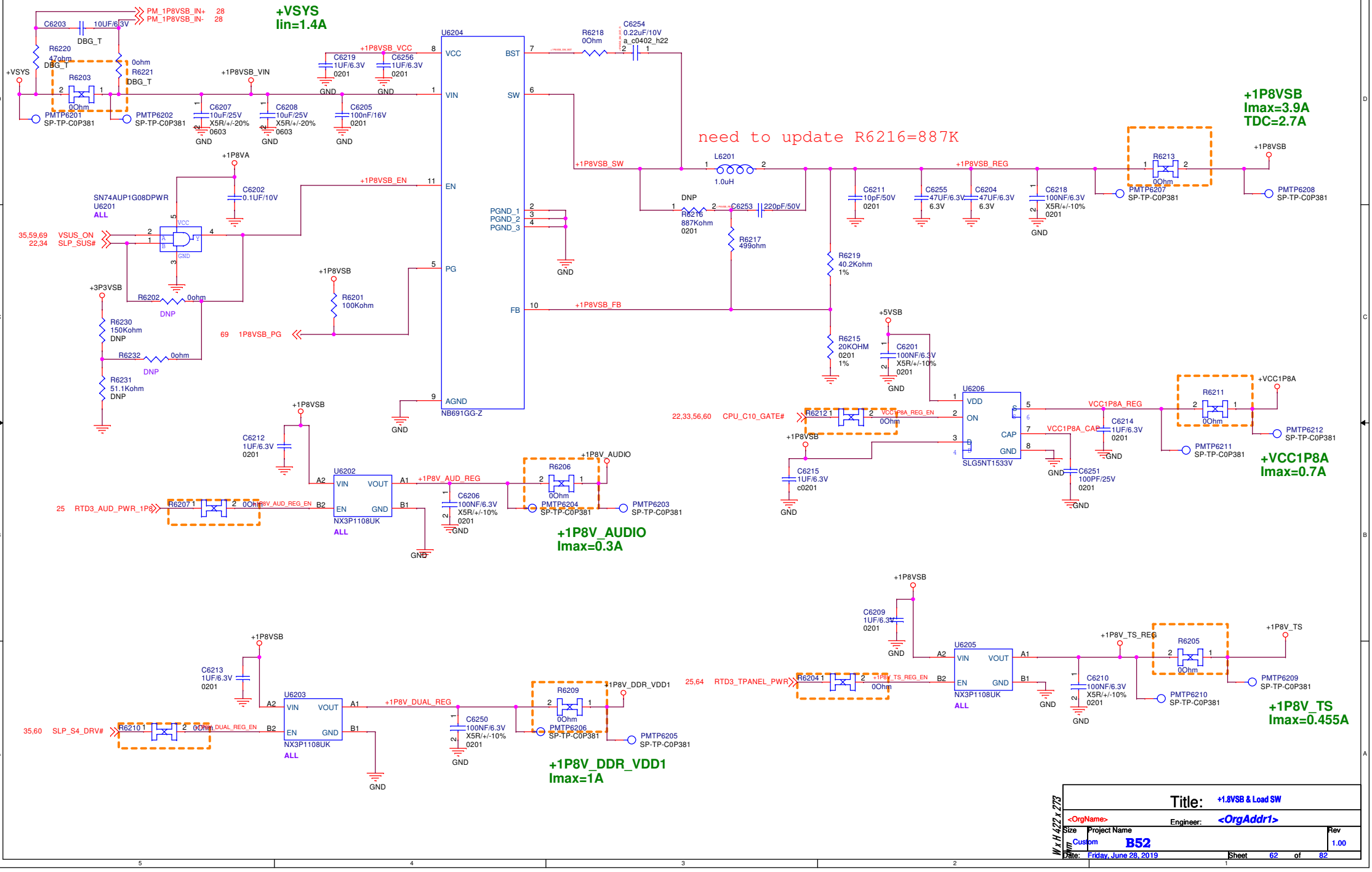
<OrgName> Engineer: <OrgAddr1>

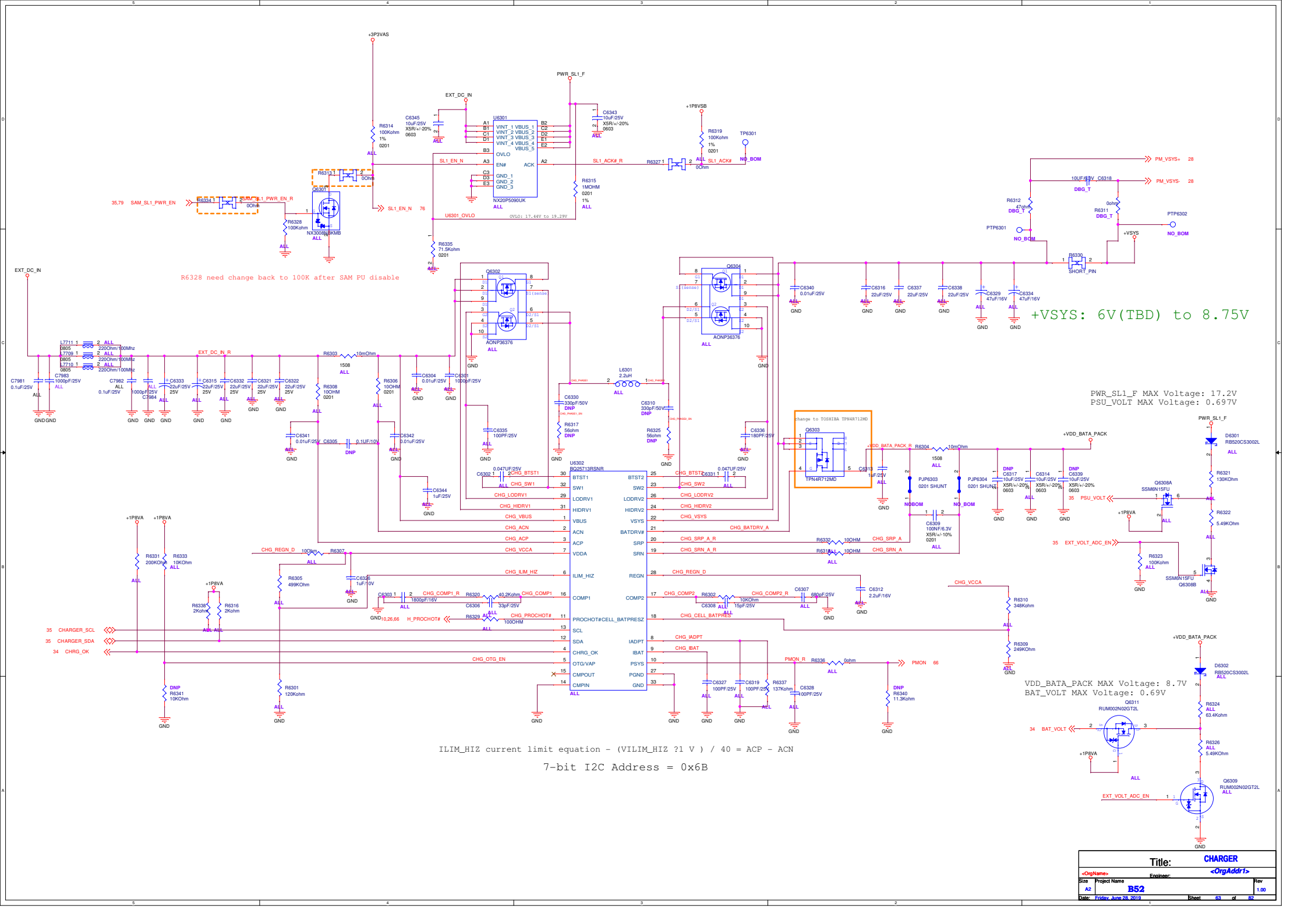
Size	Project Name	Rev
A2	B52	1.00

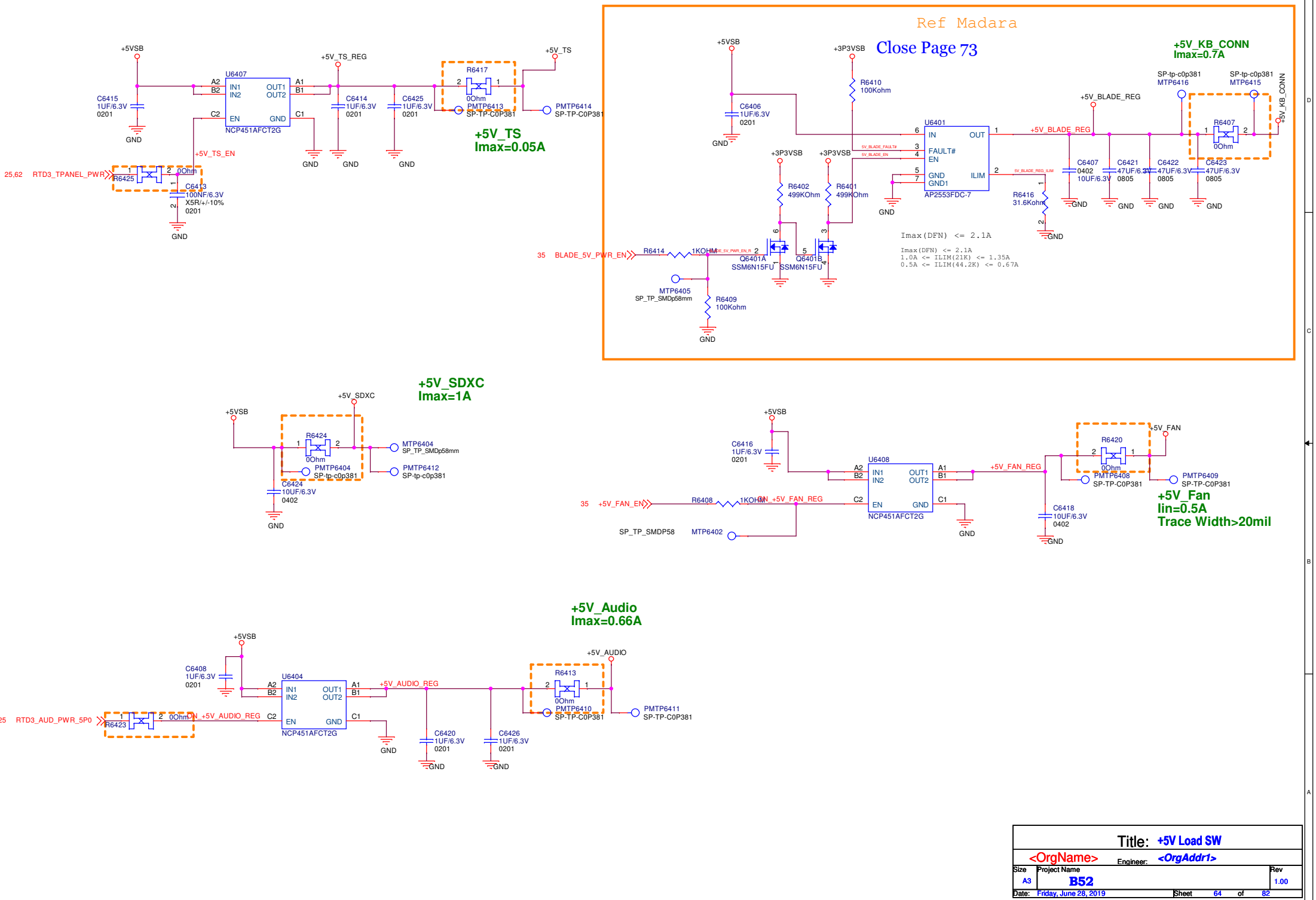
Date: Friday, June 28, 2019 Sheet 60 of 82

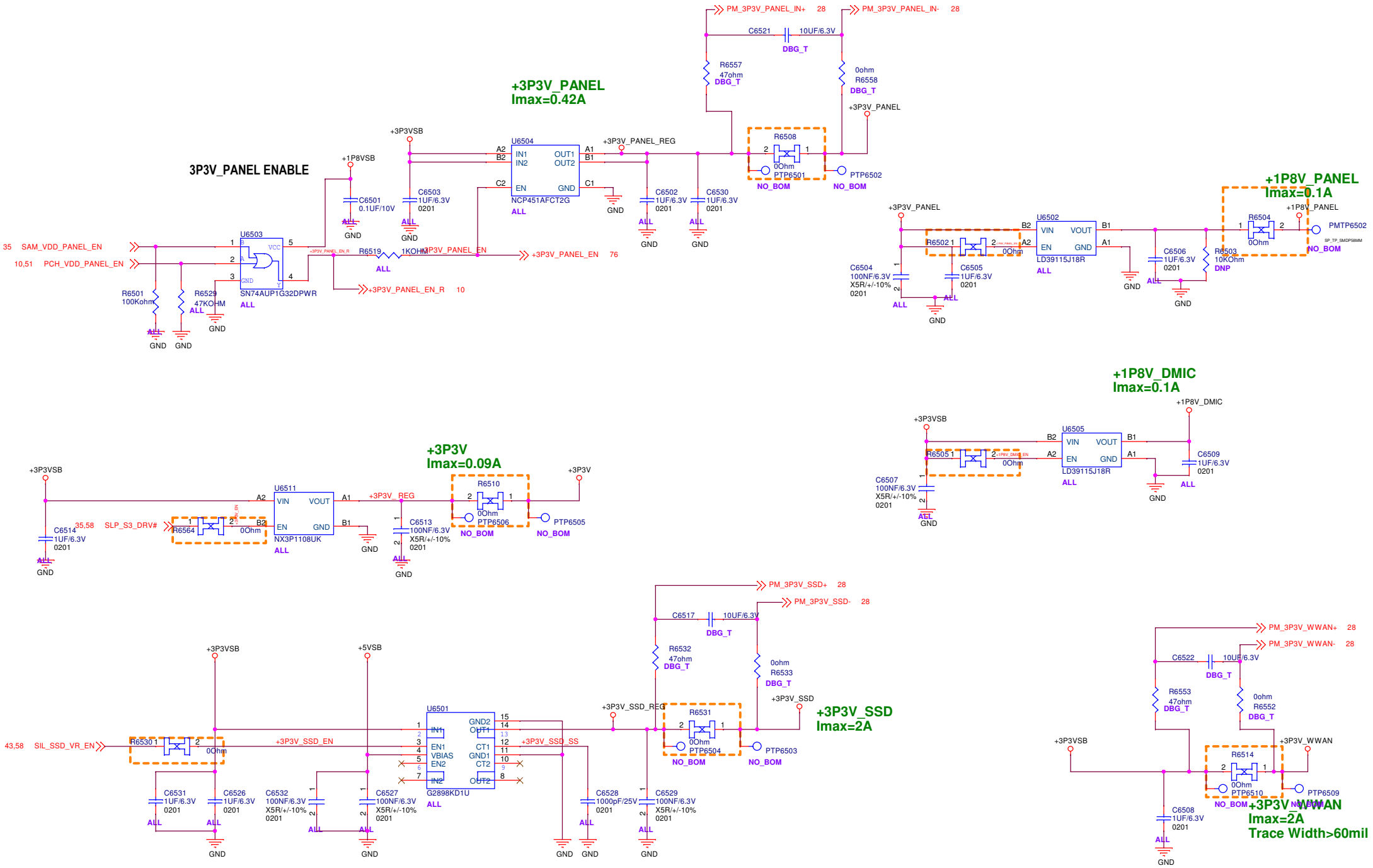


Title:	VNN BYPASS Rails	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 61 of 82	

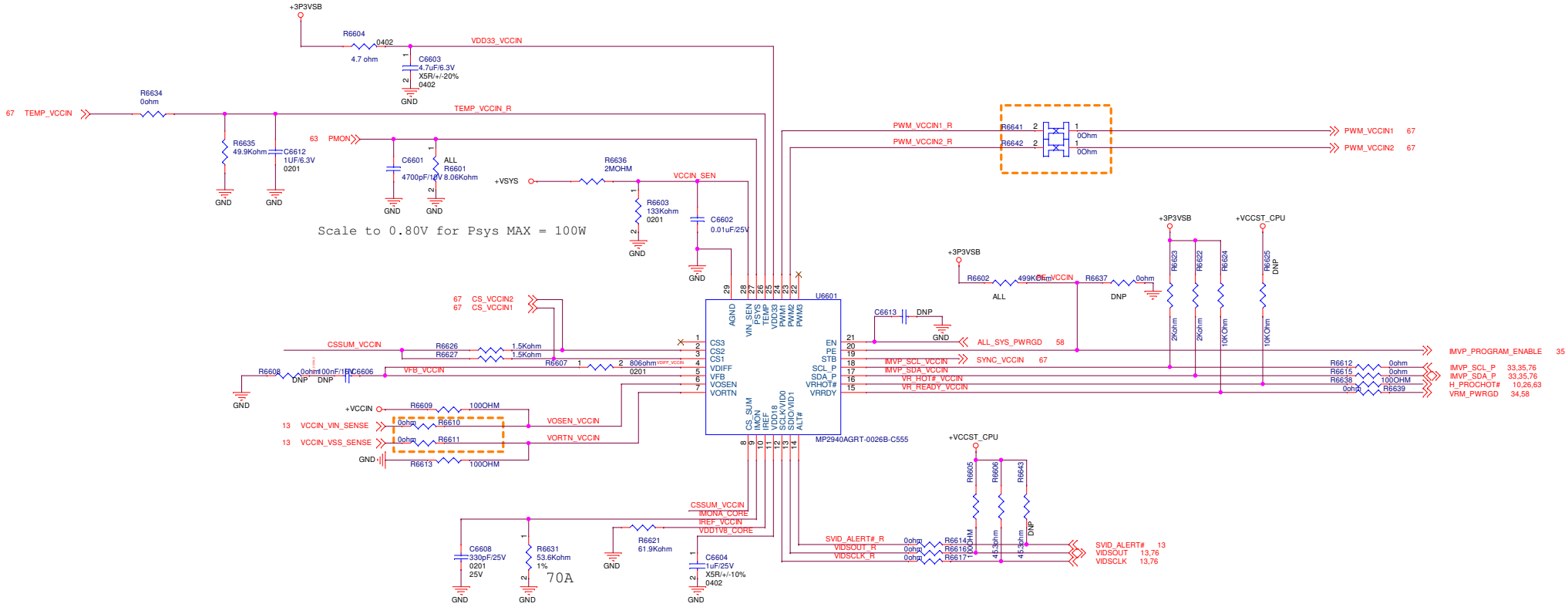

+VSYS
Iin=1.4A
PM_1P8VSB_IN+ 28
PM_1P8VSB_IN- 28
C6203 10UF/6.3V
DBG_T
R6220 47ohm DBG_T
R6203 0Ohm
R6221 0ohm DBG_T
PMTP6201 SP-TP-C0P381
PMTP6202 SP-TP-C0P381
+1P8VSB_VIN
C6207 10uF/25V X5R/+/-20% 0603
C6208 10uF/25V X5R/+/-20% 0603
C6205 100nF/16V 0201
U6204
VCC
VIN
EN
PG
FB
AGND
BST
SW
PGND_1
PGND_2
PGND_3
NB691GG-Z
+1P8VSB_VCC
C6219 1UF/6.3V 0201
C6256 1UF/6.3V 0201
R6218 0Ohm
C6254 0.22uF/10V a_c0402_h22
+1P8VSB_SW
L6201 1.0uH
+1P8VSB_REG
need to update R6216=887K
DNP
R6216 887Kohm 0201
C6253 220pF/50V
R6217 499ohm
R6219 40.2Kohm 1%
R6215 20KOHM 0201 1%
C6201 100NF/6.3V X5R/+/-10% 0201
C6211 10pF/50V 0201
C6255 47UF/6.3V 6.3V
C6204 47UF/6.3V 6.3V
C6218 100NF/6.3V X5R/+/-10% 0201
R6213 0Ohm
PMTP6207 SP-TP-C0P381
PMTP6208 SP-TP-C0P381
+1P8VSB
Imax=3.9A
TDC=2.7A
+1P8VA
C6202 0.1UF/10V
SN74AUP1G08DPWR
U6201
ALL
35,59,69 VSUS_ON
22,34 SLP_SUS#
+1P8VSB_EN
+3P3VSB
R6202 0ohm DNP
R6230 150Kohm DNP
R6232 0ohm DNP
R6231 51.1Kohm DNP
+1P8VSB
R6201 100Kohm
69 1P8VSB_PG
+5VSB
C6201 100NF/6.3V X5R/+/-10% 0201
22,33,56,60 CPU_C10_GATE#
R6212 0Ohm
VCC1P8A_REG_EN
U6206
VDD
ON
CAP
GND
SLG5NT1533V
VCC1P8A_REG
VCC1P8A_CAP
C6214 1UF/6.3V 0201
C6251 100PF/25V 0201
R6211 0Ohm
+VCC1P8A
PMTP6211 SP-TP-C0P381
PMTP6212 SP-TP-C0P381
+VCC1P8A
Imax=0.7A
C6212 1UF/6.3V 0201
U6202
VIN
VOUT
EN
GND
NX3P1108UK
ALL
+1P8V_AUD_REG
R6206 0Ohm
+1P8V_AUDIO
PMTP6204 SP-TP-C0P381
PMTP6203 SP-TP-C0P381
25 RTD3_AUD_PWR_1P8
R6207 0Ohm
+1P8V_AUDIO
Imax=0.3A
C6209 1UF/6.3V 0201
U6205
+1P8V_TS_REG
R6205 0Ohm
+1P8V_TS
PMTP6209 SP-TP-C0P381
PMTP6210 SP-TP-C0P381
25,64 RTD3_TPANEL_PWR
R6204 0Ohm
C6210 100NF/6.3V X5R/+/-10% 0201
+1P8V_TS
Imax=0.455A
C6213 1UF/6.3V 0201
U6203
+1P8V_DUAL_REG
R6209 0Ohm
+1P8V_DDR_VDD1
PMTP6206 SP-TP-C0P381
PMTP6205 SP-TP-C0P381
35,60 SLP_S4_DRV#
R6210 0Ohm
C6250 100NF/6.3V X5R/+/-10% 0201
+1P8V_DDR_VDD1
Imax=1A
Title: +1.8VSB & Load SW
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: B52
Rev: 1.00
Date: Friday, June 28, 2019
Sheet 62 of 82
W x H 422 x 273 mm


R6328 need change back to 100K after SAM PU disable
+VSYS: 6V(TBD) to 8.75V
PWR_SL1_F MAX Voltage: 17.2V
PSU_VOLT MAX Voltage: 0.697V
VDD_BATA_PACK MAX Voltage: 8.7V
BAT_VOLT MAX Voltage: 0.69V
ILIM_HIZ current limit equation - (VILIM_HIZ ?1 V) / 40 = ACP - ACN
7-bit I2C Address = 0x6B
Title: CHARGER
<OrgName>
<OrgAddr1>
Engineer:
Size A2
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 63 of 82


Ref Madara
Close Page 73
+5V_TS
Imax=0.05A
+5V_KB_CONN
Imax=0.7A
+5V_SDXC
Imax=1A
+5V_Fan
Iin=0.5A
Trace Width>20mil
+5V_Audio
Imax=0.66A
U6407
NCP451AFCT2G
U6401
AP2553FDC-7
U6408
NCP451AFCT2G
U6404
NCP451AFCT2G
Q6401A SSM6N15FU
Q6401B SSM6N15FU
Imax(DFN) <= 2.1A
1.0A <= ILIM(21K) <= 1.35A
0.5A <= ILIM(44.2K) <= 0.67A
Title: +5V Load SW
<OrgName>
Engineer: <OrgAddr1>
Size A3
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 64 of 82



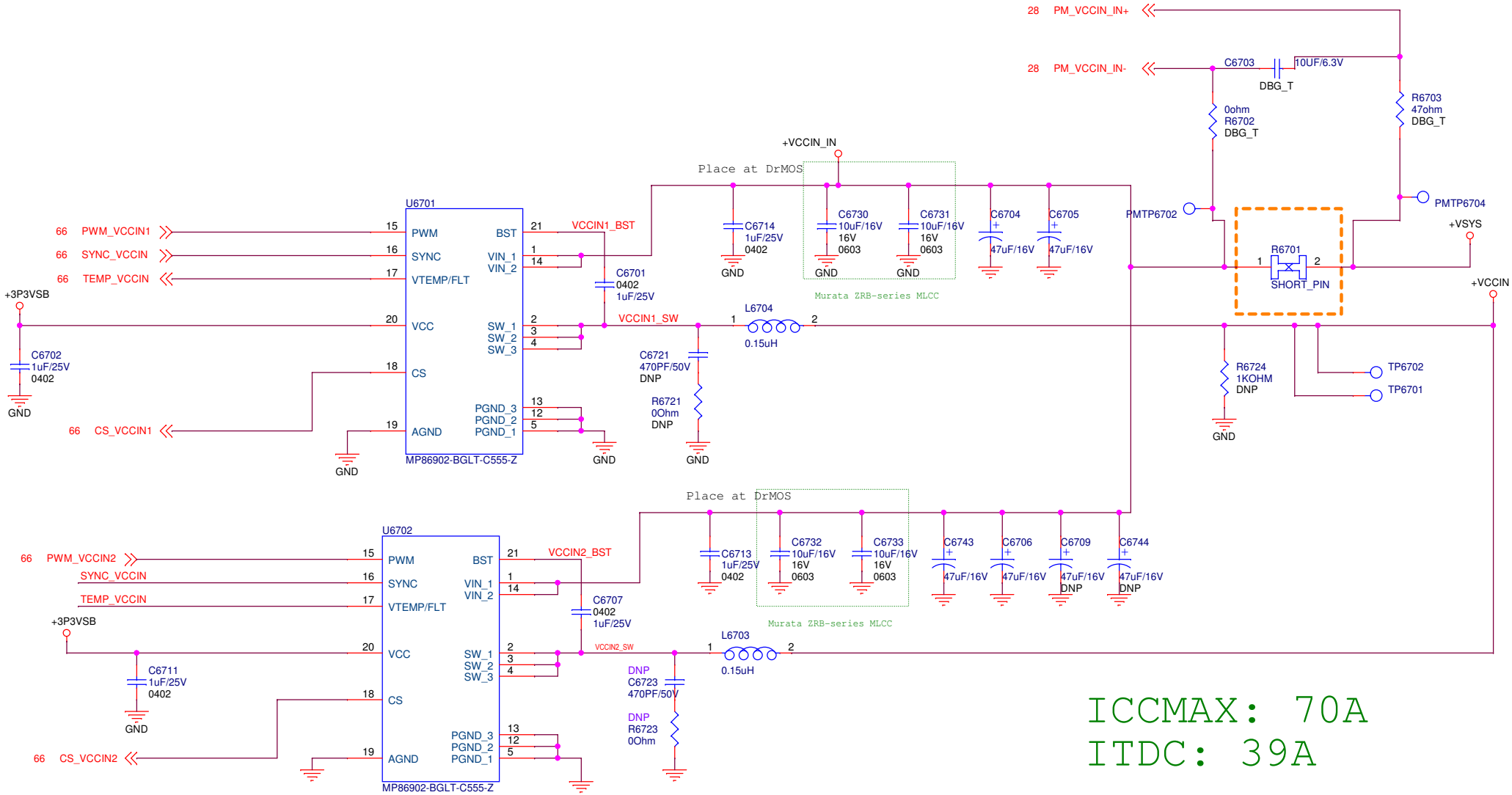
Title:	+3P3V Load SW	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 65 of 82	



Iccmax = [32*(1.6*8/11)]/(53.6kohm*10uA/A) = 69.5A

W x H 457 x 325 mm

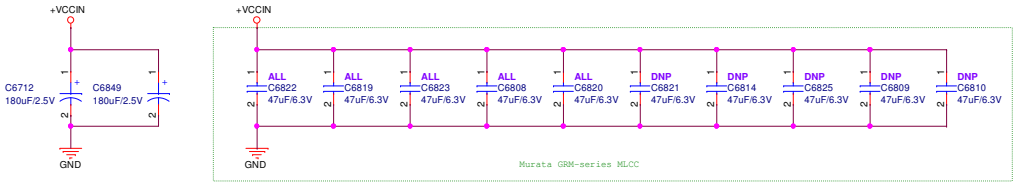
Title: CONTROLLER: CORE, SA		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 66 of 82	



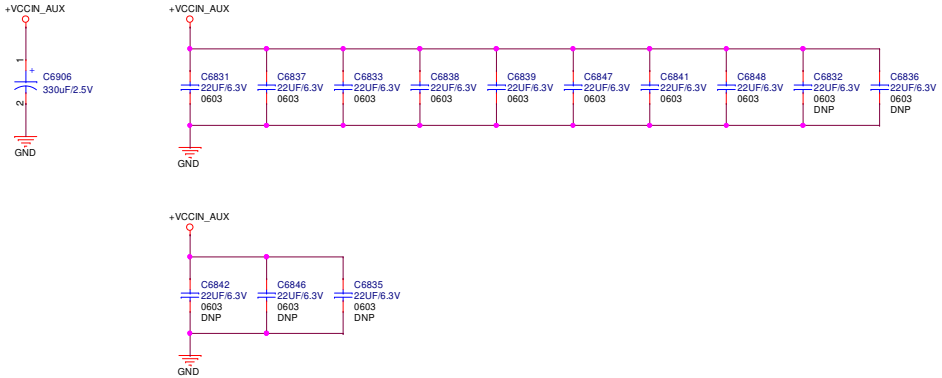
W x H577 x 335 mm

Title: +VCCIN		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 67 of 82	

+VCCIN Output Cap
47uF*5 + 5pcs DNP



+VCCIN Output Cap
22uF*8 + 5pcs DNP



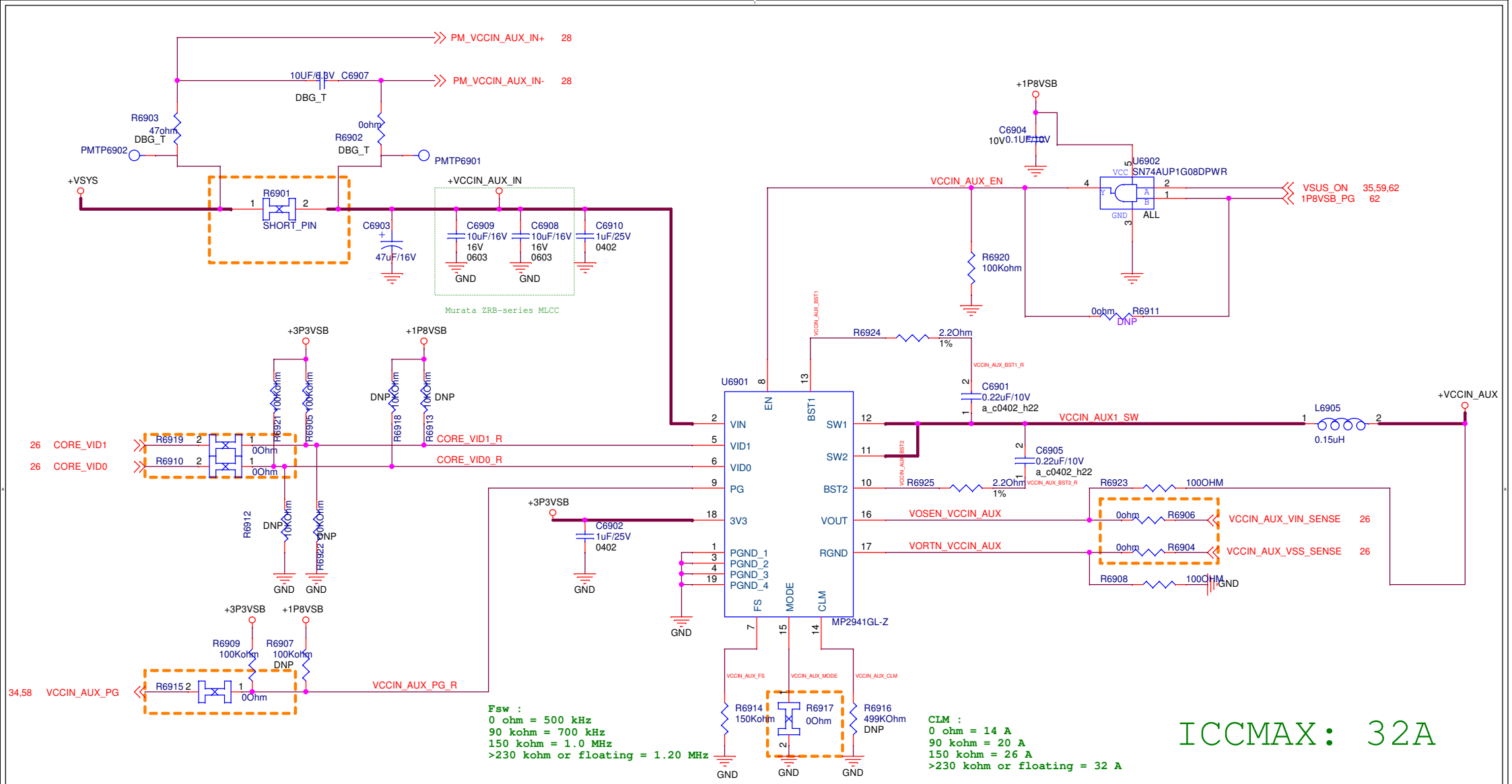
W x H 507 x 335 mm

Title: CPU PWR Capacitance

<OrgName> Engineer: <OrgAddr1>

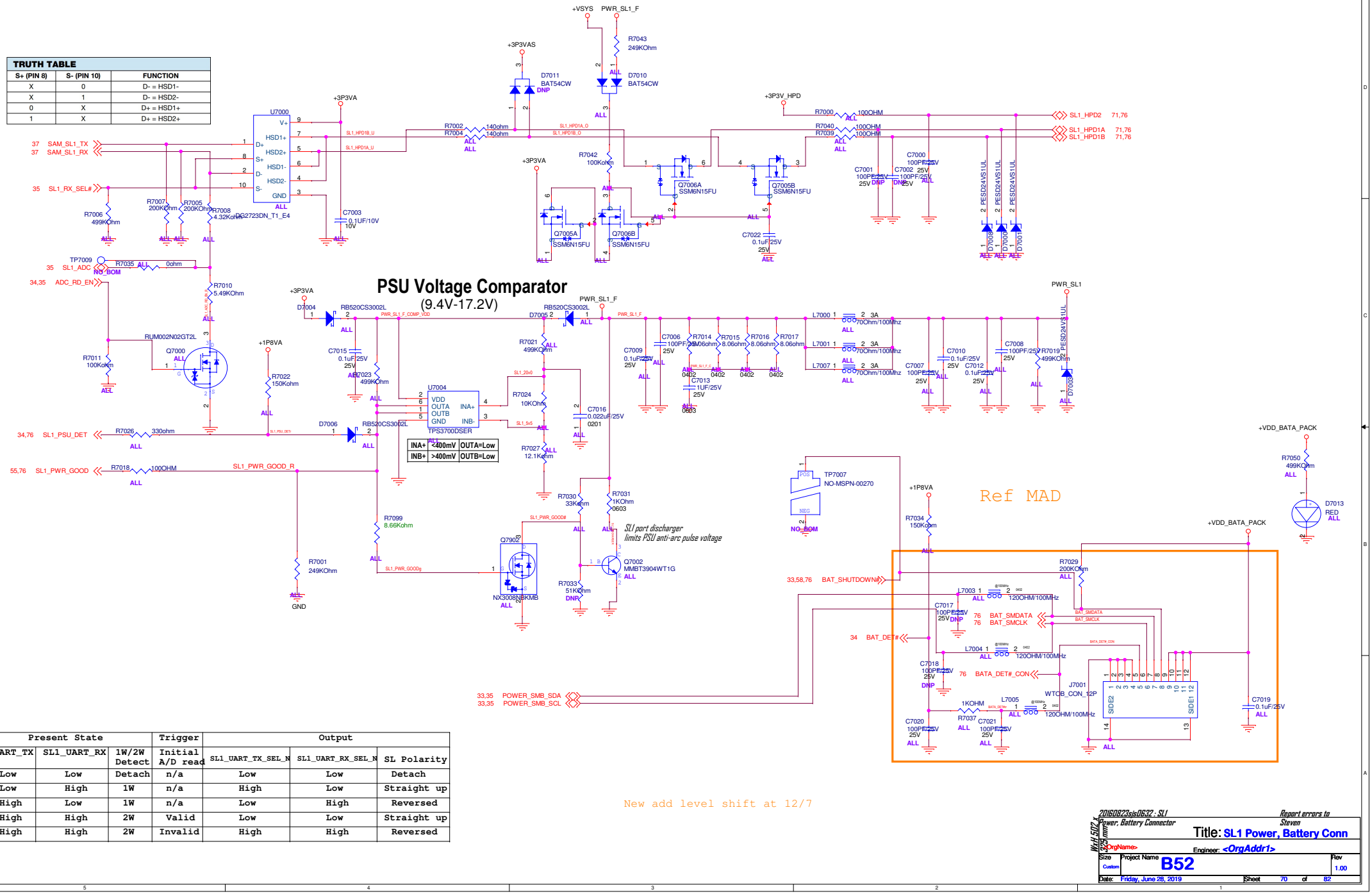
Size	Project Name	Rev
Custom	B52	1.00

Date: Friday, June 28, 2019 Sheet 68 of 82



Title: VCCIN_AUX_Controller			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 69 of 82		

W x H 357 x 241 mm


PSU Voltage Comparator
(9.4V-17.2V)
Ref MAD
New add level shift at 12/7
SL1 port discharger
limits PSU anti-arc pulse voltage
TRUTH TABLE
S+ (PIN 8) | S- (PIN 10) | FUNCTION
X | 0 | D- = HSD1-
X | 1 | D- = HSD2-
0 | X | D+ = HSD1+
1 | X | D+ = HSD2+
INA+ <400mV OUTA=Low
INB+ >400mV OUTB=Low
Present State | Trigger | Output
SL1_UART_TX | SL1_UART_RX | 1W/2W Detect | Initial A/D read | SL1_UART_TX_SEL_N | SL1_UART_RX_SEL_N | SL Polarity
Low | Low | Detach | n/a | Low | Low | Detach
Low | High | 1W | n/a | High | Low | Straight up
High | Low | 1W | n/a | Low | High | Reversed
High | High | 2W | Valid | Low | Low | Straight up
High | High | 2W | Invalid | High | High | Reversed
Title: SL1 Power, Battery Conn
Project Name B52
Rev 1.00
Sheet 70 of 82
Date: Friday, June 28, 2019

Common Mode Noise Filter CHOKE Follow E & H

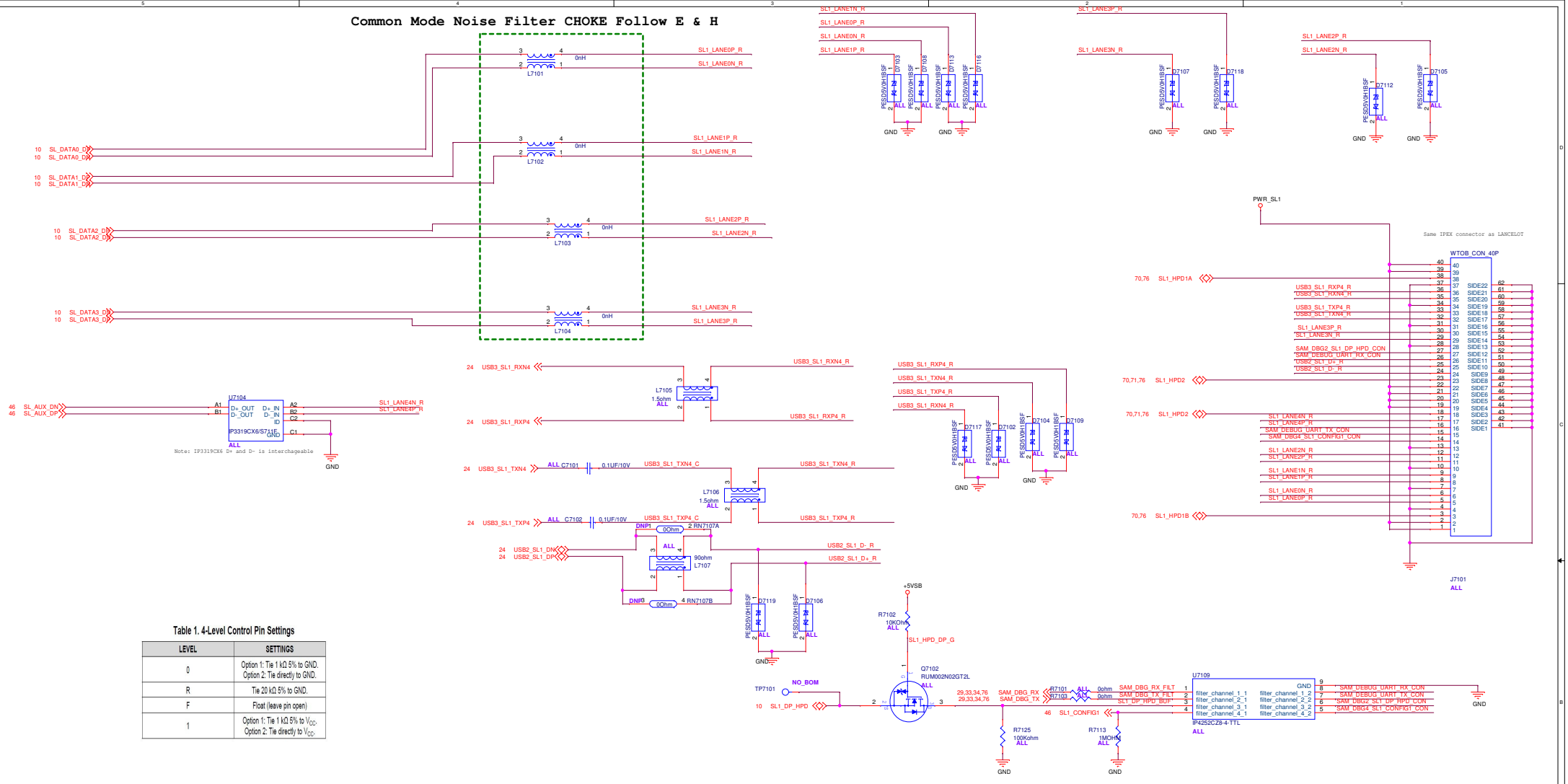
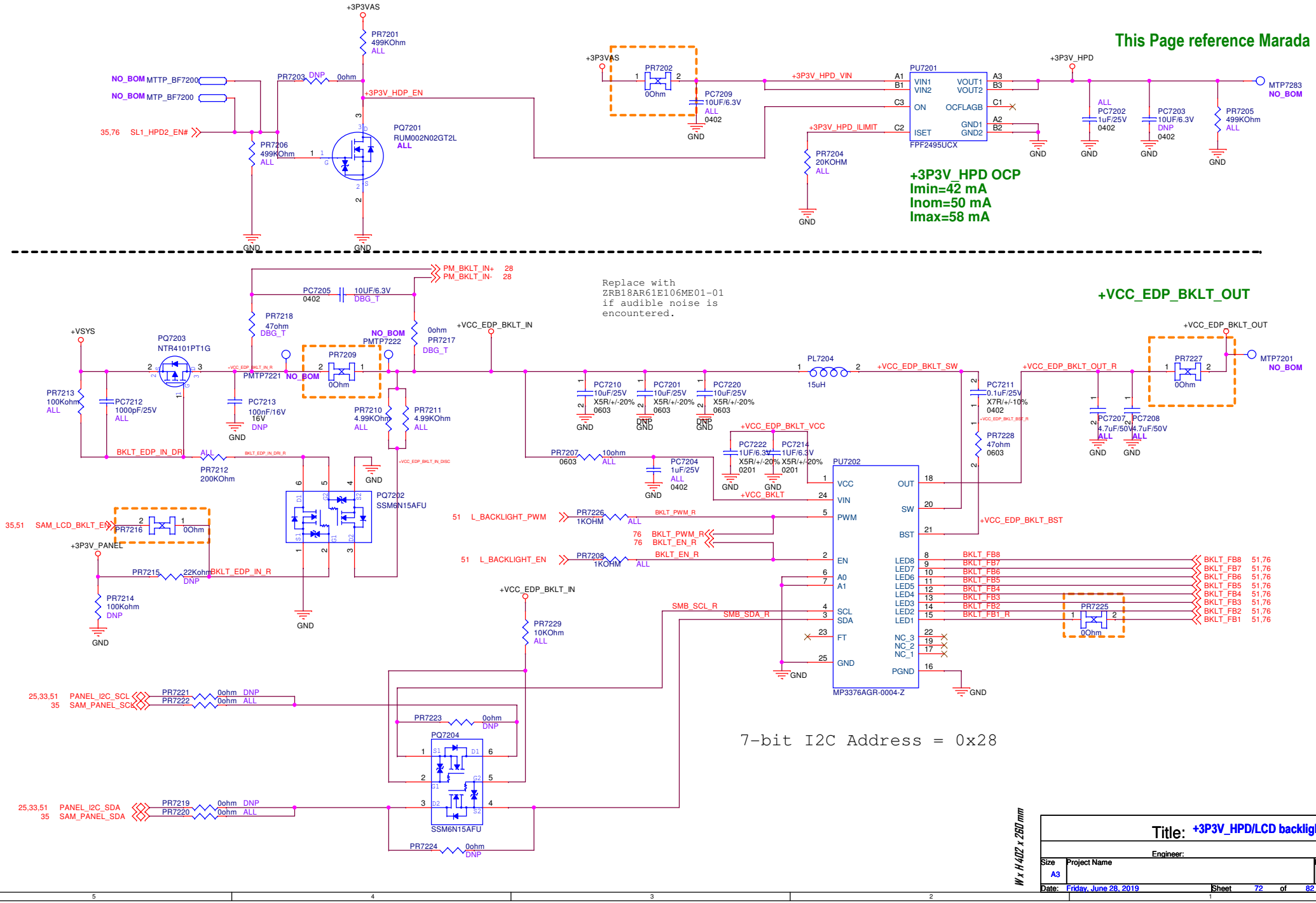


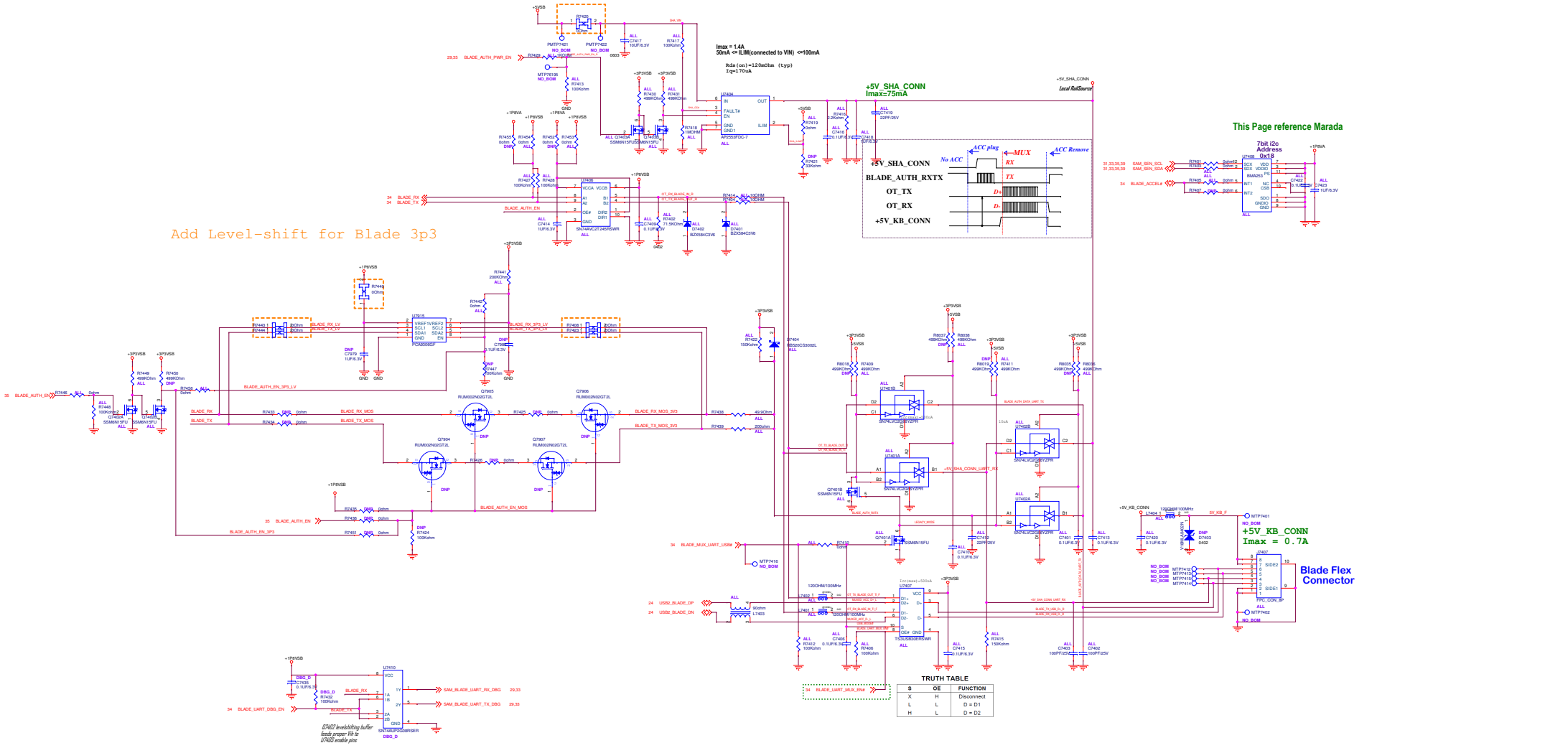
Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

Title:	SL1 SINGNALS		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: B52		Rev: 1.00
Date: Friday, June 28, 2019	Sheet 71 of 82		

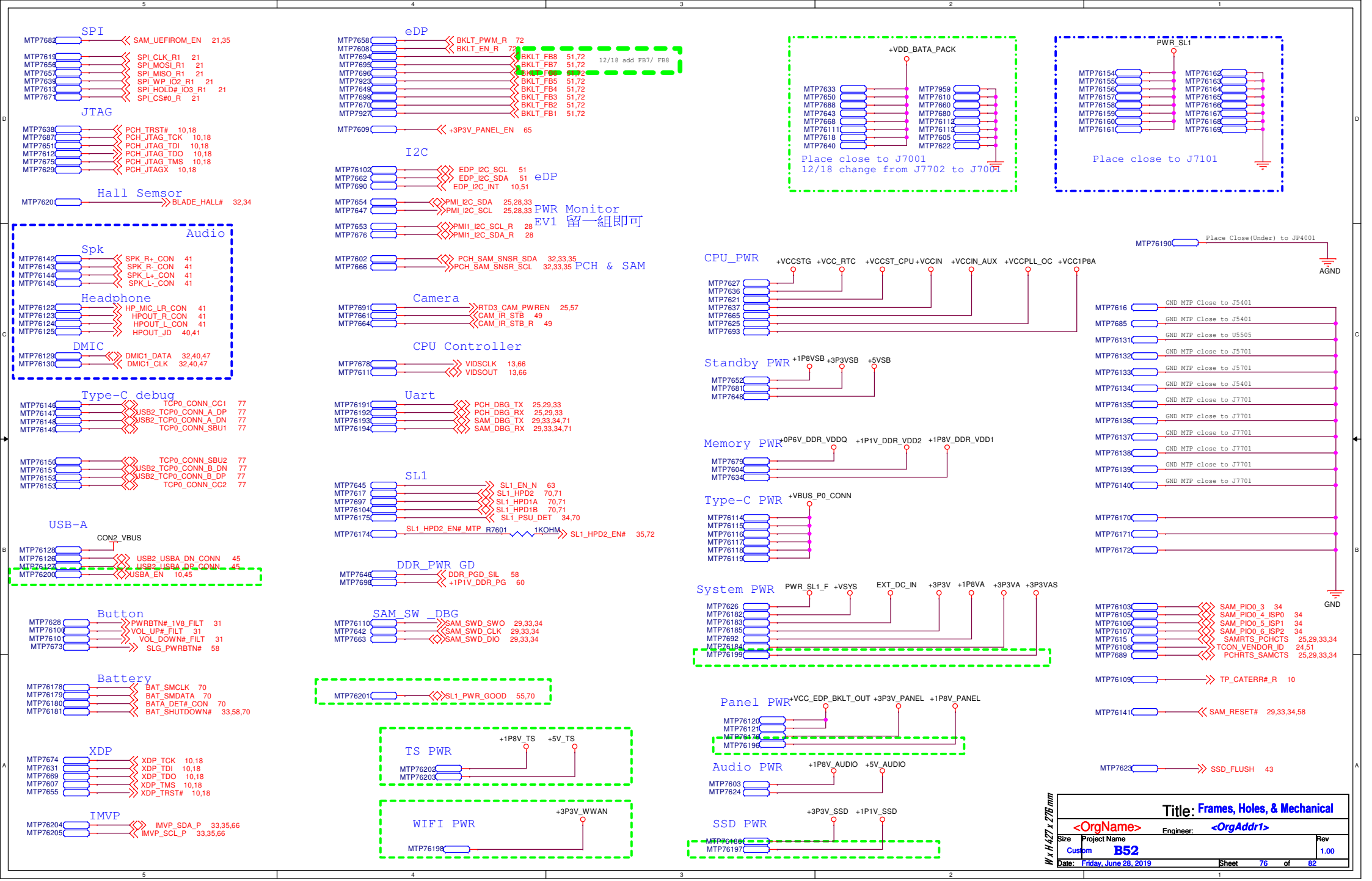

This Page reference Marada
+3P3V_HPD OCP
Imin=42 mA
Inom=50 mA
Imax=58 mA
+VCC_EDP_BKLT_OUT
Replace with
ZRB18AR61E106ME01-01
if audible noise is
encountered.
7-bit I2C Address = 0x28
Title: +3P3V_HPD/LCD backlight/TB
Engineer:
Size A3
Project Name
Rev 1.00
Date: Friday, June 28, 2019
Sheet 72 of 82
W x H402 x 280mm

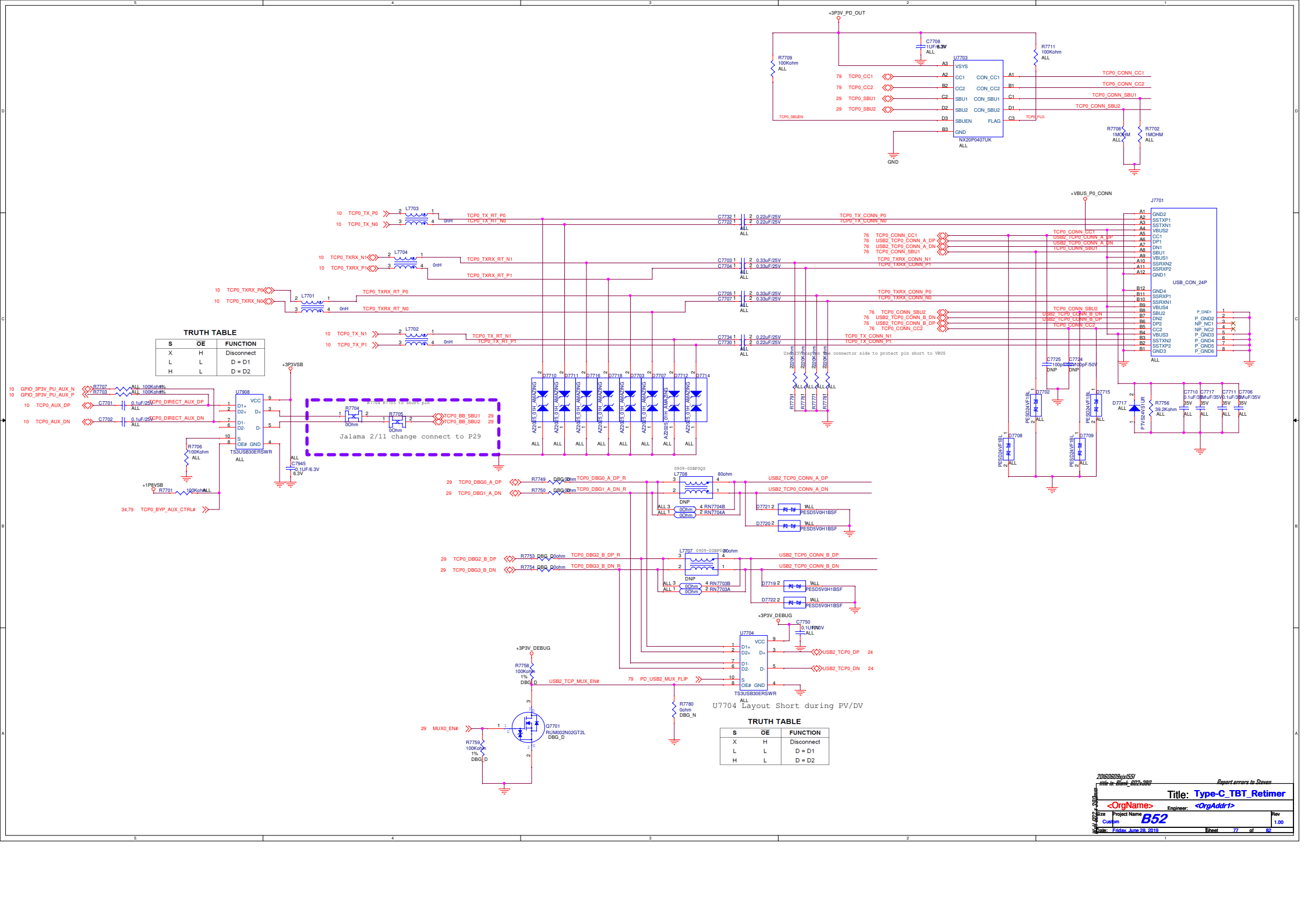
Title:	PCIe GPU	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 73 of 82	


Add Level-shift for Blade 3p3
Imax = 1.4A
50mA <= ILIM(connected to VIN) <=100mA
Rds(on)=120mOhm (typ)
Iq=170uA
+5V_SHA_CONN
Imax=75mA
+5V_SHA_CONN
Local 8x8Source
No ACC
ACC plug
MUX
ACC Remove
RX
TX
D+
D-
+5V_SHA_CONN
BLADE_AUTH_RXTX
OT_TX
OT_RX
+5V_KB_CONN
This Page reference Marada
7bit i2c Address 0x18
+5V_KB_CONN
Imax = 0.7A
Blade Flex Connector
TRUTH TABLE
S | OE | FUNCTION
X | H | Disconnect
L | L | D = D1
H | L | D = D2
U7407 level-shifting buffer feeds proper Vth to U7403 enable pins
Title: Blade Interface
<OrgName>
<OrgAddr1>
Project Name
B52
Friday, June 28, 2019

Title:	Power Protect
<OrgName>	Engineer: <OrgAddr1>
Size: Custom	Project Name: B52
Rev: 1.00	
Date: Friday, June 28, 2019	Sheet 75 of 82

W x H 357 x 231 mm


SPI
MTP7682 SAM_UEFIROM_EN 21,35
MTP7619 SPI_CLK_R1 21
MTP7656 SPI_MOSI_R1 21
MTP7657 SPI_MISO_R1 21
MTP7639 SPI_WP_IO2_R1 21
MTP7613 SPI_HOLD#_IO3_R1 21
MTP7671 SPI_CS#0_R 21
JTAG
MTP7638 PCH_TRST# 10,18
MTP7687 PCH_JTAG_TCK 10,18
MTP7651 PCH_JTAG_TDI 10,18
MTP7612 PCH_JTAG_TDO 10,18
MTP7675 PCH_JTAG_TMS 10,18
MTP7629 PCH_JTAGX 10,18
Hall Semsor
MTP7620 BLADE_HALL# 32,34
Audio
Spk
MTP76142 SPK_R+_CON 41
MTP76143 SPK_R-_CON 41
MTP76144 SPK_L+_CON 41
MTP76145 SPK_L-_CON 41
Headphone
MTP76122 HP_MIC_LR_CON 41
MTP76123 HPOUT_R_CON 41
MTP76124 HPOUT_L_CON 41
MTP76125 HPOUT_JD 40,41
DMIC
MTP76129 DMIC1_DATA 32,40,47
MTP76130 DMIC1_CLK 32,40,47
Type-C debug
MTP76146 TCP0_CONN_CC1 77
MTP76147 USB2_TCP0_CONN_A_DP 77
MTP76148 USB2_TCP0_CONN_A_DN 77
MTP76149 TCP0_CONN_SBU1 77
MTP76150 TCP0_CONN_SBU2 77
MTP76151 USB2_TCP0_CONN_B_DN 77
MTP76152 USB2_TCP0_CONN_B_DP 77
MTP76153 TCP0_CONN_CC2 77
USB-A
CON2_VBUS
MTP76128
MTP76126 USB2_USBA_DN_CONN 45
MTP76127 USB2_USBA_DP_CONN 45
MTP76200 USBA_EN 10,45
Button
MTP7628 PWRBTN#_1V8_FILT 31
MTP76100 VOL_UP#_FILT 31
MTP76101 VOL_DOWN#_FILT 31
MTP7673 SLG_PWRBTN# 58
Battery
MTP76178 BAT_SMCLK 70
MTP76179 BAT_SMDATA 70
MTP76180 BATA_DET#_CON 70
MTP76181 BAT_SHUTDOWN# 33,58,70
XDP
MTP7674 XDP_TCK 10,18
MTP7631 XDP_TDI 10,18
MTP7669 XDP_TDO 10,18
MTP7607 XDP_TMS 10,18
MTP7655 XDP_TRST# 10,18
IMVP
MTP76204 IMVP_SDA_P 33,35,66
MTP76205 IMVP_SCL_P 33,35,66
eDP
MTP7658 BKLT_PWM_R 72
MTP7608 BKLT_EN_R 72
MTP7694 BKLT_FB8 51,72
MTP7695 BKLT_FB7 51,72
MTP7696 BKLT_FB6 51,72
MTP7923 BKLT_FB5 51,72
MTP7649 BKLT_FB4 51,72
MTP7699 BKLT_FB3 51,72
MTP7670 BKLT_FB2 51,72
MTP7927 BKLT_FB1 51,72
12/18 add FB7/ FB8
MTP7609 +3P3V_PANEL_EN 65
I2C
MTP76102 EDP_I2C_SCL 51
MTP7662 EDP_I2C_SDA 51
MTP7690 EDP_I2C_INT 10,51
eDP
MTP7654 PMI_I2C_SDA 25,28,33
MTP7647 PMI_I2C_SCL 25,28,33
PWR Monitor
EV1 留一組即可
MTP7653 PMI1_I2C_SCL_R 28
MTP7676 PMI1_I2C_SDA_R 28
MTP7602 PCH_SAM_SNSR_SDA 32,33,35
MTP7666 PCH_SAM_SNSR_SCL 32,33,35
PCH & SAM
Camera
MTP7691 RTD3_CAM_PWREN 25,57
MTP7661 CAM_IR_STB 49
MTP7664 CAM_IR_STB_R 49
CPU Controller
MTP7678 VIDSCLK 13,66
MTP7611 VIDSOUT 13,66
Uart
MTP76191 PCH_DBG_TX 25,29,33
MTP76192 PCH_DBG_RX 25,29,33
MTP76193 SAM_DBG_TX 29,33,34,71
MTP76194 SAM_DBG_RX 29,33,34,71
SL1
MTP7645 SL1_EN_N 63
MTP7617 SL1_HPD2 70,71
MTP7697 SL1_HPD1A 70,71
MTP76104 SL1_HPD1B 70,71
MTP76175 SL1_PSU_DET 34,70
MTP76174 SL1_HPD2_EN#_MTP R7601 1KOHM SL1_HPD2_EN# 35,72
DDR_PWR GD
MTP7646 DDR_PGD_SIL 58
MTP7698 +1P1V_DDR_PG 60
SAM_SW _DBG
MTP76110 SAM_SWD_SWO 29,33,34
MTP7642 SAM_SWD_CLK 29,33,34
MTP7663 SAM_SWD_DIO 29,33,34
MTP76201 SL1_PWR_GOOD 55,70
TS PWR
+1P8V_TS +5V_TS
MTP76202
MTP76203
WIFI PWR
+3P3V_WWAN
MTP76198
+VDD_BATA_PACK
MTP7633 MTP7650 MTP7688 MTP7643 MTP7668 MTP76111 MTP7618 MTP7640
MTP7959 MTP7610 MTP7660 MTP7680 MTP76112 MTP76113 MTP7605 MTP7622
Place close to J7001
12/18 change from J7702 to J7001
PWR_SL1
MTP76154 MTP76155 MTP76156 MTP76157 MTP76158 MTP76159 MTP76160 MTP76161
MTP76162 MTP76163 MTP76164 MTP76165 MTP76166 MTP76167 MTP76168 MTP76169
Place close to J7101
MTP76190 Place Close(Under) to JP4001
AGND
CPU_PWR
+VCCSTG +VCC_RTC +VCCST_CPU +VCCIN +VCCIN_AUX +VCCPLL_OC +VCC1P8A
MTP7627 MTP7636 MTP7621 MTP7637 MTP7665 MTP7625 MTP7693
Standby PWR
+1P8VSB +3P3VSB +5VSB
MTP7652 MTP7681 MTP7648
Memory PWR
+0P6V_DDR_VDDQ +1P1V_DDR_VDD2 +1P8V_DDR_VDD1
MTP7679 MTP7604 MTP7634
Type-C PWR
+VBUS_P0_CONN
MTP76114 MTP76115 MTP76116 MTP76117 MTP76118 MTP76119
System PWR
PWR_SL1_F +VSYS EXT_DC_IN +3P3V +1P8VA +3P3VA +3P3VAS
MTP7626 MTP76182 MTP76183 MTP76185 MTP7692 MTP76184 MTP76199
Panel PWR
+VCC_EDP_BKLT_OUT +3P3V_PANEL +1P8V_PANEL
MTP76120 MTP76121 MTP76179 MTP76196
Audio PWR
+1P8V_AUDIO +5V_AUDIO
MTP7603 MTP7624
SSD PWR
+3P3V_SSD +1P1V_SSD
MTP76186 MTP76197
MTP7616 MTP7685 MTP76131 MTP76132 MTP76133 MTP76134 MTP76135 MTP76136 MTP76137 MTP76138 MTP76139 MTP76140
GND MTP Close to J5401
GND MTP Close to J5401
GND MTP close to U5505
GND MTP close to J5701
GND MTP close to J5701
GND MTP close to J5401
GND MTP close to J7701
GND MTP close to J7701
GND MTP close to J7701
GND MTP close to J7701
GND MTP close to J7701
GND MTP close to J7701
MTP76170 MTP76171 MTP76172
GND
MTP76103 SAM_PIO0_3 34
MTP76105 SAM_PIO0_4_ISP0 34
MTP76106 SAM_PIO0_5_ISP1 34
MTP76107 SAM_PIO0_6_ISP2 34
MTP7615 SAMRTS_PCHCTS 25,29,33,34
MTP76108 TCON_VENDOR_ID 24,51
MTP7689 PCHRTS_SAMCTS 25,29,33,34
MTP76109 TP_CATERR#_R 10
MTP76141 SAM_RESET# 29,33,34,58
MTP7623 SSD_FLUSH 43
Title: Frames, Holes, & Mechanical
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 76 of 82
W x H 427.7 x 276 mm


+3P3V_PD_OUT
C7708 1UF/6.3V ALL
R7709 100Kohm ALL
R7711 100Kohm ALL
U7703
VSYS
CC1 CON_CC1
CC2 CON_CC2
SBU1 CON_SBU1
SBU2 CON_SBU2
SBUEN FLAG
GND
NX20P0407UK ALL
TCP0_CC1
TCP0_CC2
TCP0_SBU1
TCP0_SBU2
TCP0_SBUEN
TCP0_FLG
TCP0_CONN_CC1
TCP0_CONN_CC2
TCP0_CONN_SBU1
TCP0_CONN_SBU2
R7708 1MOHM ALL
R7702 1MOHM ALL
GND
+VBUS_P0_CONN
J7701
USB_CON_24P
TCP0_TX_P0
TCP0_TX_N0
TCP0_TXRX_N1
TCP0_TXRX_P1
TCP0_TXRX_P0
TCP0_TXRX_N0
TCP0_TX_N1
TCP0_TX_P1
L7703
L7704
L7701
L7702
0nH
TCP0_TX_RT_P0
TCP0_TX_RT_N0
TCP0_TXRX_RT_N1
TCP0_TXRX_RT_P1
TCP0_TXRX_RT_P0
TCP0_TXRX_RT_N0
TCP0_TX_RT_N1
TCP0_TX_RT_P1
C7732 C7722 0.22uF/25V
C7703 C7704 0.33uF/25V
C7705 C7707 0.33uF/25V
C7734 C7730 0.22uF/25V
TCP0_TX_CONN_P0
TCP0_TX_CONN_N0
TCP0_TXRX_CONN_N1
TCP0_TXRX_CONN_P1
TCP0_TXRX_CONN_P0
TCP0_TXRX_CONN_N0
TCP0_TX_CONN_N1
TCP0_TX_CONN_P1
USB2_TCP0_CONN_A_DP
USB2_TCP0_CONN_A_DN
USB2_TCP0_CONN_B_DN
USB2_TCP0_CONN_B_DP
Use 220K ohm on connector side to protect pin short to VBUS
R7791 R7761 R7771 R7781 220K
C7725 100pF/50V DNP
C7724 100pF/50V DNP
D7702 PESD24VF1BL
D7715 PESD24VF1BL
D7708 PESD24VF1BL
D7709 PESD24VF1BL
D7717 PTVSC4V5S1UR
R7756 99.9Kohm ALL
C7710 0.1uF/35V
C7717 2.2uF/35V
C7711 0.1uF/35V
C7706 2.2uF/35V
TRUTH TABLE
S OE FUNCTION
X H Disconnect
L L D = D1
H L D = D2
+3P3VSB
U7908
TS3USB30ERSWR
R7704 R7705 to short pin
R7704 0Ohm
R7705 0Ohm
TCP0_BB_SBU1
TCP0_BB_SBU2
Jalama 2/11 change connect to P29
D7710 D7711 D7716 D7718 D7703 D7707 D7712 D7714
AZ4685-01H_AMAZING
GPIO_3P3V_PU_AUX_N
GPIO_3P3V_PU_AUX_P
TCP0_AUX_DP
TCP0_AUX_DN
TCP0_DIRECT_AUX_DP
TCP0_DIRECT_AUX_DN
R7707 R7703 ALL 100Kohm 1%
C7701 C7702 0.1uF/25V ALL
R7706 100Kohm ALL
C7945 0.1UF/6.3V
+1P8VSB
R7701 100Kohm ALL
TCP0_BYP_AUX_CTRL#
TCP0_DBG0_A_DP
TCP0_DBG1_A_DN
TCP0_DBG0_A_DP_R
TCP0_DBG1_A_DN_R
R7749 R7750 DBG_0Ohm
L7708 0909-00BP0QS 90ohm
DNP
RN7704B RN7704A
D7721 D7720 PESD5V0H1BSF
USB2_TCP0_CONN_A_DP
USB2_TCP0_CONN_A_DN
TCP0_DBG2_B_DP
TCP0_DBG3_B_DN
TCP0_DBG2_B_DP_R
TCP0_DBG3_B_DN_R
R7753 R7754 DBG_0Ohm
L7707 0909-00BP0QS 90ohm
RN7703B RN7703A
D7719 D7722 PESD5V0H1BSF
USB2_TCP0_CONN_B_DP
USB2_TCP0_CONN_B_DN
+3P3V_DEBUG
C7750 0.1UF/6.3V
U7704
TS3USB30ERSWR
USB2_TCP0_DP
USB2_TCP0_DN
R7758 100Kohm 1% DBG_D
USB2_TCP_MUX_EN#
PD_USB2_MUX_FLIP
R7780 0ohm DBG_N
Q7701 RUM002N02GT2L DBG_D
MUX0_EN#
R7759 100Kohm 1% DBG_D
U7704 Layout Short during PV/DV
TRUTH TABLE
S OE FUNCTION
X H Disconnect
L L D = D1
H L D = D2
Report errors to Steven
Title: Type-C_TBT_Retimer
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name B52
Rev 1.00
Date: Friday, June 28, 2019
Sheet 77 of 82

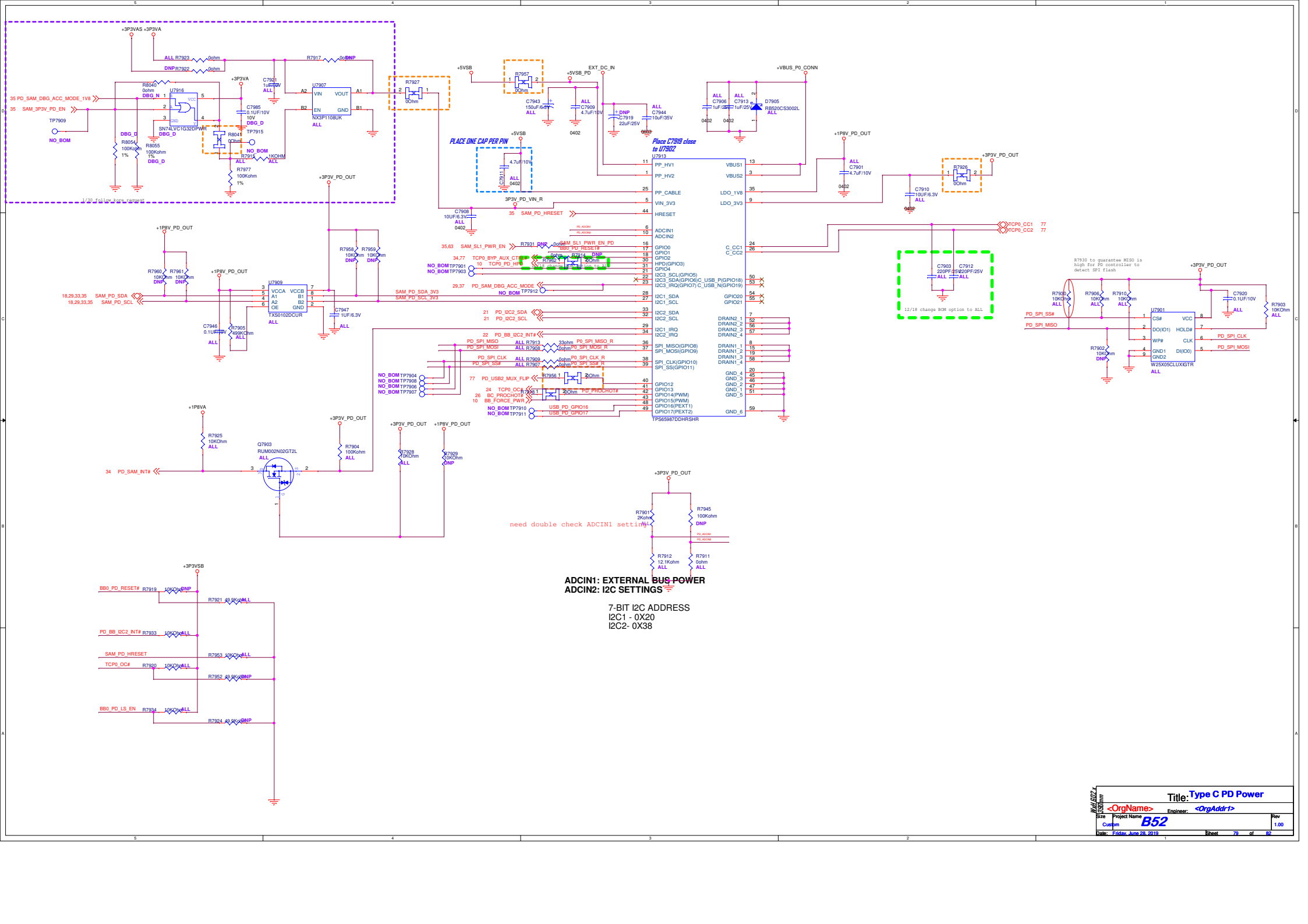
Title: Blank

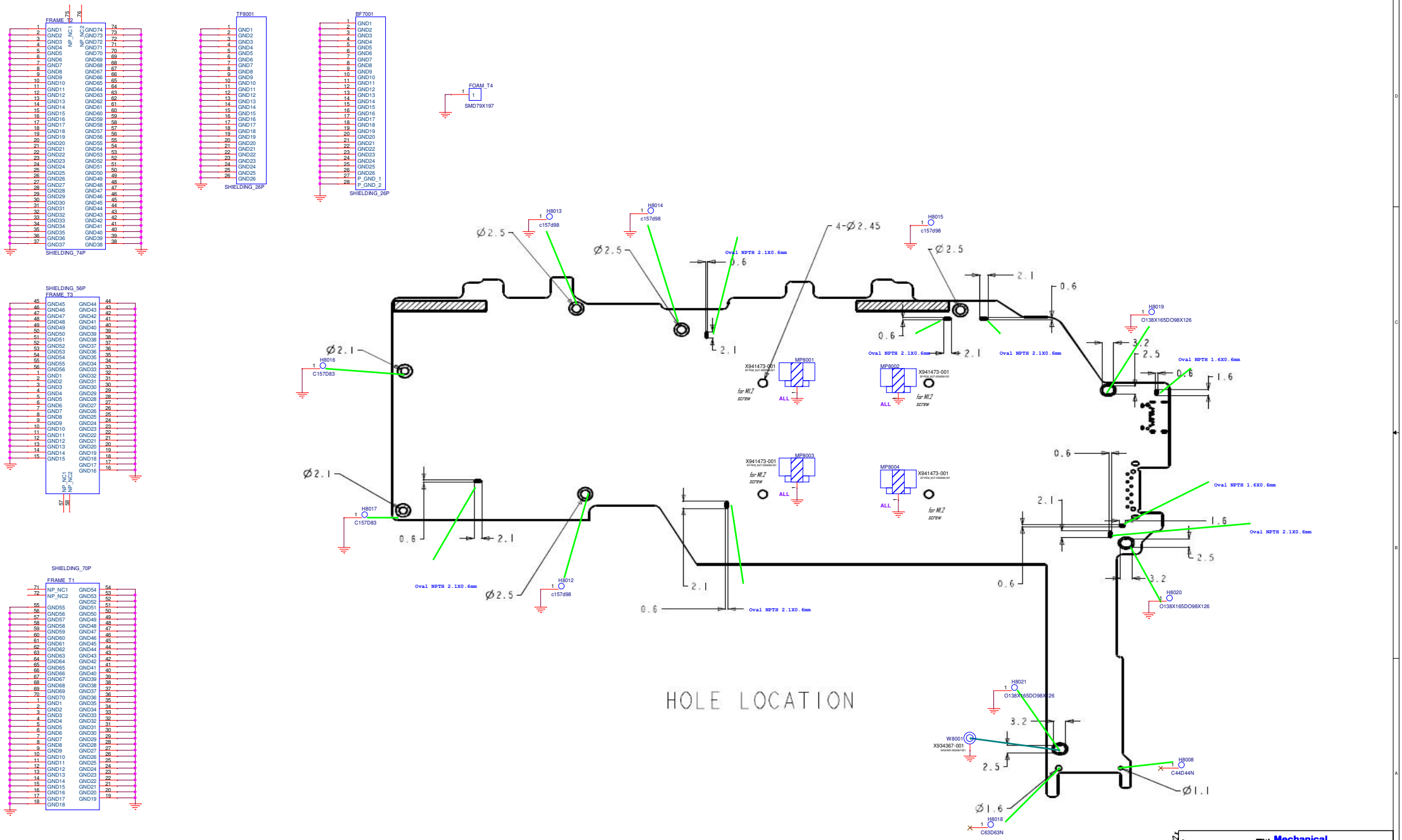
<OrgName> Engineer: <OrgAddr1>

Size: A4 | Project Name: B52 | Rev: 1.00

Custom

Date: Friday, June 28, 2019 | Sheet 78 of 82


+3P3VAS +3P3VA
ALL R7923 0ohm
DNP R7922 0ohm
R7917 0ohm DNP
35 PD_SAM_DBG_ACC_MODE_1V8
35 SAM_3P3V_PD_EN
TP7909
NO_BOM
R8040 0ohm DBG_N
U7916
SN74LVC1G32DPWR
DBG_D
R8054 100Kohm 1% DBG_D
R8055 100Kohm 1% DBG_D
+3P3VA
C7985 0.1UF/10V 10V DBG_D
R8041 0Ohm
TP7915
NO_BOM
R7915 ALL 1KOHM ALL
R7977 100Kohm 1%
C7921 1uF/10V ALL
U7907
VIN VOUT
EN GND
NX3P1108UK ALL
A2 A1 B2 B1
R7927 0Ohm
1/30 Follow Kore request
+5VSB
R7957 0ohm
C7943 150uF/6.3V ALL
+5VSB_PD
EXT_DC_IN
ALL C7909 4.7uF/10V
DNP C7919 22uF/25V 0805
ALL C7944 10uF/35V
+VBUS_PD_CONN
ALL C7906 1uF/25V 0402
ALL C7913 1uF/25V 0402
D7905 RB520CS3002L ALL
PLACE ONE CAP PER PIN
+5VSB
C7911 4.7uF/10V ALL 0402
Place C7919 close to U7302
U7913
PP_HV1 PP_HV2 PP_CABLE VIN_3V3 HRESET ADCIN1 ADCIN2
GPIO0 GPIO1 GPIO2 HPD(GPIO3) GPIO4
I2C3_SCL(GPIO5) I2C3_SDA(GPIO6)C_USB_P(GPIO18) I2C3_IRQ(GPIO7) C_USB_N(GPIO19)
I2C1_SDA I2C1_SCL I2C2_SDA I2C2_SCL I2C1_IRQ I2C2_IRQ
SPI_MISO(GPIO8) SPI_MOSI(GPIO9) SPI_CLK(GPIO10) SPI_SS(GPIO11)
GPIO12 GPIO13 GPIO14(PWM) GPIO15(PWM) GPIO16(PEXT1) GPIO17(PEXT2)
VBUS1 VBUS2 LDO_1V8 LDO_3V3 C_CC1 C_CC2 GPIO20 GPIO21
DRAIN2_1 DRAIN2_2 DRAIN2_3 DRAIN2_4 DRAIN1_1 DRAIN1_2 DRAIN1_3 DRAIN1_4 GND_4 GND_3 GND_2 GND_1 GND_5 GND_6
TPS65987DDHRSHR
+1P8V_PD_OUT
ALL C7901 4.7uF/10V 0402
C7910 10UF/6.3V ALL 0402
+3P3V_PD_OUT
R7926 0Ohm
3P3V_PD_VIN_R
35 SAM_PD_HRESET
C7908 10UF/6.3V ALL 0402
TCP0_CC1 77
TCP0_CC2 77
C7903 220PF/25V ALL
C7912 220PF/25V ALL
12/18 change BOM option to ALL
R7930 to guarantee MISO is high for PD controller to detect SPI flash
R7930 10KOhm ALL
R7906 10KOhm ALL
R7910 10KOhm ALL
PD_SPI_SS#
PD_SPI_MISO
U7901
CS# VCC DO(IO1) HOLD# WP# CLK GND1 DI(IO0) GND2
W25X05CLUXIGTR
C7920 0.1UF/10V ALL
R7903 10KOhm ALL
PD_SPI_CLK
PD_SPI_MOSI
R7902 10KOhm DNP
+1P8V_PD_OUT
R7960 10KOhm DNP
R7961 10KOhm DNP
+3P3V_PD_OUT
R7958 10KOhm DNP
R7959 10KOhm DNP
18,29,33,35 SAM_PD_SDA
18,29,33,35 SAM_PD_SCL
U7909
VCCA VCCB A1 B1 A2 B2 OE GND
TXS0102DCUR ALL
C7947 1UF/6.3V ALL
C7946 0.1UF/10V ALL
R7905 499KOhm ALL
SAM_PD_SDA_3V3
SAM_PD_SCL_3V3
35,63 SAM_SL1_PWR_EN
R7931 DNP 0ohm
SAM_SL1_PWR_EN_PD
BB0_PD_RESET#
R7914 DNP 0Ohm
34,77 TCP0_BYP_AUX_CTL
10 TCP0_PD_HPD
R7962 0Ohm
NO_BOM TP7901
NO_BOM TP7903
29,37 PD_SAM_DBG_ACC_MODE
NO_BOM TP7912
21 PD_I2C2_SDA
21 PD_I2C2_SCL
22 PD_BB_I2C2_INT#
PD_SPI_MISO
PD_SPI_MOSI
ALL R7913 33ohm P0_SPI_MISO_R
ALL R7908 0ohm P0_SPI_MOSI_R
PD_SPI_CLK
PD_SPI_SS#
ALL R7909 0ohm P0_SPI_CLK_R
ALL R7907 0ohm P0_SPI_SS#_R
77 PD_USB2_MUX_FLIP
R7956 1 20Ohm
24 TCP0_OC#
R7961 1 20Ohm PD_PROCHOT#
26 BC_PROCHOT#
10 BB_FORCE_PWR
USB_PD_GPIO16
USB_PD_GPIO17
NO_BOM TP7910
NO_BOM TP7911
NO_BOM TP7904
NO_BOM TP7905
NO_BOM TP7906
NO_BOM TP7907
+1P8VA
R7925 10KOhm ALL
Q7903 RUM002N02GT2L ALL
34 PD_SAM_INT#
R7904 100Kohm ALL
+3P3V_PD_OUT
+3P3V_PD_OUT
R7928 10KOhm ALL
+1P8V_PD_OUT
R7929 10KOhm DNP
need double check ADCIN1 setting
+3P3V_PD_OUT
R7901 2Kohm ALL
R7945 100Kohm DNP
R7912 12.1Kohm ALL
R7911 0ohm ALL
ADCIN1: EXTERNAL BUS POWER
ADCIN2: I2C SETTINGS
7-BIT I2C ADDRESS
I2C1 - 0X20
I2C2- 0X38
+3P3VSB
BB0_PD_RESET# R7919 10KOhm DNP
R7921 49.9Kohm ALL
PD_BB_I2C2_INT# R7933 10KOhm ALL
SAM_PD_HRESET
R7953 10KOhm ALL
TCP0_OC# R7920 10KOhm ALL
R7952 49.9Kohm DNP
BB0_PD_LS_EN R7934 10KOhm ALL
R7924 49.9Kohm DNP
Title: Type C PD Power
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: B52
Rev: 1.00
Date: Friday, June 28, 2019
Sheet 79 of 82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FRAME_T3
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FRAME_T1
H8013
H8014
H8015
H8016
H8017
H8012
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H8020
H8021
H8008
H8018
W8001
X934367-001
X941473-001
MP8001
MP8002
MP8003
MP8004
Ø2.5
Ø2.1
4-Ø2.45
Ø1.6
Ø1.1
Oval NPTH 2.1X0.6mm
Oval NPTH 1.6X0.6mm
for M1.2 screw
ALL
O138X165DO98X126
C157D83
c157d98
C44D44N
C63D63N
HOLE LOCATION
Title: Mechanical
<OrgName>
Engineer:
<OrgAddr1>
Project Name B52
Size Custom
Rev 1.00
Date: Friday, June 28, 2019
Sheet 80 of 82

Title: X		
<OrgName> Engineer:	<OrgAddr1>	
Size: A2	Project Name: B52	Rev: 1.00
Date: Friday, June 28, 2019	Sheet 81 of 82	