Lenovo Mississippi_uATX Schematic Rev:0.4

Reference	Description
CB	0.1UF_0402
CP	0.01UF_0402
CM	1UF_0603

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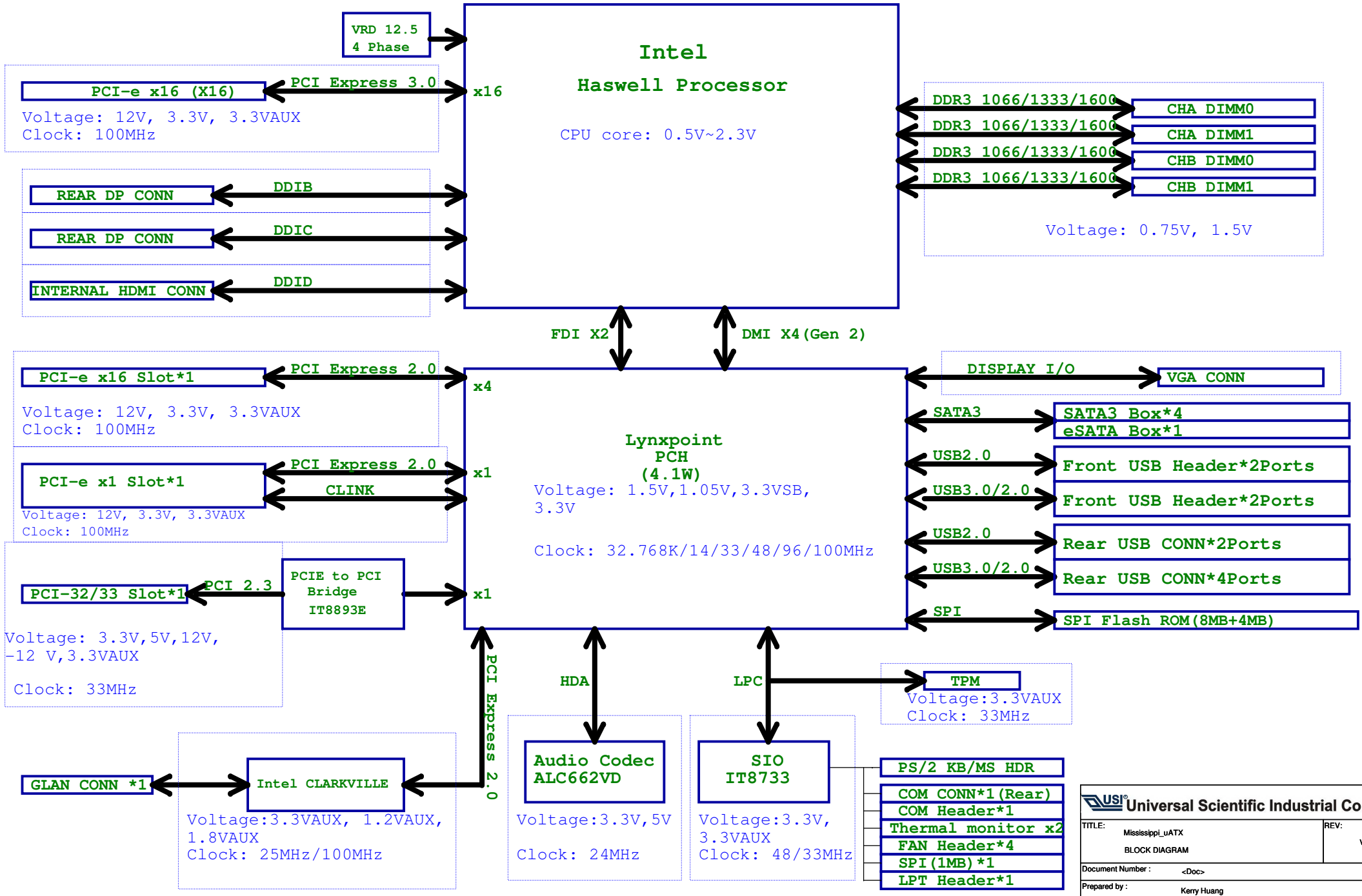
Block Diagram – Mississippi_uATX



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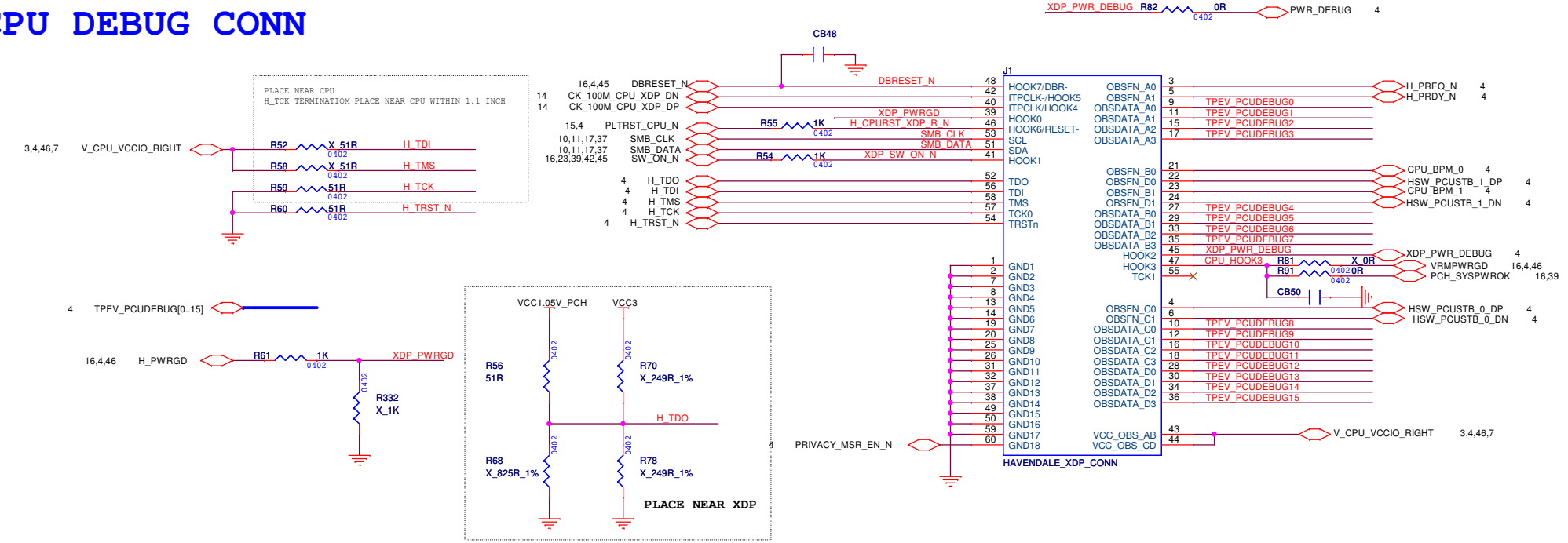
CPU DEBUG CONN



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Prepared by : Kerry Huang		
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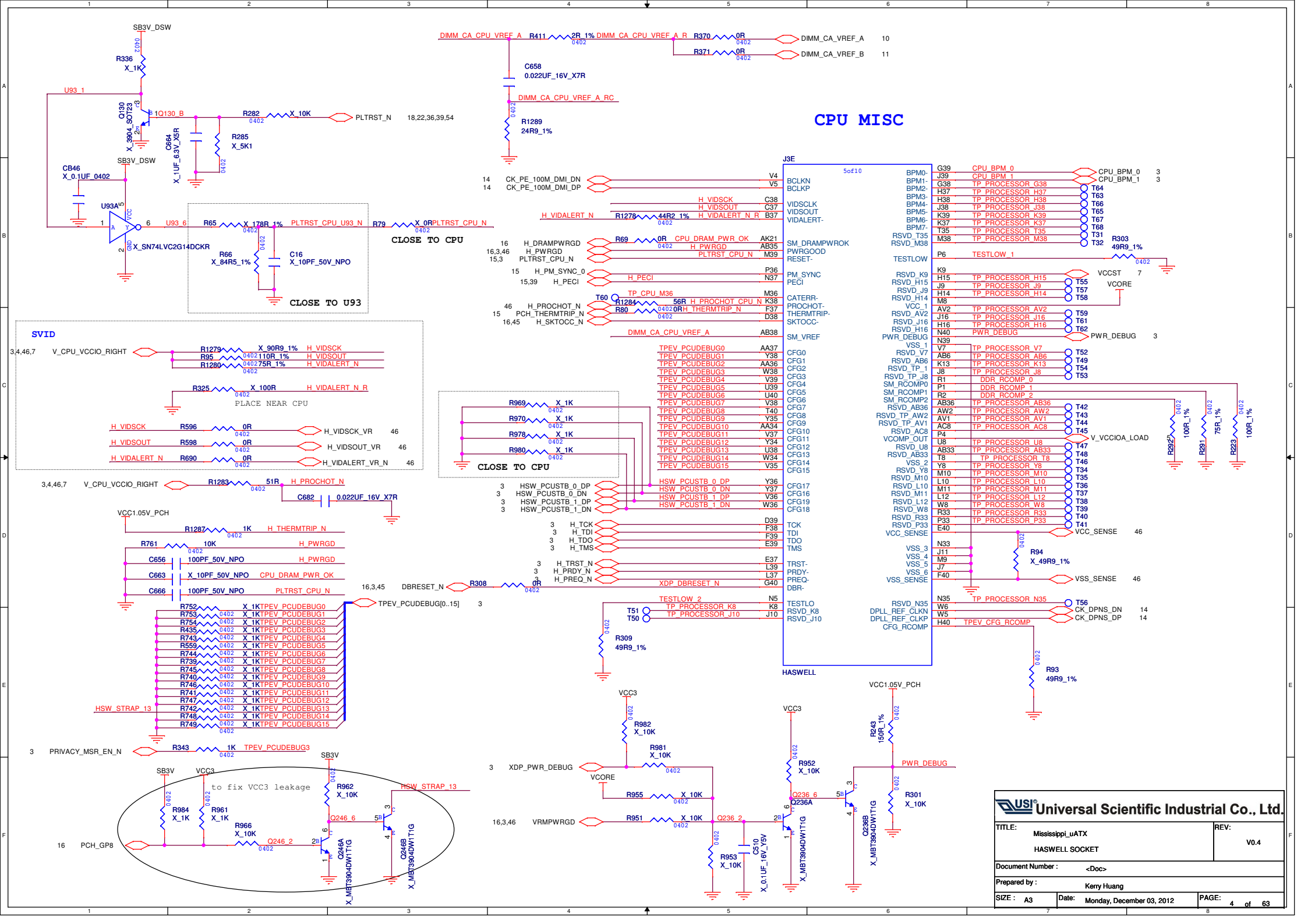
CPU MISC



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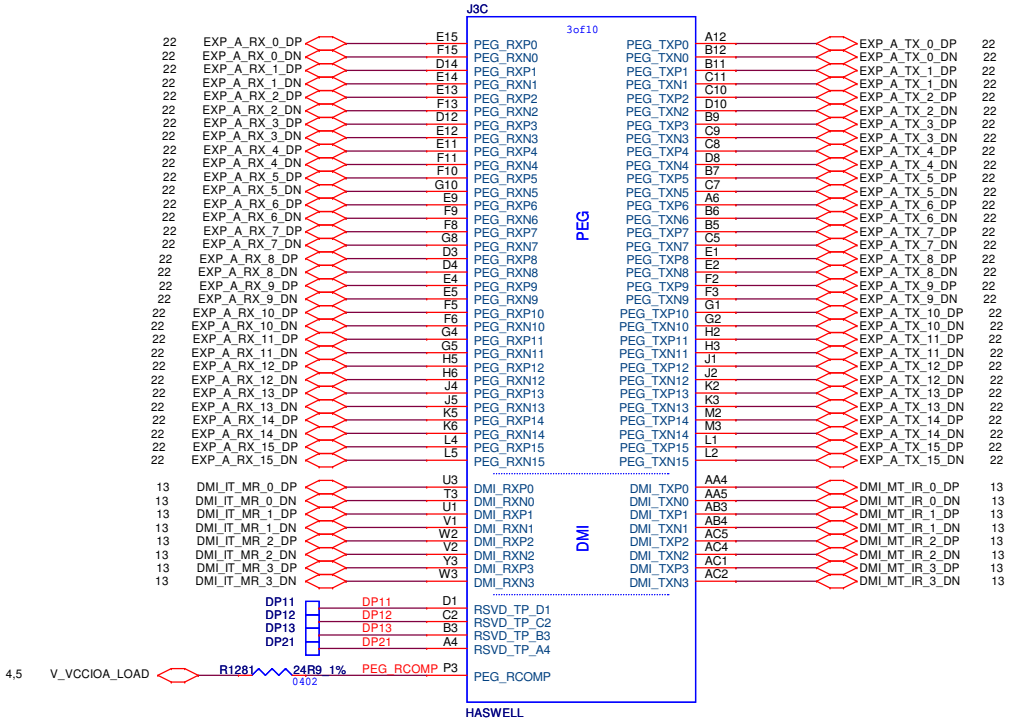
CPU PEG / DMI / GEN



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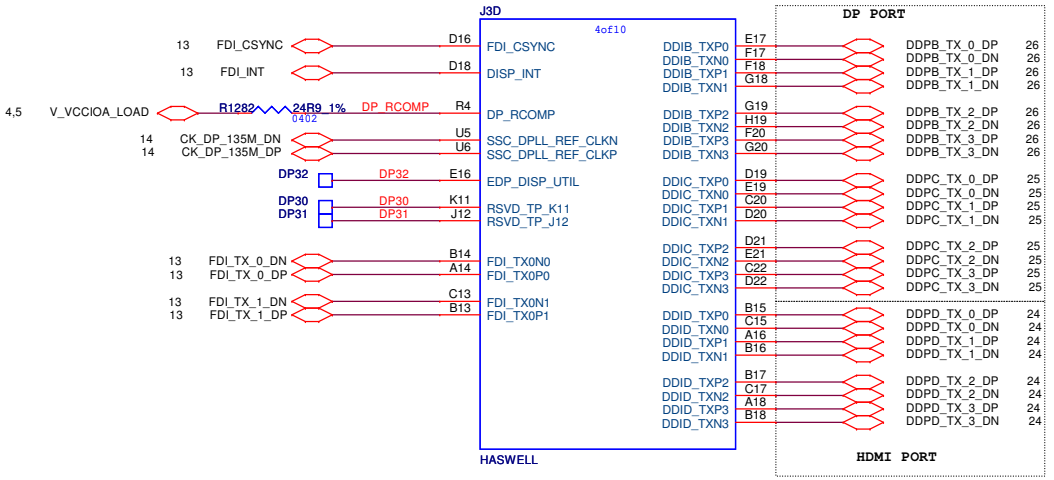

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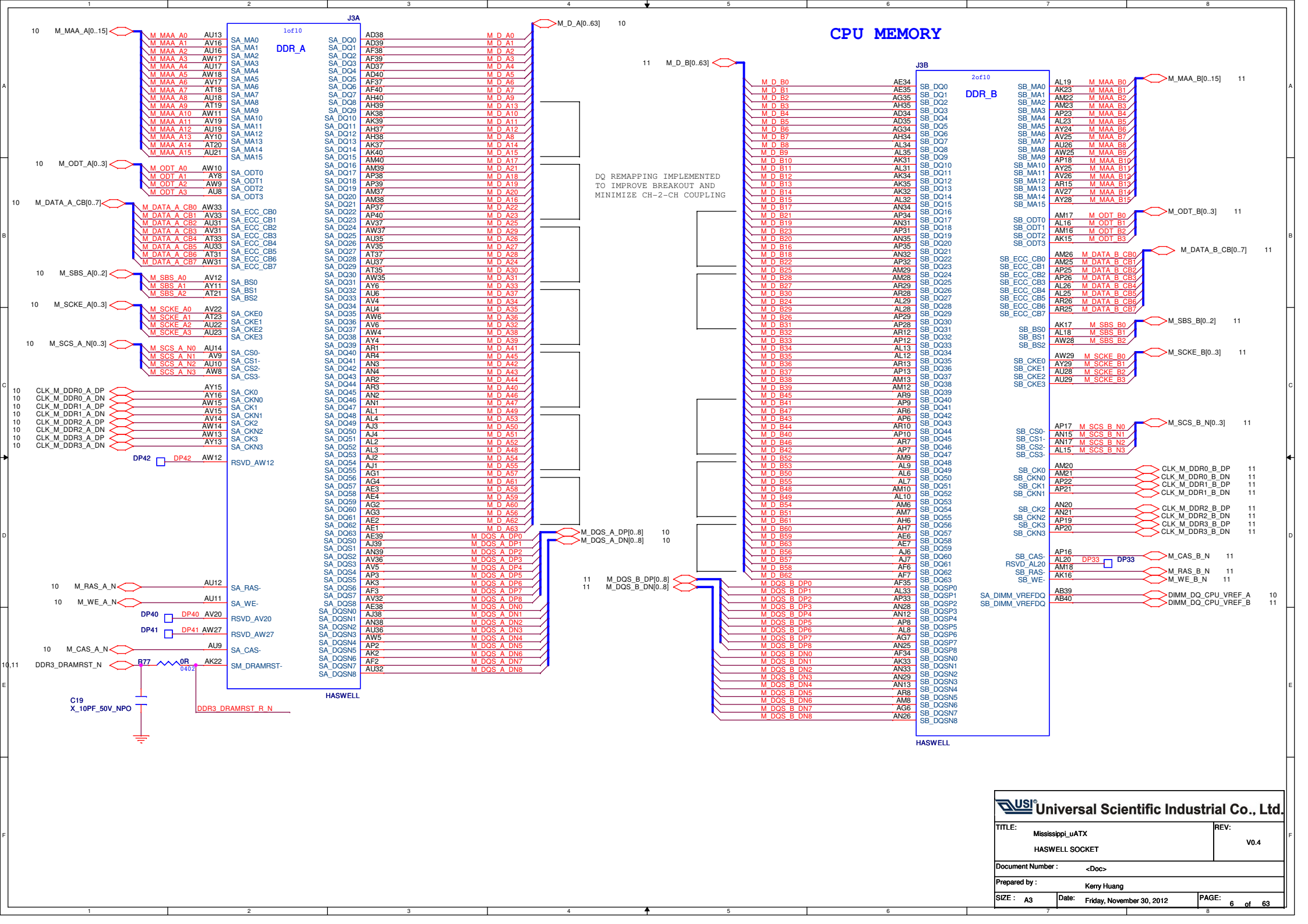
CPU MEMORY



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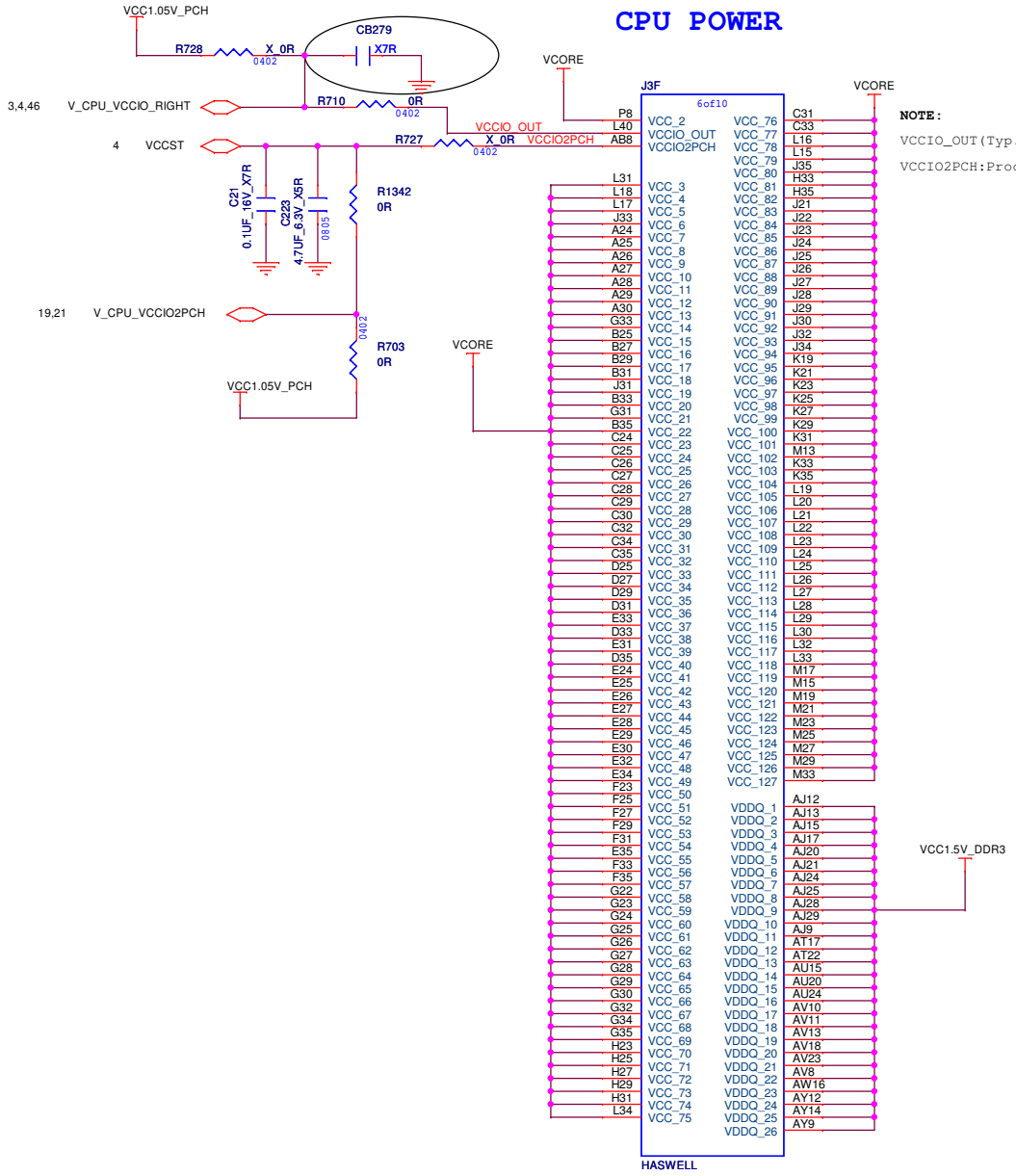
CPU POWER



NOTE:

VCCIO_OUT(Typ. 1V):Processor power reference for I/O

VCCIO2PCH:Processor power reference to PCH

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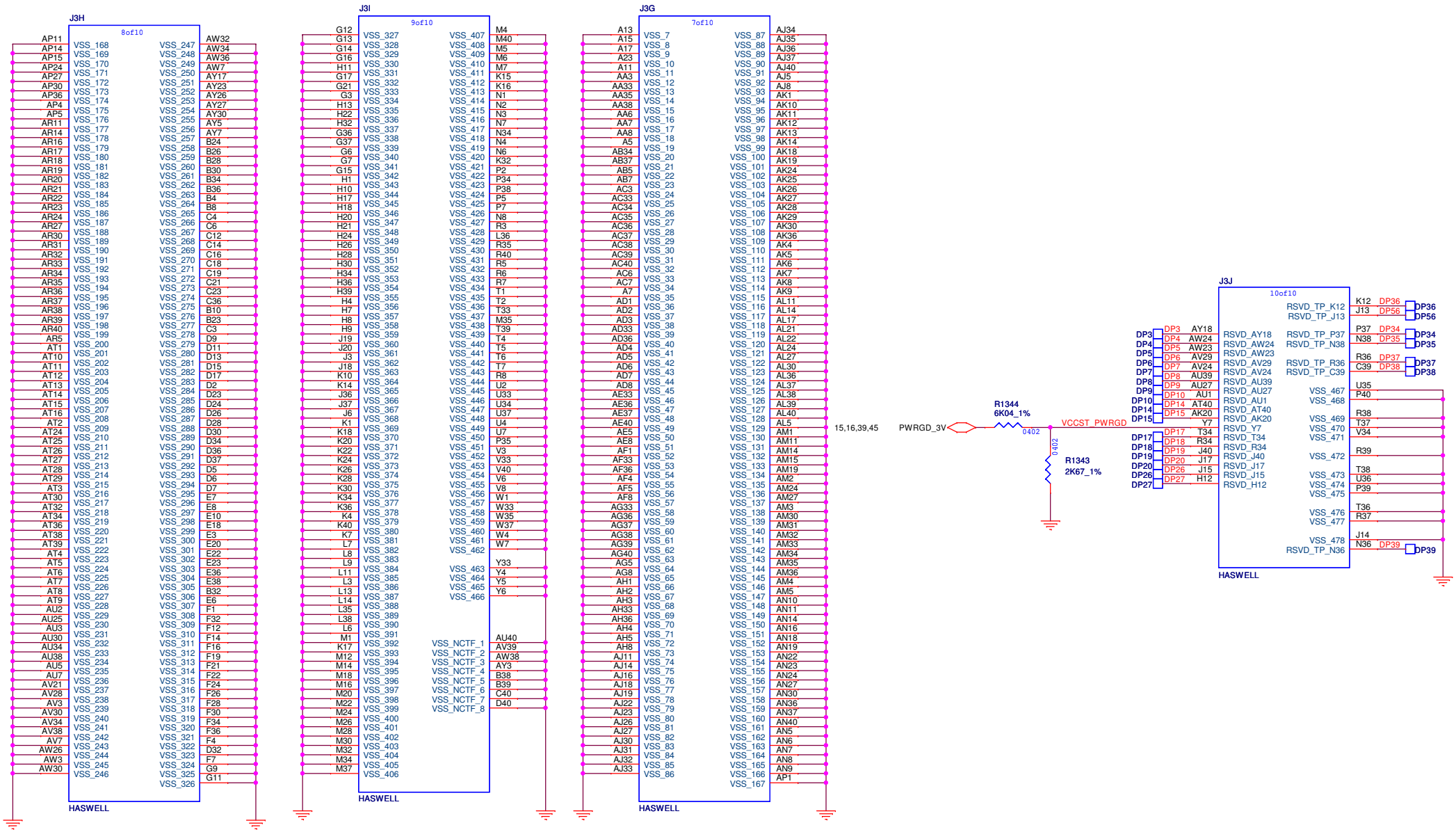
CPU GND



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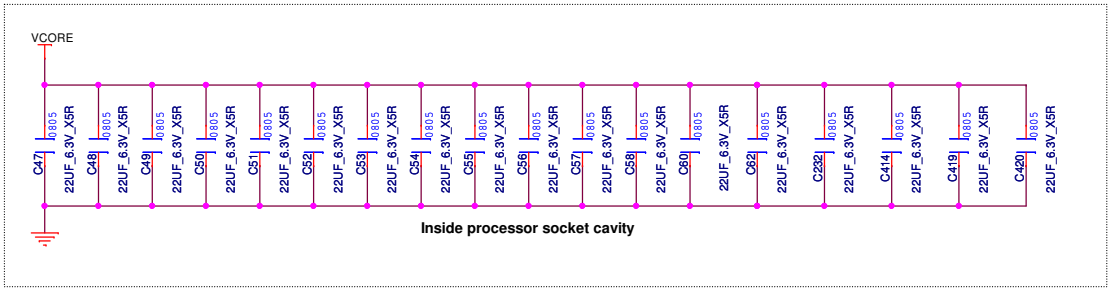
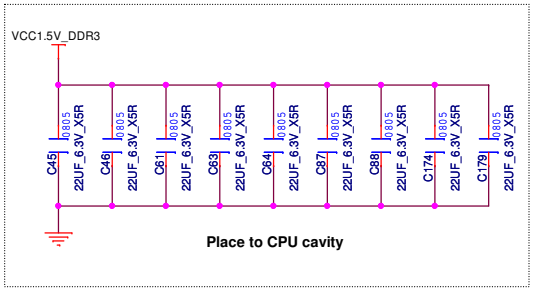
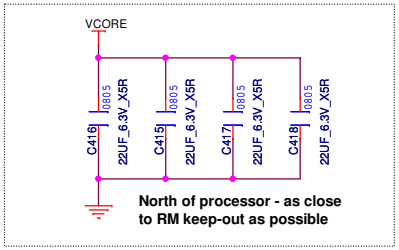
CPU DECOUPLING







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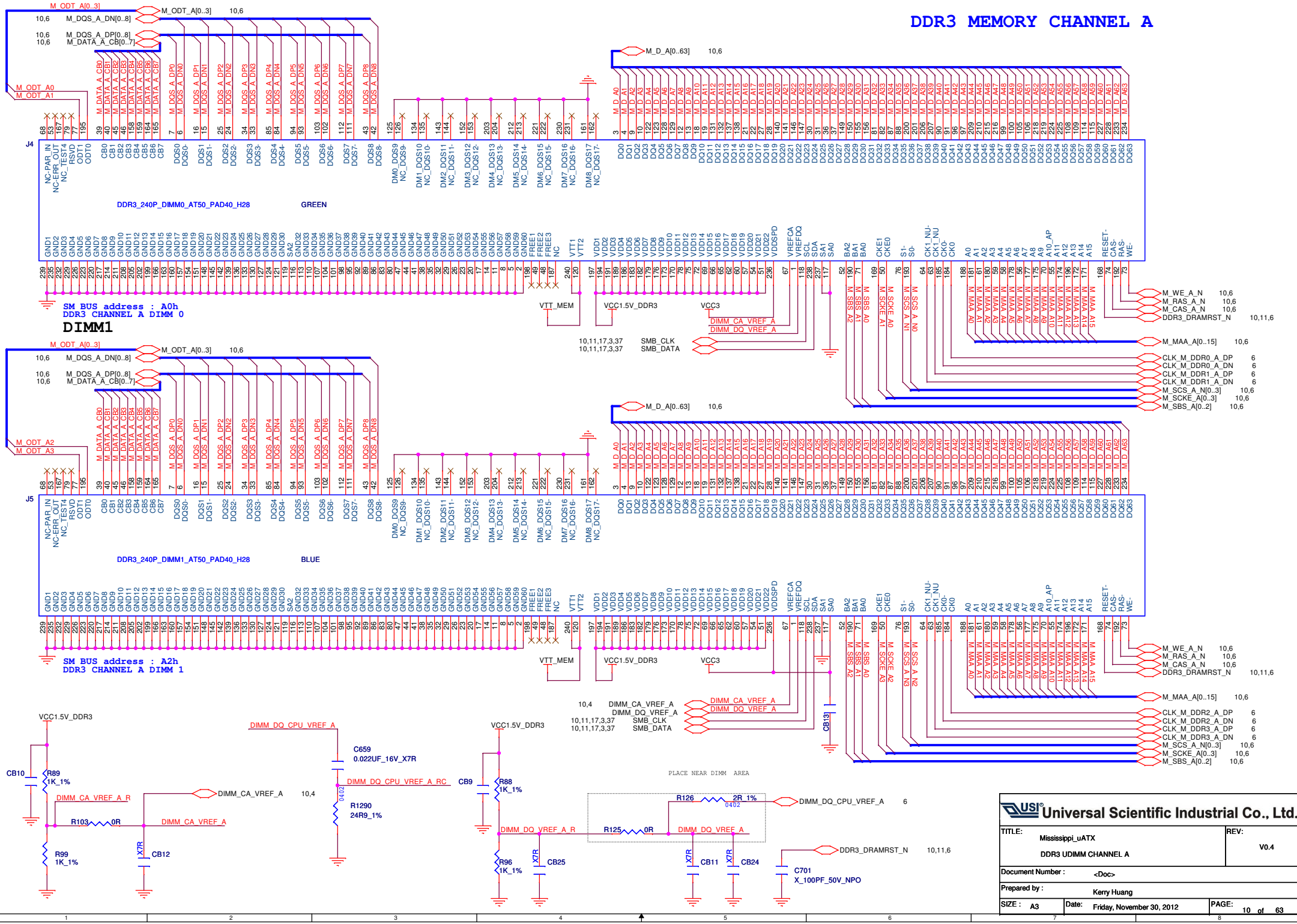
DDR3 MEMORY CHANNEL A



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DDR3 MEMORY CHANNEL B

DDR3_240P_DIMM2_AT50_PAD40_H28 GREEN

SM BUS address : A4h
DDR3 CHANNEL B DIMM 0

DIMM3

DDR3_240P_DIMM3_AT50_PAD40_H28 BLUE

SM BUS address : A6h
DDR3 CHANNEL B DIMM 1

DIMM4

PLACE NEAR DIMM AREA

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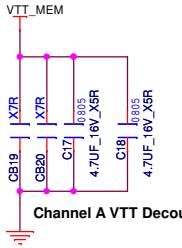
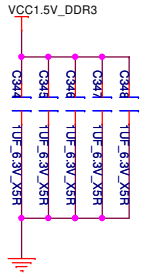
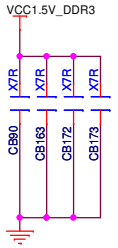
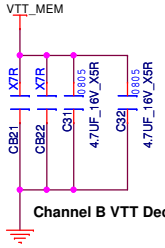
DDR3 DIMM DECOUPLING



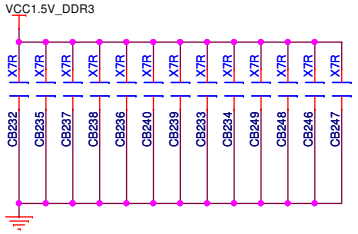
Channel A VTT Decoupling Caps

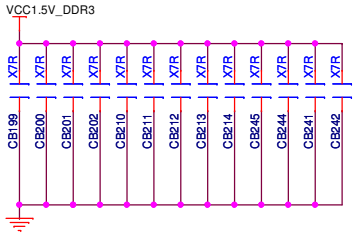




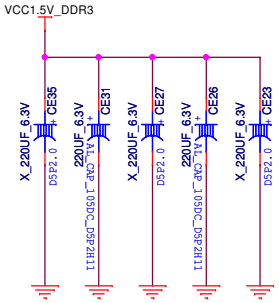


Channel B VTT Decoupling Caps

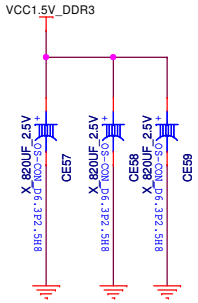




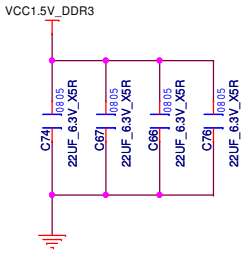
Stitching caps for DDR3 CHB CTRL and CMD



Place between CHA and CHB



Place top side of CHA



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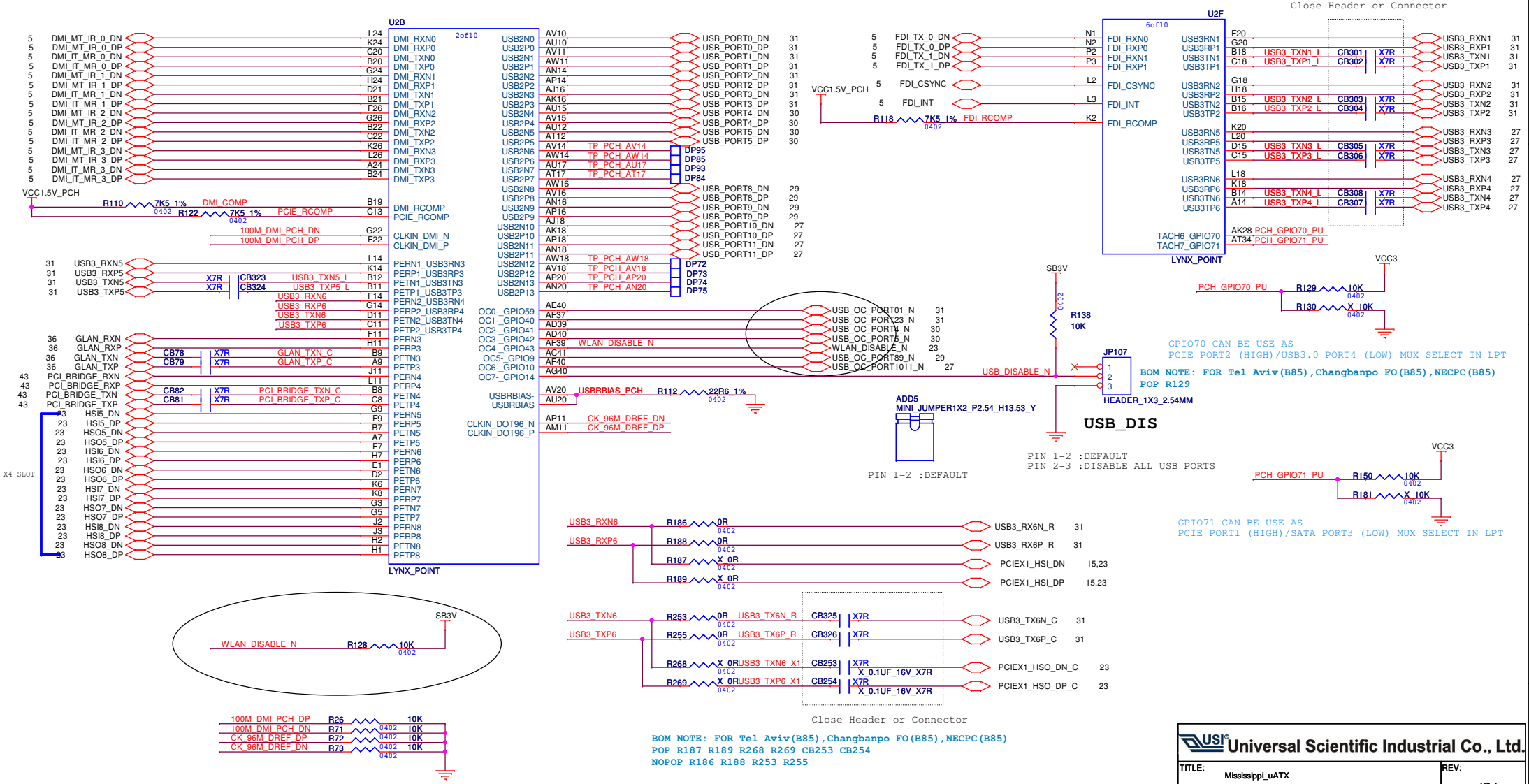
PCH DMI/PCIE/USB

PCH FDI/USB3.0



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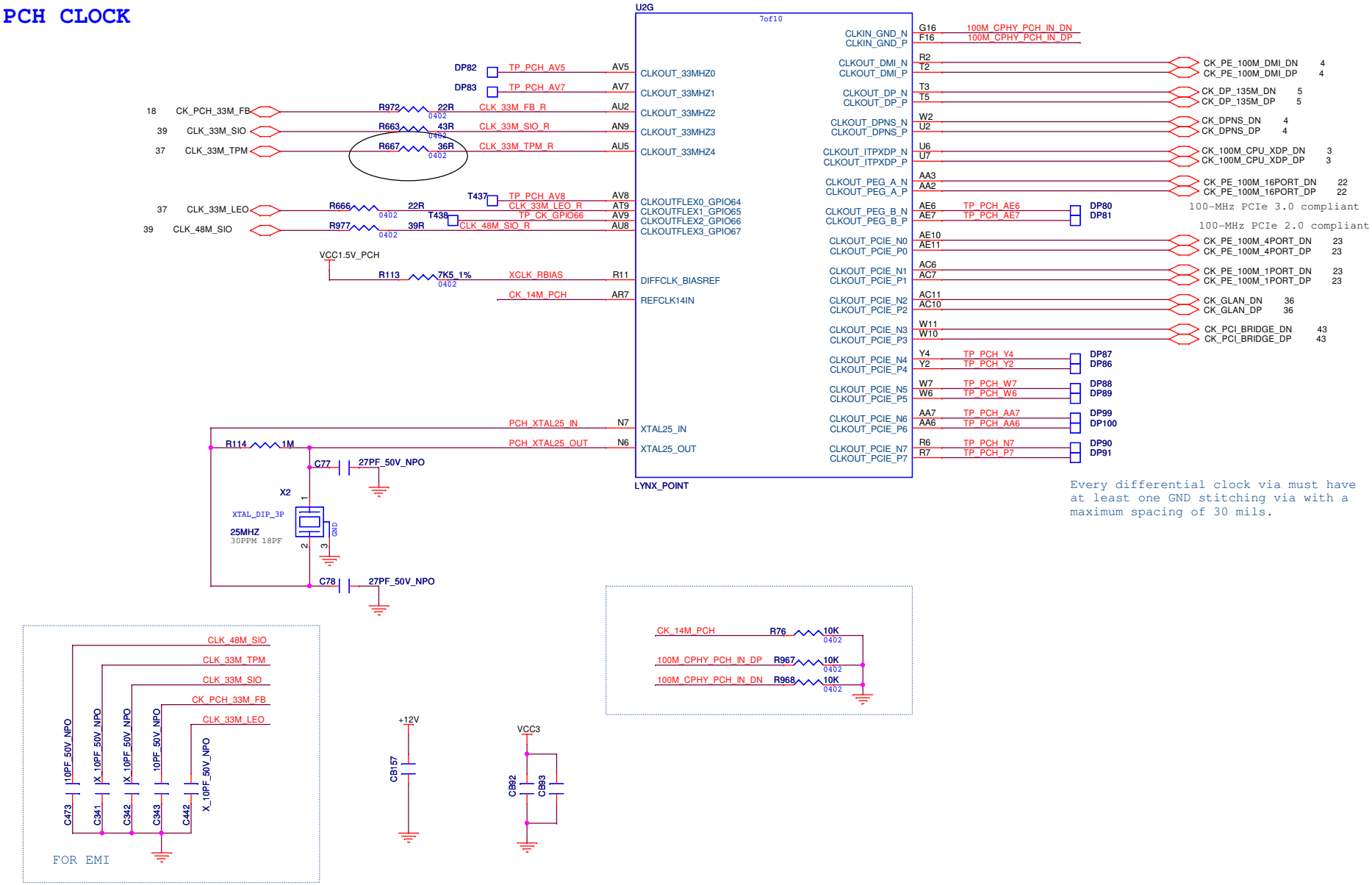
PCH CLOCK



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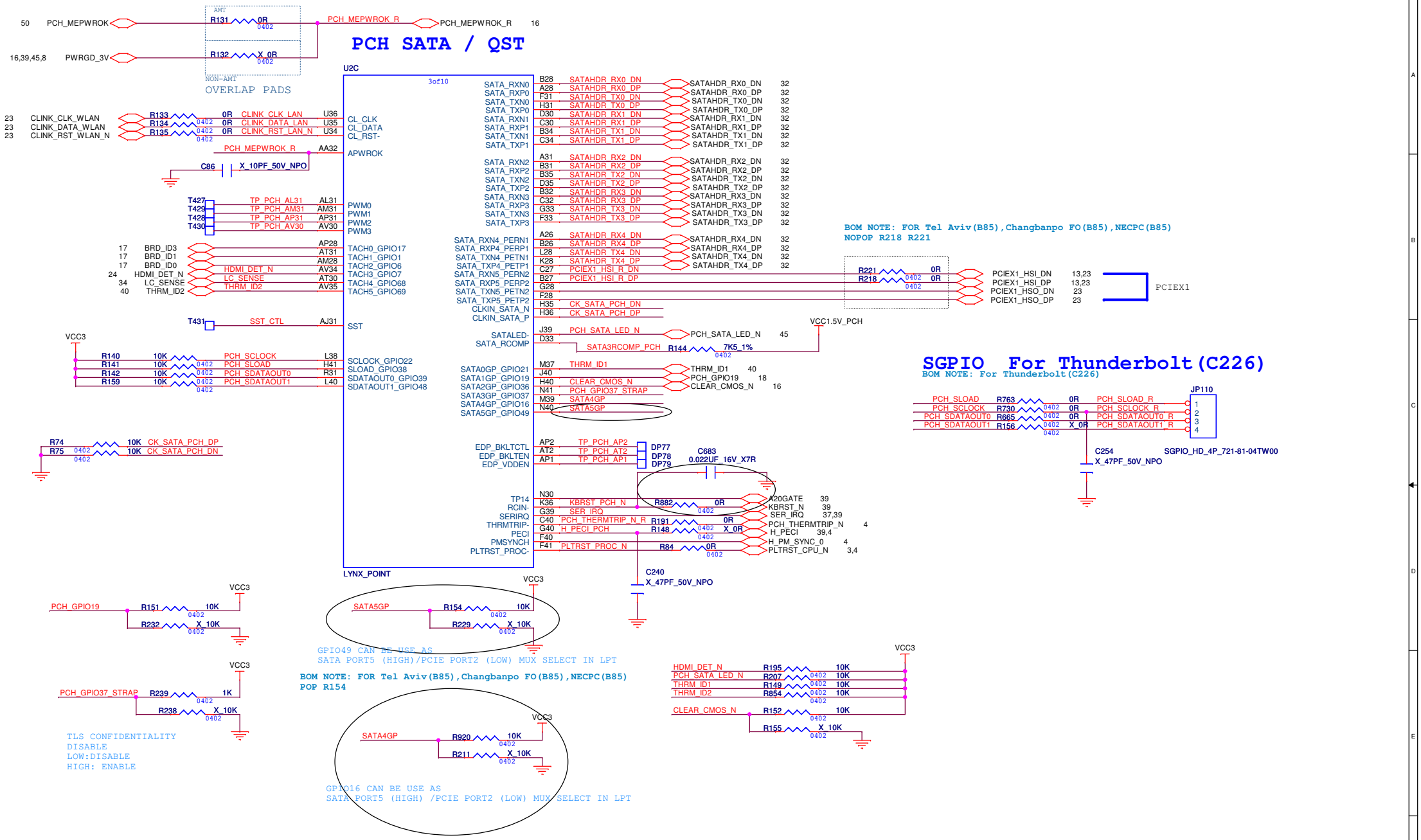
PCH SATA / QST



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PCH LPC/ HDA/ SPI/SMB

U2D
4of10
LYNX_POINT

STRAPS

ME disable header

RTC SOURCE

BATTERY

CLEAR CMOS

CASE INTRUDER HEADER

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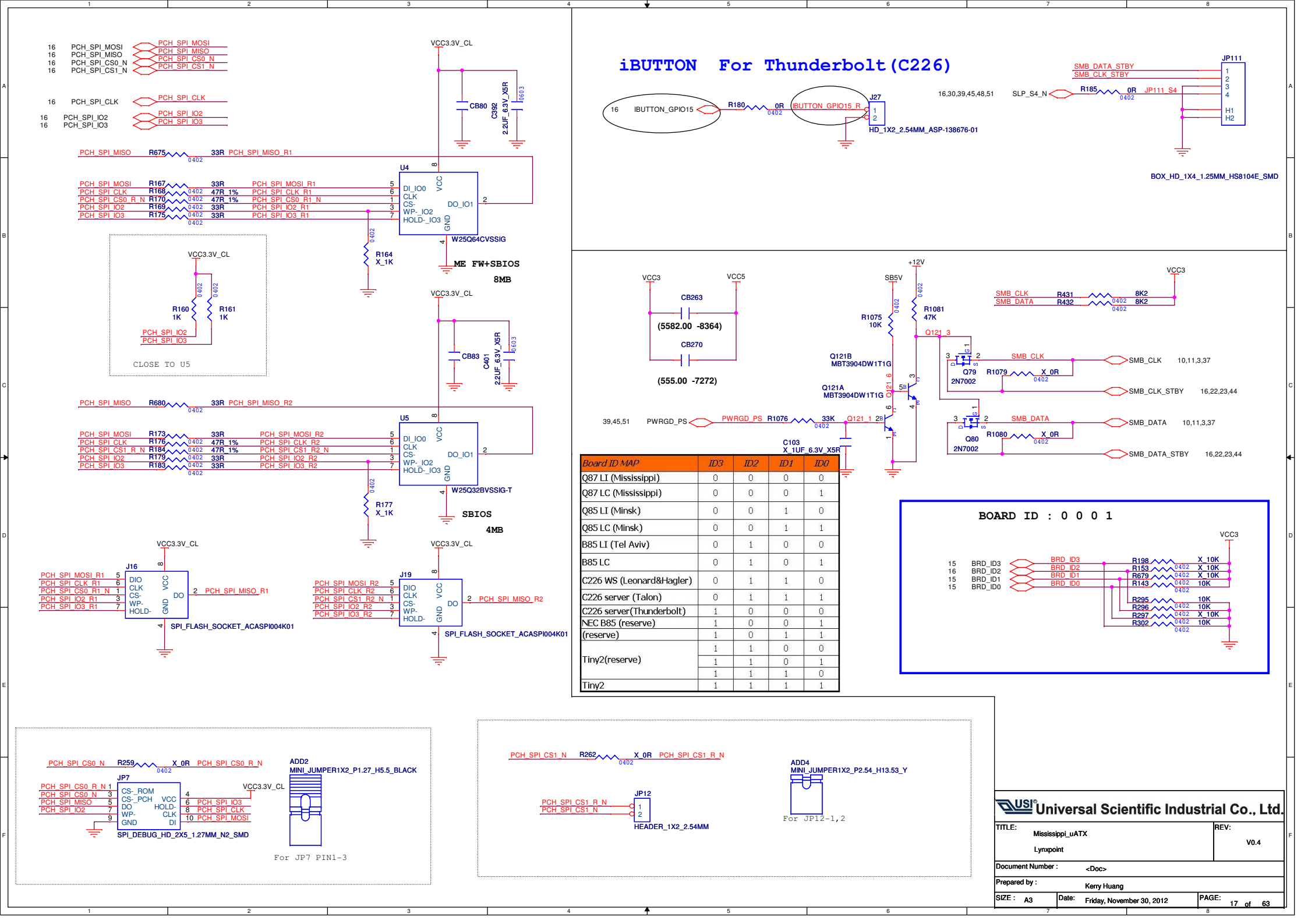

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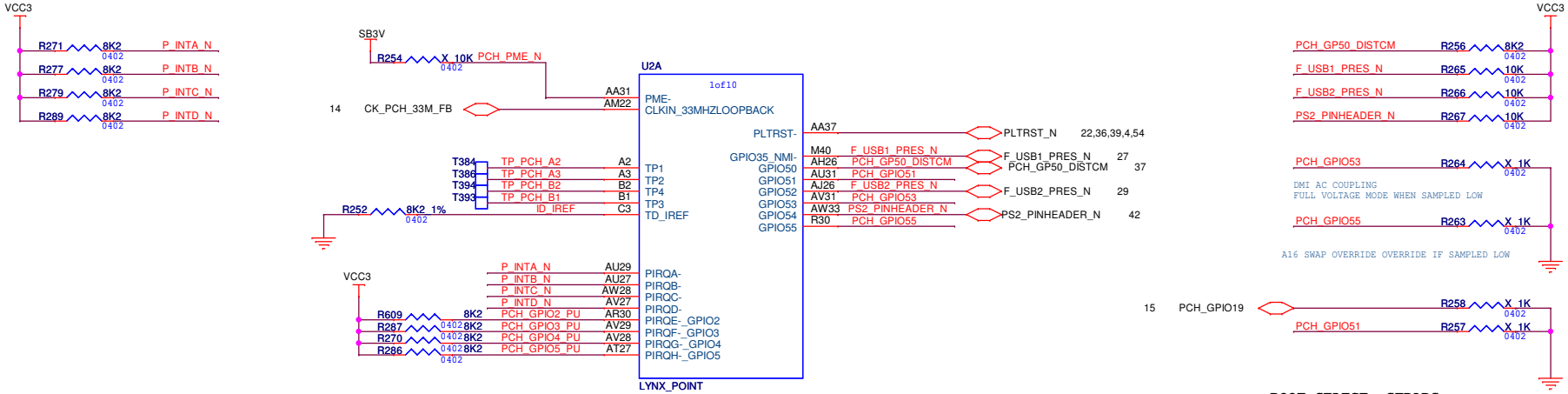
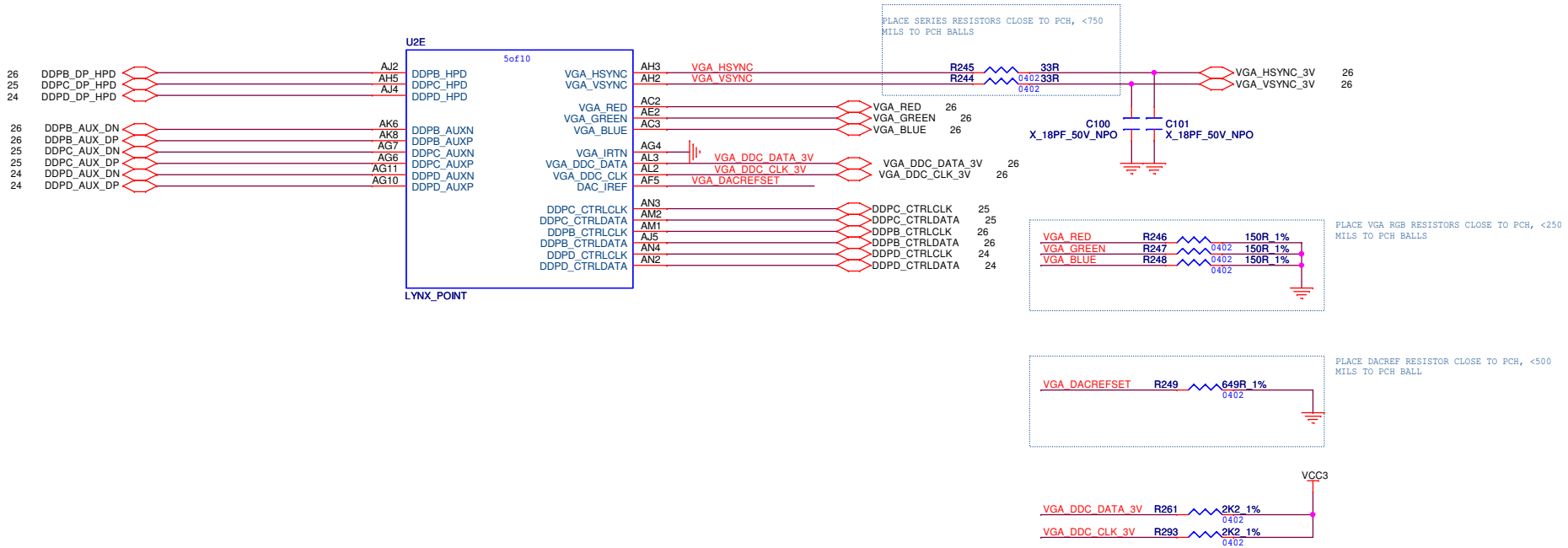


BOOT SELECT STRAPS

BOOT DEVICE	GPIO19	GPIO51
LPC	0	0
* **SPI**	**1**	**1**

PCH DISPLAY



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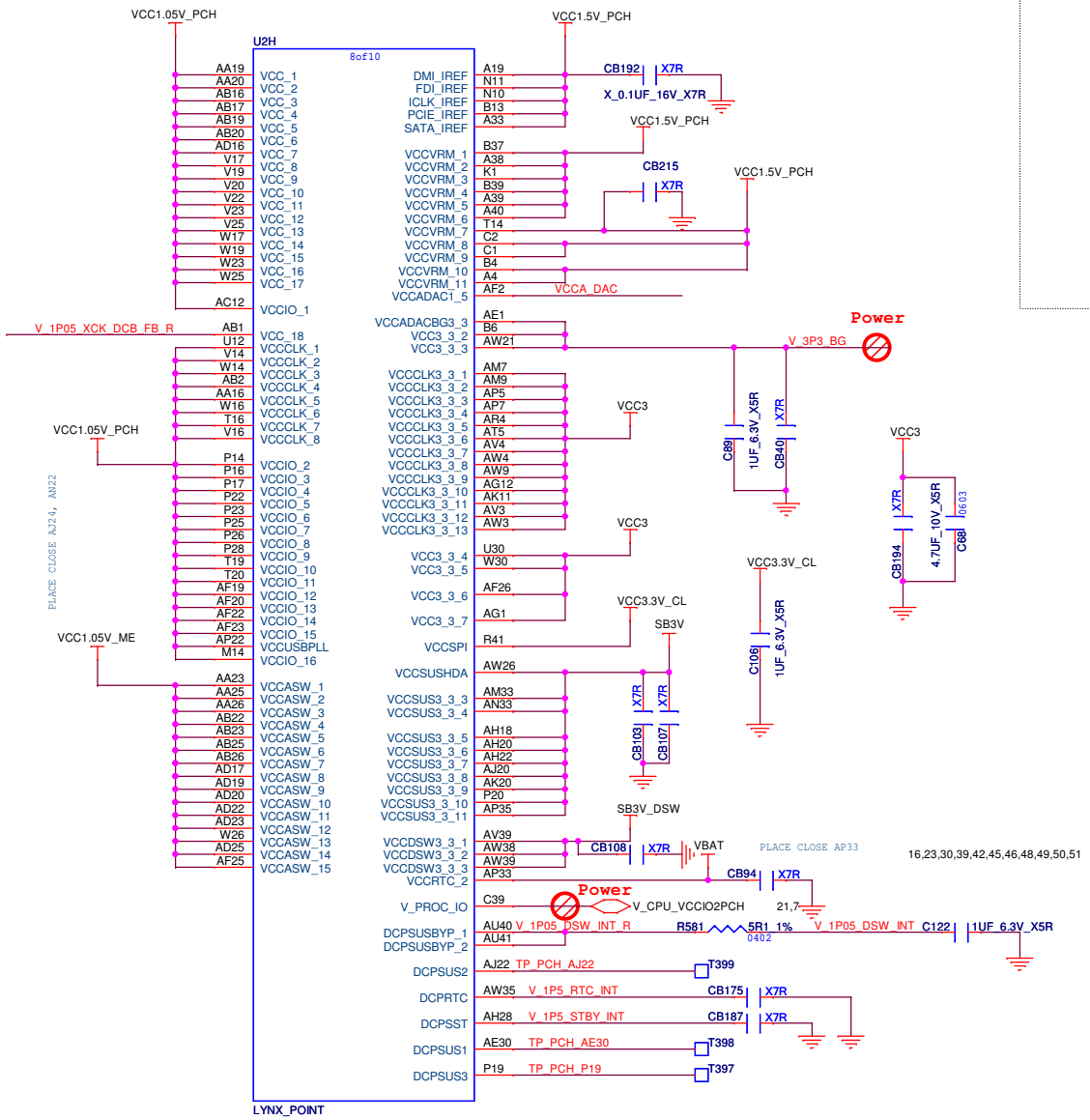
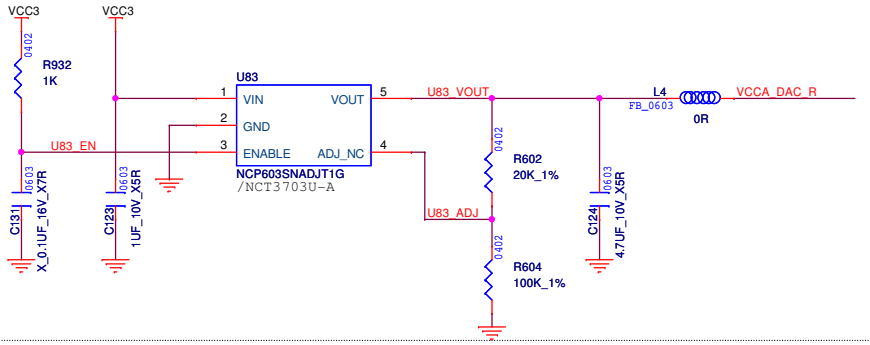
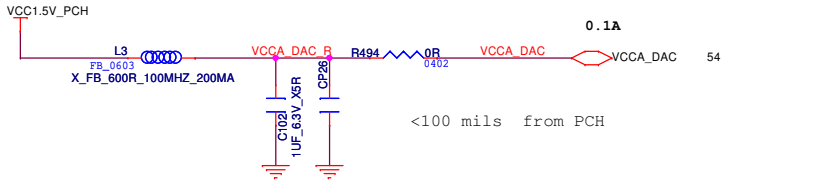
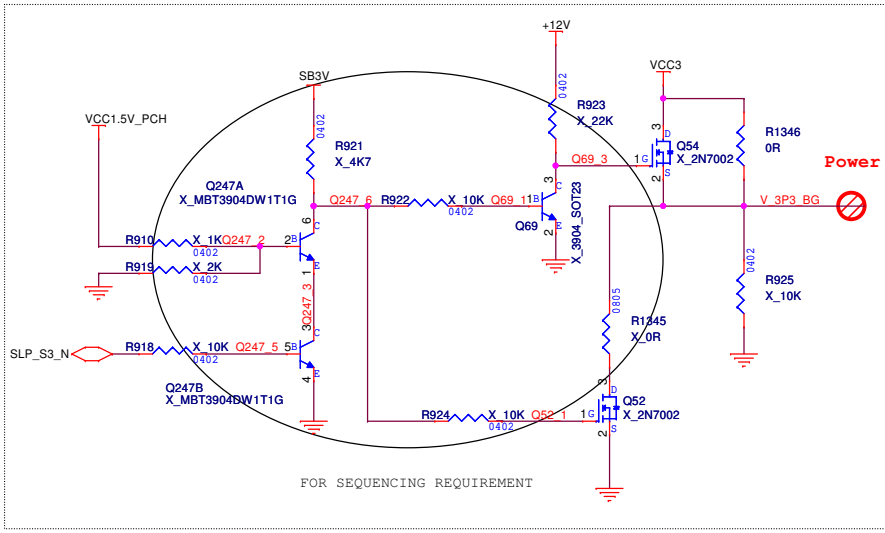
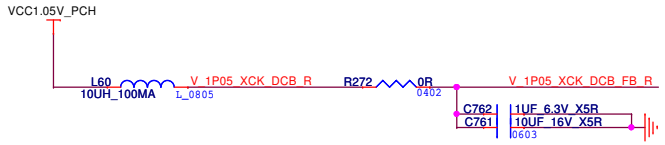
PCH POWER











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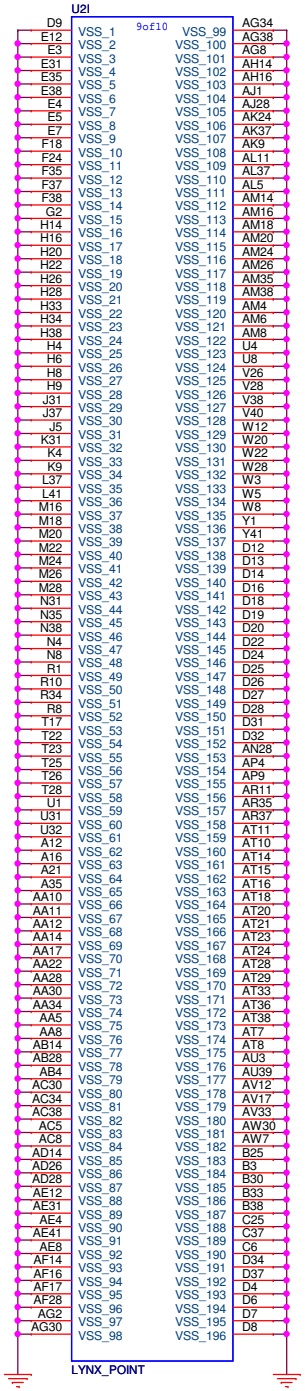
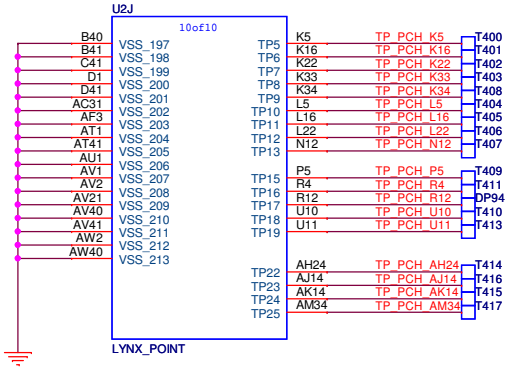
PCH GND





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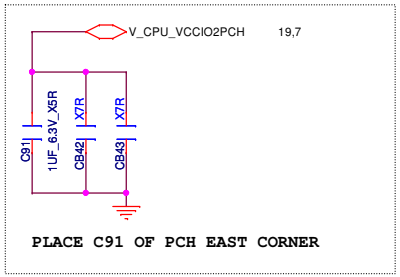
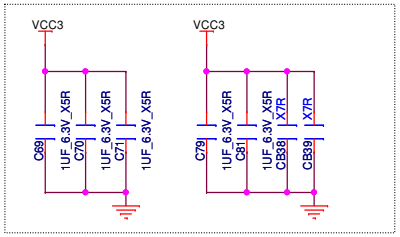
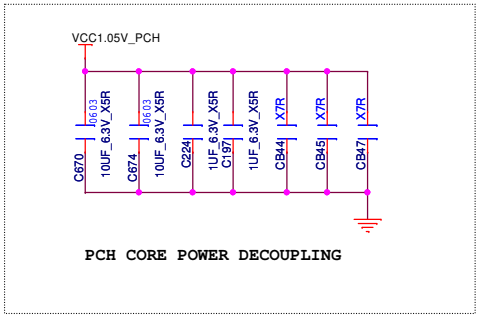
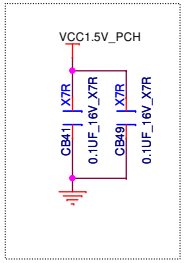
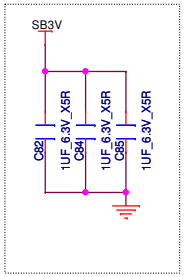
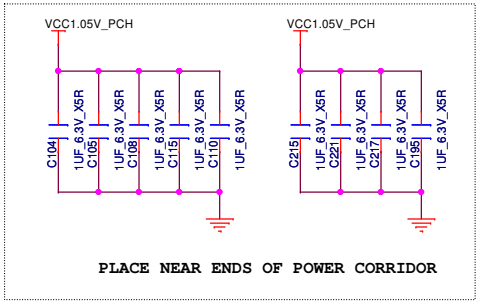


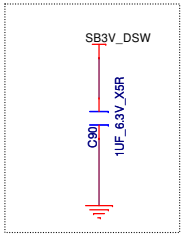


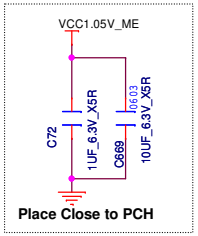




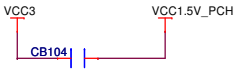


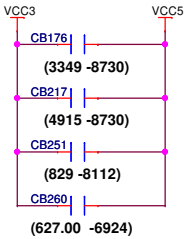


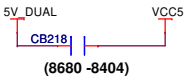


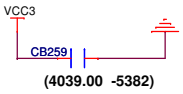


STITCHING CAP









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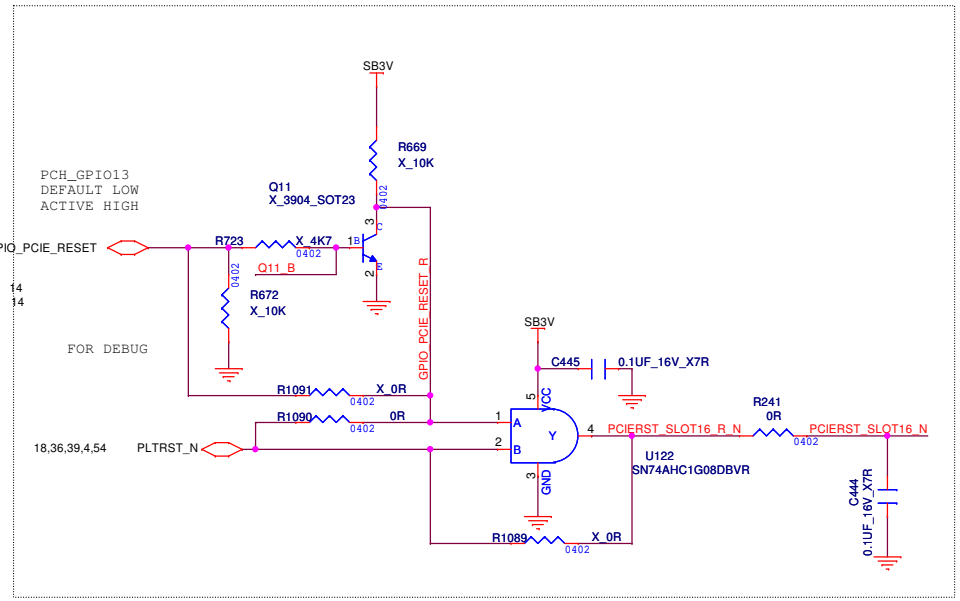
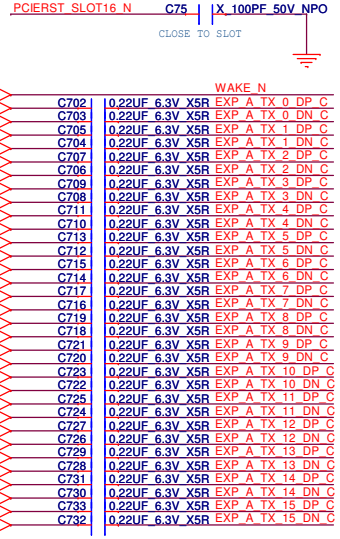
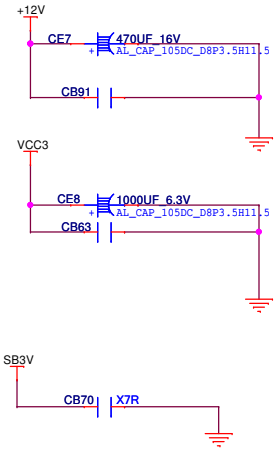
Slot1

PCIE16X Gen3





PCIE SLOT DECOUPLING



Universal Scientific Industrial Co., Ltd.	
TITLE: Mississippi_uATX PCI EXPRESS SLOT	REV: V0.4
Document Number : <Doc>	
Prepared by : Kerry Huang	
SIZE : A3	Date: Friday, November 30, 2012
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Slot3
PCIE4X Gen2

BOM NOTE:
POP PCIEX1(53-191003-02) w/o post for H81
NOPOP for NECPC

J10

	B1	+12V_1	PRSNT1-	A1	J10_PRSNT1_N → R1078 0R 0402
	B2	+12V_2	+12V_4	A2	
	B3	+12V_3	+12V_5	A3	
	B4	GND1	GND6	A4	
16,17,22,23,44 SMB_CLK_STBY	B5	SMCLK	JTAG2	A5	PCIE4X_SW_ON_N R290 0R 0402 → SW_ON_N 16,3,39,42,45
16,17,22,23,44 SMB_DATA_STBY	B6	SMDAT	JTAG3	A6	PCIE4X_LAN_OE R284 0R 0402 → LAN_OE 16
	B7	GND2	JTAG4	A7	PCIE4X_LAN_SEL R305 0R 0402 → LAN_SEL 16
	B8	+3.3V_1	JTAG5	A8	PCIE4X_SLP_S3_N R273 0R 0402 → SLP_S3_N 16,19,30,39,42,45,46,48,49,50,51
	B9	JTAG1	+3.3V_2	A9	
	B10	3.3VAUX	+3.3V_3	A10	
16,22,43 WAKE_N → WAKE_N	B11	WAKE-	PERST-	A11	PCIERST_SLOTX4_N → PCIERST_SLOTX4_N 39
		KEY			
	B12	RSVD1	GND7	A12	
13 HSO5_DP → CB197 X7R HSO5_DP_C	B13	GND3	REFCLK+	A13	CK_PE_100M_4PORT_DP 14
13 HSO5_DN → CB198 X7R HSO5_DN_C	B14	PETP0	REFCLK-	A14	CK_PE_100M_4PORT_DN 14
	B15	PETN0	GND8	A15	
	B16	GND4	PERP0	A16	
	B17	PRSNT2-_1	PERN0	A17	HSI5_DP 13
	B18	GND5	GND9	A18	HSI5_DN 13
13 HSO6_DP → CB203 X7R HSO6_DP_C	B19	PETP1	RSVD3	A19	
13 HSO6_DN → CB204 X7R HSO6_DN_C	B20	PETN1	GND16	A20	
	B21	GND10	PERP1	A21	HSI6_DP 13
	B22	GND11	PERN1	A22	HSI6_DN 13
13 HSO7_DP → CB205 X7R HSO7_DP_C	B23	PETP2	GND17	A23	
13 HSO7_DN → CB229 X7R HSO7_DN_C	B24	PETN2	GND18	A24	
	B25	GND12	PERP2	A25	
	B26	GND13	PERN2	A26	HSI7_DP 13
13 HSO8_DP → CB230 X7R HSO8_DP_C	B27	PETP3	GND19	A27	HSI7_DN 13
13 HSO8_DN → CB231 X7R HSO8_DN_C	B28	PETN3	GND20	A28	
	B29	GND14	PERP3	A29	
	B30	RSVD2	PERN3	A30	HSI8_DP 13
	B31	PRSNT2-_2	GND21	A31	HSI8_DN 13
	B32	GND15	RSVD4	A32	
	B33	PETP4	RSVD5	A33	
	B34	PETN4	GND30	A34	
	B35	GND22	PERP4	A35	
	B36	GND23	PERN4	A36	
	B37	PETP5	GND31	A37	
	B38	PETN5	GND32	A38	
	B39	GND24	PERP5	A39	
	B40	GND25	PERN5	A40	
	B41	PETP6	GND33	A41	
	B42	PETN6	GND34	A42	
	B43	GND26	PERP6	A43	
	B44	GND27	PERN6	A44	
	B45	PETP7	GND35	A45	
	B46	PETN7	GND36	A46	
	B47	GND28	PERP7	A47	
	B48	PRSNT2-_3	PERN7	A48	
	B49	GND29	GND37	A49	
	B50	PETP8	RSVD7	A50	
	B51	PETN8	GND53	A51	
	B52	GND38	PERP8	A52	
	B53	GND39	PERN8	A53	
	B54	PETP9	GND54	A54	
	B55	PETN9	GND55	A55	
	B56	GND40	PERP9	A56	
	B57	GND41	PERN9	A57	
	B58	PETP10	GND56	A58	
	B59	PETN10	GND57	A59	
	B60	GND42	PERP10	A60	
	B61	GND43	PERN10	A61	
	B62	PETP11	GND58	A62	
	B63	PETN11	GND59	A63	
	B64	GND44	PERP11	A64	
	B65	GND45	PERN11	A65	
	B66	PETP12	GND60	A66	
	B67	PETN12	GND61	A67	
	B68	GND46	PERP12	A68	
	B69	GND47	PERN12	A69	
	B70	PETP13	GND62	A70	
	B71	PETN13	GND63	A71	
	B72	GND48	PERP13	A72	
	B73	GND49	PERN13	A73	
	B74	PETP14	GND64	A74	
	B75	PETN14	GND65	A75	
	B76	GND50	PERP14	A76	
	B77	GND51	PERN14	A77	
	B78	PETP15	GND66	A78	
	B79	PETN15	GND67	A79	
	B80	GND52	PERP15	A80	
	B81	PRSNT2-_4	PERN15	A81	
	B82	RSVD6	GND68	A82	

PCIE_X16

VCC3 — CB266 — VCC5
(1365.00 -2247)
STITCHING CAP

PCIERST_SLOTX4_N → C304 100PF_50V_NPO

SB3V: CE15 100UF_25V (D5P2.0), C293 0.1UF_16V_Y5V
+12V: C290 0.1UF_16V_Y5V
VCC3: C303 0.1UF_16V_Y5V

BOM NOTE: FOR Tel Aviv(B85),Changbanpo FO(B85),NECPC(B85)
POP PCIEX1 Slot

16 BT_DISABLE_N → R145 0R 0402 → BT_DISABLE_R_N

Slot2
PCIE1X Gen2

J12

	B1	+12V_1	PRSNT1-	A1	J12_A1 R137 0R 0402
	B2	+12V_2	+12V_4	A2	
	B3	+12V_3	+12V_5	A3	
	B4	GND1	GND6	A4	
16,17,22,23,44 SMB_CLK_STBY	B5	SMCLK	JTAG2	A5	CLINK_CLK_WLAN 15
16,17,22,23,44 SMB_DATA_STBY	B6	SMDAT	JTAG3	A6	
	B7	GND2	JTAG4	A7	BT_DISABLE_R_N
	B8	+3.3V_1	JTAG5	A8	CLINK_DATA_WLAN 15
15 CLINK_RST_WLAN_N	B9	JTAG1	+3.3V_2	A9	
WAKE_N	B10	3.3VAUX	+3.3V_3	A10	
	B11	WAKE-	PERST-	A11	PCIERST_SLOTX1_N 23,39
		KEY			
WLAN_DISABLE_R_N	B12	RSVD	GND7	A12	
13 WLAN_DISABLE_N → R194 0R 0402	B13	GND3	REFCLK+	A13	CK_PE_100M_1PORT_DP 14
PCIEX1_HSO_DP_C	B14	PETP0	REFCLK-	A14	CK_PE_100M_1PORT_DN 14
PCIEX1_HSO_DN_C	B15	PETN0	GND8	A15	
	B16	GND4	PERP0	A16	PCIEX1_HSI_DP
16 WLAN_DETECT_N → R139 0R 0402	B17	PRSNT2-	PERN0	A17	PCIEX1_HSI_DN
WLAN_DETECT_R_N	B18	GND5	GND9	A18	

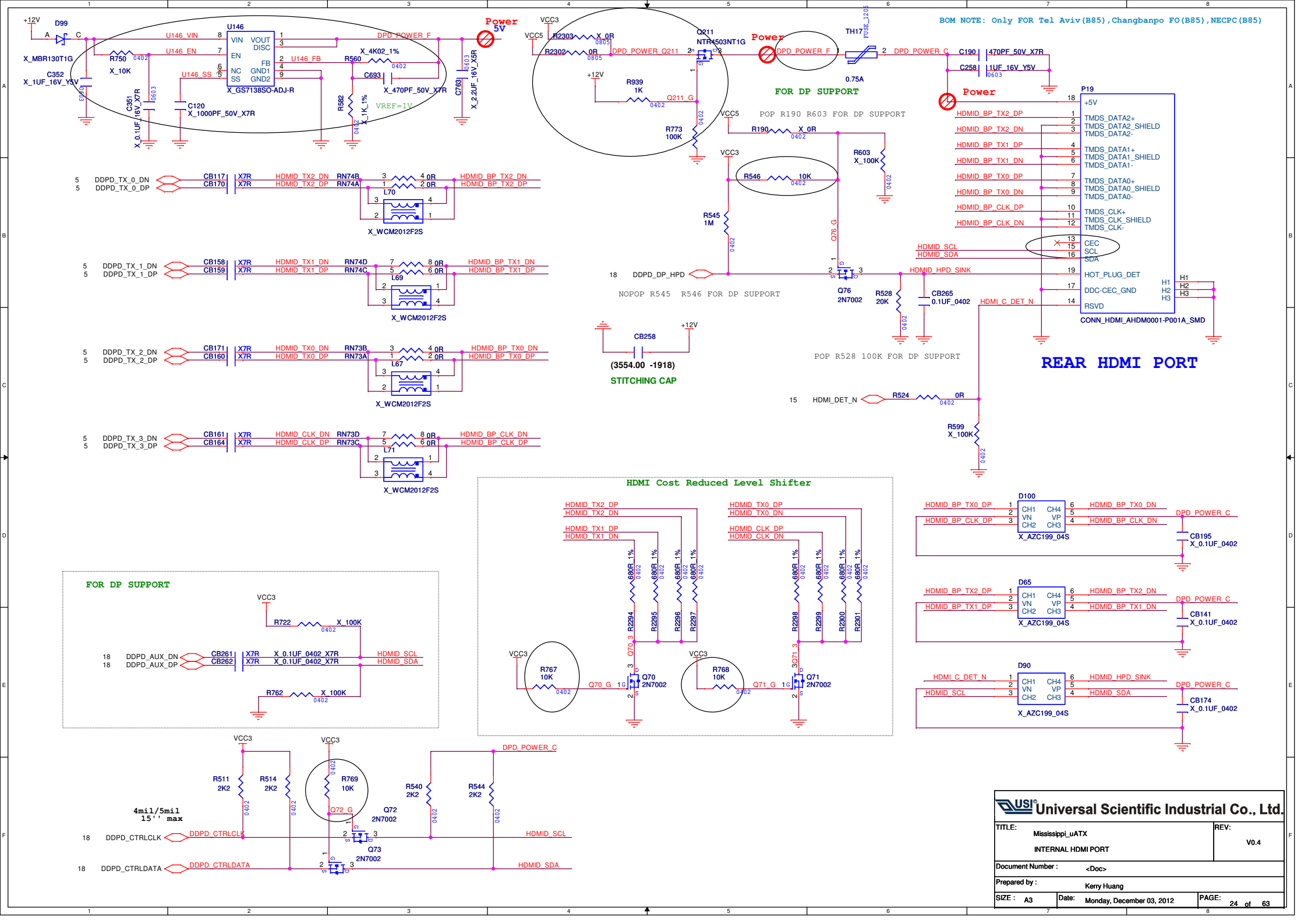
PCIE_X1

13,15 PCIEX1_HSI_DN
13,15 PCIEX1_HSI_DP
15 PCIEX1_HSO_DN
15 PCIEX1_HSO_DP
→ CB155 X7R, CB154 X7R → PCIEX1_HSI_DN, PCIEX1_HSI_DP, PCIEX1_HSO_DN_C, PCIEX1_HSO_DP_C
→ PCIEX1_HSO_DN_C 13, PCIEX1_HSO_DP_C 13

BOM NOTE: FOR Tel Aviv(B85),Changbanpo FO(B85),NECPC(B85)
NOPOP CB154 CB155

23,39 PCIERST_SLOTX1_N → PCIERST_SLOTX1_N → C310 100PF_50V_NPO

Universal Scientific Industrial Co., Ltd.	
TITLE: Mississippi_uATX PCIE X16 (X4) &X1 SLOT	REV: V0.4
Document Number : <Doc>	
Prepared by : Kerry Huang	
SIZE : A3	Date: Friday, November 30, 2012
PAGE: 23 of 63	


BOM NOTE: Only FOR Tel Aviv(B85),Changbanpo FO(B85),NECPC(B85)
REAR HDMI PORT
FOR DP SUPPORT
HDMI Cost Reduced Level Shifter
NOPOP R545 R546 FOR DP SUPPORT
POP R190 R603 FOR DP SUPPORT
POP R528 100K FOR DP SUPPORT
STITCHING CAP
(3554.00 -1918)
CONN_HDMI_AHDM0001-P001A_SMD
Universal Scientific Industrial Co., Ltd.
TITLE: Mississippi_uATX
INTERNAL HDMI PORT
REV: V0.4
Document Number : <Doc>
Prepared by : Kerry Huang
SIZE : A3
Date: Monday, December 03, 2012
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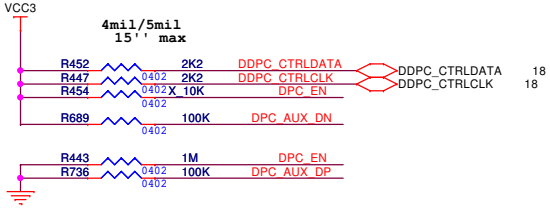
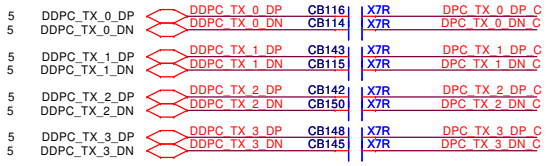
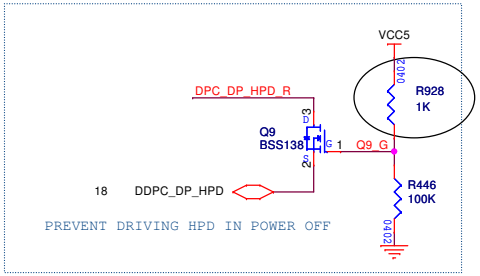
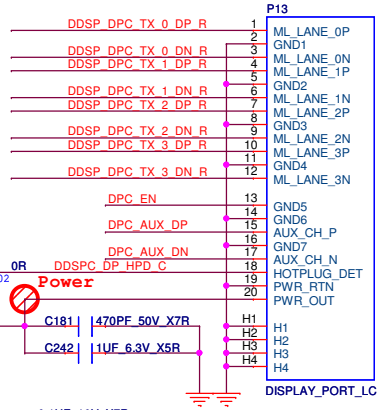
BOM NOTE: For Thunderbolt(C226)
Nopop DP1

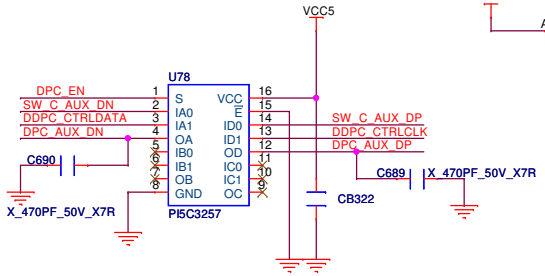
REAR DISPLAY PORT
DP2

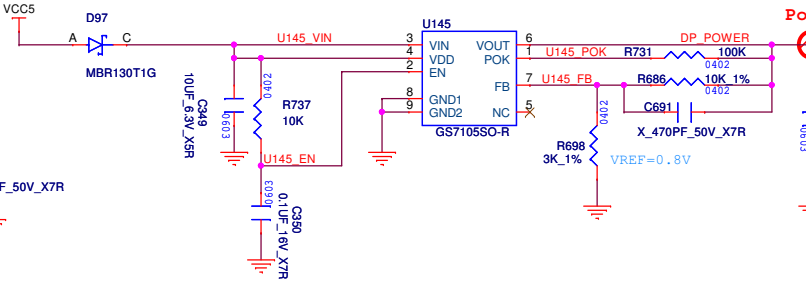


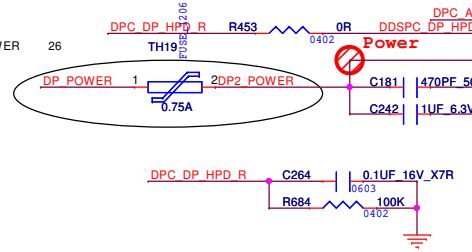






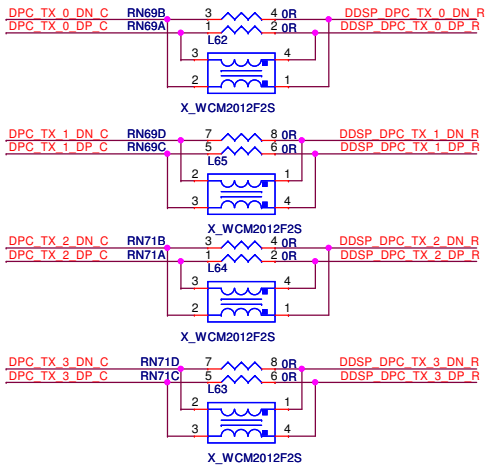


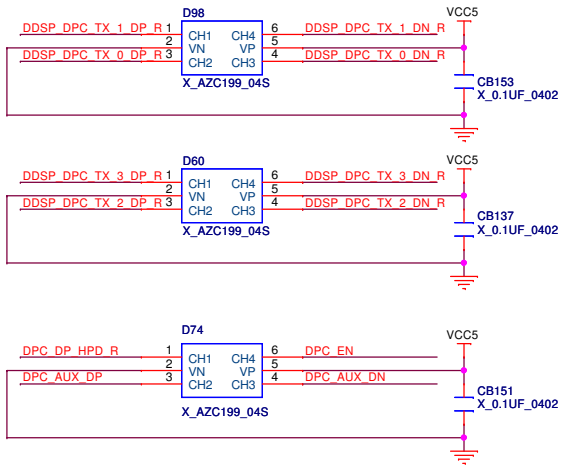




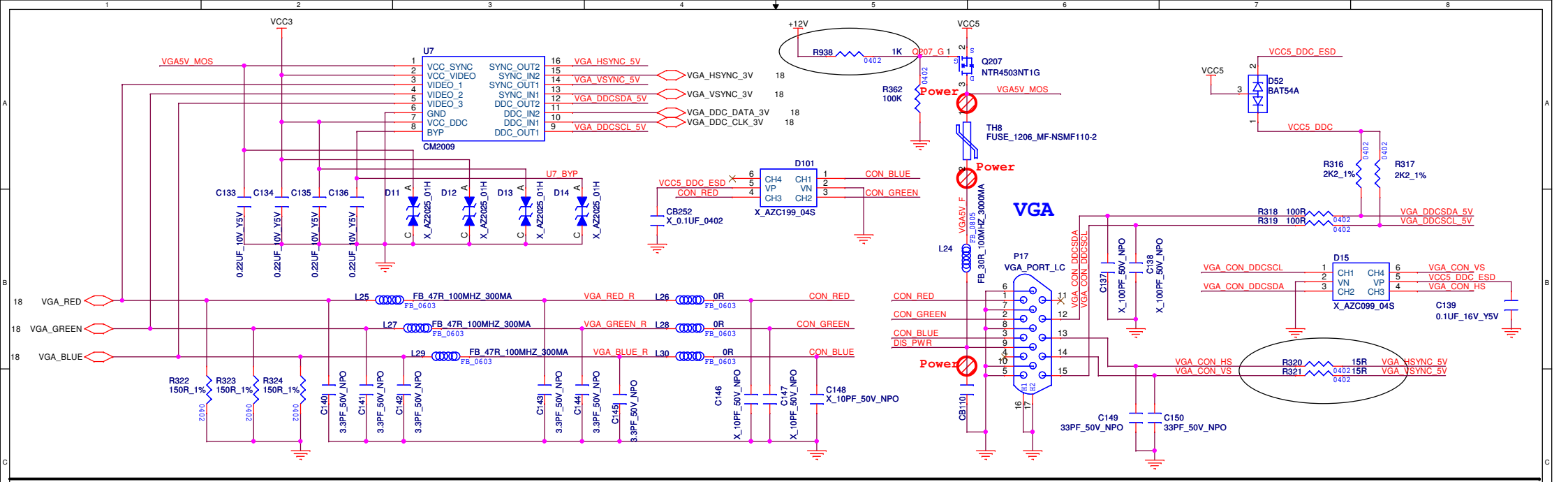
For DP to HDMI dongle

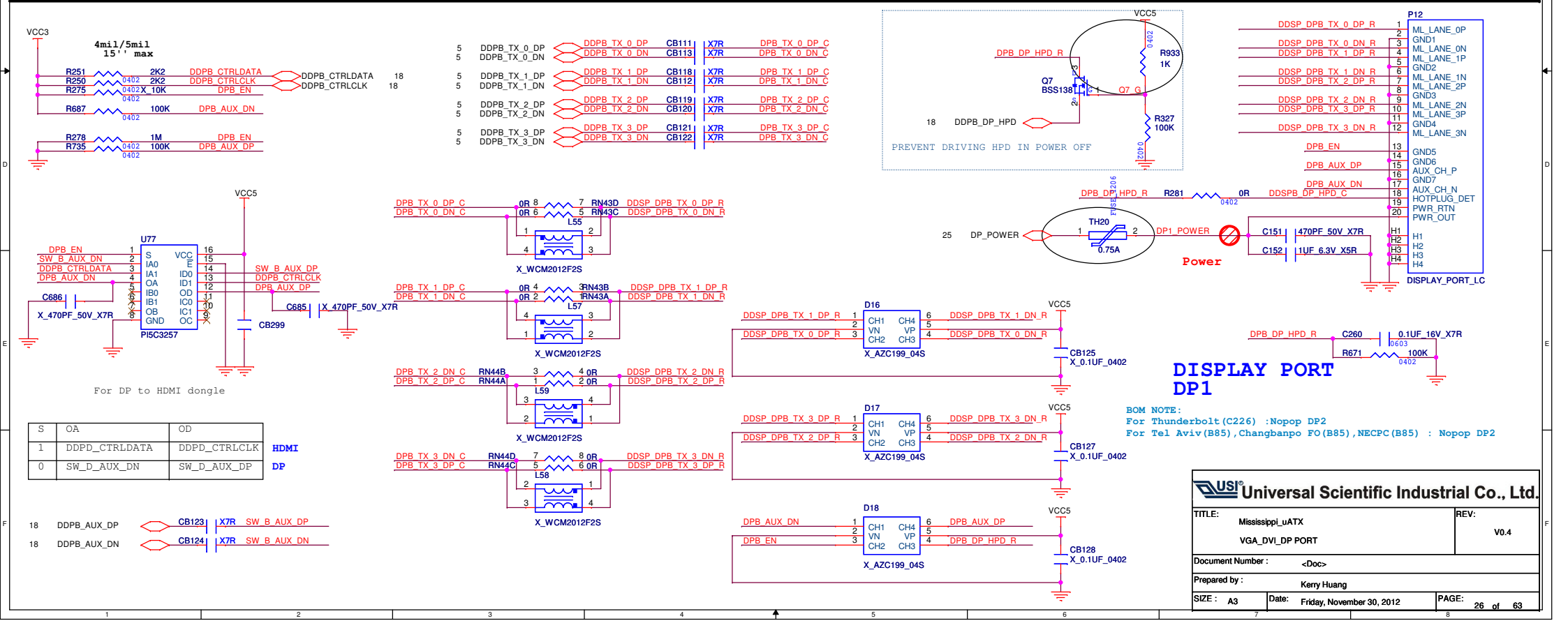
S	OA	OD	
1	DDPD_CTRLDATA	DDPD_CTRLCLK	HDMI
0	SW_D_AUX_DN	SW_D_AUX_DP	DP





Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX REAR DP			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Friday, November 30, 2012		PAGE: 25 of 63


VGA
U7
CM2009
VGA5V_MOS
VGA_HSYNC_5V
VGA_VSYNC_5V
VGA_DDCSDA_5V
VGA_DDCSCL_5V
VGA_HSYNC_3V
VGA_VSYNC_3V
VGA_DDC_DATA_3V
VGA_DDC_CLK_3V
U7_BYP
D101
X_AZC199_04S
CON_BLUE
CON_GREEN
CON_RED
CB252
X_0.1UF_0402
Q207
NTR4503NT1G
R938
1K
R362
100K
TH8
FUSE_1206_MF-NSMF110-2
Power
D52
BAT54A
VCC5_DDC_ESD
VCC5_DDC
R316
2K2_1%
R317
2K2_1%
R318 100R
R319 100R
L24
FB_30R_100MHZ_3000MA
P17
VGA_PORT_LC
C137
X_100PF_50V_NPO
C138
X_100PF_50V_NPO
D15
X_AZC099_04S
C139
0.1UF_16V_Y5V
VGA_CON_DDCSCL
VGA_CON_DDCSDA
VGA_CON_HS
VGA_CON_VS
R320
15R
R321
15R
C149
33PF_50V_NPO
C150
33PF_50V_NPO
CB110
VGA_RED
VGA_GREEN
VGA_BLUE
L25
L26
L27
L28
L29
L30
FB_47R_100MHZ_300MA
0R
VGA_RED_R
VGA_GREEN_R
VGA_BLUE_R
R322
150R_1%
R323
150R_1%
R324
150R_1%
C140
C141
C142
C143
C144
C145
C146
C147
C148
3.3PF_50V_NPO
X_10PF_50V_NPO
X_10PF_50V_NPO
X_10PF_50V_NPO
C133
C134
C135
C136
0.22UF_10V_Y5V
D11
D12
D13
D14
X_AZ2025_01H


DISPLAY PORT
DP1
BOM NOTE:
For Thunderbolt(C226) :Nopop DP2
For Tel Aviv(B85),Changbanpo FO(B85),NECPC(B85) : Nopop DP2
For DP to HDMI dongle
PREVENT DRIVING HPD IN POWER OFF
4mil/5mil
15'' max
U77
PI5C3257
X_WCM2012F2S
D16
D17
D18
X_AZC199_04S
P12
DISPLAY_PORT_LC
TH20
0.75A
DDPB_CTRLDATA
DDPB_CTRLCLK
DDPB_AUX_DN
DDPB_AUX_DP
DDPB_DP_HPD
DPB_DP_HPD_R
DP_POWER
DP1_POWER
SW_B_AUX_DP
SW_B_AUX_DN
DDPB_TX_0_DP
DDPB_TX_0_DN
DDPB_TX_1_DP
DDPB_TX_1_DN
DDPB_TX_2_DP
DDPB_TX_2_DN
DDPB_TX_3_DP
DDPB_TX_3_DN
DDSP_DPB_TX_0_DP_R
DDSP_DPB_TX_0_DN_R
DDSP_DPB_TX_1_DP_R
DDSP_DPB_TX_1_DN_R
DDSP_DPB_TX_2_DP_R
DDSP_DPB_TX_2_DN_R
DDSP_DPB_TX_3_DP_R
DDSP_DPB_TX_3_DN_R
DDSPB_DP_HPD_C
DPB_TX_0_DP_C
DPB_TX_0_DN_C
DPB_TX_1_DP_C
DPB_TX_1_DN_C
DPB_TX_2_DP_C
DPB_TX_2_DN_C
DPB_TX_3_DP_C
DPB_TX_3_DN_C
DPB_EN
DPB_AUX_DP
DPB_AUX_DN
HDMI
DP
Universal Scientific Industrial Co., Ltd.
TITLE:
Mississippi_uATX
VGA_DVI_DP PORT
REV:
V0.4
Document Number :
<Doc>
Prepared by :
Kerry Huang
SIZE : A3
Date: Friday, November 30, 2012
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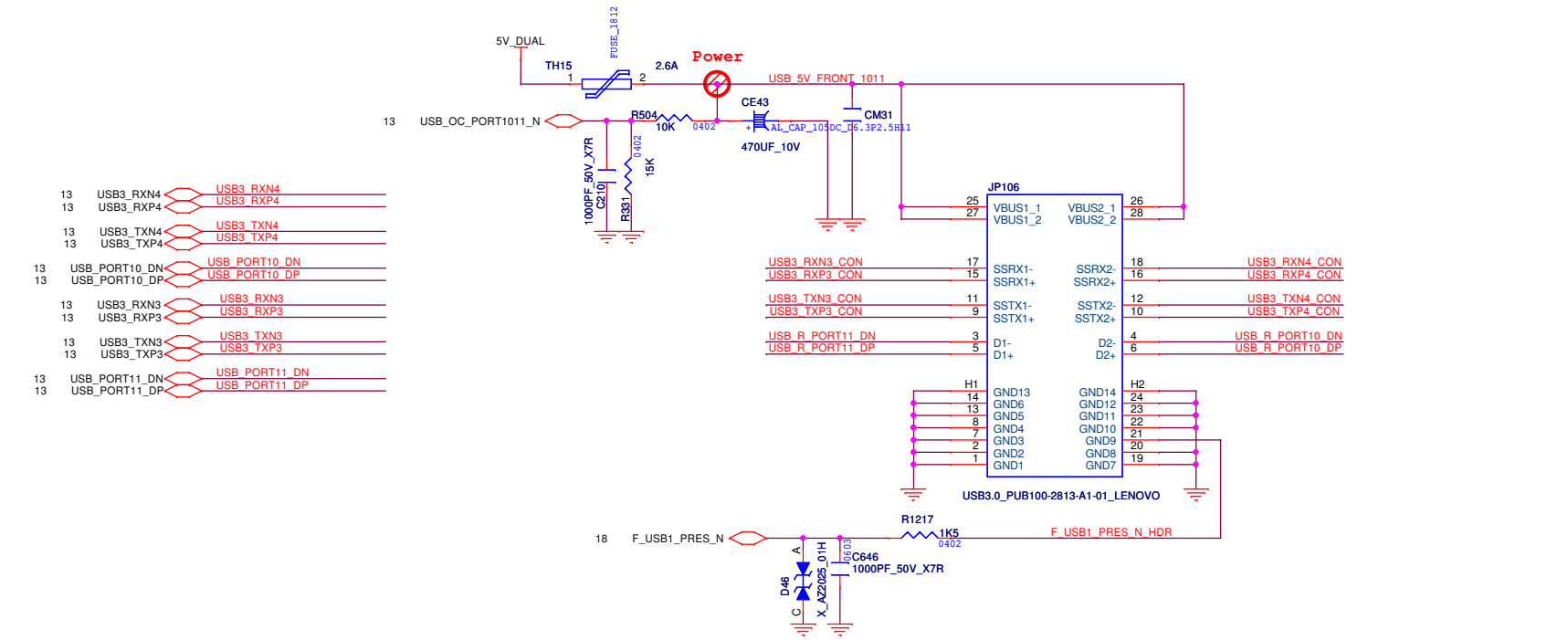
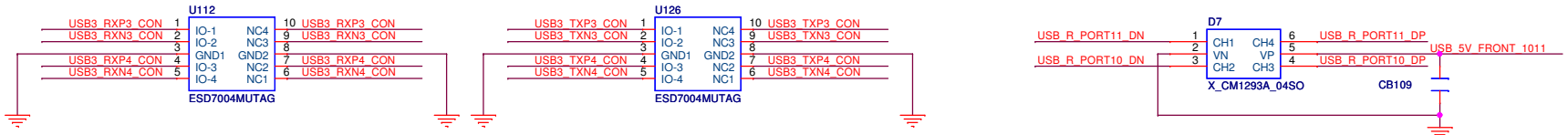
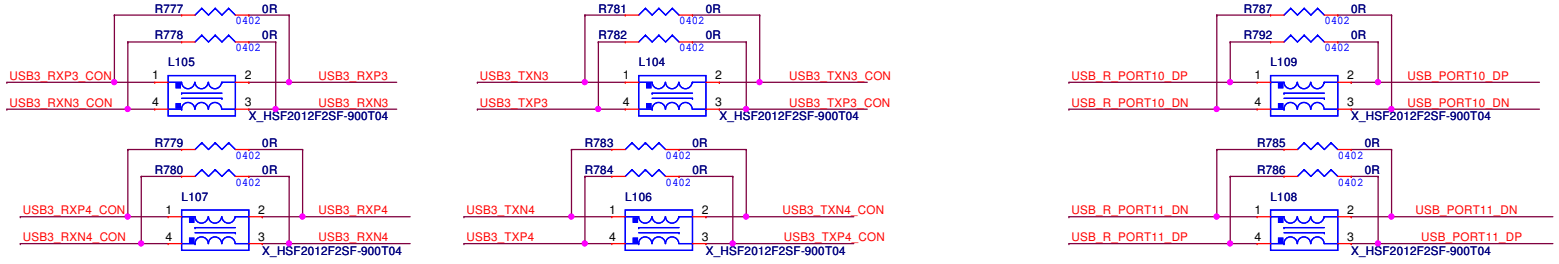
FRONT USB 10,11 PORT

F_USB3.0 HEADER







Universal Scientific Industrial Co., Ltd.	
TITLE: Mississippi_uATX F_USB3.0	REV: V0.4
Document Number : <Doc>	
Prepared by : Kerry Huang	
SIZE : A3	Date: Friday, November 30, 2012
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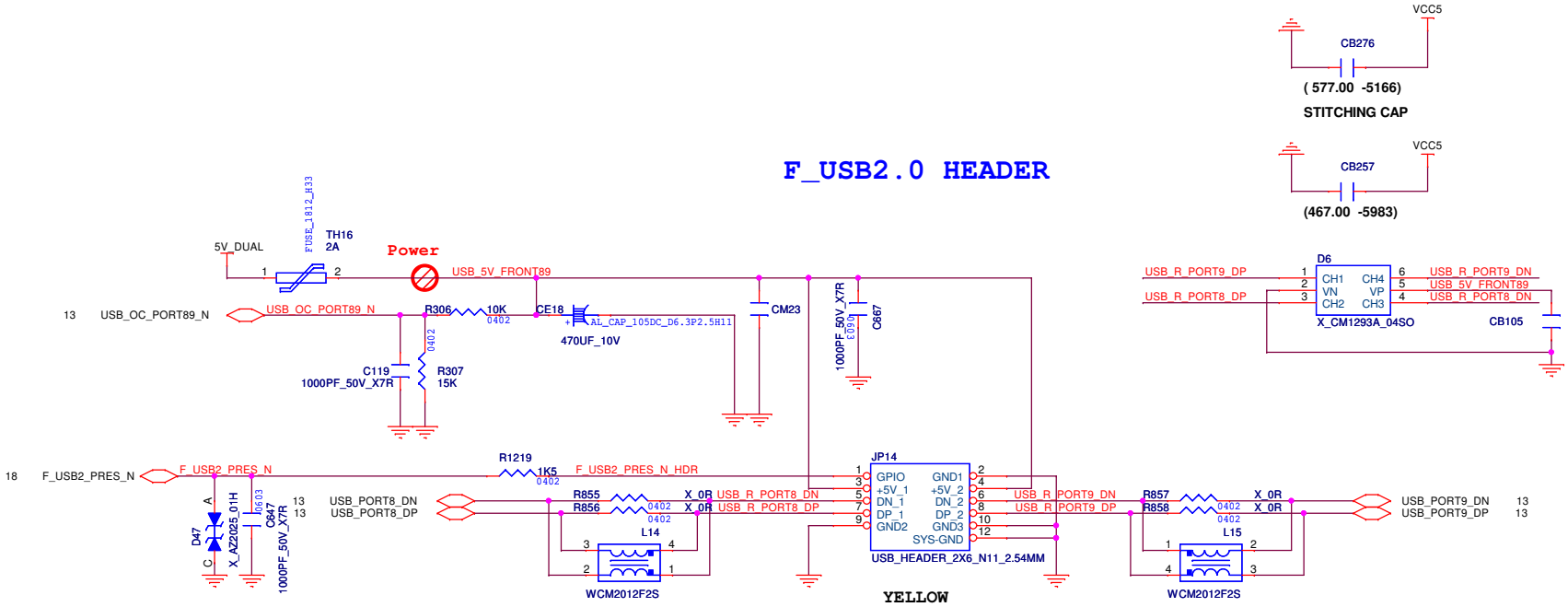
Universal Scientific Industrial Co., Ltd.		
TITLE: Mississippi_uATX BLANK		REV: V0.4
Document Number : <Doc>		
Prepared by : Kerry Huang		
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 28 of 63

FRONT USB 8,9 PORT

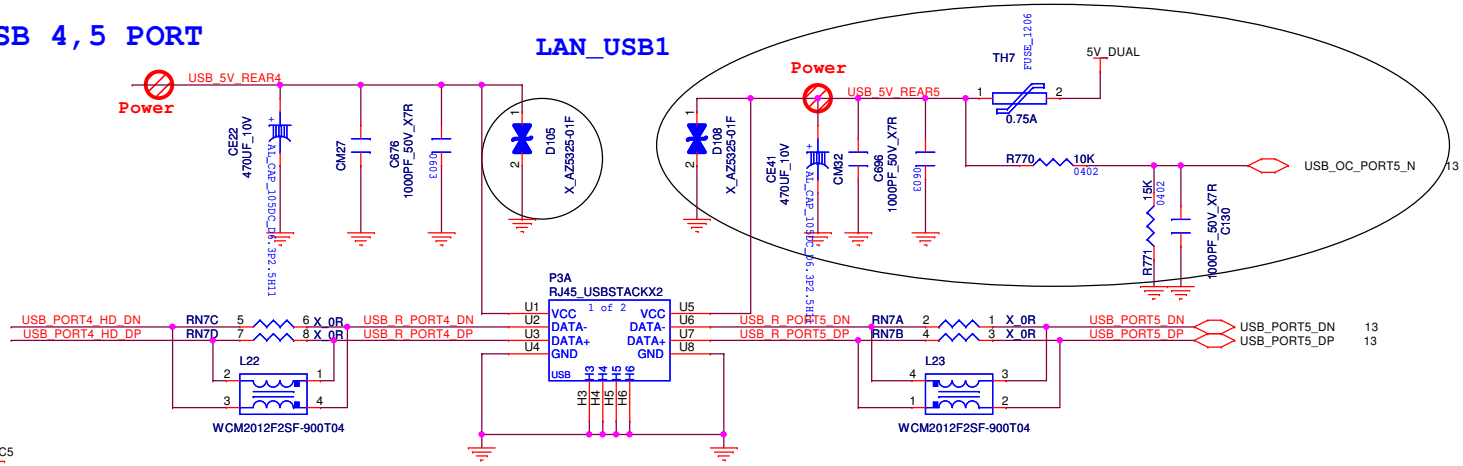
F_USB2.0 HEADER

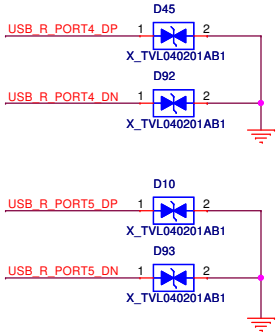


Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX F_USB2.0			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 29 of 63	

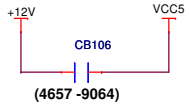
REAR USB 4,5 PORT

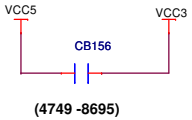
LAN_USB1

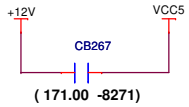


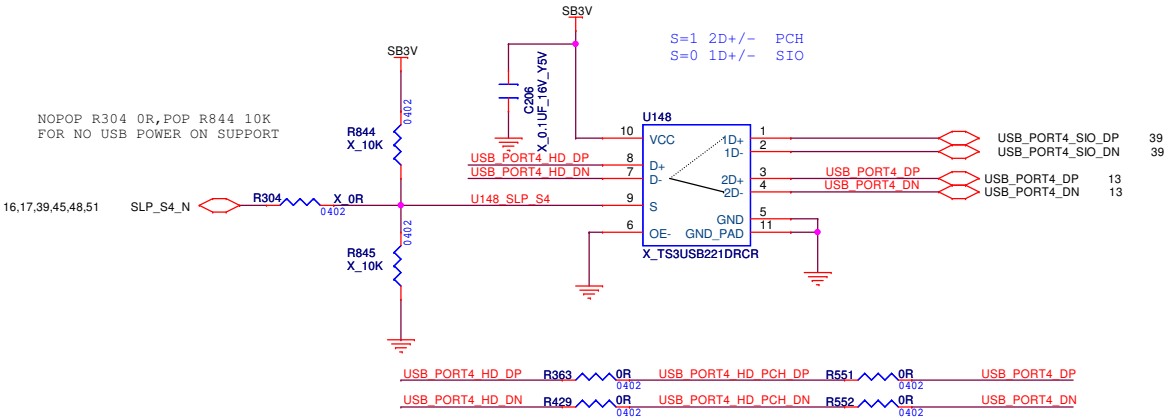


STITCHING CAP

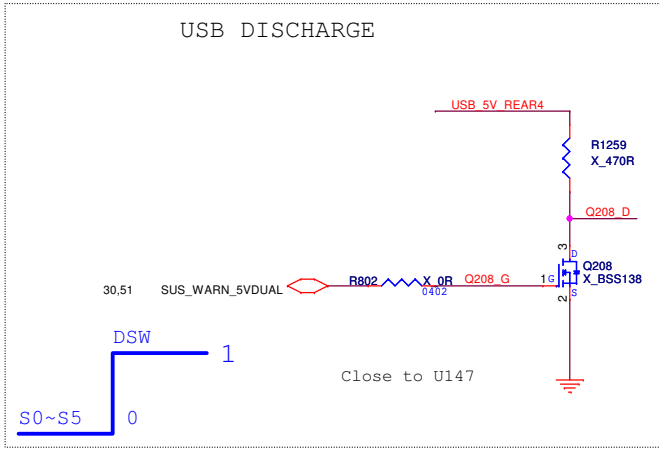






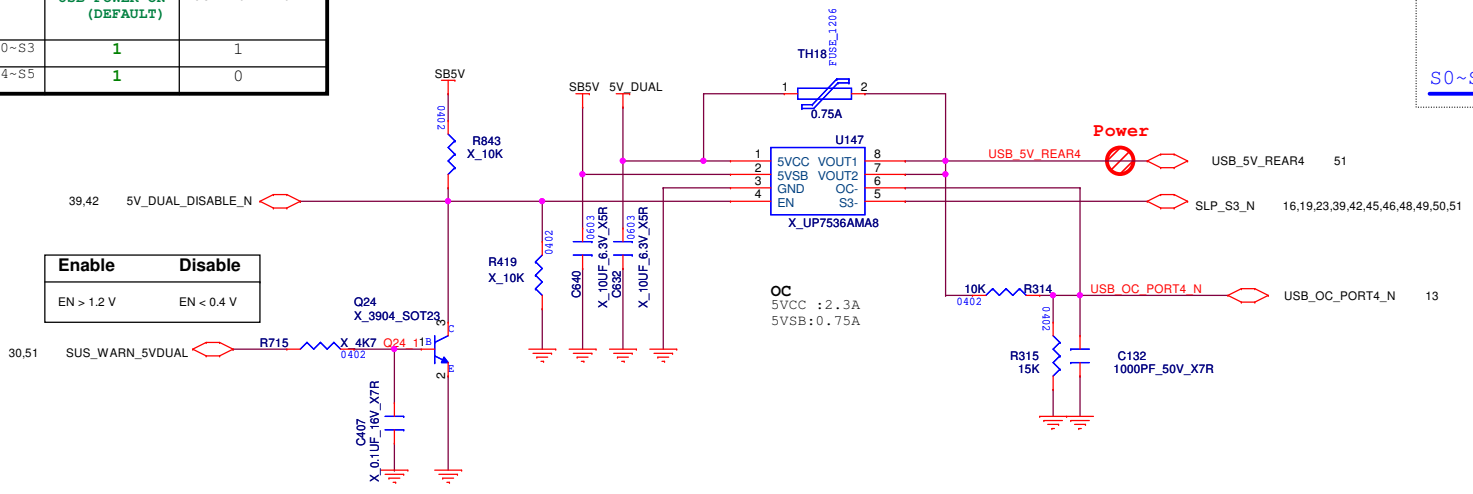


USB DISCHARGE



5V_DUAL_DISABLE_N

	Enable USB POWER ON (DEFAULT)	Disable USB POWER ON
S0~S3	1	1
S4~S5	1	0



Universal Scientific Industrial Co., Ltd.		
TITLE: Mississippi_uATX REAR USB2.0 PORT		REV: V0.4
Document Number : <Doc>		
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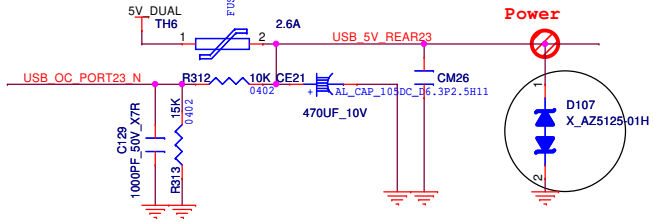
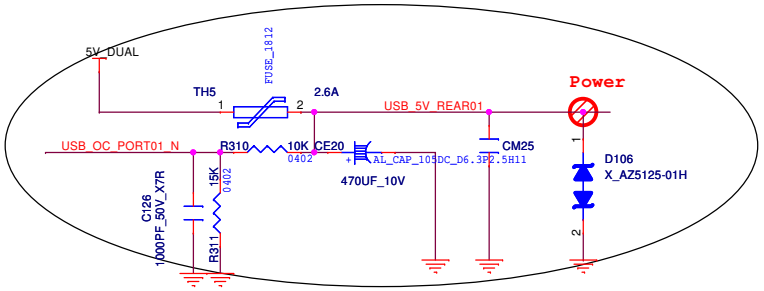
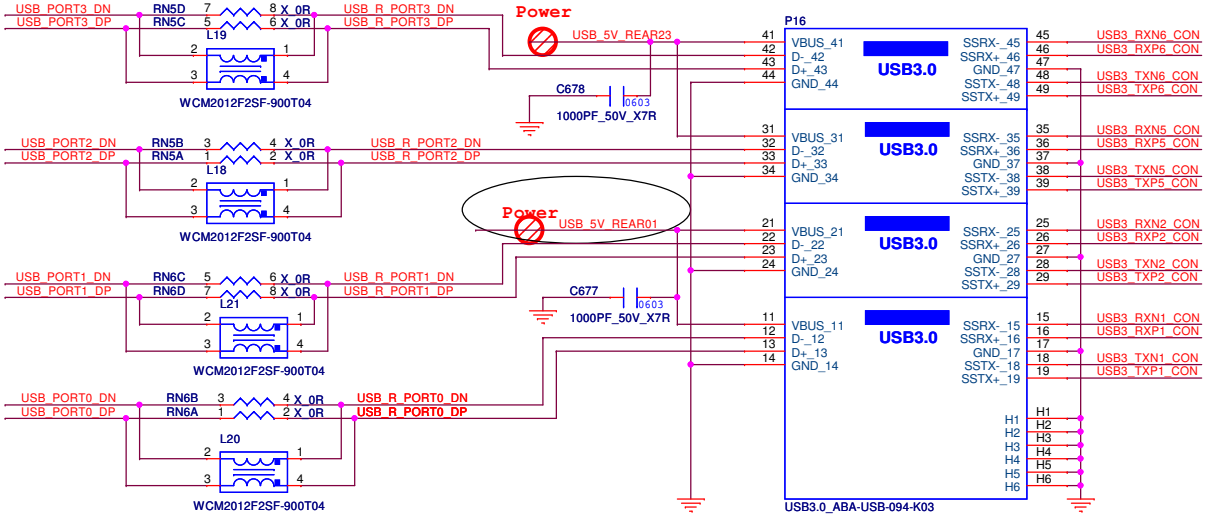
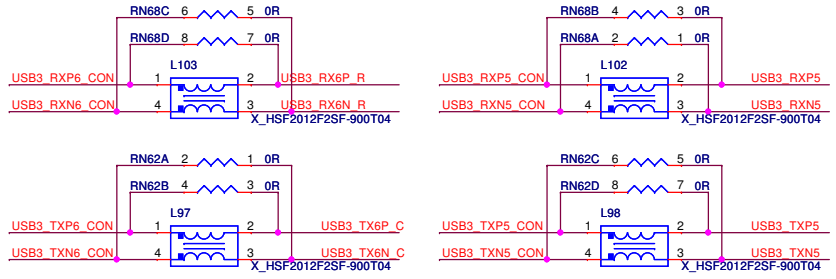
REAR USB3.0 X 4

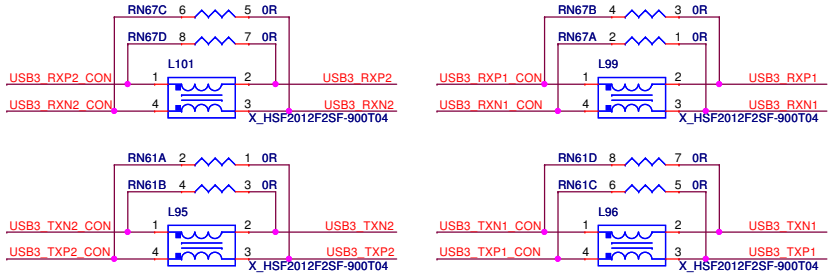
BOM NOTE:
Change to 2*USB3.0+2*USB2.0 for Minsk,Turin ,Changbanpo,NECPC(B85)
Change to 2*USB3.0 for H81,NECPC

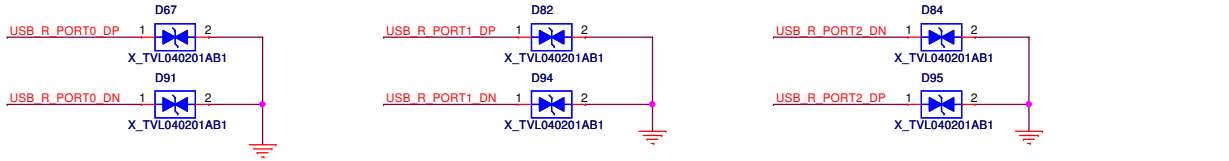


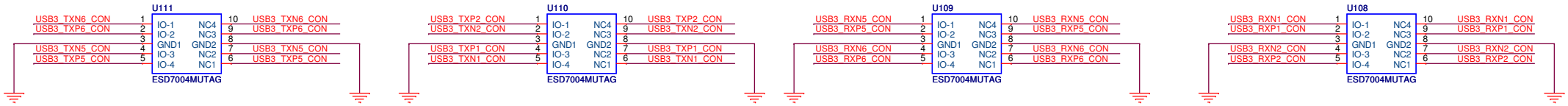












13 USB3_RXN5 → USB3_RXN5
13 USB3_RXP5 → USB3_RXP5
13 USB3_TXN5 → USB3_TXN5
13 USB3_TXP5 → USB3_TXP5

13 USB3_RX6N_R → USB3_RX6N_R
13 USB3_RX6P_R → USB3_RX6P_R
13,31 USB3_TX6N_C → USB3_TX6N_C
13,31 USB3_TX6P_C → USB3_TX6P_C

13 USB3_RXN1 → USB3_RXN1
13 USB3_RXP1 → USB3_RXP1
13 USB3_TXN1 → USB3_TXN1
13 USB3_TXP1 → USB3_TXP1

13 USB3_RXN2 → USB3_RXN2
13 USB3_RXP2 → USB3_RXP2
13 USB3_TXN2 → USB3_TXN2
13 USB3_TXP2 → USB3_TXP2

13 USB_OC_PORT23_N → USB_OC_PORT23_N
13 USB_PORT2_DN → USB_PORT2_DN
13 USB_PORT2_DP → USB_PORT2_DP
13 USB_PORT3_DN → USB_PORT3_DN
13 USB_PORT3_DP → USB_PORT3_DP

13 USB_OC_PORT01_N → USB_OC_PORT01_N
13 USB_PORT0_DN → USB_PORT0_DN
13 USB_PORT0_DP → USB_PORT0_DP
13 USB_PORT1_DN → USB_PORT1_DN
13 USB_PORT1_DP → USB_PORT1_DP

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TITLE: Mississippi_uATX REAR USB3.0 PORT	REV: V0.4
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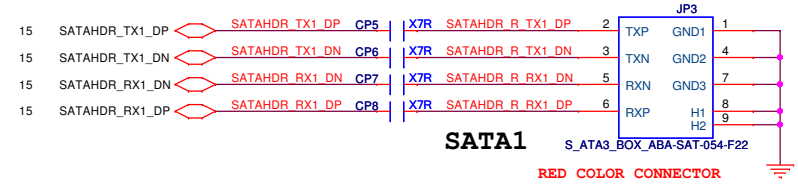
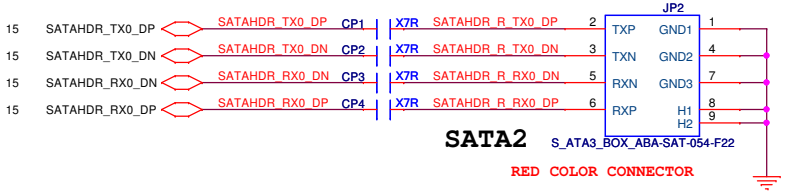
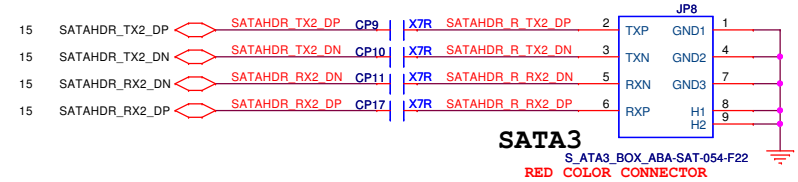
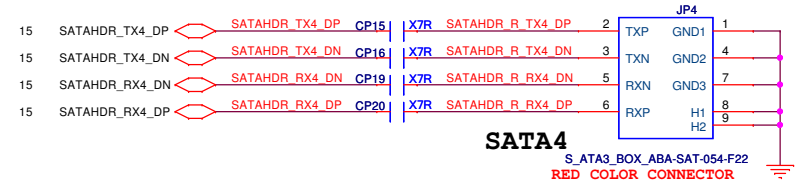
SATA CONN

SATA CONN
SATA 3.0

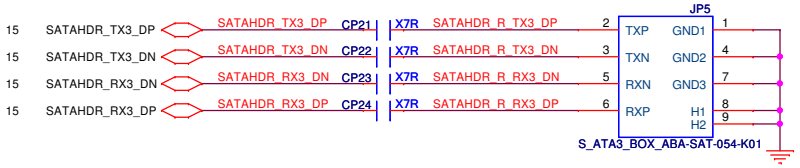


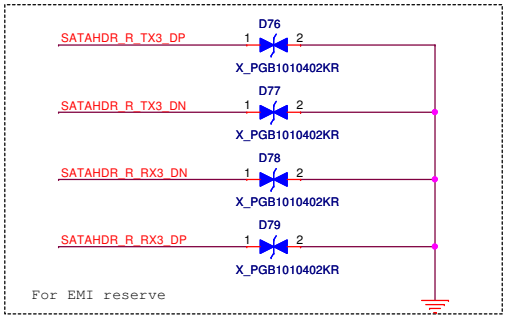






eSATA CONN





Universal Scientific Industrial Co., Ltd.		
TITLE: Mississippi_uATX SATA CONN		REV: V0.4
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BLANK

Universal Scientific Industrial Co., Ltd.		
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ALC662-VC : Stuff R1297 , Empty C196

ALC662-VD : Stuff C196 , Empty R1297

ALC662-VC : Stuff D19 , L31 , CE24 , U9 , D20 CE25 , L32 , CB130

ALC662-VD : Stuff R1295 ,L44 , CE25

AUDIO

DIGITAL AREA

ANALOG AREA

ALC662-VD0-GR

BOM NOTE:
For Thunderbolt(C226) :Nopop Audio Function

F_AUDIO

BUZZER

MONO

	U11_POP	U11_NOPOP
R350	20K_1%	0R
R386	0R	NOPOP
R389	NOPOP	0R

Reserve bypass resistor for amplifier to support cost down opportunity-amplifier on speaker

Universal Scientific Industrial Co., Ltd.	
TITLE: Mississippi_uATX AUDIO CODEC ALC662	REV: V0.4
Document Number : <Doc>	
Prepared by : Kerry Huang	
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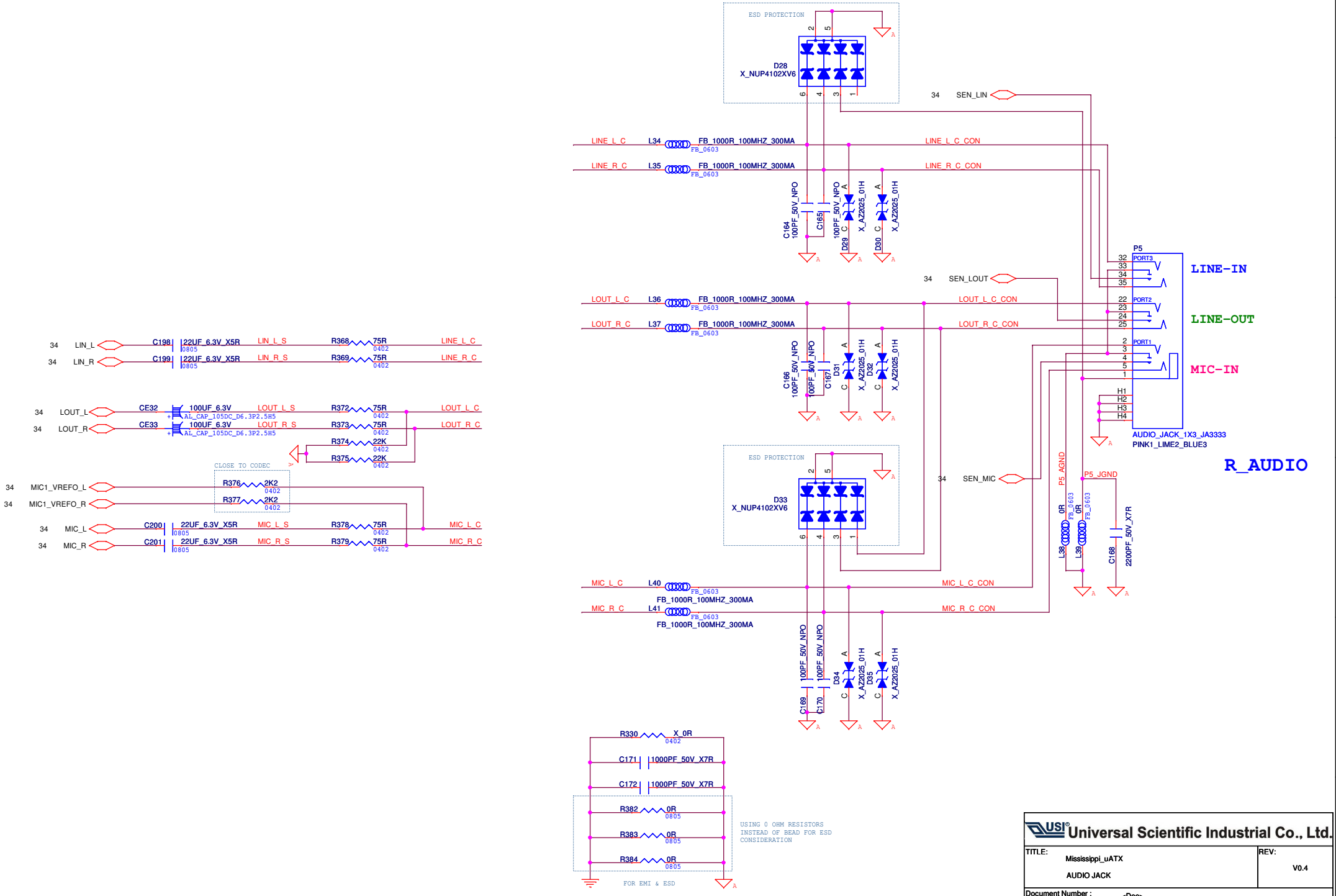
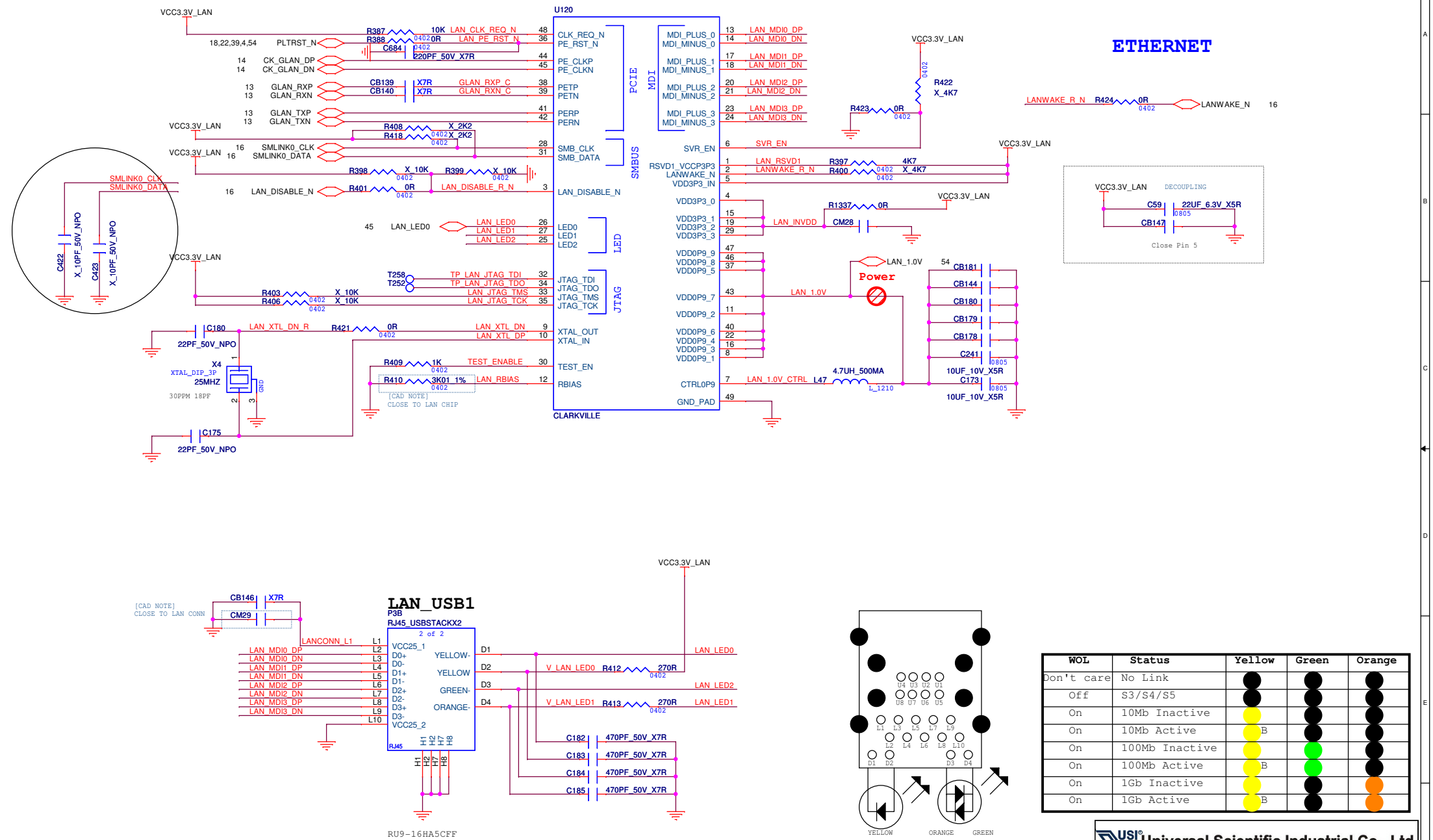


Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX AUDIO JACK			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 35 of 63	



RU9-16HA5CFF
LAN SURGE PROTECT 6KV

WOL	Status	Yellow	Green	Orange
Don't care	No Link			
Off	S3/S4/S5			
On	10Mb Inactive			
On	10Mb Active	B		
On	100Mb Inactive			
On	100Mb Active	B		
On	1Gb Inactive			
On	1Gb Active	B		

Universal Scientific Industrial Co., Ltd.

TITLE: Mississippi_uATX LAN CLARKVILLE		REV: V0.4	
Document Number : <Doc>			
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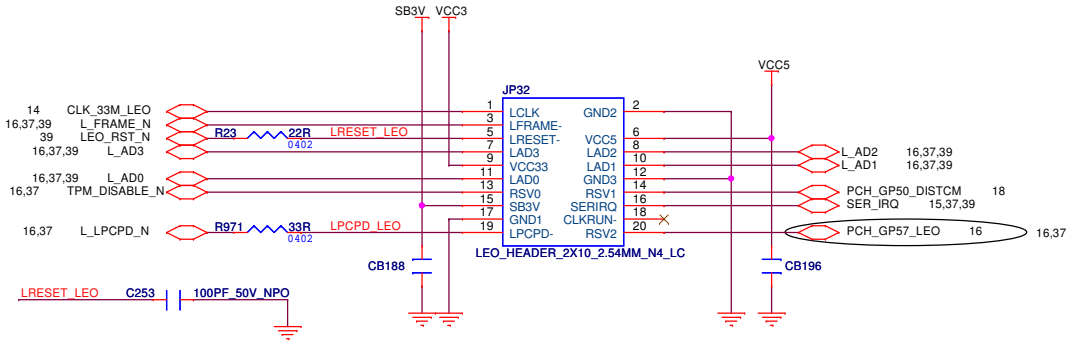
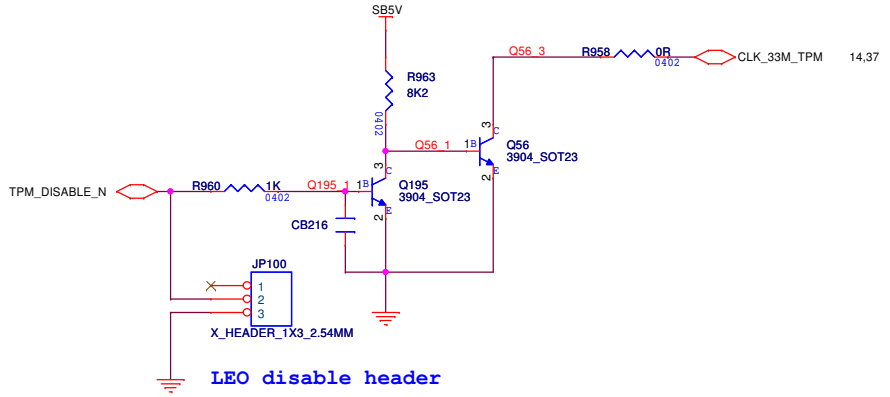
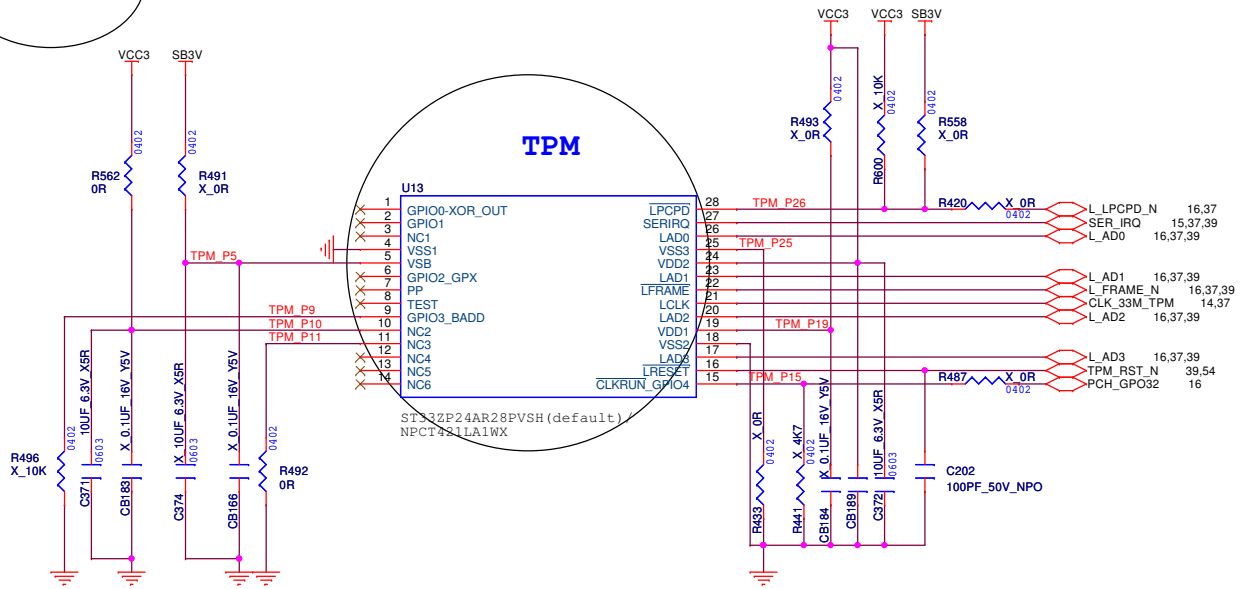
LEO CIRCUIT



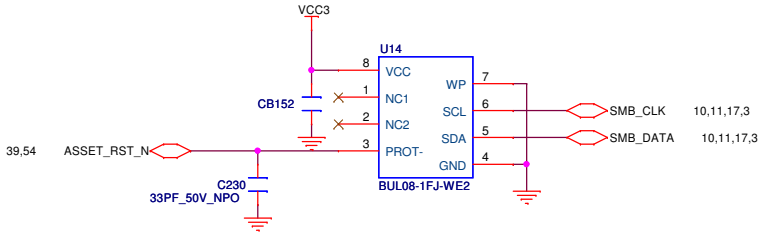


	STUFF	EMPTY
NPCT421LA1WX	R433,R493,R491,C374, CB166,CB189,CB184,C372	R492,R562,CB183 R441,C371,R420,R558,R487
ST33ZP24AR28PVSH (DEFAULT)	R562,CB183,CB189 R492,C372,C371	R491,CB166,C374,R433,R493 ,CB184,R496,R420,R558,R441,R487

TPM



ASSET ID



Universal Scientific Industrial Co., Ltd.	
TITLE: Mississippi_uATX LPT_TPM_ASSET ID	REV: V0.4
Document Number : <Doc>	
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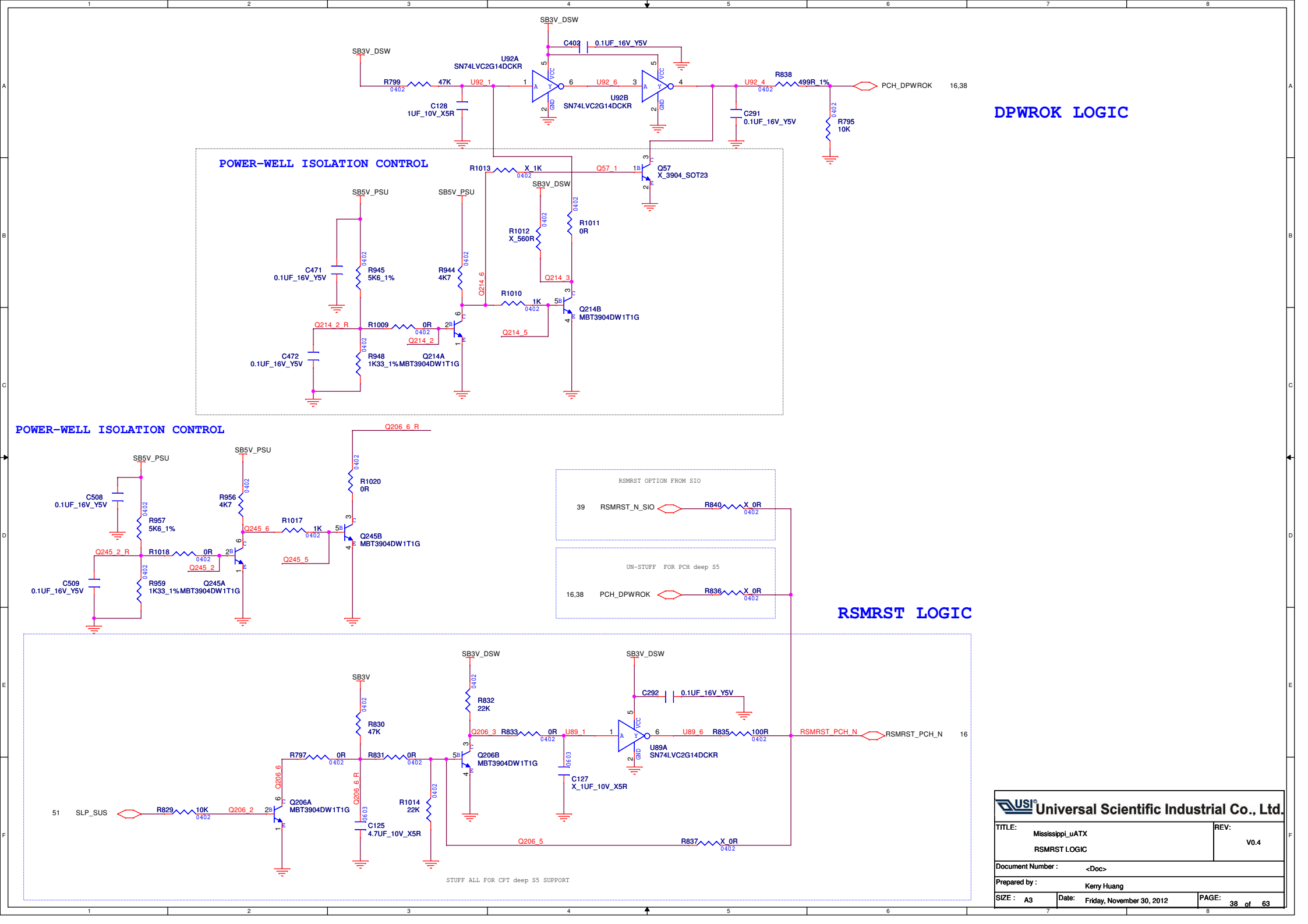
DPWROK LOGIC
POWER-WELL ISOLATION CONTROL
SB3V_DSW
C402 0.1UF_16V_Y5V
U92A SN74LVC2G14DCKR
R799 47K 0402
U92_1
C128 1UF_10V_X5R
U92_6
U92B SN74LVC2G14DCKR
U92_4
R838 499R_1%
PCH_DPWROK 16,38
C291 0.1UF_16V_Y5V
R795 10K
R1013 X_1K
Q57_1
Q57 X_3904_SOT23
SB5V_PSU
C471 0.1UF_16V_Y5V
R945 5K6_1%
R944 4K7
R1012 X_560R
R1011 0R
Q214_6
Q214_3
R1010 1K
Q214B MBT3904DW1T1G
Q214_2_R
R1009 0R
Q214_2
Q214_5
C472 0.1UF_16V_Y5V
R948 1K33_1%
Q214A MBT3904DW1T1G
POWER-WELL ISOLATION CONTROL
Q206_6_R
R1020 0R
R956 4K7
Q245_6
R1017 1K
Q245B MBT3904DW1T1G
C508 0.1UF_16V_Y5V
R957 5K6_1%
Q245_2_R
R1018 0R
Q245_2
Q245_5
C509 0.1UF_16V_Y5V
R959 1K33_1%
Q245A MBT3904DW1T1G
RSMRST OPTION FROM SIO
39 RSMRST_N_SIO
R840 X_0R
UN-STUFF FOR PCH deep S5
16,38 PCH_DPWROK
R836 X_0R
RSMRST LOGIC
SB3V
R830 47K
R832 22K
Q206_3
R833 0R
U89_1
C292 0.1UF_16V_Y5V
U89_6
R835 100R
RSMRST_PCH_N
RSMRST_PCH_N 16
U89A SN74LVC2G14DCKR
C127 X_1UF_10V_X5R
R797 0R
R831 0R
Q206B MBT3904DW1T1G
Q206_6
Q206_6_R
R1014 22K
C125 4.7UF_10V_X5R
51 SLP_SUS
R829 10K
Q206_2
Q206A MBT3904DW1T1G
Q206_5
R837 X_0R
STUFF ALL FOR CPT deep S5 SUPPORT
Universal Scientific Industrial Co., Ltd.
TITLE: Mississippi_uATX
RSMRST LOGIC
REV: V0.4
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Prepared by : Kerry Huang
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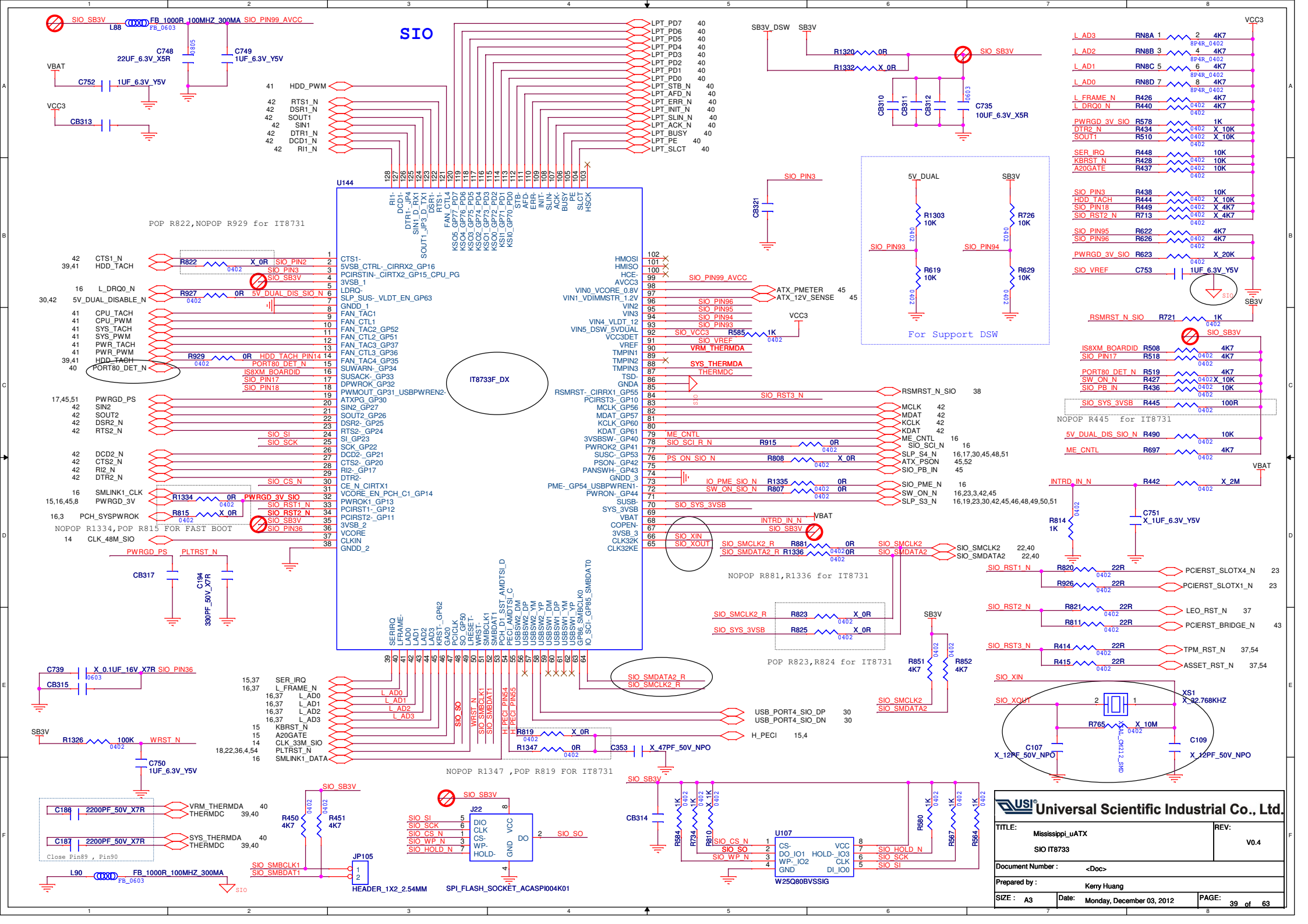
SIO
U144
IT8733F_DX
POP R822,NOPOP R929 for IT8731
NOPOP R1334,POP R815 FOR FAST BOOT
NOPOP R881,R1336 for IT8731
POP R823,R824 for IT8731
NOPOP R1347 ,POP R819 FOR IT8731
NOPOP R445 for IT8731
For Support DSW
Close Pin89 , Pin90
HEADER_1X2_2.54MM
SPI_FLASH_SOCKET_ACASPI004K01
W25Q80BVSSIG
Universal Scientific Industrial Co., Ltd.
TITLE: Mississippi_uATX
SIO IT8733
REV: V0.4
Document Number : <Doc>
Prepared by : Kerry Huang
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Date: Monday, December 03, 2012
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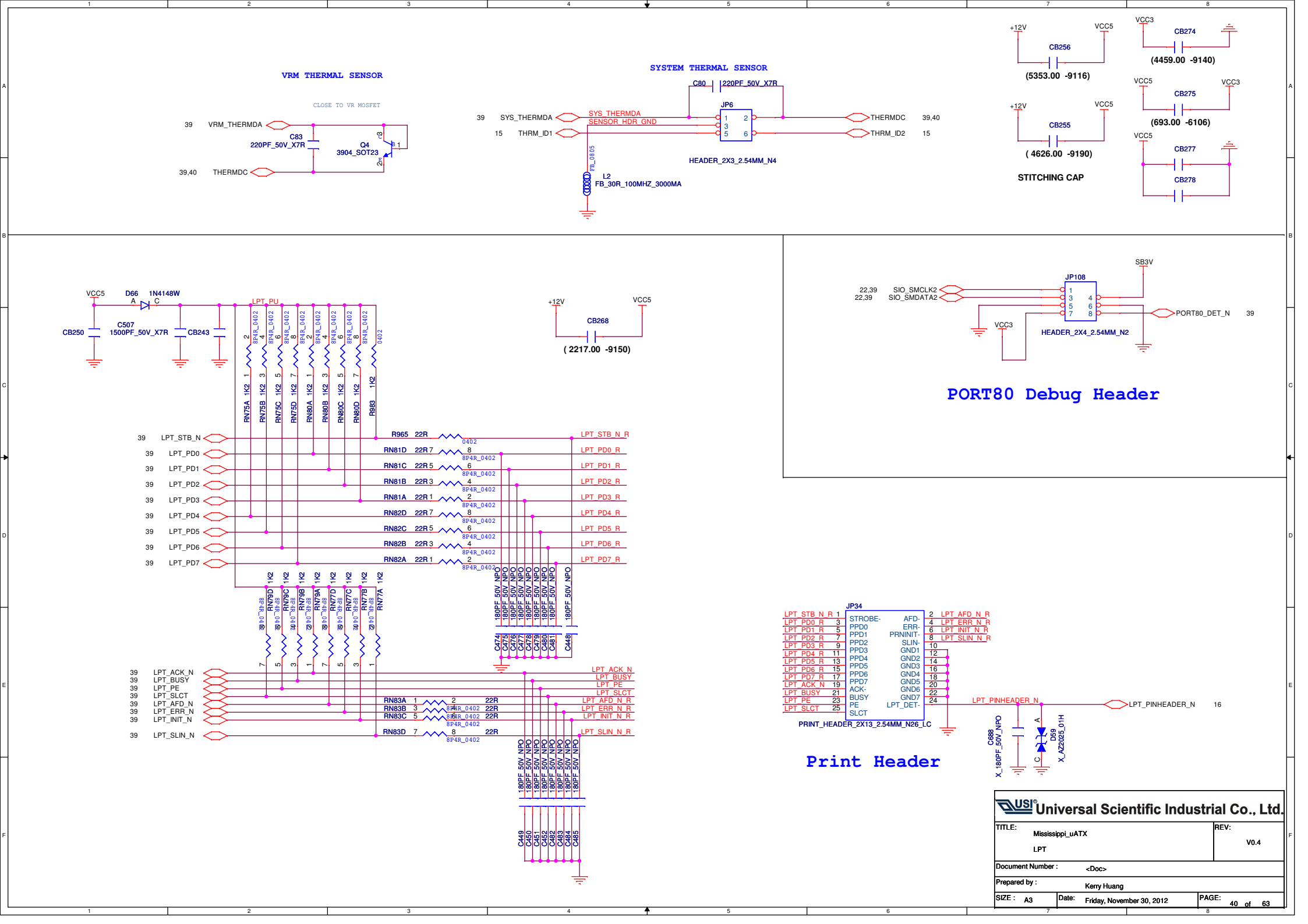
VRM THERMAL SENSOR
CLOSE TO VR MOSFET
39 VRM_THERMDA
C83
220PF_50V_X7R
Q4
3904_SOT23
39,40 THERMDC
SYSTEM THERMAL SENSOR
C80 220PF_50V_X7R
39 SYS_THERMDA
SYS_THERMDA
SENSOR_HDR_GND
JP6
15 THRM_ID1
THERMDC 39,40
THRM_ID2 15
HEADER_2X3_2.54MM_N4
L2
FB_30R_100MHZ_3000MA
+12V
VCC5
CB256
(5353.00 -9116)
VCC3
CB274
(4459.00 -9140)
CB255
(4626.00 -9190)
CB275
(693.00 -6106)
CB277
CB278
STITCHING CAP
VCC5
D66 1N4148W
CB250
C507
1500PF_50V_X7R
CB243
LPT_PU
RN75A 1K2
RN75B 1K2
RN75C 1K2
RN75D 1K2
RN80A 1K2
RN80B 1K2
RN80C 1K2
RN80D 1K2
R983 1K2
CB268
(2217.00 -9150)
39 LPT_STB_N
39 LPT_PD0
39 LPT_PD1
39 LPT_PD2
39 LPT_PD3
39 LPT_PD4
39 LPT_PD5
39 LPT_PD6
39 LPT_PD7
R965 22R
RN81D 22R
RN81C 22R
RN81B 22R
RN81A 22R
RN82D 22R
RN82C 22R
RN82B 22R
RN82A 22R
LPT_STB_N_R
LPT_PD0_R
LPT_PD1_R
LPT_PD2_R
LPT_PD3_R
LPT_PD4_R
LPT_PD5_R
LPT_PD6_R
LPT_PD7_R
180PF 50V NPO
C474
C475
C476
C477
C478
C479
C480
C481
C448
RN79D 1K2
RN79C 1K2
RN79B 1K2
RN79A 1K2
RN77D 1K2
RN77C 1K2
RN77B 1K2
RN77A 1K2
39 LPT_ACK_N
39 LPT_BUSY
39 LPT_PE
39 LPT_SLCT
39 LPT_AFD_N
39 LPT_ERR_N
39 LPT_INIT_N
39 LPT_SLIN_N
RN83A 22R
RN83B 22R
RN83C 22R
RN83D 22R
LPT_ACK_N
LPT_BUSY
LPT_PE
LPT_SLCT
LPT_AFD_N_R
LPT_ERR_N_R
LPT_INIT_N_R
LPT_SLIN_N_R
C449
C450
C451
C452
C482
C483
C484
C485
22,39 SIO_SMCLK2
22,39 SIO_SMDATA2
JP108
SB3V
VCC3
PORT80_DET_N 39
HEADER_2X4_2.54MM_N2
PORT80 Debug Header
LPT_STB_N_R 1
LPT_PD0_R 3
LPT_PD1_R 5
LPT_PD2_R 7
LPT_PD3_R 9
LPT_PD4_R 11
LPT_PD5_R 13
LPT_PD6_R 15
LPT_PD7_R 17
LPT_ACK_N 19
LPT_BUSY 21
LPT_PE 23
LPT_SLCT 25
JP34
STROBE-
PPD0
PPD1
PPD2
PPD3
PPD4
PPD5
PPD6
PPD7
ACK-
BUSY
PE
SLCT
AFD-
ERR-
PRNINIT-
SLIN-
GND1
GND2
GND3
GND4
GND5
GND6
GND7
LPT_DET-
LPT_AFD_N_R 2
LPT_ERR_N_R 4
LPT_INIT_N_R 6
LPT_SLIN_N_R 8
10
12
14
16
18
20
22
24
PRINT_HEADER_2X13_2.54MM_N26_LC
LPT_PINHEADER_N
LPT_PINHEADER_N 16
C688
X_180PF_50V_NPO
D59
X_AZ2025_01H
Print Header
Universal Scientific Industrial Co., Ltd.
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LPT
REV: V0.4
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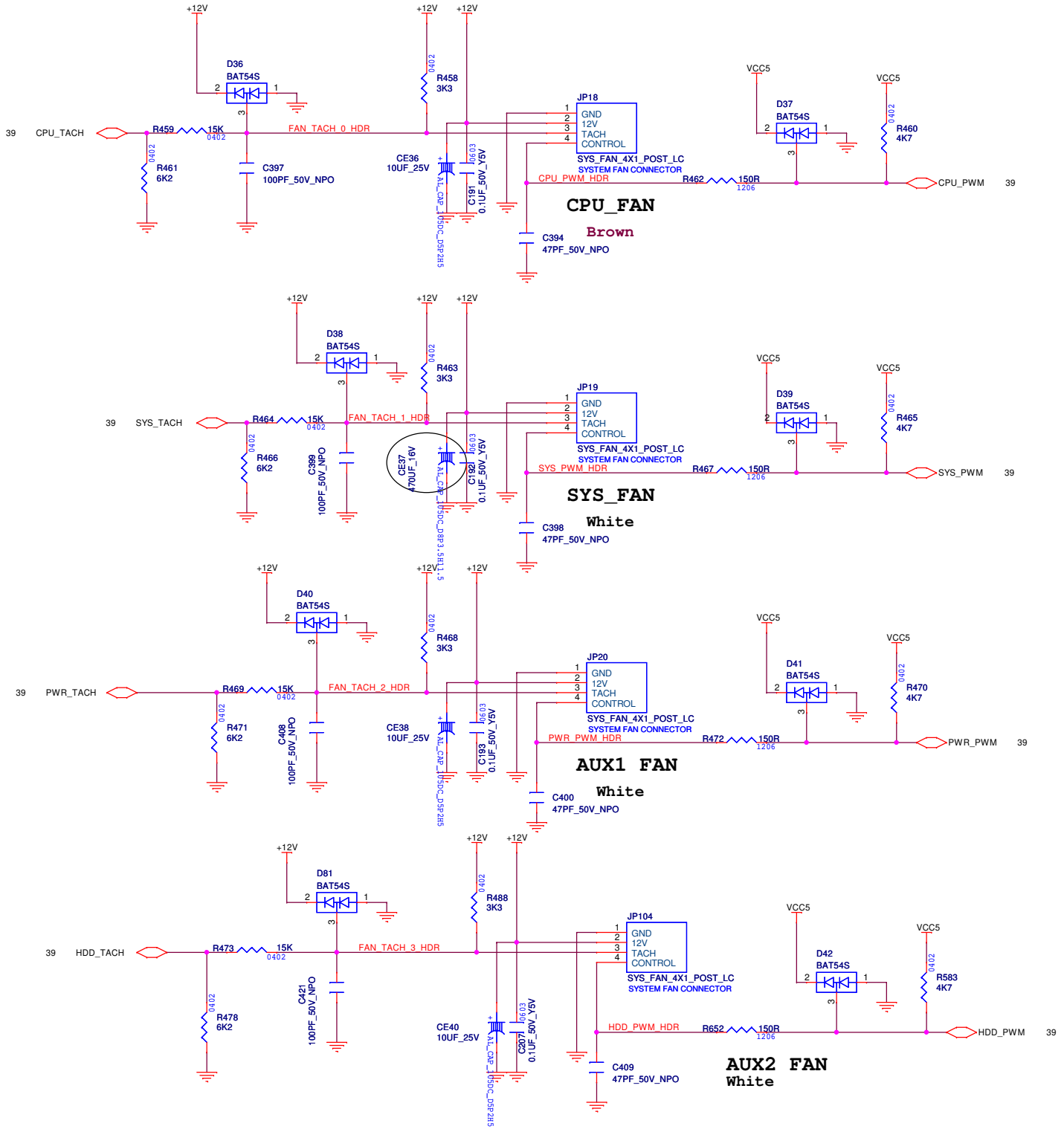

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TITLE: Mississippi_uATX FAN CONNECTOR		REV: V0.4
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Prepared by : Kerry Huang		
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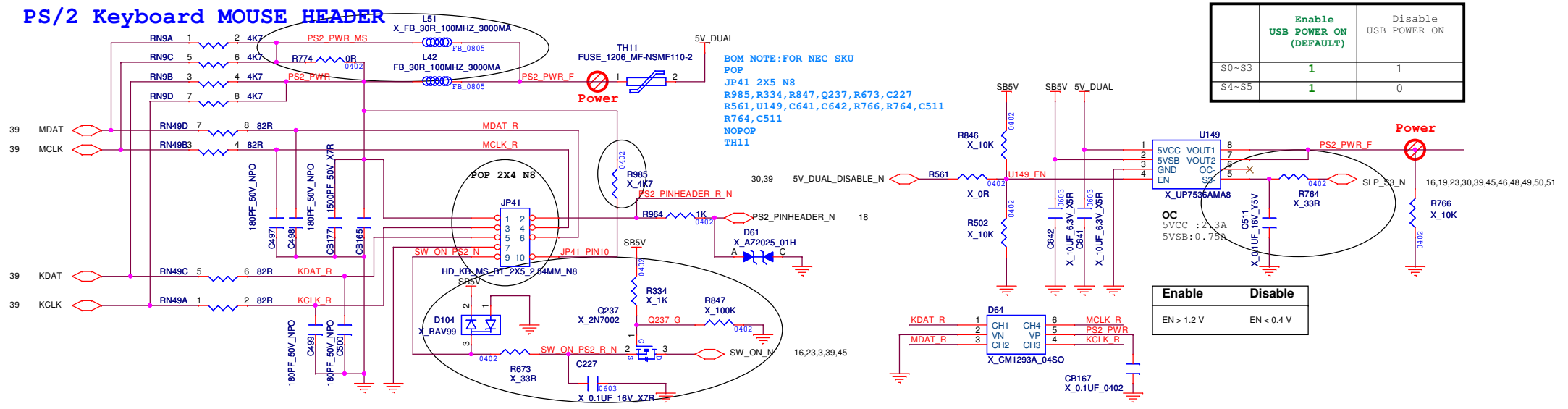
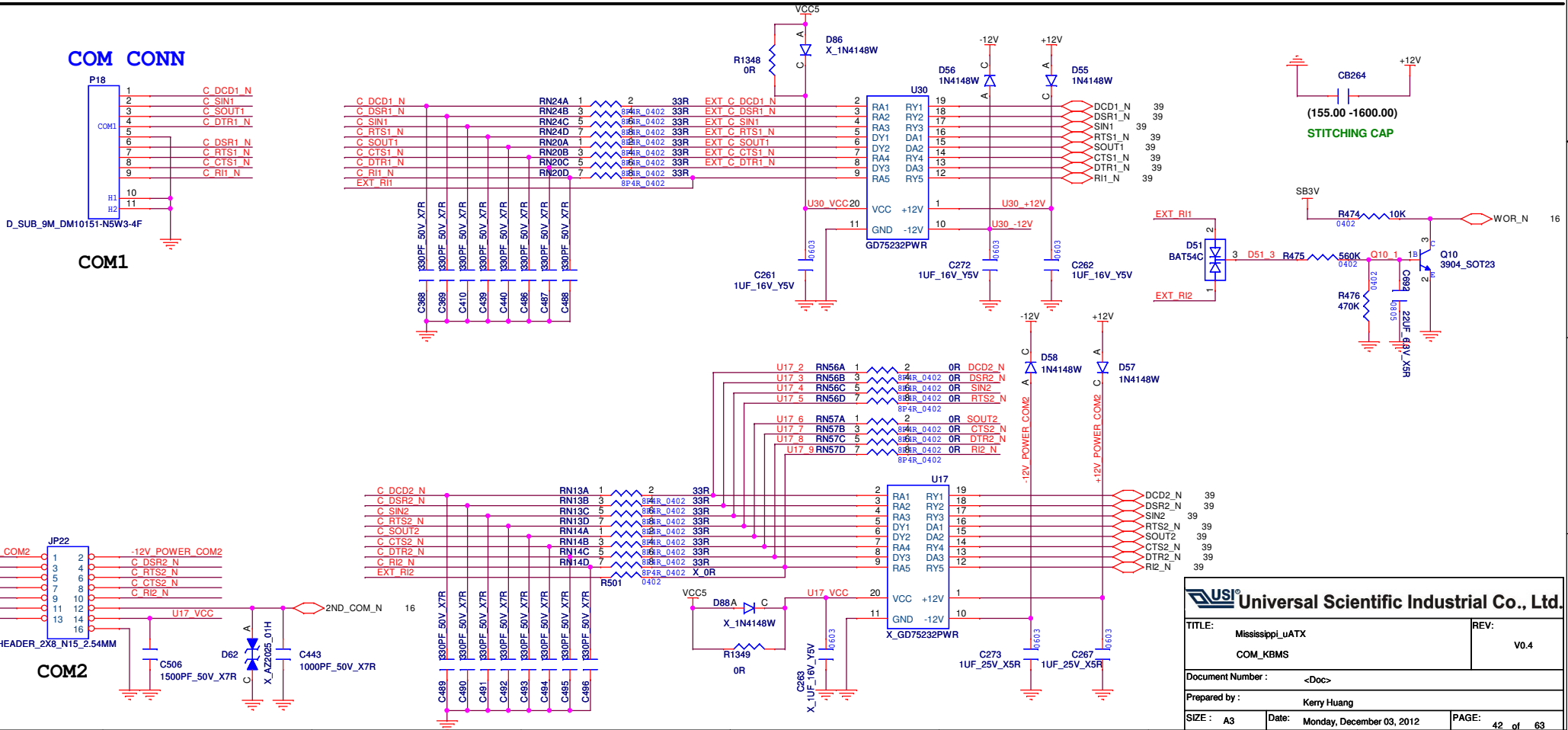
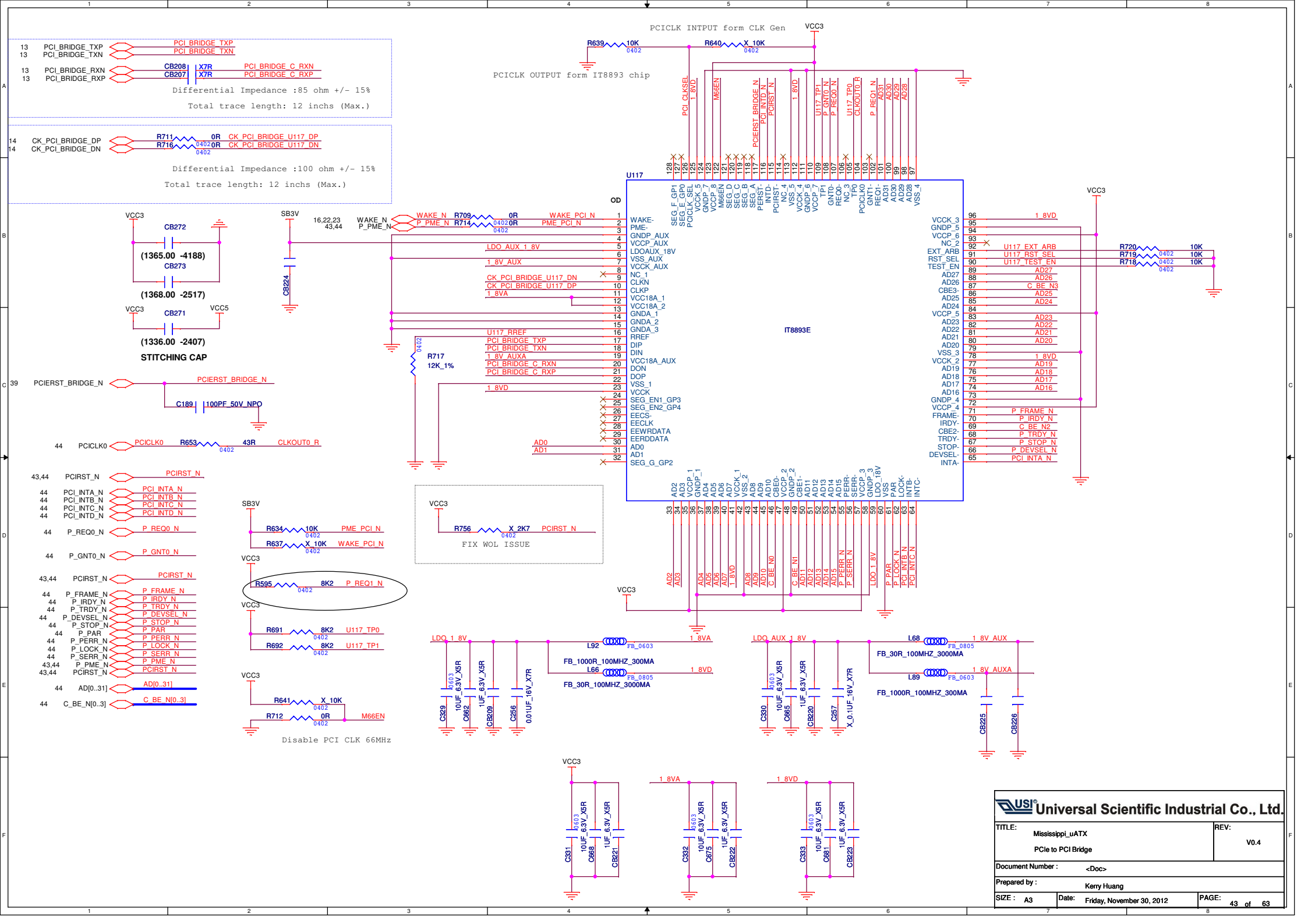
PS/2 Keyboard MOUSE HEADER



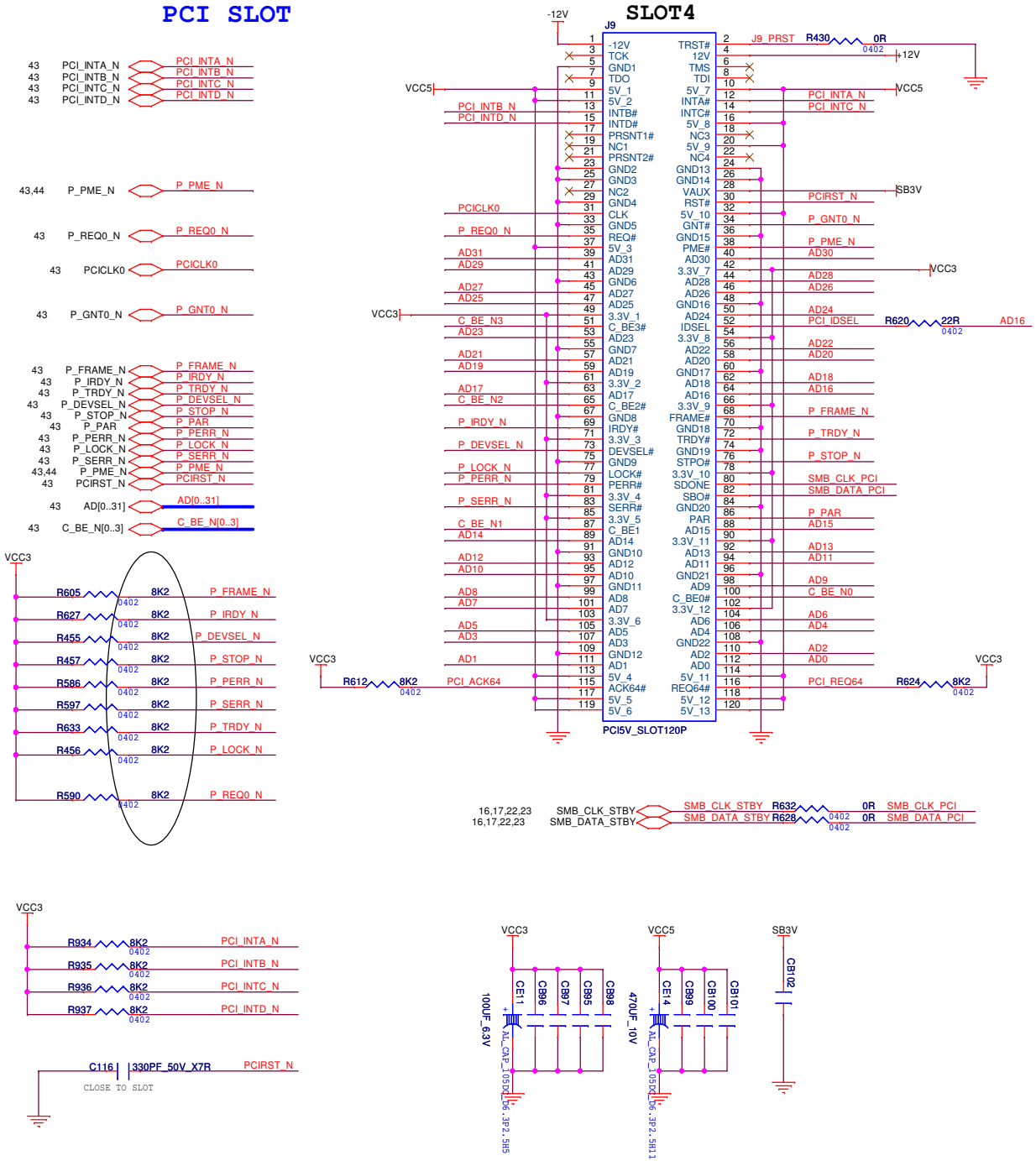
COM CONN



Universal Scientific Industrial Co., Ltd.		
TITLE: Mississippi_uATX COM_KBMS		REV: V0.4
Document Number : <Doc>		
Prepared by : Kerry Huang		
SIZE : A3	Date: Monday, December 03, 2012	PAGE: 42 of 63


PCI_BRIDGE_TXP
PCI_BRIDGE_TXN
PCI_BRIDGE_RXN
PCI_BRIDGE_RXP
CB208 X7R PCI_BRIDGE_C_RXN
CB207 X7R PCI_BRIDGE_C_RXP
Differential Impedance :85 ohm +/- 15%
Total trace length: 12 inchs (Max.)
CK_PCI_BRIDGE_DP
CK_PCI_BRIDGE_DN
R711 0R CK_PCI_BRIDGE_U117_DP
R716 0R CK_PCI_BRIDGE_U117_DN
Differential Impedance :100 ohm +/- 15%
Total trace length: 12 inchs (Max.)
PCICLK INTPUT form CLK Gen
PCICLK OUTPUT form IT8893 chip
R639 10K
R640 X_10K
U117
IT8893E
OD
VCC3
SB3V
CB272
(1365.00 -4188)
CB273
(1368.00 -2517)
CB271
VCC5
(1336.00 -2407)
STITCHING CAP
CB224
R717 12K_1%
WAKE_N
P_PME_N
WAKE_PCI_N
PME_PCI_N
LDO_AUX_1_8V
1_8V_AUX
CK_PCI_BRIDGE_U117_DN
CK_PCI_BRIDGE_U117_DP
1_8VA
U117_RREF
PCI_BRIDGE_TXP
PCI_BRIDGE_TXN
1_8V_AUXA
PCI_BRIDGE_C_RXN
PCI_BRIDGE_C_RXP
1_8VD
AD0
AD1
PCIERST_BRIDGE_N
C189 100PF_50V_NPO
PCICLK0
R653 43R
CLKOUT0_R
PCIRST_N
PCI_INTA_N
PCI_INTB_N
PCI_INTC_N
PCI_INTD_N
P_REQ0_N
P_GNT0_N
P_FRAME_N
P_IRDY_N
P_TRDY_N
P_DEVSEL_N
P_STOP_N
P_PAR
P_PERR_N
P_LOCK_N
P_SERR_N
P_PME_N
AD[0..31]
C_BE_N[0..3]
R634 10K PME_PCI_N
R637 X_10K WAKE_PCI_N
R595 8K2 P_REQ1_N
R691 8K2 U117_TP0
R692 8K2 U117_TP1
R641 X_10K
R712 0R M66EN
Disable PCI CLK 66MHz
R756 X_2K7 PCIRST_N
FIX WOL ISSUE
L92 FB_0603
FB_1000R_100MHZ_300MA
L66 FB_0805
FB_30R_100MHZ_3000MA
L68 FB_0805
L89 FB_0603
C329 10UF_6.3V_X5R
C862 1UF_6.3V_X5R
CB209
C256 0.01UF_16V_X7R
C330 10UF_6.3V_X5R
C865 1UF_6.3V_X5R
CB220
C257 X_0.1UF_16V_X7R
CB225
CB226
C331 10UF_6.3V_X5R
C868 1UF_6.3V_X5R
CB221
C332 10UF_6.3V_X5R
C675 1UF_6.3V_X5R
CB222
C333 10UF_6.3V_X5R
C681 1UF_6.3V_X5R
CB223
R720 10K
R719 10K
R718 10K
U117_EXT_ARB
U117_RST_SEL
U117_TEST_EN
Universal Scientific Industrial Co., Ltd.
TITLE: Mississippi_uATX
PCIe to PCI Bridge
REV: V0.4
Document Number : <Doc>
Prepared by : Kerry Huang
SIZE : A3
Date: Friday, November 30, 2012
PAGE: 43 of 63

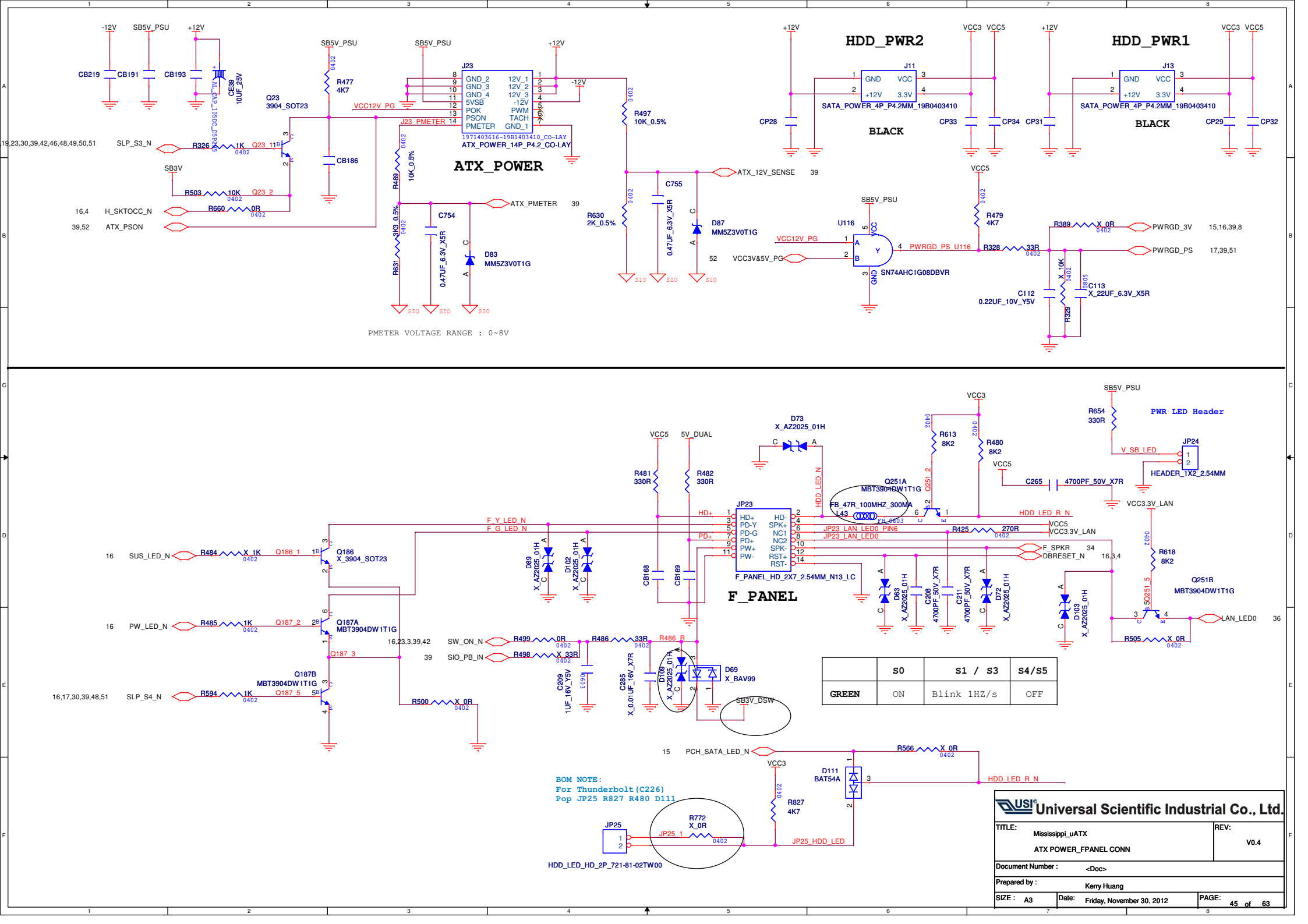
PCI SLOT



PCI Resource

Device	PCI Slot 1
IDSEL	AD16
INT1#	PCI_INTA_N
INT2#	PCI_INTB_N
INT3#	PCI_INTC_N
INT4#	PCI_INTD_N
REQ#	P_REQ0_N
GNT#	P_GNT0_N

Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX PCI SLOT			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 44 of 63	

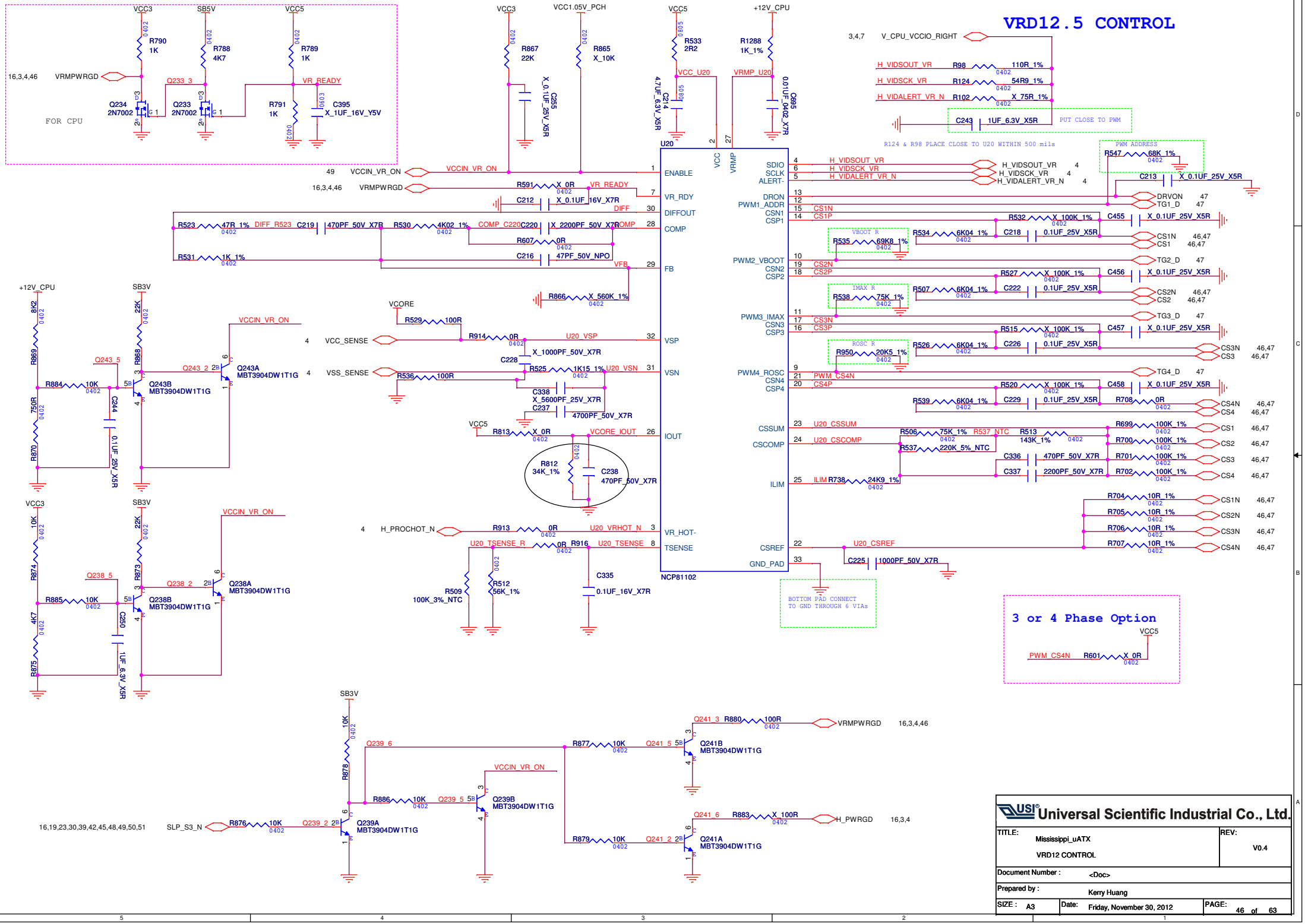


	S0	S1 / S3	S4/S5
GREEN	ON	Blink 1HZ/s	OFF

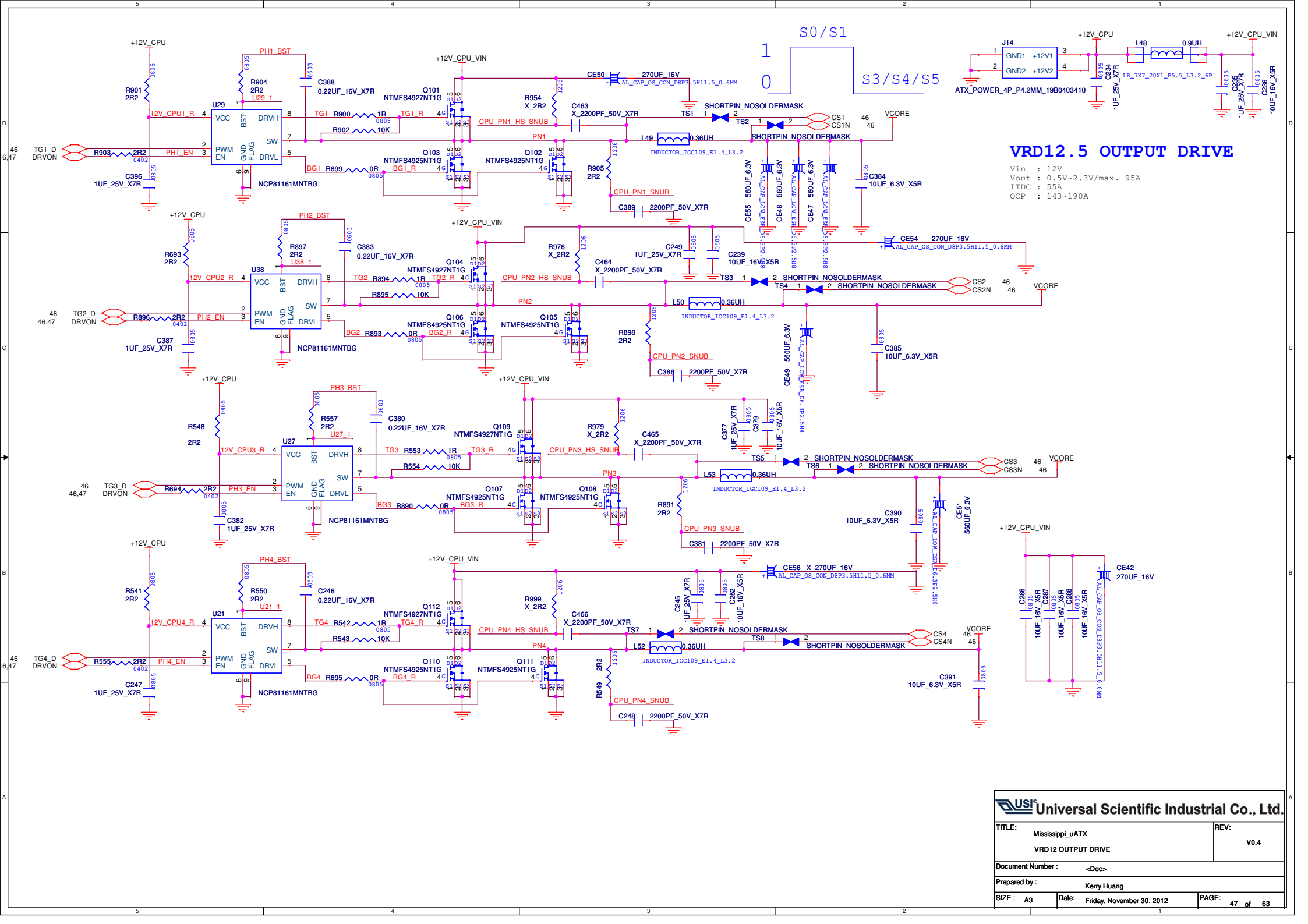
Universal Scientific Industrial Co., Ltd.

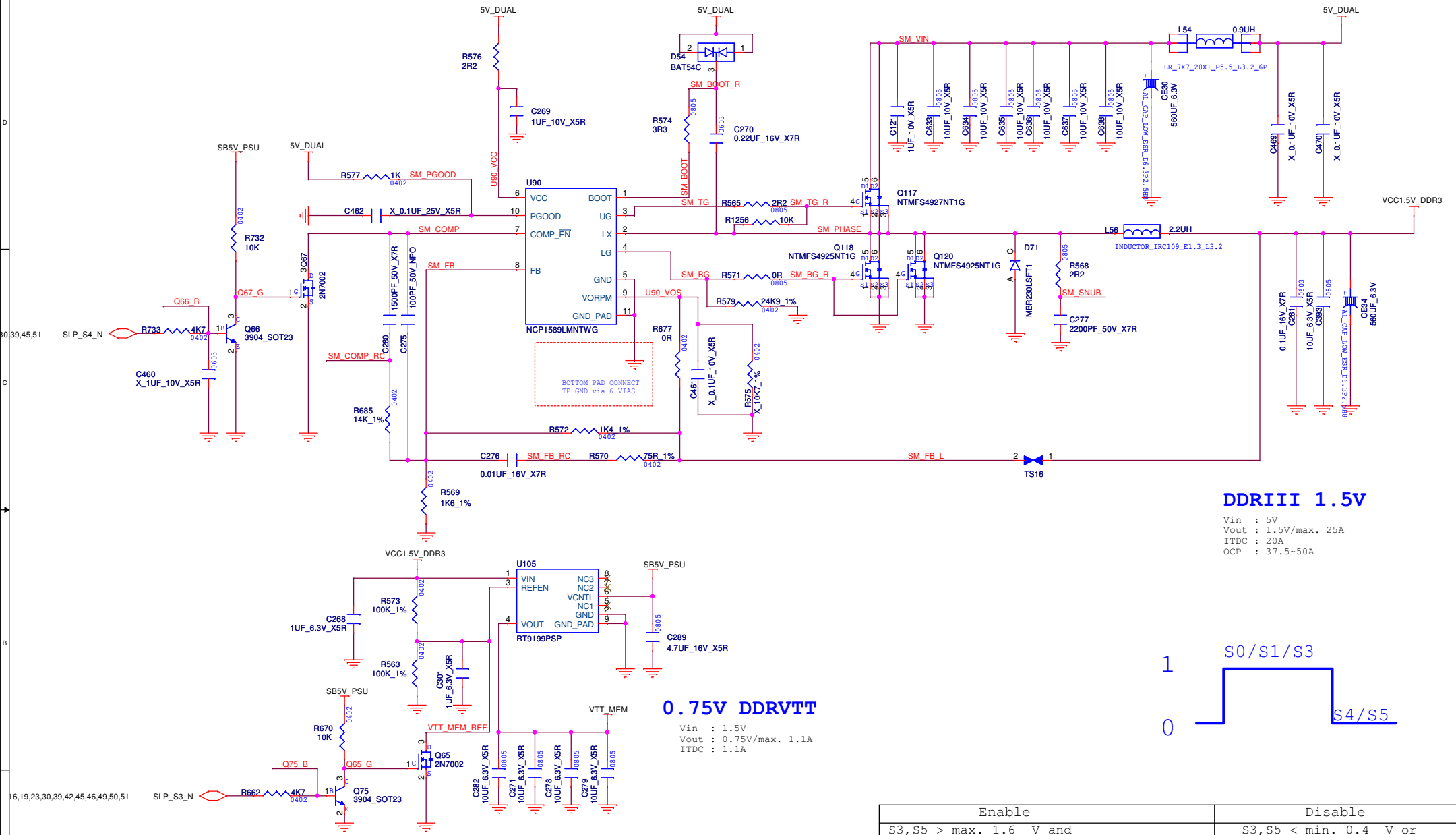
TITLE: Mississippi_uATX ATX POWER_FPANEL CONN		REV: V0.4
Document Number : <Doc>		
Prepared by : Kerry Huang		
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 45 of 63

VRD12.5 CONTROL



Universal Scientific Industrial Co., Ltd.	
TITLE: Mississippi_uATX VRD12 CONTROL	REV: V0.4
Document Number : <Doc>	
Prepared by : Kerry Huang	
SIZE : A3	Date: Friday, November 30, 2012
PAGE: 46 of 63	


S0/S1
S3/S4/S5
VRD12.5 OUTPUT DRIVE
Vin : 12V
Vout : 0.5V~2.3V/max. 95A
ITDC : 55A
OCP : 143~190A
NCP81161MNTBG
ATX_POWER_4P_P4.2MM_19B0403410
INDUCTOR_IGC109_E1.4_L3.2
AL_CAP_OS_CON_D8P3.5H11.5_0.6MM
Universal Scientific Industrial Co., Ltd.
TITLE: Mississippi_uATX
VRD12 OUTPUT DRIVE
REV: V0.4
Document Number : <Doc>
Prepared by : Kerry Huang
SIZE : A3
Date: Friday, November 30, 2012
PAGE: 47 of 63



Enable	Disable
S3,S5 > max. 1.6 V and AVCC > max. 4.4 V.	S3,S5 < min. 0.4 V or AVCC < min. 3.85 V.

	Min	Typ	Max.	Unit
LDO Source Current Limit	2	2.3	2.8	A
LDO Sink Current Limit	-1.4	-1.15	-1	A

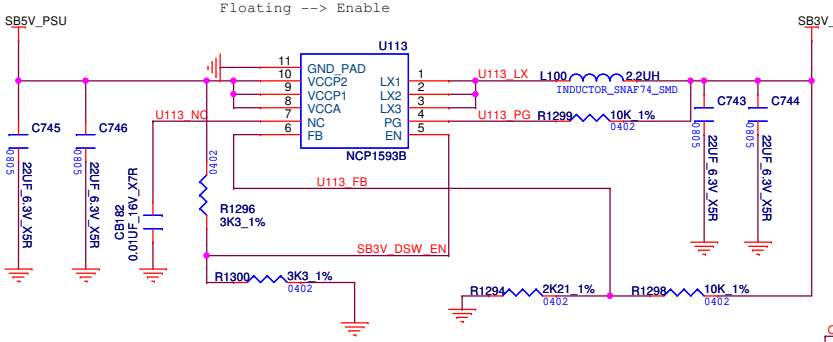
Universal Scientific Industrial Co., Ltd.

TITLE: Mississippi_uATX SM VR		REV: V0.4
Document Number : <Doc>		
Prepared by : Kerry Huang		
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 48 of 63

3.3V SB

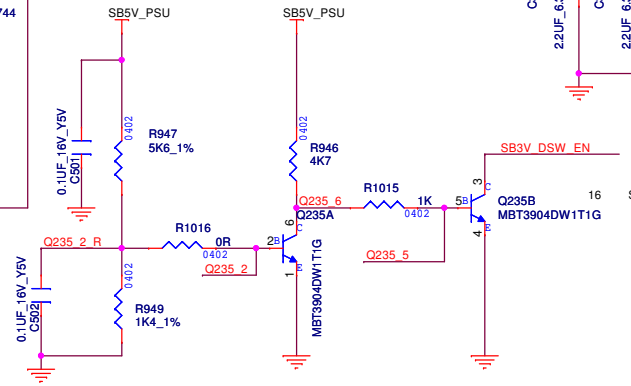
High --> Enable
Low --> Disable
Floating --> Enable

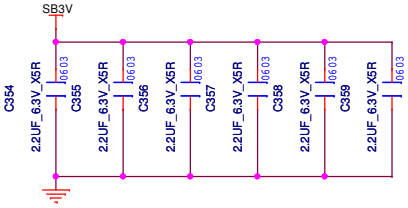
Vin : 5V
Vout : 3.3V/max. 1.1A

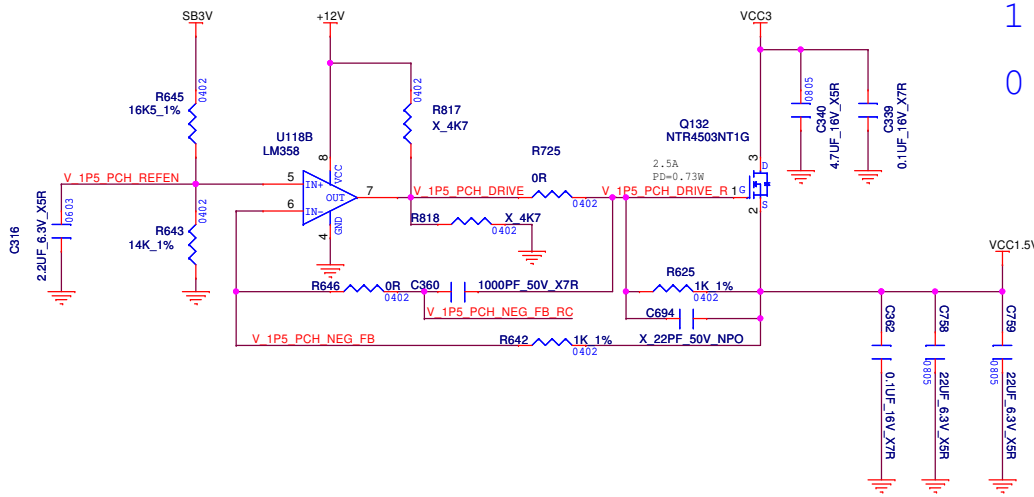


LDO current limit is 2A.

Enable	Disable
VIN > max. 3.5 V.	VIN < min. 3.2 V.

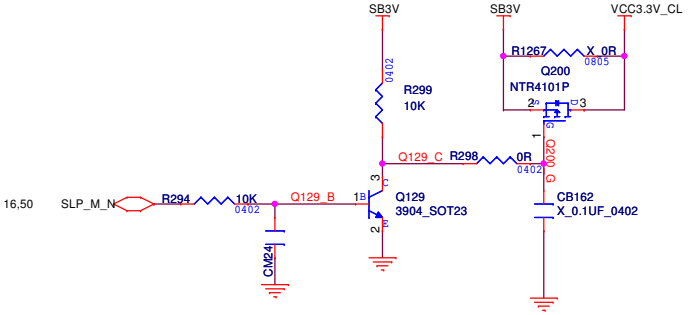


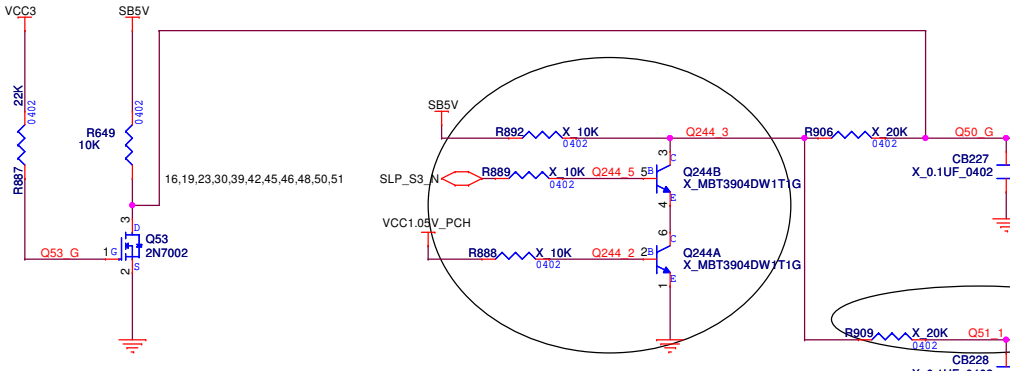


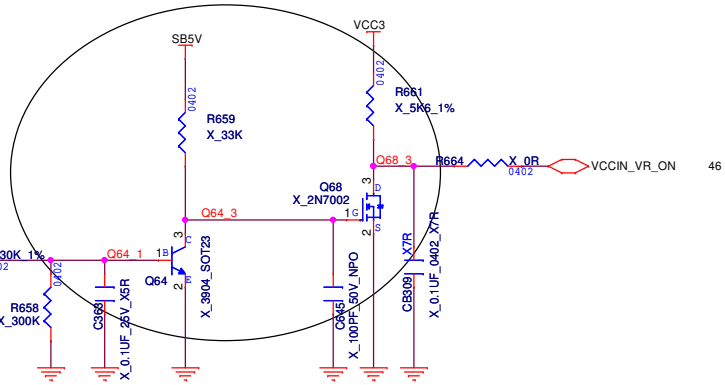


1.5V/max. 0.35 A

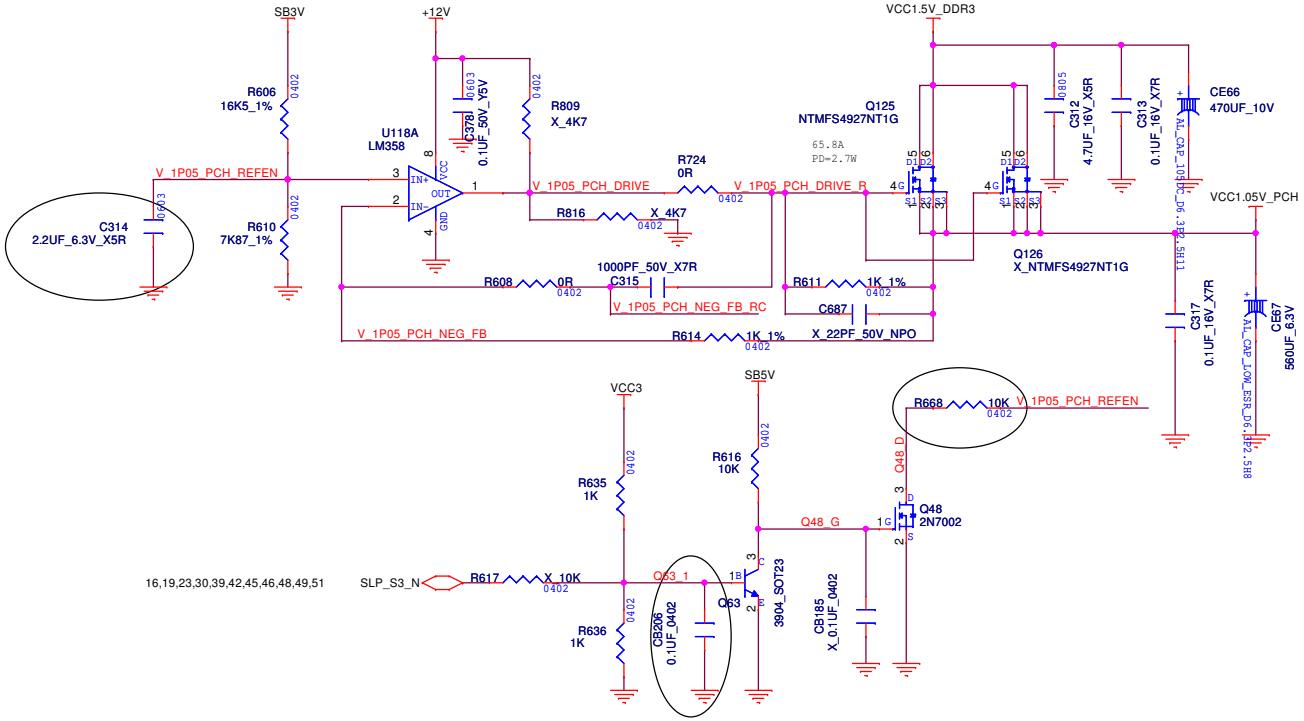
Vin : 3.3V
Vout : 1.5V/max. 0.35A
ITDC : 0.35A
Q132 Max Pd:0.63W





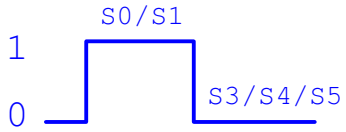


Universal Scientific Industrial Co., Ltd.	
TITLE: Mississippi_uATX VCC1.5V_PCH VR,SB3V_DSW SW , 3P3_LAN , 3P3_CL	REV: V0.4
Document Number : <Doc>	
Prepared by : Kerry Huang	
SIZE : A3 / Date: Friday, November 30, 2012	PAGE: 49 of 63



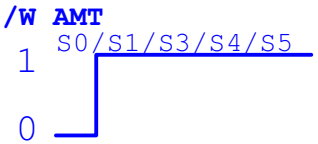
1.05V/max. 5A

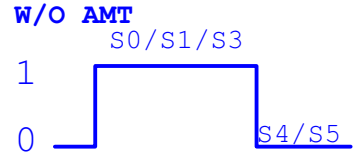
Vin : 1.5V
Vout : 1.05V/max. 5A
ITDC : 5A
Q125 Max Pd:2.25W



Vin : 5V
Vout : 1.05V/max. 1A
ITDC : 1A
OCP:3.8A

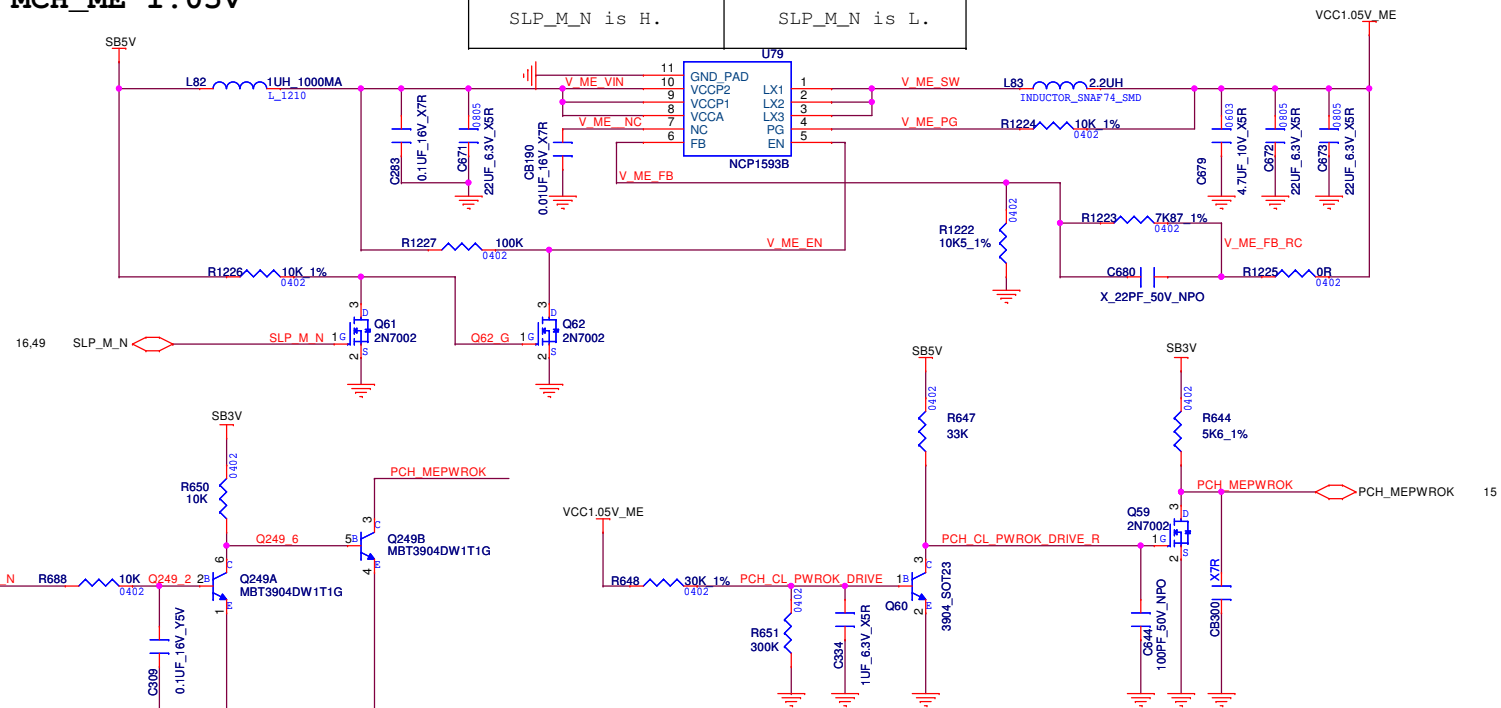
1.05V/max.1A





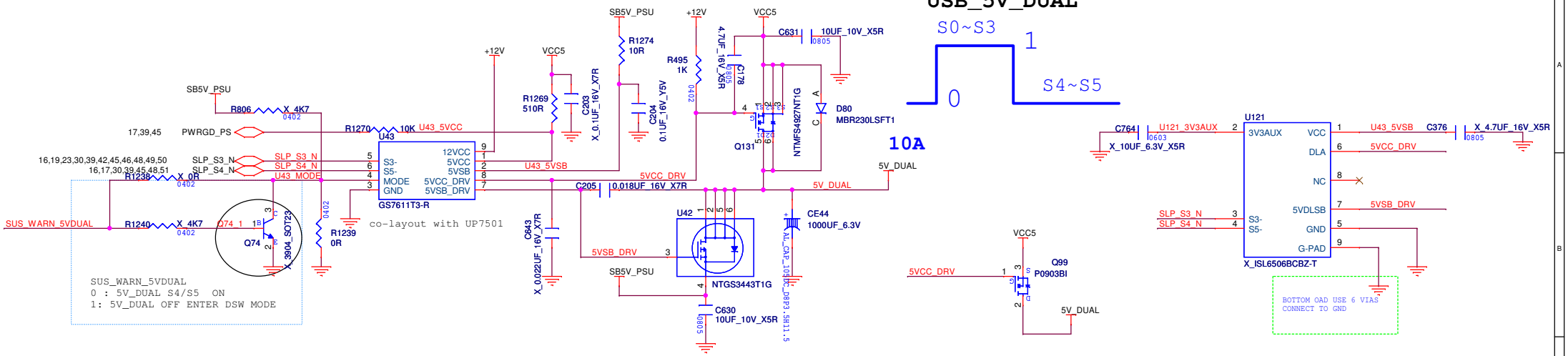
MCH_ME 1.05V

Enable	Disable
SLP_M_N is H.	SLP_M_N is L.

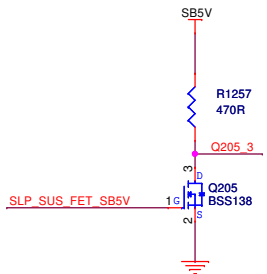


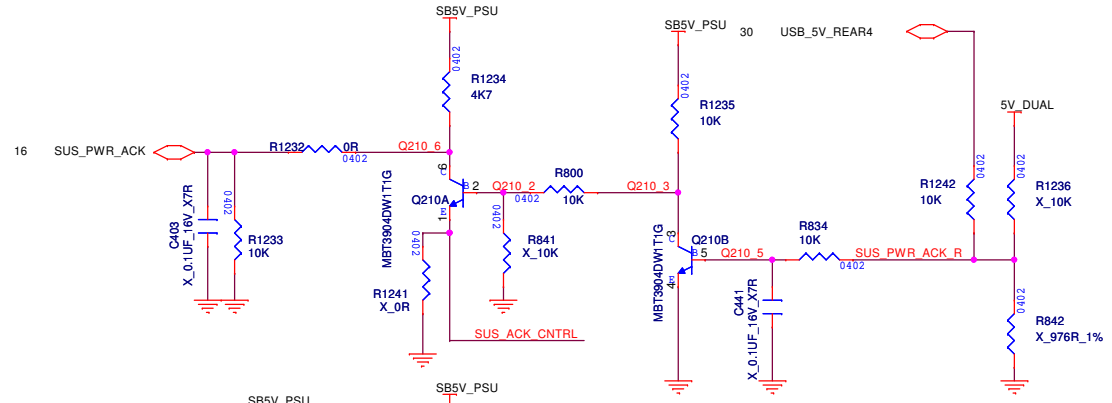
Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX ME VR & 1P05_PCH VR			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Wednesday, December 05, 2012		PAGE: 50 of 63

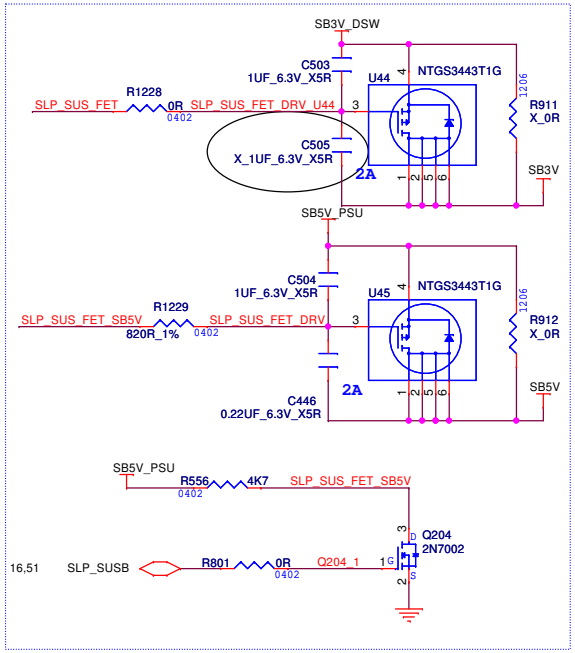
USB_5V_DUAL



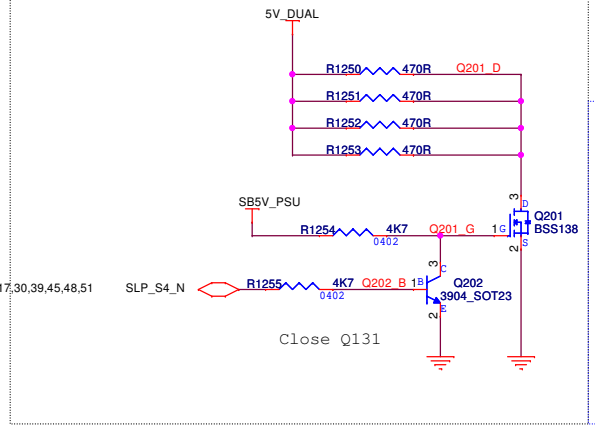
SB5V DISCHARGE

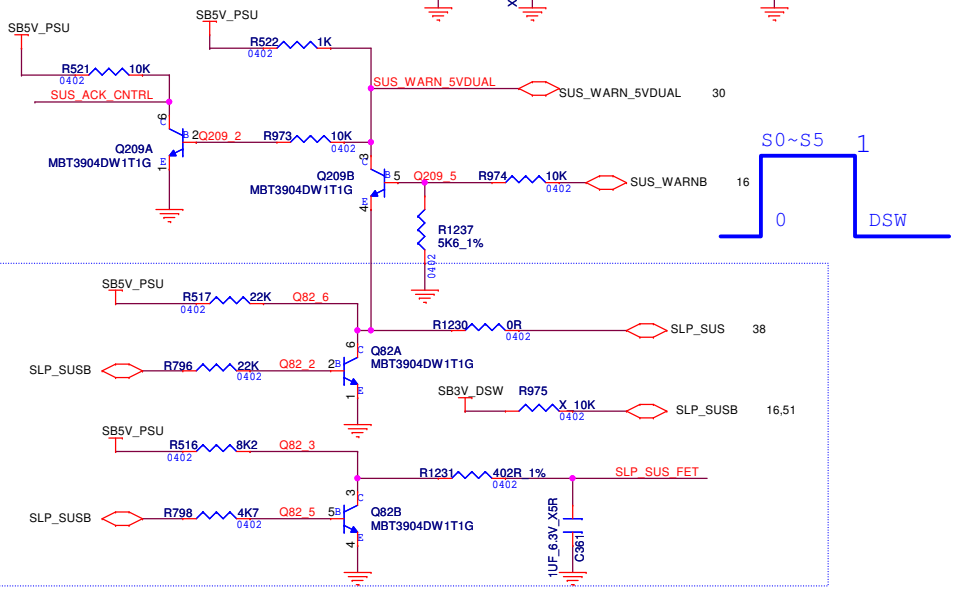






USB DISCHARGE





Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX DUAL VR			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Monday, December 03, 2012		PAGE: 51 of 63

Enable	Disable
EN1,EN2 > 1.4 V	EN1,EN2 < 0.4 V

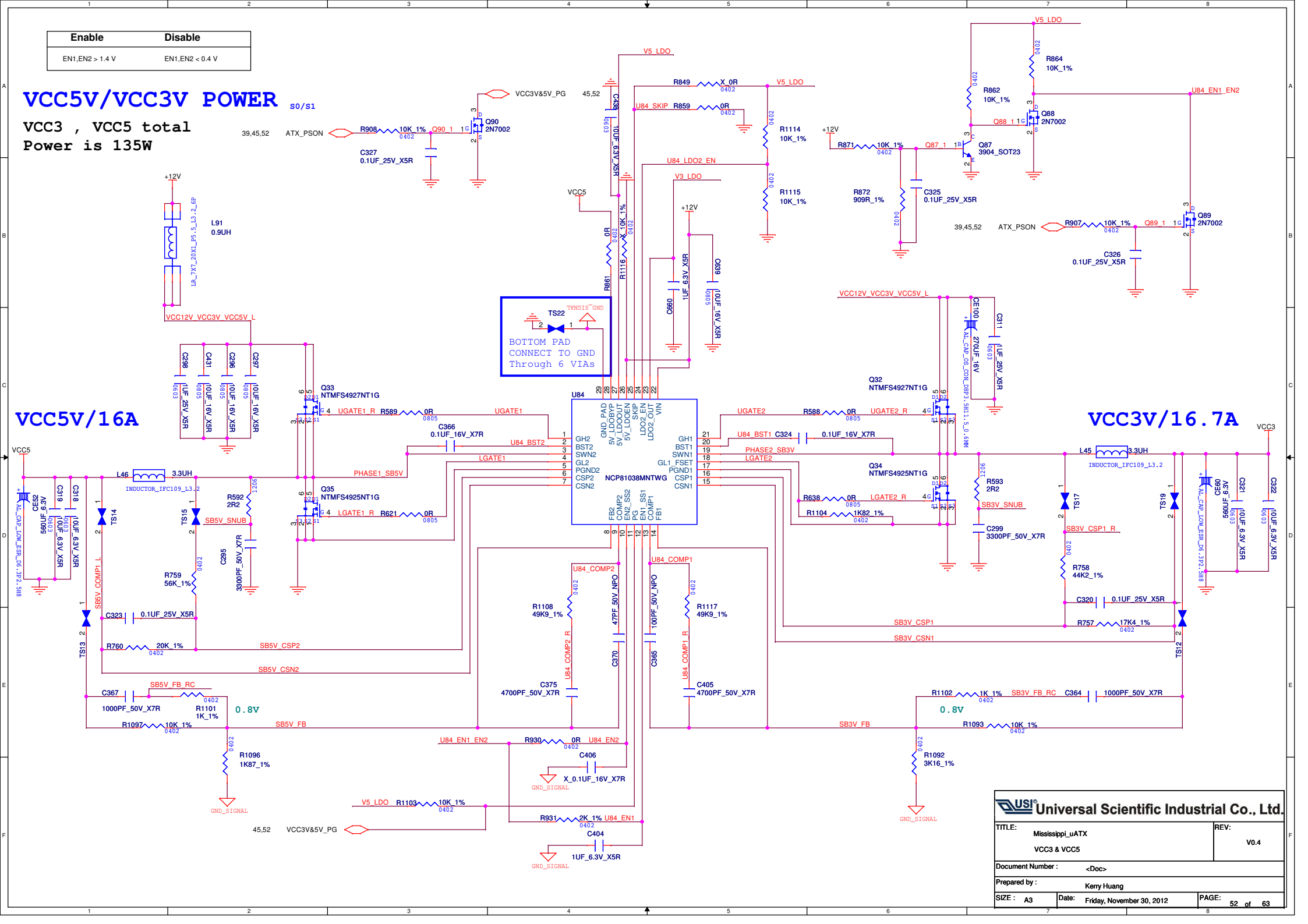
VCC5V/VCC3V POWER

S0/S1

VCC3 , VCC5 total
Power is 135W

VCC5V/16A

VCC3V/16.7A



Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX VCC3 & VCC5			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Friday, November 30, 2012		PAGE: 52 of 63

Flexible IO Assign

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB31	USB32	USB35	USB36	PCIe1	PCIe2	PCIe3	PCIe4	PCIe5	PCIe6	PCIe7	PCIe8	**SATA4** (00)	SATA5	SATA0	SATA1	SATA2	SATA3
				USB33 (01)	**USB34** (01)							PCIe1	**PCIe2** (01)				

Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX BLANK PAGE			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 53 of 63	

TEST POINTS REQUIRMENT

VRM Controller

VCC5 — T25 — VCC5

+12V_CPU — T351 — VCC12

DDR3 (DDR3 POWER)

VCC1.5V_DDR3 — T369 — V_DIMM(CPU)

10,4 DIMM_CA_VREF_A — DIMM_CA_VREF_A

10 DIMM_DQ_VREF_A — DIMM_DQ_VREF_A

11,4 DIMM_CA_VREF_B — DIMM_CA_VREF_B

11 DIMM_DQ_VREF_B — DIMM_DQ_VREF_B

PCH

VCC1.05V_PCH — VDDQ

VBAT — T363 — VCCRTC

VCC3 — T360 — VCC3.3

SB3V — T367 — V3.3SB

19 VCCA_DAC — T368 — VCCA_DAC

HD CODE

VCC3 — T362 — DVDD

VCCA — T365 — AVDD

SIO

VCC3 — T353 — VCC3.3

SPI

VCC3.3V_CL — T373 — VCC3.3_CL

LAN

VCC3.3V_LAN — T380 — 3.3VDD

36 LAN_1.0V — LAN_1.0V — T24 — 1.0VDD

COM1

VCC5 — T378 — VCC5

+12V — T379 — SERIAL1_+12V

-12V — T350 — SERIAL1_-12V

COM2

+12V — T377 — SERIAL2_+12V

-12V — T375 — SERIAL2_-12V

CLOCK

14,18 CK_PCH_33M_FB — CLK_33M_PCH

14,39 CLK_33M_SIO — CLK_33M_SIO

43,44 PCICLK0 — PCICLK0

14,37 CLK_33M_TPM — CLK_33M_TPM

14,37 CLK_33M_LEO — CLK_33M_LEO

14,39 CLK_48M_SIO — CLK_14M_SIO

Differential

14,4 CK_PE_100M_DMI_DP — CLK_100M_DMI+

14,4 CK_PE_100M_DMI_DN — CLK_100M_DMI-

14,5 CK_DP_135M_DN — CLK_DP_135M+

14,5 CK_DP_135M_DP — CLK_DP_135M-

14,4 CK_DPNS_DN — CLK_DPNS+

14,4 CK_DPNS_DP — CLK_DPNS-

14,22 CK_PE_100M_16PORT_DP — CLK_100M_16PORT+

14,22 CK_PE_100M_16PORT_DN — CLK_100M_16PORT-

14,23 CK_PE_100M_4PORT_DP — CLK_100M_4PORT+

14,23 CK_PE_100M_4PORT_DN — CLK_100M_4PORT-

14,23 CK_PE_100M_1PORT_DP — CLK_100M_1PORT+

14,23 CK_PE_100M_1PORT_DN — CLK_100M_1PORT-

14,36 CK_GLAN_DP — CLK_LAN_100M+

14,36 CK_GLAN_DN — CLK_LAN_100M-

14,43 CK_PCI_BRIDGE_DN — CLK_PCI_BRIDGE+

14,43 CK_PCI_BRIDGE_DP — CLK_PCI_BRIDGE-

J26 — N1, N2 — LYNX_POINT_HS_NONPTH_27.6X26.4

RESET

37,39 TPM_RST_N — T385 — TPM_RST

37,39 ASSET_RST_N — T355 — ASSET_RST

18,22,36,39,4 PLTRST_N — T354 — SIO_RST

43,44 PCIRST_N — PCI0_RST

16,34 AC_RST_N — T349 — AUD_RST

J18 — N1, N2, N3 — LGA1156_HS_75MMX75MM_MATX_LC

J17 — N1, N2, N3 — LGA1156_SOCKET_TOP_WITH_BOTTOM

SCREW HOLES

H1 — C_PAD_156_394_8VIA_LC

H5 — C_PAD_156_394_8VIA_S_LC

H2 — C_PAD_156_394_8VIA_S_LC

H6 — C_PAD_156_394_8VIA_LC

H3 — C_PAD_156_394_8VIA_LC

H7 — C_PAD_156_394_8VIA_LC

H4 — C_PAD_156_394_8VIA_LC

H8 — C_PAD_156_394_8VIA_LC

Impedance

T390 IMP_32R_TOP — IMP_END — T381 IMP_VIA — T382 IMP_VIA

9.5 mils 32 Ohm TOP

T391 IMP_50R_TOP — IMP_END — T383 IMP_VIA — T387 IMP_VIA

4 mils 50 Ohm TOP

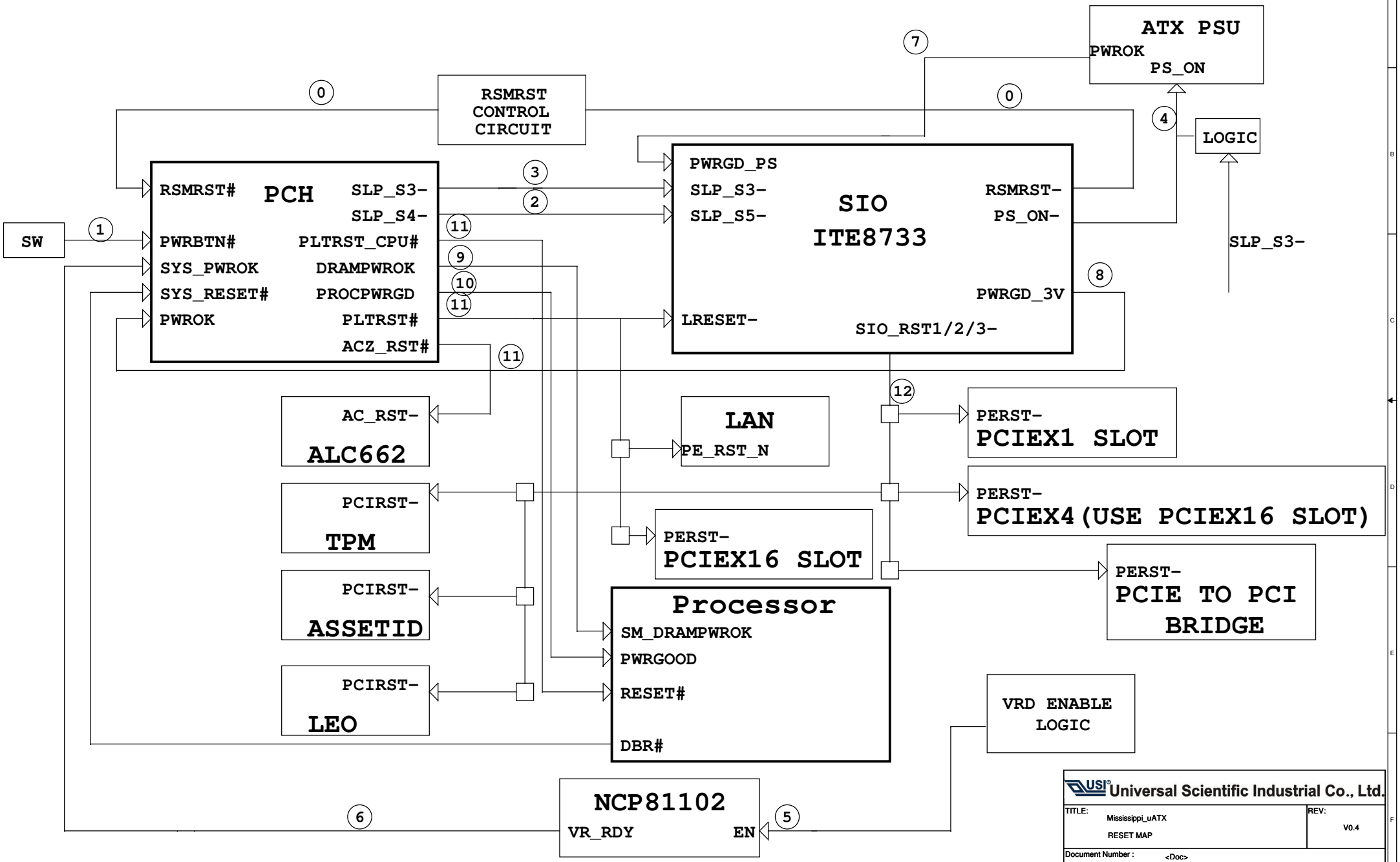
T392 IMP_50R_BOT — IMP_END — T388 IMP_VIA — T389 IMP_VIA

4 mils 50 Ohm BOT

Universal Scientific Industrial Co., Ltd.

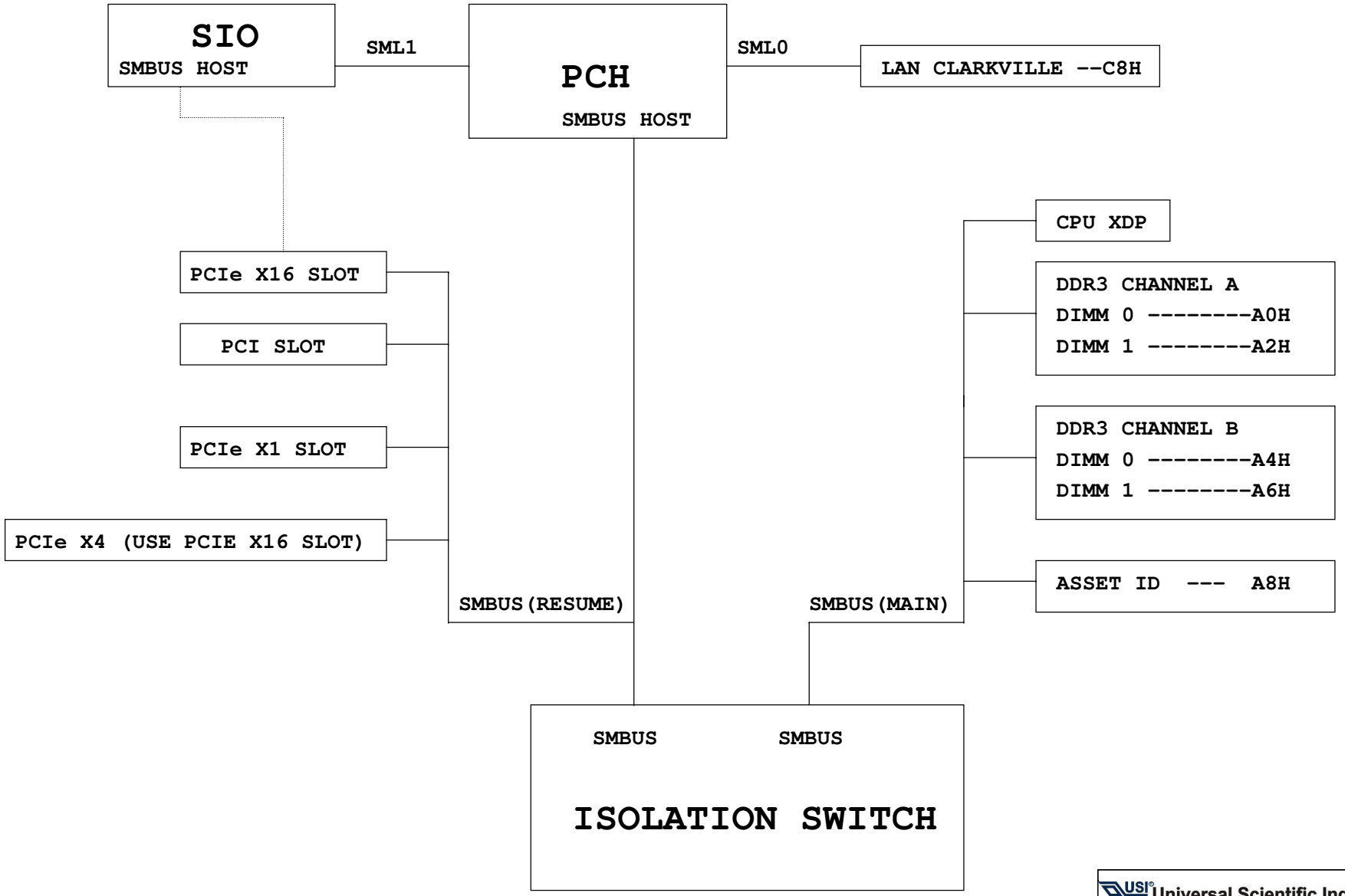
TITLE: Mississippi_uATX HOLE_HEATSINK		REV: V0.4
Document Number : <Doc>		
Prepared by : Kerry Huang		
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 54 of 63

RESET MAP



Universal Scientific Industrial Co., Ltd.			
TITLE: Mississippi_uATX RESET MAP			REV: V0.4
Document Number : <Doc>			
Prepared by : Kerry Huang			
SIZE : A3	Date: Friday, November 30, 2012	PAGE: 55 of 63	

SMBUS MAP



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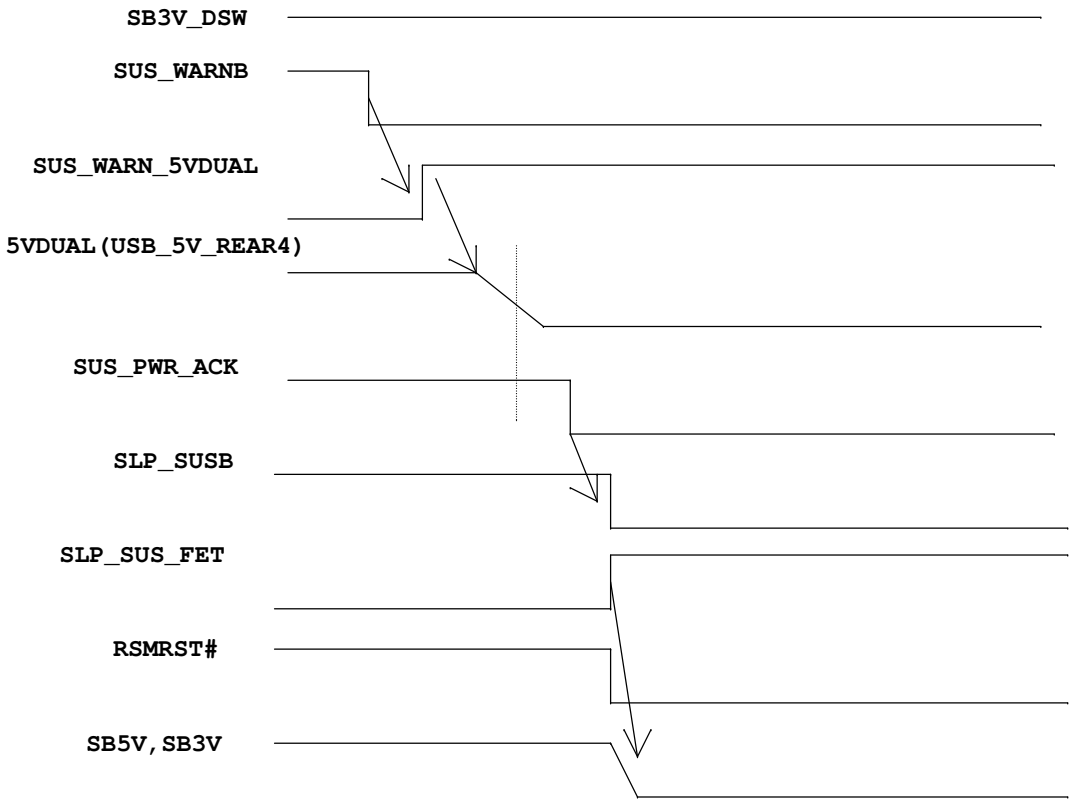
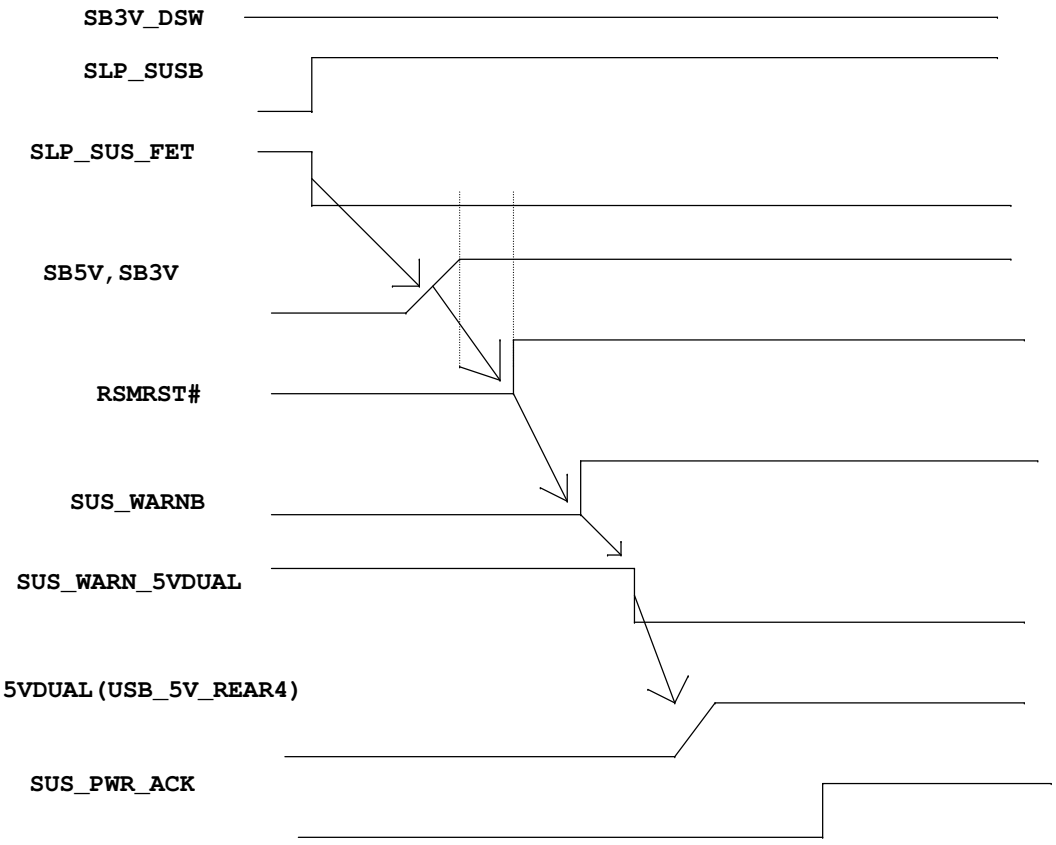
Enter DSW State timing diagram



Exit DSW State timing diagram



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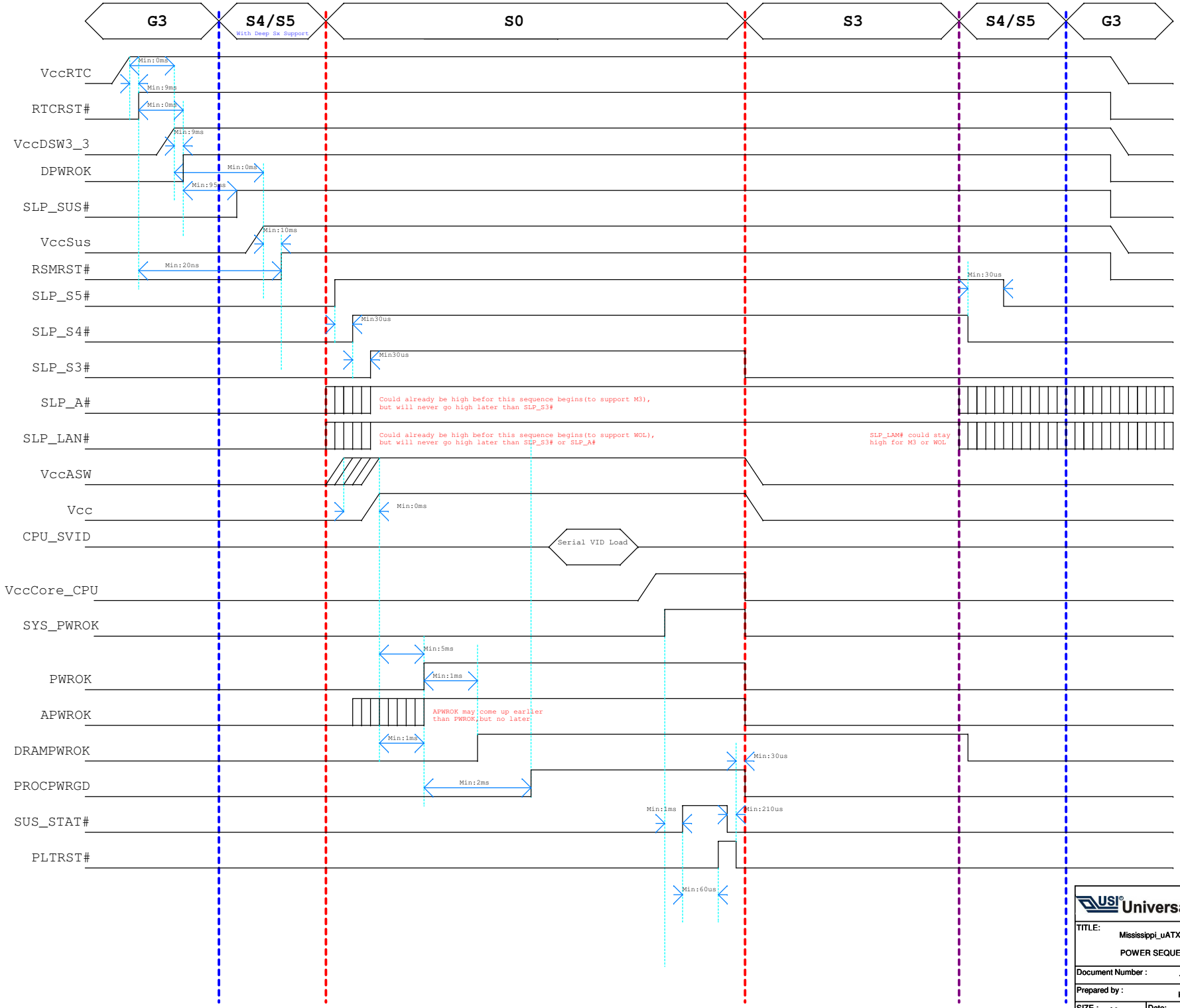

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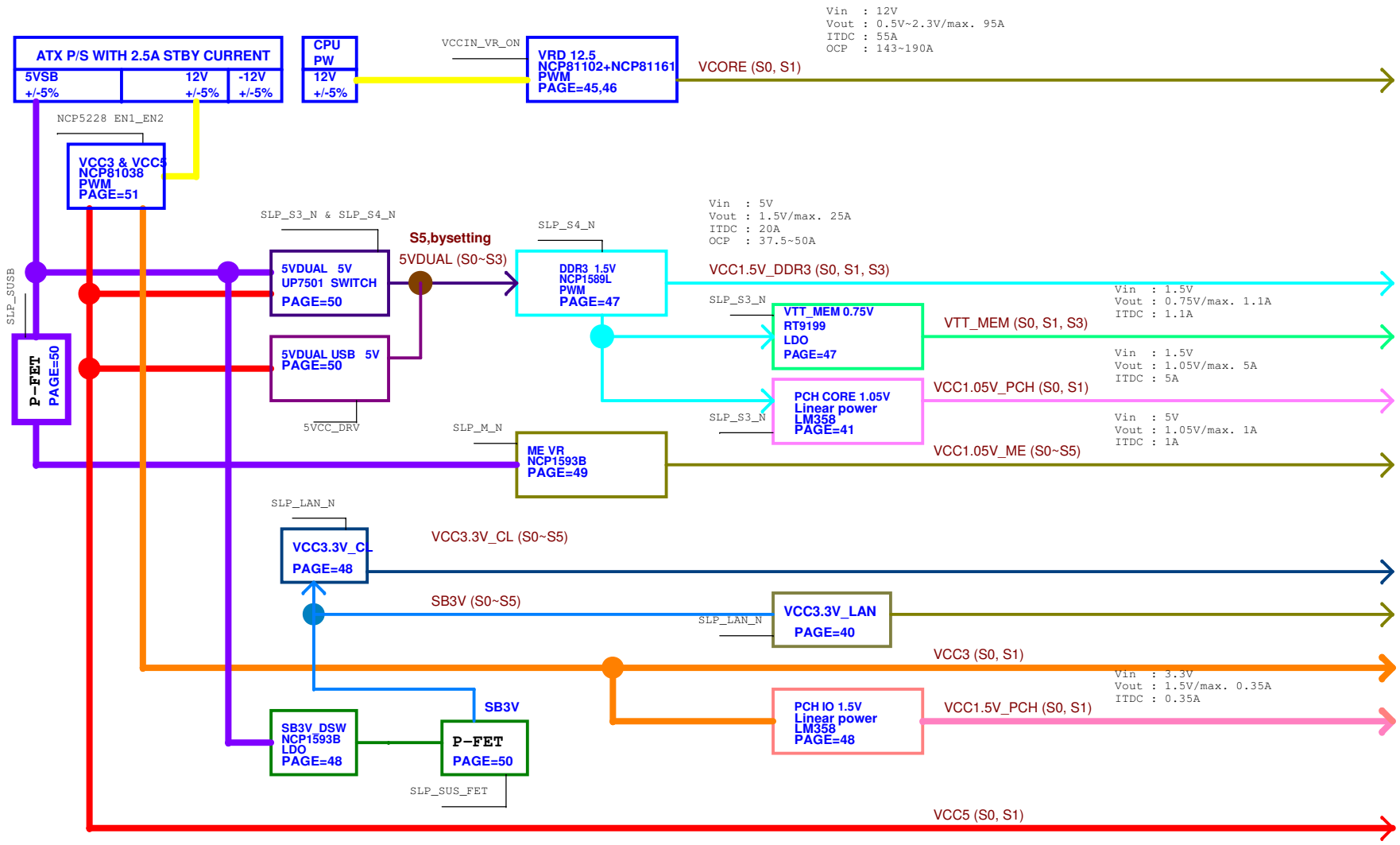

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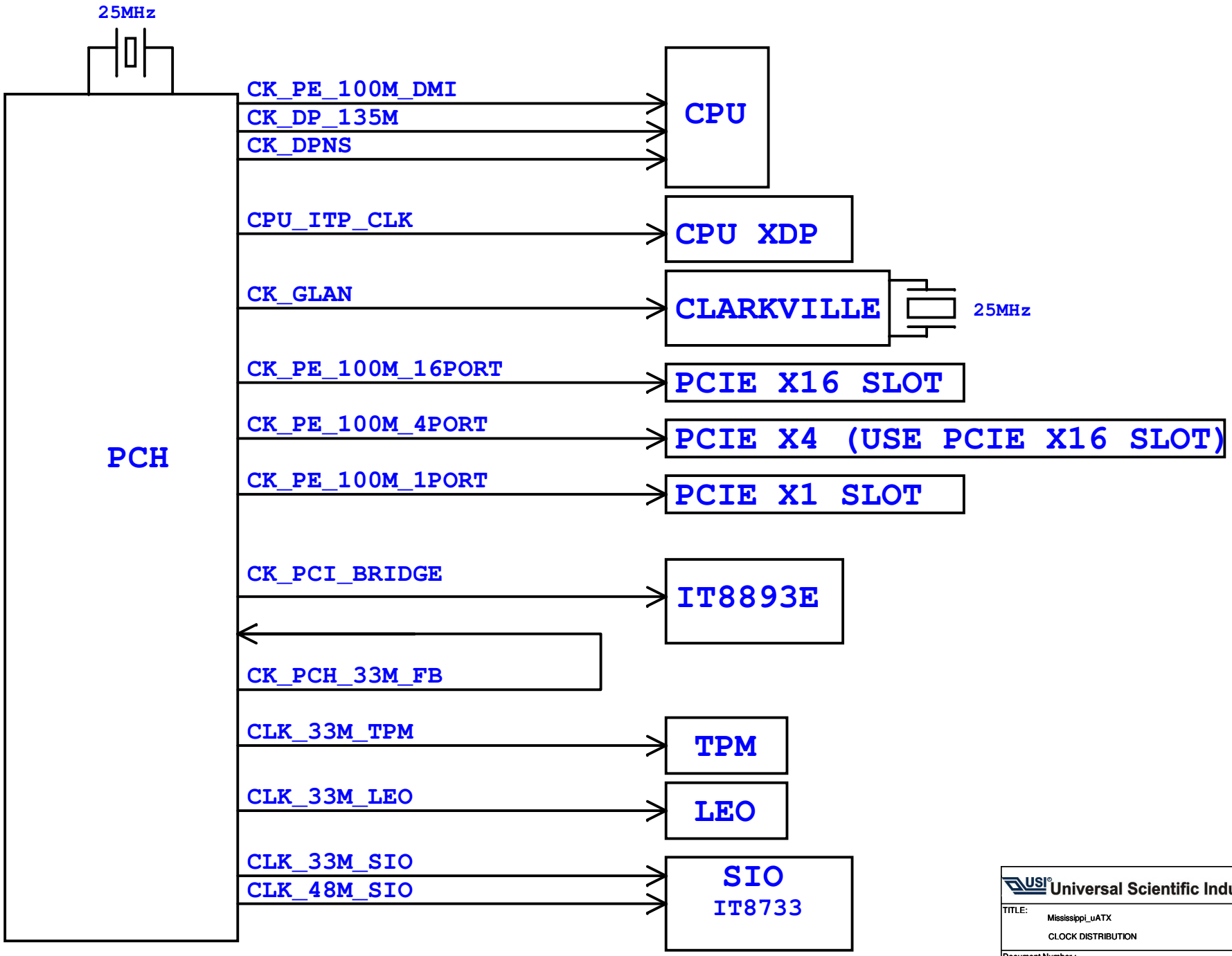
CLOCKS DIAGRAM



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GPIO	TYPE	TOLERANCE	POWER WELL	DEFAULT	BLINK	USAGE
GPIO0	I/O	3.3V	VCC3	GPI	YES	SIO_SCI_N
GPIO1	I/O	3.3V	VCC3	GPI	YES	BRD_ID1
GPIO2	I/O	3.3V	VCC3	Native	YES	NO(10K PU)
GPIO3	I/O	3.3V	VCC3	Native	YES	NO(10K PU)
GPIO4	I/O	3.3V	VCC3	Native	YES	NO(10K PU)
GPIO5	I/O	3.3V	VCC3	Native	YES	NO(10K PU)
GPIO6	I/O	3.3V	VCC3	GPI	YES	BRD_ID0
GPIO7	I/O	3.3V	VCC3	GPI	YES	HDMI_DET_N
GPIO8	I/O	3.3V	SB3V	GPI	YES	IGC_EN_N
GPIO9	I/O	3.3V	SB3V	Native	YES	USB_OC_PORT1011_N
GPIO10	I/O	3.3V	SB3V	Native	YES	USB_OC_PORT89_N
GPIO11	I/O	3.3V	SB3V	GPI	YES	SIO_PME_N
GPIO12	I/O	3.3V	SB3V	Native	YES	LAN_DISABLE_N
GPIO13	I/O	3.3V	SB3V	GP0 (high)	YES	PCH_GPIO13(FOR PEG DEBUG)
GPIO14	I/O	3.3V	SB3V	GPI	YES	USB_DISABLE_N
GPIO15	I/O	3.3V	SB3V	GPI	YES	IBUTTON_GPIO15
GPIO16	I/O	3.3V	VCC3	NATIVE	YES	NO(10K PU)
GPIO17	I/O	3.3V	VCC3	GPI	YES	BRD_ID3
GPIO18(mobile only)	I/O	3.3V	VCC3	GPI	YES	NO(10K PD)
GPIO19	I/O	3.3V	VCC3	GPI	YES	NO(10K PU)
GPIO20	I/O	3.3V	VCC3	GP0	YES	BT_DISABLE_N
GPIO21	I/O	3.3V	VCC3	GPI	YES	THRM_ID1
GPIO22	I/O	3.3V	VCC3	Native	YES	PCH_SCLOCK
GPIO23	I/O	3.3V	VCC3	GPI	YES	2ND_COM_N
GPIO24	I/O	3.3V	SB3V	GPI	YES	H_SKTOCC_N
GPIO25(mobile only)	I/O	3.3V	SB3V	GPI	YES	NO(10K PD)
GPIO26(mobile only)	I/O	3.3V	SB3V	GPI	YES	NO(10K PD)
GPIO27	I/O	3.3V	VCCDSW3_3	GPI	YES	LANWAKE_N
GPIO28	I/O	3.3V	SB3V	GP0	YES	PW_LED_N
GPIO29	I/O	3.3V	VCCDSW3_3	GP0	NO	NO(10K PU)
GPIO30	I/O	3.3V	SB3V	Native	YES	SUS_WARNB
GPIO31	I/O	3.3V	VCCDSW3_3	GPO	YES	SUS_LED_N
GPIO32	I/O	3.3V	VCC3	GPO	NO	PCH_GPO32
GPIO33	I/O	3.3V	VCC3	GPI	NO	NO(10K PD)
GPIO34	I/O	3.3V	VCC3	GPI	NO	BRD_ID2
GPIO35	I/O	3.3V	VCC3	GPI	NO	F_USB1_PRES_N
GPIO36	I/O	3.3V	VCC3	GPI	NO	CLEAR_CMOS_N
GPIO37	I/O	3.3V	VCC3	GPI	NO	PCH_GPIO37_STRAP
GPIO38	I/O	3.3V	VCC3	Native	NO	PCH_SLOAD
GPIO39	I/O	3.3V	VCC3	Native	NO	PCH_SDATAOUT0

GPIO	TYPE	TOLERANCE	POWER WELL	DEFAULT	BLINK	USAGE
GPIO40	I/O	3.3V	SB3V	Native	NO	USB_OC_PORT23_N
GPIO41	I/O	3.3V	SB3V	Native	NO	USB_OC_PORT4_N
GPIO42	I/O	3.3V	SB3V	Native	NO	USB_OC_PORT5_N
GPIO43	I/O	3.3V	SB3V	GPO	NO	WLAN_DISABLE_N
GPIO44	I/O	3.3V	SB3V	GPI	NO	LAN_OE
GPIO45	I/O	3.3V	SB3V	GPI	NO	LPT_PINHEADER_N
GPIO46	I/O	3.3V	SB3V	GPO	NO	TPM_DISABLE_N
GPIO48	I/O	3.3V	VCC3	Native	NO	PCH_SDATAOUT1
GPIO49	I/O	3.3V	VCC3	Native	NO	NO USE
GPIO50	I/O	3.3V	VCC3	GPO	NO	PCH_GP50_DISTCM
GPIO51	I/O	3.3V	VCC3	Native	NO	NO USE
GPIO52	I/O	3.3V	VCC3	GPI	NO	F_USB2_PRES_N
GPIO53	I/O	3.3V	VCC3	GPI	NO	NO USE
GPIO54	I/O	3.3V	VCC3	GPI	NO	PS2_PINHEADER_N
GPIO55	I/O	3.3V	VCC3	Native	NO	NO_USE
GPIO57	I/O	3.3V	SB3V	GPI	NO	PCH_GP57_LEO
GPIO58	I/O	3.3V	SB3V	Native	NO	SMLINK1_CLK
GPIO59	I/O	3.3V	SB3V	Native	NO	USB_OC_PORT015_N
GPIO60	I/O	3.3V	SB3V	GPI	NO	WLAN_DETECT_N
GPIO61	I/O	3.3V	SB3V	Native	NO	L_LPCPD_N
GPIO62	I/O	3.3V	SB3V	Native	NO	PCH_SUSCLK
GPIO63	I/O	3.3V	SB3V	Native	NO	NO (Test Point)
GPIO64	I/O	3.3V	VCC3	GPO	NO	BT_DISABLE_N
GPIO65	I/O	3.3V	VCC3	Native	NO	CLK_33M_LEO
GPIO66	I/O	3.3V	VCC3	Native	NO	NO (Test Point)
GPIO67	I/O	3.3V	VCC3	Native	NO	CLK_48M_SIO
GPIO68	I/O	3.3V	VCC3	GPI	NO	LC_SENSE
GPIO69	I/O	3.3V	VCC3	GPI	NO	THRM_ID2
GPIO70	I/O	3.3V	VCC3	Native	NO	NO(10K PU)
GPIO71	I/O	3.3V	VCC3	Native	NO	NO(10K PU)
GPIO72	I/O	3.3V	VCCDSW3_3	GP0	NO	NO(1K PU)
GPIO73(mobile only)	I/O	3.3V	SB3V	GPI	NO	NO(10K PD)
GPIO74	I/O	3.3V	SB3V	GPI	NO	LAN_SEL
GPIO75	I/O	3.3V	SB3V	Native	NO	SMLINK1_DATA

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PCH STRAPPING PIN

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	Set pull down. The signal has weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode
GPIO62 /SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	Set pull high THis has a weak internal pull-up .NOTE: The internal pull-up is disabled after RSMRST#
GPIO55	Top-Block Swap Override	Rising edge of PWROK	Set pull high The signal has weak internal pull-up . If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
INTVRMEN	Integrated V VRM Enable / Disable	Always	Set pull high. Integrated VRMs is enabled when INTVRMEN is sampled high
GPIO51	Boot BIOS Strap Bit[1] BBS[1]	Rising edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups
GPIO19	Boot BIOS Strap Bit[0] BBS[0]	Rising edge of PWROK	Connect to ground with un-stuff 1k Ohm pull-down resistor. This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups
GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Set pull high. Tying this strap low configures DMI for ESI compatible operation. This signal has a weak internal pull-up
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of PWROK	reserve pull up If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
GPIO36	RSVD	Rising edge of PWROK	Set pull high This signal has a weak internal pull-down.
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Set pull down , but nopop This signal has a weak internal pull up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
SATA3GP /GPIO37	TLS Confidentiality	Rising edge of PWROK	Set pull high. This signal has a weak internal pull down. TLS CONFIDENTIALITY DISABLE LOW:DISABLE
DDPB_CTRLDATA	PORT B Detected	Rising edge of PWROK	When "1" -- PORT B is detected ; When "0" -- PORT B is not detect This signal has a weak internal pull-down.
DDPC_CTRLDATA	PORT C Detected	Rising edge of PWROK	When "1" -- PORT C is detected ; When "0" -- PORT C is not detect This signal has a weak internal pull-down.
DDPD_CTRLDATA	PORT D Detected	Rising edge of PWROK	When "1" -- PORT D is detected ; When "0" -- PORT D is not detect This signal has a weak internal pull-down.
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep Sx Well (DSW) On-Die VR mode is enabled.
SATA2GP /GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1.The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
GPIO8	Reserved	Rising edge of RSMRST# pin	Set pull high INTEGRATED CLOCK CHIP ENABLE HIGH:Integrated clocking is enabled. LOW:Buffer through mode is enabled.

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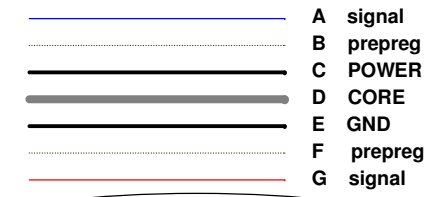
Example Fab Drawing Note

Trace Width (mils)	Differential spacing (mils)	Target Impedance	Tolerance
4	NA	50Ω signgle-end	15%
6.5/5.5(inner)	NA	40Ω signgle-end	15%
8	NA	36Ω signgle-end	15%
8.5/7(inner)	NA	35Ω signgle-end	15%
4	10	95Ω differential	10%
4	6	90Ω differential	15%
4	4	85Ω differential	15%
5	7	85Ω differential	15%
4.5	4	80Ω differential	15%
6.5/5.5(inner)	5/5.5(inner)	70Ω differential	15%
8/7(inner)	5/5.5(inner)	62Ω differential	15%

4 Layers PCB Stack-up



A signal
B prepreg
C POWER
D CORE
E GND
F prepreg
G signal

Board thickness is 1.6+/-0.13mm

Processor Impedance requiremenst by interface

Interface	Impedance required
DDR3 CLK	36Ω signgle-end
DDR3 DQ,DQS	40Ω signgle-end
DDR3 CTRL	40Ω signgle-end
DDR3 CMD	35Ω signgle-end
PEG	80Ω differential
DMI/FDI	85Ω differential
DP/HDMI	85Ω differential
DDR3 CLK	62Ω differential
VGA	37 Ω, single-ended at Ibex Peak breakout, then 50 Ω, single-ended to VGA connector

Lynx Point Impedance requiremenst by interface

Interface	Impedance required
Misc.	50Ω signgle-end
PCIE 2.0	85Ω differential
USB2/3	85Ω differential
SATA2/3	85Ω differential
Platform Clocks	90Ω differential

LAN Impedance requiremenst by interface

Interface	Impedance required
MDI	100Ω differential

PCB Stack-Up Details

Layer	Description	Minimum (in mils)	Typical (in mils)	Maximum (in mils)	Comments
A	Signal	1.1	1.9	2.7	Final thickness after plating
B	Prepreg	NA	2.7	3.5	4-mil line = 50 Ω for external layer A
C	Power	1.2	—	1.4	1 oz copper
D	Core	47 mil core height is recommended, but fab vendors will adjust core thickness to achieve overall board thickness (including soldermask height) to Intel Spec of 1.6 mm nominal, with a tolerance of +/-0.13mm			
E	Gnd	1.2	—	1.4	1 oz copper
F	Prepeg	NA	2.7	3.5	4-mil line = 50 Ω for external layer G
G	Signal	1.1	1.9	2.7	Final thickness after plating

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