Alpha

MS-7807 Ver: 1.1

CPU:

INTEL IVY BRIDGE (BGA 1023)

System Chipset:

INTEL-HM76 (PANTHER POINT)

OnBoard Chipset:

Audio Codec - REALTEK/ALC272
Audio AMPLIFIER - REALTEK/ALC113
SIO - NUVOTON/NPCE885LCE
Scaler - REALTEK/RTD2486HD
Flash ROM: 64 Mb SPI (CHIP)

Main Memory:

DDRIII * 2 (Dual Channel)

Expansion Slots:

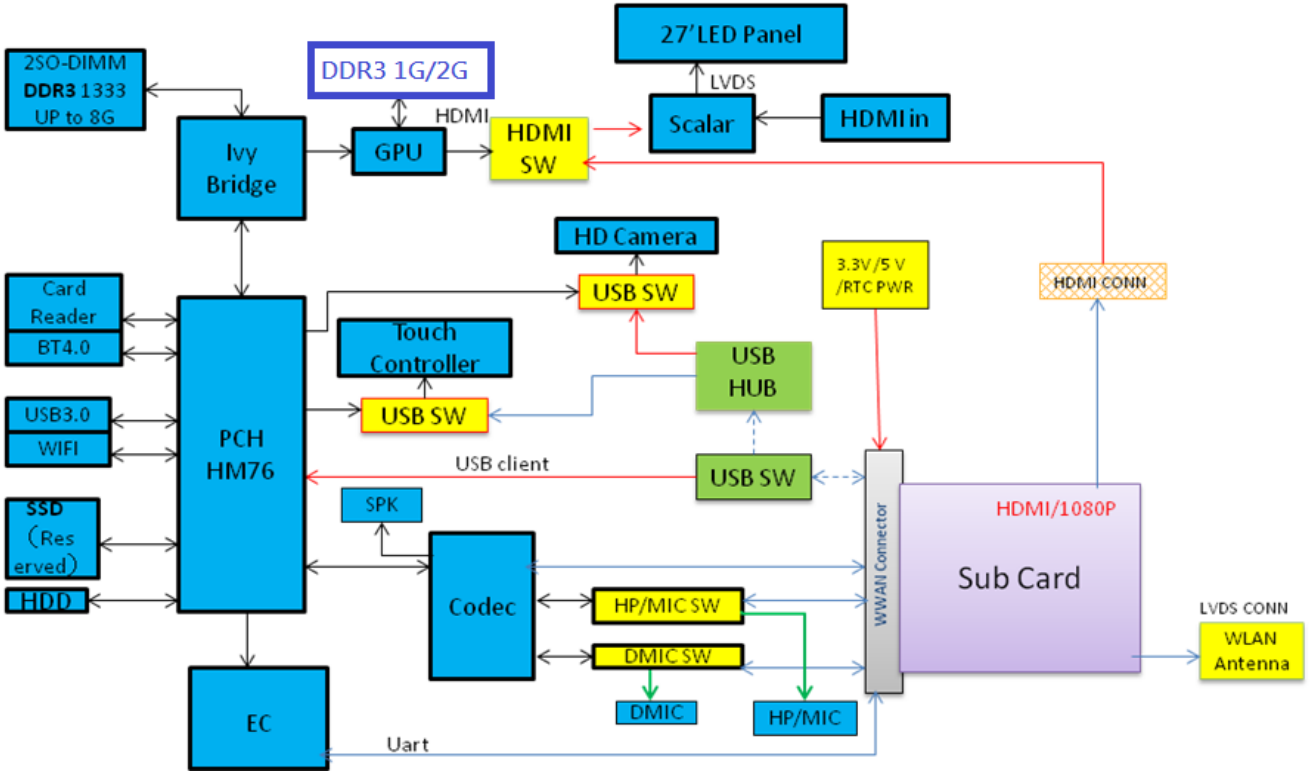
Mini PCI-e (X1) * 1
MSATA * 1
SATA * 1
Mini PCI-e (X1) * 1 for HYBRID CARD

PWM:

Controller: Intersil /ISL95837 1+1 phase

Other:

USB3.0 *2 (SIDE)
USB2.0 (Pin header for Device)
HDMI in*1
LVDS*1



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	MS-7807	
Size B	Document Description: Block Diagram	Rev 1.0
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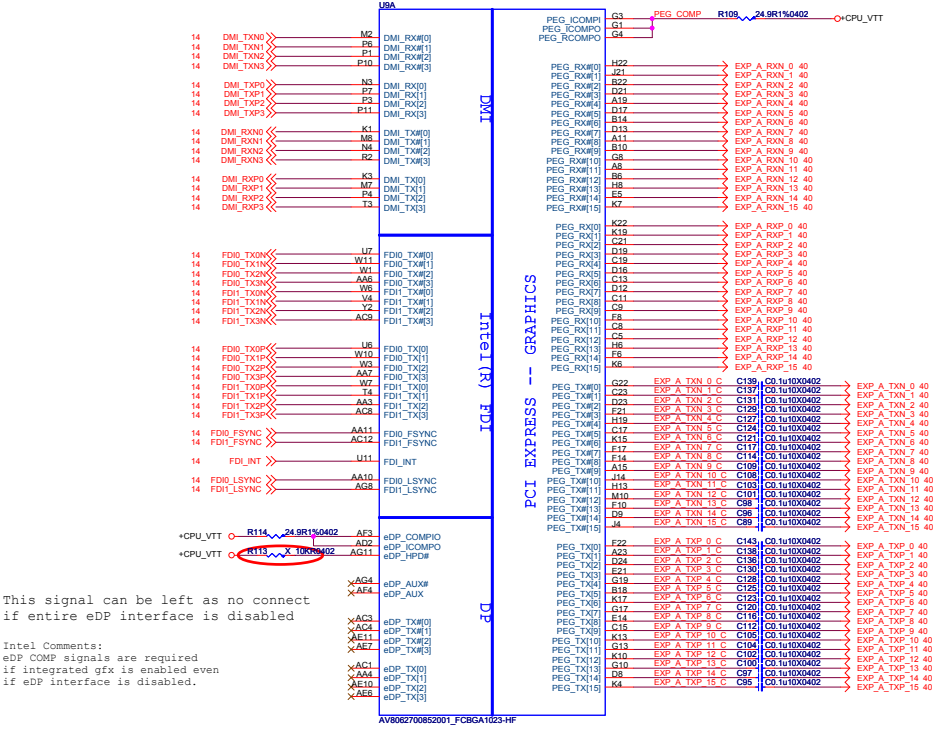
IVYBRIDGE PROCESSOR (DMI,DP,PEG,FDI)

PEG_ICOMPO Width:12 mils Spacing:15 mils
PEG_RCOMPO Width:4 mils Spacing:15 mils
PEG_ICOMPI Width:4 mils Spacing:15 mils



This signal can be left as no connect
if entire eDP interface is disabled

Intel Comments:
eDP COMP signals are required
if integrated gfx is enabled even
if eDP interface is disabled.

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	PROCESSOR (DMI,DP,PEG,FDI)		
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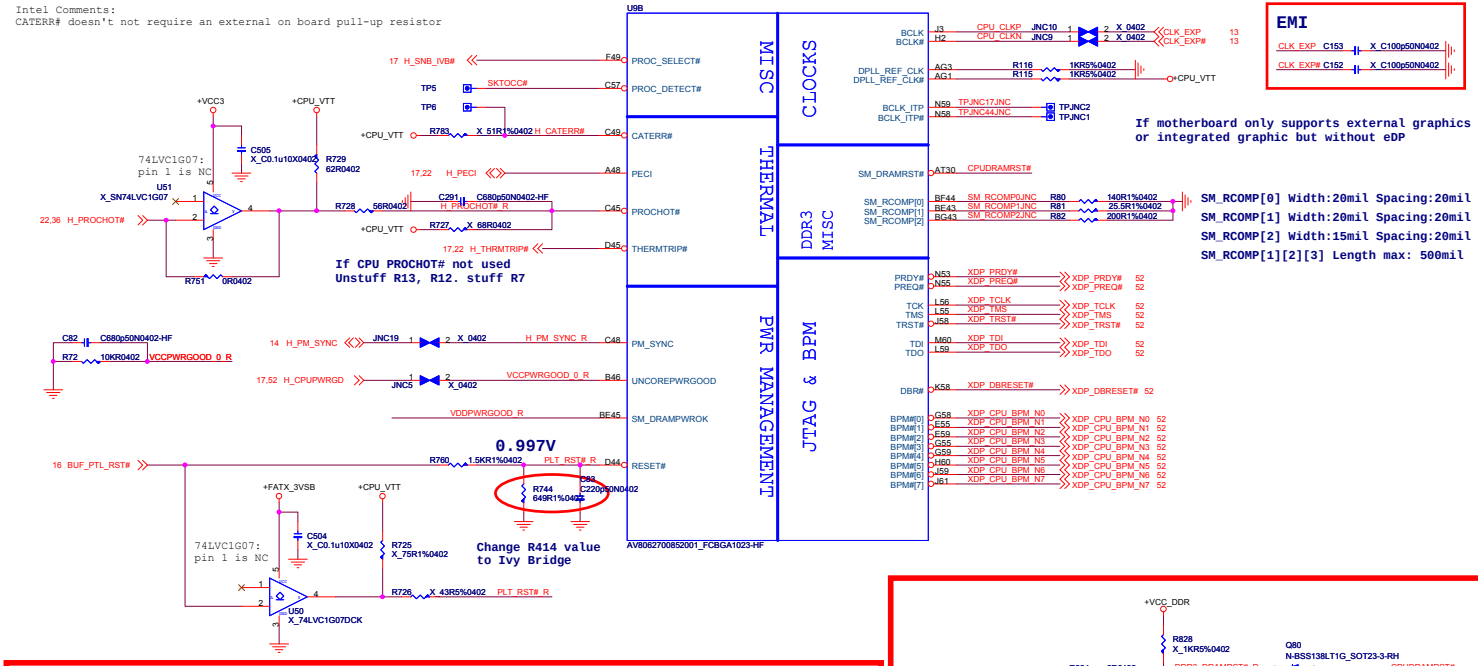
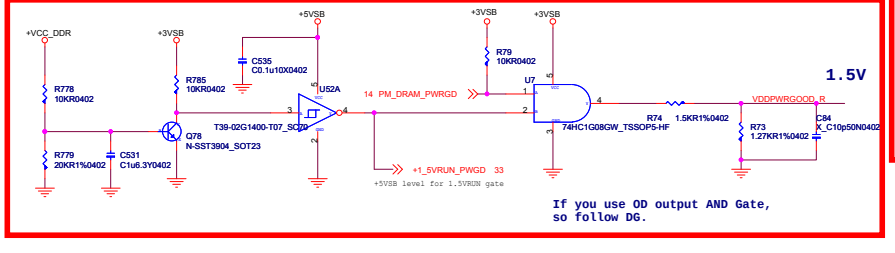
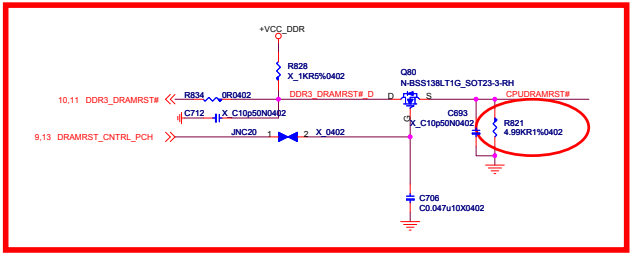
IVYBRIDGE PROCESSOR (CLK,MISC,JTAG)







MICRO-STAR INT'L CO.,LTD.			
Title: PROCESSOR (CLK,MISC,JTAG)			
Size: A3	Document Number: MS-7807		Rev: 1.0
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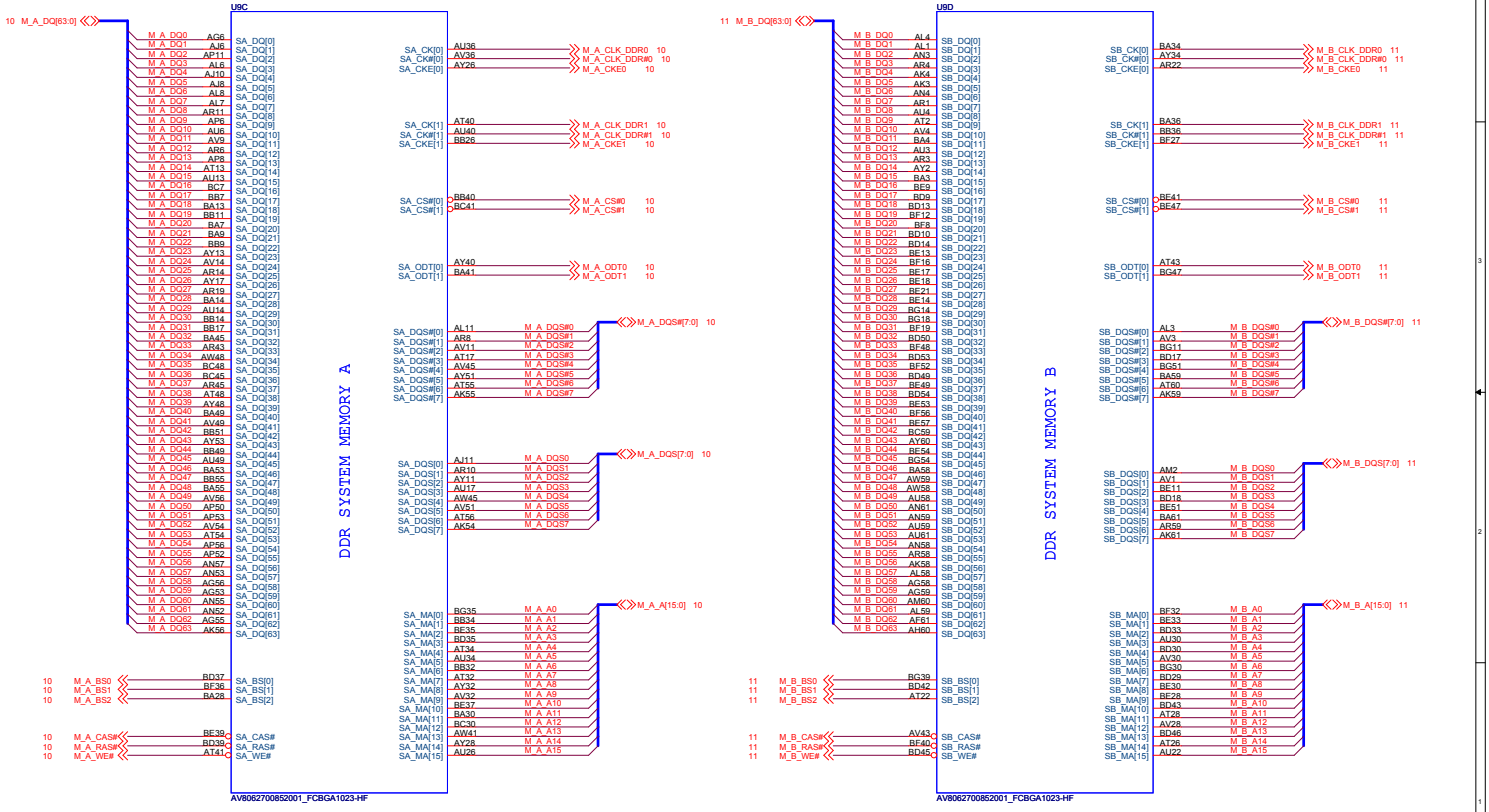
IVYBRIDGE PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.		
Title: PROCESSOR (DDR3)		
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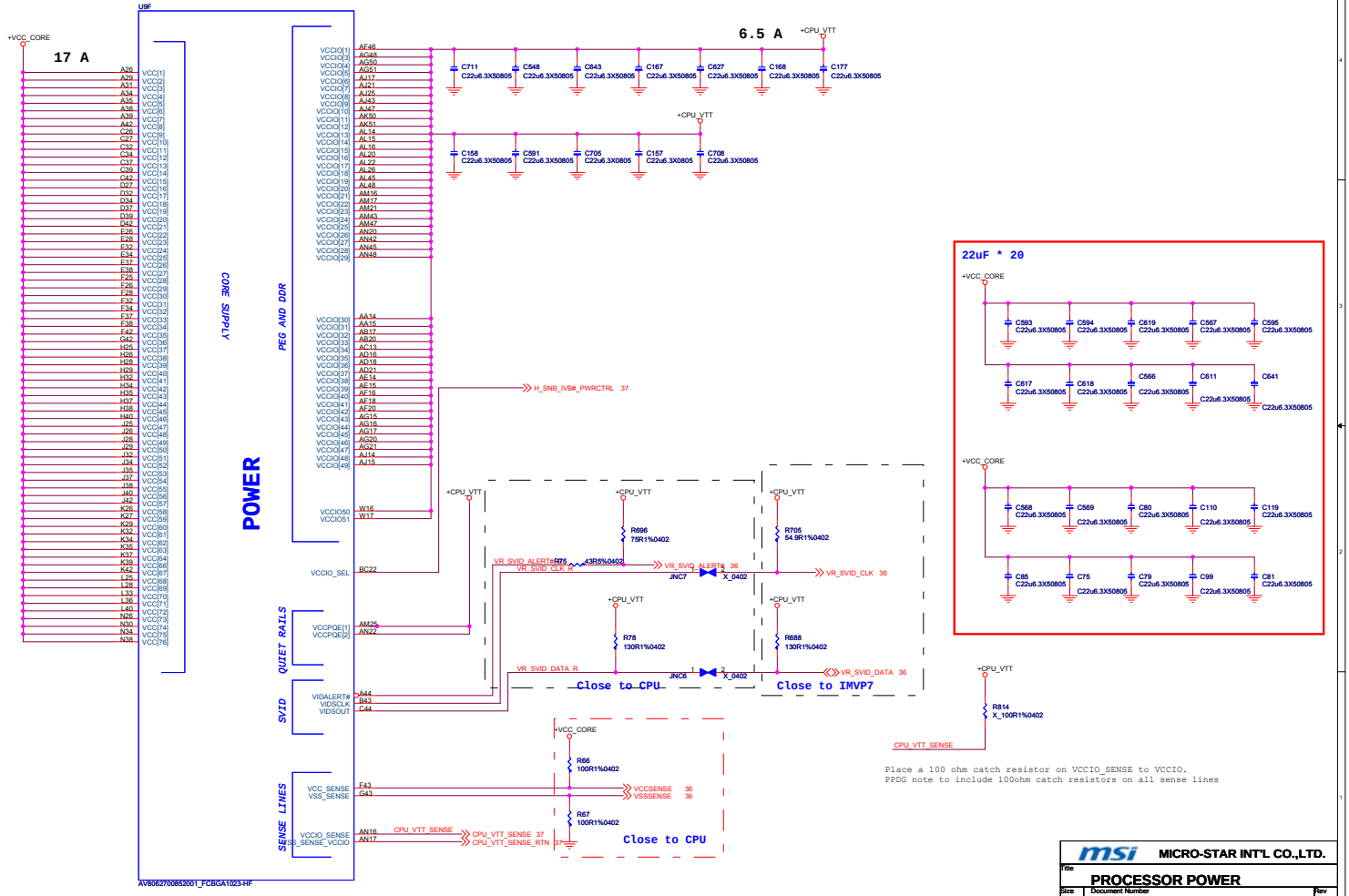
IVYBRIDGE PROCESSOR (POWER)



Title	PROCESSOR POWER
Size	Custom
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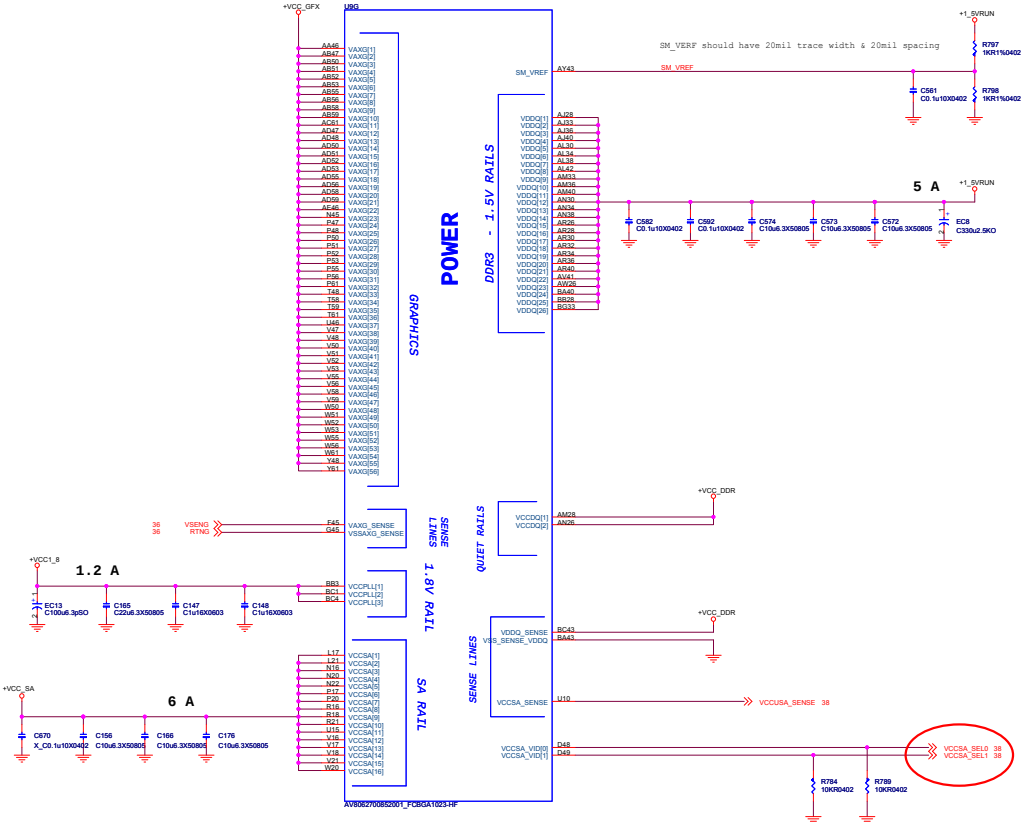
MICRO-STAR INT'L CO.,LTD.

IVYBRIDGE PROCESSOR (GRAPHICS POWER)



R151 10-K pull-down resistor should be placed on the VCCSA VID lines.
This will ensure the VID is 00 prior to VCCIO stability.

MICRO-STAR INT'L CO.,LTD.			
Title: PROCESSOR POWER(GRAPHIC)			
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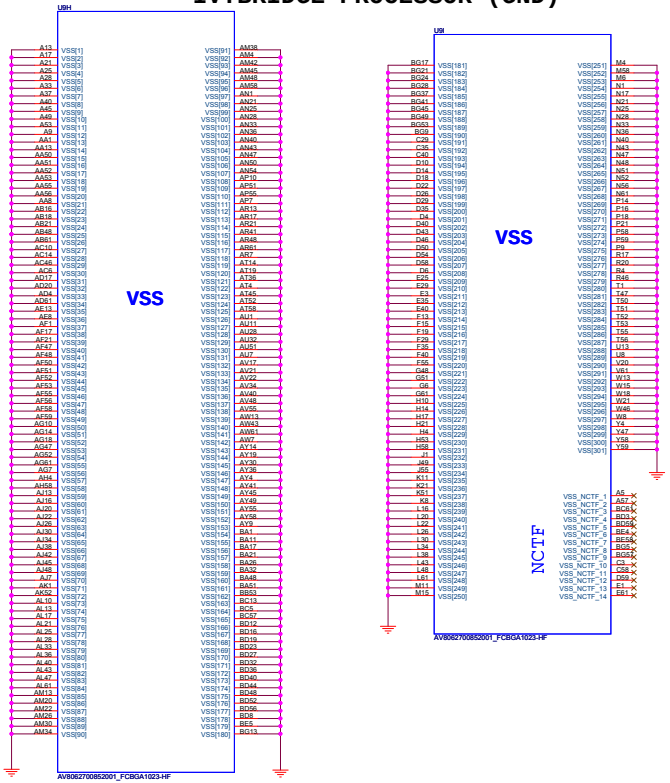
IVYBRIDGE PROCESSOR (GND)



Title	MICRO-STAR INT'L CO.,LTD.
	PROCESSOR GND
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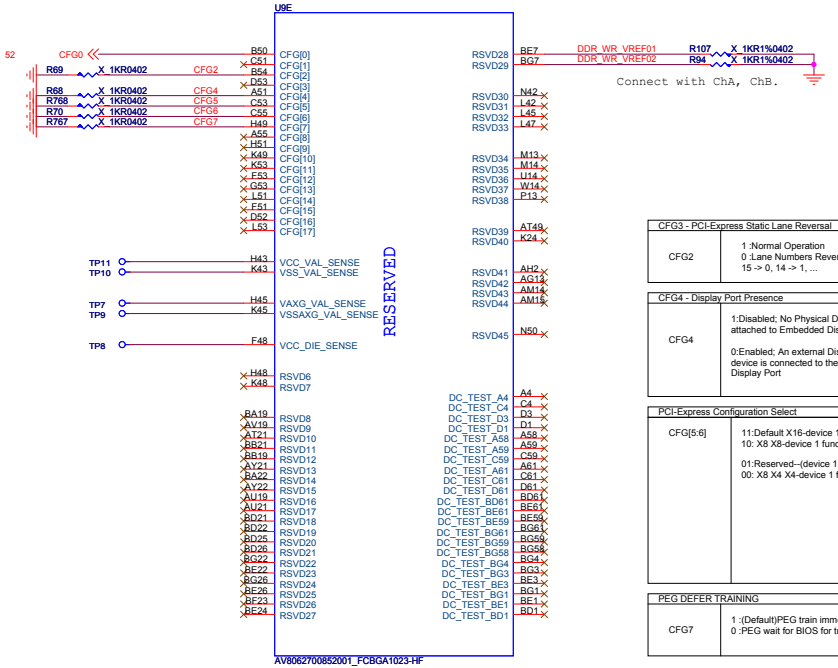
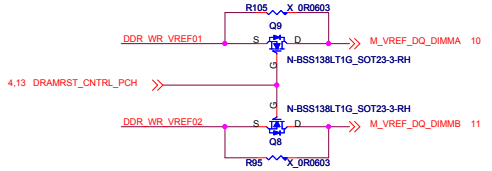
IVYBRIDGE PROCESSOR (RESERVED)



PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:
M1 Implementation: 0 ohm stuff, Mos unstuff



VERF: 20mil trace width & 20mil spacing

CFG3 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

PEG DEFER TRAINING	
CFG7	1 :(Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR RESERVED

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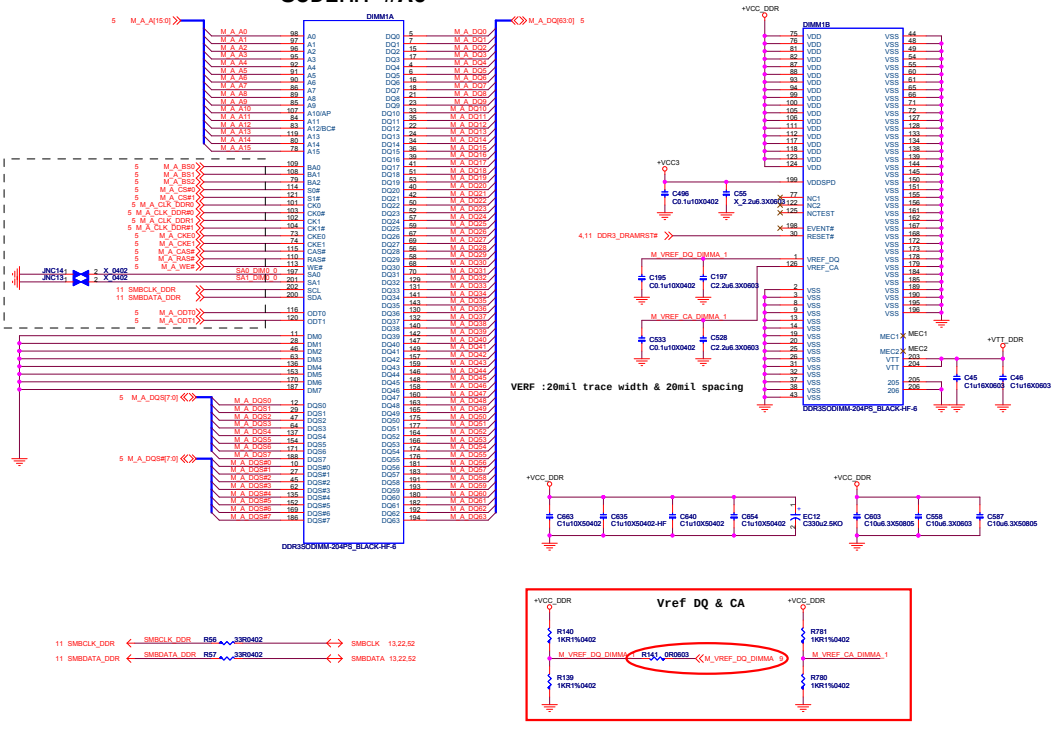
SODIMM #A0

(STD) N13-2040470-L41



Title	DDR3 SODIMM 0		
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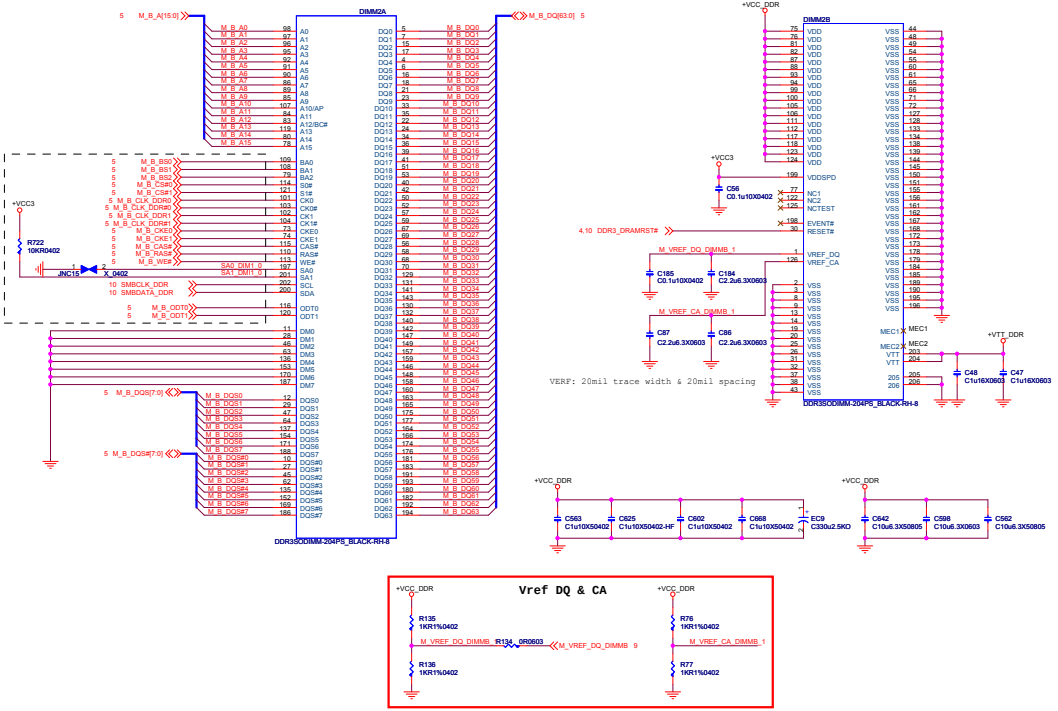
SODIMM #B0

(RVS) M13-2040490-L41



Title	DDR3 SODIMM 1		
Size C	Document Number MS-7807		Rev 1.0
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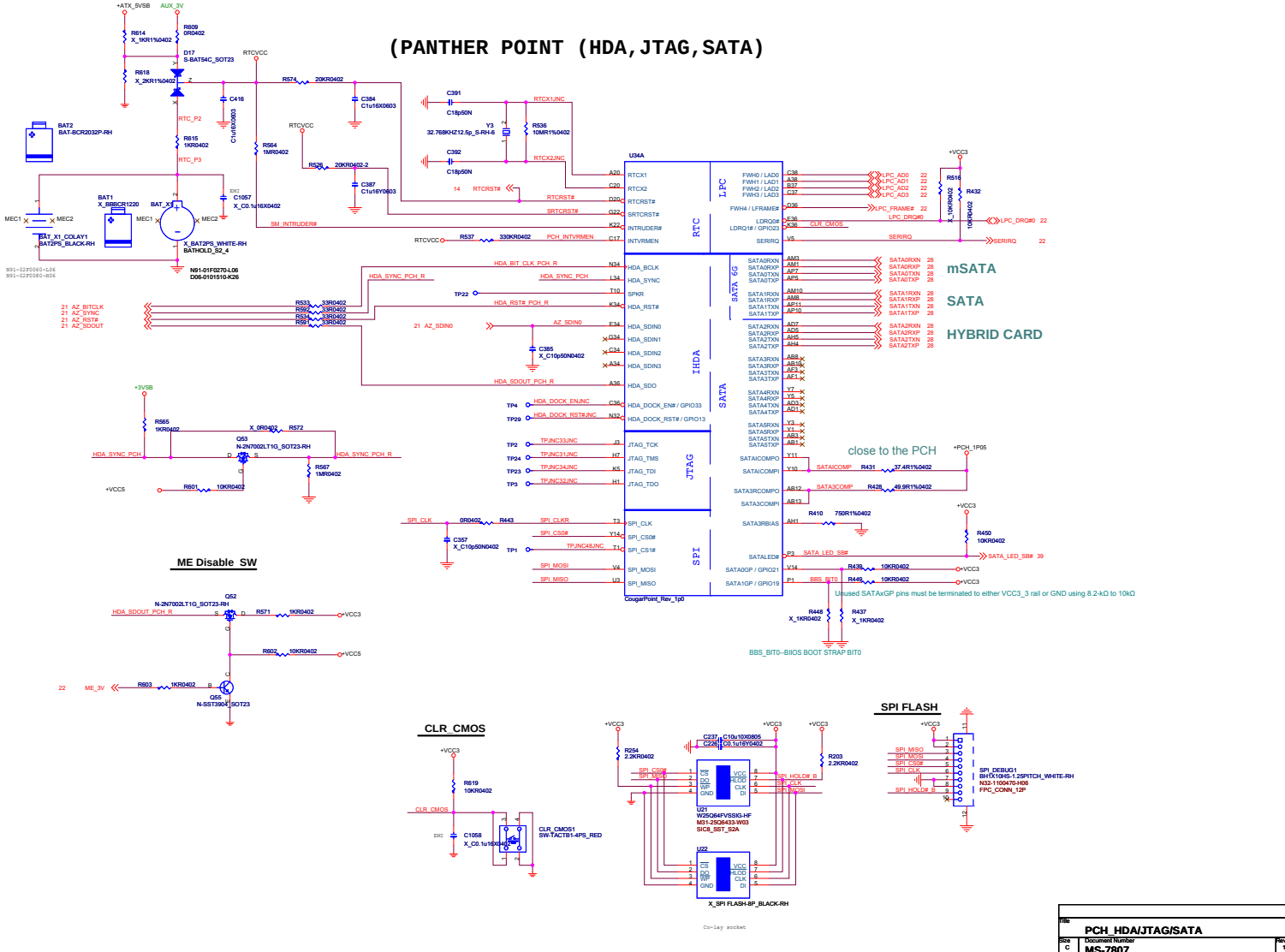
(PANTHER POINT (HDA,JTAG,SATA)



Title	PCH_HDA/JTAG/SATA
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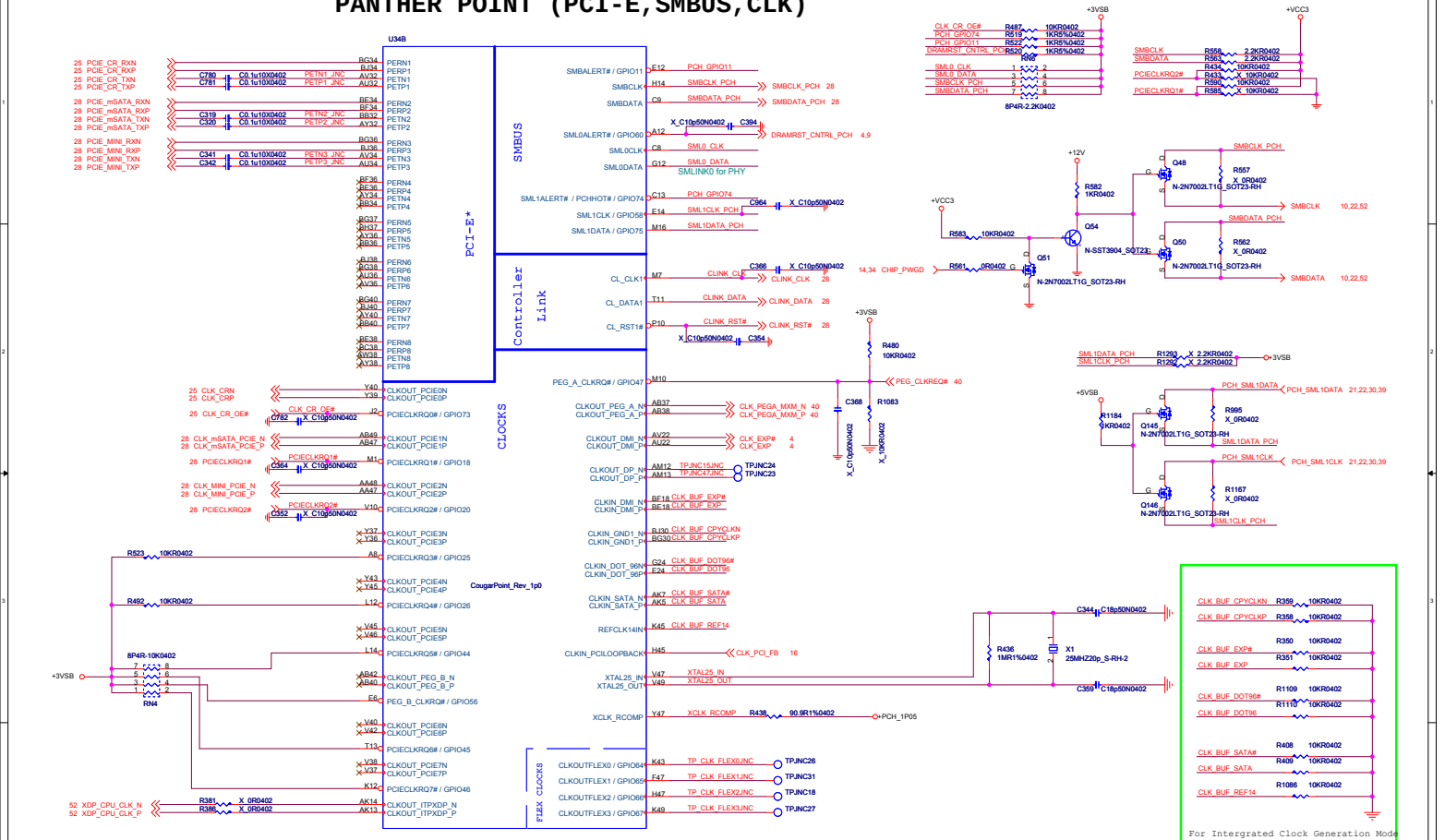
PANTHER POINT (PCI-E,SMBUS,CLK)



Intel Comments:
If CLKREQ# control is not needed, say for a free running clock, DO NOT pull-down signal to GND. This will increase leakage in Sx states.
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

Title	PCH_PCIE/SMBUS/CLK		
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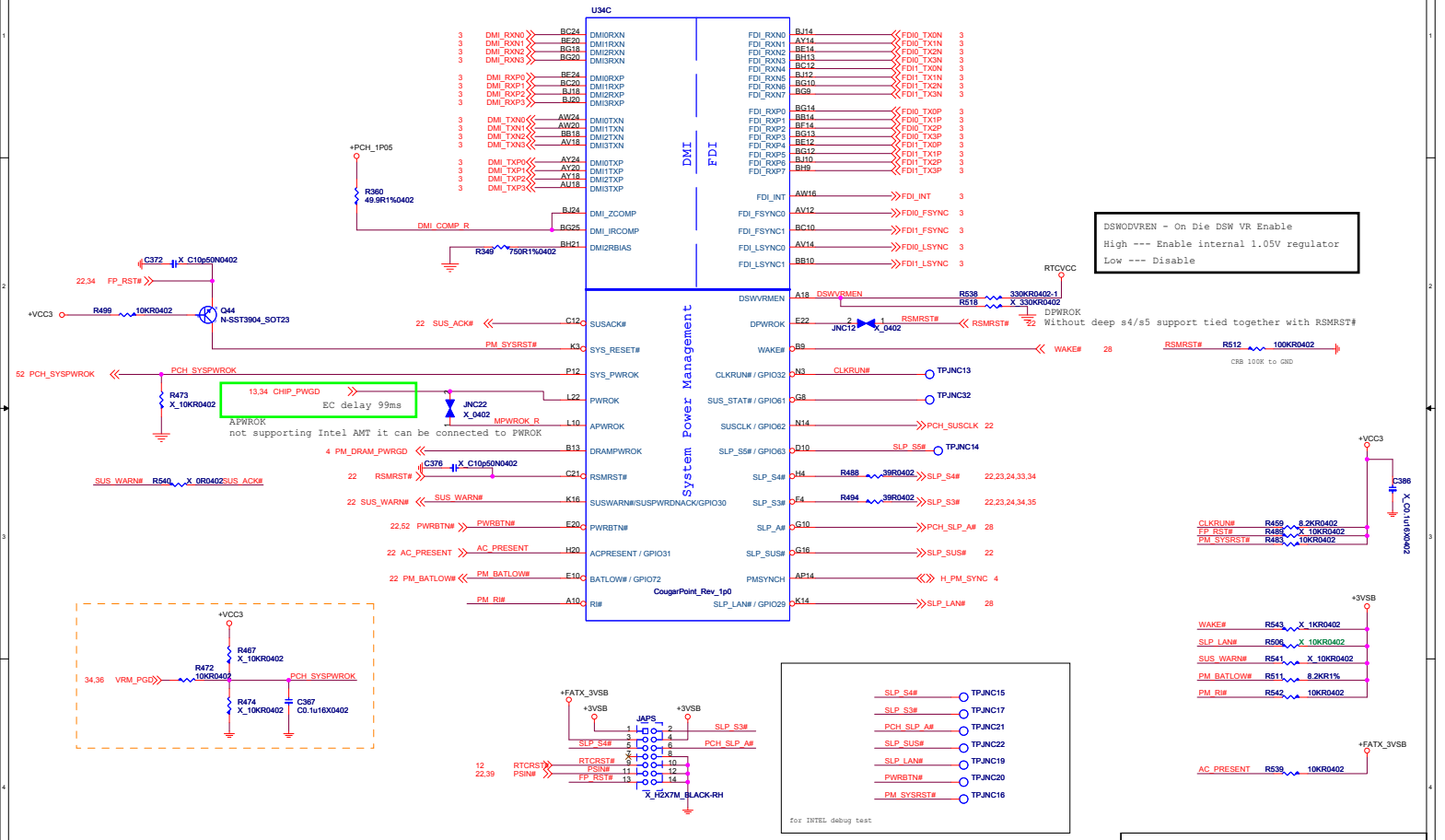
PANTHER POINT (DMI,FDI,GPIO)



Title	PCH_DMI/FDI/GPIO		
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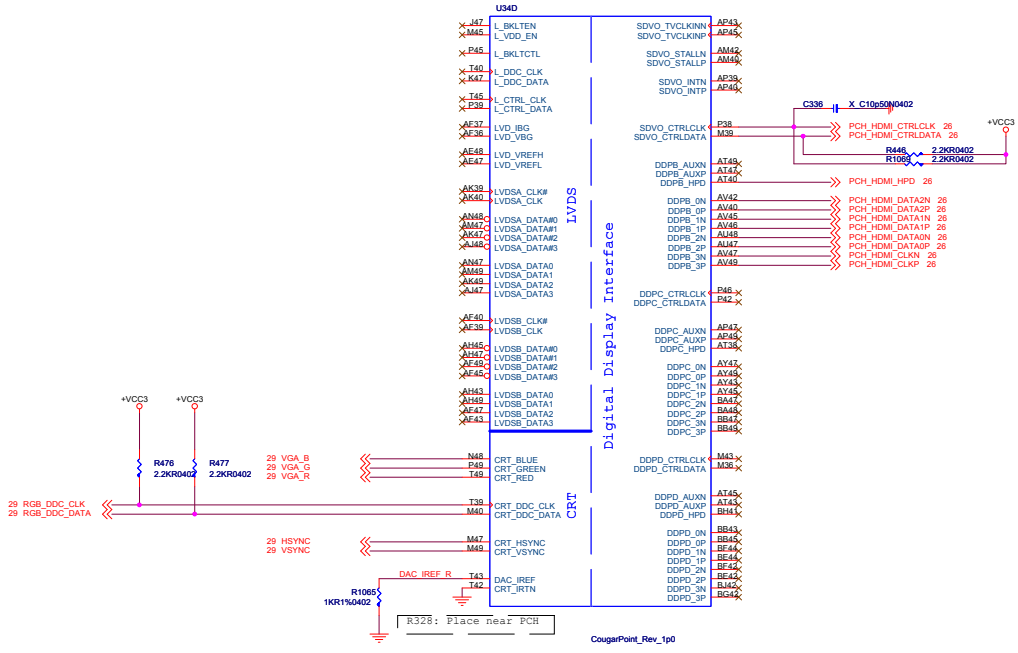
PANTHER POINT (LVDS,DDI)



Title	PCH_LVDS/DDI	
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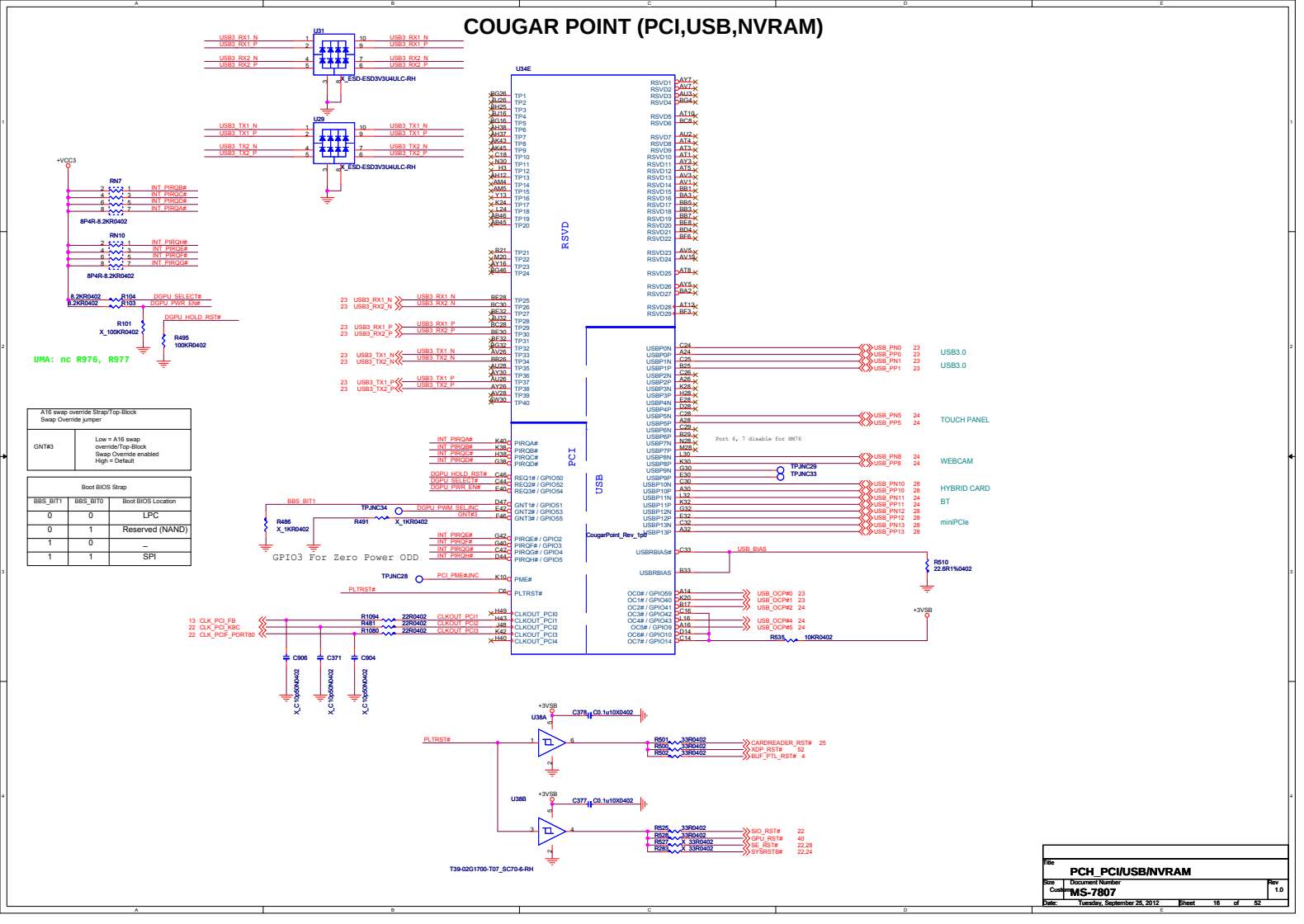
COUGAR POINT (PCI,USB,NVRAM)



A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	_
1	1	SPI

Title	PCH_PCI/USB/NVRAM		
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COUGAR POINT (GPIO,VSS_NCTF,RSVD)

GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN
GPIO57 --If not used,require pull up 3VSUS
GPIO15--Not support AMT,Transport Layer Security Disable(High is support TLS,internal pull-down)
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Define to EDID Select (If not used,require pull down)

Integrated Clock Chip Enable	
ICC_EN	High: use CK505 (buffer through mode) intelnal pull high Low: use PCH(interated clock mode)

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

GPIO28 has a weak internal pull-up.
The internal pull-up is disabled after RSMRST# deasserts.

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

GPIO36 --CRB connector to 3V

FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

PCH EDS1.0:GPl036&37 should not be pulled high when strap is sampled.
PCH EDS1.1:GPl036&37 when pins are unused as SATAGP or GPIO, terminate them to VSS via 8.2k-10k resistor.

U34F

GPIO: BMBUSY# / GPIO0, TACH1 / GPIO1, TACH2 / GPIO6, TACH3 / GPIO7, GPIO8, LAN_PHY_PWR_CTRL / GPIO12, GPIO15, SATA4GP / GPIO16, TACH0 / GPIO17, SCLOCK / GPIO22, GPIO24 / MEM_LED, GPIO27, GPIO28, STP_PCI# / GPIO34, GPIO35, SATA2GP / GPIO36, SATA3GP / GPIO37, SLOAD / GPIO38, SDATAOUT0 / GPIO39, SDATAOUT1 / GPIO48, SATA5GP / GPIO49, GPIO57

CPU/MISC: TACH4 / GPIO68, TACH5 / GPIO69, TACH6 / GPIO70, TACH7 / GPIO71, A20GATE, PECI, RCIN#, PROCPWRGD, THRMTRIP#, INIT3_3V#, DF_TVS, TS_VSS1, TS_VSS2, TS_VSS3, TS_VSS4, NC_1

NCTF: VSS_NCTF_1 … VSS_NCTF_14, VSS_NCTF_15 … VSS_NCTF_32

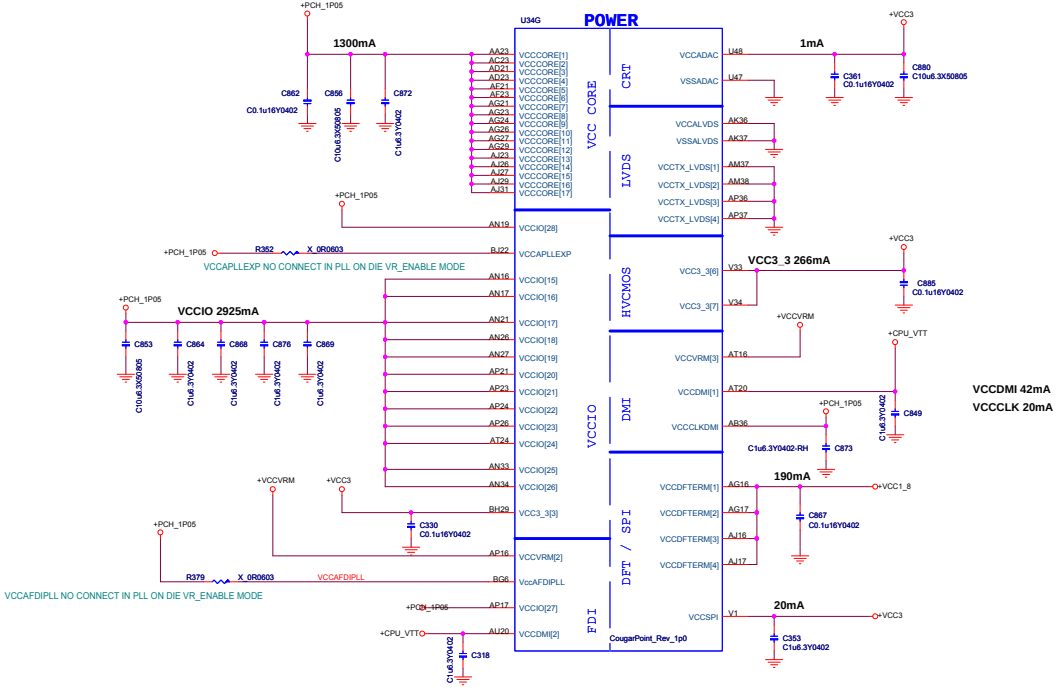
CougarPoint_Rev_1p0

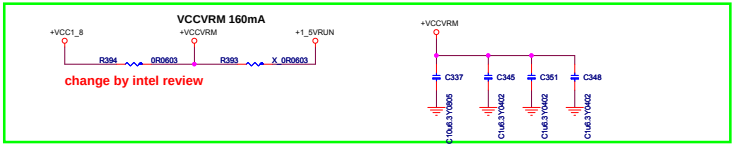
DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High

Intel Comments:
Reserve 0 ohm option in these pins
pins AH8, AK11, AH10 & AK10) to GND.

CRB_SV_DET	
GPIO39	High: External GFX
	Low: Internal GFX

COUGAR POINT (POWER)





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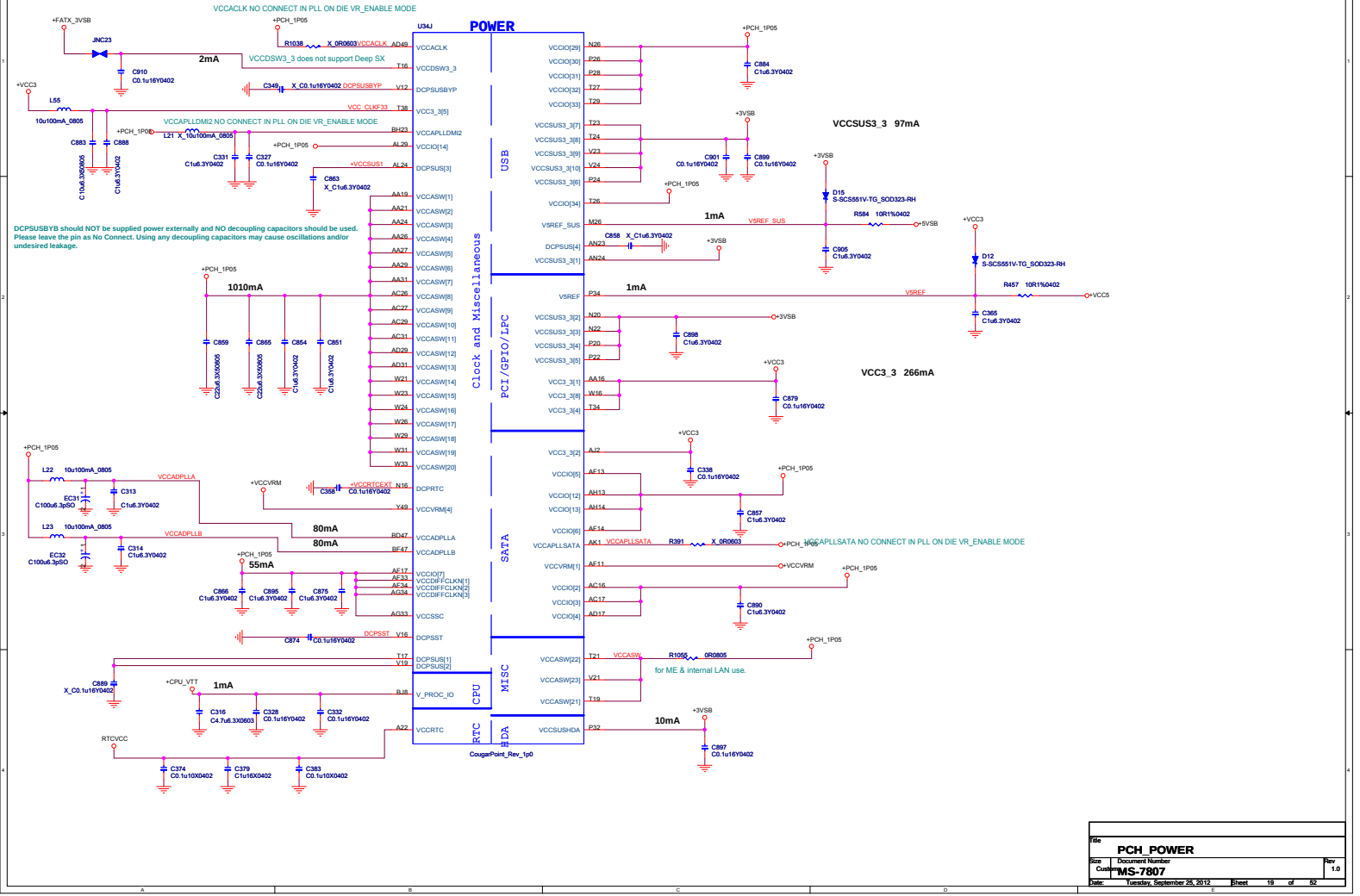
COUGAR POINT (POWER)



Title	PCH_POWER		
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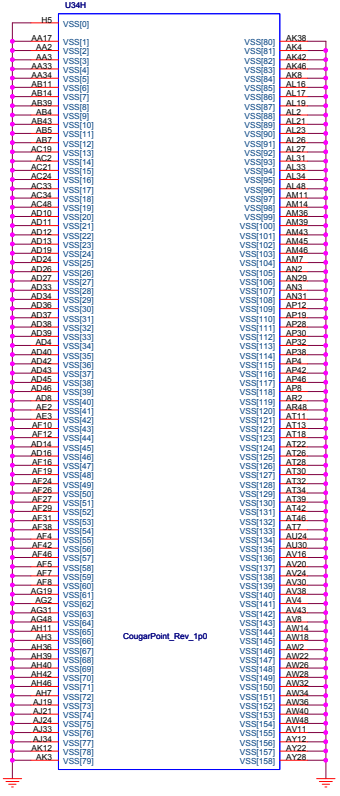
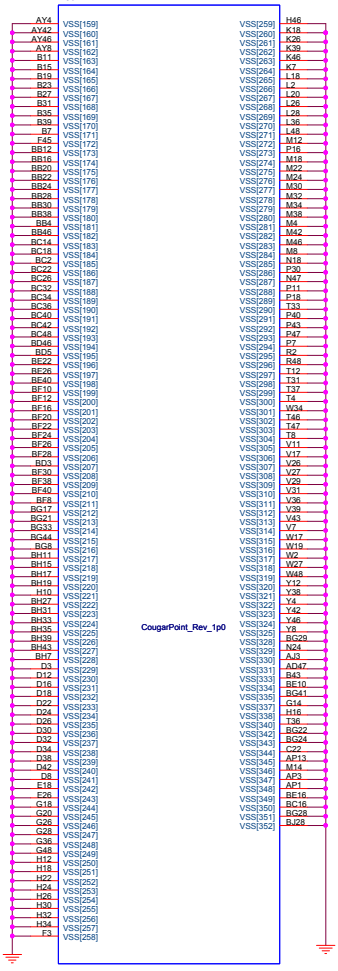
Cougar Point (GND)





Title	PCH_GND	
Size: Custom	Document Number: MS-7807	Rev: 1.0
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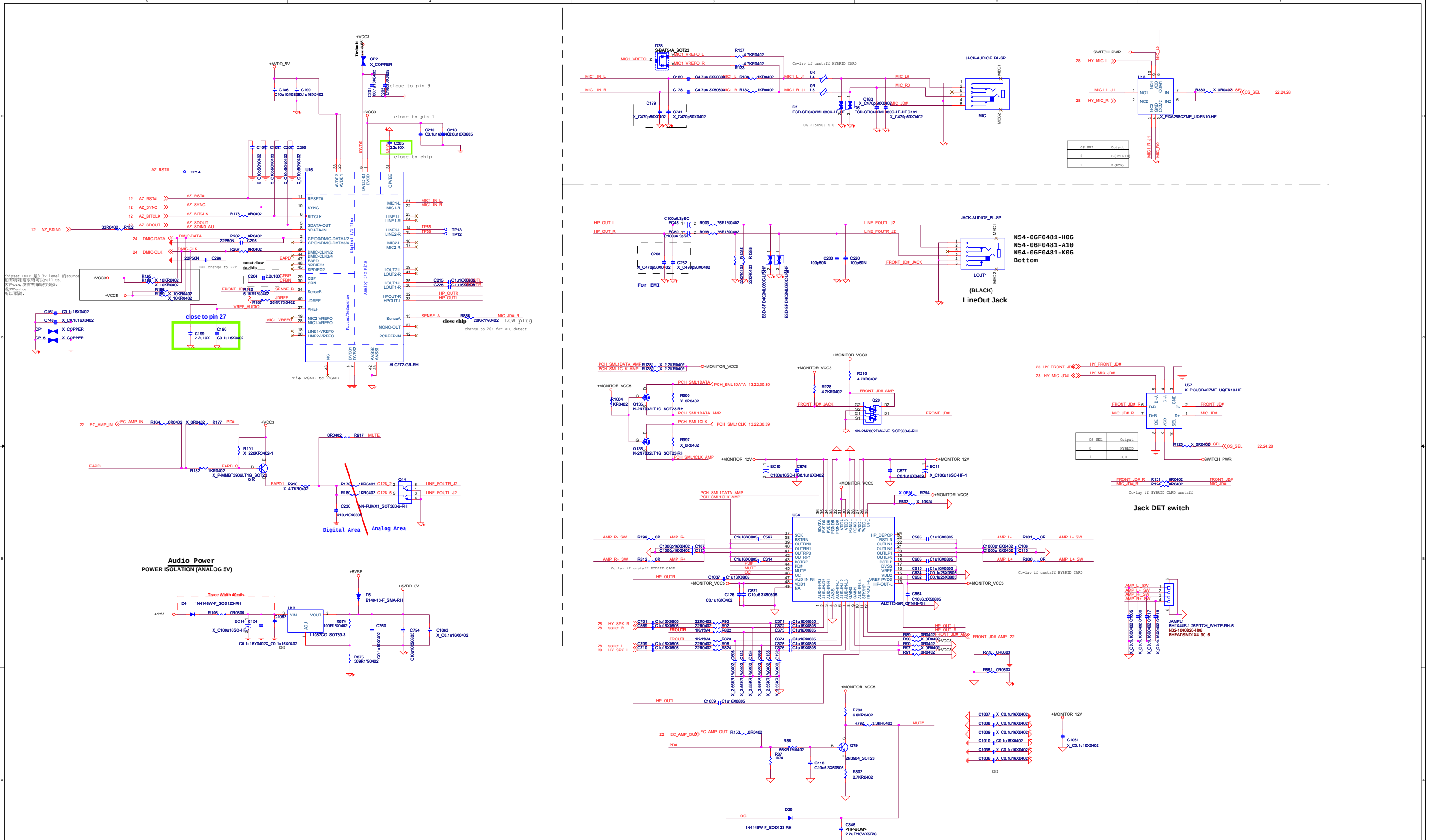

MICRO-STAR INT'L CO.,LTD

MS-7807

Document Description: Audio Codec - REALTEK/ALC272 + ALC113

Size: D

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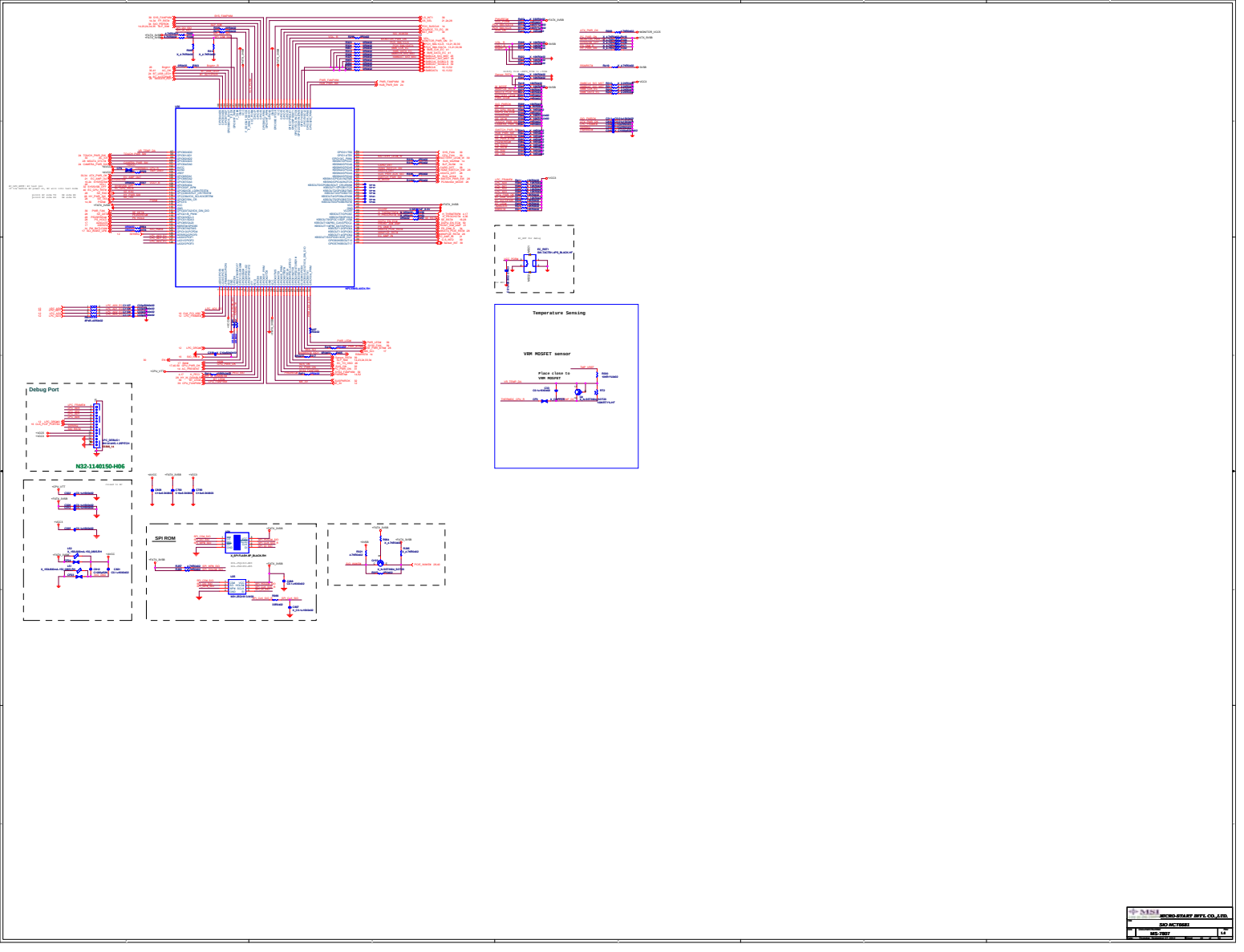
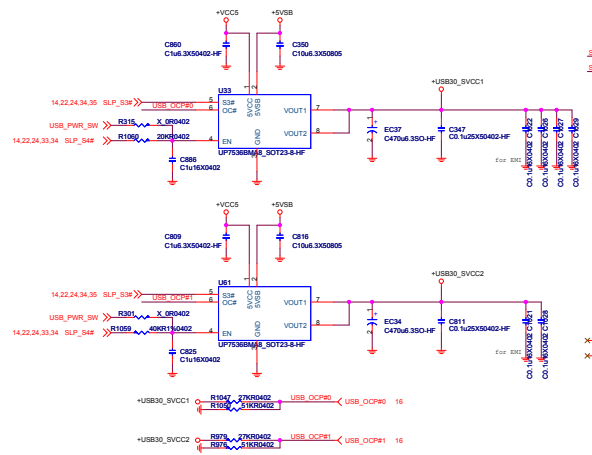
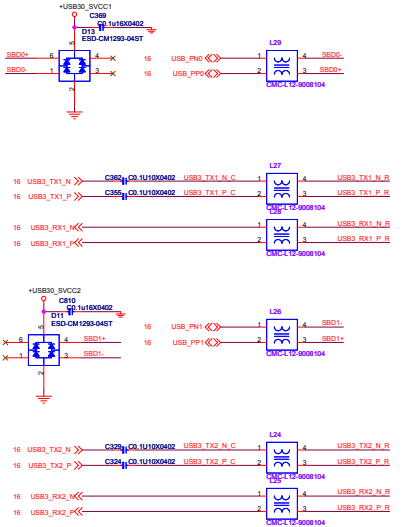


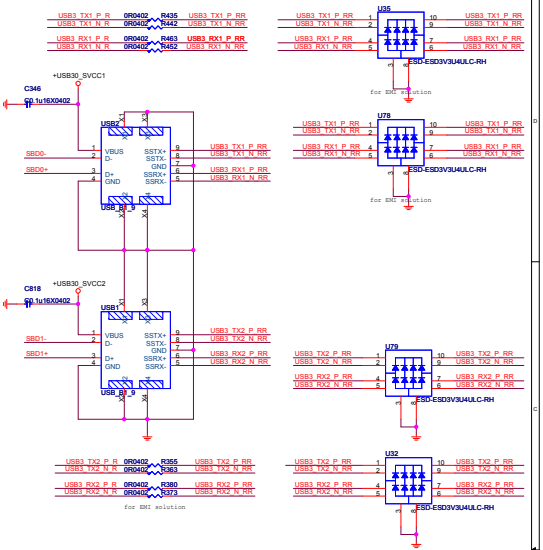
MICRO-STAR INT'L CO., LTD.	
SIO NCT6681	
MS-7897	1.0

POWER CIRCUIT FOR USB PORT 1, 2



RIGHT SIDE USB CONNECTOR FOR USB3.0 PORT 1, 2





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Size: C	Document Description: USB 3.0 Right Side	Rev: 1.0
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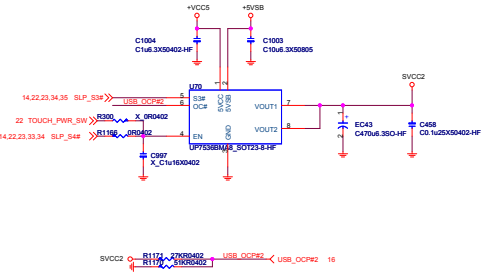
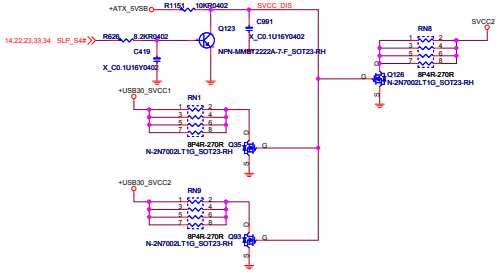
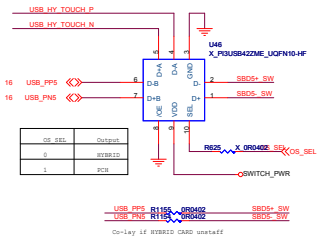
POWER CIRCUIT FOR USB PORT 4, 5



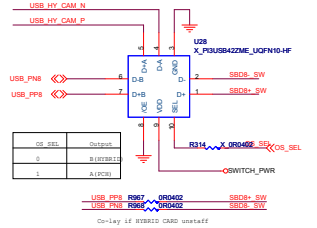
USB power discharge circuit



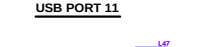
USB PORT 5



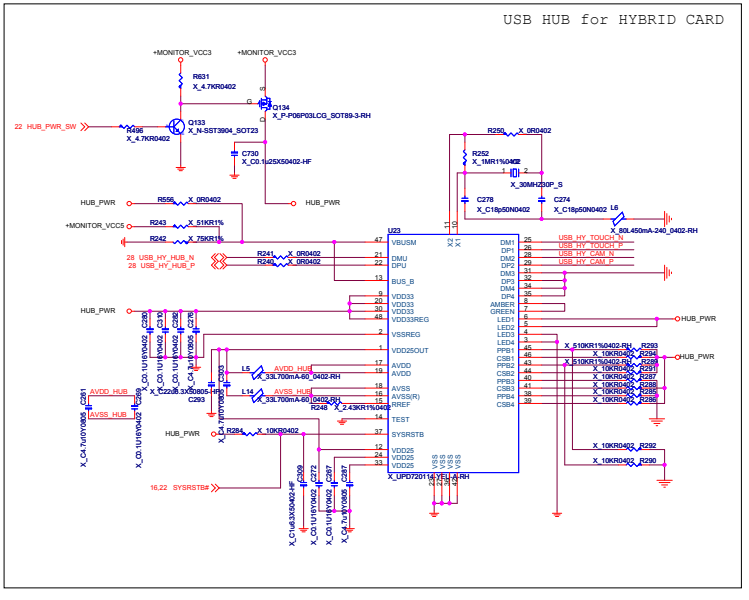
USB PORT 8



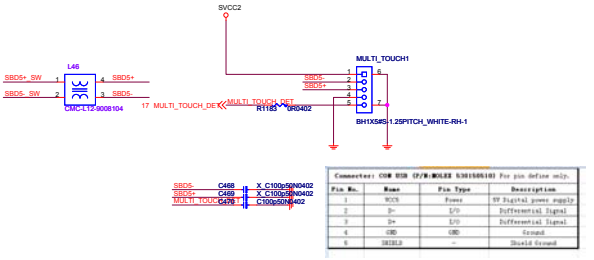
USB PORT 11



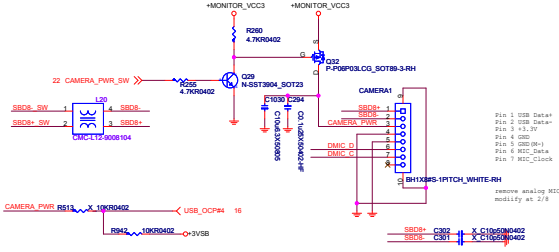
USB HUB for HYBRID CARD



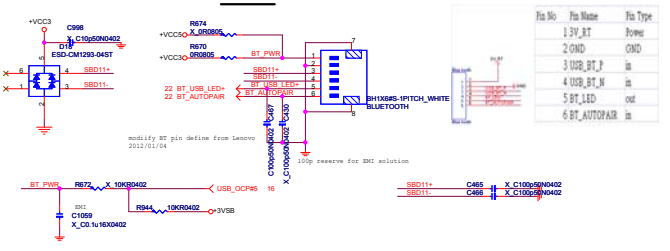
Touch board



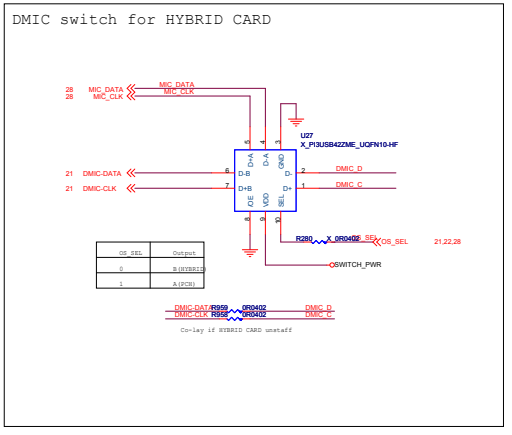
CAMERA



BT



DMIC switch for HYBRID CARD



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: USB 2.0 DEVICE/ PIN HEADER
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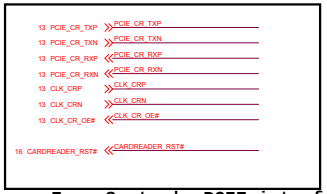
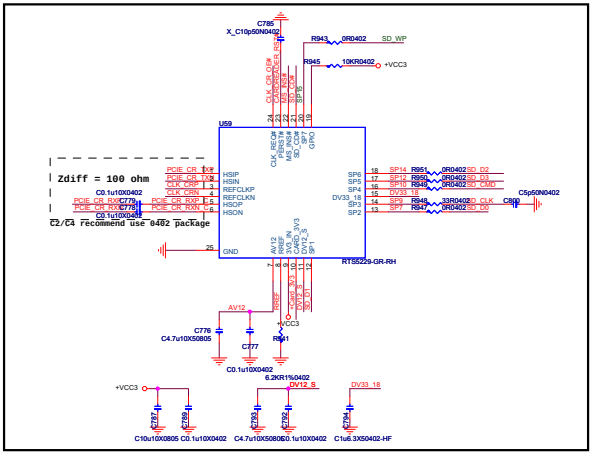
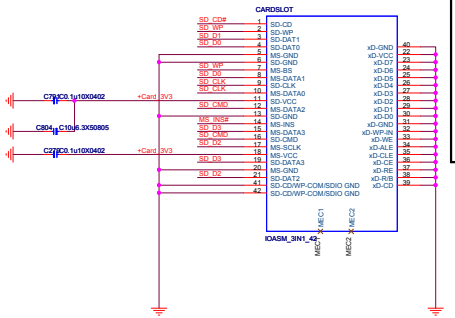
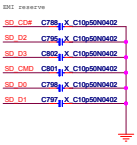


From System's PCIE interface







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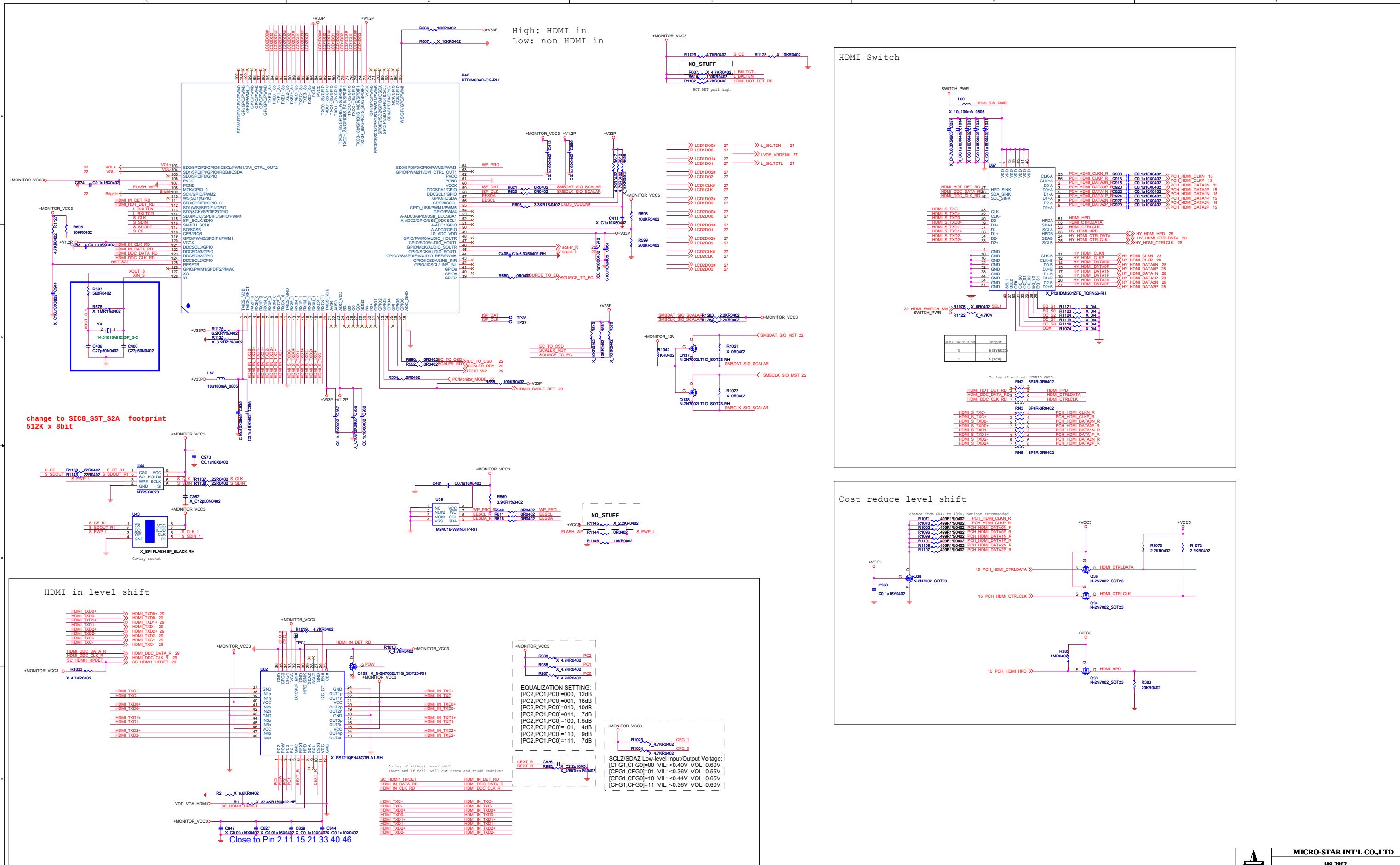

MICRO-STAR INT'L CO.,LTD

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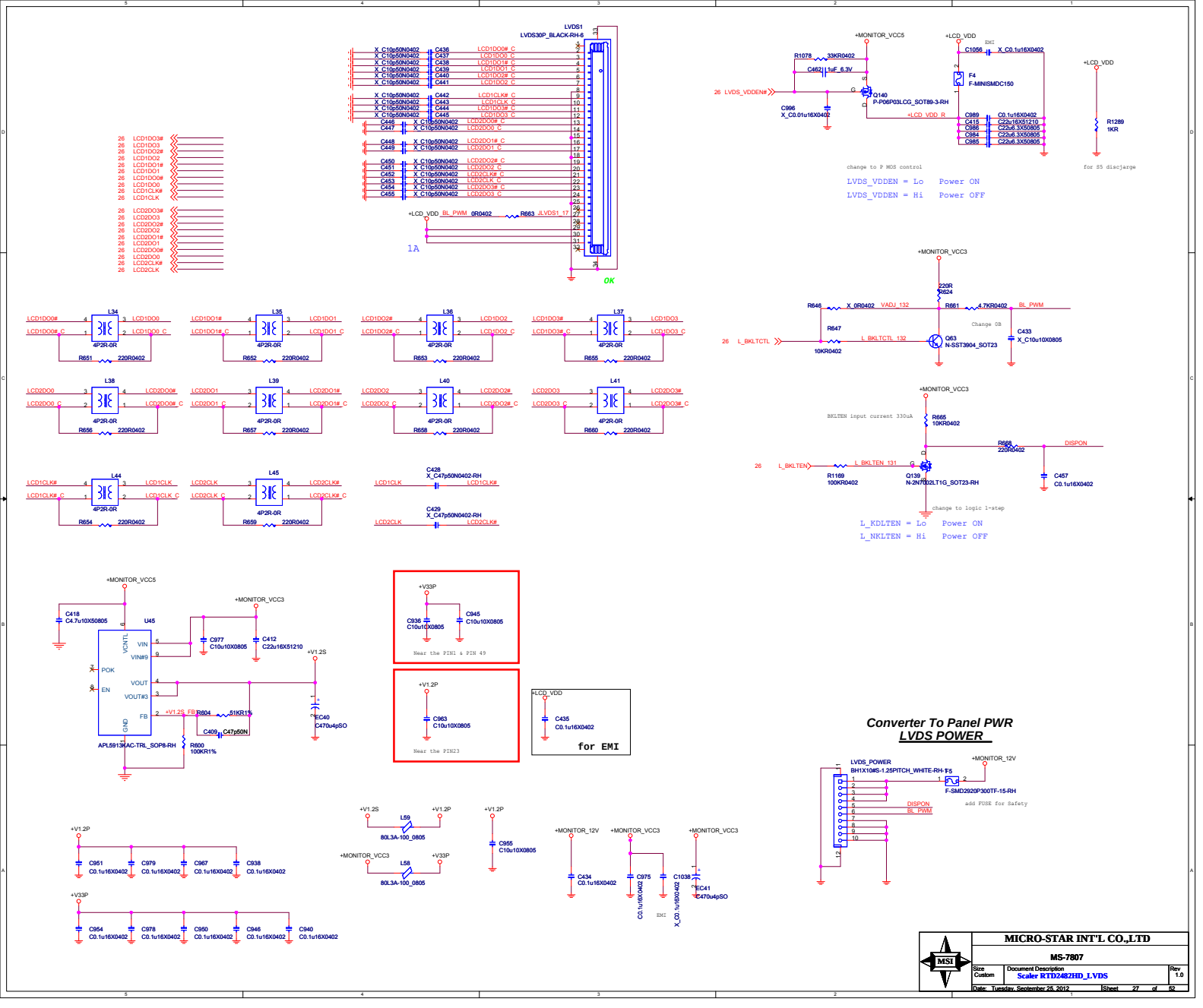
LVDS1
LVDS30P_BLACK-RH-6
+LCD_VDD
BL_PWM
0R0402
R663
JLVDS1_17
1A
OK
+MONITOR_VCC5
+LCD_VDD
R1078
33KR0402
C462
1uF_6.3V
26 LVDS_VDDEN#
Q140
P-P06P03LCG_SOT89-3-RH
C996
X_C0.01u16X0402
C1056
X_C0.1u16X0402
F4
F-MINISMDC150
C989
C415
C986
C984
C985
C0.1u16X0402
C22u18X51210
C22u6.3X50805
C22u6.3X50805
C22u6.3X50805
R1289
1KR
change to P MOS control
for S5 discjarge
LVDS_VDDEN = Lo Power ON
LVDS_VDDEN = Hi Power OFF
+MONITOR_VCC3
R624
220R
R646
X_0R0402
VADJ_132
R661
4.7KR0402
BL_PWM
Change 0B
R647
10KR0402
26 L_BKLTCTL
L_BKLTCTL_132
Q63
N-SST3904_SOT23
C433
X_C10u10X0805
BKLTEN input current 330uA
R665
10KR0402
R666
220R0402
DISPON
26 L_BKLTEN
L_BKLTEN_131
R1169
100KR0402
Q139
N-2N7002LT1G_SOT23-RH
C457
C0.1u16X0402
change to logic 1-step
L_KDLTEN = Lo Power ON
L_NKLTEN = Hi Power OFF
L34
L35
L36
L37
4P2R-0R
R651
R652
R653
R655
220R0402
L38
L39
L40
L41
R656
R657
R658
R660
L44
L45
R654
R659
C428
X_C47p50N0402-RH
C429
X_C47p50N0402-RH
+MONITOR_VCC5
+MONITOR_VCC3
C418
C4.7u10X50805
U45
APL5913KAC-TRL_SOP8-RH
VCNTL
VIN
VIN#9
POK
EN
VOUT
VOUT#3
FB
GND
C977
C10u10X0805
C412
C22u16X51210
+V1.2S
+V1.2S_FB
R604
51KR1%
C409
C47p50N
R600
100KR1%
EC40
C470u4pSO
+V33P
C936
C10u10X0805
C945
C10u10X0805
Near the PIN1 & PIN 49
+V1.2P
C963
C10u10X0805
Near the PIN23
+LCD_VDD
C435
C0.1u16X0402
for EMI
Converter To Panel PWR
LVDS POWER
LVDS_POWER
BH1X10#S-1.25PITCH_WHITE-RH-T5
+MONITOR_12V
F-SMD2920P300TF-15-RH
add FUSE for Safety
DISPON
BL_PWM
+V1.2S
+V1.2P
L59
80L3A-100_0805
+MONITOR_VCC3
+V33P
L58
80L3A-100_0805
C955
C10u10X0805
+MONITOR_12V
+MONITOR_VCC3
+MONITOR_VCC3
C434
C0.1u16X0402
C975
C0.1u16X0402
C1038
X_C0.1u16X0402
EC41
C470u4pSO
EMI
C951
C979
C967
C938
C0.1u16X0402
C954
C978
C950
C946
C940
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Document Description
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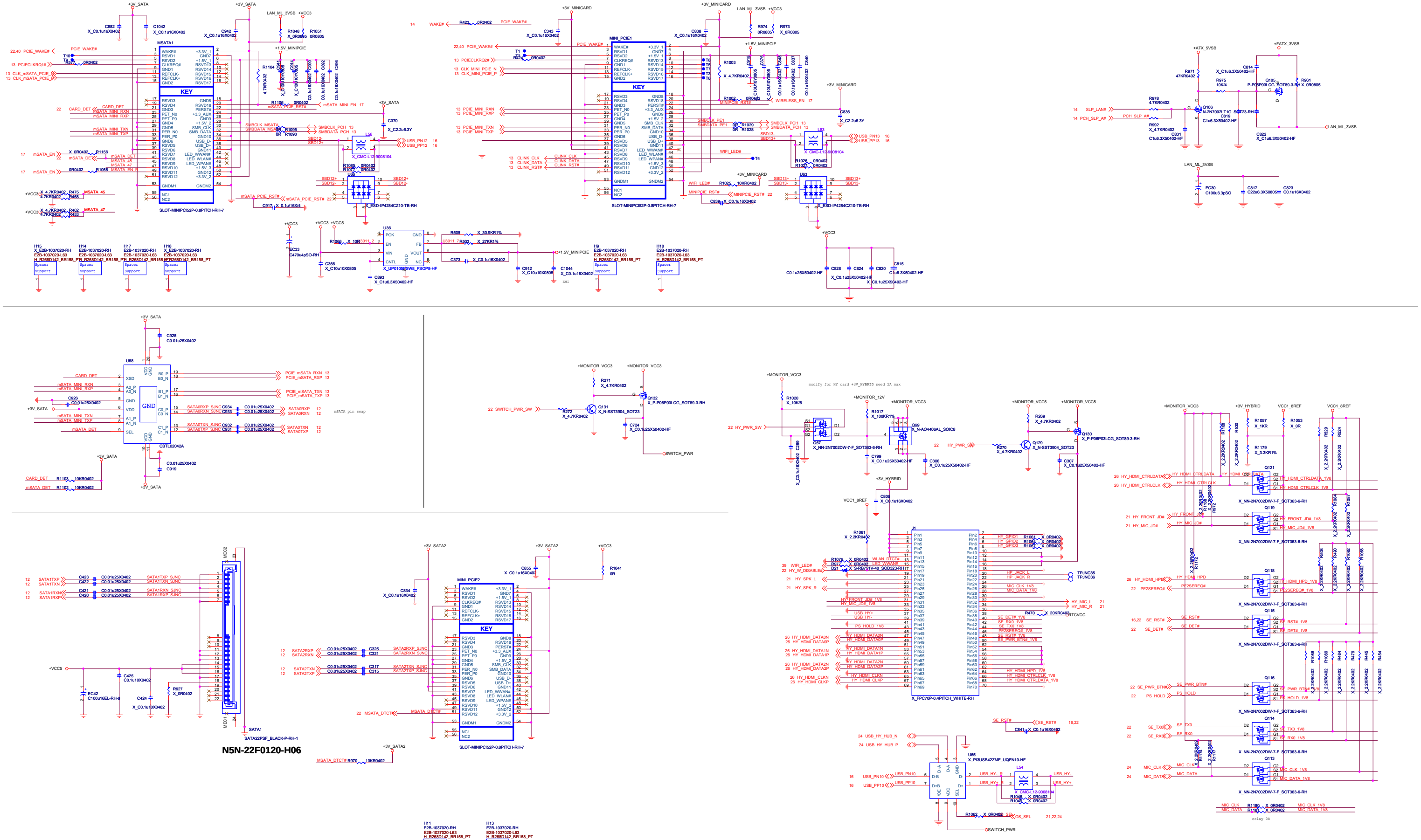

MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7807		
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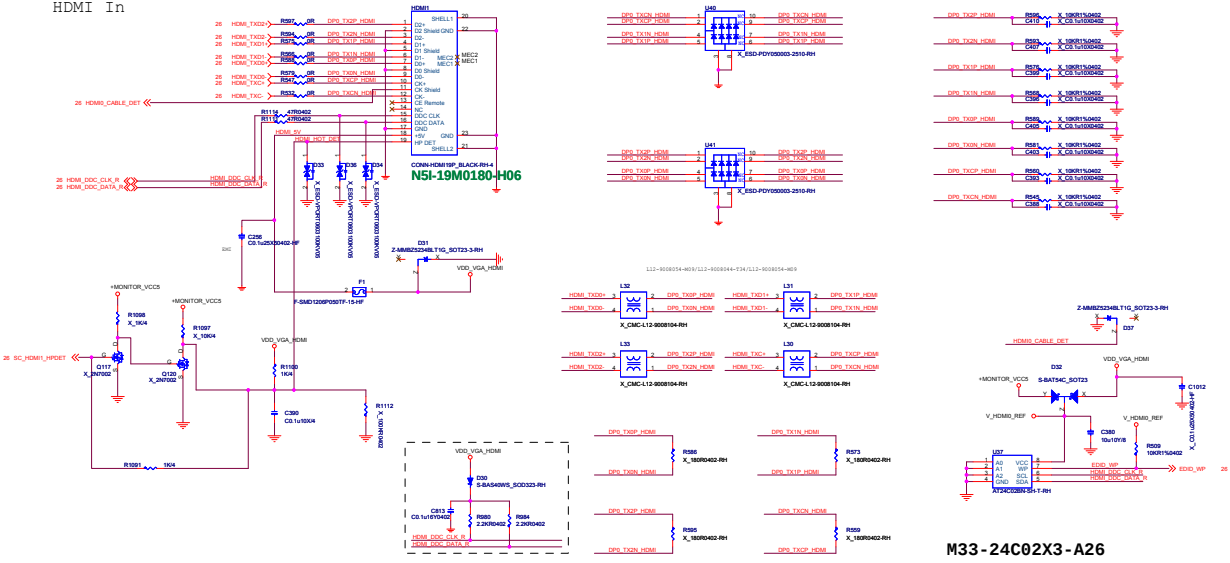
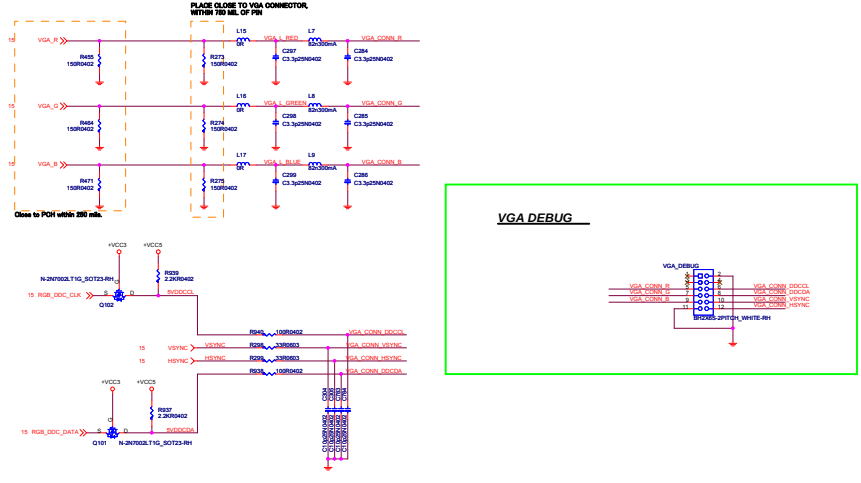
HDMI In



VGA Debug



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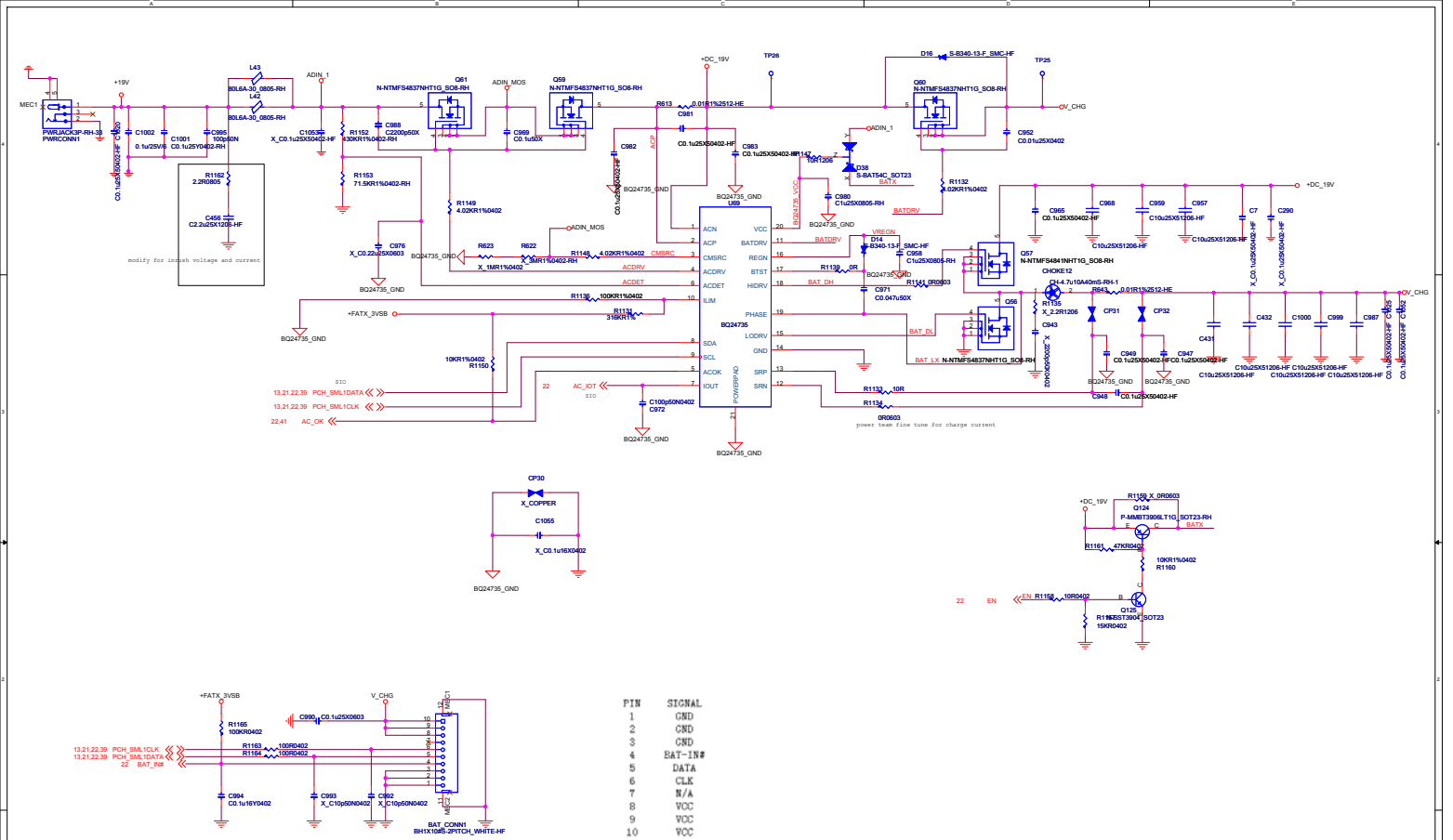

PIN	SIGNAL
1	GND
2	GND
3	GND
4	BAT-IN#
5	DATA
6	CLK
7	N/A
8	VCC
9	VCC
10	VCC

0719: change to pin header N32-1100460-H06
and Pin define

MICRO-STAR INT'L CO.,LTD.			
Title: CHARGE/Battery Select			
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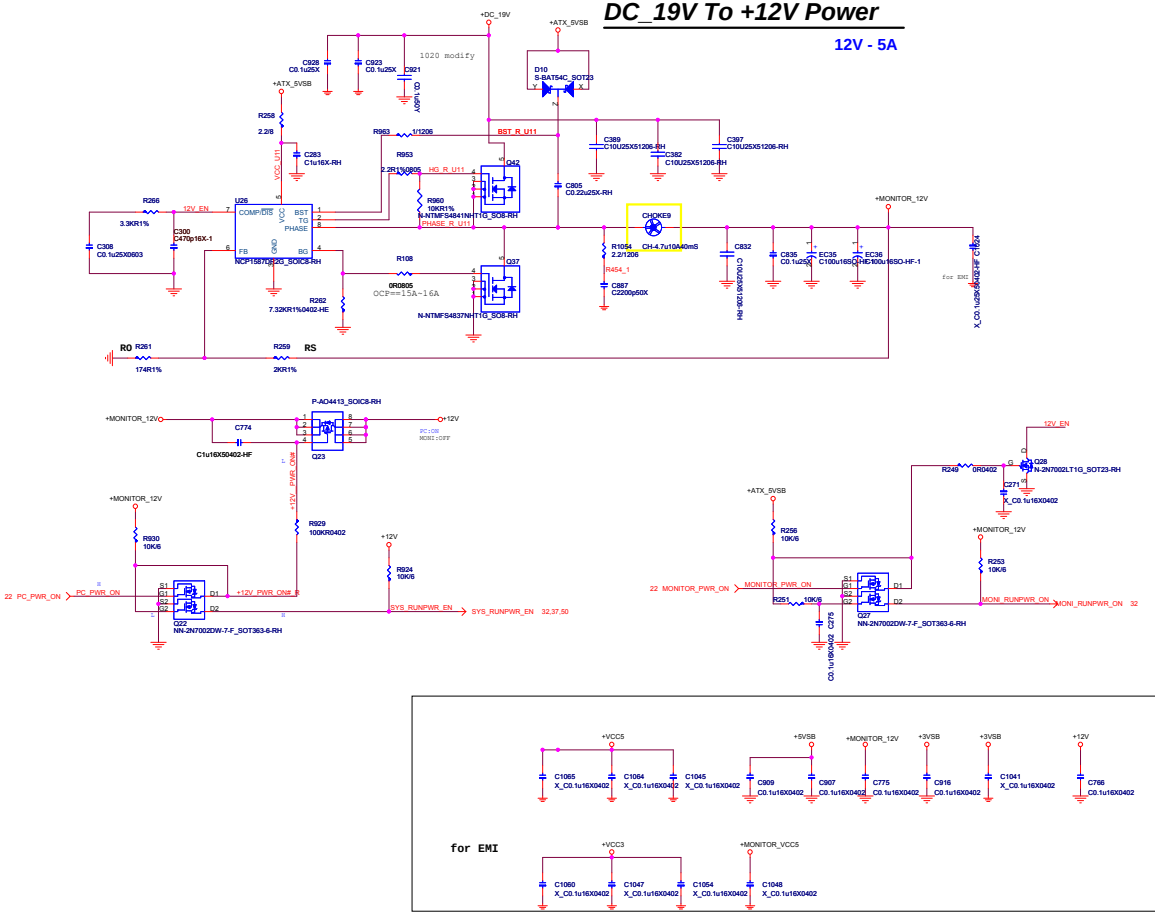

Title	DC Source Power	
Size C	Document Number MS-7807	Rev 1.0
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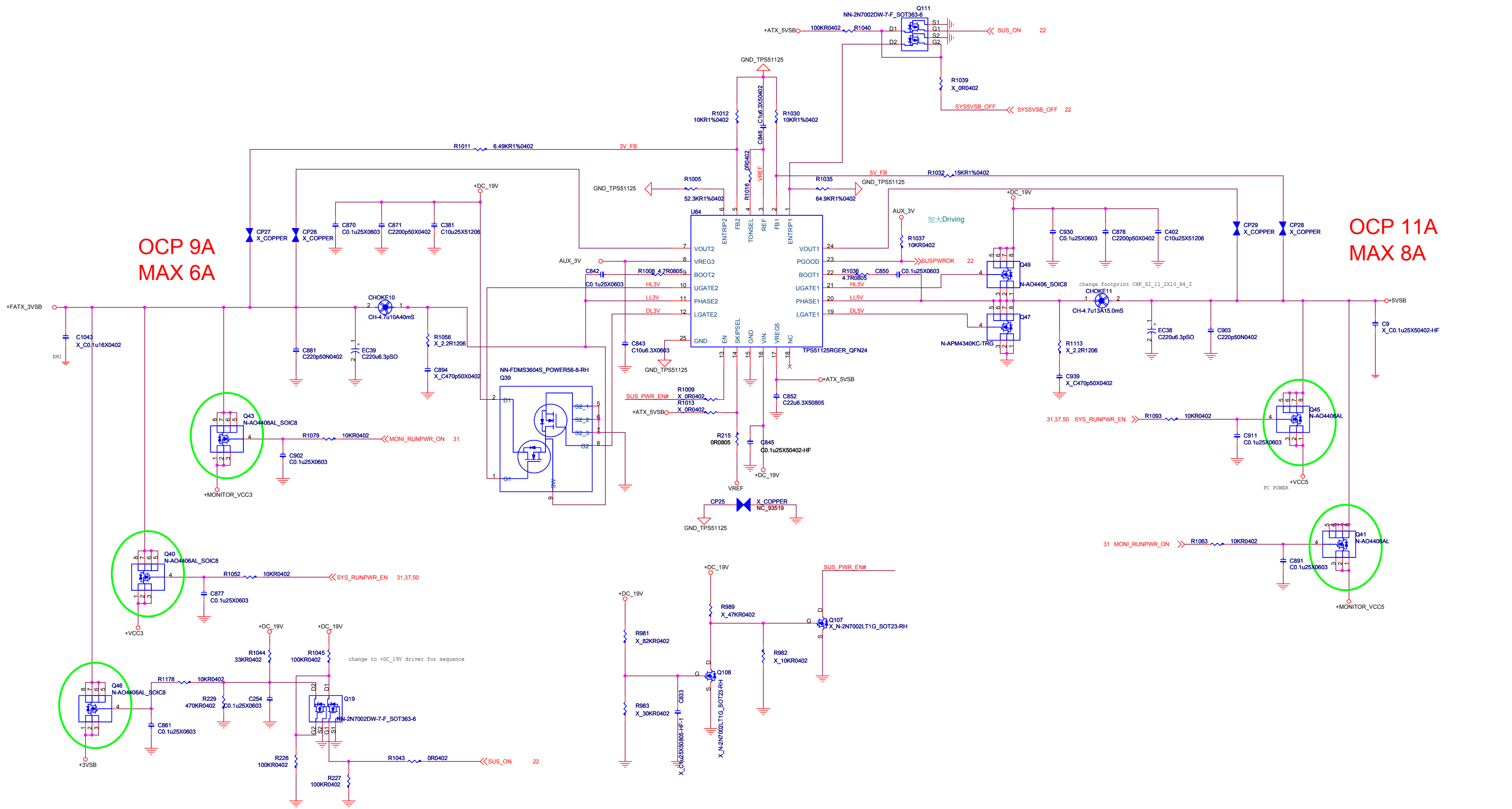

MICRO-STAR INT'L CO.,LTD.

Title	System Power
Size	A2
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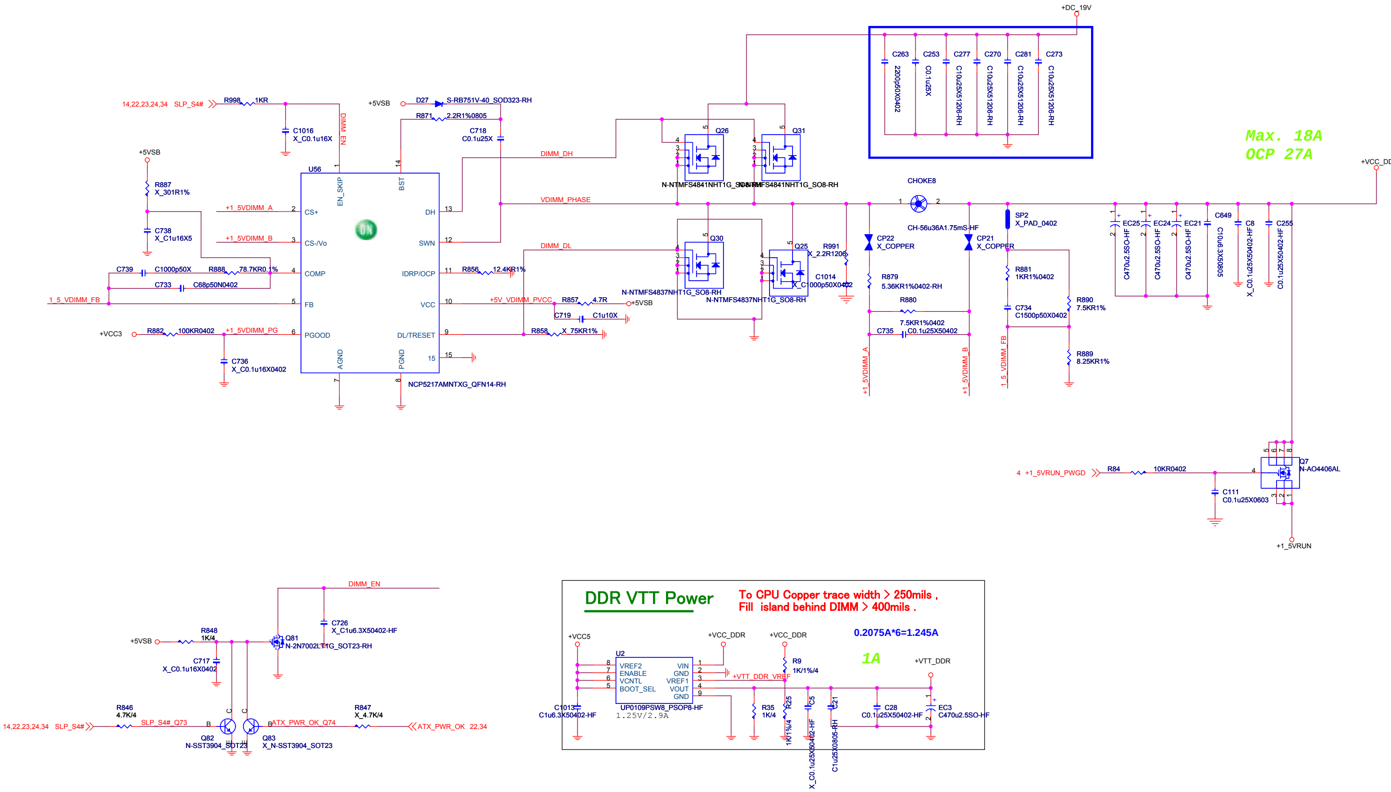

Title	DDR Power	
Size C	Document Number MS-7807	Rev 1.0
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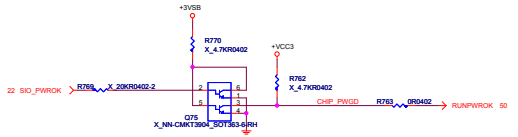
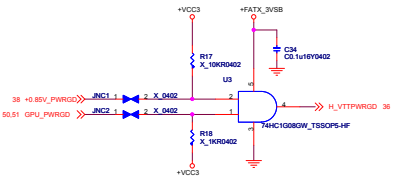
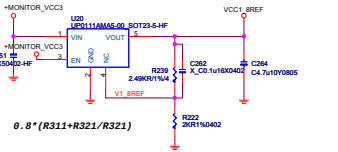


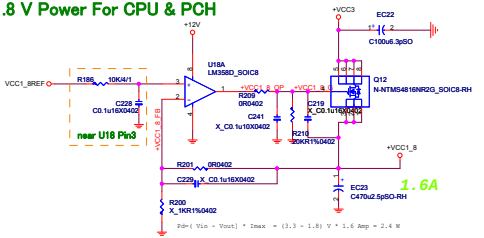
All SYS PWRGD



VCC1_8REF

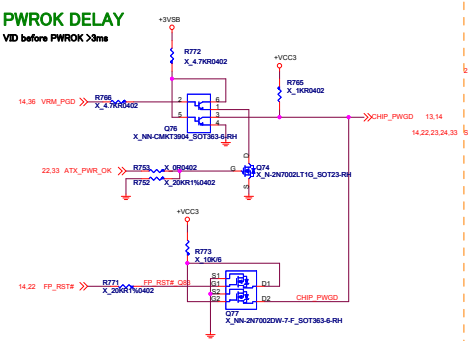


1.8 V Power For CPU & PCH



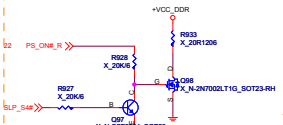
PWROK DELAY

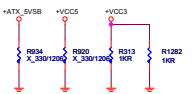
VID before PWROK >3ms

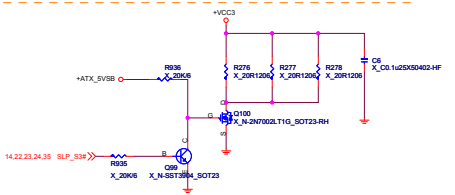


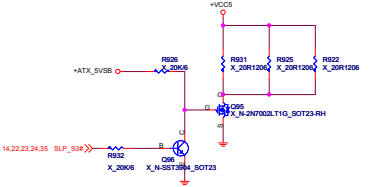
Update from SLP_S3# to VRM_PGD

Discharge Circuit









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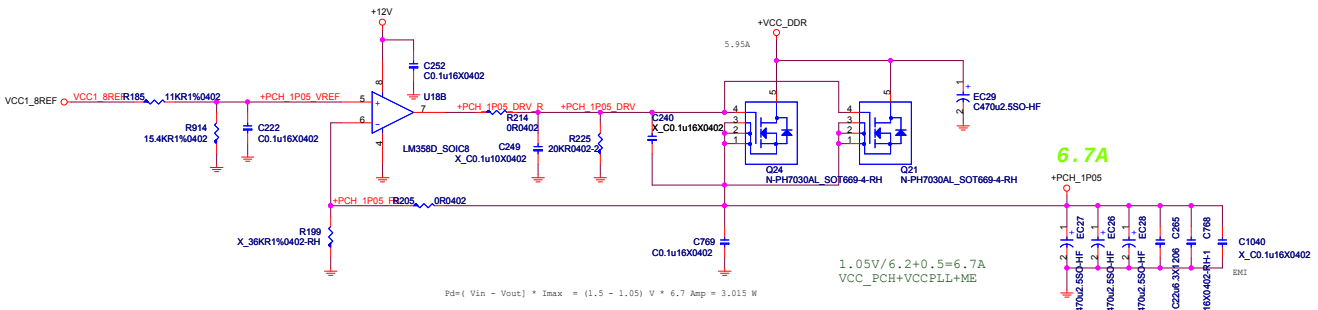
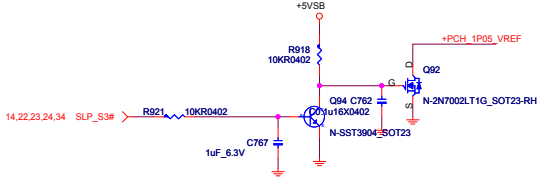
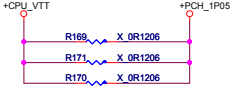
PCH Core Power





+PCH_1P05 =1.05 V TO PCH



On designs that do not support Intel ME, a single 1.05 V VR supply may be used for both the VCCIO (to the processor) and VCCIO_PCH power rails.

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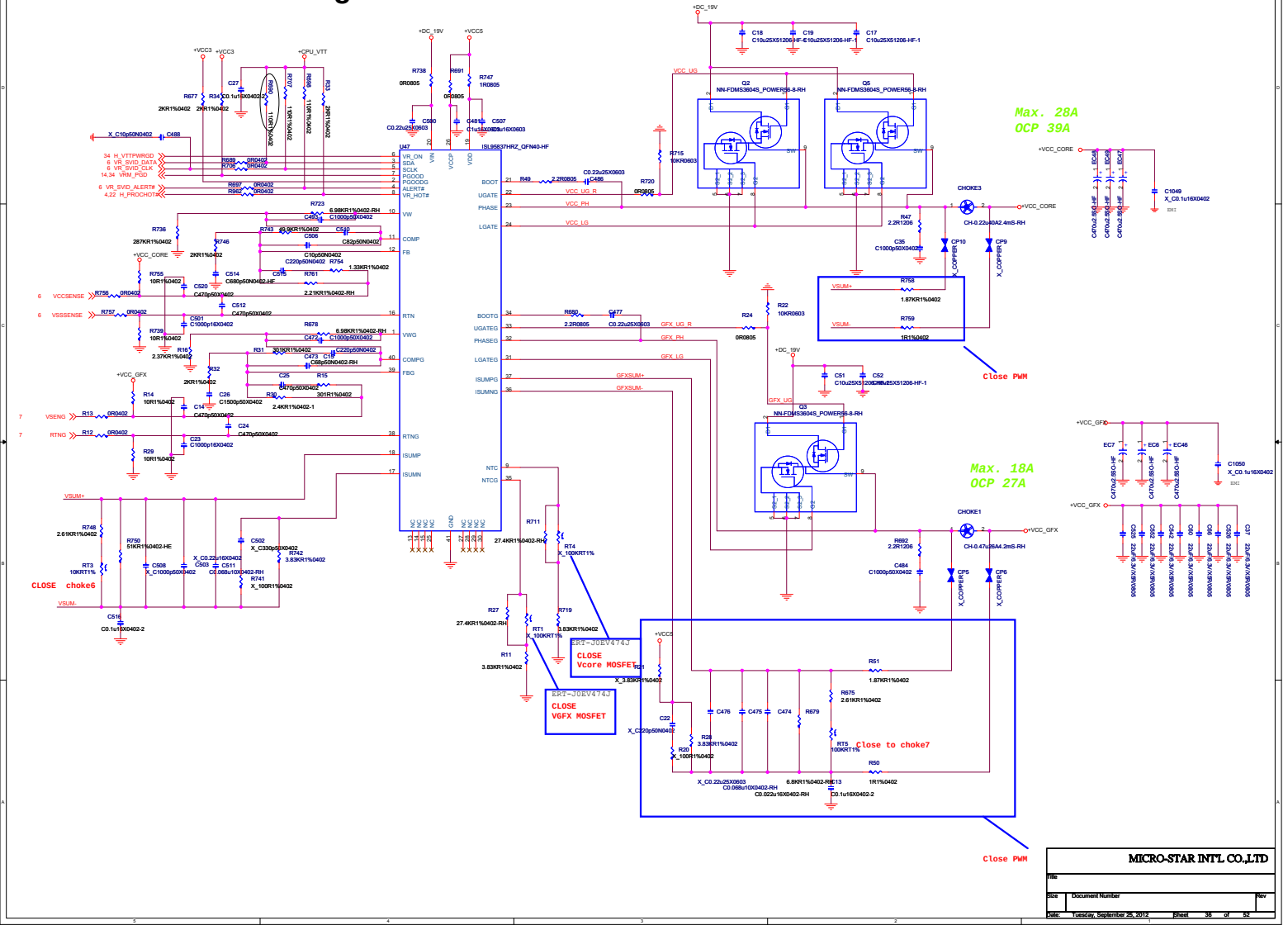
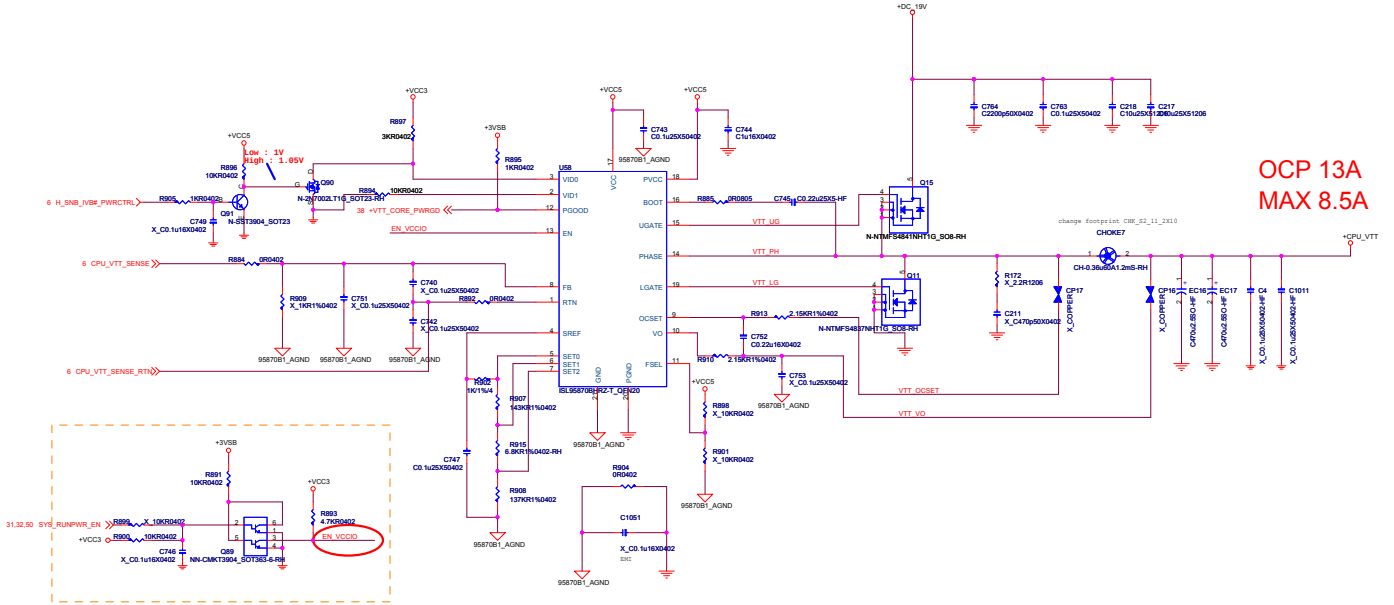
ISL95837 Single Phase For VR12 solution



CPU VTT Power



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Title		
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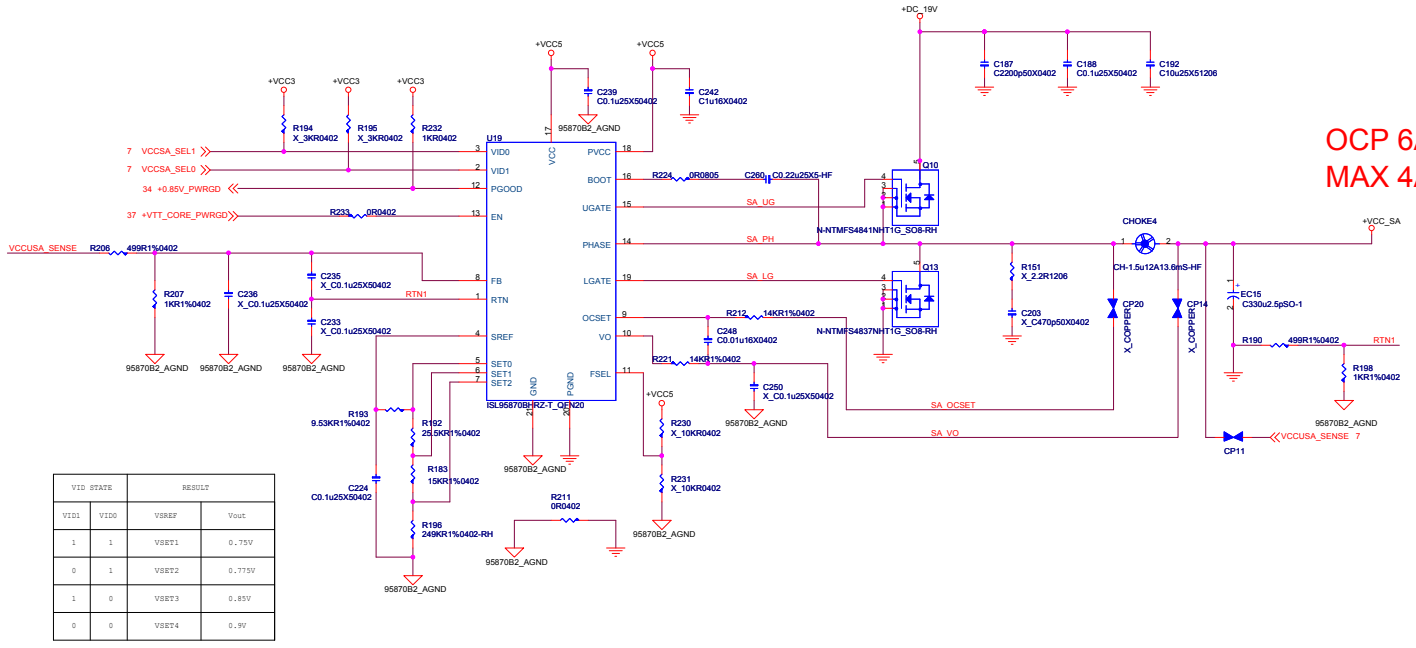

VID STATE		RESULT	
VID1	VID0	VSREF	Vout
1	1	VSET1	0.75V
0	1	VSET2	0.775V
1	0	VSET3	0.85V
0	0	VSET4	0.9V

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Title

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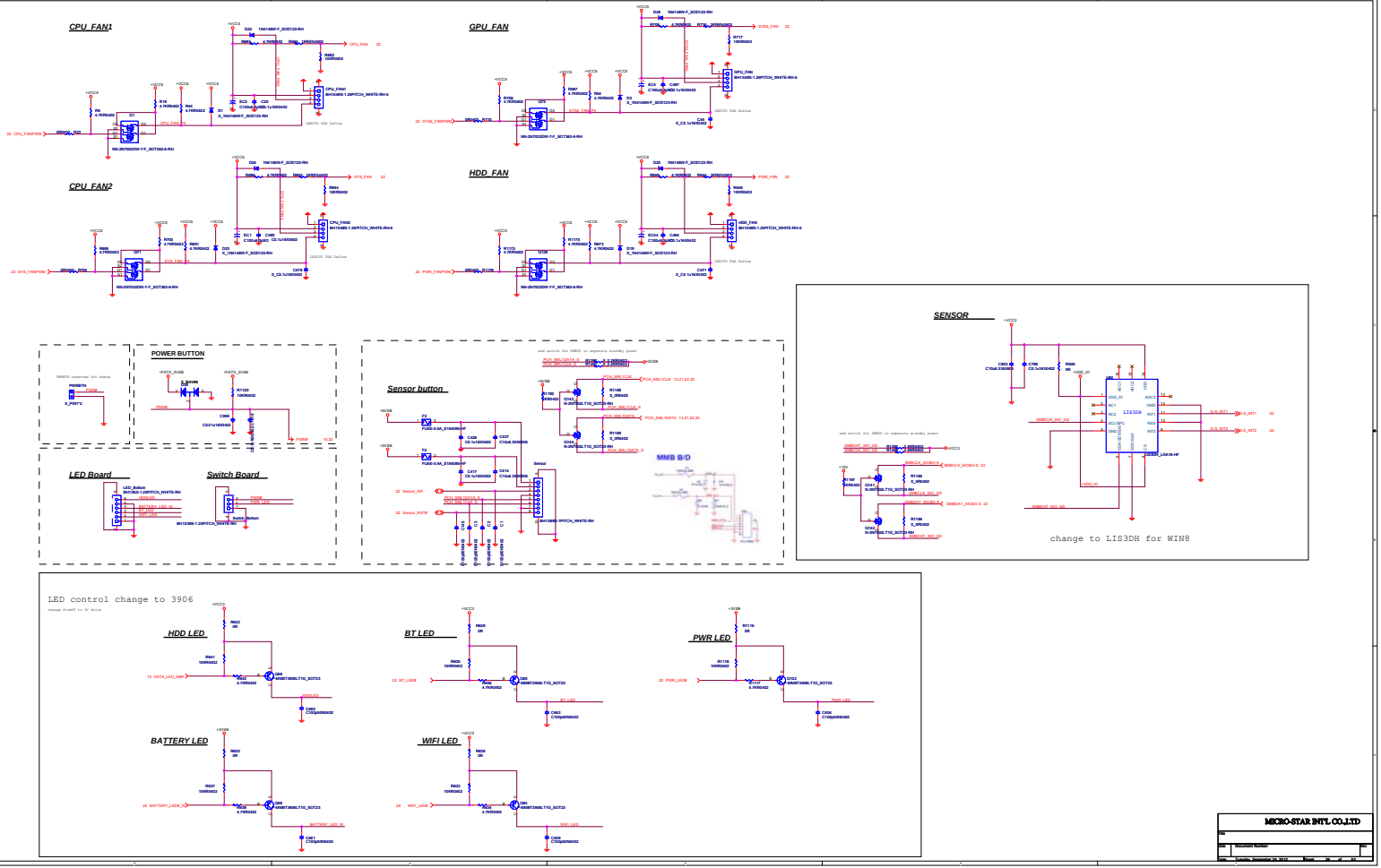
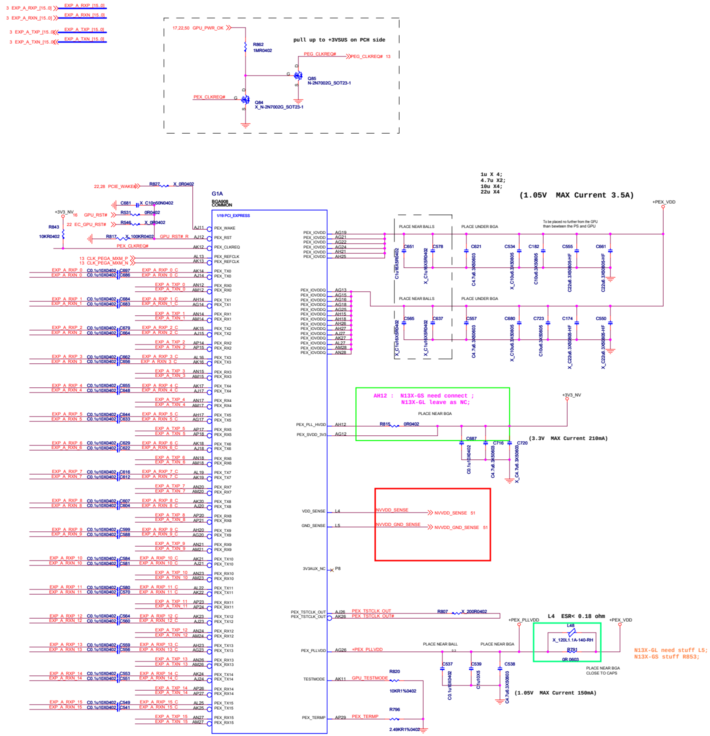

CPU_FAN1
GPU_FAN
CPU_FAN2
HDD_FAN
SENSOR
change to LIS3DH for WIN8
POWER BUTTON
Sensor button
LED Board
Switch Board
LED control change to 3906
HDD LED
BT LED
PWR LED
BATTERY LED
WIFI LED
MICRO-STAR INTL CO.,LTD



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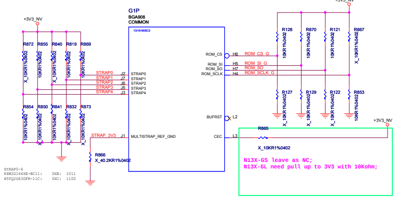
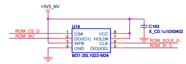
GPIOs, Thermal Sensor, I2C/GPIO Expanders



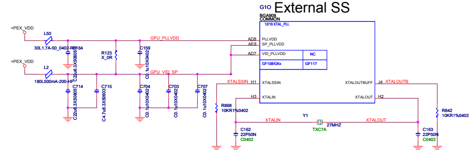
VBIOS ROM



A 256MB MEMORY APERTURE SIZE
CAN BE DEFINED USING A SEPARATE
ROM OR STRAPPING
A 256MB MEMORY APERTURE SIZE
CAN BE DEFINED USING A SEPARATE
ROM OR STRAPPING

SERIAL EEPROM 1M

External SS



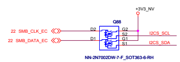


Table 5. N13M-GS/-NS DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Speed Bin (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646C-HC11	900	1152	Production candidate
		0xB		K4W2G1646E-BC11		1204	Post-production transition
	Hynix	0x6	1.5 V/ 1.5 V	H5TQ2G63BFR-11C	900	1008	Production candidate
		0xC		H5TQ2G63DFR-11C		N/A	Post-production transition

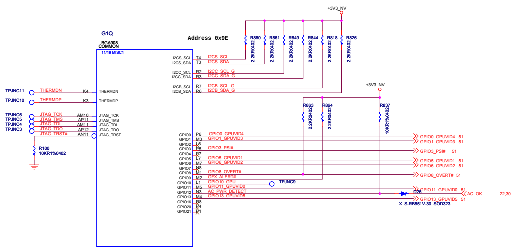
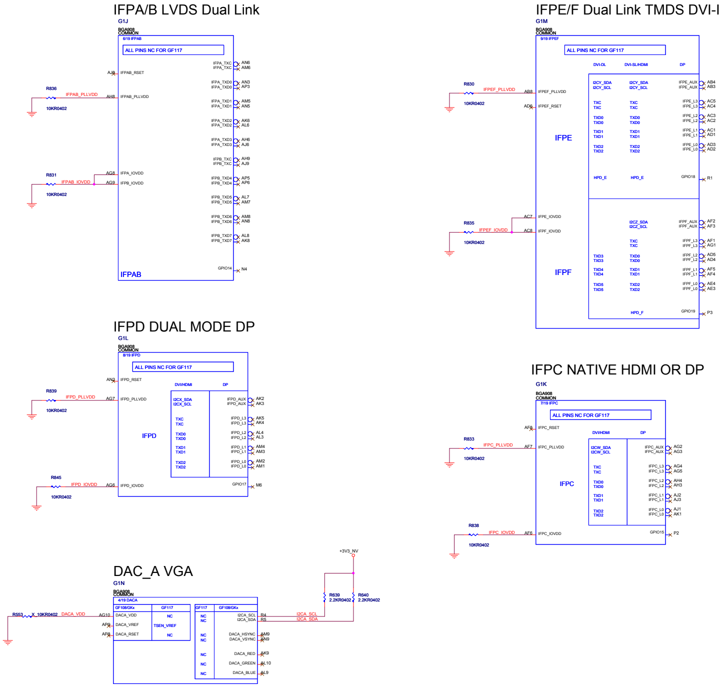
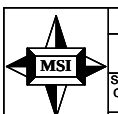


Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND


IFPA/B LVDS Dual Link
G1J
BGA908
COMMON
6/19 IFPAB
ALL PINS NC FOR GF117
IFPAB_RSET
IFPAB_PLLVDD
R836
10KR0402
IFPA_IOVDD
IFPB_IOVDD
IFPAB_IOVDD
R831
10KR0402
IFPA_TXC
IFPA_TXD0
IFPA_TXD1
IFPA_TXD2
IFPA_TXD3
IFPB_TXC
IFPB_TXD4
IFPB_TXD5
IFPB_TXD6
IFPB_TXD7
GPIO14
IFPAB
IFPE/F Dual Link TMDS DVI-I
G1M
BGA908
COMMON
9/19 IFPEF
ALL PINS NC FOR GF117
DVI-DL
DVI-SL/HDMI
DP
R830
IFPEF_PLLVDD
10KR0402
IFPEF_RSET
I2CY_SDA
I2CY_SCL
TXC
TXD0
TXD1
TXD2
IFPE_AUX
IFPE_L3
IFPE_L2
IFPE_L1
IFPE_L0
IFPE
HPD_E
GPIO18
R835
IFPEF_IOVDD
10KR0402
IFPE_IOVDD
IFPF_IOVDD
I2CZ_SDA
I2CZ_SCL
TXD3
TXD4
TXD5
IFPF_AUX
IFPF_L3
IFPF_L2
IFPF_L1
IFPF_L0
IFPF
HPD_F
GPIO19
IFPD DUAL MODE DP
G1L
BGA908
COMMON
8/19 IFPD
ALL PINS NC FOR GF117
IFPD_RSET
R839
IFPD_PLLVDD
10KR0402
DVI/HDMI
DP
I2CX_SDA
I2CX_SCL
IFPD_AUX
IFPD_L3
IFPD_L2
IFPD_L1
IFPD_L0
IFPD
R845
IFPD_IOVDD
10KR0402
GPIO17
IFPC NATIVE HDMI OR DP
G1K
BGA908
COMMON
7/19 IFPC
ALL PINS NC FOR GF117
IFPC_RSET
R833
IFPC_PLLVDD
10KR0402
I2CW_SDA
I2CW_SCL
IFPC_AUX
IFPC_L3
IFPC_L2
IFPC_L1
IFPC_L0
IFPC
R838
IFPC_IOVDD
10KR0402
GPIO15
DAC_A VGA
G1N
BGA908
COMMON
4/19 DACA
GF108/GKx
GF117
R553
10KR0402
DACA_VDD
DACA_VREF
DACA_RSET
NC
TSEN_VREF
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
+3V3_NV
R639
2.2KR0402
R640
2.2KR0402



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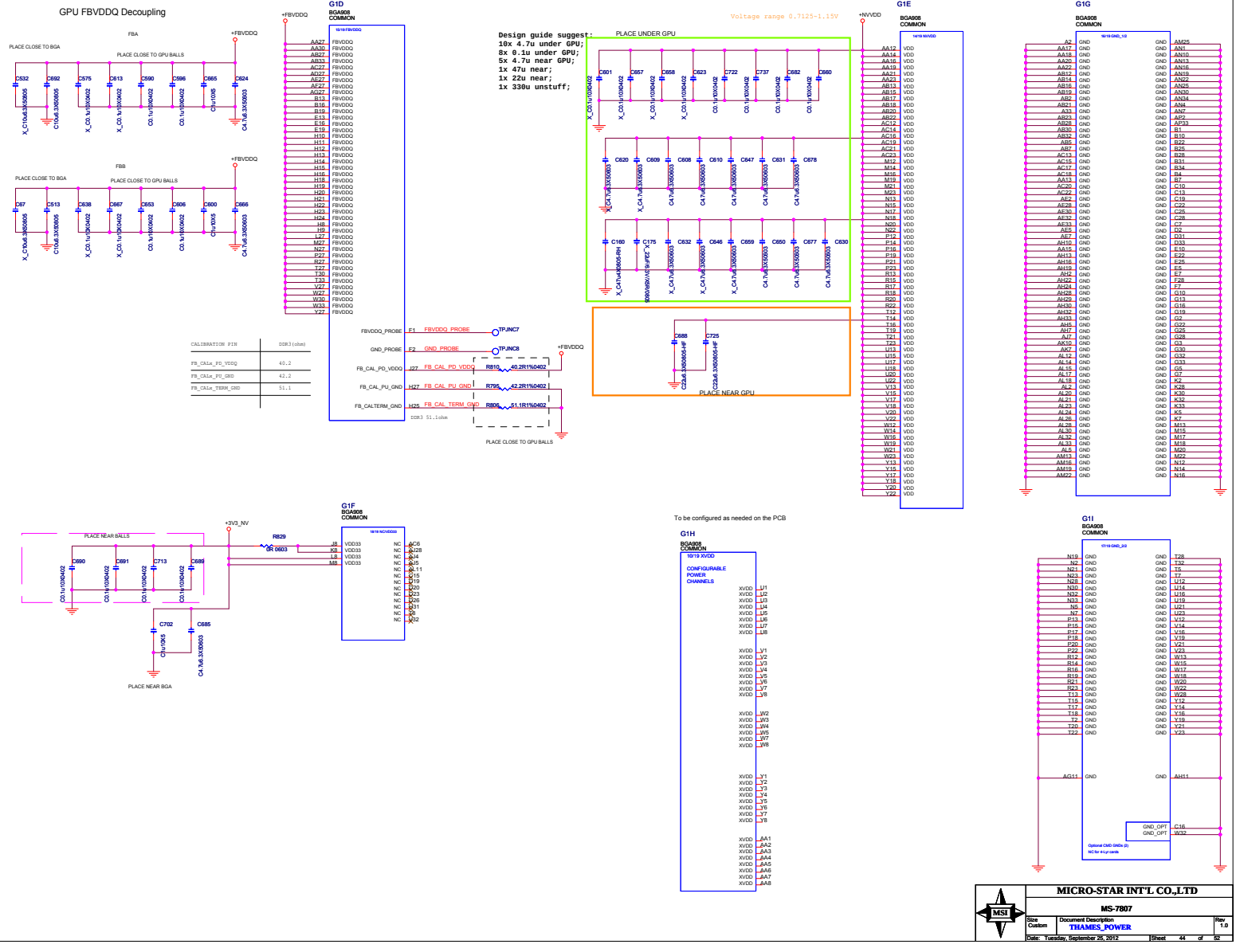
Power/Decoupling: NVVDD,3V3_NV,GRND,and Optional



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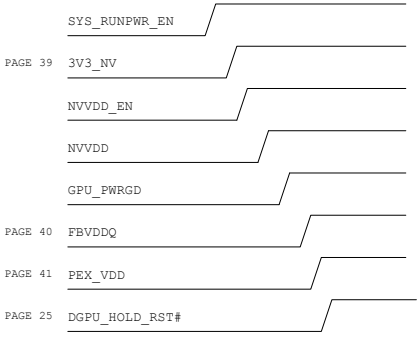
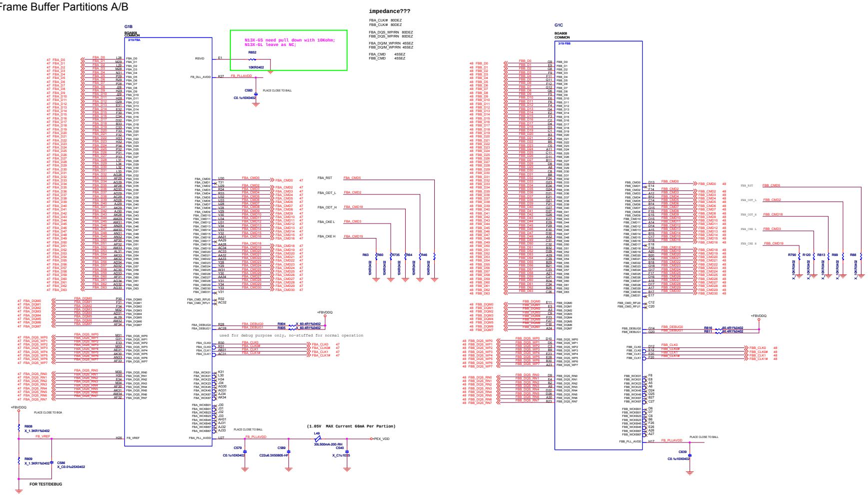


GPU Power Sequence

Frame Buffer Partitions A/B



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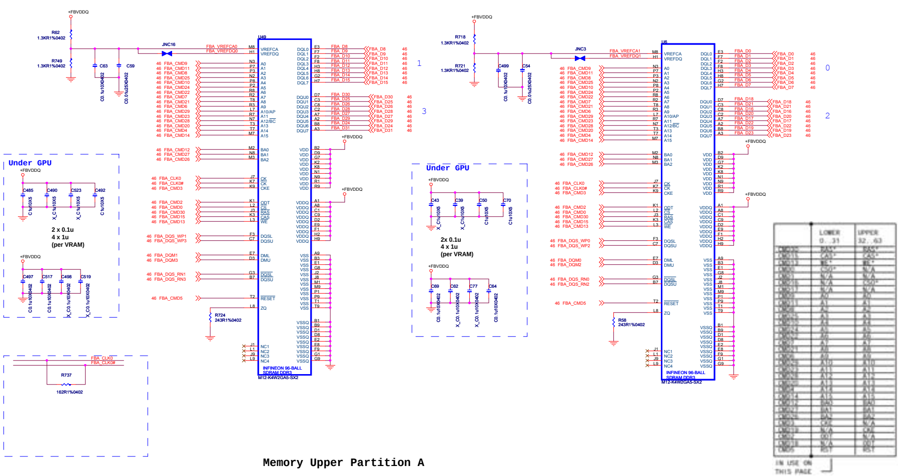
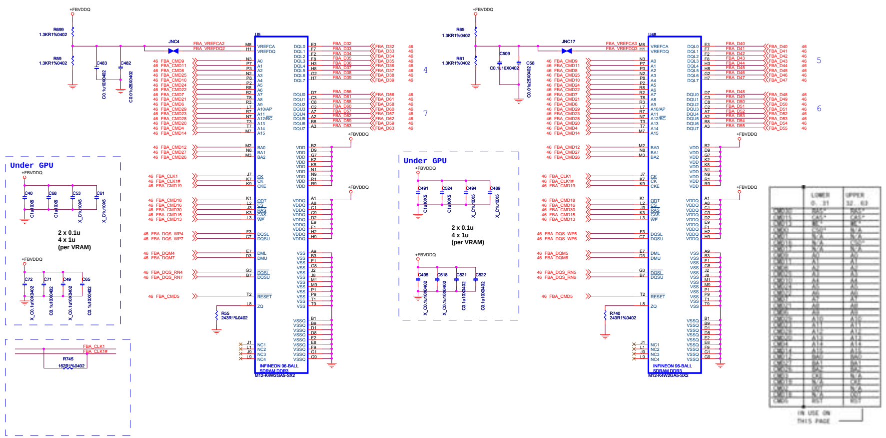
Memory Lower Partition A

M12-K4W2GA5-SX2 -- Samsung
M12-5TQ2GF5-HX3 -- Hynix



Memory Upper Partition A



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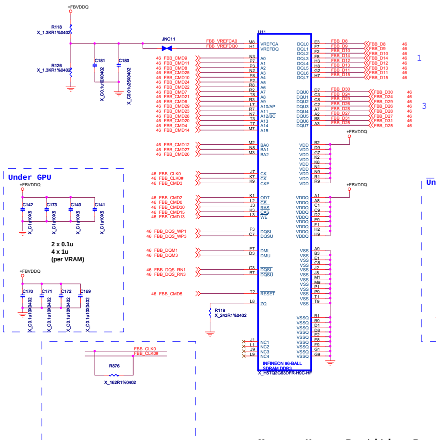
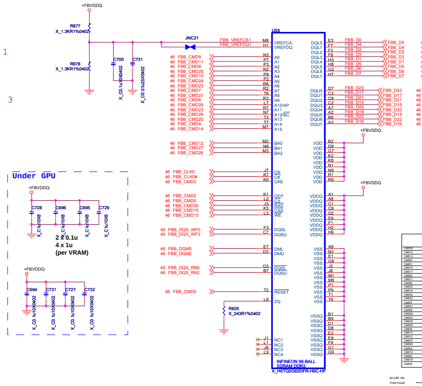
Memory Lower Partition B (Reserve)





	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

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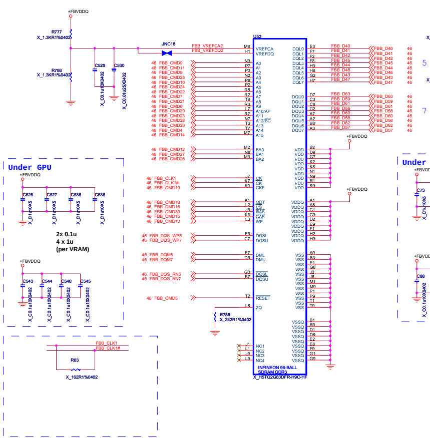
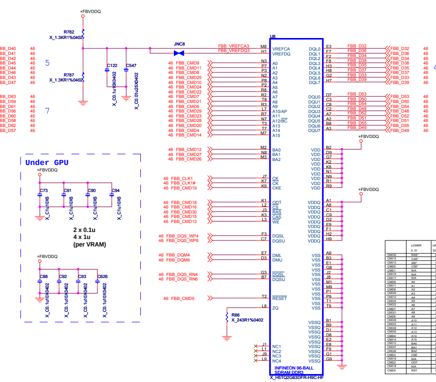
Memory Upper Partition B





	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

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Table 7. DDR3 EDP-Peak at T_J = 102 C*

Power Supply Rail	N13M-GS/-NS	N13P-GV2
	(A)	(A)
$NVVDD_{MP}$	32.10	50.46
$NVVDD_{TP}$	27.37	38.44
FBVDD+FBVDDQ	5.342	5.406
PEXVDD	1.232	1.348

Notes:

1. Memory configurations are as defined in Table 2.
2. Highest leakage GPU, power supply rails set to maximum voltage (NVVDD+2.5%, FBVDD/Q+3.0% for DDR3, PEXVDD rails + 30 mV)
3. The FBVDD and FBVDDQ data may vary with memory suppliers other than the ones specified in this document.

Table 6. DDR3 EDP-Continuous at T_J = 102 °C*

Power Supply Rail		N13M-GS/-NS	N13P-GV2
	(V)	(A)	
$NVVDD_{MP}$	–	**25.36**	**32.22**
$NVVDD_{TP}$	–	**21.78**	**26.66**
FB_DLLAVDD	1.05	0.015	0.015
FBA_PLLAVDD	1.05	0.055	0.055
PEX_IOVDD/Q	1.05	1.027	1.042
PEX_PLLVDD	1.05	0.130	0.130
PLLVDD	1.05	0.038	0.038
SP_PLLVDD	1.05	0.017	0.017
VID_PLLVDD	1.05	0.041	0.041
TOTAL	**1.05**	**1.323**	**1.338**
FBVDD+FBVDDQ	1.5	3.246	3.116
TOTAL	**1.5**	**3.246**	**3.116**
PEX_SVDD_3v3/ PEX_PLL_HVDD	3.3	0.143	0.143
VDD33	3.3	0.056	0.056
TOTAL	**3.3**	**0.199**	**0.199**

Notes:

1. Memory configurations are as defined in Table 2.
2. Highest leakage GPU, power supply rails set to maximum voltage (NVVDD+2.5%, FBVDD/Q+3.0% for DDR3, PEXVDD rails + 30 mV)
3. The FBVDD and FBVDDQ data may vary with different memory suppliers other than the ones specified in this document.

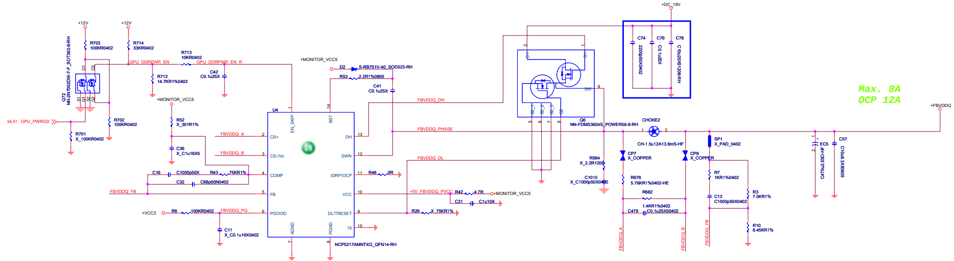
Table 5. TDP at TDP Point T_J = 102 °C * (DDR3)

	GPU	Mem	NVVDD		FBVDD		FBVDDQ		PCI Express		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3 V)	
Products	(W)	(W)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13M-GS/-NS	16.60	2.88	15.13	13.99	0.64	0.95	2.14	3.21	921.63	1.03	0	0	62.70	0.07	69.60	0.23
N13P-GV2	21.90	2.99	18.78	19.25	0.67	1.01	2.20	3.30	921.60	1.03	0	0	62.70	0.07	69.60	0.23

Notes:

1. Memory configurations are as defined in Table 2.
2. Highest leakage GPU, power supply rails set to nominal voltage
3. Display configuration: LVDS dual-link panel in 1920 x 1200
4. FBVDDQ = FBVDDQ (GPU) + FBVDDQ (Mem)
5. GPU Power = NVVDD + 40% × FBVDDQ + PCI Express + I/O + PLLVDD + Other
6. Memory Power = FBVDD + 60% × FBVDDQ
7. Power is based on the highest generation of PCI Express available for this GPU.

* Worst case TDP is at 102 °C T_J with a high leakage GPU. Clock throttling occurs at 102°C T_J.

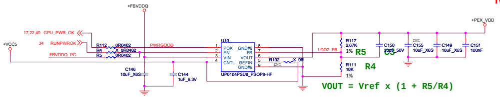


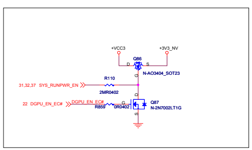
LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.05V +/- 2% Iout = 1.7A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

OCP 7A

MAX 1.3A





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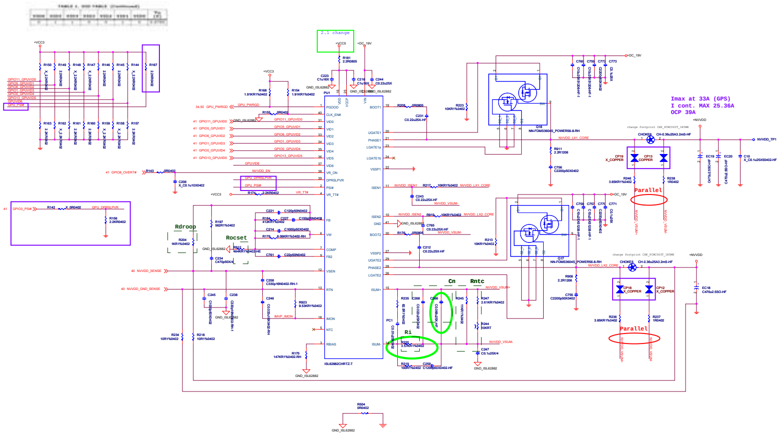

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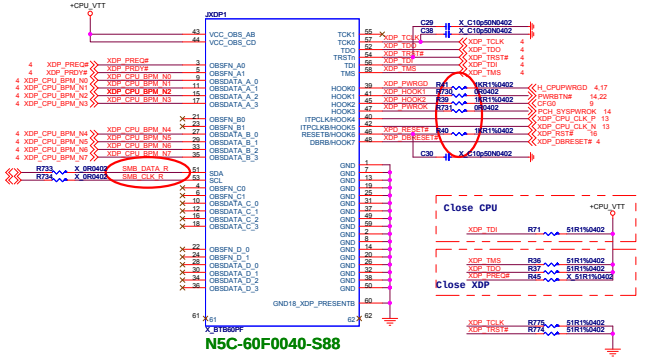
XDP(PROCESSOR)



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