# FUSION

**(MS-7800M1 Ver:10)**

mATX: 9.6 inch * 8.86 inch

## CPU:

**AMD FM2(Llano uPGA FAMILIES)**

## System Chipset:

**AMD - Hudson D3**

## On Board Chipset:

**CLOCK GEN --FCH internal clock gen**
**LPC Super I/O --F71808A**
**LAN-Realtek 8111E**

**Azalia CODEC - Realtek ALC887/662**

## Main Memory:

**DDR III * 2 (16 GB)**

## Expansion Slots:

**PCI Express X16 Slot * 1**
**PCI Express X1 Slot * 2**

## VRM

**Controller - Intersil 6277 3+2 Phase**

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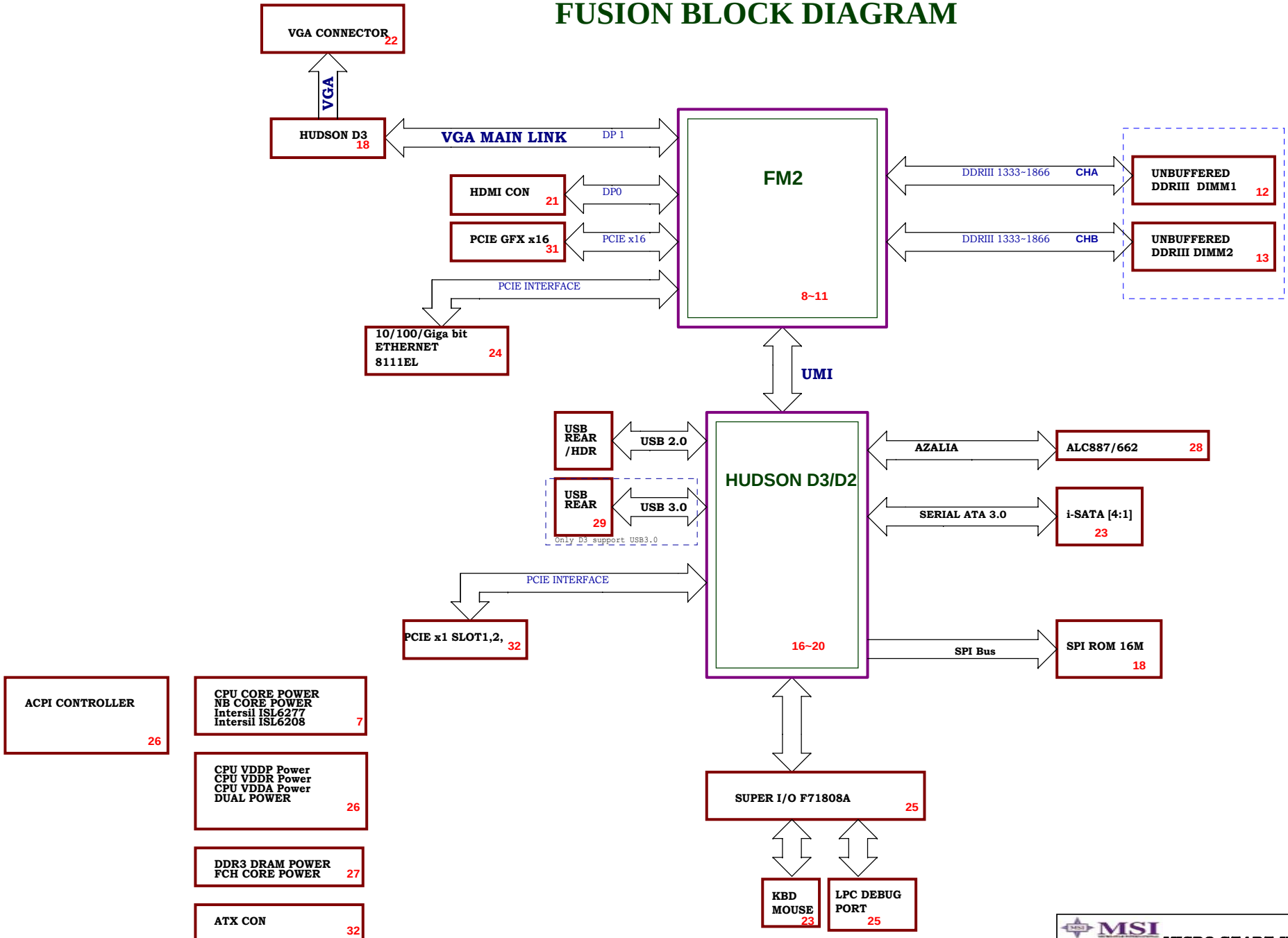
|---|---|---|
| Title: MS-7800 | | |
| Size: Custom | Document Number: Cover Sheet | Rev: 10 |
| Date: Friday, April 06, 2012 | Sheet 1 of 36 | |

# FUSION BLOCK DIAGRAM

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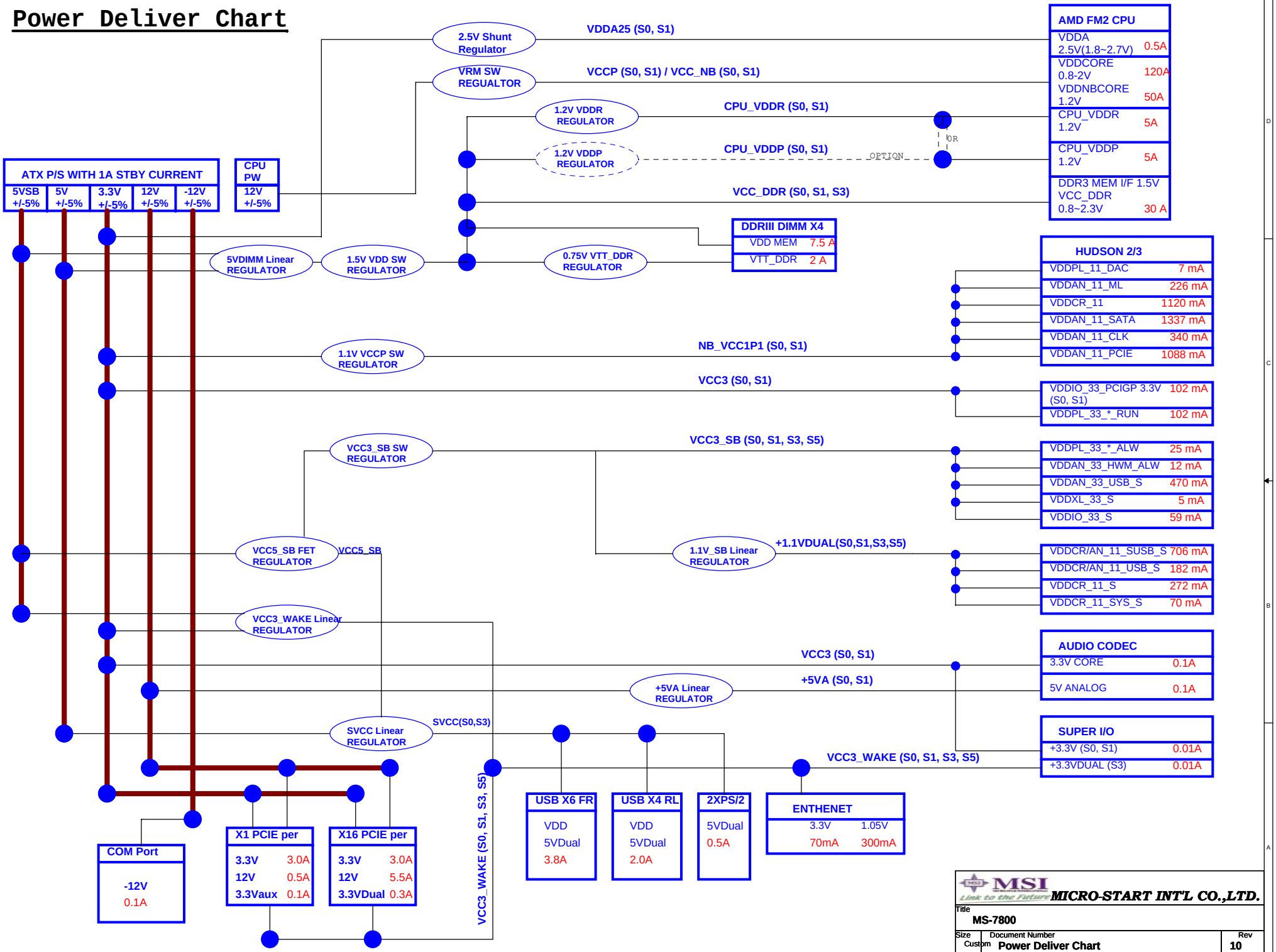
| Title | MS-7800 | |
| Size: Custom | Document Number: Block Diagram | Rev: 10 |
| Date: Friday, April 06, 2012 | Sheet 2 of 36 | |

# Power Deliver Chart

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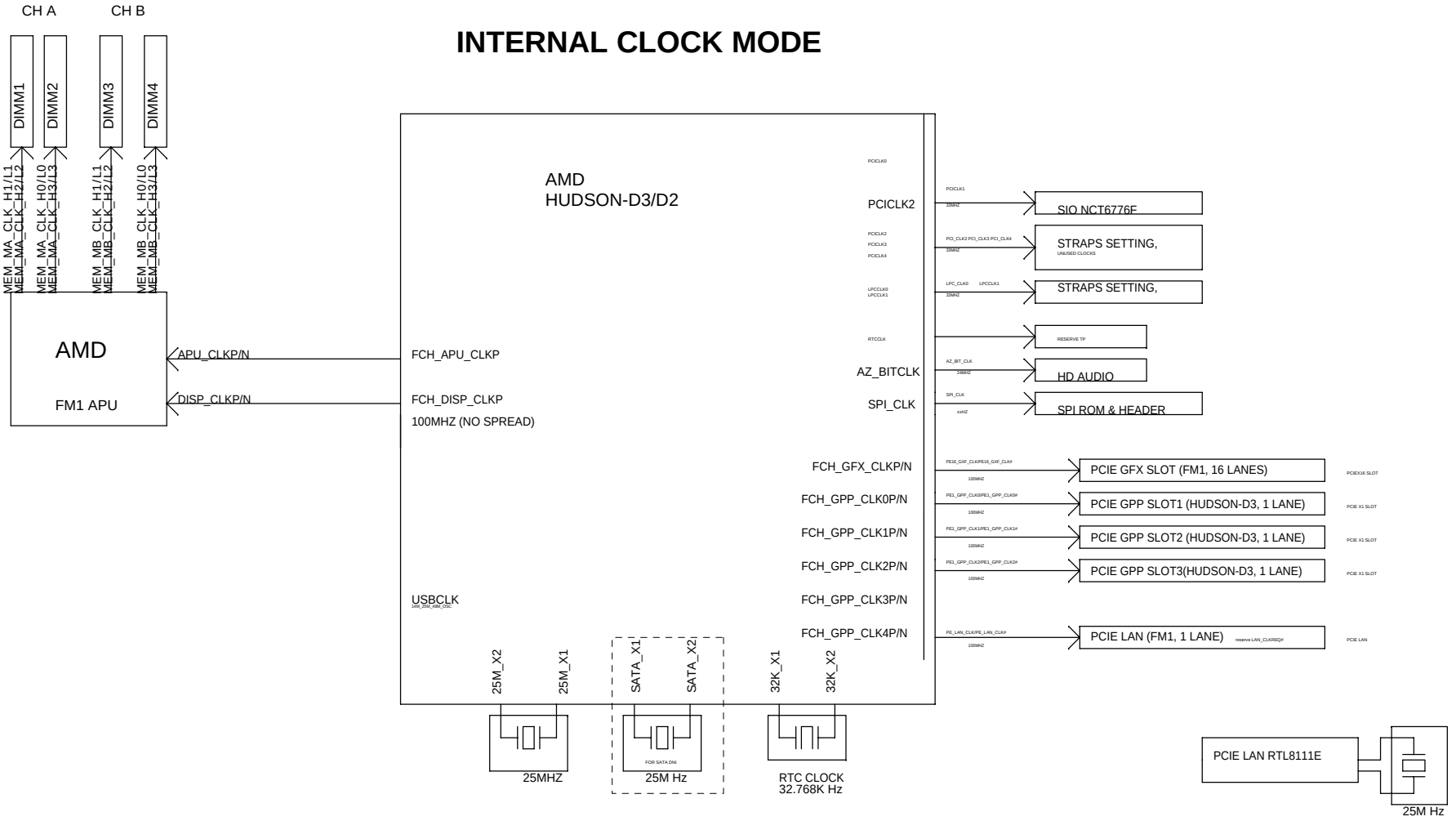
# INTERNAL CLOCK MODE

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| Title: MS-7800 | | |
| Size: Custom | Document Number: Clock Distribution | Rev: 10 |
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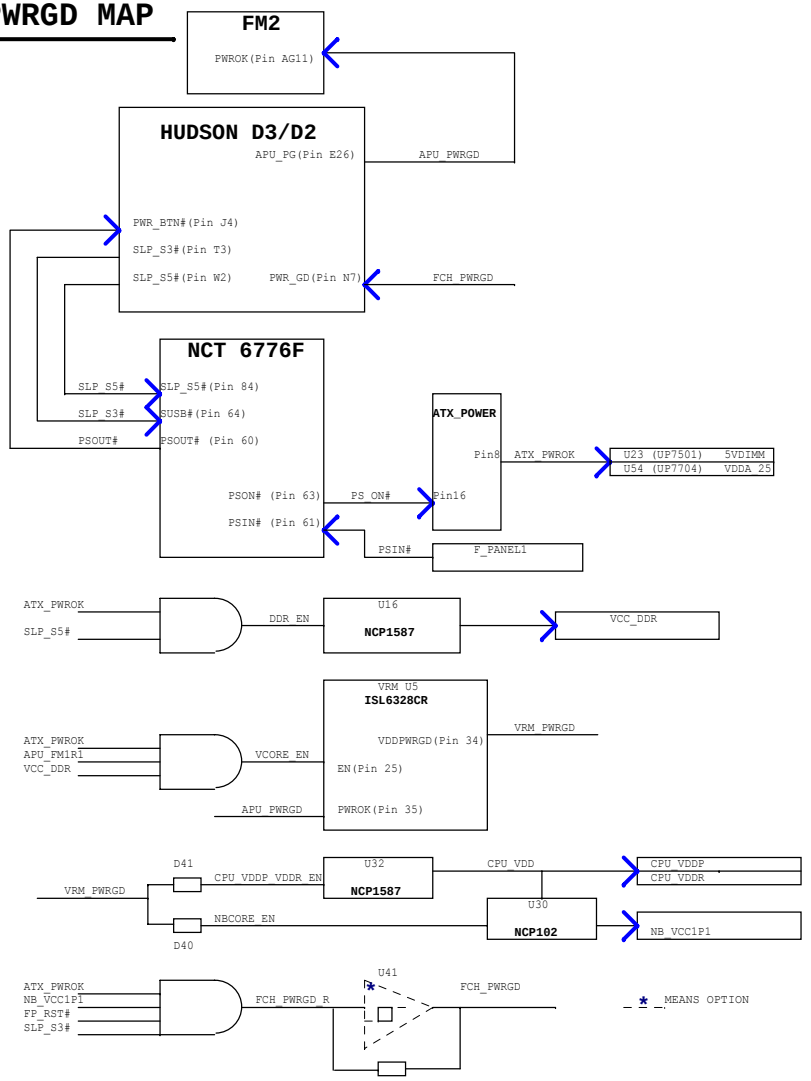
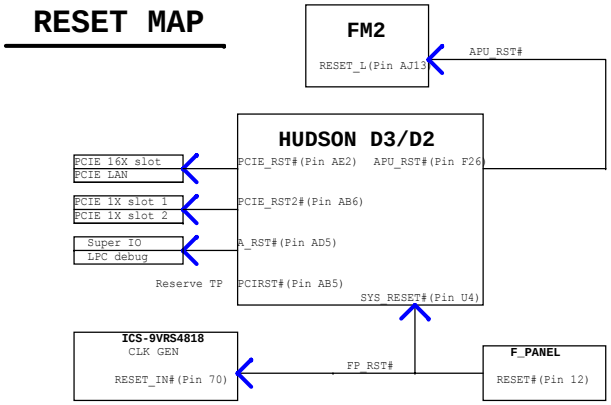
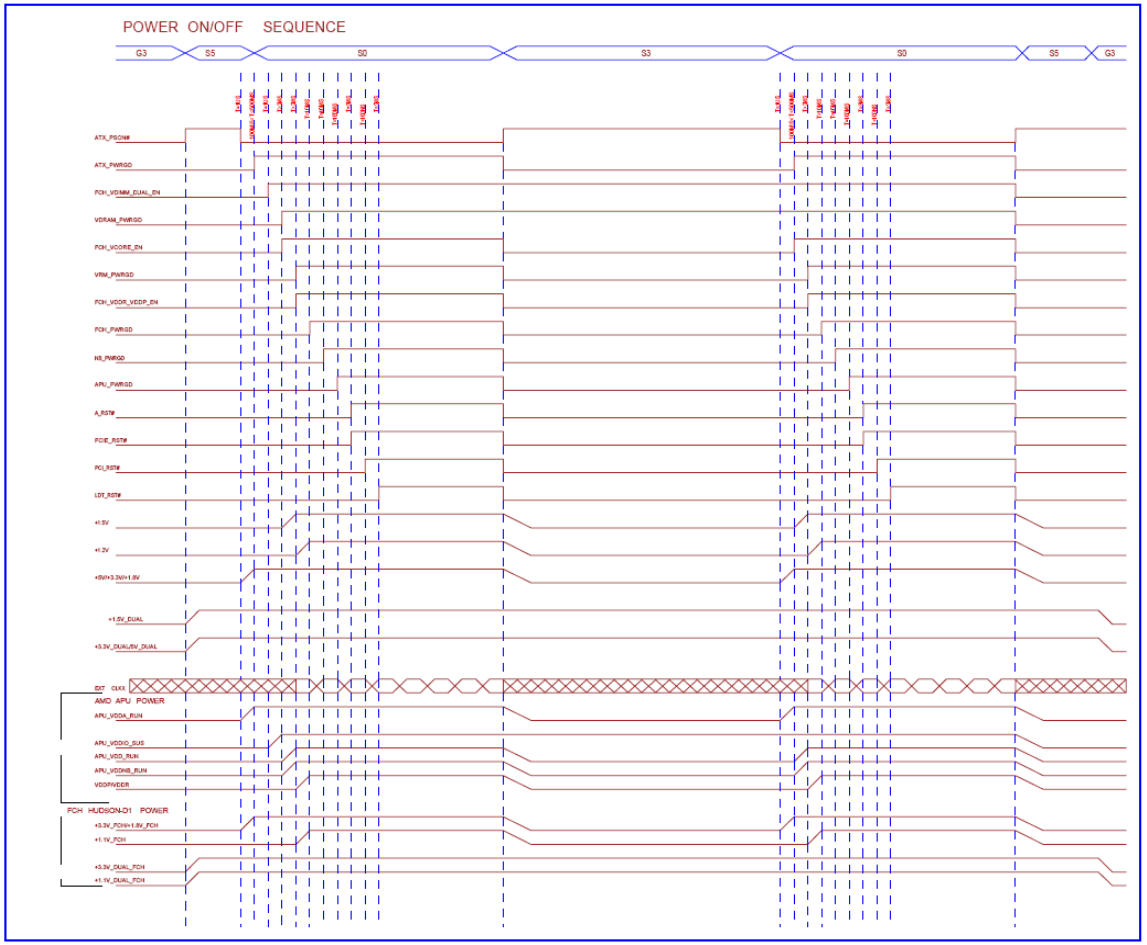
# PWRGD MAP




# RESET MAP




# POWER ON SEQUENCE




| | | |
|---|---|---|
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| Title: MS-7800 | | |
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SIO Fintek 71808A GPIO Config

| Pin | GPIO | Power Rail | Function description | Comment |
|---|---|---|---|---|
| 18 | GP20 | VSB | IO_PME# | |
| 22 | LED_VSB/GP24 | VSB | SUS_LED | reserved |
| 23 | LED_VCC/GP25 | VSB | PWR_LED | |
| 42 | GP67 | VSB | USB_EN | OD |
| 53 | GP00 | VSB | MB_ID0 | GPI reserved |
| 54 | GP01 | VSB | MB_ID1 | GPI reserved |
| 55 | GP02 | VSB | MB_ID2 | GPI reserved |
| 56 | GP03 | VCC | USB_MODE1 | IO/OD |
| 19 | GP21 | VSB | USB_MODE2 | IO/OD |
| 49 | GP30 | VSB | SIO_VCORE_EN | GPI reserved |
| 50 | GP31 | VSB | SIO_VLDT_EN | GPI reserved |

FCH HUDSON D3/D2GPIO Config

| Pin | pin Name | Function description |
|---|---|---|
| AJ3 | AD0/GPIO0 | |
| J2 | IR_LED#/LLB#/GPIO184 | |
| AD22 | SATA_ACT#/GPIO67 | |
| M6 | TEMPIN3/TALERT#/ GPIO174 | FCH_TALERT#:Thermal Alert. The FCH can be programmed to generate an SMI, SCI, or IRQ13 through GPE, or generate an SMI without GPE in response to the signal*s assertion. |
| | | |
| V3 | SPI_CLK/GPIO162 | SPI Clock |
| V6 | SPI_DI/GPIO164 | SPI Data In |
| V5 | SPI_DO/GPIO163 | SPI Data Output |
| T6 | SPI_CS1#/GPIO165 | SPI Chip Select1# |
| V1 | ROM_RST#/SPI_WP#/GPIO161 | SPI write protect (active low) |
| Y6 | SPI_HOLD#/GEVENT9# | SPI HOLD#. Assert low to hold the SPI transaction. |
| | | |
| T8 | USB_OC0#/SPI_TPM_CS#/ TRST#/GEVENT12# | OC#0:USB 3.0 port 3,USB 2.0 port 13 |
| J7 | USB_OC1#/TDI/GEVENT13# | OC#1:USB2.0 port 4,5 |
| P5 | USB_OC2#/TCK/GEVENT14# | OC#2:USB2.0 port 8,9 |
| P5 | USB_OC3#/ AC_PRES/TDO/GEVENT15# | OC#3:USB 3.0 port 0,USB 2.0 port 10 |
| P6 | USB_OC4#/IR_RX0/ GEVENT16# | OC#4:USB 3.0 port 1,USB 2.0 port 11 |
| T1 | USB_OC5#/IR_TX0/ GEVENT17# | OC#5:USB2.0 port 2,3 |
| R8 | USB_OC6#/IR_TX1/ GEVENT6# | OC#6:USB2.0 port 0,1 |
| M7 | BLINK/USB_OC7#/ GEVENT18# | OC#7:USB 3.0 port 2,USB 2.0 port12 |
| | | |
| | GPIO[171::173];GPIO[175::182]; GPIO[193::194] | Configure as one of the following: 10-k次 5% pull-up resistor to +3.3V_S5. 10-k次 5% pull-down resistor. |

## DDR DIMM Config.

| DEVICE | ADDRESS | CLOCK |
|---|---|---|
| DIMM 1 CH-A | 10100000B A0H | MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2 |
| DIMM 2 CH-B | 10100001B A2H | MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2 |

## SMBus TABLE

| SOURCE | SINGLE NAME | LINKED DEVICE |
|---|---|---|
| APU | DP0_AUXP_C /DP0_AUXN_C | HDMI |
| | DP1_AUXP_C /DP1_AUXN_C | Hudson D2/3 DP to VGA translator |
| FCH | SCLK0/SDATA0 | DIMMs, |
| | SCLK1/SDATA1 | PCIE SLOTs, |
| | SCLK3/SDATA3 | TP |

## RESET TABLE

| SOURCE | SINGLE NAME | LINKED DEVICE |
|---|---|---|
| FCH | PCIE_RST# | PCIe 16X,LAN |
| | A_RST# | SIO,LPC debug |
| | PCIE_RST2# | PCIE_1X |
| | LDT_RST# | APU |
| | AZ_RST# | AZALIA CODEC |
| | DDR3_RST# | NC |
| | FC_RST# | DEBUG BUS |
| | ROM_RST# | NC |
| FRONT PANEL | FP_RST# | FCH |

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Title: MS-7800

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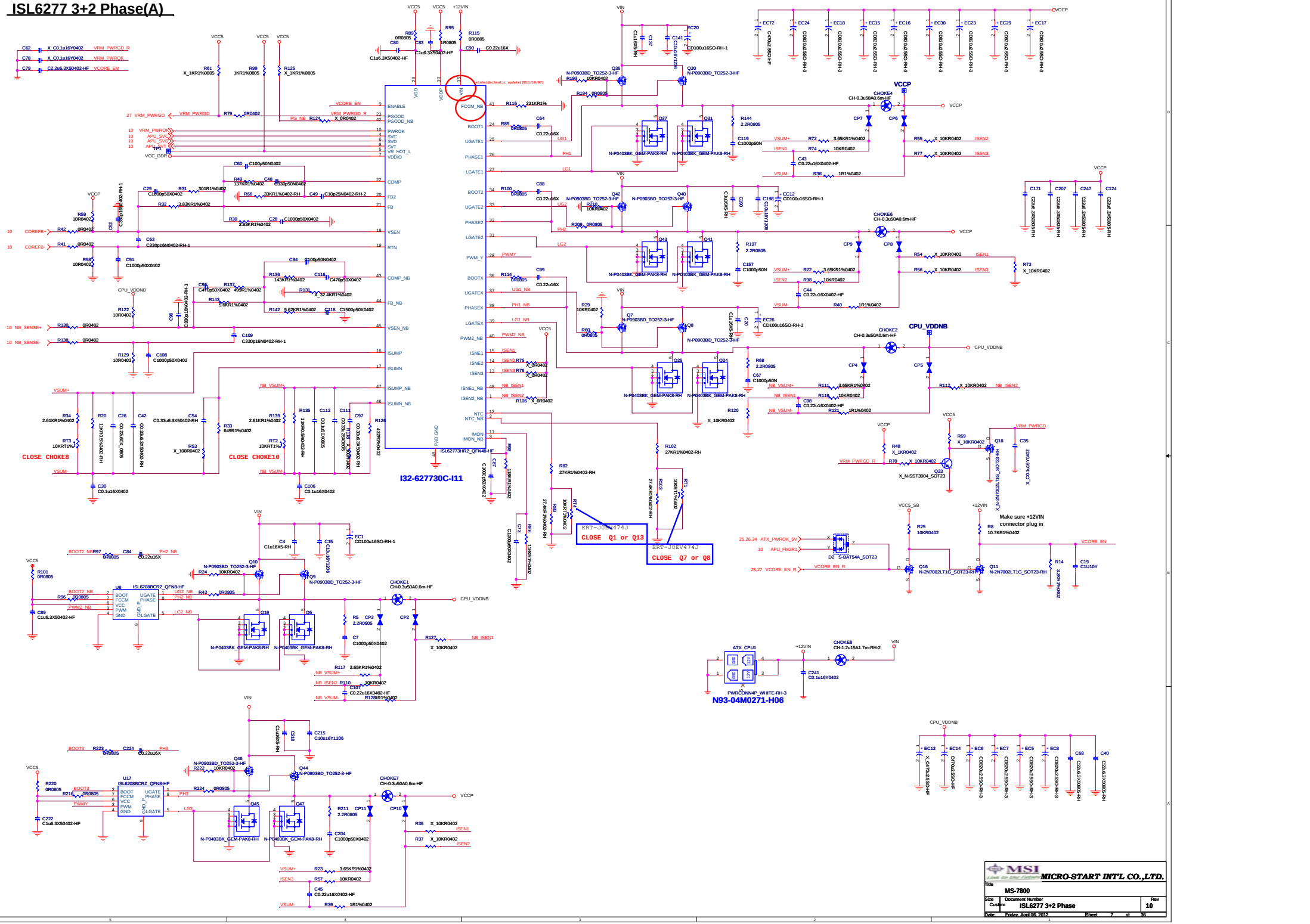
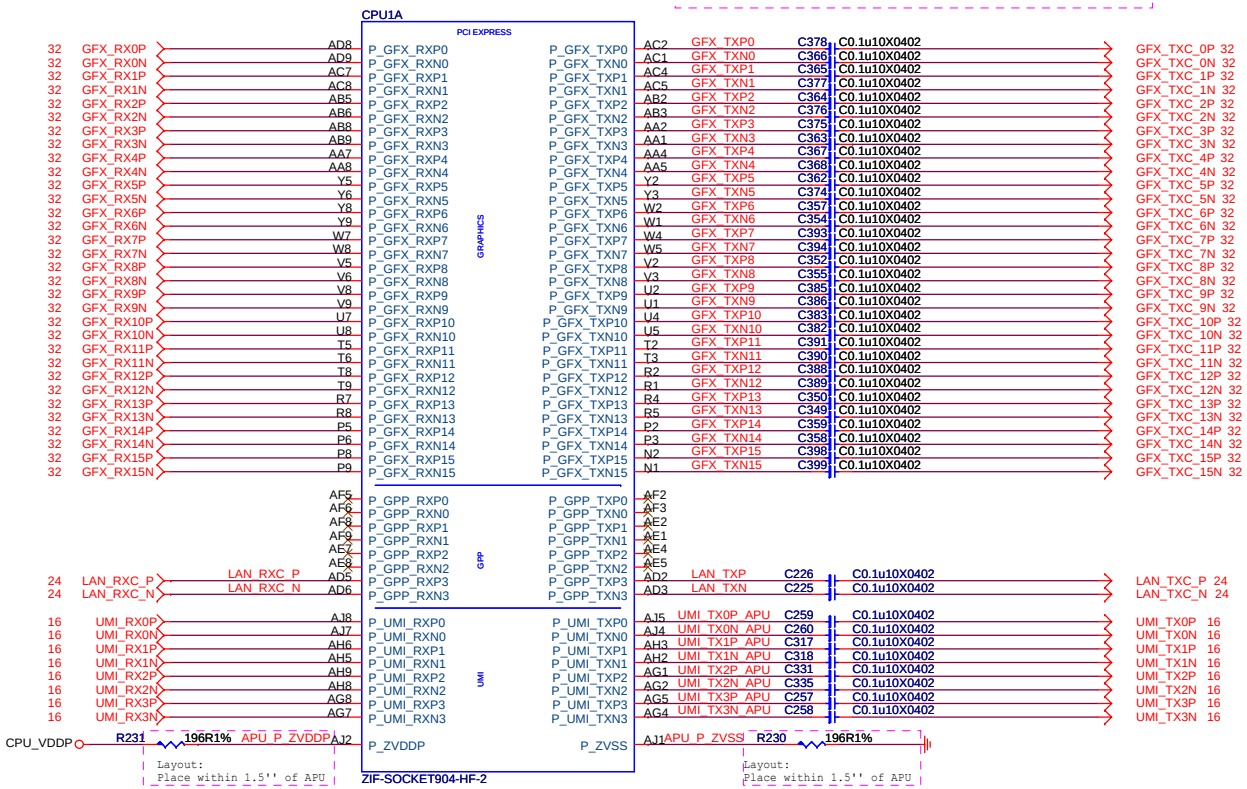
# ISL6277 3+2 Phase(A)



# FM2 PCIE I/F

mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%




| Title | | | |
|---|---|---|---|
| MICRO-START INT'L CO.,LTD. | | | |
| MS-7800 | | | |
| Size: Custom | Document Number: FM2 PCIE I/F | | Rev: 10 |
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# FM2 DDR3 I/F

12 MEM_MA_DQS_L[7..0]
12 MEM_MA_DQS_H[7..0]
12 MEM_MA_DM[7..0]
13 MEM_MB_DQS_L[7..0]
13 MEM_MB_DQS_H[7..0]
13 MEM_MB_DM[7..0]

CPU1B

MEM_MA_DATA[63..0] 12

12 MEM_MA_ADD[15..0]
MEM_MA_ADD0 V27 MA_ADD0
MEM_MA_ADD1 P27 MA_ADD1
MEM_MA_ADD2 R25 MA_ADD2
MEM_MA_ADD3 P26 MA_ADD3
MEM_MA_ADD4 R24 MA_ADD4
MEM_MA_ADD5 P24 MA_ADD5
MEM_MA_ADD6 P23 MA_ADD6
MEM_MA_ADD7 N26 MA_ADD7
MEM_MA_ADD8 N23 MA_ADD8
MEM_MA_ADD9 M25 MA_ADD9
MEM_MA_ADD10 V24 MA_ADD10
MEM_MA_ADD11 N25 MA_ADD11
MEM_MA_ADD12 M24 MA_ADD12
MEM_MA_ADD13 Y23 MA_ADD13
MEM_MA_ADD14 L27 MA_ADD14
MEM_MA_ADD15 L24 MA_ADD15

12 MEM_MA_BANK0
12 MEM_MA_BANK1
12 MEM_MA_BANK2
MEM_MA_BANK0 W26 MA_BANK0
MEM_MA_BANK1 V25 MA_BANK1
MEM_MA_BANK2 L26 MA_BANK2

MEM_MA_DM0 E17 MA_DM0
MEM_MA_DM1 H21 MA_DM1
MEM_MA_DM2 F25 MA_DM2
MEM_MA_DM3 G29 MA_DM3
MEM_MA_DM4 AF29 MA_DM4
MEM_MA_DM5 AE25 MA_DM5
MEM_MA_DM6 AG21 MA_DM6
MEM_MA_DM7 AF17 MA_DM7

MEM_MA_DQS_H0 H17 MA_DQS_H0
MEM_MA_DQS_L0 G17 MA_DQS_L0
MEM_MA_DQS_H1 F21 MA_DQS_H1
MEM_MA_DQS_L1 F21 MA_DQS_L1
MEM_MA_DQS_H2 G26 MA_DQS_H2
MEM_MA_DQS_L2 G25 MA_DQS_L2
MEM_MA_DQS_H3 F30 MA_DQS_H3
MEM_MA_DQS_L3 E30 MA_DQS_L3
MEM_MA_DQS_H4 AE28 MA_DQS_H4
MEM_MA_DQS_L4 AE29 MA_DQS_L4
MEM_MA_DQS_H5 AG24 MA_DQS_H5
MEM_MA_DQS_L5 AG25 MA_DQS_L5
MEM_MA_DQS_H6 AF20 MA_DQS_H6
MEM_MA_DQS_L6 AF21 MA_DQS_L6
MEM_MA_DQS_H7 AE16 MA_DQS_H7
MEM_MA_DQS_L7 AD16 MA_DQS_L7

mach@CLOCK assignment can be changed

12 MEM_MA_CLK_H0
12 MEM_MA_CLK_L0
MEM_MA_CLK_H0 U27 MA_CLK_H0
MEM_MA_CLK_L0 U26 MA_CLK_L0
T23 MA_CLK_H1
U23 MA_CLK_L1
T25 MA_CLK_H2
T26 MA_CLK_L2
12 MEM_MA_CLK_H3
12 MEM_MA_CLK_L3
MEM_MA_CLK_H3 R27 MA_CLK_H3
MEM_MA_CLK_L3 R28 MA_CLK_L3

12 MEM_MA_CKE0
12 MEM_MA_CKE1
MEM_MA_CKE0 L23 MA_CKE0
MEM_MA_CKE1 K26 MA_CKE1

AA24 MA0_ODT0
AC27 MA0_ODT1
12 MEM_MA1_ODT0
12 MEM_MA1_ODT1
MEM_MA1_ODT0 AA25 MA1_ODT0
MEM_MA1_ODT1 AC26 MA1_ODT1

Y27 MA0_CS_L0
AB26 MA0_CS_L1
12 MEM_MA1_CS_L0
12 MEM_MA1_CS_L1
MEM_MA1_CS_L0 W23 MA1_CS_L0
MEM_MA1_CS_L1 AB25 MA1_CS_L1

12 MEM_MA_RAS_L
12 MEM_MA_CAS_L
12 MEM_MA_WE_L
MEM_MA_RAS_L W25 MA_RAS_L
MEM_MA_CAS_L Y24 MA_CAS_L
MEM_MA_WE_L Y26 MA_WE_L

12 MEM_MA_RESET#
12 MEM_MA_HOT#
MEM_MA_RESET# J25 MA_RESET_L
MEM_MA_HOT# U24 MA_EVENT_L

APU_M_VREF K22 M_VREF
VCC_DDR R556 39.2R1%0402 APU_M_ZVDDIO J24 M_ZVDDIO
Layout: Place within 1.5'' of APU

MA_DATA0 F16 MEM_MA_DATA0
MA_DATA1 G16 MEM_MA_DATA1
MA_DATA2 H18 MEM_MA_DATA2
MA_DATA3 F19 MEM_MA_DATA3
MA_DATA4 F15 MEM_MA_DATA4
MA_DATA5 H15 MEM_MA_DATA5
MA_DATA6 E18 MEM_MA_DATA6
MA_DATA7 F18 MEM_MA_DATA7
MA_DATA8 G20 MEM_MA_DATA8
MA_DATA9 H20 MEM_MA_DATA9
MA_DATA10 E23 MEM_MA_DATA10
MA_DATA11 G23 MEM_MA_DATA11
MA_DATA12 G19 MEM_MA_DATA12
MA_DATA13 E20 MEM_MA_DATA13
MA_DATA14 E22 MEM_MA_DATA14
MA_DATA15 G22 MEM_MA_DATA15
MA_DATA16 F24 MEM_MA_DATA16
MA_DATA17 H24 MEM_MA_DATA17
MA_DATA18 E27 MEM_MA_DATA18
MA_DATA19 F27 MEM_MA_DATA19
MA_DATA20 H23 MEM_MA_DATA20
MA_DATA21 E24 MEM_MA_DATA21
MA_DATA22 E26 MEM_MA_DATA22
MA_DATA23 H26 MEM_MA_DATA23
MA_DATA24 G28 MEM_MA_DATA24
MA_DATA25 E29 MEM_MA_DATA25
MA_DATA26 H29 MEM_MA_DATA26
MA_DATA27 H30 MEM_MA_DATA27
MA_DATA28 H27 MEM_MA_DATA28
MA_DATA29 F28 MEM_MA_DATA29
MA_DATA30 F31 MEM_MA_DATA30
MA_DATA31 G31 MEM_MA_DATA31
MA_DATA32 AD30 MEM_MA_DATA32
MA_DATA33 AE30 MEM_MA_DATA33
MA_DATA34 AG27 MEM_MA_DATA34
MA_DATA35 AF27 MEM_MA_DATA35
MA_DATA36 AD31 MEM_MA_DATA36
MA_DATA37 AE31 MEM_MA_DATA37
MA_DATA38 AG28 MEM_MA_DATA38
MA_DATA39 AD28 MEM_MA_DATA39
MA_DATA40 AF26 MEM_MA_DATA40
MA_DATA41 AD25 MEM_MA_DATA41
MA_DATA42 AF23 MEM_MA_DATA42
MA_DATA43 AE23 MEM_MA_DATA43
MA_DATA44 AD27 MEM_MA_DATA44
MA_DATA45 AE26 MEM_MA_DATA45
MA_DATA46 AF24 MEM_MA_DATA46
MA_DATA47 AD24 MEM_MA_DATA47
MA_DATA48 AG22 MEM_MA_DATA48
MA_DATA49 AD21 MEM_MA_DATA49
MA_DATA50 AE19 MEM_MA_DATA50
MA_DATA51 AG19 MEM_MA_DATA51
MA_DATA52 AD22 MEM_MA_DATA52
MA_DATA53 AE22 MEM_MA_DATA53
MA_DATA54 AE20 MEM_MA_DATA54
MA_DATA55 AD19 MEM_MA_DATA55
MA_DATA56 AG18 MEM_MA_DATA56
MA_DATA57 AE17 MEM_MA_DATA57
MA_DATA58 AE15 MEM_MA_DATA58
MA_DATA59 AG15 MEM_MA_DATA59
MA_DATA60 AD18 MEM_MA_DATA60
MA_DATA61 AE18 MEM_MA_DATA61
MA_DATA62 AG16 MEM_MA_DATA62
MA_DATA63 AD15 MEM_MA_DATA63

ZIF-SOCKET904-HF-2
N12-9040040-L06

CPU1C
MEMORY CHANNEL B

MEM_MB_DATA[63..0] 13

13 MEM_MB_ADD[15..0]
MEM_MB_ADD0 V31 MB_ADD0
MEM_MB_ADD1 N28 MB_ADD1
MEM_MB_ADD2 P29 MB_ADD2
MEM_MB_ADD3 N29 MB_ADD3
MEM_MB_ADD4 N31 MB_ADD4
MEM_MB_ADD5 M30 MB_ADD5
MEM_MB_ADD6 M31 MB_ADD6
MEM_MB_ADD7 M28 MB_ADD7
MEM_MB_ADD8 M27 MB_ADD8
MEM_MB_ADD9 L30 MB_ADD9
MEM_MB_ADD10 W31 MB_ADD10
MEM_MB_ADD11 L29 MB_ADD11
MEM_MB_ADD12 K28 MB_ADD12
MEM_MB_ADD13 AB28 MB_ADD13
MEM_MB_ADD14 K31 MB_ADD14
MEM_MB_ADD15 J31 MB_ADD15

13 MEM_MB_BANK0
13 MEM_MB_BANK1
13 MEM_MB_BANK2
MEM_MB_BANK0 W29 MB_BANK0
MEM_MB_BANK1 V30 MB_BANK1
MEM_MB_BANK2 K29 MB_BANK2

MEM_MB_DM0 D16 MB_DM0
MEM_MB_DM1 B20 MB_DM1
MEM_MB_DM2 A25 MB_DM2
MEM_MB_DM3 D29 MB_DM3
MEM_MB_DM4 AL29 MB_DM4
MEM_MB_DM5 AH25 MB_DM5
MEM_MB_DM6 AK21 MB_DM6
MEM_MB_DM7 AJ17 MB_DM7

MEM_MB_DQS_H0 A17 MB_DQS_H0
MEM_MB_DQS_L0 B17 MB_DQS_L0
MEM_MB_DQS_H1 B21 MB_DQS_H1
MEM_MB_DQS_L1 C21 MB_DQS_L1
MEM_MB_DQS_H2 D25 MB_DQS_H2
MEM_MB_DQS_L2 C25 MB_DQS_L2
MEM_MB_DQS_H3 B29 MB_DQS_H3
MEM_MB_DQS_L3 A29 MB_DQS_L3
MEM_MB_DQS_H4 AJ29 MB_DQS_H4
MEM_MB_DQS_L4 AH29 MB_DQS_L4
MEM_MB_DQS_H5 AK25 MB_DQS_H5
MEM_MB_DQS_L5 AL25 MB_DQS_L5
MEM_MB_DQS_H6 AJ20 MB_DQS_H6
MEM_MB_DQS_L6 AJ21 MB_DQS_L6
MEM_MB_DQS_H7 AL16 MB_DQS_H7
MEM_MB_DQS_L7 AL17 MB_DQS_L7

13 MEM_MB_CLK_H0
13 MEM_MB_CLK_L0
MEM_MB_CLK_H0 U30 MB_CLK_H0
MEM_MB_CLK_L0 U29 MB_CLK_L0
T29 MB_CLK_H1
T28 MB_CLK_L1
R31 MB_CLK_H2
T31 MB_CLK_L2
13 MEM_MB_CLK_H3
13 MEM_MB_CLK_L3
MEM_MB_CLK_H3 P30 MB_CLK_H3
MEM_MB_CLK_L3 R30 MB_CLK_L3

13 MEM_MB_CKE0
13 MEM_MB_CKE1
MEM_MB_CKE0 J30 MB_CKE0
MEM_MB_CKE1 J28 MB_CKE1

AA30 MB0_ODT0
AC30 MB0_ODT1
13 MEM_MB1_ODT0
13 MEM_MB1_ODT1
MEM_MB1_ODT0 AA31 MB1_ODT0
MEM_MB1_ODT1 AC29 MB1_ODT1

Y29 MB0_CS_L0
AB29 MB0_CS_L1
13 MEM_MB1_CS_L0
13 MEM_MB1_CS_L1
MEM_MB1_CS_L0 Y30 MB1_CS_L0
MEM_MB1_CS_L1 AB31 MB1_CS_L1

13 MEM_MB_RAS_L
13 MEM_MB_CAS_L
13 MEM_MB_WE_L
MEM_MB_RAS_L W28 MB_RAS_L
MEM_MB_CAS_L AA27 MB_CAS_L
MEM_MB_WE_L AA28 MB_WE_L

13 MEM_MB_RESET#
13 MEM_MB_HOT#
MEM_MB_RESET# J27 MB_RESET_L
MEM_MB_HOT# V28 MB_EVENT_L

MB_DATA0 A16 MEM_MB_DATA0
MB_DATA1 C16 MEM_MB_DATA1
MB_DATA2 B18 MEM_MB_DATA2
MB_DATA3 A19 MEM_MB_DATA3
MB_DATA4 C15 MEM_MB_DATA4
MB_DATA5 B15 MEM_MB_DATA5
MB_DATA6 D17 MEM_MB_DATA6
MB_DATA7 C18 MEM_MB_DATA7
MB_DATA8 D20 MEM_MB_DATA8
MB_DATA9 A20 MEM_MB_DATA9
MB_DATA10 D22 MEM_MB_DATA10
MB_DATA11 D23 MEM_MB_DATA11
MB_DATA12 C19 MEM_MB_DATA12
MB_DATA13 D19 MEM_MB_DATA13
MB_DATA14 A22 MEM_MB_DATA14
MB_DATA15 C22 MEM_MB_DATA15
MB_DATA16 C24 MEM_MB_DATA16
MB_DATA17 B24 MEM_MB_DATA17
MB_DATA18 B26 MEM_MB_DATA18
MB_DATA19 C27 MEM_MB_DATA19
MB_DATA20 A23 MEM_MB_DATA20
MB_DATA21 B23 MEM_MB_DATA21
MB_DATA22 D26 MEM_MB_DATA22
MB_DATA23 A26 MEM_MB_DATA23
MB_DATA24 C28 MEM_MB_DATA24
MB_DATA25 D28 MEM_MB_DATA25
MB_DATA26 C31 MEM_MB_DATA26
MB_DATA27 D31 MEM_MB_DATA27
MB_DATA28 B27 MEM_MB_DATA28
MB_DATA29 A28 MEM_MB_DATA29
MB_DATA30 B30 MEM_MB_DATA30
MB_DATA31 C30 MEM_MB_DATA31
MB_DATA32 AJ30 MEM_MB_DATA32
MB_DATA33 AK30 MEM_MB_DATA33
MB_DATA34 AH28 MEM_MB_DATA34
MB_DATA35 AJ27 MEM_MB_DATA35
MB_DATA36 AG30 MEM_MB_DATA36
MB_DATA37 AH31 MEM_MB_DATA37
MB_DATA38 AK28 MEM_MB_DATA38
MB_DATA39 AL28 MEM_MB_DATA39
MB_DATA40 AJ26 MEM_MB_DATA40
MB_DATA41 AH26 MEM_MB_DATA41
MB_DATA42 AH23 MEM_MB_DATA42
MB_DATA43 AJ23 MEM_MB_DATA43
MB_DATA44 AK27 MEM_MB_DATA44
MB_DATA45 AL26 MEM_MB_DATA45
MB_DATA46 AJ24 MEM_MB_DATA46
MB_DATA47 AK24 MEM_MB_DATA47
MB_DATA48 AK22 MEM_MB_DATA48
MB_DATA49 AH22 MEM_MB_DATA49
MB_DATA50 AL19 MEM_MB_DATA50
MB_DATA51 AK19 MEM_MB_DATA51
MB_DATA52 AL23 MEM_MB_DATA52
MB_DATA53 AL22 MEM_MB_DATA53
MB_DATA54 AH20 MEM_MB_DATA54
MB_DATA55 AL20 MEM_MB_DATA55
MB_DATA56 AJ18 MEM_MB_DATA56
MB_DATA57 AH17 MEM_MB_DATA57
MB_DATA58 AJ15 MEM_MB_DATA58
MB_DATA59 AK15 MEM_MB_DATA59
MB_DATA60 AH19 MEM_MB_DATA60
MB_DATA61 AK18 MEM_MB_DATA61
MB_DATA62 AK16 MEM_MB_DATA62
MB_DATA63 AH16 MEM_MB_DATA63

ZIF-SOCKET904-HF-2
N12-9040040-L06

VCC_DDR
R206 1KR1%
R205 1KR1%
C175 C1000p50X0402
APU_M_VREF
C641 C0.1u0X0402
C642 C1000p50X0402
Layout: Place within 1.0'' of APU
VCC_DDR
R219 1KR0402 MEM_MA_HOT#
R221 1KR0402 MEM_MB_HOT#

MSI Link to the Future MICRO-START INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | MS-7800 | |
| Size: Custom | Document Number: FM2 DDR3 I/F | Rev: 10 |
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# FM2 DISPLAY I/F

ROUTE PCIE AS 85OHM +/-10%

PLACE CAPS WITH APU < 1 INCH
Trace length within 10"

mach@DP0 for HDMI

| | | | | | |
|---|---|---|---|---|---|
| 21 | DP0_TX0P | C146 C0.1u10X0402 | DP0_TX0P_APU | N4 | DP0_TXP0 |
| 21 | DP0_TX0N | C142 C0.1u10X0402 | DP0_TX0N_APU | N5 | DP0_TXN0 |
| 21 | DP0_TX1P | C148 C0.1u10X0402 | DP0_TX1P_APU | M2 | DP0_TXP1 |
| 21 | DP0_TX1N | C153 C0.1u10X0402 | DP0_TX1N_APU | M3 | DP0_TXN1 |
| 21 | DP0_TX2P | C140 C0.1u10X0402 | DP0_TX2P_APU | L2 | DP0_TXP2 |
| 21 | DP0_TX2N | C138 C0.1u10X0402 | DP0_TX2N_APU | L1 | DP0_TXN2 |
| 21 | DP0_TX3P | C155 C0.1u10X0402 | DP0_TX3P_APU | L4 | DP0_TXP3 |
| 21 | DP0_TX3N | C158 C0.1u10X0402 | DP0_TX3N_APU | L5 | DP0_TXN3 |

| | | | | | |
|---|---|---|---|---|---|
| 18 | DP1_TX0P | C193 C0.1u10X0402 | DP1_TX0P_APU | K2 | DP1_TXP0 |
| 18 | DP1_TX0N | C197 C0.1u10X0402 | DP1_TX0N_APU | K3 | DP1_TXN0 |
| 18 | DP1_TX1P | C195 C0.1u10X0402 | DP1_TX1P_APU | J2 | DP1_TXP1 |
| 18 | DP1_TX1N | C194 C0.1u10X0402 | DP1_TX1N_APU | J1 | DP1_TXN1 |
| 18 | DP1_TX2P | C203 C0.1u10X0402 | DP1_TX2P_APU | J4 | DP1_TXP2 |
| 18 | DP1_TX2N | C206 C0.1u10X0402 | DP1_TX2N_APU | J5 | DP1_TXN2 |
| 18 | DP1_TX3P | C174 C0.1u10X0402 | DP1_TX3P_APU | H2 | DP1_TXP3 |
| 18 | DP1_TX3N | C178 C0.1u10X0402 | DP1_TX3N_APU | H3 | DP1_TXN3 |

mach@DP1 for CRT

CPU1D

ANALOG/DISPLAY/MISC

DISPLAY PORT 0 · DISPLAY PORT MISC. · DISPLAY PORT 1 · DISPLAY PORT 2 · TEST · CLK · MISC · SER · CTRL · RSVD · JTAG · SENSE

| | | | | | |
|---|---|---|---|---|---|
| DP_AUX_ZVSS | G9 | DP_AUX_ZVSS | R555 | 150R1%0402 | Layout: Place within 1.5'' of APU |
| DP_BLON | F8 | APU_BLON | | | |
| DP_DIGON | G8 | APU_DIGON | | | |
| DP_VARY_BL | E8 | APU_BLPWM | | | |
| DP0_AUXP | F1 | DP0_AUXP_C | 21 | | |
| DP0_AUXN | F2 | DP0_AUXN_C | 21 | | |
| DP1_AUXP | F1 | DP1_AUXP_C | 18 | | |
| DP1_AUXN | F2 | DP1_AUXN_C | 18 | | |
| DP2_AUXP | G1 | | | | |
| DP2_AUXN | G2 | | | | |
| DP3_AUXP | E5 | | | | |
| DP3_AUXN | E6 | | | | |
| DP4_AUXP | F5 | | | | |
| DP4_AUXN | F6 | | | | |
| DP5_AUXP | G5 | | | | |
| DP5_AUXN | G6 | | | | |
| DP0_HPD | E3 | DP0_HPD_HDMI_C | 21 | | |
| DP1_HPD | F3 | DP1_HPD_VGA_C | 18 | | |
| DP2_HPD | G3 | DP2_HPD | R204 | 100KR0402 | |
| DP3_HPD | E7 | DP3_HPD | R187 | 100KR0402 | |
| DP4_HPD | F7 | DP4_HPD | R188 | 100KR0402 | |
| DP5_HPD | G7 | DP5_HPD | R180 | 100KR0402 | |

| | | | | | |
|---|---|---|---|---|---|
| TEST4 | T21 | APU_TEST4 | TP37 | | |
| TEST5 | U21 | APU_TEST5 | TP38 | | |
| TEST6 | AD14 | APU_TEST6 | TP41 | | |
| TEST9 | P21 | APU_TEST9 | TP34 | | |
| TEST10 | R21 | APU_TEST10 | TP36 | | |
| TEST14 | F12 | APU_TEST14 | TP28 | | |
| TEST15 | E12 | APU_TEST15 | TP27 | | |
| TEST16 | F13 | APU_TEST16 | TP33 | | |
| TEST17 | E13 | APU_TEST17 | TP25 | | |
| TEST18 | G13 | APU_TEST18 | R156 | 1KR0402 | |
| TEST19 | G14 | APU_TEST19 | R148 | 1KR0402 | |
| TEST20 | F14 | APU_TEST20 | R149 | 1KR0402 | |
| TEST24 | E14 | APU_TEST24 | R153 | 1KR0402 | |
| TEST25_H | AJ11 | APU_TEST25_H | R236 | 511R1%0402 | CPU_VDDP |
| TEST25_L | AH11 | APU_TEST25_L | R557 | 511R1%0402 | |
| TEST28_H | H10 | APU_TEST28_H | TP32 | | |
| TEST28_L | J10 | APU_TEST28_L | TP31 | | |
| TEST30_H | T22 | APU_TEST30_H | TP40 | | |
| TEST30_L | U22 | APU_TEST30_L | TP42 | | |
| TEST31 | AG31 | APU_TEST31 | R218 | 39.2R1%0402 | |
| TEST32_H | V22 | APU_TEST32_H | TP39 | | |
| TEST32_L | R22 | APU_TEST32L | TP35 | | |
| TEST35 | AE14 | APU_TEST35 | R229 | X_300R0402 | VCC_DDR |
| | | | R234 | 300R0402 | |

| | | | | | |
|---|---|---|---|---|---|
| FM2R1 | AC10 | APU_FM2R1 | APU_FM2R1 | 7 | |
| DMAACTIVE_L | AG14 | FCH_DMA_ACTIVE# | FCH_DMA_ACTIVE# | 16 | |
| LDTSTOP_L | AD10 | LDTSTOP_L | LDTSTOP_L | 16 | |
| BP5/IDLEEXIT_L | G12 | FM_IDLEEXIT_L | | | |
| CORETYPE | F9 | | | | |

Sabine HDMI Design Guidance
HDMI enable strapping:
TEST35 PU TO VCC_DDR thru 300R

| | | | | | |
|---|---|---|---|---|---|
| RSVD1 | AJ13 | | | | |
| RSVD2 | AH13 | | | | |
| RSVD3 | AD12 | | | | |
| RSVD4 | K23 | | | | |
| RSVD5 | K25 | | | | |
| RSVD6 | AB23 | | | | |
| RSVD7 | AC24 | | | | |
| RSVD8 | AG10 | | | | |

| | | | | | |
|---|---|---|---|---|---|
| VDDP_SENSE | C3 | VDDP_SENSE | 27 | | |
| VDDNB_SENSE | A3 | NB_SENSE+ | 7 | | |
| VDDIO_SENSE | A4 | VDDIOFB+ | 27 | | |
| VDD_SENSE | B3 | COREFB+ | 7 | | |
| VDDR_SENSE | C4 | VDDR_SENSE | 27 | | |
| VSS_SENSE | B4 | COREFB- | 7 | | |
| | | NB_SENSE- | 7 | | |

| | | | | | |
|---|---|---|---|---|---|
| CLKIN_H | AL12 | 16 | APU_CLK | | |
| CLKIN_L | AK12 | 16 | APU_CLK# | | |
| DISP_CLKIN_H | AG12 | 16 | DISP_CLK | | |
| DISP_CLKIN_L | AF12 | 16 | DISP_CLK# | | |

| | | | | | |
|---|---|---|---|---|---|
| SVC | C1 | APU_SVC_R | | | |
| SVD | C2 | APU_SVD_R | | | |
| SVT | D1 | APU_SVT_R | | | |
| SIC | AK14 | 25 | APU_SIC | C292 | X_C10p50N0402 |
| SID | AL14 | 25 | APU_SID | R238 | 10R0402 APU_SIC_R |
| RESET_L | AF10 | APU_RST# | | C291 | C180p50N0402 |
| PWROK | AF14 | APU_PWRGD | | | |
| PROCHOT_L | AE10 | APU_PROCHOT# | | C301 | C180p50N0402 |
| THERMTRIP_L | AH14 | APU_THERMTRIP# | | | |
| ALERT_L | AJ14 | APU_ALERT# | | | |
| TDI | G11 | CPU_TDI | | | |
| TDO | E10 | CPU_TDO | | | |
| TCK | F11 | CPU_TCK | | | |
| TMS | F11 | CPU_TMS | | | |
| TRST_L | F10 | CPU_TRST_L | | | |
| DBRDY | G10 | CPU_DBRDY | | | |
| DBREQ_L | E9 | CPU_DBREQ_L | | | |

16 APU_RST#
16 APU_PWRGD

ZIF-SOCKET904-HF-2

N12-9040040-L06

## PULL UP

VCC_DDR

| | | |
|---|---|---|
| R235 1KR0402 | APU_SIC_R | |
| R237 1KR0402 | APU_SID | |
| R244 300R0402 | APU_RST# | |
| R239 300R0402 | APU_PWRGD | |
| R263 300R0402 | APU_PROCHOT# | |
| R298 1KR0402 | APU_THERMTRIP# | |
| R295 1KR0402 | APU_ALERT# | |

## HDT+ Connector

VCC_DDR

J1

| | | | |
|---|---|---|---|
| 1 | CPU_VDDIO | CPU_TCK | 2 |
| 3 | GND | CPU_TMS | 4 |
| 5 | GND | CPU_TDI | 6 |
| 7 | GND | CPU_TDO | 8 |
| 9 | CPU_TRST_L | CPU_PWROK_BUF | 10 |
| 11 | CPU_DBRDY3 | CPU_RST_L_BUF | 12 |
| 13 | CPU_DBRDY2 | CPU_DBRDY0 | 14 |
| 15 | CPU_DBRDY1 | CPU_DBREQ_L | 16 |
| 17 | GND | CPU_PLLTEST0 | 18 |
| 19 | CPU_VDDIO | CPU_PLLTEST1 | 20 |

X_H2X10SM-1.27PITCH_BLUE-RH

N31-2100170-S88

| | | | |
|---|---|---|---|
| CPU_TCK | CPU_TMS | CPU_TDI | CPU_TDO |
| APU_PWROK_BUF | APU_LDT_RST_BUF | CPU_DBRDY | CPU_DBREQ_L |
| APU_TEST19 | APU_TEST18 | | |

CPU_TRST_L R551 X_0R0402
R552 X_10KR0402
R553 X_10KR0402
R554 X_10KR0402

VCC3

R3 X_10KR0402
Q2 X_N-SST3904_SOT23
APU_PWRGD E C APU_PWROK_BUF

R2 X_10KR0402
Q1 X_N-SST3904_SOT23
APU_RST# R1 X_0R0402 E C APU_LDT_RST_BUF

## VID OVERRIDE CIRCUIT

VCC_DDR

R175 1KR0402
R177 1KR0402
R160 1KR0402
R166 X_1KR0402
R163 X_1KR0402
R152 X_1KR0402

| | | | |
|---|---|---|---|
| APU_SVC_R | R162 0R0402 | APU_SVC | 7 |
| APU_SVD_R | R167 0R0402 | APU_SVD | 7 |
| APU_SVT_R | R155 33R0402 | APU_SVT | 7 |
| APU_PWRGD | R87 X_R/2 | VRM_PWROK | 7 |

R159 X_1KR0402
R154 X_1KR0402
R151 X_1KR0402
R91 X_220R0402

To overide VID:remove
R520,R521
Stuff R82 to enter FIX mode

| SVC | SVD | BOOT Voltage Pre-PWROK metel VID | V FIX MODE |
|---|---|---|---|
| 0 | 0 | 1.1 | 1.4 |
| 0 | 1 | 1.0 | 1.2 |
| 1 | 0 | 0.9 | 1.0 |
| 1 | 1 | 0.8 | 0.8 |

## SCAN Conn,

| | |
|---|---|
| APU_TEST18 | TP20 |
| APU_TEST19 | TP19 |
| APU_TEST24 | TP24 |
| APU_TEST20 | TP23 |

## WARM RESET

APU_RST# TP43

## GPU DEBUG

| | |
|---|---|
| APU_BLON | TP29 |
| APU_DIGON | TP30 |
| APU_BLPWM | TP26 |
| DP1_HPD_VGA_C | TP21 |
| VDDIOFB+ | TP2 |
| COREFB+ | TP22 |

VCC_DDR

R161 1KR0402
R51 10KR0402
Q21 N-SST3904_SOT23
FM_IDLEEXIT_L E C FCH_IDLEEXIT_L 17

VCC_DDR Layout: Place close to HDT header

| | | | |
|---|---|---|---|
| R181 | 1KR0402 | CPU_TDI | |
| R168 | 1KR0402 | CPU_TCK | |
| R176 | 1KR0402 | CPU_TMS | |
| R164 | 1KR0402 | CPU_TRST_L | |
| R189 | 300R0402 | CPU_DBREQ_L | |

VCC_DDR 3VDUAL

R300 10KR0402
R430 10KR0402
Q52 N-SST3904_SOT23
APU_THERMTRIP# E C FCH_THERMTRIP# 17

VCC_DDR 3VDUAL

R296 10KR0402
R416 10KR0402
Q53 N-SST3904_SOT23
APU_ALERT# E C FCH_TALERT# 18

VCC_DDR 3VDUAL

R262 X_10KR0402
R267 X_10KR0402
Q48 X_N-SST3904_SOT23
APU_PROCHOT# E C FCH_PROCHOT# 16
R265 0R0402

3VDUAL

APU_FM2R1 R47 10KR0402

VCC_DDR

FCH_DMA_ACTIVE# R228 1KR0402
LDTSTOP_L R233 1KR0402

| DP0 | DP0_TX0,TX1,TX2 and TX3<br>DP0_AUX0 and DP0_HPD |
|---|---|
| DP1 | DP1_TX0,TX1,TX2 and TX3<br>DP1_AUX0 and DP1_HPD |

| | | | |
|---|---|---|---|
| MSI | MICRO-START INT'L CO.,LTD. | | |
| Title | MS-7800 | | |
| Size Custom | Document Number FM2 DISPLAY/MSIC | | Rev 10 |
| Date: Friday, April 06, 2012 | | Sheet 10 of 36 | |

# FM1 DECOUPLING CAPS

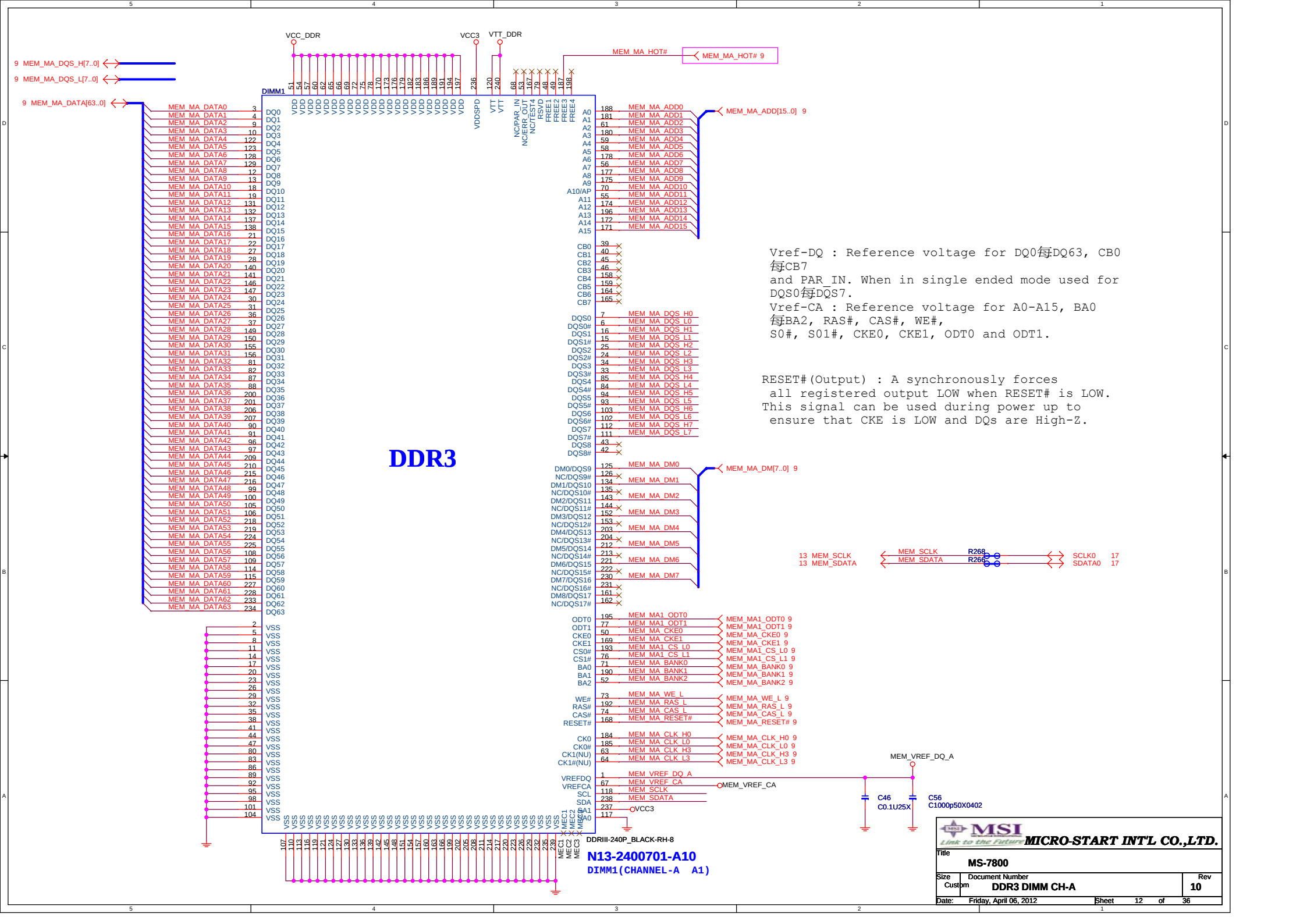
| | VSS | VDD | VDDNB | VDDIO | VDDP | VDDR | | | VDDA | Mvref |
|---|---|---|---|---|---|---|---|---|---|---|
| TOTLE POWER PINS | | | | | COMB | COMB | SPLIT | SPLIT | | |
| 416 | 226 | 102 | 19 | 51 | 8 | 8 | 4 | 4 | 2 | 1 |
| VALUE/SIZE/ MATERIAL | | | | | | | NEAR | FAR | | |
| 22U/1206/X5R | / | 11 | 2 | 4 | / | 1 | / | / | / | / |
| 10U/0805/X5R | / | 7 | 2 | 1 | 2+1(B) | 1 | / | / | / | / |
| 4.7U/0805/X5R | / | 3 | 1 | 4 | 2 | 2+2 | 2 | 2 | 1 | / |
| 0.22U/0603/X5R | / | 2 | 2 | 2+2 | 2 | 2+2 | 2 | 2 | 1 | / |
| 0.1U/0603/X5R | / | / | / | / | / | / | / | / | / | 1 |
| 0.01U/0603/X5R | / | 4 | / | / | / | / | / | / | / | / |
| 3.3 nF/0603/X5R | / | / | / | / | / | | / | / | 1 | |
| 1 nF/0603/X5R | / | / | / | / | / | / | / | / | / | 1 |
| 1 nF/0603/X5R | / | / | / | / | 4 | / | / | / | / | / |
| 180 pF/0603/X5R | / | 3 | 1 | 2+2 | 2+2 | 2 | / | / | / | / |

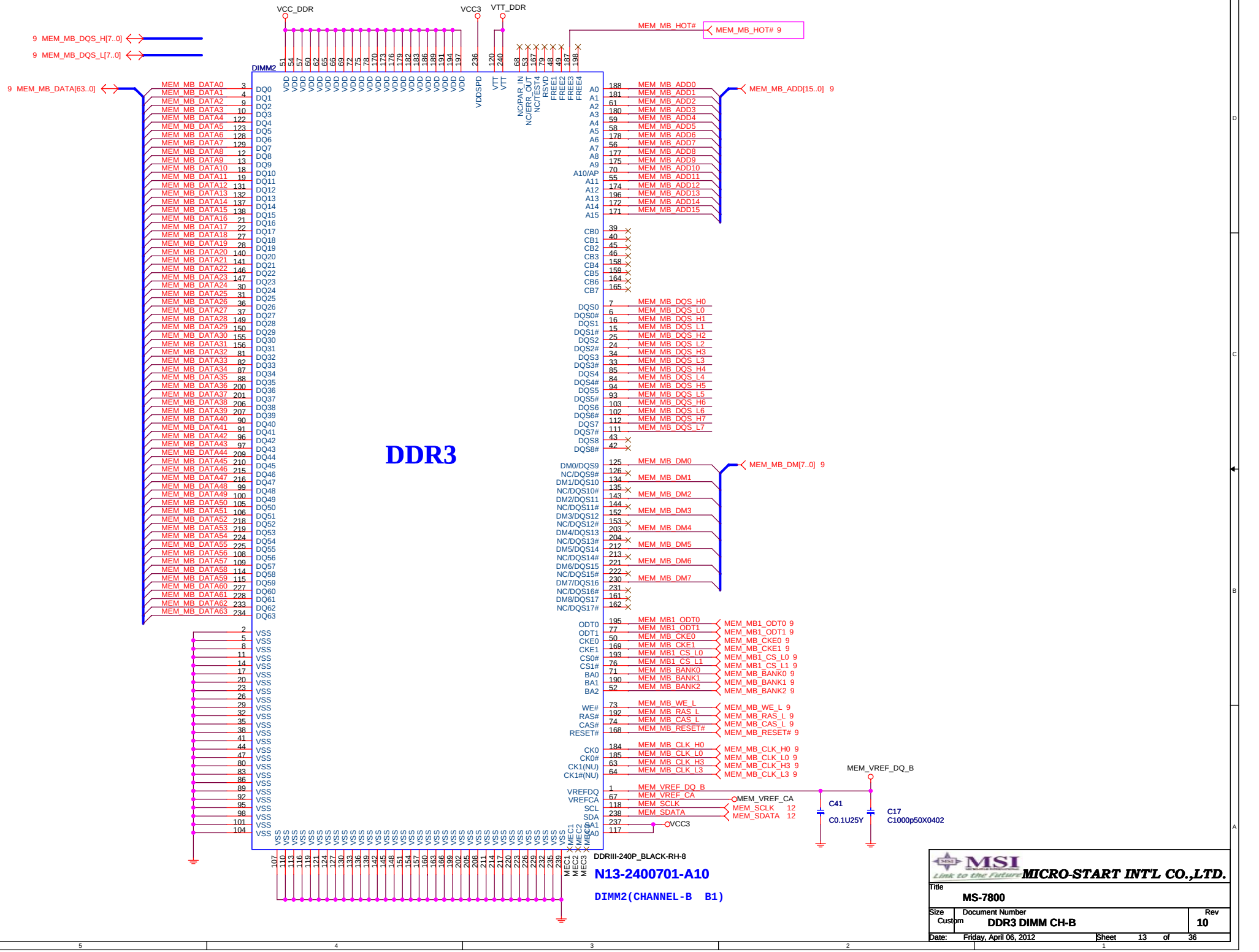
VDDR = 1.2V
VDDPCIE = 1.2V
ONLY ONE SIDE OF VDDPCIE & VDDR MUST CONNECTED ON THE PCB.CONNECTING BOTH SIDES IS ACCEPTABLE BUT NOT REQUIRED. BOTH SIDES MUST BE DECOUPLED.

VDDP and VDDR support two separate power planes with single regulator

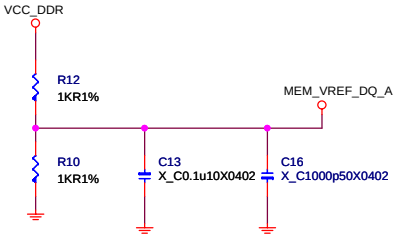
| | |
|---|---|
| Title | MS-7800 |
| Size | C |
| Document Number | FM2 POWER&DECOUPLING |
| Rev | 10 |
| Date: | Friday, April 06, 2012 |
| Sheet | 11 of 36 |

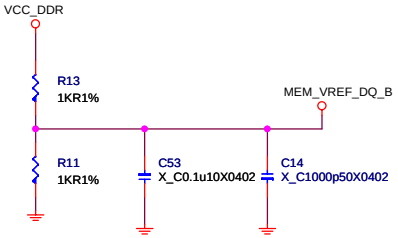
MICRO-STAR INT'L CO.,LTD.

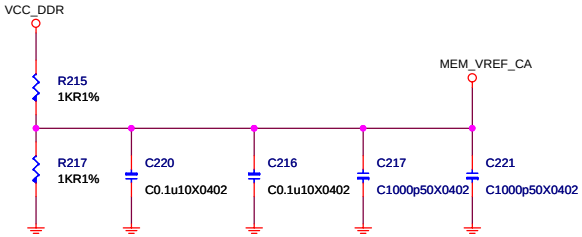

DDR3
DIMM1
VCC_DDR
VCC3
VTT_DDR
MEM_MA_HOT#
MEM_MA_HOT# 9
9 MEM_MA_DQS_H[7..0]
9 MEM_MA_DQS_L[7..0]
9 MEM_MA_DATA[63..0]
MEM_MA_ADD[15..0] 9
MEM_MA_DM[7..0] 9
Vref-DQ : Reference voltage for DQ0每DQ63, CB0 每CB7
and PAR_IN. When in single ended mode used for DQS0每DQS7.
Vref-CA : Reference voltage for A0-A15, BA0 每BA2, RAS#, CAS#, WE#,
S0#, S01#, CKE0, CKE1, ODT0 and ODT1.
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
13 MEM_SCLK
13 MEM_SDATA
MEM_SCLK
MEM_SDATA
R268
R266
SCLK0 17
SDATA0 17
MEM_VREF_DQ_A
MEM_VREF_CA
C46
C0.1U25X
C56
C1000p50X0402
DDRIII-240P_BLACK-RH-8
N13-2400701-A10
DIMM1(CHANNEL-A A1)
MICRO-START INT'L CO.,LTD.
Title
MS-7800
Size
Custom
Document Number
DDR3 DIMM CH-A
Rev
10
Date: Friday, April 06, 2012
Sheet 12 of 36


VCC_DDR
VCC3
VTT_DDR
9 MEM_MB_DQS_H[7..0]
9 MEM_MB_DQS_L[7..0]
9 MEM_MB_DATA[63..0]
MEM_MB_HOT#
MEM_MB_HOT# 9
DIMM2
DDR3
MEM_MB_ADD[15..0] 9
MEM_MB_DM[7..0] 9
MEM_MB1_ODT0 9
MEM_MB1_ODT1 9
MEM_MB_CKE0 9
MEM_MB_CKE1 9
MEM_MB1_CS_L0 9
MEM_MB1_CS_L1 9
MEM_MB_BANK0 9
MEM_MB_BANK1 9
MEM_MB_BANK2 9
MEM_MB_WE_L 9
MEM_MB_RAS_L 9
MEM_MB_CAS_L 9
MEM_MB_RESET# 9
MEM_MB_CLK_H0 9
MEM_MB_CLK_L0 9
MEM_MB_CLK_H3 9
MEM_MB_CLK_L3 9
MEM_VREF_DQ_B
MEM_VREF_CA
MEM_SCLK 12
MEM_SDATA 12
VCC3
C41
C0.1U25Y
C17
C1000p50X0402
DDRIII-240P_BLACK-RH-8
N13-2400701-A10
DIMM2(CHANNEL-B B1)
MICRO-START INT'L CO.,LTD.
Title
MS-7800
Size
Custom
Document Number
DDR3 DIMM CH-B
Rev
10
Date: Friday, April 06, 2012
Sheet 13 of 36

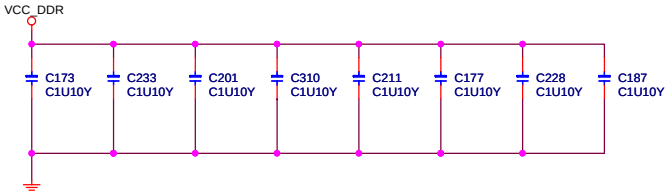
# DDR REF POWER & CAPS

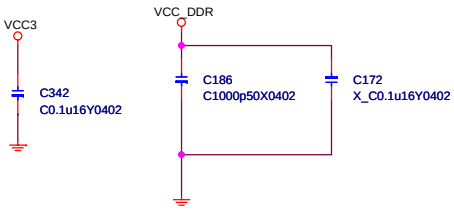


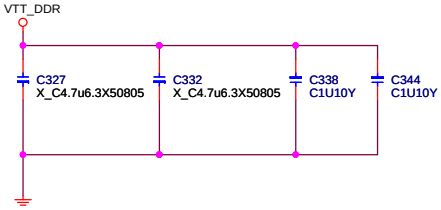




De-coupling Caps For DIMMs



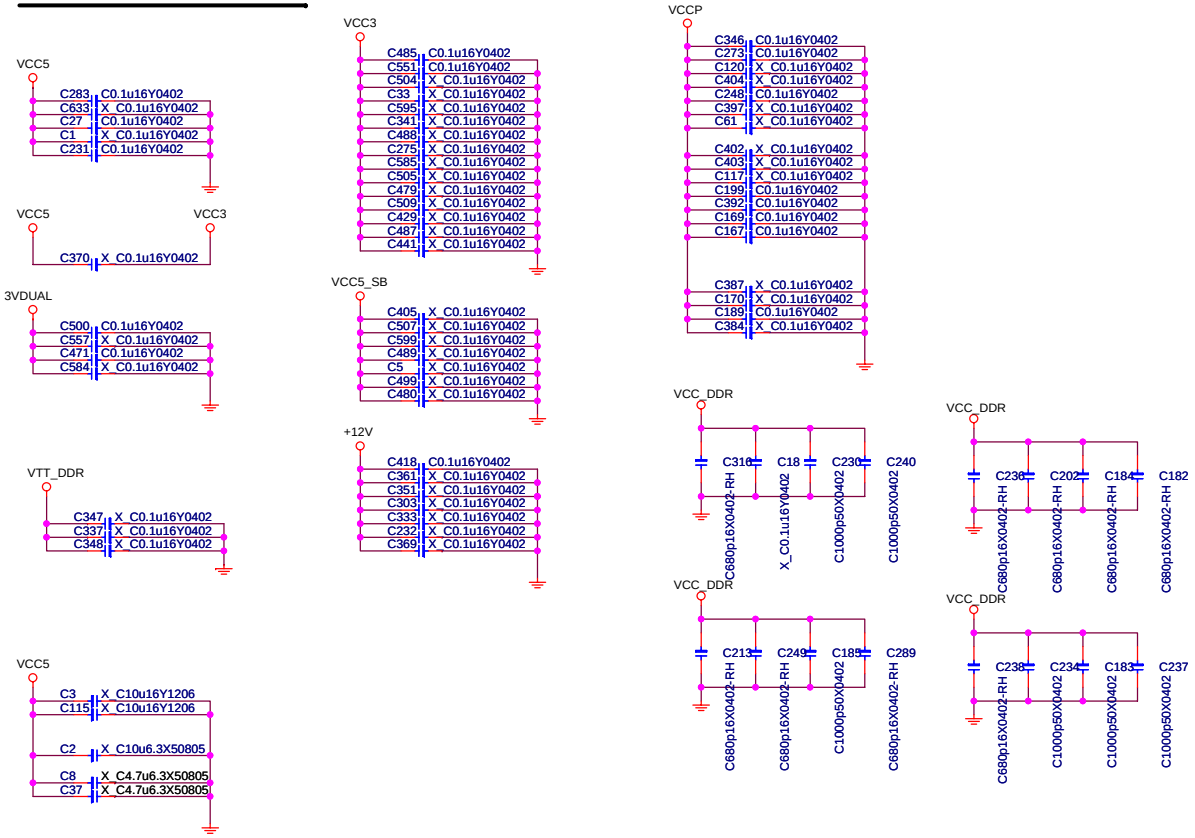




MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

| | | |
|---|---|---|
| Title: MMS-7800 | | |
| Size: Custom | Document Number: DDR REF POWER AND CAPS | Rev: 10 |
| Date: Friday, April 06, 2012 | Sheet 14 of 36 | |

# EMI Reserved




| | | |
|---|---|---|
| MSI Link to the Future | MICRO-START INT'L CO.,LTD. | |
| Title: MS-7800 | | |
| Size: Custom | Document Number: EMI Reserved | Rev: 10 |
| Date: Friday, April 06, 2012 | Sheet 15 of 36 | |

# HUDSON PCIE/PCI/APU/LPC/CLK

If PCI not implemented: Provide test points
or other means to allowaccess for debug purposes.
use these balls for alternate GPIO/GPO functions
or leave unconnected.

U30E
HUDSON-2
Part 1 of 5

## CLEAR CMOS

CMOS CLEAR JUMPER
CLR_COMS Clear CMOS

| | |
|---|---|
| 1 - 2 | Normal |
| 2 - 3 | Clear CMOS |

N41-1030191-H06

B01-21807F5-A08

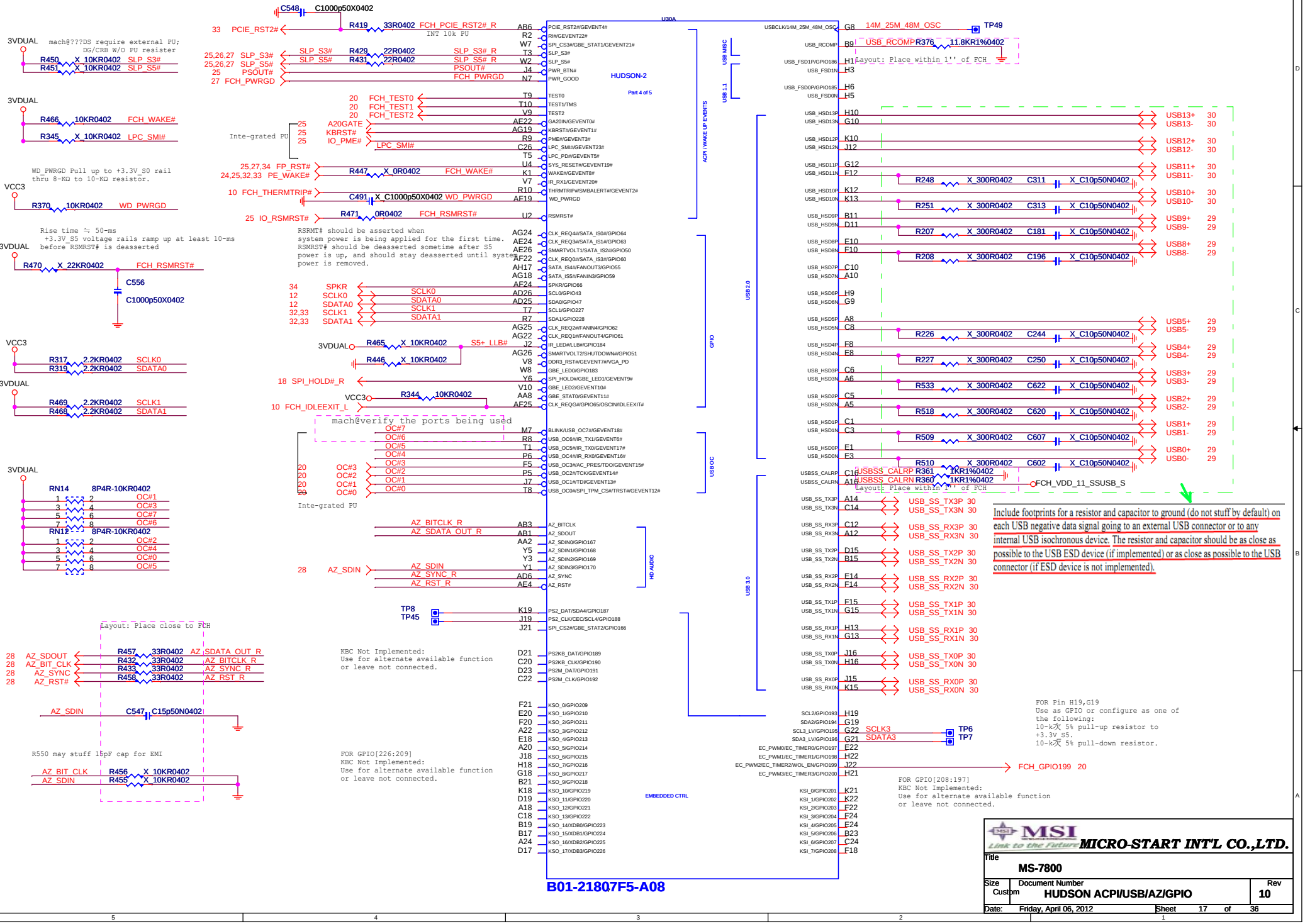
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the APU I/O rail. They are also in the S5 domain to prevent glitching at power up.

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

| | |
|---|---|
| Title | MS-7800 |
| Size | Custom |
| Document Number | HUDSON PCIE/PCI/APU/LPC/CLK |
| Rev | 10 |
| Date: | Friday, April 06, 2012 |
| Sheet | 16 of 36 |

MICRO-START INT'L CO.,LTD.

# HUDSON ACPI/USB/AZ/GPIO

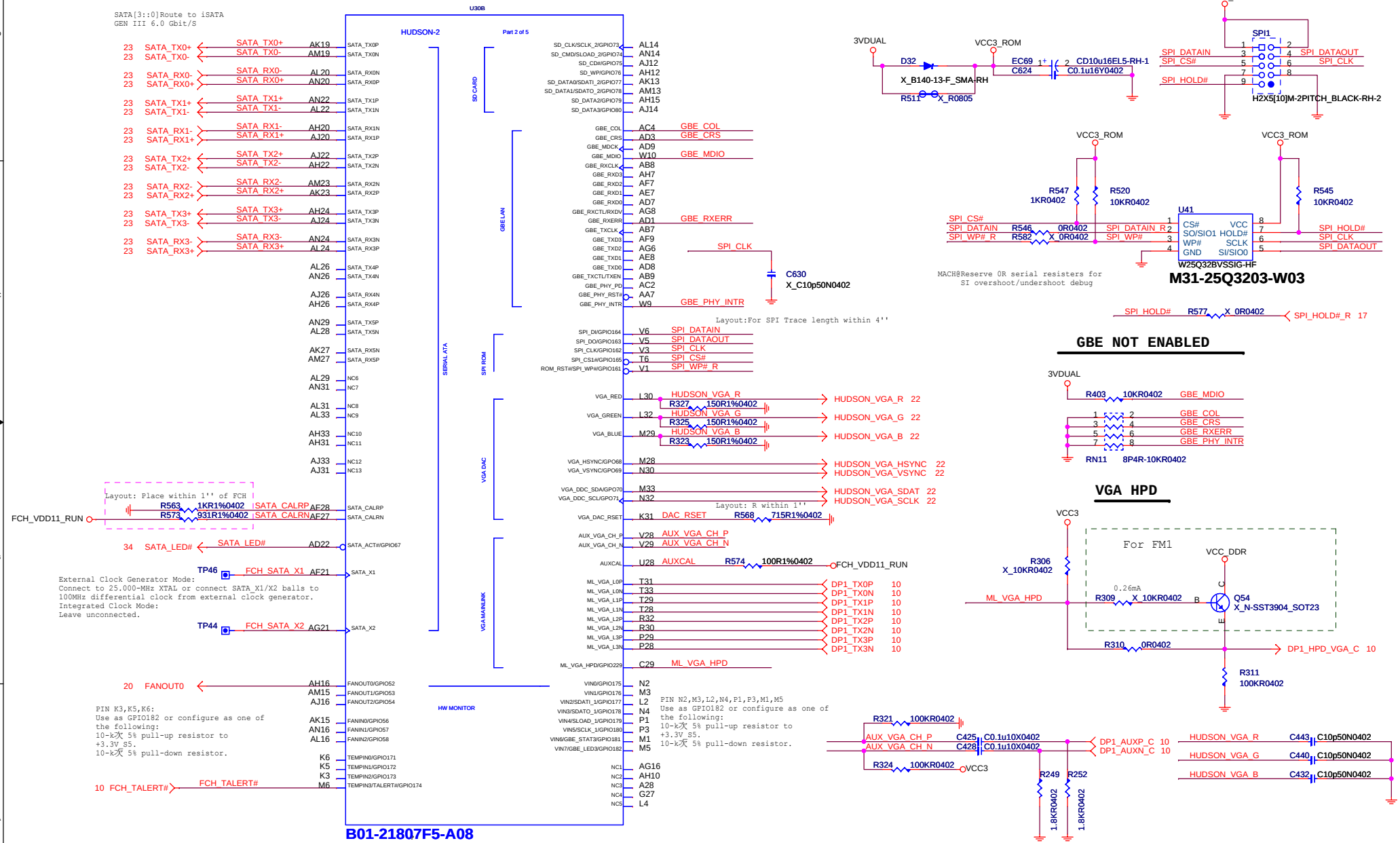



| | |
|---|---|
| Title | MS-7800 |
| Size | Custom |
| Document Number | HUDSON ACPI/USB/AZ/GPIO |
| Rev | 10 |
| Date: | Friday, April 06, 2012 |
| Sheet | 17 of 36 |

MICRO-START INT'L CO.,LTD.

# HUDSON SATA/VGA/SPI/HWM

**LAYOUT:**
**ROUTE SATA TX DIFF PAIR @ 100 OHM+/-10%**
**RX DIFF PAIR @ 90 OHM+/-10%**




MICRO-START INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | MS-7800 | |
| Size: Custom | Document Number: HUDSON SATA/VGA/HWM/SPI | Rev: 10 |
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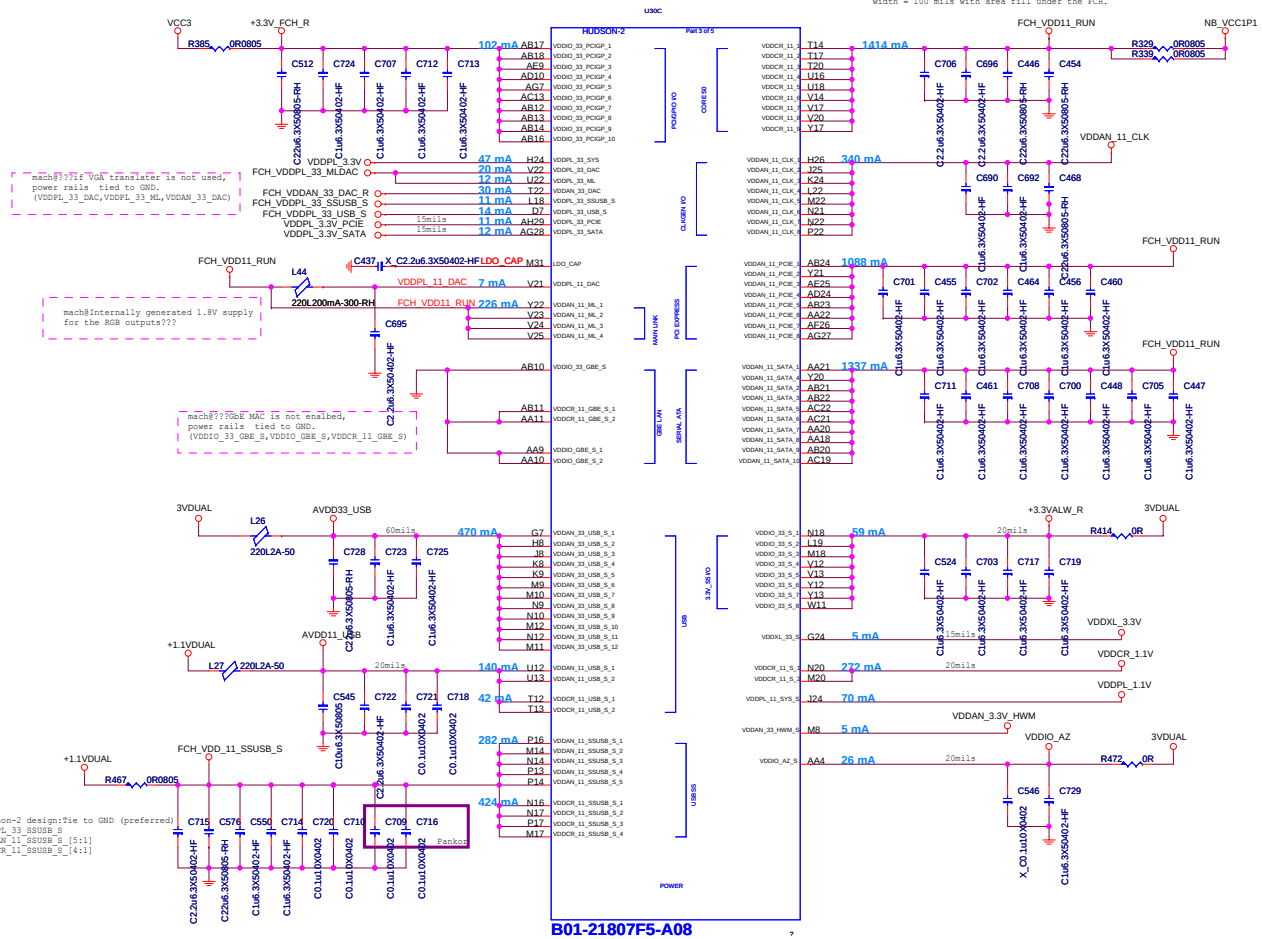
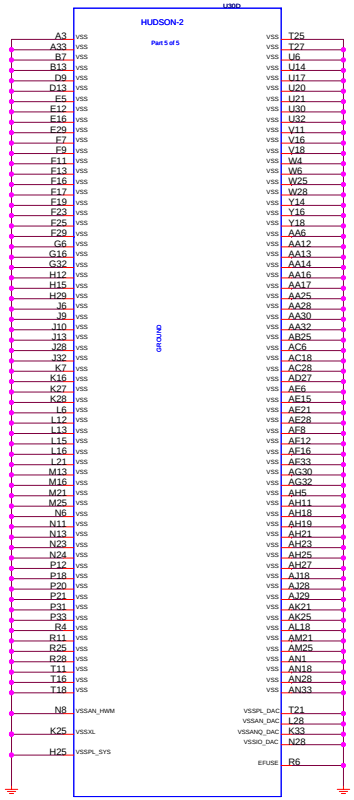
# HUDSON POWER&DECOUPLING

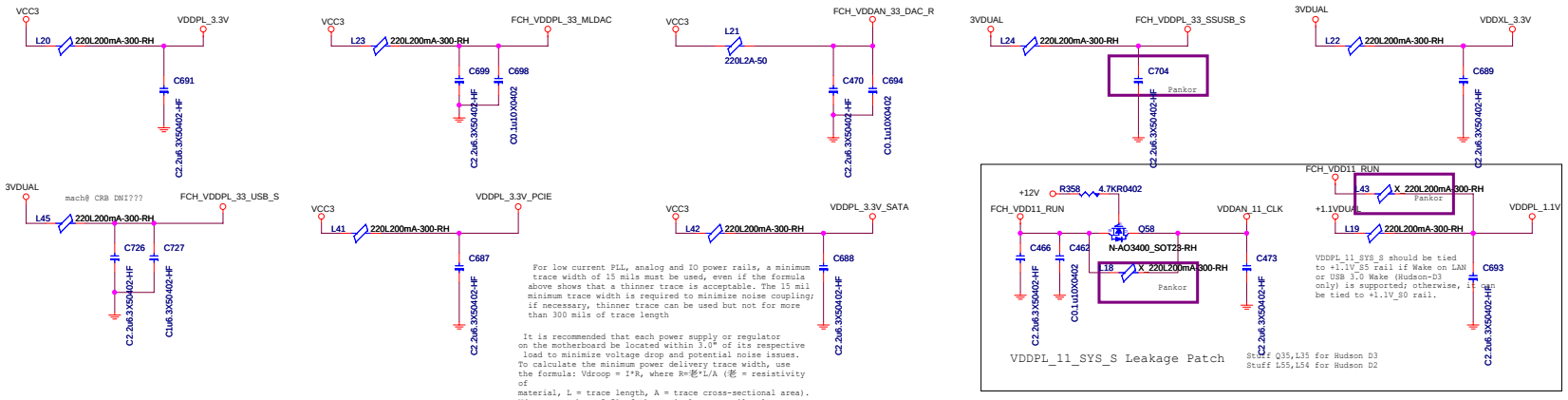



| Power Rails | Hudson D3 |
|---|---|
| **NB_VCC1P1** | max 4118 mA |
| VDDCR_11_[9:1] | 1120 mA |
| VDDAN_11_CLK_[8:1] | 340 mA |
| VDDAN_11_PCIE_[8:1] | 1088 mA |
| VDDAN_11_SATA_[10:1] | 1337 mA |
| VDDAN_11_ML_[4:1] | 226 mA |
| VDDPL_11_DAC | 7 mA |
| | |
| **VCC3** | max 234 mA |
| VDDIO_33_PCIGP_[10:1] | 102 mA |
| VDDPL_33_SYS | 47 mA |
| VDDPL_33_DAC | 20 mA |
| VDDPL_33_ML | 12 mA |
| VDDPL_33_PCIE | 11 mA |
| VDDPL_33_SATA | 12 mA |
| VDDAN_33_DAC | 30 mA |
| | |
| **VCC3_SB** | max 597 mA |
| VDDIO_33_S_[8:1] | 59 mA |
| VDDIO_AZ_S | 26 mA |
| VDDXL_33_S | 5 mA |
| VDDAN_33_HWM_S | 12 mA |
| VDDIO_GBE_S[2:1] | GND |
| VDDIO_33_GBE_S | GND |
| VDDPL_33_USB_S | 14 mA |
| VDDAN_33_USB_S_[12:1] | 470 mA |
| VDDPL_33_SSUSB_S | 11 mA |
| | |
| **+1.1VDUAL** | max 1230 mA |
| VDDCR_11_S_[2:1] | 272 mA |
| VDDCR_11_GBE_S[2:1] | GND |
| VDDPL_11_SYS_S | 70 mA |
| VDDAN_11_USB_S_[2:1] | 140 mA |
| VDDCR_11_USB_S_[2:1] | 42 mA |
| VDDAN_11_SSUSB_S_[5:1] | 282 mA |
| VDDCR_11_SSUSB_S_[4:1] | 424 mA |




Layout:
VSSPL_SYS;VSSAN_HWM CONNECT TO GND WITH A SEPREATED VIA

LAYOUT:
ROUTE THE POWER TRACES 15MILS WIDTH AT LEAST
PLACE THE DECOUPING CAPS CLOSE TO FCH ASAP
PLACE FB<=1" ,CAPS <=0.2"




For low current PLL, analog and IO power rails, a minimum trace width of 15 mils must be used, even if the formula above shows that a thinner trace is acceptable. The 15 mil minimum trace width is required to minimize noise coupling; if necessary, thinner trace can be used but not for more than 300 mils of trace length

It is recommended that each power supply or regulator on the motherboard be located within 3.0" of its respective load to minimize voltage drop and potential noise issues. To calculate the minimum power delivery trace width, use the formula: Vdroop = I*R, where R=ρ*L/A (ρ = resistivity of material, L = trace length, A = trace cross-sectional area). Vdroop must be < 2.5% of the nominal power rail voltage under maximum current conditions

VDDPL_11_SYS_S should be tied to +1.1V_S5 rail if Wake on LAN or USB 3.0 Wake (Hudson-D3 only) is supported; otherwise, it can be tied to +1.1V_S0 rail.

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| | | |
|---|---|---|
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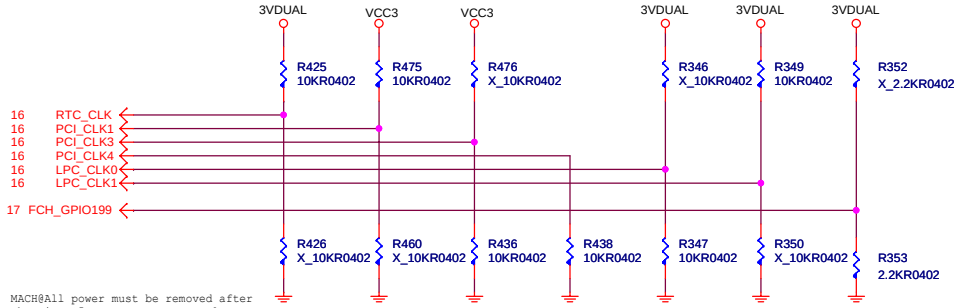
# FCH REQUIRED STRAPS



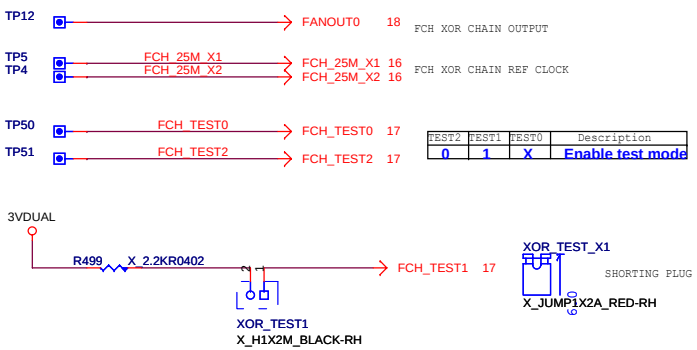

| | RTCCLK | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | GPIO199 |
|---|---|---|---|---|---|---|---|
| PULL HIGH | S5 PLUS MODE DISABLED DEFAULT | ALLOW PCIE GEN2 DEFAULT | USE DEBUG STRAPS | Reserved | EC ENABLED | INTERNAL CLOCK GEN ENABLED DEFAULT | LPC ROM |
| PULL LOW | S5 PLUS MODE ENABLED | FORCE PCIE GEN1 | IGNORE DEBUG STRAPS DEFAULT | Required setting for intergrated CLOCk MODE DEFAULT | EC DISABLED DEFAULT | INTERNAL CLOCK GEN DISABLED | SPI ROM DEFAULT |

# FCH DEBUG STRAPS

Provided test point access for lab use.
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

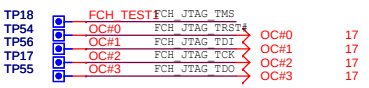

| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|
| PULL HIGH | USE PCI PLL DEFAULT | RESERVED | Normal REFCLK Termination DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL DOWN | BYPASS PCI PLL | RESERVED | Inverted REFCLK Termination | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |

FCH XOR CHAIN TEST




FCH PCIE EEPROM STRAPS


FCH ICE DEBUG /JTAG TEST PINS

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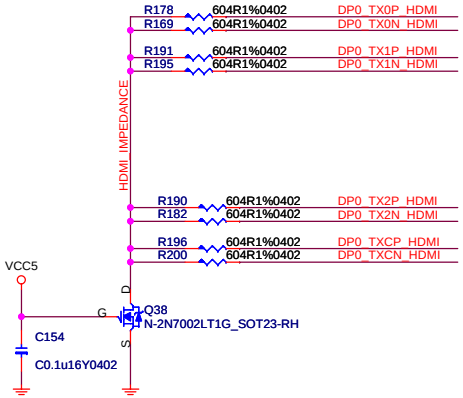
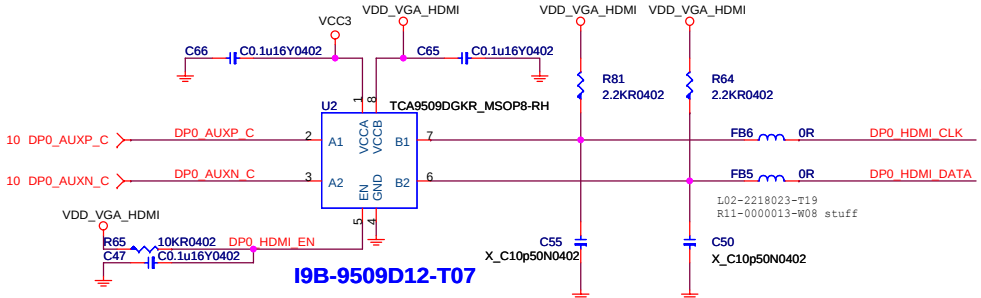
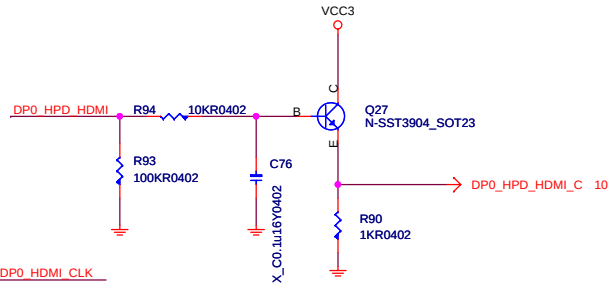
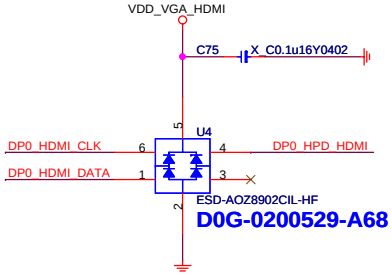
| | | | |
|---|---|---|---|
| Title | MS-7800 | | |
| Size: Custom | Document Number: HUDSON STRAPS | | Rev: 10 |
| Date: Friday, April 06, 2012 | | Sheet 20 of 36 | |

# HDMI CONN,



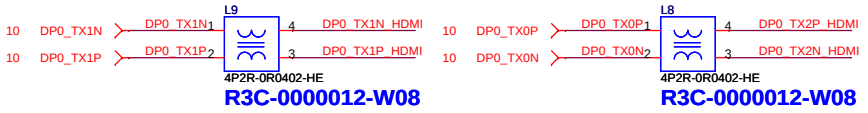



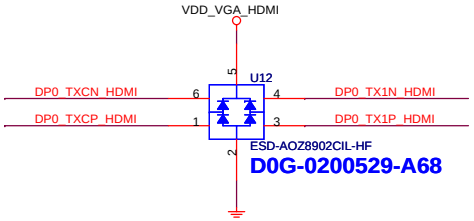



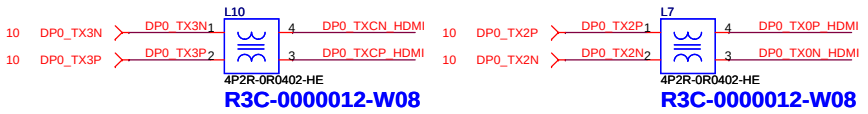

DP CONOFIGERATION TABLE

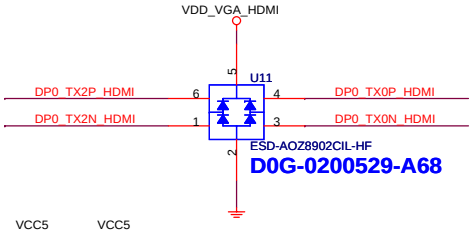
| INTERFACE | DP PORT OF FM1 | | | |
|---|---|---|---|---|
| DP | 3 | 2 | 1 | 0 |
| HDMI | Channel | Clock | Ch 0 | Ch 1 | Ch 2 |

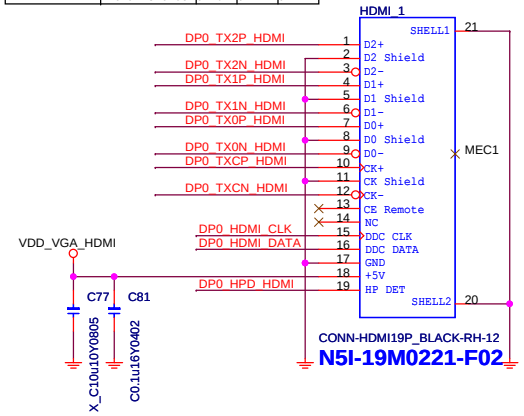


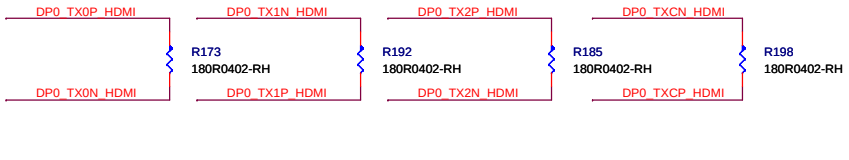



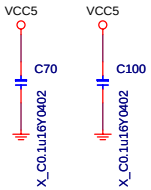

CMC料號 :L12-9008104-I05
0 ohm料號 : R3C-0000012-W08

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| | | |
|---|---|---|
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# VGA CONNECTOR

R932-R934 CLOSE TO CRT CONNECTOR, THE TRACE IMPEDANCE BETWEEN NB AND 150OHM RESISTOR SHOULD BE 37OHM+/-15%, THE TRACE IMPEDANCE BETWEEN THE 2 150OHM

RESISTOR SHOULD BE 50 OHM +/-15%,

THE IMPEDANCE BETWEEN THE 2ND RESISTOR TO THE CONNECTOR SHOULD BE 75OHM+/-15%

Layout:PLACE L 90 DEGREE FROM EACH OTHER

PLACE ESD PROTECTION DIODES
1. CLOSE TO CONNECTOR PINS
2. DIRECTLY ON SIGNAL TRACES
3. +5V & GND TRACE TO DIODE SHOULDBE LESS THAN 100MILS AND 20MILS WIDE
4. THE ESD DIODE SHOULD BE THE FIRST DEVICE FROM CONNECTOR

mach@The value of L,C refer to demo board,maybe adjusted for test

CLOSE TO VGA Connector

18 HUDSON_VGA_R — L6 10n300mA — VGA_R — L5 10n300mA
R157 150R1%0402 | C131 C3.3p50N0402 | C134 C3.3p50N0402 | C130 C10p50N0402

18 HUDSON_VGA_G — L4 10n300mA — VGA_G — L3 10n300mA
R146 150R1%0402 | C126 C3.3p50N0402 | C128 C3.3p50N0402 | C125 C10p50N0402

18 HUDSON_VGA_B — L2 10n300mA — VGA_B — L1 10n300mA
R145 150R1%0402 | C122 C3.3p50N0402 | C123 C3.3p50N0402 | C121 C10p50N0402

VDD_VGA_HDMI

C127 X_C0.1u16X0402
U10 ESD-AOZ8902CIL-HF
BLUE_CONN — RED_CONN — GREEN_CONN
D0G-0200529-A68

C92 X_C0.1u16X0402
U8 ESD-AOZ8902CIL-HF
VSYNC_CONN — DDCDATA_CONN
HSYNC_CONN — DDCCLK_CONN
D0G-0200529-A68

DDCCLK_5V R133 33R0402 — DDCCLK_CONN
VSYNC_5V R108 27R0402 — VSYNC_CONN
HSYNC_5V R134 27R0402 — HSYNC_CONN
DDCDATA_5V R107 33R0402 — DDCDATA_CONN

C113 X_C100p50N0402 | C103 X_C18P50N0402 | C110 X_C18P50N0402 | C93 X_C100p50N0402

VGA_1
DSUB-VGAF_BLUE-RH-18
N51-15F0801-K06

BLUE_CONN
GREEN_CONN
RED_CONN

VCC5 — C105 C0.1u16Y0402
18 HUDSON_VGA_HSYNC — U9 AHCT1G126GV_SOT23-5-RH
T34-1G12609-N47
R141 X_2.2KR0402 — HSYNC_5V — C114 X_C10p50N0402

VCC5 — C91 C0.1u16Y0402
18 HUDSON_VGA_VSYNC — U7 AHCT1G126GV_SOT23-5-RH
T34-1G12609-N47
R109 X_2.2KR0402 — VSYNC_5V — C104 X_C10p50N0402

18 HUDSON_VGA_SDAT — R105 — DDCDATA_5V
18 HUDSON_VGA_SCLK — R140 — DDCCLK_5V
R104 4.7KR0402 | R132 4.7KR0402

+12V — R92 4.7KR0402
VCC5 — Q26 N-2N7002LT1G_SOT23-RH
F-MICROSMD110F-RH
D08-0100210-R02
C85 X_C10u10Y0805 | C86 C0.1u16Y0402

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| | | |
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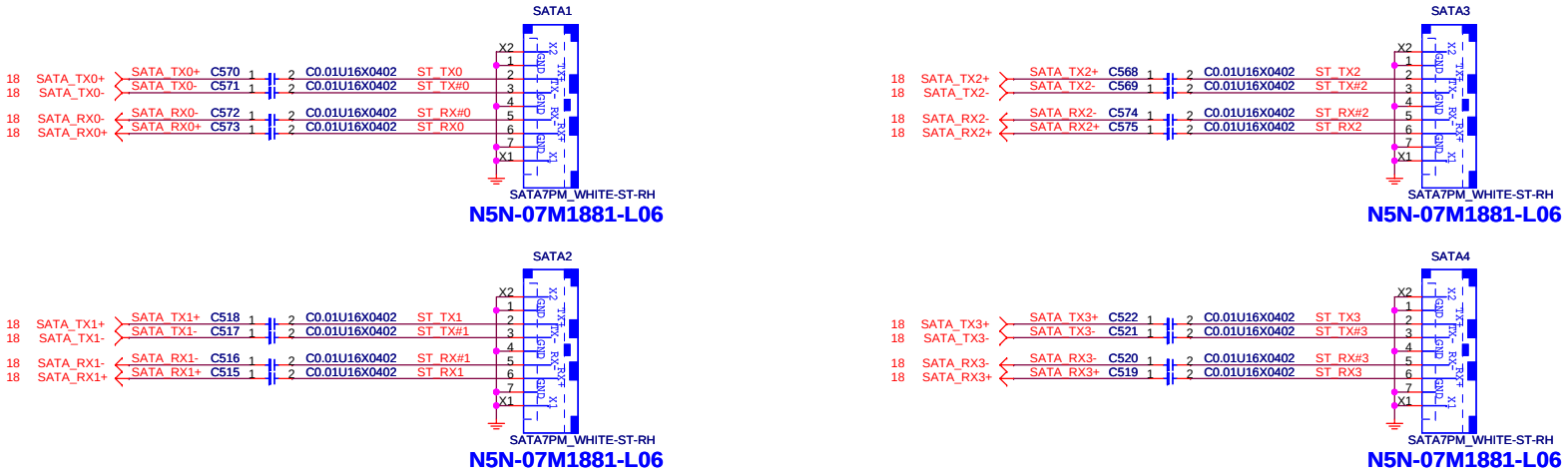
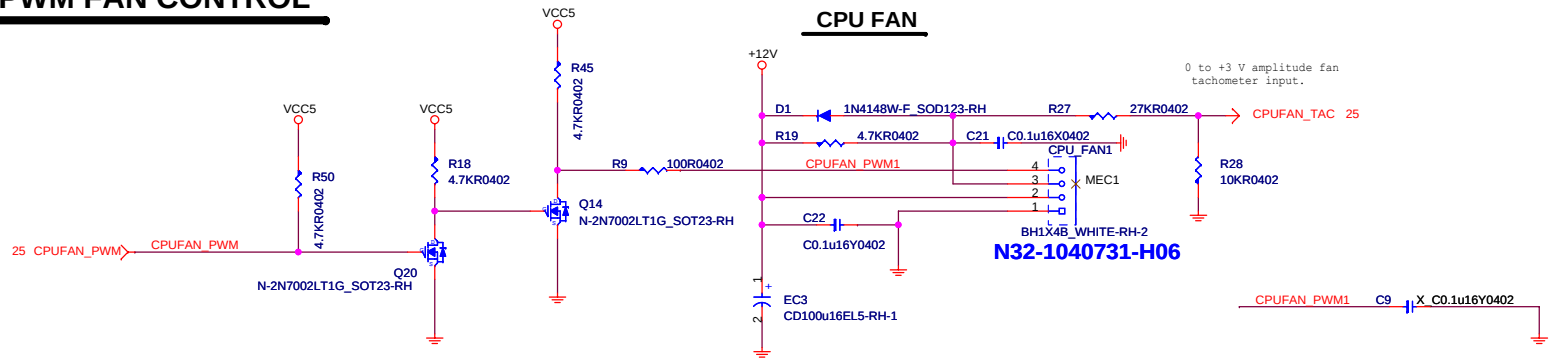
# iSATA CONNECTOR

Multiple eSATA function

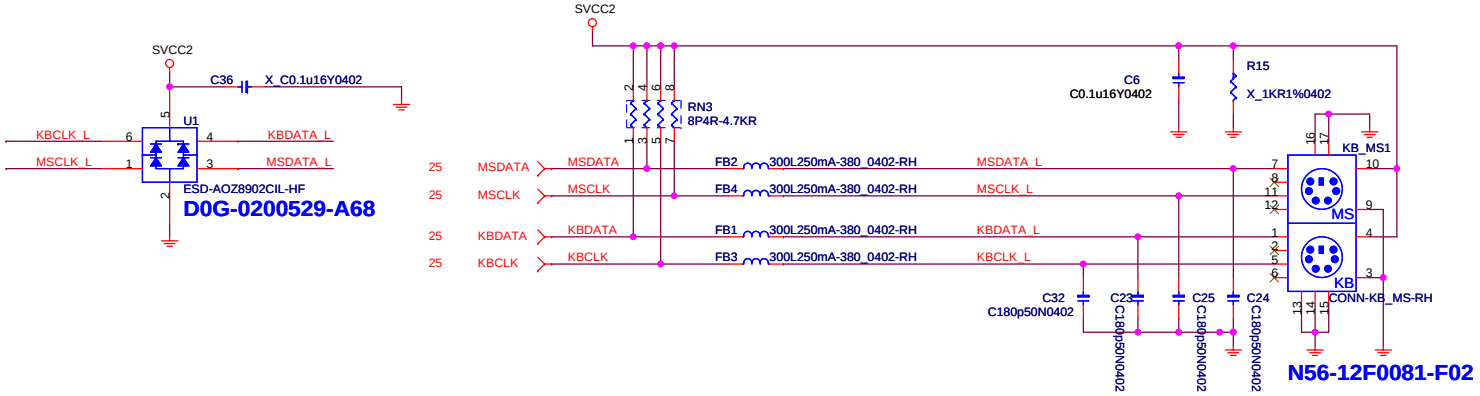
Layout:For Gen 3.0,trace length within 2.5''




# PWM FAN CONTROL




# PS2 KEYBOARD & MOUSE CONNECTOR

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| | | |
|---|---|---|
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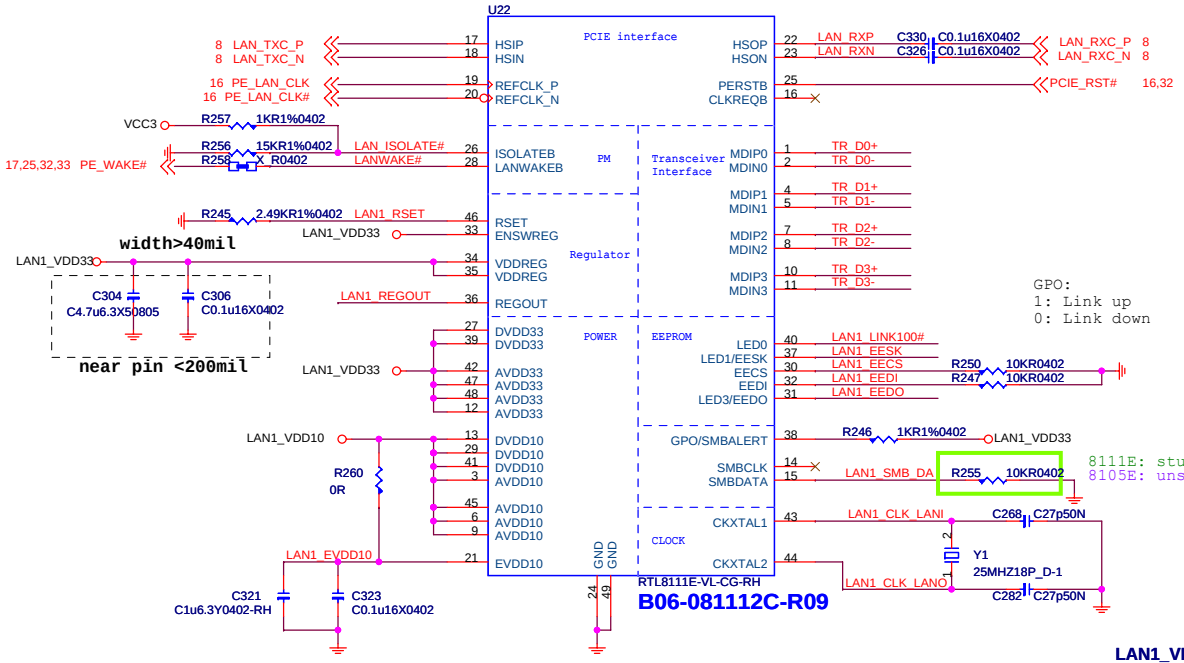
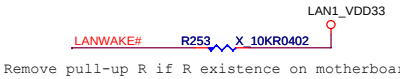
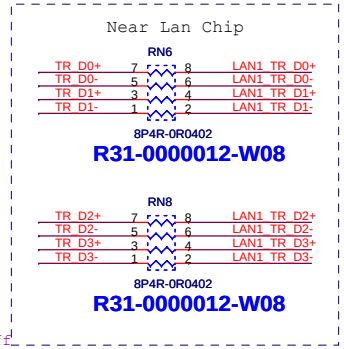
# RTL8105E 10/100M LAN RTL8111E Giga LAN

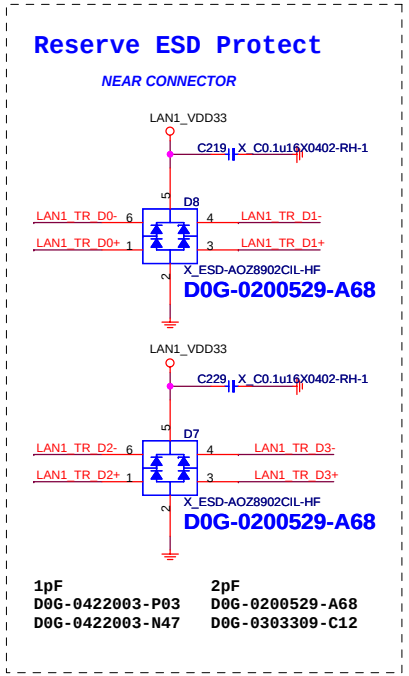


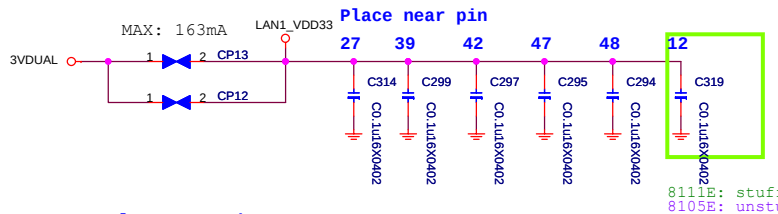



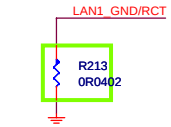

Remove pull-up R if R existence on motherboard (or SB has internal pull-up R).

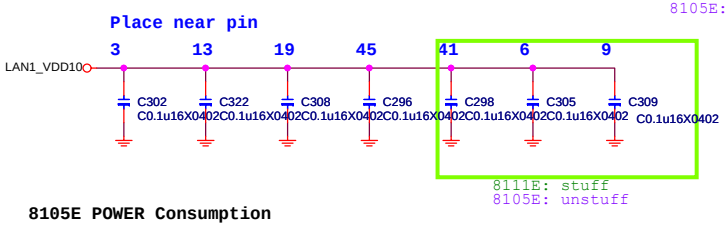
GPO:
1: Link up
0: Link down

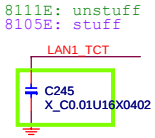


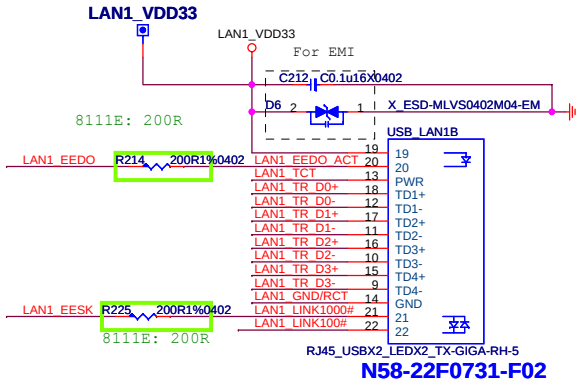



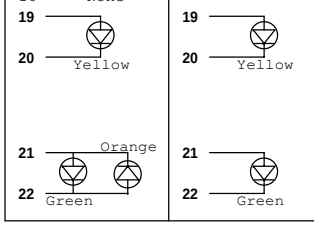

## LAN Connector




R14, R15, R17請依據所使用的LAN connector上的LED亮度去調整阻值

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

| Giga-Lan | | 10/100-Lan | |
|---|---|---|---|
| N58-22F0731-F02<br>N58-22F0731-S42<br>N58-22F0731-I60 | | N58-22F0061-S42<br>N58-22F0061-F02 | |
| Link | Yellow | Link | Yellow |
| Active | Blinking | Active | Blinking |
| 1000 | Orange | 100 | Green |
| 100 | Green | 10 | None |
| 10 | None | | |

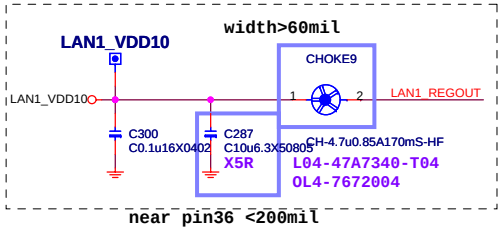


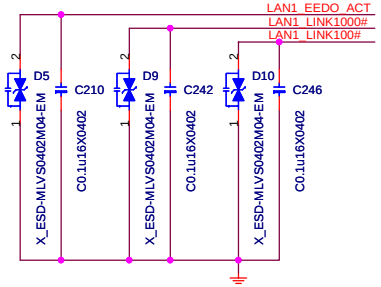

### 8105E POWER Consumption

| | 3.3V | mW |
|---|---|---|
| 10 M Idle/TxRx | 14/75 | 46/248 |
| 100 M Idle/TxRx | 43/66 | 142/218 |
| S0 ALDPS | 3.2 | 11 |

### 8111E POWER Consumption

| | 3.3V | mW |
|---|---|---|
| 10 M Idle/TxRx | 12/66 | 40/218 |
| 100 M Idle/TxRx | 31/44 | 102/145 |
| Giga Idle/TxRx | 135/163 | 452/538 |
| ALDPS | 4 | 13 |




| | |
|---|---|
| MSI MICRO-START INT'L CO.,LTD. | |
| Title | MS-7800 |
| Size: Custom | Document Number: LAN - RTL8111E |
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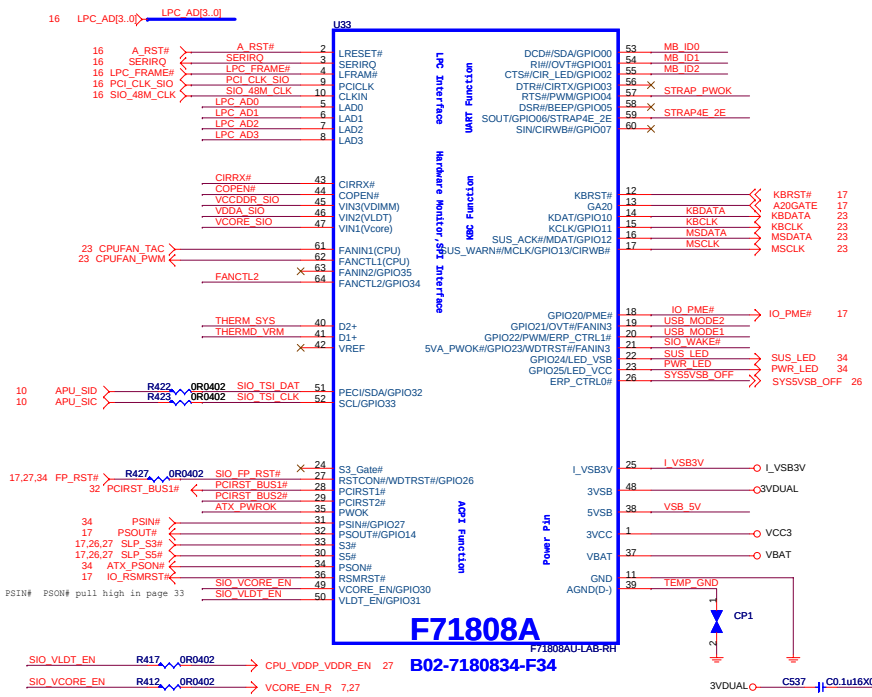
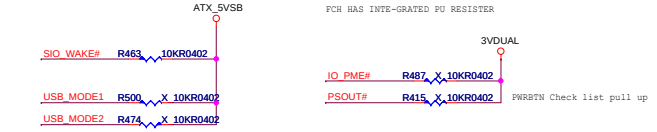
# Super I/O

## LPC SUPER I/O F71808A

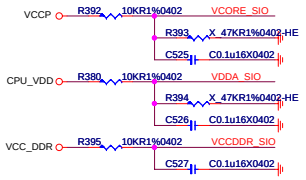



## F71808A EUP Function

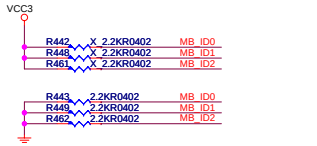



## VOLTAGE SENSING(H/W Monitor)

The best voltage input level is about 1V.

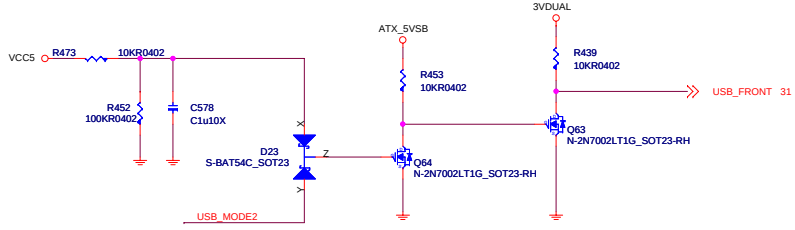


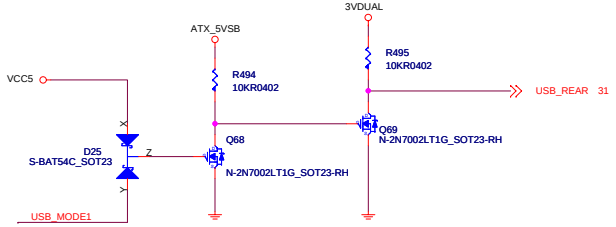

## M/B ID




| 2 | 1 | 0 | ROM TYPE |
|---|---|---|---|
| 0 | 0 | 0 | defaul |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

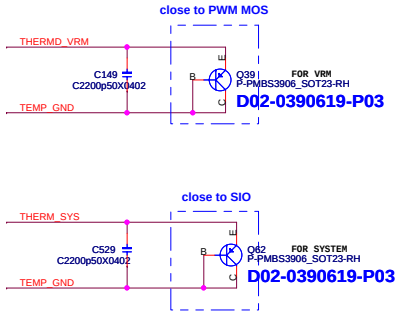
## USB_MODE CONTROL



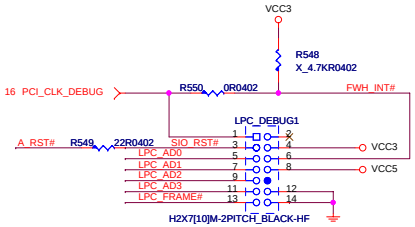




## Temperature Sensing

Diode / Resistor SENSING CIRCUIT

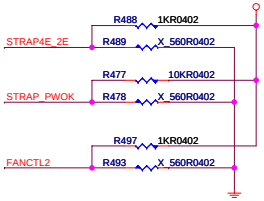



## LPC Debug Port




## LPC I/O STRAPPING RESISTOR

POWER-ON TRIP




| PIN | Function | NET Name | HI | LO |
|---|---|---|---|---|
| 59 | Config 4E/2E | SOUTA | 4E | 2E |
| 57 | STRAP_PWOK | STRAP_PWOK | PWOK (pin 35) for AMD | PWOK (pin 35) for Intel |

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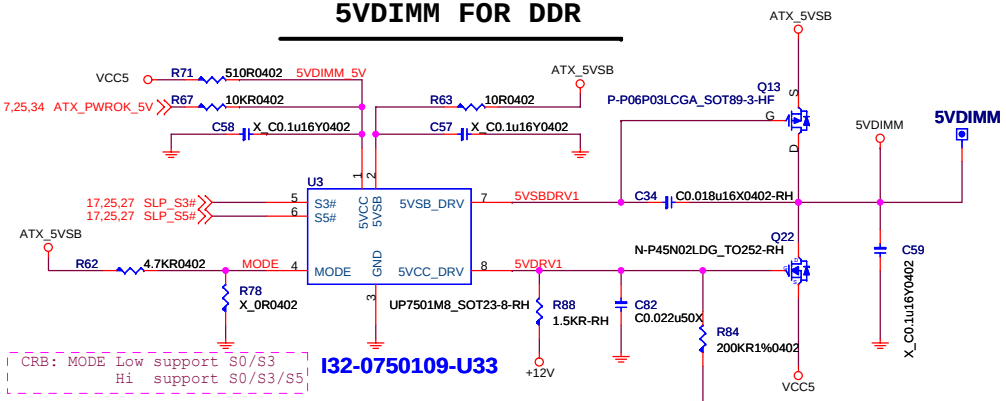
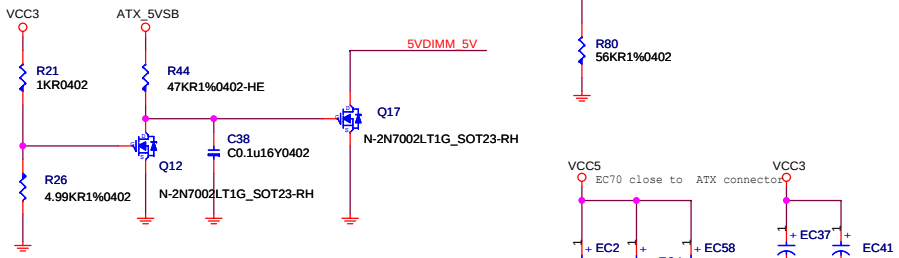
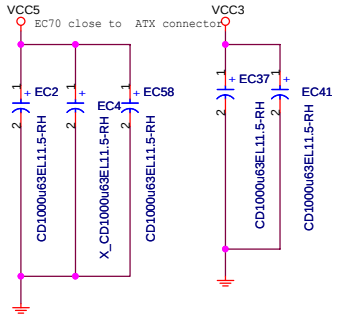
# 5VDIMM FOR DDR

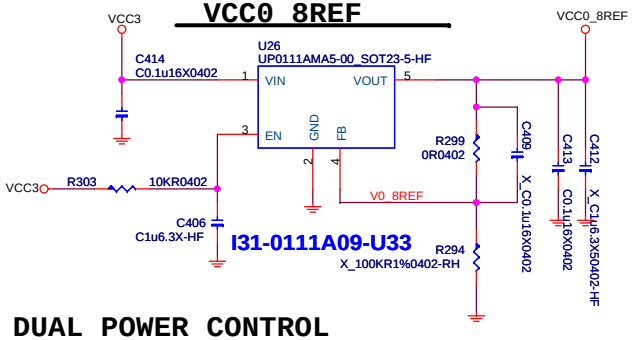



## For special PSU sequence

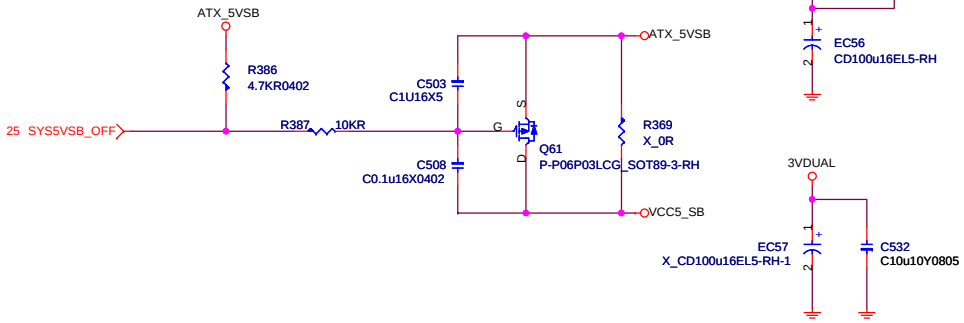



## VCC0 8REF




## DUAL POWER CONTROL

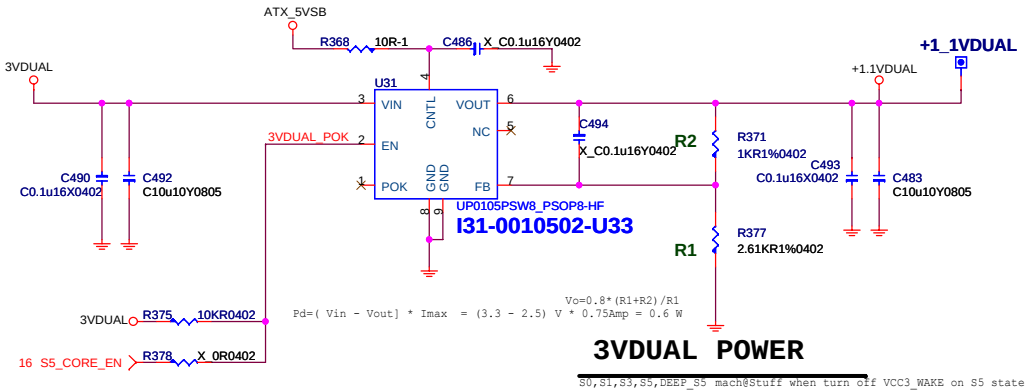



# 1.1VDUAL POWER

1.V@1.23A

measurement:700mA

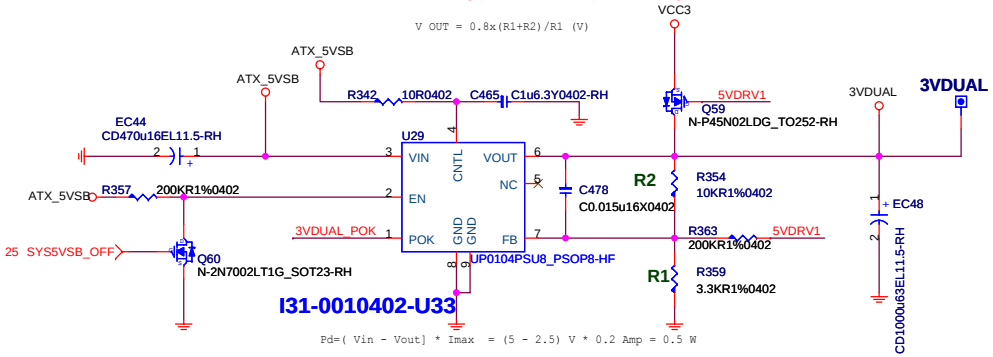
S0,S1,S3




# 3VDUAL POWER

S0,S1,S3,S5,DEEP_S5 mach@Stuff when turn off VCC3_WAKE on S5 state

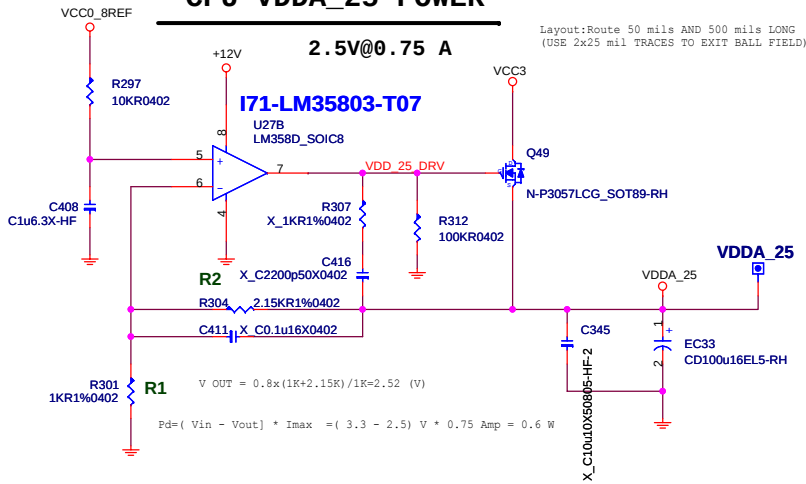
Vout : 0.8 [( R593+R599))/R599 ] = 3.3 Volt
Vout : 0.8 [( 10K+3.3K ) /3.3K ] = 3.22 Volt




# CPU VDDA_25 POWER

2.5V@0.75 A

Layout:Route 50 mils AND 500 mils LONG
(USE 2x25 mil TRACES TO EXIT BALL FIELD)




MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

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|---|---|---|
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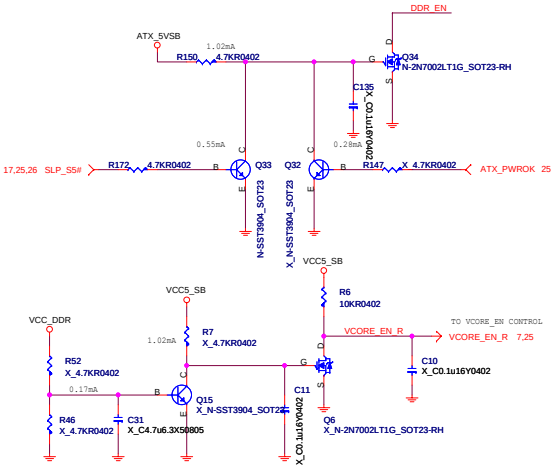
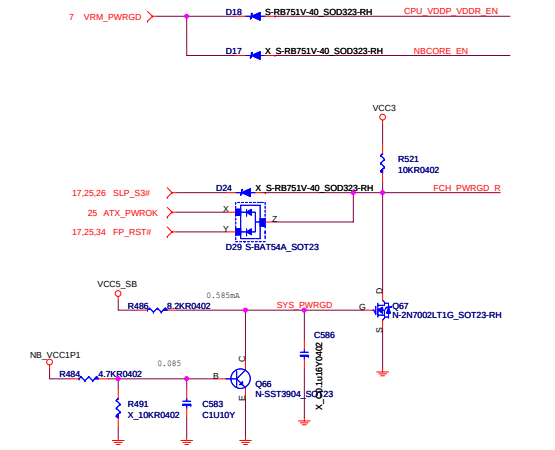
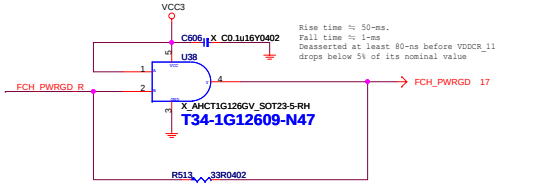
# POWER EN & PWRGD LOGIC CIRCUIT

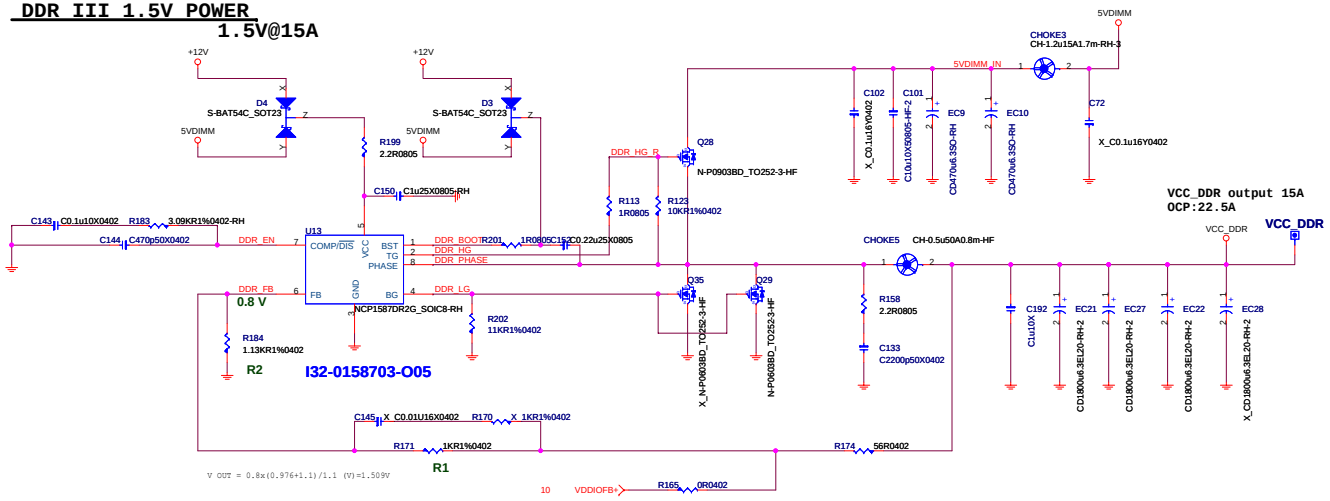


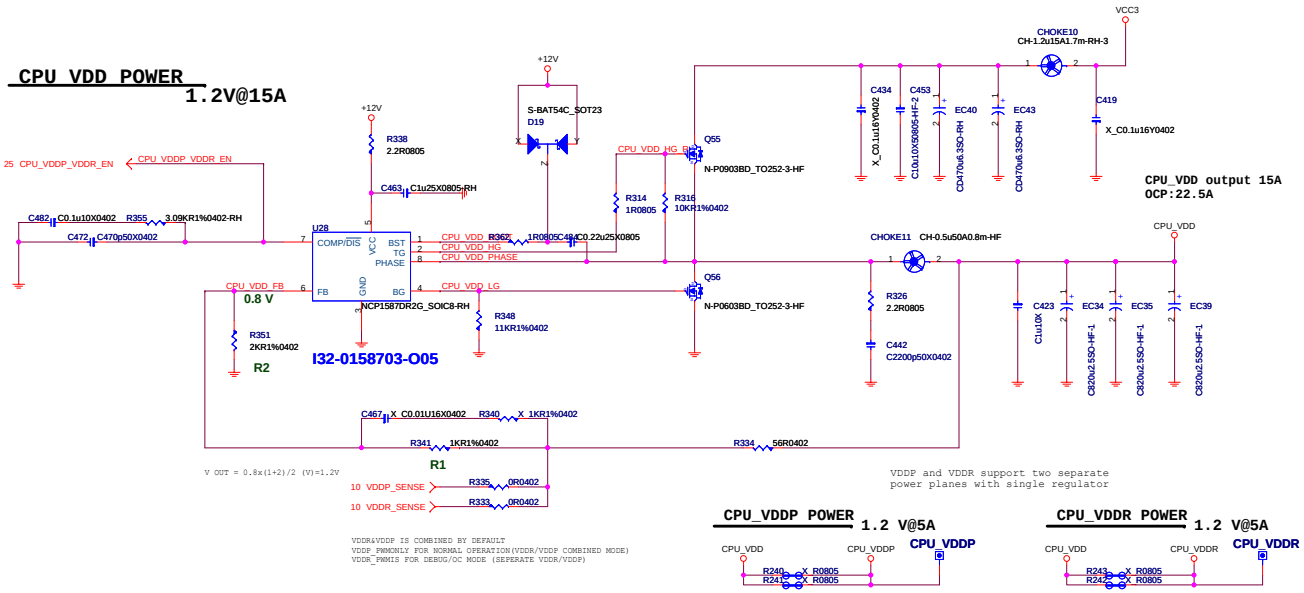

# DDR III 1.5V POWER

## 1.5V@15A




# CPU_VDD POWER

## 1.2V@15A




## CPU_VDDP POWER 1.2 V@5A

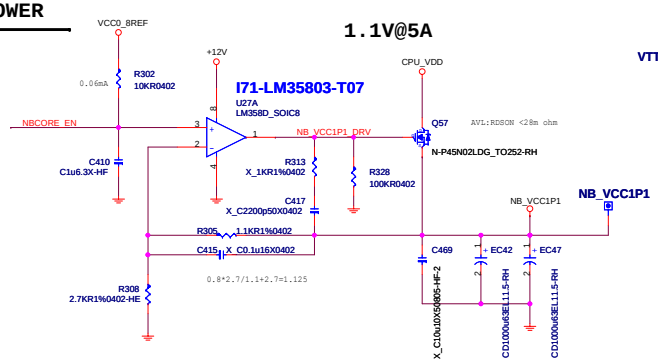



## CPU_VDDR POWER 1.2 V@5A



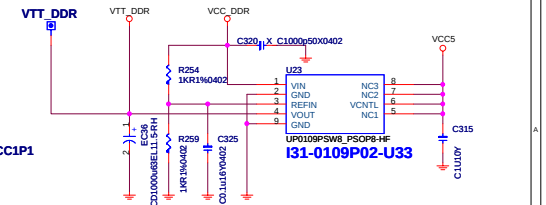

# NB_VCC1P1 POWER

## 1.1V@5A




# VTT_DDR POWER

## 0.75V@2A




MSI Link for the Future MICRO-START INT'L CO.,LTD.

| | | |
|---|---|---|
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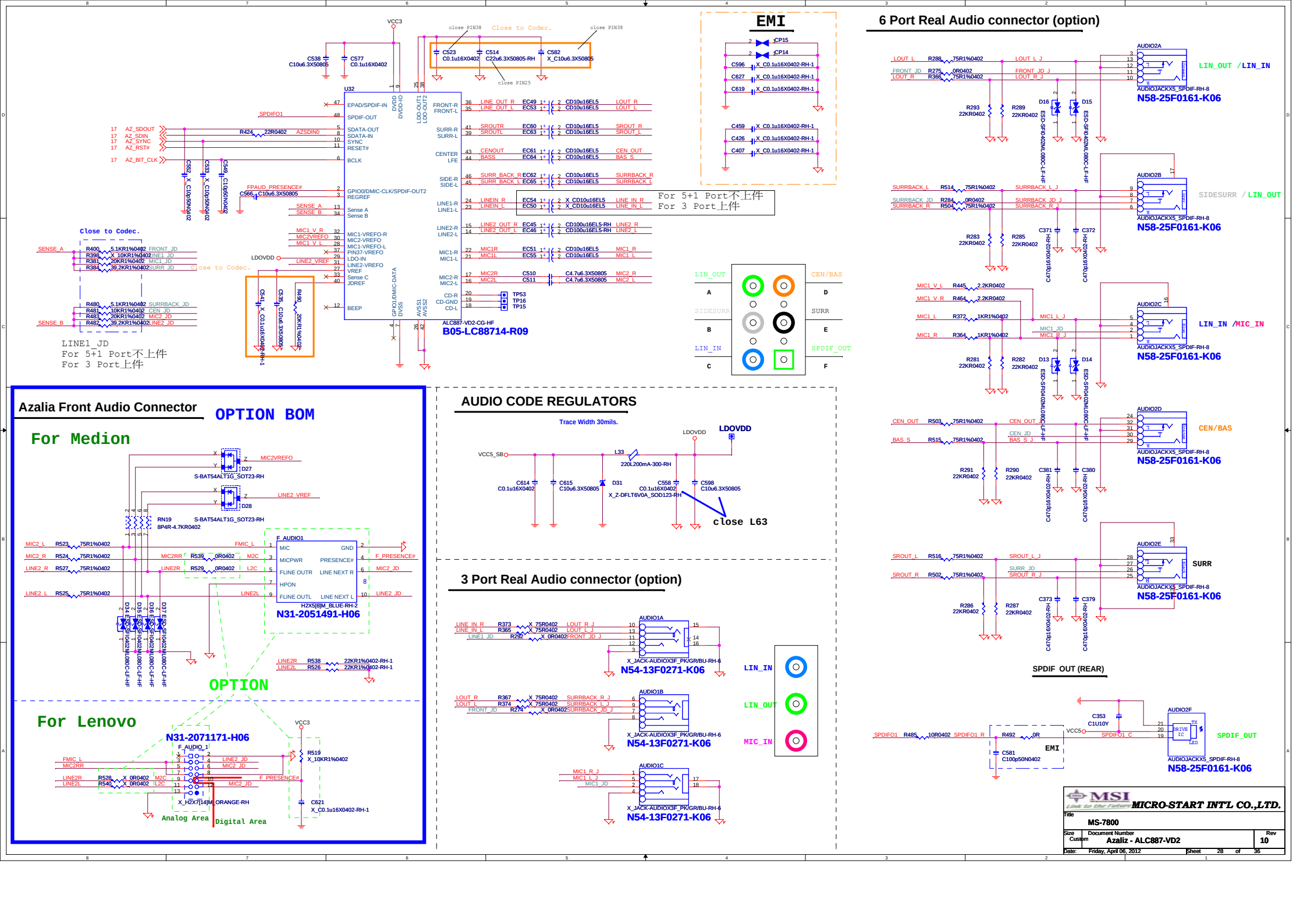
EMI
6 Port Real Audio connector (option)
Close to Codec.
U32
ALC887-VD2-CG-HF
B05-LC88714-R09
For 5+1 Port不上件
For 3 Port上件
LINE1_JD
For 5+1 Port不上件
For 3 Port上件
Azalia Front Audio Connector
OPTION BOM
For Medion
S-BAT54ALT1G_SOT23-RH
8P4R-4.7KR0402
H2X5[8]M_BLUE-RH-2
N31-2051491-H06
OPTION
For Lenovo
N31-2071171-H06
X_HZX7[14]M_ORANGE-RH
Analog Area
Digital Area
AUDIO CODE REGULATORS
Trace Width 30mils.
LDOVDD
220L200mA-300-RH
close L63
3 Port Real Audio connector (option)
X_JACK-AUDIOX3F_PK/GR/BU-RH-6
N54-13F0271-K06
LIN_OUT
SIDESURR
LIN_IN
CEN/BAS
SURR
SPDIF_OUT
AUDIOJACKX5_SPDIF-RH-8
N58-25F0161-K06
LIN_OUT /LIN_IN
SIDESURR /LIN_OUT
LIN_IN /MIC_IN
CEN/BAS
SURR
SPDIF_OUT (REAR)
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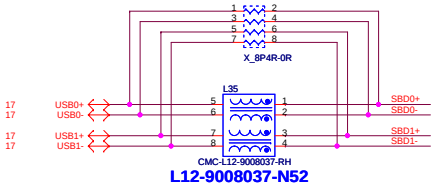
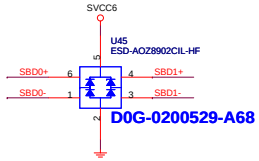
## FRONT USB PIN HEADER

R31-0000013-W08

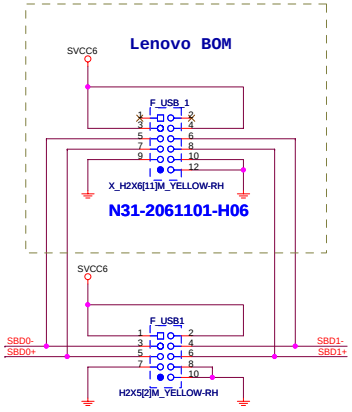



L12-9008037-N52




D0G-0200529-A68

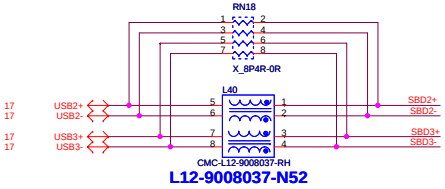
## BOM Option



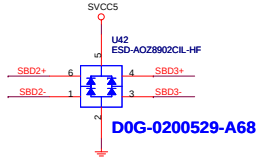

N31-2061101-H06

N31-2051321-H06

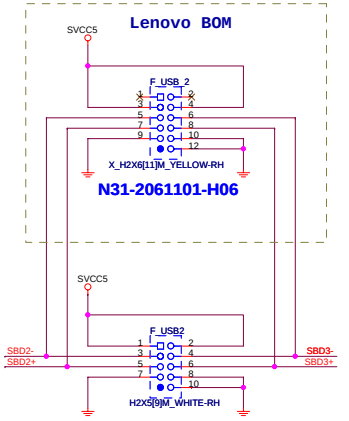
R31-0000013-W08




L12-9008037-N52




D0G-0200529-A68

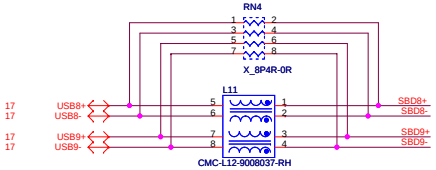



N31-2061101-H06

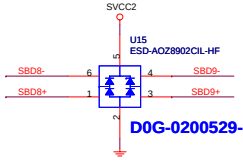
N31-2051461-H06

## REAR PANEL USB CONNECTOR

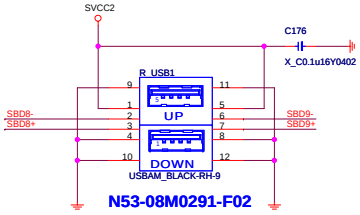
*NEAR USB CONNECTOR*



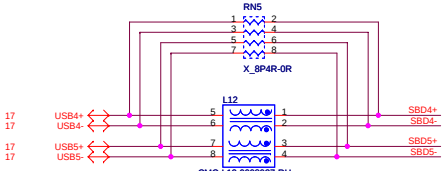

L12-9008037-N52



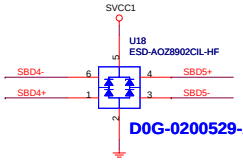

D0G-0200529-A68



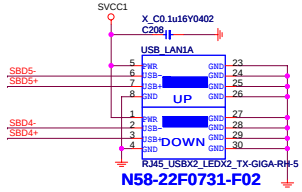

N53-08M0291-F02




L12-9008037-N52




D0G-0200529-A68




N58-22F0731-F02

USB 2.0 trace length
REAR side within 18'';
FRONT side within 6''

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| | | |
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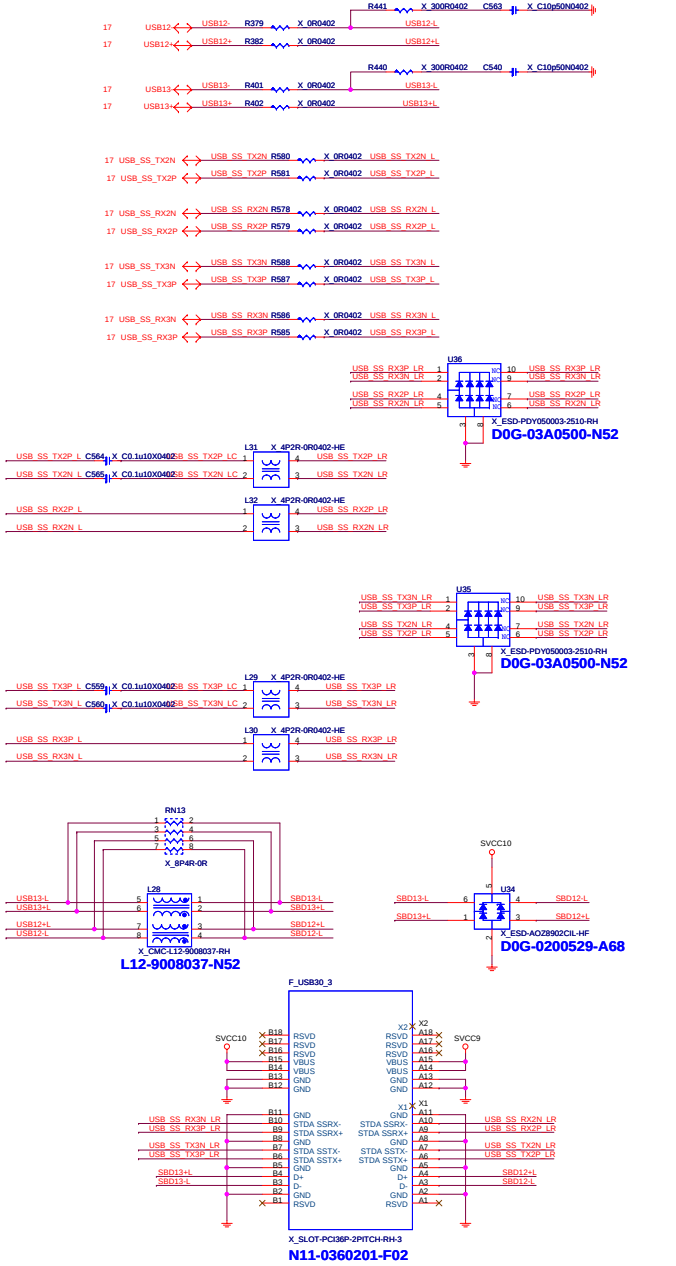
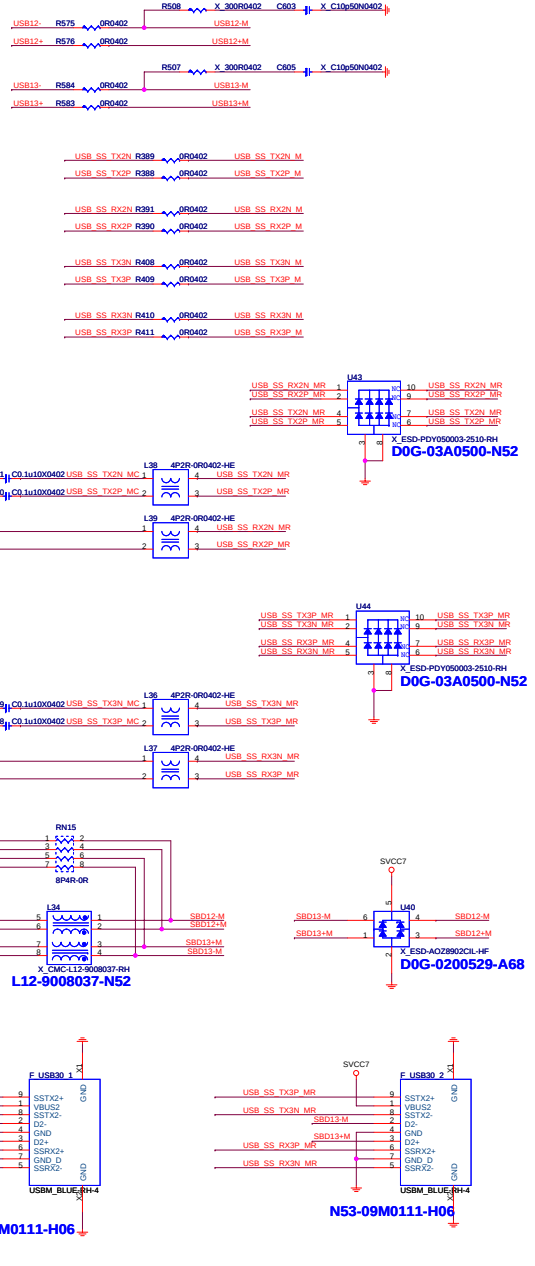
# Option BOM

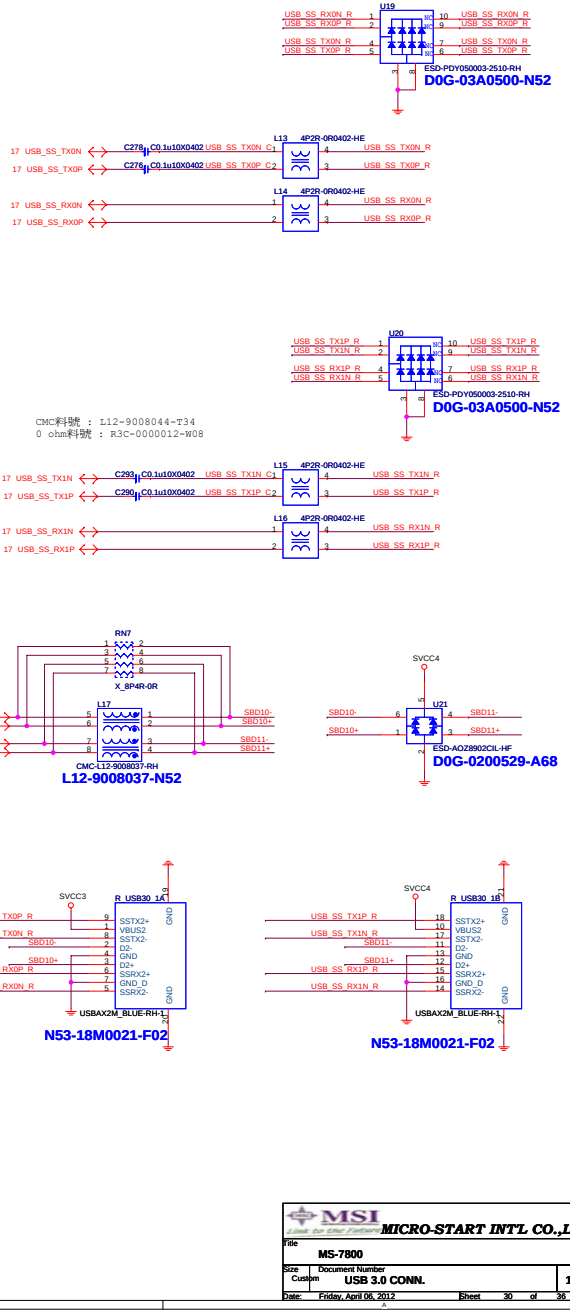
## For Lenovo front USB3.0




## For Medion front USB3.0




USB 3.0 trace length
Rear connector within 8''




| | | | |
|---|---|---|---|
| MSI | MICRO-START INT'L CO.,LTD. | | |
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| Size | Document Number | | Rev |
| Custom | USB 3.0 CONN. | | 10 |
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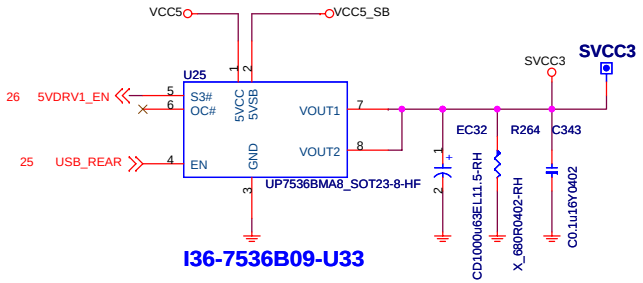
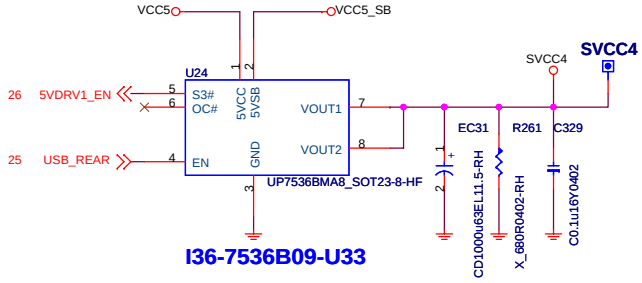
## Rear USB30 Power SVCC3 SVCC4



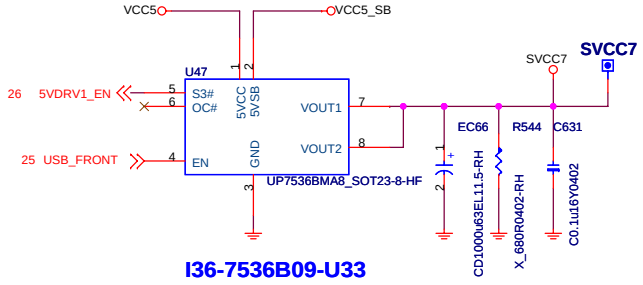

I36-7536B09-U33



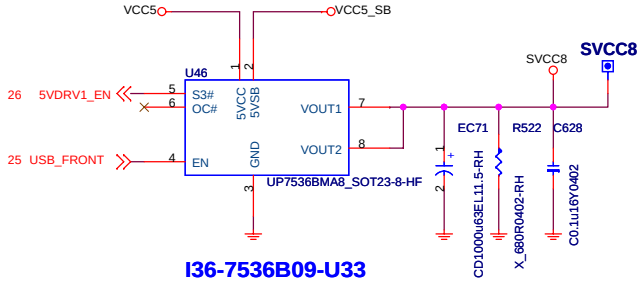

I36-7536B09-U33

# Option BOM

## Front USB30 Power SVCC7 SVCC8(Medion)

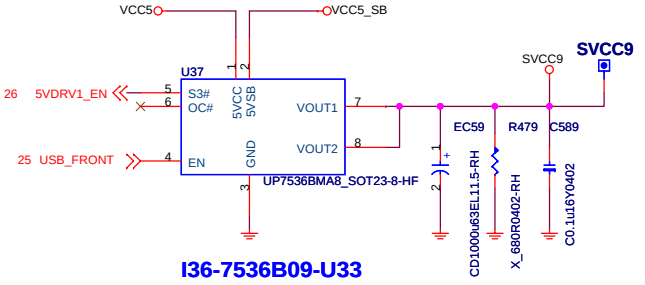



I36-7536B09-U33

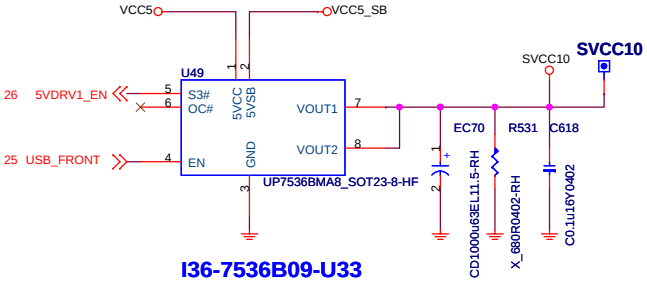



I36-7536B09-U33

## Front USB30 Power SVCC7 SVCC8(Lenovo)




I36-7536B09-U33

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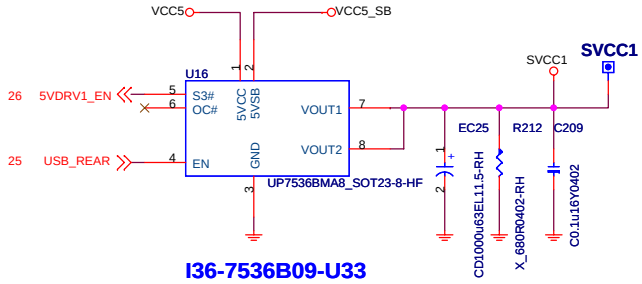
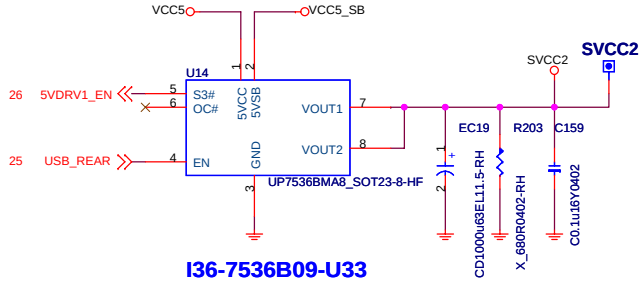
## Rear USB20 Power SVCC1 SVCC2

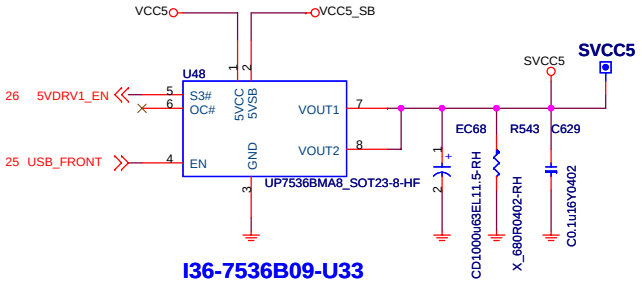



I36-7536B09-U33

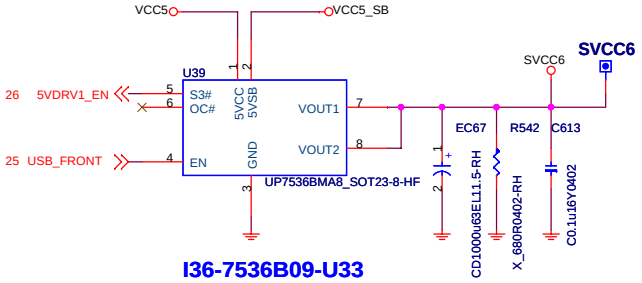



I36-7536B09-U33

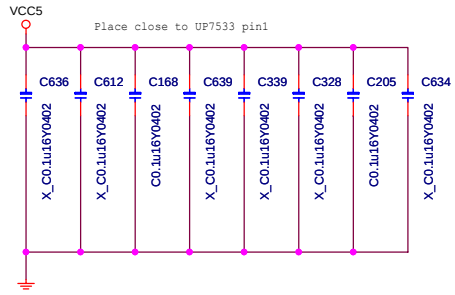
## Front USB20 Power SVCC5 SVCC6

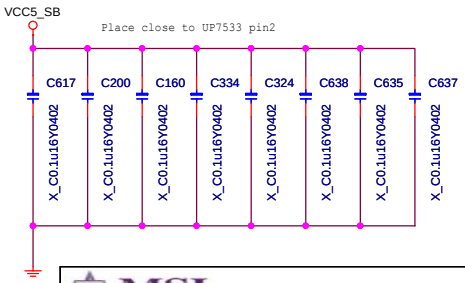



I36-7536B09-U33




I36-7536B09-U33

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| | | |
|---|---|---|
| Title | USB POWER/DISCHARGE | |
| Size: Custom | Document Number: FUSION | Rev: 10 |
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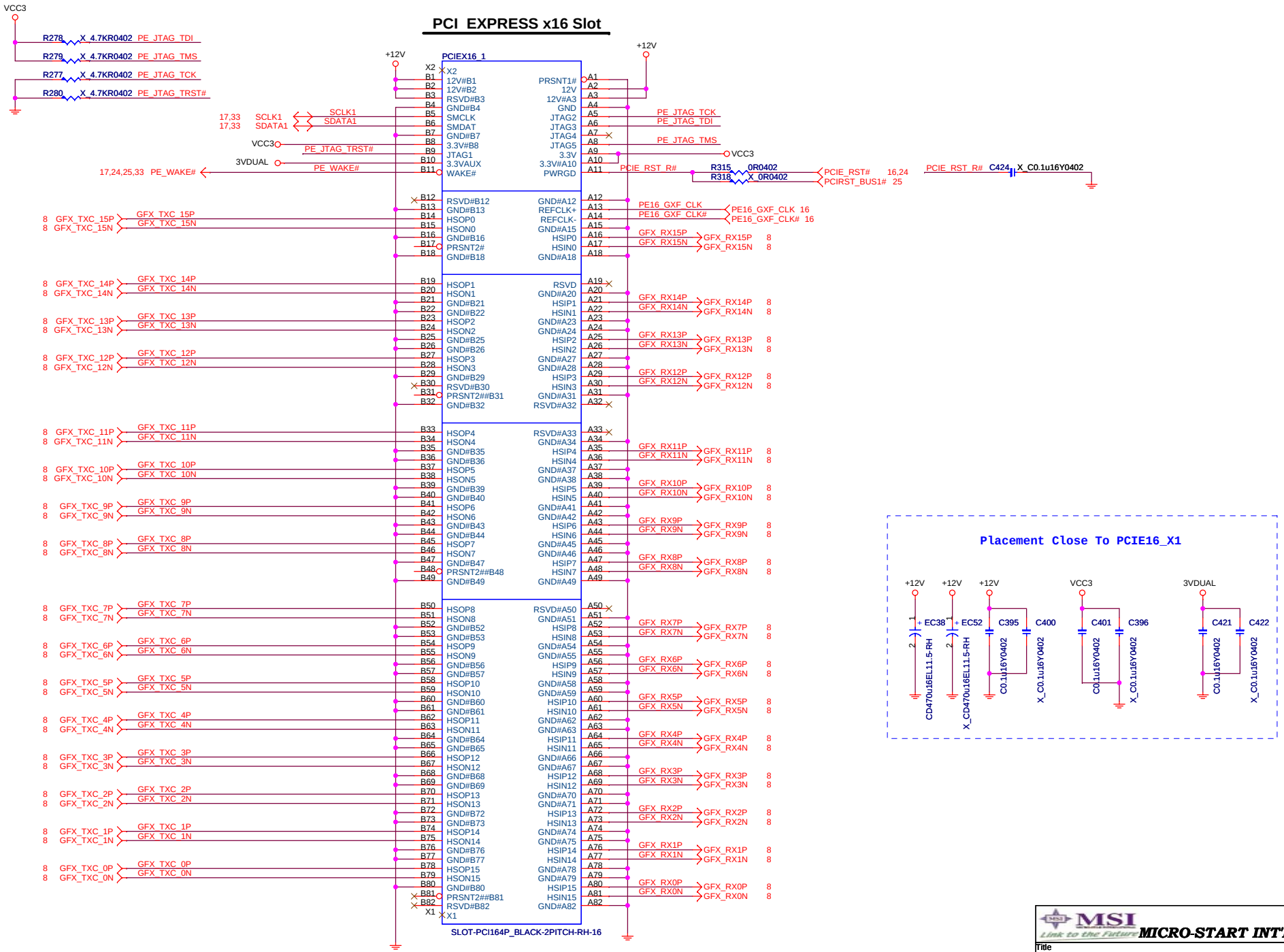
# PCI Express Slot x16




N11-1640551-K06

MICRO-START INT'L CO.,LTD.

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|---|---|---|
| Title | MS-7800 | |
| Size: Custom | Document Number: PCIE X16 SLOT | Rev: 10 |
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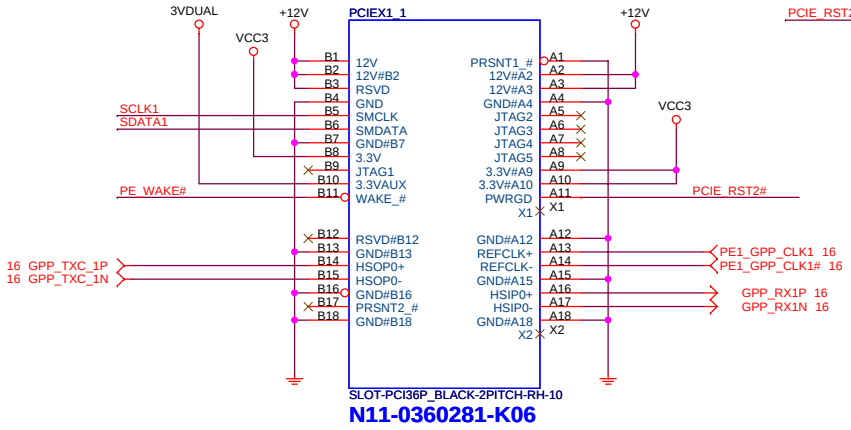
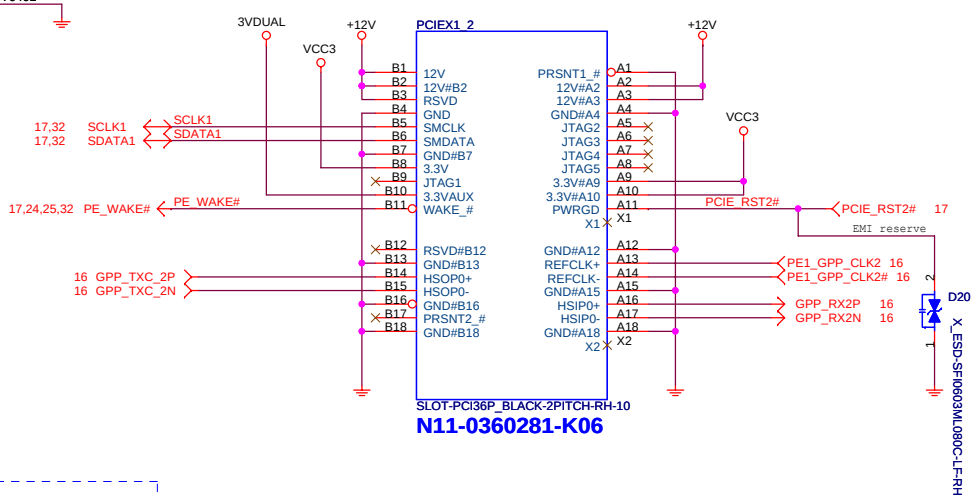
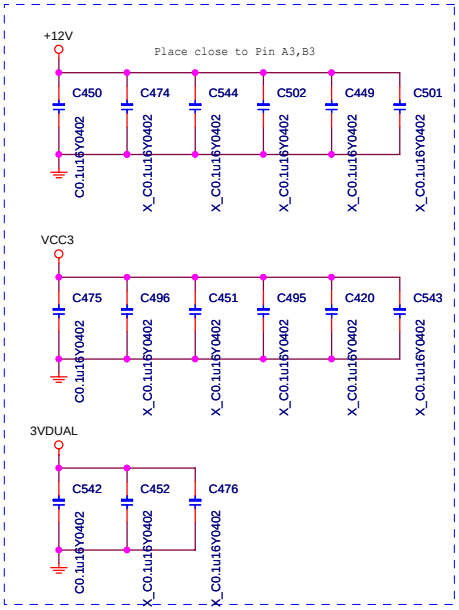
## PCI EXPRESS X1 Slot-2




PCIE_RST2# C477 X_C0.1u16Y0402

## PCI EXPRESS X1 Slot-3

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Title: PCIE X1 SLOTs

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|---|---|---|
| Custom | FUSION | 10 |

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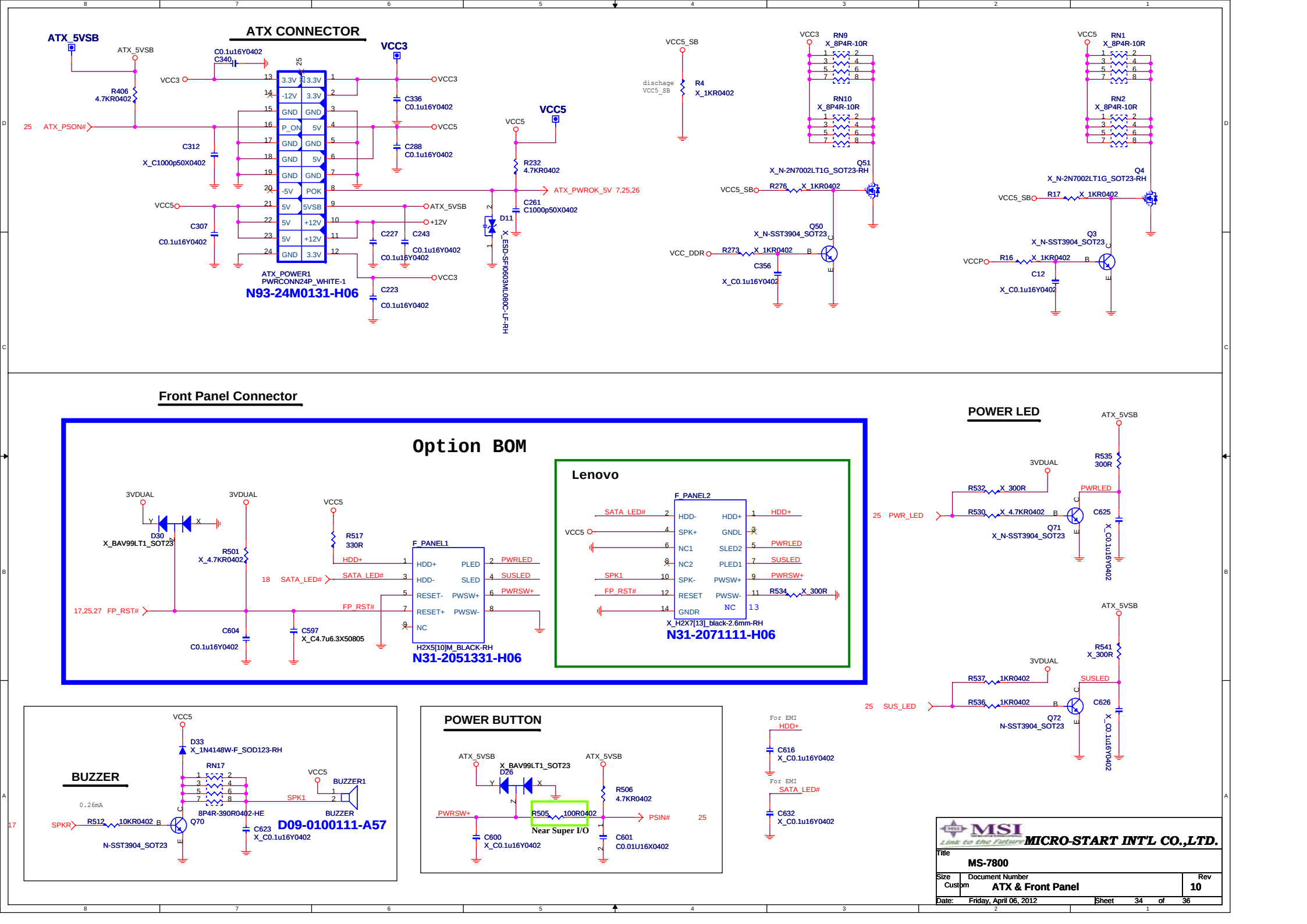
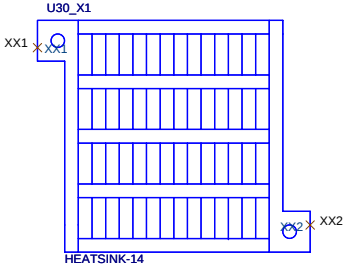

ATX_5VSB
ATX CONNECTOR
VCC3
VCC5
ATX_PSON#
ATX_PWROK_5V 7,25,26
ATX_POWER1
PWRCONN24P_WHITE-1
N93-24M0131-H06
Front Panel Connector
Option BOM
F_PANEL1
H2X5[10]M_BLACK-RH
N31-2051331-H06
Lenovo
F_PANEL2
X_H2X7[13]_black-2.6mm-RH
N31-2071111-H06
POWER LED
PWR_LED
SUS_LED
BUZZER
D09-0100111-A57
POWER BUTTON
Near Super I/O
PSIN#
MICRO-START INT'L CO.,LTD.
MS-7800
ATX & Front Panel
Friday, April 06, 2012

## HEAT SINK

U30_X1




E31-0404831-K08

Label

HDMI Logo

HDMI Royalty

Y01-RHDMI03-000

Label1

HDMI Logo

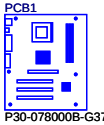
HDMI Sticker

G51-M1SPX33-Q13

## MANUAL PART

AVL:
D06-0100161-F52
D06-0100101-K26

BAT1_X1
BAT-BCR2032P-RH

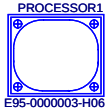


PCB1

P30-078000B-G37

P30-0780010-G37

## CPU RM



PROCESSOR1

E95-0000003-H06

E95-0000003-H06

Rubber1 Rubber2

PCB PCB

rubber1/2 rubber1/2

## Pangkor

U902

HUDSON D2

X_AMD-218-0755064-A13-RH

U909

ALC662

X_ALC662-VC1-GR-C1-RH

U912

75R

X_75R0402

U913

0R

X_0R0402

## L10

BARCODE1 BARCODE2 BIOS_LABEL

PCB PCB PCB

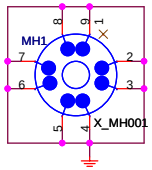
外部條碼 質保貼紙 AMI BIOS

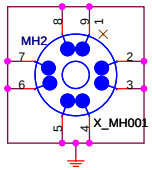
LAN
Symbol ValueMSIP/N
RTL8111E-VB-GR-RHB06-081110C-R09金製程
RTL8111E-VL-CG-RHB06-081112C-R09銅製程

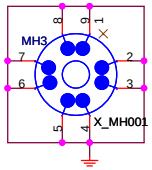
CODEC
ALC887-VD-GR-RHB05-LC88704-R09金製程
ALC887-VD2-CG-HFB05-LC88714-R09銅製程

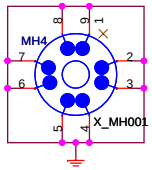
ALC892-GR-RHB05-LC89204-R09金製程
ALC892-CG-RHB05-LC89214-R09 銅製程

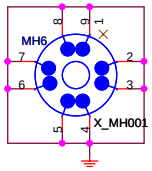
ALC662-VC1-GR-C1-RHB09-LC66234-R09金製程
ALC662-CG-RHB05-LC66204-R09銅製程

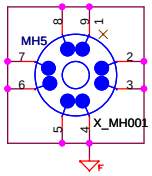


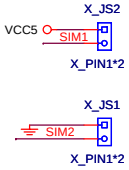




## Optics Orientation Holes

FM3 FM2
X_FM120 X_FM120
FM6 FM5
X_FM120 X_FM120
FM8 FM1
X_FM120 X_FM120
FM4 FM7
X_FM120 X_FM120

## Simulation

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## MS-7800-0A

1.Modify front MS-7748-1.1
2.change cpu from FM1 to FM2
3.Co-lay LENOVO connector and pin heater
4.Modify USB3.0 (from FCH)

## MS-7800-0B

1.Modify HDMI level shift from DDR 1.5V to VCC3
2.Modify DDR3 signal MA(B)_CLK_1/2 to MA(B)_CLK_0/3
3.Modify DDR3 signal MA(B)0_ODT, MA(B)0_CS to MA(B)1_ODT, MA(B)1_CS
4.Modify VGA connector(EMI suggestion) N51-15F0801-K06
5.Modify Power team suggestion
  R202 = 11k
  R171 = 1k
  R184 = 1.13k
  R348 = 11k
  R82 = 27k
  RT4 = 10k NTC
  R83= 27.4k
  R102 = 27k
  RT1 = 10k NTC
  R103 = 27.4k
  R116 = 221k
  EC14 = 470uF  C71-47102FE-P01

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