GA-970A-DS3P

Revision : 2.01

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Title: COVER SHEET

Size	Document Number	Rev
Custom	GA-970A-DS3P	2.01

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Model Name:GA-970A-DS3P

Version: 2.01

P-Code: U98094-0

Component value change history

Date	Change Item	Reason
2013.03.21	PVT 發行,增加ERP0.5W&修改VL805線路	01A
2013.03.21	9M970AS3P-00-10B	10B
	ALC 887 修改為加強版 移除CD1	
2014.06.23	9M970AS3P-00-10C	101C
	REMOVE SATA MLCC	
2014.08.13	9M970AS3P-00-20A	20A
	LAN 變更為8111G ,IO改為ITE8620 CX	
	FUSE 改為2PORT 1 FUSE	
	NON VCORE 加入NEC 2724替料	
	5VDUAL控制線路變更, FAN改為3941控制	
	AUDIO改為 Chemicon電容	
	REMOVE EC15,EC16,EC13,EC29,EC40,LAEC1, EC31,UEC10,EC11,EC45,EC34	
2014.10.02	REMOVE EC16	20B
2014.10.20	REMOVE SWITCHN NEC 2724 共5顆	20C
2014.10.24	REMOVE ALL NEC 2724 共6顆	20D
2014.10.31	R2794改為20K FIX 部分DDR不開機問題	20E

Circuit or PCB layout change for next version

Date	Change Item	Reason
2013.03.21	9M970AS3P-00-10A	PCB Ver 1.0
2013.12.19	PVT	PCB Ver 1.0
2014.06.23	9M970AS3P-00-10C	PCB Ver 1.01
	REMOVE SATA MLCC	
2014.08.13	9M970AS3P-00-20A	PCB Ver 2.0
	LAN 變更為8111G ,IO改為ITE8620 CX	
	FUSE 改為2PORT 1 FUSE	
	5VDUAL控制線路變更, FAN改為3941控制	
	變更SATA_LED 線路, 變更 -MPD1 線路	
2014.10.02	9M970AS3P-00-20B	PCB Ver 2.01
	REMOVE EC16	

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Title: BOM & PCB HISTORY

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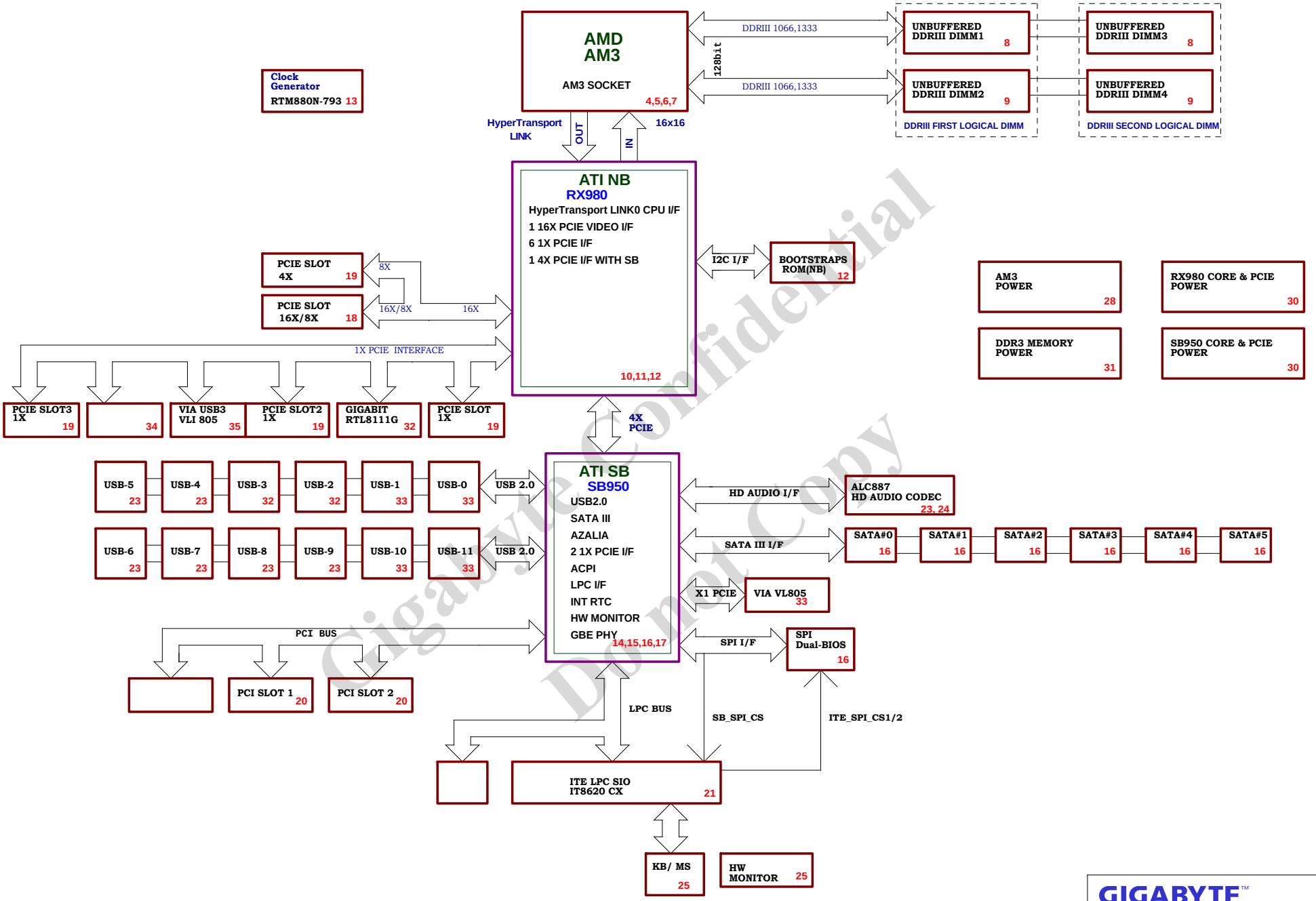
Date: Wednesday, November 19, 2014 | Sheet 2 of 33



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Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-970A-DS3P	2.01

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CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

L0_CADIN_L[0..15]
L0_CADIN_H[0..15]
L0_CADOUT_L[0..15]
L0_CADOUT_H[0..15]

M2CPUA
HYPERTRANSPORT

{10} L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 {10}
{10} L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 {10}
{10} L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 {10}
{10} L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 {10}
{10} L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 {10}
{10} L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 {10}
{10} L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 {10}
{10} L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 {10}
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-04R]

COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

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Title: CPU HYPER TRANSPORT

Size	Document Number	Rev
Custom	GA-970A-DS3P	2.01

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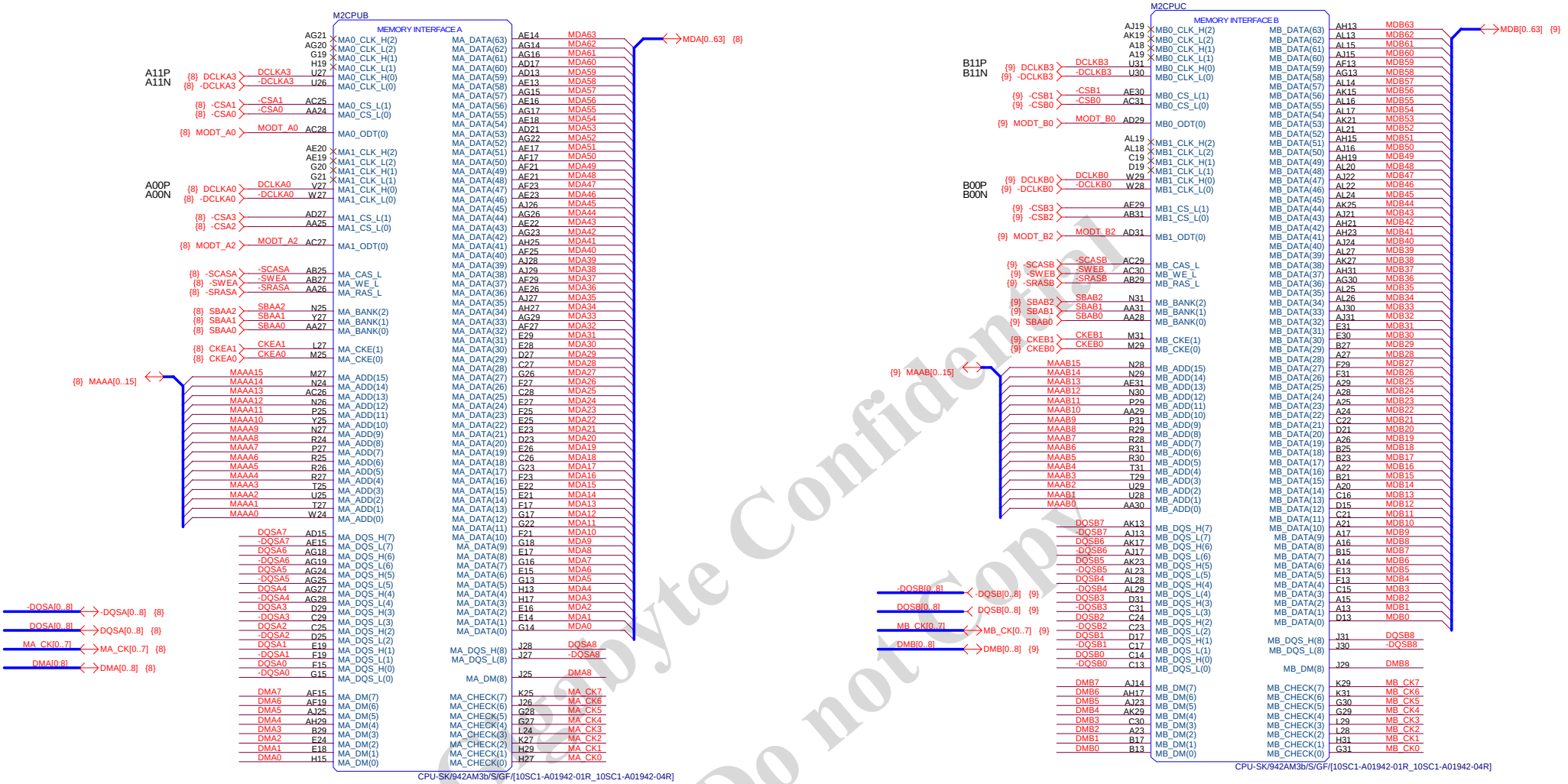

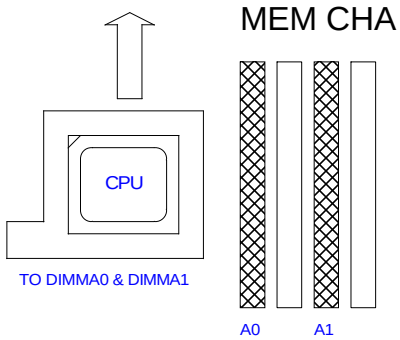

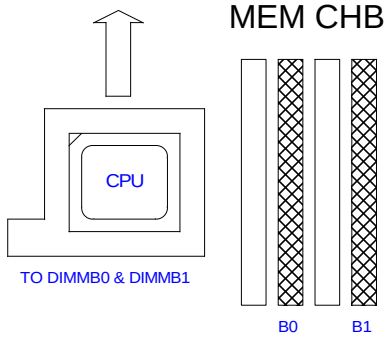

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Title	CPU DDRIII MEMORY	
Size: Custom	Document Number: GA-970A-DS3P	Rev: 2.01
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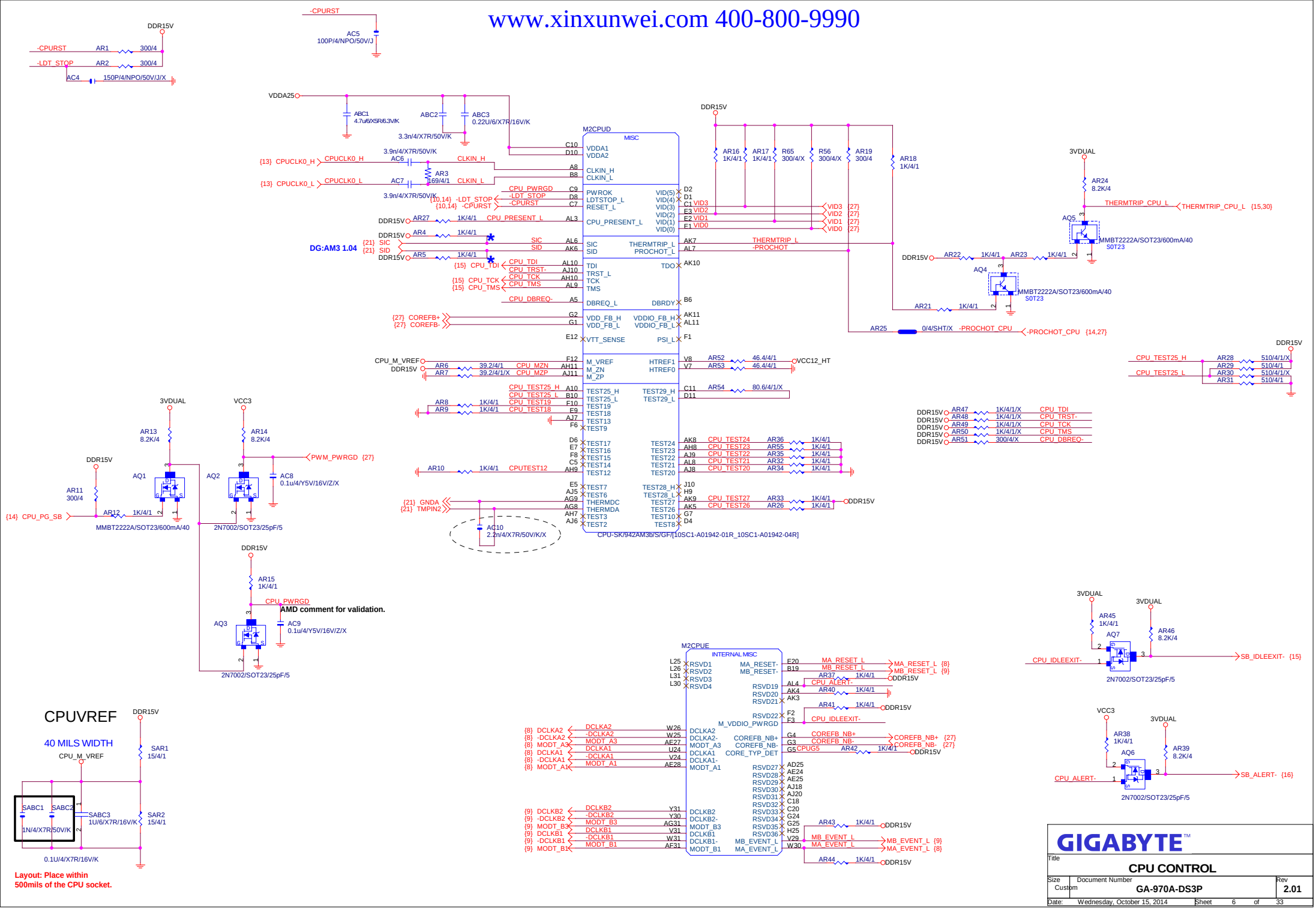

VLDT_RUN3 is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

M2CPUE
VDD1

AE9 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUG
VDD2

H22 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUH
VDD3

AM3 Only

M2CPUI
VDDIO

HT12B

BUTTOM SIDE

BUTTOM SIDE

AMD Validation

BUTTOM SIDE

AMD Validation

AMD Validation

1021 EMI

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Title	CPU POWER & GND		
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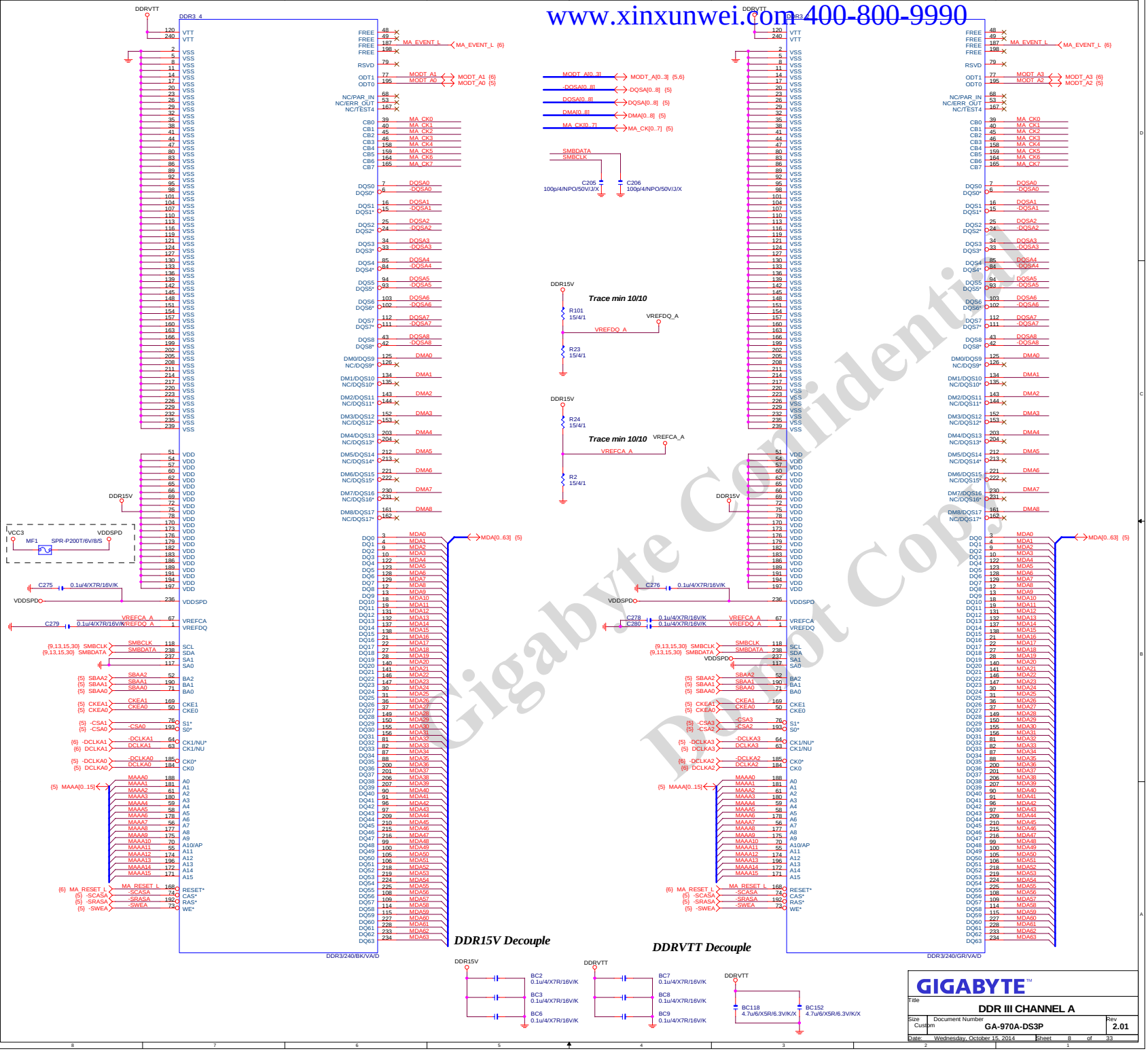

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Title	DDR III CHANNEL A	
Size: Custom	Document Number: GA-970A-DS3P	Rev: 2.01
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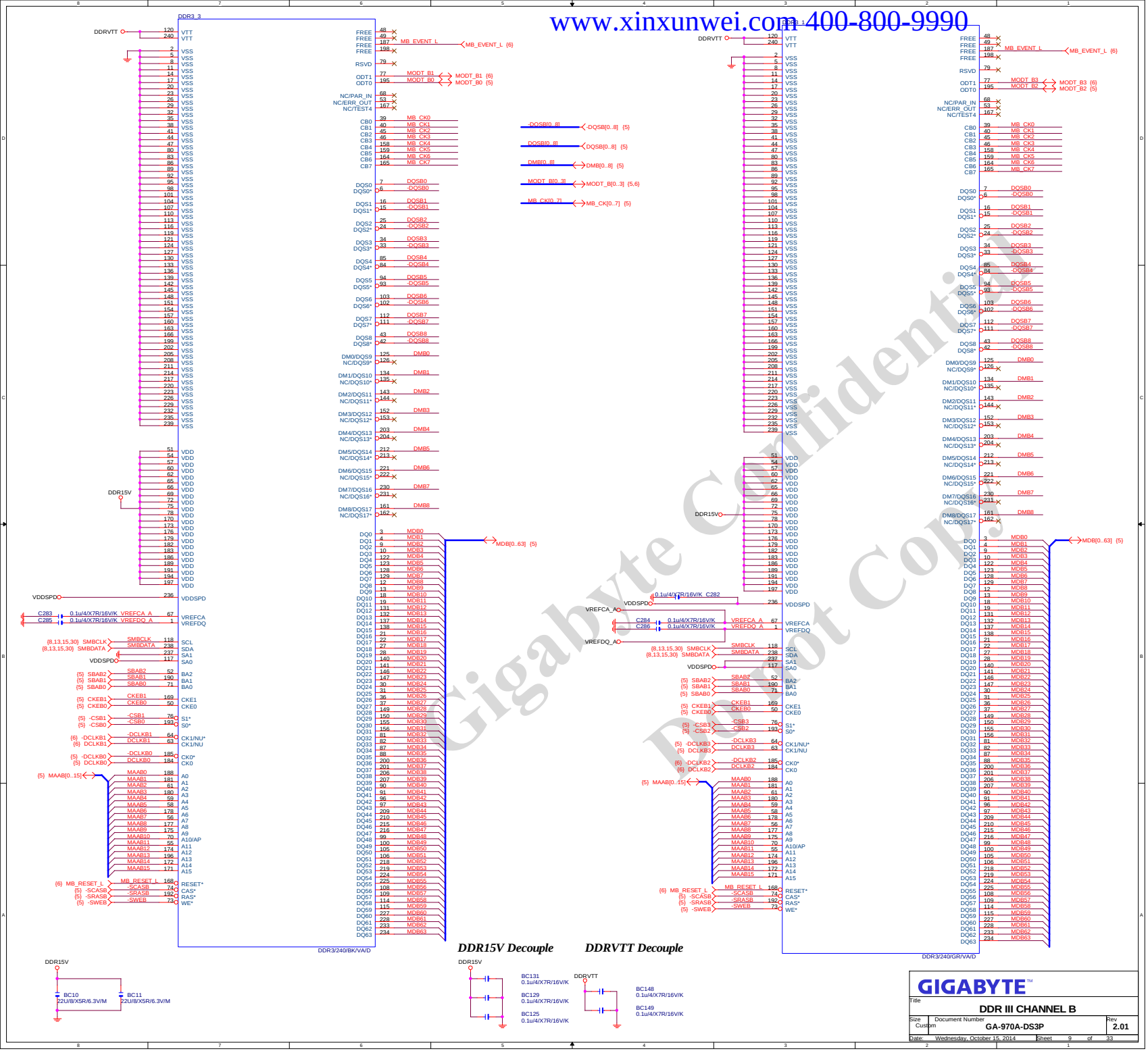

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Title: DDR III CHANNEL B

Size	Document Number	Rev
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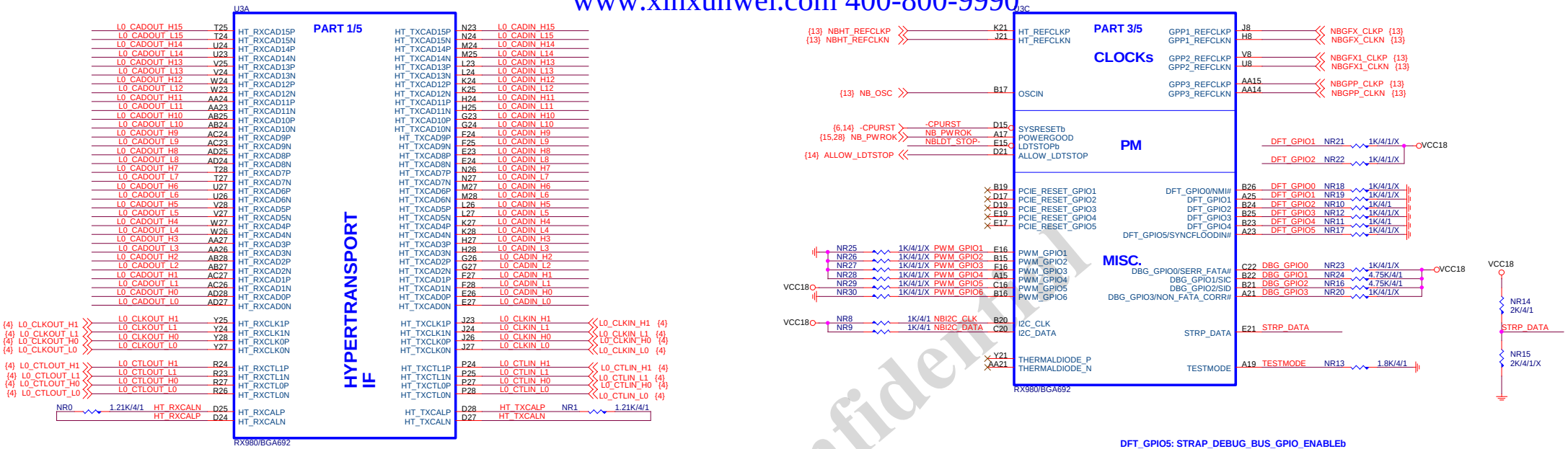

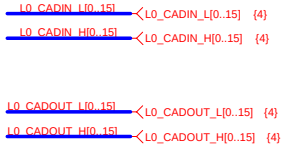

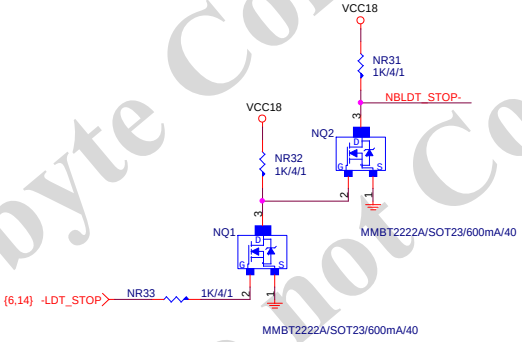

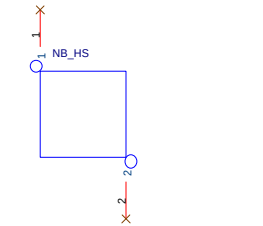

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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Title: RX980 HT-LINK I/F

Size	Document Number	Rev
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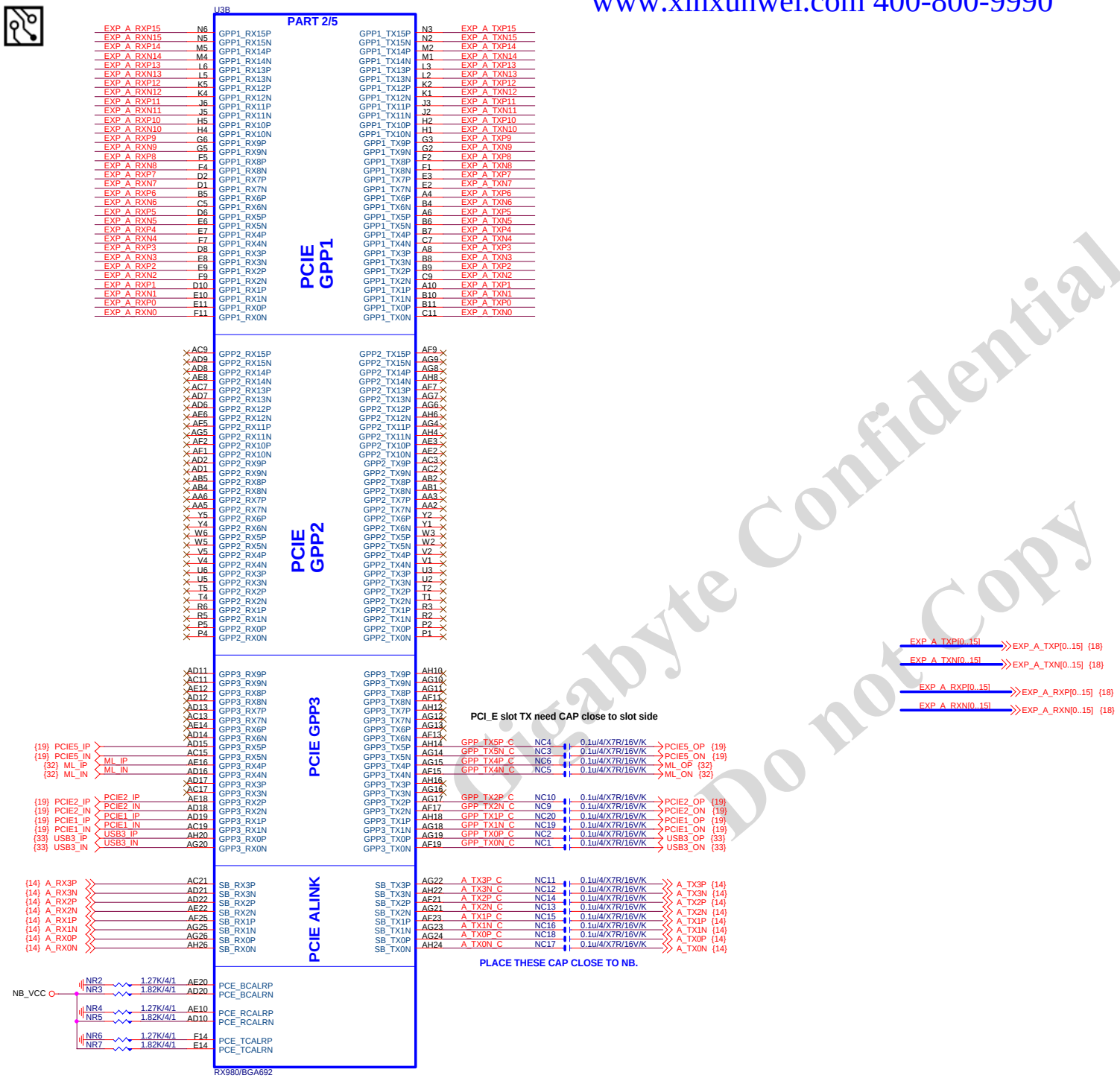

Title	RX980 PCIE I/F
Size	Custom
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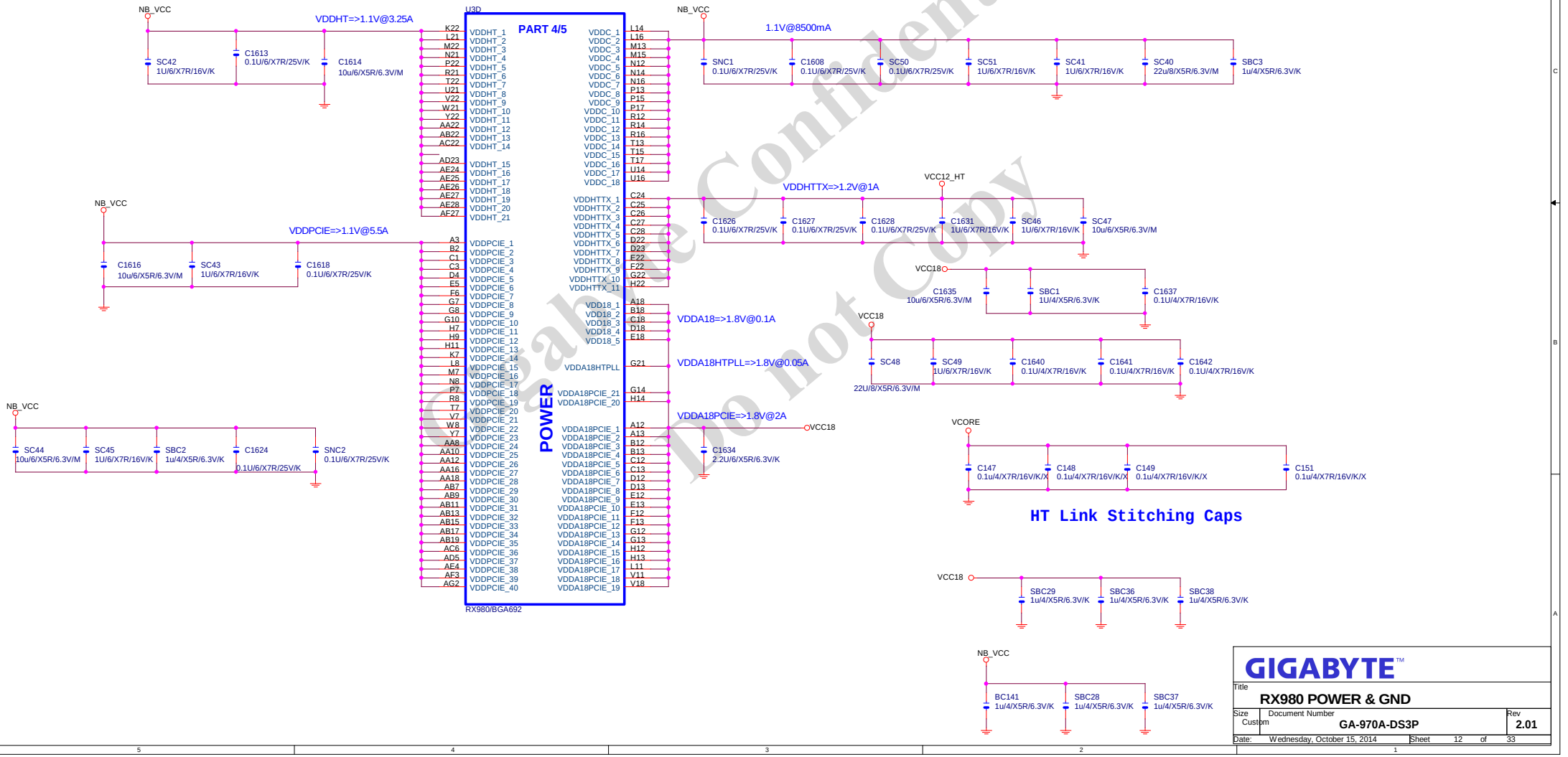

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Title	RX980 POWER & GND	
Size: Custom	Document Number: GA-970A-DS3P	Rev: 2.01
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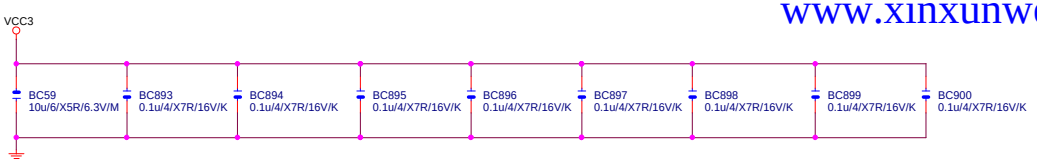


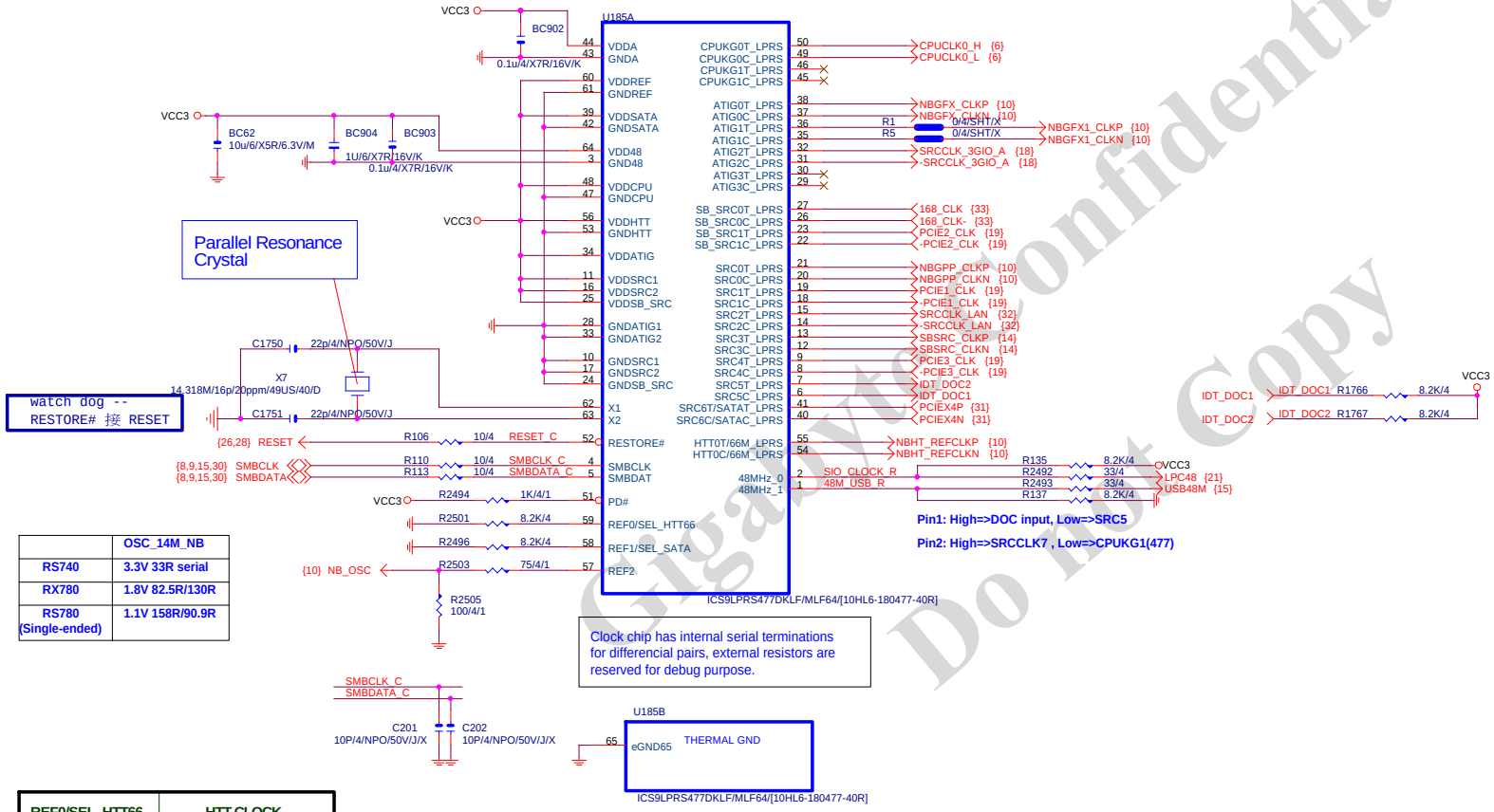
1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Pin1: High=>DOC input, Low=>SRC5
Pin2: High=>SRCCLK7 , Low=>CPUKG1(477)

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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Title: ICS9LPRS477

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-42R_12SP2-030005-43R]

SB800 Part 1 of 5

PCI EXPRESS INTERFACES

PCI INTERFACE

PCI CLKS

CLOCK GENERATOR

LPC

CPU

RTC

SB950/BGA605/[10HB1-06B950-10R]

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting
EC AOD-ACC

	LPC_CLK0 Rev.A12	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

PX1 SHW/D0.64*5.08*6.74

Title	ATI SB950 PCIE/PCI/CPU/LPC
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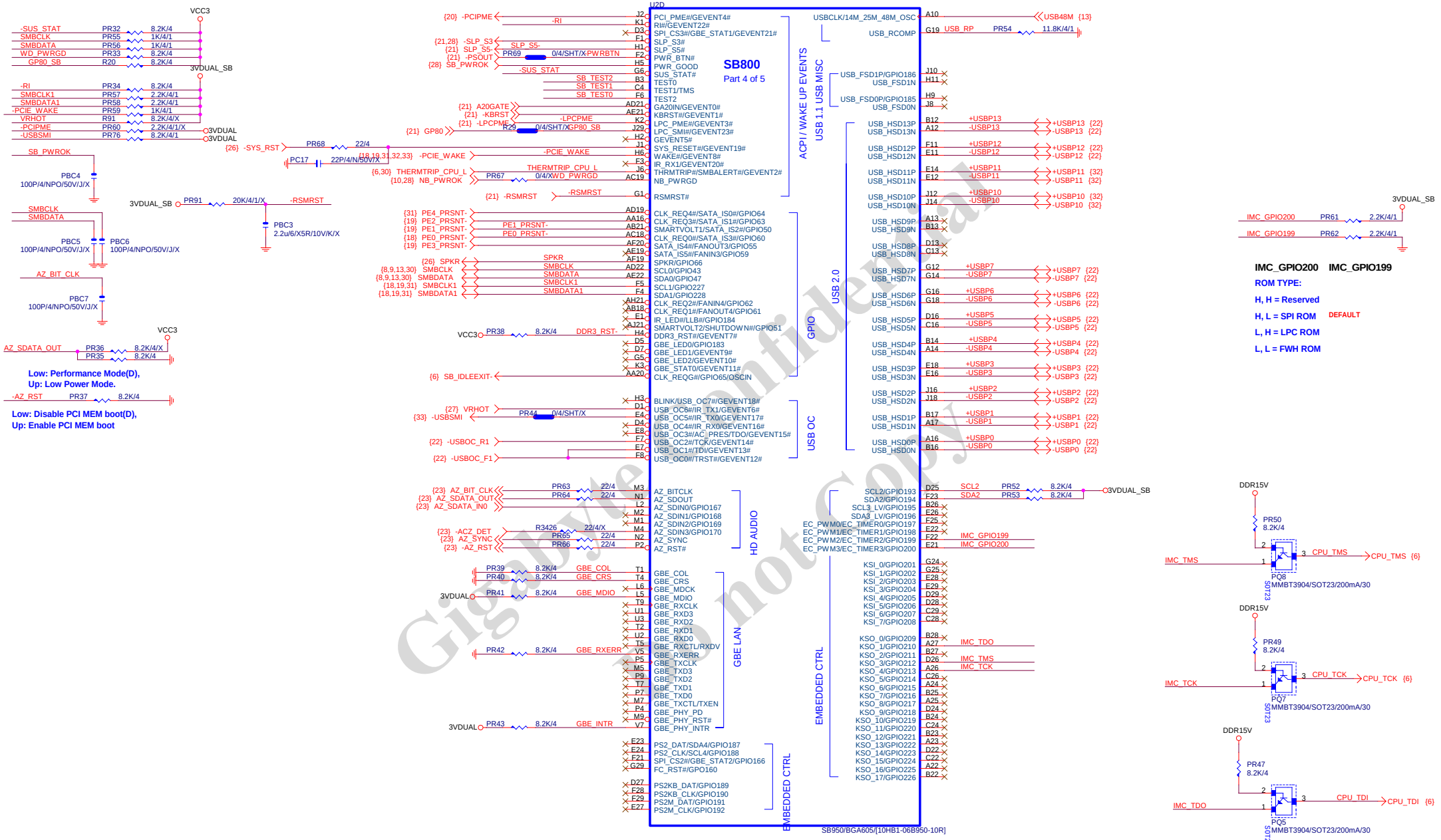

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Title: ATI SB950 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
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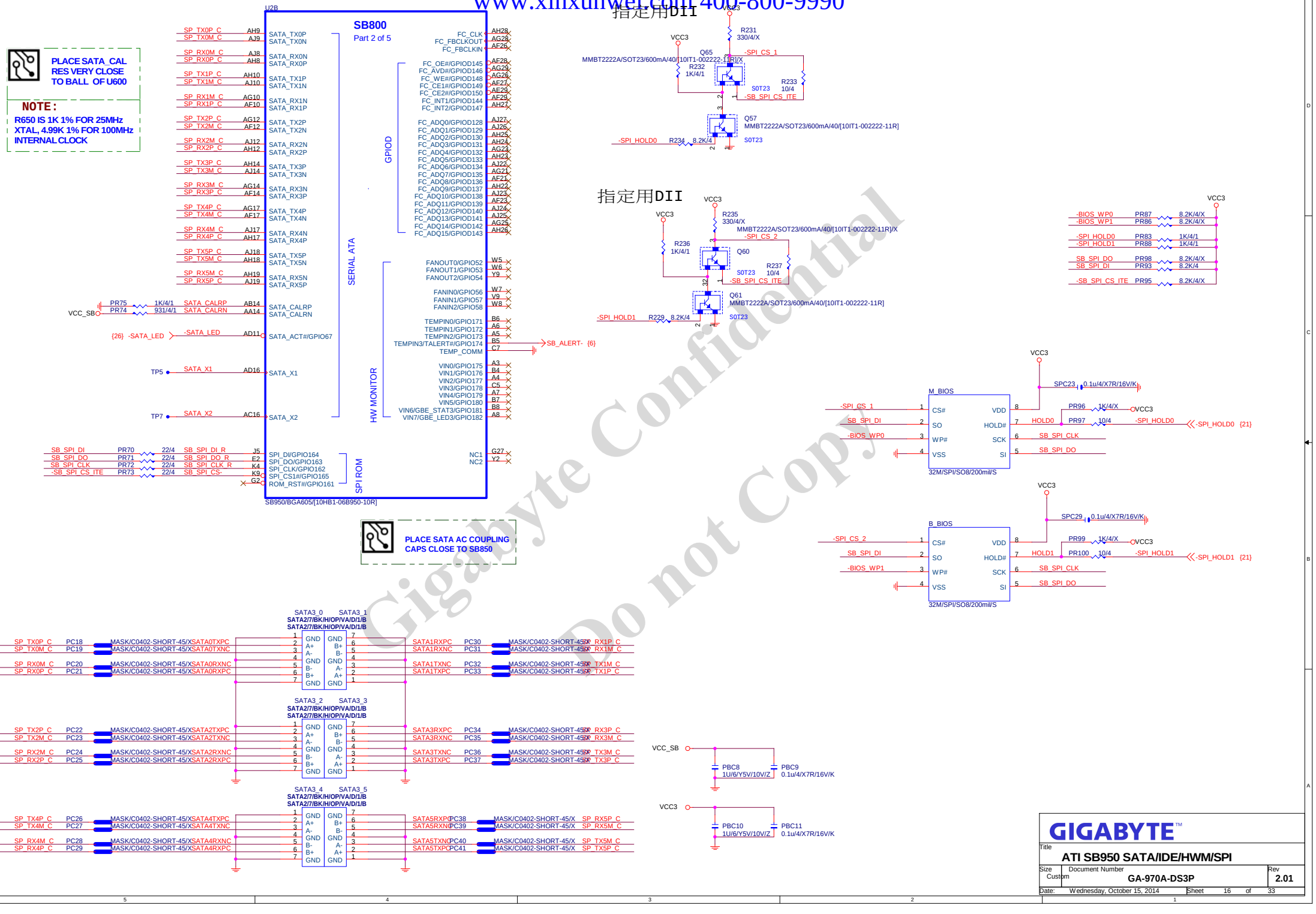

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Title: ATI SB950 SATA/IDE/HWM/SPI

Size	Document Number	Rev
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U2C

SB800 Part 3 of 5

POWER

SB950/BGA605/[10HB1-06B950-10R]

U2E

SB800

GROUND

Part 5 of 5

SB950/BGA605/[10HB1-06B950-10R]

Title	ATI SB950 POWER & GND
Size	Custom
Document Number	GA-970A-DS3P
Rev	2.01
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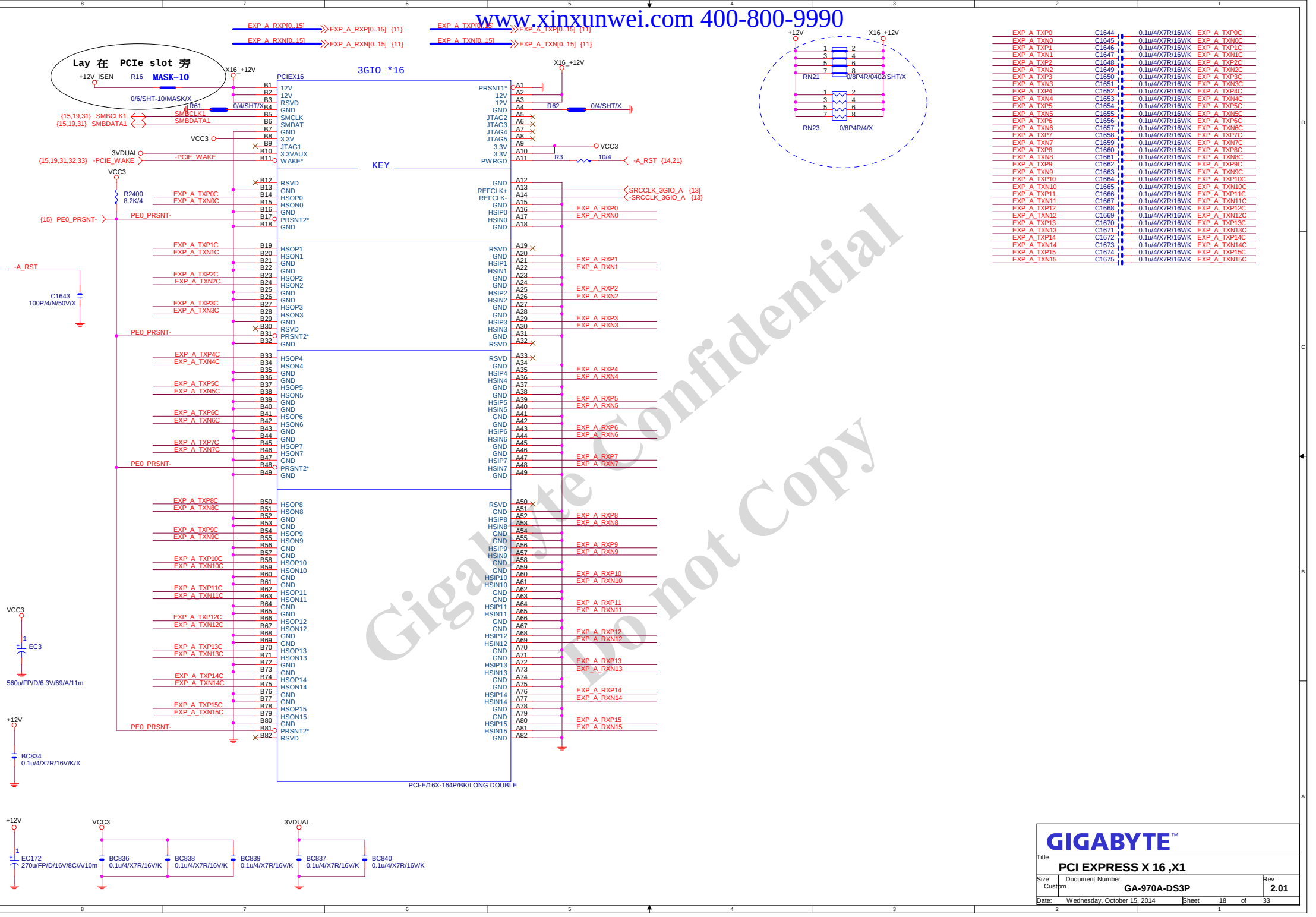

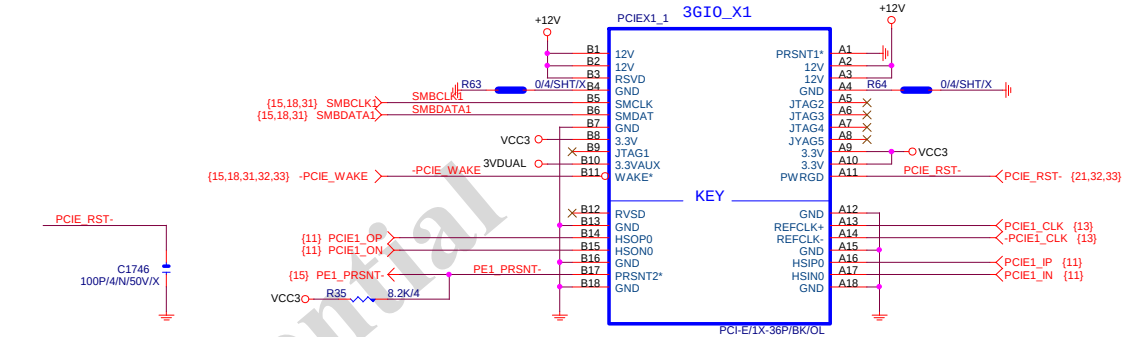

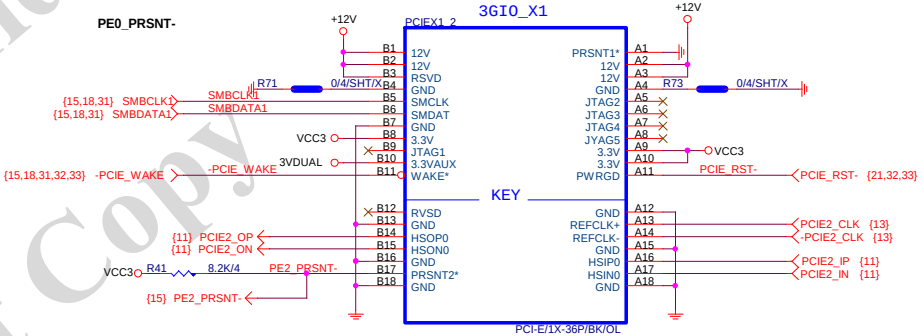

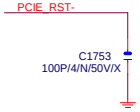

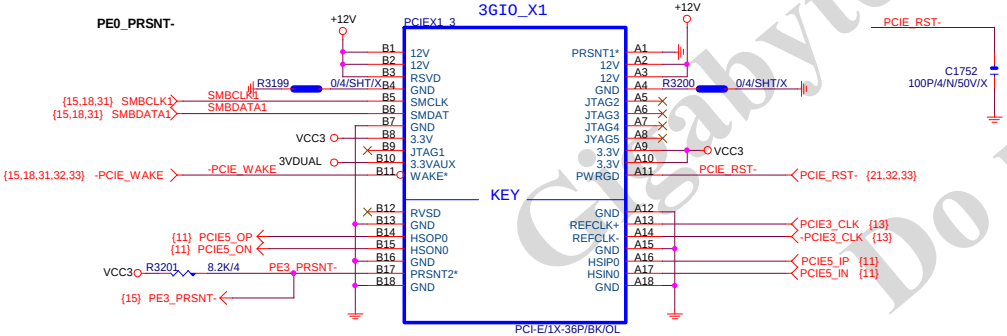

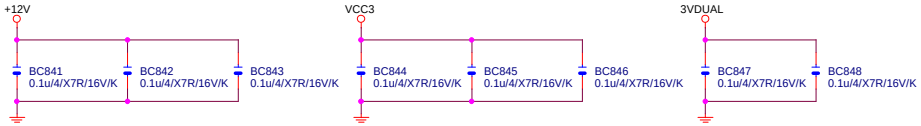

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Title: PCI_E x4 ,PCI_E x1 SLOT 2,3 ,Switch

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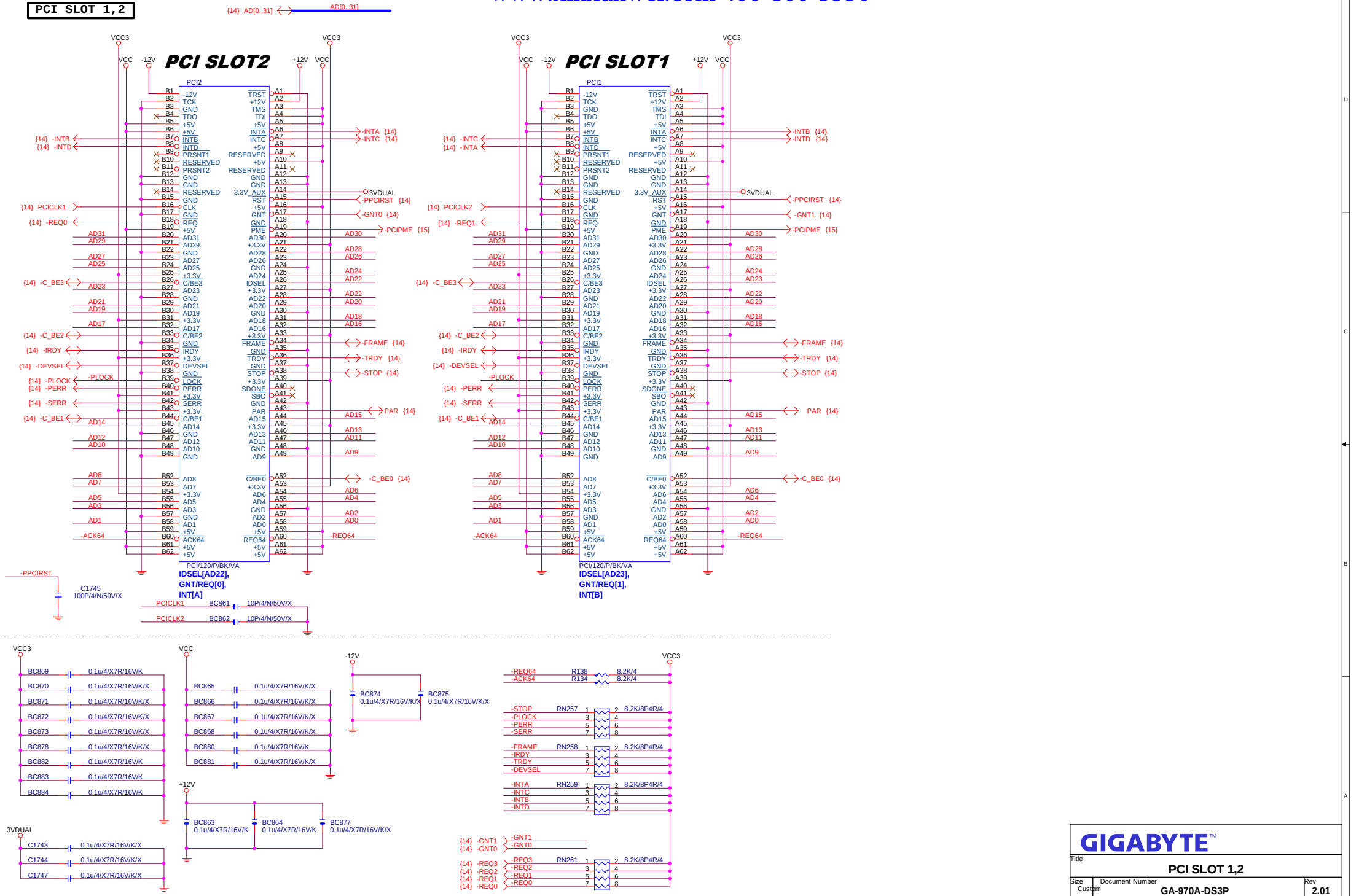
PCI SLOT 1,2



Title	PCI SLOT 1,2		
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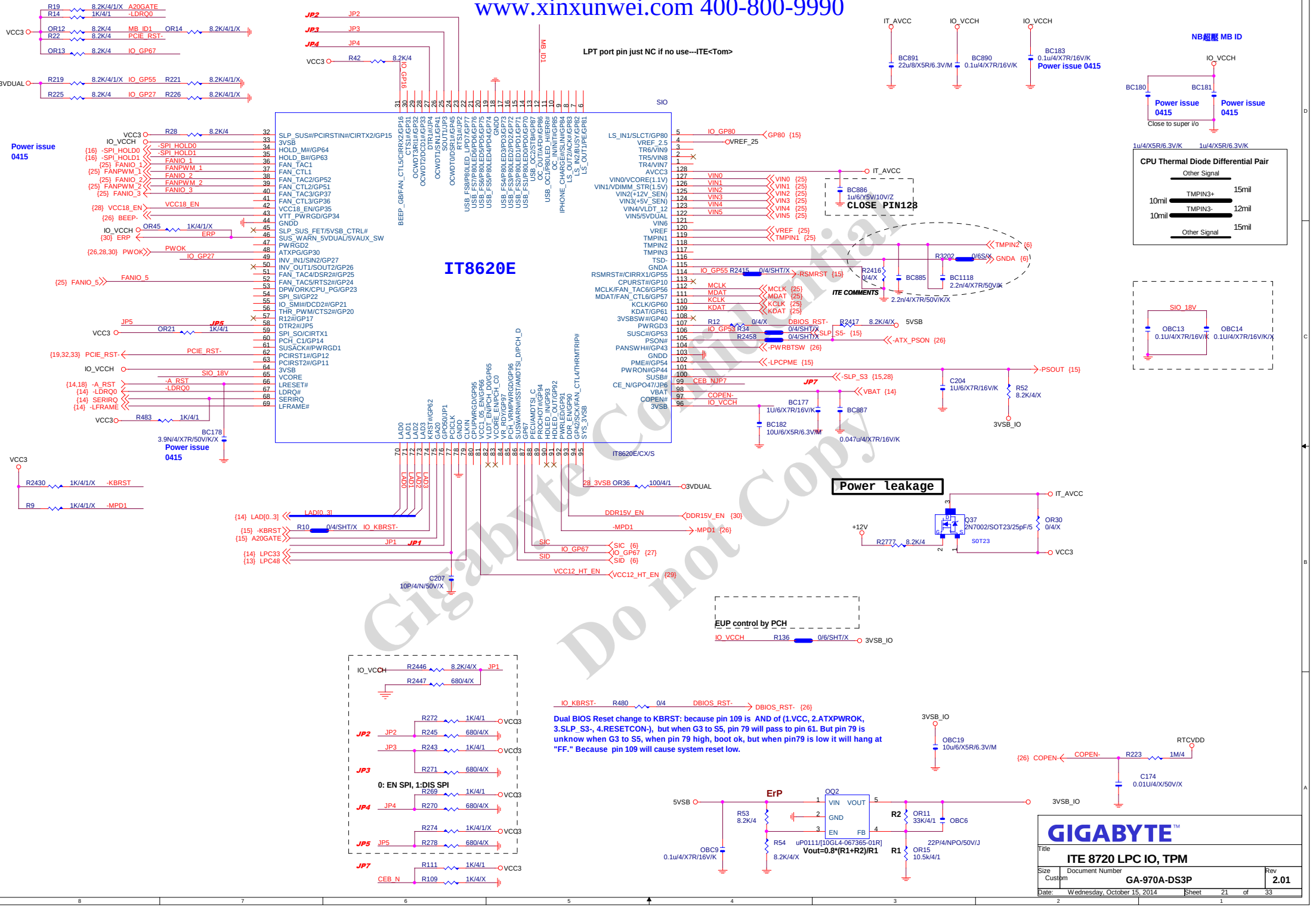

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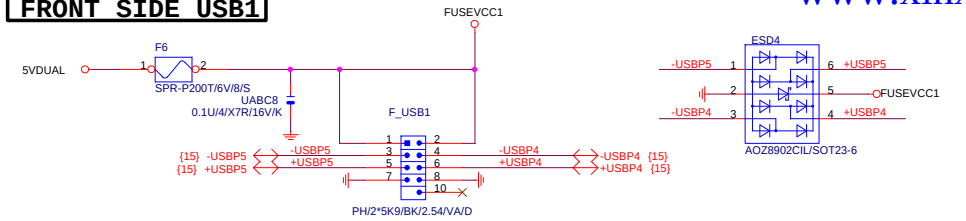
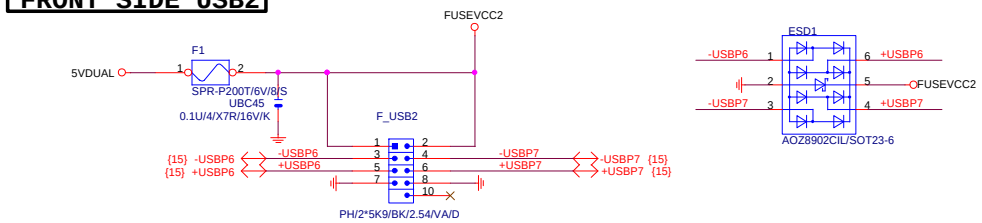
FRONT SIDE USB1



FRONT SIDE USB2



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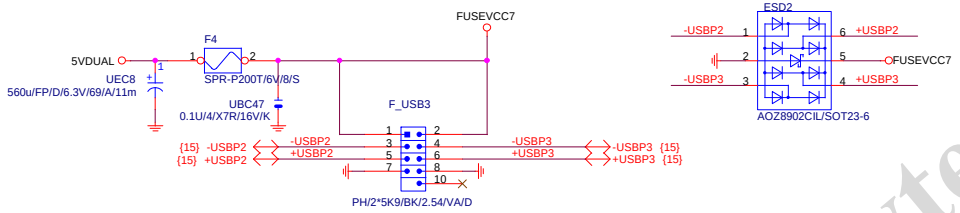

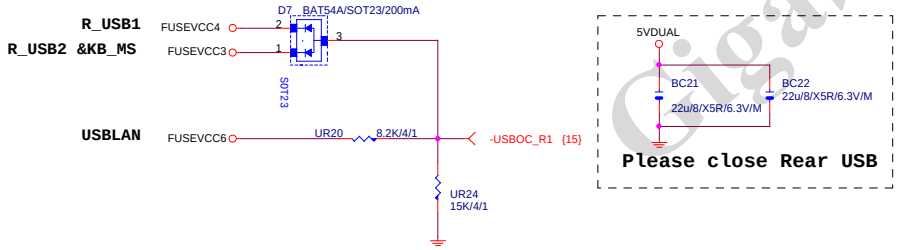

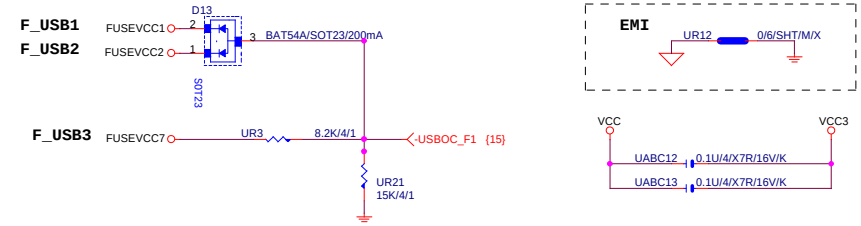

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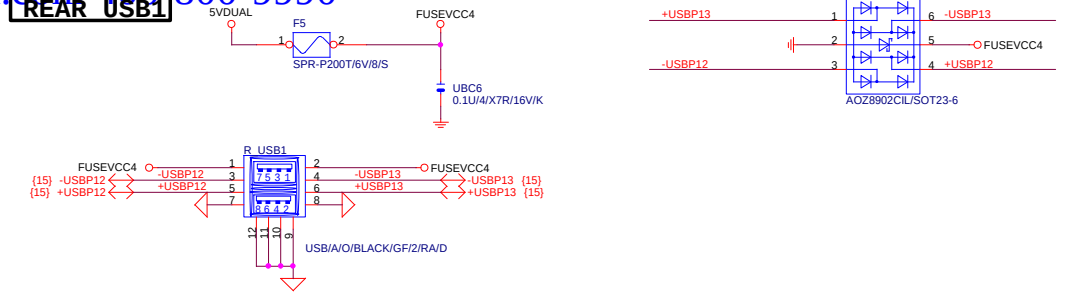

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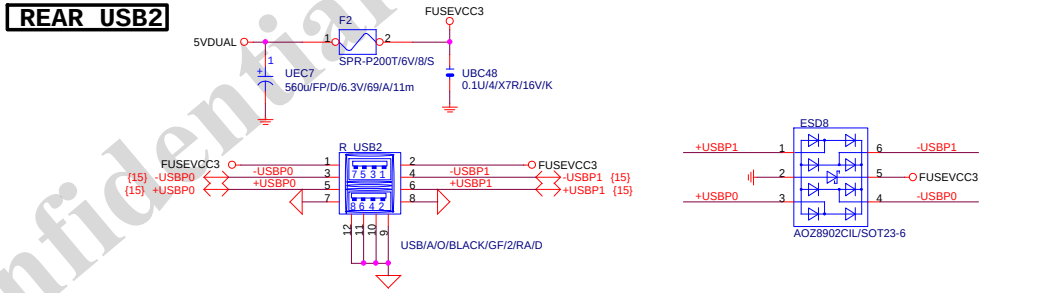

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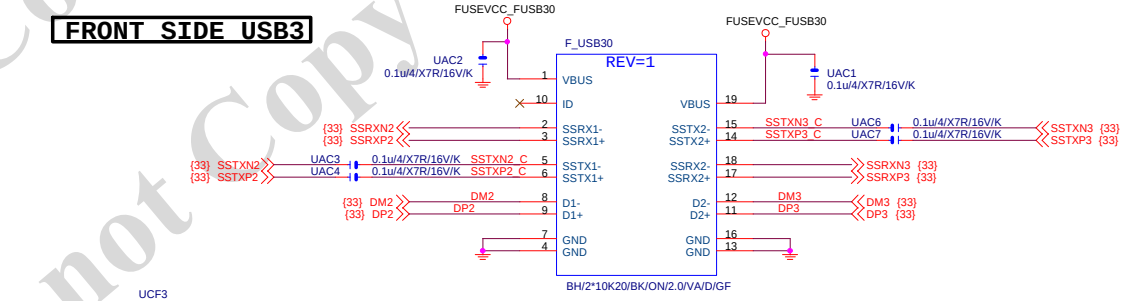
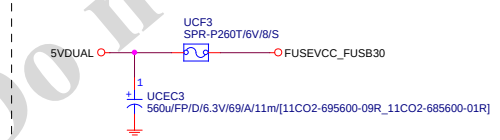
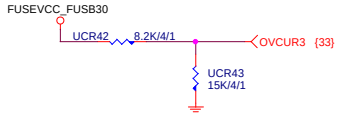
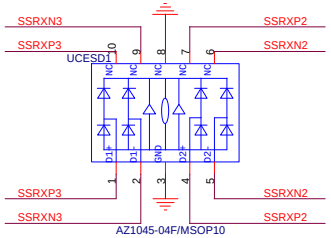
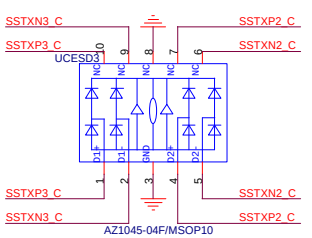




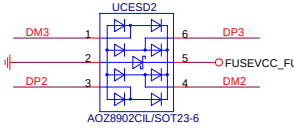




Close to connector



Close to connector



Close to connector

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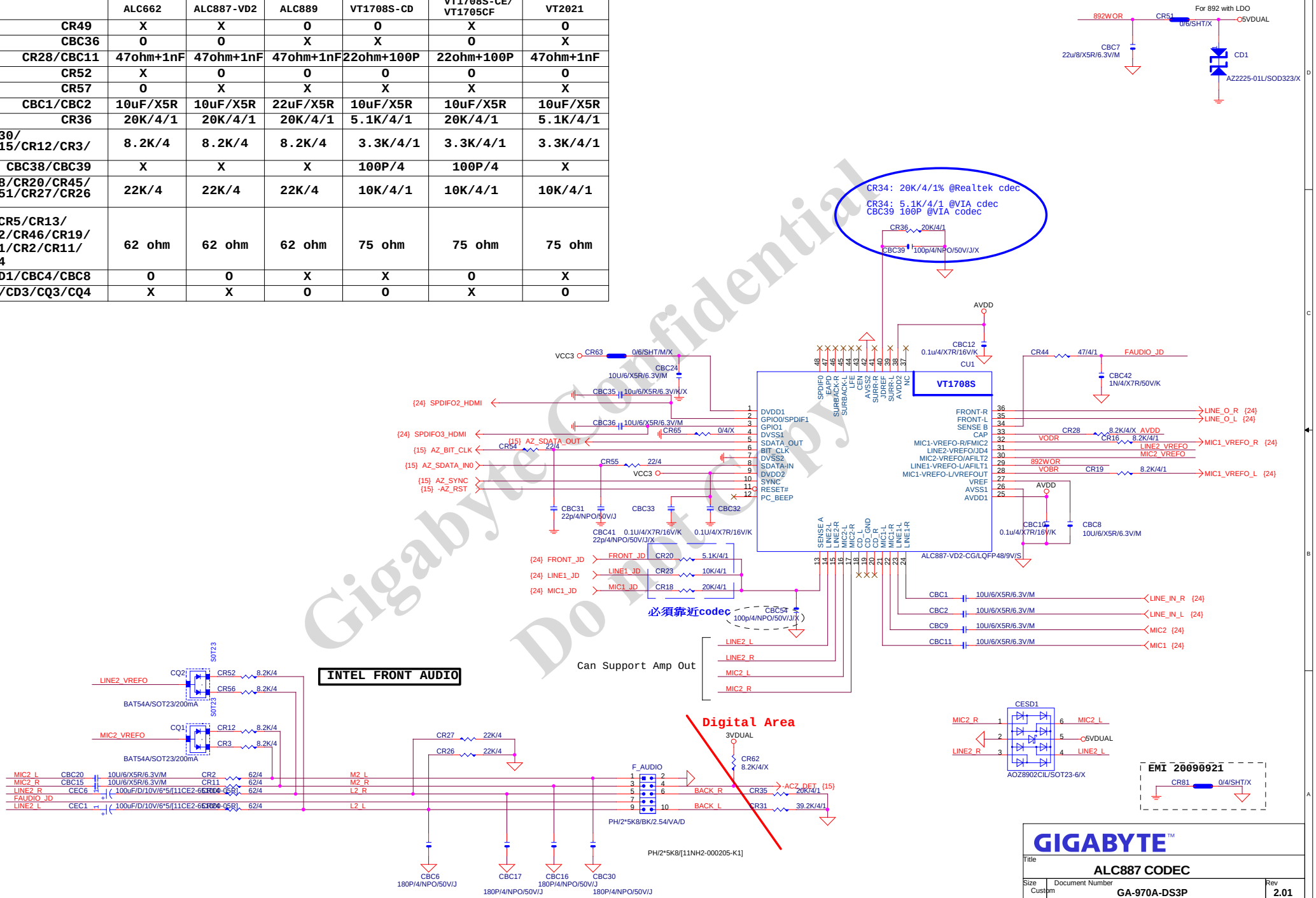
AZALIA CODEC *ALC662-VD0/ALC887-VD2/ALC889/VT1708S-CD/VT1708S-CE/VT2021 Colay*

	ALC662	ALC887-VD2	ALC889	VT1708S-CD	VT1708S-CE/ VT1705CF	VT2021
CR49	X	X	O	O	X	O
CBC36	O	O	X	X	O	X
CR28/CBC11	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P	47ohm+1nF
CR52	X	O	O	O	O	O
CR57	O	X	X	X	X	X
CBC1/CBC2	10uF/X5R	10uF/X5R	22uF/X5R	10uF/X5R	10uF/X5R	10uF/X5R
CR36	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1	5.1K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3/	8.2K/4	8.2K/4	8.2K/4	3.3K/4/1	3.3K/4/1	3.3K/4/1
CBC38/CBC39	X	X	X	100P/4	100P/4	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR27/CR26	22K/4	22K/4	22K/4	10K/4/1	10K/4/1	10K/4/1
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR2/CR11/ CR14/CR24	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm	75 ohm
CFB1/CD1/CBC4/CBC8	O	O	X	X	O	X
CD2/CD3/CQ3/CQ4	X	X	O	O	X	O



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Title	ALC887 CODEC		
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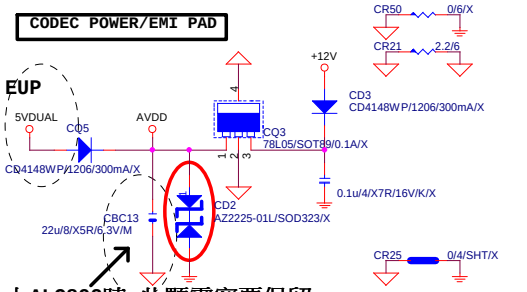
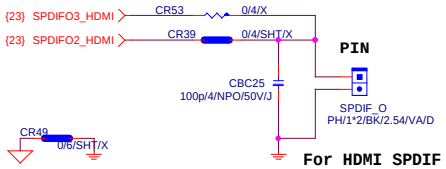
CODEC POWER/EMI PAD



上ALC892時,此顆電容要保留

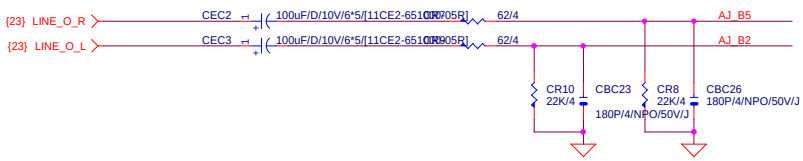
ADD CD2 For ESD PROTECT DIODE

SPDIF



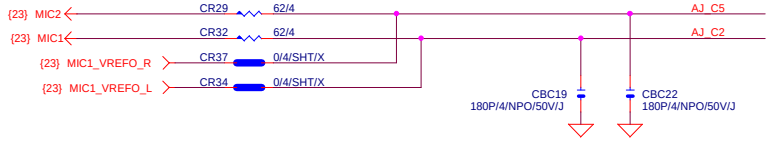
For HDMI SPDIF

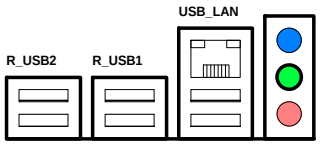
LINE OUT FRONT OUT

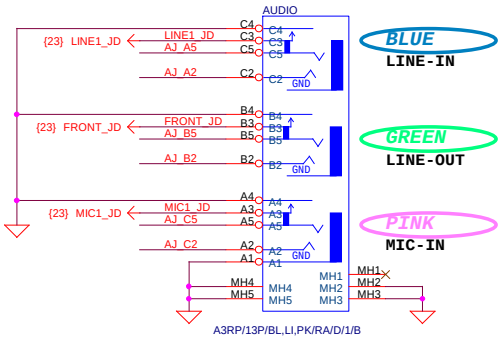


LINE-IN

MIC







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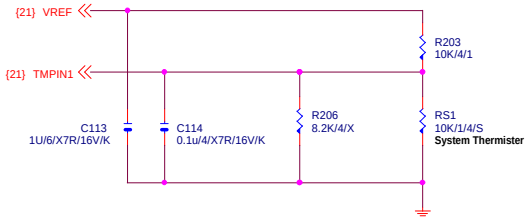
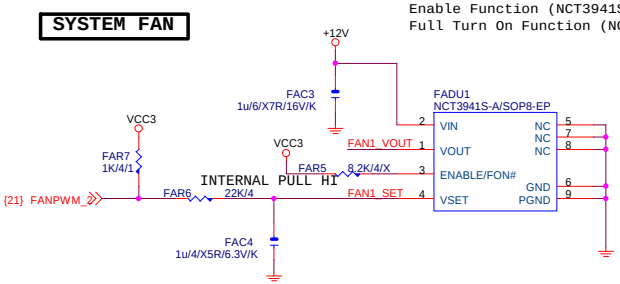
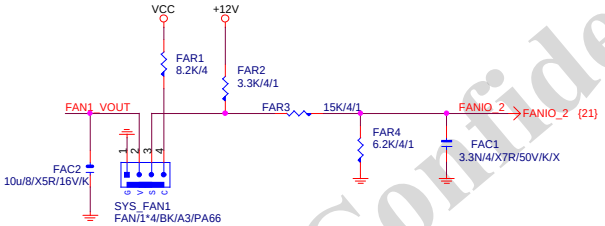
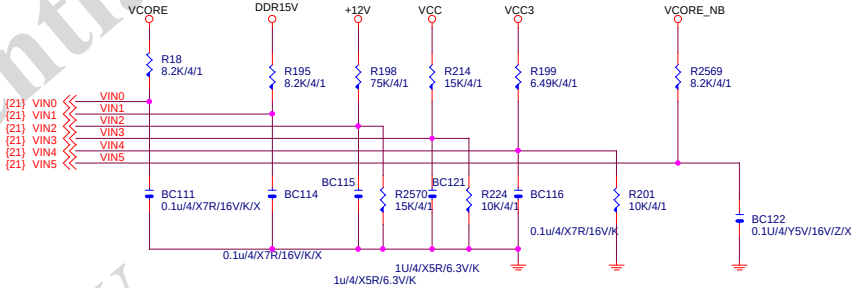
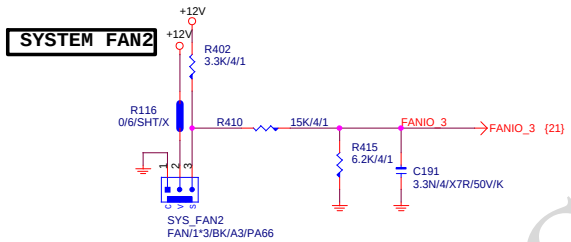
Hardware Monitor circuits

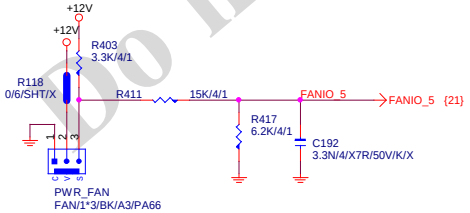


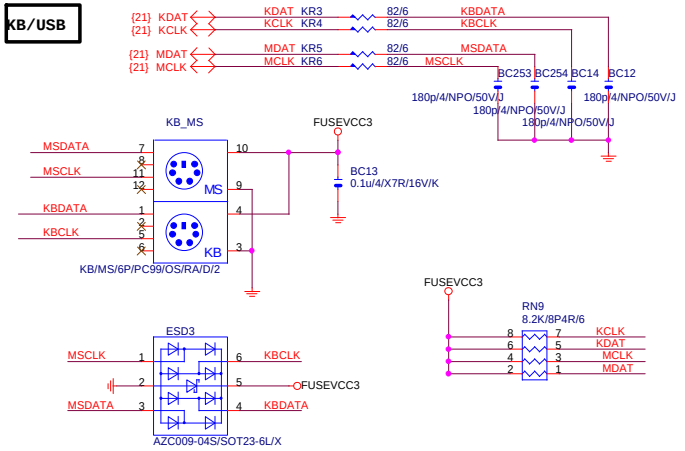


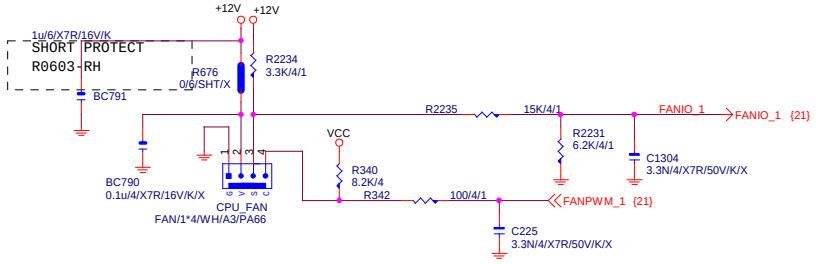












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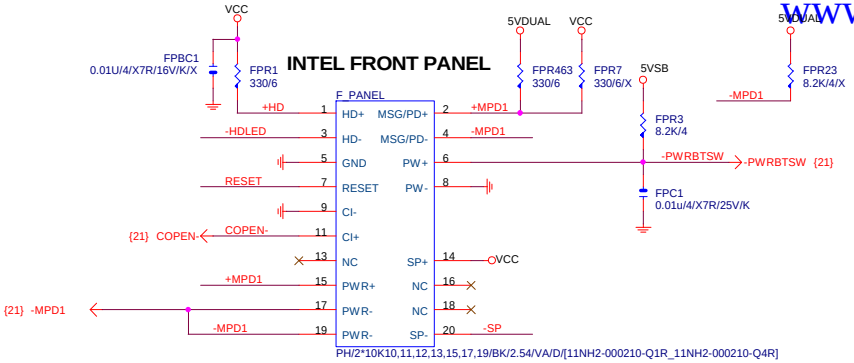
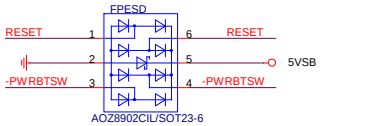
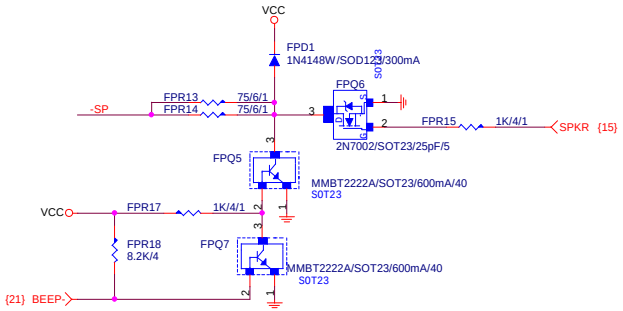
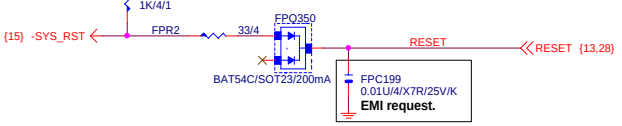
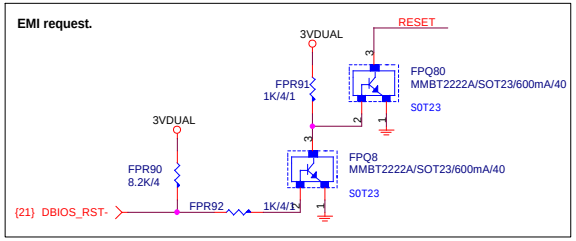
INTEL FRONT PANEL

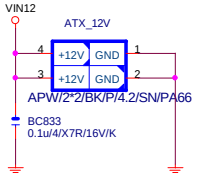


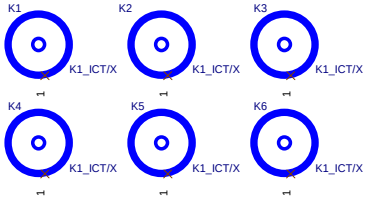


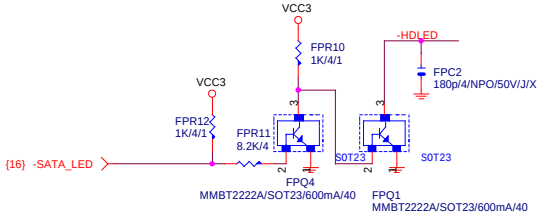




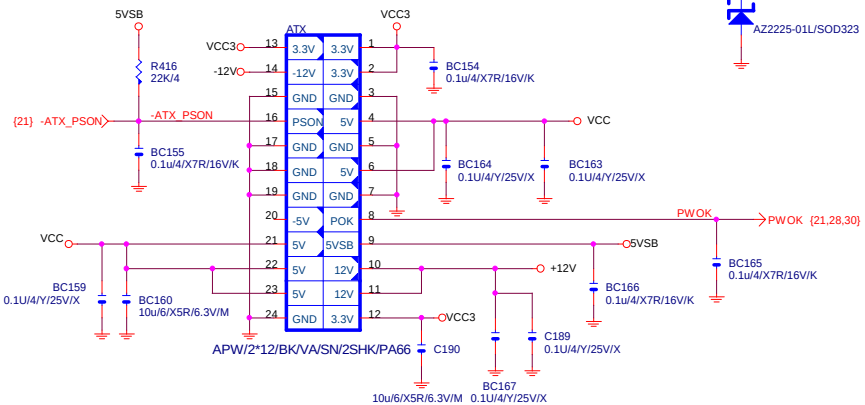


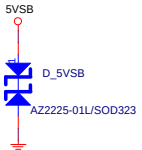


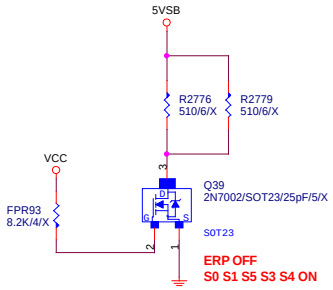


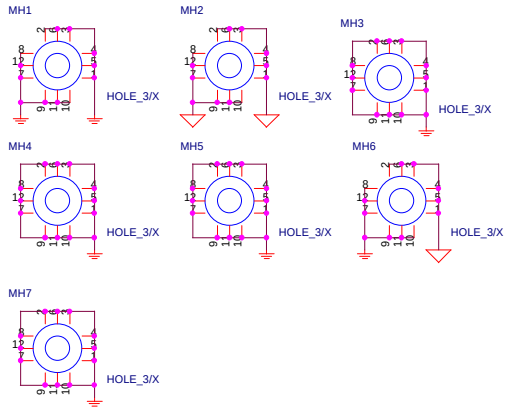


ATX POWER CONNECTOR









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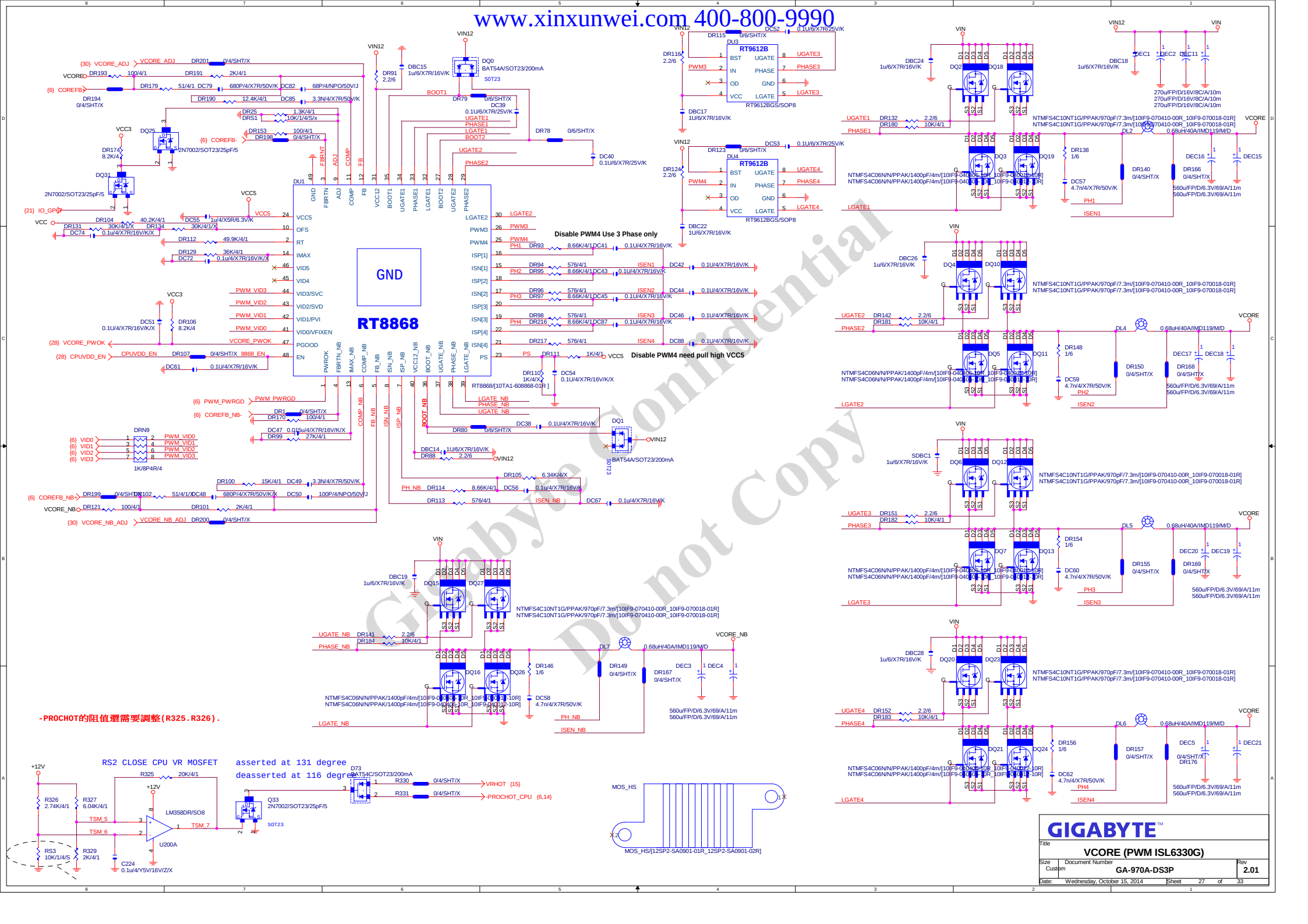
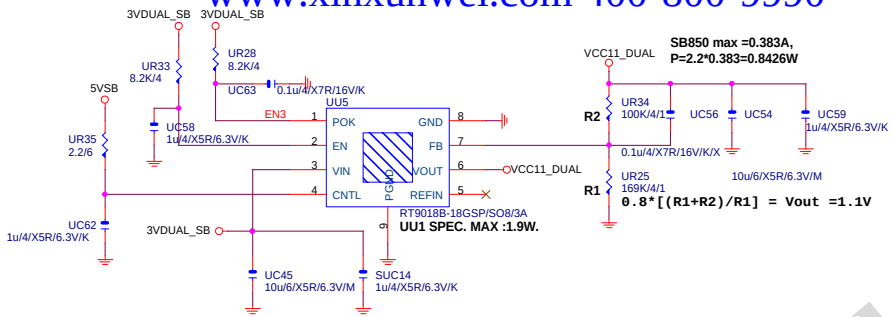
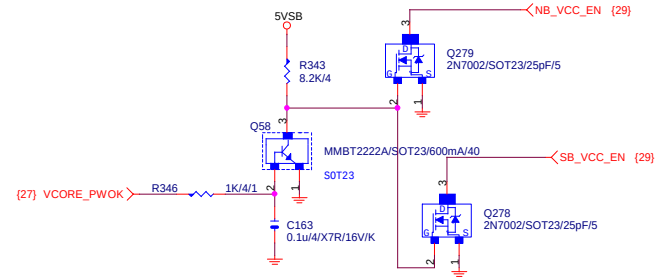
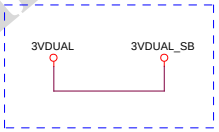
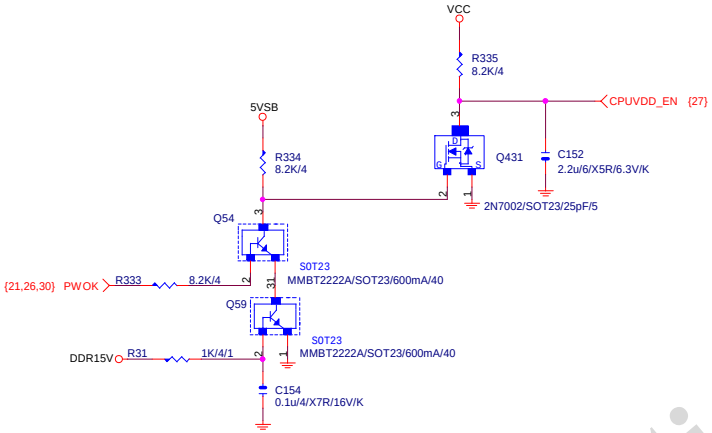


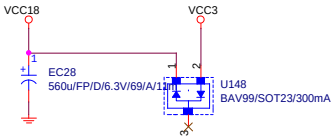


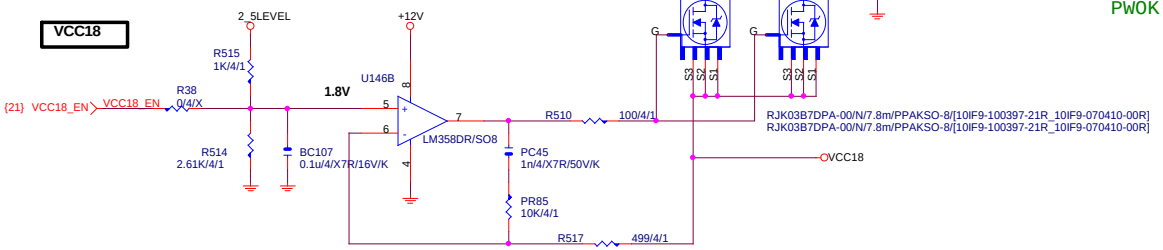


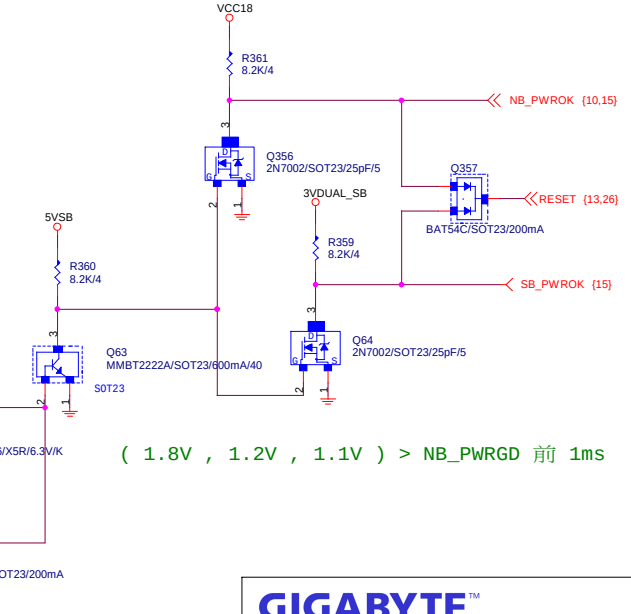




ATI for VCC3/VCC18 power ramp-up 2.1V







PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

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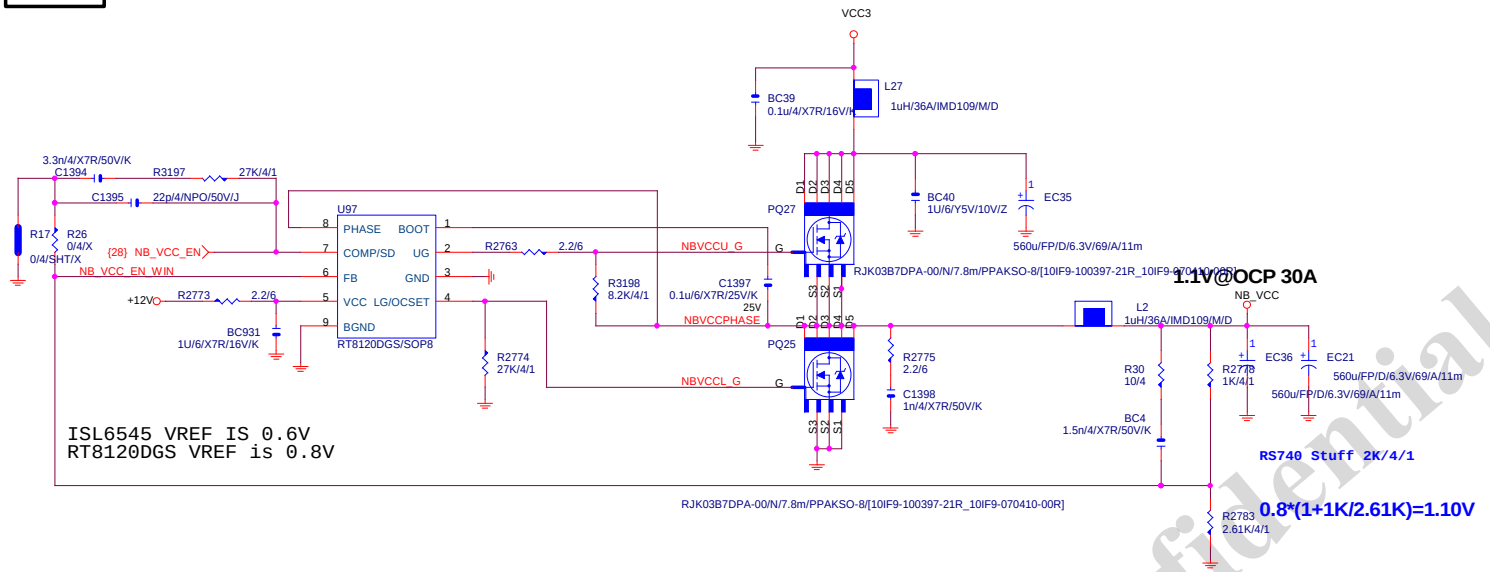
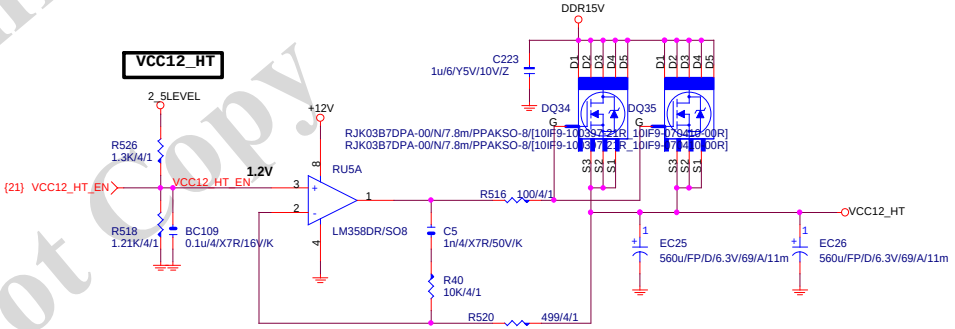
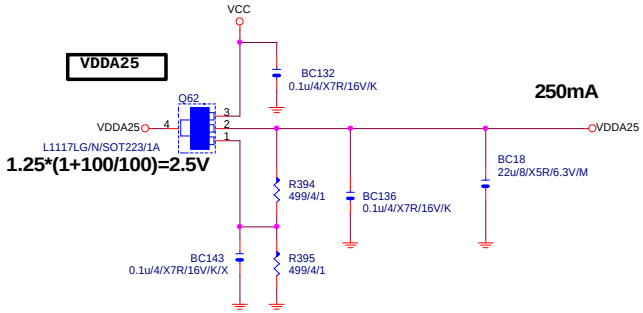
VCC_NB



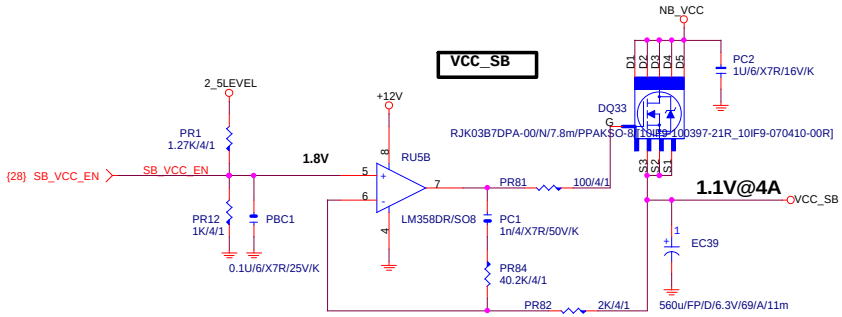
VCC12_HT



VDDA25



VCC_SB



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Title	NB POWER , VCC12HT , VDDA25	
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R2038不能上,會導致LM324 PIN1不能完全拉Lo

5VDUAL

ITE8620 FOR POWER SUPPLU ISSUE

9.5V / 25A protect

9.5*(1.21K/(13.3K+1.21K))=0.792V

5VSB OVP: 7V protect.

5.0V:0.4V,
7.5V:0.602V,
9.0V:0.722V

ErP

3.75V

0X20 = 100% xVCC

ISL6545 R9=>0 , R8=>NC
RT8120 R9=>NC, R8=>0

1.5V@OCP:30A Default: 1.5V, from AMD

0.8*(1+1K/1.14K)=1.5V

1.25*(1+169/100)=3.36V

ISL6545 VREF IS 0.6V
RT8120DGS VREF is 0.8V

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Title: DDRII POWER , VCC18

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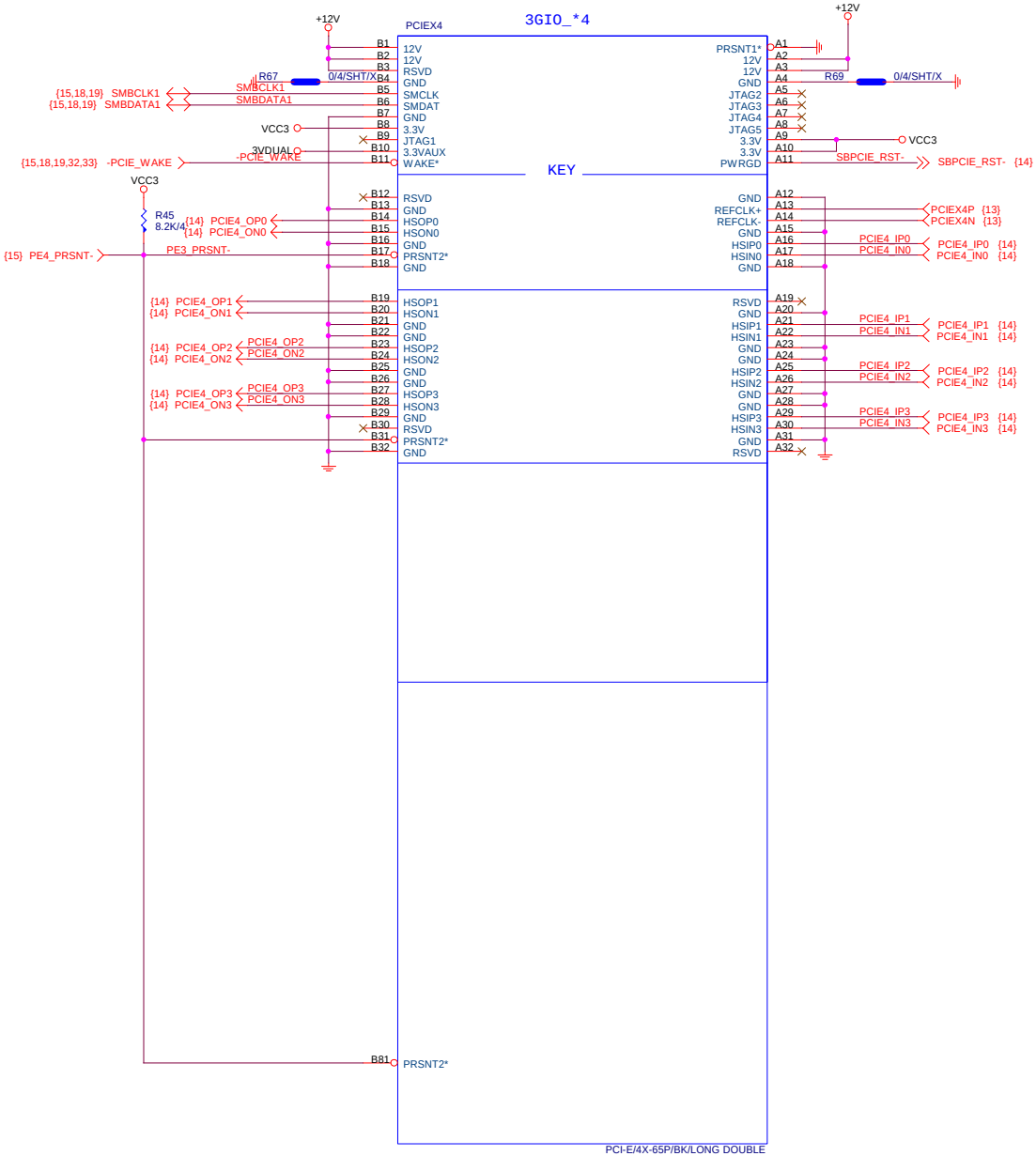

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Title: JMB362		
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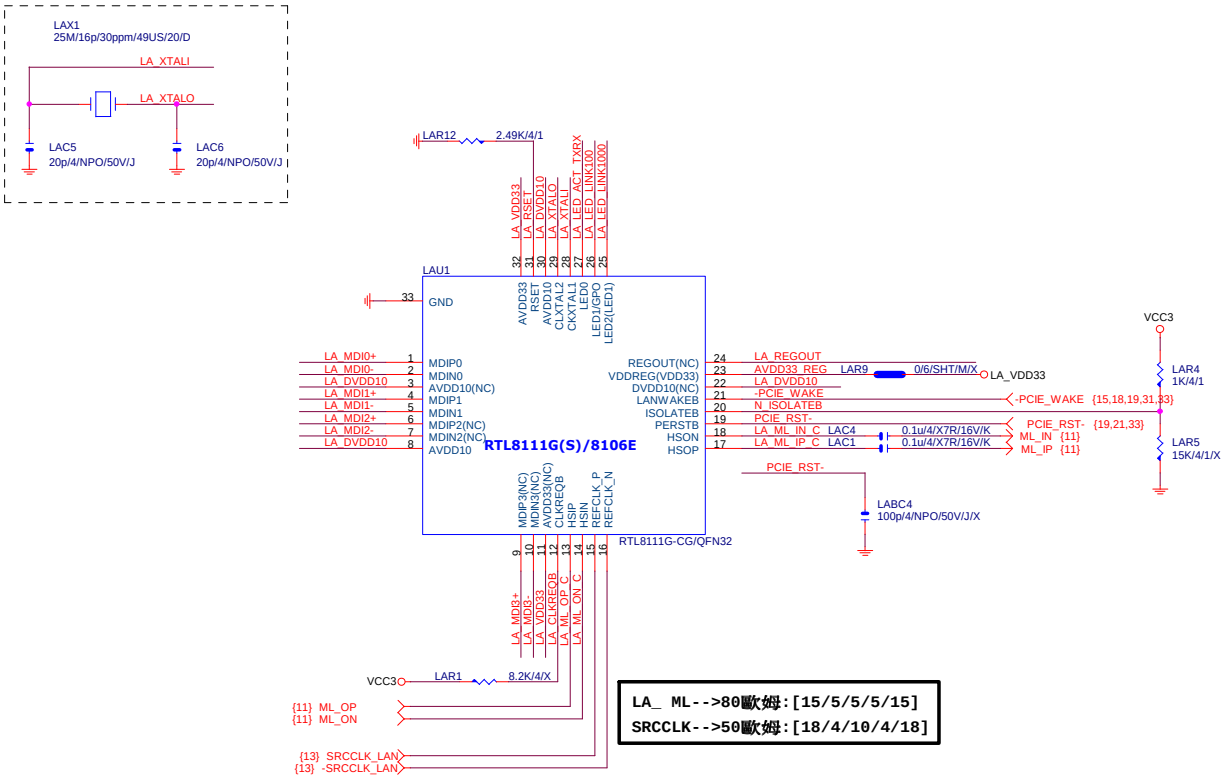
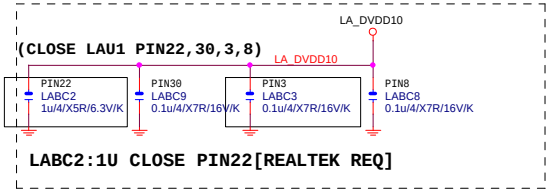
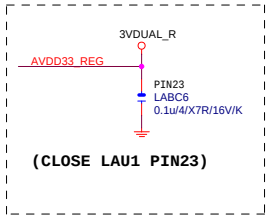
LAN:RTL8111G

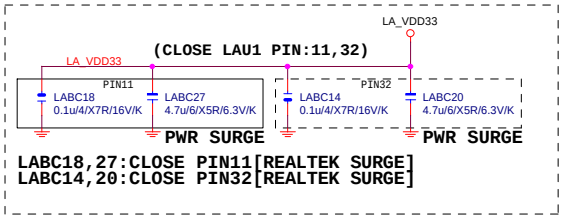


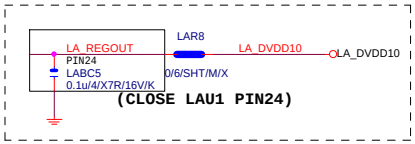
LA_ ML-->80歐姆:[15/5/5/5/15]
SRCCLK-->50歐姆:[18/4/10/4/18]

LAN POWER



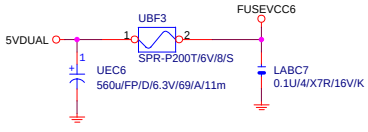


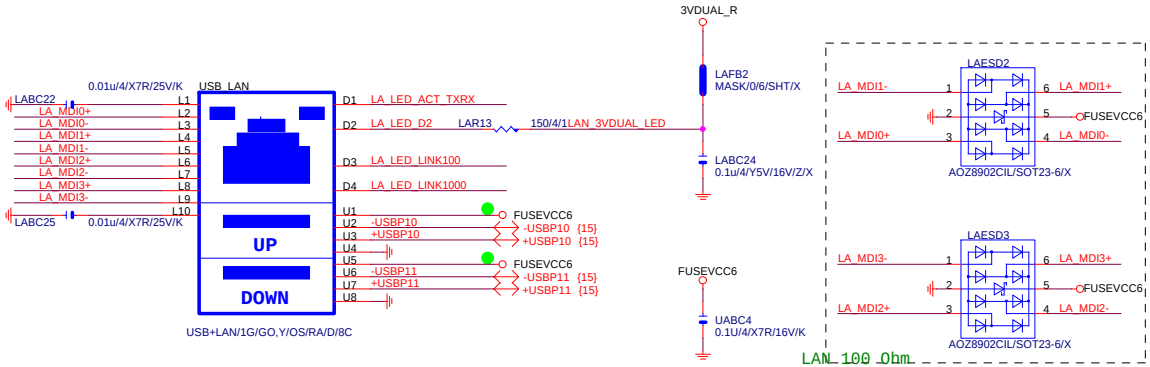




NOTE:
RT8106E:PIN3,11,22,24-->NC
LABC2LABC3,LABC5,LABC18,LABC27-->N/A

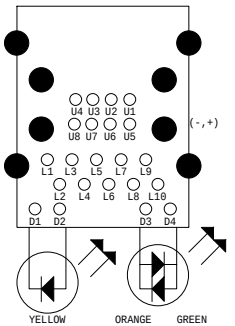
USB_LAN





EMI 2011.04.18
Between USB_LAN & USB Connector
GNDR2 MASK/0/4/SHT/M/X
Between USB & HDMI Connector
GNDR3 MASK/0/4/SHT/M/X

RU9 TYPE



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