COMPAL CONFIDENTIAL

MODEL NAME : Bullseye TGL

PCB NO : DA8001NI000

PCB 2X2 LA-K033P REV0 M/B 1 S

TGL-U+N17S-G3+MEC1515 (DSC)

2020-09-01

REV : 1.0 (A00)

TGL CPU QS

UC1 SA0000DRS1L QS_I3@
S IC A31 FH8069004531502 QVBG B1 3G S

UC1 SA0000DRR1L QS_I5@
S IC A31 FH8069004530601 QVBD B1 2.4G S

UC1 SA0000DRG1L QS_I7@
S IC A31 FH8069004529905 QVBA B1 2.8G S

TGL CPU Base-U

UC1 SA0000DXG0L PENTIUM@
S IC A31 FH8069004531802 QVBK B1 2G S

UC1 SA0000DXH0L CELERON@
S IC A31 FH8069004531901 QVBS B1 1.8G S

TGL CPU R3

UC1 SA0000DTV2L R3_I3@
S IC FH8069004531602 SRK08 B1 3G A31 !

UC1 SA0000DTU2L R3_I5@
S IC FH8069004531301 SRK05 B1 2.4G A31 !

UC1 SA0000DTT2L R3_I7@
S IC FH8069004530104 SRK02 B1 2.8G A31 !

DAZ part number
DAZ2X200201 - GCE
DAZ2X200202 - TRIPOD
DAZ2X200203 - HSB
DAZ2X200204 - TMT

@ : Un-pop Component
DIS@/DISRF@ : GPU Surpport
M_STRAP@/H_STRAP@/S_STRAP@ : VRAM strap pin
2G_G5@/4G_G5@ : 2G GDDR5 / 4G GDDR5 VRAM
UMA@ : not Support external Graphic card
N3@/V3@ : Inspiron/Vostro
MSFT@/NMSFT@ : MSFT SKU / Normal SKU
G3@ : Support G3 sharing SPI topology
CNV@ : Support CNVi function
S5LID@/LID@ : Support S5 LID power up Function/Normal LID close
ES_I3@/ES_I5A@/ES_I5B@/ES_I7@ : TGL-U QS Sample
STG@ : C10_gate control VCCSTG
I2CTCH@/USBTCH@ : Touch Screen support I2C signal / USB signal
BASE@/PREM@ : Pentium,Celeron/i3,i5,i7
I2CPAD@/PS2PAD@ : EC use I2C touch PAD signal(or PS2)
JP@/JUMP@/PJP@ : JUMP
100@/1000@ : 10/100 LAN / Giga-LAN
PRO@/ICPRO@ : only LCDVDD protection/Hinge up protection Support
EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
KBBL@ : KB Backlight
TPM@/NTPM@ : HW TPM/SW TPM
750_CTPM@ : 750 and china TPM
CTPM@/ST_CTPM@ : China TPM/ST China TPM
FFS@ : Free Fall Sensor
TYPEC@/NTYPEC@ : Support TypeC/non-TypeC
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component
LBIST@/LBIST@RF@ : LBIST for LCD monitor
N17S_G3_R3@/N17S_G3_R1@ : N17S-G3-A1_BGA_595P GPU
TP@/CMC@TP@ : Test Point/XDP Test Point
DISPCB@/UMAPCB@ : PCB MB

Layout Dell logo

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Title: **Cover Page**

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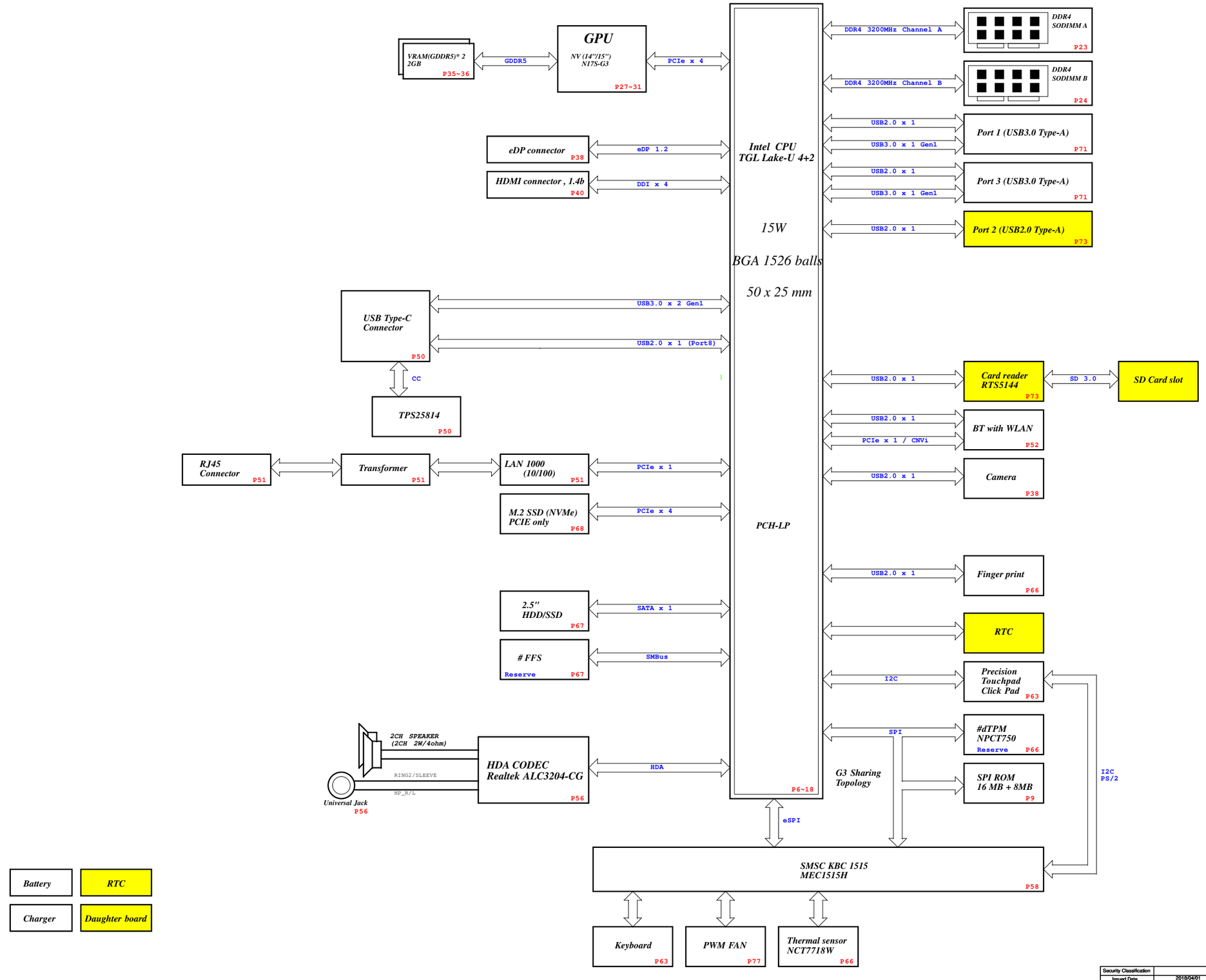
Block Diagram



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Title: Block Diagram		
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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 port3, IO/B
4	Typec-C
5	Finger printer
6	CCD
7	Card reader , IO/B
8	Touch screen
9	Reserved
10	BT

Board ID & Model ID Table

Bullseye TGL			
NBDR	SKU	Model-ID (RE4 PD-100K)	Board-ID (RE2 PD-100K)
	UMA	RE3 PU-10K	RE1 PU-10K -EVT RE1 PU-17.8K -DVT1 RE1 PU-27.0K -Reserve RE1 PU-37.4K -DVT2 RE1 PU-49.9K -Reserve RE1 PU-64.9K -Pilot RE1 PU-82.5K -Reserve
	DSC - N17S-G3	RE3 PU-17.8K	

Voltage Rails

Power Plane	Descript i on	S0	S3	S4/S5	G3	
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A	N/A	
+17.4V_BATT++	Bat t ery po wer s upply	N/A	N/A	N/A	N/A	
+19VB	AC or bat t ery po wer r ail f or Syst e m	N/A	N/A	N/A	N/A	
+RTC_SOC	RTC power	ON	ON	ON	ON	
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*	OFF	
+5VALW	System +5V always on power rail	ON	ON	ON*	OFF	
+3VALW	System +3V always on power rail	ON	ON	ON*	OFF	
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*	OFF	
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*	OFF	
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF	
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF	OFF	
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF	
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF	
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF	
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF	
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF	
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	OFF	
+3VALW_DSW	+19VB to DSW power rail for suspend power	ON	ON	ON	OFF	
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*	OFF	
+5VS	System +5VS power rail	ON	OFF	OFF	OFF	
+3VS	System +3VS power rail	ON	OFF	OFF	OFF	
+1.35V_MEM_GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF	
+3VGS	+3V power rail for GPU	ON	OFF	OFF	OFF	
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF	OFF	
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF	OFF	
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF						

RE: ICL N3V3 MLK High Power Consumption on VCCIN_AUX Under S3/S5
Wu, Eddie <eddie.wu@intel.com>
寄件日期: 2019/6/6 (週四) 下午 09:41
收件者: Chiu. David (TPE); Chen. Johnny (TPE); Hung. Henry (TPE); Chang, Jay Sj; Liu. Joe (TPE); Lai. Carol (TPE); Kenny.Lu@dell.com
副本: Chen. AlexCL (TPE); Chang, Garyl; Hsiao, Jimmy

Hi David,
VCCIN_AUX only down to 0V while SLP_S0# is asserted.
On S3 mode, it only can down to 1.1V. Thanks.

Best Regards,
Eddie Wu +886-2-66221110

10.12.4 Power States

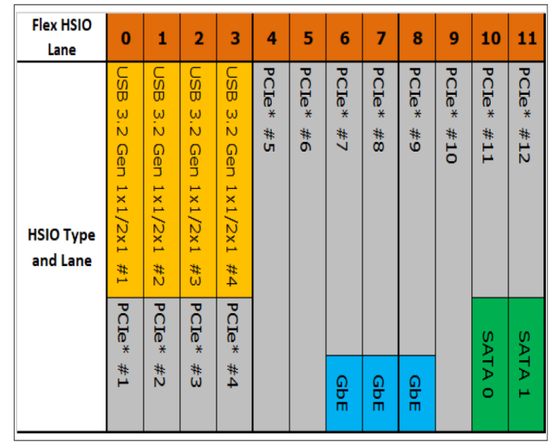
Table 207. System with M3 State Supported

Rails	SKUs	S0/M03	C102	S0ix/M-off[4]	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3[1]
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P05EXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
V1.8M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	ON [13]	ON [13]	OFF[6]	OFF[6]	OFF	No Power
VCCSTG	All	ON	OFF [2]	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON[11]	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON[11]	OFF[14]	OFF[14]	OFF[14]	OFF[14]	OFF	No Power

Note : VCCIN_AUX only down to 0V while SLP_S0# is asserted. On S3 mode, it only can down to 1.1V.

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIE-2		USB3.0 (MB)(Type-A)
USB3.0-3	PCIE-3		USB3.0 (Type-C)
USB3.0-4	PCIE-4		USB3.0 (Type-C)
	PCIE-5		PCIE SSD
	PCIE-6		PCIE SSD
	PCIE-7		PCIE SSD
	PCIE-8		PCIE SSD
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1	NC
	PCIE4 - 0		GPU
	PCIE4 - 1		GPU
	PCIE4 - 2		GPU
	PCIE4 - 3		GPU

Figure 77. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)



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Adapter/Bat t ery/19V
CPU PWR
GPU PWR
Peripheral Device PWR

ADAPTER
+19V_VIN
CHARGER ISL9538BHRTZ-T (PUB01) DSC
CHARGER ISL95522HRZ-T (PUB01) UMA
+17.4V_BATT+
BATTERY

+PWR_SRC (+19VB)

FUSE 1.5A_24V (F1) → +DCBAT_LCD

PJPW01 → RT6226AGQUF (PUW01) 1.35V_PWR_EN → +1.35VGPUP → PJPW02 → +1.35VS_VRAM

PJP501 → SY8180CRAC (PU501) ALWON -->EN_5V ENLDO_3V5V → +5VALWP → PJP502 PJP503 → +5VALW

+5VALW →
- SY6288D20AAC (UU1) USB_EN# → +USB3_VCC
- SY6288D20AAC (UU2) USB_EN# → +USB2_VCC
- EM5209VF (UZ2) SIO_SLP_S3# → +5VS
- PTP25814 (UT37) VBUS_P_CTRL# → +CCG_VBUS

+5VS →
- FUSE 1A_65V (F5) for USB TS → +TS_VDD (1)
- 0ohm 0805 (RA1) → +5V_PVDD
- 0ohm 0603 (RA3) → +5V_AVDD
- 0ohm 1206 (RS32) → +5V_HDD
- FUSE 1.5A_6V (FI1) → +5V_HDMI
- FUSE 0.5A_13.2V (F3) → +5V_KB_BL

PJP301 → SY8286BRAC (PU301) → +3VLP → BAS40C (D1) → +RTC_CELL → +RTC_CELL_VBAT to EC
+RTC_VCC → BAS40C (D1)
ALWON -->EN_3V ENLDO_3V5V → +3VALWP
PJP302 → +3VALW

+3VALW →
- SY6288C20AAC (UL2) AUX_ON → +LAN_VDD33
- EM5209VF (UZ2) SIO_SLP_S3# → +3VS
- TPS22967DSGR (UZ4) VCCDSW_EN_GPIO → +3VALW_PCH → D11 → +3.3V_SPI
  - RW1 0 ohm 0603 → +3.3V_WLAN
  - RC4165 0 ohm 0402 → +3VALW_DSW
- RT9059GSP (PU1001) 1.0VS_DGPU_EN → +1.0VGPUP
- 0 ohm 0402 (RE5) → +3VALW_EC

PJP1801 → RT8061AZQW (PU1801) PCH_PRIM_EN → +1.8VALWP → PJP1802 → +1.8V_PRIM

+1.8V_PRIM →
- PCH
- RC4164 0 ohm 0603 → +VCCPRIM_1P8
- RC4068 0 ohm 0603 → +VCCA_CLKLDO_1P8
- RC4068 0 ohm 0603 → +1.8VALW_EC
- AO3416L (QA1) → RA2 0 ohm 0402 → +1.8V_AVDD; RA5 0 ohm 0402 → +1.8V_CPVDD
- EM5209VF (UV2) → DGPU_MAIN_EN → +1.8VS_DGPU_MAIN; DGPU_PWR_EN_R → +1.8VS_DGPU_AON

G2895ALK21U (U4) Hinge up PROC SIO_SLP_S3# →
- +TS_VDD (2)
- +3VS_CAM (2)

PJP2501 → RT9059GSP (PU2501) SIO_SLP_S4# → +2.5VP → PJP2502 → +2.5V_MEM
DZ1 → +2.5V_PG

PJPM01 → RT8207PGQW (PUM01) +2.5V_PG → +1.2VP → PJPM02 → +1.2V_DDR
0.6V_DDR_VTT_ON → +0.6VSP → PJPM03 → +0.6V_DDR_VTT

RT3612EBGQW (PUZ1) IMVP_VR_ON_EN → +VCCIN
RT6543AGQW (PUG1) 1.8V_PRIM_PG → +VCCIN_AUX
RT8816BGQW (PUV01) VGA_CORE_EN → +VGA_CORE

+3VS →
- JPC3 → +3VS_SSD
- FUSE 0.5A_13.2V (F7) → +TP_VDD
- 0 ohm 0402 (RA6) → +3V_DVDD
- G2895ALK21U (U4) Hinge up PROC LCD_VCC_TEST_EN or EDP_VDD_EN → +LCDVDD (2)
- SY6288C20AAC (U1) LCD_VCC_TEST_EN or EDP_VDD_EN → +LCDVDD (1)
- FUSE 1A_65V (F4) → +3VS_CAM (1)
- FUSE 1A_65V (F6) I2C TS → +TS_VDD (1)

VCCST_EN_R → AOZ1334DI (UZ12) +VCCST_R RZ23 → +1.05V_VCCST

PCH → +VCC1.05_OUT_FET → CPU_C10_GATE# → AOZ1334DI (UZ8) +VCCSTG_R RZ17 STG@ → +VCCSTG_CPU
PCH → +VCCSTG_OUT_LGC → RC240 0 ohm 0402 → +1.05V_VCCSTG

Normal Protection use Fuse	Hinge up Protection Pop - U4
PRO@	ICPRO@
+LCDVDD (1)	+LCDVDD (2)
+TS_VDD (1)	+TS_VDD (2)
+3VS_CAM (1)	+3VS_CAM (2)

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Title: Power MAP

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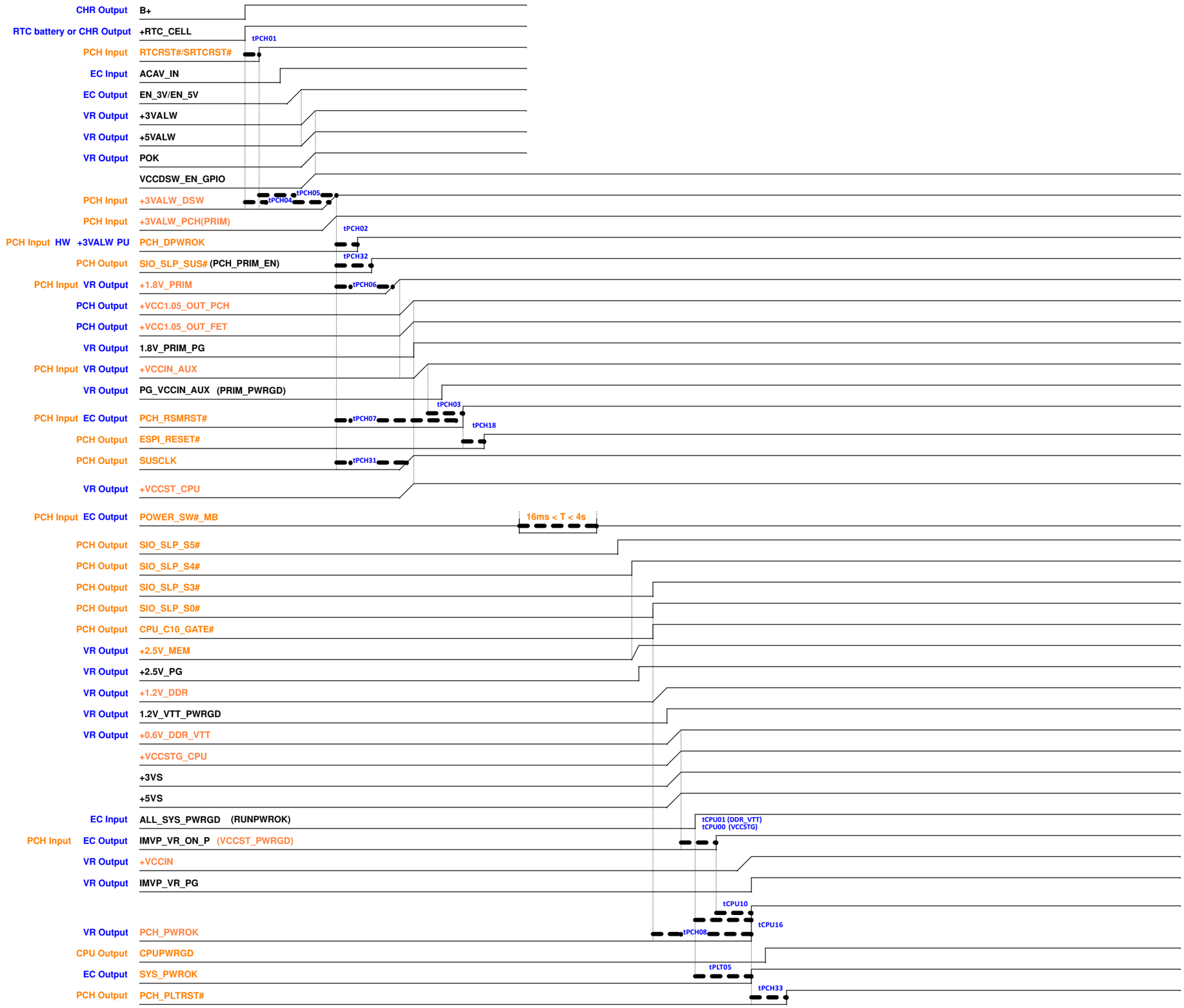
Power Up Sequence
G3 to S0



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Title: Platform Power Sequence			
Size	Document Number: LA-K033P		Rev: 1.0
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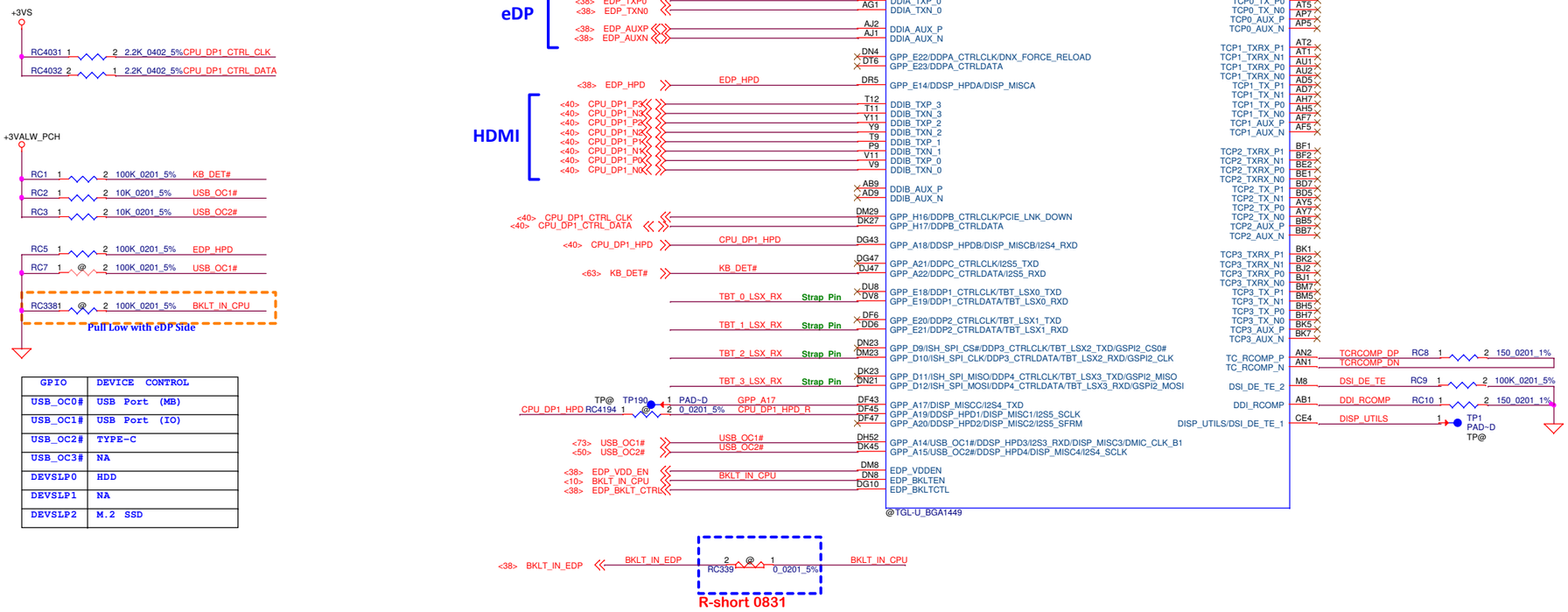

GPIO	DEVICE CONTROL
USB_OC0#	USB Port (MB)
USB_OC1#	USB Port (IO)
USB_OC2#	TYPE-C
USB_OC3#	NA
DEVSLP0	HDD
DEVSLP1	NA
DEVSLP2	M.2 SSD

TBT LSX #0 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

TBT LSX #1 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

TBT LSX #2 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

TBT LSX #3 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

PLACE CLOSE TO THE SIGNAL TO AVOID STUB

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Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Title: P006 - TGL-U(1/13)TCSS,EDP

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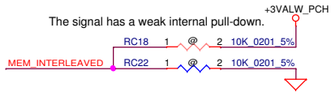
DIMM TYPE

1 : Interleave

0 : Non-Interleave

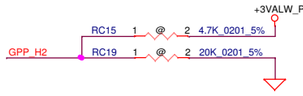
The signal has a weak internal pull-down.



BOOT STRAP 3

GPP_H2 (Weak internal PD 20K)

This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.



BOOT STRAP 2

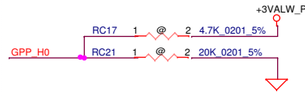
GPP_H1 (Weak internal PD 20K)

This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.

BOOT STRAP 1

GPP_H0 (Weak internal PD 20K)

This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.

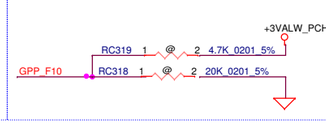


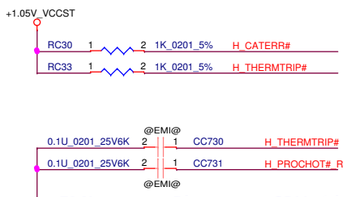
Reserved

GPP_F7 (Weak internal PD 20K)

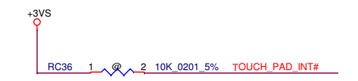
Reserved

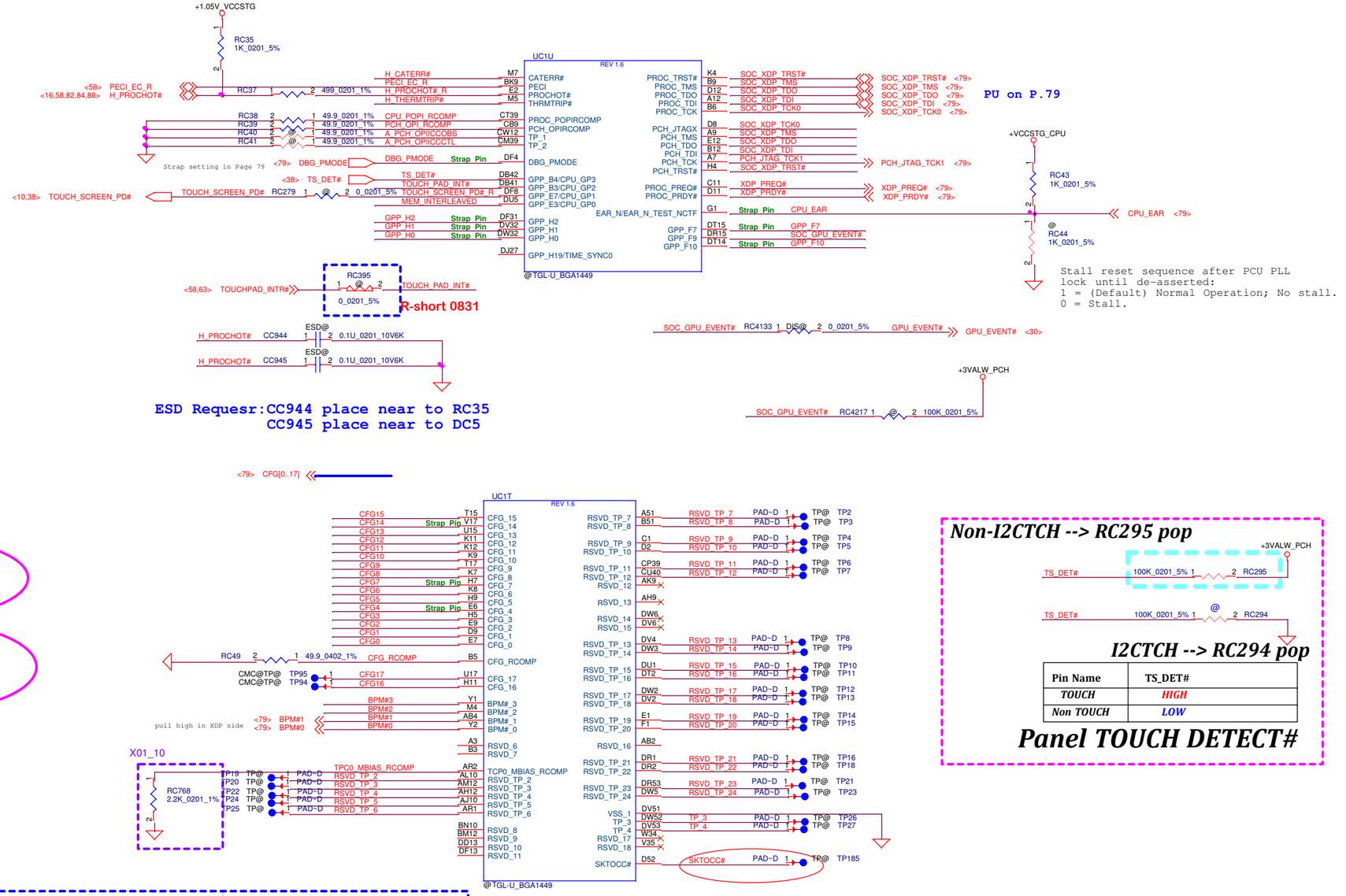
GPP_F10 (Weak internal PD 20K)



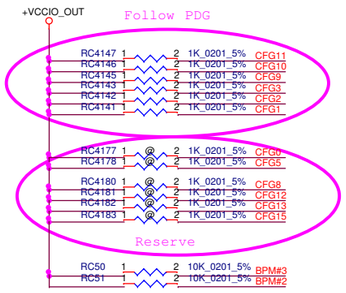


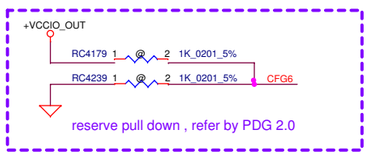
EMI request,Place near CPU side.

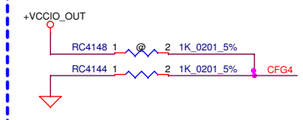




ESD Requesr:CC944 place near to RC35
CC945 place near to DC5



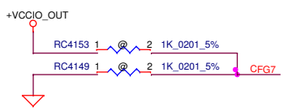




eDP enable strap

0 : enable

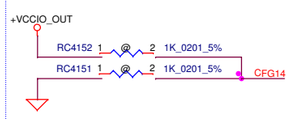
1 : disable



PEG Training

0 : PEG wait for BIOS training

1 : PEG tranin immediately following RESET# de-assertion
1 --> (default)



PEG60 Lane Reversal

0 : Reseved

1 : Normal
1 --> (default)

Non-I2CTCH --> RC295 pop

I2CTCH --> RC294 pop

Pin Name	TS_DET#
TOUCH	*HIGH*
Non TOUCH	*LOW*

Panel TOUCH DETECT#

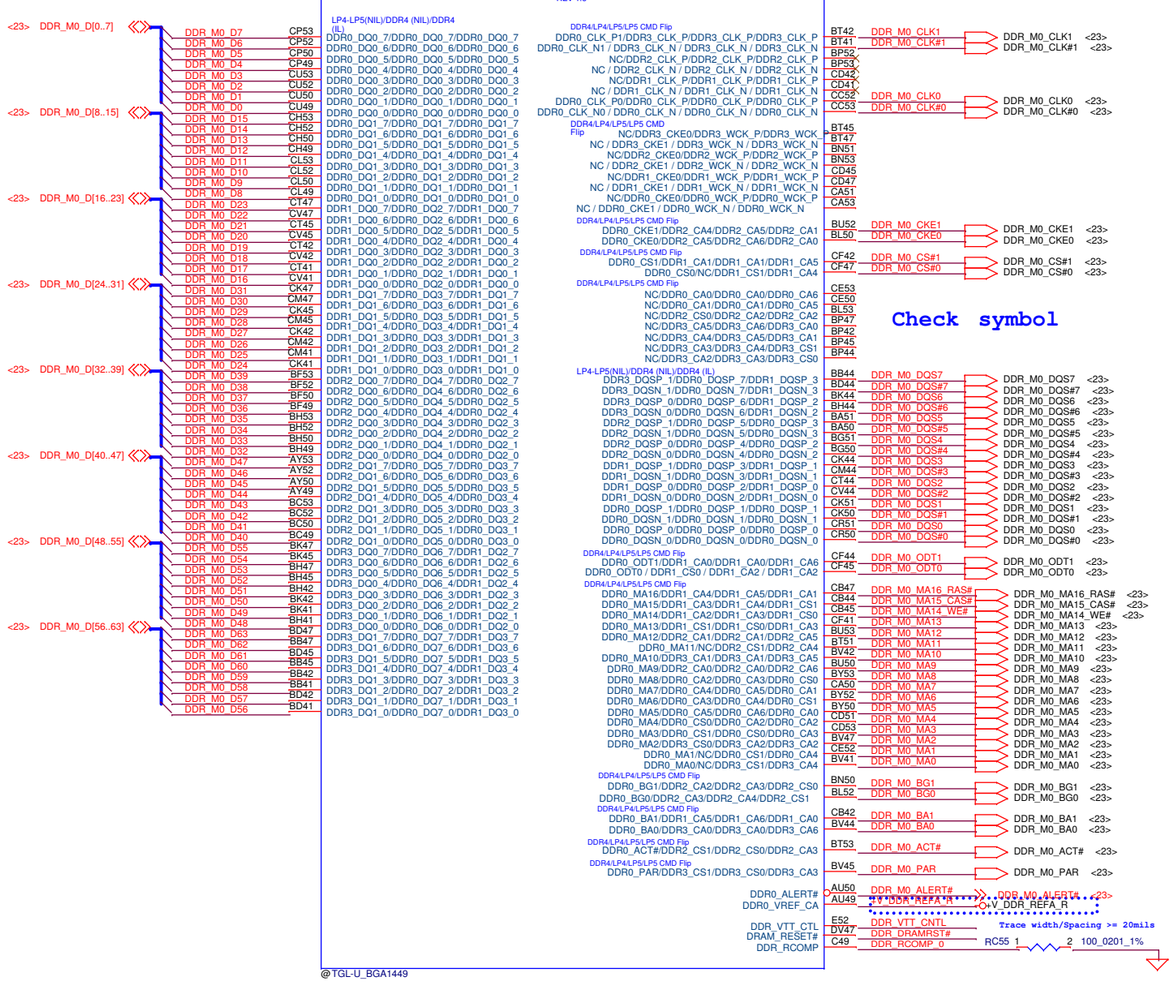
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

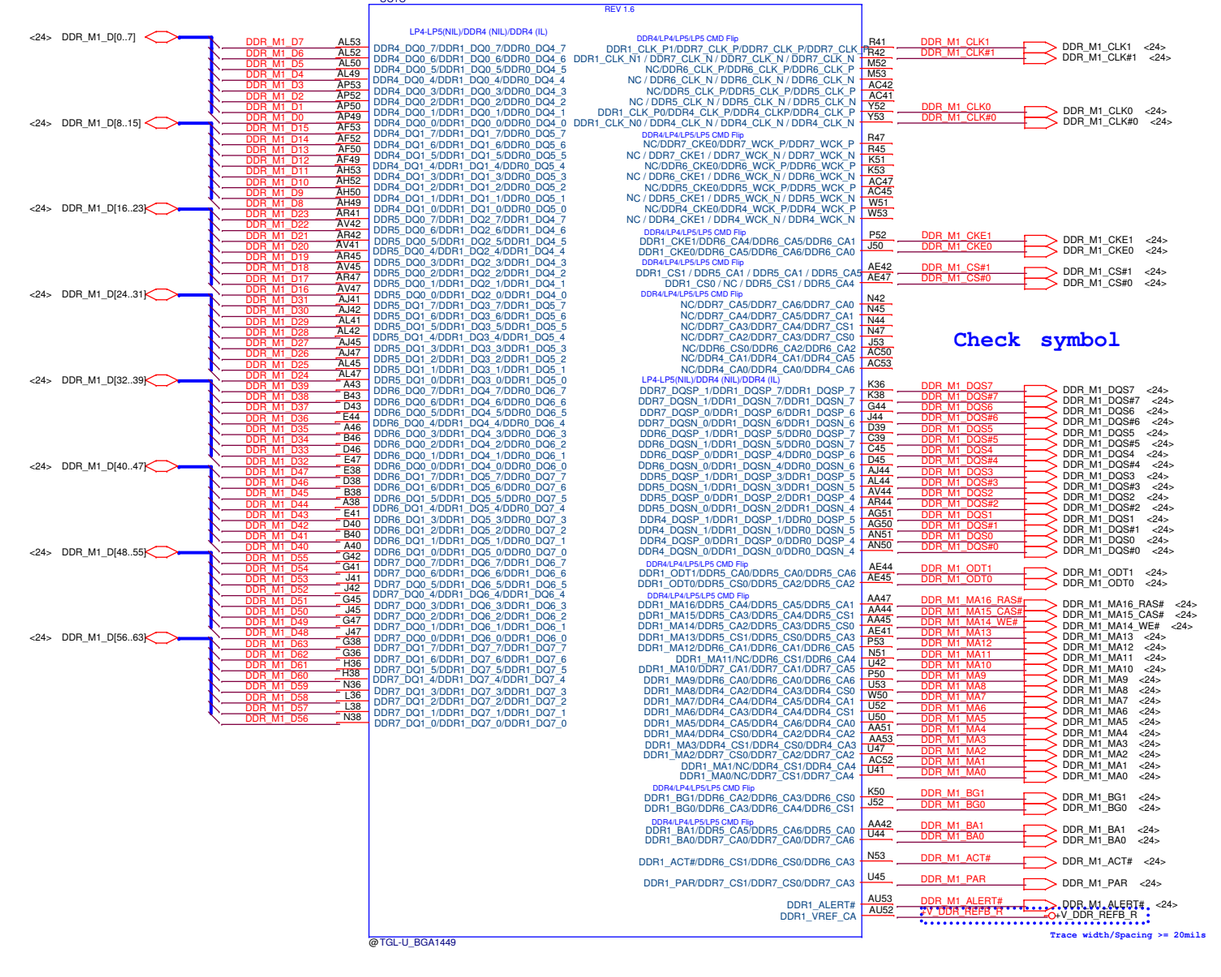
Compal Electronics, Inc.

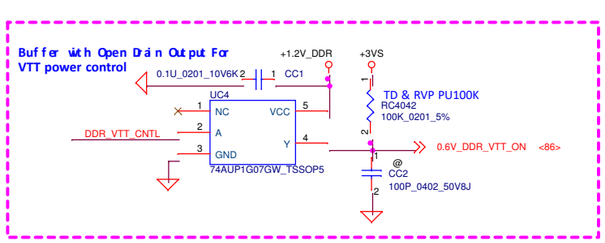
Title: ***P007 - TGL-U(2/13)MISC,MIPI60***

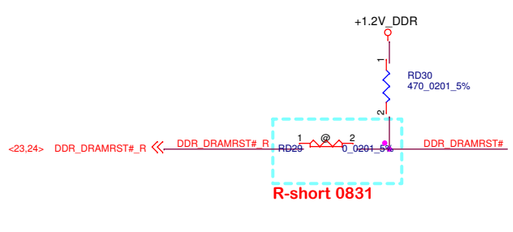
Size: | Document Number: ***LA-K033P*** | Rev: 1.0

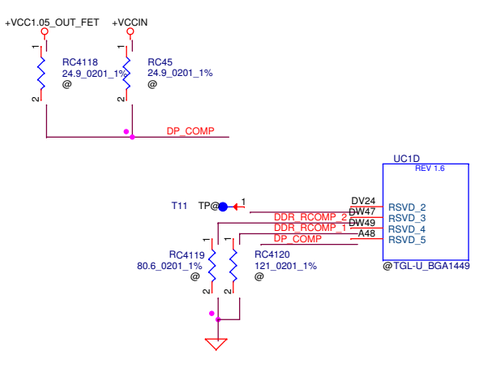
Date: Friday, September 11, 2020 | Sheet 7 of 100











Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: **P008 - TGL-U(3/13)LPDDR4/x**

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BOOT HALT

SPI0_MOSI(NO INTERNAL PU/PD)

0 = Enable

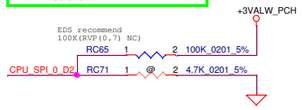
1 = Disable

CONSENT STRAP

SPI0_IO2(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

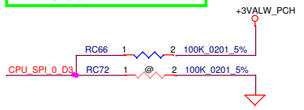


A0 PERSONALITY STRAP

SPI0_IO3

0 = Enable

1 = Disable



TLS CONFIDENTIALITY

GPP_C2 (Weak internal PD 20K)

0 = TLS CONFIDENTIALITY DISABLE

1 = TLS CONFIDENTIALITY ENABLE

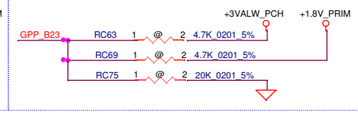
no need this security for CSME
(internal PD)

CPUNSSC CLOCK FREQ

GPP_B23 (Weak internal PD 20K)

0 = 38.4 MHz clock direct from crystal (default)

1 = 19.2 MHz clock from divider (Device from 38.4MHz crystal)

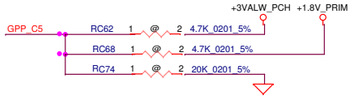


ESPI OR EC LESS

GPP_C5 (Weak internal PD 20K)

0 = Enable eSPI. (Default)

1 = Disable eSPI.



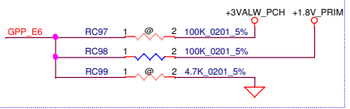
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).

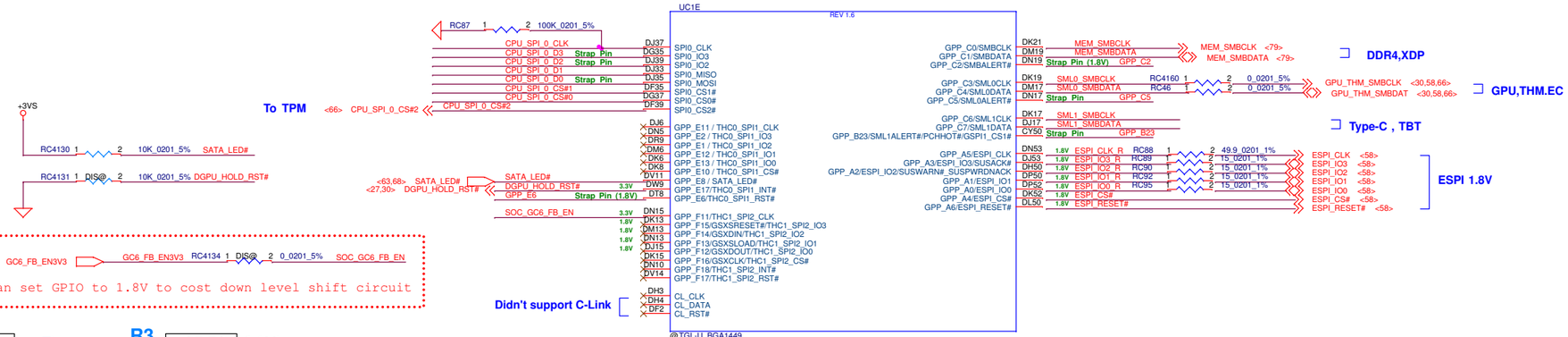
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). <--use this

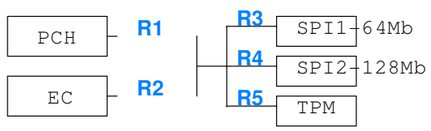
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI.
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved.

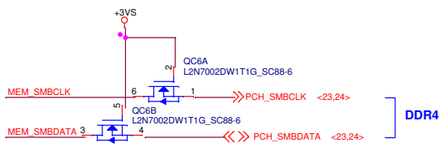
Reserved

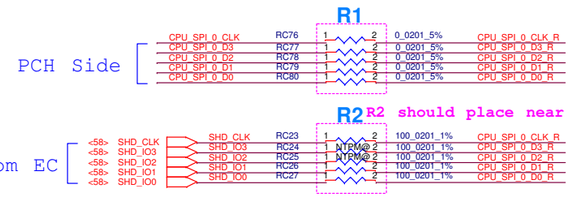
GPP_E6 (External pull-up is required)





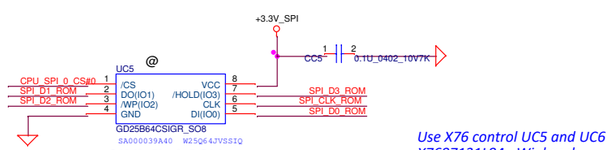


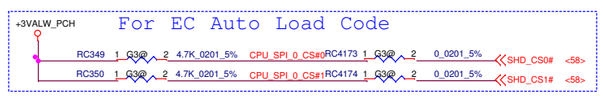




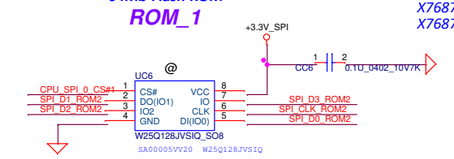
For 2 Flash + 1 TPM

R2	R3	R4
RC24 TPM@ 49.9_0201_1% SD00000TO00		
RC25 TPM@ 49.9_0201_1% SD00000TO00		

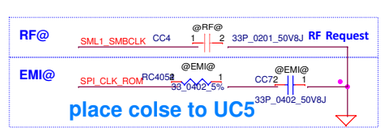




Use X76 control UC5 and UC6
X7687131L84 - Winbond
X7687131L85 - Gigadevice
X7687131L86 - XMC



FLASH ROM



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: P009 - TGL-U(4/13)SPI,SMB,ESPI

Size | Document Number: LA-K033P | Rev: 1.0

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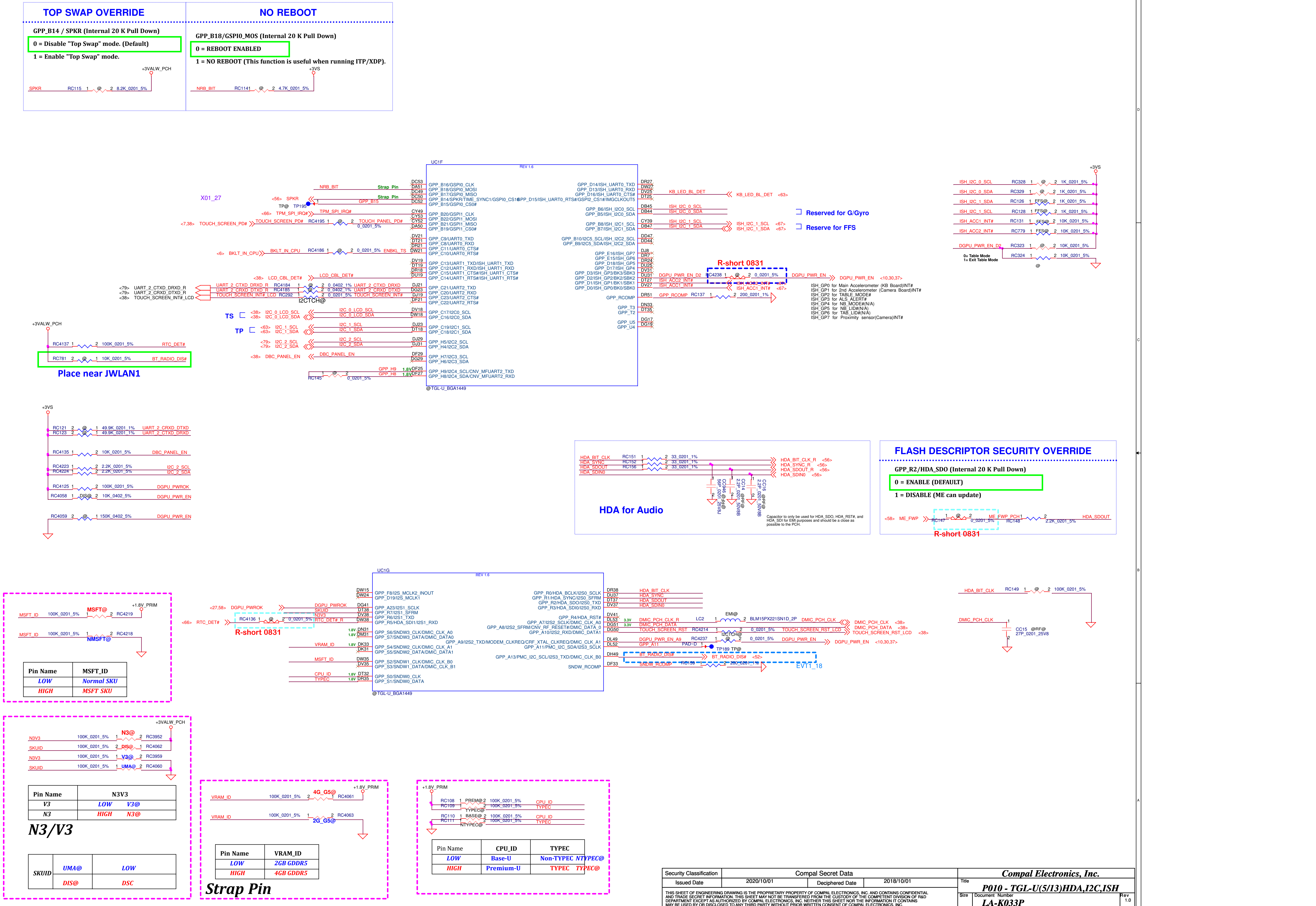

TOP SWAP OVERRIDE
GPP_B14 / SPKR (Internal 20 K Pull Down)
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.
+3VALW_PCH
SPKR RC115 1 @ 2 8.2K_0201_5%
NO REBOOT
GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)
0 = REBOOT ENABLED
1 = NO REBOOT (This function is useful when running ITP/XDP).
+3VS
NRB_BIT RC1141 @ 2 4.7K_0201_5%
UC1F
REV 1.6
X01_27
NRB_BIT Strap_Pin
<56> SPKR Strap_Pin
TP@ TP195 GPP_B15
<66> TPM_SPI_IRQ# TPM_SPI_IRQ#
<7,38> TOUCH_SCREEN_PD# TOUCH_SCREEN_PD# RC4195 1 @ 2 TOUCH_PANEL_PD# 0_0201_5%
<6> BKLT_IN_CPU BKLT_IN_CPU RC4186 1 @ 2 0_0201_5% ENBKL_TS
<38> LCD_CBL_DET# LCD_CBL_DET#
<79> UART_2_CTXD_DRXD_R
<79> UART_2_CRXD_DTXD_R
<38> TOUCH_SCREEN_INT#_LCD
UART_2_CTXD_DRXD_R RC4184 1 @ 2 0_0402_1% UART_2_CTXD_DRXD
UART_2_CRXD_DTXD_R RC4185 1 @ 2 0_0402_1% UART_2_CRXD_DTXD
TOUCH_SCREEN_INT#_LCD RC292 1 2 0_0201_5% TOUCH_SCREEN_INT#
I2CTCH@
TS <38> I2C_0_LCD_SCL <38> I2C_0_LCD_SDA
TP <63> I2C_1_SCL <63> I2C_1_SDA
<79> I2C_2_SCL <79> I2C_2_SDA
<38> DBC_PANEL_EN DBC_PANEL_EN
GPP_H9 1.8V GPP_H8 1.8V RC145 1 @ 2 0_0201_5%
GPP_B16/GSPI0_CLK
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
GPP_B15/GSPI0_CS0#
GPP_B20/GSPI1_CLK
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B19/GSPI1_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_H5/I2C2_SCL
GPP_H4/I2C2_SDA
GPP_H7/I2C3_SCL
GPP_H6/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD
@TGL-U_BGA1449
GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5
GPP_B6/ISH_I2C0_SCL
GPP_B5/ISH_I2C0_SDA
GPP_B8/ISH_I2C1_SCL
GPP_B7/ISH_I2C1_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_E16/ISH_GP7
GPP_E15/ISH_GP6
GPP_D18/ISH_GP5
GPP_D17/ISH_GP4
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCOMP
GPP_T3
GPP_T2
GPP_U5
GPP_U4
KB_LED_BL_DET KB_LED_BL_DET <63>
ISH_I2C_0_SCL ISH_I2C_0_SDA
Reserved for G/Gyro
ISH_I2C_1_SCL ISH_I2C_1_SDA ISH_I2C_1_SCL <67> ISH_I2C_1_SDA <67>
Reserve for FFS
R-short 0831
DGPU_PWR_EN_D2 RC4238 1 @ 2 0_0201_5% DGPU_PWR_EN DGPU_PWR_EN <10,30,37>
ISH_ACC2_INT# ISH_ACC1_INT# ISH_ACC2_INT# <67> ISH_ACC1_INT# <67>
GPP_RCOMP RC137 1 2 200_0201_1%
ISH_GP0 for Main Accelerometer (KB Board)INT#
ISH_GP1 for 2nd Accelerometer (Camera Board)INT#
ISH_GP2 for TABLE_MODE#
ISH_GP3 for ALS_ALERT#
ISH_GP4 for NB_MODE#(N/A)
ISH_GP5 for NB_LID#(N/A)
ISH_GP6 for TAB_LID#(N/A)
ISH_GP7 for Proximity sensor(Camera)INT#
+3VS
ISH_I2C_0_SCL RC328 1 @ 2 1K_0201_5%
ISH_I2C_0_SDA RC329 1 @ 2 1K_0201_5%
ISH_I2C_1_SDA RC126 1 FFS@ 2 1K_0201_5%
ISH_I2C_1_SCL RC128 1 FFS@ 2 1K_0201_5%
ISH_ACC1_INT# RC131 1 FFS@ 2 10K_0201_5%
ISH_ACC2_INT# RC779 1 FFS@ 2 10K_0201_5%
DGPU_PWR_EN_D2 RC323 1 @ 2 10K_0201_5%
0= Table Mode
1= Exit Table Mode
RC324 1 2 10K_0201_5% @
+3VALW_PCH
RC4137 1 2 100K_0201_5% RTC_DET#
RC781 2 @ 1 10K_0201_5% BT_RADIO_DIS#
Place near JWLAN1
+3VS
RC121 2 @ 1 49.9K_0201_1% UART_2_CRXD_DTXD
RC123 2 @ 1 49.9K_0201_1% UART_2_CTXD_DRXD
RC4135 1 2 10K_0201_5% DBC_PANEL_EN
RC4223 1 2 2.2K_0201_5% I2C_2_SCL
RC4224 1 2 2.2K_0201_5% I2C_2_SDA
RC4125 1 2 100K_0201_5% DGPU_PWROK
RC4058 1 DIS@ 2 10K_0402_5% DGPU_PWR_EN
RC4059 2 @ 1 150K_0402_5% DGPU_PWR_EN
HDA_BIT_CLK RC151 1 2 33_0201_1% HDA_BIT_CLK_R <56>
HDA_SYNC RC152 1 2 33_0201_1% HDA_SYNC_R <56>
HDA_SDOUT RC156 1 2 33_0201_1% HDA_SDOUT_R <56>
HDA_SDIN0 HDA_SDIN0 <56>
CC946 @RF@ 56P_0201_25V8J
CC14 @RF@ 2.2P_0201_50V8B
CC16 @RF@ 2.2P_0201_50V8B
HDA for Audio
Capacitor to only be used for HDA_SDO, HDA_RST#, and HDA_SDI for EMI purposes and should be a close as possible to the PCH.
FLASH DESCRIPTOR SECURITY OVERRIDE
GPP_R2/HDA_SDO (Internal 20 K Pull Down)
0 = ENABLE (DEFAULT)
1 = DISABLE (ME can update)
<58> ME_FWP RC147 1 @ 2 0_0201_5% ME_FWP_PCH 1 RC148 2 2.2K_0201_5% HDA_SDOUT
R-short 0831
UC1G
REV 1.6
<27,58> DGPU_PWROK DGPU_PWROK
SKUID
N3V3
<66> RTC_DET# RC4136 1 @ 2 0_0201_5% RTC_DET#_R
R-short 0831
VRAM_ID
MSFT_ID
CPU_ID
TYPEC
GPP_F8/I2S_MCLK2_INOUT
GPP_D19/I2S_MCLK1
GPP_A23/I2S1_SCLK
GPP_R7/I2S1_SFRM
GPP_R6/I2S1_TXD
GPP_R5/HDA_SDI1/I2S1_RXD
GPP_S6/SNDW3_CLK/DMIC_CLK_A0
GPP_S7/SNDW3_DATA/DMIC_DATA0
GPP_S4/SNDW2_CLK/DMIC_CLK_A1
GPP_S5/SNDW2_DATA/DMIC_DATA1
GPP_S2/SNDW1_CLK/DMIC_CLK_B0
GPP_S3/SNDW1_DATA/DMIC_CLK_B1
GPP_S0/SNDW0_CLK
GPP_S1/SNDW0_DATA
@TGL-U_BGA1449
GPP_R0/HDA_BCLK/I2S0_SCLK
GPP_R1/HDA_SYNC/I2S0_SFRM
GPP_R2/HDA_SDO/I2S0_TXD
GPP_R3/HDA_SDI0/I2S0_RXD
GPP_R4/HDA_RST#
GPP_A7/I2S2_SCLK/DMIC_CLK_A0
GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
GPP_A10/I2S2_RXD/DMIC_DATA1
GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
GPP_A11/PMC_I2C_SDA/I2S3_SCLK
GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0
SNDW_RCOMP
HDA_BIT_CLK HDA_SYNC HDA_SDOUT HDA_SDIN0
DMIC_PCH_CLK_R LC2 EMI@ 1 2 BLM15PX221SN1D_2P DMIC_PCH_CLK DMIC_PCH_CLK <38>
DMIC_PCH_DATA DMIC_PCH_DATA <38>
TOUCH_SCREEN_RST RC4214 1 I2CTCH@ 2 0_0201_5% TOUCH_SCREEN_RST_LCD TOUCH_SCREEN_RST_LCD <38>
DGPU_PWR_EN_A9 RC4237 1 @ 2 0_0201_5% DGPU_PWR_EN DGPU_PWR_EN <10,30,37>
GPP_A11 PAD~D TP189 TP@
BT_RADIO_DIS# BT_RADIO_DIS# <52>
SNDW_RCOMP RC159 1 2 200_0201_1%
EVT1_18
HDA_BIT_CLK RC149 1 @ 2 100K_0201_5%
DMIC_PCH_CLK CC15 @RF@ 27P_0201_25V8
+1.8V_PRIM
MSFT_ID 100K_0201_5% MSFT@ RC4219
MSFT_ID 100K_0201_5% NMSFT@ RC4218
+3VALW_PCH
N3V3 100K_0201_5% N3@ RC3952
SKUID 100K_0201_5% DIS@ RC4062
N3V3 100K_0201_5% V3@ RC3959
SKUID 100K_0201_5% UMA@ RC4060
N3/V3
+1.8V_PRIM
VRAM_ID 100K_0201_5% 4G_G5@ RC4061
VRAM_ID 100K_0201_5% 2G_G5@ RC4063
Strap Pin
+1.8V_PRIM
RC108 PREM@ 100K_0201_5% CPU_ID
RC109 TYPEC@ 100K_0201_5% TYPEC
RC110 BASE@ 100K_0201_5% CPU_ID
RC111 NTYPEC@ 100K_0201_5% TYPEC

Pin Name	MSFT_ID
LOW	Normal SKU
HIGH	MSFT SKU

Pin Name	N3V3	
V3	LOW	V3@
N3	HIGH	N3@

SKUID		
SKUID	UMA@	LOW
	DIS@	DSC

Pin Name	VRAM_ID
LOW	2GB GDDR5
HIGH	4GB GDDR5

Pin Name	CPU_ID	TYPEC
LOW	Base-U	Non-TYPEC NTYPEC@
HIGH	Premium-U	TYPEC TYPEC@

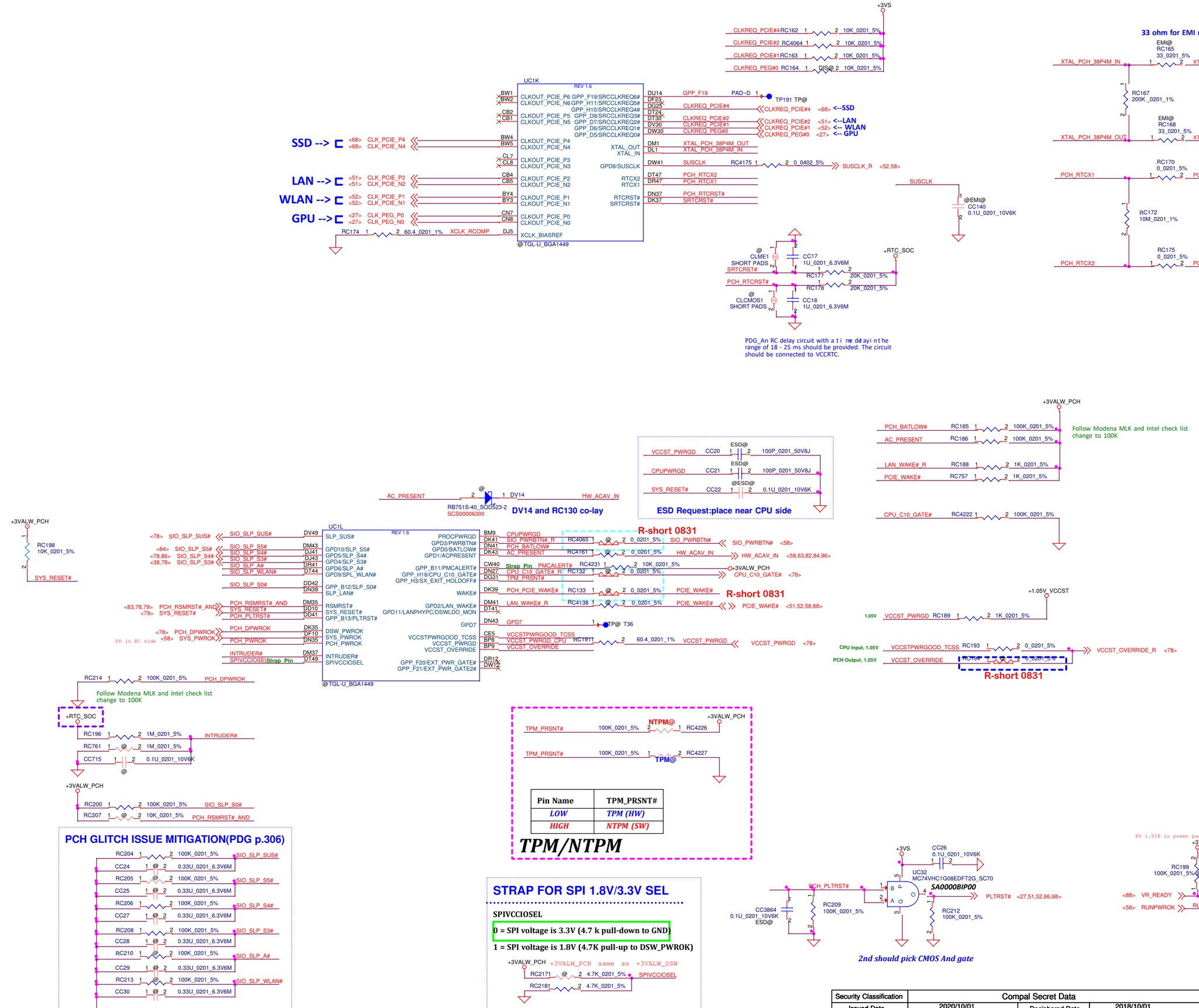
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

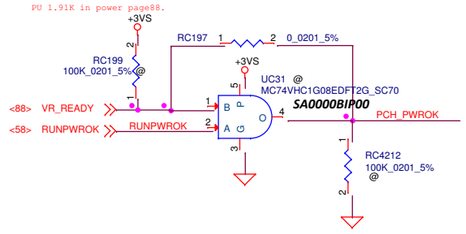
Compal Electronics, Inc.

Title: **P010 - TGL-U(5/13)HDA,I2C,ISH**

Size | Document Number: **LA-K033P** | Rev 1.0

Date: Friday, September 11, 2020 | Sheet 10 of 100





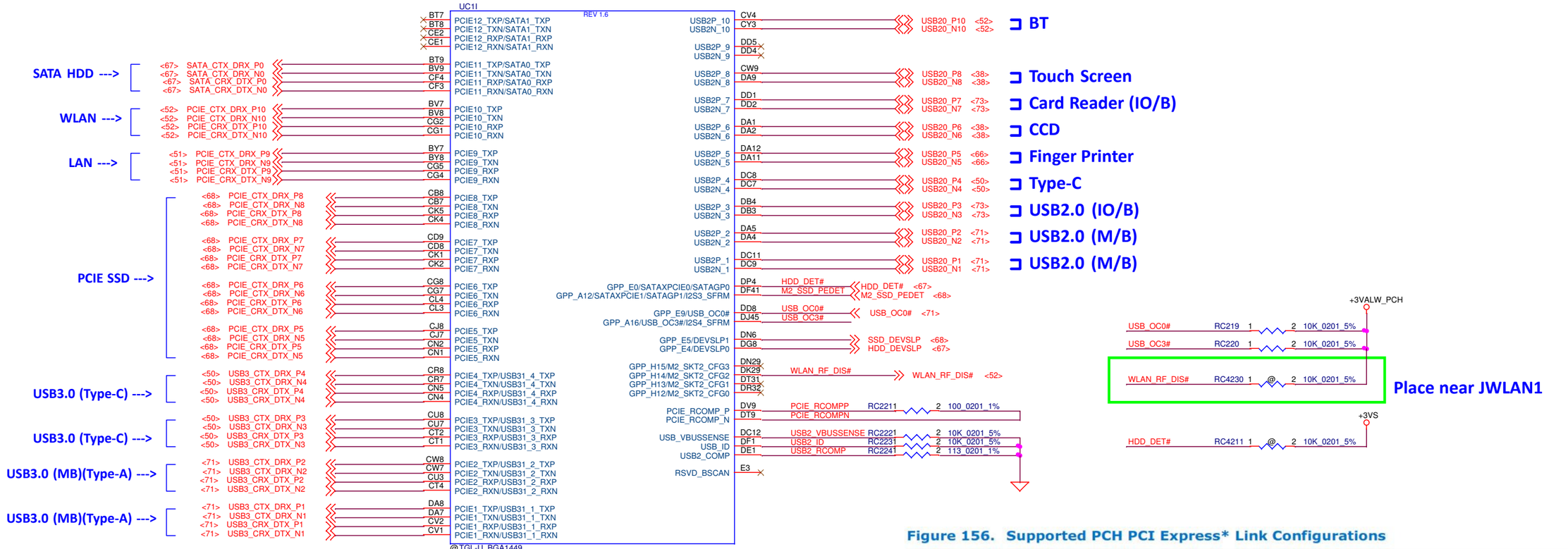
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: P011 - TGL-U(6/13)CLK,GPIO

Size: | Document Number: LA-K033P | Rev: 1.0

Date: Friday, September 11, 2020 | Sheet 11 of 100



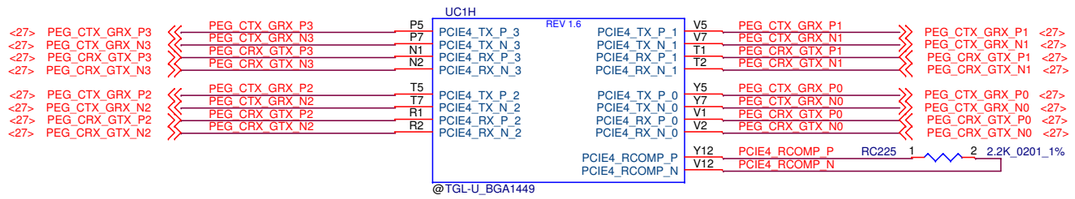


Figure 156. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lanes		0	1	2	3	4	5	6	7	8	9	10	11
PCIe* Lanes		1	2	3	4	5	6	7	8	9	10	11	12
Link Lanes	1x4	0	1	2	3	0	1	2	3	0	1	2	3
	1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0
	2x2	0	1	0	1	0	1	0	1	0	1	0	1
	1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0
	2x1+1x2	0	0	1	0	0	0	1	0	0	0	1	0
	4x1	0	0	0	0	0	0	0	0	0	0	0	0
Base-U	1x4					RP5				RP9			
	1x4 LR					RP5				RP9			
	2x2					RP5		RP7		RP9		RP11	
	1x2+2x1					RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2					RP8	RP7	RP5		RP12	RP11	RP9	
	4x1					RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-Y	1x4	RP1								RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3				RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4			RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4			RP7	RP8	RP9	RP10	RP11	RP12

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.	
Title	P012 - TGL-U(7/13)PCIE,USB
Size	Document Number: LA-K033P
Rev	1.0
Date:	Friday, September 11, 2020
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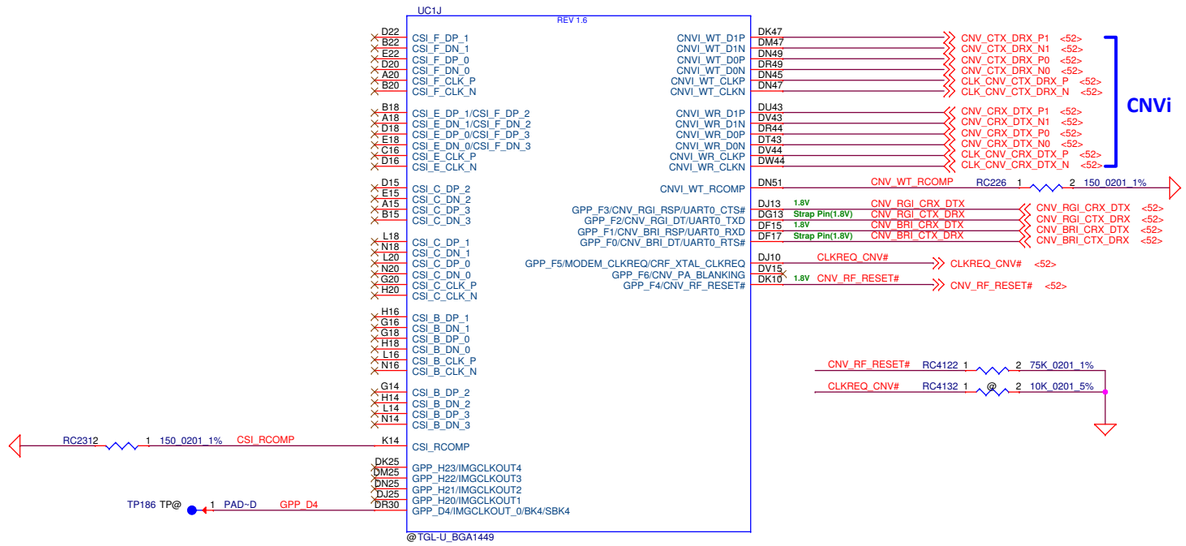
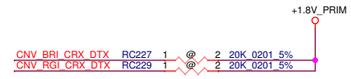
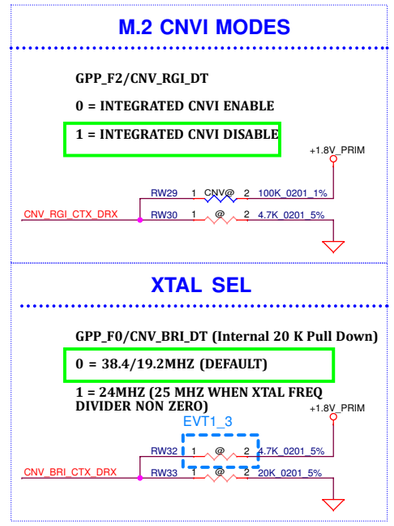






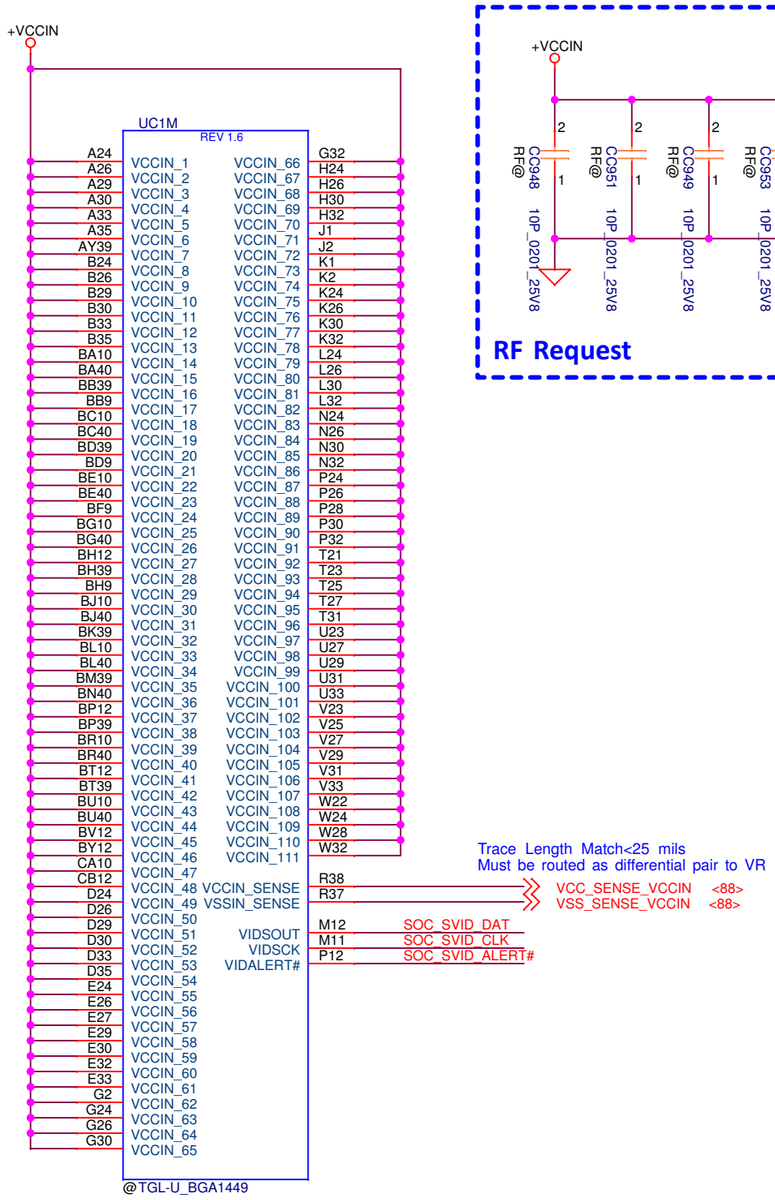
Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

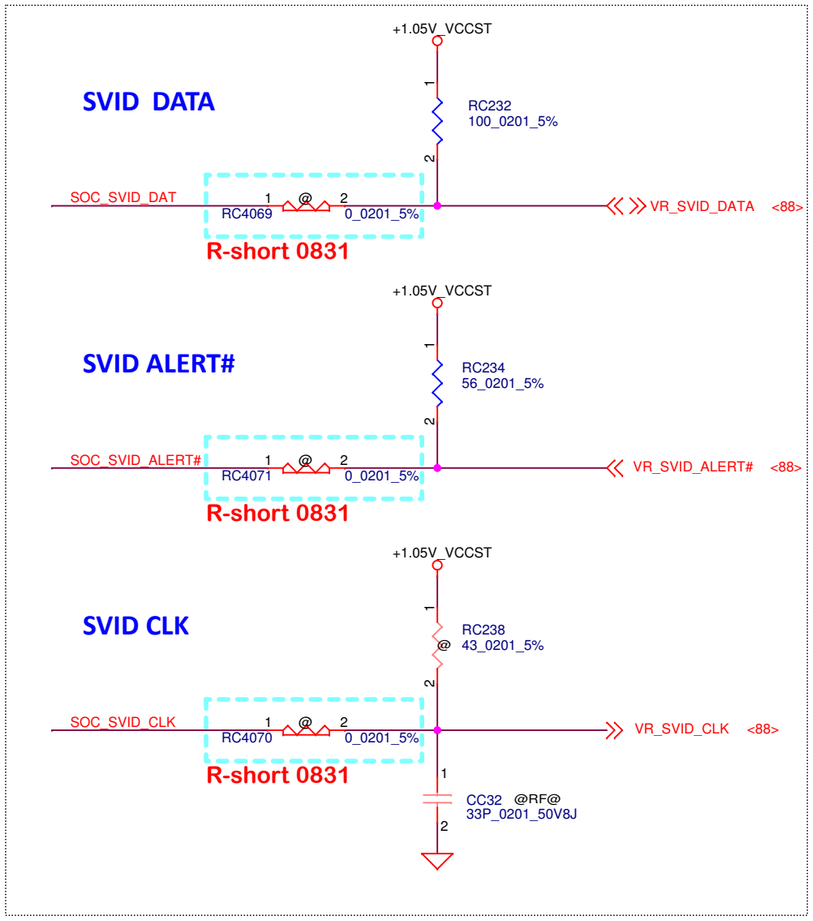
Title: P013 - TGL-U(8/13)CSI,CNVi

Size | Document Number: LA-K033P | Rev: 1.0

Date: Friday, September 11, 2020 | Sheet 13 of 100

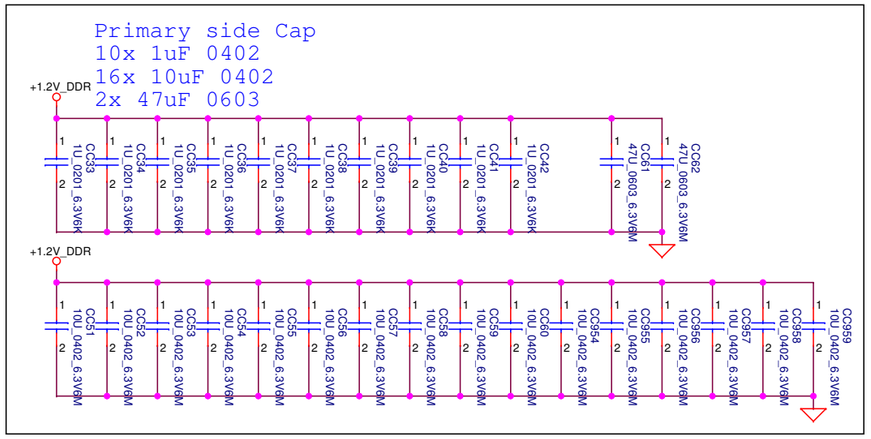


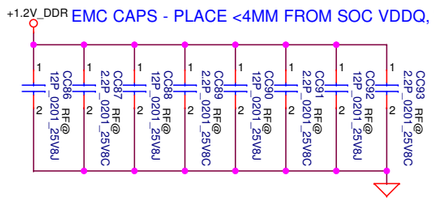
1.The total Length of Data and Clock (from CPU to each VR) must be equal (± 0 1i nch).
2.Route the Alert signal between the Clock and the Data signals.
CAD Note: Place the PU resistors close to CPU

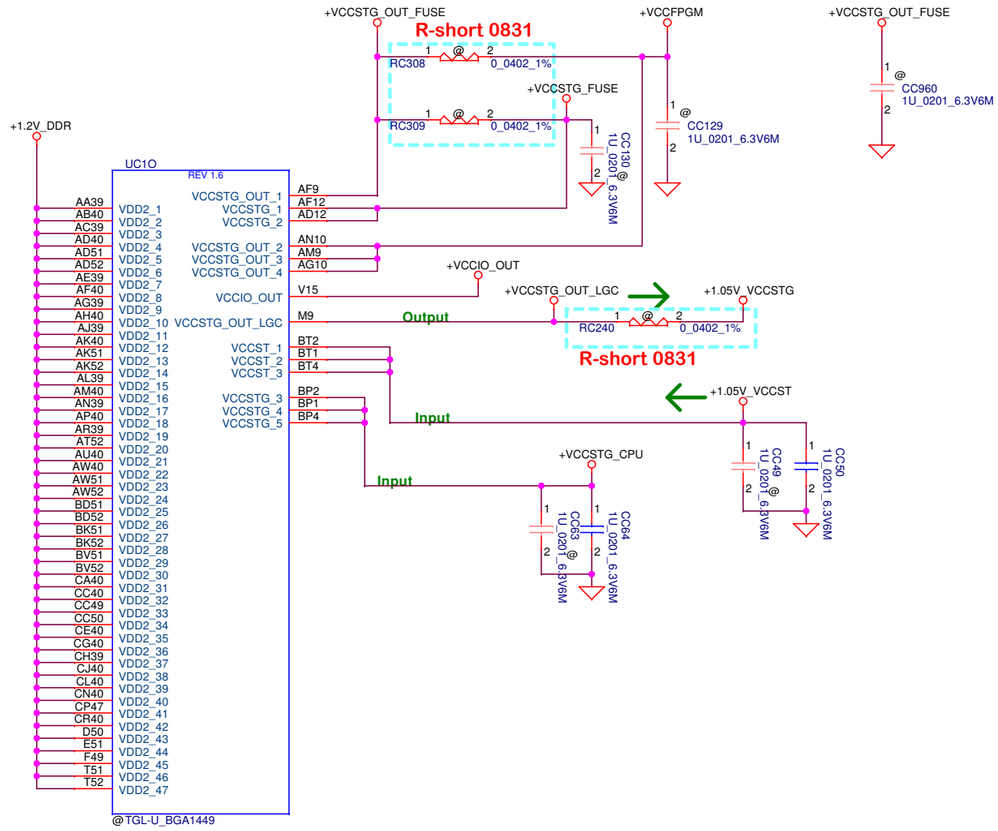


Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.			
Title: P014 - TGL-U(9/13)CPU PWR,SVID			
Size	Document Number: LA-K033P		Rev: 1.0
Date: Friday, September 11, 2020	Sheet 14 of 100		

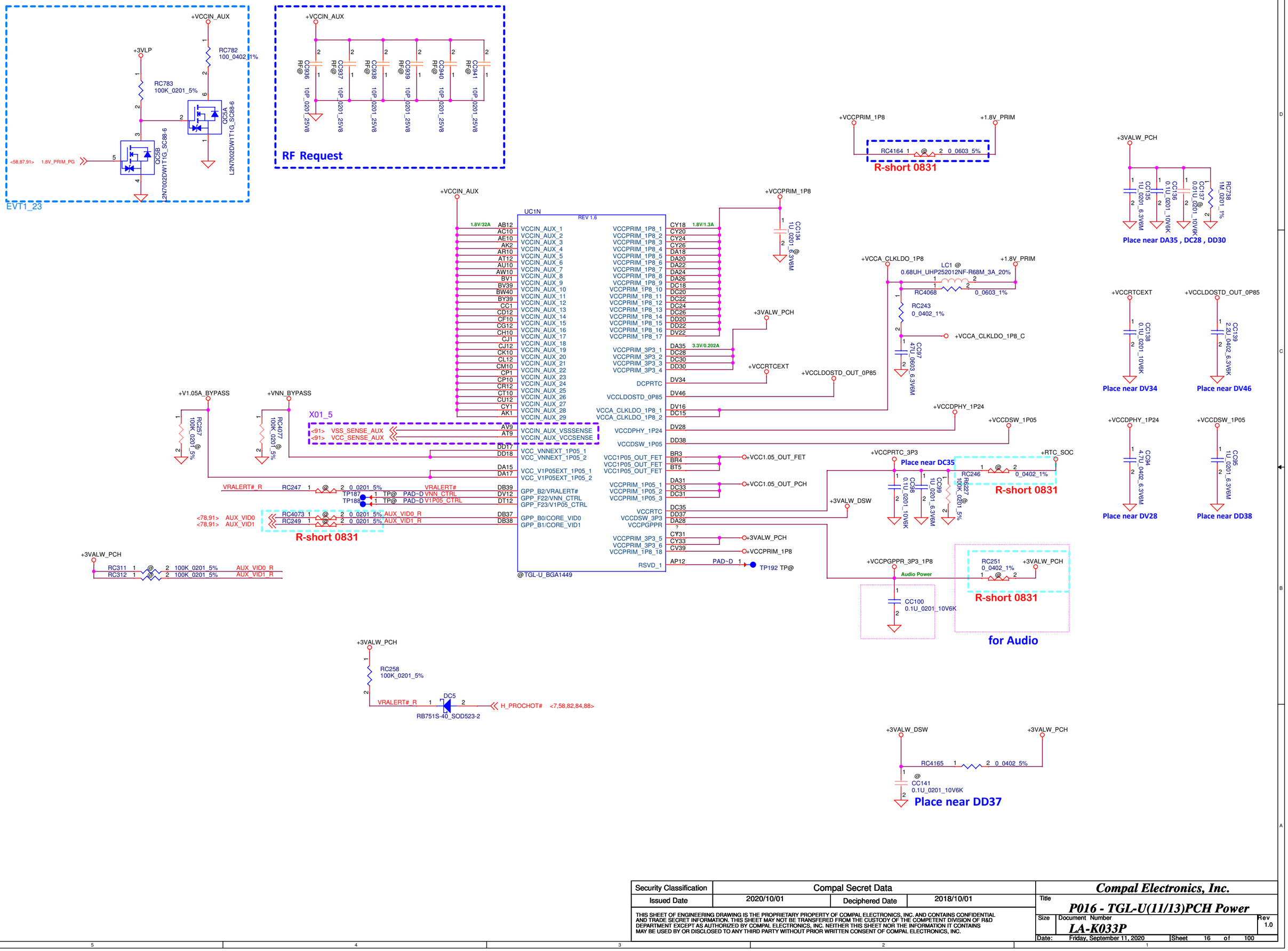






Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.			
Title	P015 - TGL-U(10/13)CPU PWR		
Size	Document Number LA-K033P		Rev 1.0
Date: Friday, September 11, 2020	Sheet 15 of 100		



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.	
Title	P016 - TGL-U(11/13)PCH Power
Size	Document Number: LA-K033P
Rev	1.0
Date:	Friday, September 11, 2020
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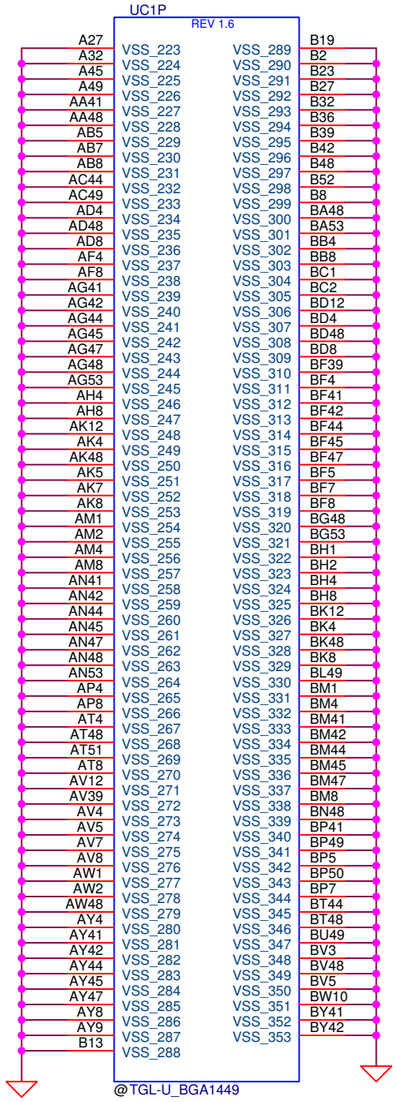
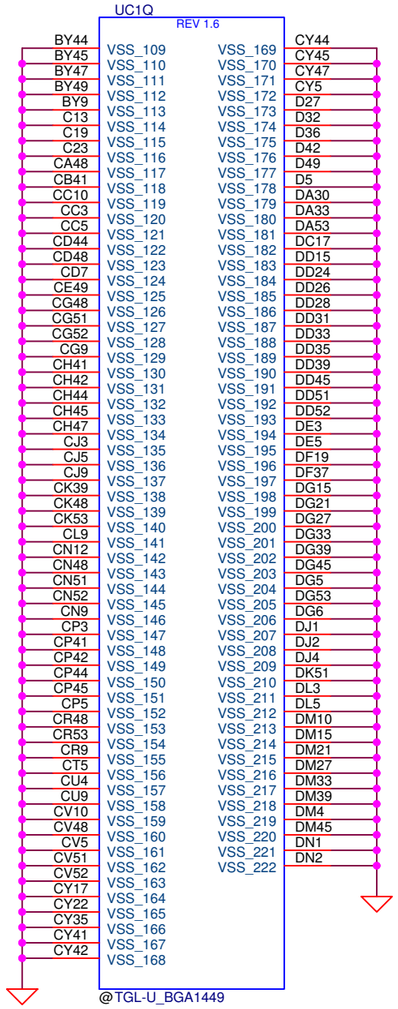
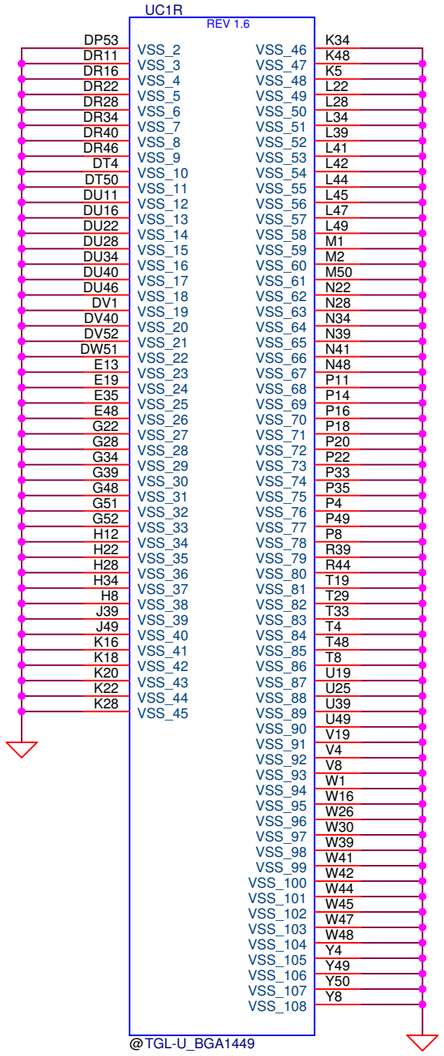




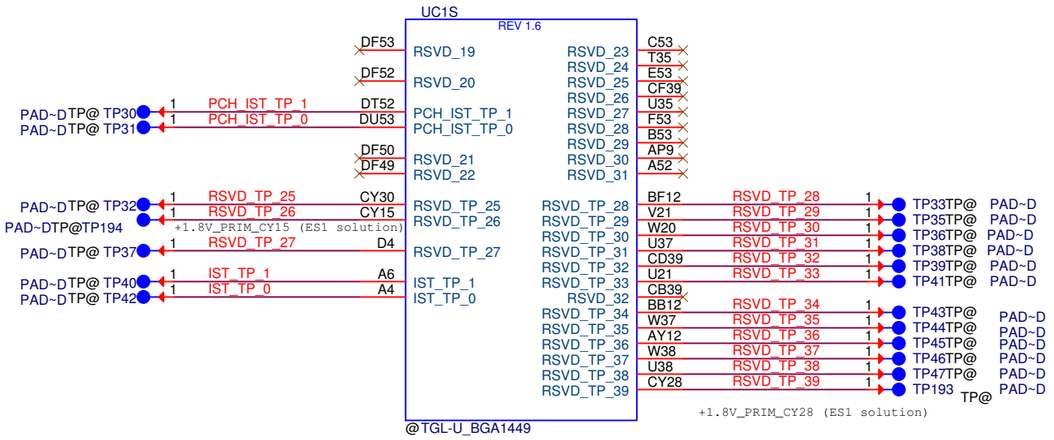


Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: **P017 - TGL-U(12/13)GND**

Size	Document Number	Rev
	LA-K033P	1.0
Date: Friday, September 11, 2020	Sheet 17 of 100	



ES1 Workaround Circuit
Intel Document Number: 614056

Compal Electronics, Inc.		
Title: *P018 - TGL-U(13/13)RSVD*		
Size	Document Number: *LA-K033P*	Rev: 1.0
Date: Friday, September 11, 2020	Sheet 18 of 100	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: (RSVD)		
Size	Document Number: LA-K033P	Rev: 1.0
Date: Friday, September 11, 2020	Sheet 19 of 101	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **(RSVD)**

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 20 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: ***(RSVD)***

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 21 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: ***(RSVD)***

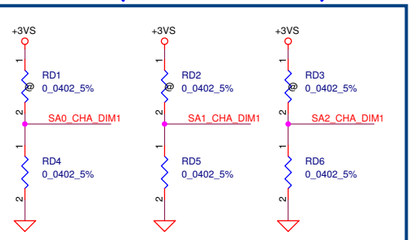
Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 22 of 101

Main Func = DDR4(1/2)

CHANNEL-M0

BOT: DIMM1(JDIMM2 CONN)Non-ECC DIMM

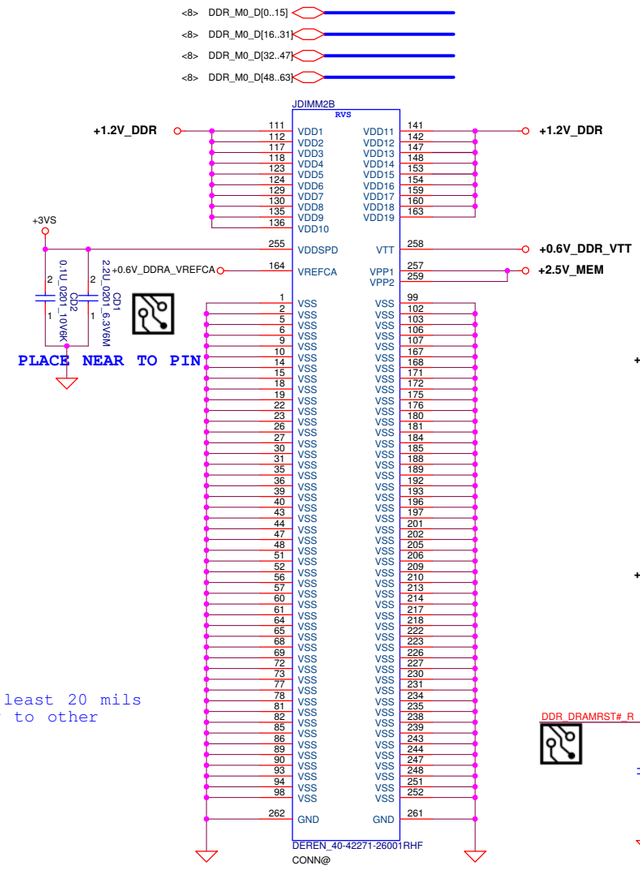


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

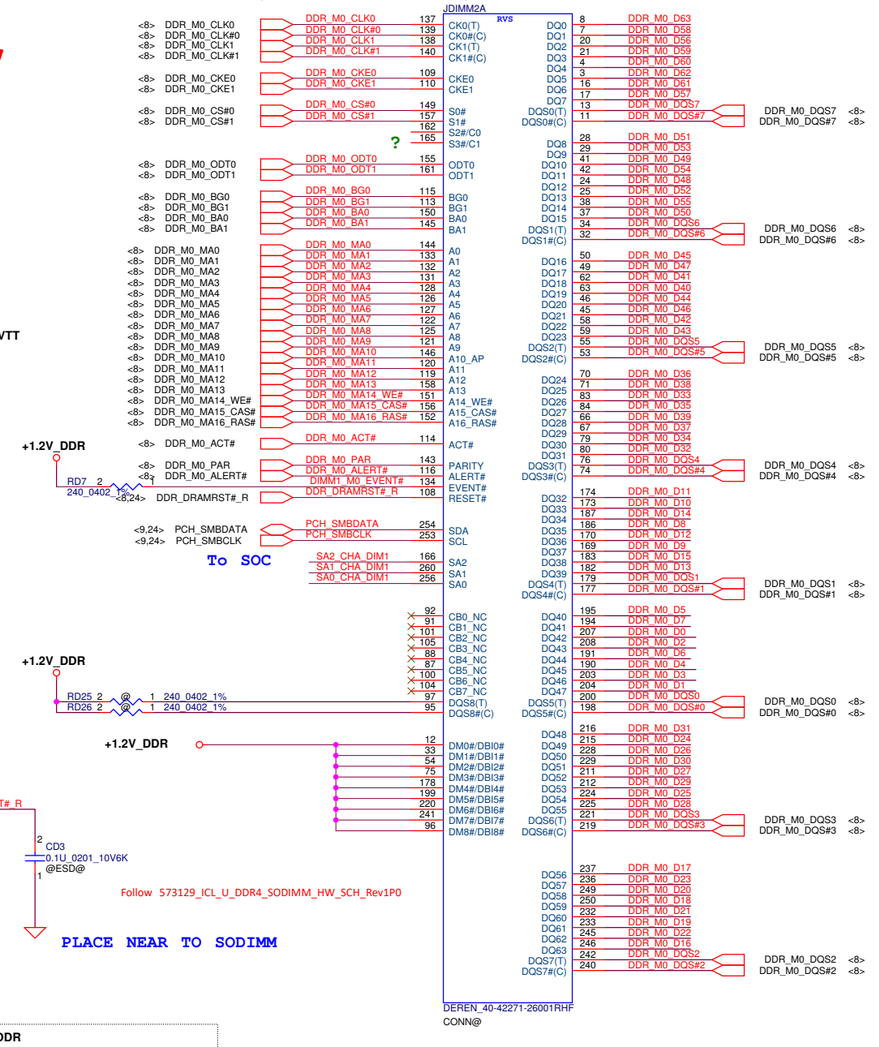
SPD ADDRESS FOR CHANNEL A :

SA0 = 0; SA1 = 0; SA2 = 0.

Non-Interleaved Memory



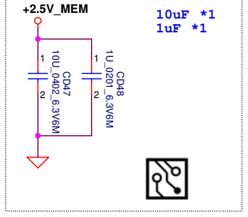
REVERSE TYPE (5.2 mm)



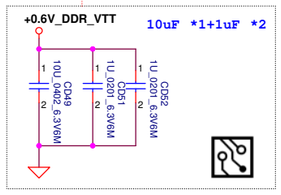
Part Number:SP07001JH00
Part Value:S SOCKET LOTES ADDR0208-P001A 260P DDR4

Decopling Cap._Channel A

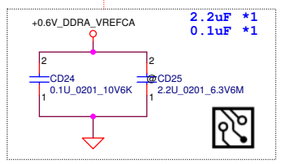
Layout Note:
Place near JDIMM2.257,259



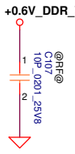
Layout Note:
Place near JDIMM2.258



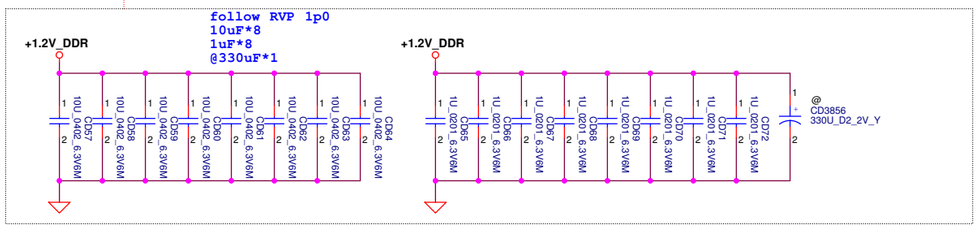
Layout Note:
PLACE THE CAP near JDIMM2. 164

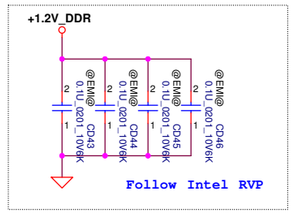


C107 place near JDIMM2

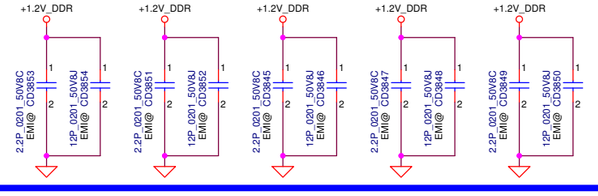


Layout Note:
Place near JDIMM2





EMC CAPS-PLACE
< 4mm from SO-DIMM VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



POP
EMI@
UNPOP
@EMI@\@ESD@\@RF@\CONN@\@

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: DDR4_CHM0: DIMM0

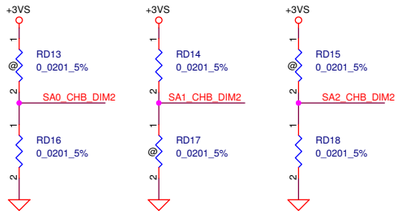
Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 Sheet 23 of 101

Main Func = DDR4(2/2)

CHANNEL-M1

BOT: DIMM2(JDIMM1 CONN)Non-ECC DIMM

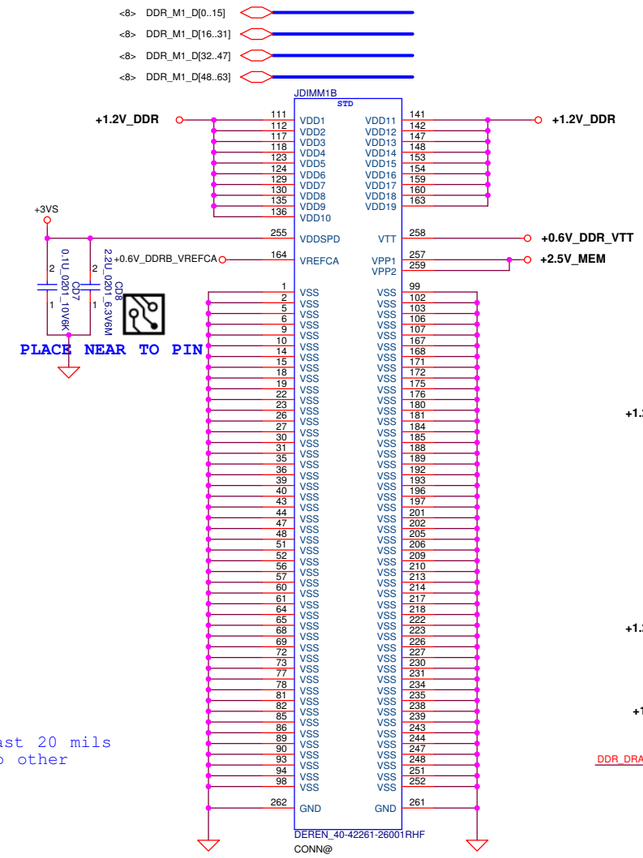


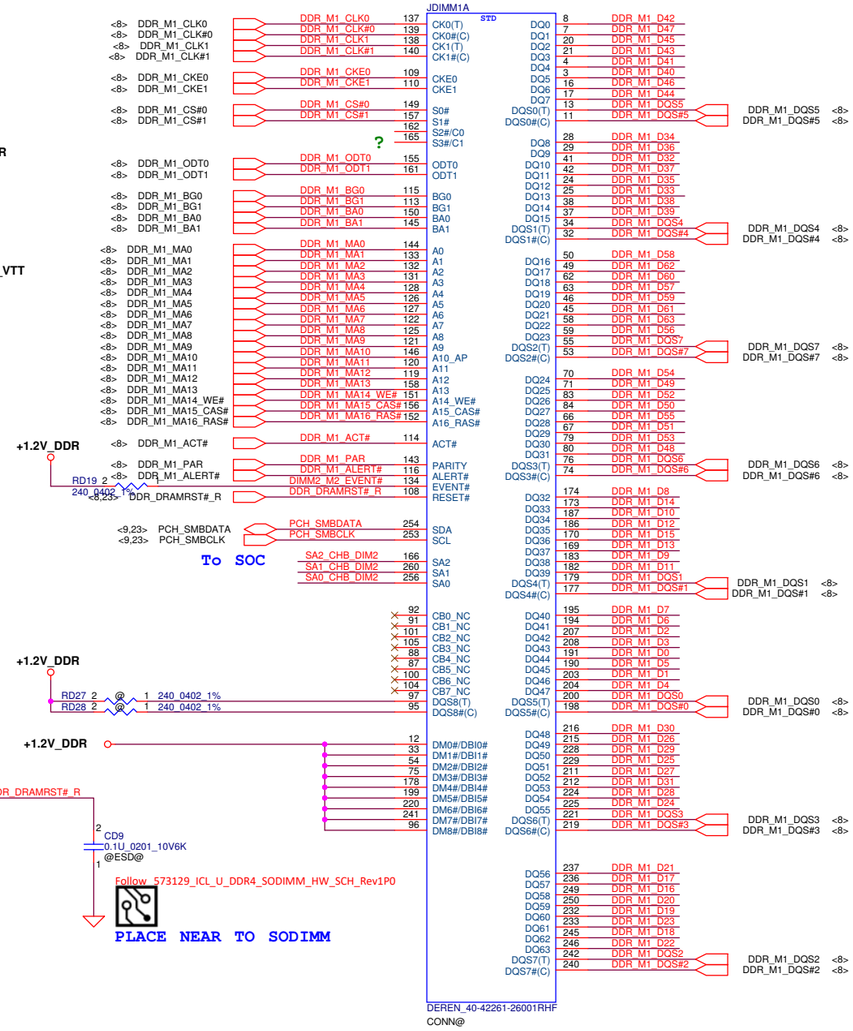
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :

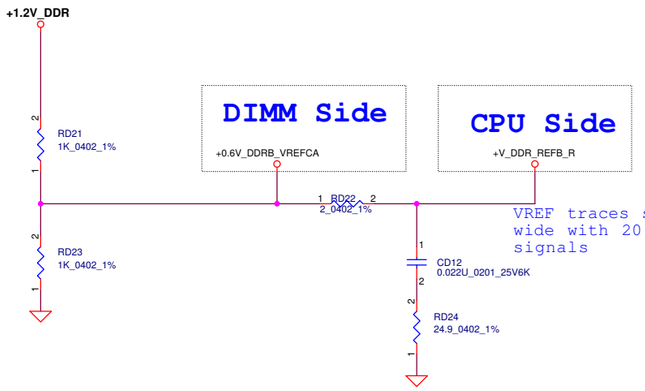
SA0 = 0; SA1 = 1; SA2 = 0.

Non-Interleaved Memory

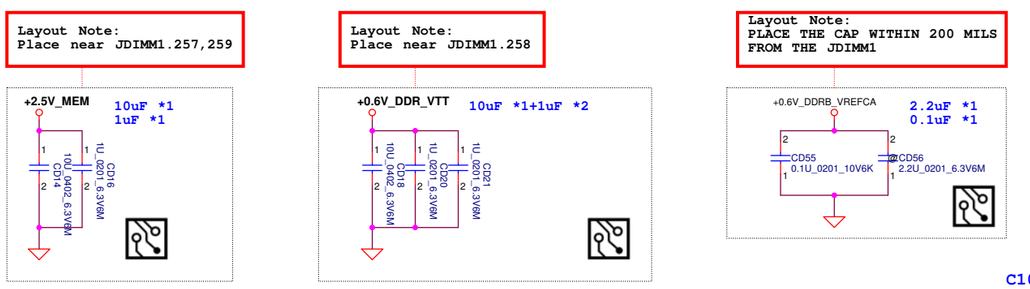


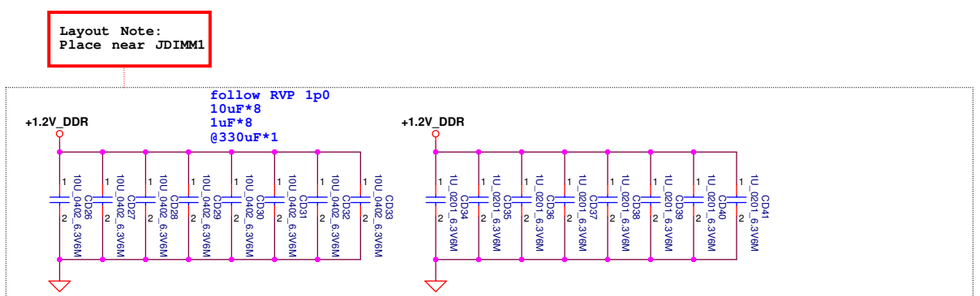


Part Number:SP07001HY00
Part Value:S SOCKET LOTES ADDR0207-P001A 260P DDR4

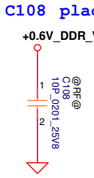


Decoupling Cap._Channel B





C108 place near JDIMM1



08/30
Update Table 4-26 for DDR4 SO-DIMM Decoupling Caps
572907_ICL_UY_PDG_Rev0p7 Page.99

Table 4-26. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)
		Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

Compal Electronics, Inc.

Title: DDR4 CHM1: DIMM1

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 Sheet 24 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **(RSVD)**

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 25 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	(RSVD)		
Size	Document Number LA-K033P		Rev 1.0
Date: Friday, September 11, 2020	Sheet 26 of 101		

Main Func = GPU

PCIE X4 Bus

<12> PEG_CRX_GTX_N[0..3] → PEG_CRX_GTX_N[0..3]
<12> PEG_CRX_GTX_P[0..3] → PEG_CRX_GTX_P[0..3]
<12> PEG_CTX_GRX_N[0..3] → PEG_CTX_GRX_N[0..3]
<12> PEG_CTX_GRX_P[0..3] → PEG_CTX_GRX_P[0..3]

PCIE CLK

<11> CLKREQ_PEG#0 → CLKREQ_PEG#0
<11> CLK_PEG_P0 → CLK_PEG_P0
<11> CLK_PEG_N0 → CLK_PEG_N0

<11,51,52,66,68> PLTRST# → PLTRST#
<9,30> DGPU_HOLD_RST# → DGPU_HOLD_RST#

<30> PLT_RST_VGA# → PLT_RST_VGA#

<30,66,85> T_CRIT# → T_CRIT#
<9,31> GC6_FB_EN3V3 → GC6_FB_EN3V3

<30,37> DGPU_MAIN_EN → DGPU_MAIN_EN

<92> GPU_CORE_PG → GPU_CORE_PG
<37,94> +1.35VGS_PGOOD → +1.35VGS_PGOOD

<10,58> DGPU_PWROK → DGPU_PWROK

GPIO
Pull High with CPU Side

Reset Control

1.8V AND GATE

+1.8VS_DGPU_AON
UV12
PLTRST# 1
(From PCH)
DGPU_HOLD_RST# 2
IN B, IN A, VCC, GND, OUT Y 4
PLT_RST_VGA#
RV378 @ 100K_0201_5%
NL17SZ08EDFT2G SOT-353
DIS@
SA0000BJI00

+3VS
RV4996 DIS@ 100K_0201_5%
+1.8VS_DGPU_AON
RV4998 DIS@ 10K_0201_5%
CV757 DIS@ 0.1U_0201_6.3V6K
UV26
T_CRIT# DV12 DIS@ RB751S-40_SOD523-2 SCS00006300
T_CRIT# D DV11 DIS@ RB751S-40_SOD523-2 SCS00006300
DGPU_MAIN_EN
PLT_RST_VGA# 1
+1.8VS_DGPU_AON_UV26 2
IN B, IN A, VCC, GND, OUT Y
PLT_RST_VGA# UV26 4
NL17SZ08EDFT2G SOT-353 DIS@ SA0000BJI00
QV150A 5
PJT138KA 2N SOT363-6 DIS@ SB000016K00
+3VS
RV4997 @ 10K_0201_5%
Pull High with PWR Side
GC6_FB_EN3V3 2
QV150B DIS@ PJT138KA 2N SOT363-6 SB000016K00
GPU_CORE_PG

+3VS
GPU_CORE_PG 1
+1.35VGS_PGOOD 2
UV11
B, A, VCC, GND, Y 4
DGPU_PWROK
MC74VHC1G09DFT2G_SC70-5 DIS@
Open Drain
Pull High with CPU Side

CLK_REQ

+1.8VS_DGPU_AON
RV68 DIS@ 10K_0201_5%
DGPU_PWROK
RV5001 0_0201_5%
CLKREQ_PEG#0_R
QV3 BSS138W 1N SOT-323-3 DIS@
CLKREQ_PEG#0 (To SOC)
VGS(Max) : 1.2 V

UV1A COMMON

1/14 PCI_EXPRESS

PLT_RST_VGA#				+1.8V_AON	AC7	PEX_RST#		
CLKREQ_PEG#0_R				+1.8V_AON	AC6	PEX_CLKREQ#		
CLK_PEG_P0					AE8	PEX_REFCLK		
CLK_PEG_N0					AD8	PEX_REFCLK#		
PEG_CRX_GTX_P0	CV11	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_P0	AC9	PEX_TX0		
PEG_CRX_GTX_N0	CV12	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_N0	AB9	PEX_TX0#		
PEG_CTX_GRX_P0	CV1	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_P0	AG6	PEX_RX0		
PEG_CTX_GRX_N0	CV6	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_N0	AG7	PEX_RX0#		
PEG_CRX_GTX_P1	CV13	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_P1	AB10	PEX_TX1		
PEG_CRX_GTX_N1	CV14	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_N1	AC10	PEX_TX1#		
PEG_CTX_GRX_P1	CV7	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_P1	AF7	PEX_RX1		
PEG_CTX_GRX_N1	CV8	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_N1	AE7	PEX_RX1#		
PEG_CRX_GTX_P2	CV15	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_P2	AD11	PEX_TX2		
PEG_CRX_GTX_N2	CV16	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_N2	AC11	PEX_TX2#		
PEG_CTX_GRX_P2	CV19	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_P2	AE9	PEX_RX2		
PEG_CTX_GRX_N2	CV20	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_N2	AF9	PEX_RX2#		
PEG_CRX_GTX_P3	CV17	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_P3	AC12	PEX_TX3		
PEG_CRX_GTX_N3	CV18	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CRX_C_GTX_N3	AB12	PEX_TX3#		
PEG_CTX_GRX_P3	CV21	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_P3	AG9	PEX_RX3		
PEG_CTX_GRX_N3	CV22	DIS@ 1	2 0.22U_0201_6.3V6M	PEG_CTX_C_GRX_N3	AG10	PEX_RX3#		

AB6 PEX_WAKE#

AB13 PEX_TX4
AC13 PEX_TX4#
AF10 PEX_RX4
AE10 PEX_RX4#
AD14 PEX_TX5
AC14 PEX_TX5#
AE12 PEX_RX5
AF12 PEX_RX5#
AC15 PEX_TX6
AB15 PEX_TX6#
AG12 PEX_RX6
AG13 PEX_RX6#
AB16 PEX_TX7
AC16 PEX_TX7#
AF13 PEX_RX7
AE13 PEX_RX7#
AD17 PEX_TX8
AC17 PEX_TX8#
AE15 PEX_RX8
AF15 PEX_RX8#
AC18 PEX_TX9
AB18 PEX_TX9#
AG15 PEX_RX9
AG16 PEX_RX9#
AB19 PEX_TX10
AC19 PEX_TX10#
AF16 PEX_RX10
AE16 PEX_RX10#
AD20 PEX_TX11
AC20 PEX_TX11#
AE18 PEX_RX11
AF18 PEX_RX11#
AC21 PEX_TX12
AB21 PEX_TX12#
AG18 PEX_RX12
AG19 PEX_RX12#
AD23 PEX_TX13
AE23 PEX_TX13#
AF19 PEX_RX13
AE19 PEX_RX13#
AF24 PEX_TX14
AE24 PEX_TX14#
AE21 PEX_RX14
AF21 PEX_RX14#
AG24 PEX_TX15
AG25 PEX_TX15#
AG21 PEX_RX15
AG22 PEX_RX15#

NC FOR GM108

NC FOR GF117/GK208/GM108

N17S-G2-A1_FCBGA_595P
@

PEX_IOVDD AA22, AB23, AC24, AD25, AE26, AE27

Place near balls AA22 AE27
CV202 DIS@ 1U_0201_6.3V6M
CV222 DIS@ 1U_0201_6.3V6M
CV205 DIS@ 4.7U_0402_6.3V6M
Place near BGA
CV2 DIS@ 4.7U_0402_6.3V6M
CV393 DIS@ 4.7U_0402_6.3V6M
Midway GPU & VR
CV199 DIS@ 10U_0603_6.3V6M
CV204 DIS@ 10U_0603_6.3V6M
CV9 DIS@ 22U_0603_6.3V6M
CV767 DISRF@ 100P_0201_25V8J
CV768 DISRF@ 0.1U_0201_6.3V6K
CV931 DISRF@ 10P_0201_25V8
+1.0VS_DGPU

PEX_IOVDDQ AA10, AA12, AA13, AA16, AA18, AA19, AA20, AA21, AB22, AC23, AD24, AE25, AF26, AF27

Place near balls AA10 AA16 AB22 AF27
CV201 DIS@ 1U_0201_6.3V6M
CV200 DIS@ 1U_0201_6.3V6M
CV390 DIS@ 1U_0201_6.3V6M
CV391 DIS@ 1U_0201_6.3V6M
Place near BGA
+PEX_IOVDDQ
CV392 DIS@ 4.7U_0402_6.3V6M
CV3 DIS@ 4.7U_0402_6.3V6M
Midway GPU & VR
CV198 DIS@ 10U_0402_6.3V6M
CV203 DIS@ 10U_0402_6.3V6M
CV10 DIS@ 22U_0603_6.3V6M
CV770 DISRF@ 100P_0201_25V8J
CV769 DISRF@ 0.1U_0201_6.3V6K
RV4970 1 DIS@ 2 0_0402_5%
+1.8VS_DGPU_MAIN

NC FOR GF119

PEX_PLL_HVDD AA8, AA9
+PEX_PLL_HVDD
RV4976 1 DIS@ 2 0_0402_5%
+1.8VS_DGPU_MAIN
CV207 DIS@ 0.1U_0201_6.3V6K
Place near ball

PEX_SVDD_3V3 AB8

VDD_SENSE F2 VDD_SENSE_GPU → VDD_SENSE_GPU <92>
GND_SENSE F1 GND_SENSE_GPU → GND_SENSE_GPU <92>
To POWER
trace width: 16mils
differential voltage sensing.
differential signal routing.

PEX_TSTCLK_OUT AF22
PEX_TSTCLK_OUT# AE22

PEX_PLLVDD AA14
PEX_PLLVDD AA15

TESTMODE AD9 GPU_TESTMODE → GPU_TESTMODE <30>

PEX_TERMP AF25 PEX_TERMP
RV376 DIS@ 2.49K_0201_1%

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	

UV1
SA0000D2G1L
N17S_G3_R3@
S IC N17S-G3-A1 BGA 595P GPU A31 !

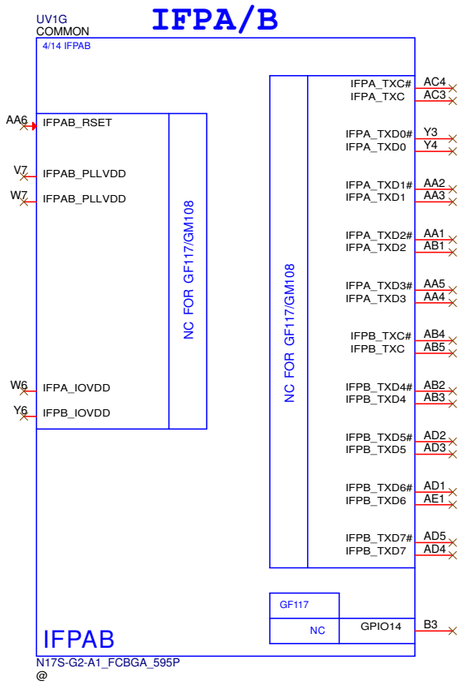
UV1
SA0000D2G0L
N17S_G3_R1@
S IC N17S-G3-A1 BGA 595P GPU

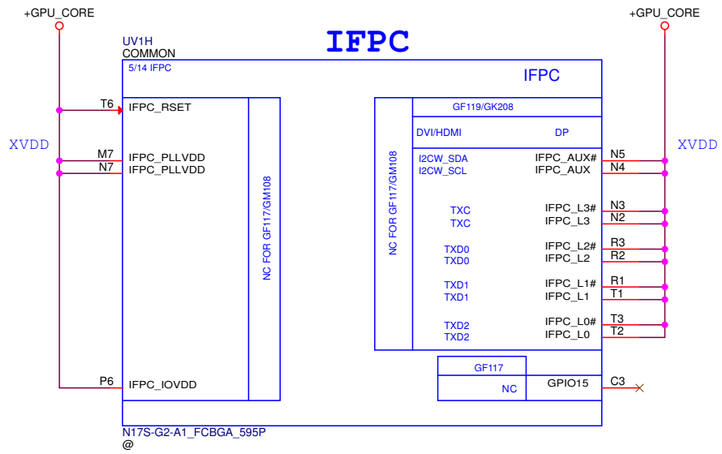
Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

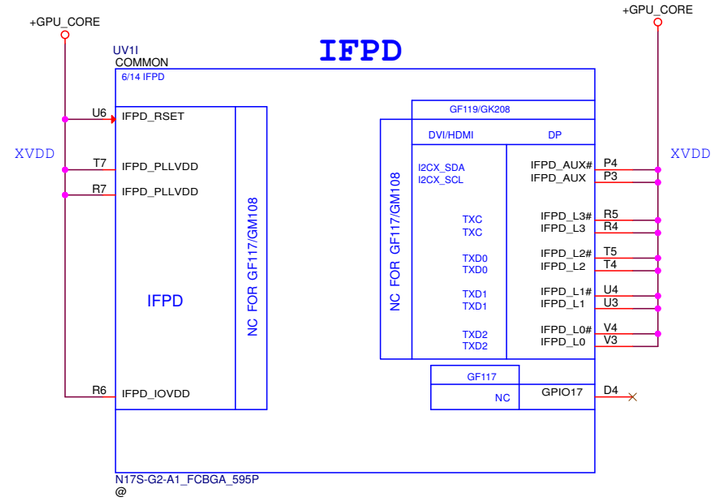
Compal Electronics, Inc.

Title: NV(1/5)-PCIE
Size: Document Number: LA-K033P
Rev: 1.0
Date: Friday, September 11, 2020 Sheet 27 of 101

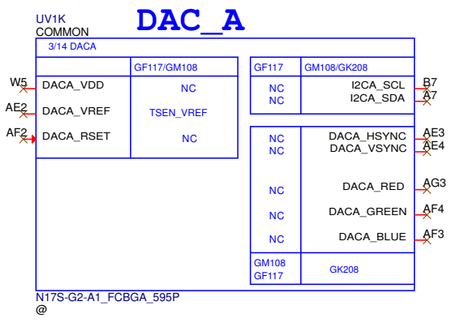
Main Func = GPU



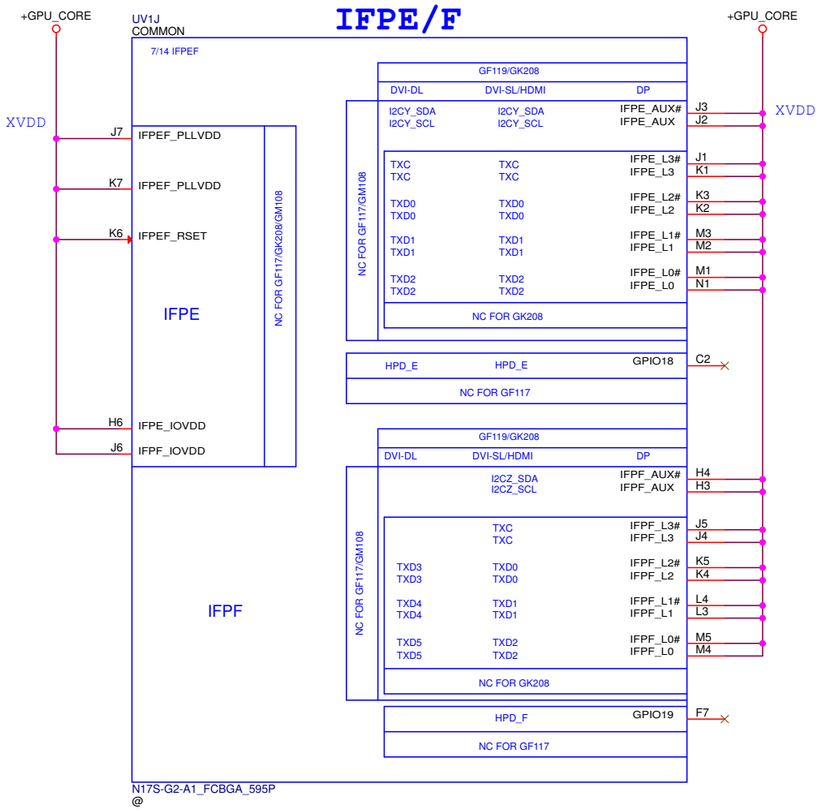




Note:
IFPC/D/E/F interface are XVDDs pin for N17S GPU, and connect them to NVVDD power for improving NVVDD power rail routing



Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
GPCPLL_AVDDx XS_PLLVDD	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω)
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 22uF (0805)
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 4.7uF (0402)



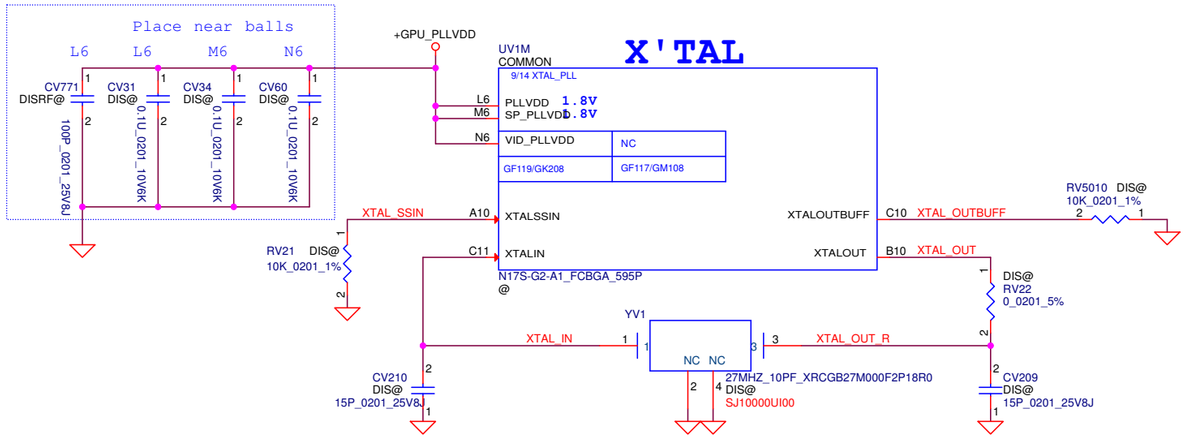


Table 11-1. Crystal Specifications

Parameter/Description	Tolerance
Nominal Frequency	27.0000 MHz
Oscillation Type	Fundamental
Operating Temperature	0 to 85°C
Absolute accuracy with respect to frequency at room temperature (25° C)	± 30 ppm
Variation over temperature range (From 0 degrees C to 70 degrees C)	± 30 ppm
Variation over time (typically 1 year)	± 5 ppm
Note: Crystal load capacitors should have 5% accuracy for best results, the value of the capacitors should be chosen according to manufacturer's specification.	

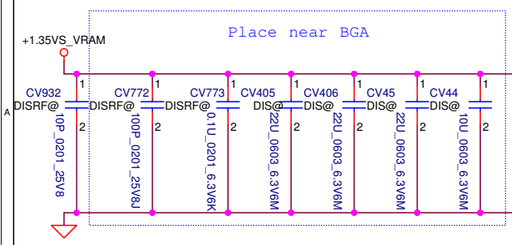
Compal Electronics, Inc.

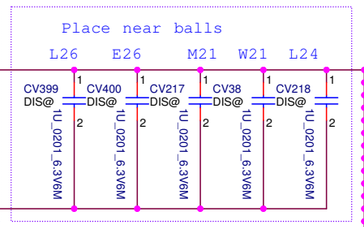
Title: NV(2/5)-IFP_ABCDEF_DAC_XTAL

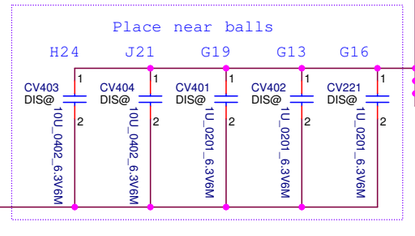
Size: | Document Number: LA-K033P | Rev: 1.0

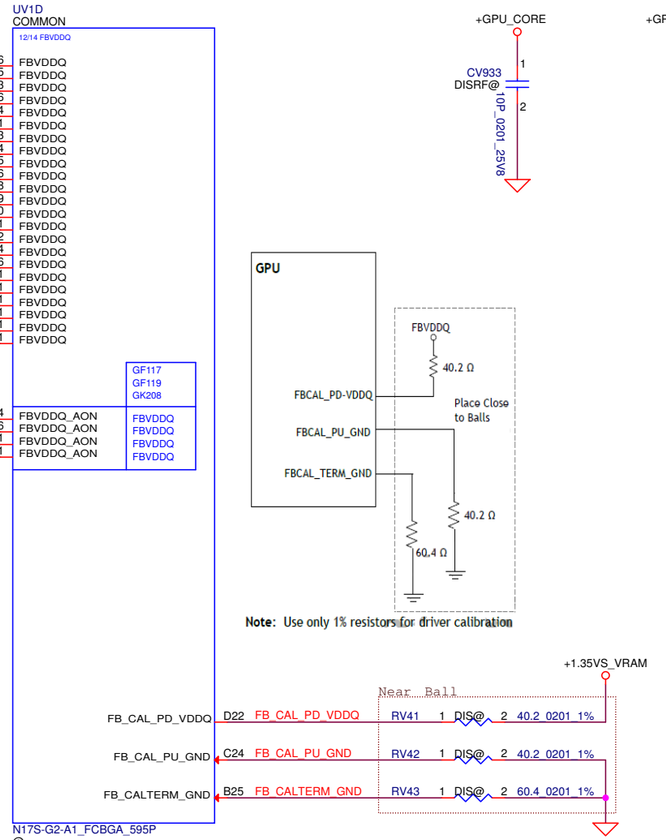
Date: Friday, September 11, 2020 | Sheet 28 of 101

Main Func = GPU

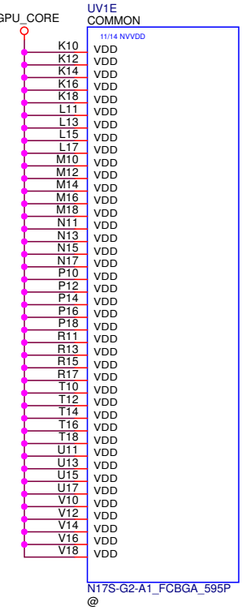






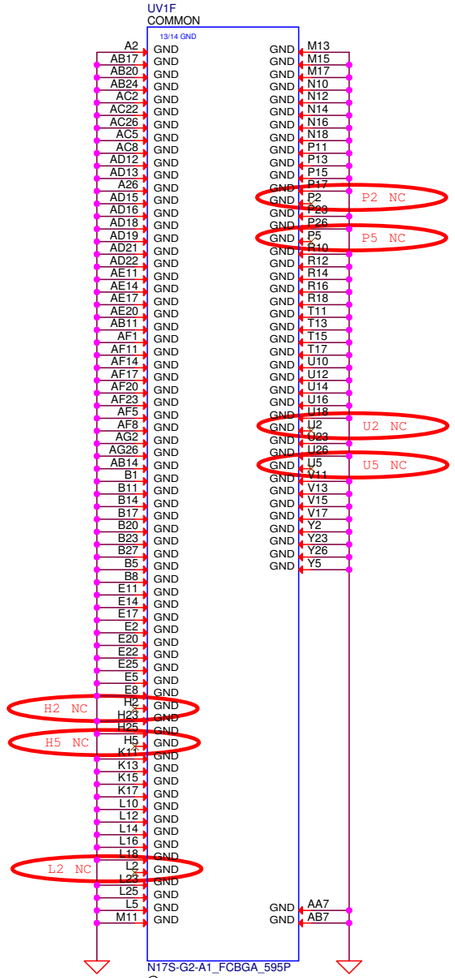


Note: Use only 1% resistors for driver calibration



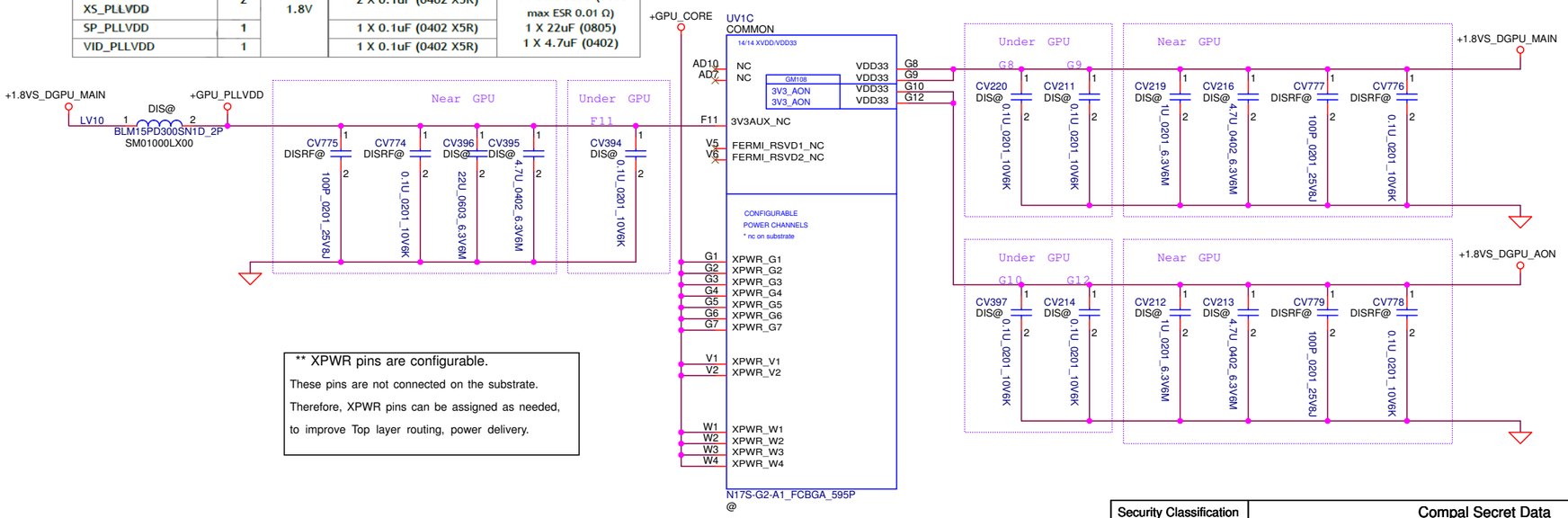
Voltage by GPU SKU

GPU_Decoupling CAPs @ Power Page



Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBVDDQ (GPU side)[1]	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
GPCPLL_AVDDx XS_PLLVDD	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω) 1 X 22uF (0805) 1 X 4.7uF (0402)
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	



Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

Title: NV(3/5)-POWER

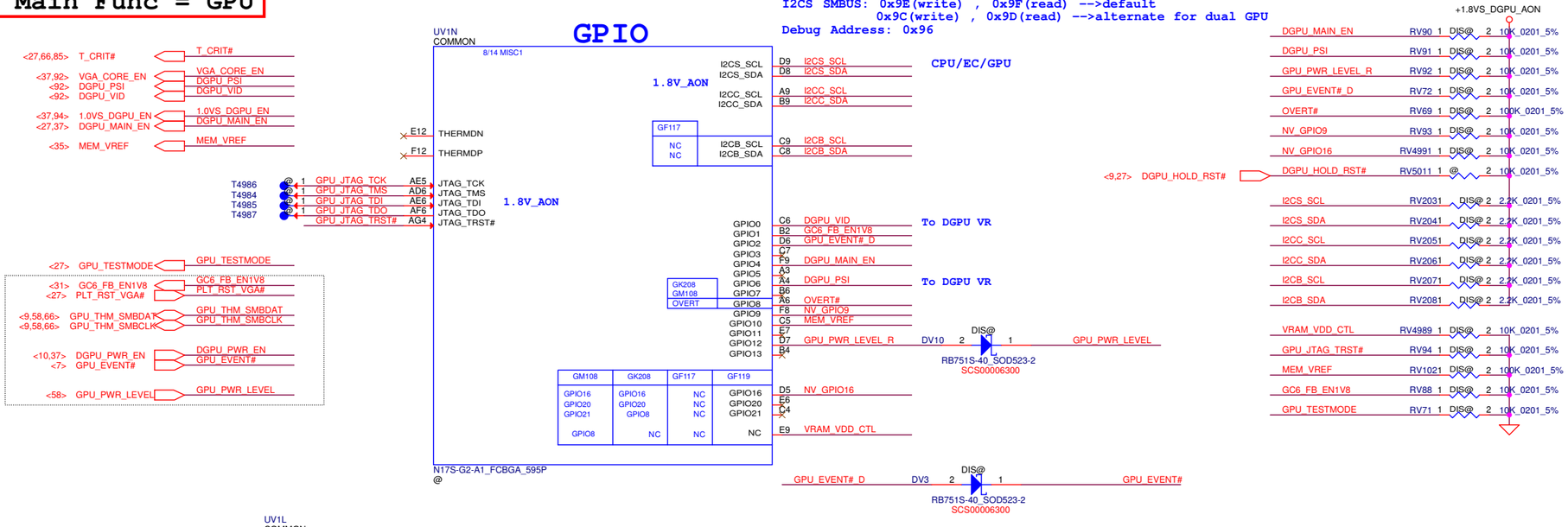
Size | Document Number: LA-K033P | Rev: 1.0

Date: Friday, September 11, 2020 | Sheet 29 of 101

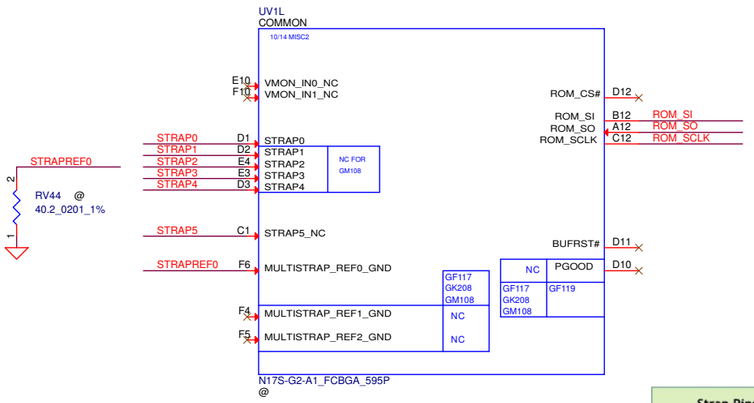
Main Func = GPU

GPIO

I2CS SMBUS: 0x9E(write) , 0x9F(read) -->default
0x9C(write) , 0x9D(read) -->alternate for dual GPU
Debug Address: 0x96



GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HVVDD_PWM	O	PWM Output to control HVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 kΩ pull-down
GPIO2	GC6M: GPU_EVENT*/ WAKE*	I	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDDS_PWM	I/O	PWM output to control the NVVDDS power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO5	FRM_LCK*	I	Active low Frame Lock	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO6	NVVDD_PSI*/ NVVDDS_PSI*	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake*	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB*	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON*	I	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	UNUSED	I/O		
GPIO18	UNUSED	I/O		
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO21	MEM_VDD_CTL	O	Frame Buffer VDD select	Open Drain; Pull-up/pull-down to set the FBVDD/Q power-on voltage at boot up
GPIO22	UNUSED	I/O		
GPIO23	GC6M: GPU_PEX_RST_HOLD*	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to gated 3V3



EXPOSED STRAP

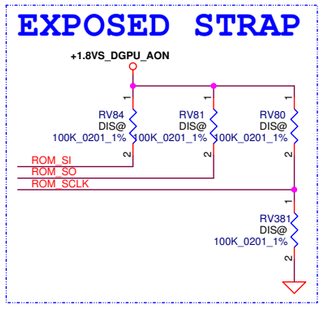
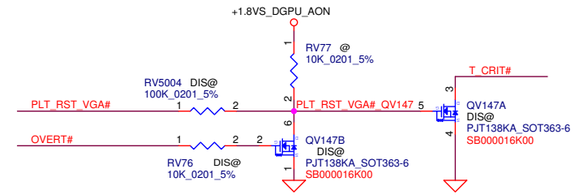
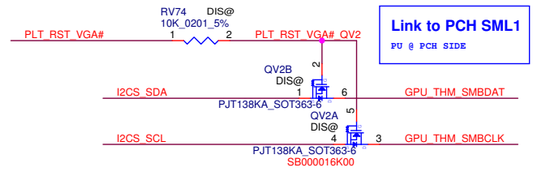


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

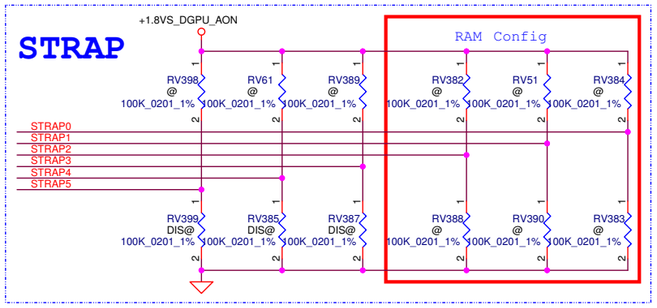
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			



Internal Thermal Sensor



STRAP



Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

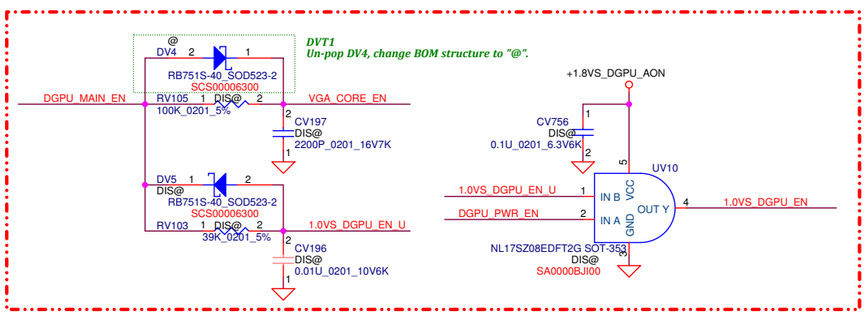


Table 6. N17S-G0/G2/G3/G4 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FC-HC25	C-die	0x3	8 Gbps	N/A	Full	Post-production ready

Notes:
1. For N17S-G0/G2/G3/G4, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

RAM_CFG	STRAP2	STRAP1	STRAP0
0x09(LML) M2G	RV388 M_STRAP@	RV390 M_STRAP@ / RV51 M_STRAP@	RV383 M_STRAP@
0x0A(LMH) H2G	RV388 H_STRAP@	RV390 H_STRAP@ / RV51 H_STRAP@	RV384 H_STRAP@
0x03(LHH) S2G	RV388 S_STRAP@	RV51 S_STRAP@	RV384 S_STRAP@

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Compal Electronics, Inc.

Title: NV(4/5)-GPIO/Strap

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Main Func = GPU

For GC6

<30> GC6_FB_EN1V8 → GC6_FB_EN1V8
<9,27> GC6_FB_EN3V3 → GC6_FB_EN3V3

<94> +1.0VS_DGPU_PGOOD → +1.0VS_DGPU_PGOOD
<37,94> 1.35V_PWR_EN → 1.35V_PWR_EN

Can set GPIO to 1.8V to cost down level shift circuit
if pop RV5012 need check double PU

GC6_FB_EN1V8 RV5012 1 @ 2 0_0201_5% GC6_FB_EN3V3

UV1B
COMMON
2/14 FBA

<35> FB_A_D[0..31]

FB_A_D0	E18	FBA_D0
FB_A_D1	F18	FBA_D1
FB_A_D2	E16	FBA_D2
FB_A_D3	F17	FBA_D3
FB_A_D4	D20	FBA_D4
FB_A_D5	D21	FBA_D5
FB_A_D6	F20	FBA_D6
FB_A_D7	E21	FBA_D7
FB_A_D8	E15	FBA_D8
FB_A_D9	D15	FBA_D9
FB_A_D10	F15	FBA_D10
FB_A_D11	F13	FBA_D11
FB_A_D12	C13	FBA_D12
FB_A_D13	B13	FBA_D13
FB_A_D14	E13	FBA_D14
FB_A_D15	D13	FBA_D15
FB_A_D16	B15	FBA_D16
FB_A_D17	C16	FBA_D17
FB_A_D18	A13	FBA_D18
FB_A_D19	A15	FBA_D19
FB_A_D20	B18	FBA_D20
FB_A_D21	A18	FBA_D21
FB_A_D22	A19	FBA_D22
FB_A_D23	C19	FBA_D23
FB_A_D24	B24	FBA_D24
FB_A_D25	C23	FBA_D25
FB_A_D26	A25	FBA_D26
FB_A_D27	A24	FBA_D27
FB_A_D28	A21	FBA_D28
FB_A_D29	B21	FBA_D29
FB_A_D30	C20	FBA_D30
FB_A_D31	C21	FBA_D31

<36> FB_A_D[32..63]

FB_A_D32	R22	FBA_D32
FB_A_D33	R24	FBA_D33
FB_A_D34	T22	FBA_D34
FB_A_D35	R23	FBA_D35
FB_A_D36	N25	FBA_D36
FB_A_D37	N26	FBA_D37
FB_A_D38	N23	FBA_D38
FB_A_D39	N24	FBA_D39
FB_A_D40	V23	FBA_D40
FB_A_D41	V22	FBA_D41
FB_A_D42	T23	FBA_D42
FB_A_D43	U22	FBA_D43
FB_A_D44	Y24	FBA_D44
FB_A_D45	AA24	FBA_D45
FB_A_D46	Y22	FBA_D46
FB_A_D47	AA23	FBA_D47
FB_A_D48	AD27	FBA_D48
FB_A_D49	AB25	FBA_D49
FB_A_D50	AD26	FBA_D50
FB_A_D51	AC25	FBA_D51
FB_A_D52	AA27	FBA_D52
FB_A_D53	AA26	FBA_D53
FB_A_D54	W26	FBA_D54
FB_A_D55	Y25	FBA_D55
FB_A_D56	R26	FBA_D56
FB_A_D57	T25	FBA_D57
FB_A_D58	N27	FBA_D58
FB_A_D59	R27	FBA_D59
FB_A_D60	V26	FBA_D60
FB_A_D61	V27	FBA_D61
FB_A_D62	W27	FBA_D62
FB_A_D63	W25	FBA_D63

NC		FB_CLAMP_F3
GF119		

FBA_CMD0 C27 FB_A_CMD0 → FB_A_CMD[0..15] <35>
FBA_CMD1 C26 FB_A_CMD1
FBA_CMD2 E24 FB_A_CMD2
FBA_CMD3 F24 FB_A_CMD3
FBA_CMD4 D27 FB_A_CMD4
FBA_CMD5 D26 FB_A_CMD5
FBA_CMD6 F25 FB_A_CMD6
FBA_CMD7 F26 FB_A_CMD7
FBA_CMD8 F23 FB_A_CMD8
FBA_CMD9 G22 FB_A_CMD9
FBA_CMD10 G23 FB_A_CMD10
FBA_CMD11 G24 FB_A_CMD11
FBA_CMD12 F27 FB_A_CMD12
FBA_CMD13 G25 FB_A_CMD13
FBA_CMD14 G27 FB_A_CMD14
FBA_CMD15 G26 FB_A_CMD15
FBA_CMD16 M24 FB_A_CMD16 → FB_A_CMD[16..31] <36>
FBA_CMD17 M23 FB_A_CMD17
FBA_CMD18 K24 FB_A_CMD18
FBA_CMD19 K23 FB_A_CMD19
FBA_CMD20 M27 FB_A_CMD20
FBA_CMD21 M26 FB_A_CMD21
FBA_CMD22 M25 FB_A_CMD22
FBA_CMD23 K26 FB_A_CMD23
FBA_CMD24 K22 FB_A_CMD24
FBA_CMD25 J23 FB_A_CMD25
FBA_CMD26 J25 FB_A_CMD26
FBA_CMD27 J24 FB_A_CMD27
FBA_CMD28 K27 FB_A_CMD28
FBA_CMD29 K25 FB_A_CMD29
FBA_CMD30 J27 FB_A_CMD30
FBA_CMD31 J26 FB_A_CMD31

<35> FB_A_DBI0 FB_A_DBI0 D19 FBA_DQM0
<35> FB_A_DBI1 FB_A_DBI1 D14 FBA_DQM1
<35> FB_A_DBI2 FB_A_DBI2 C17 FBA_DQM2
<35> FB_A_DBI3 FB_A_DBI3 C22 FBA_DQM3
<36> FB_A_DBI4 FB_A_DBI4 P24 FBA_DQM4
<36> FB_A_DBI5 FB_A_DBI5 W24 FBA_DQM5
<36> FB_A_DBI6 FB_A_DBI6 AA25 FBA_DQM6
<36> FB_A_DBI7 FB_A_DBI7 U25 FBA_DQM7

<35> FB_A_EDC0 FB_A_EDC0 E19 FBA_DQS_WP0
<35> FB_A_EDC1 FB_A_EDC1 C15 FBA_DQS_WP1
<35> FB_A_EDC2 FB_A_EDC2 B16 FBA_DQS_WP2
<35> FB_A_EDC3 FB_A_EDC3 B22 FBA_DQS_WP3
<36> FB_A_EDC4 FB_A_EDC4 R25 FBA_DQS_WP4
<36> FB_A_EDC5 FB_A_EDC5 W23 FBA_DQS_WP5
<36> FB_A_EDC6 FB_A_EDC6 AB26 FBA_DQS_WP6
<36> FB_A_EDC7 FB_A_EDC7 T26 FBA_DQS_WP7

F19 FBA_DQS_RN0
C14 FBA_DQS_RN1
A16 FBA_DQS_RN2
A22 FBA_DQS_RN3
P25 FBA_DQS_RN4
W22 FBA_DQS_RN5
AB27 FBA_DQS_RN6
T27 FBA_DQS_RN7

GF117/GF119
GK208

NC	FBA_CMD32	B19
FBA_DEBUG0	FBA_CMD34	F22 1 — T20 @
FBA_DEBUG1	FBA_CMD35	J22 1 — T21 @

FBVDDQ_GPU
1.35V

FBA_CLK0 D24 FB_A_CLK0 → FB_A_CLK0 <35>
FBA_CLK0# D25 FB_A_CLK#0 → FB_A_CLK#0 <35>
FBA_CLK1 N22 FB_A_CLK1 → FB_A_CLK1 <36>
FBA_CLK1# M22 FB_A_CLK#1 → FB_A_CLK#1 <36>

FBA_WCK01 D18 FB_A_WCK0 → FB_A_WCK0 <35>
FBA_WCK01# C18 FB_A_WCK#0 → FB_A_WCK#0 <35>
FBA_WCK23 D17 FB_A_WCK1 → FB_A_WCK1 <35>
FBA_WCK23# D16 FB_A_WCK#1 → FB_A_WCK#1 <35>
FBA_WCK45 T24 FB_A_WCK2 → FB_A_WCK2 <36>
FBA_WCK45# U24 FB_A_WCK#2 → FB_A_WCK#2 <36>
FBA_WCK67 V24 FB_A_WCK3 → FB_A_WCK3 <36>
FBA_WCK67# V25 FB_A_WCK#3 → FB_A_WCK#3 <36>

GDDR5 design

+1.35VS_VRAM

FBA_CKE_L FB_A_CMD15 RV2439 1 DIS@ 2 10K_0201_1%
FBA_CKE_H FB_A_CMD30 RV2440 1 DIS@ 2 10K_0201_1%
FBA_RST_L FB_A_CMD13 RV2437 1 DIS@ 2 10K_0201_1%
FBA_RST_H FB_A_CMD29 RV2438 1 DIS@ 2 10K_0201_1%

GF119
NC
FB_PLLAVDD F16
FB_PLLAVDD P22

FB_PLLAVDD FB_DLLAVDD H22
GF117

Place near balls

+1.8VS_DGPU_MAIN
+FB_PLLAVDD LV7 1 DIS@ 2 BLM15PD300SN1D_2P SM01000LX00

CV55 DIS@ 0.1U_0201_10V6K	CV52 DIS@ 0.1U_0201_10V6K	CV53 DIS@ 0.1U_0201_10V6K	CV398 DIS@ 0.1U_0201_10V6K	CV51 DIS@ 22U_0603_6.3V6M	CV781 DISRF@ 10P_0201_25V8	CV780 DIS@ 0.1U_0201_6.3V6K	CV783 DISRF@ 100P_0201_25V8J	CV782 DISRF@ 100P_0201_25V8J	CV784 DISRF@ 100P_0201_25V8J	CV785 DISRF@ 2200P_0201_16V7K
F16	P22	H22			F16	F16	P22	P22	H22	H22

For VRAM DEBUG using

T4988 @ 1 FB_VREF D23 FB_VREF_PROBE

N17S-G2-A1_FCBGA_595P
@

GDDR5_BGA170_MIRR COMMAND MAP

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

+3VS
RV111 100K_0201_5% DIS@
RV113 100K_0201_5% DIS@
GC6_FB_EN3V3
GC6_FB_EN3V3_Q 5
QV8A DIS@ PJT138KA 2N SOT363-6 SB000016K00
GC6_FB_EN1V8 2
QV8B DIS@ PJT138KA 2N SOT363-6 SB000016K00

+1.8VS_DGPU_AON
UV23 FBVDD/Q_EN
GC6_FB_EN3V3 2
+1.0VS_DGPU_PGOOD 1
1.35V_PWR_EN 4
74LVC1G32GW_TSSOP5 SA000014S00 DIS@
1.8V OR GATE

From DG-07158-001_v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

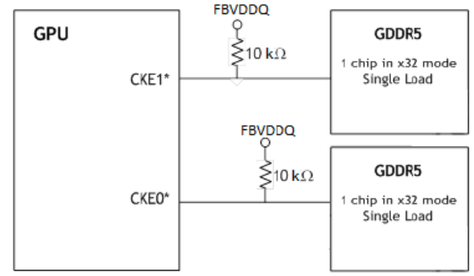

Figure 7-4. Clock Enable (CKE*) Signal Connection, ×32 Mode

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10 k Ω pull-down resistor in standard mode or in clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

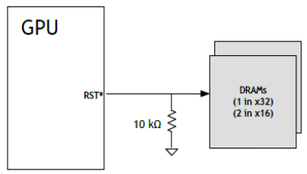

Figure 7-3. Reset Signal Connection

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 30Ω bead (0603 max ESR 10 mΩ) 1 X 22uF (0805)
FBB_PLL_AVDD	1			
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)	

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Compal Electronics, Inc.

Title: NV(5/5)-MEMORY FBA

Size: | Document Number: LA-K033P | Rev: 1.0

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Reserve

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Compal Electronics, Inc.

Title: **Reserve**

Size	Document Number	Rev
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Reserve

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **SMbus Block Diagram**

Size	Document Number	Rev
	LA-K033P	1.0

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Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

Title: **SMbus Block Diagram**

Size	Document Number	Rev
	LA-K033P	1.0

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Main Func = VRAM

Memory Partition A

<31> FB_A_CMD[0..15] — FB_A_CMD[0..15]
<31> FB_A_D[0..31] — FB_A_D[0..31]
<36> +FBA_VREFC0 — +FBA_VREFC0
<30> MEM_VREF — MEM_VREF

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to DRAM. See section 7.1.13.

UV6 MF=0

	MF=0	MF=1	MF=1	MF=0		
<31> FB_A_EDC0	EDC0	EDC3	DQ24	DQ0	A4	FB_A_D0
<31> FB_A_EDC1	EDC1	EDC2	DQ25	DQ1	A2	FB_A_D1
<31> FB_A_EDC2	EDC2	EDC1	DQ26	DQ2	B4	FB_A_D2
<31> FB_A_EDC3	EDC3	EDC0	DQ27	DQ3	B2	FB_A_D3
			DQ28	DQ4	E4	FB_A_D4
			DQ29	DQ5	E2	FB_A_D5
			DQ30	DQ6	F4	FB_A_D6
			DQ31	DQ7	F2	FB_A_D7
			DQ16	DQ8	A11	FB_A_D8
			DQ17	DQ9	A13	FB_A_D9
			DQ18	DQ10	B11	FB_A_D10
			DQ19	DQ11	B13	FB_A_D11
			DQ20	DQ12	E11	FB_A_D12
			DQ21	DQ13	E13	FB_A_D13
			DQ22	DQ14	F11	FB_A_D14
			DQ23	DQ15	F13	FB_A_D15
			DQ8	DQ16	U11	FB_A_D16
			DQ9	DQ17	U13	FB_A_D17
			DQ10	DQ18	T11	FB_A_D18
			DQ11	DQ19	T13	FB_A_D19
			DQ12	DQ20	N11	FB_A_D20
			DQ13	DQ21	N13	FB_A_D21
			DQ14	DQ22	M11	FB_A_D22
			DQ15	DQ23	M13	FB_A_D23
			DQ0	DQ24	U4	FB_A_D24
			DQ1	DQ25	U2	FB_A_D25
			DQ2	DQ26	T4	FB_A_D26
			DQ3	DQ27	T2	FB_A_D27
			DQ4	DQ28	N4	FB_A_D28
			DQ5	DQ29	N2	FB_A_D29
			DQ6	DQ30	M4	FB_A_D30
			DQ7	DQ31	M2	FB_A_D31
<31> FB_A_DBI0	DBI0#	DBI3#				
<31> FB_A_DBI1	DBI1#	DBI2#				
<31> FB_A_DBI2	DBI2#	DBI1#				
<31> FB_A_DBI3	DBI3#	DBI0#				
<31> FB_A_CLK0	CK					
<31> FB_A_CLK#0	CK#					
FB_A_CMD14 J3	CKE#					
FB_A_CMD2 H11	BA0/A2	BA2/A4				
FB_A_CMD4 K10	BA1/A5	BA3/A3				
FB_A_CMD3 K11	BA2/A4	BA0/A2				
FB_A_CMD1 H10	BA3/A3	BA1/A5				
FB_A_CMD6 K4	A8/A7	A10/A0				
FB_A_CMD11 H5	A9/A1	A11/A6				
FB_A_CMD10 H4	A10/A0	A8/A7				
FB_A_CMD7 K5	A11/A6	A9/A1				
FB_A_CMD9 J5	A12/RFU/NC					
A5	VPP/NC_2					
U5	VPP/NC_1					
RV116 DIS@ 1 — 2 1K_0201_1% — FB_A_MF J1	MF					
RV118 DIS@ 1 — 2 1K_0201_1% — FB_A_SEN J10	SEN					
RV120 DIS@ 2 — 1 121_0201_1% — FB_A_ZQ J13	ZQ					
FB_A_CMD8 J4	ABI#					
FB_A_CMD12 G3	RAS#	CAS#				
FB_A_CMD0 G12	CS#	WE#				
FB_A_CMD15 L3	CAS#	RAS#				
FB_A_CMD5 L12	WE#	CS#				
<31> FB_A_WCK#0	WCK01#	WCK23#				
<31> FB_A_WCK0	WCK01	WCK23				
<31> FB_A_WCK#1	WCK23#	WCK01#				
<31> FB_A_WCK1	WCK23	WCK01				
A10	VREFD_1					
U10	VREFD_2					
+FBA_VREFC0 J14	VREFC					
FB_A_CMD13 J2	RESET#					
H1	VSS					
K1	VSS					
B5	VSS					
G5	VSS					
L5	VSS					
T5	VSS					
B10	VSS					
D10	VSS					
G10	VSS					
L10	VSS					
P10	VSS					
T10	VSS					
H14	VSS					
K14	VSS					
G1	VDD					
L1	VDD					
G4	VDD					
L4	VDD					
C5	VDD					
R5	VDD					
C10	VDD					
R10	VDD					
D11	VDD					
G11	VDD					
L11	VDD					
P11	VDD					
G14	VDD					
L14	VDD					

BYTE0: DQ0–DQ7 / FB_A_D0–FB_A_D7
BYTE1: DQ8–DQ15 / FB_A_D8–FB_A_D15
BYTE2: DQ16–DQ23 / FB_A_D16–FB_A_D23
BYTE3: DQ24–DQ31 / FB_A_D24–FB_A_D31

+1.35VS_VRAM

VDDQ: B1, D1, F1, M1, P1, T1, G2, L2, B3, D3, F3, H3, K3, M3, P3, T3, E5, N5, E10, N10, B12, D12, F12, H12, K12, M12, P12, T12, G13, L13, B14, D14, F14, M14, P14, T14

VSSQ: A1, C1, E1, N1, R1, U1, H2, K2, A3, C3, E3, N3, R3, U3, C4, R4, F5, M5, F10, M10, C11, R11, A12, C12, E12, N12, R12, U12, H13, K13, A14, C14, E14, N14, R14, U14

170-BALL
SGRAM GDDR5
H5GC4H24MFR-T2C
@

+1.35VS_VRAM
Place near pin J14 of each VRAM
W=16mils
RV125 DIS@ 549_0201_1%
RV200 DIS@ 931_0201_1%
RV127 DIS@ 1.33K_0201_1%
CV158 DIS@ 820P_0201_25V7K
CV159 DIS@ 820P_0201_25V7K
+FBA_VREFC0
MEM_VREF
QV50 BSS138W 1N SOT-323-3 DIS@

Near to UV6
FB_A_CLK0 — RV11 DIS@ 40.2_0201_1% — FB_A_CLK0_R — RV21 DIS@ 40.2_0201_1% — FB_A_CLK#0
CV4 DIS@ 0.01U_0201_10V6K

+1.35VS_VRAM
Near VRAM
CV601 DIS@ 22U_0603_6.3V6M
CV602 DIS@ 22U_0603_6.3V6M
CV603 DIS@ 10U_0603_6.3V6M
CV604 DIS@ 10U_0603_6.3V6M
Near ball
CV605 DIS@ 10U_0603_6.3V6M
CV606 DIS@ 10U_0603_6.3V6M
CV607 DIS@ 10U_0603_6.3V6M
CV608 DIS@ 10U_0603_6.3V6M

+1.35VS_VRAM
Near ball
CV609 DIS@ 1U_0201_6.3V6M
CV610 DIS@ 1U_0201_6.3V6M
CV611 DIS@ 1U_0201_6.3V6M
CV612 DIS@ 1U_0201_6.3V6M
CV613 DIS@ 1U_0201_6.3V6M
CV614 DIS@ 1U_0201_6.3V6M
CV615 DIS@ 1U_0201_6.3V6M
CV616 DIS@ 1U_0201_6.3V6M
CV617 DIS@ 1U_0201_6.3V6M
CV618 DIS@ 1U_0201_6.3V6M
CV765 DIS@ 1U_0201_6.3V6M
CV766 DIS@ 1U_0201_6.3V6M
CV764 DIS@ 1U_0201_6.3V6M
CV763 DIS@ 1U_0201_6.3V6M

Hynix 2G

UV6: SA0000C171L H2G_R3@
UV8: SA0000C171L H2G_R3@
S IC D5 256M32 H5GC8H24AJR-R2C BGA A31! S IC D5 256M32 H5GC8H24AJR-R2C BGA A31!

Micron 2G

UV6: SA00009TI3L M2G_R3@
UV8: SA00009TI3L M2G_R3@
S IC D5 256M32 MT51J256M32HF-80:B A31! S IC D5 256M32 MT51J256M32HF-80:B A31!

Samsung 2G

UV6: SA00009TA3L S2G_R3@
UV8: SA00009TA3L S2G_R3@
S IC D5 256M32 K4G80325FC-HC25 FBGA A31! S IC D5 256M32 K4G80325FC-HC25 FBGA A31!

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.
Title: N17S_GDDR5_A
Size: | Document Number: LA-K033P | Rev: 1.0
Date: Friday, September 11, 2020 | Sheet 35 of 101

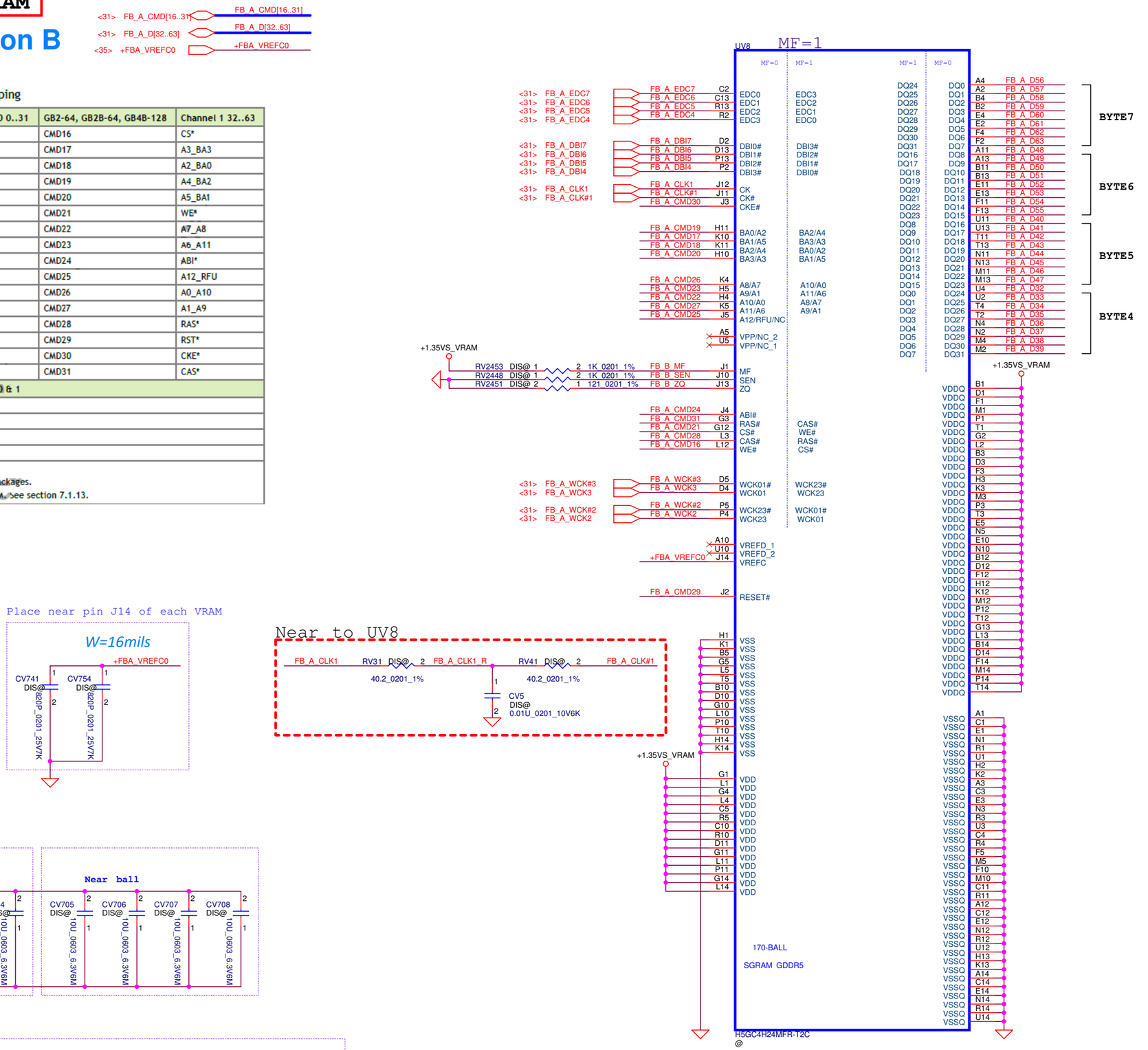
Main Func = VRAM

Memory Partition B

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to DRAM. See section 7.1.13.



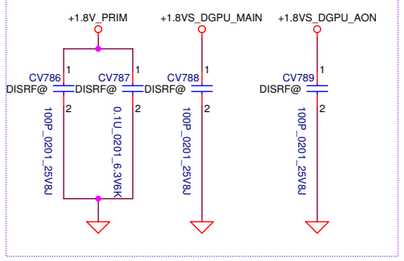
Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.			
Title: N17S_GDDR5_B			
Size	Document Number: LA-K033P		Rev: 1.0
Date: Friday, September 11, 2020	Sheet 36 of 101		

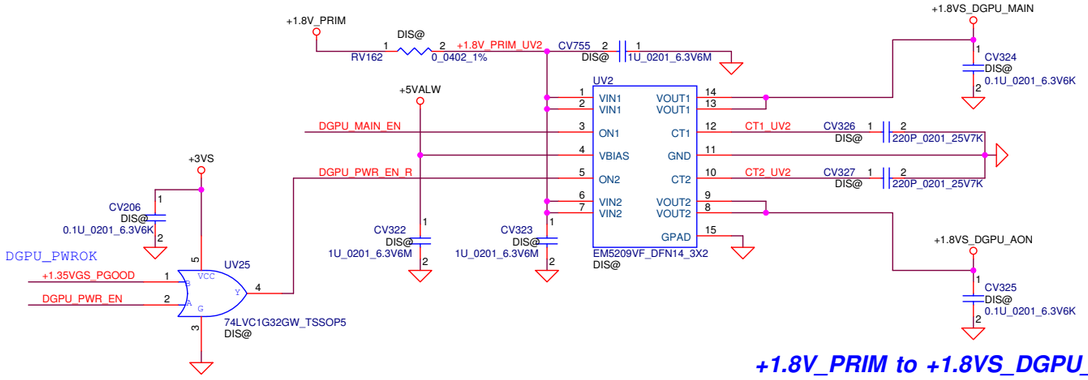
Main Func = GPU DC

<30,92> VGA_CORE_EN → VGA_CORE_EN
<30,94> 1.0VS_DGPU_EN → 1.0VS_DGPU_EN
<27,94> +1.35VGS_PGOOD → +1.35VGS_PGOOD
<10,30> DGPU_PWR_EN → DGPU_PWR_EN
<27,30> DGPU_MAIN_EN → DGPU_MAIN_EN
<31,94> 1.35V_PWR_EN → 1.35V_PWR_EN

Place near UV2

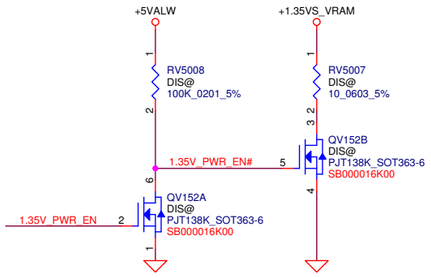


+1.8V_PRIM to +1.8VS_DGPU

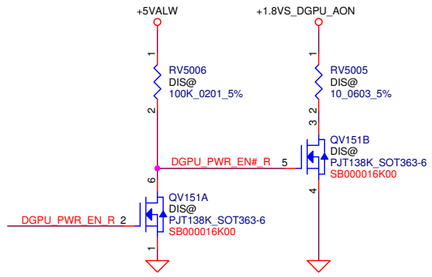


+1.8V_PRIM to +1.8VS_DGPU_AON

+1.35VS_VRAM Discharge

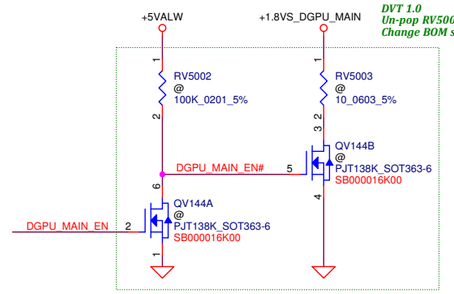


+1.8VS_DGPU_AON Discharge

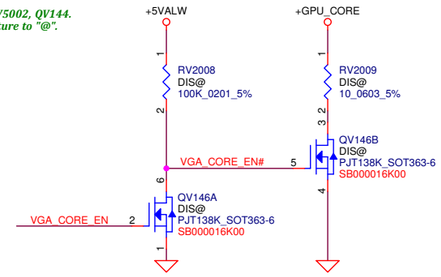


+1.8VS_DGPU_MAIN Discharge

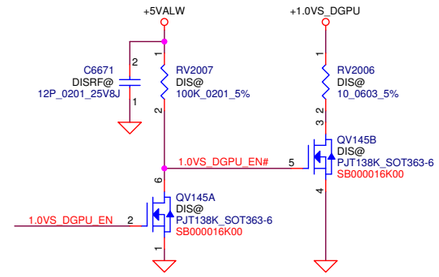
DVT 1.0
Un-pop RV5003, RV5002, QV144.
Change BOM structure to "@".



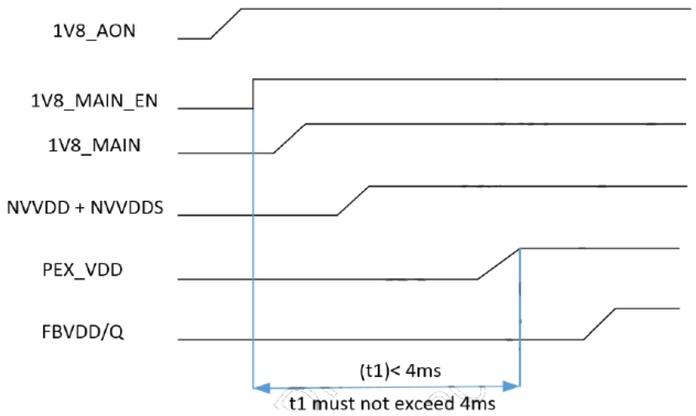
+GPU_CORE Discharge



+1.0VS_DGPU Discharge



Power-Up Sequence



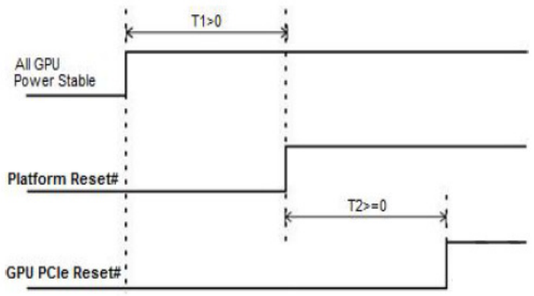
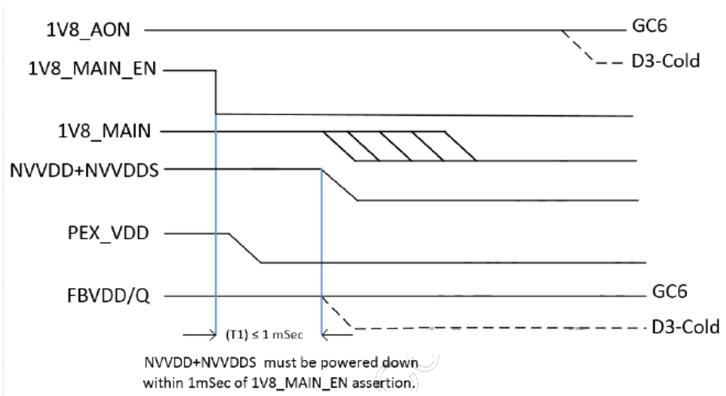
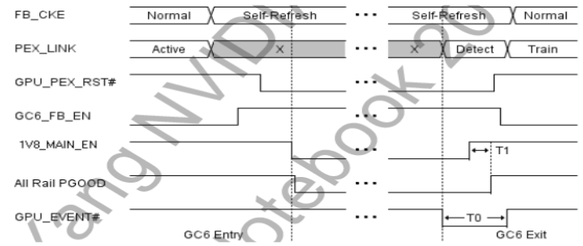


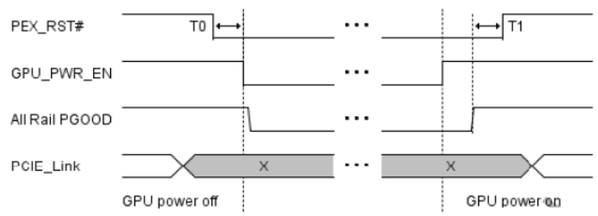
Figure 8.4 Cold Reset Sequence Requirement for Optimus

Power-Down Sequence





Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms



Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.	
Title	DGPU_DC/DC Interface
Size	Document Number: LA-K033P
Rev	1.0
Date:	Friday, September 11, 2020
Sheet	37 of 101

Main Func = LCD

Pin 5,6,9 Cable side NC
Pin 4 for 17" CAMERA

JEDP1 CONN@
ACES_51540-04001-P01
SP010029F00

+DCBAT_LCD
+3VS
+MIC_VCC
+3VS_CAM
+TS_VDD
+LCDVDD_LCD

LCD_TST_C
DBC_PANEL_EN_R
EDP_HPD
LCD_CBL_DET#
EDP_AUXP_C
EDP_AUXN_C
EDP_TXN0_C
EDP_TXP0_C
EDP_TXN1_C
EDP_TXP1_C
TOUCH_SCREEN_INT#_LCD
TOUCH_SCREEN_RST_LCD
LCD_BRIGHTNESS
BLON_OUT_C
DMIC_DATA_EDP
DMIC_CLK_EDP
USB20_N6_R
USB20_P6_R
USB20_N8_R
USB20_P8_R
TS_DET#
TS_EN

R96 close JEDP! @ 08/15

60 mils
C105 place near JEDP1

INVERTER POWER

+19VB
F1 1.5A_24V_SMD1812P150TF-24
+DCBAT_LCD
+LCDVDD_LCD
+LCDVDD
R8 0_0603_5%
DMIC_CLK_EDP
DMIC_DATA_EDP
ED4 CEST523NC5VB_SOT-523-3 @ESD@

EE note: Never change R8 to short pad after MP

to Codec
to PCH

R-short 0831

Brightness

Backlight

BAT54C_SOT23-3~D

EC (BIST MODE)

High Active

SY6288C20AAC_SOT23-5

40mil

For BL_PWR_SRC & LCDVDD monitor

RF Request
place as close as QV18

SB00000W600 MMDT3906_SOT363-6 QV18A LBIST@
SB00000W600 MMDT3906_SOT363-6 QV18B LBIST@
LMBT3904WT1G_SC70-3

Main Func = CAM&MIC, TS

TCH@ -->Touch Screen
@RF@ --> RF
I2CTCH@ --> I2C Touch Screen
USBTCH@ --> USB Touch Screen

Non-TCH -->R81, R82, F5 unpop

C36: colse to JEDP1.29
C102: colse to JEDP1

TOUCH_SCREEN

Main Func = Hinge up protection

U4 ICPRO@ G2895ALK21U_TDFN10_2X2

to EC

I2C Touch Screen (Reserved)

Close to JEDP1

USBTCH@
R-short 0831

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: LCD/Cam/MIC/T.Panel

Size: | Document Number: LA-K033P | Rev: 1.0

Date: Friday, September 11, 2020 | Sheet 38 of 101

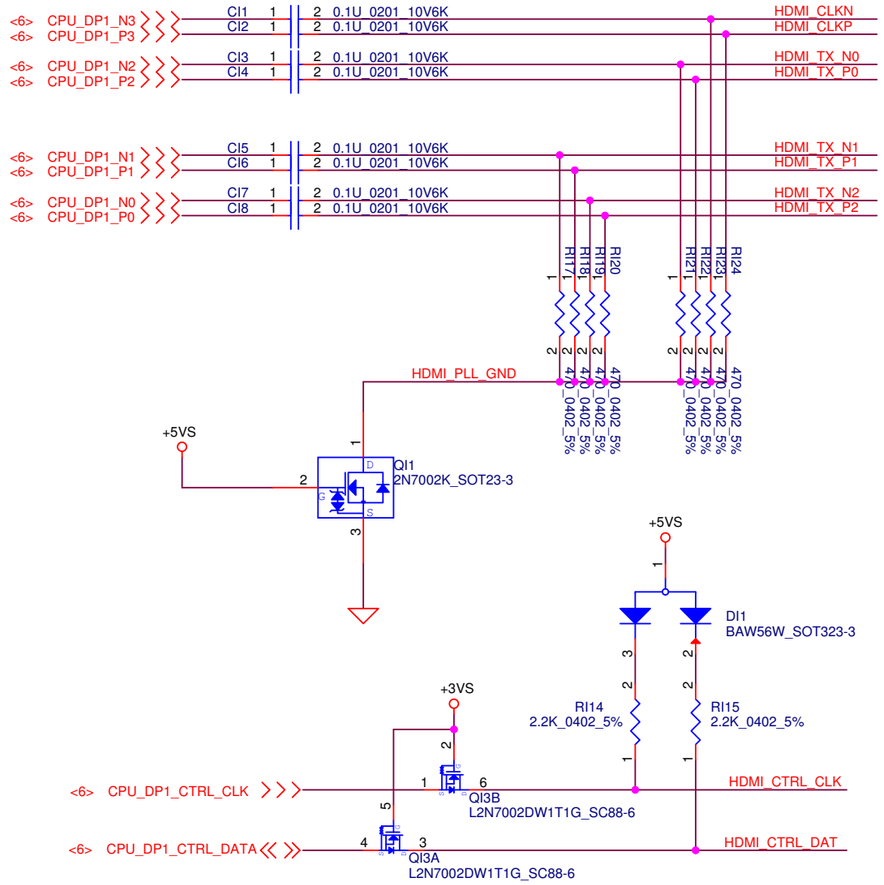
Main Function:

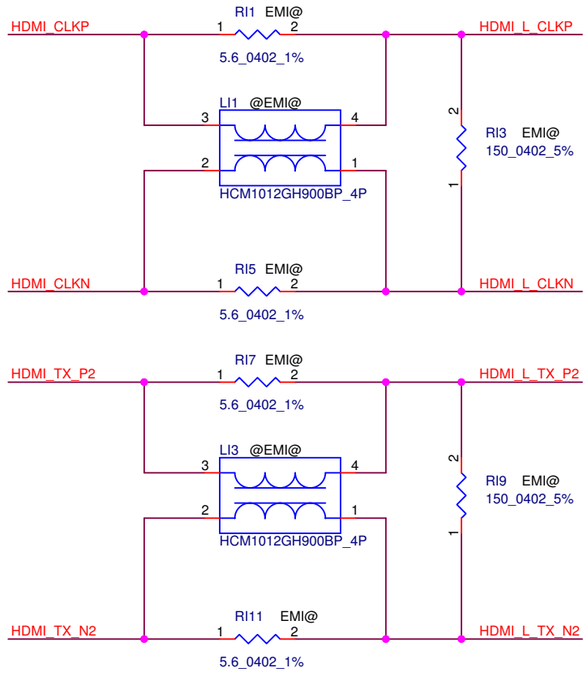
Reserve

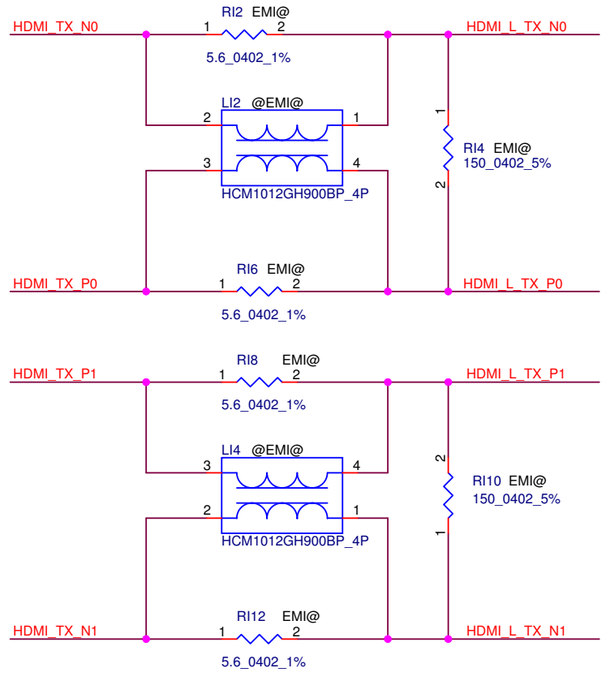
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

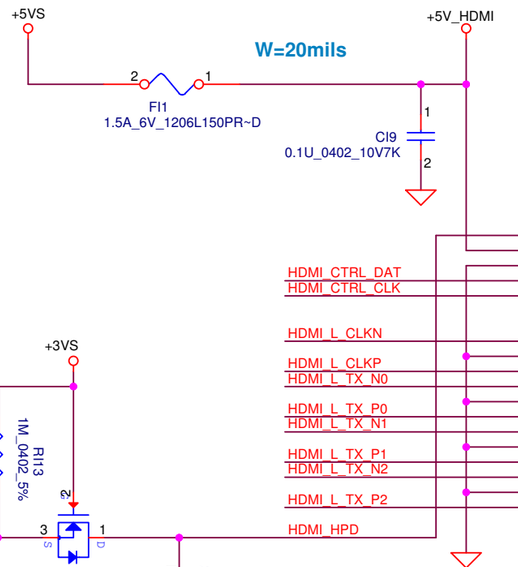
Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 39 of 101	

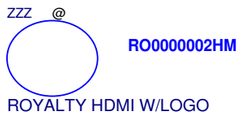
Main Func = HDMI











Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: HDMI L.Shifter/Conn			
Size	Document Number: LA-K033P		Rev: 1.0
Date: Friday, September 11, 2020		Sheet 40 of 101	

Main Function:

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 41 of 101	

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port0 (1/2)**

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 42 of 101

Main Func =

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.		
Title: TBT TYPE-C Port0 (2/2)		
Size	Document Number: LA-K033P	Rev: 1.0
Date: Friday, September 11, 2020	Sheet 43 of 101	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port1 (1/2)**

Size | Document Number: **LA-K033P** | Rev: 1.0

Date: Friday, September 11, 2020 | Sheet 44 of 101

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **TBT_TYPE-C Port1 (2/2)**

Size	Document Number	Rev
	LA-K033P	1.0
Date: Friday, September 11, 2020	Sheet 45 of 101	

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/12/24	Deciphered Date	2018/12/31	Title: TBT_TYPE-C Port2 (1/2)
				Size: Document Number: LA-K033P Rev: 1.0
				Date: Friday, September 11, 2020 Sheet 46 of 101

Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **TBT TYPE-C Port2 (2/2)**

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 47 of 101

Reserve

Compal Electronics, Inc.
Title: TBT TYPE-C Port3 (1/2)
Size | Document Number: LA-K033P | Rev: 1.0
Date: Friday, September 11, 2020 | Sheet 48 of 101

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/12/24	Deciphered Date	2018/12/31	Title: Reserve for TBT_TYPE-C Port3 (2/2)
				Size: — Document Number: LA-K033P — Rev: 1.0
				Date: Friday, September 11, 2020 — Sheet 49 of 101

MB_USB3.1 TypeC Conn. (Power Path)

POP
TYPEC@

UNPOP
CCG5C@/TBT@

5V@3A

+5VALW → RT1423 @ 0_0603_5% → +5VALW_25814

R-short 0831

+5VALW_25814 → 22U_0603_6.3V6M ×8 (CT3965/CT3966/CT3967/CT3968/CT3969/CT3970/CT3971/CT3972 TYPEC@)

+CCG_VBUS → CT3957 4.7U_0603_25V6K TYPEC@

W=120 mils

+3VALW → CT3967 10U_0402_6.3V6M TYPEC@

+LDO_3V3 → RT1446 100K_0201_5% @TYPEC@ / RT5 100K_0201_5% TYPEC@ → ADCIN1 / ADCIN2

RT1447 100K_0201_5% TYPEC@ / RT1448 100K_0201_5% @TYPEC@

+3VALW → RT1451 1 TYPEC@2 100K_0201_5% TPS25814_EN#

need to ask EC , low act i vef or TPS25814

+5VALW → RT1425 100K_0201_5% @ → CHG_HI# → RT1456 100K_0201_5% TYPEC@

CHG_HI PD set for 3A
(replay by TI FAE)

+LDO_3V3 → RT1445/RT1444/RT1443 10K_0201_5% TYPEC@ → TPS25814_I2C_SDA / TPS25814_I2C_SCL / TPS25814_I2C_IRQ#

UT37 TYPEC@ — PTPS25814AARSMR_QFN32_4X4

29	PP5V2	VBUS1	26
28	PP5V1	VBUS2	27
32	VIN_3V3	USB_P	22 — TPS25814_USB_P — RT1452 1 TYPEC@2 0_0201_5% — USB20_P4
		USB_N	23 — TPS25814_USB_N — RT1453 1 TYPEC@2 0_0201_5% — USB20_N4
2	ADCIN1	CC1	24 — 20 mils — TYPEC_CC1 <50>
3	ADCIN2	CC2	25 — TYPEC_CC2 <50>
5	DISABLE	DEBUG	6 — RT1422 1 TYPEC@2 100K_0201_5% — +3VALW
17	CHG_HI	FAULT	7 — RT1426 1 @ 2 0_0201_5% — USB_OC2# <6>
30	CTL	POL	13 — TPS25814_POL# — TPS25814_POL# <58>
8	I2C_EC_SDA	SINK	18 — TPS25814_UFP# — TPS25814_UFP# <58>
9	I2C_EC_SCL	LD_HIGH	31 — RT1454 1 @ 2 0_0201_5%
10	I2C_EC_IRQ		
1	LDO_3V3		
4	LDO_1V5		
11 NC1, 12 NC2, 15 NC3, 16 NC4, 19 NC5, 20 NC6, 21 NC7, 33 thermal pad, 14 GND1			

low Active

<58> TPS25814_EN# → RT1457 1 TYPEC@2 100K_0201_5%

CDP mode

+LDO_3V3 → CT3966 10U_0402_6.3V6M TYPEC@

+LDO_1V5 → CT3965 10U_0402_6.3V6M TYPEC@

Can be f l oat i ng, if no need

R-short 0831

for EC inform Type-C port has device plugging

TPS25814_POL# 1 TYPEC@2 RT1450 100K_0201_5%
TPS25814_UFP# 1 TYPEC@2 RT1449 100K_0201_5% → +3VALW

USB3 CTX DRX P3

<12> USB3_CTX_DRX_P3 → USB3_CTX_DRX_P3 → CU22 0.1U_0402_10V7K TYPEC@ → USB3_CTX_C_DRX_P3 → RT1434 0_0402_5% (TYPEC@EMI@) → LT13@EMI@ → USB3_CTX_L_DRX_P3

USB3 CTX DRX N3

<12> USB3_CTX_DRX_N3 → USB3_CTX_DRX_N3 → CU23 0.1U_0402_10V7K TYPEC@ → USB3_CTX_C_DRX_N3 → RT1439 0_0402_5% (TYPEC@EMI@) → HCM1012GH900BP_4P → USB3_CTX_L_DRX_N3

EU15

USB3_CRX_L_DTX_P3 / USB3_CRX_L_DTX_N3 / USB3_CTX_L_DRX_P3 / USB3_CTX_L_DRX_N3 ↔ USB3_CRX_L_DTX_P3 / USB3_CRX_L_DTX_N3 / USB3_CTX_L_DRX_P3 / USB3_CTX_L_DRX_N3

S DIO(BR) AZ1045-04F.R7G DFN2510P10E ESD
TYPEC@ESD@

+CCG_VBUS → TYPEC@CT3964 10U_0603_25V6M

+CCG_VBUS → L3ESD24VC3-2SC6 @ESD@

+3VALW → C6672 10P_0402_50V8J @ → +5VALW

+3VALW → C6673 10P_0402_50V8J @ → +5VALW

Cross Moat Cap
DSC Only

POP
EMI@/TYPEC@/TYPEC@EMI@/TYPEC@ESD@
UNPOP
CCG5C@/@EMI@/CCG5C@EMI@/@ESD@/CCG5C@RF@

USB3 CRX DTX P3

<12> USB3_CRX_DTX_P3 → USB3_CRX_DTX_P3 → RT1440 0_0402_5% (TYPEC@EMI@) → LT14@EMI@ → USB3_CRX_L_DTX_P3

USB3 CRX DTX N3

<12> USB3_CRX_DTX_N3 → USB3_CRX_DTX_N3 → RT1435 0_0402_5% (TYPEC@EMI@) → HCM1012GH900BP_4P → USB3_CRX_L_DTX_N3

USB3 CTX DRX P4

<12> USB3_CTX_DRX_P4 → USB3_CTX_DRX_P4 → CU25 0.1U_0402_10V7K TYPEC@ → USB3_CTX_C_DRX_P4 → RT1438 0_0402_5% (TYPEC@EMI@) → HCM1012GH900BP_4P → LT15@EMI@ → USB3_CTX_L_DRX_P4

USB3 CTX DRX N4

<12> USB3_CTX_DRX_N4 → USB3_CTX_DRX_N4 → CU24 0.1U_0402_10V7K TYPEC@ → USB3_CTX_C_DRX_N4 → RT1433 0_0402_5% (TYPEC@EMI@) → USB3_CTX_L_DRX_N4

USB3 CRX DTX P4

<12> USB3_CRX_DTX_P4 → USB3_CRX_DTX_P4 → RT1437 0_0402_5% (TYPEC@EMI@) → HCM1012GH900BP_4P → LT16@EMI@ → USB3_CRX_L_DTX_P4

USB3 CRX DTX N4

<12> USB3_CRX_DTX_N4 → USB3_CRX_DTX_N4 → RT1436 0_0402_5% (TYPEC@EMI@) → USB3_CRX_L_DTX_N4

USB20 N4 / USB20 P4

<12> USB20_N4 → USB20_N4 → RT74 1 @EMI@ 2 0_0201_5% → DLM0NSN900HY2D_4P → USB20_N4_R

<12> USB20_P4 → USB20_P4 → LT2 TYPEC@EMI@ → RT75 1 @EMI@ 2 0_0201_5% → USB20_P4_R

TYPE-C

+CCG_VBUS → JUSBC1 (JAE_DX07S024JJ2R1300-D CONN@)

A1	GND1	GND3	B12
A2	SSTXP1	SSRXP1	B11
A3	SSTXN1	SSRXN1	B10
A4	VBUS1	VBUS3	B9
A5	CC1	SUB2	B8
A6	DP1	DN2	B7
A7	DN1	DP2	B6
A8	SUB1	CC2	B5
A9	VBUS2	VBUS4	B4
A10	SSRXN2	SSTXN2	B3
A11	SSRXP2	SSTXP2	B2
A12	GND2	GND4	B1
1	GND5	GND8	4
2	GND6	GND9	5
3	GND7	GND10	6

TOP / Bottom

USB3_CTX_L_DRX_P3 / USB3_CTX_L_DRX_N3 → CT3962 2 1 0.47U_0402_50V6K TYPEC@ → TYPEC_CC1 <50>

USB20_P4_R / USB20_N4_R

RT1275 2 TYPEC@1 1M_0201_5%

USB3_CTX_L_DRX_N4 / USB3_CTX_L_DRX_P4 → DVT1 → CT3963 2 1 0.47U_0402_50V6K TYPEC@

USB20_P4_R / USB20_N4_R → EU14 AZC199-02SPR7G_SOT23-3 TYPEC@ESD@

USB3_CRX_L_DTX_P3 / USB3_CRX_L_DTX_N3 → CT3960 1 2 0.47U_0402_50V6K TYPEC@ → 1M_0201_5% 1 TYPEC@2 RT1276

USB20_N4_R / USB20_P4_R

TYPEC_CC2 <50> → CT3961 1 2 0.47U_0402_50V6K TYPEC@

USB3_CRX_L_DTX_N4 / USB3_CRX_L_DTX_P4 → DVT1

TYPEC_CC1 / TYPEC_CC2 → EU13 AZC199-02SPR7G_SOT23-3 TYPEC@ESD@

JAE_DX07S024JJ2R1300-D
CONN@

EU12

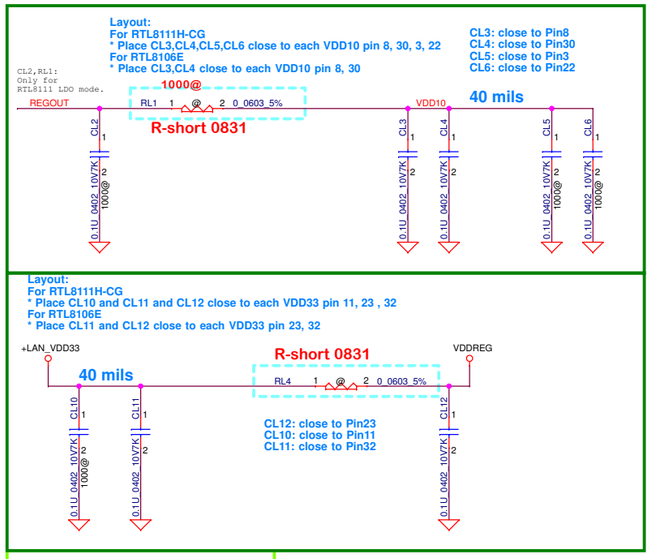
USB3_CTX_L_DRX_P4 / USB3_CTX_L_DRX_N4 / USB3_CRX_L_DTX_P4 / USB3_CRX_L_DTX_N4 ↔ USB3_CTX_L_DRX_P4 / USB3_CTX_L_DRX_N4 / USB3_CRX_L_DTX_P4 / USB3_CRX_L_DTX_N4

S DIO(BR) AZ1045-04F.R7G DFN2510P10E ESD
TYPEC@ESD@

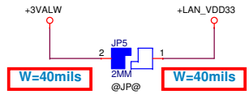
Security Classification	Compal Secret Data		
Issued Date	2018/12/24	Deciphered Date	2018/12/31

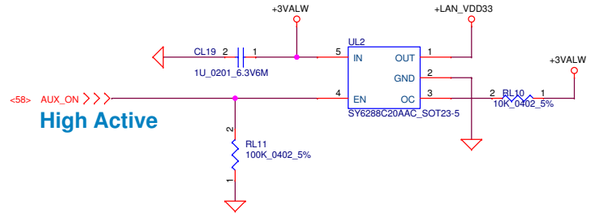
Compal Electronics, Inc.			
Title: TYPE-C Power Path			
Size	Document Number: LA-K033P		Rev: 1.0
Date: Friday, September 11, 2020	Sheet 50 of 101		

Main Func = LAN



+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

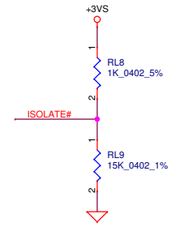


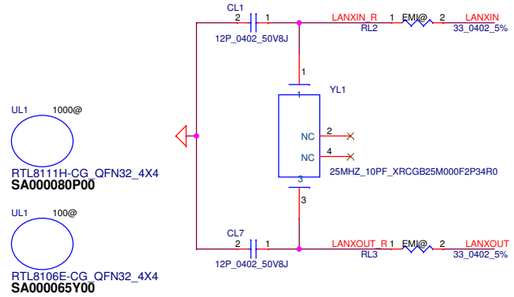


	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

LAN CHIP 10/100/1000

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M

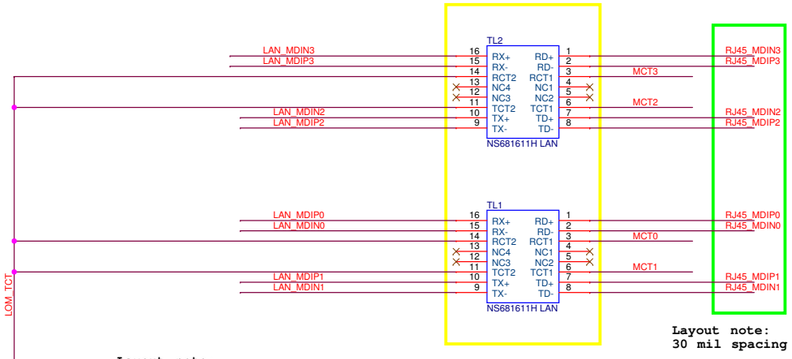




"PCIE_WAKE#" PU 1k on CPU side

Main Func = LAN

LAN TransFormer 10/100M x2

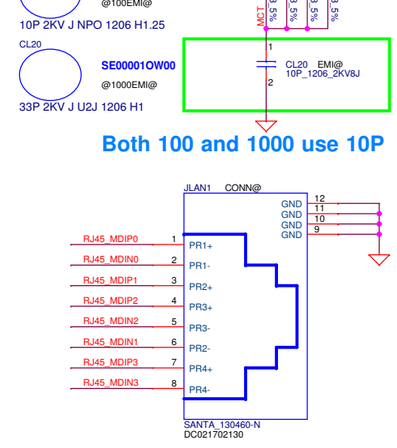


TL1 TOP, TL2 BOT

Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



Main:
SP050009800, S X'FORM_ NS681611H LAN
2nd:
SP050006H00, S X'FORM_ NS0014 LF LAN
3rd:
SP050006W00, S X'FORM_ HD-245 10/100 PC CARD LAN

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: LAN RTL8111/RTL8106

Size: Custom | Document Number: LA-K033P | Rev: 0.3

Date: Thursday, September 17, 2020 | Sheet 51 of 101

Main Func = WLAN

E Key CONN

+3VALW_PCH — 1A — +3.3V_WLAN

RW1 1 @ 2 0_0603_5%

R-short 0831

+3.3V_WLAN

CW1 10U_0402_6.3V6M

CW2 0.1U_0402_10V7K

CW3 0.1U_0402_10V7K

CW4 RF@ 10P_0402_50V8J

JWLAN1

<12> USB20_P10	3	USB_D+	
<12> USB20_N10	5	USB_D-	
	7	GND2	
<13> CNV_CRX_DTX_N1	9	SDIO_CLK	
<13> CNV_CRX_DTX_P1	11	SDIO_CMD	
	13	SDIO_DAT0	
<13> CNV_CRX_DTX_N0	15	SDIO_DAT1	
<13> CNV_CRX_DTX_P0	17	SDIO_DAT2	
	19	SDIO_DAT3	
<13> CLK_CNV_CRX_DTX_N	21	SDIO_WAKE#	
<13> CLK_CNV_CRX_DTX_P	23	SDIO_RESET#	
<12> PCIE_CTX_DRX_P10	33	GND4	
<12> PCIE_CTX_DRX_N10	35	PETp0	
	37	PETn0	
<12> PCIE_CRX_DTX_P10	39	GND5	
<12> PCIE_CRX_DTX_N10	41	PERp0	
	43	PERn0	
<11> CLK_PCIE_P1	45	GND6	
<11> CLK_PCIE_N1	47	REFCLKP0	
	49	REFCLKN0	
<11> CLKREQ_PCIE#1	51	GND7	
<11,51,58,68> PCIE_WAKE#	53	CLKREQ0#	
	55	PEWAKE0#	
	57	GND8	
<13> CNV_CTX_DRX_N1	59	RESERVED/PETp1	
<13> CNV_CTX_DRX_P1	61	RESERVED/PETn1	
	63	GND9	
<13> CNV_CTX_DRX_N0	65	RESERVED/PERp1	
<13> CNV_CTX_DRX_P0	67	RESERVED/PERn1	
	69	GND10	
<13> CLK_CNV_CTX_DRX_N	71	RESERVED/REFCLKP1	
<13> CLK_CNV_CTX_DRX_P	73	RESERVED/REFCLKN1	
	75	GND11	

	2	3.3V1	+3.3V_WLAN
	4	3.3V2	
	6	LED1#	TP51
	8	PCM_CLK/I2S_SCK	
	10	PCM_SYNC/I2S_WS	CNV_RF_RESET# <13>
	12	PCM_IN/I2S_SD_IN	
	14	PCM_OUT/I2S_SD_OUT	CLKREQ_CNV# <13>
	16	LED2#	TP52
	18	GND3	
	20	UART_WAKE#	
CNV_BRI_CRX_DTX_R	22	UART_RXD	
CNV_RGI_CTX_DRX_R	32	UART_TXD	
CNV_RGI_CRX_DTX_R	34	UART_CTS	
CNV_BRI_CTX_DRX_R	36	UART_RTS	
	38	VENDER_DEFINED1	
	40	VENDOR_DEFINED2	
	42	VENDOR_DEFINED3	
	44	COEX3	
	46	COEX2	
	48	COEX1	
WLAN_SUSCLK	50	SUSCLK(32kHz)	
BT_RADIO_DIS#_R	52	PERST0#	
WLAN_RF_DIS#_R	54	W_DISABLE2#	
	56	W_DISABLE1#	
	58	I2C_DATA	
	60	I2C_CLK	
	62	ALERT#	
	64	RESERVED	TP125
	66	UIM_SWP/PERST1#	
	68	UIM_POWER_SNK/CLKREQ1#	+3.3V_WLAN
	70	UIM_POWER_SRC/GPIO1/PEWAKE1#	
	72	3.3V3	
	74	3.3V4	
	76	GND12	
	77	GND13	

CONN@ LOTES_APCI0136-P001A

1.8V

CNV_BRI_CRX_DTX_R — RW3 1 CNV@ 2 49.9_0201_1% — CNV_BRI_CRX_DTX <13>

RW4 1 @ 2 0_0201_5% — HOST_DEBUG_TX <58>

CNV_RGI_CTX_DRX_R — RW5 1 CNV@ 2 0_0201_5% — CNV_RGI_CTX_DRX <13>

CNV_RGI_CRX_DTX_R — RW6 1 CNV@ 2 49.9_0201_1% — CNV_RGI_CRX_DTX <13>

CNV_BRI_CTX_DRX_R — RW7 1 CNV@ 2 0_0201_5% — CNV_BRI_CTX_DRX <13>

RW5,RW7 close to CPU

WLAN_SUSCLK — RW24 1 2 0_0402_5% — SUSCLK_R — SUSCLK_R <11,58>

BT_RADIO_DIS#_R — RC4123 1 @ 2 0_0201_5% — PLTRST# <11,27,51,66,68>

WLAN_RF_DIS#_R — RC4124 1 @ 2 0_0201_5% — BT_RADIO_DIS# <10>

WLAN_RF_DIS# <12>

0.1U_0201_10V6K CW5 1 2 PCIE_CTX_C_DRX_P10

0.1U_0201_10V6K CW6 1 2 PCIE_CTX_C_DRX_N10

R-Short 0831

RW8 1 @ 2 0_0201_5% CLKREQ_PCIE#1_R

RW10 1 @ 2 0_0201_5% PCIE_WAKE#_R

Security Classification	Compal Secret Data	
Issued Date	2018/04/01	Deciphered Date 2019/04/01

Compal Electronics, Inc.

Title: NGFF_WLAN CONN

Size | Document Number: LA-K033P | Rev: 1.0

Date: Friday, September 11, 2020 | Sheet 52 of 101

Main Function: WIGIG / WIDI

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **WIGIG / WIDI(RSVD)**

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 53 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 54 of 101	

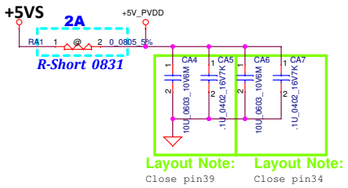
Main Function:

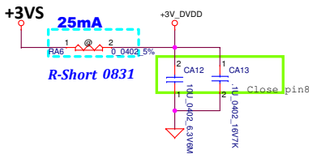
Reserve

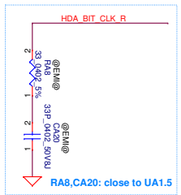
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

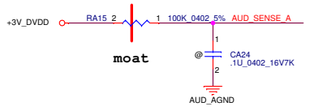
Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 55 of 101	

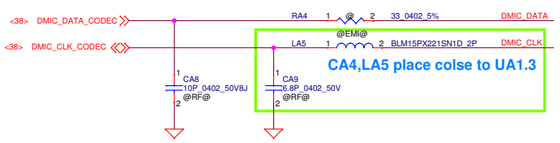
Main Func = Audio

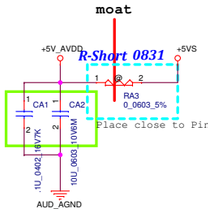


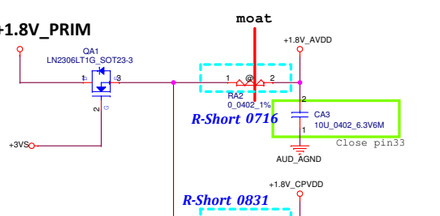


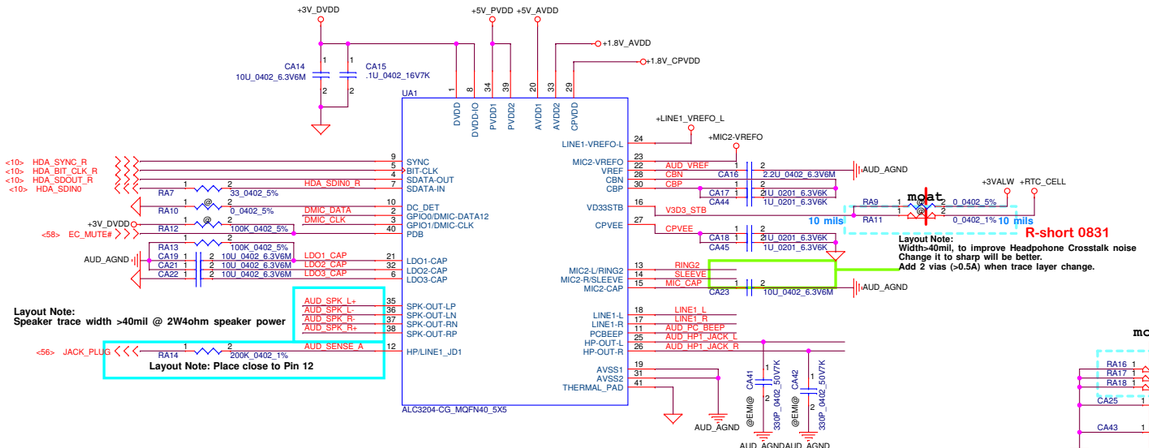


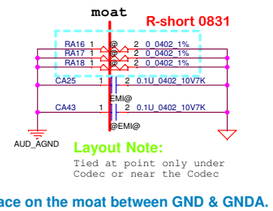




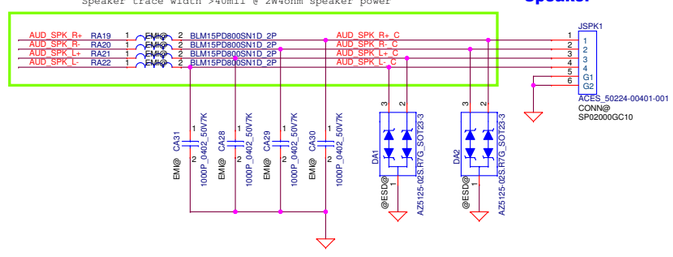




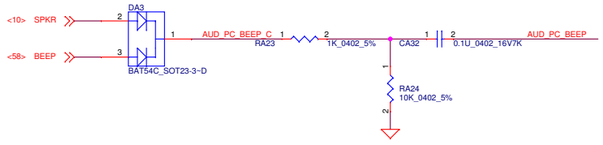


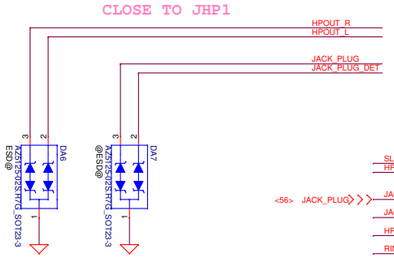


Place on the moat between GND & GNDA.



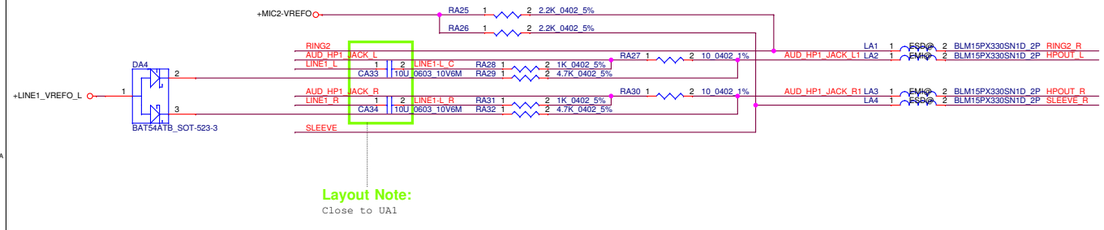
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



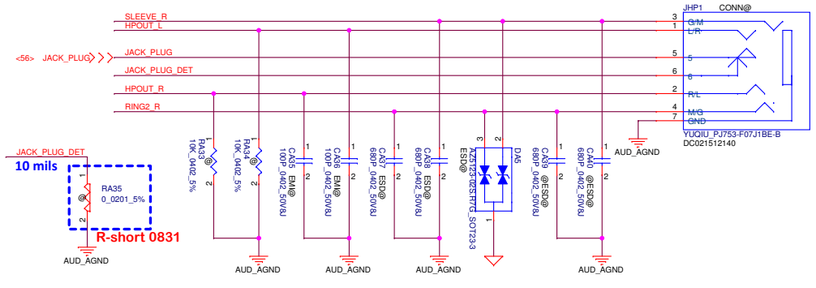


Main Func = Audio Jack

Universal Jack
(Global Headset Jack + mic phone in + line in support)



Universal Jack
(Global Headset Jack + mic phone in + line in support)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title: Audio Codec ALC3204
				Size: — Document Number: LA-K033P Rev: 1.0
				Date: Friday, September 11, 2020 Sheet 56 of 101

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **(RSVD)**

Size	Document Number	Rev
	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 57 of 101

Main Func = EC

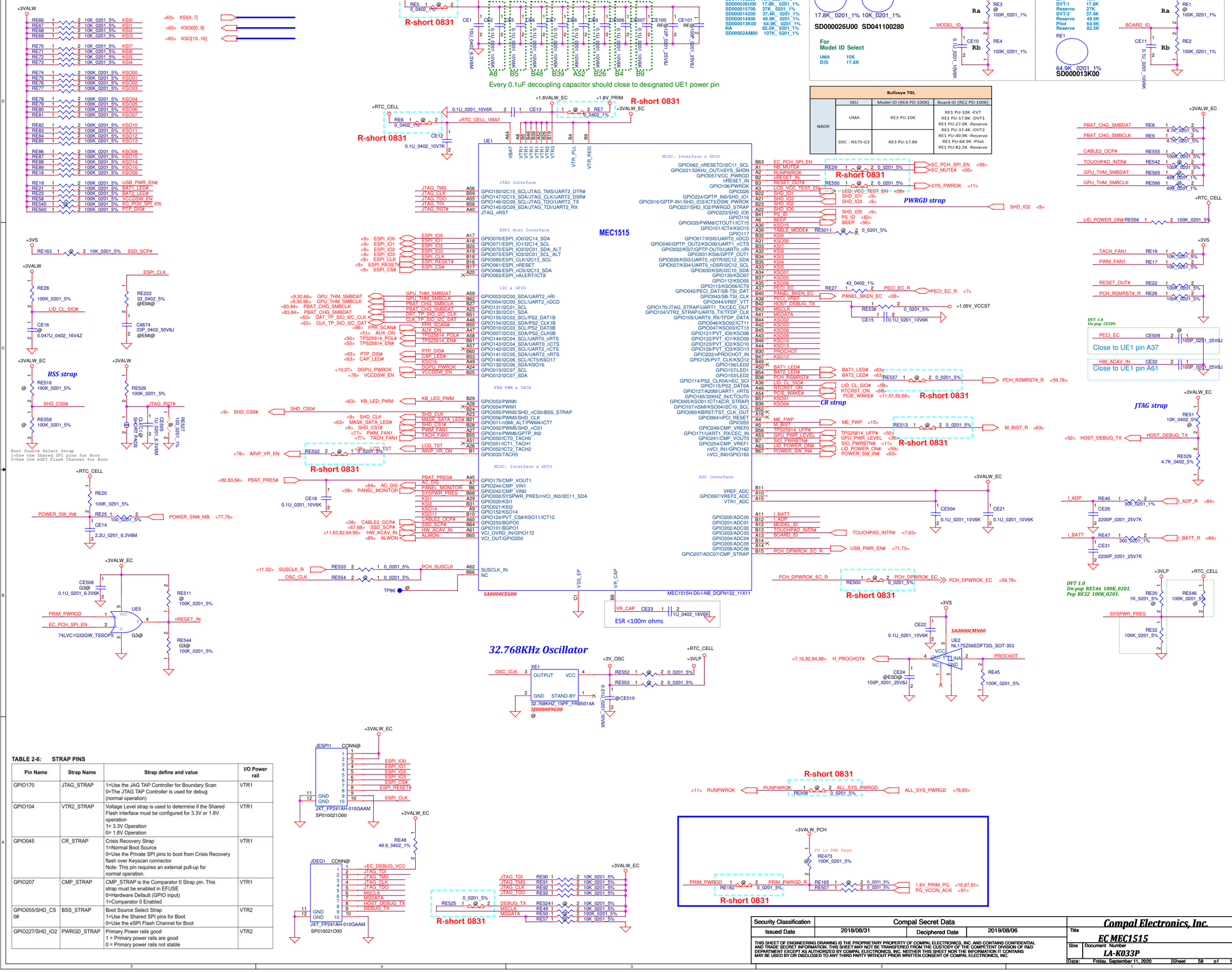
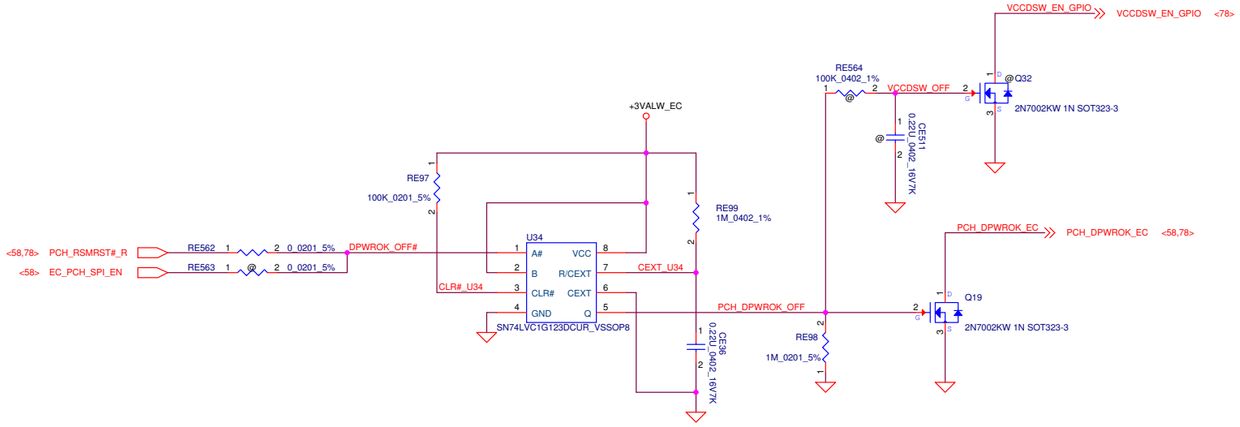


TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO170	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VTR1
GPIO104	VTR2_STRAP	Voltage Level strap is used to determine if the Shared Flash interface must be configured for 3.3V or 1.8V operation 1= 3.3V Operation 0= 1.8V Operation	VTR1
GPIO045	CR_STRAP	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Keyscan connector Note: This pin requires an external pull-up for normal operation.	VTR1
GPIO207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in EFUSE 0=Hardware Default (GPIO input) 1=Comparator 0 Enabled	VTR1
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot	VTR2
GPIO227/SHD_IO2	PWRGD_STRAP	Primary Power rails good 1 = Primary power rails are good 0 = Primary power rails not stable	VTR2

Main Function: WDT circuit



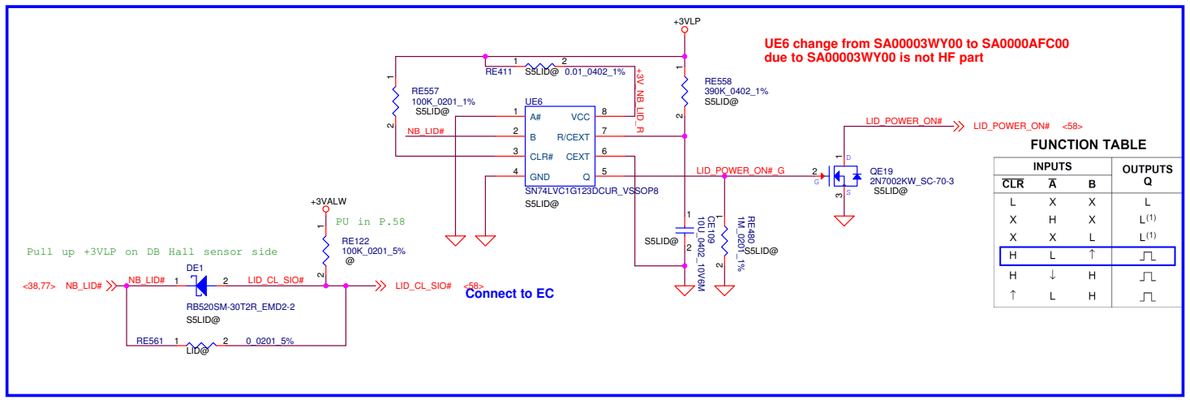
FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

t_wOUT(2)		Q	C_{ext} = 28 pF, R_{ext} = 2 kΩ	225	600	190	220	170	200	150	180	ns
			C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	100	110	100	110	100	110	100	110	µs
			C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	1	1.1	1	1.1	1	1.1	1	1.1	ms

Main Function: S5 LID

S5 LID OPEN POWER ON



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 59 of 101	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	(RSVD)		
Size	Document Number LA-K033P		Rev 1.0
Date: Friday, September 11, 2020	Sheet 60 of 101		

Main Function:SMB/I2C Block Diagrams

4-1. General Specifications

The contents provide general characteristics for the model LP156WFD.

	Item	Spec	Notes
General Specification	System	Self Capacitive type	
	Multi Touch Points	10 points	
	Active touch area	Same as LCD A/A	
	Sensor Type.	Advanced In-Cell Touch	
	Sensor Channel Pitch	4.50mm (X) x 5.36mm(Y)	
	IC	MIT-410	Melfas
	Firmware	01.00	
	Slave **Address**	0x10	
	PID	8010	
	VID	1FD2	
	Number of Sensor Channel	80ea (X) x 36ea (Y)	
	Interface	HID over I2C	

I2C Address:0x10

JeDP CONN
For Touch Screen

USB20_P8_R — 0 ohm — I2C_0_LCD_SCL
USB20_N8_R — 0 ohm — I2C_0_LCD_SDA

+3VS — 4.7k ohm — 4.7k ohm
+3VS — @ 2.2k ohm — @ 2.2k ohm

I2C_0_SCL DV18 — I2C0_SCL
I2C_0_SDA DW18 — I2C0_SDA

I2C Address: 0x2C
0b0101 100 + R/W

JTP CONN
Touch PAD
I2C

+TP_VDD (+3VS) — 2.2k ohm — 2.2k ohm
+3VS — @ 2.2k ohm — @ 2.2k ohm

I2C_1_SCL_R — 0 ohm
I2C_1_SDA_R — 0 ohm

I2C_1_SCL DJ23 — I2C1_SCL
I2C_1_SDA DT18 — I2C1_SDA

- I^2C

The I^2C interface complies with I^2C Bus Specification, Version 2.1.
The device address is 0x2C.
I^2C clock rate: 400KHz

+3VS — @ 2.2k ohm — @ 2.2k ohm

Power Monitor
CONN

DJ23 I2C_2_SCL — I2C2_SCL
DT18 I2C_2_SDA — I2C2_SDA

I2C_1_SCL_R — 0 ohm
I2C_1_SDA_R — 0 ohm

+TP_VDD (+3VS) — 4.7k ohm — 4.7k ohm

JTP CONN
Touch PAD
PS2

DAT_TP_SIO_R — 0 ohm — DAT_TP_SIO_I2C_CLK
CLK_TP_SIO_R — 0 ohm — CLK_TP_SIO_I2C_DAT

TGL-U

ISH_I2C_0_SCL — DB45 ISH_I2C_0_SCL — @ 1k ohm — @ 1k ohm — +3VS
ISH_I2C_0_SDA — DB44 ISH_I2C_0_SDA — Reserved

ISH_I2C_1_SCL — CY39 ISH_I2C_1_SCL — 1k ohm — 1k ohm — +3VS
ISH_I2C_1_SDA — DB47 ISH_I2C_1_SDA

SCL / SDA — FreeFall Sensor LNG2DMTR LGA

FreeFall Sensor reserved
SMBus Address: 0101001b

The slave address (SAD) associated to the LNG2DM is 0101001xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I^2C lines.

SMBCLK — DK21 MEM_SMBCLK — 1k ohm — 1k ohm — +3VALW_PCH
SMBDATA — DM19 MEM_SMBDATA

2N7002KDW QC6

PCH_SMBCLK — 2.2k ohm — 2.2k ohm — +3VS
PCH_SMBDAT

SCL / SDA — XDP CONN

PCH_SMBCLK 253 — SCL — DIMMA — SDA 254 PCH_SMBDATA — DDR4

SMBus Address: 000

PCH_SMBCLK 253 — SCL — DIMMB — SDA 254 PCH_SMBDATA — DDR4

SMBus Address: 010

SML0CLK — DK19 SML0_SMBCLK — 499 ohm — 499 ohm — +3VALW_PCH
SML0DATA — DM17 SML0_SMBDATA — 0 ohm — 0 ohm — GPU_THM_SMBCLK / GPU_THM_SMBDAT

2N7002KDW Q11

2.2k ohm — 2.2k ohm — +3VS
THM_SML1_CLK 8
THM_SML1_DATA 7

Thermal Sensor NCT7718W

SML1CLK — DK17 SML1_SMBCLK — 1k ohm — 1k ohm — +3VALW_PCH
SML1DATA — DJ17 SML1_SMBDATA — Reserved for Type-C , TBT

PJT138KA QV2

I2CS_SCL D9
I2CS_SDA D8

GPU N17S-G3

2.2k ohm — 2.2k ohm — +1.8VS_DGPU_AON

6.3 Address Setting

NCT7718W I^2C/ SMBus™ address is 1001100xb (x is R/W bit).

SMBus Address: 1001100xb (x is R/W bit)

I2CS SMBUS: 0x9E(write) , 0x9F(read)
Debug Address: 0x96

13.3.2.1 I2CS Slave Address

The default I2CS address is 0x9E. This address can not be used by another device on the same bus. The GPU has an alternative I2CS address (0x9C) which is used when a second GPU is placed on the board. This alternative address is enable by using the SMB_ALT_ADDR strap. See Chapter "GPU Straps" for information regarding this strap. By using this alternative I2CS address, two GPUs on the board can be placed on the same I2CS bus.

Specification	Description
Base Address	• BAR0: 16 MB • BAR1: 256 MB • BAR2: 32 MB • I/O BAR: 4 KB
PCI Class Code	0x03 - Display Controller
PCI Sub-Class Code	0x02 - 3D Controller
ECC Support	Not Supported
SMBus (8-Bit Address)	0x9E (write), 0x9F (read) or 0x9C (write), 0x9D (read)

KBC MEC 1515

GPIO155 — GPIO004 — GPU_THM_SMBCLK
GPIO154 — GPIO003 — GPU_THM_SMBDAT

PBAT_CHG_SMBCLK — GPIO131
PBAT_CHG_SMBDAT — GPIO130

4.7K ohm — 4.7K ohm — +3VALW_EC

100 ohm — CLK_SMB — 7 — SCL
100 ohm — DAT_SMB — 6 — SDA

BATT CONN

7-bit Address:0x0B
0001011x x is R/W

0 ohm — 21 — SDA
0 ohm — 22 — SCL

Charger
ISL95522
PUB01

SMBus Address:0b00010011(resd)
0b00010010 (write)

System Management Bus (SMBus) Specification Version 3.0

Appendix C. SMBus Device Address Assignments

Table 17 lists the pre-assigned and reserved SMBus device assignments.

Table 17. Reserved and pre-assigned SMBus addresses

Slave Address Bits [7:1]	R/W# Bit [0]	Description	Specification
0000 000	0	General Call Address	I²C-Bus Specification And User Manual [RD1]
0000 000	1	START byte	I²C-Bus Specification And User Manual [RD1]
0000 001	X	CBUS address	I²C-Bus Specification And User Manual [RD1]
0000 010	X	Address reserved for different bus format	I²C-Bus Specification And User Manual [RD1]
0000 011	X	Reserved for future use	I²C-Bus Specification And User Manual [RD1]
0000 1XX	X	HS Mode Master Code	I²C-Bus Specification And User Manual [RD1]
0001 000	X	SMBus Host	System Management Bus Specification V 1.1, December 1998
0001 001	X	Smart Battery Charger	Smart Battery Charger Specification V 1.1, December 1998
0001 010	X	Smart Battery Selector Smart Battery System Manager	Smart Battery Selector Specification V 1.1, December 1998 Smart Battery System Manager Specification V 1.0B, August 1999
0001 011	X	Smart Battery	Smart Battery Data Specification V 1.1, December 1998
0001 100	X	SMBus Alert Response Address	System Management Bus Specification V 1.1, December 1998
0101 000	1	PMBus™ ZONE READ	PMBus Power System Management Protocol Specification, Part I, Revision 1.3
0101 100	X	Reserved by previous versions of the	

The ISL95522 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL95522 uses the SMBus Read Word and Write Word protocols shown in Figure 33 on page 32 to communicate with the host system and a smart battery. The ISL95522 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_:

Read address = 0b00010011(0X13H)
Write address = 0b00010010(0X12H)

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: SMB/I2C Block Diagrams

Size: — Document Number: LA-K033P — Rev: 1.0

Date: Friday, September 11, 2020 — Sheet 61 of 101

Main Function:

Reserve

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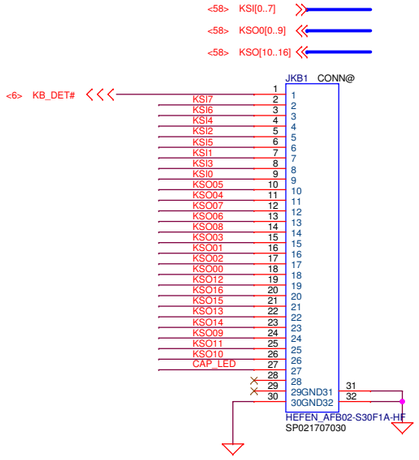
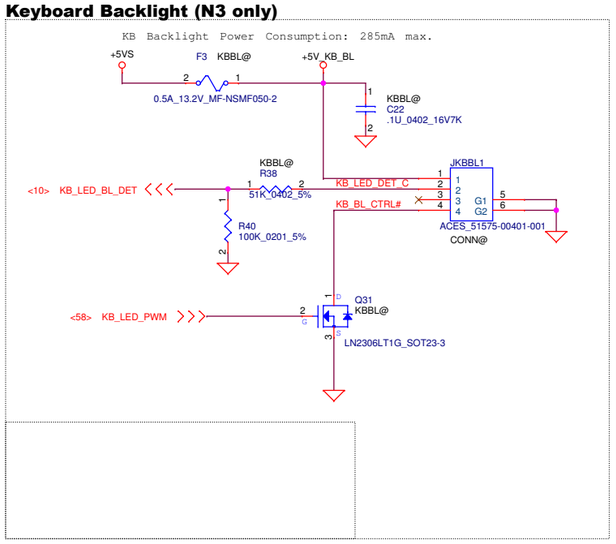
Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 62 of 101	

Main Func = KB

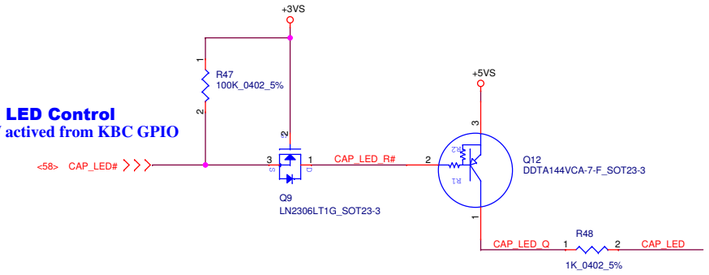


Keyboard Backlight (N3 only)

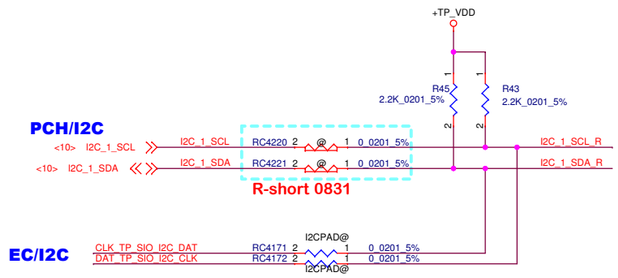


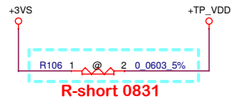
CAP LED Control

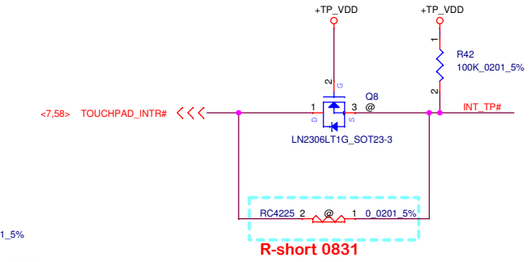
LOW actived from KBC GPIO



Main Func = TPAD

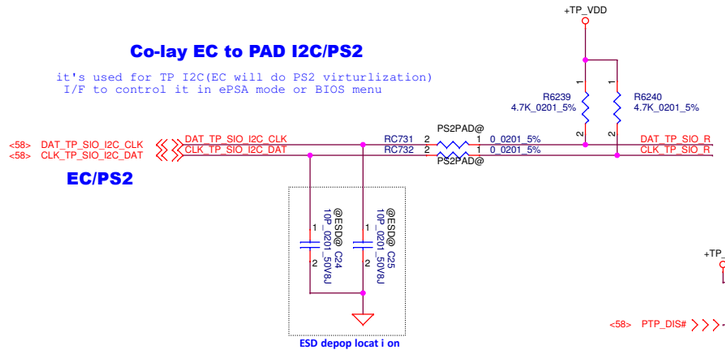


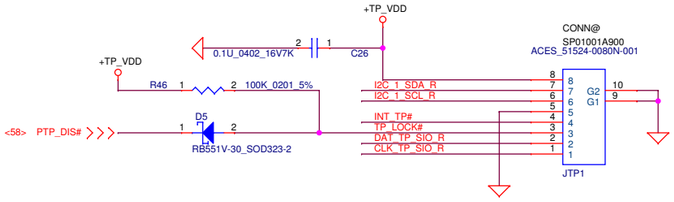




Co-lay EC to PAD I2C/PS2

it's used for TP I2C(EC will do PS2 virturlization)
I/F to control it in ePSA mode or BIOS menu

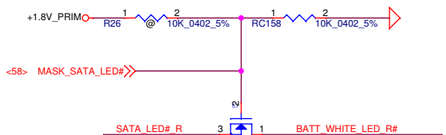


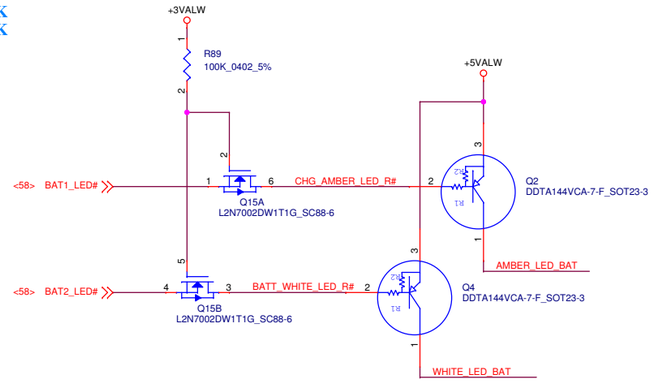


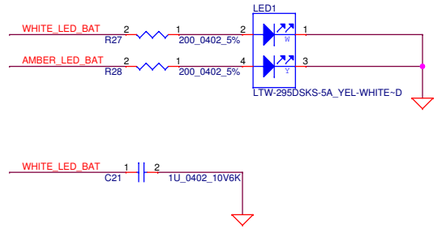
Main Func = Battery LED

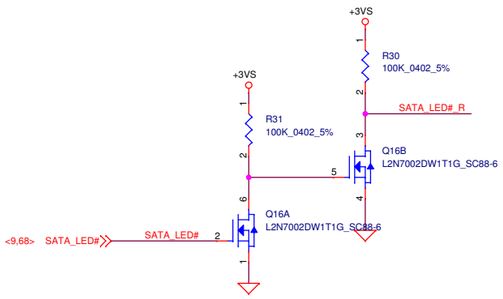
BJT
R1: 47 K
R2: 10 K

Low actived from KBC GPIO

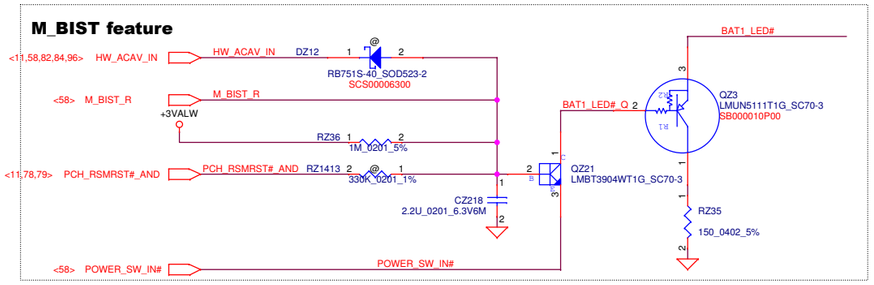








M_BIST feature



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Issued Date	2018/04/01	Deciphered Date	2019/04/01

Title	Compal Electronics, Inc.		
	Keyboard/Touch Pad/Thermal/FAN		
Size	Document Number		Rev
	LA-K033P		1.0
Date:	Friday, September 11, 2020	Sheet	63 of 101

Main Function:

Reserve

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Compal Electronics, Inc.		
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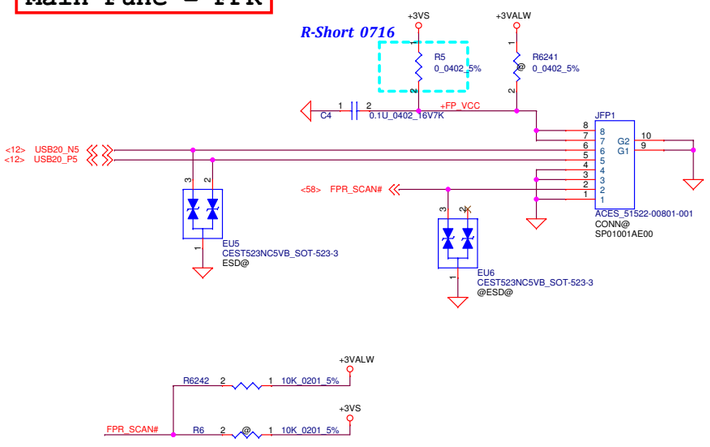
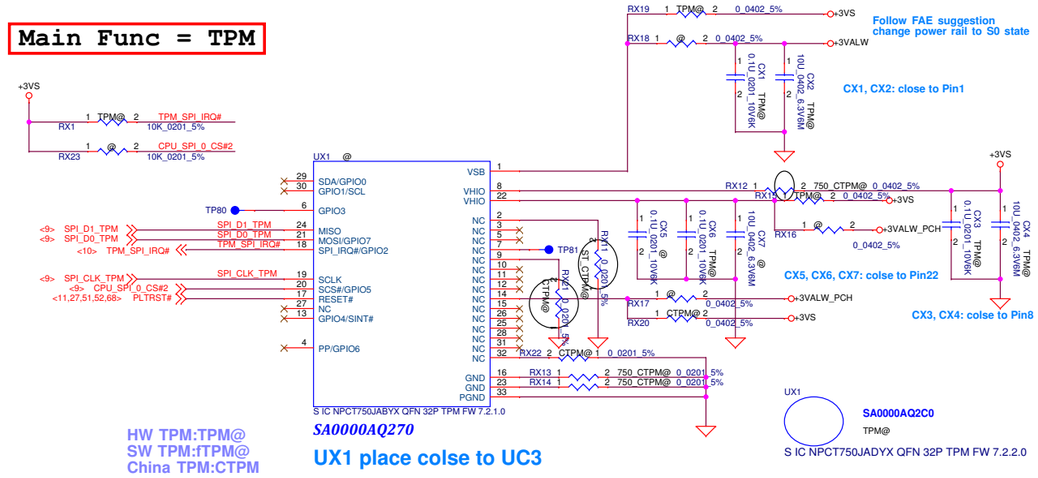
Main Func = FPR

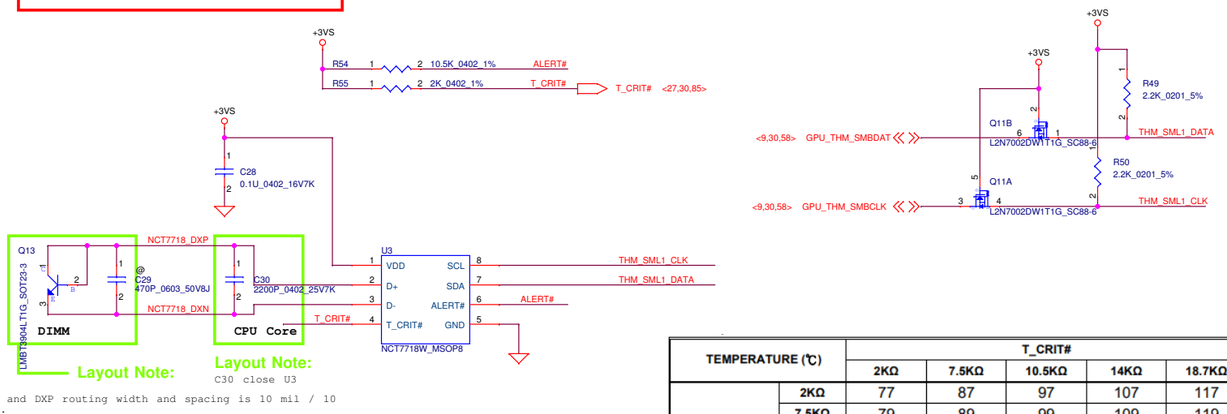


Main Func = OTP

Main Func = TPM



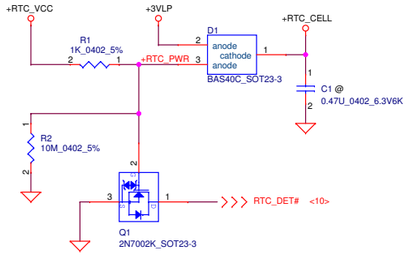
Main Func = Thermal

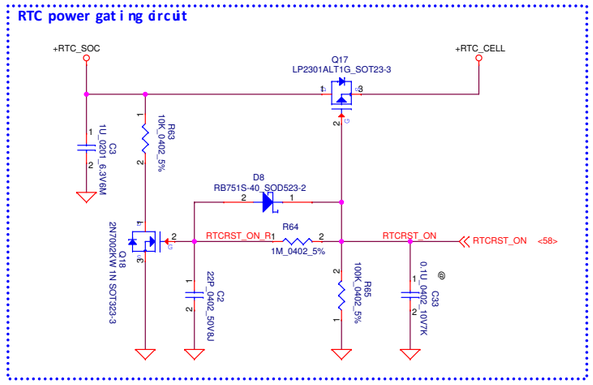


DXN and DXP routing width and spacing is 10 mil / 10 mil.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = RTC

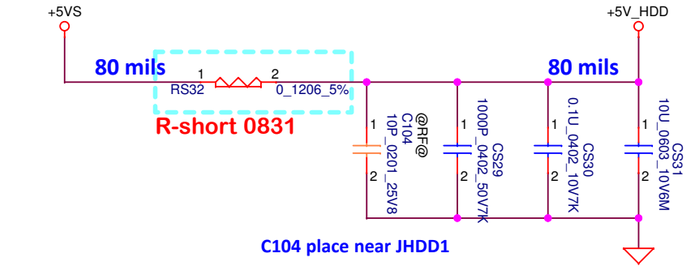


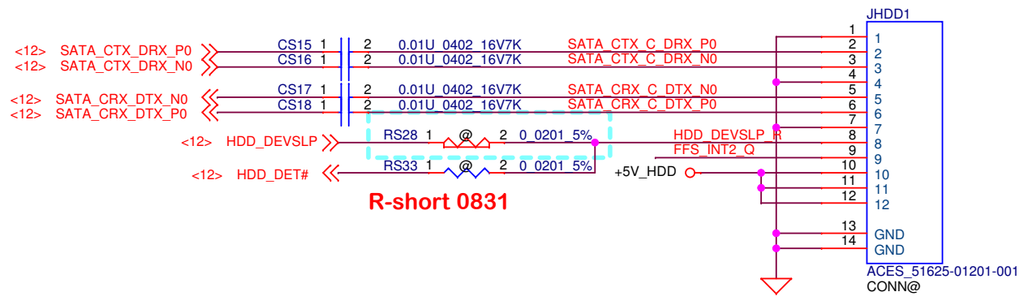


Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

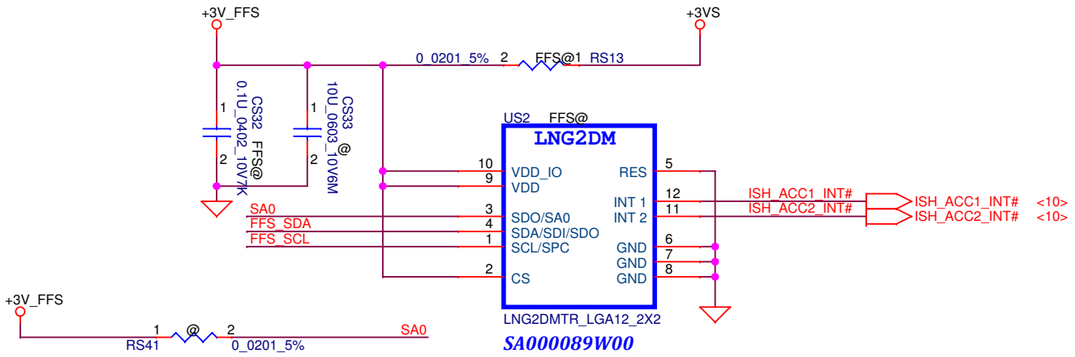
Compal Electronics, Inc.			
Title	TPM/RTC/Screw hole		
Size	Document Number LA-K033P		Rev 1.0
Date: Friday, September 11, 2020	Sheet 66 of 101		

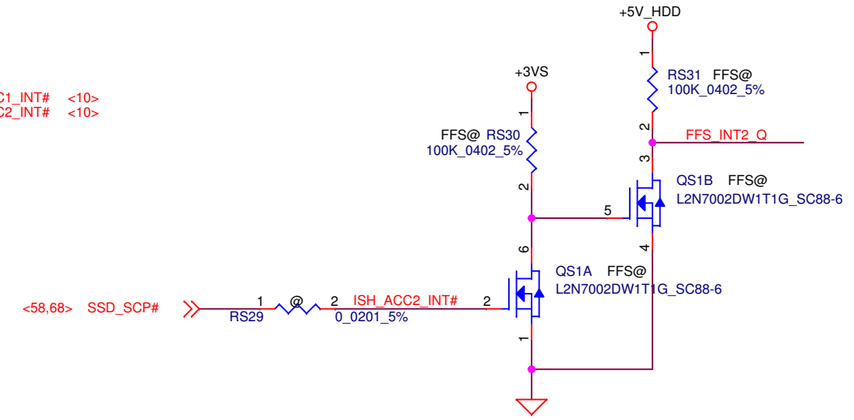
Main Func = HDD&FFS



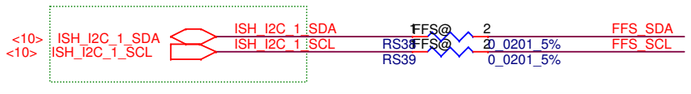


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

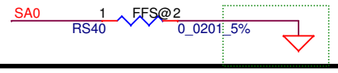




DVT 1.0
Change US2.1 and US2.4(SCL/SDA) connect from PCH_SMBCLK/PCH_SMBDATA to ISH_I2C_0_SCL/ISH_I2C_0_SDA.



DVT 1.0
Change US2.3 (SA0) connect from +3V_FFS to GND.



Main Func = ODD

Cancel ODD

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: HDD/FFS/ODD

Size: Custom | Document Number: LA-K033P | Rev: 1.0

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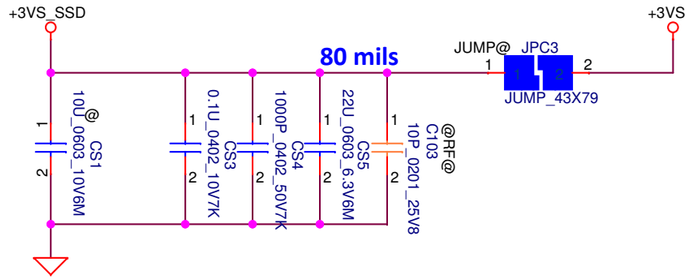
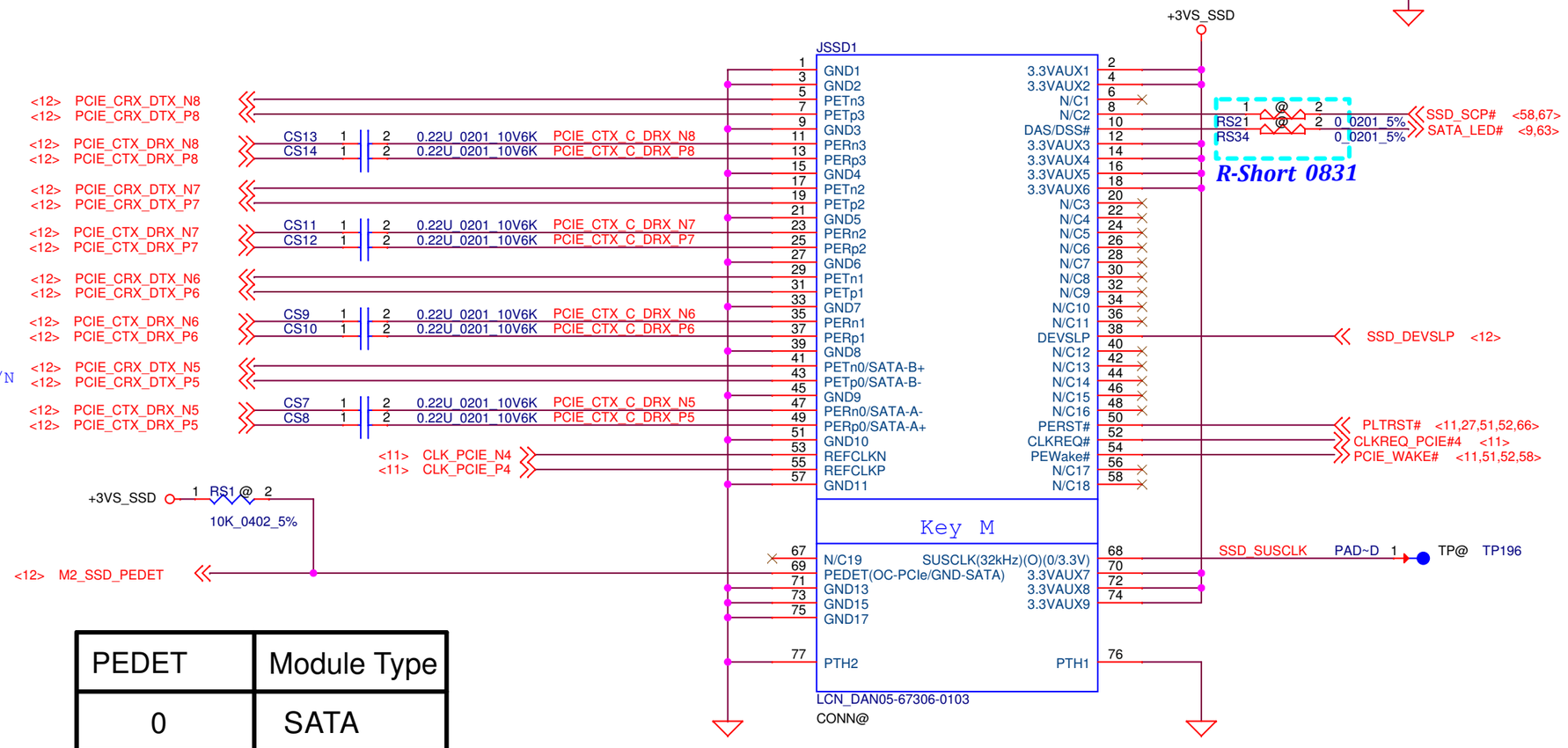
Main Func = SSD

M Key CONN

NGFF Key M





PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **NVME SSD**

Size	Document Number	Rev
	LA-K033P	1.0

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Main Func = eMMC

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Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: eMMC (RSVD)

Size | Document Number: LA-K033P | Rev: 1.0

Date: Friday, September 11, 2020 | Sheet 69 of 101

Main Function:

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Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	(RSVD)		
Size	Document Number LA-K033P		Rev 1.0
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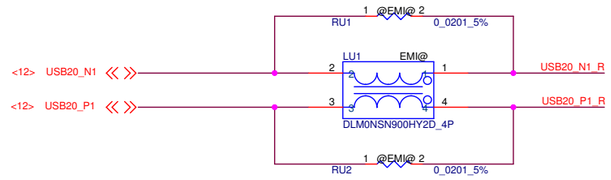
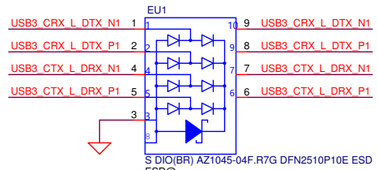
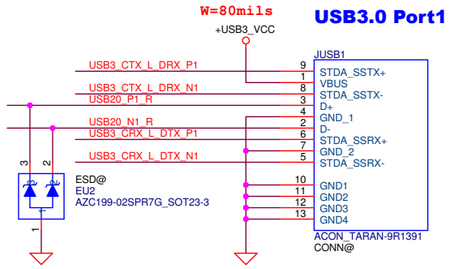
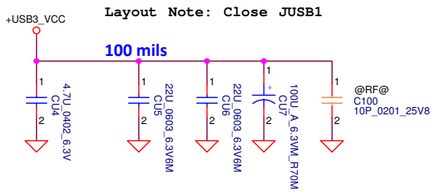
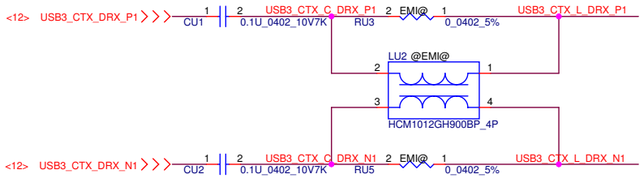
Main Func = USB3.0 Port1

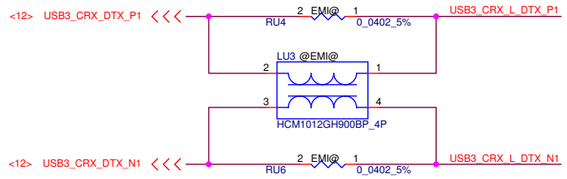




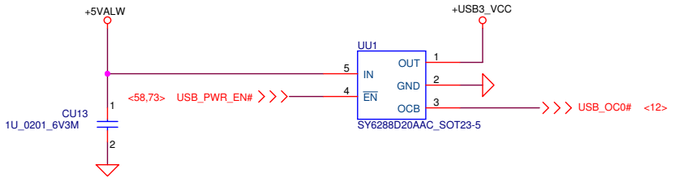




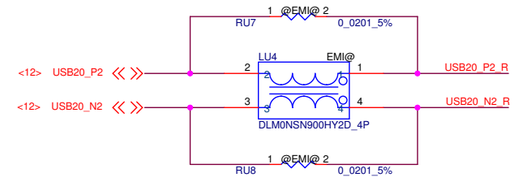


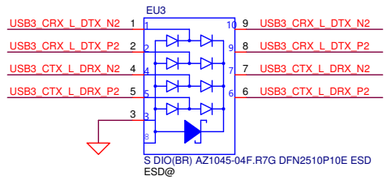


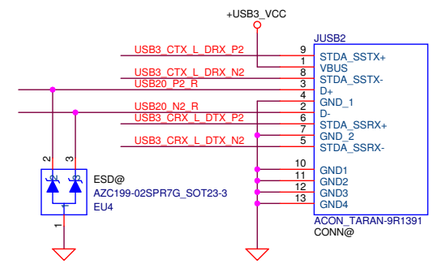
Maximum Output Current 2A

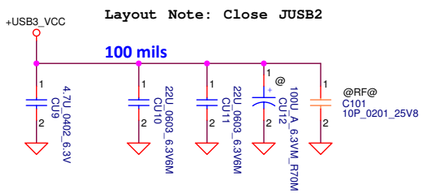


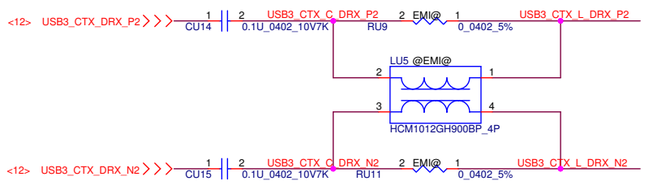
Main Func = USB3.0 Port2

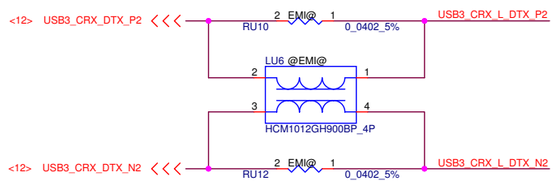












Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: USB3.0			
Size	Document Number: LA-K033P		Rev: 1.0
Date: Friday, September 11, 2020	Sheet 71 of 101		

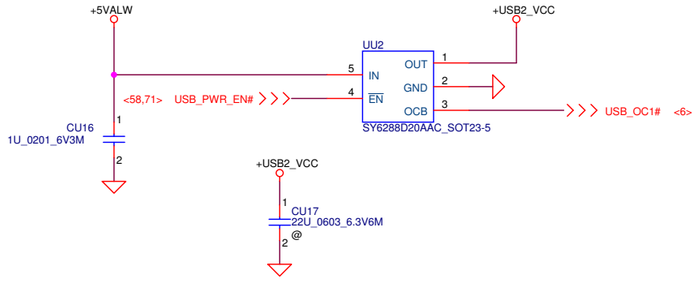
Main Function:

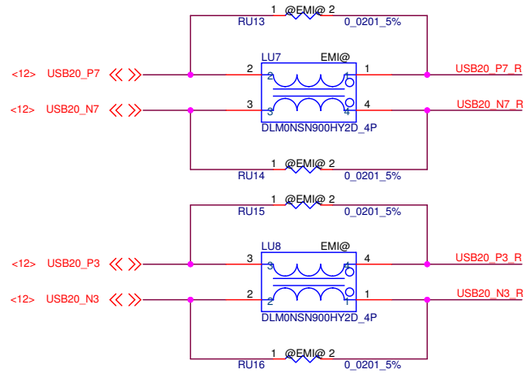
Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 72 of 101	

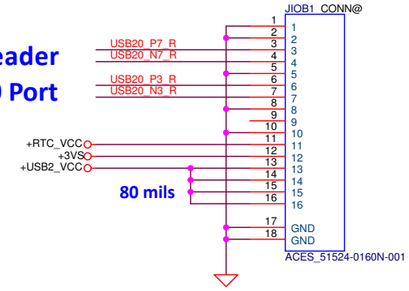
Main Func = USB2.0 Port3 + Card Reader on IO/B





USB2.0/Card Reader connector

CardReader
USB2.0 Port



	Compal Electronics, Inc.	
Title	Finger Print & I/O CONN	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 73 of 101	

Main Function:

Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **DOCK(RSVD)**

Size	Document Number	Rev
	LA-K033P	1.0

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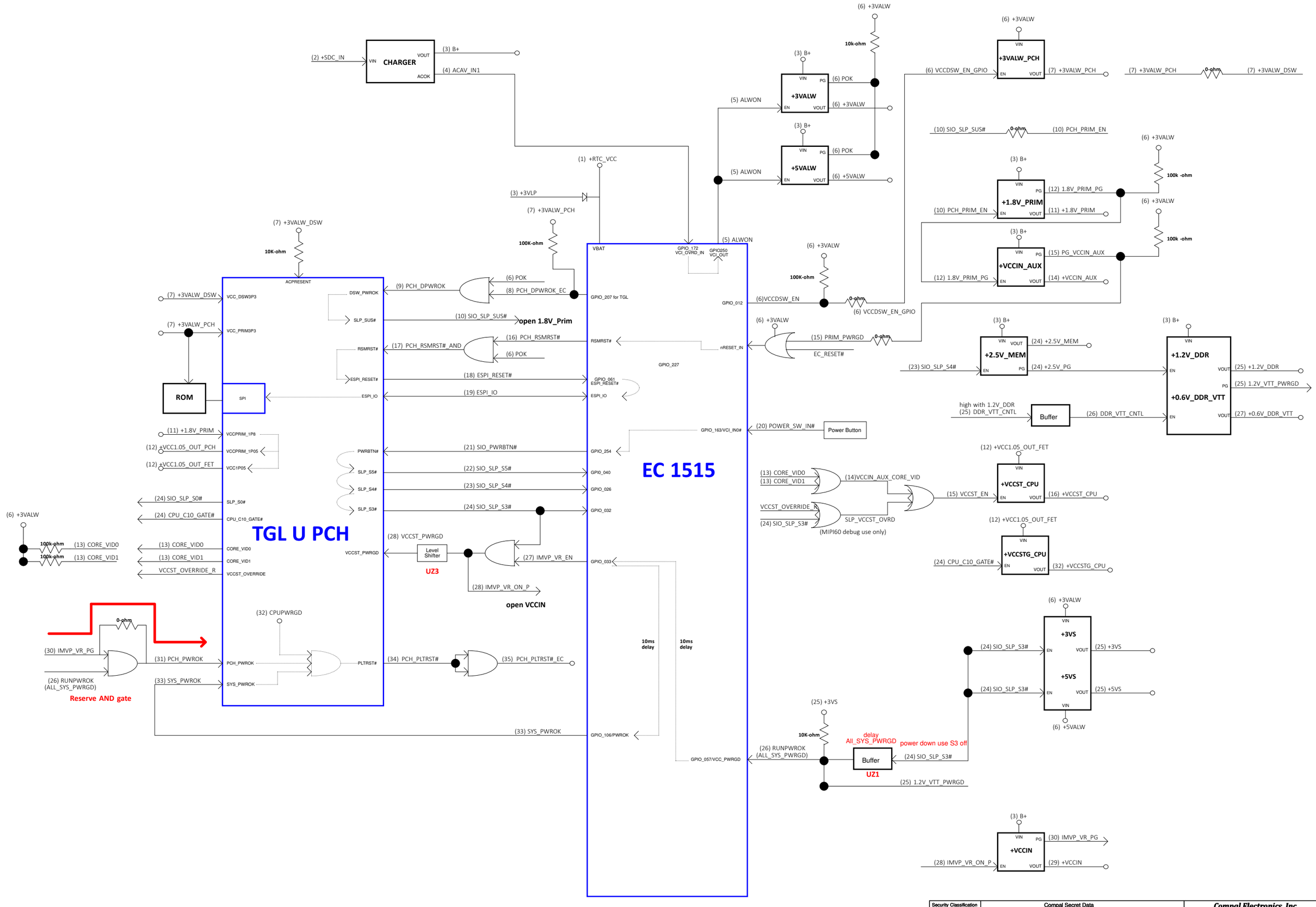

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/01	Deciphered Date 2019/04/01	Title (RSVD)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Document Number LA-K033P Rev 1.0
			Date: Friday, September 11, 2020 Sheet 75 of 101

Main Function:

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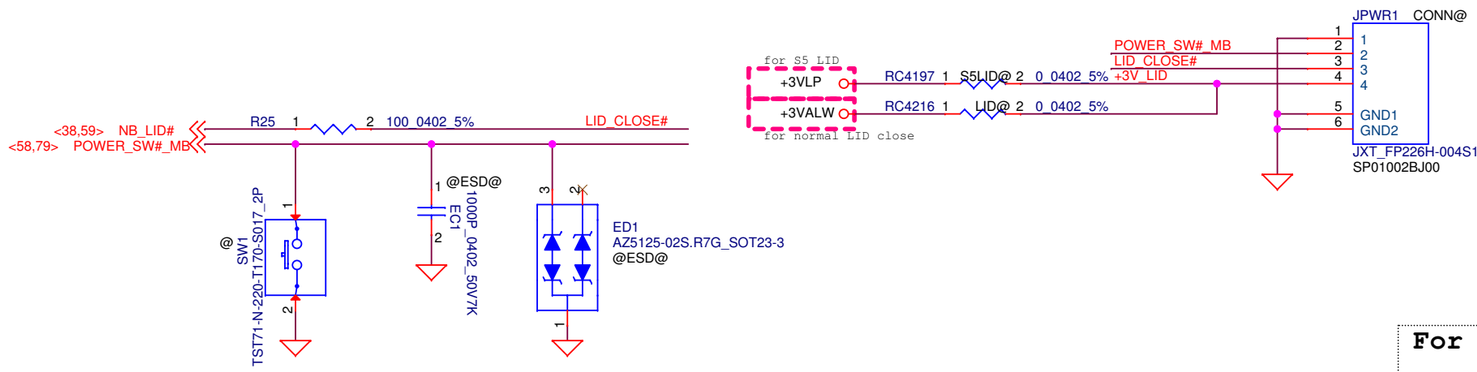
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

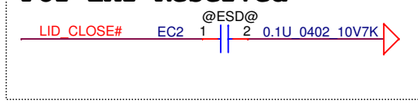
Compal Electronics, Inc.		
Title	(RSVD)	
Size	Document Number LA-K033P	Rev 1.0
Date: Friday, September 11, 2020	Sheet 76 of 101	

Main Func = Power BTN

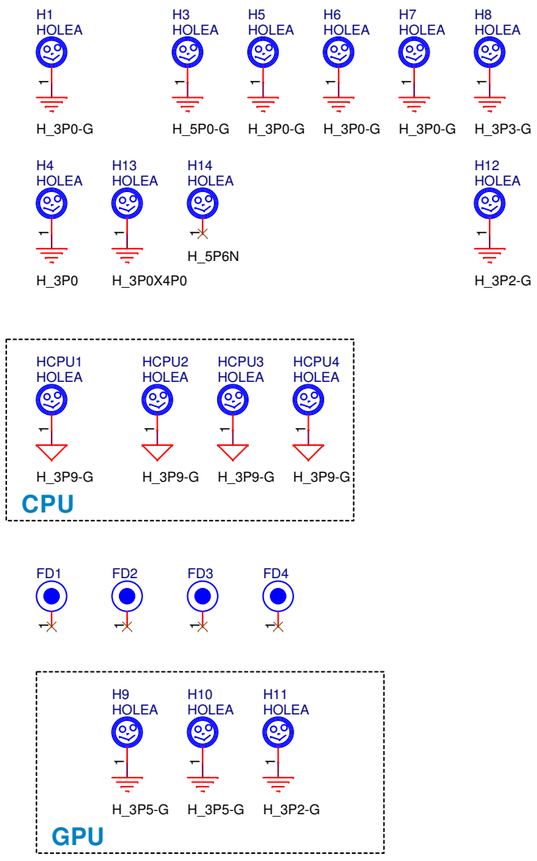
Low actived from KBC GPIO



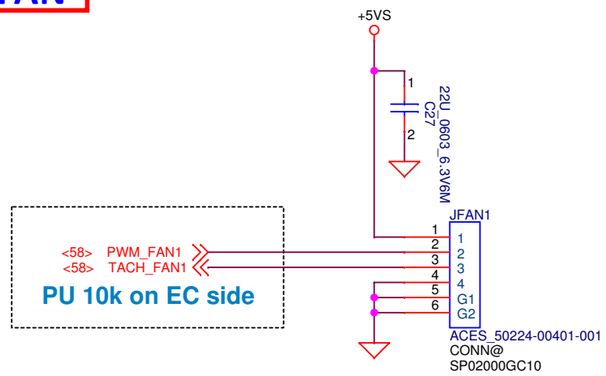
For EMI Reserved



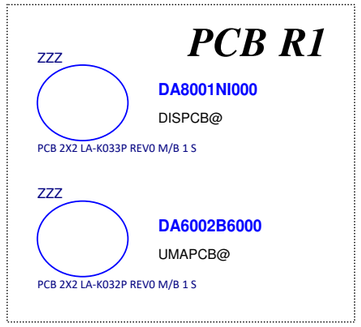
Screw hole/FD



FAN



PCB PN



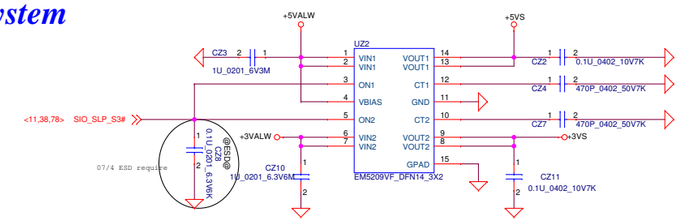
PCB R3

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

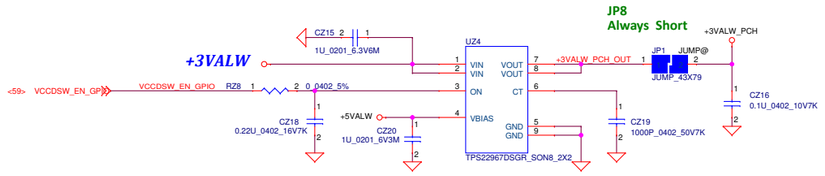
Compal Electronics, Inc.			
Title: PWRBTN/PCB PN//SCREW/FAN			
Size	Document Number: LA-K033P		Rev: 1.0
Date: Friday, September 11, 2020		Sheet 77 of 101	

Main Func = DC/DC

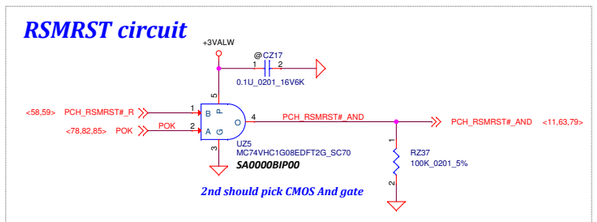
+5VS / +3VS for System



+3VALW TO +3VALW_PCH

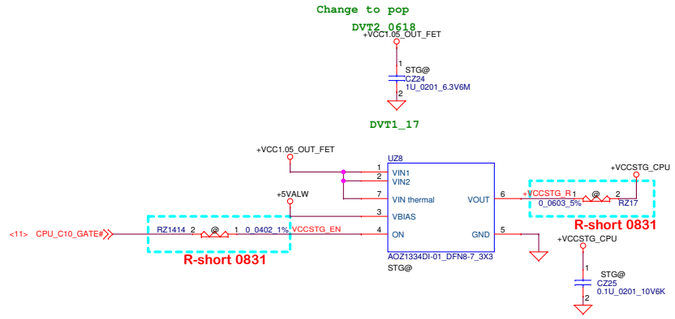


RSMRST circuit



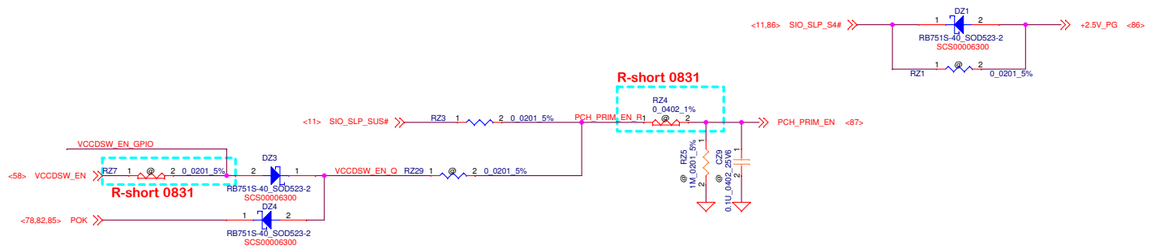
Change to pop

VCCSTG

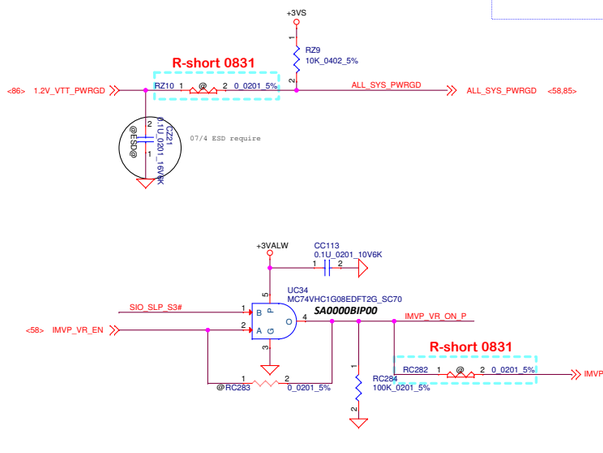


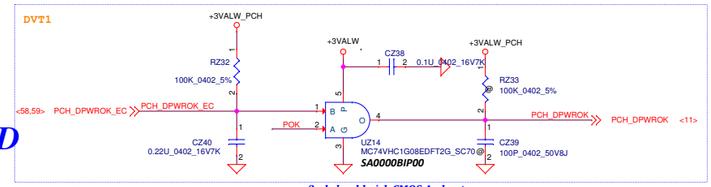
+1.2V_VDDQ TO +1.2V_VCCPLL_OC

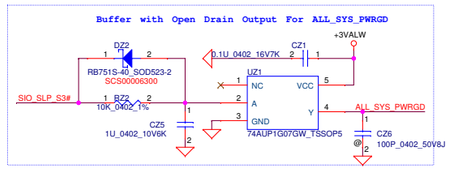
Sequence Logic

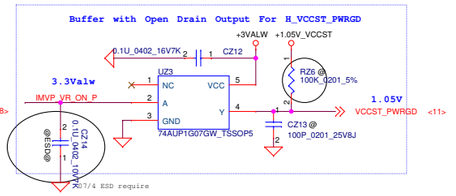


IMVP_VR_ON&VCCST_PWRGD

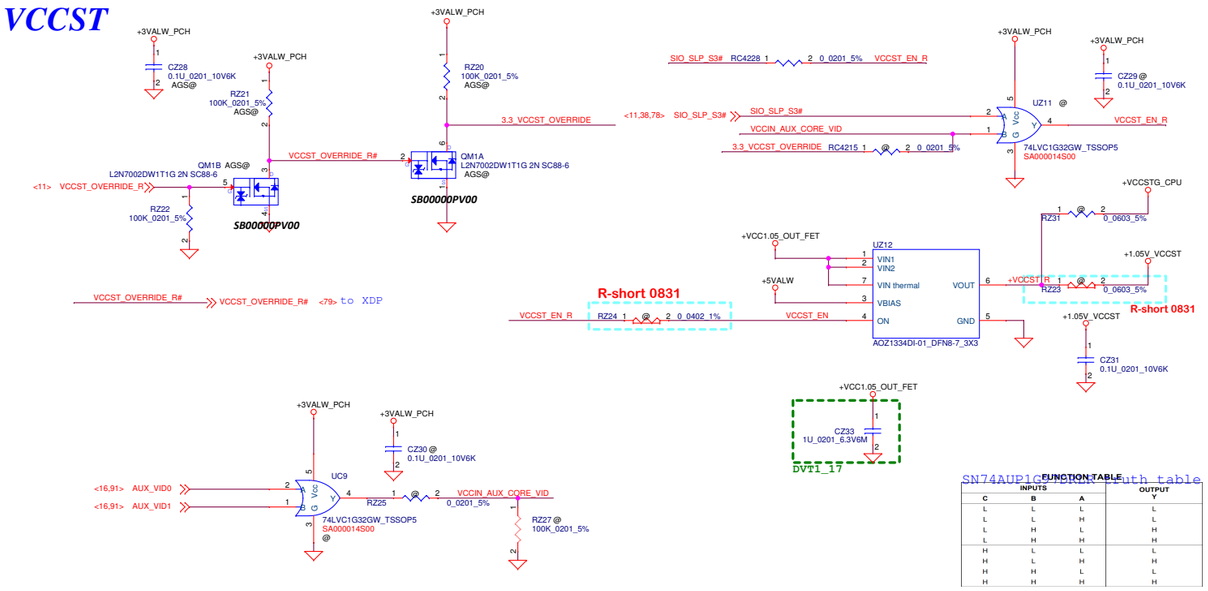








VCCST



SN74AUP1G... truth table

FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: DC/DC

Size: | Document Number: LA-K033P | Rev: 1.0

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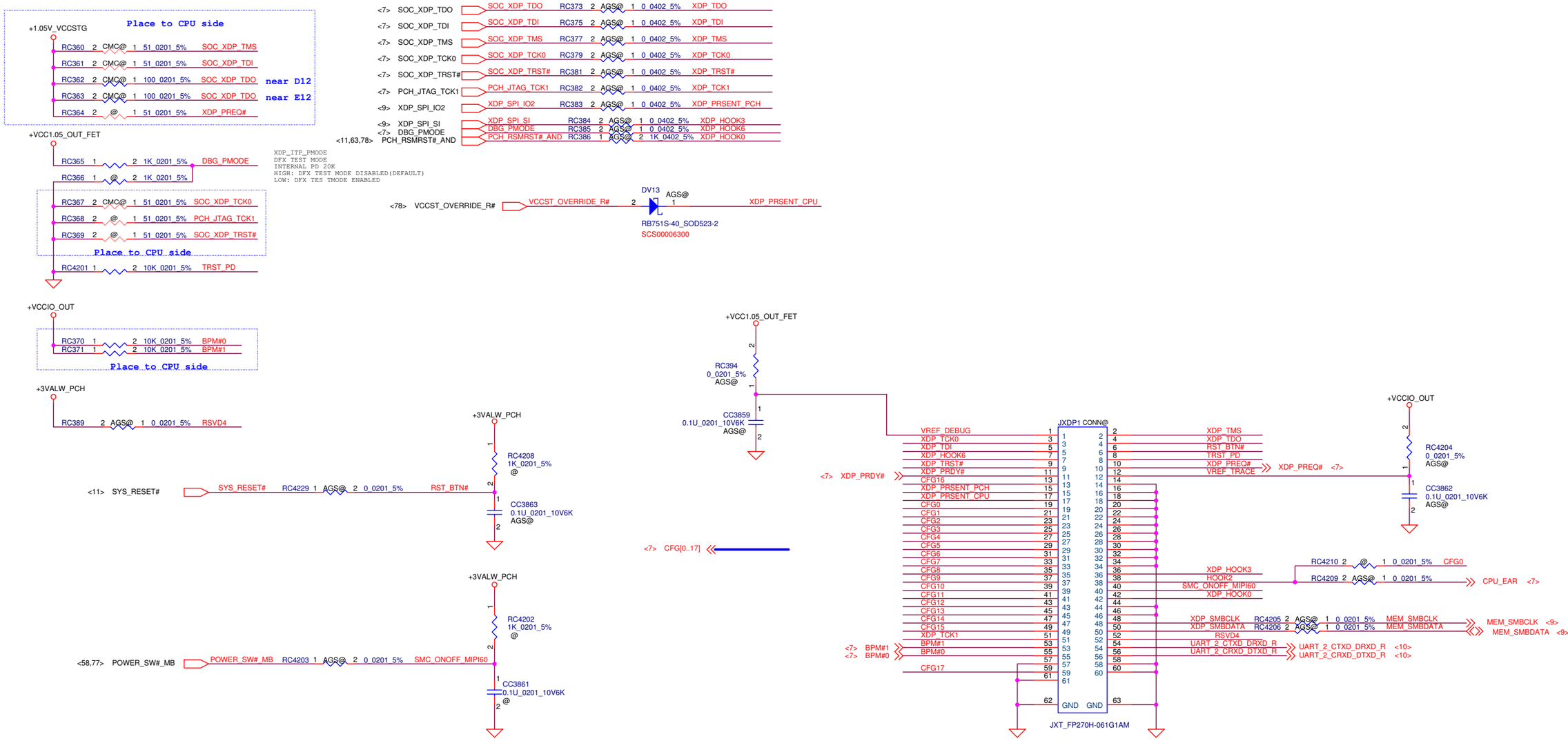
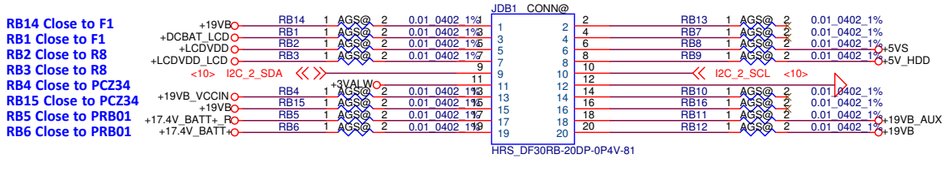
Main Func = Debug connector



Power Monitor



RB14 Close to F1
RB1 Close to F1
RB2 Close to R8
RB3 Close to R8
RB4 Close to PCZ34
RB15 Close to PCZ34
RB5 Close to PRB01
RB6 Close to PRB01

RB13 Close to RW1
RB7 Close to RW1
RB8 Close to RS32
RB9 Close to RS32
RB10 Close to PJPM01
RB16 Close to PJPM01
RB11 Close to PJG2
RB12 Close to PJG2

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: Debug connector			
Size	Document Number: LA-K033P		Rev: 1.0
Date: Friday, September 11, 2020	Sheet 79 of 101		

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **XDP**

Size	Document Number	Rev
B	LA-K033P	1.0

Date: Friday, September 11, 2020 | Sheet 80 of 101

Reserve

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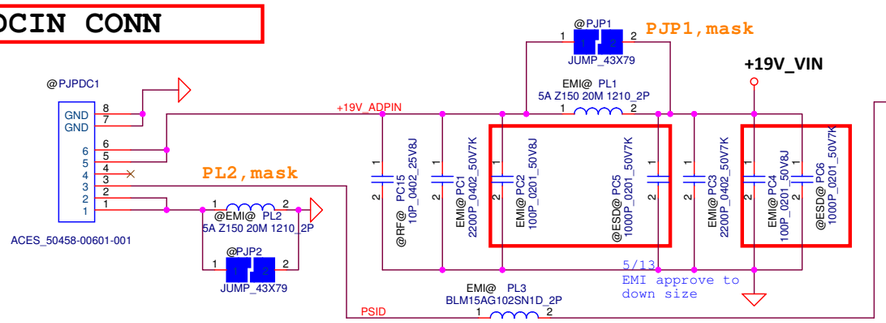
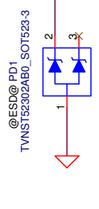
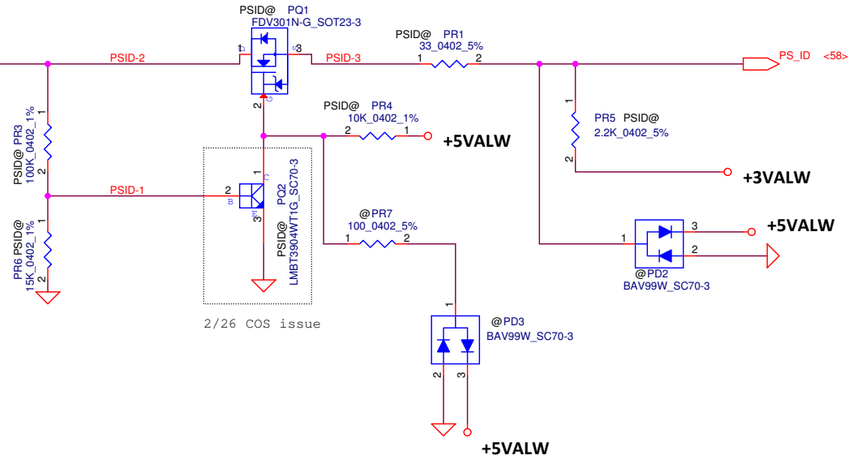
Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.		
Title: *Reserve for PWR*		
Size	Document Number: *LA-K033P*	Rev: 0.1
Date: Friday, September 11, 2020	Sheet 81 of 101	

Main Func = DCIN CONN







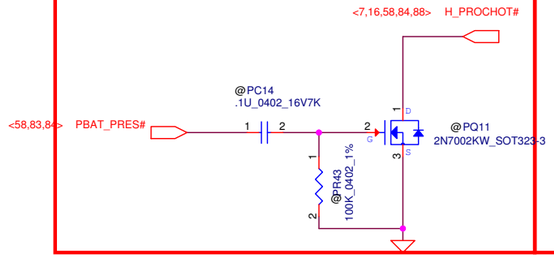
Battery Bat Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T

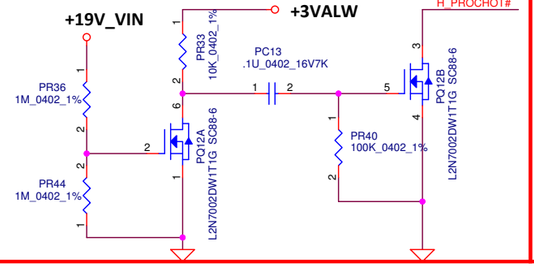
Adapter protection

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

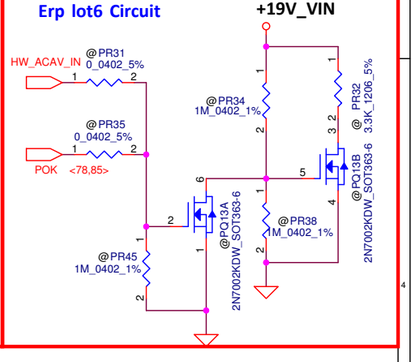


Battery protection

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



Erp lot6 Circuit



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Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: ***PWR_DCIN CONN***

Size	Document Number	Rev
	LA-K033P	0.1

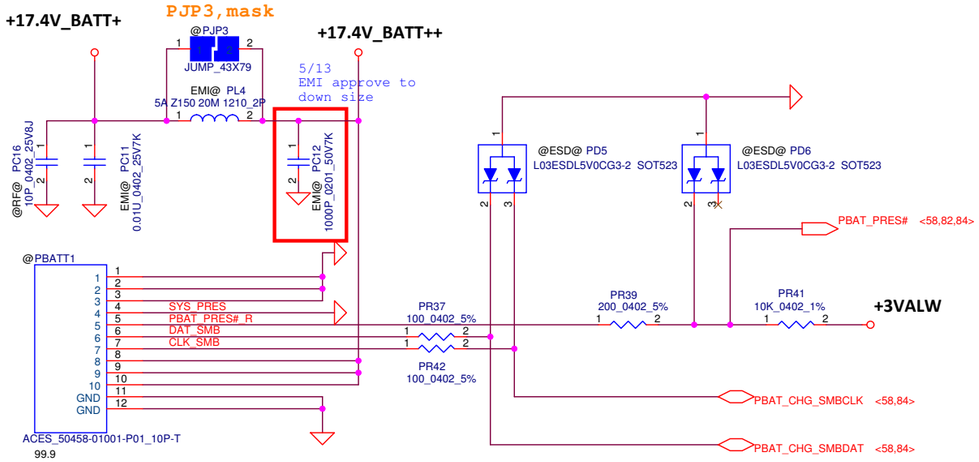
Date: Friday, September 11, 2020 | Sheet 82 of 101

Main Func = BATT CONN

Battery Bat Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: PWR_BATT CONN		
Size	Document Number: LA-K033P	Rev: 0.1
Date: Friday, September 11, 2020	Sheet 83 of 101	

Main Func = CHARGER

PJPB01,mask

Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

Delay adaptor OC H_PROCHOT#
2ms while hybrid power
transit i on

Close to EC ADP_I pin

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

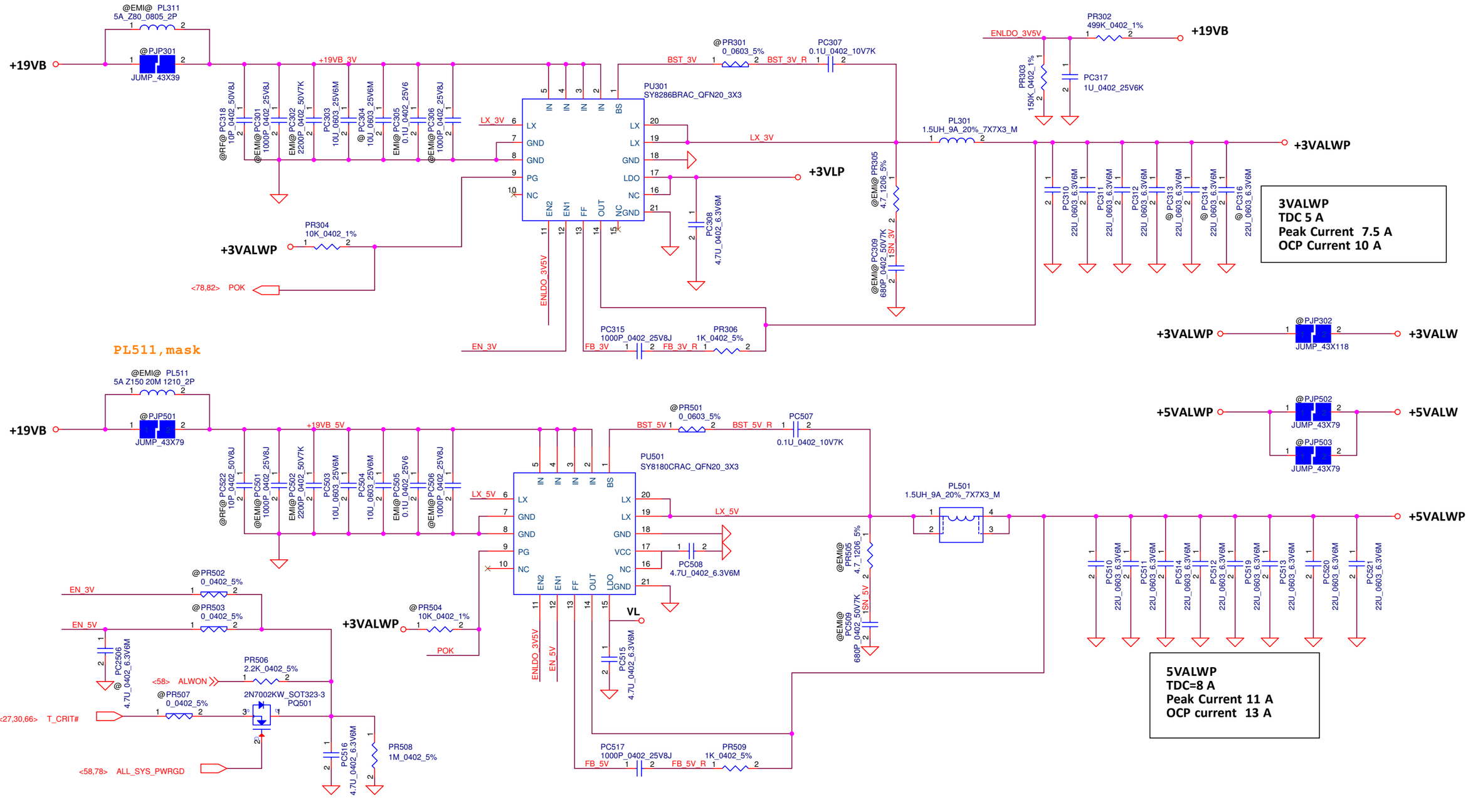
Compal Electronics, Inc.

Title: PWR_CHARGER

Size: | Document Number: LA-K033P | Rev: 0.1

Date: Friday, September 11, 2020 | Sheet 84 of 101

Main Func = 3.3VALWP/5VALWP



Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size: | Document Number: LA-K033P | Rev: 0.1

Date: Friday, September 11, 2020 | Sheet 85 of 101

Main Func = +1.2V_DDR/+0.6V_DDR_VTT/+2.5VP

0.6Volt +/- 5%
TDC 1.2A
Peak Current 1.5A

+1.2V_DDR
TDC 5.5 A
Peak Current 7.8 A
OCP Current 9.4 A

+2.5V
TDC 0.32 A
Peak Current 0.45 A

5/13
EMI approve to
down size

Vref=0.8V

Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

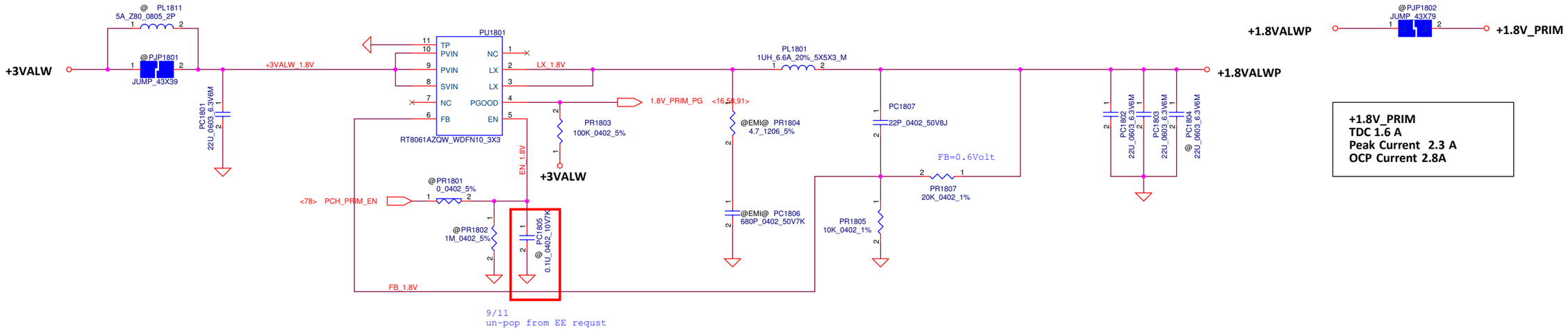
Compal Electronics, Inc.

Title: PWR_+1.2V_MEN/+0.6V_/+2.5VP

Size | Document Number: LA-K033P | Rev: 0.1

Date: Friday, September 11, 2020 | Sheet 86 of 101

Main Func = +1.8VALWP / +1.05VALWP

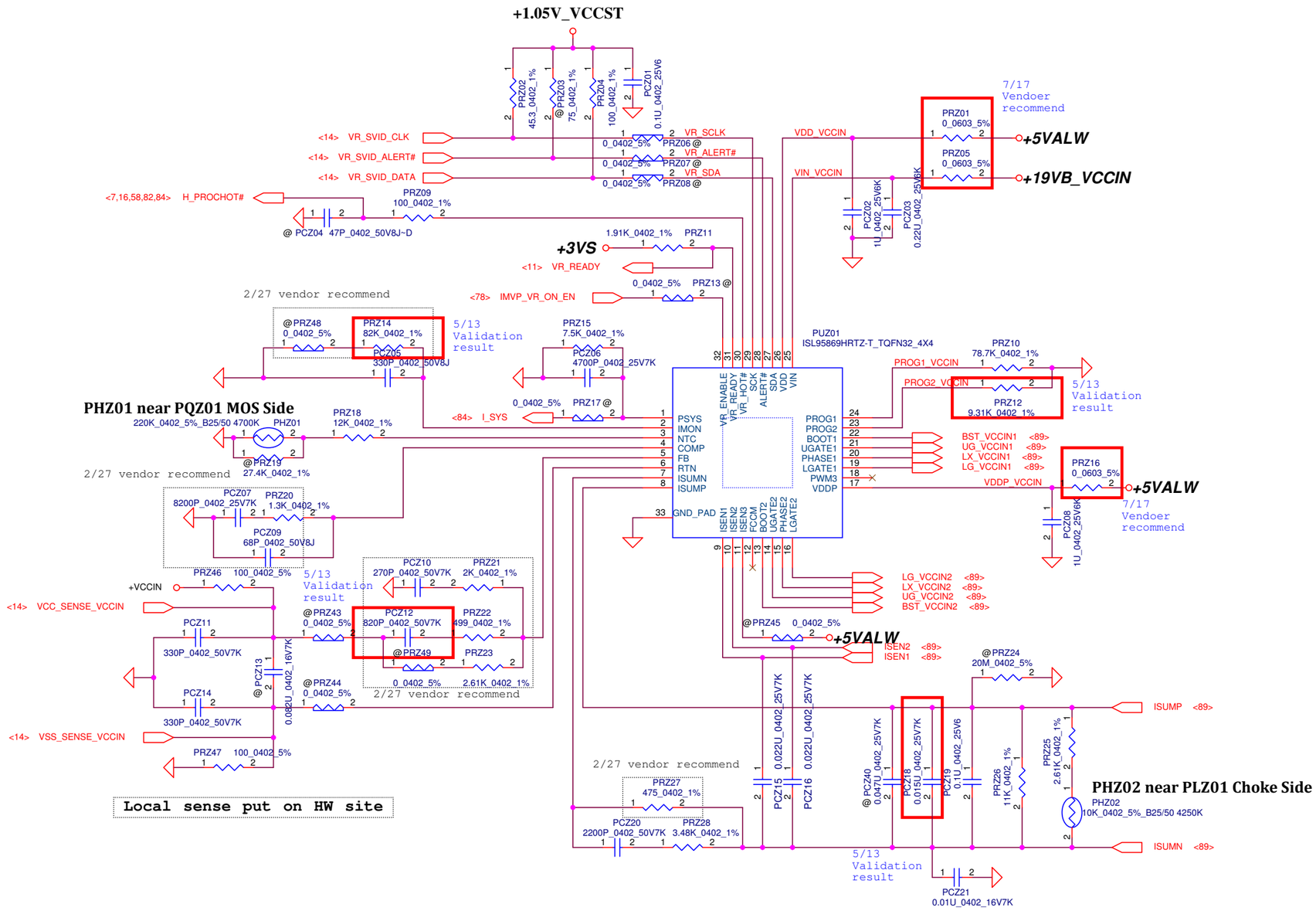


+1.8V_PRIM
TDC 1.6 A
Peak Current 2.3 A
OCP Current 2.8A

9/11
un-pop from EE requst

Compal Electronics, Inc.

Title	PWR_+1.8VALWP	
Size	Document Number: LA-K033P	Rev 0.1
Date: Friday, September 11, 2020	Sheet 87 of 101	



DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_VCCIN

Size: | Document Number: LA-K033P | Rev: X00(0.1)

Date: Friday, September 11, 2020 | Sheet 88 of 101

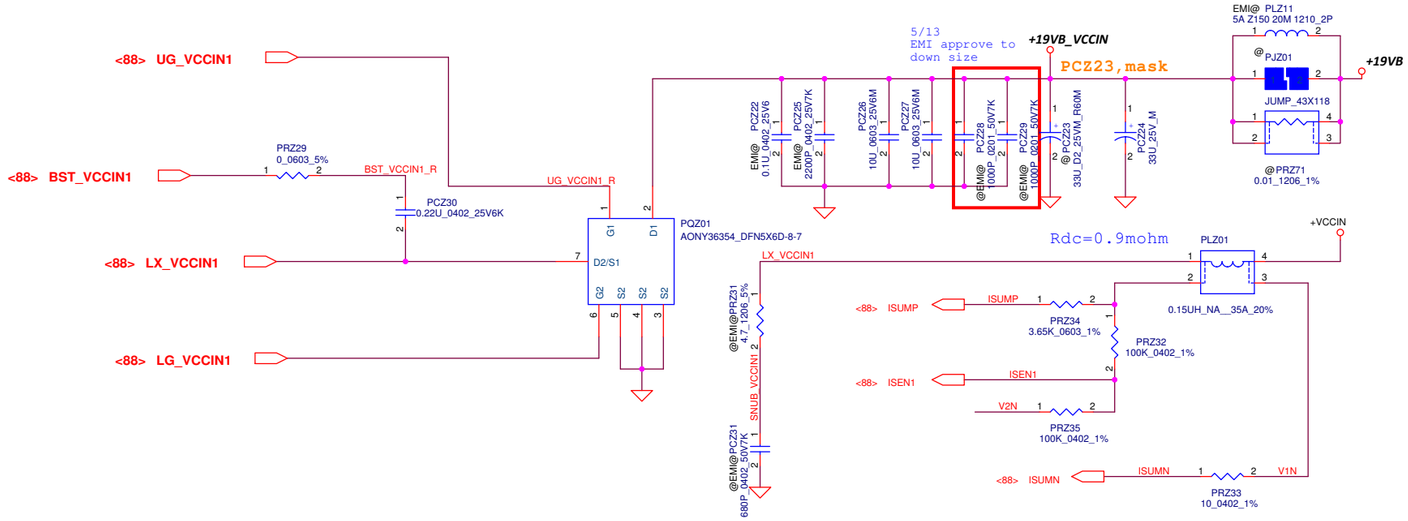
Baseline
UP3_4+2 15W (U42)

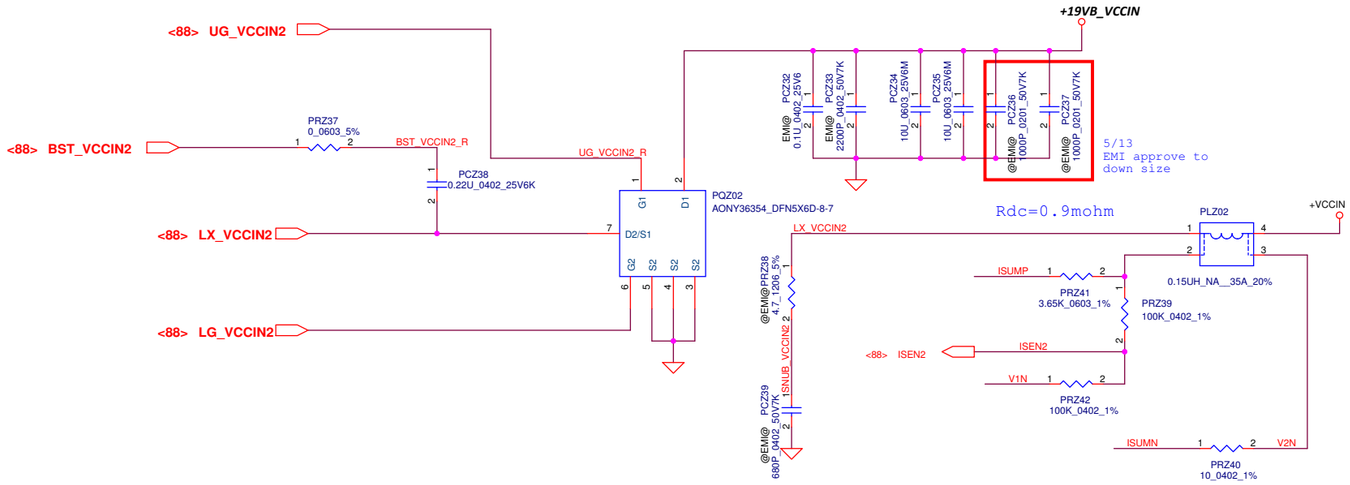
ICCMAX=47A
TDC=30A

Baseline
UP3_4+2 28W (U42)

ICCMAX=55A
TDC=36A

Frequency 750KHz





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **PWR_VCCIN**

Size | Document Number: **LA-K033P** | Rev: 0.1

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Main Func = VCCIN/ VCCIN_AUX

+VCCIN

PCZ107 330_B2_2.5VM_R9M @ 1 2
PCZ97 330U_D2_2.5Y_R9M 1 2
PCZ77 330U_D2_2.5VY_R9M 1 2

Primary side :
330U_R9 *2
22U_0603 *14

+VCCIN

PCZ100 22U_0603_6.3V6M 1 2
PCZ98 22U_0603_6.3V6M 1 2
PCZ91 22U_0603_6.3V6M 1 2
PCZ79 22U_0603_6.3V6M 1 2
PCZ102 22U_0603_6.3V6M 1 2
PCZ90 22U_0603_6.3V6M 1 2
PCZ80 22U_0603_6.3V6M 1 2
PCZ84 22U_0603_6.3V6M 1 2
PCZ87 22U_0603_6.3V6M 1 2
PCZ86 22U_0603_6.3V6M 1 2

PCZ89 @ 47U_0603_6.3V6M 1 2
PCZ101 @ 47U_0603_6.3V6M 1 2
PCZ88 @ 47U_0603_6.3V6M 1 2
PCZ85 22U_0603_6.3V6M 1 2
PCZ96 22U_0603_6.3V6M 1 2
PCZ99 22U_0603_6.3V6M 1 2
PCZ93 @ 22U_0603_6.3V6M 1 2
PCZ95 @ 22U_0603_6.3V6M 1 2
PCZ83 @ 22U_0603_6.3V6M 1 2
PCZ82 22U_0603_6.3V6M 1 2

+VCCIN

PCZ76 @ 1U_0201_6.3V6M 1 2
PCZ92 @ 1U_0201_6.3V6M 1 2
PCZ75 @ 1U_0201_6.3V6M 1 2
PCZ91 @ 1U_0201_6.3V6M 1 2
PCZ94 @ 1U_0201_6.3V6M 1 2
PCZ78 @ 1U_0201_6.3V6M 1 2

+VCCIN_AUX

PCG45 @ 330U_D2_2.5VY_R9M 1 2
PCG46 330U_D2_2.5VY_R9M 1 2

330U_R9 *1
22U_0603 *25

+VCCIN_AUX

PCG20 22U_0603_6.3V6M 1 2
PCG25 22U_0603_6.3V6M 1 2
PCG51 22U_0603_6.3V6M 1 2
PCG50 22U_0603_6.3V6M 1 2
PCG55 22U_0603_6.3V6M 1 2
PCG67 22U_0603_6.3V6M 1 2
PCG70 22U_0603_6.3V6M 1 2
PCG68 22U_0603_6.3V6M 1 2
PCG69 22U_0603_6.3V6M 1 2
PCG19 22U_0603_6.3V6M 1 2

PCG81 22U_0603_6.3V6M 1 2
PCG83 22U_0603_6.3V6M 1 2
PCG76 22U_0603_6.3V6M 1 2
PCG75 22U_0603_6.3V6M 1 2
PCG21 22U_0603_6.3V6M 1 2
PCG22 22U_0603_6.3V6M 1 2
PCG23 22U_0603_6.3V6M 1 2
PCG26 22U_0603_6.3V6M 1 2
PCG27 22U_0603_6.3V6M 1 2
PCG28 22U_0603_6.3V6M 1 2

+VCCIN_AUX

PCG72 @ 47U_0603_6.3V6M 1 2
PCG73 @ 47U_0603_6.3V6M 1 2
PCG84 @ 47U_0603_6.3V6M 1 2
PCG66 22U_0603_6.3V6M 1 2
PCG74 22U_0603_6.3V6M 1 2
PCG85 22U_0603_6.3V6M 1 2
PCG24 22U_0603_6.3V6M 1 2
PCG71 22U_0603_6.3V6M 1 2

5/21
Validation result

Compal Electronics, Inc.

Title: PWR_VCCIN/ VCCIN_AUX

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Main Func = VCCIN_AUX

ICCMAX=27A
TDC=14A
DC LL=1.8m(mV/A)
AC LL=TBD

OCP is Lowside MOSFET Rdson sense

2/18 change OCP

5/13
EMI approve to
down size

Rdc=1.19mohm

2/24 vendor recommend

2/18
pop from vendor comment

3/18
pop from vendor comment

5V: 800KHz
Float: 600KHz
GND: 400KHz

High > 1V
Low <0.4V

VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

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Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

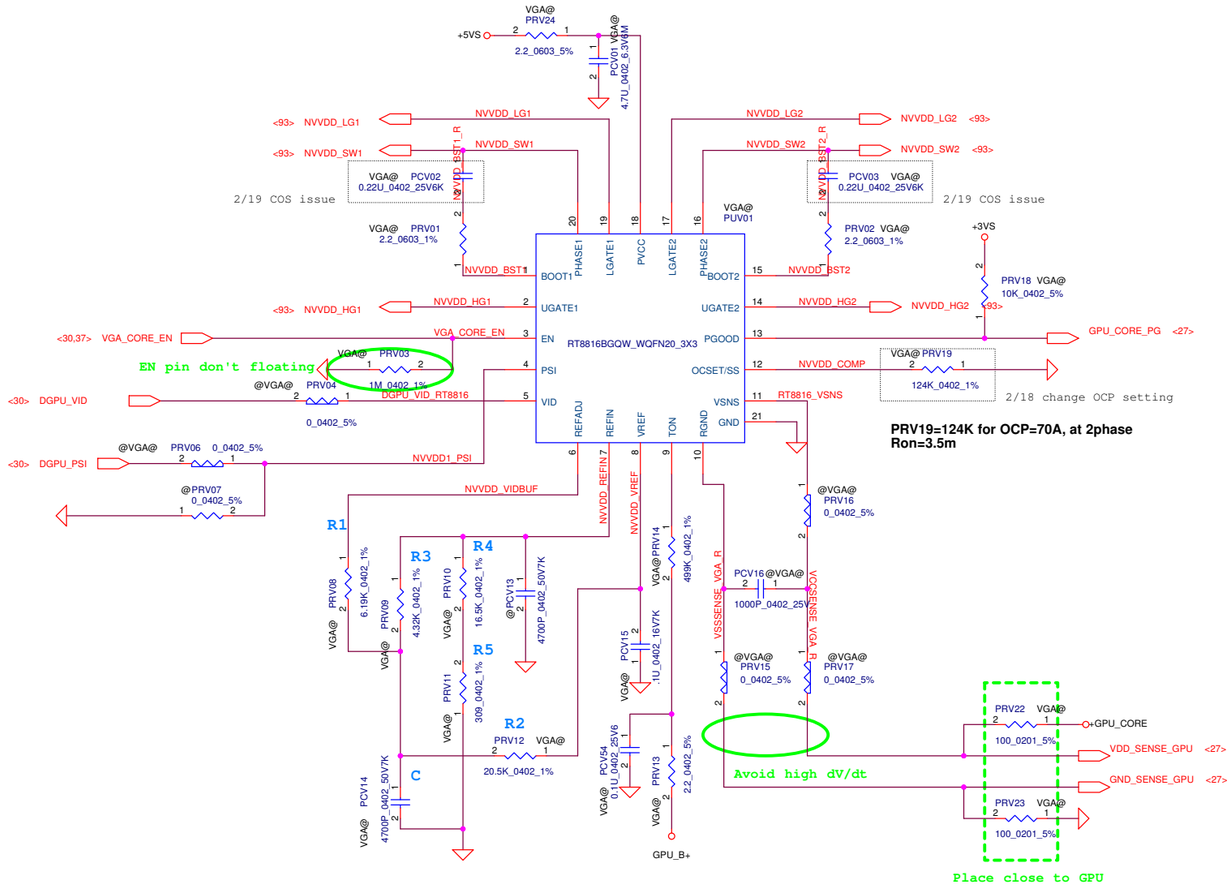
Compal Electronics, Inc.

Title: PWR VCCIN_AUX

Size | Document Number: LA-K033P | Rev: 0.1

Date: Friday, September 11, 2020 | Sheet 91 of 101

Main Func = VGA CORE



Operation Phase Number PSI Voltage Setting

1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

```
+GPU_CORE  (N17S-G3)
TDC=29.8A
Peak Current 58.7A
OCP=   70A
DCR:0.98mohm  +-5%
              TYP          MAX
H/SRds(on):  8.2mohm    10.5mohm
L/SRds(on):  2.8mohm     3.5mohm
```


Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

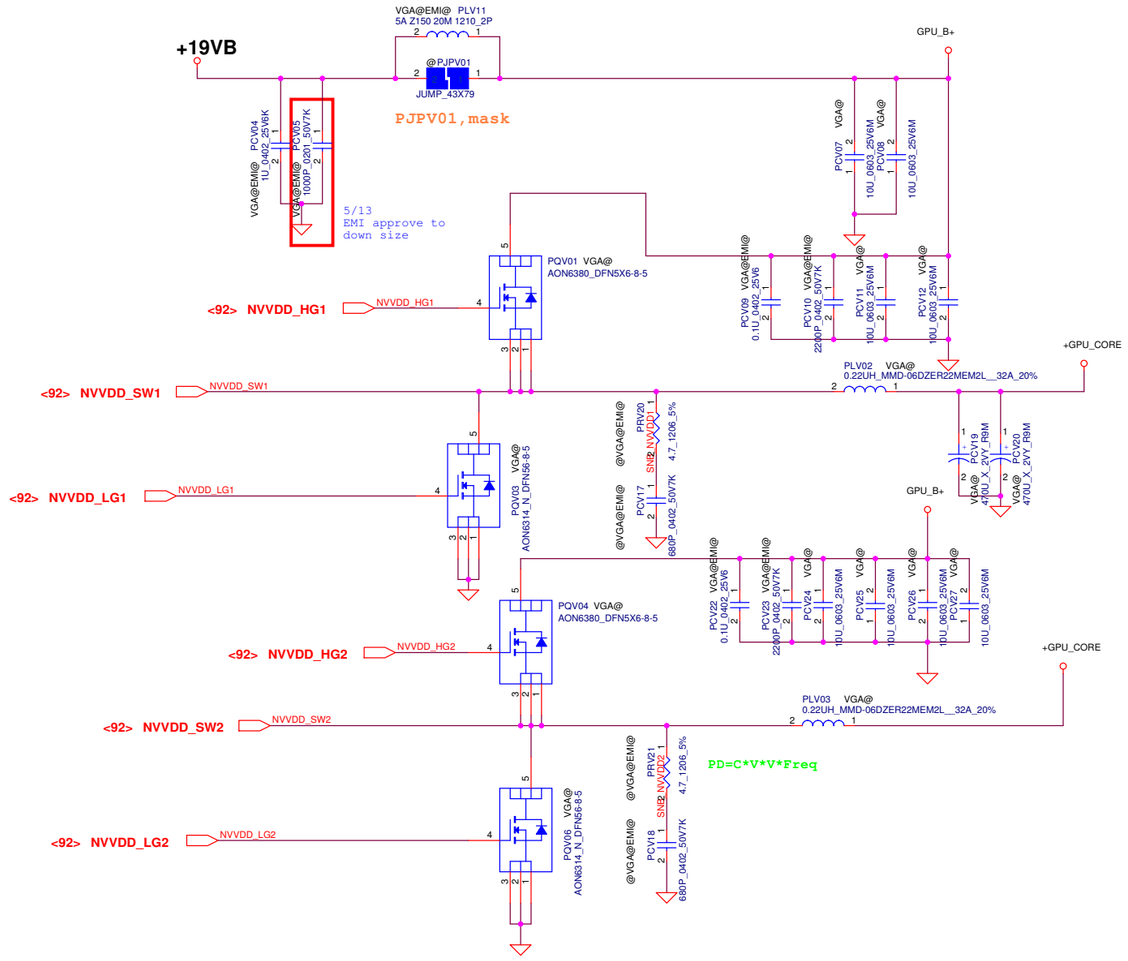
Compal Electronics, Inc.

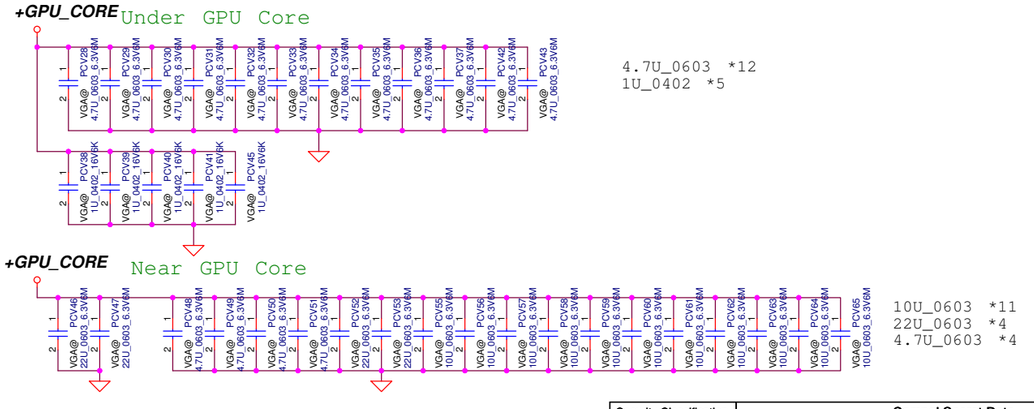
Title: PWR_VGA_CORE

Size | Document Number: LA-K033P | Rev: 0.1

Date: Friday, September 11, 2020 | Sheet 92 of 101

Main Func = VGA CORE





Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.	
Title	GPU_Decoupling
Size	Document Number: LA-K033P
Rev	0.1
Date:	Friday, September 11, 2020
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Main Func = +1.35VGPUP

+1.35VGPUP
TDC 5.2A
Peak Current 7.4A
OCP Current 10 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

+3VS
VGA@ PRW05 100K_0402_5%
<27,37> +1.35VGS_PGOOD
VGA@ PRW06 10_0402_1%
BST_+1.35VGPU
VGA@ PCW12 0.1U_0402_10V6K
BST_+1.35VGPU_R
PUW01 VGA@ RT6226AGQUF_UQFN12_3X3
@VGA@EMI@ PLW11 5A_Z80_0805_2P
+19VB
@PJPW01 JUMP_43X39
+19VB +1.35VGPU
@VGA@EMI@ PCW15 1000P_0201_50V7K
@VGA@EMI@ PCW16 1000P_0201_50V7K
VGA@EMI@ PCW01 0.1U_0402_25V6
@VGA@EMI@ PCW02 2200P_0402_50V7K
VGA@ PCW03 10U_0603_25V6M
VGA@ PCW04 10U_0603_25V6M
@RF@ PCW21 10P_0402_50V8J
VIN PGOOD BOOT LX FB BYP VCC EN ILMT PGND AGND NC
LX_+1.35VGPU
VGA@ PLW01 1UH_6.6A_20%_5X5X3_M
+5VALW
VGA@ PRW11 2.2_0402_1%
@VGA@EMI@ PRW07 4.7_1206_5%
SNNI_+1.35VGPU
Vfb=0.6
FB_+1.35VGPU
@VGA@ PCW14 330P_0402_50V7K
@VGA@ PRW13 1K_0402_1%
R1
VGA@ PRW09 39.2K_0402_1%
VGA@ PRW10 31.6K_0402_1%
R2
@VGA@EMI@ PCW13 680P_0402_50V7K
VGA@ PCW05 22U_0603_6.3V6M
VGA@ PCW06 22U_0603_6.3V6M
VGA@ PCW07 22U_0603_6.3V6M
VGA@ PCW08 22U_0603_6.3V6M
@VGA@ PCW17 22U_0603_6.3V6M
@VGA@ PCW18 22U_0603_6.3V6M
@VGA@ PCW19 22U_0603_6.3V6M
@VGA@ PCW20 22U_0603_6.3V6M
+1.35VGPUP
@PJPW02 JUMP_43X118
+1.35VS_VRAM
+1.35VGPUP
5/13
EMI approve to down size
VGA@ PRW01 0_0402_5%
<31,37> 1.35V_PWR_EN
EN_+1.35VGPU
VGA@ PRW02 1M_0402_1%
@VGA@ PCW09 0.1U_0402_25V6
LIMT_+1.35VGPU
+5VALW
PRW03 @VGA@ 0_0402_5%
PRW04 @VGA@ 0_0402_5%
5/13
update by FAE command with RT6226A
LX_+1.35VGPU
VCC_+1.35VGPU
VGA@ PCW10 1U_0402_10V6K
VGA@ PCW11 1U_0402_10V6K

+5VALW
PR1004 2.2_0402_1% VGA@
+5VALW_VDD_1.0V
PC1004 VGA@ 1U_0402_6.3V6K
VGA@
PU1001 G9661MF11U_SO8
VPP VIN VEN POK NC VO ADJ GND GND
@PJP1001 JUMP_43X39
+3VALW
+3VALW_1.0V
VGA@ PC1001 22U_0603_6.3V6M
ADJ_1.0V
+1.0VGPUP
VGA@ PR1002 2.55K_0402_1%
@PC1005 0.01U_0402_25V7K
VGA@ PC1002 22U_0603_6.3V6M
Vref=0.8V
PR1001
<30,37> 1.0VS_DGPU_EN
0_0402_5% VGA@
EN_1.0V
+1.0VS_DGPU_PGOOD
<31>
PR1005 VGA@ 100K_0402_5%
VGA@ PR1003 10K_0402_1%
@VGA@ PC1003 0.1U_0402_10V6K
+3VS

+1.0VGPUP
@PJP1002 JUMP_43X39
+1.0VS_DGPU

+1.0VGPUP
TDC 0.28 A
Peak Current 0.4 A

Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.			
Title: PWR_+1.35VGPUP			
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Reserve

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Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.		
Title: Reserve for PWR		
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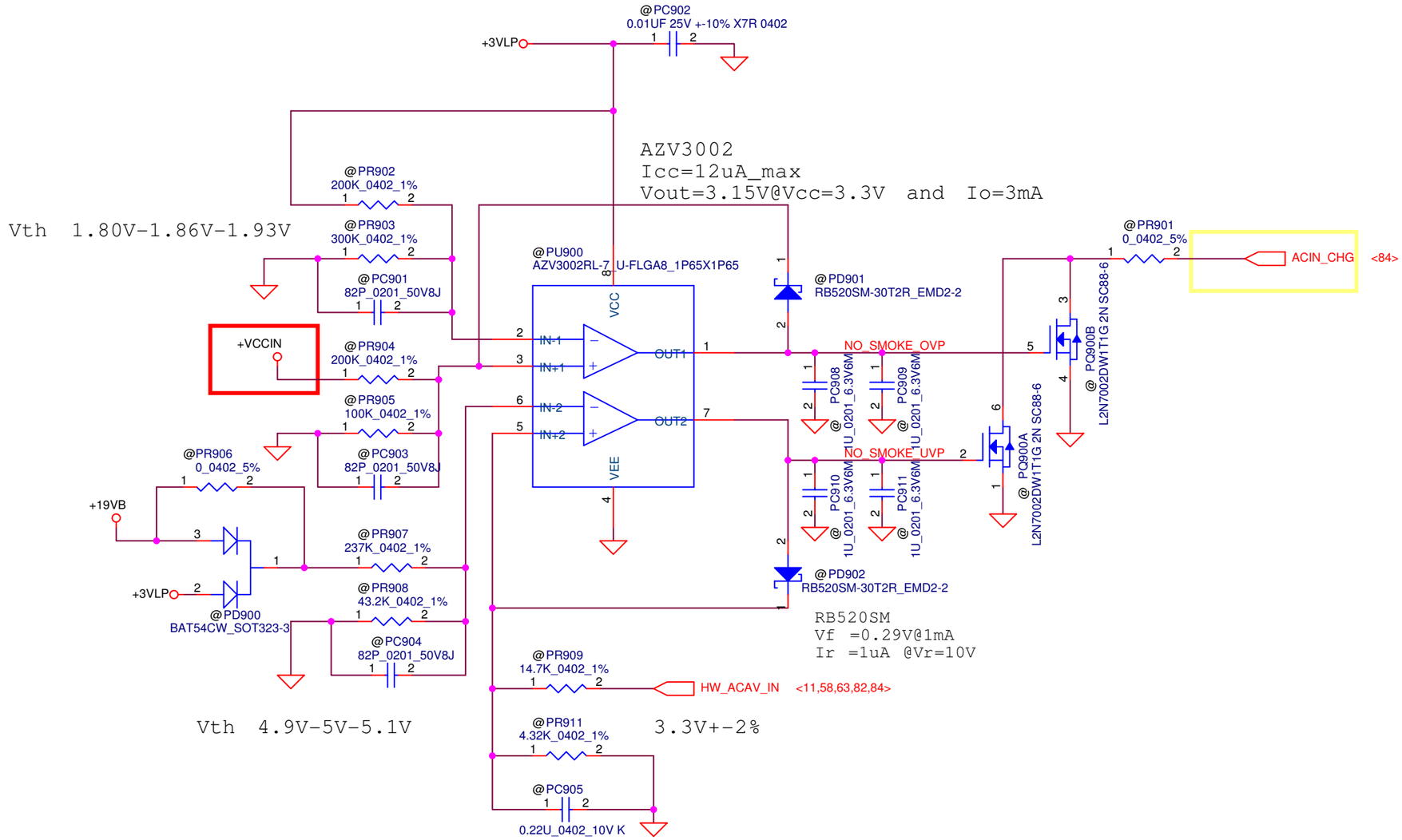

Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.

Title: **NO SMOKE**

Size	Document Number	Rev
	LA-K033P	0.1

Date: Friday, September 11, 2020 Sheet 96 of 101

Reserve

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Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.		
Title: Reserve for PWR		
Size	Document Number: LA-K033P	Rev: 0.1
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Reserve

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Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.		
Title: Reserve for PWR		
Size	Document Number: LA-K033P	Rev: 0.1
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Reserve

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Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.		
Title: *Reserve for PWR*		
Size	Document Number: *LA-K033P*	Rev: 0.1
Date: Friday, September 11, 2020	Sheet 99 of 101	

Version Change List (P. I. R. List)

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						

Security Classification	Compal Secret Data		
Issued Date	2019/05/10	Deciphered Date	2024/05/10

Compal Electronics, Inc.		
Title: PWR P.I.R		
Size	Document Number: LA-K033P	Rev: 0.1
Date: Friday, September 11, 2020	Sheet 100 of 101	

Version Change List (P. I. R. List)

DVT1 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 05/15								
1	2018/5/17	8		Add RC207, CPU_SPI_0_CS#1	For 2nd ROM	Y	N	Y
2	2018/5/17	66		Del JP7, short +5VS and +5VS_ODD	Optimal B+ routing	Y	N	Y
3	2018/5/17	14		CC52,CC48,CC51,C5 change to 0402	meet purchase requirement	Y	Y	Y
4	2018/5/17	29		CV73~CV78, CV100~CV109 change to 0402	meet purchase requirement	Y	Y	Y
5	2018/5/17	71		del CU3,CU8 CU4,CU9 1U change to 4.7U	meet purchase requirement	Y	Y	Y
6	2018/5/20			Del CS6,CU3,CU8; CU13,CU16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize	Y	Y	Y
7	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch	Y	N	Y
8	2018/6/4	38		Connect UC1.CC30 to R72, Add RC208,RC209	For 17" Touch	Y	N	Y
9	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize	Y	Y	Y
10	2018/6/4	31		CV161,CV162,CV163,CV164,CV165,CV166,CV167,CV168,CV169,CV170,CV182,CV183, CV184,CV185,CV186,CV187,CV188,CV189,CV190,CV191,CL16 change to 0201	MLCC downsize	Y	Y	Y
11	2018/6/13	56		CA16 change to 0402	MLCC downsize	Y	Y	Y
12	2018/7/4	65		add Rx10~14	co-lay ST TPM	Y	N	Y
13	2018/7/4			add CC75(pop),CZ41,CC76,CC77,CC78,CC79	For ESD requirement	Y	Y	Y
14	2018/7/6	65		add Rx15~RX19	co-lay China TPM	Y	N	Y

DVT2 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 07/16								
1	2018/8/14	66	RX20,RX21,RX22	reserve 0 ohm 0402	reserve for china TPM	Y	N	Y
2	2018/8/15	38	R96	reserve 0 ohm 0201	disconnet B+	Y	N	Y
3			EU1,EU3,EU8,EU9	SC300002C00=>SC300001Y00	ESD require	Y	Y	N
4		71	RE1	SD03417828O=>SD034270280 17.8K change to 27K	EC board ID	Y	Y	N
5			CC54,CC57		fixed 1.05 OVP(BITS382716)	Y	Y	N
6			UZ2	SA00007XR00=>SA00008R600(Vccio load switch)	fixed 1.05 OVP(BITS382716)	Y	Y	N
7				Remove Typec configuration	Dell PCR	N	Y	N
8			CC64,CC52,CC59,CC17,CC15,CC18,CC19	0402 1u =>0201 1u	MLCC downsize	Y	Y	Y
9			R52	7.15K =>6.49K	Fixed OTP issue(BITS383003)	Y	Y	N

Title	Compal Electronics, Inc.	
	FE Change list	
Size	Document Number	Rev
	LA-K933P	1.0
Date:	Sheet 1 of 1	