Compal Confidential

V330/V530/EX3

DIS M/B Schematics Document

Intel Kabylake RU Processor with DDR4

AMD R17M

2017-06-15

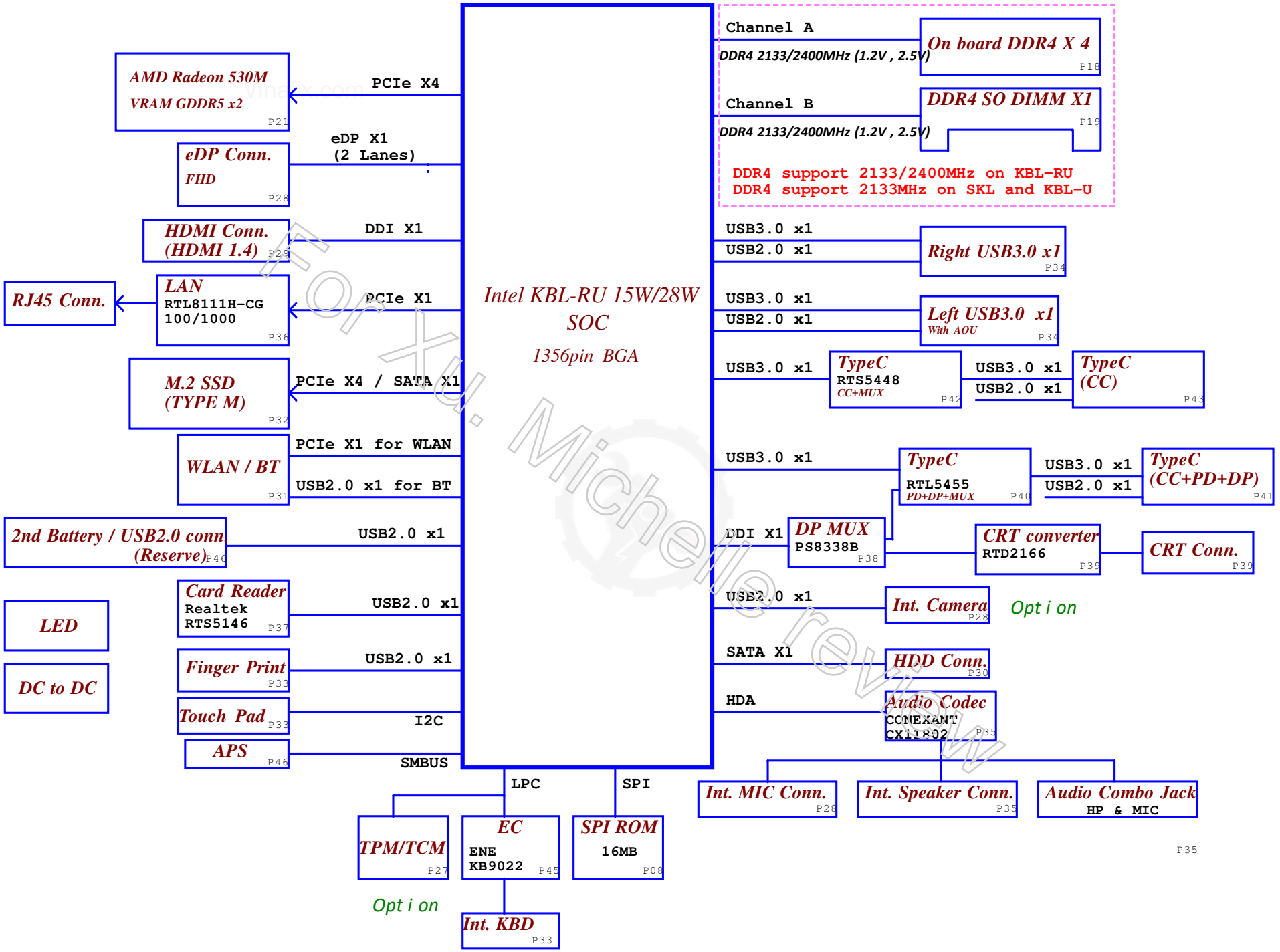
LA-F481P

REV :0.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Cover Page

Size	Document Number	Rev
C	LA-D562P	0.1

Date: Thursday, June 15, 2017 Sheet 1 of 66



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Block Diagram
Size: C	Document Number: LA-D562P		Rev: 1.0
Date: Thursday, June 15, 2017	Sheet 2 of 66		

Voltage Rails

State \ power plane	+RTCBATT	+B +5VL +3VL	+5VALW +3VALW +1.8VALW +1VALW	+1.0V_VCCST +2.5V +1.2V	+5VS +3VS +3VGS +1.8VGS +1.0VS_VCCIO +PCIE_VGS +VGA_CORE +1.35VS_VRAM +0.6VS +VCCCORE +VCCGT +VCCSA
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 and S4/AC	O	O	O	X	X
S5 and S4/Battery only	O	O	X	X	X
S5 and S4/AC&Battery don't exist(Only RTC)	O	X	X	X	X

USB 2.0 Port Table

Port	3 External USB Port
1	USB 3.0 Port (AOU)
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	TYPE-C USB 3.0 Port(FULL)
5	Camera
6	M.2 BT
7	Card Reader
8	Finger Print
9	2nd Battery
10	

USB 3.0 Port Table

Port	
1	USB 3.0 Port (AOU)
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	TYPE-C USB 3.0 Port(FULL)
5	
6	

SATA Port Table

Port	
0	HDD
1	
2	M.2 SATA SSD

PCIE Port Table

Port	Lane	
1	1	GPU
2	2	
3	3	
4	4	
5		LAN
6		M.2 WLAN+BT
7		
8		
9		
10		M.2 PCIE*4 SSD
11		
12		

BOM Structure Table

Item	BOM Structure
SKL only	SKL@
For 2+2	U22@
For 2+3	U23@
For 4+2	U42@
For DIS	DIS@
For UMA	UMA@
Camera	CMOS@
EMI pop	EMI@
EMI Un-pop	@EMI@
ESD pop	ESD@
ESD Un-pop	@ESD@
RF pop	RF@
RF unpop	@RF@
For SPI 8M	8M@
For SPI 16M	16M@
Finger Print	FP@
Keyboard backlight	KBL@
AOU	AOU@
NONAOU	NONAOU@
TYPEC FULL	TYPEC@
NONTYPEC	NONTYPEC@
APS	APS@
NOAPS	NOAPS@
2nd Battery USB	BATT2@
NO 2nd Battery USB	NOBATT2@
Onboard RAM HYNIX	X76DDRH@
Onboard RAM MICRON	X76DDRM@
Onboard RAM SAMSUNG	X76DDRS@
VRAM HYNIX	X76H2G@
VRAM MICRON	X76M4G@
VRAM SAMSUNG	X76S2G@
CardReader RTS5146	X76RT@
CardReader GL835	X76GL@
TPM	TPM@
TCM	TCM@
NO TPM/TCM	NOTPM@
Connector	ME@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

PCH SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
GPU	1000 001x A0h
RTS5455	1010 1100 A0h
RTD2166	1100 100 A0h
APS	1111 0100 A0h

SMBUS Control Table

	SOURCE	GPU	BATT	NECP388	SODIMM	SOC
SMB_EC_CK1 SMB_EC_DA1	EC KB9022 +3VALW	X	V +3VALW	X	X	X
SMB_EC_CK2 SMB_EC_DA2	EC KB9022 +3VS	V +3VGS	X	X	X	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V(RAM)	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

CPU

2+2

2+3

SKL-U

UC1 CPU1@ i7-6500U SA000092P60
UC1 CPU2@ i5-6300U SA000092T40
UC1 CPU3@ i5-6200U SA000092O70
UC1 CPU4@ i3-6006U SA0000ACN10
UC1 CPU5@ i7-6567U SA00009E620
UC1 CPU6@ i5-6267U SA00009E530

KBL-U

UC1 CPU7@ i3-7100U SA0000A38H0
UC1 CPU8@ i5-7200U SA0000A372G
UC1 CPU9@ i7-7500U SA0000A34F0
UC1 CPU10@ i5-7300U SA0000ADQ20
UC1 CPU11@ 3865U SA0000ADL30
UC1 CPU12@ 4415U SA0000AD140
UC1 CPU13@ i7-7567U SA0000AW620
UC1 CPU14@ i5-7267U SA0000AKR20

KBL-RU 4+2

UC1 CPU15@ KBL-R QN5D SA0000AR010
UC1 CPU16@ KBL-R QN5C SA0000AQZ10
UC1 CPU17@ KBL-R QNEF SA0000AWB00
UC1 CPU18@ KBL-R QNBF SA0000AWC00

On Board RAM

ZZZ X76DDR4H@ 2G HYNIX X7675138L01
ZZZ X76DDR4M@ 2G MICRON X7675138L02
ZZZ X76DDR4S@ 2G SAMSUNG X7675138L03

GPU

UV1 GPU1@ VGA SA000098VB0

ZZZ PCB DA8001CE000

CardReader

ZZZ X76RT@ RTS5146 X7675138L61
ZZZ X76GL@ GL835 X7675138L62

ZZZ X4E@ X4E X4EA8X38L01

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Notes List

Size: C | Document Number: LA-D562P | Rev: 0.1

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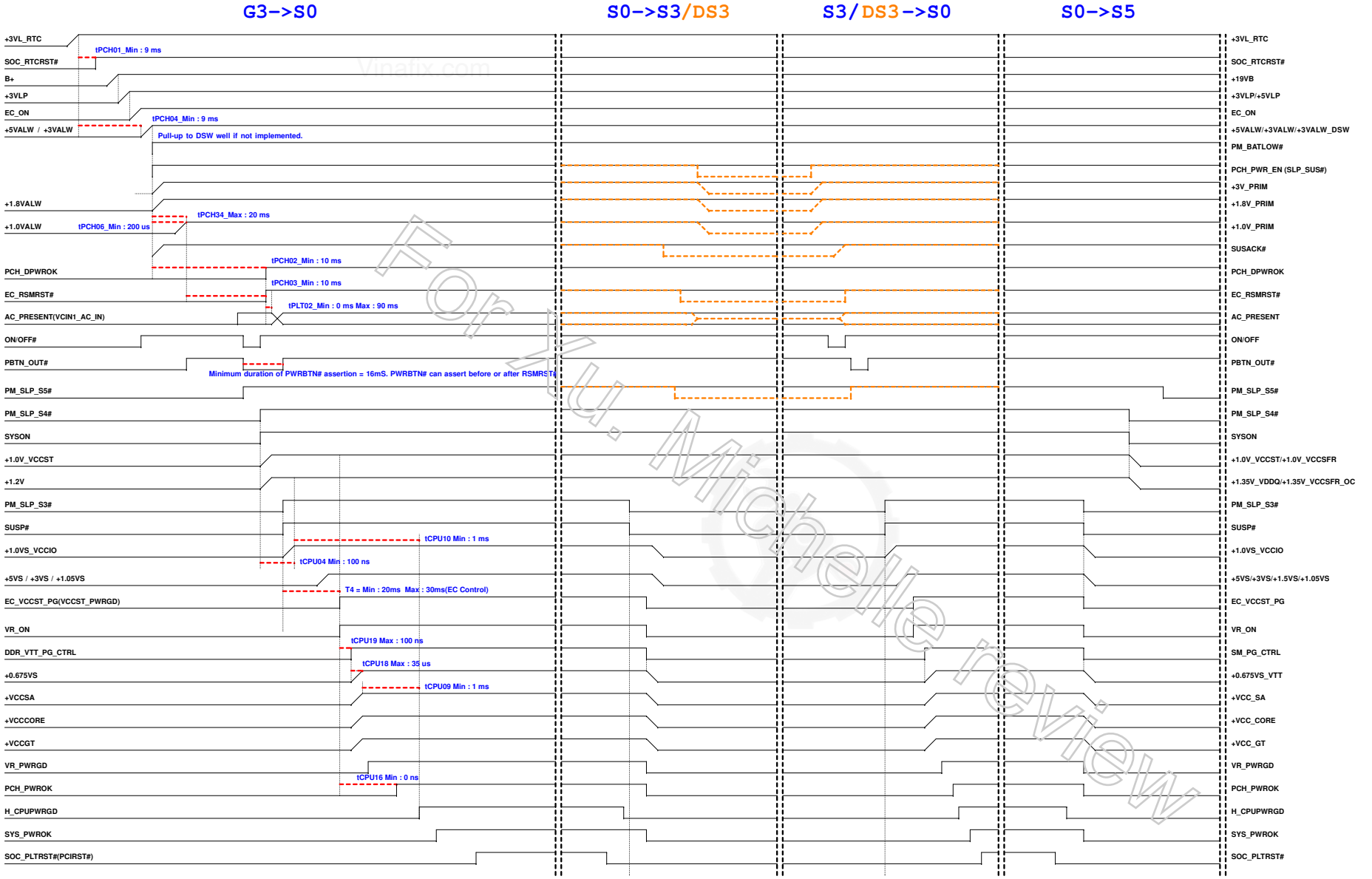
[BIWB6/B7/E7/E8-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



Security Classification	Compal Secret Data		
Issued Date	2015/01/29	Deciphered Date	2016/01/29

Compal Electronics, Inc.

Title: Power Sequence

Size	Document Number	Rev
	LA-D561P	0.1

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M1-30 VRAM STRAP

	Vendor UV3, UV4, UV5, UV6	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV22	X76@ R_pd RV27
X76H2G@ X7667538L03	HYNIX 4096Mbits 2GBytes SA000076P80 TEMP 256MX16 K4W4G1646E-BC1A TEMP	0	0	0	0	NC	4.75K
X76M2G@ X7667538L04	Micron 4096Mbits 2GBytes SA00009HF00 TEMP 256Mx16 MT41J256M16LY-091G:N TEMP	1	0	0	1	8.45K	2K
X76S2G@ X7667538L05	SAMSUNG 4096Mbits 2GBytes SA00008DN00 TEMP 256MX16 H5TC4G63CFR-N0C TEMP	2	0	1	0	4.53K	2K
		4	1	0	0	4.53K	4.99K
		5	1	0	1	3.24K	5.62K
		6	1	1	0	3.4K	10K

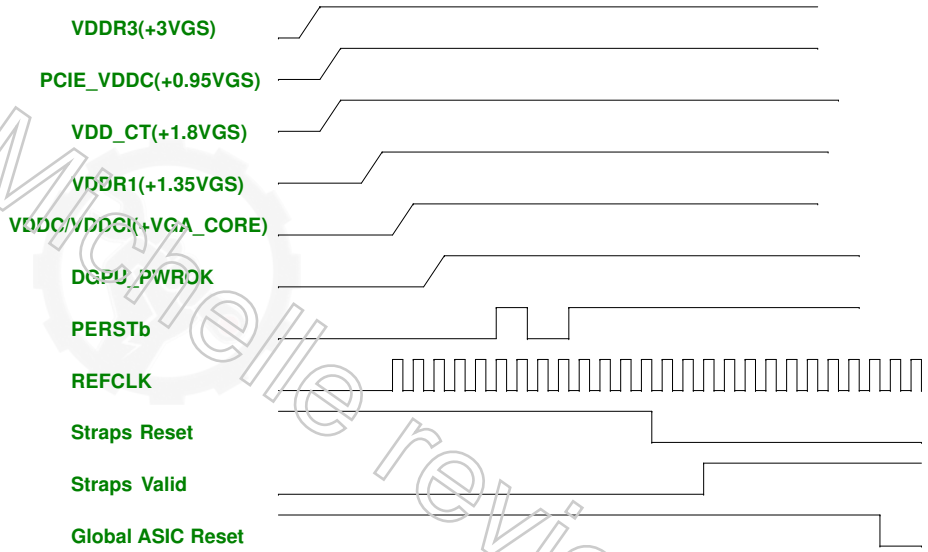
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Power-Up/Down Sequence

"M1" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.
- It is recommended that the 3.3-V rail ramp up frist.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpressTM idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≦ 50mV/us)
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/07	Deciphered Date	2016/01/07
Title	VGA Notes List		
Size C	Document Number LA-D562P		Rev 0.1
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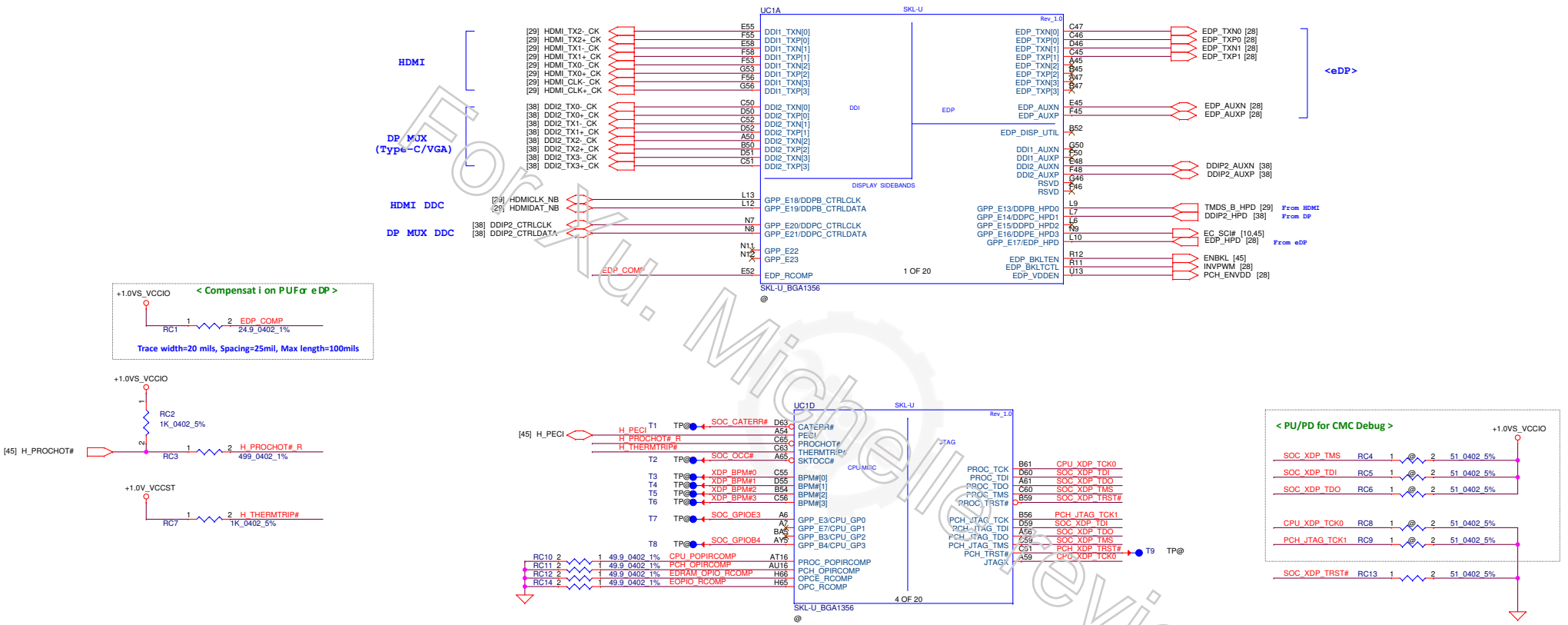

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	SKL-U(1/12)DDI,EDP,MISC,CMC		
Size: Custom	Document Number: LA-D562P		Rev: 0.1
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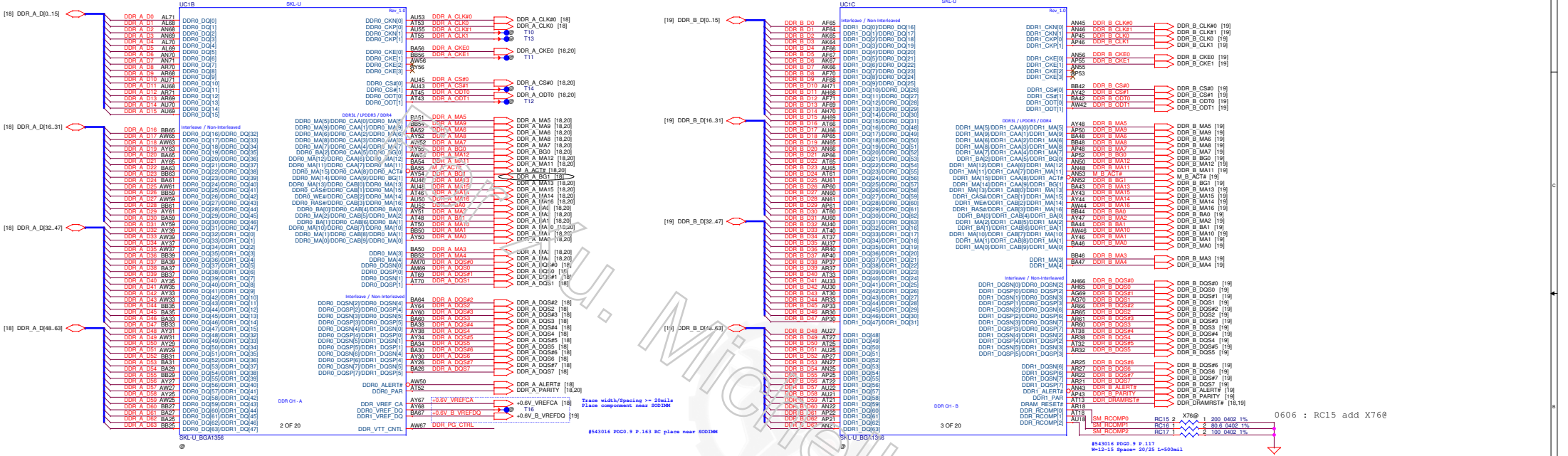
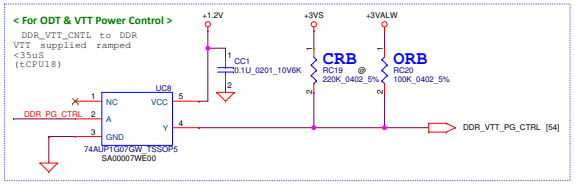
Interleaved Memory



< For ODT & VTT Power Control >

DDR_VTT_CNTL to DDR VTT supplied ramped <35uS (tCPU18)



	SDP	DDP
RC15	200 1%	121 1%

Security Classification	Compal Secret Data		
Issued Date	2015/01/29	Deciphered Date	2016/01/29

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Title: SKL-U(2/12)DDR4

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SMBALERT# (Internal Pull Down):

0 = Disable Intel ME TLS function ==> Default

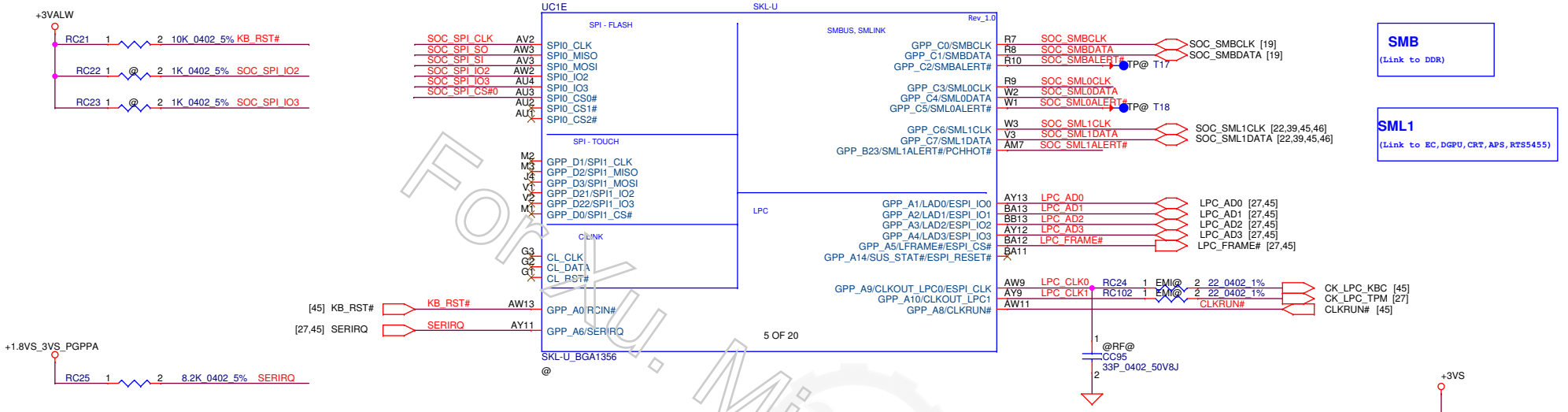
1 = Enable Intel ME TLS function

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

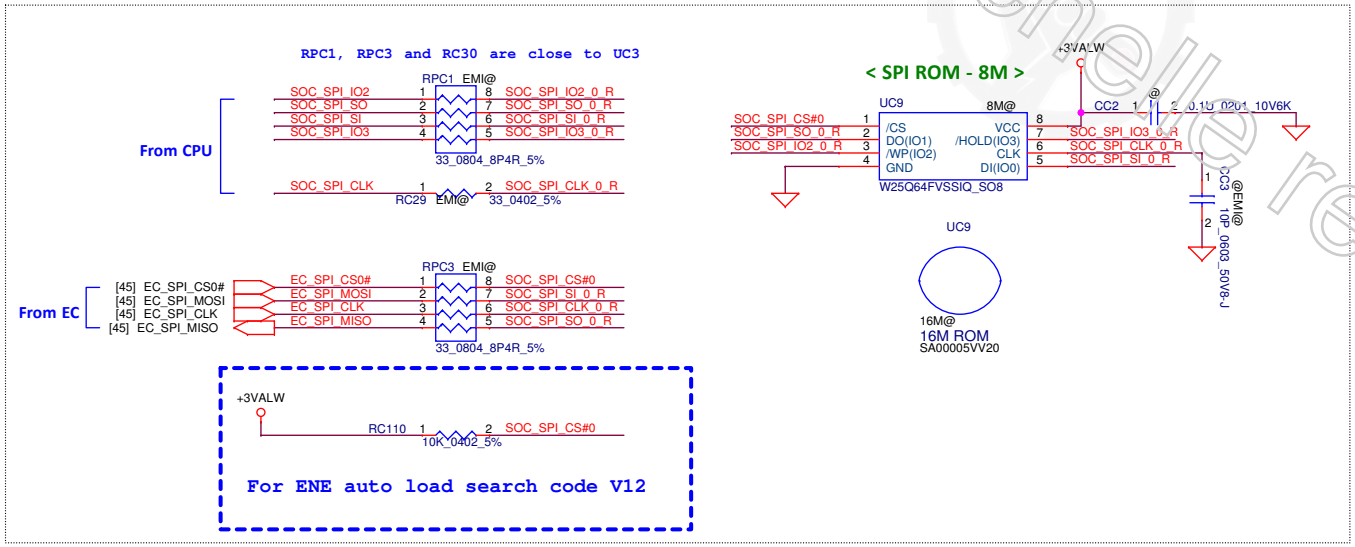
1 = eSPI is selected for EC



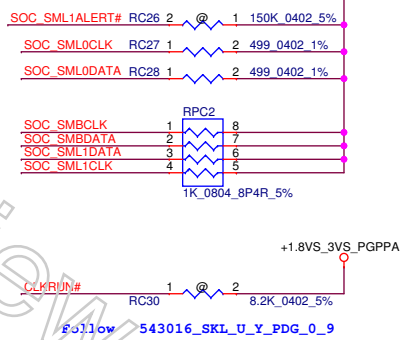
SMB (Link to DDR)

SML1 (Link to EC,DGPU,CRT,APS,RTS5455)

RPC1, RPC3 and RC30 are close to UC3



< SPI ROM - 8M >



Follow 543016_SKL_U_Y_PDG_0_9

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,SMB,LPC,ESPI

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< HD AUDIO >

RPC4_EMI@

[35] HDA_BITCLK_AUDIO — 1 — 8 — HDA_BIT_CLK
[35] HDA_SYNC_AUDIO — 2 — 7 — HDA_SYNC
[35] HDA_SDOUT_AUDIO — 3 — 6 — ME_EN
[35] HDA_RST_AUDIO# — 4 — 5 — HDA_RST#

33_0804_8P4R_5%

< To Enable ME Override >

UC1G — SKL-U — Rev_1.0

AUDIO

[44] HDA_SYNC — HDA_SYNC — BA22 — HDA_SYNC/I2S0_SFRM
[44] HDA_BIT_CLK — HDA_BIT_CLK — AY22 — HDA_BLK/I2S0_SCLK
[44,45] ME_EN — ME_EN — BB22 — HDA_SDO/I2S0_TXD
[35] HDA_SDIN0 — BA21 — HDA_SDI0/I2S0_RXD
AY21 — HDA_SDI1/I2S1_RXD
[44] HDA_RST# — HDA_RST# — AW22 — HDA_RST#/I2S1_SCLK
J5 — GPP_D23/I2S_MCLK
AY20 — I2S1_SFRM
AW20 — I2S1_TXD

AK7 — GPP_F1/I2S2_SFRM
AK8 — GPP_F0/I2S2_SCLK
AK9 — GPP_F2/I2S2_TXD
AK10 — GPP_F3/I2S2_RXD

H5 — GPP_D19/DMIC_CLK0
D7 — GPP_D20/DMIC_DATA0

[38] DDI_PRIORITY — DDI_PRIORITY — D8 — GPP_D17/DMIC_CLK1
C8 — GPP_D18/DMIC_DATA1

[35] HDA_SPKR — HDA_SPKR — AW5 — GPP_B14/SPKR

SDIO / SDXC

AB11 — GPP_G0/SD_CMD
AB13 — GPP_G1/SD_DATA0
AB12 — GPP_G2/SD_DATA1
W12 — GPP_G3/SD_DATA2
W11 — GPP_G4/SD_DATA3
W10 — GPP_G5/SD_CD#
W8 — GPP_G6/SD_CLK
W7 — GPP_G7/SD_WP

BA9 — GPP_A17/SD_PWR_EN#/ISH_GP7
BB9 — GPP_A16/SD_1P8_SEL

AB7 — SD_RCOMP — RC31 2 @ 1 200_0402_1%

AF13 — GPP_F23

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SKL-U_BGA1356

@

+3VS

1 — RC32 — 2 — HDA_SPKR — 2.2K_0402_5%

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

UC1I — SKL-U — Rev_1.0

CSI-2

A36 — CSI2_DN0
B36 — CSI2_DP0
C38 — CSI2_DN1
D38 — CSI2_DP1
C36 — CSI2_DN2
D36 — CSI2_DP2
A38 — CSI2_DN3
B38 — CSI2_DP3

C31 — CSI2_DN4
D31 — CSI2_DP4
C33 — CSI2_DN5
D33 — CSI2_DP5
A31 — CSI2_DN6
B31 — CSI2_DP6
A33 — CSI2_DN7
B33 — CSI2_DP7

A29 — CSI2_DN8
B29 — CSI2_DP8
C28 — CSI2_DN9
D28 — CSI2_DP9
A27 — CSI2_DN10
B27 — CSI2_DP10
C27 — CSI2_DN11
D27 — CSI2_DP11

C37 — CSI2_CLKN0
D37 — CSI2_CLKP0
C32 — CSI2_CLKN1
D32 — CSI2_CLKP1
C29 — CSI2_CLKN2
D29 — CSI2_CLKP2
B26 — CSI2_CLKN3
A26 — CSI2_CLKP3

E13 — CSI2_COMP — RC33 2 @ 1 100_0402_1%
B7 — GPP_D4/FLASHTRIG

EMMC

AP2 — GPP_F13/EMMC_DATA0
AP1 — GPP_F14/EMMC_DATA1
AP3 — GPP_F15/EMMC_DATA2
AN2 — GPP_F16/EMMC_DATA3
AN1 — GPP_F17/EMMC_DATA4
AN3 — GPP_F18/EMMC_DATA5
AM4 — GPP_F19/EMMC_DATA6
AM1 — GPP_F20/EMMC_DATA7

AM2 — GPP_F21/EMMC_RCLK
AM3 — GPP_F22/EMMC_CLK
AP4 — GPP_F12/EMMC_CMD

AT1 — EMMC_RCOMP — RC34 2 @ 1 200_0402_1%

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SKL-U_BGA1356

@

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size	Document Number	Rev
Custom	LA-D562P	0.1

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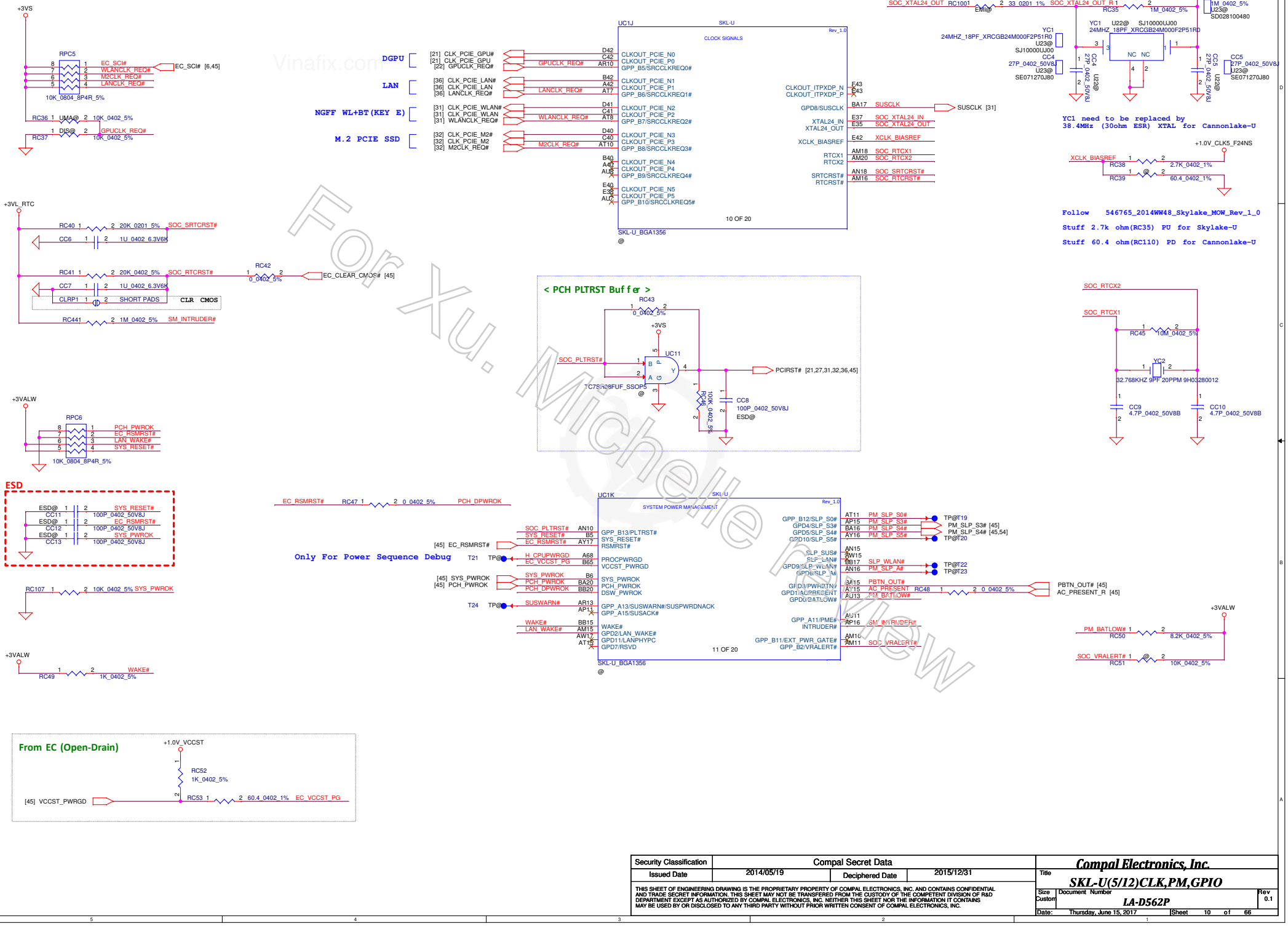
0606 change



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	SKL-U(5/12)CLK,PM,GPIO		
Size Custom	Document Number LA-D562P		Rev 0.1
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RAM vender	OBRAM_ID2	OBRAM_ID1	OBRAM_ID0
Hynix	1	1	1
Micron	1	1	0
Samsung	1	0	1
Reserve	1	0	0

Reserve

RC105 10K_0402_5% X76@ — OBRAM_ID2 — RC104 10K_0402_5% X76@

RC55 10K_0402_5% X76@ — OBRAM_ID1 — RC57 10K_0402_5% X76@

RC54 10K_0402_5% X76@ — OBRAM_ID0 — RC56 10K_0402_5% X76@

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode

+3VS — RC58 @ 2.2K_0402_5% GSPI0_MOSI

RC59 @ 2.2K_0402_5% GSPI1_MOSI

RC1031 10K_0402_5% WLBT_OFF#

RC1061 10K_0402_5% DMIC_DET#

RC60 49.9K_0402_1% UART_2_CRXD_DTXD

RC61 49.9K_0402_1% UART_2_CTXD_DRXD

+3VS — R469 2.2K_0201_5% I2C1_SDA_TP

R470 2.2K_0201_5% I2C1_SCL_TP

UC1F SKL-U Rev_1.0

LPSS

OBRAM_ID2 — AN8 GPP_B15/GSPI0_CS#

OBRAM_ID0 — AP7 GPP_B16/GSPI0_CLK

OBRAM_ID1 — AP8 GPP_B17/GSPI0_MISO

GSPI0_MOSI — AR7 GPP_B18/GSPI0_MOSI

AM5 GPP_B19/GSPI1_CS#

AN2 GPP_B20/GSPI1_CLK

AP5 GPP_B21/GSPI1_MISO

GSPI1_MOSI — AN5 GPP_B22/GSPI1_MOSI

[33] TP_INT# — AB1

[28] DMIC_DET# — AB2 GPP_C8/UART0_RXD

GPP_C9/UART0_TXD

W4 GPP_C10/UART0_RTS#

[31] WLBT_OFF# — WLBT_OFF# — AB5 GPP_C11/UART0_CTS#

[31] UART_2_CRXD_DTXD — UART_2_CRXD_DTXD — AD1 GPP_C20/UART2_RXD

[31] UART_2_CTXD_DRXD — UART_2_CTXD_DRXD — AD2 GPP_C21/UART2_TXD

AD3 GPP_C22/UART2_RTS#

AD4 GPP_C23/UART2_CTS#

U7 GPP_C16/I2C0_SDA

U8 GPP_C17/I2C0_SCL

[33] I2C1_SDA_TP — I2C1_SDA_TP — U8 GPP_C18/I2C1_SDA

[33] I2C1_SCL_TP — I2C1_SCL_TP — U9 GPP_C19/I2C1_SCL

AH9 GPP_F4/I2C2_SDA

AH10 GPP_F5/I2C2_SCL

AH11 GPP_F6/I2C3_SDA

AH12 GPP_F7/I2C3_SCL

AF11 GPP_F8/I2C4_SDA

AF12 GPP_F9/I2C4_SCL

ISH

P2 GPP_D9

P3 GPP_D10

P4 GPP_D11

P1 GPP_D12

M4 GPP_D5/ISH_I2C0_SDA

M3 GPP_D6/ISH_I2C0_SCL

N1 GPP_D7/ISH_I2C1_SDA

N2 GPP_D8/ISH_I2C1_SCL

AD11 GPP_F10/I2C5_SDA/ISH_I2C2_SDA

AD12 GPP_F11/I2C5_SCL/ISH_I2C2_SCL

U1 GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA

U2 GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL

U3 GPP_D15/ISH_UART0_RTS#

U4 GPP_D16/ISH_UART0_CTS#/SML0BALERT#

AC1 DGPU_PWR_EN — DGPU_PWR_EN [23,45,57,58]

AC2 DGPU_HOLD_RST# — DGPU_HOLD_RST# [21]

AC3 DGPU_PWROK — DGPU_PWROK [57,58]

AB4 DGPU_PRSNT#

GPP_C12/UART1_RXD/ISH_UART1_RXD

GPP_C13/UART1_TXD/ISH_UART1_TXD

GPP_C14/UART1_RTS#/ISH_UART1_RTS#

GPP_C15/UART1_CTS#/ISH_UART1_CTS#

AY8 AOU_STRAP

BA8 TPM_STRAP

BB7 TPM_STRAP2

BA7 APS_STRAP

AY7 PD_STRAP

AW7 ULTBY_STRAP

AP13 SX_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY# / ISH_GP6

GPP_A18/ISH_GP0

GPP_A19/ISH_GP1

GPP_A20/ISH_GP2

GPP_A21/ISH_GP3

GPP_A22/ISH_GP4

GPP_A23/ISH_GP5

6 OF 20

SKL-U_BGA1356

@

+3VS — RPC7 DIS@ — DGPU_HOLD_RST# 1 8 — DGPU_PWR_EN 2 7 — DGPU_PWROK 3 6 — DGPU_PRSNT# 4 5 — 10K_0804_8P4R_5%

DGPU_PRSNT# PD for DIS SKU

Function	GPP_C15
UMA	1
DIS	0

+3VS — RC62 1 UMA@ 2 10K_0402_5% DGPU_PRSNT#

Function	GPP_A18
AOU	1
NONAOU	0

+3VS — AOU_STRAP — 10K_0402_5% AOU@ RC112 — 10K_0402_5% NONAOU@ RC111

Function	GPP_A20
APS	1
NO APS	0

+3VS — APS_STRAP — 10K_0402_5% APS@ RC108 — 10K_0402_5% NOAPS@ RC109

Function	GPP_A23
ULTRA BAY	1
NO ULTRA BAY	0

+3VS — ULTBY_STRAP — 10K_0402_5% BAT12@ RC114 — 10K_0402_5% NOBAT12@ RC113

Function	GPP_A22
PD	1
NO PD	0

+3VS — PD_STRAP — 10K_0402_5% TYPEC@ RC116 — 10K_0402_5% NONTYPEC@ RC115

R3163 TCM@ 10K_0402_5% SD028100280

TPM_STRAP — 10K_0402_5% NOTPM@ R3163 — 10K_0402_5% TPM@ R3164

TPM_STRAP2 — 10K_0402_5% TCM@ R3165 — 10K_0402_5% NOTPM@ R3166

R3165 TPM@ 10K_0402_5% SD028100280

Function	PCH_[GPPA20,GPPA19]	
	TPM_STARP2	TPM_STARP
NOTPM	0	1
TCM	1	1
TPM	1	0

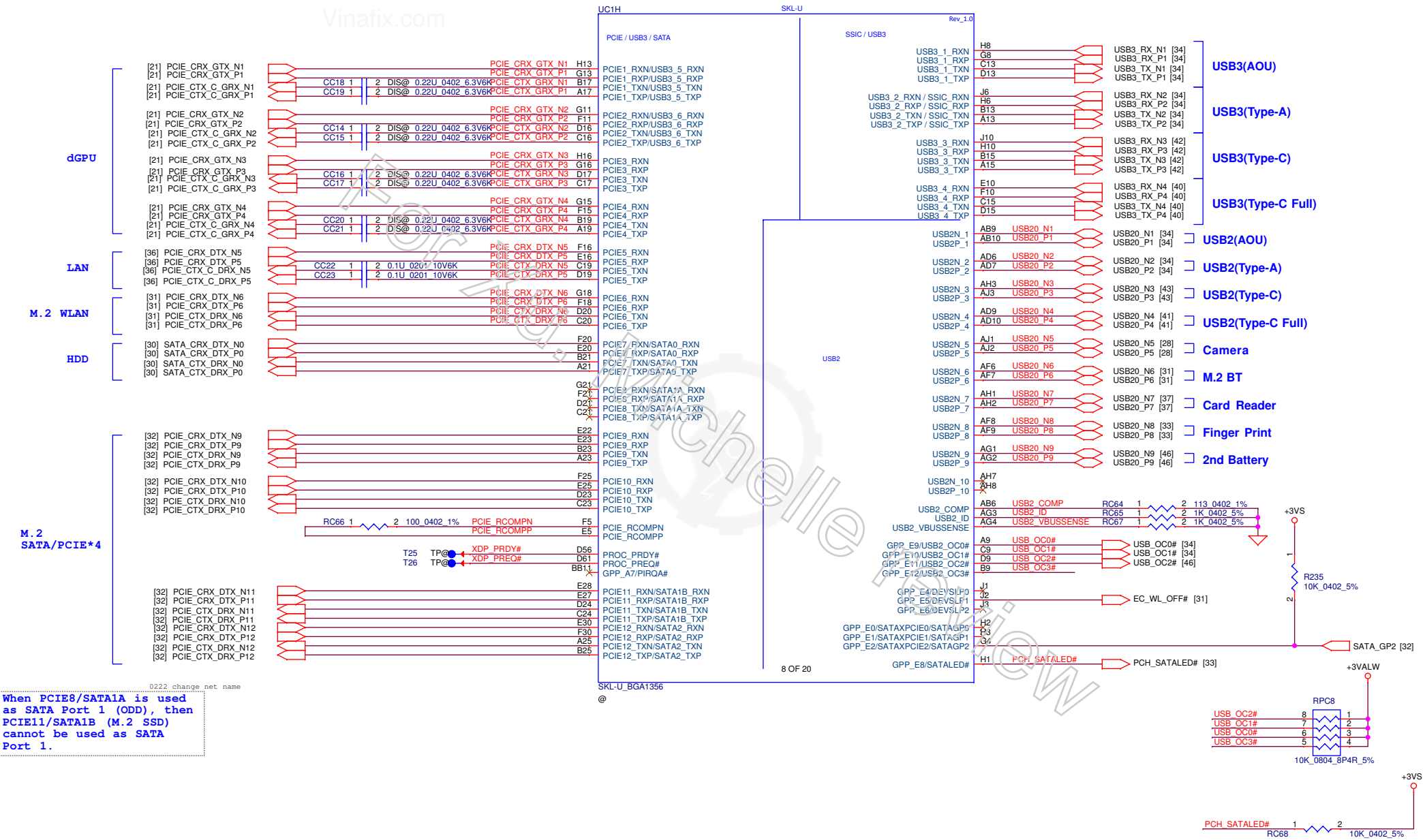
Security Classification	Compal Secret Data	
Issued Date	2014/05/19	Deciphered Date 2015/12/31

Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

Size: Custom | Document Number: LA-D562P | Rev: 0.1

Date: Thursday, June 15, 2017 | Sheet 11 of 66



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

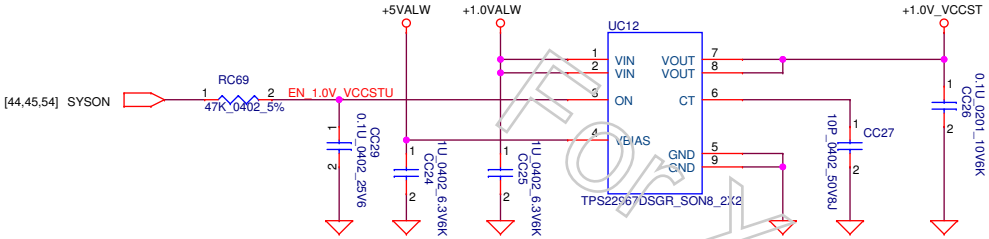
Size	Document Number	Rev
Custom	LA-D562P	0.1

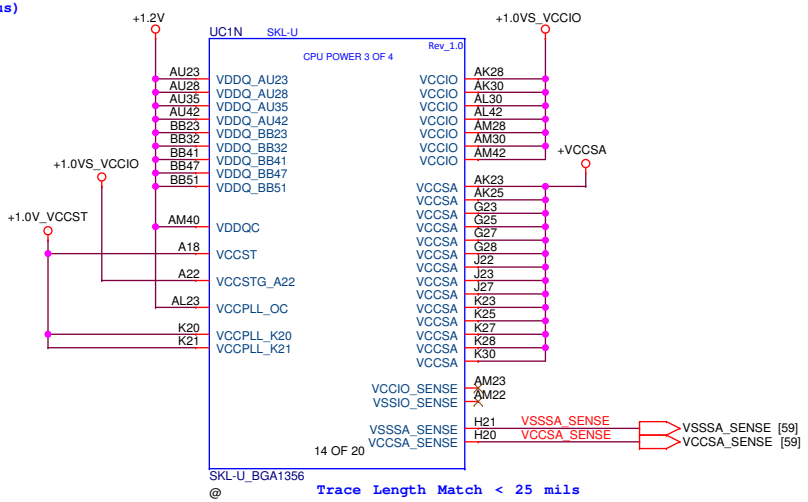
Date: Thursday, June 15, 2017 | Sheet 12 of 66

Follow 543977_SKL_PDDG_Rev0_91
CC24 10PF ->22us(Spec:<= 65us)

+1.0VALW TO +1.0V_VCCST

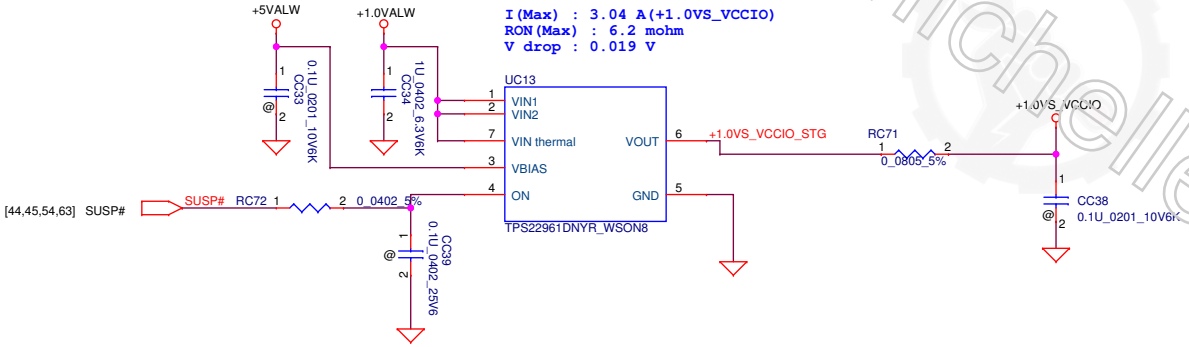
I(Max) : 0.16 A(+1.0V_VCCST)
RON(Max) : 25 mohm
V drop : 0.004 V

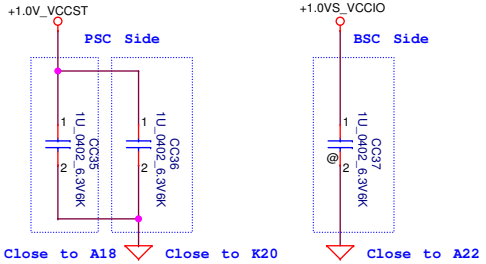


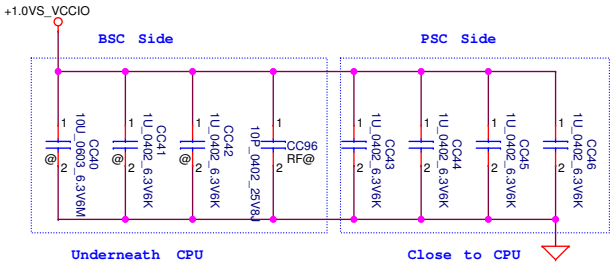


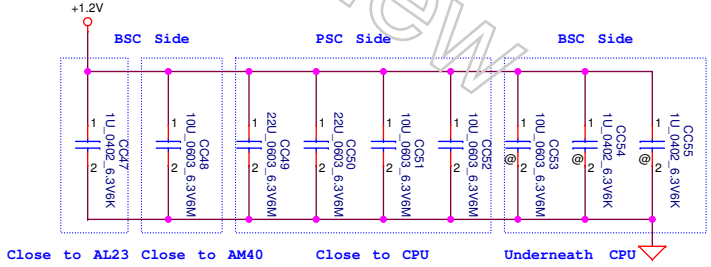
+1.0VALW TO +1.0VS_VCCIO

I(Max) : 3.04 A(+1.0VS_VCCIO)
RON(Max) : 6.2 mohm
V drop : 0.019 V



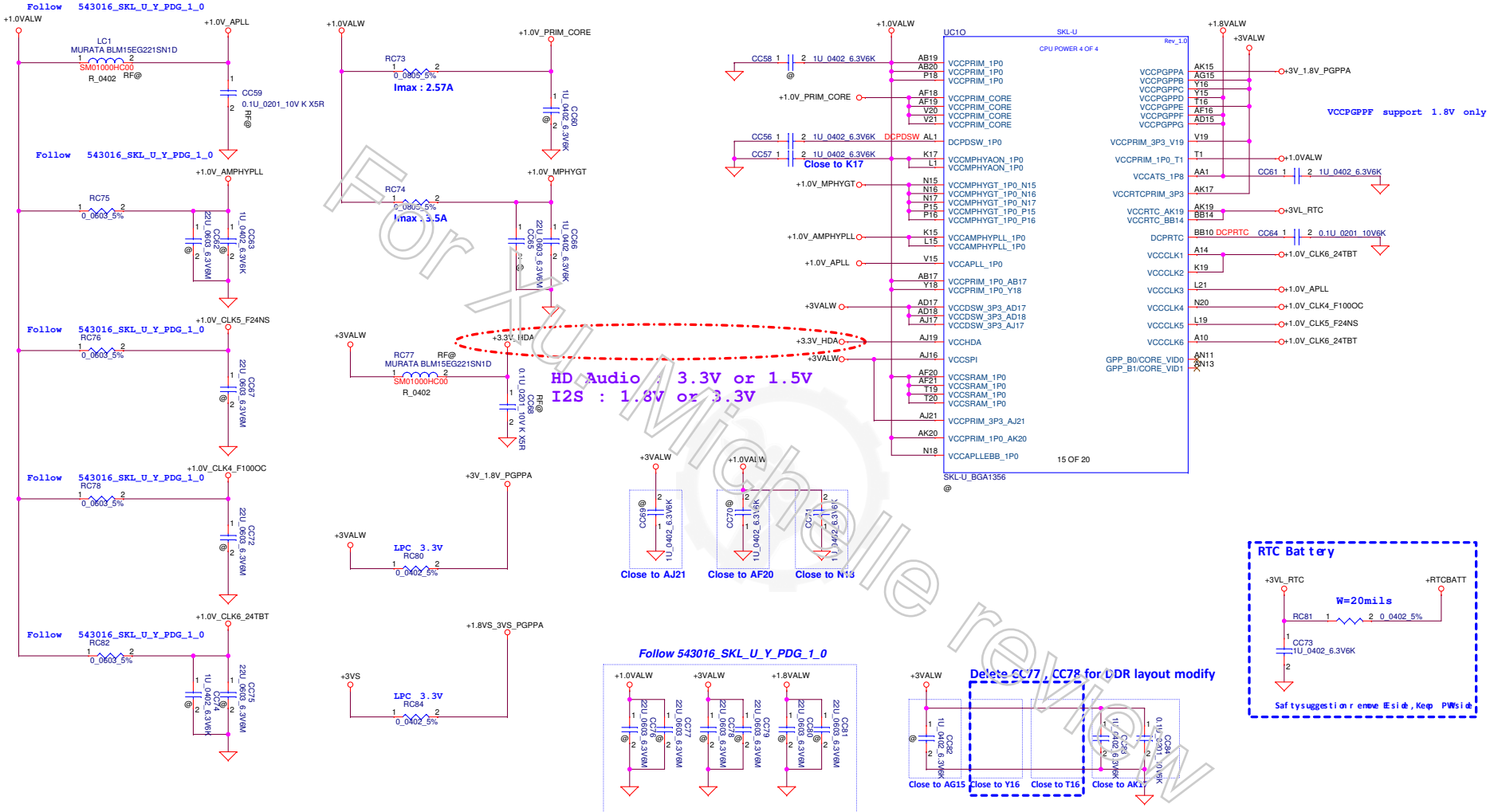






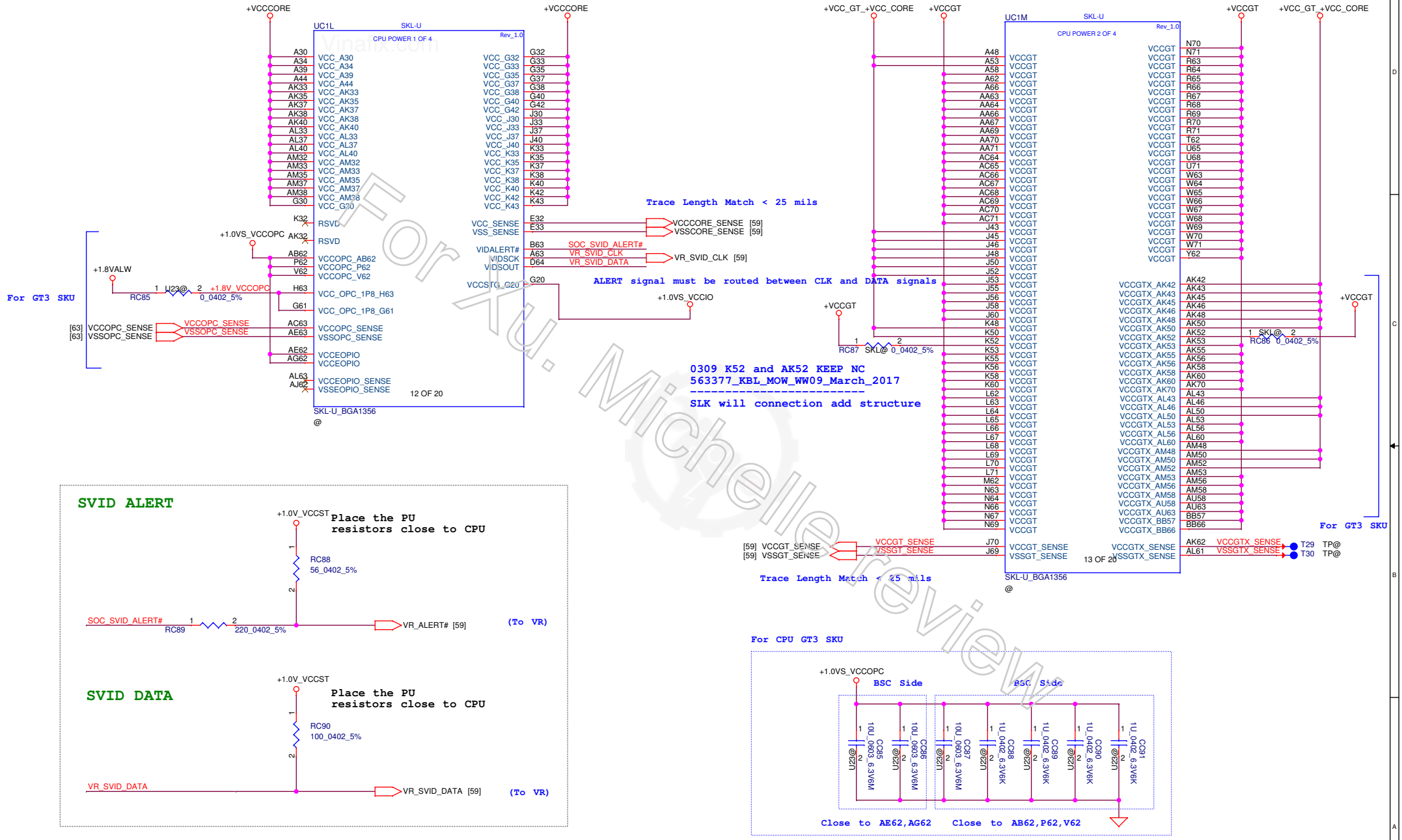
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SKL-U(8/12)Power			
Size: Custom	Document Number: LA-D562P		Rev: 0.1
Date: Thursday, June 15, 2017	Sheet 13 of 66		



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
Size: Custom	Document Number: LA-D562P		Rev: 0.1
Date: Thursday, June 15, 2017	Sheet 14 of 66		



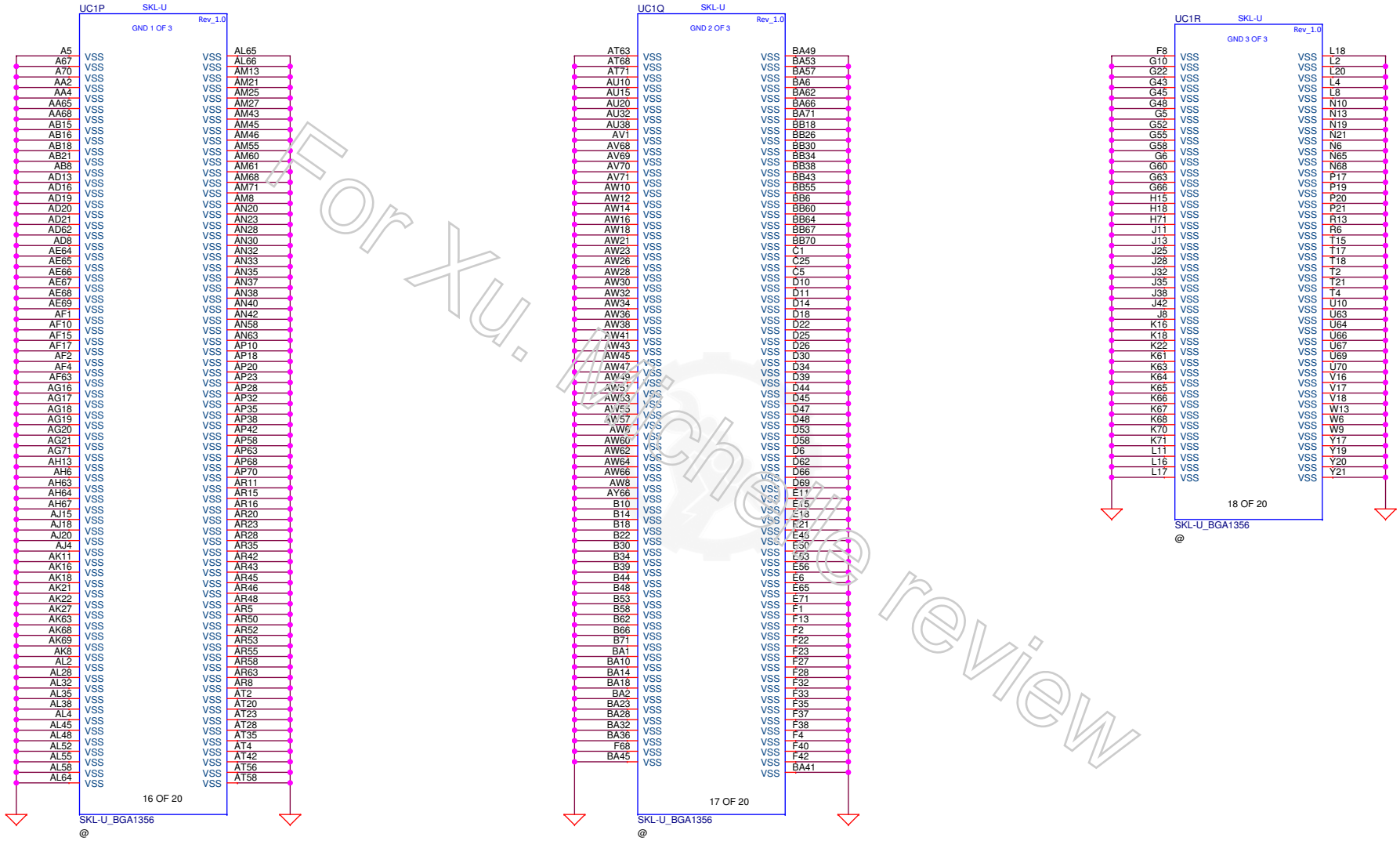
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size	Document Number	Rev
Custom	LA-D562P	0.1

Date: Thursday, June 15, 2017 Sheet 15 of 66



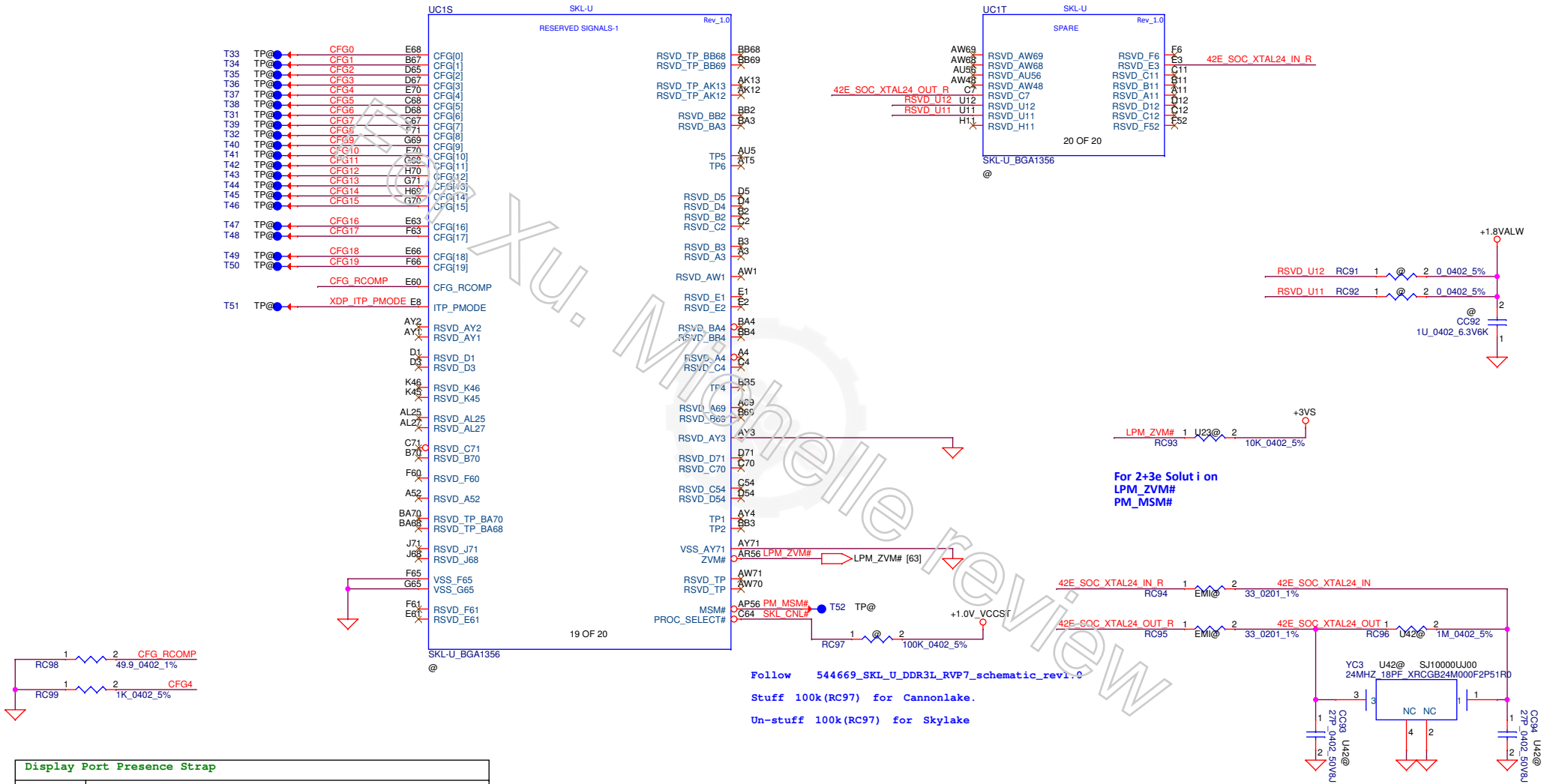
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size	Document Number	Rev
Custom	LA-D562P	0.1

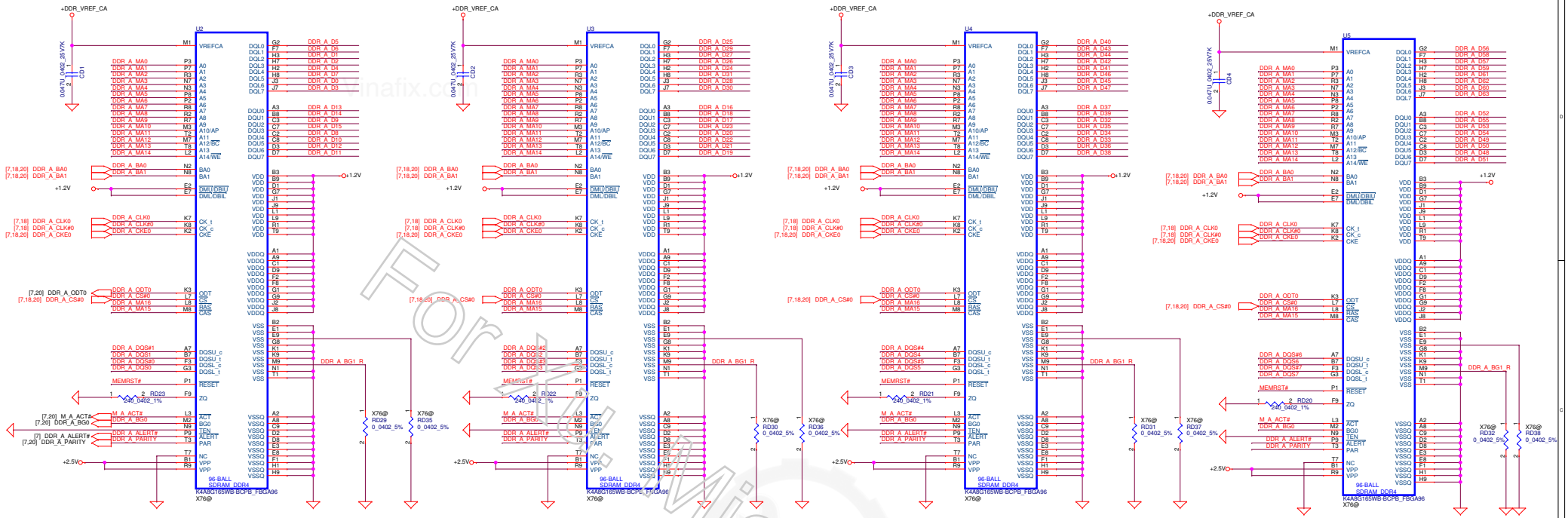
Date: Thursday, June 15, 2017 Sheet 16 of 66



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

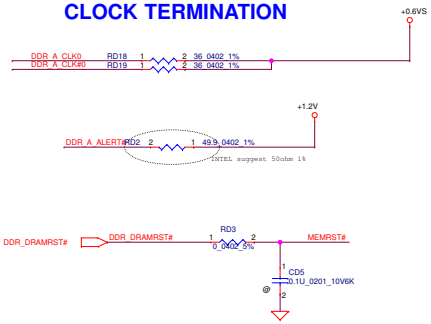
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SKL-U(12/12)CFG,RSVD			
Size: Custom	Document Number: LA-D562P		Rev: 0.1
Date: Thursday, June 15, 2017	Sheet 17 of 66		



[7,20] DDR_A_MA[0..16]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_DQS[0..7]
[7] DDR_A_D[0..63]

CLOCK TERMINATION

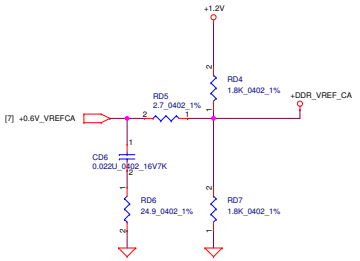


0606 add

TABLE

	SDP	DDP
RD29 RD30 RD31 RD32	ASM ASM ASM ASM	NA NA NA NA
RD33	NA	ASM
RD34	NA	ASM
RD35 RD36 RD37 RD38	0_5% 0_5% 0_5% 0_5%	243_1% 243_1% 243_1% 243_1%

LOGIC



Data mapping

U2	DQ	U3	DQ	U4	DQ	U5	DQ
DQL0	D3	DQL0	D19	DQL0	D35	DQL0	D51
DQL1	D1	DQL1	D17	DQL1	D33	DQL1	D49
DQL2	D2	DQL2	D18	DQL2	D34	DQL2	D50
DQL3	D0	DQL3	D16	DQL3	D32	DQL3	D48
DQL4	D7	DQL4	D23	DQL4	D39	DQL4	D55
DQL5	D5	DQL5	D21	DQL5	D37	DQL5	D53
DQL6	D6	DQL6	D22	DQL6	D38	DQL6	D54
DQL7	D4	DQL7	D20	DQL7	D36	DQL7	D52
DQU0	D10	DQU0	D26	DQU0	D42	DQU0	D58
DQU1	D8	DQU1	D24	DQU1	D40	DQU1	D56
DQU2	D11	DQU2	D27	DQU2	D43	DQU2	D59
DQU3	D9	DQU3	D25	DQU3	D41	DQU3	D57
DQU4	D14	DQU4	D30	DQU4	D46	DQU4	D62
DQU5	D13	DQU5	D29	DQU5	D45	DQU5	D61
DQU6	D15	DQU6	D31	DQU6	D47	DQU6	D63
DQU7	D12	DQU7	D28	DQU7	D44	DQU7	D60

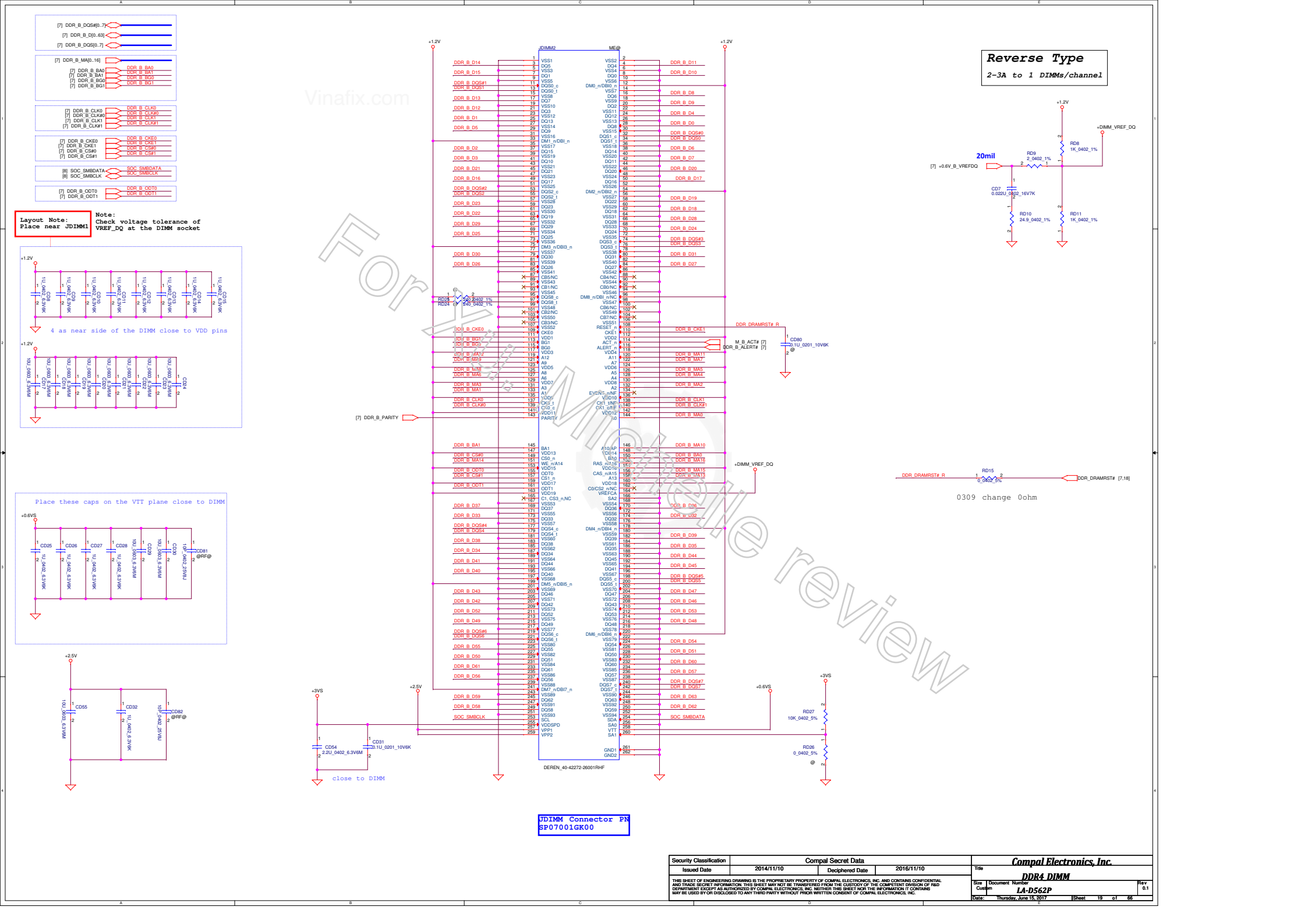
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics

Title: DDR4 ON BOARD CHIPS

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, June 15, 2017 | Sheet 18 of 66



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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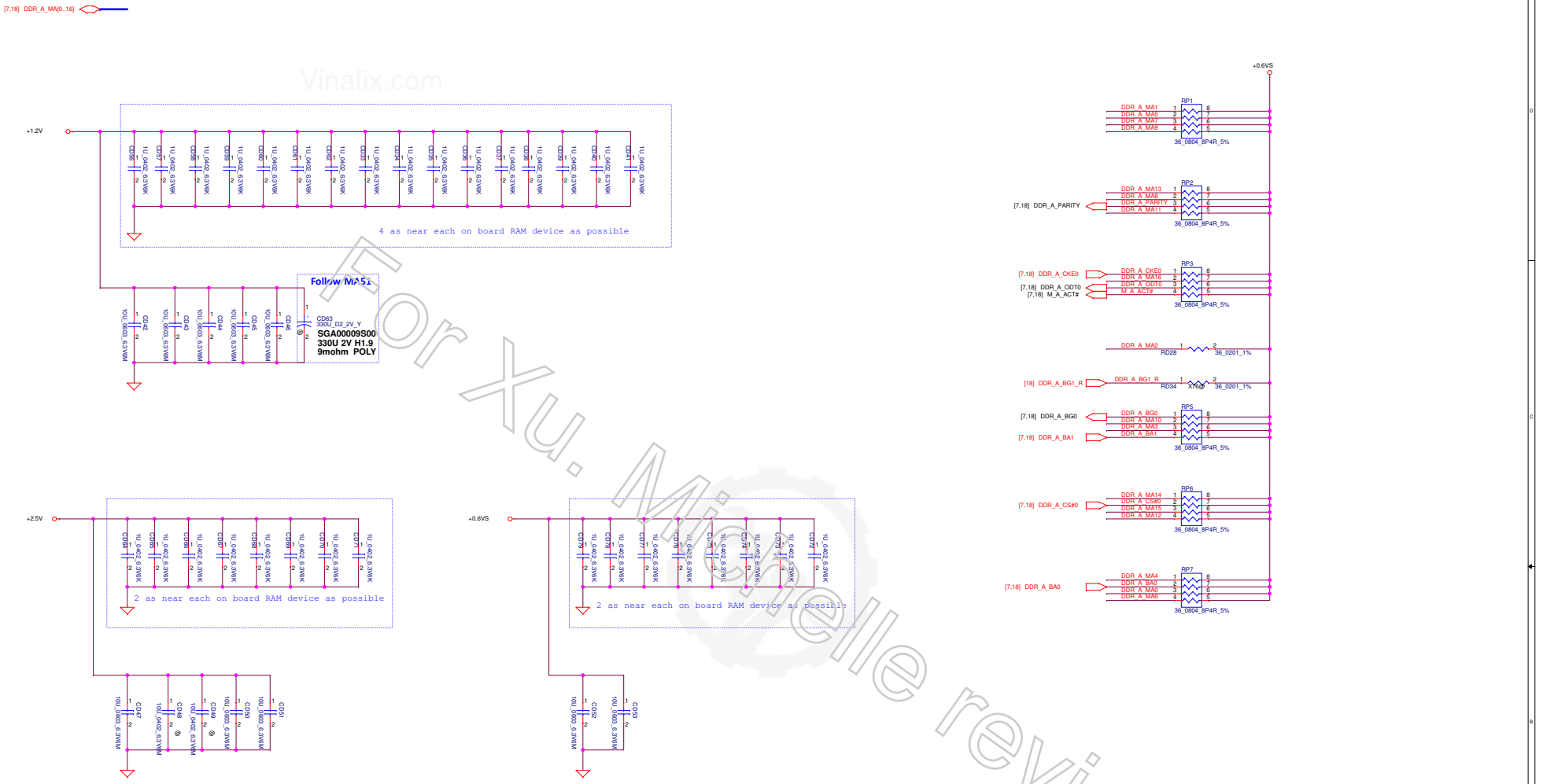
Compal Electronics, Inc.

Title: DDR4 DIMM

Size: Custom | Document Number: LA-D562P | Rev: 0.1

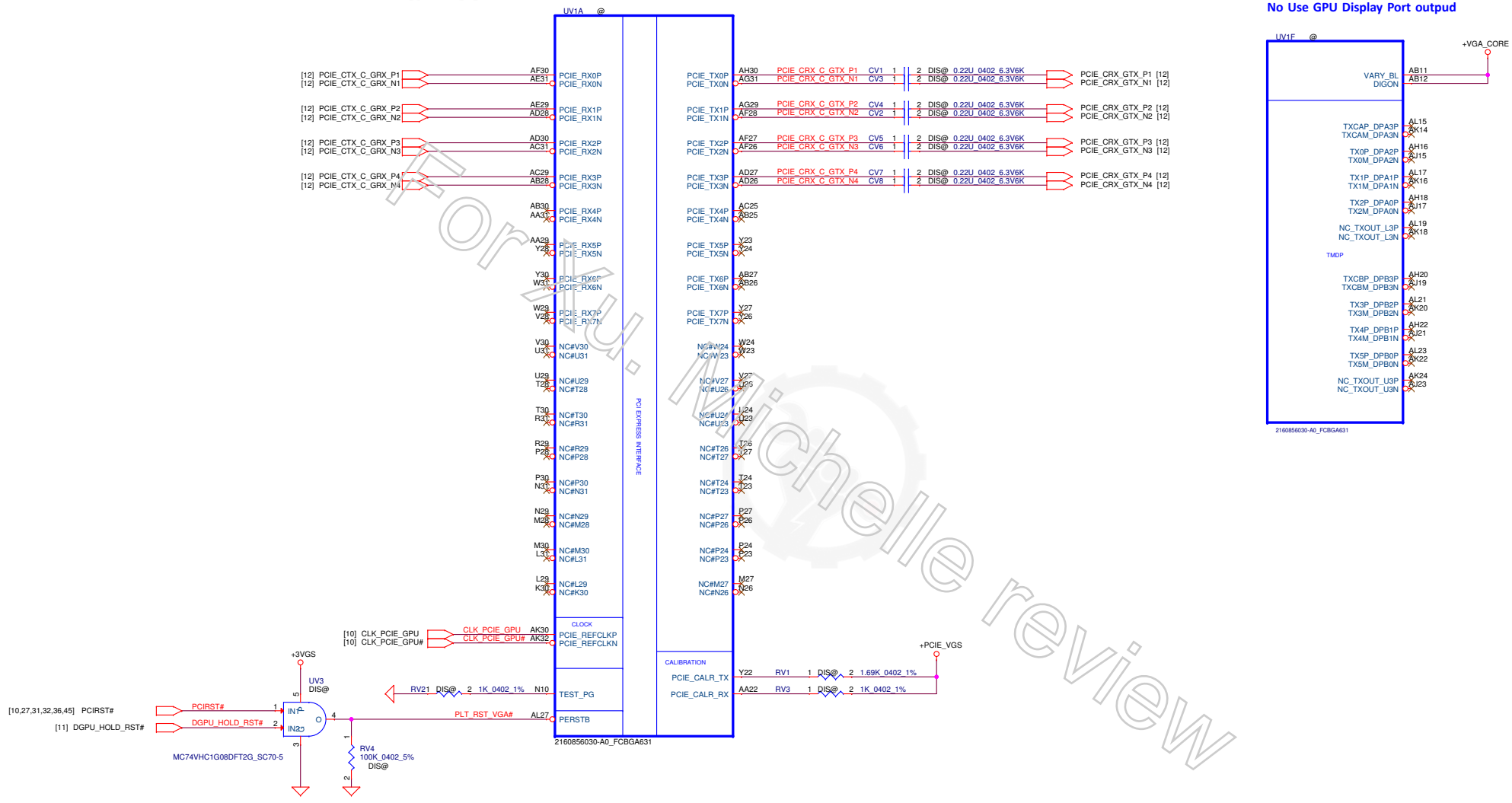
Date: Thursday, June 15, 2017 | Sheet 19 of 66



Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Title: **DDR4 ON BOARD CHIPS**

Size: Custom	Document Number	Rev: 0.1
Date: Thursday, June 15, 2017	Sheet 20 of 66	



No Use GPU Display Port outpud

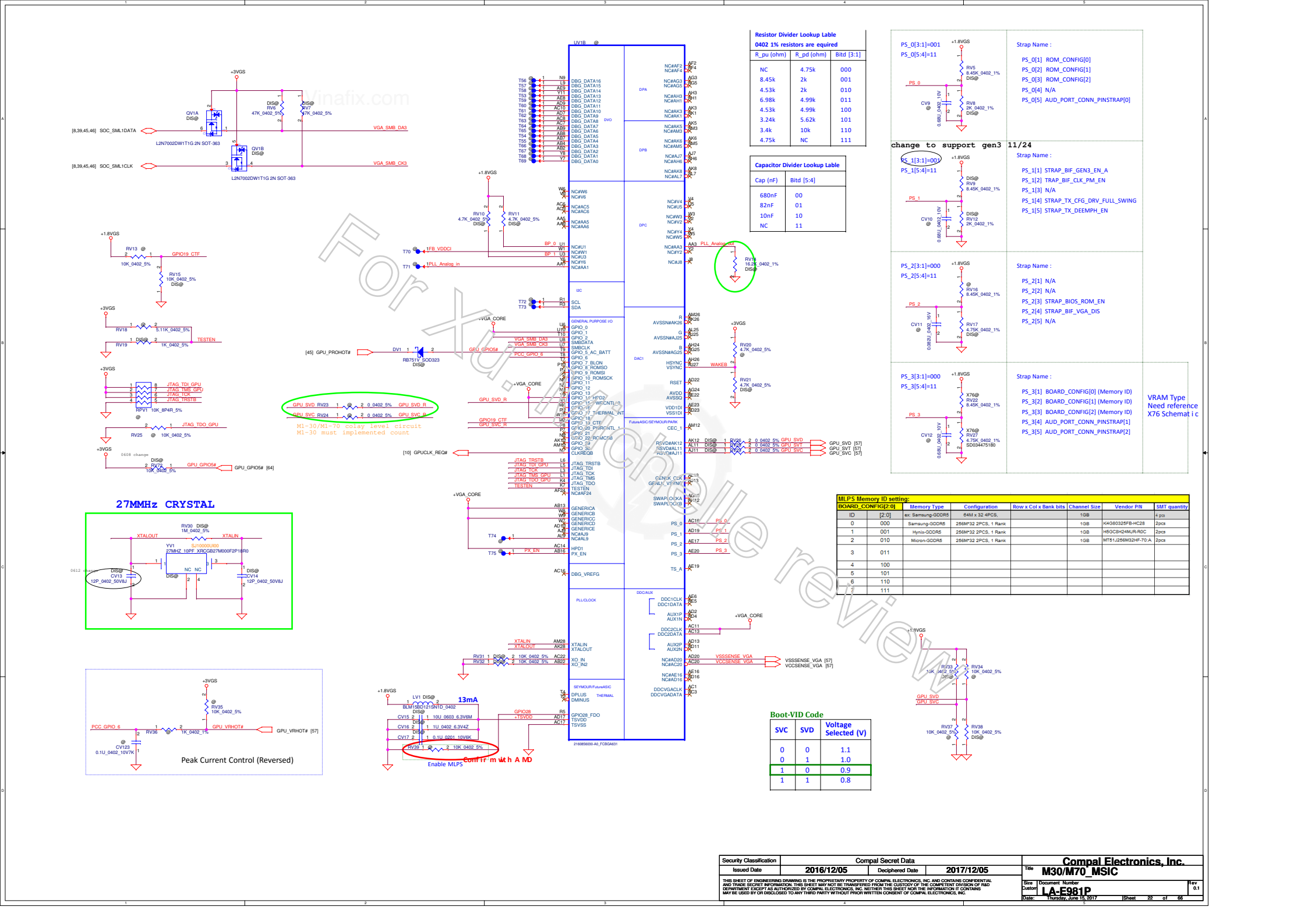
Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/12/05

Compal Electronics, Inc.

Title: **M30/M70_PCIE/DP**

Size: Custom | Document Number: **LA-E981P** | Rev: 0.1

Date: Thursday, June 15, 2017 | Sheet 21 of 66


Resistor Divider Lookup Lable
0402 1% resistors are equired
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
change to support gen3 11/24
PS_1[3:1]=001
PS_1[5:4]=11
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=11
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
VRAM Type
Need reference
X76 Schemat i c
MLPS Memory ID setting:
BOARD_CONFIG[2:0] | Memory Type | Configuration | Row x Col x Bank bits | Channel Size | Vendor P/N | SMT quantity
ID | [2:0] | ex: Samsung-GDDR5 | 64M x 32 4PCS, | 1GB | | 4 pcs
0 | 000 | Samsung-GDDR5 | 256M*32 2PCS, 1 Rank | 1GB | K4G80325FB-HC28 | 2pcs
1 | 001 | Hynix-GDDR5 | 256M*32 2PCS, 1 Rank | 1GB | H5GC8H24MJR-R0C | 2pcs
2 | 010 | Micron-GDDR5 | 256M*32 2PCS, 1 Rank | 1GB | MT51J256M32HF-70:A | 2pcs
3 | 011
4 | 100
5 | 101
6 | 110
7 | 111
27MMHz CRYSTAL
M1-30/M1-70 colay level circuit
M1-30 must implemented count
13mA
Confirm with AMD
Enable MLPS
Peak Current Control (Reversed)
Boot-VID Code
SVC | SVD | Voltage Selected (V)
0 | 0 | 1.1
0 | 1 | 1.0
1 | 0 | 0.9
1 | 1 | 0.8
For Xu Michelle review
Security Classification | Compal Secret Data
Issued Date | 2016/12/05 | Deciphered Date | 2017/12/05
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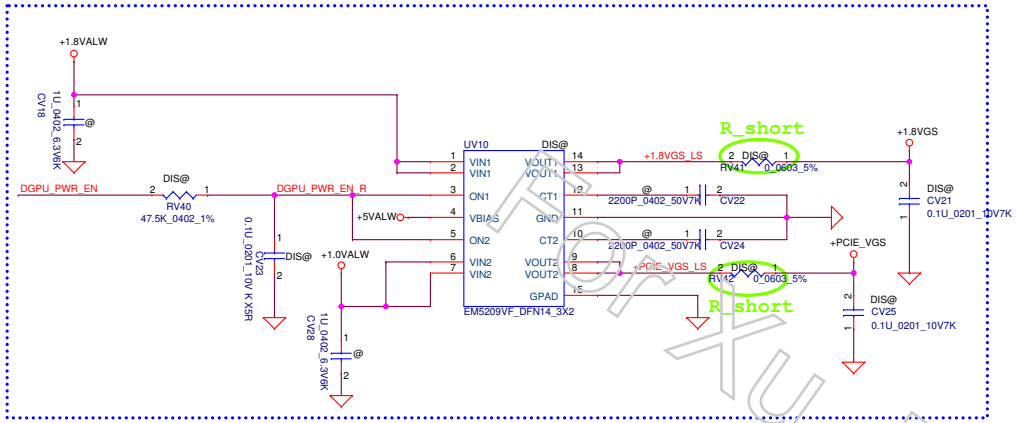
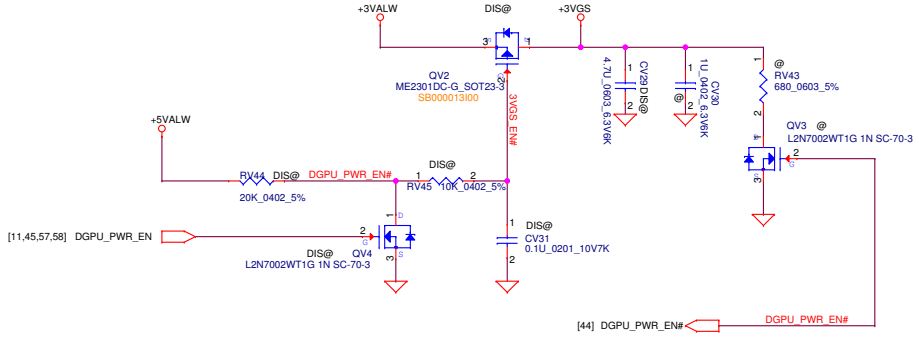
Compal Electronics, Inc.
Title M30/M70_MSIC
Size Custom | Document Number LA-E981P | Rev 0.1
Date: Thursday, June 15, 2017 | Sheet 22 of 66

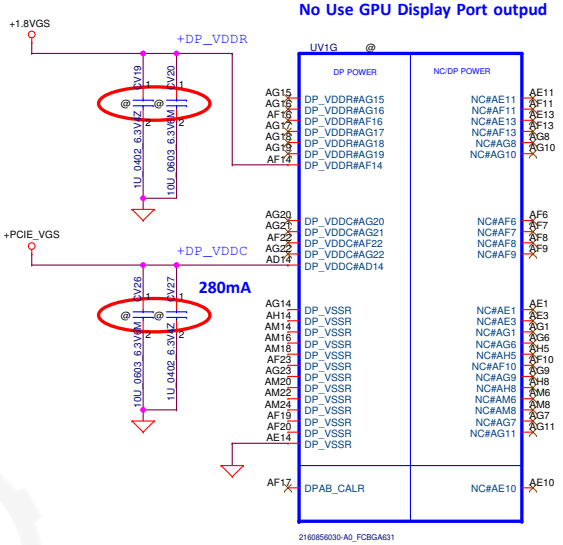
+1.8VALW TO +1.8VGS
+1.0VALW TO +PCIE_VGS
Load switch

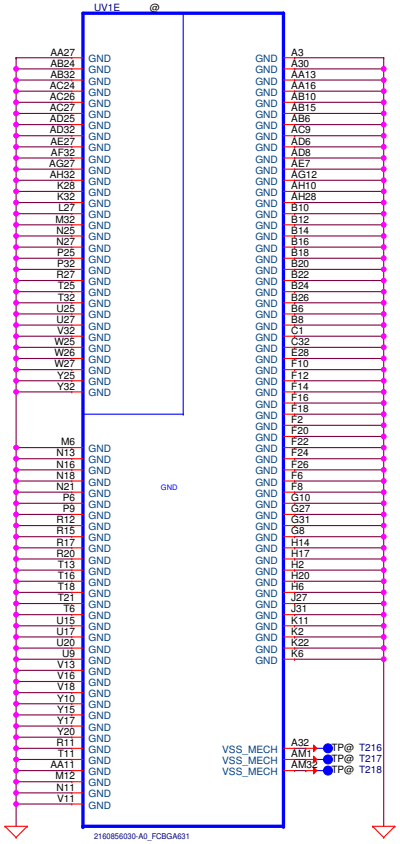


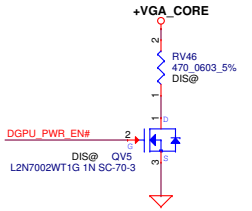
+3VALW to +3VGS

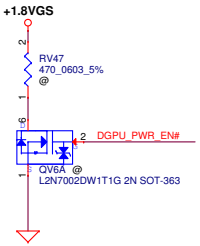


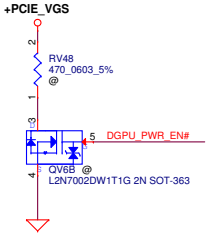
No Use GPU Display Port outpud











Title	<Title>		
Size	Document Number		Rev
Custom	LA-E981P		0.1
Date:	Thursday, June 15, 2017	Sheet 23 of 66	

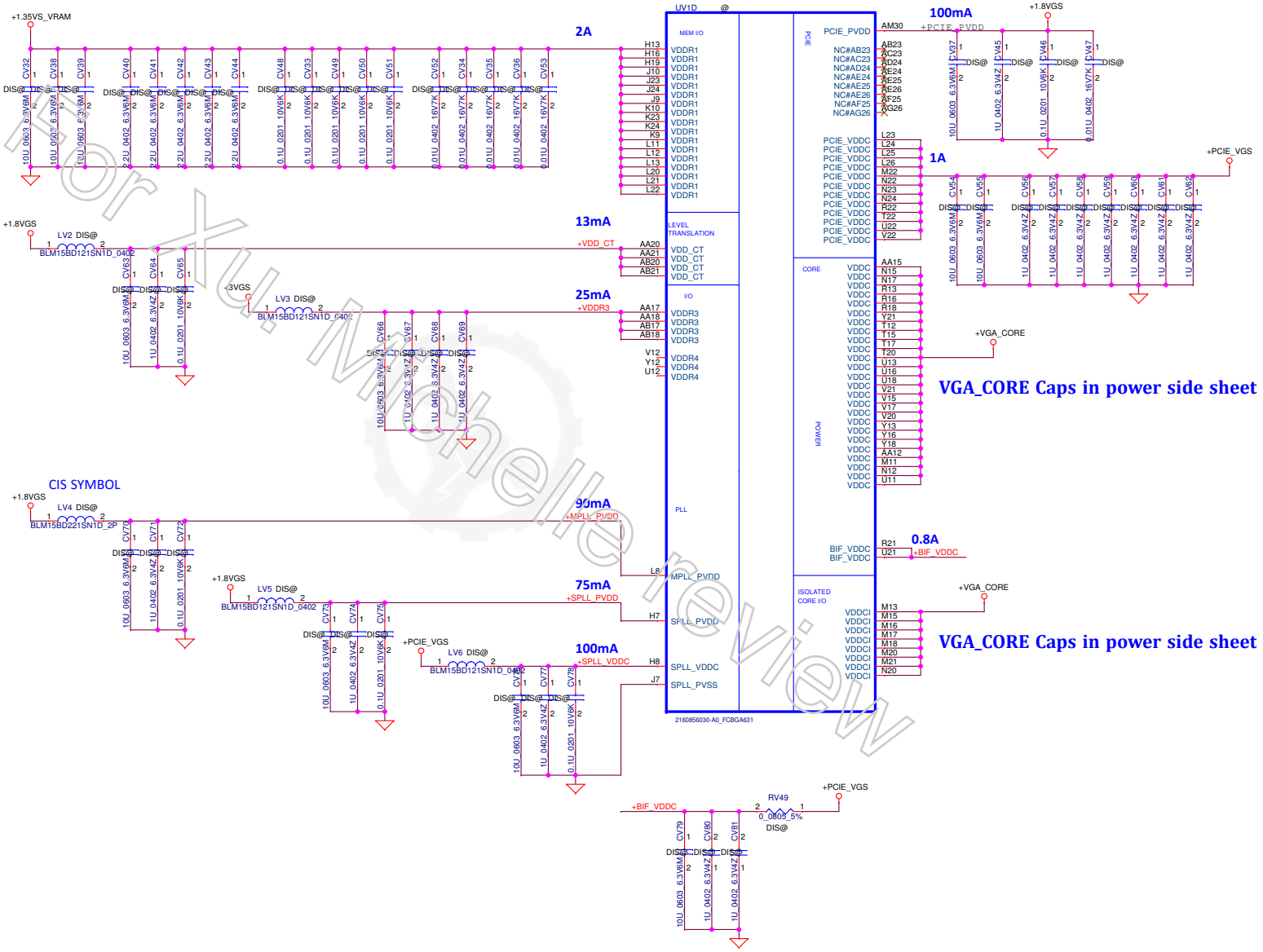
+VGA_CORE	10uF	1uF	0.1uF
VDDC VDDC and VDDCI TDC 28A	4	30	0
VDDCI	1	3	3

+PCIE_VGS		10uF	1uF	0.1uF
PCIE_VDDC	2A	2	7	0
BIF_VDDC	0.8A	1	2	0
SPLL_VDDC	100mA	1	1	1

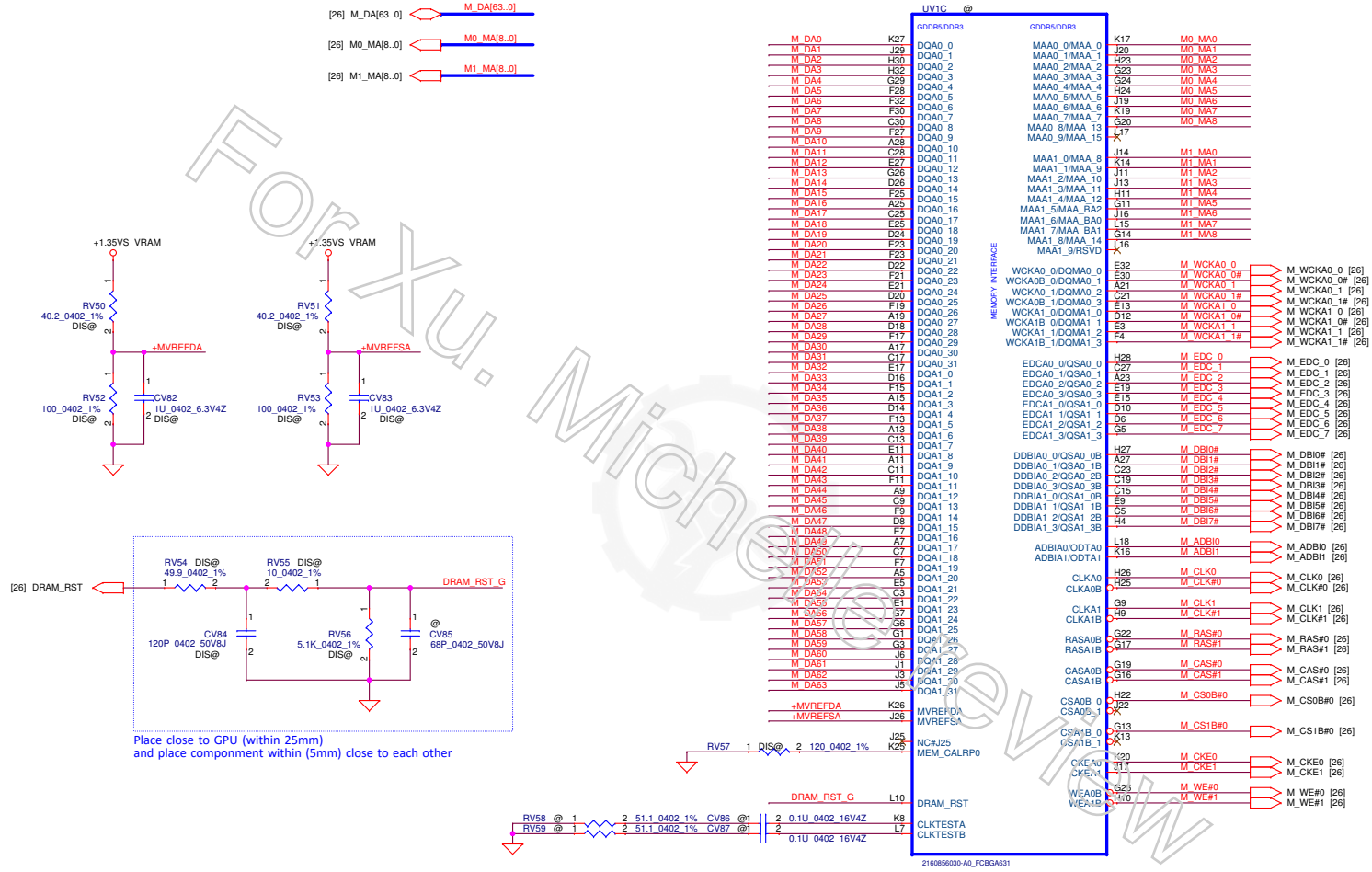
+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 2A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF	0.01uF
PCIE_PVDD	100mA	1	1	1	1
MPLL_PVDD	90mA	1	1	1	0
SPLL_PVDD	75mA	1	1	1	0
VDD_CT	13mA	1	1	1	0
+DP_VDDR	40mA	1(@)	1(@)	1(@)	0
+DP_VDDC		1(@)	1(@)	1(@)	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	1	3	0



Title	<Title>		
Size	Document Number		Rev
Custom	LA-E981P		0.1
Date:	Thursday, June 15, 2017	Sheet 24 of 66	



Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/12/05

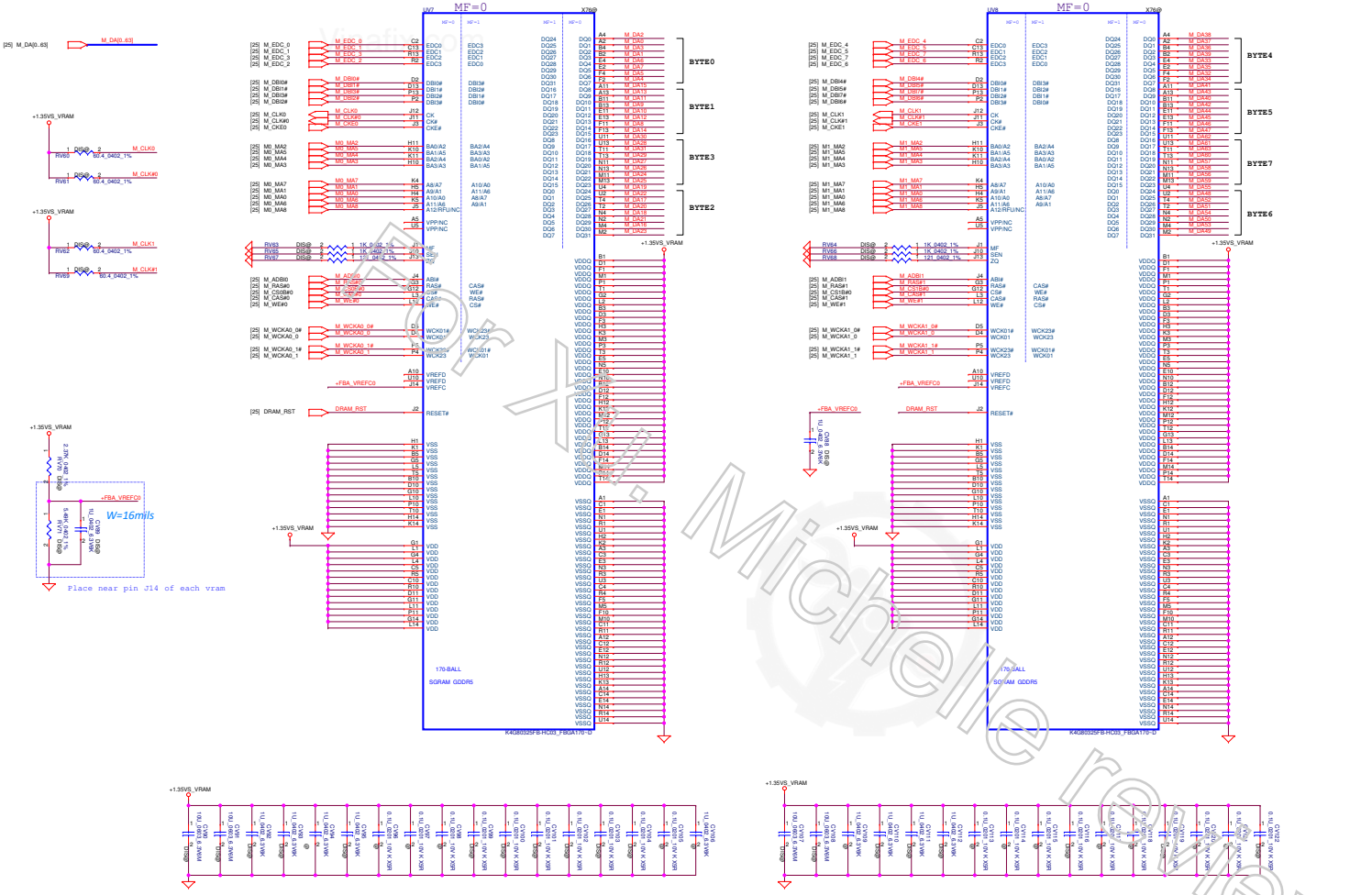
Compal Electronics, Inc.

Title: **M30/M70_MEM**

Size: Custom | Document Number: **LA-E981P** | Rev: 0.1

Date: Thursday, June 15, 2017 | Sheet 25 of 66

Memory Partition A

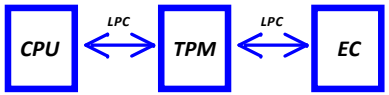


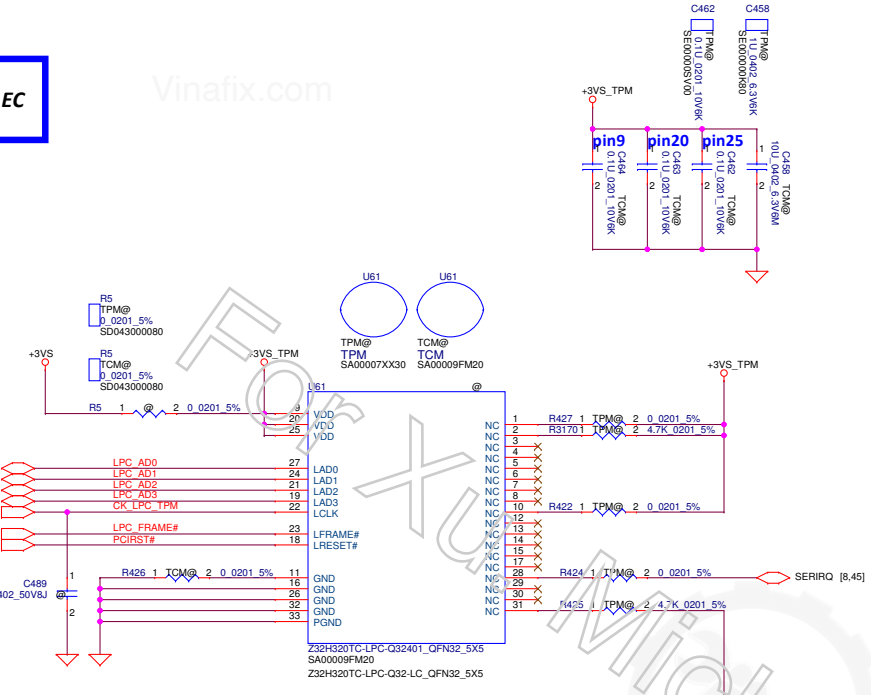
Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/12/05

Compal Electronics, Inc.			
Title: GDDR5_A0			
Size:	Document Number: LA-E981P		Rev: 0.1
Date: Thursday, June 15, 2017		Sheet: 25 of 55	

TPM 2.0

Layout Routing





TPM/TCP Colay

	Nationz Infineon TCM	TPM		Nationz Infineon TCM	TPM
Pin1	NC	VDD	Pin17	NC	NC
Pin2	NC	GPIO	Pin18	LRESET#	LRESET#
Pin3	NC	NC	Pin19	LAD3	LAD3
Pin4	NC	NC	Pin20	VDD	VDD
Pin5	NC	NC	Pin21	LAD2	LAD2
Pin6	NC	NC	Pin22	LCLK	LCLK
Pin7	NC	NC	Pin23	LFRAME#	LFRAME#
Pin8	NC	NC	Pin24	LAD1	LAD1
Pin9	VDD	VDD	Pin25	VDD	VDD
Pin10	NC	VDD	Pin26	GND	GND
Pin11	GND	NC	Pin27	LAD0	LAD0
Pin12	NC	NC	Pin28	NC	SERIRQ
Pin13	NC	NC	Pin29	NC	NC
Pin14	NC	NC	Pin30	NC	NC
Pin15	NC	GND	Pin31	NC	PP
Pin16	GND	GND	Pin32	GND	GND

Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

Compal Electronics, Inc.		
Title: TPM/TCM		
Size	Document Number: LA-E581P	Rev: 0.1
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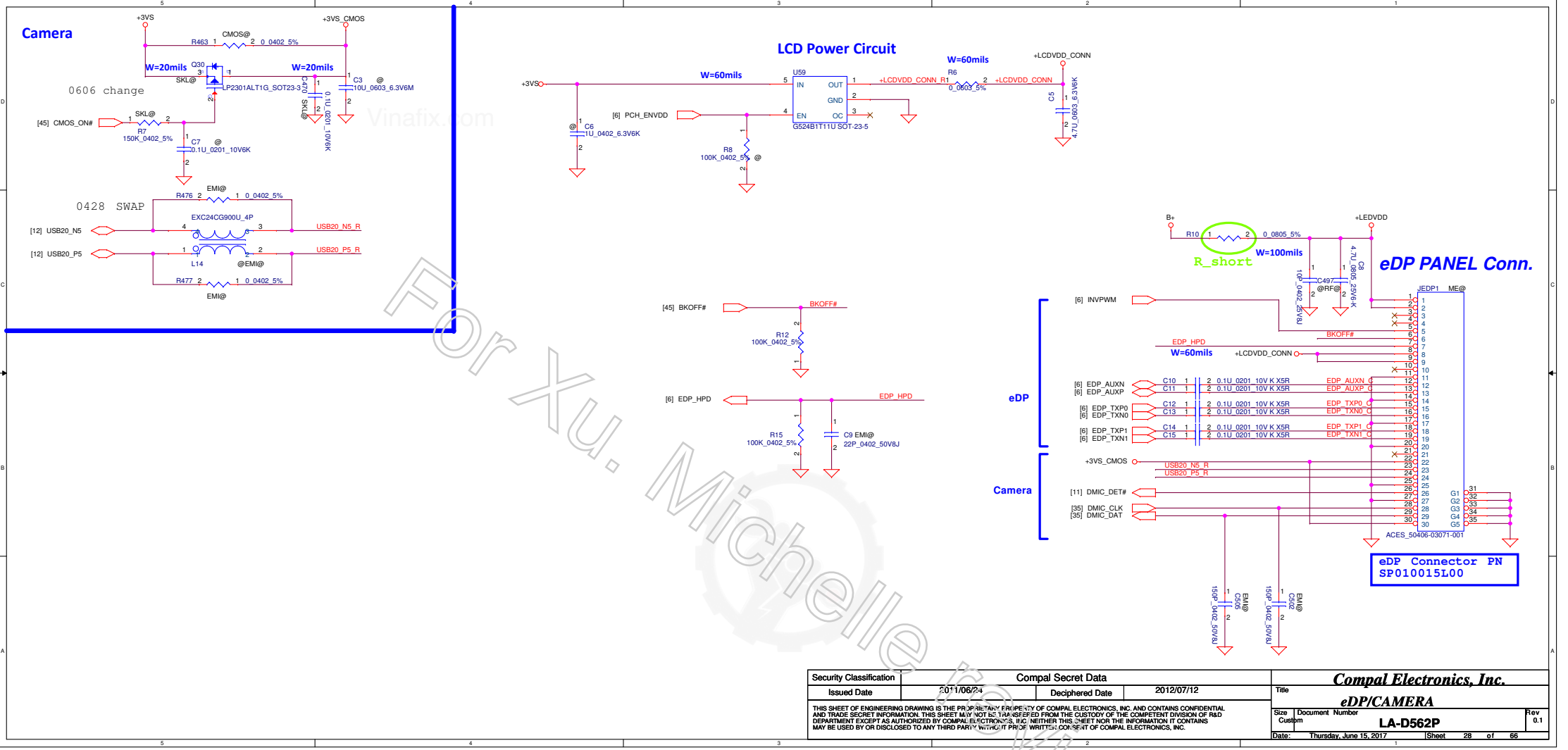

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: eDP/CAMERA

Size: Custom | Document Number: LA-D562P | Rev: 0.1

Date: Thursday, June 15, 2017 | Sheet 28 of 66

EMI

Near JHDMI1

Near JHDMI1

[6] HDMI_CLK-_CK — C17 0.1U_0201_10V6K — HDMI_CLK-_CK_C
[6] HDMI_CLK+_CK — C20 0.1U_0201_10V6K — HDMI_CLK+_CK_C
[6] HDMI_TX0-_CK — C21 0.1U_0201_10V6K — HDMI_TX0-_CK_C
[6] HDMI_TX0+_CK — C22 0.1U_0201_10V6K — HDMI_TX0+_CK_C
[6] HDMI_TX1-_CK — C23 0.1U_0201_10V6K — HDMI_TX1-_CK_C
[6] HDMI_TX1+_CK — C24 0.1U_0201_10V6K — HDMI_TX1+_CK_C
[6] HDMI_TX2-_CK — C25 0.1U_0201_10V6K — HDMI_TX2-_CK_C
[6] HDMI_TX2+_CK — C26 0.1U_0201_10V6K — HDMI_TX2+_CK_C

EMI@ R16 0_0402_5% — HDMI_CLK-_CONN — R17 @EMI@ 150_0402_5%
EMI@ R18 0_0402_5% — HDMI_CLK+_CONN
EMI@ R19 0_0402_5% — HDMI_TX0-_CONN — R20 @EMI@ 150_0402_5%
EMI@ R21 0_0402_5% — HDMI_TX0+_CONN
EMI@ R22 0_0402_5% — HDMI_TX1-_CONN — R24 @EMI@ 150_0402_5%
EMI@ R25 0_0402_5% — HDMI_TX1+_CONN
EMI@ R27 0_0402_5% — HDMI_TX2-_CONN — R28 @EMI@ 150_0402_5%
EMI@ R29 0_0402_5% — HDMI_TX2+_CONN

For HDMI

U9 G5250Q1T73U SOT-23
+5VS — @ C19 0.1U_0201_10V6K — IN
OUT — W=40mils — +5V_DSP
GND — C18 0.1U_0201_10V6K

+3VS — R23 1M_0402_5% — Q2 2N7002K_SOT23-3
[6] TMDS_B_HPD — R26 20K_0402_5% — HDMI_DET

+5V_DSP — JHDMI1 ME@ ACON_HMRA3-AK120C

HDMI_DET	19	HP_DET	
	18	+5V	
HDMIDAT_R	17	DDC/CEC_GND	
HDMICLK_R	16	SDA	
	15	SCL	
	14	Reserved	
	13	CEC	
HDMI_CLK-_CONN	12	CK-	GND 20
HDMI_CLK+_CONN	11	CK_shield	GND 21
HDMI_TX0-_CONN	10	CK+	GND 22
	9	D0-	GND 23
HDMI_TX0+_CONN	8	D0_shield	
HDMI_TX1-_CONN	7	D0+	
	6	D1-	
HDMI_TX1+_CONN	5	D1_shield	
HDMI_TX2-_CONN	4	D1+	
	3	D2-	
HDMI_TX2+_CONN	2	D2_shield	
	1	D2+	

HDMI Connector PN DC232003A00

+3VS — R30 2.2K_0402_5% — HDMIDAT_NB
+3VS — R31 2.2K_0402_5% — HDMICLK_NB

HDMIDAT_NB(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

+3VS — Q3A L2N7002DW1T1G 2N SC88-6
[6] HDMICLK_NB — HDMICLK_R
[6] HDMIDAT_NB — HDMIDAT_R
Q3B L2N7002DW1T1G 2N SC88-6

+5V_DSP — R32 2.2K_0402_5% — HDMIDAT_R
+5V_DSP — R33 2.2K_0402_5% — HDMICLK_R

HDMI_TX1-_CK_C — RP8 — 470 +-5% 8P4R — HDMI_TX1-_CONN
HDMI_TX1+_CK_C — HDMI_TX1+_CONN
HDMI_TX2-_CK_C — HDMI_TX2-_CONN
HDMI_TX2+_CK_C — HDMI_TX2+_CONN

HDMI_CLK-_CK_C — RP9 — 470 +-5% 8P4R — HDMI_CLK-_CONN
HDMI_CLK+_CK_C — HDMI_CLK+_CONN
HDMI_TX0-_CK_C — HDMI_TX0-_CONN
HDMI_TX0+_CK_C — HDMI_TX0+_CONN

+3VS — Q4 2N7002K_SOT23-3

ESD

D1 ESD@ L05ESDL5V0NA-4_SLP2510P8-10-9 SC300003Z00

HDMIDAT_R	9	1	HDMIDAT_R
HDMICLK_R	8	2	HDMICLK_R
HDMI_DET	7	4	HDMI_DET
	6	5	
		3	

D2 ESD@ L05ESDL5V0NA-4_SLP2510P8-10-9 SC300003Z00

HDMI_CLK-_CONN	9	1	HDMI_CLK-_CONN
HDMI_CLK+_CONN	8	2	HDMI_CLK+_CONN
HDMI_TX0-_CONN	7	4	HDMI_TX0-_CONN
HDMI_TX0+_CONN	6	5	HDMI_TX0+_CONN
		3	

D3 ESD@ L05ESDL5V0NA-4_SLP2510P8-10-9 SC300003Z00

HDMI_TX1-_CONN	9	1	HDMI_TX1-_CONN
HDMI_TX1+_CONN	8	2	HDMI_TX1+_CONN
HDMI_TX2-_CONN	7	4	HDMI_TX2-_CONN
HDMI_TX2+_CONN	6	5	HDMI_TX2+_CONN
		3	

ZZZ15 45@ HDMI Logo RO0000003HM

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: HDMI CONN

Size	Document Number	Rev
C	LA-D562P	0.1

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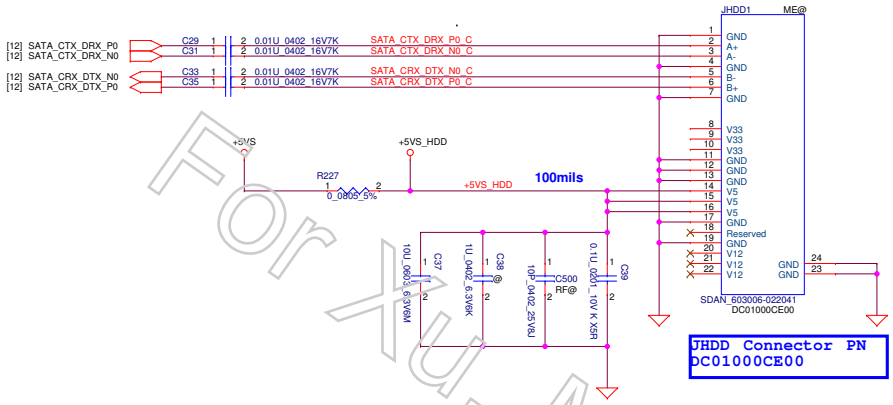
HDD

SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: **HDD/ODD Connector**

Size	Document Number	Rev
C	LA-D562P	0.1

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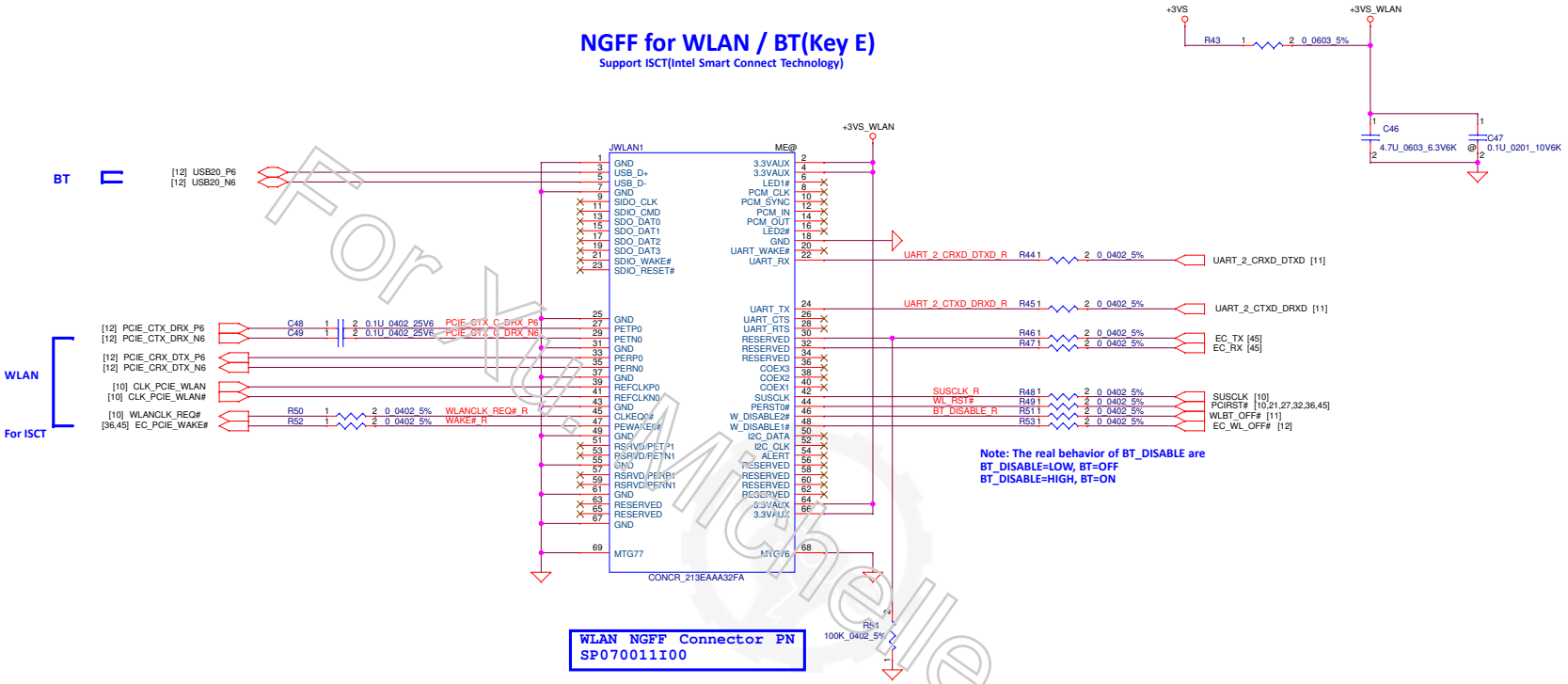
NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)



Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

WLAN NGFF Connector PN
SP070011I00

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

Size	Document Number	Rev
	LA-D562P	0.1

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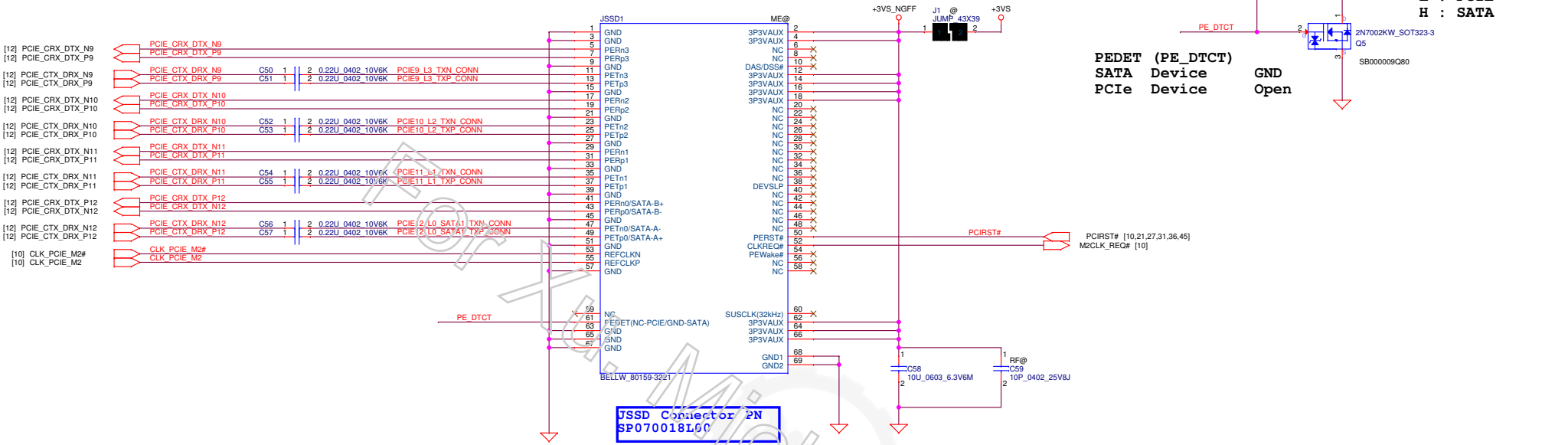
M.2 mSATA Conn



Security Classification	Compal Secret Data		
Issued Date	2015/03/06	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **M.2 SSD**

Size: Custom | Document Number: **Merlyn LA-D211P** | Rev: 0.1

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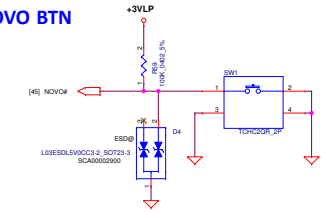
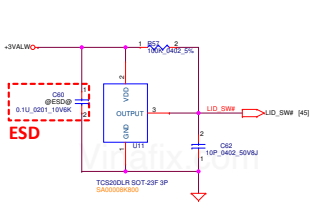
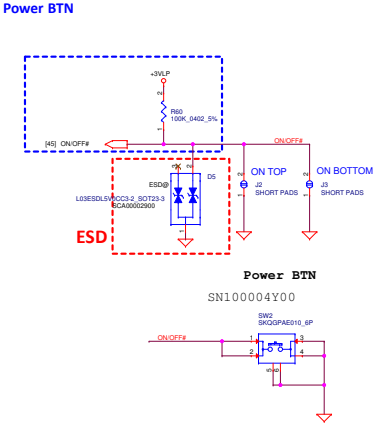
NOVO BTN



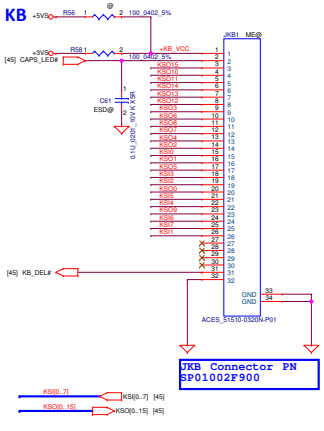
LID



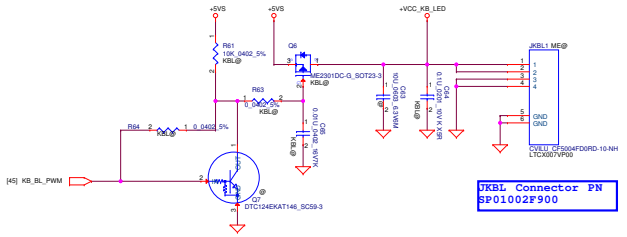
Power BTN



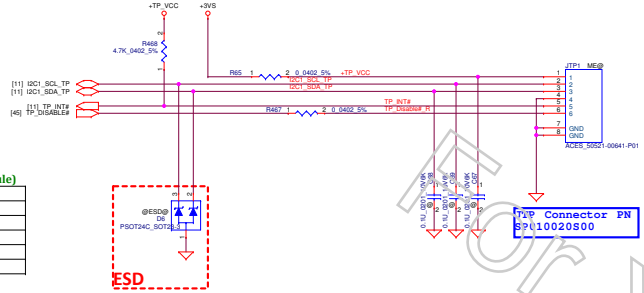
KB



Keyboard Backlight



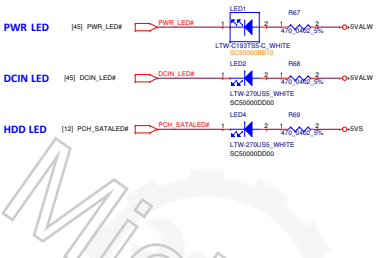
ClickPad



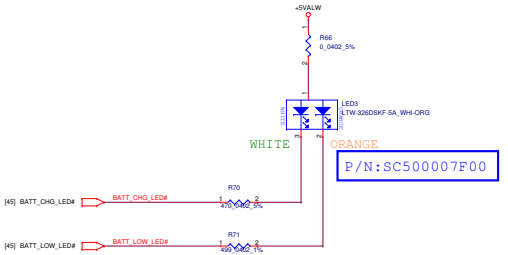
Click Pad Pin define(Module)

Pin1	VDD_3.3V
Pin2	SCL
Pin3	SDA
Pin4	GND
Pin5	INT
Pin6	LID CLOSE

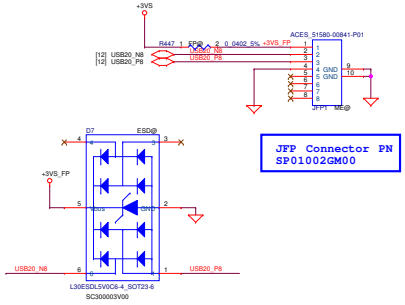
LED



Charge LED



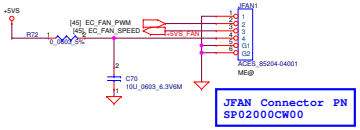
FingerPrint



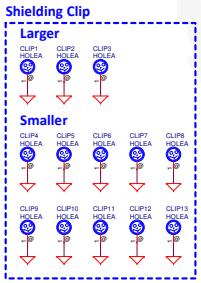
FP Pin define(Module)

Pin1	NC
Pin2	NC
Pin3	NC
Pin4	NC
Pin5	GND
Pin6	D+
Pin7	D-
Pin8	3.3VCC

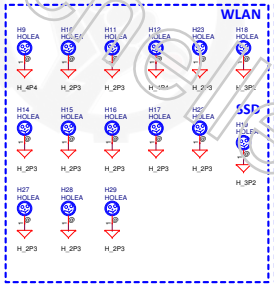
FAN Conn



Shielding Clip



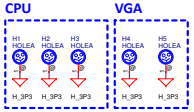
WLAN



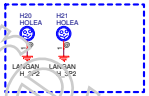
Thermal

CPU

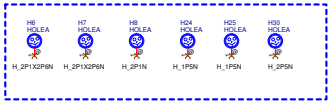
VGA



LAN



NPTH



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Title	Compal Electronics, Inc. KBD/PWR/CR/LED/TP Conn.		
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USB 3.0 AOU

+5VALWP

For USB Charger to improve +5VALWP power ripple

V330 only NONAOU

W=80mils +5VALW

W=80mils +5V_CHGUSB

NONAOU@ C71 0.1U_0201_10V K X5R

U55_NONAOU@ SY6288D20AAC_SOT23-5

[45,46] USB_EN#

R73 0_0402_5% NONAOU@

USB_OC0# [12]

USB20_P1 R232 0_0402_5% USB20_CH_P1

USB20_N1 R233 0_0402_5% USB20_CH_N1

USB 3.0

W=80mils +5VALW

W=80mils +5V_USB

U56 SY6288D20AAC_SOT23-5

USB_EN#

R228 0_0402_5%

USB_OC1# [12]

C248 0.1U_0201_10V K X5R

+3VALW +5VALW_USBCH +5V_CHGUSB

U12 AOU@ TPS2546RTER QFN 16P SA000064O00

80mil

[45] USB_CHG_STATUS#

USB_CHG# 0606 change

[45] USB_CHG_ILIM_SEL

[45] USB_CHG_EN

[45] USB_CHG_CTL1

[45] USB_CHG_CTL2

[45] USB_CHG_CTL3

USB_OC0# [12]

USB20_CH_P1 USB20_CH_N1 USB20_N1 [12] USB20_P1 [12]

USB3.0 With USB2.0 For Charge

C76 0.1U_0201_10V K X5R

2	DM_OUT	Input/Output	D- data line to USB host controller
3	DP_OUT	Input/Output	D+ data line to USB host controller

AOU control

+5VL +5VALW_USBCH +5VALW

R231 2 0_0603_5% AOU@

R234 2 0_0603_5% AOU@

Q28 AOU@ ME2301DC-G_SOT23-3

C454 AOU@ 22U_0603_6.3V6M

C453 AOU@ 22U_0603_6.3V6M

+5VL

R446 1 100K_0402_5% AOU@

[40,45,52,53,55] 3V5VALW_PG

Q29 AOU@ 2N7002K_SOT23-3

C466 AOU@ .1U_0402_16V7K

+5V_USB

0411

C499 RF@

C477 470P_0402_50V7K

JUSB2 ME@ ACON_TARAC-3UTU91

USB20_N2_L USB20_P2_L

USB3_RX_N2_R USB3_RX_P2_R USB3_TX_N2_R USB3_TX_P2_R

USB3.0 Connector PN DC23300AGB0

[12] USB3_RX_N2 [12] USB3_RX_P2

R3188 2 RF@ 1 0_0402_5%

L2002 @RF@

DLW21HN900HQ2L_4P

R3189 2 RF@ 1 0_0402_5%

0614 swap L2002,L2003

R3190 2 RF@ 1 0_0402_5%

L2003 @RF@

R3191 2 RF@ 1 0_0402_5%

[12] USB3_TX_N2 C481 0.1U_0201_10V K X5R

[12] USB3_TX_P2 C480 0.1U_0201_10V K X5R

USB3_TX_N2_C USB3_TX_P2_C

[12] USB20_N2 [12] USB20_P2

L11 EMI@ EXC24CG900U_4P

USB20_N2_L USB20_P2_L

USB3.0_Port

+5V_CHGUSB

JUSB1 ME@ ACON_TARAC-3UTU91

USB20_N1_C USB20_P1_C

[12] USB3_RX_N1 [12] USB3_RX_P1

C75 0.1U_0201_10V K X5R C74 0.1U_0201_10V K X5R

USB3_RX_N1 USB3_RX_P1 USB3_TX_N1_C USB3_TX_P1_C

0406 Change Conn

USB3_0 Connector PN DC23300AGB0

+5V_CHGUSB

C246 470P_0402_50V7K

ESD

D43 ESD@ L3SE5DL5V9NA-4_SLP2510P8-10-9 SC300005Z00

USB3_RX_N1 USB3_RX_P1 USB3_TX_N1_C USB3_TX_P1_C

USB3_RX_N1 USB3_RX_P1 USB3_TX_N1_C USB3_TX_P1_C

D8 ESD@ L3SE3DL5V0DK4_SOT23-6 SC300004W00

+5V_CHGUSB

USB20_N1_L USB20_P1_L

USB20_CH_P1 USB20_CH_N1

L13 EMI@ EXC24CG900U_4P

USB20_P1_L USB20_N1_L

ESD

D39 ESD@ L3SE5DL5V9NA-4_SLP2510P8-10-9 SC300003Z00

USB3_RX_N2_R USB3_RX_P2_R USB3_TX_N2_C_R USB3_TX_P2_C_R

USB3_RX_N2_R USB3_RX_P2_R USB3_TX_N2_C_R USB3_TX_P2_C_R

D38 ESD@ L3SE3DL5V0DK4_SOT23-6 SC300004W00

USB20_N2_L USB20_P2_L

+5V_USB

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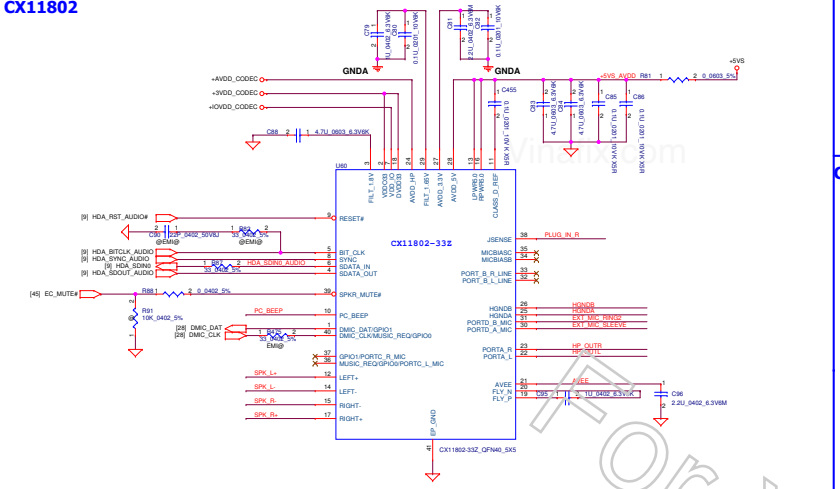
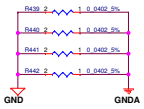
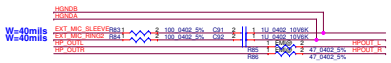
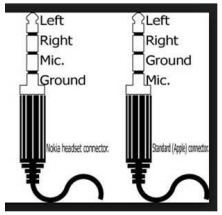
CX11802

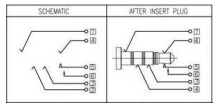




Combo Jack

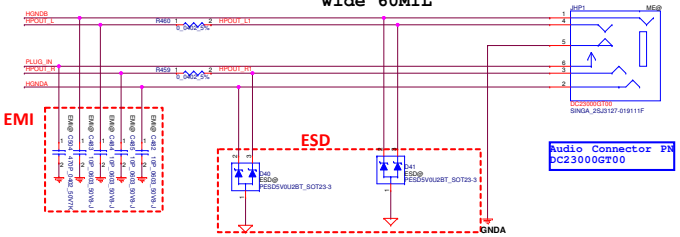






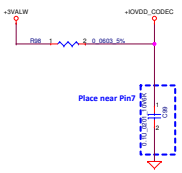
wide 60MIL

Combo Jack
(Normal Open)



place close audio codec

+3VS → +IOVDD_CODEC

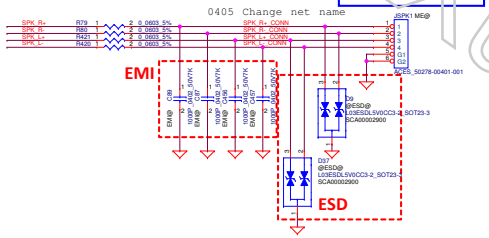


Speaker

wide 40MIL

0405 Change net name

Speaker Connector PN
SP02000PL00

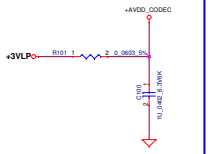


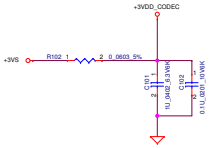
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V	V	V	V	V
Intel Braswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M	V	V	V	V	V

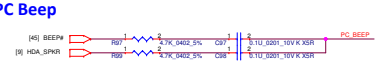
Each Platform HDA Link Voltage Support (Pin 7):

	1.5V	1.8V	1.5V/1.8V
AMD Carrizo			V
AMD Carrizo-L			V
Intel Broadwell		V	
Intel Braswell			V
Intel Skylake		V	
Intel Bay trail-M			V

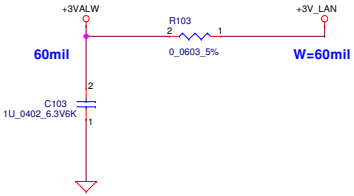


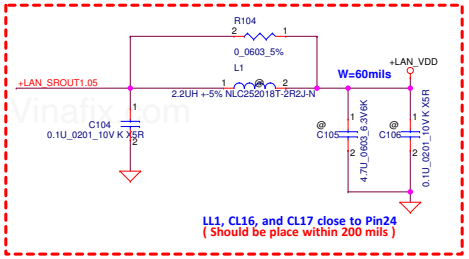


PC Beep



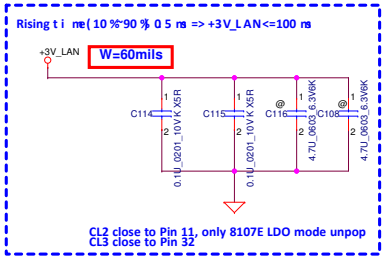
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/01	Deciphered Date 2015/09/01	Title: HD Audio Codec_ALC3240
			Size: Custom; Document Number: LA-D562P; Rev: 0.1
			Date: Thursday, June 15, 2017; Sheet 35 of 66

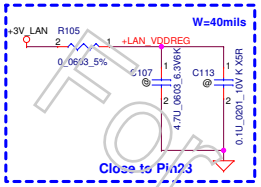


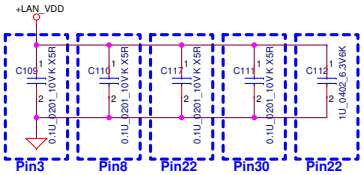


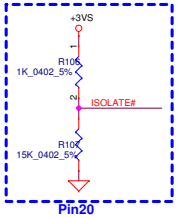
	1.0V Source	LL1	CL16,CL17	CL9,CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O

Please refer to the table above when using different 1.0V supply source.

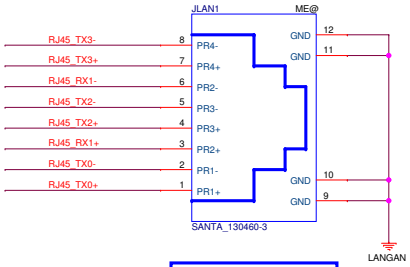




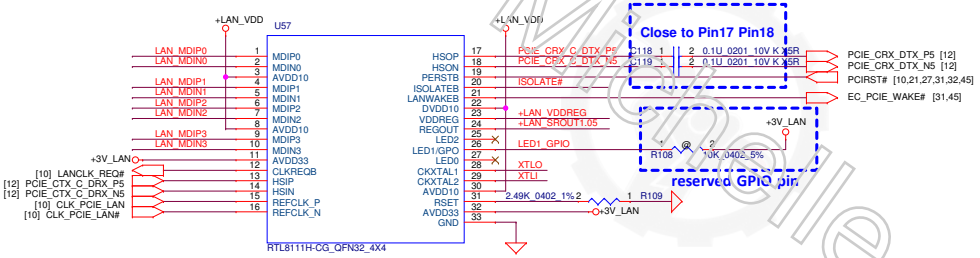


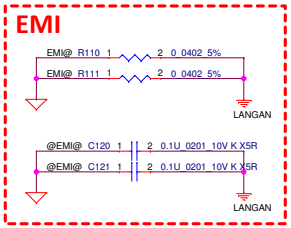


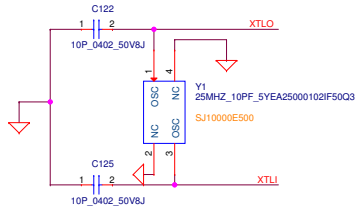
RJ-45 CONN.

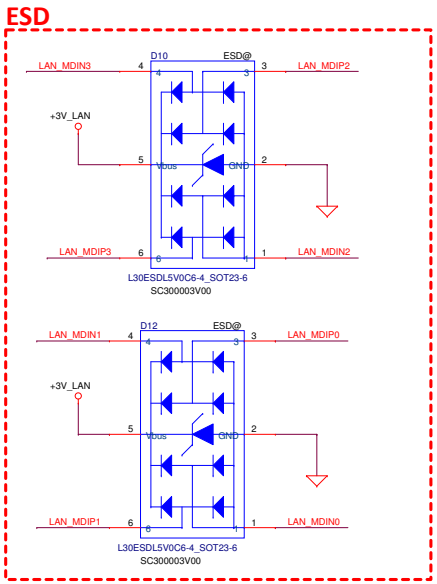


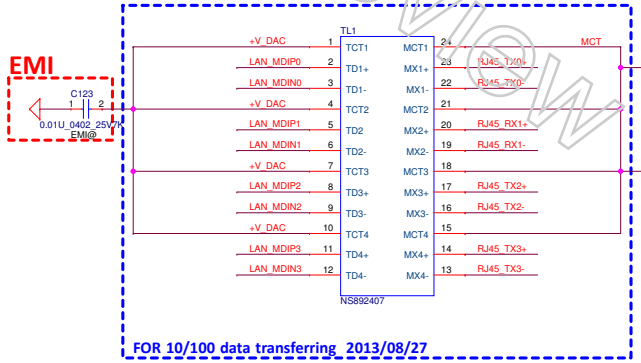
LAN Connector PN DC23400DP00

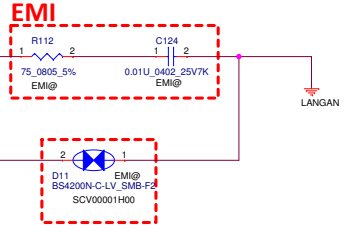












Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

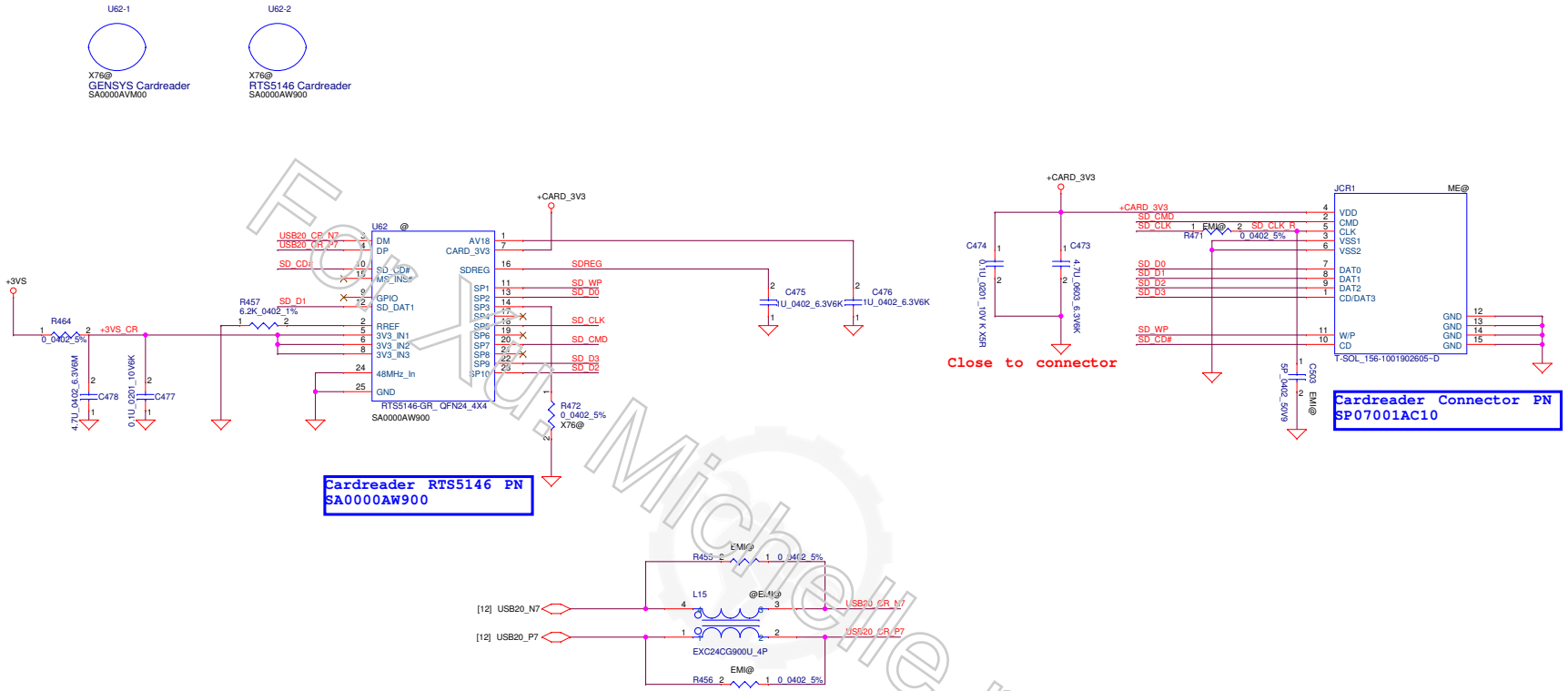
Compal Electronics, Inc.

Title: LAN_RTL8111H / RTL8107E

Size	Document Number	Rev
C	LA-D061P	0.3

Date: Thursday, June 15, 2017 Sheet 36 of 66

Card Reader



0329 move

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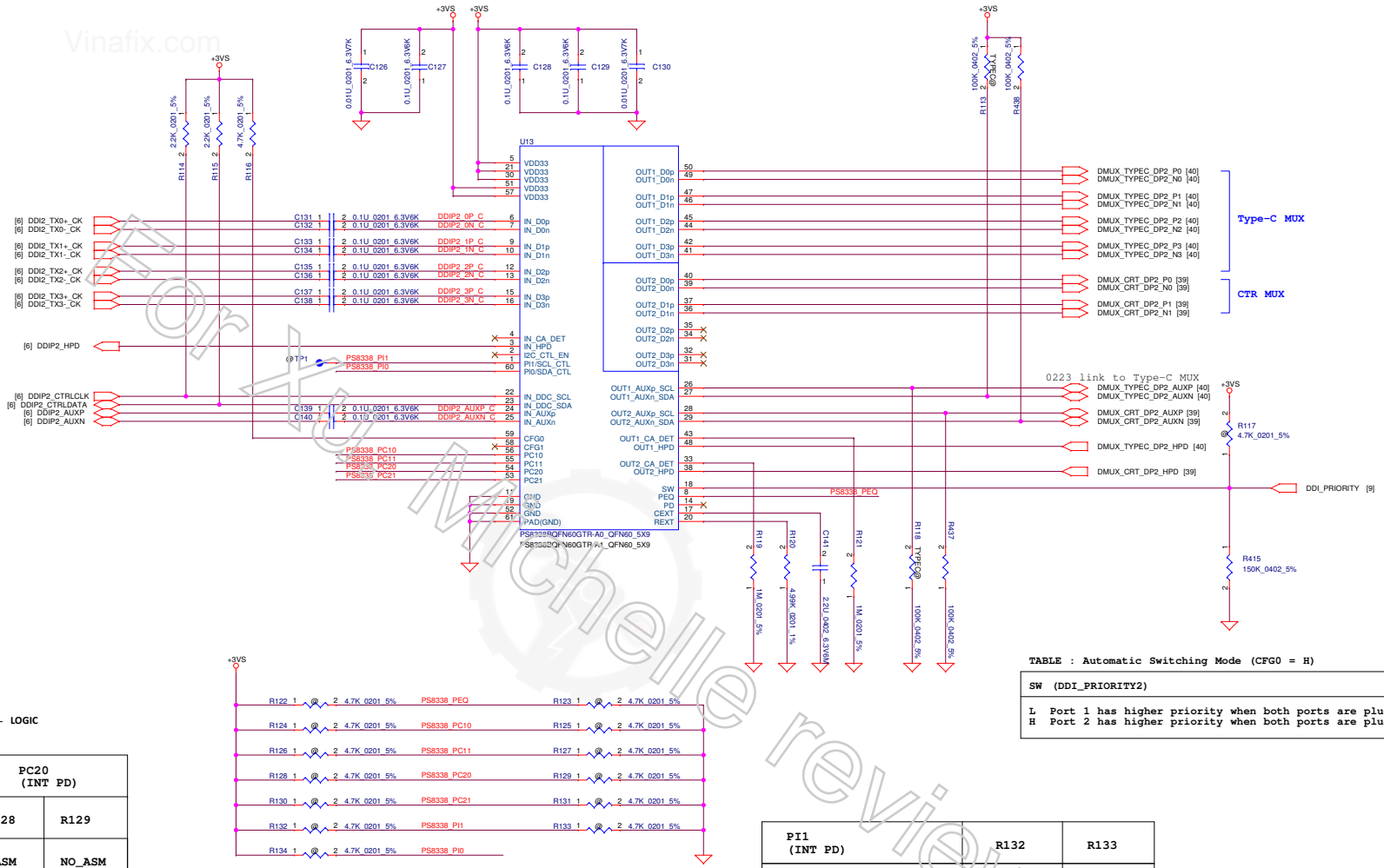
Size	Document Number		Rev
Custom	<Doc>		<RevCode>
Date:	Thursday, June 15, 2017	Sheet 37 of 66	



PEQ (INT PD)	R122	R123
HEQ 14.5dB	ASM	NO_ASM
LLEQ 8.5dB	ASM	ASM
LEQ 11.5dB	NO_ASM	NO_ASM

← LOGIC

	PC10 (INT PD)		PC20 (INT PD)	
	R124	R125	R128	R129
AUX interception DIS Output 800mV & 0dB	ASM	NO_ASM	ASM	NO_ASM
AUX interception DIS Output 400mV & 0dB	ASM	ASM	ASM	ASM
AUX interception EN	NO_ASM	NO_ASM	NO_ASM	NO_ASM

← LOGIC

	PC11 (INT PD)		PC21 (INT PD)	
	R126	R127	R130	R131
Swing +20%	ASM	NO_ASM	ASM	NO_ASM
Swing -16.7%	ASM	ASM	ASM	ASM
Swing default	NO_ASM	NO_ASM	NO_ASM	NO_ASM

← LOGIC

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY2)
L Port 1 has higher priority when both ports are plugged H Port 2 has higher priority when both ports are plugged

PI1 (INT PD)	R132	R133
Auto test EN & Offset cancellation EN	ASM	NO_ASM
Auto test DIS & Offset cancellation DIS	ASM	ASM
Auto test DIS & Offset cancellation EN	NO_ASM	NO_ASM

← LOGIC

PI0 (INT PD)	R134
Auto EQ DIS	ASM
Auto EQ EN	NO_ASM

← LOGIC

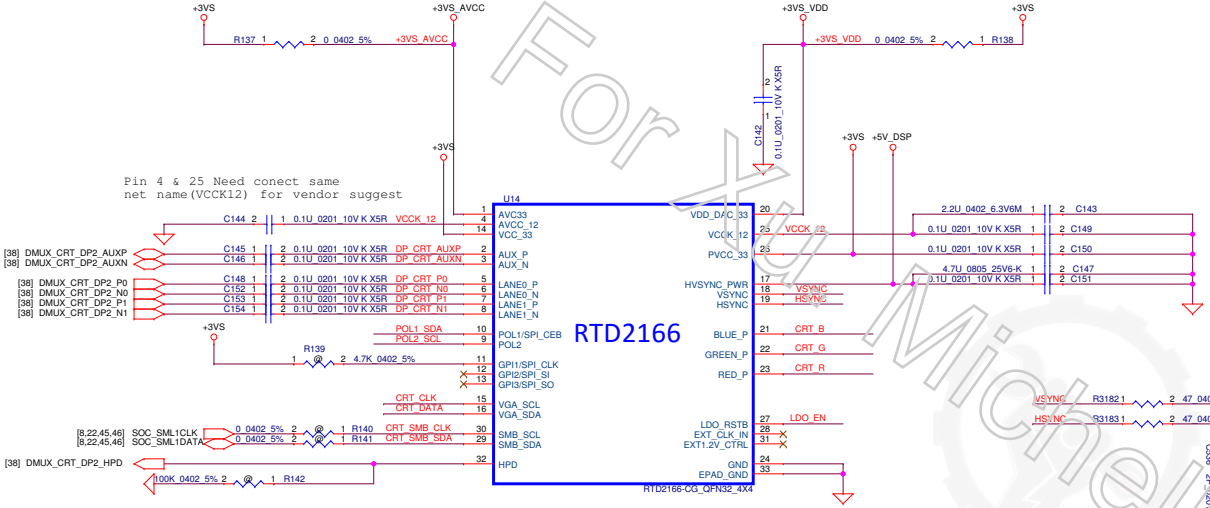
Security Classification	Compal Secret Data		
Issued Date	2014/11/04	Deciphered Date	2016/12/31

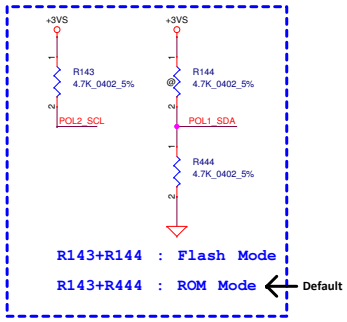
Compal Electronics, Inc.

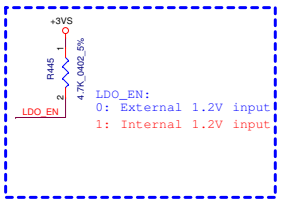
Title: DDI DEMULTIPLEXER

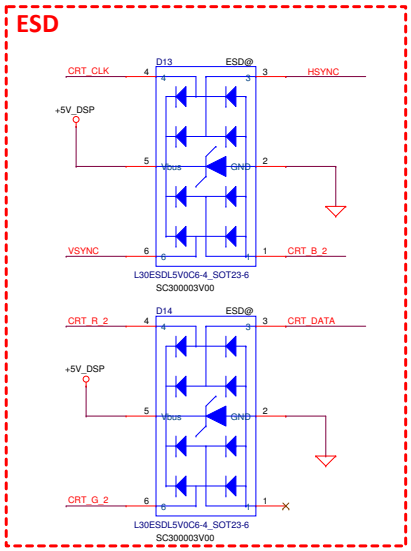
Size	Document Number	Rev
Custom	LA-C581P	0.5

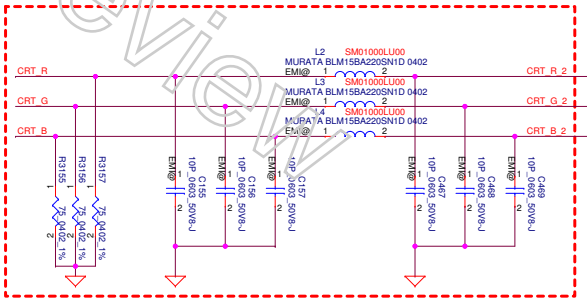
Date: Thursday, June 15, 2017 Sheet 38 of 66

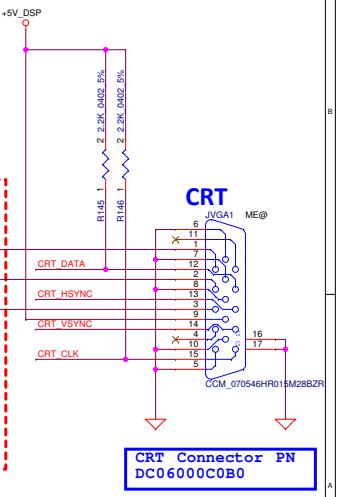












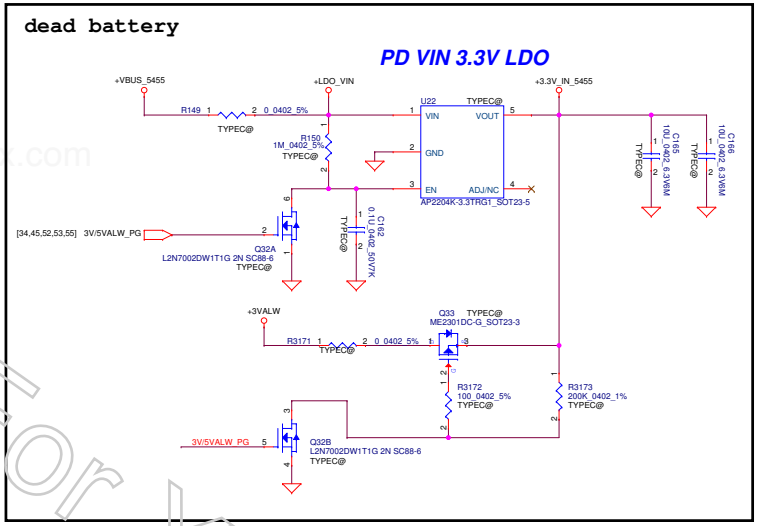
Security Classification	Compal Secret Data		
Issued Date	2014/08/16	Deciphered Date	2015/08/16

Compal Electronics, Inc.

Title: DP to VGA - RTD2168

Size	Document Number	Rev
Custom	LA-D061P	0.3

Date: Thursday, June 15, 2017 | Sheet 39 of 66



Close to Pin10

+5VALW R147 0_0603_5% +VCON_IN_5455
C158 10U_0402_6.3V6M
C217 10U_0402_6.3V6M
Q1 LP2301ALT1G_SOT23-3
GPIO9
R219 47K_0603_1%
R220 0_0402_5%

Support 3.3V IN version

+LDO_3V3_5455 R156 0_0402_5%
+3.3V_IN_5455
C167 4.7U_0603_6.3V6K
+VCON_IN_1_5455

SYMBOL
PD+MUX

Realtek RTS5455

U16
VCON_IN
5V_IN
LDO_3V3
SSRX_1P/2N
SSRX_1N/2P
SSTX_1P/2N
SSTX_1N/2P
DP0_1P/2N
DP0_1N/2P
DP1_1P/2N
DP1_1N/2P
DP2_1P/2N
DP2_1N/2P
DP3_1P/2N
DP3_1N/2P
10Gps 3:2 MUX
AUX_P/MGPIO4
AUX_N/MGPIO5
Low Speed MUX
H_DP/DCI_DATA/MGPIO2
H_DM/DCI_CLK/MGPIO3
BC1.2 Switch
SM_SDA/GPIO6
SM_SCL/GPIO5
SM_INT/GPIO4
REXT
E-PAD
RTS5455-GR_QFN46_6P5X4P5

From USB3.1
[12] USB3_RX_P4
[12] USB3_RX_N4
[12] USB3_TX_P4
[12] USB3_TX_N4

From DP MUX
[38] DMUX_TYPEC_DP2_P0
[38] DMUX_TYPEC_DP2_N0
[38] DMUX_TYPEC_DP2_P1
[38] DMUX_TYPEC_DP2_N1
[38] DMUX_TYPEC_DP2_P2
[38] DMUX_TYPEC_DP2_N2
[38] DMUX_TYPEC_DP2_P3
[38] DMUX_TYPEC_DP2_N3

TO SOC
[38] DMUX_TYPEC_DP2_AUXP
[38] DMUX_TYPEC_DP2_AUXN
[38] DMUX_TYPEC_DP2_HPD
DMUX_TYPEC_DP2_HPD

R171 100K_0402_5%
[45] EC_SMB_DA2
[45] EC_SMB_CK2
[45] PD_INT
R164 6.2K_0402_1%

Dead battery function Cfig. pin.
Tie to GND to disable dead battery ' Rd' .
Floating to enable dead battery ' Rd'

DB_CFG R157 0_0402_5%
C168 220P_0402_25V8J
C169 220P_0402_25V8J
PD_CC1 [41]
PD_CC2 [41]

ISP Channel via CCs

C_TX2_1P/2N
C_TX2_1N/2P
C_RX2_1P/2N
C_RX2_1N/2P
C_TX1_1P/2N
C_TX1_1N/2P
C_RX1_1P/2N
C_RX1_1N/2P
0.22U_0402_16V7K
USB3_DP_MTX_C_DRX_P2 [41]
USB3_DP_MTX_C_DRX_N2 [41]
USB3_DP_MRX_DTX_P2 [41]
USB3_DP_MRX_DTX_N2 [41]
USB3_DP_MTX_C_DRX_P1 [41]
USB3_DP_MTX_C_DRX_N1 [41]
USB3_DP_MRX_DTX_P1 [41]
USB3_DP_MRX_DTX_N1 [41]

SBU1/MGPIO6
SBU2/MGPIO7
AUX_SBU1 [41]
AUX_SBU2 [41]

ISP Channel via USB Billboard

C_DP/BB_DP
C_DM/BB_DM
VBUS_DSCHG
SNK_PS_EN [50]
I2C_SCL/GPIO7
I2C_SDA/GPIO8
I2C_INT/GPIO9
I2C_EN/GPIO10
FRS_5455
GPIO9
VBUS_EN_5455
MGPIO8/ IMON
MGPIO9/ VMON
MGPIO10/ LOC_PWR_MON
OCP_DET_5455
VMON_5455
LOC_PWR_MON

R163 1M_0402_5%
R165 1M_0402_5%

+5VALW R245 47K_0402_5% R244 100K_0402_5%
C159 10U_0603_6.3V6M
C592 10U_0603_25V6M
+VBUS_5455
+3.3V_IN_5455
R3179 10K_0402_5%
OCP_DET_5455
U15 DPS1113FIA-13_QFN18_4X4
IN
OUT
EN
FRS
DISC1
DISC2
VREG
GND
DV/DT
IMON
FAULTB
SRC
VLIM
ILIM
VBUS_EN_5455
FRS_5455
VBUS_DSCHG
VLIM_1114
ILIM_1113
IMON_1113
OCP_DET_5455
R3176 100K_0402_5%
C593 0.1U_0402_50V7K
R3180 100K_0402_5%
C535 100P_0402_25V8K
C534 100P_0402_25V8K
R3177 27K_0402_5%
R3178 54.9K_0402_1%

VBUS Discharge

+VBUS_5455
R168 100_2010_1%
Q9 IRLML2030TRPBF_SOT23-3 SB000013300
VBUS_DSCHG
R173 100K_0402_5%

Close to USB typeC(JTYPEC2)

+VBUS_5455
R169 200K_0402_1%
VMON_5455
R172 10K_0402_1%

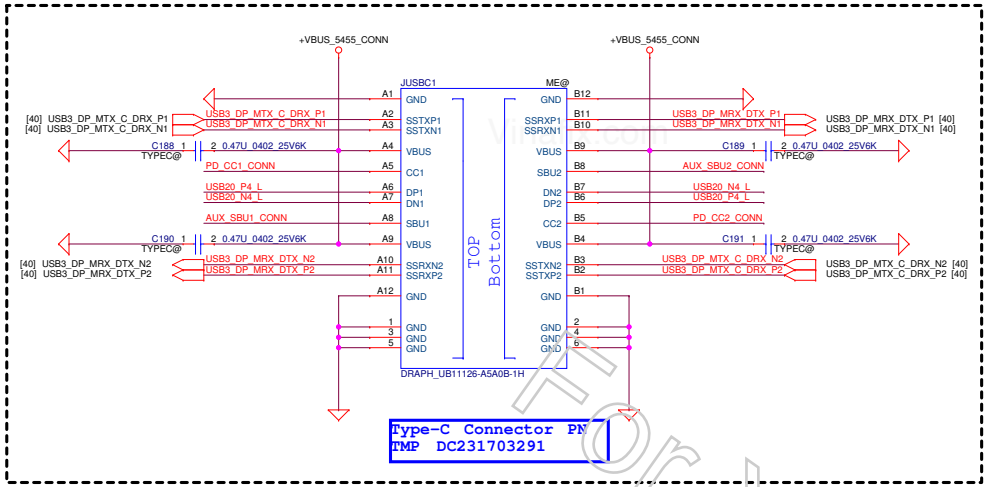
+1.DO_3V3_5455
+5VALW
R221 10K_0402_5%
R224 590K_0402_1% SD034590380
LOC_PWR_MON
R222 10K_0402_5%
R223 10K_0402_5%

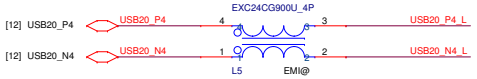
0314_Add
Connect 'LOC_PWR' net to local power for F/W to decide if C port can become provider via PR_SWAP. Leave floating if no local power exists in the system or in the application that 545x can only be powered on by local power.

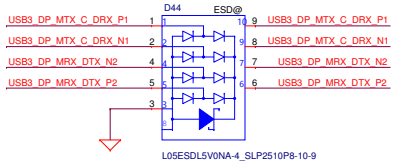
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

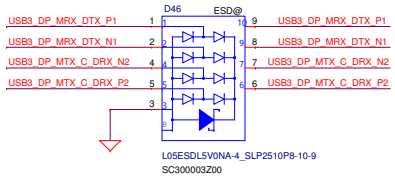
Security Classification	Compal Secret Data	
Issued Date	2014/05/19	Deciphered Date 2015/12/31

Compal Electronics, Inc.
Title: Type-C RTS5455
Size: Custom | Document Number: LA-E521P | Rev: 0.1
Date: Thursday, June 15, 2017 | Sheet 40 of 63

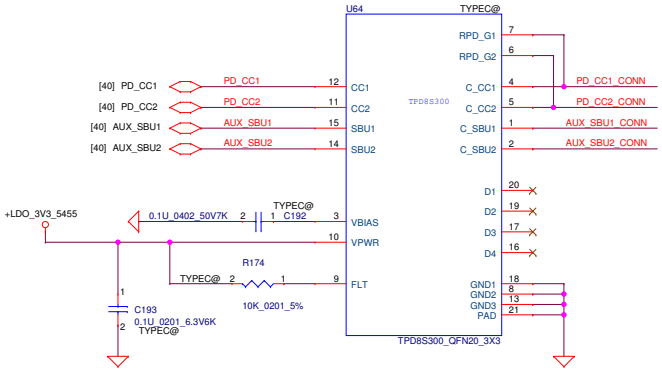


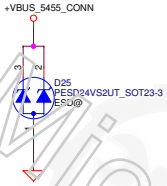


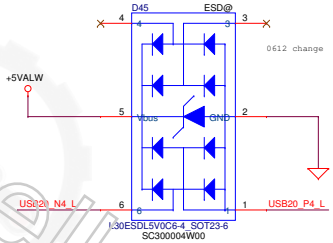


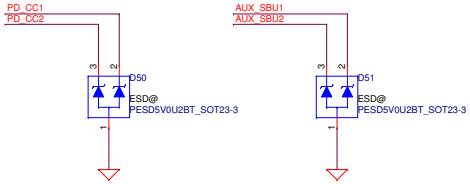


ESD for USBC1 Lines and Control lines







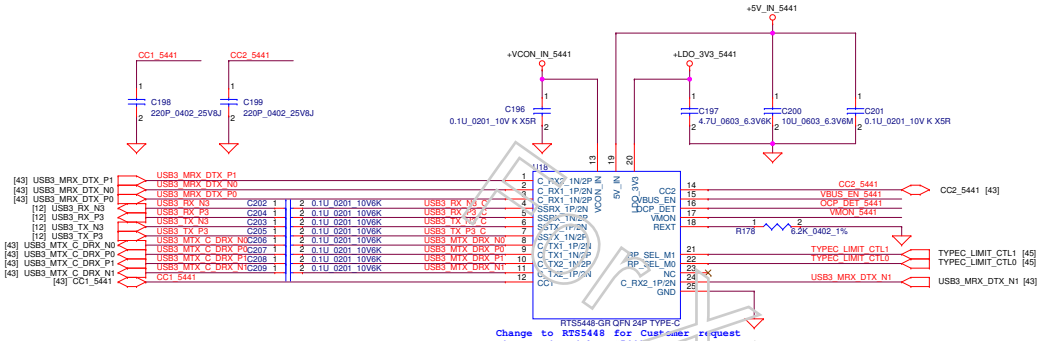


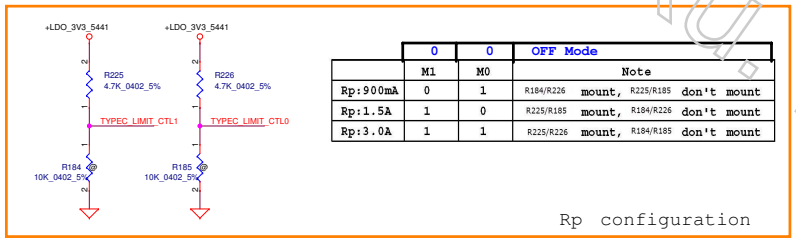
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title: *Type-C_RTS5455_CONN*

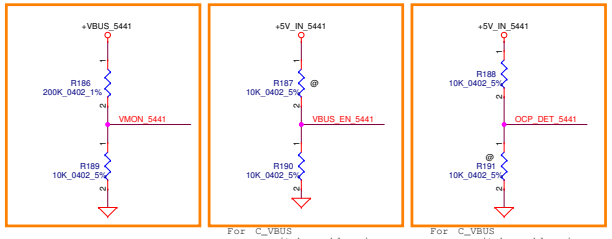
Size	Document Number	Rev
C		0.1

Date: Thursday, June 15, 2017 | Sheet 41 of 63





0	0	OFF Mode	
	M1	M0	Note
Rp:900mA	0	1	R184/R226 mount, R225/R185 don't mount
Rp:1.5A	1	0	R225/R185 mount, R184/R226 don't mount
Rp:3.0A	1	1	R225/R226 mount, R184/R185 don't mount



Power switch enable pin	Note
Low Active	R190/R187 mount
High Active	R190 mount,R187 don't mount

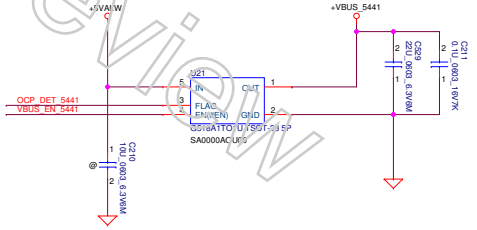
Pull Up & Down

Pull Down

Power switch OCP pin	Note
Low Active	R191/R188 mount
High Active	R191 mount,R188 don't mount

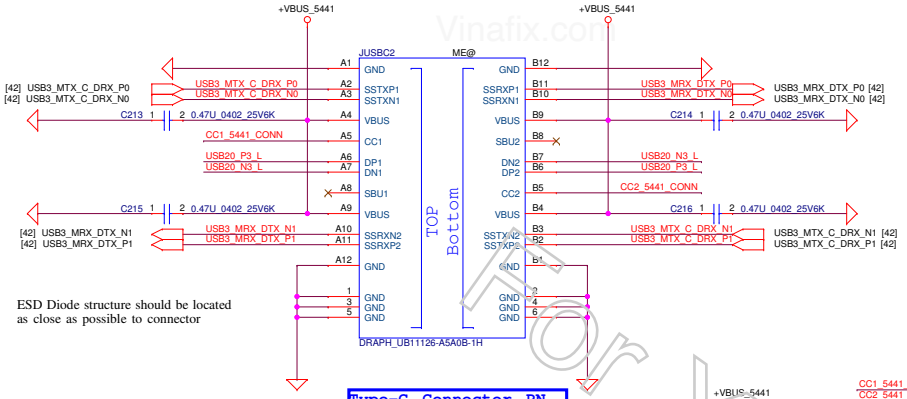
Pull Up & Down

Pull Down



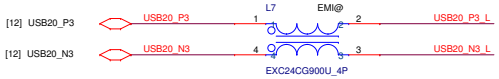
Security Classification	Compal Secret Data		
Issued Date	2014/11/04	Deciphered Date	2016/12/31

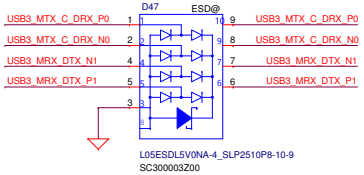
Compal Electronics, Inc.	
Title	Type-C RTS5441
Size: Custom	Document Number: LA-C581P
Rev	0.5
Date: Thursday, June 15, 2017	Sheet 42 of 63

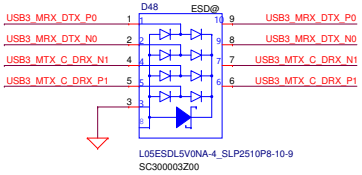


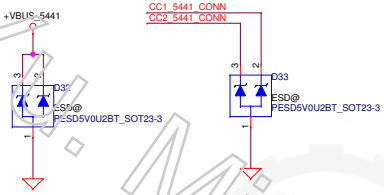
ESD Diode structure should be located as close as possible to connector

Type-C Connector PN TMP DC231703291

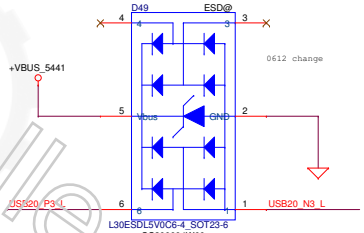


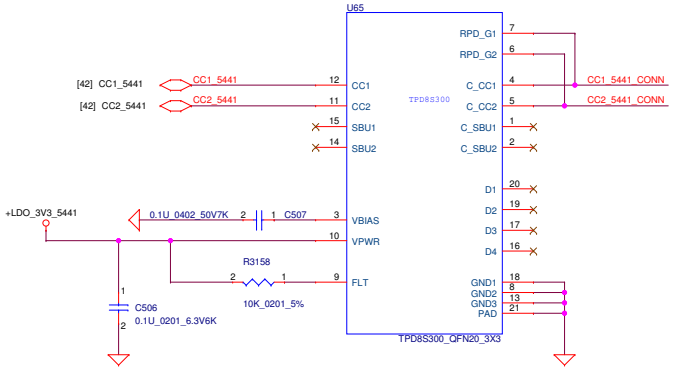






ESD for USBC2 Lines and Control lines





0614 add
CC1_5441 R3196 1 @ESD@2 0_0201_5% CC1_5441_CONN
CC2_5441 R3197 1 @ESD@2 0_0201_5% CC2_5441_CONN

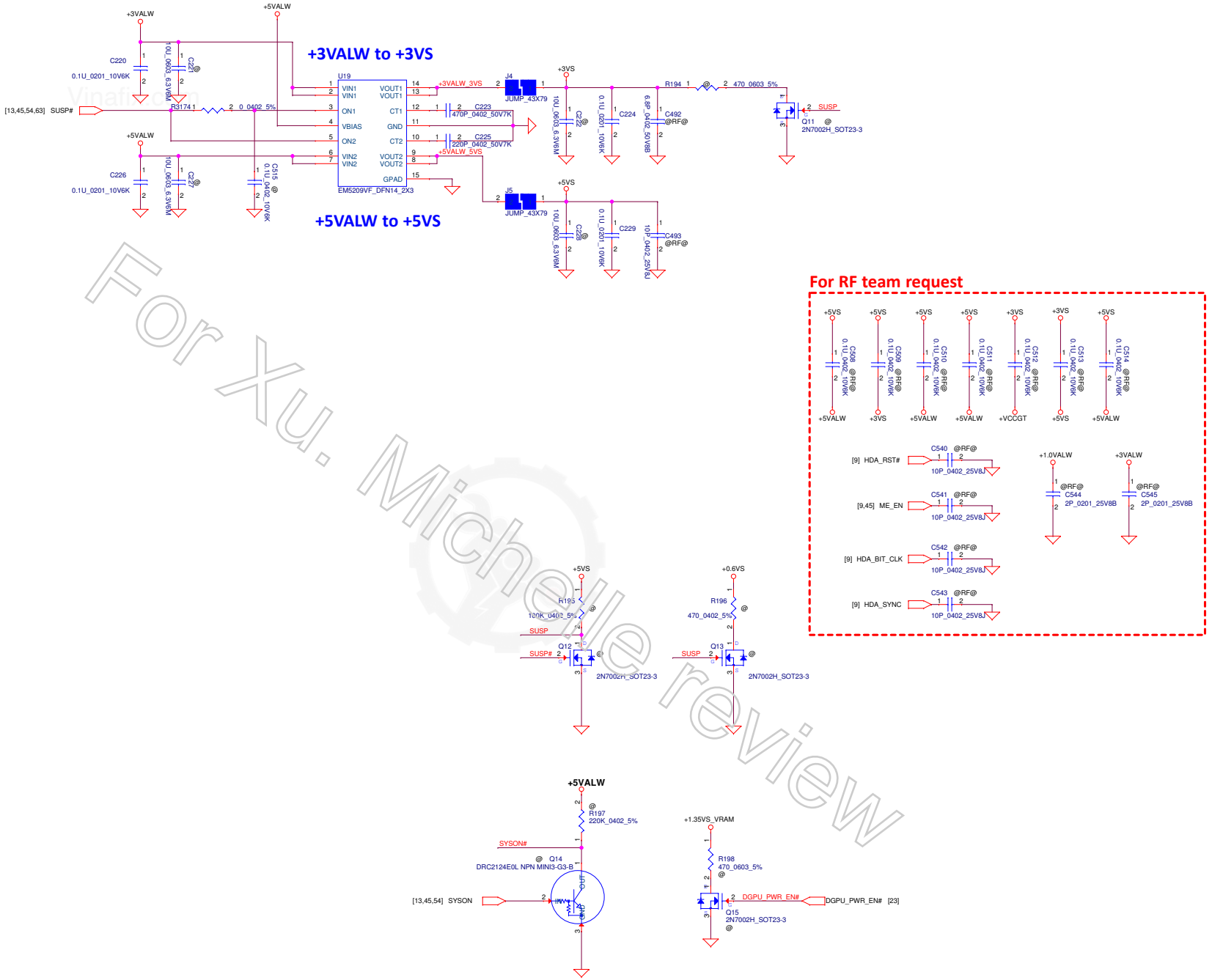
Security Classification	Compal Secret Data		
Issued Date	2014/11/04	Deciphered Date	2016/12/31

Compal Electronics, Inc.

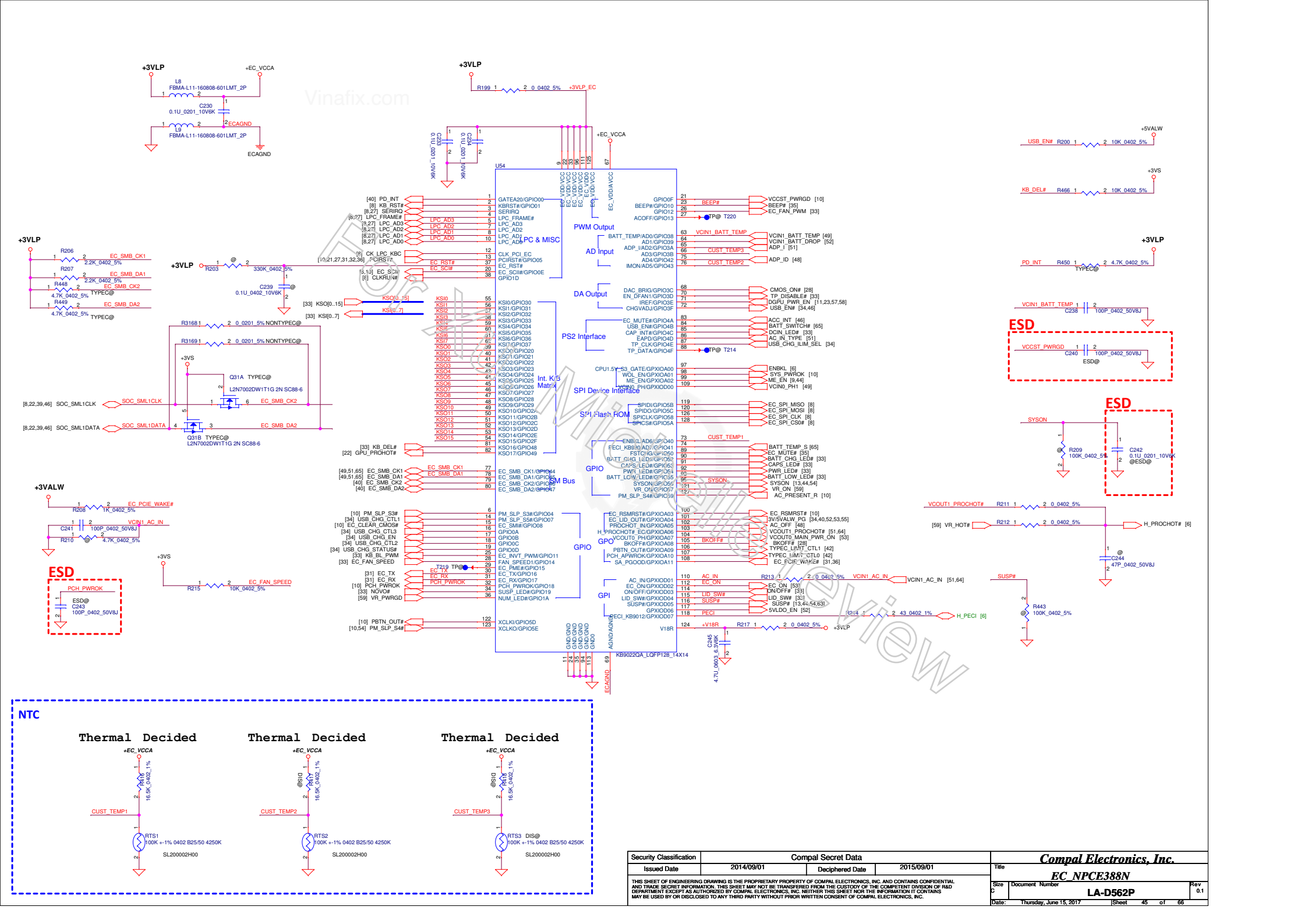
Title: Type-C RTS5441 CONN

Size	Document Number	Rev
C	LA-C581P	0.5

Date: Thursday, June 15, 2017 Sheet 43 of 63



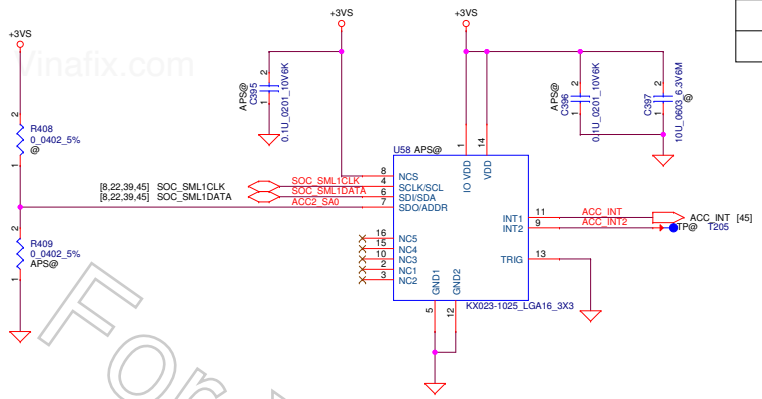
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: DC Interface
			Size C / Document Number LA-D562P / Rev 0.1
			Date: Thursday, June 15, 2017 / Sheet 44 of 66


+3VLP
+EC_VCCA
L8
FBMA-L11-160808-601LMT_2P
C230
0.1U_0201_10V6K
L9
FBMA-L11-160808-601LMT_2P
ECAGND
R199 0 0402 5% +3VLP_EC
U54
KB9022QA_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
+3VALW
+3VS
+5VALW
ESD
NTC
Thermal Decided
RTS1 100K +-1% 0402 B25/50 4250K
RTS2 100K +-1% 0402 B25/50 4250K
RTS3 DIS@ 100K +-1% 0402 B25/50 4250K
SL200002H00
Security Classification
Compal Secret Data
Issued Date
2014/09/01
Deciphered Date
2015/09/01
Compal Electronics, Inc.
EC_NPCE388N
LA-D562P
Rev 0.1
Thursday, June 15, 2017
Sheet 45 of 66

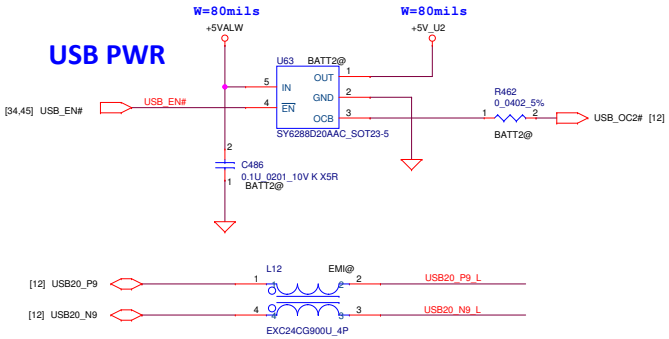
APS G-Sensor

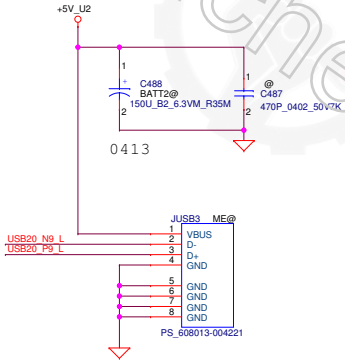
Kionix KX023-1025

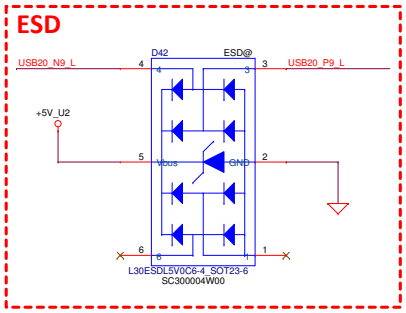
SDO/ADDR	Address R/W
VDD	3Fh/3Eh
VSS	3Dh/3Ch



2nd Battery USB2_CONN

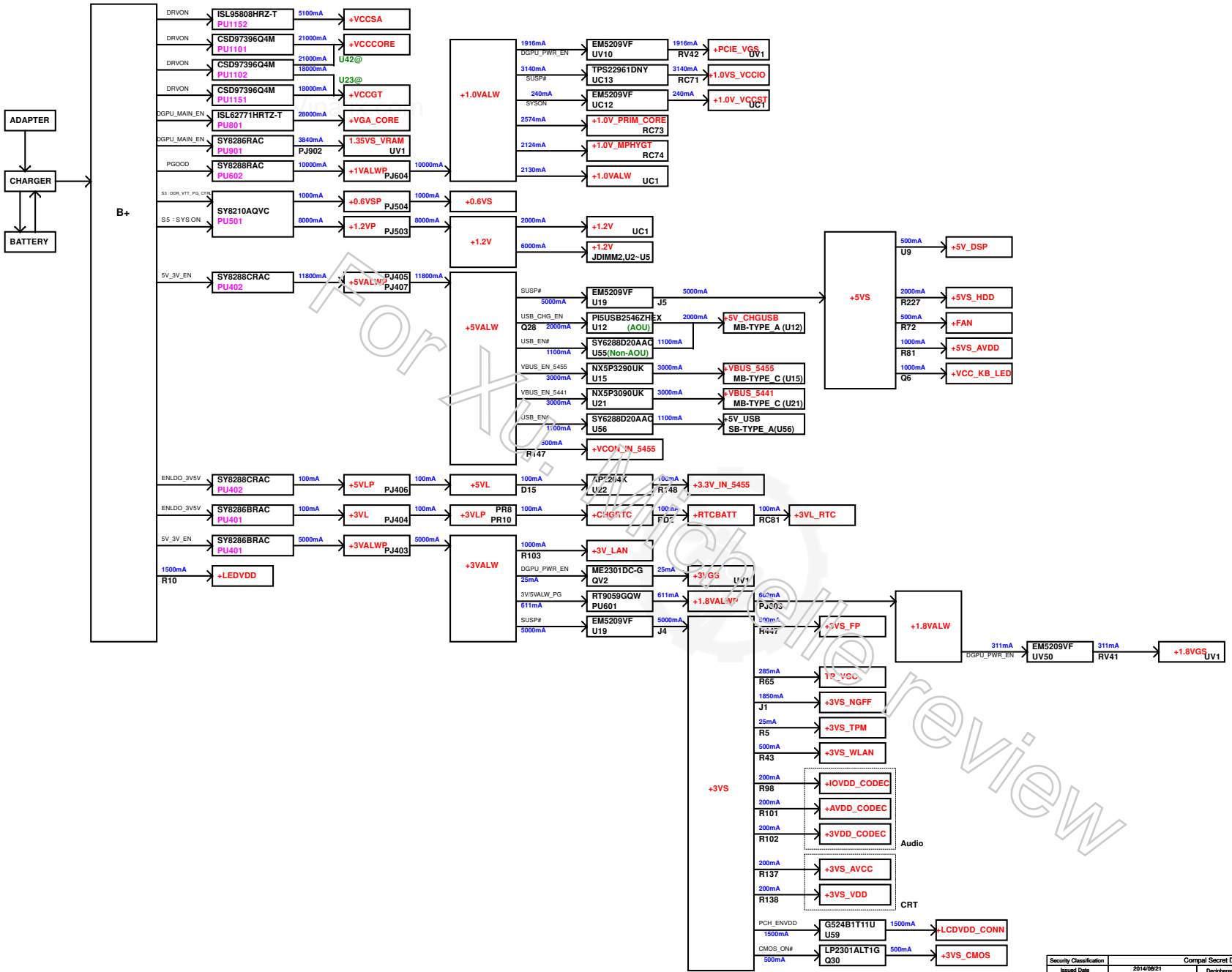




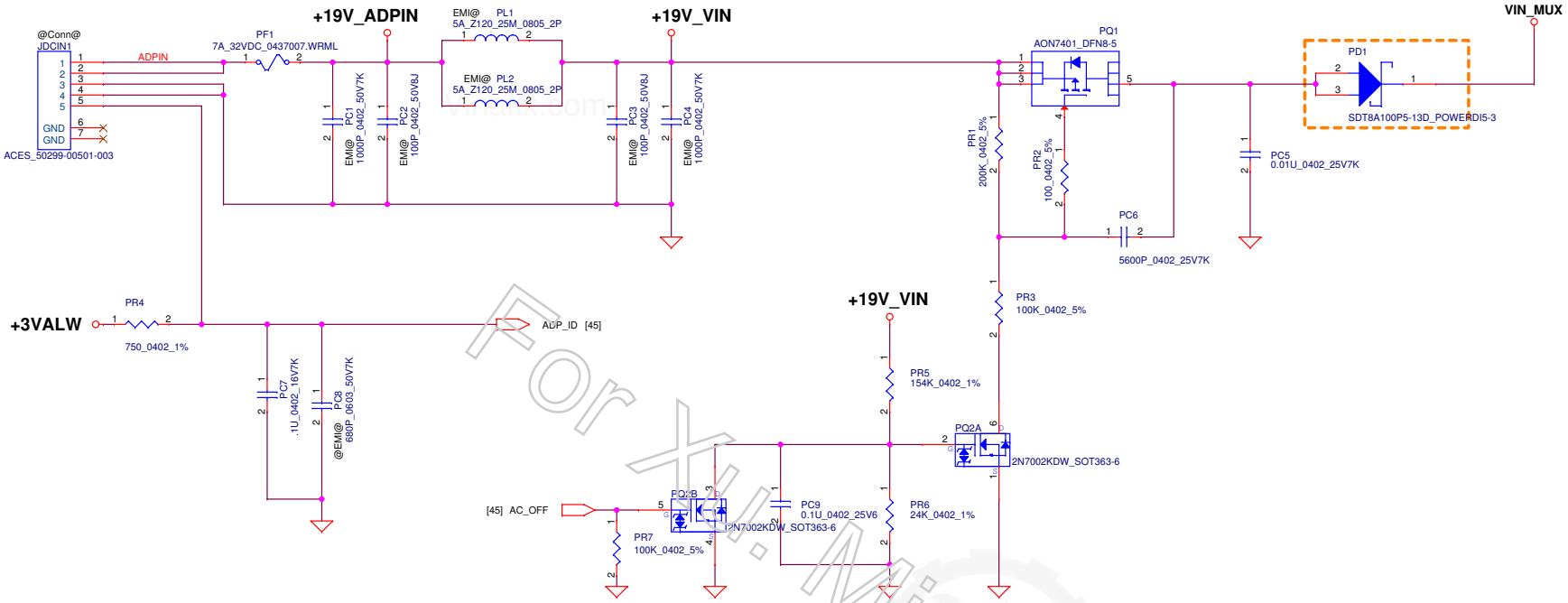


USB2.0 Connector PN DC23300H300

Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Thursday, June 15, 2017	Sheet 46 of 66	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/08/21	Deciphered Date	2015/08/21
Title	Power Rail		
Size	Document Number		Rev
D	LA-D561P		0.1
Date:	Thursday, June 15, 2017	Sheet	47 of 65



BOM Structure Table

Item	BOM Structure
For U22	U22@
For U23e	U23@
For U42	U42@
For DIS	VGA@
Support Type-C PD	PD@
For EMI	EMI@
For DIS of EMI	VGA_EMI@
For U23e of EMI	U23_EMI@
For U42 of EMI	U42_EMI@
For RF	RF@
For DIS of RF	VGA_RF@
For U23e of RF	U23_RF@
For U42 of RF	U42_RF@

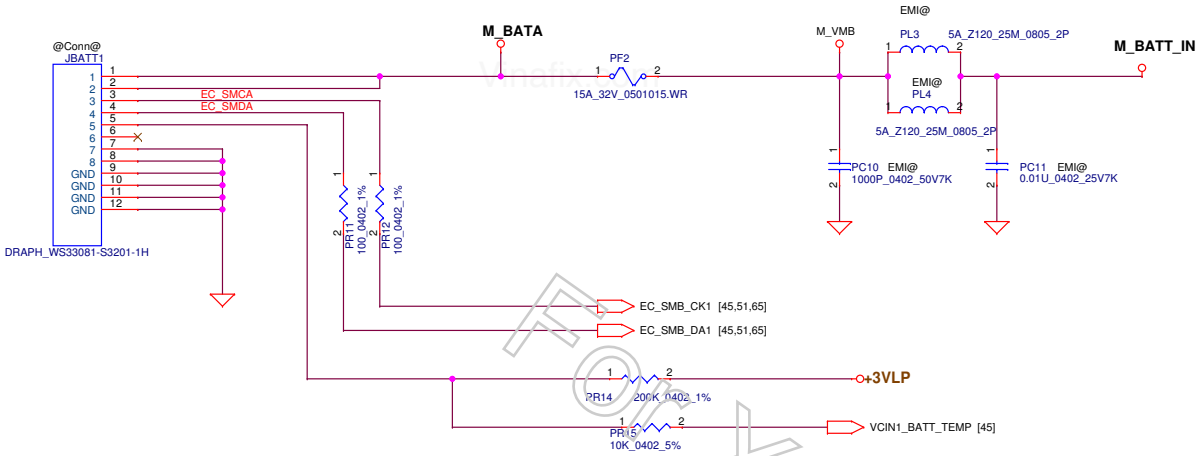
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

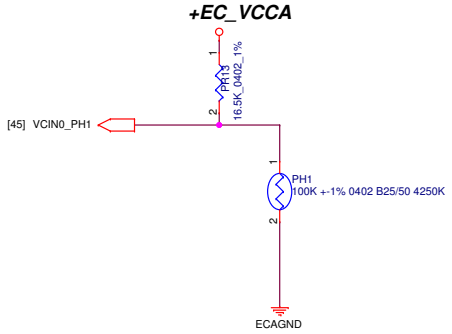
Title: **PWR-DCIN / Vin Detector**

Size	Document Number	Rev
Custom	VE	0.1

Date: Thursday, June 15, 2017 | Sheet 48 of 66



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



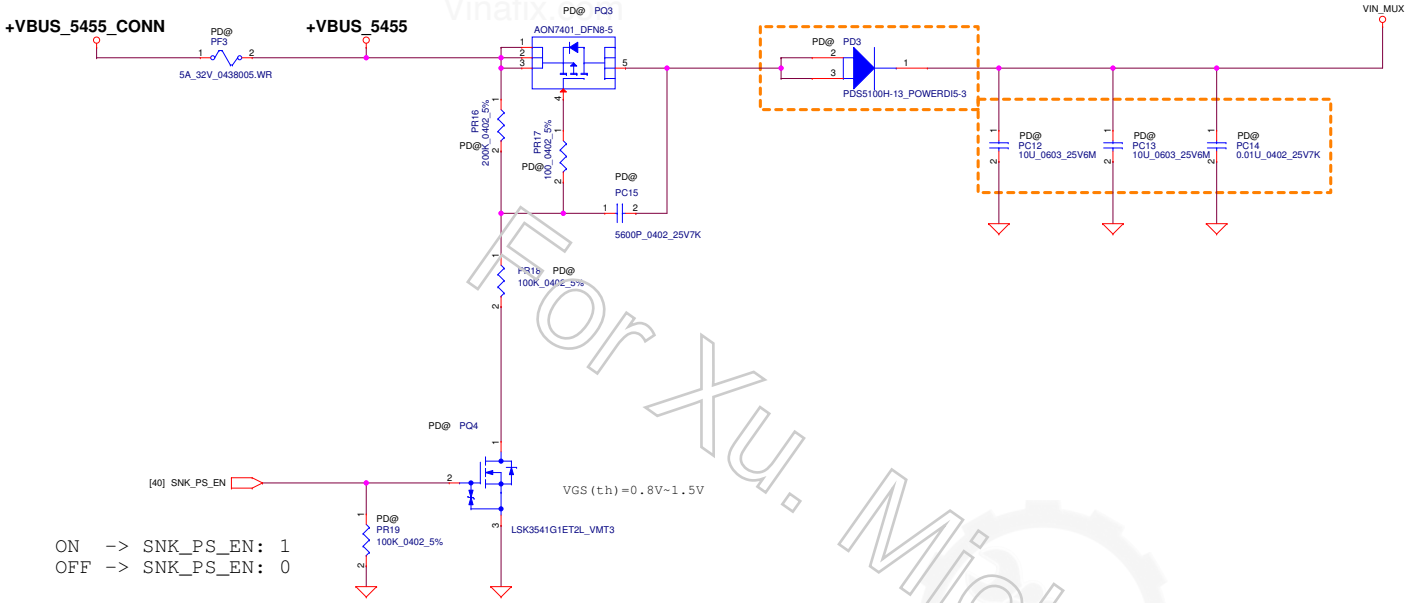
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	VE	0.1

Date: Thursday, June 15, 2017 | Sheet 49 of 66



ON -> SNK_PS_EN: 1
OFF -> SNK_PS_EN: 0

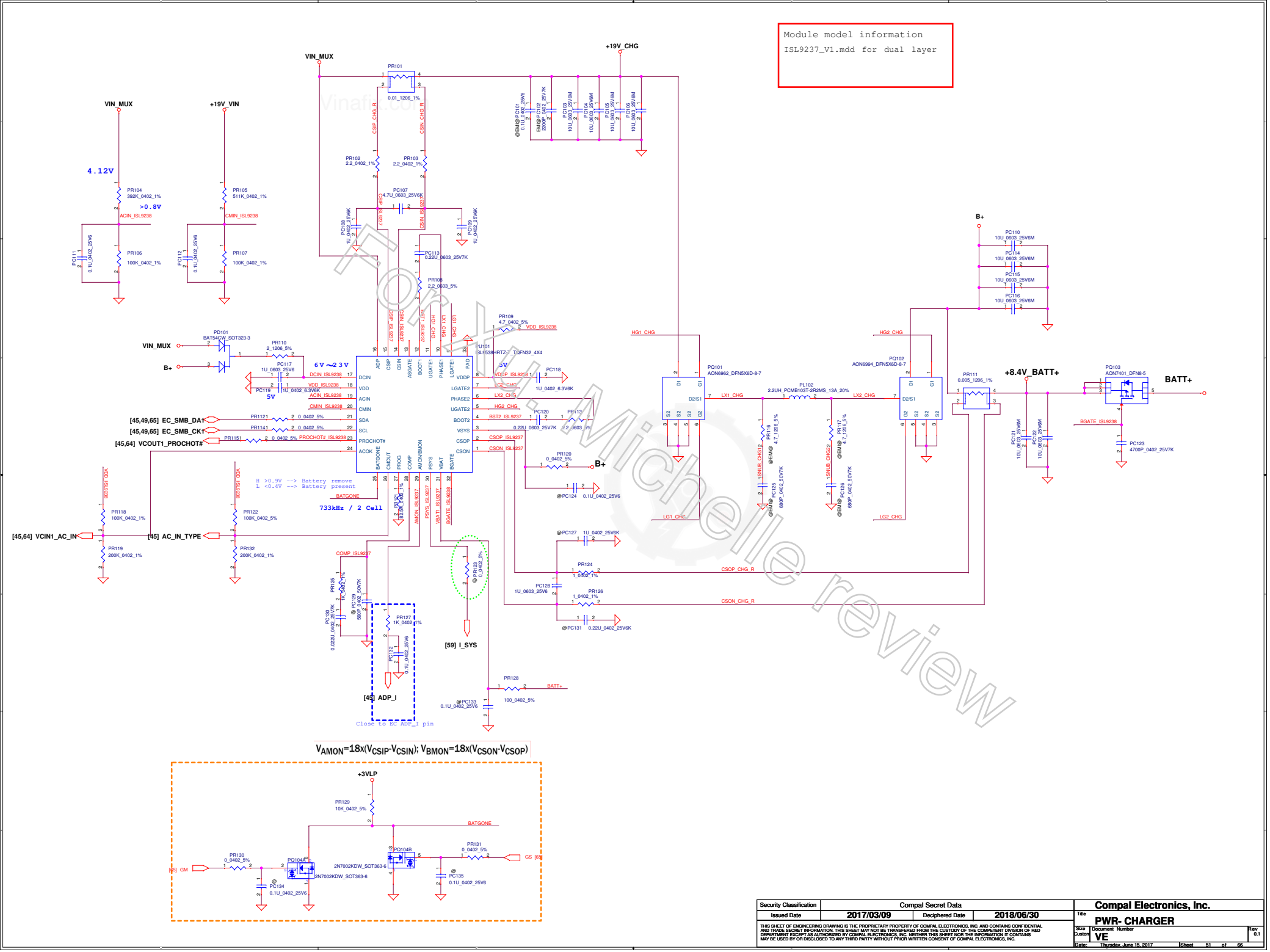
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- TYPE-C**

Size	Document Number	Rev
C	VE	0.1

Date: Thursday, June 15, 2017 | Sheet 50 of 66


Module model information
ISL9237_V1.mdd for dual layer
VIN_MUX
+19V_CHG
+19V_VIN
4.12V
>0.8V
ACIN_ISL9238
CMIN_ISL9238
PR101
0.01_1206_1%
PR102 2.2_0402_1%
PR103 2.2_0402_1%
PC107 4.7U_0603_25V6K
PC108 1U_0402_25V6K
PC109 1U_0402_25V6K
PC113 0.22U_0603_25V7K
PR108 2.2_0603_5%
PR104 392K_0402_1%
PR105 511K_0402_1%
PR106 100K_0402_1%
PR107 100K_0402_1%
PC111 0.1U_0402_25V6
PC112 0.1U_0402_25V6
PD101 BAT54CW_SOT323-3
PR110 2_1206_5%
PC117 1U_0603_25V6
PC119 1U_0402_6.3V6K
6V~23V
5V
PR109 4.7_0402_5%
VDD_ISL9238
U1U101 ISL6536HRTZ-T_TQFN32_4X4
PC118 1U_0402_6.3V6K
PC120 0.22U_0603_25V7K
PR113 2.2_0603_5%
PR120 0_0402_5%
PC124 0.1U_0402_25V6
B+
[45,49,65] EC_SMB_DAT
[45,49,65] EC_SMB_CK1
[45,64] VCOUT1_PROCHOT#
PR1121 2_0_0402_5%
PR1141 2_0_0402_5%
PR1151 2_0_0402_5%
PROCHOT#_ISL9238
H >0.9V --> Battery remove
L <0.4V --> Battery present
BATGONE
733kHz / 2 Cell
[45,64] VCIN1_AC_IN
[45] AC_IN_TYPE
PR118 100K_0402_1%
PR119 200K_0402_1%
PR122 100K_0402_5%
PR132 200K_0402_1%
COMP_ISL9237
PR125 1K_0402_1%
PC129 560P_0402_50V7K
PC130 0.022U_0402_25V7K
PR127 1K_0402_1%
PC132 0.1U_0402_25V6
[45] ADP_I
Close to EC ADP_I pin
PR123 @ 0_0402_5%
[59] I_SYS
PR128 100_0402_5%
@PC133 0.1U_0402_25V6
@PC127 1U_0402_25V6K
PR124 1_0402_1%
PC128 1U_0603_25V6
PR126 1_0402_1%
@PC131 0.22U_0402_25V6K
CSOP_CHG_R
CSON_CHG_R
PQ101 AON6962_DFN5X6D-8-7
PQ102 AON6994_DFN5X6D-8-7
PL102 2.2UH_PCMB103T-2R2MS_13A_20%
LX1_CHG
LX2_CHG
HG1_CHG
HG2_CHG
LG1_CHG
LG2_CHG
PR116 @EM@ 4.7_1206_5%
PR117 @EM@ 4.7_1206_5%
PC125 @EM@ 680P_0402_50V7K
PC126 @EM@ 680P_0402_50V7K
PC110 10U_0603_25V6M
PC114 10U_0603_25V6M
PC115 10U_0603_25V6M
PC116 10U_0603_25V6M
PR111 0.005_1206_1%
+8.4V_BATT+
PC121 10U_0603_25V6M
PC122 10U_0603_25V6M
PQ103 AON7401_DFN8-5
BATT+
BGATE_ISL9238
PC123 4700P_0402_25V7K
$V_{AMON}=18x(V_{CSIP}-V_{CSIN})$; $V_{BMON}=18x(V_{CSON}-V_{CSOP})$
+3VLP
PR129 10K_0402_5%
PR130 0_0402_5%
PQ104A
2N7002KDW_SOT363-6
PQ104B
PR131 0_0402_5%
GS [65]
[65] GM
PC134 0.1U_0402_25V6
PC135 0.1U_0402_25V6
Security Classification
Compal Secret Data
Issued Date
2017/03/09
Deciphered Date
2018/06/30
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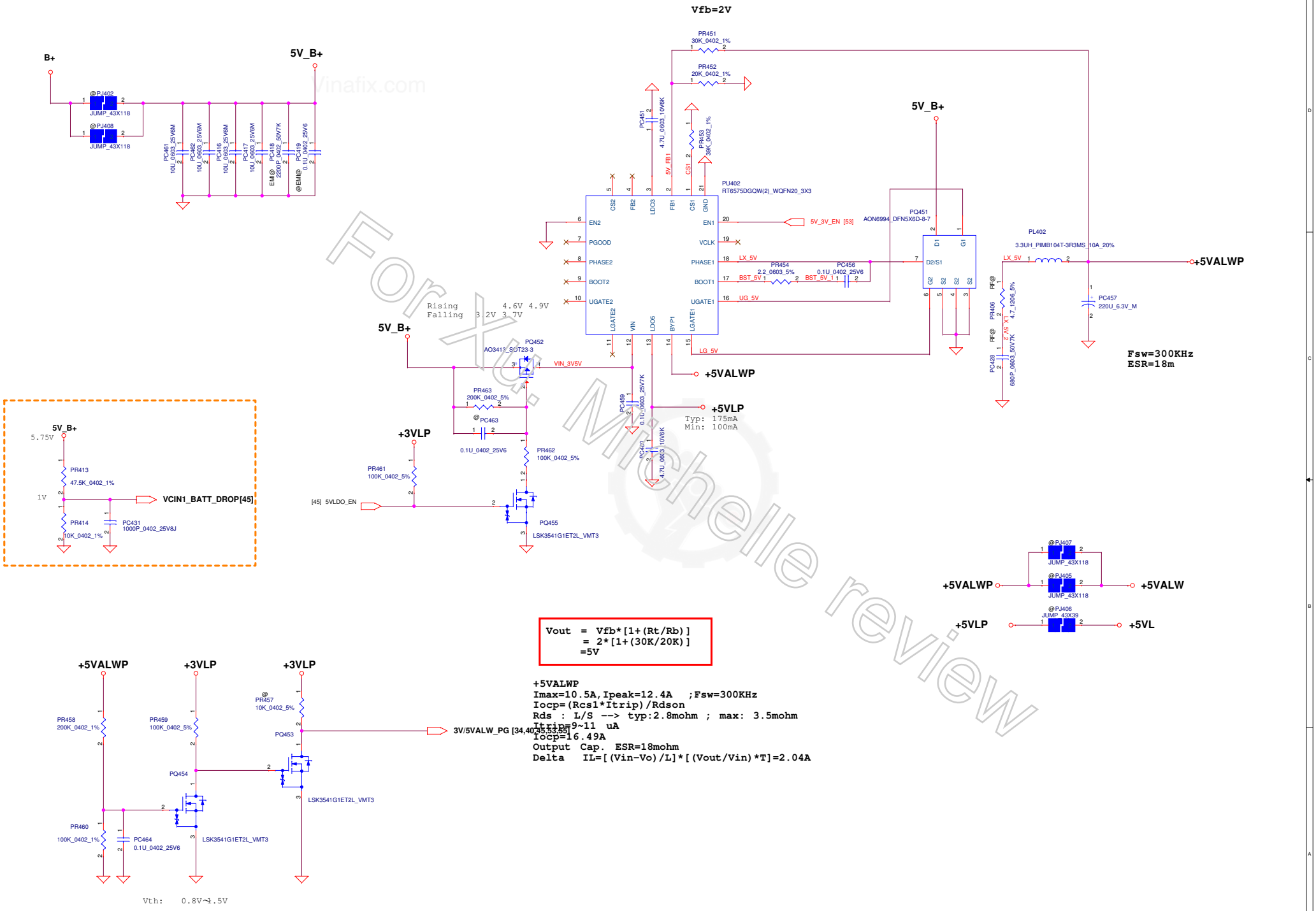
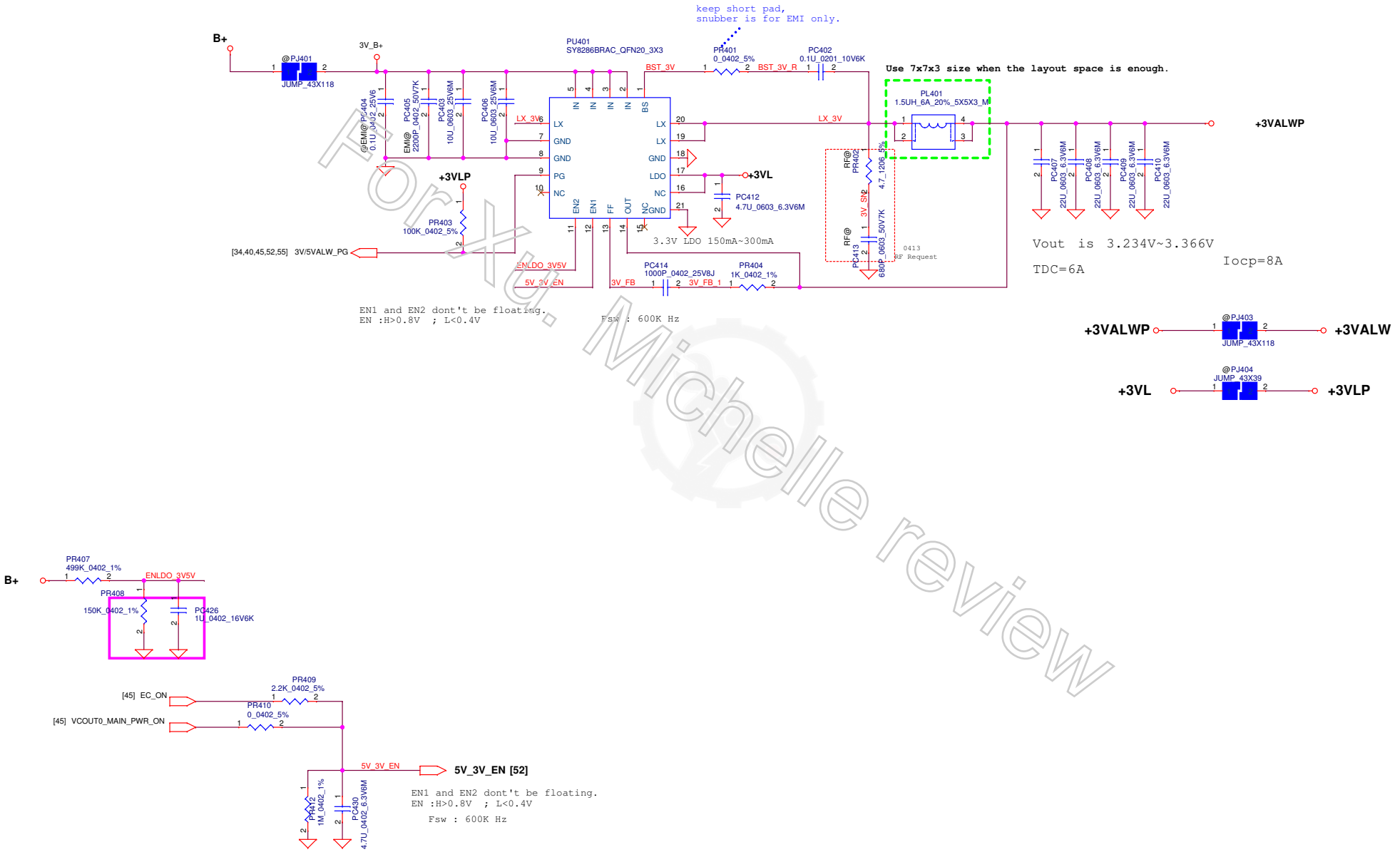
Compal Electronics, Inc.
Title
PWR- CHARGER
Size
Custom
Document Number
VE
Rev
0.1
Date:
Thursday, June 15, 2017
Sheet
51
of
66



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date	2018/06/30
Title	PWR- 5VALWP		
Size C	Document Number VE		Rev 0.1
Date: Thursday, June 15, 2017	Sheet 52 of 66		



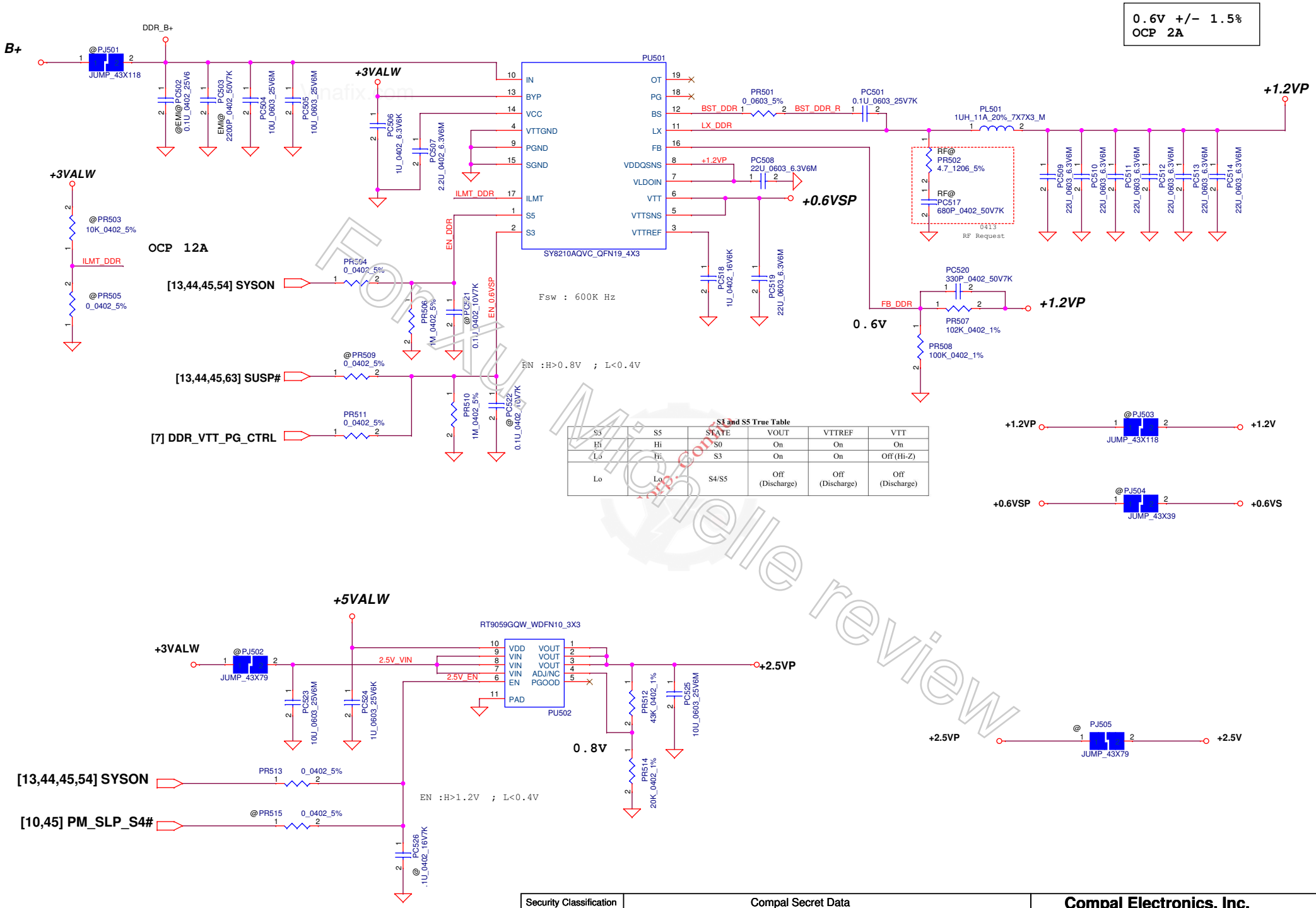
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- 3VALWP**

Size	Document Number	Rev
Custom	VE	0.1

Date: Thursday, June 15, 2017 | Sheet 53 of 66



S3 and S5 True Table

S5	S5	STATE	VOUT	VTTREF	VTT
Hi	Hi	S0	On	On	On
Lo	Hi	S3	On	On	Off (Hi-Z)
Lo	Lo	S4/S5	Off (Discharge)	Off (Discharge)	Off (Discharge)

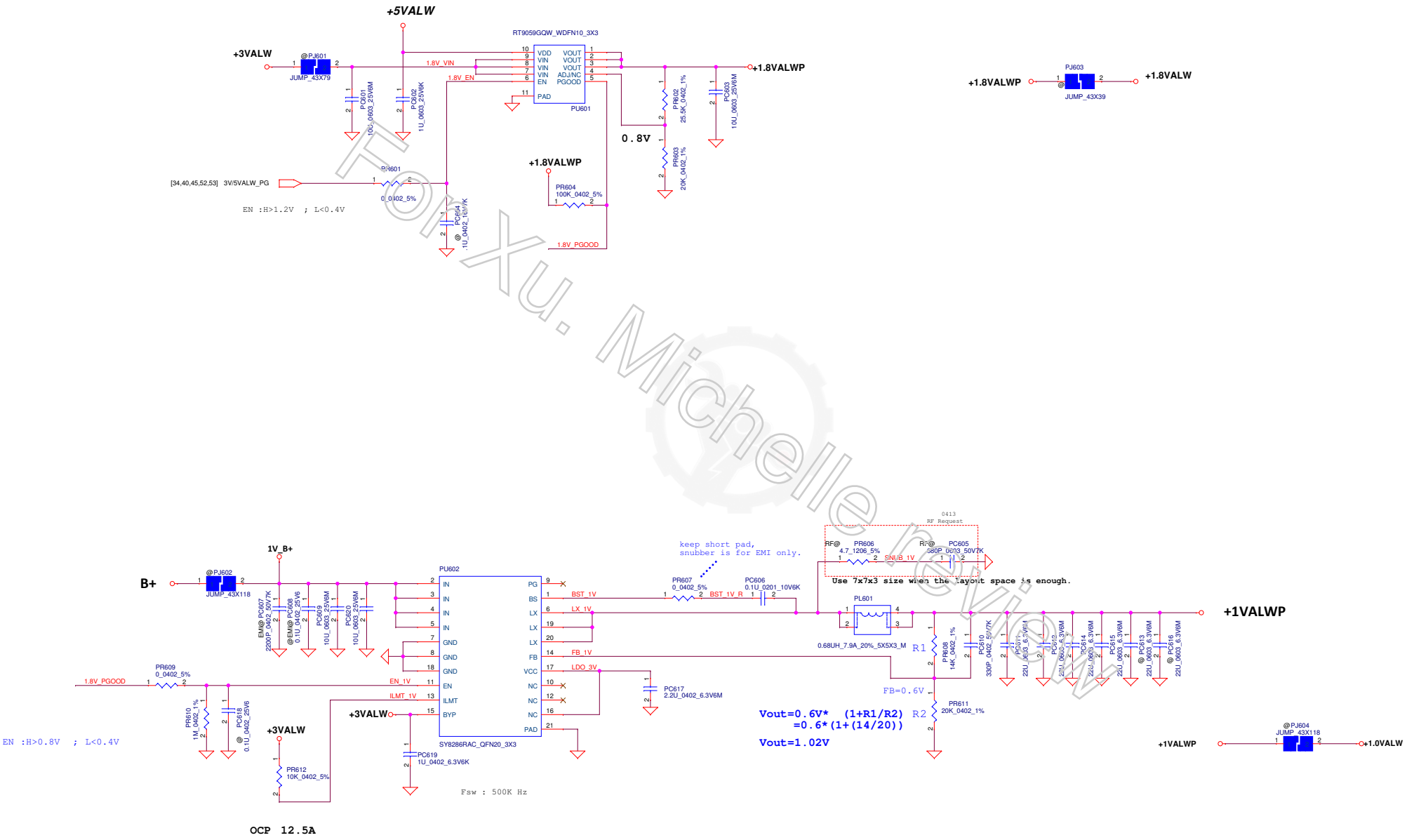
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- 1.2VP/0.6VSP/2.5VP**

Size	Document Number	Rev
Custom	VE	0.1

Date: Thursday, June 15, 2017 Sheet 54 of 66



Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.	
Title	PWR- 1.8VALWP/1VALWP
Size C	Document Number VE
Rev	0.1
Date: Thursday, June 15, 2017	Sheet 55 of 66

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Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title	BLANK	
Size: Custom	Document Number: VE	Rev: 0.1
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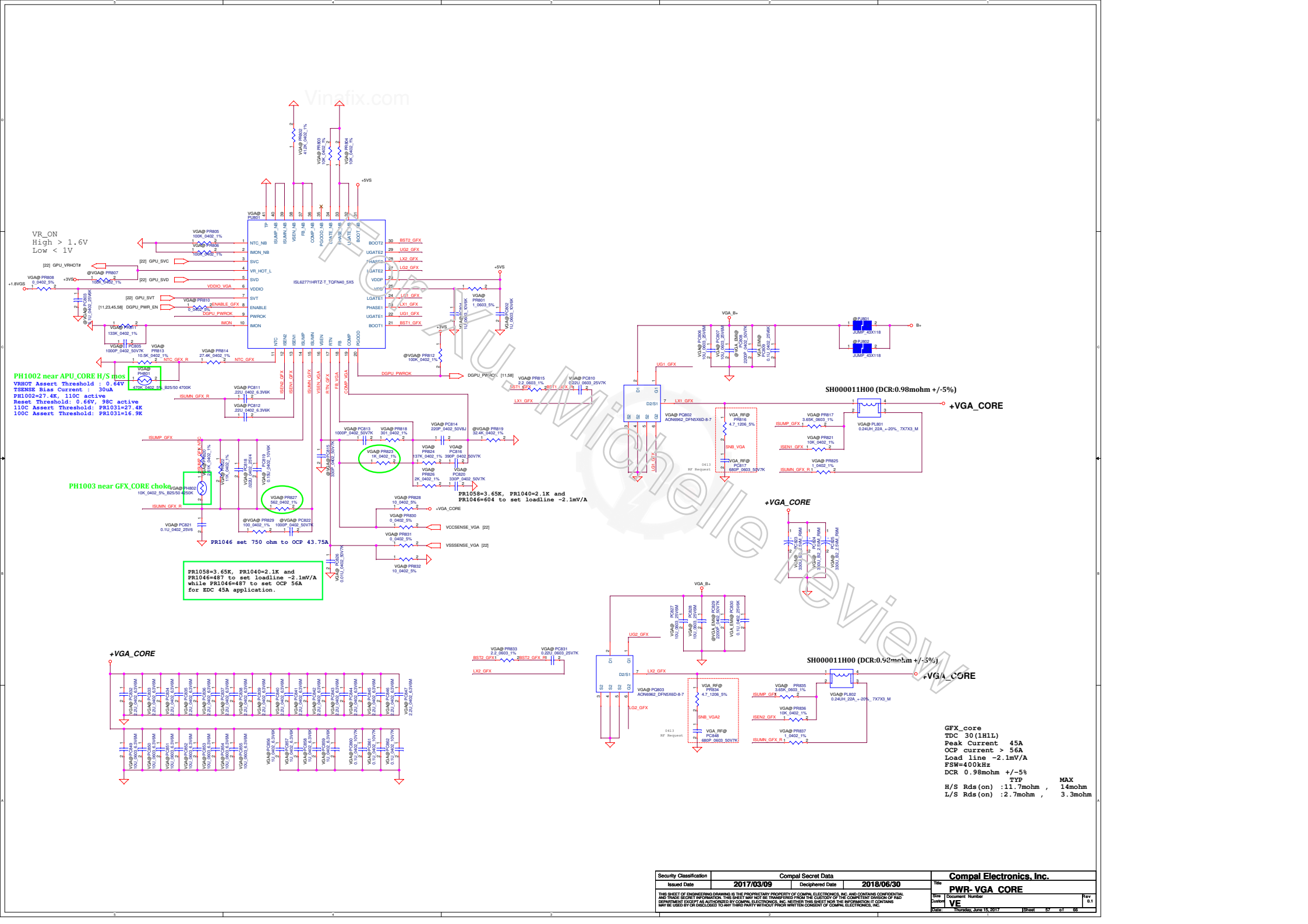

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.			
Title	PWR- VGA_CORE		
Size	Document Number		Rev
Custom	VE		0.1
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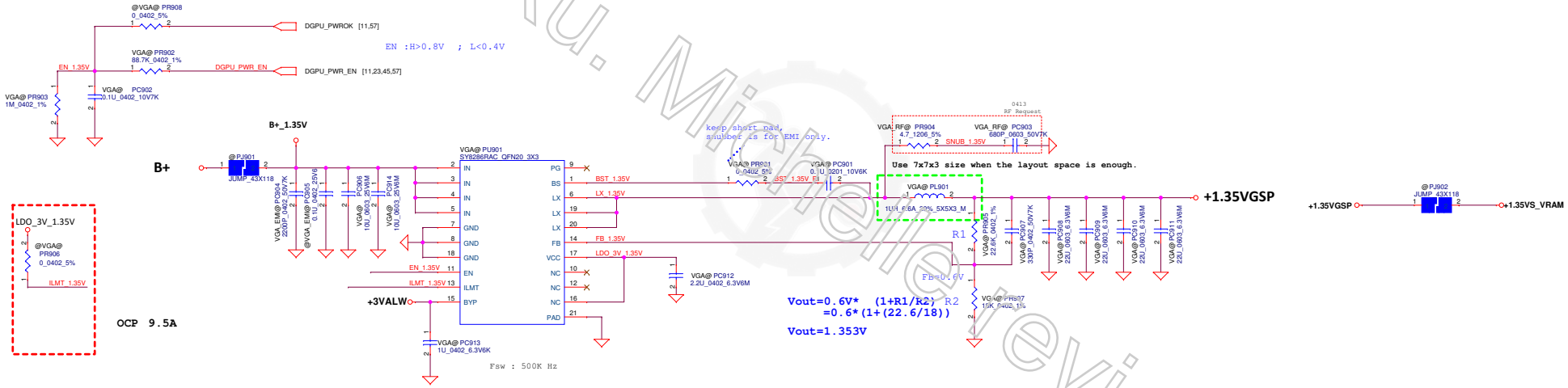

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- 1.35VRAM**

Size	Document Number	Rev
Custom	VE	0.1

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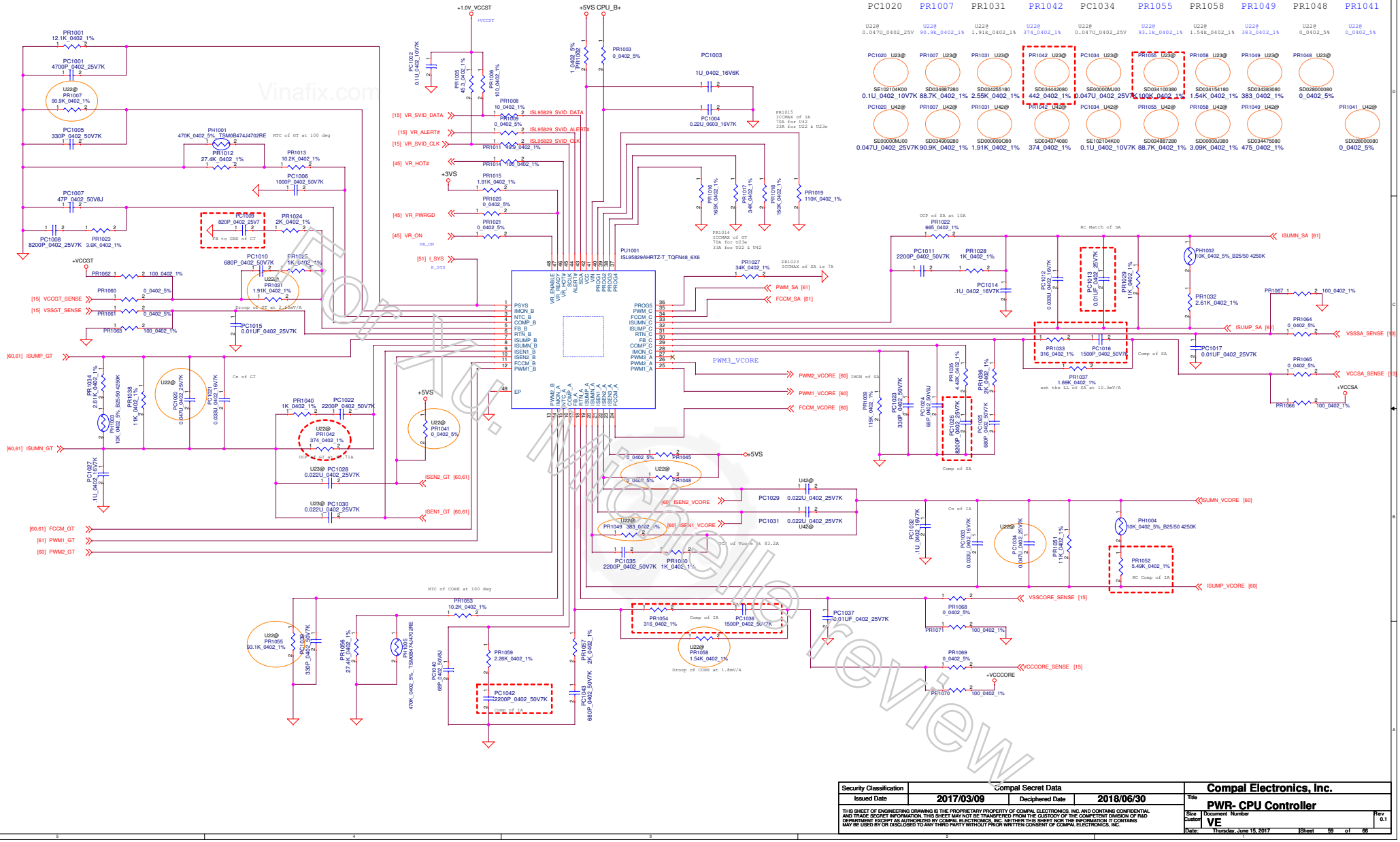

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.	
Title	PWR- CPU Controller
Size / Custom	VE
Document Number	
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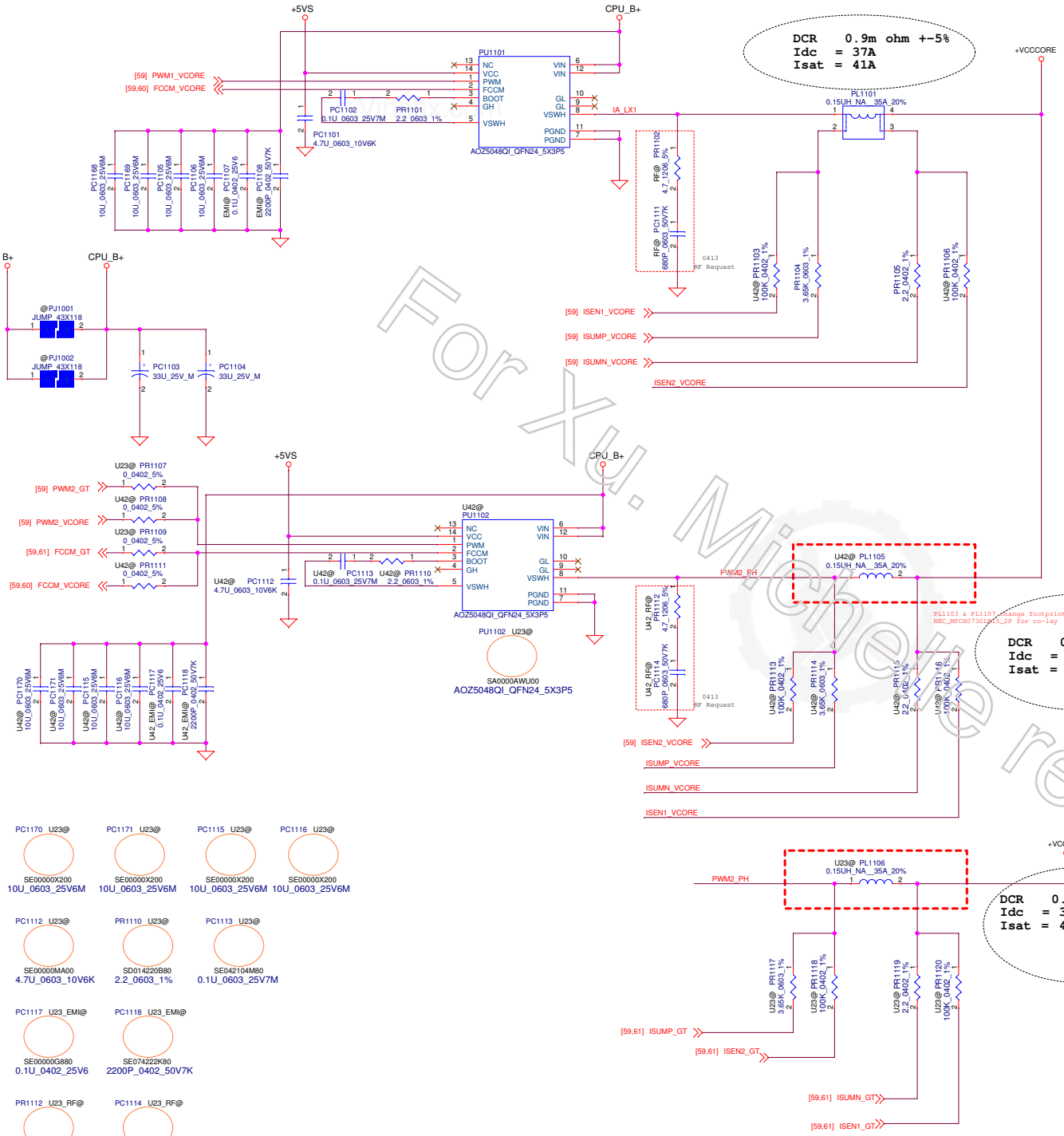

	KBL-R U42 pre-silicon	KBL U22 (GT1/GT2) rev.1.5 EDS rev.1.2/1.5 PAG	KBLU23e (15/28W) rev.1.5 EDS rev.1.2/1.5 PAG
IA+ring ICCMAX[A]	64	29/32	29/32
IA+ring TDC[A]	42	21	21/23
IA+ring di[A]	55	25	25
IA+ring DC/AC LL[mohm]	2.4	2.4	2.4
GT ICCMAX S+US[A]	28	31	64 for merged VR 57 for separated VR
GT TDC[A]	12	18	35/45 for separated VR
GT di[A]	20	28	46
GT DC/AC LL[mohm]	3.1	3.1	2
SA ICCMAX[A]	5	4.5	5.1
SA DC/AC LL[mohm]	10.3	10.3	10.3
PL2 extreme[W]	51	29	43/56
PL4 extreme[W]	71	51	66/86

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- VCCCORE,VCCGT**

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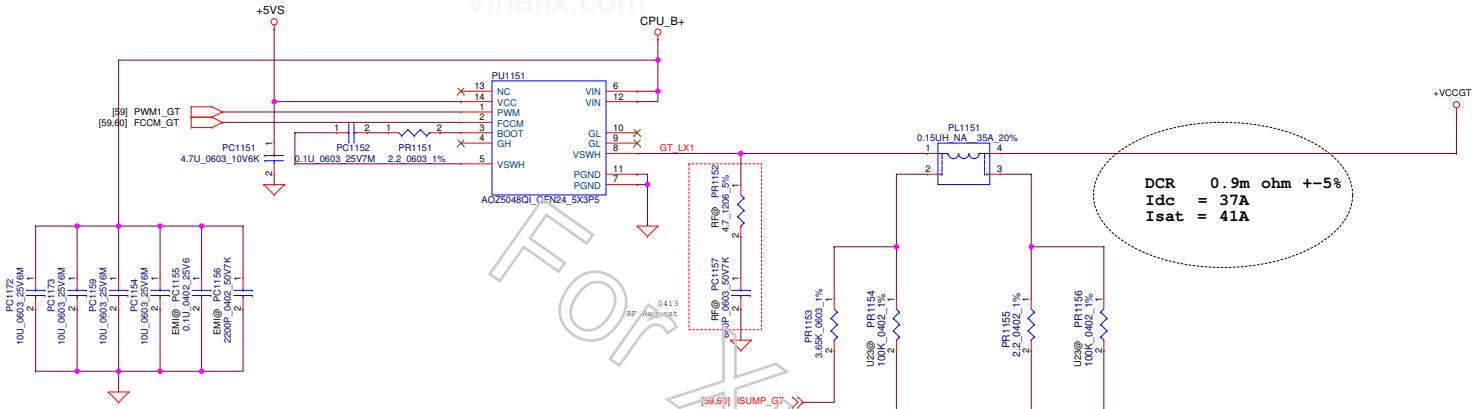
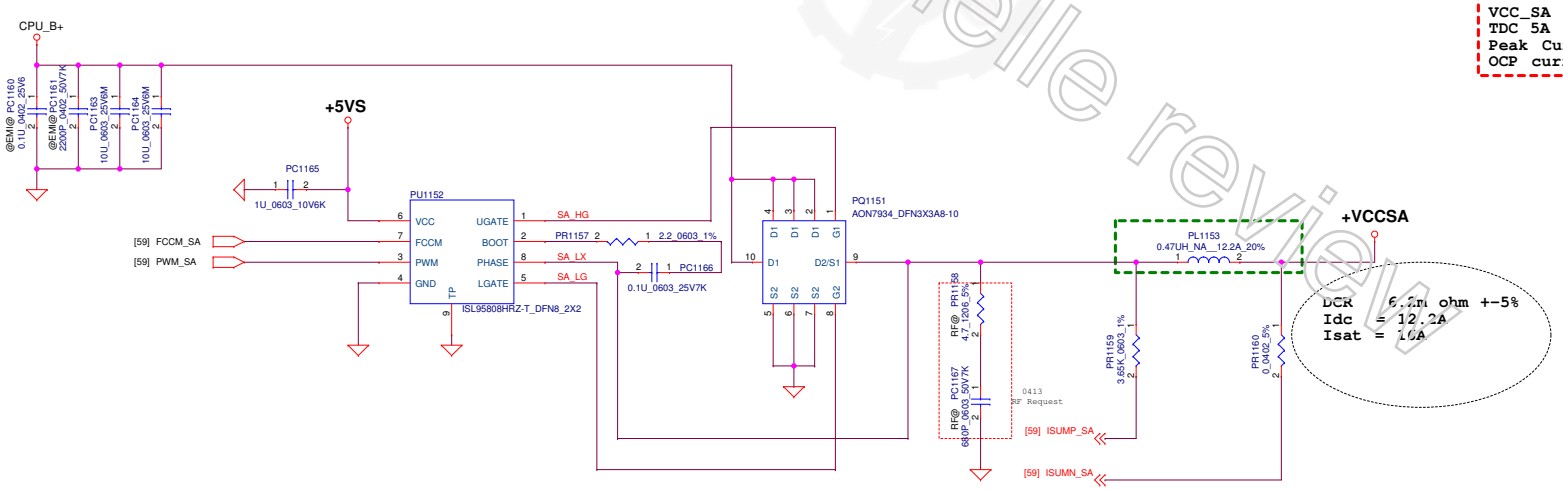
VCC_GT (U-line 22)
TDC 18A
Peak Current 31A
OCP current 37A

VCC_GT Merged(GT+GTx)(U-line 23e)
TDC 35A
Peak Current 64A
OCP current 74A



VCC_SA
TDC 5A
Peak Current 5.1A
OCP current 7A



Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: PWR- VCCGT,VCCSA

Size	Document Number	Rev
	VE	0.1

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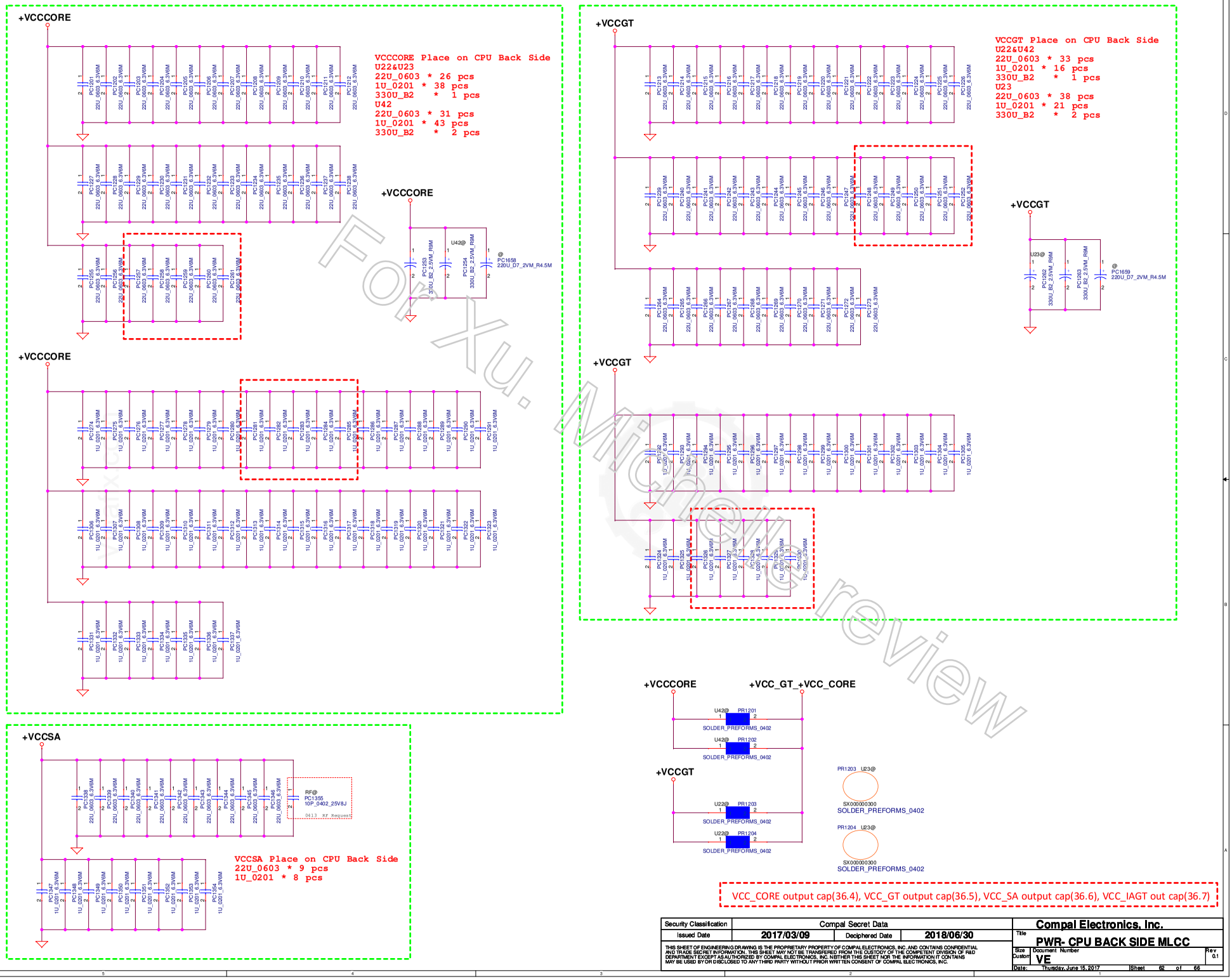

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date	2018/06/30
Title	PWR- CPU BACK SIDE MLCC		
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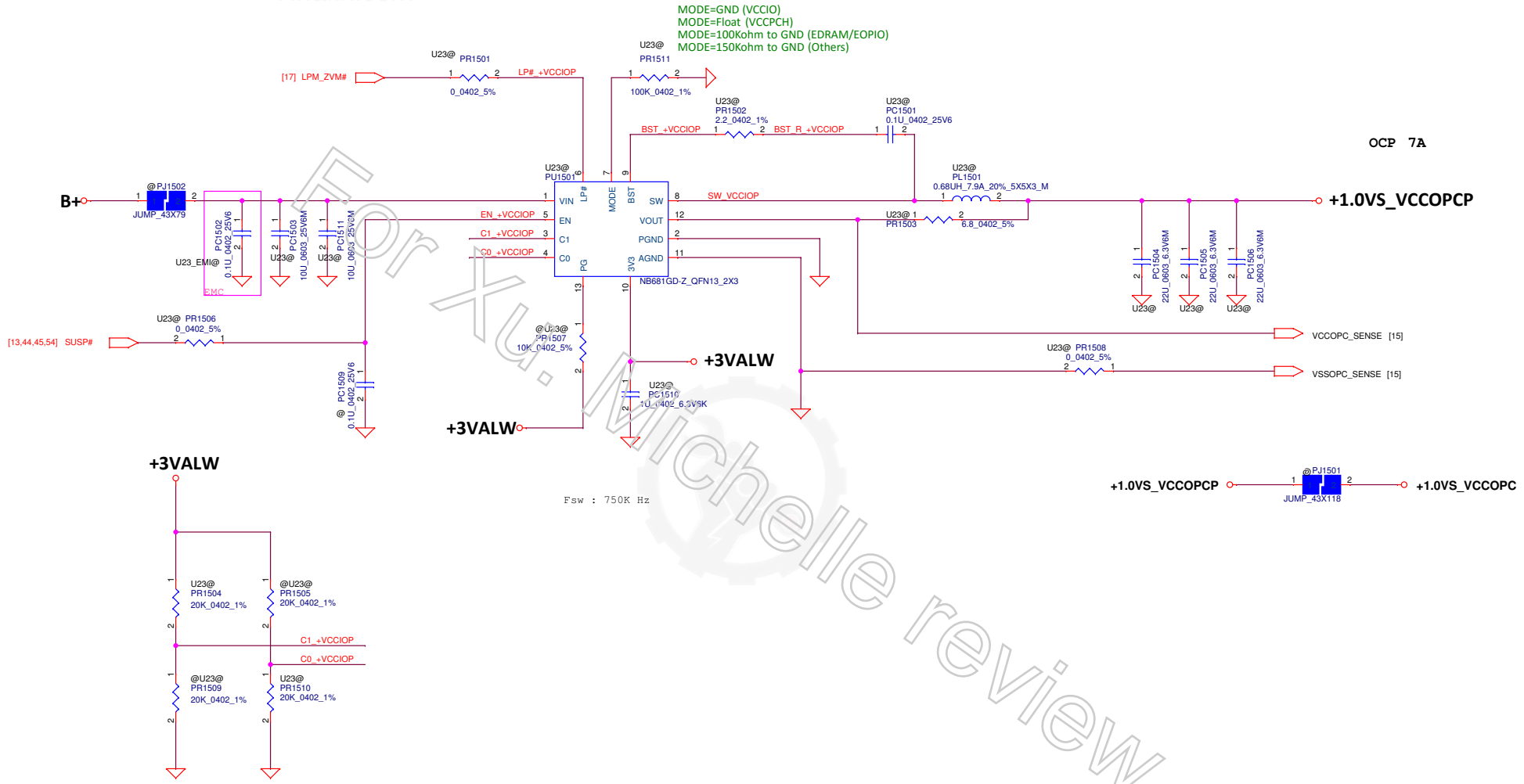

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- VCCOPC**

Size	Document Number	Rev
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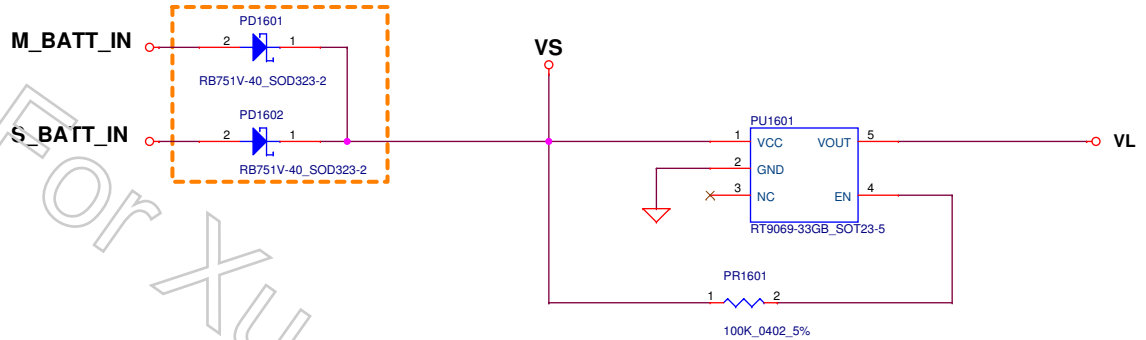

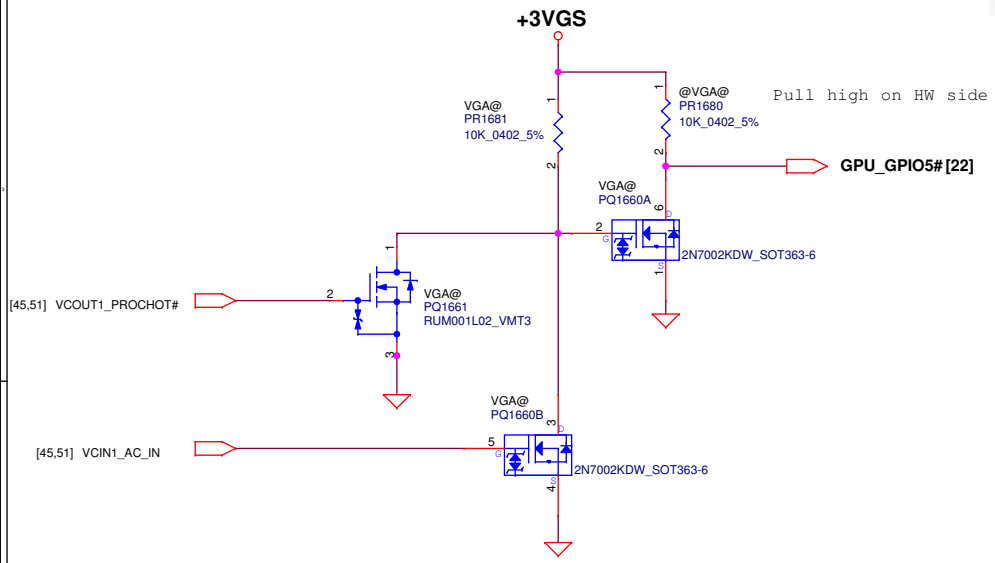

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- Battery Select (1/2)**

Size	Document Number	Rev
Custom	VE	0.1

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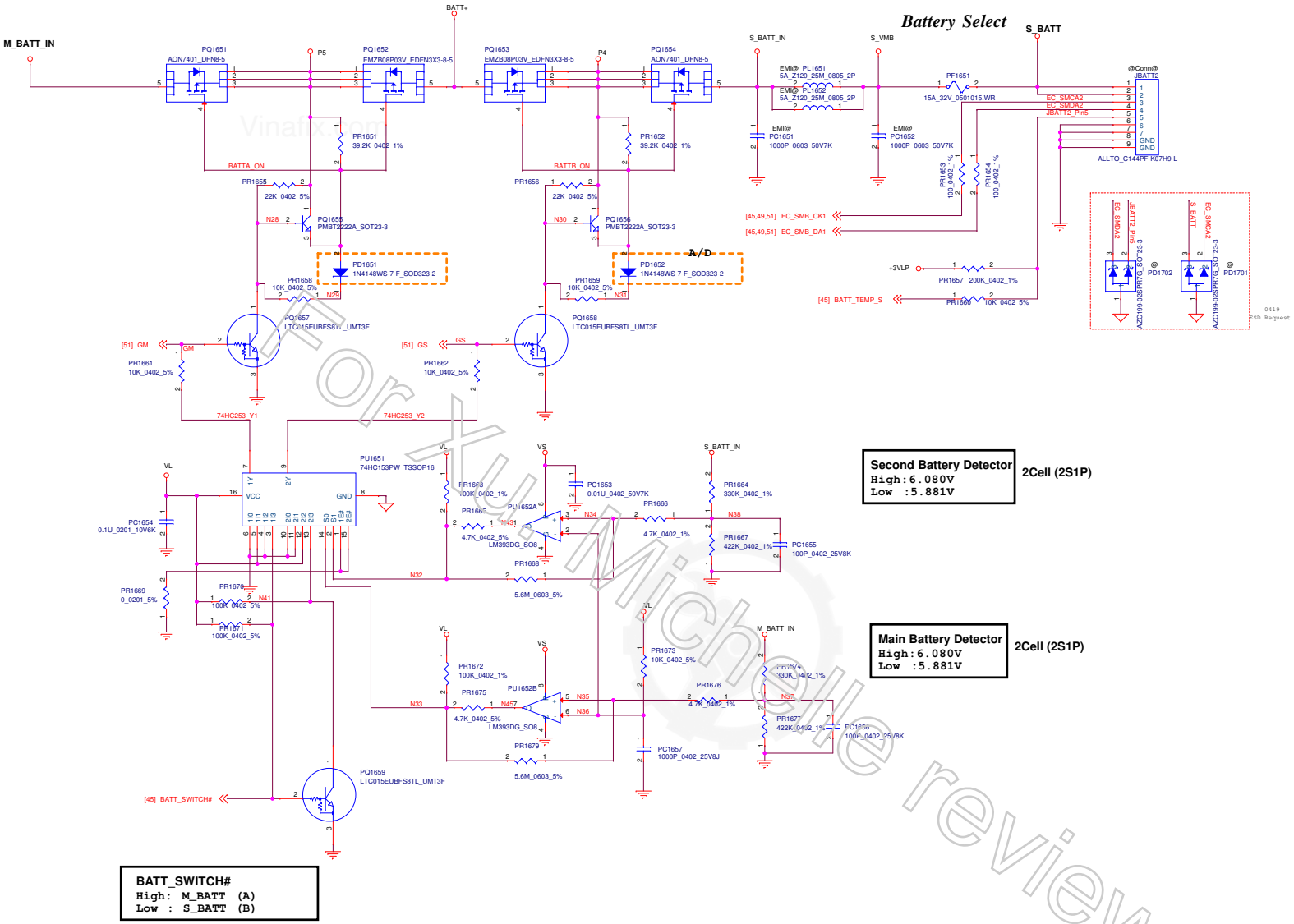

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.			
Title	PWR- Battery Select (2/2)		
Size	Document Number		Rev
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1		62	Change PR1201,PR1202,PR1203,PR1204 from 0.0002_0805_5% to SOLDER_PREFORMS_0402	0606A	SIV
2	Follow battery connector change	49	Change JBATT1 from SUYIN_125022HB008M200ZL to DRAPH_WS33081-S3201-1H	0606A	SIV
3	Adjust 1V voltage to meet ripple spec.	55	Change PR608 from 14.3K_0402_1% to 14K_0402_1%	0606A	SIV
4		64	Change PR1680.2 net from VGA_PROCHOT# to GPU_GPIO5#	0606A	SIV
5		60 61	1. Change PU1101,PU1102,PU1151 from CSD97396Q4M to AOZ5048QI 2. Change PC1101,PC1112,PC1151 from 1U_0603_10V6K to 4.7U_0603_10V6K	0606A	SIV
6		52 60 54 63 60 61	1. Change PC457 from SF000006500 to SF000006R00 2. Change PC1103,PC1104 from SF000006800 to SF000007200 3. Change PL501 from SH00000PJ00 to SH00000YE00 4. Change PL1501 from SH00000UE00 to SH00000Z300 5. Change PL1101,PL1105,PL1106,PL1151 from SH00000X700 to SH00001EF00 6. Change PL1153 from SH000015M00 to SH00001ED00	0606A	SIV
7		57	Change PU801.4 netname from GPU_PROCHOT# to GPU_VRHOT#	0607B	SIV
8	HW request. Avoid +1VALW turn on twice.	55	Change PU601 PGood pull high from +3VALW to +1.8ALWP	0609A	SIV
9		62	Reserve 220u D7 4.5mohm poscap on +VCCCORE and +VCCGT power rails (PC1658,PC1659)	0612A	SIV
10		55 58 63	1. Add PC620 for +1VALW input cap 2. Add PC914 for +1.35VGSP input cap 3. Add PC1511 for +1.0VS_VCCOPCP input cap	0612A	SIV
11		64	1. Change PD1601 from 1N4148WS-7-F_SOD323-2 to RB751V-40_SOD323-2 2. Delete PQ1601,PR1602,PD1603	0614A	SIV
12	For HW sequence request.	58	1. PR902 change from 0 to 88.7K 2. PC902 change to 0.1uF and pop.	0614B	SIV
13	During EC autoload, need turn on power LED	53	Add PR461 for pull high 5VLDO_EN to +3VLP	0614B	SIV

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/03/09	Deciphered Date 2018/06/30	Title: PWR- PIR
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