MS-7817 ATX Ver: 7.0

Intel -ShakeBay plamform

CPU:

INTEL-Haswell LGA1150

CPU DISPLAY

HDMI(portB) DVI (port C)

System Chipset:

H81

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-INTEL/I218-V

SIO:Nuvoton NCT6792D

Main Memory:

DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 1

PWM:

VRD12 - UP1649(3 Phase 6MOS)

Other:

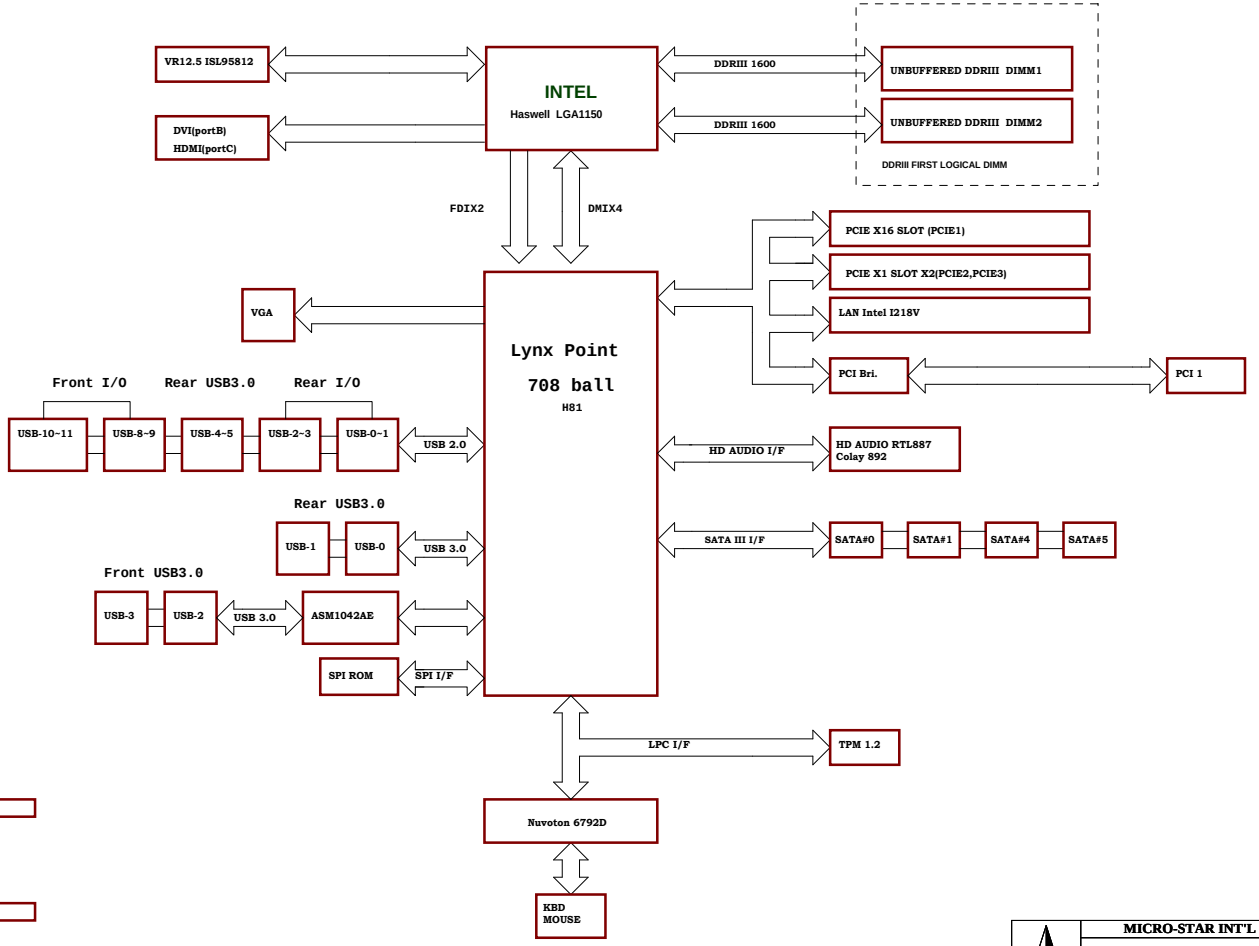
SATA3 *2
SATA2 *2
REAL USB2.0 *4
FRONT USB2.0 *4
REAL USB3.0 *2
FRONT USB3.0 *2

MICRO-STAR INT'L CO.,LTD

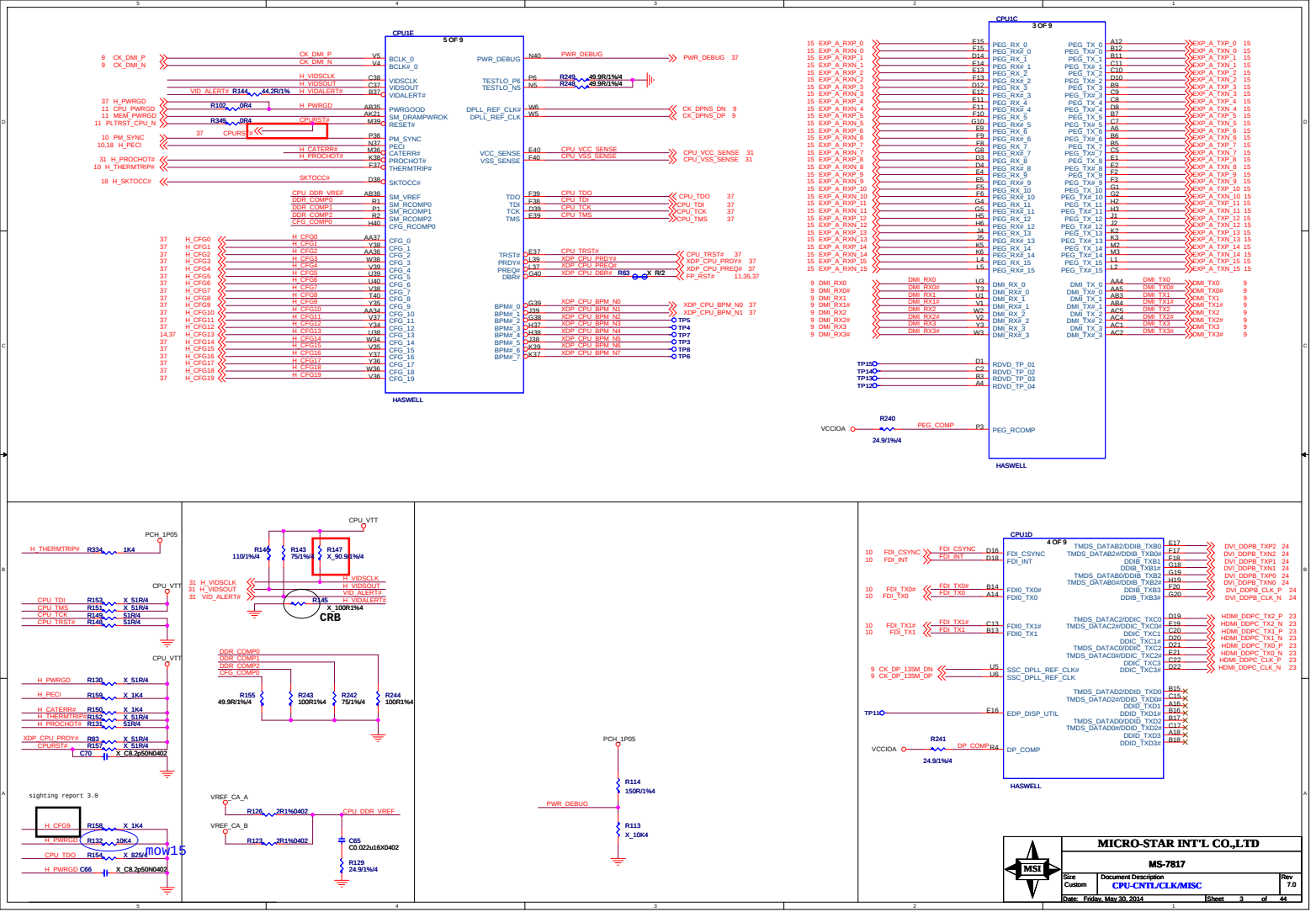
MS-7817

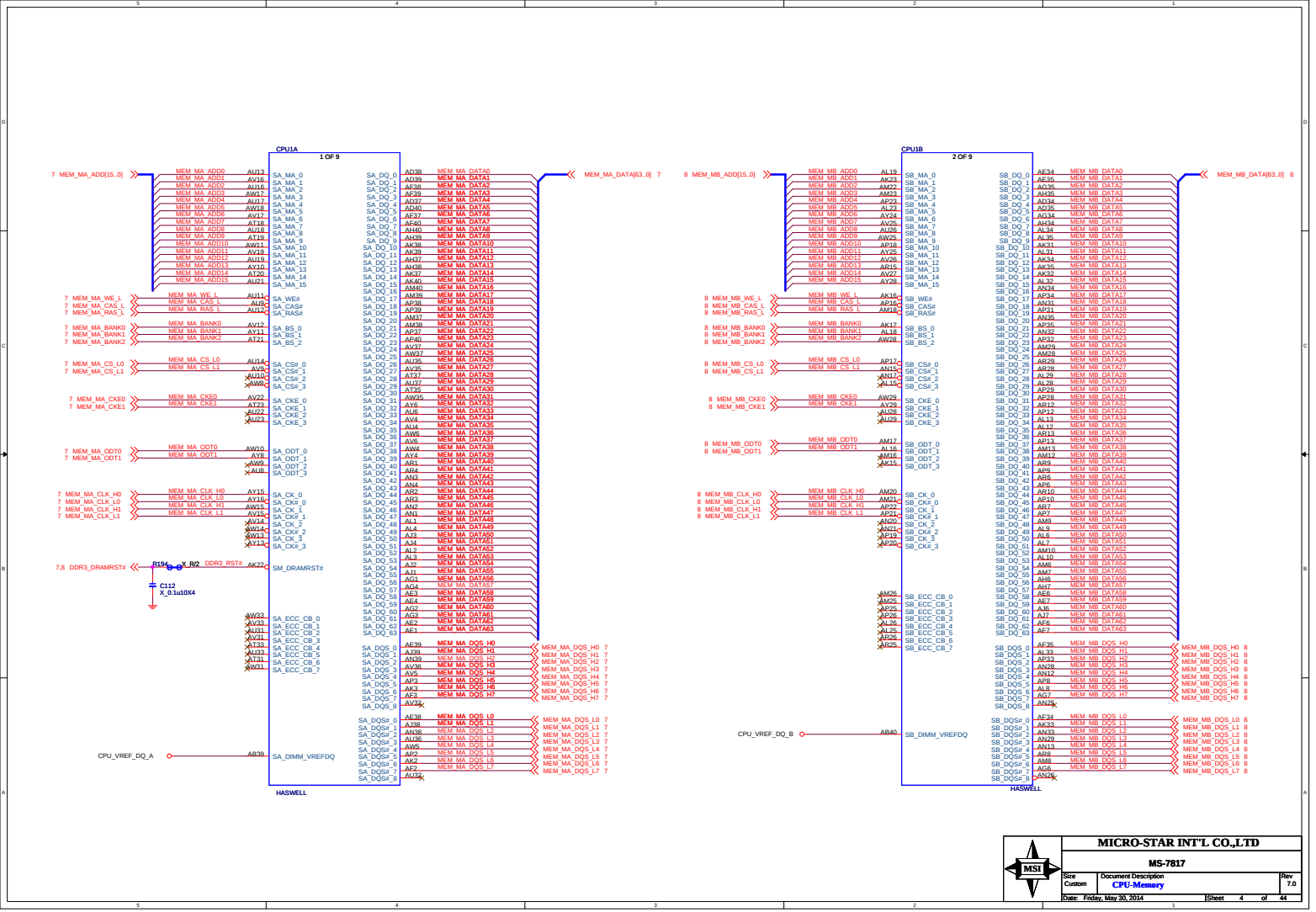
Size: Custom | Document Description: Cover Sheet | Rev: 7.0

Date: Friday, May 30, 2014 | Sheet 1 of 44



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7817	
Size: Custom	Document Description: Block Diagram	Rev: 7.0
Date: Friday, May 30, 2014	Sheet 2 of 44	


CPU1E
5 OF 9
HASWELL
CPU1C
3 OF 9
HASWELL
CPU1D
4 OF 9
HASWELL
PCH_1P05
CPU_VTT
CRB
sighting report 3.0
MICRO-STAR INT'L CO.,LTD
MS-7817
CPU-CNTL/CLK/MISC
Date: Friday, May 30, 2014
Sheet 3 of 44



MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: CPU-Memory	Rev: 7.0
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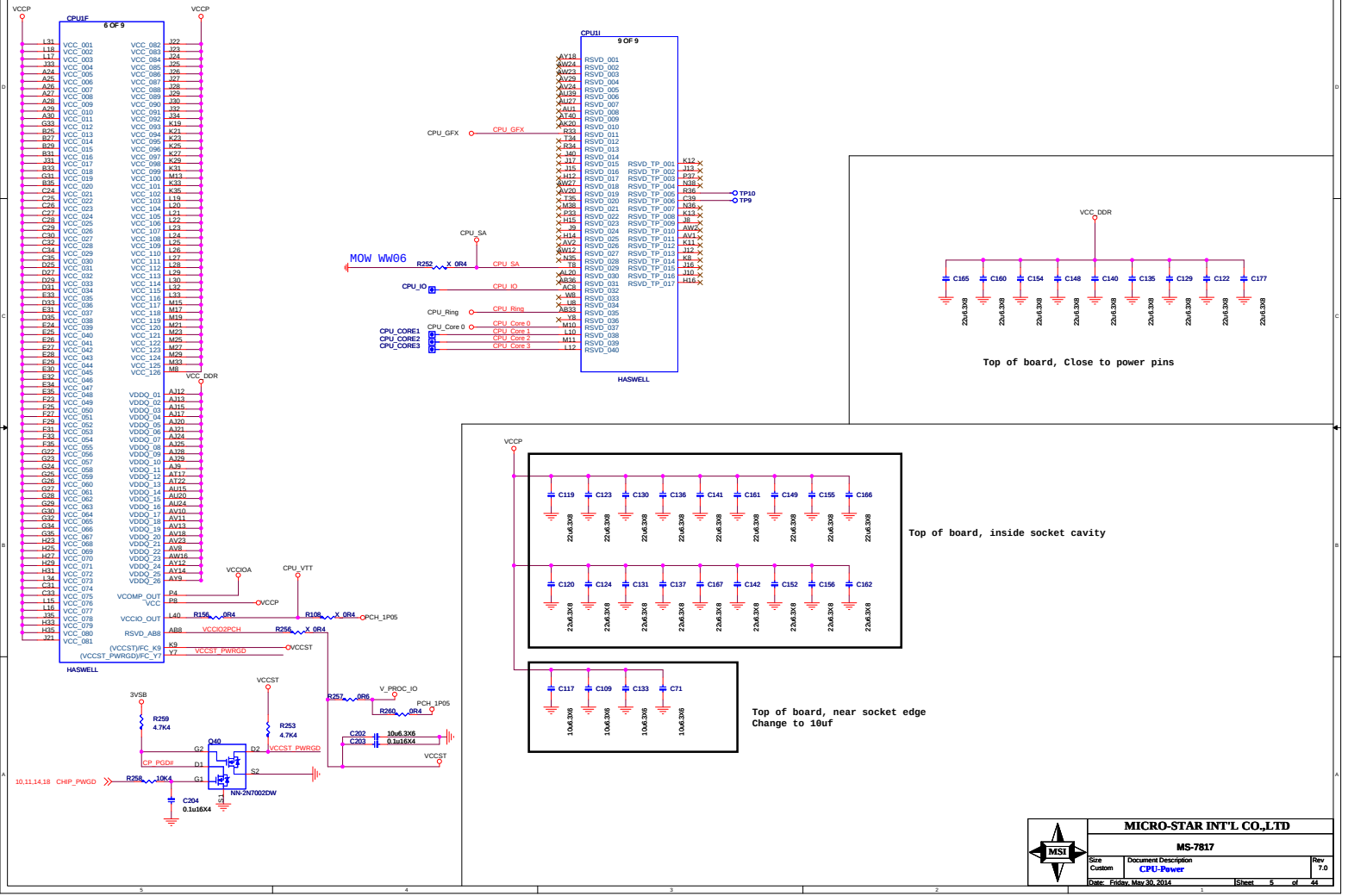

MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: CPU-Power
Rev: 7.0	
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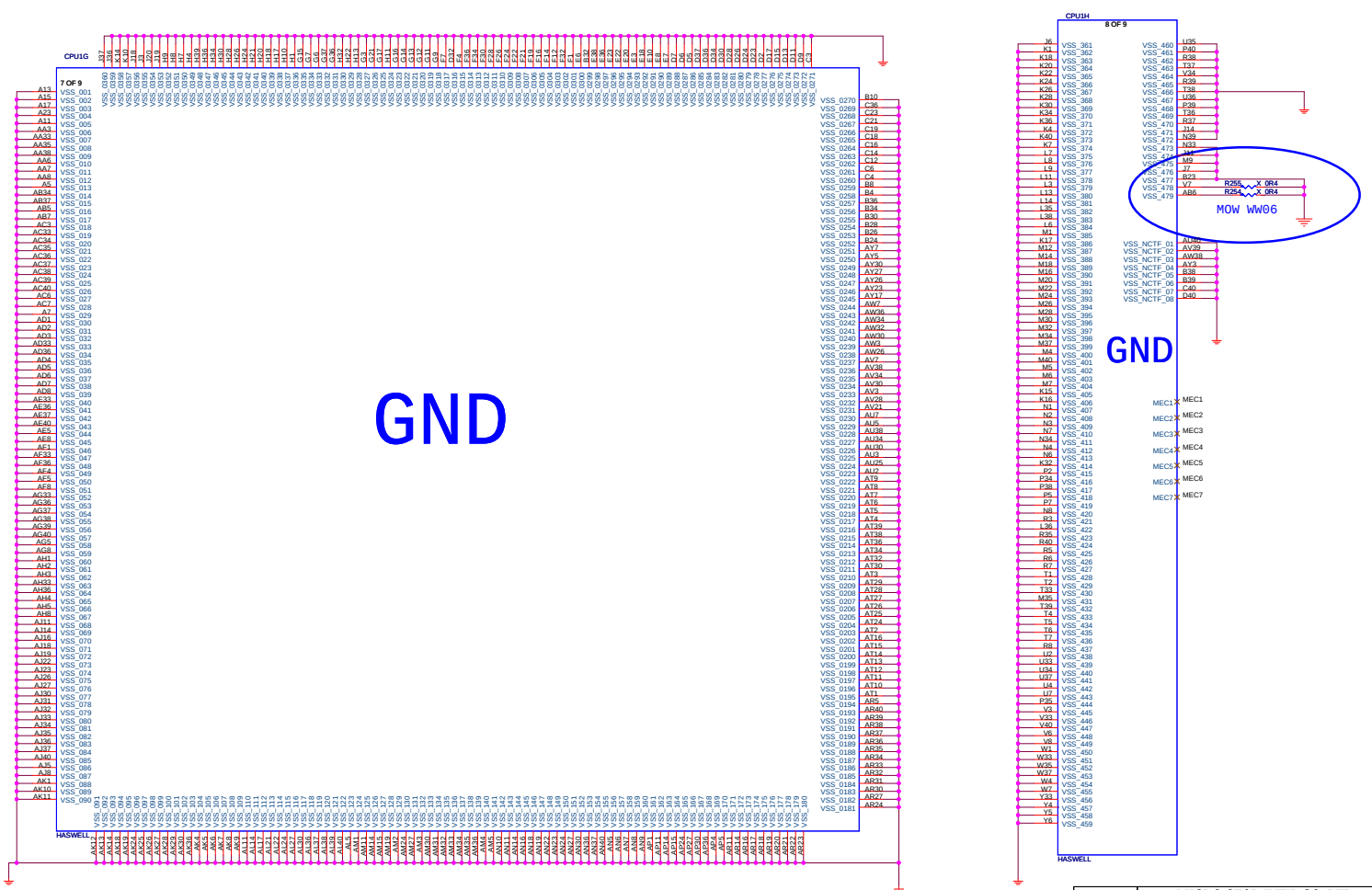
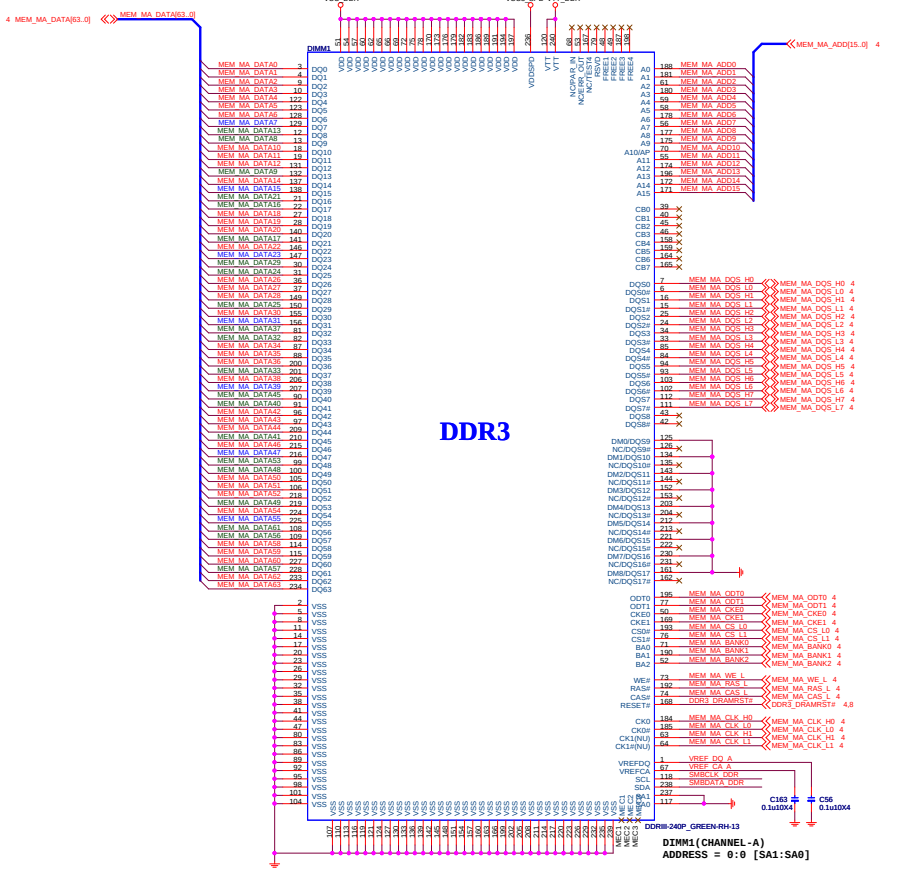
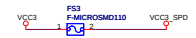


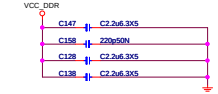
MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: CPU-GND
Rev: 7.0	
Date: Friday, May 30, 2014	Sheet 6 of 44

DDRIII DIMM_A

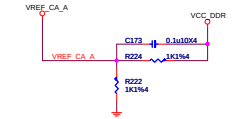




Place close to DIMM1

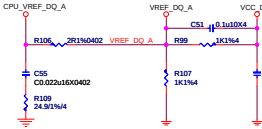


UPI VOLTAGE CONSOLE



Spacing:10/12/12

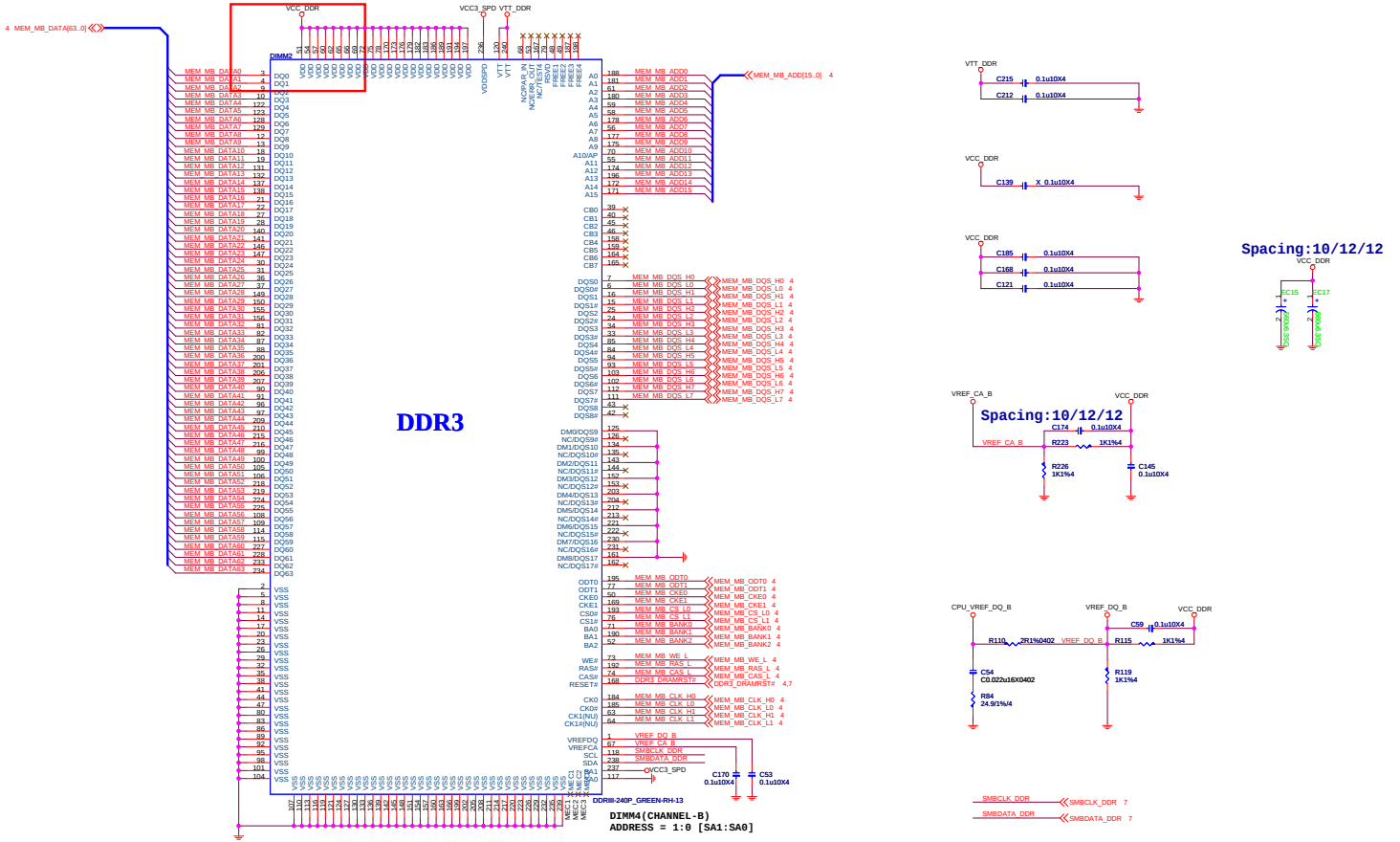
UPI VOLTAGE CONSOLE



Spacing:10/12/12

MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: DDR3 Chanel-A DIMM1	Rev: 7.0
Date: Friday, May 30, 2014	Sheet 7 of 44	

DDRIII DIMM_B



MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: DDR III B DIMM 2
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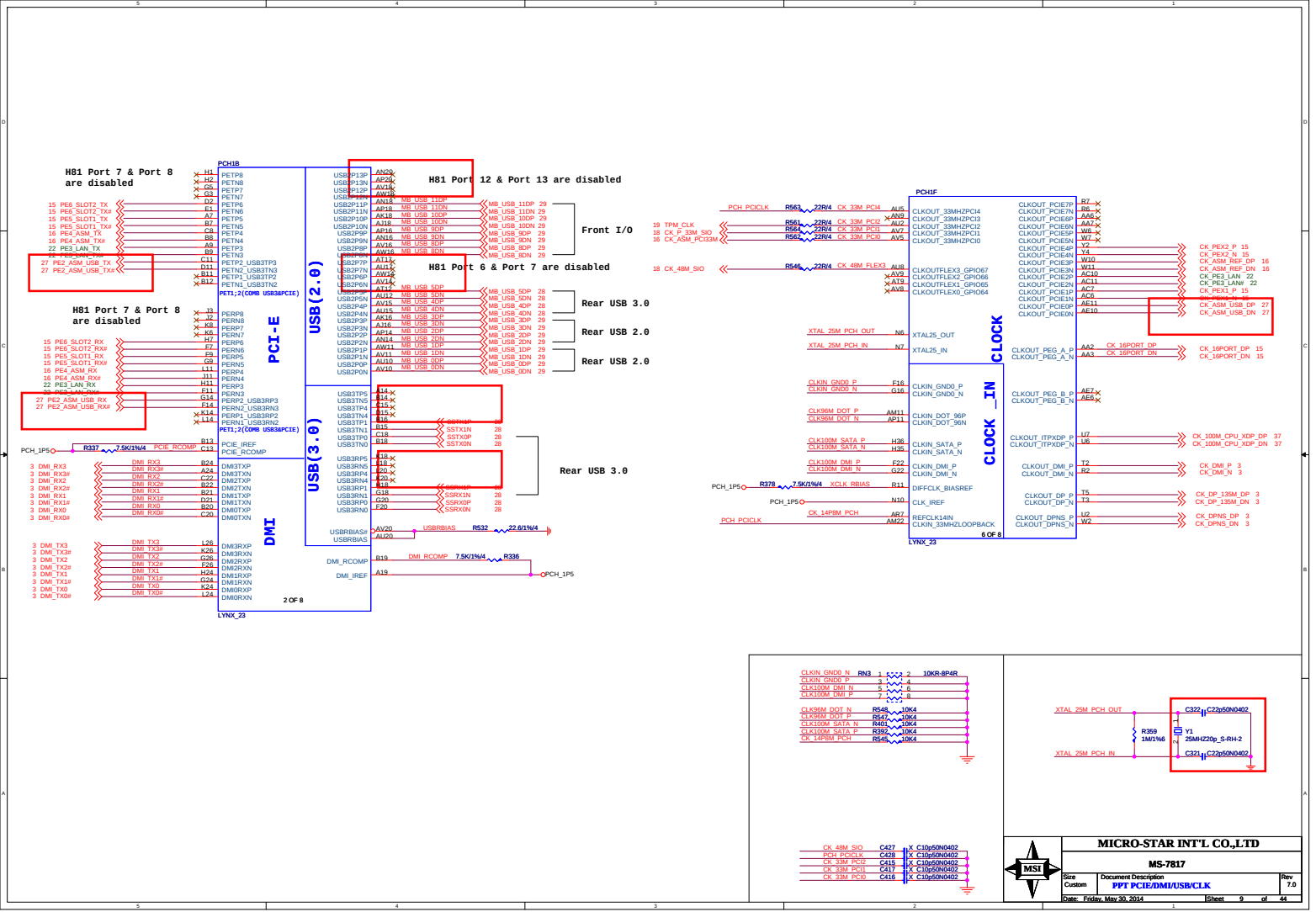
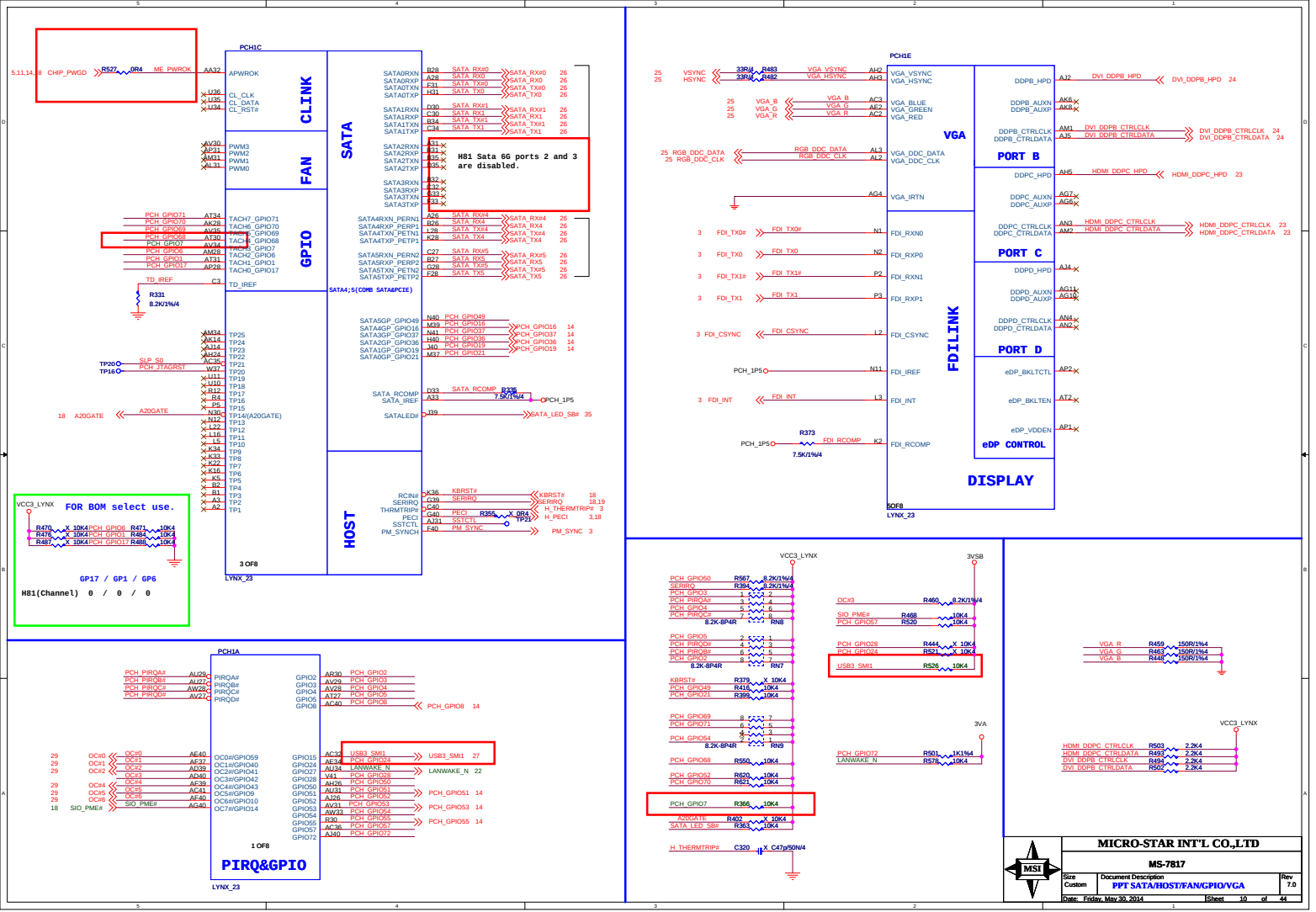

H81 Port 7 & Port 8 are disabled
H81 Port 7 & Port 8 are disabled
H81 Port 12 & Port 13 are disabled
H81 Port 6 & Port 7 are disabled
Front I/O
Rear USB 3.0
Rear USB 2.0
Rear USB 2.0
Rear USB 3.0
PCH1B
PCI-E
USB(2.0)
USB(3.0)
DMI
CLOCK
CLOCK_IN
PCH1F
LYNX_23
2 OF 8
6 OF 8
MICRO-STAR INT'L CO.,LTD
MS-7817
PPT PCIE/DMI/USB/CLK


PCH1C
CLINK
FAN
GPIO
SATA
HOST
APWROK
CL_CLK
CL_DATA
CL_RST#
PWM3
PWM2
PWM1
PWM0
TACH7_GPIO71
TACH6_GPIO70
TACH5_GPIO69
TACH4_GPIO68
TACH3_GPIO7
TACH2_GPIO6
TACH1_GPIO1
TACH0_GPIO17
TD_IREF
R331
8.2K/1%/4
TP25
TP24
TP23
TP22
TP21
TP20
TP19
TP18
TP17
TP16
TP15
TP14/(A20GATE)
TP13
TP12
TP11
TP10
TP9
TP8
TP7
TP6
TP5
TP4
TP3
TP2
TP1
3 OF8
LYNX_23
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
H81 Sata 6G ports 2 and 3 are disabled.
SATA4RXN_PERN1
SATA4RXP_PERP1
SATA4TXN_PETN1
SATA4TXP_PETP1
SATA5RXN_PERN2
SATA5RXP_PERP2
SATA5TXN_PETN2
SATA5TXP_PETP2
SATA4;5(COMB SATA&PCIE)
SATA5GP_GPIO49
SATA4GP_GPIO16
SATA3GP_GPIO37
SATA2GP_GPIO36
SATA1GP_GPIO19
SATA0GP_GPIO21
SATA_RCOMP
SATA_IREF
SATALED#
BCI#
SERIRQ
THRMTRIP#
PECI
SSTCTL
PM_SYNCH
KBRST#
H_THERMTRIP#
H_PECI
PM_SYNC
FOR BOM select use.
GP17 / GP1 / GP6
H81(Channel) 0 / 0 / 0
PCH1E
VGA
PORT B
PORT C
PORT D
FDILINK
eDP CONTROL
DISPLAY
VGA_VSYNC
VGA_HSYNC
VGA_BLUE
VGA_GREEN
VGA_RED
VGA_DDC_DATA
VGA_DDC_CLK
VGA_IRTN
DDPB_HPD
DDPB_AUXN
DDPB_AUXP
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_HPD
DDPC_AUXN
DDPC_AUXP
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_HPD
DDPD_AUXN
DDPD_AUXP
DDPD_CTRLCLK
DDPD_CTRLDATA
eDP_BKLTCTL
eDP_BKLTEN
eDP_VDDEN
FDI_RXN0
FDI_RXP0
FDI_RXN1
FDI_RXP1
FDI_CSYNC
FDI_IREF
FDI_INT
FDI_RCOMP
FDI_TX0#
FDI_TX0
FDI_TX1#
FDI_TX1
R373
7.5K/1%/4
LYNX_23
PCH1A
PIRQ&GPIO
1 OF8
LYNX_23
PIRQA#
PIRQB#
PIRQC#
PIRQD#
OC#0
OC#1
OC#2
OC#3
OC#4
OC#5
OC#6
OC#7
SIO_PME#
GPIO2
GPIO3
GPIO4
GPIO5
GPIO8
GPIO15
GPIO24
GPIO27
GPIO28
GPIO50
GPIO51
GPIO52
GPIO53
GPIO54
GPIO55
GPIO57
GPIO72
USB3_SMI1
LANWAKE_N
PCH_GPIO8
PCH_GPIO51
PCH_GPIO53
PCH_GPIO55
VCC3_LYNX
3VSB
3VA
R567
R384
R383
R379
R369
R368
R366
R402
R363
R460
R408
R520
R444
R521
R526
R501
R578
R459
R463
R448
R503
R497
R494
R502
C320
MICRO-STAR INT'L CO.,LTD
MS-7817
PPT SATA/HOST/FAN/GPIO/VGA
Rev 7.0
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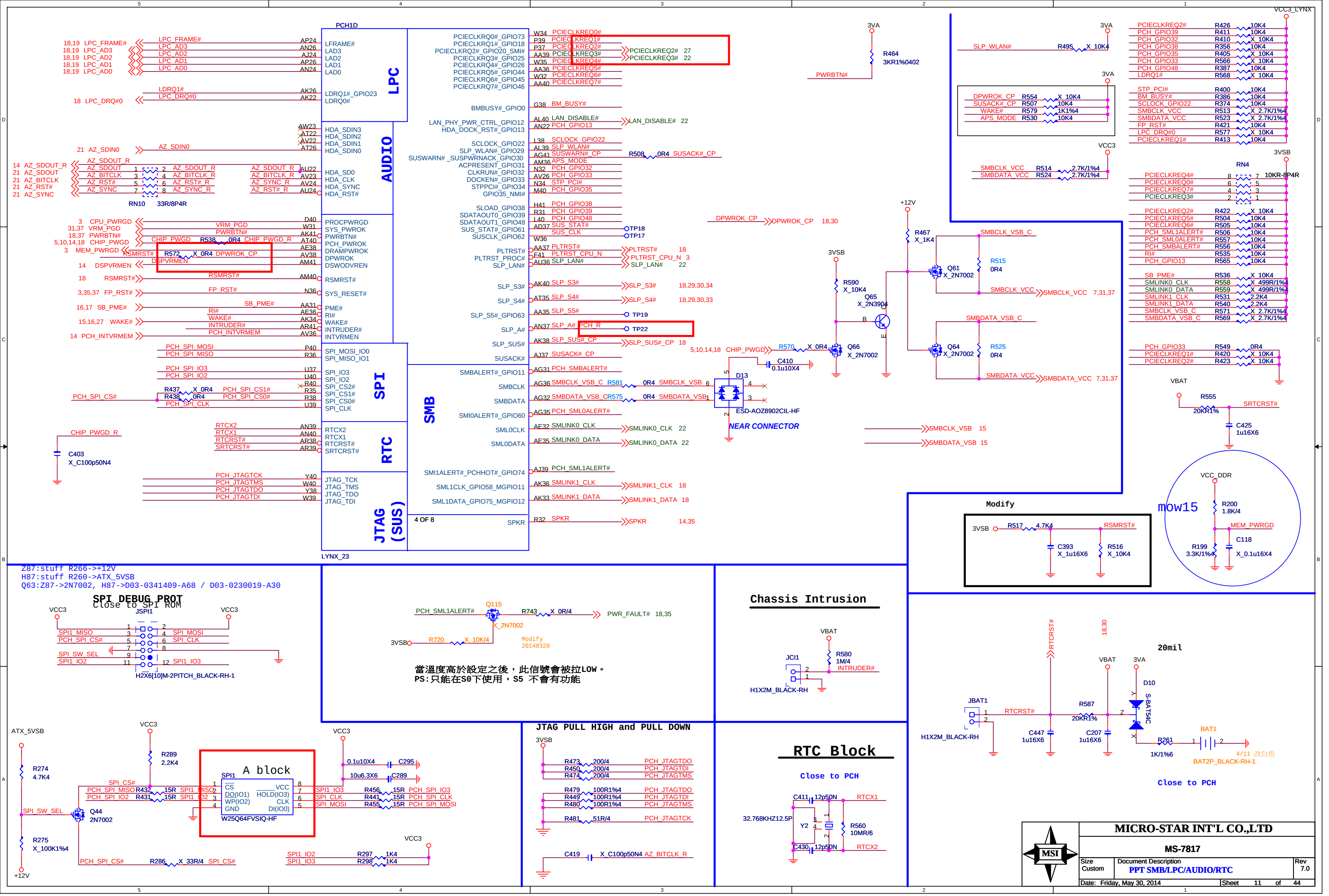
PCH1D
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
4 OF 8
LYNX_23
LFRAME#
LAD3
LAD2
LAD1
LAD0
LDRQ1#_GPIO23
LDRQ0#
HDA_SDIN3
HDA_SDIN2
HDA_SDIN1
HDA_SDIN0
HDA_SDO
HDA_CLK
HDA_SYNC
HDA_RST#
PROCPWRGD
SYS_PWROK
PWRBTN#
PCH_PWROK
DRAMPWROK
DPWROK
DSWODVREN
RSMRST#
SYS_RESET#
PME#
RI#
WAKE#
INTRUDER#
INTVRMEN
SPI_MOSI_IO0
SPI_MISO_IO1
SPI_IO3
SPI_IO2
SPI_CS2#
SPI_CS1#
SPI_CS0#
SPI_CLK
RTCX2
RTCX1
RTCRST#
SRTCRST#
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
PCIECLKRQ0#_GPIO73
PCIECLKRQ1#_GPIO18
PCIECLKRQ2#_GPIO20_SMI#
PCIECLKRQ3#_GPIO25
PCIECLKRQ4#_GPIO26
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
BMBUSY#_GPIO0
LAN_PHY_PWR_CTRL_GPIO12
HDA_DOCK_RST#_GPIO13
SCLOCK_GPIO22
SLP_WLAN#_GPIO29
SUSWARN#_SUSPWRNACK_GPIO30
ACPRESENT_GPIO31
CLKRUN#_GPIO32
DOCKEN#_GPIO33
STPPCI#_GPIO34
GPIO35_NMI#
SLOAD_GPIO38
SDATAOUT0_GPIO39
SDATAOUT1_GPIO48
SUS_STAT#_GPIO61
SUSCLK_GPIO62
PLTRST#
PLTRST_PROC#
SLP_LAN#
SLP_S3#
SLP_S4#
SLP_S5#_GPIO63
SLP_A#
SLP_SUS#
SUSACK#
SMBALERT#_GPIO11
SMBCLK
SMBDATA
SMI0ALERT#_GPIO60
SML0CLK
SML0DATA
SMI1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO58_MGPIO11
SML1DATA_GPIO75_MGPIO12
SPKR
PCIECLKREQ2# 27
PCIECLKREQ3# 22
LAN_DISABLE# 22
DPWROK_CP 18,30
SMBCLK_VCC 7,31,37
SMBDATA_VCC 7,31,37
SMBCLK_VSB 15
SMBDATA_VSB 15
ESD-AOZ8902CIL-HF
NEAR CONNECTOR
RN10 33R/8P4R
RN4 10KR-8P4R
Modify
mow15
Z87:stuff R266->+12V
H87:stuff R260->ATX_5VSB
Q63:Z87->2N7002, H87->D03-0341409-A68 / D03-0230019-A30
SPI DEBUG PROT
Close to SPI ROM
JSPI1
H2X6[10]M-2PITCH_BLACK-RH-1
A block
SPI1
W25Q64FVSIQ-HF
PWR_FAULT# 18,35
Modify 20140320
當溫度高於設定之後，此信號會被拉LOW。
PS:只能在S0下使用，S5 不會有功能
Chassis Intrusion
JCI1
H1X2M_BLACK-RH
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
32.768KHZ12.5P
20mil
JBAT1
H1X2M_BLACK-RH
BAT1
BAT2P_BLACK-RH-1
4/11 改白色
Close to PCH
MICRO-STAR INT'L CO.,LTD
MS-7817
Size Custom
Document Description
PPT SMB/LPC/AUDIO/RTC
Rev 7.0
Date: Friday, May 30, 2014
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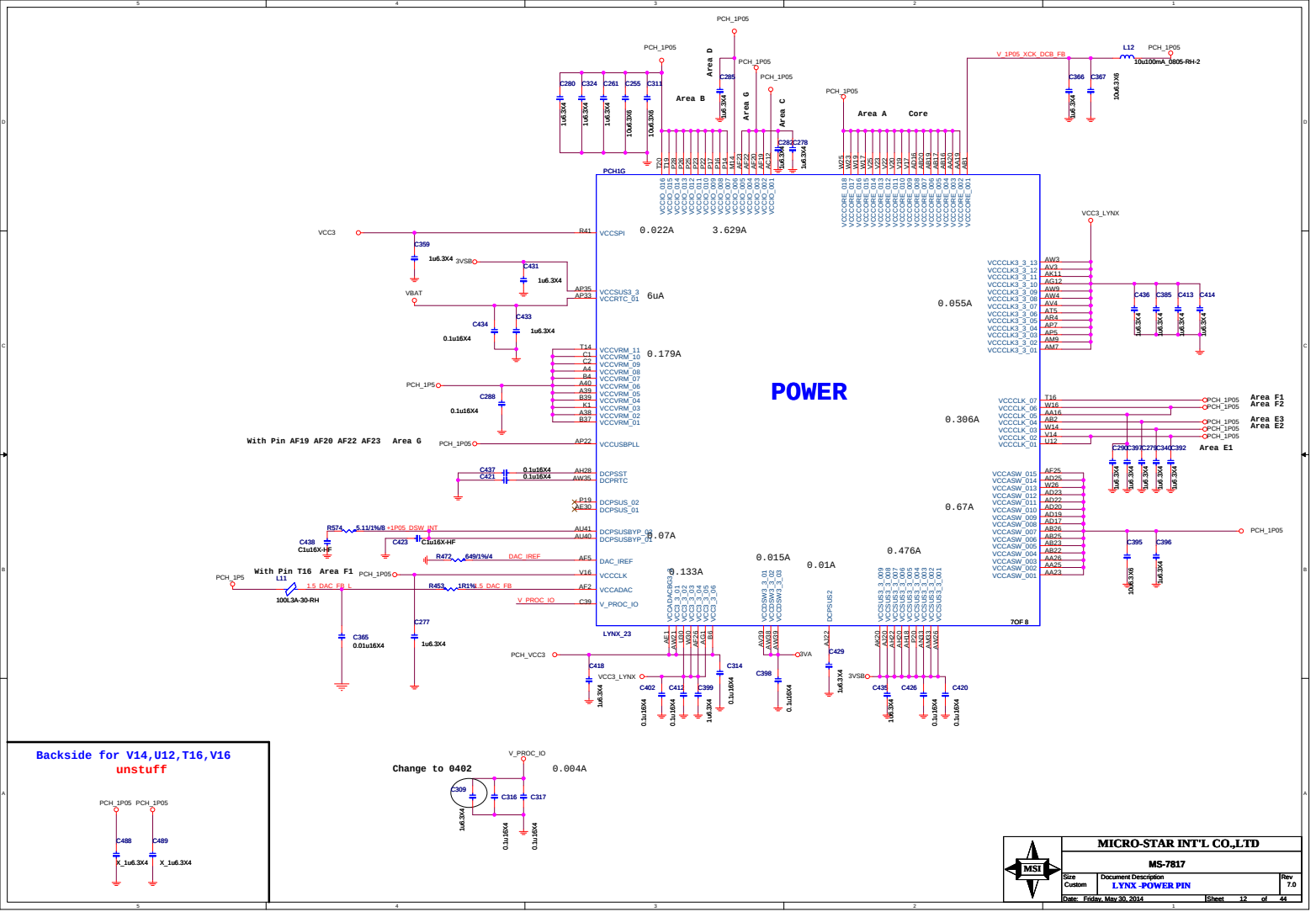
POWER
PCH1G
LYNX_23
7OF 8
Area A
Core
Area B
Area C
Area D
Area E1
Area E2
Area E3
Area F1
Area F2
Area G
0.022A
3.629A
6uA
0.179A
0.055A
0.306A
0.67A
0.07A
0.133A
0.015A
0.01A
0.476A
0.004A
With Pin AF19 AF20 AF22 AF23 Area G
With Pin T16 Area F1
Change to 0402
Backside for V14,U12,T16,V16
unstuff
MICRO-STAR INT'L CO.,LTD
MS-7817
LYNX -POWER PIN
Date: Friday, May 30, 2014
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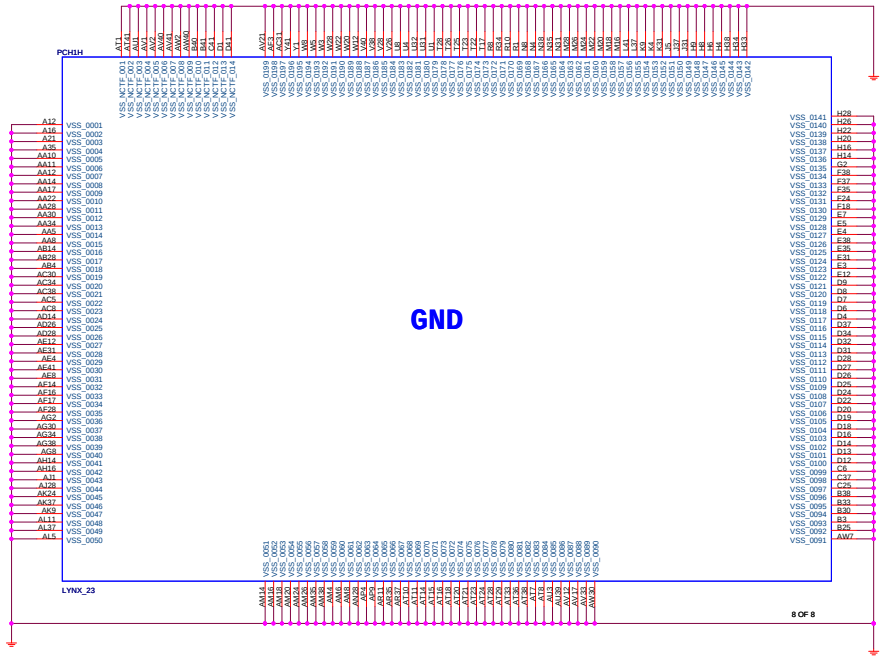

MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: PPT GND/NVRAM
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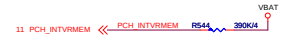
Pull high to enable integrated VRM



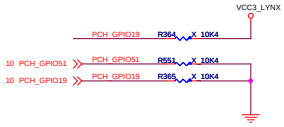
Pull high to enable integrated Deep-Sx well On-die VR

Internal weak pull down
Pull high to enable "No Reboot" mode

Internal weak pull up
Pull low to enable "Top-Block Swap" mode

BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



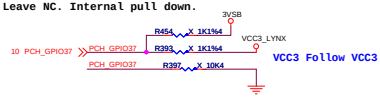
Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.

Enable TLS:

Pull up with 1k Ohm to VccSus3.3.

Default (Disable TLS):

Leave NC. Internal pull down.

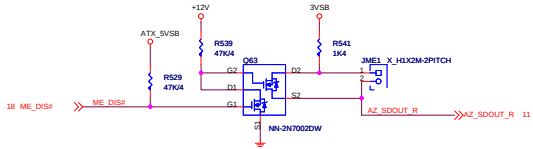


Default:

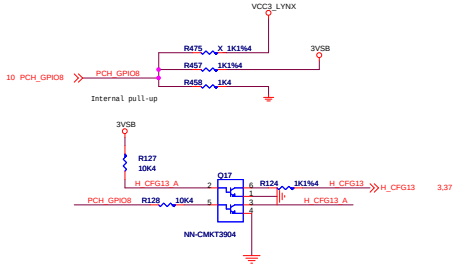
Do not pull high.

Disable ME in Manufacturing Mode:

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

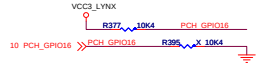


Follow CRG 1.0

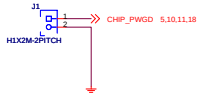


Internal weak pull down (function reserved)
Signal should not be pulled high when strap is sampled

PCIE1 and SATA4 flexible IO function select
High: SATA Low: PCIE



For test cpu voltage



MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: PPT STRAPS
Rev: 7.0	
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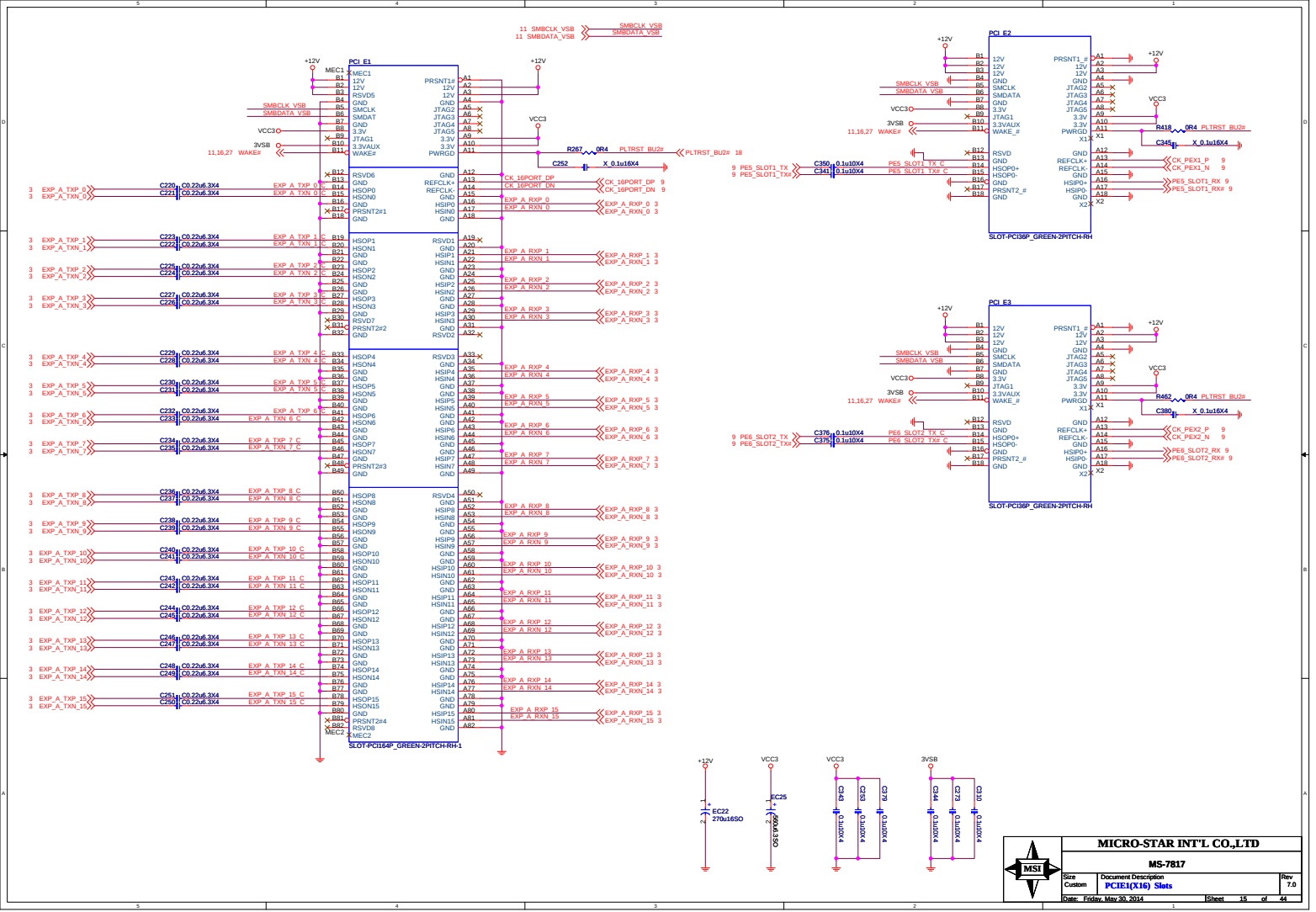
PCI E1
PCI_E2
PCI E3
SLOT-PCI164P_GREEN-2PITCH-RH-1
SLOT-PCI36P_GREEN-2PITCH-RH
SMBCLK_VSB
SMBDATA_VSB
PLTRST_BU2#
MICRO-STAR INT'L CO.,LTD
MS-7817
PCIE1(X16) Slots
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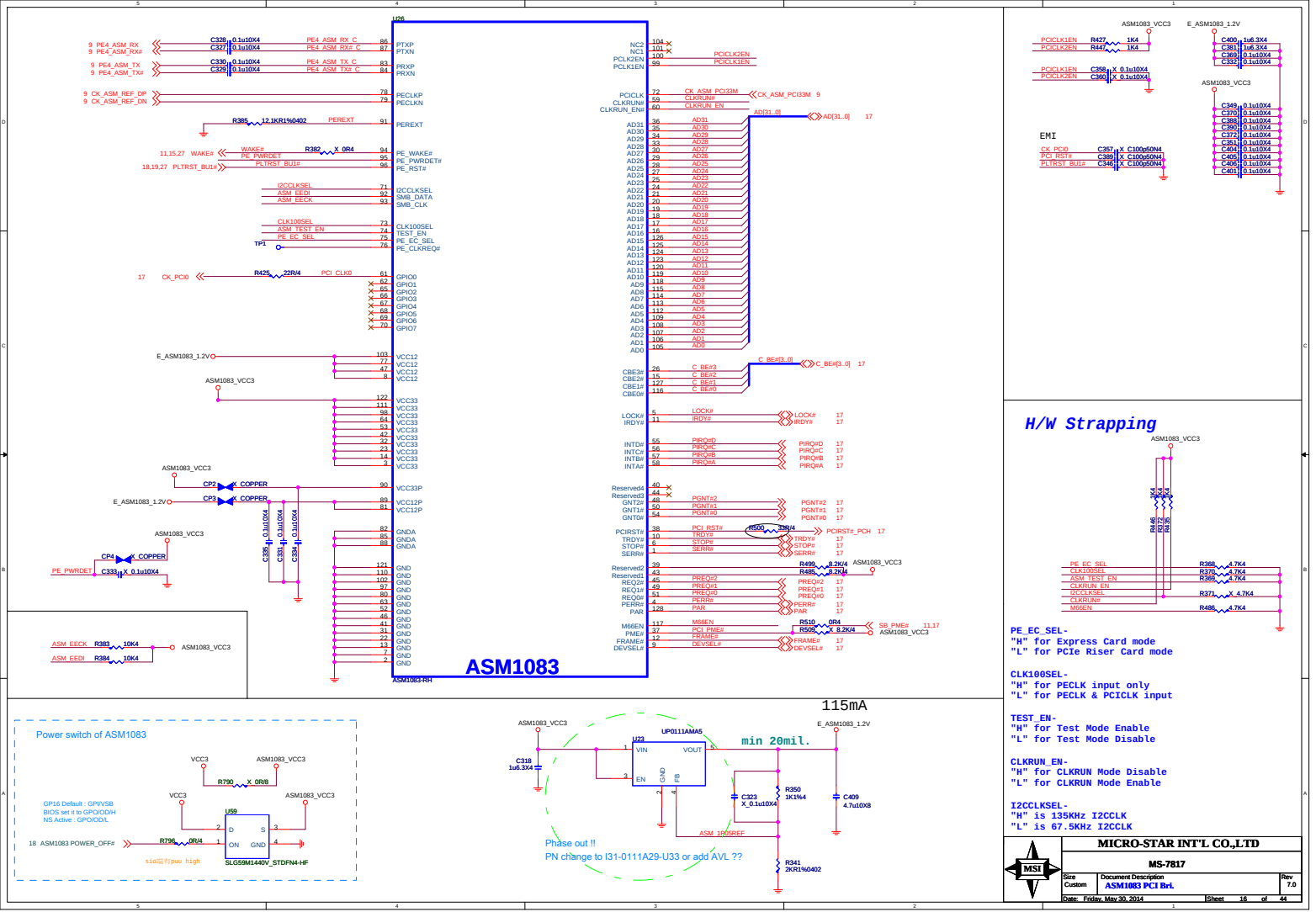
ASM1083
ASM1083-RH
U26
PTXP
PTXN
PRXP
PRXN
PECLKP
PECLKN
PEREXT
PE_WAKE#
PE_PWRDET#
PE_RST#
I2CCLKSEL
SMB_DATA
SMB_CLK
CLK100SEL
TEST_EN
PE_EC_SEL
PE_CLKREQ#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
VCC12
VCC33
VCC33P
VCC12P
GNDA
GND
PCICLK2EN
PCICLK1EN
CK_ASM_PCI33M
CLKRUN#
CLKRUN_EN
AD[31..0]
C_BE#[3..0]
LOCK#
IRDY#
PIRQ#D
PIRQ#C
PIRQ#B
PIRQ#A
PGNT#2
PGNT#1
PGNT#0
PCI_RST#
TRDY#
STOP#
SERR#
PAR
M66EN
PCI_PME#
FRAME#
DEVSEL#
PREQ#2
PREQ#1
PREQ#0
PERR#
SB_PME#
E_ASM1083_1.2V
ASM1083_VCC3
EMI
CK_PCI0
PCI_RST#
PLTRST_BU1#
H/W Strapping
PE_EC_SEL
CLK100SEL
ASM_TEST_EN
CLKRUN_EN
I2CCLKSEL
M66EN
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
Power switch of ASM1083
GP16 Default : GPI/VSB
BIOS set it to GPO/OD/H
NS Active : GPO/OD/L
U59
SLG59M1440V_STDFN4-HF
115mA
UP0111AMA5
U23
min 20mil.
Phase out !!
PN change to I31-0111A29-U33 or add AVL ??
MICRO-STAR INT'L CO.,LTD
MS-7817
ASM1083 PCI Bri.
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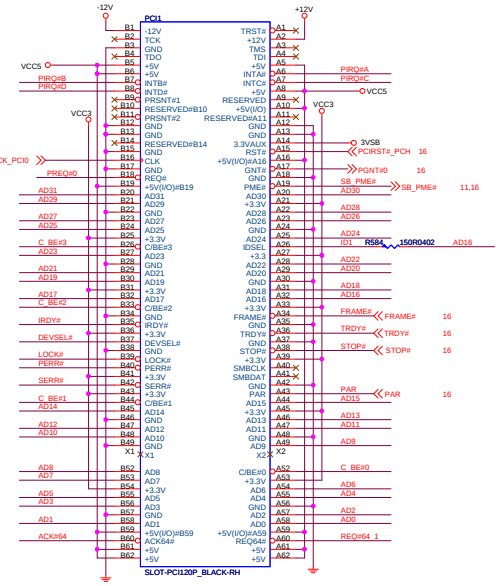
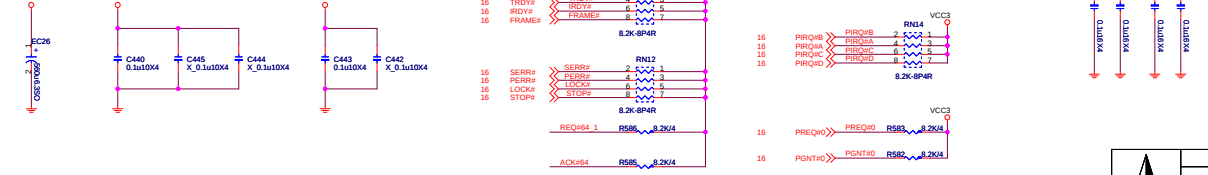


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

AD[31..0] AD[31..0] 16

C_BE#[3..0] C_BE#[3..0] 16

PCI PULL-UP / DOWN RESISTORS



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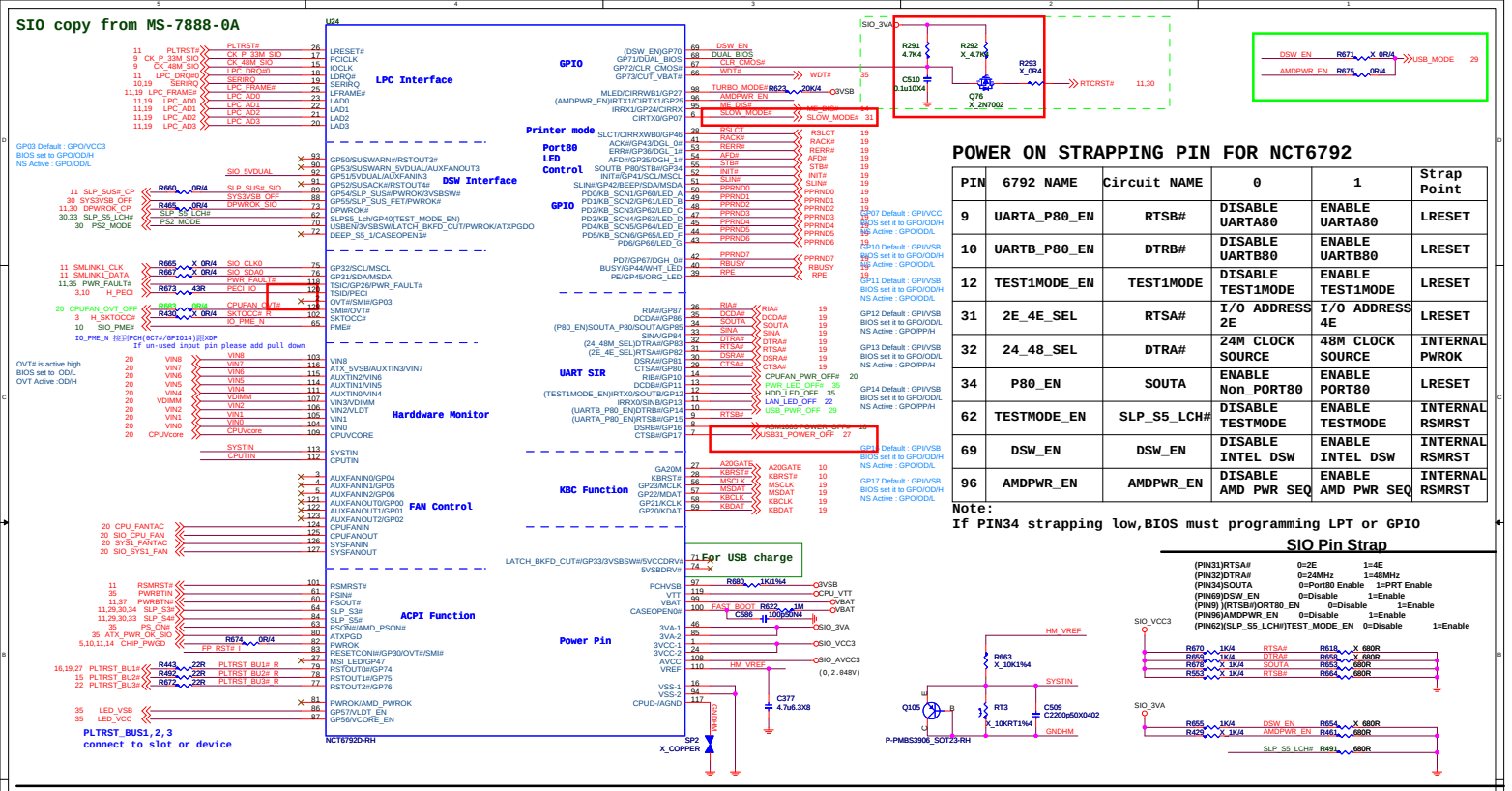

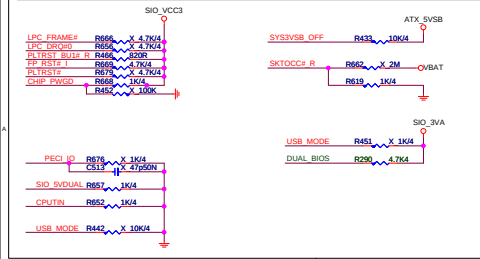

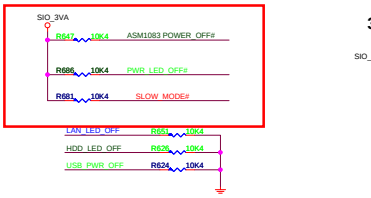

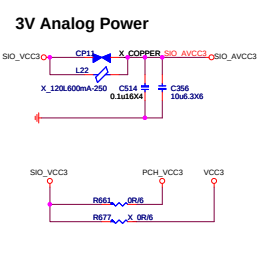

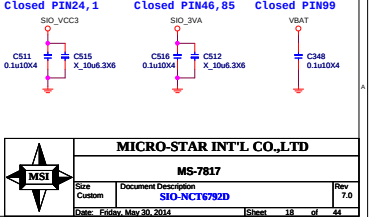

POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))RTSB#)/ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable

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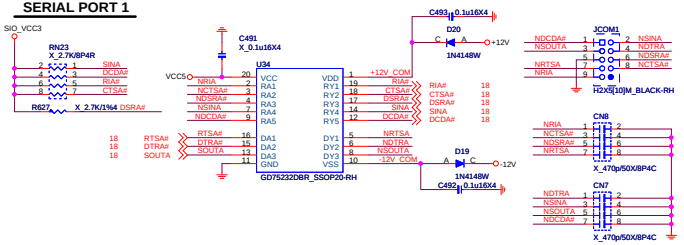
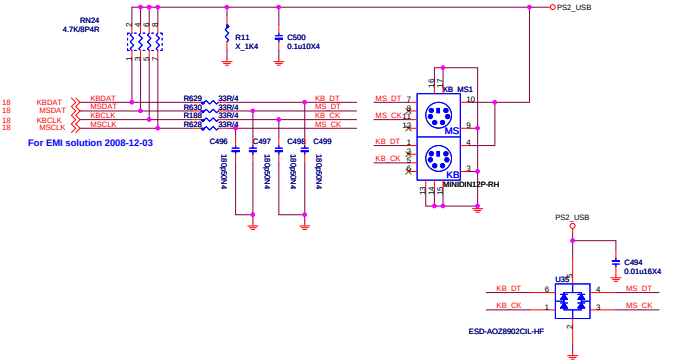
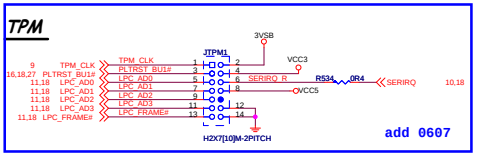
SERIAL PORT 1



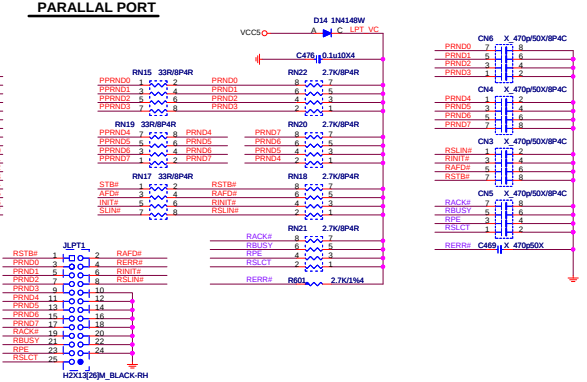
PS2 KEYBOARD & MOUSE CONNECTOR



TPM



PARALLAL PORT



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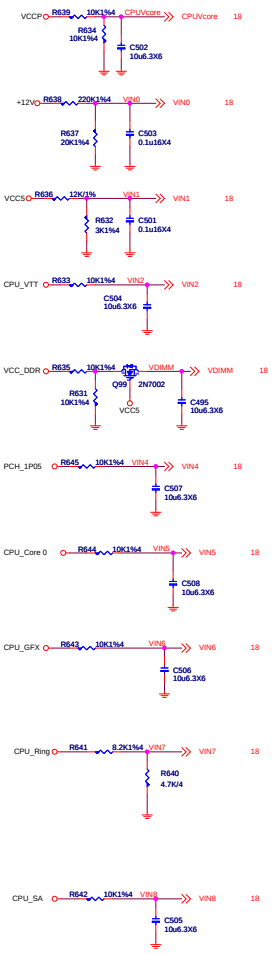
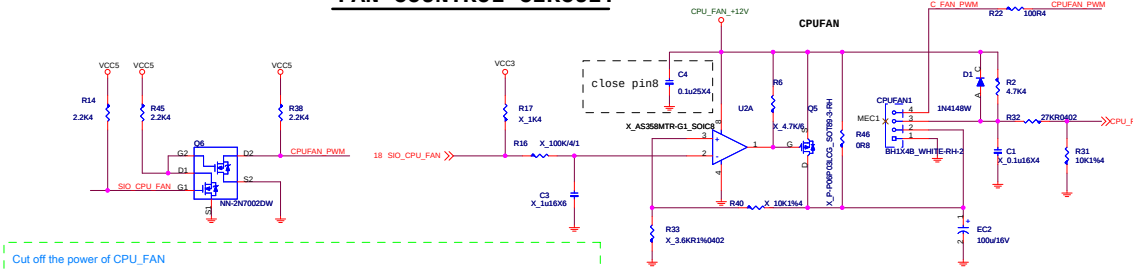
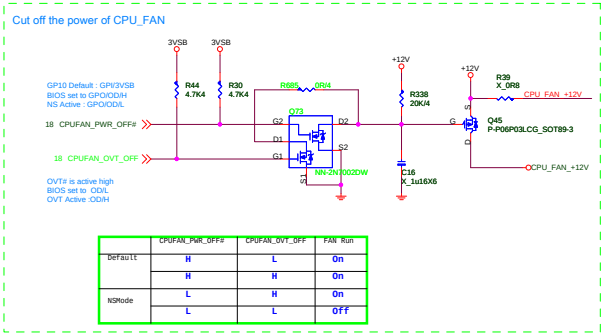
HW Monitor - Voltage

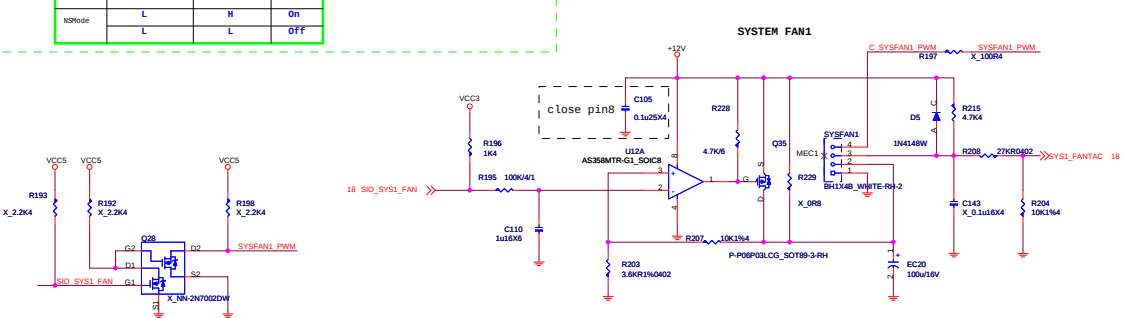


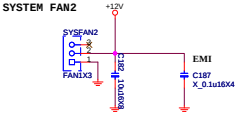
FAN-COUNTROL CIRCUIT





	CPUFAN_PWR_OFF#	CPUFAN_OVT_OFF	FAN Run
Default	H	L	On
	H	H	On
NSMode	L	H	On
	L	L	Off





MSI	MICRO-STAR INT'L CO.,LTD
	MS-7817
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ALC887-VD
VT1708S CE

11mA
Closed Codec
VCC3
CA1 10u6.3X6
CA2 0.1u10X4
Closed Codec
C640 closed PIN25
C651 closed PIN38
VOUT
CA3 0.1u10X4
CA4 22u6.3X8

UA1
EAPD 47
SPDIF-OUT 48
11 AZ_SDOUT → RA6 22R/4 → SDIN0 8
11 AZ_SDIN0
11 AZ_SYNC → SDATA-IN 10
11 AZ_RST# → RESET# 11
11 AZ_BITCLK → RA8 0R4 HDA_BITCLK_R → BCLK 6
X_C10p50N0402 C452
REGREF 2
GPIO0/DMIC-CLK/SPDIF-OUT2 3
X5R CA9 10u6.3X6
SENSE A 13
SENSE B 34
MIC1_V_R 32
MIC2_VREFO 30
MIC1_V_L 28
PIN37-VREFO 29
45.8mA LDOVDD
LINE2_VREFO 31
VREF_AUDIO
VCAP 33
JDREF 40
CA16 X_0.1u16X4
CA18 10u6.3X6
CA17 X_100p50N4
RA13 20K/1%4 12
BEEP
Reserve for 1708
Closed Codec
C647.C649 close to Pin27

EPAD/SPDIF-IN
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
Sense A
Sense B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
Sense C
JDREF
BEEP
DVDD DVDD-IO LDO-OUT1 LDO-OUT2
GPIO1/DMIC-DATA DVSS AVSS1 AVSS2
ALC887-VD2-CG-HF

FRONT-R 36 ← A_LOUT_R ECA62 1u 2 100u/16V → LOUT_R
FRONT-L 35 ← A_LOUT_L ECA61 1u 2 100u/16V → LOUT_L
SURR-R 41
SURR-L 39
CENTER 43
LFE 44
SIDE-R 46
SIDE-L 45
LINE1-R 24 ← A_LINE_IN_R CA7 4.7u6.3X8 → LINE_IN_R
LINE1-L 23 ← A_LINE_IN_L CA8 4.7u6.3X8 → LINE_IN_L
LINE2-R 15 ← A_LINE2_R ECA59 1u 2 100u/16V → LINE2_R
LINE2-L 14 ← A_LINE2_L ECA60 1u 2 100u/16V → LINE2_L
MIC1-R 22 ← A_MIC1_R CA10 4.7u6.3X8 → MIC1_R
MIC1-L 21 ← A_MIC1_L CA11 4.7u6.3X8 → MIC1_L
MIC2-R 17 ← A_MIC2_R CA14 4.7u6.3X8 → MIC2_R
MIC2-L 16 ← A_MIC2_L CA15 4.7u6.3X8 → MIC2_L
CD-R 20
CD-GND 19
CD-L 18
X5R

EL 100u (C94-1012511-N07)

EMI
CA21 X_0.1u16X4
CA22 X_1000p16X
CA34 X_0.1u16X4

CPA1 X_COPPER
CPA2 X_COPPER

100pF Cap can change to TVS by PM request.

LIN_OUT
LOUT_R RA1 75R → LOUT_RA
LOUT_L RA2 75R → LOUT_LA
FRONT_JD
AUDIO1B
JACK-AUDIOX3F_PK/GR/BU-RH-6
LOUT_LA CA5 100p50N4
LOUT_RA CA6 100p50N4
LOUT_LA RA3 22K
LOUT_RA RA4 22K

LIN_IN
LINE_IN_R RA5 75R → LINE_IN_RA
LINE_IN_L RA7 75R → LINE_IN_LA
LINE1_JD
AUDIO1A
JACK-AUDIOX3F_PK/GR/BU-RH-6
LINE_IN_LA CA32 100p50N4
LINE_IN_RA CA33 100p50N4

MIC1
MIC1_V_L RA9 2.2K4 → MIC1_LA
MIC1_V_R RA10 2.2K4 → MIC1_RA
MIC1_R RA11 75R → MIC1_RA
MIC1_L RA12 75R → MIC1_LA
MIC1_JD
AUDIO1C
JACK-AUDIOX3F_PK/GR/BU-RH-6
MIC1_RA CA12 100p50N4
MIC1_LA CA13 100p50N4

ATX_5VSB
LA2 0R8 → LDOVDD
DA3 X_TVS
CA24 PXDT10
CA25 10u6.3X6
C659,C669 close to L35

D LIN_IN
E LIN_OUT
F MIC1
N54-13F8271-K56

VCAP
CA19 X_0.1u16X4
CA20 X_10u6.3X6
887:Remove
1708:Stuff
Closed Codec

SENSE_A
RA16 5.1K/1%
RA17 10K1%4
RA18 20K/1%4
FRONT_JD
LINE1_JD
MIC1_JD
CA23 X_100p50N4

Closed Codec
SENSE_B
CA26 100p50N4

Rear Line OUT De-POP circuit
20140217

3VSB
VCC3
RA37 10K/4
RA45 0R/4
RA42 10K/4
RA41 220K
CA36 0.1u10X4
CA37 22u6.3X8
QA3 P-MMBT3906
QA4 P-MMBT3906
QA5 P-MMBT3906
MUTE
EAPD RA38 1K/4 EAPD_R

Digital
Analog

QA2
MUTE RA39 1K/4 LOUT_LA
RA44 1K/4 LOUT_RA
NN-HBN2515S6R

QA1
MUTE RA43 1K/4 F_LINE2_R
RA40 1K/4 F_LINE2_L
NN-HBN2515S6R

DA1
LINE2_VREFO
S-BAT54A_SOT23
MIC2_VREFO
S-BAT54A_SOT23
DA2
RNA1 4.7K/8P4R

RNA2 75R/8P4R
MIC2_R F_MIC2_R
MIC2_L F_MIC2_L
LINE2_L F_LINE2_L
LINE2_R F_LINE2_R
F_LINE2_L RA14 22K
F_LINE2_R RA15 22K
Reserved for Front Panel

N31-2051411-H06
JAUD1
MIC GND
MICPWR PRESENCE#
FLINE OUTR LINE NEXT R
HPON
FLINE OUTL LINE NEXT L
H2X5(8)M_BLACK-RH
F_MIC2_L
F_MIC2_R
F_LINE2_R
SENSE_B
F_LINE2_L
MIC2_JD
LINE2_JD
RA15 47R
CA27 100p50N4
CA28 100p50N4
CA29 100p50N4
CA30 1000p16X
RA20 39.2K/1%
RA21 20K/1%4
Close to Jack
Varister --> cap for cost down
Close to Front panel
For HDA/AC97 front cable.

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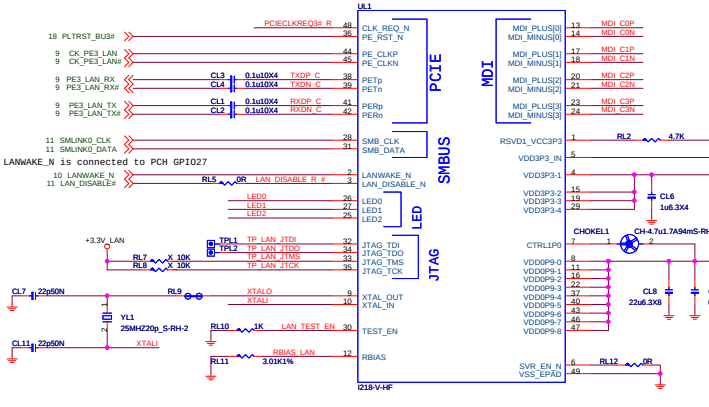
Intel Clvrkville I217V / I218V PHY

LAN copy from MS-7914-0A

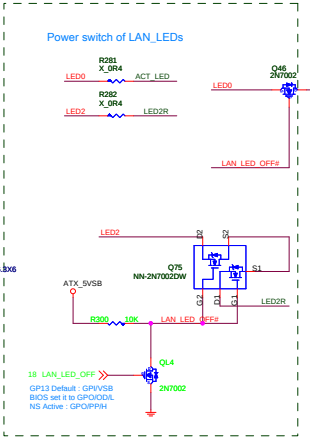


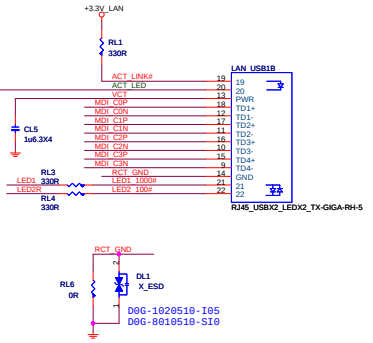
PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is left as NC

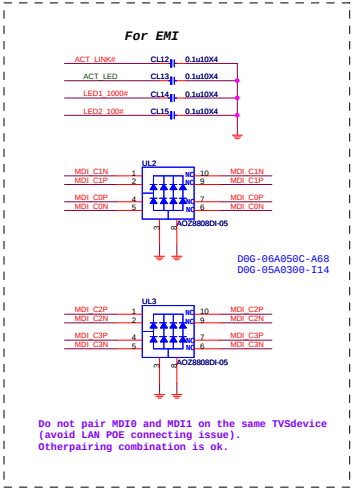
The 10Kohm pull-up resistor of CLK_REQ_N
is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well
of PCH's input PCIECLKRQ<n> buffer.

SMBUS PULL-UP OPTIONS
SMBUS SPEED
1MHz (Defaul setting) 499 ohm
100KHz/400KHz 2.2K ohm

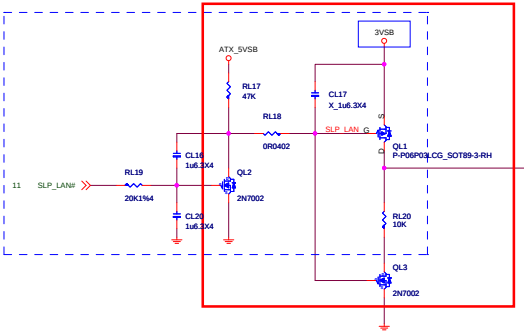
Remove pull-up R if R existence on motherboard
(or PCH has internal pull-up R).







support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218.
NOT support WOL from Deep Sx:
Power source from 3VSB



+3.3V_LAN
132mA

Note:These caps closed to PHY

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HDMI level shifter

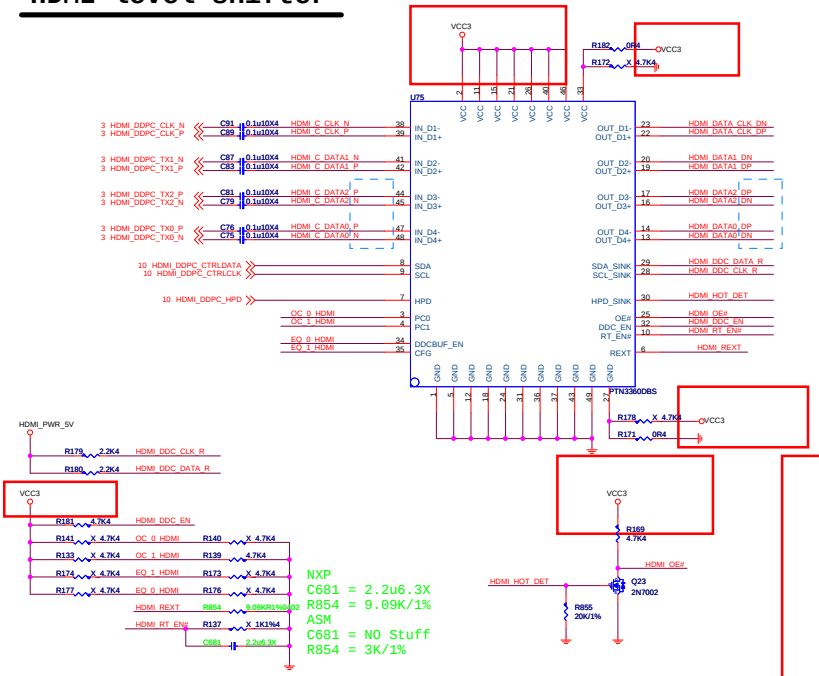
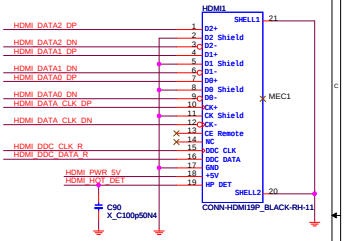
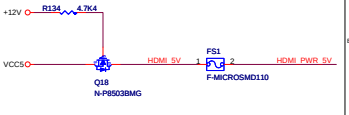


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	



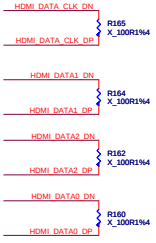


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

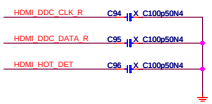
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

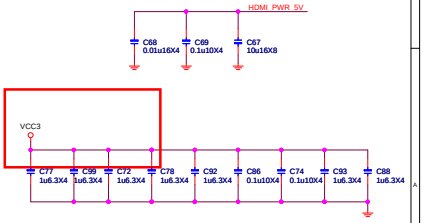
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

EMI



EMI cap.





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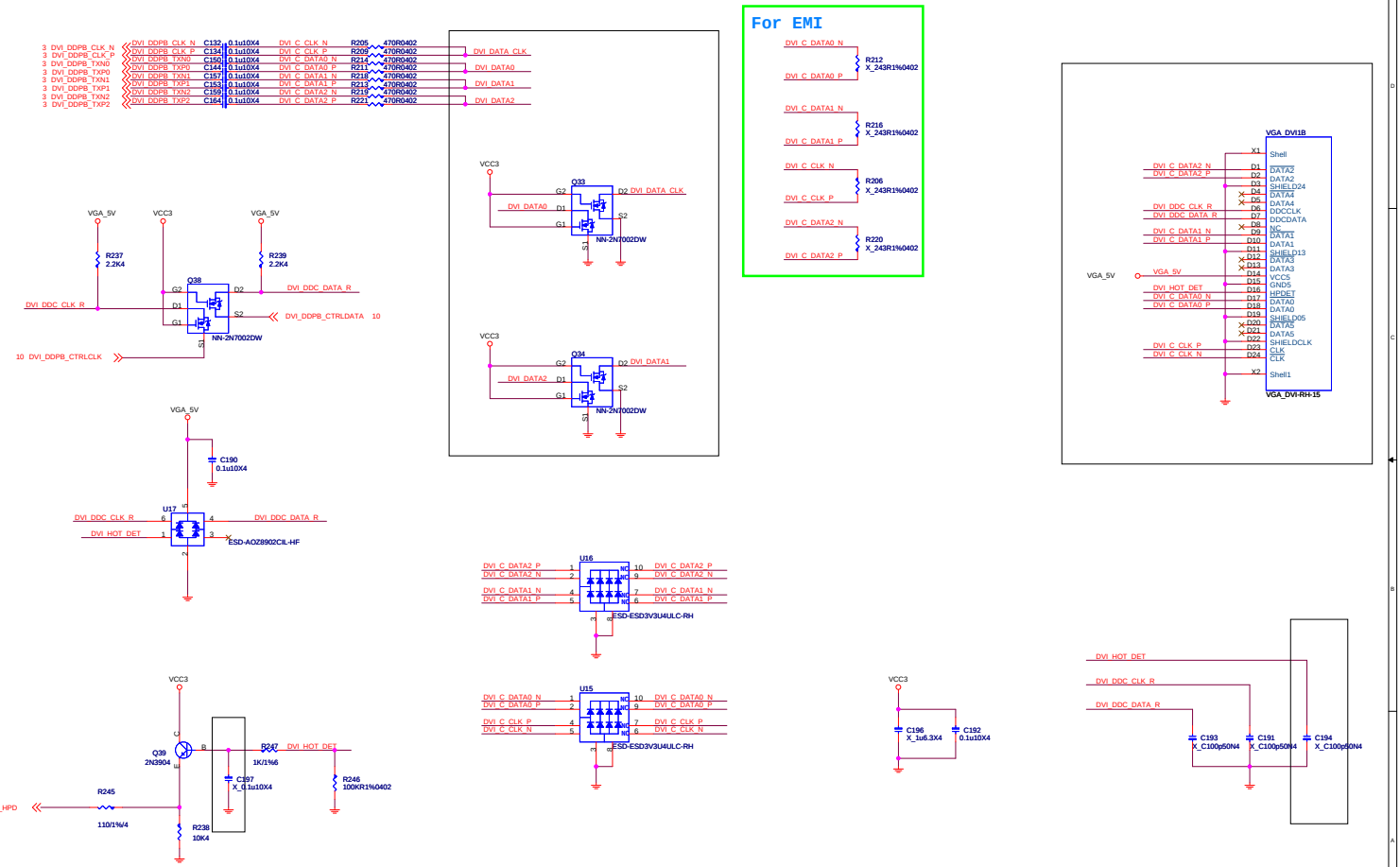
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



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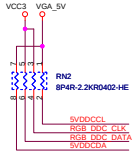
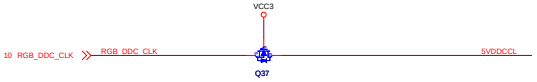
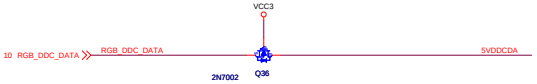
D-Sub

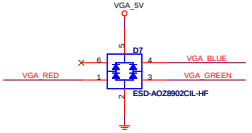
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

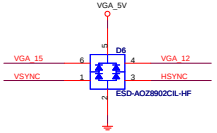
Level shift

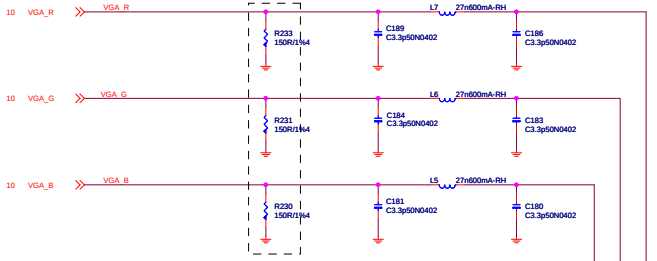


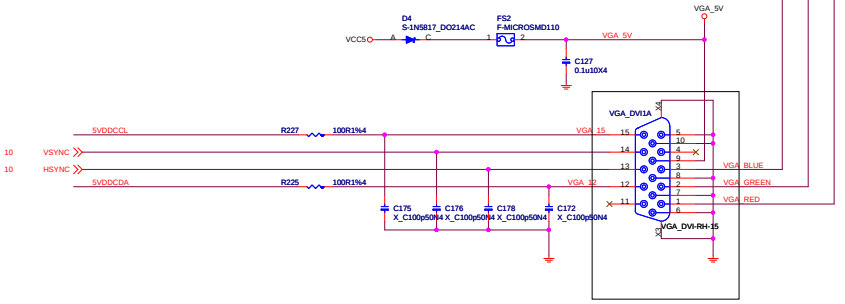












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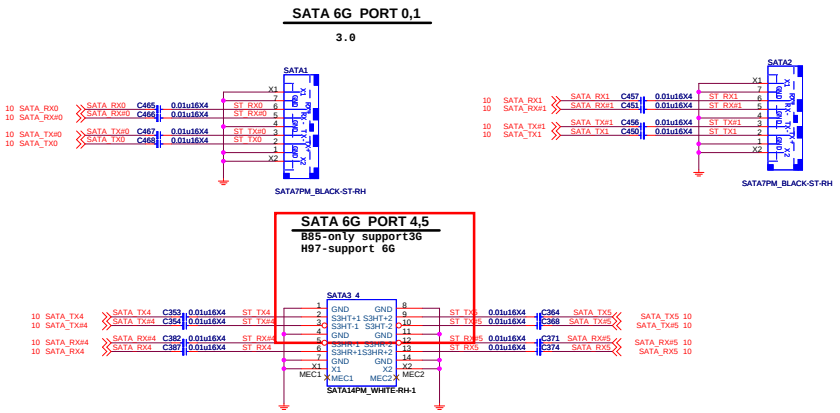
SATA Connector



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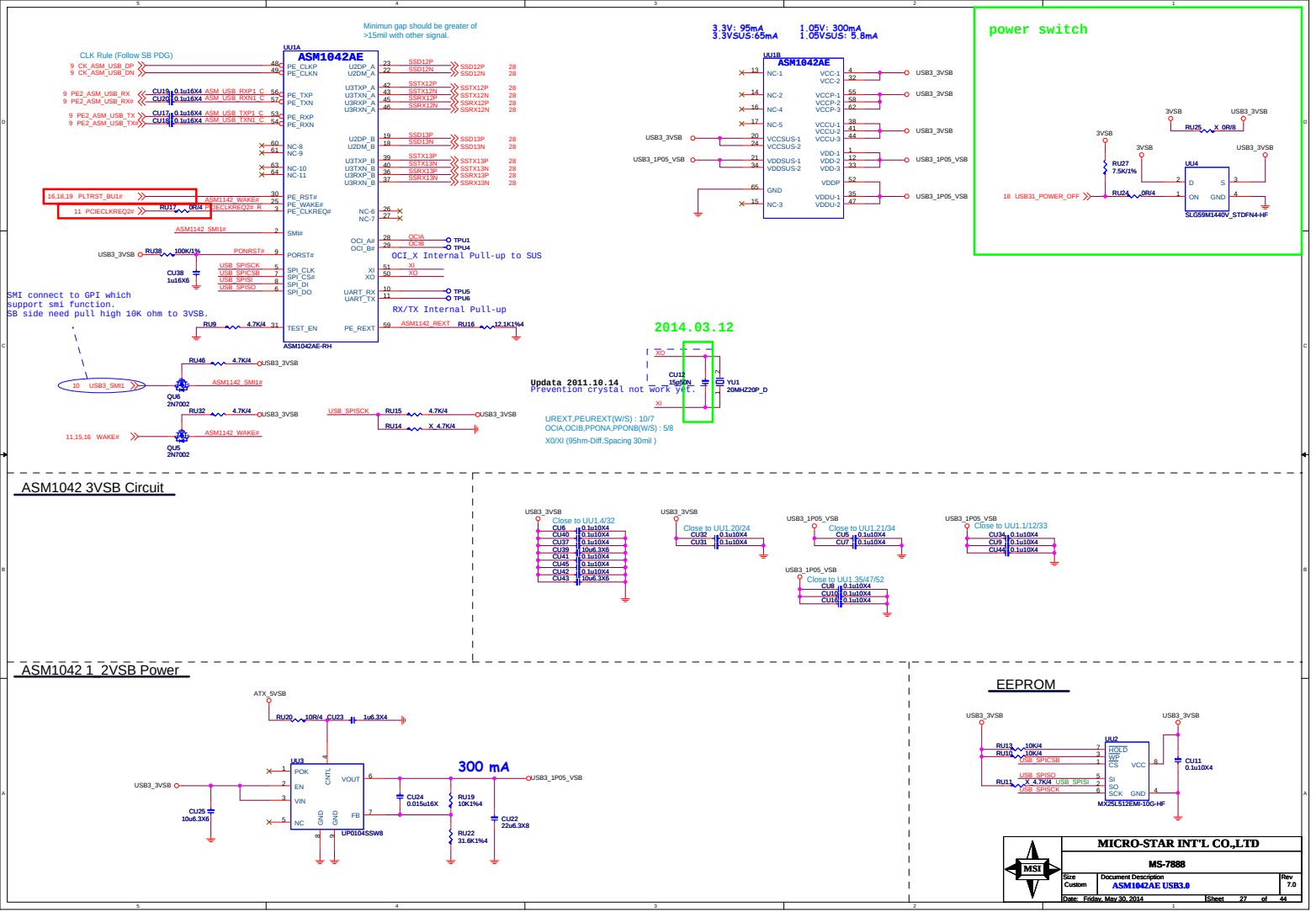
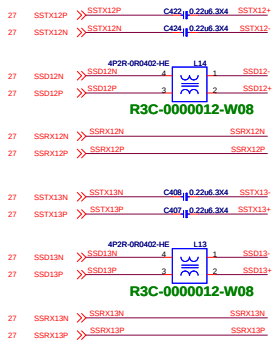
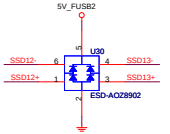
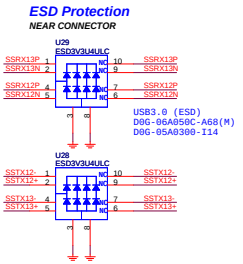
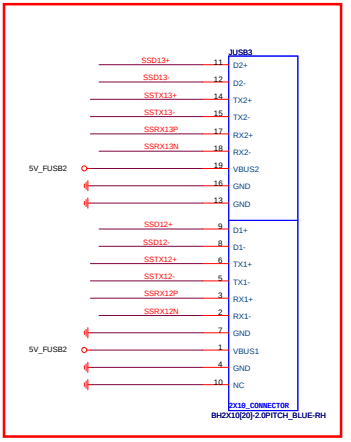

Minimum gap should be greater of
>15mil with other signal.
3.3V: 95mA
3.3VSUS:65mA
1.05V: 300mA
1.05VSUS: 5.8mA
power switch
CLK Rule (Follow SB PDG)
UU1A
ASM1042AE
UU1B
ASM1042AE
SLG59M1440V_STDFN4-HF
OCI_X Internal Pull-up to SUS
RX/TX Internal Pull-up
SMI connect to GPI which
support smi function.
SB side need pull high 10K ohm to 3VSB.
ASM1042AE-RH
2014.03.12
Updata 2011.10.12
Prevention crystal not work yet.
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8
X0/XI (95hm-Diff,Spacing 30mil)
ASM1042 3VSB Circuit
ASM1042 1_2VSB Power
EEPROM
MX25L512EMI-10G-HF
MICRO-STAR INT'L CO.,LTD
MS-7888
ASM1042AE USB3.0
Friday, May 30, 2014

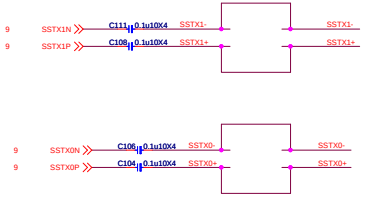
USB3.0 Connector

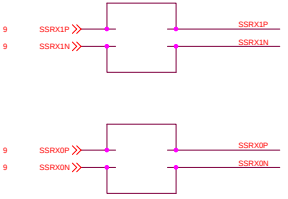


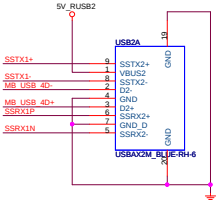


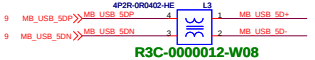


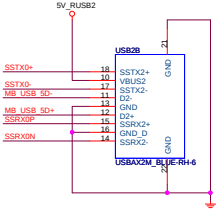




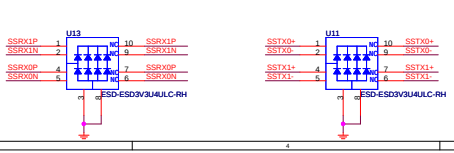








EMI



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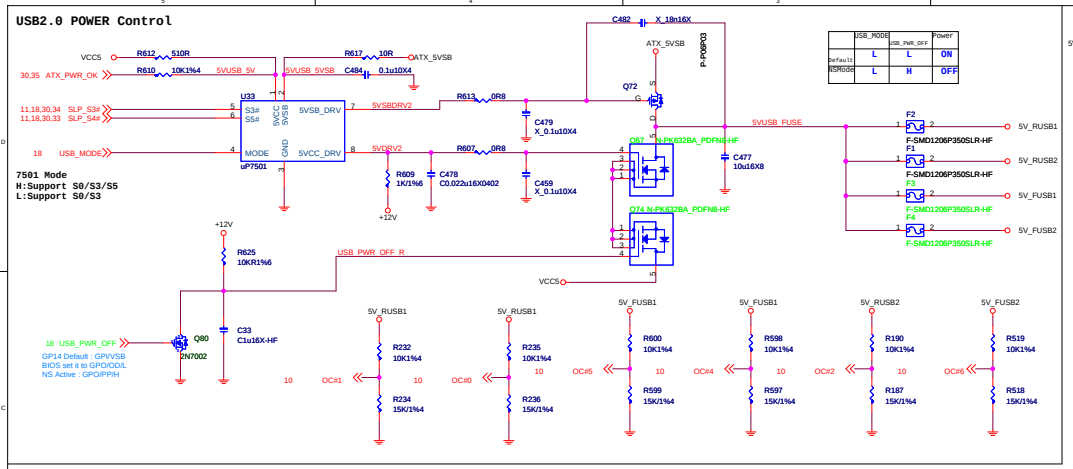
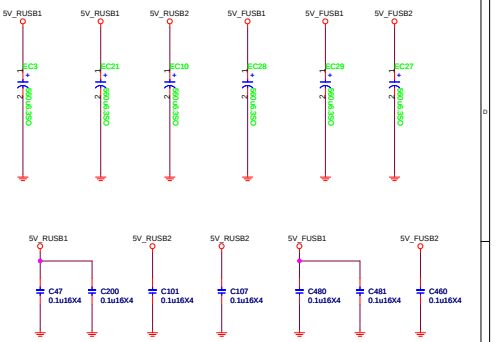
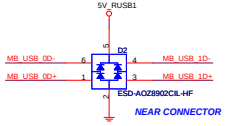
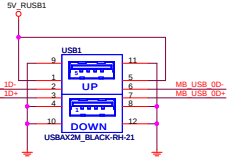


USB_MODE	USB_PWR_OFF	Power
Default	L	L	ON
MSMode	L	H	OFF

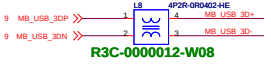


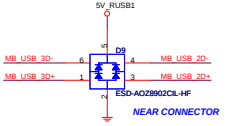
REAR USB PORT0,1

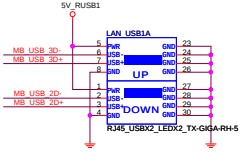




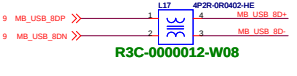
REAR USB PORT2,3(With Lan)

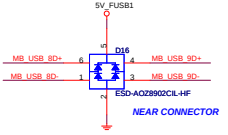


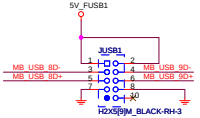




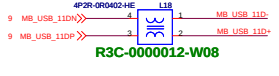
FRONT USB PORT8,9

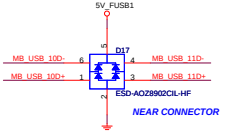


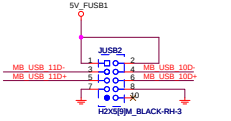




FRONT USB PORT 10,11







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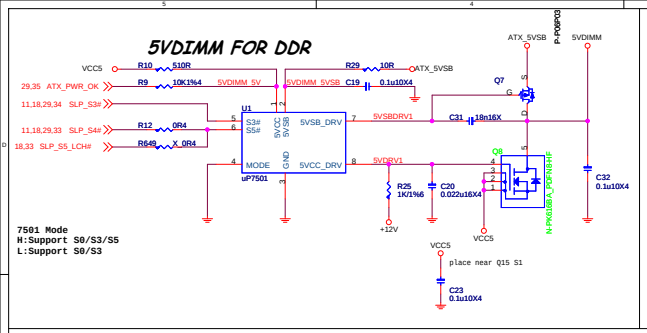

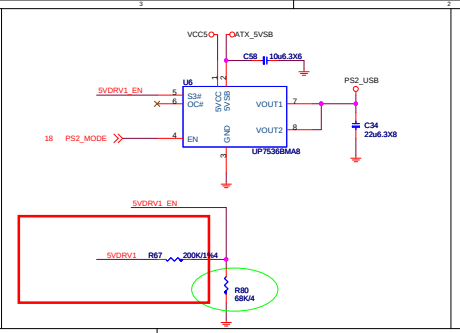

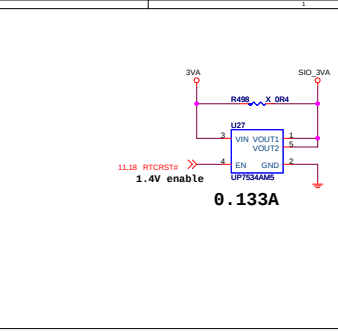

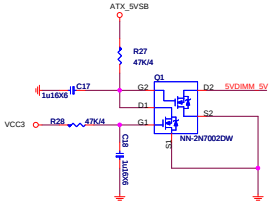

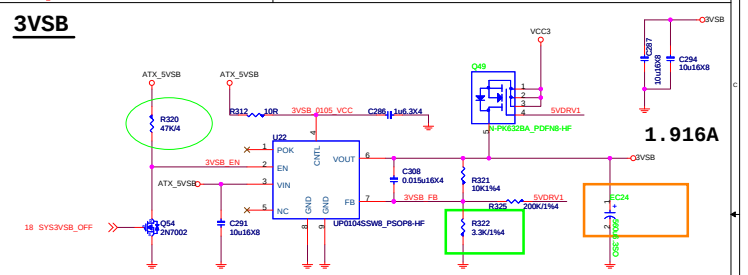

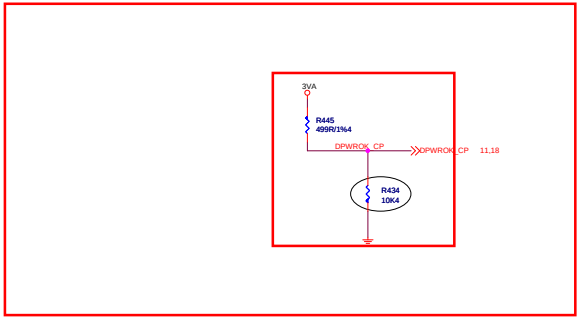

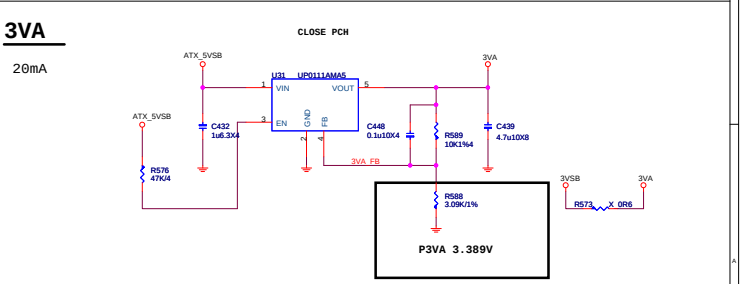

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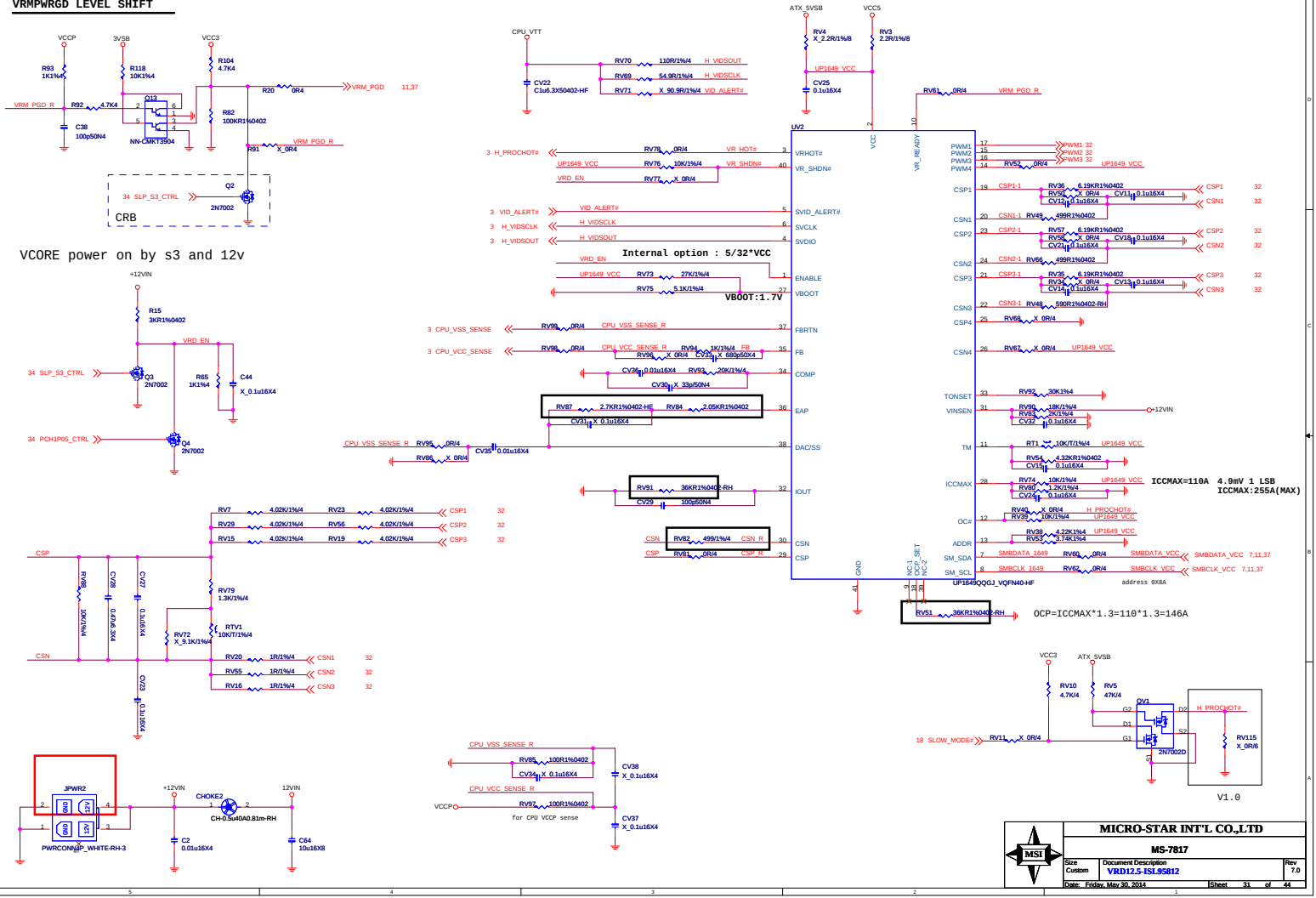
VRMPWRGD LEVEL SHIFT



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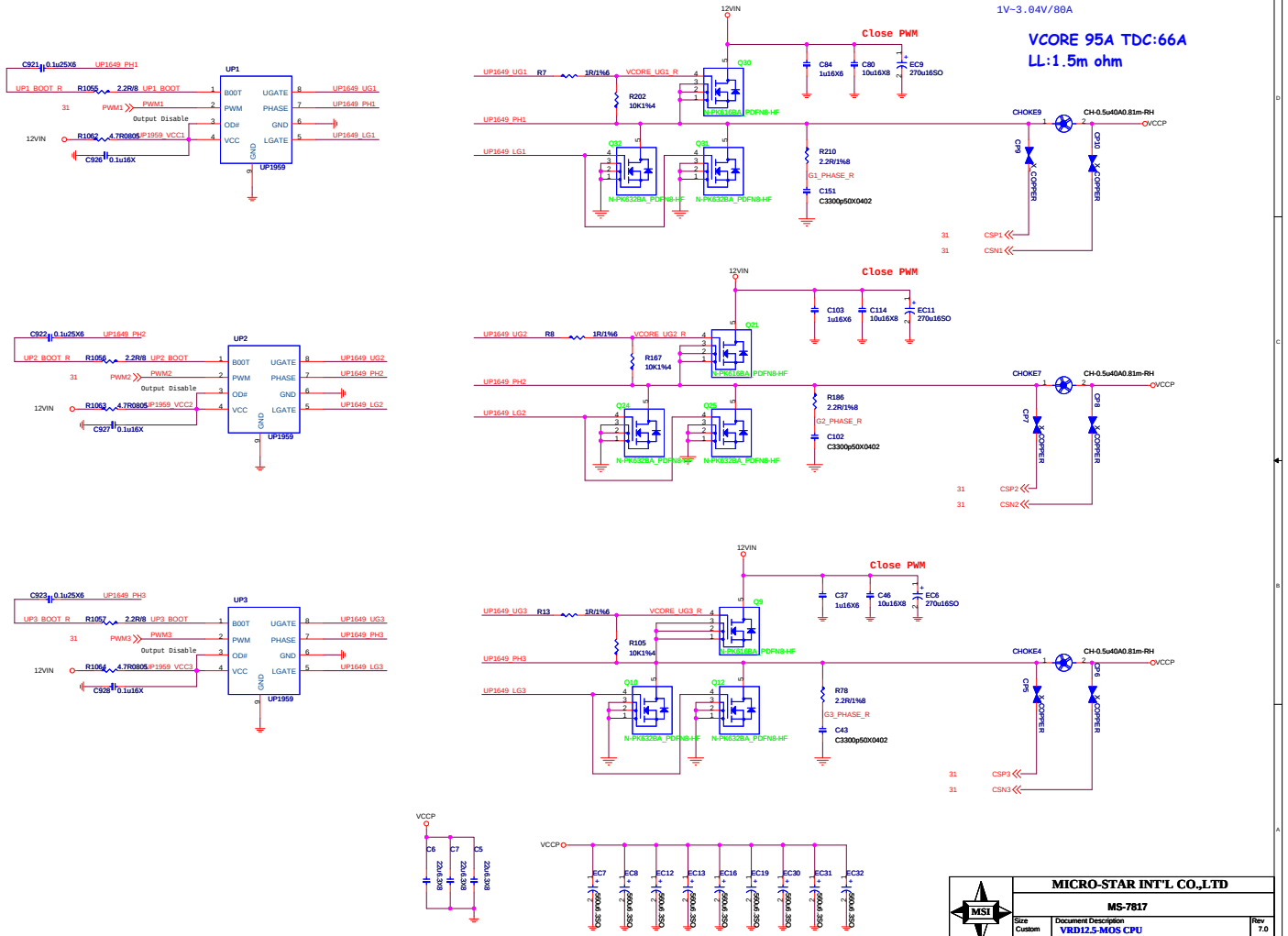
1V~3.04V/80A
VCORE 95A TDC:66A
LL:1.5m ohm
Close PWM
12VIN
UP1
UP2
UP3
UP1649_PH1
UP1649_PH2
UP1649_PH3
UP1649_UG1
UP1649_UG2
UP1649_UG3
UP1649_LG1
UP1649_LG2
UP1649_LG3
UP1_BOOT_R
UP2_BOOT_R
UP3_BOOT_R
UP1_BOOT
UP2_BOOT
UP3_BOOT
PWM1
PWM2
PWM3
Output Disable
VCC_UG1_R
VCC_UG2_R
VCC_UG3_R
G1_PHASE_R
G2_PHASE_R
G3_PHASE_R
N-PK616BA_PDFN8-HF
N-PK632BA_PDFN8-HF
CHOKE9
CHOKE7
CHOKE4
CH-0.5u40A0.81m-RH
COPPER
VCCP
CSP1
CSN1
CSP2
CSN2
CSP3
CSN3
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VRD12.5-MOS CPU
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DDR Power:1.5V

DDR3_1.5V ICCMAX 23.6A

4.5A FOR CPU

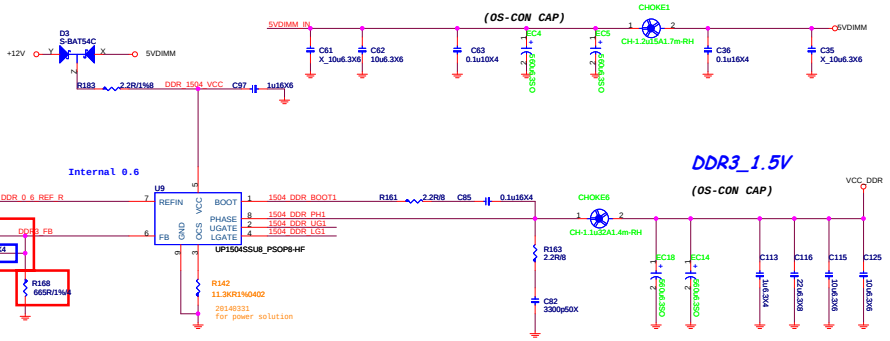
12A FOR 4DIMM

1.1A FOR DDR VTT

6A FOR PCH_1P05

Iripple=9.6

4.7*2*1=9.4A<9.6A

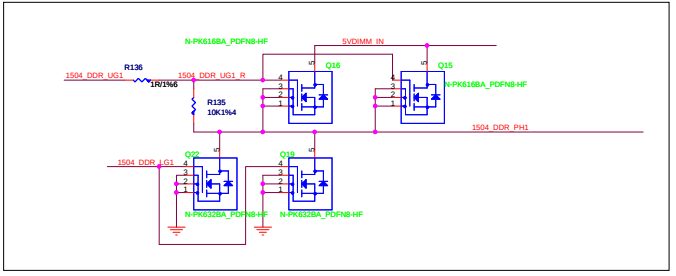


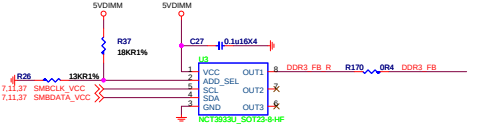
OCP 23.6*1.5=35A

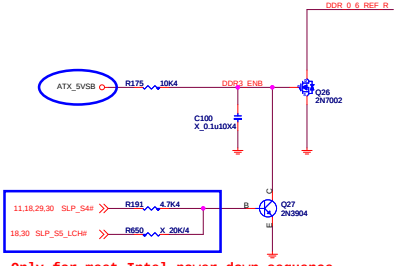
35A=(20uA*Rocs(R142))/4*Rdson(Low side1.65mohm)

R142=11.9K ohm

((R221/R226)+1)*0.6=1.5V



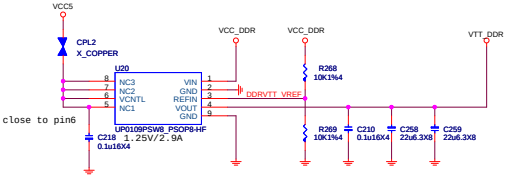




P.S. Only for meet Intel power down sequence.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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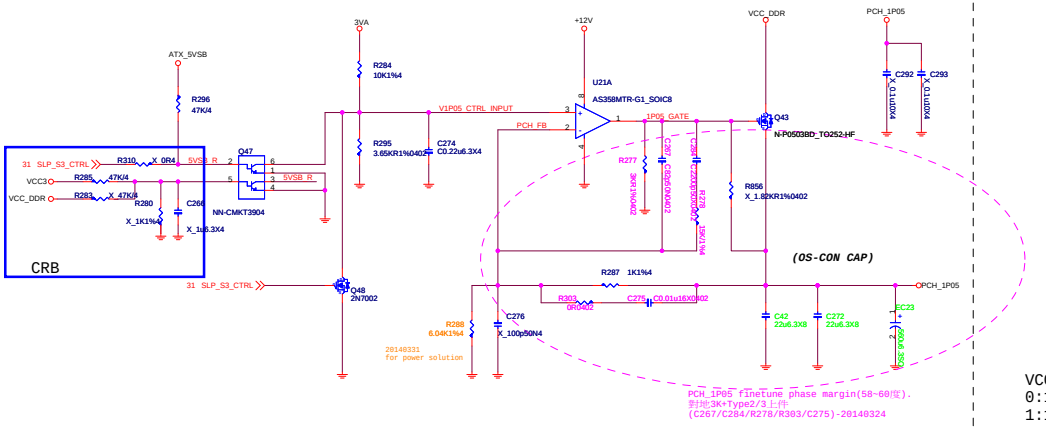
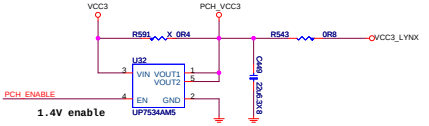
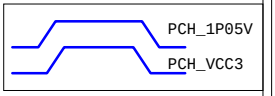
PCH Power:1.05V 5.747A



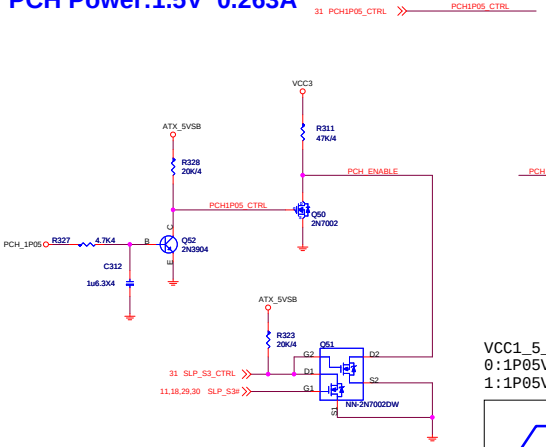
0.133A

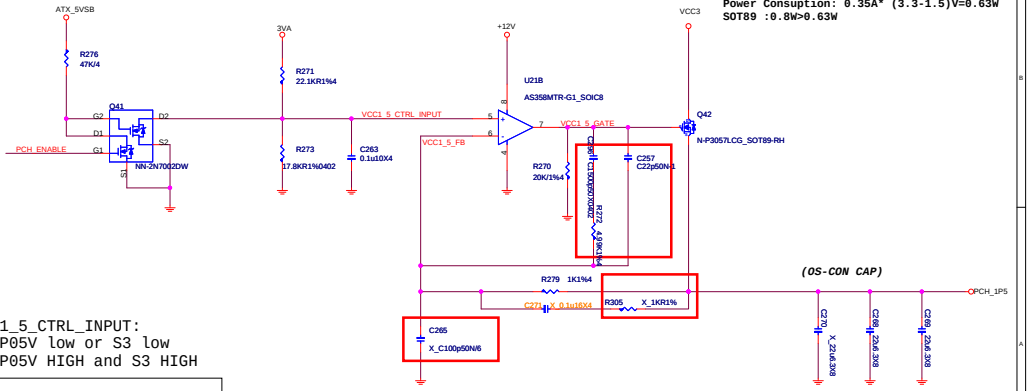


VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

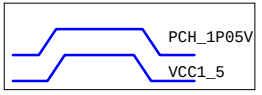


PCH Power:1.5V 0.263A





VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



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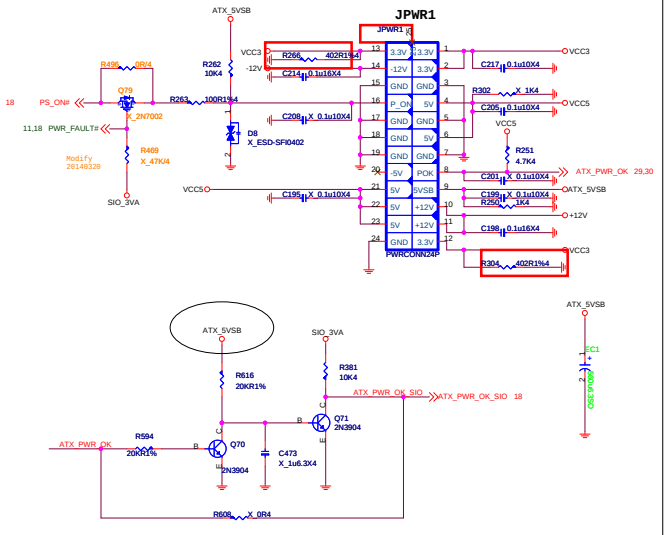
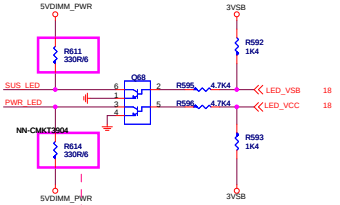
ATX POWER CONNECTOR

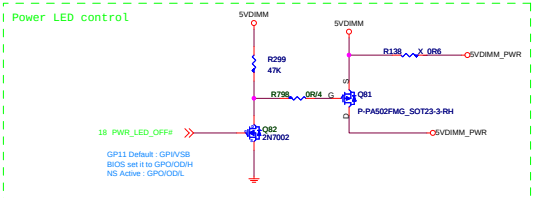


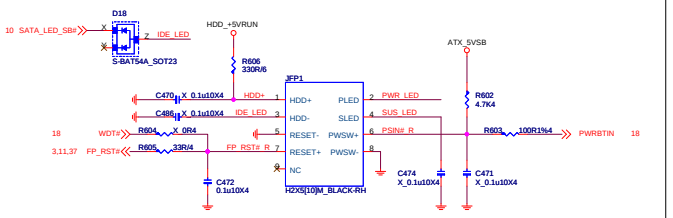
LED (for Fintek 71869)

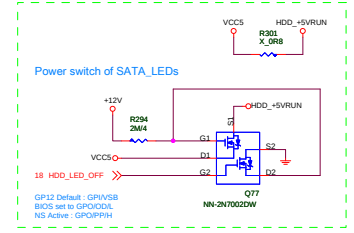


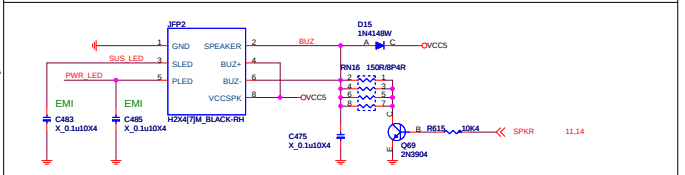
Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.

Power LED control









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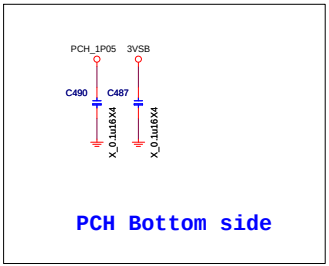

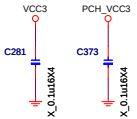

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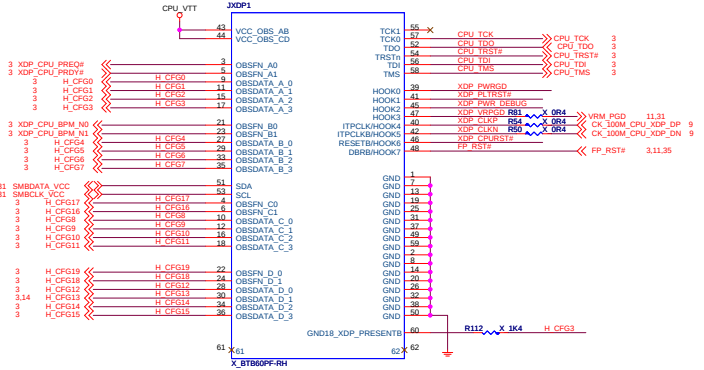
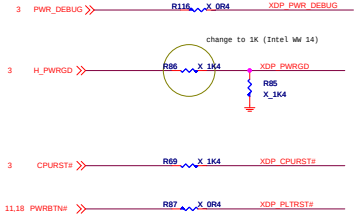
Reserve debug port 5020





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Voltage test point

CPU_H1

CPU_H1

HS_PCH1

MEC1

MEC2

MEC2

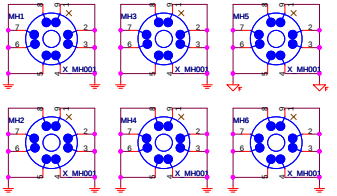
HS-0407170-RH

PCB1

7817-71

PK0-B781770-G37,精成,23,寶安恩斯福廠(MSIS)-COFFEE
PK0-B781770-E48,錫華,23,寶安恩斯福廠(MSIS)-COFFEE

Mounting Holes



VCCP
CPU_VTT
VCC_DDR
VTT_DDR
PCH_1P05
PCH_1P5
5VDIMM
+12V
VCC5
VCC3
ATX_5VSB
3VSB
VBAT
3VA
VCCIOA

VCCP
CPUIO
VCC_DDR
VTT_DDR
PCH_1P05
PCH_1P5
5VDIMM
+12V
VCC5
VCC3
ATX_5VSB
3VSB
VBAT
3VA
VCCIOA

LABEL1

AMI_BIOS LABLE

BIOS_LABLE

LABEL2

Label
601-7798-XXX

MKT-LABEL

BAT1_X1

BAT-BCR2032P-RH

HDMI VIRTUAL PN

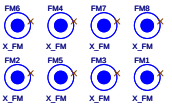
HDMI_RYT1

HDMI Logo

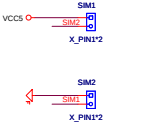
0.04 PER UNIT

Y01-RHDMI03-000

Optical Fiducial Marks-120



Simulation



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