# Thor-P (T15p/P15v) Schematic Page Number



## *Thor Tp / Thor Pv - 12L*

**Project Code: GT5A0 / GP5A0**
**12L NM-C641 Rev : 1.0**
**NV N19M-Q3/N17P-G0-K1**



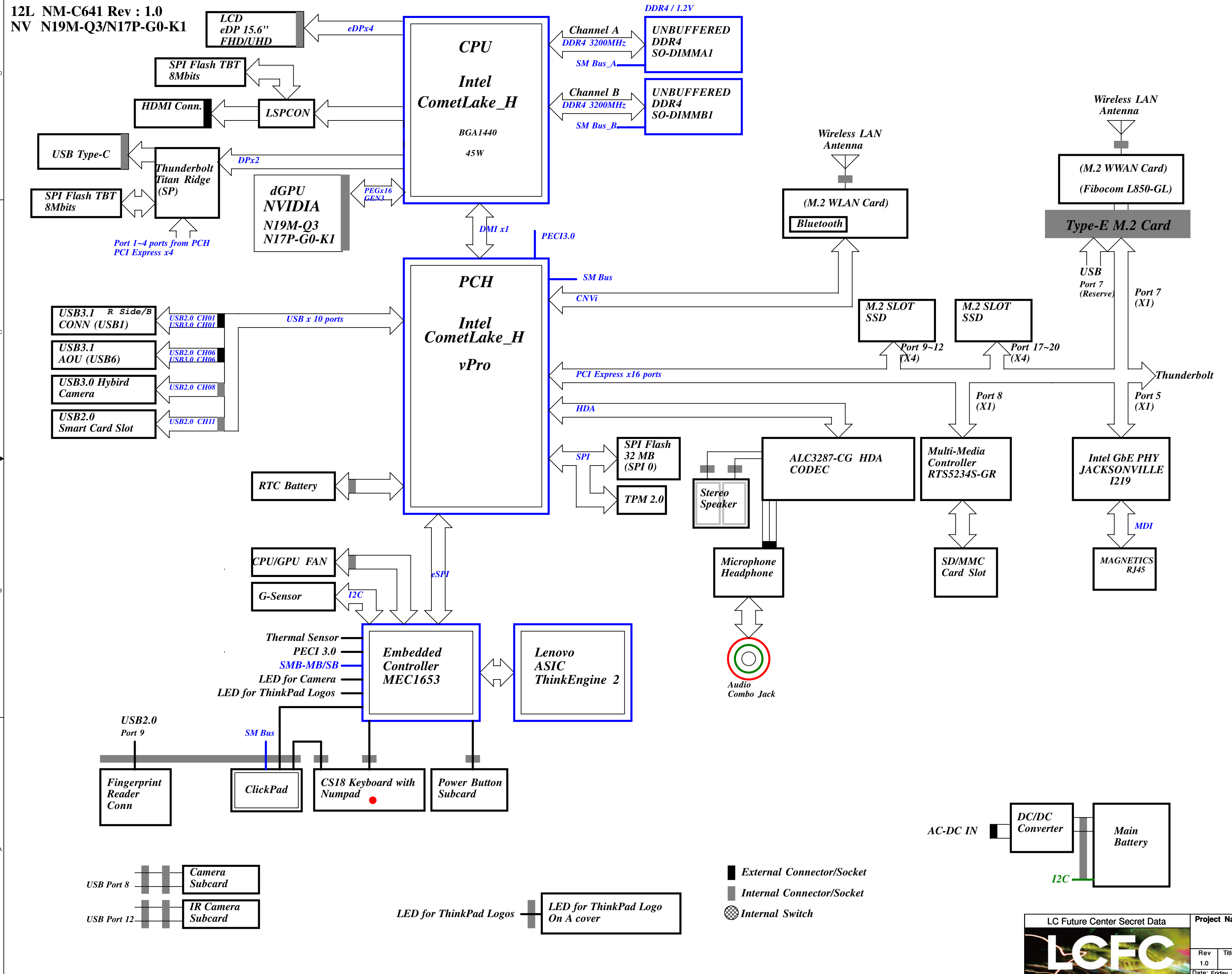
| Project Name | |
|---|---|
| *TpPv* | |
| Rev 1.0 | Title: **TITLE PAGE** |
| Date: Friday, May 15, 2020 | Sheet 1 of 133 |

# Thor-P Block Diagram

**Project Code: GT5A0 / GP5A0**

**12L NM-C641 Rev : 1.0**

**NV N19M-Q3/N17P-G0-K1**




| PCB Layer Stackup |
|---|
| L1:TOP |
| L2:GND1 |
| L3:Signal 1 |
| L4:GND 2 |
| L5:Signal 2 |
| L6:GND3 |
| L7:VCC1 |
| L8:Signal 3 |
| L9:VCC2 |
| L10:Signal 4 |
| L11:GND4 |
| L12:BOTTOM |

| INPUTS | OUTPUTS |
|---|---|
| **Battery Charger** BQ24780SRUYR | |
| BAT-PWR12 | M-BAT-PWR |
| **System DC/DC** TPS51285B-1RUKR | |
| VINT20 | VCC5M VCC3M |
| **CPU DC/DC** M: NCP81215MNTXG S: NCP302045MNTWG | |
| VINT20 | VCCCPUCORE VCCGFXCORE_I VCCSA |
| **VCCCPUIO** NB694GD-Z | |
| VINT20 | VCCCPUIO |
| **VCC1R05_SUS** NB693GQ-Z | |
| VCC5M | VCC1R0_SUS |
| **VCC1R2A/VCC0R6B** TPS51716RUKR | |
| VINT20 | VCC0R6B VCC1R2A |
| **VCC1R8_SUS** NB694GD-Z | |
| VCC5M | VCC1R8_SUS |
| **VCC2R5A** NB695GD-Z | |
| VCC5M | VCC2R5A |
| **GFXCORE_D** NCP81276MNTXG | |
| VINT20 | VCCGFXCORE_D |
| **VCC1R35VIDEO** TPS51219RTER | |
| VCC5M | VCC1R35VIDEO |
| **VCC1R0VIDEO** NB695GD-Z | |
| VCC5M | VCC1R0VIDEO |

## EC SMBus1 address

| Device | Address |
|---|---|
| G-Senor (BMA255) | 0011 000Xb |
| G-Senor (KX022-1020) | 0011 110Xb |

## EC SMBus2 address

| Device | Address |
|---|---|
| Smart Battery | 0001 0110 b |
| Charge Controller | 0001 0010 b |

## EC SMBus3 address

| Device | Address |
|---|---|
| PCH | 0x96h |
| USB Re-driver | 0x20h / 0x21h (Reserved) |
| USB Re-driver (AOU) | 0x52h / 0x53h (Reserved) |

## EC SMBus4 address

| Device | Address |
|---|---|
| DGPU | 0x9Eh |

## EC SMBus3 address

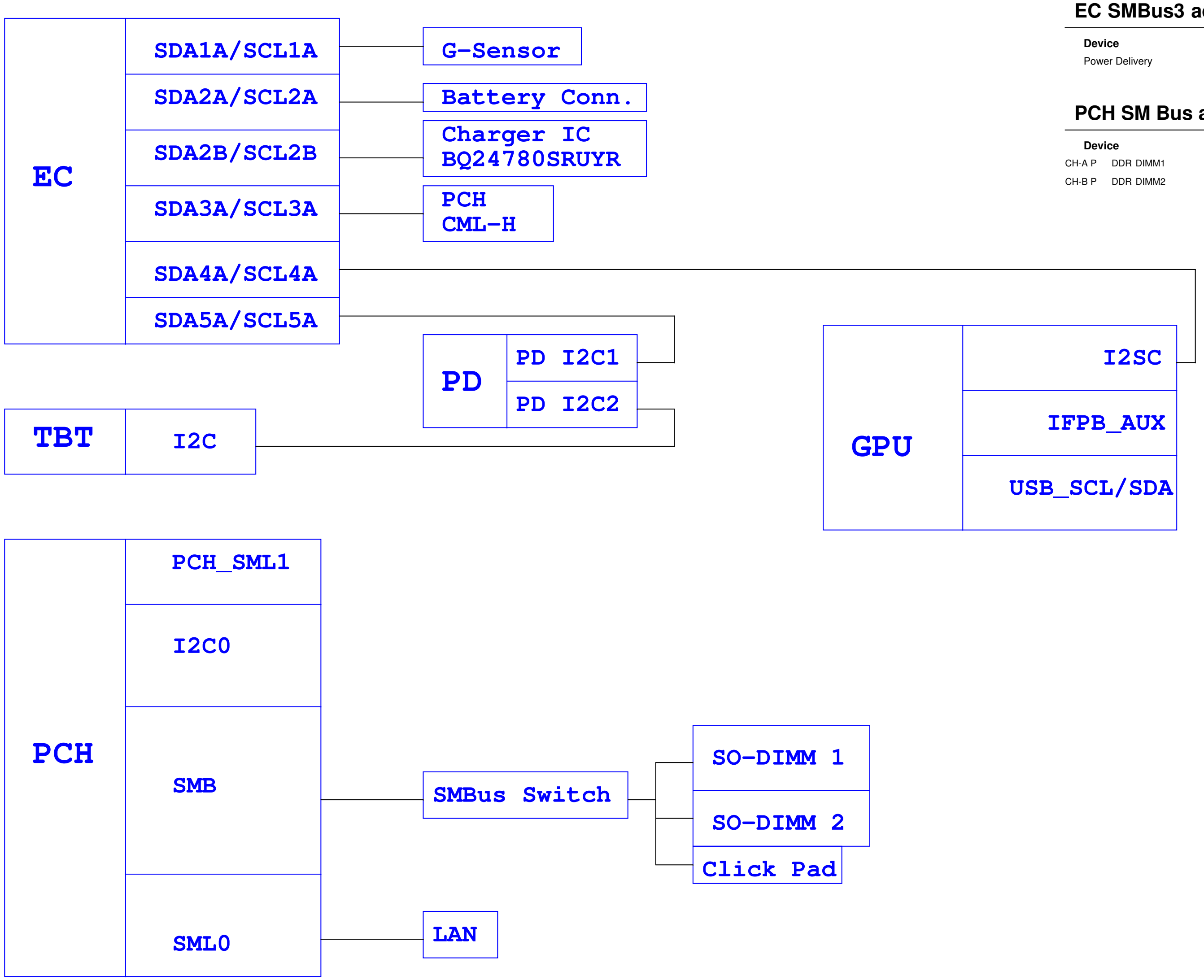
| Device | Address |
|---|---|
| Power Delivery | 01001 xxxxb |

## PCH SM Bus address

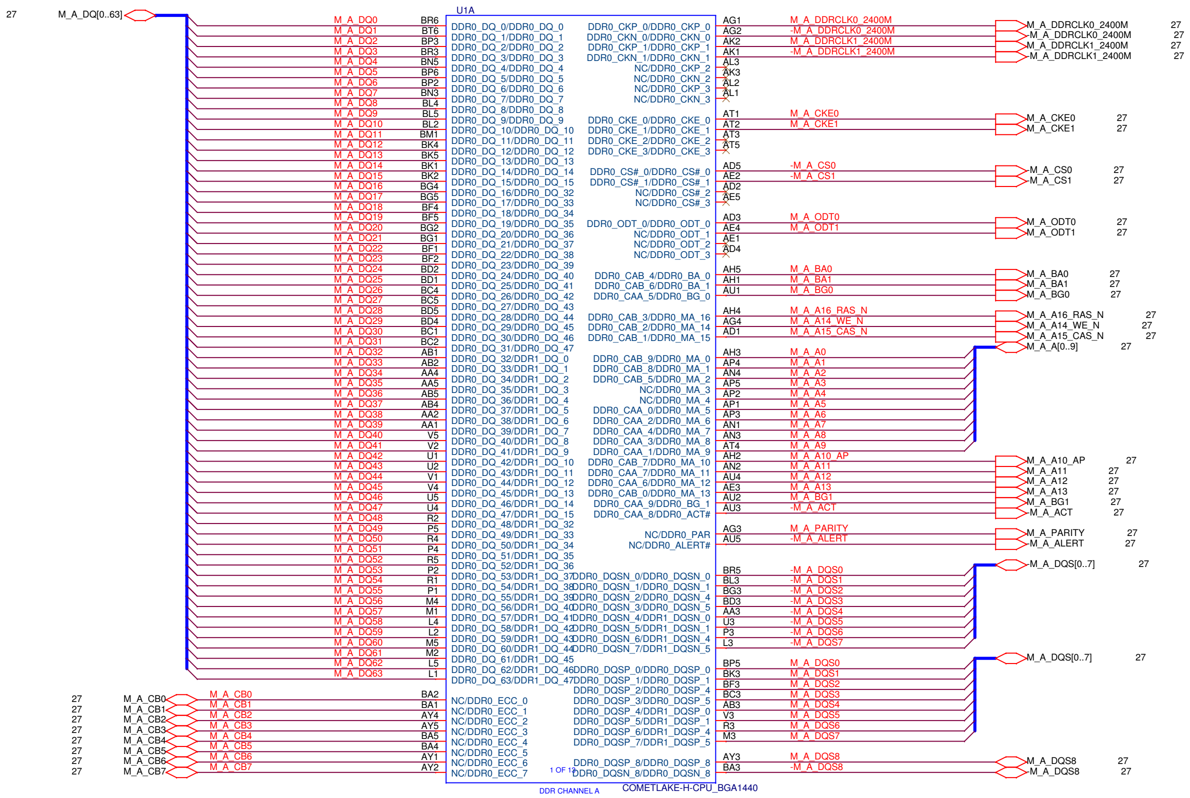
| | Device | Address |
|---|---|---|
| CH-A P | DDR DIMM1 | 0xA0h |
| CH-B P | DDR DIMM2 | 0xA4h |

## PCH SM Bus0 address

| Device | Address |
|---|---|
| Intel Lan_I219 | 0XC8h |



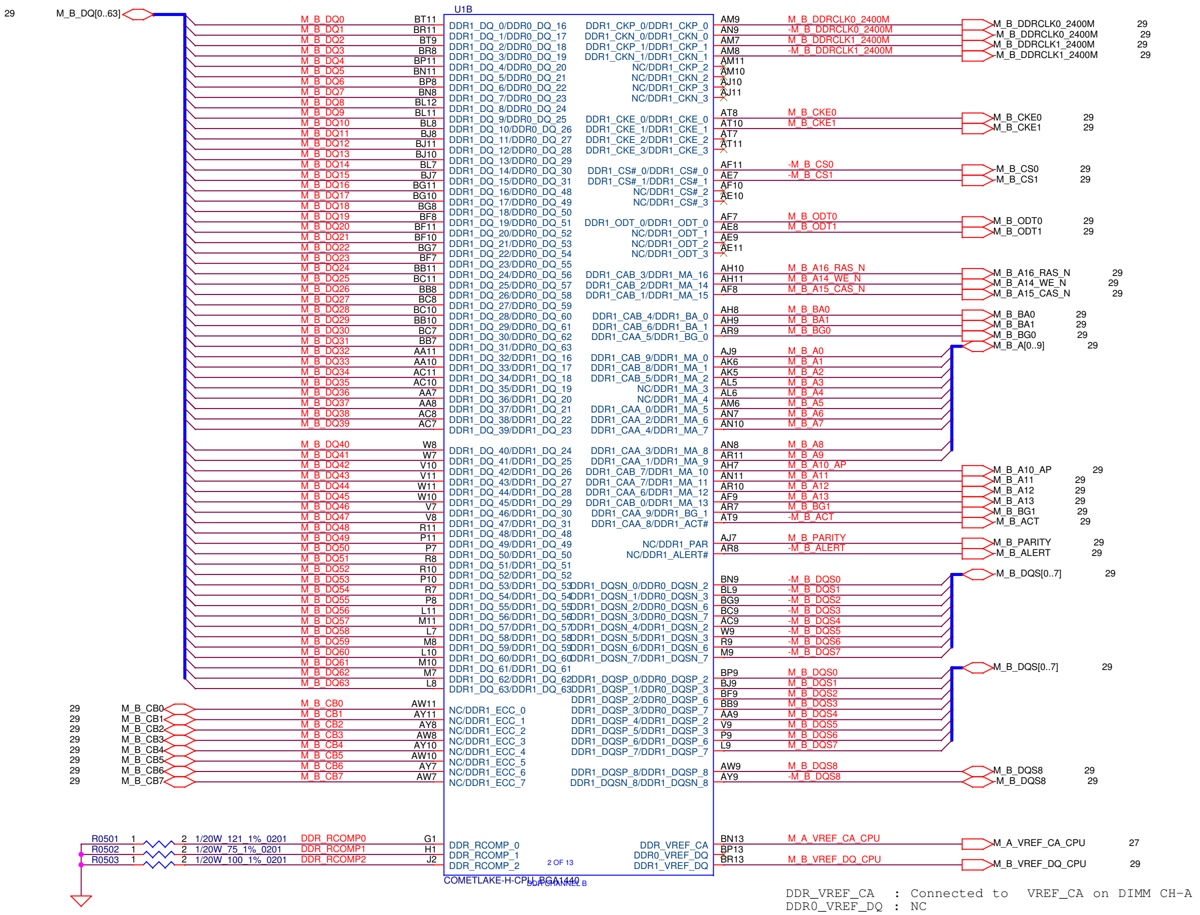
# CPU




## DDR4 INTERLEAVE IMPLEMENTATION

| LC Future Center Secret Data | Project Name | |
|---|---|---|
| LCFC | TpPv | |
| | Rev 1.0 | Title CPU |
| | Date: Friday, May 15, 2020 | Sheet 4 of 133 |

# CPU




DDR_VREF_CA : Connected to VREF_CA on DIMM CH-A
DDR0_VREF_DQ : NC
DDR1_VREF_DQ : Connected to VREF_CA on DIMM CH-B

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LCFC

Project Name: TpPv

Rev: 1.0

Title: CPU

Date: Friday, May 15, 2020

# CPU




Project Name: TpPv

Rev: 1.0

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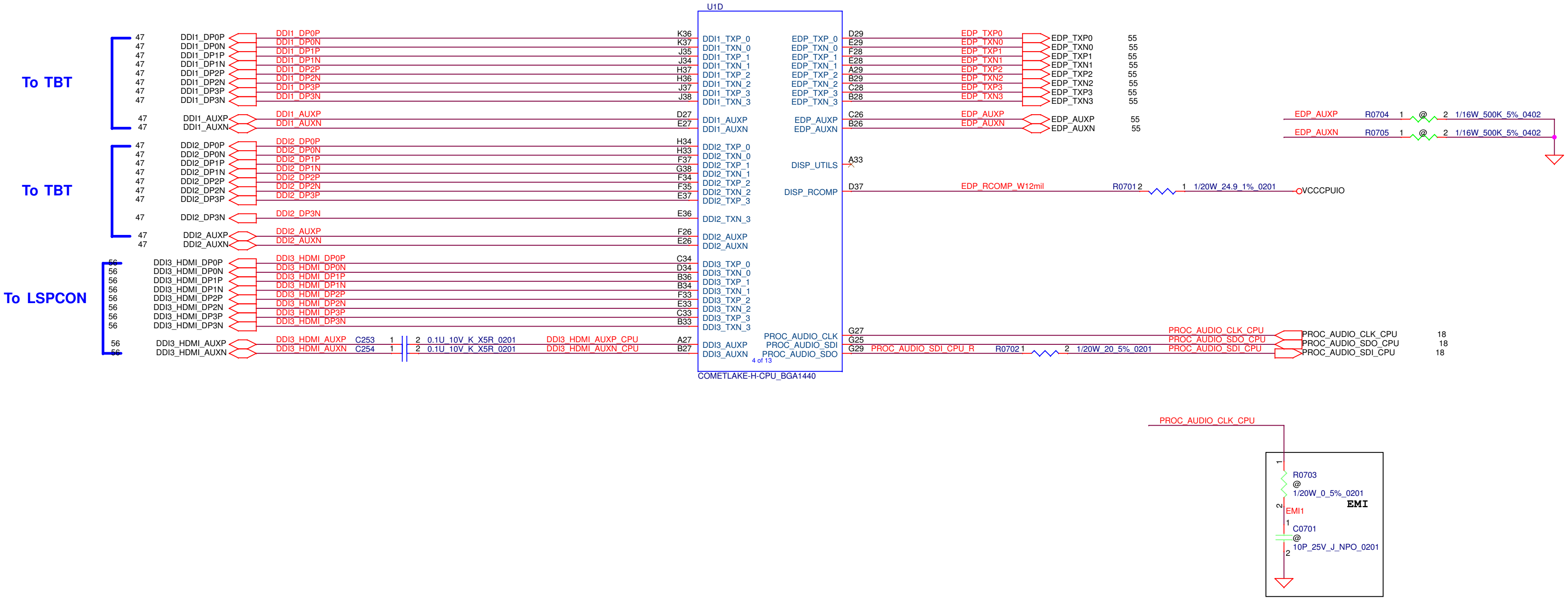
# CPU




| | | |
|---|---|---|
| LC Future Center Secret Data | Project Name | TpPv |
| LCFC | Rev 1.0 | Title CPU |
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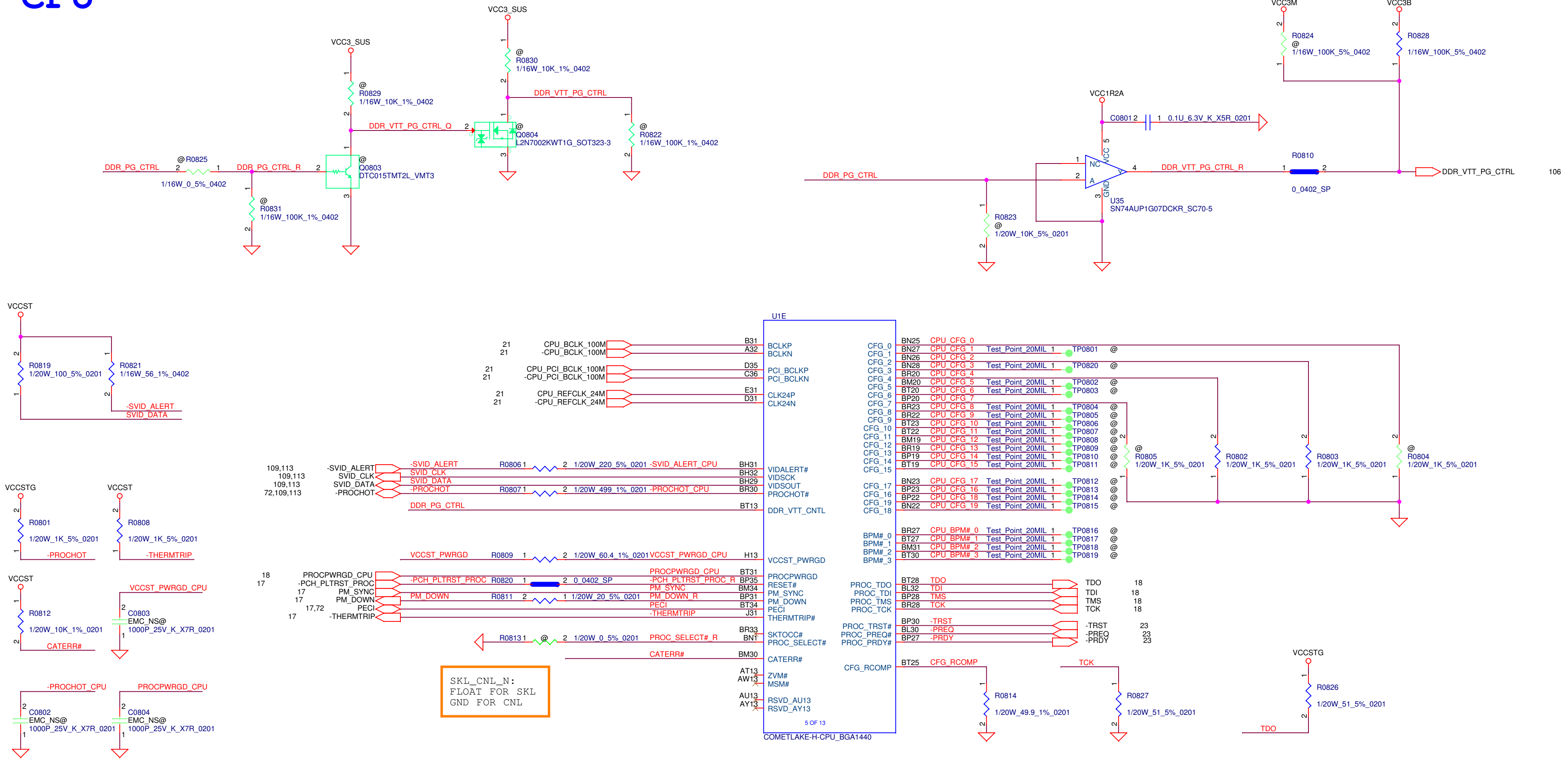
# CPU




```
If VCCSTG is used instead of VCC1R05_SUS,
VCCST_PWRGD will be off in Sleep S0 because
VCCSTG may be turned off when in Sleep S0.
Currently, VCCSTG is still on in Sleep S0
but we may change logic to turn off VCCSTG in sleep S0.
(CT_20141216)
```

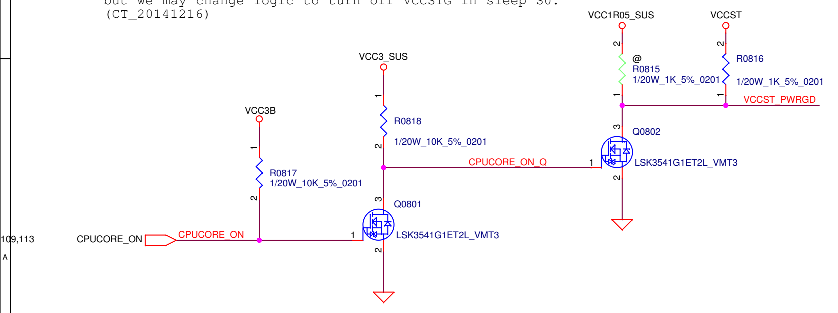


**TABLE** CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

**CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:**
1 : No Stall <----------- LOGIC
0 : Stall

**CFG[2] : PEG Static Lane Reversal**
1 : Normal Operation
0 : Lane Reversal <----------- LOGIC

**CFG[4] : eDP enable**
1 : Disabled
0 : Enabled <----------- LOGIC

**CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0**
11 : 1x16 <----------- LOGIC

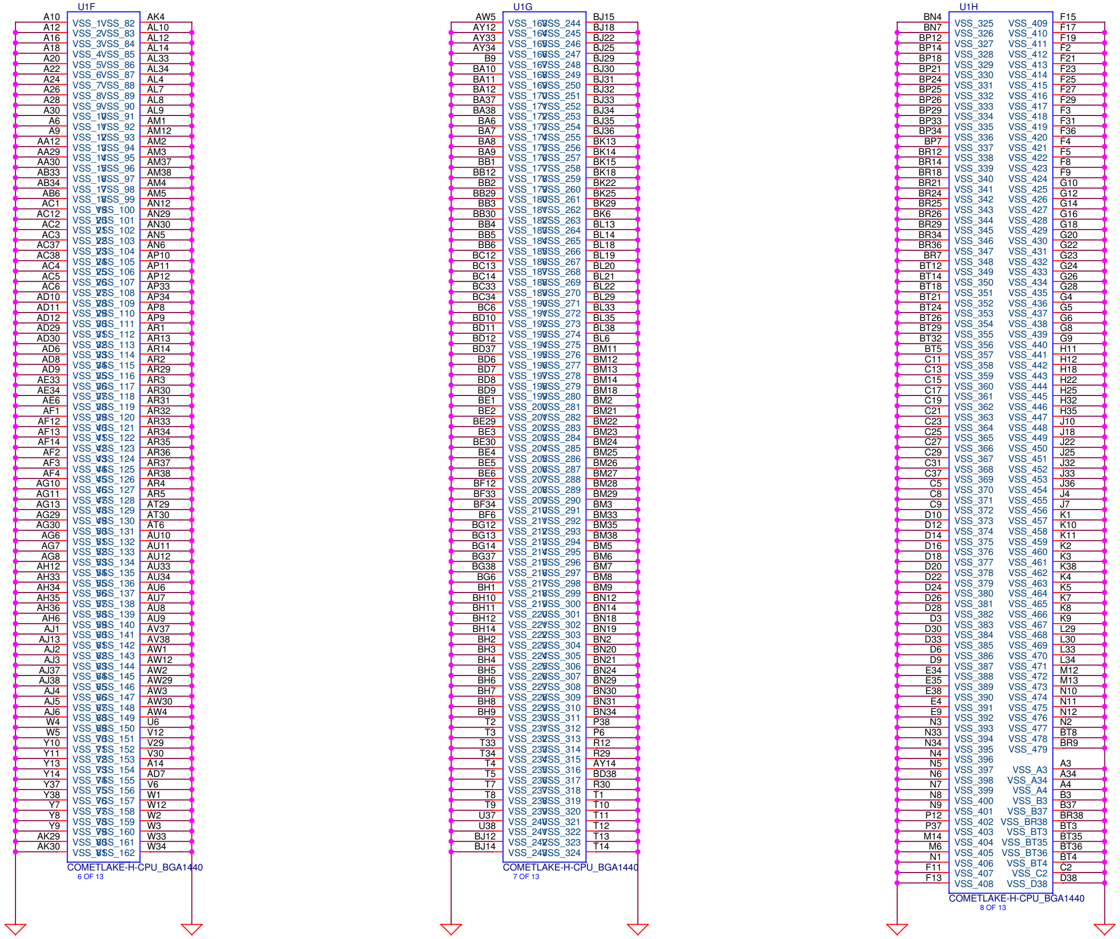
**CFG[7] : PEG Training**
1 : PEG Train immediately following RESET# deassertion <----------- LOGIC
0 : PEG Wait for BIOS for training

**CFG[19:8] : Reserved**

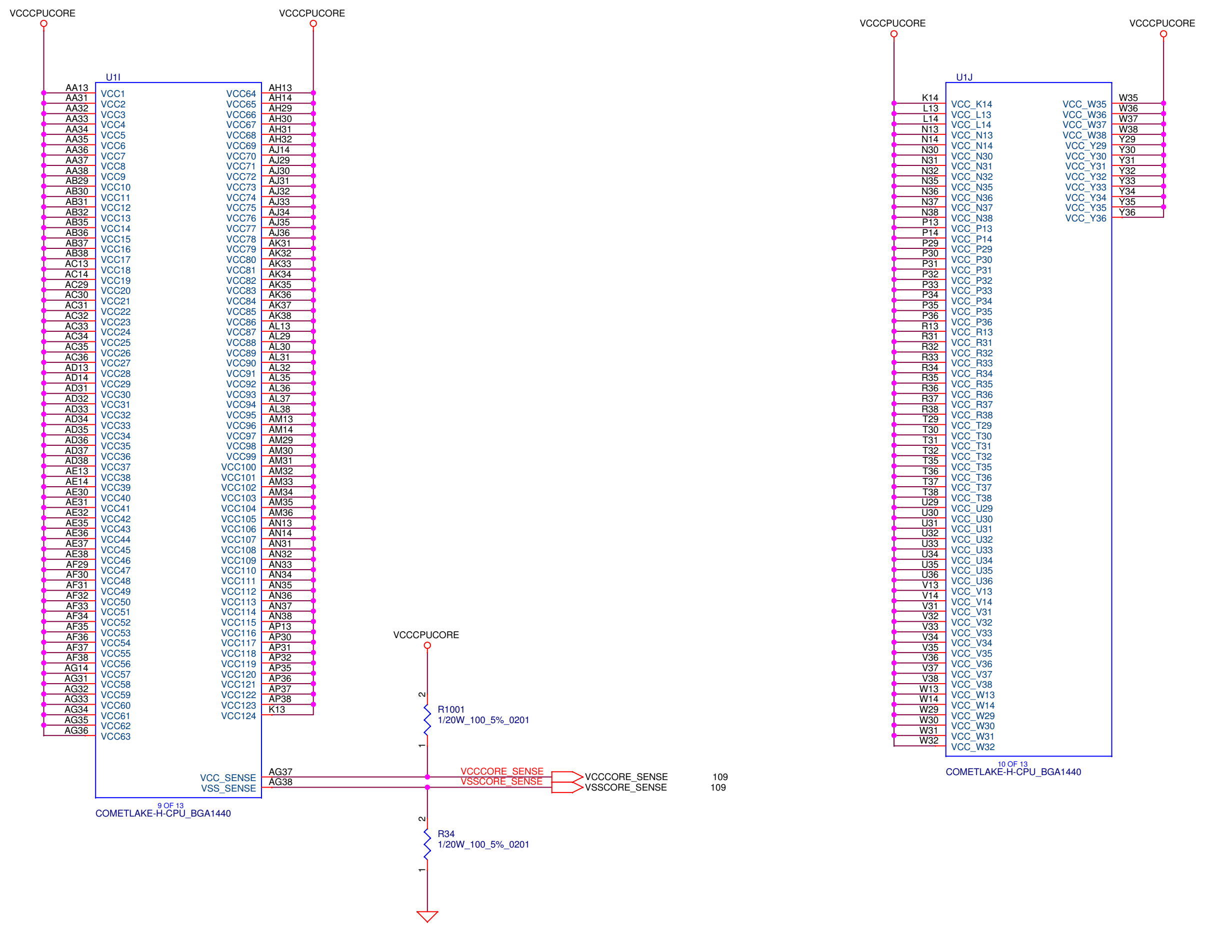
**For x16 Reversal Lanes - CFG[6/5/2] setting is 110**
**For x4 Reversal Lanes - CFG[6/5/2] setting is 000**

VCCST_PWRGD requirements
1) Indication that the VCCST\VDDQ power supplies are stable and within specification
2) VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
3) VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

# CPU

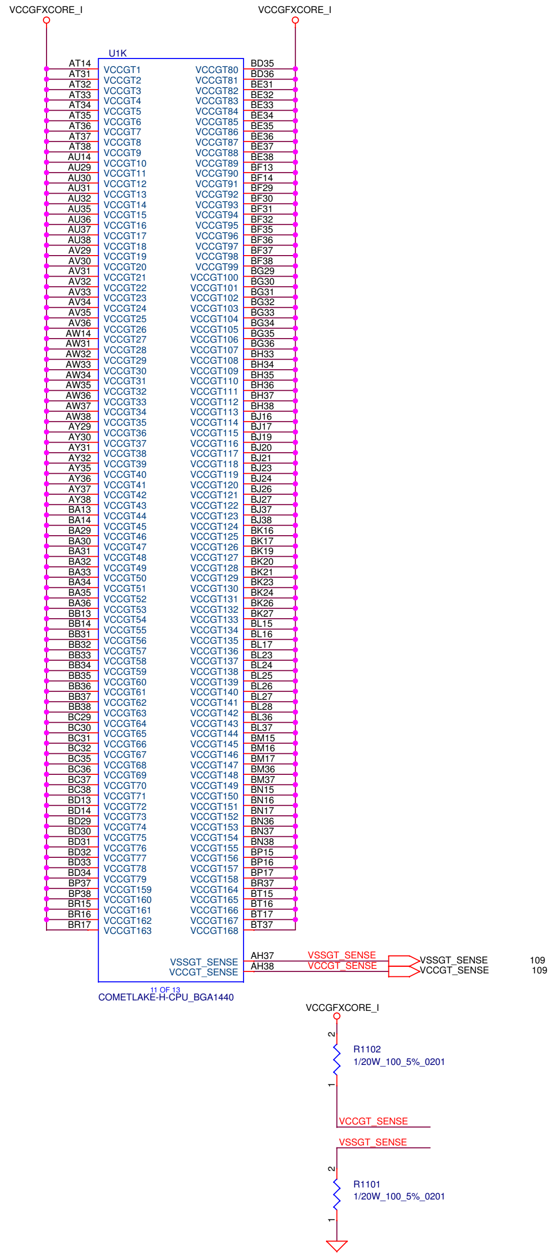

U1F
COMETLAKE-H-CPU_BGA1440
6 OF 13
U1G
COMETLAKE-H-CPU_BGA1440
7 OF 13
U1H
COMETLAKE-H-CPU_BGA1440
8 OF 13

# CPU



VCCCPUCORE
U1I
VCC_SENSE
VSS_SENSE
AG37
AG38
9 OF 13
COMETLAKE-H-CPU_BGA1440
R1001
1/20W_100_5%_0201
R34
1/20W_100_5%_0201
VCCCORE_SENSE
VSSCORE_SENSE
109
U1J
10 OF 13
COMETLAKE-H-CPU_BGA1440

# CPU

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LCFC

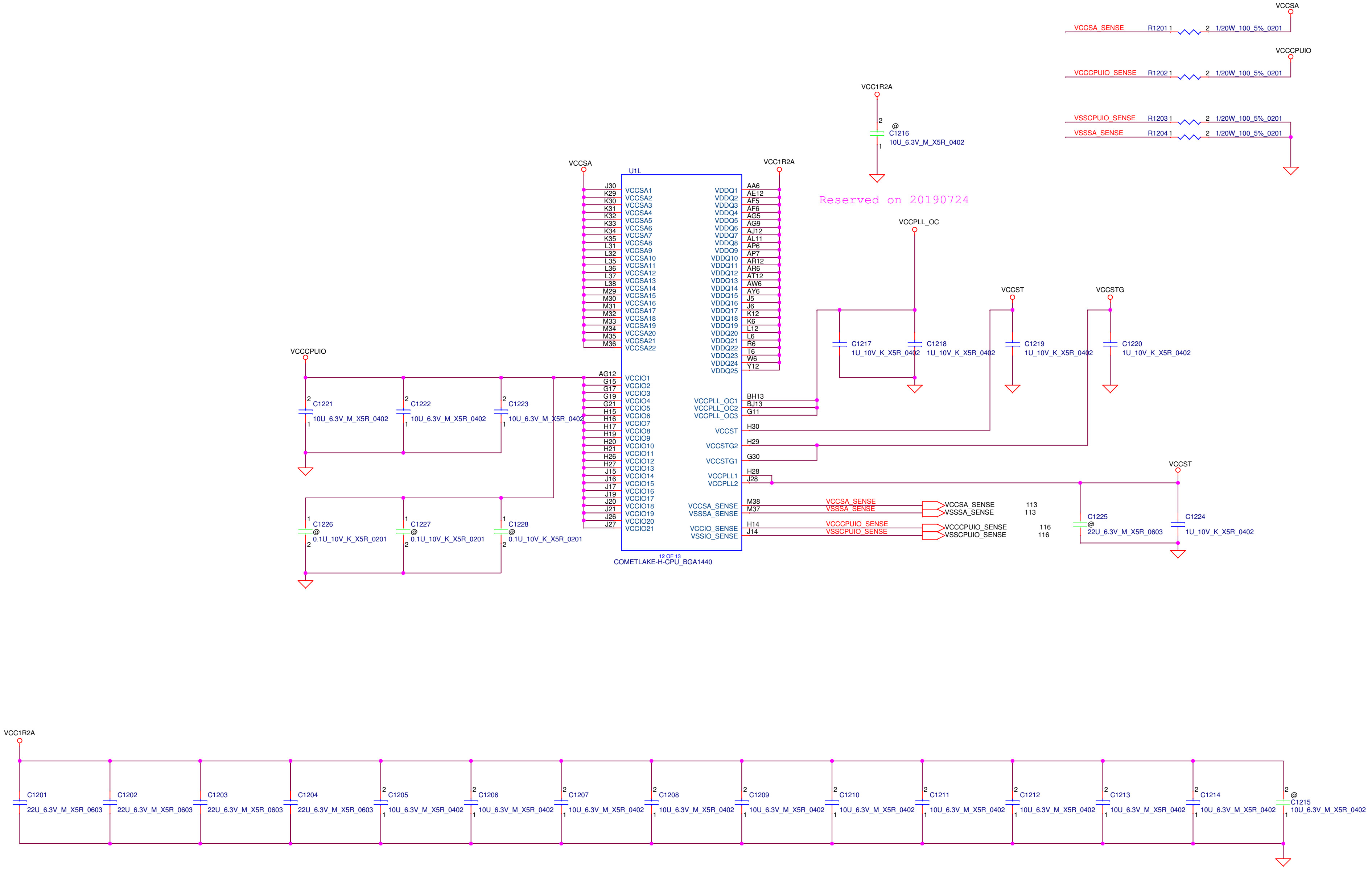
Project Name: TpPv

Rev: 1.0

Title: CPU

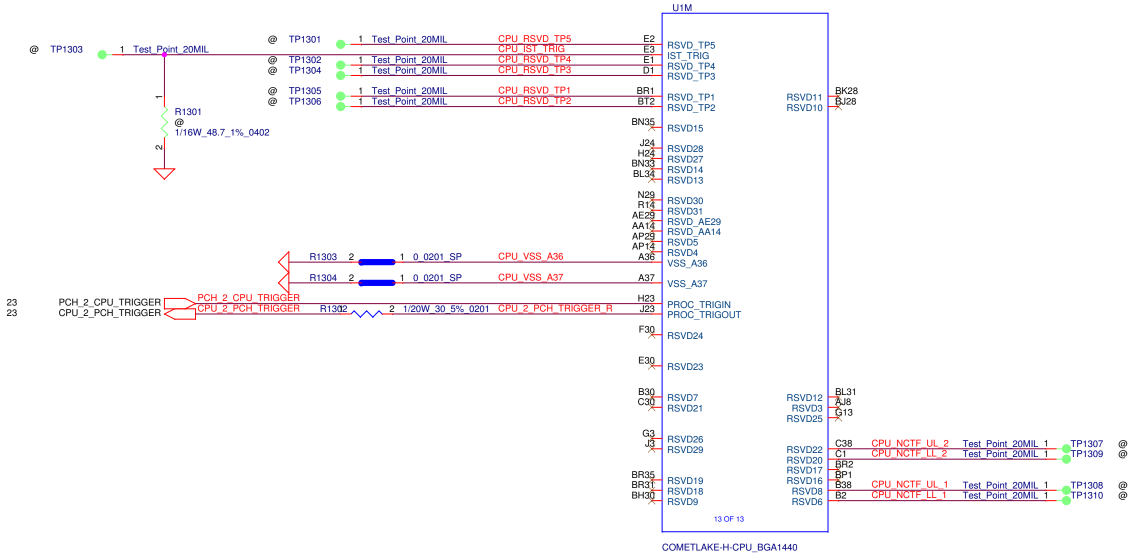
Date: Friday, May 15, 2020

# CPU



VCCSA
VCCSA_SENSE R1201 1 2 1/20W_100_5%_0201
VCCCPUIO
VCCCPUIO_SENSE R1202 1 2 1/20W_100_5%_0201
VSSCPUIO_SENSE R1203 1 2 1/20W_100_5%_0201
VSSSA_SENSE R1204 1 2 1/20W_100_5%_0201
VCC1R2A
@ C1216 10U_6.3V_M_X5R_0402
Reserved on 20190724
VCCPLL_OC
VCCST
VCCSTG
C1217 1U_10V_K_X5R_0402
C1218 1U_10V_K_X5R_0402
C1219 1U_10V_K_X5R_0402
C1220 1U_10V_K_X5R_0402
U1L
VCCSA1 – VCCSA22
VDDQ1 – VDDQ25
VCCIO1 – VCCIO21
VCCPLL_OC1 VCCPLL_OC2 VCCPLL_OC3
VCCST VCCSTG2 VCCSTG1 VCCPLL1 VCCPLL2
VCCSA_SENSE VSSSA_SENSE VCCIO_SENSE VSSIO_SENSE
12 OF 13
COMETLAKE-H-CPU_BGA1440
VCCCPUIO
C1221 10U_6.3V_M_X5R_0402
C1222 10U_6.3V_M_X5R_0402
C1223 10U_6.3V_M_X5R_0402
C1226 @ 0.1U_10V_K_X5R_0201
C1227 @ 0.1U_10V_K_X5R_0201
C1228 @ 0.1U_10V_K_X5R_0201
VCCSA_SENSE 113
VSSSA_SENSE 113
VCCCPUIO_SENSE 116
VSSCPUIO_SENSE 116
C1225 @ 22U_6.3V_M_X5R_0603
C1224 1U_10V_K_X5R_0402
VCC1R2A
C1201 22U_6.3V_M_X5R_0603
C1202 22U_6.3V_M_X5R_0603
C1203 22U_6.3V_M_X5R_0603
C1204 22U_6.3V_M_X5R_0603
C1205 10U_6.3V_M_X5R_0402
C1206 10U_6.3V_M_X5R_0402
C1207 10U_6.3V_M_X5R_0402
C1208 10U_6.3V_M_X5R_0402
C1209 10U_6.3V_M_X5R_0402
C1210 10U_6.3V_M_X5R_0402
C1211 10U_6.3V_M_X5R_0402
C1212 10U_6.3V_M_X5R_0402
C1213 10U_6.3V_M_X5R_0402
C1214 10U_6.3V_M_X5R_0402
@ C1215 10U_6.3V_M_X5R_0402

# CPU




LC Future Center Secret Data

Project Name: TpPv

Rev 1.0 | Title: CPU

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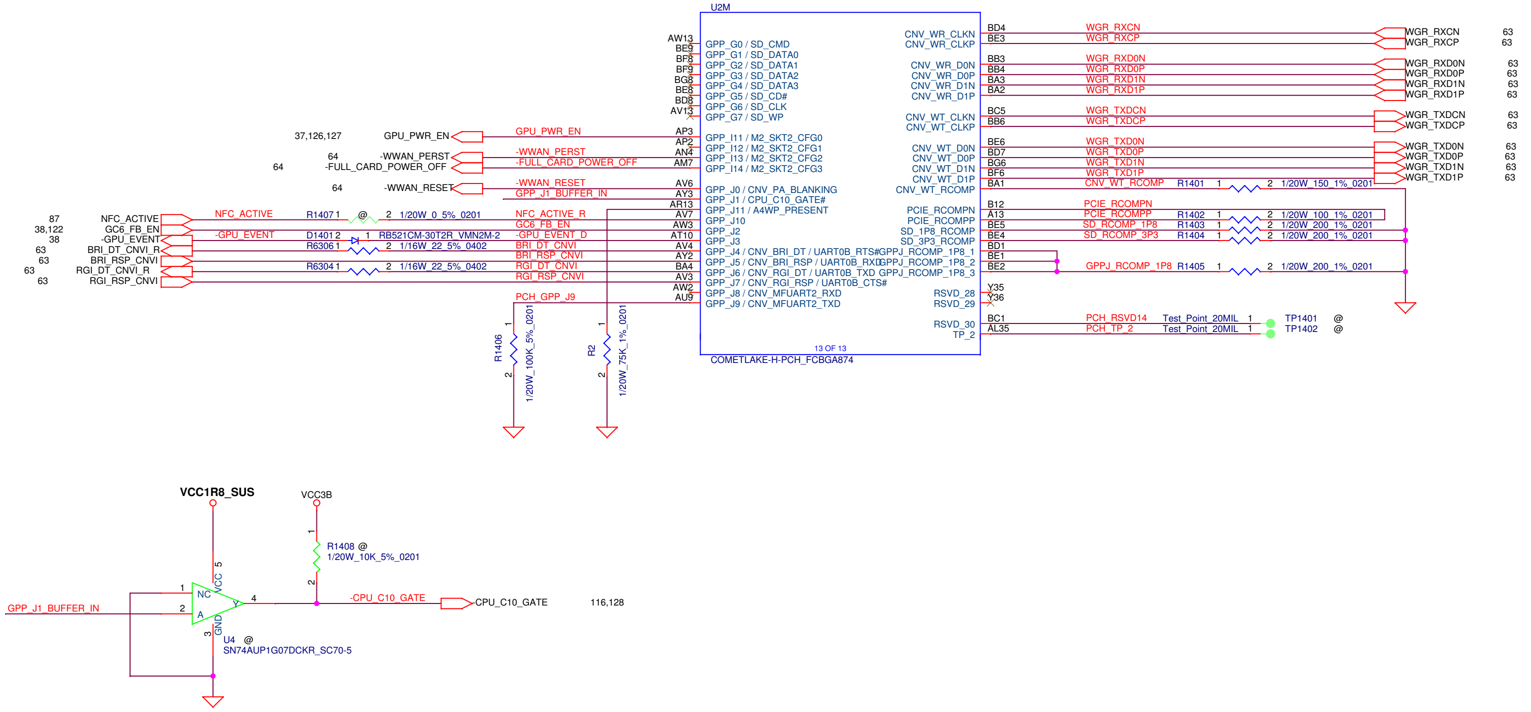
# PCH




| LC Future Center Secret Data | Project Name: TpPv |
| --- | --- |
| Rev 1.0 | Title: PCH |
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# PCH

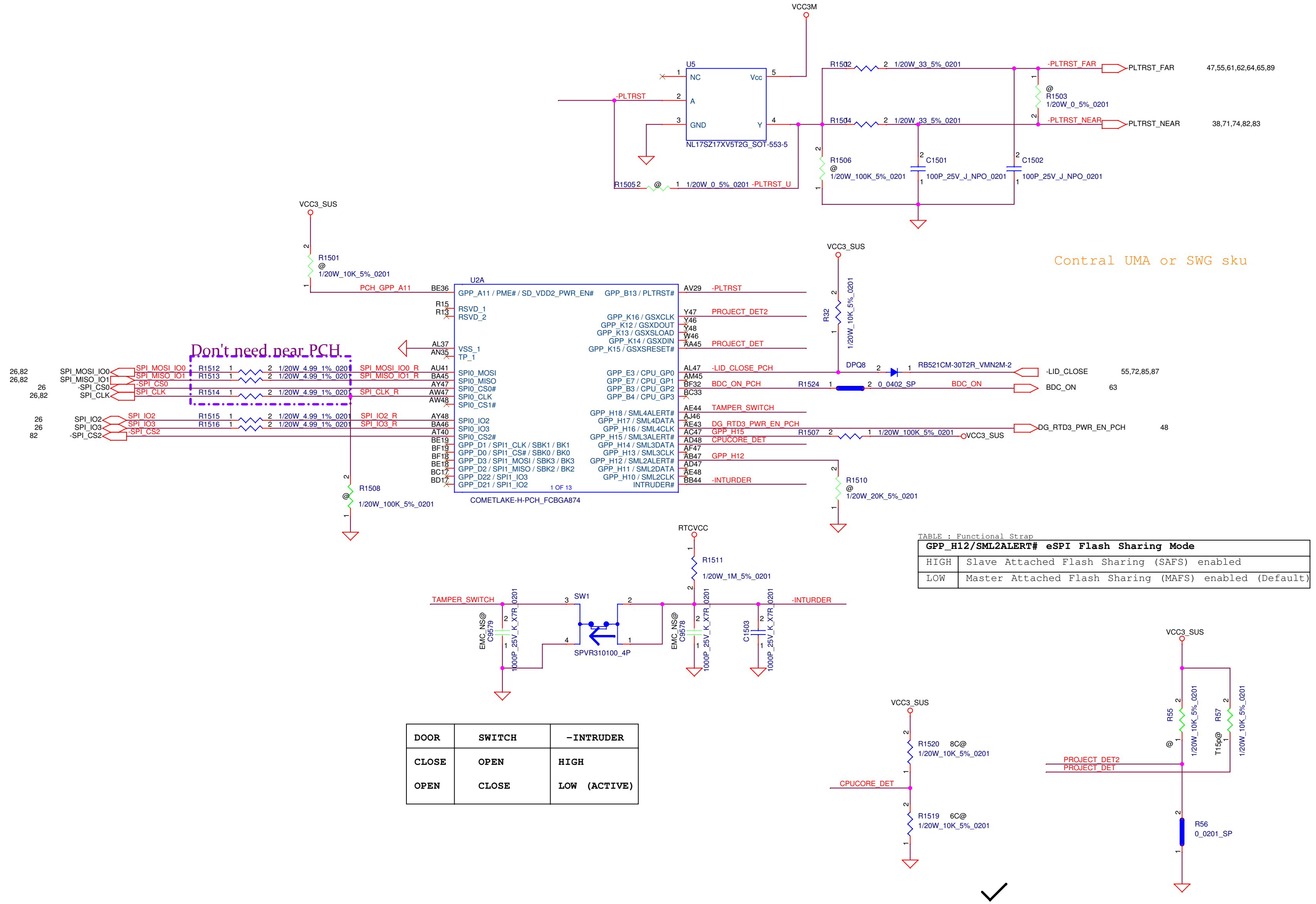



TABLE : Functional Strap

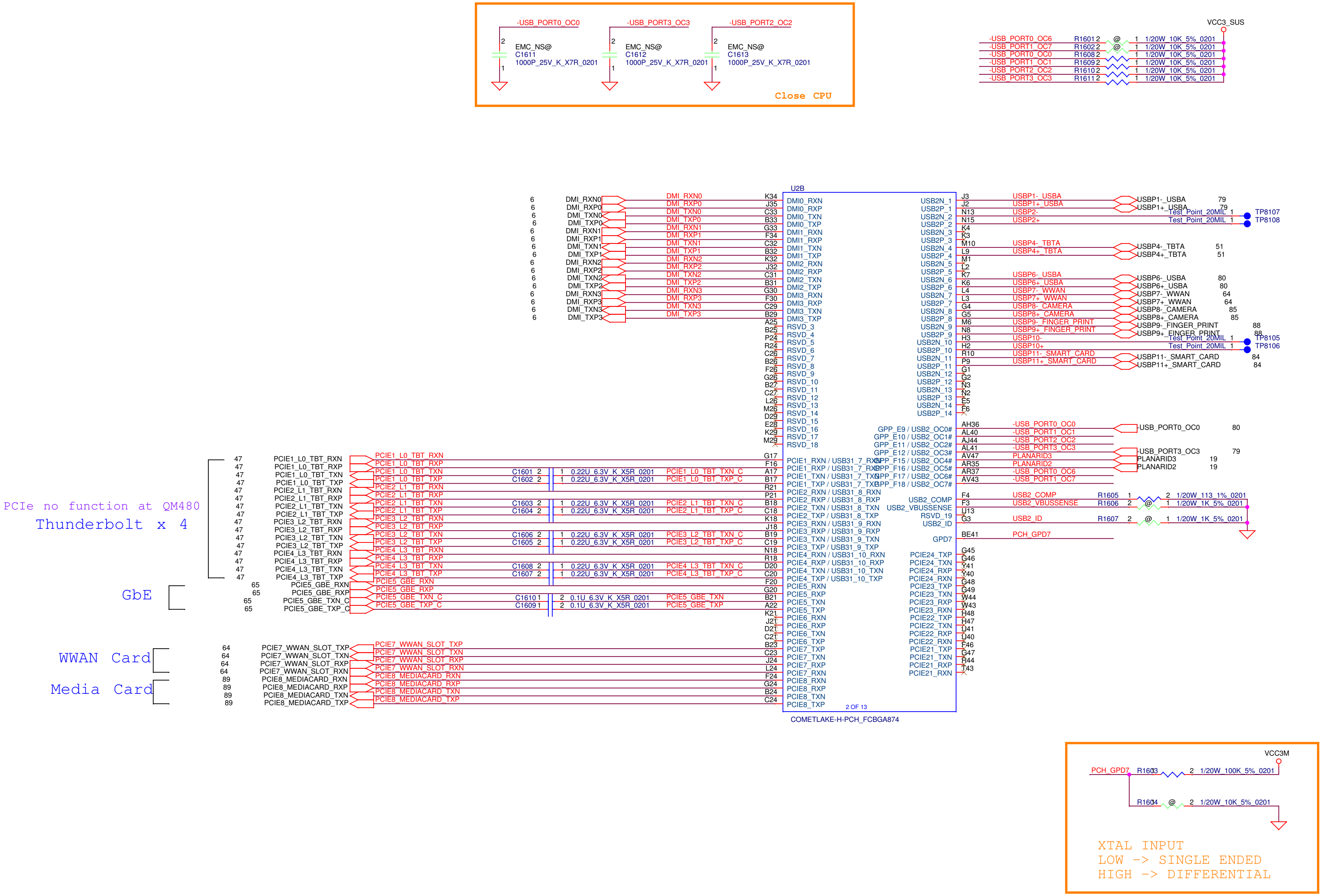
| GPP_H12/SML2ALERT# | eSPI Flash Sharing Mode |
|---|---|
| HIGH | Slave Attached Flash Sharing (SAFS) enabled |
| LOW | Master Attached Flash Sharing (MAFS) enabled (Default) |

| DOOR | SWITCH | -INTRUDER |
|---|---|---|
| CLOSE | OPEN | HIGH |
| OPEN | CLOSE | LOW (ACTIVE) |

✓

| CPUCORE_DET | HIGH | LOW |
|---|---|---|
| | 8C@ | 6C@ |

# PCH




LC Future Center Secret Data

LCFC

Project Name: TpPv

Rev: 1.0

Title: PCH

Date: Friday, May 15, 2020

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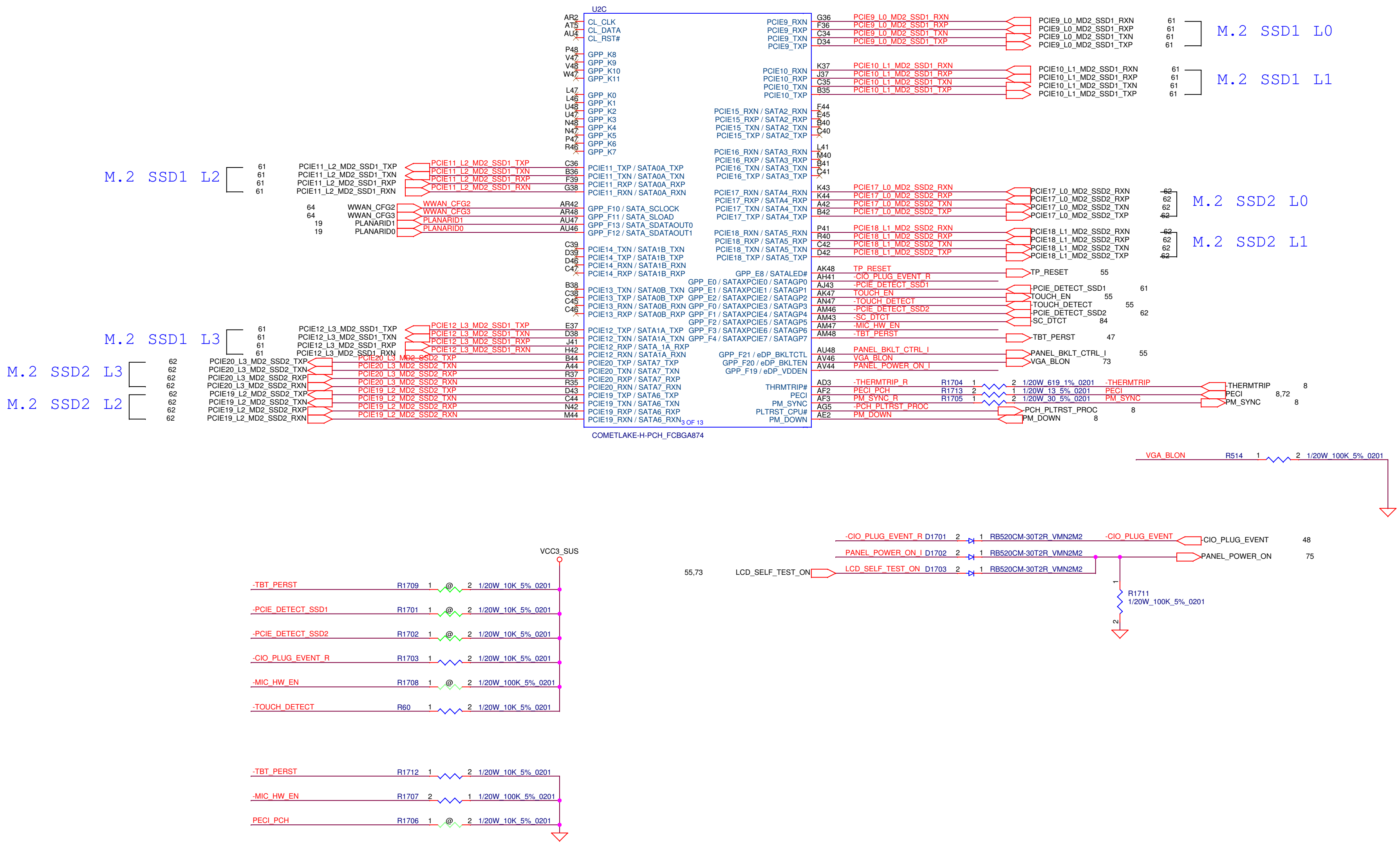
# PCH



U2C
COMETLAKE-H-PCH_FCBGA874
3 OF 13
CL_CLK
CL_DATA
CL_RST#
GPP_K8
GPP_K9
GPP_K10
GPP_K11
GPP_K0
GPP_K1
GPP_K2
GPP_K3
GPP_K4
GPP_K5
GPP_K6
GPP_K7
PCIE11_TXP / SATA0A_TXP
PCIE11_TXN / SATA0A_TXN
PCIE11_RXP / SATA0A_RXP
PCIE11_RXN / SATA0A_RXN
GPP_F10 / SATA_SCLOCK
GPP_F11 / SATA_SLOAD
GPP_F13 / SATA_SDATAOUT0
GPP_F12 / SATA_SDATAOUT1
PCIE14_TXN / SATA1B_TXN
PCIE14_TXP / SATA1B_TXP
PCIE14_RXN / SATA1B_RXN
PCIE14_RXP / SATA1B_RXP
PCIE13_TXN / SATA0B_TXN
PCIE13_TXP / SATA0B_TXP
PCIE13_RXN / SATA0B_RXN
PCIE13_RXP / SATA0B_RXP
PCIE12_TXP / SATA1A_TXP
PCIE12_TXN / SATA1A_TXN
PCIE12_RXP / SATA_1A_RXP
PCIE12_RXN / SATA1A_RXN
PCIE20_TXP / SATA7_TXP
PCIE20_TXN / SATA7_TXN
PCIE20_RXP / SATA7_RXP
PCIE20_RXN / SATA7_RXN
PCIE19_TXP / SATA6_TXP
PCIE19_TXN / SATA6_TXN
PCIE19_RXP / SATA6_RXP
PCIE19_RXN / SATA6_RXN
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP
PCIE15_RXN / SATA2_RXN
PCIE15_RXP / SATA2_RXP
PCIE15_TXN / SATA2_TXN
PCIE15_TXP / SATA2_TXP
PCIE16_RXN / SATA3_RXN
PCIE16_RXP / SATA3_RXP
PCIE16_TXN / SATA3_TXN
PCIE16_TXP / SATA3_TXP
PCIE17_RXN / SATA4_RXN
PCIE17_RXP / SATA4_RXP
PCIE17_TXN / SATA4_TXN
PCIE17_TXP / SATA4_TXP
PCIE18_RXN / SATA5_RXN
PCIE18_RXP / SATA5_RXP
PCIE18_TXN / SATA5_TXN
PCIE18_TXP / SATA5_TXP
GPP_E8 / SATALED#
GPP_E0 / SATAXPCIE0 / SATAGP0
GPP_E1 / SATAXPCIE1 / SATAGP1
GPP_E2 / SATAXPCIE2 / SATAGP2
GPP_F0 / SATAXPCIE3 / SATAGP3
GPP_F1 / SATAXPCIE4 / SATAGP4
GPP_F2 / SATAXPCIE5 / SATAGP5
GPP_F3 / SATAXPCIE6 / SATAGP6
GPP_F4 / SATAXPCIE7 / SATAGP7
GPP_F21 / eDP_BKLTCTL
GPP_F20 / eDP_BKLTEN
GPP_F19 / eDP_VDDEN
THRMTRIP#
PECI
PM_SYNC
PLTRST_CPU#
PM_DOWN
M.2 SSD1 L0
PCIE9_L0_MD2_SSD1_RXN 61
PCIE9_L0_MD2_SSD1_RXP 61
PCIE9_L0_MD2_SSD1_TXN 61
PCIE9_L0_MD2_SSD1_TXP 61
M.2 SSD1 L1
PCIE10_L1_MD2_SSD1_RXN 61
PCIE10_L1_MD2_SSD1_RXP 61
PCIE10_L1_MD2_SSD1_TXN 61
PCIE10_L1_MD2_SSD1_TXP 61
M.2 SSD1 L2
PCIE11_L2_MD2_SSD1_TXP 61
PCIE11_L2_MD2_SSD1_TXN 61
PCIE11_L2_MD2_SSD1_RXP 61
PCIE11_L2_MD2_SSD1_RXN 61
WWAN_CFG2 64
WWAN_CFG3 64
PLANARID1 19
PLANARID0 19
M.2 SSD2 L0
PCIE17_L0_MD2_SSD2_RXN 62
PCIE17_L0_MD2_SSD2_RXP 62
PCIE17_L0_MD2_SSD2_TXN 62
PCIE17_L0_MD2_SSD2_TXP 62
M.2 SSD2 L1
PCIE18_L1_MD2_SSD2_RXN 62
PCIE18_L1_MD2_SSD2_RXP 62
PCIE18_L1_MD2_SSD2_TXN 62
PCIE18_L1_MD2_SSD2_TXP 62
TP_RESET 55
-CIO_PLUG_EVENT_R
-PCIE_DETECT_SSD1 61
TOUCH_EN 55
-TOUCH_DETECT 55
-PCIE_DETECT_SSD2 62
-SC_DTCT 84
-MIC_HW_EN
-TBT_PERST 47
PANEL_BKLT_CTRL_I 55
VGA_BLON 73
PANEL_POWER_ON_I
M.2 SSD1 L3
PCIE12_L3_MD2_SSD1_TXP 61
PCIE12_L3_MD2_SSD1_TXN 61
PCIE12_L3_MD2_SSD1_RXP 61
PCIE12_L3_MD2_SSD1_RXN 61
M.2 SSD2 L3
PCIE20_L3_MD2_SSD2_TXP 62
PCIE20_L3_MD2_SSD2_TXN 62
PCIE20_L3_MD2_SSD2_RXP 62
PCIE20_L3_MD2_SSD2_RXN 62
M.2 SSD2 L2
PCIE19_L2_MD2_SSD2_TXP 62
PCIE19_L2_MD2_SSD2_TXN 62
PCIE19_L2_MD2_SSD2_RXP 62
PCIE19_L2_MD2_SSD2_RXN 62
-THERMTRIP_R R1704 1/20W_619_1%_0201 -THERMTRIP 8
PECI_PCH R1713 1/20W_13_5%_0201 PECI 8,72
PM_SYNC_R R1705 1/20W_30_5%_0201 PM_SYNC 8
-PCH_PLTRST_PROC 8
PM_DOWN 8
VGA_BLON R514 1/20W_100K_5%_0201
-CIO_PLUG_EVENT_R D1701 RB520CM-30T2R_VMN2M2 -CIO_PLUG_EVENT 48
PANEL_POWER_ON_I D1702 RB520CM-30T2R_VMN2M2 PANEL_POWER_ON 75
55,73 LCD_SELF_TEST_ON D1703 RB520CM-30T2R_VMN2M2
R1711 1/20W_100K_5%_0201
VCC3_SUS
-TBT_PERST R1709 1/20W_10K_5%_0201
-PCIE_DETECT_SSD1 R1701 1/20W_10K_5%_0201
-PCIE_DETECT_SSD2 R1702 1/20W_10K_5%_0201
-CIO_PLUG_EVENT_R R1703 1/20W_10K_5%_0201
-MIC_HW_EN R1708 1/20W_100K_5%_0201
-TOUCH_DETECT R60 1/20W_10K_5%_0201
-TBT_PERST R1712 1/20W_10K_5%_0201
-MIC_HW_EN R1707 1/20W_100K_5%_0201
PECI_PCH R1706 1/20W_10K_5%_0201

# PCH

TABLE : Functional Strap

| HDA_SDO/I2S0_TXD | |
|---|---|
| Flash Descriptor Security Override | |
| HIGH | Disable Flash Descriptor Security (Override) |
| LOW | Enable Flash Descriptor Security (Default) |

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.

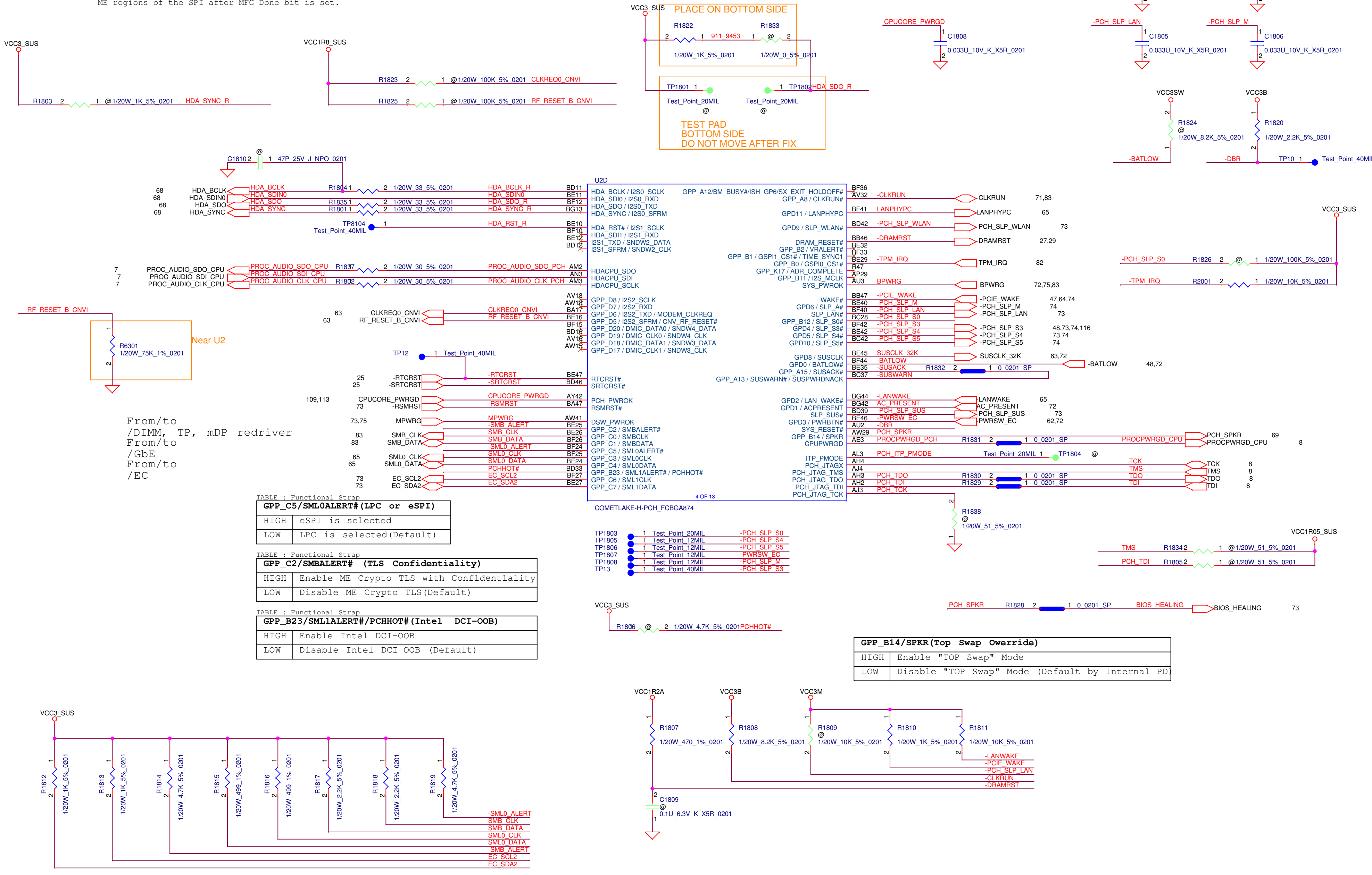



TABLE : Functional Strap

| GPP_C5/SML0ALERT#(LPC or eSPI) | |
|---|---|
| HIGH | eSPI is selected |
| LOW | LPC is selected(Default) |

TABLE : Functional Strap

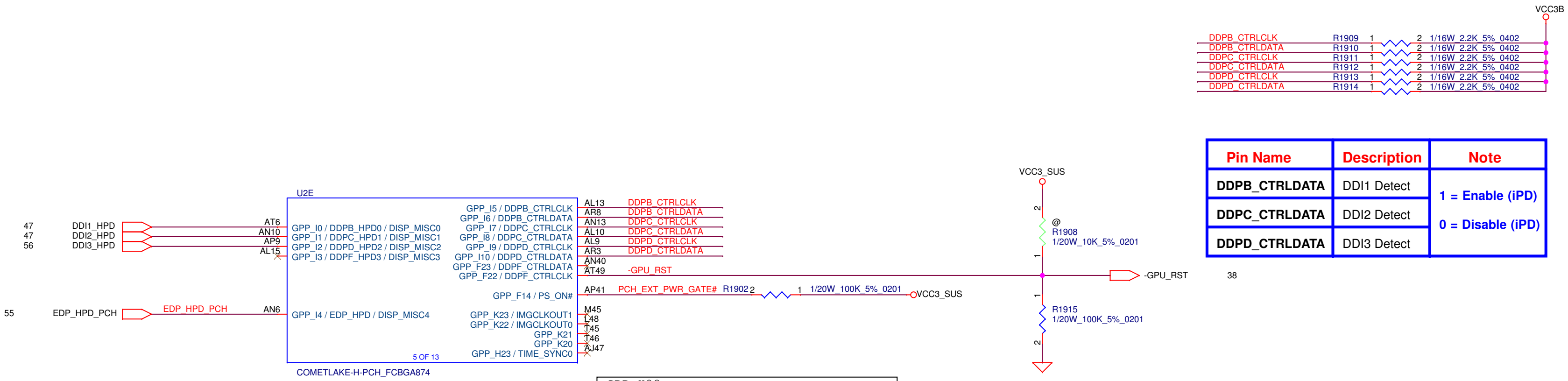
| GPP_C2/SMBALERT# (TLS Confidentiality) | |
|---|---|
| HIGH | Enable ME Crypto TLS with Confldentlality |
| LOW | Disable ME Crypto TLS(Default) |

TABLE : Functional Strap

| GPP_B23/SML1ALERT#/PCHHOT#(Intel DCI-OOB) | |
|---|---|
| HIGH | Enable Intel DCI-OOB |
| LOW | Disable Intel DCI-OOB (Default) |

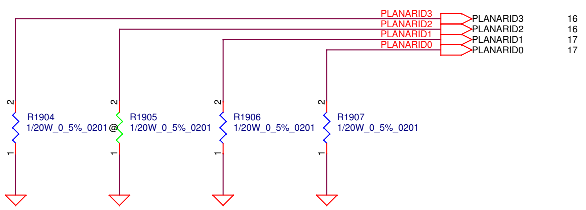
| GPP_B14/SPKR(Top Swap Override) | |
|---|---|
| HIGH | Enable "TOP Swap" Mode |
| LOW | Disable "TOP Swap" Mode (Default by Internal PD) |

# PCH




| Pin Name | Description | Note |
|---|---|---|
| DDPB_CTRLDATA | DDI1 Detect | 1 = Enable (iPD) |
| DDPC_CTRLDATA | DDI2 Detect | 0 = Disable (iPD) |
| DDPD_CTRLDATA | DDI3 Detect | |

```
GPP_H23
PAYTON: T.B.D
WALTER: -DGFX_WITH_DISPLAYOUT (INPUT)
  N18E QUADRO = LOW
  T.B.D= HIGH
```



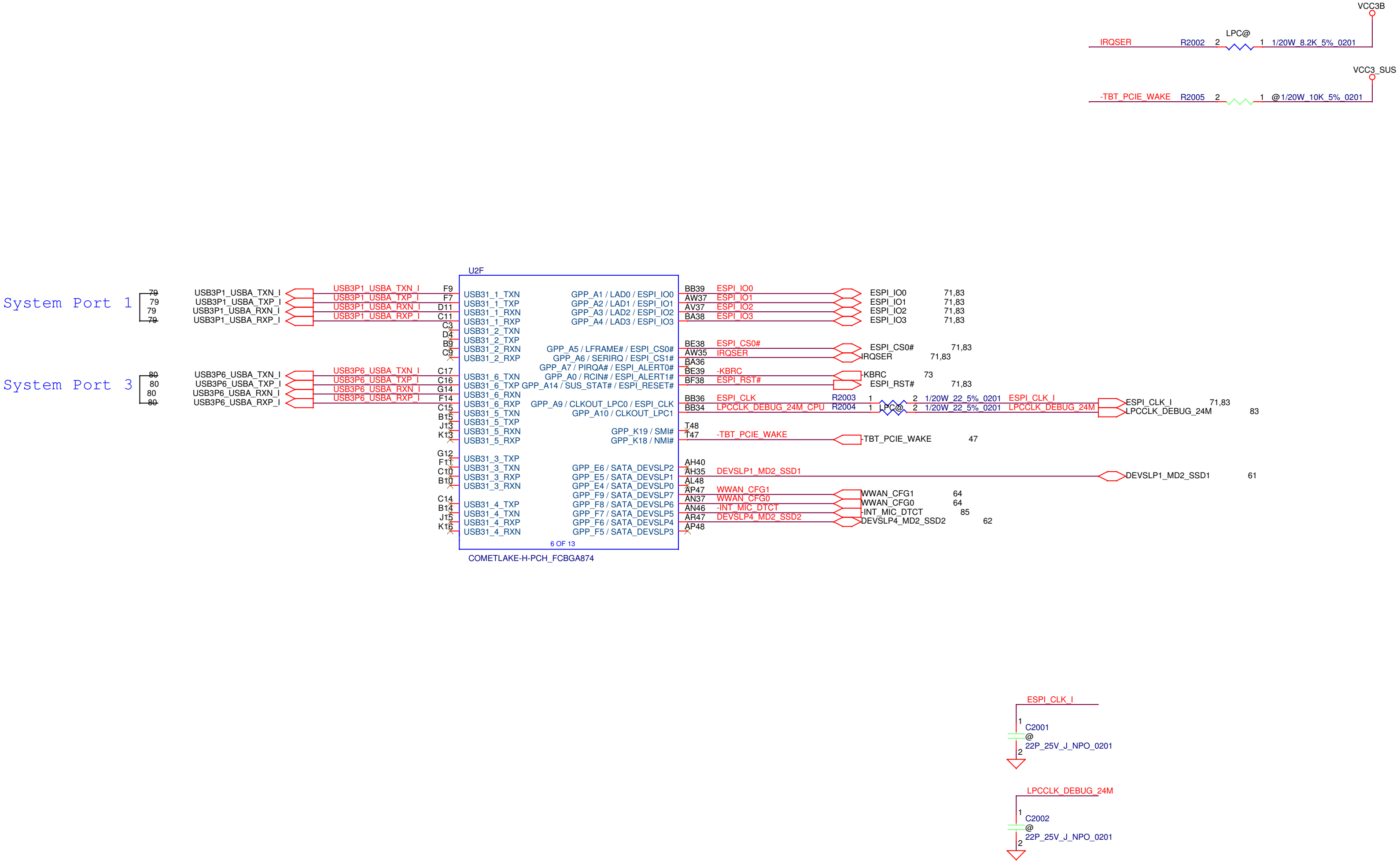

**TABLE**

| | PLANAR ID | | | |
|---|---|---|---|---|
| | 3 | 2 | 1 | 0 |
| | R1904 | R1905 | R1906 | R1907 |
| 1 | NA | NA | NA | NA |
| 0 | ASM | ASM | ASM | ASM |

**TABLE**

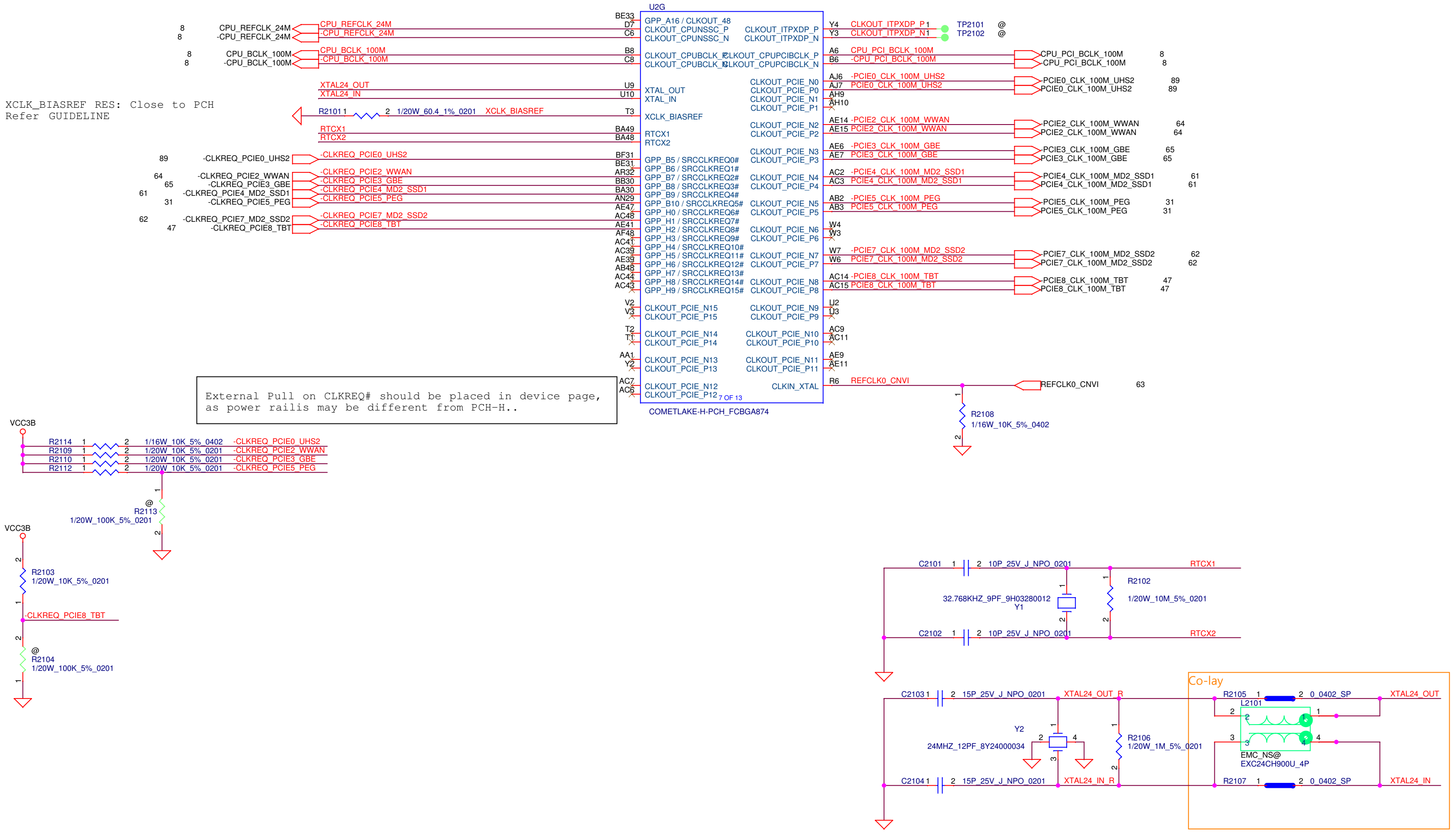
| LEVEL | PLANARID[3..0] | CPU | PCH |
|---|---|---|---|
| PDV | -------- | -------- | -------- |
| EVT | 0001b | ES | ES |
| FVT | 0010b | ES | ES |
| SIT | 0011b | QS | QS |
| SIT-R | 0100b | QS | QS |
| SVT | 0100b | QS | QS |

# PCH



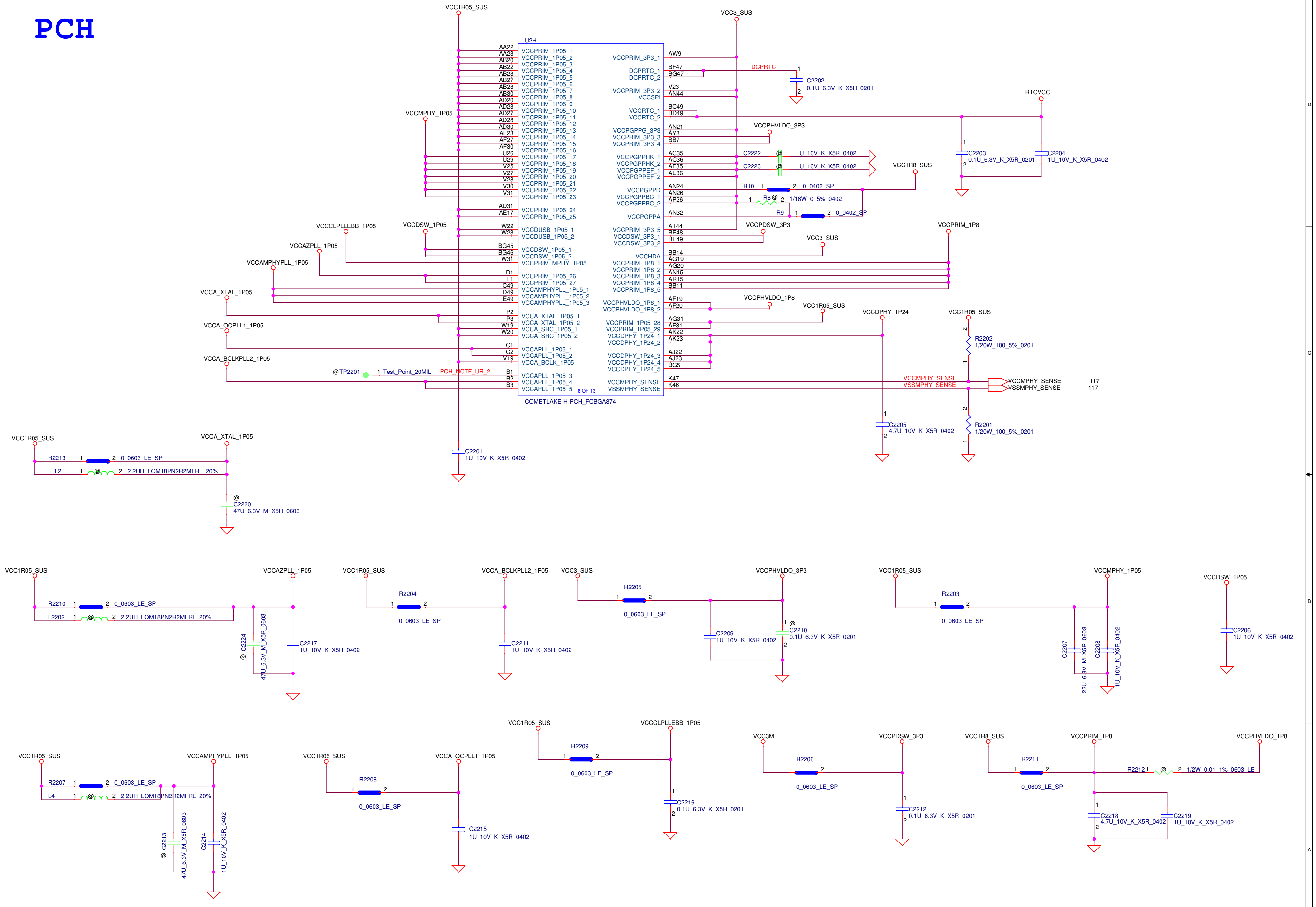

| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| Rev 1.0 | Title: PCH |
| Date: Friday, May 15, 2020 | Sheet 20 of 133 |

# PCH




| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| Rev 1.0 | Title: PCH |
| Date: Friday, May 15, 2020 | Sheet 21 of 133 |

# PCH



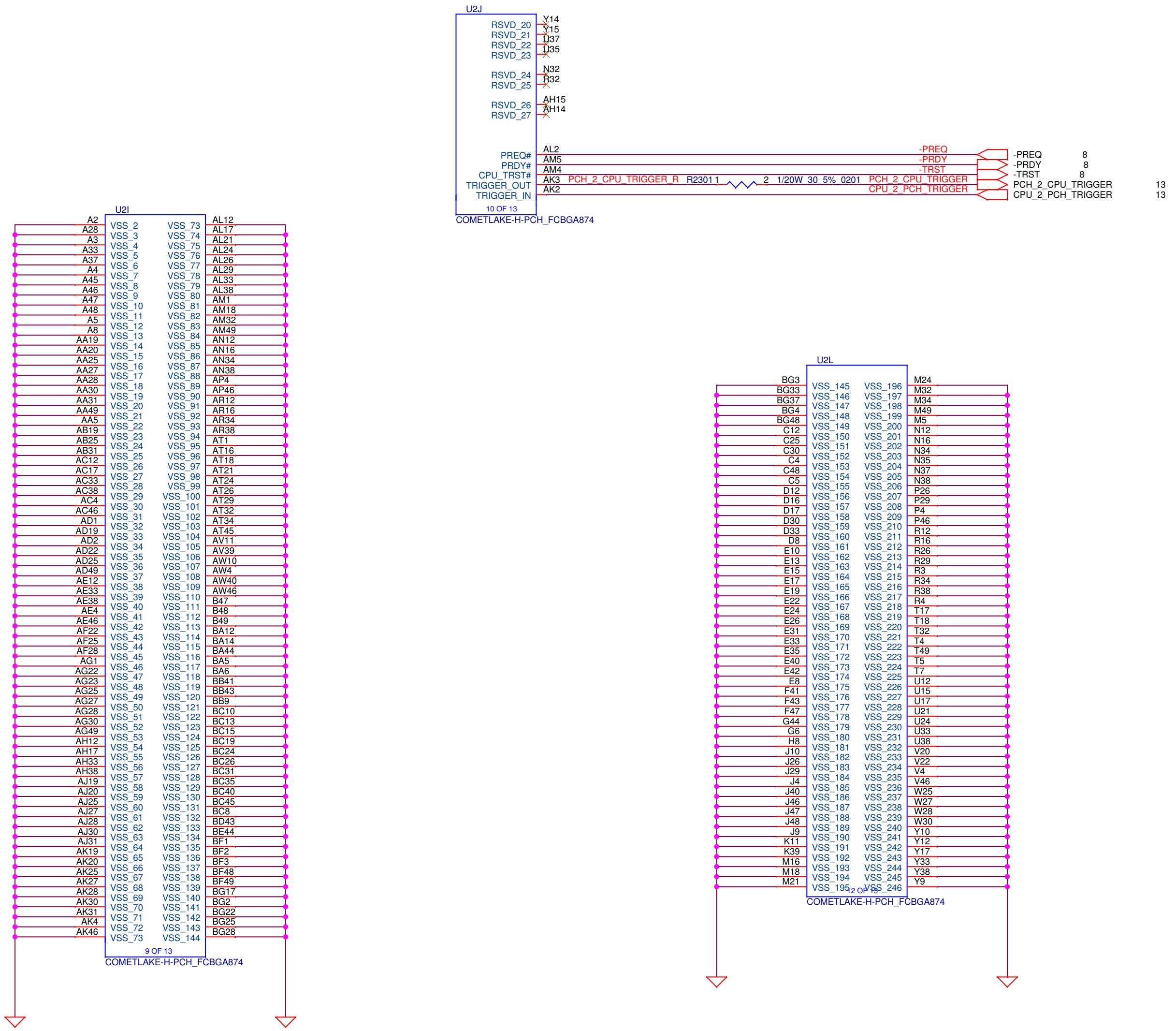

LC Future Center Secret Data

Project Name: TpPv

Rev 1.0 | Title: PCH

Date: Friday, May 15, 2020 | Sheet 22 of 133

# PCH



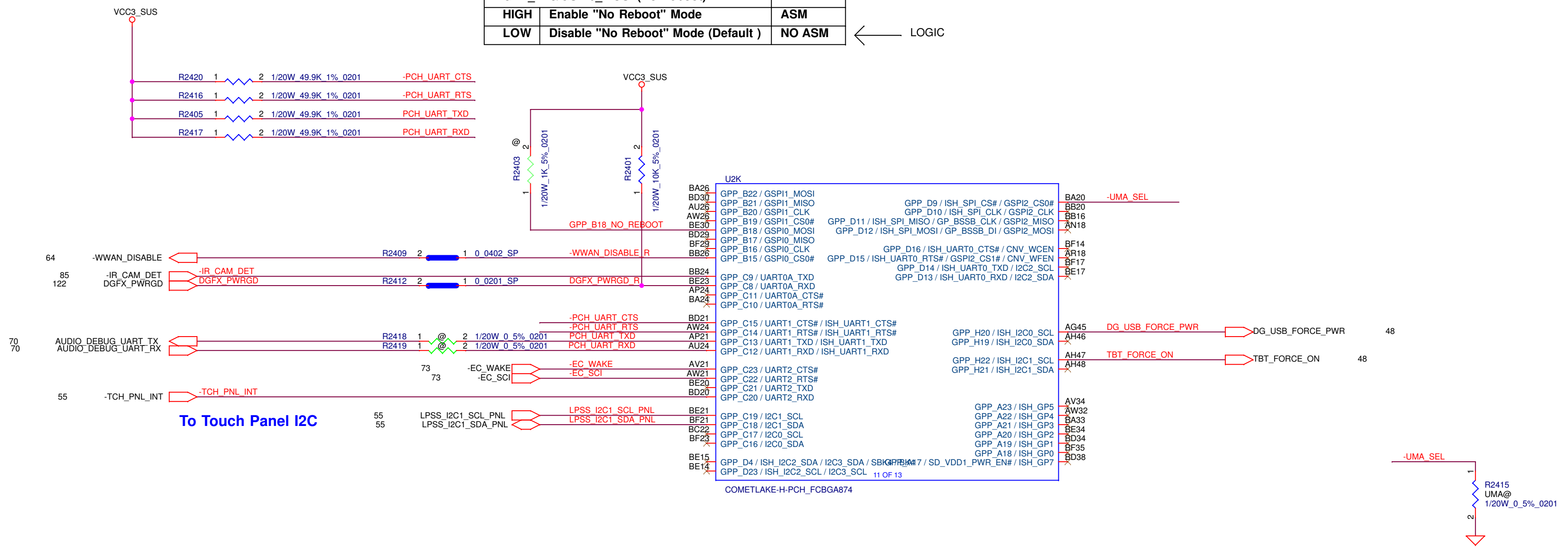

| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| LCFC | Rev 1.0 — Title: PCH |
| | Date: Friday, May 15, 2020 — Sheet 23 of 133 |

# PCH

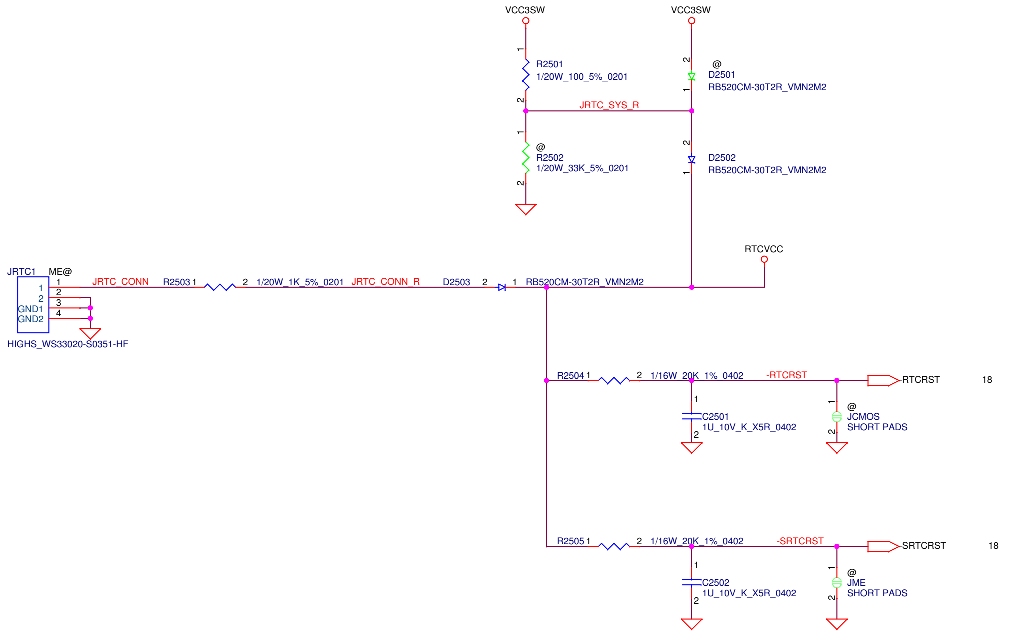
**TABLE : Functional Strap**

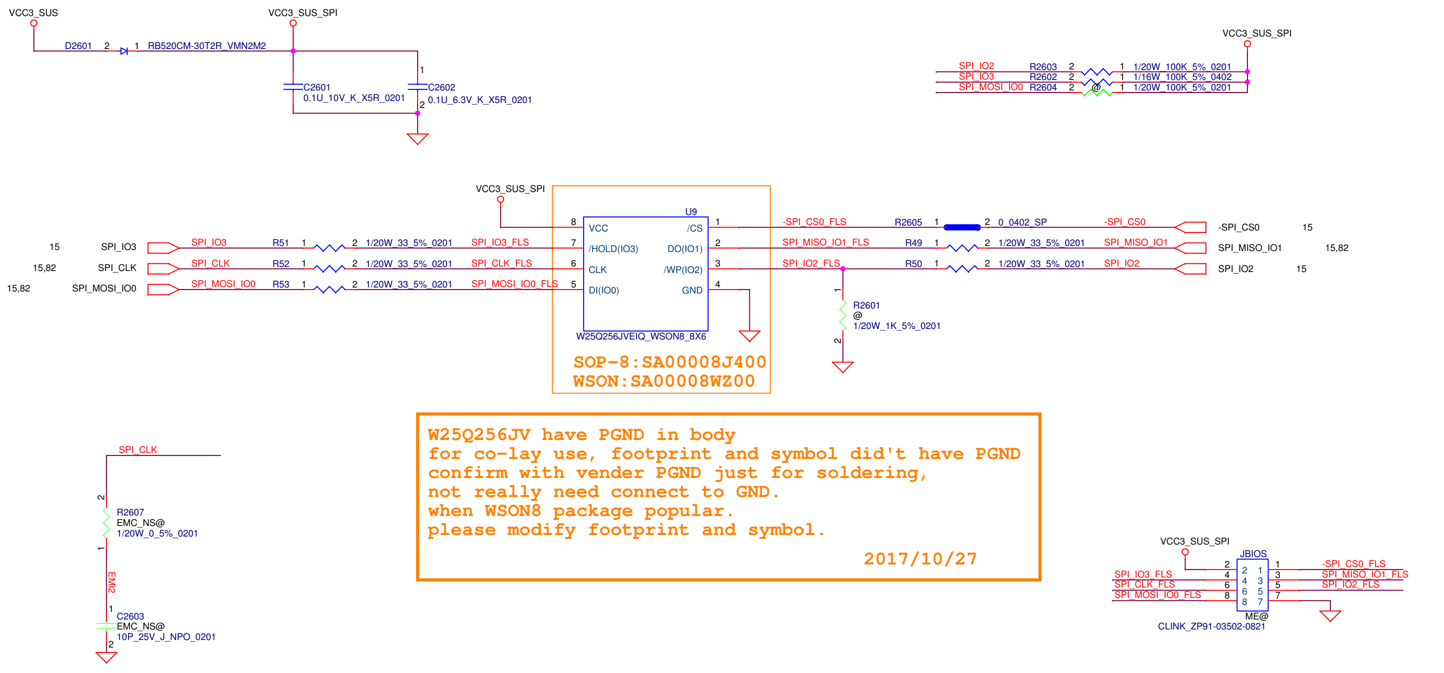
| GPP_B18/GSPI0_MOSI (No Reboot) | | PCHR96 |
|---|---|---|
| HIGH | Enable "No Reboot" Mode | ASM |
| LOW | Disable "No Reboot" Mode (Default ) | NO ASM |

LOGIC



# RTC


VCC3SW
VCC3SW
R2501
1/20W_100_5%_0201
@
D2501
RB520CM-30T2R_VMN2M2
JRTC_SYS_R
@
R2502
1/20W_33K_5%_0201
D2502
RB520CM-30T2R_VMN2M2
RTCVCC
JRTC1
ME@
GND1
GND2
HIGHS_WS33020-S0351-HF
JRTC_CONN
R2503
1/20W_1K_5%_0201
JRTC_CONN_R
D2503
RB520CM-30T2R_VMN2M2
R2504
1/16W_20K_1%_0402
-RTCRST
RTCRST
18
C2501
1U_10V_K_X5R_0402
@
JCMOS
SHORT PADS
R2505
1/16W_20K_1%_0402
-SRTCRST
SRTCRST
18
C2502
1U_10V_K_X5R_0402
@
JME
SHORT PADS




LC Future Center Secret Data

LCFC

Project Name: TpPv

Rev 1.0

Title: SPI

Date: Friday, May 15, 2020

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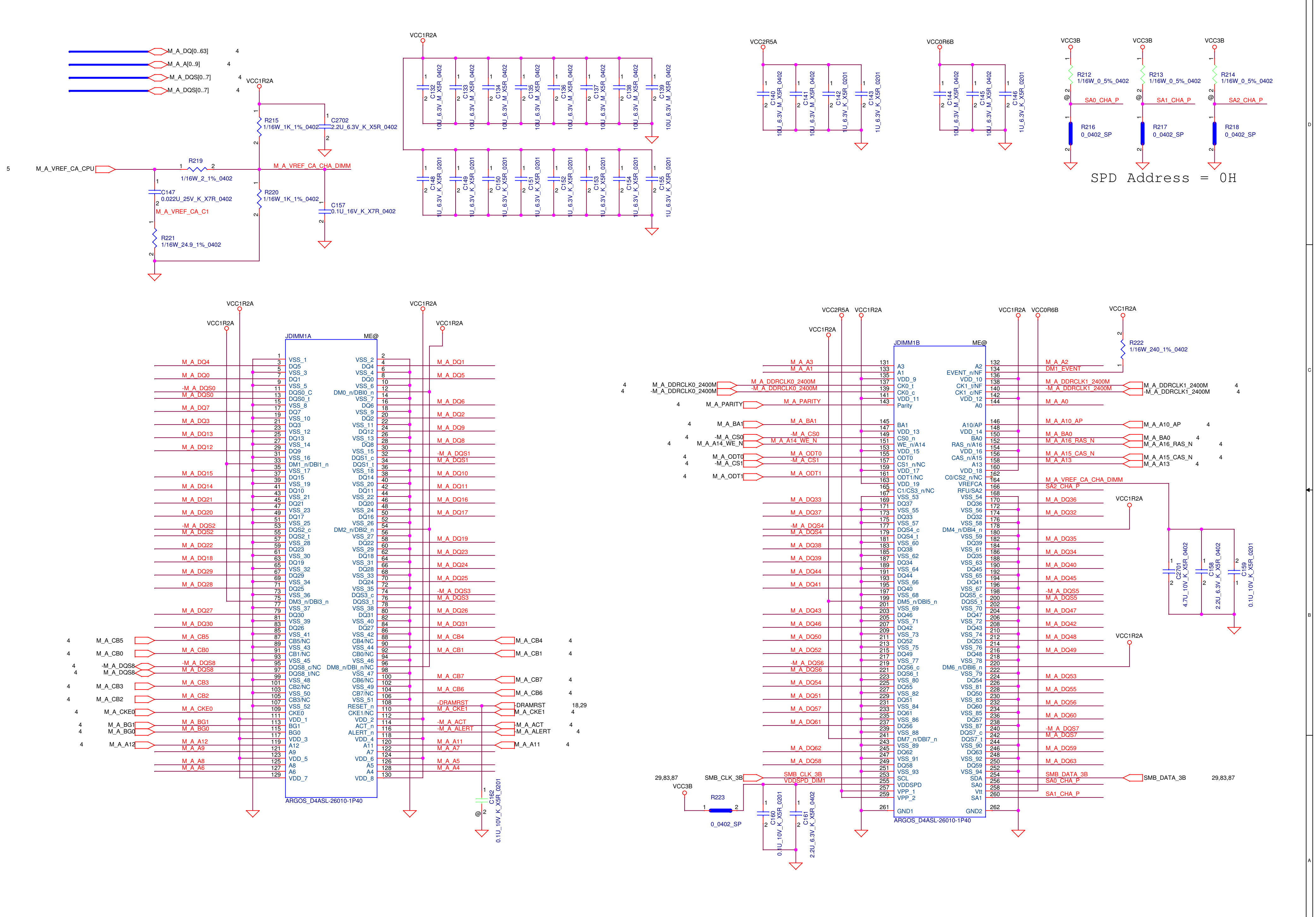
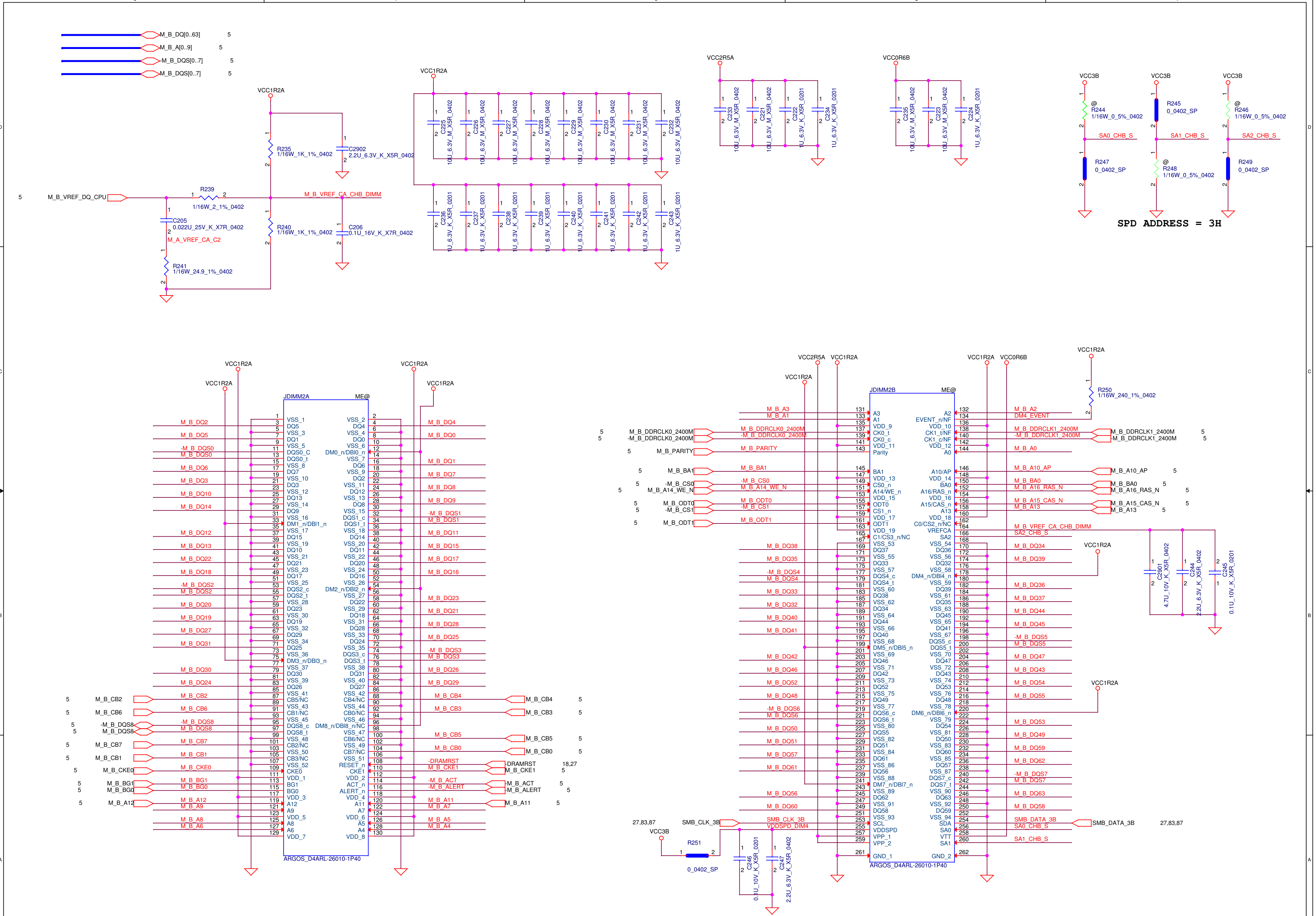



LC Future Center Secret Data

LCFC

| Project Name | TpPv |
|---|---|
| Rev 1.0 | Title DDR |
| Date: Friday, May 15, 2020 | Sheet 27 of 133 |




LC Future Center Secret Data

Project Name: TpPv

Rev: 1.0

Title: DDR

Date: Friday, May 15, 2020

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| LC Future Center Secret Data | Project Name |
|---|---|
| LCFC | TpPv |
| | Rev 1.0 |
| | Title DDR |
| | Date: Friday, May 15, 2020 |
| | Sheet 30 of 133 |

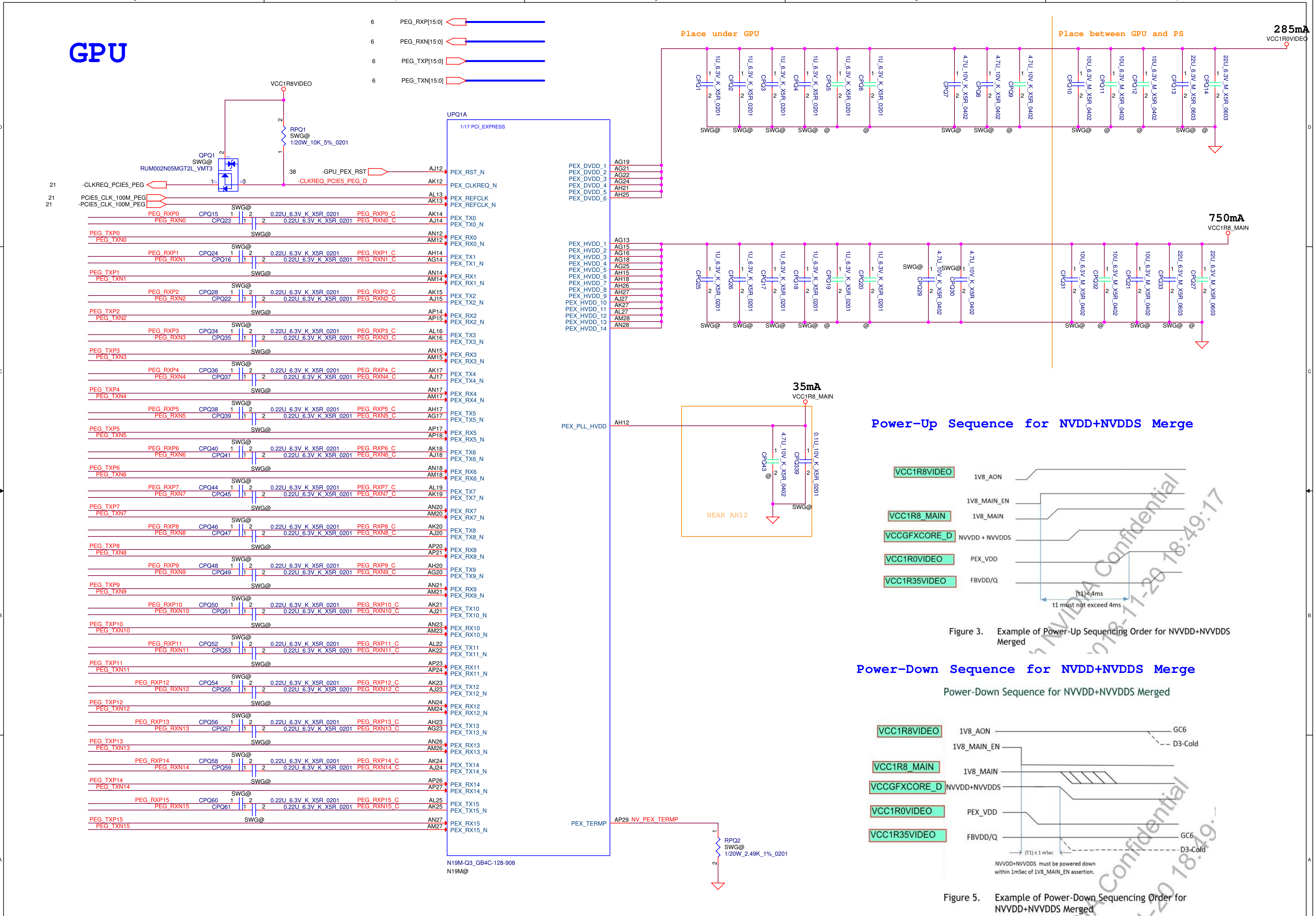



Figure 3. Example of Power-Up Sequencing Order for NVVDD+NVVDDS Merged

Figure 5. Example of Power-Down Sequencing Order for NVVDD+NVVDDS Merged

# GPU

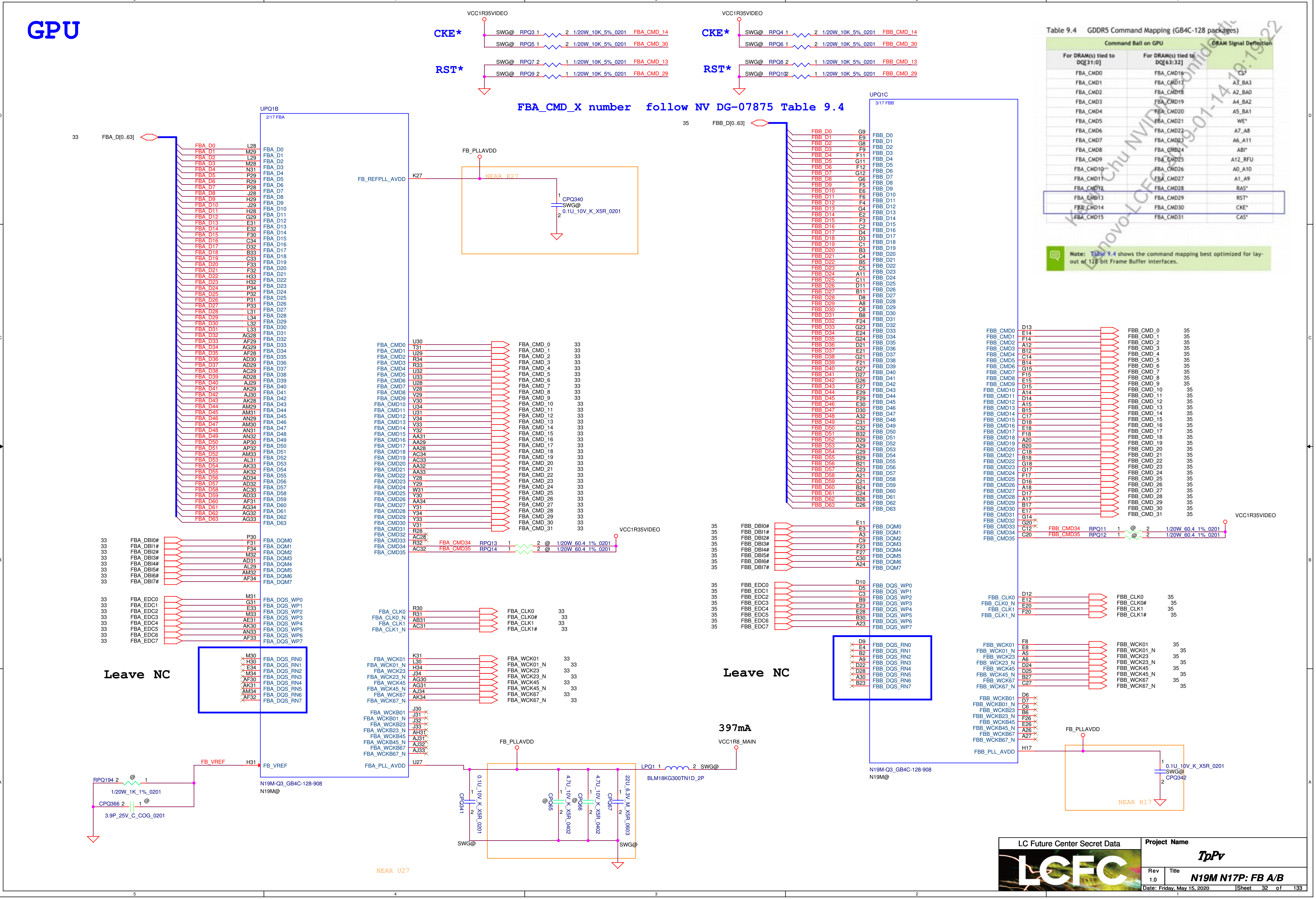



Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

| Command Ball on GPU: For DRAM(s) tied to DQ[31:0] | Command Ball on GPU: For DRAM(s) tied to DQ[63:32] | DRAM Signal Definition |
|---|---|---|
| FBA_CMD0 | FBA_CMD16 | CS* |
| FBA_CMD1 | FBA_CMD17 | A3_BA3 |
| FBA_CMD2 | FBA_CMD18 | A2_BA0 |
| FBA_CMD3 | FBA_CMD19 | A4_BA2 |
| FBA_CMD4 | FBA_CMD20 | A5_BA1 |
| FBA_CMD5 | FBA_CMD21 | WE* |
| FBA_CMD6 | FBA_CMD22 | A7_A8 |
| FBA_CMD7 | FBA_CMD23 | A6_A11 |
| FBA_CMD8 | FBA_CMD24 | ABI* |
| FBA_CMD9 | FBA_CMD25 | A12_RFU |
| FBA_CMD10 | FBA_CMD26 | A0_A10 |
| FBA_CMD11 | FBA_CMD27 | A1_A9 |
| FBA_CMD12 | FBA_CMD28 | RAS* |
| FBA_CMD13 | FBA_CMD29 | RST* |
| FBA_CMD14 | FBA_CMD30 | CKE* |
| FBA_CMD15 | FBA_CMD31 | CAS* |

Note: Table 9.4 shows the command mapping best optimized for lay-out of 128-bit Frame Buffer interfaces.



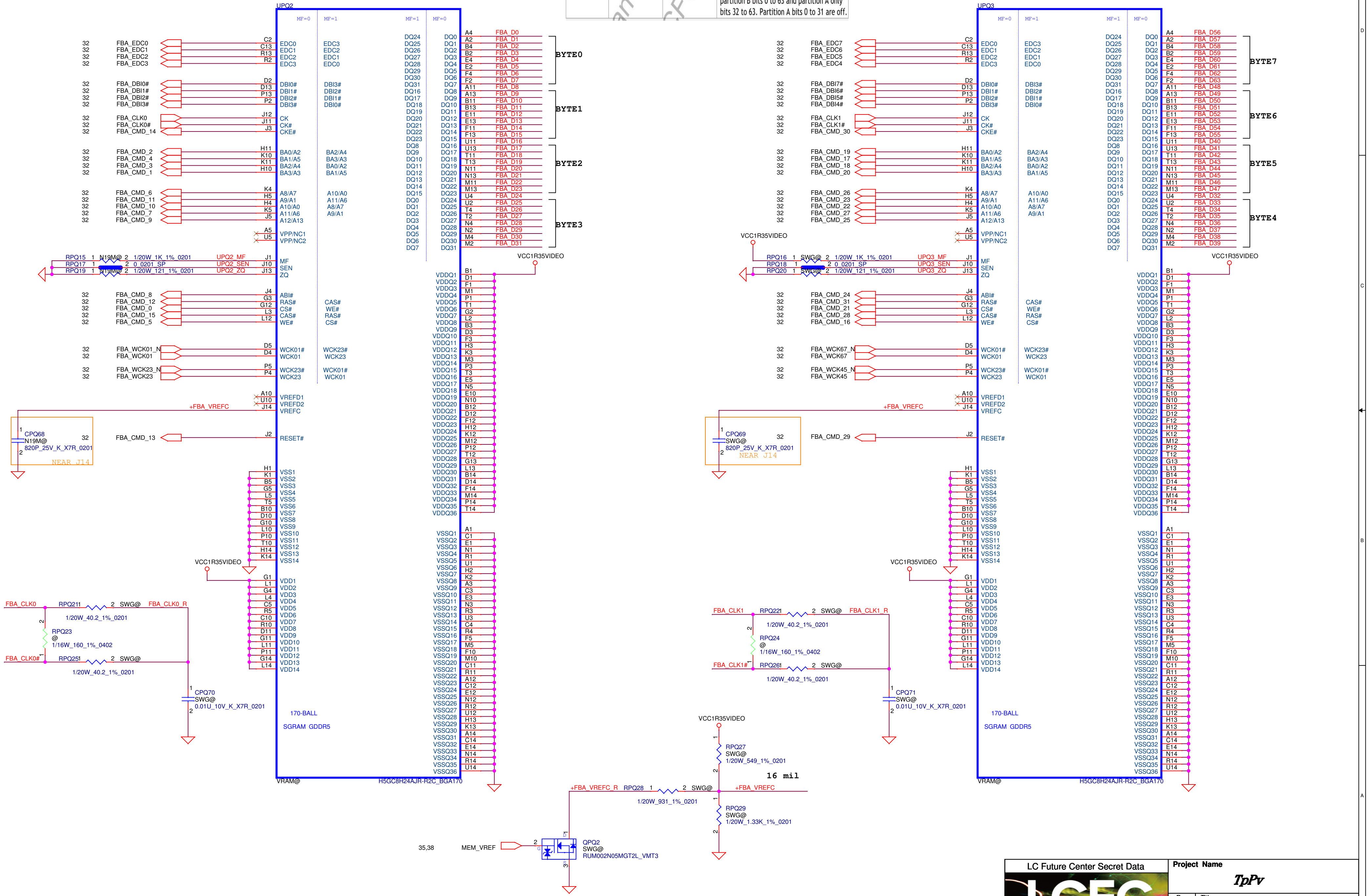


| Project Name | TpPv |
|---|---|
| Rev | 1.0 |
| Title | N19M N17P: FB A/B |
| Date | Friday, May 15, 2020 |
| Sheet | 32 of 133 |

# GPU

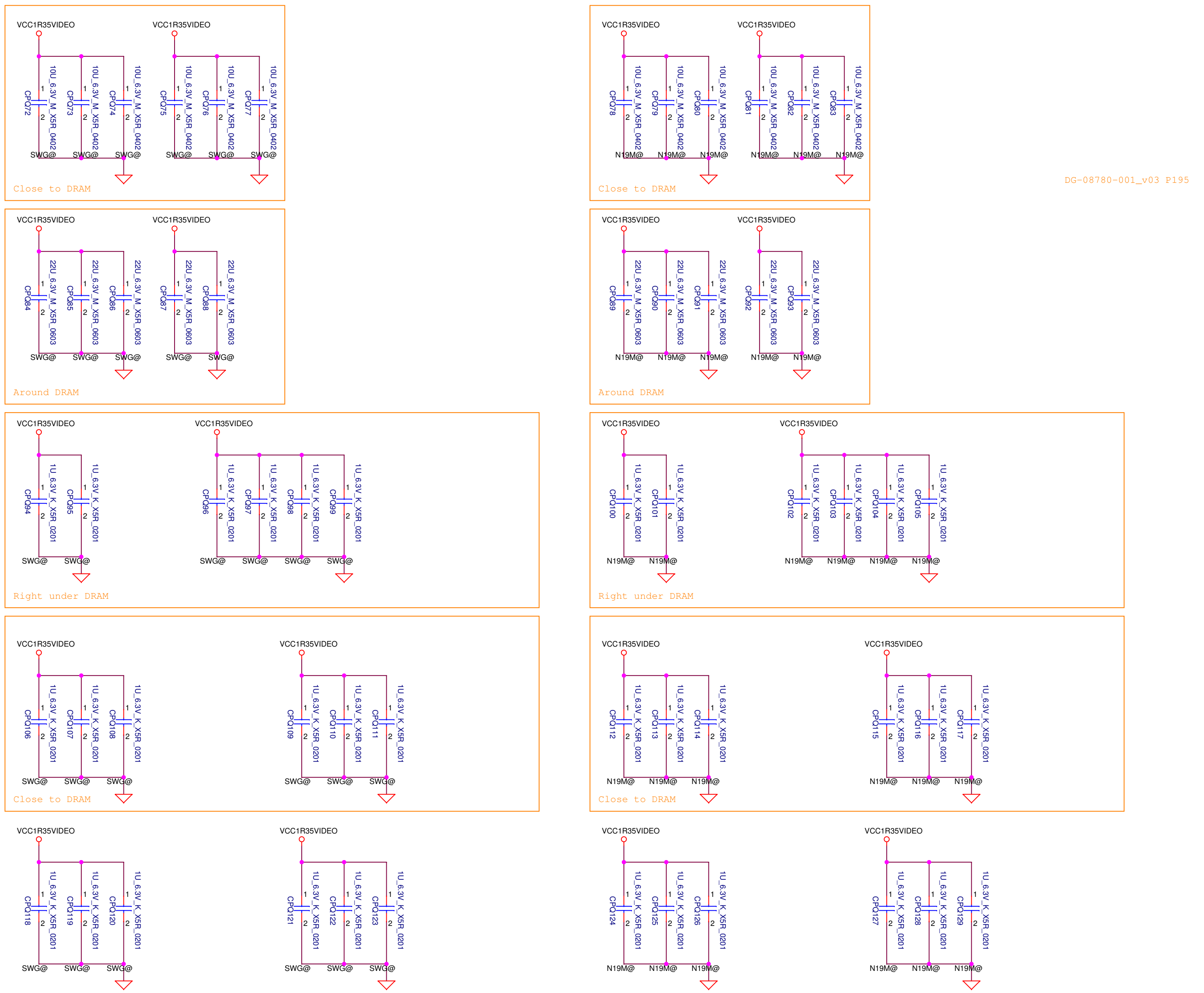
UPQ2 (Fba_D [0....31] no stuff for N17P-G0-K1 GPU

| Products Affected/Ordering Codes | | | |
| --- | --- | --- | --- |
| Product | NVIDIA Part Number [1] | Marketing Part Number for P.O. | Comments |
| N17P-G0-K1 | GP107-726-K1-A1 | N17P-G0-K1-A1 | 29 mm × 29 mm 908 ball BGA (GB4c-128)<br>Supports 96-bit memory interface on partition B bits 0 to 63 and partition A only bits 32 to 63. Partition A bits 0 to 31 are off. |




| LC Future Center Secret Data | Project Name: TpPv |
| --- | --- |
| Rev 1.0 | Title: N19M N17P: VRAM CH_A |
| Date: Friday, May 15, 2020 | Sheet 33 of 133 |

# GPU




LC Future Center Secret Data

Project Name: TpPv

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Title: N19M N17P : VRAM CH_A_CAP

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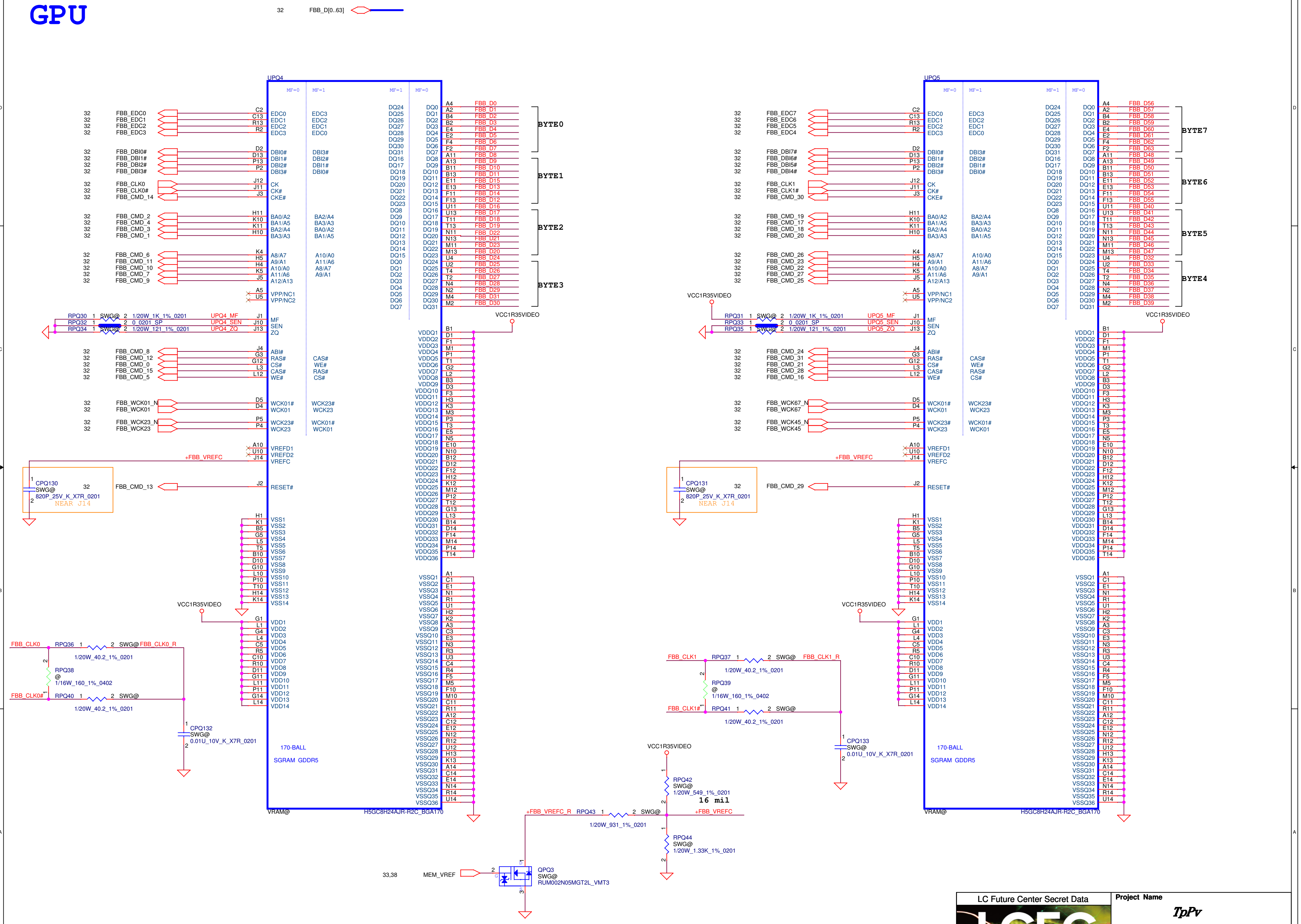
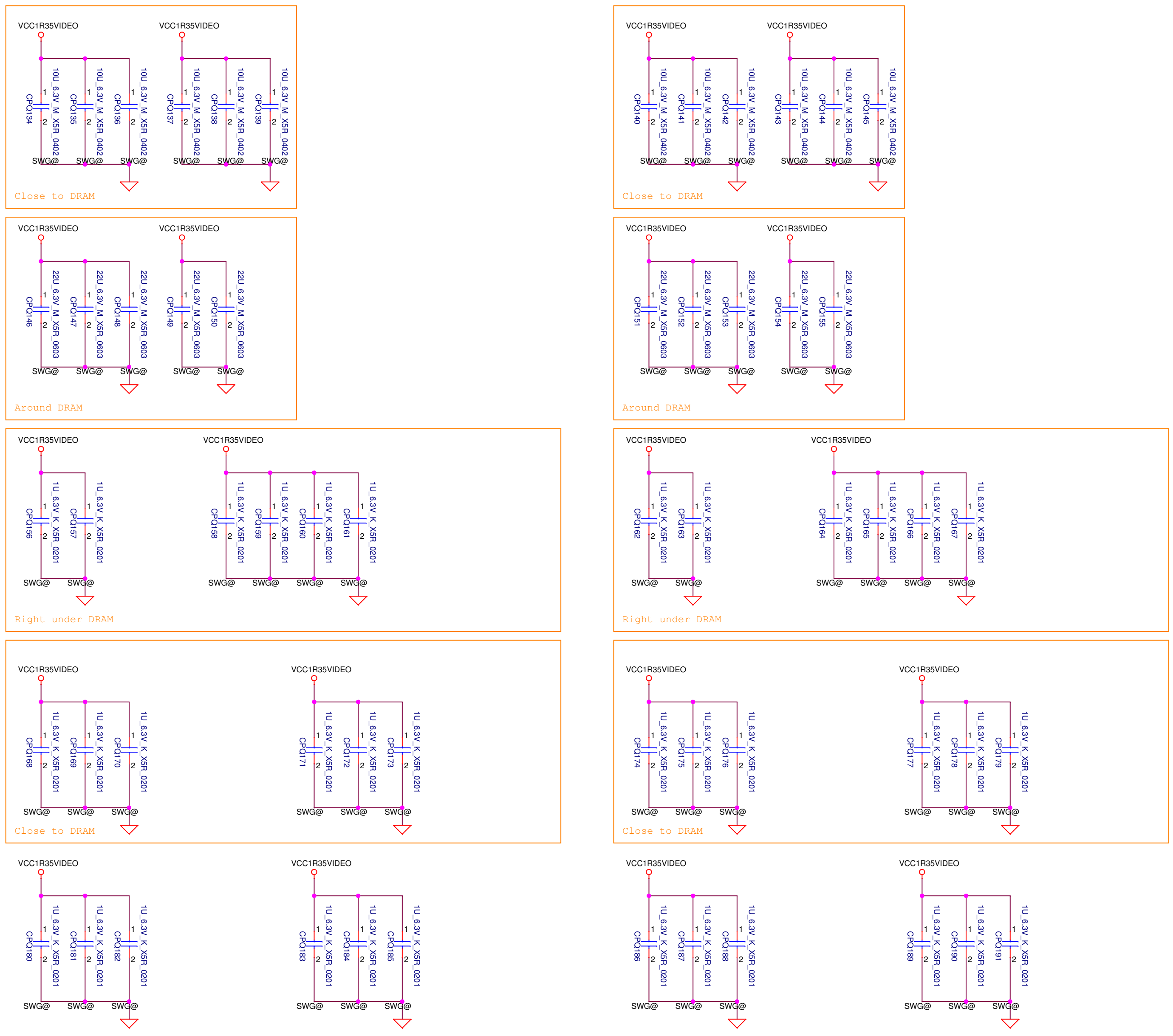
# GPU




LC Future Center Secret Data

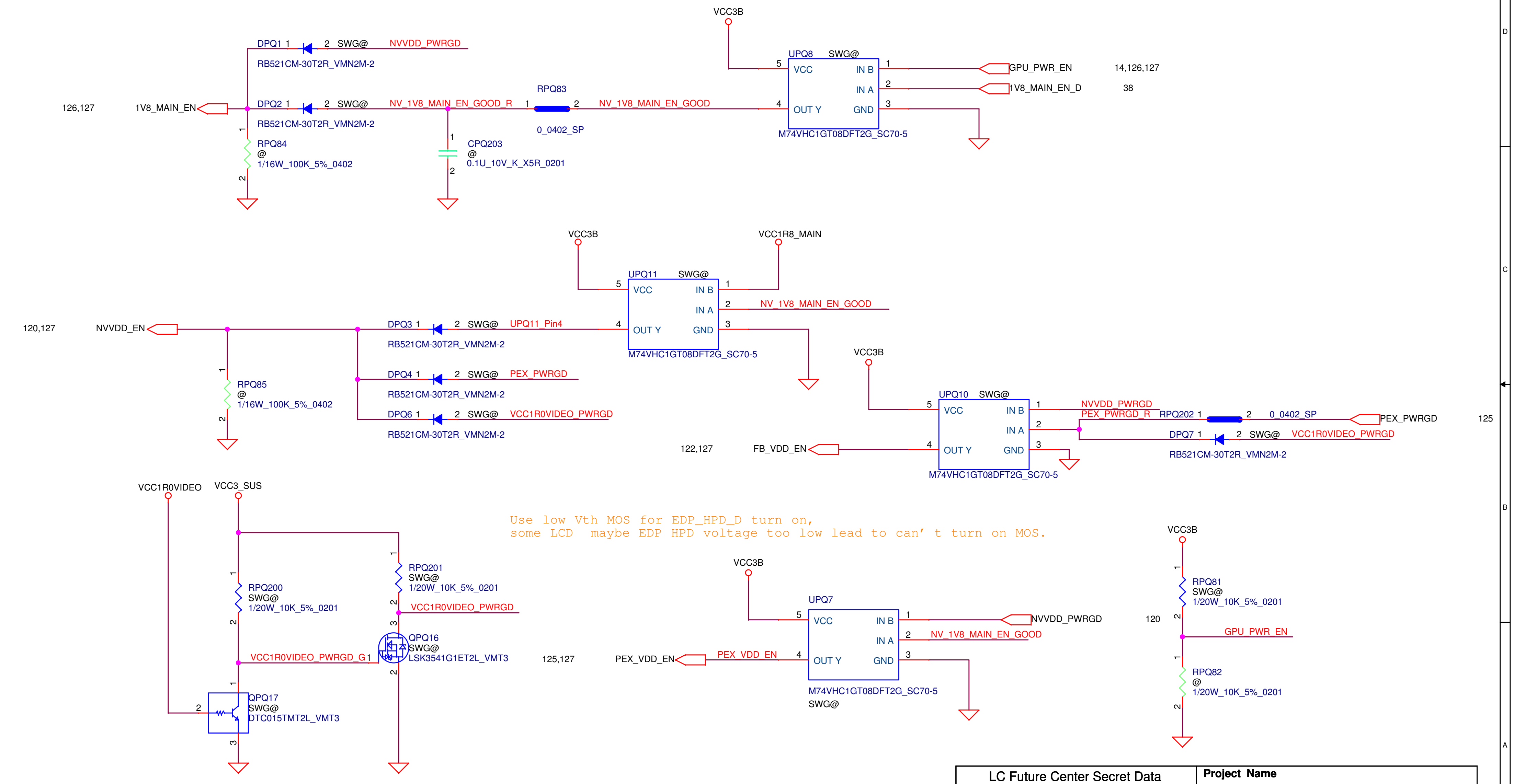
| Project Name | TpPv |
|---|---|
| Rev 1.0 | Title N19M N17P : VRAM CH_B |
| Date: Friday, May 15, 2020 | Sheet 35 of 133 |

# GPU




| LC Future Center Secret Data | Project Name: TpPv |
| --- | --- |
| Rev 1.0 | Title: N19M N17P : VRAM CH_B_CAP |
| Date: Friday, May 15, 2020 | Sheet 36 of 133 |

# GPU




LC Future Center Secret Data

Project Name: TpPv

Rev 1.0

Title: N19M N17P : ENABLE Pin AND GATE

Date: Friday, May 15, 2020

# GPU

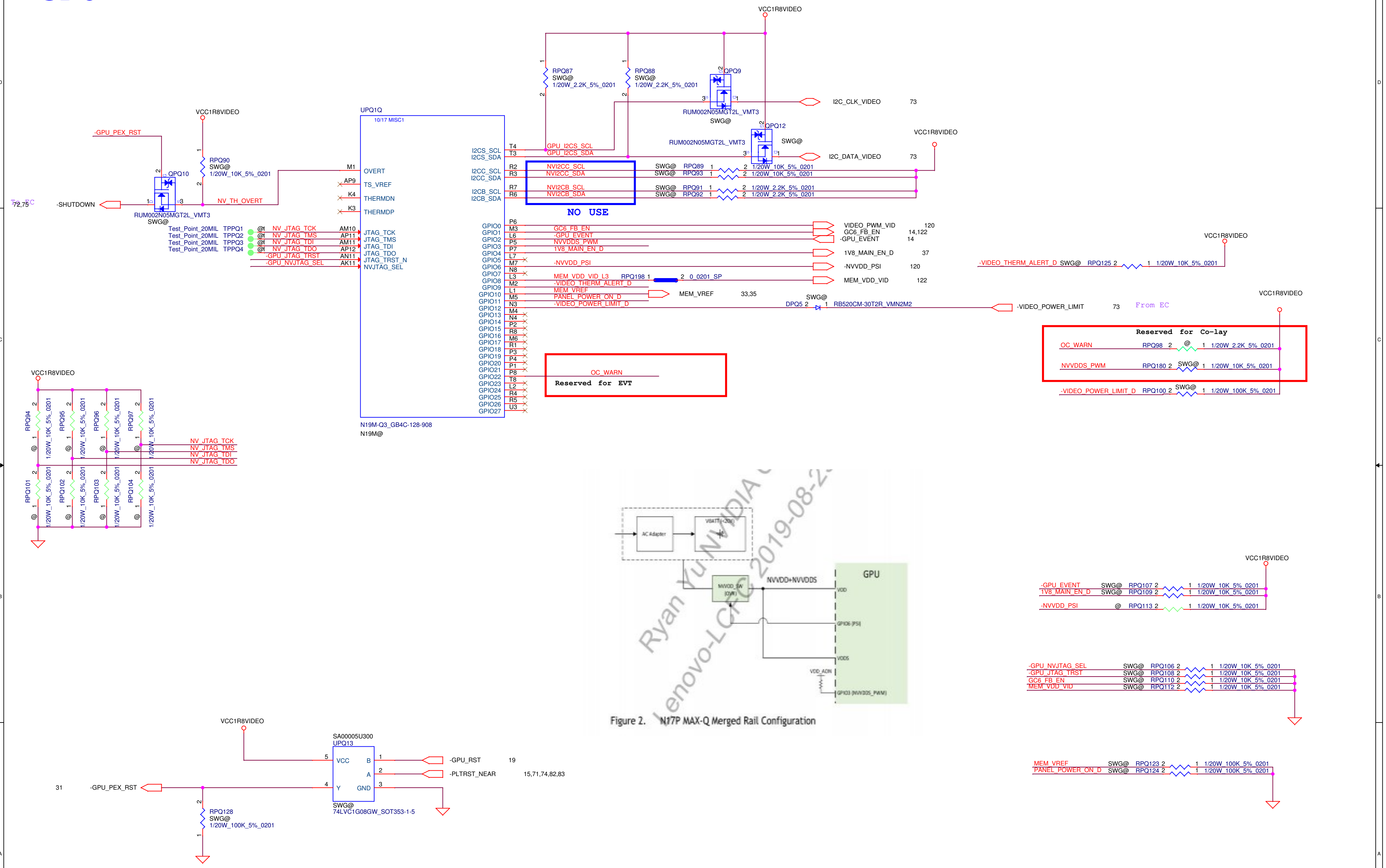


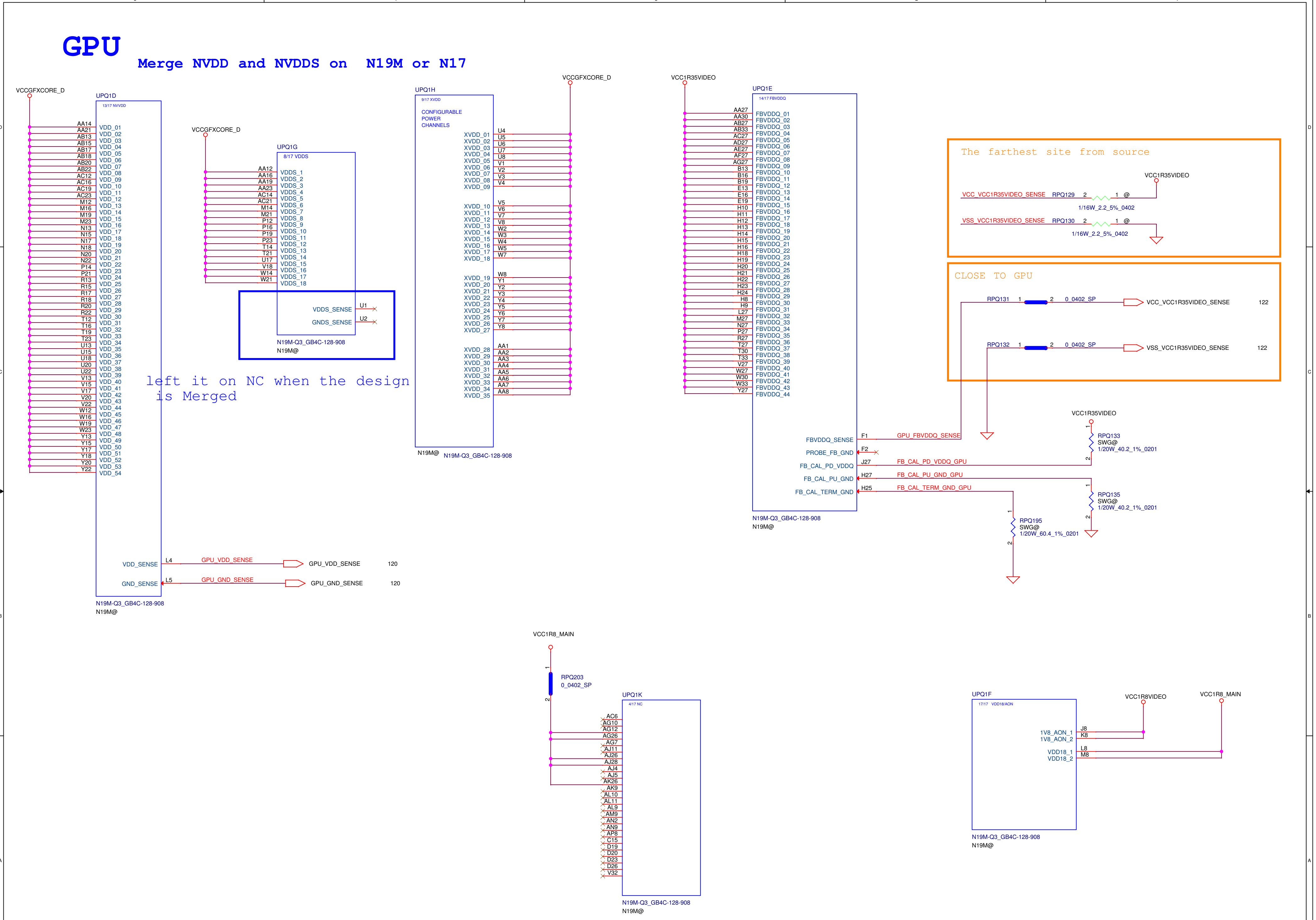

Figure 2. N17P MAX-Q Merged Rail Configuration

LC Future Center Secret Data

| | |
|---|---|
| Project Name | TpPv |
| Rev | 1.0 |
| Title | N19M N17P : GPIO and I2C |
| Date: Friday, May 15, 2020 | Sheet 38 of 133 |

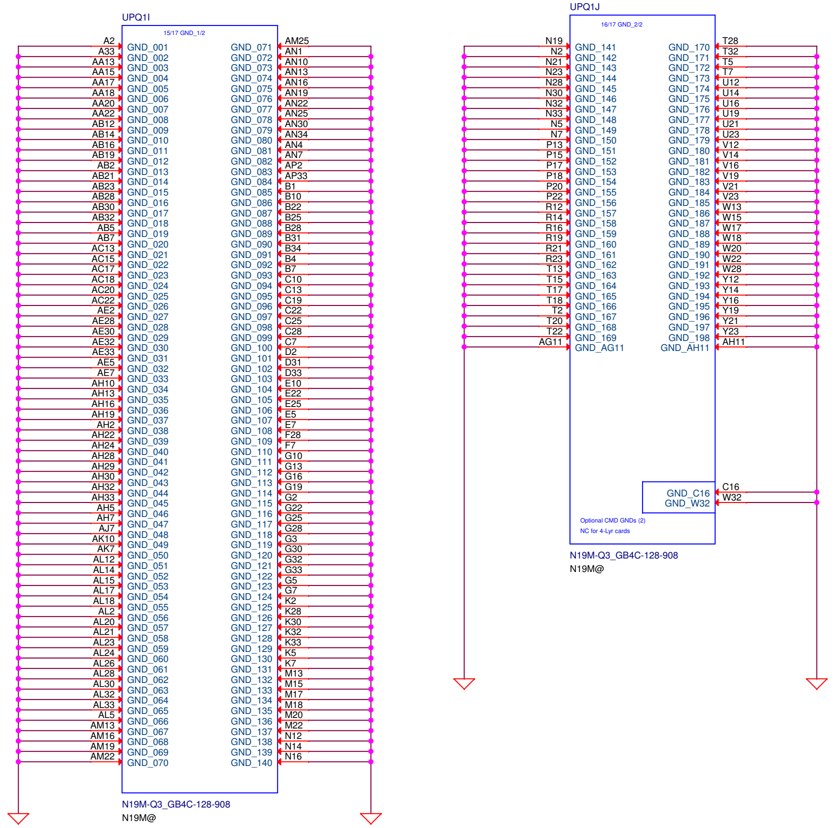
# GPU

Merge NVDD and NVDDS on N19M or N17



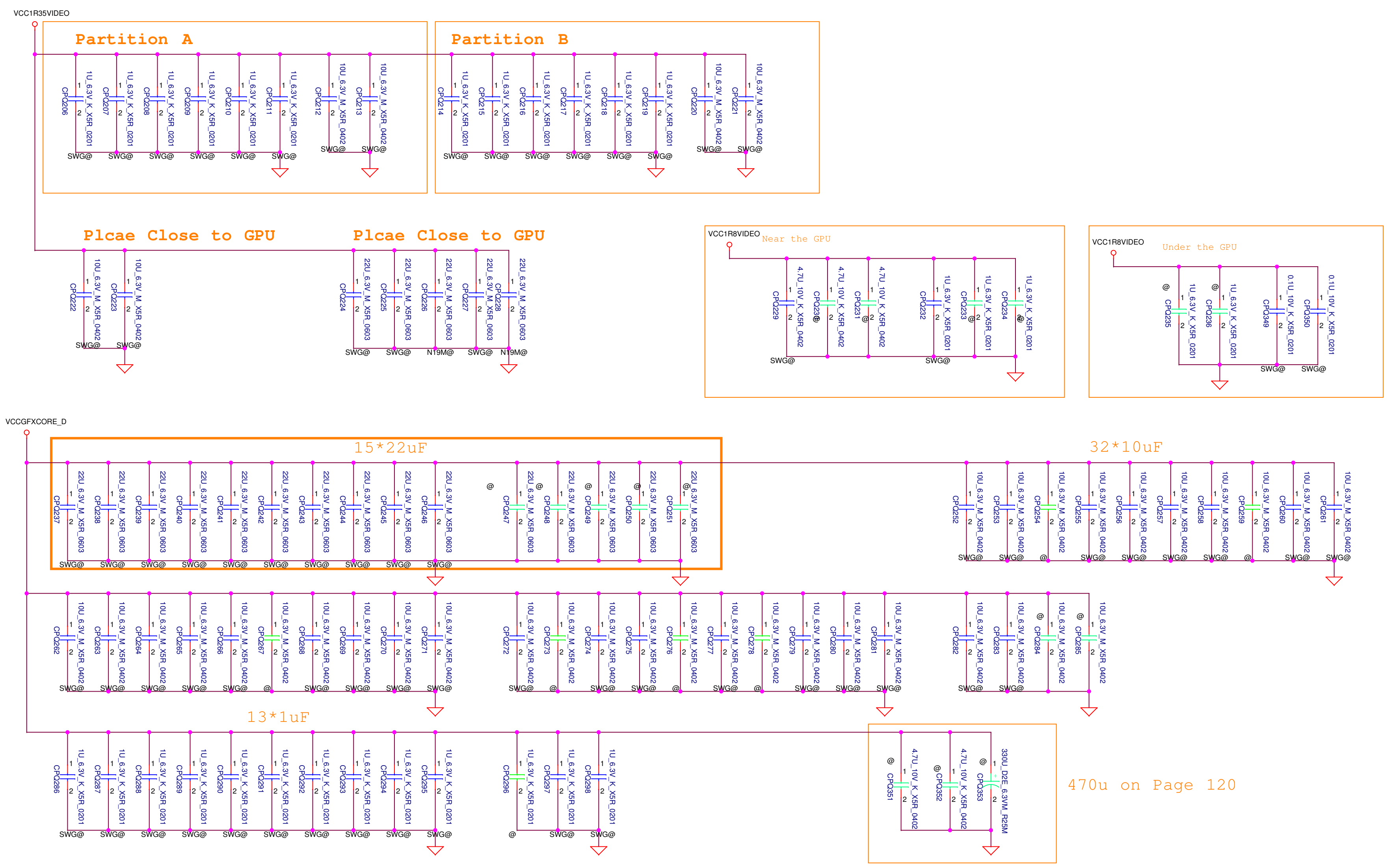

| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| Rev 1.0 | Title: N19M N17P: POWER |
| Date: Friday, May 15, 2020 | Sheet 39 of 133 |

# GPU




| LC Future Center Secret Data | Project Name |
|---|---|
| | TpPv |
| Rev 1.0 | Title N19M N17P : GND |
| Date: Friday, May 15, 2020 | Sheet 40 of 133 |

# GPU




LC Future Center Secret Data

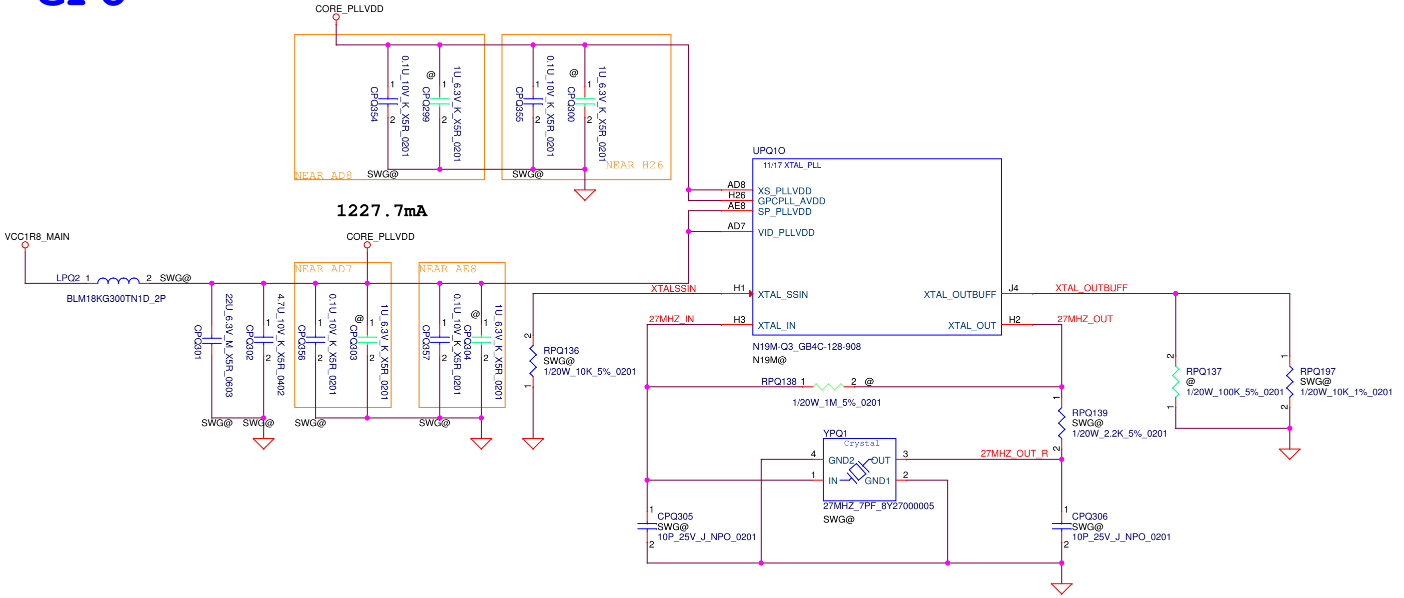
Project Name: TpPv

Rev 1.0

Title: N19M N17P : DECOUPLING (1/2)

Date: Friday, May 15, 2020

# GPU




# IFPA:NC
# IFPB:NC

| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| Rev 1.0 | Title: N19M N17P : IFP A/B and XTAL |
| Date: Friday, May 15, 2020 | Sheet 42 of 133 |

# GPU

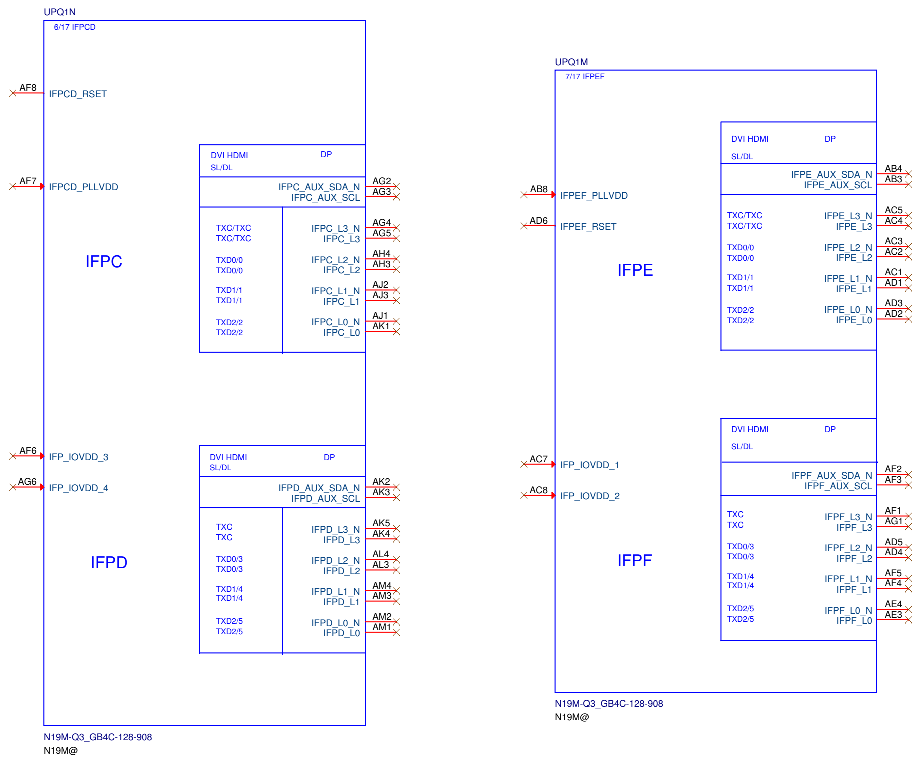



Table 10.1 Digital Display Link Summary

| Digital Display Link | Dual-Link DVI | HDMI | DisplayPort |
|---|---|---|---|
| IFPA (Link A) | ✓(Dual Link with IFPB) | ✓ | ✓ |
| IFPB (Link B) | ✓(Dual Link with IFPA) | ✓ | ✓ |
| IFPC (Link C) | ✓(Dual Link with IFPD) | ✓ | ✓ |
| IFPD (Link D) | (not supported) | (not supported) | eDP Only (no ext. display) |
| IFPE (Link E) | ✓(Dual Link with IFPF) | ✓ | ✓ |
| IFPF (Link F) | ✓(Dual Link with IFPE) | ✓ | ✓ |

# GPU

| Strap Table (GDDR5) | | | | STRAP 0 | | STRAP 1 | | STRAP 2 | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | STRAP0_H@ | STRAP0_L@ | STRAP1_H@ | STRAP1_L@ | STRAP2_H@ | STRAP2_L@ |
| N19M-Q3<br>N17P-G0-K1 | Micron | B | 0x4 | No ASM | ASM | No ASM | ASM | ASM | No ASM |
| | Hynix | A | 0x5 | ASM | No ASM | No ASM | ASM | ASM | No ASM |
| | Samsung | C | 0x3 | ASM | No ASM | ASM | No ASM | No ASM | ASM |

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

| Strap Pins Note 1 | | | Functions Selected by This Strapping | | | |
|---|---|---|---|---|---|---|
| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
| L | L | L | 0 | 0 | 0 | 0 |
| L | L | H | 0 | 0 | 0 | 1 |
| L | H | L | 0 | 0 | 1 | 0 |
| L | H | H | 0 | 0 | 1 | 1 |
| H | L | L | 0 | 1 | 0 | 0 |
| H | L | H | 0 | 1 | 0 | 1 |
| H | H | L | 0 | 1 | 1 | 0 |
| H | H | H | 0 | 1 | 1 | 1 |
| L | L | M | 1 | 0 | 0 | 0 |

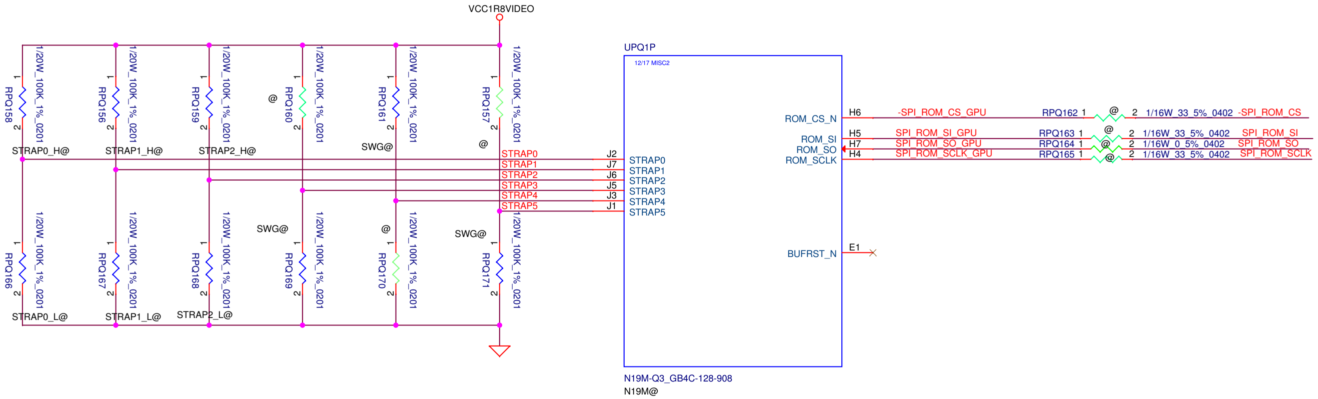
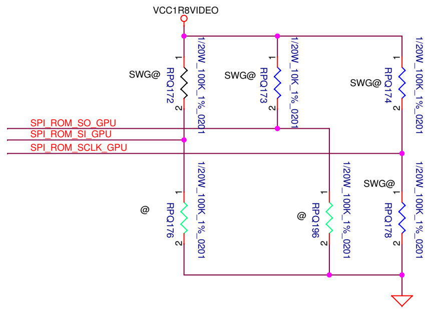



Table 5.3 RAMCFG

| Strap Pins see Note | | | RAMCFG Setting Number |
|---|---|---|---|
| STRAP2 | STRAP1 | STRAP0 | (see Memory RVL for memory configs corresponding to these numbers) |
| L | L | L | 0 (0x0000) |
| L | L | H | 1 (0x0001) |
| L | H | L | 2 (0x0002) |
| L | H | H | 3 (0x0003) |
| H | L | L | 4 (0x0004) |
| H | L | H | 5 (0x0005) |
| H | H | L | 6 (0x0006) |
| H | H | H | 7 (0x0007) |
| L | L | M | 8 (0x0008) |
| L | M | L | 9 (0x0009) |
| L | M | H | 10 (0x000A) |
| L | H | M | 11 (0x000B) |
| M | L | L | 12 (0x000C) |
| M | L | H | 13 (0x000D) |
| M | H | L | 14 (0x000E) |
| M | H | H | 15 (0x000F) |
| H | L | M | 16 (0x0010) |
| H | M | L | 17 (0x0011) |
| H | M | H | 18 (0x0012) |
| H | H | M | 19 (0x0013) |
| L | M | M | 20 (0x0014) |
| M | L | M | 21 (0x0015) |
| M | M | L | 22 (0x0016) |
| M | M | H | 23 (0x0017) |
| M | H | M | 24 (0x0018) |
| H | M | M | 25 (0x0019) |
| M | M | M | 26 (0x001A) |

Note: The ternary strap pins listed in the STRAP columns must be pulled to one of three voltage levels. "L" means Low level (GND). "M" means middle level (0.9V). "H" means High level (1.8V).



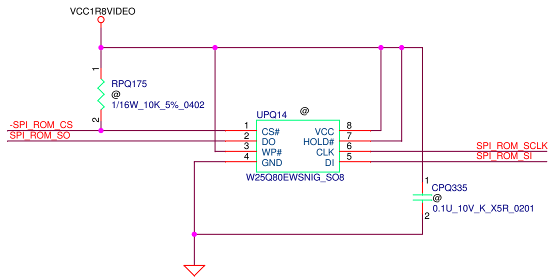
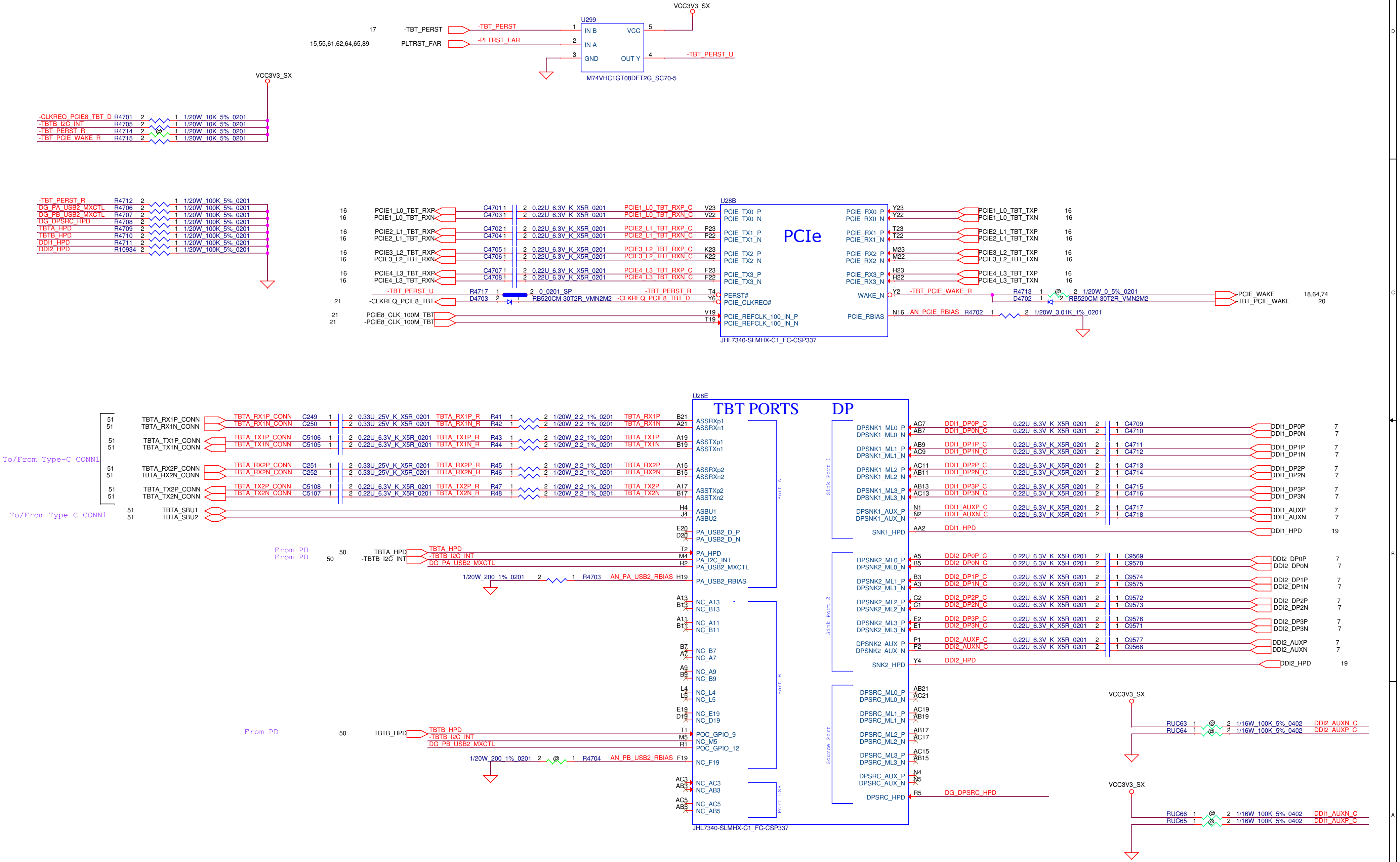




Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

| Row Index | Strap Pins see Note | | | Resulting SORx_EXPOSED Enablements | | | |
|---|---|---|---|---|---|---|---|
| | ROM_SO | ROM_SI | ROM_SCLK | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| 15 | L | L | L | ENABLED | ENABLED | ENABLED | ENABLED |
| 14 | L | L | H | ENABLED | ENABLED | ENABLED | disabled |
| 13 | L | H | L | ENABLED | ENABLED | disabled | ENABLED |
| 12 | L | H | H | ENABLED | ENABLED | disabled | disabled |
| 8 | H | H | H | ENABLED | disabled | disabled | disabled |
| 0 | H | H | M | disabled | disabled | disabled | disabled |
| | M | X | X | (Reserved; do not configure) | | | |
| | All other Strap Configurations | | | (Reserved) | | | |

| LC Future Center Secret Data | Project Name: TpPv |
| --- | --- |
| LCFC | Rev 1.0 — Title: BLANK |
| | Date: Friday, May 15, 2020 — Sheet 45 of 133 |

# TUNDERBOLT




LC Future Center Secret Data

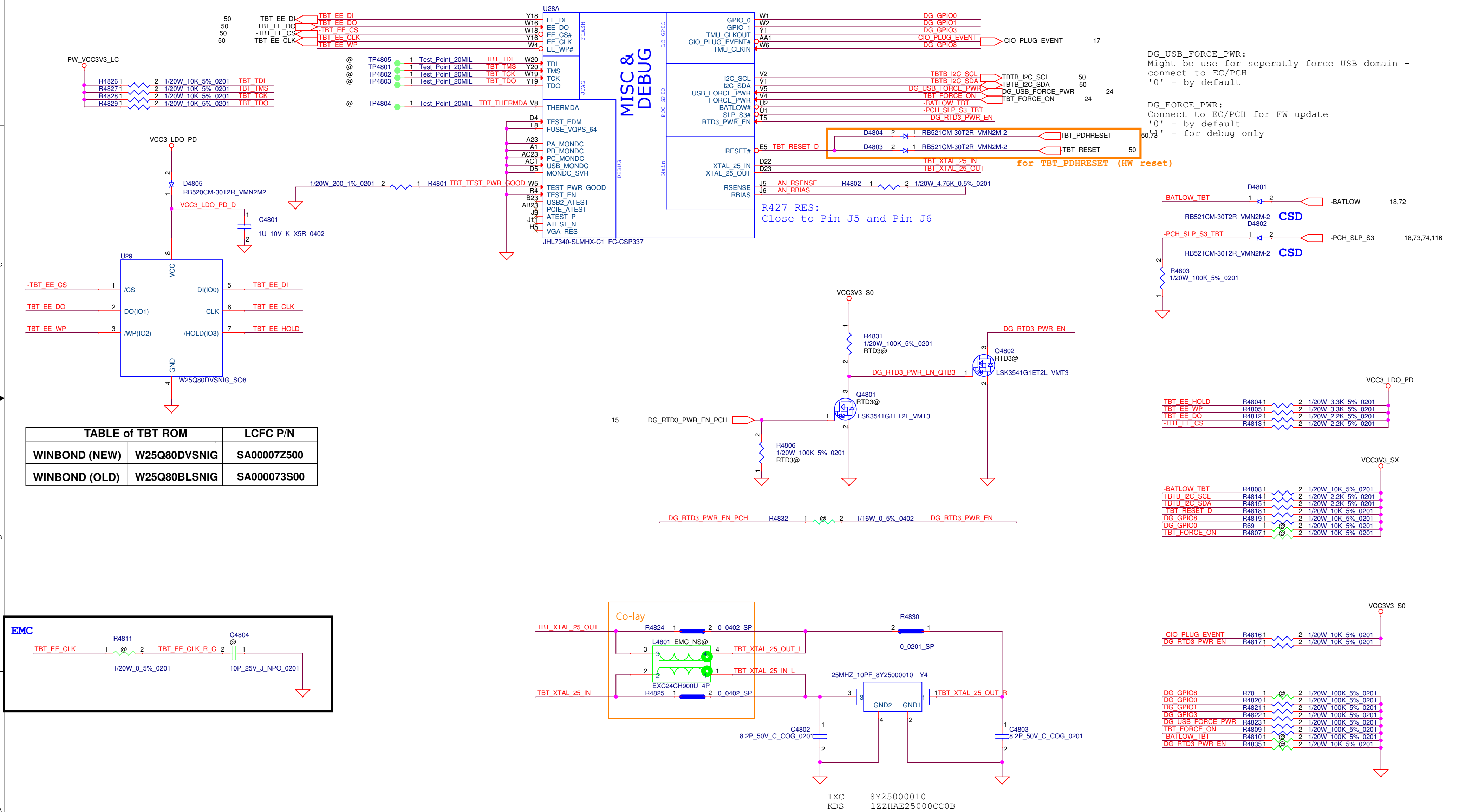
Project Name: TpPv

Rev 1.0

Title: Titan Ridge (1/3)

Date: Friday, May 15, 2020

# TUNDERBOLT




DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain -connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

| TABLE of TBT ROM | | LCFC P/N |
|---|---|---|
| WINBOND (NEW) | W25Q80DVSNIG | SA00007Z500 |
| WINBOND (OLD) | W25Q80BLSNIG | SA000073S00 |

LC Future Center Secret Data

Project Name: TpPv

Rev 1.0

Title: Titan Ridge (2/3)

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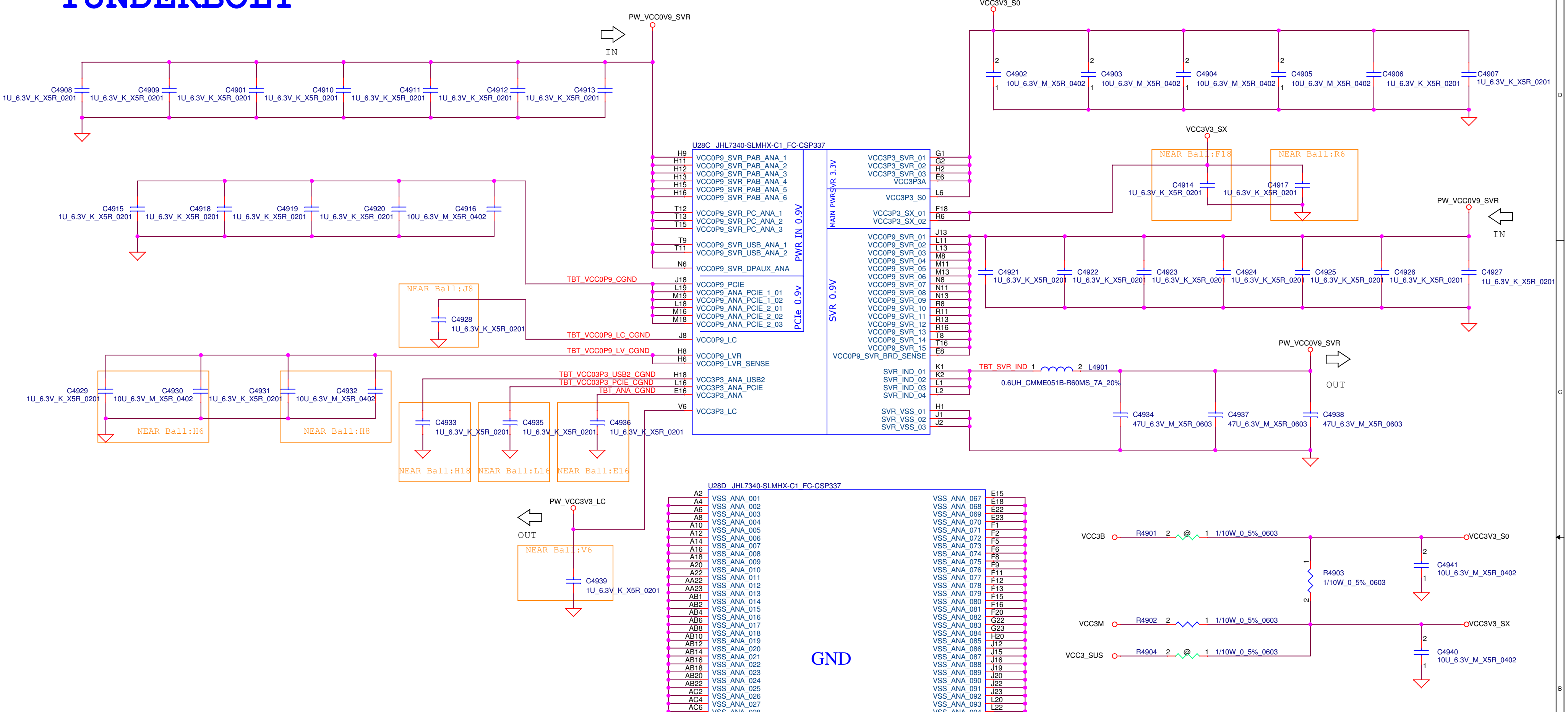
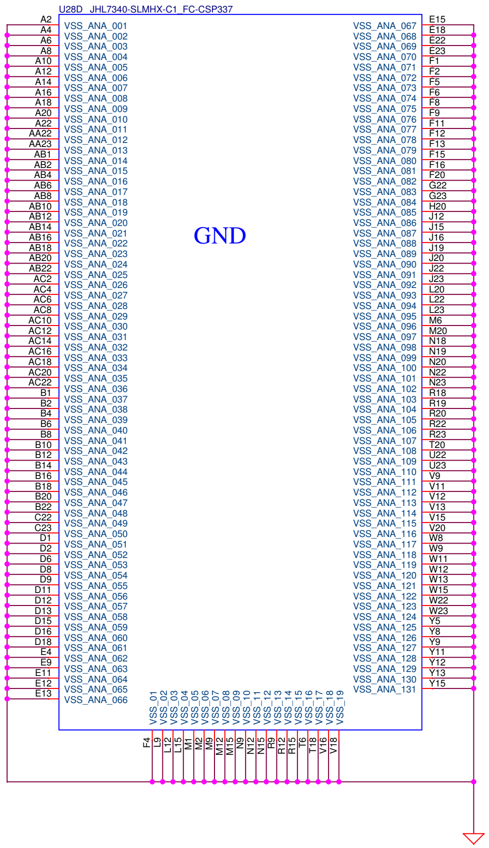
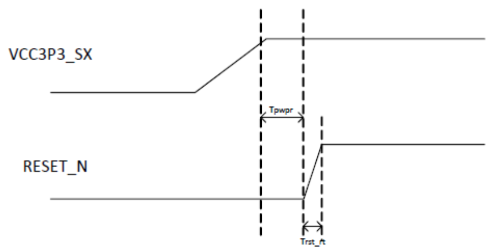
# TUNDERBOLT




## Power On Sequence




## Power On Sequence

| Parameter | Description | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| Tpwpr | From VCC3P3_SX at 90% to RESET_N de-assertion | 100 | - | us | |
| Trst_rt | RESET_N rise time | 0.1 | 500 | ns | |

LC Future Center Secret Data

Project Name: TpPv

Rev: 1.0

Title: Titan Ridge (3/3)

Date: Friday, May 15, 2020

# POWER DELIVERY

ADCIN1 BUS POWER CONFIGURATION

| DIV = PDR3 / (PDR1 + PDR3) | | CONFIGURATION |
|---|---|---|
| DIV MIN | DIV MAX | |
| 0.00 | 0.18 | BP_NoResponse |
| 0.20 | 0.38 | BP_WaitFor3V3_Internal |
| 0.40 | 0.58 | BP_WaitFor3V3_External |
| 0.60 | 1.00 | BP_NoWait |

← LOGIC

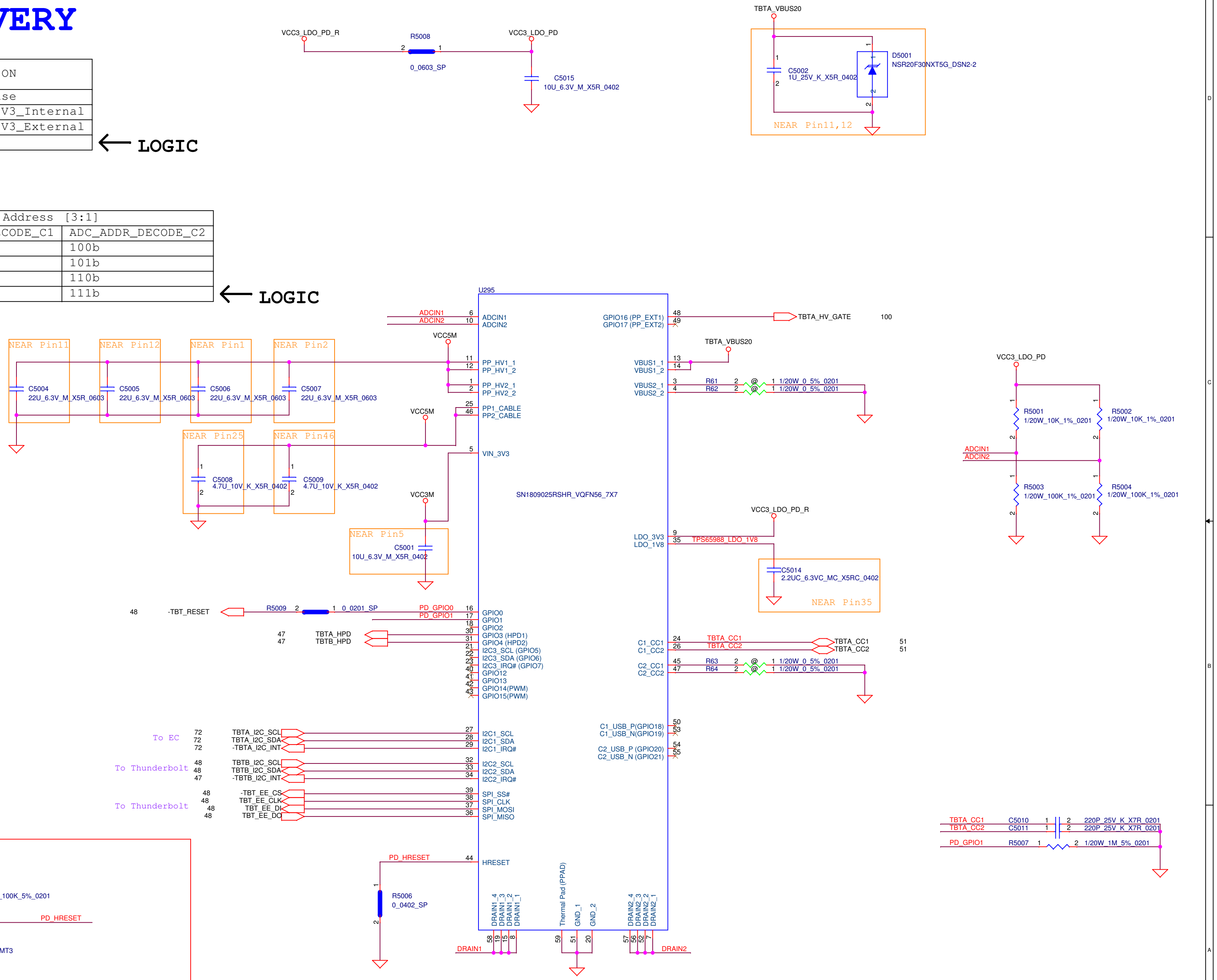
ADCIN2 I2C Address Setting

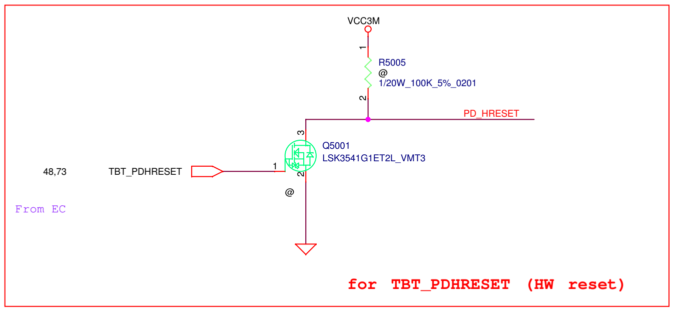
| DIV = PDR4 / (PDR2 + PDR4) | | I2C Unique Address [3:1] | |
|---|---|---|---|
| DIV MIN | DIV MAX | ADC_ADDR_DECODE_C1 | ADC_ADDR_DECODE_C2 |
| 0.00 | 0.18 | 000b | 100b |
| 0.20 | 0.38 | 001b | 101b |
| 0.40 | 0.58 | 010b | 110b |
| 0.60 | 1.00 | 011b | 111b |

← LOGIC

I2C Address

| | | |
|---|---|---|
| I2C1 (to EC) | TBT PORT | 0X23 |
| | USBC PORT | 0X27 |
| I2C2 (to TR) | TBT PORT | 0X38 |
| | USBC PORT | 0X3F |




LC Future Center Secret Data

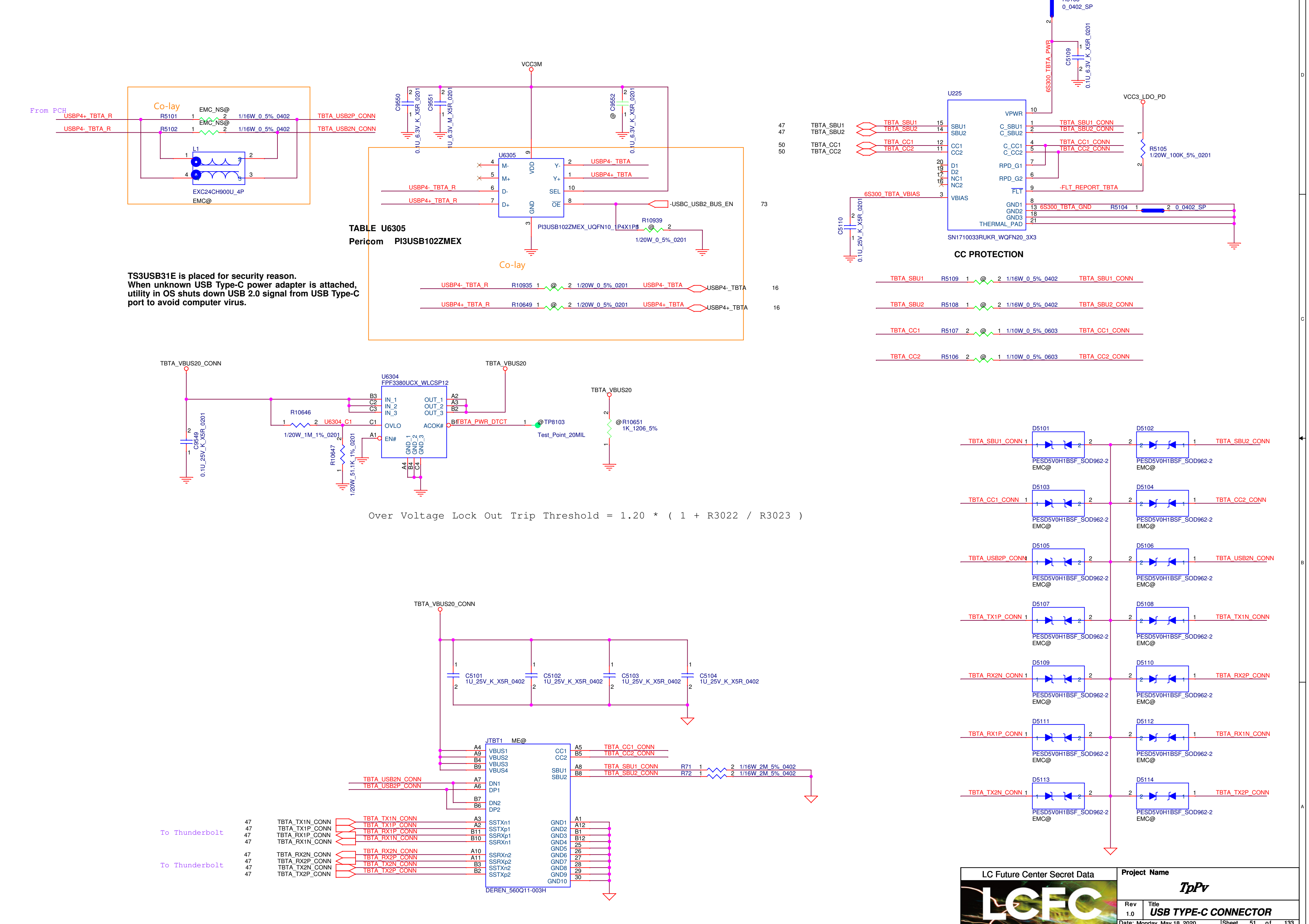
Project Name: TpPv

Rev 1.0

Title: POWER DELIVERY (TPS65988)

Date: Friday, May 15, 2020

# USB TYPE-C CONN 1(Thunderbolt)



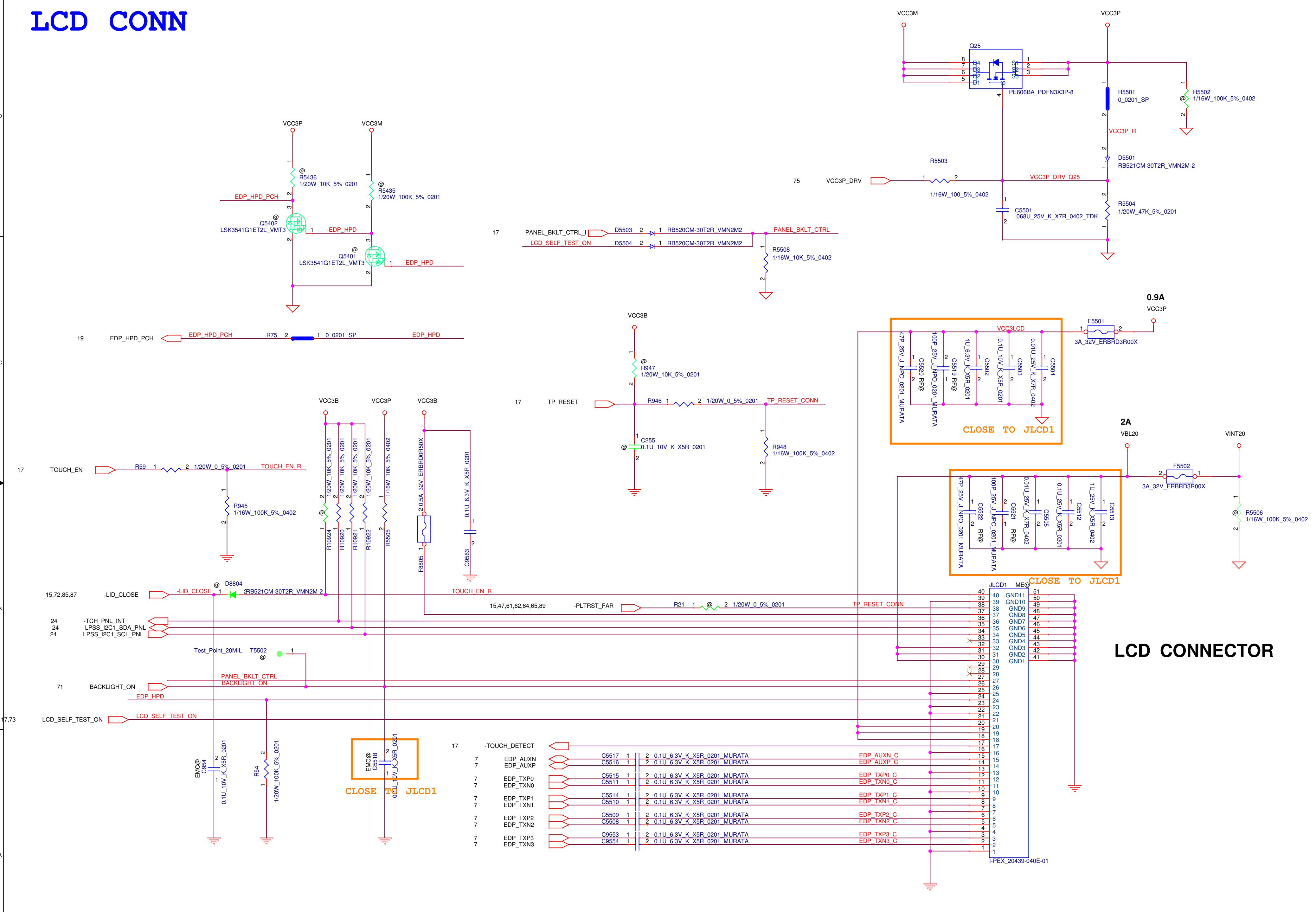

| LC Future Center Secret Data | Project Name |
|---|---|
| LCFC | TpPv |
| Rev 1.0 | Title: USB TYPE-C CONNECTOR |
| Date: Monday, May 18, 2020 | Sheet 51 of 133 |

BLANK

BLANK

# BLANK

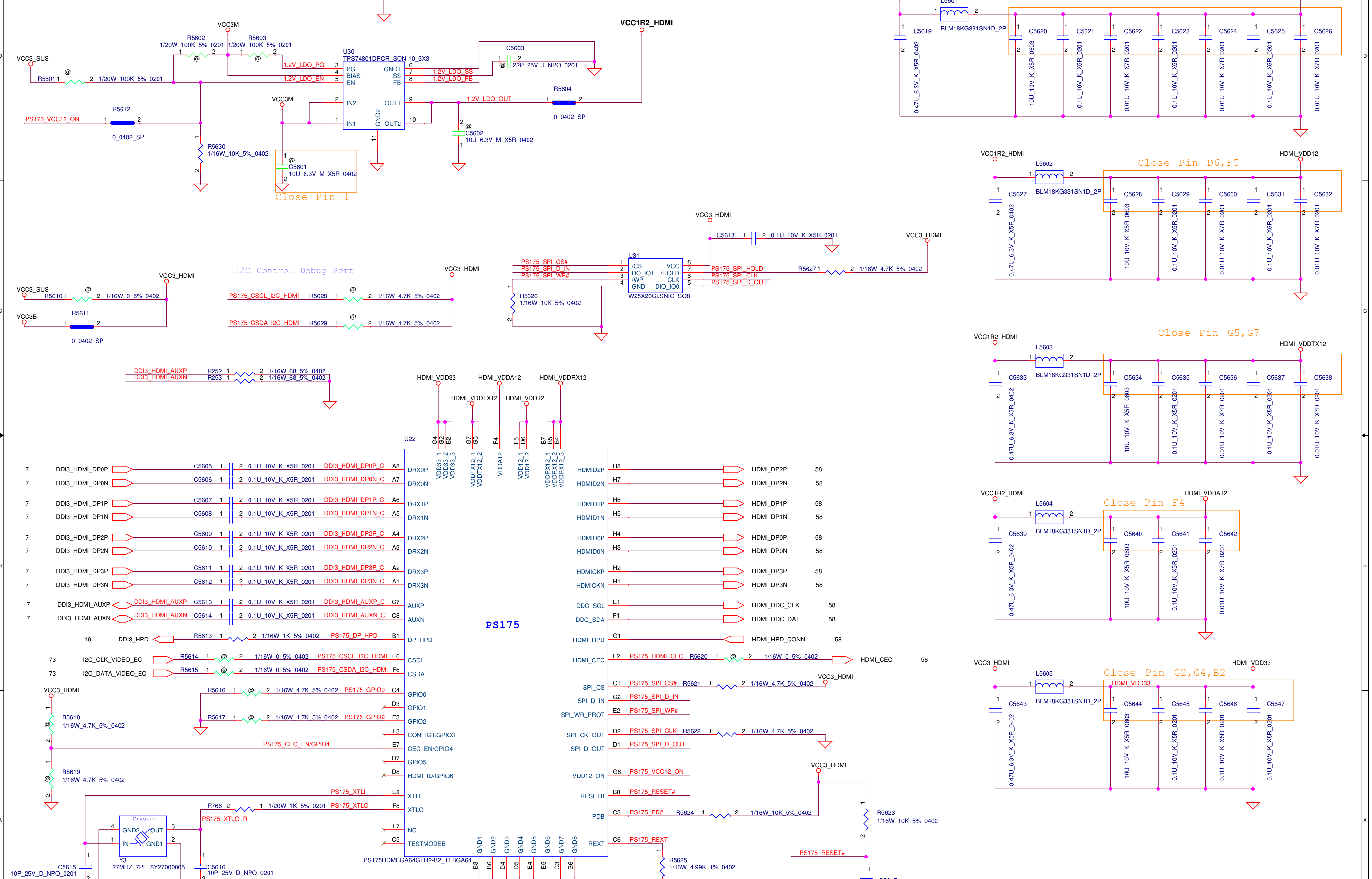
# LCD CONN




| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| LCFC | Rev 1.0 — Title: LCD CONNECTOR |
| | Date: Friday, May 15, 2020 — Sheet 55 of 133 |

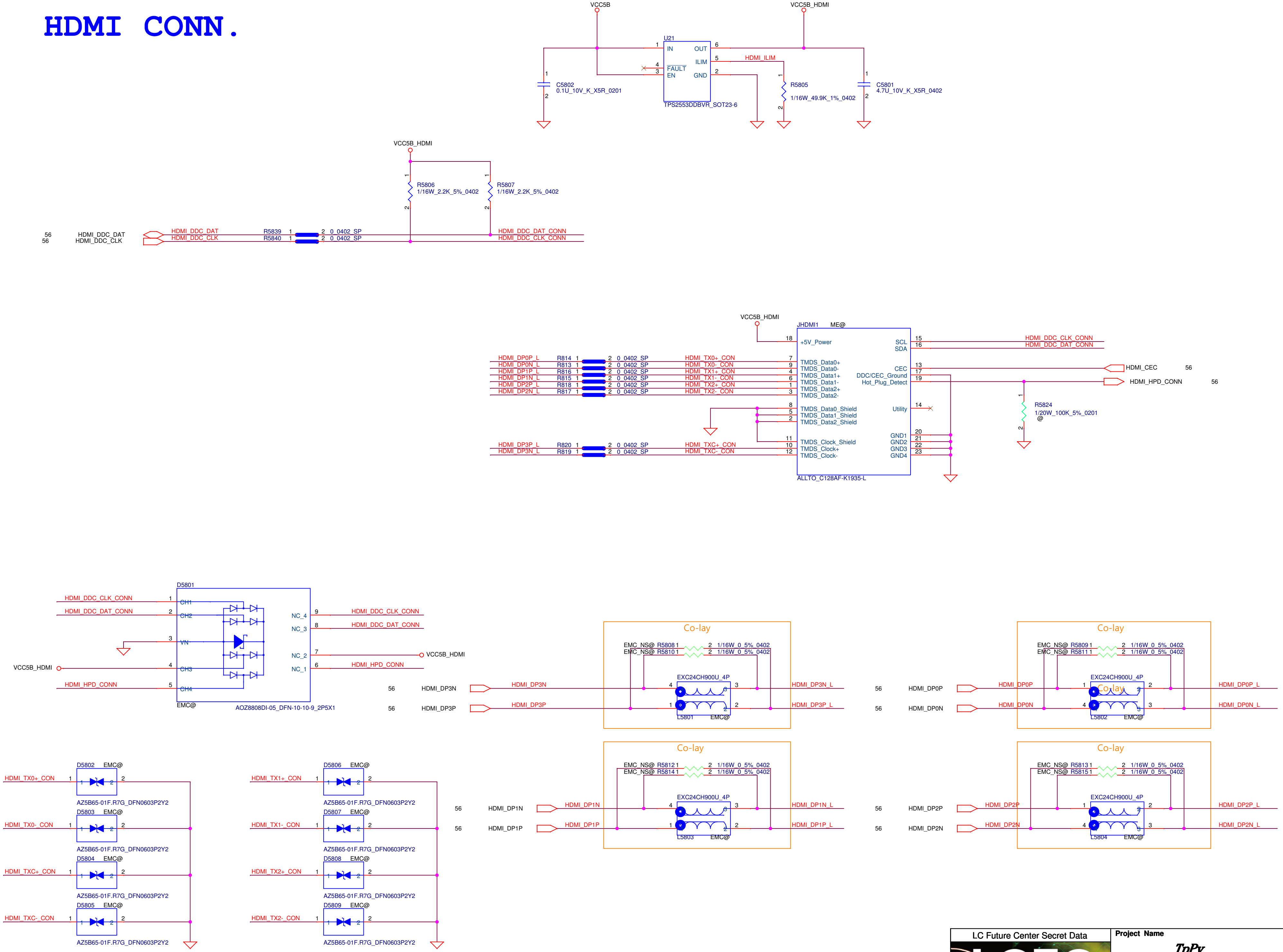
# HDMI LSPCON

same HDMI retimer 1.2V source.




| LC Future Center Secret Data | Project Name TpPv |
|---|---|
| LCFC | Rev 1.0 / Title HDMI LSPCON |
| | Date: Friday, May 15, 2020 / Sheet 56 of 133 |

# HDMI CONN.




| LC Future Center Secret Data | Project Name: TpPv |
| --- | --- |
| LCFC | Rev 1.0 — Title: HDMI CONNECTOR |
| | Date: Friday, May 15, 2020 — Sheet 58 of 133 |

5 4 3 2 1

D

C

B

A

LC Future Center Secret Data

Project Name

*TpPv*

| Rev | Title |
|---|---|
| 1.0 | ***BLANK*** |

Date: Friday, May 15, 2020 | Sheet 59 of 133

LC Future Center Secret Data

Project Name

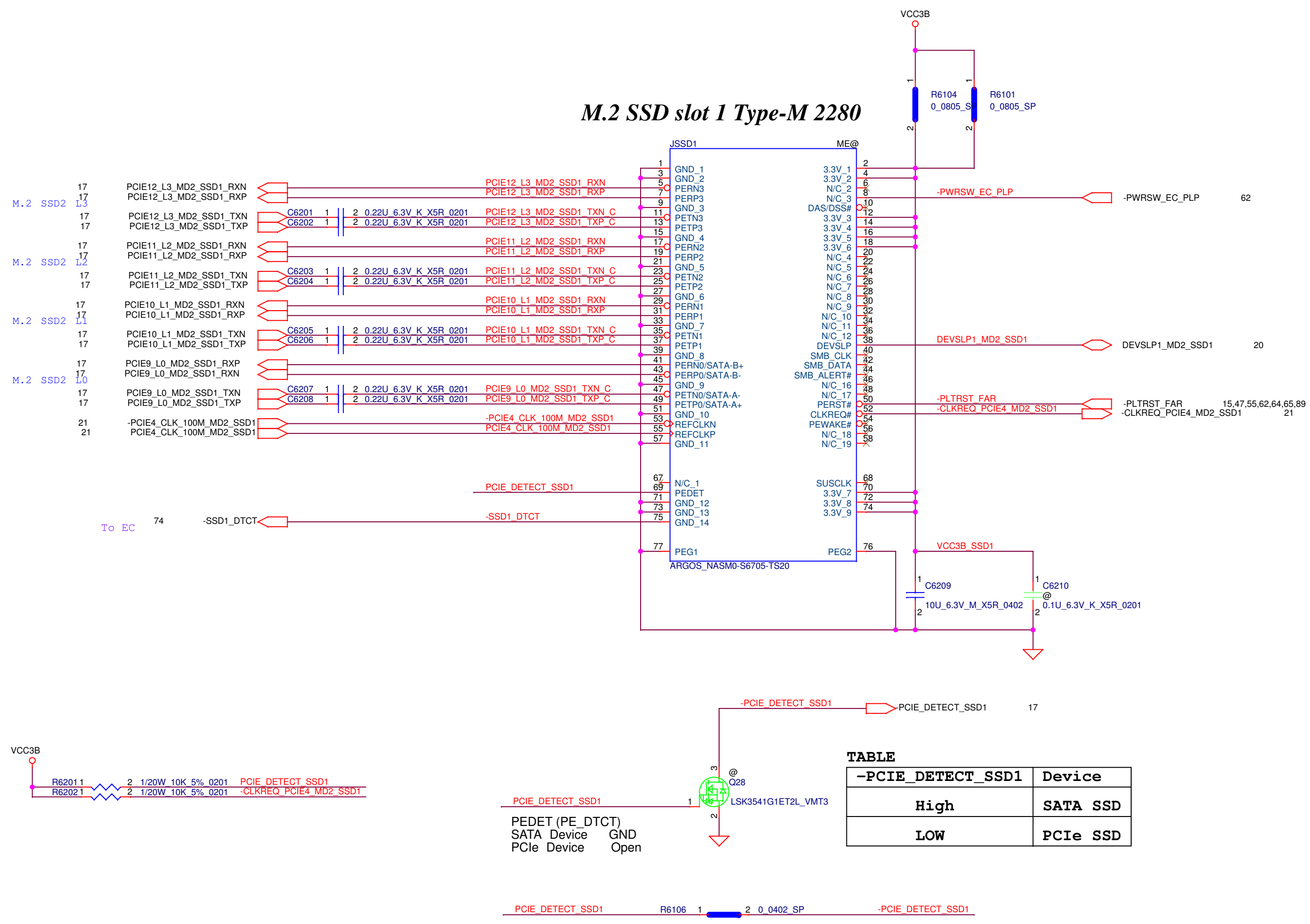
TpPv

Rev 1.0

Title BLANK

Date: Friday, May 15, 2020

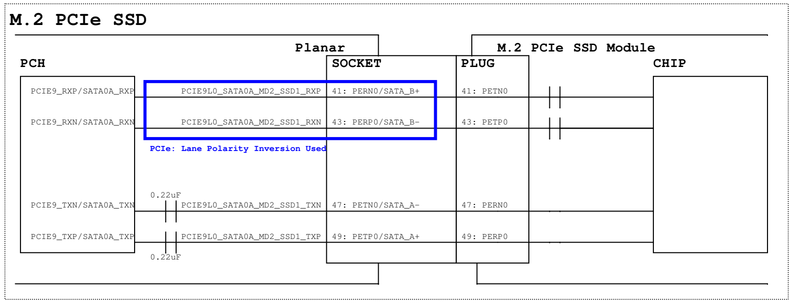
# M.2 SSD

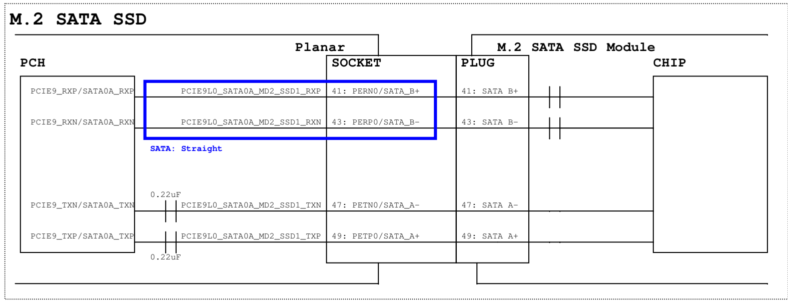



TABLE

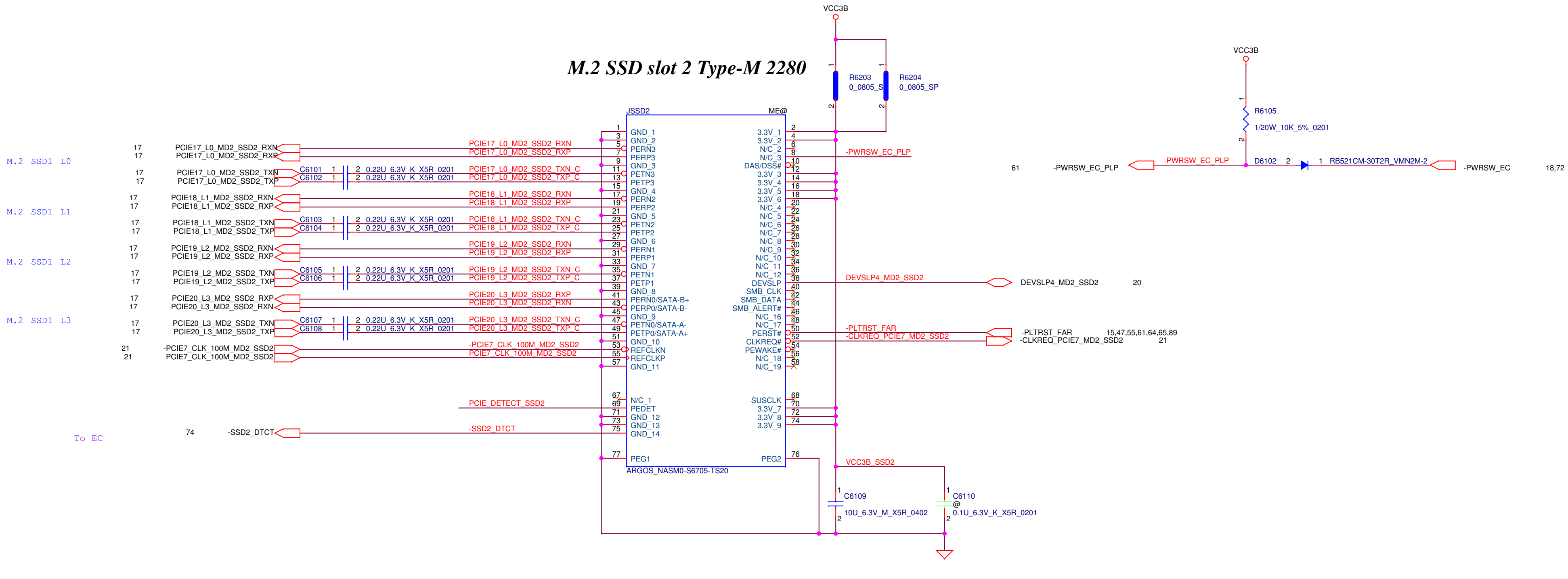
| -PCIE_DETECT_SSD1 | Device |
|---|---|
| High | SATA SSD |
| LOW | PCIe SSD |

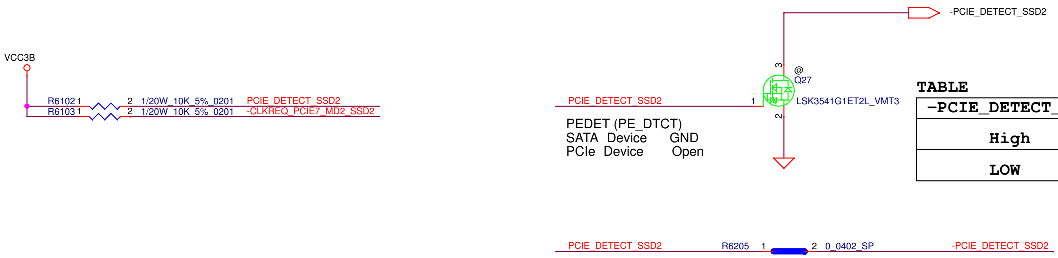
# M.2 SSD




## M.2 SSD slot 2 Type-M 2280




TABLE

| -PCIE_DETECT_SSD2 | Device |
|---|---|
| High | SATA SSD |
| LOW | PCIe SSD |

LC Future Center Secret Data

Project Name: TpPv

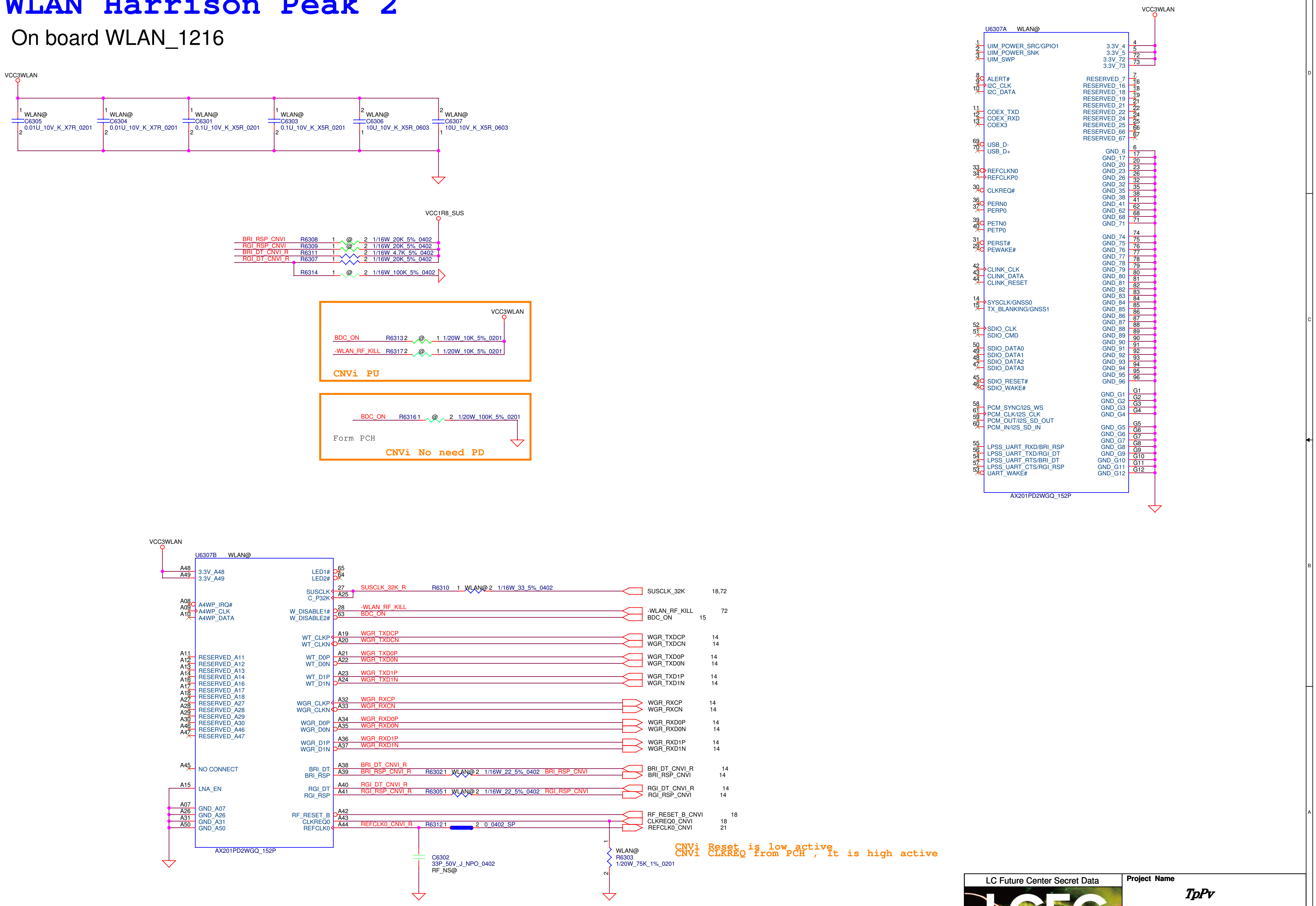
Rev 1.0

Title: M.2 SATA/PCIE SSD SLOT_2

Date: Friday, May 15, 2020 Sheet 62 of 133

# WLAN Harrison Peak 2

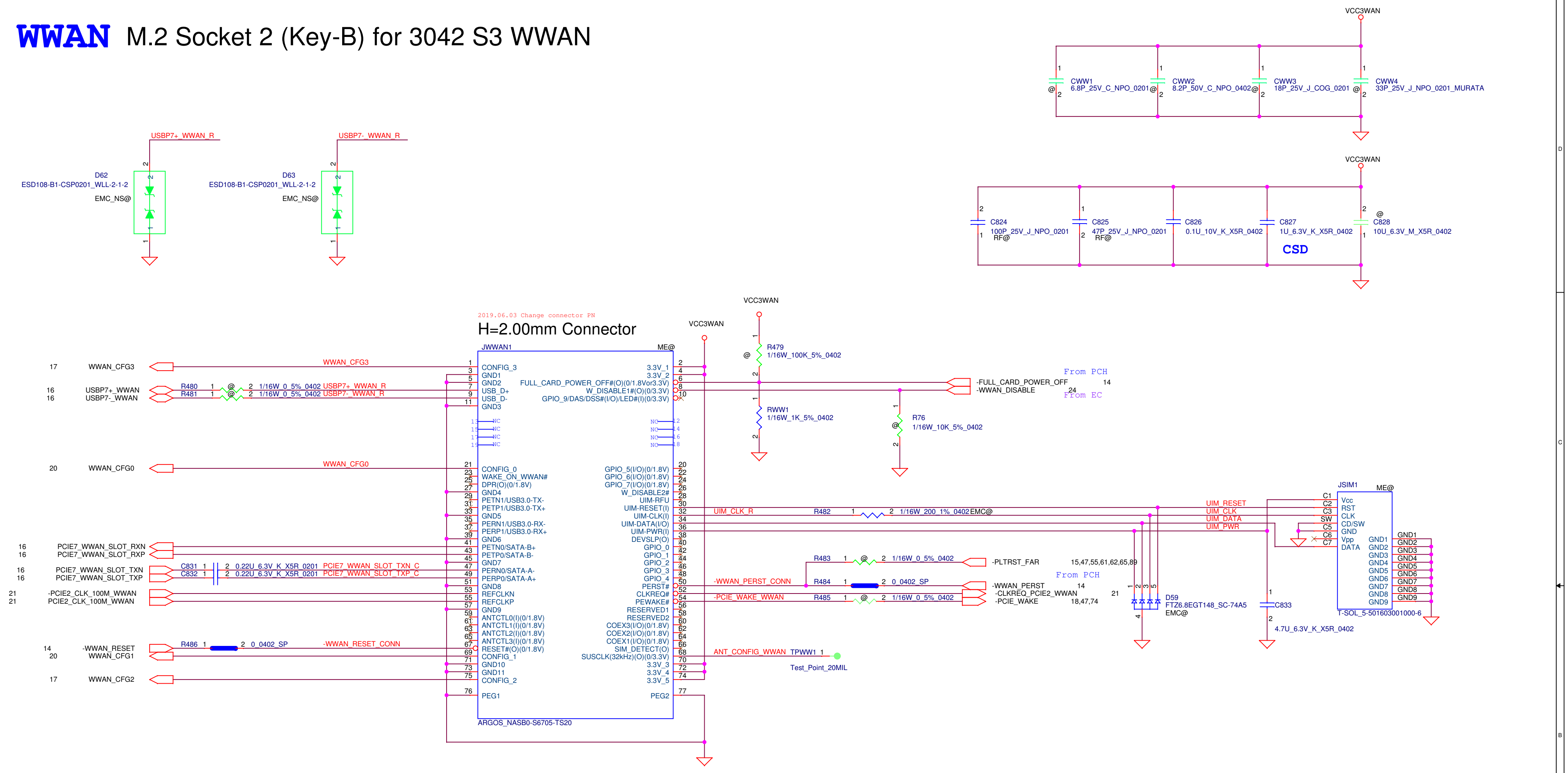
On board WLAN_1216



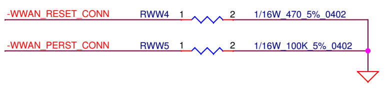

LC Future Center Secret Data

| | | |
|---|---|---|
| Project Name | TpPv | |
| Rev 1.0 | Title | WLAN Harrison Peak 2 |
| Date: Friday, May 29, 2020 | Sheet 63 of 133 | |

# WWAN M.2 Socket 2 (Key-B) for 3042 S3 WWAN



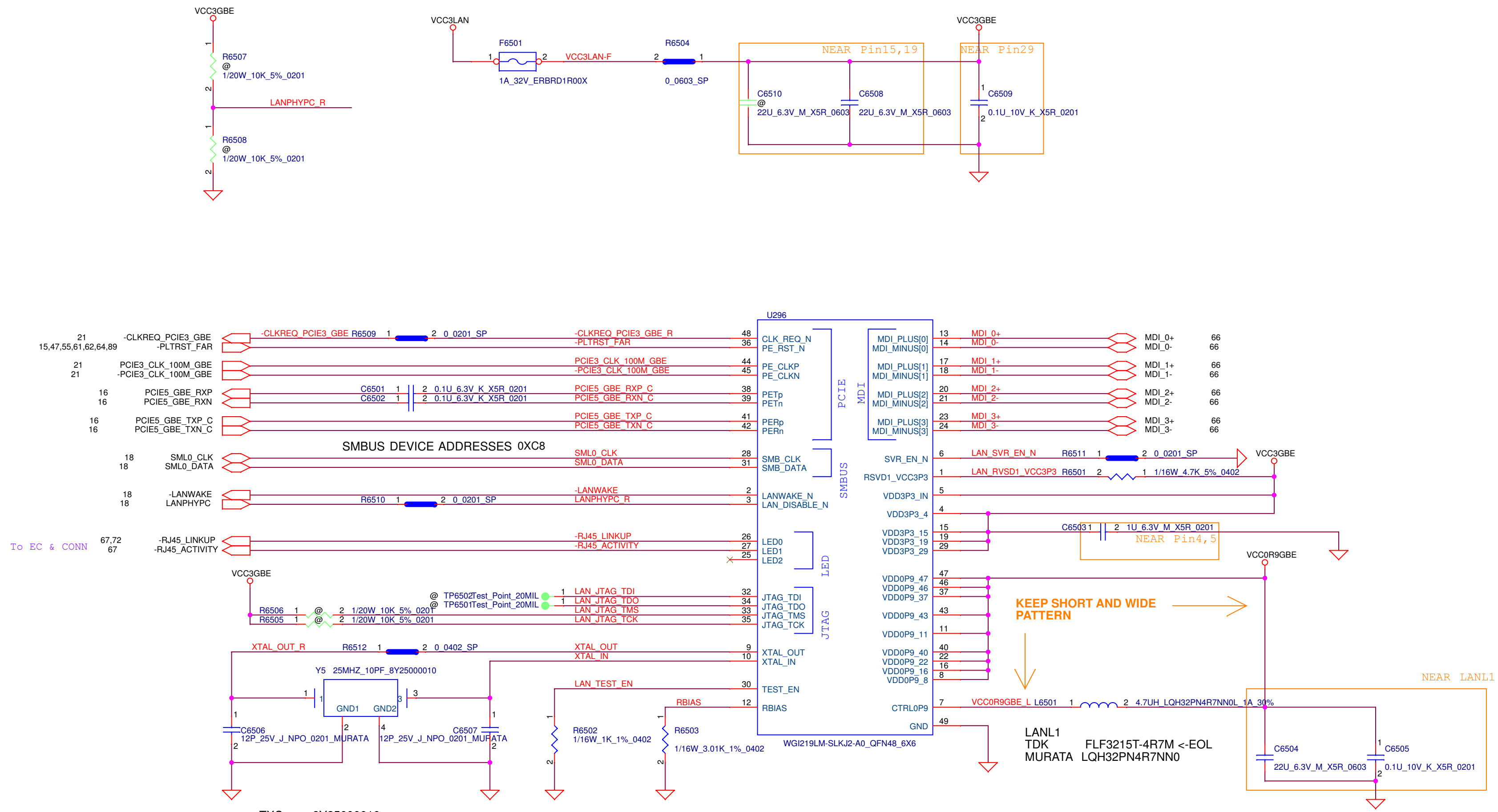

| Pin | Pin Name | I/O | Reset Value | Description | Type |
|---|---|---|---|---|---|
| 36 | UIM_PWR | PO | - | USIM power supply | 1.8V/3V |
| 30 | UIM_RESET | O | L | USIM reset | 1.8V/3V |
| 32 | UIM_CLK | O | L | USIM clock | 1.8V/3V |
| 34 | UIM_DATA | I/O | L | USIM data, internal pull up(4.7KΩ) | 1.8V/3V |
| 66 | SIM_DETECT | I | PD | USIM card detect, internal 390K pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached. | 1.8V |




TABLE

| | CONFIG 0 | CONFIG 3 | CONFIG 2 | CONFIG 1 |
|---|---|---|---|---|
| Fibocom L850-GL | GND | N.C. | GND | GND |

# LAN




TXC 8Y25000010
KDS 1ZZHAE25000CC0B

LANU1 GBE PHY

| vPRO Model | Non-vPRO Model |
|---|---|
| I219LM | I219V |

LC Future Center Secret Data

LCFC

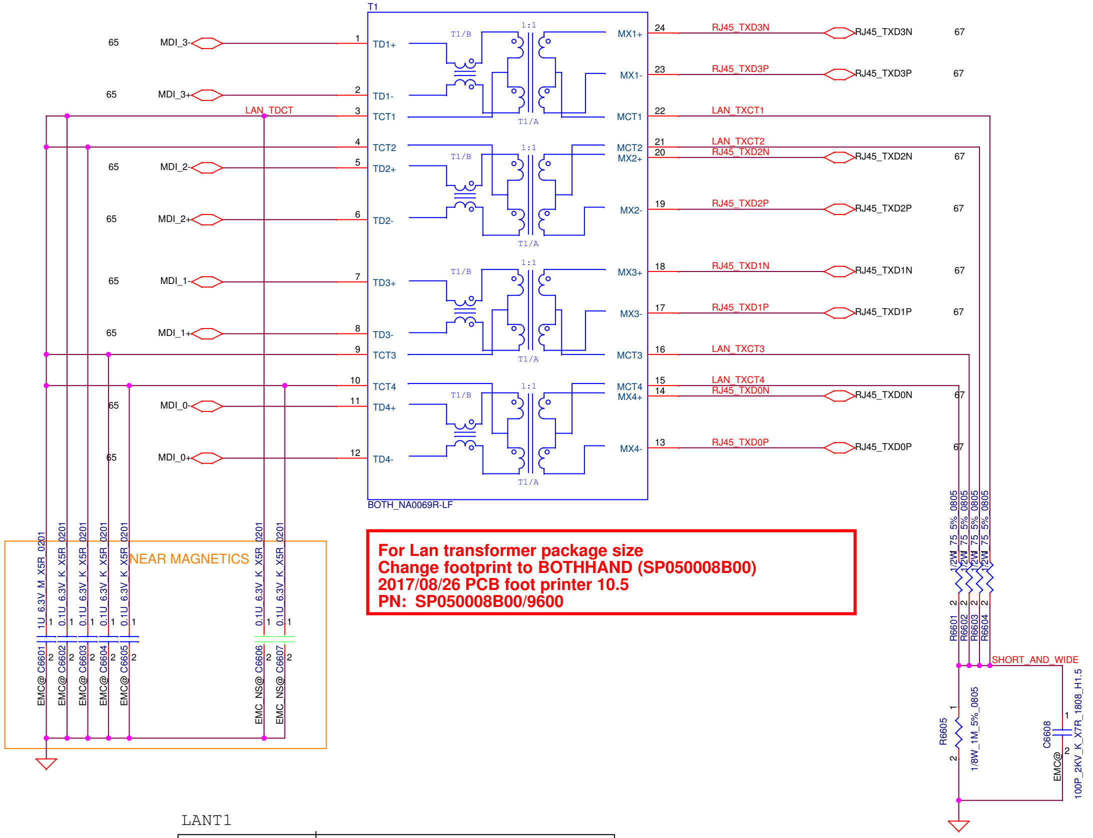
Project Name: TpPv

Rev 1.0

Title: GBE JACKSONVILLE

Date: Friday, May 15, 2020

# LAN



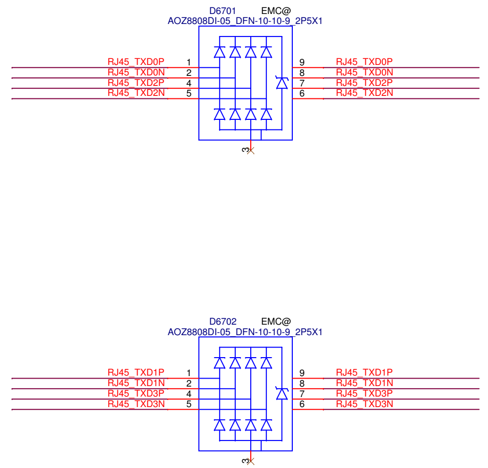

PATTERN MUST BE SHORT AND WIDE.

HIGH VOLTAGE 1500PF CAP IS OPTIONAL

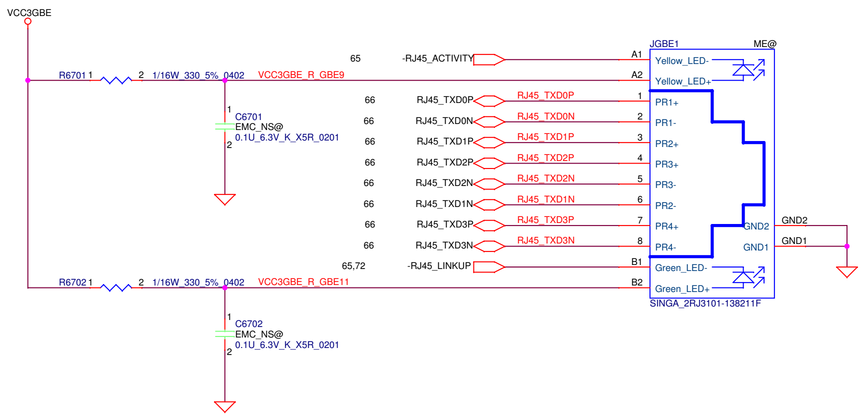
LANT1

| Vendor | P/N |
|---|---|
| Bothhand | SP050008B00 NA69LF |
| TAIMAG | SP050009J00 IH-189-F LAN |

# LAN




| | |
|---|---|
| D6701<br>D6702 | 1st:AOS AOZ8808DI-05 DFN-10 (SC300003H00)<br>2nd:AMAZING AZ1045-04F.R7G DFN2510P10E (SC300001Y0J)<br>3th:Nexperia IP4292CZ10-TBR DFN2510A-10 (SC300003A00) |




| NODE | | COLOR | |
|---|---|---|---|
| A2(+) | A1(−) | YELLOW | A2→A1 |
| B2(+) | B1(−) | GREEN | B2→B1 |

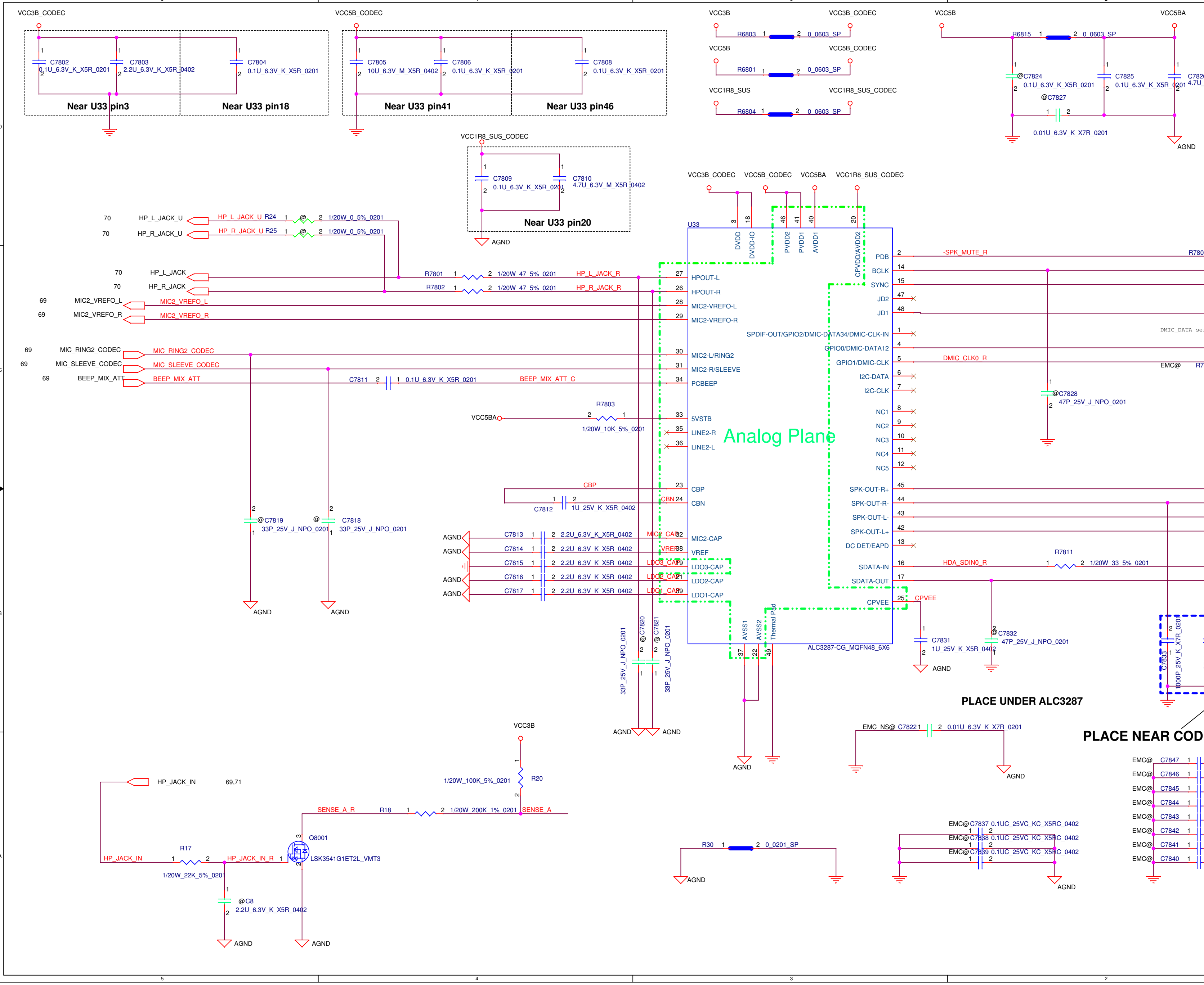
LC Future Center Secret Data

Project Name: TpPv

Rev: 1.0

Title: GBE_RJ45 CONNECTOR

Date: Friday, May 15, 2020




LC Future Center Secret Data

Project Name: TpPv

Rev: 1.0

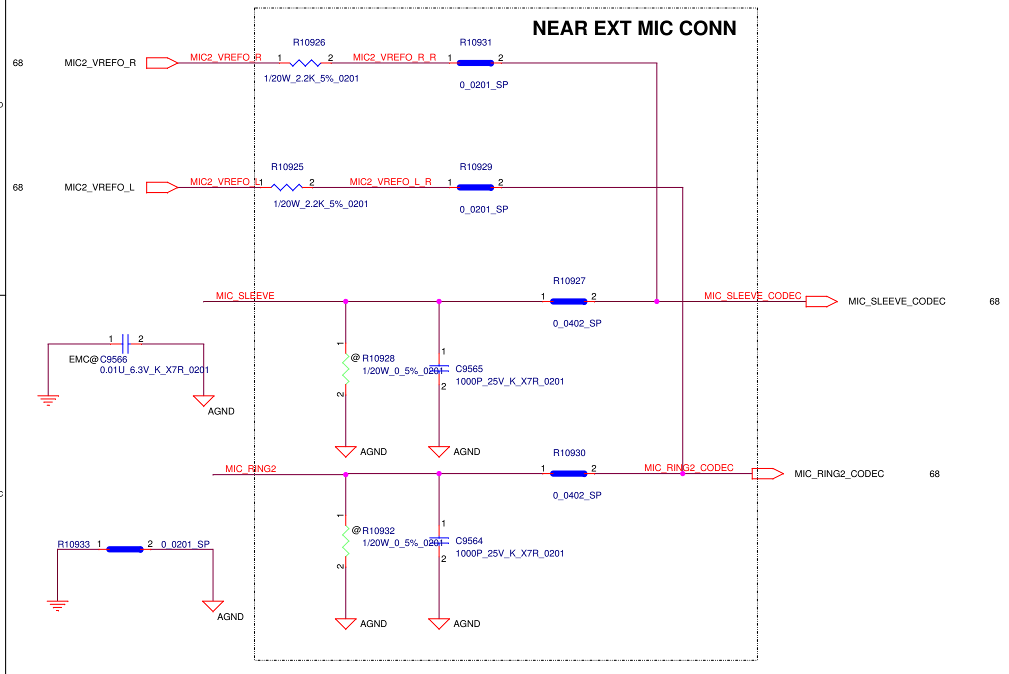
Title: AUDIO ALC3287-CG

Date: Friday, May 15, 2020

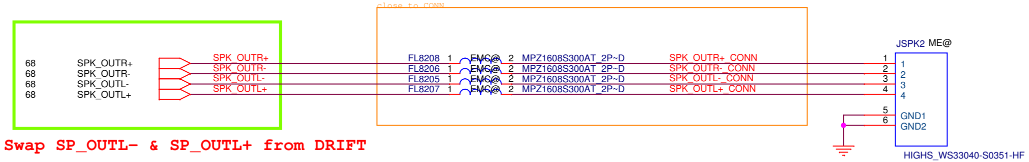
Sheet 68 of 133

C

# HEAD PHONE/LINE OUT

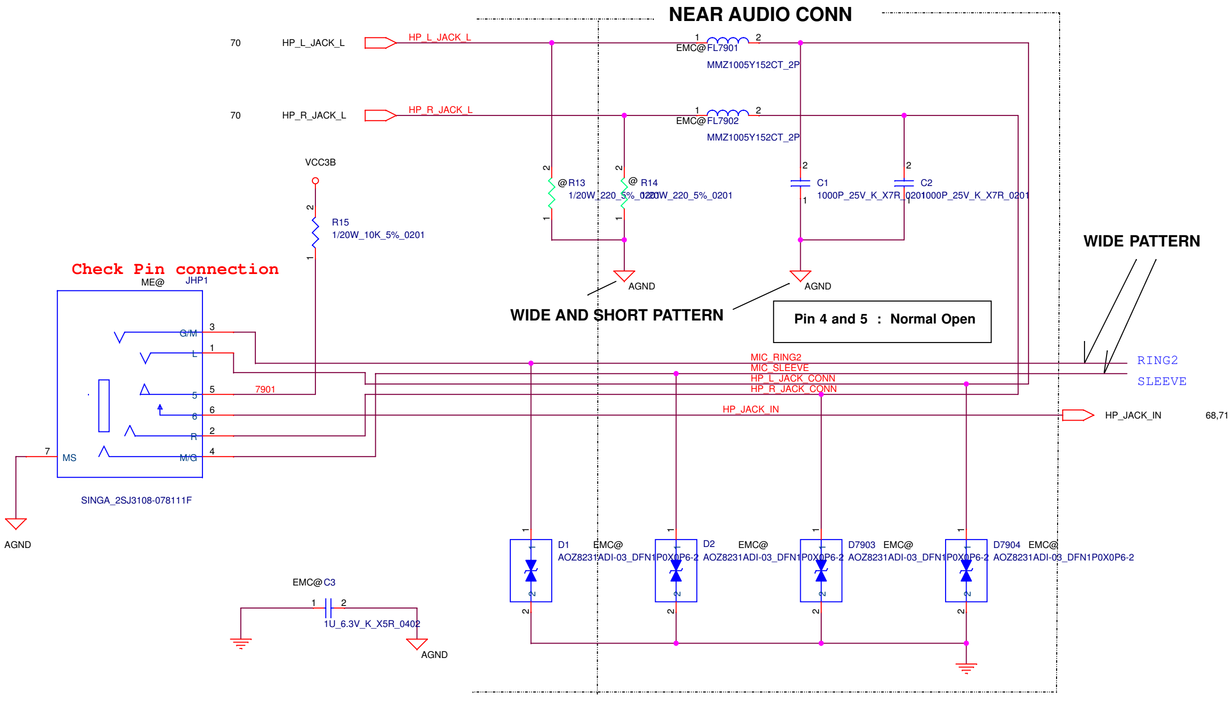



# SPEAKER




| FL8205~FL8208 | Description | LCFC PN |
|---|---|---|
| Main | MPZ1608S300AT | SM01003110J |
| 2nd | BLM18KG300TN1D | SM01000L000 |
| 3rd | UPB160808T-300Y-N | SM01000MH00 |

# AUDIO JACK/EXT. MIC/LINE IN




# PC BEEP

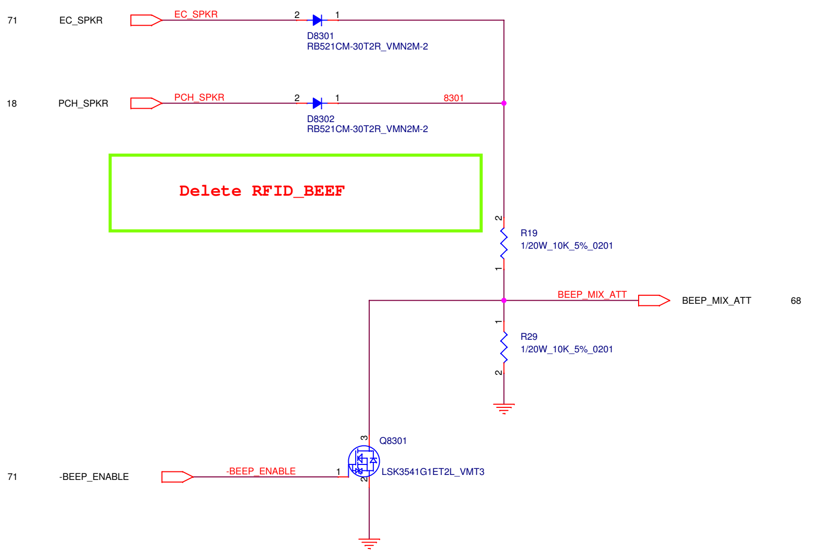
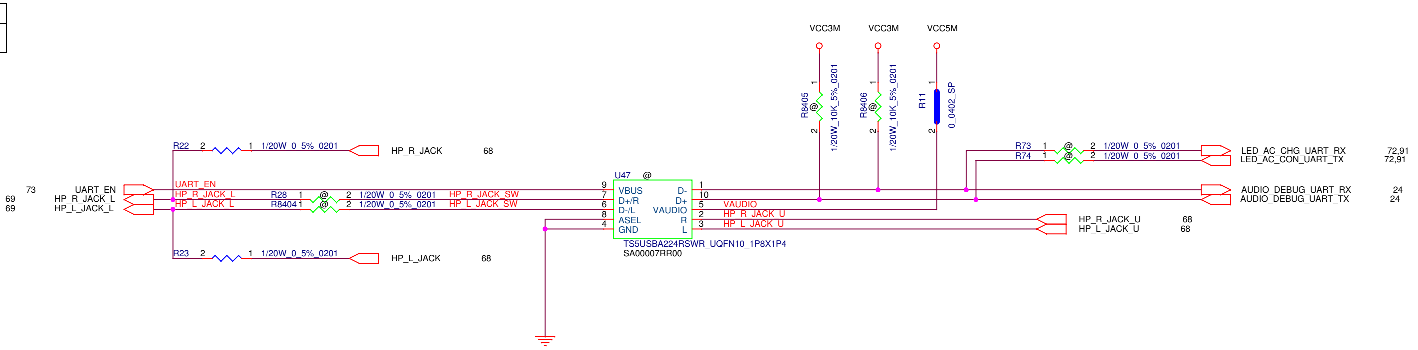


**TABLE:**

| Mode | Audio | UART |
|---|---|---|
| UART_EN | L | H |




LC Future Center Secret Data

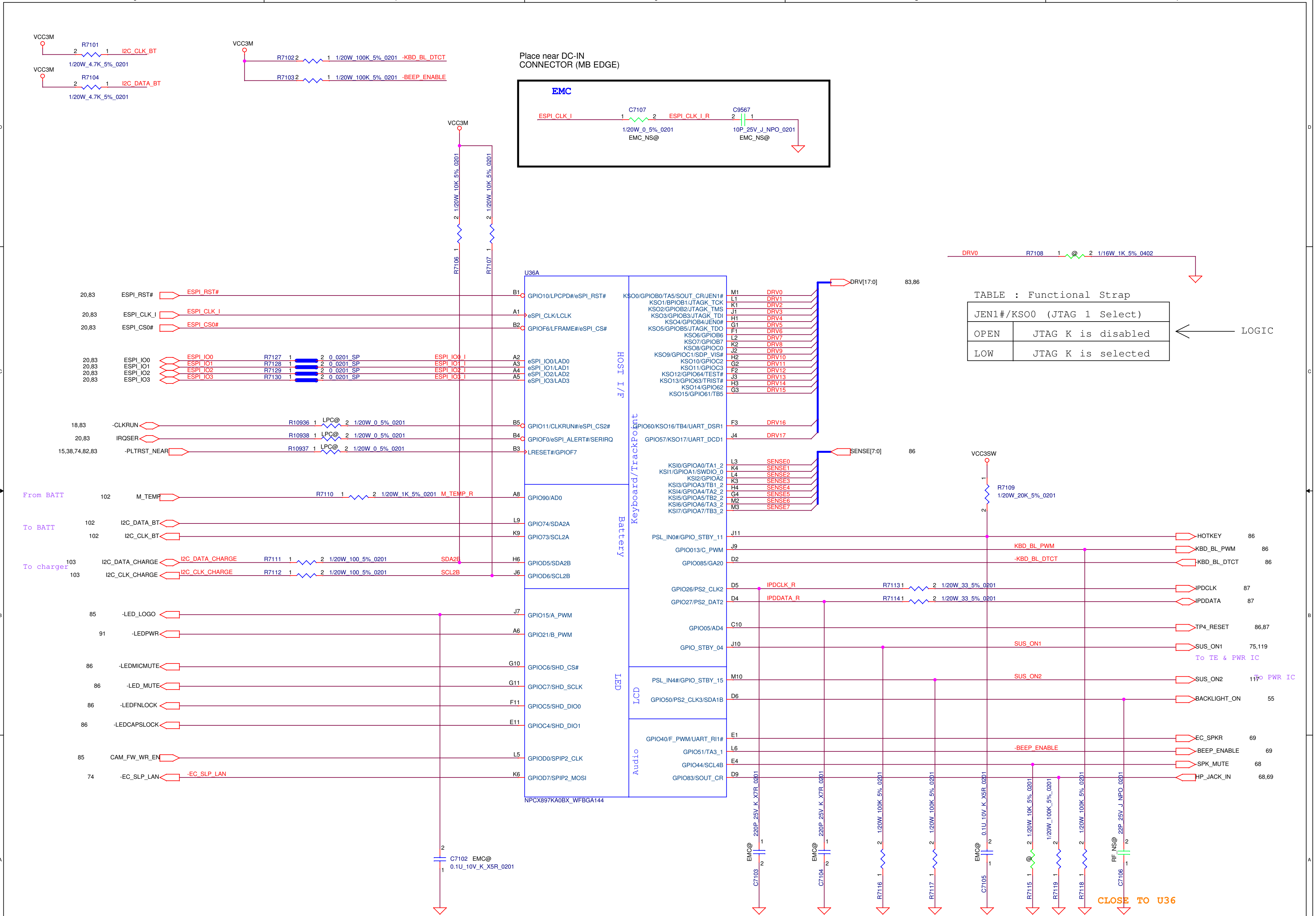
LCFC

Project Name: TpPv

Rev: 1.0

Title: AUDIO DEBUG

Date: Friday, May 15, 2020




| TABLE : Functional Strap | |
|---|---|
| JEN1#/KSO0 (JTAG 1 Select) | |
| OPEN | JTAG K is disabled |
| LOW | JTAG K is selected |

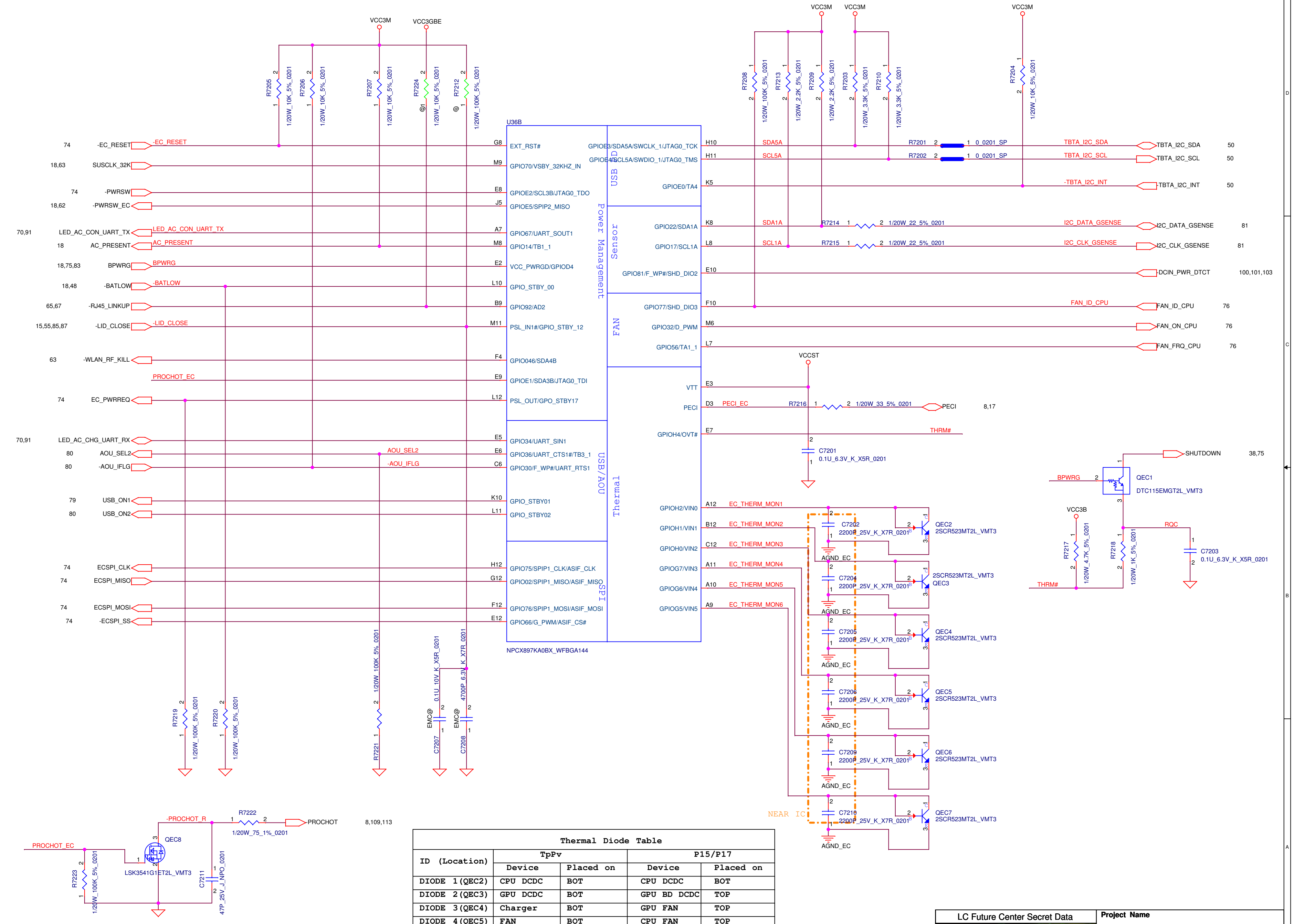
← LOGIC

LC Future Center Secret Data

Project Name: TpPv

Rev 1.0 | Title: NPCX897KA0BX(1/3)

Date: Friday, May 15, 2020 | Sheet 71 of 133



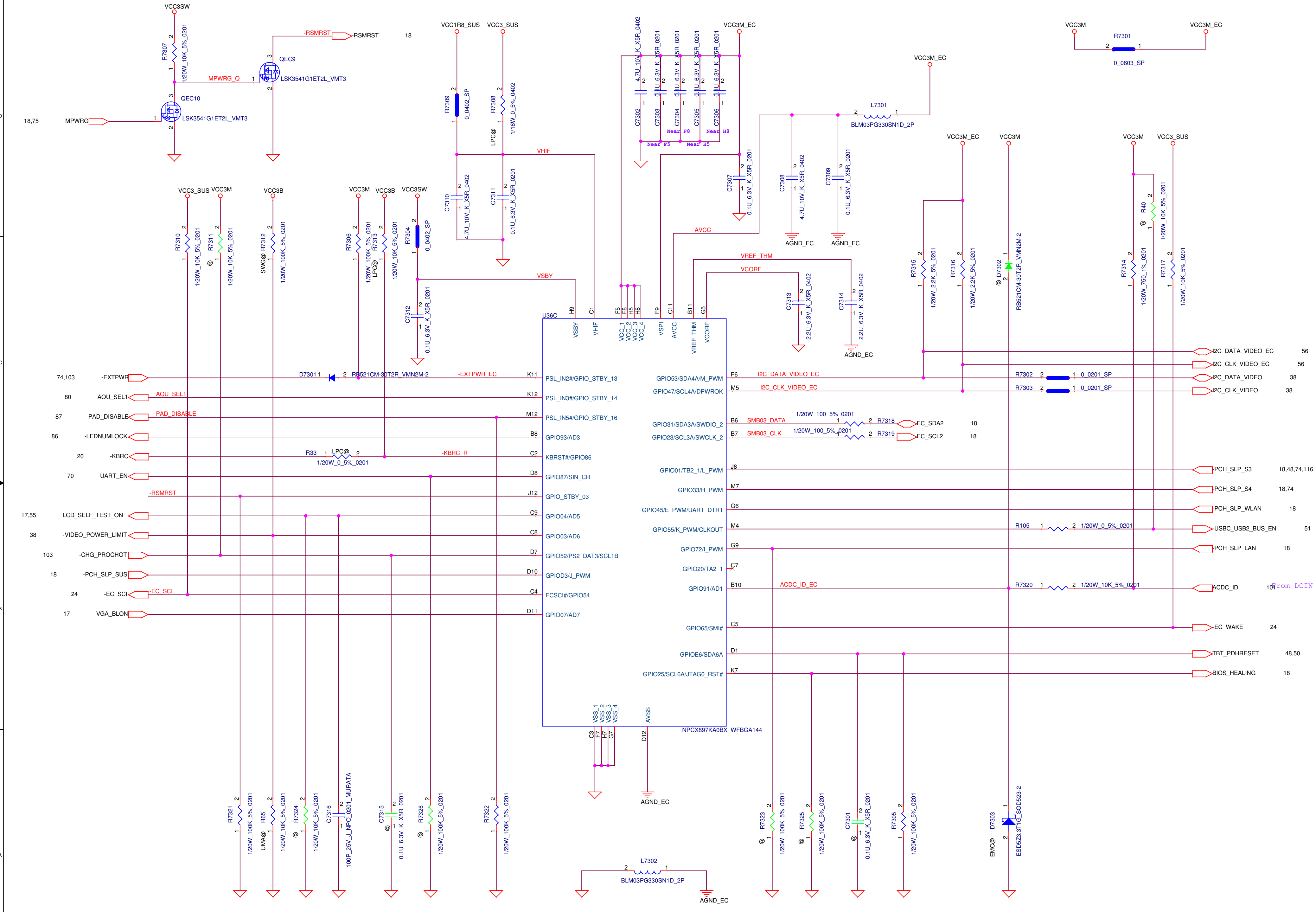

**Thermal Diode Table**

| ID (Location) | TpPv Device | TpPv Placed on | P15/P17 Device | P15/P17 Placed on |
|---|---|---|---|---|
| DIODE 1(QEC2) | CPU DCDC | BOT | CPU DCDC | BOT |
| DIODE 2(QEC3) | GPU DCDC | BOT | GPU BD DCDC | TOP |
| DIODE 3(QEC4) | Charger | BOT | GPU FAN | TOP |
| DIODE 4(QEC5) | FAN | BOT | CPU FAN | TOP |
| DIODE 5(QEC6) | DIMM | BOT | DIMM | TOP |
| DIODE 6(QEC7) | SSD | BOT | SSD | BOT |



Project Name: TpPv

Rev 1.0 Title: NPCX897KA0BX(2/3)




LC Future Center Secret Data

LCFC

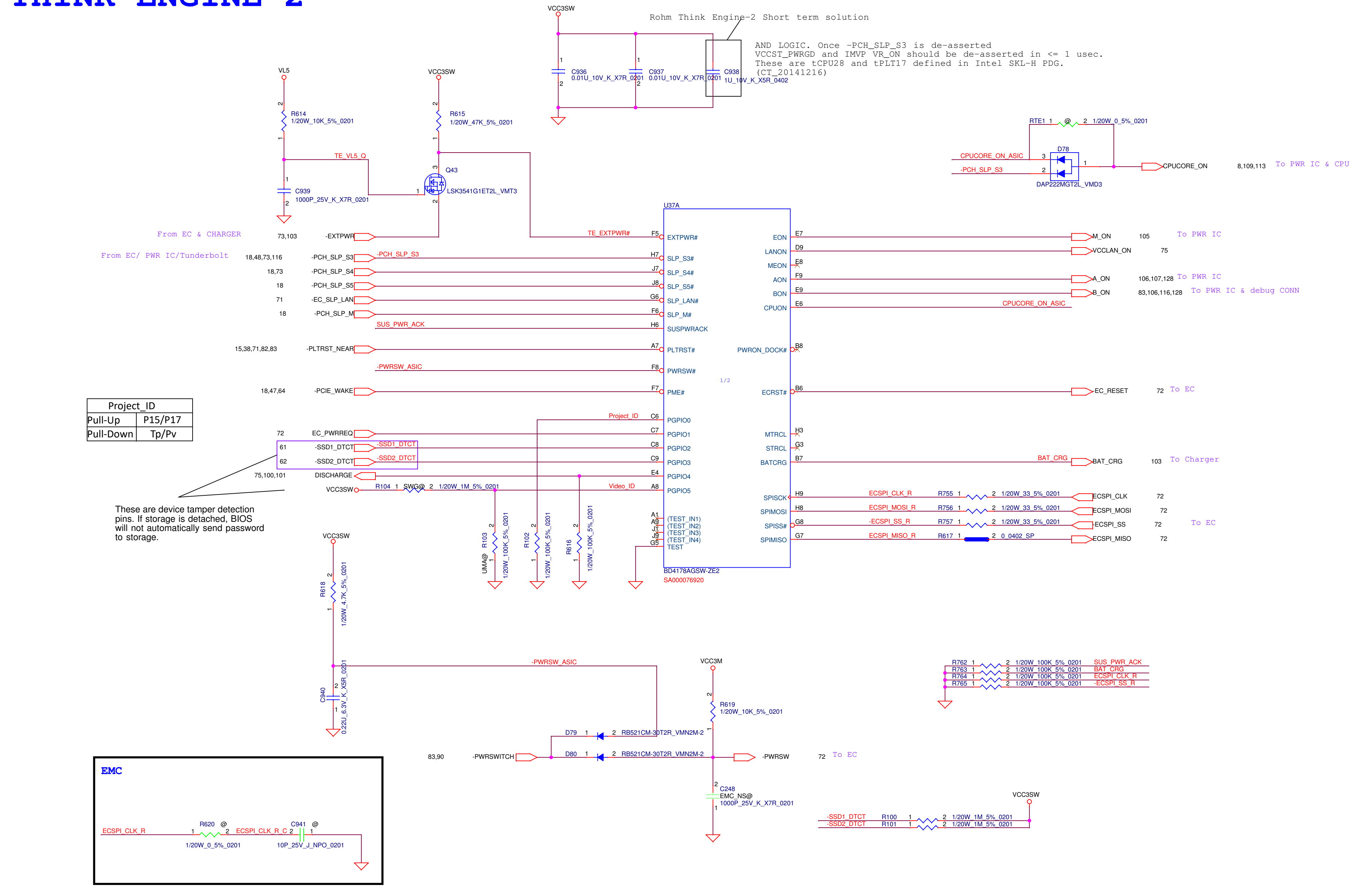
Project Name: TpPv

Rev 1.0

Title: NPCX897KA0BX(3/3)

Date: Monday, May 18, 2020

# THINK ENGINE 2



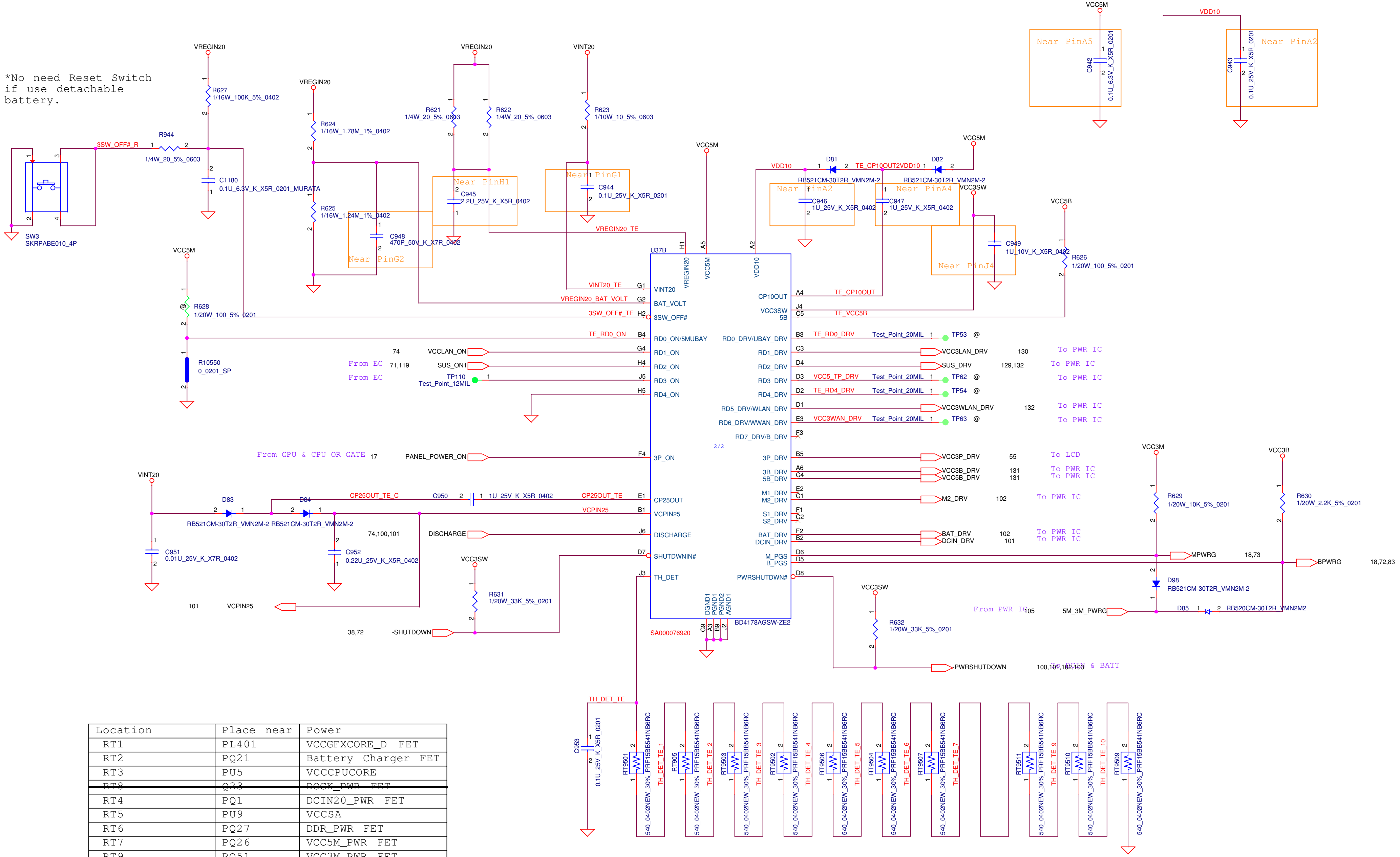

| Project_ID | |
|---|---|
| Pull-Up | P15/P17 |
| Pull-Down | Tp/Pv |

These are device tamper detection pins. If storage is detached, BIOS will not automatically send password to storage.

| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| LCFC | Rev 1.0 — Title: THINK ENGINE 2(1/2) |
| | Date: Friday, May 15, 2020 — Sheet 74 of 133 |

# THINK ENGINE 2

*No need Reset Switch
if use detachable
battery.

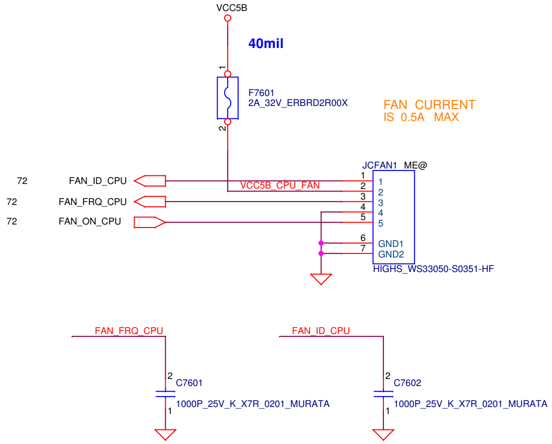



| Location | Place near | Power |
|---|---|---|
| RT1 | PL401 | VCCGFXCORE_D FET |
| RT2 | PQ21 | Battery Charger FET |
| RT3 | PU5 | VCCCPUCORE |
| ~~RT8~~ | ~~Q23~~ | ~~DOCK_PWR FET~~ |
| RT4 | PQ1 | DCIN20_PWR FET |
| RT5 | PU9 | VCCSA |
| RT6 | PQ27 | DDR_PWR FET |
| RT7 | PQ26 | VCC5M_PWR FET |
| RT9 | PQ51 | VCC3M_PWR FET |
| RT10 | PQ10 | M_BAT_PWR FET |
| RT11 | PU7 | VCCGFXCORE_I |
| RT12 | PQ9 | Charge FET |
| ~~PRT1(BAT_FET_HOT)~~ | ~~PQ11~~ | ~~BAT_IN~~ |

LC Future Center Secret Data
LCFC

Project Name: TpPv
Rev: 1.0
Title: THINK ENGINE 2(2/2)
Date: Friday, May 15, 2020 | Sheet 75 of 133

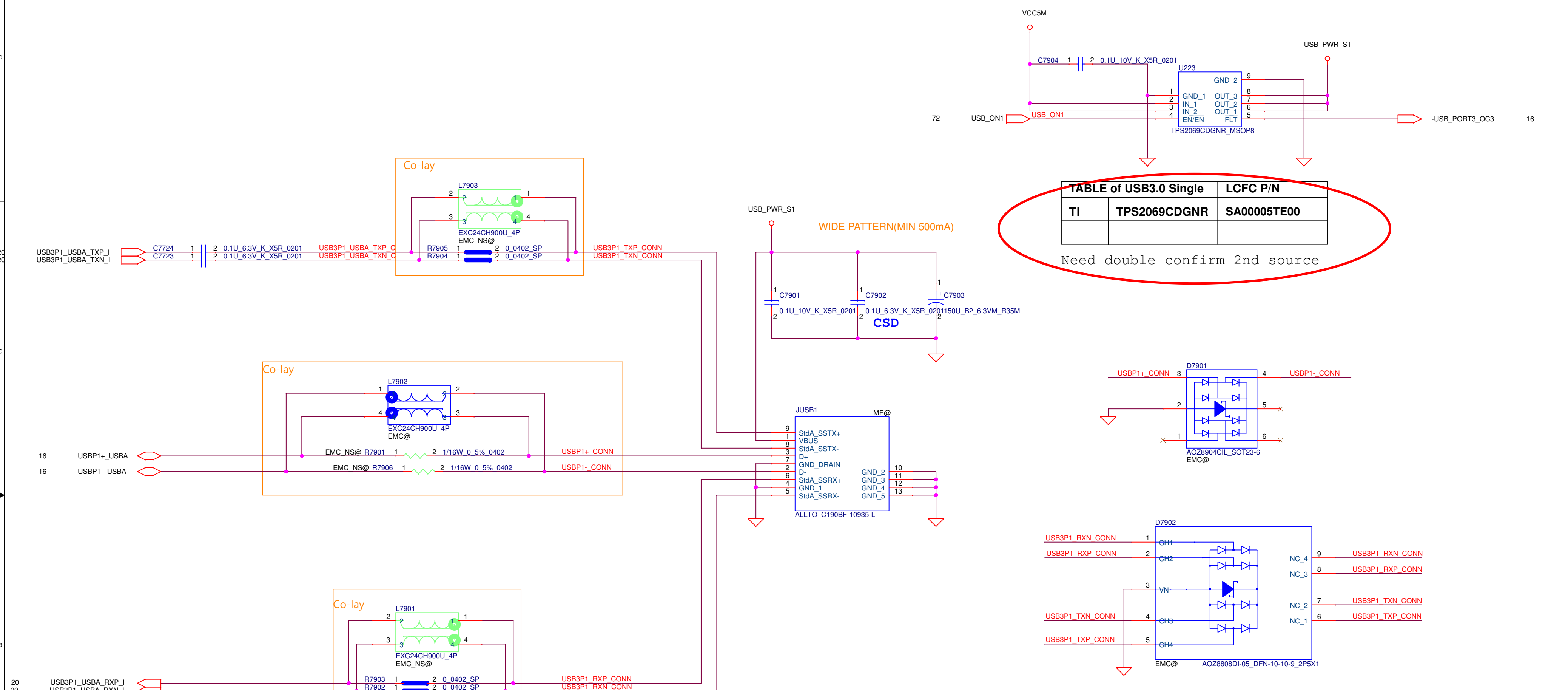
# CPU and GPU FAN




| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| | Rev 1.0 / Title: FAN CONNECTOR |
| | Date: Friday, May 15, 2020 / Sheet 76 of 133 |

| | | |
|---|---|---|
| LC Future Center Secret Data | Project Name | TpPv |
| LCFC | Rev 1.0 | Title BLANK |
| | Date: Friday, May 15, 2020 | Sheet 78 of 133 |

# USB3.1 CONN




| TABLE of USB3.0 Single | | LCFC P/N |
|---|---|---|
| TI | TPS2069CDGNR | SA00005TE00 |
| | | |

Need double confirm 2nd source

| | |
|---|---|
| D87 | 1st:Semtech AOZ8808DI-05 DFN-10 (SC300003H00)<br>2nd:LittelFuse<br>3th:LittelFuse |

LC Future Center Secret Data

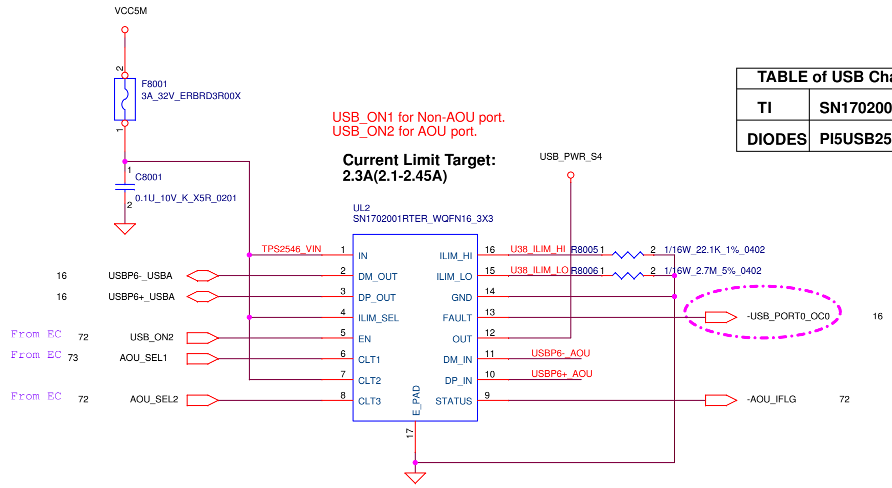
LCFC

Project Name: TpPv

Rev 1.0

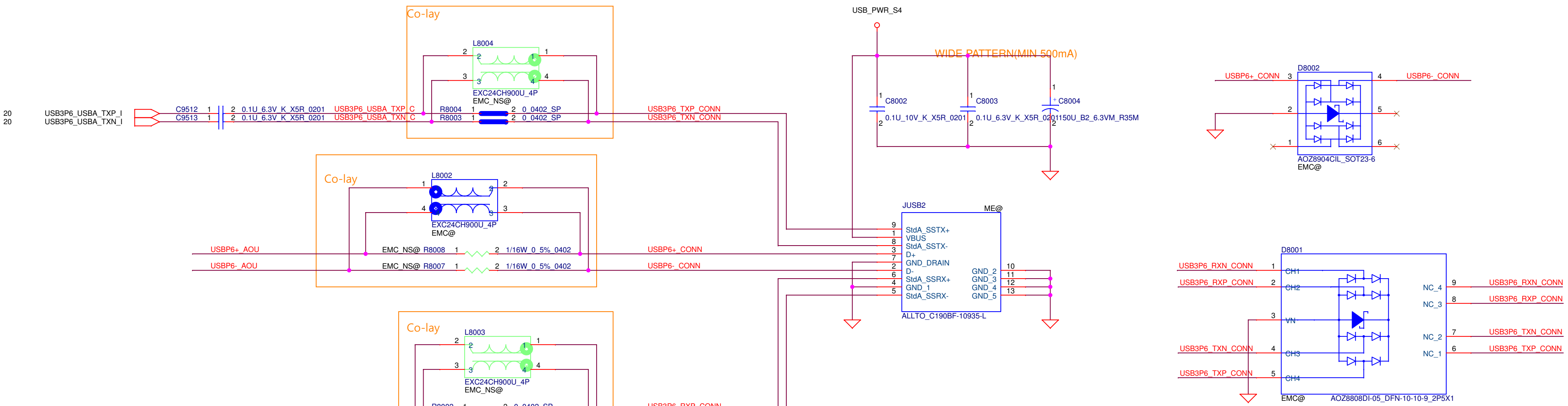
Title: USB POWER/CONNECTOR_1

# USB Charger IC




| TABLE of USB Charge | | LCFC P/N |
|---|---|---|
| TI | SN1702001RTER | SA00008HF00 |
| DIODES | PI5USB2546HZHDEX | SA00009D800 |

# USB3.0 CONN




| | |
|---|---|
| DL1 | 1st:Semtech AOZ8808DI-05 DFN-10 (SC300003H00)<br>2nd:LittelFuse<br>3th:LittelFuse |

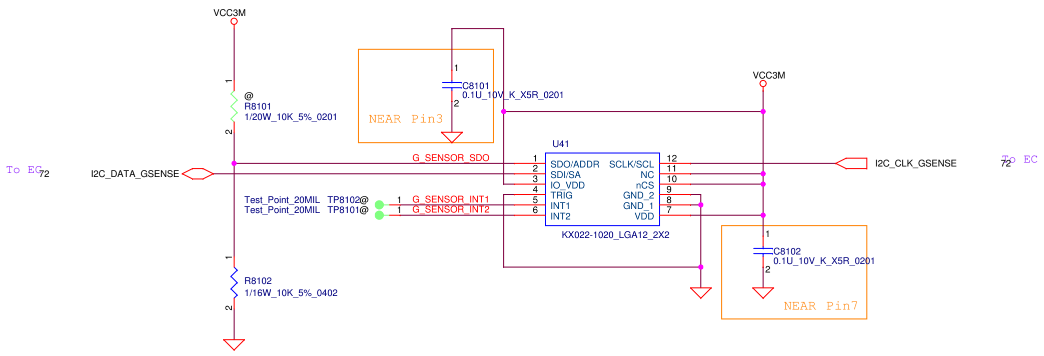
# G-SENSOR

**TABLE**

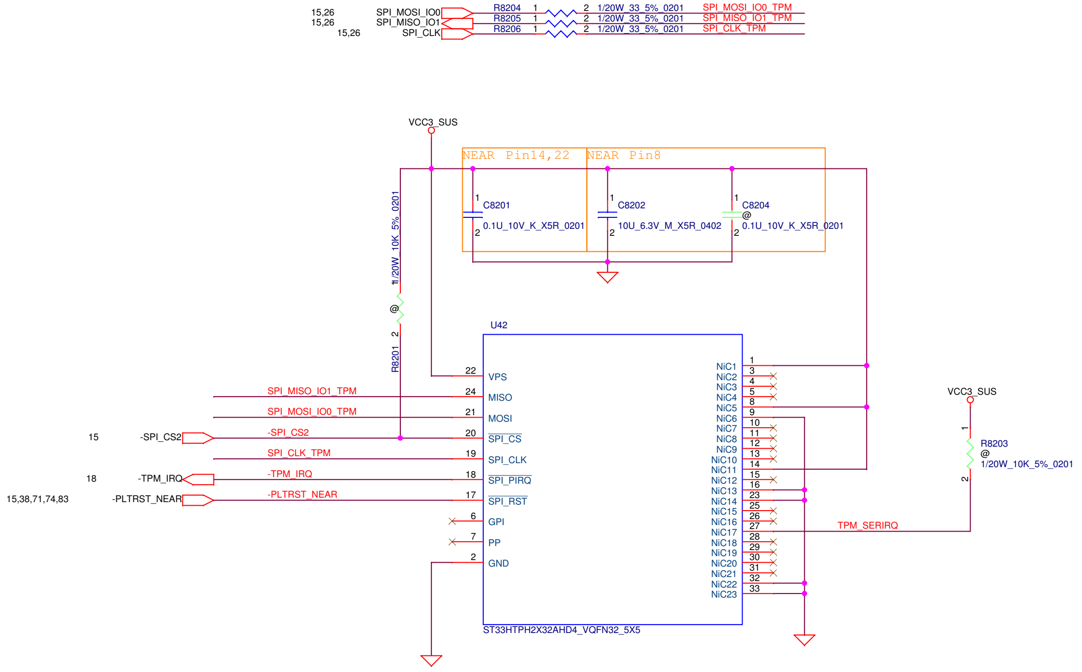
| P/N | ADDR_SEL | Address |
|---|---|---|
| KX022-1020 | H<br>L | 3Eh (W) & 3Fh (R)<br>3Ch (W) & 3Dh (R) |
| LIS2DWLTR | H<br>L | 32h (W) & 33h (R)<br>30h (W) & 31h (R) |
| BMA280 | H<br>L | 30h (W) & 31h (R)<br>32h (W) & 33h (R) |

**TABLE of G-Sersor (GSU1)**

| Vendor | P/N | LCFC P/N |
|---|---|---|
| Kionix | KX022-1020 | SA000081E00 |
| ST | LIS2DWLTR LGA | SA00009AQ00 |
| BOSCH | BMA280 | SA0000A1600 |



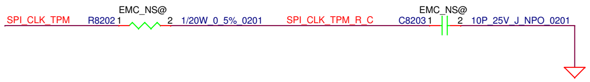
# TPM




TABLE

Main Source

| Pin No | TCG PTP Spec (v38) | Infineon SLB9670VQ2.0FW7.63 SA000075L50 | ST Micro ST33HTPH2X32AHD4 SA000089E10 |
|---|---|---|---|
| 1 | VDD | VDD | NC |
| 2 | GND | GND | GND |
| 3 | GPIO | NC | NC |
| 4 | GPIO | NC | PP |
| 5 | NC | NC | NC |
| 6 | VNC/GPIO | GPIO | NC |
| 7 | GPIO/VDD | PP | GPIO |
| 8 | VDD | VDD | NC |
| 9 | GND | GND | NC |
| 10 | VNC | NC | NC |
| 11 | NC | NC | NC |
| 12 | NC | NC | NC |
| 13 | VNC/GPIO | NC | NC |
| 14 | VDD | NC | NC |
| 15 | NC | NC | NC |
| 16 | GND | NC | NC |
| 17 | SPI_RST# | RST# | SPI_RST# |
| 18 | SPI_PIRQ# | PIRQ# | SPI_PIRQ# |
| 19 | SPI_CLK | SCLK | SPI_CLK |
| 20 | SPI_CS# | CS# | SPI_CS# |
| 21 | MOSI | MOSI | MOSI |
| 22 | VDD | VDD | VPS |
| 23 | GND | GND | NC |
| 24 | MISO | MISO | MISO |
| 25 | NC | NC | NC |
| 26 | NC | NC | NC |
| 27 | NC | NC | NC |
| 28 | NC | NC | NC |
| 29 | VNC/GPIO | NC | NC |
| 30 | VNC/GPIO | NC | NC |
| 31 | VNC | NC | NC |
| 32 | GND | GND | NC |




LC Future Center Secret Data

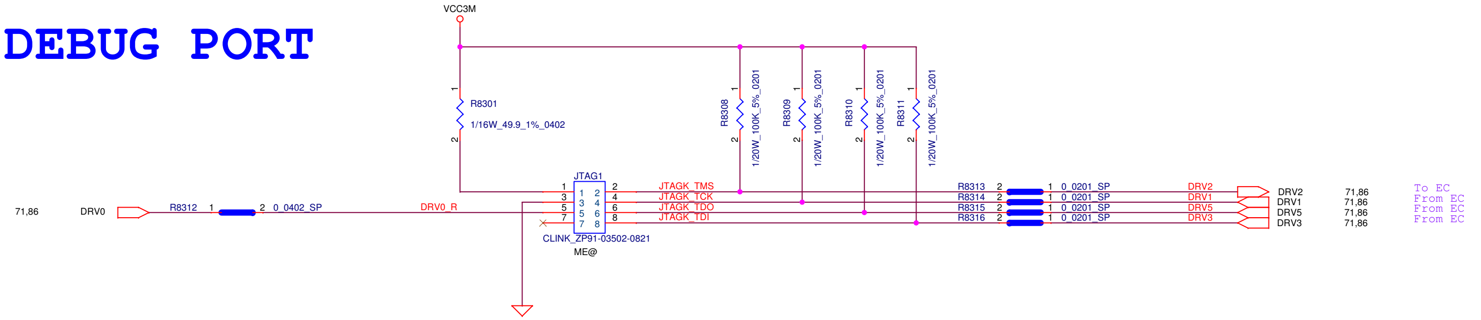
Project Name: TpPv

Rev 1.0

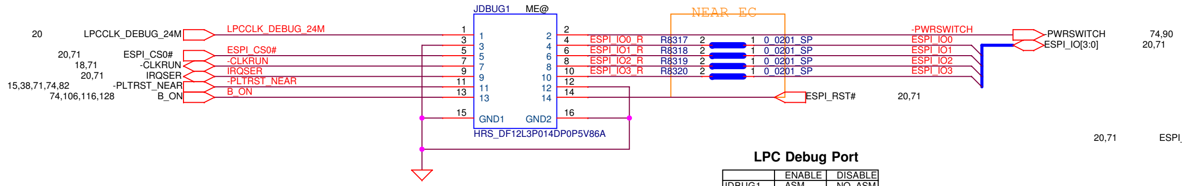
Title: DISCRETE TPM 2.0

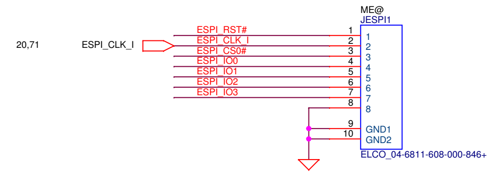
Date: Friday, May 15, 2020

# JTAG DEBUG PORT




# LPC DEBUG PORT



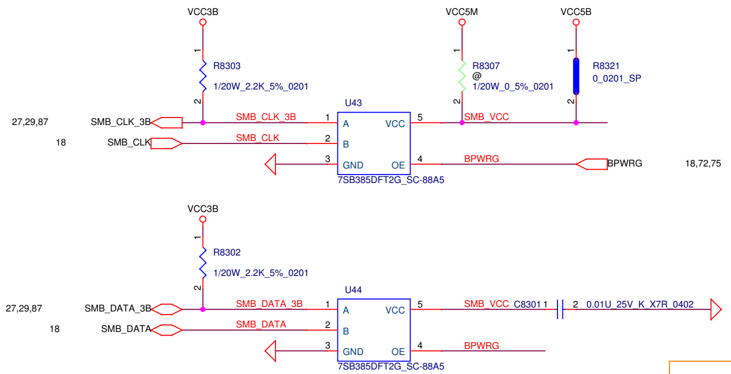




**LPC Debug Port**

| | ENABLE | DISABLE |
|---|---|---|
| JDBUG1 | ASM | NO_ASM |
| DBUGR8 | ASM | NO_ASM |
| DBUGR9 | ASM | NO_ASM |
| DBUGR10 | ASM | NO_ASM |
| DBUGR11 | ASM | NO_ASM |

LOGIC

# SMBUS SWITCH



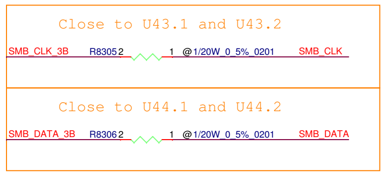
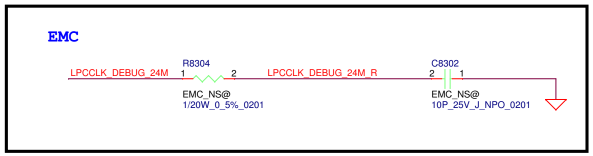
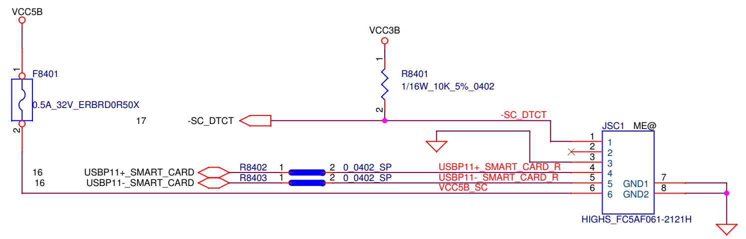




**TABLE of U43/U44**

| Vendor | Description | LCFC P/N |
|---|---|---|
| ON | 7SB385DFT2G | SA00007CW00 |
| PERICOM | PI5A121BCEX | SA000050100 |



# SMART CARD




LC Future Center Secret Data

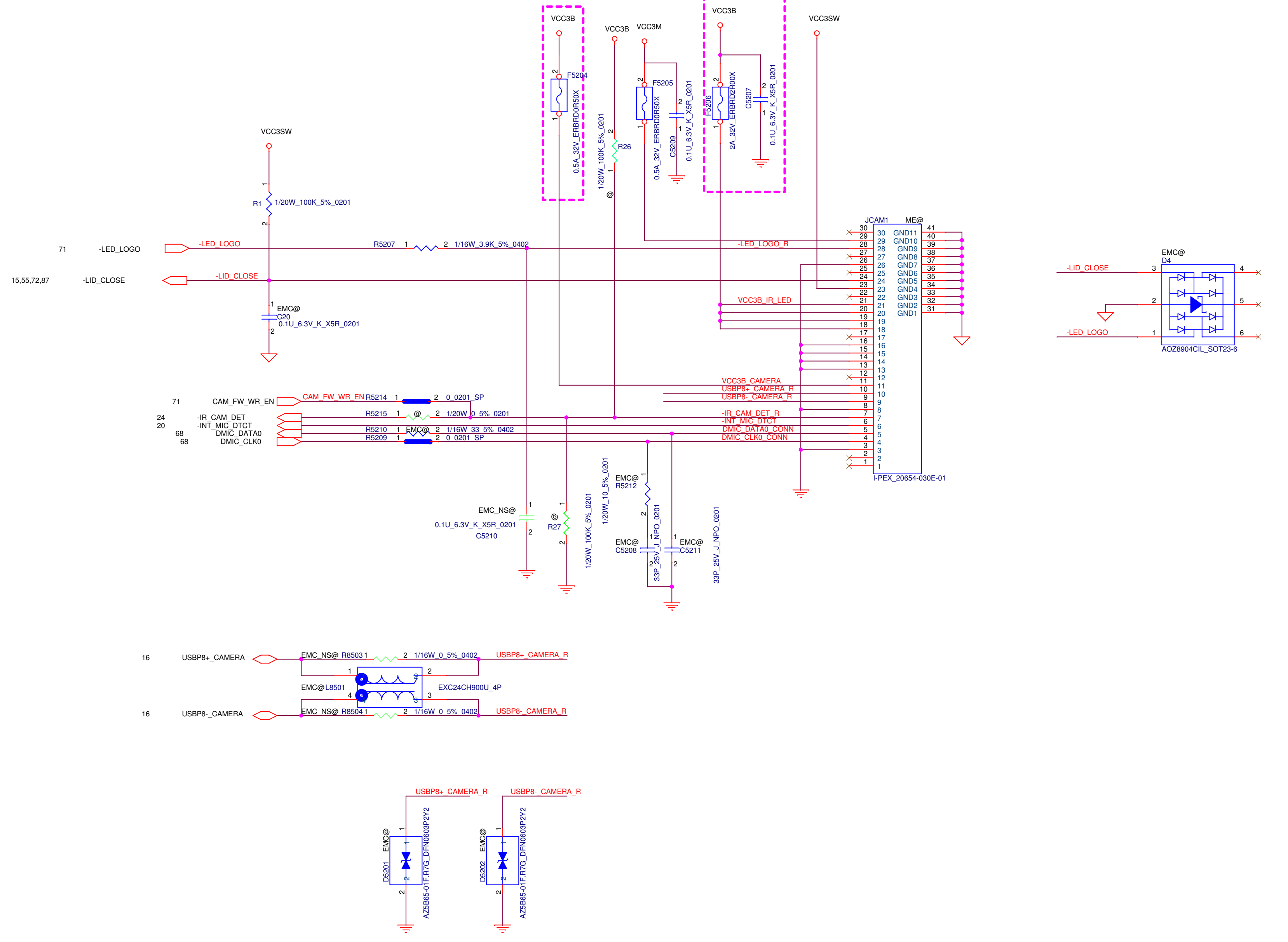
Project Name: TpPv

Rev 1.0

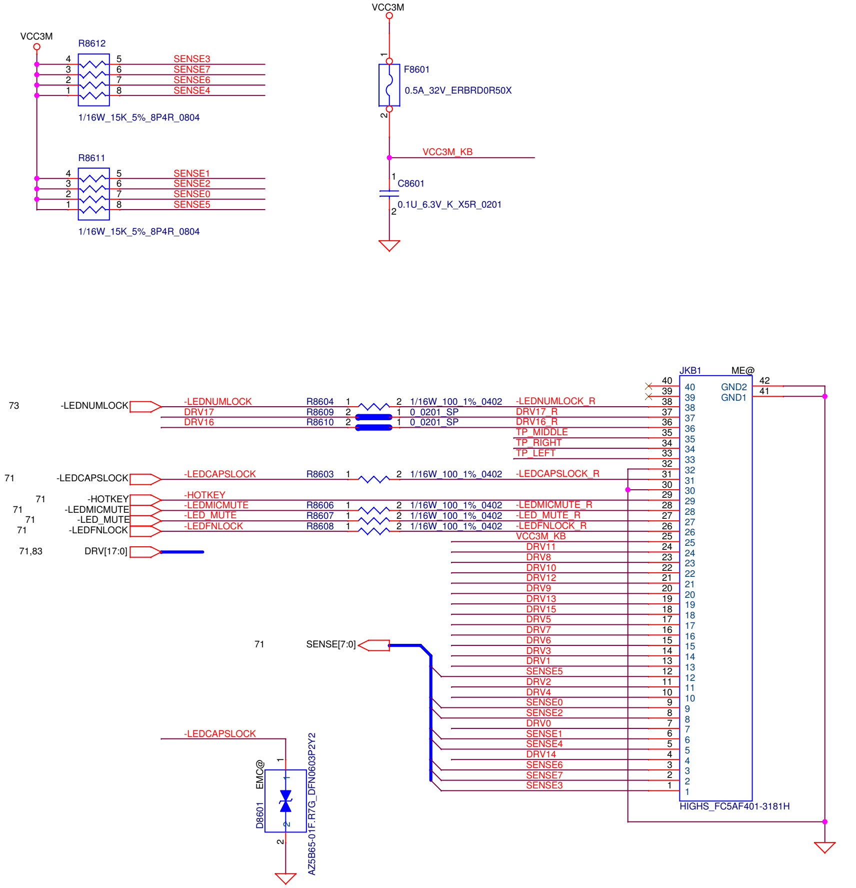
Title: SMART CARD Conn

Date: Friday, May 15, 2020

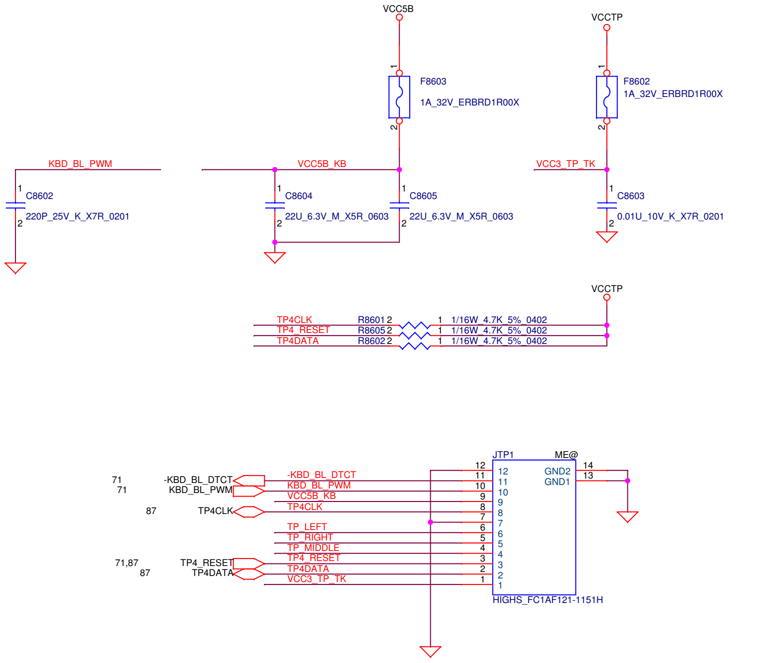
# CAMERA/LID/TOUCH



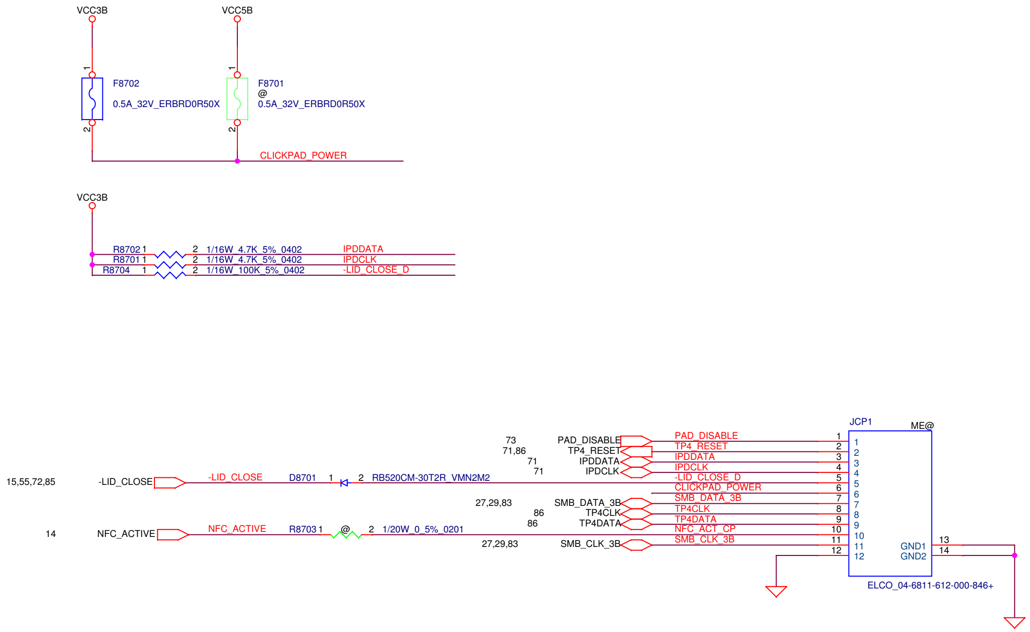
# KEYBOARD




# TRACK POINT



# CLICK PAD




LC Future Center Secret Data

Project Name: TpPv

Rev 1.0

Title: CLICK PAD

Date: Friday, May 15, 2020

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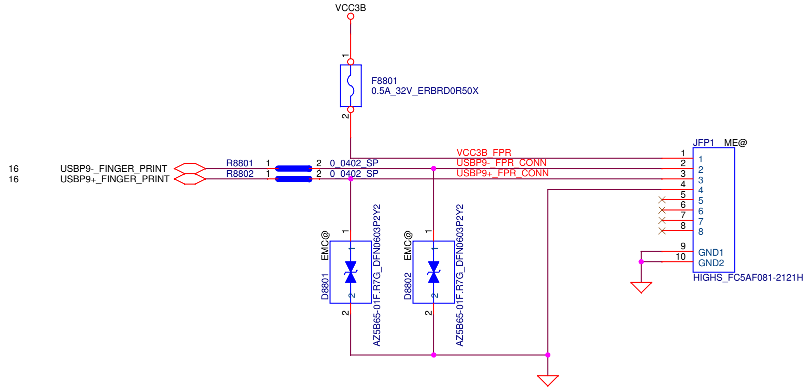
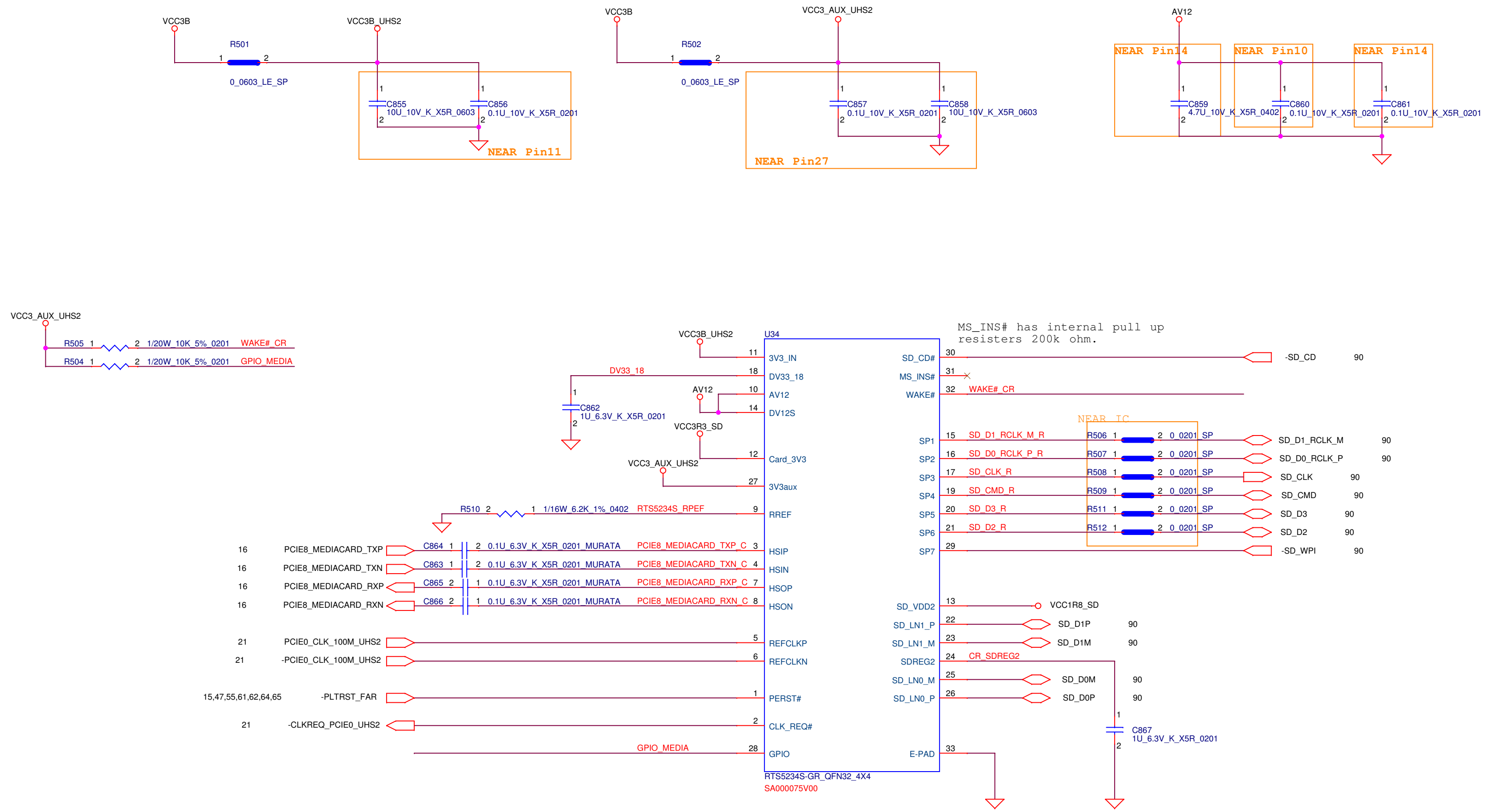
# FINGERPRINT



# Card Reader

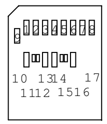



| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| | Rev 1.0 — Title: MEDIA CARD UHS-II(R) |
| | Date: Friday, May 15, 2020 — Sheet 89 of 133 |

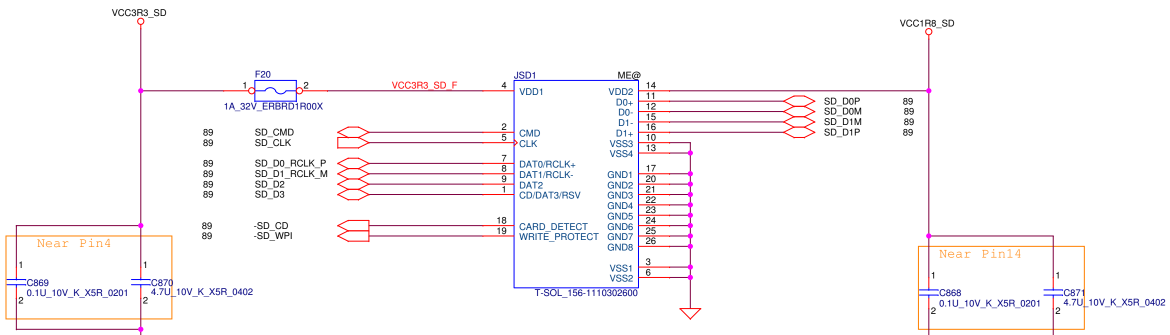
# Card Reader

| Normal type UHS-II SD Slot Pin No | SD Mode | UHS II Mode |
|---|---|---|
| 1 | CD/DAT3 | |
| 2 | CMD | |
| 3 | VSS1 | |
| 4 | VDD | VDD1 |
| 5 | CLK | |
| 6 | VSS2 | |
| 7 | DAT0 | RCLKP |
| 8 | DAT1 | RCLKM |
| 9 | DAT2 | |
| 10 | | VSS3 |
| 11 | | D0P |
| 12 | | D0M |
| 13 | | VSS4 |
| 14 | | VDD2 |
| 15 | | D1M |
| 16 | | D1P |
| 17 | | VSS5 |
| CD | CARD DETECT | |
| WP | WRITE PROTECT | |

Bottom View



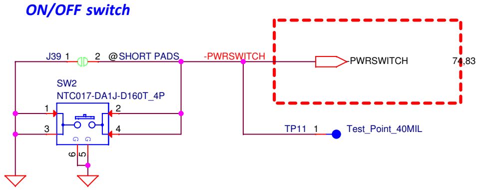

| UHS II Interface | UHS I Inteface |
|---|---|
| 4 VDD1 3.3V | 1 CD/DAT3 |
| 7 RCLKP | 2 CMD |
| 8 RCLKM | 3 VSS1 |
| 10 VSS3 | 4 VDD 3.3V |
| 11 D0P | 5 CLK |
| 12 D0M | 6 VSS2 |
| 13 VSS4 | 7 DAT0 |
| 14 VDD2 1.8V | 8 DAT1 |
| 15 D1M | 9 DAT2 |
| 16 D1P | |
| 17 VSS5 | |

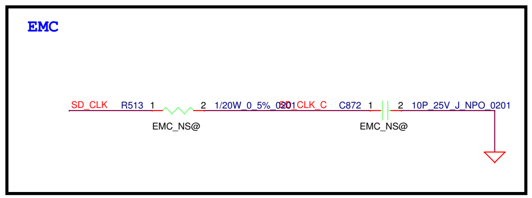


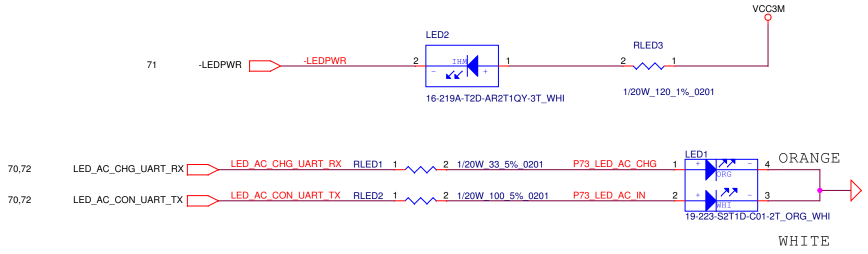

CD : Low => Insertion Card
High => No Card
WP : Low => Write Protection on
High => Write Protection off or No Card

# ON/OFF switch

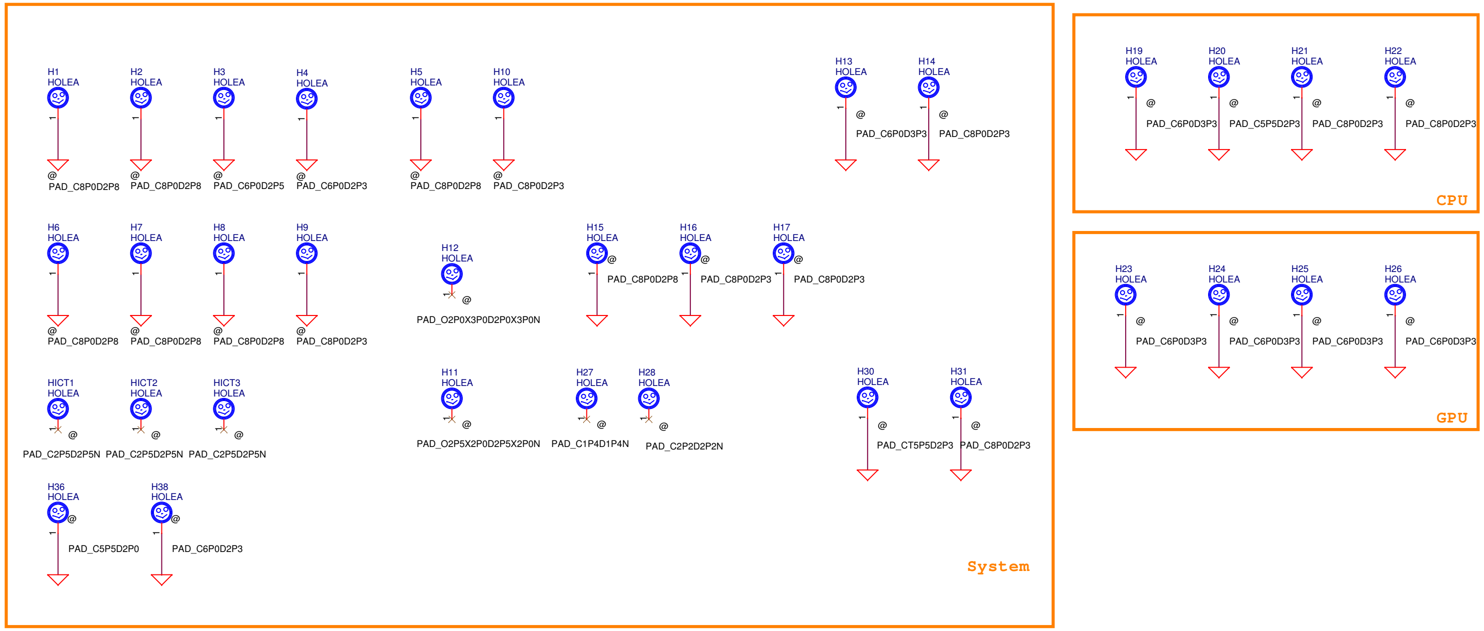
*ON/OFF switch*






| TABLE of LED1 | | |
|---|---|---|
| Vendor | Description | P/N |
| EVERLIGHT | 19-223/S2T1D-C01/2T 1.6X1.5 ORG/WH | SC50000GS00 |
| LITE ON | LTW-C195DSKF-LC 1.6X1.5 ORANGE/WHI | SC50000H800 |




LC Future Center Secret Data

Project Name

TpPv

Rev 1.0

Title BLANK

Date: Friday, May 15, 2020

| LC Future Center Secret Data | Project Name: TpPv |
| --- | --- |
| LCFC | Rev 1.0 — Title: BLANK |
| | Date: Friday, May 15, 2020 — Sheet 95 of 133 |

LC Future Center Secret Data

Project Name

TpPv

Rev 1.0

Title

BLANK

Date: Friday, May 15, 2020

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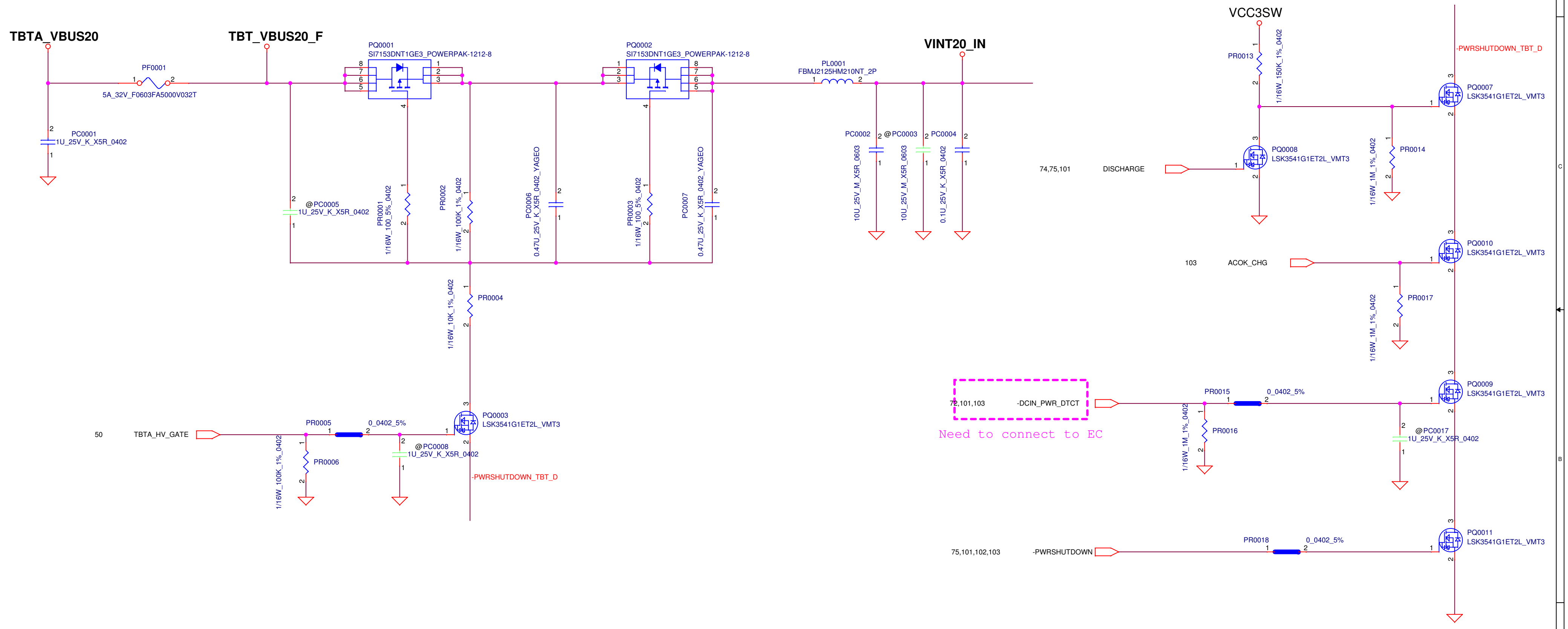
| | |
|---|---|
| Project Name | TpPv |
| Rev 1.0 | Title BLANK |
| Date: Friday, May 15, 2020 | Sheet 99 of 133 |




LC Future Center Secret Data

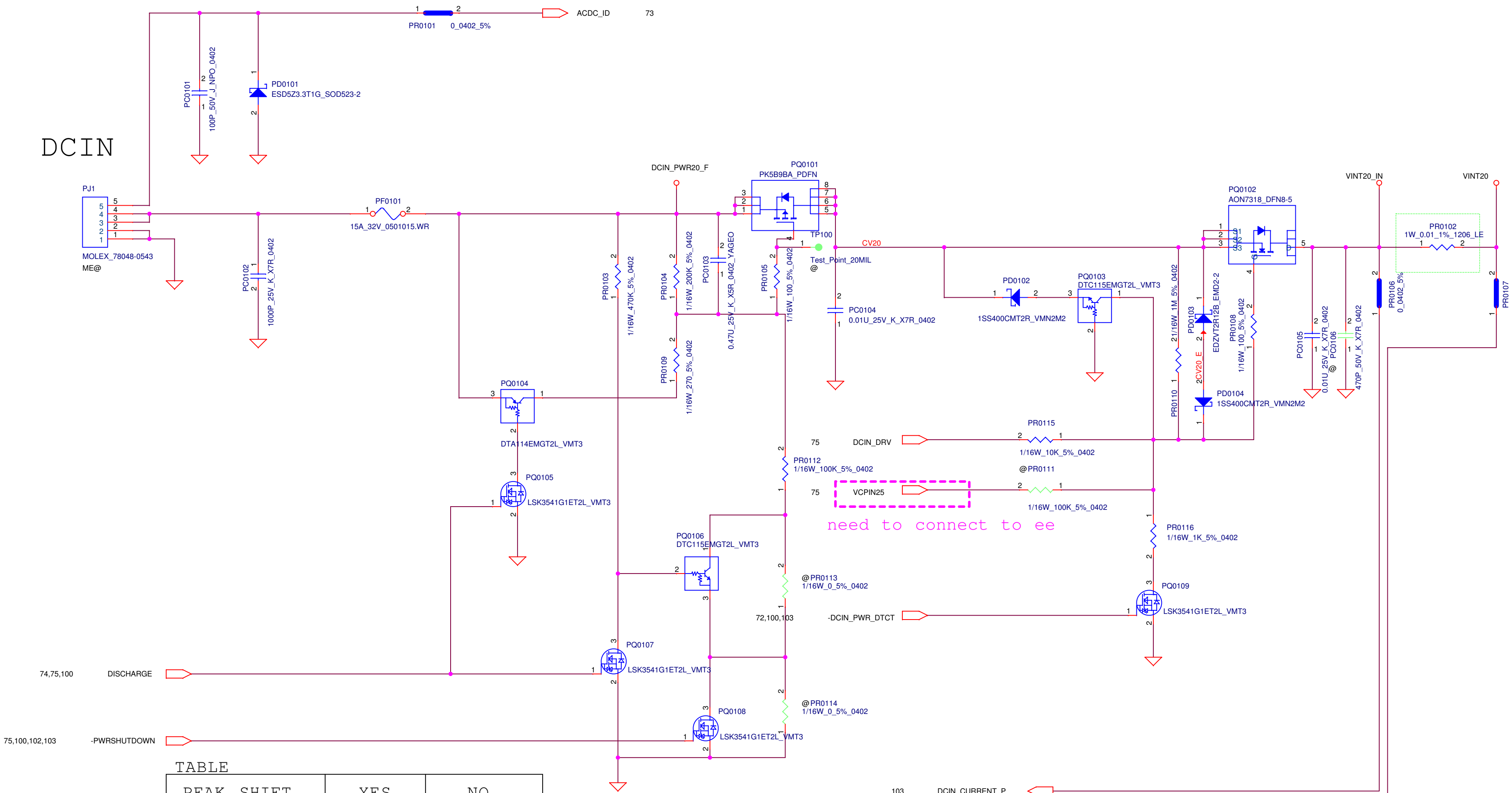
LCFC

Project Name: TpPv

Rev 1.0

Title: Type C Adapter

Date: Friday, May 15, 2020




TABLE

| PEAK SHIFT | YES | NO |
|---|---|---|
| PR0113 | NO-ASM | ASM |
| PR0103 | ASM | NO-ASM |
| PQ0106 | ASM | NO-ASM |
| PQ0107 | ASM | NO-ASM |

LOGIC

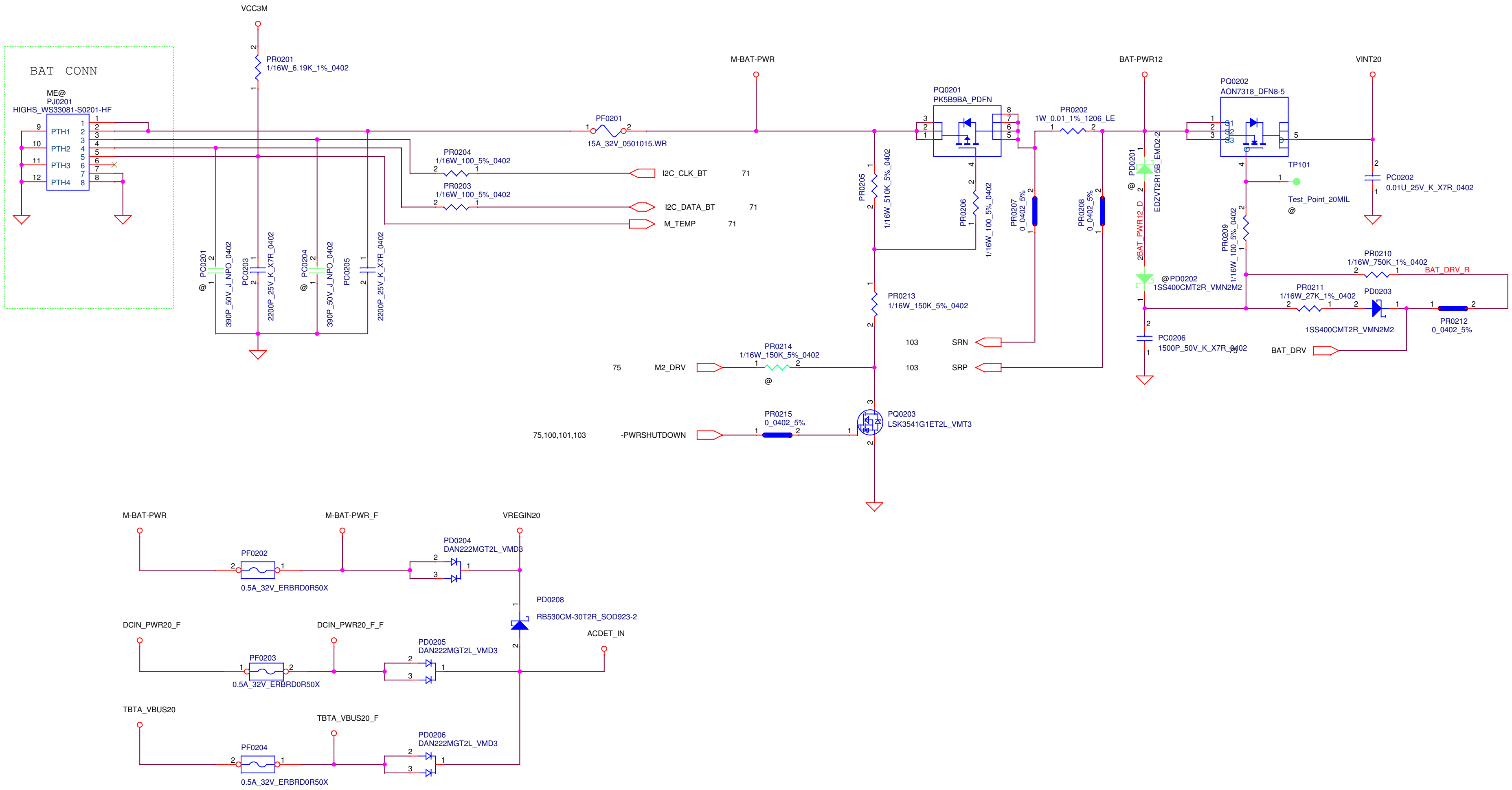


Project Name: TpPv

Rev 1.0

Title: DC-IN

Date: Friday, May 15, 2020




LC Future Center Secret Data

LCFC

Project Name: TpPv

Rev 1.0

Title: BATTERY INPUT

Date: Friday, May 15, 2020

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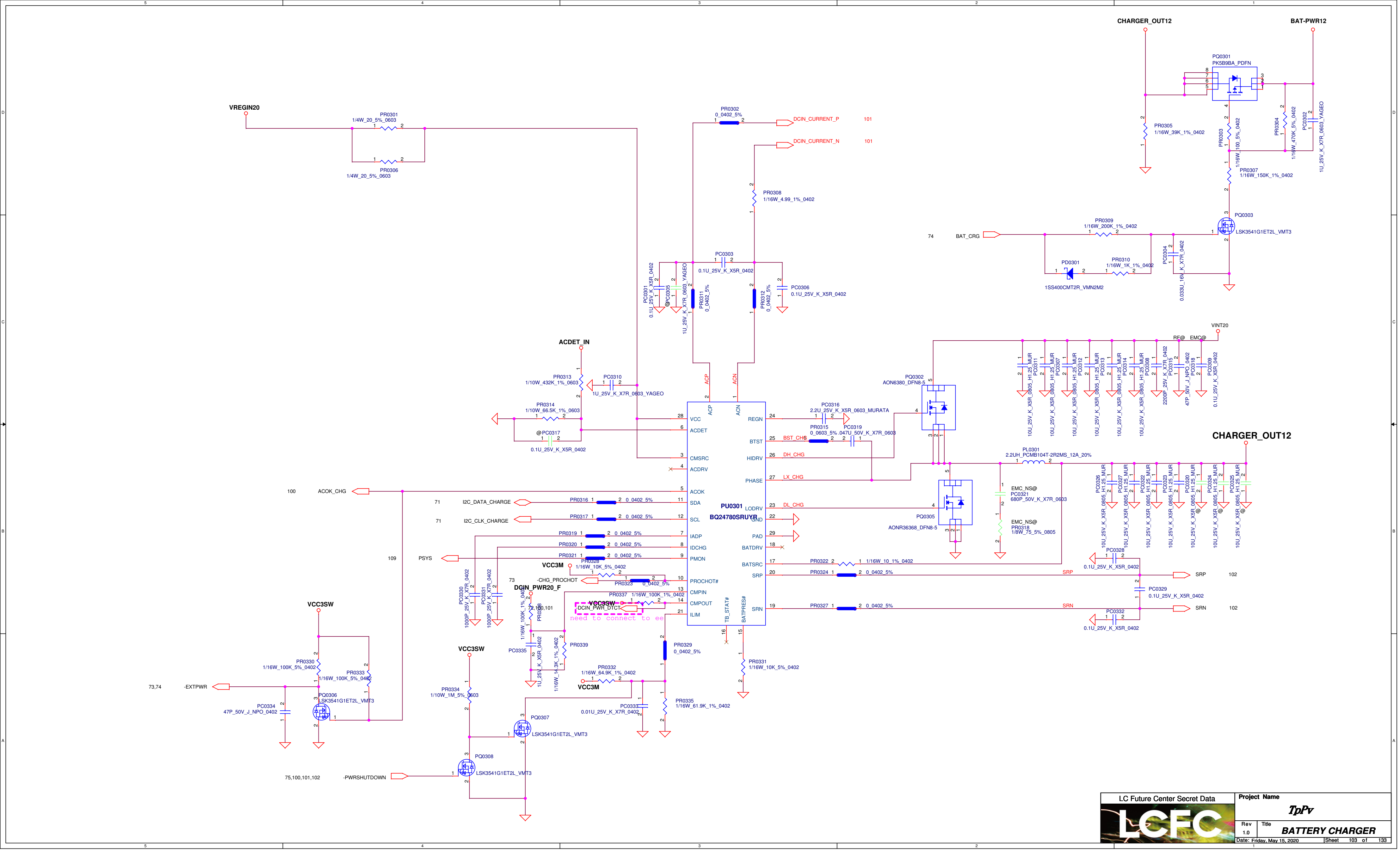
CHARGER_OUT12
BAT-PWR12
PQ0301
PK5B9BA_PDFN
PR0305
1/16W_39K_1%_0402
PR0303
1/16W_100_5%_0402
PR0304
1/16W_470K_5%_0402
PC0302
1U_25V_K_X7R_0603_YAGEO
PR0307
1/16W_150K_1%_0402
PQ0303
LSK3541G1ET2L_VMT3
BAT_CRG
PR0309
1/16W_200K_1%_0402
PD0301
1SS400CMT2R_VMN2M2
PR0310
1/16W_1K_1%_0402
PC0304
0.033U_16V_K_X7R_0402
VREGIN20
PR0301
1/4W_20_5%_0603
PR0306
1/4W_20_5%_0603
PR0302
0_0402_5%
DCIN_CURRENT_P
DCIN_CURRENT_N
101
PR0308
1/16W_4.99_1%_0402
PC0303
0.1U_25V_K_X5R_0402
PC0301
0.1U_25V_K_X5R_0402
@PC0305
1U_25V_K_X7R_0603_YAGEO
PR0311
0_0402_5%
PR0312
0_0402_5%
PC0306
0.1U_25V_K_X5R_0402
VINT20
RF@ EMC@
ACDET_IN
PR0313
1/10W_432K_1%_0603
PC0310
1U_25V_K_X7R_0603_YAGEO
PR0314
1/10W_66.5K_1%_0603
@PC0317
0.1U_25V_K_X5R_0402
PQ0302
AON6380_DFN8-5
PC0316
2.2U_25V_K_X5R_0603_MURATA
PR0315
0_0603_5%
PC0319
.047U_50V_K_X7R_0603
PU0301
BQ24780SRUYR
VCC ACDET CMSRC ACDRV ACOK SDA SCL IADP IDCHG PMON PROCHOT# CMPIN CMPOUT ILIM
ACP ACN REGN BTST HIDRV PHASE LODRV GND PAD BATDRV BATSRC SRP SRN TB_STAT# BATPRES#
BST_CHG DH_CHG LX_CHG DL_CHG
PL0301
2.2UH_PCMB104T-2R2MS_12A_20%
CHARGER_OUT12
EMC_NS@
PC0321
680P_50V_K_X7R_0603
EMC_NS@
PR0318
1/8W_75_5%_0805
PQ0305
AONR36368_DFN8-5
ACOK_CHG
I2C_DATA_CHARGE
I2C_CLK_CHARGE
PR0316 0_0402_5%
PR0317 0_0402_5%
PR0319 0_0402_5%
PR0320 0_0402_5%
PR0321 0_0402_5%
PSYS
VCC3M
PR0328
1/16W_10K_5%_0402
-CHG_PROCHOT
PR0323
0_0402_5%
DCIN_PWR20_F
PR0337
1/16W_100K_1%_0402
VCC3SW
DCIN_PWR_DTCT
need to connect to ee
PR0322
1/16W_10_1%_0402
PR0324 0_0402_5%
PR0327 0_0402_5%
PC0328
0.1U_25V_K_X5R_0402
PC0329
0.1U_25V_K_X5R_0402
PC0332
0.1U_25V_K_X5R_0402
SRP SRN 102
PC0330
1000P_25V_K_X7R_0402
PC0331
1000P_25V_K_X7R_0402
PR0338
1/16W_100K_1%_0402
PC0335
1U_25V_K_X5R_0402
PR0339
1/16W_14.3K_1%_0402
PR0329
0_0402_5%
PR0331
1/16W_10K_5%_0402
PR0332
1/16W_64.9K_1%_0402
PC0333
0.01U_25V_K_X7R_0402
PR0335
1/16W_61.9K_1%_0402
PR0330
1/16W_100K_5%_0402
PR0333
1/16W_100K_5%_0402
-EXTPWR
PC0334
47P_50V_J_NPO_0402
PQ0306
LSK3541G1ET2L_VMT3
PR0334
1/10W_1M_5%_0603
PQ0307
LSK3541G1ET2L_VMT3
PQ0308
LSK3541G1ET2L_VMT3
-PWRSHUTDOWN
75,100,101,102
LC Future Center Secret Data
Project Name
TpPv
Rev 1.0
Title
BATTERY CHARGER
Date: Friday, May 15, 2020
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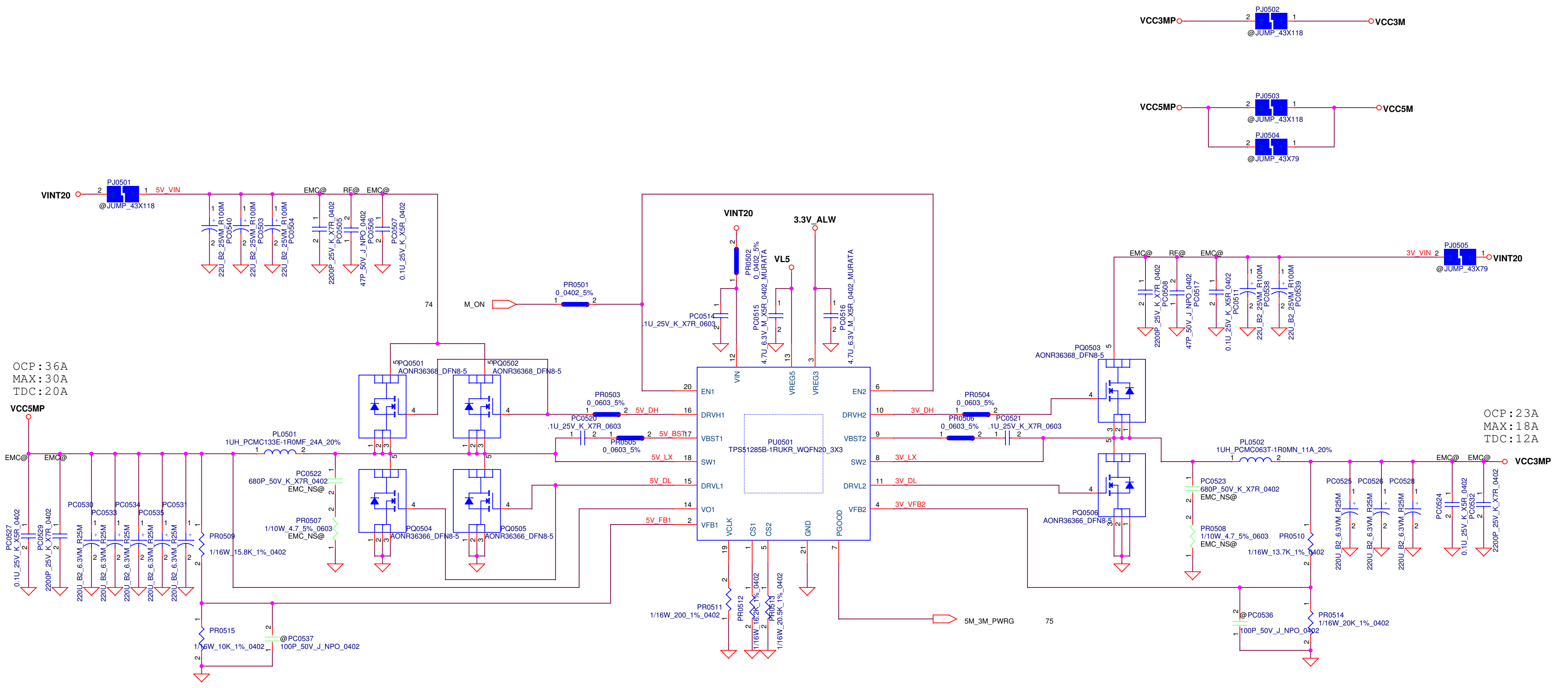
| LC Future Center Secret Data | Project Name | |
|---|---|---|
| LCFC | TpPv | |
| | Rev 1.0 | Title BLANK |
| | Date: Friday, May 15, 2020 | Sheet 104 of 133 |



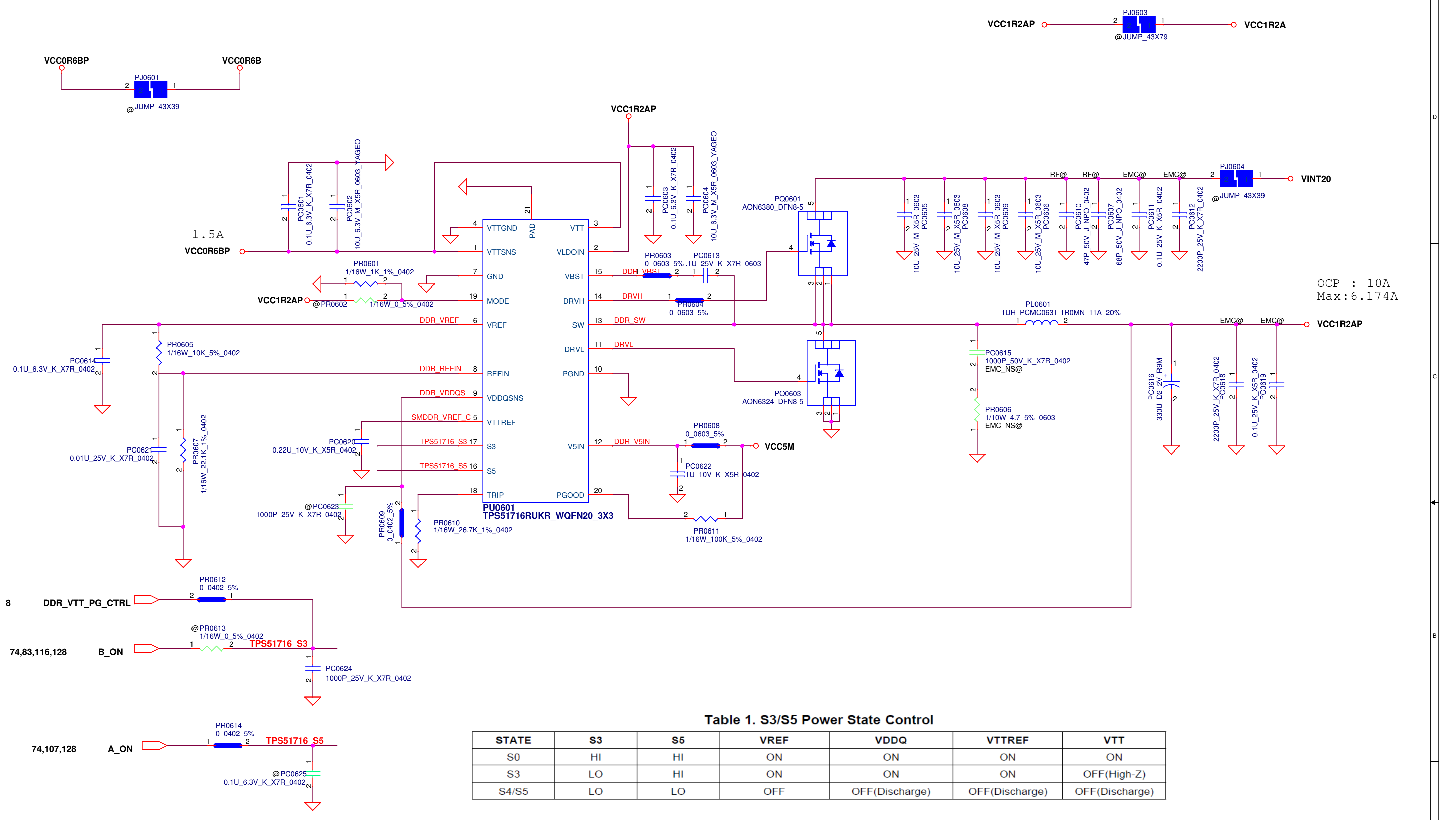

LC Future Center Secret Data

Project Name: TpPv

Rev 1.0

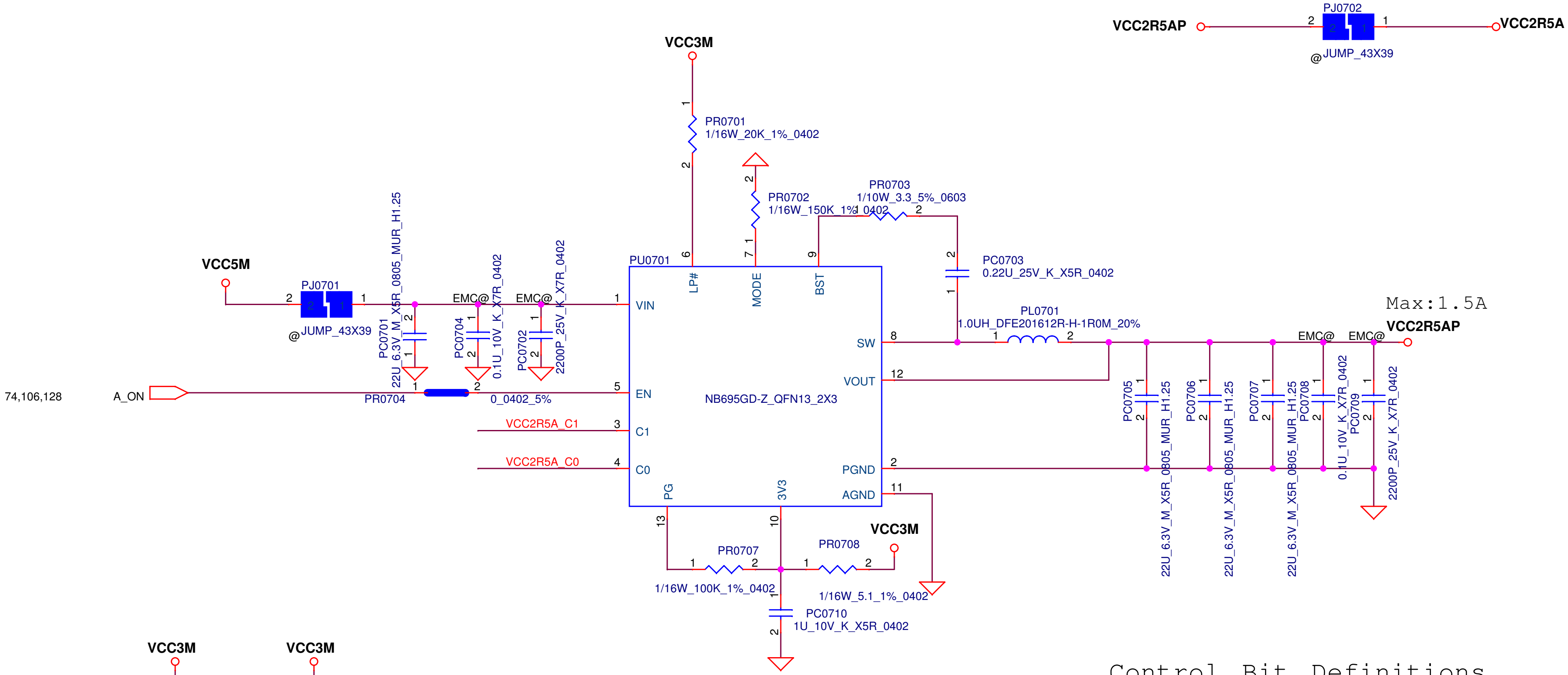
Title: DC/DC VCC5M/VCC3M

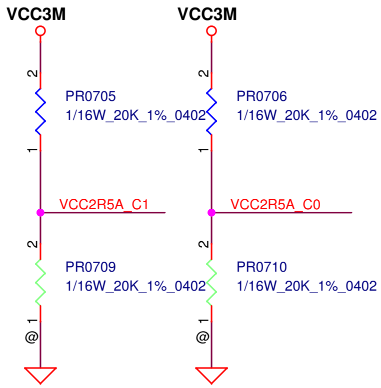
Date: Friday, May 15, 2020




## Table 1. S3/S5 Power State Control

| STATE | S3 | S5 | VREF | VDDQ | VTTREF | VTT |
|---|---|---|---|---|---|---|
| S0 | HI | HI | ON | ON | ON | ON |
| S3 | LO | HI | ON | ON | ON | OFF(High-Z) |
| S4/S5 | LO | LO | OFF | OFF(Discharge) | OFF(Discharge) | OFF(Discharge) |




## Control Bit Definitions

| LP# | C1 | C0 | VOUT(V) |
|---|---|---|---|
| 1 | 0 | 0 | 1.2 |
| 1 | 0 | 1 | 1.5 |
| 1 | 1 | 0 | 1.8 |
| 1 | 1 | 1 | 2.5 |

LC Future Center Secret Data

| Project Name | | |
|---|---|---|
| TpPv | | |
| Rev 1.0 | Title | DC/DC VCC2R5A |
| Date: Friday, May 15, 2020 | Sheet 107 of 133 | |

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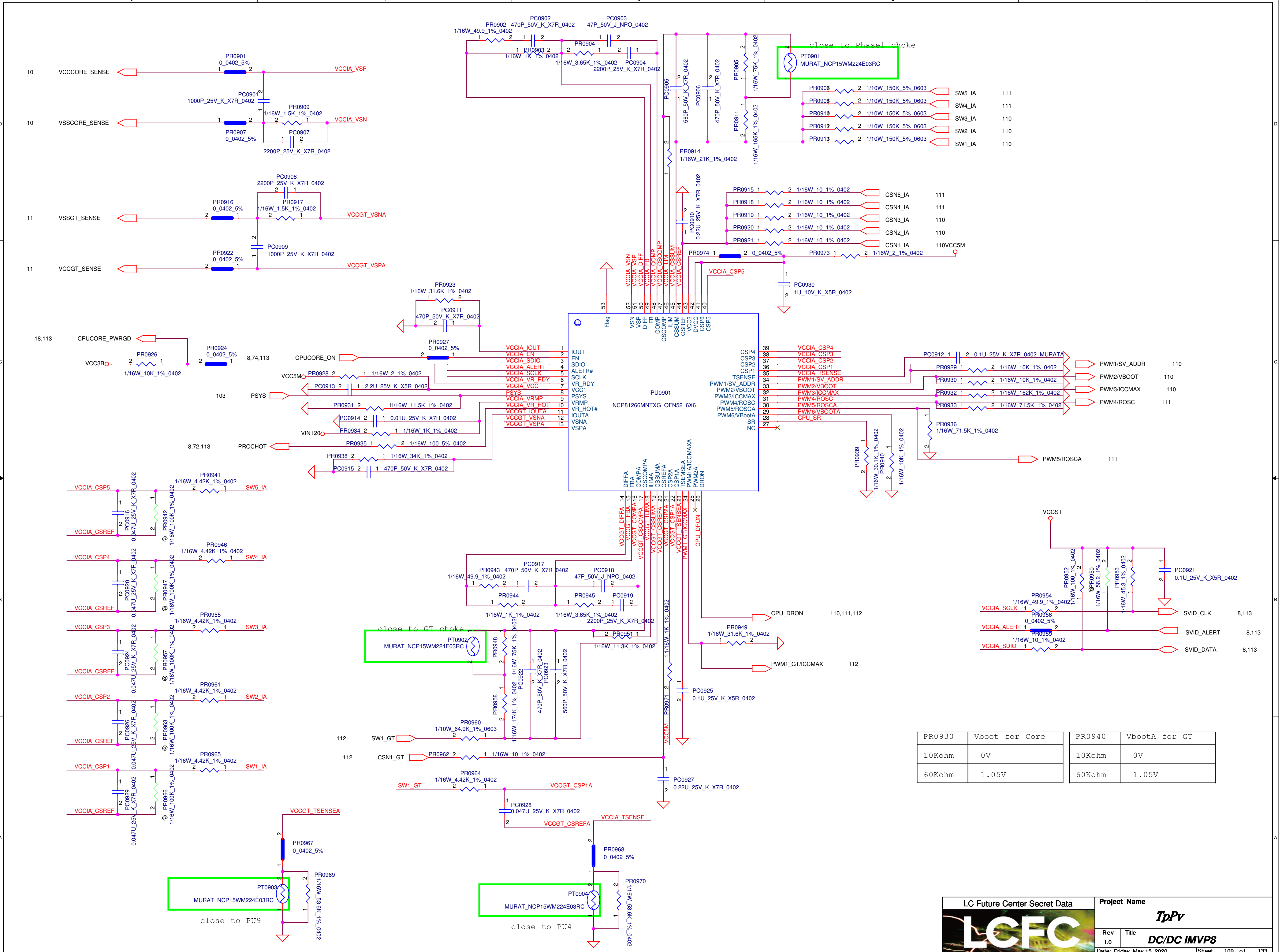
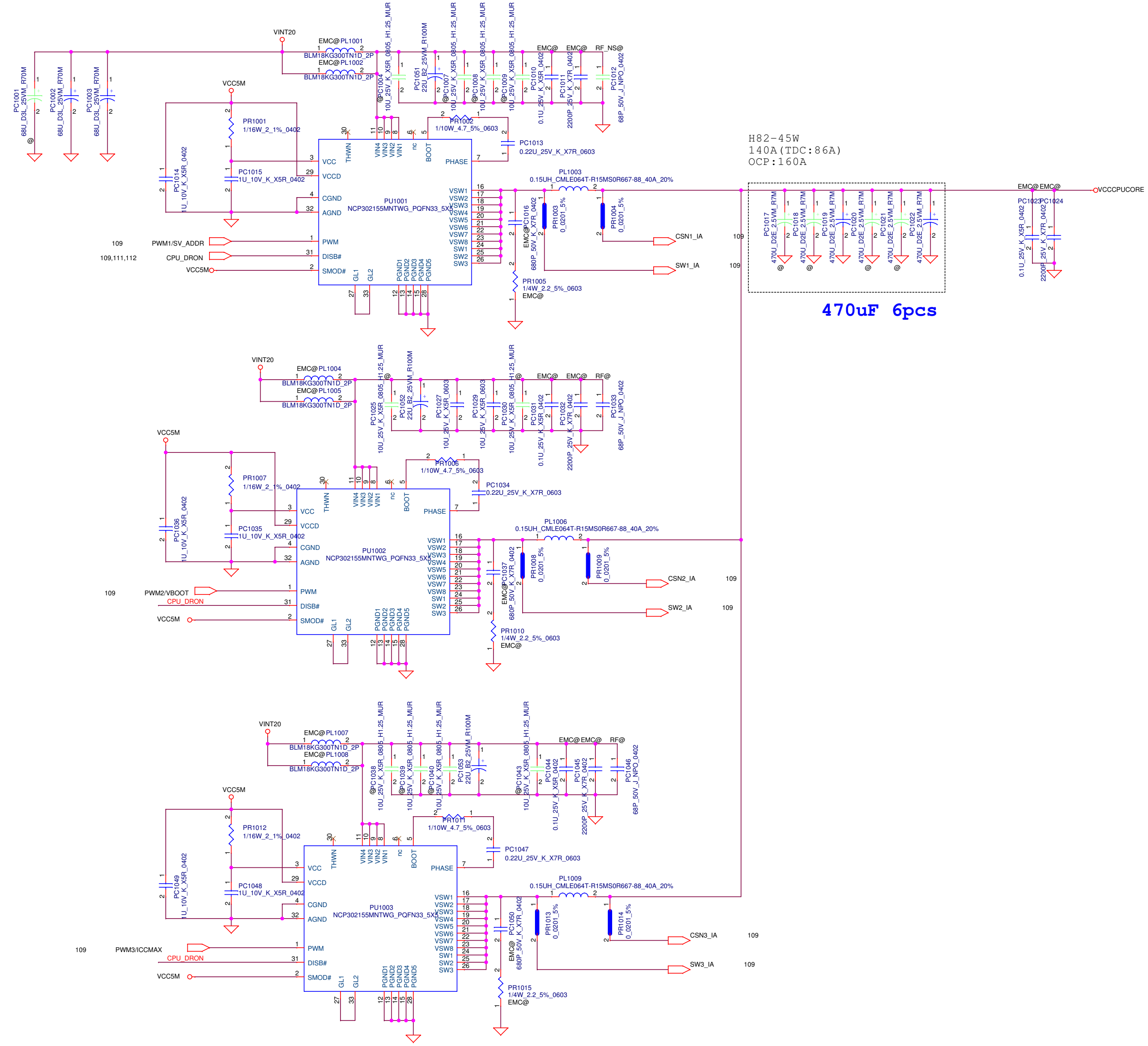



| PR0930 | Vboot for Core |
|---|---|
| 10Kohm | 0V |
| 60Kohm | 1.05V |

| PR0940 | VbootA for GT |
|---|---|
| 10Kohm | 0V |
| 60Kohm | 1.05V |




LC Future Center Secret Data

Project Name: TpPv

Rev: 1.0

Title: DC/DC VCCPUCORE 1

Date: Friday, May 15, 2020

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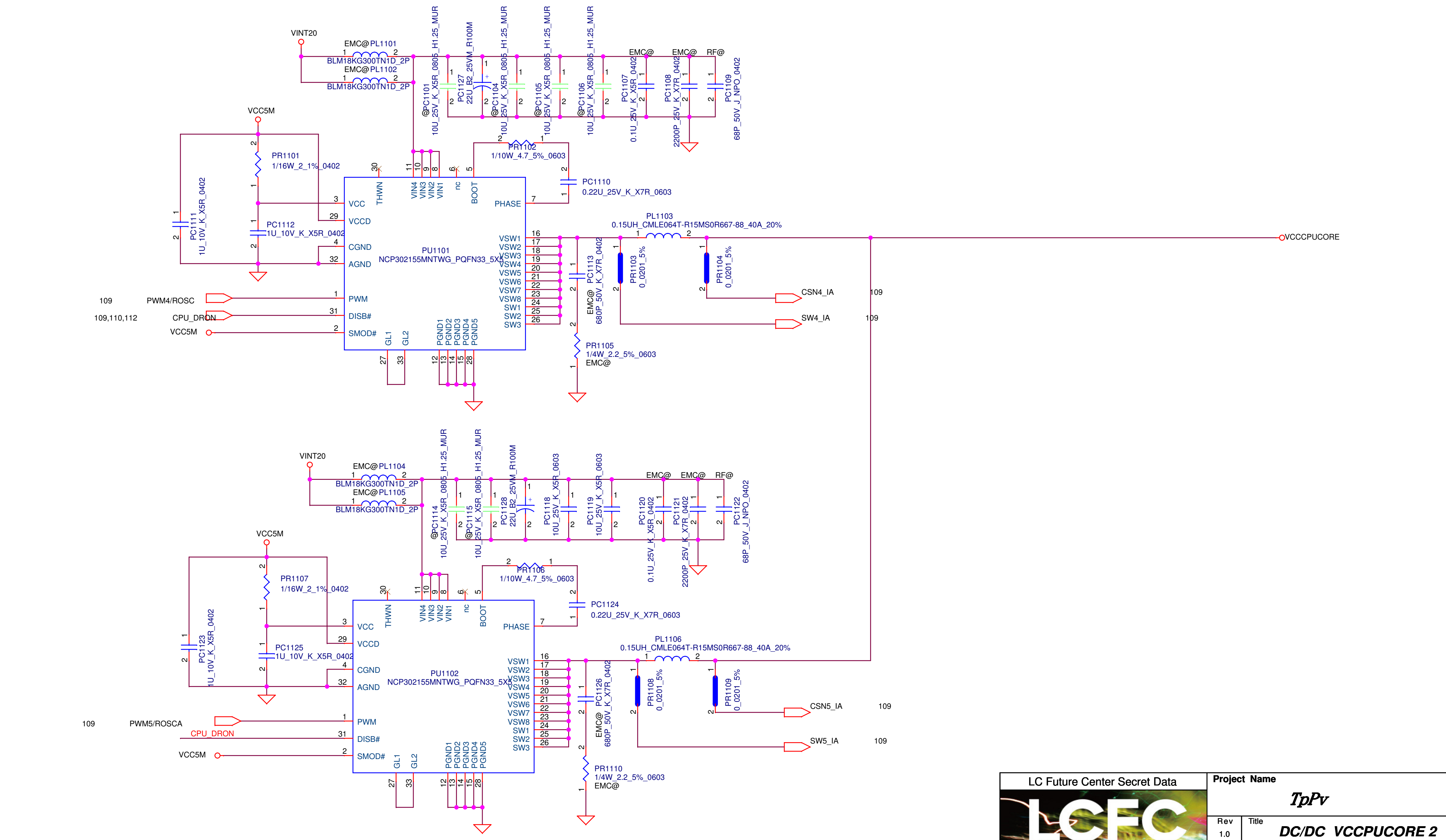


LC Future Center Secret Data

Project Name: TpPv

Rev 1.0

Title: DC/DC VCCPUCORE 2

Date: Friday, May 15, 2020

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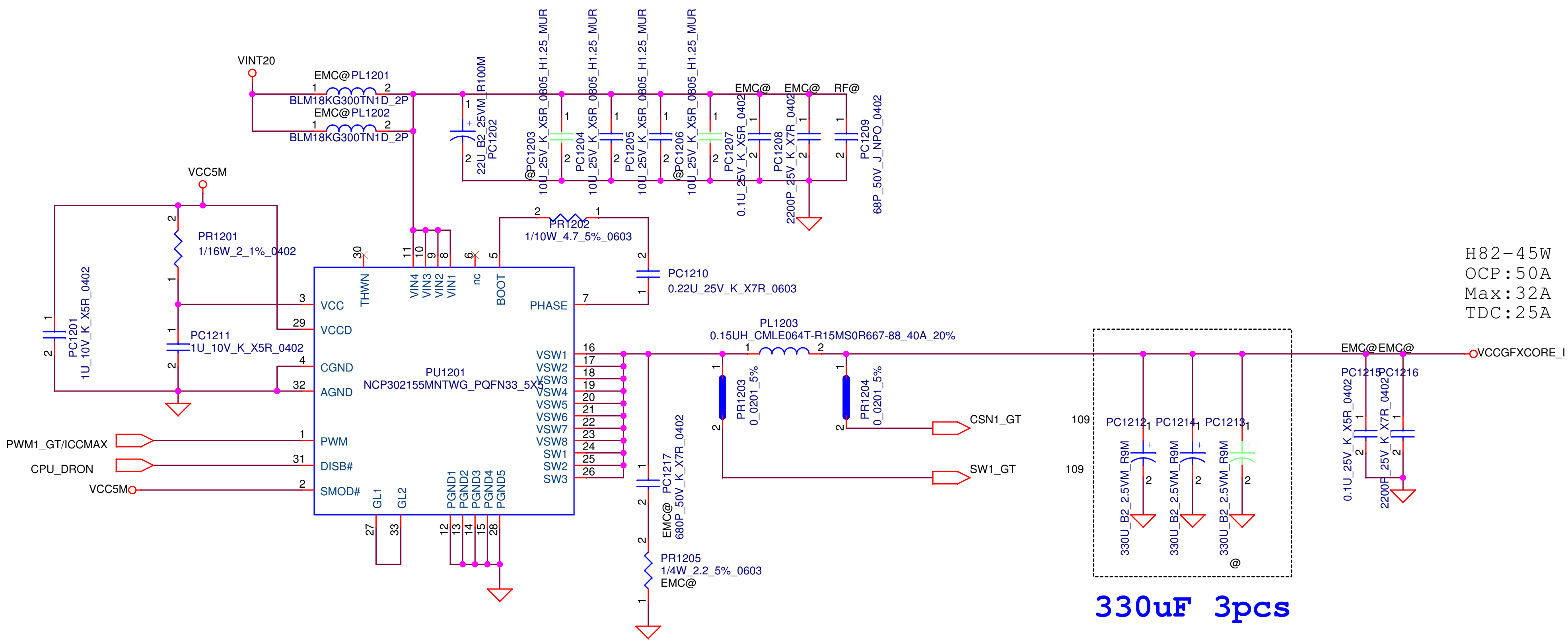
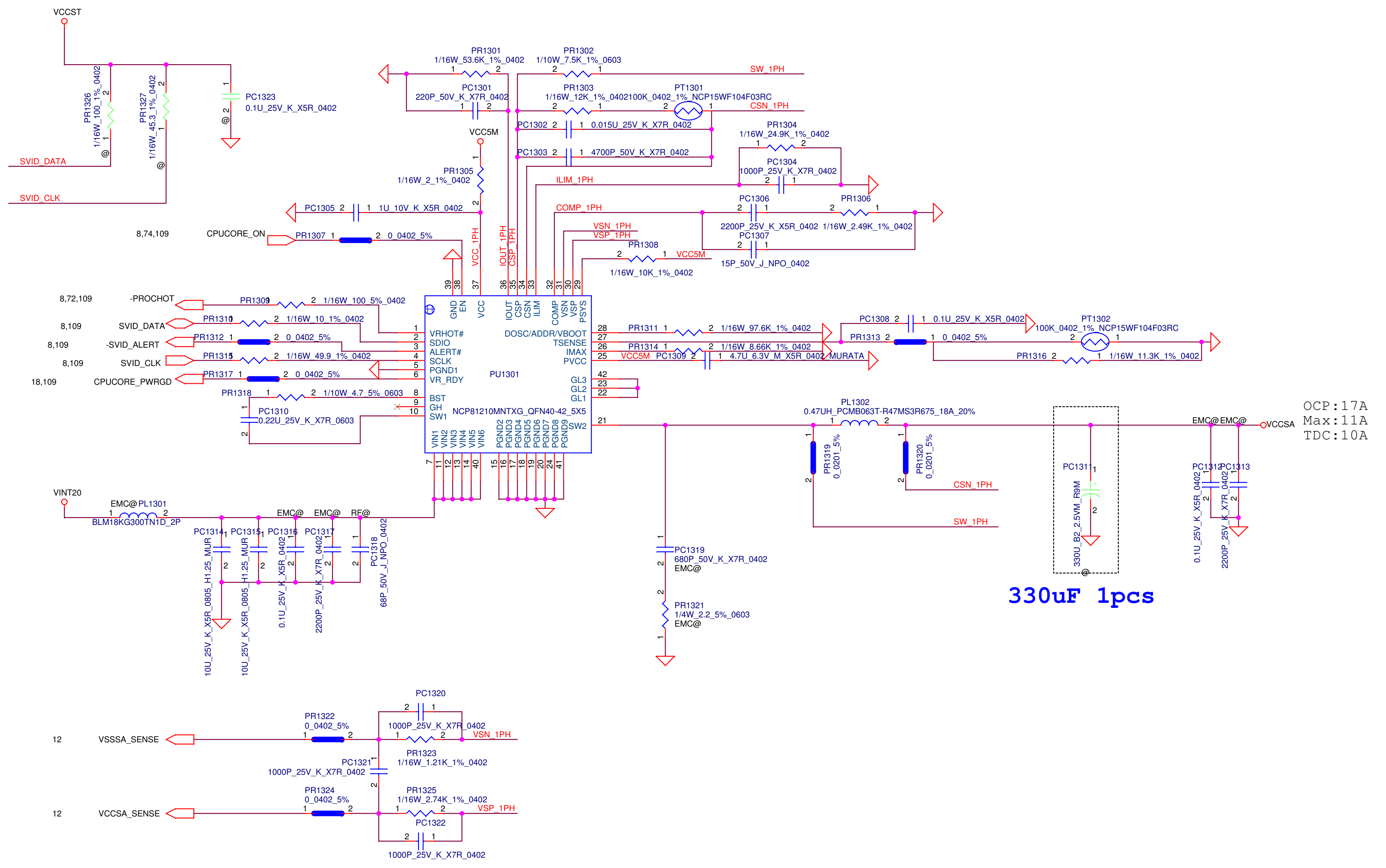


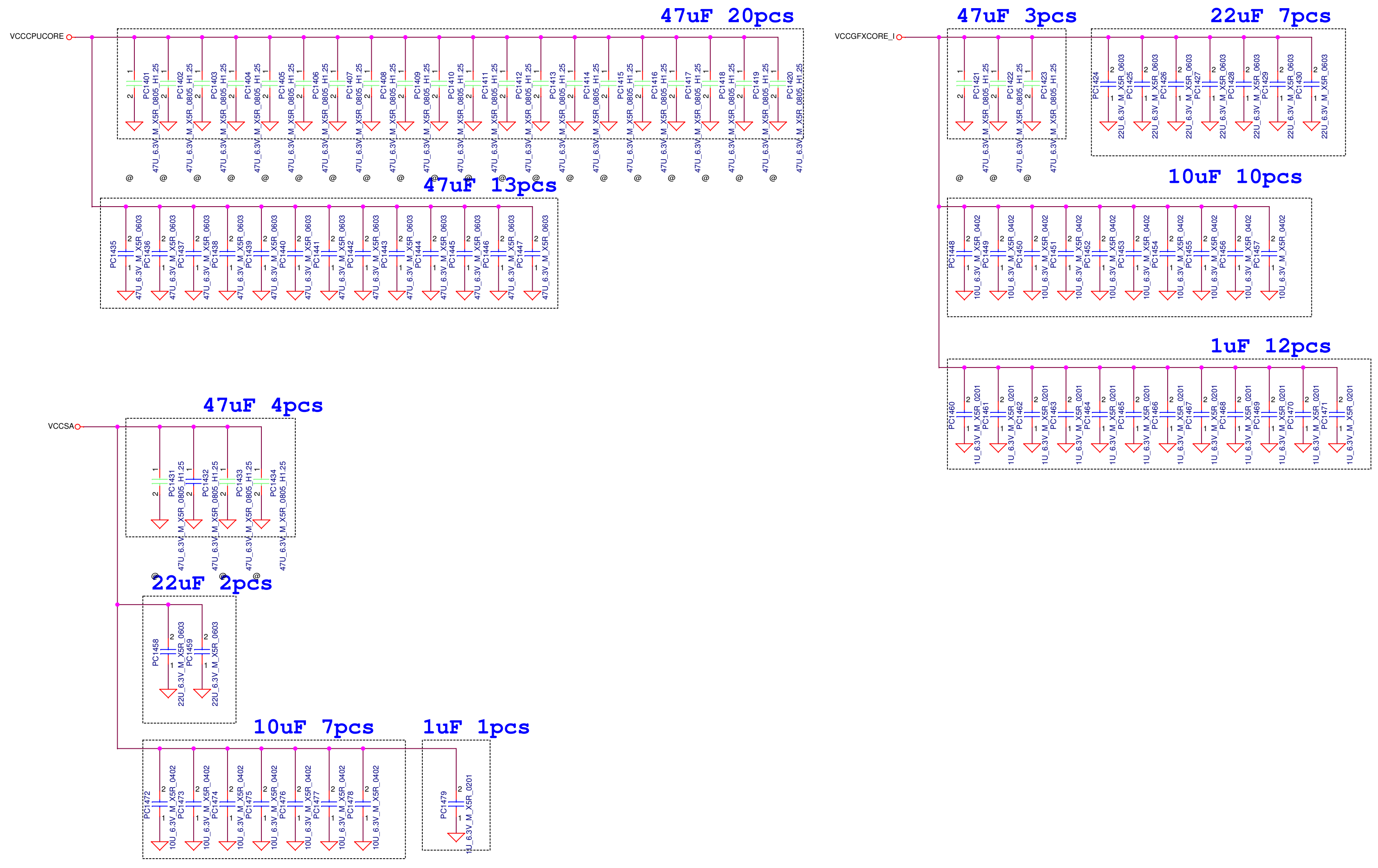

H82-45W
OCP:50A
Max:32A
TDC:25A

330uF 3pcs

| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| LCFC | Rev 1.0 — Title: DC/DC VCCGFXCORE_I |
| | Date: Friday, May 15, 2020 — Sheet 112 of 133 |




| | |
|---|---|
| LC Future Center Secret Data | Project Name: TpPv |
| LCFC | Rev 1.0 — Title: DC/DC VCCSA |
| | Date: Friday, May 15, 2020 — Sheet 113 of 133 |



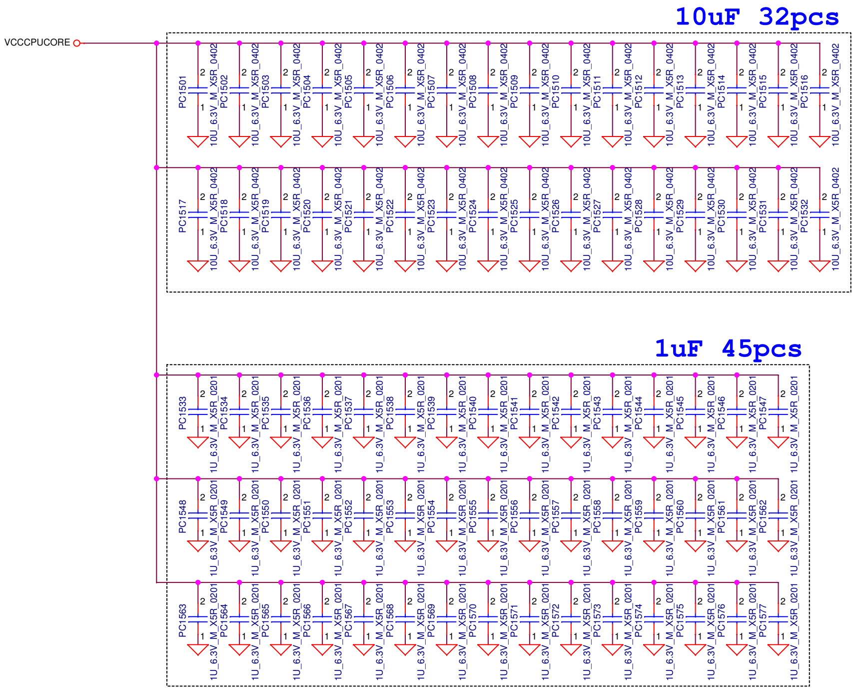

LC Future Center Secret Data

Project Name: TpPv

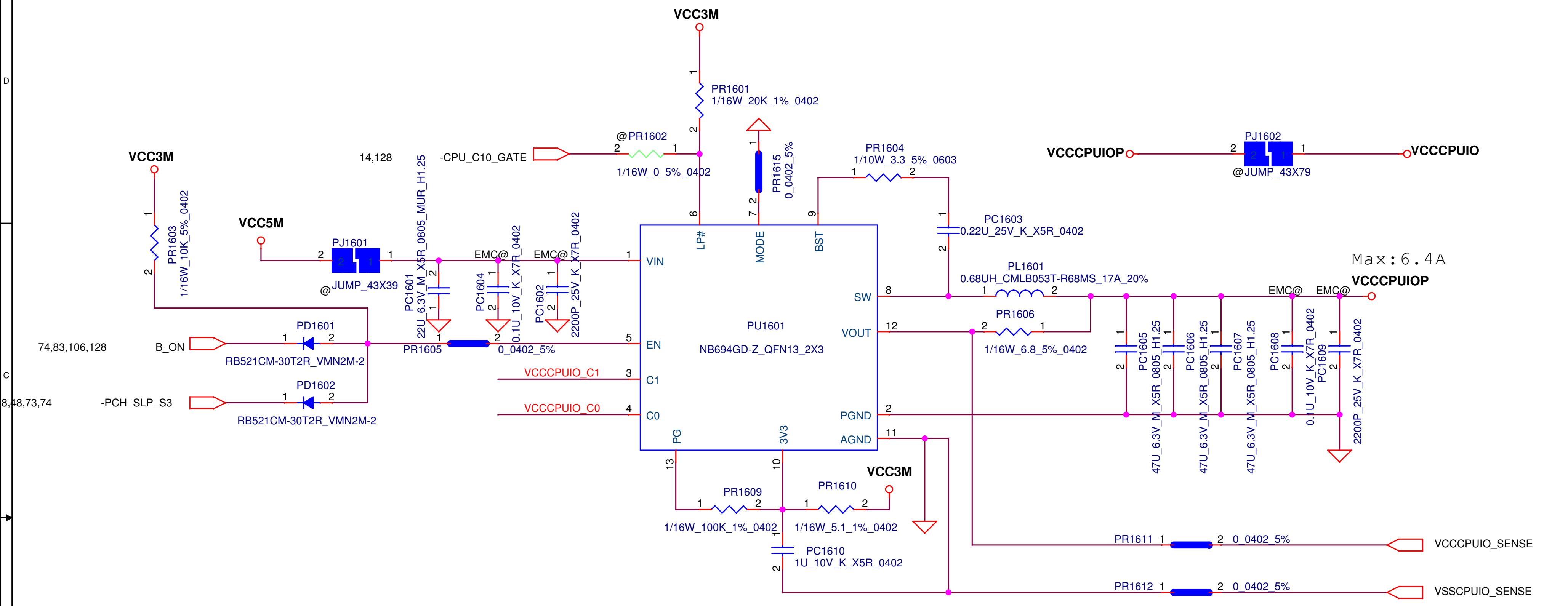
Rev 1.0

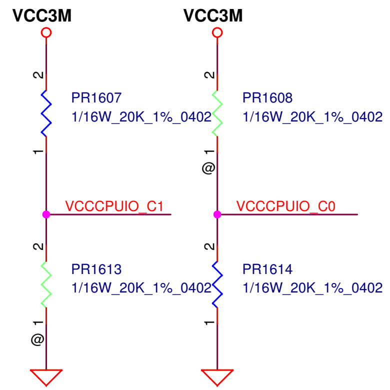
Title: VCCPUCORE DECOUPLING 1

Date: Friday, May 15, 2020




| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| LCFC | Rev 1.0 — Title: VCCPUCORE DECOUPLING 2 |
| | Date: Friday, May 15, 2020 — Sheet 115 of 133 |




Control Bit Definitions

| LP# | C1 | C0 | VOUT(V) |
|---|---|---|---|
| 0 | X | X | 0 |
| 1 | 0 | 0 | 0.85 |
| 1 | 0 | 1 | 0.875 |
| 1 | 1 | 0 | 0.95 |
| 1 | 1 | 1 | 0.975 |



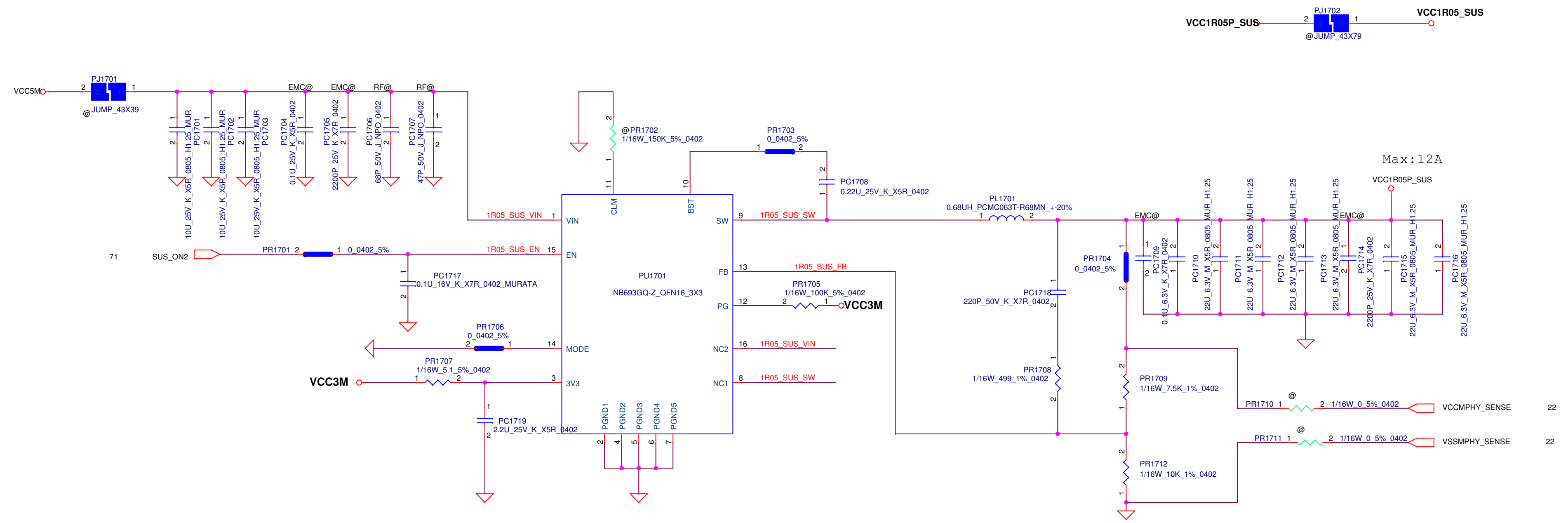
LCFC

Project Name: TpPv

Rev 1.0

Title: DC/DC VCCCPUIO

Date: Friday, May 15, 2020




LC Future Center Secret Data

LCFC

Project Name: TpPv

Title: DC/DC VCC1R05_SUS

Rev 1.0

Date: Friday, May 15, 2020

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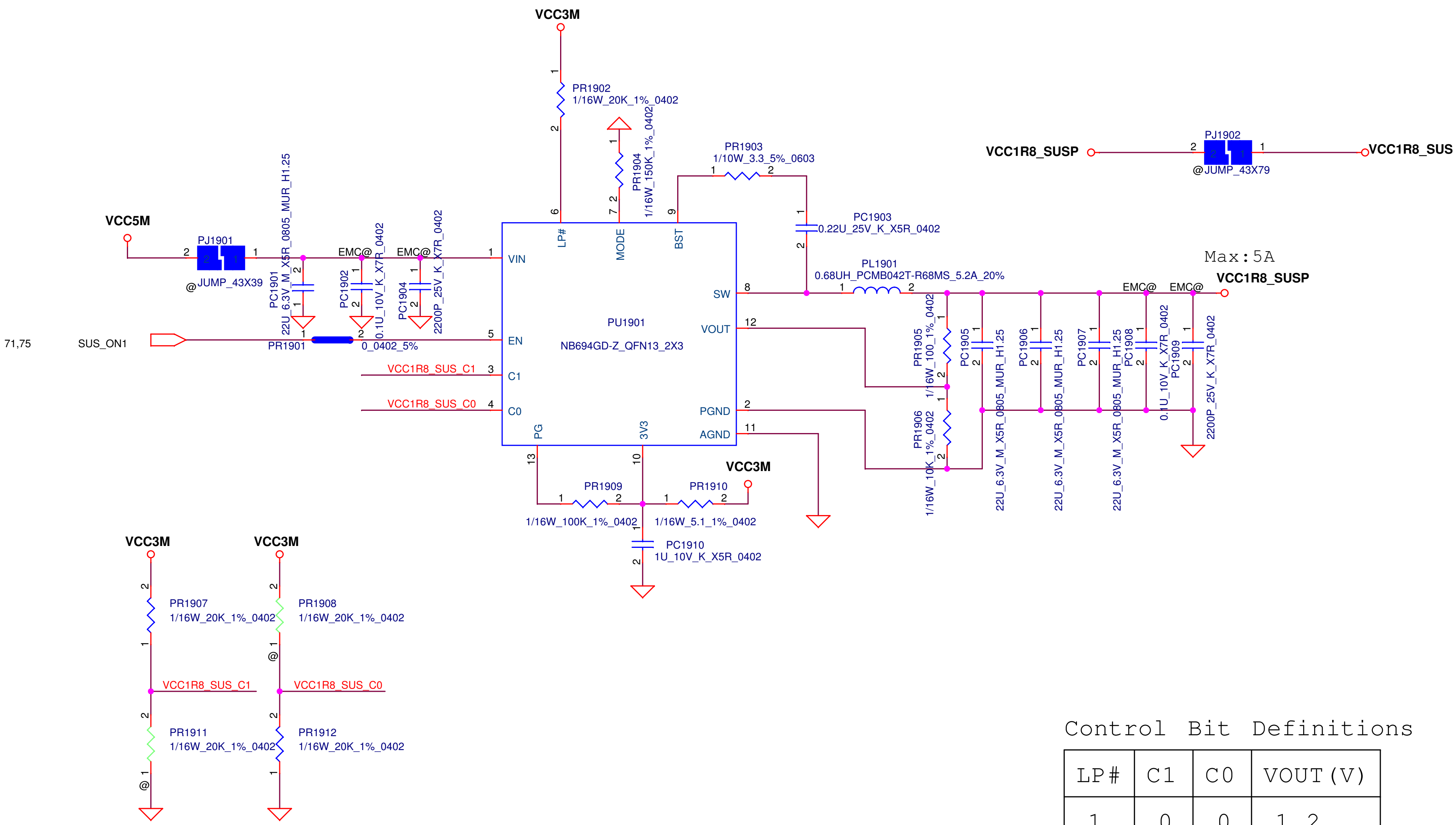
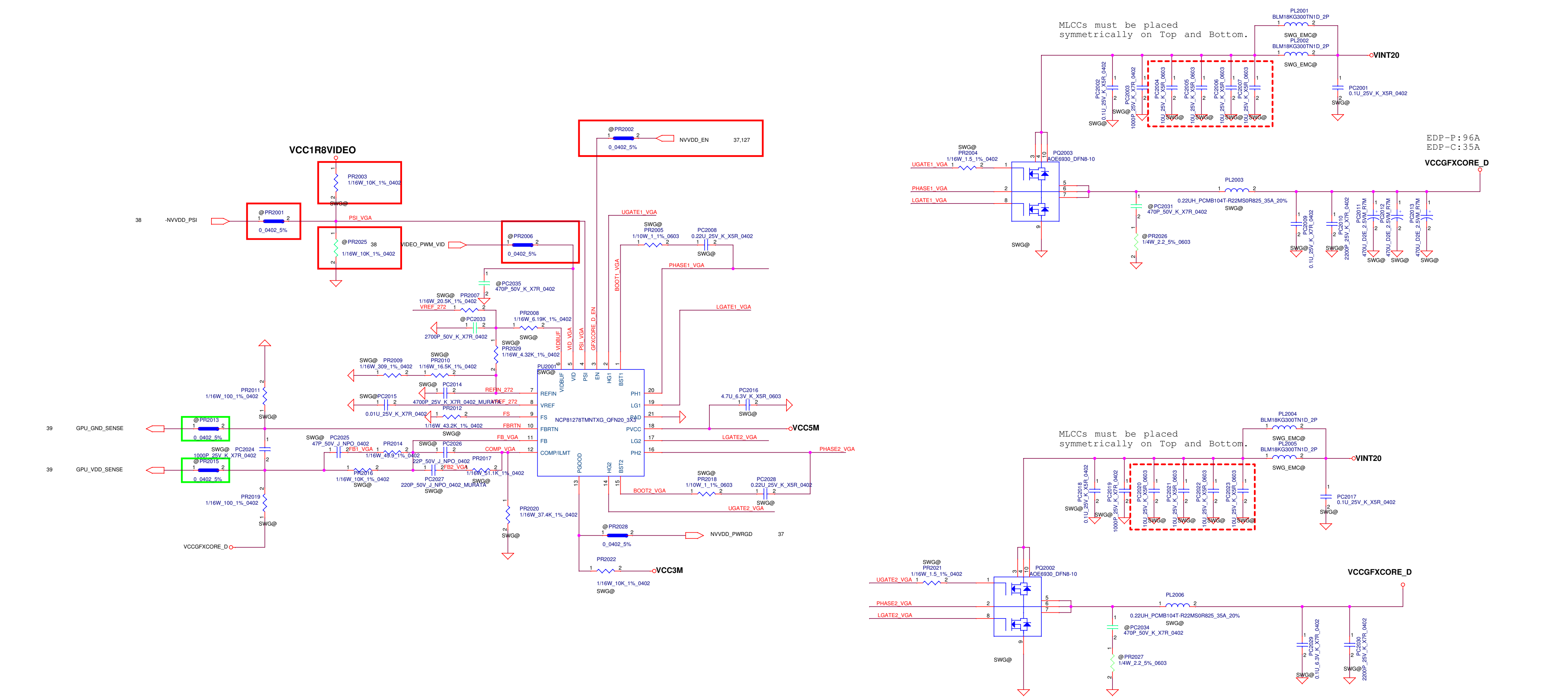



Control Bit Definitions

| LP# | C1 | C0 | VOUT(V) |
|---|---|---|---|
| 1 | 0 | 0 | 1.2 |
| 1 | 0 | 1 | 1.5 |
| 1 | 1 | 0 | 1.8 |
| 1 | 1 | 1 | 2.5 |




| LC Future Center Secret Data | Project Name TpPv |
|---|---|
| LCFC | Rev 1.0 Title DC/DC VCCGFXCORE_D IC |
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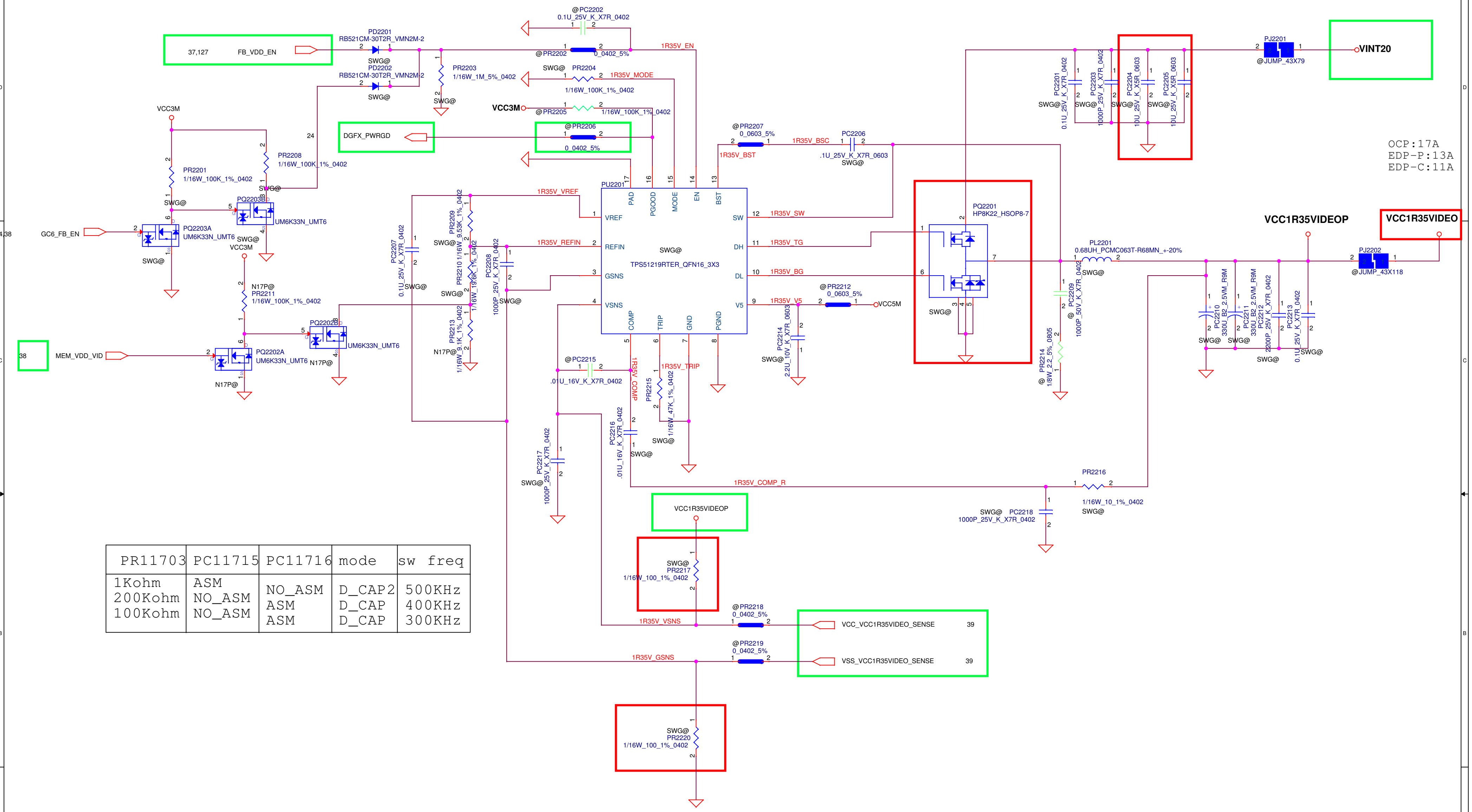
LC Future Center Secret Data

| Project Name | | |
|---|---|---|
| *TpPv* | | |
| Rev 1.0 | Title | **BLANK** |
| Date: Friday, May 15, 2020 | Sheet 121 of 133 | |




| PR11703 | PC11715 | PC11716 | mode | sw freq |
|---|---|---|---|---|
| 1Kohm | ASM | NO_ASM | D_CAP2 | 500KHz |
| 200Kohm | NO_ASM | ASM | D_CAP | 400KHz |
| 100Kohm | NO_ASM | ASM | D_CAP | 300KHz |

| | PR2213 | PR2211 | PQ2202 | VCC1R35VIDEO |
|---|---|---|---|---|
| N19M | 0 ohm | No stuff | No stuff | 1.35V |
| N17P | 9.1K ohm | 100k | stuff | MEM_VDD_VID = H --> 1.5V<br>MEM_VDD_VID = L --> 1.35V |

LC Future Center Secret Data

LCFC

Project Name: TpPv

Title: DC/DC VCC1R35VIDEO

Rev 1.0

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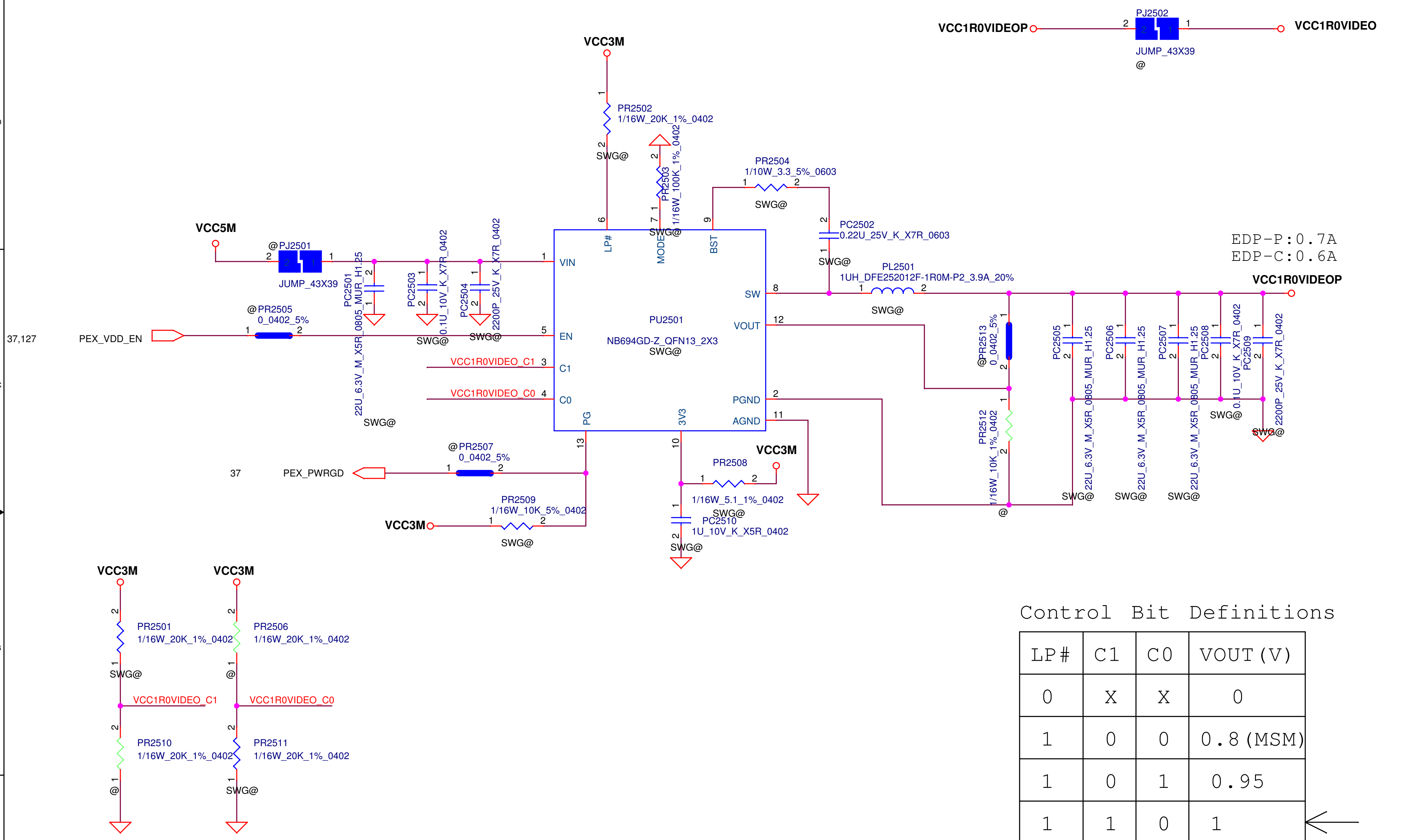
| LC Future Center Secret Data | Project Name |
|---|---|
| LCFC | TpPv |
| | Rev 1.0 / Title: BLANK |
| | Date: Friday, May 15, 2020 / Sheet 124 of 133 |




Control Bit Definitions

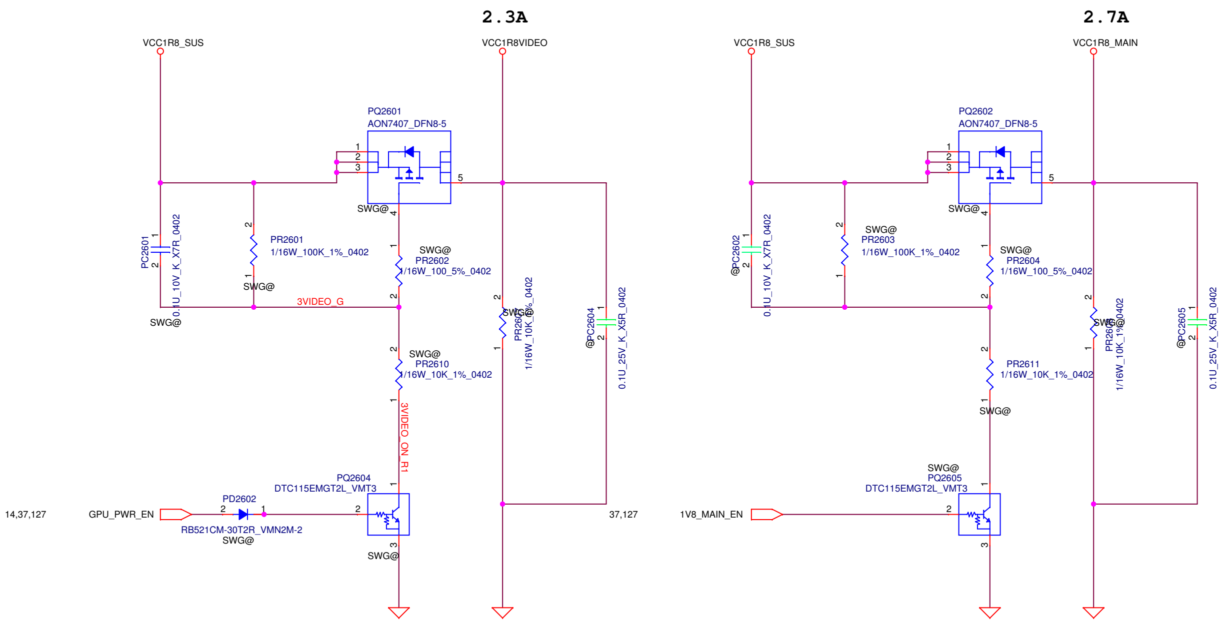
| LP# | C1 | C0 | VOUT(V) |
|---|---|---|---|
| 0 | X | X | 0 |
| 1 | 0 | 0 | 0.8(MSM) |
| 1 | 0 | 1 | 0.95 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1.05 |

LC Future Center Secret Data

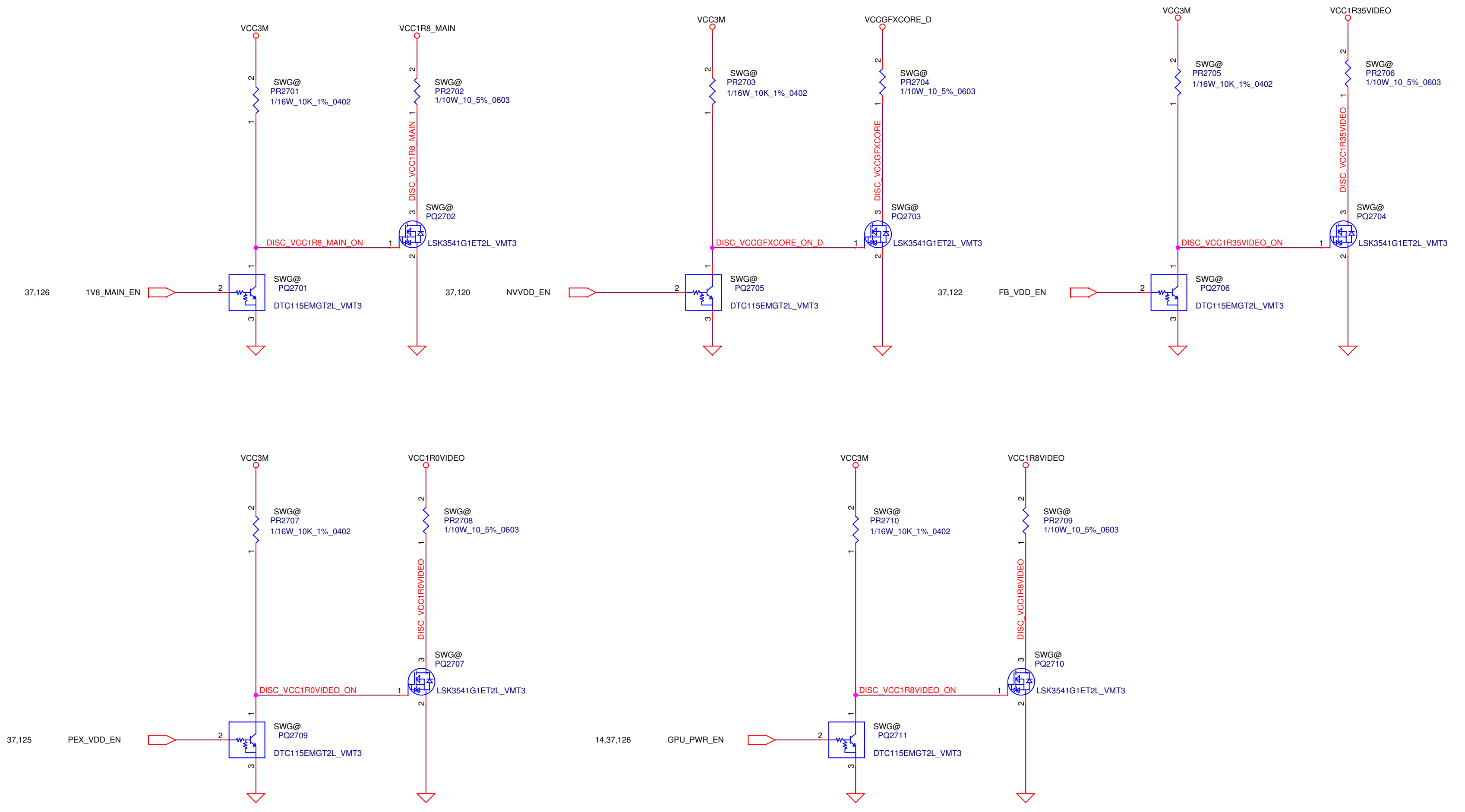
Project Name: TpPv

Rev 1.0 | Title: VCC1R0VIDEO

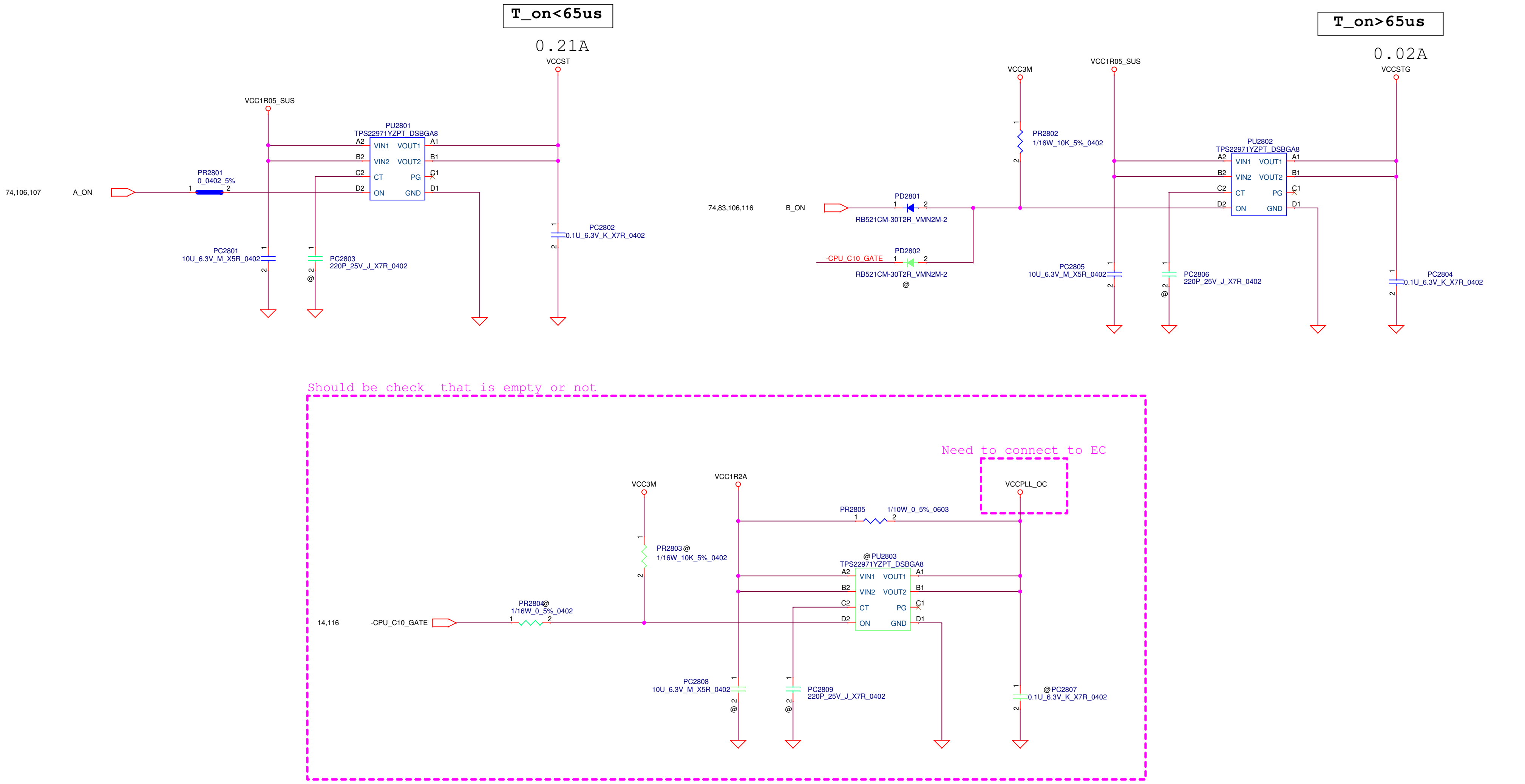
Date: Friday, May 15, 2020 | Sheet 125 of 133



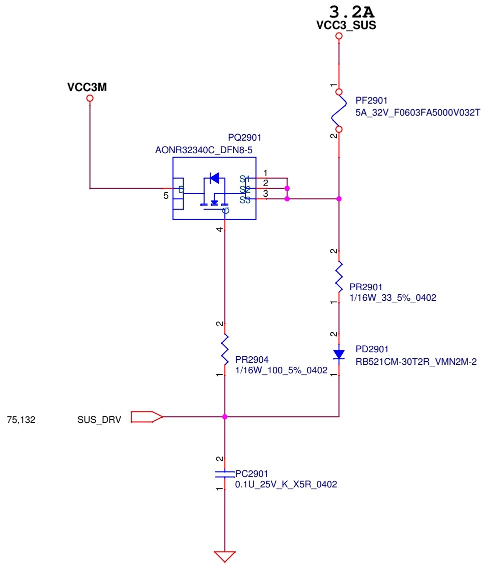

| LC Future Center Secret Data | Project Name: TpPv |
|---|---|
| LCFC | Rev 1.0 — Title: LOAD SW VIDEO/3SUS |
| Date: Friday, May 15, 2020 | Sheet 126 of 133 |




| LC Future Center Secret Data | Project Name: TpPv |
| --- | --- |
| Rev 1.0 | Title: DISCHARGE CIRUIT VIDEO |
| Date: Friday, May 15, 2020 | Sheet 127 of 133 |




| | | |
|---|---|---|
| LC Future Center Secret Data | Project Name | TpPv |
| | Rev 1.0 | Title LOAD SW VCCST/VCCSTG |
| | Date: Friday, May 15, 2020 | Sheet 128 of 133 |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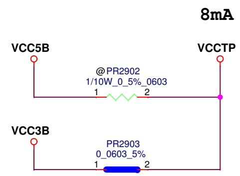
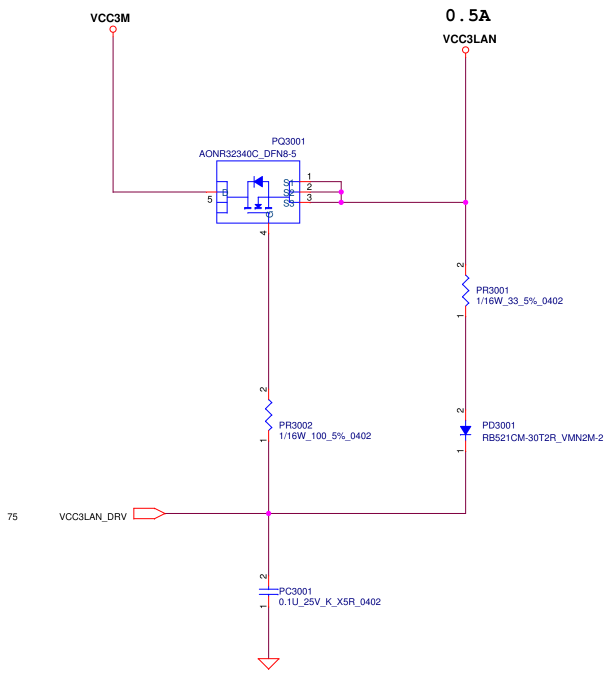
VCC3_SUS
PF2901
5A_32V_F0603FA5000V032T
VCC3M
PQ2901
AONR32340C_DFN8-5
PR2901
1/16W_33_5%_0402
PR2904
1/16W_100_5%_0402
PD2901
RB521CM-30T2R_VMN2M-2
75,132
SUS_DRV
PC2901
0.1U_25V_K_X5R_0402


8mA
VCC5B
VCCTP
@PR2902
1/10W_0_5%_0603
VCC3B
PR2903
0_0603_5%



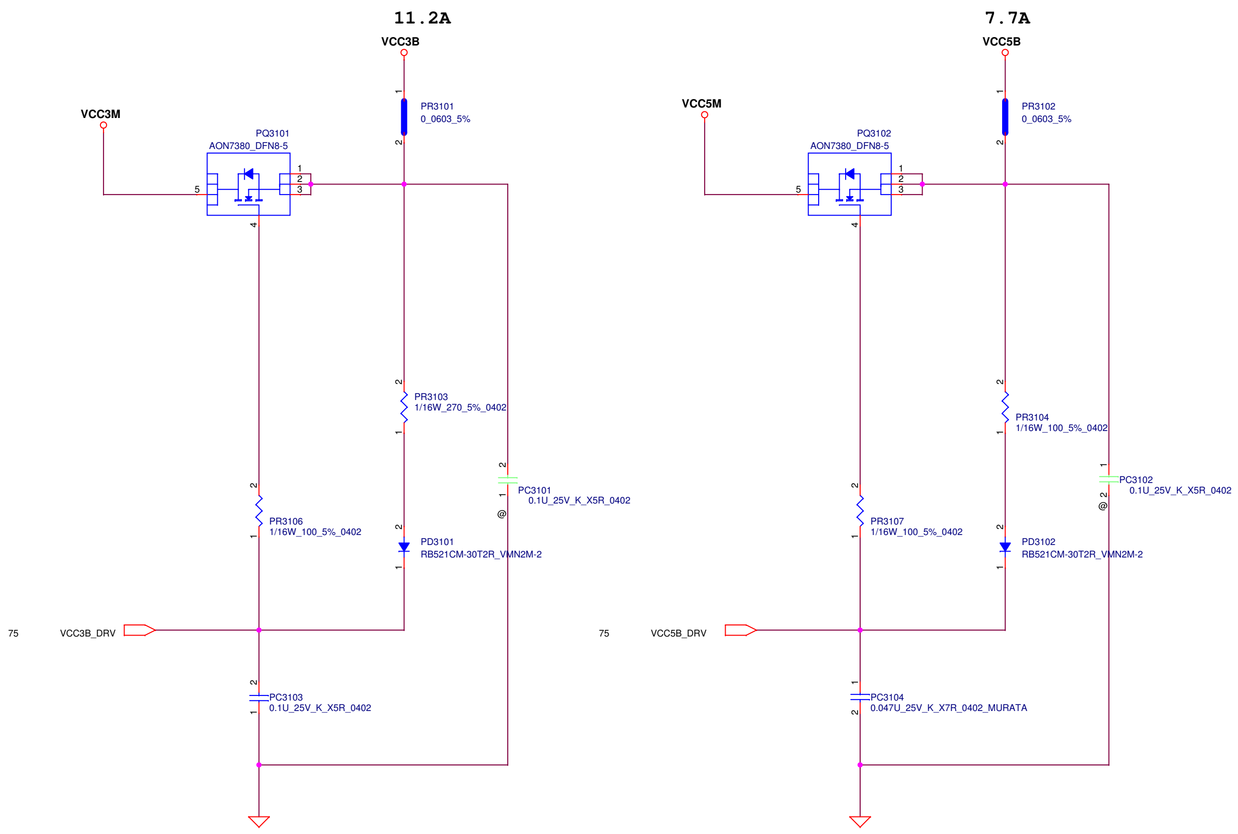

LC Future Center Secret Data

Project Name: TpPv

Rev: 1.0

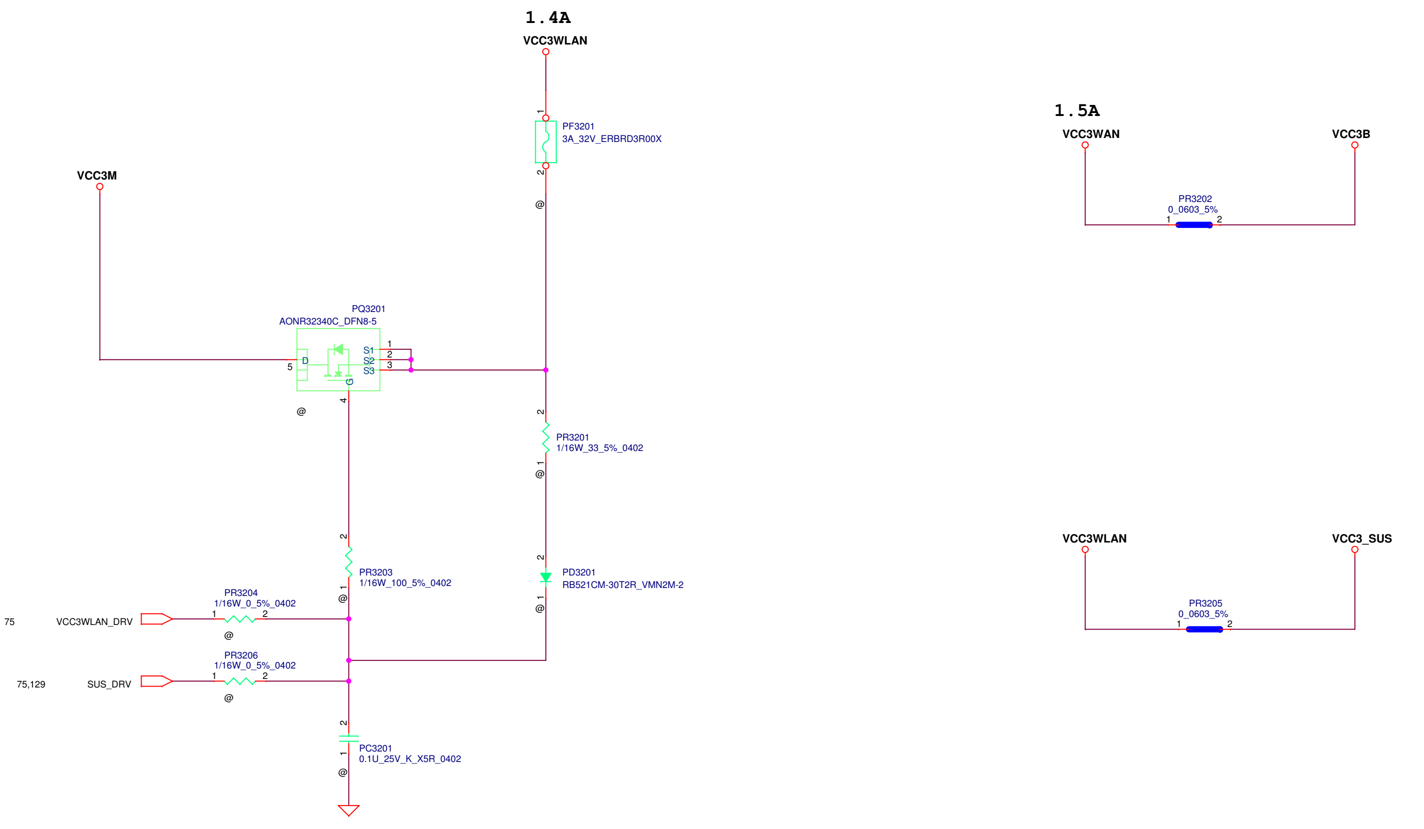
Title: **LOAD SW LAN**

Date: Friday, May 15, 2020






| Project Name | TpPv |
|---|---|
| Rev 1.0 | Title: LOAD SW B |
| Date: Friday, May 15, 2020 | Sheet 131 of 133 |




LC Future Center Secret Data

LCFC

Project Name: TpPv

Rev: 1.0

Title: LOAD SW WWAN&WLAN

Date: Friday, May 15, 2020

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N19M@
0_0402_5%