COMPAL CONFIDENTIAL

MODEL NAME : AAPA0

PCB NO : LA-C541P

BOM P/N : 4319X031L01

GPIO MAP: Gen7 GPIO Master_0612

MIRAMAR 15"

Skylake H-type (2 chip)

REV : 1.0(A00)

2015.08.17

@,@EMC@ : Nopop Component

EMC@ : EMI/ESD/RF part

AAC@ : pop AAC config

XDP@ : Total debug Component (pop them until ST)

CONN@ : Connector Component

@AAC@ : Nopop AAC config(control by EC)

Layout Dell logo

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REV: X00
PWB: XXXXX
DATE: 1448-02

PCB 1DI LA-C541P REV0 M/B

Part Number	Description
DAA000A2010	PCB 1DI LA-C541P REV1 M/B

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Power CKT: 0108

Compal Electronics, Inc.		
Title: Cover Sheet		
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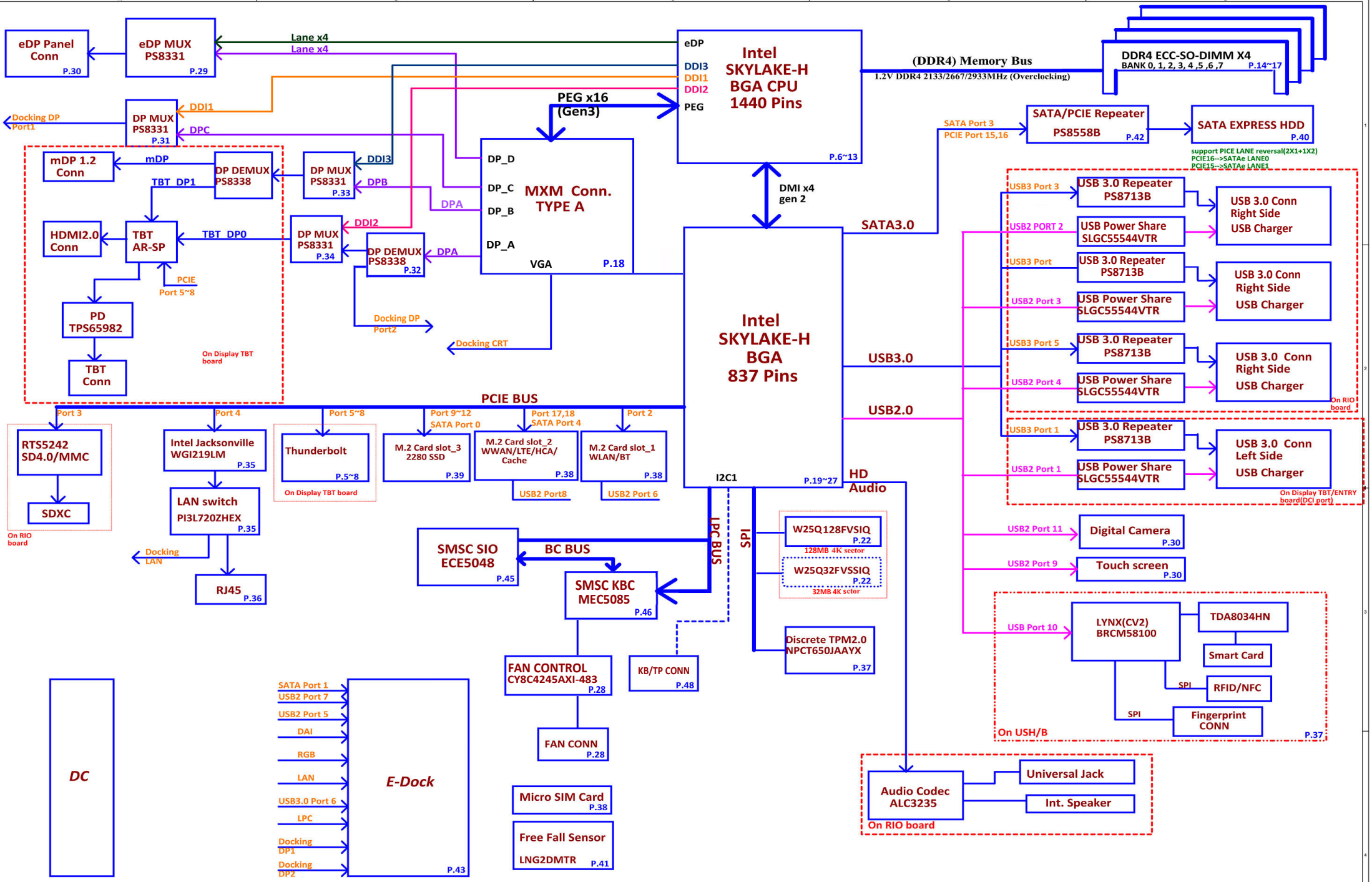

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Title	Block Diagram	
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +3.3V_MXM +5V_MXM +MXM_PWR_SRC	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_EDRAM +VCC_EOPIO +VCC_GTU +VCC_GT +1.0V_VCCSTG +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top		Copper foil	0.5oz
		3.7	Prepreg	1080
2	GND/PWR		Copper foil	1oz
		3.7	Core	4mil
3	Sig 1		Copper foil	1oz
		4.1	Prepreg	2116Mx2
4	GND/PWR		Copper foil	1oz
		3.7	Core	4mil
5	Sig 2		Copper foil	1oz
		3.8	Prepreg	1080Hx2
6	Sig 3		Copper foil	1oz
		3.7	Core	4mil
7	GND/PWR		Copper foil	1oz
		4.1	Prepreg	2116Mx2
8	Sig 4		Copper foil	1oz
		3.7	Core	4mil
9	GND/PWR		Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	
Overall Thickness (1.45mm ± 10%)			57.09	

Vinafix

SATA	DESTINATION
SATA 0	SSD 2280
SATA 1	Dock ESATA
SATA 2	NA
SATA 3	SATAe HDD
SATA 4	M.2 Slot-2(cache)
SATA 5	NA

USB3.0	DESTINATION
Port 1	Left Side JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE/HCA)
Port 3	Right Side JUSB1
Port 4	Right Side JUSB2
Port 5	Right Side JUSB3
Port 6	Docking

	USB PORT#	DESTINATION
PCH	1	Left Side JUSB1
	2	Right Side JUSB1
	3	Right Side JUSB2
	4	Right Side JUSB3
	5	Docking USB3.0
	6	M.2 Slot-1 (BT)
	7	Docking USB 2.0
	8	M.2 Slot-2 (WWAN/LTE/HCA)
	9	Touch Screen
	10	LYNX(CV2)
	11	Camera
	12	NA
	13	NA
	14	NA

LYNX(CV2)	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	M.2 Slot-1 (WLAN)
Lane 3	MMI(Card reader)
Lane 4	10/100/1G LOM
Lane 5~8	TBT-Alpine Ridge
Lane 9~12	M.2 Slot-3 (SSD 2280)
Lane 13~14	(Dock ESATA),NA(LANE reservsal)
Lane 15~16	SATA-Express HDD(LANE reservsal)
Lane 17~18	M.2 Slot-2 (WWAN/LTE/HCA)

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Title: Index and Config.

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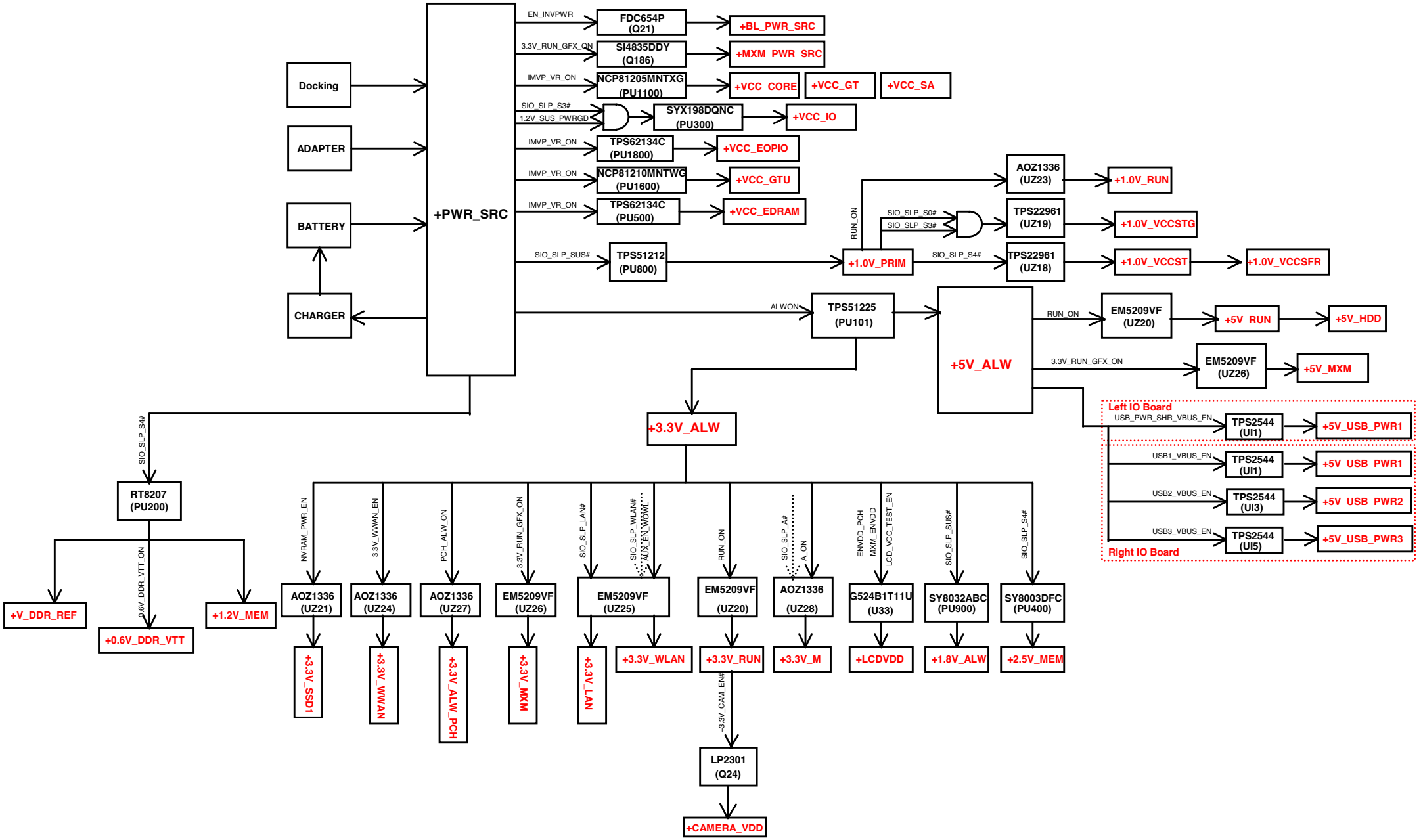

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Title	Power Rail
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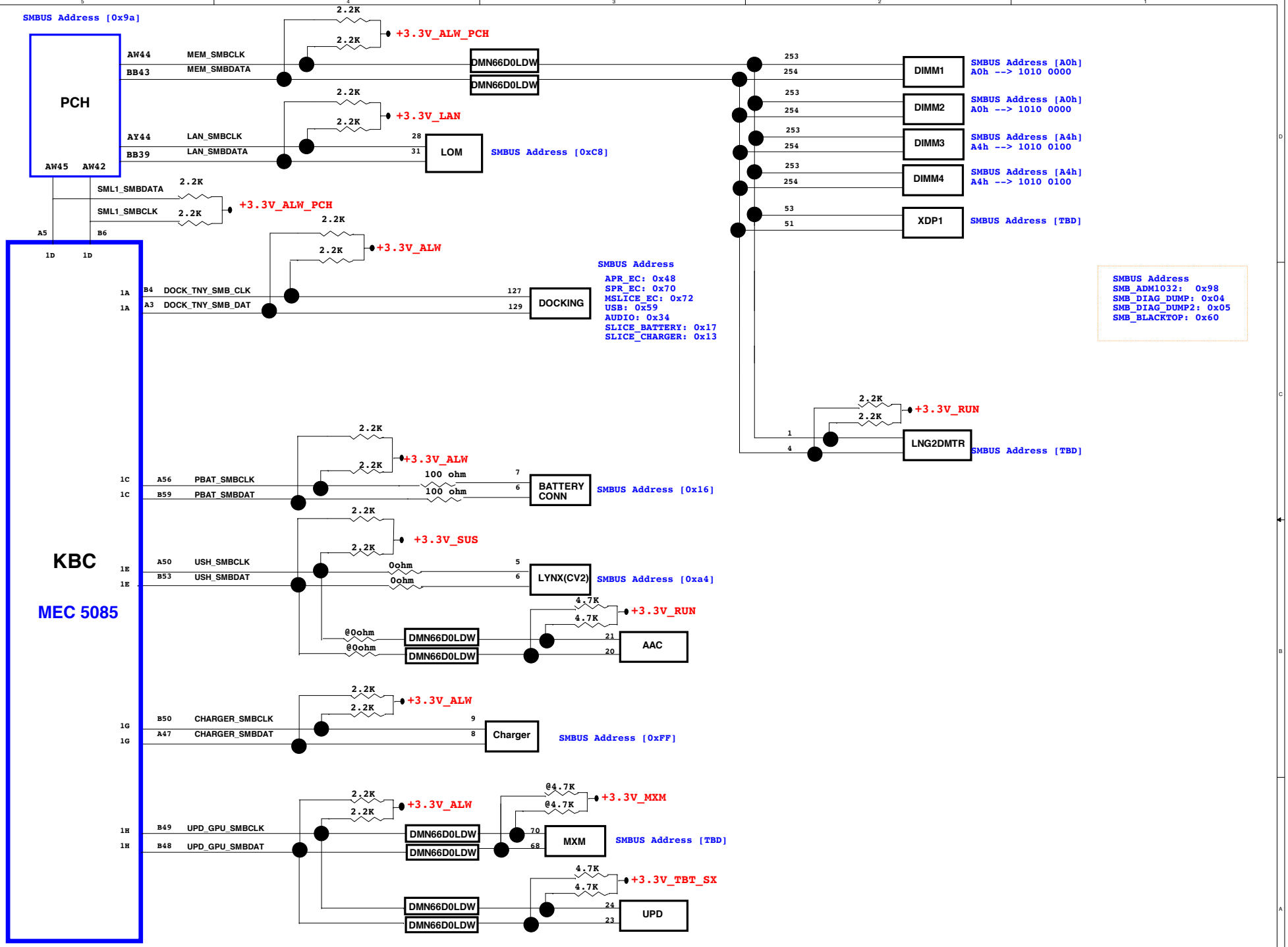

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Title: SMBUS Bolck Diagram

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PEG_CRX_C_GTX_P[0..15] PEG_CRX_C_GTX_P[0..15] <18>
PEG_CRX_C_GTX_N[0..15] PEG_CRX_C_GTX_N[0..15] <18>
PEG_CTX_C_GRX_P[0..15] PEG_CTX_C_GRX_P[0..15] <18>
PEG_CTX_C_GRX_N[0..15] PEG_CTX_C_GRX_N[0..15] <18>

CPU1C SKYLAKE_HALO
BGA1440

PEG_CRX_C_GTX_P15	CC32	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P15	E25	PEG_RXP[0]	PEG_TXP[0]	B25	PEG_CTX_GRX_P15	CC64	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P15
PEG_CRX_C_GTX_N15	CC16	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N15	D25	PEG_RXN[0]	PEG_TXN[0]	A25	PEG_CTX_GRX_N15	CC50	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N15
PEG_CRX_C_GTX_P14	CC31	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P14	E24	PEG_RXP[1]	PEG_TXP[1]	B24	PEG_CTX_GRX_P14	CC63	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P14
PEG_CRX_C_GTX_N14	CC15	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N14	F24	PEG_RXN[1]	PEG_TXN[1]	C24	PEG_CTX_GRX_N14	CC77	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N14
PEG_CRX_C_GTX_P13	CC30	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P13	E23	PEG_RXP[2]	PEG_TXP[2]	B23	PEG_CTX_GRX_P13	CC72	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P13
PEG_CRX_C_GTX_N13	CC14	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N13	D23	PEG_RXN[2]	PEG_TXN[2]	A23	PEG_CTX_GRX_N13	CC62	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N13
PEG_CRX_C_GTX_P12	CC29	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P12	E22	PEG_RXP[3]	PEG_TXP[3]	B22	PEG_CTX_GRX_P12	CC61	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P12
PEG_CRX_C_GTX_N12	CC13	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N12	F22	PEG_RXN[3]	PEG_TXN[3]	C22	PEG_CTX_GRX_N12	CC49	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N12
PEG_CRX_C_GTX_P11	CC28	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P11	E21	PEG_RXP[4]	PEG_TXP[4]	B21	PEG_CTX_GRX_P11	CC60	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P11
PEG_CRX_C_GTX_N11	CC12	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N11	D21	PEG_RXN[4]	PEG_TXN[4]	A21	PEG_CTX_GRX_N11	CC76	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N11
PEG_CRX_C_GTX_P10	CC27	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P10	E20	PEG_RXP[5]	PEG_TXP[5]	B20	PEG_CTX_GRX_P10	CC71	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P10
PEG_CRX_C_GTX_N10	CC11	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N10	F20	PEG_RXN[5]	PEG_TXN[5]	C20	PEG_CTX_GRX_N10	CC59	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N10
PEG_CRX_C_GTX_P9	CC26	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P9	E19	PEG_RXP[6]	PEG_TXP[6]	B19	PEG_CTX_GRX_P9	CC58	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P9
PEG_CRX_C_GTX_N9	CC10	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N9	D19	PEG_RXN[6]	PEG_TXN[6]	A19	PEG_CTX_GRX_N9	CC48	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N9
PEG_CRX_C_GTX_P8	CC25	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P8	E18	PEG_RXP[7]	PEG_TXP[7]	B18	PEG_CTX_GRX_P8	CC57	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P8
PEG_CRX_C_GTX_N8	CC9	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N8	F18	PEG_RXN[7]	PEG_TXN[7]	C18	PEG_CTX_GRX_N8	CC75	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N8
PEG_CRX_C_GTX_P7	CC24	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P7	D17	PEG_RXP[8]	PEG_TXP[8]	A17	PEG_CTX_GRX_P7	CC70	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P7
PEG_CRX_C_GTX_N7	CC8	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N7	E17	PEG_RXN[8]	PEG_TXN[8]	B17	PEG_CTX_GRX_N7	CC56	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N7
PEG_CRX_C_GTX_P6	CC23	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P6	F16	PEG_RXP[9]	PEG_TXP[9]	C16	PEG_CTX_GRX_P6	CC55	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P6
PEG_CRX_C_GTX_N6	CC7	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N6	E16	PEG_RXN[9]	PEG_TXN[9]	B16	PEG_CTX_GRX_N6	CC47	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N6
PEG_CRX_C_GTX_P5	CC22	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P5	D15	PEG_RXP[10]	PEG_TXP[10]	A15	PEG_CTX_GRX_P5	CC54	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P5
PEG_CRX_C_GTX_N5	CC6	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N5	E15	PEG_RXN[10]	PEG_TXN[10]	B15	PEG_CTX_GRX_N5	CC74	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N5
PEG_CRX_C_GTX_P4	CC21	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P4	F14	PEG_RXP[11]	PEG_TXP[11]	C14	PEG_CTX_GRX_P4	CC69	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P4
PEG_CRX_C_GTX_N4	CC5	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N4	E14	PEG_RXN[11]	PEG_TXN[11]	B14	PEG_CTX_GRX_N4	CC46	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N4
PEG_CRX_C_GTX_P3	CC20	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P3	D13	PEG_RXP[12]	PEG_TXP[12]	A13	PEG_CTX_GRX_P3	CC52	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P3
PEG_CRX_C_GTX_N3	CC4	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N3	E13	PEG_RXN[12]	PEG_TXN[12]	B13	PEG_CTX_GRX_N3	CC73	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N3
PEG_CRX_C_GTX_P2	CC19	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P2	F12	PEG_RXP[13]	PEG_TXP[13]	C12	PEG_CTX_GRX_P2	CC51	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P2
PEG_CRX_C_GTX_N2	CC3	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N2	E12	PEG_RXN[13]	PEG_TXN[13]	B12	PEG_CTX_GRX_N2	CC53	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N2
PEG_CRX_C_GTX_P1	CC18	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P1	D11	PEG_RXP[14]	PEG_TXP[14]	A11	PEG_CTX_GRX_P1	CC68	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P1
PEG_CRX_C_GTX_N1	CC2	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N1	E11	PEG_RXN[14]	PEG_TXN[14]	B11	PEG_CTX_GRX_N1	CC45	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N1
PEG_CRX_C_GTX_P0	CC17	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_P0	F10	PEG_RXP[15]	PEG_TXP[15]	C10	PEG_CTX_GRX_P0	CC67	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_P0
PEG_CRX_C_GTX_N0	CC1	2	1	0.22U_0402_10V6K	PEG_CRX_GTX_N0	E10	PEG_RXN[15]	PEG_TXN[15]	B10	PEG_CTX_GRX_N0	CC44	2	1	0.22U_0402_10V6K	PEG_CTX_C_GRX_N0

PEG_COMP G2
PEG_RCOMP

+VCC_IO
PEG_COMP 2 1 RC2
24.9_0402_1%

CAD Note:
Trace width=12 mils
,Spacing=15mil
Max length= 400 mils.

<20> DMI_CRX_PTX_P0	DMI_CRX_PTX_P0	D8	DMI_RXP[0]	DMI_TXP[0]	B8	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0 <20>
<20> DMI_CRX_PTX_N0	DMI_CRX_PTX_N0	E8	DMI_RXN[0]	DMI_TXN[0]	A8	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0 <20>
<20> DMI_CRX_PTX_P1	DMI_CRX_PTX_P1	E6	DMI_RXP[1]	DMI_TXP[1]	C6	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1 <20>
<20> DMI_CRX_PTX_N1	DMI_CRX_PTX_N1	F6	DMI_RXN[1]	DMI_TXN[1]	B6	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1 <20>
<20> DMI_CRX_PTX_P2	DMI_CRX_PTX_P2	D5	DMI_RXP[2]	DMI_TXP[2]	B5	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2 <20>
<20> DMI_CRX_PTX_N2	DMI_CRX_PTX_N2	E5	DMI_RXN[2]	DMI_TXN[2]	A5	DMI_CTX_PRX_N2	DMI_CTX_PRX_N2 <20>
<20> DMI_CRX_PTX_P3	DMI_CRX_PTX_P3	J8	DMI_RXP[3]	DMI_TXP[3]	D4	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3 <20>
<20> DMI_CRX_PTX_N3	DMI_CRX_PTX_N3	J9	DMI_RXN[3]	DMI_TXN[3]	B4	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3 <20>

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SKL-H_BGA1440

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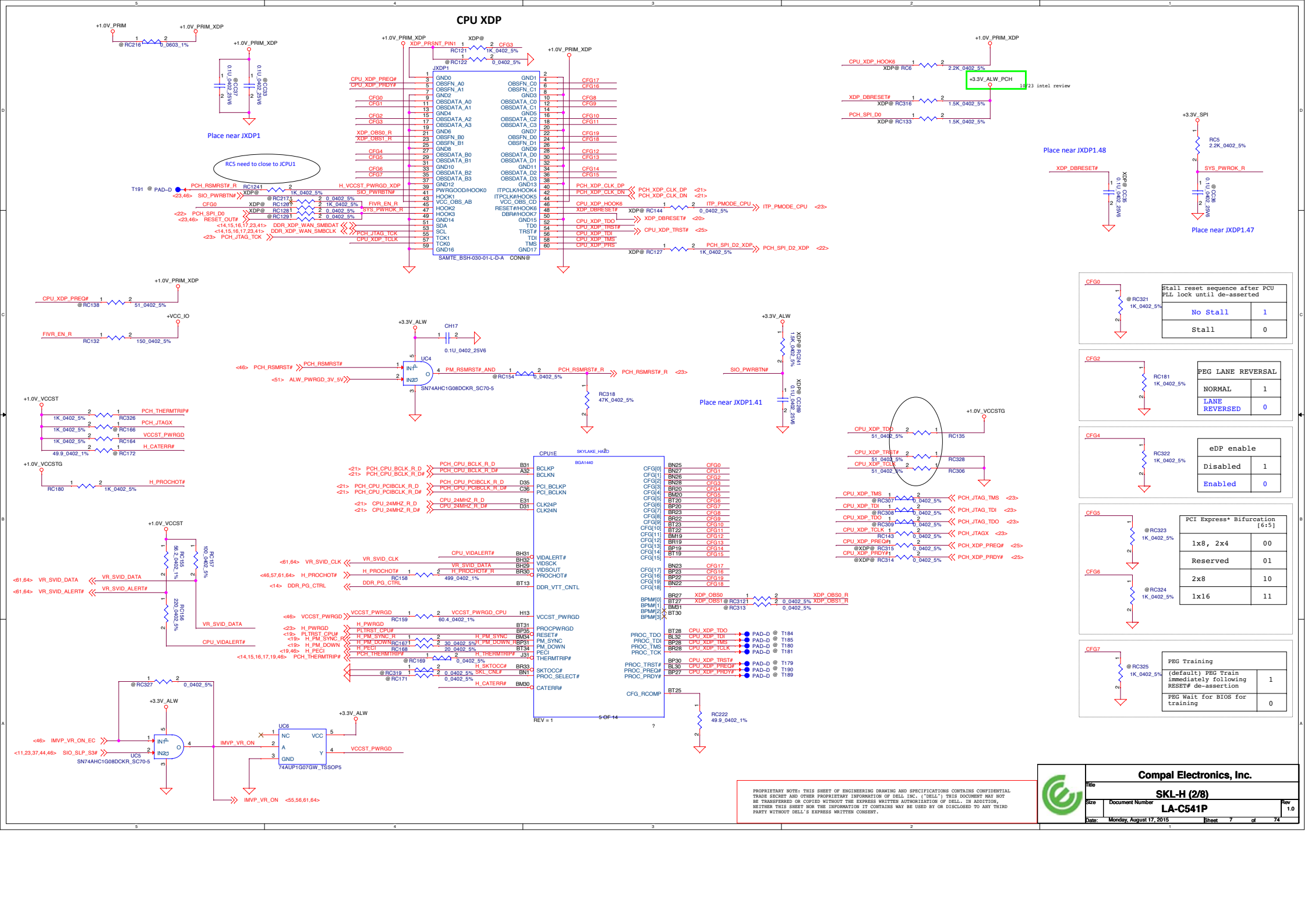
CPU XDP



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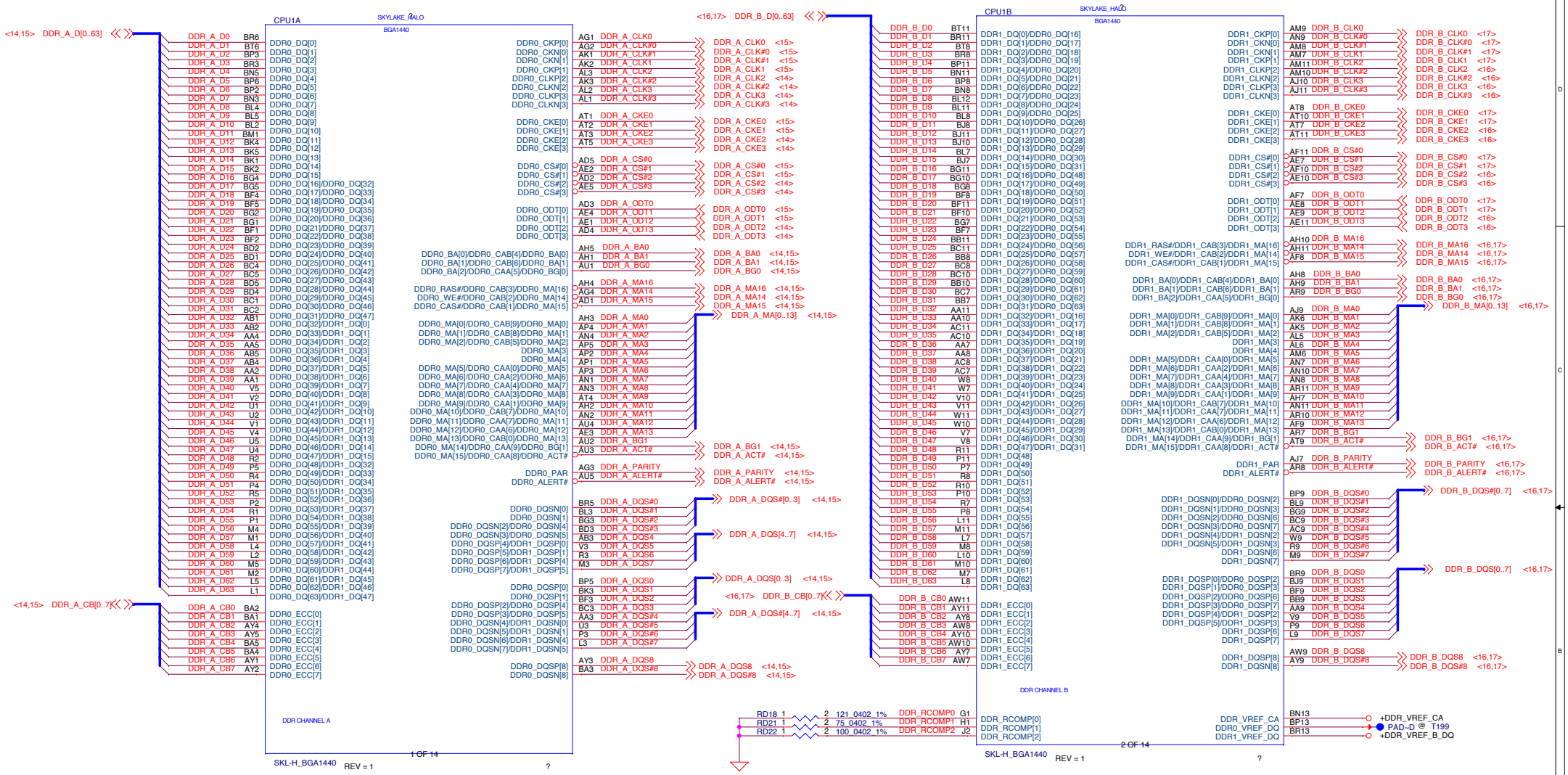

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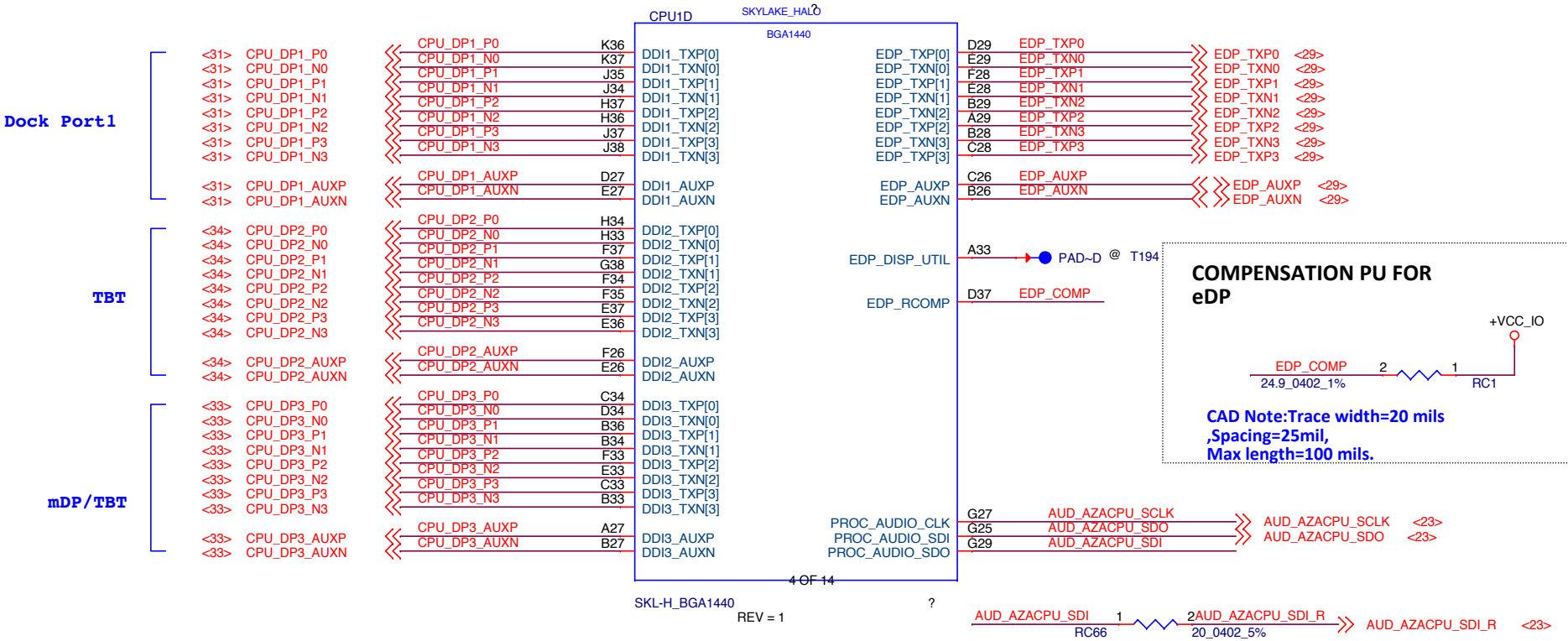
Title: SKL-H (3/8)

Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 8 of 74



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Title: SKL-H (4/8)

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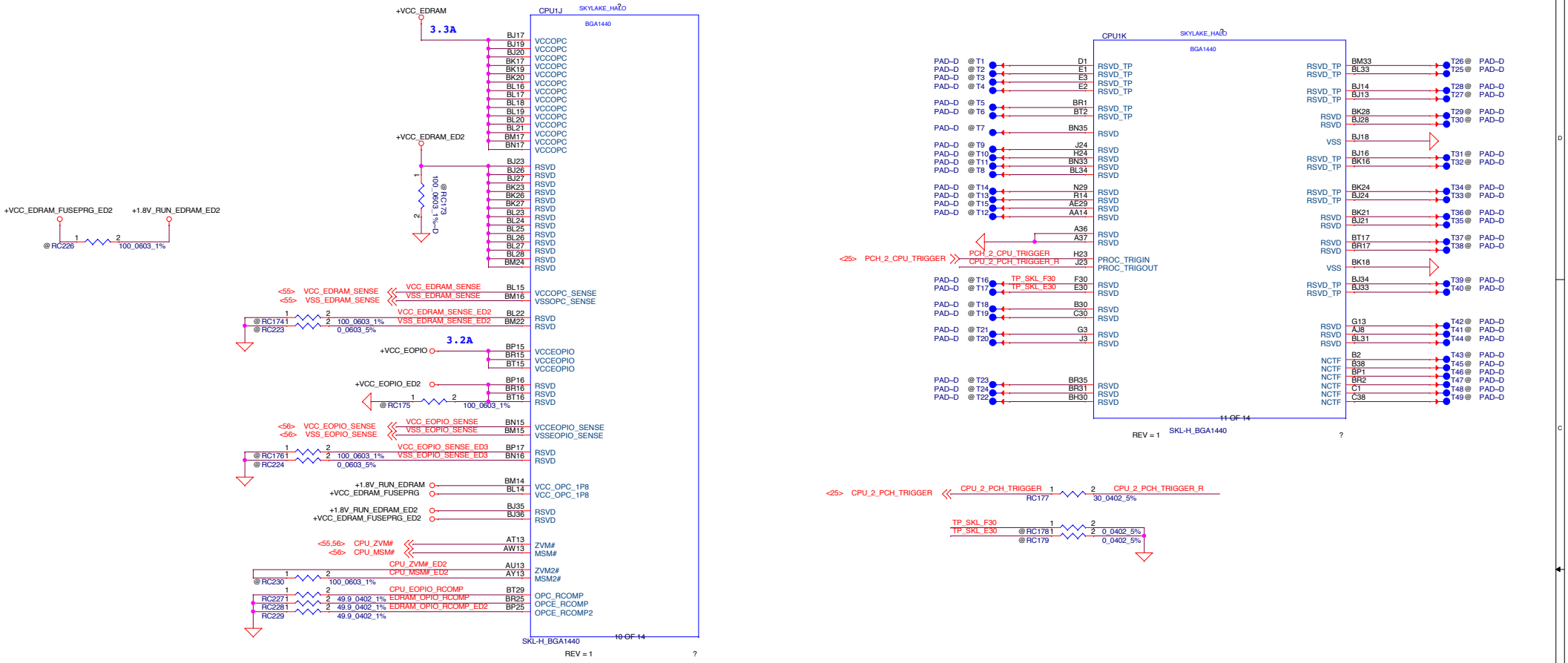

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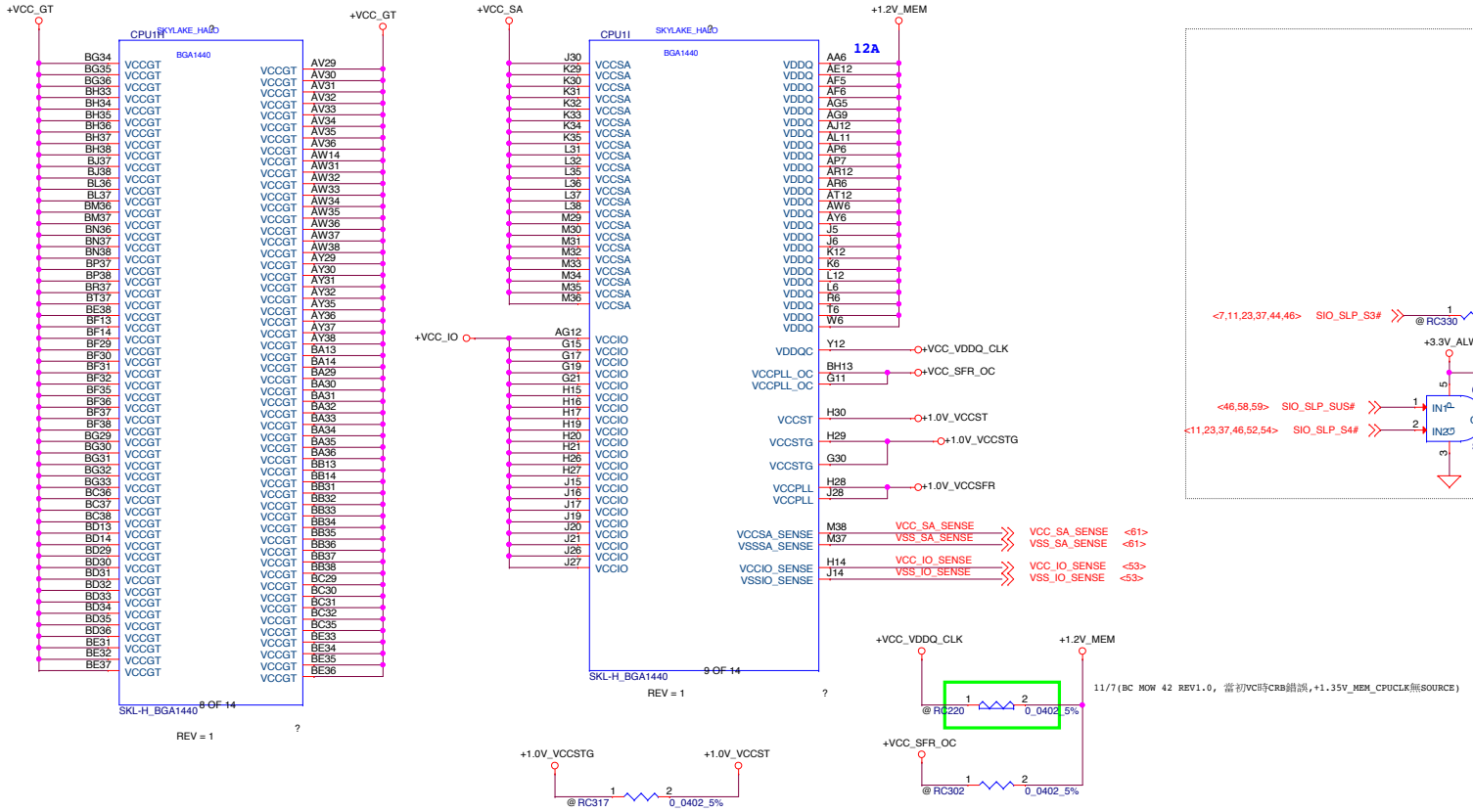
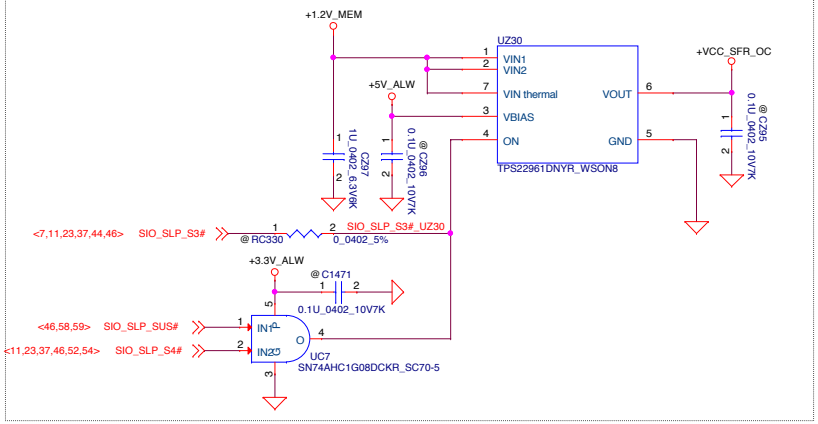
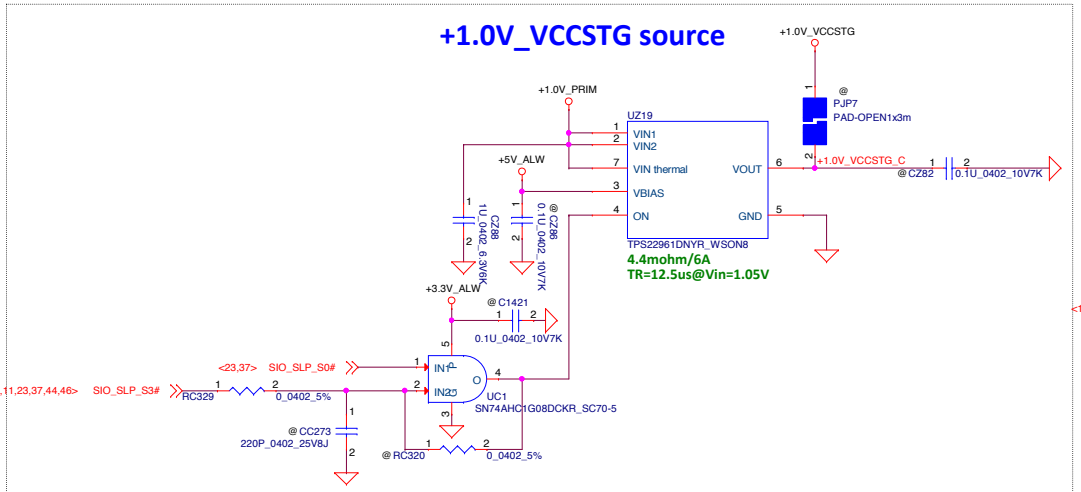
Size	Document Number: LA-C541P	Rev: 1.0
Date: Monday, August 17, 2015	Sheet 10 of 74	



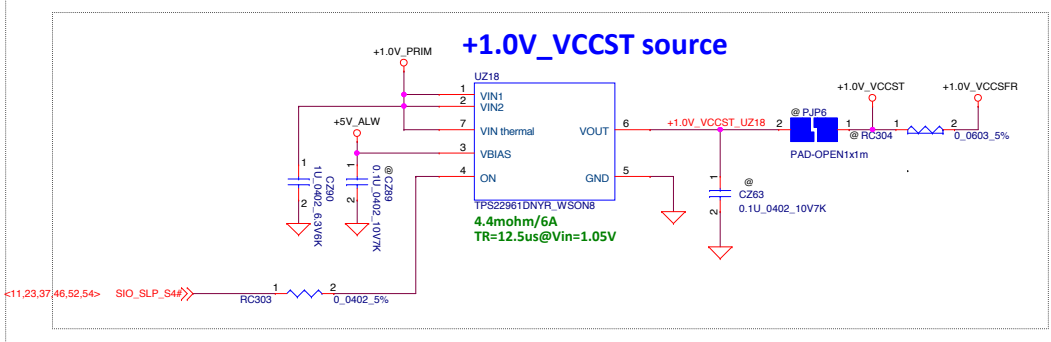
+VCC_SFR_OC source



+1.0V_VCCSTG source



+1.0V_VCCST source



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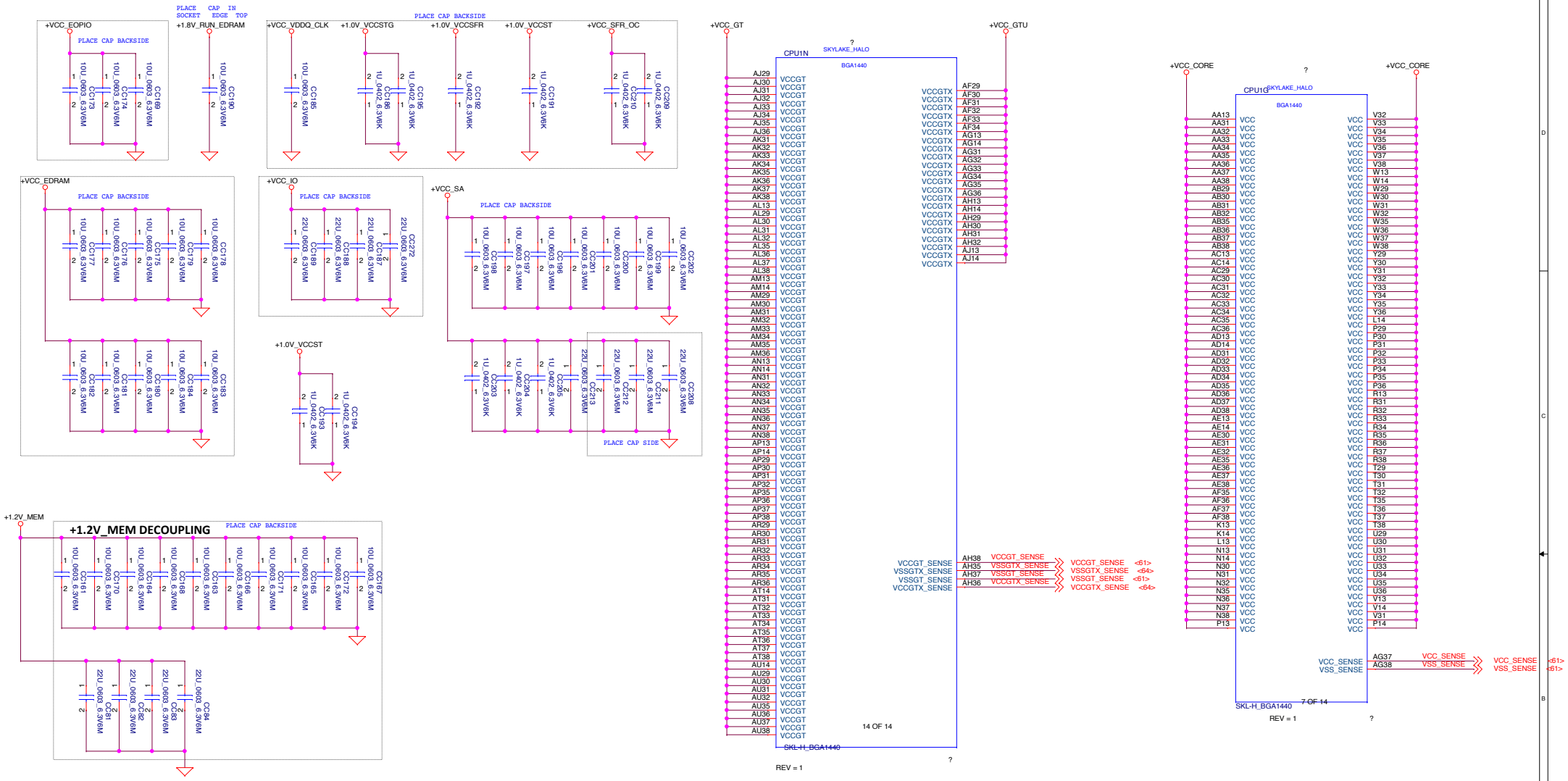
Title	SKL-H (6/8)	
Size	Document Number: LA-C541P	Rev: 1.0
Date: Monday, August 17, 2015	Sheet 11 of 74	



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Title: SKL-H (7/8)		
Size	Document Number: LA-C541P	Rev: 1.0
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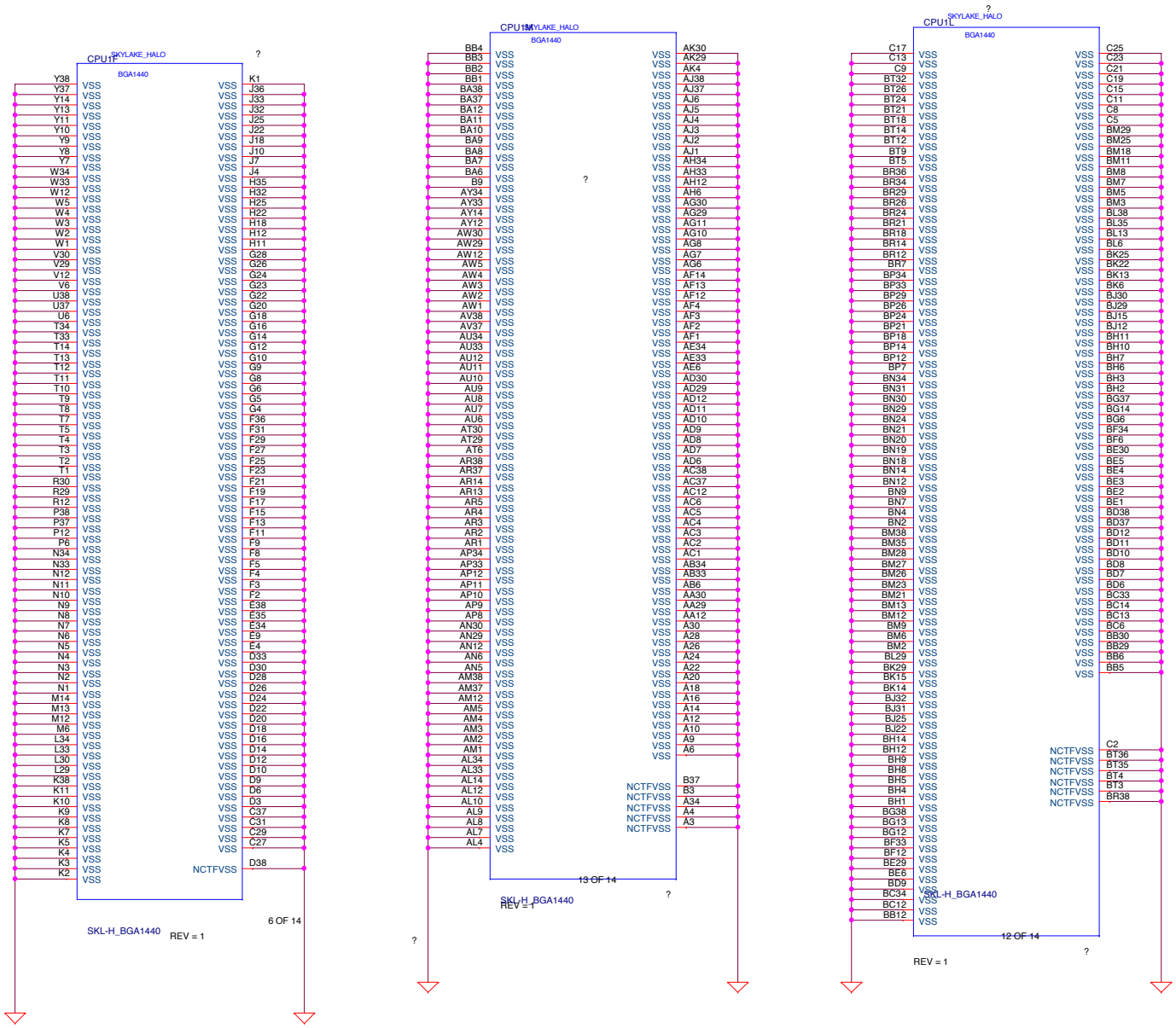

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Title: SKL-H (8/8)		
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JDIMM1 STD Type H=9.2

All VREF traces should have 10 mil trace width

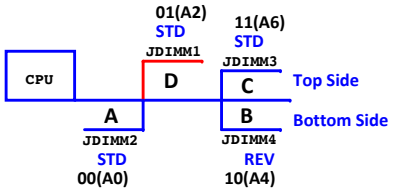
Populate RD1, De-Populate RD2 for Intel DDR3 VREFDQ multiple methods M1
Populate RD2, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

CD14 change to SGA20331E10

Layout Note: Place near JDIMM1.258

DIMM Select

	SA0	SA1	SA2
* DIMM1	1	0	0
DIMM2	0	0	0
DIMM3	1	1	0
DIMM4	0	1	0



CONN LIST1020

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Compal Electronics, Inc.

Title: DDR4-SODIMM SLOT1

Size: | Document Number: LA-C541P | Rev: 1.0

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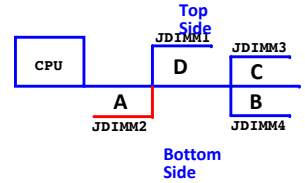
JDIMM2 STD Type H=4



CD14 change to SGA20331E10

Layout Note:
Place near JDIMM2.258

DIMM Select

	SA0	SA1	SA2
DIMM1	1	0	0
* DIMM2	0	0	0
DIMM3	1	1	0
DIMM4	0	1	0

CONN LIST1124

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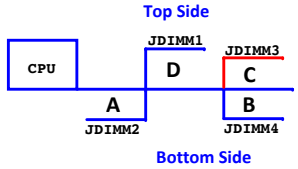
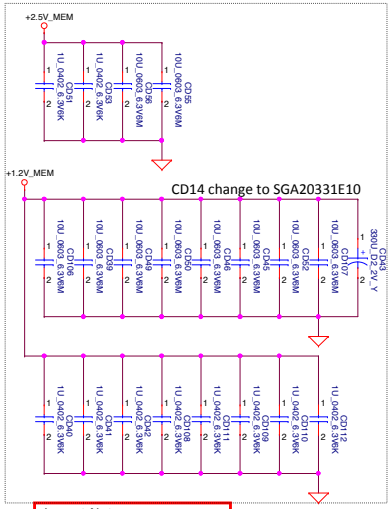
Title: DDR4-SODIMM SLOT2

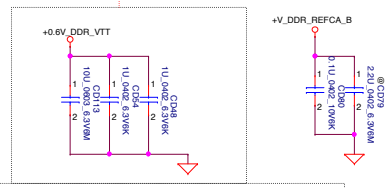
Size: | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 15 of 74

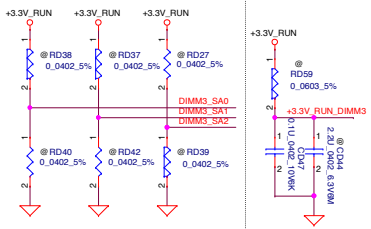
JDIMM3 STD Type H=5.2



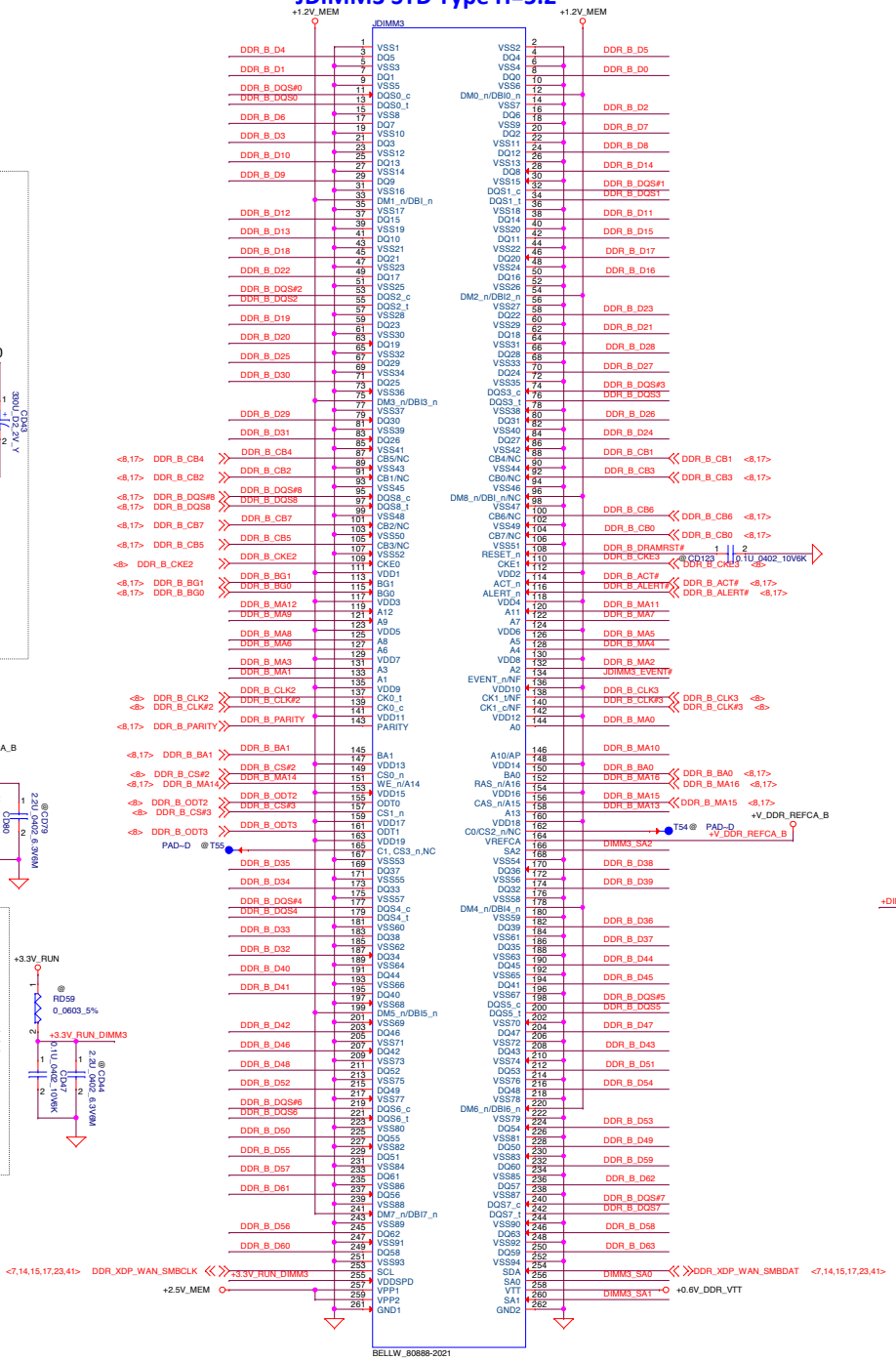




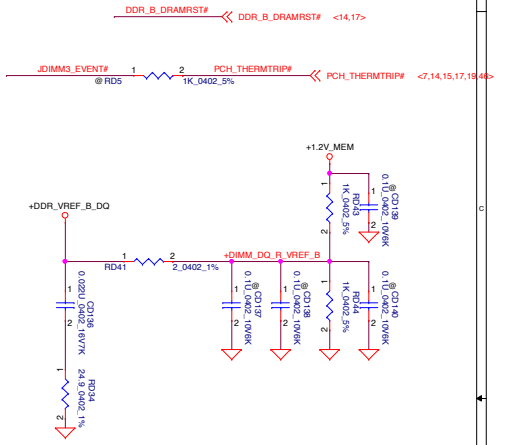
DIMM Select

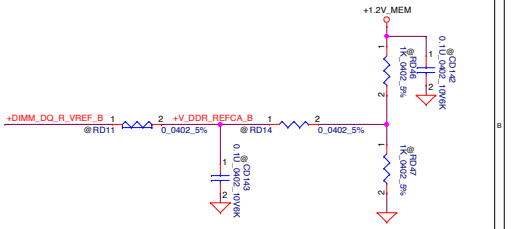


	SA0	SA1	SA2
DIMM1	1	0	0
DIMM2	0	0	0
* DIMM3	1	1	0
DIMM4	0	1	0



CONN LIST1020





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Title	DDR4-SODIMM SLOT3	
Size	Document Number: LA-C541P	Rev: 1.0
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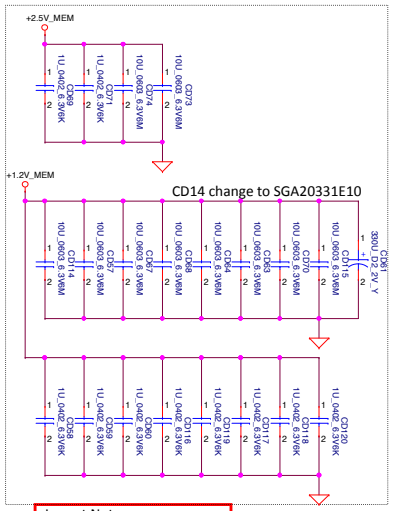
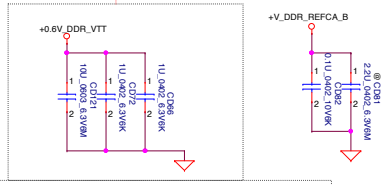
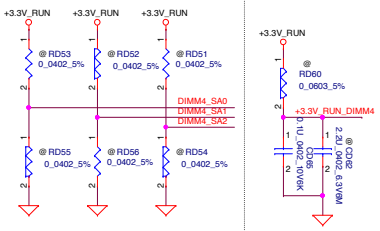
JDIMM4 REV Type H=4

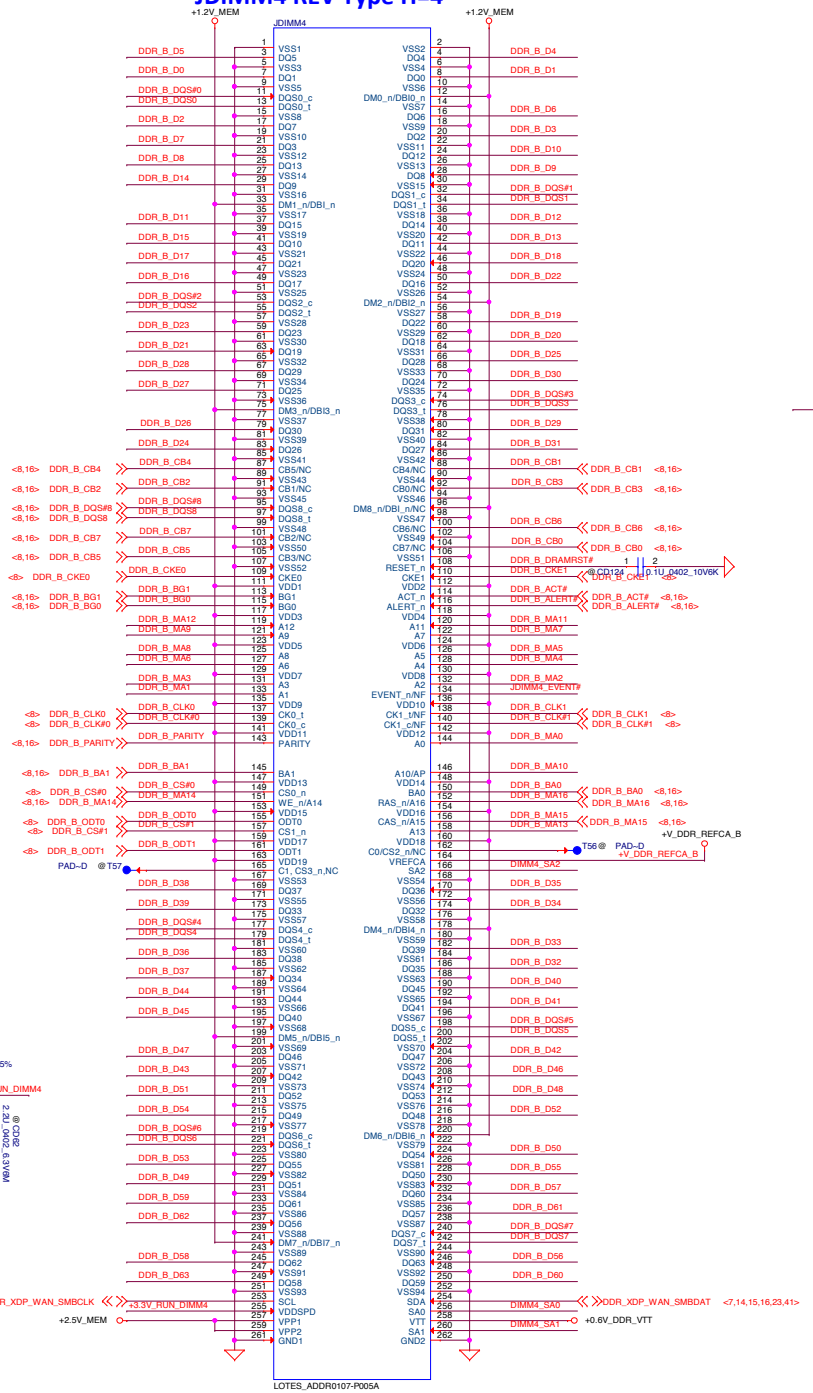


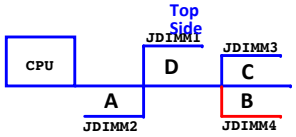


DIMM Select

	SA0	SA1	SA2
DIMM1	1	0	0
DIMM2	0	0	0
DIMM3	1	1	0
* DIMM4	0	1	0







CONN LIST1124

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Title: DDR4-SODIMM SLOT4

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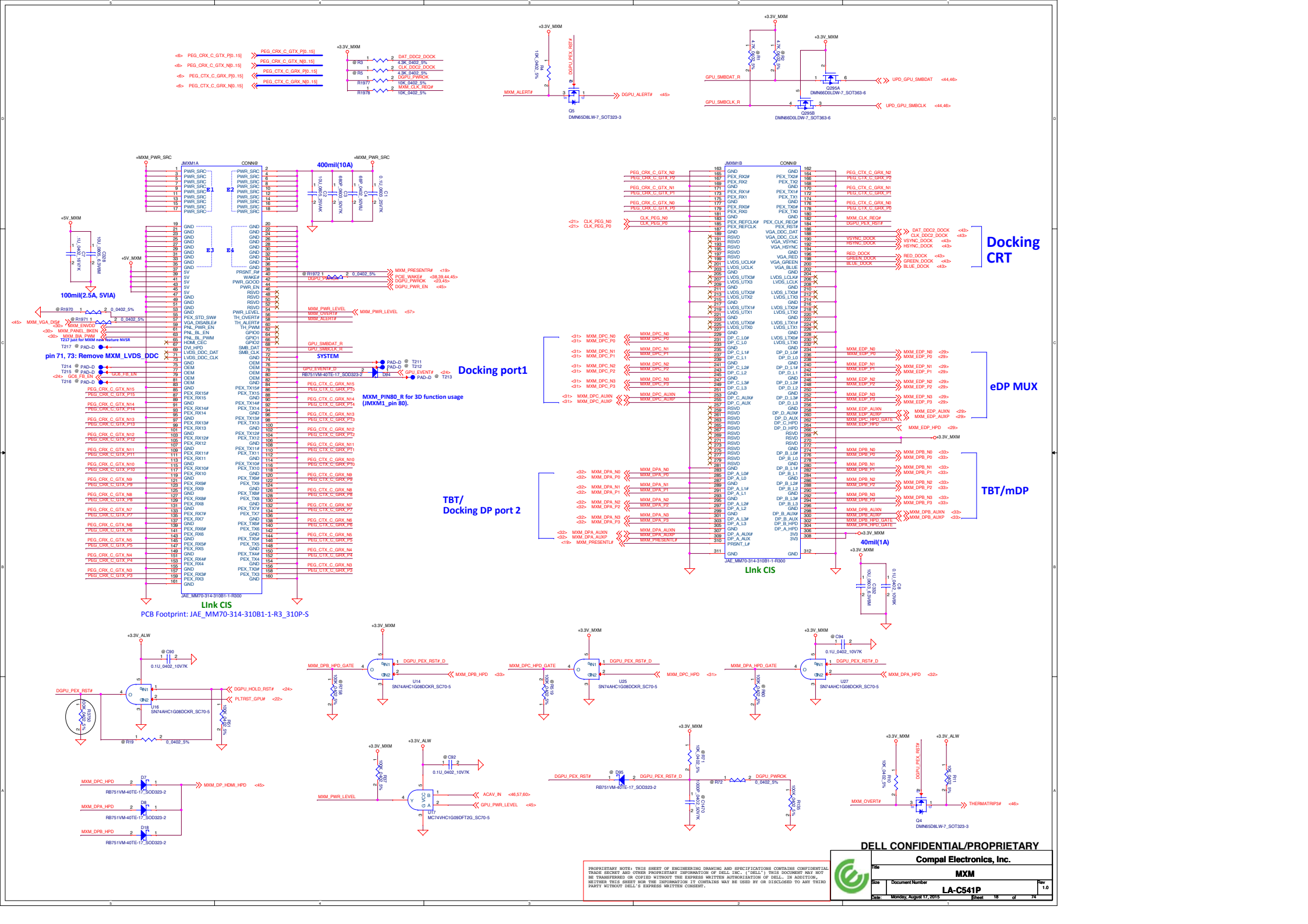
Date: Monday, August 17, 2015 | Sheet 17 of 74


Docking CRT
eDP MUX
TBT/mDP
Docking port1
TBT/
Docking DP port 2
100mil(2.5A, 5VIA)
400mil(10A)
40mil(1A)
pin 71, 73: Remove MXM_LVDS_DDC
MXM_PIN80_R for 3D function usage (JMXM1_pin 80).
LInk CIS
PCB Footprint: JAE_MM70-314-310B1-1-R3_310P-S
JMXM1A
JMXM1B
CONN@
JAE_MM70-314-310B1-1-R300
SYSTEM
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Compal Electronics, Inc.
MXM
LA-C541P
Monday, August 17, 2015
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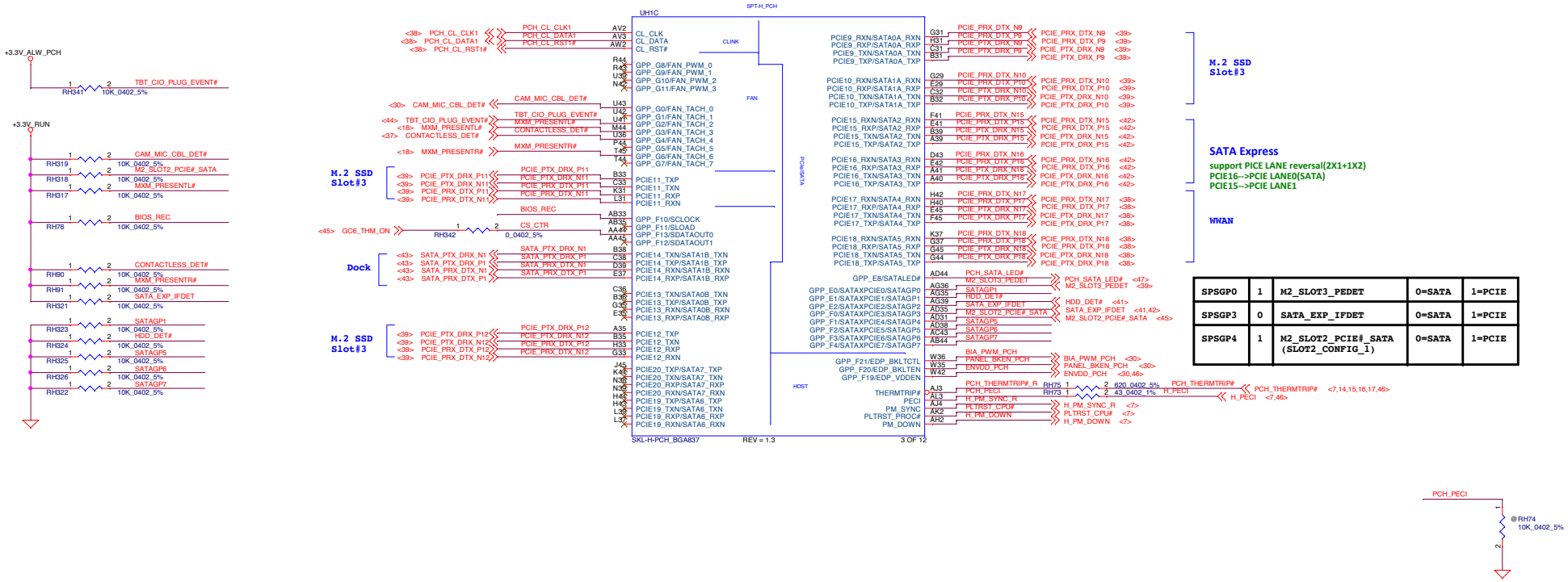

SPSGP0	1	M2_SLOT3_PEDET	0=SATA	1=PCIE
SPSGP3	0	SATA_EXP_IFDET	0=SATA	1=PCIE
SPSGP4	1	M2_SLOT2_PCIE#_SATA (SLOT2_CONFIG_1)	0=SATA	1=PCIE

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Title: SKYLAKE PCH-H (1/9)

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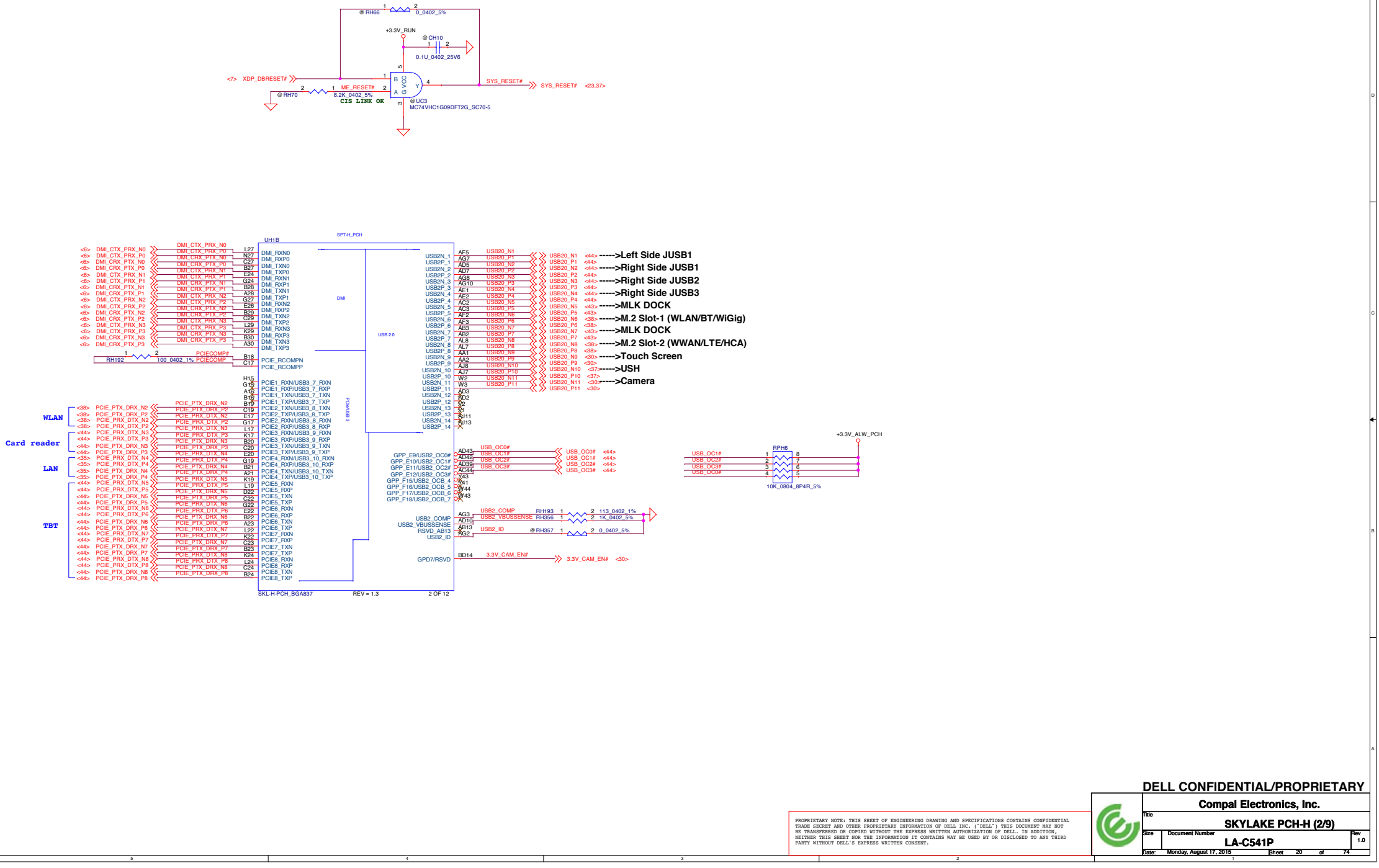

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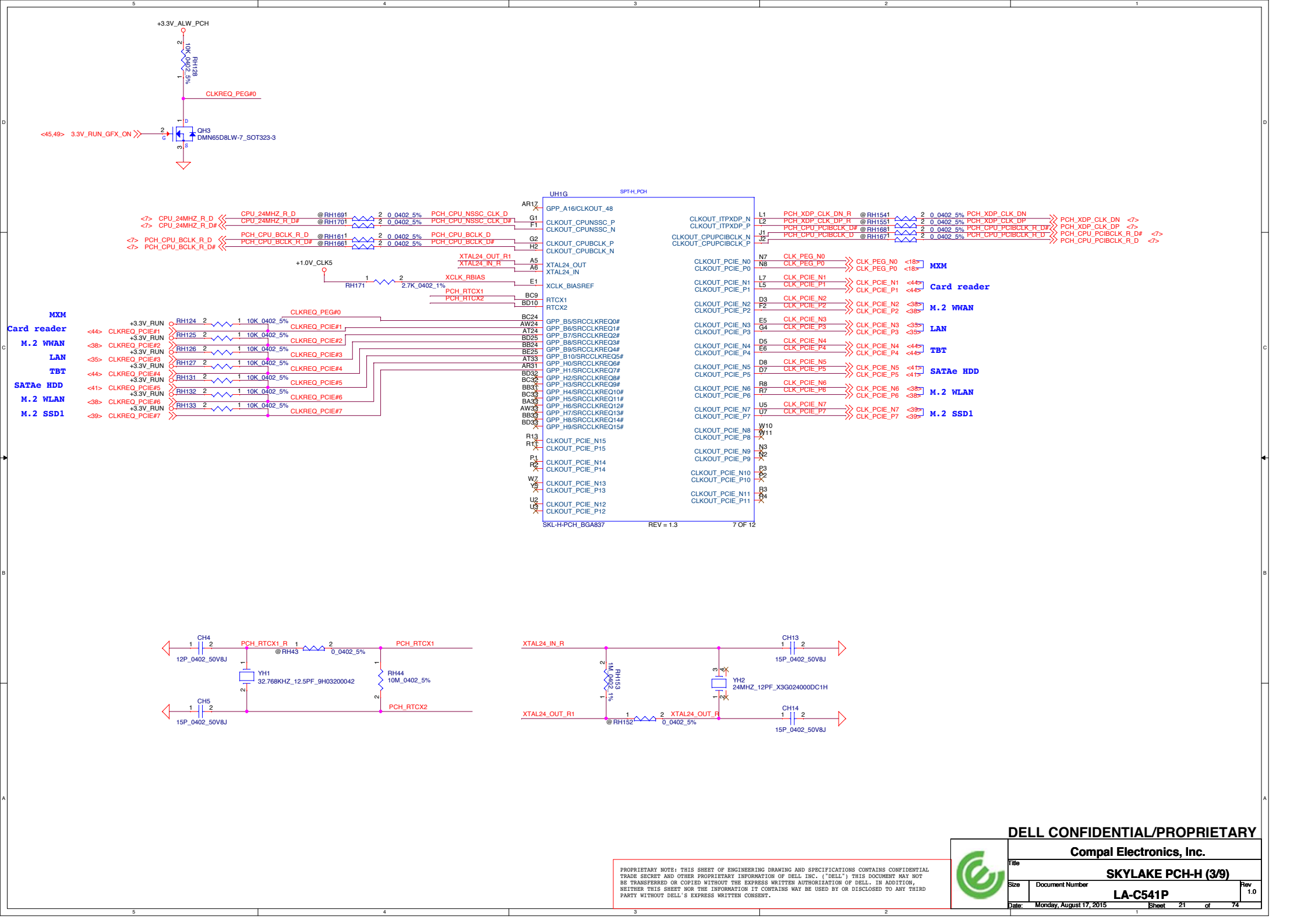
Title: SKYLAKE PCH-H (2/9)

Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 20 of 74


+3.3V_ALW_PCH
10K_0402_5%
RH128
CLKREQ_PEG#0
<45,49> 3.3V_RUN_GFX_ON
QH3
DMN65D8LW-7_SOT323-3
UH1G
SPT-H_PCH
GPP_A16/CLKOUT_48
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
XTAL24_OUT
XTAL24_IN
XCLK_BIASREF
RTCX1
RTCX2
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
SKL-H-PCH_BGA837
REV = 1.3
7 OF 12
MXM
Card reader
M.2 WWAN
LAN
TBT
SATAe HDD
M.2 WLAN
M.2 SSD1
CH4
12P_0402_50V8J
YH1
32.768KHZ_12.5PF_9H03200042
RH44
10M_0402_5%
CH5
15P_0402_50V8J
RH153
1M_0402_1%
YH2
24MHZ_12PF_X3G024000DC1H
CH13
CH14
15P_0402_50V8J
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SKYLAKE PCH-H (3/9)
Size
Document Number
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1.0
Date: Monday, August 17, 2015
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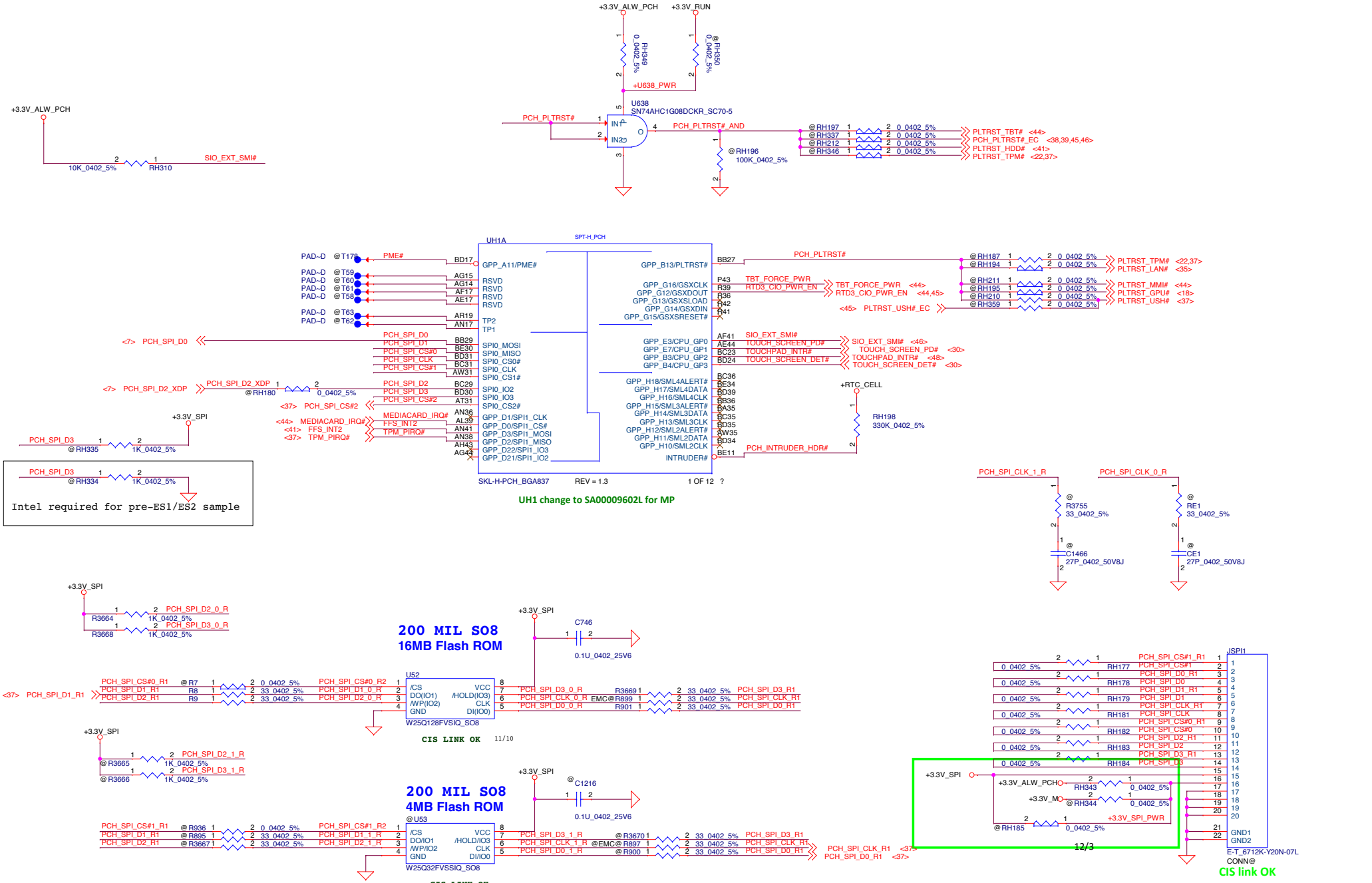

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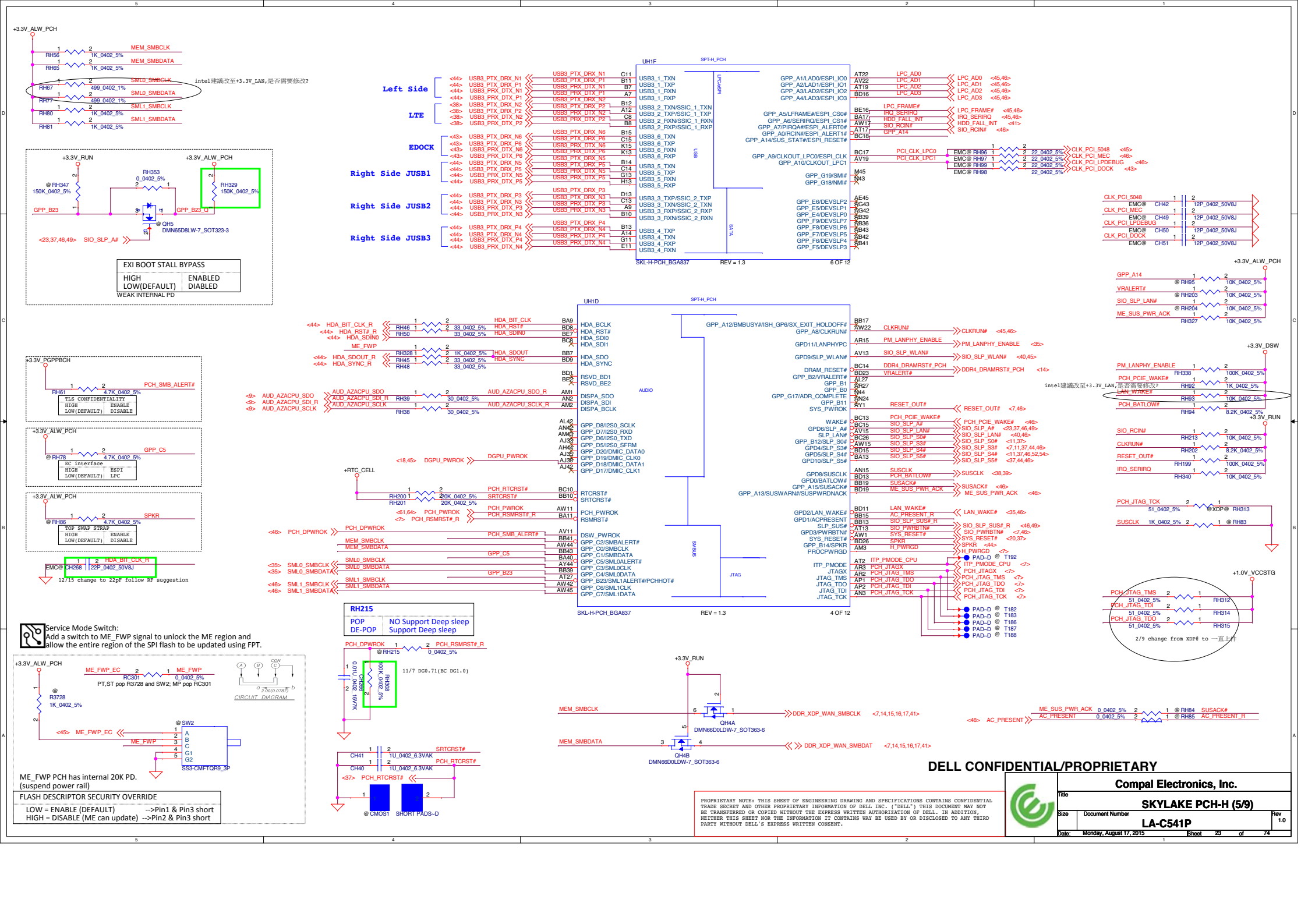
+3.3V_ALW_PCH
MEM_SMBCLK
MEM_SMBDATA
SML0_SMBCLK
SML0_SMBDATA
SML1_SMBCLK
SML1_SMBDATA
intel建議改至+3.3V_LAN,是否需要修改?
+3.3V_RUN
GPP_B23
SIO_SLP_A#
EXI BOOT STALL BYPASS
HIGH ENABLED
LOW(DEFAULT) DIABLED
WEAK INTERNAL PD
UH1F
SPT-H_PCH
Left Side
LTE
EDOCK
Right Side JUSB1
Right Side JUSB2
Right Side JUSB3
SKL-H-PCH_BGA837
REV = 1.3
6 OF 12
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
IRQ_SERIRQ
HDD_FALL_INT
SIO_RCIN#
GPP_A14
PCI_CLK_LPC0
PCI_CLK_LPC1
CLK_PCI_5048
CLK_PCI_MEC
CLK_PCI_LPDEBUG
CLK_PCI_DOCK
+3.3V_PGPPBCH
PCH_SMB_ALERT#
TLS CONFIDENTIALITY
+3.3V_ALW_PCH
GPP_C5
EC interface
+3.3V_ALW_PCH
SPKR
TOP SWAP STRAP
HDA_BIT_CLK_R
12/15 change to 22pF follow RF suggestion
UH1D
SPT-H_PCH
AUDIO
SMBUS
JTAG
SKL-H-PCH_BGA837
REV = 1.3
4 OF 12
HDA_BIT_CLK
HDA_RST#
HDA_SDI0
HDA_SDO
HDA_SYNC
AUD_AZACPU_SDO_R
AUD_AZACPU_SDI_R
AUD_AZACPU_SCLK_R
DGPU_PWROK
RTCRST#
SRTCRST#
PCH_PWROK
PCH_RSMRST#_R
DSW_PWROK
PCH_DPWROK
PCH_SMB_ALERT#
GPP_C5
GPP_B23
SML0_SMBCLK
SML0_SMBDATA
SML1_SMBCLK
SML1_SMBDATA
CLKRUN#
PM_LANPHY_ENABLE
SIO_SLP_WLAN#
DDR4_DRAMRST#_PCH
VRALERT#
RESET_OUT#
PCH_PCIE_WAKE#
SIO_SLP_A#
SIO_SLP_LAN#
SIO_SLP_S0#
SIO_SLP_S3#
SIO_SLP_S4#
SIO_SLP_S5#
SUSCLK
PCH_BATLOW#
SUSACK#
ME_SUS_PWR_ACK
LAN_WAKE#
AC_PRESENT_R
SIO_SLP_SUS#_R
SIO_PWRBTN#
SYS_RESET#
H_PWRGD
ITP_PMODE_CPU
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
+3.3V_DSW
+3.3V_RUN
+1.0V_VCCSTG
RH215
POP NO Support Deep sleep
DE-POP Support Deep sleep
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and
allow the entire region of the SPI flash to be updated using FPT.
ME_FWP_EC
ME_FWP
PT,ST pop R3728 and SW2; MP pop RC301
CIRCUIT DIAGRAM
SS3-CMFTQR9_3P
ME_FWP PCH has internal 20K PD.
(suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
QH5
DMN65D8LW-7_SOT323-3
QH4A
QH4B
DMN66D0LDW-7_SOT363-6
DDR_XDP_WAN_SMBCLK
DDR_XDP_WAN_SMBDAT
@CMOS1 SHORT PADS~D
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Compal Electronics, Inc.
Title
SKYLAKE PCH-H (5/9)
Size
Document Number
LA-C541P
Rev
1.0
Date: Monday, August 17, 2015
Sheet 23 of 74

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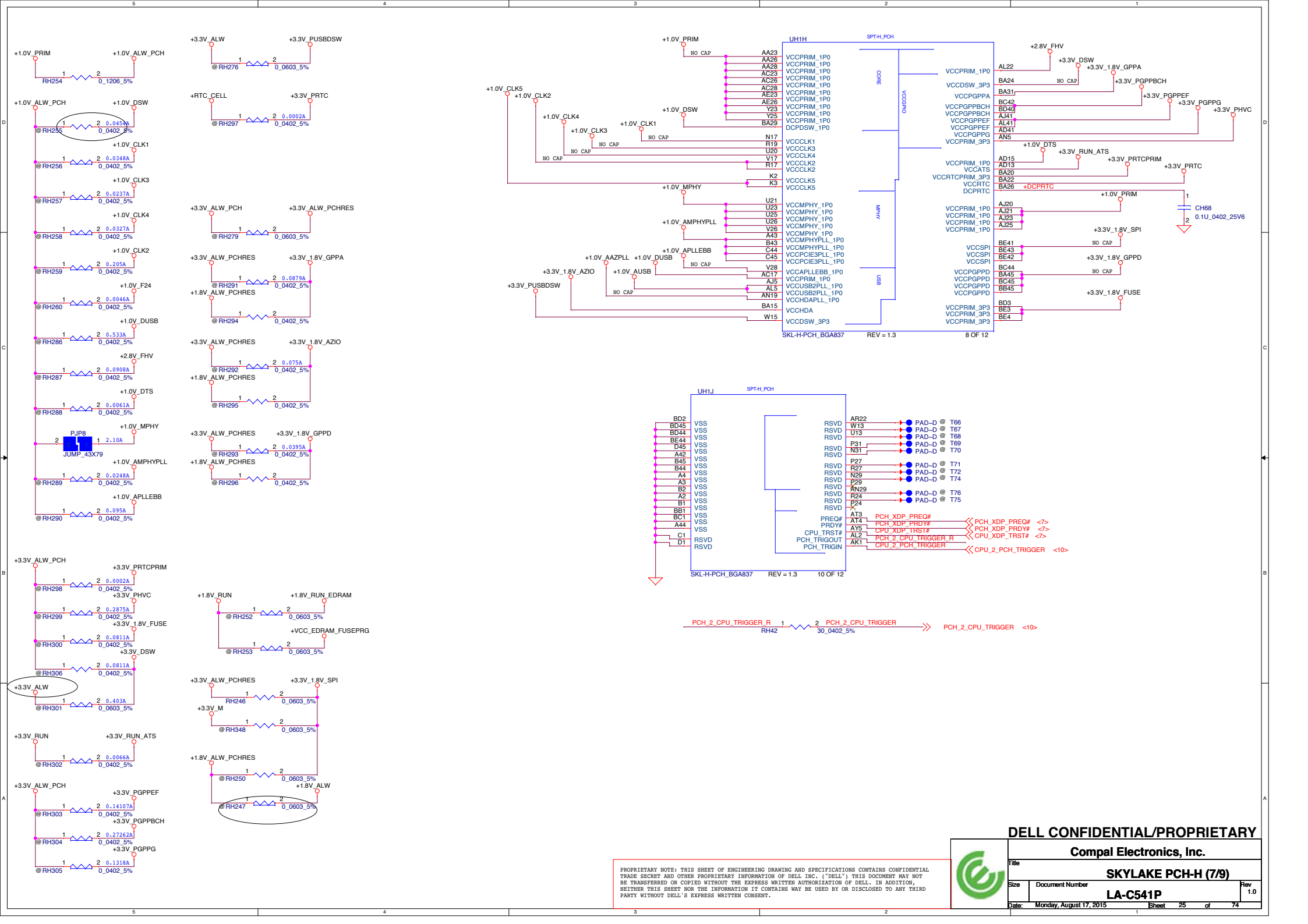
Compal Electronics, Inc.		
Title: SKYLAKE PCH-H (6/9)		
Size	Document Number: LA-C541P	Rev: 1.0
Date: Monday, August 17, 2015	Sheet 24 of 74	



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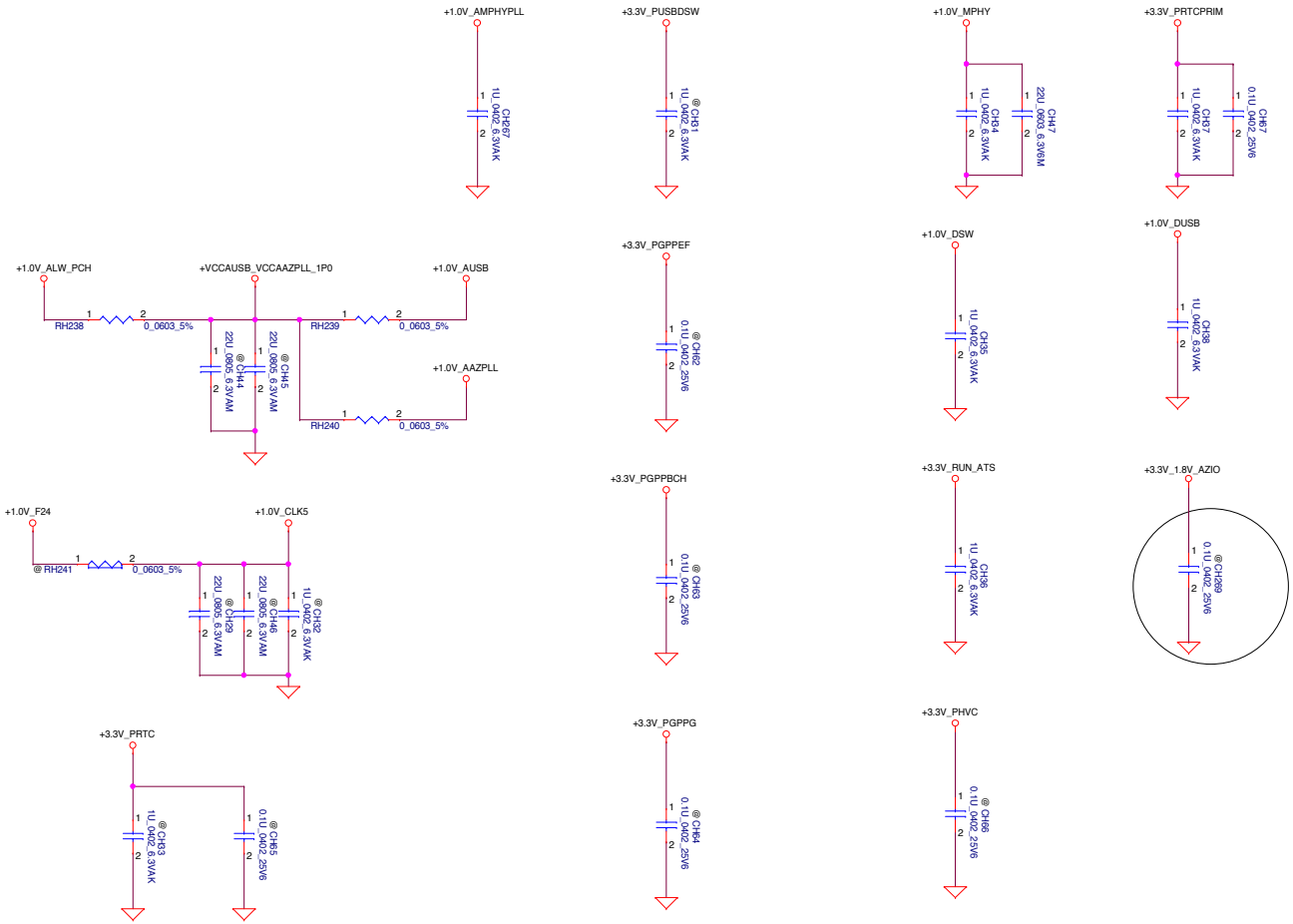
Compal Electronics, Inc.

Title: SKYLAKE PCH-H (7/9)

Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 25 of 74



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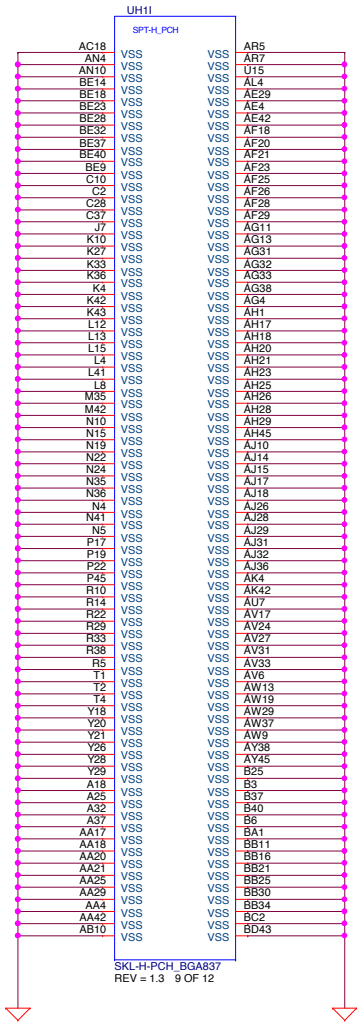
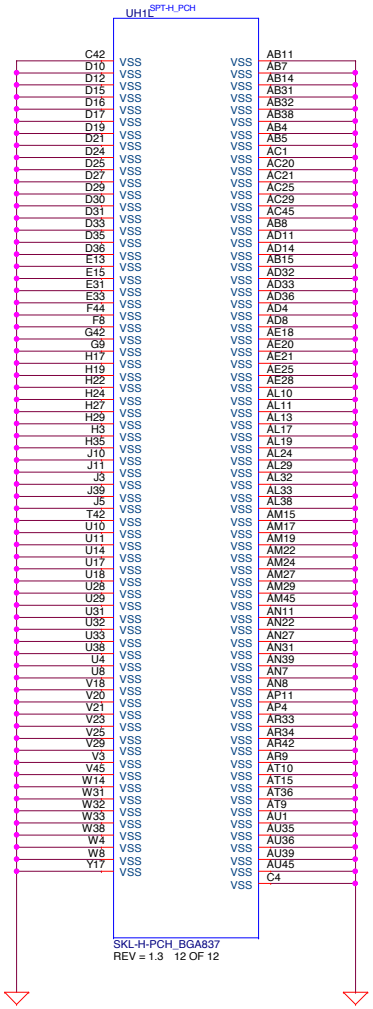
Title: SKYLAKE PCH-H (8/9)

Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 26 of 74





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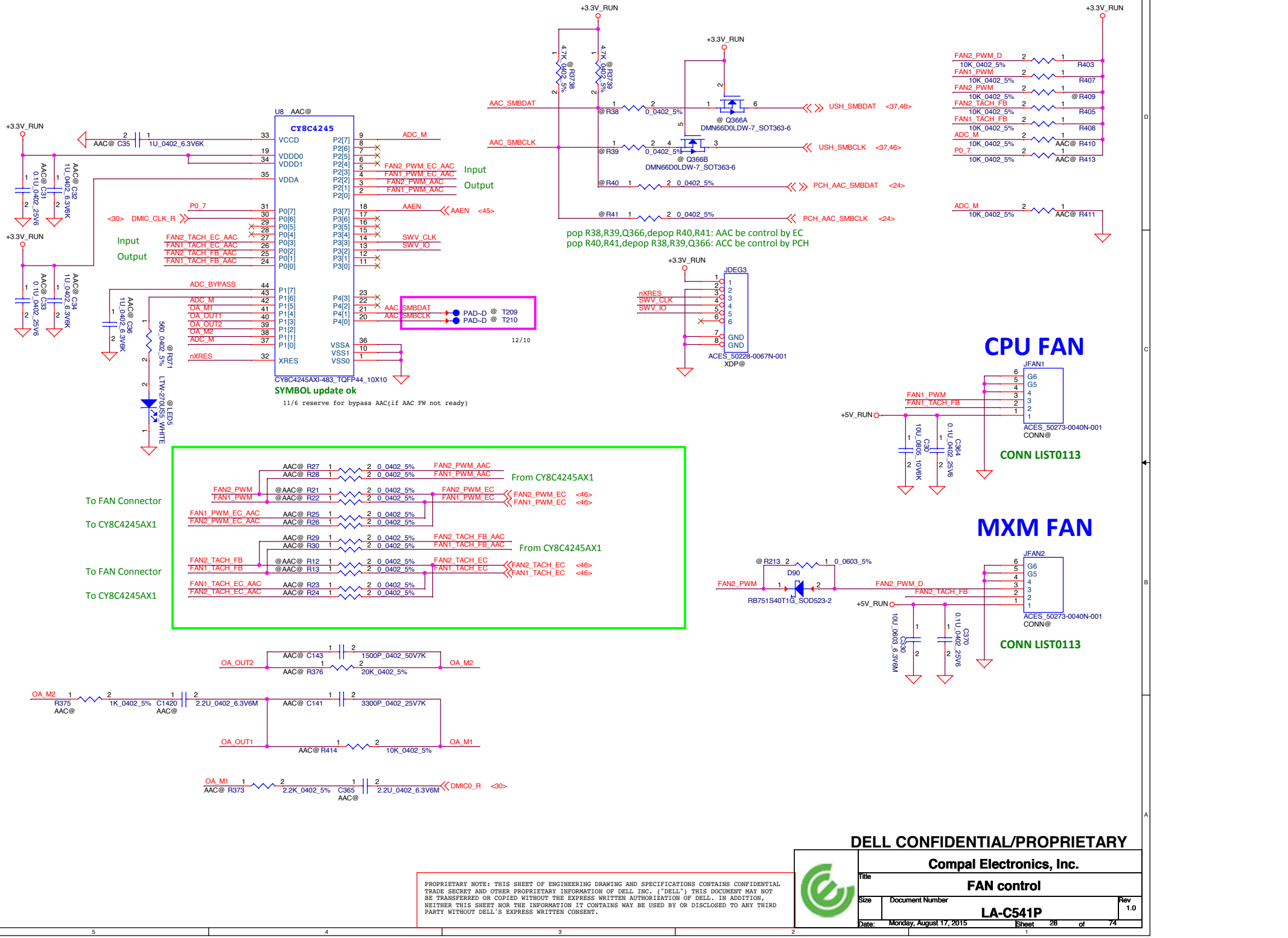
Compal Electronics, Inc.	
Title	SKYLAKE PCH-H (9/9)
Size	Document Number: LA-C541P
Rev	1.0
Date: Monday, August 17, 2015	Sheet 27 of 74



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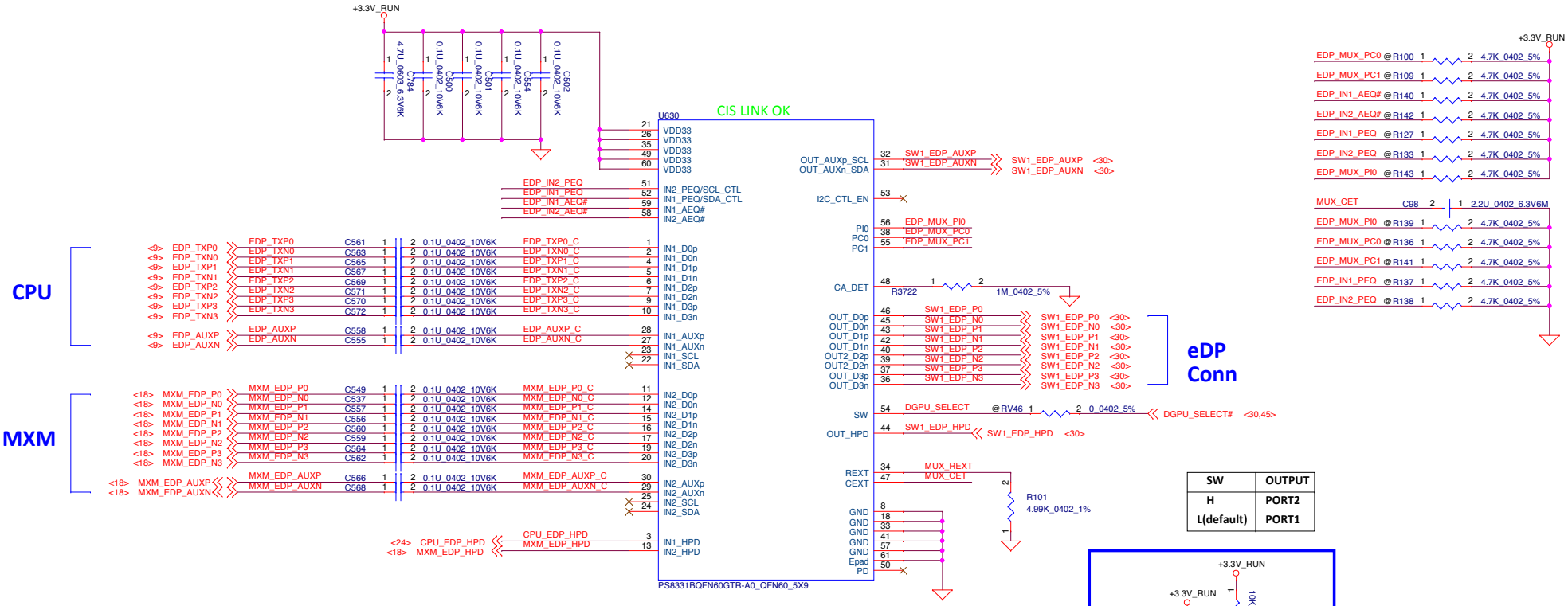
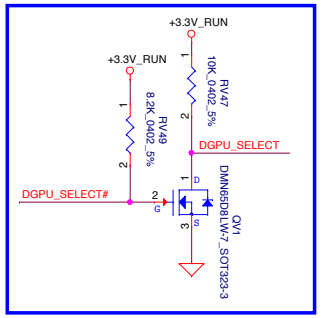
Compal Electronics, Inc.	
Title	FAN control
Size	Document Number: LA-C541P
Rev	1.0
Date:	Monday, August 17, 2015
Sheet	28 of 74



SW	OUTPUT
H	PORT2
L(default)	PORT1



for DP Lane bus layout routing smoothly.

```
INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2
```

```
INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable
```

```
PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable
```

```
PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB
```

```
PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%
```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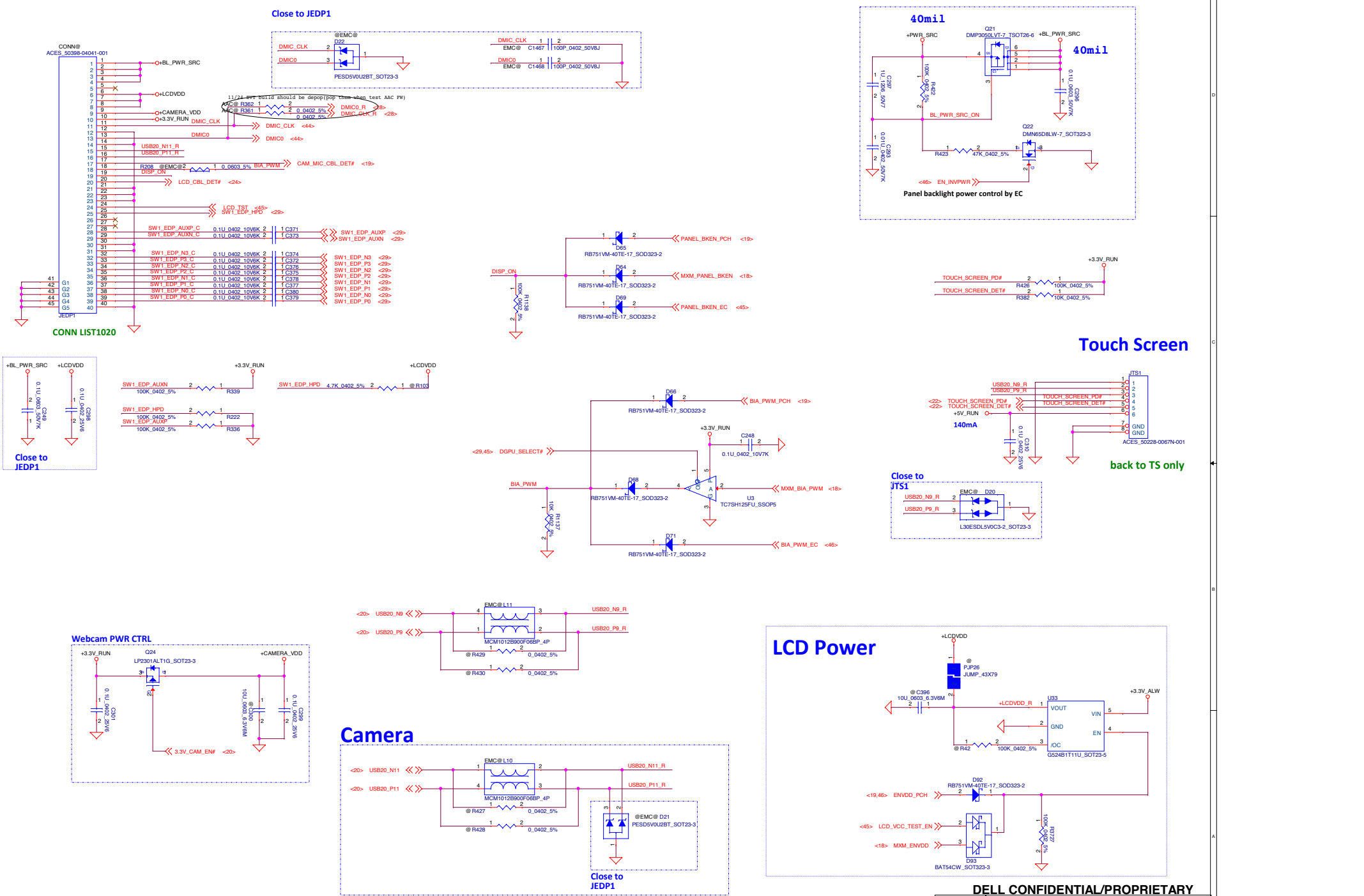
Compal Electronics, Inc.

Title: eDP MUX (PS8331)

Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 29 of 74



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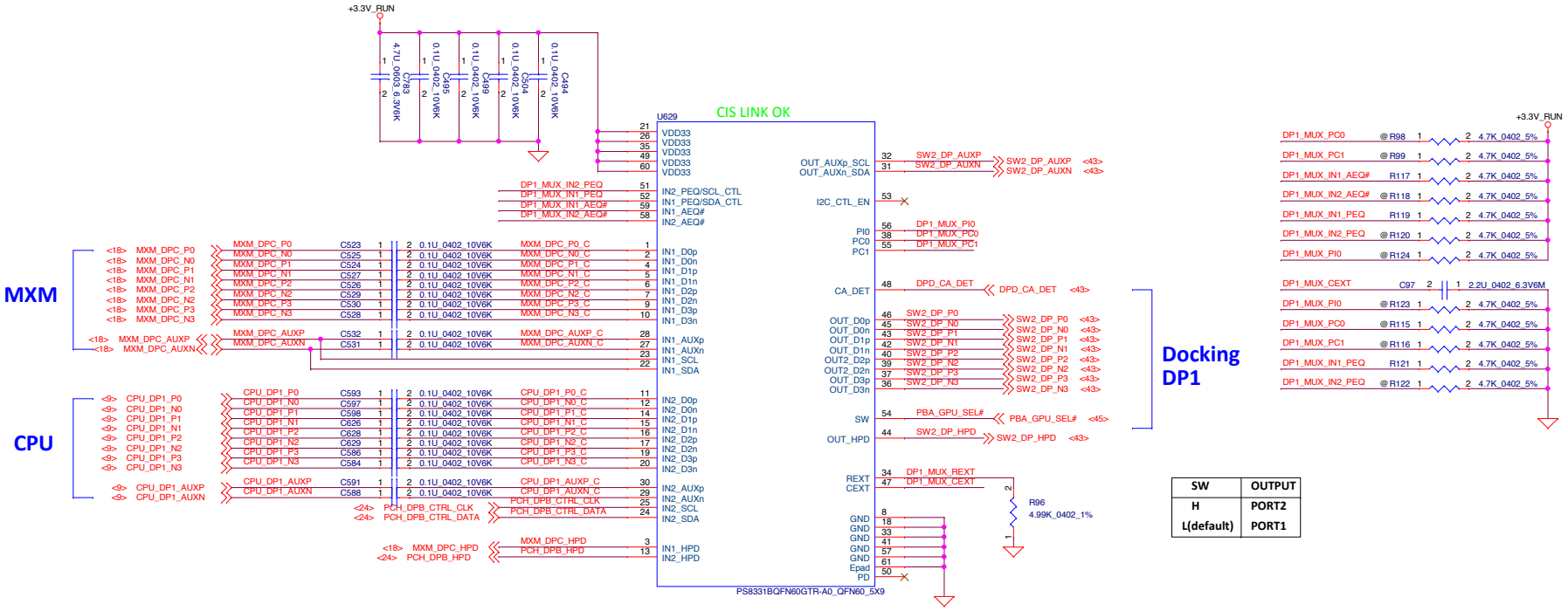
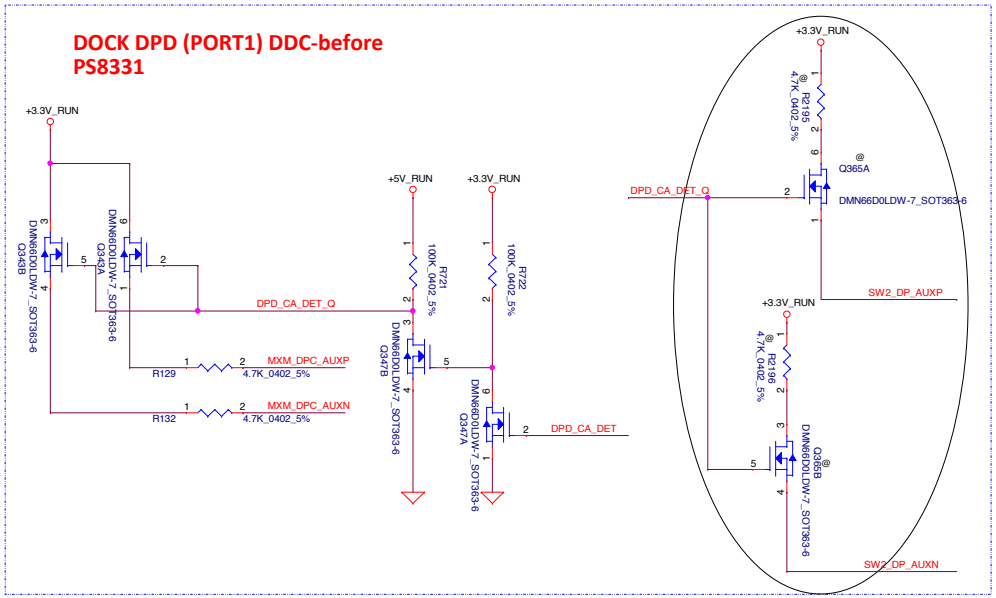


SW	OUTPUT
H	PORT2
L(default)	PORT1

11/11 parade2級串接,中間ddc可不用加pull up



INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

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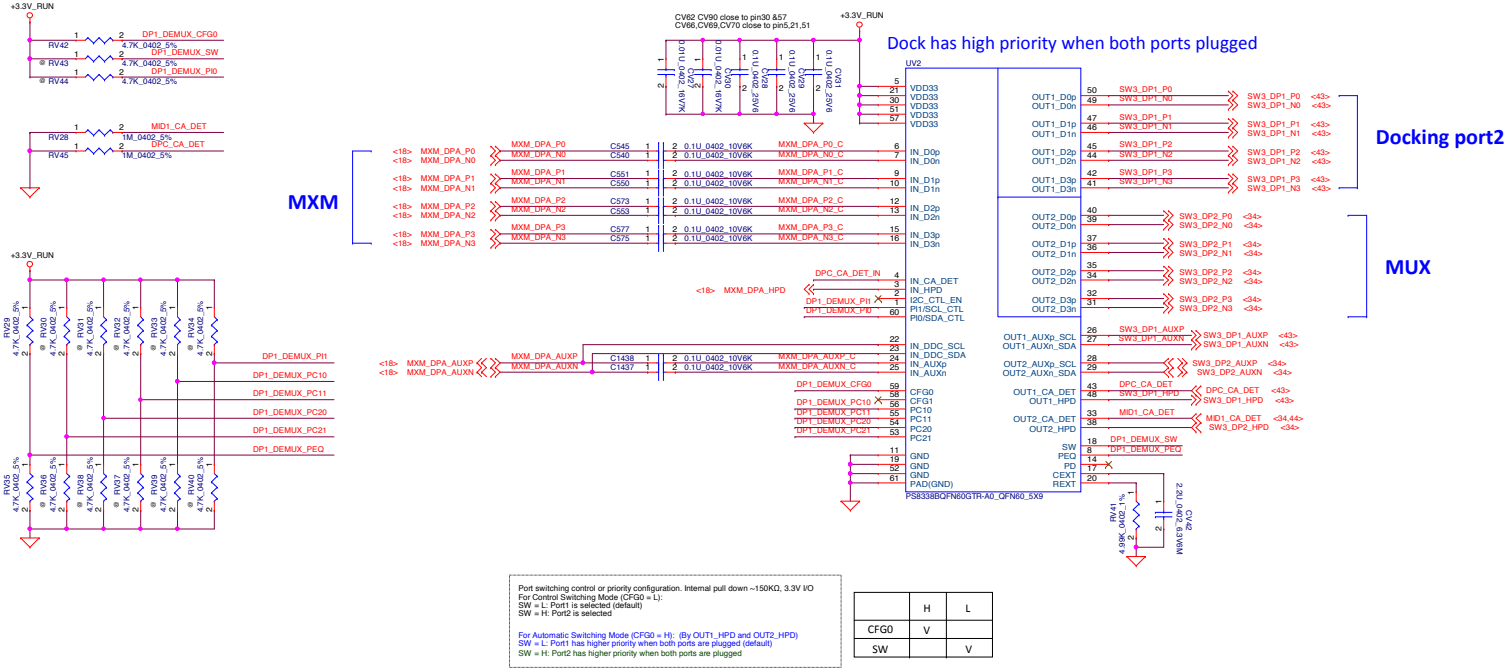
DELL CONFIDENTIAL/PROPRIETARY

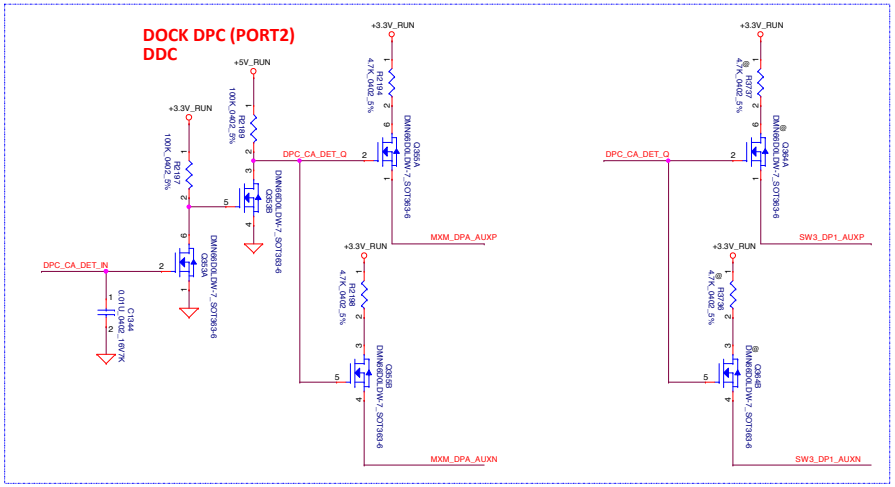
Compal Electronics, Inc.

Title: MXM/CPU MUX(PS8331)

Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 31 of 74





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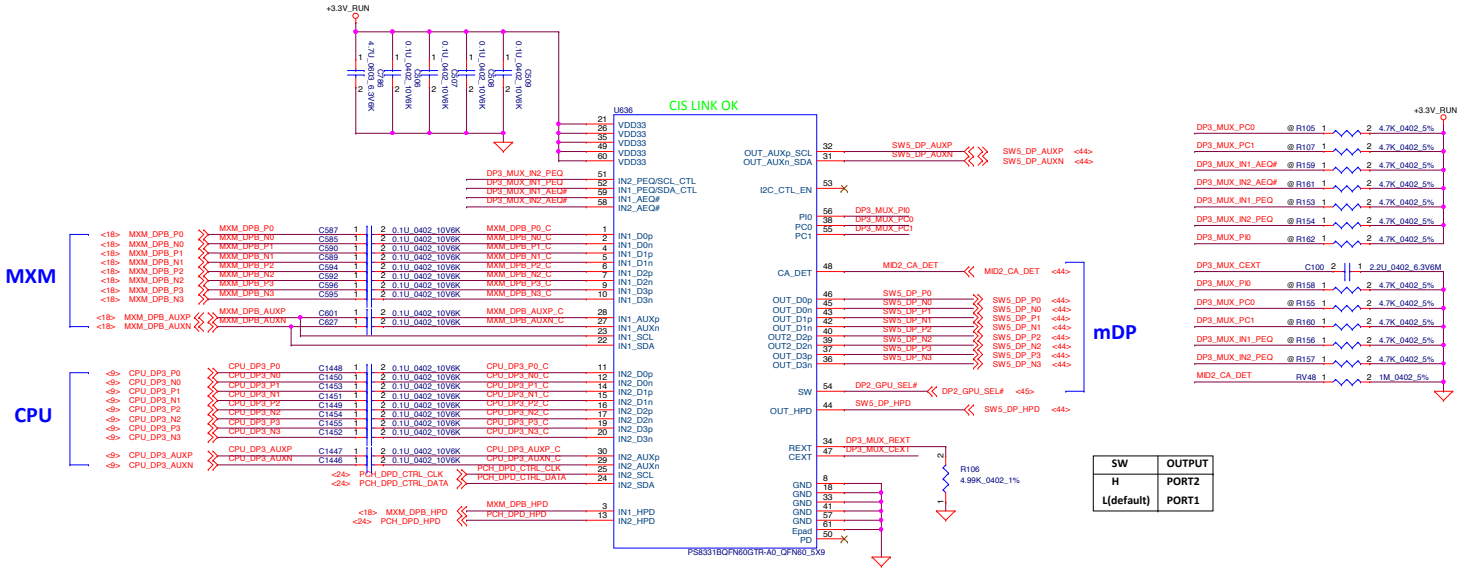
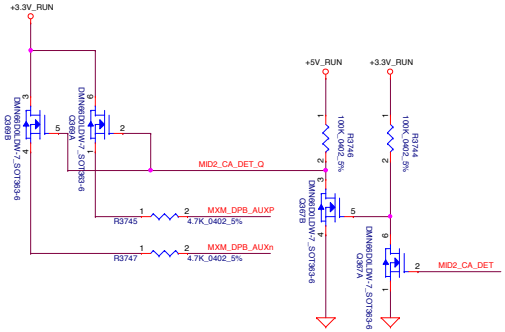
Compal Electronics, Inc.		
Title	DP DeMUX (PS8338)	
Size	Document Number: LA-C541P	Rev: 1.0
Date: Monday, August 17, 2015	Sheet 32 of 74	





INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PIO = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PCO = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

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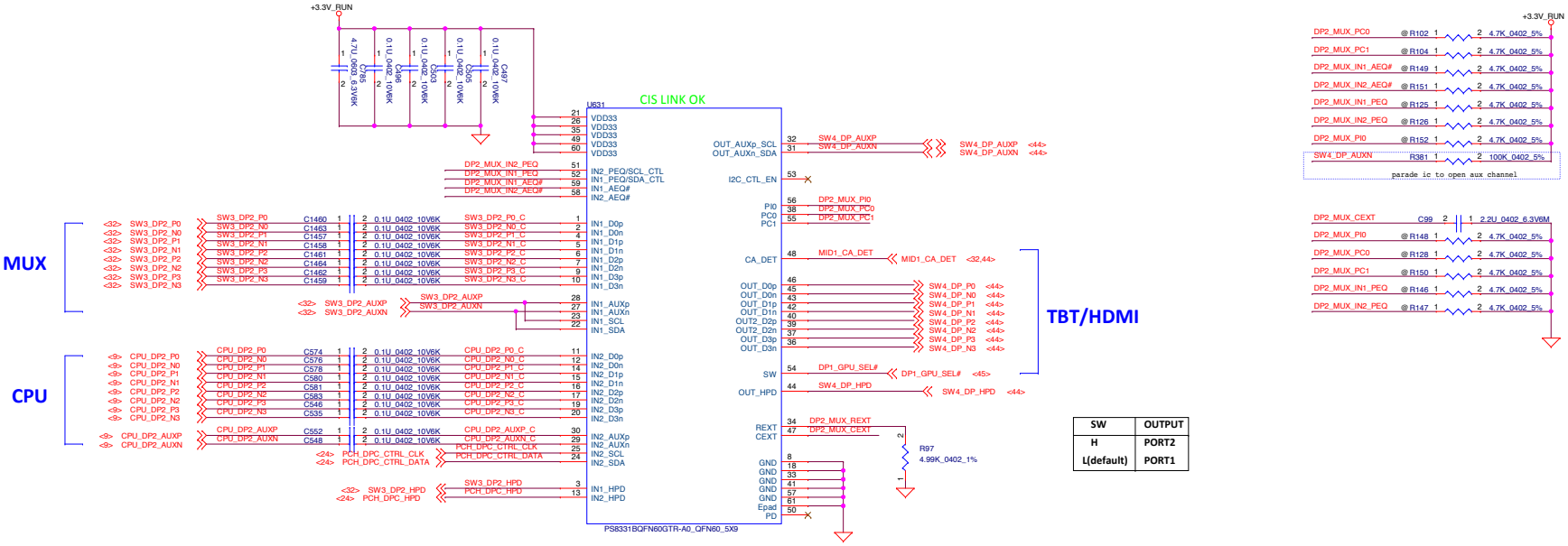
Compal Electronics, Inc.

Title: DP MUX(PS8331)

Size: | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 33 of 74



SW	OUTPUT
H	PORT2
L(default)	PORT1

INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

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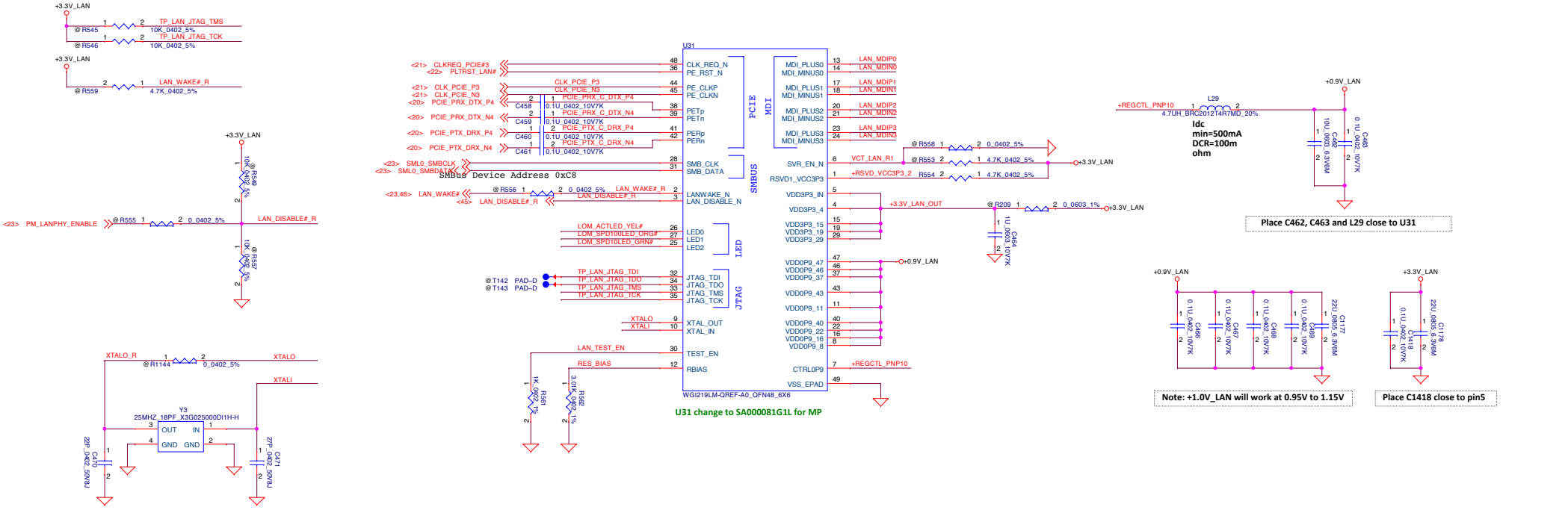
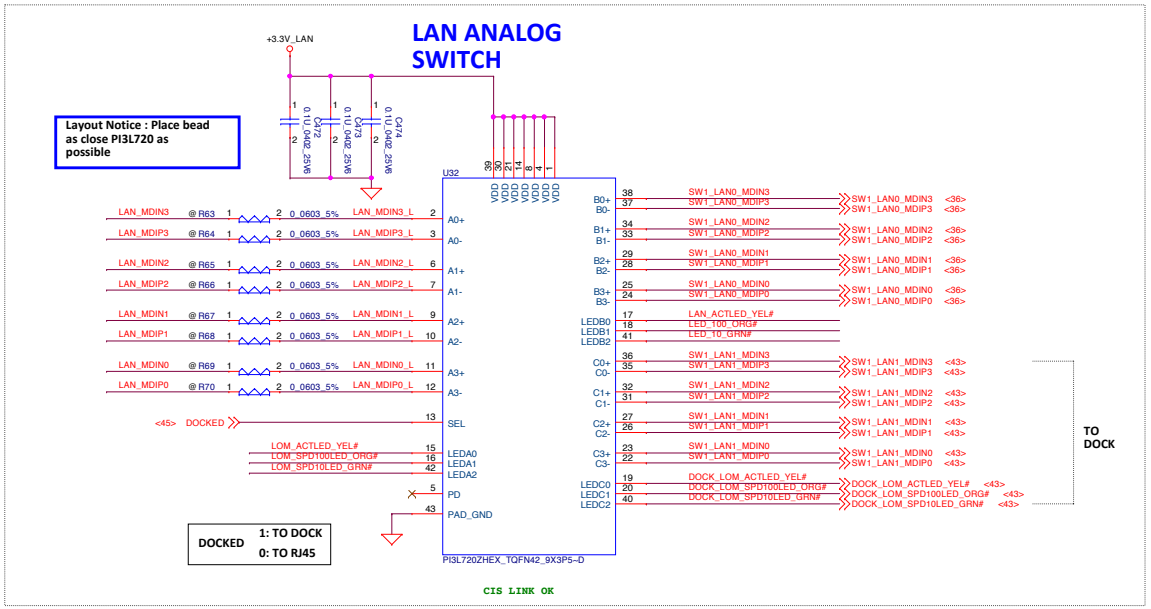
Compal Electronics, Inc.

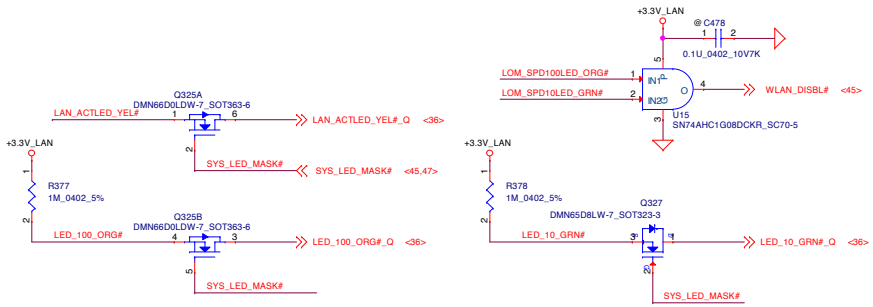
Title: TBT MUX(PS8331)

Size: | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 34 of 74







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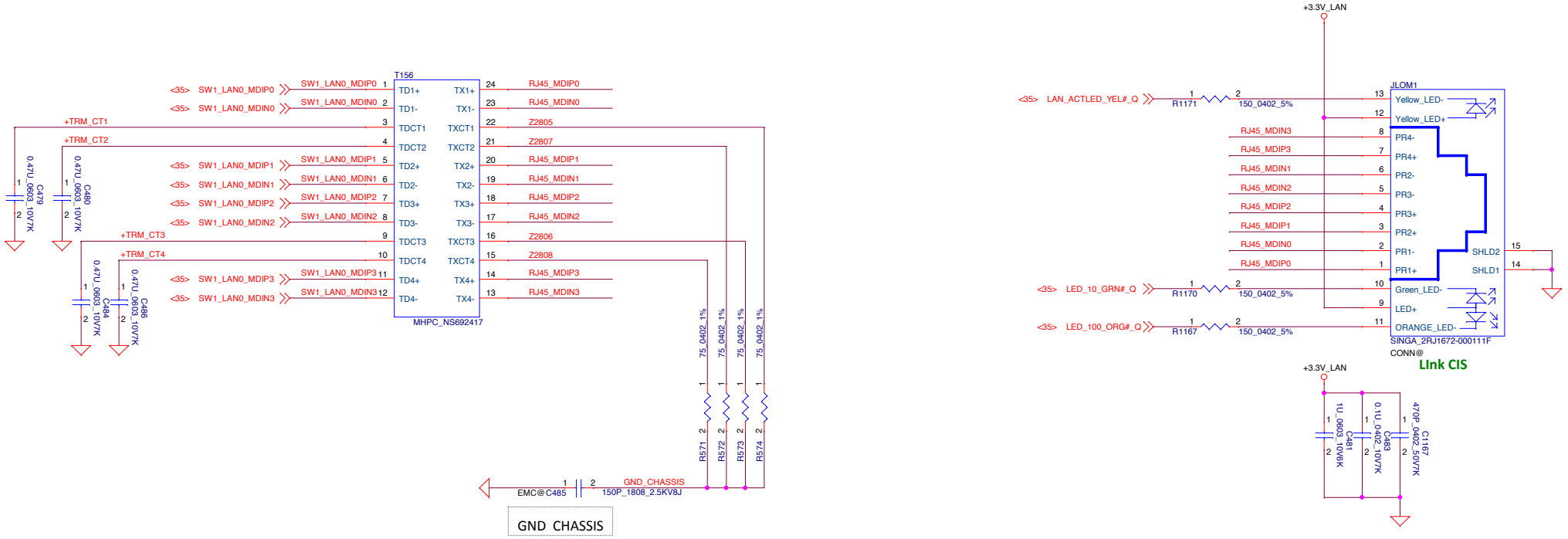
Compal Electronics, Inc.

Title: LAN/LAN SW

Size: | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 35 of 74

+3.3V_LAN/+3.3V_LAN_LOM:20mils



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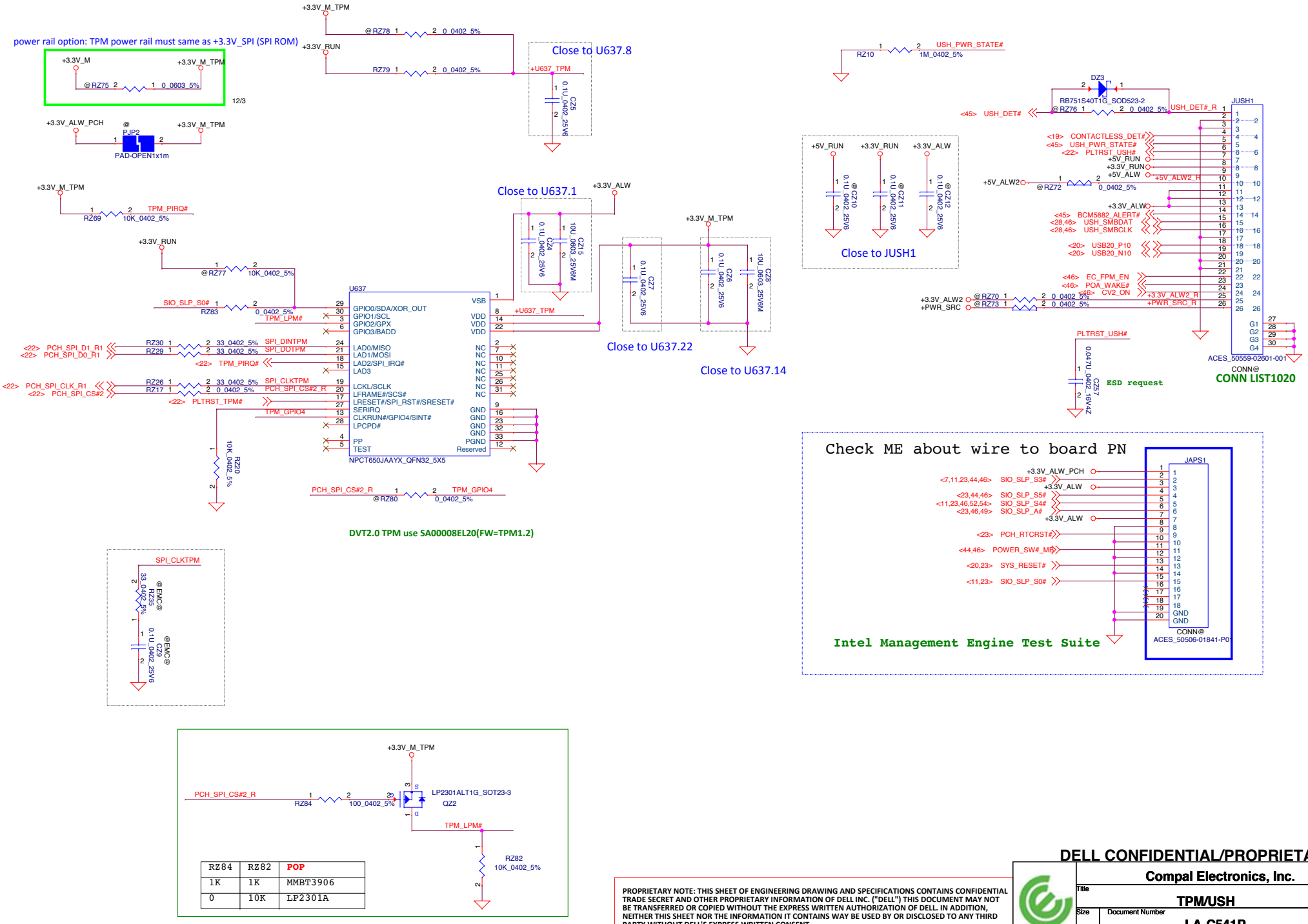
Compal Electronics, Inc.

Title: RJ45

Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 36 of 74



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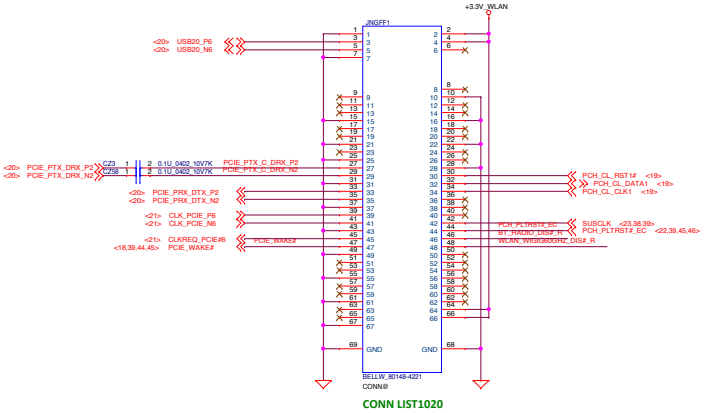
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

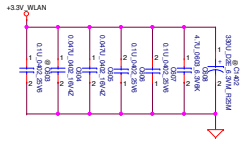
Title	TPM/USH	
Size	Document Number: LA-C541P	Rev: 1.0
Date: Monday, August 17, 2015	Sheet 37 of 74	

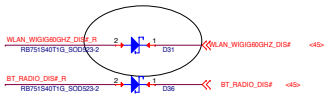
WLAN/BT

NGFF slot_1 Key A



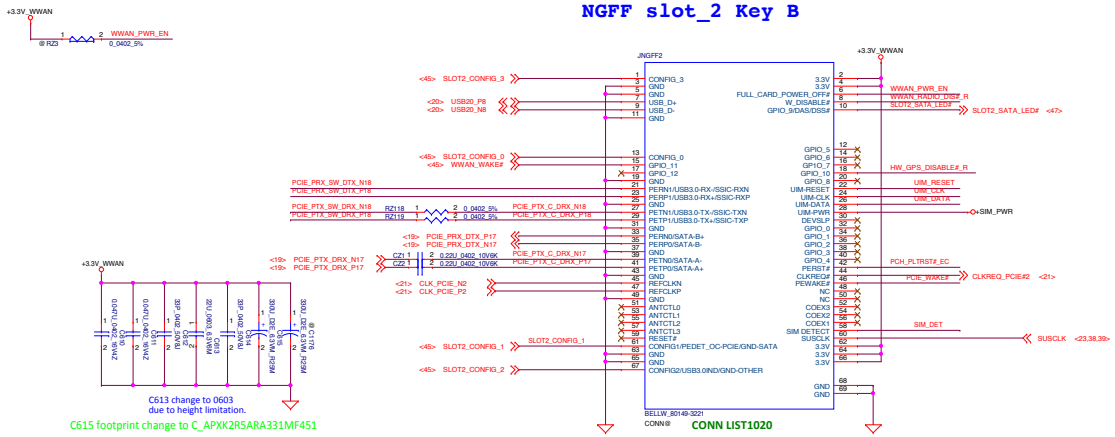
CONN LIST1020





WWAN/LTE/HCA/Cache

NGFF slot_2 Key B

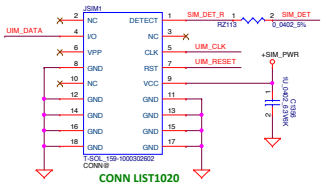


CONN LIST1020

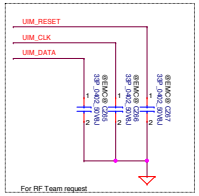
C613 change to 0603
due to height limitation.

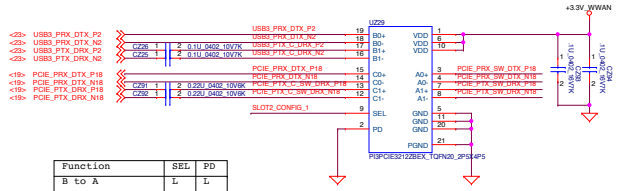
C615 footprint change to C_APXK2R5ARA331MF451

SIM Card Push-Push



JSIM1 pin1 (detect)	SIM card detect
0	SIM no present
1	SIM tray present





Function	SEL	PD
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
1	0	1	0	0	SSD-PCIE
8	0	0	1	1	WWAN-USB3.0
14	1	0	1	1	HCA-PCIE

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Compal Electronics, Inc.	
Title	M.2 Card-1/2
Size	Document Number: LA-C541P
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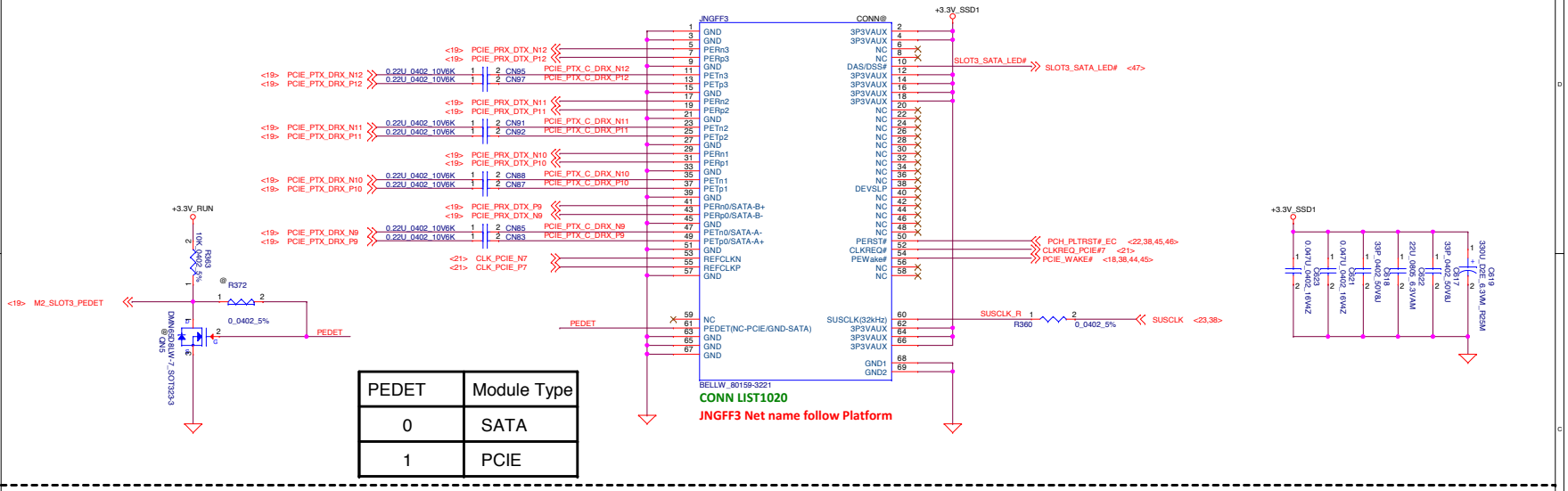
Date: Monday, August 17, 2015	Sheet 38 of 74

SSD
NGFF slot_3 Key M



PEDET	Module Type
0	SATA
1	PCIE

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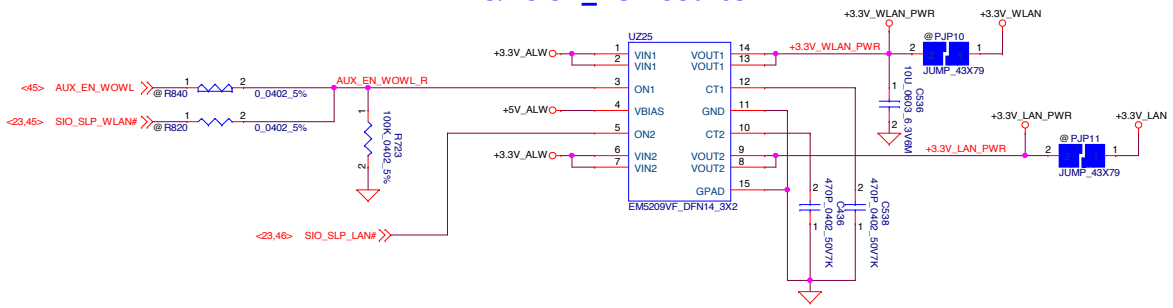
Compal Electronics, Inc.

Title: M.2 Card-2/2

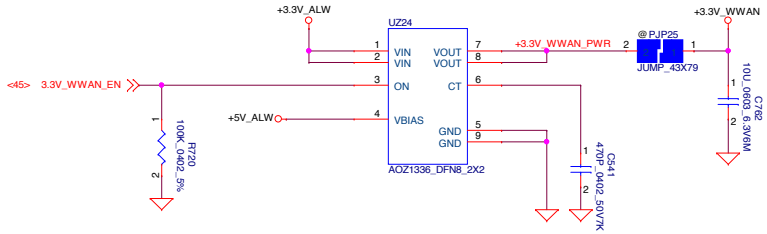
Size: Document Number: LA-C541P Rev: 1.0

Date: Monday, August 17, 2015 Sheet 39 of 74

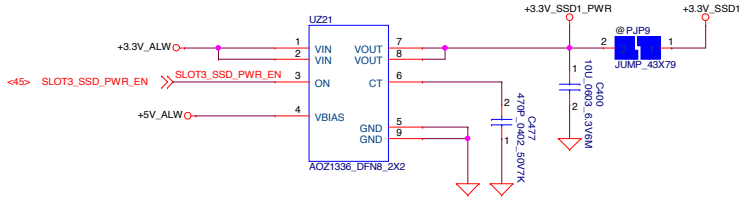
Power Control for M.2 slot 1. & +3.3V_RUN Source



Power Control for M.2 slot 2.



Power Control for M.2 slot 3. Source



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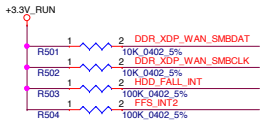
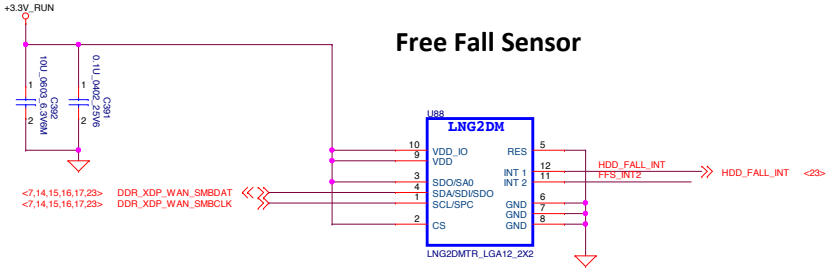
Compal Electronics, Inc.

Title: M.2 Card PWR

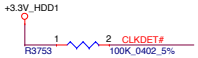
Size | Document Number: LA-C541P | Rev: 1.0

Date: Monday, August 17, 2015 | Sheet 40 of 74

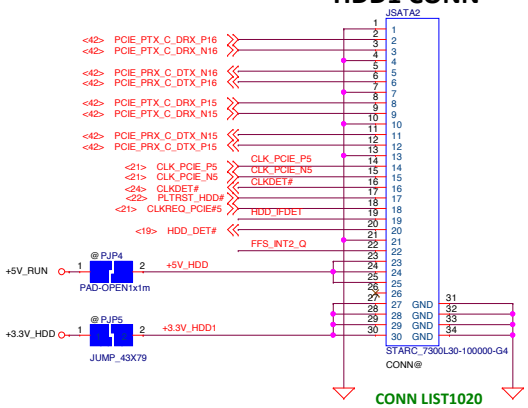




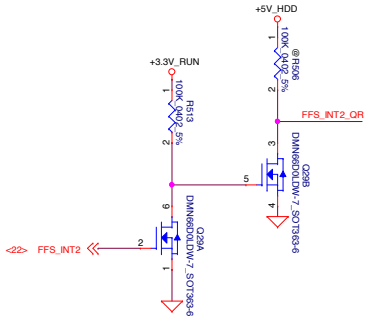
Free Fall Sensor



HDD1 CONN



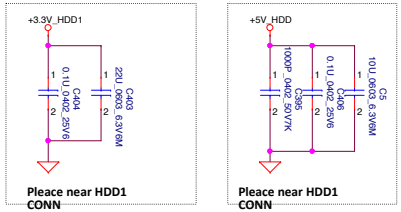
CONN LIST1020

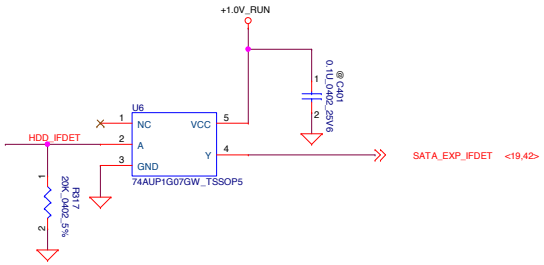


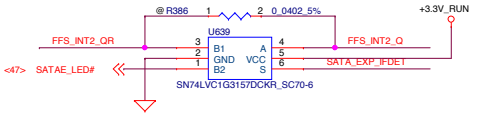
HDD_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

SATA_EXP_IFDET	channel on
0	A-->B1
1	A-->B2







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Compal Electronics, Inc.

Title	HDD CONN	
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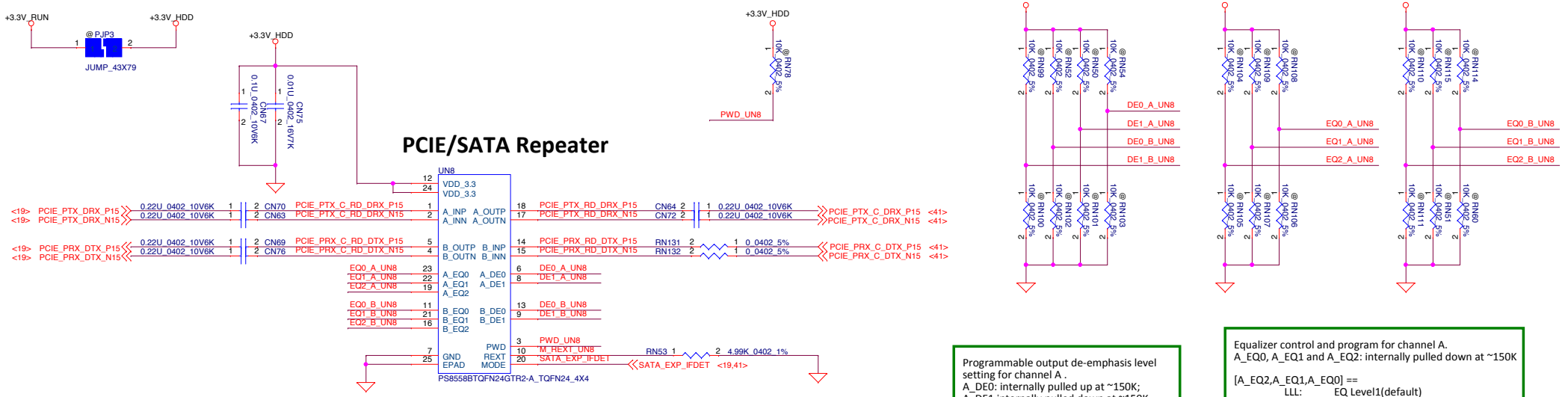


PWD	Funtion
0	Normal mode(Default)
1	Chip power down

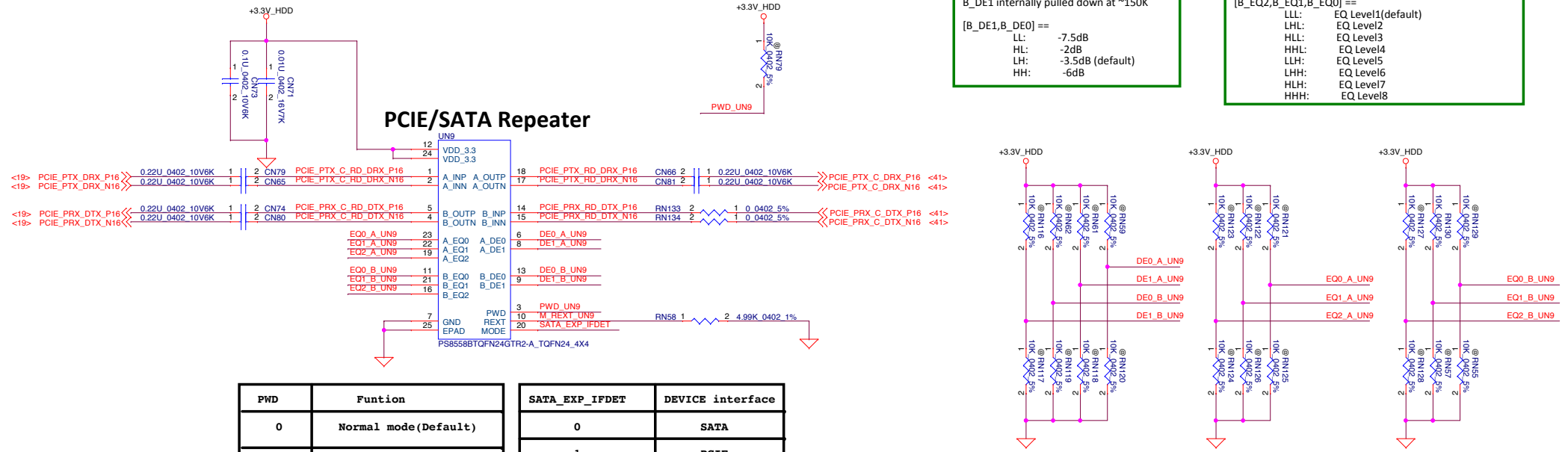
SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

Programmable output de-emphasis level setting for channel A .
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
LL: -7.5dB
HL: -2dB
LH: -3.5dB (default)
HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

[A_EQ2,A_EQ1,A_EQ0] ==
LLL: EQ Level1(default)
LHL: EQ Level2
HLL: EQ Level3
HHL: EQ Level4
LLH: EQ Level5
LHH: EQ Level6
HLH: EQ Level7
HHH: EQ Level8



PWD	Funtion
0	Normal mode(Default)
1	Chip power down

SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

[B_DE1,B_DE0] ==
LL: -7.5dB
HL: -2dB
LH: -3.5dB (default)
HH: -6dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

[B_EQ2,B_EQ1,B_EQ0] ==
LLL: EQ Level1(default)
LHL: EQ Level2
HLL: EQ Level3
HHL: EQ Level4
LLH: EQ Level5
LHH: EQ Level6
HLH: EQ Level7
HHH: EQ Level8

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

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Compal Electronics, Inc.

Title: HDD PCIE/SATA repeater

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EMI request add 33ohm for DOCK DVI signals.

Dock DPD (Port 1)

Dock DPC (Port 2)

R492 1 2 DPD_CA_DET 1M_0402_5%

JDOCK1 CONN@

DOCK_DET_1

<35> DOCK_LOM_SPD10LED_GRN#
<31> DPD_CA_DET

<31> SW2_DP_P0 / <31> SW2_DP_N0 — C366 / C367 0.1U_0402_10V7K — SW2_DP_P0_C / SW2_DP_N0_C — EMC@ R2164 / R2165 33_0402_5% — SW2_DP_P0_R / SW2_DP_N0_R

<31> SW2_DP_P1 / <31> SW2_DP_N1 — C368 / C369 0.1U_0402_10V7K — SW2_DP_P1_C / SW2_DP_N1_C — EMC@ R2166 / R2167 33_0402_5% — SW2_DP_P1_R / SW2_DP_N1_R

<31> SW2_DP_P2 / <31> SW2_DP_N2 — C424 / C425 0.1U_0402_10V7K — SW2_DP_P2_C / SW2_DP_N2_C — EMC@ R2168 / R2169 33_0402_5% — SW2_DP_P2_R / SW2_DP_N2_R

<31> SW2_DP_P3 / <31> SW2_DP_N3 — C426 / C427 0.1U_0402_10V7K — SW2_DP_P3_C / SW2_DP_N3_C — EMC@ R2170 / R2171 33_0402_5% — SW2_DP_P3_R / SW2_DP_N3_R

<31> SW2_DP_AUXP / <31> SW2_DP_AUXN — SW2_DP_AUXP / SW2_DP_AUXN

<31> SW2_DP_HPD — 0.033U_0402_16V7K @C695

Close to DOCK
Its for Enhance ESD on dock issue.

SW2_DP_HPD — 100K_0402_5% R757

+NBDOCK_DC_IN_SS

<18> BLUE_DOCK — BLUE_DOCK
<18> RED_DOCK — RED_DOCK
<18> GREEN_DOCK — GREEN_DOCK
<18> HSYNC_DOCK
<18> VSYNC_DOCK
<46> CLK_MSE
<46> DAT_MSE
<44> DAI_BCLK#
<44> DAI_LRCK#
<44> DAI_DI
<44> DAI_DO#
<44> DAI_12MHZ#
<45> D_LAD0
<45> D_LAD1
<45> D_LAD2
<45> D_LAD3
<45> D_LFRAME#
<45> D_CLKRUN#
<45> D_SERIRQ
<45> D_DLDRQ1#
<23> CLK_PCI_DOCK
<44,46> DOCK_TNY_SMB_CLK
<44,46> DOCK_TNY_SMB_DAT
<44,45,50> DOCK_TNY_SMBUS_ALRT#
<50> DOCK_PSID
<46> DOCK_PWR_BTN#
<45,50,60> SLICE_BAT_PRES#

+DOCK_PWR_BAR — 4.7U_0805_25V6-K @C58 — 0.1U_0603_50V7K @C702 — 3 2 1 @D33 30ESD24VC3-2_SOT23-3

GND1 PWR1 PWR1 — Shield_G x6 — WD2F144WB8 — FOX_QL01723-D265G1-8H

GND2 PWR2 PWR2 — Shield_G x6 — +DOCK_PWR_BAR — 0.1U_0603_50V7K @C703

DOCK_AC_OFF <60>
DOCK_LOM_SPD100LED_ORG# <35>
DPC_CA_DET <32>

SW3_DP1_P0 / SW3_DP1_N0 — EMC@ R2172 / R2173 33_0402_5% — SW3_DP1_P0_C / SW3_DP1_N0_C — 0.1U_0402_10V7K — C431 / C438 — SW3_DP1_P0 / SW3_DP1_N0 <32>

SW3_DP1_P1 / SW3_DP1_N1 — EMC@ R2174 / R2175 33_0402_5% — SW3_DP1_P1_C / SW3_DP1_N1_C — 0.1U_0402_10V7K — C439 / C440 — SW3_DP1_P1 / SW3_DP1_N1 <32>

SW3_DP1_P2 / SW3_DP1_N2 — EMC@ R2176 / R2177 33_0402_5% — SW3_DP1_P2_C / SW3_DP1_N2_C — 0.1U_0402_10V7K — C441 / C442 — SW3_DP1_P2 / SW3_DP1_N2 <32>

SW3_DP1_P3 / SW3_DP1_N3 — EMC@ R2178 / R2179 33_0402_5% — SW3_DP1_P3_C / SW3_DP1_N3_C — 0.1U_0402_10V7K — C443 / C444 — SW3_DP1_P3 / SW3_DP1_N3 <32>

SW3_DP1_AUXP / SW3_DP1_AUXN <32>

SW3_DP1_HPD

ACAV_DOCK_SRC# <57,60>
DAT_DDC2_DOCK <18>
CLK_DDC2_DOCK <18>

SATA_PRX_C_DTX_P1 / SATA_PRX_C_DTX_N1 — C697 / C698 0.01U_0402_16V7K — SATA_PRX_DTX_P1 / SATA_PRX_DTX_N1 <19>

SATA_PTX_C_DRX_P1 / SATA_PTX_C_DRX_N1 — C699 / C700 0.01U_0402_16V7K — SATA_PTX_DRX_P1 / SATA_PTX_DRX_N1 <19>

2/9 P/N error

USB20_P5 <20> / USB20_N5 <20>
USB20_P7 <20> / USB20_N7 <20>
CLK_KBD <46>
DAT_KBD <46>
USB3_PRX_DTX_N6 <23> / USB3_PRX_DTX_P6 <23>
USB3_PTX_DRX_N6 <23> / USB3_PTX_DRX_P6 <23>
BREATH_LED# <46,47>
DOCK_LOM_ACTLED_YEL# <35>
SW1_LAN1_MDIP0 <35> / SW1_LAN1_MDIN0 <35>
SW1_LAN1_MDIP1 <35> / SW1_LAN1_MDIN1 <35>
SW1_LAN1_MDIP2 <35> / SW1_LAN1_MDIN2 <35>
SW1_LAN1_MDIP3 <35> / SW1_LAN1_MDIN3 <35>
DOCK_DCIN_IS+ <57> / DOCK_DCIN_IS- <57>
DOCK_POR_RST# <46>

+LOM_VCT — 1U_0402_6.3V6K @C701

DOCK_DET_R# — D32 RB751S40T1G_SOD523-2 — DOCK_DET# <45>

SW3_DP1_HPD <32> — 0.033U_0402_16V7K @C696

Close to DOCK
Its for Enhance ESD on dock issue.

SW3_DP1_HPD — 100K_0402_5% R2160

audio not transfer to DP display if play movie when attached external DP display

+3.3V_ALW — DOCK_DET# — 10K_0402_5% R755

System hangs after hot dock.

CONN LIST1124

DAI_12MHZ# — EMC@ RE11 10_0402_1% — EMC@ CE8 4.7P_0402_50V8C

DAI_BCLK# — EMC@ RE12 10_0402_1% — EMC@ CE9 4.7P_0402_50V8C

CLK_PCI_DOCK — EMC@ R756 33_0402_5% — EMC@ C704 12P_0402_50V8J

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Compal Electronics, Inc.	
Title	Docking
Size	Document Number: LA-C541P
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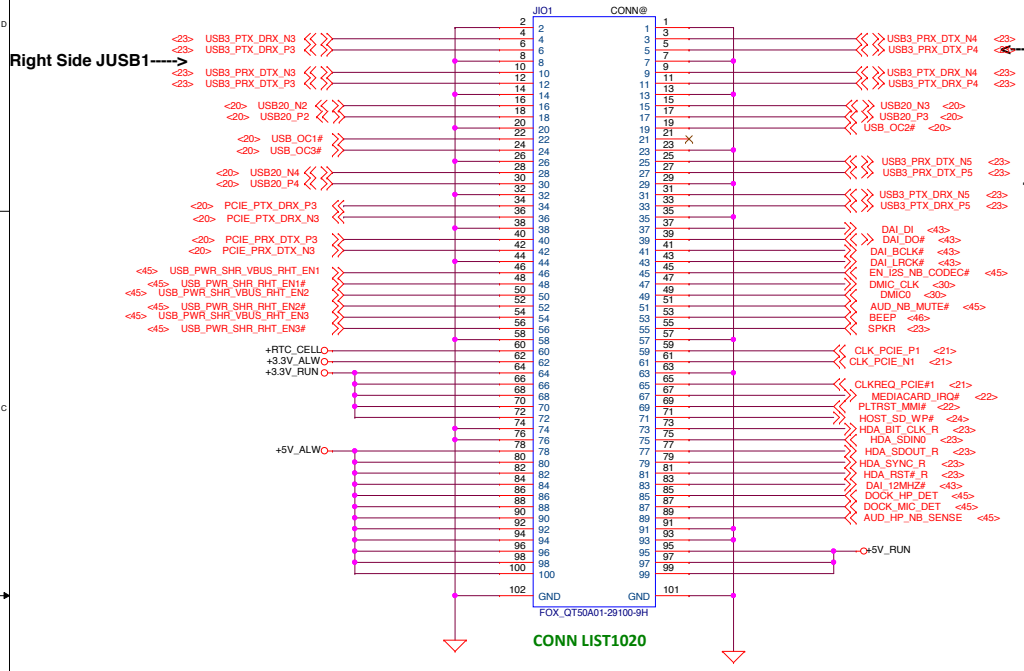
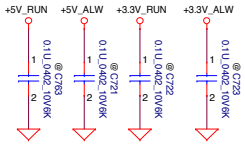
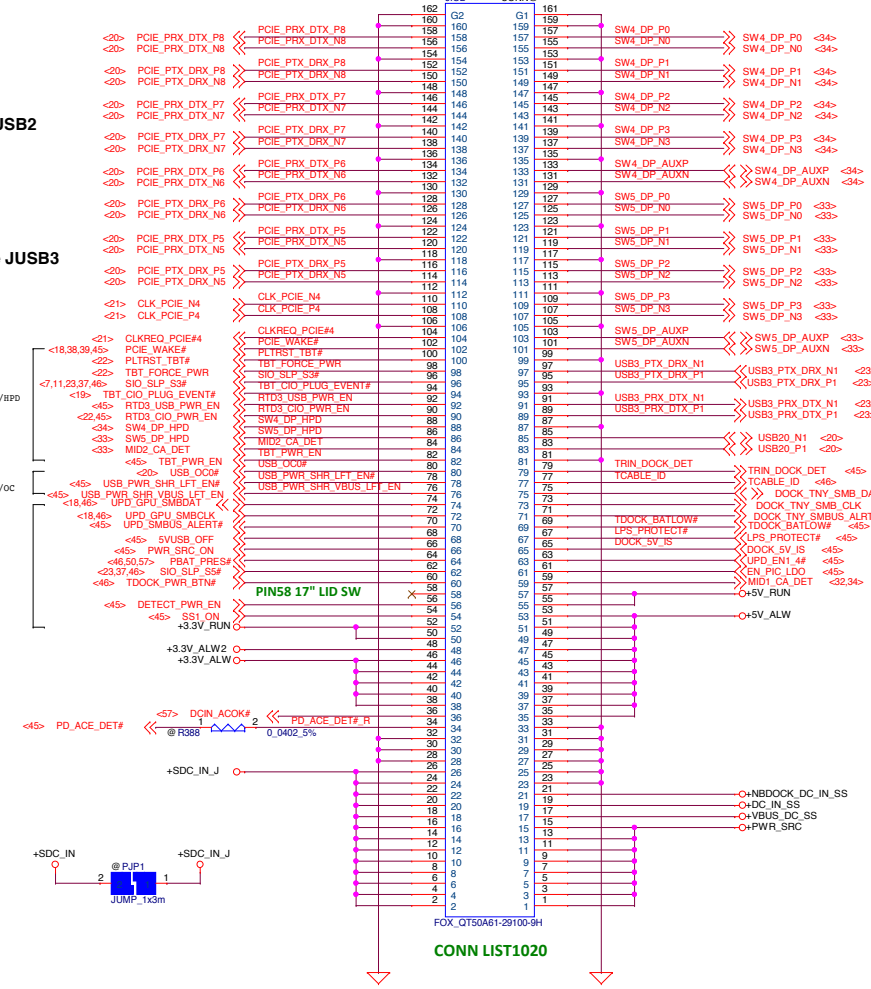
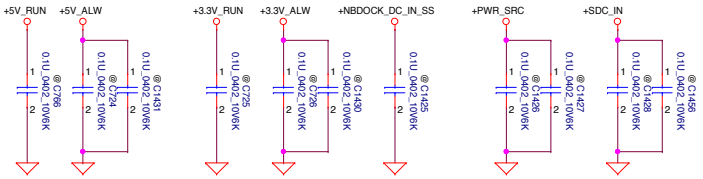
USB/Codec/Card reader IO/B



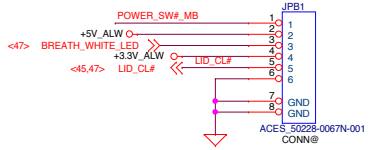


Display daughter /B

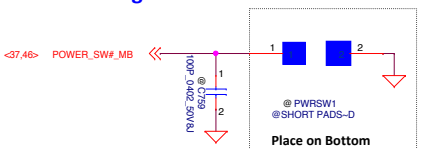


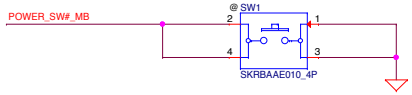


Power Button CONN



Power Switch for debug





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Compal Electronics, Inc.	
Title	IO / PWR Button
Size	Document Number: LA-C541P
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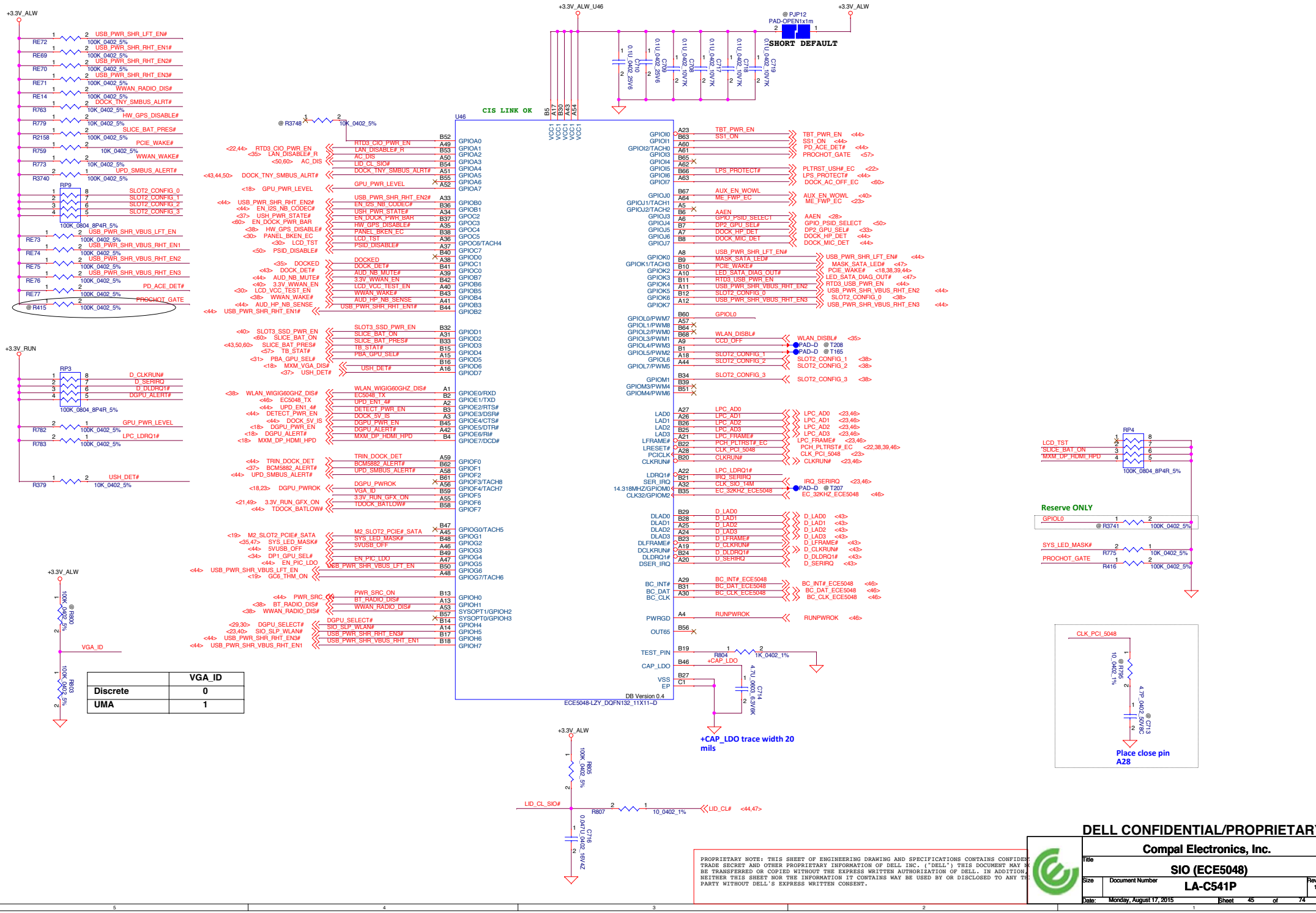
+3.3V_ALW
+3.3V_ALW_U46
+3.3V_RUN
U46
CIS LINK OK
SHORT DEFAULT
@ PJP12
PAD-OPEN1x1m
ECE5048-LZY_DQFN132_11X11~D
DB Version 0.4
+CAP_LDO trace width 20 mils
Place close pin A28
Reserve ONLY
VGA_ID
Discrete 0
UMA 1
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SIO (ECE5048)
LA-C541P
Rev 1.0
Monday, August 17, 2015
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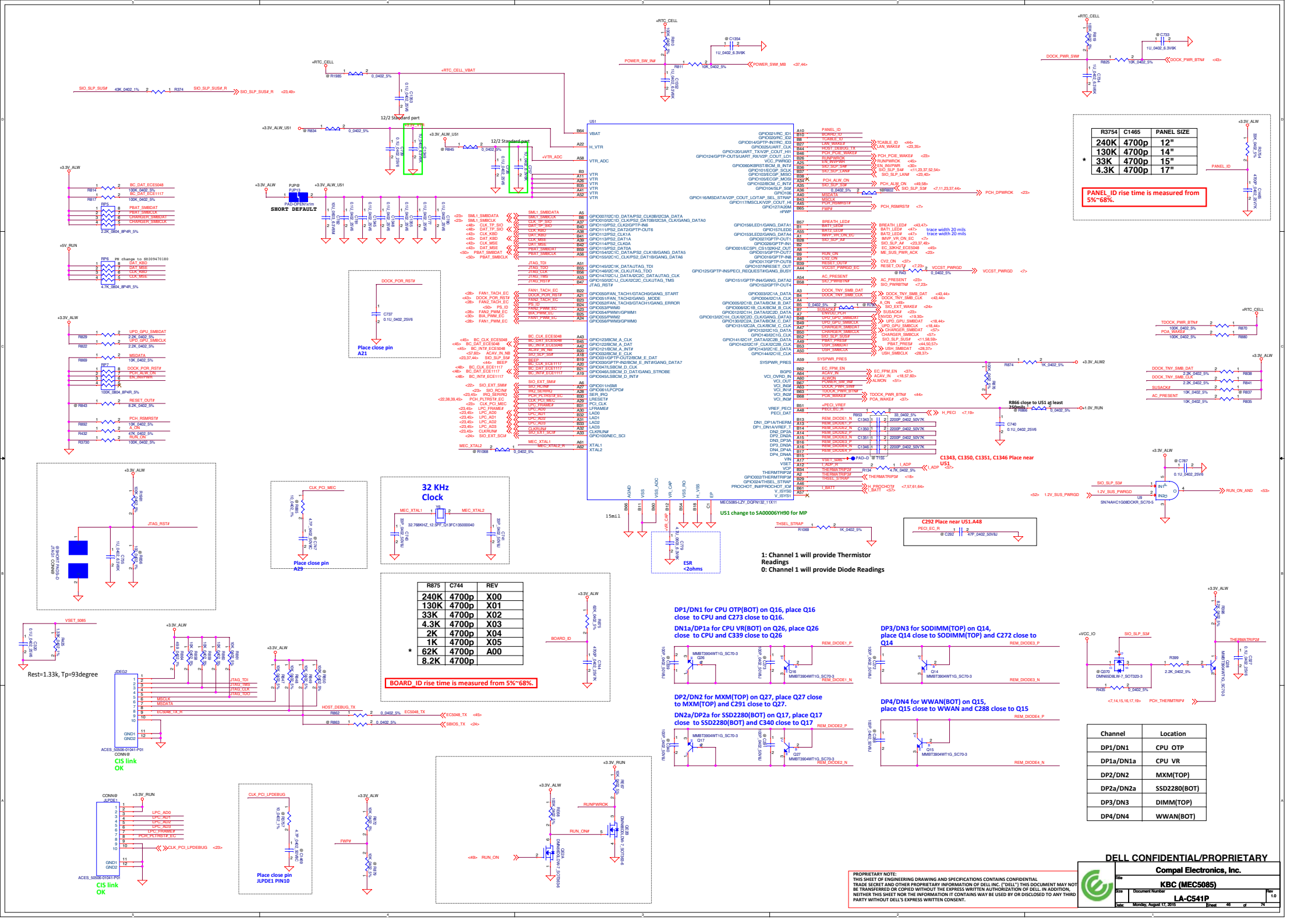
+RTC_CELL
+RTC_CELL_VBAT
SIO_SLP_SUS#
SIO_SLP_SUS#_R
12/2 Standard part
+3.3V_ALW_U51
+3.3V_ALW
+5V_RUN
SHORT DEFAULT
PJP@
PJP3
PAD-OPEN16-1in
DOCK_POR_RST#
Place close pin A21
32 KHz Clock
MEC_XTAL1
MEC_XTAL2
32.768KHZ_12.5PF_Q13FC135000040
CLK_PCI_MEC
Place close pin A29
JTAG_RST#
JTAG_TDI
JTAG_TMS
JTAG_CLK
JTAG_TDO
JDEG2
ACES_50506-01041-P01
CONN@
CIS link OK
Rest=1.33k, Tp=93degree
VSET_5085
BOARD_ID
HOST_DEBUG_TX
ECS048_TX_R
ECS048_TX
BBIOS_TX
CLK_PCI_LPDEBUG
Place close pin JLPDE1 PIN10
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
PCIR_PCI_RST1#_EC
JLPDE1
RUNPWROK
RUN_ON#
RUN_ON
FWP#
US1
MEC5085-LZY_DQFN132_11X11
US1 change to SA00006YH90 for MP
15mil
ESR <2ohms
1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings
THSEL_STRAP
C292 Place near U51.A48
PECI_EC_R
C1343, C1350, C1351, C1346 Place near U51
R866 close to US1 at least 250mils
TDOCK_PWR_BTN#
DOCK_PWR_SW#
DOCK_PWR_BTN#
PANEL_ID
R3754 C1465 PANEL SIZE
240K 4700p 12"
130K 4700p 14"
33K 4700p 15"
4.3K 4700p 17"
PANEL_ID rise time is measured from 5%~68%.
R875 C744 REV
240K 4700p X00
130K 4700p X01
33K 4700p X02
4.3K 4700p X03
2K 4700p X04
1K 4700p X05
62K 4700p A00
8.2K 4700p
BOARD_ID rise time is measured from 5%~68%.
DP1/DN1 for CPU OTP(BOT) on Q16, place Q16 close to CPU and C273 close to Q16.
DN1a/DP1a for CPU VR(BOT) on Q26, place Q26 close to CPU and C339 close to Q26
DP2/DN2 for MXM(TOP) on Q27, place Q27 close to MXM(TOP) and C291 close to Q27.
DN2a/DP2a for SSD2280(BOT) on Q17, place Q17 close to SSD2280(BOT) and C340 close to Q17
DP3/DN3 for SODIMM(TOP) on Q14, place Q14 close to SODIMM(TOP) and C272 close to Q14
DP4/DN4 for WWAN(BOT) on Q15, place Q15 close to WWAN and C288 close to Q15
Channel Location
DP1/DN1 CPU OTP
DP1a/DN1a CPU VR
DP2/DN2 MXM(TOP)
DP2a/DN2a SSD2280(BOT)
DP3/DN3 DIMM(TOP)
DP4/DN4 WWAN(BOT)
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Compal Electronics, Inc.
KBC (MEC5085)
LA-C541P
Monday, August 17, 2015
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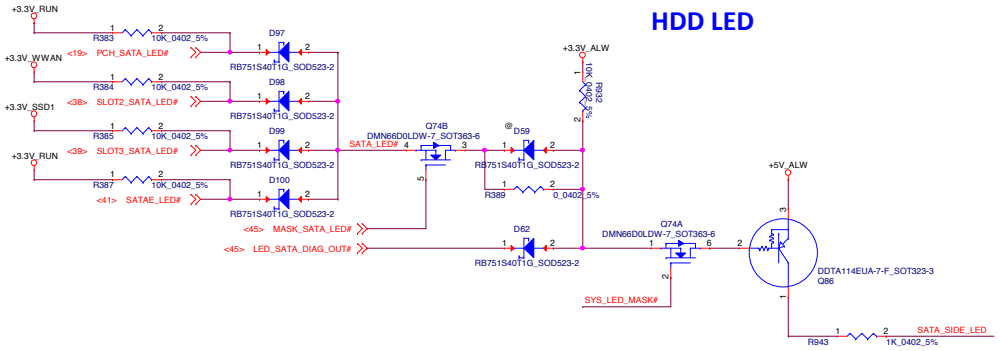
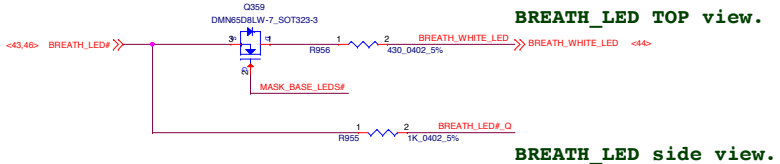
HDD LED



Breath LED

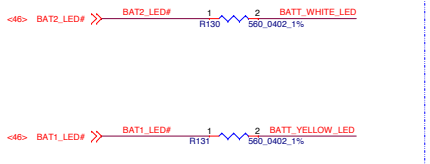


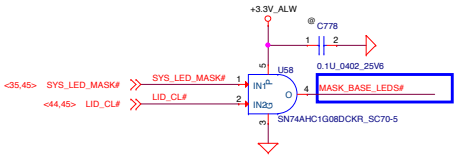
BREATH_LED TOP view.

BREATH_LED side view.

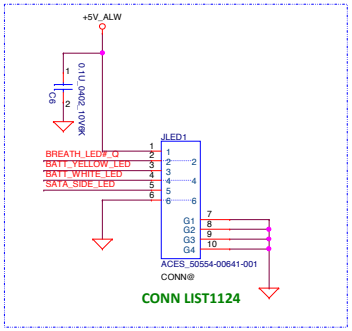
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

BATT LED



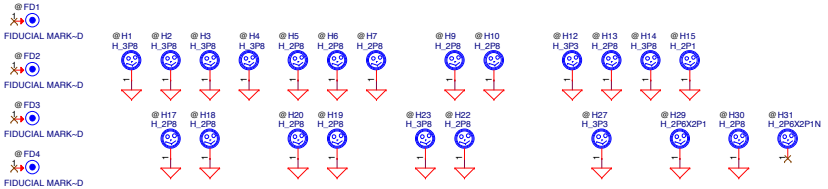


To LED/B Conn



CONN LIST1124

Fiducial Mark



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Compal Electronics, Inc.			
Title: LED / Screw hole			
Size	Document Number: LA-C541P		Rev: 1.0
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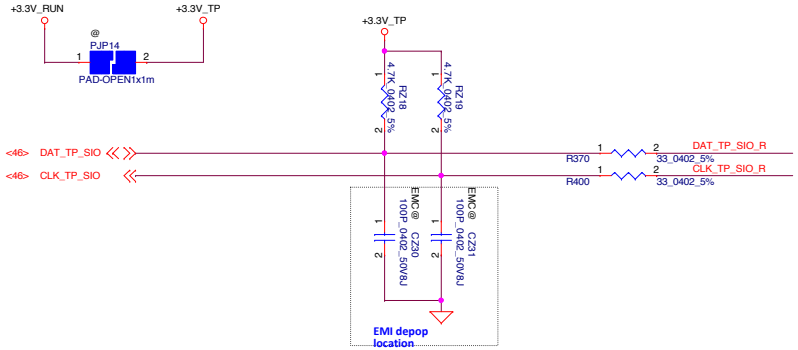
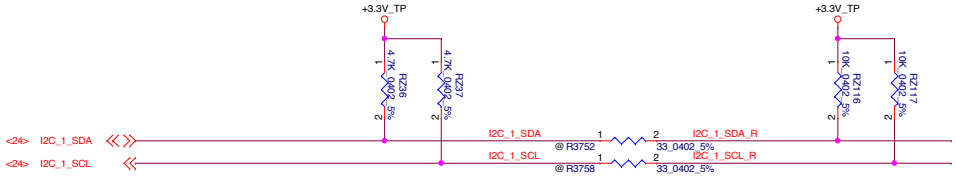
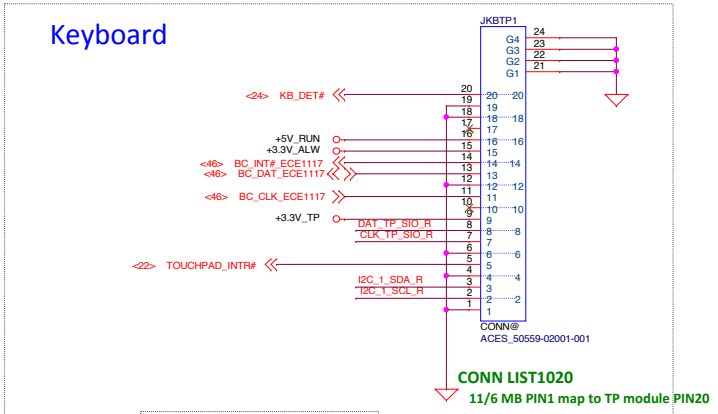
Touch Pad





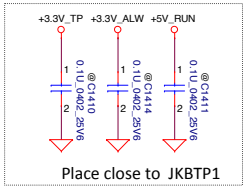
pop R3752,R3758 and depop RZ36,RZ37 when use I2C_TP

Keyboard



CONN LIST1020

11/6 MB PIN1 map to TP module PIN20



Place close to JKBTP1

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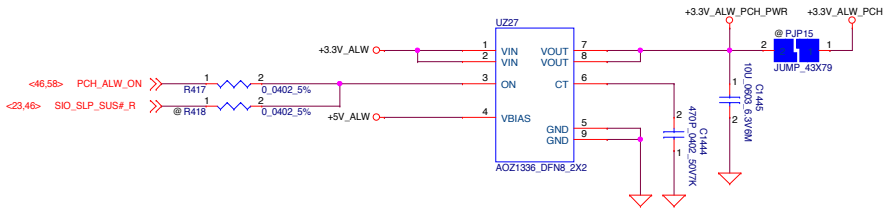
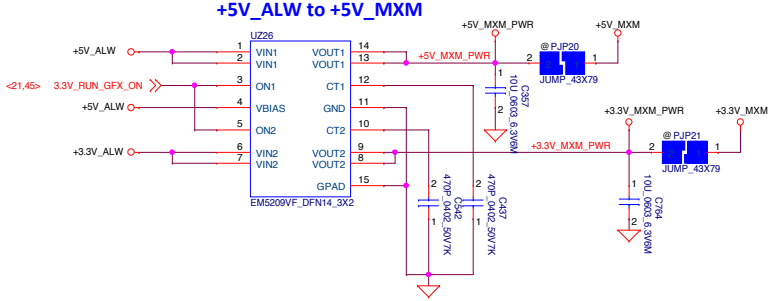
Compal Electronics, Inc.		
Title: KB / TP		
Size	Document Number: LA-C541P	Rev: 1.0
Date: Monday, August 17, 2015	Sheet 48 of 74	

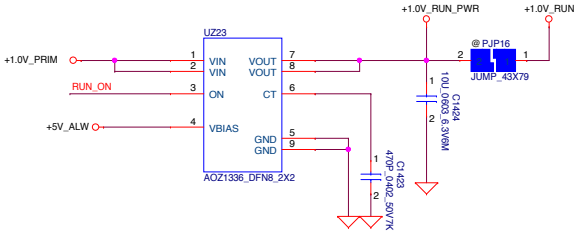
+3.3V_ALW_PCH Source



+3.3V_ALW to +3.3V_MXM
+5V_ALW to +5V_MXM

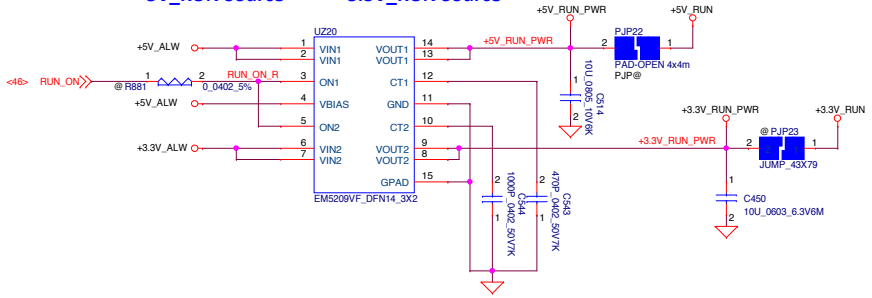


+1.0V_PRIM to +1.0V_RUN

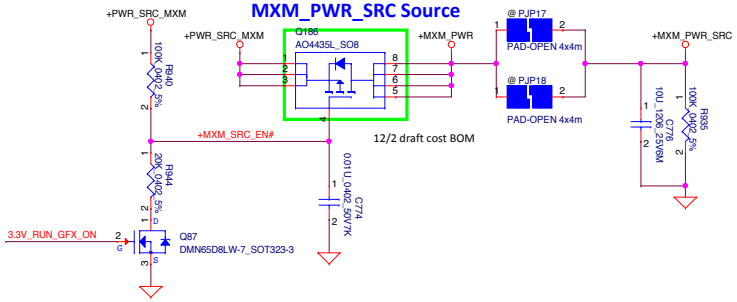


+5V_RUN Source

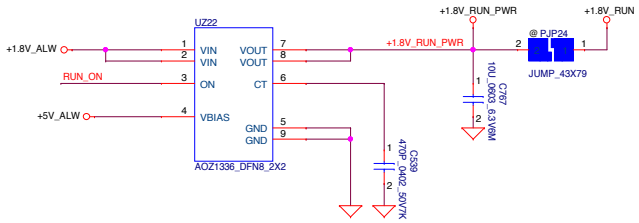
+3.3V_RUN Source



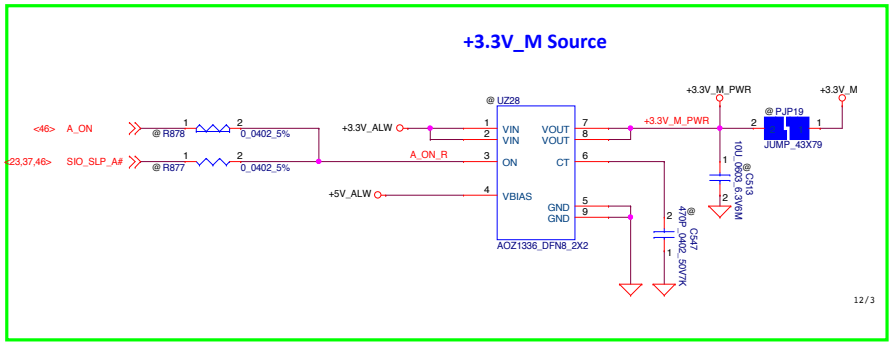
MXM_PWR_SRC Source



+1.8V_RUN Source



+3.3V_M Source



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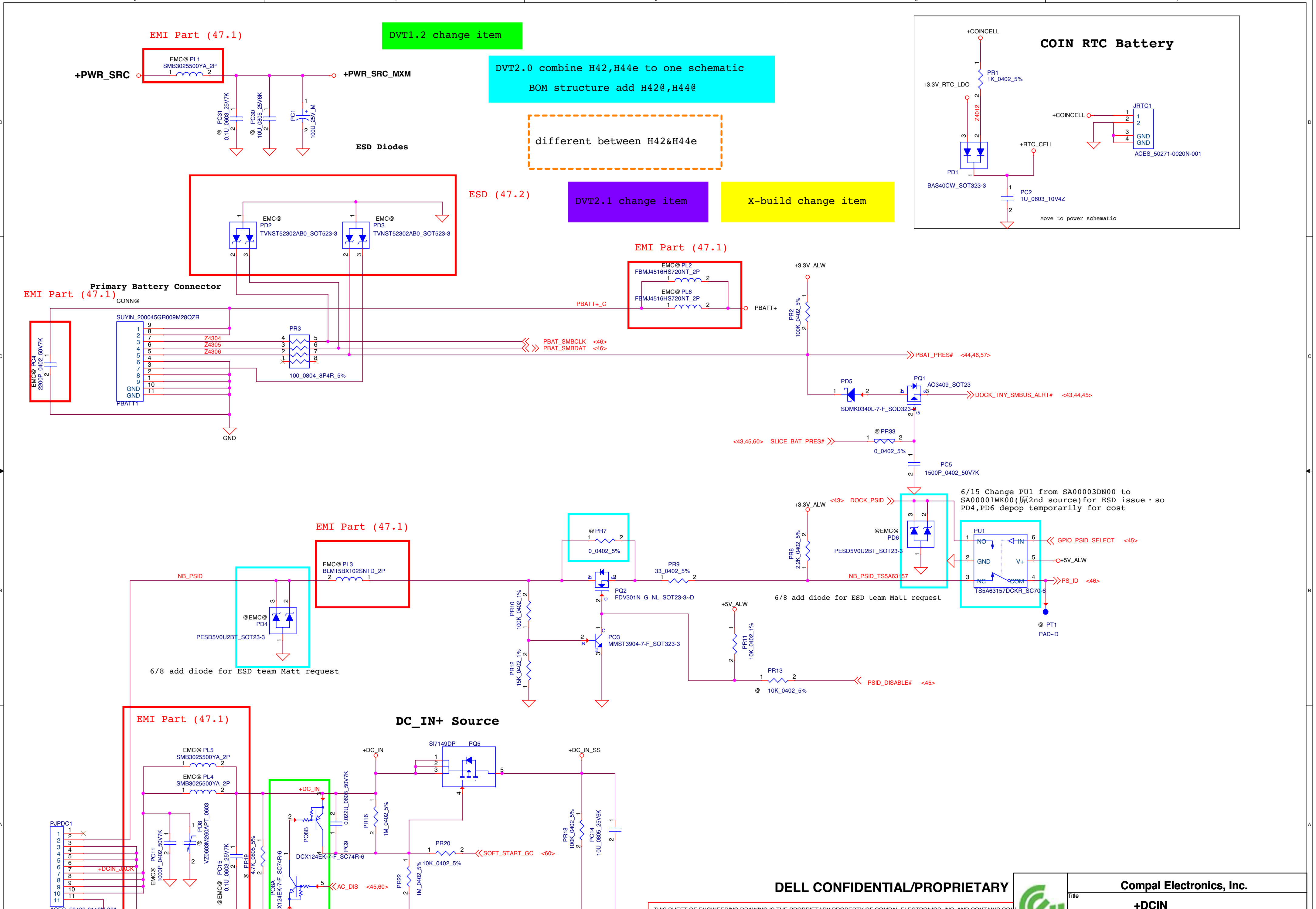
Compal Electronics, Inc.			
Title: Power Control			
Size	Document Number: LA-C541P		Rev: 1.0
Date: Monday, August 17, 2015	Sheet 49 of 74		



EMI Part (47.1)
DVT1.2 change item
DVT2.0 combine H42,H44e to one schematic
BOM structure add H42@,H44@
different between H42&H44e
DVT2.1 change item
X-build change item
COIN RTC Battery
+COINCELL
PR1
1K_0402_5%
+3.3V_RTC_LDO
Z4012
+RTC_CELL
JRTC1
GND
ACES_50271-0020N-001
PD1
BAS40CW_SOT323-3
PC2
1U_0603_10V4Z
Move to power schematic
EMC@ PL1
SMB3025500YA_2P
+PWR_SRC
+PWR_SRC_MXM
PC31
0.1U_0603_25V7K
PC30
10U_0805_25V6K
PC1
100U_25V_M
ESD Diodes
ESD (47.2)
EMC@
PD2
TVNST52302AB0_SOT523-3
EMC@
PD3
TVNST52302AB0_SOT523-3
EMI Part (47.1)
EMC@ PL2
FBMJ4516HS720NT_2P
EMC@ PL6
FBMJ4516HS720NT_2P
PBATT+_C
PBATT+
+3.3V_ALW
PR2
100K_0402_5%
Primary Battery Connector
EMI Part (47.1)
CONN@
SUYIN_200045GR009M28QZR
EMC@ PC4
2200P_0402_50V7K
PBATT1
Z4304
Z4305
Z4306
PR3
100_0804_8P4R_5%
PBAT_SMBCLK <46>
PBAT_SMBDAT <46>
PBAT_PRES# <44,46,57>
GND
PD5
SDMK0340L-7-F_SOD323-2
PQ1
AO3409_SOT23
DOCK_TNY_SMBUS_ALRT# <43,44,45>
<43,45,60> SLICE_BAT_PRES#
@ PR33
0_0402_5%
PC5
1500P_0402_50V7K
6/15 Change PU1 from SA00003DN00 to SA00001WK00(原2nd source)for ESD issue，so PD4,PD6 depop temporarily for cost
+3.3V_ALW
<43> DOCK_PSID
@EMC@
PD6
PESD5V0U2BT_SOT23-3
PR8
2.2K_0402_5%
PU1
NO
IN
GND
V+
NC
COM
TS5A63157DCKR_SC70-6
GPIO_PSID_SELECT <45>
+5V_ALW
PS_ID <46>
@ PT1
PAD~D
NB_PSID_TS5A63157
6/8 add diode for ESD team Matt request
EMI Part (47.1)
EMC@ PL3
BLM15BX102SN1D_2P
NB_PSID
@EMC@
PD4
PESD5V0U2BT_SOT23-3
6/8 add diode for ESD team Matt request
@ PR7
0_0402_5%
PR9
33_0402_5%
PQ2
FDV301N_G_NL_SOT23-3~D
PR10
100K_0402_1%
PR12
15K_0402_1%
PQ3
MMST3904-7-F_SOT323-3
+5V_ALW
PR11
10K_0402_1%
PR13
10K_0402_5%
PSID_DISABLE# <45>
EMI Part (47.1)
DC_IN+ Source
EMC@ PL5
SMB3025500YA_2P
EMC@ PL4
SMB3025500YA_2P
PJPDC1
ACES_50493-0110N-001
CONN@
+DCIN_JACK
EMC@ PC11
1000P_0402_50V7K
PD8
VZ0603M260APT_0603
@EMC@ PC15
0.1U_0603_25V7K
@ PR19
4.7K_0805_5%
PQ8A
DCX124EK-7-F_SC74R-6
PQ8B
DCX124EK-7-F_SC74R-6
+DC_IN
PC9
0.022U_0603_50V7K
+DC_IN
PR16
1M_0402_5%
SI7149DP
PQ5
PR20
10K_0402_5%
SOFT_START_GC <60>
PR22
1M_0402_5%
AC_DIS <45,60>
+DC_IN_SS
PR18
100K_0402_5%
PC14
10U_0805_25V6K
4/29 PQ8 SB000009N00 is X1 code ,replaced to second source SB000009P80

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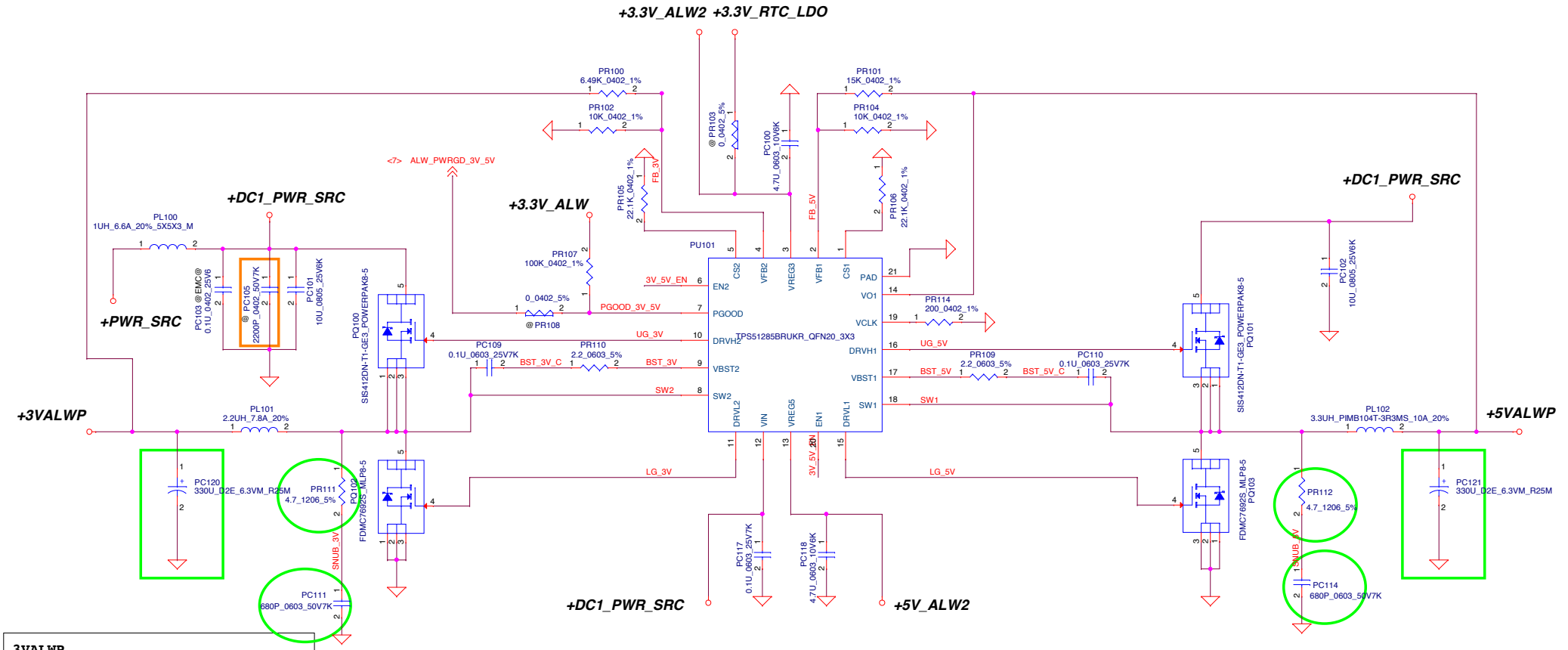
Compal Electronics, Inc.

Title: +DCIN

Size | Document Number: LA-C541P | Rev 1.0

Date: Monday, August 17, 2015



3VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 355kHz
TDC 7.35 A
Peak Current 10.5 A
OCP current 12.6 A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	10.8mohm ,	13.6mohm

Choke DCR:15m ohm(MAX)
Bulk cap ESR 25mohm

5VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 300kHz
TDC 7.8 A
Peak Current 11.15 A
OCP current 13.38 A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	10.8mohm ,	13.6mohm

Choke DCR Max:11.8mohm
Choke Ityp:10A / Isat:16A
Bulk cap ESR 25mohm

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Compal Electronics, Inc.	
Title	+5V_ALW/3.3V_ALW
Size	Document Number: LA-C541P
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Date:	Monday, August 17, 2015
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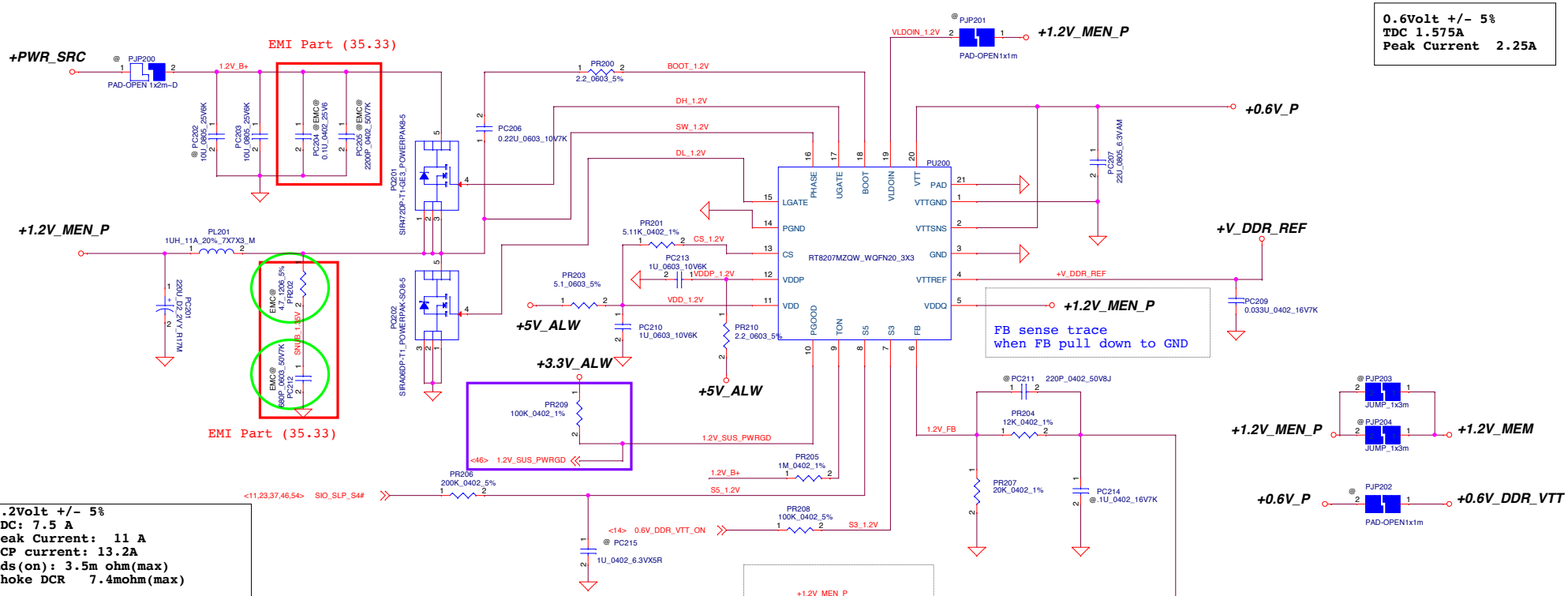

1.2Volt +/- 5%
TDC: 7.5 A
Peak Current: 11 A
OCP current: 13.2A
Rds(on): 3.5m ohm(max)
Choke DCR 7.4mohm(max)

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

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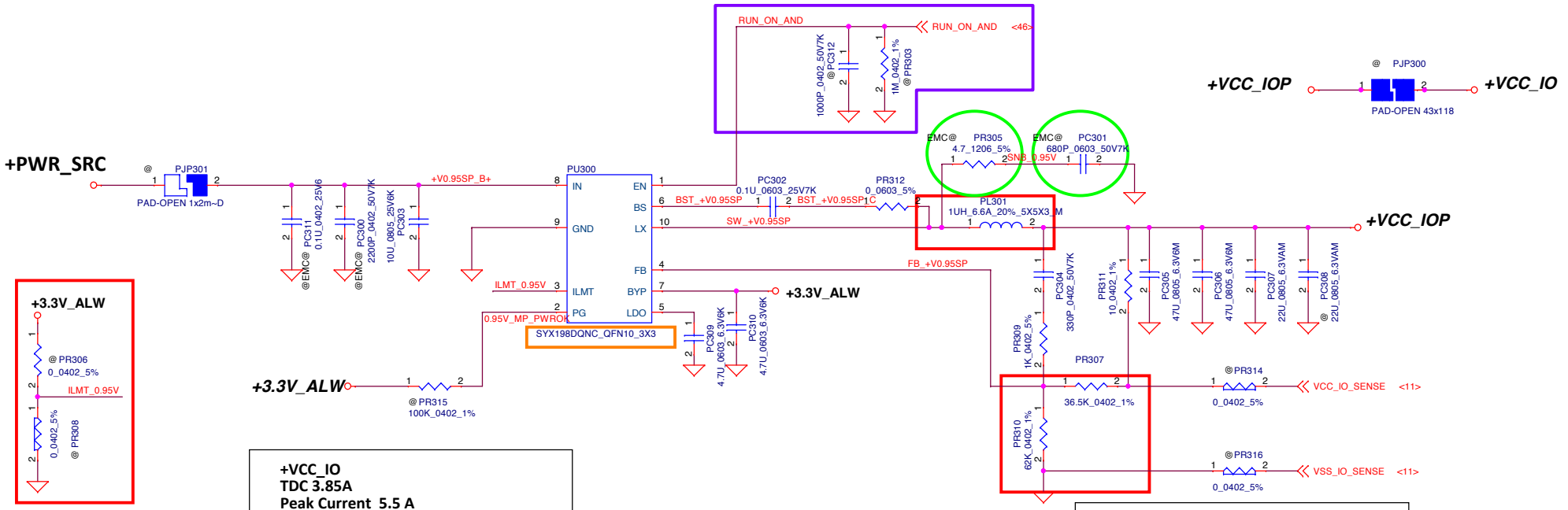
Compal Electronics, Inc.

Title	1.2VP/0.6VSP	
Size	Document Number: LA-C551P	Rev: 1.0
Date: Monday, August 17, 2015	Sheet 52 of 74	



+VCC_IO
TDC 3.85A
Peak Current 5.5 A
OCP Current 8 A

	TYP	MAX
Choke DCR	13.0mohm ,	14.0mohm

proximal
PR311 0 ohm PR314 10 ohm PR316 10 ohm

remote
PR311 10 ohm PR314 0 ohm PR316 0 ohm

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Title	+VCC_IO 0.95V
Size	Document Number: LA-C541P
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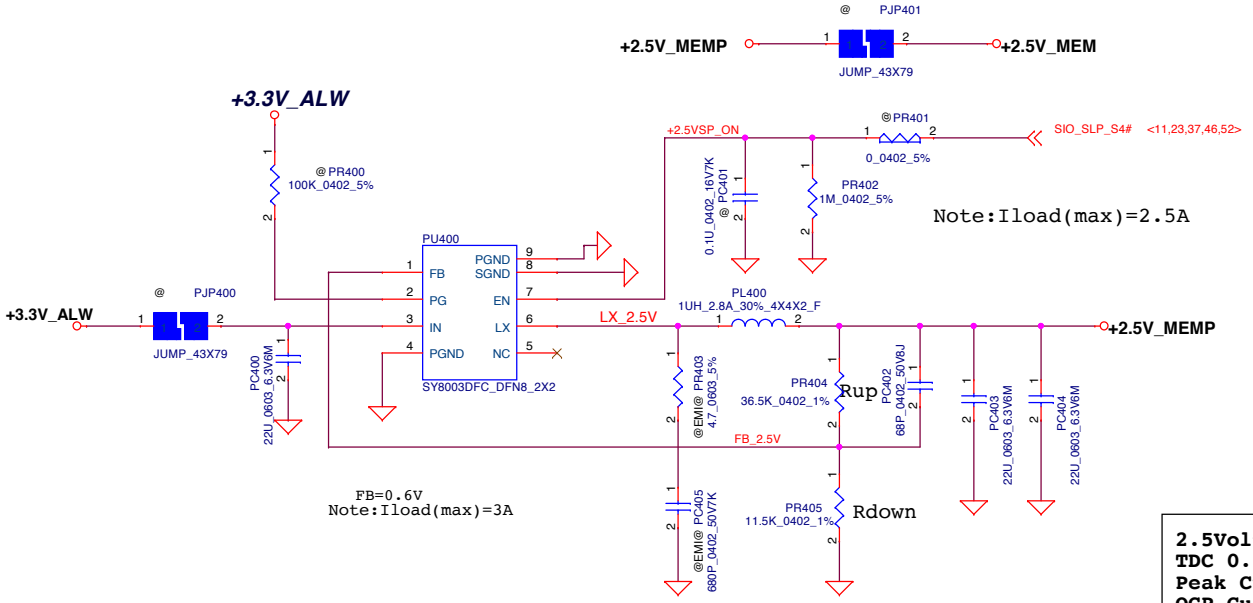

2.5Volt
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

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Compal Electronics, Inc.		
Title: +2.5V_MEM		
Size	Document Number: LA-C541P	Rev: 1.0
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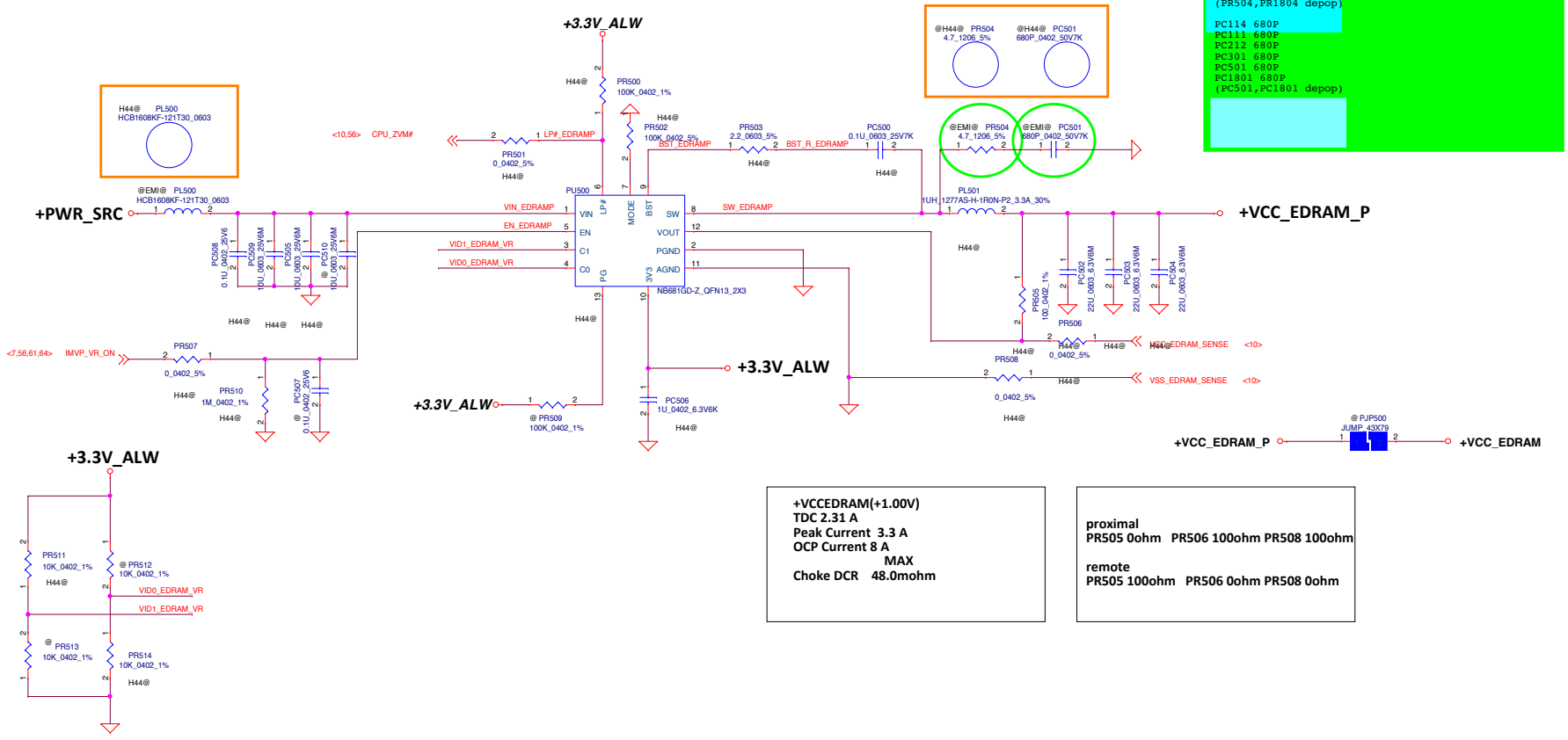
Only H44e

6/17 depop modify (5/27 RF team Brian suggest to pop)
PR112-4.7
PR111-4.7
PR202-4.7
PR305-4.7
PR504-4.7
PR1804-4.7
(PR504,PR1804 depop)

PC114 680P
PC111 680P
PC212 680P
PC301 680P
PC501 680P
PC1801 680P
(PC501,PC1801 depop)



+VCCEDRAM(+1.00V)
TDC 2.31 A
Peak Current 3.3 A
OCP Current 8 A
MAX
Choke DCR 48.0mohm

proximal
PR505 0ohm PR506 100ohm PR508 100ohm

remote
PR505 100ohm PR506 0ohm PR508 0ohm

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Compal Electronics, Inc.

Title: +VCCEDRAM, 1V

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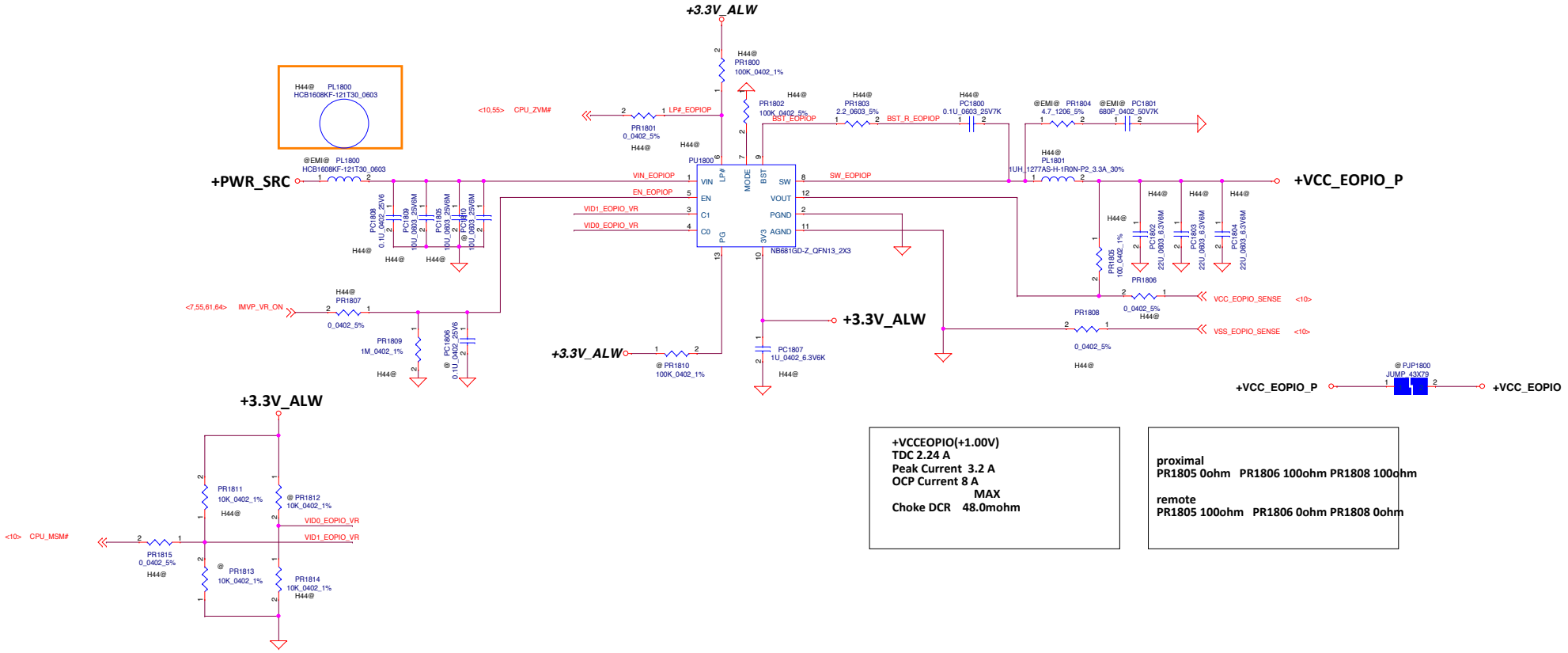
Date: Monday, August 17, 2015 | Sheet 55 of 74

Only H44e



+VCCEOPIO(+1.00V)
TDC 2.24 A
Peak Current 3.2 A
OCP Current 8 A
MAX
Choke DCR 48.0mohm

proximal
PR1805 0ohm PR1806 100ohm PR1808 100ohm

remote
PR1805 100ohm PR1806 0ohm PR1808 0ohm

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Compal Electronics, Inc.

Title: +VCCEOPIO, 1V

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Iada=0~9.23A(180W)

ADP_I = 40*Iadapter*Rsense

Current limit
Charger :7.8A Vilim=1.56V
6 Cell (0.8C)
Max Boost Charger :7.8A, Vilim=0.39V

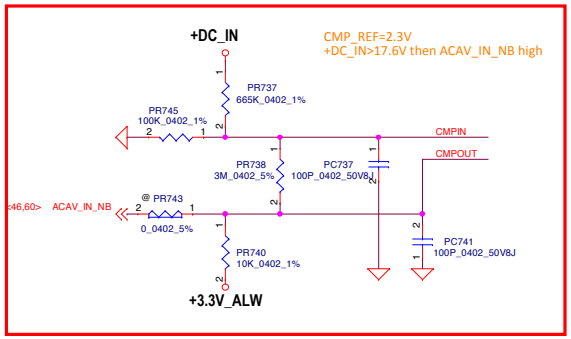
AC Det (typ 2.4V)
Max:16.994V
Typ :16.540V
Min :16.098V

EMI Part (47.1)

EMI Part (47.1)

EMI Part (35.33)

5/14 change the circuit for bettary current sense



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Title	PWR_Charger
Size	Document Number: LA-C541P
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Date:	Monday, August 17, 2015
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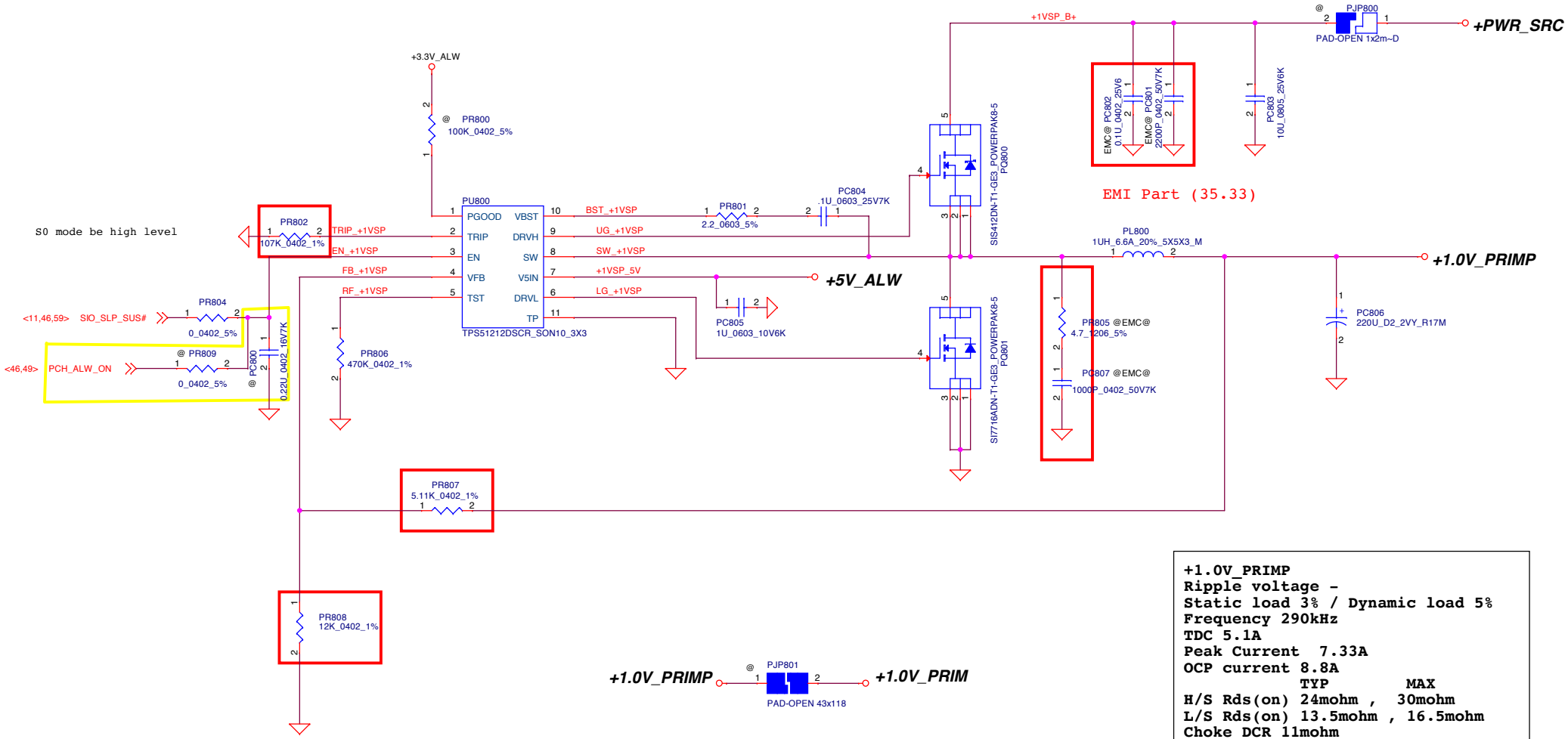

+1.0V_PRIMP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 5.1A
Peak Current 7.33A
OCP current 8.8A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	13.5mohm ,	16.5mohm

Choke DCR 11mohm
Bulk cap ESR 17mohm

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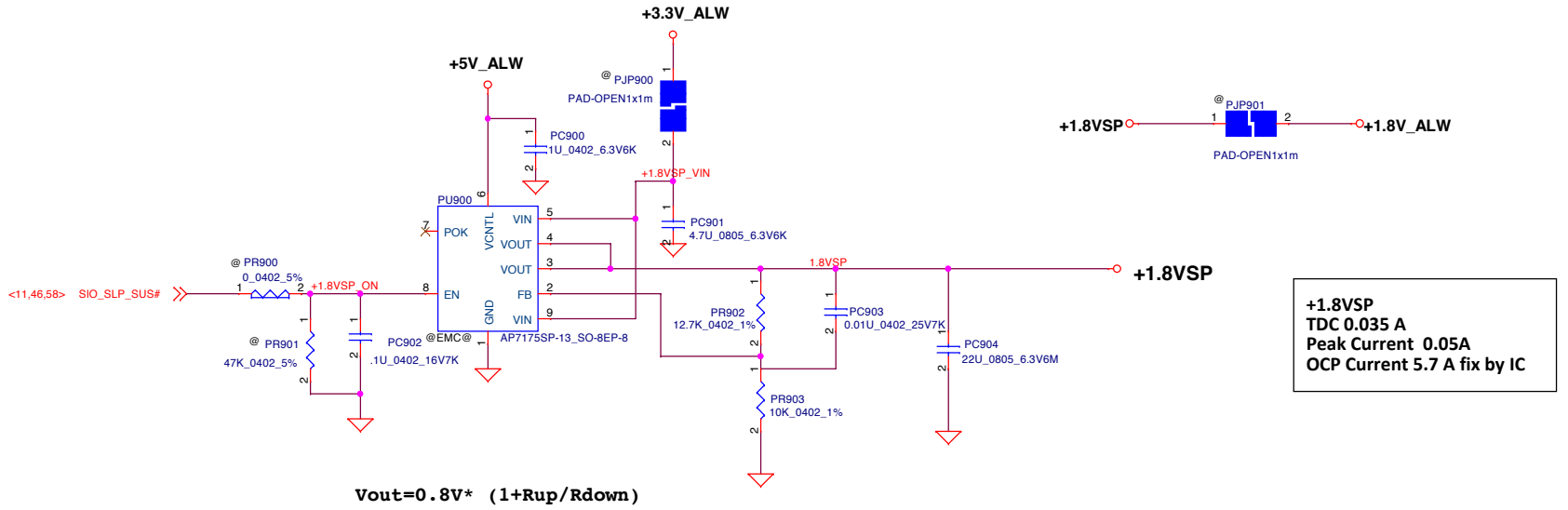
Compal Electronics, Inc.

Title	+1.0V_PRIM	
Size	Document Number LA-C541P	Rev 1.0
Date: Monday, August 17, 2015	Sheet 58 of 74	



+1.8VSP
TDC 0.035 A
Peak Current 0.05A
OCP Current 5.7 A fix by IC

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Compal Electronics, Inc.		
Title: +1.8V_ALW		
Size	Document Number: LA-C541P	Rev: 1.0
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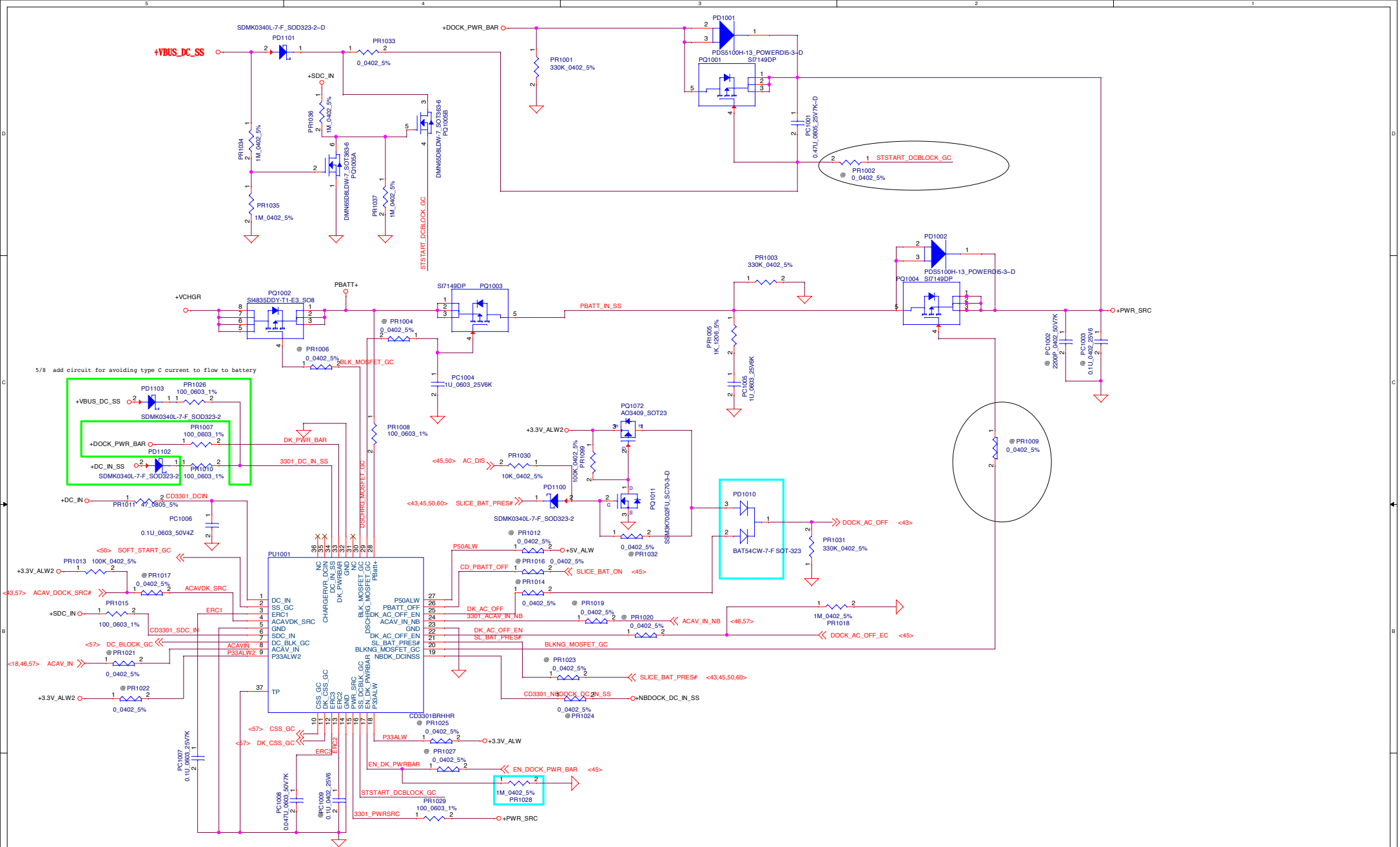

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Compal Electronics, Inc.

Title: Selector

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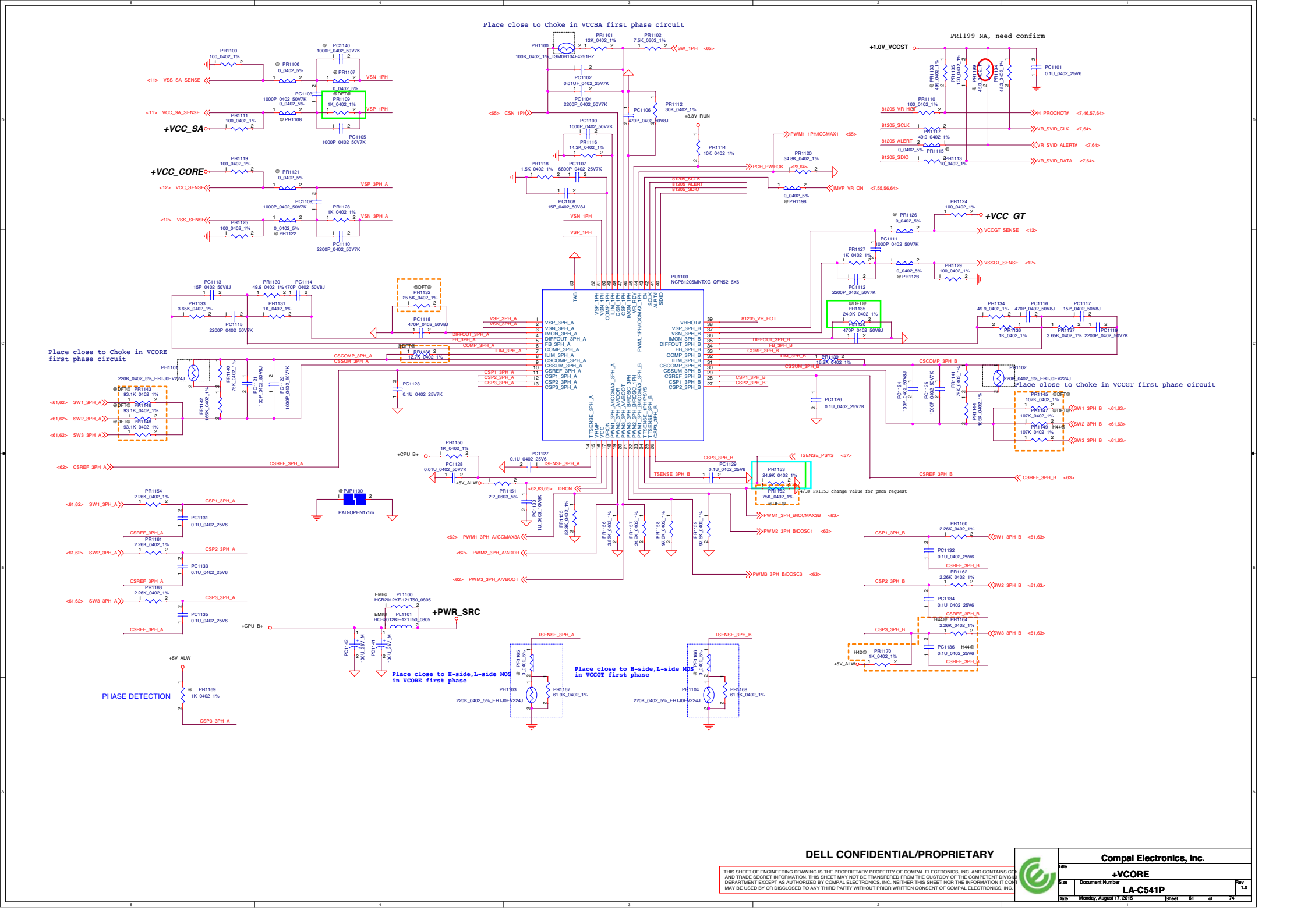
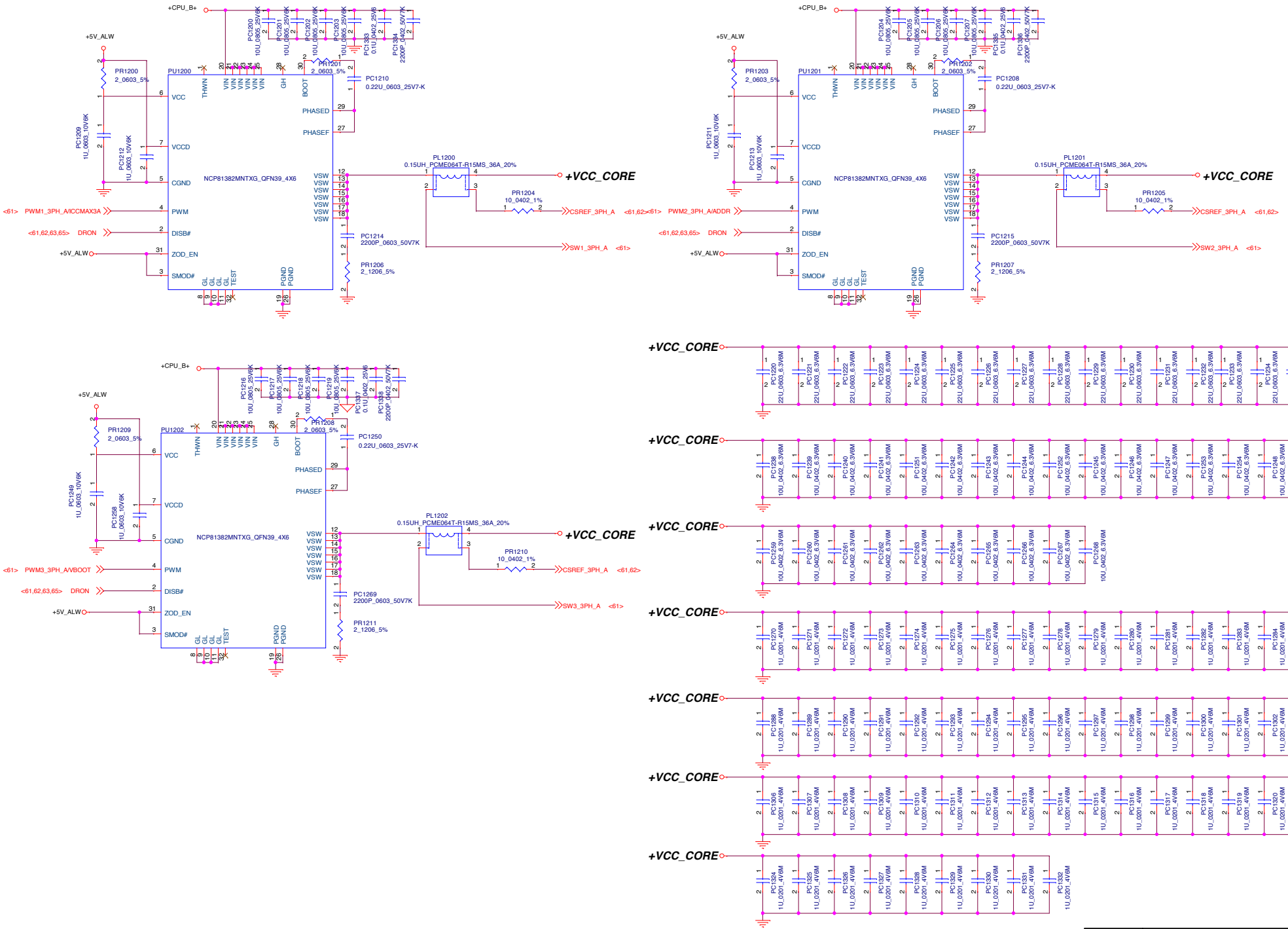

Place close to Choke in VCCSA first phase circuit
PR1199 NA, need confirm
+VCC_SA
+VCC_CORE
+VCC_GT
+1.0V_VCCST
PU1100
NCP81205MNTXG_QFN52_6X6
Place close to Choke in VCORE first phase circuit
Place close to Choke in VCCGT first phase circuit
+PWR_SRC
PHASE DETECTION
Place close to H-side,L-side MOS in VCORE first phase
Place close to H-side,L-side MOS in VCCGT first phase
PR1153 change value for pmon request
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
+VCORE
LA-C541P
Monday, August 17, 2015



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Compal Electronics, Inc.

Title: +VCC_CORE

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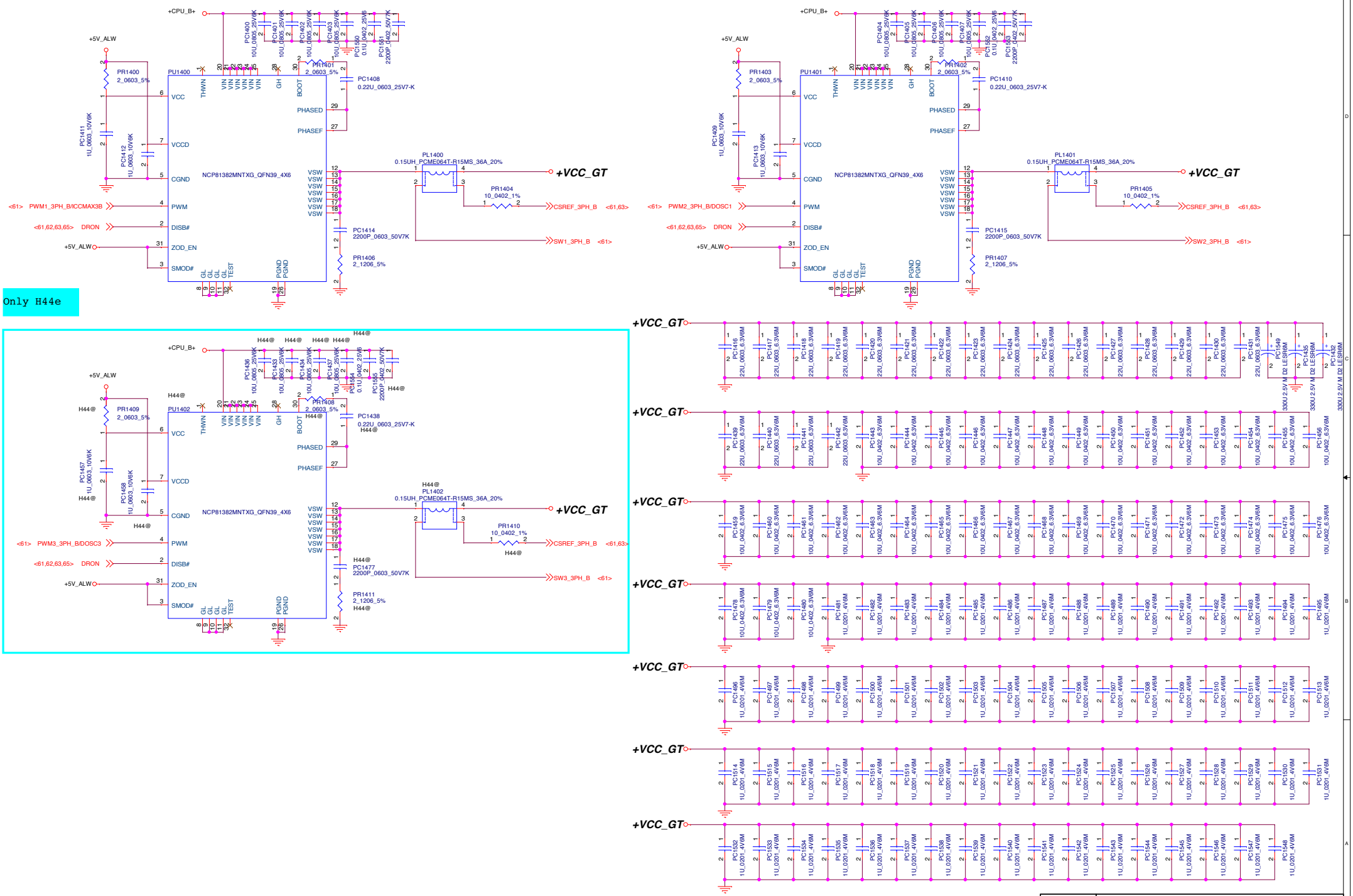

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Compal Electronics, Inc.	
Title	+VCC_GT
Size	Document Number: LA-C541P
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Date:	Monday, August 17, 2015
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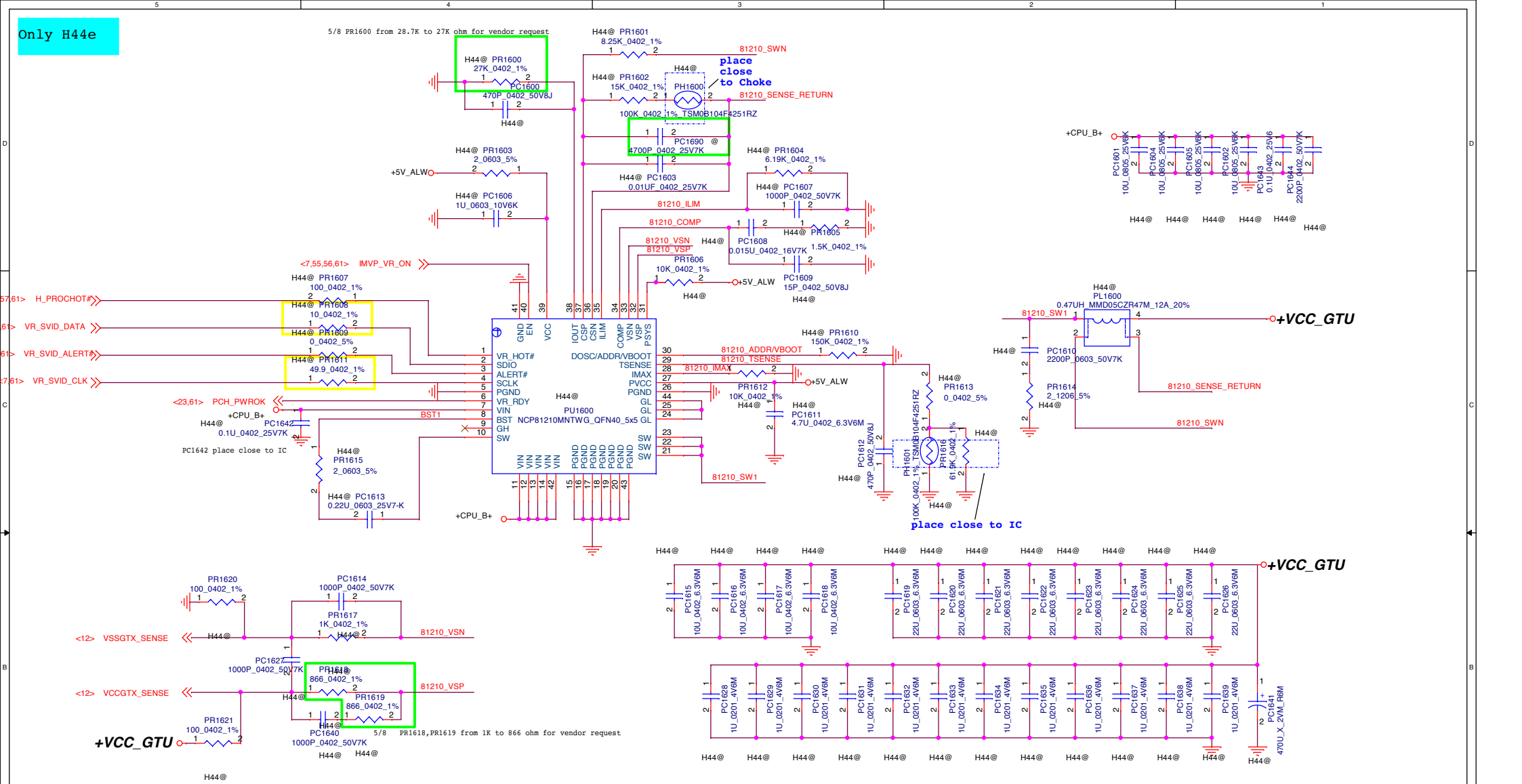

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Compal Electronics, Inc.	
Title	+VCC_GTX
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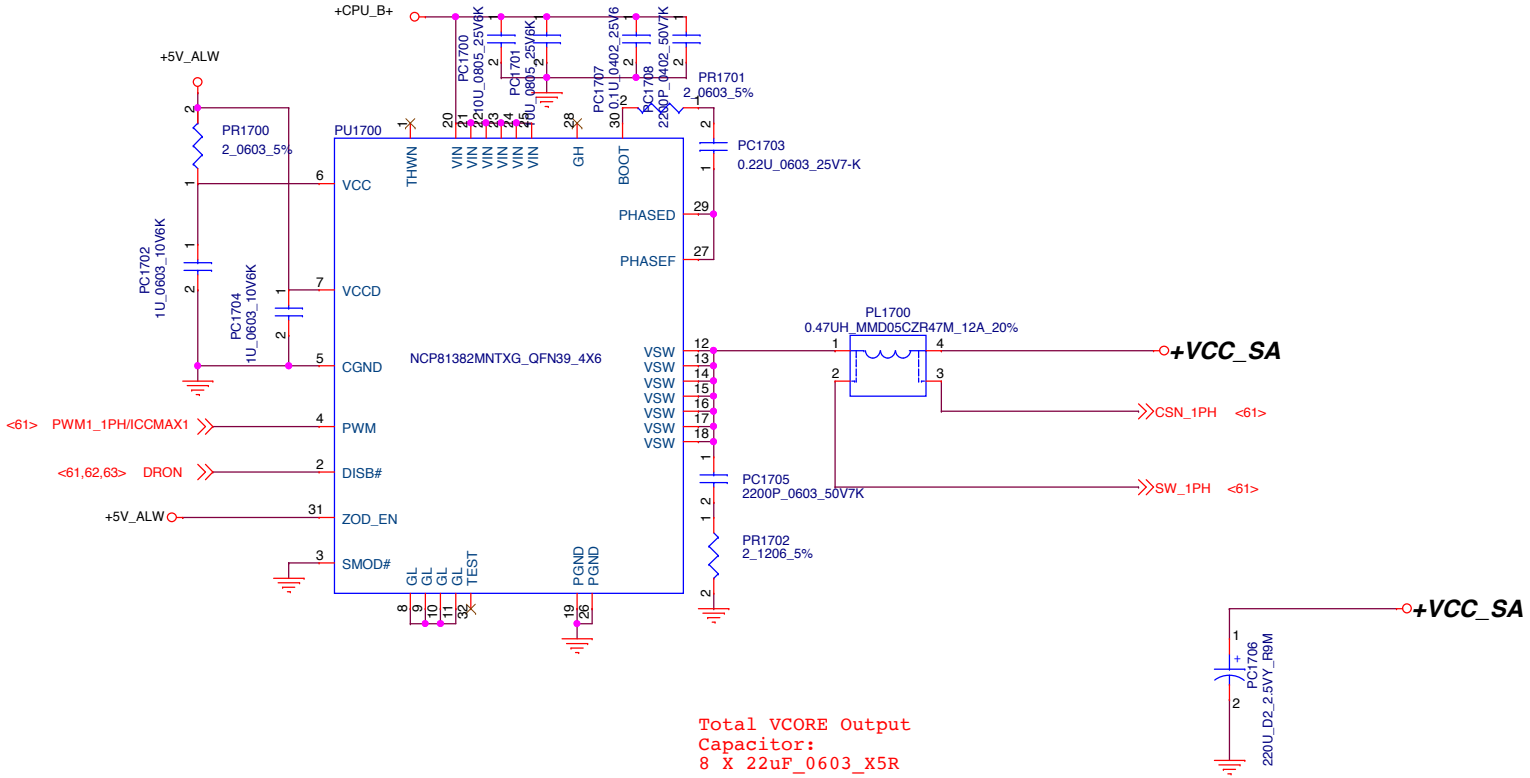
InputCapacitor:
10uF_0805_X5R_25V



Total VCORE Output
Capacitor:
8 X 22uF_0603_X5R

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Compal Electronics, Inc.

Title: +VCC_SA

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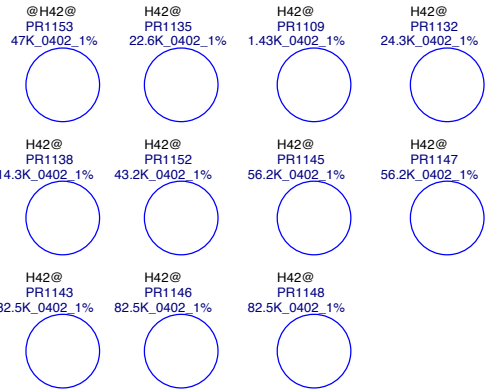
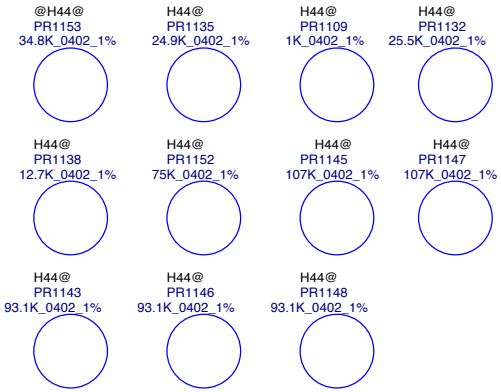
C541_H42 component



C541_H44e component



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Compal Electronics, Inc.

Title: PWR_table

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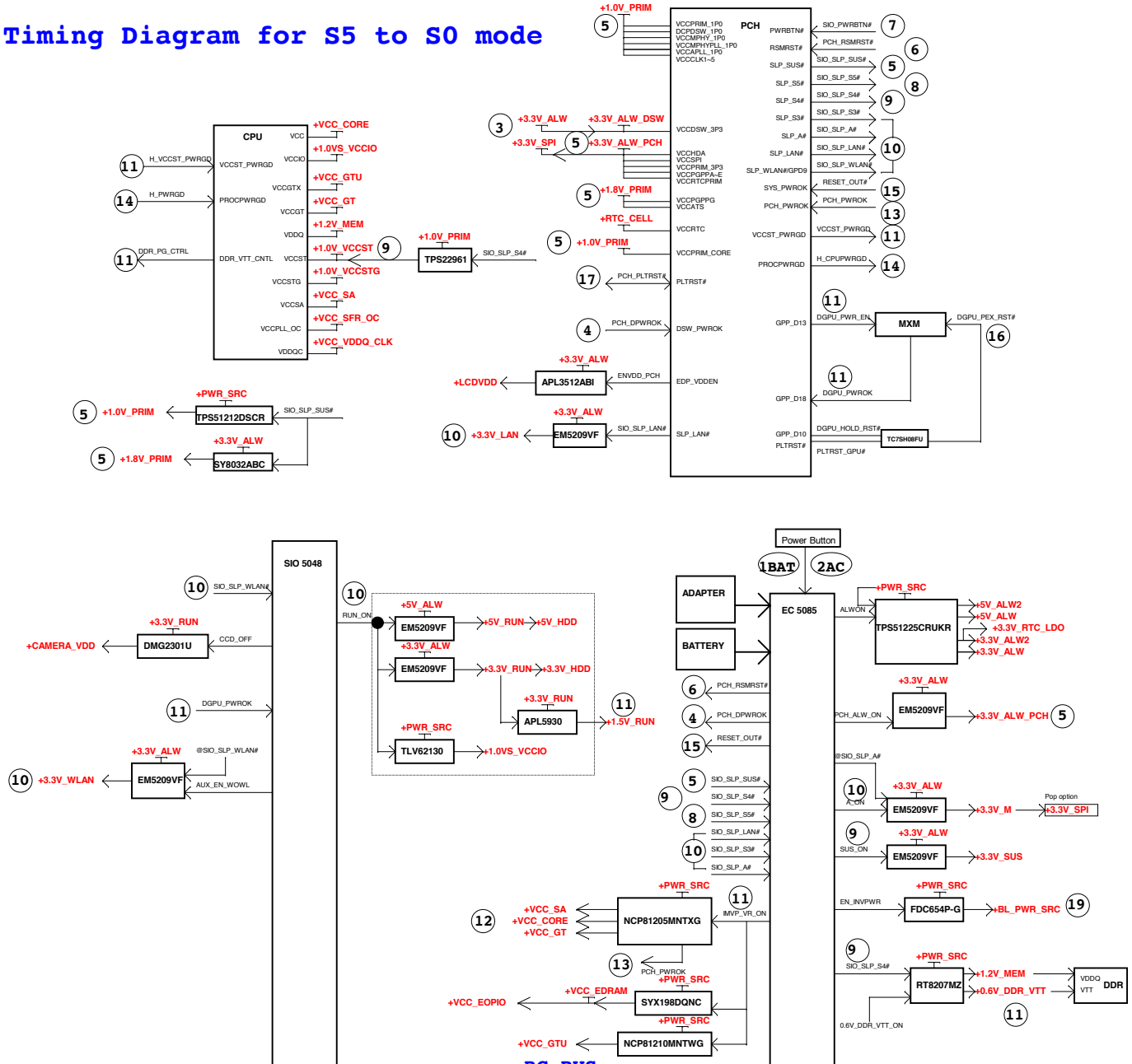
Timing Diagram for S5 to S0 mode



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Compal Electronics, Inc.

Power Sequence

LA-C541P

Monday, August 17, 2015

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	22,37,49	HW	12/6/2014	compal	reserve SPI and TPM PWR rail optional +3.3V_ALW_PCH or +3.3V_M.	Add RH343,RH344,RZ75,depop UZ28,C547,C513 for SPI and TPM PWR rail change to +3.3V_ALW_PCH,add @RH348 to +3.3V_M power rail option for +3.3V_1.8V_SPI.	X01(0.2)
2	37,46	HW	12/6/2014	compal	GPIO MAP:Gen7_GPIO1211	U51.B62 change netname from POA_EN to EC_FPM_EN and U51.A9 change netname from SUS_ON to CV2_ON for follow GPIO MAP	X01(0.2)
3	41	HW	12/6/2014	compal	correct U6 PWR rail to map U6 input level.	U6.5 PWR change from +3.3V_HDD to +1.0V_RUN for U6 input signal is 1.4V level.	X01(0.2)
4	45	HW	12/6/2014	compal	Avoid backdrive to +3.3V_RUN.	R3740.2(UPD_SMBUS_ALERT#) PWR rail change from +3.3V_RUN to +3.3V_ALW.	X01(0.2)
5	48	HW	12/6/2014	compal	TP I2C interface reserve 0ohm	add R3752,R3758	X01(0.2)
6	28,35	HW	12/9/2014	compal	symbol link CIS normal CPN	update U8 symbol for SA00007ZW00,update U31 symbol for SA000081G0L	X01(0.2)
7	24	HW	12/9/2014	AMD	aviod incorrect behavior when system w/AMD MXM cards	Reserve a pull up 10k(RH345) to +3.3V_ALW_PCH close to PCH side on GPU_EVENT#	X01(0.2)
8	24	HW	12/10/2014	compal	FAN control SMBUS connect error	AAC_SMBCLK change to connect U8.20,AAC_SMBDAT change to connect U8.21 change U8.43 connect R371 then connect LED to GND	X01(0.2)
9	25,30	HW	12/10/2014	compal	add "+" on PWR trace netname and others no "+"	add netname +DCPRTC on CH68.1,change netname +3.3V_CAM_EN# to 3.3V_CAM_EN#	X01(0.2)
10	38	HW	12/10/2014	compal	symbol CPN and Value not match.	change C1176,C1402 PN to SGA00002B00,and depop C1402	X01(0.2)
11	41	HW	12/11/2014	compal	double PU	remove @R3754	X01(0.2)
12	30	HW	12/11/2014	compal	align BC change Q24 main source	change Q24 to SB00000QP00	X01(0.2)
13	23	HW	12/15/2014	RF	RF request	change CH268 from 0.01uF to 22pF	X01(0.2)
14	45,46	HW	12/17/2014	compal	Gen7_GPIO1211	remove R851,R852,R853,R854,change netname CPU_ID to GPIOL0,U51.A40 to MSDATA,U51.B43 to MSCLK,U51.B46 to PCH_PCIE_WAKE#,U46.A64 to ME_FW_EC,U46.A8 to USB_PWR_SHR_LFT_EN#	X01(0.2)
15	19,42,41	HW	12/19/2014	compal	SATA express HDD function issue-PCIE13-16 lane reverse	SATA express interface change to PCIE14(match HDD port1),PCIE13(match HDD port0),UH1.AG39 change to HDD_DET#,UH1.AD35 to SATA_EXP_IFDET.	X01(0.2)
16	46	HW	12/23/2014	compal	reserve for next-gen EC that use the Intel chipset UART TXD for the SBIOS Serouts	add R862,R863,change netname GPP_C9 to SBIOS_TX	X01(0.2)
17	46	HW	12/29/2014	compal	SB339045100 EOL	change Q28 to SB000008P00	X01(0.2)
18	22	HW	12/30/2014	compal	solve TPM PLTRST leakage	add RH346 and depop RH187,RH196, change U638.5 to_3.3V_ALW_PCH	X01(0.2)
19	6,39,35, 47,22,7,36	HW	12/30/2014	compal	same Value a CPN on Board	PEG 0.22UF AC CAP(CC1-CC64) and SSD 0.22UF AC CAP(CN83,CN85-CN88,CN91,CN92,CN95,CN97)change from SE00000R700 to SE095224K00 U15,U58,U638,UC4 change from SA007080120 to SA007080180 Q327 change from SB00000ST00 to SB00000U000 T156 change from SP050006P00 to SP050006Y00	X01(0.2)
20	21	HW	12/30/2014	compal	DG1.0 RTC Crystal MAX ESR is 50Kohm	YH1 change to SJ10000LV00	X01(0.2)
21	42	HW	12/30/2014	compal	HDD SATA/PCIE repeater change to GEN3 chip	UN8,UN9 change from PS8555 to PS8558(SA00008DT00),CN75,CN71 change to 0.01uF,CN70,CN63,CN69,CN76,CN64,CN72,CN79,CN65,CN74,CN80,CN66,CN81 change to 0.22uF,remove CN77,CN68,CN82,CN78,add RH99-RH111,RH114-RH130	X01(0.2)
22	23	HW	12/31/2014	compal	MOW Rev1.0-To enable Direct Connect Interface (DCI),a 150K pull up resistor will need to be added to PCHHOT# pin.	RH329 change to 150kohm(SD028150380) and pop it,reserve RH347 pull up to +3.3V_RUN,add RH353,@QH5	X01(0.2)
23	37	HW	01/05/2015	compal	System will shut down as soon as system power on with FPM and RFID/NFC testing result is failed	add DZ3,RZ76,RZ72,RZ73.change JUSH1.9 from +5V_ALW2 to +5V_ALW, JUSH1.10 from +3.3V_ALW2 to +5V_ALW2,JUSH1.25 from GND to +3.3V_ALW2, JUSH1.26 from GND to +PWR_SRC.	X01(0.2)
24	39	HW	01/06/2015	compal	no business with vender-KEMET	change C619 from SGA00000N00 to SGA00002B00	X01(0.2)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	15,17	HW	01/06/2015	compal	CONN LIST1124	change JDIMM2 to ADDR0106-P005A, JDIMM4 to ADDR0107-P005A	X01(0.2)
26	46	HW	01/06/2015	compal	Board ID	change R875 to 130Kohm(SD028130380)	X01(0.2)
27	28	HW	01/08/2015	compal	Follow FAN CONTROL DEBUG tool connector PIN define	remove SWV_DBG from JDEG3.4, change JDEG1 PIN define.	X01(0.2)
28	28	HW	01/08/2015	compal	USH SMBUS PULL UP when wo/ USH/B	remove R3738,R3739,Q366 BS AAC@(let them always pop w/USH or wo/USH)	X01(0.2)
29	21	HW	01/08/2015	compal	Crystal EA	change CH13,CH14 from 22pF to 15pF.	X01(0.2)
30	40,30	HW	01/08/2015	compal	for Battery life measure	add PJP25,PJP26	X01(0.2)
31	18,20,30	HW	01/08/2015	compal	cost saving	change U17,UC3 from SA00003Y000 to SA000046R00,U33 from SA00003AR00 to SA00006Y800 and add @R42,change Q21 from SB000009K10 to SB000010C00	X01(0.2)
32	46	HW	01/08/2015	compal	EC5085 change CPN	change U51 to SA00006YH60	X01(0.2)
33	22	HW	01/09/2015	compal	ADD PWR net on pin16 of JSPI1	netname is +3.3V_SPI_R on JSPI1.16	X01(0.2)
34	22	HW	01/09/2015	compal	PLTRST group change balance before AND GATE and after	add RH349,@RH350,change RH210.1 to PCH_PLTRST#,RH337.1 to PCH_PLTRST#_AND,RH195.1 to PCH_PLTRST#	X01(0.2)
35	24	BIOS	01/13/2015	compal	AMI BIOS Bidirection debug	remove dummy net PCH_NFC_RST,add RH351,RH352 PU to +3.3V_ALW_PCH and add @RH354,@RH355 PU to +3.3V_RUN on UH1.AR39,UH1.AR45,add JUART1	X01(0.2)
36	14	HW	01/14/2015	compal	MOW rev1.0 ww02- recommended not to install any capacitor on DDR Reset signal (DRAMRST)	depop CD16	X01(0.2)
37	28	HW	01/19/2015	compal	resevrve AAC SMBUS control from PCH	add R38,R39,@R40,@R41,and R40.2 connect to UH1.AT42, R41.2 connect to UH1.AR38	X01(0.2)
38	47	ME	01/19/2015	compal	Screw hole	remove H26,H28,add H30,change H1,H2,H3,H4 from H_4P2 to H_3P8	X01(0.2)
39	10,11	HW	01/20/2015	intel	VENDER suggestion	remove RC218,@RC219,@RC311	X01(0.2)
40	28	HW	01/20/2015	COMPAL	ARD1.3	connect FAN1_TACH_FB_AAC to U8.24,FAN2_TACH_FB_AAC to U8.25,FAN1_TACH_EC_AAC to U8.26,FAN2_TACH_EC_AAC to U8.27	X01(0.2)
41	47	HW	01/20/2015	COMPAL	LED limit current R value	change R956,R955 to 1Kohm,R130,R131,R943 to 560ohm	X01(0.2)
42	31,32	HW	01/20/2015	COMPAL	DOCK DP1,DP2 EA	pop R117,R119,R121(AEQ disable,PEQ=8.5dB),RV29,RV35(PEQ=8.5dB)	X01(0.2)
43	37	HW	01/21/2015	COMPAL	TPM improve S3 support and back drive issue	Add RZ78,@RZ79,@RZ77,@RZ80,QZ2,RZ82,change U637.1 to +3.3V_ALW_PCH,U637.8 to +U637_TPM,U637.12 to NC	X01(0.2)
44	30	HW	01/22/2015	COMPAL	TOUCH_SCREEN_PD# PU PWR rail align with PC	change R426.1 to +3.3V_RUN	X01(0.2)
45	7	HW	01/26/2015	COMPAL	Solving for when system force shut down,it can't power on with power botten between 1 minute.	add @R43,@RC327,UC5,UC6	X01(0.2)
46	7	HW	01/26/2015	INTEL	DCI debug-when no XDP function,we can debug CPU and PCH from USB interface	change RC307,RC308,RC309,RC143 Bom Structure from XDP@ to always pop.	X01(0.2)
47	35	HW	03/16/2015	COMPAL	LAN EA	change L63~L70 to 0ohm(R63~R70)	X02(0.3)
48	20	HW	03/16/2015	INTEL	546717_SKL_PCH_H_EDS_R1_2(add a 1K PD for USB2_VBUSSENSE, if the signal is not used.Else it impacts Intel DCI test with warm boot),546765 WW10 MOW USB2_ID connected directly to GND,if platform no support dual role	add RH356,RH357 pull down to GND.	X02(0.3)
49	43	HW	03/16/2015	COMPAL	DOCK E-SATA signal reverse.	SWAP SATA_PTX_C_DRX_P1 to JDOCK1.60(C699.1),SATA_PTX_C_DRX_N1 to JDOCK1.62(C700.1)	X02(0.3)
50	28	HW	03/16/2015	COMPAL	FAN module keep EVT pin define,FAN connector pin define of MB need change to meet it from H type to V type.	change JFAN1,JFAN2 pin define to PIN1=+5V_RUN,PIN2=FB,PIN3=PWM,PIN4=GND	X02(0.3)
51	37	HW	03/16/2015	VENDER	reserve @RZ83 for modern standby,RZ84 for TPM detect issue.	add RZ83 connect to SIO_SLP_S0#,RZ84 between PCH_SPI_CS#2_R and QZ2.2, pop RZ79,depop RZ78.	X02(0.3)

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52	30	HW	03/16/2015	compal	reserve IR camera layout.	change JTS1 from 6pin to 10pin,add +BL_PWR_SRC on JTS1.9, JTS1.10 and add GND on JTS1.7,JTS1.8	X02(0.3)
53	23	RF	03/16/2015	compal	RF EA	pop CH42,CH49,CH50,CH51	X02(0.3)
54	30	HW	03/16/2015	compal	for AAC function	pop R361,R362	X02(0.3)
55	46	HW	03/17/2015	compal	material lack	change R374 from SD014430280 to SD034430280	X02(0.3)
56	18	HW	03/18/2015	compal	solve never detect Hot plug event input at Optimus GPU off	add R71,C1470,D95,R72change U14.1,U25.1,U27.1 from DGPU_PWROK to DGPU_PEX_RST#_D,remove @C95,@C96	X02(0.3)
57	24	HW	03/19/2015	compal	reserve DIMM TYPE selection	add RH358	X02(0.3)
58	47	HW	03/19/2015	compal	LED luminance adjust	change R943 from 560ohm to 1Kohm,R956 from 1Kohm to 430ohm	X02(0.3)
59	47	HW	03/24/2015	compal	screw hole	change H15 from NPTH to PTH	X02(0.3)
60	7	HW	03/24/2015	compal	XDP working	depop RC314,RC315,add RC328	X02(0.3)
61	44	HW	03/24/2015	compal	Keep VBUS PWR stable	change JIO2.17 from +PWR_SRC to +VBUS_DC_SS	X02(0.3)
62	7,23	HW	03/24/2015	compal	backdrive and DG1.0	change RH312.1,RH314.1,RH315.1 from +1.0V_VCCSTG to +1.0V_VCCST	X02(0.3)
63	21,46	HW	03/24/2015	compal	Crystal EA	change C741,C743 from 22pF to 33pF,CH4 from 18pF to 12pF,CH5 from 18pF to 15pF	X02(0.3)
64	24,30	HW	03/25/2015	compal	IR camera detect pin for verb table	add GPP_A23 to IR_CAM_DET# and connect to JEDP1 pin26,add R366 pull up to +3.3V_RUN	X02(0.3)
65	46	HW	03/30/2015	compal	board ID	change R875 from 130Kohm to 33Kohm	X02(0.3)
66	38	RF	04/21/2015	compal	reserve SIM detection design	add RZ113 between SIM pin1(JSIM1) to WWAN pin58(JNGFF2)	X03(0.4)
67	48	HW	04/21/2015	compal	TP module add damping R,PU and new touchpad support PS2(in DOS),I2C bus(in OS)	add R370,R400(PS2),depop R3752,R3758,add RZ116,RZ117 pull up to +3.3V_TP	X03(0.4)
68	45	HW	04/24/2015	compal	BITS211484: Left IO/B USB port 1 can't charge smart mobile device under S3/S4/S5	add RE72,RE73,RE74,RE75,RE76 pull up to +3.3V_ALW.	X03(0.4)
69	28	HW	04/27/2015	DELL	AAC update BOM for mic	change C1420 and C365 from 0.1uf to 2.2uF.	X03(0.4)
70	22	HW	04/27/2015	boardcom	USH reset by BCM58102	depop RH359	X03(0.4)
71	24,30	HW	05/18/2015	DELL	back to without IR support	Change TS1 from 10pin(ACES_50228-01071-001)to 6pin(ACES_50228-0067N-001),remove IR_CAM_DET# netname and R366.	X03(0.4)
72	22,30	HW	05/18/2015	DELL	Add Touch screen detect signal	Add TOUCH_SCREEN_DET# on UH1.BD24 and JTS1.5, Add R382 PU to +3.3V_RUN,and remove RH336.	X03(0.4)
73	18	HW	05/18/2015	NVIDIA	add test pad on DVI_HPD of MXM	Add T217 on DVI_HPD	X03(0.4)
74	46	HW	05/18/2015	compal	common EC code	change U51 from SA00006YH60 to SA00006YH30.	X03(0.4)
75	47	HW	05/18/2015	compal	HDD active LED behavior for PCIe M.2 SSD module	add D97,D98,D99,@R389,and add R383 PU to +3.3V_RUN,R384 PU to +3.3V_WWAN,R385 PU to +3.3V_SSD1	X03(0.4)
76	48	HW	05/21/2015	compal	BOM change for Touchpad function	pop CZ30,CZ31 and change them to 100pF	X03(0.4)
77	47	ME	05/21/2015	compal	Screw hole change	remove H11,H24,add H31	X03(0.4)
78	44,45	PWR	05/21/2015	compal	TBT PD power support	change JIO2.36 from GND to DCIN_ACOK#,and add PROCHOT_GATE on U46.A61	X03(0.4)
79	45	BIOS	05/22/2015	compal	EC detect for AR/B or non AR/B	change JIO2.34 from GND to PD_ACE_DET#_R,and add R388 between U46.A60 and PD_ACE_DET#_R.add RE77 PU to +3.3V_ALW	X03(0.4)
80	46	HW	05/22/2015	compal	board ID	change R875 from 33Kohm to 4.3Kohm	X03(0.4)
81	41,47	HW	05/22/2015	compal	BITS224631 [DVT1.1_M15/17]HDD LED indicator not light if use NVMe SSD	add U639,R386,D100,and add R387 PU to +3.3V_RUN	X03(0.4)

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82	26	HW	06/03/2015	compal	reserve 0.1uF for 5.76G noise	add @CH269	X04(0.5)
83	46	HW	06/03/2015	compal	Board ID	change R875 from 4.3kohm to 2kohm	X04(0.5)
84	44	HW	06/03/2015	compal	GPIO pin can direct PU/PD no need serise R to limilt current	change R388 from 10kohm to 0ohm	X04(0.5)
85	38	HW	06/03/2015	compal	SSD support gen3	change CZ1,CZ2,CZ91,CZ92 from 0.1uF to 0.22uF,remove CZ23,CZ24,add RZ118,RZ119	X04(0.5)
86	38	HW	06/04/2015	compal	WLAN module still need support LAN disable	pop D31	X04(0.5)
87	22	HW	06/08/2015	compal	QS CPU no need PD on SPI0_IO3 for boot	depop RH334	X04(0.5)
88	18	HW	06/11/2015	compal	MXM3.1 SPEC	remove @R6,@R1979,change JMXM1 pin268,pin270 to +3.3V_MXM	X04(0.5)
89	19,45	HW	06/11/2015	compal	reserve GPIO pin for tell EC don't read GFX Temp.in GC6	connect RH342.1 to U46.A48,remove R3749	X04(0.5)
90	45	HW	06/11/2015	compal	PROCHOT_GATE initial status	add @R415 PU to +3.3V_ALW,R416 PD to GND	X04(0.5)
91	49	HW	06/15/2015	compal	Dirty shutdown	add R417(PCH_ALW_ON)and @R418(SIO_SLP_SUS#_R)option select turn on +3.3V_ALW_PCH	X04(0.5)
92	46	HW	07/05/2015	compal	power on/off sequence tCPU05/tPLT18/tCPU03 and global reset issue	add U9,@C787 for tCPU05 and tPLT18,add RC329,CC273 for tCPU03,add @Q370,R435 for global reset	X05(0.6)
93	37	HW	07/05/2015	compal	TPM DS3 support	change U637.1 from +3.3V_ALW_PCH to +3.3V_ALW	X05(0.6)
94	46	HW	07/05/2015	compal	Board ID	change R875 from 2kohm to 1kohm	X05(0.6)
95	42	HW	07/29/2015	compal	SATA IEMT CTLE(change RX EQ from level 1 to 2)	pop RN130	1.0(A00)
96	41	HW	07/29/2015	compal	SATA PWR supply for over loading	pop C404,change C403 for 0.1uF to 22uF,and pop it.	1.0(A00)
97	11	HW	07/31/2015	compal	VCCPLL_OC power gate requirement for Deep Sleep support	depop RC302,add UZ30,@RC330,@CZ95,@CZ96,CZ97,UC7,@CZ98	1.0(A00)
98	46	HW	08/03/2015	compal	Board ID	change R875 from 1kohm to 62kohm	1.0(A00)
99	7,23	HW	08/07/2015	compal	backdrive and CPU EDS0.95	change RC135.1,RH312.1,RH314.1,RH315.1 from +1.0V_VCCST to +1.0V_VCCSTG	1.0(A00)
100	22,35,46	HW	08/07/2015	compal	MP component CPN	change UH1 to SA00009602L,U31 to SA000081G1L,U51 to SA00006YH90	1.0(A00)
101	7,23,28,30,44,49	HW	08/13/2015	compal	MP BOM change	depop R3739,R3738,R40,R41,U8,C31~C36,R23~R30,C141,C143,C365,C1420,R373,R375,R414,R410,R413,R411,R361,R362(drop AAC),SW1,SW2,R3728,UZ28,C513,C547,pop RC301	1.0(A00)

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1	P57	POWER	1/6	COMPAL	BQ24780 IFAULT LOW latch off	1. PC702 chagne to 0.1uF 2. PC704 change to 0.01uF	PR02
2	P51	POWER	1/6	COMPAL	PU101 change to TPS51285B	1. PU101 change to TPS51285B 2. PC100/PC118 chagne to 4.7uF 3. add PR114 4. PR105 change to 29.4k ohm 5. PR106 change to 31.6k ohm	PR02
3	P64	POWER	1/19	COMPAL	VCC_GTU sense	Add PR1620/PR1621 100ohm	PR02
4	P61	POWER	1/28	COMPAL	VCORE parameter adjust for vendor request	1. PR1109 change to 1.43k ohm 2. PR1137/PR1133 change to 3.65k ohm 3. PC1121/PC1124 change to 100pF 4. PR1132 change to 25.5k ohm 5. PC1123/PC1125 change to 0.1uF 6. PC1104 change to 2200pF 7. PR1112 change to 30k ohm 8. PC1107 change to 6800pF 9. PR1135 change to 24.9k ohm 10. PR1152 change to 75k ohm	PR02
5	P52	POWER	3/18	COMPAL	change unmount for HW request(power sequence)	PC215 change to numount	PR03
6	P53	POWER	3/18	COMPAL	Add RC for HW request(Power sequence)	Add PR317/PC312	PR03
7	P57	POWER	3/18	COMPAL	change to connect RENG for BATTERY reverse input protection	Add PD703 in IC RENG pin	PR03
8	P64	POWER	3/18	COMPAL	change VCC_GTU parameter for Vendor request	PR1604 change to 6.19k ohm add PC1690 to 4700p F	PR03
9	P57 P60	POWER	3/24	COMPAL	Add circuit to prevent +SDC_IN oscillation	Add PD704/PR766~PR770/PQ708 Add PD1101/1033~PR1037/PQ1005	PR03

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10	P61	POWER	3/26	COMPAL	Add PR1170 for CPU H LINE-42	Add PR1170	PR03
11	P57	POWER	4/29	COMPAL	change CHARGER parameter for Vendor request	PR744 change to 45.3k ohm	PR03
12	P57	POWER	4/30	COMPAL	Add circuit to detect type C current	Add PQ1073(SB00000DH00) /PR771(SD028000080) ,PR772(SD034100380) ,PR773(SD028000080)	PR04
13	P61	POWER	4/30	COMPAL	change VCORE parameter for IPCC solution	PR1153 change to 34.8k ohm(H44e) 、47kohm(H42)	PR04
14	P60	POWER	5/8	COMPAL	Add circuit for avoiding type C current to flow to battery	Add PD1102/ PD1103(SCS0340L010)/ PR1026 100 ohm(SD014100080)	PR04
15	P57	POWER	5/14	COMPAL	Change the charger ILIM circuit for current sense	PR758 from 18K to 20K、PR760 from 3.16K to 5.36K and PR764 from 20K to 2.74K	PR04
16	P57	POWER	5/19	COMPAL	Add circuit for the PD	Add PC151(SE102104K00)/ PQ1074(SB00000DH00)/ PU105(SA007080120)	PR04
17	P50	POWER	6/8	COMPAL	Add diodes for ESD team request	Add PD4/PD6(SCA00000T00)	PR05
18	P50	POWER	6/15	COMPAL	Change PU1 for ESD issue	Change PU1 from SA00003DN00 to SA00001WK00/ depop PD4/PD6	PR05
19	P61	POWER	6/23	COMPAL	change VCORE parameter for IPCC solution	PR1153 change to 30.9Kohm(SD034309280)	PR05
20	P52 P53	POWER	7/6	COMPAL	For tCPU05 (VDDQ 1.2V to VCCIO 1.0V) add one AGATE 7408 and control by SIO_SLP_S3# and 1.2V_SUS_PWRGD(for HW)	Depop PC312/PR303 Remove PR317 Change EC netname(to HW) from SIO_SLP_S3# to RUN_ON_AND Pop PR209 Add offpagethe for 1.2V_SUS_PWRGD	PR06

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21	P58	POWER	8/3	COMPAL	Add circuit control line for dirty shutdown issue	1.pop PR804 2. add line PCH_ALW_ON and PR809 0 ohm(depop) 3.depop PC800	PR10

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