NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

HEDWIG

INTEL TIGER LAKE-UP3 15W

DIS : 24.5X24.5

GPU : N18S-G5

VRAM : GDDR5 256MX32X2PCS

MV BUILD
2021.03.25

SSID
UMA 8819
DIS 881A

CPU LIST				
I3-		TGL	6025B0436701	QU7M
I5-		TGL	6025B0436401	QU7K
I7-		TGL	6025B0436301	QU7J

GPU LIST	
NV N18S-G5	6019B2036901

VRAM LIST		
Hynix	H5GC8H24MJR-R0C	6019B1542101
Micron	MT51J256M32HF-70:A	6019B1486001
Samsung	K4G80325FB-HC28	6019B1485901
Hynix	H5GC8H24AJR-R2C A	6019B1723701
Micron	MT51J256M32HF-80:B B	6019B1721101
Samsung	K4G80325FC-HC25	6019B1926601

LOCATION	LEVEL		CO-LAY	
PAD6015	PVBAT	SHORT		
PAD60200	P5V0A	SHORT		
PAD60203	P5V0AL	OPEN		
PAD60210	PVBAT	SHORT		
PAD60100	P3V3A	SHORT		
PAD60110	PVBAT	SHORT		
PAD60103	P3V3AL	SHORT		
PAD60310	PVBAT	SHORT		
PAD60300	P1V2	SHORT	R60399	OPEN
PAD60350	P0V6S	SHORT		
PAD60410	P3V3A	SHORT		
PAD60400	P2V5	SHORT		
PAD6970	P1V8A	SHORT		
PAD6980	P5V0A	SHORT		
PAD66020	PVBAT	SHORT		
PAD66010	PVBAT	SHORT		
PAD66610	PVBAT	SHORT		
PAD2500	P5V0A_USBPWR	OPEN		
PAD67010	PVBAT	SHORT	R67010	OPEN
PAD67200	P1V35S_DGPU	SHORT		
PAD67210	PVBAT	SHORT		
PAD67410	P3V3A	SHORT		
PAD67610	P3V3A	SHORT		
PAD67600	P1V0S_DGPU	SHORT		
PAD7402	P1V8S_MAIN1	SHORT		
PAD7401	P1V8S_AO1	SHORT		

ID PIN FOR BIOS

DGPU_PRSNT#	UMA	DIS
R4587	MOUNT	OPEN
R4588	OPEN	MOUNT
	3V	0V

DGPU_PWROK	UMA	DIS
R4591	MOUNT	OPEN

BUILD ID	ID1 (R44236 : 0, R44224 : 1)	ID0 (R44222 : 0, R44221 : 1)
DB	0	0
SI	0	1
PV	1	0
MV	1	1

WWAN_SKU_ID	WWAN	Non-WWAN
R4523	MOUNT	OPEN
R4524	OPEN	MOUNT
	3V	0V

BOARD_ID0	ATI	NV
R4559	MOUNT	OPEN
R4618	OPEN	MOUNT
	3V	0V

PROJECT_ID0	VRAM 2G	VRAM 4G
R4579	MOUNT	OPEN
R4578	OPEN	MOUNT
	3V	0V

BOARD_ID1	DIS	UMA
R4535	MOUNT	OPEN
R4536	OPEN	MOUNT
	3V	0V

PROJECT_ID1	17-SNAPE	14-HEDWING
R4530	MOUNT	OPEN
R4526	OPEN	MOUNT
	3V	0V

BOARD_ID2	U42	U22
R4632	MOUNT	OPEN
R4514	OPEN	MOUNT
	3V	0V

PROJECT_ID2	14-GRANGER	14-SLIVERBELL
R4532	MOUNT	OPEN
R4533	OPEN	MOUNT
	3V	0V

ID PIN FOR EC

GPU_UMA_SEL	DIS	UMA
R392	MOUNT	OPEN
R393	OPEN	MOUNT
	3V	0V

Phase_ID	SI	DB	PV / MV
R337	10K_short	10K_short	10K_open
R322	10K_open	10K_short	10K_short
	3V	1.5V	0V

GPU_ID	NV	ATI
R390	MOUNT	OPEN
R391	OPEN	MOUNT
	3V	0V

EC_PROJECT_ID	SNAPE17"	GRANGER14"
R310	10K_short	10K_open
R311	10K_open	10K_short
	3V	0V

ADP_SEL	65W	45W
R307	MOUNT	OPEN
R309	OPEN	MOUNT
	3V	0V

CPU_ID	R42_15W	U22_15W
R343	MOUNT	OPEN
R338	OPEN	MOUNT
	3V	0V

HEDWIG TGL + N18S-G5		6050A3285801 (8L)
DAUGHTER BOARD (8L)	PICK BUTTON BOARD (TYPE C)	6050A3163901 (8L)
	CARD READER BOARD (TYPE C)	6050A3283201 (8L)

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL	Hsu Andy		
FILE NAME	Hsu Andy		
PCB P/N	6[illegible]	PCB VER	XXX

INVENTEC

TITLE: MLB 17" - RANGERS Main Board

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET [illegible] of [illegible]

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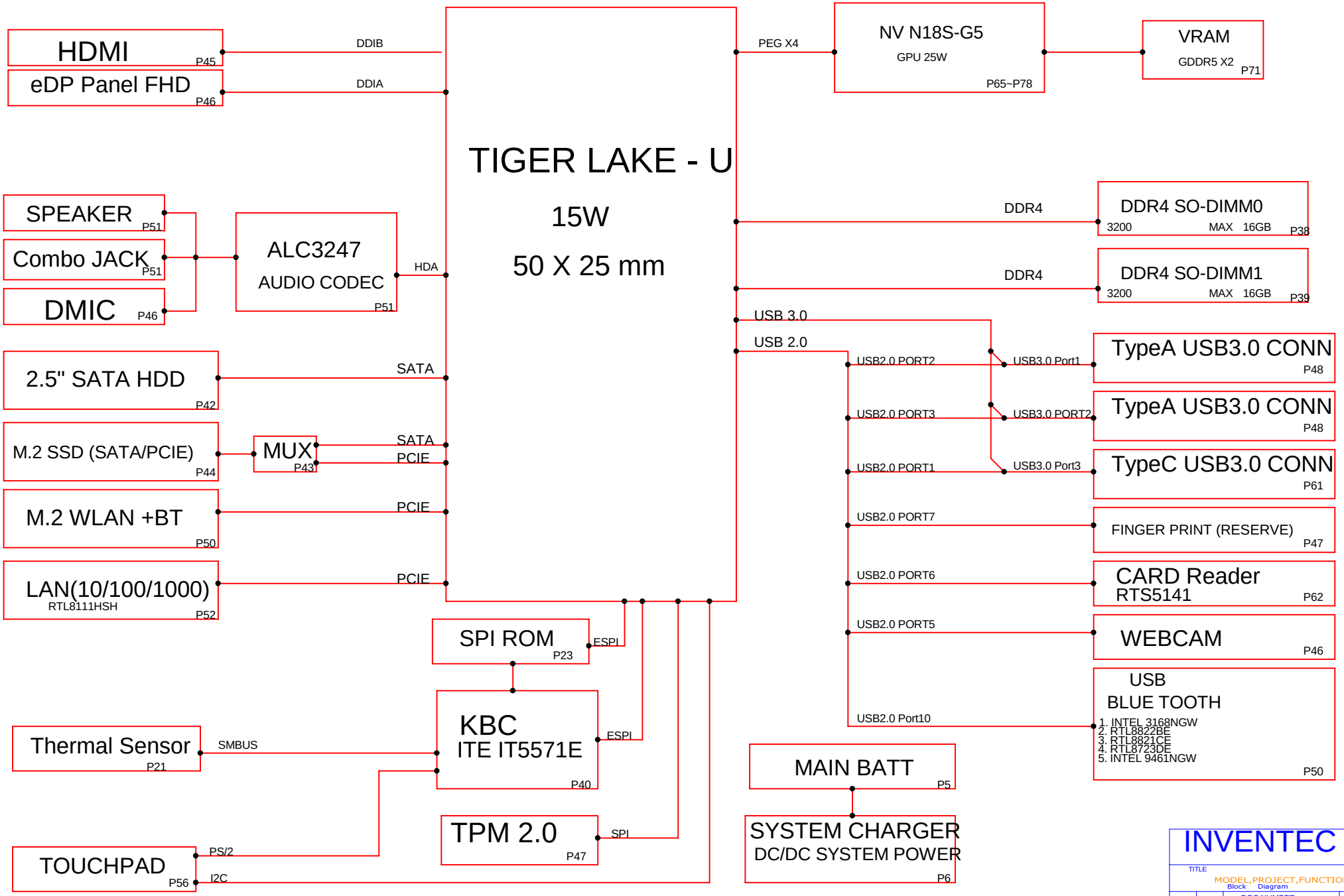
2 index
3 Block Diagram
4 Power Procedure
5 seletor
6 STORAGE MODE
7 CHARGER_BQ24725A
8 DC PROCHOT#
9 P5V0A_SYV126C
10 P3V3A_SYV126B
11 DDR POWER(P1V2_P0V675S)
12 P2V5_AP2132B
13 P1V8A_RT8068A
14 CPU VR CONTROLLER RT3613EE
15 VCORE MOS
16 PVCCIN AUX MP2941
17 CPU POWER LOAD SW
18 POWER LOAD SW
19 ENABLE PIN
20 PDG SEQUENCE
21 THERMAL & FAN
22 MCP_MEMORY
23 SPI ROM
24 MCP-GPIO1, LPC, SPI
25 MCP-GPIO2, I2C, UART
26 MCP-MISC, HDA, JTAG
27 MCP-CSI, CNV
28 MCP-PCIE, USB3, USB2
29 MCP-CLK, RTC, CFG
30 DDI, TCP
31 MCP-POWER MANAGEMENT
32 MCP-POWER1
33 MCP-POWER2
34 MCP-POWER3
35 MCP-GND, RSVD
36 MCP-STRAPS-1
37 MCP-STRAPS-1
38 DDR4 DIMM0
39 DDR4 DIMM1
40 EC
41 KB CONN & LED
42 SATA HDD
43 MUX FOR SATA /PCIE SSD
44 SSD_M2_2280_S3_M-KEY
45 HDMI
46 30PIN LCM
47 TPM 2.0 & FINGER PRINTER
48 USB3.0 CONN_2 PORT
49 USB3.0 CHARGER
50 WLAN_M2_2230_E-KEY
51 AUDIO CODEC
52 LAN_RTL8166EH
53 TRANSFORMER & RJ45
54 EMC CAP
55 RF SOLUTION
56 MB TO DB CONN & SCREW
57 MB TO CR BOARD
58 DB COVER
59 DB1-USB3.0
60 DB1-USB3.0 HUB
61 DB1-USB3.0 TYPE_C
62 DB1-CARD READER
63 DB1-POWER BUTTON & LID
64 DB2-PICK BUTTON
65 GPU COVER
66 GPU-1
67 GPU-2
68 GPU-3
69 GPU-4
70 GPU-5
71 GPU VRAM
72 PVCORE_DGPU (RT8816A 2 PHASE)
73 P1V35S_DGPU (NB685A)
74 P1V8S_DGPU (RT8097A)
75 P1V0S_DGPU (RT8097A)
76 DGPU POWER SEQUENCE
77 GPU DISCHARGE
78 GPU SEQUENCE

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION INDEX			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 2 of 77			


HDMI
P45
eDP Panel FHD
P46
DDIB
DDIA
TIGER LAKE - U
15W
50 X 25 mm
PEG X4
NV N18S-G5
GPU 25W
P65~P78
VRAM
GDDR5 X2
P71
SPEAKER
P51
Combo JACK
P51
DMIC
P46
ALC3247
AUDIO CODEC
P51
HDA
DDR4
DDR4 SO-DIMM0
3200 MAX 16GB
P38
DDR4
DDR4 SO-DIMM1
3200 MAX 16GB
P39
USB 3.0
USB 2.0
2.5" SATA HDD
P42
SATA
M.2 SSD (SATA/PCIE)
P44
MUX
P43
SATA
PCIE
M.2 WLAN +BT
P50
PCIE
LAN(10/100/1000)
RTL8111HSH
P52
PCIE
USB2.0 PORT2
USB3.0 Port1
TypeA USB3.0 CONN
P48
USB2.0 PORT3
USB3.0 PORT2
TypeA USB3.0 CONN
P48
USB2.0 PORT1
USB3.0 Port3
TypeC USB3.0 CONN
P61
USB2.0 PORT7
FINGER PRINT (RESERVE)
P47
USB2.0 PORT6
CARD Reader
RTS5141
P62
USB2.0 PORT5
WEBCAM
P46
USB
BLUE TOOTH
1. INTEL 3168NGW
2. RTL8822BE
3. RTL8821CE
4. RTL8723DE
5. INTEL 9461NGW
P50
USB2.0 Port10
SPI ROM
P23
ESPI
KBC
ITE IT5571E
P40
ESPI
Thermal Sensor
P21
SMBUS
TPM 2.0
P47
SPI
TOUCHPAD
P56
PS/2
I2C
MAIN BATT
P5
SYSTEM CHARGER
DC/DC SYSTEM POWER
P6
INVENTEC
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Block Diagram
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CODE CS
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REV X01
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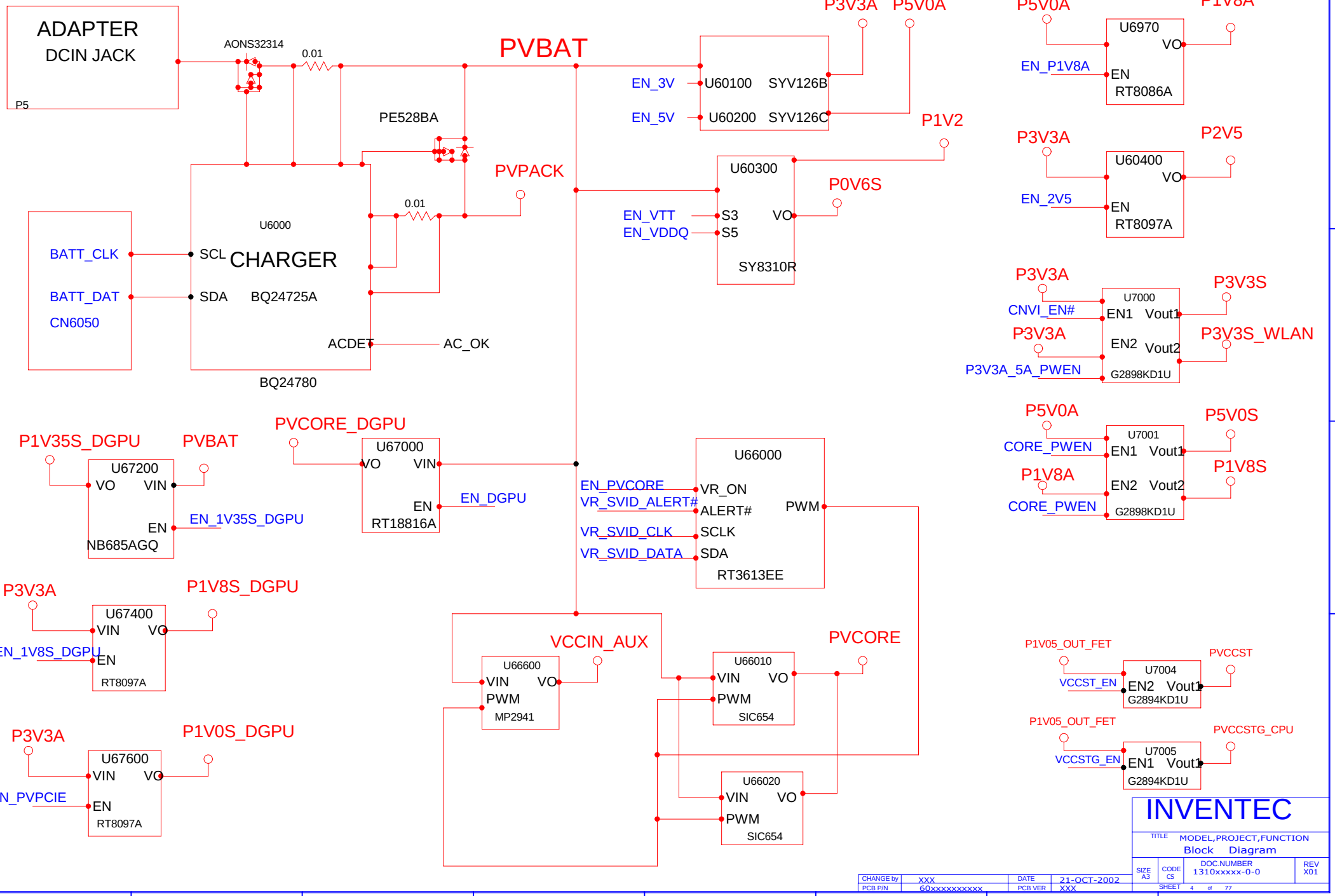
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX


ADAPTER
DCIN JACK
P5
AONS32314
0.01
PVBAT
PE528BA
0.01
PVPACK
U6000
BATT_CLK
BATT_DAT
CN6050
SCL
SDA
CHARGER
BQ24725A
ACDET
AC_OK
BQ24780
P3V3A
P5V0A
EN_3V
EN_5V
U60100
SYV126B
U60200
SYV126C
P1V2
U60300
P0V6S
EN_VTT
EN_VDDQ
S3
S5
VO
SY8310R
P5V0A
P1V8A
U6970
VO
EN_P1V8A
EN
RT8086A
P3V3A
P2V5
U60400
VO
EN_2V5
EN
RT8097A
P3V3A
P3V3S
U7000
CNVI_EN#
EN1
Vout1
P3V3A
P3V3S_WLAN
EN2
Vout2
P3V3A_5A_PWEN
G2898KD1U
P5V0A
P5V0S
U7001
CORE_PWEN
EN1
Vout1
P1V8A
P1V8S
EN2
Vout2
CORE_PWEN
G2898KD1U
P1V35S_DGPU
PVBAT
U67200
VO
VIN
EN
EN_1V35S_DGPU
NB685AGQ
PVCORE_DGPU
U67000
VO
VIN
EN
EN_DGPU
RT18816A
U66000
EN_PVCORE
VR_SVID_ALERT#
VR_SVID_CLK
VR_SVID_DATA
VR_ON
ALERT#
SCLK
SDA
PWM
RT3613EE
P3V3A
P1V8S_DGPU
U67400
VIN
VO
EN_1V8S_DGPU
EN
RT8097A
VCCIN_AUX
PVCORE
U66600
VIN
VO
PWM
MP2941
U66010
VIN
VO
PWM
SIC654
U66020
VIN
VO
PWM
SIC654
P3V3A
P1V0S_DGPU
U67600
VIN
VO
EN_PVPCIE
EN
RT8097A
P1V05_OUT_FET
PVCCST
VCCST_EN
U7004
EN2
Vout1
G2894KD1U
P1V05_OUT_FET
PVCCSTG_CPU
VCCSTG_EN
U7005
EN1
Vout1
G2894KD1U
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
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REV X01
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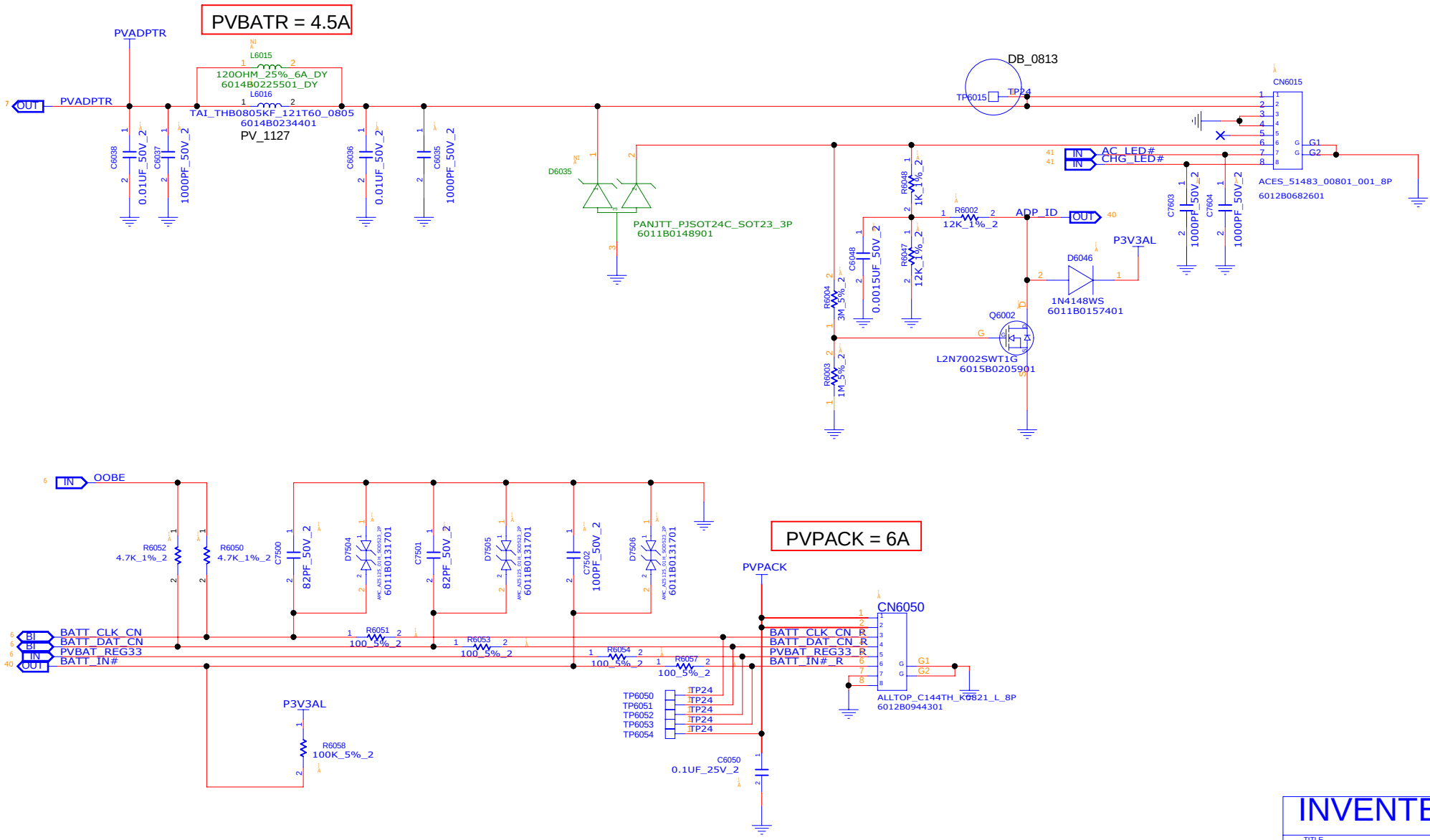
CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

SELETOR

VER.04_20171113



INVENTEC

TITLE: MODEL, PROJECT, FUNCTION Block Diagram

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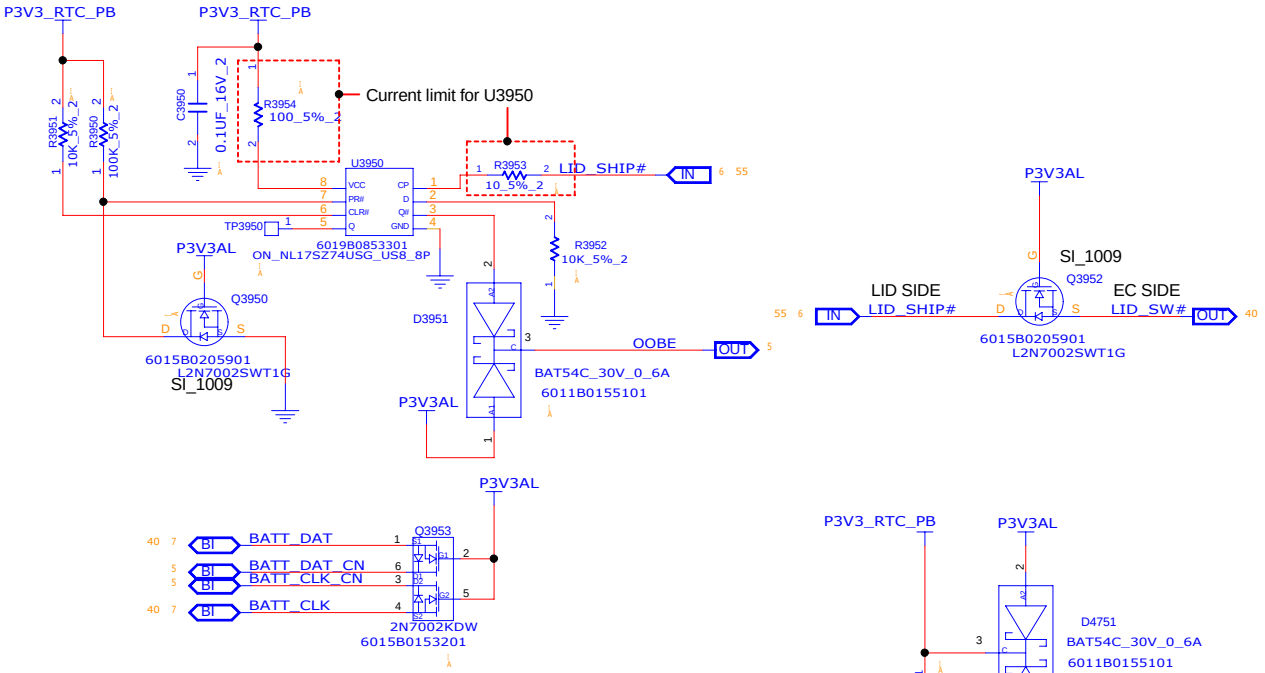
STORAGE MODE

VER.01_20170918



TRUTH TABLE

INPUT				OUTPUT		OPARATING MODE
PR#	CLR#	CP	D	Q	Q#	
L	H	X	X	H	L	ASYNCHRONOUS SET
H	L	X	X	L	H	ASYNCHRONOUS CLEAR
L	L	X	X	H	H	UNDETERNLNED
H	H	↑	H	H	L	LOAD AND READ REGISTER
H	H	↑	L	L	H	

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Storage Mode

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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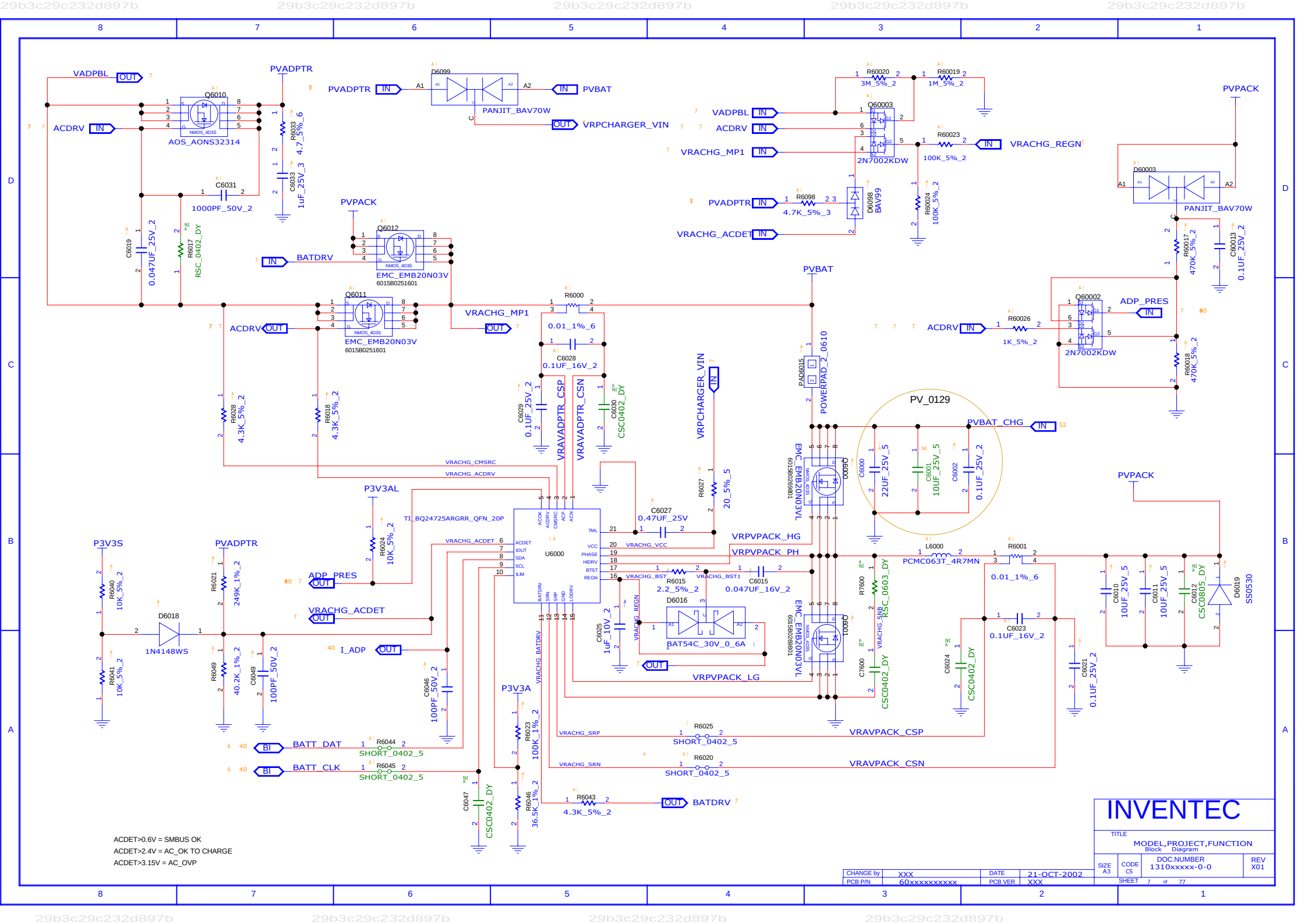
PCB P/N	60xxxxxxxxxx	PCB VER	XXX


VADPBL
PVADPTR
PVPACK
PVBAT
ACDRV
BATDRV
VRACHG_MP1
VRACHG_ACDET
VRACHG_REGN
ADP_PRES
VRACHG_ACDET
I_ADP
BATT_DAT
BATT_CLK
VRPCHARGER_VIN
PVBAT_CHG
VRPVPACK_HG
VRPVPACK_PH
VRPVPACK_LG
VRAVPACK_CSP
VRAVPACK_CSN
VRAVADPTR_CSP
VRAVADPTR_CSN
P3V3S
P3V3AL
P3V3A
AOS_AONS32314
EMC_EMB20N03V
6015B0251601
2N7002KDW
PANJIT_BAV70W
BAV99
BAT54C_30V_0_6A
1N4148WS
TI_BQ24725ARGRR_QFN_20P
PCMC063T_4R7MN
SS0530
POWERPAD_2_0610
PV_0129
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
DOC.NUMBER
1310xxxxx-0-0
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X01
SIZE
A3
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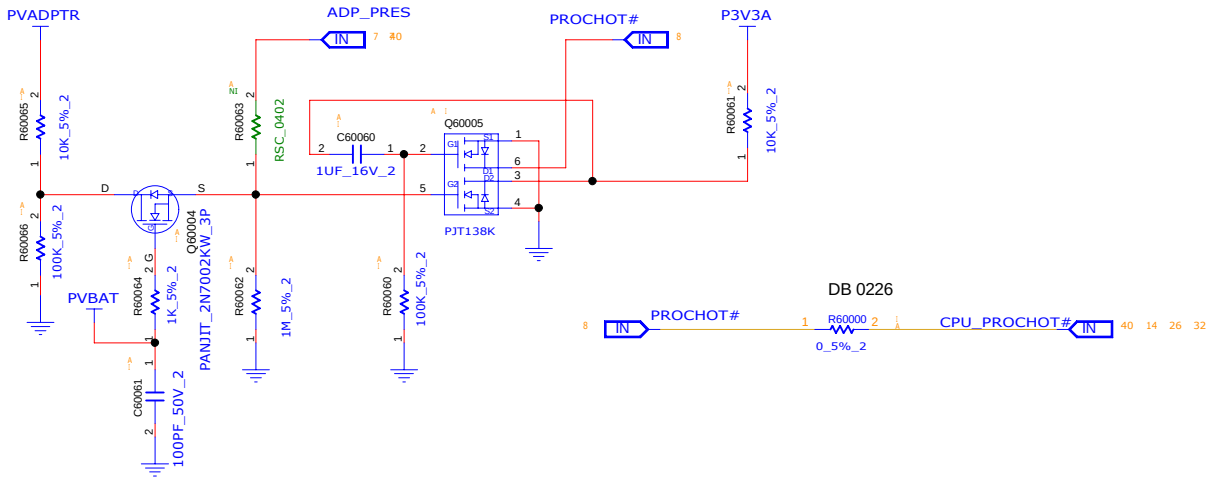
XXX
ACDET>0.6V = SMBUS OK
ACDET>2.4V = AC_OK TO CHARGE
ACDET>3.15V = AC_OVP



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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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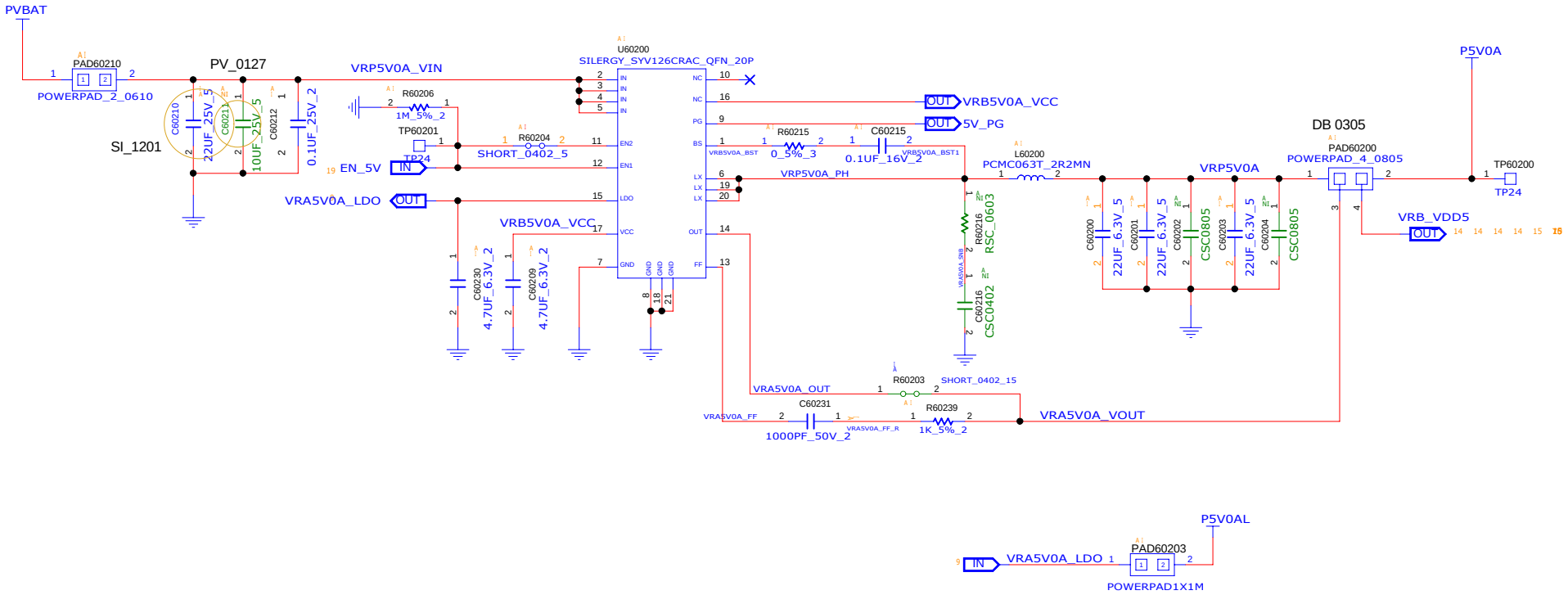

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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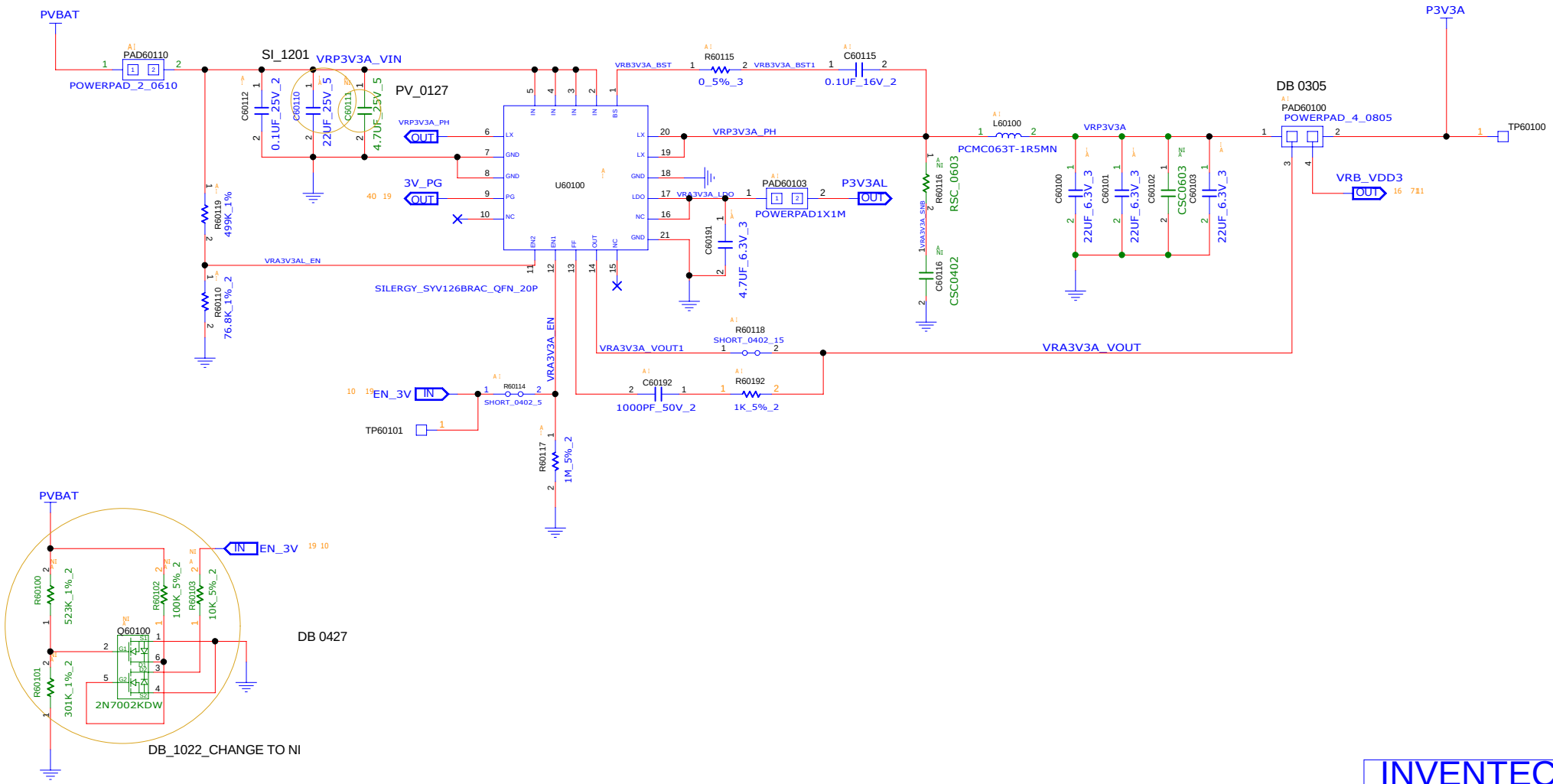
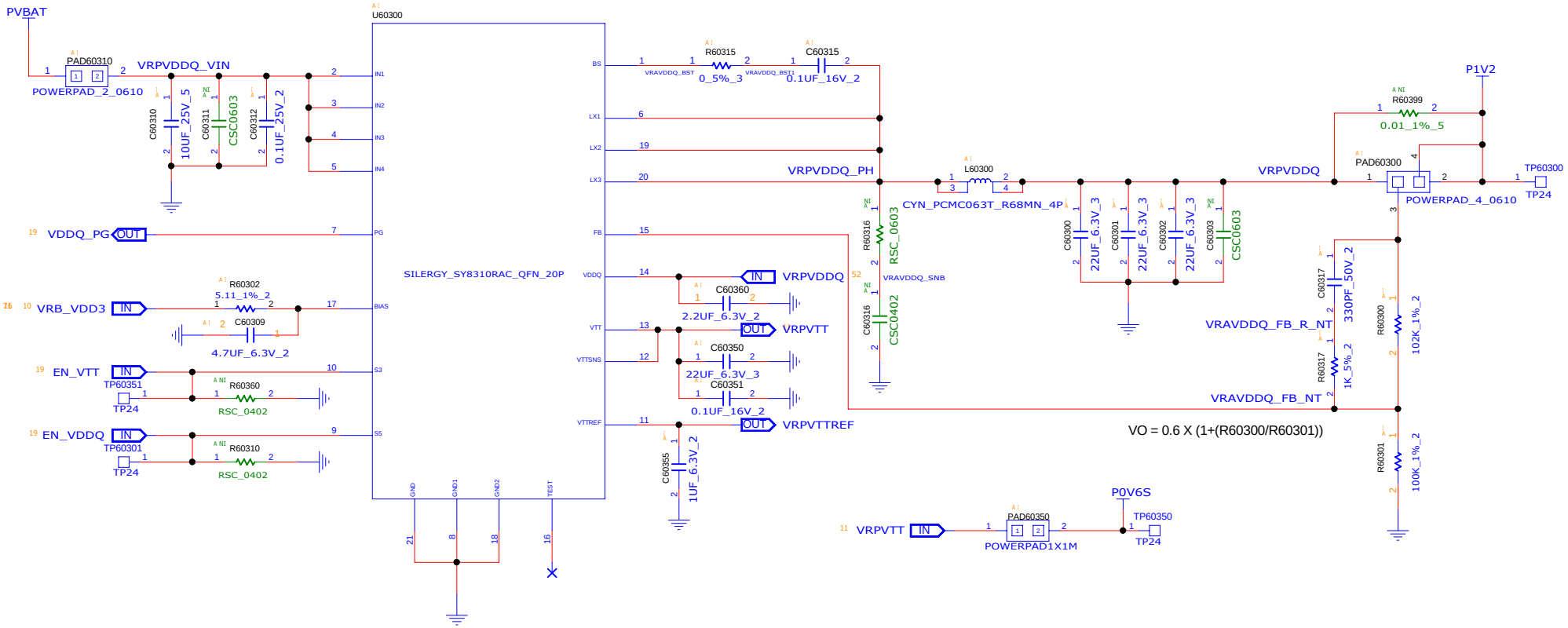


INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET 10 of 77	



S3	S5	STATE	BUCK	VTTREF	VTT
High	High	S0	On	On	On
Low	High	S3	On	On	Off (High-Z)
Low	Low	S4/S5	Off (Discharge)	Off (Discharge)	Off (Discharge)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
S5/S3 Rising Threshold	V_{S3_R}		1			V
S5/S3 Falling Threshold	V_{S3_F}				0.3	V
S5 Voltage for USM Mode	V_{S5_USM}		1		1.8	V
S5 Voltage for PFM Mode	V_{S5_PFM}		2.1		V_{IN}	V

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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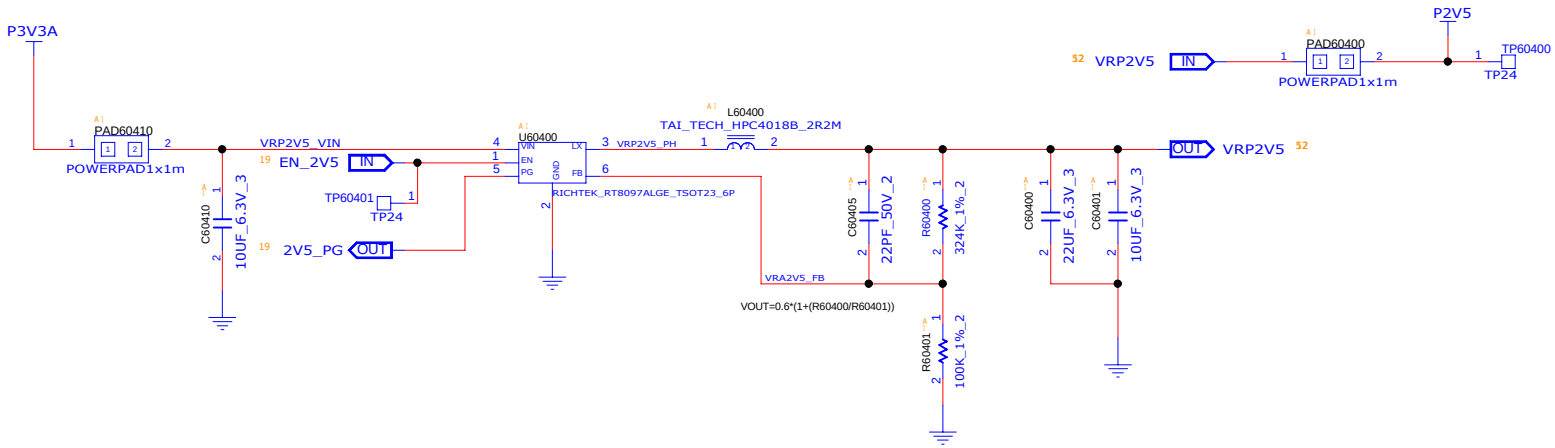

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
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Block Diagram

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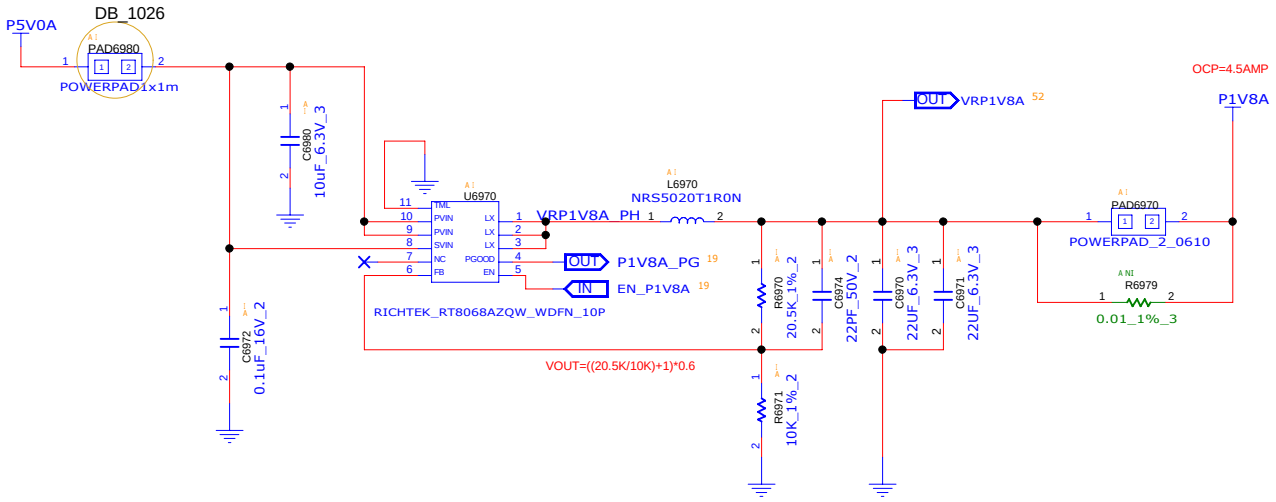

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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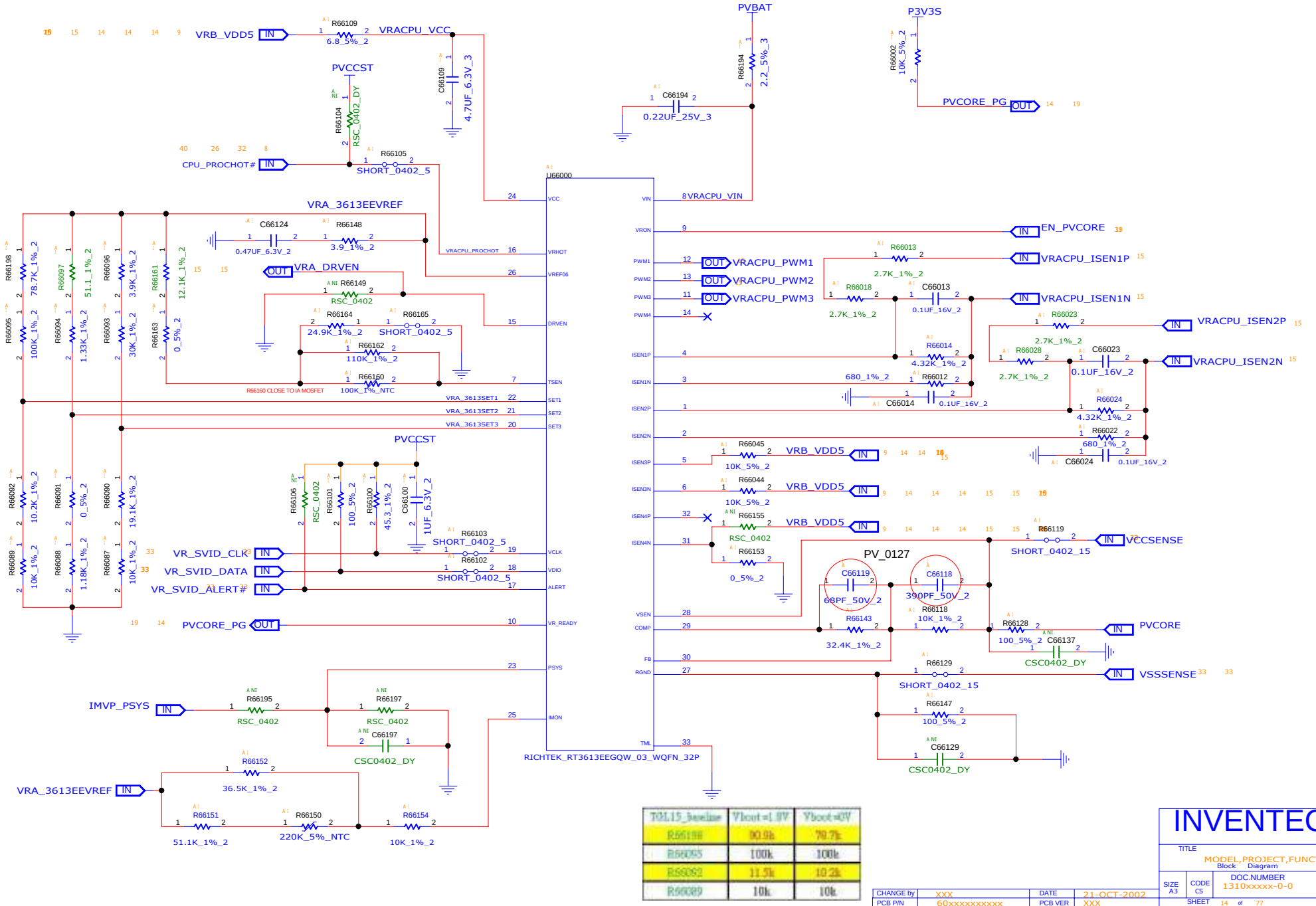
VRB_VDD5
R66109
6.8_5%_2
VRACPU_VCC
PVCCST
R66104
RSC_0402_DY
C66109
4.7UF_6.3V_3
CPU_PROCHOT#
R66105
SHORT_0402_5
PVBAT
R66194
2.2_5%_3
C66194
0.22UF_25V_3
P3V3S
R66002
10K_5%_2
PVCORE_PG
U66000
VRA_3613EEVREF
C66124
0.47UF_6.3V_2
R66148
3.9_1%_2
VRACPU_PROCHOT
VRA_DRVEN
R66149
RSC_0402
R66164
24.9K_1%_2
R66165
SHORT_0402_5
R66162
110K_1%_2
R66160
100K_1%_NTC
R66160 CLOSE TO IA MOSFET
VRA_3613SET1
VRA_3613SET2
VRA_3613SET3
R66198
78.7K_1%_2
R66097
51.1_1%_2
R66096
3.9K_1%_2
R66161
12.1K_1%_2
R66095
100K_1%_2
R66094
1.33K_1%_2
R66093
30K_1%_2
R66163
0_5%_2
R66092
10.2K_1%_2
R66091
0_5%_2
R66090
19.1K_1%_2
R66089
10K_1%_2
R66088
1.18K_1%_2
R66087
10K_1%_2
R66106
RSC_0402
R66101
100_5%_2
R66100
45.3_1%_2
C66100
1UF_6.3V_2
R66103
SHORT_0402_5
R66102
SHORT_0402_5
VR_SVID_CLK
VR_SVID_DATA
VR_SVID_ALERT#
PVCORE_PG
IMVP_PSYS
R66195
RSC_0402
R66197
RSC_0402
C66197
CSC0402_DY
R66152
36.5K_1%_2
VRA_3613EEVREF
R66151
51.1K_1%_2
R66150
220K_5%_NTC
R66154
10K_1%_2
RICHTEK_RT3613EEGQW_03_WQFN_32P
VRACPU_VIN
EN_PVCORE
VRACPU_PWM1
VRACPU_PWM2
VRACPU_PWM3
R66013
2.7K_1%_2
VRACPU_ISEN1P
R66018
2.7K_1%_2
C66013
0.1UF_16V_2
VRACPU_ISEN1N
R66014
4.32K_1%_2
680_1%_2
R66012
C66014
0.1UF_16V_2
R66023
2.7K_1%_2
VRACPU_ISEN2P
R66028
2.7K_1%_2
C66023
0.1UF_16V_2
VRACPU_ISEN2N
R66024
4.32K_1%_2
R66022
680_1%_2
C66024
0.1UF_16V_2
R66045
10K_5%_2
VRB_VDD5
R66044
10K_5%_2
VRB_VDD5
R66155
RSC_0402
R66153
0_5%_2
VRB_VDD5
PV_0127
C66119
68PF_50V_2
C66118
390PF_50V_2
R66119
SHORT_0402_15
VCCSENSE
R66143
32.4K_1%_2
R66118
10K_1%_2
R66128
100_5%_2
C66137
CSC0402_DY
PVCORE
R66129
SHORT_0402_15
VSSSENSE
R66147
100_5%_2
C66129
CSC0402_DY
TGL15_baseline
Vboot=1.8V
Vboot=0V
R66198
90.9k
78.7k
R66095
100k
100k
R66092
11.5k
10.2k
R66089
10k
10k
INVENTEC
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MODEL,PROJECT,FUNCTION
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SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
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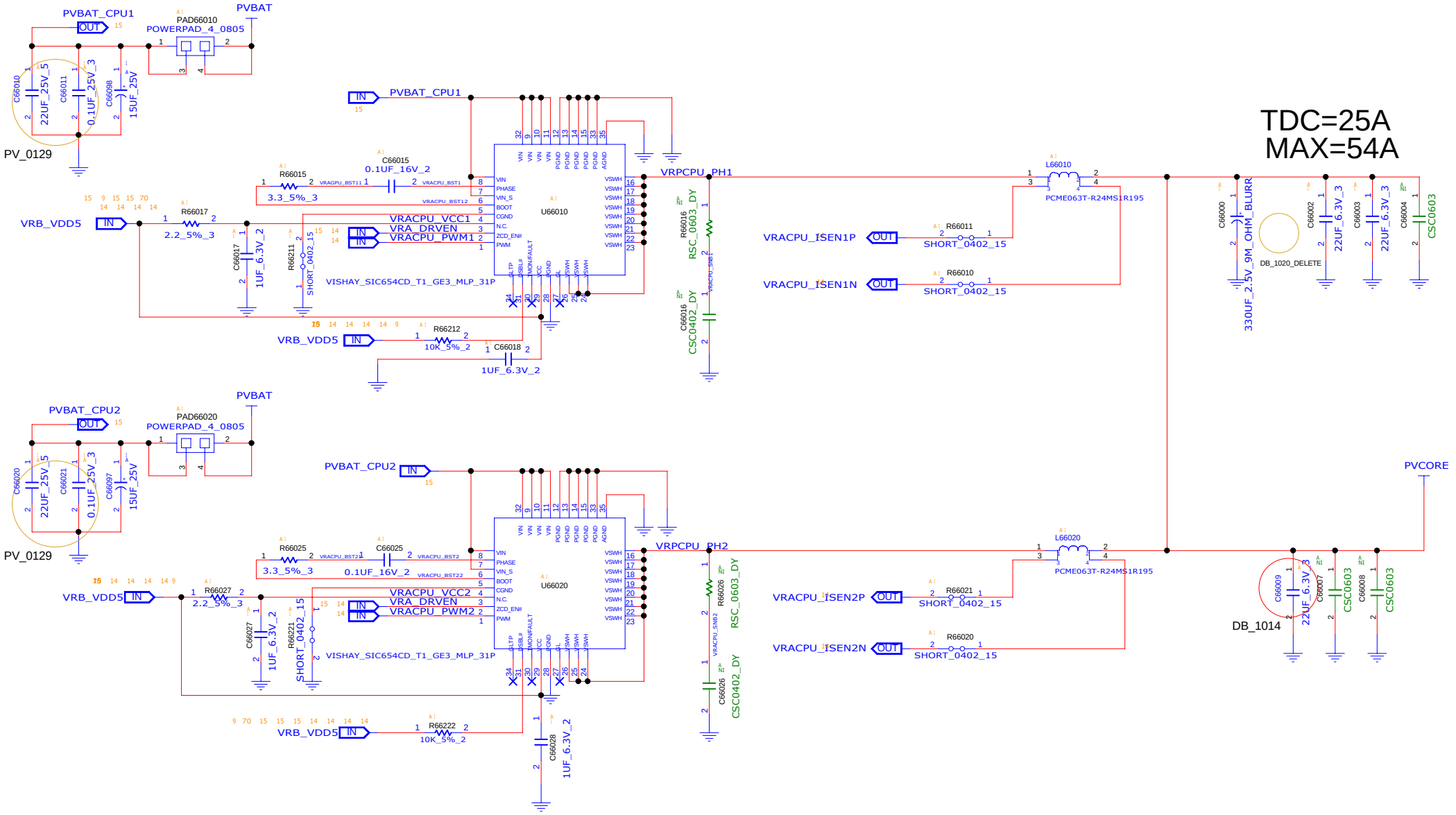
SHEET 14 of 77
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX



		IA			AUX		PL(W)		
TGL 15	Thermal sku	IccMax (A)	I_PL2 (A)	LL (mΩ)	IccMax (A)	I_PL2 (A)	PL1	PL2	PL4
U42	Baseline	47	30	2	27	14	15	51	93

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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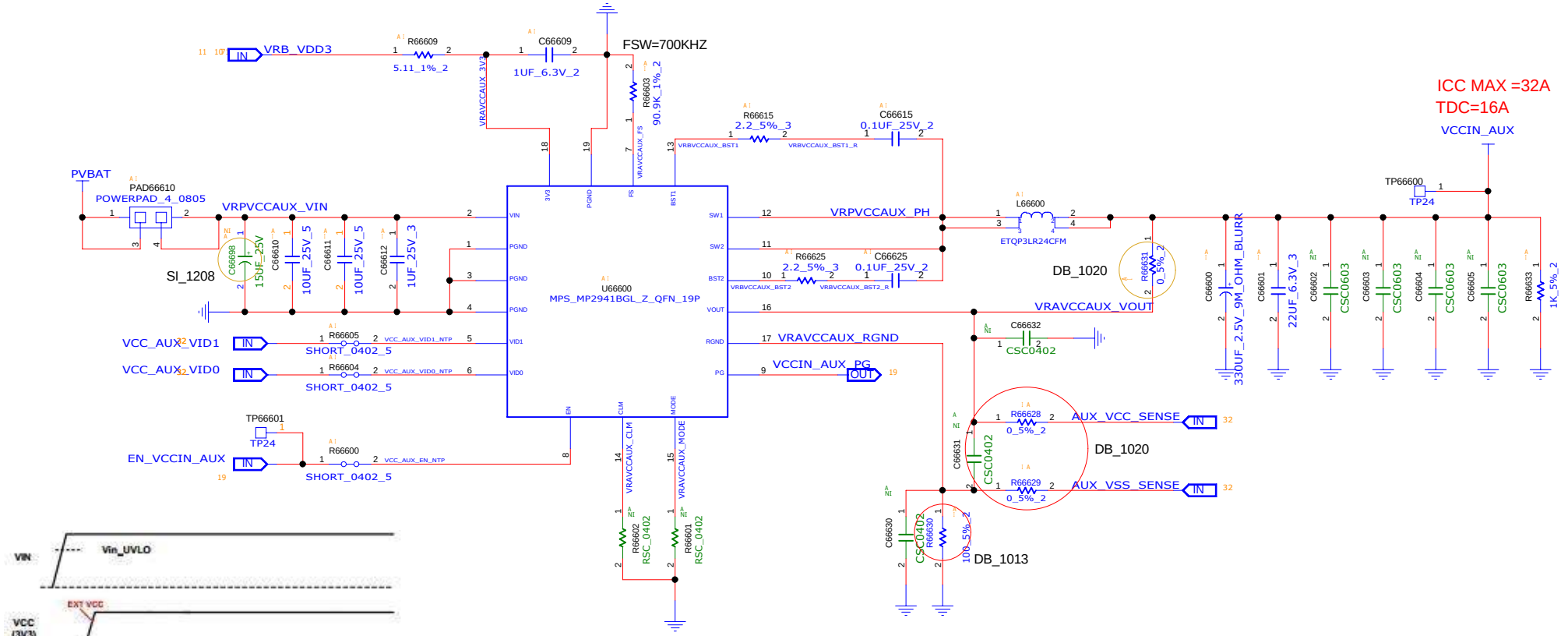
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET 15 of 77	



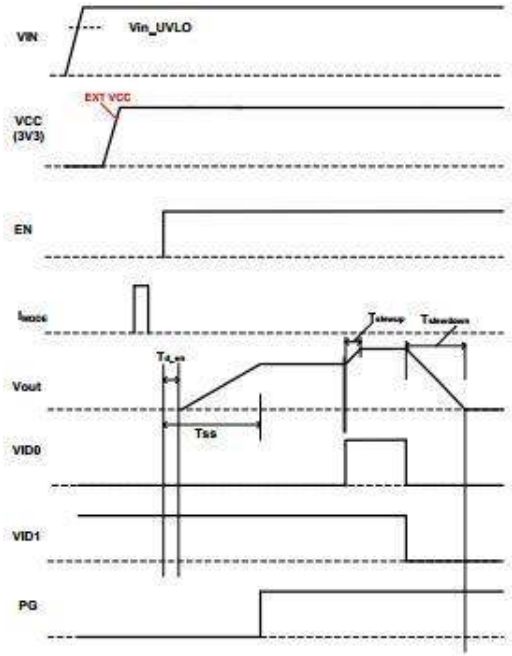


Figure 4—Start-up power sequence

Table 1—MODE Select

State	Interleaving	VID Down	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90 K
M3	Y	Decay	150 K
M4	N	Decay	>230 K or float

Table 2—FS Selection

State	Fs	Resistor to GND
M1	500kHz	0
M2	700kHz	90 K
M3	1000kHz	150 K
M4	1200kHz	>230 K or float

Table 3—VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table 4—CLM/Phase Selection

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90 K
M3	13A	150 K
M4	16A	>230 K or float

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION PVCCGT			
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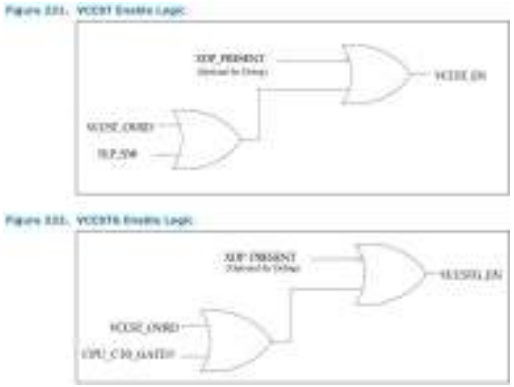
P1V05_OUT_FET
P5V0A
DB 0309
U7004
GMT_G2894KD1U_TDFN_15P
6019B1978801
PV_0121
PVCCST
C7029
10uF_6.3V_3
PVCCST = 0.5A
PVCCSTG_CPU
PVCCSTG = 0.3A
0.01_1%_3
6013A0006701
C7028 1UF_10V_2
C7040 1uF_10V_2
C7041 1000PF_50V_2
C7042 1000PF_50V_2
C7002 22UF_6.3V_3
C7031 1uF_10V_2
C7020 10uF_6.3V_3
R7045 10K_5%_2
VCCST_EN
C7027 0.1UF_25V_2
DB_1007
R7030 SHORT_0402_5
VCCSTG_EN
C7025 0.01UF_50V_2
SI_1117
R7037 SHORT_0402_5
DB_0507
SLP_S3#
P3V3_VCCST_ORD
P3V3A
U7005
NXP_74AUP1G32GW_TSSOP_5P
6019B1778801
DB_1005
R7020 100K_5%_2
CPU_C10_GATE#
R7033 SHORT_0402_5
U7010
VCCSTG_EN
R7018 100K_5%_2
R7026 100K_5%_2
VCCST_ORD#G
Q7002
L2N7002SWT1G
6015B0205901
Q7003
PJC7428
6015B0206501
R7008 0_5%_2
VCCST_ORD
VCCST_PG_TCSS
R7010 SHORT_0402_5
R7011 100K_5%_2



FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

DISCHARGE
P5V0A
PVCCSTG_CPU
DG 10.1.13
R7041 200K_5%_2
R7034 33_5%_3
Q7001
DB_1022_CHANGE TO NI
VCCSTG_EN
EM6K1GT2R
6015B0155001

INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV X01
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CHANGE by XXX | DATE 21-OCT-2002
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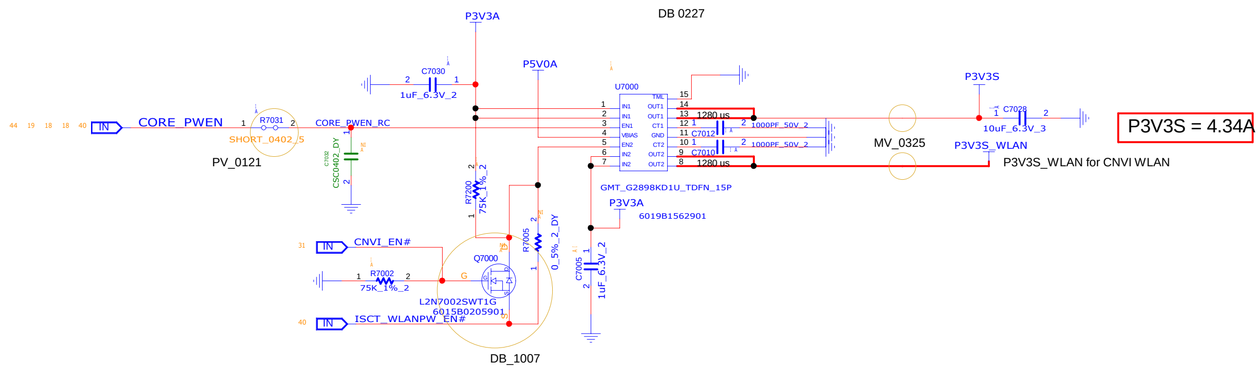
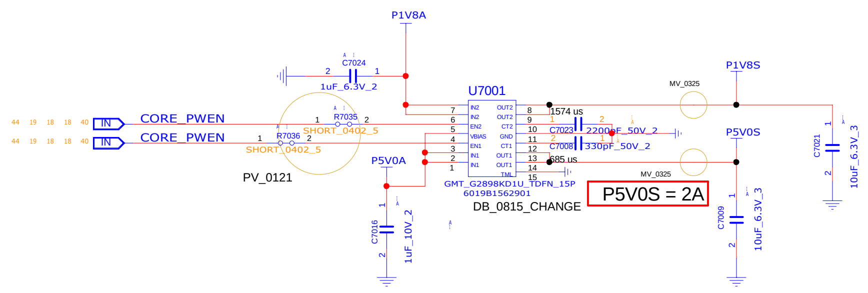


DB_1005



DB_1005

Table 11-10. Differences between Power Maps

Volume	Premium
VccRTG and VccST are merged and gated by SLP_S0#	VccRTG gated by (CPU_C10_GATE#)
VccPLL_OC is supplied directly from VDDQ	VccPLL_OC is supplied from VDDQ through a load switch
VCC1P8A on the CPU is supplied directly by V1.8A	VCC1P8A is supplied from V1.8A and gated by CPU_C10_GATE#
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH PWR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH PWR during light load
Various system devices share load switches	Various system devices have their own independent load switches

Notes:
1. VCC_VNNEXT_1P05 is also known as VNN BYP
2. VCC_V1P05EXT_1P05 is also known as VP105 BYP
3. Other changes may be present. Refer to the Power Map for details.

Estimated power deltas of each SoC load between different configurations is shown in Table below.

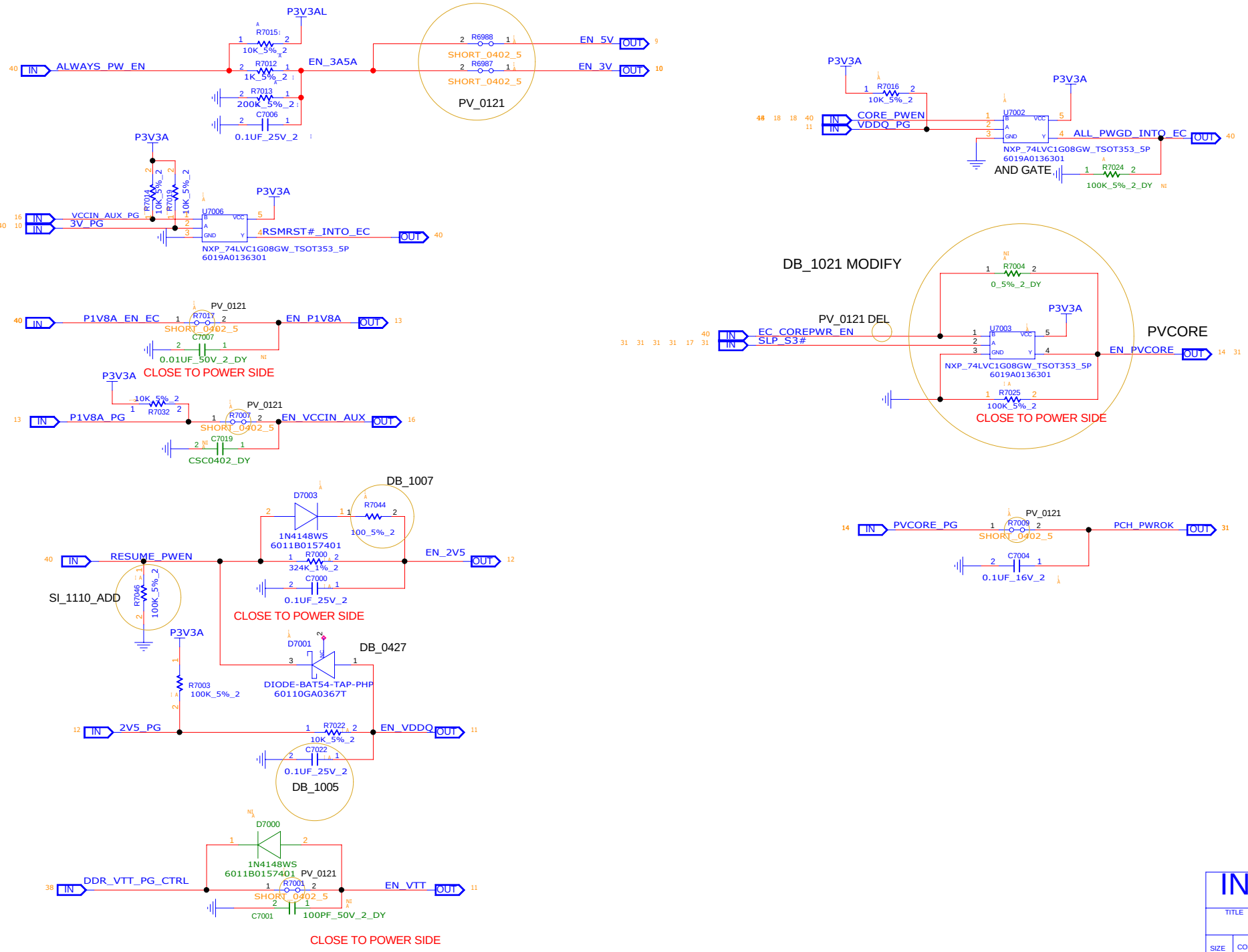
C_{SS}(pF)	Soft-Start Time (μs) 10% to 90%, V_{BIAS}=5V, C_L=0.1μF, C_{IN}=1μF, R_L=10Ω, Typical values are at T_A=25°C						
	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=1.8V	V_{IN}=1.5V	V_{IN}=1.2V	V_{IN}=1.05V	V_{IN}=0.8V
0	112	73	53	49	45	42	38
220	492	322	197	170	146	132	128
330	685	450	270	230	198	180	145
470	911	598	355	307	263	233	188
1000	2030	1280	749	635	538	470	388
2200	4360	2740	1574	1336	1118	1014	797
4700	8780	5540	3218	2696	2289	2037	1624
10000	19060	12011	6862	5700	4806	4301	3410

Note: The table Contains soft-start time values measured on a typical device. The soft-start times shown are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and EN pin is asserted high.

INVENTEC

MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	
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FIGURE 11-29. ICE LAKE NON-DSX SYSTEM ARCHITECTURE BLOCK DIAGRAM

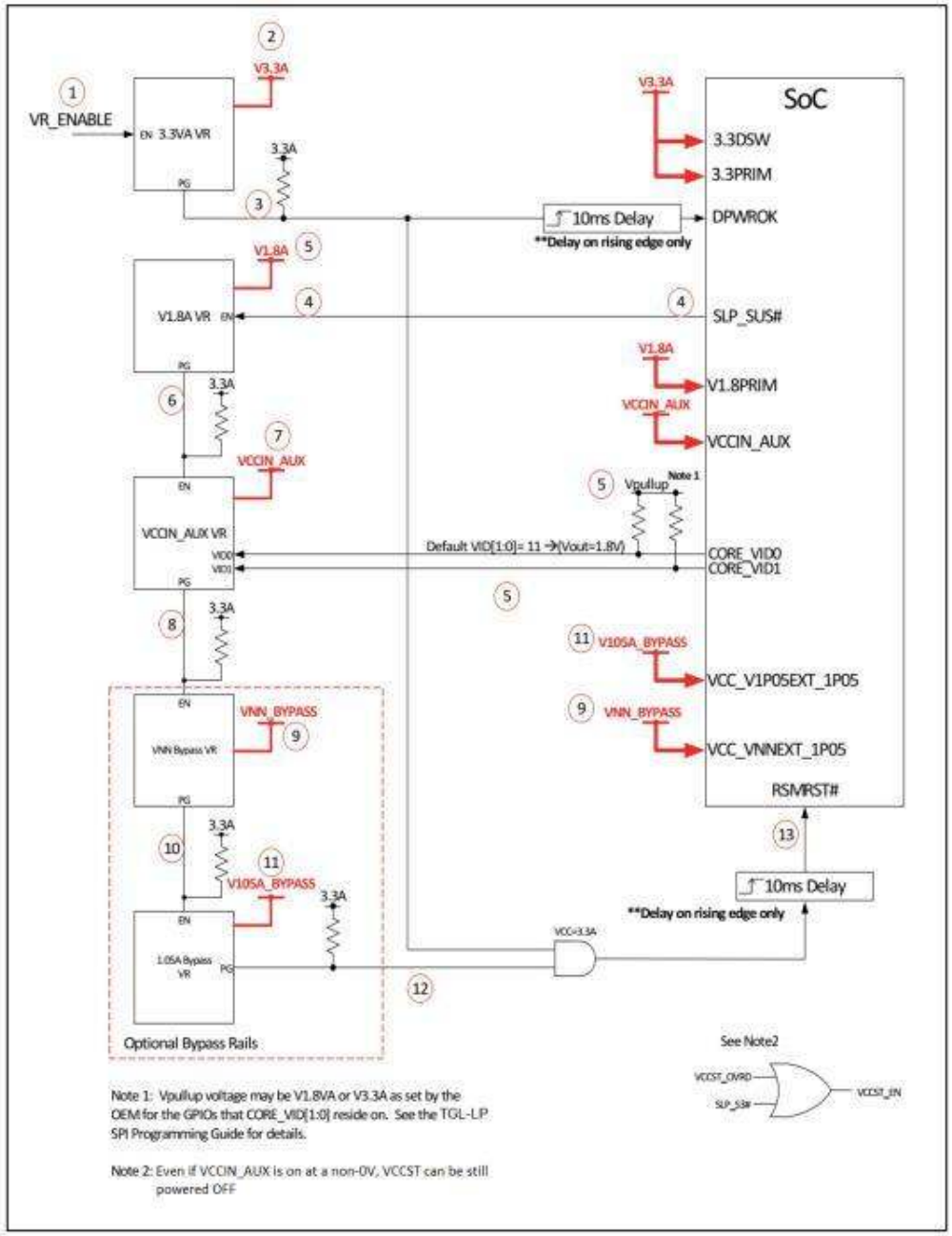

Table 195. System with M3 State Supported

Rails	SKUs	S0/M0 3	C102	S0ix/M-off[4]	S3/M3	S3/M -off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G31
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P0SEXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
V1.8M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	ON [13]	ON [13]	OFF[6]	OFF[6]	OFF	No Power
VCCSTG	All	ON	OFF [2]	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON[11]	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON[11]	OFF[14]	OFF[14]	OFF[14]	OFF[14]	OFF	No Power

Notes:
1. The state of the system without RTC well powered can also be considered G3.
2. VCCSTG can be turned off when the processor is in C10
3. S0/M0 state includes all Package C-states from C0-C10
4. Assume SLP_S0# and CPU_C10_GATE# have asserted from the PCH
5. V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not use directly by the CPU/PCH, and are not present on non-M3 supported systems
6. VCCST and VCCSTG can remain powered during S4 and S5 power states for board cost optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Platform Debug and Test Hooks chapter for more details.
7. NA
8. NA
9. VCCSTG is allowed to be ramped to 0V during S0 only when CPU_C10_GATE# is asserted. Specific exit latency targets are required when this feature is implemented. If VCCSTG power gating is not supported on the platform (shared with VCCST), VCCSTG is allowed to stay ON during S0ix and S3 states. Note that merging power rails may reduce power optimization opportunities on the platform.
10. For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3
11. This supply is expected to be 0V during states where SLP_S0# is asserted. It may be left on during this condition, but the SoC will not achieve it is lowest power consumption. Specific power up latencies apply when exiting this state. Applicable to form factors with battery only (ie. AIO)Optional depending platform design; ON if AC is present
12. NA
13. For additional power savings in S3, Refer Power Sequencing Timing Diagrams Legacy Signals on page 416.
14. VCCIN_AUX may be ON in these power states if required by the SOC.

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01		
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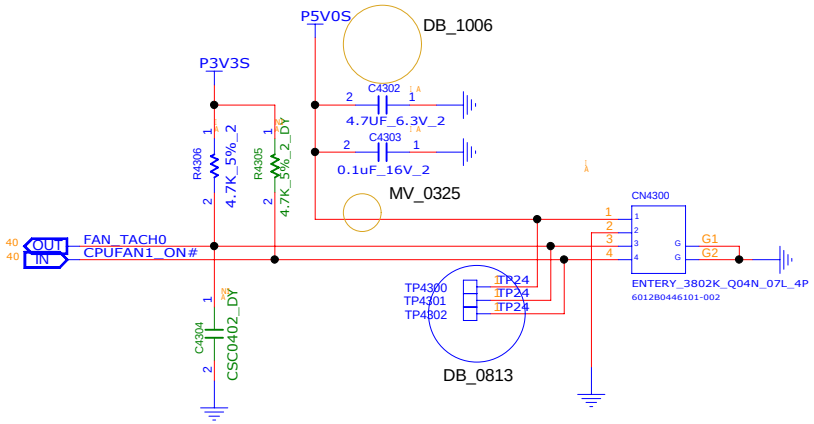
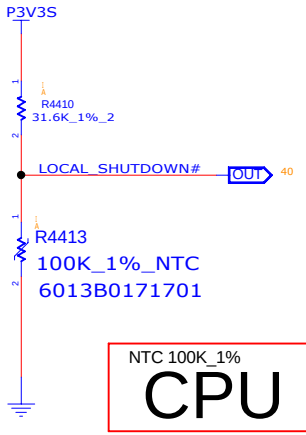
FAN & THERMAL

FOR BIG CORE USE

VER.04_20171011

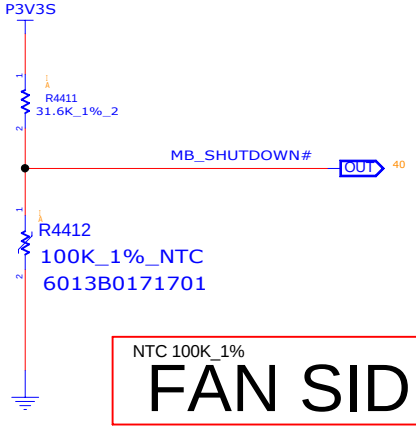
FAN CONN





NTC 100K_1%

CPU SIDE



NTC 100K_1%

FAN SIDE

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION THERMAL & FAN		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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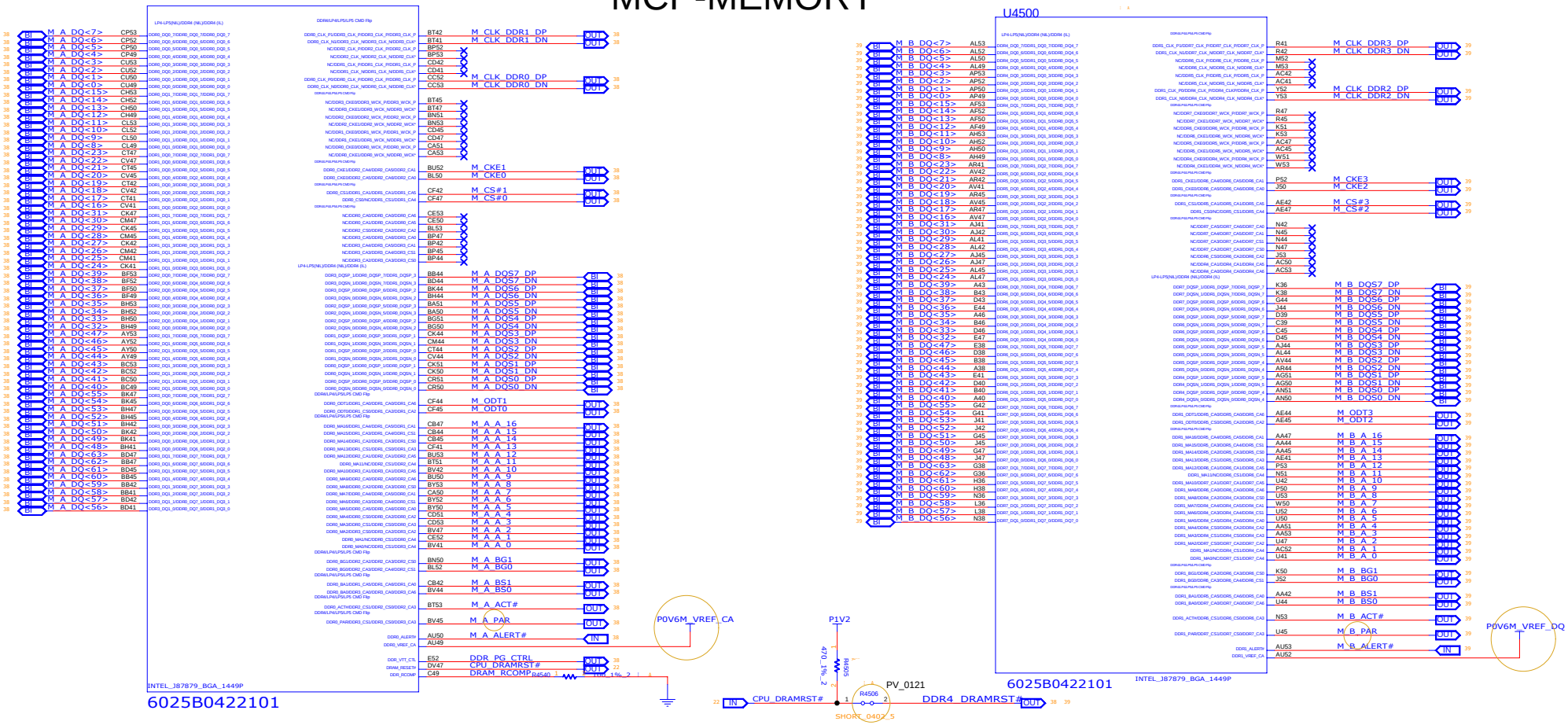
MCP-MEMORY



REFERENCE:4500~4949

CHANGE ID	XXX	DATE	
PCB P/N	60.xxxxx.xxxx	PCB VER	2.1

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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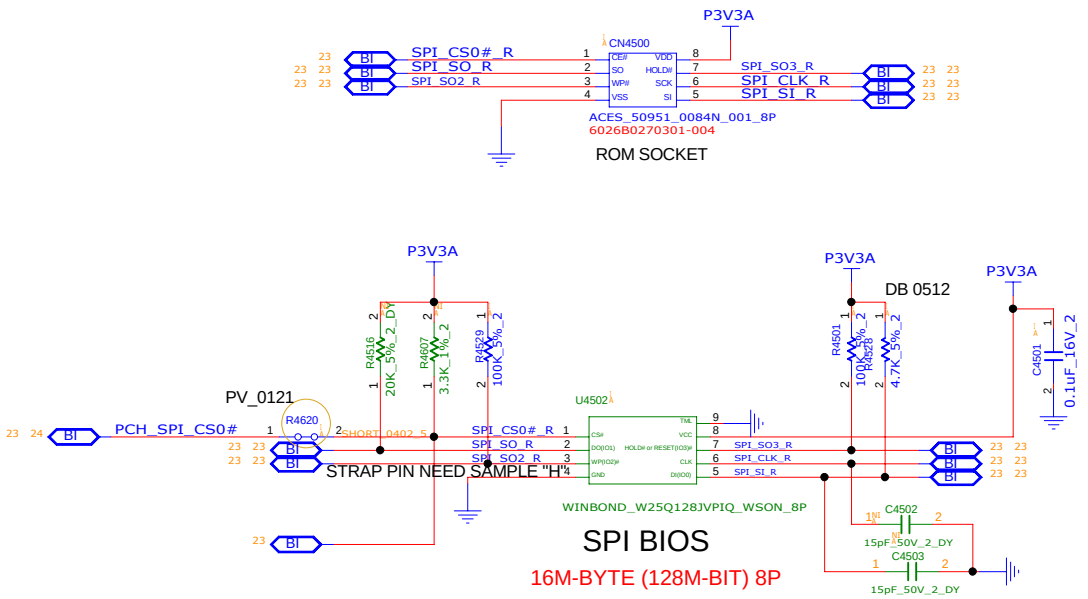
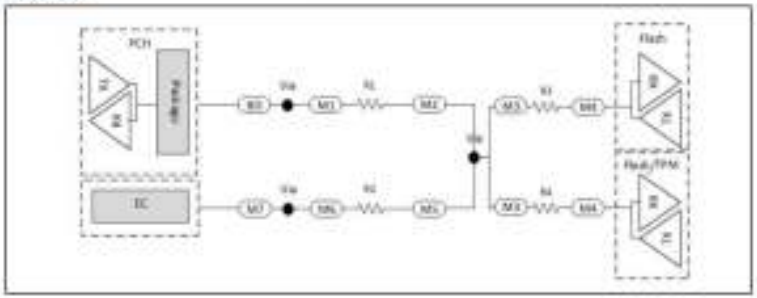
CORE - SPI ROM

SPI FLASH & SOCKET CO-LAYOUT

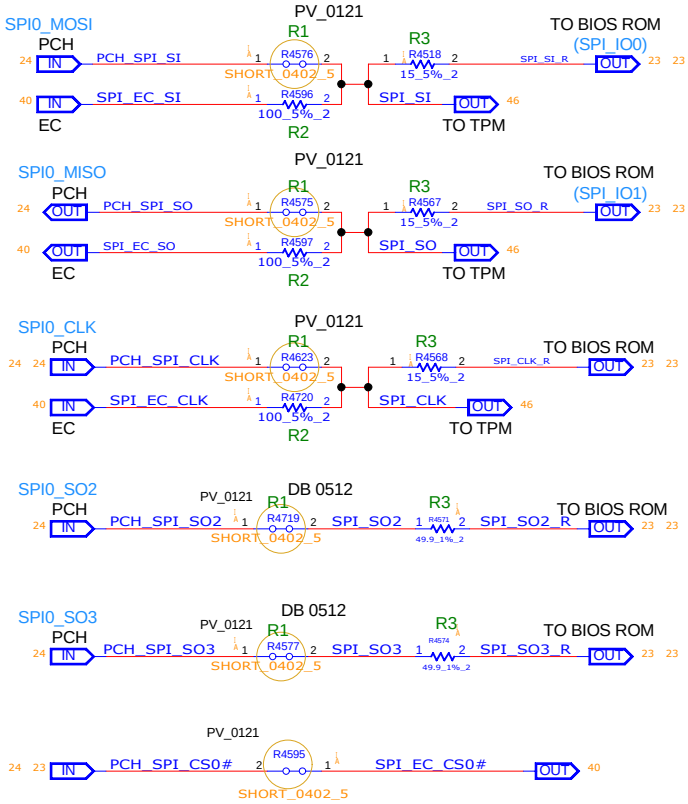


PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
S SOIC-8 208-mil	128M-bit	W25Q128JVSIQ	25Q128JVSQ
F SOIC-16 300-mil	128M-bit	W25Q128JVFIQ	25Q128JVFQ
P WSON-8 6x5-mm	128M-bit	W25Q128JVPIQ	25Q128JVPQ
E WSON-8 8x6-mm	128M-bit	W25Q128JVEIQ	25Q128JVEQ
B[1] TFBGA-24 8x6-mm (5x5 Ball Array)	128M-bit	W25Q128JVBIQ	25Q128JVBQ
C[1] TFBGA-24 8x6-mm (6x4 Ball Array)	128M-bit	W25Q128JVCIQ	25Q128JVCQ

Figure 6-84. SPI0 2-Load(1 Flash and 1 Flash/1 TPM) EC G3 Flash Sharing with Wire-OR Topology



INTEL#572907



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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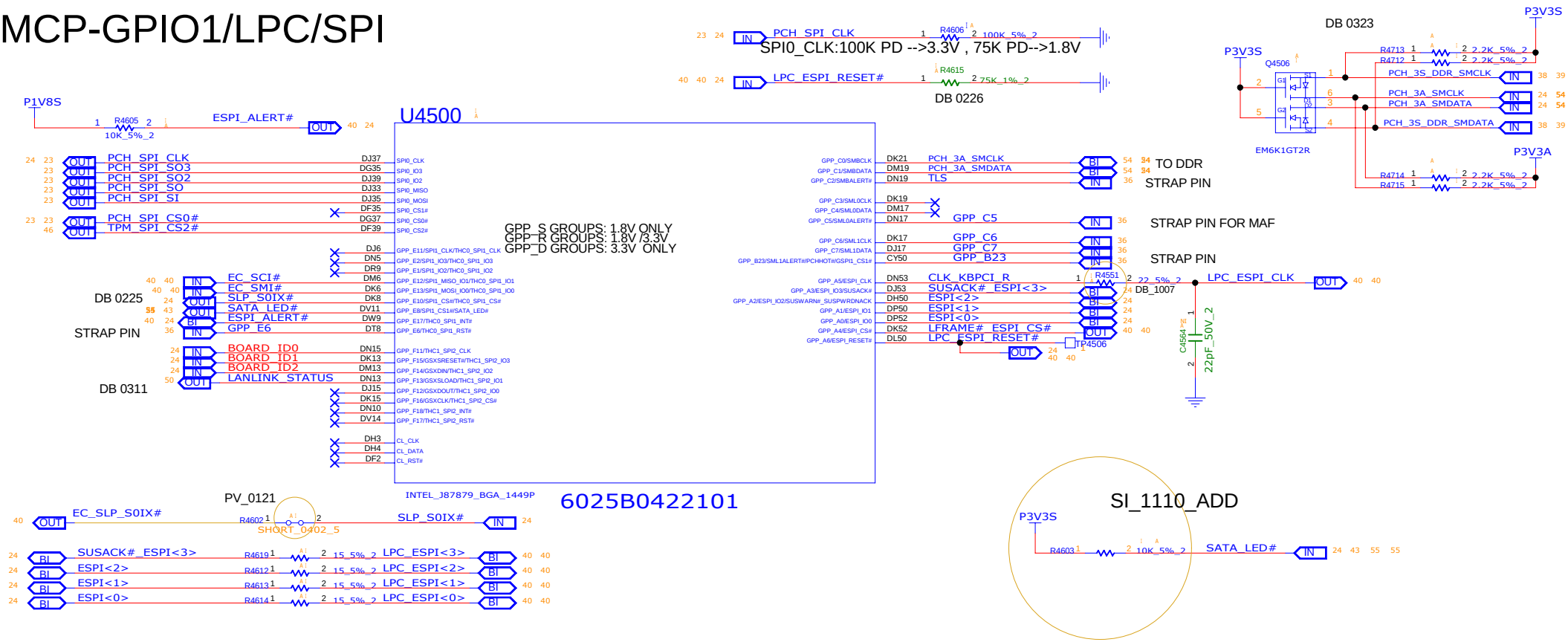
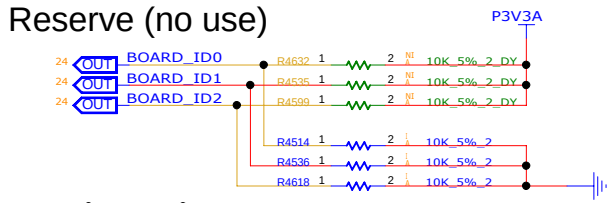
MCP-GPIO1/LPC/SPI



Reserve (no use)



BOARD_ID0	RESERVED	RESERVED
R4632	MOUNT	OPEN
R4514	OPEN	MOUNT
	3V	0V

BOARD_ID1	I3 CPU	I5 & I7 CPU
R4535	MOUNT	OPEN
R4536	OPEN	MOUNT
	3V	0V

BOARD_ID2	RESERVED	RESERVED
R4599	MOUNT	OPEN
R4618	OPEN	MOUNT
	3V	0V

DB 1012 UPDATE

REFERENCE:4500~4949

SCI / SMI# and NMI

SCI capability is available on all GPIOs, while SMI and NMI capability is available on only select GPIOs.

Below are the PCH GPIOs that can be routed to generate SMI# or NMI:

- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0], GPP_E[16:13]

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
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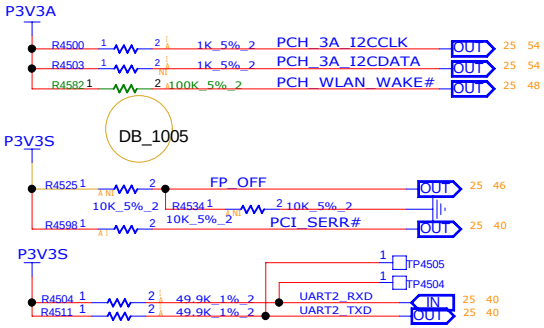
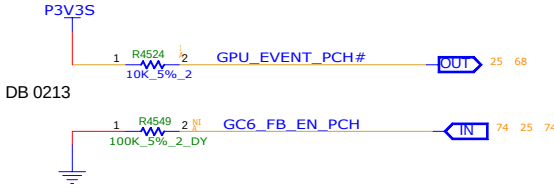
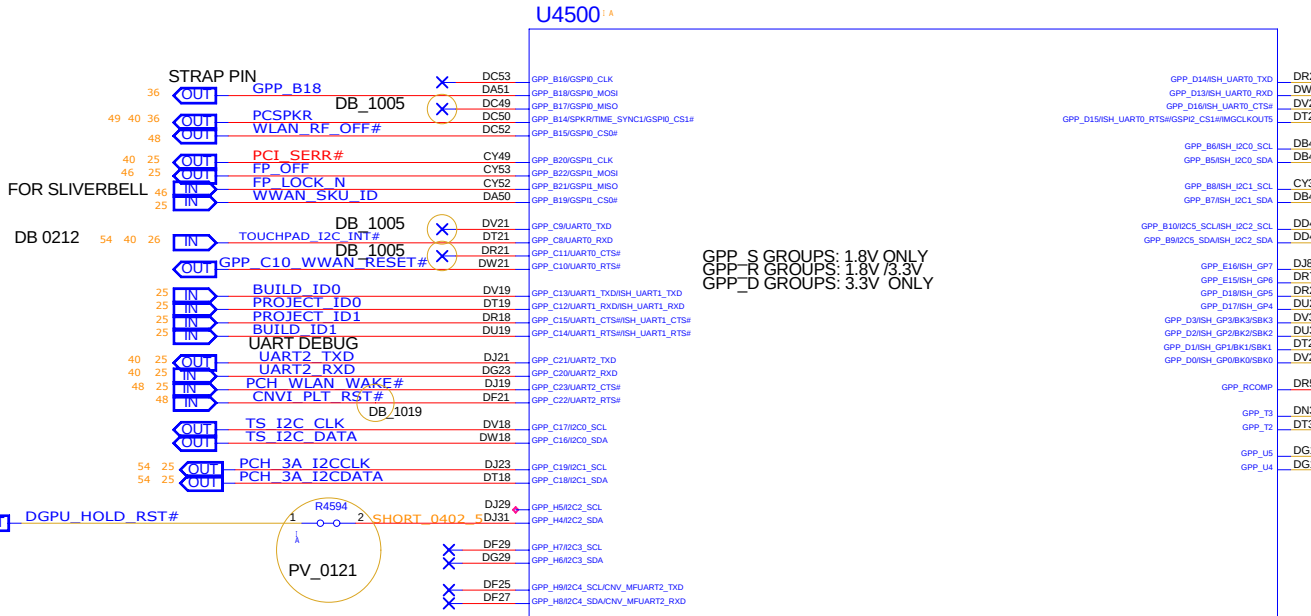
MCP-GPIO2/I2C/UART

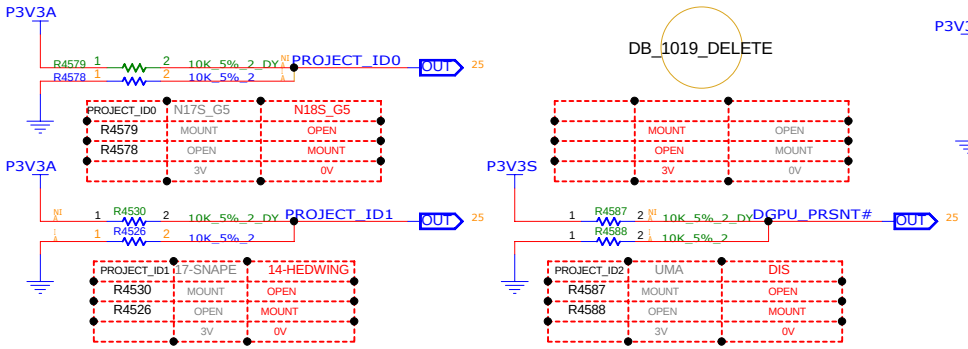
REFERENCE:4500~4949

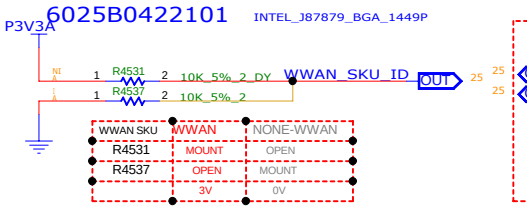


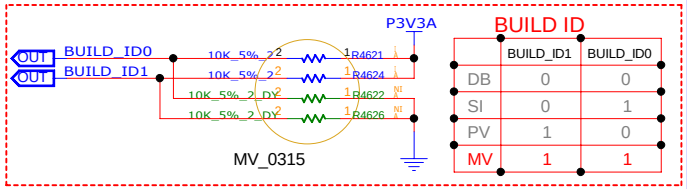


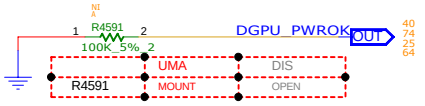
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0], GPP_E[16:13]











INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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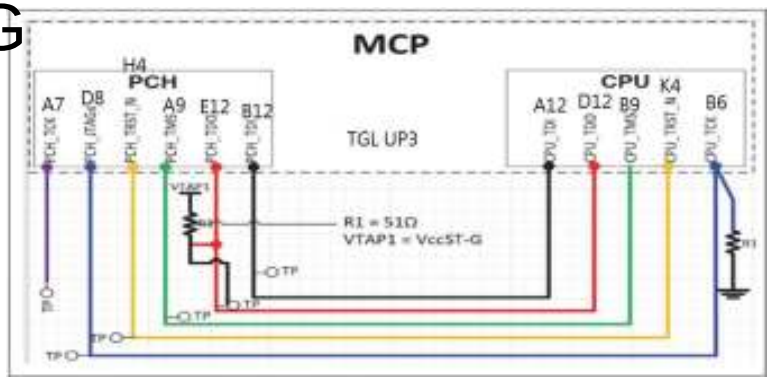
MCP-MISC/HDA/JTAG



DB 0505

P3V3S

P1V8S

U4504

DMIC_CLK_LS_PCH

DMIC_CLK_R_PCH

NXP_74AVC1T45GW_SOT363_6P

DB_1007

PVCCST

DB_1026

R4604 1K_5%_2 CATERR#

R4569 1K_5%_2 CPU_THERMTRIP#

P3V3A

R4718 10K_5%_2 TOUCHPAD_I2C_INT#

PVCCSTG

CPU_PROCHOT#

R4515 499_1%_2

R4517 1K_5%_2

C4514 47PF_50V_2

CATERR#

H_PECI

CPU_PROCHOT#_R

CPU_THERMTRIP#

PROC_RCOMP

PCH_RCOMP

STRAP PIN

DBG_PMODE

CPU_RTD3_HDD

DB 0212

STRAP PIN

GPP_H2

GPP_H1

GPP_H0

U4500

INTEL_J87879_BGA_1449P

6025B0422101

TP4517

TP4518

TP4519

TP4520

H_TRST#

H_TMS

H_TDO

H_TDI

H_TCK

PCH_TCK

H_TRST#

TP4516

PVCCSTG_CPU

R4717 1K_5%_2

CPU_EAR

GPP_F7

GPP_F10

STRAP PIN

STRAP PIN

PLACE NEAR CPU

H_TDO

R4716 51_5%_2

PLACE NEAR CPU

H_TCK

R4509 51_5%_2

U4500

DMIC_CLK_R_PCH

DMIC_DAT_R_PCH

R4553 0_5%_2

R4552 1K_1%_2

R4503 2K_1%_2

DB_1007

DB_1005

R4543 100K_5%_2

HDA_BITCLK_PCH R4634 33_5%_2 HDA_BITCLK

HDA_SYNC_PCH R4635 33_5%_2 HDA_SYNC

HDA_SDO_PCH R4636 33_5%_2 HDA_SDO_R

HDA_SDIN0

HDA_RST#

CNV_RF_RESET#

CNV_CLKREQ

2ND_WLAN_RF_OFF#

SNDW_RCOMP R4639 200_5%_2

R4513 RSC_0402_DY

C4558 CSC0402_DY

R4617 75K_1%_2

INTEL_J87879_BGA_1449P

6025B0422101

REFERENCE:4500~4949

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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MCP-CSI/CNV

DB_1019_DELETE

PV_0121

27 IN CNV_BRI_DT_UART0_RTS — R4585 SHORT_0402_5 — CNV_BRI_DT_UART0_RTS_R OUT 48 48

27 IN CNV_RGI_DT_UART0_TXD — R4586 SHORT_0402_5 — CNV_RGI_DT_UART0_TXD_R OUT 48 48

U4500

D22	CSI_F_DP_1		
B22	CSI_F_DN_1		
E22	CSI_F_DP_0		
D20	CSI_F_DN_0		
A20	CSI_F_CLK_P		
B20	CSI_F_CLK*		
B18	CSI_E_DP_1/CSI_F_DP_2		
A18	CSI_E_DN_1/CSI_F_DN_2		
D18	CSI_E_DP_0/CSI_F_DP_3		
E18	CSI_E_DN_0/CSI_F_DN_3		
C16	CSI_E_CLK_P		
D16	CSI_E_CLK*		
D15	CSI_C_DP_2		
E15	CSI_C_DN_2		
A15	CSI_C_DP_3		
B15	CSI_C_DN_3		
L18	CSI_C_DP_1		
N18	CSI_C_DN_1		
L20	CSI_C_DP_0		
N20	CSI_C_DN_0		
G20	CSI_C_CLK_P		
H20	CSI_C_CLK*		
H16	CSI_B_DP_1		
G16	CSI_B_DN_1		
G18	CSI_B_DP_0		
H18	CSI_B_DN_0		
L16	CSI_B_CLK_P		
N16	CSI_B_CLK*		
G14	CSI_B_DP_2		
H14	CSI_B_DN_2		
L14	CSI_B_DP_3		
N14	CSI_B_DN_3		
K14	CSI_RCOMP		
DK25	GPP_H23/IMGCLKOUT4		
DM25	GPP_H22/IMGCLKOUT3		
DN25	GPP_H21/IMGCLKOUT2		
DJ25	GPP_H20/IMGCLKOUT1		
DR30	GPP_D4/IMGCLKOUT_0/BK4/SBK4		
CNVI_WT_D1P	DK47	CNV_WT_LANE1_DP	OUT 48
CNVI_WT_D1N	DM47	CNV_WT_LANE1_DN	OUT 48
CNVI_WT_D0P	DN49	CNV_WT_LANE0_DP	OUT 48
CNVI_WT_D0N	DR49	CNV_WT_LANE0_DN	OUT 48
CNVI_WT_CLKP	DN45	CNV_WT_CLK_DP	OUT 48
CNVI_WT_CLKN	DN47	CNV_WT_CLK_DN	OUT 48
CNVI_WR_D1P	DU43	CNV_WR_LANE1_DP	IN 48
CNVI_WR_D1N	DV43	CNV_WR_LANE1_DN	IN 48
CNVI_WR_D0P	DR44	CNV_WR_LANE0_DP	IN 48
CNVI_WR_D0N	DT43	CNV_WR_LANE0_DN	IN 48
CNVI_WR_CLKP	DV44	CNV_WR_CLK_DP	OUT 48
CNVI_WR_CLKN	DW44	CNV_WR_CLK_DN	OUT 48
CNVI_WT_RCOMP	DN51	CNV_WT_RCOMP R4508 150_1%_2	
GPP_F3/CNV_RGI_RSP/UART0_CTS#	DJ13	CNV_RGI_RSP_UART0_CTS	IN 48
GPP_F2/CNV_RGI_DT/UART0_TXD	DG13	CNV_RGI_DT_UART0_TXD	IN 27
GPP_F1/CNV_BRI_RSP/UART0_RXD	DF15	CNV_BRI_RSP_UART0_RXD	IN 48
GPP_F0/CNV_BRI_DT/UART0_RTS#	DF17	CNV_BRI_DT_UART0_RTS	IN 27
GPP_F5/MODEM_CLKREQ/CRF_XTAL_CLKREQ	DJ10		
GPP_F6/CNV_PA_BLANKING	DV15		
GPP_F4/CNV_RF_RESET#	DK10		

150_1%_2 R4507 CSI_RCOMP

INTEL_J87879_BGA_1449P

6025B0422101

REFERENCE #575882 V2.9

REFERENCE:4500~4949

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

MCP-PCIE/USB3/USB2

DOC:575683

PCI Express* Support

The TGL UP4/UP3 processor PCI Express* Interface is a 4-lane (x4) port. The interconnect between the TGL UP4/UP3 processor and NVMe* storage provided through the M.2 connector. In addition, it will support graphics PCIe Gen4 devices too.

Table 72. PCH PCIe* Configuration Lane Reversal Mapping

PCIe* Configuration	PCI Express* Lanes				PCI Express* Down Device or Connector Lanes
	PCIe* Controller #1	PCIe* Controller #2 PCH-LP (UP3)	PCIe* Controller #2 PCH-LP (UP4)	PCIe* Controller #3	
1x4	1	5	Not Available	9	3
	2	6	Not Available	10	2
	3	7	Not Available	11	1
	4	8	Not Available	12	0

PORT# TABLE

M2.SSD	PCIE	PCIE4
0	12	0
1	11	1
2	10	2
3	9	3

U4500

INTEL_J87879_BGA_1449P

6025B0422101

GPU

PEG_TX3_DP / PEG_TX3_DN / PEG_RX3_DP / PEG_RX3_DN

PEG_TX2_DP / PEG_TX2_DN / PEG_RX2_DP / PEG_RX2_DN

PEG_TX1_DP / PEG_TX1_DN / PEG_RX1_DP / PEG_RX1_DN

PEG_TX0_DP / PEG_TX0_DN / PEG_RX0_DP / PEG_RX0_DN

PCIE4_RCOMP_P / PCIE4_RCOMP_N — R4608 2.2K_1%_2

SATA FOR HDD

SATA_HDD_TX_DP / SATA_HDD_TX_DN / SATA_HDD_RX_DP / SATA_HDD_RX_DN

SATA FOR SSD

SI_1126_MODIFY

LAN

PCIE_LAN_TX_C_DP / PCIE_LAN_TX_C_DN / PCIE_LAN_RX_C_DP / PCIE_LAN_RX_C_DN — C4703, C4702 0.1UF_16V_2

WLAN

PCIE_WLAN_TX_C_DP / PCIE_WLAN_TX_C_DN / PCIE_WLAN_RX_C_DP / PCIE_WLAN_RX_C_DN — C4701, C4700 0.1UF_16V_2

SSD

PCIE_SSD4_TX_C_DP / PCIE_SSD4_TX_C_DN / PCIE_SSD4_RX_C_DP / PCIE_SSD4_RX_C_DN — C4704, C4705 0.22UF_16V_2

PCIE_SSD3_TX_C_DP / PCIE_SSD3_TX_C_DN / PCIE_SSD3_RX_C_DP / PCIE_SSD3_RX_C_DN — C4706, C4707 0.22UF_16V_2

PCIE_SSD2_TX_C_DP / PCIE_SSD2_TX_C_DN / PCIE_SSD2_RX_C_DP / PCIE_SSD2_RX_C_DN — C4708, C4709 0.22UF_16V_2

PCIE_SSD1_TX_C_DP / PCIE_SSD1_TX_C_DN / PCIE_SSD1_RX_C_DP / PCIE_SSD1_RX_C_DN — C4710, C4711 0.22UF_16V_2

USB3.0 PORT R1

USB3_R1_TX_DP / USB3_R1_TX_DN / USB3_R1_RX_DP / USB3_R1_RX_DN

USB3.0 PORT L2

USB3_L2_TX_DP / USB3_L2_TX_DN / USB3_L2_RX_DP / USB3_L2_RX_DN

USB3.0 PORT L1

USB3_L1_TX_DP / USB3_L1_TX_DN / USB3_L1_RX_DP / USB3_L1_RX_DN

BLUETOOTH

USB_WLAN_DP / USB_WLAN_DN

17 FOR ODD / 14 FOR FP

CARD READER

USB_FP_DP / USB_FP_DN

WEBCAM

USB_CARD_DP / USB_CARD_DN

USB_CAM_DP / USB_CAM_DN

USB2.0 PORT L2 MB

USB_L2_DP / USB_L2_DN

USB2.0 PORT L1 MB

USB_L1_DP / USB_L1_DN

USB2.0 PORT R1 DB

USB_R1_DP / USB_R1_DN

GPP_E0 / SATA_SSD_DET# — P3V3A

GPP_E9 — R4592 10K_5%_2 — R4539

GPP_A16

SSD_DEVSLP2 / TPM_SERIRQ#

PCIE_RCOMPP / PCIE_RCOMPN — R4510 100_1%_2

USB2_VBUSSENSE — R4701 10K_5%_2

USB2_ID — R4700 10K_5%_2

USB2_COMP — R4756 113_1%_2

REFERENCE:4500~4949

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION

Block Diagram

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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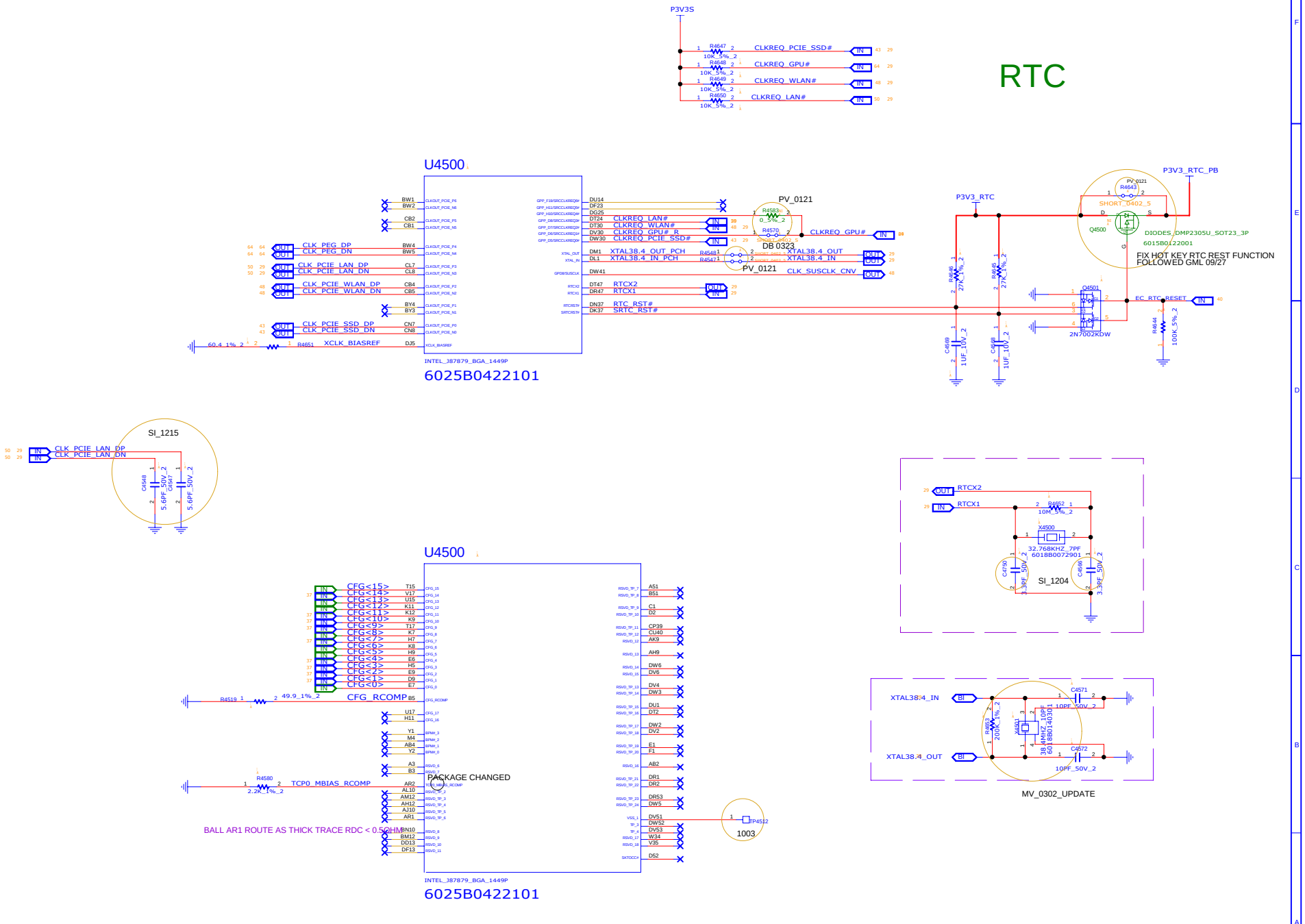
MCP-CLK/RTC/CFG



REFERENCE:4500~4949

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 29 of 77			

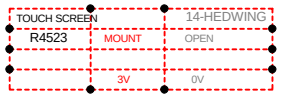
CHANGE SI	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

MCP-DDI/TCP

5.3 Display Interfaces

Table 35. DDI Ports Availability

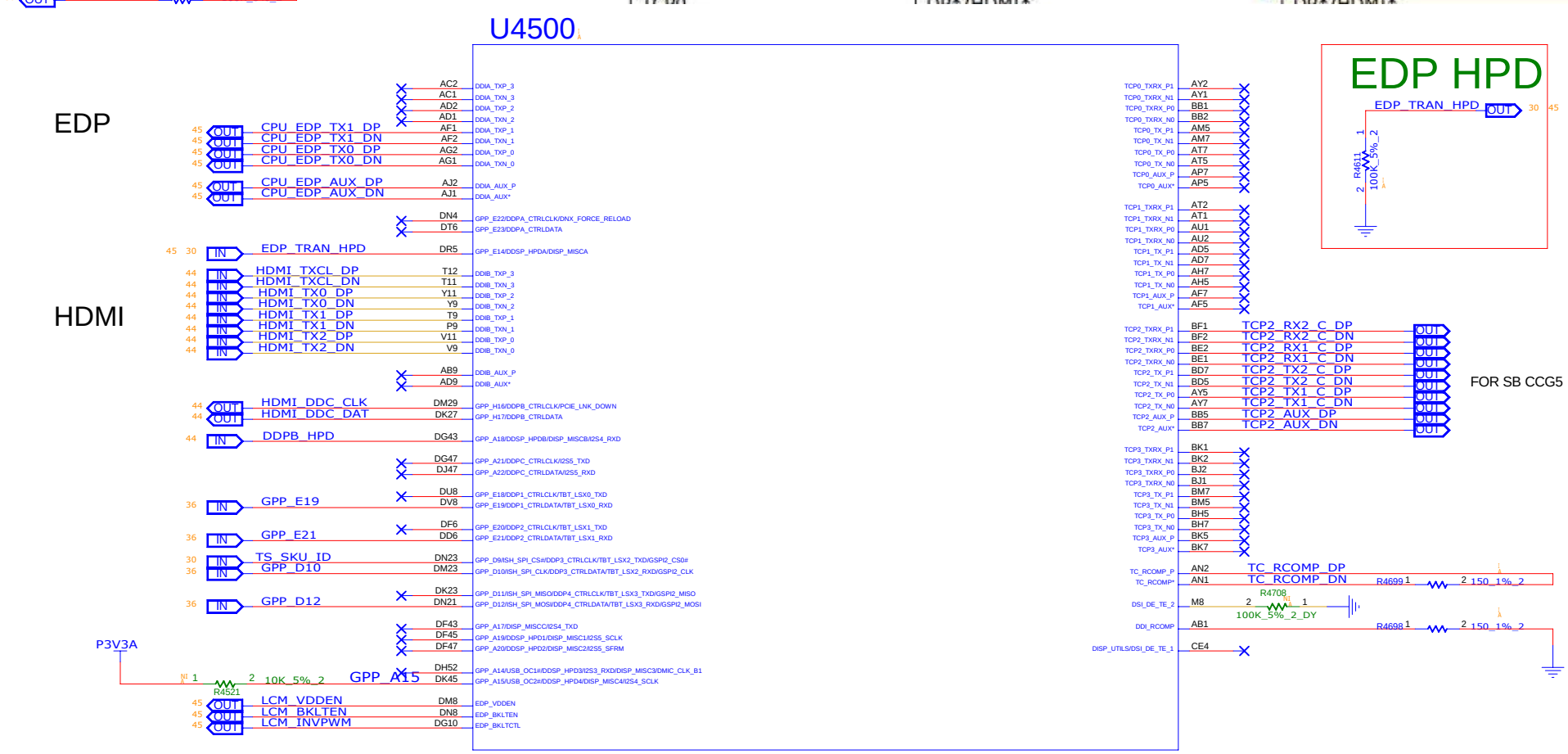
SKU	UP4 Processor Line Quad Core GT2	UP3 Processor Line Quad Core GT2
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	DP*/HDMI*/MIPI_1	DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*



H: NA
L: TOUCH

P3V3A

30 OUT TS_SKU_ID 1 R4523 2 100K_5%_2



FOR SB CCG5

EDP HPD

INTEL_J87879_BGA_1449P

6025B0422101

REFERENCE:4500~4949

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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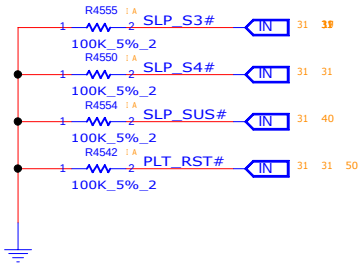
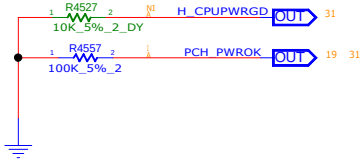
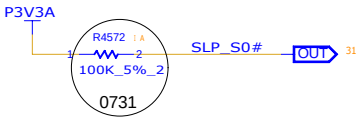
MCP-POWER MANAGEMENT

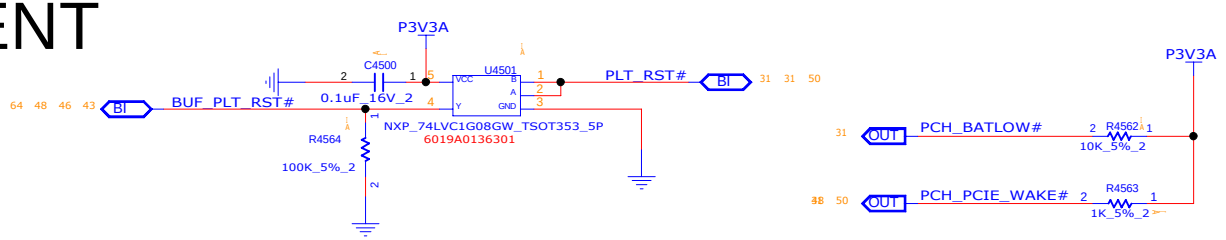
08/13

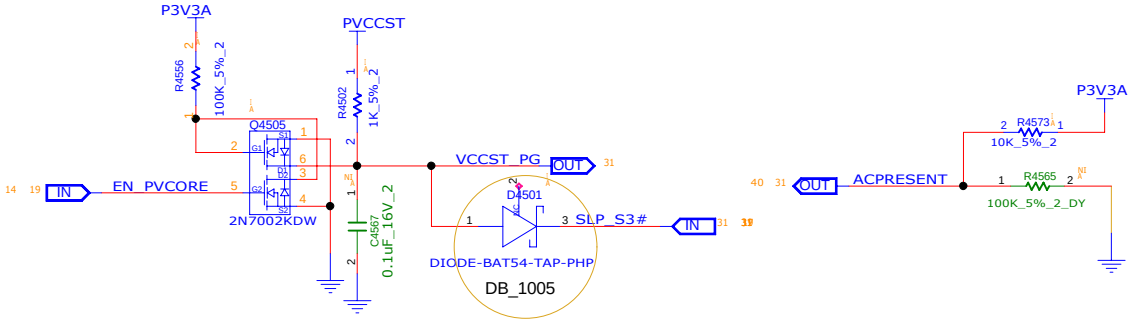
DG #607872
TABLE 102

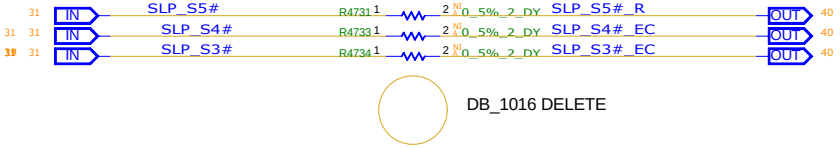


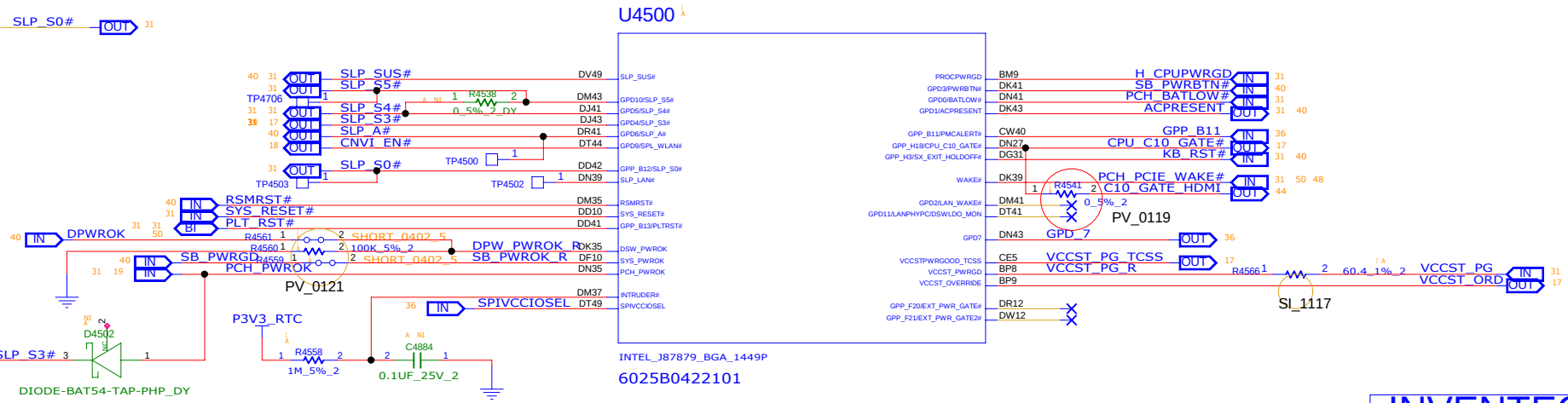












INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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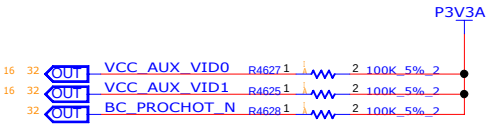
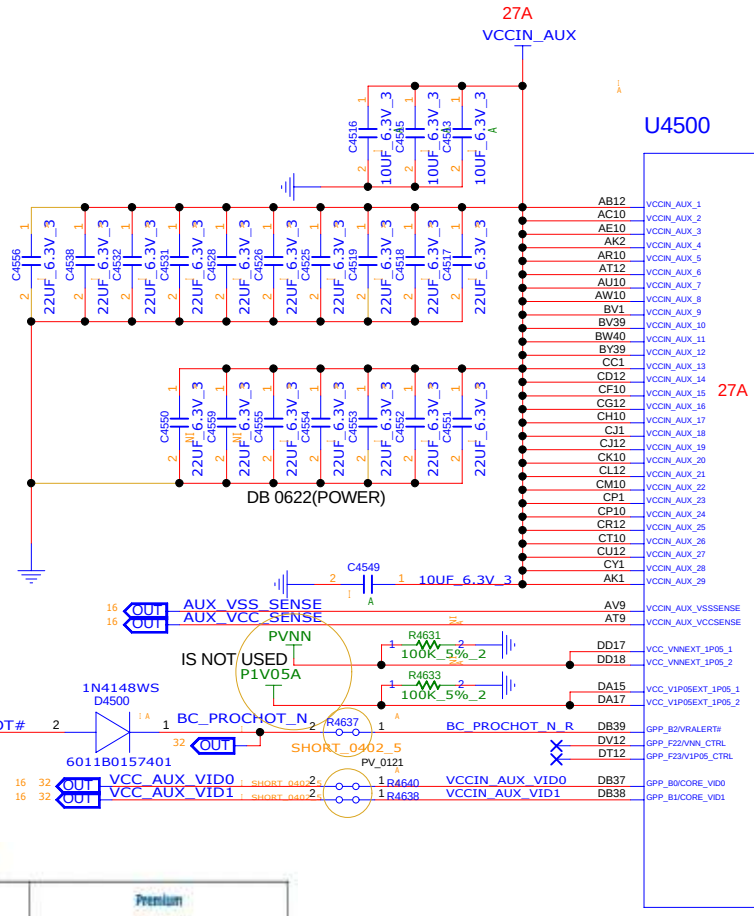
CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

MCP-POWER1

REFERENCE:4500~4949

VCCIN: 47A
VCCIN_AUX: 27A
VCCSTG: 0.3A
VCCST: 0.5A
VDD2_CPU: 3.25A
VCCPRIM_3P3: 0.202A
VCCDSW_3P3: 0.003A
VCCPRIM_1P8: 1.3A
VCCRTC: 0.005A
VCCA_CLKLDO_1P8: 0.165A





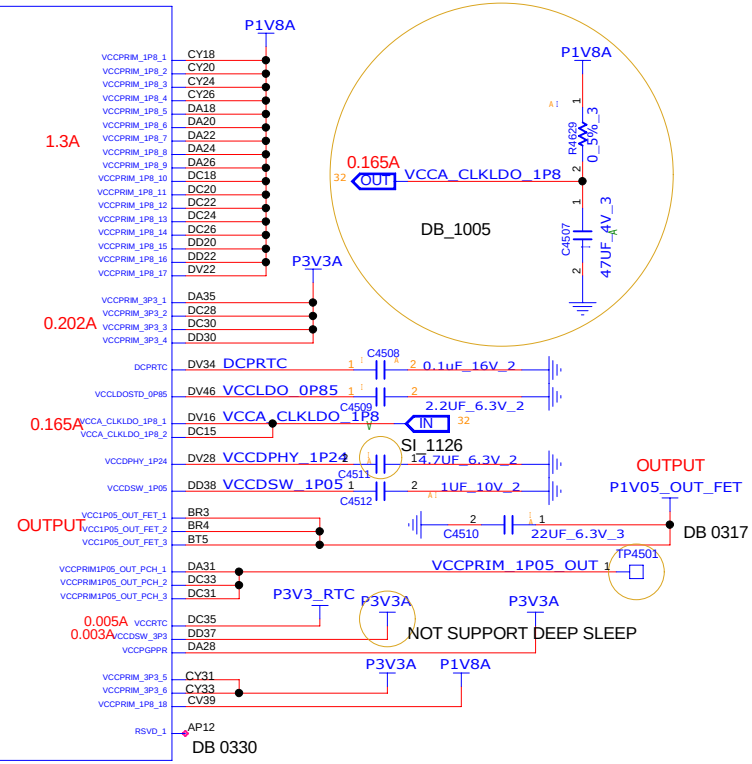
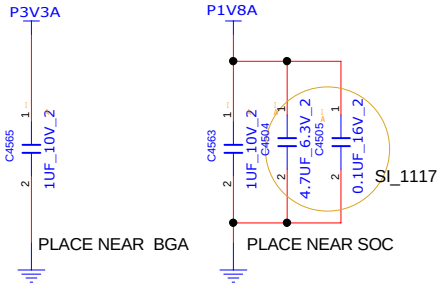


Table 372. Differences between Power Maps

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by (CPU_C10_GATE#)
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches

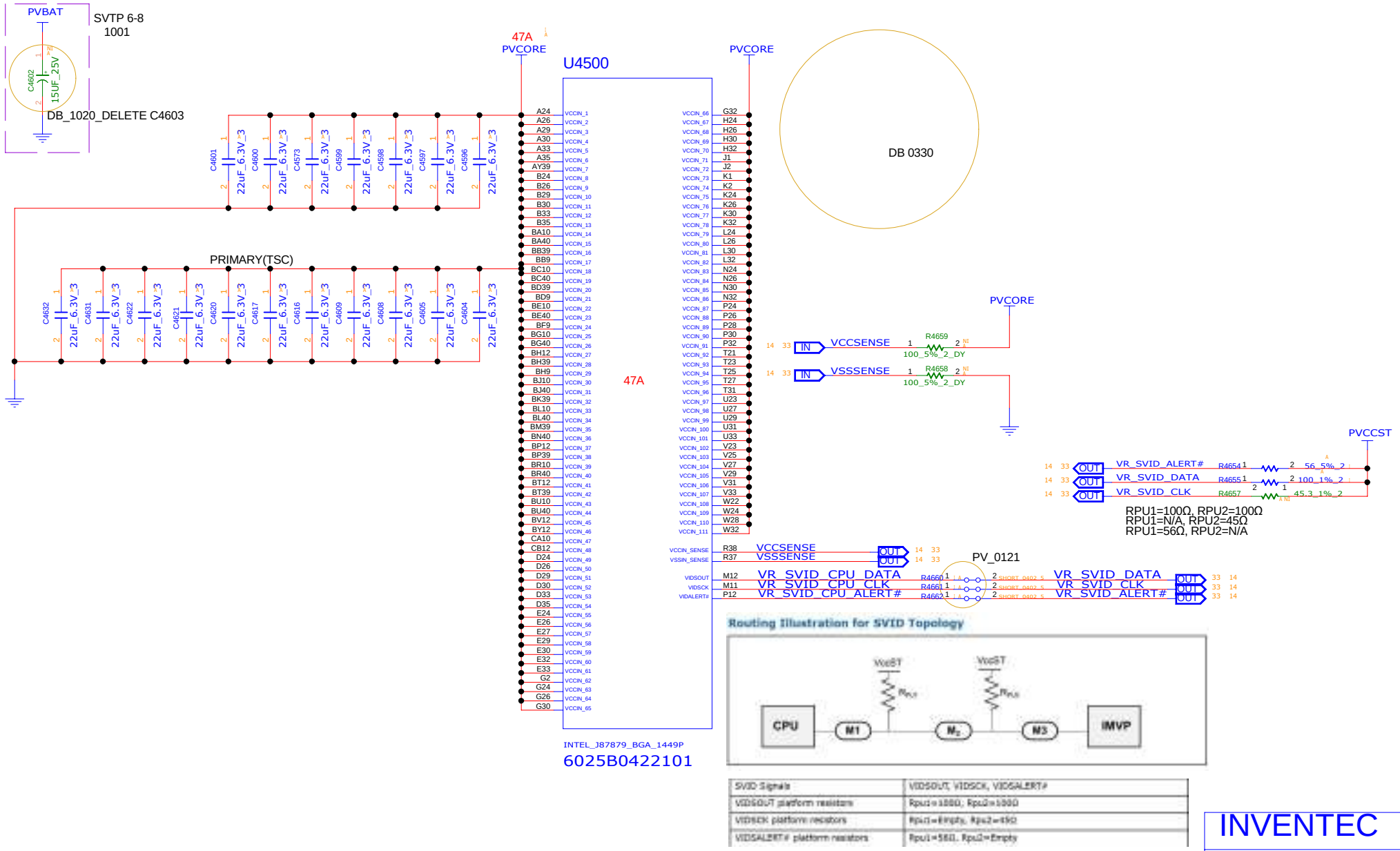
Note:
1. VCC_VNNEXT_1P05 is also known as VNN BYP
2. VCC_V1P05EXT_1P05 is also known as VP1D5 BYP
3. Other changes may be present. Refer to the Power Map for details.



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE OCT-2002	
PCB P/N 6025B0xxxxxx		PCB VER X01	
SHEET 32 of 77			

MCP-POWER2



SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty

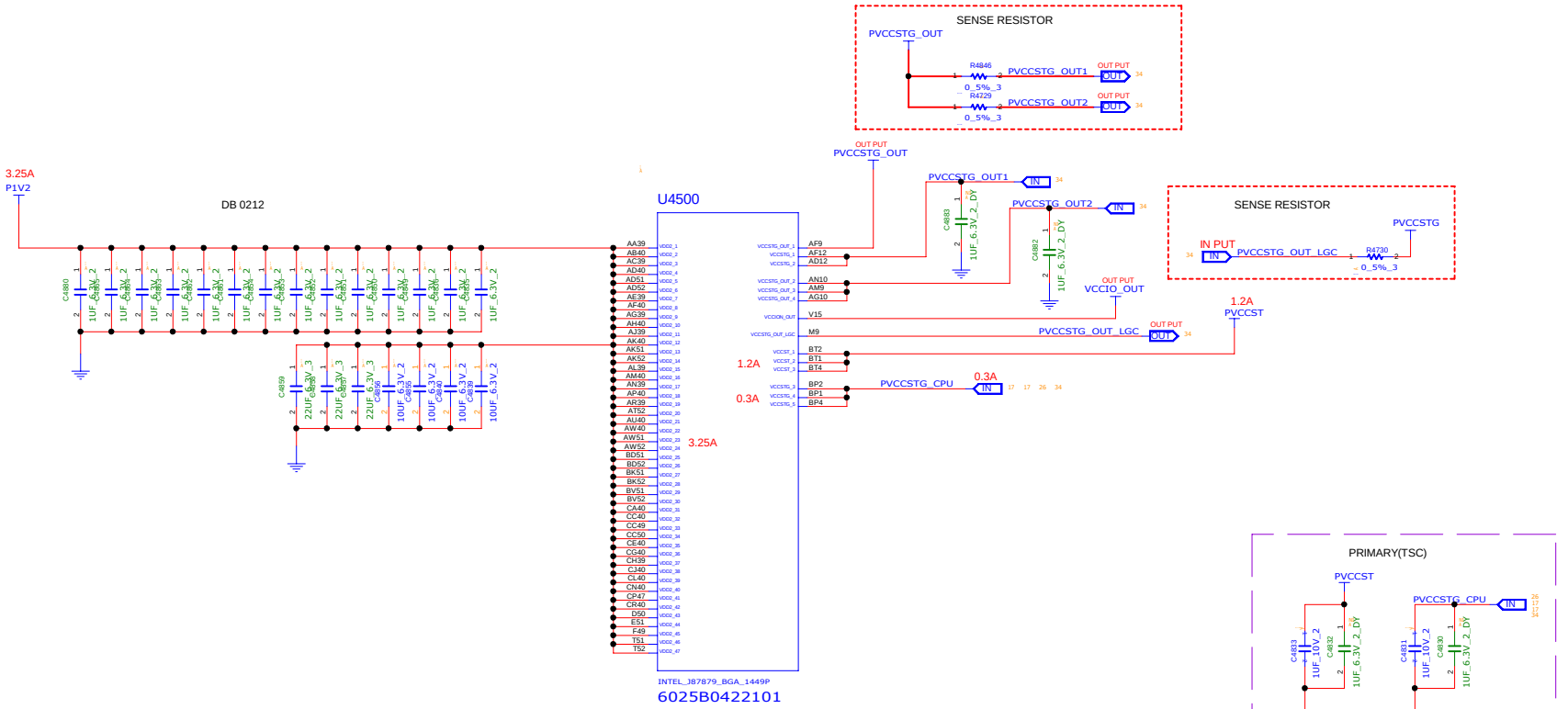
REFERENCE:4500~4949

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION		
	Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 33 of 77	

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

MCP-POWER3



REFERENCE:4500~4949

CHANGE ID	xENGx	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	xVERx

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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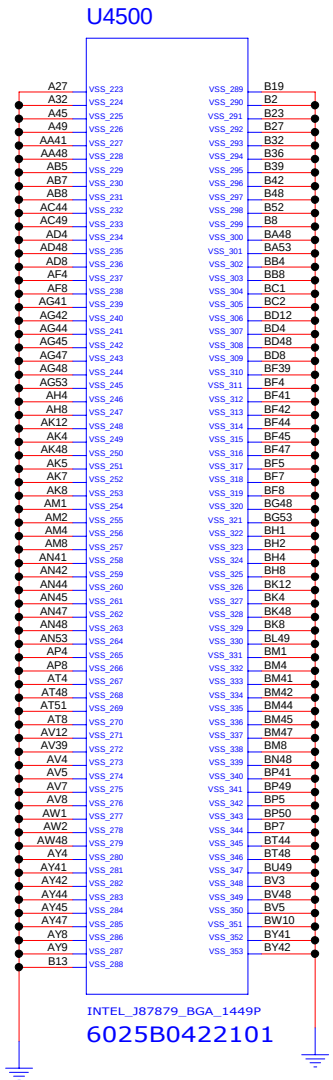
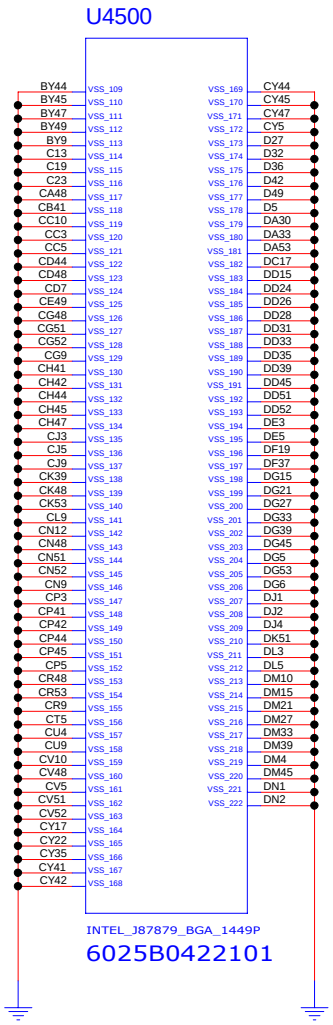
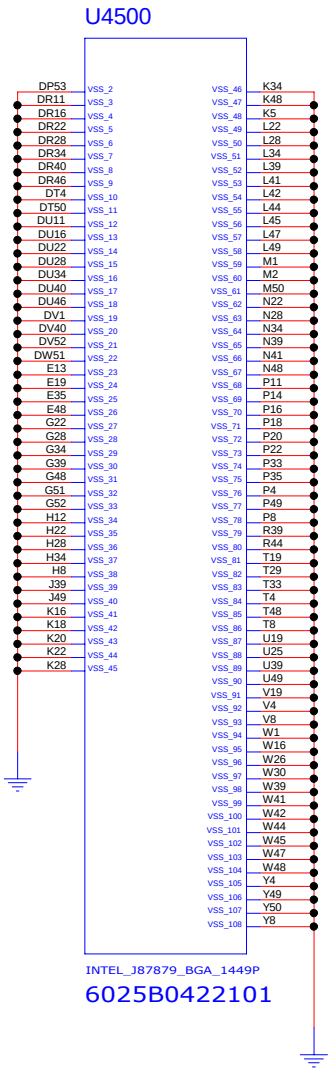
MCP-GND







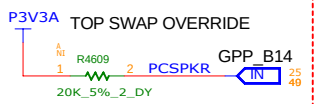
REFERENCE:4500~4949

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0		REV X01	
CHANGE by	<ENG>	DATE	21-OCT-2002	SHEET 35 of 77	
PCB P/N	60xxxxxxxxx	PCB VER	<VER>		

#576591 PIN STRAP

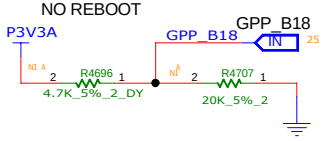
TOP SWAP OVERRIDE



THE INTERNAL PULL-DOWN IS DISABLED AFTER PCH_PWROK IS HIGH.

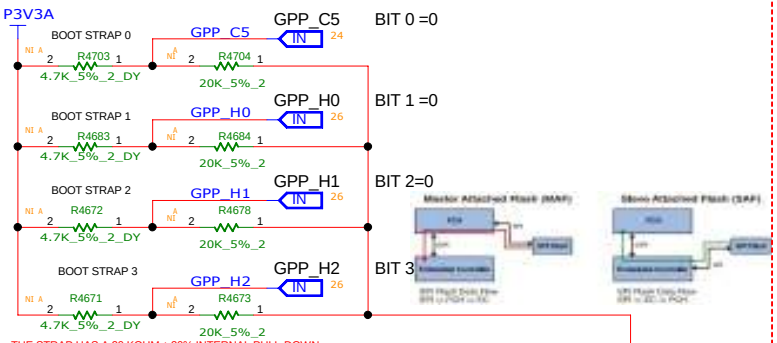
THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
0=>DISABLE "TOP SWAP" MODE. (DEFAULT)
1=>ENABLE "TOP SWAP" MODE.

NO REBOOT



THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
0=>DISABLE "NO REBOOT" MODE. (DEFAULT).
1=>ENABLE "NO REBOOT" MODE (PCH WILL DISABLE THE TCO TIMER SYSTEM REBOOT FEATURE).
THIS FUNCTION IS USEFUL WHEN RUNNING ITP/XDP.

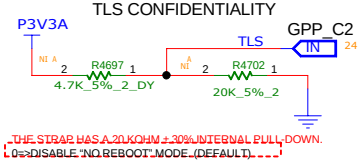
BOOT STRAP



THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
THIS STRAP IS USED IN CONJUNCTION WITH BOOT STRAP 1,2,3, (ON GPP_H0, GPP_H1, GPP_H2 RESPECTIVELY).
1000 = MASTER ATTACHED FLASH CONFIGURATION(BIOS / CSME ON ESPI ATTACHED DEVICE)

THE INTERNAL PULL-DOWN IS DISABLED AFTER RSMRST# DE-ASSERTS.

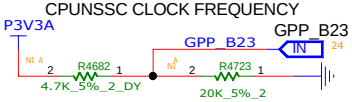
TLS CONFIDENTIALITY



THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
0=>DISABLE "NO REBOOT" MODE. (DEFAULT).

THIS FUNCTION IS USEFUL WHEN RUNNING ITP/XDP.

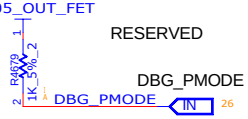
CPUNSSC CLOCK FREQUENCY



0 = 38.4 MHZ CLOCK (DIRECT FROM CRYSTAL) (DEFAULT)
1 = 19.2 MHZ CLOCK (DERIVED FROM 38.4 MHZ CRYSTAL)

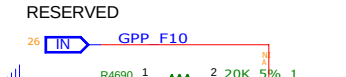
THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.

P1V05_OUT_FET



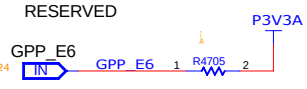
THIS STRAP SHOULD SAMPLE HIGH

RESERVED



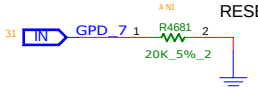
THIS STRAP SHOULD SAMPLE LOW
THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.

RESERVED



EXTERNAL PULL-UP IS REQUIRED.

RESERVED



THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
THIS STRAP SHOULD SAMPLE LOW.

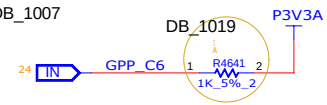
RESERVED

THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
THIS STRAP SHOULD SAMPLE LOW.

SPI0_IO3 SPI0_IO2 SPI0_MOSI

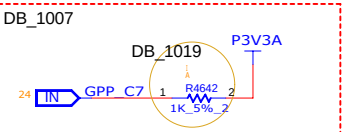
Signal	Usage	When Sampled	Comments
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 1 KOHM if pulled up to 3.3V or 750 if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 1 KOHM if pulled up to 3.3V or 750 if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 1 KOHM if pulled up to 3.3V or 750 if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

DB_1007



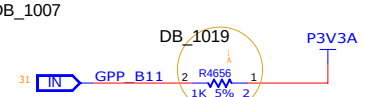
EXTERNAL PULL-UP IS REQUIRED.

DB_1007



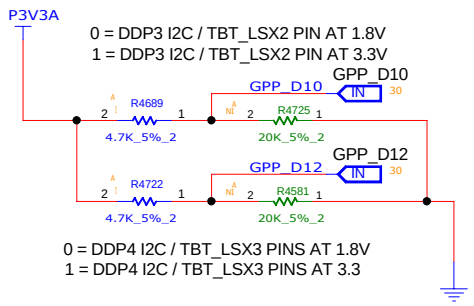
EXTERNAL PULL-UP IS REQUIRED.

DB_1007

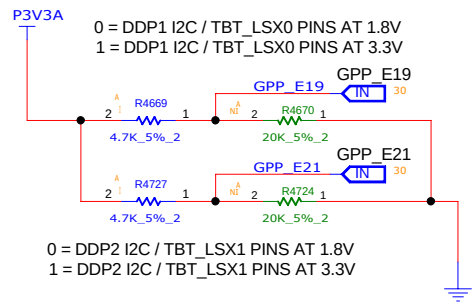


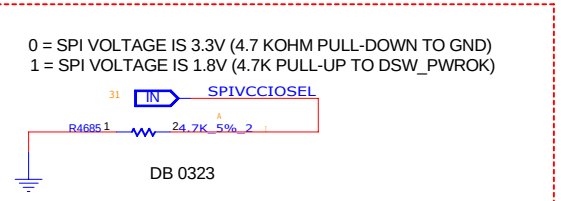
EXTERNAL PULL-UP IS REQUIRED.

THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.



THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.





INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxx		PCB VER XXX	
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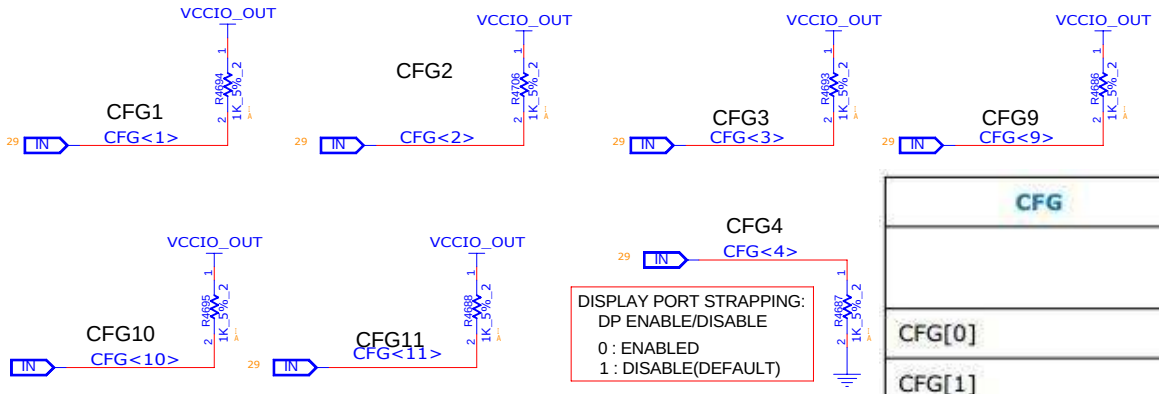
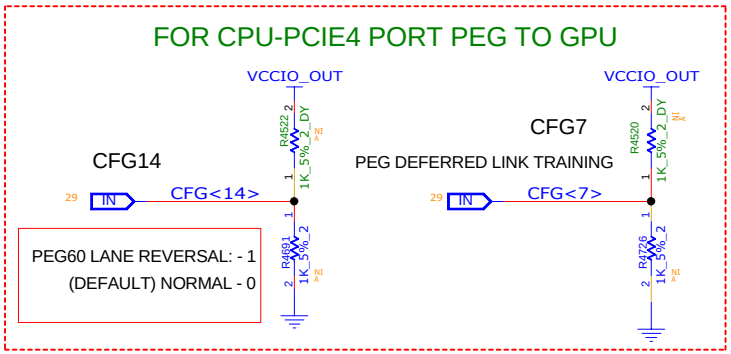
MCP-STRAPS-1

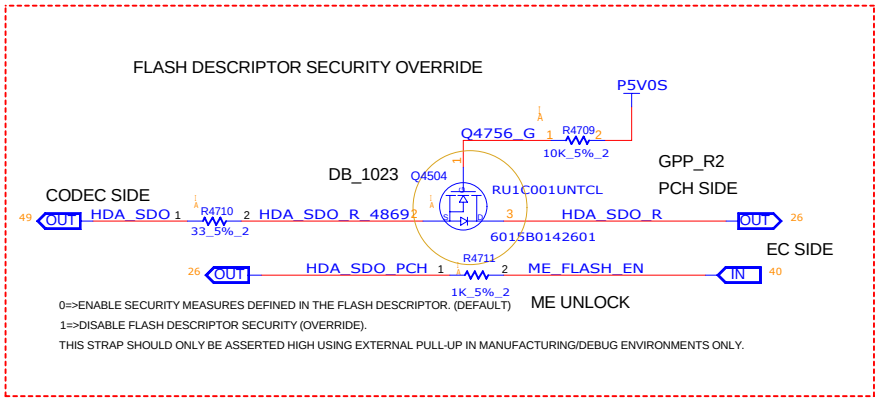
607872 TABLE62





CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

ME UNLOCK FLASH



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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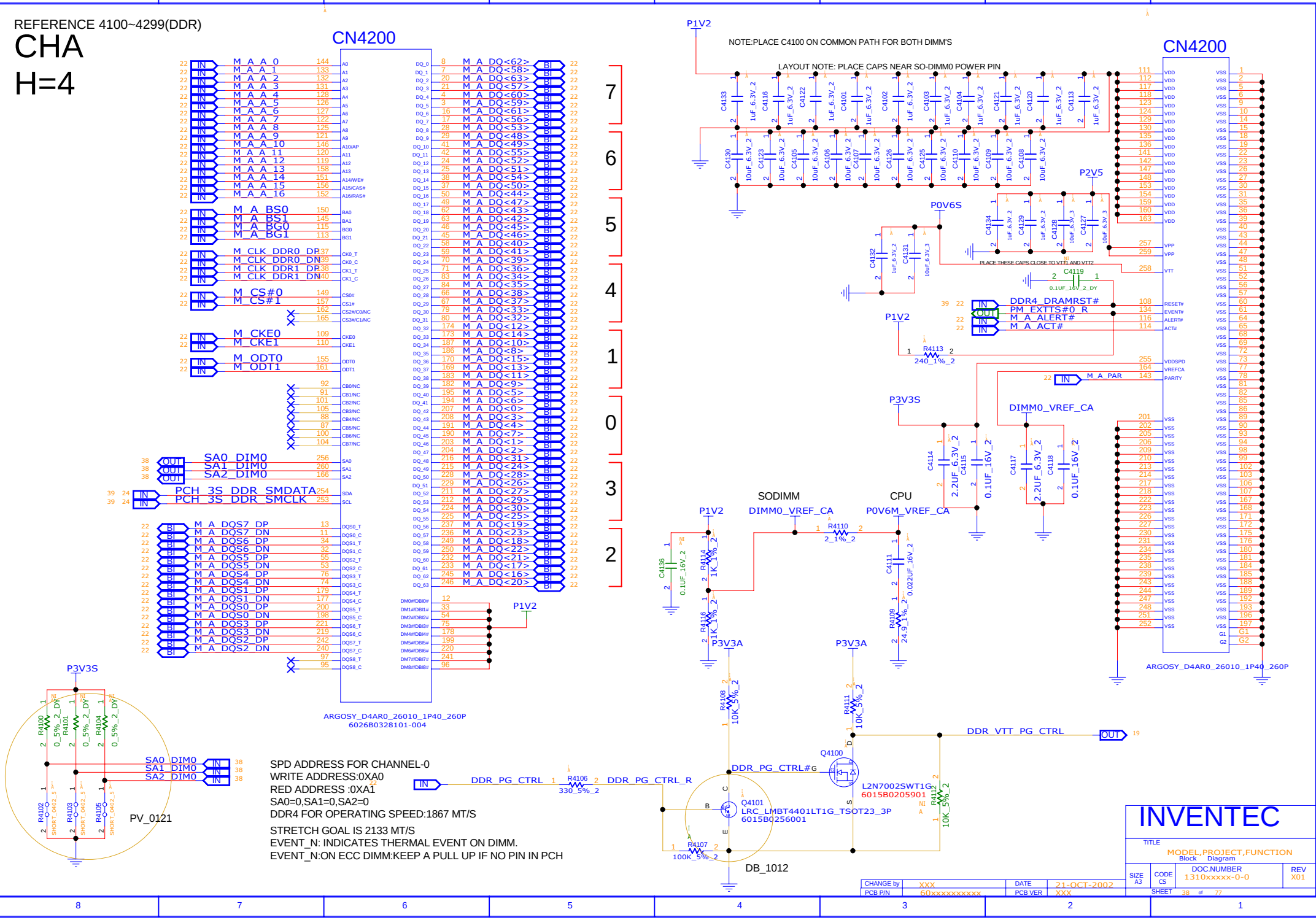
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

REFERENCE 4100~4299(DDR)

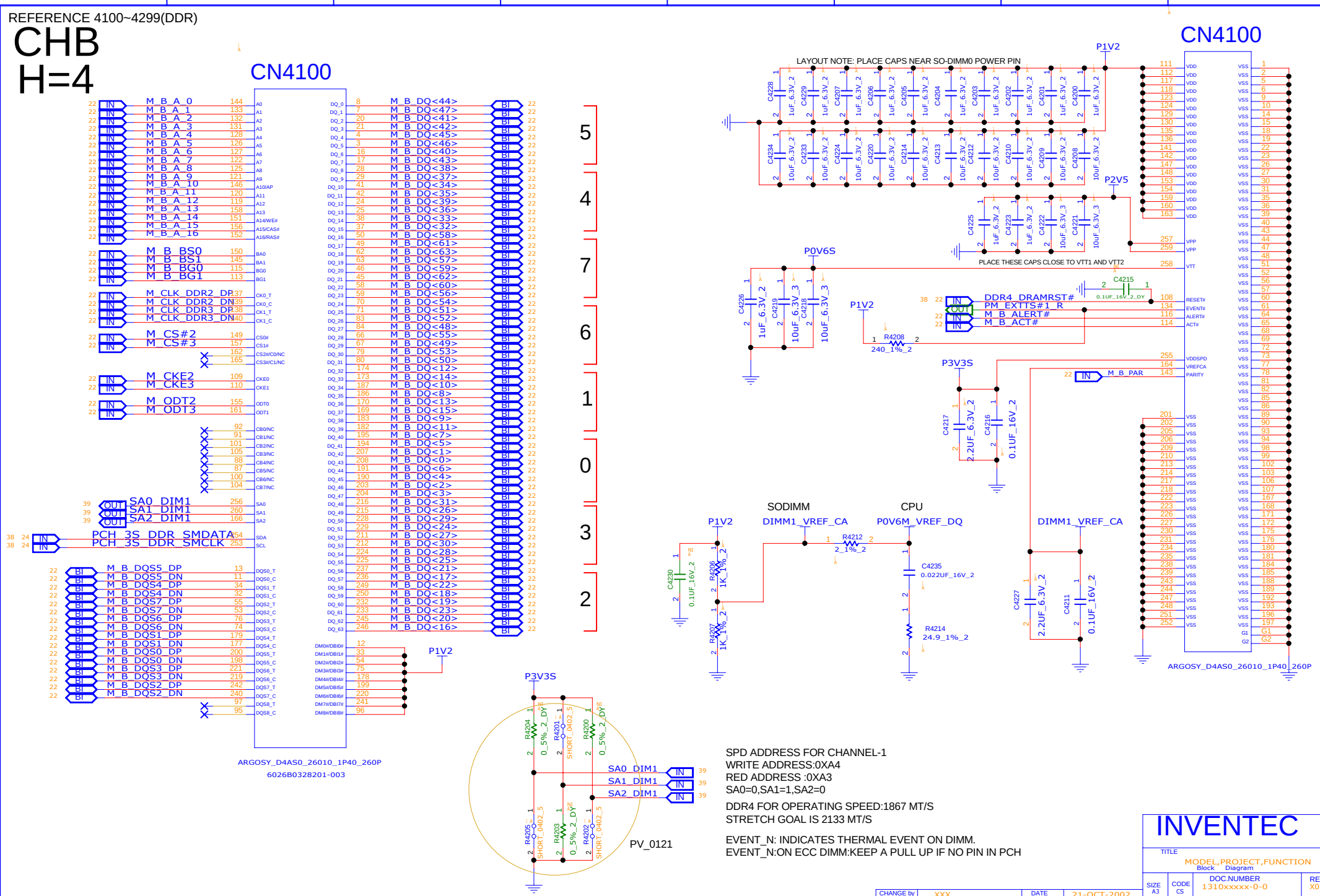
CHA

H=4



REFERENCE 4100~4299(DDR)

CHB
H=4



SPD ADDRESS FOR CHANNEL-1
WRITE ADDRESS:0XA4
RED ADDRESS :0XA3
SA0=0,SA1=1,SA2=0

DDR4 FOR OPERATING SPEED:1867 MT/S
STRETCH GOAL IS 2133 MT/S

EVENT_N: INDICATES THERMAL EVENT ON DIMM.
EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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PCB P/N 60xxxxxxxxxx		PCB VER XXX	
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EC

Location 300 ~ 389

2013EE1B

Ver.05_20120824

IT5571E_BX	VCC(1.8V OR 3.3V) PIN5 : SERIRQ/GPM6 PIN13: ESCK/GPM4 PIN7: LAD3/GPM3 PIN8: LAD2/GPM2 PIN9: LAD1/GPM1 PIN10: LAD0/GPM0 PIN6 : LFRAME#/GPM5 PIN22 : EBST#/GPD2

U300

ITE_IT5571E_128_CX_LQFP_128P

6019B1965801

SM BUS

PS/2

LPC / eSPI

GPIO

CIR

PWM

UART port

WAKE UP

EXTERNAL SERIAL FLASH

SPI ENABLE

A/D D/A

KBMX

CLOCK

Intel DS3 function support

DB 0224
DB 0226

C314
For Intel platform

noise cap

DB 0306

DB_0802_CHANGE P/N

EC DEBUG CNTR

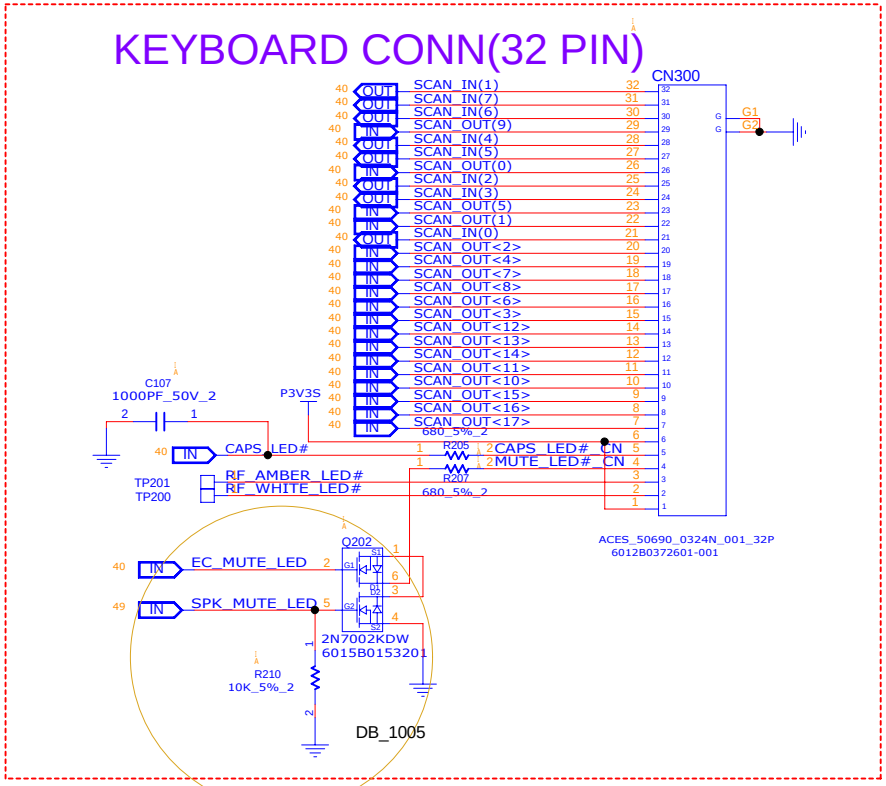
INVENTEC

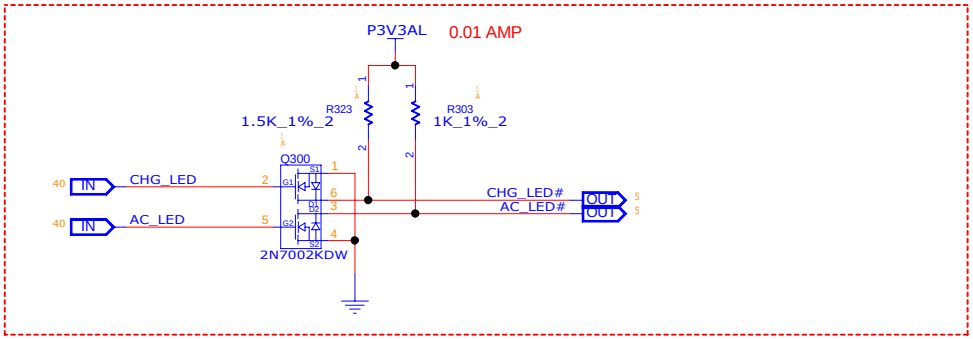
MODEL,PROJECT,FUNCTION

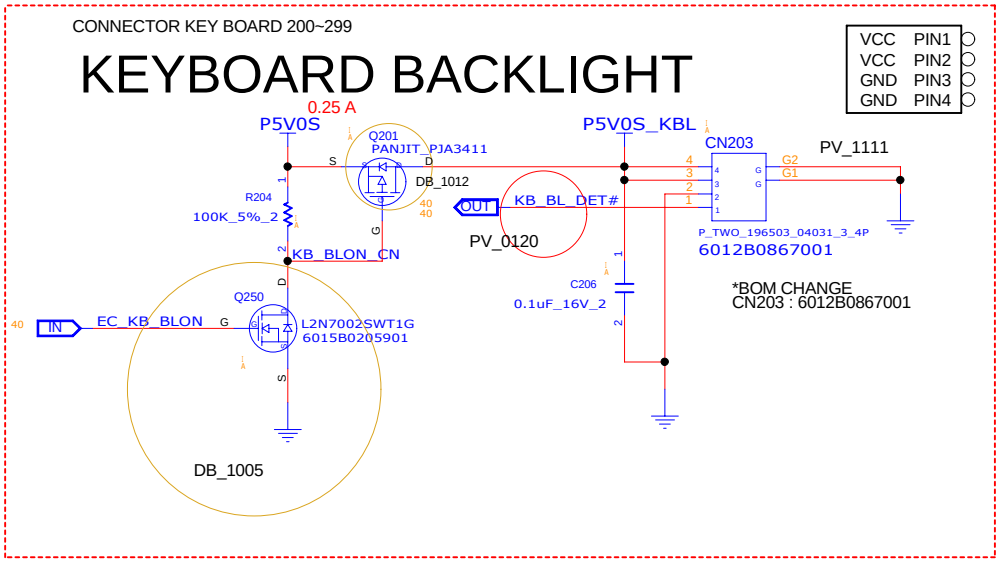
Block Diagram

KEYBOARD CONNECTOR

VER.07_20171110







INVENTEC

TITLE	MODEL,PROJECT,FUNCTION KB_CONN & LED		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>
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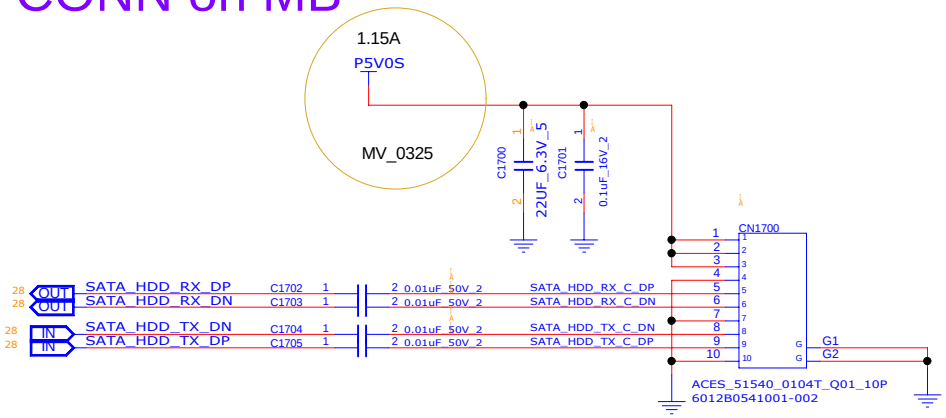
SATA HDD CABLE CONN on MB

VER.01_20170918



INVENTEC

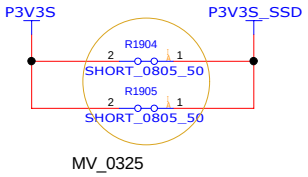
TITLE	MODEL,PROJECT,FUNCTION SATA HDD & SATA ODD		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET	of 42	77	

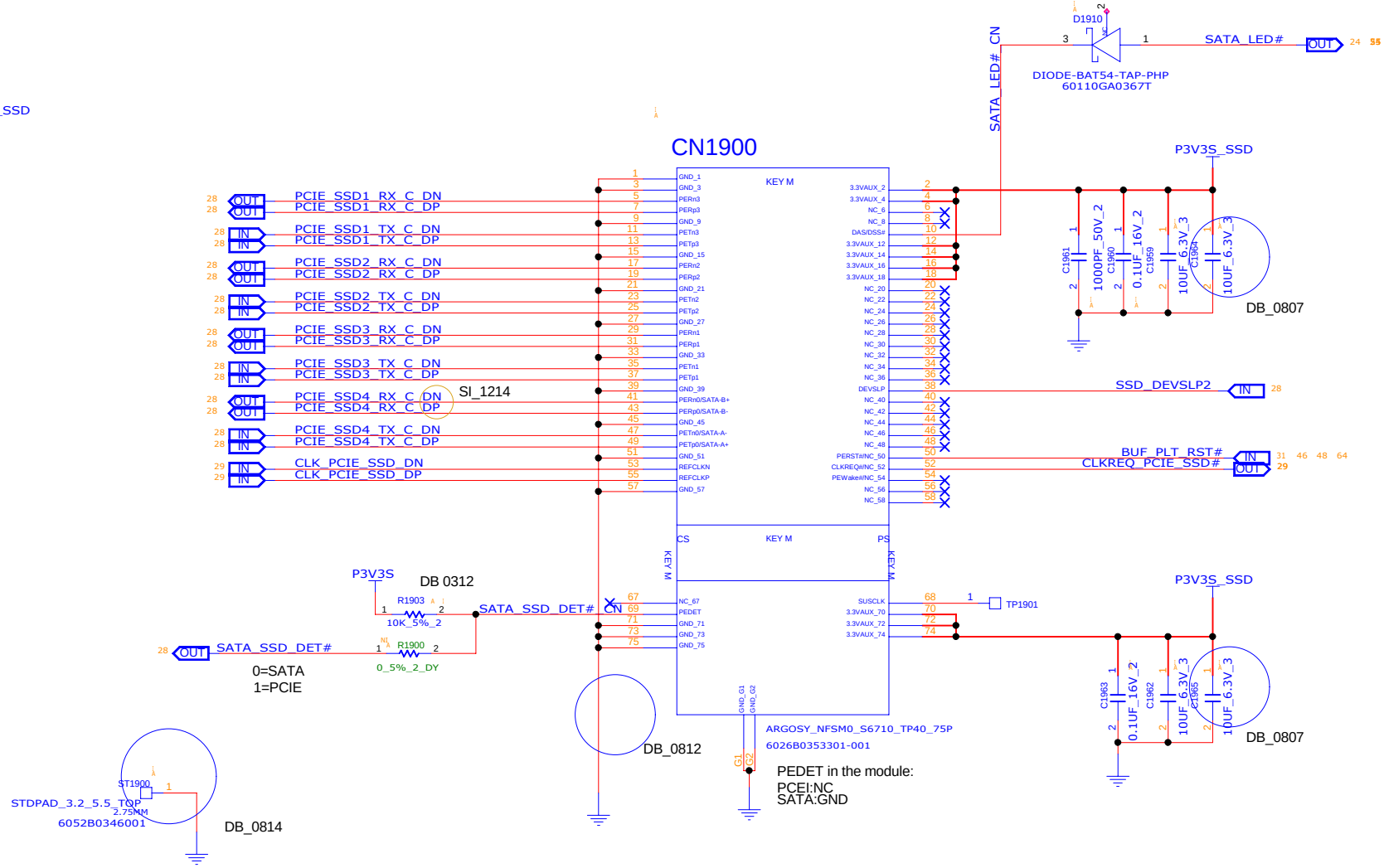
CHANGE by	XXX	DATE	
PCB P/N	60NBxxxxxxxx	PCB VER	XX

M.2 SSD

REFERENCE NUMBER:1900~1949

VER.03_20171004





CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
NGFF- SSD

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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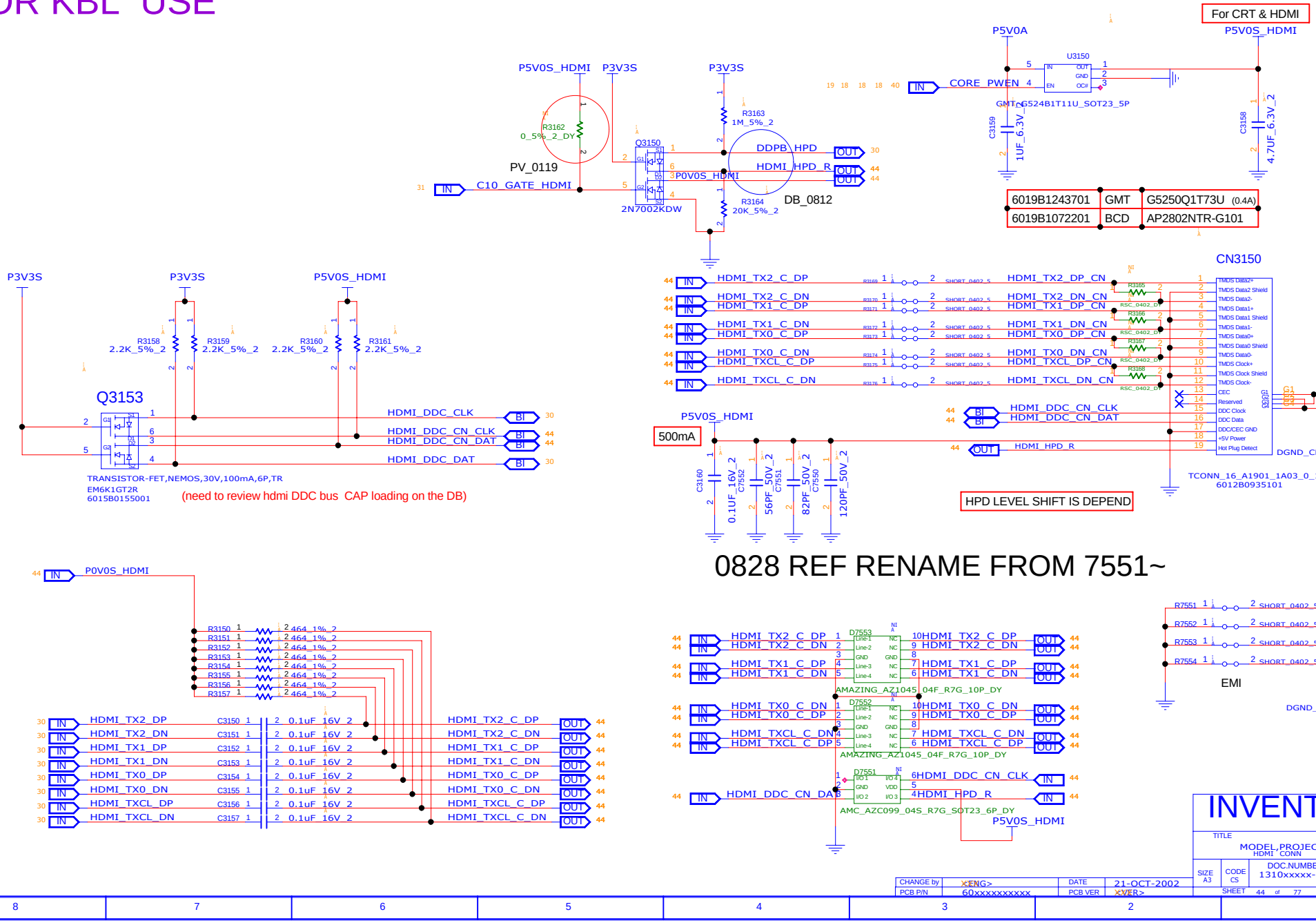
HDMI

Location 3150 ~ 3199

VER.08_20171115-2

FOR KBL USE



CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
HDMI CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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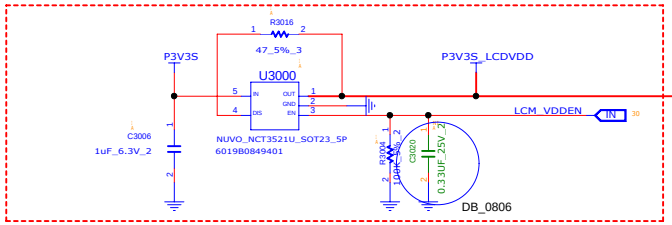
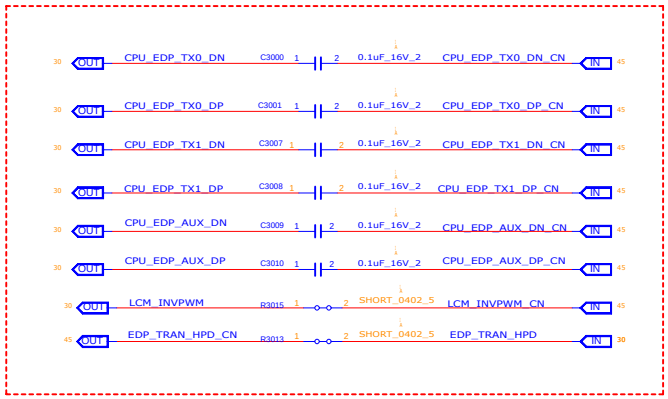
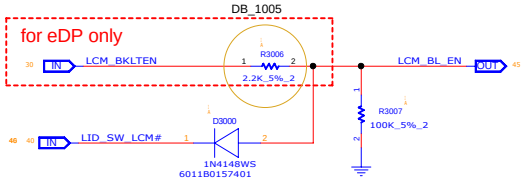
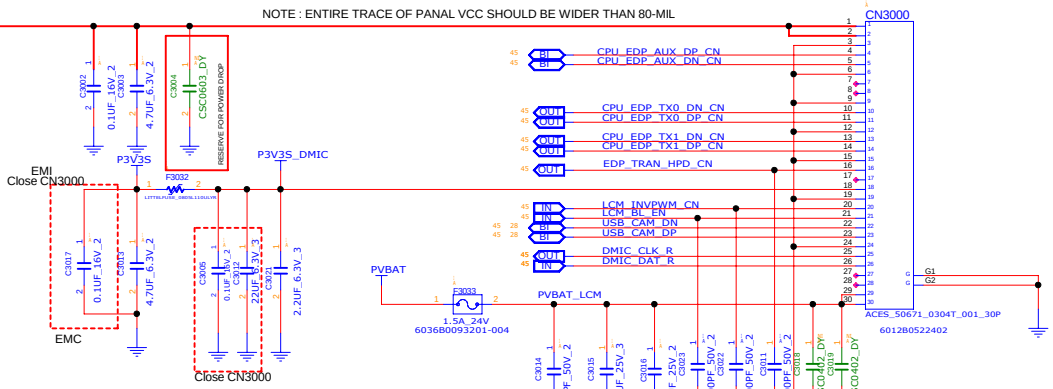
LCM : eDP

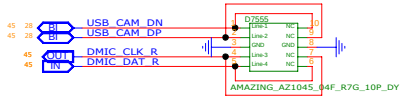
LOCATION 3000 ~ 3049

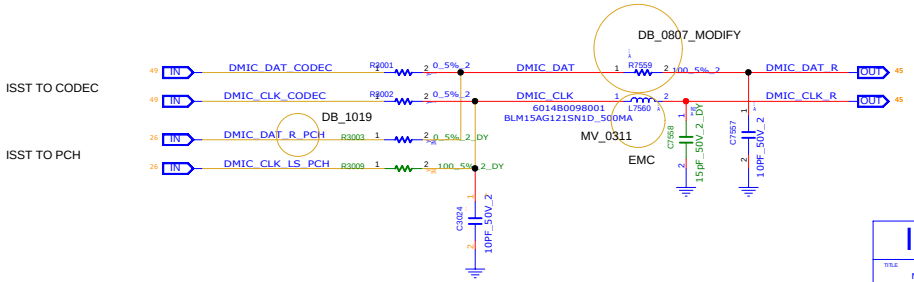












INVENTEC

MODEL,PROJECT,FUNCTION
LVDS

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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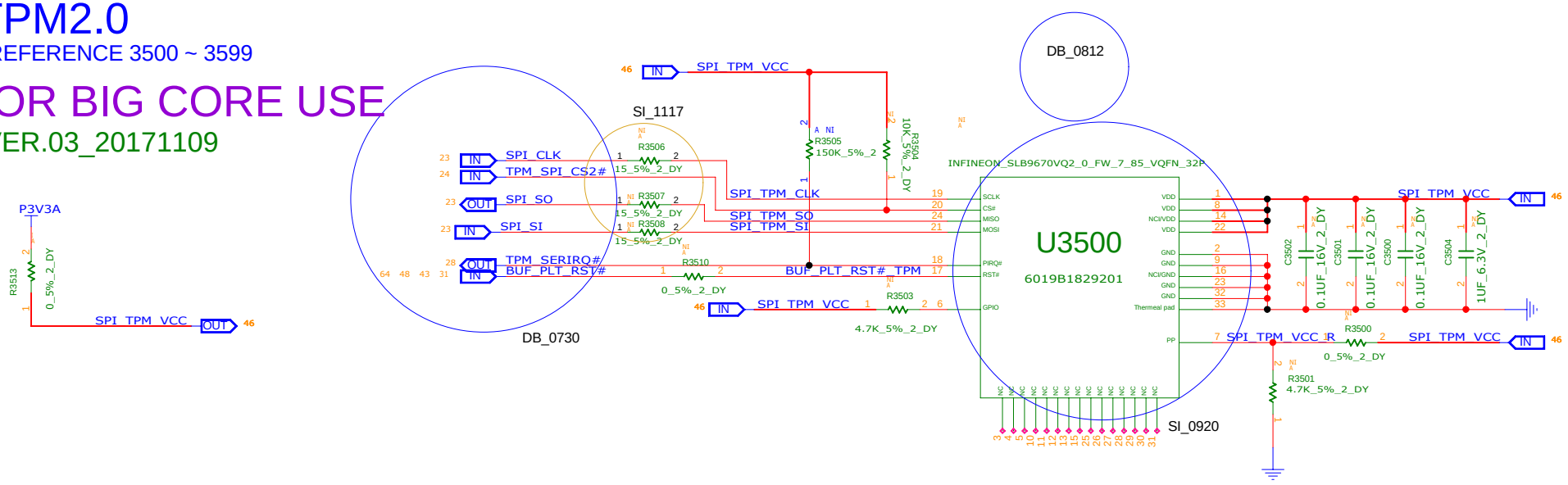
TPM2.0

REFERENCE 3500 ~ 3599

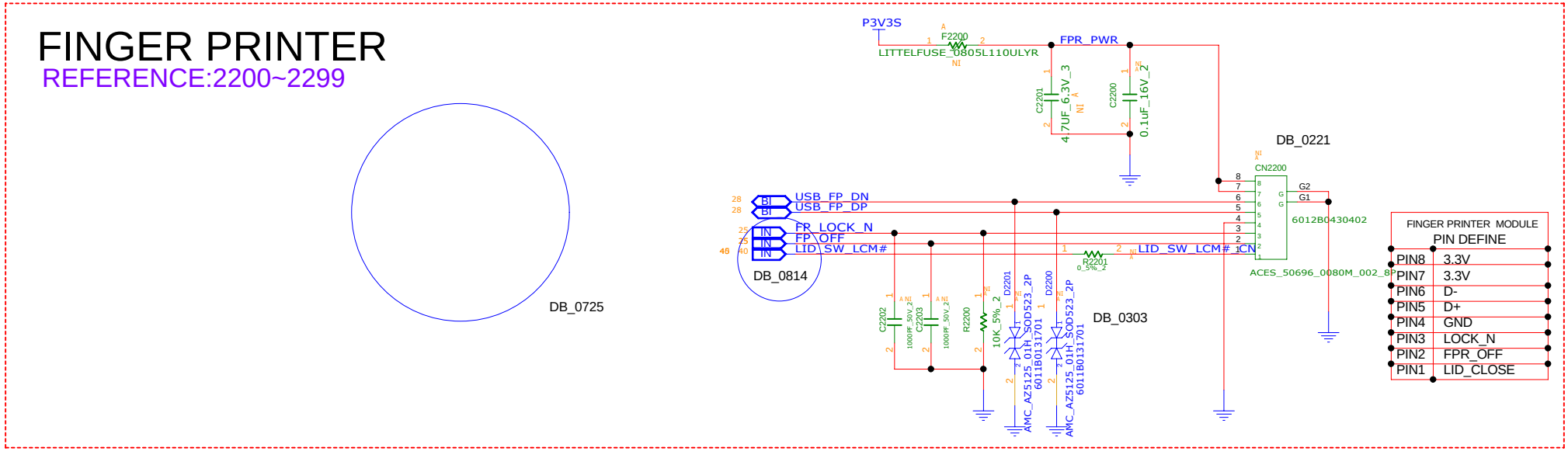
FOR BIG CORE USE

VER.03_20171109



FINGER PRINTER

REFERENCE:2200~2299



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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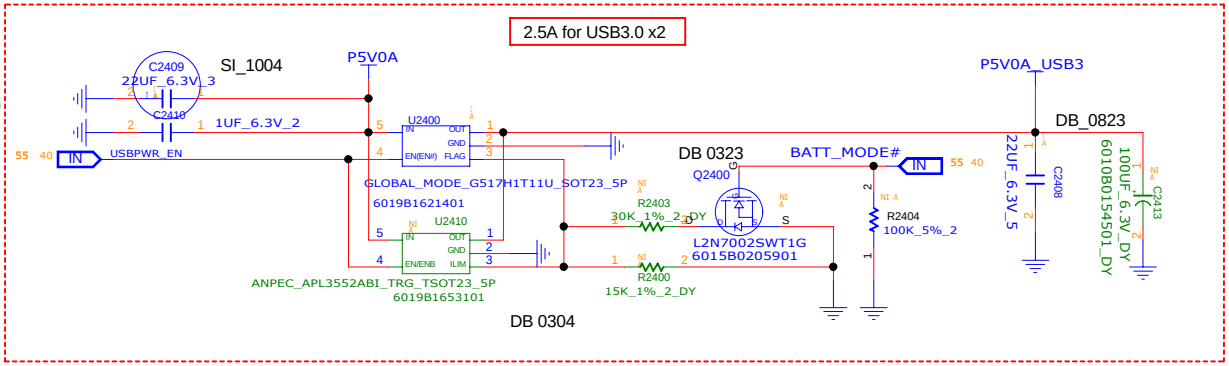
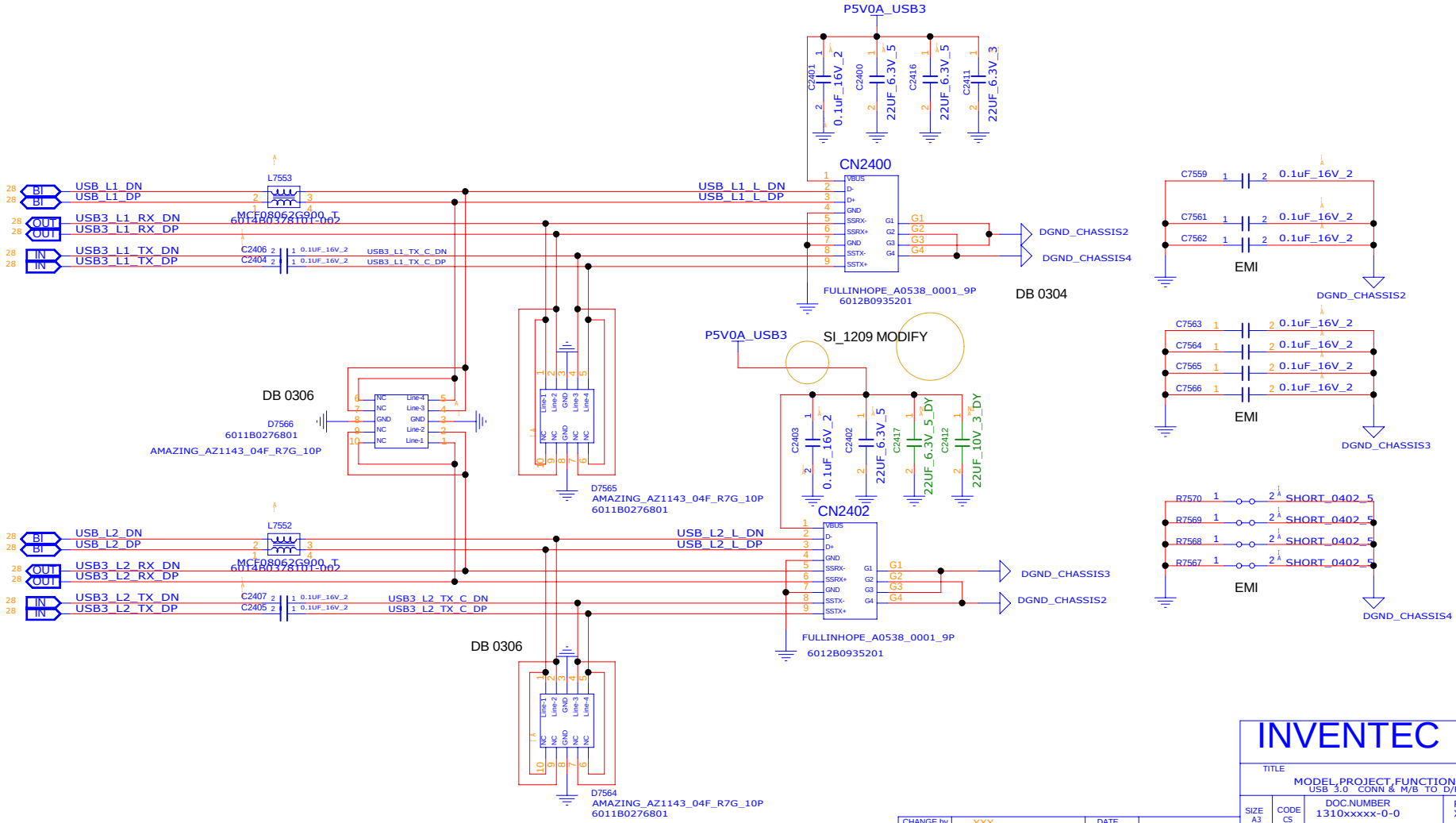
CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

USB3.0

LOCATION 2400~2499

VER.08_20171119





CHANGE by	XXX	DATE	
PCB P/N	60NGxxxxxxxx	PCB VER	XX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
USB 3.0 CONN & M/B TO D/B CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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HYBRIDE-M.2E KEY VER.08_20171221

CNVI-WLAN

REFERENCE 1300 ~ 1349

P1V8A

DB_1019

CNV_RGI_DT_UART0_TXD_R

CNV_BRI_DT_UART0_RTS_R

CNV_RGI_RSP_UART0_CTS

CNV_BRI_RSP_UART0_RXD

R1307 49.9_1%_2

R1302 49.9_1%_2

CNV_RGI_RSP_UART0_CTS_R

CNV_BRI_RSP_UART0_RXD_R

DB 0107

PCI-E-WAKE

PCH_PCIE_WAKE#

R1310 0_5%_2_DY

PCH_WLAN_WAKE#

R1308 0_5%_2

FROM GPP

P3V3S_WLAN

DB_1019

R1312 100K_5%_2

Q1303

L2N7002SWT1G

6015B0205901

WLAN_WAKE#

P3V3S_WLAN

1.5A

CLOSE PIN2 & 4

CLOSE PIN70 & 72

C1308 4.7UF_6.3V_2_DY

C1309 4.7UF_6.3V_2_DY

C1304 10uF_6.3V_3 6010B0044902-001

C1301 0.1uF_16V_2

C1302 0.01UF_50V_2

C1300 10uF_6.3V_3 6010B0044902-001

C1306 0.1uF_16V_2

C1303 0.01UF_50V_2

P3V3S_WLAN

SI _1118

R1301 10K_5%_2

R1306 10K_5%_2

CN1300

TP1301

CNV_WT_CLK_DP

CNV_WT_CLK_DN

CNV_WT_LANE0_DP

CNV_WT_LANE0_DN

CNV_WT_LANE1_DP

CNV_WT_LANE1_DN

CNVI

JfP support 1.8V/3.3V on W_DISABLE pin

WLAN_RF_OFF#

2ND_WLAN_RF_OFF#

BUF_PLT_RST#

R1303 SHORT_0402_5

R1304 SHORT_0402_5

R1311 SHORT_0402_5

CLK_SUSCLK_CNV

R1328 SHORT_0402_5

WLAN_RF_OFF#_R

2ND_WLAN_RF_OFF#_R

BUF_PLT_RST#_R

M2_SUS_CLK_CN

C1305 220pF_50V_2_DY

PV_0121

R1313 0_5%_2_DY

R1314 100K_5%_2_DY

CNVI_PLT_RST#

CNV_BRI_DT_UART0_RTS_R

CNV_RGI_RSP_UART0_CTS_R

CNV_RGI_DT_UART0_TXD_R

WLAN_WAKE#

CLKREQ_WLAN#_Q

R1305 0_5%_2

CLKREQ_WLAN#

CLK_PCIE_WLAN_DN

CLK_PCIE_WLAN_DP

PCIE_WLAN_RX_C_DN

PCIE_WLAN_RX_C_DP

PCIE_WLAN_TX_C_DN

PCIE_WLAN_TX_C_DP

CNVI

CNV_BRI_RSP_UART0_RXD_R

TP1300

CNV_CLKREQ

CNV_RF_RESET#

WLAN_IND#

P3V3S_WLAN

R1309 71.5K_1%_2_DY

P3V3S_WLAN

R1300 10K_5%_2

DB_0807

LOTES_APCI0076_P002H03_75P

M2_E Key

CNV_WR_CLK_DP

CNV_WR_CLK_DN

CNV_WR_LANE0_DP

CNV_WR_LANE0_DN

CNV_WR_LANE1_DP

CNV_WR_LANE1_DN

USB_WLAN_DN

USB_WLAN_DP

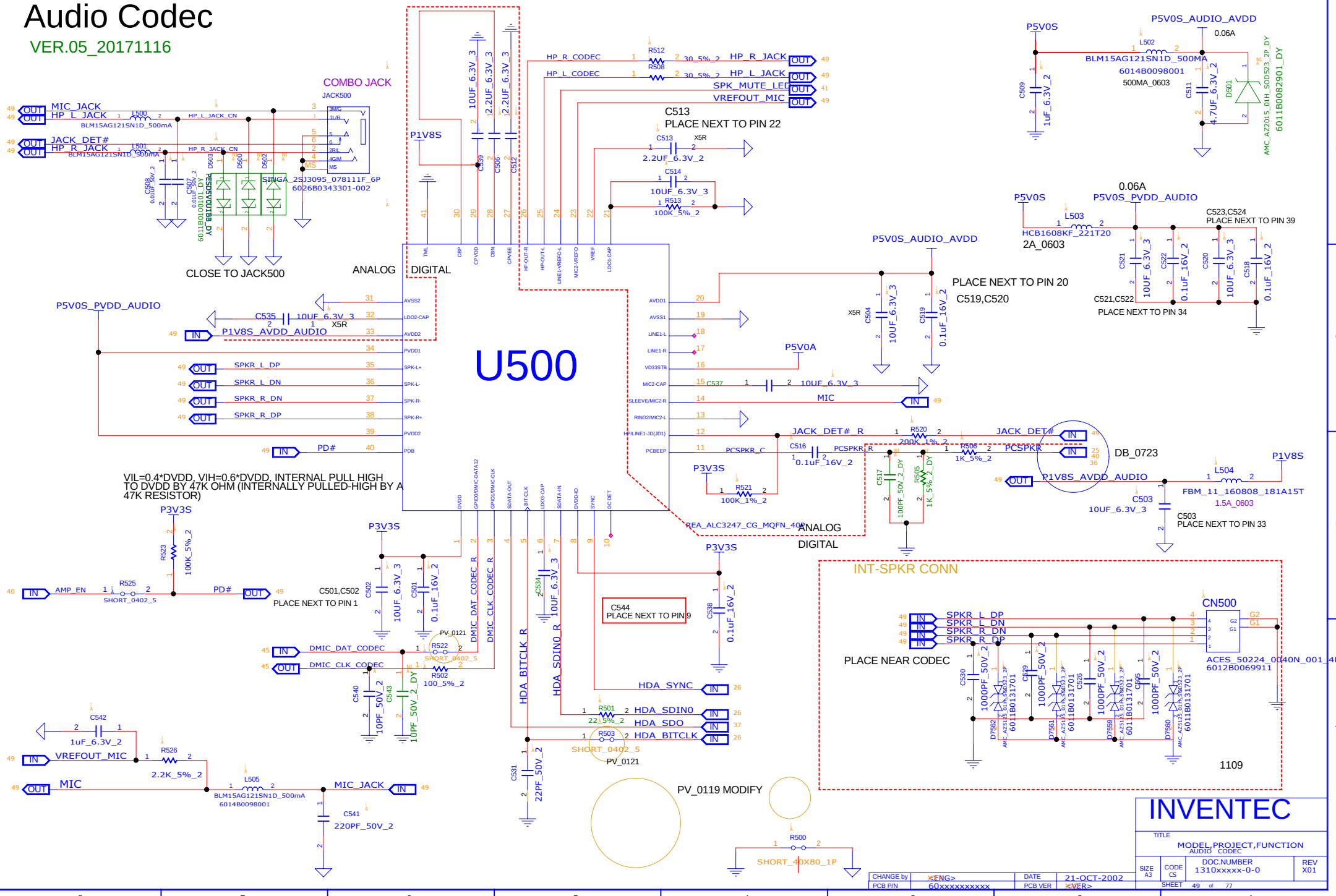
CNVI

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION WLAN & BT		
SIZE 3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by	XXX	DATE	
PCB P/N	60NSxxxxxxxx	PCB VER	XX
VER	OCT-2002	SHEET	of 48 77

Audio Codec

VER.05_20171116



CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
AUDIO CODEC

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 49 of 77

LAN (Controller)

Location 400 ~ 469

VER.05_20171115-2

★ 6019B1264001	RTL8111HSH-CGT	10/100/1000

P3V3A_LAN RISING TIME (10%~90%)NEED>0.5MS AND <100MS
LAN POWER NOISE P3V3A_LAN < 200MV VPEAK TO VPEAK

0.5A

P3V3A → R407 SHORT_0805_50 → P3V3A_LAN

MV_0325

Pin11, Pin32

C404 0.1UF_16V_2, C418 4.7uF_6.3V_3, C405 0.1UF_16V_2, C419 4.7uF_6.3V_3, C416 4.7uF_6.3V_3, C417 0.1UF_16V_2, C7555 56PF_50V_2, C7554 82PF_50V_2, C7553 120PF_50V_2

FOR RTL8111

P1V0_LAN_REG → L400 LQM21PN2R2MC0D 6014B0168601 → P1V0_LAN

Switch MODE(RTL8111HSH-CG)
L400,C414,C415 mount

C414 4.7uF_6.3V_3, C415 0.1UF_16V_2

L400
1ST : 6014B0200401
2ND : 6014B0190301

LAN POWER NOISE P1V0_LAN < 100MV VPEAK TO VPEAK
Close to LAN chip

Pin3, Pin8, Pin30, Pin 22, Pin 22, PIN 24

C400 0.1UF_16V_2, C406 0.1UF_16V_2, C408 0.1UF_16V_2, C407 0.1UF_16V_2, C413 1uF_6.3V_2, C424 0.1UF_16V_2

FOR RTL8111HSH

P3V3S → R404 1K_5%_2, R403 15K_5%_2

P3V3A_LAN → R402 4.7K_5%_2

P1V0_LAN → R401 2.49K_1%_2

XTAL25LAN2 IN 50
XTAL25LAN1 IN 50
LED_LANRXACT# TP9000 OUT 51
GPO
LED_LANLINK# TP9002 OUT 50
WOL_PWEN IN 40

U400
RTL8111HSH-CG
REA_RTL8111HSH_CG_QFN_32P
6019B1264001

GND 33

LAN_TRD0_DP BI 51
LAN_TRD0_DN BI 51
LAN_TRD1_DP BI 51
LAN_TRD1_DN BI 51
LAN_TRD2_DP BI 51
LAN_TRD2_DN BI 51
LAN_TRD3_DP BI 51
LAN_TRD3_DN BI 51

P1V0_LAN_REG, P1V0_LAN, P3V3A_LAN

R409 10K_5%_2_DY

LAN_WAKE# OUT 50
LAN_RST# IN 50

PCIE_LAN_RX_DN, PCIE_LAN_RX_DP → C402, C403 0.1UF_16V_2 → PCIE_LAN_RX_C_DN OUT 28, PCIE_LAN_RX_C_DP OUT 28

PLACE CLOSE TO PIN 17,18

C401 CSC0402_DY

CLKREQ_LAN# OUT 29 → R400 short_0402_15_nsp → CLKREQ_LAN#_R

PCIE_LAN_TX_C_DP IN 28
PCIE_LAN_TX_C_DN IN 26
CLK_PCIE_LAN_DP IN 29
CLK_PCIE_LAN_DN IN 29

XTAL25LAN2 OUT 50 → R405 1K_5%_2
XTAL25LAN1 OUT 50 → X400 25MHZ_10PF 6018B0058301 PV_0119

C409 15PF_50V_2, C410 15PF_50V_2

DB_1005

LAN_WAKE# IN 50 → R411 0_5%_2 → PCH_PCIE_WAKE# OUT 31
LAN_RST# OUT 50 → R408 0_5%_2 → PLT_RST# IN 31

DB 0323

FOR DONGTING WAKE ON WLAN
DONGTING MOUNT
HEDWIG DY

P3V3A → R406 10K_5%_2 → LANLINK_STATUS OUT 24

P3V3A → Q401 L2N7002SWT1G 6015B0205901

P3V3A_LAN → Q400 L2N7002SWT1G 6015B0205901 → LED_LANLINK# IN 50 51

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 50 of 77	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

LAN (Transformer & RJ45)

Location 470 ~ 499

VER.05_20171107

For 10/100 /1000 LAN

GIGA main BOM change to 6016B0000201

10/100/1000 MAIN===> BOTHHAND P/N : 6016B0000201 GST5009

10/100/1000 2ND===> UDE P/N : 6016B0022201 L22N001-0

U470

LAN_TRD0_DP / LAN_TRD0_DN

LAN_TRD1_DP / LAN_TRD1_DN

LAN_TRD2_DP / LAN_TRD2_DN

LAN_TRD3_DP / LAN_TRD3_DN

BOTH_GST5009_SOP_24P

6016B0000201

LAN_TRD0_CN_DP / LAN_TRD0_CN_DN

LAN_TRD1_CN_DP / LAN_TRD1_CN_DN

LAN_TRD2_CN_DP / LAN_TRD2_CN_DN

LAN_TRD3_CN_DP / LAN_TRD3_CN_DN

C475 0.01UF_100V_3

C474 0.01UF_100V_3

C470 0.01UF_100V_3

C471 0.01UF_100V_3

R474 75_5%_2

R475 75_5%_2

R471 75_5%_2

R470 75_5%_2

C472 1000PF_2000V_6

6010A0034001

SIZE : 1206

C478 10PF_50V_2

C479 CSC0402_DY

C473 0.01uF_50V_2

D470

AMAZING_AZ1045_04F_R7G_10P_DY

6011B0172501_DY

D471

AMAZING_AZ1045_04F_R7G_10P_DY

6011B0172501_DY

RJ-45

P3V3A_LAN

JACK470

6026B0421601

SINGA_2RJ1792_000111F_12P

R473 330_5%_2

R472 4.7K_5%_2

LED_LANRXACT#

LED_LANLINK#

C477 1000PF_50V_2

C476 1000PF_50V_2

DGND_CHASSIS1

EMI

P3V3A_LAN

C480 1000PF_50V_2

C481 1000PF_50V_2

NODE	COLOR	
A1(+) A2(-)	AMBER	A1 A2
B1(+) B2(-)	WHITE	B1 B2

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION

Block Diagram

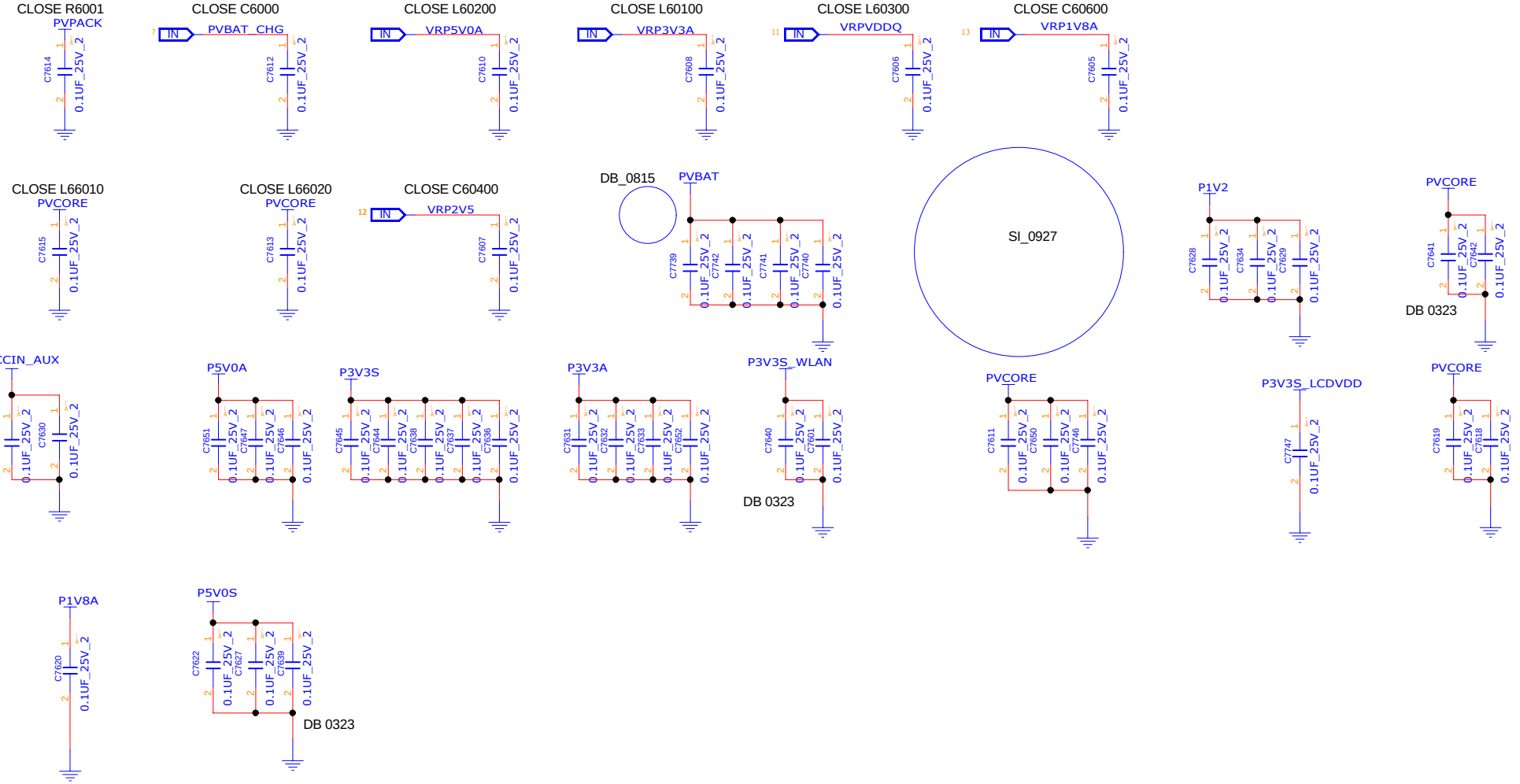
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 51 of 77

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

EMI SOLUTION

LOCATION : 7600 - 7699



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

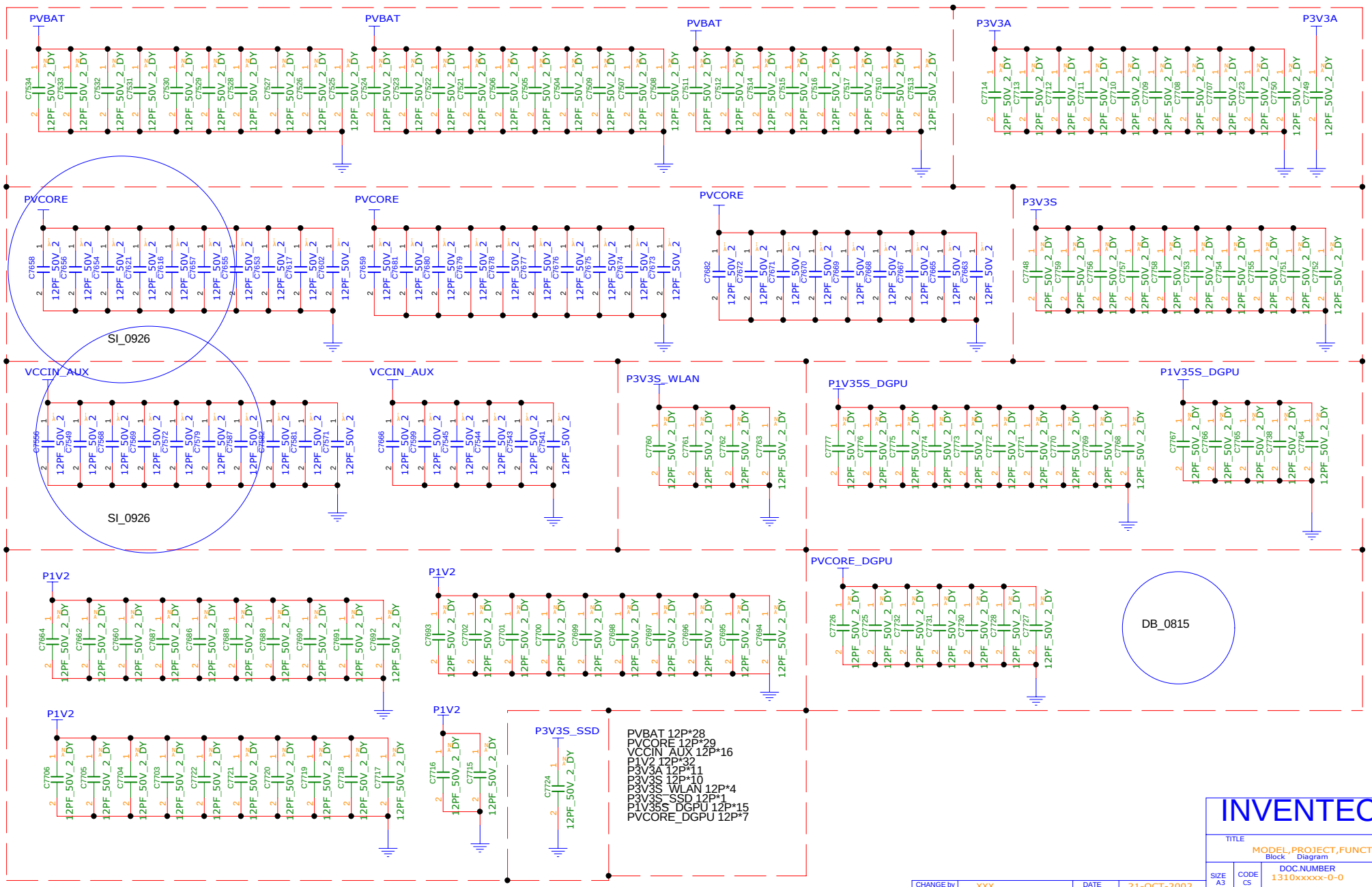
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 52 of 77

RF SOLUTION

LOCATION: 7500 - 7599



INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

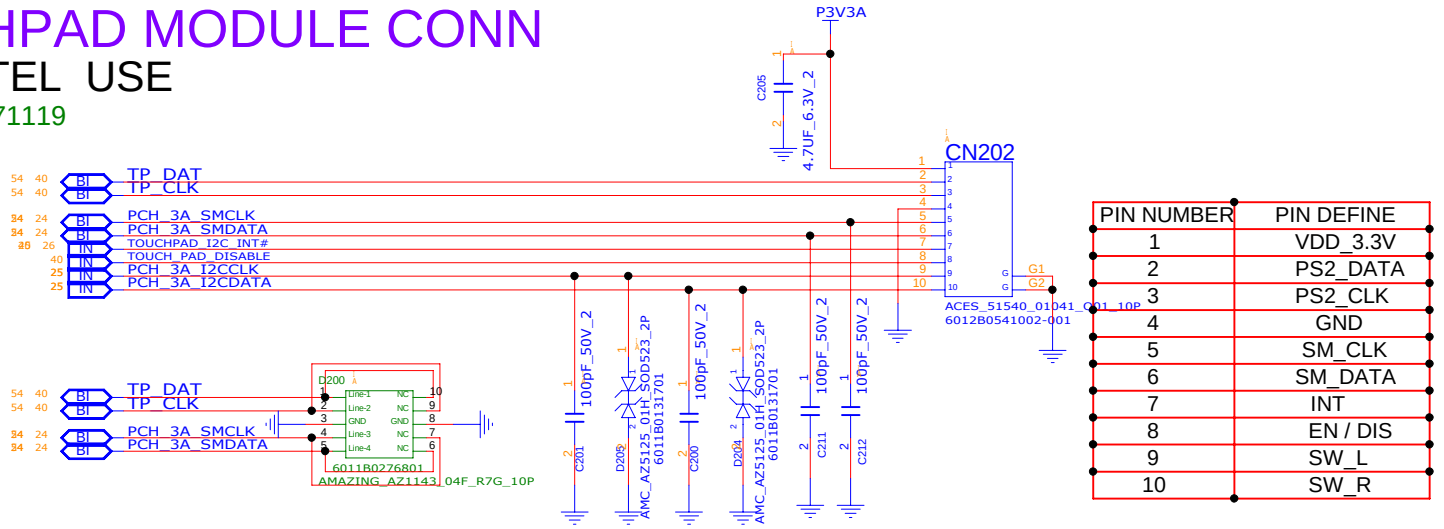
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 53 of 77

TOUCHPAD MODULE CONN

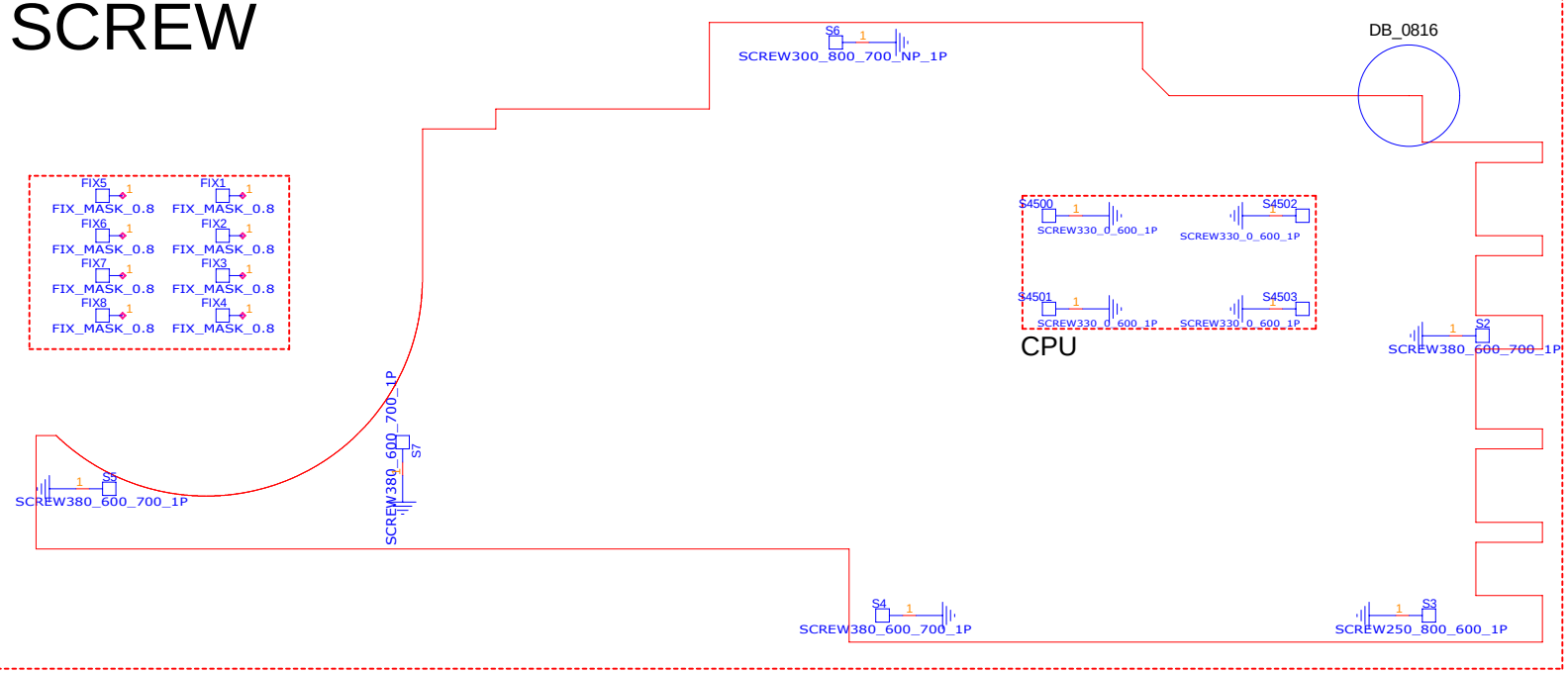
FOR INTEL USE

VER.14_20171119



PIN NUMBER	PIN DEFINE
1	VDD_3.3V
2	PS2_DATA
3	PS2_CLK
4	GND
5	SM_CLK
6	SM_DATA
7	INT
8	EN / DIS
9	SW_L
10	SW_R

SCREW



INVENTEC

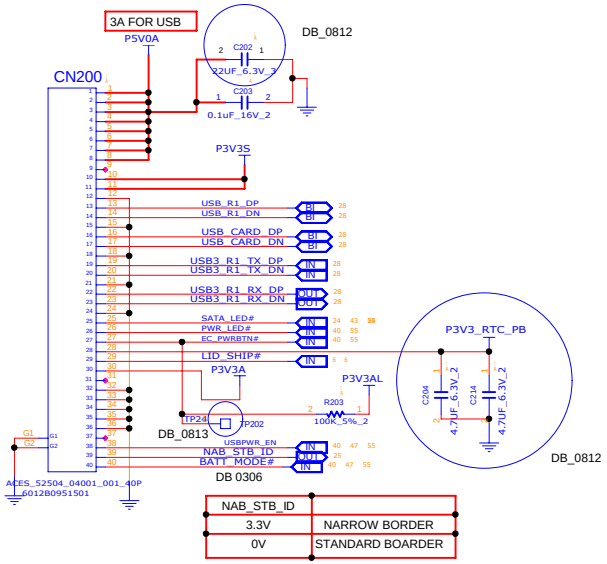
TITLE	MODEL,PROJECT,FUNCTION POWER_BUTTON		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET	of 54	77	

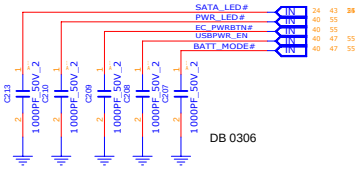
CHANGE by	XXX	DATE	OCT-2002
PCB P/N	60NBxxxxxxxx	PCB VER	X01

MB TO USB CARDREADER BOARD CONN

FOR NARROW BORDER USE

VER.12_20171120





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 55 of 77

CHANGE ID	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

Small Board

1.USB & CR FOR NARROW BORDER (LOCATION : 9200)

2.USB & CR FOR STANDARD BORDER (LOCATION : 9600)

3. PICK BUTTON BOARD (LOCATION : 9300)

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

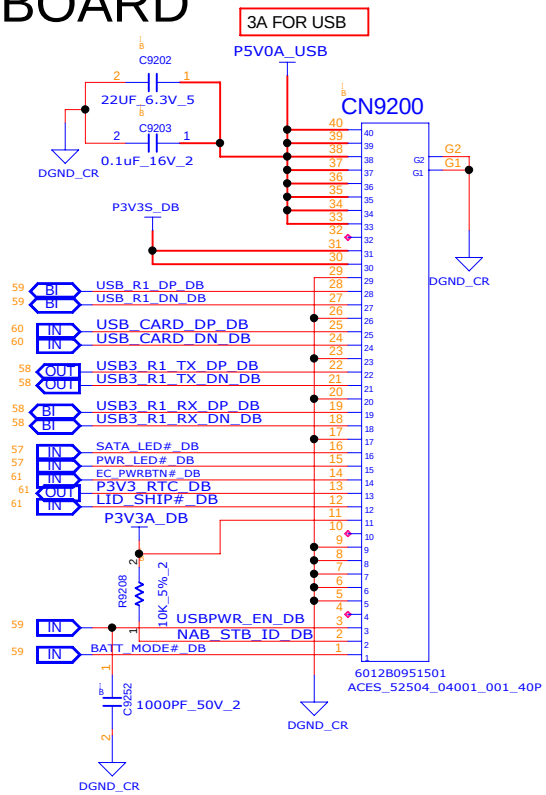
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

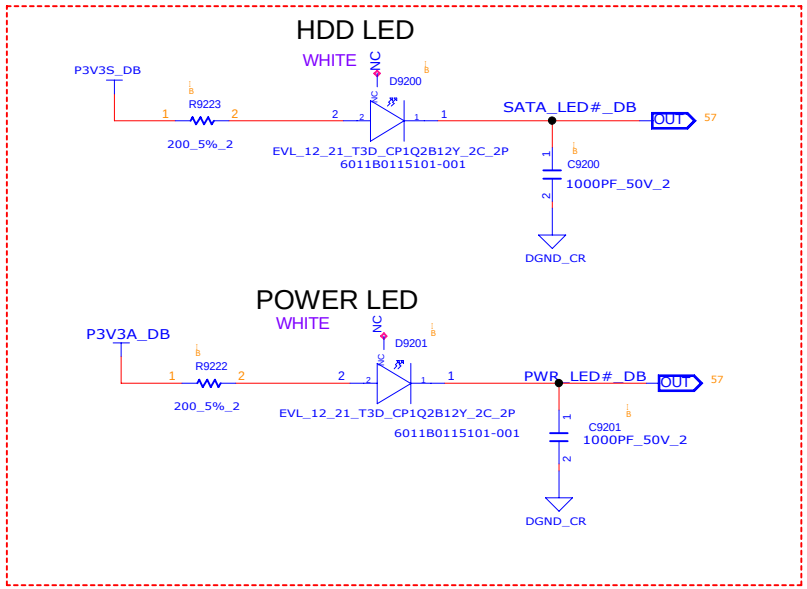
SHEET 56 of 77

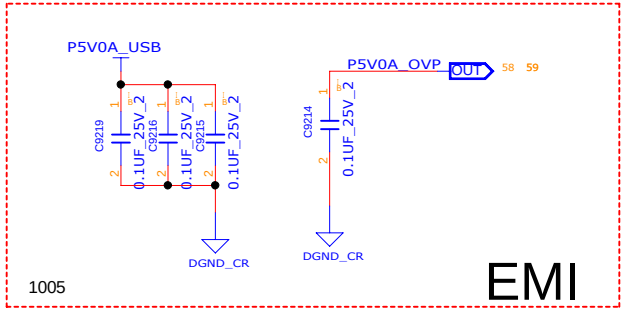
CARDREADER USB BOARD

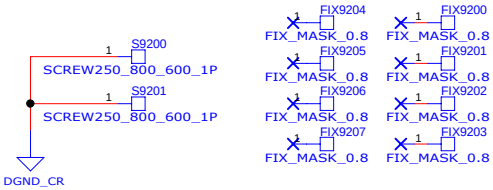
FOR NARROW BORDER USE

VER.09_20171109









INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	
PCB P/N	60NBxxxxxxxx	PCB VER	X01

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

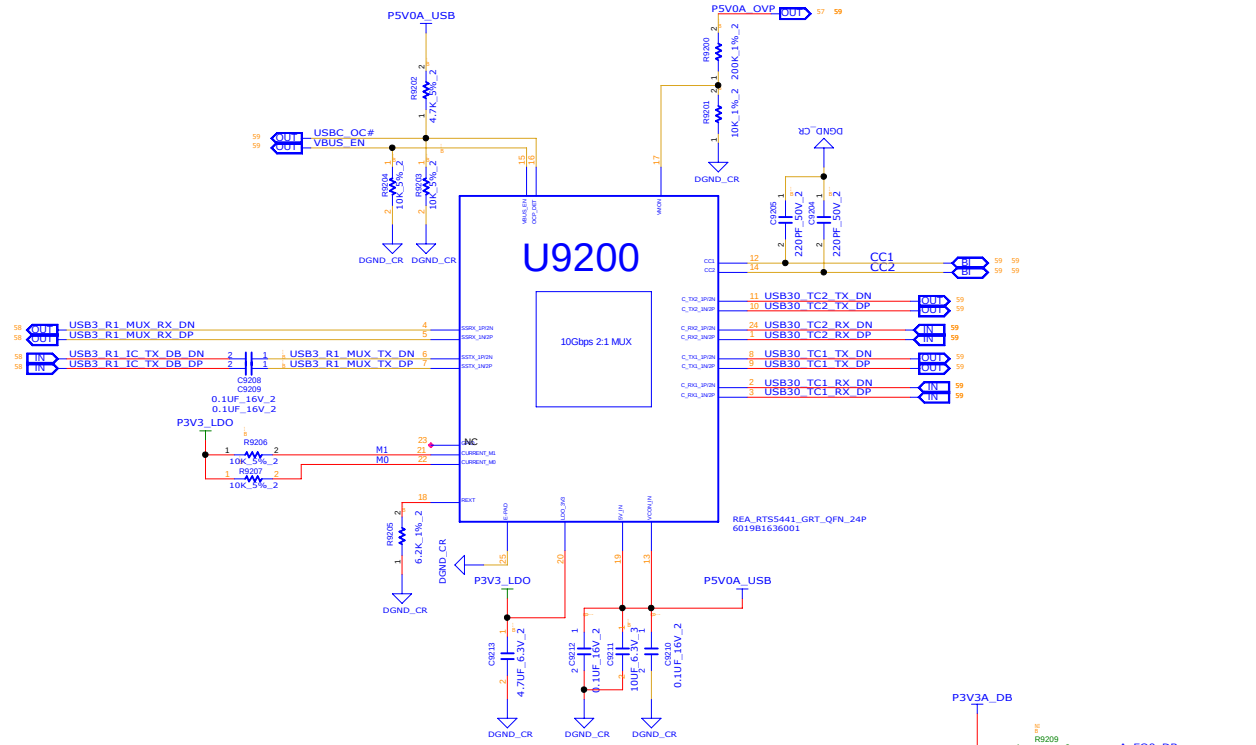
SHEET of 57 77

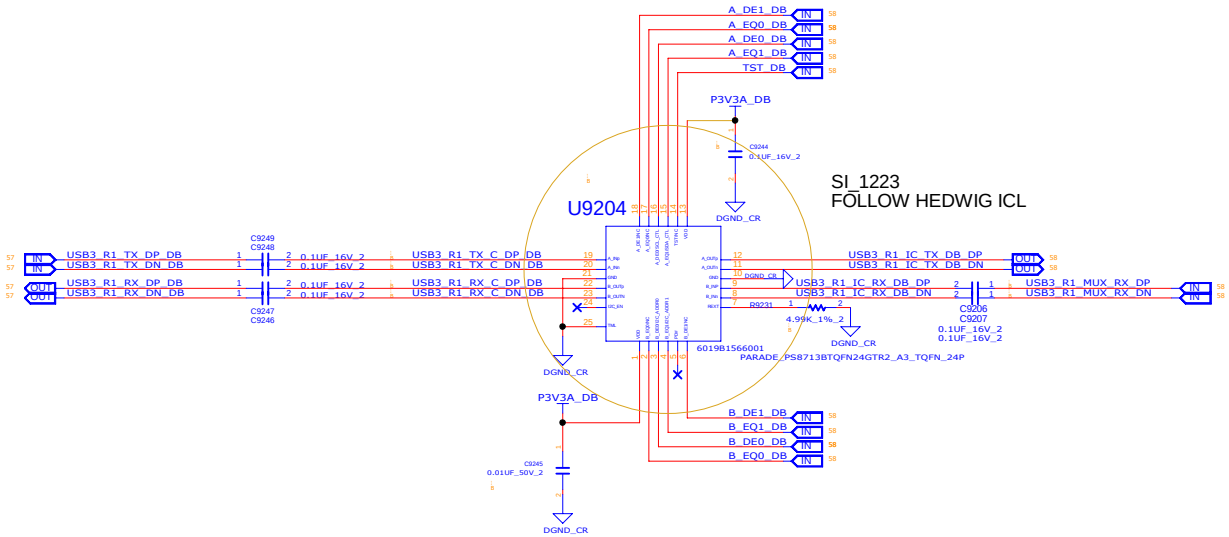
OCT-2002

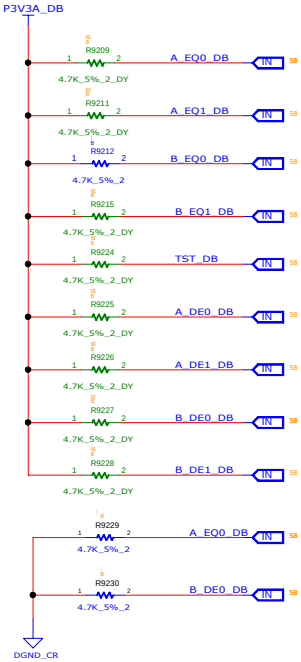
USB3.0 MUX

FOR NARROW BORDER USE

VER.02_20170919







CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

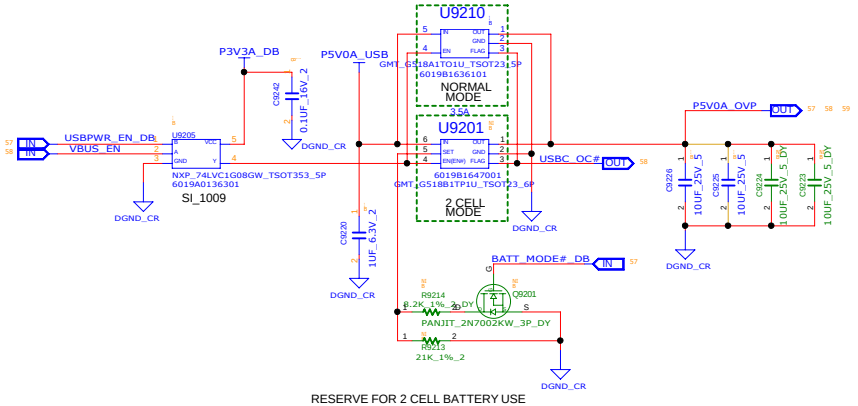
SHEET 58 of 77

USB3.0 TYPEC CNTR

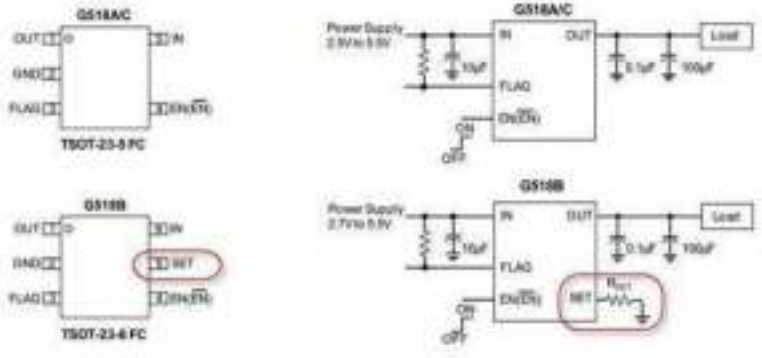
FOR NARROW BORDER USE

VER.13_20171119

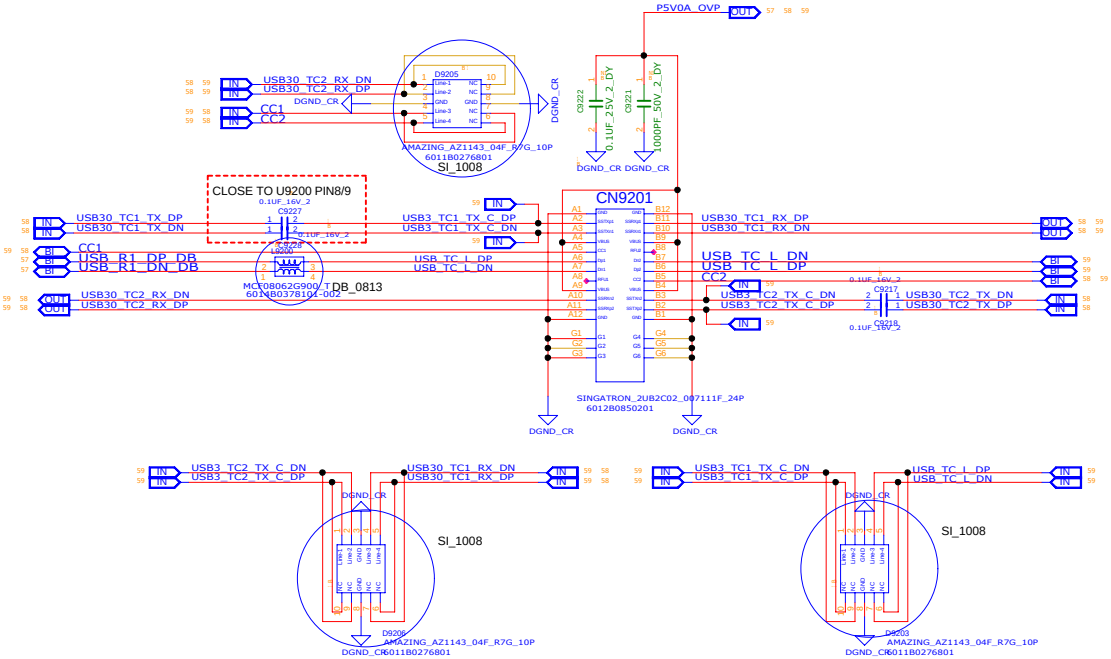
TYPE C OVP



RESERVE FOR 2 CELL BATTERY USE



				MIN	TYPE	MAX	UNIT	
NORMAL	G518A (TSOT-23-5)	6019B1636101		3.1	3.5	4	A	
SUPPORT 2 CELL	G518B (TSOT-23-6)	AC MODE	R_SET=6K	3.1	3.5	4	A	BATT_MODE#_DB = HIGH
	6019B1647001	DC MODE	R_SET=21K	0.8	1	1.2	A	BATT_MODE#_DB = LOW



INVENTEC

MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

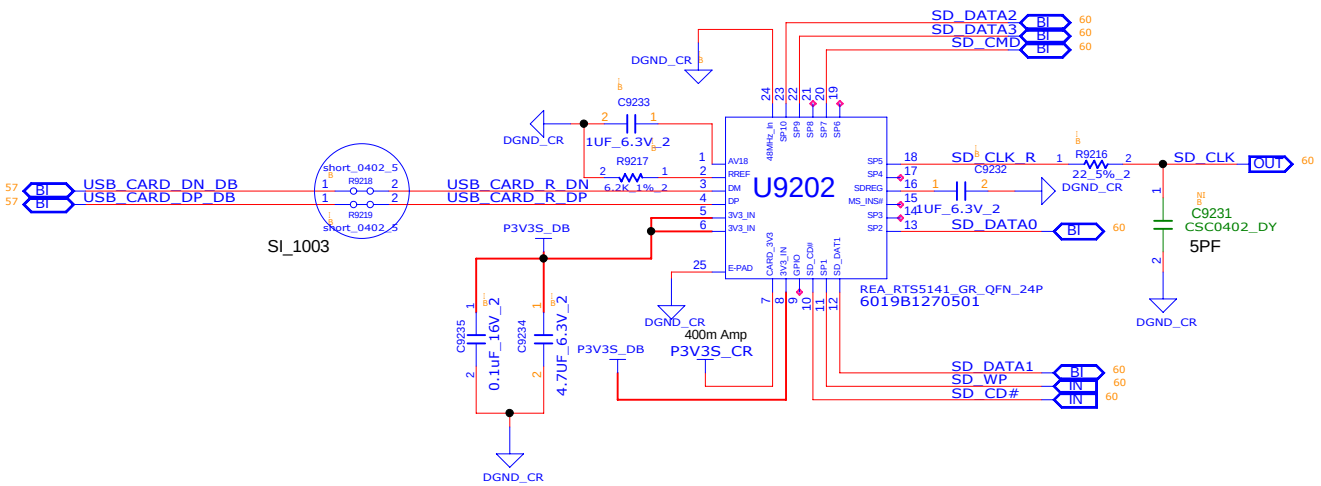
SHEET 1 of 59 77

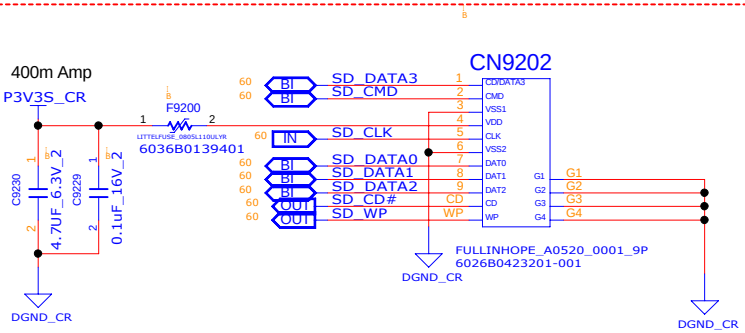
CARD READER

RTS5141-GR

FOR NARROW BORDER USE

VER.03_20171107





CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
CRT_CONN

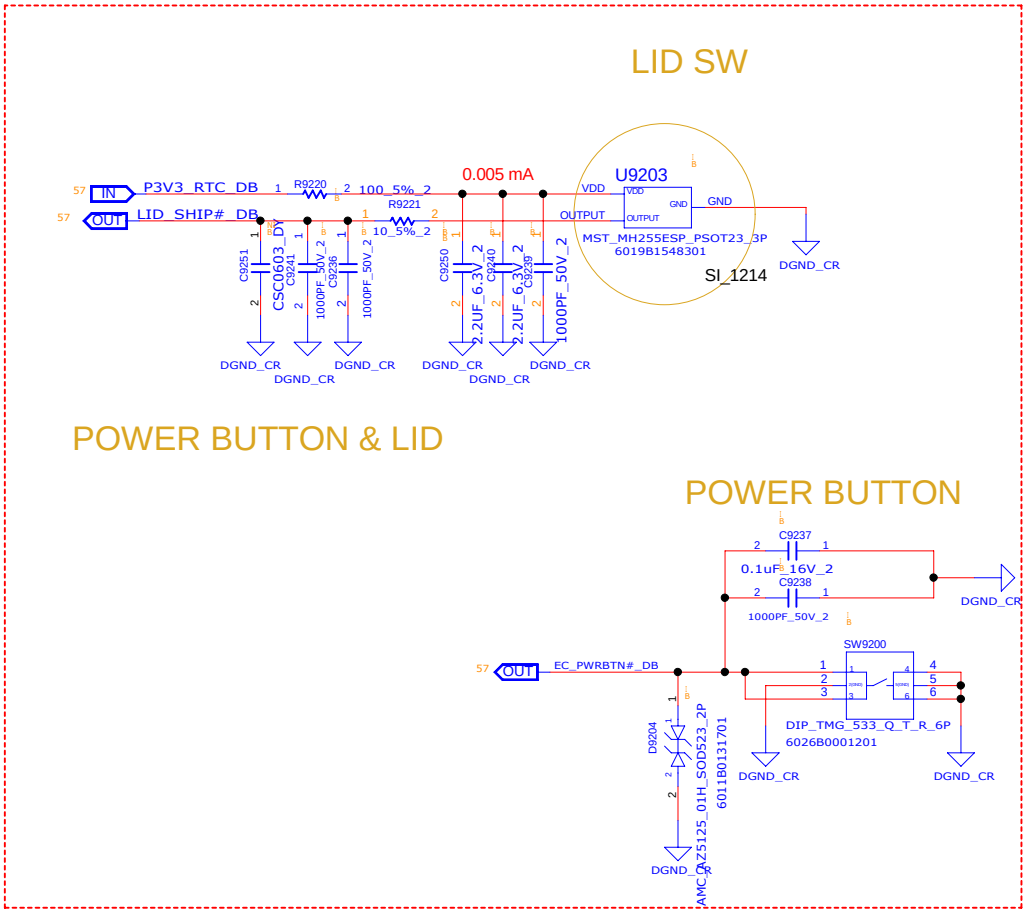
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 60 of 77

LID SW & POWER BUTTON

FOR NARROW BORDER USE

VER.07_20171120



INVENTEC

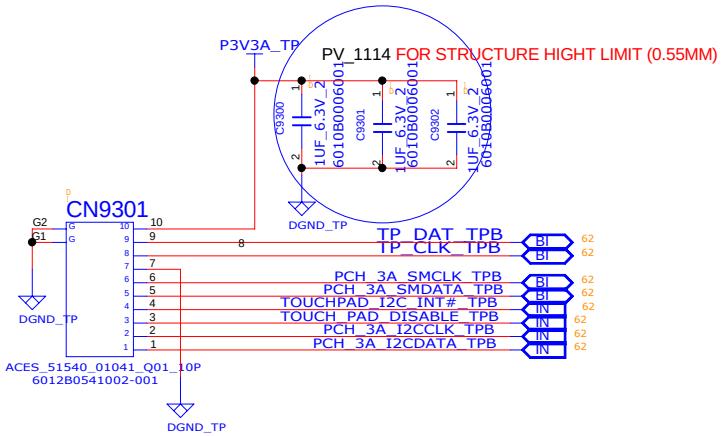
TITLE: MODEL,PROJECT,FUNCTION Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET 61 of 77	

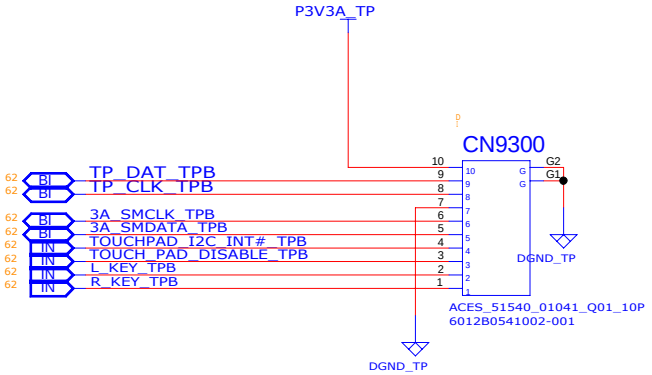
PICK BUTTON (TYPE_C)

TOUCHPAD R / L BOARD

VER.03_20171119

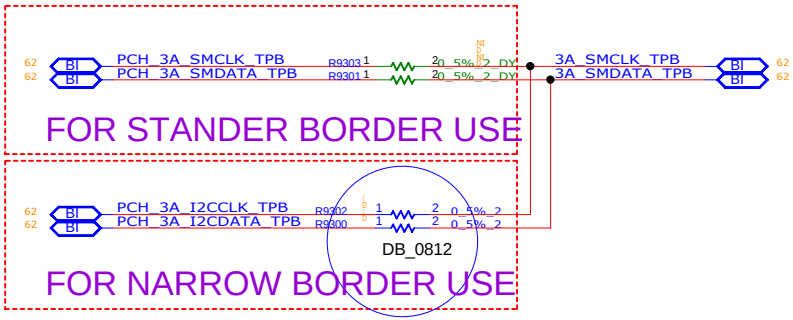


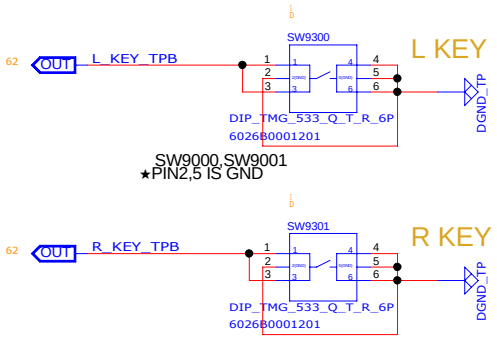
TO MAIN BOARD

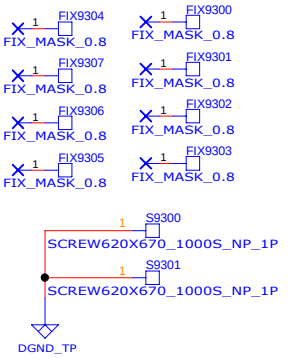


TO TP MODULE

PIN DEFINE	PIN NUMBER
VDD_3.3V	1
PS2_DATA	2
PS2_CLK	3
GND	4
SM_CLK	5
SM_DATA	6
INT	7
EN / DIS	8
SW_L	9
SW_R	10







INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 62 of 77			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

N18S-G5

GDDR5 SINGL RANK 23X23

2021.03.02

PCA CODE NAME：N18S-G5-A1 GPU
PCB VERSION：AX1

BOARD SIZE:

HP
SCH P/N:
PCB P/N:
PCA P/N:

DATE	CHANGE NO.	REV
21-OCT-2002		
21-OCT-2002	2013-ECO-002392	A

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK	Hsu Andy		
APPROVAL	Hsu Andy		
FILE NAME	MLB 17.3 - RANGERS		
PCB P/N	60-xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL, PROJECT, FUNCTION

SIZE	CODE	DOC.NUMBER	REV
J	CS	1310xxxxx-0-0	X01

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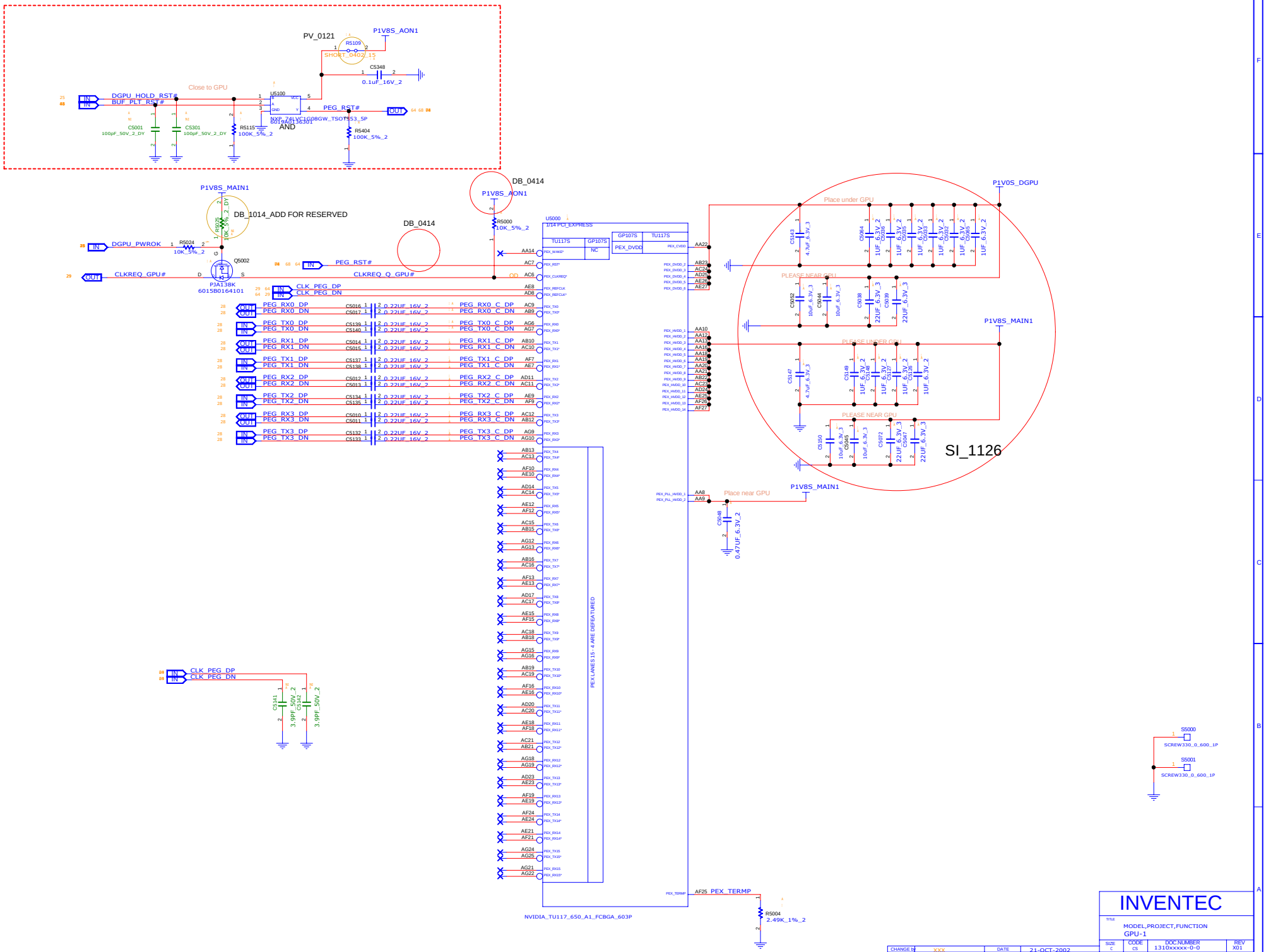
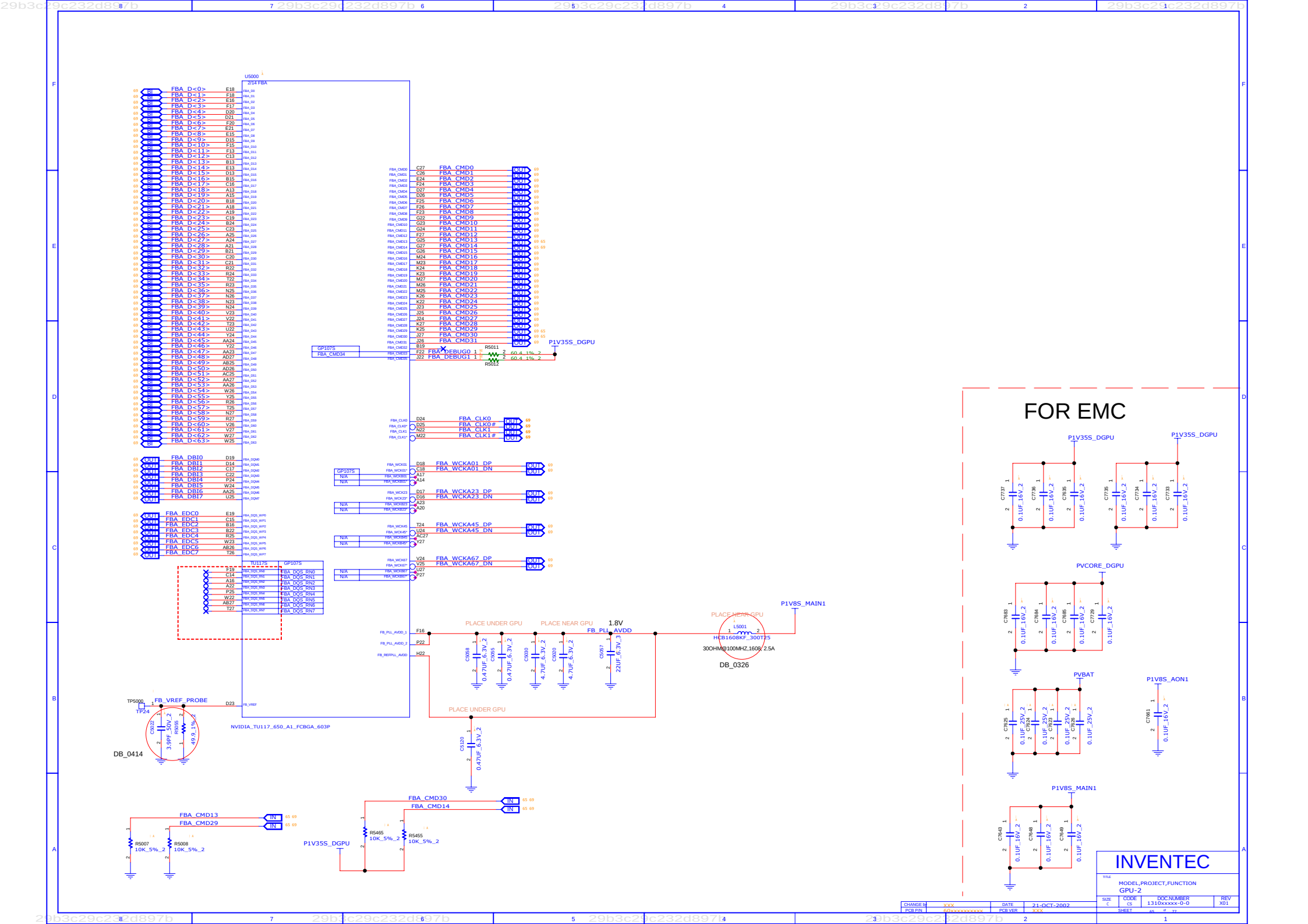
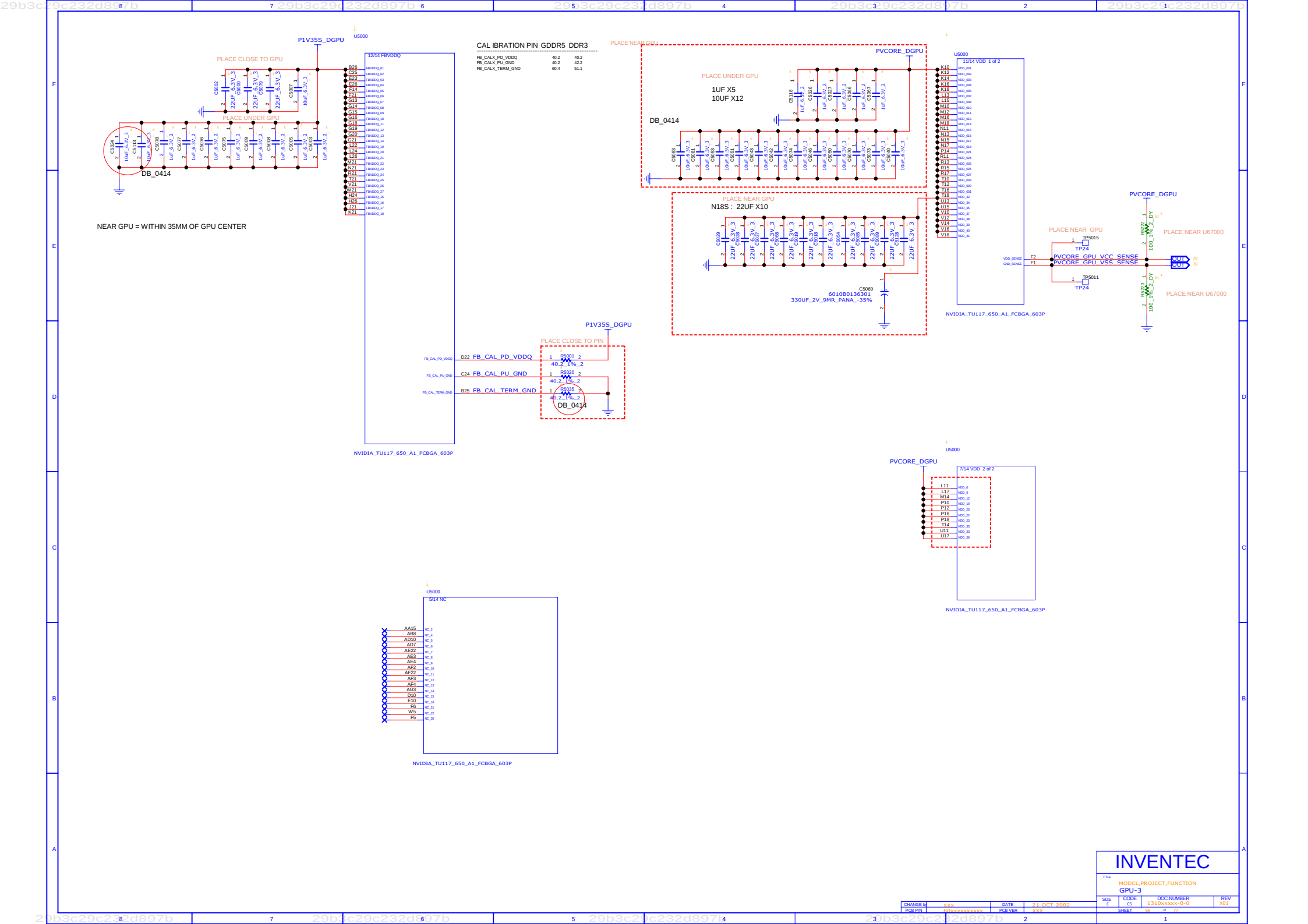

PV_0121
P1V8S_AON1
R5109
SHORT_0402_1S
CS348
0.1UF_16V_2
Close to GPU
DGPU_HOLD_RST#
BUF_PLT_RST#
U5100
MXP_74LVC1G08RGW_TSOT353_5P
0019A0136301
AND
PEG_RST#
CS001
100pF_50V_2_DY
CS301
100pF_50V_2_DY
R5115
100K_5%_2
R5404
100K_5%_2
DB_0414
P1V8S_MAIN1
DB_1014_ADD FOR RESERVED
R5025
10K_5%_2
DGPU_PWROK
R5024
10K_5%_2
Q5002
PJA138K
6015B0164101
CLKREQ_GPU#
CLKREQ_Q_GPU#
R5000
10K_5%_2
U5000
1/14 PCI_EXPRESS
GP107S
TU117S
PEX_DVDD
NC
CLK_PEG_DP
CLK_PEG_DN
PEG_RX0_DP
PEG_RX0_DN
PEG_TX0_DP
PEG_TX0_DN
PEG_RX1_DP
PEG_RX1_DN
PEG_TX1_DP
PEG_TX1_DN
PEG_RX2_DP
PEG_RX2_DN
PEG_TX2_DP
PEG_TX2_DN
PEG_RX3_DP
PEG_RX3_DN
PEG_TX3_DP
PEG_TX3_DN
PEX LANES 15 - 4 ARE DEFEATURED
NVIDIA_TU117_650_A1_FCBGA_603P
P1V0S_DGPU
Place under GPU
PLEASE NEAR GPU
PLEASE UNDER GPU
SI_1126
Place near GPU
PEX_TERMP
R5004
2.49K_1%_2
S5000
S5001
SCREW330_0_600_1P
INVENTEC
MODEL,PROJECT,FUNCTION
GPU-1
DOC NUMBER
1310xxxxx-0-0
21-OCT-2002


U5000
2/14 FBA
NVIDIA_TU117_650_A1_FCBGA_603P
FOR EMC
P1V35S_DGPU
P1V8S_MAIN1
P1V8S_AON1
PVCORE_DGPU
PVBAT
1.8V
FB_PLL_AVDD
PLACE UNDER GPU
PLACE NEAR GPU
DB_0414
DB_0326
INVENTEC
MODEL,PROJECT,FUNCTION
GPU-2



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
GPU-3

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-D-D	X01

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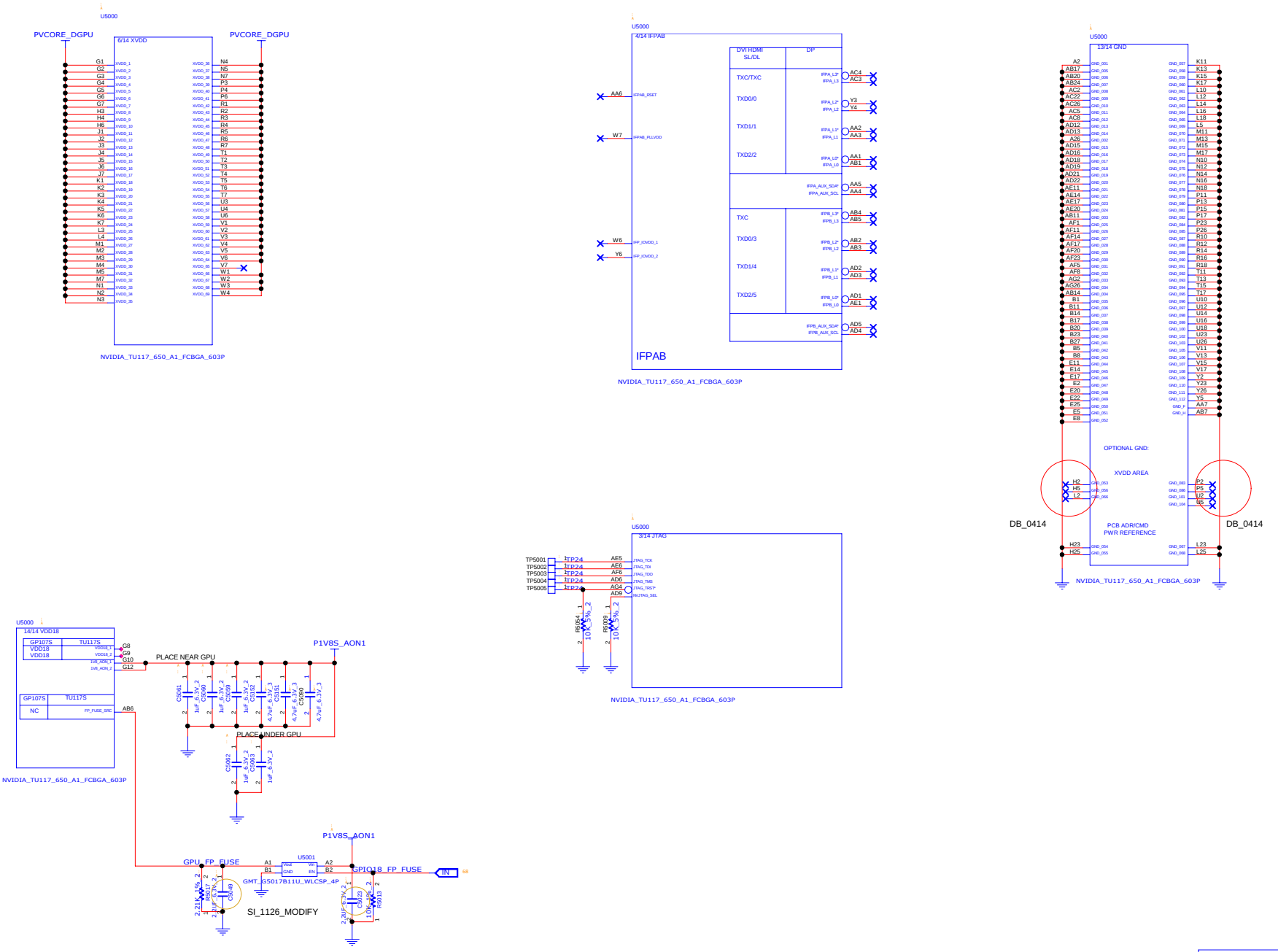
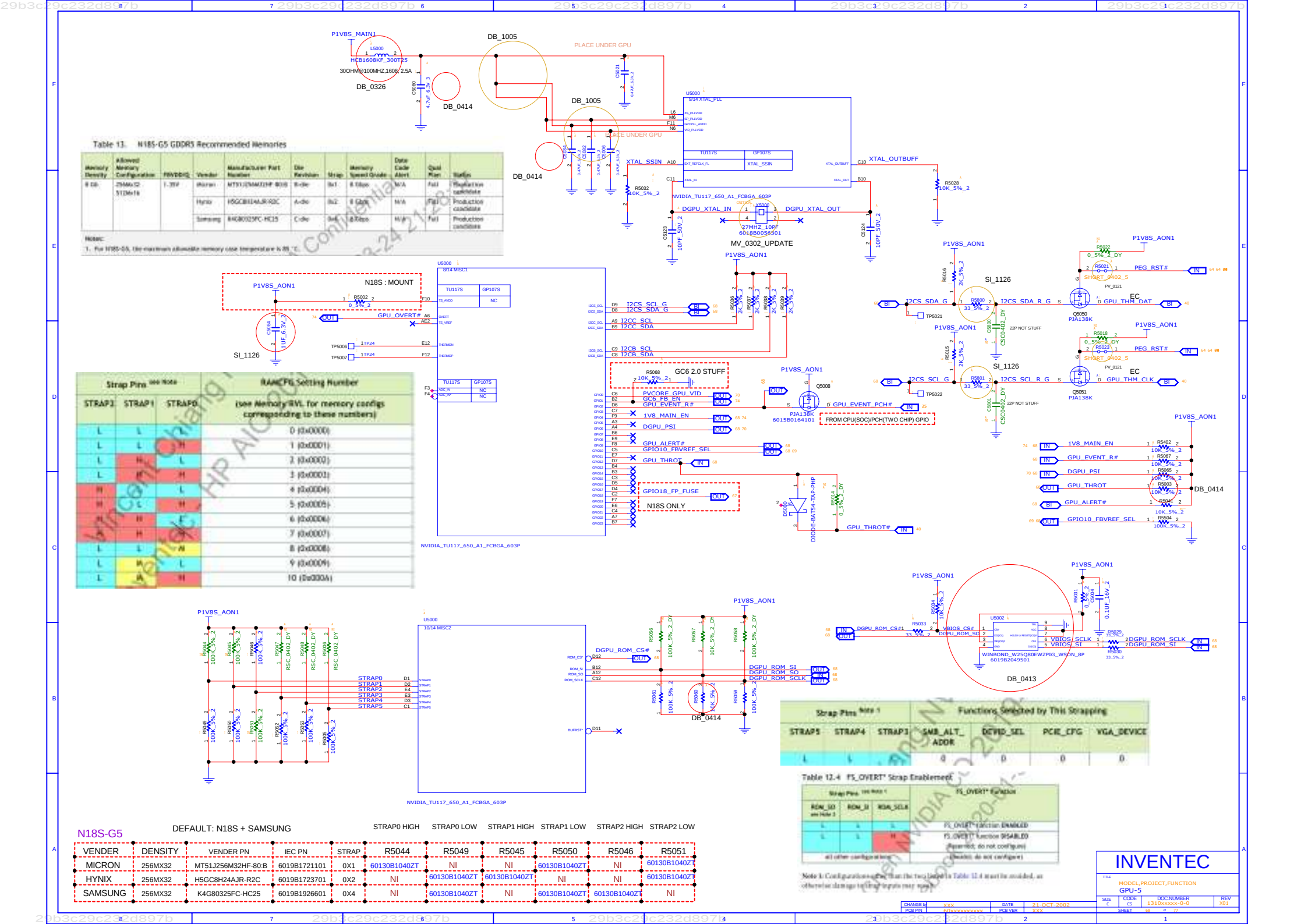
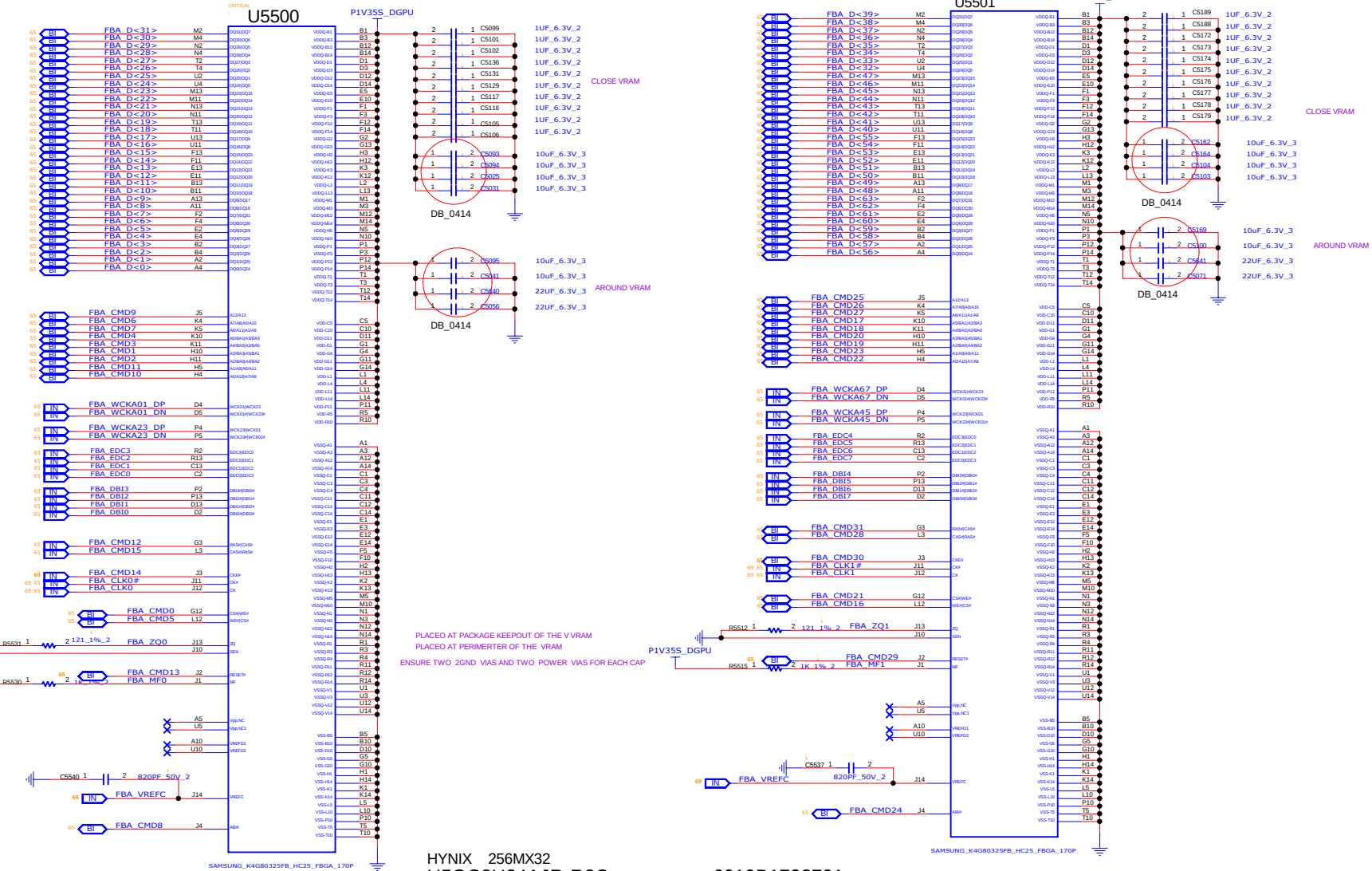
CHANGE SE	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX


U5000
PVCORE_DGPU
6/14 XVDD
NVIDIA_TU117_650_A1_FCBGA_603P
U5000
4/14 IFPAB
DVI/HDMI SL/DL
DP
TXC/TXC
TXD0/0
TXD1/1
TXD2/2
TXC
TXD0/3
TXD1/4
TXD2/5
IFPAB_RSET
IFPAB_PLLVDD
IFP_IOVDD_1
IFP_IOVDD_2
IFPAB
NVIDIA_TU117_650_A1_FCBGA_603P
U5000
13/14 GND
OPTIONAL GND:
XVDD AREA
PCB ADR/CMD
PWR REFERENCE
DB_0414
DB_0414
NVIDIA_TU117_650_A1_FCBGA_603P
U5000
3/14 JTAG
TP5001
TP5002
TP5003
TP5004
TP5005
R5054
R5009
NVIDIA_TU117_650_A1_FCBGA_603P
U5000
14/14 VDD18
GP107S
TU117S
VDD18
NC
FP_FUSE_SRC
NVIDIA_TU117_650_A1_FCBGA_603P
PLACE NEAR GPU
PLACE UNDER GPU
P1V8S_AON1
C5061
C5060
C5059
C5058
C5151
C5090
C5062
C5063
C5064
P1V8S_AON1
GPU_FP_FUSE
U5001
GMT_G5017B11U_WLCSP_4P
GPIO18_FP_FUSE
IN
C5148
R5017
C5035
R5013
SI_1126_MODIFY
INVENTEC
MODEL,PROJECT,FUNCTION
GPU-4
CHANGE NO
PCB P/N
DATE
21-OCT-2002
PCB VER
SIZE
CODE
DOC NUMBER
REV
SHEET


P1V8S_MAIN1
L5000
HCB1608KF-300T25
30OHM@100MHZ,1608,2.5A
DB_0326
DB_1005
DB_0414
PLACE UNDER GPU
U5000
9/14 XTAL_PLL
XTAL_SSIN
XTAL_OUTBUFF
NVIDIA_TU117_650_A1_FCBGA_603P
DGPU_XTAL_IN
DGPU_XTAL_OUT
27MHZ_10PF
6018B0056301
MV_0302_UPDATE
Table 13. N18S-G5 GDDR5 Recommended Memories
N18S : MOUNT
SI_1126
GPU_OVERT#
8/14 MISC1
GC6 2.0 STUFF
PVCORE_GPU_VID
GC6_FB_EN
GPU_EVENT_R#
1V8_MAIN_EN
DGPU_PSI
GPU_ALERT#
GPIO10_FBVREF_SEL
GPU_THROT
GPIO18_FP_FUSE
N18S ONLY
Q5008
PJA138K
6015B0164101
FROM CPU(SOC)/PCH(TWO CHIP) GPIO
GPU_EVENT_PCH#
DIODE-BAT54-TAP-PHP
GPU_THROT#
I2CS_SDA_G
I2CS_SCL_G
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
EC
GPU_THM_DAT
GPU_THM_CLK
PEG_RST#
Strap Pins
RAMCFG Setting Number
STRAP3
STRAP1
STRAP0
(see Memory BVL for memory configs corresponding to these numbers)
10/14 MISC2
DGPU_ROM_CS#
DGPU_ROM_SI
DGPU_ROM_SO
DGPU_ROM_SCLK
WINBOND_W25Q80EWZPIG_WSON_8P
6019B2049501
DB_0413
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
STRAP5
Functions Selected by This Strapping
SMB_ALT_ADDR
DEVID_SEL
PCIE_CFG
VGA_DEVICE
Table 12.4 FS_OVERT* Strap Enablement
FS_OVERT* Function
FS_OVERT* function ENABLED
FS_OVERT* function DISABLED
(Reserved; do not configure)
(Invalid; do not configure)
all other configurations
Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to the chip may occur.
N18S-G5
DEFAULT: N18S + SAMSUNG
STRAP0 HIGH
STRAP0 LOW
STRAP1 HIGH
STRAP1 LOW
STRAP2 HIGH
STRAP2 LOW
VENDER
DENSITY
VENDER PN
IEC PN
STRAP
R5044
R5049
R5045
R5050
R5046
R5051
MICRON
256MX32
MT51J256M32HF-80:B
6019B1721101
0X1
60130B1040ZT
NI
NI
60130B1040ZT
NI
60130B1040ZT
HYNIX
256MX32
H5GC8H24AJR-R2C
6019B1723701
0X2
NI
60130B1040ZT
60130B1040ZT
NI
NI
60130B1040ZT
SAMSUNG
256MX32
K4G80325FC-HC25
6019B1926601
0X4
NI
60130B1040ZT
NI
60130B1040ZT
60130B1040ZT
NI
INVENTEC
MODEL,PROJECT,FUNCTION
GPU-5
SIZE C
CODE CS
DOC NUMBER 1310xxxxx-D-0
REV X01
SHEET 68 of 77
CHANGE SI
PCB P/N
DATE 21-OCT-2002
PCB VER XXX

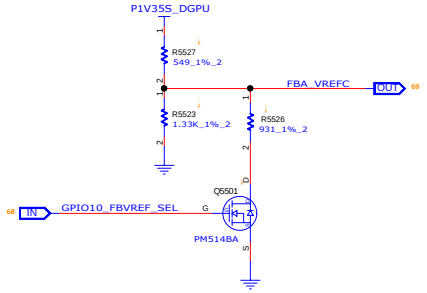
VRAM A PARTITION

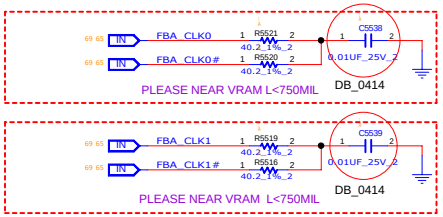


PLACEO AT PACKAGE KEEPOUT OF THE V VRAM
PLACEO AT PERIMERTER OF THE VRAM
ENSURE TWO 2GND VIAS AND TWO POWER VIAS FOR EACH CAP

HYNIX 256MX32
H5GC8H24AJR-R2C 6019B1723701

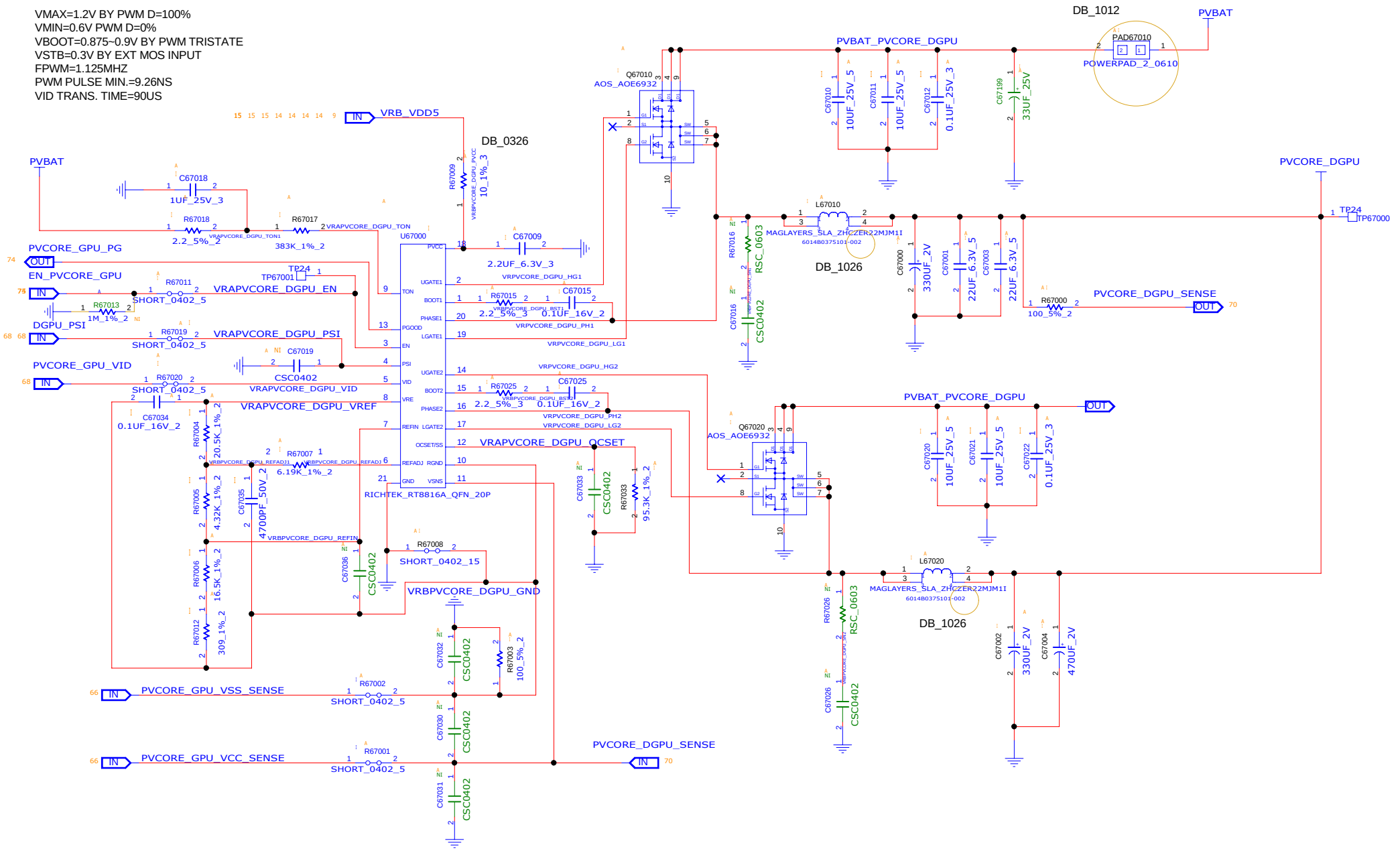
MICRON 256MX32
MT51J256M32HF-80:B 6019B1721101





DRAWN BY	XXX		
TITLE	MODEL,PROJECT,FUNCTION		
SIZE A3	DOC.NUMBER 1310xxxxx-0-0		REV X01
CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX
SHEET 69 of 77			

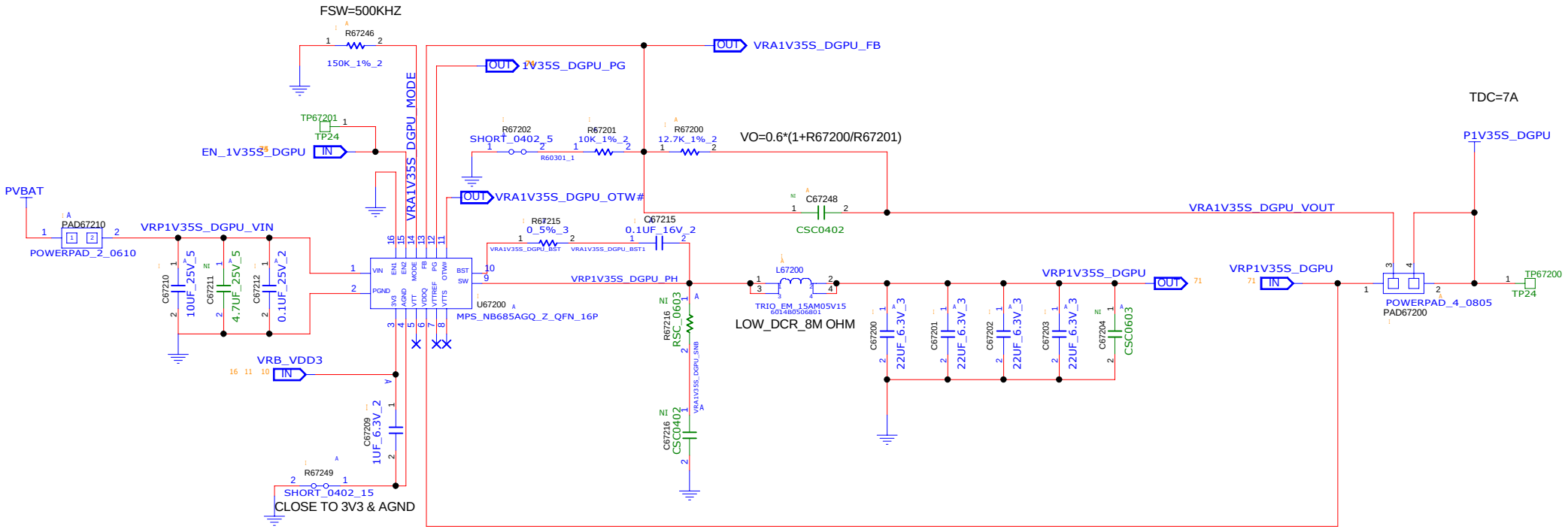
VMAX=1.2V BY PWM D=100%
VMIN=0.6V PWM D=0%
VBOOT=0.875~0.9V BY PWM TRISTATE
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=90US



	NVVDD		1.35V		1.0V		1.8V	
N18S-G5	EDP-c(A)	EDP-p(A)	EDP-c(A)	EDP-p(A)	EDP-c(A)	EDP-p(A)	EDP-c(A)	EDP-p(A)
	30	75	7	8	1.2	1.9	0.9	2

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION VCORE MOS		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by	XXX	DATE	
PCB P/N	60NGxxxxxxxx	PCB VER	XXX-OCT-2002
SHEET	of 70 77		



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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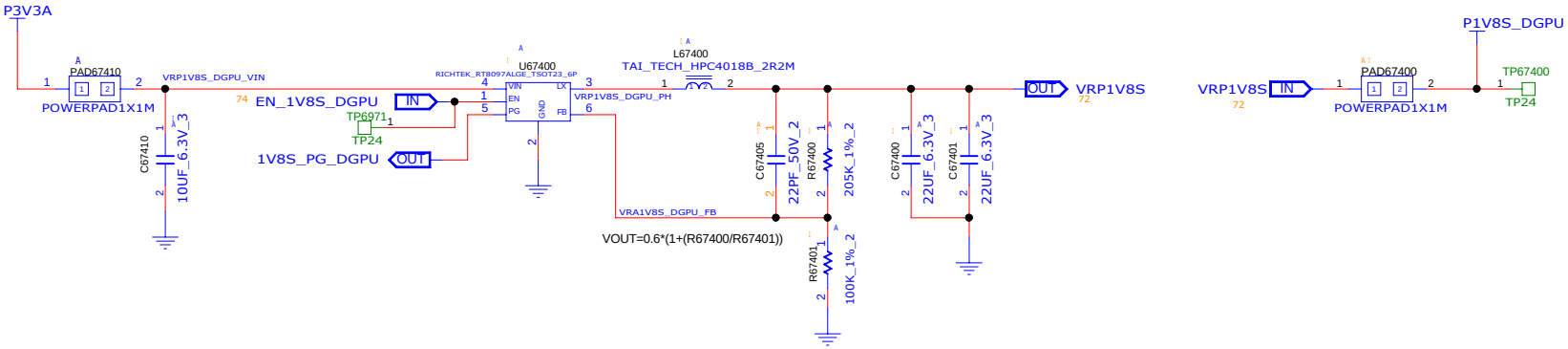
TDC=0.9A



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P1V8DS_DGPU(AP2132B)

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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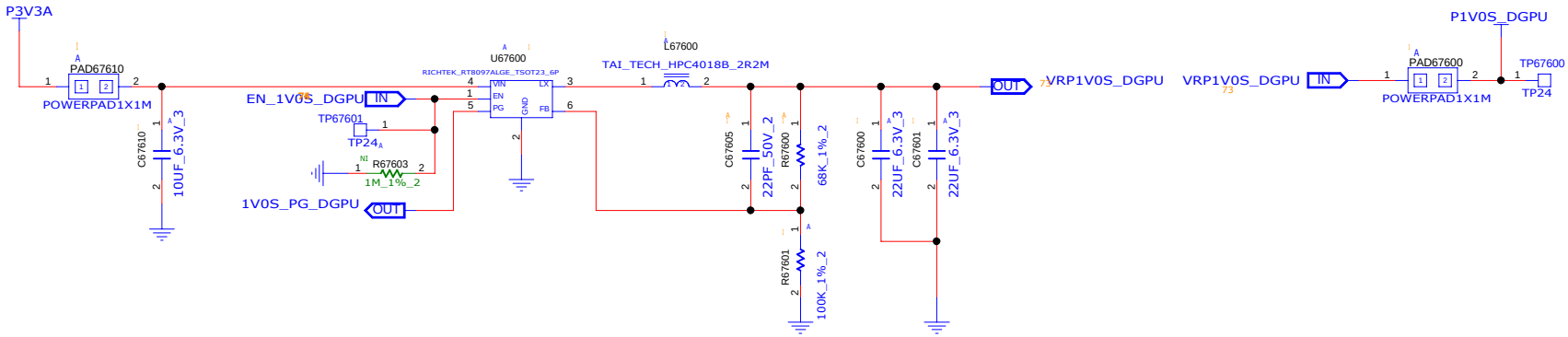
TDC=1.2A



VOUT=0.6*(1+(R67400/R67401))

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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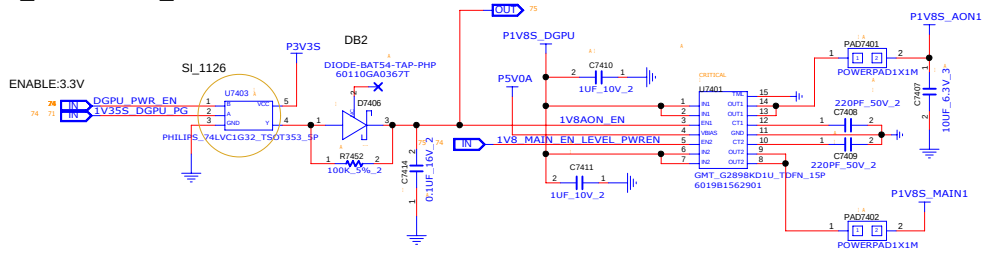
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

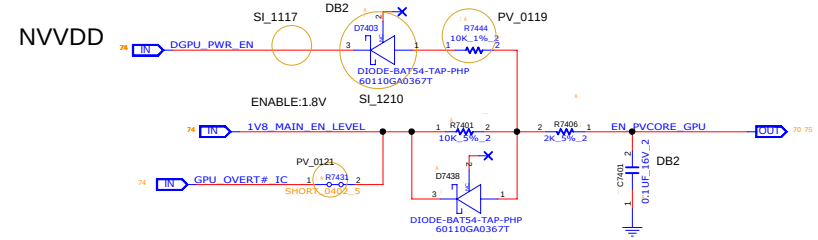
POWER_ON:P1V8S_AON1-->P1V8S_MAIN1-->NVVDD-->PEX_VDD-->FBVDD

POWER_OFF:PEX_VDD-->FBVDD-->NVVDD-->P1V8S_MAIN1-->P1V8S_AON1

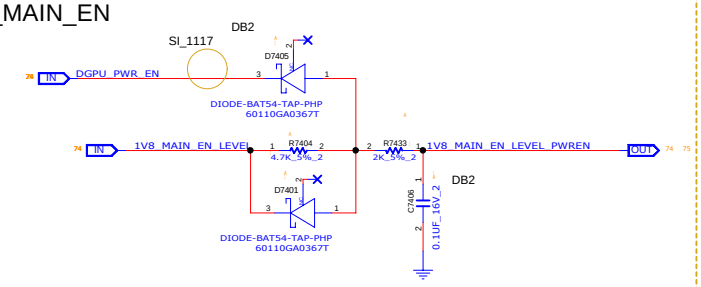
1V8_AON & 1V8_MAIN



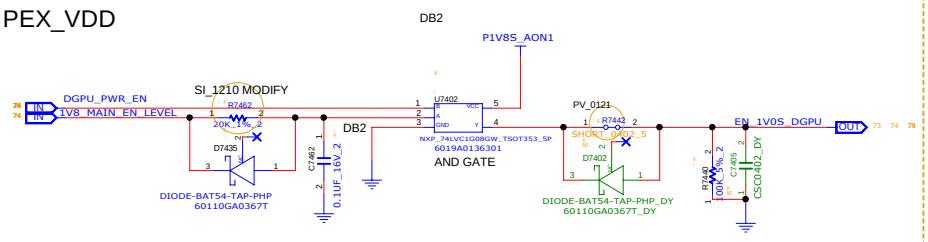
NVVDD



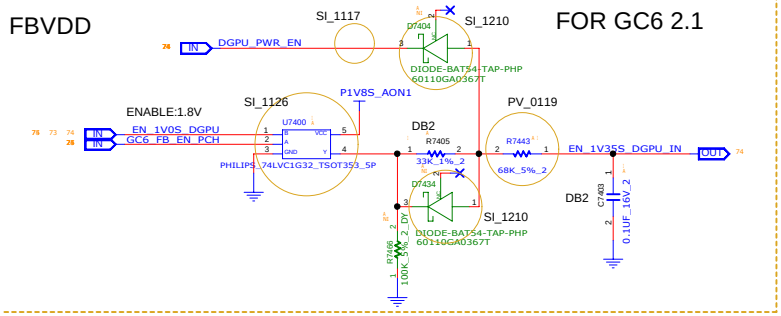
1V8_MAIN_EN

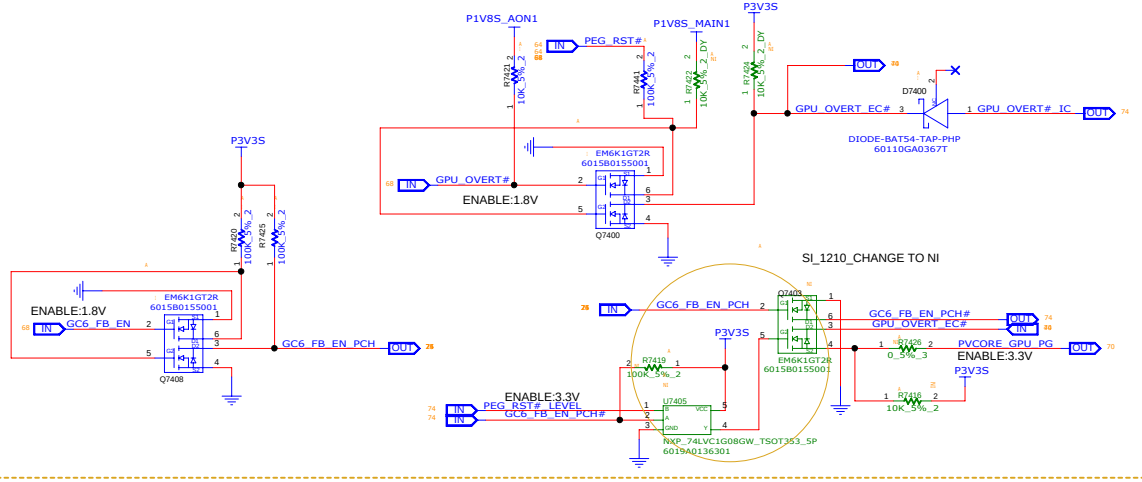


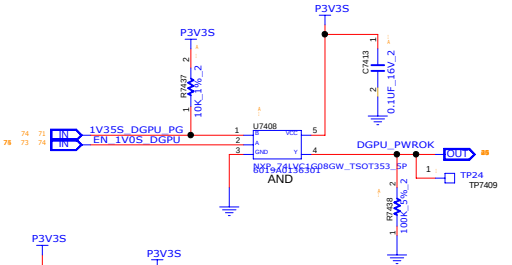
PEX_VDD

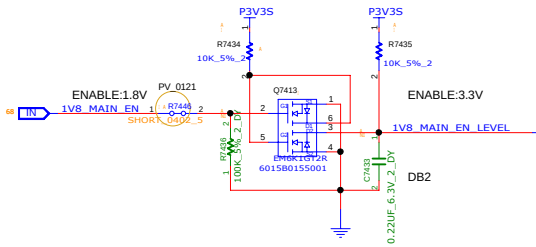


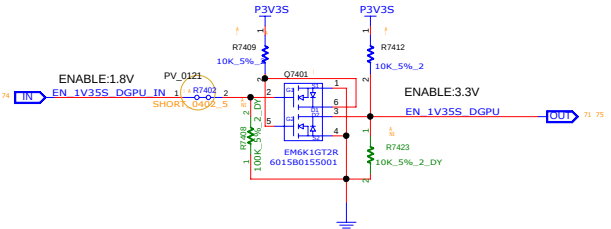
FBVDD

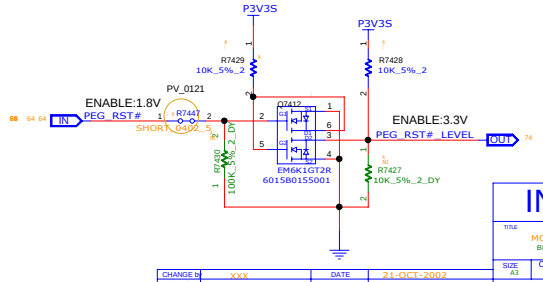












INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-0	X01

CHANGE ID	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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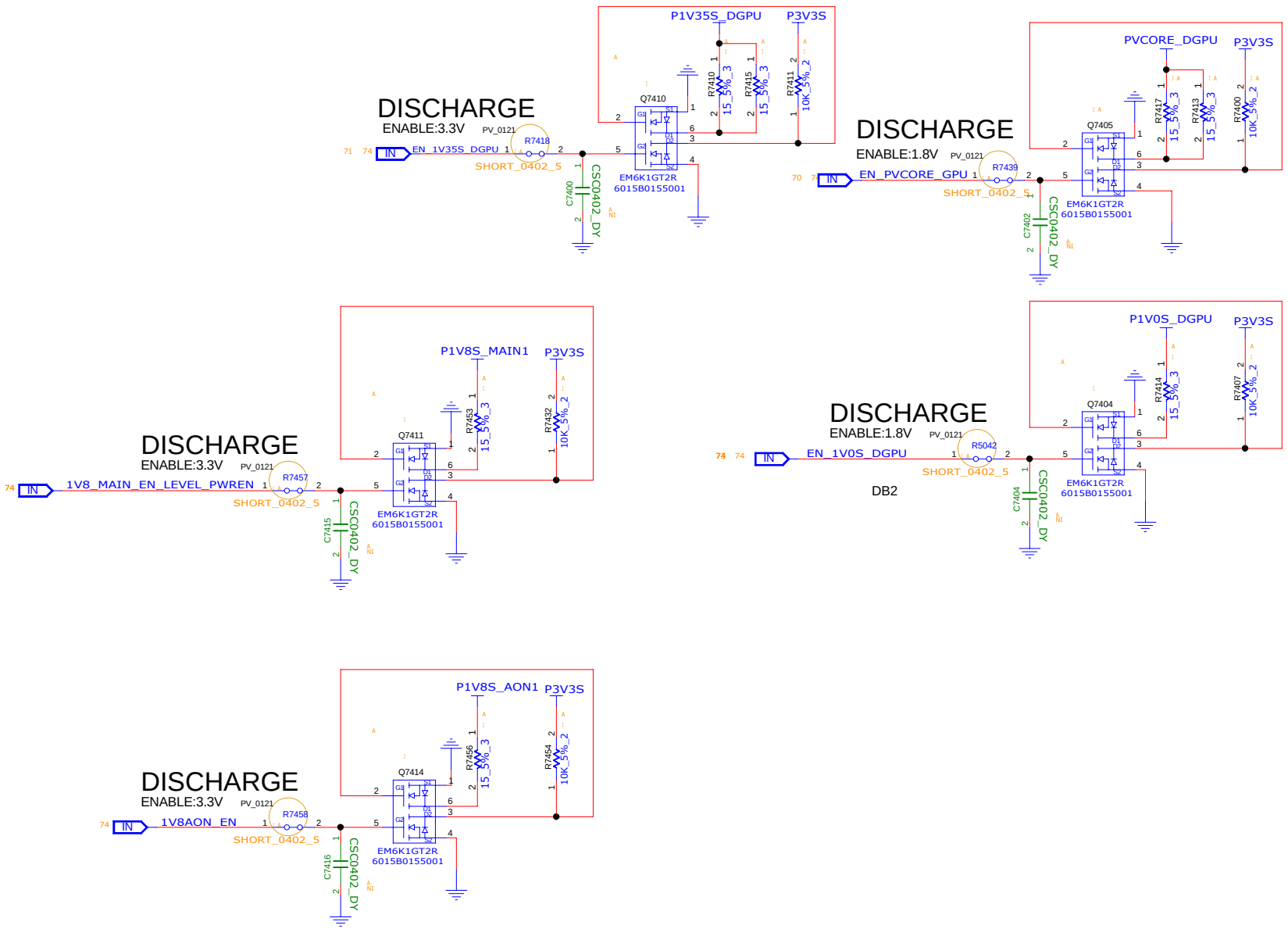

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	
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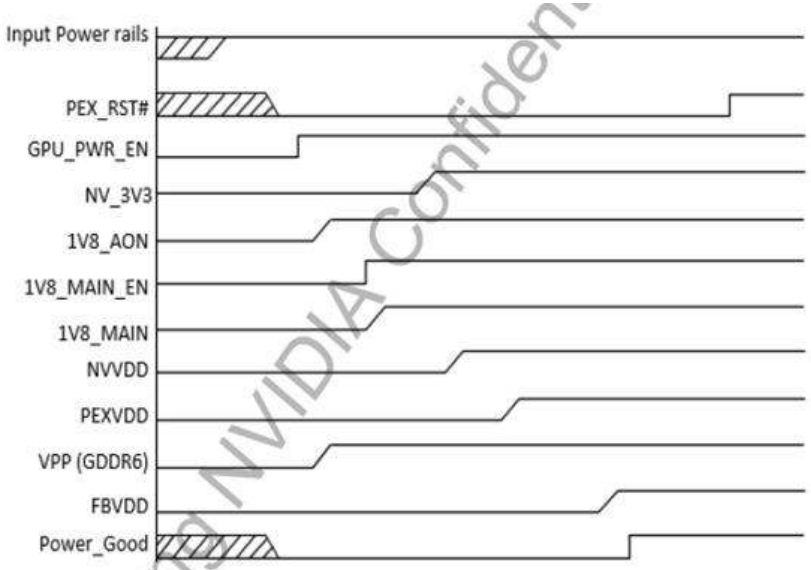

Figure 5.6 Power-Up Sequence

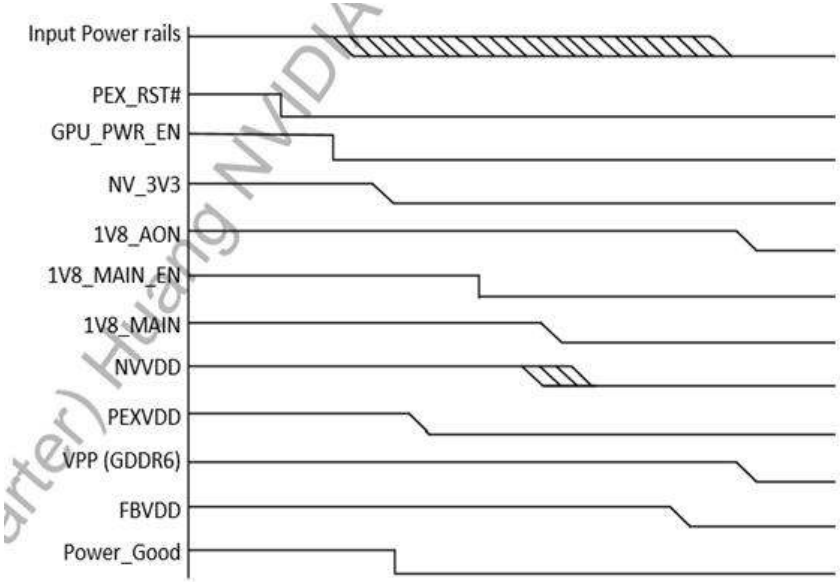

Figure 5.7 Power-Down Sequence

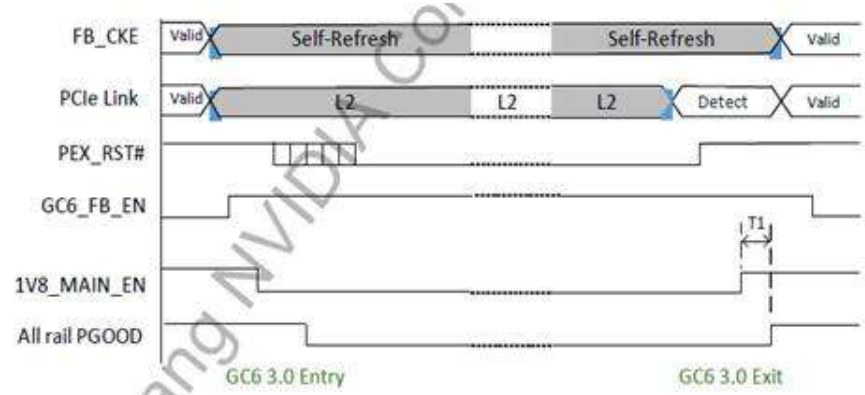

Figure 6.19 GC6 3.0 Entry/Exit Timing Sequence

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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