MS-7823

Version : 32

212mm x 231mm

Intel Sharkbay plamform B85

CPU:

INTEL-Haswell LGA1150

System Chipset:

B85

Memory:

DDRIII (1333/1666MHz) * 4 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-Atheros_E2205-B

SIO:NUVOTON 5533D

SPI ROM: 128 MB

Other:

DVI*1
VGA*1

SATA2*2
SATA3*4

FRONT USB2.0 *4
FRONT USB3.0 *2

REAL USB2.0 *2
REAL USB3.0 *2

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

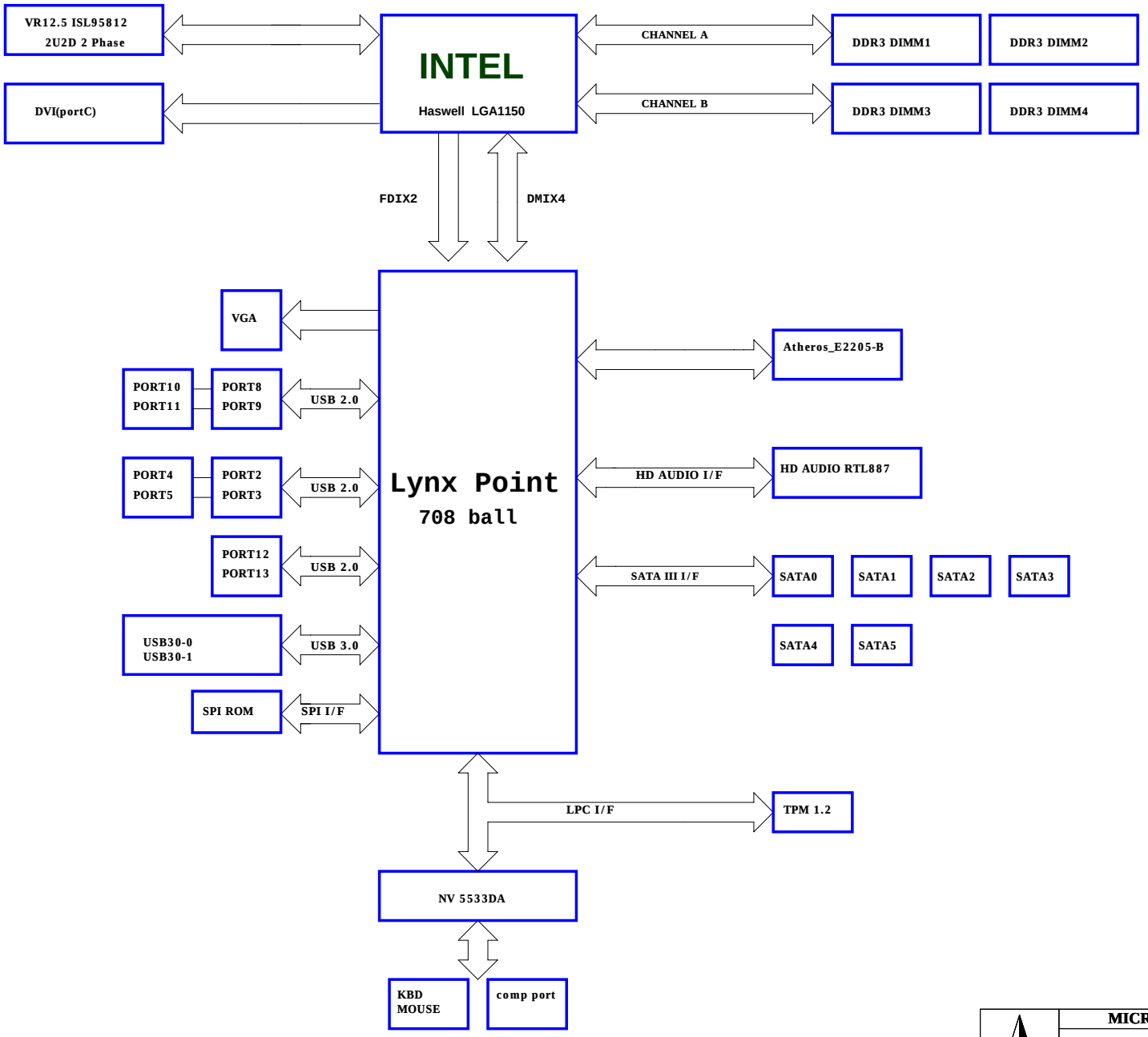
MICRO-STAR INT'L CO.,LTD

MS-7823

Size	Document Description	Rev
Custom	Cover Sheet	32

Date: Monday, October 20, 2014 Sheet 1 of 37

MS-7823 Block Diagram

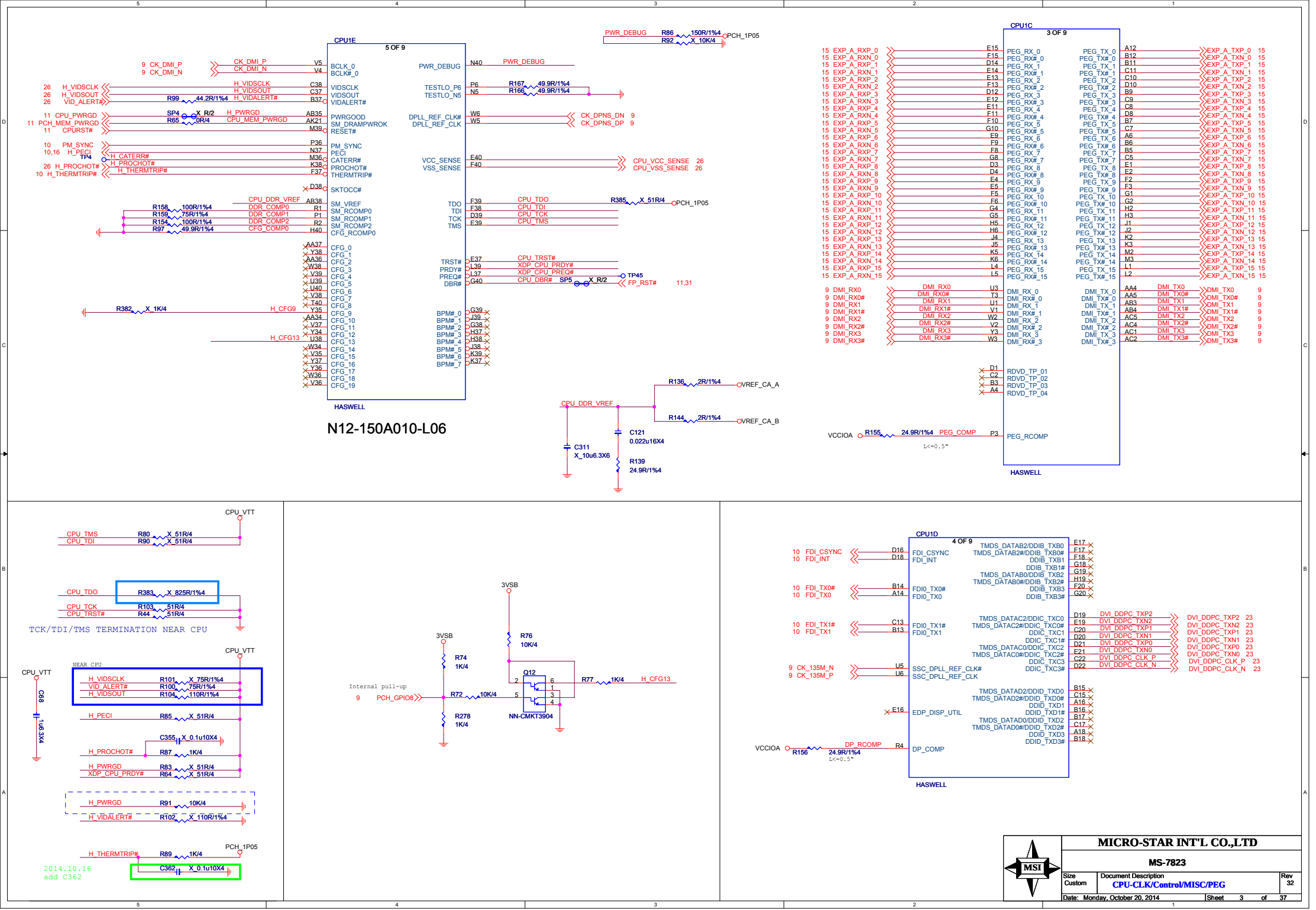


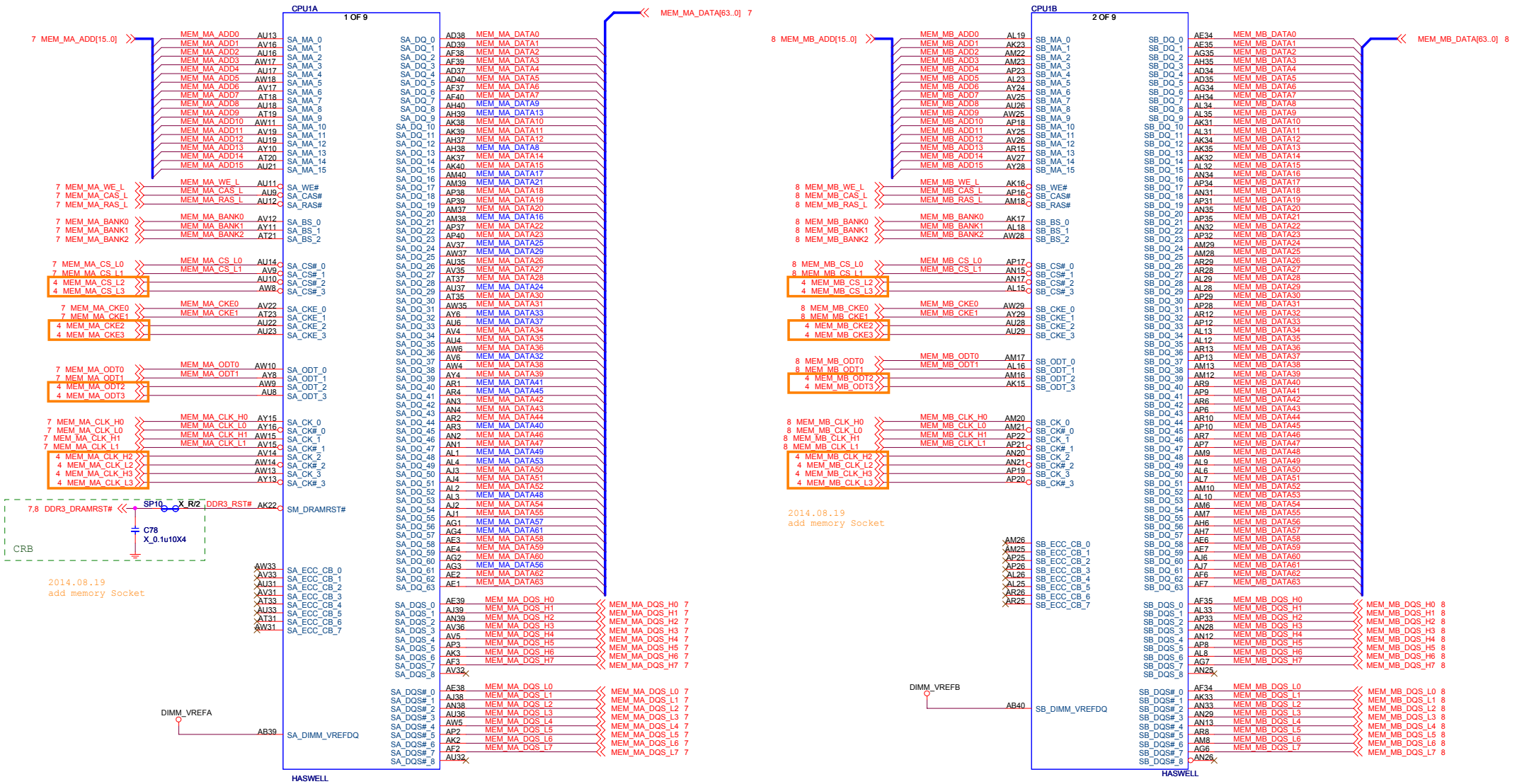
MICRO-STAR INT'L CO.,LTD

MS-7823

Size	Document Description	Rev
Custom	Block Diagram	32

Date: Monday, October 20, 2014 Sheet 2 of 37


CPU1E
5 OF 9
HASWELL
CPU1C
3 OF 9
HASWELL
CPU1D
4 OF 9
HASWELL
N12-150A010-L06
TCK/TDI/TMS TERMINATION NEAR CPU
2014.10.16
add C362
MICRO-STAR INT'L CO.,LTD
MS-7823
CPU-CLK/Control/MISC/PEG
Rev 32
Monday, October 20, 2014
Sheet 3 of 37



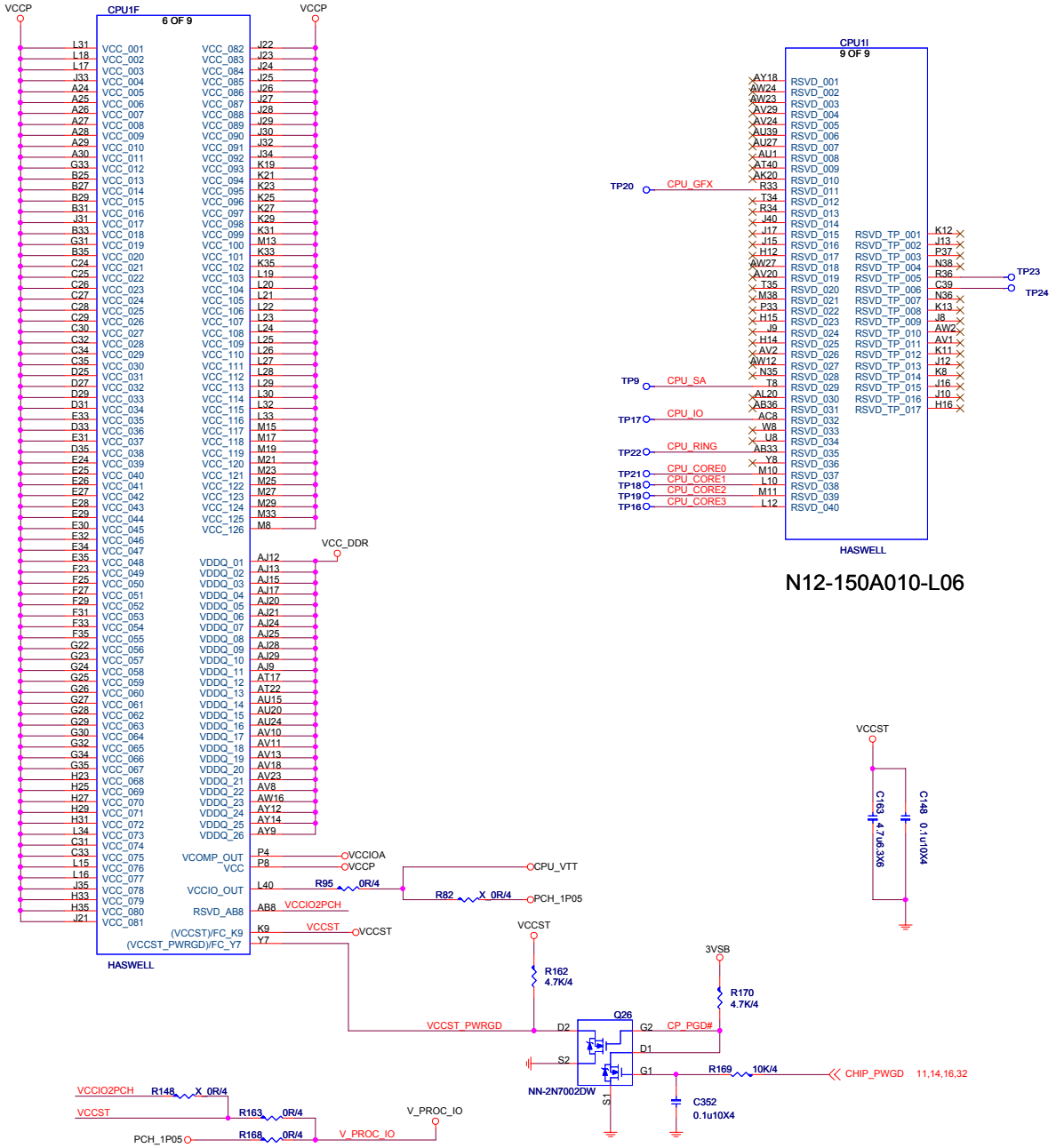
N12-150A010-L06

MICRO-STAR INT'L CO.,LTD

MS-7823

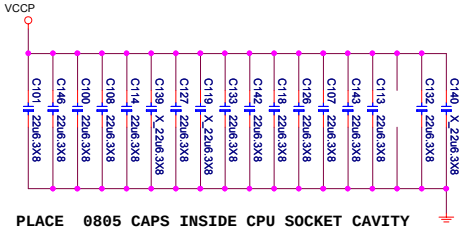
Size	Document Description	Rev
Custom	CPU-Memory	32

Date: Monday, October 20, 2014 Sheet 4 of 37



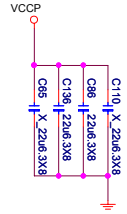
N12-150A010-L06

+CPU_VCCP-Decoupling

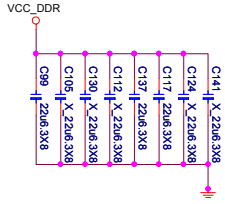


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

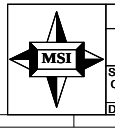
PLACE 0805 CAPS Near CPU SOCKET edge



+1.5V_DDR3-Decoupling



CPU SOCKET CAVITY CAPS

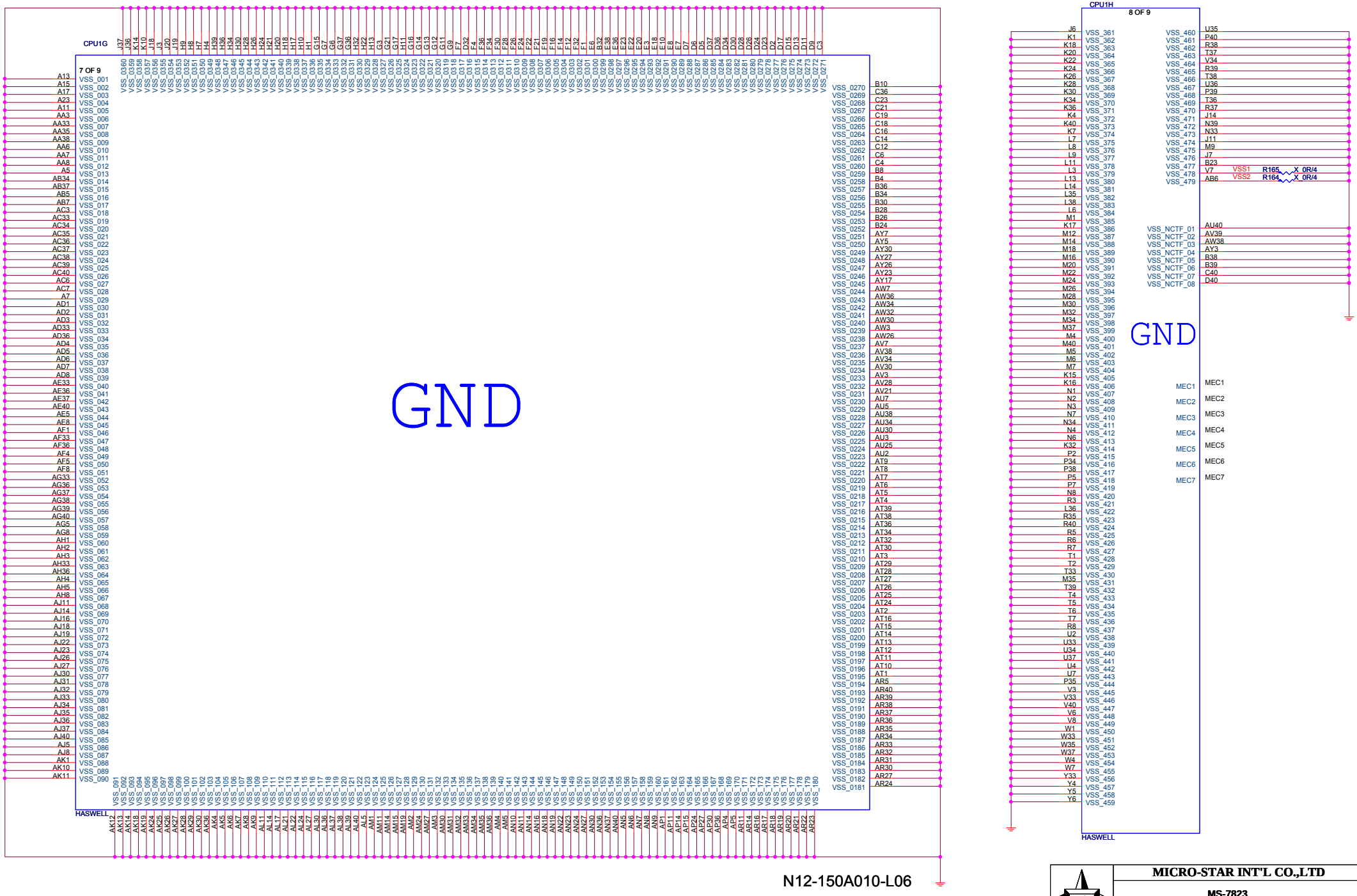


MICRO-STAR INT'L CO.,LTD

MS-7823

Size	Document Description	Rev
Custom	CPU-Power	32

Date: Monday, October 20, 2014 Sheet 5 of 37



MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: CPU-GND	Rev: 32
Date: Monday, October 20, 2014	Sheet 6 of 37	

2014.08.19
add memory Socket

A0 A1 B0 B1

Place close to DIMM1

Place close to DIMM2

D08-0100200-B07

Place close to DIMM1

DDR3

N13-2401691-L06

DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

DDRIII-240P_BLACK-RH-33

2014.10.07
DIMM1 change to using N13-2401691-L06

DDR3

N13-2401691-L06

DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

DDRIII-240P_BLACK-RH-33

2014.10.07
DIMM2 change to using N13-2401691-L06

MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: DDR3 Chanel-A DIMM1
Rev: 32	
Date: Monday, October 20, 2014	Sheet 7 of 37

DDRIII DIMM_B0

DDRIII DIMM_B1

2014.08.19
add memory Socket

4 MEM_MB_DATA[63..0]

Place close to DIMM3

VCC_DDR C270 X_0.1u/10X/4

VCC_DDR C94 0.1u10X C97 0.1u10X C269 0.1u10X

VCC_DDR EC24 2 1 CD560u6.3SO-RH-5

VCC3_SPD C361 0.1u10X C360 0.1u10X

VREF_CA_B C135 0.1u10X4 R146 1K/1%4 R145 1K/1%4

DIMM_VREFB R27 2R/1%4 VREF_DQ_B R46 1K/1%4 R34 1K/1%4 C46 0.022u16X4 R55 24.9R/1%4 VCC_DDR C27 0.1u10X4

VCC_DDR VCC3_SPD VTT_DDR

4 MEM_MB_ADD[15..0]

DIMM3

MEM_MB_DATA0 3
MEM_MB_DATA1 4
MEM_MB_DATA2 9
MEM_MB_DATA3 10
MEM_MB_DATA4 122
MEM_MB_DATA5 123
MEM_MB_DATA6 128
MEM_MB_DATA7 129
MEM_MB_DATA8 12
MEM_MB_DATA9 13
MEM_MB_DATA10 18
MEM_MB_DATA11 19
MEM_MB_DATA12 131
MEM_MB_DATA13 132
MEM_MB_DATA14 137
MEM_MB_DATA15 138
MEM_MB_DATA16 21
MEM_MB_DATA17 22
MEM_MB_DATA18 27
MEM_MB_DATA19 28
MEM_MB_DATA20 140
MEM_MB_DATA21 141
MEM_MB_DATA22 146
MEM_MB_DATA23 147
MEM_MB_DATA24 30
MEM_MB_DATA25 31
MEM_MB_DATA26 36
MEM_MB_DATA27 37
MEM_MB_DATA28 149
MEM_MB_DATA29 150
MEM_MB_DATA30 155
MEM_MB_DATA31 156
MEM_MB_DATA32 81
MEM_MB_DATA33 82
MEM_MB_DATA34 87
MEM_MB_DATA35 88
MEM_MB_DATA36 200
MEM_MB_DATA37 201
MEM_MB_DATA38 206
MEM_MB_DATA39 207
MEM_MB_DATA40 90
MEM_MB_DATA41 91
MEM_MB_DATA42 96
MEM_MB_DATA43 97
MEM_MB_DATA44 209
MEM_MB_DATA45 210
MEM_MB_DATA46 215
MEM_MB_DATA47 216
MEM_MB_DATA48 99
MEM_MB_DATA49 100
MEM_MB_DATA50 105
MEM_MB_DATA51 106
MEM_MB_DATA52 218
MEM_MB_DATA53 219
MEM_MB_DATA54 224
MEM_MB_DATA55 225
MEM_MB_DATA56 108
MEM_MB_DATA57 109
MEM_MB_DATA58 114
MEM_MB_DATA59 115
MEM_MB_DATA60 227
MEM_MB_DATA61 228
MEM_MB_DATA62 233
MEM_MB_DATA63 234

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

VSS

VDD VDDSPD VTT NC/PAR_IN NC/ERR_OUT NC/TEST RSVD FREE1 FREE2 FREE3 FREE4

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15

MEM_MB_ADD0 MEM_MB_ADD1 MEM_MB_ADD2 MEM_MB_ADD3 MEM_MB_ADD4 MEM_MB_ADD5 MEM_MB_ADD6 MEM_MB_ADD7 MEM_MB_ADD8 MEM_MB_ADD9 MEM_MB_ADD10 MEM_MB_ADD11 MEM_MB_ADD12 MEM_MB_ADD13 MEM_MB_ADD14 MEM_MB_ADD15

CB0 CB1 CB2 CB3 CB4 CB5 CB6 CB7

DQS0 DQS0# DQS1 DQS1# DQS2 DQS2# DQS3 DQS3# DQS4 DQS4# DQS5 DQS5# DQS6 DQS6# DQS7 DQS7# DQS8 DQS8#

MEM_MB_DQS_H0 MEM_MB_DQS_L0 MEM_MB_DQS_H1 MEM_MB_DQS_L1 MEM_MB_DQS_H2 MEM_MB_DQS_L2 MEM_MB_DQS_H3 MEM_MB_DQS_L3 MEM_MB_DQS_H4 MEM_MB_DQS_L4 MEM_MB_DQS_H5 MEM_MB_DQS_L5 MEM_MB_DQS_H6 MEM_MB_DQS_L6 MEM_MB_DQS_H7 MEM_MB_DQS_L7

DM0/DQS9 NC/DQS9# DM1/DQS10 NC/DQS10# DM2/DQS11 NC/DQS11# DM3/DQS12 NC/DQS12# DM4/DQS13 NC/DQS13# DM5/DQS14 NC/DQS14# DM6/DQS15 NC/DQS15# DM7/DQS16 NC/DQS16# DM8/DQS17 NC/DQS17#

ODT0 ODT1 CKE0 CKE1 CS0# CS1# BA0 BA1 BA2 WE# RAS# CAS# RESET# CK0 CK0# CK1(NU) CK1#(NU) VREFDQ VREFCA SCL SDA SA1 SA0

MEM_MB_ODT0 MEM_MB_ODT1 MEM_MB_CKE0 MEM_MB_CKE1 MEM_MB_CS_L0 MEM_MB_CS_L1 MEM_MB_BANK0 MEM_MB_BANK1 MEM_MB_BANK2 MEM_MB_WE_L MEM_MB_RAS_L MEM_MB_CAS_L DDR3_DRAMRST# MEM_MB_CLK_H0 MEM_MB_CLK_L0 MEM_MB_CLK_H1 MEM_MB_CLK_L1 VREF_DQ_B VREF_CA_B SMBCLK_DDR SMBDATA_DDR VCC3_SPD

SMEC1 SMEC2 SMEC3

C129 0.1u10X4 C26 0.1u10X4

DDR3

N13-2401691-L06

DIMM3(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]

DDRIII-240P_BLACK-RH-33

2014.10.07
DIMM3 change to using N13-2401691-L06

SMBCLK_DDR SMBCLK_DDR 7
SMBDATA_DDR SMBDATA_DDR 7

DIMM4

MEM_MB_DATA0 3
MEM_MB_DATA1 4
MEM_MB_DATA2 9
MEM_MB_DATA3 10
MEM_MB_DATA4 122
MEM_MB_DATA5 123
MEM_MB_DATA6 128
MEM_MB_DATA7 129
MEM_MB_DATA8 12
MEM_MB_DATA9 13
MEM_MB_DATA10 18
MEM_MB_DATA11 19
MEM_MB_DATA12 131
MEM_MB_DATA13 132
MEM_MB_DATA14 137
MEM_MB_DATA15 138
MEM_MB_DATA16 21
MEM_MB_DATA17 22
MEM_MB_DATA18 27
MEM_MB_DATA19 28
MEM_MB_DATA20 140
MEM_MB_DATA21 141
MEM_MB_DATA22 146
MEM_MB_DATA23 147
MEM_MB_DATA24 30
MEM_MB_DATA25 31
MEM_MB_DATA26 36
MEM_MB_DATA27 37
MEM_MB_DATA28 149
MEM_MB_DATA29 150
MEM_MB_DATA30 155
MEM_MB_DATA31 156
MEM_MB_DATA32 81
MEM_MB_DATA33 82
MEM_MB_DATA34 87
MEM_MB_DATA35 88
MEM_MB_DATA36 200
MEM_MB_DATA37 201
MEM_MB_DATA38 206
MEM_MB_DATA39 207
MEM_MB_DATA40 90
MEM_MB_DATA41 91
MEM_MB_DATA42 96
MEM_MB_DATA43 97
MEM_MB_DATA44 209
MEM_MB_DATA45 210
MEM_MB_DATA46 215
MEM_MB_DATA47 216
MEM_MB_DATA48 99
MEM_MB_DATA49 100
MEM_MB_DATA50 105
MEM_MB_DATA51 106
MEM_MB_DATA52 218
MEM_MB_DATA53 219
MEM_MB_DATA54 224
MEM_MB_DATA55 225
MEM_MB_DATA56 108
MEM_MB_DATA57 109
MEM_MB_DATA58 114
MEM_MB_DATA59 115
MEM_MB_DATA60 227
MEM_MB_DATA61 228
MEM_MB_DATA62 233
MEM_MB_DATA63 234

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

VSS

VDD VDDSPD VTT NC/PAR_IN NC/ERR_OUT NC/TEST4 RSVD FREE1 FREE2 FREE3 FREE4

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15

MEM_MB_ADD0 MEM_MB_ADD1 MEM_MB_ADD2 MEM_MB_ADD3 MEM_MB_ADD4 MEM_MB_ADD5 MEM_MB_ADD6 MEM_MB_ADD7 MEM_MB_ADD8 MEM_MB_ADD9 MEM_MB_ADD10 MEM_MB_ADD11 MEM_MB_ADD12 MEM_MB_ADD13 MEM_MB_ADD14 MEM_MB_ADD15

CB0 CB1 CB2 CB3 CB4 CB5 CB6 CB7

DQS0 DQS0# DQS1 DQS1# DQS2 DQS2# DQS3 DQS3# DQS4 DQS4# DQS5 DQS5# DQS6 DQS6# DQS7 DQS7# DQS8 DQS8#

MEM_MB_DQS_H0 MEM_MB_DQS_L0 MEM_MB_DQS_H1 MEM_MB_DQS_L1 MEM_MB_DQS_H2 MEM_MB_DQS_L2 MEM_MB_DQS_H3 MEM_MB_DQS_L3 MEM_MB_DQS_H4 MEM_MB_DQS_L4 MEM_MB_DQS_H5 MEM_MB_DQS_L5 MEM_MB_DQS_H6 MEM_MB_DQS_L6 MEM_MB_DQS_H7 MEM_MB_DQS_L7

DM0/DQS9 NC/DQS9# DM1/DQS10 NC/DQS10# DM2/DQS11 NC/DQS11# DM3/DQS12 NC/DQS12# DM4/DQS13 NC/DQS13# DM5/DQS14 NC/DQS14# DM6/DQS15 NC/DQS15# DM7/DQS16 NC/DQS16# DM8/DQS17 NC/DQS17#

ODT0 ODT1 CKE0 CKE1 CS0# CS1# BA0 BA1 BA2 WE# RAS# CAS# RESET# CK0 CK0# CK1(NU) CK1#(NU) VREFDQ VREFCA SCL SDA SA1 SA0

MEM_MB_ODT2 MEM_MB_ODT3 MEM_MB_CKE2 MEM_MB_CKE3 MEM_MB_CS_L2 MEM_MB_CS_L3 MEM_MB_BANK0 MEM_MB_BANK1 MEM_MB_BANK2 MEM_MB_WE_L MEM_MB_RAS_L MEM_MB_CAS_L DDR3_DRAMRST# MEM_MB_CLK_H2 MEM_MB_CLK_L2 MEM_MB_CLK_H3 MEM_MB_CLK_L3 VREF_DQ_B VREF_CA_B SMBCLK_DDR SMBDATA_DDR VCC3_SPD

SMEC1 SMEC2 SMEC3

C179 0.1u10X4 C36 0.1u10X4

DDR3

N13-2401691-L06

DIMM4(CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]

DDRIII-240P_BLACK-RH-33

2014.10.07
DIMM4 change to using N13-2401691-L06

MICRO-STAR INT'L CO.,LTD

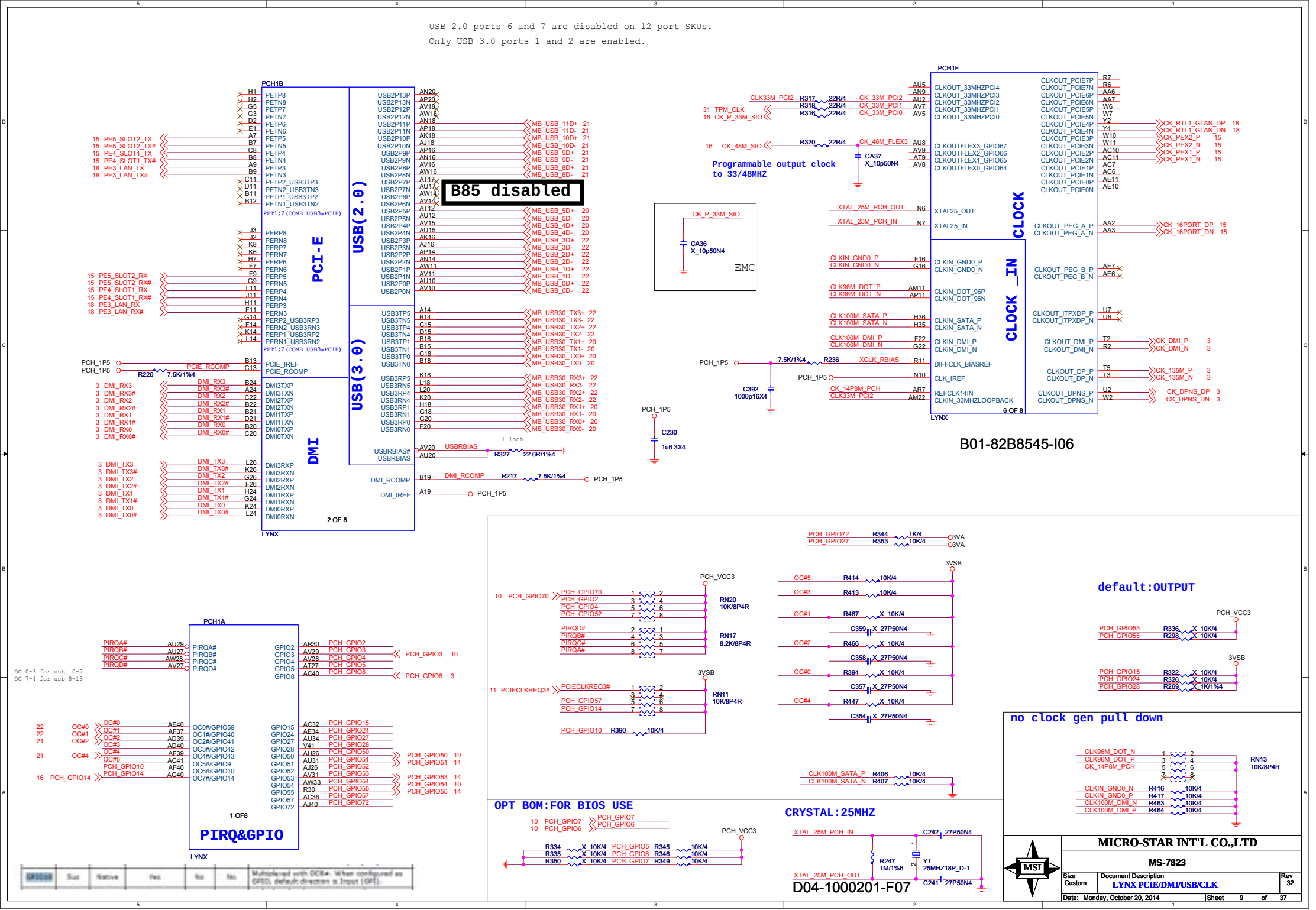
MS-7823

Size	Document Description	Rev
Custom	DDR3 Chanel-B DIMM2	32

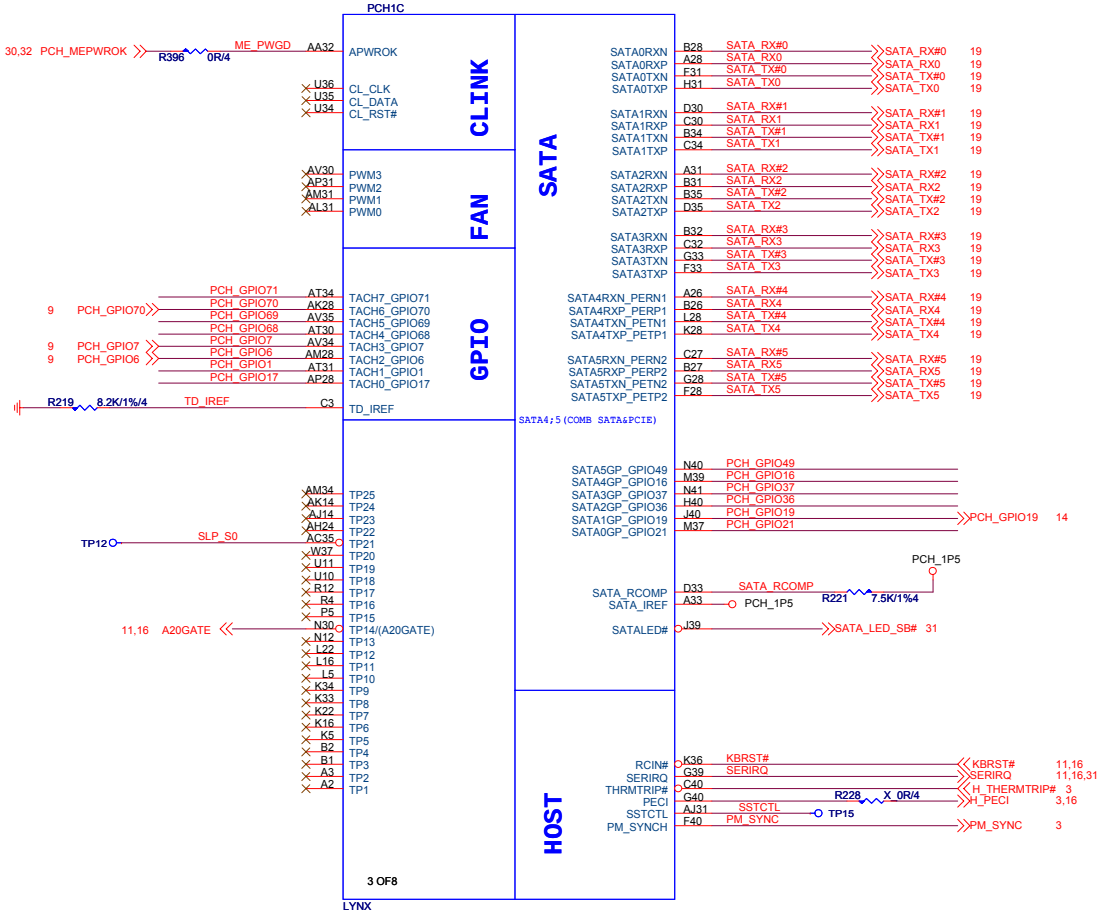
Date: Monday, October 20, 2014 Sheet 8 of 37

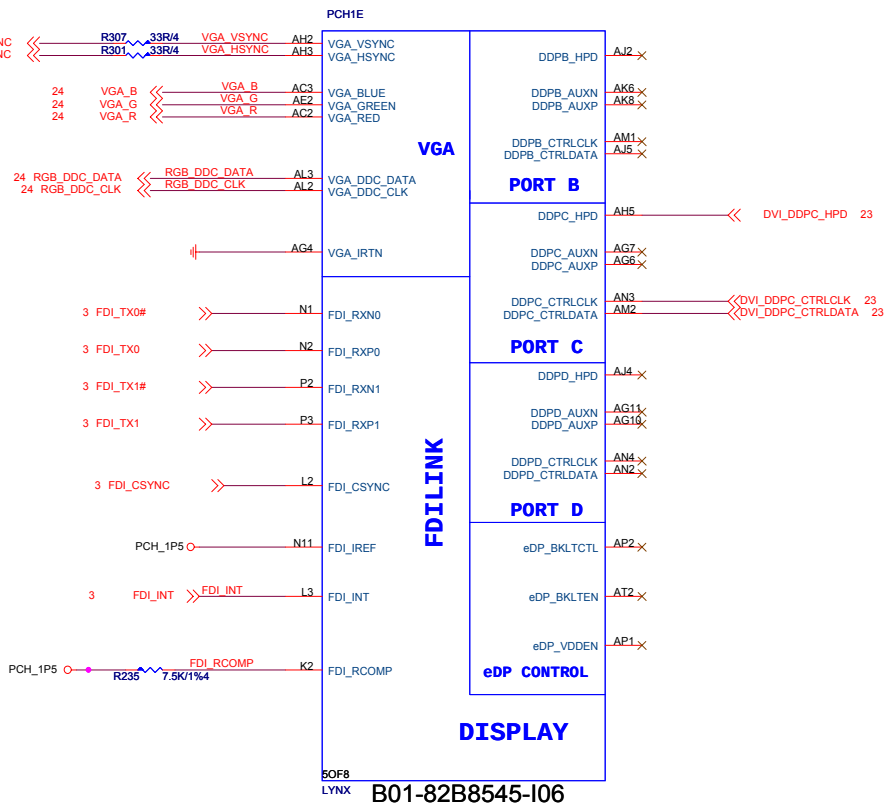
USB 2.0 ports 6 and 7 are disabled on 12 port SKUs.

Only USB 3.0 ports 1 and 2 are enabled.



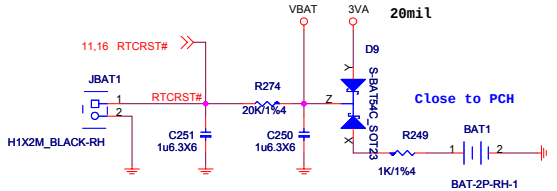
SATA ports 2 and 3 are disabled on 4 port SKUs.
SATA 6 Gb/s support on ports 0 and 1 only.





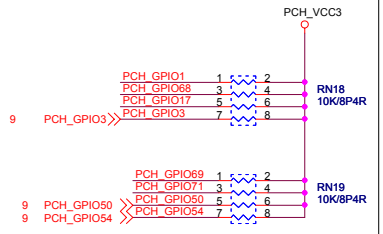
B01-82B8545-I06

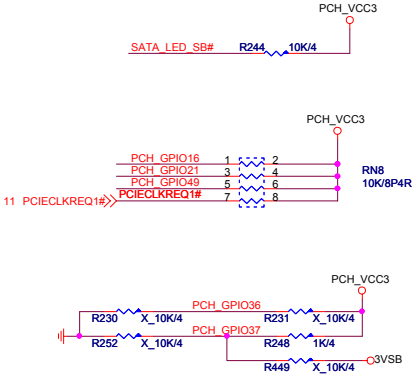
RTC and CLR_CMOS



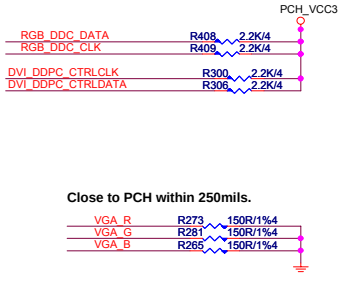
N31-1020151-H06

N91-01F0151-L06

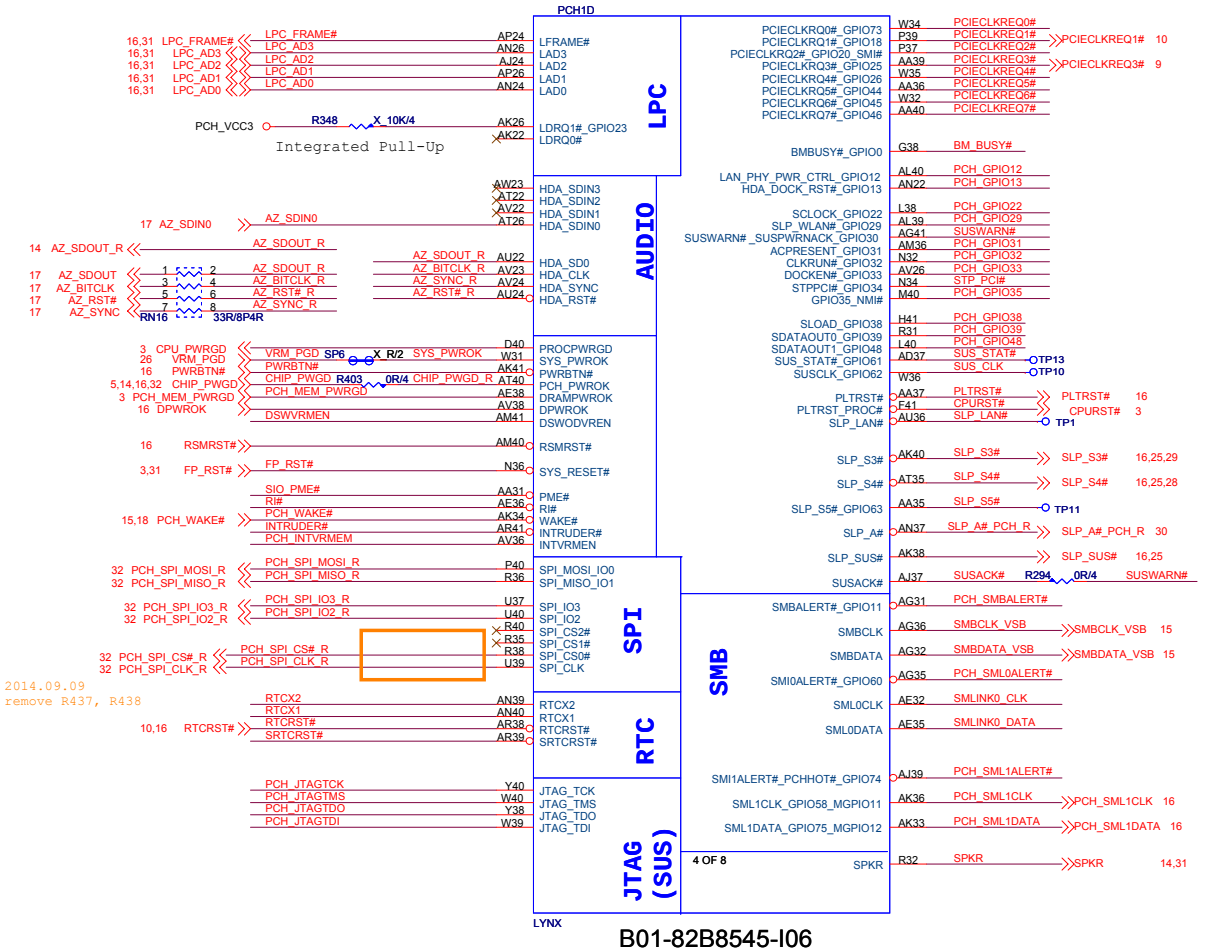




Enable VGA(CTRLCLK/DATA Pull High)

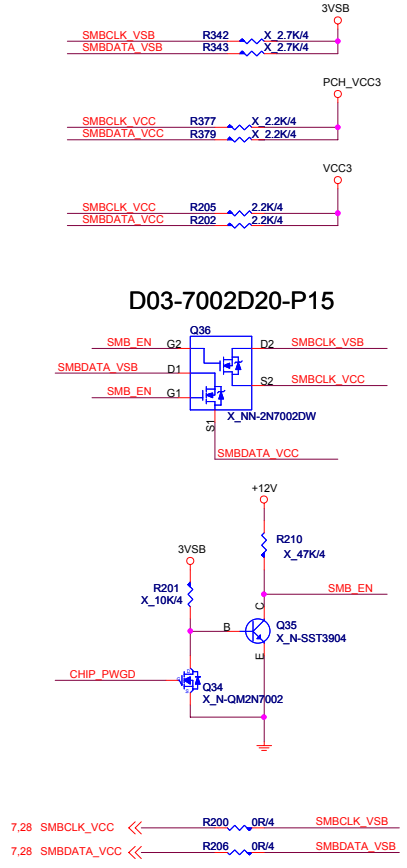


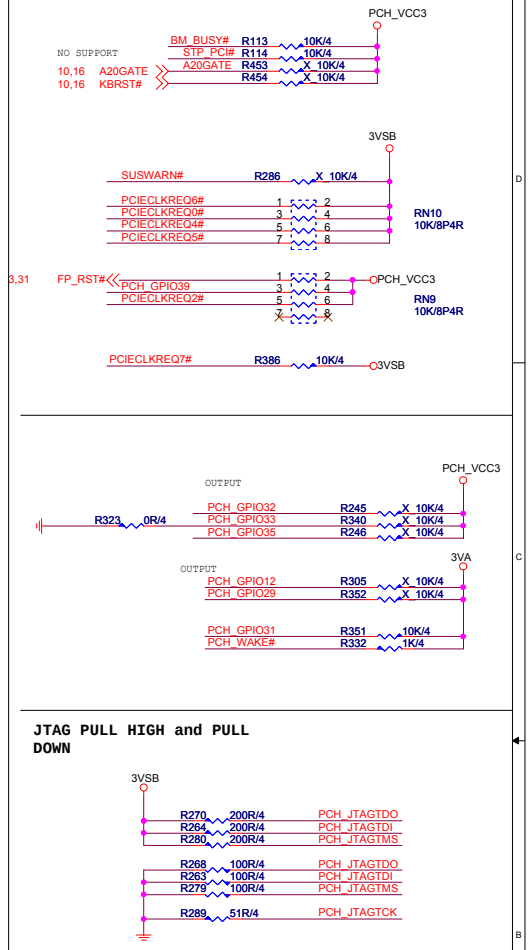
MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: LYNX-SATA/HOST/GPIO/VGA
Rev: 32	
Date: Monday, October 20, 2014	Sheet 10 of 37



B01-82B8545-I06

SMBUS
VSB TO PCH & PCIE
VCC TO DDR & XDP

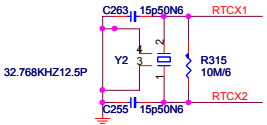




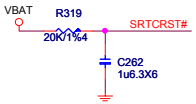
JTAG PULL HIGH and PULL DOWN

RTC Block

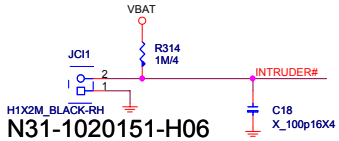
Close to PCH



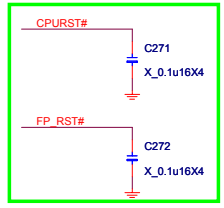
D04-0301211-F07



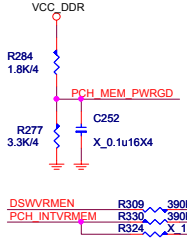
Chassis Intrusion

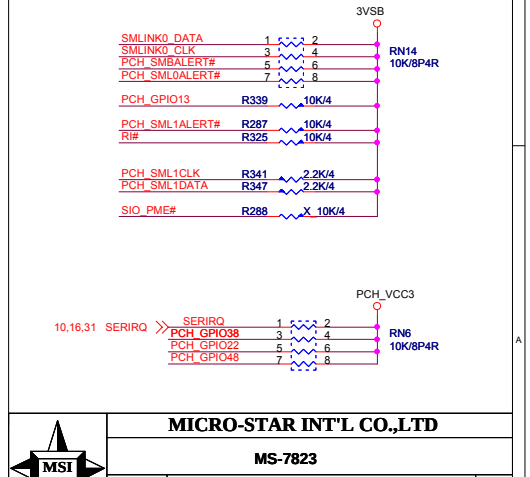


N31-1020151-H06



2014.10.16
add C271, C272





MICRO-STAR INT'L CO.,LTD

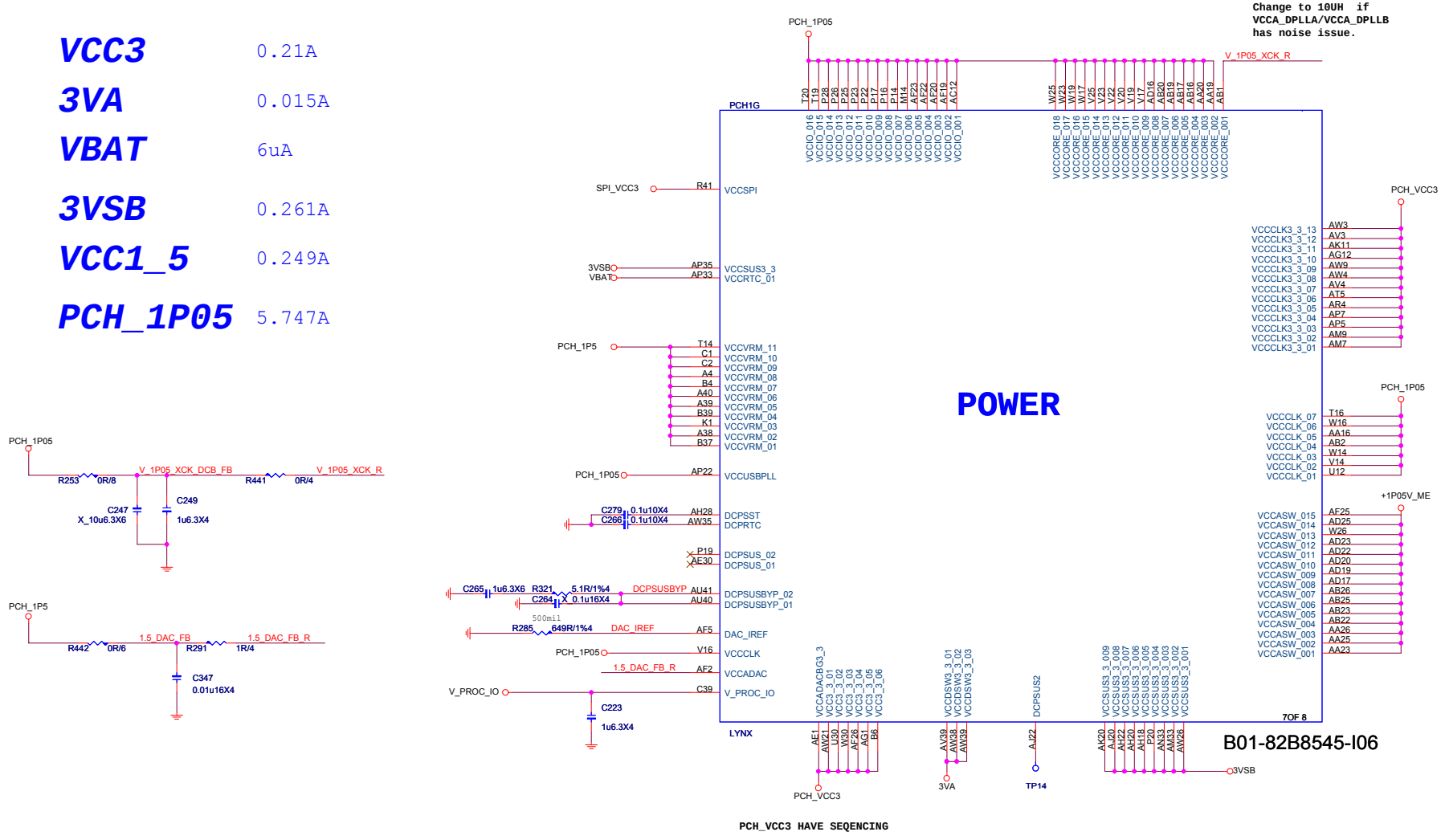
MS-7823

Size	Document Description	Rev
Custom	LYNX-SMB/LPC/AUDIO/RTC	32

Date: Monday, October 20, 2014 | Sheet 11 of 37

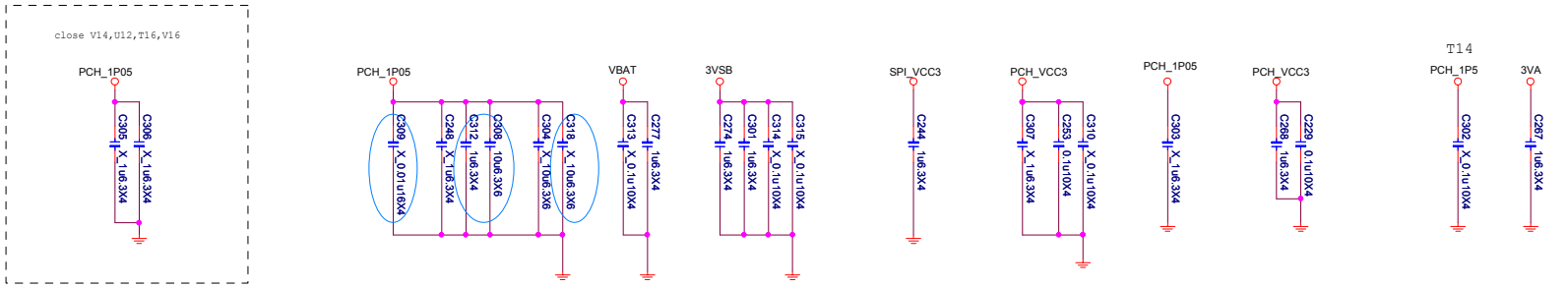
VCC3	0.21A
3VA	0.015A
VBAT	6uA
3VSB	0.261A
VCC1_5	0.249A
PCH_1P05	5.747A

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

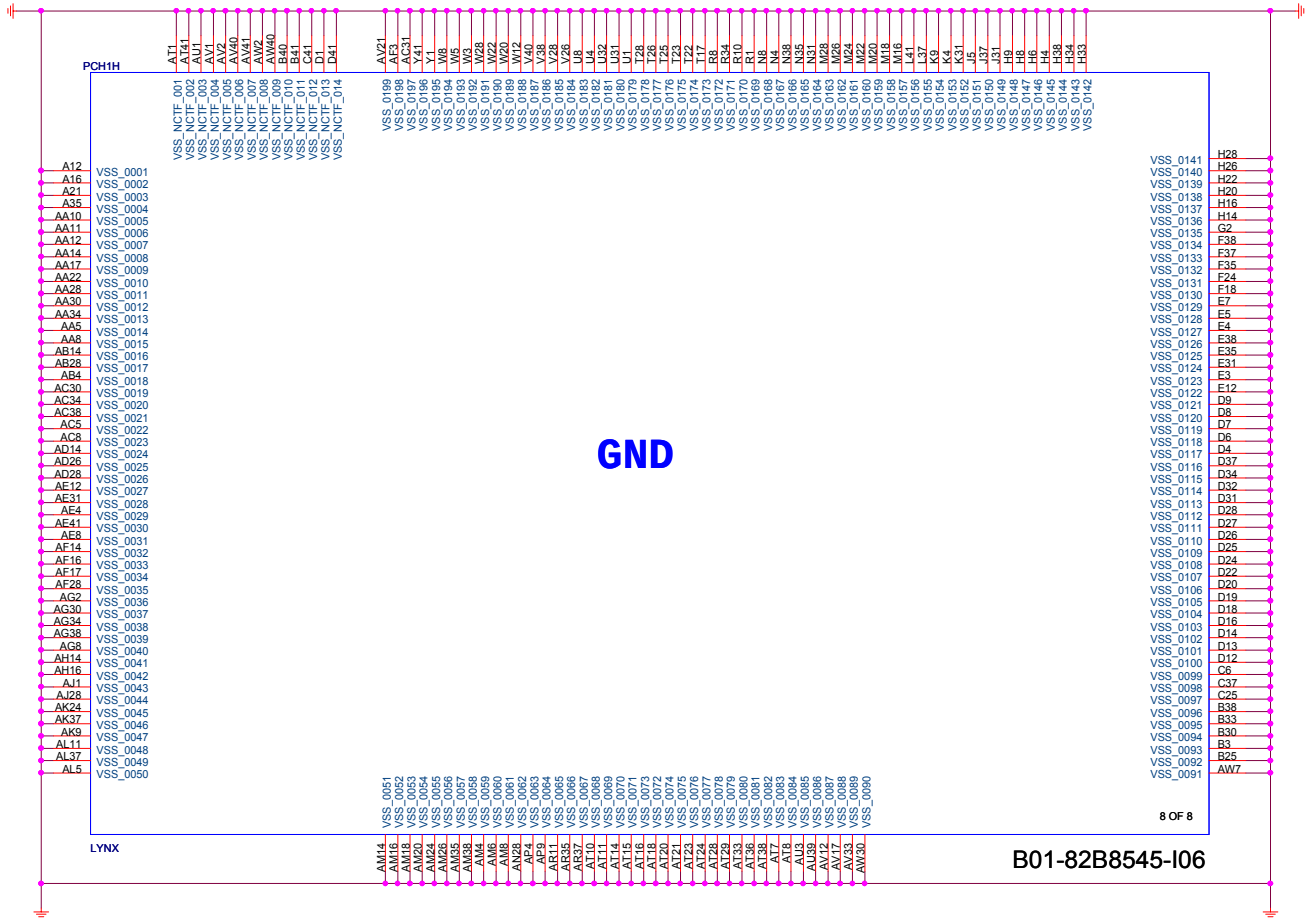


PCH_VCC3 HAVE SEQENCING

PCH decoupling cap

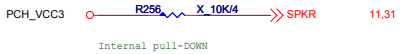


MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: LYNX -POWER PIN	Rev: 32
Date: Monday, October 20, 2014	Sheet 12 of 37	



MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: LYNX-GND
Rev: 32	
Date: Monday, October 20, 2014	Sheet 13 of 37

PCH Straps



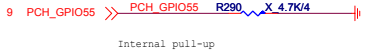
SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:

Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



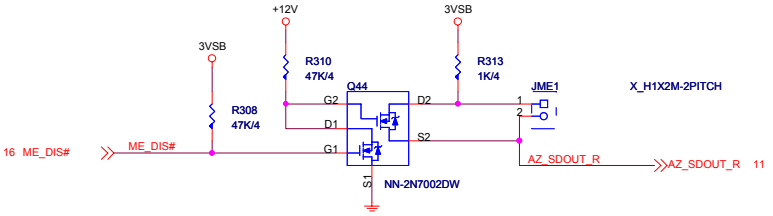
GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:

Connect to ground with 4.7k Ohm weak pulldown resistor.



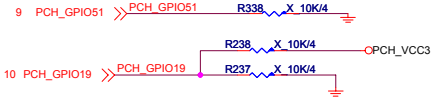
HDA_SDO

Default:

Do not pull high.

Disable ME in Manufacturing Mode:

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.



SATA1GP/GPIO19, GPIO51

Default (SPI):

Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:

Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:

Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

GPIO37

Enable TLS:

Pull up with 1k Ohm to VccSus3.3.

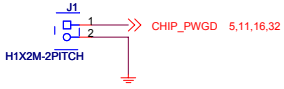
Default (Disable TLS):

Leave NC. Internal pull down.

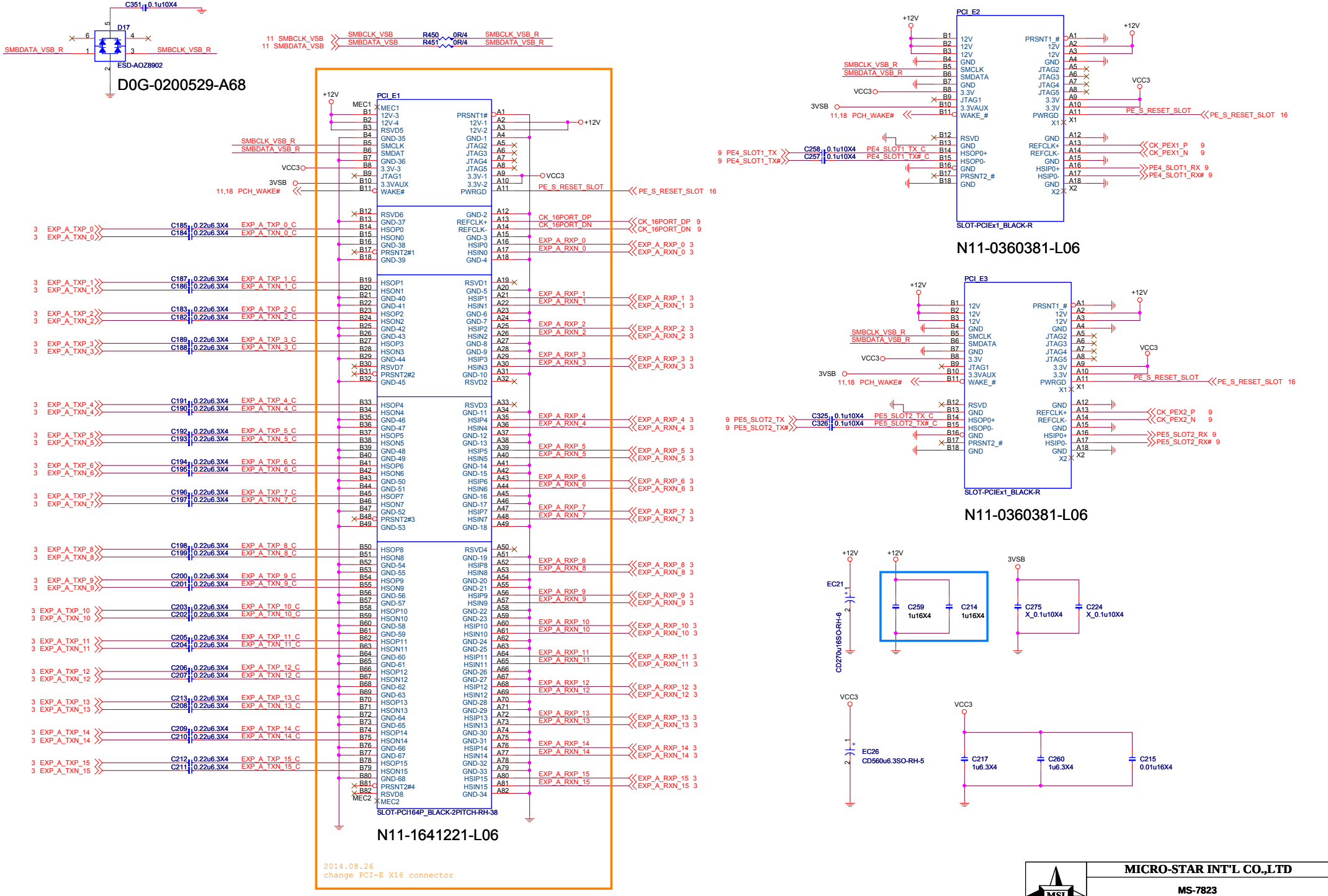
GPIO53

Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.

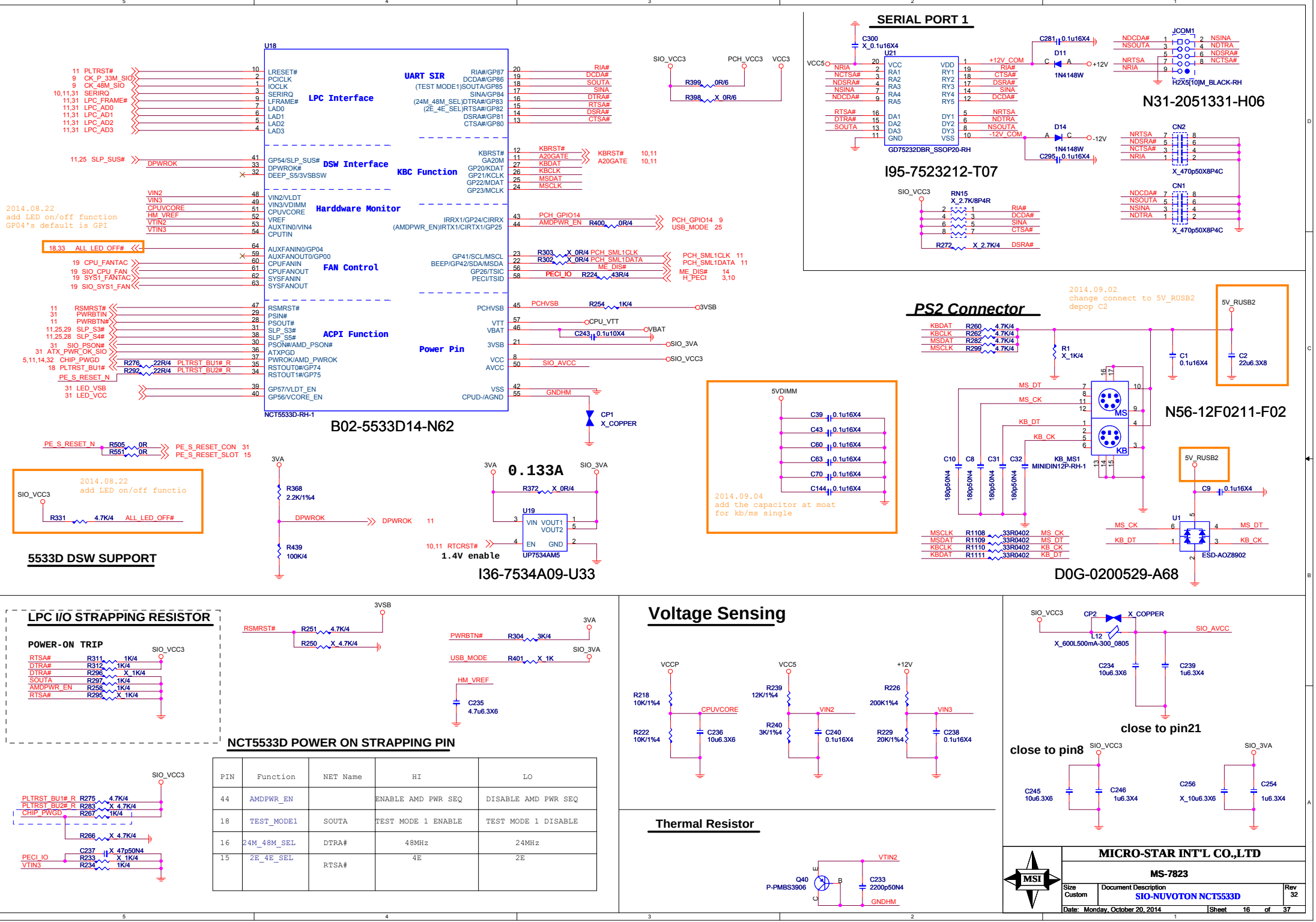
For test cpu voltage



MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: LYNX STRAPS	Rev: 32
Date: Monday, October 20, 2014	Sheet 14 of 37	

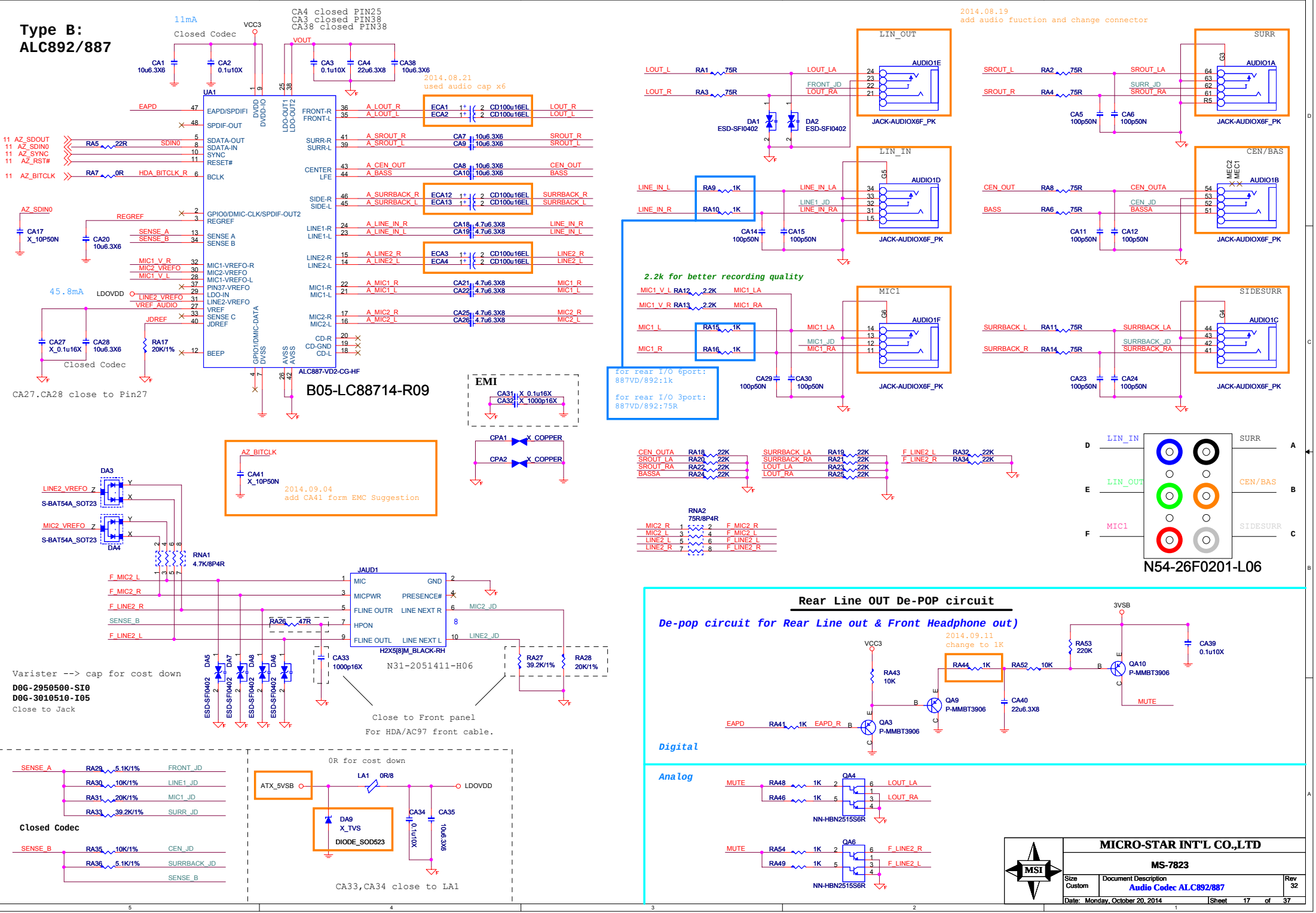


MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: PCIE(X1) & PCIE(X16) Slots	Rev: 32
Date: Monday, October 20, 2014	Sheet 15 of 37	



PIN	Function	NET Name	HI	LO
44	AMDPWR_EN		ENABLE AMD PWR SEQ	DISABLE AMD PWR SEQ
18	TEST_MODE1	SOUTA	TEST MODE 1 ENABLE	TEST MODE 1 DISABLE
16	24M_48M_SEL	DTRA#	48MHz	24MHz
15	2E_4E_SEL	RTSA#	4E	2E

Type B: ALC892/887



MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: Audio Codec ALC892/887
Rev: 32	
Date: Monday, October 20, 2014	Sheet 17 of 37

E2205-B Giga LAN

2014.08.19
change to use E2205-B

LED0:
1=hi core voltage(overclocking)
0=low core voltage (non-overclocking)

LED1:
1=SWR mode
0=LDO mode

LED3:
1=25MHz clock
0=48MHz clock

Pull-up resister RL1 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

Reserve for strap hi

2014.04.02
Suggest pull-up to VDD_IO,
if pull-up to other power soruce might cause leakage issue

CHOKEL1:
L04-47A7310-C08
L04-47A7680-T15

LL1:
L02-3018023-C08
L02-3018023-T19

D0G-1020510-I05
D0G-8010510-SI0

D0G-05A0300-I14
D0G-06A050C-A68

Close to Pin52 (<200mil)
Close to Pin24 (<200mil)
near Pin52 (<400mil)
Close to Pin9
Close to Pin21
Close to Pin44
Close to Pin25
Close to Pin47
Close to CHOKEL1 (<200mil)
Close to Pin32
Close to Pin18
Close to Pin12

VDD33 power trace should be wider than 30mils;
AVDD33 power trace should be wider than 30mils;
VDD_IO power trace should be wider than 30mils;
VDDIO_REG power trace should be wider than 20mils;
AVDDH power trace should be wider than 20mils;
AVDDL power traces should be wider than 20mils.
DVDDL power traces should be wider than 20mils.

9 GND Vias

2014.08.19
change LAN_USB connector

RJ45_USBX2_LEDX2_TX-1000-RH-43

N58-22F1891-U30

LED1 low is Orange 1000
LED2 low is Green 100

2014.09.04
EMC Suggestion

HS_LAN1
E21-7823050-RH
Audio Cover

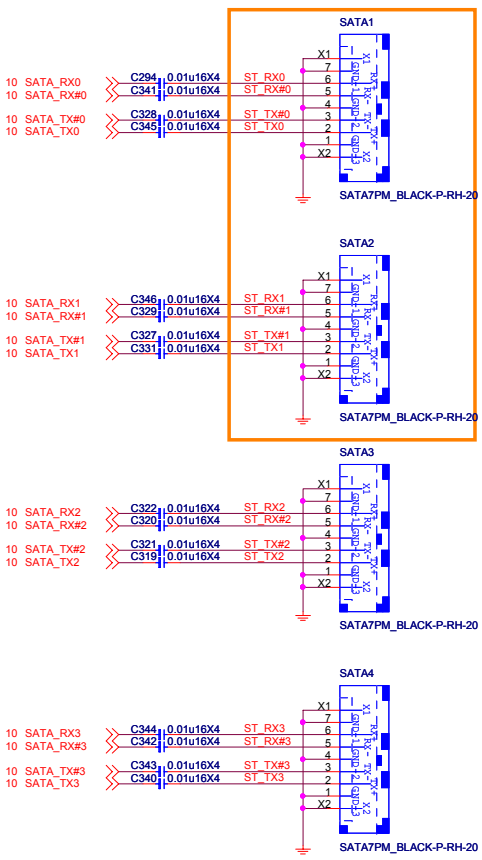
2014.08.19
add LAN cover and LED
These LED must be cloes to LAN cover
2014.09.03
LAN cover change to E23-7920010-RH
LEDA7,LEDA8, QL1, RL21, RL22 in top

10:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRIO13.

MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: LAN-Atheros_E2205-B
Rev: 32	
Date: Monday, October 20, 2014	Sheet 18 of 37

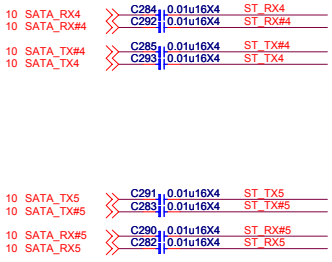
SATA CONNECTOR

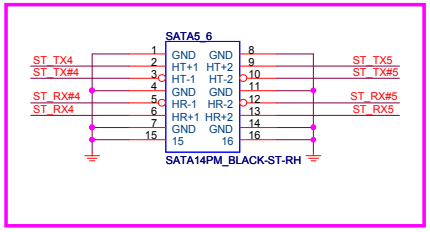
SATA 6G PORT 0,1,2,3



2014.09.01
change SATA connector

SATA 3G PORT 4,5

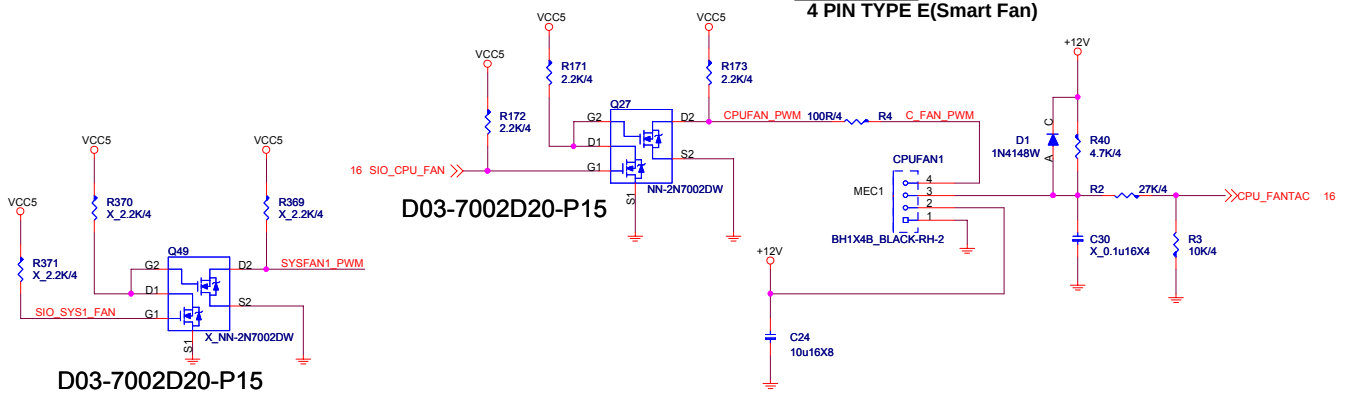




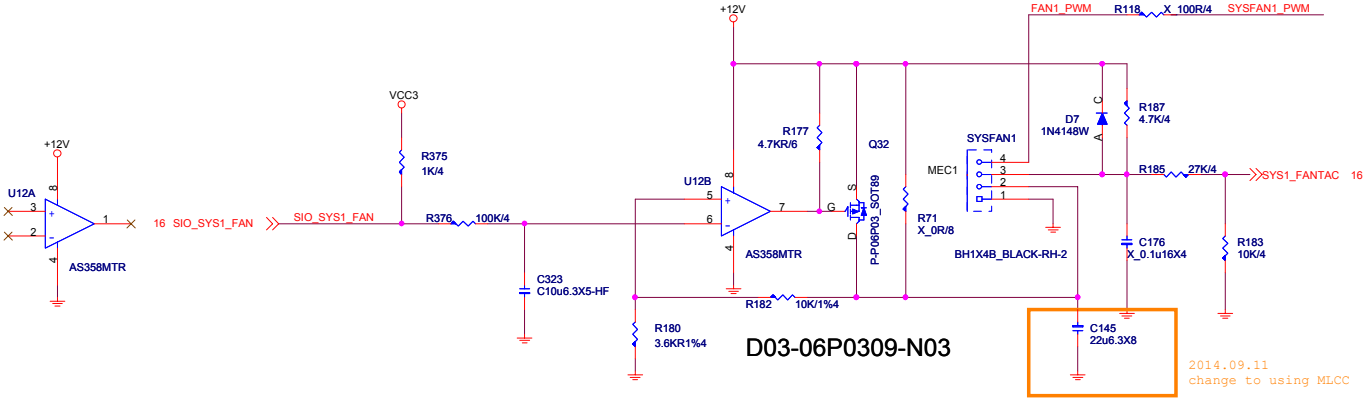
2014.09.30
change SATA 4's TX and RX single

FAN-COUNTROL CIRCUIT

CPU FAN
4 PIN TYPE E(Smart Fan)



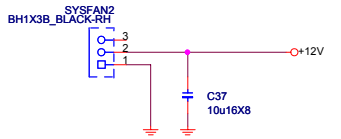
SYSTEM FAN1
4 PIN TYPE F(Smart Fan)



2014.09.11
change to using MLCC

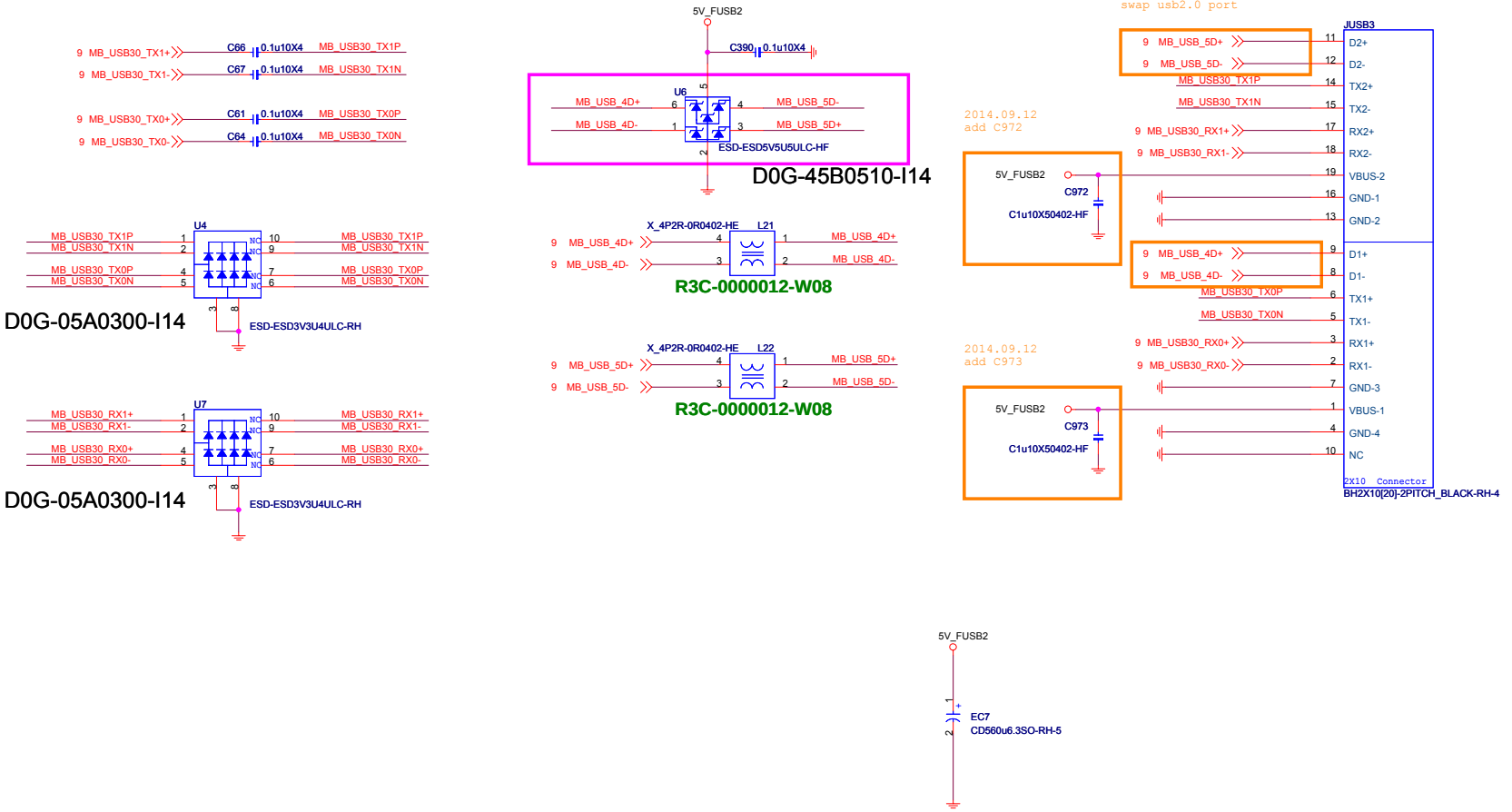
SYSTEM FAN2
3 PIN TYPE C(Full Speed)

2014.08.21
add SYSFAN2



MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: SATA/FAN
Rev: 32	
Date: Monday, October 20, 2014	Sheet 19 of 37

Front USB3.0 Connector



MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: Front USB3.0 Connector
Rev: 32	
Date: Monday, October 20, 2014	Sheet 20 of 37

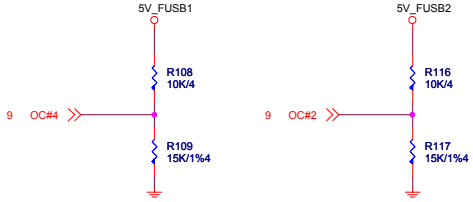
PCH/FCH side: OC# pull high to +3VSB

Near Front ==>

D08-0300700-P16

D08-0300700-P16

over current protect



D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

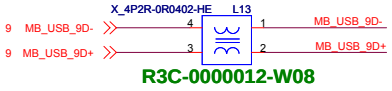
FRONT USB PORT 8,9

R3C-0000012-W08

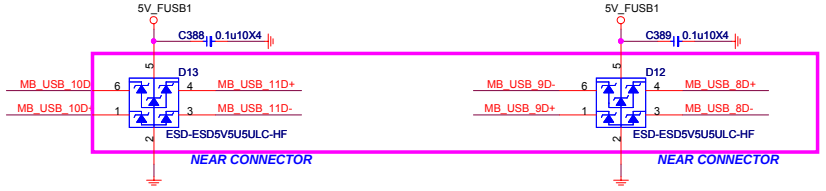
R3C-0000012-W08

FRONT USB PORT 10.11

R3C-0000012-W08



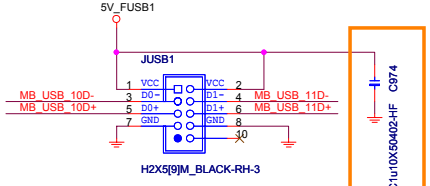
R3C-0000012-W08



D0G-45B0510-I14

D0G-45B0510-I14

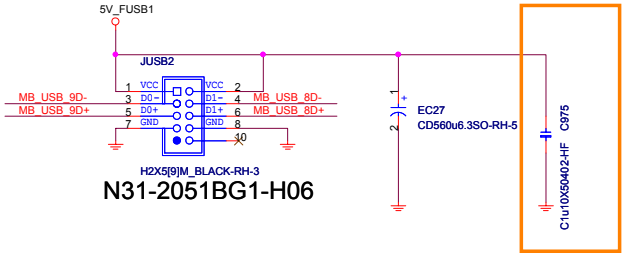
2014.10.02
change D12, D13 to D0G-45B0510-I14



N31-2051BG1-H06

2014.09.12
add C974

2014.09.12
add C975

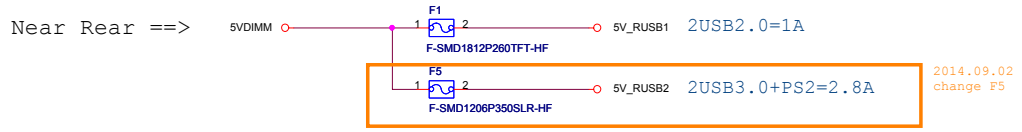


N31-2051BG1-H06

MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: Front USB2.0 Connector	Rev: 32
Date: Monday, October 20, 2014	Sheet 21 of 37	

PCH/FCH side: OC# pull high to +3VSB

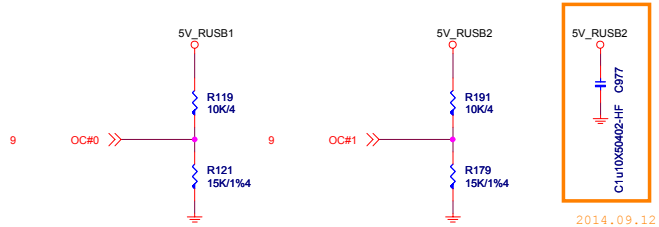
Near Rear ==>



2014.09.02
change F5

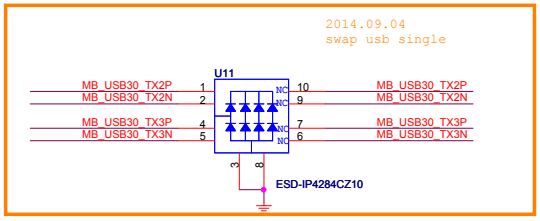
D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

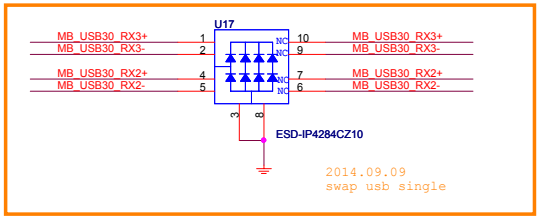
over current protect

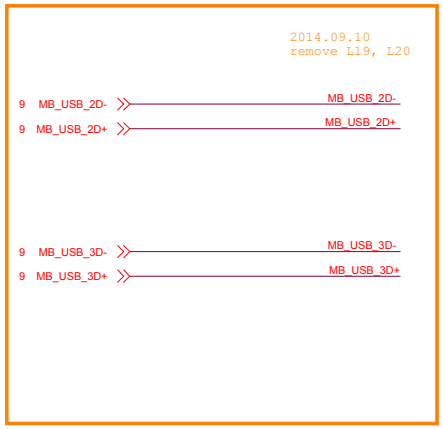


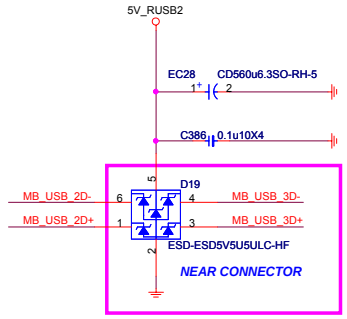
2014.09.12
add C977

REAR USB3.0 PORT



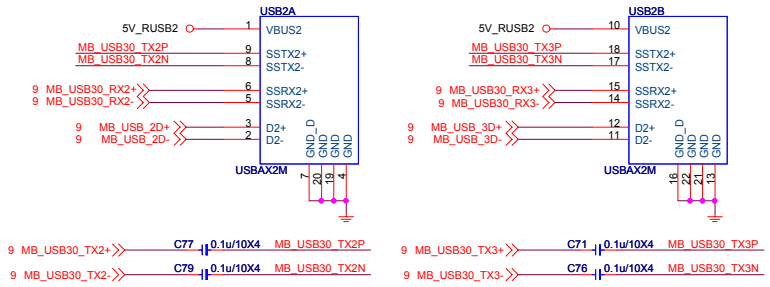






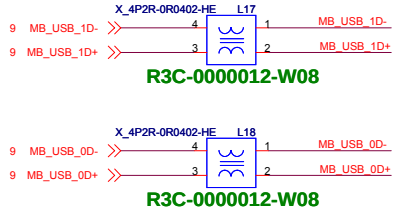
D0G-45B0510-I14

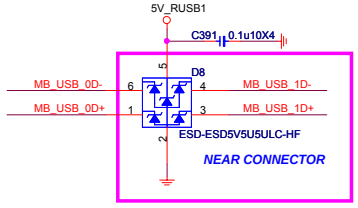
N53-18M0091-F02



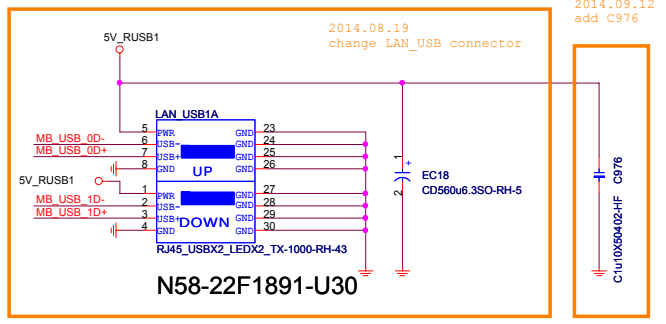
2014.10.02
change D19, D8 to D0G-45B0510-I14

REAR USB2.0 PORT 4.5





D0G-45B0510-I14



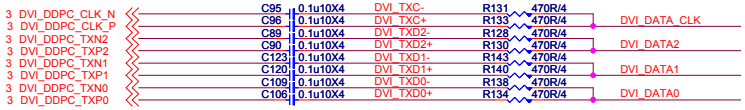
2014.09.12
add C976

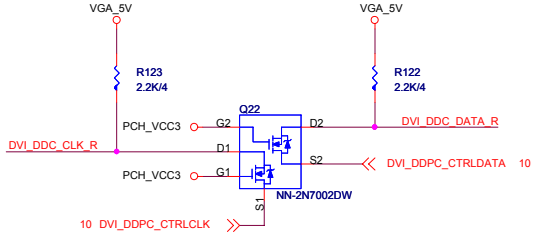
N58-22F1891-U30

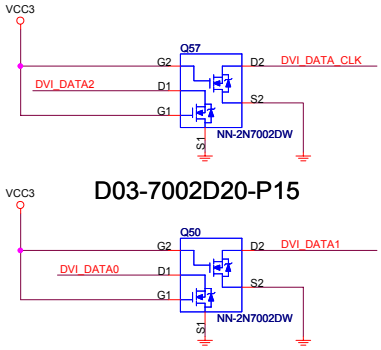
MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: Rear USB2.0 / 3.0 Connector	Rev: 32
Date: Monday, October 20, 2014	Sheet 22 of 37	

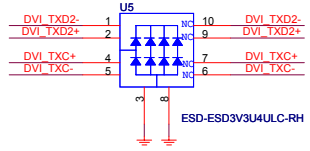
DVI

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

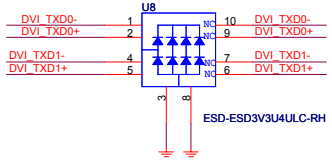




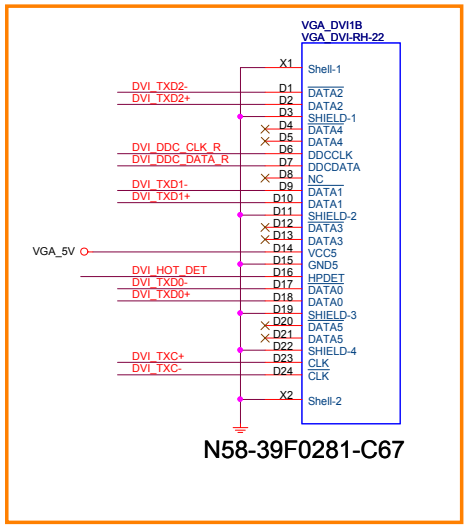




D0G-05A0300-I14

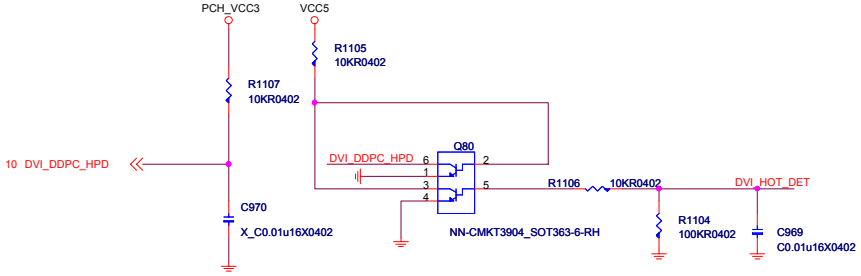


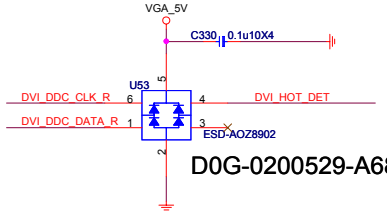
2014.08.19
change DVI_VGA connector



N58-39F0281-C67

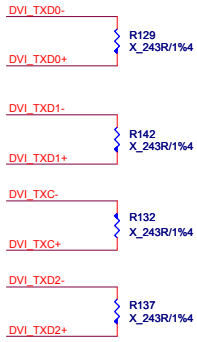
HPD

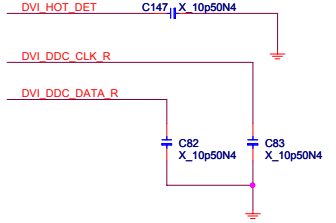




D0G-0200529-A68

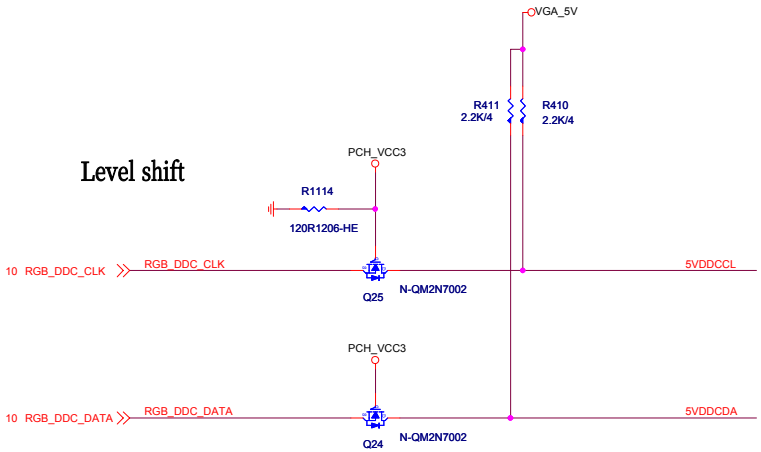
For EMI

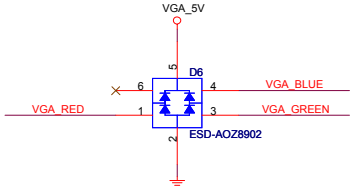


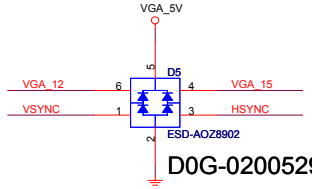


MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: DVI Connector	Rev: 32
Date: Monday, October 20, 2014	Sheet 23 of 37	

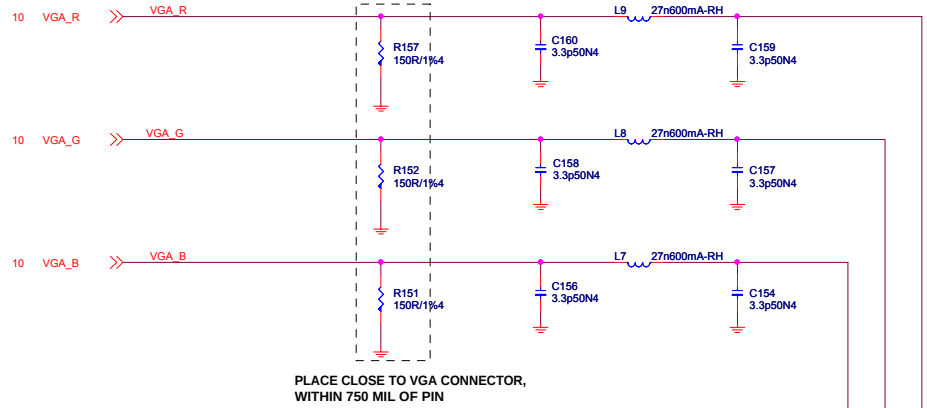
D-Sub



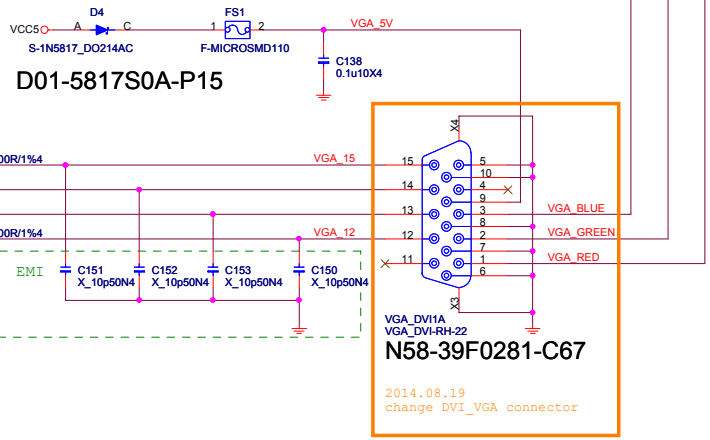




D0G-0200529-A68

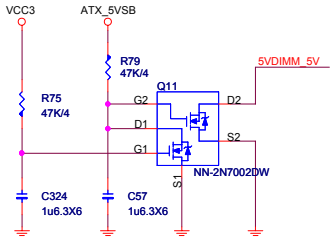


D08-0100200-B07



MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: VGA Connector	Rev: 32
Date: Monday, October 20, 2014	Sheet 24 of 37	

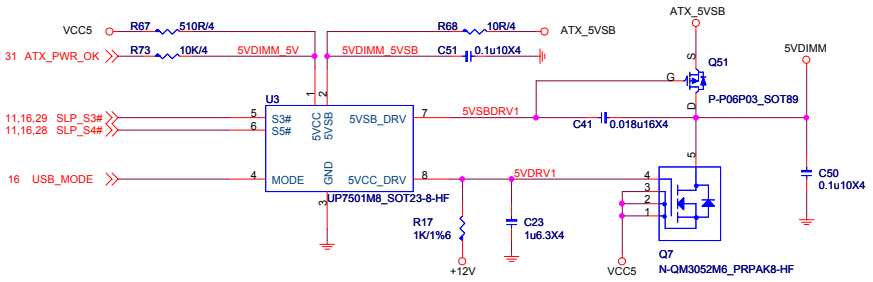
5VDIMM FOR DDR

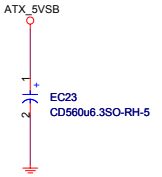


Patch coolermaster 700w power sequence

D03-7002D20-P15

D03-06P0319-N03



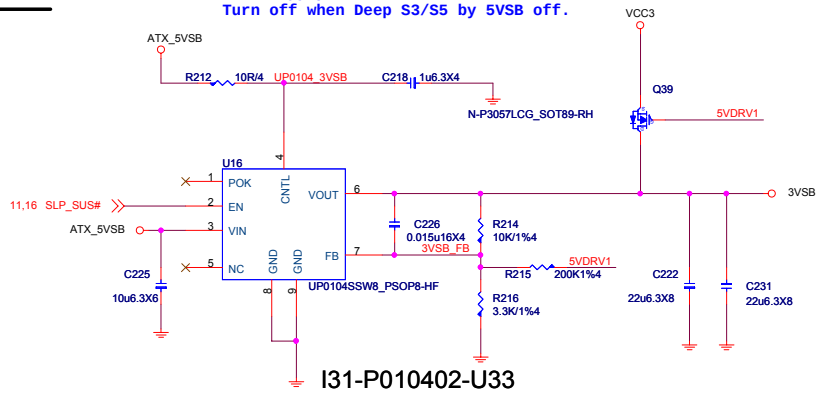


D03-3052M00-U47

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB

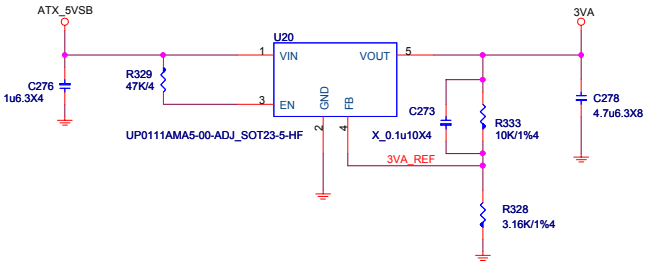
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



I31-P010402-U33

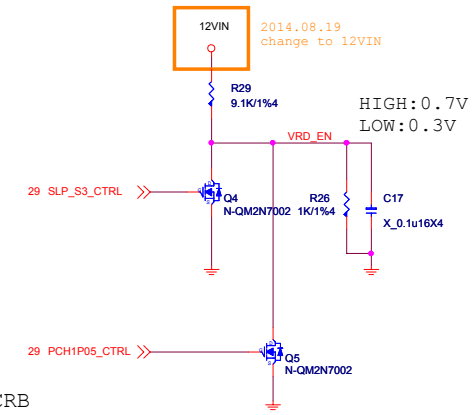
3VA

20mA

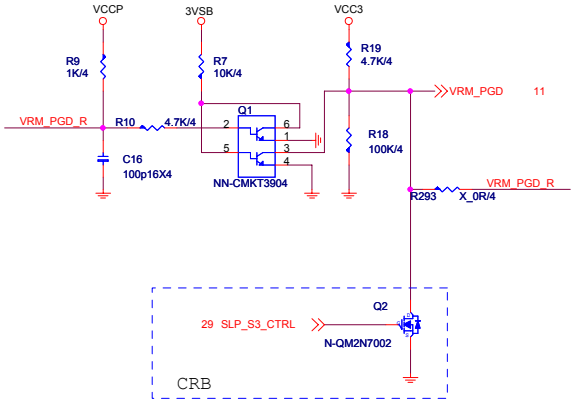


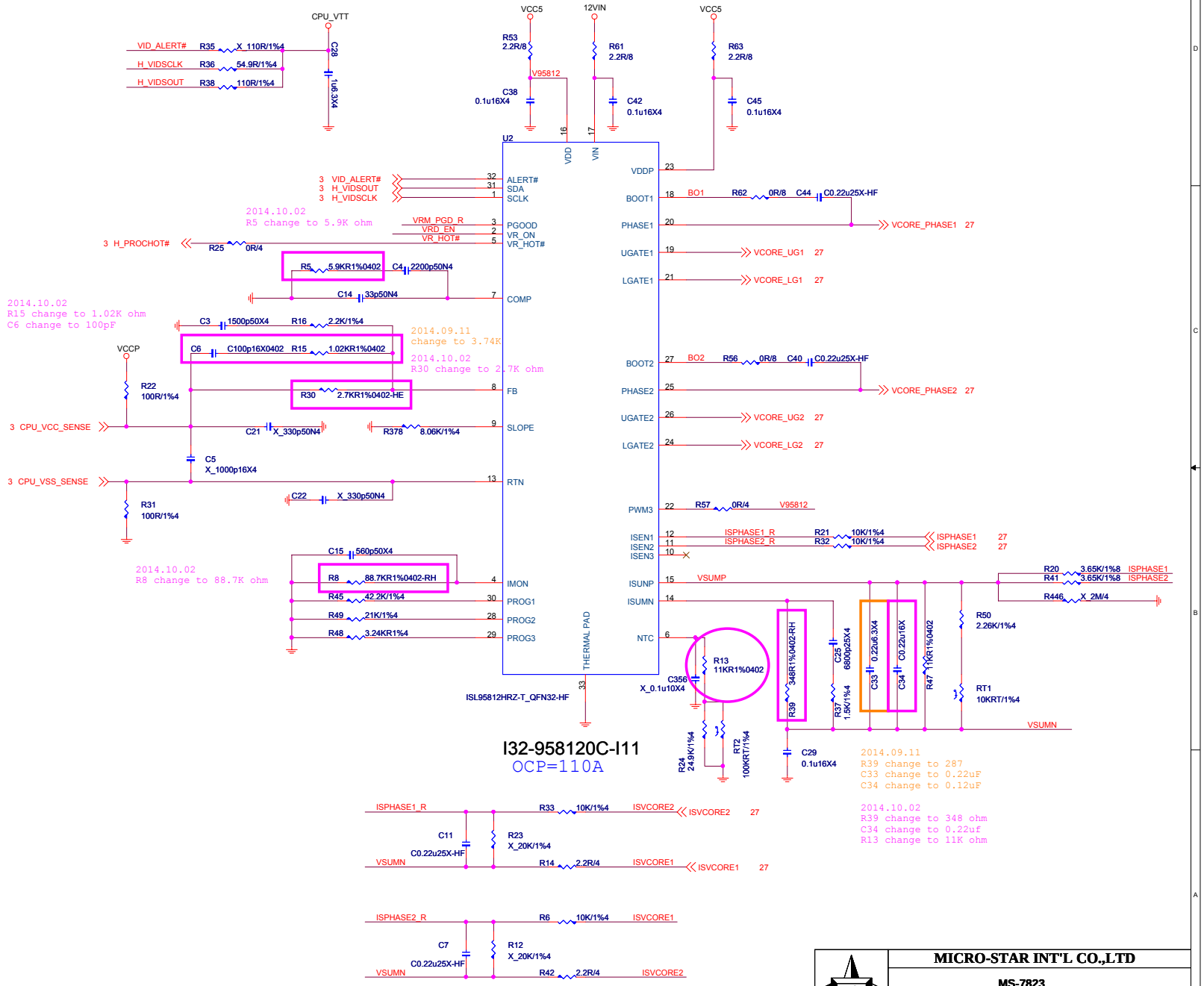
MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: ACPI controller UPI	Rev: 32
Date: Monday, October 20, 2014	Sheet 25 of 37	

VCORE power on by s3 and 12v



VRMPWRGD LEVEL SHIFT





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7823	
Size: Custom	Document Description: CPU Power - ISL95812	Rev: 32
Date: Monday, October 20, 2014	Sheet 26 of 37	

VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm

2014.08.19
delete JPWR2 in-put choke "L04-47B9041-T15"

JPWR2
PWRCONN2P_BLACK-RH-3
N93-04M0441-H06

12VIN
EC2 CD270u16SO-RH-6
EC4 CD270u16SO-RH-6
EC8 CD270u16SO-RH-6

D03-3052M00-U47
D03-3056M00-U47

26 VCORE_UG1
R66 1R/1%6
VCORE_UG1_R
R69 10K/1%4
Q6 N-QM3052M6_PRPAK8-HF
Q52 N-QM3052M6_PRPAK8-HF
C75 X_1u16X6
C13 10u16X8
C72 10u16X8
26 VCORE_PHASE1
26 VCORE_LG1
Q10 N-QM3056M6_PRPAK8-HF
Q13 N-QM3056M6_PRPAK8-HF
R78 2.2R/8
C56 3300p50X4

L04-47B9041-T15
CHOKE6 CH-0.47u60A0.98m-HF
CHOKE2 CH-0.47u60A0.98m-HF
2014.08.19
add VCCP out-put choke
CP3 X_COPPER
CP4 X_COPPER
26 ISPHASE1
26 ISVCORE1
VCCP
EC12 CD560u6.3SO-RH-5
EC13 CD560u6.3SO-RH-5
EC19 CD560u6.3SO-RH-5
EC33 CD560u6.3SO-RH-5

12VIN
D03-3052M00-U47
D03-3056M00-U47

26 VCORE_UG2
R126 1R/1%6
VCORE_UG2_R
R124 10K/1%4
Q19 N-QM3052M6_PRPAK8-HF
Q53 N-QM3052M6_PRPAK8-HF
C20 X_1u16X6
C81 10u16X8
C134 10u16X8
2014.08.19
add C134
26 VCORE_PHASE2
26 VCORE_LG2
Q23 N-QM3056M6_PRPAK8-HF
Q20 N-QM3056M6_PRPAK8-HF
R127 2.2R/8
C87 3300p50X4

L04-47B9041-T15
CHOKE5 CH-0.47u60A0.98m-HF
CHOKE4 CH-0.47u60A0.98m-HF
CP5 X_COPPER
CP6 X_COPPER
26 ISPHASE2
26 ISVCORE2

12VIN
C58 X_10u16X8
C73 X_10u16X8
C91 X_10u16X8

MICRO-STAR INT'L CO.,LTD
MS-7823
Size: Custom
Document Description: CPU Power - MOS
Rev: 32
Date: Monday, October 20, 2014
Sheet 27 of 37

DDR Power:1.5V

DDR3_1.5V 4.75A+12A+1.1A+6A=23.85A OCP:36A

4.75A FOR CPU

12A FOR 4DIMM

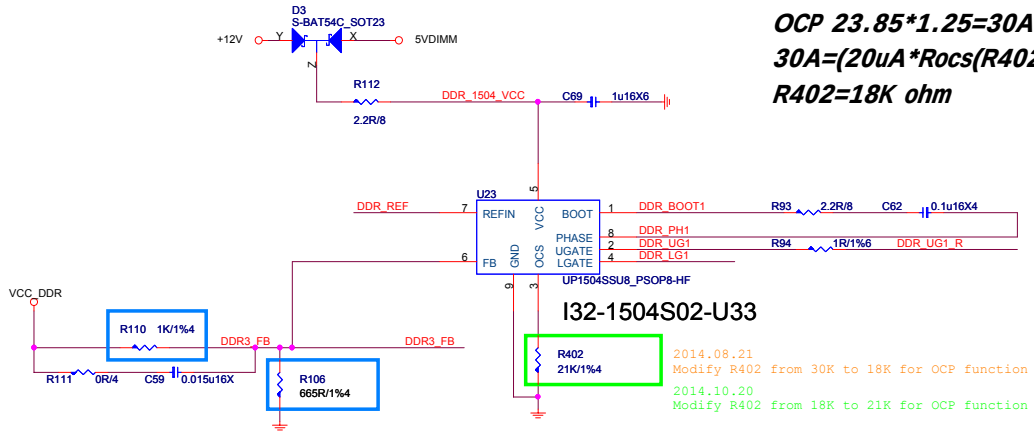
1.1A FOR DDR VTT

6A FOR PCH_Core 1.05V

OCP 23.85*1.25=30A

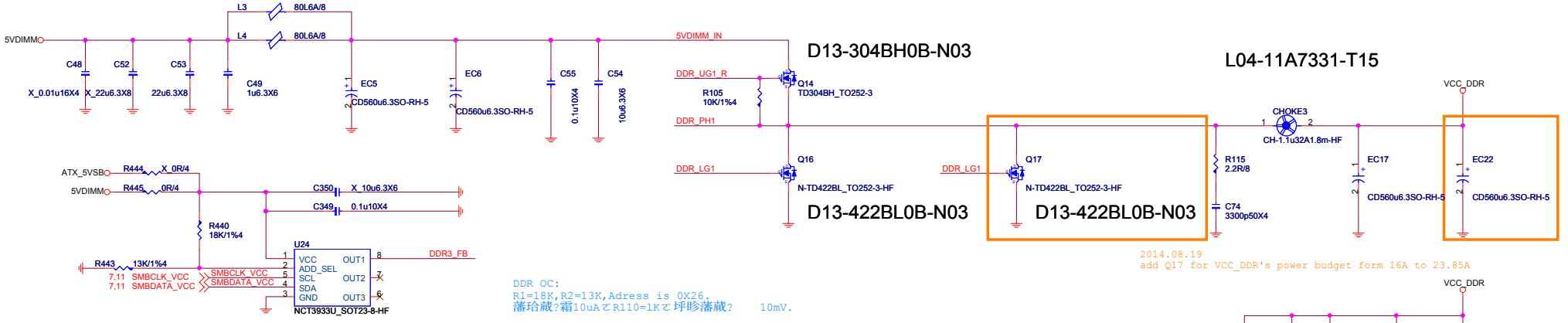
30A=(20uA*Rocs(R402)/(4*Rdson(Low side 3mohm))

R402=18K ohm



I32-1504S02-U33

L02-8008074-M26

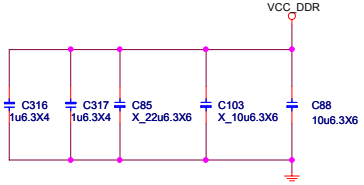


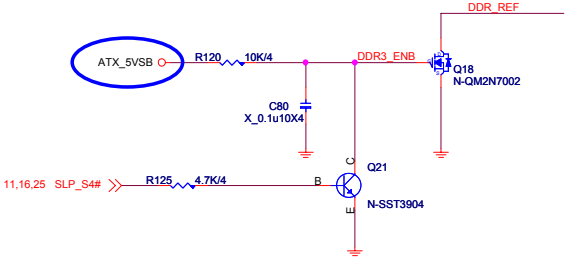
I34-3933U09-N62

DDR OC:
R1=18K,R2=13K,Adress is 0X26.
藩玲葳?霜10uAぞR110=1Kぞ坪眇藩葳? 10mV.

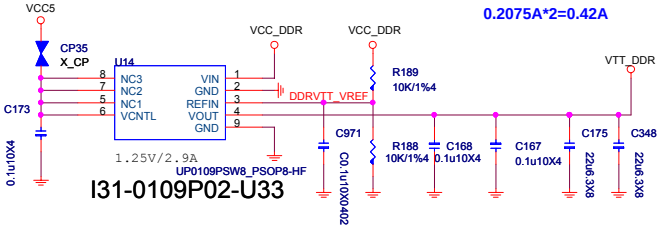
2014.08.19
add Q17 for VCC_DDR's power budget form 16A to 23.85A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





DDR VTT Power

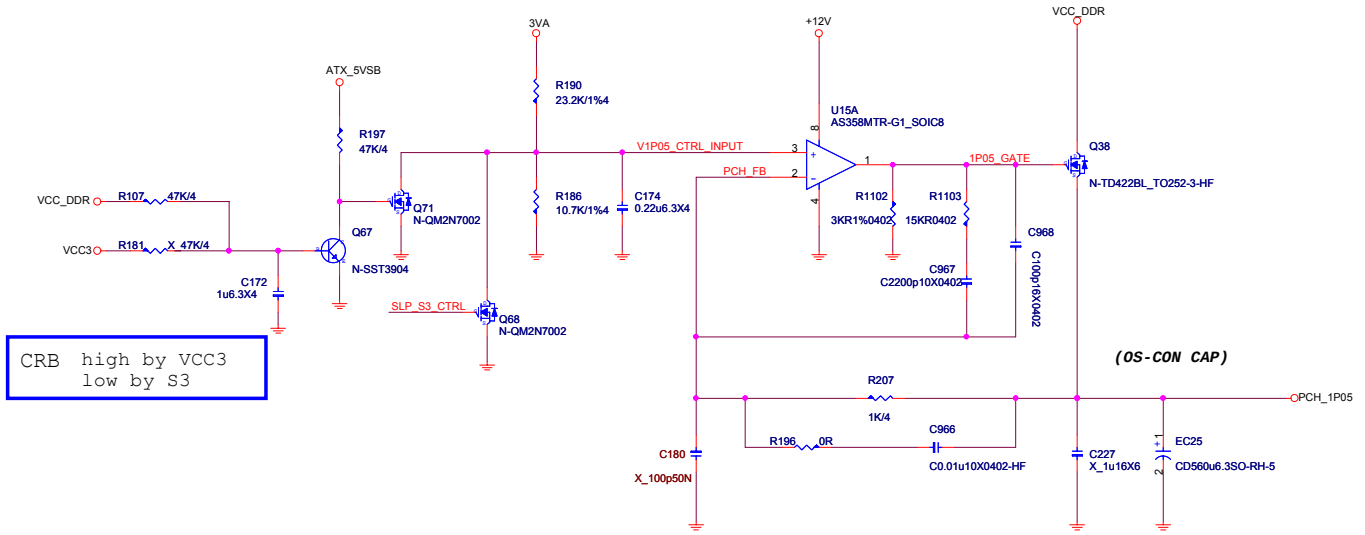


I31-0109P02-U33

P.S. Only for meet Intel power down sequence.

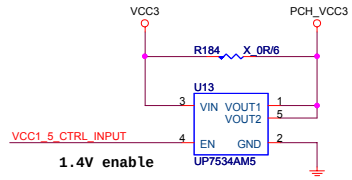
MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: DDR Power -UP1504 1-Phase	Rev: 32
Date: Monday, October 20, 2014	Sheet 28 of 37	

PCH Power:1.05V 5.747A



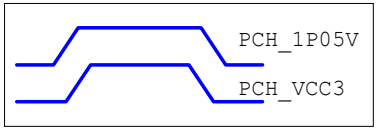
CRB high by VCC3
low by S3

0.133A

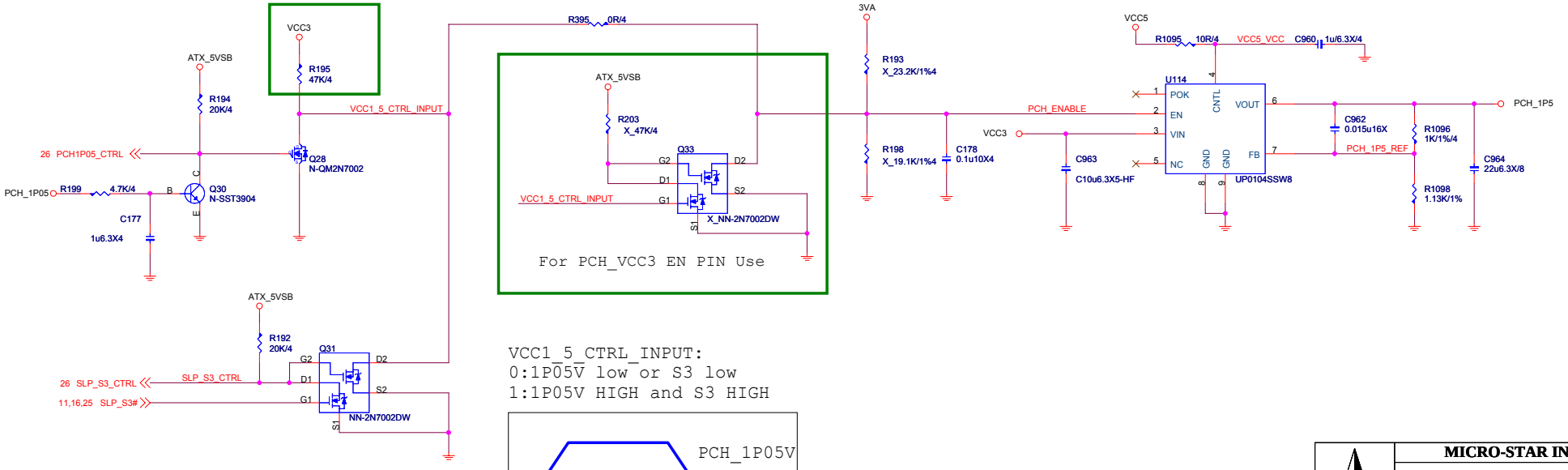


1.4V enable

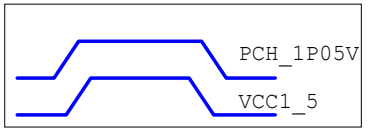
I36-7534A09-U33



PCH Power:1.5V 0.183A



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



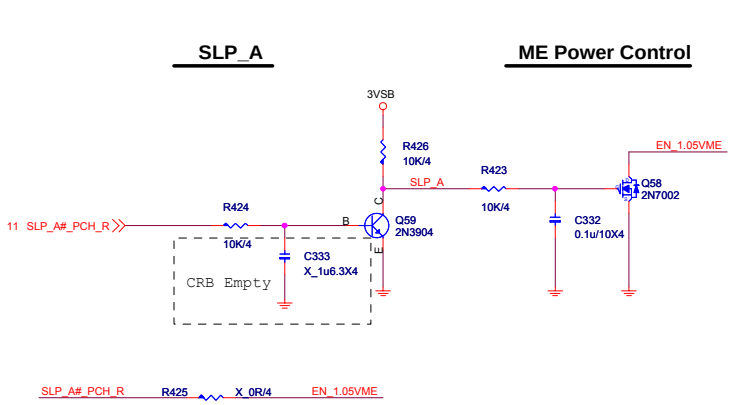
MICRO-STAR INT'L CO.,LTD

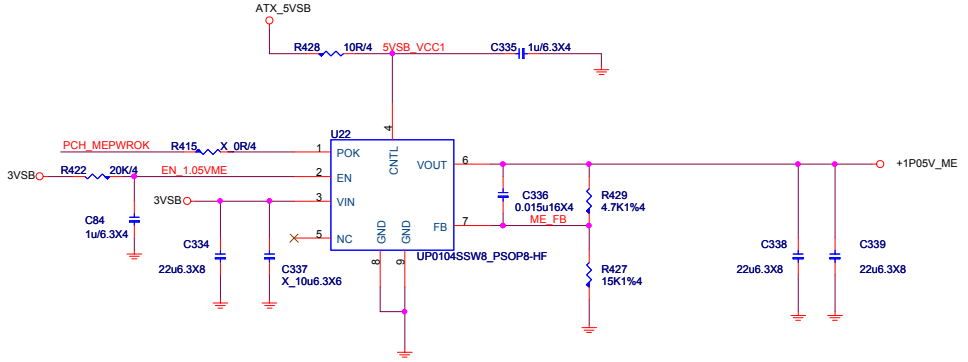
MS-7823

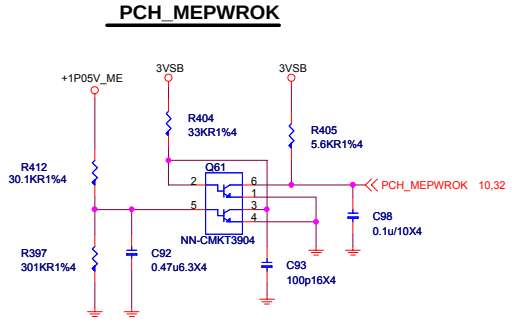
Size	Document Description	Rev
Custom	PCH Power - OP+MOS	32

Date: Monday, October 20, 2014 Sheet 29 of 37

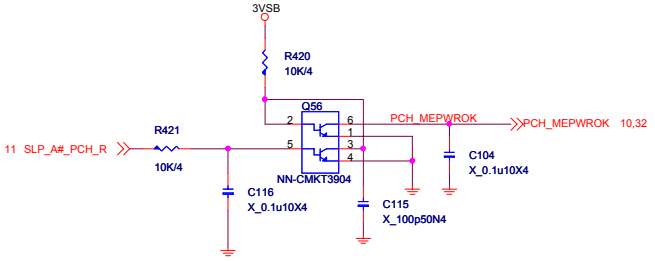
PCH ME Power:1.05V 0.670A



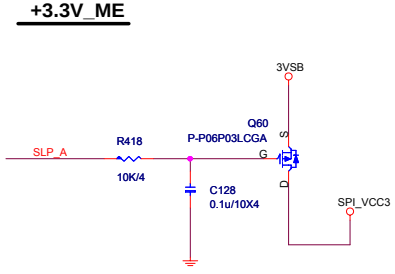




VccASW active to APWROK high 1ms

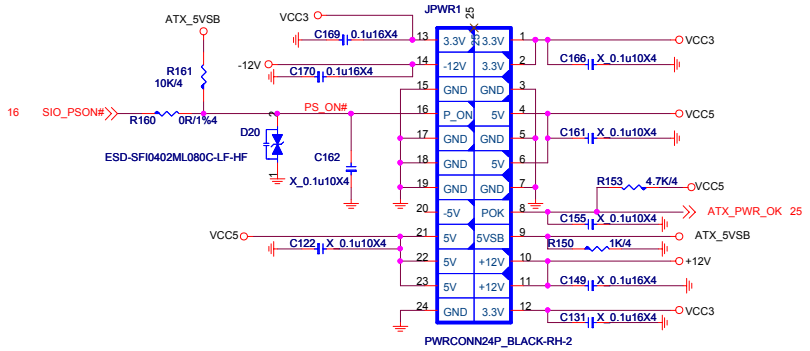


APWROK falling to VccASW falling 40ns

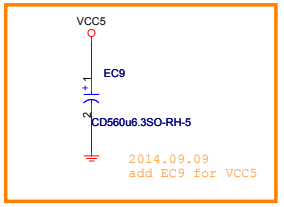


MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: PCH Power - ME POWER	Rev: 32
Date: Monday, October 20, 2014	Sheet 30 of 37	

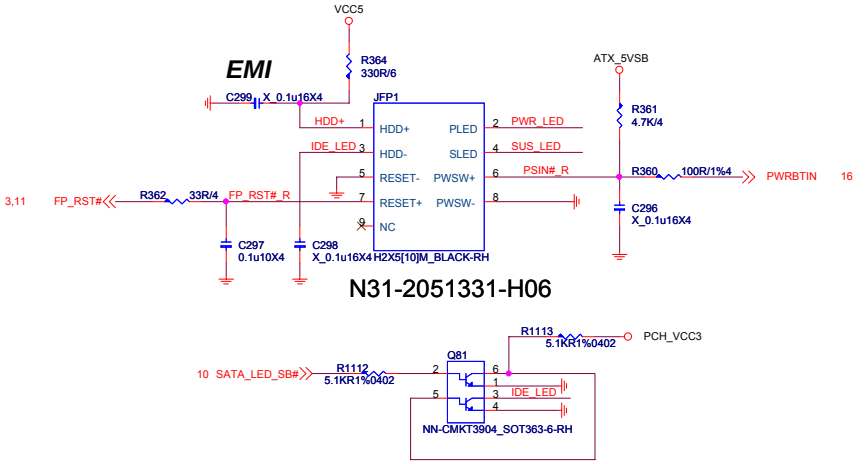
ATX POWER CONNECTOR



N93-24M0191-H06

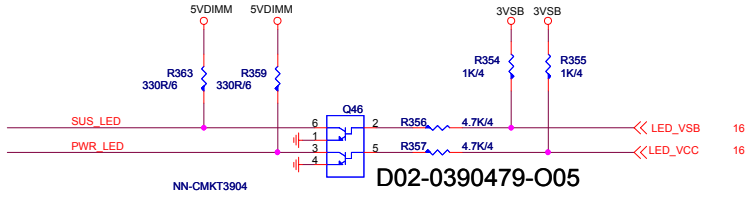


FRONT PANNEL



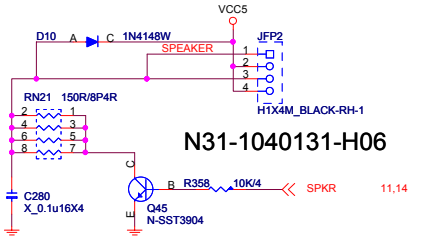
N31-2051331-H06

LED (for NV5533)



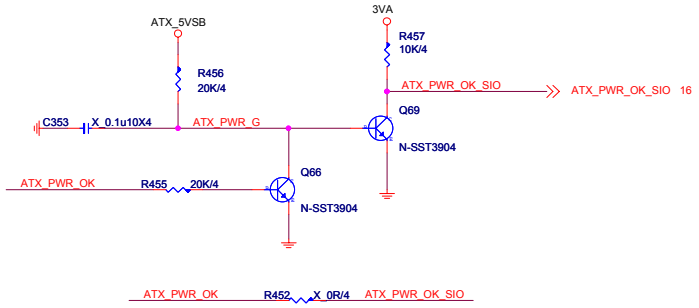
D02-0390479-O05

Speaker Pin Header

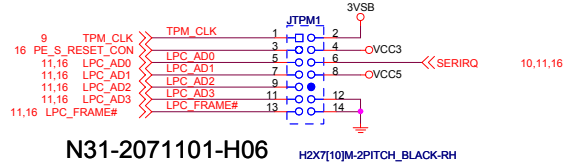


N31-1040131-H06

5VCC leakage from ATXPGD.(NCT6779 PIN80)
(NCT5533 PIN36)



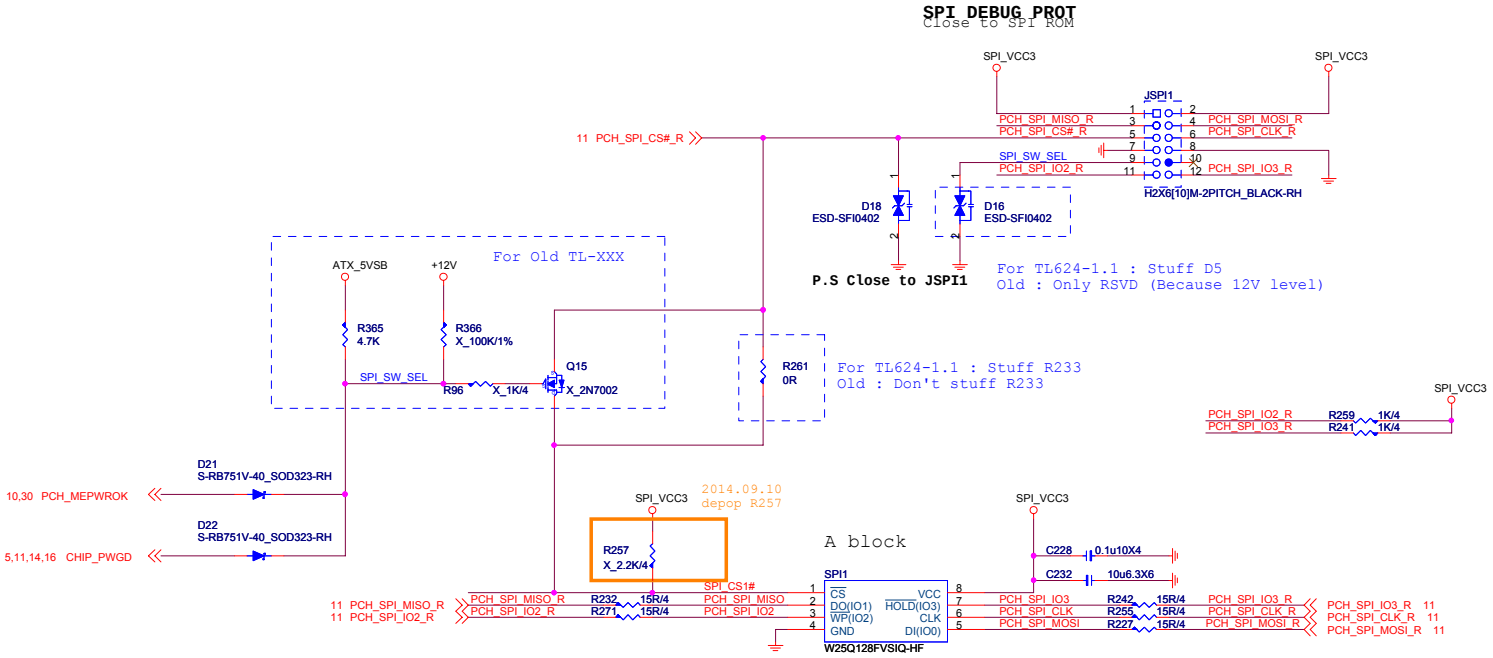
TPM/JLPC



N31-2071101-H06

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7823	
Size: Custom	Document Description: ATX F_Panel/LED/TPM	Rev: 32
Date: Monday, October 20, 2014	Sheet 31 of 37	

SPI ROM



MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: SPI ROM	Rev: 32
Date: Monday, October 20, 2014	Sheet 32 of 37	

LABEL

MARKET Name

2014.09.15
depop label

AMI
LABEL3
LABEL
LABEL

G51-M1SPXXA-A09

PCB

PCB1

7823_32

PK0-0782332-G37

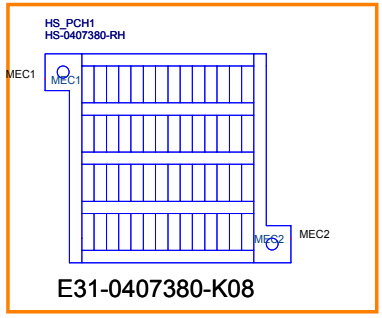
PCH Heatsink

Battery

D06-0100101-P01

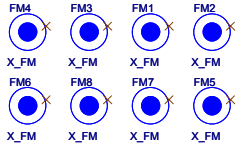
CPU Socket

E21-7788020-F02



E31-0407380-K08

Optical Fiducial Marks-120

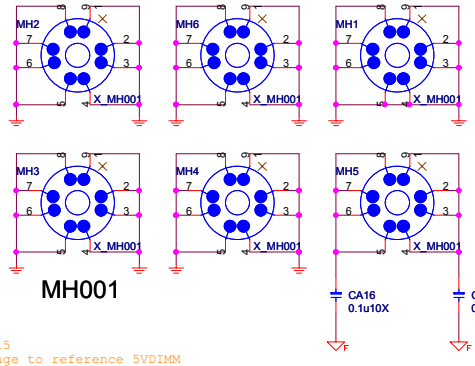


FM002

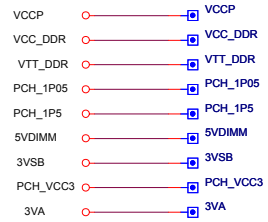
F_PAD_X

Mounting Holes

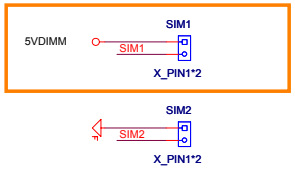
HOLES_4S



MH001



Simulation



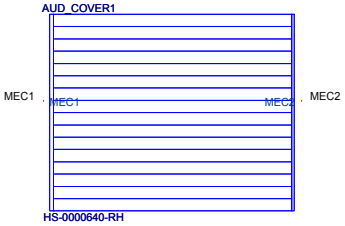
SINGLE_SIP2

2014.09.15
SIM1 change to reference 5VDIMM

2014.09.05
change PCH HEATSINK

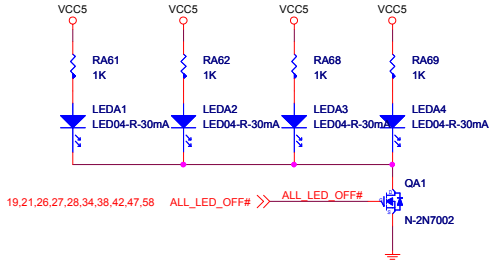
2014.08.21
add audio cover and moat LED

Audio cover

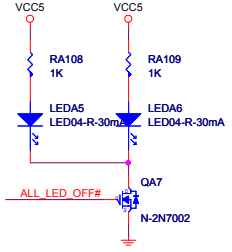


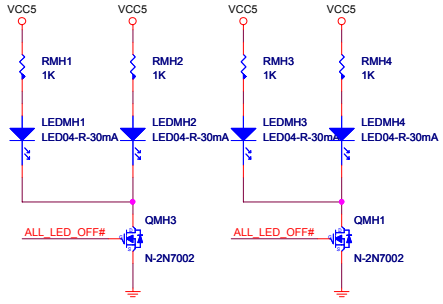
E31-0000640-K08

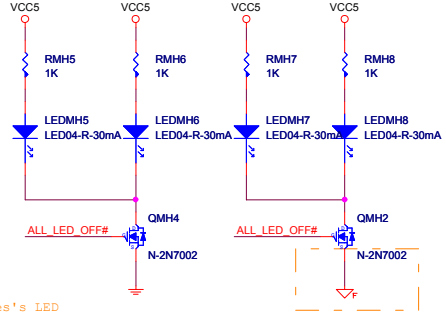
Audio moat is transparent and width 40mil



LEDA15 and LEDA16 must be hidden in the AUD_COVER1







2014.08.22
add Mounting Holes's LED
These LED must be cloes to Mounting Holes
2014.09.04
QMH2 change to AGND

MICRO-STAR INT'L CO.,LTD

MS-7823

Size	Document Description	Rev
Custom	Manual Parts	32

Date: Monday, October 20, 2014 Sheet 33 of 37