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MS-7823

mATX

Ver: 20(243.84x243.84)

Intel -SharkBay plamform Z87

CPU:

Haswell LGA1150

System Chipset:

Lynx B85 co-lay H81

Onboard Chip:

HD Audio Codec-ALC1150
LAN-E2205
(USB3.0-VL806 for H81)
SIO:Nuvoton 6779D
Flash ROM: SPI 64 MB/128MB

Main Memory:

*DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)*

ACPI:

UPI

PWM:

ISL95812 3 Phase

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 2*
*PCI Express (X4) Slot * 1*

Other:

SATA3.0 x6(PCH)
*REAL USB2.0 *4*
*FRONT USB2.0 *6*
*REAL USB3.0 *2*
*FRONT USB3.0 *2*

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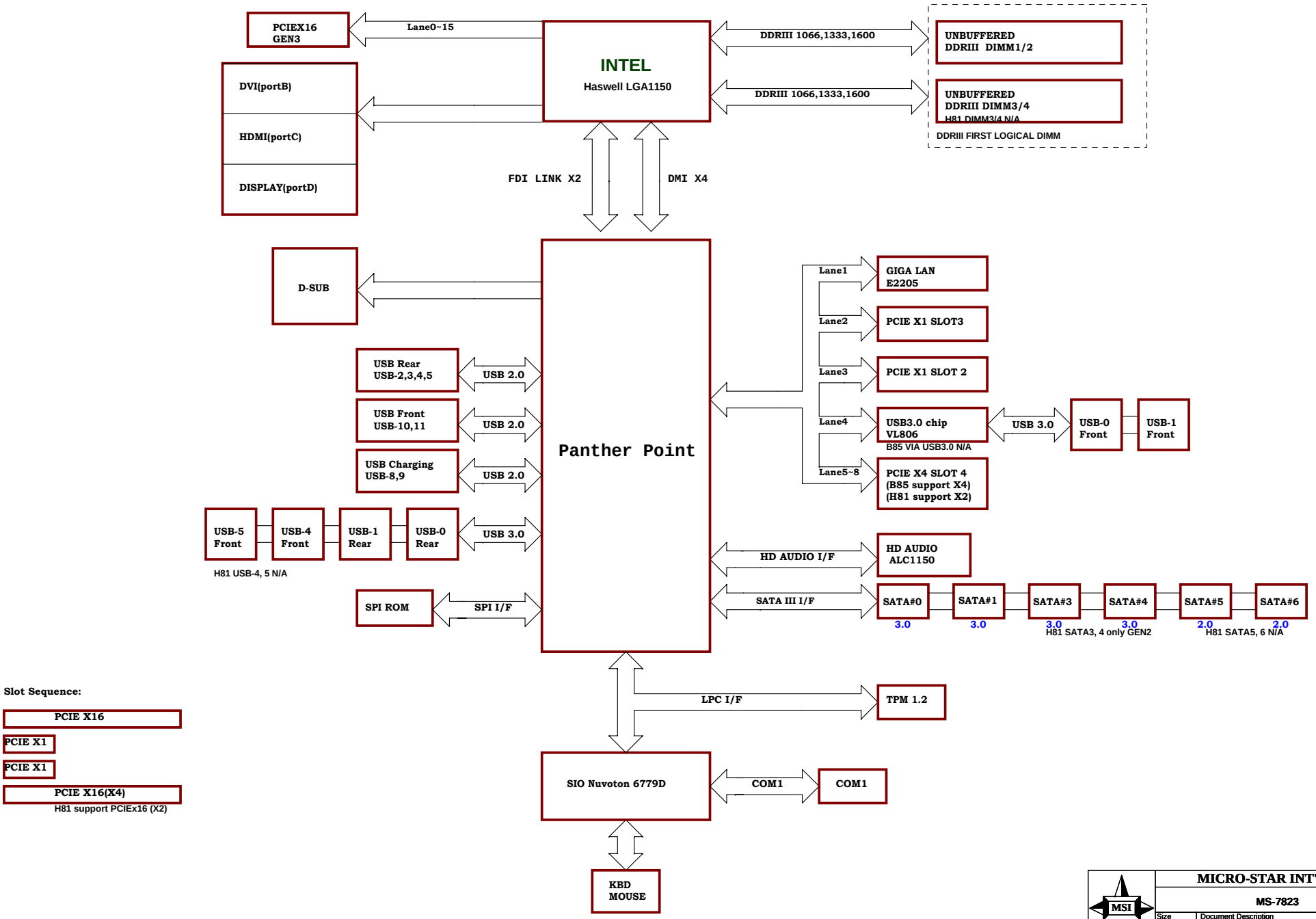
MS-7823 Block Diagram



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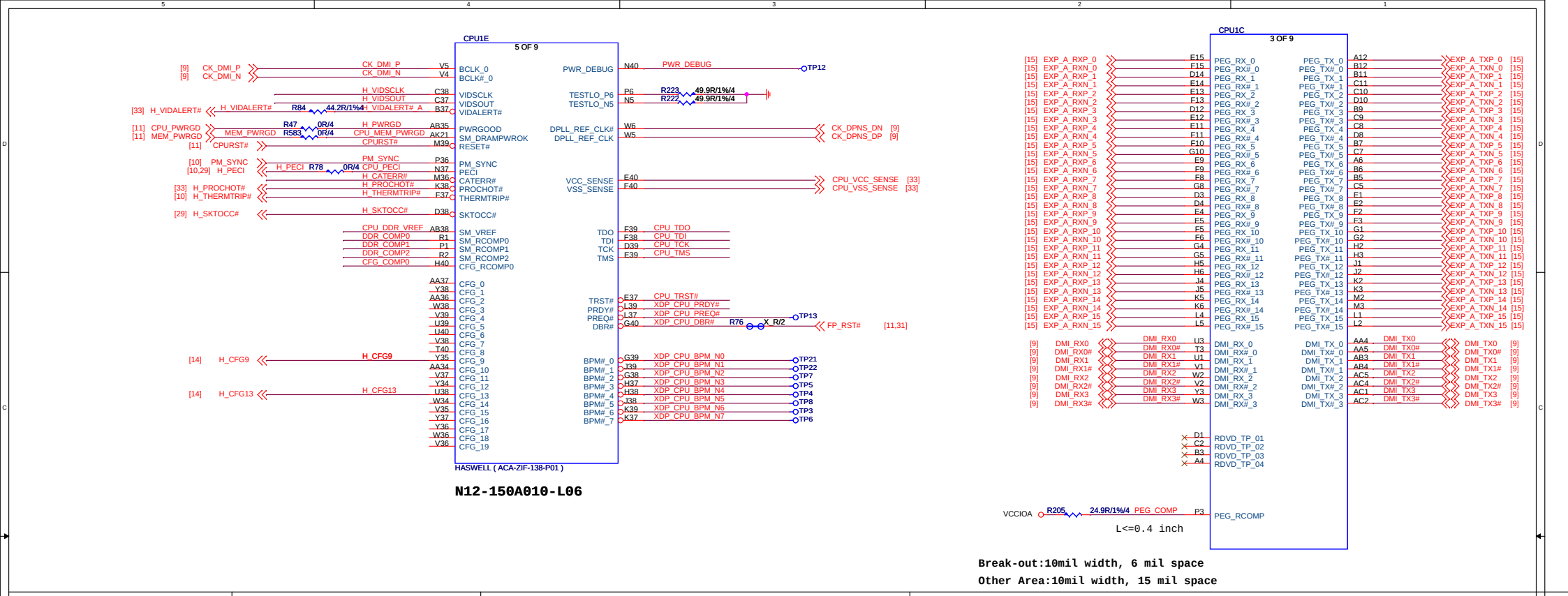
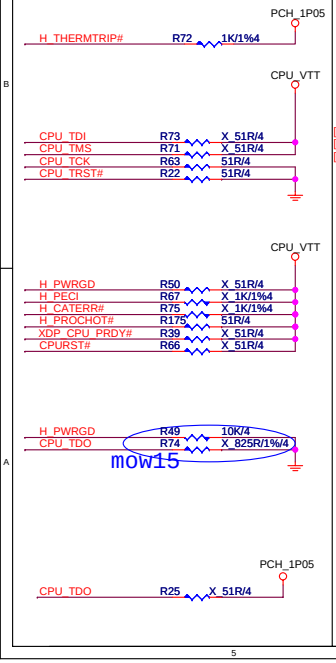
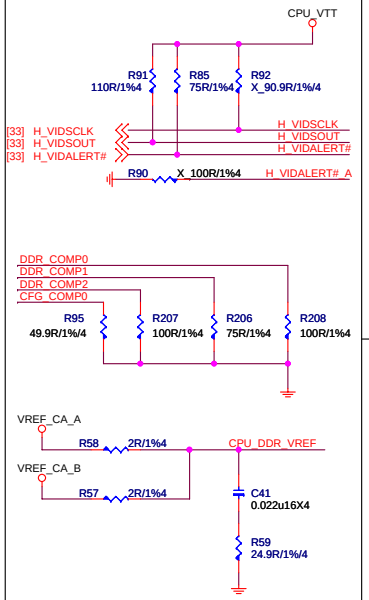
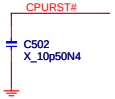


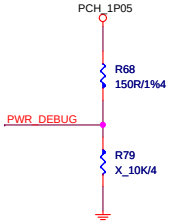


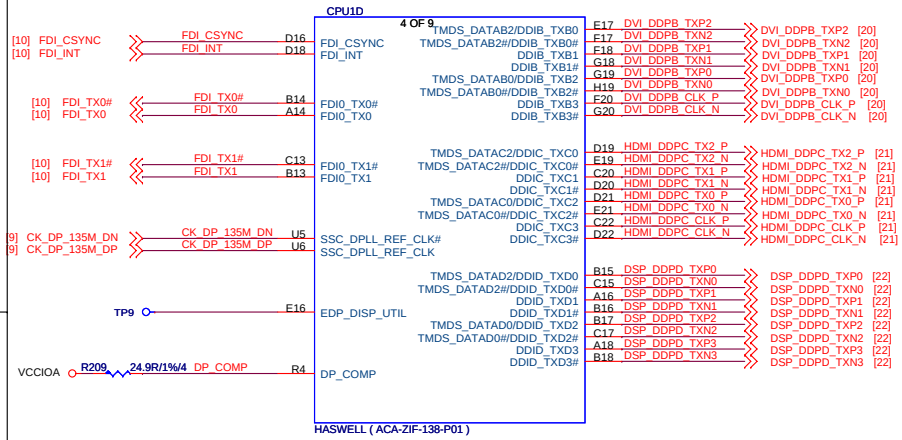


CPU_RESET#

"PDG 25.3.13PLTRST_PROC# Usage Model"
PLTRST_PROC# is a new signal which is a copy of PLTRST# signal on PCH with lower voltage. The main usage of the signal is to connect directly to RESET# signal of processor without requiring an external voltage divider.







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MS-7823	
Size: Custom	Document Description: CPU-CNTL/CLK/MISC
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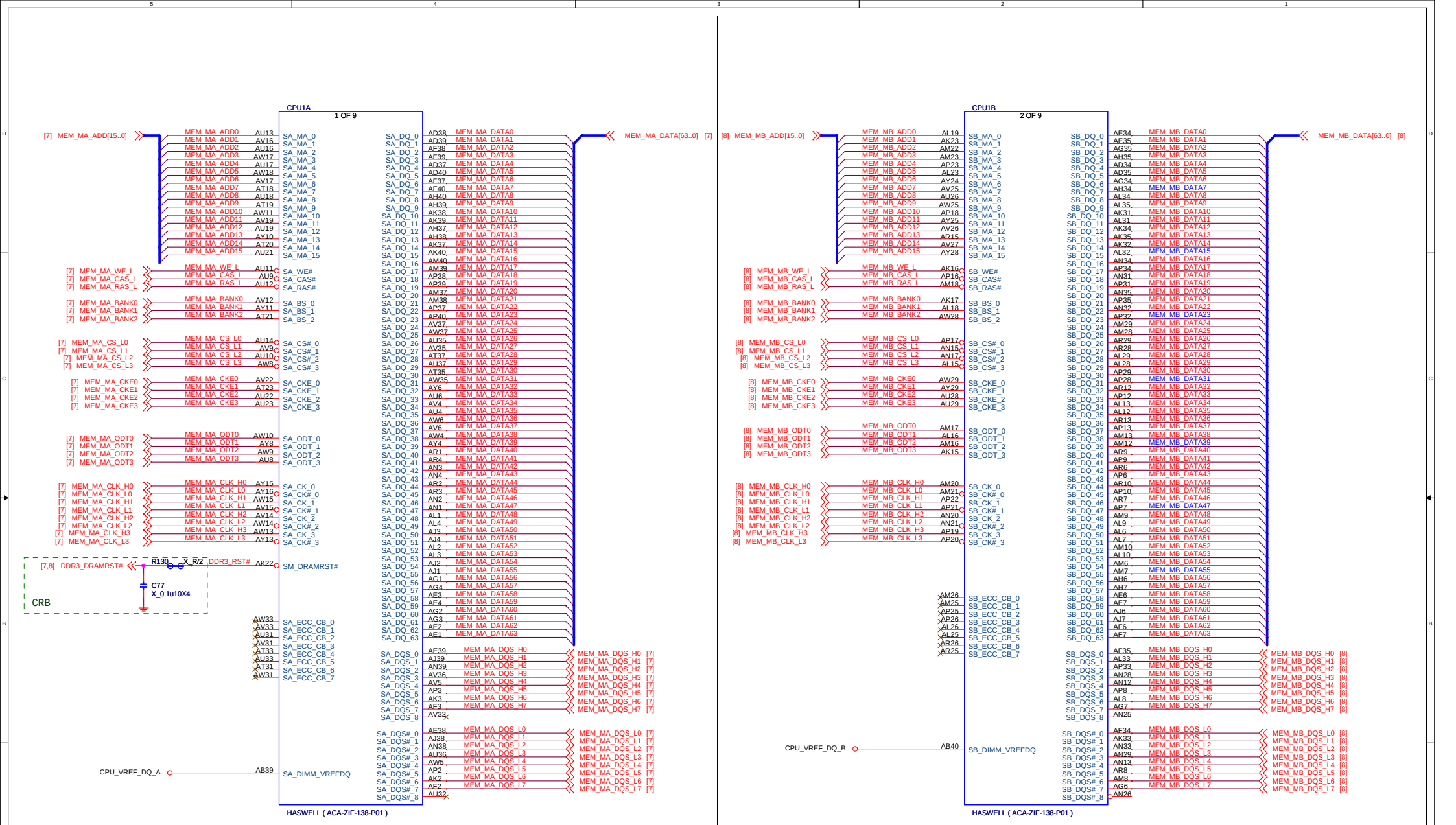
CPU1A
1 OF 9
[7] MEM_MA_ADD[15..0]
MEM_MA_ADD0 AU13 SA_MA_0
MEM_MA_ADD1 AV16 SA_MA_1
MEM_MA_ADD2 AU16 SA_MA_2
MEM_MA_ADD3 AW17 SA_MA_3
MEM_MA_ADD4 AU17 SA_MA_4
MEM_MA_ADD5 AW18 SA_MA_5
MEM_MA_ADD6 AV17 SA_MA_6
MEM_MA_ADD7 AT18 SA_MA_7
MEM_MA_ADD8 AU18 SA_MA_8
MEM_MA_ADD9 AT19 SA_MA_9
MEM_MA_ADD10 AW11 SA_MA_10
MEM_MA_ADD11 AV19 SA_MA_11
MEM_MA_ADD12 AU19 SA_MA_12
MEM_MA_ADD13 AV10 SA_MA_13
MEM_MA_ADD14 AT20 SA_MA_14
MEM_MA_ADD15 AU21 SA_MA_15
[7] MEM_MA_WE_L
[7] MEM_MA_CAS_L
[7] MEM_MA_RAS_L
MEM_MA_WE_L AU11 SA_WE#
MEM_MA_CAS_L AU9 SA_CAS#
MEM_MA_RAS_L AU12 SA_RAS#
[7] MEM_MA_BANK0
[7] MEM_MA_BANK1
[7] MEM_MA_BANK2
MEM_MA_BANK0 AV12 SA_BS_0
MEM_MA_BANK1 AV11 SA_BS_1
MEM_MA_BANK2 AT21 SA_BS_2
[7] MEM_MA_CS_L0
[7] MEM_MA_CS_L1
[7] MEM_MA_CS_L2
[7] MEM_MA_CS_L3
MEM_MA_CS_L0 AU14 SA_CS#_0
MEM_MA_CS_L1 AV9 SA_CS#_1
MEM_MA_CS_L2 AU10 SA_CS#_2
MEM_MA_CS_L3 AW8 SA_CS#_3
[7] MEM_MA_CKE0
[7] MEM_MA_CKE1
[7] MEM_MA_CKE2
[7] MEM_MA_CKE3
MEM_MA_CKE0 AV22 SA_CKE_0
MEM_MA_CKE1 AT23 SA_CKE_1
MEM_MA_CKE2 AU22 SA_CKE_2
MEM_MA_CKE3 AU23 SA_CKE_3
[7] MEM_MA_ODT0
[7] MEM_MA_ODT1
[7] MEM_MA_ODT2
[7] MEM_MA_ODT3
MEM_MA_ODT0 AW10 SA_ODT_0
MEM_MA_ODT1 AY8 SA_ODT_1
MEM_MA_ODT2 AW9 SA_ODT_2
MEM_MA_ODT3 AU8 SA_ODT_3
[7] MEM_MA_CLK_H0
[7] MEM_MA_CLK_L0
[7] MEM_MA_CLK_H1
[7] MEM_MA_CLK_L1
[7] MEM_MA_CLK_H2
[7] MEM_MA_CLK_L2
[7] MEM_MA_CLK_H3
[7] MEM_MA_CLK_L3
MEM_MA_CLK_H0 AY15 SA_CK_0
MEM_MA_CLK_L0 AY16 SA_CK#_0
MEM_MA_CLK_H1 AW15 SA_CK_1
MEM_MA_CLK_L1 AY15 SA_CK#_1
MEM_MA_CLK_H2 AY14 SA_CK_2
MEM_MA_CLK_L2 AW14 SA_CK#_2
MEM_MA_CLK_H3 AW13 SA_CK_3
MEM_MA_CLK_L3 AY13 SA_CK#_3
[7,8] DDR3_DRAMRST#
R130 X_R2
DDR3_RST# AK22 SM_DRAMRST#
C77 X_0.1u10X4
CRB
AW33 SA_ECC_CB_0
AV33 SA_ECC_CB_1
AU31 SA_ECC_CB_2
AV31 SA_ECC_CB_3
AT33 SA_ECC_CB_4
AU33 SA_ECC_CB_5
AT31 SA_ECC_CB_6
AW31 SA_ECC_CB_7
CPU_VREF_DQ_A
AB39 SA_DIMM_VREFDQ
SA_DQ_0 AD38 MEM_MA_DATA0
SA_DQ_1 AD39 MEM_MA_DATA1
SA_DQ_2 AE38 MEM_MA_DATA2
SA_DQ_3 AE39 MEM_MA_DATA3
SA_DQ_4 AD37 MEM_MA_DATA4
SA_DQ_5 AD40 MEM_MA_DATA5
SA_DQ_6 AE37 MEM_MA_DATA6
SA_DQ_7 AE40 MEM_MA_DATA7
SA_DQ_8 AH40 MEM_MA_DATA8
SA_DQ_9 AH39 MEM_MA_DATA9
SA_DQ_10 AK38 MEM_MA_DATA10
SA_DQ_11 AK39 MEM_MA_DATA11
SA_DQ_12 AH37 MEM_MA_DATA12
SA_DQ_13 AH38 MEM_MA_DATA13
SA_DQ_14 AK37 MEM_MA_DATA14
SA_DQ_15 AK40 MEM_MA_DATA15
SA_DQ_16 AM40 MEM_MA_DATA16
SA_DQ_17 AM39 MEM_MA_DATA17
SA_DQ_18 AP38 MEM_MA_DATA18
SA_DQ_19 AP39 MEM_MA_DATA19
SA_DQ_20 AM37 MEM_MA_DATA20
SA_DQ_21 AM38 MEM_MA_DATA21
SA_DQ_22 AP37 MEM_MA_DATA22
SA_DQ_23 AP40 MEM_MA_DATA23
SA_DQ_24 AV37 MEM_MA_DATA24
SA_DQ_25 AW37 MEM_MA_DATA25
SA_DQ_26 AU35 MEM_MA_DATA26
SA_DQ_27 AV35 MEM_MA_DATA27
SA_DQ_28 AT37 MEM_MA_DATA28
SA_DQ_29 AU37 MEM_MA_DATA29
SA_DQ_30 AT35 MEM_MA_DATA30
SA_DQ_31 AW35 MEM_MA_DATA31
SA_DQ_32 AY6 MEM_MA_DATA32
SA_DQ_33 AU6 MEM_MA_DATA33
SA_DQ_34 AV4 MEM_MA_DATA34
SA_DQ_35 AU4 MEM_MA_DATA35
SA_DQ_36 AW6 MEM_MA_DATA36
SA_DQ_37 AV6 MEM_MA_DATA37
SA_DQ_38 AW4 MEM_MA_DATA38
SA_DQ_39 AY4 MEM_MA_DATA39
SA_DQ_40 AR1 MEM_MA_DATA40
SA_DQ_41 AR4 MEM_MA_DATA41
SA_DQ_42 AN3 MEM_MA_DATA42
SA_DQ_43 AN4 MEM_MA_DATA43
SA_DQ_44 AR2 MEM_MA_DATA44
SA_DQ_45 AR3 MEM_MA_DATA45
SA_DQ_46 AN2 MEM_MA_DATA46
SA_DQ_47 AN1 MEM_MA_DATA47
SA_DQ_48 AL1 MEM_MA_DATA48
SA_DQ_49 AL4 MEM_MA_DATA49
SA_DQ_50 AJ3 MEM_MA_DATA50
SA_DQ_51 AJ4 MEM_MA_DATA51
SA_DQ_52 AL2 MEM_MA_DATA52
SA_DQ_53 AL3 MEM_MA_DATA53
SA_DQ_54 AJ2 MEM_MA_DATA54
SA_DQ_55 AJ1 MEM_MA_DATA55
SA_DQ_56 AG1 MEM_MA_DATA56
SA_DQ_57 AG4 MEM_MA_DATA57
SA_DQ_58 AE3 MEM_MA_DATA58
SA_DQ_59 AE4 MEM_MA_DATA59
SA_DQ_60 AG2 MEM_MA_DATA60
SA_DQ_61 AG3 MEM_MA_DATA61
SA_DQ_62 AE2 MEM_MA_DATA62
SA_DQ_63 AE1 MEM_MA_DATA63
MEM_MA_DATA[63..0] [7]
SA_DQS_0 AE39 MEM_MA_DQS_H0
SA_DQS_1 AJ39 MEM_MA_DQS_H1
SA_DQS_2 AN39 MEM_MA_DQS_H2
SA_DQS_3 AV36 MEM_MA_DQS_H3
SA_DQS_4 AV5 MEM_MA_DQS_H4
SA_DQS_5 AP3 MEM_MA_DQS_H5
SA_DQS_6 AK3 MEM_MA_DQS_H6
SA_DQS_7 AF3 MEM_MA_DQS_H7
SA_DQS_8 AV32
MEM_MA_DQS_H0 [7]
MEM_MA_DQS_H1 [7]
MEM_MA_DQS_H2 [7]
MEM_MA_DQS_H3 [7]
MEM_MA_DQS_H4 [7]
MEM_MA_DQS_H5 [7]
MEM_MA_DQS_H6 [7]
MEM_MA_DQS_H7 [7]
SA_DQS#_0 AE38 MEM_MA_DQS_L0
SA_DQS#_1 AJ38 MEM_MA_DQS_L1
SA_DQS#_2 AN38 MEM_MA_DQS_L2
SA_DQS#_3 AU36 MEM_MA_DQS_L3
SA_DQS#_4 AW5 MEM_MA_DQS_L4
SA_DQS#_5 AP2 MEM_MA_DQS_L5
SA_DQS#_6 AK2 MEM_MA_DQS_L6
SA_DQS#_7 AF2 MEM_MA_DQS_L7
SA_DQS#_8 AU32
MEM_MA_DQS_L0 [7]
MEM_MA_DQS_L1 [7]
MEM_MA_DQS_L2 [7]
MEM_MA_DQS_L3 [7]
MEM_MA_DQS_L4 [7]
MEM_MA_DQS_L5 [7]
MEM_MA_DQS_L6 [7]
MEM_MA_DQS_L7 [7]
HASWELL (ACA-ZIF-138-P01)
CPU1B
2 OF 9
[8] MEM_MB_ADD[15..0]
MEM_MB_ADD0 AL19 SB_MA_0
MEM_MB_ADD1 AK23 SB_MA_1
MEM_MB_ADD2 AM22 SB_MA_2
MEM_MB_ADD3 AM23 SB_MA_3
MEM_MB_ADD4 AP23 SB_MA_4
MEM_MB_ADD5 AL23 SB_MA_5
MEM_MB_ADD6 AY24 SB_MA_6
MEM_MB_ADD7 AV25 SB_MA_7
MEM_MB_ADD8 AU26 SB_MA_8
MEM_MB_ADD9 AW25 SB_MA_9
MEM_MB_ADD10 AP18 SB_MA_10
MEM_MB_ADD11 AY25 SB_MA_11
MEM_MB_ADD12 AV26 SB_MA_12
MEM_MB_ADD13 AR15 SB_MA_13
MEM_MB_ADD14 AV27 SB_MA_14
MEM_MB_ADD15 AY28 SB_MA_15
[8] MEM_MB_WE_L
[8] MEM_MB_CAS_L
[8] MEM_MB_RAS_L
MEM_MB_WE_L AK16 SB_WE#
MEM_MB_CAS_L AP16 SB_CAS#
MEM_MB_RAS_L AM18 SB_RAS#
[8] MEM_MB_BANK0
[8] MEM_MB_BANK1
[8] MEM_MB_BANK2
MEM_MB_BANK0 AK17 SB_BS_0
MEM_MB_BANK1 AL18 SB_BS_1
MEM_MB_BANK2 AW28 SB_BS_2
[8] MEM_MB_CS_L0
[8] MEM_MB_CS_L1
[8] MEM_MB_CS_L2
[8] MEM_MB_CS_L3
MEM_MB_CS_L0 AP17 SB_CS#_0
MEM_MB_CS_L1 AN15 SB_CS#_1
MEM_MB_CS_L2 AN17 SB_CS#_2
MEM_MB_CS_L3 AL15 SB_CS#_3
[8] MEM_MB_CKE0
[8] MEM_MB_CKE1
[8] MEM_MB_CKE2
[8] MEM_MB_CKE3
MEM_MB_CKE0 AW29 SB_CKE_0
MEM_MB_CKE1 AY29 SB_CKE_1
MEM_MB_CKE2 AU28 SB_CKE_2
MEM_MB_CKE3 AU29 SB_CKE_3
[8] MEM_MB_ODT0
[8] MEM_MB_ODT1
[8] MEM_MB_ODT2
[8] MEM_MB_ODT3
MEM_MB_ODT0 AM17 SB_ODT_0
MEM_MB_ODT1 AL16 SB_ODT_1
MEM_MB_ODT2 AM16 SB_ODT_2
MEM_MB_ODT3 AK15 SB_ODT_3
[8] MEM_MB_CLK_H0
[8] MEM_MB_CLK_L0
[8] MEM_MB_CLK_H1
[8] MEM_MB_CLK_L1
[8] MEM_MB_CLK_H2
[8] MEM_MB_CLK_L2
[8] MEM_MB_CLK_H3
[8] MEM_MB_CLK_L3
MEM_MB_CLK_H0 AM20 SB_CK_0
MEM_MB_CLK_L0 AM21 SB_CK#_0
MEM_MB_CLK_H1 AP22 SB_CK_1
MEM_MB_CLK_L1 AP21 SB_CK#_1
MEM_MB_CLK_H2 AN20 SB_CK_2
MEM_MB_CLK_L2 AN21 SB_CK#_2
MEM_MB_CLK_H3 AP19 SB_CK_3
MEM_MB_CLK_L3 AP20 SB_CK#_3
AM26 SB_ECC_CB_0
AM25 SB_ECC_CB_1
AP25 SB_ECC_CB_2
AP26 SB_ECC_CB_3
AL26 SB_ECC_CB_4
AL25 SB_ECC_CB_5
AR26 SB_ECC_CB_6
AR25 SB_ECC_CB_7
CPU_VREF_DQ_B
AB40 SB_DIMM_VREFDQ
SB_DQ_0 AE34 MEM_MB_DATA0
SB_DQ_1 AE35 MEM_MB_DATA1
SB_DQ_2 AG35 MEM_MB_DATA2
SB_DQ_3 AH35 MEM_MB_DATA3
SB_DQ_4 AD34 MEM_MB_DATA4
SB_DQ_5 AD35 MEM_MB_DATA5
SB_DQ_6 AG34 MEM_MB_DATA6
SB_DQ_7 AH34 MEM_MB_DATA7
SB_DQ_8 AL34 MEM_MB_DATA8
SB_DQ_9 AL35 MEM_MB_DATA9
SB_DQ_10 AK31 MEM_MB_DATA10
SB_DQ_11 AL31 MEM_MB_DATA11
SB_DQ_12 AK34 MEM_MB_DATA12
SB_DQ_13 AK35 MEM_MB_DATA13
SB_DQ_14 AK32 MEM_MB_DATA14
SB_DQ_15 AL32 MEM_MB_DATA15
SB_DQ_16 AN34 MEM_MB_DATA16
SB_DQ_17 AP34 MEM_MB_DATA17
SB_DQ_18 AN31 MEM_MB_DATA18
SB_DQ_19 AP31 MEM_MB_DATA19
SB_DQ_20 AN35 MEM_MB_DATA20
SB_DQ_21 AP35 MEM_MB_DATA21
SB_DQ_22 AN32 MEM_MB_DATA22
SB_DQ_23 AP32 MEM_MB_DATA23
SB_DQ_24 AM29 MEM_MB_DATA24
SB_DQ_25 AM28 MEM_MB_DATA25
SB_DQ_26 AR29 MEM_MB_DATA26
SB_DQ_27 AR28 MEM_MB_DATA27
SB_DQ_28 AL29 MEM_MB_DATA28
SB_DQ_29 AL28 MEM_MB_DATA29
SB_DQ_30 AP29 MEM_MB_DATA30
SB_DQ_31 AP28 MEM_MB_DATA31
SB_DQ_32 AR12 MEM_MB_DATA32
SB_DQ_33 AP12 MEM_MB_DATA33
SB_DQ_34 AL13 MEM_MB_DATA34
SB_DQ_35 AL12 MEM_MB_DATA35
SB_DQ_36 AR13 MEM_MB_DATA36
SB_DQ_37 AP13 MEM_MB_DATA37
SB_DQ_38 AM13 MEM_MB_DATA38
SB_DQ_39 AM12 MEM_MB_DATA39
SB_DQ_40 AR9 MEM_MB_DATA40
SB_DQ_41 AP9 MEM_MB_DATA41
SB_DQ_42 AR6 MEM_MB_DATA42
SB_DQ_43 AP6 MEM_MB_DATA43
SB_DQ_44 AR10 MEM_MB_DATA44
SB_DQ_45 AP10 MEM_MB_DATA45
SB_DQ_46 AR7 MEM_MB_DATA46
SB_DQ_47 AP7 MEM_MB_DATA47
SB_DQ_48 AM9 MEM_MB_DATA48
SB_DQ_49 AL9 MEM_MB_DATA49
SB_DQ_50 AL6 MEM_MB_DATA50
SB_DQ_51 AL7 MEM_MB_DATA51
SB_DQ_52 AM10 MEM_MB_DATA52
SB_DQ_53 AL10 MEM_MB_DATA53
SB_DQ_54 AM6 MEM_MB_DATA54
SB_DQ_55 AM7 MEM_MB_DATA55
SB_DQ_56 AH6 MEM_MB_DATA56
SB_DQ_57 AH7 MEM_MB_DATA57
SB_DQ_58 AE6 MEM_MB_DATA58
SB_DQ_59 AE7 MEM_MB_DATA59
SB_DQ_60 AJ6 MEM_MB_DATA60
SB_DQ_61 AJ7 MEM_MB_DATA61
SB_DQ_62 AF6 MEM_MB_DATA62
SB_DQ_63 AF7 MEM_MB_DATA63
MEM_MB_DATA[63..0] [8]
SB_DQS_0 AF35 MEM_MB_DQS_H0
SB_DQS_1 AL33 MEM_MB_DQS_H1
SB_DQS_2 AP33 MEM_MB_DQS_H2
SB_DQS_3 AN28 MEM_MB_DQS_H3
SB_DQS_4 AN12 MEM_MB_DQS_H4
SB_DQS_5 AP8 MEM_MB_DQS_H5
SB_DQS_6 AL8 MEM_MB_DQS_H6
SB_DQS_7 AG7 MEM_MB_DQS_H7
SB_DQS_8 AN25
MEM_MB_DQS_H0 [8]
MEM_MB_DQS_H1 [8]
MEM_MB_DQS_H2 [8]
MEM_MB_DQS_H3 [8]
MEM_MB_DQS_H4 [8]
MEM_MB_DQS_H5 [8]
MEM_MB_DQS_H6 [8]
MEM_MB_DQS_H7 [8]
SB_DQS#_0 AF34 MEM_MB_DQS_L0
SB_DQS#_1 AK33 MEM_MB_DQS_L1
SB_DQS#_2 AN33 MEM_MB_DQS_L2
SB_DQS#_3 AN29 MEM_MB_DQS_L3
SB_DQS#_4 AN13 MEM_MB_DQS_L4
SB_DQS#_5 AR8 MEM_MB_DQS_L5
SB_DQS#_6 AM8 MEM_MB_DQS_L6
SB_DQS#_7 AG6 MEM_MB_DQS_L7
SB_DQS#_8 AN26
MEM_MB_DQS_L0 [8]
MEM_MB_DQS_L1 [8]
MEM_MB_DQS_L2 [8]
MEM_MB_DQS_L3 [8]
MEM_MB_DQS_L4 [8]
MEM_MB_DQS_L5 [8]
MEM_MB_DQS_L6 [8]
MEM_MB_DQS_L7 [8]
HASWELL (ACA-ZIF-138-P01)
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Document Description CPU-Memory
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Date: Friday, January 24, 2014
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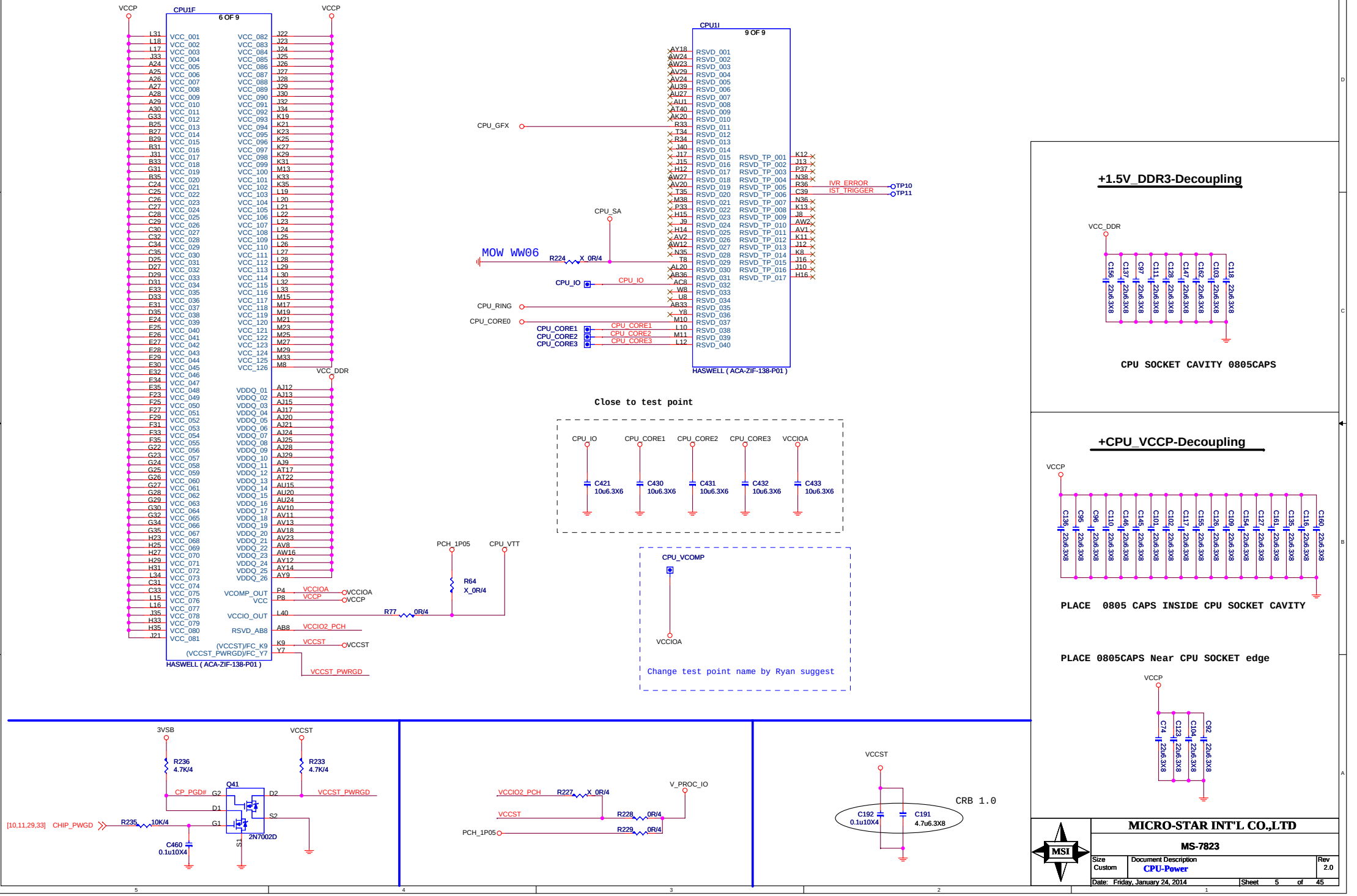
CPU1F
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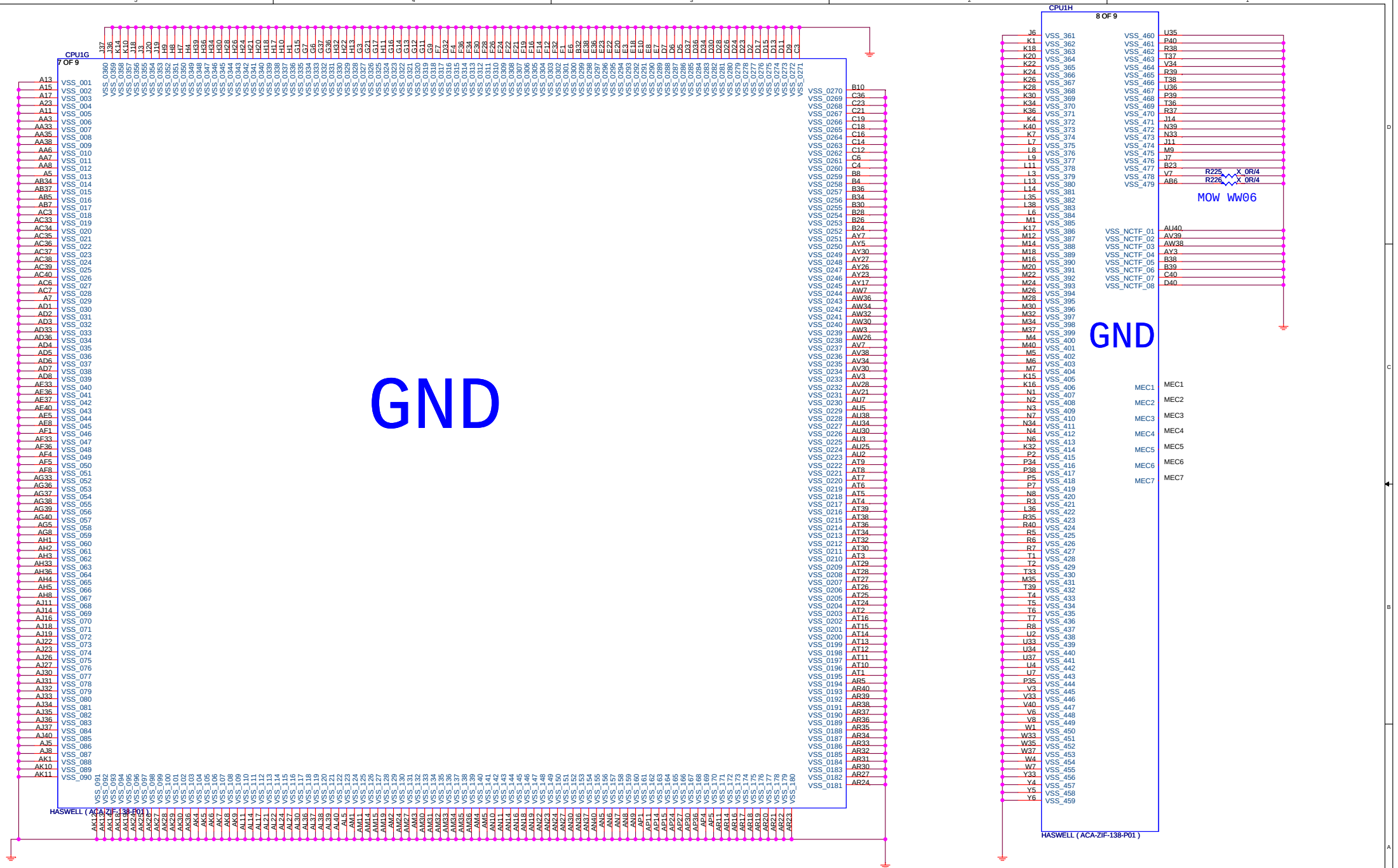
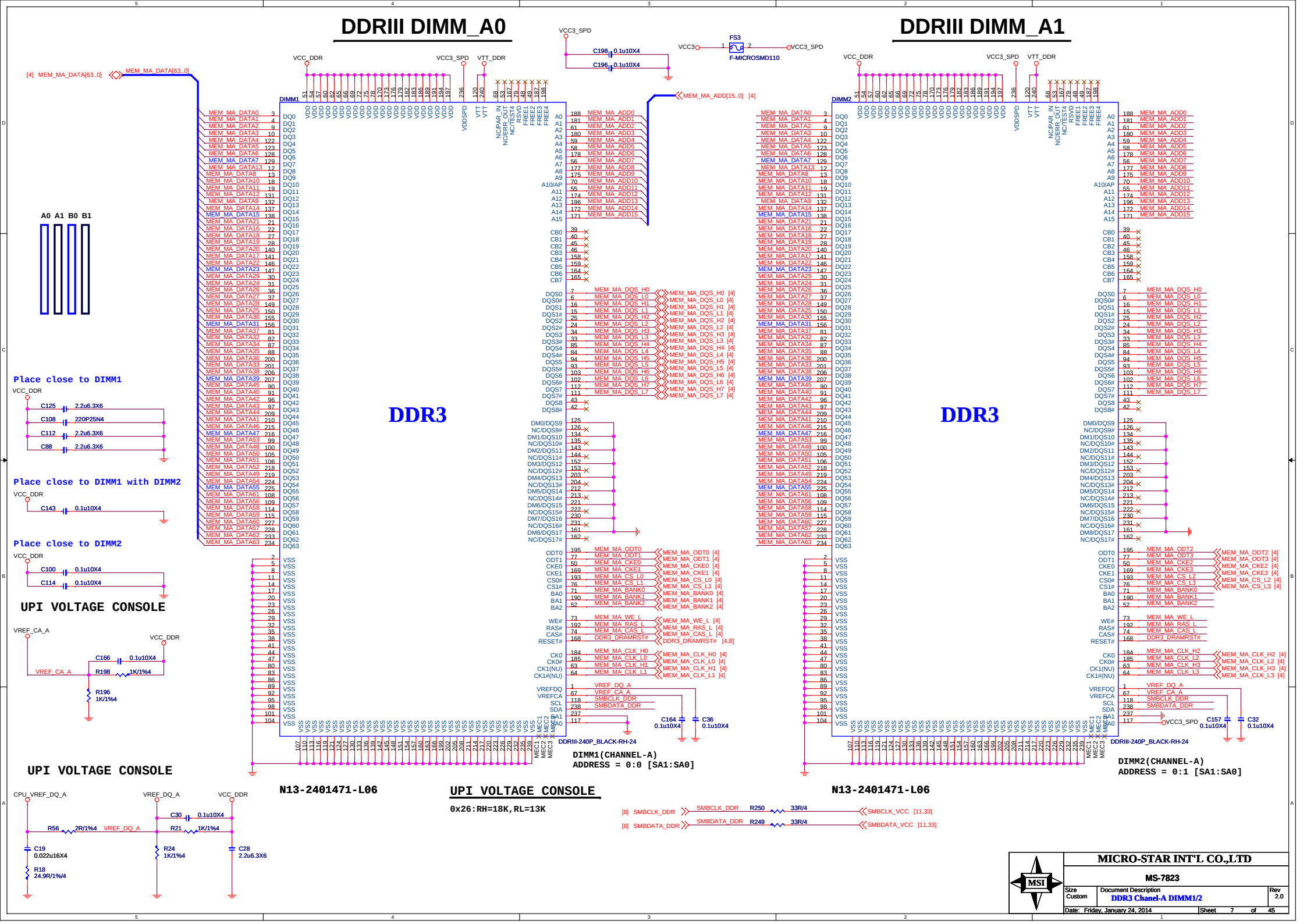
HASWELL (ACA-ZIF-138-P01)
VCCP
VCC_DDR
VCC_001
VCC_002
VCC_003
VCC_004
VCC_005
VCC_006
VCC_007
VCC_008
VCC_009
VCC_010
VCC_011
VCC_012
VCC_013
VCC_014
VCC_015
VCC_016
VCC_017
VCC_018
VCC_019
VCC_020
VCC_021
VCC_022
VCC_023
VCC_024
VCC_025
VCC_026
VCC_027
VCC_028
VCC_029
VCC_030
VCC_031
VCC_032
VCC_033
VCC_034
VCC_035
VCC_036
VCC_037
VCC_038
VCC_039
VCC_040
VCC_041
VCC_042
VCC_043
VCC_044
VCC_045
VCC_046
VCC_047
VCC_048
VCC_049
VCC_050
VCC_051
VCC_052
VCC_053
VCC_054
VCC_055
VCC_056
VCC_057
VCC_058
VCC_059
VCC_060
VCC_061
VCC_062
VCC_063
VCC_064
VCC_065
VCC_066
VCC_067
VCC_068
VCC_069
VCC_070
VCC_071
VCC_072
VCC_073
VCC_074
VCC_075
VCC_076
VCC_077
VCC_078
VCC_079
VCC_080
VCC_081
VCC_082
VCC_083
VCC_084
VCC_085
VCC_086
VCC_087
VCC_088
VCC_089
VCC_090
VCC_091
VCC_092
VCC_093
VCC_094
VCC_095
VCC_096
VCC_097
VCC_098
VCC_099
VCC_100
VCC_101
VCC_102
VCC_103
VCC_104
VCC_105
VCC_106
VCC_107
VCC_108
VCC_109
VCC_110
VCC_111
VCC_112
VCC_113
VCC_114
VCC_115
VCC_116
VCC_117
VCC_118
VCC_119
VCC_120
VCC_121
VCC_122
VCC_123
VCC_124
VCC_125
VCC_126
VDDQ_01
VDDQ_02
VDDQ_03
VDDQ_04
VDDQ_05
VDDQ_06
VDDQ_07
VDDQ_08
VDDQ_09
VDDQ_10
VDDQ_11
VDDQ_12
VDDQ_13
VDDQ_14
VDDQ_15
VDDQ_16
VDDQ_17
VDDQ_18
VDDQ_19
VDDQ_20
VDDQ_21
VDDQ_22
VDDQ_23
VDDQ_24
VDDQ_25
VDDQ_26
VCOMP_OUT
VCC
VCCIO_OUT
RSVD_AB8
(VCCST)/FC_K9
(VCCST_PWRGD)/FC_Y7
VCCIOA
VCCP
VCCST
VCCST_PWRGD
VCCIO2_PCH
R64
X_0R/4
R77
0R/4
PCH_1P05
CPU_VTT
CPU1I
9 OF 9
RSVD_001
RSVD_002
RSVD_003
RSVD_004
RSVD_005
RSVD_006
RSVD_007
RSVD_008
RSVD_009
RSVD_010
RSVD_011
RSVD_012
RSVD_013
RSVD_014
RSVD_015
RSVD_016
RSVD_017
RSVD_018
RSVD_019
RSVD_020
RSVD_021
RSVD_022
RSVD_023
RSVD_024
RSVD_025
RSVD_026
RSVD_027
RSVD_028
RSVD_029
RSVD_030
RSVD_031
RSVD_032
RSVD_033
RSVD_034
RSVD_035
RSVD_036
RSVD_037
RSVD_038
RSVD_039
RSVD_040
RSVD_TP_001
RSVD_TP_002
RSVD_TP_003
RSVD_TP_004
RSVD_TP_005
RSVD_TP_006
RSVD_TP_007
RSVD_TP_008
RSVD_TP_009
RSVD_TP_010
RSVD_TP_011
RSVD_TP_012
RSVD_TP_013
RSVD_TP_014
RSVD_TP_015
RSVD_TP_016
RSVD_TP_017
HASWELL (ACA-ZIF-138-P01)
CPU_GFX
CPU_SA
MOW WW06
R224
X_0R/4
CPU_IO
CPU_RING
CPU_CORE0
CPU_CORE1
CPU_CORE2
CPU_CORE3
IVR_ERROR
IST_TRIGGER
TP10
TP11
Close to test point
C421
10u6.3X6
C430
10u6.3X6
C431
10u6.3X6
C432
10u6.3X6
C433
10u6.3X6
CPU_VCOMP
VCCIOA
Change test point name by Ryan suggest
+1.5V_DDR3-Decoupling
VCC_DDR
C156
22u6.3X8
C137
22u6.3X8
C97
22u6.3X8
C111
22u6.3X8
C128
22u6.3X8
C147
22u6.3X8
C162
22u6.3X8
C103
22u6.3X8
C118
22u6.3X8
CPU SOCKET CAVITY 0805CAPS
+CPU_VCCP-Decoupling
VCCP
C136
22u6.3X8
C95
22u6.3X8
C96
22u6.3X8
C110
22u6.3X8
C146
22u6.3X8
C145
22u6.3X8
C101
22u6.3X8
C102
22u6.3X8
C117
22u6.3X8
C155
22u6.3X8
C126
22u6.3X8
C109
22u6.3X8
C154
22u6.3X8
C127
22u6.3X8
C161
22u6.3X8
C135
22u6.3X8
C116
22u6.3X8
C160
22u6.3X8
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY
PLACE 0805CAPS Near CPU SOCKET edge
C74
22u6.3X8
C123
22u6.3X8
C104
22u6.3X8
C92
22u6.3X8
3VSB
R236
4.7K/4
VCCST
R233
4.7K/4
CP_PGD#
Q41
2N7002D
VCCST_PWRGD
[10,11,29,33]
CHIP_PWGD
R235
10K/4
C460
0.1u10X4
VCCIO2_PCH
R227
X_0R/4
V_PROC_IO
VCCST
R228
0R/4
PCH_1P05
R229
0R/4
VCCST
C192
0.1u10X4
C191
4.7u6.3X8
CRB 1.0
MICRO-STAR INT'L CO.,LTD
MS-7823
Size
Custom
Document Description
CPU-Power
Rev
2.0
Date: Friday, January 24, 2014
Sheet 5 of 45



MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: CPU-GND
Rev: 2.0	
Date: Friday, January 24, 2014	Sheet 6 of 45

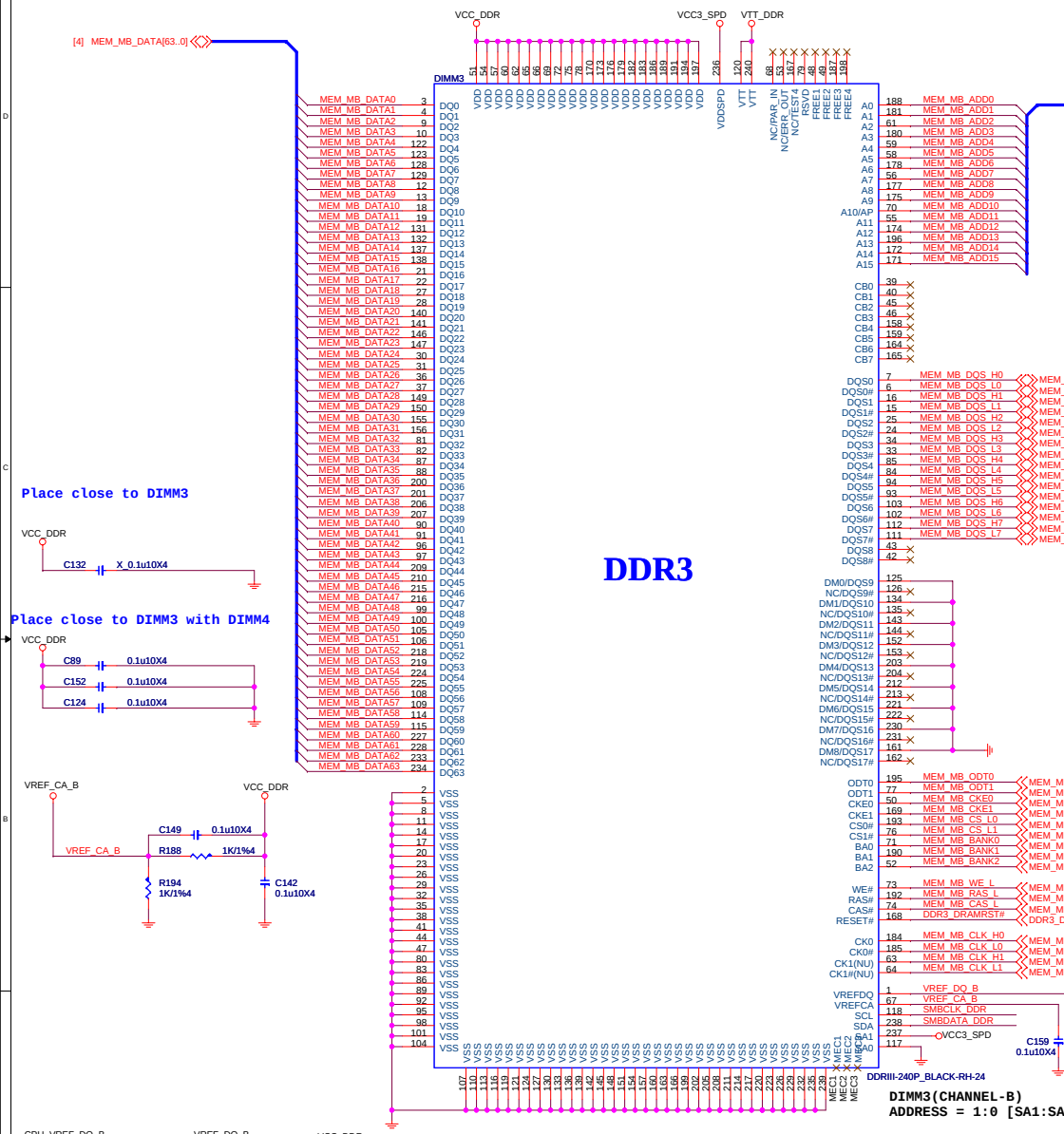
DDRIII DIMM_A0

DDRIII DIMM_A1



MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
Rev: 2.0	
Date: Friday, January 24, 2014	Sheet 7 of 45

DDRIII DIMM_B0



DIMM3(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]

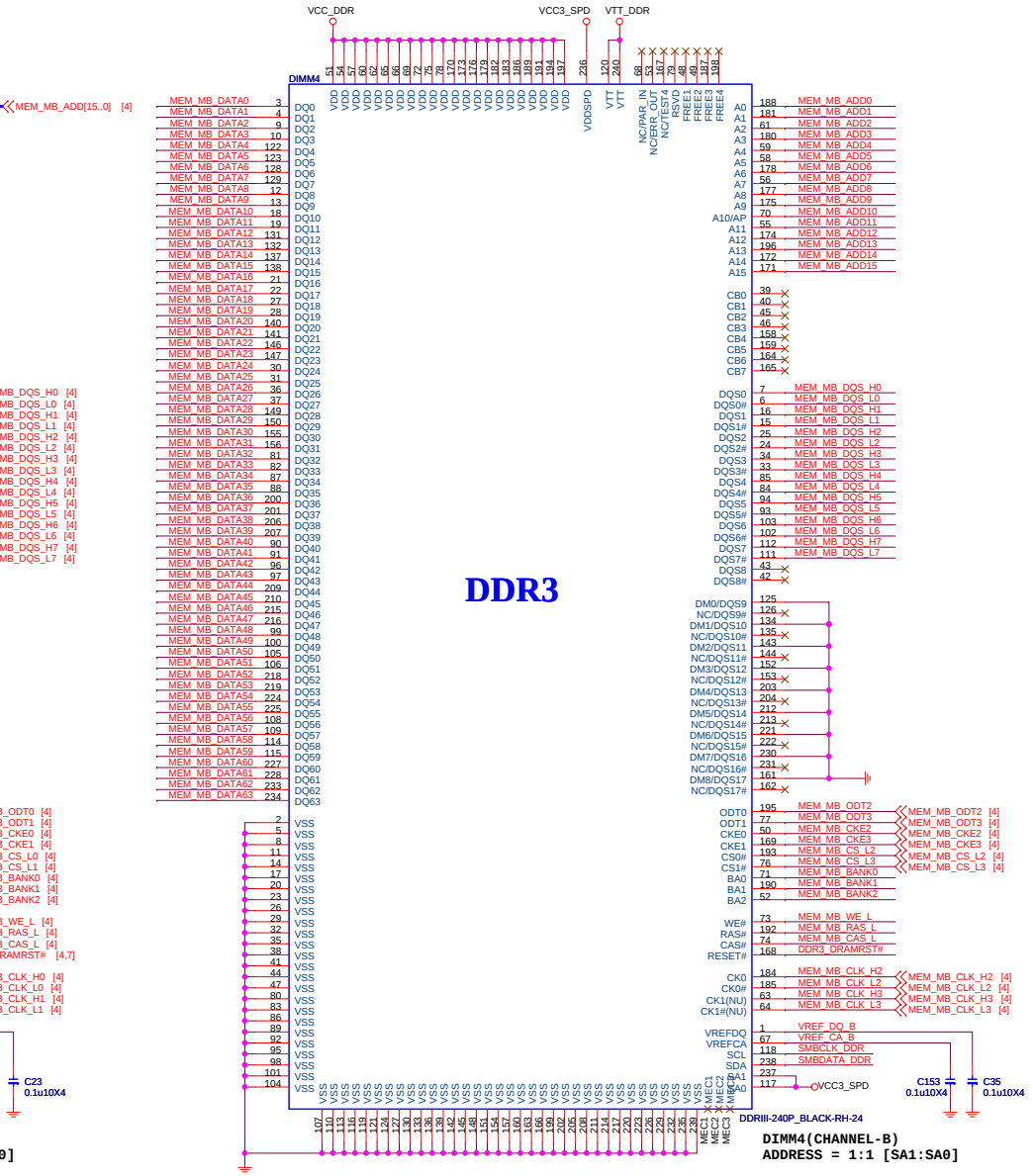
N13-2401471-L06

SMBCLK_DDR → SMBCLK_DDR [7]
SMBDATA_DDR → SMBDATA_DDR [7]

UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K

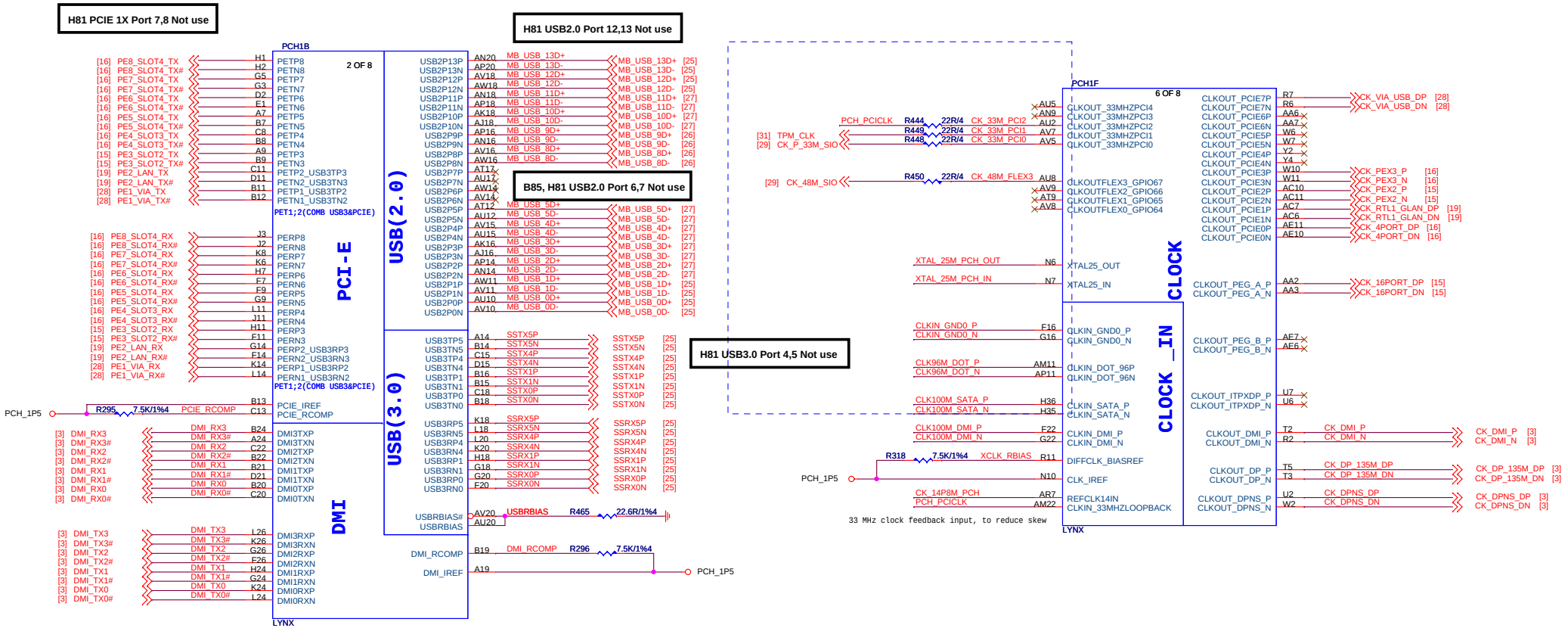
DDRIII DIMM_B1

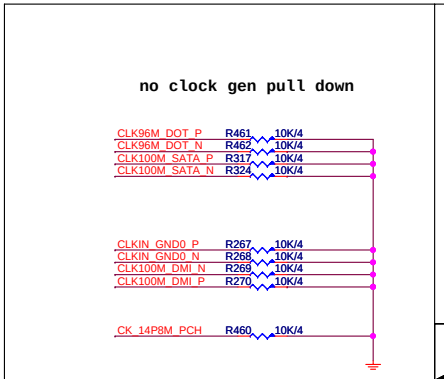


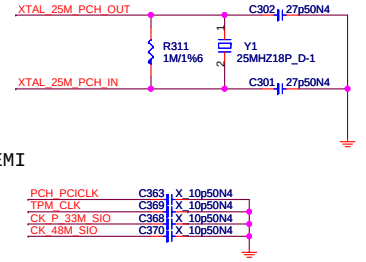
DIMM4(CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]

N13-2401471-L06

MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4	Rev: 2.0
Date: Friday, January 24, 2014	Sheet 8 of 45	







MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: LYNX-PCIE/DMI/CLK/USB20	Rev: 2.0
Date: Friday, January 24, 2014	Sheet 9 of 45	

SATA port
Z87,H87: port 0, 1, 2, 3, 4, 5, 6 are SATA 6G
B85: GEN3 port 0, 1, 2, 3
H81: GEN3 port 0, 1 , GEN2 port 5, 6

H81->Stuff R456
B85->Stuff R459

H81 SATA Port 2,3 Not use

PCH1C

CLINK
FAN
GPIO
SATA
HOST

SATA4;5(COMB SATA&PCIE)

3 OF8
LYNX

OC#0 Rear USB3.0 for SVCC1
(USB3.0 port1 ; USB2.0 Port1)
OC#1 Rear USB3.0 for SVCC2
(USB3.0 port0 ; USB2.0 Port0)
OC#2 Front USB2.0 for 5V_RUSB1
(USB2.0 Port2,3,4,5)
OC#4 Rear USB2.0 for 5V_FUSB1
(USB2.0 Port10,11)
OC#5 Front USB charge port I_VCC1, I_VCC2
(USB2.0 Port8,9)
OC#6 Front USB3.0 for SVCC0
(USB3.0 port4,5 ; USB2.0 Port12,13)

PCH1A

Some condition control for BIOS use

1 OF8
PIRQ&GPIO
LYNX

PCH1E

VGA
PORT B
PORT C
PORT D
eDP CONTROL
FDILINK
DISPLAY

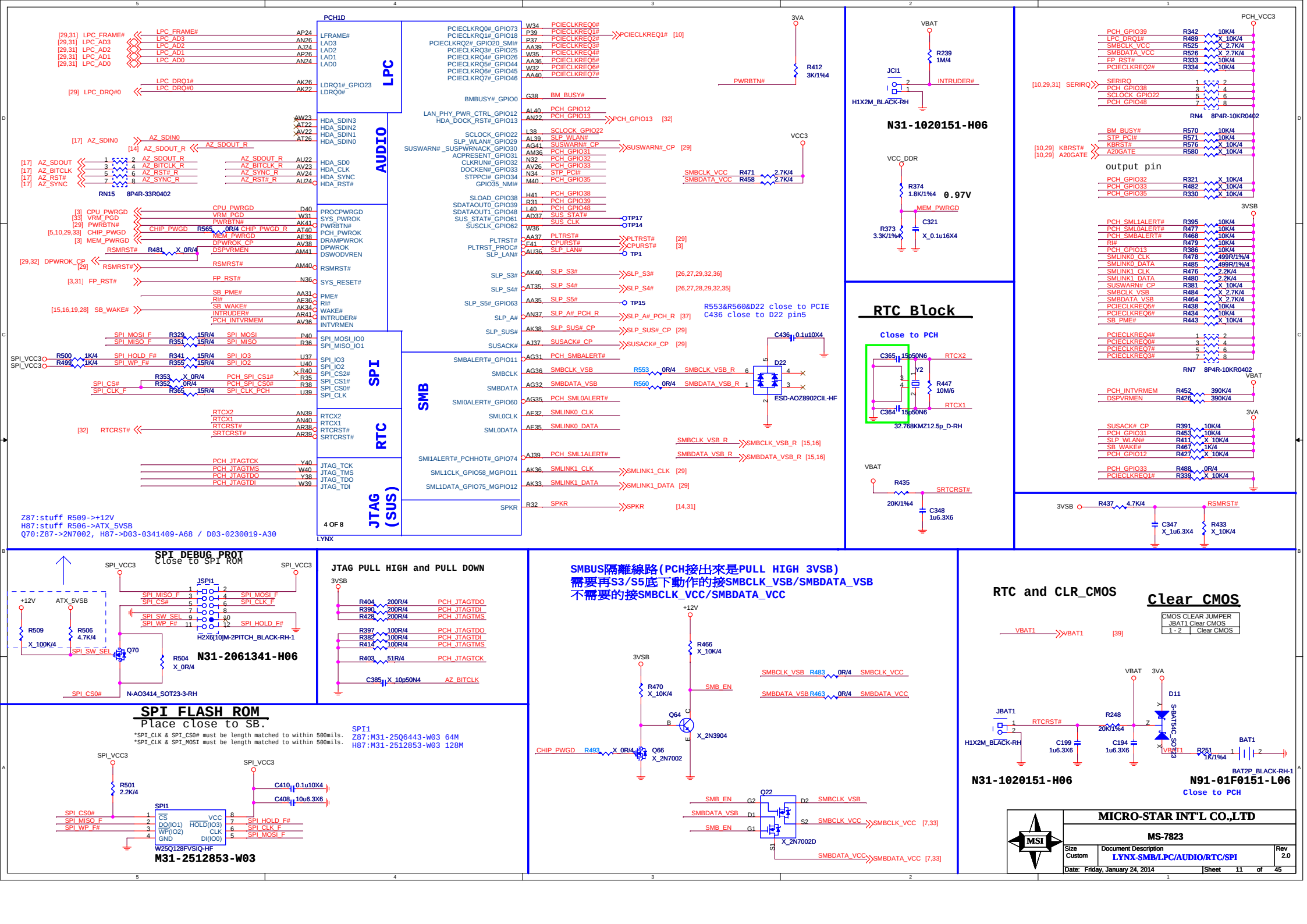
LYNX

OC#3 not used
need pull high

output pin

Close to PCH within 250 mils.

MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: LYNX-SATA/HOST/GPIO/VGA
Rev: 2.0	
Date: Friday, January 24, 2014	Sheet 10 of 45


PCH1D
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
LFRAME#
LAD3
LAD2
LAD1
LAD0
LDRQ1#_GIO23
LDRQ0#
HDA_SDIN3
HDA_SDIN2
HDA_SDIN1
HDA_SDIN0
HDA_SD0
HDA_CLK
HDA_SYNC
HDA_RST#
PROCPWRGD
SYS_PWROK
PWRBTN#
PCH_PWROK
DRAMPWROK
DPWROK
DSWODVREN
RSMRST#
SYS_RESET#
PME#
RI#
WAKE#
INTRUDER#
INTVRMEN
SPI_MOSI_IO0
SPI_MISO_IO1
SPI_IO3
SPI_IO2
SPI_CS2#
SPI_CS1#
SPI_CS0#
SPI_CLK
RTCX2
RTCX1
RTCRST#
SRTCRST#
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
4 OF 8
LYNX
PCIECLKRQ0#_GPIO73
PCIECLKRQ1#_GPIO18
PCIECLKRQ2#_GPIO20_SMI#
PCIECLKRQ3#_GPIO25
PCIECLKRQ4#_GPIO26
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
BMBUSY#_GPIO0
LAN_PHY_PWR_CTRL_GPIO12
HDA_DOCK_RST#_GPIO13
SCLOCK_GPIO22
SLP_WLAN#_GPIO29
SUSWARN#_SUSPWRNACK_GPIO30
ACPRESENT_GPIO31
CLKRUN#_GPIO32
DOCKEN#_GPIO33
STPPCI#_GPIO34
GPIO35_NMI#
SLOAD_GPIO38
SDATAOUT0_GPIO39
SDATAOUT1_GPIO48
SUS_STAT#_GPIO61
SUSCLK_GPIO62
PLTRST#
PLTRST_PROC#
SLP_LAN#
SLP_S3#
SLP_S4#
SLP_S5#_GPIO63
SLP_A#
SLP_SUS#
SUSACK#
SMBALERT#_GPIO11
SMBCLK
SMBDATA
SMI0ALERT#_GPIO60
SML0CLK
SML0DATA
SMI1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO58_MGPIO11
SML1DATA_GPIO75_MGPIO12
SPKR
PCIECLKREQ0#
PCIECLKREQ1#
PCIECLKREQ2#
PCIECLKREQ3#
PCIECLKREQ4#
PCIECLKREQ5#
PCIECLKREQ6#
PCIECLKREQ7#
BM_BUSY#
PCH_GPIO12
PCH_GPIO13
SCLOCK_GPIO22
SLP_WLAN#
SUSWARN#_CP
PCH_GPIO31
PCH_GPIO32
PCH_GPIO33
STP_PCI#
PCH_GPIO35
PCH_GPIO38
PCH_GPIO39
PCH_GPIO48
SUS_STAT#
SUS_CLK
TP17
TP14
PLTRST#
CPURST#
SLP_LAN#
TP1
SLP_S3#
SLP_S4#
TP15
SLP_A#_PCH_R
SLP_SUS#_CP
SUSACK#_CP
PCH_SMBALERT#
SMBCLK_VSB
SMBDATA_VSB
PCH_SML0ALERT#
SMLINK0_CLK
SMLINK0_DATA
PCH_SML1ALERT#
SMLINK1_CLK
SMLINK1_DATA
SPKR
R553 0R/4
R560 0R/4
SMBCLK_VSB_R
SMBDATA_VSB_R
D22
ESD-AOZ8902CIL-HF
C436 0.1u10X4
3VA
R412 3K/1%4
PWRBTN#
VCC3
SMBCLK_VCC R471 2.7K/4
SMBDATA_VCC R458 2.7K/4
LPC_FRAME# AP24
LPC_AD3 AN26
LPC_AD2 AJ24
LPC_AD1 AP26
LPC_AD0 AN24
LPC_DRQ1# AK26
LPC_DRQ0 AK22
AZ_SDIN0 AW23
AZ_SDIN2 AT22
AZ_SDIN1 AV22
AZ_SDIN0 AT26
AZ_SDOUT_R
AZ_BITCLK_R
AZ_RST#_R
AZ_SYNC_R
AZ_SDOUT_R AU22
AZ_BITCLK_R AV23
AZ_SYNC_R AV24
AZ_RST#_R AU24
RN15 8P4R-33R0402
CPU_PWRGD D40
VRM_PGD W31
PWRBTN# AK41
CHIP_PWGD R565 0R/4 CHIP_PWGD_R AT40
MEM_PWRGD AE38
DPWROK_CP AV38
DSPVRMEN AM41
RSMRST# R481 X_0R/4
RSMRST# AM40
FP_RST# N36
SB_PME# AA31
RI# AE36
SB_WAKE# AK34
INTRUDER# AR41
PCH_INTVRMEM AV36
SPI_MOSI_F R329 15R/4 SPI_MOSI P40
SPI_MISO_F R351 15R/4 SPI_MISO R36
SPI_HOLD_F# R341 15R/4 SPI_IO3 U37
SPI_WP_F# R355 15R/4 SPI_IO2 U40
R500 1K/4
R499 1K/4
R353 X_0R/4 PCH_SPI_CS1# R40
SPI_CS# R352 0R/4 PCH_SPI_CS0# R35
SPI_CLK_F R365 15R/4 SPI_CLK_PCH R38
U39
RTCX2 AN39
RTCX1 AN40
RTCRST# AR38
SRTCRST# AR39
PCH_JTAGTCK Y40
PCH_JTAGTMS W40
PCH_JTAGTDO Y38
PCH_JTAGTDI W39
Z87:stuff R509->+12V
H87:stuff R506->ATX_5VSB
Q70:Z87->2N7002, H87->D03-0341409-A68 / D03-0230019-A30
R553&R560&D22 close to PCIE
C436 close to D22 pin5
VBAT
R239 1M/4
JCI1
INTRUDER#
H1X2M_BLACK-RH
N31-1020151-H06
VCC_DDR
R374 1.8K/1%4 0.97V
MEM_PWRGD
C321
R373 3.3K/1%4
X_0.1u16X4
RTC Block
Close to PCH
C365 15p50N6
RTCX2
Y2
R447 10M/6
RTCX1
C364 15p50N6
32.768KMZ12.5p_D-RH
VBAT
R435
SRTCRST#
20K/1%4
C348 1u6.3X6
PCH_VCC3
PCH_GPIO39 R342 10K/4
LPC_DRQ1# R489 X_10K/4
SMBCLK_VCC R525 X_2.7K/4
SMBDATA_VCC R526 X_2.7K/4
FP_RST# R333 10K/4
PCIECLKREQ2# R334 10K/4
[10,29,31] SERIRQ
SERIRQ R570 10K/4
PCH_GPIO38 R571 10K/4
SCLOCK_GPIO22 R576 X_10K/4
PCH_GPIO48 R580 X_10K/4
RN4 8P4R-10KR0402
[10,29] KBRST#
[10,29] A20GATE
output pin
PCH_GPIO32 R321 X_10K/4
PCH_GPIO33 R482 X_10K/4
PCH_GPIO35 R330 X_10K/4
3VSB
PCH_SML1ALERT# R395 10K/4
PCH_SML0ALERT# R477 10K/4
PCH_SMBALERT# R468 10K/4
RI# R479 10K/4
PCH_GPIO13 R386 10K/4
SMLINK0_CLK R478 499R/1%/4
SMLINK0_DATA R485 499R/1%/4
SMLINK1_CLK R476 2.2K/4
SMLINK1_DATA R480 2.2K/4
SUSWARN#_CP R381 X_10K/4
SMBCLK_VSB R484 X_2.7K/4
SMBDATA_VSB R464 X_2.7K/4
PCIECLKREQ5# R438 10K/4
PCIECLKREQ6# R434 10K/4
SB_PME# R443 X_10K/4
PCIECLKREQ4# 1 2
PCIECLKREQ0# 3 4
PCIECLKREQ7# 5 6
PCIECLKREQ3# 7 8
RN7 8P4R-10KR0402
VBAT
PCH_INTVRMEM R452 390K/4
DSPVRMEN R426 390K/4
3VA
SUSACK# CP R391 10K/4
PCH_GPIO31 R453 10K/4
SLP_WLAN# R411 X_10K/4
SB_WAKE# R467 1K/4
PCH_GPIO12 R427 X_10K/4
PCH_GPIO33 R488 0R/4
PCIECLKREQ1# R339 X_10K/4
3VSB R437 4.7K/4 RSMRST#
C347 X_1u6.3X4
R433 X_10K/4
SPI DEBUG PROT
Close to SPI ROM
SPI_VCC3
JSPI1
SPI_MISO_F
SPI_CS#
SPI_SW_SEL
SPI_WP_F#
SPI_MOSI_F
SPI_CLK_F
SPI_HOLD_F#
H2X6[10]M-2PITCH_BLACK-RH-1
+12V
ATX_5VSB
R509
R506 4.7K/4
X_100K/4
Q70
R504 X_0R/4
SPI_CS0#
N-AO3414_SOT23-3-RH
N31-2061341-H06
JTAG PULL HIGH and PULL DOWN
3VSB
R404 200R/4 PCH_JTAGTDO
R390 200R/4 PCH_JTAGTDI
R428 200R/4 PCH_JTAGTMS
R397 100R/4 PCH_JTAGTDO
R382 100R/4 PCH_JTAGTDI
R414 100R/4 PCH_JTAGTMS
R403 51R/4 PCH_JTAGTCK
C385 X_10p50N4 AZ_BITCLK
SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC
+12V
R466 X_10K/4
3VSB
R470 X_10K/4
SMB_EN
Q64
X_2N3904
CHIP_PWGD R493 X_0R/4
Q66 X_2N7002
SMBCLK_VSB R483 0R/4 SMBCLK_VCC
SMBDATA_VSB R463 0R/4 SMBDATA_VCC
Q22
SMB_EN G2
SMBDATA_VSB D1
SMB_EN G1
D2 SMBCLK_VSB
S2 SMBCLK_VCC SMBCLK_VCC [7,33]
S1
X_2N7002D
SMBDATA_VCC SMBDATA_VCC [7,33]
RTC and CLR_CMOS
Clear CMOS
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Clear CMOS
VBAT1 VBAT1 [39]
VBAT
3VA
D11
S-BAT54C-SOT23
JBAT1
H1X2M_BLACK-RH
RTCRST#
R248 20K/1%4
C199 1u6.3X6
C194 1u6.3X6
VBAT1
R251 1K/1%4
BAT1
BAT2P_BLACK-RH-1
N31-1020151-H06
N91-01F0151-L06
Close to PCH
SPI FLASH ROM
Place close to SB.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
SPI1
Z87:M31-25Q6443-W03 64M
H87:M31-2512853-W03 128M
SPI_VCC3
R501 2.2K/4
C410 0.1u10X4
C408 10u6.3X6
SPI_CS0#
SPI_MISO_F
SPI_WP_F#
SPI_HOLD_F#
SPI_CLK_F
SPI_MOSI_F
CS
DO(IO1)
WP(IO2)
GND
VCC
HOLD(IO3)
CLK
DI(IO0)
W25Q128FVSIQ-HF
M31-2512853-W03
MICRO-STAR INT'L CO.,LTD
MS-7823
Size Custom
Document Description LYNX-SMB/LPC/AUDIO/RTC/SPI
Rev 2.0
Date: Friday, January 24, 2014
Sheet 11 of 45

Change to 10UH if
VCCA_DPLLA/VCCA_DPLLB
has noise issue.

AF25 ;AD25 DT CRB0.7 ASW POWER

(Internal) 1.312A+(External)1.38A=2.45A

POWER

VCC3	0.21A
3VA	0.015A
VBAT	6uA
3VSB	0.261A
VCC1_5	0.249A
PCH_1P05	5.921A

PCH_VCC3 HAVE SEQENCING

AG1 DT CRB0.7 VCC3 POWER

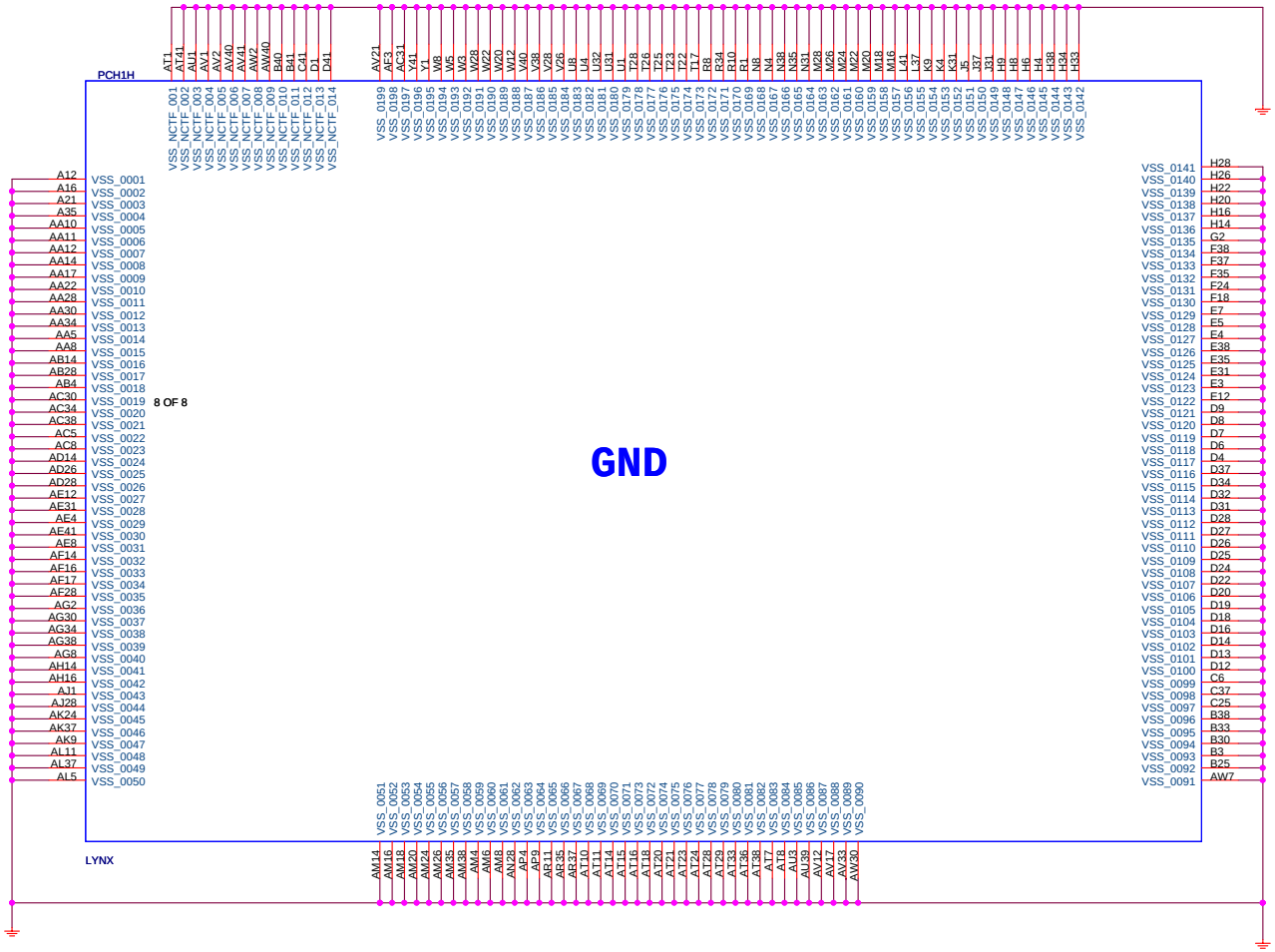
(Internal) 0.261A+(External)0.261A=0.522A

Backside for V14,U12,T16,V16 unstuff

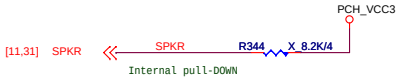
PCH decoupling cap

2013.0514.add C470

MICRO-STAR INT'L CO.,LTD			
MS-7823			
Size: Custom	Document Description: LYNX-POWER		Rev: 2.0
Date: Friday, January 24, 2014		Sheet 12 of 45	

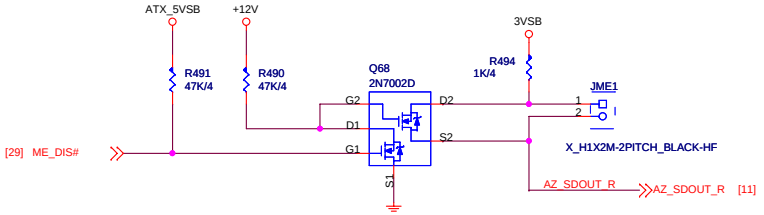


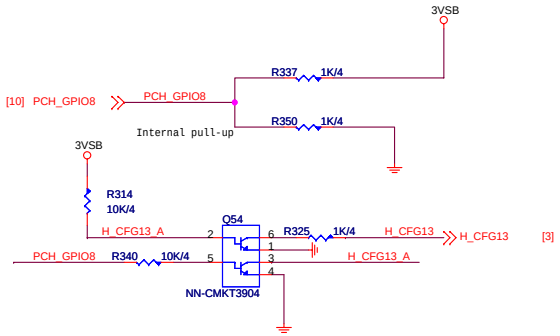
MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: LYNX-GND/NVRAM/USB30	Rev: 2.0
Date: Friday, January 24, 2014	Sheet 13 of 45	



SPKR
Default Mode:
Internal weak Pull-down.

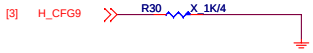
No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



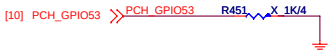


GPIO55
Default Mode:
Internal pull-up.

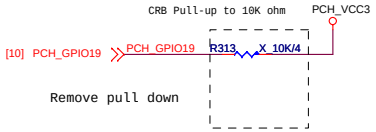
Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



For Sx power Cycling May Fail Due to SVID Logic Race Condition Within the Processor



GPIO53
Connect to ground with 1k Ohm pull-down resistor.



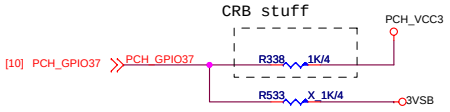
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

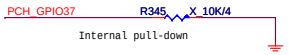
Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default





Enable TLS:
Pull up with 1k Ohm to VccSus3.3.

Default (Disable TLS):
Leave NC. Internal pull down.

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: LYNX-Strap
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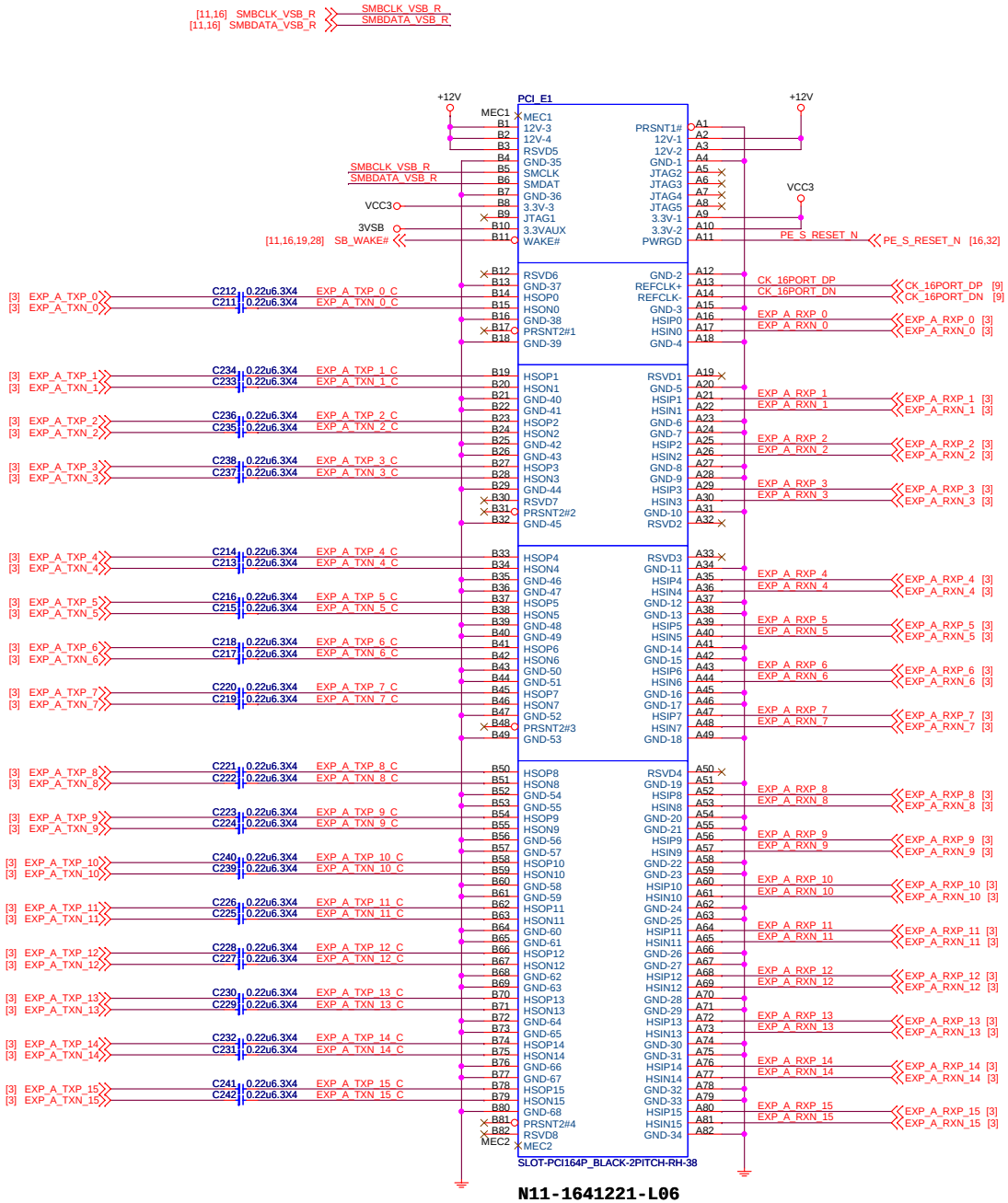

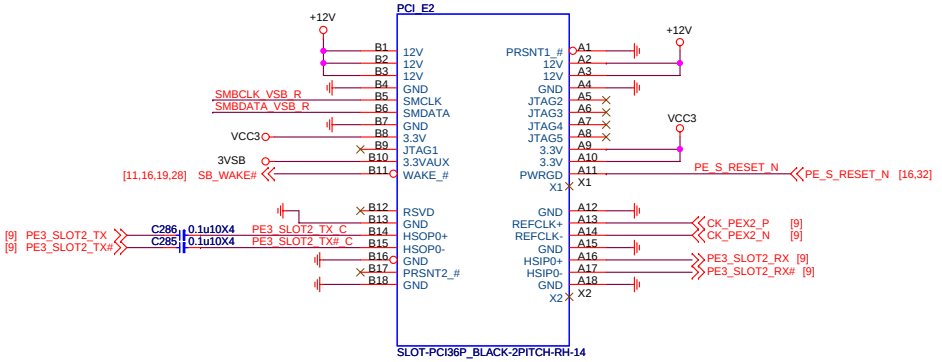

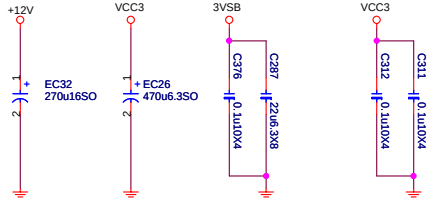

MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: PCIE1(X1) & PCIE2(X16) Slots	Rev: 2.0
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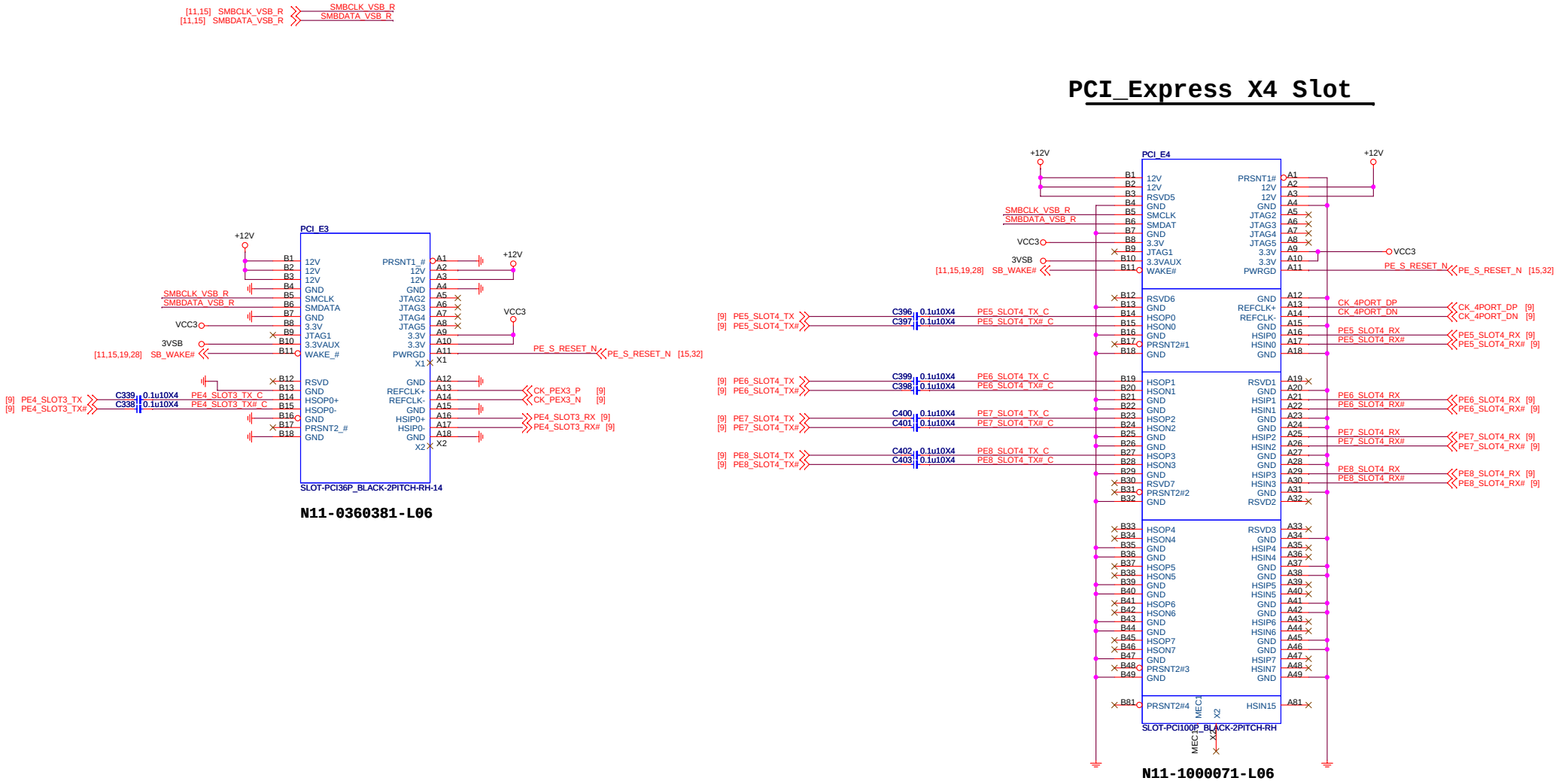
PCI_Express X4 Slot



MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: PCIE3(X1) & PCIE4(X4.) Slots	Rev: 2.0
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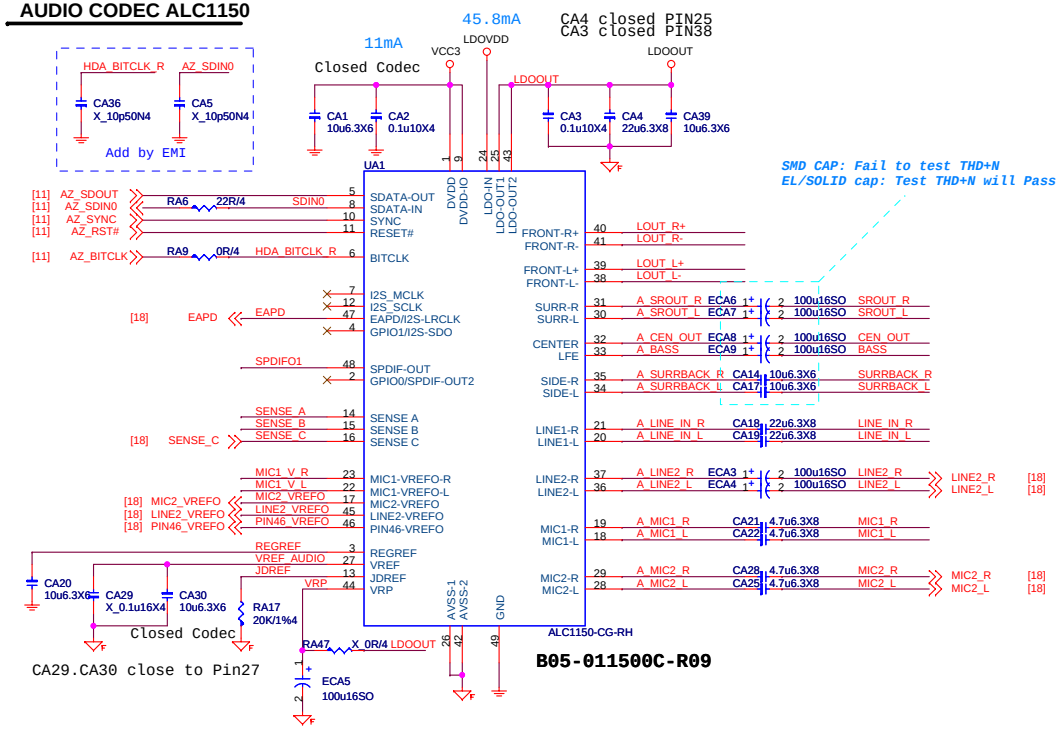
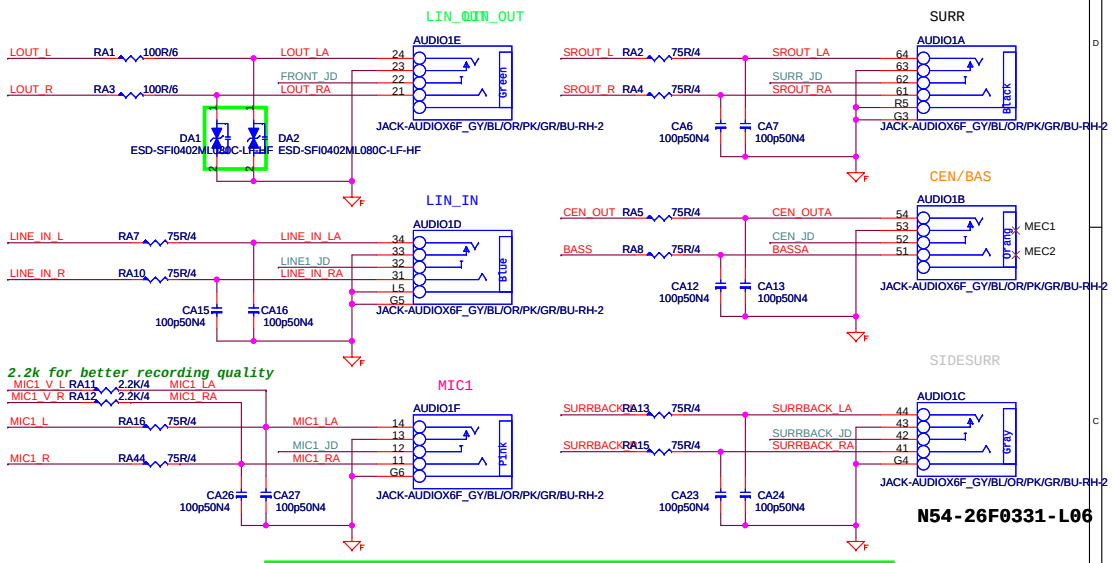
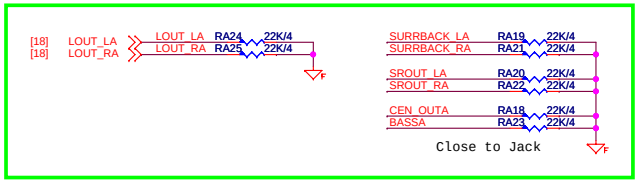
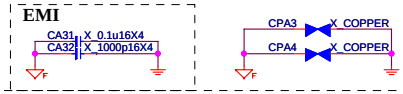
AUDIO CODEC ALC1150

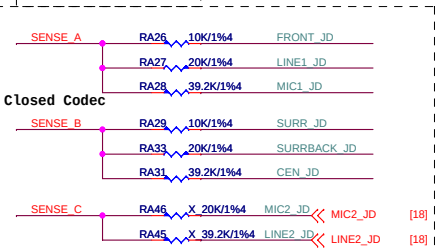


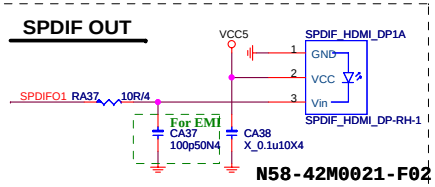
AUDIO Rear I/O

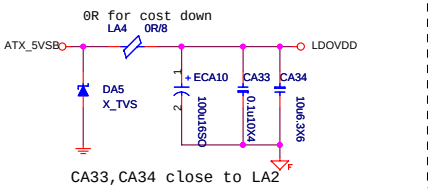


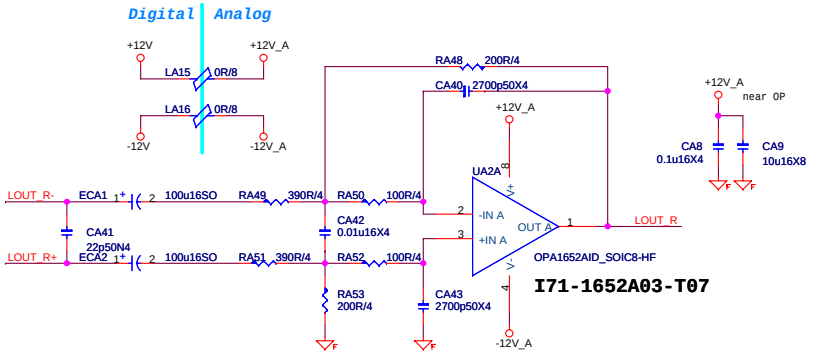


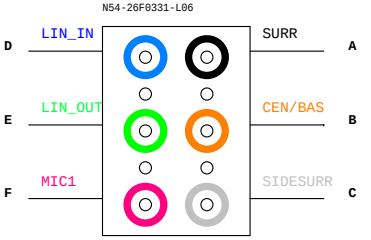












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MS-7823	
Size: Custom	Document Description: Audio Codec ALC892
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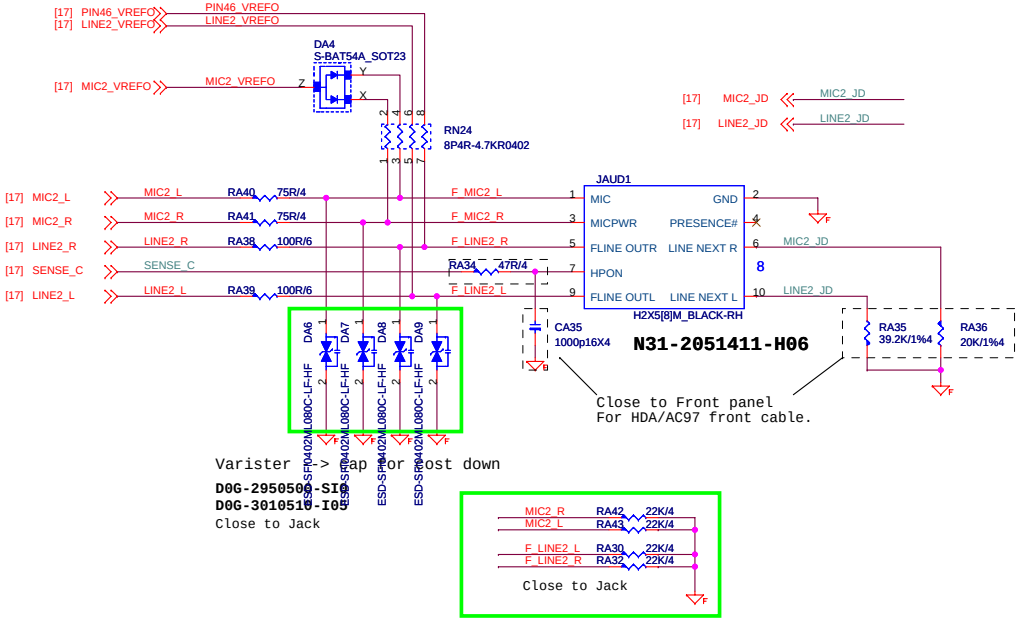
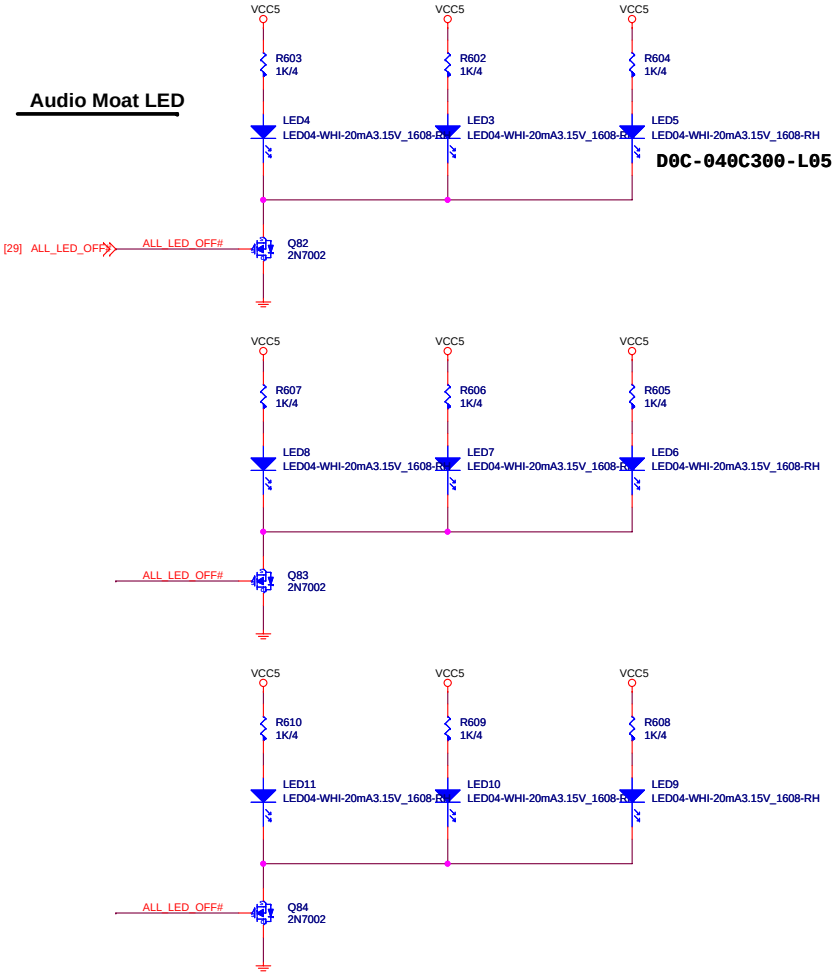
FRONT AUDIO

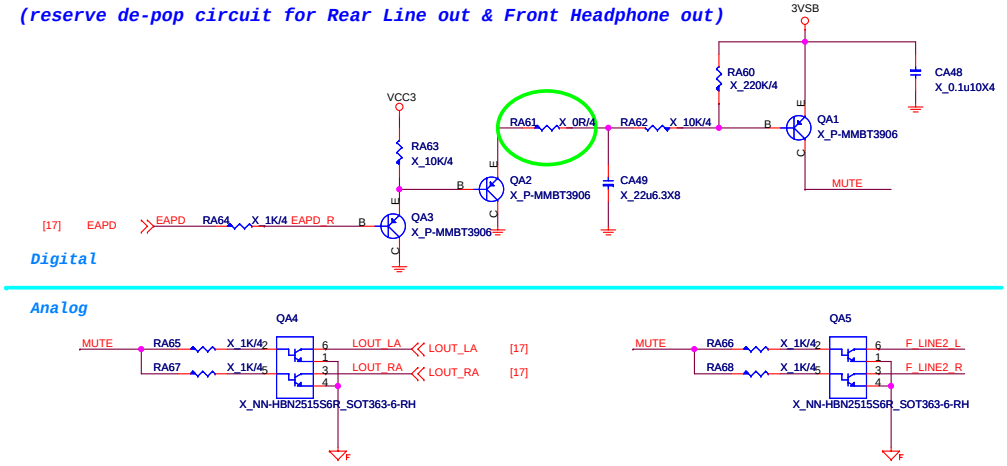


Audio Moat LED

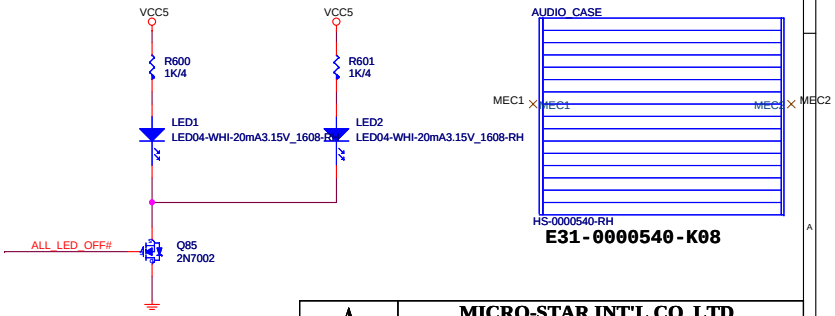


Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)



Audio Heatsink and LED



MICRO-STAR INT'L CO.,LTD		
MS-7823		
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E2205-B Giga LAN

VDD33 RL7 X_10K/4 SB_WAKE#

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).

VDD33 power trace should be wider than 30mils;
AVDD33 power trace should be wider than 30mils;
VDD_IO power trace should be wider than 30mils;
VDDIO_REG power trace should be wider than 20mils;
AVDDH power trace should be wider than 20mils;
AVDDL power traces should be wider than 20mils.
DVDDL power traces should be wider than 20mils.

LED0:
1=hi core voltage(overclocking)
0=low core voltage (non-overclocking)

LED1:
1=SWR mode
0=LDO mode

LED3:
1=25MHz clock
0=48MHz clock

3VSB CPL1 X_COPPER CL22 10u6.3X6 CL23 10u6.3X6 CL3 1u6.3X4 CL10 0.1u10X4 CL12 0.1u10X4
width > 30mil
151.6 mA
VDD33
near Pin52 (<400mil)
Close to Pin52 (<200mil)
Close to Pin24 (<200mil)

VDD33 CPL2 X_COPPER CL34 1u6.3X4 CL35 0.1u10X4
AVDD33
width > 30mil
Close to Pin18

DVDDL CPL3 X_COPPER CL26 1u6.3X4 CL27 0.1u10X4
AVDDL
1.05V~1.33V
width > 20mil
CL28 0.1u10X4
LL1 300L600mA-150-RH
Close to Pin9
Close to Pin21

2.7V
AVDDH CL36 1u6.3X4 CL37 0.1u10X4
Close to Pin12

UL3 E2205-BL3A-R-HF

[9] PE2_LAN_TX / [9] PE2_LAN_TX# — CL14 0.1u10X4 PE2_LAN_TX_C, CL16 0.1u10X4 PE2_LAN_TX#_C — RX_P, RX_N
[9] PE2_LAN_RX / [9] PE2_LAN_RX# — CL18 0.1u10X4 PE2_LAN_RX_C, CL19 0.1u10X4 PE2_LAN_RX#_C — TX_P, TX_N
[9] CK_RTL1_GLAN_DP / [9] CK_RTL1_GLAN_DN — CK_RTL1_GLAN_DP, CK_RTL1_GLAN_DN — REFCLK_P, REFCLK_N
[28,29,31] PLTRST_BU1# / [11,15,16,28] SB_WAKE# — PLTRST_BU1#, SB_WAKE# — PERSTn, WAKEn
VDD33 RL11 4.7K/4 LAN_CLKREQ# — CLKREQn
AVDDH RL12 10K/4 ISOLATn — NC
SPI_CS_LAN — IO14/SPI_CS
SPI_DO_LAN — IO13/SPI_CLK/PPS
VDD33 RL15 4.7K/4 SPI_DI_LAN — IO7/SPI_DO, SPI_DI
CL17 27p50N4 LAN_XTAL1 — XTLI
YL1 25MHZ18P_D-1
LAN_XTAL2 — XTLO
CL15 27p50N4
IO11, IO10, IO9, IO8
VDD33 — VDD33 (24, 52)
AVDD33 — AVDD33 (18)
AVDDH — AVDDH (12)
AVDDH_REG
AVDDL_REG (9, 21)
AVDDL
AVDDVCO (44)
EPAD (53)
VDD_IO (25)
VDDIO_REG (32)
LX (51)
DVDDL_REG (47)

TRXP0 TR_D0+ (14, 15)
TRXP1 TR_D1+ (16, 17)
TRXP2 TR_D2+ (19, 20)
TRXP3 TR_D3+ (22, 23)
TRXN0 TR_D0-
TRXN1 TR_D1-
TRXN2 TR_D2-
TRXN3 TR_D3-

LED[0]/PPS LED0 (48)
LED[1]/PPS LED1 (50)
LED[2]/PPS LED2 (49)
LED[3] LED3 (26) RL14 10K/4 AVDDH
Reserve for strap hi
RL13 X_10K/4 VDD33
RBIAS (13) RBIAS RL16 2.37K/1%/4
IO3, IO2, IO1, IO0, IO4, IO12, IO6, IO5 (33–36, 37–39, 31)
RL17 10K/4, RL18 10K/4, RL19 10K/4, RL20 10K/4 VDDIO_REG
VDDIO_REG

CHOKEL1
L04-47A7310-C08
L04-47A7680-T15
CHOKEL1 CH-4.7u1.7A94mS-RH
LX width > 30mil
DVDDL
Close to CHOKEL1 (<200mil)
CL24 10u6.3X6 CL25 0.1u10X4
CL29 0.1u10X4
Close to Pin47

VDD_IO CL32 1u6.3X4 CL33 0.1u10X4
Close to Pin25

VDDIO_REG CL20 1u6.3X4 CL21 0.1u10X4
Close to Pin32

LL1:
L02-3018023-C08
L02-3018023-T19

9 GND Vias
Close to Pin44

B06-E22050C-Q24

AVDDH RL21 X_10K/4 RL22 10K/4 SPI_CS_LAN
AVDDH RL23 10K/4 RL24 X_10K/4 SPI_DO_LAN

10:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRIO13.

UL2 ESD-ESD3V3U4ULC-RH
TR_D1-, TR_D1+ (1, 2) — TR_D1-, TR_D1+ (10, 9)
TR_D0-, TR_D0+ (4, 5) — TR_D0-, TR_D0+ (7, 6)

UL1 ESD-ESD3V3U4ULC-RH
TR_D3-, TR_D3+ (1, 2) — TR_D3-, TR_D3+ (10, 9)
TR_D2-, TR_D2+ (4, 5) — TR_D2-, TR_D2+ (7, 6)

D0G-05A0300-I14
D0G-06A050C-A68

TCT CL38 0.1u10X4 CL5 0.1u10X4
for EMI
DL1 ESD-VPORT0603102KV05-HF
D0G-1020510-I05
D0G-8010510-SI0

LAN Connector

VDD33 RL10 220R/4 CL1 X_0.1u10X4 for EMI

LED0 RL2 75R/4 CL2 470p50X4
LED1 RL4 220R/4 CL6 470p50X4
LED2 RL3 220R/4 CL7 470p50X4
LED1 low is Orange 1000
LED2 low is Green 100

LAN_USB1B
LED0_A (29) YELLOW+
LED0_ACT (30) YELLOW-
TCT (19) POWER
TR_D0+ (20) TD1+
TR_D0- (21) TD1-
TR_D1+ (22) TD2+
TR_D1- (23) TD2-
TR_D2+ (24) TD3+
TR_D2- (25) TD3-
TR_D3+ (26) TD4+
TR_D3- (27) TD4-
GND (28)
LED1_LINK1000# (31) GREEN+/ORANGE-
LED2_LINK100# (32) GREEN-/ORANGE+
RJ45_USBX2_LEDX2_TX-1000-RH-33
N58-32F0111-U30

MICRO-STAR INT'L CO.,LTD
MS-7815
Size: Custom
Document Description: LAN-Atheros_E2205-B
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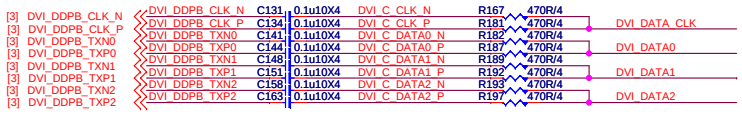
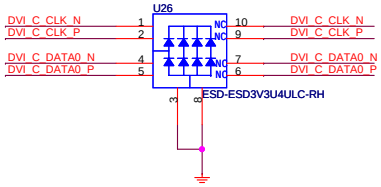
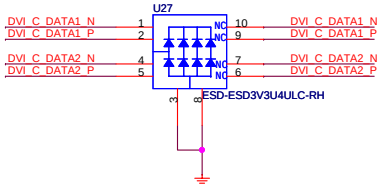
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

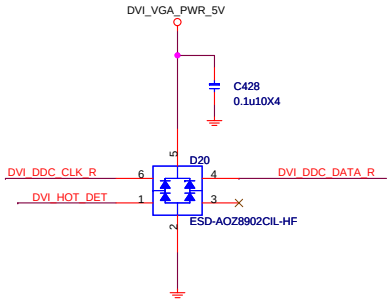


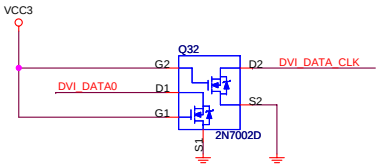
U26 AVL:D0G-05A050C-O05
D0G-06A050C-A68

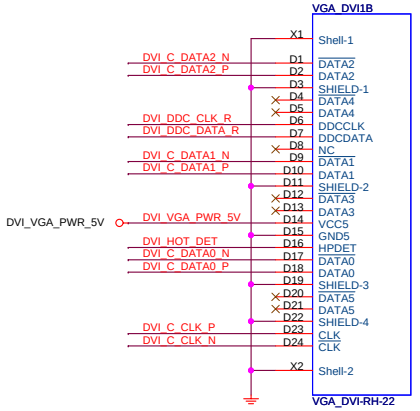


U27 AVL:D0G-05A050C-O05
D0G-06A050C-A68

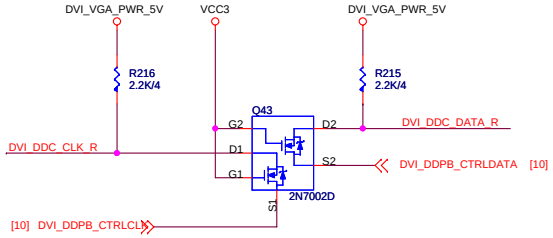


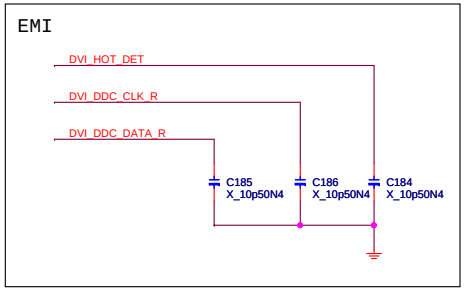


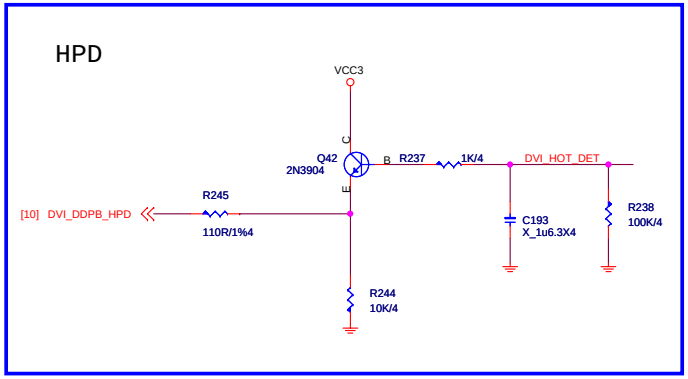


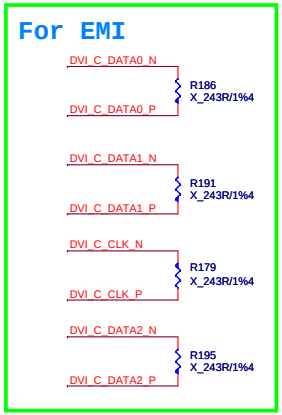


N58-39F0281-C67









MICRO-STAR INT'L CO.,LTD

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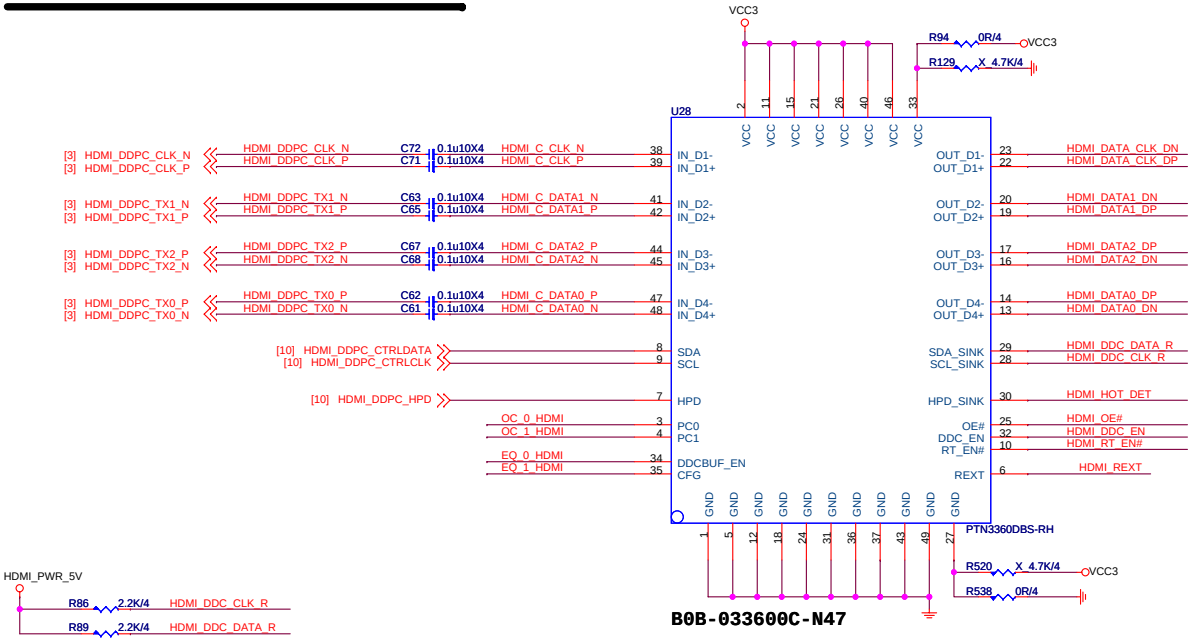
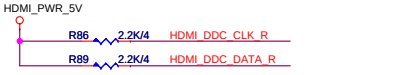
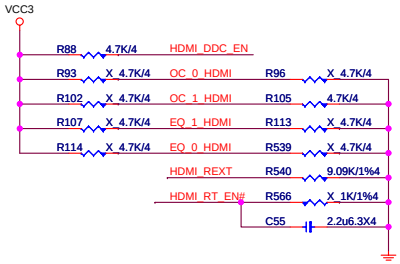
HDMI level shifter

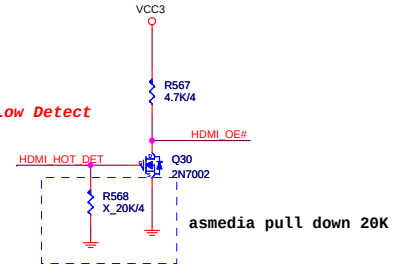


B0B-033600C-N47





注意High/Low Detect



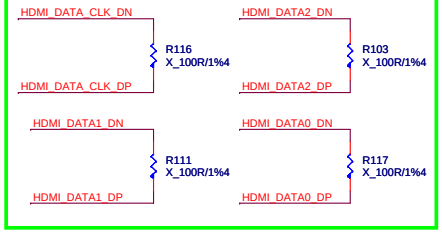
asmedia pull down 20K

	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	

For EMI



EMI

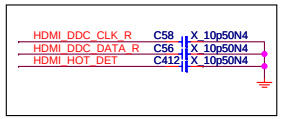
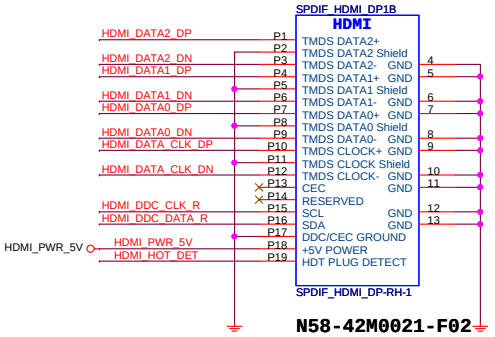
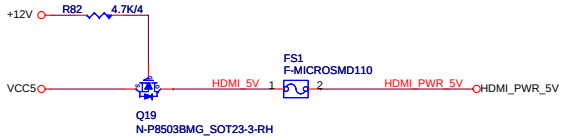


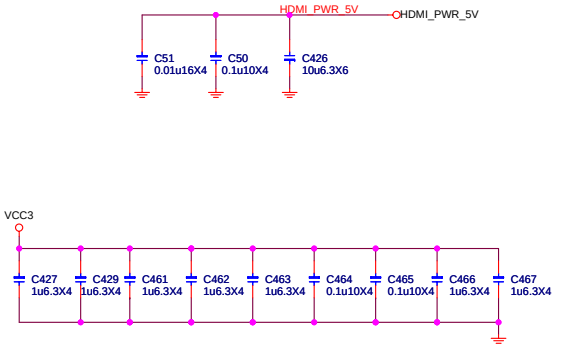
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	



N58-42M0021-F02





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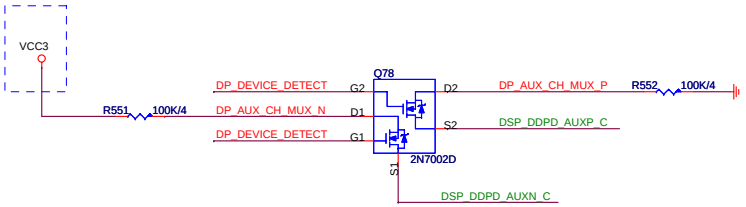
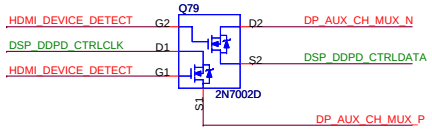
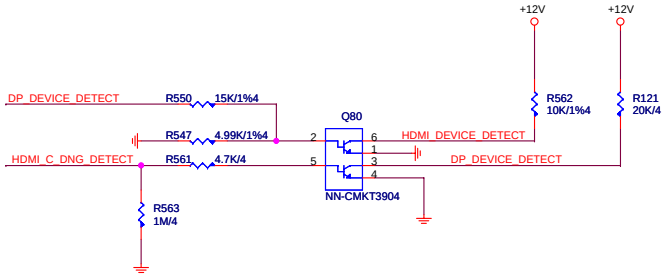
DP

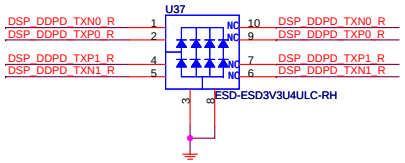




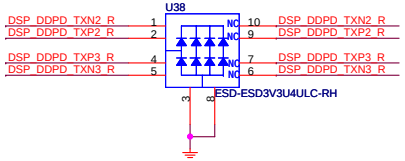


	DP	HDMI
HDMI_C_DNG_DETECT	L	H
DP_DEVICE_DETECT	H	L
HDMI_DEVICE_DETECT	L	H

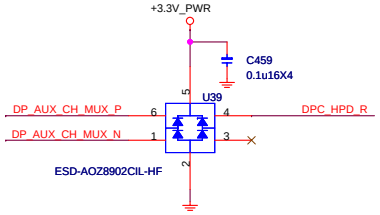
U76 AVL:D0G-06A050C-A68

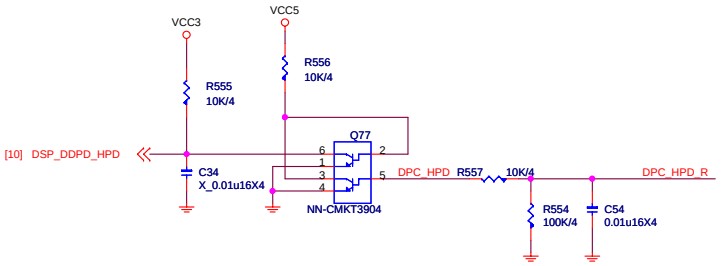


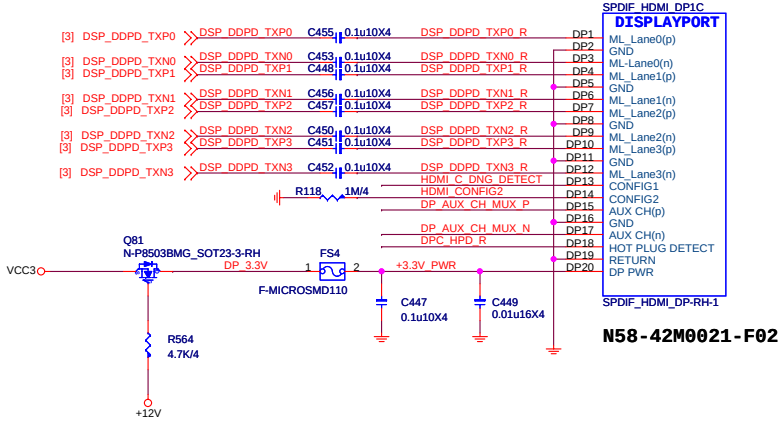
U77 AVL:D0G-06A050C-A68



U2 AVL:D0G-0100619-I05







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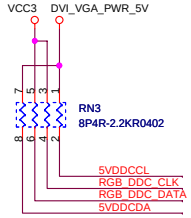
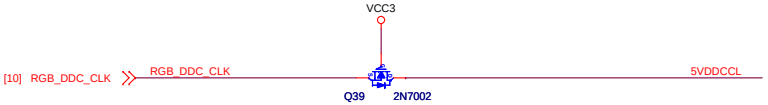
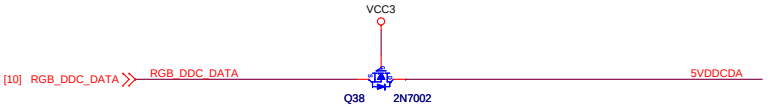
D-Sub

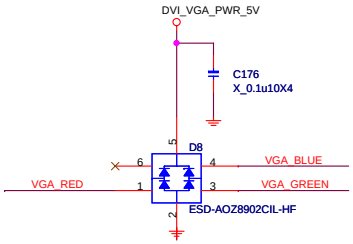
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

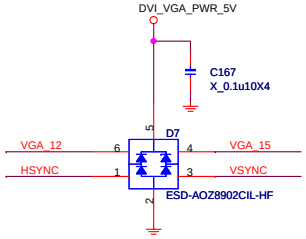
Level shift

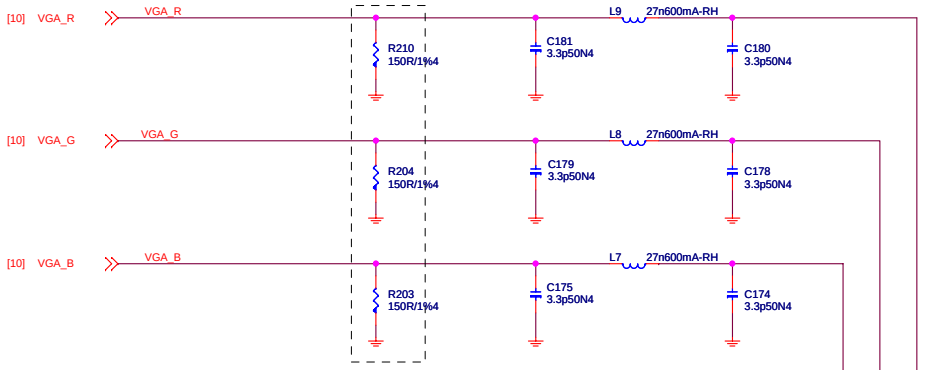




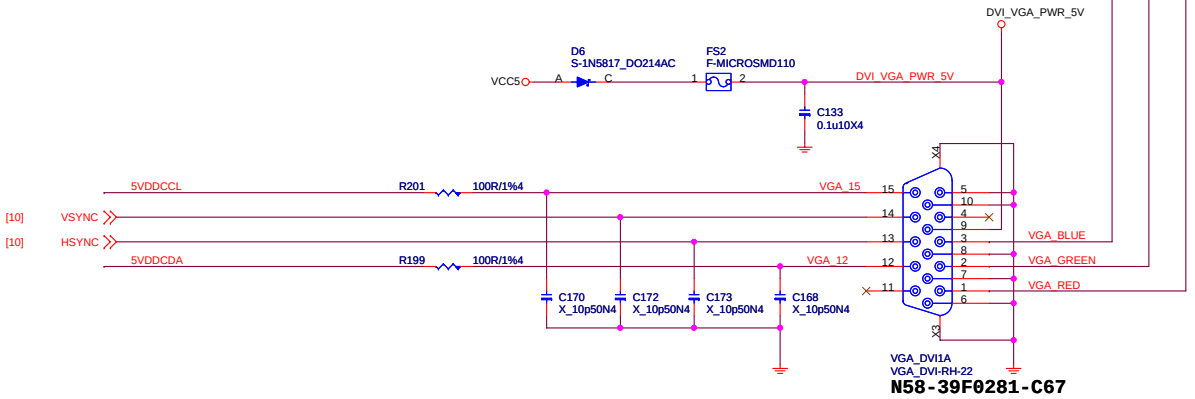








PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



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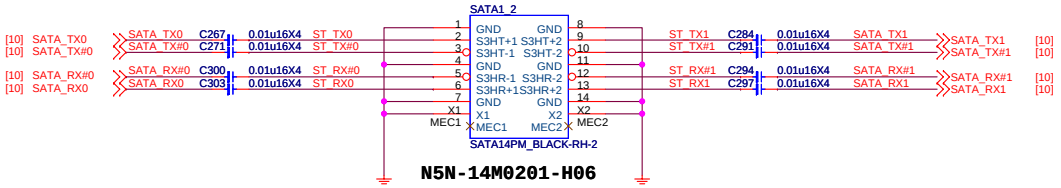
SATA 6G PORT 0,1

3.0 Black

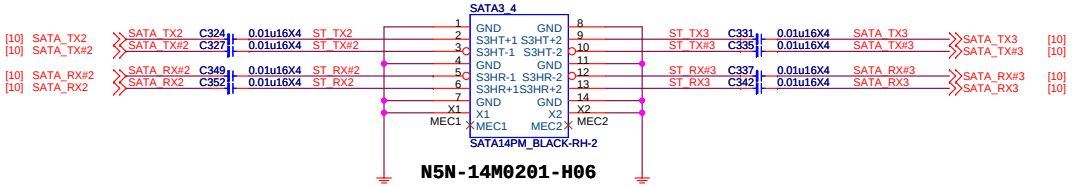


N5N-14M0201-H06

SATA 3G PORT 2,3

3.0 Black

B85 chip support SATA3.0
H81 can't support



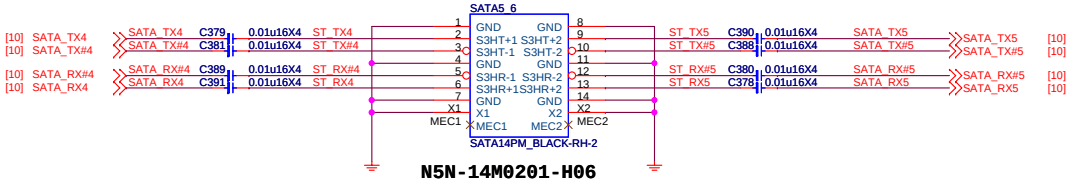
N5N-14M0201-H06

Change 90 by PM

SATA 3G PORT 4,5

3.0 Black

Z87, H87 chip support SATA3.0
B85, H81 chip support SATA2.0



N5N-14M0201-H06

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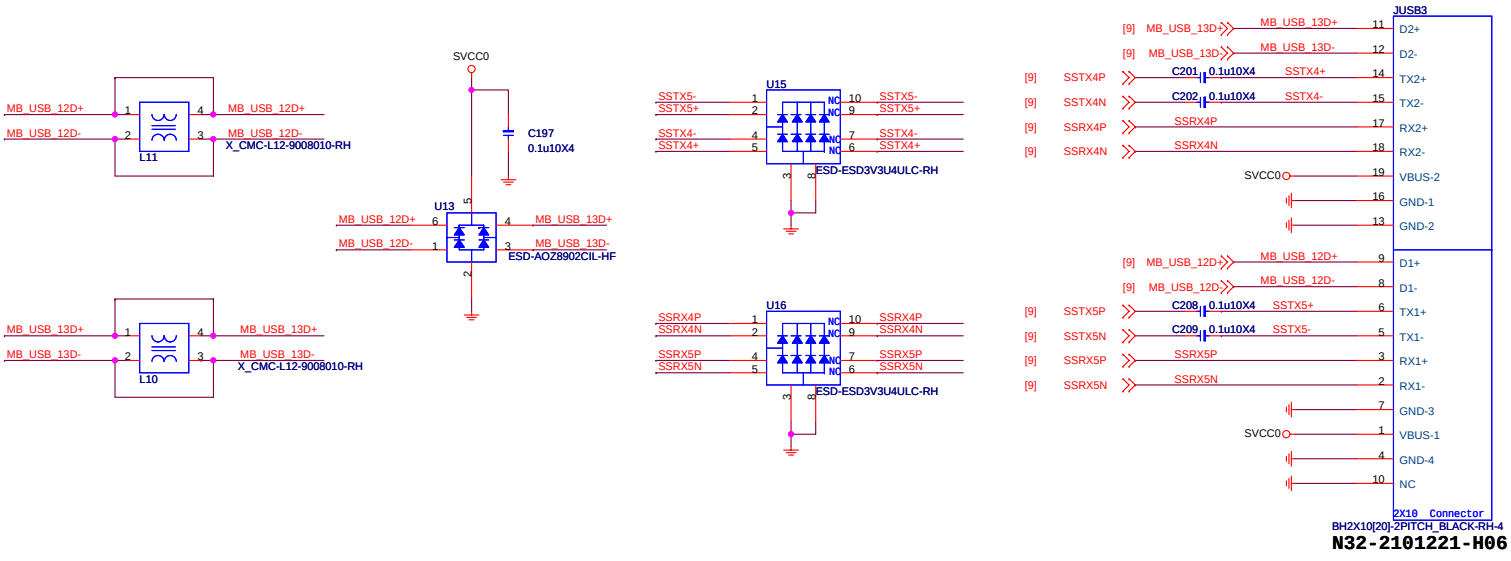
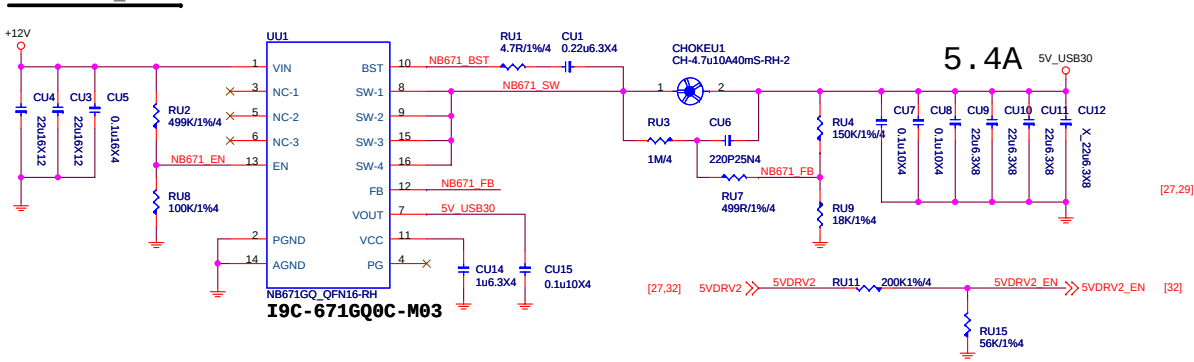
Front JUSB3 for B85

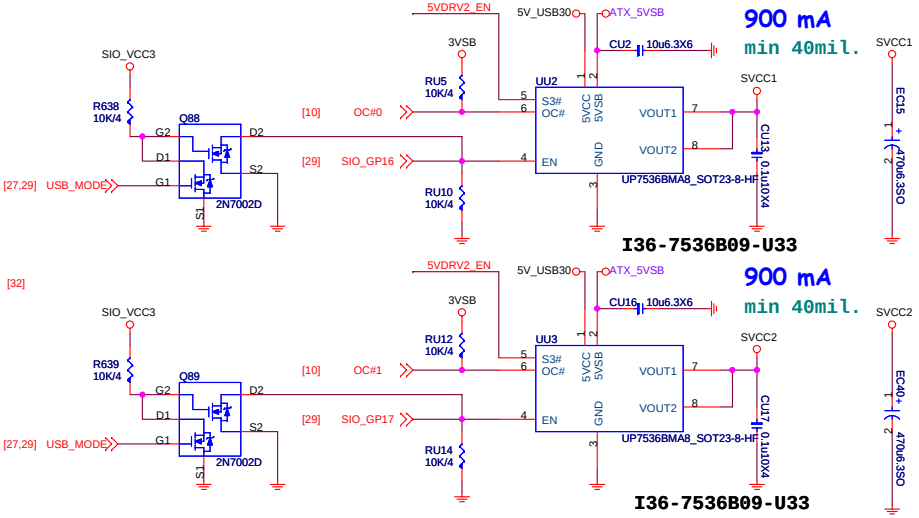


N32-2101221-H06

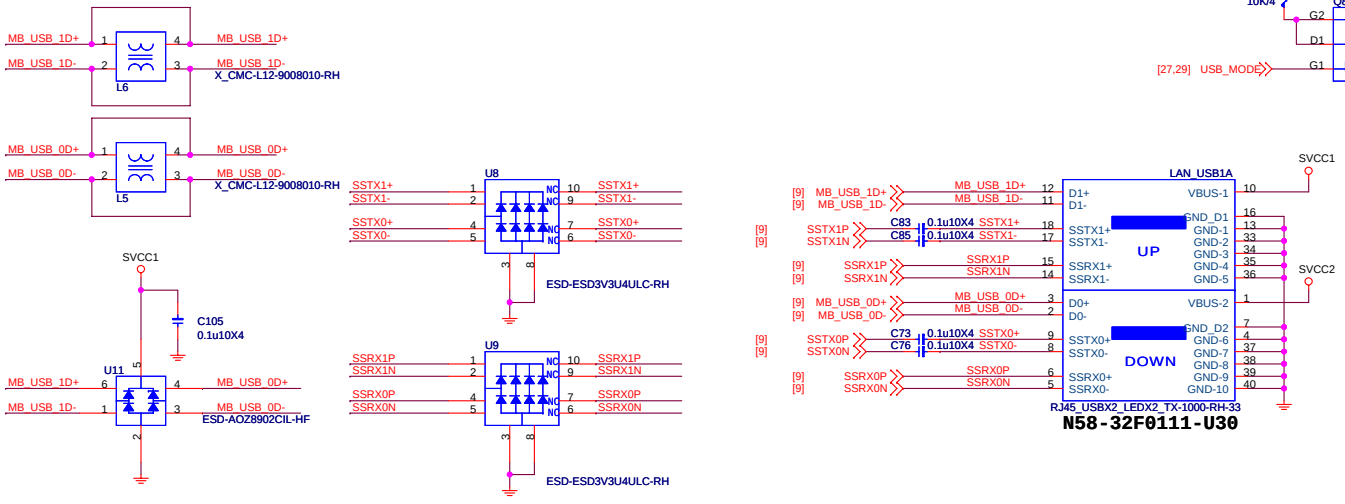
Rear LAN_USB1



I9C-671GQ0C-M03



I36-7536B09-U33



N58-32F0111-U30

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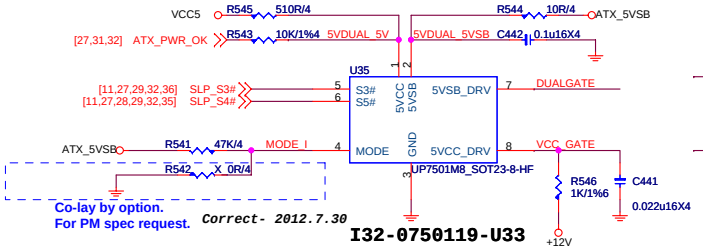
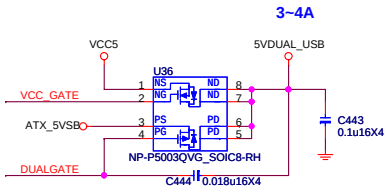
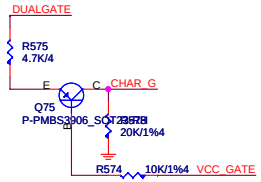
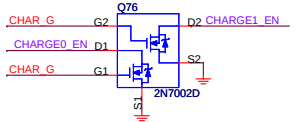
5VDUAL_USB - uP7501



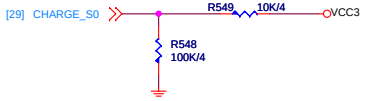




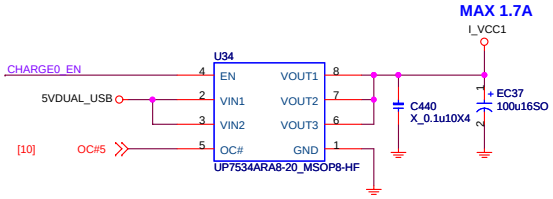


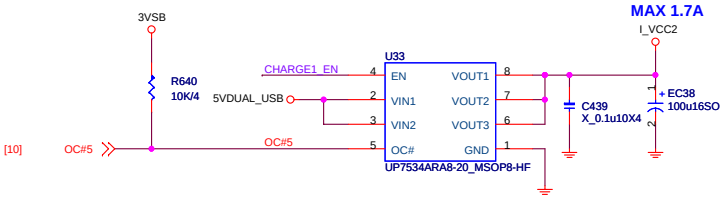
F71868 GPIO12

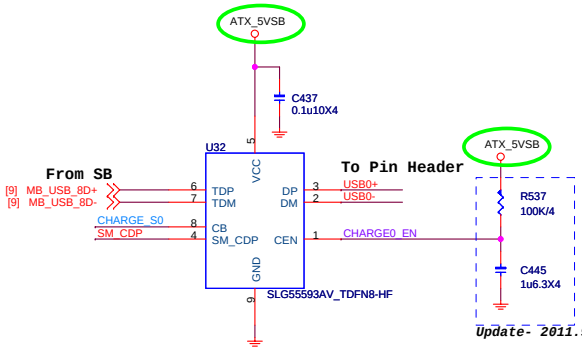
NCT6779D GPIO24
F71889 GPIO25

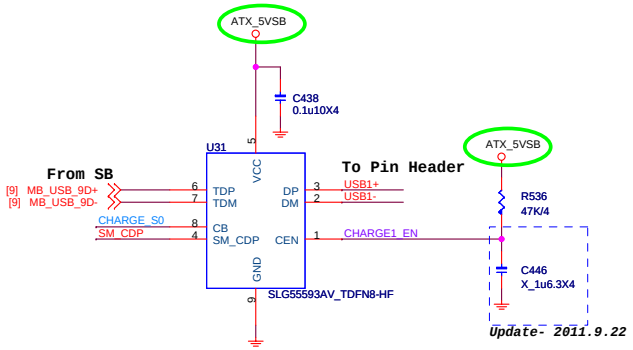


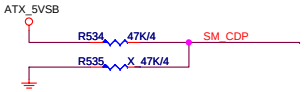
USB Charging POWER For JUSB1



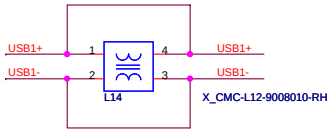


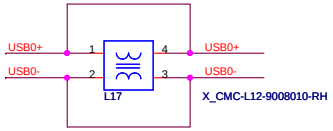




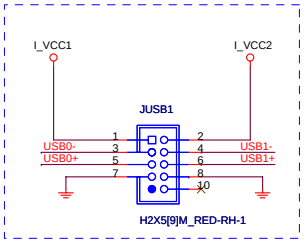


FRONT JUSB1





SLG55583A has internal ESD diode.



Please name the pin header JUSB1.

N31-2051B01-H06

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USB POWER

2013.03.14 update

VCC5 R514 510R/4 R119 10R/4 ATX_5VSB
[26,31,32] ATX_PWR_OK R100 10K/4 5VUSB_5V 5VUSB_5VSB C59 0.1u10X4
U30
[11,26,29,32,36] SLP_S3#
[11,26,28,29,32,35] SLP_S4#
S3# S5# 5VCC 5VSB GND 5VSB_DRV 5VCC_DRV MODE
5VSBDRV2
[25,29] USB_MODE
5VDRV2 5VDRV2
UP7501M8_SOT23-8-HF
R516 1K/1%6 C70 0.022u16X4 +12V

TO:NCT6779 GP72

H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

I32-0750119-U33

ATX_5VSB Q73 P-P06P03LCGA_SOT89-3-HF 5V_FUSB
5VSBDRV2 C422 X_18n16X4 5V_FUSB F4 F-SMD1812P260TFT-HF 5V_FUSB1
5VDRV2 Q72 F3 F-SMD1812P260TFT-HF SVCC0
N-NTMFS4C05NT1G_SO8-HF
VCC5 [25,32]

ATX_5VSB Q28 P-P06P03LCGA_SOT89-3-HF 5V_RUSB
5VSBDRV2 C69 X_18n16X4 5V_RUSB F1 F-SMD1812P260TFT-HF 5V_RUSB1
5VDRV2 Q24
N-NTMFS4C05NT1G_SO8-HF
VCC5

D03-06P0319-N03
D03-4C05N03-005

5V_FUSB1 EC35 470u6.3SO
SVCC0 EC28 470u6.3SO
5V_FUSB1 C413 0.1u10X4
C413 near D19 Pin5
5V_FUSB1 R581 10K/1%4 [10] OC#4 R585 15K/1%4
SVCC0 R582 10K/1%4 OC#6 R586 15K/1%4

5V_RUSB1 EC5 470u6.3SO
5V_RUSB1 C60 0.1u10X4 C43 0.1u10X4
C60&C43 near D3&D2 Pin5
5V_RUSB1 R636 10K/1%4 [10] OC#2 R637 15K/1%4

5VDRV1, 5VSBDRV1 width 12mil
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 2 USB ports

REAR USB PORT 2,3 for PS2_USB1

[9] MB_USB_3D- MB_USB_3D-
[9] MB_USB_3D+ MB_USB_3D+
L4 X_CMC-L12-9008010-RH
[9] MB_USB_2D- MB_USB_2D-
[9] MB_USB_2D+ MB_USB_2D+
L3 X_CMC-L12-9008010-RH

5V_RUSB1
D3
MB_USB_3D- MB_USB_2D-
MB_USB_3D+ MB_USB_2D+
ESD-AOZ8902CIL-HF
NEAR CONNECTOR

5V_RUSB1
PS2_USB1B
MB_USB_2D- MB_USB_2D+ VCC-1 USB2- USB2+ GND-1
MB_USB_3D- MB_USB_3D+ VCC-2 USB1- USB1+ GND-2
MINIDIN_USBX2-RH-4

N58-14M0171-L06

REAR USB PORT 4,5 for USB1

[9] MB_USB_5D- MB_USB_5D-
[9] MB_USB_5D+ MB_USB_5D+
L1 X_CMC-L12-9008010-RH
[9] MB_USB_4D- MB_USB_4D-
[9] MB_USB_4D+ MB_USB_4D+
L2 X_CMC-L12-9008010-RH

5V_RUSB1
D2
MB_USB_4D- MB_USB_5D-
MB_USB_4D+ MB_USB_5D+
ESD-AOZ8902CIL-HF
NEAR CONNECTOR

5V_RUSB1
USB1
MB_USB_5D- MB_USB_5D+ MB_USB_4D- MB_USB_4D+
UP DOWN
USBAX2M_BLACK-RH-21

N53-08M0421-H06

FRONT USB PORT 10,11 for JUSB2

[9] MB_USB_10D- MB_USB_10D-
[9] MB_USB_10D+ MB_USB_10D+
L13 X_CMC-L12-9008010-RH
[9] MB_USB_11D- MB_USB_11D-
[9] MB_USB_11D+ MB_USB_11D+
L16 X_CMC-L12-9008010-RH

5V_FUSB1
D19
MB_USB_11D- MB_USB_10D-
MB_USB_11D+ MB_USB_10D+
ESD-AOZ8902CIL-HF
NEAR CONNECTOR

5V_FUSB1
JUSB2
MB_USB_11D- MB_USB_10D-
MB_USB_11D+ MB_USB_10D+
H2X5[9]M_BLACK-RH-3

N31-2051BG1-H06

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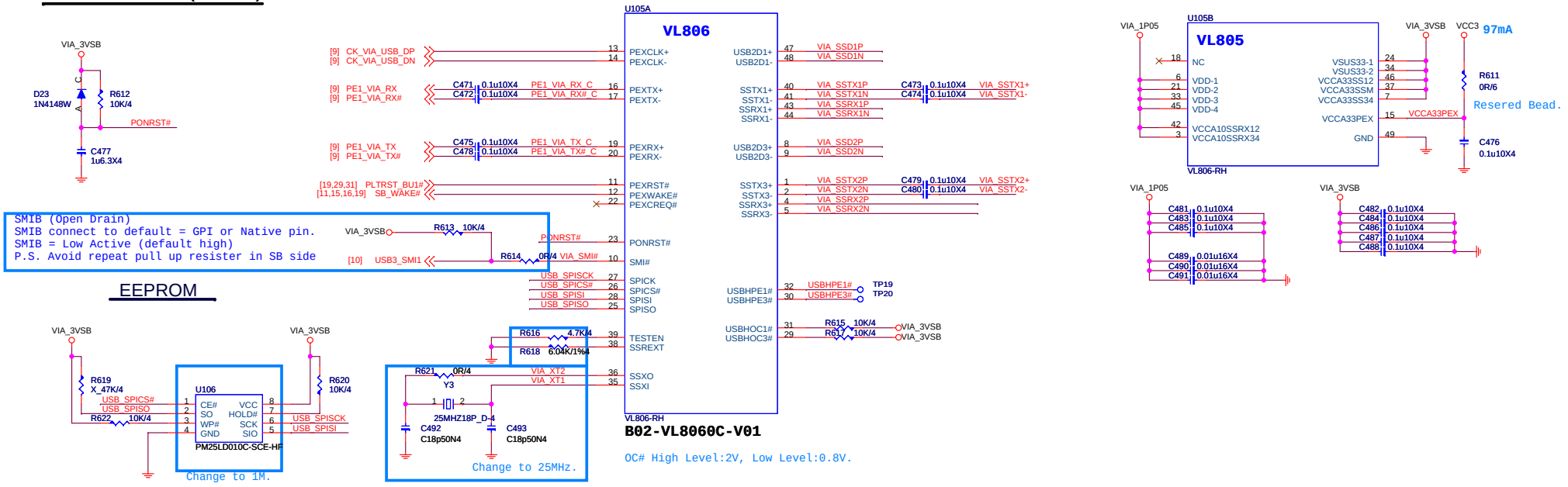
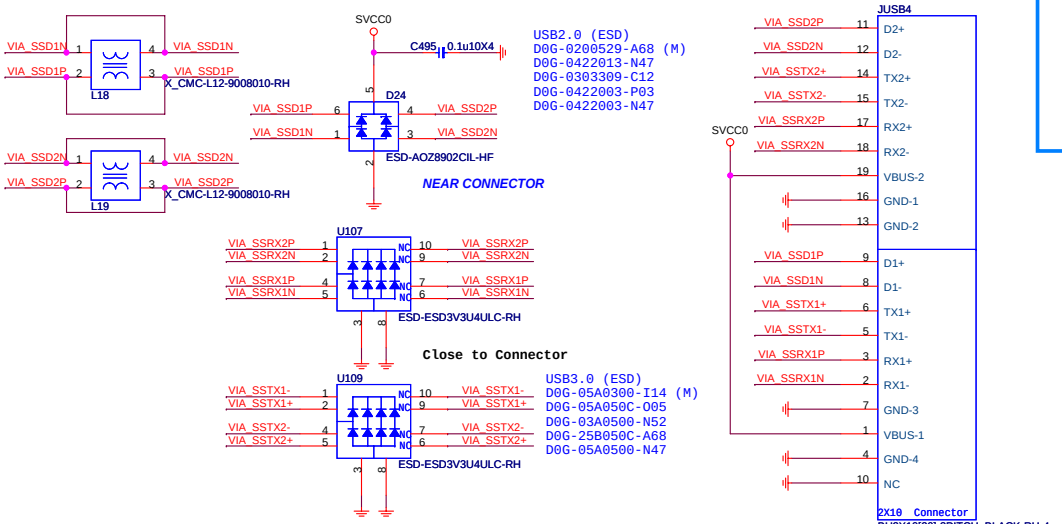
VIA VL806 USB3.0 (for H81)



B02-VL8060C-V01

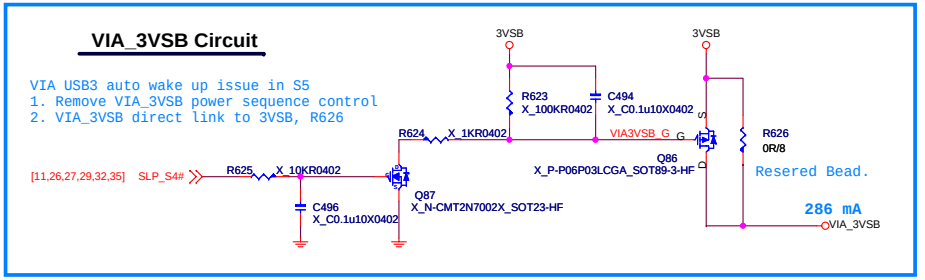
M31-2501073-P81

VIA USB3.0 for JUSB4



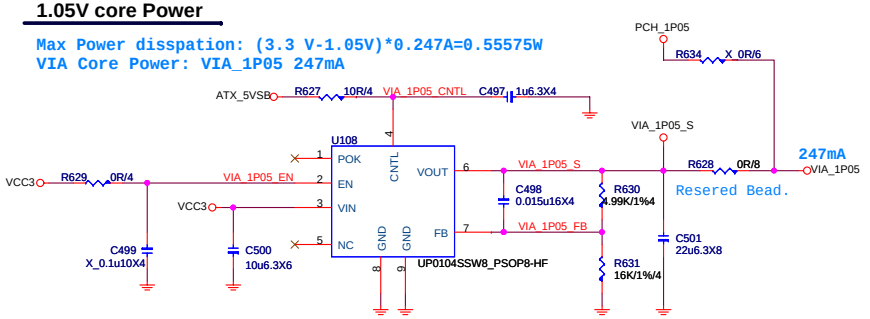
N32-2101221-H06

VIA_3VSB Circuit



1.05V core Power

Max Power disspation: (3.3 V-1.05V)*0.247A=0.55575W
VIA Core Power: VIA_1P05 247mA



I31-P010402-U33

MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: VIA VL806 USB3.0	Rev: 2.0
Date: Friday, January 24, 2014	Sheet 28 of 45	

SUPER I/O NCT6779D

U19

LPC Interface
GPIO
Printer mode
Port80
LED Control
DSW Interface
GPIO
AMD used TSIC/D but intel used GPIO
UART SIR
Harddware Monitor
KBC Function
FAN Control
ACPI Function
Power Pin

If un-used input pin please add pull down

PLTRST_BUS1,2,3
connect to slot or device

NCT6779D-RH-1

B02-6779D24-N62

GPIO 41, 46, 31 and 32 that Support Wake-Up Function

FOR BIOS USED

SERIAL PORT 1

NO USE UART PORT1

都當GPIO
沒用的GPIO PIN 請PULL DOWN FOR SIO POWER CONSUMPTION

GP73 BIOS要PO成WDT# FUNCTION

GD75232DBR_SSOP20-RH

I95-7523212-T07

JCOM1

N31-2051331-H06

X_470p50X/8P4C

X_470p50X/8P4C

PS2 KEYBOARD & MOUSE CONNECTOR

MINIDIN_USBX2-RH-4

N58-14M0171-L06

ESD-AOZ8902CIL-HF

3V Analog Power

X_120L600mA-250

Closed PIN99

Closed PIN46,85

Closed PIN24,108

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable

HW Monitor - Voltage

VCCP	R276 10K/1%4	CPUVcore	R279 10K/1%4, C268 10u6.3X6
+12V	R291 200K/1%4	VIN0	R287 20K/1%4, C263 0.1u16X4
VCC5	R290 12K/1%4	VIN1	R286 3K/1%4, C262 0.1u10X4
CPU_VTT	R280 10K/1%4	VIN2	C272 10u6.3X6
VCC_DDR	R272 10K/1%4	VDIMM	Q50 2N7002, R273 10K/1%4, C257 10u6.3X6
PCH_1P05	R285 10K/1%4	VIN4	C282 10u6.3X6
CPU_CORE0	R283 10K/1%4	VIN5	C281 10u6.3X6
CPU_GFX	R282 10K/1%4	VIN6	C280 10u6.3X6
CPU_RING	R281 10K/1%4	VIN7	C279 10u6.3X6
CPU_SA	R298 10K/1%4	VIN8	C293 10u6.3X6

LPC_FRAME#	R385 X_4.7K/4		
LPC_DRQ#0	R371 X_4.7K/4		
PLTRST_BU1# R	R368 820R/4		
CHIP_PWGD	R359 1K/4		
	R358 X_100K/4		
FP_RST# I	R349 4.7K/4		
PLTRST#	R384 X_4.7K/4		
PECI_IO	C266 X_47p50N4		
	R289 X_1K/4		
SIO_5VDUAL	R312 1K/4		
SYSFANIN	R310 1K/4		
AUXFANIN2	R309 1K/4		
ALL_LED_OFF#	R588 1K/4		
TURBO_MODE#	R20 1K/4		
CPUTIN	R284 1K/4		
USB_MODE	R431 10K/4		

HM_VREF	R278 X_10K/1%4		
SYSTIN			
Q51 P-PMBS3906_SOT23-RH	R273	RT3	C289 2200P50X4
		X_10KRT1%	
		GNDHM	

SYS3VSB_OFF	R328 10K/4		
SKTOCC# R	R297 X_2M/4	VBAT	
	R299 1K/4		

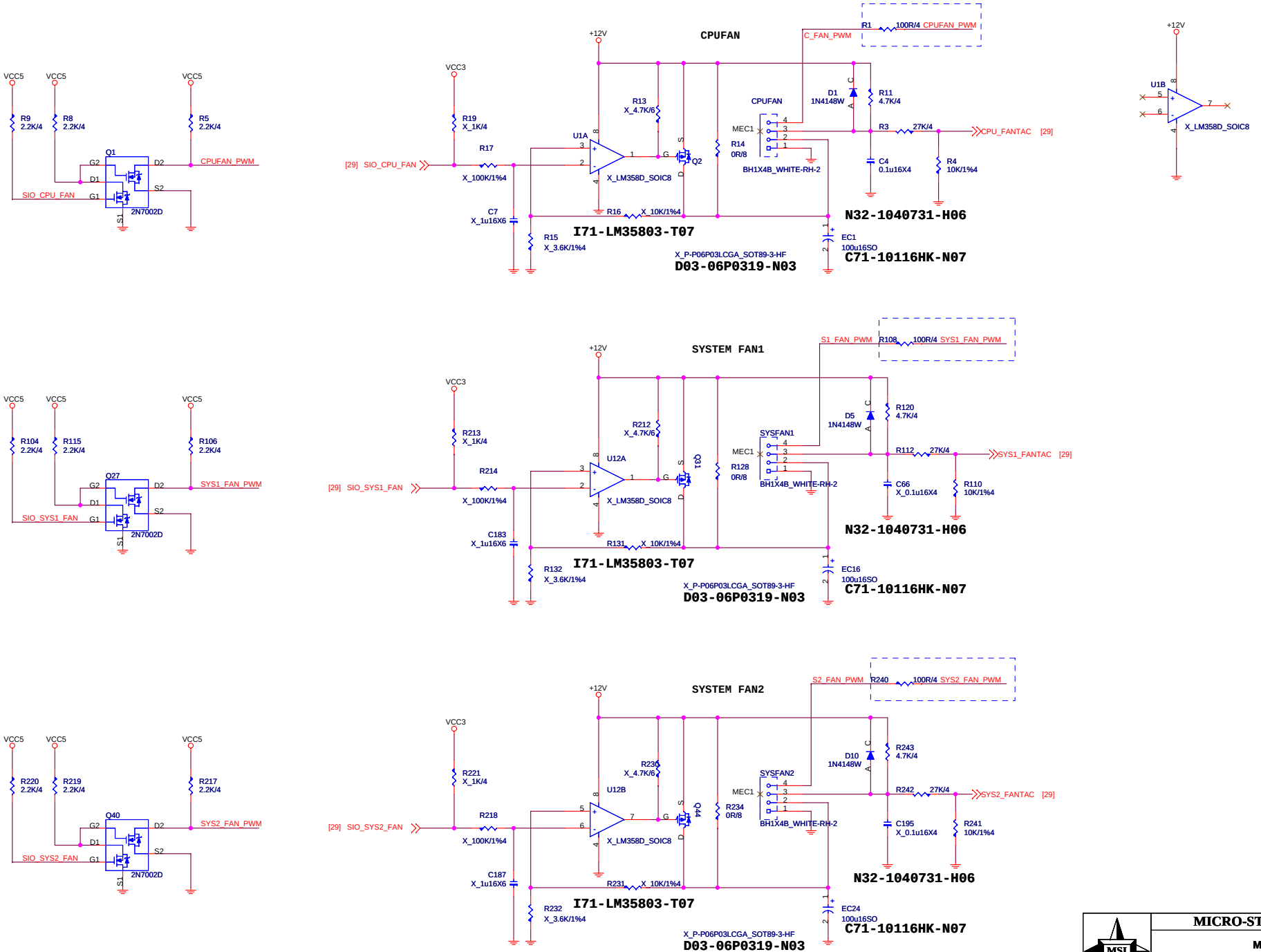
MICRO-STAR INT'L CO.,LTD

MS-7823

Size	Document Description	Rev
Custom	SIO-NTC6779D/PS2	2.0

Date: Friday, January 24, 2014 Sheet 29 of 45

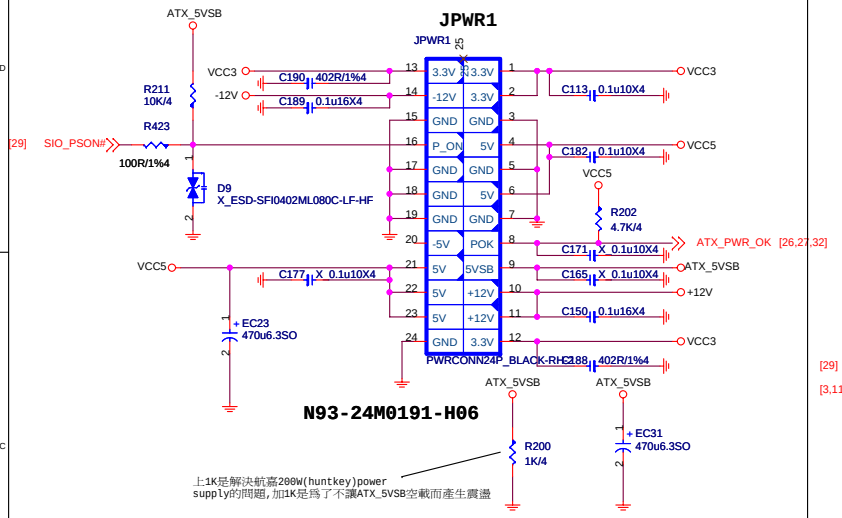
FAN-COUNTROL CIRCUIT



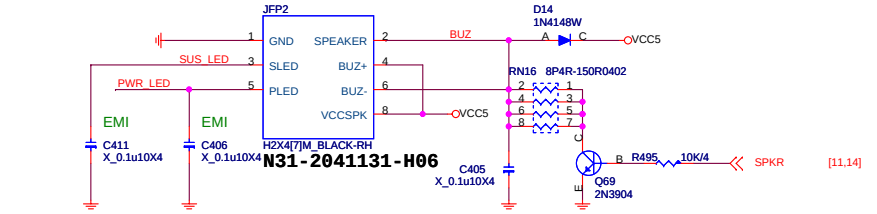
MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: FAN Control	Rev: 2.0
Date: Friday, January 24, 2014	Sheet 30 of 45	

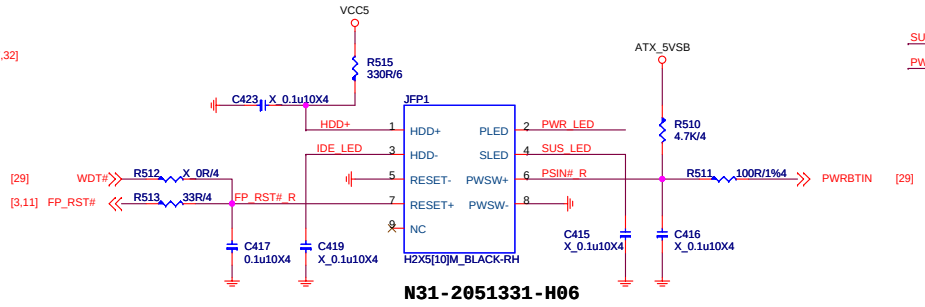
ATX POWER CONNECTOR

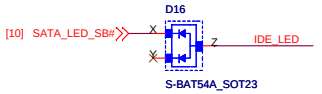
C188&C190 stuff 402 ohm for DVI leakage issue



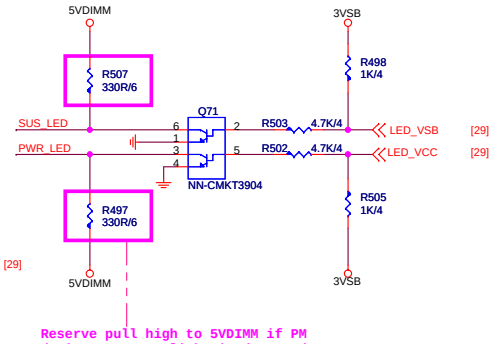
FRONT PANNEL



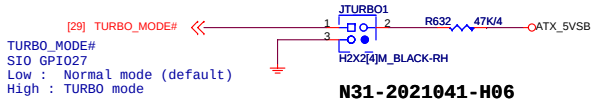


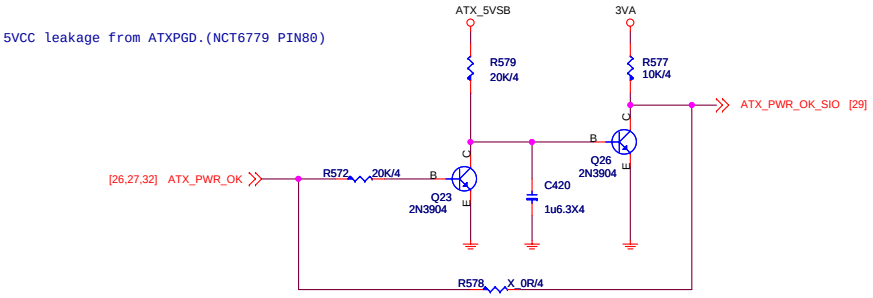


LED (for Fintek 71869)

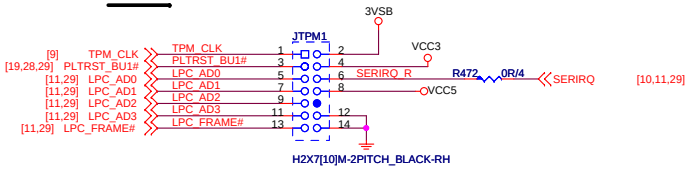


OC GENIE



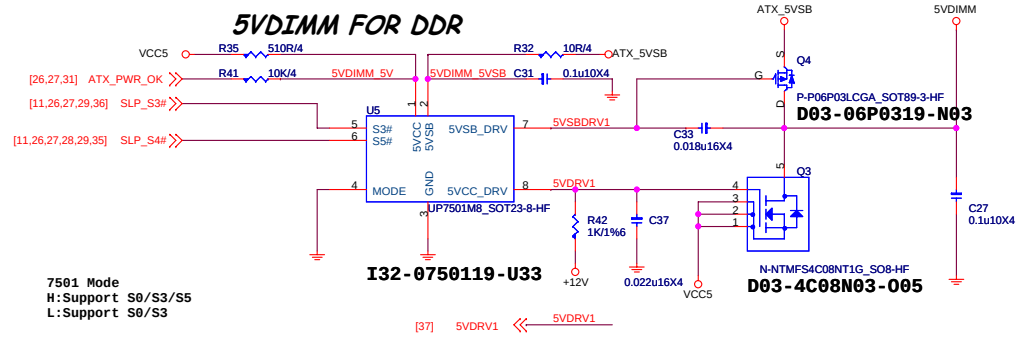


TPM



MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: ATX F_Panel/EMI/TPM
Rev: 2.0	
Date: Friday, January 24, 2014	Sheet 31 of 45

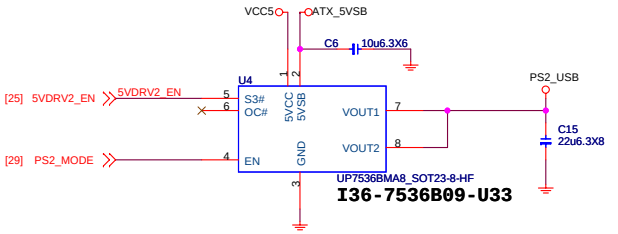
5VDIMM FOR DDR



I32-0750119-U33

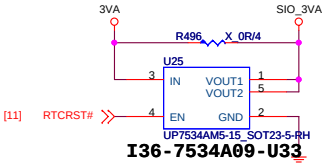
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

PS2 Power



I36-7536B09-U33

隔離PCH&SIO的3VA

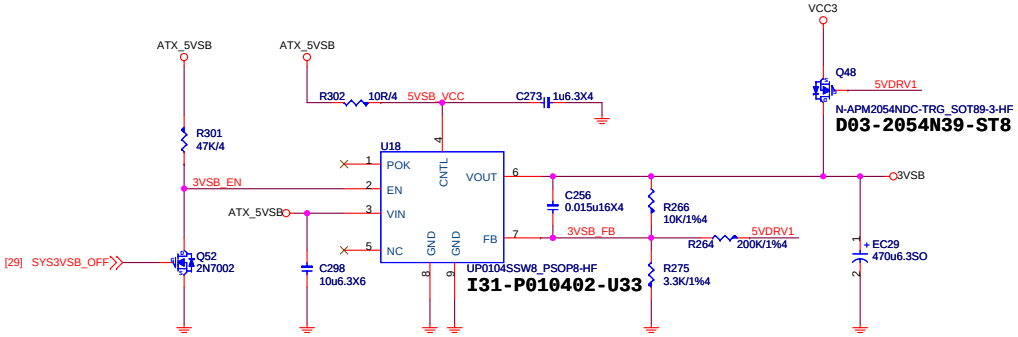


I36-7534A09-U33

3VSB

0.216+0.2+1.5+0.67=2.586A
PCH:216mA
LAN:200mA
PCIE Slot:375mA x4
up0104 ME Power:0.67A

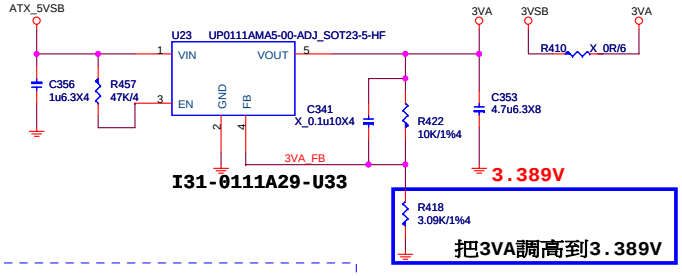
Q48 AVL:D03-3057L19-N03



I31-P010402-U33

3VA

20mA

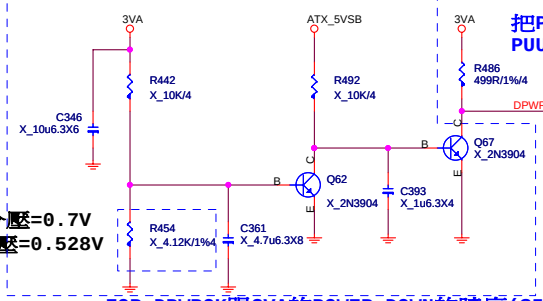


I31-0111A29-U33

3.389V

把3VA調高到3.389V

for NCT6779 Ver.C not stuff

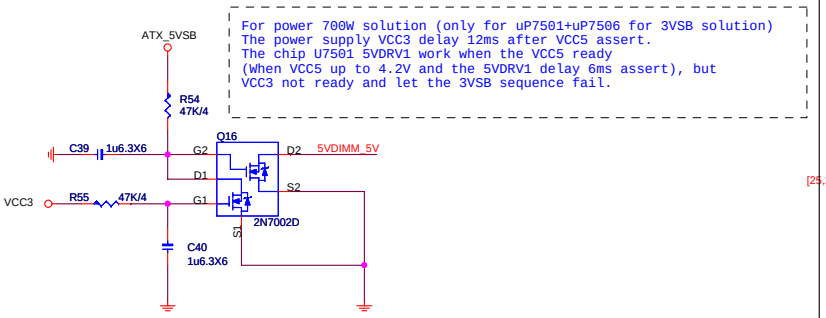


把PCH DPWRROK_CP的
PUULL HIGH移到這裡

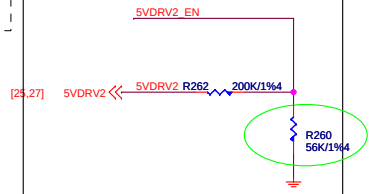
DPWROK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題

3.389V分壓=0.7V
2.55V分壓=0.528V

FOR DPWROK跟3VA的POWER DOWN的時序(S5-->G3)

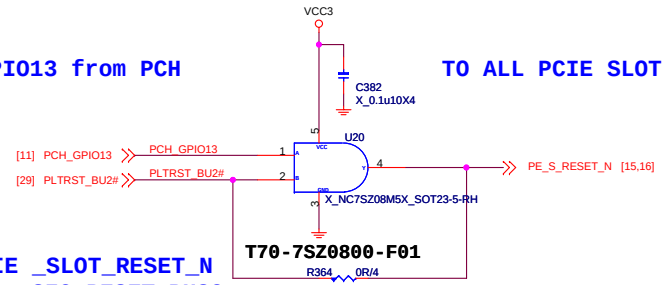


USB MODE



GPIO13 from PCH

TO ALL PCIE SLOT RESET#



T70-7SZ0800-F01

PCIE _SLOT_RESET_N
from SIO RESET_BUS2

MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size: Custom	Document Description: ACPI controller UPI	Rev: 2.0
Date: Friday, January 24, 2014	Sheet 32 of 45	

ISL95812 for VR12.5 suggest schematic

VCCP: 95W
IccMAX: 95A
TDC: 55A
VID1: 1.8V

VCORE power on by s3 and 12v

HIGH:0.7V
LOW:0.3V

R177 Load line

R145 TO 24.9K. ICCMAX:105A FW:LOW 300/500K
R139 TO 73.2K. 300K VBOOT 1.7V
R140 3.24K SLEW RATE 12MV/US PS1 2-PH

IC thermal pad 8 VIA connent GND lay

I32-958120C-I11

Since Idroop also sets the overcurrent protection level, it is recommended to first scale Idroop based on OCP requirement, then select an appropriate Rdroop value to obtain the desired load line slope.

RT1close to Q7

RT2 close to CHOKE5

UPI VOLTAGE CONSOLE

0x26:RH=3K,RL=2.3K

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x26:RH=18K,RL=13K

I34-1811B09-U33

MICRO-STAR INT'L CO.,LTD	
MS-7823	
Size: Custom	Document Description: VRD12 - PWM-UT501
Rev: 2.0	
Date: Friday, January 24, 2014	Sheet 33 of 45

OUTPUT CURRENT: ICCMAX 95A
Irms = 15.76A
Input Cap 5.08A*3= 15.24A

VCORE 95A TDC:66A
LL:1.5m ohm

L04-47B9041-T15
C71-2711771-N07
C71-5610681-N07
N93-04M0441-H06
D03-4C08N03-O05
D03-4C05N03-O05
I33-062081C-I11

JPWR2
PWRCONN4P_BLACK-RH-3
+12VIN
12VIN
CHOKE1
CH-0.47u60A0.98m-HF
C18 10u10x8
C14 10u16X8

[33] VCORE_UG1
R52 0R/8
VCORE_UG1_R
R45 10K/1%4
Q7
N-NTMFS4C08NT1G_SO8-HF
C17 1u16X6
C16 10u16X8
EC4 270u16SO
[33] VCORE_PHASE1
[33] VCORE_LG1
Q12
Q13
N-NTMFS4C05NT1G_SO8-HF
R29 2.2R/8
C22 1500p50X4

VCCP
EC14 EC8 EC9 EC10 EC11 EC12
560u6.3SO
CHOKE5
CH-0.47u60A0.98m-HF
CP3 X_COPPER
CP5 X_COPPER
VSUM+ R144 3.65K/1%8 Phase1_R
ISEN1 R143 10K/1%4
R142 10K/1%4 V2N
R141 10K/1%4 V3N
C98 0.22u25X6
R137 10K/1%4
VSUM- R138 10R/1%4
V1N
Close PWM

C47 C48 C49 10u6.3X6

[33] VCORE_UG2
R53 0R/8
VCORE_UG2_R
R46 10K/1%4
Q6
C24 1u16X6
C3 10u16X8
EC2 270u16SO
[33] VCORE_PHASE2
[33] VCORE_LG2
Q10
Q11
R28 2.2R/8
C21 1500p50X4

CHOKE4
CH-0.47u60A0.98m-HF
CP2 X_COPPER
CP6 X_COPPER
VSUM+ R153 3.65K/1%8 Phase2_R
ISEN2 R152 10K/1%4
R151 10K/1%4 V1N
R150 10K/1%4 V3N
C106 0.22u25X6
R147 X_20K/1%4
VSUM- R148 10R/1%4
V2N
Close PWM

BOOT3 R60 0R/8 BOOT3_C C38 0.22u25X6
U6
PWM3
VCORE_UG3
FCCM R80 0R/8
VCC5
C46 22u6.3X8
PWM FCCM BOOT GND UGATE PHASE VCC LGATE THERMAL PAD
FCCM
VCORE_PHASE3
VCORE_LG3
ISL6208BCRZ_QFN8-HF

[33] VCORE_UG3
R51 0R/8
VCORE_UG3_R
R43 10K/1%4
Q5
C13 1u16X6
C12 10u16X8
EC3 270u16SO
VCORE_PHASE3
VCORE_LG3
Q8
Q9
R27 2.2R/8
C20 1500p50X4

CHOKE3
CH-0.47u60A0.98m-HF
CP4 X_COPPER
CP7 X_COPPER
VSUM+ R166 3.65K/1%8 Phase3_R
ISEN3 R163 10K/1%4
R164 10K/1%4 V1N
R165 10K/1%4 V2N
C115 0.22u25X6
R155 13K/1%4
VSUM- R156 10R/1%4
V3N
Close PWM

MICRO-STAR INT'L CO.,LTD
MS-7823
Size: Custom
Document Description: 30 ISL6208B 3-Phase+MOS CPU
Rev: 2.0
Date: Friday, January 24, 2014
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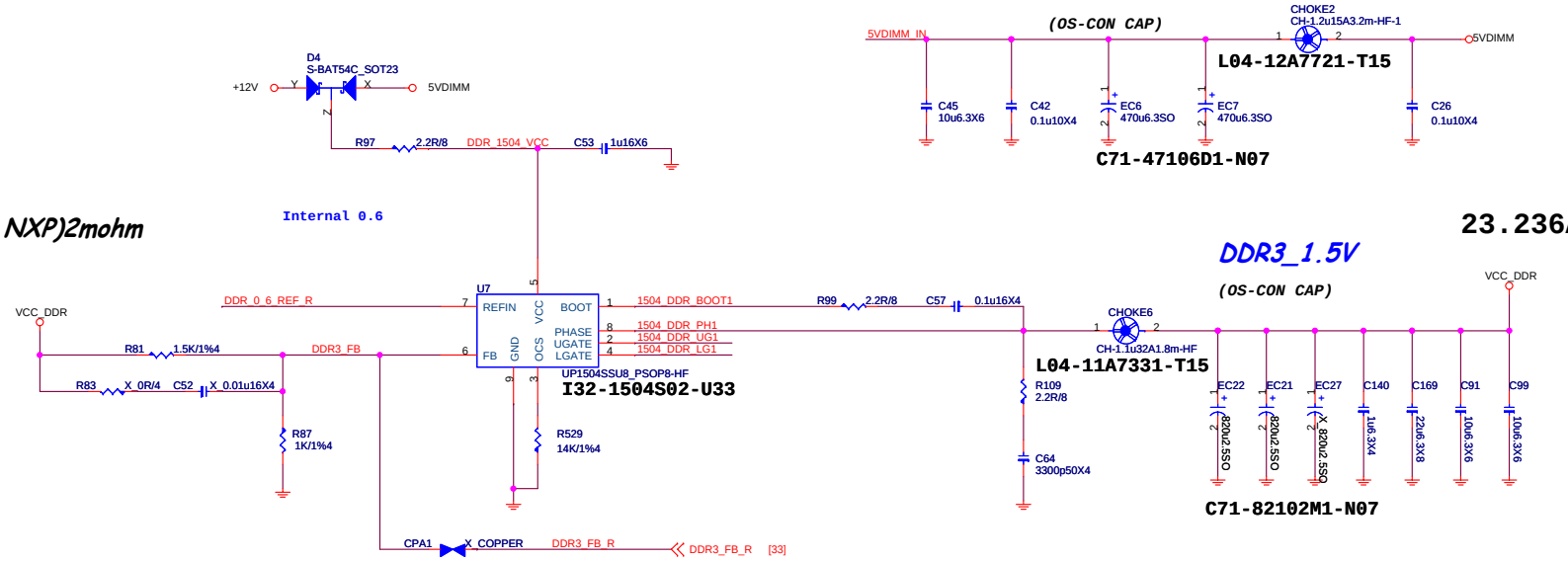
DDR Power:1.5V

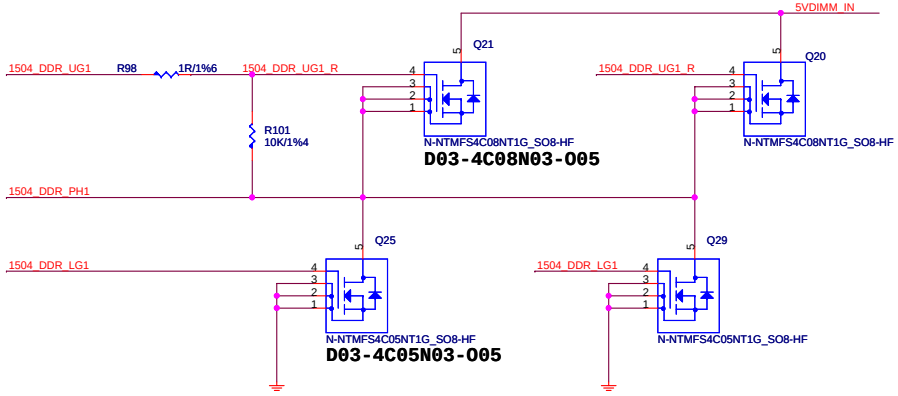
DDR3_1.5V 4.2A+12A+1.115A+5.921A=23.236A

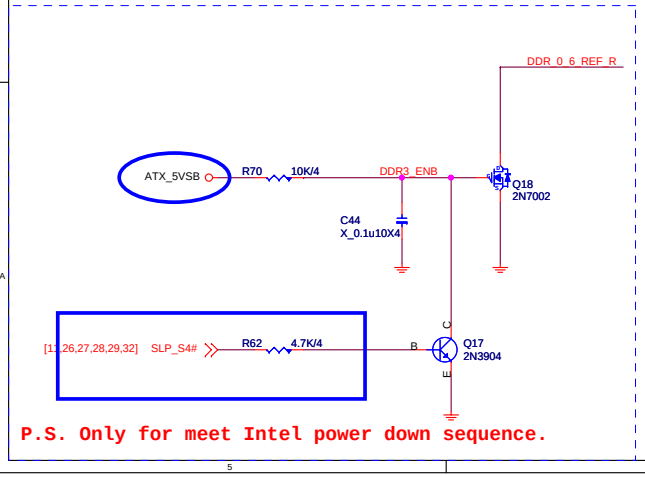
4.2A FOR CPU
12A FOR 4DIMM
1.115A FOR VTT_DDR
5.921A FOR PCH

*OCP 23.236A*1.5=34.845A*
*OCP=[20uA*Rocs(R320)]/4*Rdson(Low side NXP)2mohm*
R529=14K ohm

Iripple=10.64807288A
4.7*2*1=9.4A

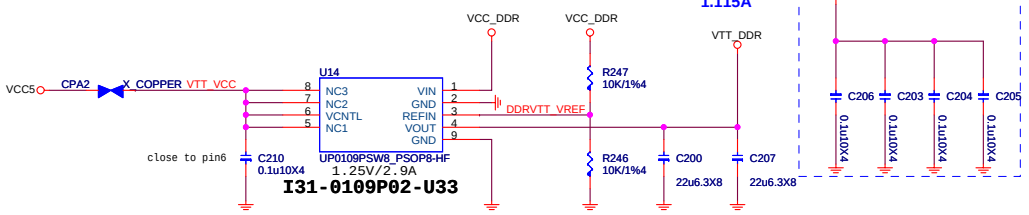






DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MICRO-STAR INT'L CO.,LTD

MS-7823

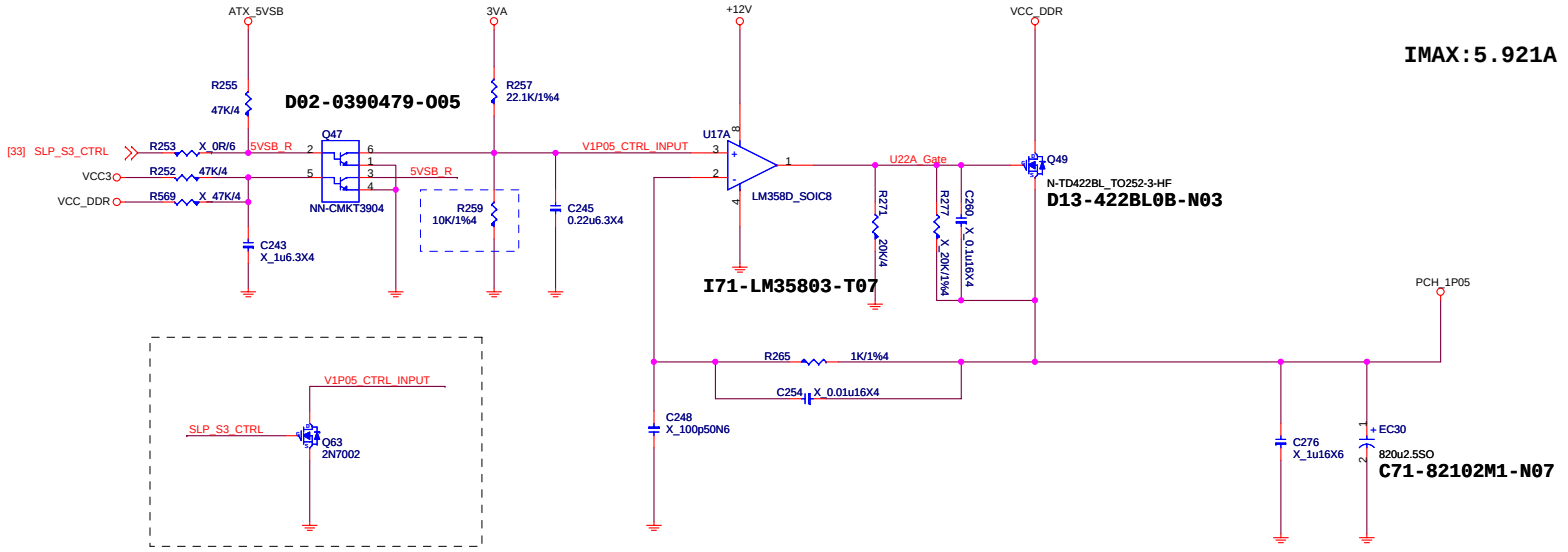
Size	Document Description	Rev
Custom	DDR Power -UP1504S 2-Phase MOS	2.0

Date: Friday, January 24, 2014 | Sheet 35 of 45

PCH Power:1.05V

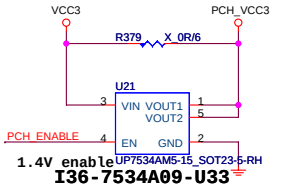
PCH Core 5.921A

R259->for Z87 Modify to 11K,PCH_1P05=1.12V
fix when BCLK=101~103MHz issue

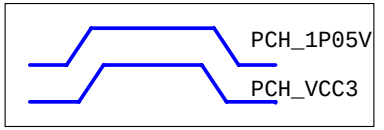


PCH Power:3.3V

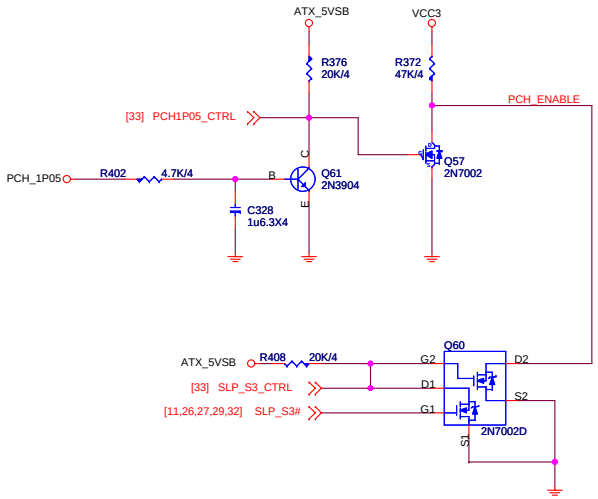
0.133A



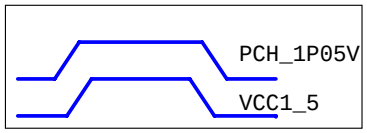
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



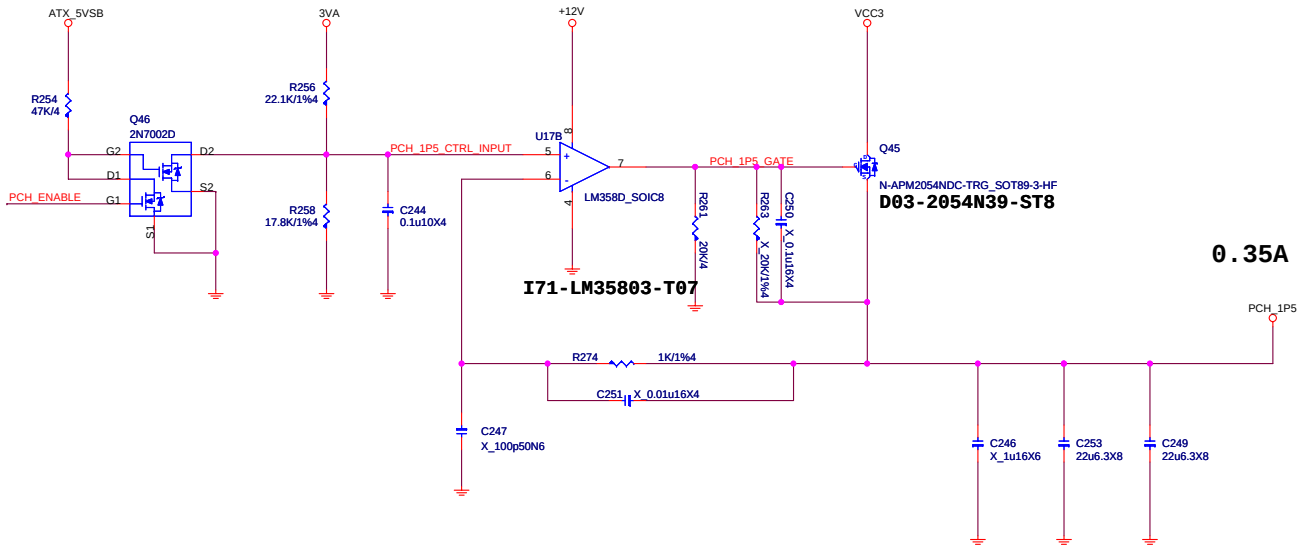
Waitting PCH_1P05 Ready



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



PCH Power:1.5V



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MS-7823		
Size: Custom	Document Description: PCH Power - uP1513 1-Phase MOS	Rev: 2.0
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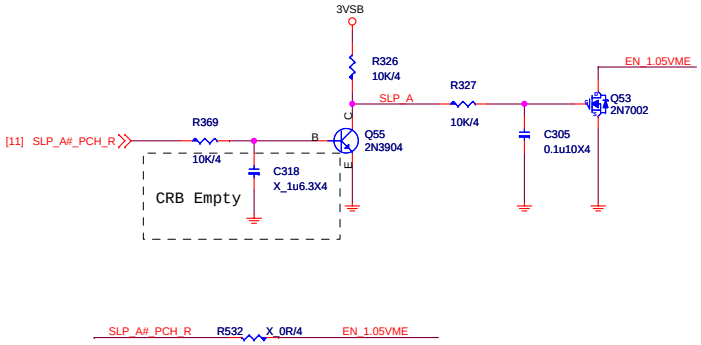
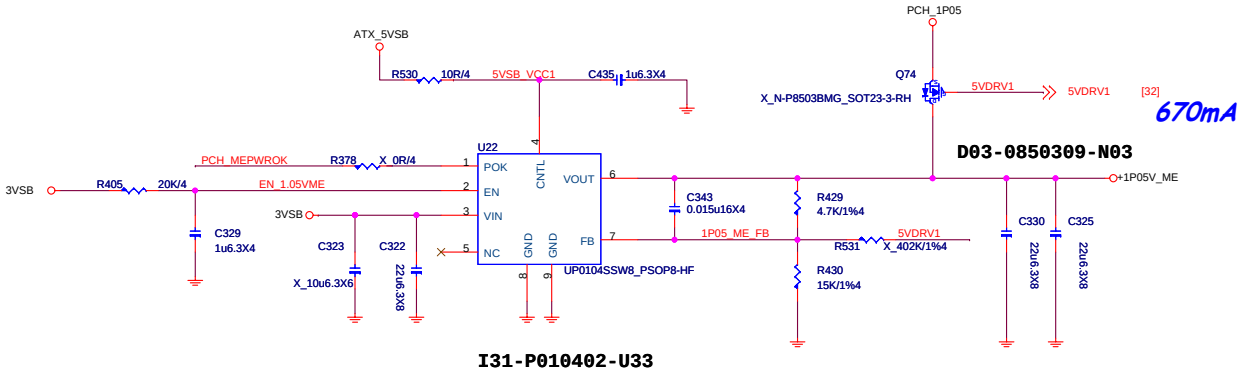
SLP_A

ME Power Control

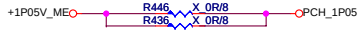


+1.05V_ME(VCCIO_ME)

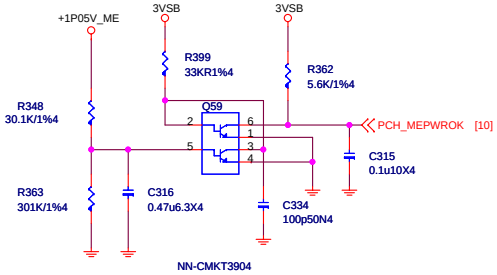


I31-P010402-U33

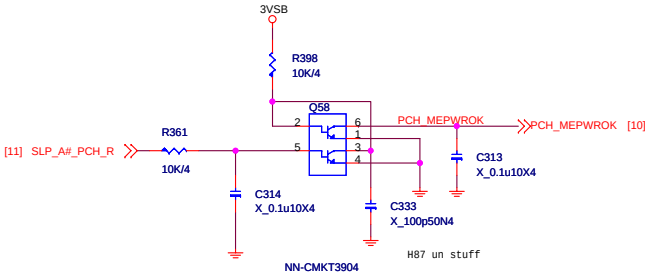
Reserve R for PCH_1P05 and +1P05V_ME short]
H81->Stuff R466, R436 and remove U22 circuit
B85->unused R466, R436 change use U22 circuit



PCH_MEPWROK

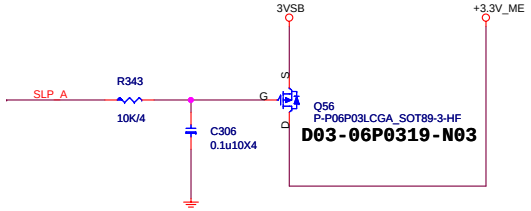


VccASW active to APWROK high 1ms



APWROK falling to VccASW falling 40ns

+3.3V_ME



For INTEL ME BUG
H81->Stuff R366
B85->Stuff R354

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Reserve debug port 5020

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Rev: 2.0	
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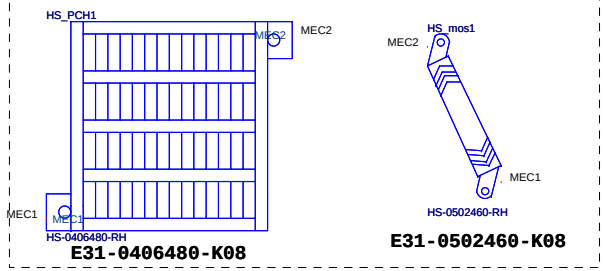
HEATSINK



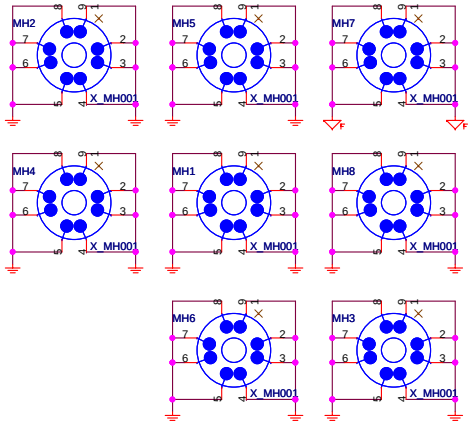
E31-0406480-K08

E31-0502460-K08

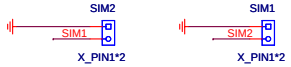
PCB1

PK0-0782320-E48
PK0-0782320-E48,聲華,23,寶安恩斯邁廠(MSIS)
PK0-0782320-G37,精成,23,寶安恩斯邁廠(MSIS)

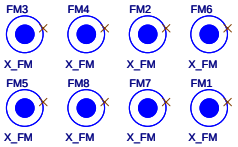
Mounting Holes



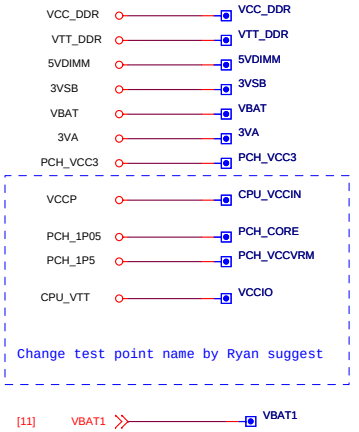
Simulation



Optical Fiducial Marks-120



Test point



SBC_LA1
Label
SBC
SBC LABEL

THX_LA2
Label
THX
X_THX LABEL

THX Virtual Part Number

LA3
AMI_BIOS LABLE
BIOS_LABLE

HDMI_LA1
Label
HDMI
HDMI LABEL

HDMI_RLA1
Real Label
HDMI
X_HDMI_RLA

LABEL2
MKT
X_BUY

BAT1_X1
BAT-BCR2032P-RH

CPU_H1
CPU
鐵座
ACA-ZIF-082-P35

E21-7670030-L06

Label OPT.

LA2
Label
601-7823-XXX
MKT-LABEL

B85

LA12
Label
601-7823-XXX
MKT-LABEL

B85

Chip OPT.

U103
LPT
B85
INTEL-DH82B85-RH-2

B85

U110
LPT
Z87
INTEL-DH82H81-RH

H81

Z87 SPI OPT.

SPI10
SPI
8M
W25Q64FVSSIQ-HF

D1000
MOS
2N7002
Q70 for Z87

Z87 PCH_1P05 OPT.

R1100
R
11K/1%4

R259 for Z87

MS-7823-2.0 主BOM爲B85

OPT	Configure	BOM	Function	GPIO Setting(page 29:GP10/GP11/GP12)
A	CFG-7823-20_B85	601-7823-?	MS-7823 20 OPT:A B85 B85M-?,B85,LGA1150,4DDR3,2PCI-Ex16,2PCI-Ex1 6SATA3,4USB3,HD Audio,Gb LAN,HDMI,DP,DVI,D-Sub	0,0,0
B	CFG-7823-20_H81	601-7823-?	MS-7823 20 OPT:B H81 H81M-?,H87,LGA1150,4DDR3,2PCI-Ex16,2PCI-Ex1 4SATA3,2USB3,,2VIA USB3,HD Audio,Gb LAN,HDMI,DP,DVI,D-Sub	0,0,1

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Custom	EMI CAP	2.0

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