X510UNR SCHEMATIC Revision

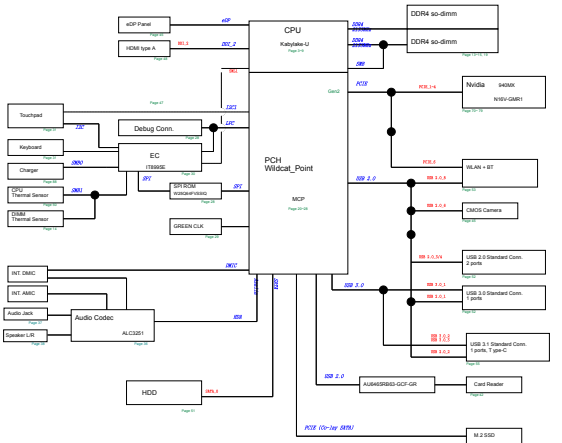
(UA : UMA)
(UQ : DGPU = Nvidia N16S-GTR, 940MX)

SYSTEM PAGE REF.

PAGE	Content
001	Block Diagram
002	System Setting
003	CPU_DISPLAY
004	CPU_DDR3
005	CPU_LPC,SPI,SMB,CLINK
006	CPU_POWER
008	CPU_MISC,JTAG
009	CPU_CFG,RSVD
010	CPU_POWER_CAP
012	DDR3L_TERMINATION
014	DDR3L_SO-DIMM2_A(1)
015	DDR3L_SO-DIMM2_A(2)
016	DDR3L_SO-DIMM_B
019	DDR3L_CA_DQ_VOLTAGE
020	CPU_PCH_CN12,XDMC
021	CPU_PCH_CNF20, LF20, MISC
022	CPU_PCH_AUDIO,SDIO,SDXC
023	CPU_PCH_PCIE,USB,SATA
024	CPU_PCH_CLOCK SIGNALS,RTC
025	CPU_PCH_FDI_POWER
026	CPU_PCH_PCHPWR,GND
027	CPU_PCH_PCHPWR,GND
028	PCH-SPI ROM,CTN
030	KBC_IT8995E/AX
031	KBC_WK,TP
032	RST_Reset Circuit
033	LAN_RTL8111GDR-CG
034	LAN RJ45
044	DEBUG PORT
042	eDP_LVDS
047	eDP to VGA & CRT D-SUB
048	HDMI-Type D
050	FAN & SENSOR
051	SATA ODD
052	USB 3.0 + 2.0 CONN
053	MISC(BAG/SLAB)
054	PWR_BTN & LID_SW
057	DSG_Discharge
058	PRO_Protect
060	DC_DC & BAT IN
064	
065	MB_Conn & Skew Hole
066	
067	IO Board-USB_LED_FPC_Screw
069	B to B connector
069	EMI
070	VGA_NVIDIA_N16V/S_PCIE
071	VGA_NVIDIA_N16V/S_FB-IF
072	VGA_NVIDIA_N16V/S_FB-DDR3
073	VGA_NVIDIA_N16V/S_VDD
074	VGA_NVIDIA_N16V/S_DISPLAY
075	VGA_NVIDIA_N16V/S_ROM,XTAL
076	VGA_NVIDIA_N16V/S_GPIO
077	VGA_NVIDIA_N16V/S_POWER
080	PW_IMVP8 (1) (RT3601BCGQW)
081	PW_IMVP8 (2) (RT3601BCGQW)
083	PW_ +1.0VSUS / +1.8VSUS
084	PW_+1.2VS
085	PW_1.35V/+0.675VS (UP5011Q)
087	PW_+3VADSW/+5VSUS (RT8249C)
088	PW_LOAD SWITCH
089	PW_CHARGER(BQ24780)
090	PW_PROTECTION
091	PW_DGPU_2PHASE(RT8815A)

BLOCK DIAGRAM

Non Connected Standby



CPU XDP | Discharge Circuit | DC & BATT. Conn. | PWM Fan
Reset Circuit | Skew Holes

PCH_CPT GPIO

Note	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	Note
	GPP_A0	Native1	RC_IN#		EXT PU 10K	+3VS	PU at EC
	GPP_A1	Native1	LPC_AD0				
	GPP_A2	Native1	LPC_AD1				
	GPP_A3	Native1	LPC_AD2				
	GPP_A4	Native1	LPC_AD3				
	GPP_A5	Native1	LPC_FRAME#				
	GPP_A6	Native1	INT_SERIRQ		EXT PU 10K	+3VS	
	GPP_A7	GPO	N/A				
	GPP_A8	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS	
	GPP_A9	Native1	CLK_KBCPCI_PCH				
	GPP_A10	Native	CLK_DEBUG				
For 555 N/A	GPP_A11	GPI	N/A	需確認是否具wake 功能			
	GPP_A12	GPO	N/A				
	GPP_A13	Native1	SUSWARN#		EXT PU 10K	+3VSUS	
	GPP_A14	Native1	PCH_SUS_STAT#				
Need Add EC	GPP_A15	Native1	PCH_SUSACK#				
For 555 N/A	GPP_A16	GPO	N/A (SD_1P8_SEL)				
For 555 N/A	GPP_A17	GPO	N/A (SD_PWR_EN#)				
	GPP_A18	GPO	N/A				
	GPP_A19	GPO	N/A				
	GPP_A20	GPO	N/A				
	GPP_A21	GPO	N/A				
	GPP_A22	GPO	N/A				
	GPP_A23	GPO	N/A				
For 555 N/A	GPP_B0	Native	N/A (VCCPRIM_VID0)		EXT PU 10K	+3VS	
For 555 N/A	GPP_B1	Native	N/A (VCCPRIM_VID1)		EXT PU 10K	+3VS	
	GPP_B2	GPO	N/A				
	GPP_B3	GPO	N/A				
	GPP_B4	GPO	N/A				
	GPP_B5	Native	CK_REQ_P0# DGPU		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B6	Native	CK_REQ_P1#		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B7	Native	CK_REQ_P2#		EXT PU 10K	+3VS	
	GPP_B8	Native	CK_REQ_P3#		EXT PU 10K	+3VS	
	GPP_B9	Native	CK_REQ_P4# GLAN		EXT PU 10K	+3VS	
	GPP_B10	Native	CK_REQ_P5# WLAN		EXT PU 10K	+3VS	
	GPP_B11	Native	MPHY_PWREN (N/A)		EXT PU 20K	+3VSUS	
	GPP_B12	Native	PCH_SLP_S0#				
	GPP_B13	Native	PLT_RST#				
	GPP_B14	GPO	PCH_GPPB14				
For 555 N/A	GPP_B15	GPO	N/A (GSPI0_CS_R#)				
For 555 N/A	GPP_B16	GPO	N/A (GSPI0_CLK_R)				
For 555 N/A	GPP_B17	GPO	N/A (GSPI0_MISO_R)				
	GPP_B18	GPO	PCH_GPPB18				
	GPP_B19	GPO	BT_ON/OFF#				
	GPP_B20	GPO	GPU_EVENT#		EXT PU 10K	+3VSG	
	GPP_B21	GPI	DGPU_FB_CLAMP_GPIO		EXT PD 10K	PU at DGPU	
	GPP_B22	GPO	PCH_GPPB22				
	GPP_B23	Native	SML1ALERT#		EXT PU 150K	+3VSUS	
	GPP_C0	Native	SMB_CK		EXT PU 2.2K	+3VSUS	
	GPP_C1	Native	SMB_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C2	GPO	GPP_C2				
For 555 N/A	GPP_C3	Native	SML0_CK		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C4	Native	SML0_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C5	GPO	GPP_C5				
	GPP_C6	Native	SML1_CK		EXT PU 2.2K	+3VSUS	
	GPP_C7	Native	SML1_DATA		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C8	GPO	N/A (PCH_GPPC8)				
For 555 N/A	GPP_C9	GPO	N/A (PCH_GPPC9)				
For 555 N/A	GPP_C10	GPO	N/A (PCH_GPPC10)				
For 555 N/A	GPP_C11	GPO	N/A (PCH_GPPC11)				
	GPP_C12	GPI	DIMM_SEL0		EXT PU 10K	+3VSUS	
	GPP_C13	GPI	DIMM_SEL1		EXT PU 10K	+3VSUS	
	GPP_C14	GPI	DIMM_SEL2	UART1_RTS#	EXT PU 10K	+3VSUS	
	GPP_C15	GPI	NFC_ID	UART1_CTS#	EXT PU 10K	+3VSUS	
	GPP_C16	GPO	AOAC_WLANLED(N/A)				
For 555 N/A	GPP_C17	GPO	N/A (ALS_INT#)				
For X541UV N/A	GPP_C18	Native	N/A				
For X541UV N/A	GPP_C19	Native	N/A				
	GPP_C20	GPI	DGPU_PWROK		EXT PU 10K	+3VSG	PU at DGPU
	GPP_C21	GPO	GPU_RST#		EXT PU 10K	+3VS	
	GPP_C22	GPO	DGPU_PWR_EN#		EXT PU 10K	+3VSUS	
	GPP_C23	GPI	TPanel_INT#		EXT PU 10K	+3VS	
	GPP_D0	GPO	N/A				
	GPP_D1	GPO	N/A				
	GPP_D2	GPO	N/A				
	GPP_D3	GPO	N/A				
For 555 N/A	GPP_D4	GPI	GPIO_SMI_ASM1142(N/A)				
	GPP_D5	GPO	SATA_ODD_PWRGT		EXT PU 10K	+3VS	
	GPP_D6	GPI	SATA_ODD_DA#		EXT PU 10K	+3VS	
	GPP_D7	GPO	N/A				
	GPP_D8	GPO	N/A				
	GPP_D9	GPI	PCB_ID0		EXT PD 10K		
For X541UV N/A	GPP_D10	GPI	DMIC_ID		EXT PD 10K		
	GPP_D11	GPI	TOUCHPAD_ID		EXT PD 10K		
	GPP_D12	GPI	TOUCH_PANEL_ID		EXT PD 10K		
	GPP_D13	GPI	TOUCHPAD_INTR#		EXT PU 10K	+3VS	
	GPP_D14	GPO	WLAN_LED_R				
X541UV Change	GPP_D15	GPO	SNSR_HUB_PWREN				
	GPP_D16	GPO	N/A	UART0_CTS#			
	GPP_D17	GPO	N/A				
	GPP_D18	GPO	N/A				
For 555 N/A	GPP_D19	GPO	(N/A) DMIC_CLK_PCH				
For 555 N/A	GPP_D20	GPO	(N/A) DMIC_DATA_PCH				
	GPP_D21	GPO	N/A				
	GPP_D22	GPO	N/A				

Note	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power
	GPP_D23	GPO	N/A			
	GPP_E0	GPO	DIRECT_ESATA_DETECT_R#		INT PD 20K	
	GPP_E1	GPO	SATA_ODD_PRSNT_R#		INT PD 20K	
	GPP_E2	GPO	MSATA_MPCIE_DET#		INT PD 20K	
	GPP_E3	GPO	N/A			
	GPP_E4	GPO	SATA0_DEVSLP			
	GPP_E5	GPO	SATA1_PHYSLP_DIRECT			
	GPP_E6	GPO	SATA2_DEVSLP			
	GPP_E7	GPO	N/A			
	GPP_E8	NATIVE	PCH_SATA_LED#		EXT PU 10K	+3VS
	GPP_E9	NATIVE	USB_OC_1_2#		EXT PU 10K	+3VSUS
	GPP_E10	GPI	USB_OC_3_4#		EXT PU 10K	+3VSUS
	GPP_E11	GPI	USB_OC_5_6#		EXT PU 10K	+3VSUS
	GPP_E12	GPI	USB_OC_7_8#		EXT PU 10K	+3VSUS
	GPP_E13	NATIVE	DDPB_HPD_PCH		EXT PD 100K	PD at IC of eDP to VGA
	GPP_E14	NATIVE	HDMI_HP		EXT PU 1M	+3VS PD at HDMI conn
	GPP_E15	GPO	EXT_SMI#		EXT PU 10K	+3VS
	GPP_E16	GPI	EXT_SCI#		EXT PU 10K	+3VS
	GPP_E17	NATIVE	EDP_HPD_CON		EXT PD 100K	PD at LVDS conn
	GPP_E18	NATIVE	DDPB_SCL_PCH		EXT PU 10K	+3VS
	GPP_E19	NATIVE	DDPB_SDA_PCH		EXT PU 10K	+3VS
	GPP_E20	NATIVE	DDPC_SCL_PCH		EXT PU 2.2K	+3VS PU at HDMI conn
	GPP_E21	NATIVE	DDPC_SDA_PCH		EXT PU 2.2K	+3VS PU at HDMI conn
	GPP_E22	GPO	N/A			
	GPP_E23	GPO	N/A			
	GPP_F0	GPO	N/A			
	GPP_F1	GPO	N/A			
	GPP_F2	GPO	N/A			
	GPP_F3	GPO	N/A			
	GPP_F4	GPO	I2C1_SDA_TCH_PAD		EXT PU 4.7K	+3VS
	GPP_F5	GPO	I2C1_SCL_TCH_PAD		EXT PU 4.7K	+3VS
	GPP_F6	GPO	N/A			
	GPP_F7	GPO	N/A			
	GPP_F8	GPO	N/A			
	GPP_F9	GPO	N/A			
	GPP_F10	GPO	N/A			
	GPP_F11	GPO	N/A			
	GPP_F12	GPO	N/A			
	GPP_F13	GPO	N/A			
	GPP_F14	GPO	N/A			
	GPP_F15	GPO	N/A			
	GPP_F16	GPO	N/A			
	GPP_F17	GPO	N/A			
	GPP_F18	GPO	N/A			
	GPP_F19	GPO	N/A			
	GPP_F20	GPO	N/A			
	GPP_F21	GPO	N/A			
	GPP_F22	GPO	N/A			
	GPP_F23	GPO	N/A			
For 555 N/A	GPP_G0	GPO	N/A (SDIO_CMD)			
For 555 N/A	GPP_G1	GPO	N/A (SDIO_D0)			
For 555 N/A	GPP_G2	GPO	N/A (SDIO_D1)			
For 555 N/A	GPP_G3	GPO	N/A (SDIO_D2)			
For 555 N/A	GPP_G4	GPO	N/A (SDIO_D3)			
For 555 N/A	GPP_G5	GPO	N/A (SDIO_CD#)			
For 555 N/A	GPP_G6	GPO	N/A (SDIO_CLK)			
For 555 N/A	GPP_G7	GPO	N/A (SDIO_WP)			
For 555 ADD	GPD0	Native	PM_BATLOW_R#		EXT PU 8.2K	+3VA_DSW
	GPD1	Native	ME_AC_PRESENT_PCH		EXT PU 100K	+3VA_DSW
	GPD2	GPI	PCH_GPD2#		EXT PU 10K	+3VA_DSW
	GPD3	Native	PM_PWRBTN#			
	GPD4	Native	PM_SUSB#		EXT PD 100K	PD at EC
	GPD5	Native	PM_SUSC#		EXT PD 100K	PD at EC
For 555 ADD	GPD6	Native	PM_SLP_A_R#			
	GPD7	GPO	WLAN_ON#			
For 555 N/A	GPD8	Native	NA (SUS_CK)		EXT PD 1K	
	GPD9	Native	SLP_WLAN#			
	GPD10	Native	SLP_S5# (N/A)			
	GPD11	Native	LAN_PWREN (N/A)			

EC IT8995 GPIO

Note	Pin Name	Config	Signal Name	Default status	Ext Pull up / down	Power
	GPA0	O	PWR_LED	LOW		
	GPA1	OD	CHG_LED#	HIGH	EXT 10K PU	+3VA_EC
	GPA2	OD	CHG_FULL_LED#	HIGH	EXT 10K PU	+3VA_EC
For 555 N/A	GPA3	Alt	FAN_PWM_GPU(N/A)	LOW		
For 555 N/A	GPA4	O	CLICK_WAKE#/WLAN_WAKE#_EC(N/A)	LOW	EXT 10K PU	+3VA_EC
	GPA5	Alt	FAN0_PWM	LOW		
	GPA6	Alt	KB_LED_PWM	LOW		
For 555 N/A	GPA7	O	OS_LED# (N/A)	HIGH		
	GPB0	Alt	AC_IN_OC#	HIGH	EXT 10K PU	+3VA
	GPB1	I	LID_SW#	HIGH	EXT 10K PU	+3VA
For 555 N/A	GPB2	OD	(N/A)	LOW	EXT 10K PU	+3VA_EC
	GPB3	I	PWR_SW#	HIGH	EXT 10K PU	+3VA
	GPB4	O	PS_ON	HIGH		
For 555 N/A	GPB5	O	A20GATE (N/A)	LOW	EXT 10K PU	+3VS
	GPB6	OD	RC_IN#	HIGH	EXT 10K PU	+3VS
For 555 N/A	GPC0	O	(N/A)	LOW		
	GPC1	Alt	SMB1_CLK	LOW	EXT 4.7K PU	+3VA_EC
	GPC2	Alt	SMB1_DAT	LOW	EXT 4.7K PU	+3VA_EC
	GPC3	O	PM_PWRBTN#	HIGH	EXT 10K PU	+3VSUS
For 555 N/A	GPC4	I	EC_GPC4 (N/A)	LOW	EXT 10K PU	+3VS
	GPC5	I	PM_SUSC#	HIGH	EXT 100K PD	
	GPC6	Alt	BAT1_IN_OC#	HIGH	EXT 10K PD	
For 555 N/A	GPC7	I	(N/A)	LOW		
	GPD0	I	PCH_SLP_S0#	HIGH		
	GPD1	O	ME_AC_PRESENT	LOW	EXT 100K PU	+3VA_DSW
	GPD2	Alt	BUF_PLT_RST#	HIGH	EXT 100K PD	
	GPD3	OD	EXT_SCI#	HIGH	EXT 10K PU	+3VS
	GPD4	OD	EXT_SMI#	HIGH	EXT 10K PU	+3VS
	GPD5	O	OP_SD#	HIGH		
	GPD6	Alt	FAN0_TACH	LOW	EXT 10K PU	+3VS
For 555 N/A	GPD7	Alt	(N/A)	LOW	EXT 10K PU	+3VS
	GPE0	O	SUSB_EC#	HIGH	EXT 10K PD	
	GPE1	O	SUSC_EC#	HIGH	EXT 10K PD	
	GPE2	O	1.2V_ON	LOW		
	GPE3	O	LAN_WAKE#	HIGH		
For 555 N/A	GPE4	O	(N/A)	HIGH		
	GPE5	I	PM_SUSB#	LOW	EXT 100K PD	
For 555 N/A	GPE6	OD	CAP_LED#	HIGH		
	GPE7	OD	THRO_CPU#	HIGH	EXT 1K PU	+VCCSTG
	GPF0	O	5VSUS_ON	LOW	EXT 10K PU/ 1M PD	+3VA_EC
	GPF1	O	VSUS_ON	LOW	EXT 100K PU	+3VA_EC
	GPF2	Alt	SMB0_CLK	HIGH	EXT 4.7K PU	+3VA_EC
	GPF3	Alt	SMB0_DATA	HIGH	EXT 4.7K PU	+3VA_EC
	GPF4	Alt	TP_CLK	HIGH	EXT 4.7K PU	+3VS
	GPF5	Alt	TP_DAT	HIGH	EXT 4.7K PU	+3VS
	GPF6	Alt	PECI_EC	LOW		
	GPF7	O	PCH_SPI_OV	LOW		
	GPG0	O	DGPU_LIMIT	LOW		
	GPG1	O	PCH_SUSACK#	HIGH		
	GPG2	I	PWRLIMIT_EC#	HIGH	EXT 100K PU	+3VA_EC
For 555 N/A	GPG6	O	(N/A)	LOW		
	GPH0	Alt	PM_CLKRUN#	HIGH	EXT 8.2K PU	+3VS
For 555 N/A	GPH1	Alt	SMB3_CLK N/A	HIGH		
For 555 N/A	GPH2	Alt	SMB3_DAT N/A	HIGH		
	GPH3	O	PM_RSMRST#	HIGH	EXT 10K PD	
	GPH4	O	DPWROK_EC	LOW	EXT 10K PD	
	GPH5	O	PM_PWROK	LOW	EXT 100K PD	
	GPH6	O	PM_SYSPWROK	LOW	EXT 10K PD	
	GPH7	O	LCD_BACKOFF#	HIGH		
	GPI0	I	PM_SLP_SUS#	HIGH	EXT 10K PU/ 100K PD	+3VA_EC
	GPI1	I	3VSUS_PWRGD	LOW		
	GPI2	I	ALL_SYSTEM_PWRGD	LOW	EXT 10K PU	+3VS
	GPI3	I	IMVP8_PWRGD	LOW	EXT 10K PU	+3VS
	GPI4	I	3VA_DSW_PWRGD	LOW	EXT 100K PU	+3VA_DSW
	GPI5	I	ME_SusPwrDnAck_EC	LOW		
	GPI6	Alt	A/D_MAX_POWER	LOW	EXT 0 PD	
	GPI7	Alt	MB_MAX_POWER	LOW	EXT 100K PU/93.1K PD	+3VACC
	GPJ0	I	EC_WAKE_SCI	LOW		
VC lose	GPJ1	O	3VADSW_ON	LOW	EXT 100K PU	+3VA_EC
For 555 N/A	GPJ2	Alt	PL_REF_EC N/A	LOW		
	GPJ3	O	PCH_SUS_STAT#	LOW		
For 555 N/A	GPJ4	Alt	IBAT_REF_EC N/A	LOW		
For 555 N/A	GPJ5	I	EC_GPJ5	LOW		
For 555 N/A	GPJ6	I	N/A	LOW		+3VS
For 555 N/A	GPJ7	O	N/A	HIGH		

*1: EC config GPI; Function output

Design IP Source:

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
EC Master (SMB1)	SM-Bus Address	
SM-Bus Device		
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

USB3 Port

USB3_1	USB 3.0 Port 0
USB3_2	USB 3.0 Port 1
USB3_3	
USB3_4	

PCI Express

PCIE 1	DGPU
PCIE 2	
PCIE 3	
PCIE 4	
PCIE 5	GLAN
PCIE 6	WLAN
PCIE 9	
PCIE 10	
PCIE 11	
PCIE 12	

SATA Port

SATA 0	HDD
SATA 1	ODD / 2nd HDD

PCI CLK

CLK0	DGPUx4
CLK1	
CLK2	
CLK3	
CLK4	LAN
CLK5	WLAN

USB Port

USB 1	USB 2.0 Port
USB 2	USB 2.0 Port
USB 3	USB 2.0 Port
USB 4	CARD READER
USB 5	
USB 6	CAMERA
USB 7	TOUCH_PANEL
USB 8	WLAN/BT
USB 9	
USB 10	

USB 3.0 Port 0
USB 3.0 Port 1

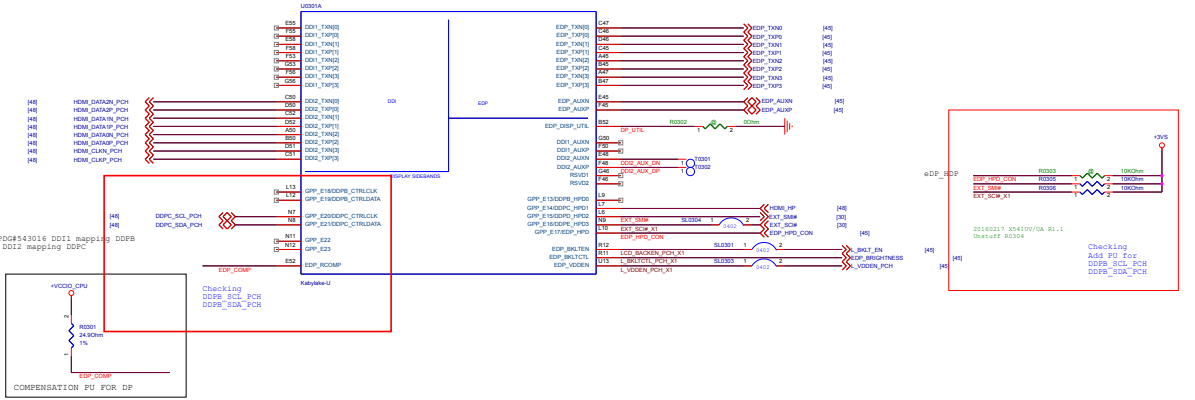
Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

Display Port

A	EDP
B	VGA
C	HDMI

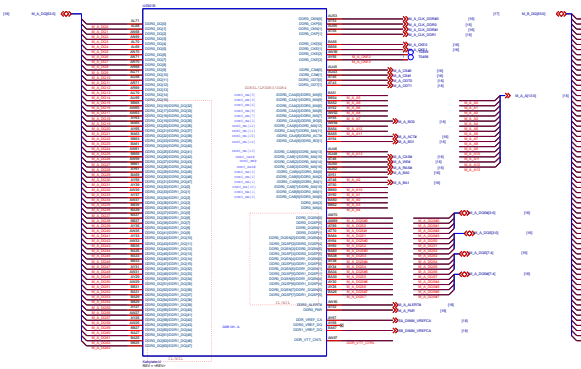
Intel Version	ASUS P/N
pre-ES	



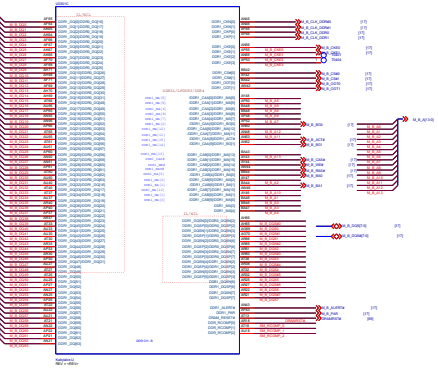
Main Board

512M x 8bit x 8

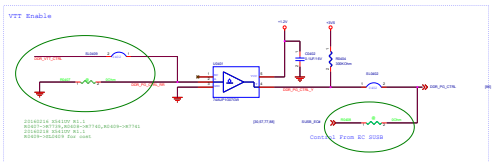
For On Board (A)

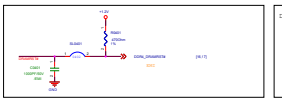


For SO-DIMM (B)

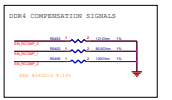


DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the pla. orm memory VTT regulator
in S3 and deeper and Sy...
Ref:546924_546924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120



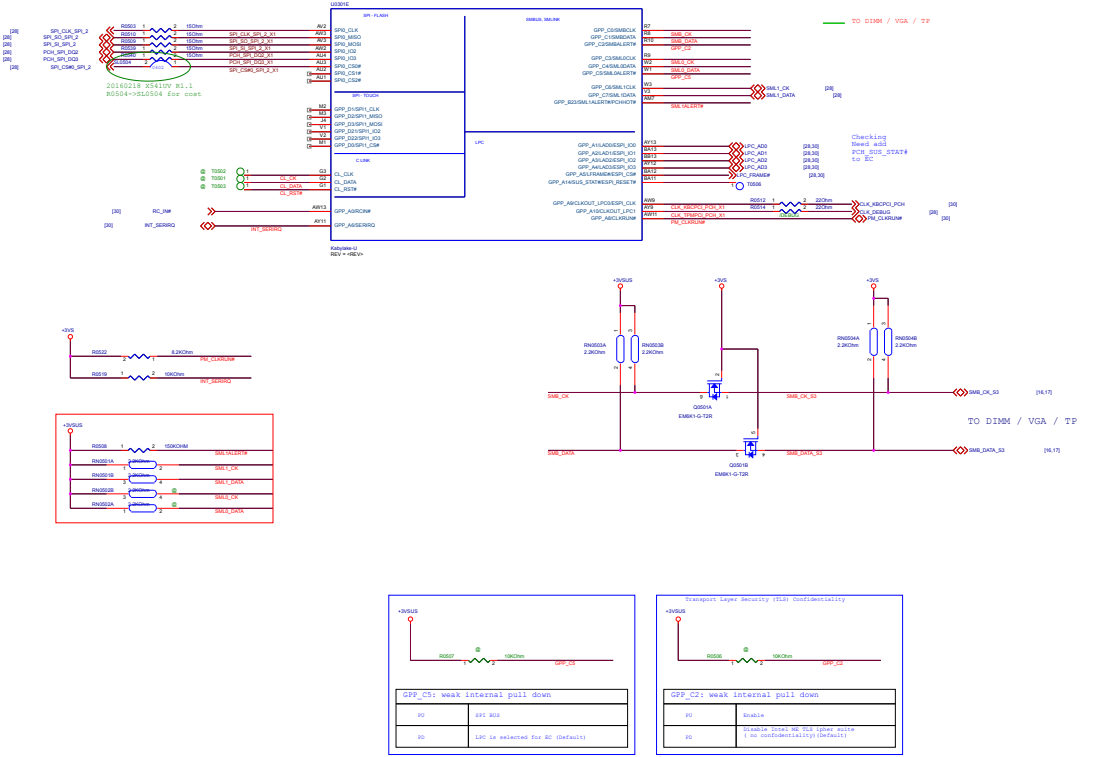


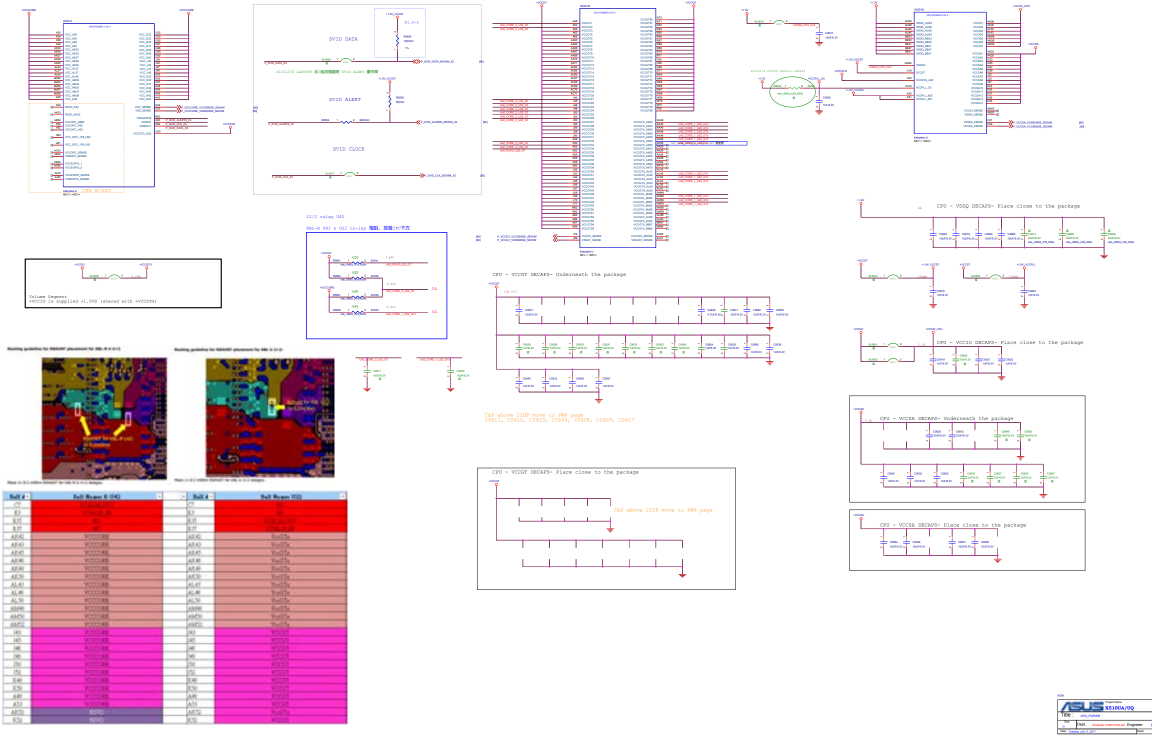
DDR4 COMPENSATION SIGNALS



www.teknisi-indonesia.com

Main Board

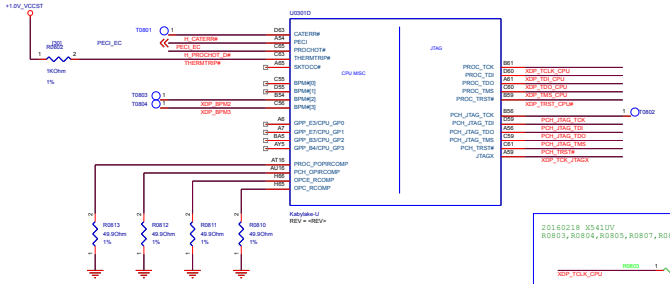

20160218 X541UV R1.1
R0504->1k1504 for cost
TO DIMM / VGA / TP
Checking
Need add
PCH_BIOS_STAT#
to EC
TO DIMM / VGA / TP
GPP_C5: weak internal pull down
PU
SPI BIOS
PD
LPC is selected for EC (Default)
Transport Layer Security (TLS) Confidentiality
GPP_C2: weak internal pull down
PU
Enable
PD
Disable Intel ME TLS cipher suite
(no confidentiality)(Default)



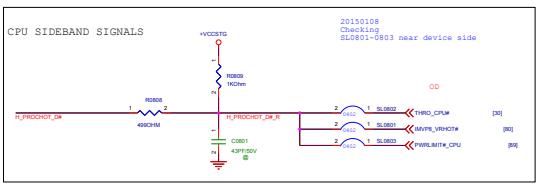
CPU_B/OPC
SVID DATA
SVID ALERT
SVID CLOCK
Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)
12/2 colay U42
KBL-R U42 & U22 co-lay 電阻, 放置CPU下方
CPU - VCCGT DECAPS- Underneath the package
CAP above 22UF move to PWR page
C0611, C0610, C0620, C0604, C0608, C0609, C0607
CPU - VCCGT DECAPS- Place close to the package
CAP above 22UF move to PWR page
CPU - VDDQ DECAPS- Place close to the package
CPU - VCCIO DECAPS- Place close to the package
CPU - VCCSA DECAPS- Underneath the package
CPU - VCCSA DECAPS- Place close to the package

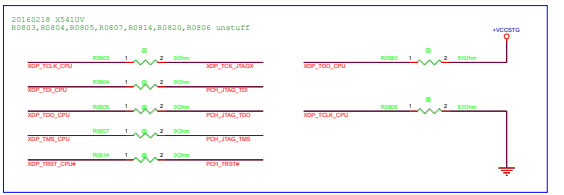
BOM

Project Name	X510UA/UQ	Rev R1.0
Title :	CPU_POEWR	
Size D	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Tuesday, July 11, 2017	Sheet 7	of 103

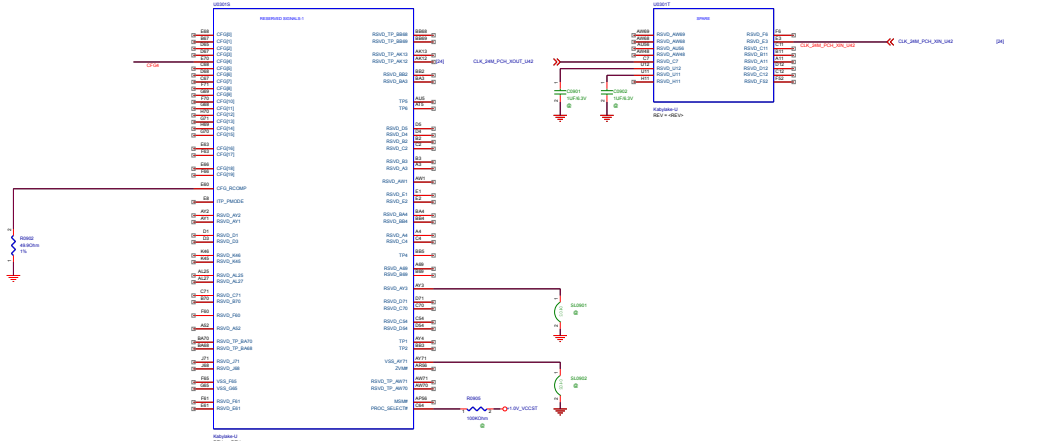


teknisi-indonesia



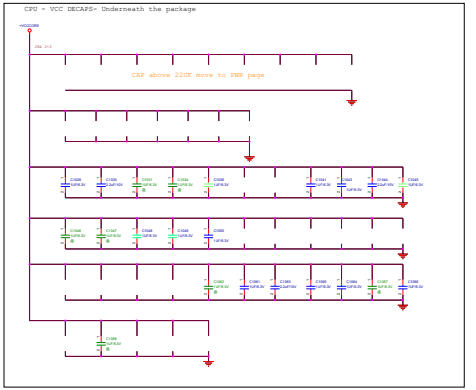


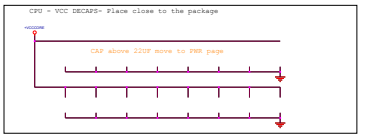
Main Board

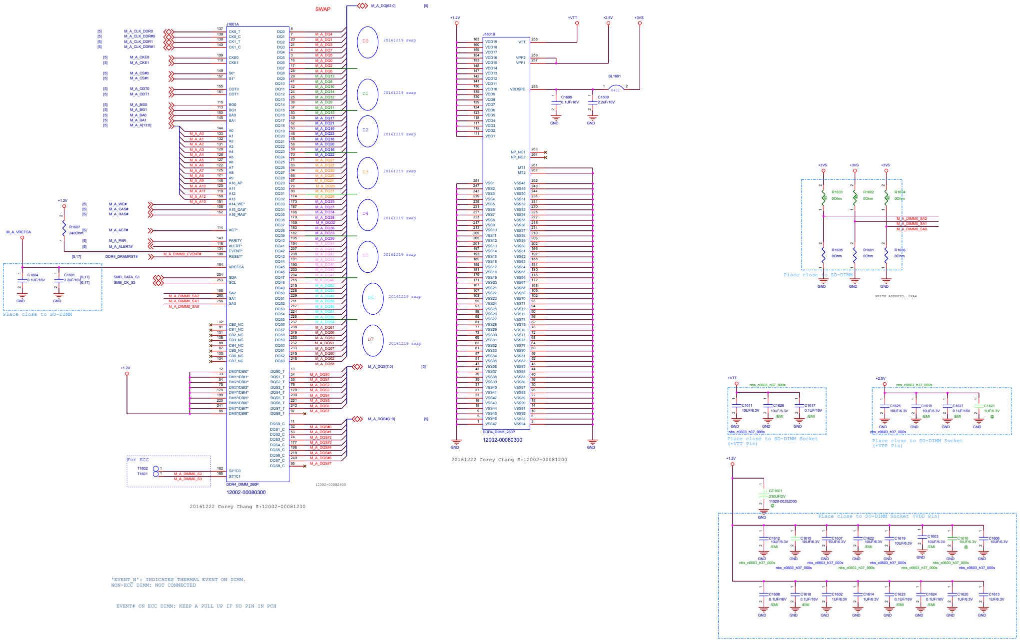


CFG STRAPS

	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE


CPU - VCC DECAPS- Underneath the package
CAP above 22UF move to PWR page


CPU - VCC DECAPS- Place close to the package
CAP above 22UF move to PWR page



'EVENT_N': INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

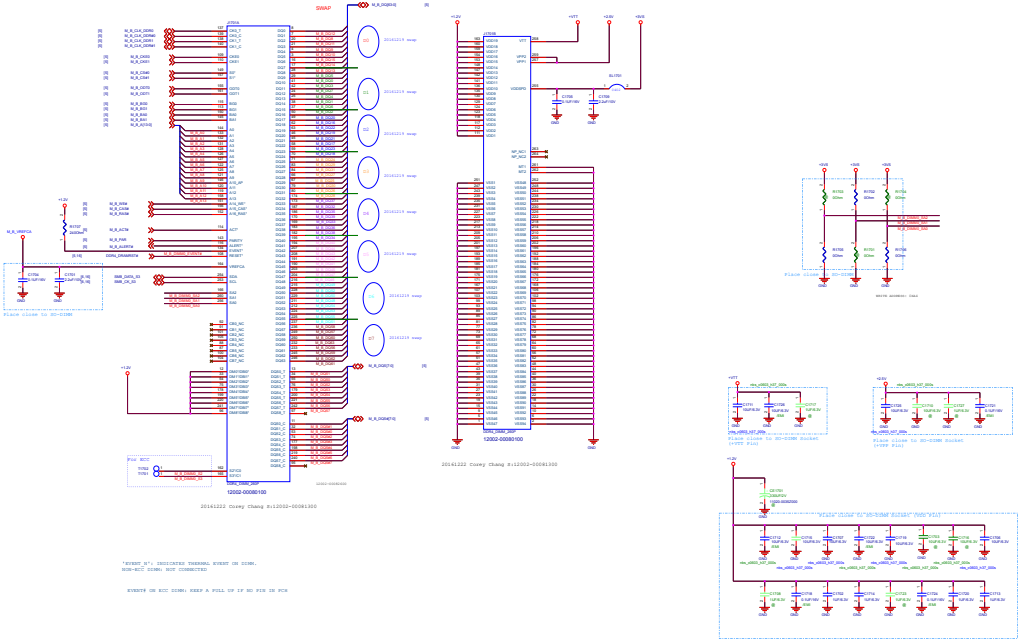

SWAP
Place close to SO-DIMM
Place close to SO-DIMM Socket +VTT Pin
Place close to SO-DIMM Socket +VDD Pin
'EVENT_N': INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED
EVENTB ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V_{REF-CA} Overview

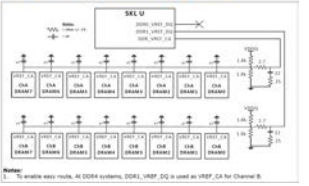
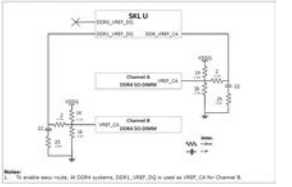
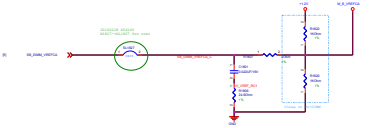
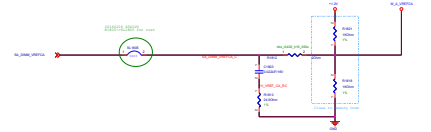


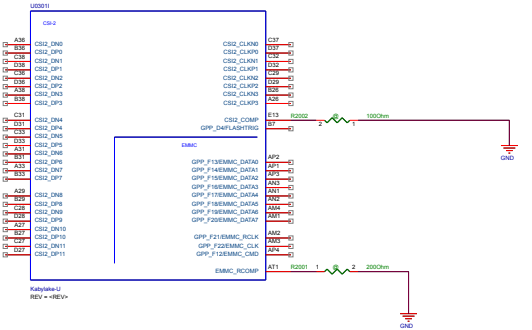
Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview

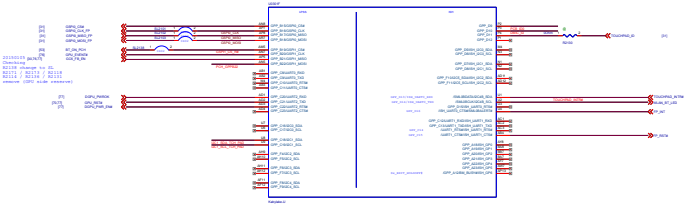


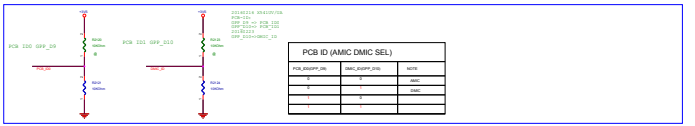
All Vref trace must be 20 mils width



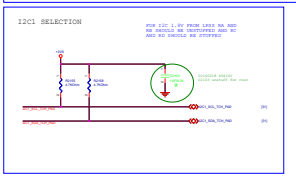


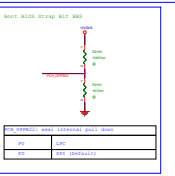

U03011
CSI-2
A36
B36
C38
D38
C36
D36
A38
B38
C31
D31
C33
D33
A31
B31
A33
B33
A29
B29
C28
D28
A27
B27
C27
D27
CSI2_DN0
CSI2_DP0
CSI2_DN1
CSI2_DP1
CSI2_DN2
CSI2_DP2
CSI2_DN3
CSI2_DP3
CSI2_DN4
CSI2_DP4
CSI2_DN5
CSI2_DP5
CSI2_DN6
CSI2_DP6
CSI2_DN7
CSI2_DP7
CSI2_DN8
CSI2_DP8
CSI2_DN9
CSI2_DP9
CSI2_DN10
CSI2_DP10
CSI2_DN11
CSI2_DP11
CSI2_CLKN0
CSI2_CLKP0
CSI2_CLKN1
CSI2_CLKP1
CSI2_CLKN2
CSI2_CLKP2
CSI2_CLKN3
CSI2_CLKP3
CSI2_COMP
GPP_D4/FLASHTRIG
C37
D37
C32
D32
C29
D29
B28
A26
E13
B7
R2202
2
1
100Ohm
GND
EMMC
GPP_F13/EMMC_DATA0
GPP_F14/EMMC_DATA1
GPP_F15/EMMC_DATA2
GPP_F16/EMMC_DATA3
GPP_F17/EMMC_DATA4
GPP_F18/EMMC_DATA5
GPP_F19/EMMC_DATA6
GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK
GPP_F22/EMMC_CLK
GPP_F12/EMMC_CMD
EMMC_RCOMP
AP2
AP1
AP3
AN3
AN1
AN2
AM4
AM1
AM2
AN5
AP4
AT1
R2001
1
2
200Ohm
GND
Kabylake-U
REV = <REV>



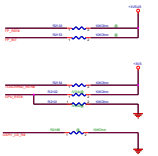


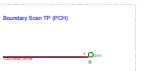
PCB ID (AMIC DMIC SEL)		
PCH_IDD(GPP_D9)	DMIC_ID(GPP_D10)	NOTE
0	0	AMIC
0	1	DMIC
1	0	
1	1	

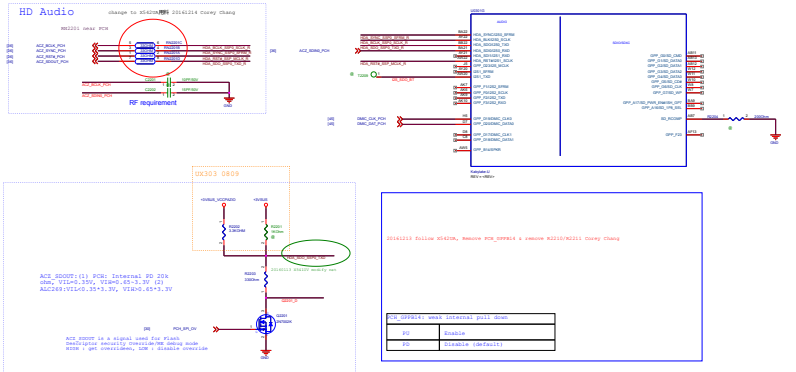


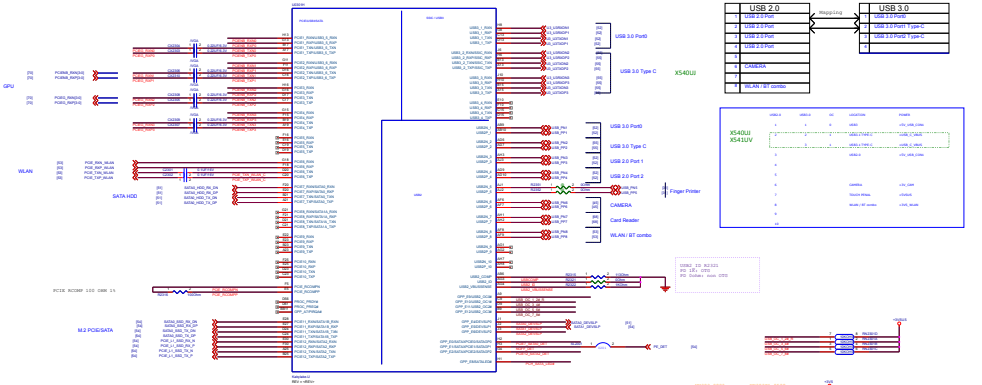


PCH_SPIWP(1): weak internal pull down	
0	LPC
1	SPI (Default)





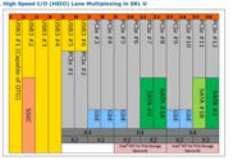


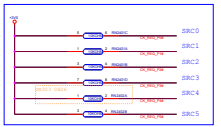


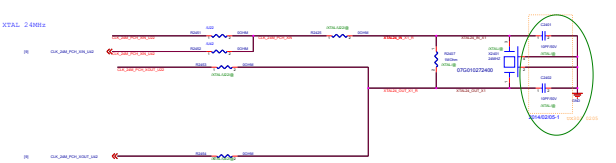
PCI-E* #1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
slot 1	ODD2		Port0
slot 2	ODD2		
slot 3	ODD2		
slot 4	ODD2		
slot 5	ELAN		Port4
slot 6	WLAN		Port5
slot 7/SSD1	HDD		
slot 8/SSD2	HDD & 2nd HDD		
slot 9			
slot 10			
slot 11/SSD3	N/A		

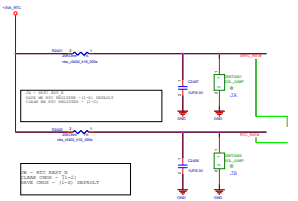
SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	ODD & 2nd HDD
PORT 2	N/A
PORT 3	N/A

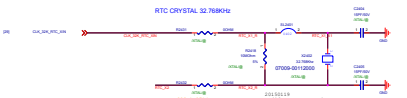
Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in SKL U



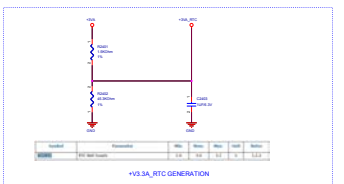




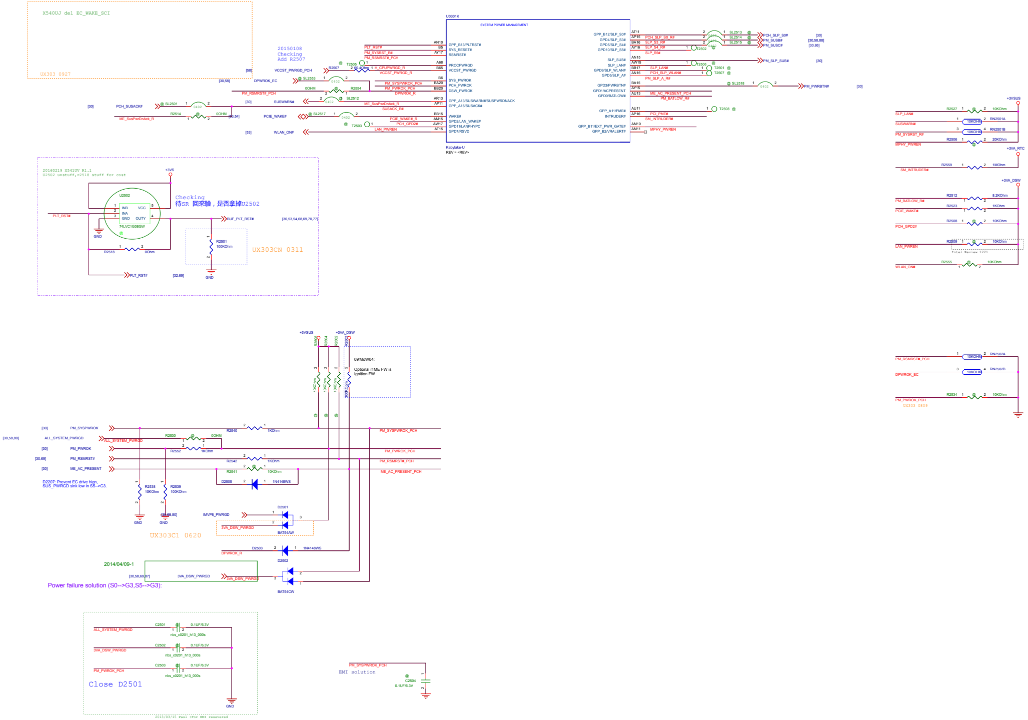




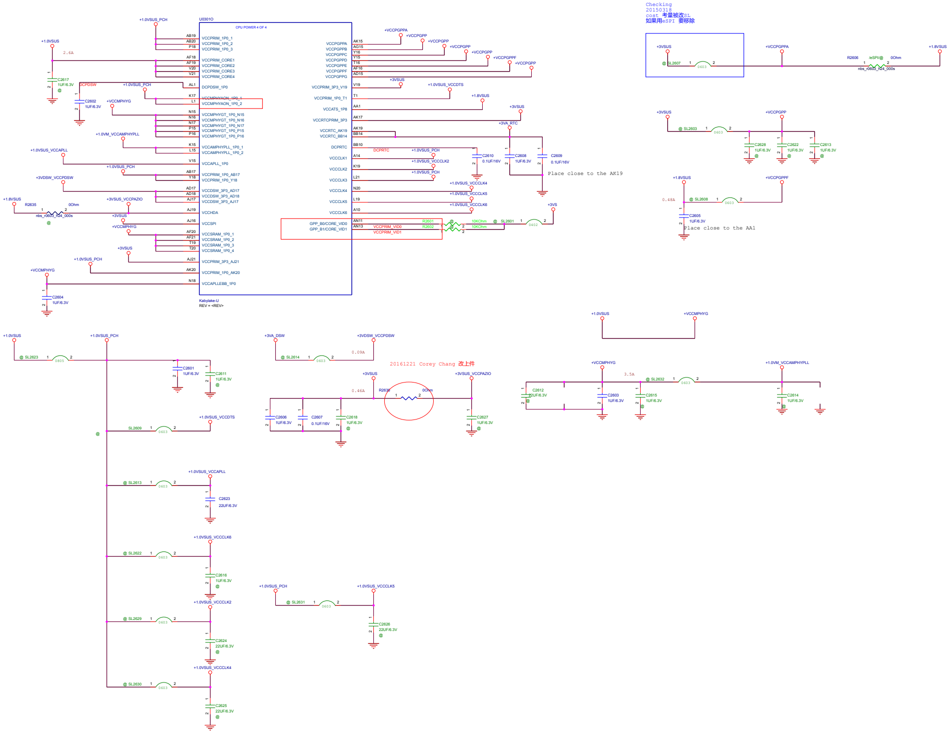
Follow UX310 Corey Chang 2016/12/08



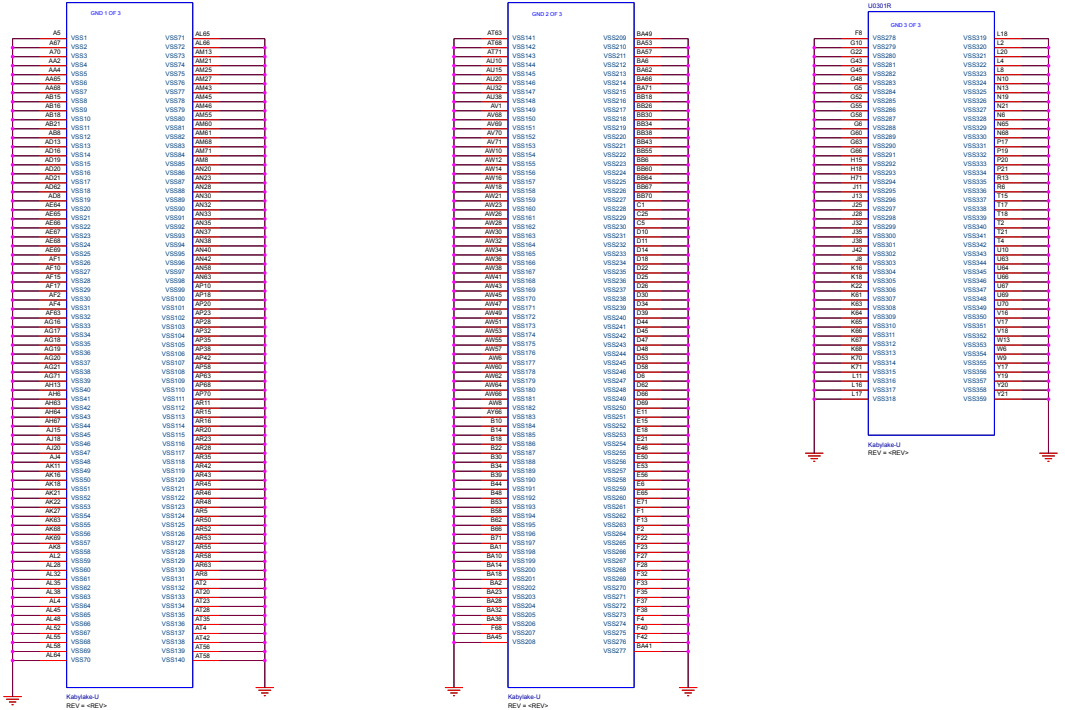
Main Board

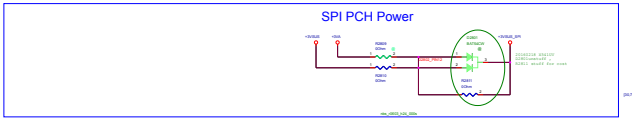


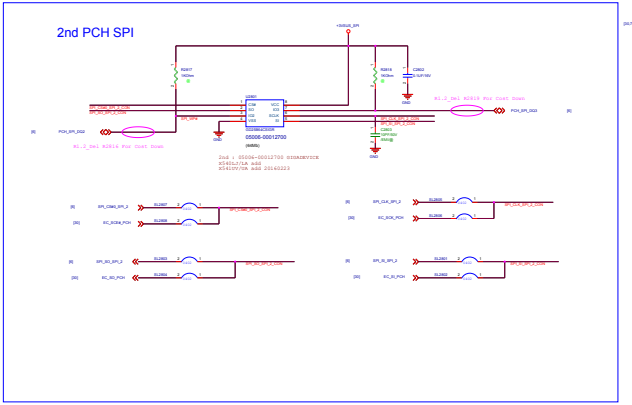
X540UJ del EC_WAKE_SCI
UX303 0927
20150108
Checking
Add R2507
U0301K
SYSTEM POWER MANAGEMENT
Kabylake-U
Checking
待SR 回來驗，是否拿掉U2502
UX303CN 0311
U2502
74LVC1G08GW
D2207: Prevent EC drive high, SUS_PWRGD sink low in S5-->G3.
UX303C1 0620
09'MoW04:
Optional if ME FW is Ignition FW
2014/04/09-1
Power failure solution (S0-->G3,S5-->G3):
Close D2501
EMI solution

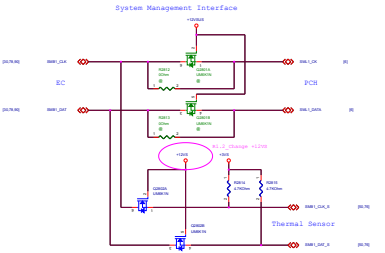


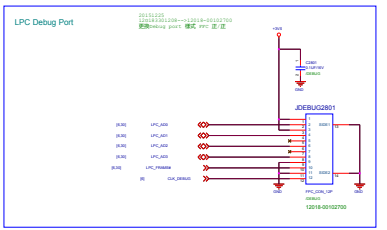
Checking
20150318
cost 考量被改SL
如果用eSPI 要移除
U0301O
CPU POWER 4 OF 4
Kabylake-U
REV = <REV>
+1.0VSUS_PCH
+1.0VSUS
2.6A
C2617
1UF/6.3V
DCPDSW
C2602
1UF/6.3V
+VCCMPHYG
+1.0VM_VCCAMPHYPLL
+1.0VSUS_VCCAPLL
+3VDSW_VCCPDSW
+1.8VSUS
R2635
0Ohm
+3VSUS_VCCPAZIO
+3VSUS
C2604
1UF/6.3V
VCCPRIM_1P0_1
VCCPRIM_1P0_2
VCCPRIM_1P0_3
VCCPRIM_CORE1
VCCPRIM_CORE2
VCCPRIM_CORE3
VCCPRIM_CORE4
DCPDSW_1P0
VCCMPHYAON_1P0_1
VCCMPHYAON_1P0_2
VCCMPHYGT_1P0_N15
VCCMPHYGT_1P0_N16
VCCMPHYGT_1P0_N17
VCCMPHYGT_1P0_P15
VCCMPHYGT_1P0_P16
VCCAMPHYPLL_1P0_1
VCCAMPHYPLL_1P0_2
VCCAPLL_1P0
VCCPRIM_1P0_AB17
VCCPRIM_1P0_Y18
VCCDSW_3P3_AD17
VCCDSW_3P3_AD18
VCCDSW_3P3_AJ17
VCCHDA
VCCSPI
VCCSRAM_1P0_1
VCCSRAM_1P0_2
VCCSRAM_1P0_3
VCCSRAM_1P0_4
VCCPRIM_3P3_AJ21
VCCPRIM_1P0_AK20
VCCAPLLEBB_1P0
VCCPGPPA
VCCPGPPB
VCCPGPPC
VCCPGPPD
VCCPGPPE
VCCPGPPF
VCCPGPPG
VCCPRIM_3P3_V19
VCCPRIM_1P0_T1
VCCATS_1P8
VCCRTCPRIM_3P3
VCCRTC_AK19
VCCRTC_BB14
DCPRTC
VCCCLK1
VCCCLK2
VCCCLK3
VCCCLK4
VCCCLK5
VCCCLK6
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
+VCCPGPPA
+VCCPGPP
+VCCPGPPF
+1.0VSUS_VCCDTS
+3VA_RTC
C2610
0.1UF/16V
C2608
1UF/6.3V
C2609
0.1UF/16V
Place close to the AK19
+1.0VSUS_VCCCLK2
+1.0VSUS_VCCCLK4
+1.0VSUS_VCCCLK5
+1.0VSUS_VCCCLK6
VCCPRIM_VID0
VCCPRIM_VID1
R2601
R2602
10KOhm
SL2601
+3VS
R2606
0Ohm
nbs_r0603_h24_000s
+1.8VSUS
SL2607
SL2603
C2628
C2622
C2613
1UF/6.3V
SL2608
0.48A
C2605
1UF/6.3V
Place close to the AA1
+1.0VSUS
+VCCMPHYG
SL2623
C2601
1UF/6.3V
C2611
1UF/6.3V
SL2609
SL2613
+1.0VSUS_VCCAPLL
C2623
22UF/6.3V
SL2622
+1.0VSUS_VCCCLK6
C2618
1UF/6.3V
SL2629
+1.0VSUS_VCCCLK2
C2624
22UF/6.3V
SL2630
+1.0VSUS_VCCCLK4
C2625
22UF/6.3V
+3VA_DSW
+3VDSW_VCCPDSW
SL2614
0.09A
20161221 Corey Chang 改上件
+3VSUS
+3VSUS_VCCPAZIO
0.46A
R2638
0Ohm
C2606
1UF/6.3V
C2607
0.1UF/16V
C2618
1UF/6.3V
C2627
1UF/6.3V
+1.0VSUS_PCH
+1.0VSUS_VCCCLK5
SL2631
C2626
22UF/6.3V
+VCCMPHYG
3.5A
SL2632
+1.0VM_VCCAMPHYPLL
C2612
22UF/6.3V
C2603
1UF/6.3V
C2615
1UF/6.3V
C2614
1UF/6.3V


U0301P
GND 1 OF 3
Kabylake-U
REV = <REV>
U0301Q
GND 2 OF 3
Kabylake-U
REV = <REV>
U0301R
GND 3 OF 3
Kabylake-U
REV = <REV>



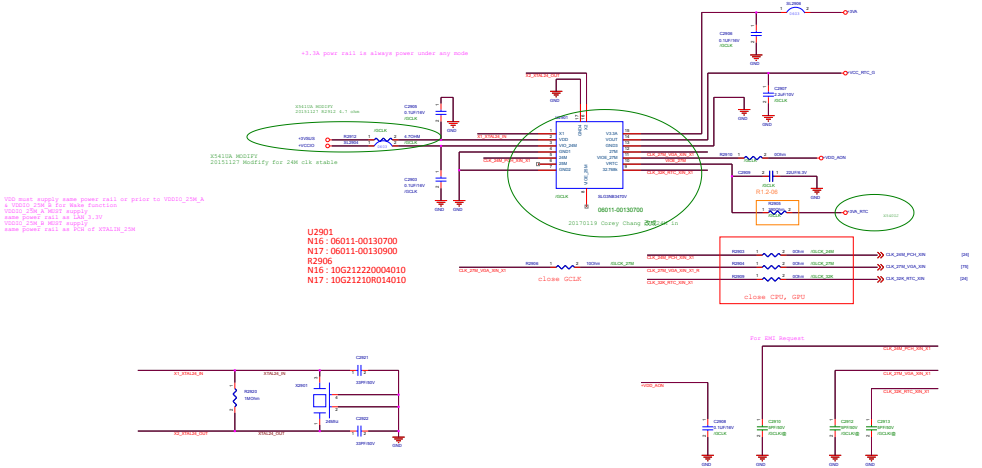


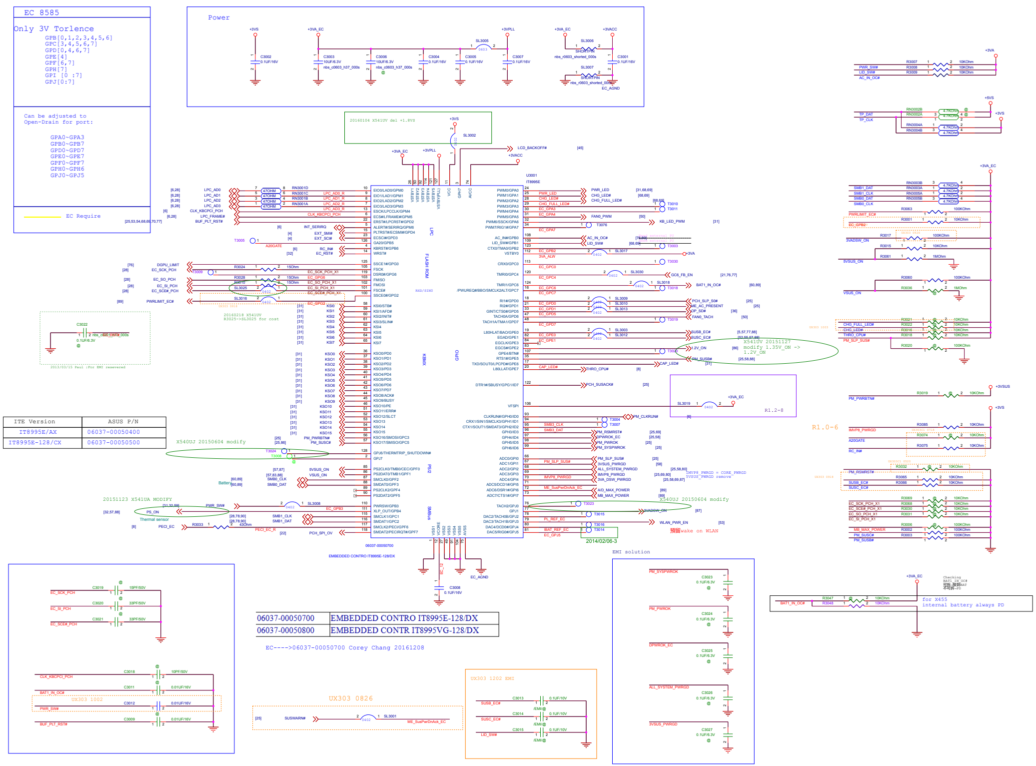




www.teknisi-indonesia.com

Silego Green CLK





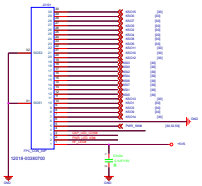
EC 8585
Only 3V Torlence
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
Can be adjusted to
Open-Drain for port:
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5
EC Require
Power
20160104 X541UV del +1.8VS
U3001
IT8995E
LPC
FLASH ROM
KBMX
GPIO
PS2
SMBus
06037-00050700
EMBEDDED CONTRO IT8995E-128/DX
X540UJ 20150604 modify
20151123 X541UA MODIFY
X541UV 20151127
modify 1.35V_ON ->
1.2V_ON
R1.2-8
R1.0-6
EMI solution
UX303 0826
UX303 1202 EMI
UX303 1002
for X455
internal battery always PD
2014/02/06-3

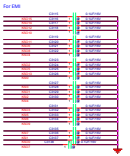
ITE Version	ASUS P/N
IT8995E/AX	06037-00050400
IT8995E-128/CX	06037-00050500

06037-00050700	EMBEDDED CONTRO IT8995E-128/DX
06037-00050800	EMBEDDED CONTR IT8995VG-128/DX

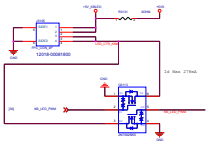
EC---->06037-00050700 Corey Chang 20161208

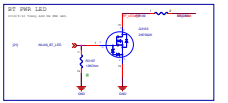
Internal Keyboard

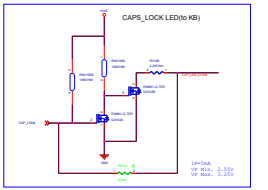




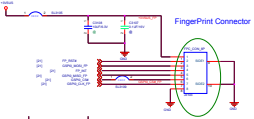
BL

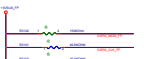




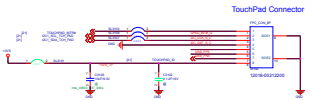


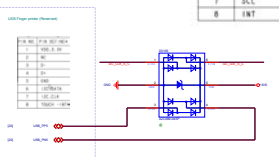
Touch PAD



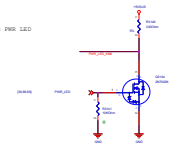


CN1		CN2	
PIN NO.	PIN DEFINE	PIN NO.	PIN DEFINE
1	VDD_3.3V_TP	1	VDD_3.3V_FP
2	GND	2	FP_RSTN
3	PS2_CLK	3	FP_MOSI
4	PS2_DATA	4	FP_INTN
5	GND	5	FP_MISO
6	SDA	6	FP_CSN
7	SCL	7	FP_SCK
8	INT	8	GND

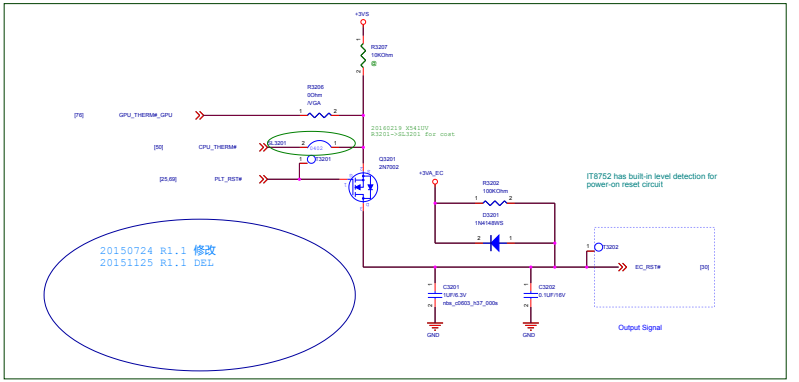




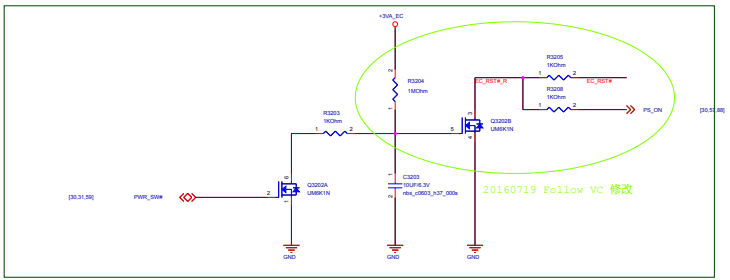
KB PWR LED



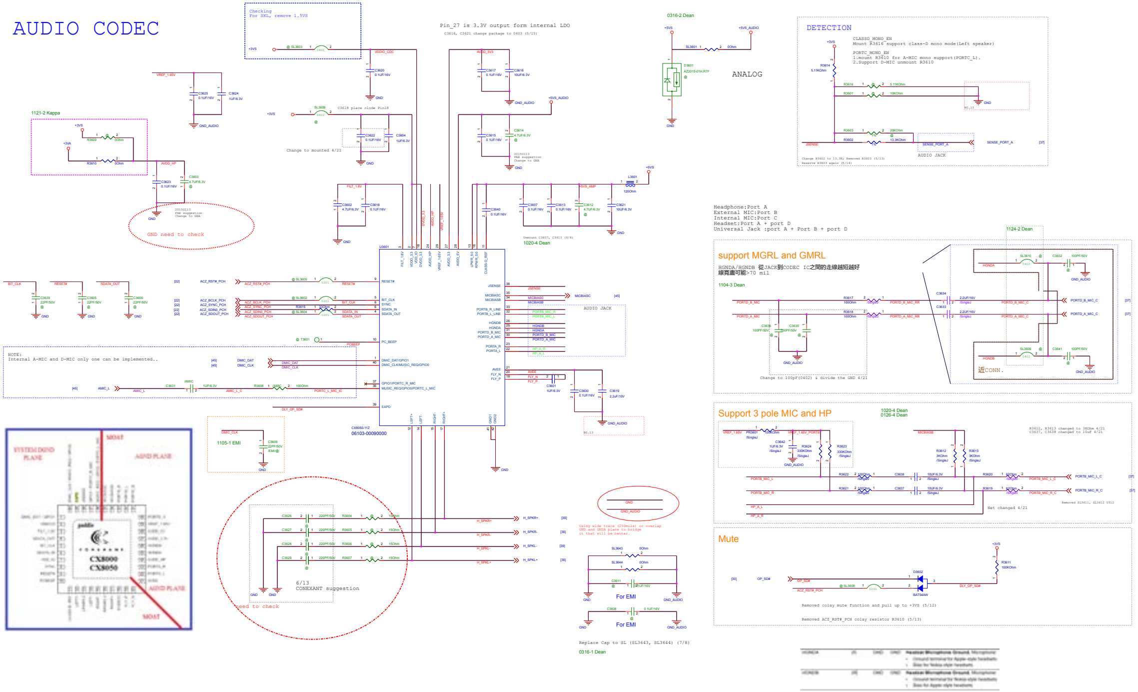
Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)

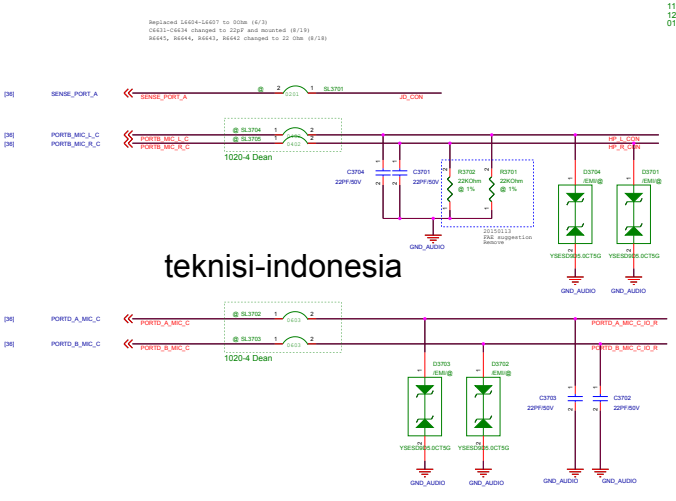


AUDIO CODEC



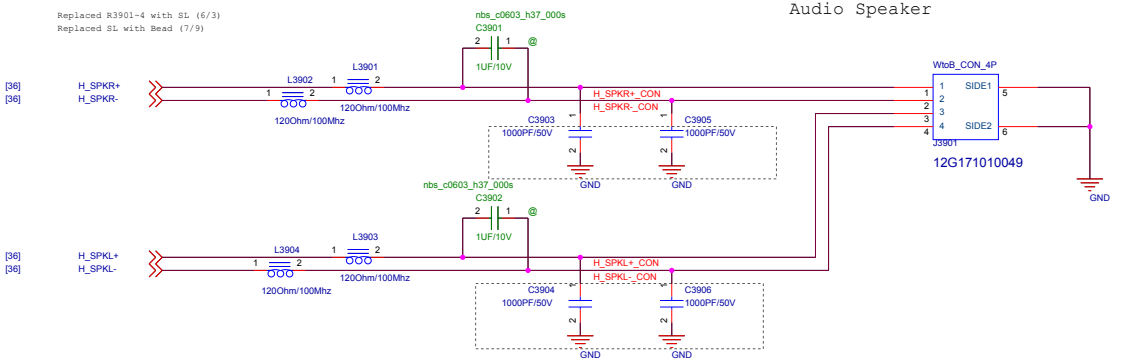
Checking
For SKL, remove 1.5VS
Pin_27 is 3.3V output form internal LDO
C3616, C3621 change package to 0603 (5/15)
0316-2 Dean
ANALOG
DETECTION
CLASSD_MONO_EN
Mount R3616 support class-D mono mode(Left speaker)
PORTC_MONO_EN
1.mount R3610 for A-MIC mono support(PORTC_L).
2.Support D-MIC unmount R3610
AUDIO JACK
SENSE_PORT_A
1121-2 Kappa
C3618 place close Pin18
Change to mounted 4/21
GND need to check
Unmount C3607, C3613 (4/8)
1020-4 Dean
Headphone:Port A
External MIC:Port B
Internal MIC:Port C
Headset:Port A + port D
Universal Jack :port A + Port B + port D
1124-2 Dean
support MGRL and GMRL
HGNDA/HGNDB 從JACK到CODEC IC之間的走線越短越好
線寬盡可能>70 mil
1104-3 Dean
Change to 100pF(0402) & divide the GND 4/21
近CONN.
NOTE:
Internal A-MIC and D-MIC only one can be implemented..
CX8050-11Z
06103-00090000
1105-1 EMI
SYSTEM DGND PLANE
MOAT
AGND PLANE
CX8000
CX8050
6/13
CONEXANT suggestion
Need to check
Using wide trace (250mils) or overlap GND and GNDA plane to bridge it that will be better.
For EMI
Replace Cap to SL (SL3643, SL3644) (7/8)
0316-1 Dean
Support 3 pole MIC and HP
1020-4 Dean
0126-4 Dean
R3612, R3613 changed to 3kOhm 4/21
C3637, C3638 changed to 10uF 4/21
Net changed 4/21
Mute
Removed colay mute function and pull up to +3VS (5/12)
Removed ACZ_RST#_PCH colay resistor R3610 (5/13)

Audio Jack


Replaced L6604-L6607 to 0Ohm (4/3)
C6631-C6634 changed to 22pF and mounted (8/19)
R6645, R6644, R6643, R6642 changed to 22 Ohm (8/18)
1116-1 Dean
1207-4 EMI
0106-7 Dean
[36] SENSE_PORT_A
SENSE_PORT_A
SL3701
JD_CON
[36] PORTB_MIC_L_C
[36] PORTB_MIC_R_C
PORTB_MIC_L_C
PORTB_MIC_R_C
SL3704
SL3705
0402
1020-4 Dean
C3704
22PF/50V
C3701
22PF/50V
R3702
22KOhm
@ 1%
R3701
22KOhm
@ 1%
DNI suggestion
Remove
HP_L_CON
HP_R_CON
D3704
/EMI@
D3701
/EMI@
YSESD05.0CT5G
GND_AUDIO
teknisi-indonesia
[36] PORTD_A_MIC_C
[36] PORTD_B_MIC_C
PORTD_A_MIC_C
PORTD_B_MIC_C
SL3702
SL3703
0603
1020-4 Dean
D3703
/EMI@
D3702
/EMI@
PORTD_A_MIC_C_IO_R
PORTD_B_MIC_C_IO_R
C3703
22PF/50V
C3702
22PF/50V
JD pin = Normal open.
JD_CON
PORTD_A_MIC_C_IO_R
HP_L_CON
HP_R_CON
PORTD_B_MIC_C_IO_R
J3701
AUDIO_JACK_6P
12014-00715000
GND_AUDIO
20161222 Corey Chang SR 新申請用料
JD_CON
D3705
/EMI@
YSESD05.0CT5G
GND_AUDIO
Add C6647, C6648 for EMI (8/19)
C3706
0.1UF/16V
/EMI@
C3705
0.1UF/16V
/EMI@
GND
0317-1 EMI

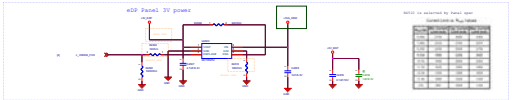
1112-1 Dean

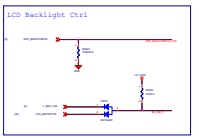
Audio Speaker

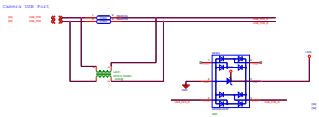


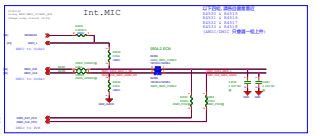
Change to 1000pF 4/21
Mount C3904~C3906 (7/9)

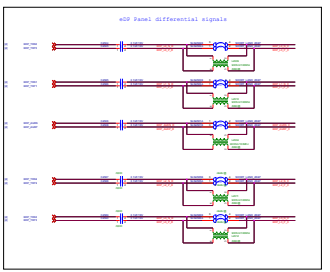
eDP (LVDS) Panel

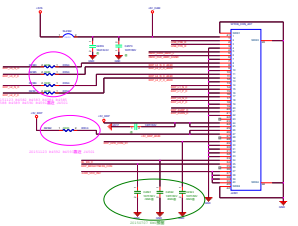




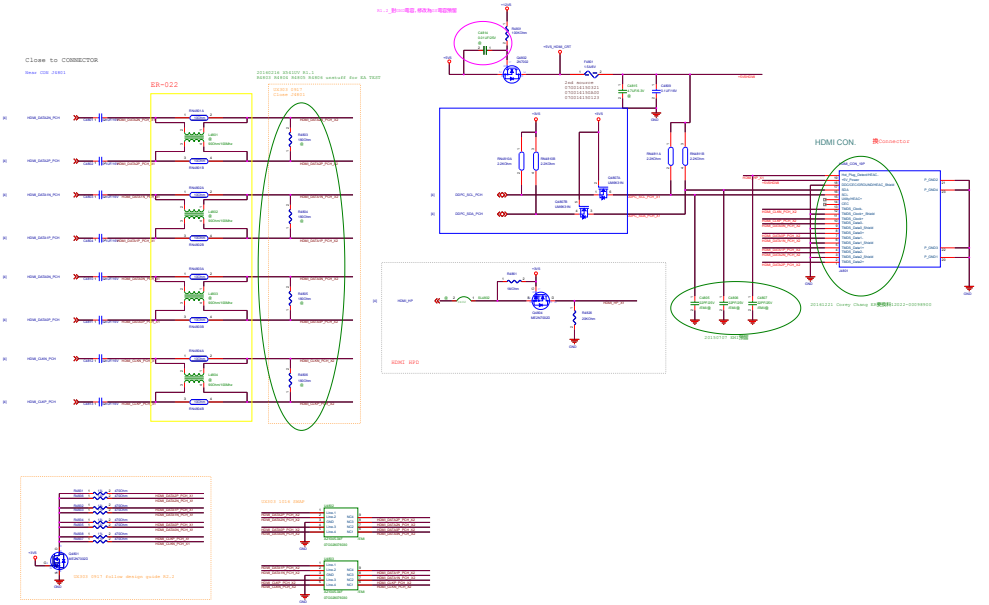




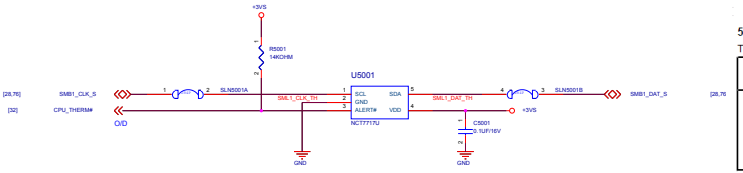




HDMI type-A



CPU Thermal Sensor



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

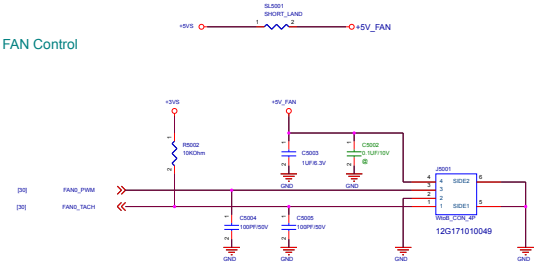
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

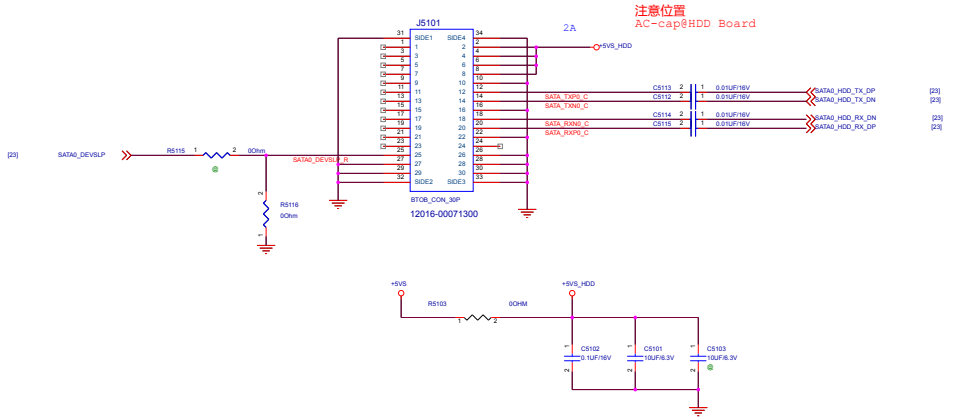
PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

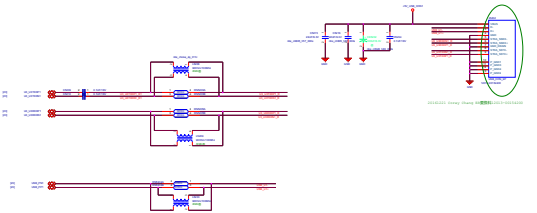
----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS
Avoid FSB,Power

DC FAN Control

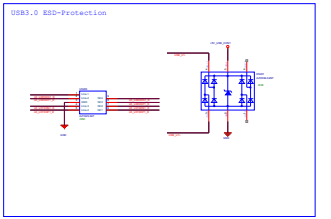



注意位置
AC-cap@HDD Board
J5101
2A
+5VS_HDD
SIDE1
SIDE4
SIDE2
SIDE3
BTOB_CON_30P
12016-00071300
[23]
SATA0_DEVSLP
R5115
0Ohm
SATA0_DEVSLP_R
R5116
0Ohm
SATA_TXP0_C
SATA_TXN0_C
SATA_RXN0_C
SATA_RXP0_C
C5113
C5112
C5114
C5115
0.01UF/16V
SATA0_HDD_TX_DP
SATA0_HDD_TX_DN
SATA0_HDD_RX_DN
SATA0_HDD_RX_DP
+5VS
R5103
0OHM
+5VS_HDD
C5102
0.1UF/16V
C5101
10UF/6.3V
C5103
10UF/6.3V

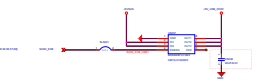
USB3.0_Port 0



USB3.0 ESD-Protection

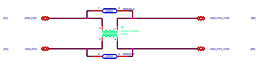


USB3.0 port 0 Power SW for Power Protect

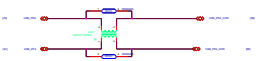


TO IO BD

USB2.0_Port 3

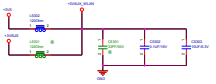


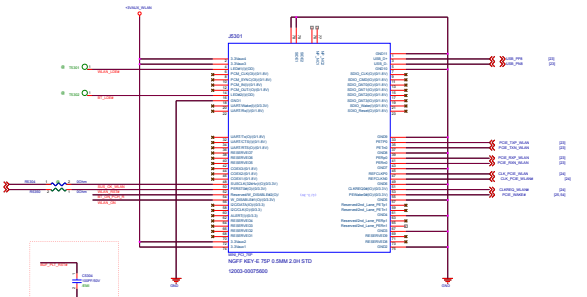
USB2.0_Port 4

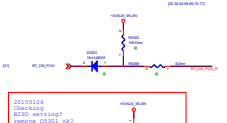


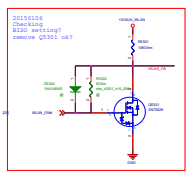
USB2.0 port 0 Power SW for Power Protect

WLAN con.

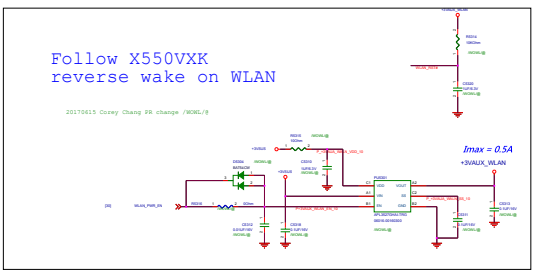


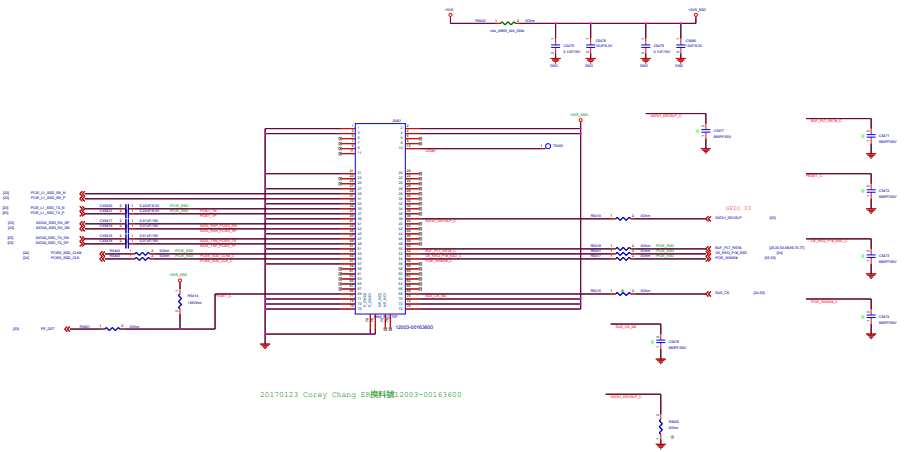




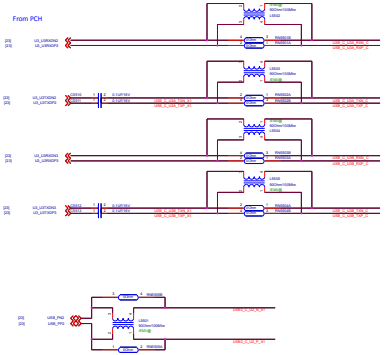


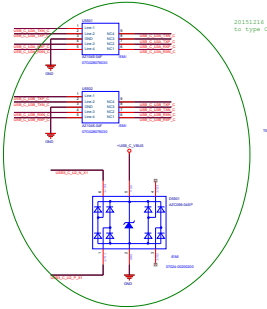
www.teknisi-indonesia.com

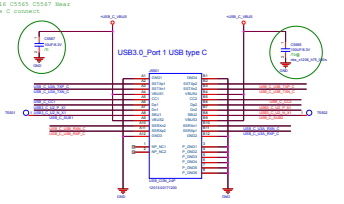


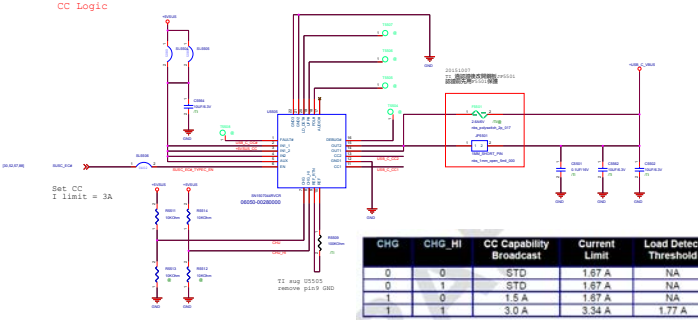


20170123 Corey Chang EM換料號12003-00163600



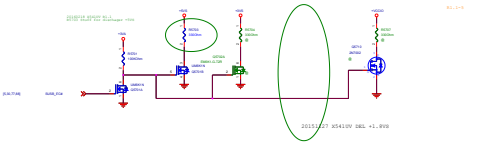


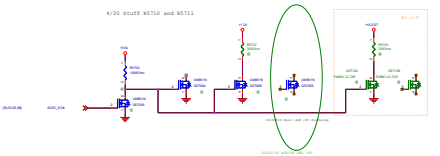


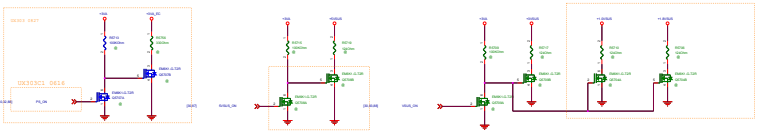


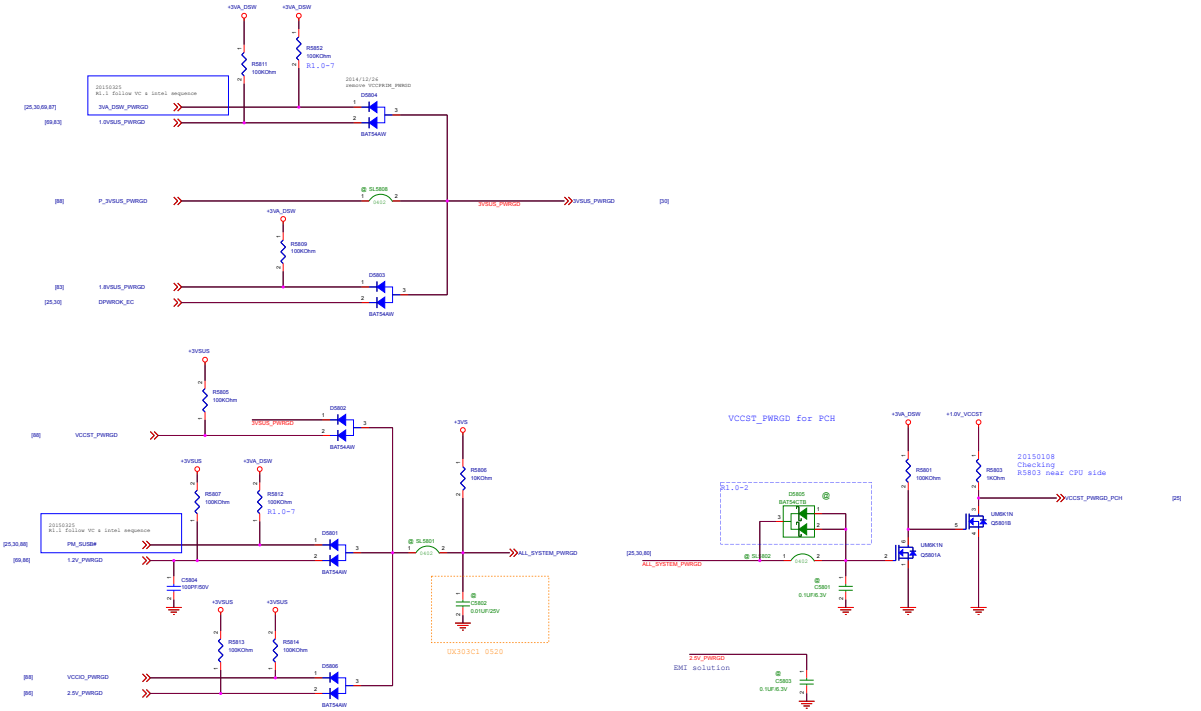
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

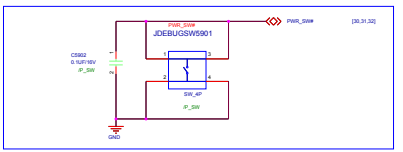
Main Board

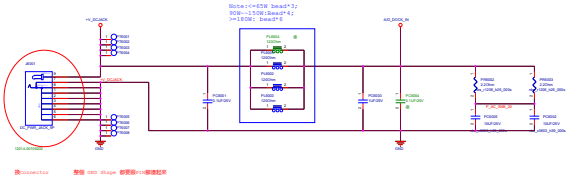




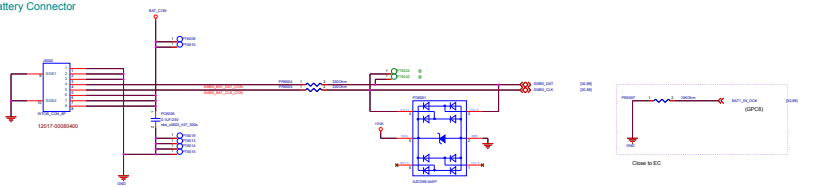



+3VA_DSW
+3VA_DSW
R5811
100KOhm
R5852
100KOhm
R1.0-7
20150325
R1.1 follow VC & intel sequence
3VA_DSW_PWRGD
1.0VSUS_PWRGD
[25,30,69,87]
[69,83]
2014/12/24
remove VCCPKDK_PWRGD
D5804
BAT54AW
SL5806
3VSUS_PWRGD
P_3VSUS_PWRGD
[88]
[30]
R5809
100KOhm
D5803
BAT54AW
1.8VSUS_PWRGD
DPWROK_EC
[83]
[25,30]
+3VSUS
R5805
100KOhm
D5802
BAT54AW
VCCST_PWRGD
[88]
+3VS
R5806
10KOhm
+3VSUS
+3VA_DSW
R5807
100KOhm
R5812
100KOhm
R1.0-7
20150325
R1.1 follow VC & intel sequence
PM_SUSB#
1.2V_PWRGD
[25,30,88]
[69,86]
D5801
BAT54AW
SL5801
ALL_SYSTEM_PWRGD
C5804
100PF/50V
C5802
0.01UF/25V
UX303C1 0520
+3VSUS
+3VSUS
R5813
100KOhm
R5814
100KOhm
D5806
BAT54AW
VCCID_PWRGD
2.5V_PWRGD
[68]
[65]
VCCST_PWRGD for PCH
+3VA_DSW
+1.0V_VCCST
R1.0-2
D5805
BAT54CTB
R5801
100KOhm
R5803
1KOhm
20150108
Checking
R5803 near CPU side
VCCST_PWRGD_PCH
[25]
UM6K1N
Q5801B
UM6K1N
Q5801A
[25,30,80]
ALL_SYSTEM_PWRGD
SL5802
C5801
0.1UF/6.3V
2.5V_PWRGD
EMI solution
C5803
0.1UF/6.3V


PWR_SW#
JDEBUGSW5901
PWR_SW#
[30,31,32]
C5902
0.1UFI 16V
P_SW
SW_4P
P_SW
GND

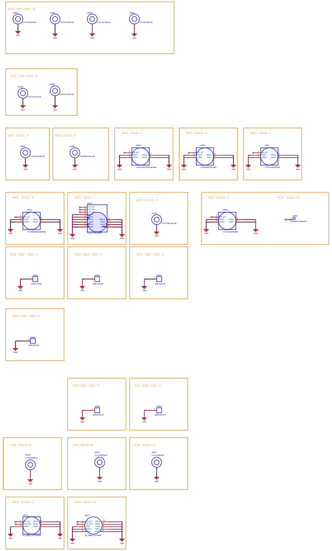


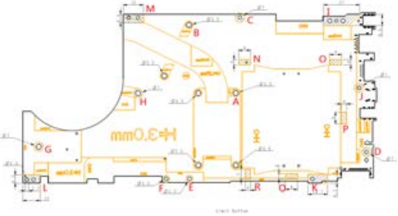
Battery Connector

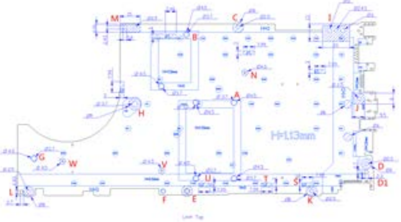


Pin define should be checked after battery team confirm

Pin Seq.	Name	Description	Remark
1	P-	Battery pack negative terminal	GND
2	P-	Battery pack negative terminal	GND
3	P-	Battery pack negative terminal	GND
4	SMBD	Serial data input	SMBD
5	SMBC	Serial clock input	SMBC
6	P+	Battery pack positive terminal	Output voltage
7	P+	Battery pack positive terminal	Output voltage
8	P+	Battery pack positive terminal	Output voltage

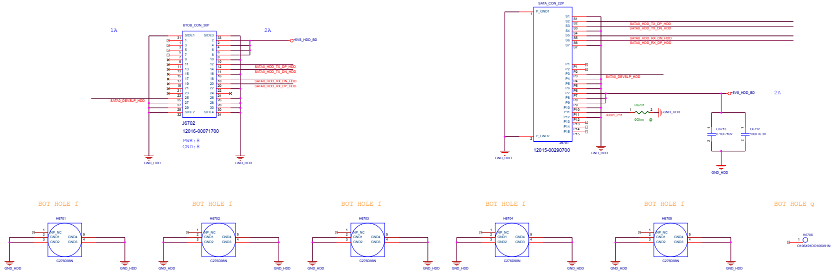

BOT CPU NUT A
BOT CPU NUT B
BOT HOLE F
BOT HOLE E
BOT HOLE J
BOT HOLE H
BOT HOLE C
BOT HOLE K
BOT HOLE I
BOT HOLE G
BOT HOLE D
BOT HOLE D1
BOT EMI PAD O
BOT EMI PAD P
BOT EMI PAD Q
BOT EMI PAD R
TOP EMI PAD T
TOP EMI PAD U
TOP HOLE X
TOP HOLE W
TOP HOLE V
BOT HOLE L
BOT HOLE M

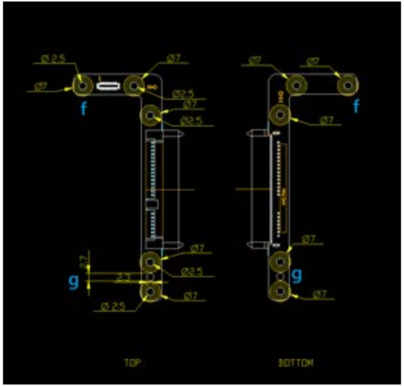

H=3.0mm


H=1.13mm

MB TO HDD BD

SATA HDD

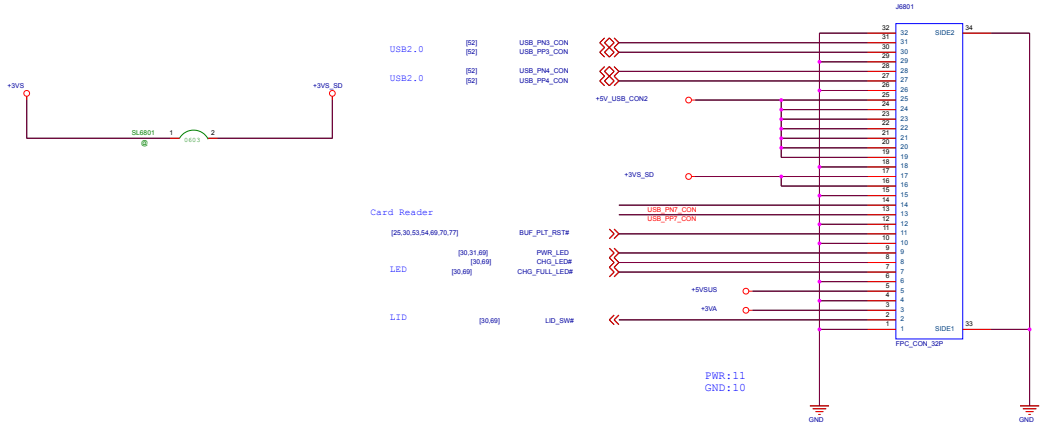




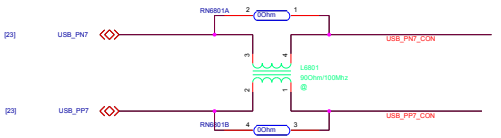
<Variant Name>

ASUSTeK COMPUTER INC.	Title : HDD_BD	
	Engineer: EE	
Size: Custom	Project Name: X510UA/UQ	Rev: 1.0
Date: Tuesday, July 11, 2017	Sheet 67 of 103	

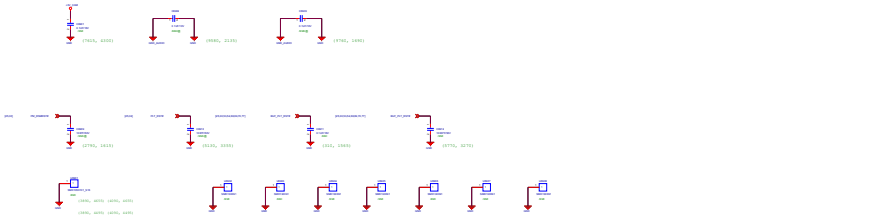
12018-00630300



USB2.0_Port 7 for Card Reader

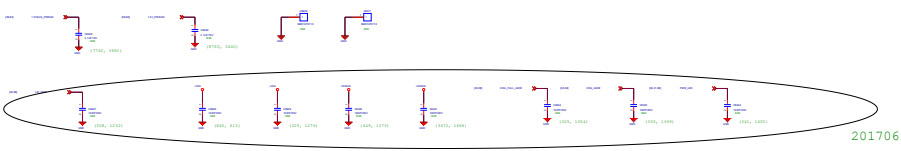


SR

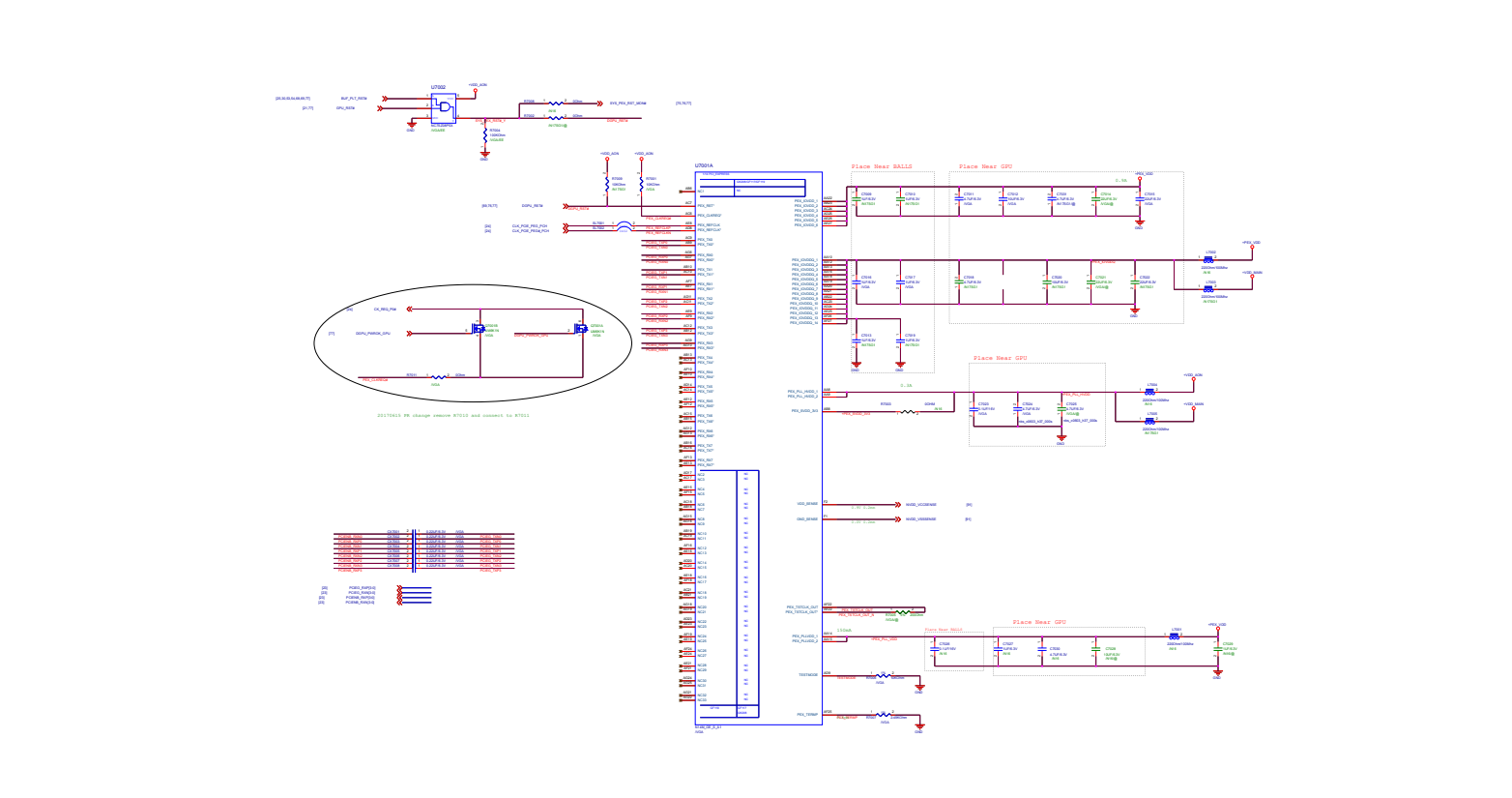


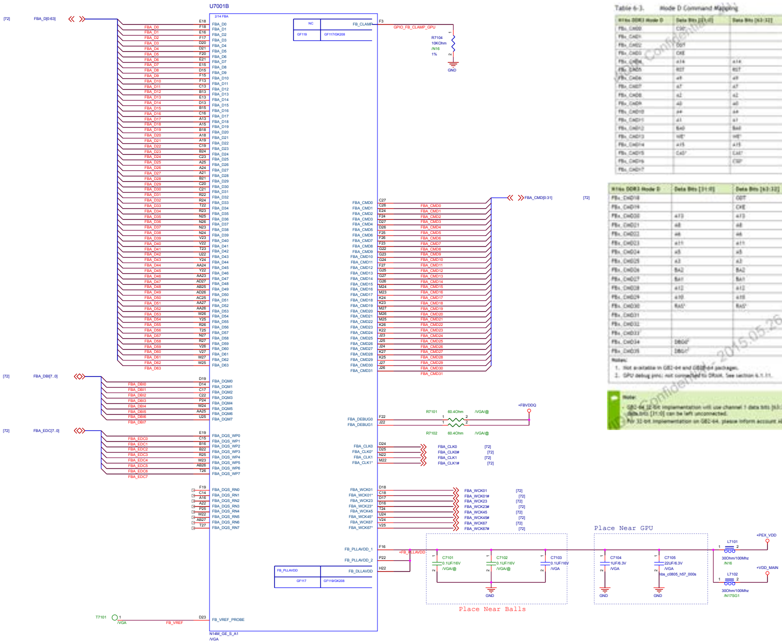
ER

PR



20170615 Corey Chang EMI add


Place Near BALLS
Place Near GPU
Place Near GPU
Place Near GPU
20170615 PR change remove R7010 and connect to R7011



BOM Mount: 02004-00300400

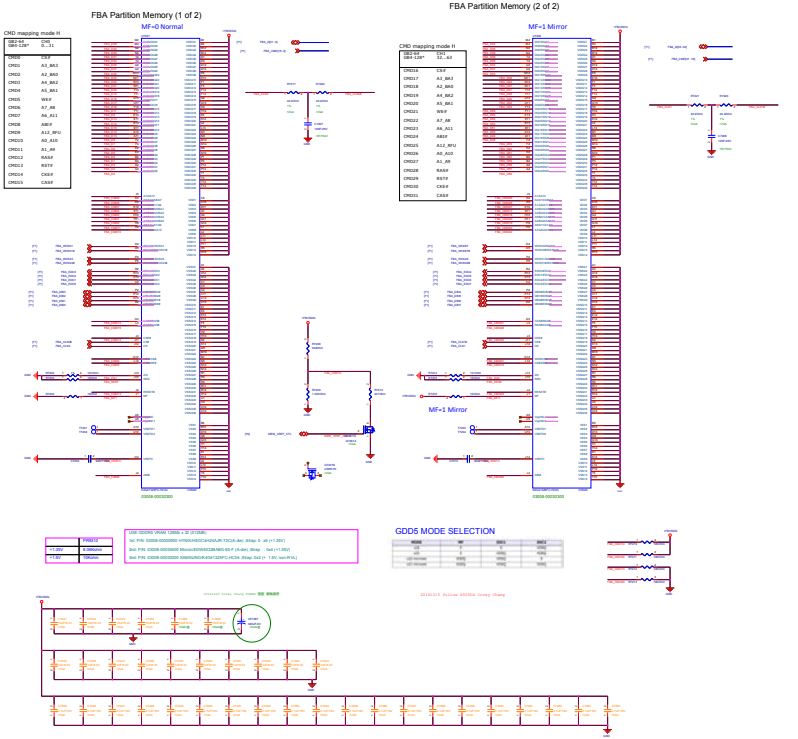
Table 6-3. Mode D Command Mapping

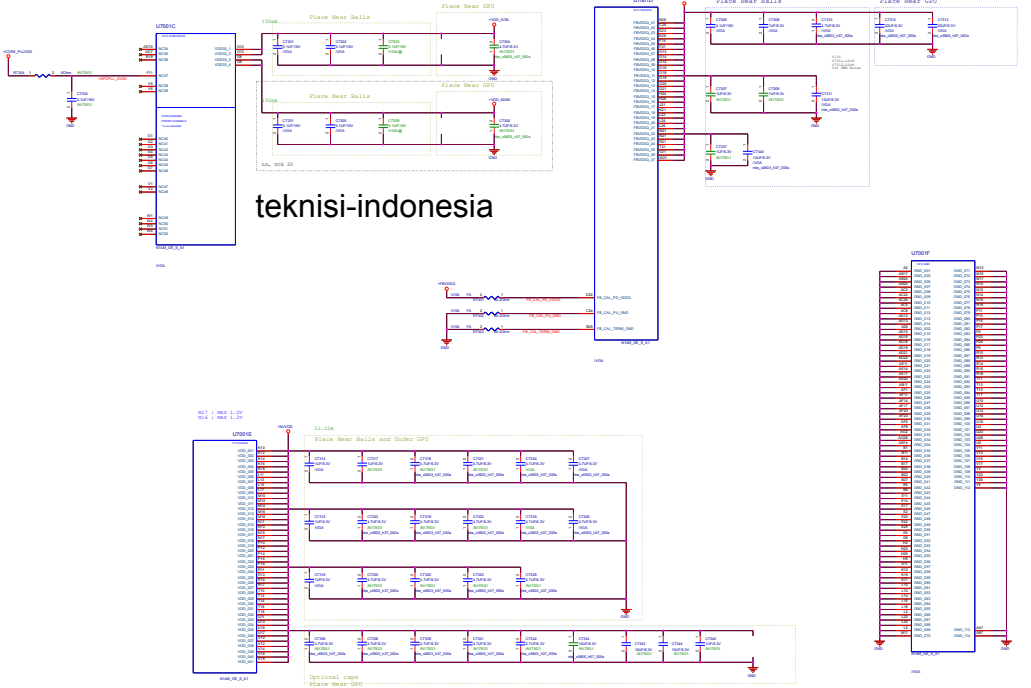
x16s DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD00	CS0*	
FBx_CMD01		
FBx_CMD02	ODT	
FBx_CMD03	CKE	
FBx_CMD04	a14	a14
FBx_CMD05	RST	RST
FBx_CMD06	a9	a9
FBx_CMD07	a7	a7
FBx_CMD08	a2	a2
FBx_CMD09	a0	a0
FBx_CMD10	a4	a4
FBx_CMD11	a1	a1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	a15	a15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		

x16s DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	a13	a13
FBx_CMD21	a8	a8
FBx_CMD22	a6	a6
FBx_CMD23	a11	a11
FBx_CMD24	a5	a5
FBx_CMD25	a3	a3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	a12	a12
FBx_CMD29	a10	a10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

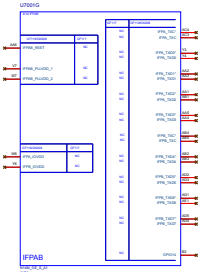
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins: not connected to DRAM. See section 6.1.11.

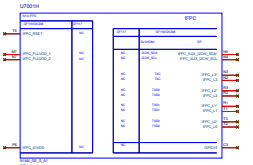
Note:
- GB2-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel 0 data bits [31:0] can be left unconnected.
- For 32-bit implementation on GB2-64, please inform account AE for VBIOS support.

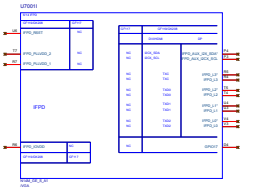

FBA Partition Memory (1 of 2)
MF=0 Normal
CMD mapping mode H
FBA Partition Memory (2 of 2)
MF=1 Mirror
CMD mapping mode H
MF=1 Mirror
GDD5 MODE SELECTION


U7001C
U7001D
U7001E
U7001F
Place Near Balls
Place Near GPU
Place Near Balls and Under GPU
Optional caps
Place Near GPU
teknisi-indonesia

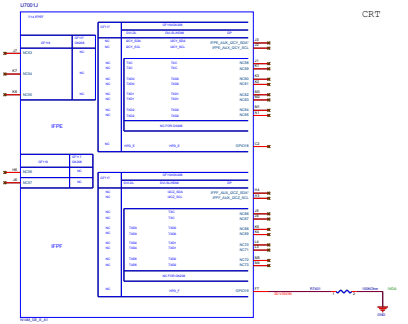
LVDS


U7001G
IFPAB
IVGA


U7001H
IFPC
IVGA


U7001I
IFPD
IVGA

CRT


U7001J
IFPE
IFPF
IVGA

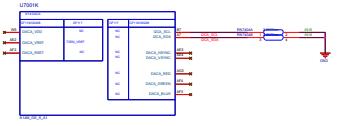

U7001K
IVGA

Table 4. N17S-G1 GDDR5 Recommended Memories

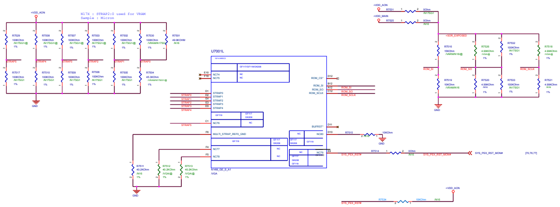
Memory Density	Allowed Memory Configuration	FBVDDQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Data Cycle Alert	Spd Plan	Status
8 Gb	[illegible]	1.35V	Samsung	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Full	Production candidate
			Micron	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Full	Production candidate
			Hynix	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Full	Post production candidate
4 Gb	[illegible]	1.35V	Hynix	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Full	Production candidate
			Samsung	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Full	Production candidate
			Micron	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Full	Post production candidate

Notes:

1. For N17S-G1, the maximum allowable [illegible]

03008-00050300
03008-00050100

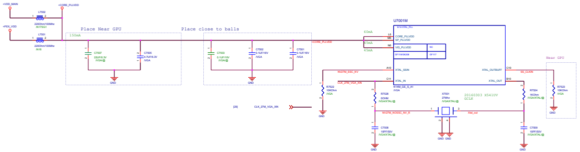
P/N	Type/Config	VRAM	RAM_CFG	BI
03008-00050300	GDDR5 256M*32 6.0 1.5V FBGA170	MICRON/MT51J256M32HF-60:A	0x1	PD_10K
03008-00050100		SAMSUNG/K4G80325FB-HC03	0x0	PD_4.99K



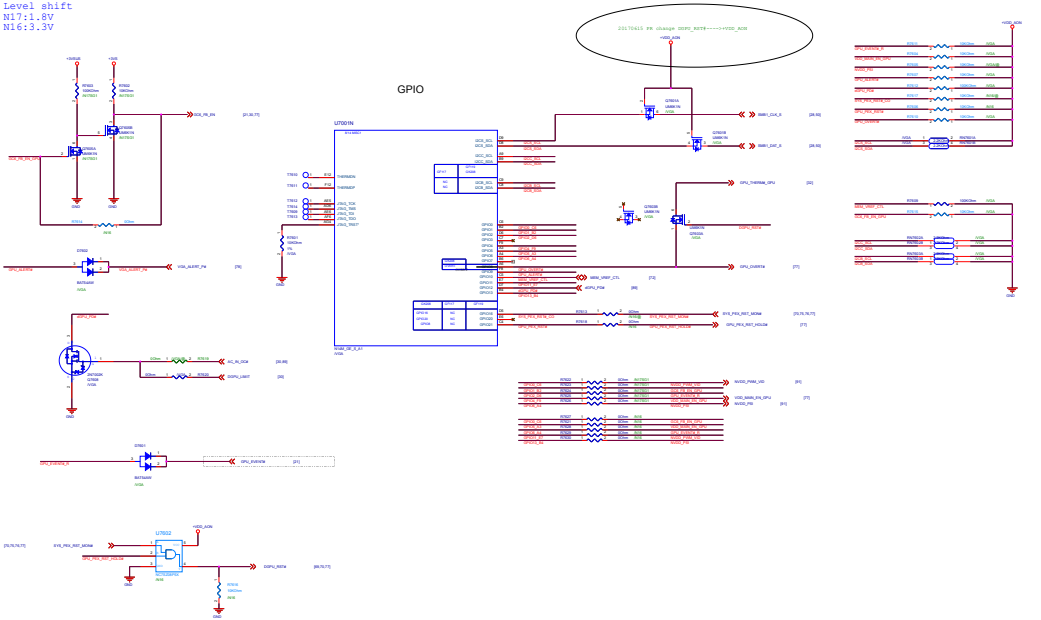
VG BOM 帶入主料時記得要加2nd Source

4.99K = 10G212499114010
10K = 10G212100214010
15K = 10G212150214030
20K = 10G212200214030
24.9K = 10G212249214010
30.1K = 10G212301214010
34.8K = 10G212348214010
45.3K = 10G212453214010
49.9K = 10G212499214010

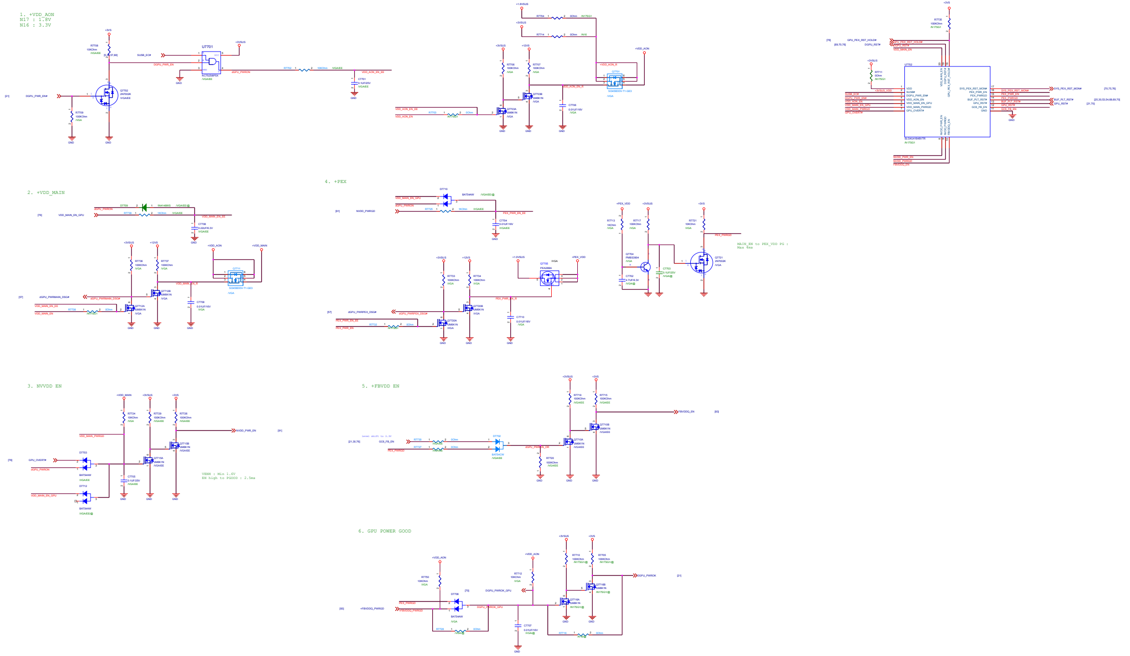
Xtal



Level shift
N17:1.8V
N16:3.3V

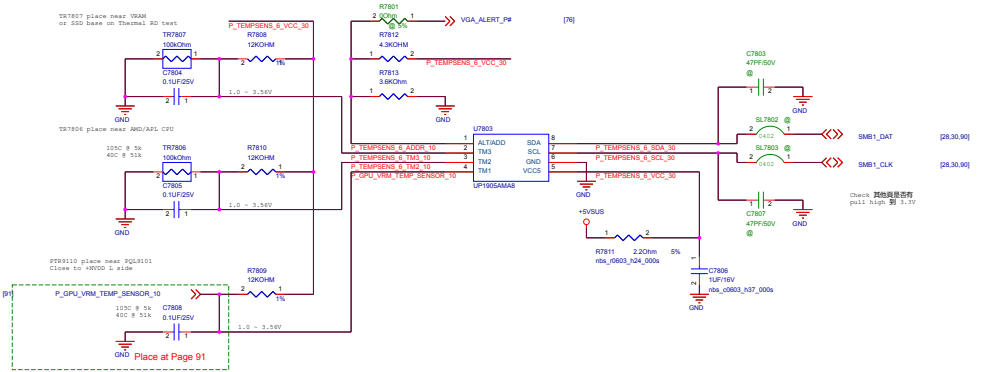


dGPU Power Sequence

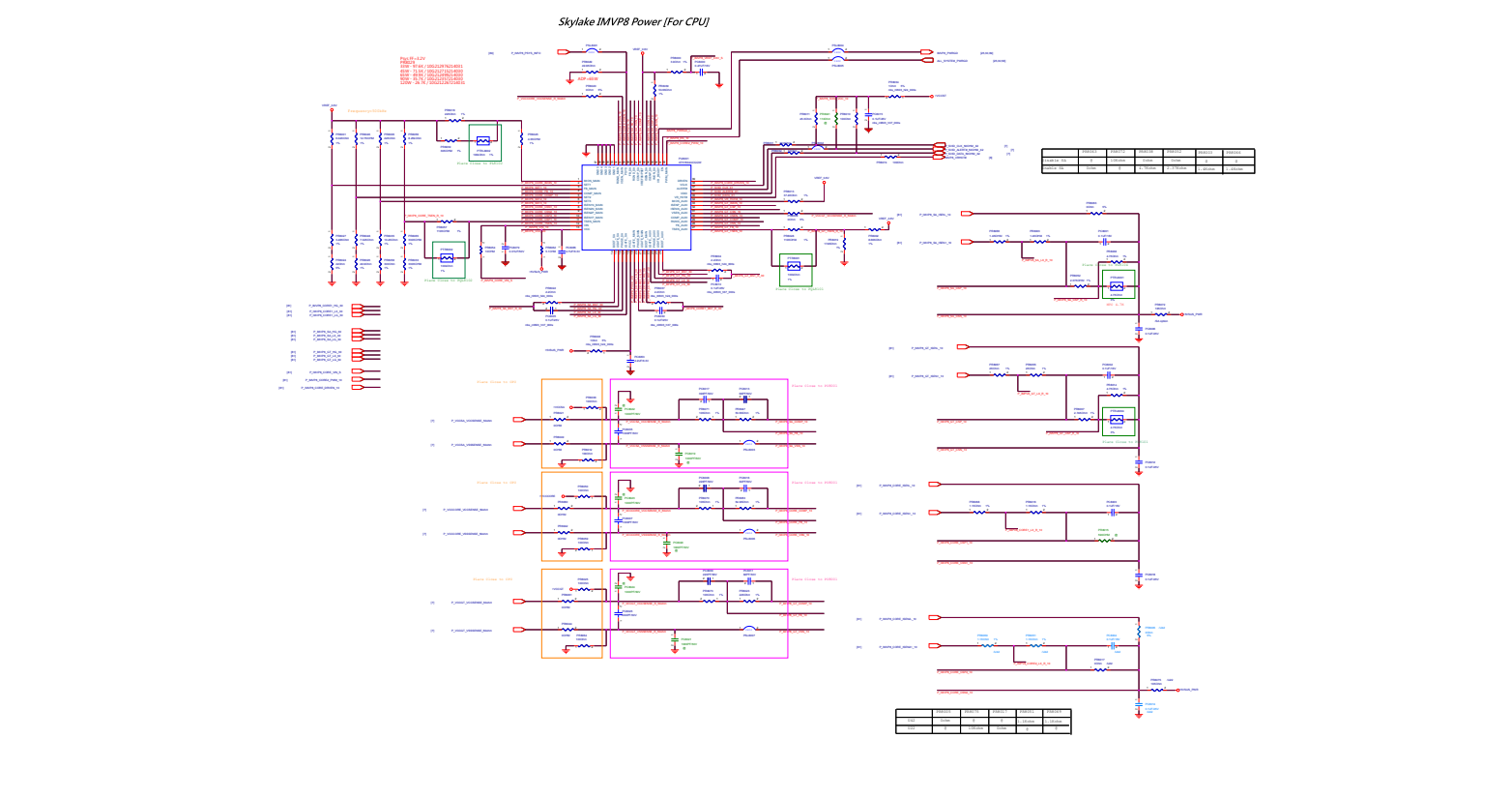


Address Selection Table

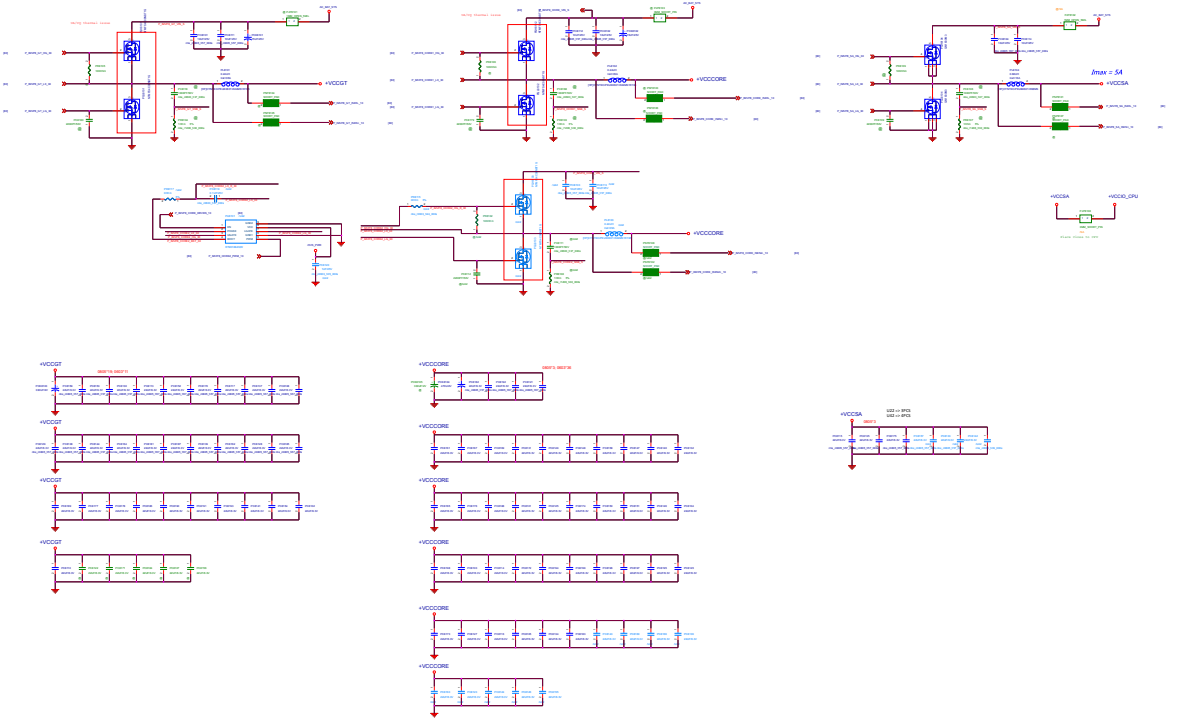
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7812	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7813	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k



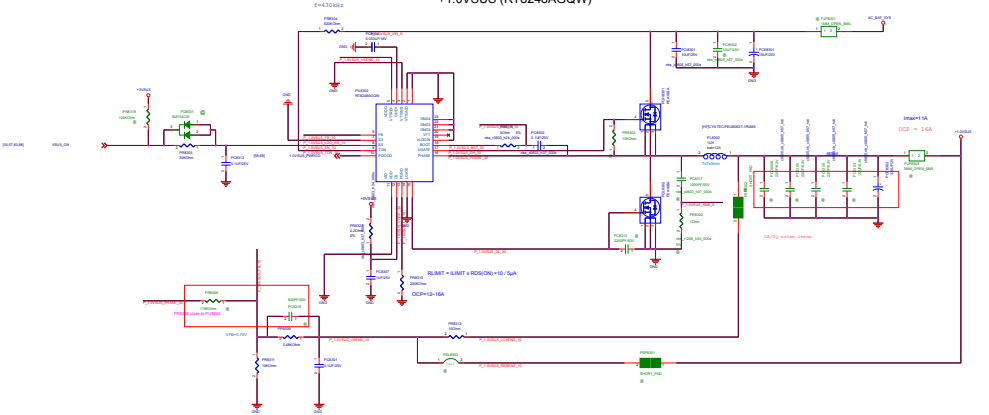
Skylake IMVP8 Power [For CPU]



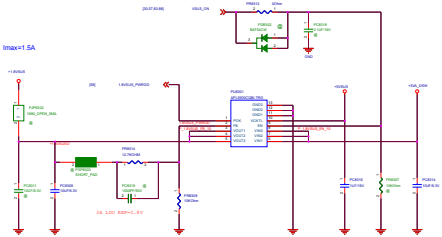
Kaby Lake-U IMVP8 Power (2) [For CPU]



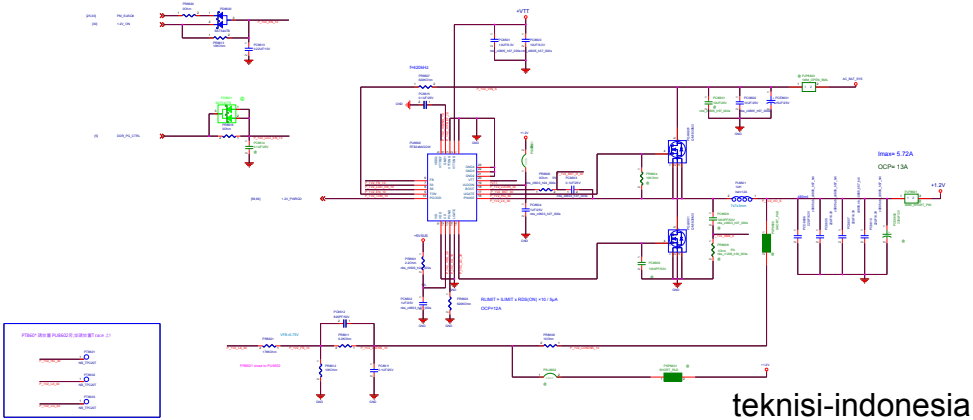
+1.0VSUS (RT8248AGQW)



+1.8VSUS [For PCH]

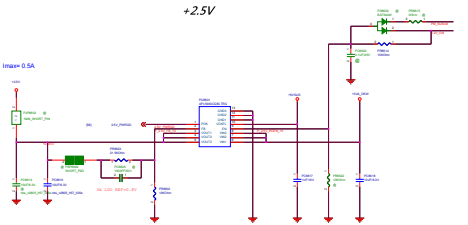


+1.2V / +VTT / +2.5V[For Memory]

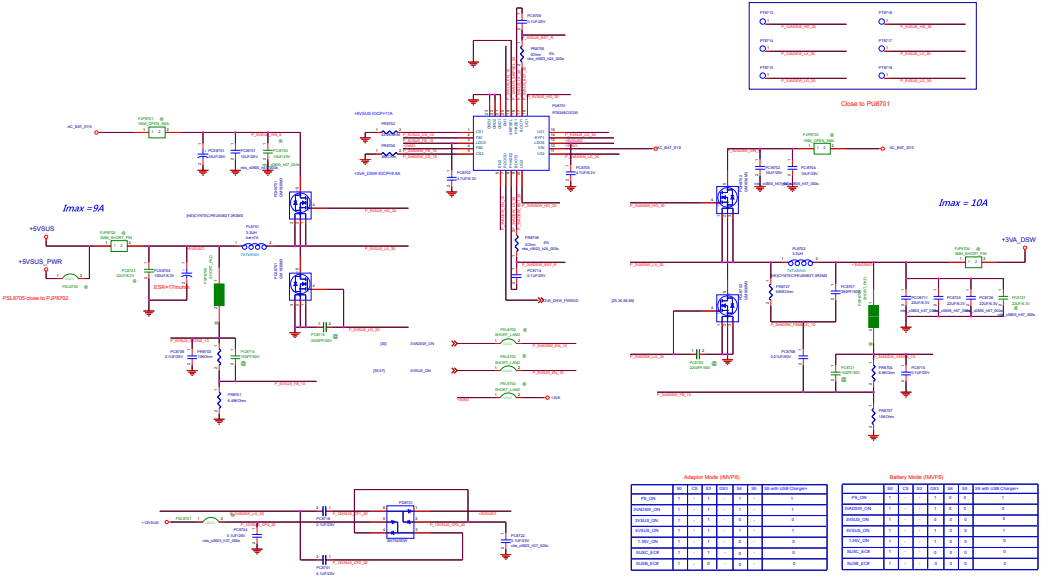


teknisi-indonesia

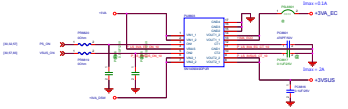
+2.5V

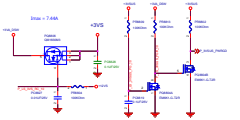


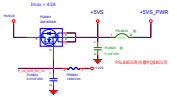
+3VA_DSW / +5VSUS [System Power]

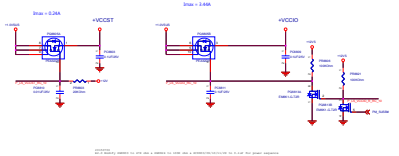


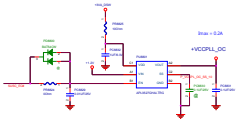
Load Switch

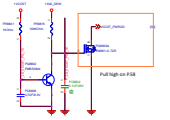


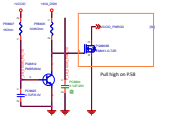






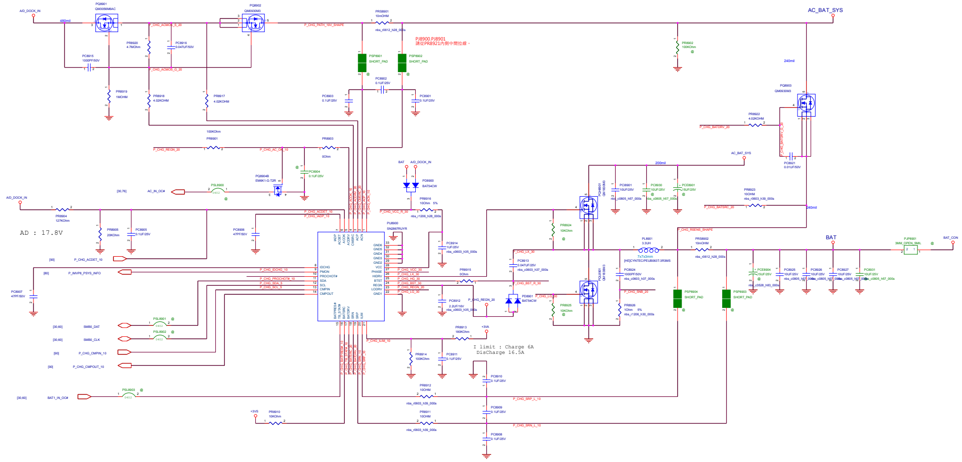




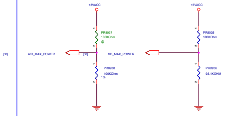


Main Board

PRS8901	<=40W	<=120W	>=120W
	20m	10m	5m
	10125-0004m000	10125-0001m100	10G21DR00515111

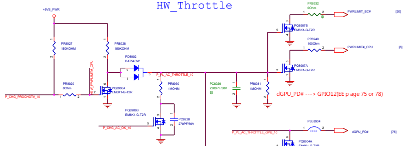


Adaptor select
total power = 90% ADP



Adaptor select			
		N Series	G Series
PR8921		10m	5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle



AC limit = 103% ADP
Bat limit = byte 7 x 1.7

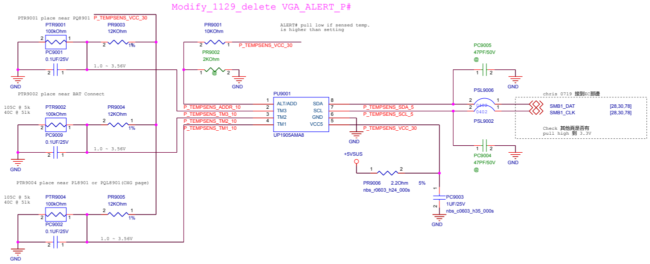
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

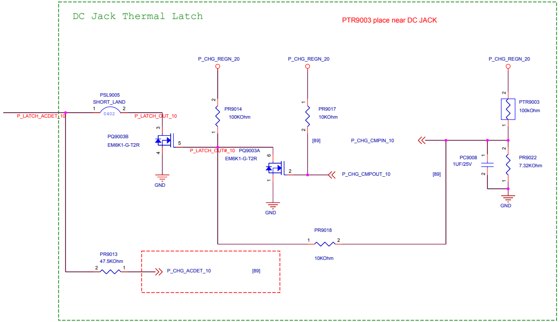
Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

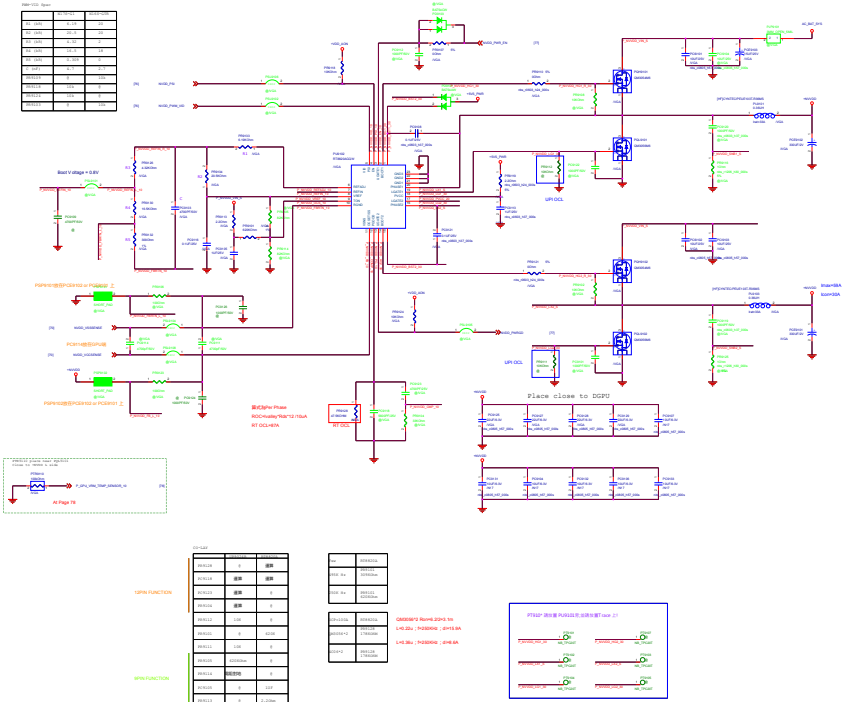
Modify_1129_delete VGA_ALERT_P#



DC Jack Thermal Latch

PTR9003 place near DC JACK

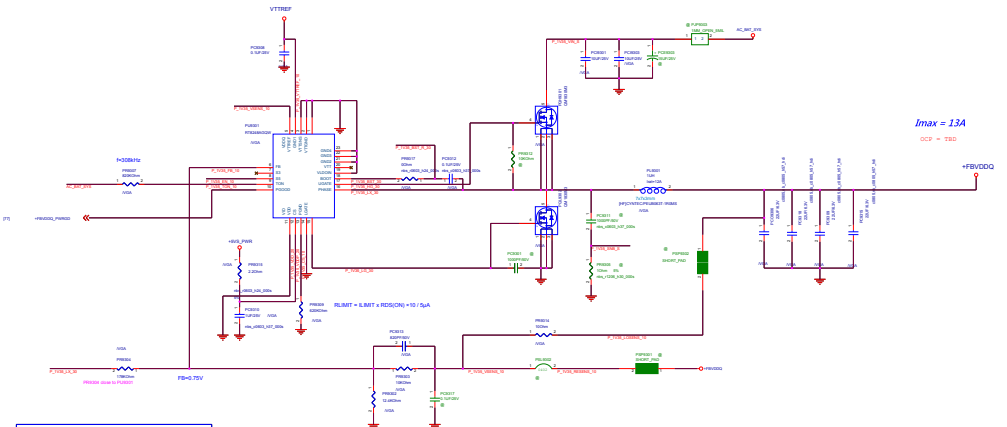


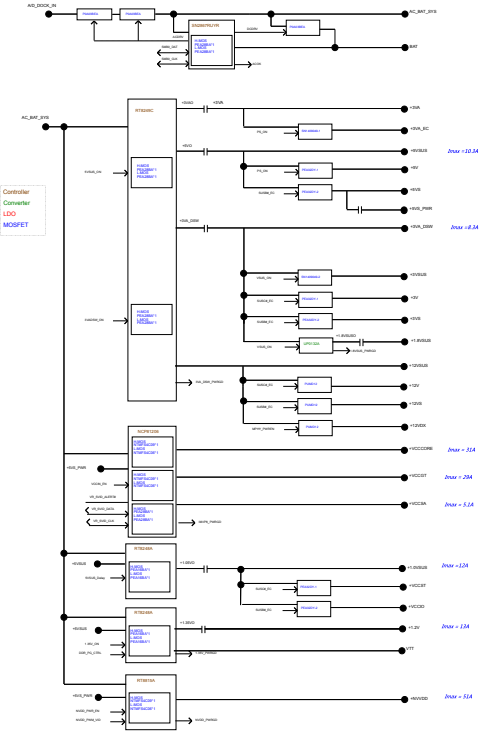


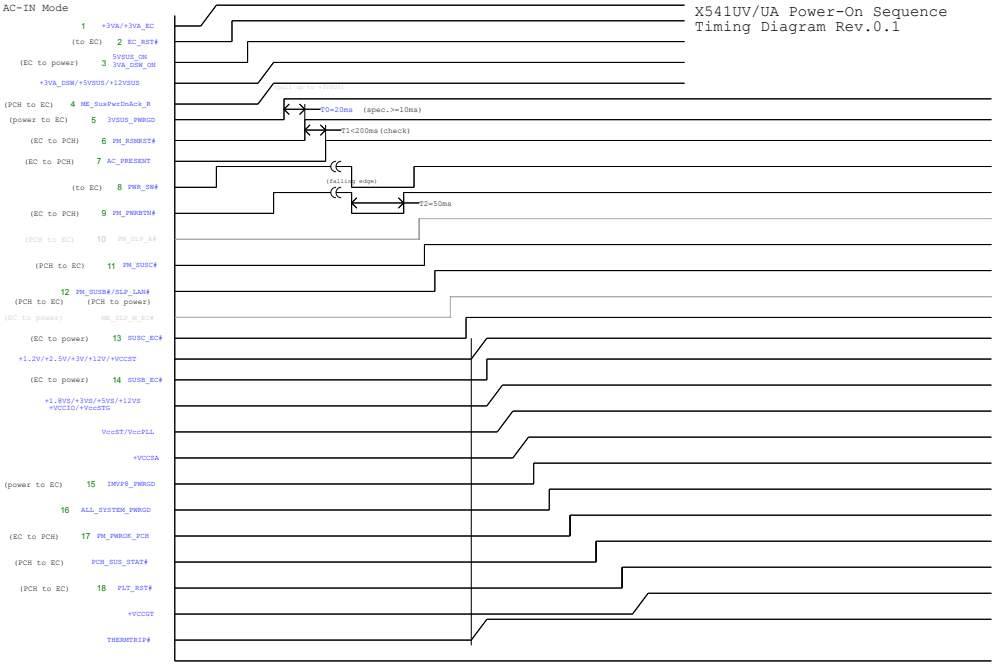
S3 And S5 Truth Table

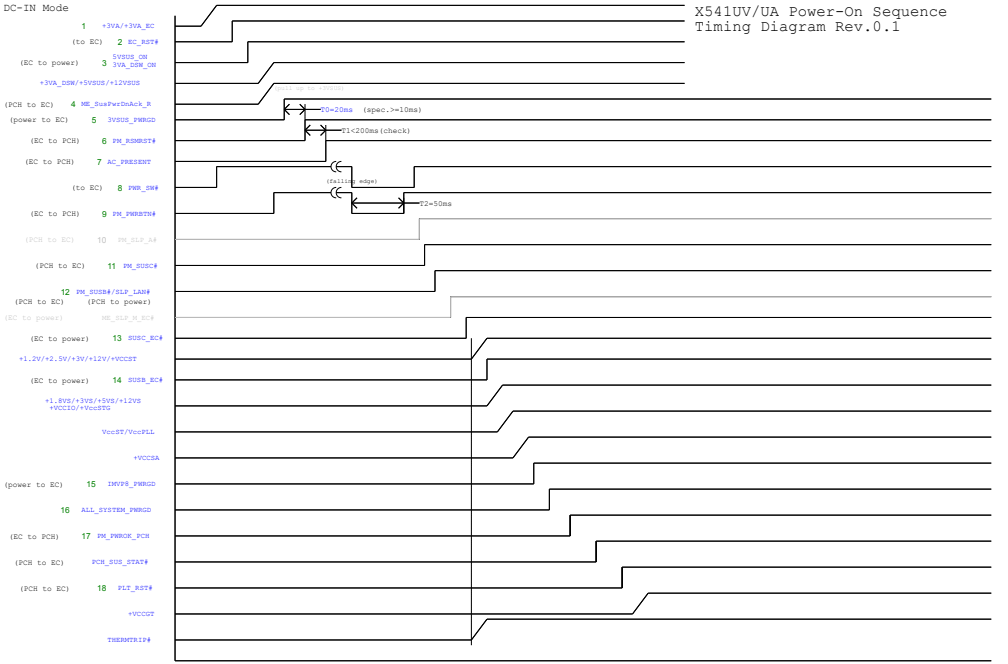
State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

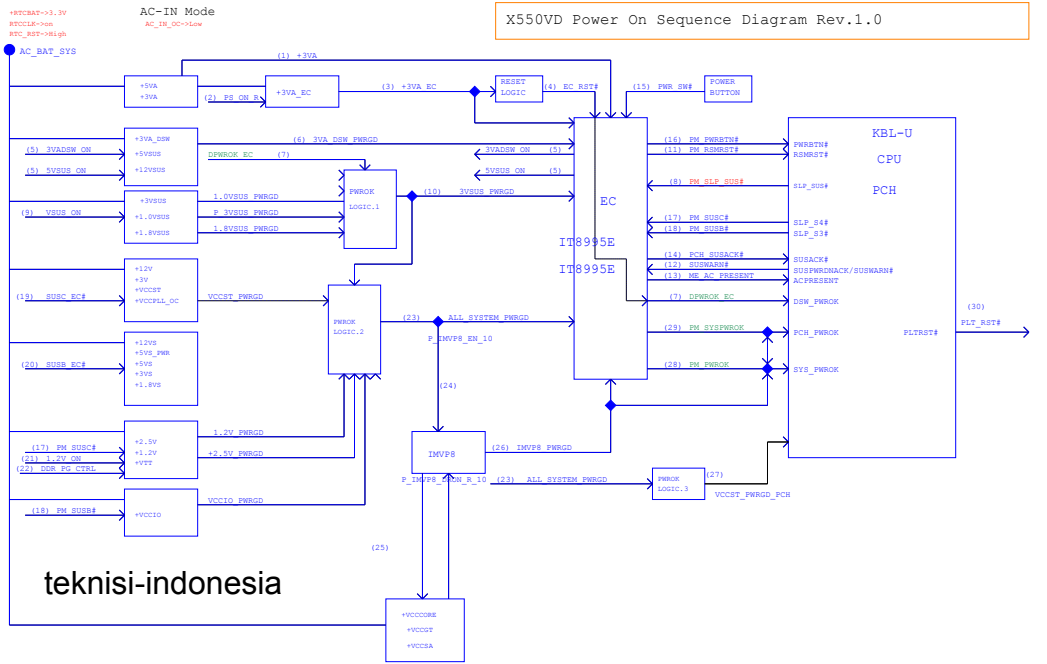
+1.35VSG




AC_BAT_SYS
Controller
Converter
LDO
MOSFET
Imax =10.3A
Imax =8.3A
Imax =31A
Imax = 29A
Imax = 5.1A
Imax =12A
Imax = 13A
Imax = 51A


AC-IN Mode
X541UV/UA Power-On Sequence
Timing Diagram Rev.0.1
1 +3VA/+3VA_EC
(to EC) 2 EC_RST#
(EC to power) 3 5VSUS_ON 3VA_DSW_ON
+3VA_DSW/+5VSUS/+12VSUS
(PCH to EC) 4 ME_SusPwrDnAck_R
(power to EC) 5 3VSUS_PWRGD
(EC to PCH) 6 PM_RSMRST#
(EC to PCH) 7 AC_PRESENT
(to EC) 8 PWR_SW#
(EC to PCH) 9 PM_PWRBTN#
(PCH to EC) 10 PM_SLP_A#
(PCH to EC) 11 PM_SUSC#
12 PM_SUSB#/SLP_LAN#
(PCH to EC) (PCH to power)
(EC to power) ME_SLP_M_EC#
(EC to power) 13 SUSC_EC#
+1.2V/+2.5V/+3V/+12V/+VCCST
(EC to power) 14 SUSB_EC#
+1.8VS/+3VS/+5VS/+12VS
+VCCIO/+VccSTG
VccST/VccPLL
+VCCSA
(power to EC) 15 IMVP8_PWRGD
16 ALL_SYSTEM_PWRGD
(EC to PCH) 17 PM_PWROK_PCH
(PCH to EC) PCH_SUS_STAT#
(PCH to EC) 18 PLT_RST#
+VCCGT
THERMTRIP#
T0=20ms (spec.>=10ms)
T1<200ms(check)
(falling edge)
T2=50ms


X541UV/UA Power-On Sequence
Timing Diagram Rev.0.1
DC-IN Mode
1 +3VA/+3VA_EC
(to EC) 2 EC_RST#
(EC to power) 3 5VSUS_ON 3VA_DSW_ON
+3VA_DSW/+5VSUS/+12VSUS
(PCH to EC) 4 ME_SusPwrDnAck_R
(power to EC) 5 3VSUS_PWRGD
(EC to PCH) 6 PM_RSMRST#
(EC to PCH) 7 AC_PRESENT
(to EC) 8 PWR_SW#
(EC to PCH) 9 PM_PWRBTN#
(PCH to EC) 10 PM_SLP_A#
(PCH to EC) 11 PM_SUSC#
12 PM_SUSB#/SLP_LAN#
(PCH to EC) (PCH to power)
(EC to power) ME_SLP_M_EC#
(EC to power) 13 SUSC_EC#
+1.2V/+2.5V/+3V/+12V/+VCCST
(EC to power) 14 SUSB_EC#
+1.8VS/+3VS/+5VS/+12VS
+VCCIO/+VccSTG
VccST/VccPLL
+VCCSA
(power to EC) 15 IMVP8_PWRGD
16 ALL_SYSTEM_PWRGD
(EC to PCH) 17 PM_PWROK_PCH
(PCH to EC) PCH_SUS_STAT#
(PCH to EC) 18 PLT_RST#
+VCCGT
THERMTRIP#
T0=20ms (spec.>=10ms)
T1<200ms(check)
(falling edge)
T2=50ms


X550VD Power On Sequence Diagram Rev.1.0
AC-IN Mode
+RTCBAT->3.3V
RTCCLK->on
RTC_RST->High
AC_IN_OC->Low
AC_BAT_SYS
(1) +3VA
+5VA
+3VA
(2) PS_ON_E
+3VA_EC
(3) +3VA_EC
RESET LOGIC
(4) EC_RST#
(15) PWR_SW#
POWER BUTTON
+3VA_DSW
+5VSUS
+12VSUS
(5) 3VADSW_ON
(5) 5VSUS_ON
(6) 3VA_DSW_PWRGD
DPWROK_EC (7)
3VADSW_ON (5)
5VSUS_ON (5)
+3VSUS
+1.0VSUS
+1.8VSUS
(9) VSUS_ON
1.0VSUS_PWRGD
P_3VSUS_PWRGD
1.8VSUS_PWRGD
PWROK LOGIC.1
(10) 3VSUS_PWRGD
EC
IT8995E
IT8995E
(16) PM_PWRBTN#
(11) PM_RSMRST#
(8) PM_SLP_SUS#
(17) PM_SUSC#
(18) PM_SUSB#
(14) PCH_SUSACK#
(12) SUSWARN#
(13) ME_AC_PRESENT
(7) DPWROK_EC
(29) PM_SYSPWROK
(28) PM_PWROK
KBL-U
CPU
PCH
PWRBTN#
RSMRST#
SLP_SUS#
SLP_S4#
SLP_S3#
SUSACK#
SUSPWRDNACK/SUSWARN#
ACPRESENT
DSW_PWROK
PCH_PWROK
SYS_PWROK
PLTRST#
(30)
PLT_RST#
+12V
+3V
+VCCST
+VCCPLL_OC
(19) SUSC_EC#
VCCST_PWRGD
PWROK LOGIC.2
(23) ALL_SYSTEM_PWRGD
P_IMVP8_EN_10
+12VS
+5VS_PWR
+5VS
+3VS
+1.8VS
(20) SUSB_EC#
(24)
+2.5V
+1.2V
+VTT
(17) PM_SUSC#
(21) 1.2V_ON
(22) DDR_PG_CTRL
1.2V_PWRGD
+2.5V_PWRGD
IMVP8
(26) IMVP8_PWRGD
P_IMVP8_PGN_R_10
(23) ALL_SYSTEM_PWRGD
PWROK LOGIC.3
(27)
VCCST_PWRGD_PCH
+VCCIO
(18) PM_SUSB#
VCCIO_PWRGD
(25)
+VCCCORE
+VCCGT
+VCCSA
teknisi-indonesia