Hellcat 13 Schematics
Tiger Lake - U/ LPPDR4X

2020-08-04
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Cover Page*		
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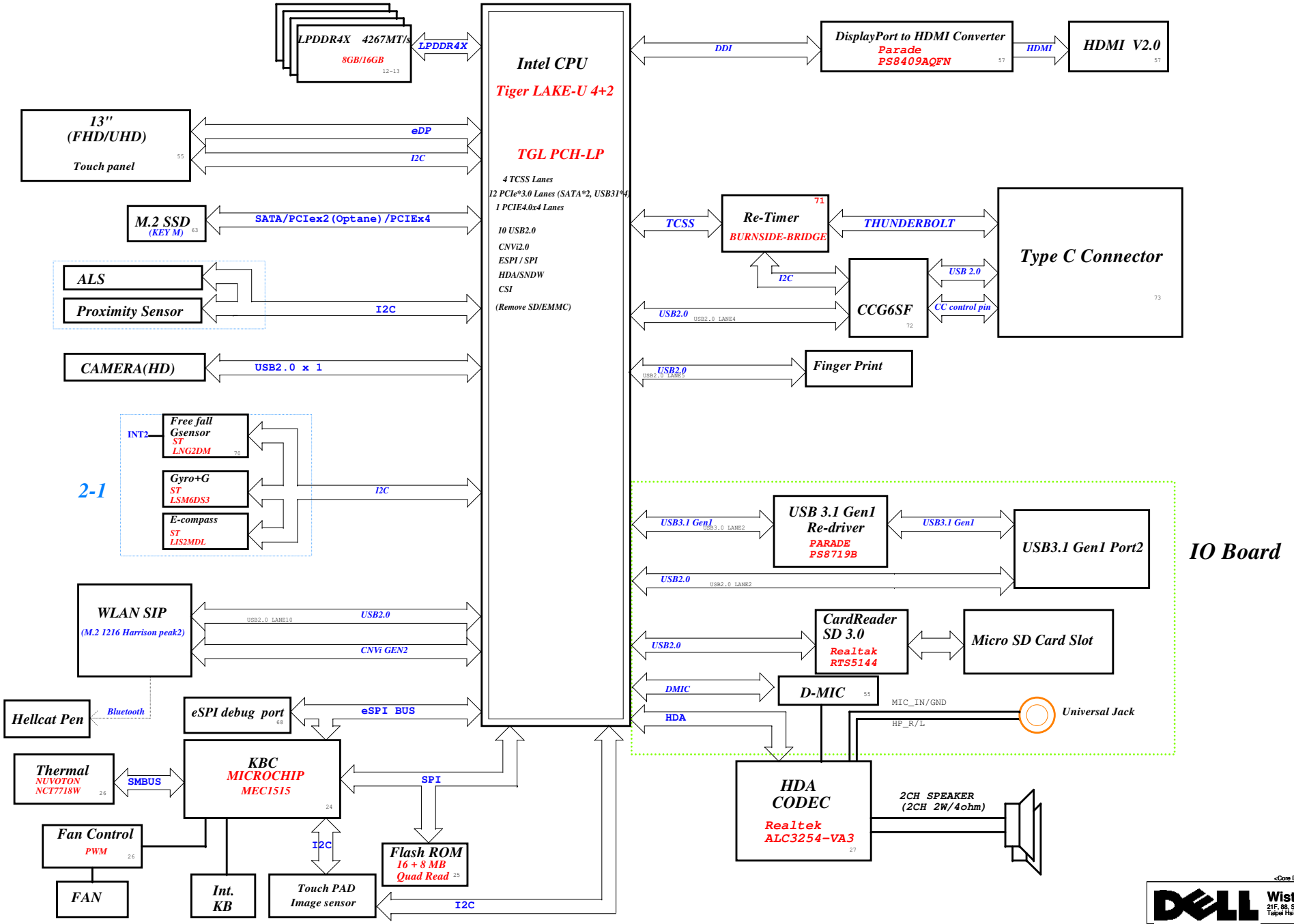
Hellcat 13 CPU 15W Block Diagram

Project code: 4PD0LB010001
PCB P/N: 19827
Revision: A00



<Core Design>

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Title: Block Diagram

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Follow Hellcat15 Upsell TGL

20191128(EVT)
Follow Nakia Shuri N7

1D05V_VCCSTG
R301 1KR2F-3-GP
EAR_N_TEST_NCTF
R309 1KR2J-1-GP DY

Follow Nakia Shuri N7

20191128(EVT)
Modify

1D05V_VCCSTG_TERM
R311 1 100R2F-L1-GP-U XDP_TDO_CPU
R308 1 DY 51R2J-2-GP XDP_PREQ#
RN302 XDP SRN51J-GP
XDP_TDI
XDP_TMS
XDP_TCLK R310 1 XDP 51R2J-2-GP
XDP_TRST# R312 1 DY 51R2J-2-GP
20191210(EVT)
Change RN304 -> R312
Layout request

24 PECI_CPU
15 DBG_PMODE
22,24,44,46,72 PROCHOT#_CPU
24,65 TOUCH_PAD_INTR#

21 MEM_CONFIG4
55 TOUCH_PANEL_PD#

1D05V_VCCSTG_TERM
R302 1 1KR2F-3-GP PROCHOT#_CPU

1D05V_VCCST
R304 1 1KR2F-3-GP THERMTRIP#_CPU
R307 1 1KR2F-3-GP CPU_CATERR
CPU_POPI_RCOMP R305 1 49D9R2F-GP
PCH_OPI_RCOMP R306 1 49D9R2F-GP

CATERR# Signal needs a 1Kohms Pull up resistor to VCCST domain. PDG (excel sheet need to update correct value from 49.9 Ohms to 1K Ohms) [WW37 MOW]

PROCHOT#_CPU R303 1 499R2F-2-GP

CPU1U 21 OF 21

CPU_CATERR	M7	CATERR#	
PECI_CPU	BK9	PECI	
PROCHOT#_CPU_R	E2	PROCHOT#	
THERMTRIP#_CPU	M5	THRMTRIP#	
CPU_POPI_RCOMP	CT39	PROC_POPIRCOMP	
PCH_OPI_RCOMP	CB9	PCH_OPIRCOMP	
	CW12	TP#CW12	
	CM39	TP#CM39	
DBG_PMODE	DF4	DBG_PMODE	
	DB42	GPP_B4/CPU_GP3	
TOUCH_PAD_INTR#	DB41	GPP_B3/CPU_GP2	
TOUCH_PANEL_PD#	DF8	GPP_E7/CPU_GP1	
	DU5	GPP_E3/CPU_GP0	
		EAR_N/EAR_N_TEST_NCTF	
	DF31	GPP_H2	
	DV32	GPP_H1	
	DW32	GPP_H0	
MEM_CONFIG4	DJ27	GPP_H19/TIME_SYNC0	

PROC_TRST#	K4	XDP_TRST# 1	TP309
PROC_TMS	B9	XDP_TMS 1	TP310
PROC_TDO	D12	XDP_TDO_CPU 1	TP311
PROC_TDI	A12	XDP_TDI 1	TP312
PROC_TCK	B6	XDP_TCLK 1	TP313
PCH_JTAGX	D8		
PCH_TMS	A9		
PCH_TDO	E12		
PCH_TDI	B12		
PCH_TCK	A7	PCH_TCK 1	TP314
PCH_TRST#	H4		
PROC_PREQ#	C11	XDP_PREQ#	
PROC_PRDY#	D11	XDP_PRDY# 1	TP302
	G1	EAR_N_TEST_NCTF	
GPP_F7	DT15		
GPP_F9	DR15		
GPP_F10	DT14		

XDP

20191128(EVT)
Follow Nakia Shuri N7
No GPU

DB42: TOUCH_PANEL_DET#
DF8: TOUCH_PANEL_PD#

TGL-U-1-GP-U2
ZZ.00CPU.481

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Title	CPU (THML/JTAG)	
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Follow Hellcat15 Upsell TGL

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 EDP_HPD
24 L_BKLT_EN
55 eDP_VDD_EN
55 L_BKLT_CTRL

HDMI

57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 CPU_DPB_CTRL_CLK
57 CPU_DPB_CTRL_DATA
57 CPU_DISP_HPDB

TBT

71 USB1_TCSS_TX_N0
71 USB1_TCSS_TX_P0
71 USB1_TCSS_TX_N1
71 USB1_TCSS_TX_P1
71 USB1_TCSS_RX_N0
71 USB1_TCSS_RX_P0
71 USB1_TCSS_RX_N1
71 USB1_TCSS_RX_P1
71 TBT_LSX0_TXD
71 TBT_LSX0_RXD
71 USB1_TCSS_AUX_P
71 USB1_TCSS_AUX_N

Other

15 GPP_E21
15 GPP_D12
15 GPP_D10
65 KB_DET#
SOC_OC_FAULT
USB_OC1#

USB3.2 Type-A Port2 (IO)

DN4: WWAN_GPO_PERST#
DT6: WWAN_CARD_PWR_OFF#
DG47: 3.3V_CAM_EN
DF6: TBT_LSX1_TXD
DN23: SENSOR_DB_DET#
DD6: TBT_LSX1_RXD
DK23: CPU_DDP4_CTRL_CLK
DN21: CPU_DDP4_CTRL_DATA
DF47: CPU_DISP_HPD2
DH52: USB_OC1#
DK45: CPU_DISP_HPD4

CPU1A — 1 OF 21

eDP_TX_CPU_P3 AC2 DDIA_TXP3
eDP_TX_CPU_N3 AC1 DDIA_TXN3
eDP_TX_CPU_P2 AD2 DDIA_TXP2
eDP_TX_CPU_N2 AD1 DDIA_TXN2
eDP_TX_CPU_P1 AF1 DDIA_TXP1
eDP_TX_CPU_N1 AF2 DDIA_TXN1
eDP_TX_CPU_P0 AG2 DDIA_TXP0
eDP_TX_CPU_N0 AG1 DDIA_TXN0
eDP_AUX_CPU_P AJ2 DDIA_AUX_P
eDP_AUX_CPU_N AJ1 DDIA_AUX_N

TP401 — 1 GPP_E23 DN4 DT6 GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD GPP_E23/DDPA_CTRLDATA

EDP_HPD DR5 GPP_E14/DDSP_HPDA/DISP_MISCA

HDMI_DDI_TX_P3 T12 DDIB_TXP3
HDMI_DDI_TX_N3 T11 DDIB_TXN3
HDMI_DDI_TX_P0 Y11 DDIB_TXP2
HDMI_DDI_TX_N0 Y9 DDIB_TXN2
HDMI_DDI_TX_P1 T9 DDIB_TXP1
HDMI_DDI_TX_N1 P9 DDIB_TXN1
HDMI_DDI_TX_P2 V11 DDIB_TXP0
HDMI_DDI_TX_N2 V9 DDIB_TXN0
AB9 DDIB_AUX_P
AD9 DDIB_AUX_N

CPU_DPB_CTRL_CLK DM29 GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
CPU_DPB_CTRL_DATA DK27 GPP_H17/DDPB_CTRLDATA

CPU_DISP_HPDB DG43 GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

DG47 GPP_A21/DDPC_CTRLCLK/I2S5_TXD
KB_DET# DJ47 GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT_LSX0_TXD DU8 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
TBT_LSX0_RXD DV8 GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

GPP_E21 DF6 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
DD6 GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

DN23 GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10 DM23 GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK

DK23 GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12 DN21 GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI

CPU_DISP_HPD1 DF43 GPP_A17/DISP_MISCC/I2S4_TXD
DF45 GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
DF47 GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

USB_OC1# DH52 GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
SOC_OC_FAULT DK45 GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

eDP_VDD_EN DM8 EDP_VDDEN
L_BKLT_EN DN8 EDP_BKLTEN
L_BKLT_CTRL DG10 EDP_BKLTCTL

TGL-U-1-GP-U2

ZZ.00CPU.481

TCP0_TXRX_P1 AY2 USB1_TCSS_RX_P1
TCP0_TXRX_N1 AY1 USB1_TCSS_RX_N1
TCP0_TXRX_P0 BB1 USB1_TCSS_RX_P0
TCP0_TXRX_N0 BB2 USB1_TCSS_RX_N0
TCP0_TX_P1 AM5 USB1_TCSS_TX_P1
TCP0_TX_N1 AM7 USB1_TCSS_TX_N1
TCP0_TX_P0 AT7 USB1_TCSS_TX_P0
TCP0_TX_N0 AT5 USB1_TCSS_TX_N0
TCP0_AUX_P AP7 USB1_TCSS_AUX_P
TCP0_AUX_N AP5 USB1_TCSS_AUX_N

TBT

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX_N AF5

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE2
TCP2_TXRX_N0 BE1
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX_N BB7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7

TC_RCOMP_P AN2 TCSS_RCOMP_P
TC_RCOMP_N AN1 TCSS_RCOMP_N R402 1 2 150R2F-1-GP

DSI_DE_TE_2 M8

DDI_RCOMP AB1 DISP_RCOMP R401 1 2 150R2F-1-GP

DISP_UTILS/DSI_DE_TE_1 CE4

GP

R404 1 DY 2 CPU_DISP_HPD1
100KR2J-1-GP

20191209(EVT)
Add R403 PU 10k
3D3V_S0 R403 1 2 10KR2J-3-GP KB_DET#

<Core Design>

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Title	CPU (DDI/EDP/TBT)	
Size A3	Document Number Hellcat 13" TGL	Rev A00
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Follow Nakia Shuri N7

M_A_DQ[7:0]

M_A_DQ[15:8]

M_A_DQ[23:16]

M_A_DQ[31:24]

M_B_DQ[7:0]

M_B_DQ[15:8]

M_B_DQ[23:16]

M_B_DQ[31:24]

M_C_DQ[7:0]

M_C_DQ[15:8]

M_C_DQ[23:16]

M_C_DQ[31:24]

M_D_DQ[7:0]

M_D_DQ[15:8]

M_D_DQ[23:16]

M_D_DQ[31:24]

CPU1B

2 OF 21

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

DDR4/LP4/LP5/LP5 CMD Flip

TGL-U-1-GP-U2

ZZ.00CPU.481

CPU1C

3 OF 21

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

DDR4/LP4/LP5/LP5 CMD

TGL-U-1-GP-U2

ZZ.00CPU.481

<Core Design>

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Title: CPU (DDR)

Size: Custom | Document Number: Hellcat 13" TGL | Rev: A00

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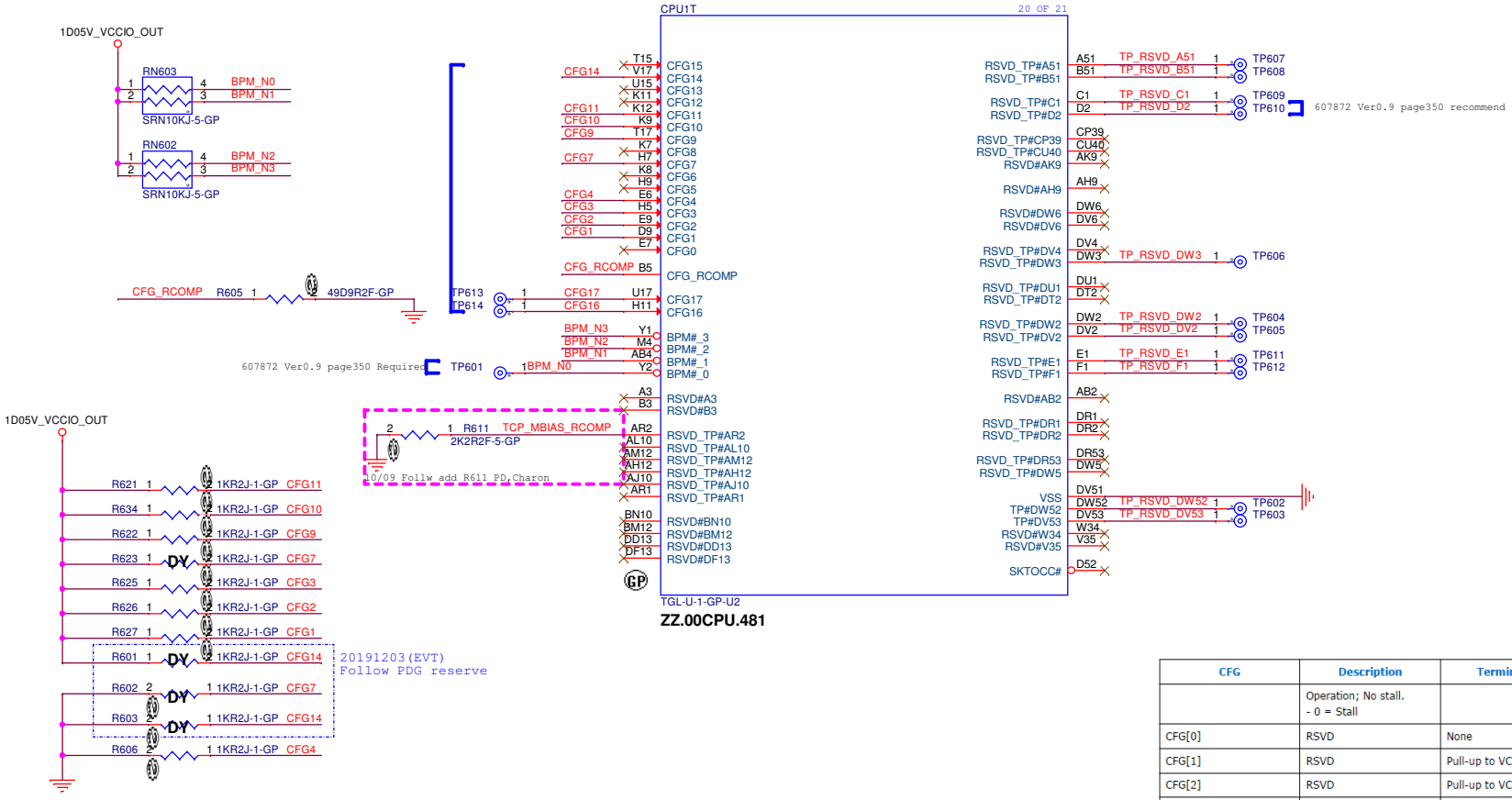

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION;
	0: LANE REVERSAL

DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED
	AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1: DISABLED
	NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
	10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
	01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

<Core Design>

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Title: CPU (CFG/IST)

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Follow Hellcat15 Upsell TGL

46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_ALERT#_CPU
46 SVID_CLK_CPU
46 SVID_DATA_CPU

CPU1M 13 OF 21

VCCIN

A24 A26 A29 A30 A33 A35 AY39 B24 B26 B29 B30 B33 B35 BA10 BA40 BB39 BB9 BC10 BC40 BD39 BD9 BE10 BE40 BF9 BG10 BG40 BH12 BH39 BH9 BJ10 BJ40 BK39 BL10 BL40 BM39 BN40 BP12 BP39 BR10 BR40 BT12 BT39 BU10 BU40 BV12 BY12 CA10 CB12 D24 D26 D29 D30 D33 D35 E24 E26 E27 E29 E30 E32 E33 G2 G24 G26 G30

VCCIN

G32 H24 H26 H30 H32 J1 J2 K1 K2 K24 K26 K30 K32 L24 L26 L30 L32 N24 N26 N30 N32 P24 P26 P28 P30 P32 T21 T23 T25 T27 T31 U23 U27 U29 U31 U33 V23 V25 V27 V29 V31 V33 W22 W24 W28 W32

VCCIN_SENSE R38 VCCCORE_SENSE
VSSIN_SENSE R37 VSSCORE_SENSE

VIDSOUT M12 SVID_DATA_CPU
VIDSCK M1 SVID_CLK_CPU
VIDALERT# P12 SVID_ALERT#_CPU_R

TGL-U-1-GP-U2

ZZ.00CPU.481

1D05V_VCCST

R703 1 100R2F-L1-GP-U SVID_DATA_CPU
R701 1 56R2J-4-GP SVID_ALERT#_CPU
R707 1 DV 56R2J-4-GP SVID_CLK_CPU

20200218(DVT1)
Change R701 to 56.2 ohm
Reverse R707

Layout note:
3.Length matchin 25mil, and close SOC in 2inch "

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

VCCIN

R704 1 100R2F-L1-GP-U VCCCORE_SENSE
R705 1 100R2F-L1-GP-U VSSCORE_SENSE

20191203(EVT)
Follow Nakiri shuri N7

R706 1 2 0R0402-PAD-2-GP SVID_ALERT#_CPU

<Core Design>

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Title	CPU (VCCIN/VID)	
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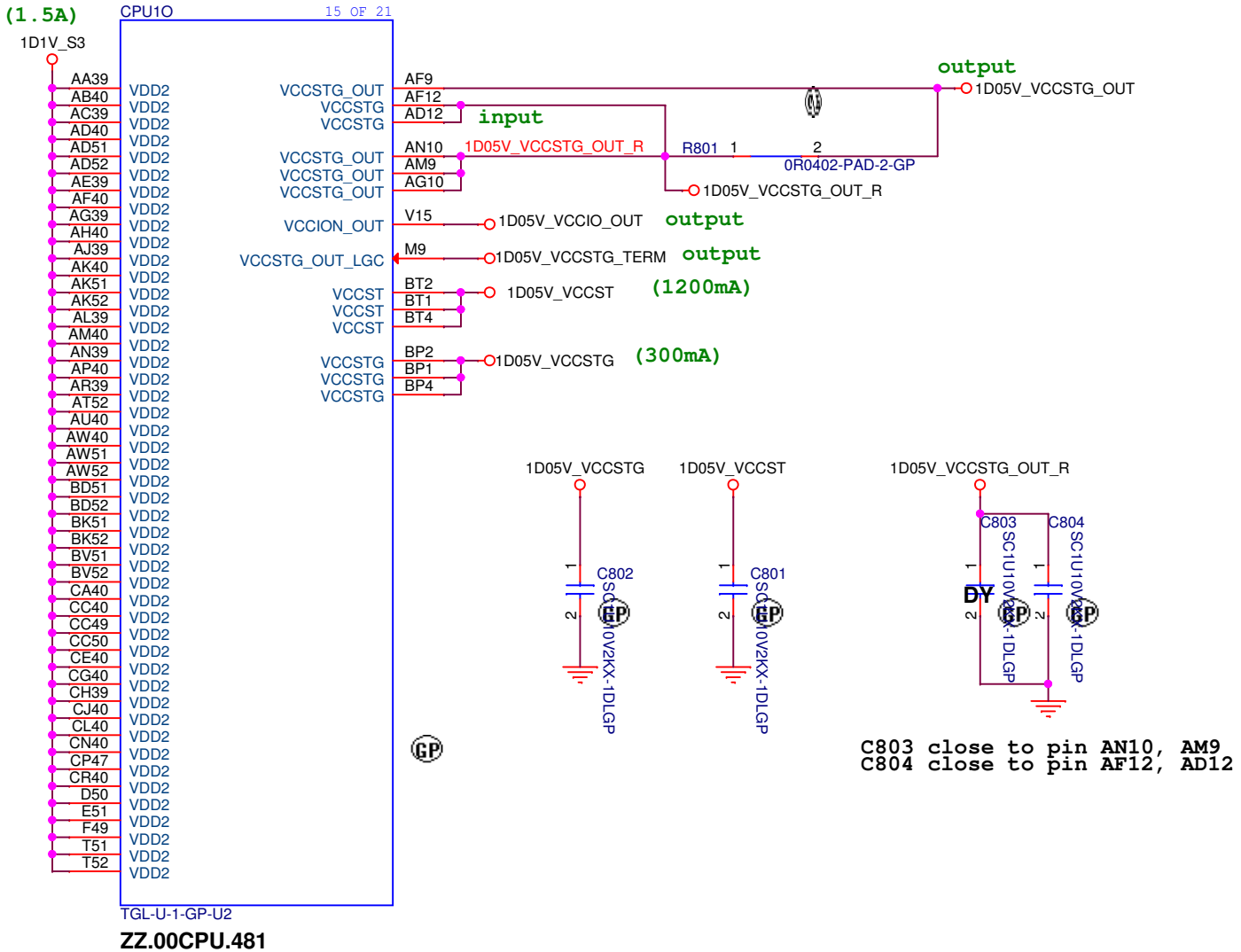

ZZ.00CPU.481

Lack of VCCPLL_OC / VCC1P8A / VCCPLL

<Core Design>

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Title	CPU (VDDQ/VCCST/VCCSTG)	
Size: A4	Document Number: Hellcat 13" TGL	Rev: A00
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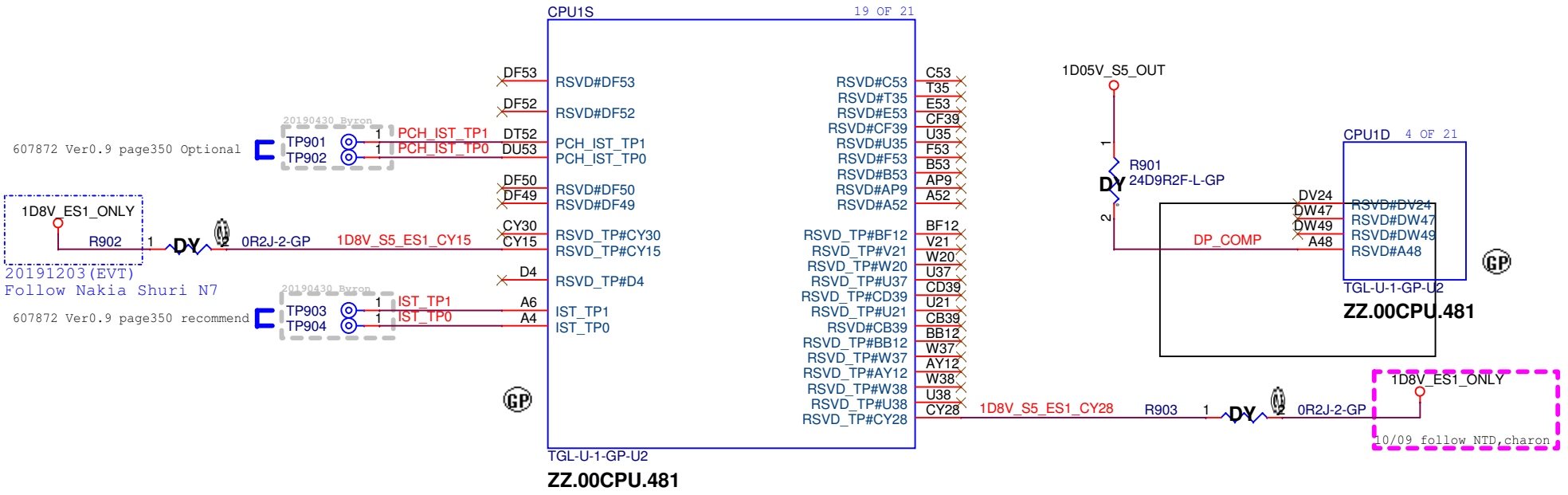
Follow Hellcat15 Upsell TGL



<Core Design>

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Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	***Hellcat 13" TGL***	***A00***

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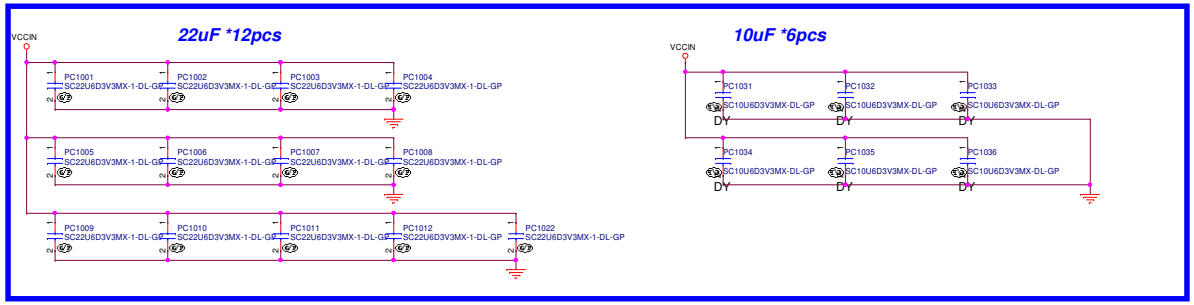
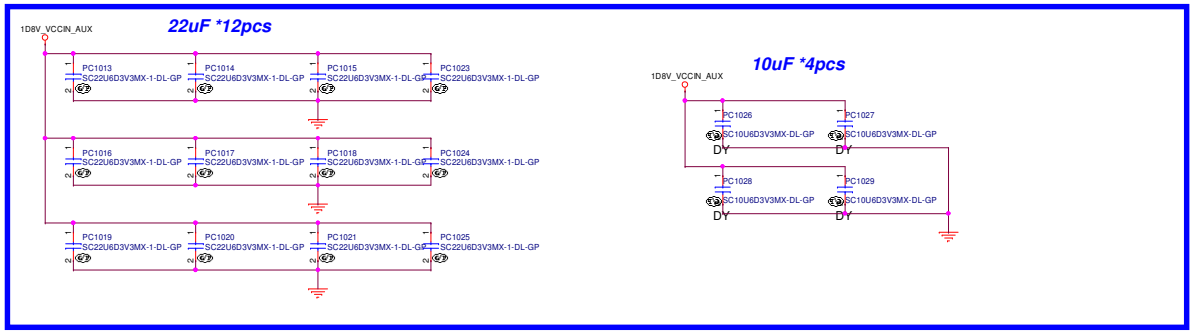
Main Func = CPU Follow Hellcat15 Upsell TGL





<Core Design>

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Title: CPU (CORE Power Cap1)

Size	Document Number	Rev
A2	Hellcat 13" TGL	A00

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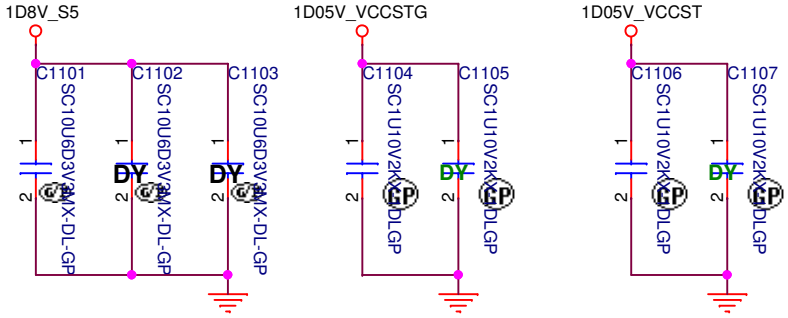
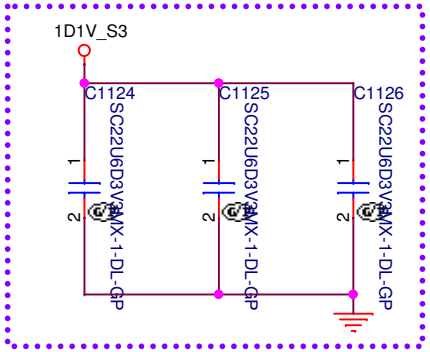
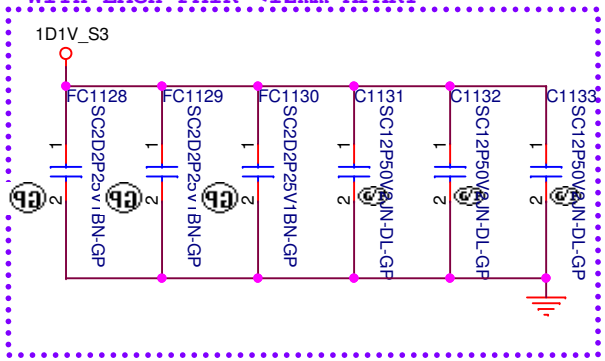


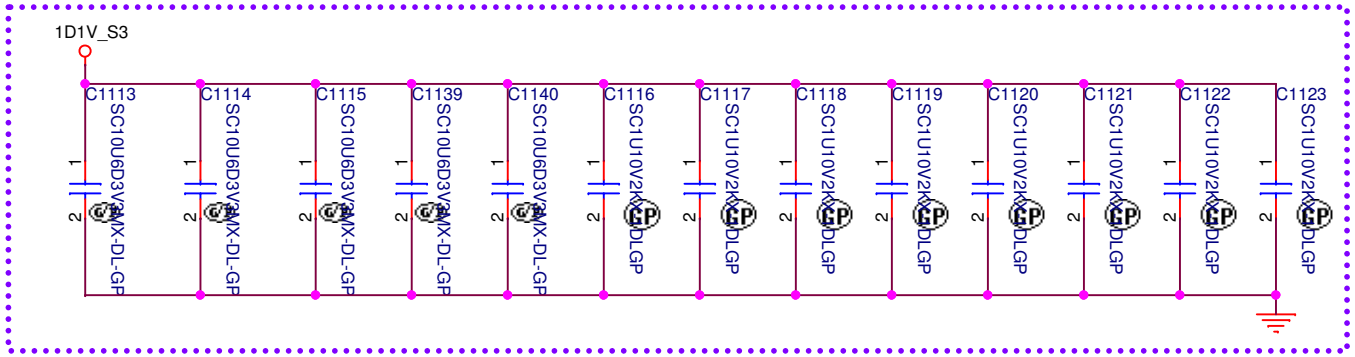
PLACE on CPU Same Side



EMC CAPS – PLACE <4mm FROM SOC VDDQ, WITH EACH PAIR <12mm APART



PLACE on BACK SIDE



<Core Design>

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Title	CPU (Power Cap2)	
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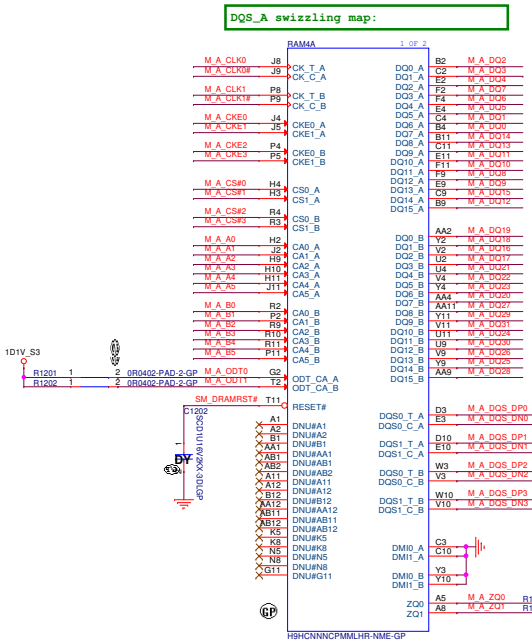
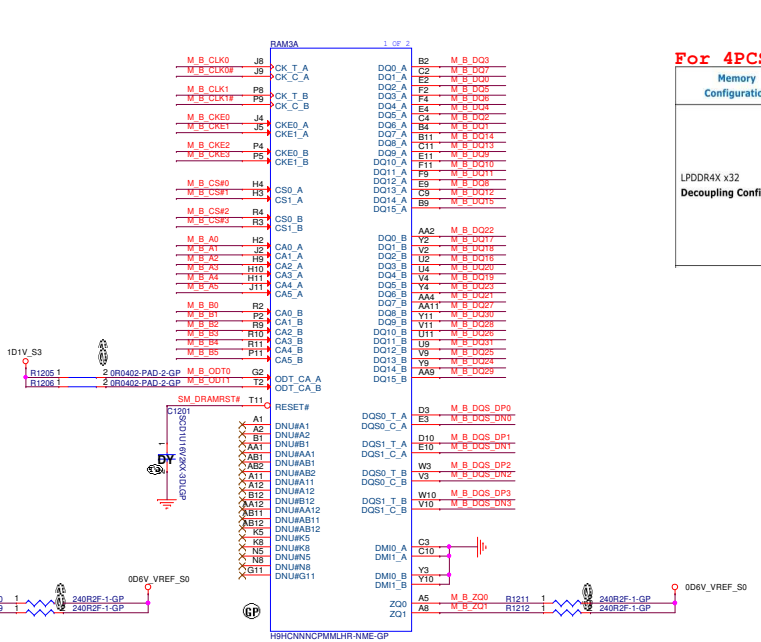
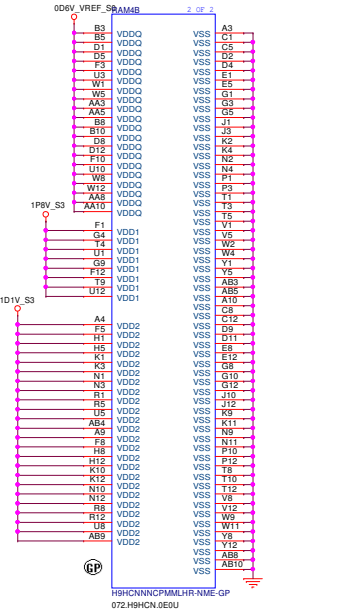
Follow Nakia Shuri N7

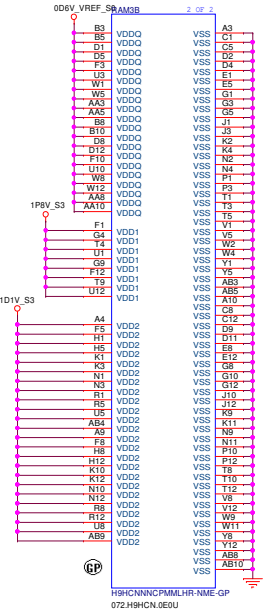
BOM change
15NY1$AA
K7HT2$AA

DQS_A swizzling map:





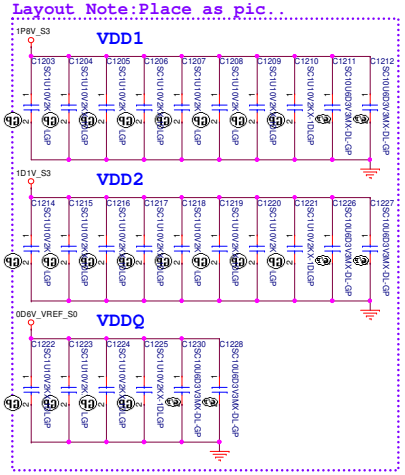




For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

Layout Note:Place as pic..



	LPDDR4		LPDDR4X		
VDDQ	1.1V	410mA	0.6V	185mA	PWR_VDDQ_VTT
VDD1	1.8V	6.8mA	1.8V	12mA	PWR_VDDQ_1D8V
VDD2	1.1V	290mA	1.1V	465mA	1D1V_S3

PWR_VDDQ
PWR_VDDQ_1D8V
PWR_VDDQ

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

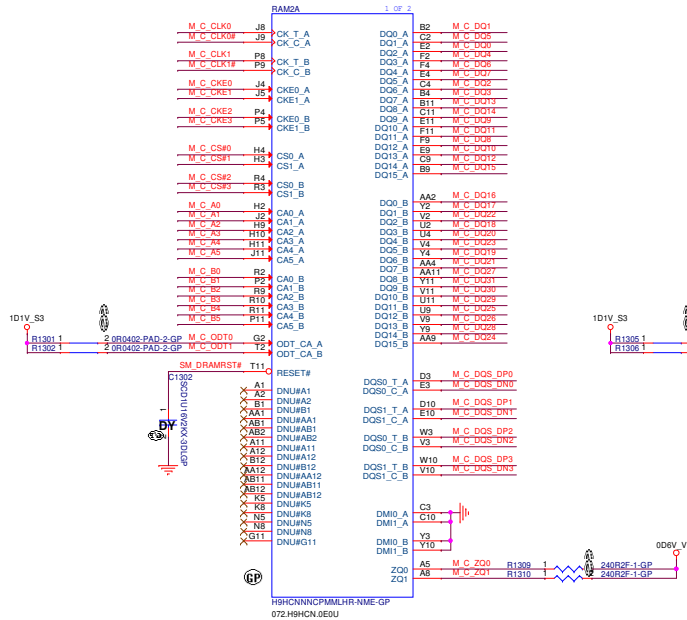
Title: DDR (LPDDR4X-CHA)

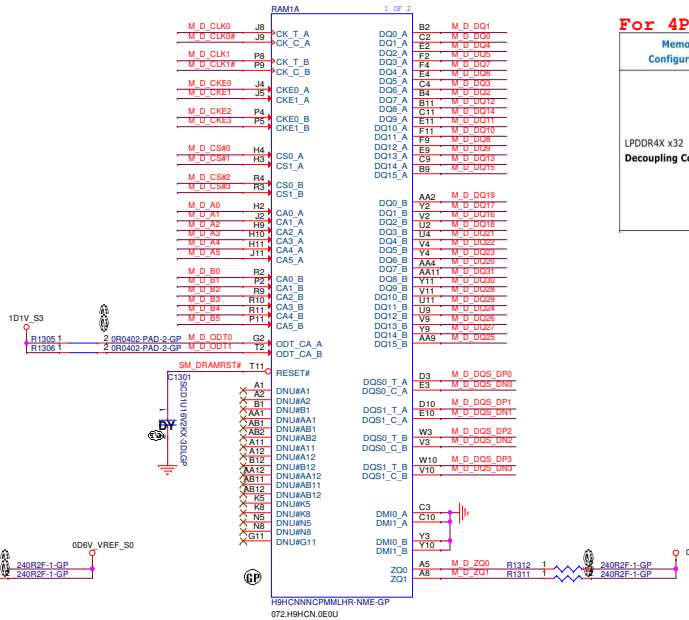
Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

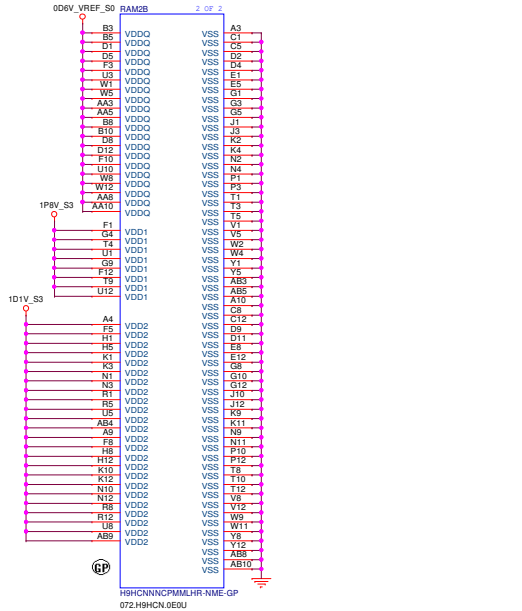
Date: Wednesday, August 05, 2020 | Sheet 12 of 105

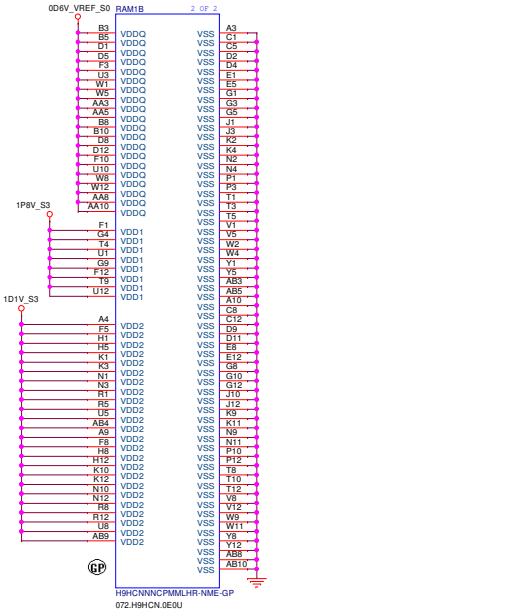
Follow Nakia Shuri N7

DQS_B swizzling map:





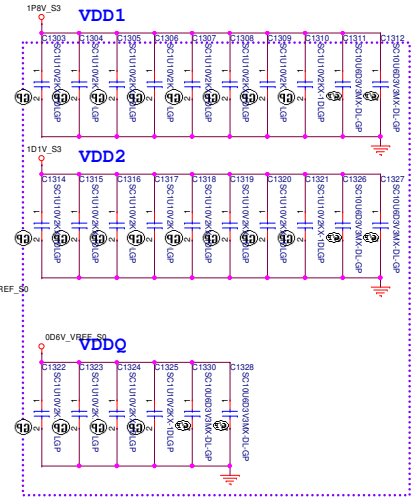




For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

Layout Note:Place as pic..



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (LPDDR4X-CHB)

Size	Document Number	Rev
A2	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 13 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR (RSVD) (DDR4-CHA1)

Size	Document Number	Rev
A4	*Hellcat 13" TGL*	*A00*

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18,24,25	SPI_SI_ROM	
18,24,25	SPI_WP_ROM	
18,24,25	SPI_HOLD_ROM	
21,61	CNV_RGI_DT	
18	SML0_ALERT#	
18	GPP_E6	
19	HDA_SDO	
4,71	TBT_LSX0_RXD	
4	GPP_D10	
3	DBG_PMODE	
4	GPP_D12	
4	GPP_E21	
18	GPP_E10	
18	GPP_E11	

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic	3D3V_S5 =20K PD= R1501 4K7R2J-2-GP DY SML0_ALERT# R1502 20K5R2F-GP	3D3V_SPI =NO INTERNAL= R1503 4K7R2J-2-GP 20200219(DVT1) Change to 4.7k SPI_SI_ROM BOOT_HALT Close to U2501 R1511 4K7R2J-2-GP DY	3D3V_S5 =NO INTERNAL= R1504 100KR2J-1-GP 20191204(EVT) Change to 3D3V_S5 Follow Nakia GPP_E6 R1512 4K7R2J-2-GP DY	=20K PD=	3D3V_SPI =NO INTERNAL= R1506 100KR2J-1-GP SPI_WP_ROM Close to U2501 R1514 4K7R2J-2-GP DY CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	=20K PD= * PH as VCCPGPPR 1D8V_GPPR_S5 R1509 4K7R2J-2-GP DY ME_UNLOCK R1515 0R2J-2-GP HDA_SDO	1D8V_S5 =NO INTERNAL= R1507 100KR2J-1-GP CNV_RGI_DT R1516 4K7R2J-2-GP DY
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic	E19 3D3V_S5 =NO INTERNAL= R1518 4K7R2J-2-GP DY TBT_LSX0_RXD R1521 20KR2J-L2-GP sky 0329	E21 3D3V_S5 =NO INTERNAL= R1519 4K7R2J-2-GP DY GPP_E21 R1522 20KR2J-L2-GP sky 0329	D10 3D3V_S5 =NO INTERNAL= R1520 4K7R2J-2-GP DY GPP_D10 R1523 20KR2J-L2-GP sky 0329	D12 3D3V_S5 =NO INTERNAL= R1524 4K7R2J-2-GP DY GPP_D12 R1525 20KR2J-L2-GP sky 0329	3D3V_S5 =NO INTERNAL= R1526 100KR2J-1-GP SPI_HOLD_ROM Close to U2501 DY R1527 100KR2J-1-GP	1D05V_S5_OUT =20K PU= R1528 1KR2F-3-GP 20191204(EVT) Always stuff Follow Nakia DBG_PMODE R1529 1KR2F-3-GP DY	1D8V_S5 R1531 20KR2J-L2-GP GPP_E10	1D8V_S5 R1530 20KR2J-L2-GP GPP_E11
High	3.3V	3.3V	3.3V	3.3V	Disable	DEXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DEXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	RA RB	RA RB		

Follow Hellcat15 Upsell TGL

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
A2	Hellcat 13" TGL	A00

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GPU

M.2 SSD

63 SSD_PCIE_TX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_RX_N3
63 SSD_PCIE_TX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_RX_N2
63 SSD_PCIE_TX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_RX_N1
63 SSD_SATA_TX_P
63 SSD_SATA_TX_N
63 SSD_SATA_RX_P
63 SSD_SATA_RX_N
63 M2_PEDET1
63 M2_DEVSLP1

USB1
USB3.2 Type-A Port1 (MB)

USB2
USB3.2 Type-A Port2 (IO)

66 USB2_USB31_TX_P
66 USB2_USB31_TX_N
66 USB2_USB31_RX_P
66 USB2_USB31_RX_N
66 USB2_USB20_P
66 USB2_USB20_N
66 USB_OC0#
4 USB_OC1#

Card Reader

66 CARD1_USB20_P
66 CARD1_USB20_N

Camera

55 CCD_USB20_P
55 CCD_USB20_N

Finger Print

92 FP1_USB20_N
92 FP1_USB20_P

TBT

72 USB4_USB20_P
72 USB4_USB20_N
71,72 TBT_FORCE_PWR

BT

WLAN

61 WLAN_RF_DIS#

PD

7,31 PCH_TBT_PERST#

MM

A 24 DUAL_BOOT_EVENT#

M.2 SSD

SSD_SATA_TX_P BT7 PCIE12_TXP/SATA1_TXP
SSD_SATA_TX_N BT8 PCIE12_TXN/SATA1_TXN
SSD_SATA_RX_P CE2 PCIE12_RXP/SATA1_RXP
SSD_SATA_RX_N CE1 PCIE12_RXN/SATA1_RXN
SSD_PCIE_TX_P1 BT9 PCIE11_TXP/SATA0_TXP
SSD_PCIE_TX_N1 BV9 PCIE11_TXN/SATA0_TXN
SSD_PCIE_RX_P1 CF4 PCIE11_RXP/SATA0_RXP
SSD_PCIE_RX_N1 CF3 PCIE11_RXN/SATA0_RXN
SSD_PCIE_TX_P2 BV7 PCIE10_TXP
SSD_PCIE_TX_N2 BV8 PCIE10_TXN
SSD_PCIE_RX_P2 CG2 PCIE10_RXP
SSD_PCIE_RX_N2 CG1 PCIE10_RXN
SSD_PCIE_TX_P3 BY7 PCIE9_TXP
SSD_PCIE_TX_N3 BY8 PCIE9_TXN
SSD_PCIE_RX_P3 CG5 PCIE9_RXP
SSD_PCIE_RX_N3 CG4 PCIE9_RXN

CB8 CB7 PCIE8_TXP/PCIE8_TXN
CK5 CK4 PCIE8_RXP/PCIE8_RXN
CD9 CD8 PCIE7_TXP/PCIE7_TXN
CK1 CK2 PCIE7_RXP/PCIE7_RXN
CG8 CG7 PCIE6_TXP/PCIE6_TXN
CL4 CL5 PCIE6_RXP/PCIE6_RXN
CJ6 CJ7 PCIE5_TXP/PCIE5_TXN
CN2 CN1 PCIE5_RXP/PCIE5_RXN
CR8 CR7 PCIE4_TXP/USB31_4_TXP / PCIE4_TXN/USB31_4_TXN
CN5 CN4 PCIE4_RXP/USB31_4_RXP / PCIE4_RXN/USB31_4_RXN
CU8 CU7 PCIE3_TXP/USB31_3_TXP / PCIE3_TXN/USB31_3_TXN
CT2 CT1 PCIE3_RXP/USB31_3_RXP / PCIE3_RXN/USB31_3_RXN

USB2_IO

USB2_USB31_TX_P CW8 PCIE2_TXP/USB31_2_TXP
USB2_USB31_TX_N CW7 PCIE2_TXN/USB31_2_TXN
USB2_USB31_RX_P CU3 PCIE2_RXP/USB31_2_RXP
USB2_USB31_RX_N CT4 PCIE2_RXN/USB31_2_RXN

DA8 DA7 PCIE1_TXP/USB31_1_TXP / PCIE1_TXN/USB31_1_TXN
CV2 CV1 PCIE1_RXP/USB31_1_RXP / PCIE1_RXN/USB31_1_RXN

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TGL-U-1-GP-U2
ZZ.00CPU.481

USB2P_10 / USB2N_10 CV4 CV3 — 20191204(EVT) CNVi only, remove USB2.0 BT
USB2P_9 / USB2N_9 DD5 DD4
USB2P_8 / USB2N_8 CW9 DA9
USB2P_7 / USB2N_7 DD1 CARD1_USB20_P, DD2 CARD1_USB20_N → Card Reader
USB2P_6 / USB2N_6 DA1 CCD_USB20_P, DA2 CCD_USB20_N → Camera
USB2P_5 / USB2N_5 DA12 FP1_USB20_P, DA11 FP1_USB20_N → Finger Print
USB2P_4 / USB2N_4 DC8 DC7
USB2P_3 / USB2N_3 DB4 USB4_USB20_P, DB3 USB4_USB20_N → TBT
USB2P_2 / USB2N_2 DA5 USB2_USB20_P, DA4 USB2_USB20_N → USB2_IO
USB2P_1 / USB2N_1 DC11 DEBUG_USB20_P, DC9 DEBUG_USB20_N — TP1601, TP1602 — 20191218(EVT) Add for Intel debug used

20191217(EVT) Follow Intel check list
3D3V_S5_VCCPRIM
USB_OC0# R1605 10KR2J-3-GP
USB_OC1# R1606 10KR2J-3-GP
USB_OC3# R1607 10KR2J-3-GP

GPP_E0/SATAXPCIE0/SATAGP0 / GPP_A12/SATAXPCIE1/SATAGP1/I2S3_SFRM DP4 DF41 M2_PEDET1
GPP_E9/USB_OC0# / GPP_A16/USB_OC3#/I2S4_SFRM DD8 USB_OC0#, DJ45 USB_OC3#
GPP_E5/DEVSLP1 / GPP_E4/DEVSLP0 DN6 M2_DEVSLP1, DG8
GPP_H15/M2_SKT2_CFG3 DN29 DUAL_BOOT_EVENT#
GPP_H14/M2_SKT2_CFG2 DK25 WLAN_RF_DIS#
GPP_H13/M2_SKT2_CFG1 DT31 PCH_TBT_PERST#
GPP_H12/M2_SKT2_CFG0 DR32 TBT_FORCE_PWR
20191224(EVT) Dell request reserve
R1609 100R2F-L1-GP-U PCH_TBT_PERST#

PCIE_RCOMP_P DV9 PCIE_RCOMP_P, R1601 100R2F-L1-GP-U
PCIE_RCOMP_N DT9 PCIE_RCOMP_N
USB_VBUSSENSE DC12 USB_VBUSSENSE, R1602 10KR2F-2-GP
USB_ID DF1 USB_ID, R1604 10KR2F-2-GP
USB2_COMP DE1 USB2_COMP, R1603 113R2F-GP
RSVD_BSCAN E3

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TGL-U-1-GP-U2
ZZ.00CPU.481

PCIE4_TX_P3 P5, PCIE4_TX_N3 P7, PCIE4_RX_P3 N1, PCIE4_RX_N3 N2
PCIE4_TX_P2 T5, PCIE4_TX_N2 T7, PCIE4_RX_P2 R1, PCIE4_RX_N2 R2
PCIE4_TX_P1 V5, PCIE4_TX_N1 V7, PCIE4_RX_P1 T1, PCIE4_RX_N1 T2
PCIE4_TX_P0 Y5, PCIE4_TX_N0 Y7, PCIE4_RX_P0 V1, PCIE4_RX_N0 V2
PCIE4_RCOMP_P Y12, PCIE4_RCOMP_N V12
PCIE4_RCOMP_P — R1608 2K2R2F-GP — PCIE4_RCOMP_N
20200122(DVT1) Add R1608

PCIE4_RCOMP resistor should be stuffed Even if PCIE4 not used.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
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Date: Wednesday, August 05, 2020 Sheet 16 of 105

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Power on sequence for G3 sharing

61,63,71 PCH_PLTRST#
40,53,55 SIO_SLP_S3#
40,92 SIO_SLP_S4#
24,25,45 3V_5V_PWRGD
24 SIO_PWRBTN#
24,64 PCH_RSMRST#
24,26 IMVP_VR_ON
24 SYS_PWROK
40,61 SIO_SLP_SUS#
40 VCCST_OVERRIDE
40 CPU_C10_GATE#
72 TBT_PD_ALERT#
43,44 AC_IN#
24,40,44,46 ALL_SYS_PWRGD
44,46 PWR_IMVP_PWRGD
24 PCH_DPWROK
24 EC_PCH_SPI_EN
16,71 PCH_TBT_PERST#
40,50 VCCIN_AUX_PWRGD

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TGL-U-1-GP-U2
ZZ.00CPU.481

Check with EC
PCH_DPWROK
R1723 NON_G3 0R2J-2-GP
20200213(DVT1) R1723 NON_G3
D1704 RB520S30-GP DY
ALL_SYS_PWRGD
PWR_IMVP_PWRGD R1745 1 0R0402-PAD-2-GP
IMVP_VR_ON R1747 1 2 0R0402-PAD-2-GP
20191204(EVT) DY D1704 Follow Nakia N7

SIO_SLP_SUS# DV49 SLP_SUS#
SIO_SLP_S5# DM43 GPD10/SLP_S5#
SIO_SLP_S4# DJ41 GPD5/SLP_S4#
SIO_SLP_S3# DJ43 GPD4/SLP_S3#
SIO_SLP_A# DF41 GPD6/SLP_A#
DT44 GPD9/SPL_WLAN#
SIO_SLP_S0# DD42 GPP_B12/SLP_S0#
DD39 SLP_LAN#
PM_RSMRST# DM35 RSMRST#
SYS_RESET# DD10 SYS_RESET#
PCH_PLTRST# DD41 GPP_B13/PLTRST#
DSW_PWROK_R DK35 DSW_PWROK
SYS_PWROK DF10 SYS_PWROK
PCH_PWROK DN35 PCH_PWROK
RTC_INTRUDER# DM37 INTRUDER#
SPI_VCC_SEL DT49 SPIVCCIOSEL

PROCPWRGD BM9 TP_VCORE_PWRGD 1 TP1702 follow 612304 Ver0.9
GPD3/PWRBTN# DK41 SIO_PWRBTN#
GPD0/BATLOW# DN41 PCH_BATLOW#
GPD1/ACPRESENT DK43 AC_PRESENT
GPP_B11/PMCALERT# CW40 TBT_PD_ALERT# 1 TP1703
GPP_H18/CPU_C10_GATE# DN27 CPU_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF# DG31 TPM_PRSNT#
WAKE# DK39 PCIE_WAKE_N
GPD2/LAN_WAKE# DM41
GPD11/LANPHYPC/DSWLDO_MON DT41
GPD7 DN43 PCH_TBT_PERST#_GPD7 R1748 1 DY 0R2J-2-GP PCH_TBT_PERST#
20200220(DVT1) Reserve 0 ohm to GPD7
VCCSTPWRGOOD_TCSS CE5 VCCSTPWRGOOD_TCSS R1731 1 0R0402-PAD-2-GP VCCST_OVERRIDE
VCCST_PWRGD BP8 VCCST_PWRGD_R
VCCST_OVERRIDE BP9 VCCST_OVERRIDE_R R1728 1 2 0R0402-PAD-2-GP VCCST_OVERRIDE
GPP_F20/EXT_PWR_GATE# DR12 EXT_PWR_GATE#
GPP_F21/EXT_PWR_GATE2# DW12 EXT_PWR_GATE2#

D1701 RB520S30-GP A K AC_IN# 83.R2003.A8M AC_PRESENT
Q1702 2N7002KDW-1-GP 75.27002.F7C
3D3V_AUX_S5 R1737 1 100KR2J-1-GP PM_RSMRST#_M PM_RSMRST#
2nd = 075.27002.0E7C

SPI SELECT STRAP
Cap LOW → 3.3V
Cap DY → 1.8V
SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V

RTC_AUX_S5 R1704 MR2F-GP RTC_INTRUDER# C1701 SCD1U16V2KX-3DLGP R1714 MR2F-GP DY
3D3V_S5_VCCPRIM R1705 4K7R2J-2-GP DY SPI_VCC_SEL R1706 4K7R2J-2-GP
20200102(EVT) Follow Intel CRB & checklist

3D3V_S5_VCCPRIM
20200218(DVT1) Change PU to 3.3V_PRIM
R1701 1 2 10KR2J-3-GP SYS_RESET#
R1713 1 2 100KR2J-1-GP AC_PRESENT
20200416(DVT2) Change R1713 to 100k Follow Intel checklist
R1715 1 2 10KR2J-3-GP PCH_BATLOW#
R1740 1 2 100KR2J-1-GP EXT_PWR_GATE#
R1741 1 DY 2 100KR2J-1-GP EXT_PWR_GATE2#
3D3V_S5 R1746 1 1KR2J-1-GP PCIE_WAKE_N
3D3V_S5 20200512(DVT2) Change to 3D3V_S5 Follow CY20 table
R1712 1 TPM 2 100KR2J-1-GP TPM_PRSNT#

VCCST_OVERRIDE R1730 1 2 100KR2J-1-GP
PCH_PWROK R1732 1 2 100KR2J-1-GP
SYS_PWROK R1733 1 2 100KR2J-1-GP
PCH_PLTRST# R1744 1 2 100KR2J-1-GP
DSW_PWROK_R R1726 1 2 100KR2J-1-GP
201912119(EVT) Follow Intel design

VCCIN_AUX_PWRGD R1725 1 DY 68KR2F-GP PM_RSMRST#
20200224(DVT1) Reserve R1725, C1704 Follow Nakia
C1704 SCD1U16V2KX-3DLGP DY
3V_5V_PWRGD R1750 1 DY 68KR2F-GP DSW_PWROK_R
C1750 SCD1U10V2KX-4DLGP DY
1.11 Follow Nakia

Volatge Level 1V
3D3V_S5 C1702 SCD1U16V2KX-3DLGP
1D05V_VCCST R1702 1KR2F-3-GP
U1701 NC#1 VCC A GND Y 74LVC1G07GW-GP
ALL_SYS_PWRGD VCCST_PWRGD_RR R1703 1 2 60D4R2F-GP VCCST_PWRGD_R
73.01G07.0HG
2nd = 73.17S07.0AG

3D3V_AUX_S5 R1707 1 2 100KR2J-1-GP R1708 10KR2J-3-GP
Q1701 2N7002KDW-1-GP 75.27002.F7C
3V_5V_POK# 3V_5V_POK_C R1710 1 2 0R0402-PAD-2-GP 3V_5V_PWRGD
PM_RSMRST# R1709 1 DY 1KR2J-1-GP PCH_RSMRST#
R1711 100KR2J-1-GP
2nd = 075.27002.0E7C

20191217(EVT) Follow Mocking bird ICL modify
3D3V_S5 C1714 SCD1U16V2KX-3DLGP
PCH_RSMRST# R1773 1 2 0R0402-PAD-2-GP PCH_RSMRST#_U
PCH_DPWROK R1775 1 2 0R0402-PAD-2-GP PCH_DPWROK_R
3D3V_S5_R R1771 1 2 0R0402-PAD-2-GP 3D3V_S5_U
U1703 VDD PCH_RSMRST# PCH_DPWPOK DSW_PWROK 3V_5V_PWRGD NC#7 EC_PCH_SPI_EN GND SLG4E43789VTR-1-GP
3V_5V_PWRGD_U R1772 1 2 0R0402-PAD-2-GP 3V_5V_PWRGD
EC_PCH_SPI_EN_R R1774 1 2 0R0402-PAD-2-GP EC_PCH_SPI_EN
074.43789.M001
2nd = 074.03904.0053

20191213(EVT) Follow Mocking bird ICL modify
3D3V_S5_VCCPRIM 20200706(PVT) Fine tune to 330K Watch Dog sequence
3D3V_S5 R1738 1 330KR2F-L-GP 3D3V_S5_PCH_R
R1721 1 100KR2J-1-GP 3D3V_S5_R
C1713 SCD1U16V2KX-3DLGP
U1710 B A VCC Y GND 74LVC1G08GW-1-GP
73.01G08.L04
2nd = 073.7SZ08.000G
3rd = 73.01G08.IHG
R1776 1 DY 2 0R2J-2-GP
DSW_PWROK_R C1712 SCD1U16V2KX-3DLGP
R1734 1 2 0R0402-PAD-2-GP
Q1703 2N7002KDW-1-GP 75.27002.F7C
Q1703_2_3 R1735 DY 1 100KR2J-1-GP
R1736 10KR2F-2-GP DY
DSW_PWROK
R1739 1MR2F-GP DY
201912120(EVT) DY because R1726 stuff
PCH_RSMRST# DSW_PWROK U1702 B A VCC Y GND 74LVC1G08GW-1-GP PM_RSMRST#
73.01G08.L04
2nd = 073.7SZ08.000G
3rd = 73.01G08.IHG

DSW_PWROK_R A D1703 K PCH_DPWROK DY RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
3D3V_S5_R A D1702 K PCH_DPWROK DY RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (PMU)
Size: Custom | Document Number: Hellcat 13" TGL | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 17 of 105

Follow Hellcat15 Upsell TGL

SPI ROM
- SPI_CLK_ROM
- SPI_HOLD_ROM
- SPI_WP_ROM
- SPI_SO_ROM
- SPI_SI_ROM
- SPI_CS_ROM_N0
- SPI_CS_ROM_N1

EC
- ESPI_IO0
- ESPI_IO1
- ESPI_IO2
- ESPI_IO3
- ESPI_CS#
- ESPI_RESET#
- ESPI_CLK

Audio
- SPK_ID

M.2 SSD
- SSD_CLK_CPU_N
- SSD_CLK_CPU_P
- CLK_PCIE_NVME_REQ#
- SATA_LED#

GPU

SMBUS
- SML1_SMBCLK
- SML1_SMBDATA
- SML0_SMBCLK
- SML0_SMBDATA
- SML1_SMBCLK_THM
- SML1_SMBDATA_THM

OTHER
- SUSCLK

HW STRAP
- SML0_ALERT#
- GPP_E6
- GPP_E10
- GPP_E11

MEMORY
- MEM_CHA_EN
- MEM_SPEED_SEL

SD
- HOST_SD_WP#

3D3V_S0 — R1821 10KR2J-3-GP — SPK_ID

20200512(DVT2) Change to 0 ohm Follow Intel T PDG 1.1

SPI_CLK_ROM R1826 0R0402-PAD-2-GP SPI0_CLK_R_CPU DJ37
SPI_HOLD_ROM R1827 0R0402-PAD-2-GP SPI0_HOLD_R_CPU DG35
SPI_WP_ROM R1828 0R0402-PAD-2-GP SPI0_WP_R_CPU DJ39
SPI_SO_ROM R1829 0R0402-PAD-2-GP SPI0_SO_R_CPU DJ33
SPI_SI_ROM R1830 0R0402-PAD-2-GP SPI0_SI_R_CPU DJ35
SPI_CS_ROM_N1 R1831 0R0402-PAD-2-GP SPI_CS_CPU_N1 DF35
SPI_CS_ROM_N0 R1832 0R0402-PAD-2-GP SPI_CS_CPU_N0 DG37

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SPI0_CLK
SPI0_IO3
SPI0_IO2
SPI0_MISO
SPI0_MOSI
SPI0_CS1#
SPI0_CS0#
SPI0_CS2#

GPP_E11 — DJ6
GPP_E11/SPI1_CLK/THC0_SPI1_CLK
GPP_E2/SPI1_IO3/THC0_SPI1_IO3
GPP_E1/SPI1_IO2/THC0_SPI1_IO2
GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
GPP_E10/SPI1_CS#/THC0_SPI1_CS#
GPP_E8/SPI1_CS1#/SATA_LED#
GPP_E17/THC0_SPI1_INT#
GPP_E6/THC0_SPI1_RST#

GPP_E10 — DV11 — SATA_LED#
TP1802 — DGPU_HOLD_RST# — DW9
GPP_E6 — DT8

SPK_ID — DN15
GPP_F11/THC1_SPI2_CLK
GPP_F15/GSXSRESET#/THC1_SPI2_IO3
GPP_F14/GSXDIN/THC1_SPI2_IO2
HOST_SD_WP# — DM13
GPP_F13/GSXSLOAD/THC1_SPI2_IO1
GPP_F12/GSXDOUT/THC1_SPI2_IO0
MEM_CHA_EN — DK15
GPP_F16/GSXCLK/THC1_SPI2_CS#
GPP_F18/THC1_SPI2_INT#
GPP_F17/THC1_SPI2_RST#

DH3 CL_CLK
DH4 CL_DATA
DF2 CL_RST#

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GPP_C0/SMBCLK — DK21 — CPU_SMB_SCL
GPP_C1/SMBDATA — DM19 — CPU_SMB_SDA
GPP_C2/SMBALERT# — DN19 — CPU_SMB_ALERT#
XDP
20200218(DVT1) Reverse 0 ohm
GPP_C3/SML0CLK — DK19 — SML0_SMBCLK_R — R1812 0R0402-PAD-2-GP — SML0_SMBCLK
GPP_C4/SML0DATA — DM17 — SML0_SMBDATA_R — R1813 0R0402-PAD-2-GP — SML0_SMBDATA
GPP_C5/SML0ALERT# — DN17 — SML0_ALERT#
BB non-TBT

GPP_C6/SML1CLK — DK17 — SML1_SMBCLK
GPP_C7/SML1DATA — DJ17 — SML1_SMBDATA
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# — CY50 — SML1_ALERT#
Thermal.EC

GPP_A5/ESPI_CLK — DN53 — PCH_ESPI_CLK — R1804 49D9R2F-GP — ESPI_CLK
GPP_A3/ESPI_IO3/SUSACK# — DJ53 — PCH_ESPI_IO3 — R1808 15R2F-2-GP — ESPI_IO3
GPP_A2/ESPI_IO2/SUSWARN# SUSPWRDNACK — DH50 — PCH_ESPI_IO2 — R1807 15R2F-2-GP — ESPI_IO2
GPP_A1/ESPI_IO1 — DP50 — PCH_ESPI_IO1 — R1806 15R2F-2-GP — ESPI_IO1
GPP_A0/ESPI_IO0 — DP52 — PCH_ESPI_IO0 — R1805 15R2F-2-GP — ESPI_IO0
GPP_A4/ESPI_CS# — DK52 — PCH_ESPI_CS# — R1809 0R0402-PAD-2-GP — ESPI_CS#
GPP_A6/ESPI_RESET# — DL50 — PCH_ESPI_RST# — R1810 0R0402-PAD-2-GP — ESPI_RESET#
R1814 75KR2F-GP
20191209(EVT) Follow Intel CRB use 1%
20191210(EVT) Follow EC net name
to EC,debug14pin

3D3V_S5 — RN1803 SRN1KJ-7-GP — CPU_SMB_SDA, CPU_SMB_SCL — 11,08 3D3V_S0->3D3V_S5
20191216(EVT) Layout swap request
RN1807 SRN1KJ-7-GP — SML0_SMBDATA, SML0_SMBCLK
RN1801 SRN1KJ-7-GP — SML1_SMBCLK, SML1_SMBDATA
1D8V_S5 — R1823 10KR2J-3-GP — CPU_SMB_ALERT#
R1824 10KR2J-3-GP
R1825 10KR2J-3-GP — SML1_ALERT#

20200318(DVT1) Follow Nakia
RN1808 SRN0J-6-GP — SML0_SMBCLK, SML0_SMBDATA — SML1_SMBCLK_THM, SML1_SMBDATA_THM
RN1809 SRN0J-6-GP — SML1_SMBCLK, SML1_SMBDATA

CPU1K — 11 OF 21

BW1 CLKOUT_PCIE_P6
BW2 CLKOUT_PCIE_N6
CB2 CLKOUT_PCIE_P5
CB1 CLKOUT_PCIE_N5
BW4 CLKOUT_PCIE_P4
BW5 CLKOUT_PCIE_N4
CL7 CLKOUT_PCIE_P3
CL8 CLKOUT_PCIE_N3
CB4 CLKOUT_PCIE_P2
CB5 CLKOUT_PCIE_N2
BY4 CLKOUT_PCIE_P1
BY3 CLKOUT_PCIE_N1
CN7 CLKOUT_PCIE_P0
CN8 CLKOUT_PCIE_N0
DJ5 XCLK_BIASREF

GPP_F19/SRCCLKREQ6# — DU14 — MEM_SPEED_SEL
GPP_H11/SRCCLKREQ5# — DF23 — CLK_PCIE_NVME_REQ#
GPP_H10/SRCCLKREQ4# — DG25
GPP_D8/SRCCLKREQ3# — DT24
GPP_D7/SRCCLKREQ2# — DT30
GPP_D6/SRCCLKREQ1# — DV26
GPP_D5/SRCCLKREQ0# — DW32
20191211(EVT) Follow GPIO review

XTAL_OUT — DM1 — XTL_38D4M_X2_CPU
XTAL_IN — DL1 — XTL_38D4M_X1_CPU
GPD8/SUSCLK — DW41 — SUSCLK
RTCX2 — DT47 — XTL_32K_X2_CPU
RTCX1 — DR47 — XTL_32K_X1_CPU
RTCRST# — DN37 — RTC_RST#
SRTCRST# — DK37 — SRTC_RST#

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M.2 SSD: SSD_CLK_CPU_P, SSD_CLK_CPU_N
WLAN
R1819 60D4R2F-GP — XCLK_BIASREF

20191204(EVT) Change RN1805 to R1801
3D3V_S0 — R1801 10KR2J-3-GP — CLK_PCIE_NVME_REQ#

20191216(EVT) Add R1802 PU 10K Follow ICAT 13 CML
3D3V_S0 — R1802 10KR2J-3-GP — SATA_LED#
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

RTC_AUX_S5 — RN1802 SRN20KJ-1-GP — SRTC_RST#, RTC_RST#
G1801 GAP-OPEN — C1803 SC1U10V2KX-1DLGP — C1804 SC1U10V2KX-1DLGP
Layout: Place at the open door area.

DJ6: TS_SPI_CLK
DN5: TS_SPI_IO3
DR9: TS_SPI_IO2
DM6: TS_SPI_SO
DK6: TS_SPI_SI
DK8: TS_SPI_CS#

DW9: DGPU_HOLD_RST#
DK13: SPK_ID
DM13: AUD_PWR_EN
DN13: HOST_SD_WP#
DJ15: WWAN_DB_DET#
DM15: USBC1_AUX_P_BIAS

DV14: USBC1_AUX_N_BIAS
DT24: CLK_PCIE_SD_REQ#
DT30: CLK_PCIE_LAN_REQ#
DK21: MEM_SMBCLK
DN19: MEM_SMBDATA
DN19: SMLB_ALERT#

XTL_32K_X2_CPU
XTL_32K_X1_CPU
R1811 10MR2J-L-GP
C1802 SC15P50V2JN-DL-GP — X1801 XTAL-32D768KHZ-88-GP — C1801 SC15P50V2JN-DL-GP
082.30003.0191
2nd = 082.30003.0301
20191223(EVT) c1=C2 default

20191217(EVT) Follow Nakia N7 TGL Intel check list
XTL_38D4M_X1_CPU — R1834 0R2J-2-GP — XTL_38D4M_X1_CPU_R
XTL_38D4M_X2_CPU — R1835 0R2J-2-GP — XTL_38D4M_X2_CPU_R
R1820 200KR2F-L-GP
C1806 SC12P50V2JN-DL-GP — X1802 XTAL-38D4MHZ-38-GP — C1805 SC12P50V2JN-DL-GP
082.30040.0241
2nd = 082.30040.0251
3rd = 082.30040.0231
20200304(DVT1) BOM use 082.30040.0251 main 082.30040.0241 2nd

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00
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Follow Hellcat15 Upsell TGL

Audio

- HDA_SYNC_CODEC
- HDA_BITCLK_CODEC
- HDA_SDOUT_CODEC
- HDA_SDIN0_CPU
- HDA_SDO
- DMIC_PCH_CLK
- DMIC_PCH_DATA

GPU

G SENSOR

- FFS_INT2

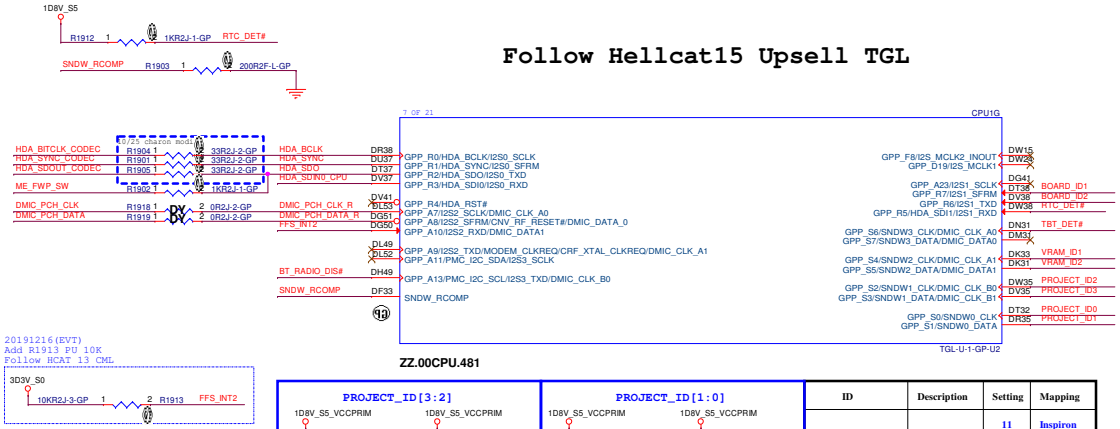
RTC

- RTC_DET#

BT

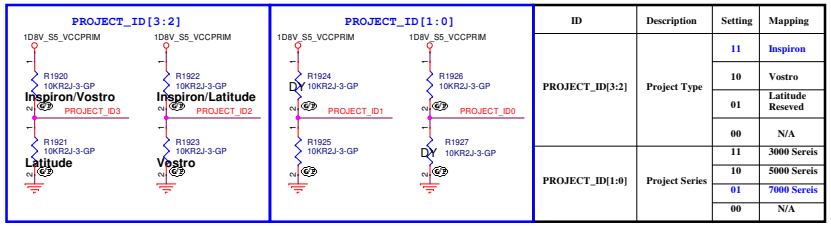
- BT_RADIO_DIS#

- ME_FWP_SW



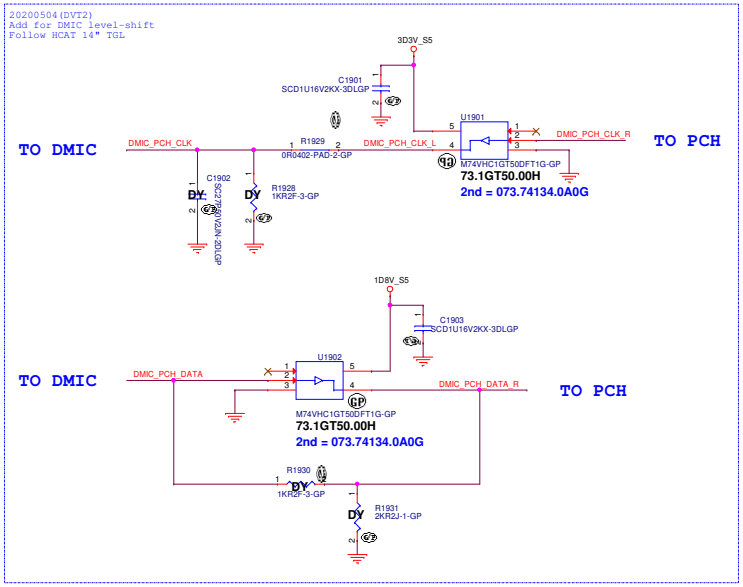
ZZ.00CPU.481

20191216(EVT)
Add R1913 PU 10K
Follow HCAT 13 CML



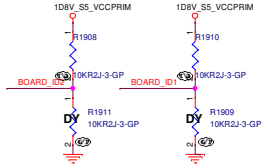
ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude Reseved
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Sereis
		01	7000 Sereis
		00	N/A

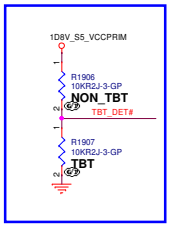
20200504(DVT2)
Add for DMIC level-shift
Follow HCAT 14" TGL



CY19 Board ID Mapping table

ID	Description	Setting	Mapping
Board ID[2:1]	Board SKU ID	11	HCAT 13" TGL
		10	N/A
		01	TGL-UP4
		00	TGL-UP3

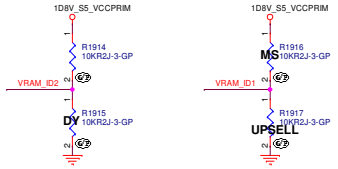




ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	no TBT
		0	Have TBT

CY19 VRAM ID Mapping table

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)

Size	Document Number	Rev
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TOUCH PAD/E3
65,66 PCH_I2C1_SCL_TP
65,66 PCH_I2C1_SDA_TP

G SENSOR
66 FFS_INT1
55,66 ISH_I2C0_ACC_SCL
55,66 ISH_I2C0_ACC_SDA
66 GSEN2_INT1_C
55 ISH_ACC1_INT#

AUDIO
27 SPKR

KEYBOARD
65 KB_LED_BL_DET

OTHER
24 TABLE_MODE#
24 NB_MODE#
55 P_GPIO

MEMORY
18 MEM_CHA_EN
21 MEM_DIE_CFG1

PCH to Type-C PD
71 I2C5_SCL
71 I2C5_SDA

eDP
55 DBC_PANEL_EN

LID
24,67,92 LID_CL_SIO#

68 UART_2_CTXD_DRXD
68 UART_2_CRXD_DTXD

55 ISH_I2C1_ALS_SDA
55 ISH_I2C1_ALS_SCL

TOUCH
55 I2C0_SDA_TS
55 I2C0_SCL_TS
55 TOUCH_DETECT
55 TOUCH_PANEL_INTR#
55 ALS_INT#
24,67 LID_CL_SIO_TAB#
55 CAM_SHUTTER#

DA51: NRB_BIT
DC49: VGA_DB_DET#
CY49: TPM_PIRQ#
CY53: GC6_THM_DIS#_PCH
CY52: PCH_3.3V_TS_EN
DA50: HDD_FALL_INT
DV21: SBIOS_TX
DR21: USBC0_AUX_N_BIAS
DW21: USBC0_AUX_P_BIAS
DV19: DGPU_MACO_EN
DT19: SIO_EXT_WAKE#
DR18: PCH_HDD_EN
DU19: LCD_CBL_DET#
DG23: cTPM_PRSNT#
DJ19: TOUCH_PANEL_INTR#
DF21: TOUCH_I2C_DET#
DV18: I2C0_SCL_TS
DW18: I2C0_SDA_TS
DF29: DBC_PANEL_EN
DG29: LOM_CABLE_DETECT#
DF25: CNV_COEX1
DF27: CNV_COEX2
DR27: STYLUS_PWR_OCP#
DW27: CAM_SHUTTER#
DT25: IO_DB_DET#
CY39: ISH_I2C1_ALS_SCL
DB47: ISH_I2C1_ALS_SDA
DD47: ISH_I2C2_SCL
DD44: ISH_I2C2_SDA
DJ8: ISH_P_SENSOR_INT#
DV31: ISH_ALS_INT#
DG17: ZPODD_PWR_EN#
DG19: ZPODD_DA#

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MEM_CHB_EN → DC53 GPP_B16/GSPI0_CLK; DA51 GPP_B18/GSPI0_MOSI
SPKR → DC49 GPP_B17/GSPI0_MISO; DC50 GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#; DC52 GPP_B15/GSPI0_CS0#
TP2010 1 GC6_THM_DIS#_PCH → CY49 GPP_B20/GSPI1_CLK; CY53 GPP_B22/GSPI1_MOSI; CY52 GPP_B21/GSPI1_MISO; DA50 GPP_B19/GSPI1_CS0#
FFS_INT1 → DV21 GPP_C9/UART0_TXD; DT21 GPP_C8/UART0_RXD; DR21 GPP_C11/UART0_CTS#; DW21 GPP_C10/UART0_RTS#
TOUCH_DETECT → R2050 1 2 0R0402-PAD-2-GP → TOUCH_DETECT_CPU
20191211(EVT) Stuff R2050 GPIO review
DV19 GPP_C13/UART1_TXD/ISH_UART1_TXD; DT18 GPP_C12/UART1_RXD/ISH_UART1_RXD; DR18 GPP_C15/UART1_CTS#/ISH_UART1_CTS#; DU19 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
20191213(EVT) Swap modify
UART_2_CTXD_DRXD → DJ21 GPP_C21/UART2_TXD
UART_2_CRXD_DTXD → DG23 GPP_C20/UART2_RXD
TOUCH_PANEL_INTR# → DJ19 GPP_C23/UART2_CTS#; DF21 GPP_C22/UART2_RTS#
I2C0_SCL_TS → DV18 GPP_C17/I2C0_SCL
I2C0_SDA_TS → DW18 GPP_C16/I2C0_SDA
PCH_I2C1_SCL_TP → DJ23 GPP_C19/I2C1_SCL
PCH_I2C1_SDA_TP → DT18 GPP_C18/I2C1_SDA
DJ29 GPP_H5/I2C2_SCL; DJ31 GPP_H4/I2C2_SDA
DBC_PANEL_EN → DF29 GPP_H7/I2C3_SCL
MEM_DIE_CFG1 → DG29 GPP_H6/I2C3_SDA
20191224(EVT) Change from GPP_H15 -> GPP_H6
DF25 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD; DF27 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

TOUCH
PCH to Touch Pad / E3
SDA/SCL/INT Pull UP on TP side(page65)
PCH to Type-C PD
SDA/SCL/INT Pull UP on PD side(page72)

GPP_D14/ISH_UART0_TXD → DR27 CAM_SHUTTER#; DW27 KB_LED_BL_DET
GPP_D13/ISH_UART0_RXD → DV25
GPP_D16/ISH_UART0_CTS# → DT25
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5
20200219(DVT1) GPP_C10 -> GPP_D16 Follow GPIO table
GPP_B6/ISH_I2C0_SCL → DB45 ISH_I2C0_ACC_SCL
GPP_B5/ISH_I2C0_SDA → DB44 ISH_I2C0_ACC_SDA
Accelerometer sensor
GPP_B8/ISH_I2C1_SCL → CY39 ISH_I2C1_ALS_SCL
GPP_B7/ISH_I2C1_SDA → DB47 ISH_I2C1_ALS_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL → DD47 I2C5_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA → DD44 I2C5_SDA
20200218(DVT1) Follow Nak's
GPP_E16/ISH_GP7 → DJ8 ISH_P_SENSOR_INT# R2006 2 0R0402-PAD-2-GP P_GPIO
GPP_E15/ISH_GP6 → DR7 LID_CL_SIO_TAB# 1 0R0402-PAD-2-GP LID_CL_SIO#
GPP_D18/ISH_GP5 → DR24 ISH_LID_CL#_NB R2001 1 0R0402-PAD-2-GP
GPP_D17/ISH_GP4 → DU25 ISH_NB_MODE
GPP_D3/ISH_GP3/BK3/SBK3 → DV31 ISH_ALS_INT# R2057 1 0R0402-PAD-2-GP ALS_INT#
GPP_D2/ISH_GP2/BK2/SBK2 → DU31 ISH_TABLE_MODE# R2009 2 0R0402-PAD-2-GP TABLE_MODE#
GPP_D1/ISH_GP1/BK1/SBK1 → DT27 ISH_ACC2_INT# R2025 1 2 0R0402-PAD-2-GP GSEN2_INT1_C
GPP_D0/ISH_GP0/BK0/SBK0 → DV27 ISH_ACC1_INT#
20191206(EVT) Follow HCAT DG1
GPP_RCOMP → DR51 GPP_RCOMP R2021 1 200R2F-L-GP
GPP_T3/I2C7_SCL → DN33
GPP_T2/I2C7_SDA → DT33
GPP_U5/GSPI3_CLK → DG17
GPP_U4/GSPI3_CS0# → DG18

TGL-U-1-GP-U2
ZZ.00CPU.481

3D3V_S0
ISH_I2C0_ACC_SCL R2051 2 1 2K2R2J-2-GP
ISH_I2C0_ACC_SDA R2052 2 1 2K2R2J-2-GP
UART_2_CRXD_DTXD R2048 51KR2J-1-GP DEBUG
UART_2_CTXD_DRXD R2049 51KR2J-1-GP DEBUG
20191210(EVT) Add PU 51K Follow HCAT 13 CML

Pull high to enable DDR
1D8V_S5 R2031 10KR2J-3-GP MEM_CHA_EN R2030 10KR2J-3-GP DY
1D8V_S5 R2033 10KR2J-3-GP MEM_CHB_EN R2032 10KR2J-3-GP DY

20191210(EVT) Add R2018 100k Follow HCAT 13 CML
ISH_NB_MODE → R2018 100KR2J-1-GP
Q2001 PJA138KA-GP
3D3V_S5 R2005 10KR2J-3-GP NB_MODE#
084.00138.0A31
2nd = 084.00138.0C31

20191206(EVT) Follow HCAT DG1
3D3V_HINGE_S0 R2010 1 10KR2J-3-GP P_GPIO

<Core Design>

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Title: CPU (UART/I2C/ISH)
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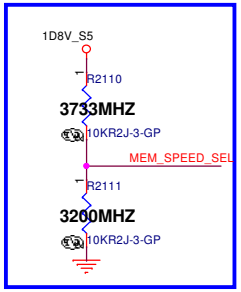
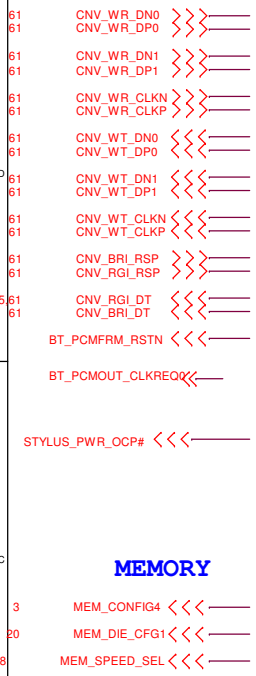
Follow Nakia Shuri N7

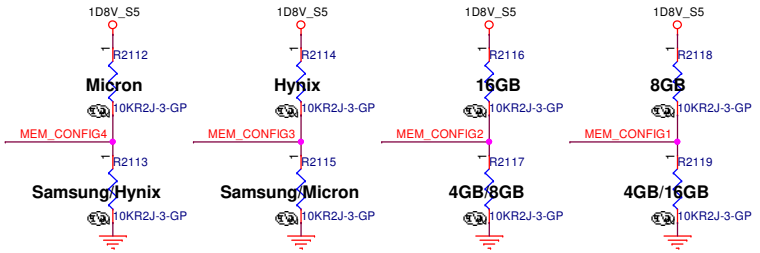
ID	Description	Setting	Mapping
MEM_Speed SEL	Speed Configuration	1	3733MHz
		0	3200MHz





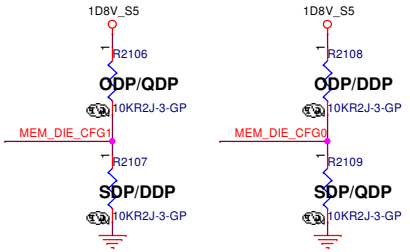
MEM_CONFIG Mapping table

ID	Description	Setting	Mapping
MEM_CONFIG[4:3]	On-board memory configuration for chip vendor	11	DIMM Design
		10	Micron
		01	Hynix
		00	Samsung
MEM_CONFIG[2:1]	On-board memory configuration for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	QDP/DDP Configuration	1	QDP
		0	DDP



CY19 Board ID Mapping table

ID	Description	Setting	Mapping
MEM_Die CONFIG[1:0]	SDP/DDP/QDP/ODP Configuration	11	ODP
		10	QDP
		01	DDP
		00	SDP



<Core Design>

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Title: CPU (CSI/EMMC/CNVi)

Size: A3 | Document Number: Hellcat 13" TGL | Rev: A00

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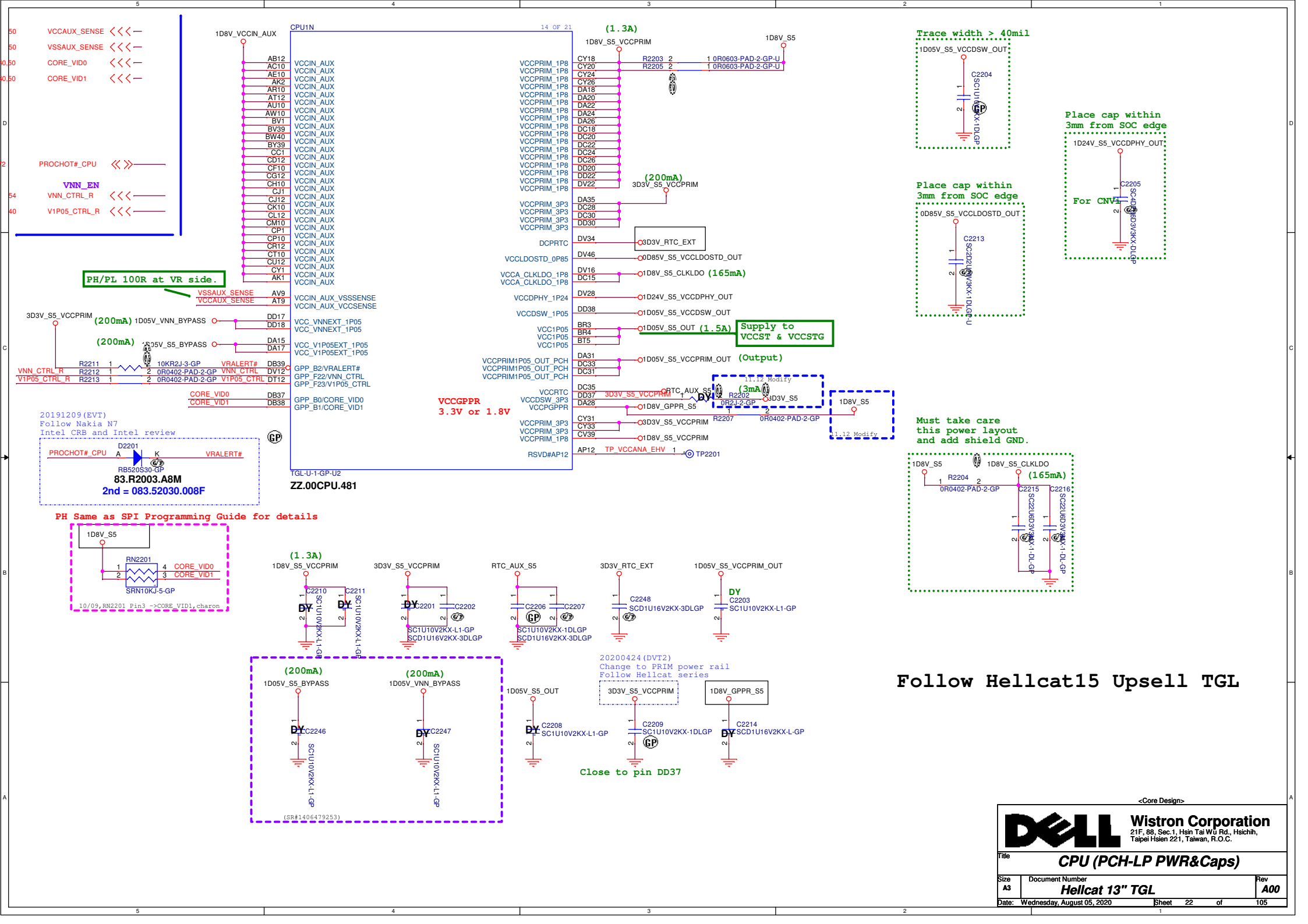

<Core Design>
Wistron Corporation
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Title	CPU (PCH-LP PWR&Caps)	
Size: A3	Document Number: Hellcat 13" TGL	Rev: A00
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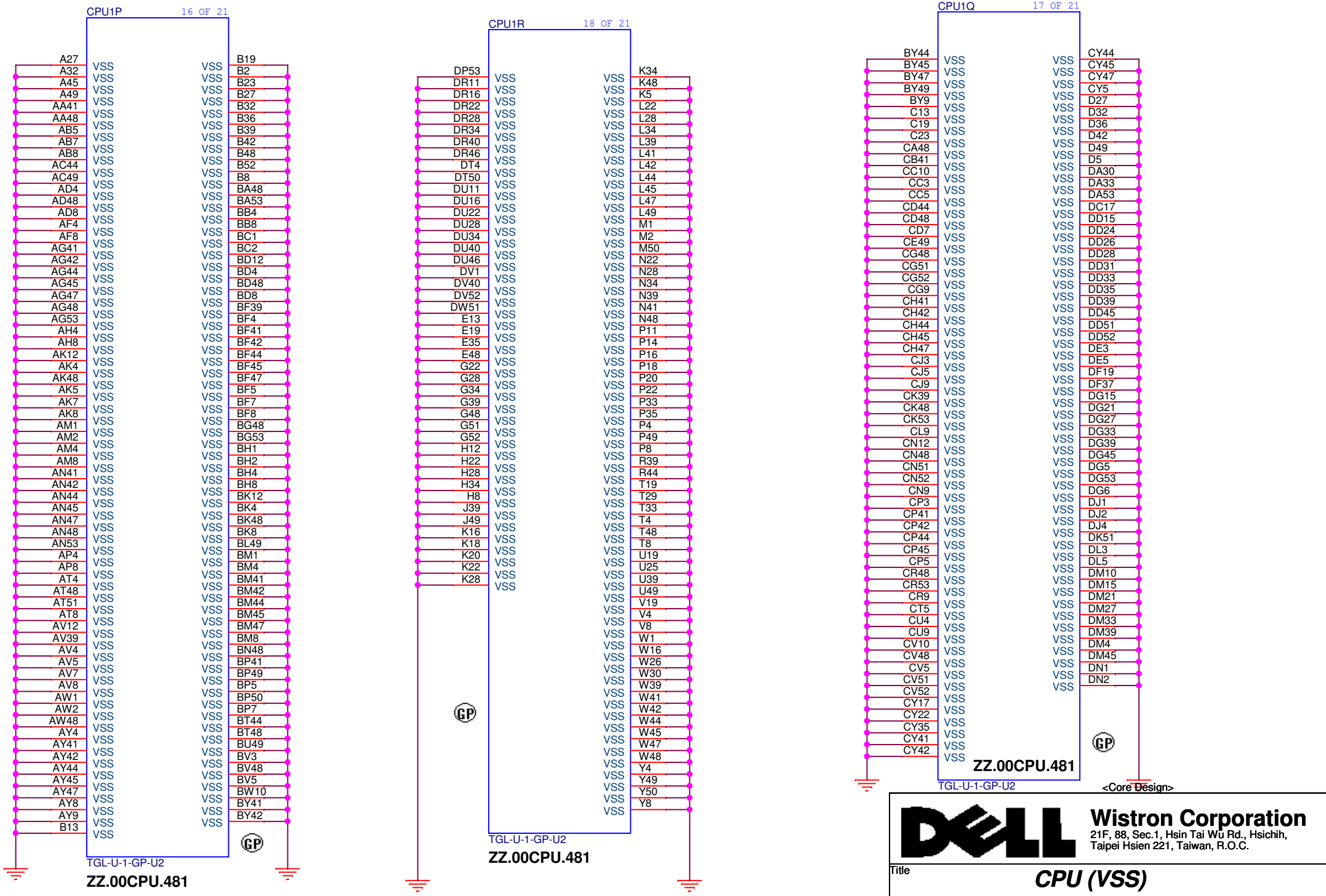
CPU1P
16 OF 21
A27 A32 A45 A49 AA41 AA48 AB5 AB7 AB8 AC44 AC49 AD4 AD48 AD8 AF4 AF8 AG41 AG42 AG44 AG45 AG47 AG48 AG53 AH4 AH8 AK12 AK4 AK48 AK5 AK7 AK8 AM1 AM2 AM4 AM8 AN41 AN42 AN44 AN45 AN47 AN48 AN53 AP4 AP8 AT4 AT48 AT51 AT8 AV12 AV39 AV4 AV5 AV7 AV8 AW1 AW2 AW48 AY4 AY41 AY42 AY44 AY45 AY47 AY8 AY9 B13
VSS
B19 B2 B23 B27 B32 B36 B39 B42 B48 B52 B8 BA48 BA53 BB4 BB8 BC1 BC2 BD12 BD4 BD48 BD8 BF39 BF4 BF41 BF42 BF44 BF45 BF47 BF5 BF7 BF8 BG48 BG53 BH1 BH2 BH4 BH8 BK12 BK4 BK48 BK8 BL49 BM1 BM4 BM41 BM42 BM44 BM45 BM47 BM8 BN48 BP41 BP49 BP5 BP50 BP7 BT44 BT48 BU49 BV3 BV48 BV5 BW10 BY41 BY42
GP
TGL-U-1-GP-U2
ZZ.00CPU.481
CPU1R
18 OF 21
DP53 DR11 DR16 DR22 DR28 DR34 DR40 DR46 DT4 DT50 DU11 DU16 DU22 DU28 DU34 DU40 DU46 DV1 DV40 DV52 DW51 E13 E19 E35 E48 G22 G28 G34 G39 G48 G51 G52 H12 H22 H28 H34 H8 J39 J49 K16 K18 K20 K22 K28
VSS
K34 K48 K5 L22 L28 L34 L39 L41 L42 L44 L45 L47 L49 M1 M2 M50 N22 N28 N34 N39 N41 N48 P11 P14 P16 P18 P20 P22 P33 P35 P4 P49 P8 R39 R44 T19 T29 T33 T4 T48 T8 U19 U25 U39 U49 V19 V4 V8 W1 W16 W26 W30 W39 W41 W42 W44 W45 W47 W48 Y4 Y49 Y50 Y8
GP
TGL-U-1-GP-U2
ZZ.00CPU.481
CPU1Q
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BY44 BY45 BY47 BY49 BY9 C13 C19 C23 CA48 CB41 CC10 CC3 CC5 CD44 CD48 CD7 CE49 CG48 CG51 CG52 CG9 CH41 CH42 CH44 CH45 CH47 CJ3 CJ5 CJ9 CK39 CK48 CK53 CL9 CN12 CN48 CN51 CN52 CN9 CP3 CP41 CP42 CP44 CP45 CP5 CR48 CR53 CR9 CT5 CU4 CU9 CV10 CV48 CV5 CV51 CV52 CY17 CY22 CY35 CY41 CY42
VSS
CY44 CY45 CY47 CY5 D27 D32 D36 D42 D49 D5 DA30 DA33 DA53 DC17 DD15 DD24 DD26 DD28 DD31 DD33 DD35 DD39 DD45 DD51 DD52 DE3 DE5 DF19 DF37 DG15 DG21 DG27 DG33 DG39 DG45 DG5 DG53 DG6 DJ1 DJ2 DJ4 DK51 DL3 DL5 DM10 DM15 DM21 DM27 DM33 DM39 DM4 DM45 DN1 DN2
GP
TGL-U-1-GP-U2
ZZ.00CPU.481
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (VSS)
Size
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Main Func = KBC

#	MODEL_ID(GPIO202)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	14" UMA	100.0K (64.10035.6DL)	10.0K (64.10025.6DL)	3
2	13" UPSELL UMA	100.0K	17.8K (64.17825.6DL)	2.801
3	13" MS/15" MS UMA	100.0K	27.0K (64.27025.6DL)	2.598
4	17" CS UMA	100.0K	37.4K (64.37425.6DL)	2.402
5	15" UPSELL UMA	100.0K	49.9K (64.49925.6DL)	2.201
6	17" 2in1 UMA	100.0K	64.9K (64.64925.6DL)	2.001
7	14"/15" MS DIS	100.0K	82.5K (64.82525.6DL)	1.808
8	17" CS DIS	100.0K	107K (64.10735.6DL)	1.594
9	15" UPSELL DIS	100.0K	154K (64.15435.6DL)	1.299
10	17" 2in1 DIS	100.0K	200K (64.20035.6DL)	1.1

#	BOARD_ID(GPIO204)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K (64.10035.6DL)	10.0K (64.10025.6DL)	3
2	X01	100.0K	17.8K (64.17825.6DL)	2.801
3	X02	100.0K	27.0K (64.27025.6DL)	2.598
4	X03(Reserve)	100.0K	37.4K (64.37425.6DL)	2.402
5	A00	100.0K	49.9K (64.49925.6DL)	2.201
6	A01	100.0K	64.9K (64.64925.6DL)	2.001
7	A02	100.0K	82.5K (64.82525.6DL)	1.808
8	A03	100.0K	107K (64.10735.6DL)	1.594
9	Reserve	100.0K	154K (64.15435.6DL)	1.299
10	Reserve	100.0K	200K (64.20035.6DL)	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

MODEL ID

BOARD_ID

JTAG DEBUG CONN

For USB TypeC

For eSPI

EC G3 Flash Share

pull high on CPU side

Layout Note: Place close to Mec1515

Power Switch Logic(PSL)

Layout Placement Request

GPIO045 (CR_STRAP)

GPIO055 (BSS_STRAP)

Already pull low on CPU side

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS	BSS_STRAP	Boot Source Select Strap: 1=Use the Shared SPI pins for Bootblock 2 0=Use the eSPI Flash Channel for Boot New	VTR2

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS# pin is used as an indication that the Shared SPI is powered. This pin must be at a High level when the Shared SPI is powered. See Table 2-6, "Strap Pins".

There is presently a requirement for a pull-up resistor on the SHD_CS# pin on the board if the Shared SPI flash interface is used so that the SPI CS# is detected high while RSMRST# is low.

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ECIO(MEC 1515)

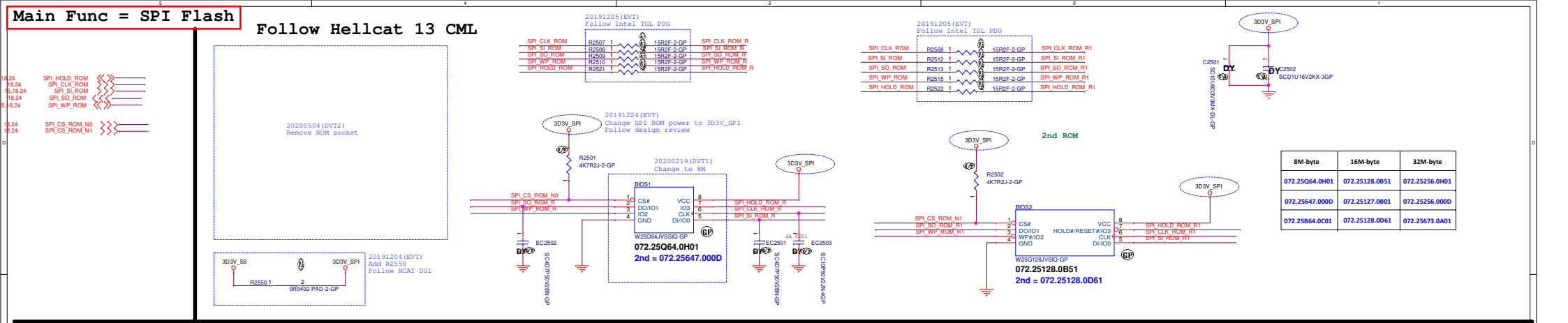
Helicat 13" TGL

A00

Wednesday, August 05, 2020

Main Func = SPI Flash

Follow Hellcat 13 CML



8M-byte	16M-byte	32M-byte
072.25Q64.0H01	072.25128.0B51	072.25256.0H01
072.25647.000D	072.25127.0B01	072.25256.000D
072.25864.0C01	072.25128.0D61	072.25673.0A01

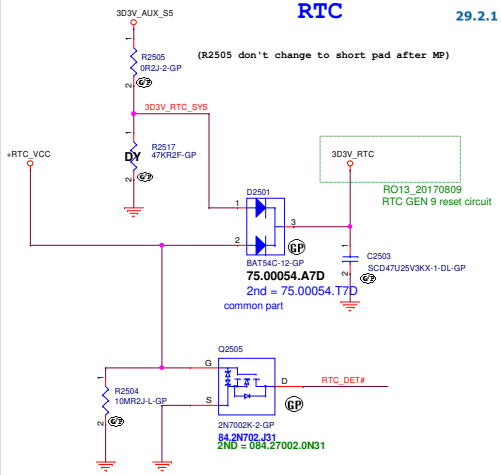
Main Func = RTC

Delivery Voltage 3.19V

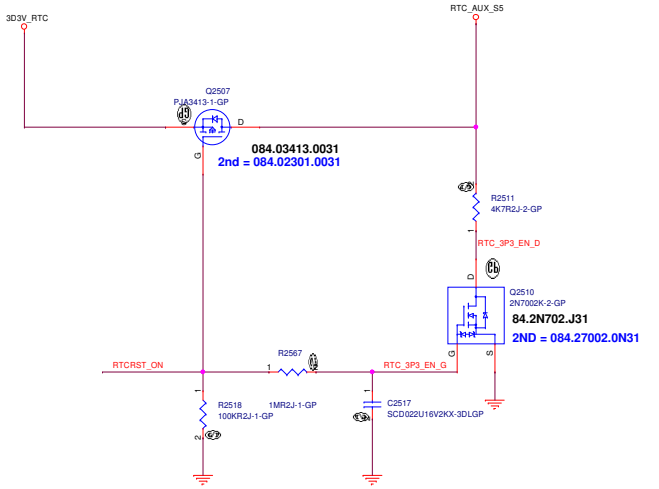
RTC

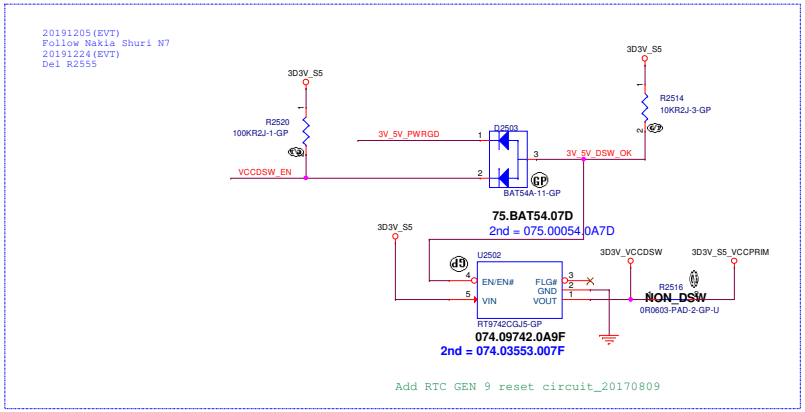
29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



Follow Hellcat 13 CML





Hynix 8G

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

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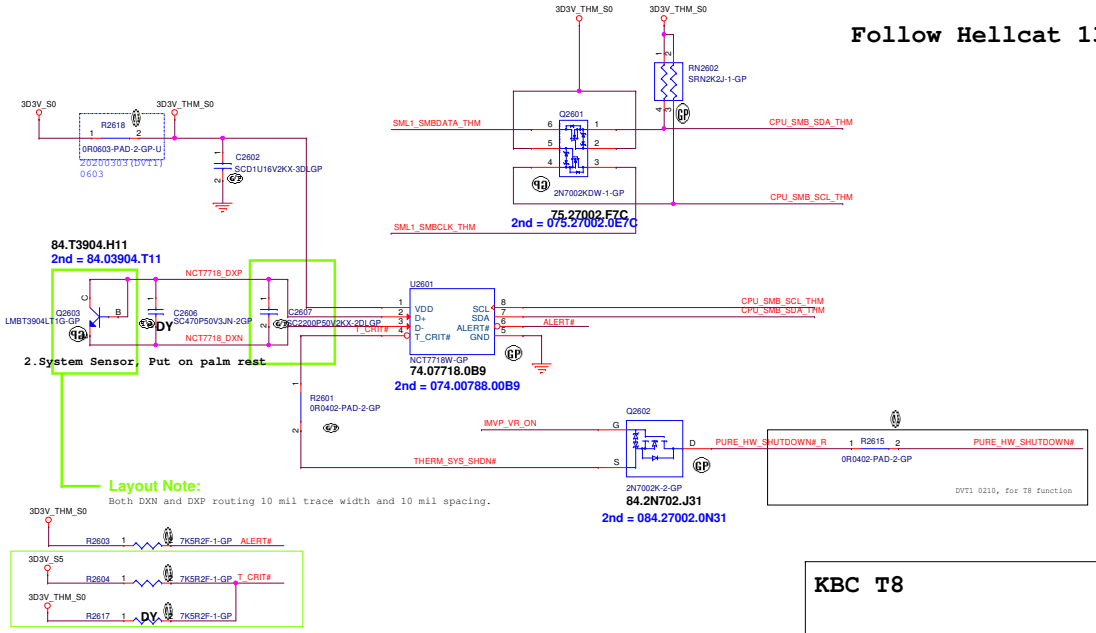
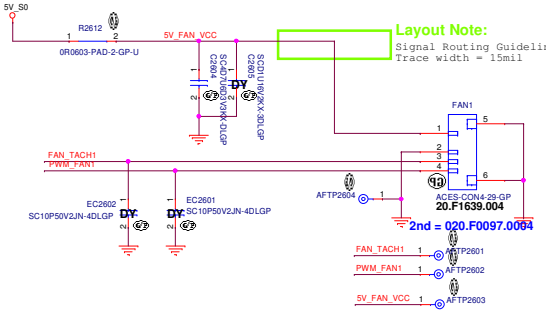
Main Func = Thermal Sensor

18,24 SML1_SMBCLK_THM
18,24 SML1_SMBDATA_THM
17,24 IMVP_VR_ON
40 PURE_HW_SHUTDOWN#
24 FAN_TACH1
24 PWM_FAN1

Follow Hellcat 13 CML



PWM FAN1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8

Close to KBC

Hynix 8G

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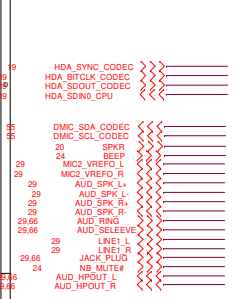
Title: INT IO (Thermal/Fan)

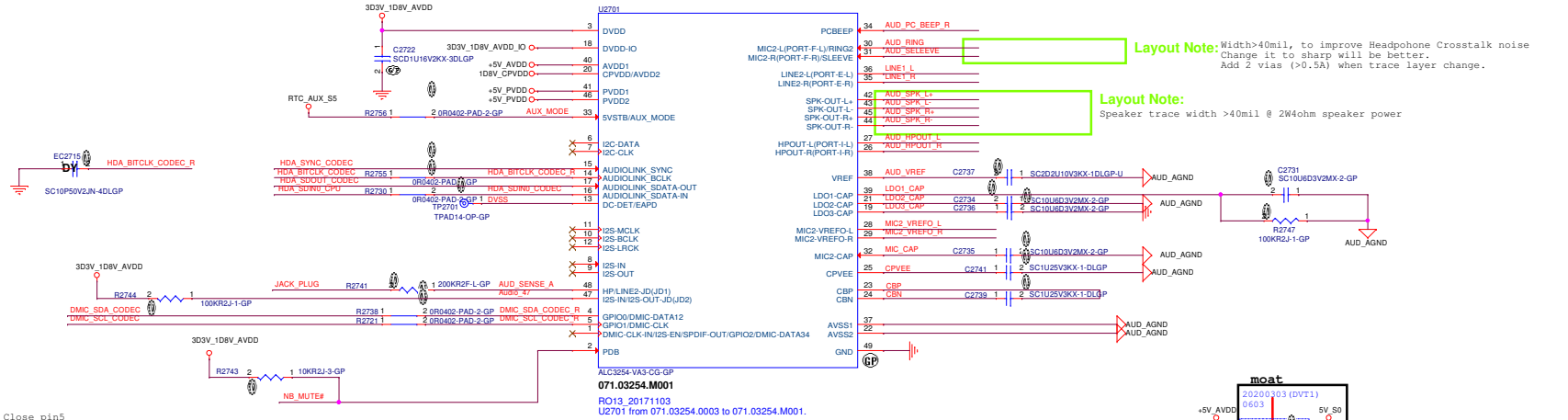
Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 26 of 106

Main Func = Audio

Follow Hellcat 13 CML





Hynix 8G

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Title: Audio (Codec ALC3254)

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	***Hellcat 13" TGL***	***A00***

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Main Func = Audio

27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R+
27 AUD_SPK_R-

18 SPK_ID
27 MIC2_VREFO_R
27 MIC2_VREFO_L
27,66 AUD_RING
,66 AUD_HPOUT_L
27 LINE1_L
66 AUD_HPOUT_R
27 LINE1_R
66 AUD_SELEEVE

27,66 JACK_PLUG

Follow Hellcat 13 CML

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

RO13_20171002
follow ME connector list

AUD_SPK_L+ — ER2902 2 — 1 0R0402-PAD-2-GP — AUD_SPK_L+_C
AUD_SPK_L- — ER2901 2 — 1 0R0402-PAD-2-GP — AUD_SPK_L-_C
AUD_SPK_R+ — ER2904 2 — 1 0R0402-PAD-2-GP — AUD_SPK_R+_C
AUD_SPK_R- — ER2903 2 — 1 0R0402-PAD-2-GP — AUD_SPK_R-_C

AUD_SPK_L+_C
AUD_SPK_L-_C
AUD_SPK_R+_C
AUD_SPK_R-_C

ED2908 AZ5725-01FDR7G-GP
ED2907 AZ5725-01FDR7G-GP
ED2906 AZ5725-01FDR7G-GP
ED2905 AZ5725-01FDR7G-GP

AUD_SPK_L-_C — AFTP2901
AUD_SPK_L+_C — AFTP2902
AUD_SPK_R-_C — AFTP2903
AUD_SPK_R+_C — AFTP2904

SC1KP50V2KX-1DLGP EC2901
SC1KP50V2KX-1DLGP EC2902
SC1KP50V2KX-1DLGP EC2903
SC1KP50V2KX-1DLGP EC2904

SPK_ID

SPK1
ACES-CON6-20-GP-U
20.F1639.006
2nd = 020.F1263.0006

CONN Pin	Net name
Pin1	SPK_L+_C
Pin2	SPK_L-_C
Pin3	SPK_R+_C
Pin4	SPK_R-_C
Pin5	GND
Pin6	SPK_DET#_CON

Follow Hellcat 13 CML

RN2901
SRN2K2J-1-GP

MIC2_VREFO_R
MIC2_VREFO_L
AUD_RING
AUD_HPOUT_L
LINE1_L — C2907 — SC10U6D3V3MX-DL-GP
AUD_HPOUT_R
LINE1_R — C2908 — SC10U6D3V3MX-DL-GP
AUD_SELEEVE

Delay circuit

(JACK_PLUG_DET: on IO Board)

JACK_PLUG — 10 mils — 10 mils
JEDI 13_20180706
C2909 SC10U6D3V3MX-DL-GP
AUD_AGND

Hynix 8G

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio (HP/SPK/MIC Jack)*

Size: A3 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 29 of 106

(Blanking)

<Core Design>

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Title

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Size	Document Number	Rev
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Main Func = LAN

(Blanking)

<Core Design>

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Title: LAN(RSV)

Size	Document Number	Rev
A4	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 31 of 105

Main Func = LAN

(Blanking)

<Core Design>

Wistron Corporation
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Title: RJ45&Transformer(RSV)

Size: A3 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 32 of 105

Main Func = Card Reader

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader_RTL5170(RSV)

Size	Document Number	Rev
A4	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 33 of 105

Main Func = USB2.0

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD) (USB 2.0 CONN)

Size | Document Number: Hellcat 13" TGL | Rev: A00

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(Blanking)

Hynix 8G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB3.0 Conn)

Size | Document Number: Hellcat 13" TGL | Rev: A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD) (USB Charger)

Size	Document Number	Rev
A3	Hellcat 13" TGL	A00

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB3.0 PORT

Size	Document Number	Rev
A4	Hellcat 13" TGL	A00

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(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Hellcat 13" TGL***	***A00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(RSVD)

Size	Document Number	Rev
A3	*Hellcat 13" TGL*	*A00*

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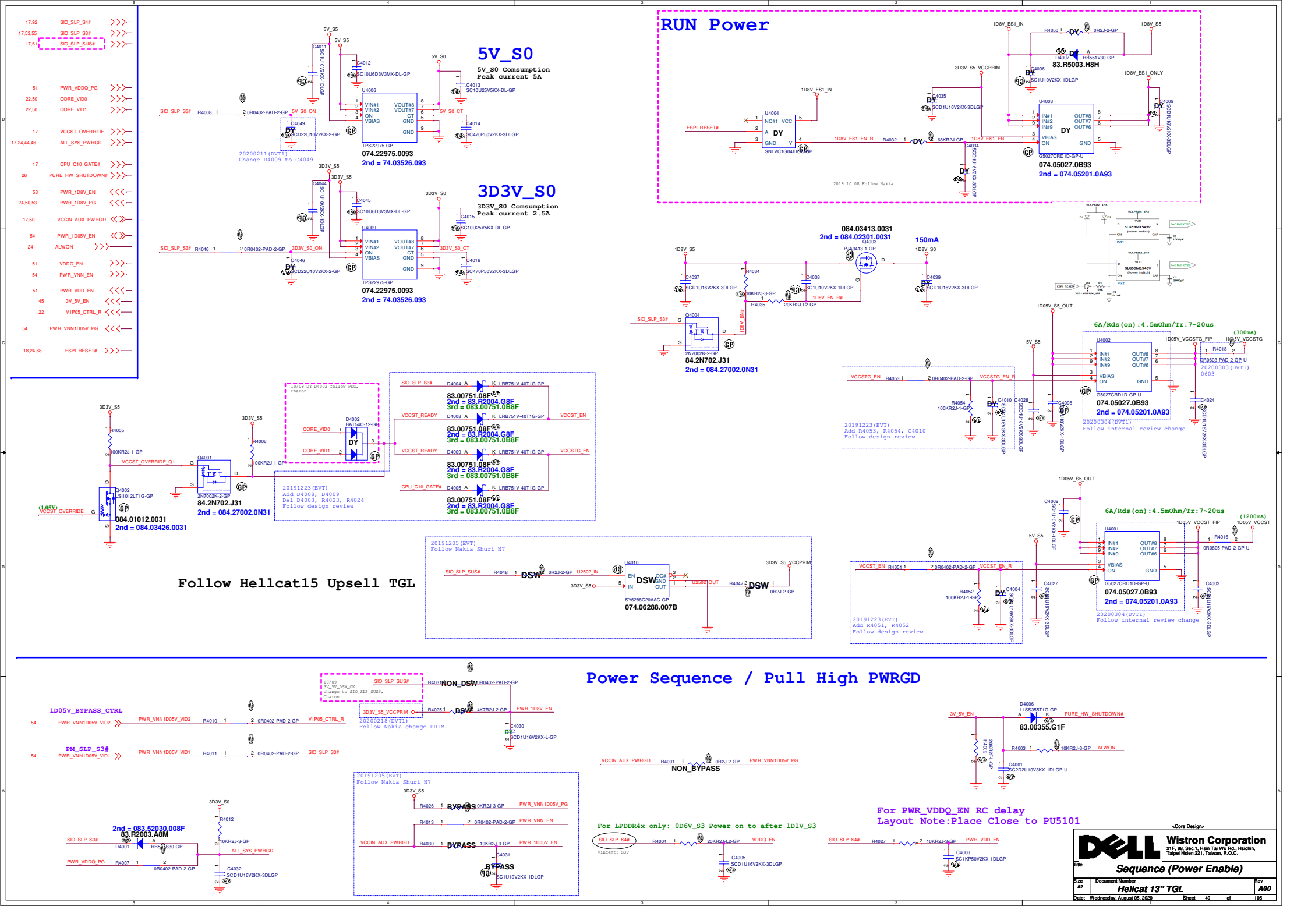
17,92 SIO_SLP_S4#
17,53,55 SIO_SLP_S3#
17,61 SIO_SLP_SUS#
51 PWR_VDDQ_PG
22,50 CORE_VID0
22,50 CORE_VID1
17 VCCST_OVERRIDE
17,24,44,46 ALL_SYS_PWRGD
17 CPU_C10_GATE#
26 PURE_HW_SHUTDOWN#
53 PWR_1D8V_EN
24,50,53 PWR_1D8V_PG
17,50 VCCIN_AUX_PWRGD
54 PWR_1D05V_EN
24 ALWON
51 VDDQ_EN
54 PWR_VNN_EN
51 PWR_VDD_EN
45 3V_5V_EN
22 V1P05_CTRL_R
54 PWR_VNN1D05V_PG
18,24,68 ESPI_RESET#
5V_S0
5V Comsumption
Peak current 5A
TPS22975-GP
074.22975.0093
2nd = 74.03526.093
20200211(DVT1)
Change R4009 to C4049
3D3V_S0
3D3V_S0 Comsumption
Peak current 2.5A
RUN Power
2019.10.08 Follow Nakia
83.R5003.H8H
084.03413.0031
2nd = 084.02301.0031
150mA
PJA3413-1-GP
84.2N702.J31
2nd = 084.27002.0N31
6A/Rds(on):4.5mOhm/Tr:7~20us
(300mA)
(1200mA)
G5027CRD1-GP-U
074.05027.0B93
2nd = 074.05201.0A93
20200304(DVT1)
Follow internal review change
20191223(EVT)
Add R4053, R4054, C4010
Follow design review
Add R4051, R4052
Add D4008, D4009
Del D4003, R4023, R4024
Follow design review
084.01012.0031
2nd = 084.03426.0031
83.00751.08F
2nd = 83.R2004.G8F
3rd = 083.00751.0B8F
Follow Hellcat15 Upsell TGL
20191205(EVT)
Follow Nakia Shuri N7
SY6288C20AAC-GP
074.06288.007B
Power Sequence / Pull High PWRGD
1D05V_BYPASS_CTRL
PM_SLP_S3#
NON_BYPASS
BYPASS
83.00355.G1F
2nd = 083.52030.008F
83.R2003.A8M
For LPDDR4x only: 0D6V_S3 Power on to after 1D1V_S3
For PWR_VDDQ_EN RC delay
Layout Note:Place Close to PU5101
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Sequence (Power Enable)
Size A2
Document Number
Hellcat 13" TGL
Rev A00
Date: Wednesday, August 05, 2020
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V-tree_VCCIO

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (V-Tree)

Size: A3 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 41 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(RSVD)*

Size	Document Number	Rev
A4	Hellcat 13" TGL	A00

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Main Func = ADT Input

Follow Hellcat15 Upsell TGL

Layout Note:
PSID Layout width > 25mil

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

S1

Move S2 MOSFET and control logic SCH to page 44

If=0.3A

Main Func = M-BAT Input

Batt Connecter

Placement: Close to Batt Connector

Barrel Adapter Piug-in Detect
Follow Bandon

20190621 Hellcat15 N7 X00

<Core Design>

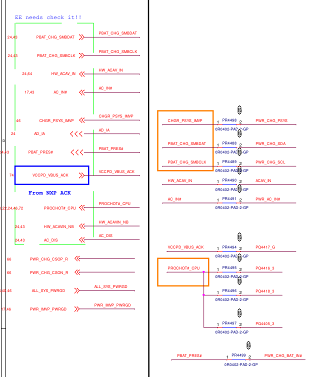
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (ATX/ DC/ BATT Conn)
Size: Custom | Document Number: Hellcat 13" TGL | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 43 of 105

Main Func = Charger

ISL9538H For Charger

OFFPAGE



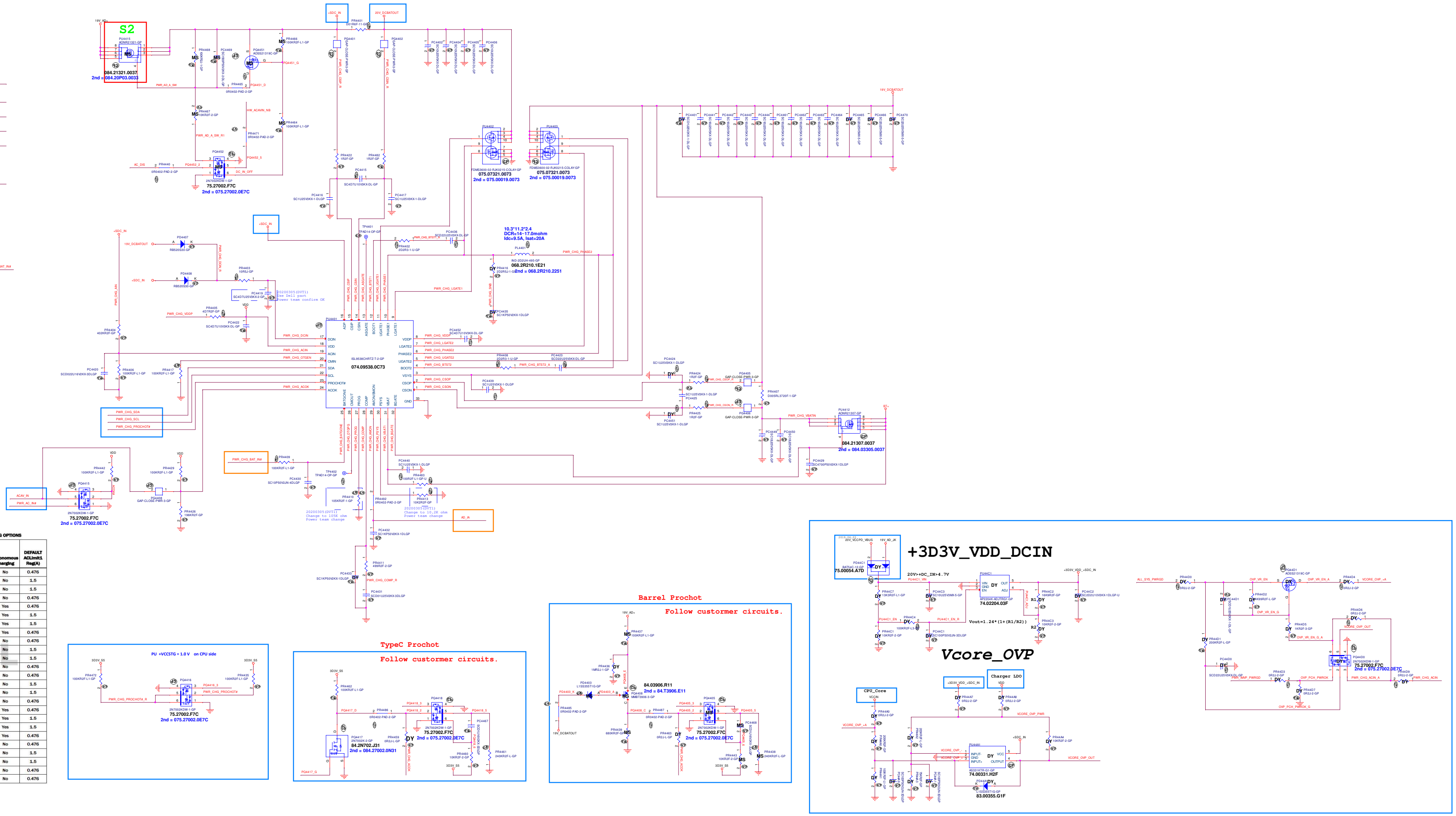


TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

RO UMA/DIS 2IN1

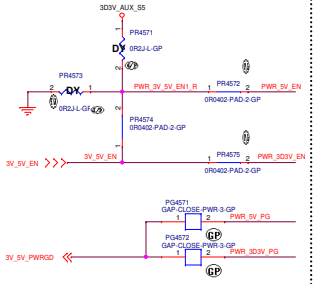
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (CHARGER_ISL9538HRTZ)

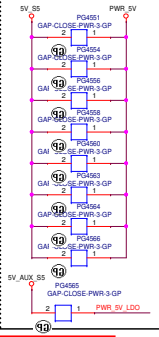
Size: A0 | Document Number: Hellcat 13" TGL | Rev: A00

SSID = PWR.Plane.Regulator_5V

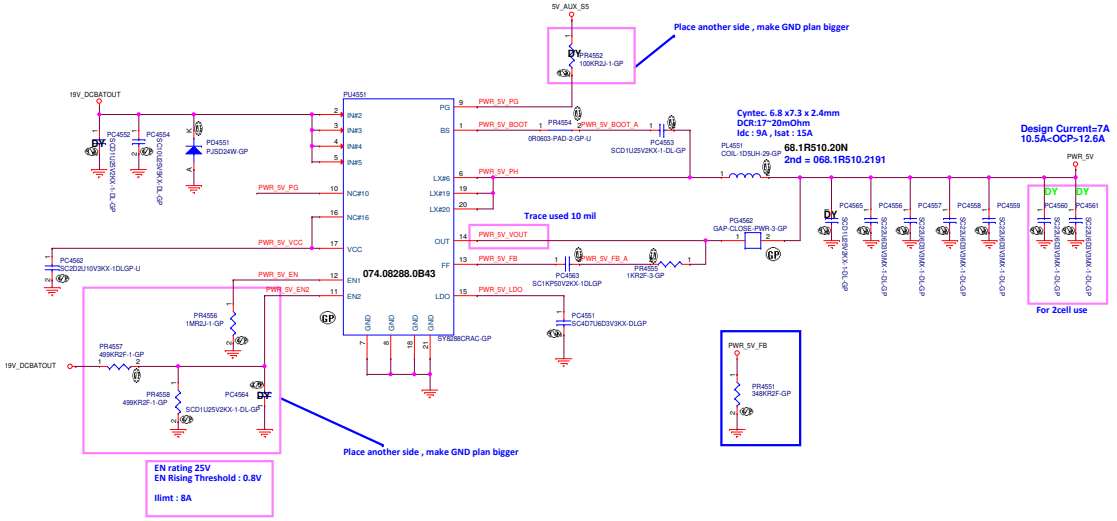
OFFPAGE-Signal



OFFPAGE-GAP



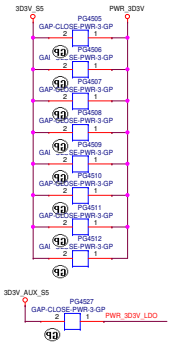
SY8288C For 5V



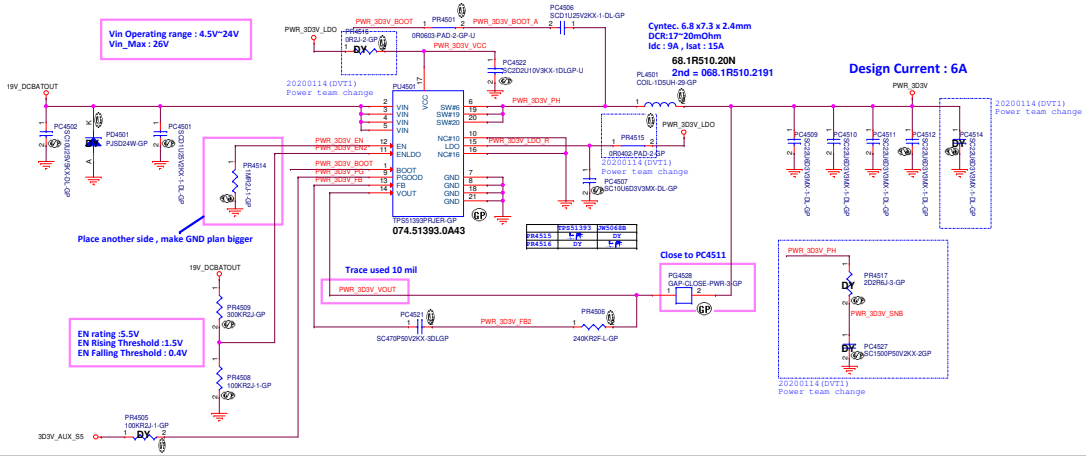
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP



TPS51393 For 3D3V



DVT2 remove FPR S5 SSO

RO UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8286_5V/3D3V)

Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00

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Main Func = CPU_CORE

OFFPAGE

SVID

- SVID_CLK_CPU (7) — PR4632 0R0402-PAD-2-GP — PWR_VCORE_SCLK_R
- SVID_DATA_CPU (7) — PR4633 0R0402-PAD-2-GP — PWR_VCORE_SDIO_R
- SVID_ALERT#_CPU (7) — PR4634 0R0402-PAD-2-GP — PWR_VCORE_ALERT#_R

- CHGR_PSYS_IMVP (44) — PR4688 0R0402-PAD-2-GP — PWR_CORE_PSYS
- PROCHOT#_CPU (4,44,72) — PR4631 0R0402-PAD-2-GP — PWR_VCORE_VRHOT_R

- PWR_IMVP_PWRGD (7,44) — PR4636 0R0402-PAD-GP — PWR_VCORE_VR_READY
- ALL_SYS_PWRGD (5) — PR4635 0R0402-PAD-2-GP — PWR_VCORE_VR_EN

VCORE SENSE

- VSSCORE_SENSE (7) — VSSCORE_SENSE
- VCCCORE_SENSE (7) — VCCCORE_SENSE

- PWR_VCORE_UGATE1 (47) — PWR_VCORE_UGATE1
- PWR_VCORE_PHASE1 (47) — PWR_VCORE_PHASE1
- PWR_VCORE_LGATE1 (47) — PWR_VCORE_LGATE1

- PWR_VCORE_UGATE2 (47) — PWR_VCORE_UGATE2
- PWR_VCORE_PHASE2 (47) — PWR_VCORE_PHASE2
- PWR_VCORE_LGATE2 (47) — PWR_VCORE_LGATE2

- PWR_VCORE_ISEN2 (47) — PWR_VCORE_ISEN2
- PWR_VCORE_ISEN1 (47) — PWR_VCORE_ISEN1
- PWR_VCORE_ISUMP (47) — PWR_VCORE_ISUMP
- PWR_VCORE_ISUMN (47) — PWR_VCORE_ISUMN

1D05V_VCCST

20191203(EVT)
Follow Nakia shuri N7

PR4606 100R2F-L1-GP-U
PR4621 100R2F-L1-GP-U
PR4622 100R2F-L1-GP-U
PR4623 100R2F-L1-GP-U
PR4624 100R2F-L1-GP-U

DY PC4626 SCD1U25V2KX-1-DL-GP — Close to IC

PR4603 1KR2F-3-GP

PWR_VCORE_SCLK_R
PWR_VCORE_ALERT#_R
PWR_VCORE_SDIO_R

5V_S5

PR4607 100R2F-L1-GP-U — PWR_VCORE_VRHOT_R

PR4617 0R0402-PAD-2-GP

3D3V_S0

PR4609 10KR2F-2-GP

PC4613 SC1U10V2KX-1DLGP

PR4601 0R0402-PAD-2-GP — 19V_DCBATOUT

PC4601 SCD22U25V2KX-4-GP

PWR_VCORE_VR_READY

PWR_VCORE_VR_EN

PC4612 SC4700P50V2KX-1DLGP

PR4602 12K1R2F-L1-GP

PC4609 SC330P50V2KX-3-DL-GP

PR4608 93K1R2F-L-GP

PROG1
VBOOT: 0V
F=750kHz

PR4619 78K7R2F-GP

PR4620 9K31R2F-GP

PU4601
ISL95869HRTZ-T-GP
074.95869.0073

PWR_CORE_PSYS
PWR_VCORE_IMON
PWR_VCORE_NTC
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_RTN
PWR_VCORE_ISUMN

PSYS
IMON
NTC
COMP
FB
RTN
ISUMN
ISUMP

PROG1
PROG2
BOOT1
UGATE1
PHASE1
LGATE1
PWM3
VDDP

PWR_VCORE_PROG1
PWR_VCORE_PROG2
PWR_VCORE_BOOT1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_VCORE_LGATE1
PWR_VCORE_VDDP

PR4621 0R0603-PAD-2-GP-U — PWR_VCORE_BOOT1_N
PC4610 SCD22U25V2KX-4-GP

PR4625 0R0402-PAD-2-GP — O5V_S5

PC4625 SC1U10V2KX-1DLGP

PR4616 10KR2F-2-GP

PWR_VCORE_NTC_N

B=4500

PR4655 27K4R2F-GP

PR4618 NTC-470K-17-GP

PR4611 0R0603-PAD-2-GP-U — PWR_VCORE_BOOT2_N
PC4611 SCD22U25V2KX-4-GP

O5V_S5

PWR_VCORE_ISEN2
PWR_VCORE_ISEN1

20200522(DVT2)
Change to 1.5K ohm
Power team change

PR4615 1K5R2F-2-GP

PC4608 SC82P50V2JN-3-DL-GP

PWR_VCORE_COMP_N

20200110(DVT1)
Change to 392 ohm
Power team change

PR4614 2KR2F-3-GP DY
PR4613 392R2F-GP
PR4612 392R2F-GP

PC4607 SC1U10V2KX-3DLGP

PC4606 SC330P50V2KX-3-DL-GP DY

PWR_VCORE_FB1
PWR_VCORE_FB2
PWR_VCORE_FB4

VCCCORE_SENSE

PR4667 0R0402-PAD-2-GP

PR4640 100R2F-L1-GP-U

VCCIN

PC4604 SC820P50V2KX-1-DL-GP

PR4665 0R0402-PAD-2-GP

PWR_VCORE_FB3

PC4615 SCD01U25V2KX-3DLGP DY

PR4666 0R0402-PAD-2-GP

VSSCORE_SENSE

PC4605 SC330P50V2KX-3-DL-GP

PC4638 SC330P50V2KX-3-DL-GP

PR4626 100R2F-L1-GP-U

PC4623 SC2200P50V2KX-2DLGP

PWR_VCORE_ISUMN_N

PR4628 3K48R2F-GP

PR4627 523R2F-GP

PC4614 SCD22U25V2KX-3DLGP

PC4618 SCD22U25V2KX-3DLGP

PR4629 0R0402-PAD-2-GP — PWR_VCORE_ISUMP_N

PC4616 SCD22U25V2KX-3DLGP

PC4602 SCD1U10V2KX-3DLGP

PR4653 2K61R2F-1-GP

PR4630 11KR2F-L-GP

PR4650 NTC-10K-29-GP-U — B=3370

PWR_VCORE_ISUMP
PWR_VCORE_ISUMNP_2
PWR_VCORE_ISUMN

PC4603 SCD01U25V2KX-3DLGP

20200514(DVT2)
Change to common part
Confirm with power team ok

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (ISL95869_VCORE(1/2))

Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

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Main Func = VCCIN

OFFPAGE

PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_VCORE_LGATE1
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_VCORE_LGATE2
PWR_VCORE_ISEN2
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN

19V_DCBATOUT → PWR_DCBATOUT_VCOREA

R4701 R4702 R4703 R4704 R4705 R4706 R4707 R4708 0R0805-PAD-2-GP-U

20191202(EVT)
Change to 0 ohm 0805
Power team suggest 2 phase = 8pcs

PWR_DCBATOUT_VCOREA

PC4702 PC4703 PC4704 PC4705 SC101U25V3MX-6-GP
PC4706 SC2D1U25V2KX-1DL-GP

20200424(DVT2)
For acoustic noice cost down
DY TC4701, change TC4702 to 100uF

PWR_DCBATOUT_VCOREA

DY TC4701 ST33U25VDM-6-GP
077.53361.0021
2nd = 077.23361.0001

TC4702 ST100U25VDM-1-GP
077.C1071.0071
2nd = 077.C1071.0101

TGL_U42 28W
Performance
TDC=38A
ICCMAX=62A

PWR_VCORE_LGATE1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_DCBATOUT_VCOREA

PU4701 AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073

PWR_VCORE_PHASE1

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

20191203(EVT)
High limit change, follow HCAT13 CML
Confirmed with power team.

PL4701 COL-D15UH-8-GP
068.R1510.2091
2nd = 068.R1510.2111

VCCIN

PT4701 SE330U2D5VDM-2GP
79.3371V.2PL
2nd = 80.3371V.L01

PT4702 SE330U2D5VDM-2GP
79.3371V.2PL

DY PR4705 2D2R6J-3-GP
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP

PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP

PWR_VCORE_ISUMP_GA

PWR_VCORE_ISUMN_GA

PWR_VCORE_ISEN1
PR4721 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4708 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN2

PR4709 10R2F-L-GP
PR4722 100KR2F-L1-GP

PWR_DCBATOUT_VCOREA

PC4717 PC4714 PC4716 PC4715 SC101U25V3MX-6-GP
PC4718 SC2D1U25V2KX-1DL-GP

PWR_VCORE_LGATE2
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_DCBATOUT_VCOREA

PU4702 AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073

PWR_VCORE_PHASE2

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

20191203(EVT)
High limit change, follow HCAT13 CML
Confirmed with power team.

PL4702 COL-D15UH-8-GP
068.R1510.2091
2nd = 068.R1510.2111

VCCIN

DY PR4714 2D2R6J-3-GP
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP

PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP

PWR_VCORE_ISUMP_GB

PWR_VCORE_ISUMN_GB

PWR_VCORE_ISEN2
PR4723 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4716 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN1

PR4715 10R2F-L-GP
PR4724 100KR2F-L1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (ISL95869_VCORE(2/2))

Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

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Main Func = CPU_CORE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (IMVP9_RESERVE)

Size: A3 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 48 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

POWER (RSVD)

Size	Document Number	Rev
A	***Hellcat 13" TGL***	***A00***

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Main Func = VCCIN_AUX

OFFPAGE

VID

22,40 CORE_VID0 — PR5014 0R0402-PAD-2-GP — PWR_VCCIN_AUX_VID0

22,40 CORE_VID1 — PR5015 0R0402-PAD-2-GP — PWR_VCCIN_AUX_VID1

24,53 PWR_1D8V_PG — PR5012 0R0402-PAD-2-GP — PWR_VCCIN_AUX_EN_R

40 VCCIN_AUX_PWRGD — PR5013 0R0402-PAD-2-GP — PWR_VCCIN_AUX_PG

VCCIN_AUX SENSE

22 VCCAUX_SENSE — PR5017 0R0402-PAD-2-GP — PWR_VCCIN_AUX_FB_O

22 VSSAUX_SENSE — PR5018 0R0402-PAD-2-GP — PWR_VCCIN_AUX_RGND

19V_DCBATOUT — R5002 0R1206-PAD-1-GP — PWR_DCBATOUT_VCCSA

19V_DCBATOUT — R5003/R5004/R5005/R5006 0R0805-PAD-2-GP-U — PWR_VCCIN_AUX_IN

20191203(EVT)
Change to 0 ohm 0805
Power team suggest 4pcs

PWR_VCCIN_AUX_IN — PC5006/PC5007/PC5012/PC5013 SC1U10V6KX-GP

PWR_VCCIN_AUX_BOOT — PC5009 SC1U10V2KX-1DLGP

PU5001 RT6543AGQW-GP 074.06543.0073

Pin	Net
CS_DIS	PWR_VCCIN_AUX_CS
PVCC	PWR_VCCIN_AUX_VCC
VCC	PC5008 SC1U10V2KX-1DLGP
PG	PWR_VCCIN_AUX_PG
EN	PWR_VCCIN_AUX_EN
VID1	PWR_VCCIN_AUX_VID1
VID0	PWR_VCCIN_AUX_VID0
FSWSEL	PR5003 10KR2F-2-GP
BOOT	PC5009 SC1U10V2KX-1DLGP
VSYS	PWR_VCCIN_AUX_IN
UG	PWR_VCCIN_AUX_UG
PH	PWR_VCCIN_AUX_LX
LG	PWR_VCCIN_AUX_LG
PGND	
ISENSEP	PWR_VCCIN_AUX_ISENP
ISENSEN	PWR_VCCIN_AUX_ISENN
VOUT	1D8V_VCCIN_AUX
COMP	PWR_VCCIN_AUX_COMP
FB	PWR_VCCIN_AUX_FB
RGND	PWR_VCCIN_AUX_RGND
AGND	

PR5001 2D2R2J-GP — PC5010 SC1U10V2KX-1DLGP — PR5002 133KR2F-GP — PR5004 10KR2F-2-GP (3D3V_S5) — PR5005 2D2R2J-GP

PWR_VCCIN_AUX_IN — PU5002 / PU5003 FDMS3600-02-RJK0215-COLAY-GP 075.07321.0073 2nd = 075.00019.0073

PL5001 COIL-D22UH-2-GP 68.R2210.20D

Cyntec. 6.8 x 7.3 x 3mm
DCR: 2.5~2.8 mOhm
Idc : 23A , Isat : 40A

20191205(EVT)
High limit change
Confirmed with power team.

1D8V_VCCIN_AUX — PT5001 SE330U2D5VDM-2GP 79.3371V.2PL 2nd = 80.3371V.L01

PR5021 17K8R2F-GP — PC5011 SCD1U25V2KX-1-DL-GP — PR5016 0R0402-PAD-2-GP — PR5007 100R2F-L1-GP-U

PR5008 240R2F-1-GP — PWR_VCCIN_AUX_RC — PR5022 732R2F-GP — PR5023 NTC-10K-29-GP-U B=3370K

PC5003 SC2200P50V2KX-2DLGP — PWR_VCCIN_AUX_COMP_R — PR5011 10KR2F-2-GP

PC5002 SC470P50V2KX-3DLGP — PWR_VCCIN_AUX_FB_R — PR5009 1K6R2F-GP

PC5004 SC22P50V2JN-4DLGP — PR5010 5K62R2F-GP

PR5006 100R2F-L1-GP-U — PR5020 0R0402-PAD-2-GP

PWR_VCCIN_AUX_FB_O

TGL_U42 28W
Performance
TDC=16A
ICCMAX=32A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT6543A_VCCIN_AUX)

Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

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OFFPAGE

S5(PM_SLP_S4#)

40 PWR_VDD_EN → PWR_VDD_EN

S3(VTT_CNTL)

40 VDDQ_EN → VDDQ_EN

PH on EE Side

40 PWR_VDDQ_PG → PWR_VDDQ_PG

OFFPAGE_GAP

19V_DCBATOUT → PWR_DCBATOUT_VDDQ

R5101 0R1206-PAD-1-GP

20200505(DVT2)
Change Gap to 1206 size for E3 board
Confirm with power team

1D1V_S3 → PWR_VDDQ

PG5131 GAP-CLOSE-PWR-3-GP
PG5132 GAP-CLOSE-PWR-3-GP
PG5121 GAP-CLOSE-PWR-3-GP
PG5120 GAP-CLOSE-PWR-3-GP
PG5125 GAP-CLOSE-PWR-3-GP
PG5122 GAP-CLOSE-PWR-3-GP
PG5129 GAP-CLOSE-PWR-3-GP
PG5130 GAP-CLOSE-PWR-3-GP

1D1V_S3 → PWR_VDDQ_VLDOIN

PG5124 GAP-CLOSE-PWR-3-GP

DD6V_VREF_S0 → PWR_VDDQ_VTT

PR5122 0R0402-PAD-2-GP

1P8V_S3 → PWR_VDDQ_1D8V

PG5126 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VDDQ

PC5117 SCD1U25V2KX-1-DL-GP
PC5101 SC10U25V5KX-DL-GP
PC5102 SC10U25V5KX-DL-GP

PWR_VDDQ_VLDOIN

PC5103 SC10U6D3V3MX-DL-GP

5V_S5 → PR5110 0R2F-1-GP

PWR_VDDQ_VCC

PC5113 SC2D2U10V3KX-1DLGP-U

3D3V_S5 → PR5107 0R0402-PAD-2-GP

PR5108 100KR2F-L1-GP

PWR_VDDQ_VDD1

PC5104 SC10U6D3V3MX-DL-GP
PC5116 SCD1U16V2KX-3DLGP

PWR_VDDQ_PG
PWR_VDD_EN
PWR_VDDQ_EN

VDDQ_EN → PR5101 0R0402-PAD-2-GP

PU5101
TPS51487XRJER-1-GP
074.51487.M002

PVIN, VLDOIN, VCC_5V, PVIN_VDD1, PGOOD, VDD_EN, VDDQ_EN
BST, SW, VDD2SNS, VDDQ, VDDQSNS, VDDQREF, SW_VDD1, VDD1SNS, PGND_VDD1, PGND, AGND

PWR_VDDQ_PH
PWR_VDDQ_SENSE
PWR_VDDQVTT_SENSE
PWR_VDDQ_VDDQREF
PWR_VDDQVID8V_PH
PWR_VDDQTD8V_SENSE

PWR_VDDQ_BOOT_A → PR5109 5D1R3F-GP

PWR_VDDQ_BOOT → PC5108 SCD1U25V2KX-1-DL-GP

20200114(DVT1)
Power team change

Cyntec. 6.6mmx7.3mmx3.0 mm
DCR:4.8~5.3mOhm
Idc :16A , Isat : 17A

VDDQ:Design Current=8A

PL5102 COIL-D68UH-20-GP
068.R6810.2111

20191203(EVT)
High limit change
Confirmed with power team.

PWR_VDDQ

PC5109 SC22U6D3V3MX-1-DL-GP
PC5110 SC22U6D3V3MX-1-DL-GP
PC5111 SC22U6D3V3MX-1-DL-GP
PC5112 SC22U6D3V3MX-1-DL-GP
PC5115 SC22U6D3V3MX-1-DL-GP

PR5106 2D2R6J-3-GP

PWR_VDDQ_SNB

PC5114 SC1500P50V2KX-2-DL-GP

PG5133 GAP-CLOSE-PWR-3-GP

PWR_VDDQ_VTT

VTT:Design Current=0.73A

PC5107 SC10U6D3V3MX-DL-GP

PR5104 0R0402-PAD-2-GP

20200114(DVT1)
Power team change

PC5106 SC1U10V2KX-1DLGP

PWR_VDDQ_1D8V

VDDQ:Design Current=0.2A

PL5101 IND-4D7UH-352-GP
068.4R710.1111
2nd = 068.4R710.1981

PC5105 SC22U6D3V3MX-1-DL-GP

PR5103 0R0402-PAD-2-GP

TOKO. 2.5mmx2.0mmX1.2mm
DCR: 240m Ohm
Idc : 1.3A , Isat :1.5A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (TPS51487X_VDDQVTT)

Size: Custom | Document Number: Hellcat 13" TGL | Rev: A00

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(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (RSVD)

Size: B | Document Number: Hellcat 13" TGL | Rev: A00

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Main Func = 1D8V/1D2V

OFFPAGE

PH on EE Side

PWR_1D8V_PG <<< PWR_1D8V_PG

PWR_1D8V_EN >>> PWR_1D8V_EN

EE confirm

PRIM_PWRGD <<< PRIM_PWRGD

SIO_SLP_S3# >>> SIO_SLP_S3#

OFFPAGE_GAP

3D3V_S5 — PG5301 GAP-CLOSE-PWR-3-GP — PWR_1D8V_VIN

PG5302 GAP-CLOSE-PWR-3-GP

1D8V_S5 — PG5303 GAP-CLOSE-PWR-3-GP — PWR_1D8V

PG5304 GAP-CLOSE-PWR-3-GP

PG5305 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PG5306 GAP-CLOSE-PWR-3-GP — PWR_1D2V_VIN

20191223(EVT)
Change to S0 power

1D2V_S0 — PG8626 GAP-CLOSE-PWR-3-GP — PWR_1D2V

Design Current=1.7A

Chilisin. 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 4A

PWR_1D8V_VIN

PC5301 SC22U6D3V3MX-1-DL-GP

PU5301 RT5797ALGQW-GP
PGND, VIN, PG, FB, SGND, NC#5, LX, EN
074.05797.0073
2nd = 074.02822.0A43

PWR_1D8V_PG
PWR_1D8V_EN
PWR_1D8V_FB
PWR_1D8V_PH

PL5301 IND-1UH-300-GP

PR5307 100KR2F-L1-GP — R1
PR5304 49K9R2F-L-GP — R2

PC5305 SC22P50V2JN-L-GP — DY

PC5302 SC22U6D3V3MX-1-DL-GP
PC5303 SC22U6D3V3MX-1-DL-GP

PWR_1D8V

PR5305 10KR2J-3-GP
20200310(DVT1)
Change PR5305 to 10k

PC5307 SC1U10V2KX-1DLGP — DY

Design Current=0.5A

PWR_1D2V_VIN

Vo=0.6x(1+R1/R2)
=0.6x(1+100/49.9)
=1.802V

5V_S5

3D3V_S5

PC5311 SC2D2U6D3V2MX-DL-GP

PR5301 1KR2F-3-GP

PC5312 SC10U6D3V3MX-DL-GP

PU5302 APL5934KAI-TRG-GP-U
VCNTL, POK, EN, VIN#9, VIN#5, VOUT#4, VOUT#3, FB, GND
074.05934.003D
2nd = 074.94611.003D

PRIM_PWRGD
PR5302 0R0402-PAD-2-GP

PWR_1D2V_POK
PWR_1D2V_EN
PWR_1D2V_FB_LDO

SIO_SLP_S3#
PR5303 0R0402-PAD-2-GP

20191223(EVT)
Change to S0 power

PR5311 47KR2J-2-GP — DY

PC5313 SC4700P50V2KX-1DLGP — DY

PR5312 18KR2F-GP — R1
PR5306 35K7R2F-GP — R2

PC5304 SC68P50V2JN-1DLGP — DY

PC5314 SC10U6D3V3MX-DL-GP — DY

PC5306 SC10U6D3V3MX-DL-GP

PWR_1D2V

Vo=0.8x(1+R1/R2)
=0.8x(1+18/35.7)
=1.203V

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (RT5797_1D8V_S5)	
Size: B	Document Number: Hellcat 13" TGL	Rev: A00
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OFFPAGE

PH on EE Side

VCCIN_AUX_PWRGD
40 PWR_VNN_EN >> PWR_VNN_EN

1D05V_BP_PWRGD
40 PWR_VNN1D05V_PG << PWR_VNN1D05V_PG

40 PWR_1D05V_EN >> PWR_1D05V_EN

PH on EE Side

1D05V_BYPASS_CTRL
40 PWR_VNN1D05V_VID2 >> PWR_VNN1D05V_VID2

PM_SLP_S3#
40 PWR_VNN1D05V_VID1 >> PWR_VNN1D05V_VID1

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

22 VNN_CTRL_R >> R5401 1 DY 2 0R2J-2-GP PWR_VNN1D05V_VID1

20191223(EVT)
Follow design review reserve

OFFPAGE-GAP

1D05V_VNN_BYPASS — R5499 1 2 0R0603-PAD-2-GP-U — PWR_VNN

1D05V_S5_BYPASS — R5498 1 2 0R0603-PAD-2-GP-U — PWR_1D05V

20200303(DVT1)
0603

3D3V_S5 — PR5420 1 100KR2J-1-GP 2 PWR_VNN1D05V_PG
DY

Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A

PL5401 IND-1UH-382-GP — PWR_VNN
PC5411 SC222U6D3V3MX-1-DL-GP
PC5412 SC222U6D3V3MX-1-DL-GP

5V_S5 — PR5413 2D2R2F-GP — PC5401 1 2 SC1U10V2KX-1DLGP

PC5402 SC4D7U25V3KX-2-GP
19V_DCBATOUT — PR5422 2 0R0402-PAD-2-GP — PR5410 1 2 0R0402-PAD-2-GP — PC5403 SC4D7U25V3KX-2-GP

PU5401

VCC	8	PWR_VNN1D05V_VCC	
VIN1	11	PWR_VNN1D05V_VINA	
VIN2	10	PWR_VNN1D05V_VINB	
VID1	13	PWR_VNN1D05V_VID1	
BOOT1	2	PWR_VNN1D05V_BOOTA	PC5404 1 2 SCD1U25V2KX-1-DL-GP
BOOT2	3	PWR_VNN1D05V_BOOTB	PC5405 1 2 SCD1U25V2KX-1-DL-GP
VID2	14	PWR_VNN1D05V_VID2	
POK	7	PWR_VNN1D05V_PG	PC5406 1 DY 2 SCD1U16V2KX-L-GP
EN1	15	PWR_VNN_EN	
EN2	6	PWR_1D05V_EN	
LX1	1	PWR_VNN1D05V_PHA	
LX2	4	PWR_VNN1D05V_PHB	
VOUT2	5	PWR_VNN1D05V_FB2	
VOUT1	16	PWR_VNN1D05V_VOUT1	
AGND	17		
PGND	9		
PGND	12		

APW8743CQBI-TRG-GP
074.08743.0A73

PR5423 1 0R0402-PAD-2-GP PWR_VNN1D05V_PHB
PR5401 1 2 0R0402-PAD-2-GP PWR_VNN1D05V_PHA

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A

PL5402 IND-10UH-330-GP — PWR_1D05V
PC5414 DY SC100P50V2JN-3GP
PR5408 0R0402-PAD-2-GP
PR5407 DY 0R2J-L-GP
PC5410 SC222U6D3V3MX-1-DL-GP
PC5413 SC222U6D3V3MX-1-DL-GP

PR5419 1 2 0R0402-PAD-2-GP PWR_VNN
PR5430 DY 0R2J-L-GP

3D3V_S5 3D3V_S5
PR5426 10KR2F-2-GP DY PWR_VNN1D05V_VID1
PR5427 10KR2F-2-GP DY PWR_VNN1D05V_VID2
PR5433 10KR2F-2-GP
PR5428 10KR2F-2-GP

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT5797_1D8V_S5)

Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00

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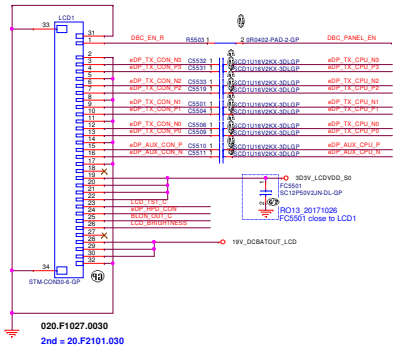
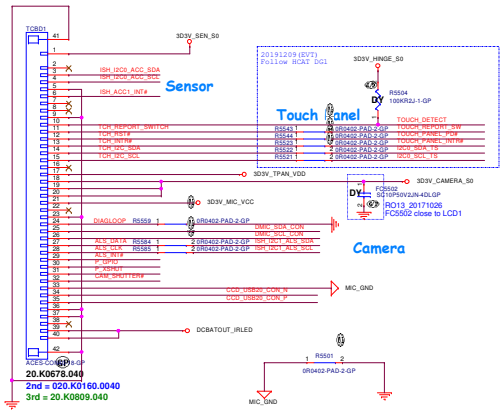
Main Func = LCD

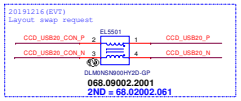
eDP Panel



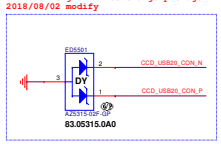
Sensor/TOUCH PANEL/IR Camera



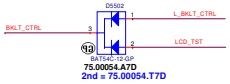
20191216 (EVT)
Layout swap request

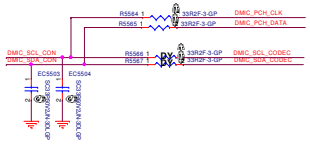


JEDI 13 height limite change package
2018/08/02 modify

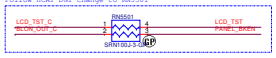


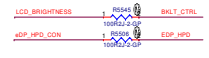
Follow Hellcat 13 CML

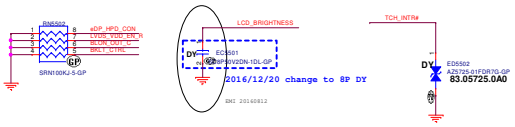




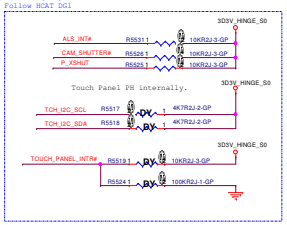
20191209(EVT)
Follow HCAT DG1 change to RN5501



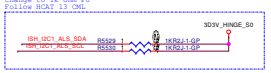




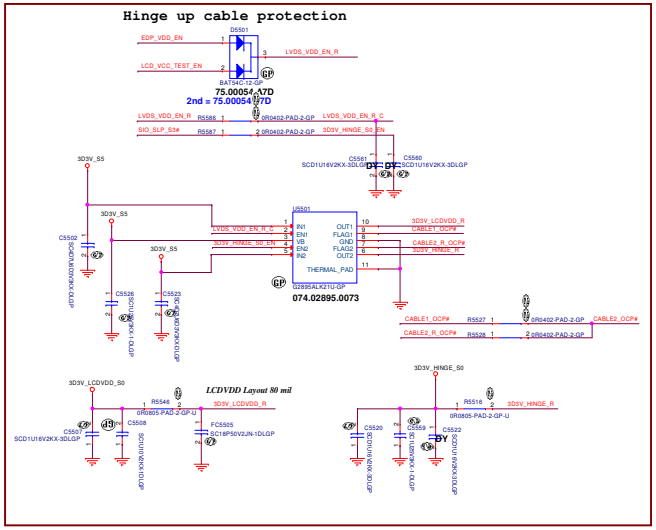
20191209(EVT)
Follow HCAT DG1



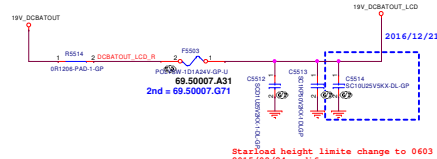
20200417(DVT2)
Change to 1k ohm PU
Follow HCAT 13 CML



Hinge up cable protection



INVERTER POWER

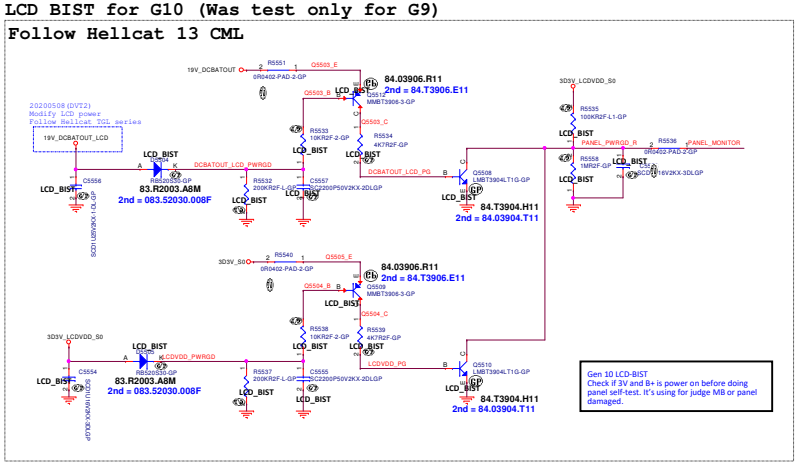


Starload height limite change to 0603 package
2015/09/24 modify

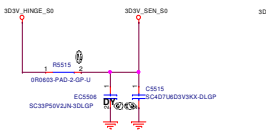
IR LED POWER

LCD BIST for G10 (Was test only for G9)

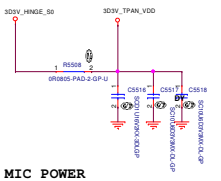
Follow Hellcat 13 CML



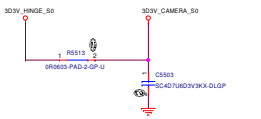
SENSOR POWER



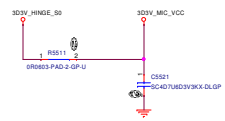
TOUCH PANEL POWER



CAMERA POWER



MIC POWER



Hynix BG

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD&CAM&DMC&Touch	
Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00
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<Core Design>

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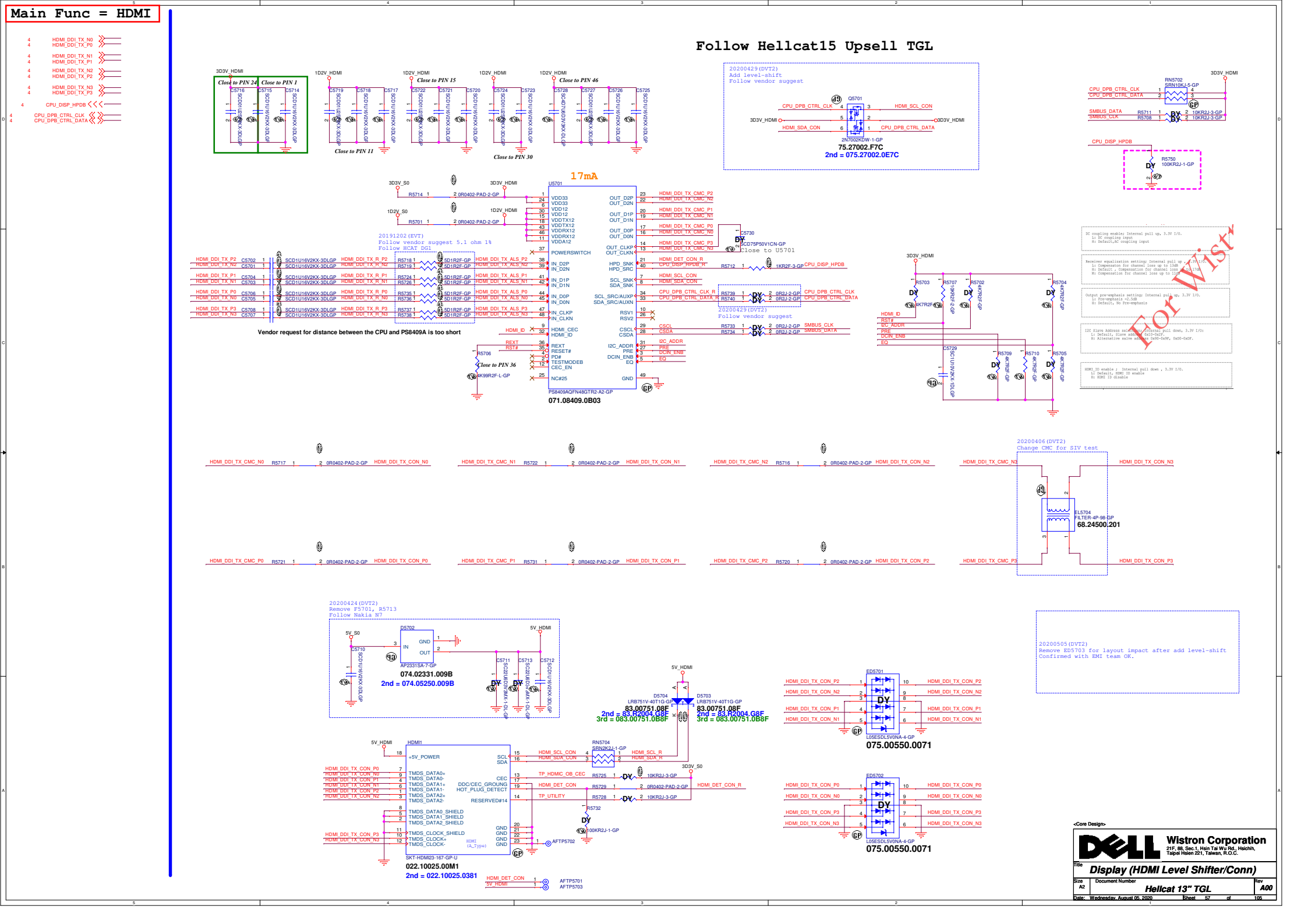
Title: Display (CRT/IR Camera)

Size	Document Number	Rev
A2	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 56 of 105

Main Func = HDMI

Follow Hellcat15 Upsell TGL



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (HDMI Level Shifter/Conn)

Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 57 of 105

<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00

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<Core Design>

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Title: *(Reserved)*		
Size: A3	Document Number: *Hellcat 13" TGL*	Rev: *A00*
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(Blanking)

<Core Design>

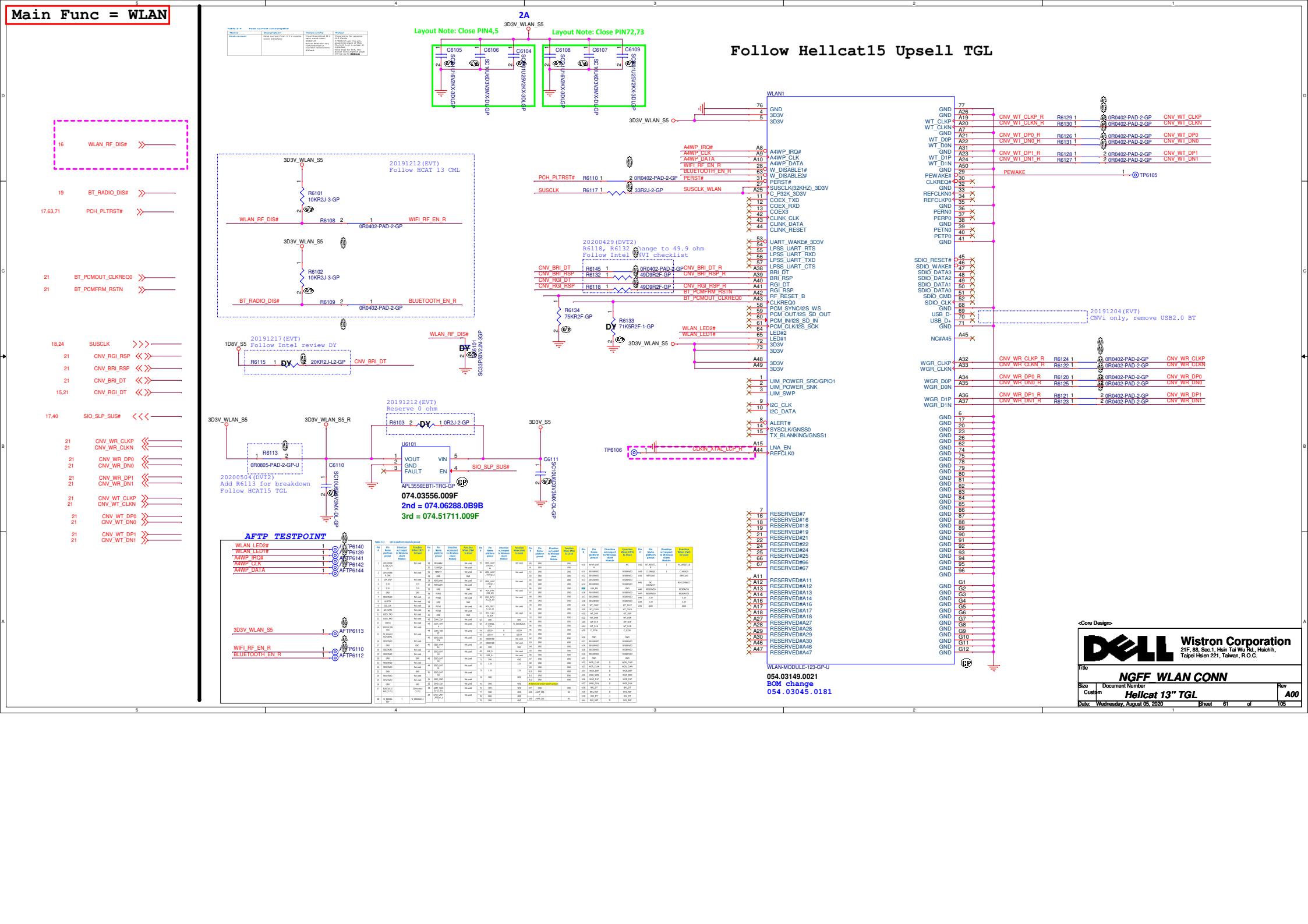
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF HDD/ODD

Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 60 of 105

Main Func = WLAN



(Blanking)

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Title

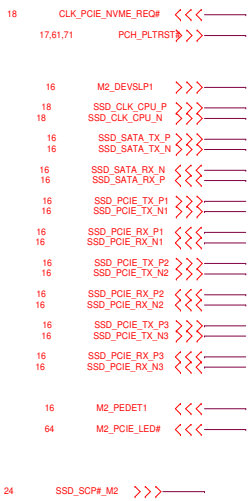
Reserved

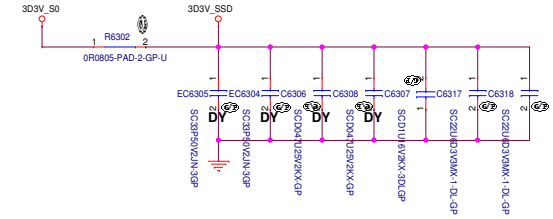
Size	Document Number	Rev
A4	***Hellcat 13" TGL***	***A00***

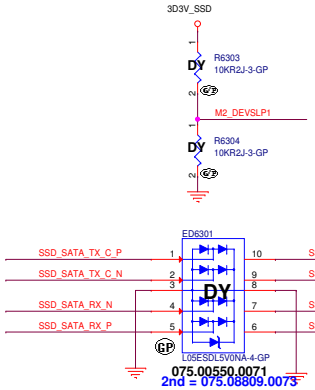
Date: Wednesday, August 05, 2020 Sheet 62 of 105

Main Func = SSD M.2

Follow Hellcat15 Upsell TGL







Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

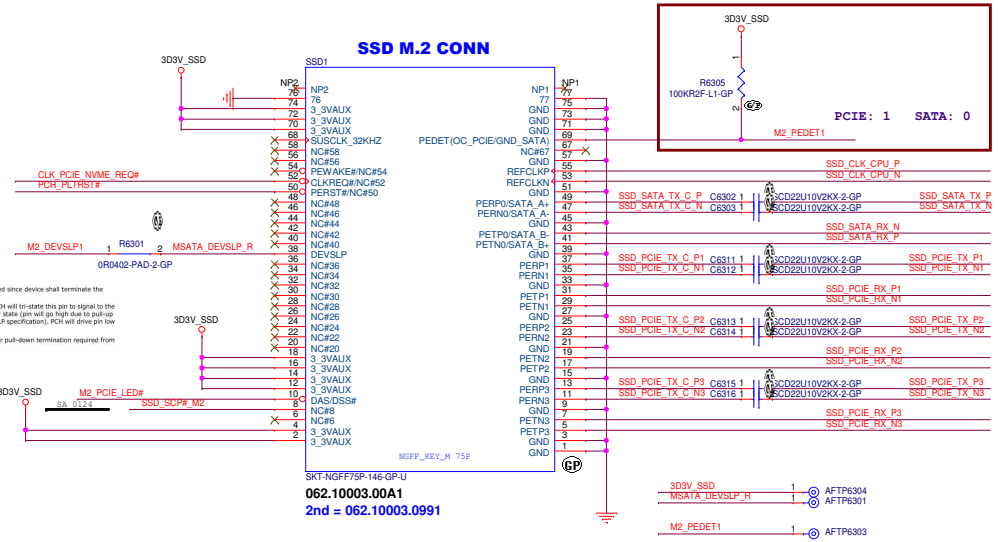


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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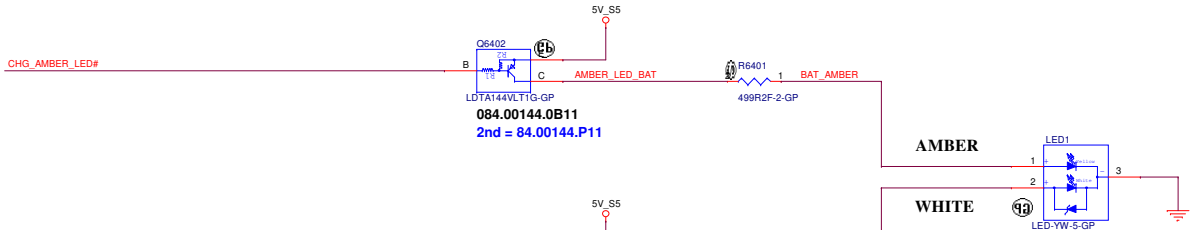
Main Func = Power BTN

Follow Hellcat 13 CML

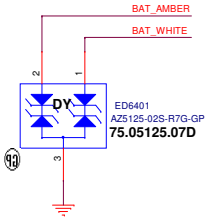
Battery LED1 (AMBER_LED)

Low actived from KBC GPIO



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO



24 CHG_AMBER_LED#
24 BATT_WHITE_LED#

18 SATA_LED#
63 M2_PCIE_LED#

24 MASK_SATA_LED#

17,24 PCH_RSMRST#

24,66,92 KBC_PWRBTN#

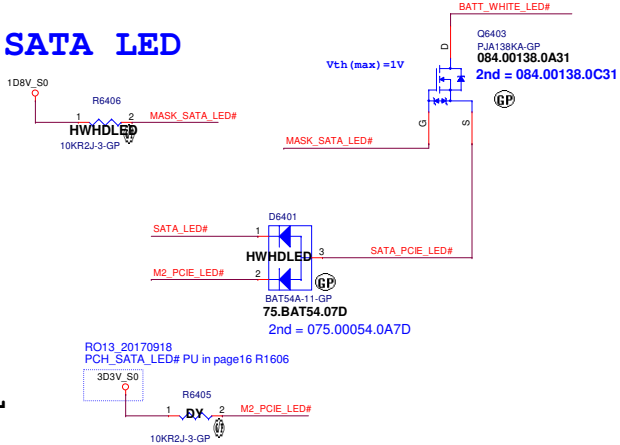
24,44 HW_ACAV_IN

24 M_BIST

check

JEDI 13_20180709

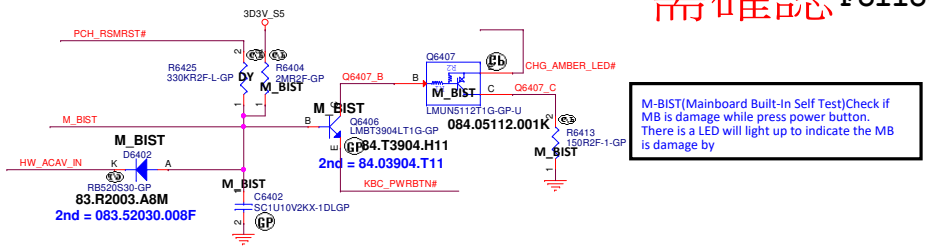
SATA LED



Follow Hellcat 13 CML

M-BIST for G10 (Proposed schematic)

需確認 **Follow Hellcat 13 CML**



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

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Title: **LED / Button / Power Button**

Size: Custom | Document Number: **Hellcat 13" TGL** | Rev: **A00**

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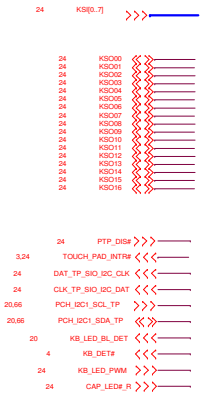
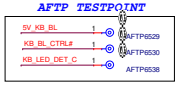
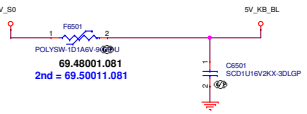
Main Func = Keyboard Follow Hellcat15 Upsell TGL

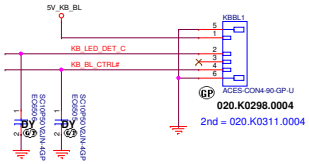


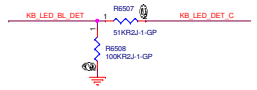
AFTP TESTPOINT

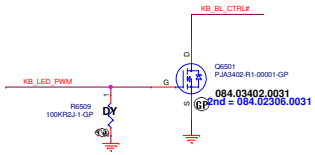


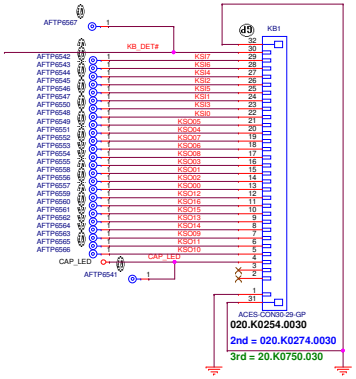
KB Backlight Power Consumption: 285mA max.



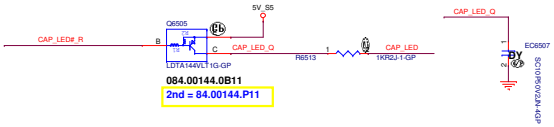




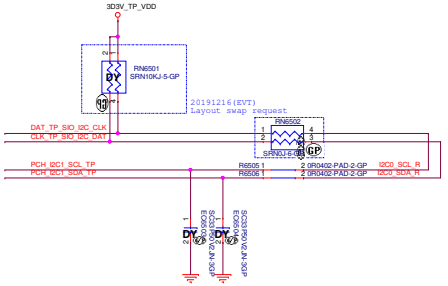


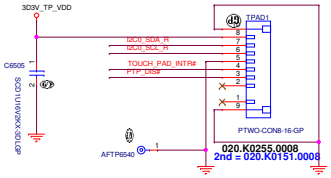


CAP LED Control
LOW actived from KBC GPIO

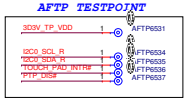


Main Func = TPAD Follow Hellcat15 Upsell TGL

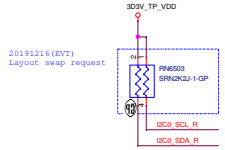


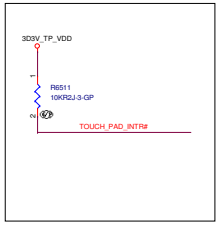


AFTP TESTPOINT



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.





Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

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Title: Key Board&Touch Pad

Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00

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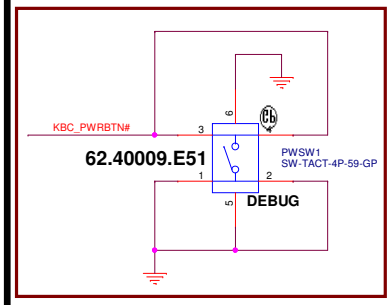
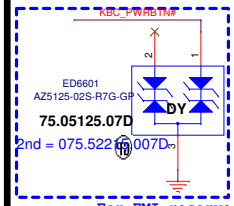
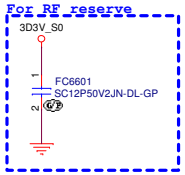
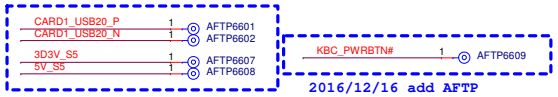
Main Func = IO Connector

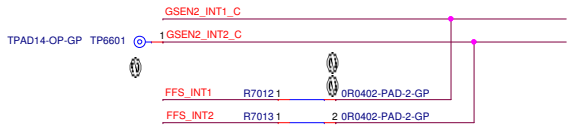
Follow Hellcat 13 CML

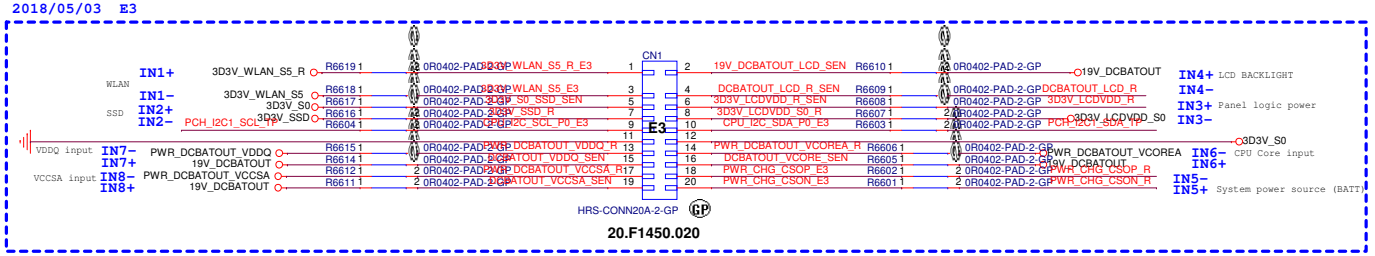


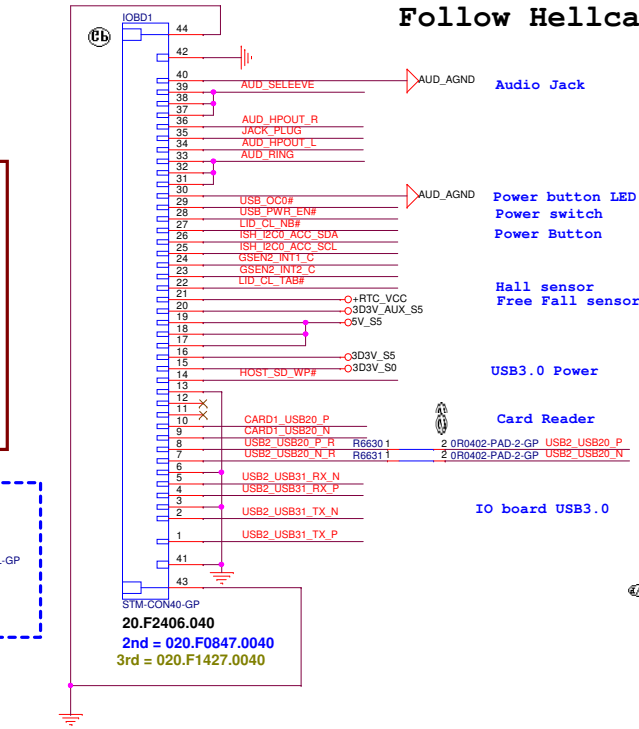


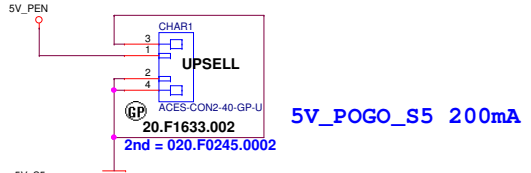


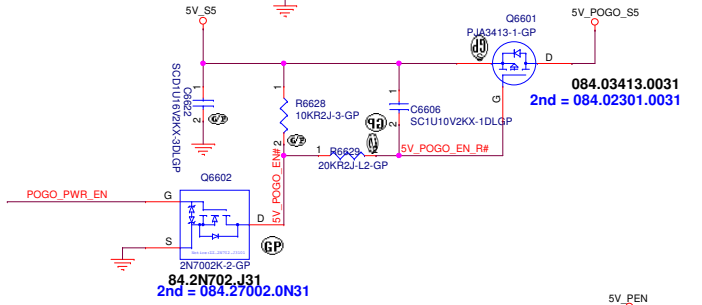












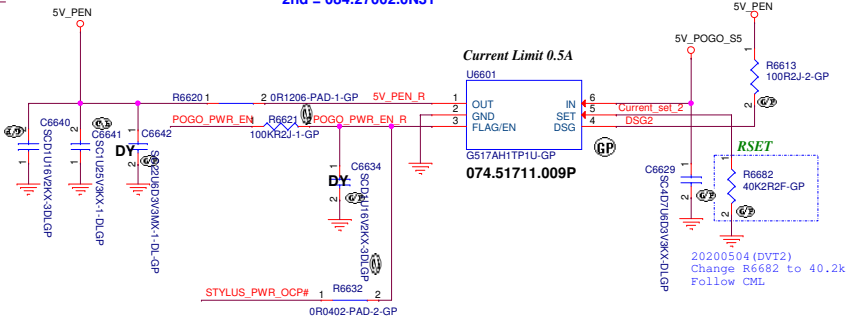


Table 1. Current Limit RSET Value for G517AH

RSET(kΩ)	Current Limit Min (A)	Current Limit Typ (A)	Current Limit Max (A)
7.68	2.43	2.7	2.97
8.25	2.25	2.5	2.75
9.53	1.98	2.2	2.42
10.5	1.8	2	2.2
11.5	1.62	1.8	1.98
14.3	1.35	1.5	1.65
17.4	1.08	1.2	1.32
21	0.9	1	1.1
34.8	0.5	0.6	0.7
42	0.4	0.5	0.6

16 USB2_USB31_TX_N
16 USB2_USB31_TX_P
16 USB2_USB31_RX_N
16 USB2_USB31_RX_P
16 USB2_USB20_N
16 USB2_USB20_P
16 CARD1_USB20_N
16 CARD1_USB20_P
18 HOST_SD_WP#
27,29 AUD_HPOUT_L
27,29 AUD_HPOUT_R
27,29 AUD_SELEEVE
27,29 AUD_RING
27,29 JACK_PLUG
24,64,92 KBC_PWRBTN#
16 USB_OC0#
24 USB_PWR_EN#
20,55 ISH_I2C0_ACC_SDA
20,55 ISH_I2C0_ACC_SCL
20 GSEN2_INT1_C
20 FFS_INT1
19 FFS_INT2
67 LID_CL_TAB#
67 LID_CL_NB#
20,65 PCH_I2C1_SDA_TP
20,65 PCH_I2C1_SCL_TP
55 3D3V_LCDVDD_R
55 DCBATOUT_LCD_R
44 PWR_CHG_CSOP_R
44 PWR_CHG_CSON_R
24 POGO_PWR_EN
21 STYLUS_PWR_OCP#

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Title: IO Board Connector
Size: Custom
Document Number: Hellcat 13" TGL
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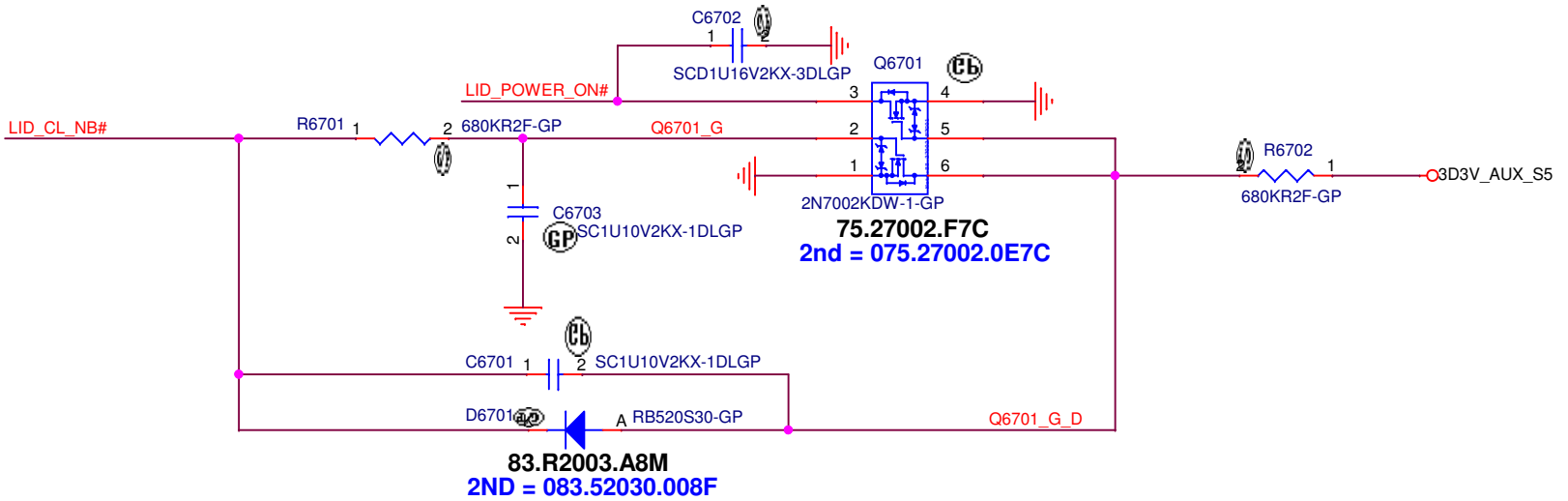
Main Func = HALL SENSOR

Follow Hellcat 13 CML



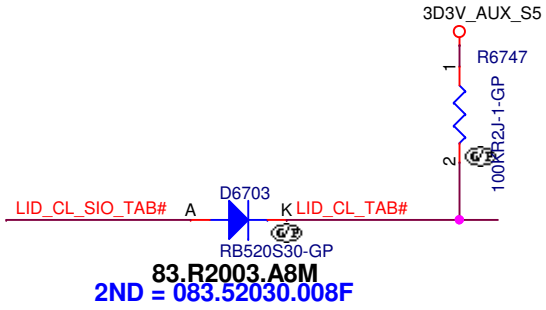
24 LID_POWER_ON#

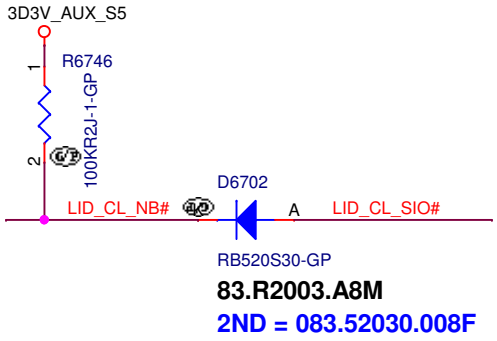
20,24 LID_CL_SIO_TAB#

24,92 LID_CL_SIO#

LID_CL_TAB#

LID_CL_NB#





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Title: Reserved

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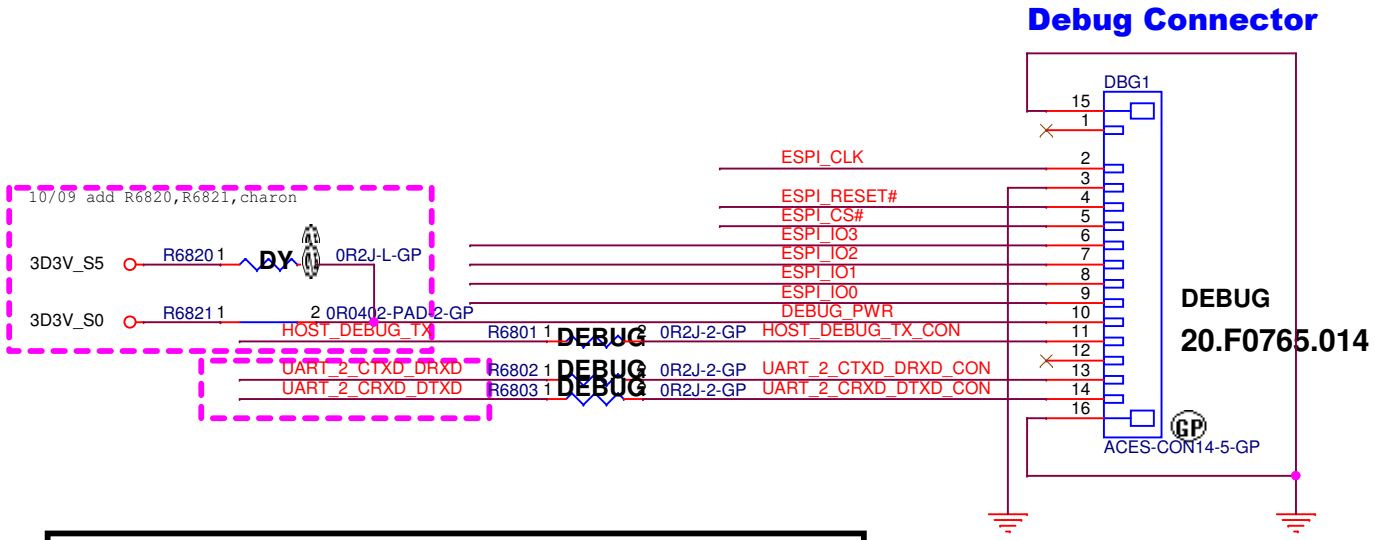
Main Func = Debug

Follow Hellcat15 Upsell TGL

Debug Connector

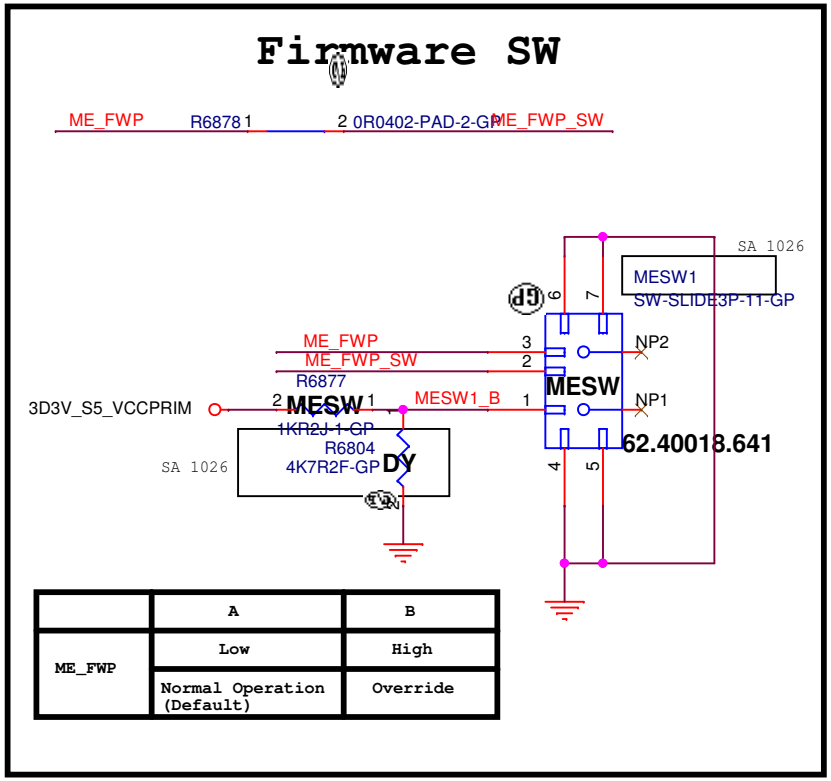


24 HOST_DEBUG_TX
20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

18,24 ESPI_CLK
18,24,40 ESPI_RESET#
18,24 ESPI_CS#
18,24 ESPI_IO0
18,24 ESPI_IO1
18,24 ESPI_IO2
18,24 ESPI_IO3

24 ME_FWP
19 ME_FWP_SW

Firmware SW



ME_FWP	A	B
	Low	High
	Normal Operation (Default)	Override

<Core Design>

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Title: *Dubug connector*

Size	Document Number	Rev
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Main FUNC = GMR

Move to IO Board

<Core Design>

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Title: Reserved

Size	Document Number	Rev
A3	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 69 of 105

Hynix 8G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A2	***Hellcat 13" TGL***	***A00***

Date: Wednesday, August 05, 2020 Sheet 70 of 108

Main Func = TBT

HP team on applying, only murata have sample can meet Intel request
220nF AC cap must be placed on RX lines close to SOC side

HP team on applying , only murata have sample can meet Intel request

Follow Hellcat15 Upsell TGL

	WPN	DPN
TBT	071.00TBT.0F0U	M11GX
NON_TBT	071.00TBT.0D0U	7DYVG

TBT PORTS

Type-C PD

MISC & DEBUG

Power

GND

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

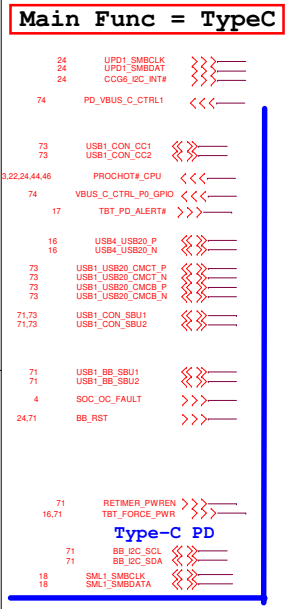
EXT IO (Thunderbolt(1/3)/Type C Re-driver)

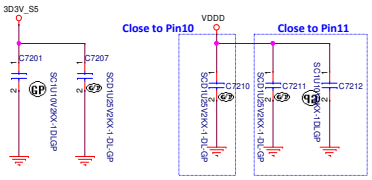
Hellcat 13" TGL

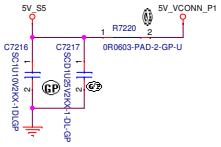
A00

Wednesday, August 05, 2020

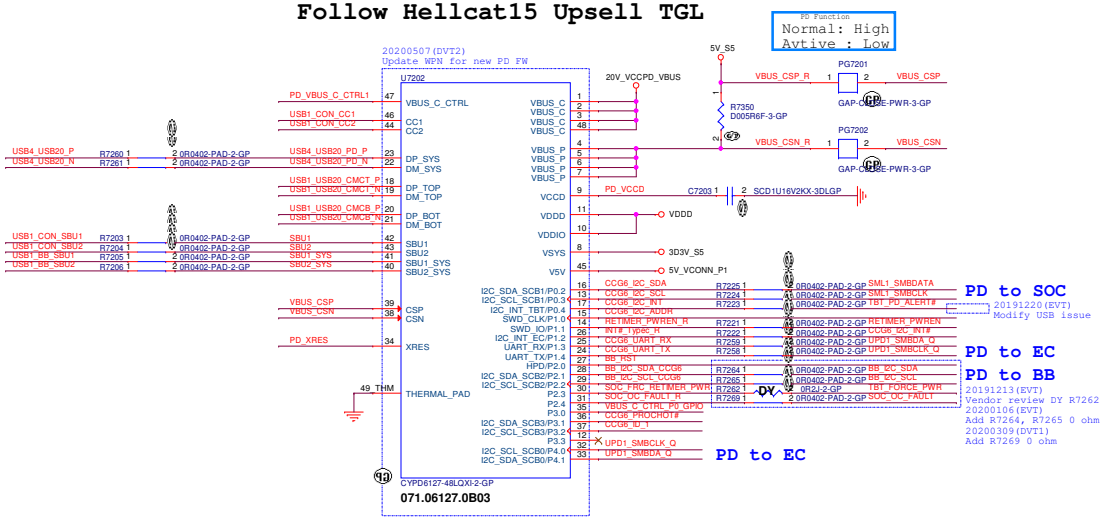
Main Func = TypeC

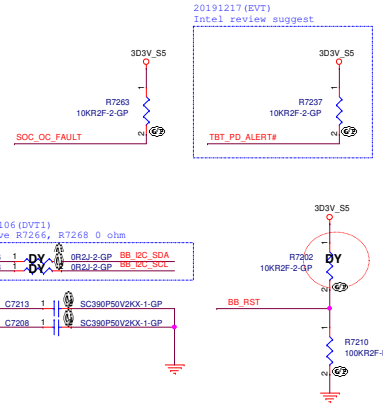


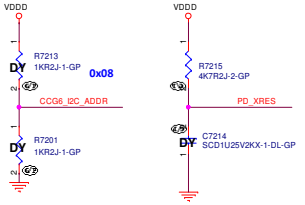


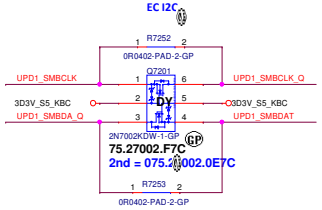


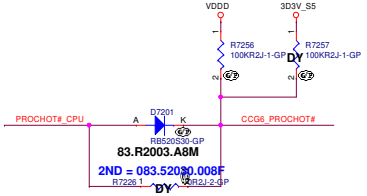
Follow Hellcat15 Upsell TGL



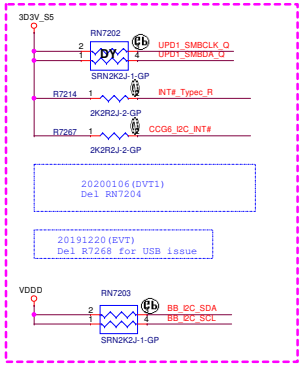


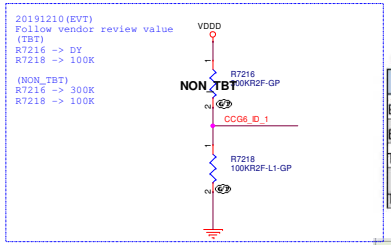


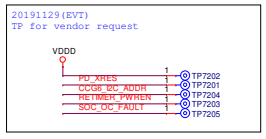




Notes
CCG6DF device's I2C address is determined by SWD_CLK pin.
1K resistors not populated = I2C address 0x08 (default)
1K resistor connected to GND = I2C address 0x40
1K resistor connected to VDDD = I2C address 0x42



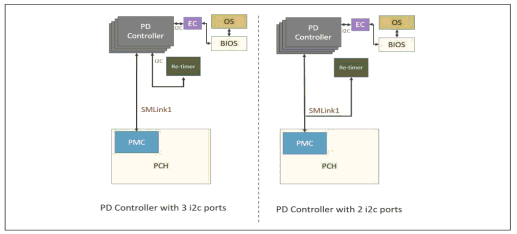




Dell TGL Platform MOD_ID Options			
MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	N/A	TBT Configuration w/BB Retimer
BB8010R	L2	N/A	non-TBT Configuration w/BB Retimer
TUSB546/1046	L6	L0	TUSB546 Equalizer config #1
TUSB546/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

Figure 87. SMBus / SMlink Connectivity for USB Type-C PD Controller



<Core Design>

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Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)

Size	Document Number	Rev
A2	Hellcat 13" TGL	A00

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Main Func = TypeC

USB1

71 USB1_SSTX_CON_P0
71 USB1_SSTX_CON_N0
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N1

71 USB1_SSRX_AR_P0
71 USB1_SSRX_AR_N0
71 USB1_SSRX_AR_P1
71 USB1_SSRX_AR_N1

72 USB1_USB20_CMCT_P
72 USB1_USB20_CMCT_N
72 USB1_USB20_CMCB_P
72 USB1_USB20_CMCB_N

72 USB1_CON_CC1
72 USB1_CON_CC2

71,72 USB1_CON_SBU1
71,72 USB1_CON_SBU2

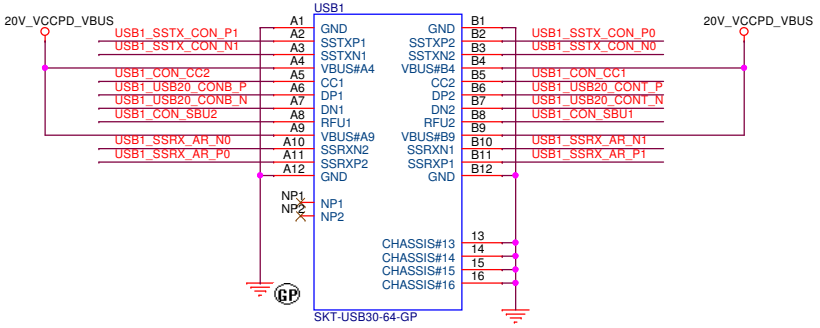
71 USB1_SSTX_RC_N1
71 USB1_SSRX_RC_P1

71 USB1_SSRX_RC_N0
71 USB1_SSTX_RC_N0

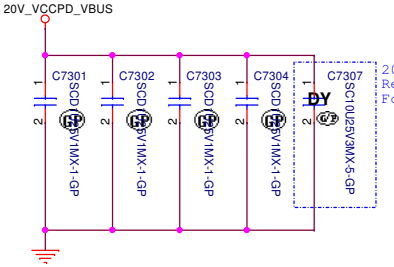
71 USB1_SSRX_RC_P0
71 USB1_SSTX_RC_P0

71 USB1_SSRX_RC_N1
71 USB1_SSTX_RC_P1

Follow Hellcat15 Upsell TGL

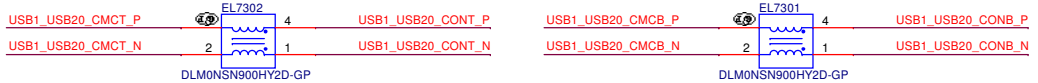


062.10009.M029



20200318(DVT1)
Reserve C7307
Follow Intel TBT check list

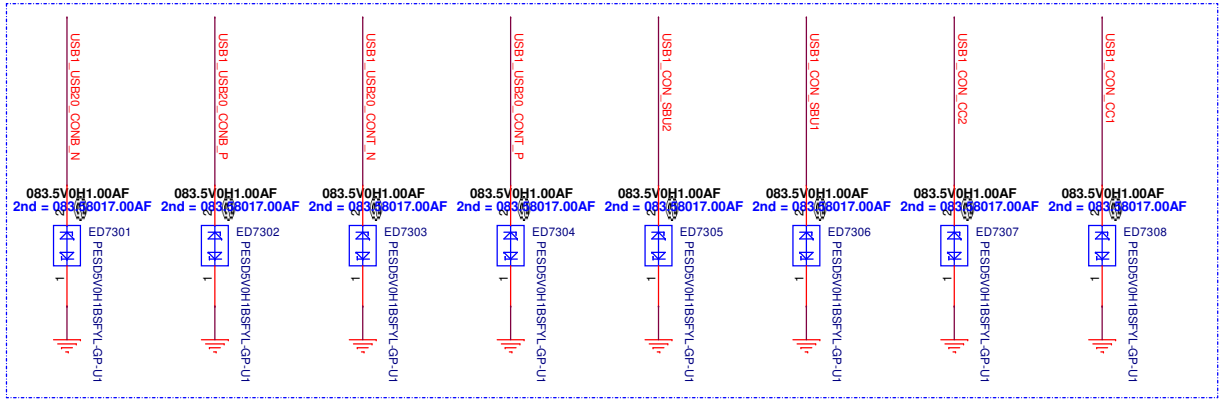
20191216(EVT)
Layout swap request

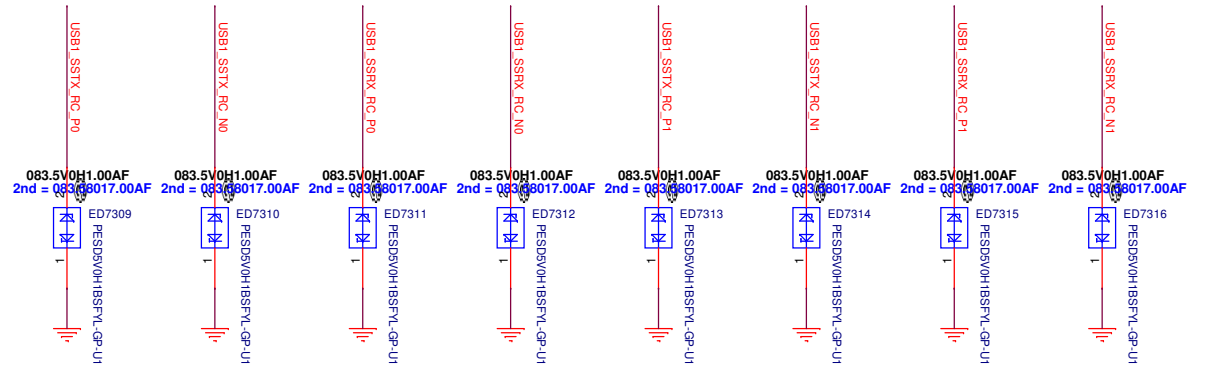


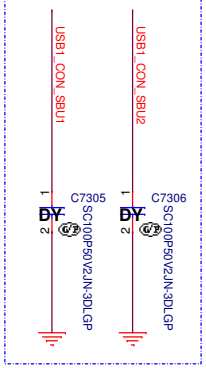
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0011

068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0011

20200508(DVT2)
Change to common part
Follow Hellcat TGL series







20191212(EVT)
Follow Nakia N7
Follow Intel CRB

<Core Design>

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Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size	Document Number	Rev
A3	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 73 of 105

Main FUNC = LPS

72 PD_VBUS_C_CTRL1

44 VCCPD_VBUS_ACK

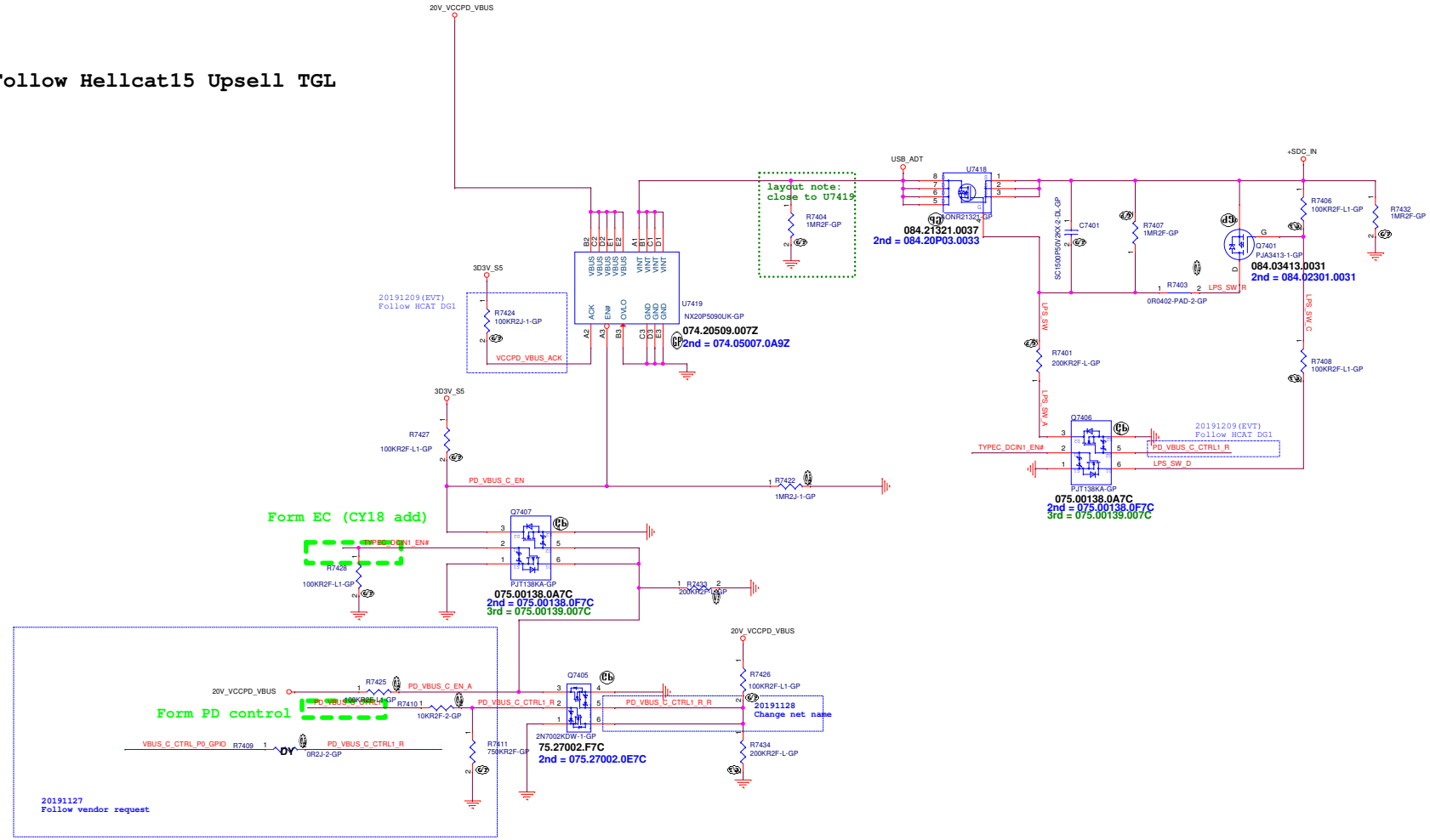
72 VBUS_C_CTRL_P0_GPIO

24 TYPEC_DCIN1_EN#

Default: High
Avtive : Low
RO13 Shauchi

Form PD control

Follow Hellcat15 Upsell TGL



<Core Design>

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Title: GPU(2/5)DIGITALOUT

Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 74 of 105

(Blanking)

<Core Design>

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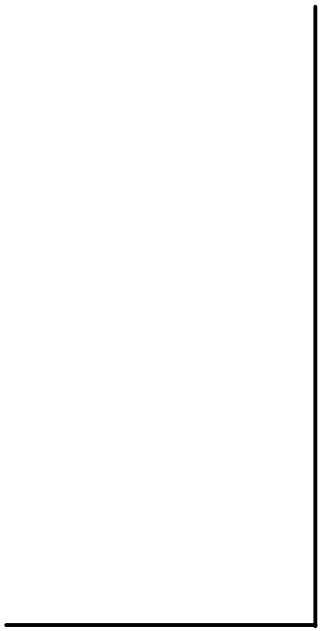
Title

Reserved

Size	Document Number	Rev
A3	***Hellcat 13" TGL***	***A00***

Date: Wednesday, August 05, 2020 Sheet 75 of 105

Main Func = dGPU



<Core Design>

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Title: ***GPU(1/5)PEG***

Size	Document Number	Rev
A3	**Hellcat 13" TGL**	**A00**

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Main Func = dGPU

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GPU2/SDIGITALOUT

Hellcat 13" TGL

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A3	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 79 of 155

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Core Design

DELL

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Title

GPU/2/SDIGITALOUT

Size: A4

Document Number: Helicat 13" TQL

Rev: A00

Date: Monday, February 04, 2008

Sheet 1 of 1

For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

Layout Note:Place as pic..

	LPDDR4		LPDDR4X		
VDDQ	1.1V	410mA	0.6V	185mA	PWR_VDDQ_VTT
VDD1	1.8V	6.8mA	1.8V	12mA	PWR_VDDQ_1D8V
VDD2	1.1V	290mA	1.1V	465mA	1D1V_S3

PWR_VDDQ
PWR_VDDQ_1D8V
PWR_VDDQ

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: Helicat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 81 of 105

For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

Layout Note:Place as pic..

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3.4 (2/4)

Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00

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<Core Design>

Wistron Corporation
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Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	Hellcat 13" TGL	A00

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<Core Design>

Wistron Corporation
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Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	Hellcat 13" TGL	A00

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *POWER (MP2940A_VGA)*

Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 85 of 105

Main Func = dGPU

OFFPAGE

OFFPAGE_GAP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (TPS51487X_VDDQ)

Size	Document Number	Rev
Custom	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 86 of 105

Main Func = VCCSTDG1

OFFPAGE

OFFPAGE_GAP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (1D05V_VCCST_GPU)

Size: A3 | Document Number: Hellcat 13" TGL | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 87 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
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Title: GPU_PWR Sequence

Size	Document Number	Rev
A2	Hellcat 13" TGL	A00

Date: Wednesday, August 05, 2020 Sheet 88 of 105

Main Func = UnusedParts

Follow Hellcat 13 CML

34.4YW18.001

H1 HOLE233R150-GP ZZ.00PAD.WN1
H2 HOLE233R150-GP ZZ.00PAD.WN1
H3 HOLE233R150-GP ZZ.00PAD.WN1
H4 HOLE233R150-GP ZZ.00PAD.WN1
H5 HOLET355B375X375R174-GP ZZ.00PAD.XU1
H12 HOLE256R142-1-GP ZZ.PAD01.V91
H9 HOLE256R142-1-GP ZZ.PAD01.V91

SB 0129 just footprint

HS1 STFT237B158R128H48-1-GP 434.0HH0J.0001

SSID = EMI

Mind the voltage rating of the caps.

19V_DCBATOUT
3D3V_S5
5V_S5
3D3V_S0
5V_S0
+SDC_IN
1D1V_S3
PWR_DCBATOUT_VCOREA
BT+

SSID = RF

19V_DCBATOUT
5V_S5
3D3V_S5
1D05V_S5_BYPASS

20191203(EVT)
Reserve for RF
Follow Nakia_Shuri_N7

VCCIN
1D8V_VCCIN_AUX
20200316(DVT1)
EMI & RF team confirm stuff

Hynix 8G

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Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: Hellcat 13" TGL | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 89 of 106

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Title

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Size	Document Number	Rev
A3	*Hellcat 13" TGL*	*A00*

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Title

INT IO (TPM)

Size	Document Number	Rev
A4	*Hellcat 13" TGL*	*A00*

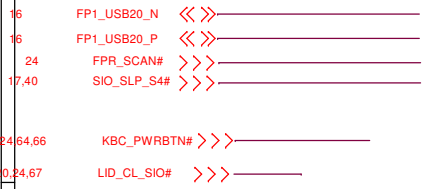
Date: Wednesday, August 05, 2020 Sheet 91 of 105

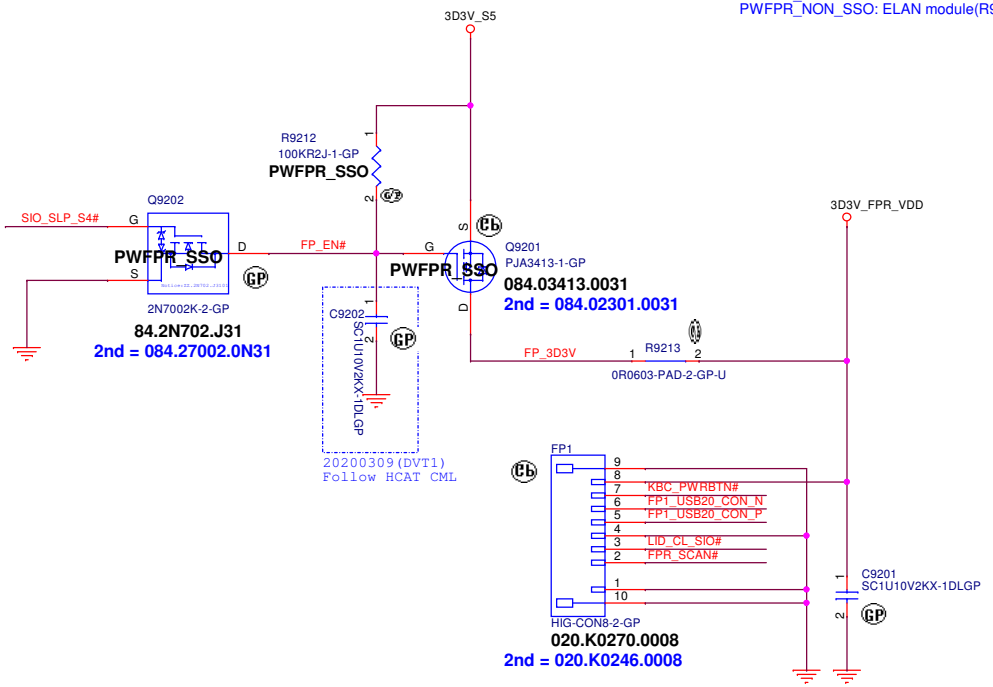
Main Func = FPR

FBR(Botton side finger Print Sensor)

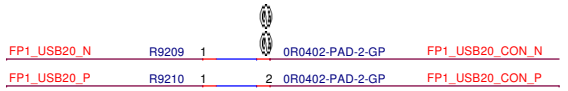
RO13_CFLU
PWFPR_SSO: GOODIX module
PWFPR_NON_SSO: ELAN module(R9211 R9214 R9217)

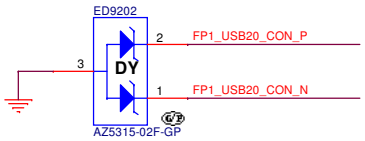
Follow Hellcat 13 CML





	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0





GF5288WN1+GF128A+GM168 Module design

Pin Definition

CN PIN MAP	
PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding
8	GND(ID pin)

Hynix 8G

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Finger Print*

Size: A3 | Document Number: *Hellcat 13" TGL* | Rev: *A00*

Date: Wednesday, August 05, 2020 | Sheet 92 of 106

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A2	*Hellcat 13" TGL*	*A00*

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(Blanking)

<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
A3	*Hellcat 13" TGL*	*A00*

Date: Wednesday, August 05, 2020 Sheet 94 of 105

(Blanking)

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Size	Document Number	Rev
A3	*Hellcat 13" TGL*	*A00*

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A4	***Hellcat 13" TGL***	***A00***

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Title: *LVDS_Switch*

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Main Func = Firmware SW

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Title: CRT_Switch

Size: A3 | Document Number: Hellcat 13" TGL | Rev: A00

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Title: **Debug (XDP/HDT conn)**

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CLK Block Diagram

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Title: CLK Block Diagram		
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Power Sequence

Haitrel 15" TDL

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Title: Power Block Diagram

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Title: SMBUS Block Diagram

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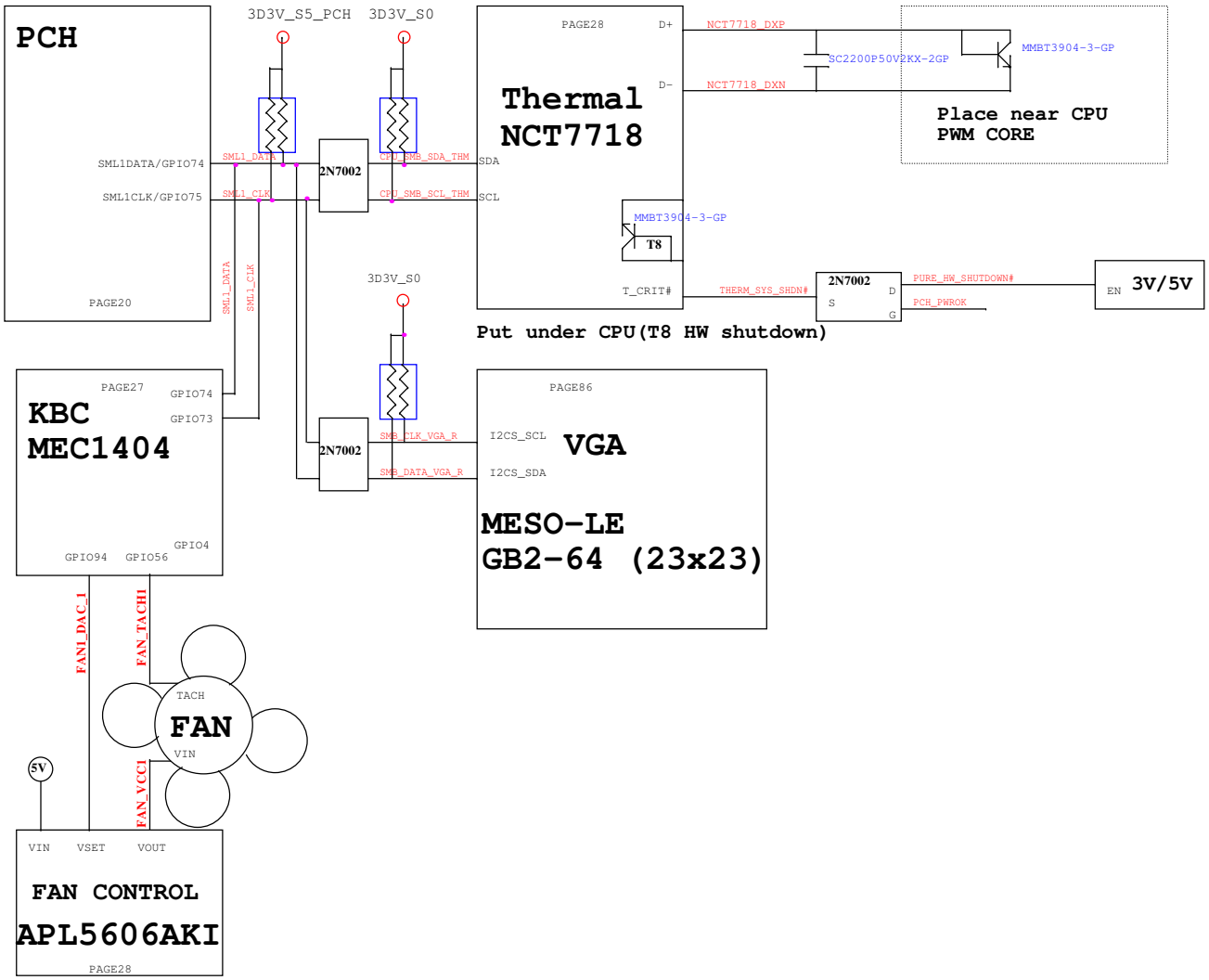
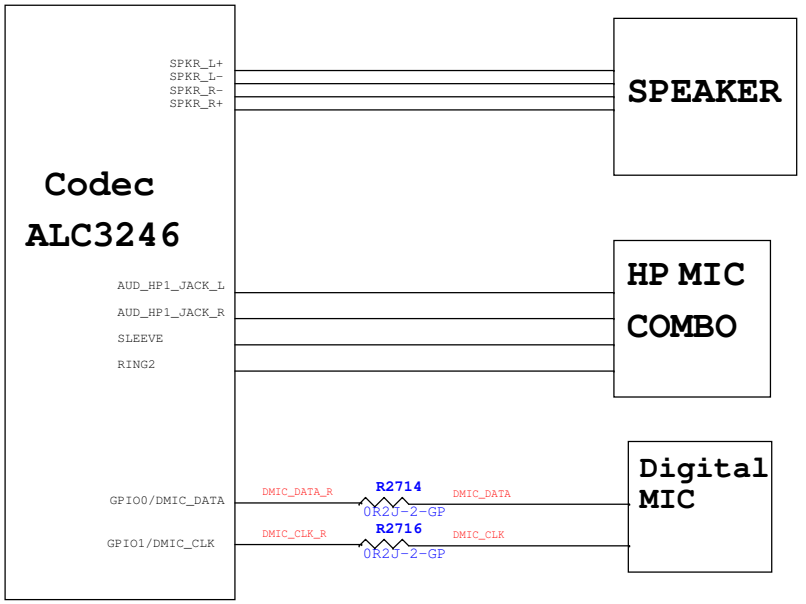
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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