Strongbow_KL
Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

<Core Design>

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Title		
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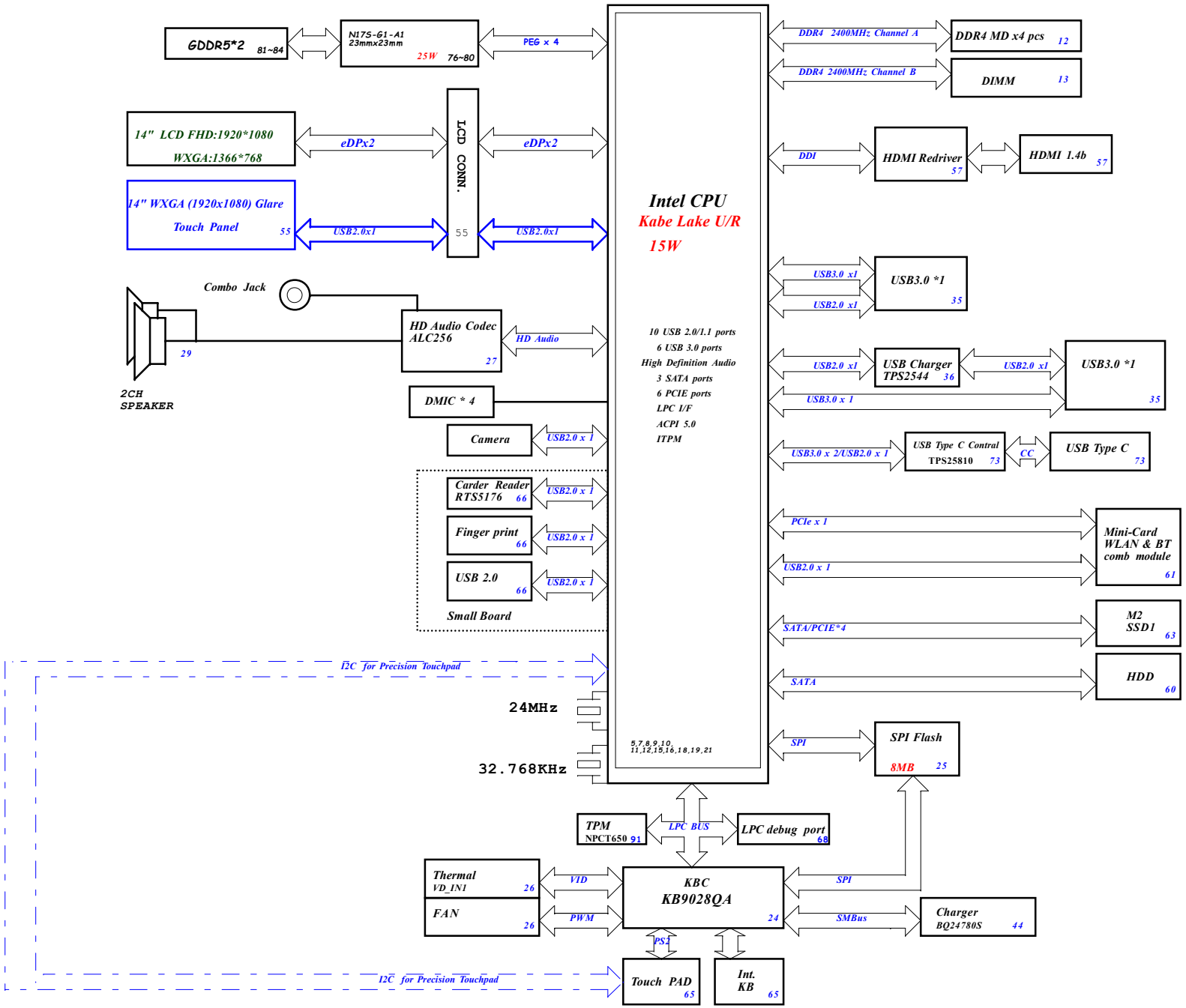
Project Code:4PD0E7010001
PCB No :17863
Revision : 1

Strongbow_KBL Block Diagram



GPU DC/DC RT8813DGQW-GP 85	
INPUTS	OUTPUTS
5V_S0	1V_VGACORE_S0

GPU DC/DC RT8816AGQW-GP 86	
INPUTS	OUTPUTS
5V_S5	1D35V_VGA_S0

GPU DC/DC SY8003ADFC-GP 86	
INPUTS	OUTPUTS
3D3V_S5	1D8V_AON_S0

GPU DC/DC APE8939GN3-GP 86	
INPUTS	OUTPUTS
1D8V_AON_S0	1D8V_VGA_S0

GPU DC/DC APE8939GN3-GP 86	
INPUTS	OUTPUTS
1D0V_S5	1V_1D05V_VGA_S0

CHARGER BQ24780S 44	
INPUTS	OUTPUTS
AD+ BT+	19V_DCBATOUT

SYSTEM DC/DC RT6258CGQUF-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 5V_S5

SYSTEM DC/DC RT6256BGQUF-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_S5

CPU DC/DC RT3602 46-47	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC AOZ5049 48	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VCCGT

CPU DC/DC RT9610B 50	
INPUTS	OUTPUTS
5V_S5	1V_VCCSA

CPU DC/DC G5388K11U-GP 51	
INPUTS	OUTPUTS
5V_S5	PWR_VDDQ

CPU DC/DC APL5930KAI 51	
INPUTS	OUTPUTS
5V_S5	2D5V_S3

SYSTEM DC/DC G5388K11U-GP 52	
INPUTS	OUTPUTS
5V_S5	1D0V_S5

SYSTEM DC/DC G9661-25ADJ 53	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM Load switch TPS22976 40	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
5V_S5	5V_S0
1D0V_S5	1V_VCCST
1D8V_S5	1D8V_S0

SYSTEM Load switch APE8939 40	
INPUTS	OUTPUTS
1D0V_S5	1V_VCCIO

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Title: Block Diagram

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Main Func = CPU

eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1

[55] eDP_AUX_CPU_P
[55] eDP_AUX_CPU_N

[55] eDP_HPD_CPU
[24] eDP_BLEN_CPU
[55] eDP_BLCTRL_CPU
[55] eDP_VDDEN_CPU

HDMI

[57] HDMI_DDI_TX_N2
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P3

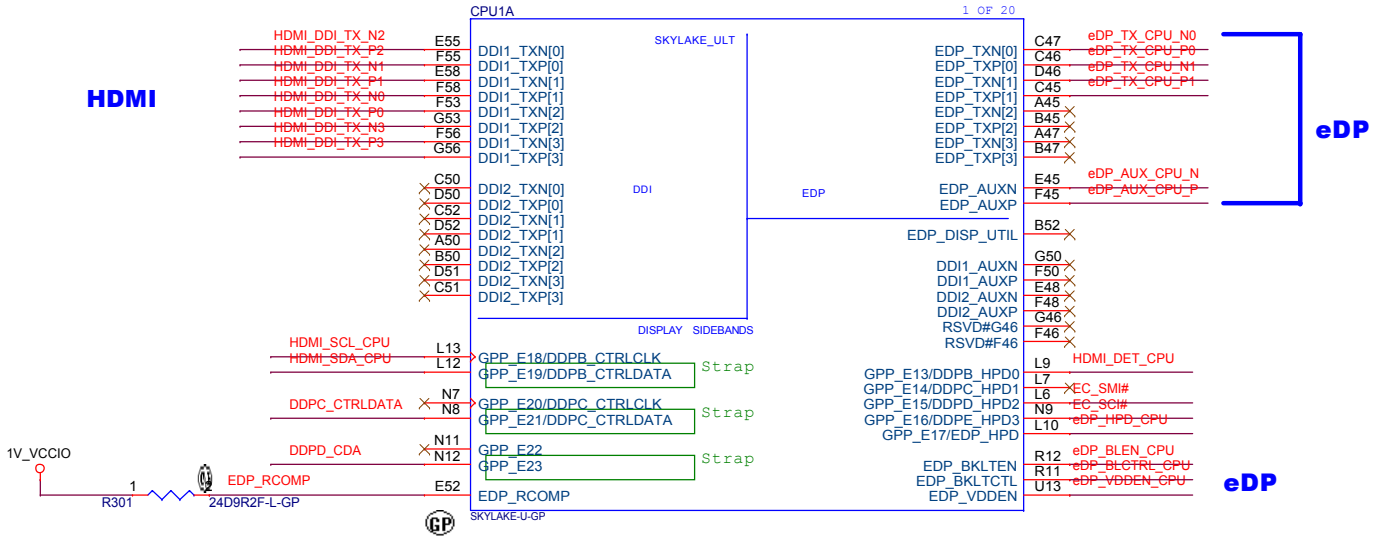
[15,57] HDMI_SCL_CPU
[15,57] HDMI_SDA_CPU

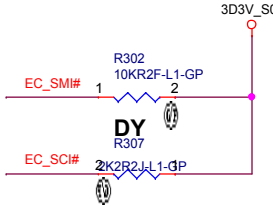
[57] HDMI_DET_CPU

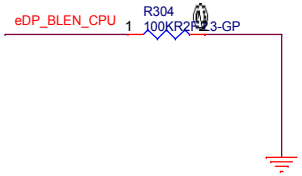
STRAP

[15] DDPC_CTRLDATA
[15] DDPD_CDA

[24] EC_SCI#







(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ± 1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ± 1% Ω resistor

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Title: CPU_(DISPLAY)

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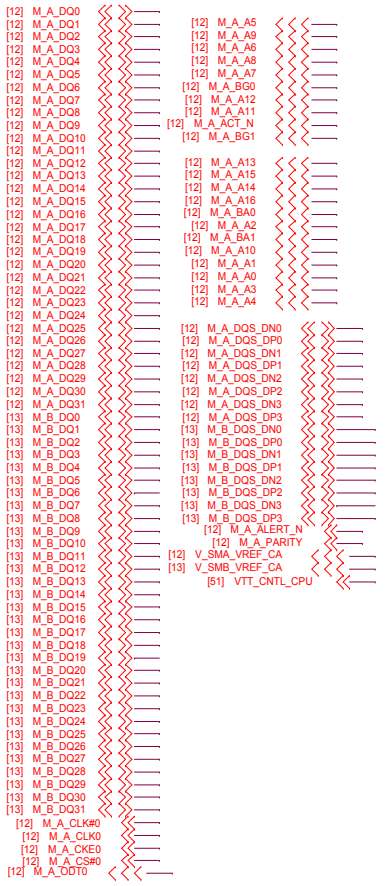
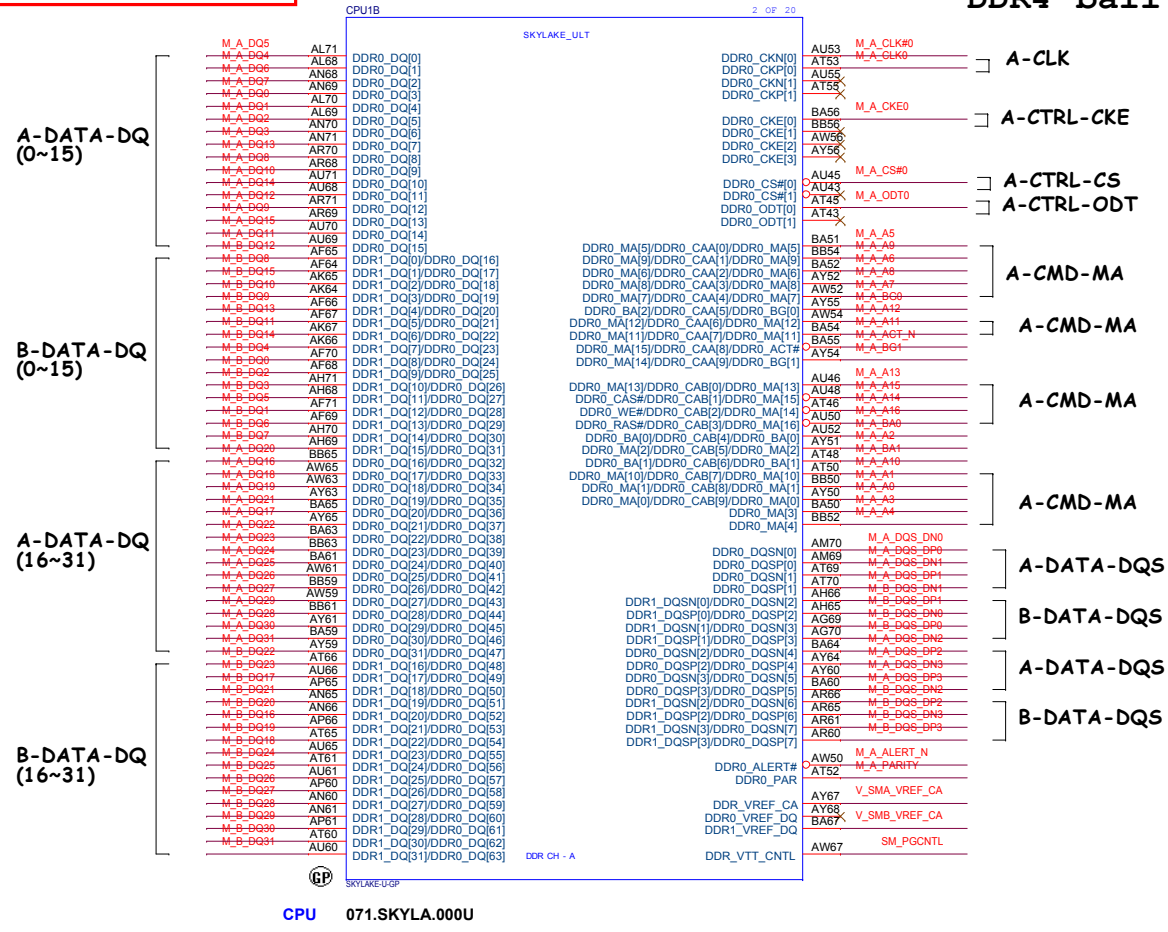
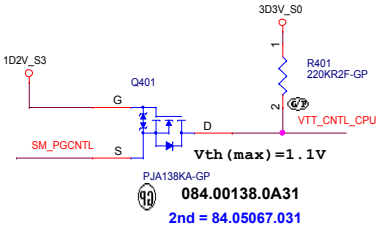
Main Func = CPU

DDR4 ball type:Interleaved Type







CPU 071.SKYLA.000U

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Title: CPU_(DDR)

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Main Func = CPU

DDR4 ball type:Interleaved Type

CPU1C

SKYLAKE_ULT

3 OF 20

A-DATA-DQ (32~47)

B-DATA-DQ (32~47)

A-DATA-DQ (48~63)

B-DATA-DQ (48~63)

B-CLK

B-CTRL-CKE

B-CTRL-CS

B-CTRL-ODT

B-CMD-MA

B-CMD-MA

B-CMD-MA

B-CMD-MA

A-DATA-DQS

B-DATA-DQS

A-DATA-DQS

B-DATA-DQS

SKYLAKE-U-GP

DDR CH - B

071.SKYLA.000U

CPU

#543016

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

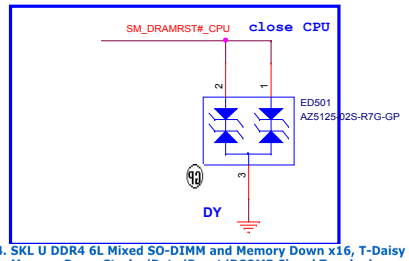
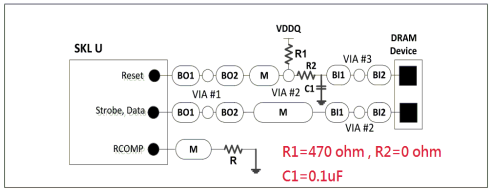
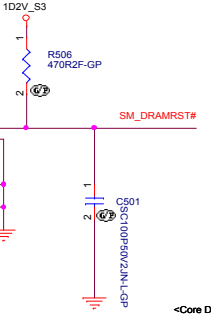


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down Strobe/Data/Reset/RCOMP Signal Topologies





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Title: CPU_(DDR)

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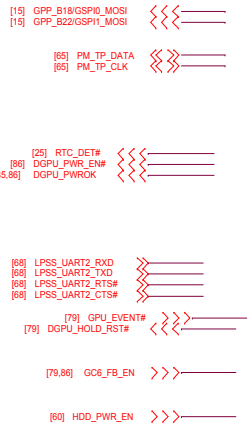
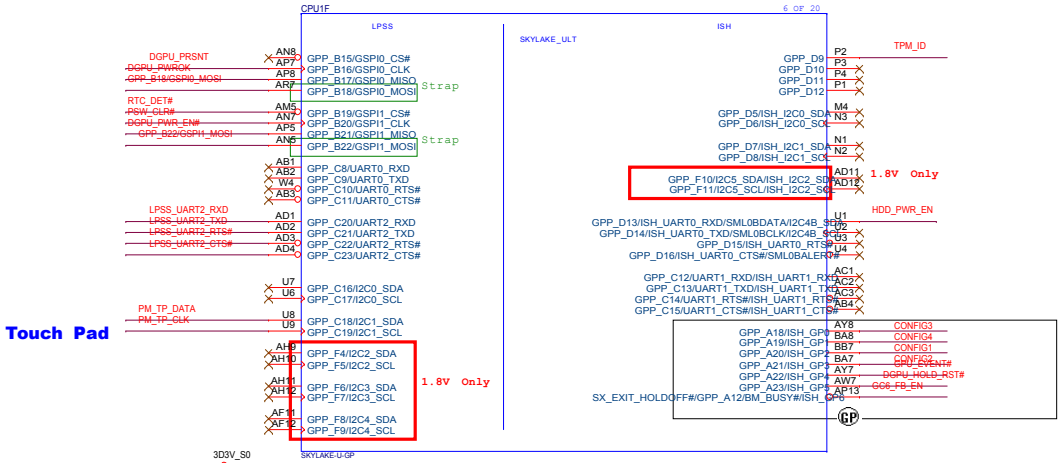
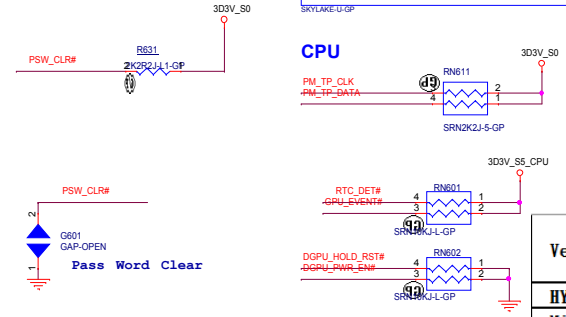
Main Func = PCH

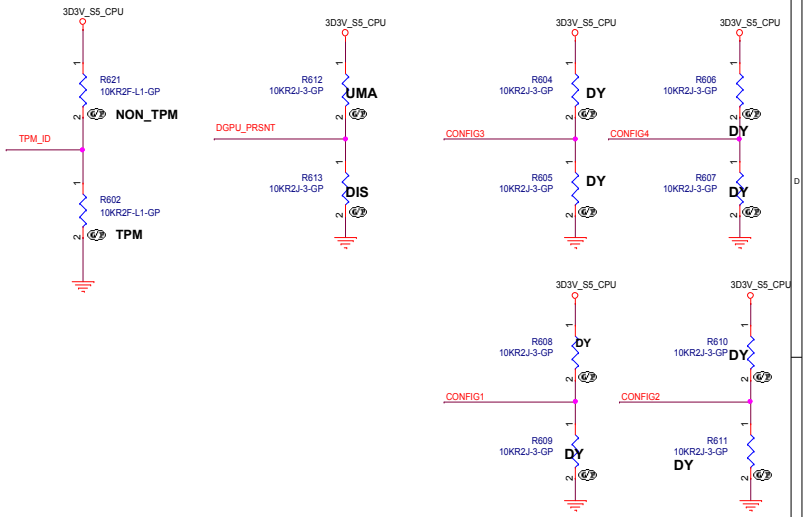




Touch Pad



CPU



Vendor	NFIG4 (GPP_A1	NFIG3 (GPP_A1	NFIG2 (GPP_A2	FIG1 (GPP_A1	Mfr. PN	DDP/SDP	Wistron . P/N	Capacity	Stage
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	SDP	KN.8GB0G.049	8Gb	
Micron	0	0	0	1	MT40A512M16LY-075	SDP	KN.8GB04.027	8Gb	LAB
Micron	0	0	1	0	MT40A1G16KNR-075	DDP	KN.01604.003	16Gb	LAB
HYNIX	0	0	1	1	H5ANAG6NAMR-UHC	DDP	KN.0160G.010	16Gb	

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

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Title: CPU_(LPSS/ISH)

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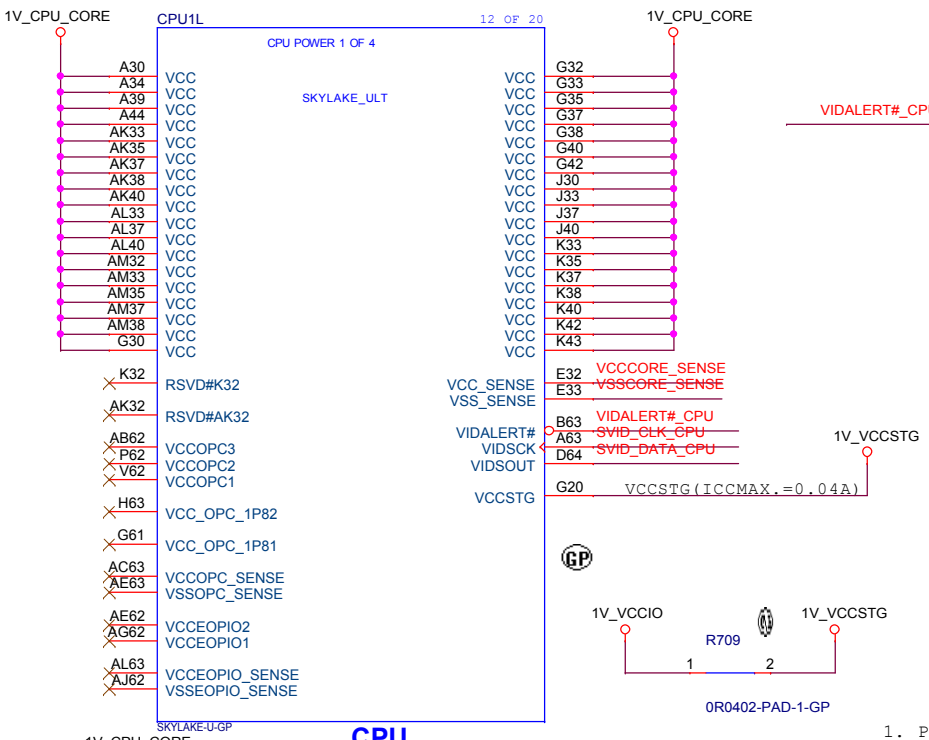
Main Func = CPU

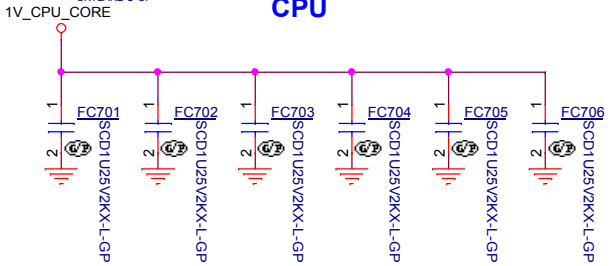
SVID

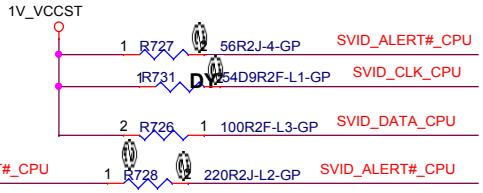
[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU

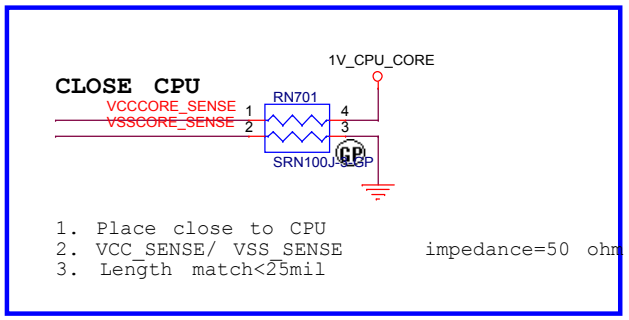
[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE
[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU
[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE



CPU







Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

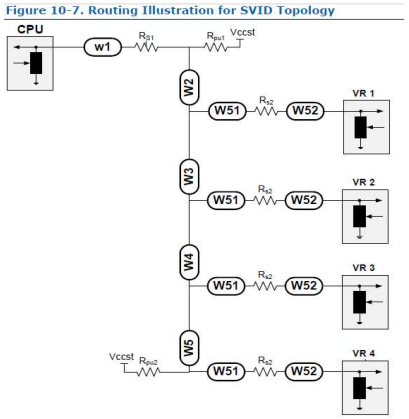


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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Title: CPU_POWER1

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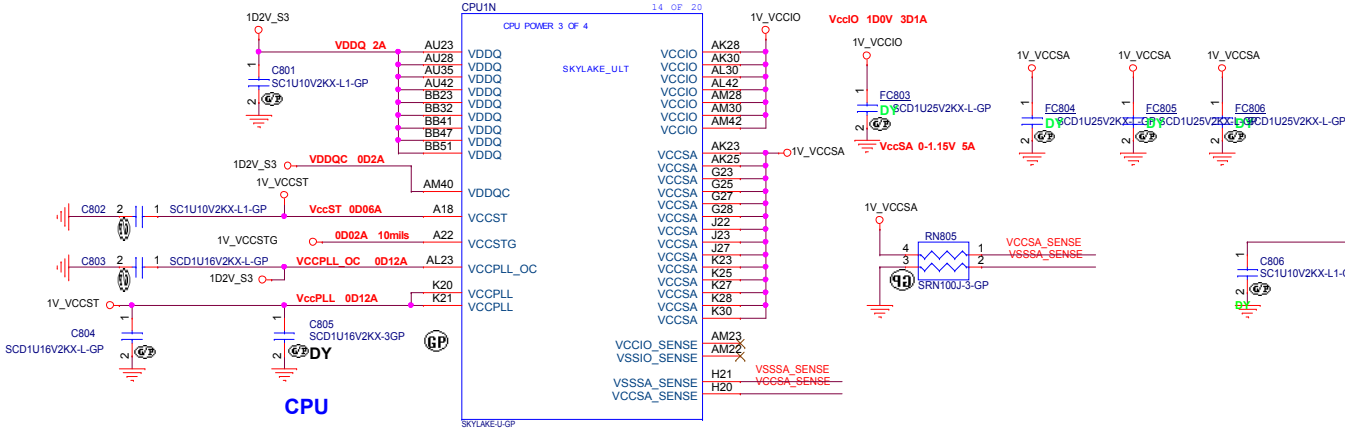
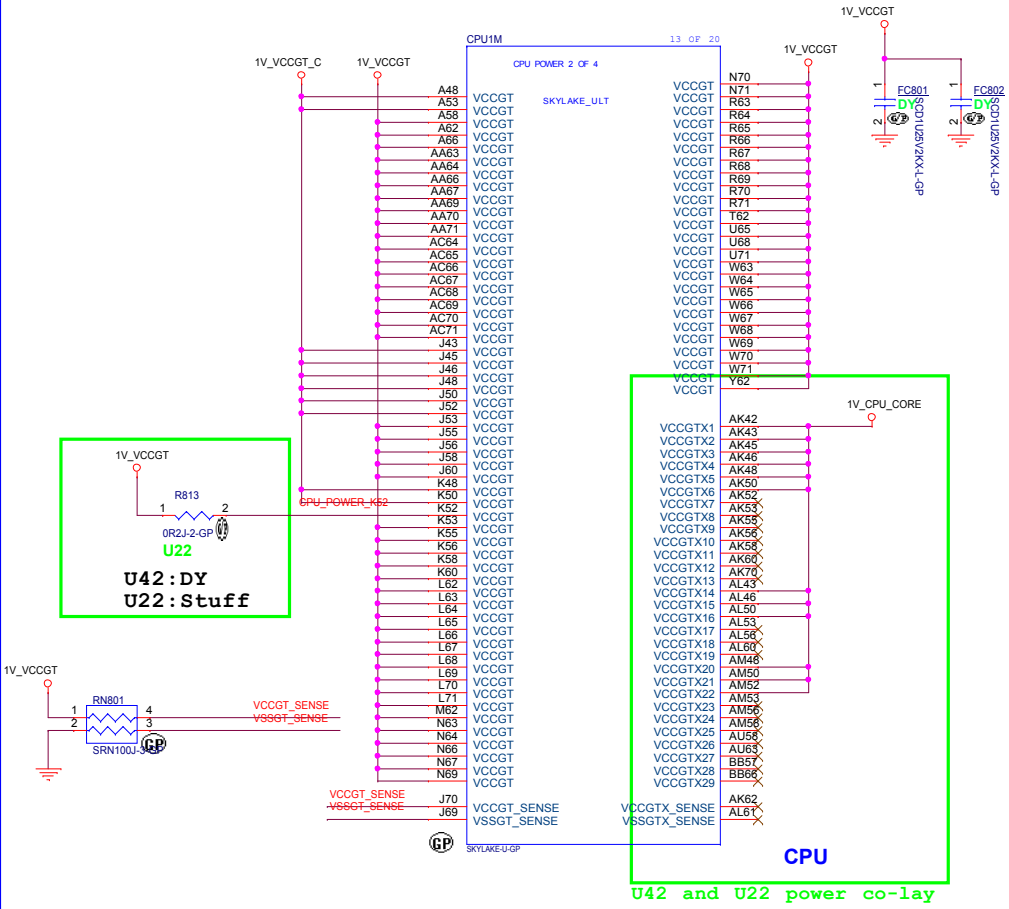
Main Func = CPU

[46] VSSSA_SENSE
[46] VCCSA_SENSE
[46] VCCGT_SENSE
[46] VSSGT_SENSE

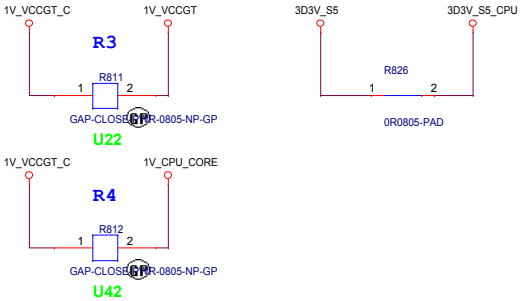


VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 44, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.



KBL U42 Board Compatibility with KBL U22/23e

- 4 Rshunts Required
- R1 – between VCCGTU VR and VCCGTU
- R2 – between VCCGTU and VCCCORE
- R3 – between VCCGT and VCCGT VR
- R4 – between VCCGT and VCCCORE
- Stuff R1 and R3 when U22 or U23e mount on board
- Stuff R2 and R4 and de-pop R1 and R3 when U42 mount on board



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Title: CPU_POWER1

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Blanking

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Title

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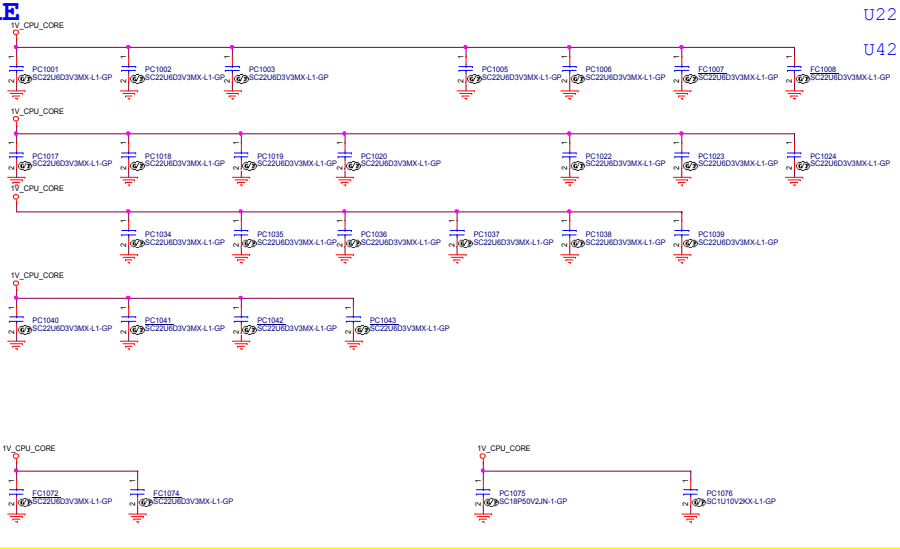
Main Func = CPU

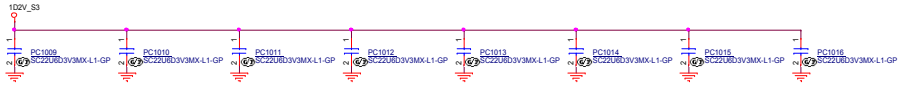
VCORE

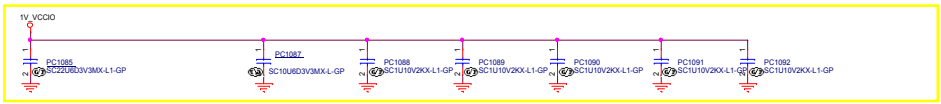


1V_CPU_CORE

U22 0603 22uF *25 , 0603 10uF*1

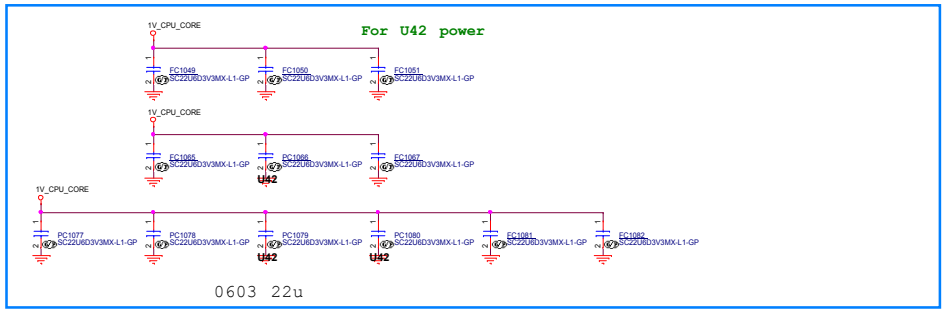
U42 0603 22uF *12





1V_VCCIO

22uF* 1 10uF * 1 1uF *4



Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)		Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

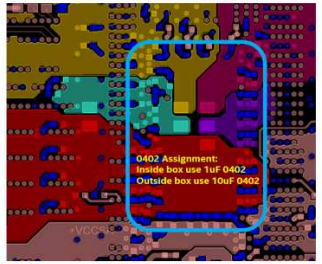
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/Vcc_{GT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1 x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1 x 1 uF 0201	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{GT} closest adjacent layer over any power net other than ground.
Vcc_{GT}		1 x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.



<Core Design>

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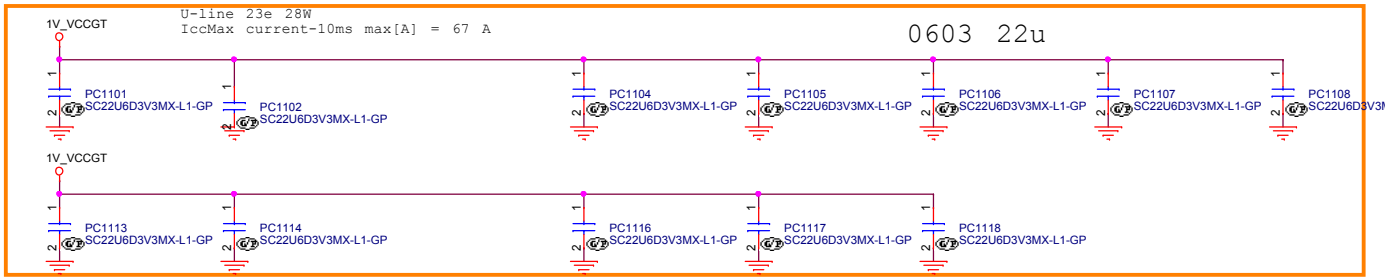
Title: CPU_POWER1

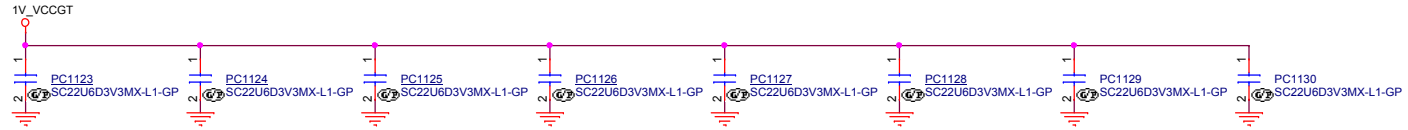
Size: Custom | Document Number: Strongbow_KL | Rev: 1

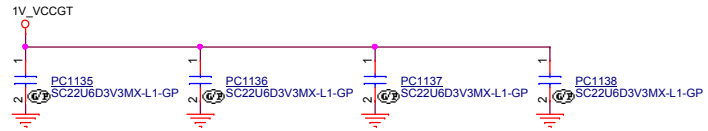
Date: Thursday, January 11, 2018 | Sheet 10 of 106

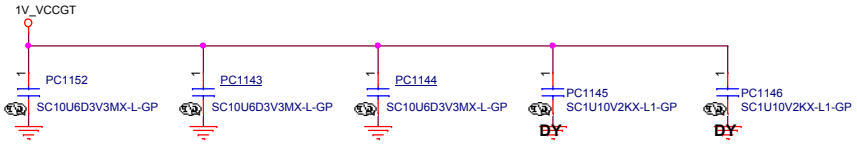
Main Func = CPU

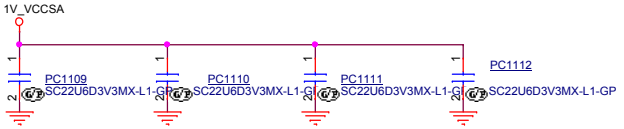
SLICED GT

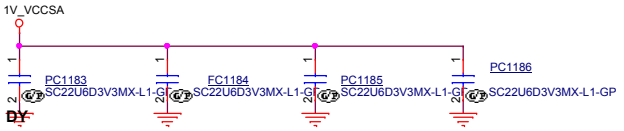


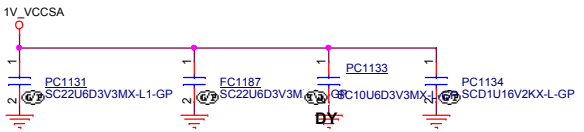


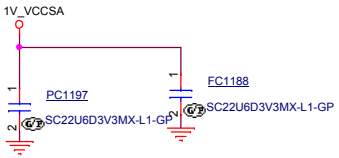




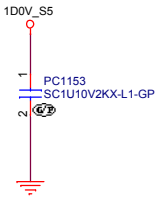




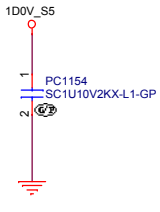




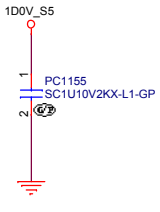
U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF



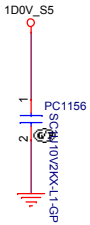
CLOSE CPU AB19



CLOSE CPU AF18



CLOSE CPU K17



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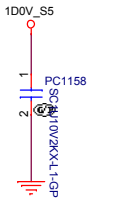

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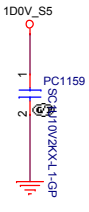

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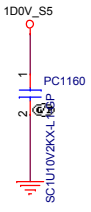

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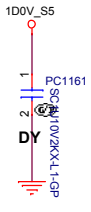

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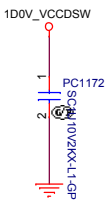
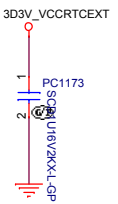


CLOSE CPU AL1



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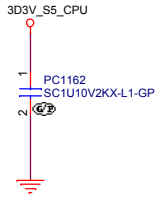

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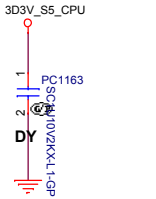

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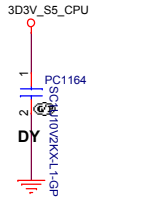

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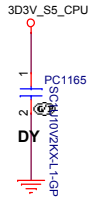

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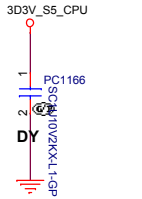
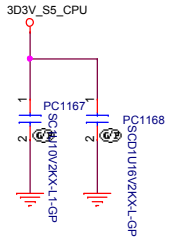
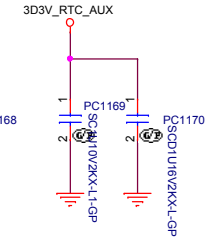


CLOSE CPU T16



CLOSE CPU AK17



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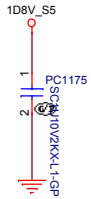

CLOSE CPU AA1

<Core Design>

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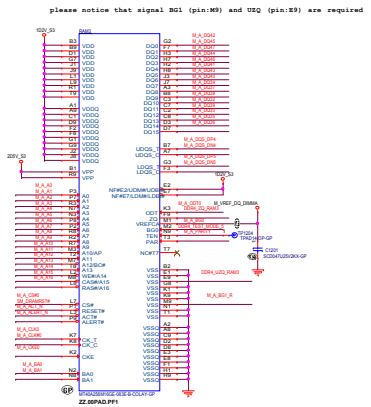
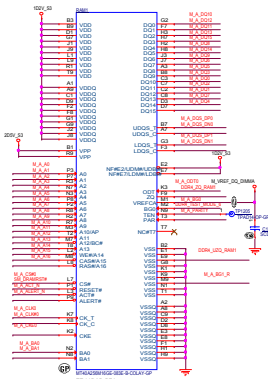
Title	CPU_(Power CAP2)	
Size A3	Document Number Strongbow_KL	Rev 1
Date: Monday, January 15, 2018	Sheet 11 of 106	

SSID = DDR4 CHA

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

please notice that signal BG1 (pin:M9) and UEQ (pin:E9) are required





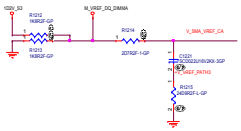
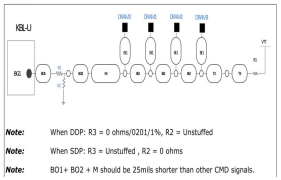


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology

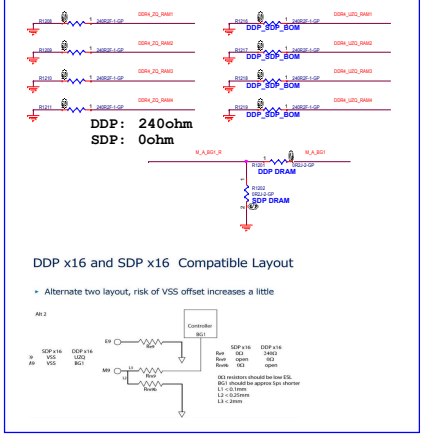


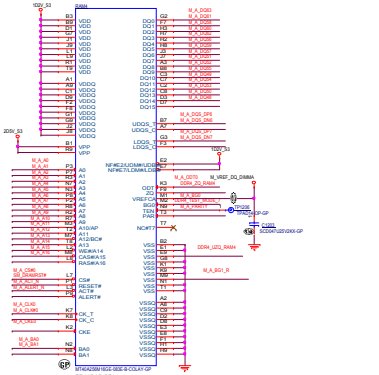
Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed

Note: When SDP: R3 = Unstuffed , R2 = 0 ohms

Note: BO1+ BO2 + M should be 25mils shorter than other CMD signals.

SDP & DDP SETTING





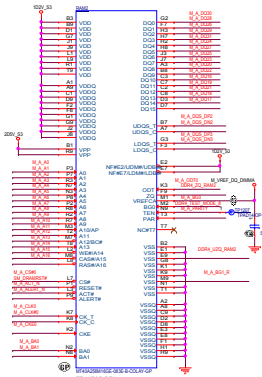
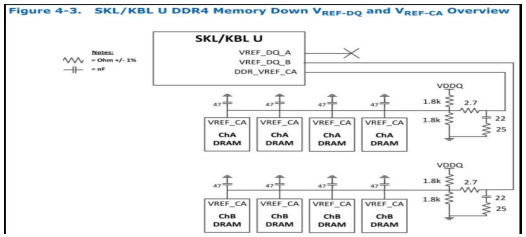
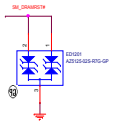


Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



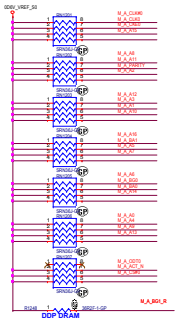


4.14.3 KBL-R DDR4 Memory Down Decoupling

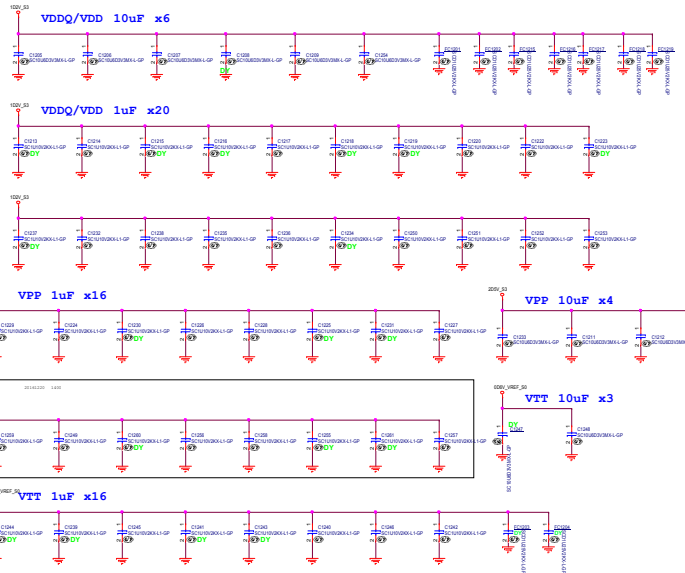
This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	



DDR4 On Board RAM Power Decouple Cap



For ODIMM1,ODIMM2,ODIMM3,ODIMM4

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File: LPDDR3L_CHA

Size: | Document Number: | Rev: 1

Custom: Strongbow_KL

Date: Saturday, January 14, 2017 | Sheet 13 of 105

SSID = DDR4 CHB

Reverse Type

All VREF traces should have width=20mil; spacing=20 mil

Layout Note:

Note:
SO-DIMMB SPD Address is 0xA4

Place these Caps near DIMM2.

DIMM1A 1 OF 4 — DDR4-260P-6-GP

DIMM1C 3 OF 4 — DDR4-260P-6-GP

DIMM1B 2 OF 4 — DDR4-260P-6-GP

DIMM1D 4 OF 4 — DDR4-260P-6-GP

2nd = 062.10011.0C61

3rd = 062.10011.0D21

Thermal EVENT

1D2V_S3 — R1303 240R2F-1-GP — TS#_DIMM1_1 — DY

SPD Address of XMM1

SPD SA1	1
SPD SA0	0

need close to PIN 255

3D3V_S0 — C1306 — C1305 — DY

Layout Note:
Place these caps close to DM2 PIN1

M_VREF_CA_DIMMB — RN1301 SRN1KJ-7-GP — R1305 2R2F-GP — V_SMB_VREF_CA — C1328 SCD022U16V2KX-3GP — +V_VREF_PATH2 — R1306 24D9R2F-L-GP — C1302 SCD1U16V2KX-L-GP

<Core Design>

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Title: LPDDR3L_CHB

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 13 of 106

<Core Design>

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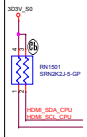
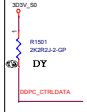
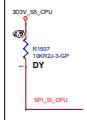
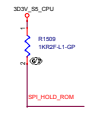
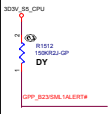
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_POWER3***

Size	Document Number	Rev
Custom	Strongbow_KL	1
Date: Thursday, January 11, 2018	Sheet 14 of 106	

SSID = STRAP

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Name	Internal Pull-up/ Pull-Down (Note 1)	De-Glitch (Note 2) Input	De-Glitch (Note 2) Output	Multiplexed With	Default	NMI or SMI Capable	Note
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts
GPP_B23	20K PD (see note)	Yes	No	SML1ALERT#/ PCHHOT#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio Interface					
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLK	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Driven Low		OFF
HDA_SDI[1:0]	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	Off
SPI0_MOSI	Primary	Internal Pull up/ Pull-down (See Note 1 &2)	Driven Low	Driven Low	Off
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	Off
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	Off
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	Off
SPI1_CLK	Primary	Undriven	Undriven	Undriven	Off
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	Off
SPI1_MISO	Primary	Undriven	Undriven	Undriven	Off
SPI1_CS#	Primary	Undriven	Undriven	Undriven	Off
SPI_IO[2:3]	Primary	Undriven	Undriven	Undriven	Off

Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit 10 — Boot BIOS Destination 0 — SPI 1 — LPC *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A19) as selected in Top Swap Block size soft strap (handled through FITC). *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. 1 = **eSPI** Is selected for EC. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

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Title: (Reserved)_SODIMM_SODIMM4

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Main Func = PCH

GPU

[76] GFX_PCIE_RX_P3
[76] GFX_PCIE_RX_N3
[76] GFX_PCIE_RX_P2
[76] GFX_PCIE_RX_N2
[76] GFX_PCIE_RX_P1
[76] GFX_PCIE_RX_N1
[76] GFX_PCIE_RX_P0
[76] GFX_PCIE_RX_N0
[76] GFX_PCIE_TX_CON_P3
[76] GFX_PCIE_TX_CON_N3
[76] GFX_PCIE_TX_CON_P2
[76] GFX_PCIE_TX_CON_N2
[76] GFX_PCIE_TX_CON_P1
[76] GFX_PCIE_TX_CON_N1
[76] GFX_PCIE_TX_CON_P0
[76] GFX_PCIE_TX_CON_N0

M.2 PCIE SSD1

[63] SSD1_PCIE_RX_N3
[63] SSD1_PCIE_RX_P3
[63] SSD1_PCIE_TX_N3
[63] SSD1_PCIE_TX_P3
[63] SSD1_PCIE_RX_N2
[63] SSD1_PCIE_RX_P2
[63] SSD1_PCIE_TX_N2
[63] SSD1_PCIE_TX_P2
[63] SSD1_PCIE_RX_N1
[63] SSD1_PCIE_RX_P1
[63] SSD1_PCIE_TX_N1
[63] SSD1_PCIE_TX_P1
[63] SSD1_PCIE_RX_N0
[63] SSD1_PCIE_RX_P0
[63] SSD1_PCIE_TX_N0
[63] SSD1_PCIE_TX_P0

HDD

[60] HDD_SATA_TX_P
[60] HDD_SATA_TX_N
[60] HDD_SATA_RX_P
[60] HDD_SATA_RX_N

WLAN

[61,89] WLAN_PCIE_RX_N
[61,89] WLAN_PCIE_RX_P
[61,89] WLAN_PCIE_TX_N
[61,89] WLAN_PCIE_TX_P

USB3 port1

[35] USB1_USB30_RX_N
[35] USB1_USB30_RX_P
[35] USB1_USB30_TX_N
[35] USB1_USB30_TX_P
[36] USB1_USB20_N
[36] USB1_USB20_P

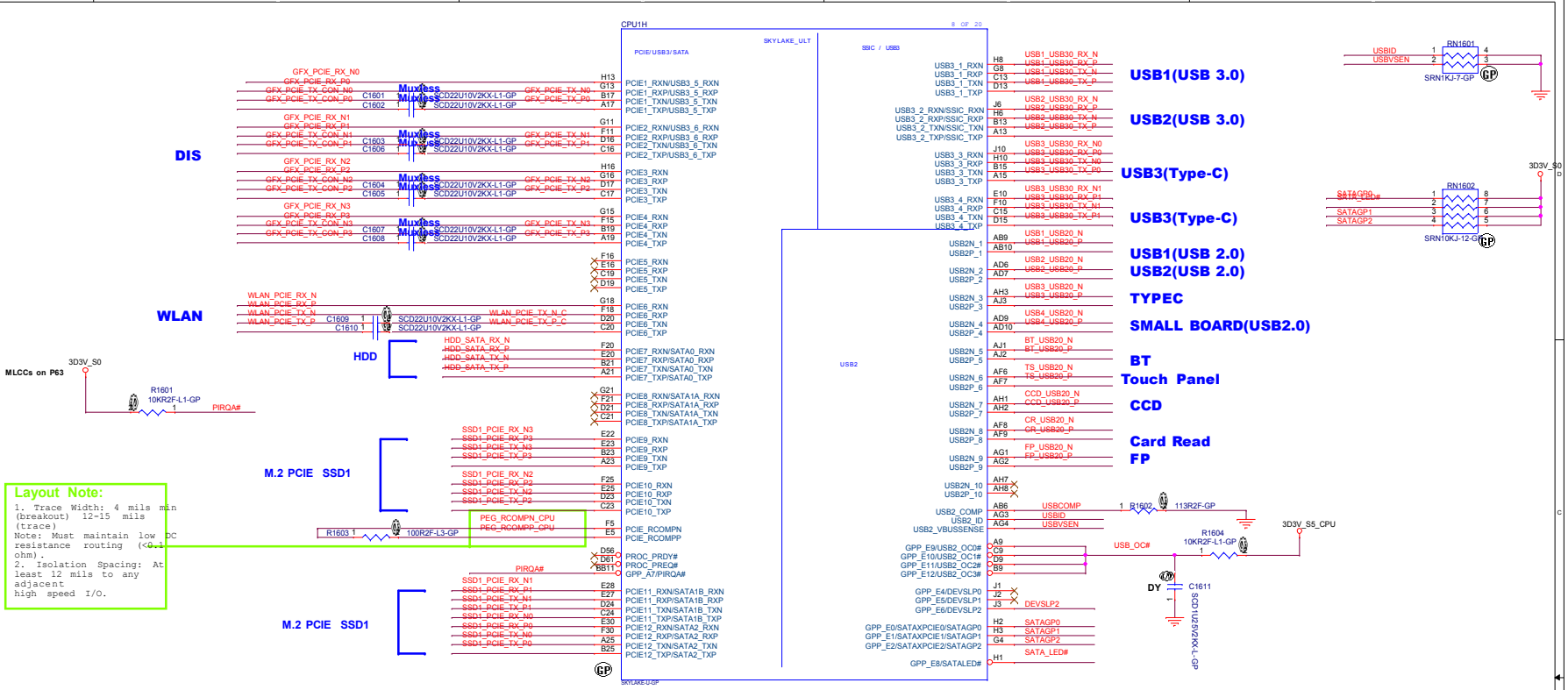
USB3 port2

[35] USB2_USB30_RX_N
[35] USB2_USB30_RX_P
[35] USB2_USB30_TX_N
[35] USB2_USB30_TX_P
[35] USB2_USB20_N
[35] USB2_USB20_P

TYPE-C

[73] USB3_USB30_RX_N0
[73] USB3_USB30_RX_P0
[73] USB3_USB30_TX_N0
[73] USB3_USB30_TX_P0
[73] USB3_USB30_RX_N1
[73] USB3_USB30_RX_P1
[73] USB3_USB30_TX_N1
[73] USB3_USB30_TX_P1
[73] USB3_USB20_N
[73] USB3_USB20_P

[55] TS_USB20_N
[55] TS_USB20_P
[66,89] USB4_USB20_N
[66,89] USB4_USB20_P
[66,89] CR_USB20_N
[66,89] CR_USB20_P
[61,89] BT_USB20_N
[61,89] BT_USB20_P
[55] CCD_USB20_N
[55] CCD_USB20_P
[66,89] FP_USB20_N
[66,89] FP_USB20_P
[63] SSD1_PEDET
[63] DEVSLP2



Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

071.SKYLA.000U

CPU

Table 27. Socket 2 Module Configuration

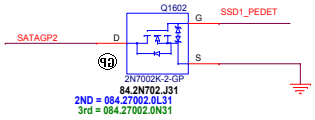
State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

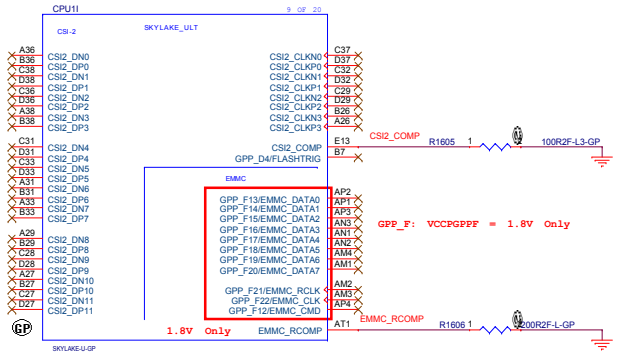
	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

M.2 auto detection



	KBL Premium U		Acer 2015		2017 R15(Premium)		2017 R15(base)
Lane1	USB3 Port1		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane2	USB3 Port2		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane3	USB3 Port3		USB 3 (I/O)		USB 3 Type-C (I/O)		USB 3 Type-C (I/O)
Lane4	USB3 Port4						
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU		dGPU		dGPU
Lane6	USB3 Port6 (Premium)	PCIe Port2					
Lane7		PCIe Port3					
Lane8		PCIe Port4					
Lane9		PCIe Port5	LAN				
Lane10		PCIe Port6	WIFI		WIFI		WIFI
Lane11	SATA0 (Base/Premium)	PCIe Port7 (Premium)	HDD		HDD		HDD
Lane12	SATA1 (Base/Premium)	PCIe Port8 (Premium)	ODD				
Lane13		PCIe Port9					
Lane14		PCIe Port10	NA	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal		M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal
Lane15	SATA1 (Premium)	PCIe Port11					
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x1)		M.2 SSD SATA		
	USB2 Port1		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port2		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port3		USB 3 (I/O)		USB 2 Type-C (I/O)		USB 2 Type-C (I/O)
	USB2 Port4		USB 2 (I/O) / SensorHub		USB 2 (I/O)		USB 2 (I/O)
	USB2 Port5		BT		BT		BT
	USB2 Port6		TS		TS		TS
	USB2 Port7		CCD		CCD		CCD
	USB2 Port8		CR (USB) / FP		CR		CR
	USB2 Port9		CR		FP		FP
	USB2 Port10						



CPU

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Title: CPU_(PCIE/SATA/USB)

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Main Func = PCH

DIS

[76] PEG_CLK_CPU_P
[76] PEG_CLK_CPU_N
[76] PEG_CLKREQ_CPU#

WLAN

[61,89] WLAN_CLK_CPU_N
[61,89] WLAN_CLK_CPU_P
[61,89] WLAN_CLKREQ_CPU#

NGFF1

[63] SSD1_CLK_CPU_N
[63] SSD1_CLK_CPU_P
[63] SSD1_CLKREQ_CPU_N

KBC

[24] RTCRST_ON

CPU1J — 10 OF 20 — CLOCK SIGNALS — SKYLAKE_ULT — SKYLAKE-U-GP

DIS
PEG_CLK_CPU_N — D42 CLKOUT_PCIE_N0
PEG_CLK_CPU_P — C42 CLKOUT_PCIE_P0
PEG_CLKREQ_CPU# — AR10 GPP_B5/SRCCLKREQ0#

WLAN
LAN_CLKREQ_CPU# — B42 CLKOUT_PCIE_N1, A42 CLKOUT_PCIE_P1, AT7 GPP_B6/SRCCLKREQ1#
WLAN_CLK_CPU_N — D41 CLKOUT_PCIE_N2
WLAN_CLK_CPU_P — C41 CLKOUT_PCIE_P2
WLAN_CLKREQ_CPU# — AT8 GPP_B7/SRCCLKREQ2#

NGFF1
SSD1_CLK_CPU_N — D40 CLKOUT_PCIE_N3
SSD1_CLK_CPU_P — C40 CLKOUT_PCIE_P3
SSD1_CLKREQ_CPU_N — AT10 GPP_B8/SRCCLKREQ3#
SSD2_CLKREQ_CPU_N — B40 CLKOUT_PCIE_N4, A40 CLKOUT_PCIE_P4, AU8 GPP_B9/SRCCLKREQ4#

CPU
SRCCLKREQ5# — E40 CLKOUT_PCIE_N5, E38 CLKOUT_PCIE_P5, AU7 GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N — F43
CLKOUT_ITPXDP_P — E43
GPD8/SUSCLK — BA17 SUS_CLK_CPU — TP1701
XTAL24_IN — E37 XTL_24M_X1_CPU
XTAL24_OUT — E35 XTL_24M_X2_CPU
XCLK_BIASREF — E42 XCLK_BIASREF — R1701 2K7R2F-GP — 1D0V_S5
RTCX1 — AM18 XTL_32K_X1_CPU
RTCX2 — AM20 XTL_32K_X2_CPU
SRTCRST# — AN18 SRTC_RST#
RTCRST# — AM16 RTC_RST#

3D3V_RTC_AUX
RN1701 SRN20KJ-1-GP
C1702 SC1U50V3KX-GP
G1701 GAP-OPEN
C1701 SC1U50V3KX-GP

RTC Reset

For AFR
RTCRST_ON — Q1701 2N7002K-2-GP — RTC_RST#
RTC_RST#_R
R1703 100KR2F-L3-GP
R1704 2K2R2J-L1-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 084.27002.0N31

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1702 10MR2J-L-GP
X1701 XTAL-32D768KHZ-88-GP
082.30003.0191
C1703 SC15P50V2JN-2-GP
C1704 SC15P50V2JN-2-GP

XTL_24M_X1_CPU
C1705 SC18P50V2JN-1-GP
U22
R1705 1MR2F-L-GP
X1702 XTAL-24MHZ-135-GP
INPUT/OUTPUT#1
NC#2
INPUT/OUTPUT#3
082.30006.0041
2nd = 82.30004.A01
XTL_24M_X2_CPU
C1706 SC18P50V2JN-1-GP

close to CPU
3D3V_S0
RN1702 SRN10KJ-12-GP
SSD1_CLKREQ_CPU_N
PEG_CLKREQ_CPU#
WLAN_CLKREQ_CPU#
SSD2_CLKREQ_CPU_N
RN1703 SRN10KJ-L-GP
LAN_CLKREQ_CPU#
SRCCLKREQ5#

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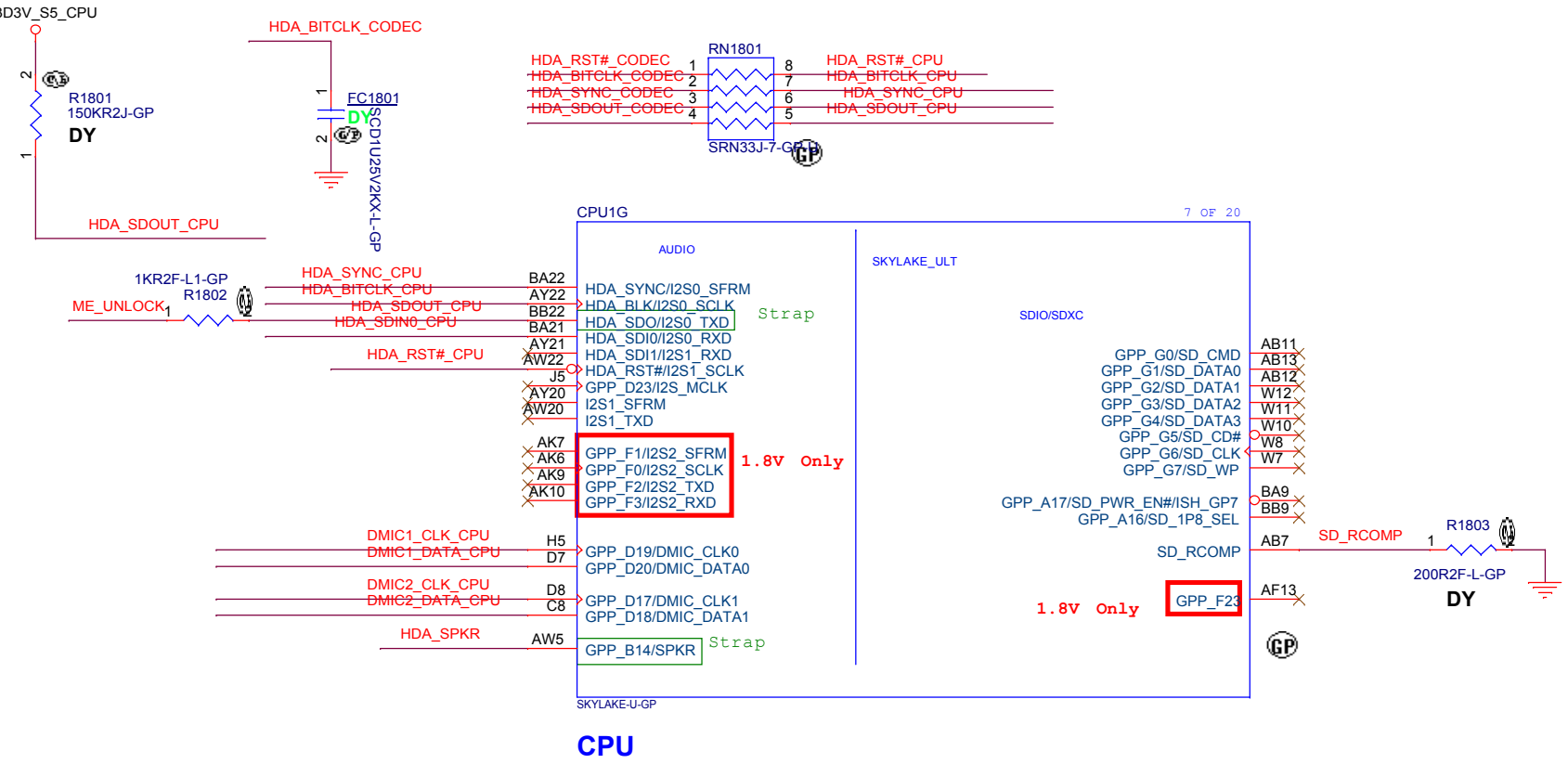
Main Func = PCH

Audio Code

[27] HDA_SDOUT_CODEC
[27] HDA_SDIN0_CPU
[15,27] HDA_SPKR
[27] HDA_RST#_CODEC
[24] ME_UNLOCK
[27] HDA_SYNC_CODEC
[27] HDA_BITCLK_CODEC
[55] DMIC2_DATA_CPU
[55] DMIC1_DATA_CPU
[55] DMIC1_CLK_CPU
[55] DMIC2_CLK_CPU



CPU

18.3 Terminating Unused SDXC Signals

SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

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Title: CPU_(AUDIO/SDIO/SDXC)

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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Main Func = PCH

LPC

[24,68,91] LPC_AD_CPU_P0
[24,68,91] LPC_AD_CPU_P1
[24,68,91] LPC_AD_CPU_P2
[24,68,91] LPC_AD_CPU_P3
[24,68,91] LPC_FRAME#_CPU
[19,24] LPC_CLK_KBC
[19,68] LPC_CLK_DBG

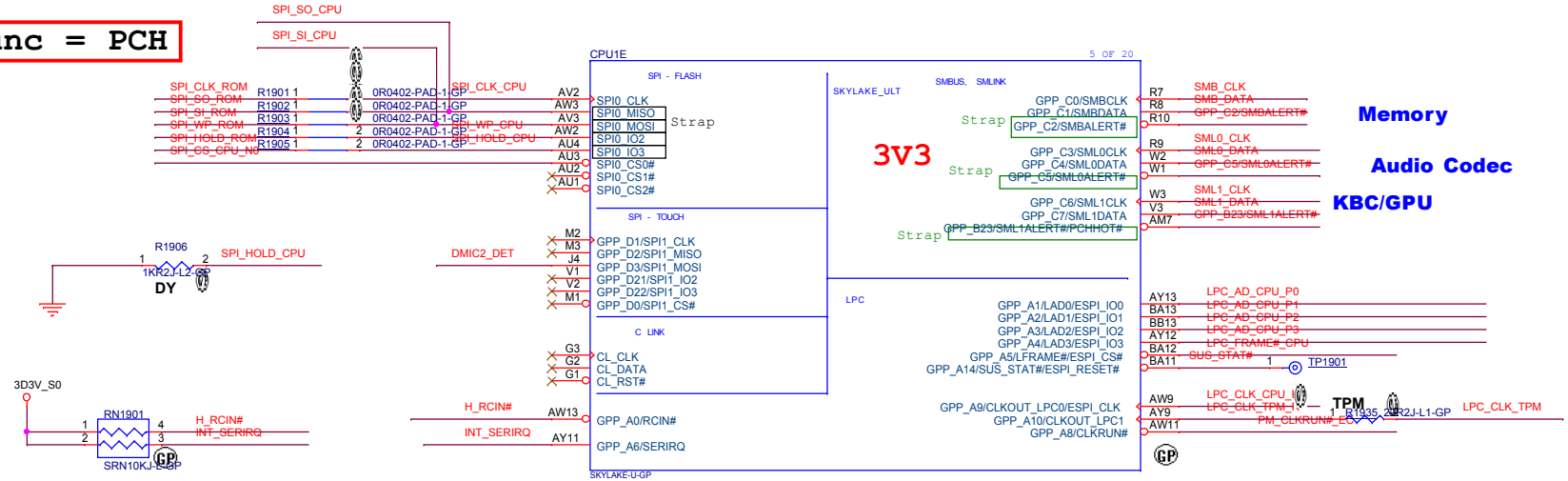
SPI

[24,25] SPI_CS_CPU_N0
[24,25] SPI_CLK_ROM
[15,25] SPI_WP_ROM
[15,25] SPI_HOLD_ROM
[24,25] SPI_SO_ROM
[24,25] SPI_SI_ROM
[15] SPI_SO_CPU
[15] SPI_SI_CPU

DM1&2 TPAD and XDP

KBC

[24,79] SML1_CLK
[24,79] SML1_DATA
[24] H_RCIN#
[24,68,91] INT_SERIRQ
[24,91] PM_CLKRUN#_EC
[13] SMB_DATA_CPU
[13] SMB_CLK_CPU
[19,24] LPC_CLK_KBC
[19,68] LPC_CLK_DBG
[15] GPP_C2/SMBALERT#
[15] GPP_C5/SML0ALERT#
[15] GPP_B23/SML1ALERT#
[91] LPC_CLK_TPM
[55,89] DMIC2_DET



Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

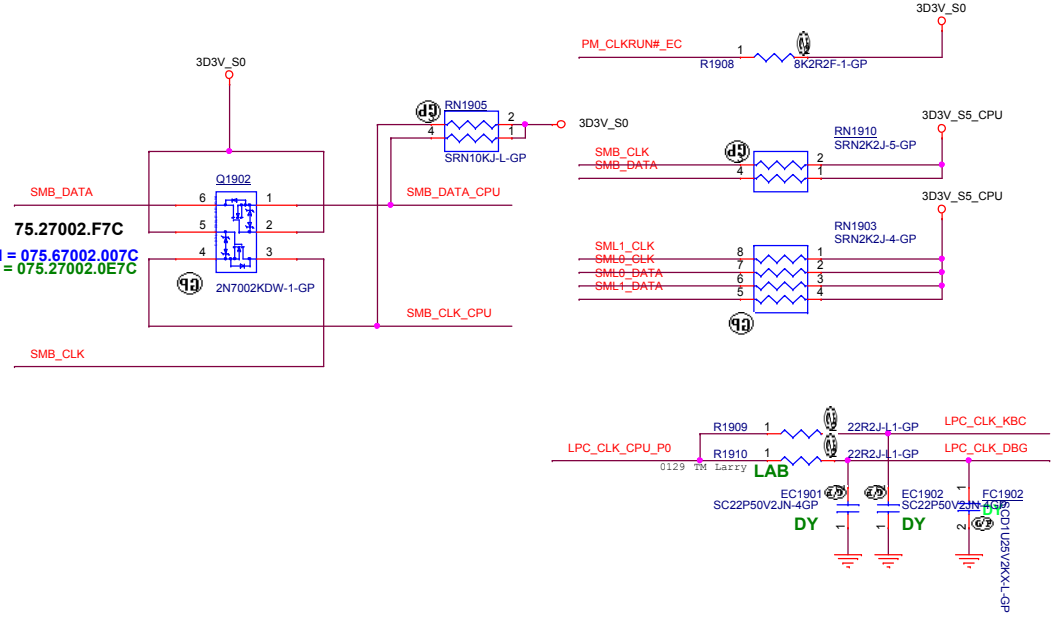
20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.



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Title: LPC,SPI,SMBUS,CLINK

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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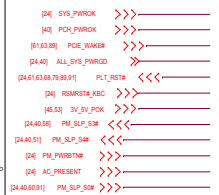
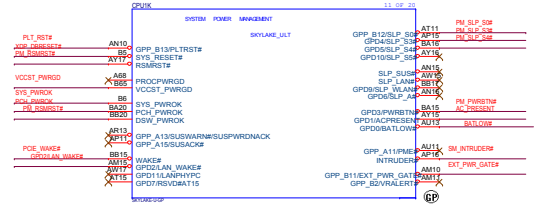
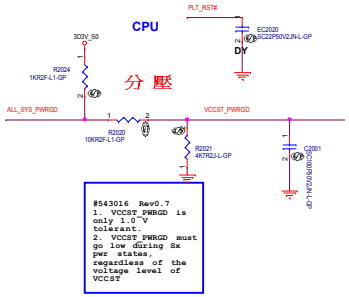
Main Func = PCH

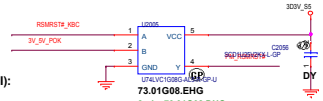




CPU

BATLOW#:
Pull-up required even if not implemented.

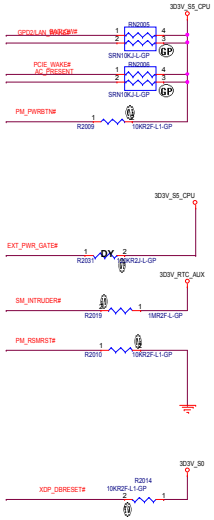




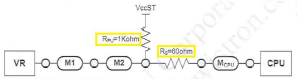
GPP_A13-15 pin(LPC/eSPI):

73.01G08.EHG
2nd = 73.01G08.DHG

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)



VCCST_PWRGOOD



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

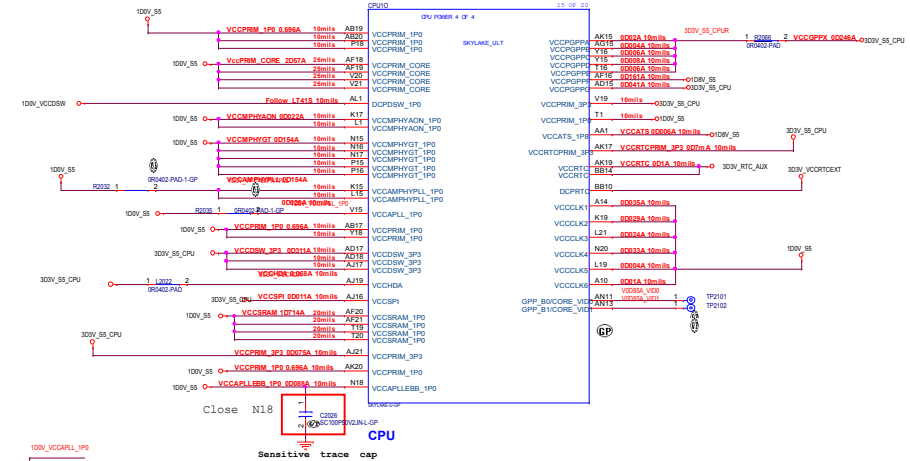


Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SML0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

Title: **CPU_(POWER MANAGEMENT)**

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 20 of 105

Main Func = PCH

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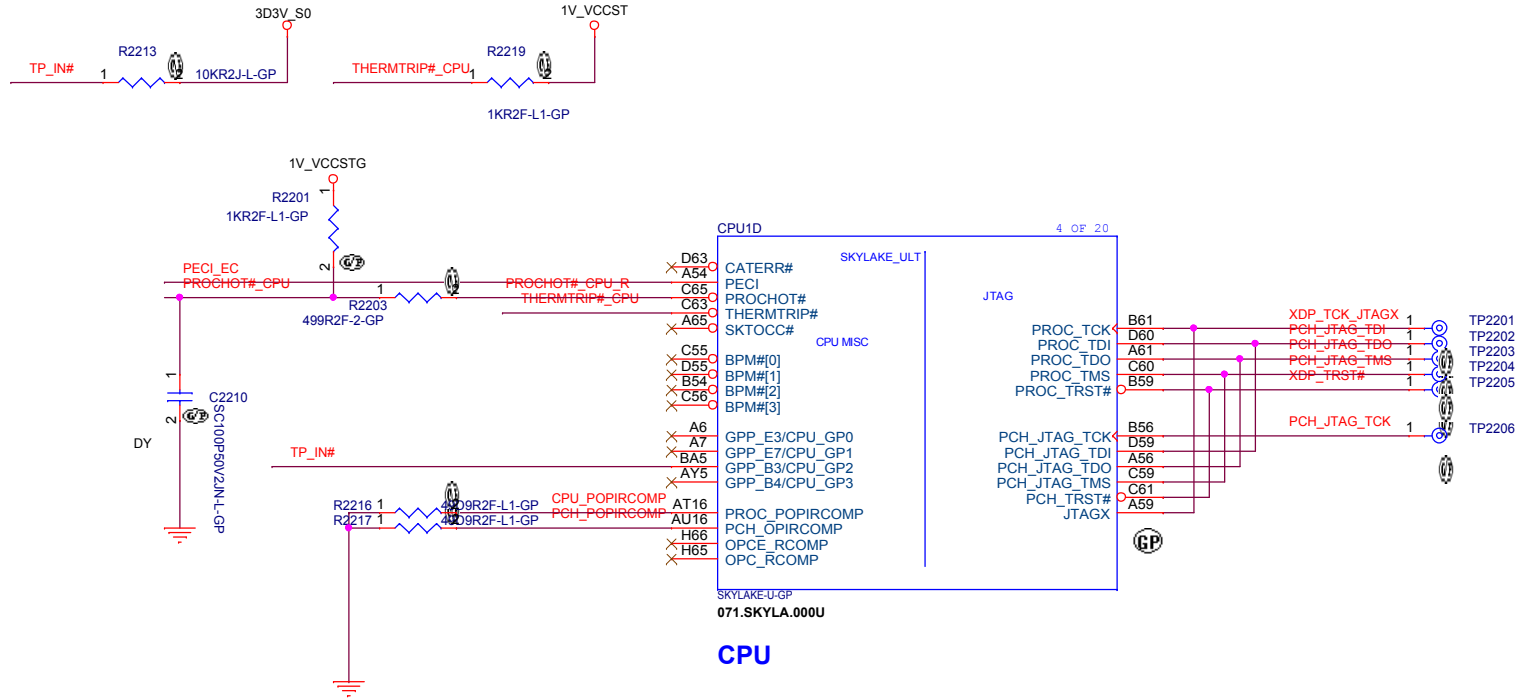
Title: CPU_(VSS)

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 21 of 106

Main Func = CPU

[24] PECI_EC
[24,44,46] PROCHOT#_CPU
[65] TP_IN#



CPU

PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

<Core Design>

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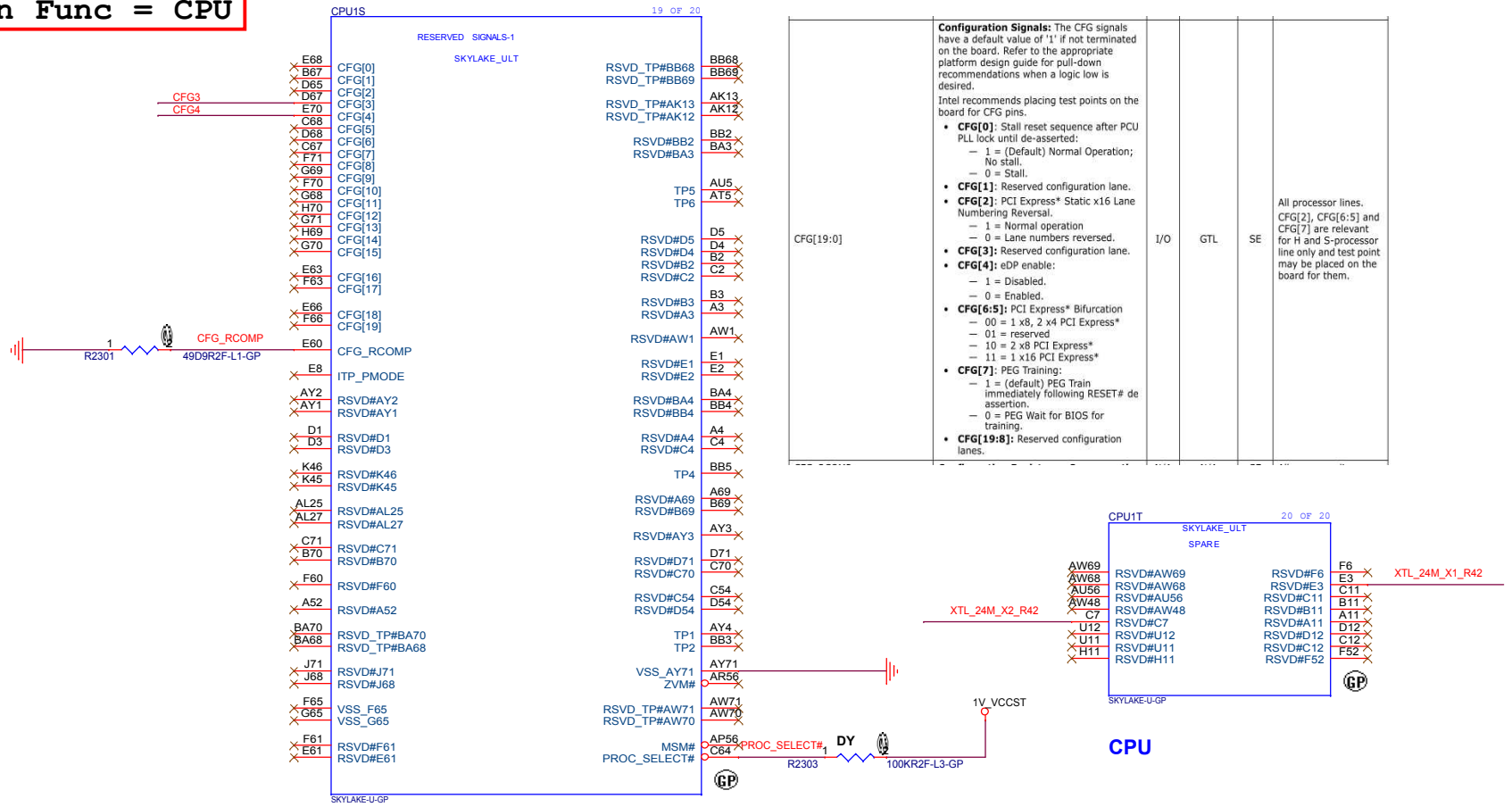
Title: **CPU_(JTAG/CPU SIDE BAND)**

Size	Document Number	Rev
Custom	Strongbow_KL	1

Date: Monday, January 15, 2018 Sheet 22 of 106

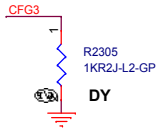
Main Func = CPU



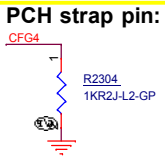
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

CPU

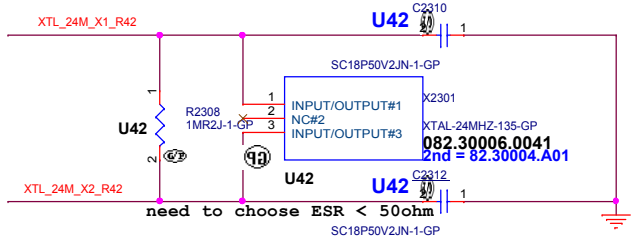
PCH strap pin:



PCH strap pin:



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines

<Core Design>

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Title: **CPU_RESERVED,CFG**

Size: Custom | Document Number: **Strongbow_KL** | Rev: 1

Date: Monday, January 15, 2018 | Sheet 23 of 106

SSID = KBC

Power

Signal

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

Type_C

Charger

Close to the EC

For EC power consumption reserver

VCC_LPC(Pin9)

GPU ---> BATTER /CHARGER --->

Touch Pad

2017/11/1 BS Rober

071.09028.000G

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

close RN2407

GPIO0 High Active

84.03906.R11
2nd = 84.13906.E11

68.00084.921
2nd = 68.00217.401

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Sapero		100K	
Strongbow_KL_UMA	0K		
Strongbow_KL_DIS	100.0K	33.0K	2.481V
Reserver	100.0K	47.0K	2.245
Reserver	100.0K	64.9K	2.001V
Reserver	100.0K	76.8K	1.867V
Reserver	100.0K	100K	1.650V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.335 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.553 V	0.659 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
150W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
180W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.395 V
Reserved	76.8 K	100.0 K	1.433 V	1.458 V	>= 1.395 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
0A	100.0 K	10.0 K	0.000 V	0.000 V	>= 2.875 V	
0B	100.0 K	20.0 K	0.750 V	0.769 V	>= 2.616 V	< 2.875 V
0C	100.0 K	33.0 K	2.481 V	2.481 V	>= 2.350 V	< 2.616 V
0D	100.0 K	47.0 K	2.549 V	2.299 V	>= 2.123 V	< 2.350 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.954 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.857 V	1.883 V	>= 1.759 V	< 1.954 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.554 V	< 1.759 V
Reserved for project use	100.0 K	143.0 K	1.359 V	1.374 V	>= 1.281 V	< 1.554 V
Reserved for project use	100.0 K	174.0 K	1.224 V	1.220 V	>= 1.120 V	< 1.281 V
Reserved for project use	100.0 K	210.0 K	1.048 V	1.062 V	>= 0.924 V	< 1.120 V

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Title: KBC_KB9028

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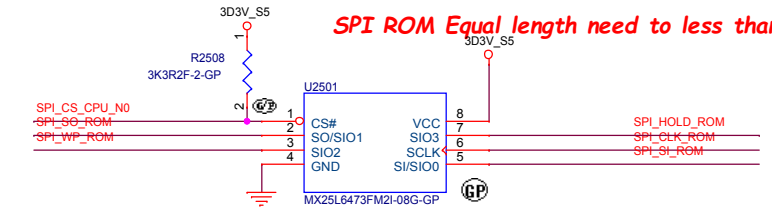
[19,24] SPI_CS_CPU_N0
[19,24] SPI_SO_ROM
[15,19] SPI_WP_ROM

[15,19] SPI_HOLD_ROM
[19,24] SPI_CLK_ROM
[19,24] SPI_SI_ROM
[6] RTC_DET#

Main Func = SPI Flash

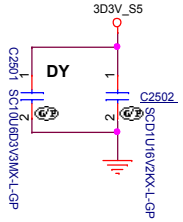
SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

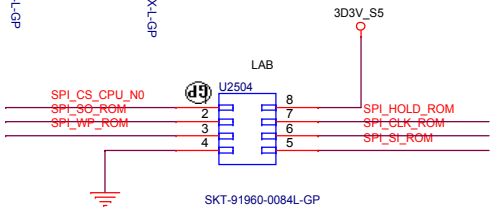


072.25647.000D

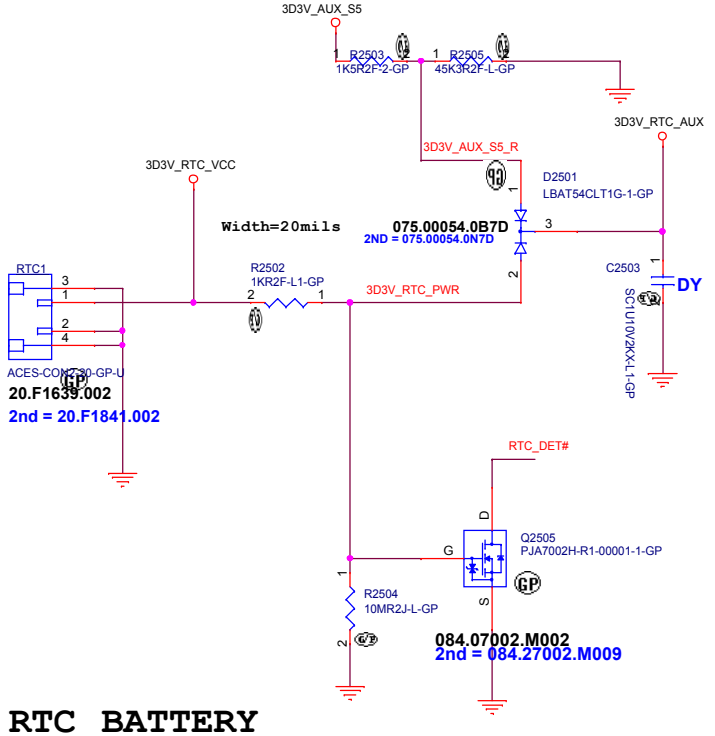
2nd = 072.25Q64.0H01



072.25647.000D_MX25L6473FM2I-08G_MXIC
072.25Q64.0H01_W25Q64FVSSIQ_WINBOND



Main Func = RTC



RTC BATTERY
1st= TBD
2nd= TBD

<Core Design>

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Title: *Flash(KBC+PCH)/RTC*

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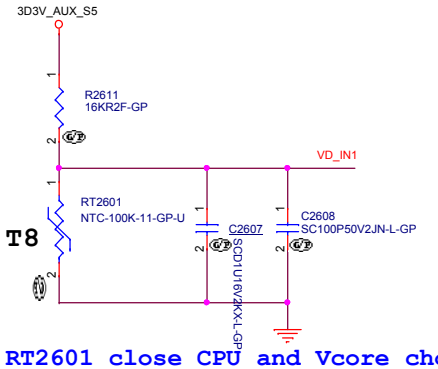
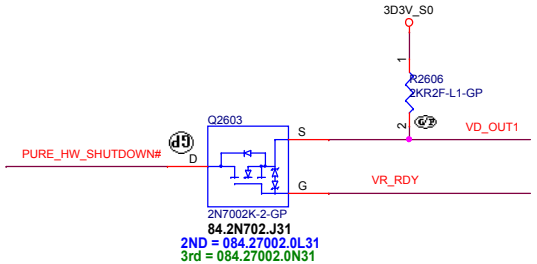
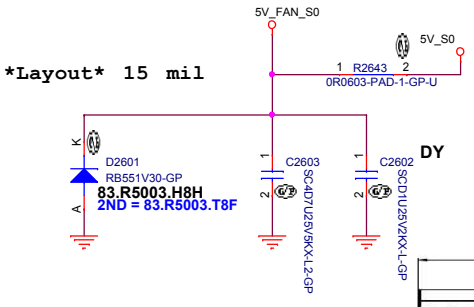
SSID = Thermal

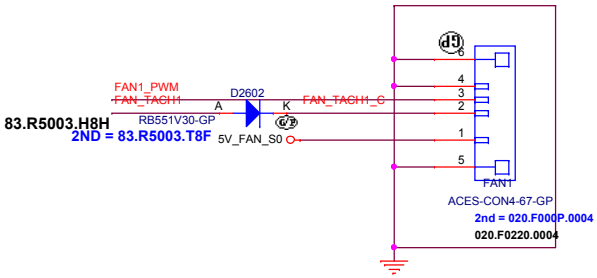
[24] VD_IN1
[24] FAN1_PWM
[24] FAN_TACH1
[24] FAN_TACH1_C
[24,40] PURE_HW_SHUTDOWN#
[24] VD_OUT1
[40,46] VR_RDY
[20,24,40,58] PM_SLP_S3#

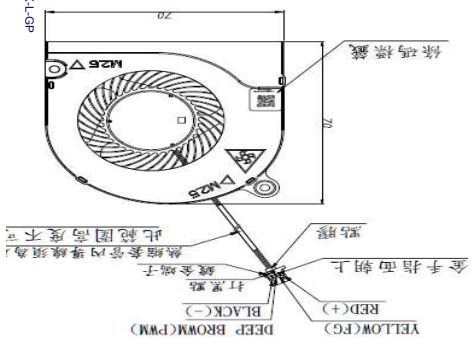


RT2601 close CPU and Vcore chock
VD_IN1 trace 10 mli









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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

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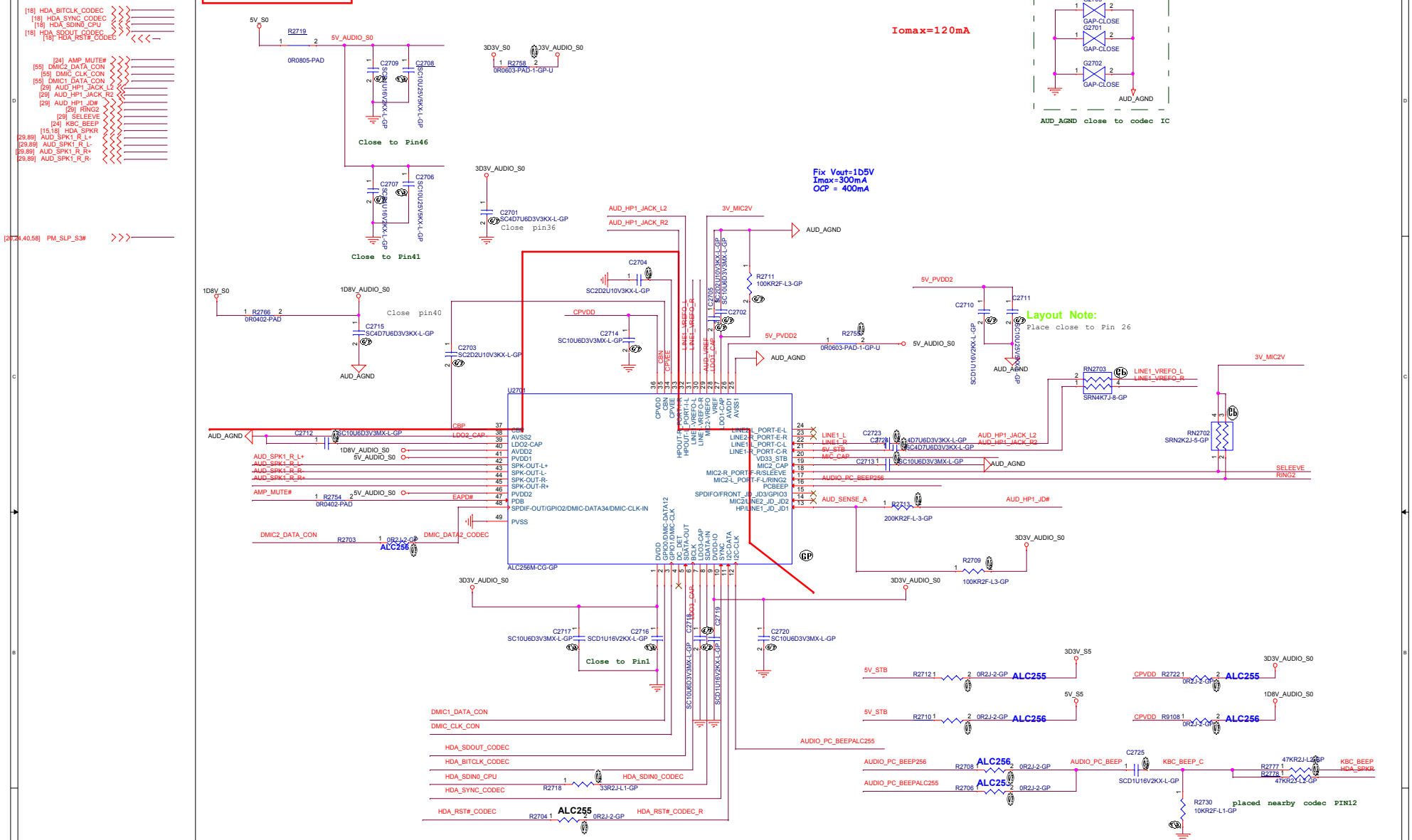
SSID = AUDIO



<Core Design>

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Title	Audio Codec ALC256
Size: Custom	Document Number: Strongbow_KL
Rev	1
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<Core Design>

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Title

Size	Document Number	Rev
A4	Strongbow_KL	1

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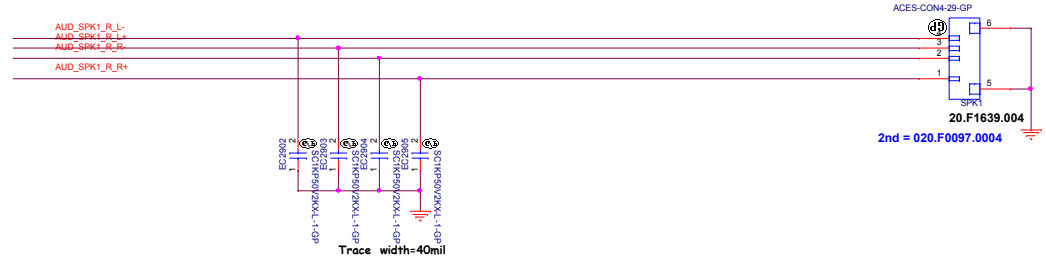
SSID = AUDIO *Speaker*

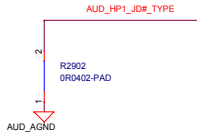
[27,89] AUD_HP1_JACK_R1

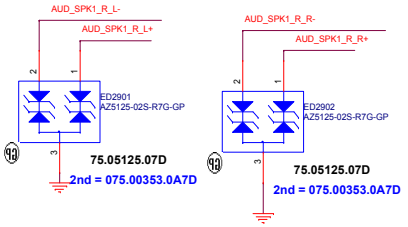
[27,89] AUD_HP1_JACK_L1

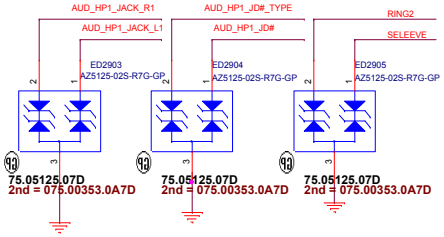
[27,89] AUD_SPK1_R_L-
[27,89] AUD_SPK1_R_L+
[27,89] AUD_SPK1_R_R-
[27,89] AUD_SPK1_R_R+

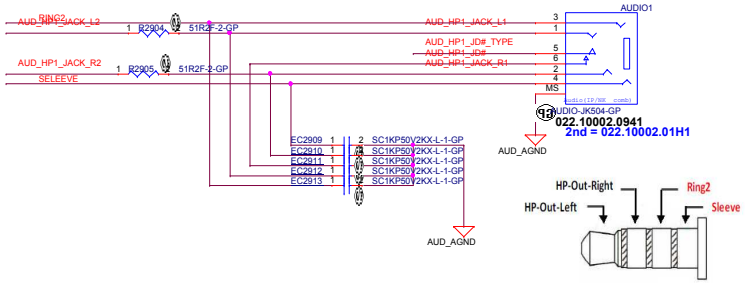
[27] AUD_HP1_JACK_L2
[27] AUD_HP1_JACK_R2
[27] AUD_HP1_JD#
[27] RING2
[27] SELEEVE











<Core Design>

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Title: ***Speaker/HPMIC***

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<Core Design>

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Title		
Size A4	Document Number Strongbow_KL	Rev 1
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<Core Design>

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Title
(LAN+VGA) CONNECTOR

Size	Document Number	Rev
A4	**Strongbow_KL**	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5170(CARD READER)***

Size	Document Number	Rev
A3	Strongbow_KL	1

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SSID = SDIO

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<Core Design>

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Title

Size	Document Number	Rev
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	Strongbow_KL	1

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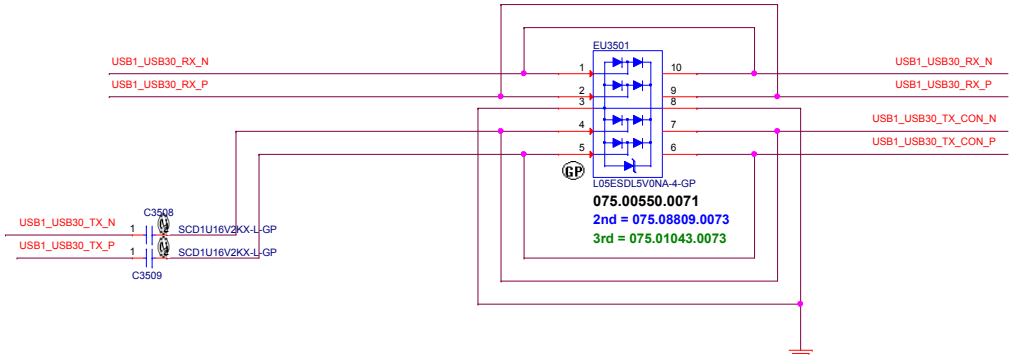
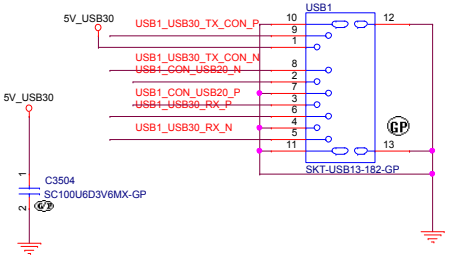
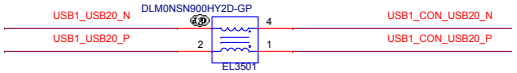
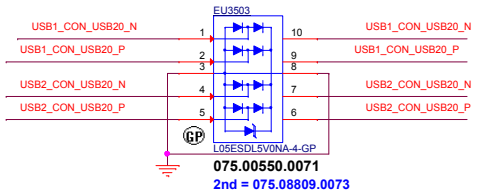
[16] USB1_USB20_N
[16] USB1_USB20_P
[24,66] USB_PWR_EN
[16] USB1_USB30_RX_N
[16] USB1_USB30_RX_P
[16] USB1_USB30_TX_N
[16] USB1_USB30_TX_P
[89] USB1_CON_USB20_N
[89] USB1_CON_USB20_P
[36] USB2_USB20_CHAR_N
[36] USB2_USB20_CHAR_P
[16] USB2_USB30_RX_N
[16] USB2_USB30_RX_P
[16] USB2_USB30_TX_N
[16] USB2_USB30_TX_P
[89] USB2_CON_USB20_N
[89] USB2_CON_USB20_P

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

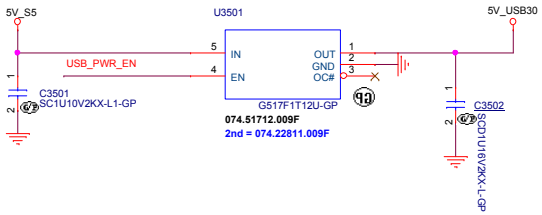


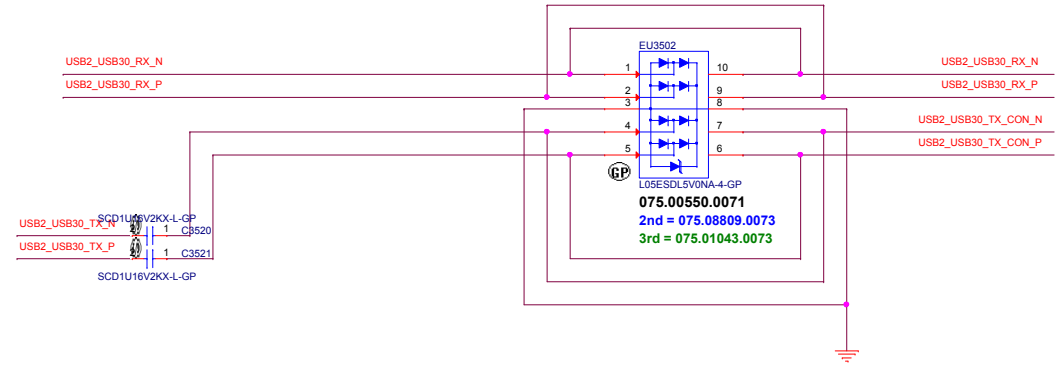


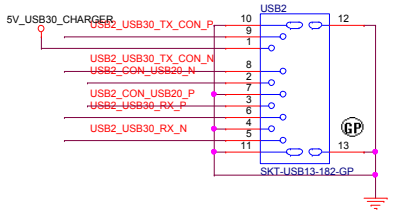


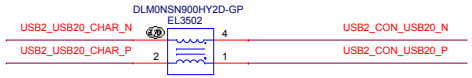


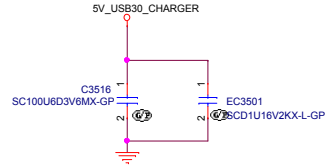
High Active 2A











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Title: **USB 3.0**

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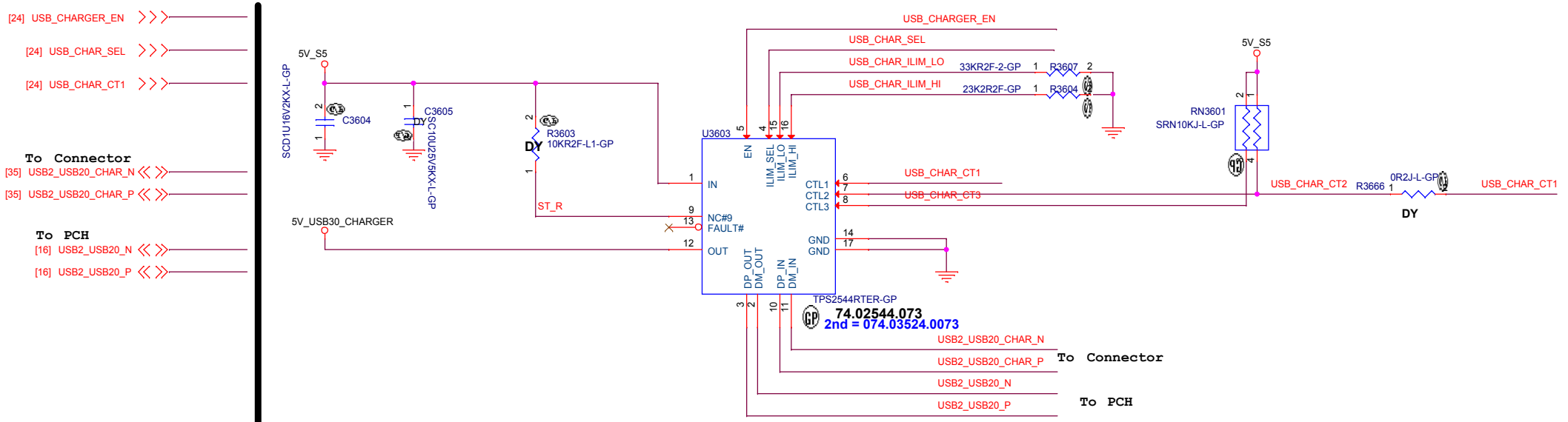

CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines
0	1	1	X			Disconnected
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

S5 (at low bateery and non support charger)

S3 and S5 state

S0 and S3 (at low bateery and non support charger)

S0 state

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Title: USB CHARGER

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Title	***Reserved***	
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Title		
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Title		
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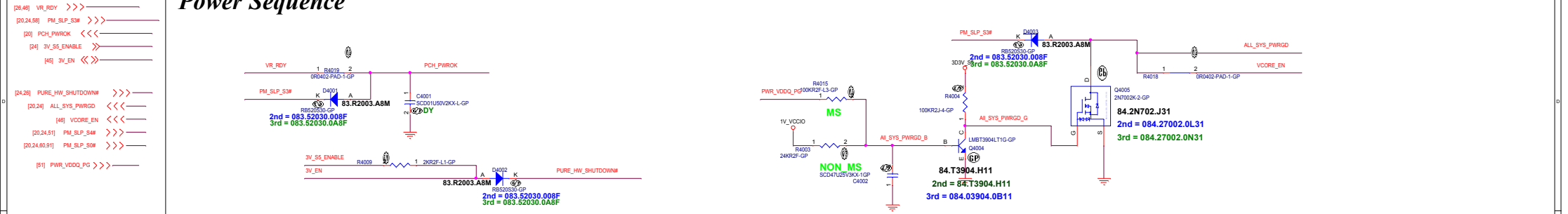
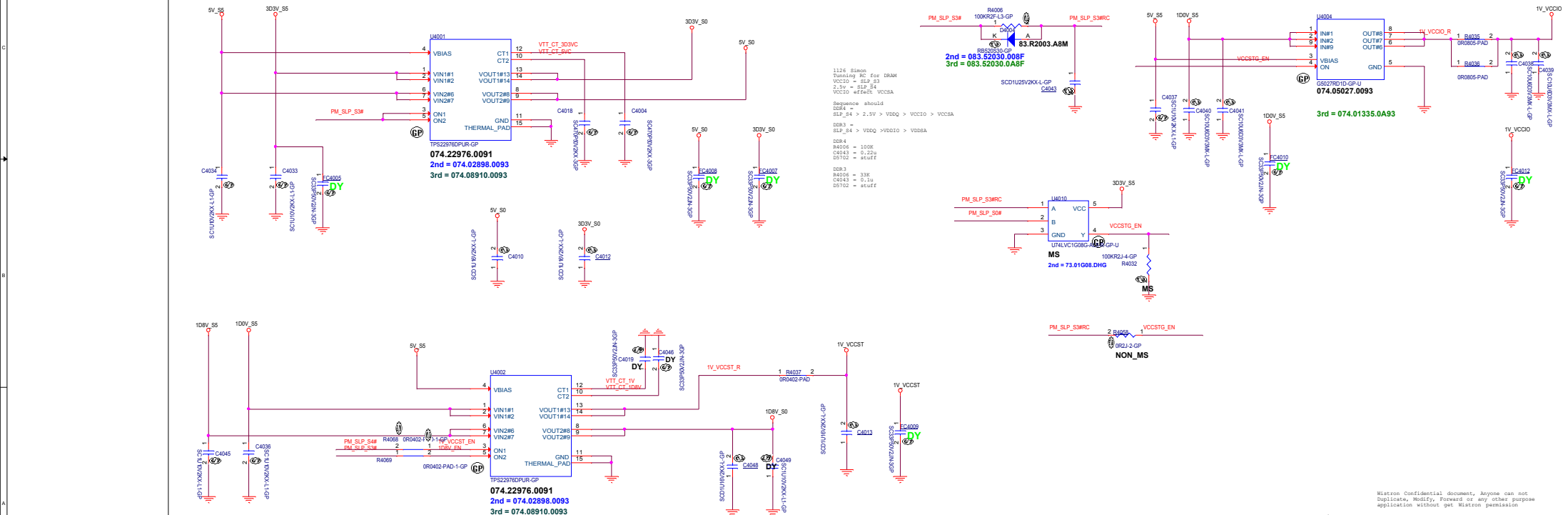
Power Sequence



ANNIE Run Power



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Title: Power Plane Enable & SEQUENCE

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Title: ***DCIN JACK***

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ANNIE solution

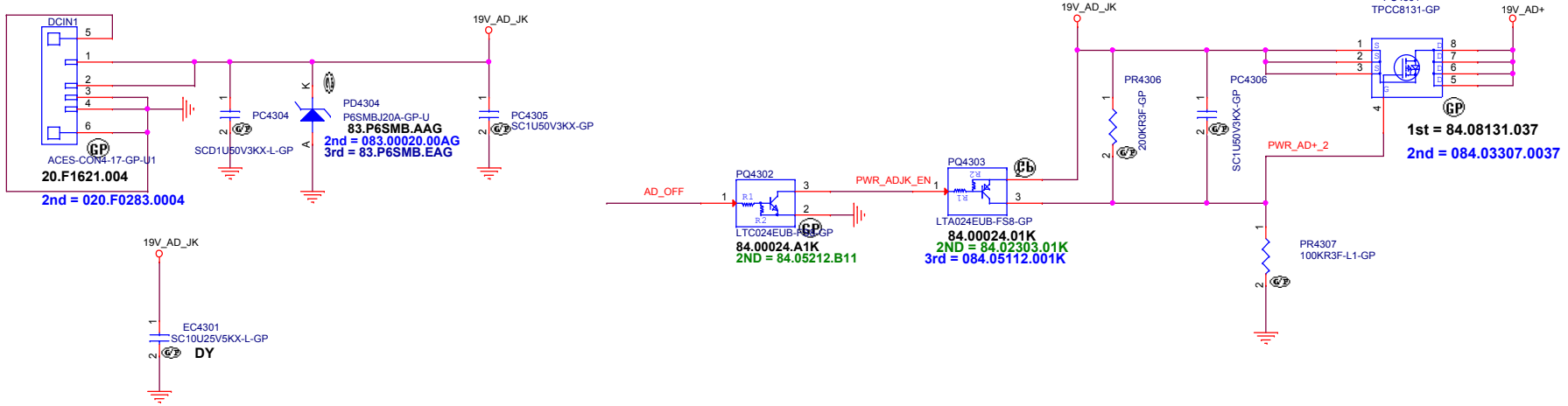
[24] AD_OFF

[24,44] BAT_IN#
[24,44] BAT_SCL
[24,44] BAT_SDA

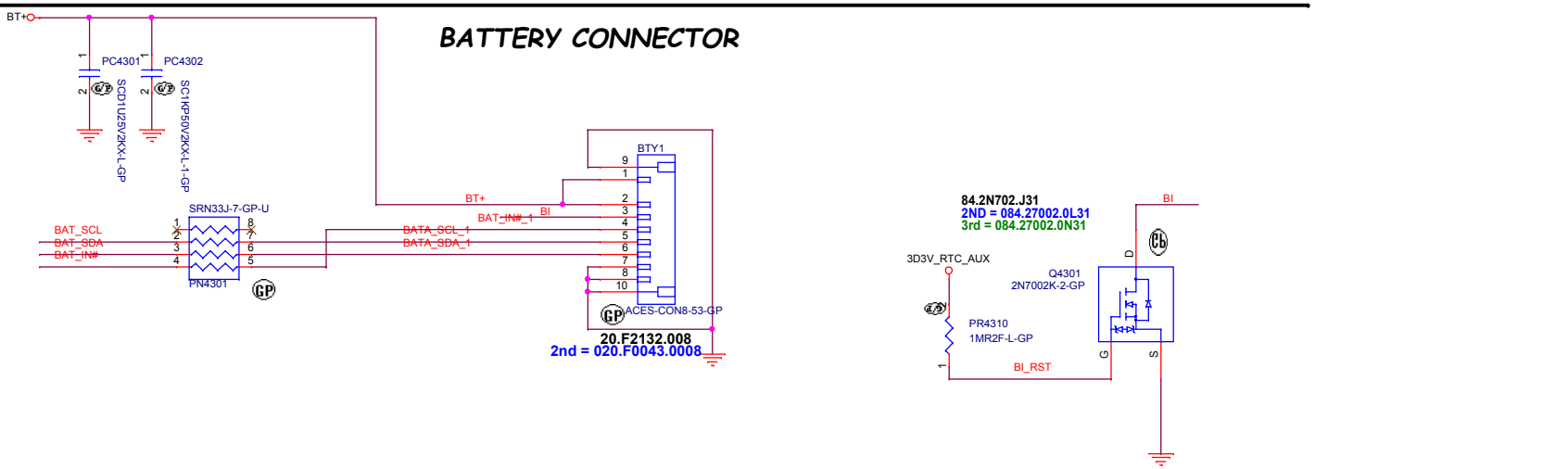
[89] BI
[89] BAT_IN#_1
[89] BATA_SCL_1
[89] BATA_SDA_1

[66,89] BI_RST

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title	**BATT CONN**
Size: A3	Document Number: **Strongbow_KL**
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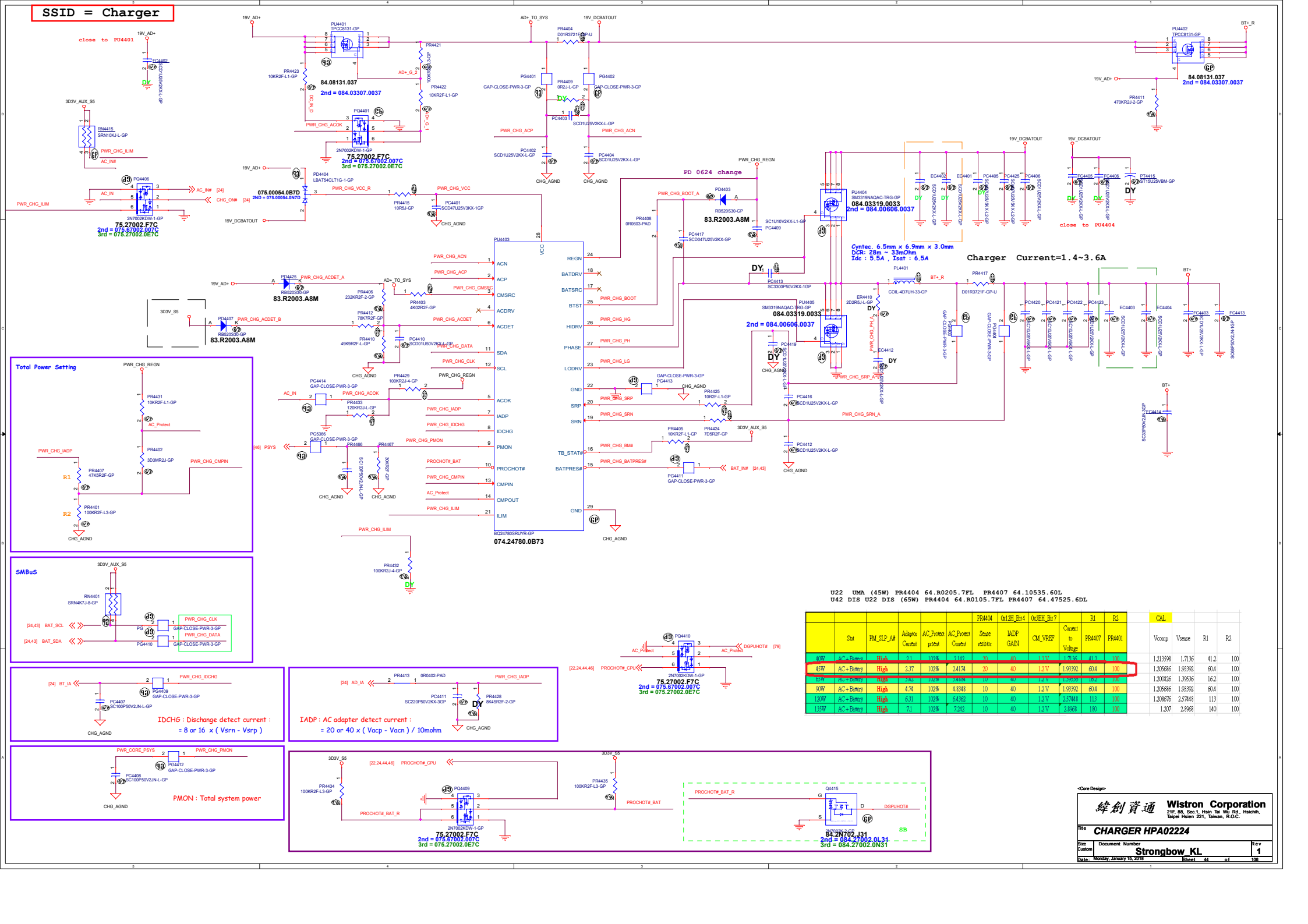
SSID = Charger



U22 UMA (45W) PR4404 64.R0205.7FL PR4407 64.10535.60L
U42 DIS U22 DIS (65W) PR4404 64.R0105.7FL PR4407 64.47525.6DL

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect prcent	AC_Protect Current	PR4404 Sense resistor	0x12H_Bit4 IADP GAIN	0x39H_Bit 7 OM_VREF	Current to Voltage	R1	R2	CAL Vcomp	Vsense	R1	R2
40W	AC+Battery	High	2.1	102%	2.142	20	40	1.2 V	1.93392	60.4	100	1.213598	1.7136	41.2	100
45W	AC+Battery	High	2.37	102%	2.4174	20	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
65W	AC+Battery	High	3.42	102%	3.4884	10	40	1.2 V	1.39536	16.2	100	1.200826	1.39536	16.2	100
90W	AC+Battery	High	4.74	102%	4.8348	10	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
120W	AC+Battery	High	6.31	102%	6.4362	10	40	1.2 V	2.57448	113	100	1.208676	2.57448	113	100
135W	AC+Battery	High	7.1	102%	7.242	10	40	1.2 V	2.8968	180	100	1.207	2.8968	140	100

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Title: CHARGER HPA02224

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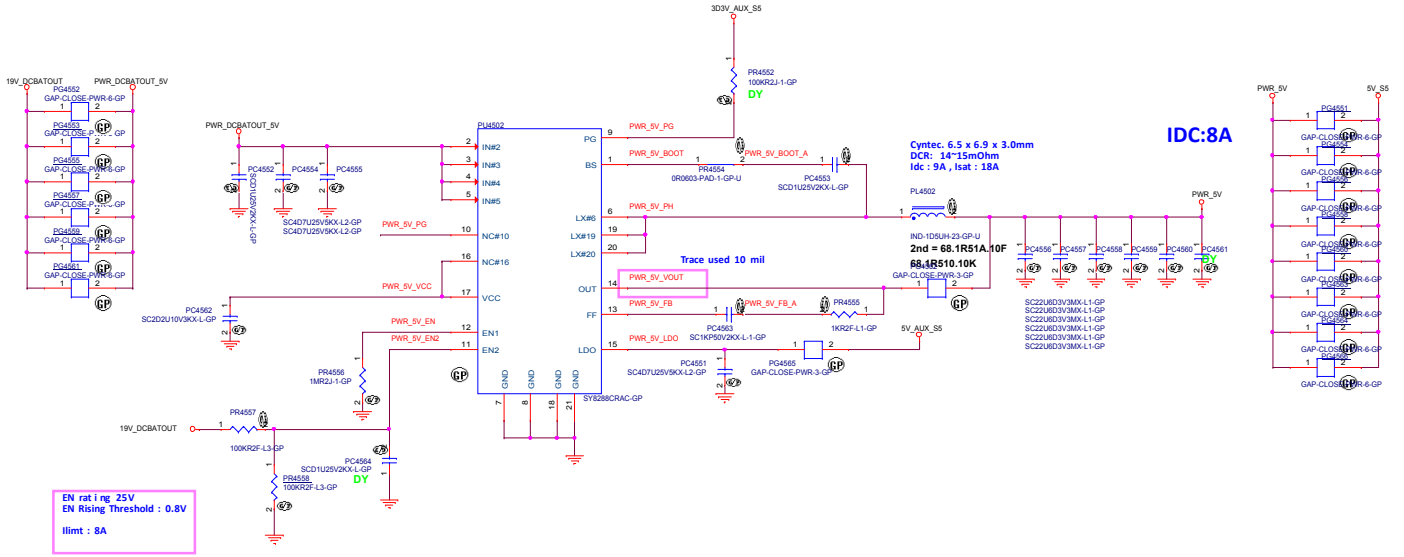
OFFPAGE

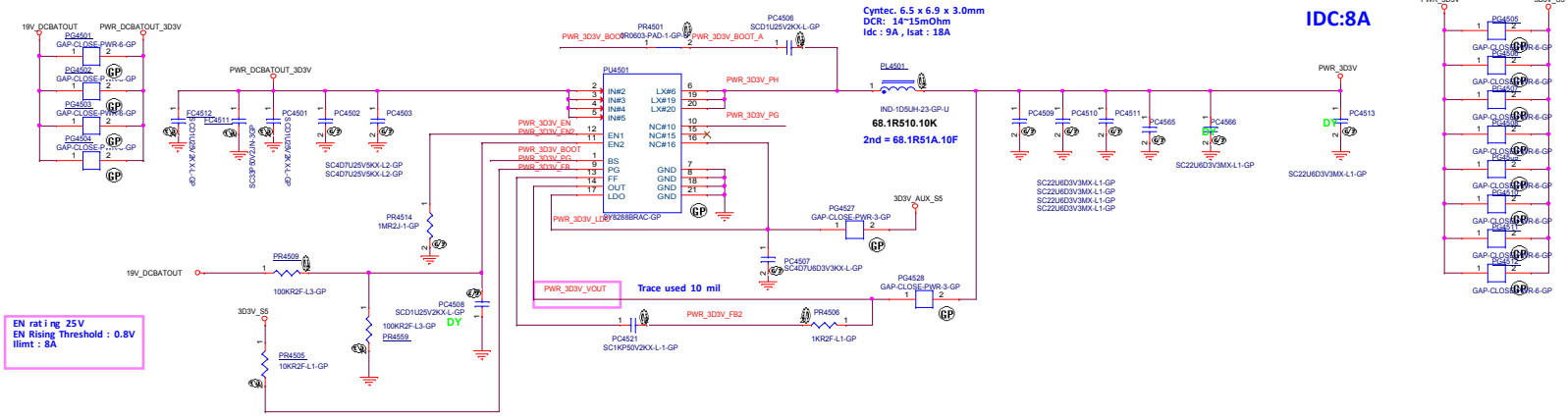
[24] 5V_EN — PR4517 0R0402-PAD-1-GP — PWR_5V_EN

OFFPAGE

[40] 3V_EN — PR4515 0R0402-PAD-1-GP — PWR_3D3V_EN

[20,53] 3V_5V_POK — PR4516 0R0402-PAD-1-GP — PWR_3D3V_PG





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Title: RT6575D_5V/3D3V

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Main Func = CPU_CORE

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[22,24,44] PROCHOT#_CPU — PR4602 0R0402-PAD-1-GP — PWR_CPU_PROCHOT#

[7] SVID_ALERT#_CPU — PR4603 0R0402-PAD-1-GP — PWR_VCORE_ALERT#

[7] SVID_CLK_CPU — PR4607 0R0402-PAD-1-GP — VIDSCK_CPU_R

[7] SVID_DATA_CPU — PR4608 0R0402-PAD-1-GP — VIDSOUT_CPU_R

[26,40] VR_RDY — PR4612 0R0402-PAD-1-GP — PWR_IMVP_PWRGD

[40] VCORE_EN — PR4616 0R0402-PAD-1-GP — PWR_VR_EN

[7] VSSCORE_SENSE — PR4617 0R0402-PAD-1-GP — PWR_VCORE_RTN

[7] VCCCORE_SENSE — PR4627 0R0402-PAD-1-GP — PWR_VCORE_VSEN

[8] VCCGT_SENSE — PR4623 0R0402-PAD-1-GP — PWR_VCCGT_VSEN

[8] VSSGT_SENSE — PR4625 0R0402-PAD-1-GP — PWR_VCCGT_RTN

[8] VSSSA_SENSE — PR4631 0R0402-PAD-1-GP — PWR_VCCSA_RTN

[8] VCCSA_SENSE — PR4634 0R0402-PAD-1-GP — PWR_VCCSA_FB2

[44] PSYS — PR4643 0R0402-PAD-1-GP — PWR_VCORE_PSYS

1V_VCCST — PR4600 0R0402-PAD-1-GP — PR4601 0R0402-PAD-1-GP — PC4602 SC31U25V2KX-L-GP

PR4603 0R0402-PAD-1-GP — PR4605 0R0402-PAD-1-GP — PR4606 0R0402-PAD-1-GP — PR4607 0R0402-PAD-1-GP — PR4608 0R0402-PAD-1-GP — PR4612 0R0402-PAD-1-GP — PR4616 0R0402-PAD-1-GP — PR4617 0R0402-PAD-1-GP — PR4627 0R0402-PAD-1-GP — PR4623 0R0402-PAD-1-GP — PR4625 0R0402-PAD-1-GP — PR4631 0R0402-PAD-1-GP — PR4634 0R0402-PAD-1-GP — PR4643 0R0402-PAD-1-GP

VIDSOUT_CPU_R — PWR_VCORE_ALERT# — VIDSCK_CPU_R

1V_VCCST — PR4619 1KR2F-L1-GP — PR4601 100R2F-L3-GP — PWR_CPU_PROCHOT# — PWR_VCORE_VRHOT#

PWR_VREF

PR4604 4K22R2F-GP — PWR_VCORE_SET1_A — PR4613 226R2F-GP — PWR_VCORE_SET1 — PR4620 4K22R2F-GP — PWR_VCORE_SET1_B — PR4629 95D3R2F-GP

PR4605 9K53R2F-GP — PWR_VCORE_SET2_A — PR4614 0R0402-PAD-1-GP — PWR_VCORE_SET2 — PR4621 9K1R2F-1-GP — PWR_VCORE_SET2_B — PR4630 143R2F-1-GP

PR4606 21KR3F-GP — PWR_VCORE_SET3_A — PR4615 392R2F-GP — PWR_VCORE_SET3 — PR4622 10K7R2F-GP — PWR_VCORE_SET3_B — PR4626 130R2F-1-GP

5V_S5 — PR4618 8D2R3F-GP — PC4603 SC4D7U6D3V3KX-L-GP

PWR_VREF — PR4624 37K4R2F-1-GP — PR4628 2D2R3F-L-GP — PC4606 SCD22U25V3KX-GP — PC4608 SC1KP50V2JN-2GP

19V_DCBATOUT

PWR_VREF — PR4632 3D9R2F-GP — PC4604 SCD47U25V3KX-1GP

PWR_VREF — PR4633 41K2R2F-GP — PC4610 SC1KP50V2JN-2GP

VIDSCK_CPU_R — VIDSOUT_CPU_R — PR4638 49D9R2F-L1-GP — PR4639 10R2F-L1-GP

3D3V_S0 — PR4636 10KR2F-L1-GP

PWR_IMVP_PWRGD — PWR_VCORE_VRHOT# — PWR_VCORE_SCLK — PWR_VCORE_SDIO — PWR_VCORE_ALERT#

PWR_VREF — PR4640 36K5R2F-GP — PWR_VCORE_IMON_A — PR4641 11K5R2F-GP — PC4612 SC1KP50V2JN-2GP

PR4678 NTC-100K-12-GP-U — B = 4250 — PWR_VCORE_IMON_B — PR4642 44K2R2F-1-GP

PWR_VCCGT_VSEN — PR4648 10KR2F-L1-GP — PWR_VCCGT_COMP_B — PR4649 0R0402-PAD-1-GP — PR4650 21KR2F-GP — PWR_VCCGT_COMP_A — PR4651 120R2F-GP — PC4617 SC68P50V2JN-1GP — PC4616 SC220P50V2KX-3GP

PC4618 SC1KP50V2JN-2GP — PWR_VCCGT_FB_A — PR4653 0R2F-1-GP

5V_S5 — SB — PR4645 0R0402-PAD-1-GP — PWR_VCORE_DRVEN_SET

PWR_VCORE_VSEN — PR4657 10KR2F-L1-GP — PWR_VCORE_COMP_B — PR4658 0R0402-PAD-1-GP — PR4659 52K3R2F-L-GP — PWR_VCORE_COMP_A — PR4660 0R0402-PAD-1-GP — PC4620 SC68P50V2JN-1GP — PC4619 SC220P50V2KX-3GP — PR4663 0R2F-1-GP — PC4621 SC1KP50V2JN-2GP — PWR_VCORE_FB_A

PWR_VCCSA_FB2 — PR4666 10KR2F-L1-GP — PWR_VCCSA_COMP_B — PR4667 0R0402-PAD-1-GP — PR4668 73K2R2F-GP — PWR_VCCSA_COMP_A — PR4669 0R0402-PAD-1-GP — PC4623 SC68P50V2JN-1GP — PC4622 SC470P50V2KX-L-GP

PC4624 SC1KP50V2JN-2GP — PWR_VCCSA_FB_A — PR4673 0R2F-1-GP

PU4601 RT3602AEGQW-GP — 074.03602.0073

PWR_VCORE_PSYS — PWR_VCORE_VCC — PWR_VCORE_SET1 — PWR_VCORE_SET2 — PWR_VCORE_SET3 — PWR_VCORE_VIN — PWR_VCCGT_IMON — PWR_VCORE_IMON — PWR_VCCSA_IMON — PWR_VR_EN — PWR_VCCGT_VSEN — PWR_VCCGT_COMP — PWR_VCCGT_FB — PWR_VCCGT_RTN — PWR_VCORE_DRVEN_SET — PWR_VCORE_COMP — PWR_VCORE_FB — PWR_VCORE_RTN — PWR_VCORE_VSEN — PWR_VCCSA_COMP — PWR_VCCSA_FB — PWR_VCCSA_RTN

PWM_SA — PWR_VCCSA_PWM [50]

ISENP_SA — PWR_VCCSA_ISUMP — PC4601 SC1KP50V2JN-2GP — PWR_VCCSA_ISUMP [50]

ISENN_SA — PWR_VCCSA_ISUMN — PC4605 SCD1U25V2KX-L-GP — PWR_VCCSA_ISUMN [50]

PWM_AUXI — PWR_VCCGT_PWM [48]

ISENP_AUXI — PWR_VCCGT_ISUMP — PC4607 SC1KP50V2JN-2GP — PWR_VCCGT_ISUMP [48]

ISENN_AUXI — PWR_VCCGT_ISUMN — PC4609 SCD1U25V2KX-L-GP — PWR_VCCGT_ISUMN [48]

PWM1_MAIN — PWR_VCORE_PWMA [47]

ISEN1P_MAIN — PWR_VCORE_ISUMP_A — PC4611 SC1KP50V2JN-2GP — PWR_VCORE_ISUMP_A [47]

ISEN1N_MAIN — PR4683 1KR2F-GP — PWR_VCORE_ISEN1N_B — PC4613 SCD1U25V2KX-L-GP — PWR_VCORE_ISUMN_A [47]

PWM2_MAIN — PWR_VCORE_PWMB [47]

ISEN2P_MAIN — PWR_VCORE_ISUMP_B — PR4682 0R2F-2-GP — PR4684 — PWR_VCORE_ISUMP_B [47]

ISEN2N_MAIN — PWR_VCORE_ISEN2N_B — PR4652 0R2F-2-GP — PWR_VCORE_ISUMN_B [47]

	PR4652	PR4682	PR4684
U22	0	0	DY
U42	DY	DY	1R

U22_U42_1 — U42_2 — U22_U42_1

DRVEN — PWR_VCORE_FCCM# [47,48,50] — PC4615 SCD1U25V2KX-L-GP

TSEN_AUXI — PWR_VCCGT_TSEN

TSEN_MAIN — PWR_VCORE_TSEN

GND

PR4676 NTC-100K-12-GP-U — B = 4250 — PR4664 1KR2F-L-GP — PWR_VCCGT_TSEN_A

PR4681 NTC-100K-12-GP-U — B = 4250 — PR4677 1KR2F-L-GP — PWR_VCORE_TSEN_A

PWR_VREF

PR4654 8K45R2F-2-GP — PWR_VCCGT_TSEN_B — PR4661 191R2F-GP — PR4670 180KR2F-4-L-GP — VCCGT_TSEN_C — PR4674 357R2F-GP

PR4655 8K25R2F-1-GP — PWR_VCORE_TSEN_B — PR4662 169R2F-GP — PR4671 560KR2F-GP — VCORE_TSEN_C — PR4675 768R2F-1-GP

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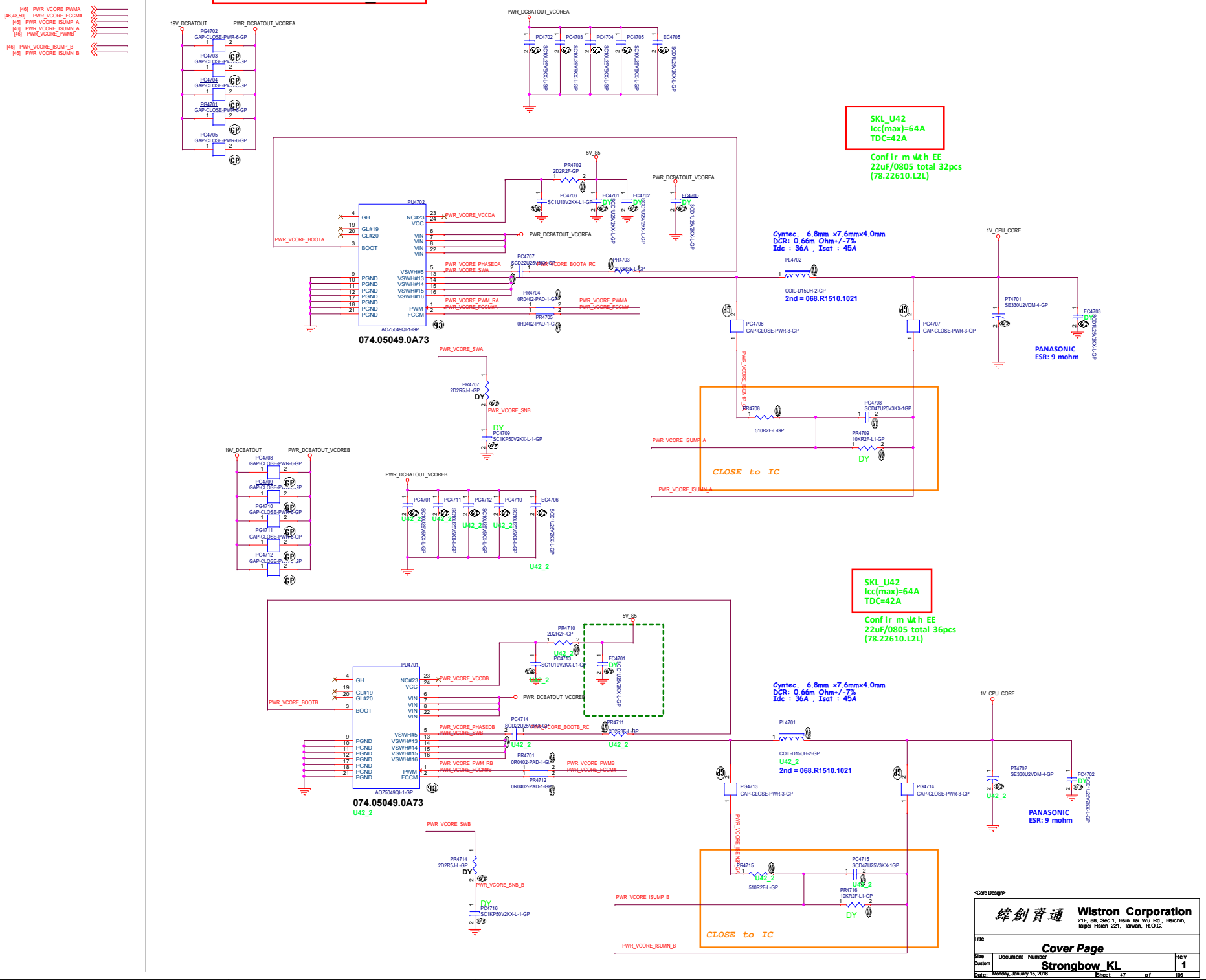

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Main Func = CPU_CORE

[46] PWR_VCCGT_PWM
[46,47,50] PWR_VCORE_FCCM#
[46] PWR_VCCGT_ISUMP
[46] PWR_VCCGT_ISUMN

19V_DCBATOUT
PWR_DCBATOUT_VCCGTA

PG4802 GAP-CLOSE-PWR-6-GP
PG4803 GAP-CLOSE-PWR-6-GP
PG4804 GAP-CLOSE-PWR-6-GP
PG4801 GAP-CLOSE-PWR-6-GP
PG4805 GAP-CLOSE-PWR-6-GP
PG4806 GAP-CLOSE-PWR-6-GP

PT4802 ST15U25VBM-GP
DY

PC4802 SC10U25V5KX-L-GP
PC4803 SC10U25V5KX-L-GP
PC4804 SC10U25V5KX-L-GP
PC4801 SC10U25V5KX-L-GP
EC4805 SCD1U25V2KX-L-GP

SKL_U42
Icc(max)=28A
TDC=12A

Confir m wit h EE
22uF/0805 total 26pcs
(78.22610.L2L)

PU4801
AOZ5049QI-1-GP
074.05049.0A73

GH
GL#19
GL#20
BOOT
NC#23
VCC
VIN
VSWH#5
VSWH#13
VSWH#14
VSWH#15
VSWH#16
PGND
PWM
FCCM

PWR_VCCGT_BOOT
PWR_VCCGT_VCC_R
PWR_VCCGT_PHASE
PWR_VCCGT_SW
PWR_VCCGT_PWM_R
PWR_VCCGT_FCCM#_R

PR4802 2D2R2F-GP
5V_S5
PC4805 SC1U10V2KX-L1-GP
EC4801 DY SCD1U25V2KX-L-GP
EC4802 DY SCD1U25V2KX-L-GP
FC4805 DY SCD1U25V2KX-L-GP
PR4803 2D2R3F-L-GP
PC4806 SCD22U25V3KX-GP
PWR_VCCGT_BOOT_RC
PR4804 0R0402-PAD-1-GP
PR4805 0R0402-PAD-1-GP
PWR_VCCGT_PWM
PWR_VCORE_FCCM#

Cyntec. 6.8mm x7.6mmx4.0mm
DCR: 0.66m Ohm+/-7%
Idc : 36A , Isat : 45A

PL4801
COIL-D15UH-2-GP
2nd = 068.R1510.1021

1V_VCCGT
PG4807 GAP-CLOSE-PWR-3-GP
PG4808 GAP-CLOSE-PWR-3-GP
FC4801 SCD1U25V2KX-L-GP
EC4803 SCD1U25V2KX-L-GP
PT4801 SE330U2VDM-4-GP
DY

PWR_VCCGT_SW
PR4808 2D2R5J-L-GP
DY
_VCCGT_SNB
DY
PC4808 SC1KP50V2KX-L-1-GP

PWR_VCCGT_ISEN
PR4807 590R2F-GP
PC4807 SCD47U25V3KX-1GP
PR4809 487R2F-GP
PR4810 10KR2F-L1-GP
PWR_VCCGT_ISUMP
CLOSE to IC
PR4801 NTC-10K-29-GP-U
B = 3370
PWR_VCCGT_ISUMN

<Core Design>

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***

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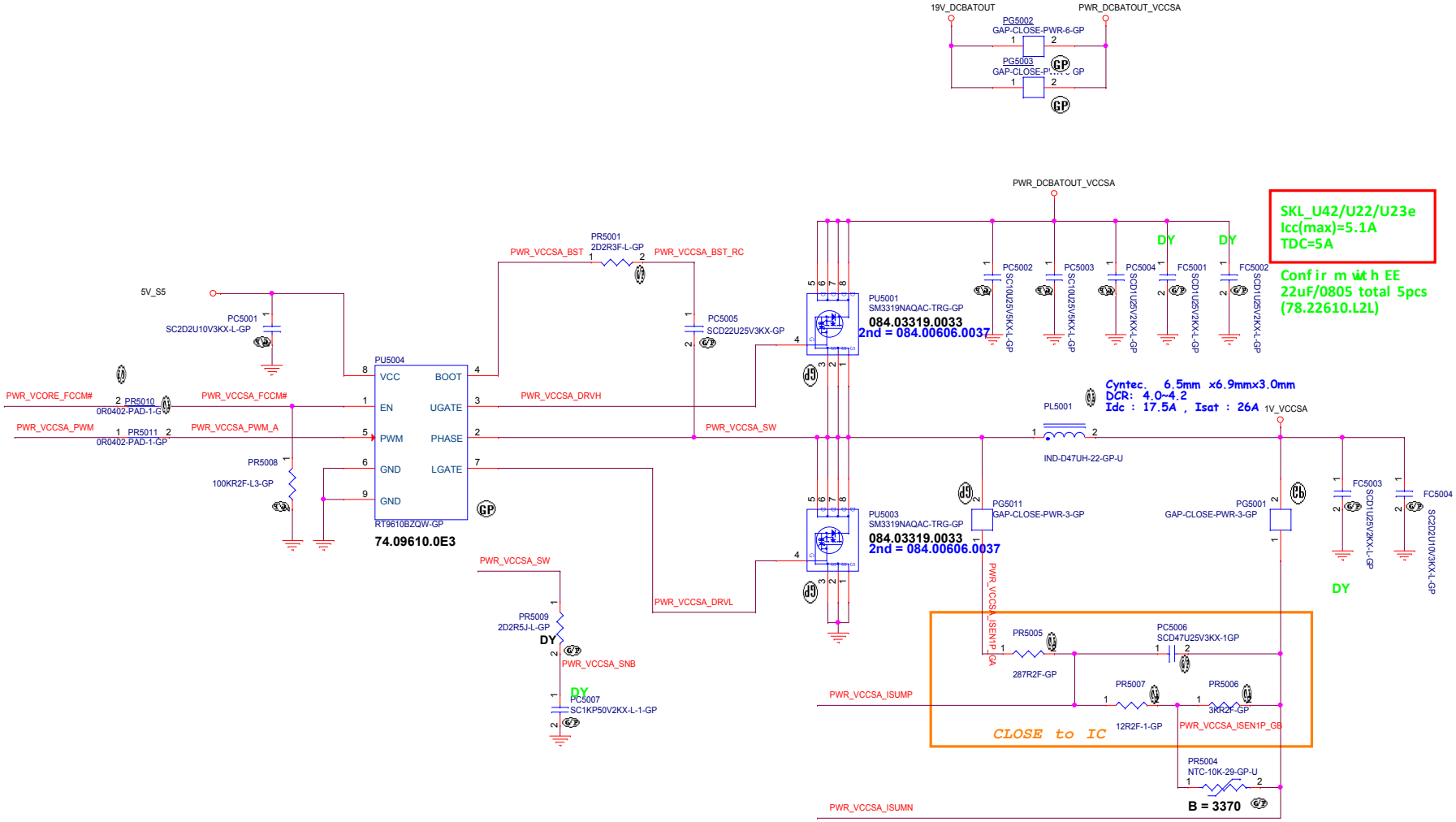
Main Func = CPU_CORE

[46,47,48] PWR_VCORE_FCCM#
[46] PWR_VCCSA_PWM
[46] PWR_VCCSA_ISUMP
[46] PWR_VCCSA_ISUMN



<Core Design>

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VDDQ ENABLE CONTROL

[4] VTT_CNTL_CPU

2D5V ENABLE CONTROL

[20,24,40] PM_SLP_S4#

[40] PWR_VDDQ_PG

19V_DCBATOUT

PWR_DCBATOUT_VDDQ

PG5101 GAP-CLOSE-PWR-6-GP

PG5102 GAP-CLOSE-PWR-6-GP

PG5103 GAP-CLOSE-PWR-6-GP

PWR_VDDQ

1D2V_S3

PG5105 GAP-CLOSE-PWR-6-GP

PG5106 GAP-CLOSE-PWR-6-GP

PG5107 GAP-CLOSE-PWR-6-GP

PG5108 GAP-CLOSE-PWR-6-GP

PG5109 GAP-CLOSE-PWR-6-GP

PG5110 GAP-CLOSE-PWR-6-GP

PG5112 GAP-CLOSE-PWR-6-GP

PG5114 GAP-CLOSE-PWR-6-GP

PG5118 GAP-CLOSE-PWR-6-GP

5V_S5

PR5101 10R2F-L1-GP

PWR_VDDQ_VCC

EC5102 SCD1U25V2KX-L-GP

EC5101 SCD1U25V2KX-L-GP

PC5102 SC10U25V5KX-L-GP

PC5104 SC1U10V2KX-L1-GP

PR5102 12KR2F-L-GP

PWR_VDDQ_CS

3D3V_S5

PR5152 10KR2F-L1-GP

PR5108 = 510K
Fs = 400~550KHz

PWR_VDDQ_PG

PWR_DCBATOUT_VDDQ

PR5108 510KR2F-GP

PWR_VDDQ_TON

2D5V_S3_PWRGD

VTT_CNTL_CPU

PU5101

CS

VCC

PGOOD

TON

S5

S3

VLDOIN

VTTGND

VTTGND

VTTGND

VTT

VTTSNS

NC#26

GND

VTTREF

G5388K11U-GP

074.05388.0043

PWR_VDDQ_VTTREF

PC5114 SCD1U25V2KX-L-GP

PWR_VDDQ_VTT

PC5111

PC5112 SC10U6D3V3MX-L-GP

SC10U6D3V3MX-L-GP

0D6V_VREF_S0

PG5111 GAP-CLOSE-PWR-6-GP

PG5113 GAP-CLOSE-PWR-6-GP

PWR_VDDQ_LVOIN

PC5103 SC1U10V2KX-L1-GP

PG5115 GAP-CLOSE-PWR-6-GP

PG5119 GAP-CLOSE-PWR-6-GP

PWR_VDDQ_BST

PR5112

0R0805-PAD

PC5110 SCD1U25V2KX-L-GP

PWR_VDDQ_BOOTA

LX#25

LX#17

LX#18

LX#19

LX#20

LX#35

PWR_VDDQ_PH

PL5101 COIL-1UH-34-GP-U1

Cyntec. 6.5 x 6.9 x 3.0mm
DCR: 9~10mOhm
Idc : 11A , Isat : 22A

2nd = 68.1R01E.10C

PGND

VDDQSNS

VDDQSET

PWR_VDDQ_VDDQ

PWR_VDDQ_FB

PR5105 6K2R2F-GP

PR5106 10K2R2F-GP

PG5104 GAP-CLOSE-PWR-6-GP

PC5106 SC221U6D3V6MX-L1-GP

PC5107 SC221U6D3V6MX-L1-GP

PC5109 SC221U6D3V6MX-L1-GP

PC5121 SC221U6D3V6MX-L1-GP

PC5113 SC221U6D3V6MX-L1-GP

EC5103 SCD1U25V2KX-L-GP

EC5104 SCD1U25V2KX-L-GP

PC5108 SCD1U25V2KX-L-GP

PC5101 SC10U25V5KX-L-GP

PC5122 SC10U25V5KX-L-GP

FC5102 SCD1U25V2KX-L-GP

PD5101 AZ4024-01L-R7G-GP

FC5106 SCD1U25V2KX-L-GP

TDC : 8.0A

Vout= 0.75*(1+R1/R2) = 1.2

V2D5_S5
MAX=1A

Pd=(3.3-2.5)*1=0.8W

2D5V_S3

PG5116 GAP-CLOSE-PWR-6-GP

PG5117 GAP-CLOSE-PWR-6-GP

PWR_2D5V_S3

PC5116 SC10U6D3V3MX-L-GP

PC5115 SC10U6D3V3MX-L-GP

PC5117 SC100P50V2JN-L-GP

2D5V_SS_FB

PU5102

NC#1

VO#2

VO#3

ADJ

POK

VPP

NC#9

VIN

VIN

VEN

GND

G9661-25ADJRE1U-GP

PWR_2D5V_EN

PC5119 SC1U50V3KX-GP

PC5120 SCD1U25V2KX-L-GP

PR5125 0R0402-PAD-1-GP

PM_SLP_S4#

3D3V_S5

SC10U6D3V3MX-L-GP PC5118

PR5111 100KR2J-4-GP

2D5V_PWR_GOOD

PWR_2D5V_PG

FC5107 SCD1U25V2KX-L-GP

PR5115 21.5K_1% 0402

R1

PR5110 10KR2F-L-1-GP

R2

0R0402-PAD-1-GP

2D5V_SS_PWRGD

PR5113

PWR_2D5V_PG

FC5109 SCD1U25V2KX-L-GP

Vout = 0.8*(1+R1/R2)=2.52V

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Title: DCDC APW8861_VDDQ DDR4

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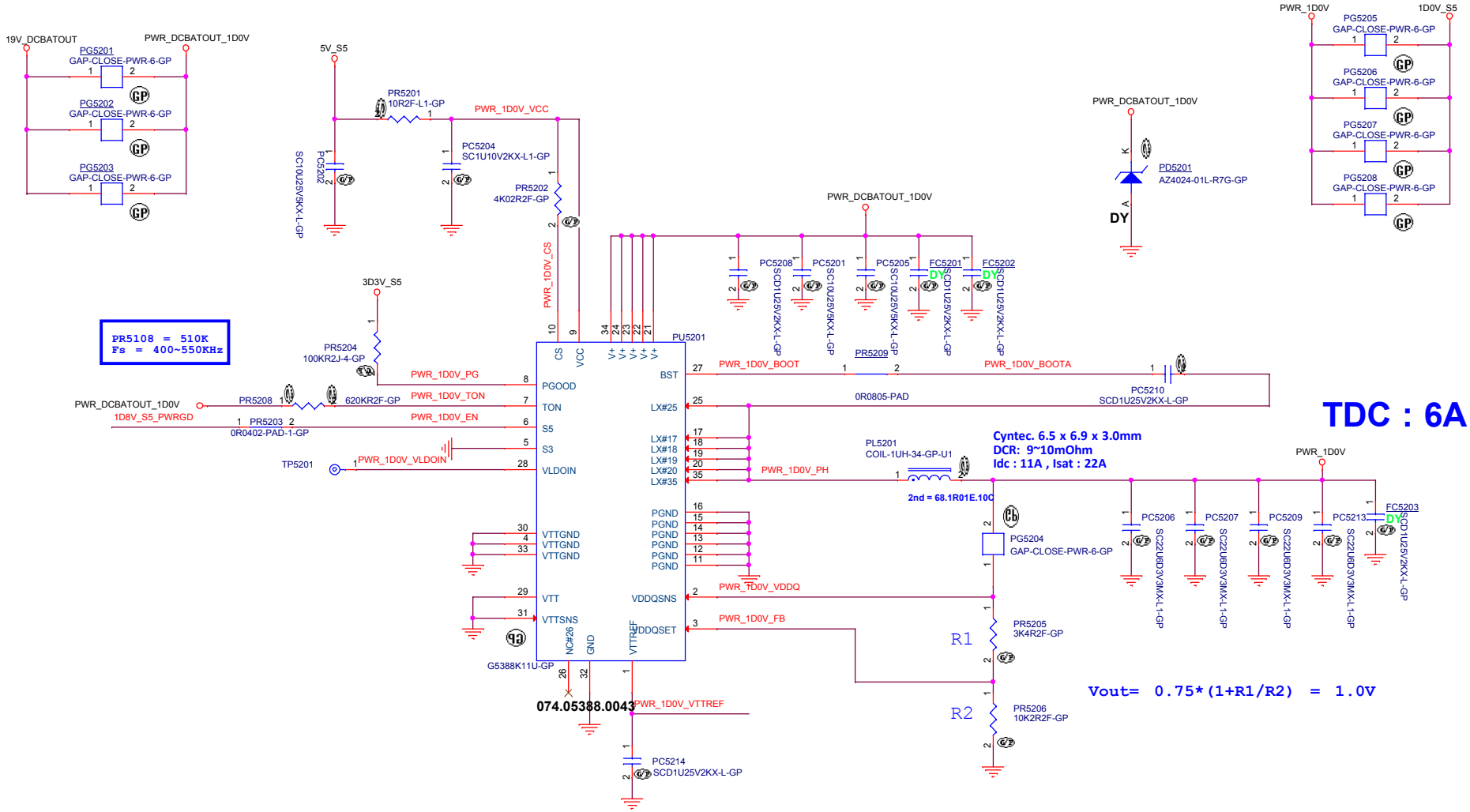
1D0V ENABLE CONTROL

[53] 1D8V_S5_PWRGD



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	RT8237_1D0V_S5	
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1D8V_S5

1D8V_S5 POWER GOOD

[52] 1D8V_S5_PWRGD

[20,45] 3V_5V_POK

[0,24,40,58] PM_SLP_S3#

PD = (Vin_Vout) x Iout
= (3.3 - 1.8) x 0.3A = 0.45W
PD de-rating(%) = 0.45W/1.33W = 33.8%

1125 Simon
Vendor suggest to replace 74.09025.A3D by 74.09025.D3D

5V_S5
PR5302 2D2R2F-GP
PC5302 SC1U10V2KX-L1-GP
PU5301
PWR_1D8V_S5_VDD
PWR_1D8V_S5_PVDD
PWR_1D8V_S5_EN
VPP NC#9 VIN VIN VEN GND
NC#1 VO#2 VO#3 ADJ POK
PWR_1D8V_S5_FB
1D8V_S5_PWRGD
G9661-25ADJRE1U-GP

3D3V_S5
PG5301 GAP-CLOSE-PWR-6-GP
PG5302 GAP-CLOSE-PWR-3-GP
PC5303 SC10U6D3V3MX-L-GP
DY PC5304 SC10U6D3V3MX-L-GP
FC5301 DY SCD1U25V2KX-L-GP
3V_5V_POK
PR5301 0R0402-PAD-1-GP
PWR_1D8V_S5_EN
PC5307 SC1U10V2KX-L1-GP DY

R1 PR5303 12K7R2F-GP
PC5305 SC22P50V2JN-L-GP
PWR_1D8V_S5_FB
R2 PR5304 10KR2F-L1-GP

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

DY PC5306 SC10U6D3V3MX-L-GP
PC5301 SC10U6D3V3MX-L-GP
PWR_1D8V
PG5303 GAP-CLOSE-PWR-6-GP
PG5304 GAP-CLOSE-PWR-3-GP
1D8V_S5
FC5310 DY SCD1U25V2KX-L-GP

3D3V_S5
PR5305 10KR2F-L1-GP
1D8V_S5_PWRGD

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: RT5797_1D8V
Size: Custom | Document Number | Rev
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
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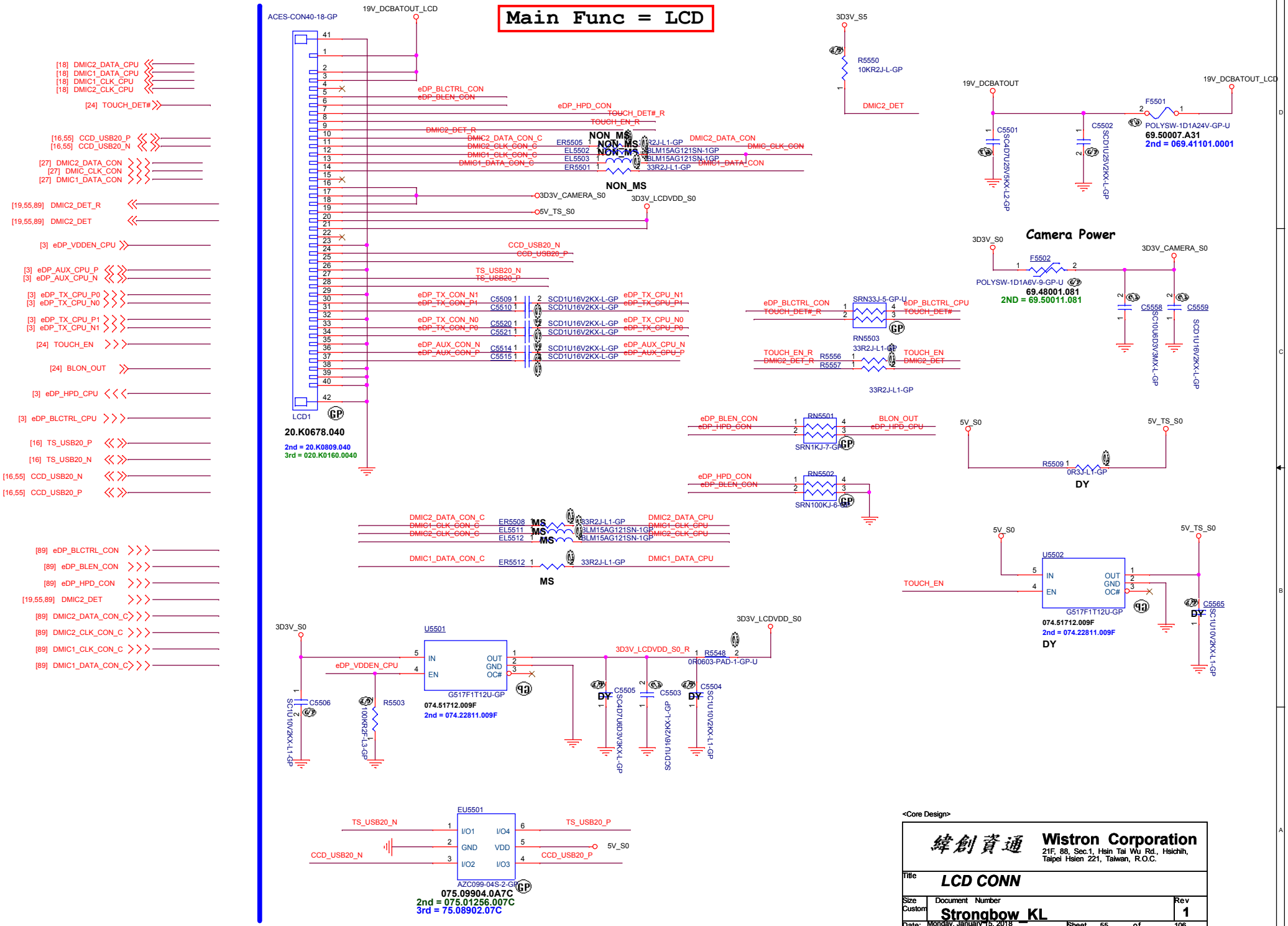
Main Func = LCD



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size: Custom	Document Number: Strongbow_KL	Rev: 1
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<Core Design>

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Title		
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SSID = VIDEO

HDMI 1.4 & CONNECTOR

HDMI CONN

[3] HDMI_DDI_TX_P0
[3] HDMI_DDI_TX_N0
[3] HDMI_DDI_TX_P1
[3] HDMI_DDI_TX_N1
[3] HDMI_DDI_TX_P2
[3] HDMI_DDI_TX_N2
[3] HDMI_DDI_TX_P3
[3] HDMI_DDI_TX_N3
[3,15] HDMI_SCL_CPU
[3,15] HDMI_SDA_CPU
[3] HDMI_DET_CPU
[89] HDMI_DDI_TX_CON_N3
[89] HDMI_DDI_TX_CON_P3
[89] HDMI_DDI_TX_CON_P0
[89] HDMI_DDI_TX_CON_N0
[89] HDMI_DDI_TX_CON_P1
[89] HDMI_DDI_TX_CON_N1
[89] HDMI_DDI_TX_CON_P2
[89] HDMI_DDI_TX_CON_N2
[89] HDMI_SCL_CON
[89] HDMI_SDA_CON
[89] HDMI_DET_CON

3D3V_S0 4K7R2J-L-GP DY R5701 PS8201_EN
3D3V_S0 4K7R2J-L-GP LS R5703 PS8201_DDCBUF
4K7R2J-L-GP DY R5705
3D3V_S0 4K7R2J-L-GP DY R5710 PS8201_PRE
4K7R2J-L-GP DY R5711
3D3V_S0 4K7R2J-L-GP LS R5702 PS8201_CFG
3D3V_S0 4K7R2J-L-GP LS R5704 PS8201_EQ
4K7R2J-L-GP DY R5706
3D3V_S0 4K7R2J-L-GP DY R5707 PS8201_ISET
4K7R2J-L-GP DY R5708

ER5701 150R2J-L1-GP-U HDMI_DDI_TX_CON_N3
ER5702 150R2J-L1-GP-U HDMI_DDI_TX_CON_P3
ER5703 150R2J-L1-GP-U HDMI_DDI_TX_CON_N4
ER5704 150R2J-L1-GP-U HDMI_DDI_TX_CON_P4

5V_HDMI_S0
D5701 BAW56-9-GP
75.00056.07D
2nd = 83.00056.Y11
3rd = 75.00056.B7D
5V_DDC_HDMI1
5V_DDC_HDMI2
RN5701 SRN2K2J-5-GP
HDMI_SCL_CON
HDMI_SDA_CON

5V_HDMI_S0
F5701 POLYSW-1608V-9-GP-U
5V_S0
C5709 SCD1U16V2KX-L-GP
69.48001.081
2ND = 69.50011.081

U5701
3D3V_S0 VDD33
1D5V_S0 VDD15 VDD15 VDD15 VDD15
HDMI_DDI_TX_P0 C5723 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_P0 IN_D0P
HDMI_DDI_TX_N0 C5711 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_N0 IN_D0N
HDMI_DDI_TX_P1 C5710 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_P1 IN_D1P
HDMI_DDI_TX_N1 C5712 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_N1 IN_D1N
HDMI_DDI_TX_P2 C5714 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_P2 IN_D2P
HDMI_DDI_TX_N2 C5713 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_N2 IN_D2N
HDMI_DDI_TX_P3 C5716 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_P3 IN_CKP
HDMI_DDI_TX_N3 C5715 LS SCD1U16V2KX-L-GP HDMI_DDI_CMC_N3 IN_CKN
PS8201_EN
PS8201_DDCBUF DCIN_EN/SCL_CTL DDCBUF/SDA_CTL
PS8201_EQ
PS8201_CFG EQ/I2C_ADDR CFG
PS8201_REXT REXT
R5718 4K02R2F-GP LS
1D5V_S0 NC#12
3D3V_S0 PS8201_ISET NC#15 NC#37 NC#34
OUT_CKN HDMI_DDI_TX_CON_N3
OUT_CKP HDMI_DDI_TX_CON_P3
OUT_D0P HDMI_DDI_TX_CON_P0
OUT_D0N HDMI_DDI_TX_CON_N0
OUT_D1P HDMI_DDI_TX_CON_P1
OUT_D1N HDMI_DDI_TX_CON_N1
OUT_D2P HDMI_DDI_TX_CON_P2
OUT_D2N HDMI_DDI_TX_CON_N2
SCL_SNK HDMI_SCL_CON
SDA_SNK HDMI_SDA_CON
HPD_SNK HDMI_DET_CON
SCL_SRC HDMI_SCL_CPU
SDA_SRC HDMI_SDA_CPU
HPD_SRC HDMI_DET_CPU
I2C_CTL_EN
PRE PS8201_PRE
PD# PS8201_PD#
GND GND
PS8201ATQFN40GTR2-A0-GP
71.08201.G03
LS
R5716 DY 4K7R2J-L-GP 3D3V_S0
R5719 0R0402-PAD-1-GP
R5717 DY 4K7R2J-L-GP 3D3V_S0

HDMI1
5V_HDMI_S0 +5V_POWER
HDMI_SCL_CON SCL
HDMI_SDA_CON SDA
HDMI_DDI_TX_CON_P0 TMDS_DATA0+
HDMI_DDI_TX_CON_N0 TMDS_DATA0-
HDMI_DDI_TX_CON_P1 TMDS_DATA1+
HDMI_DDI_TX_CON_N1 TMDS_DATA1-
HDMI_DDI_TX_CON_P2 TMDS_DATA2+
HDMI_DDI_TX_CON_N2 TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
HDMI_DDI_TX_CON_P3 TMDS_CLOCK_SHIELD
HDMI_DDI_TX_CON_N3 TMDS_CLOCK+
TMDS_CLOCK-
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND GND GND GND
HDMI_DET_CON
R5785 100KR2J-4-GP DY
SKT-HDMI23-187-GP-U

3D3V_S0 C5701 SCD01U50V2KX-L-GP LS
3D3V_S0 C5702 SCD01U50V2KX-L-GP LS
1D5V_S0 C5703 SCD01U16V2KX-L-GP LS
C5704 SCD01U16V2KX-L-GP LS
C5705 SCD01U16V2KX-L-GP LS
1D5V_S0 C5706 SCD01U50V2KX-L-GP LS
C5707 SCD01U50V2KX-L-GP LS
C5708 SCD01U50V2KX-L-GP LS

EMI Request:

HDMI_DDI_TX_CON_N0 HDMI_DDI_TX_CON_P0 ED5701 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.PUSB3.0073
HDMI_DDI_TX_CON_P3 HDMI_DDI_TX_CON_P3 DY

HDMI_DDI_TX_CON_N2 HDMI_DDI_TX_CON_P2 ED5702 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.PUSB3.0073
HDMI_DDI_TX_CON_N1 HDMI_DDI_TX_CON_P1 DY

HDMI_SCL_CON HDMI_SDA_CON
HDMI_DET_CON
EU5701 I/O1 I/O4 I/O2 I/O3 GND VDD
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.08902.07C
DY
5V_HDMI_S0

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
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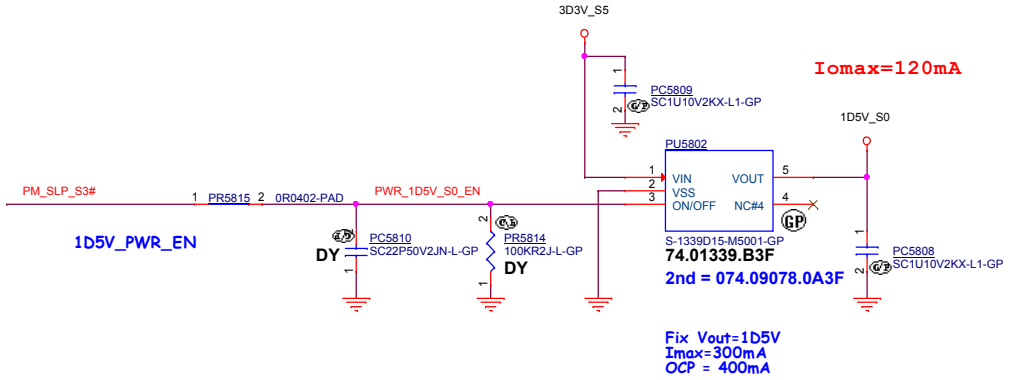
[20,24,40] PM_SLP_S3#



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Power		
Size: A3	Document Number: Strongbow_KL	Rev: 1
Date: Monday, January 15, 2018	Sheet 58 of 106	

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<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

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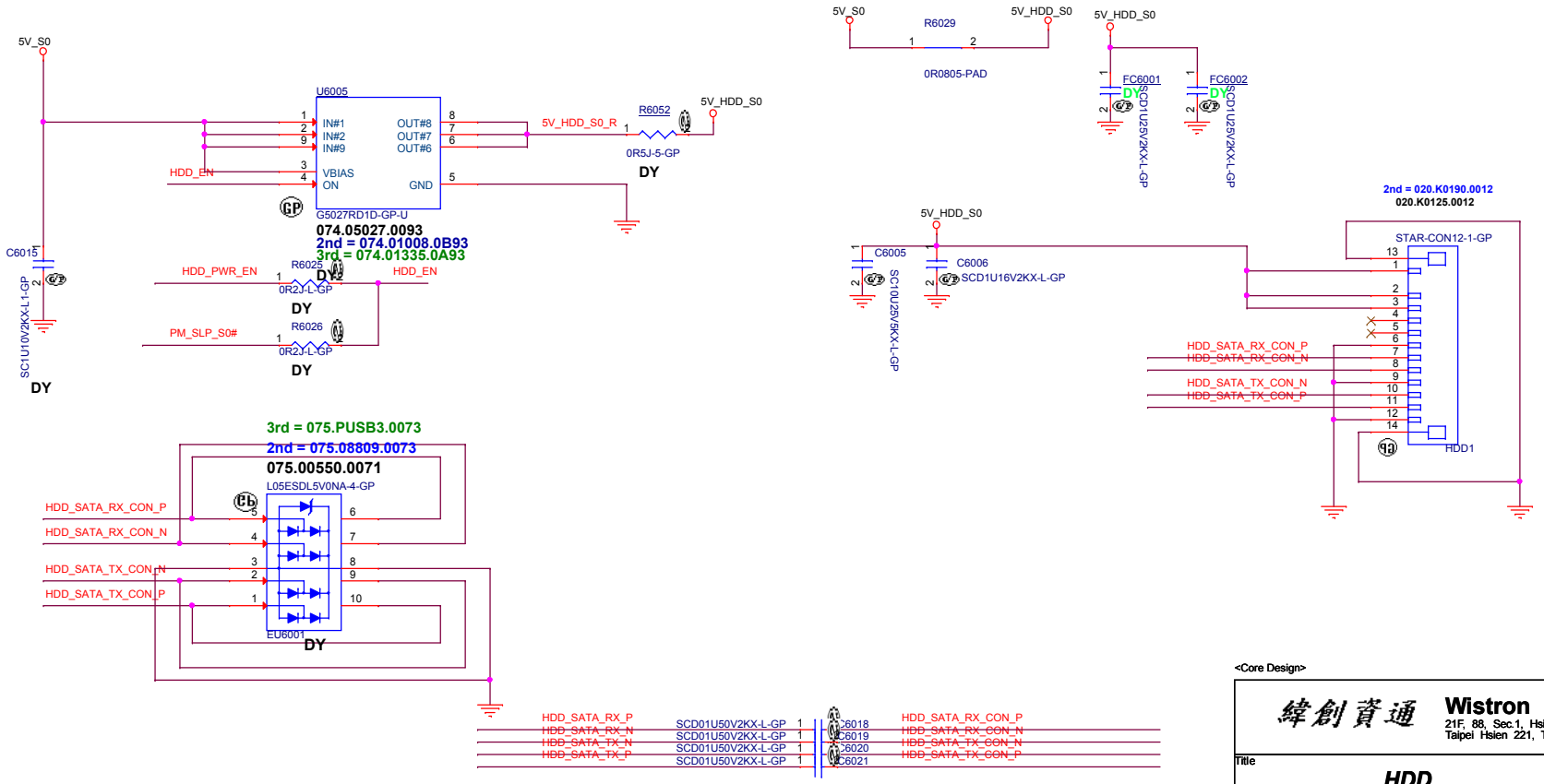
HDD_SATA_RX_P [16]
HDD_SATA_RX_N [16]
HDD_SATA_TX_N [16]
HDD_SATA_TX_P [16]
PM_SLP_S3# [20,24,40,58]
PM_SLP_S0# [20,24,40,91]
HDD_PWR_EN [6]

SSID = SATA

SATA HDD Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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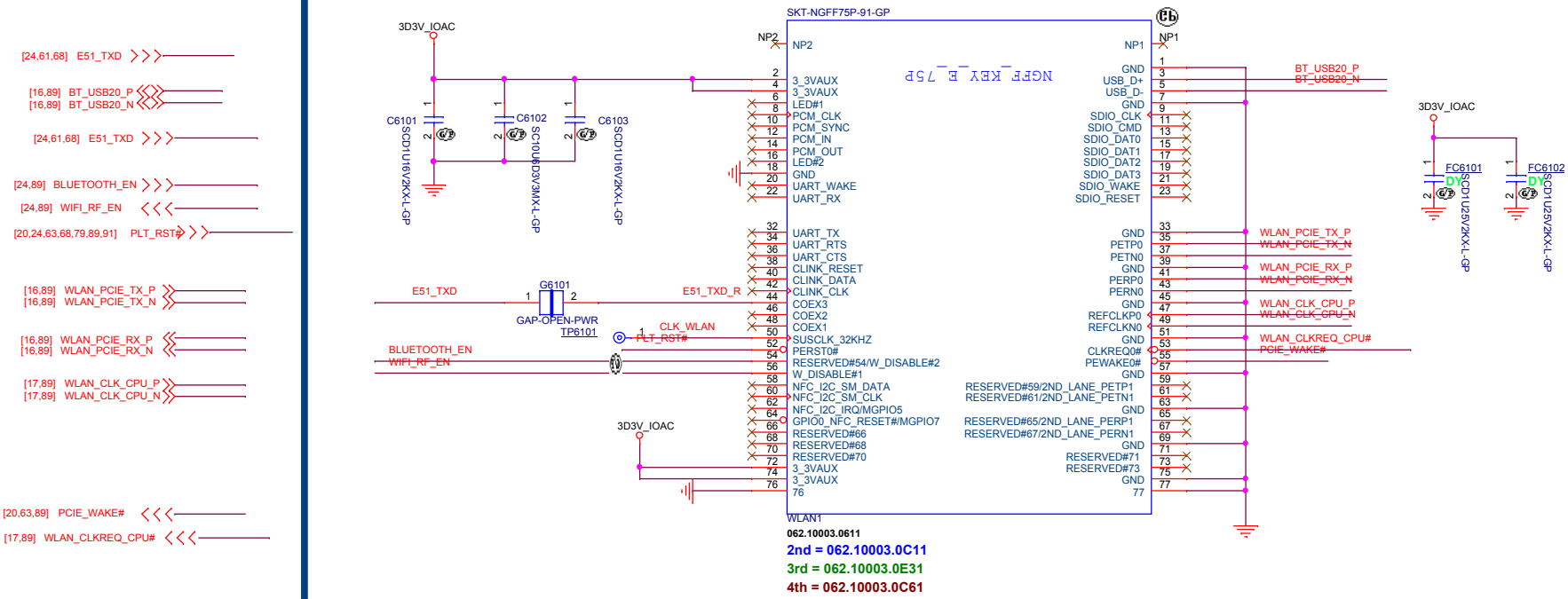
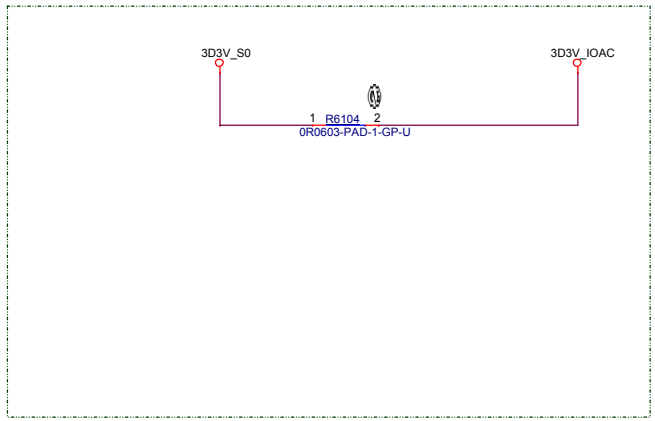
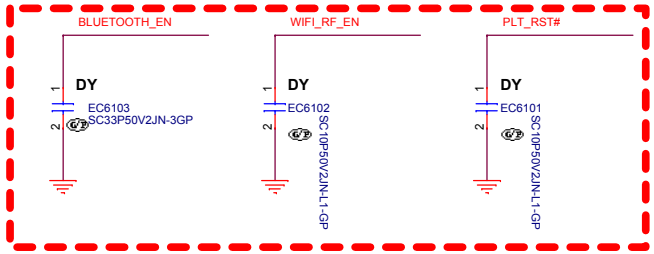
SSID = Wireless Mini Card Connector(802.11a/b/g/n)







[24,61,68] E51_TXD
[16,89] BT_USB20_P
[16,89] BT_USB20_N
[24,61,68] E51_TXD
[24,89] BLUETOOTH_EN
[24,89] WIFI_RF_EN
[20,24,63,68,79,89,91] PLT_RST#
[16,89] WLAN_PCIE_TX_P
[16,89] WLAN_PCIE_TX_N
[16,89] WLAN_PCIE_RX_P
[16,89] WLAN_PCIE_RX_N
[17,89] WLAN_CLK_CPU_P
[17,89] WLAN_CLK_CPU_N
[20,63,89] PCIE_WAKE#
[17,89] WLAN_CLKREQ_CPU#

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Title: Mini Card-WLAN

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 61 of 106

<Core Design>

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Title: ***(Reserved)WWAN***

Size	Document Number	Rev
Custom	Strongbow_KL	1
Date: Thursday, January 11, 2018	Sheet 62 of 106	

SSID = mSATA

Mini Card Connector(mSATA)

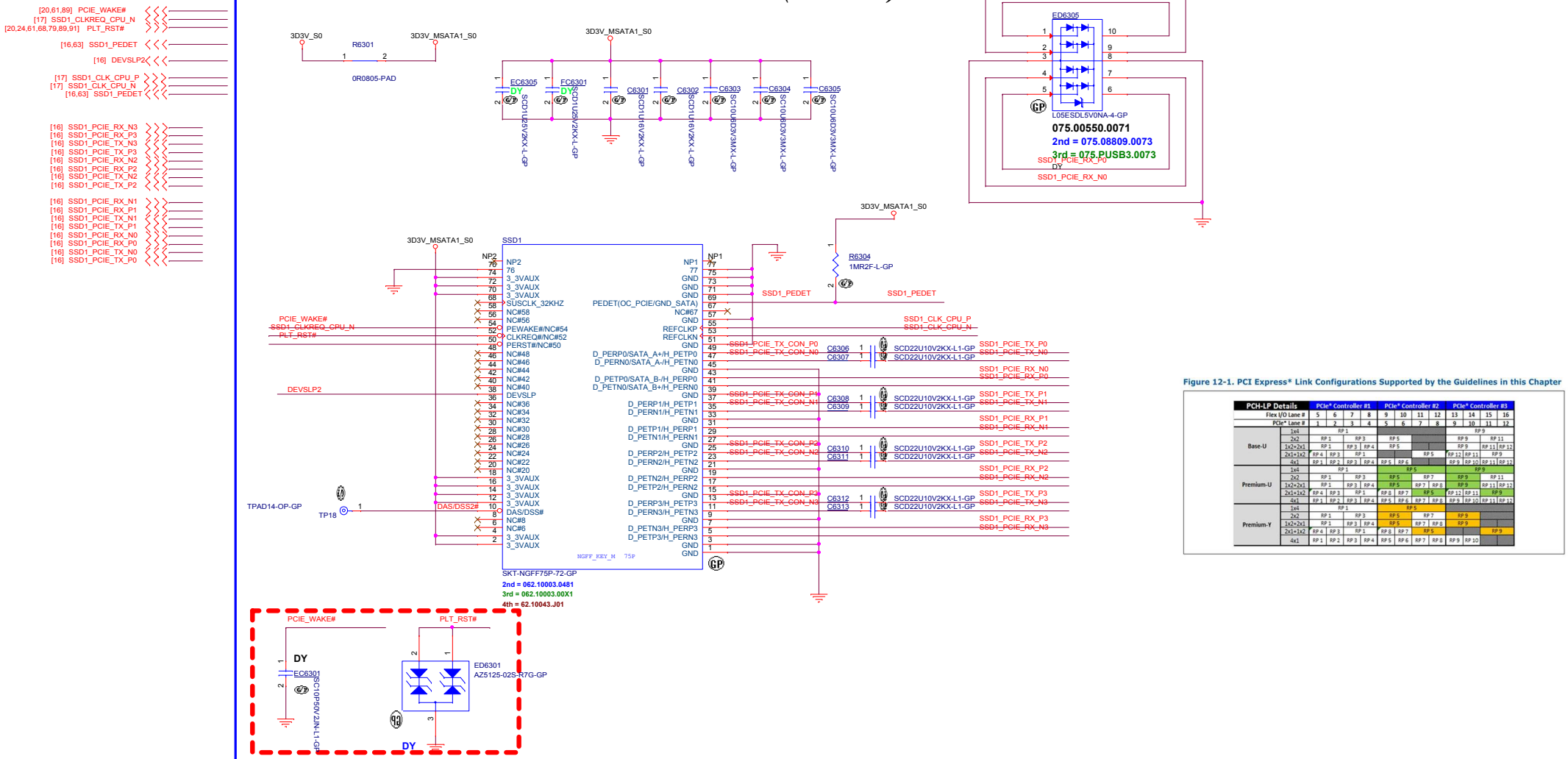

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1				RP 9							
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1				RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12
Premium-Y	1x4	RP 1				RP 5							
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9			
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9			
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5				RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10		

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

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Title: SSD-NGFF-1

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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Title: ***LED Bard/Power Button***

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SSID = KBC

[24,89] KSI[0..7]
[24,89] KSO[0..17]
[24] EC_TPCLK
[24] EC_TPDATA
[24,89] FUN_OFF#
[89] EC_TP_CLK_C
[89] EC_TP_DATA_C
[89] I2C1_DATA_TP
[89] I2C1_CLK_TP
[24] PTP_PWR_EN
[22] TP_IN#
[24,89] EC_TP_IN#
[24,89] EC_TP_IN_R#
[6] PM_TP_CLK
[6] PM_TP_DATA
[24] KB_BL_PWM
[24] KB_BL_DET
[89] KB_BL_DET_R
[89] KB_LED_PWM_R
[24,64,89] KBC_PWRBTN#

3D3V_TP_S3
3D3V_S0
RN6505
SRN2K2J-5-GP
PM_TP_CLK
PM_TP_DATA
I2C1_CLK_TP
I2C1_DATA_TP
Q6503
75.27002.E7C
2nd = 075.67002.007C
3rd = 075.27002.0E7C
EC6504
EC6505
DY
SCD1U16V2KX-L-GP

3D3V_TP_S3
3D3V_S0
R6506
100KR2F-L3-GP
Q6502
TP_IN#
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.27002.0N31
EC_TP_IN#
R6518
33R2J-L-GP
EC_TP_IN_R#
EC6507
DY
SCD1U16V2KX-L-GP

3D3V_S5
U6502
IN
EN
OUT
GND
OC#
G517F1T12U-GP
074.51712.009F
2nd = 074.22811.009F
PTP_PWR_EN
C6509
SC4D7U6D3V3KX-L-GP
3D3V_TP_S3_R
R6558
0R0603-PAD-1-GP-U
3D3V_TP_S3
C6504
SC4D7U6D3V3KX-L-GP

TOUCH PAD

3D3V_TP_S3
RN6503
SRN4K7J-8-GP
RN6502
SRN33J-5-GP-U
EC_TPCLK
EC_TPDATA
FUN_OFF#
EC6502
SC22P50V2JN-L-GP
DY
EC_TP_CLK_C
EC_TP_DATA_C
I2C1_DATA_TP
I2C1_CLK_TP
EC_TP_IN_R#
EC6501
EC6503
SC22P50V2JN-3GP
TP1
STARCON8-2-GP
020.K0182.0008
2nd = 020.K0243.0008

Internal KeyBoard Connector

KB1
ACES-CON28-10-GP
020.K0173.0028
2nd = 020.K0266.0028
KBC_PWRBTN#

PTWO-CON6-16-GP
KBBL1
KB_BL_DET_R
KB_LED_PWM_R
R6504
100KR2F-L3-GP
KB_BL_DET
R6502
200KR2F-L-3-GP
KB_BL
5V_S0
C6501
SCD1U16V2KX-L-GP
DY
KB_BL
Q6501
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.27002.0N31
KB_BL_PWM

Circuit Diagram

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Title: Key Board/Touch Pad
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[24,66,89] STDBY_LED
[24,66,89] POWER_LED
[24,66,89] CHARGE_LED
[24,66,89] DC_BATFULL
[24,66,89] LID_CLOSE#
[43,66,89] BI_RST
[16,89] USB4_USB20_N
[16,89] USB4_USB20_P
[16,89] CR_USB20_N
[16,89] CR_USB20_P
[24,35] USB_PWR_EN
[16,89] FP_USB20_N
[16,89] FP_USB20_P
3D3V_CR_S0
3D3V_AUX_S5
[24,66,89] STDBY_LED
[24,66,89] POWER_LED
[24,66,89] DC_BATFULL
[24,66,89] CHARGE_LED
5V_AUX_S5
5V_USB20
5V_S5
[24,66,89] LID_CLOSE#

SSID = User.Interface

Close connector

High Active 2A

5V_S5 — C6608 SC1U10V2KX-L1-GP — U6601 G517F1T12U-GP (IN, EN, OUT, GND, OC#) — USB_PWR_EN — 5V_USB20 — C6609 SCD1U16V2KX-L-GP

074.51712.009F
2nd = 074.22811.009F

EU6602 AZC099-04S-2-GP
USB4_USB20_N, CR_USB20_N, 5V_USB20, USB4_USB20_P, CR_USB20_P

075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.08902.07C

EU6603 AZC099-04S-2-GP
FP_USB20_P, FP_USB20_N, 5V_S5

075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.08902.07C

3D3V_S0 — R6648 0R0805-PAD — 3D3V_CR_S0

5V_S0 — R6649 0R0805-PAD — 5V_FP_S0

ACES-CON30-20-GP-U

USB4_USB20_P
USB4_USB20_N
CR_USB20_P
CR_USB20_N
FP_USB20_N
FP_USB20_P
BI_RST
LID_CLOSE#
CHARGE_LED
DC_BATFULL
POWER_LED
STDBY_LED
3D3V_CR_S0
5V_FP_S0
3D3V_AUX_S5
5V_AUX_S5
5V_S5
5V_USB20
IOBD1

20.K0848.030
2nd = 020.K0190.0030
3rd = 20.K0809.030

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[19,24,91] INT_SERIRQ
[19] LPC_CLK_DBG

[20,24,61,63,79,89,91] PLT_RST#
[19,24,91] LPC_FRAME#_CPU

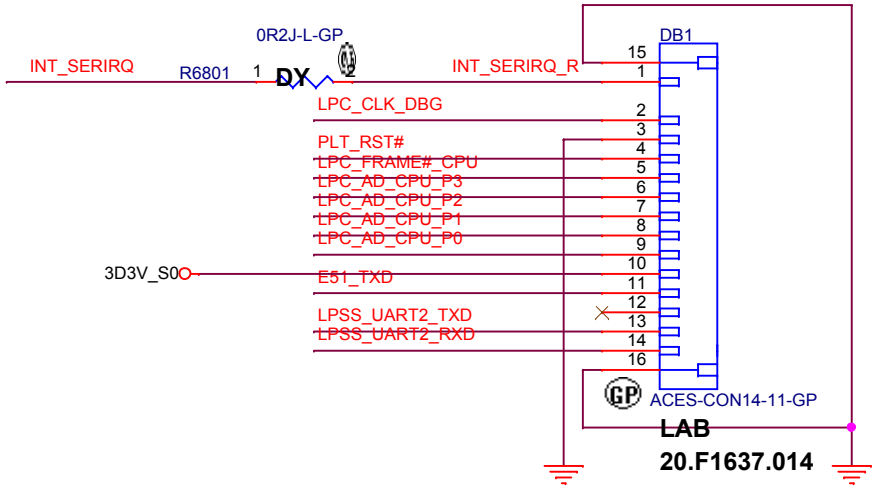
[19,24,91] LPC_AD_CPU_P3
[19,24,91] LPC_AD_CPU_P2

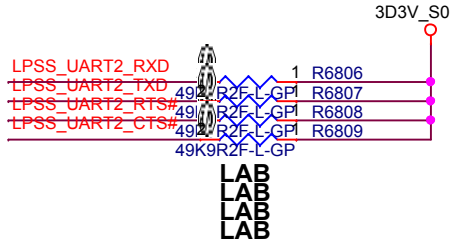
[19,24,91] LPC_AD_CPU_P1
[19,24,91] LPC_AD_CPU_P0

[24,61] E51_TXD

[6,68] LPSS_UART2_TXD
[6,68] LPSS_UART2_RXD

[6,68] LPSS_UART2_RXD
[6,68] LPSS_UART2_TXD
[6] LPSS_UART2_RTS#
[6] LPSS_UART2_CTS#





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Title: ***Dubug connector***

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SSID = User.Interface

G Sensor

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Title: G SENSOR

Size	Document Number	Rev
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Title: *Thunderbolt (4/5)*

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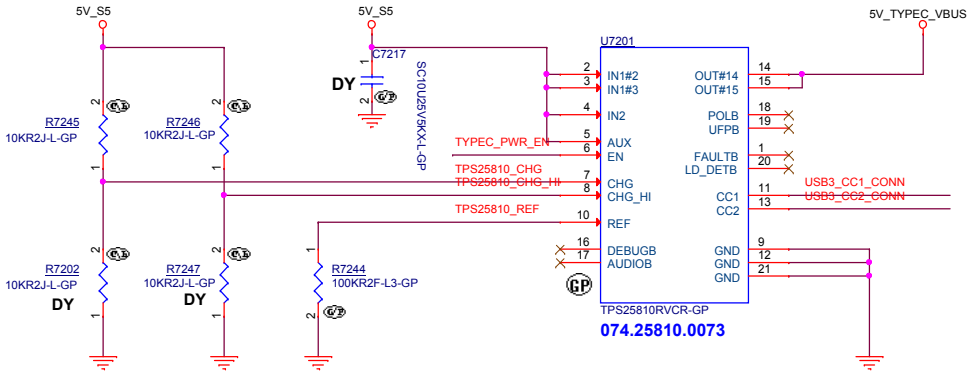
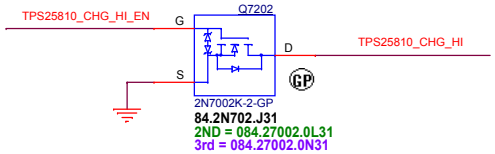
[24] TPS25810_CHG_HI_EN

[24] TYPEC_PWR_EN

[73,89] USB3_CC1_CONN
[73,89] USB3_CC2_CONN





CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

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Type_C CC

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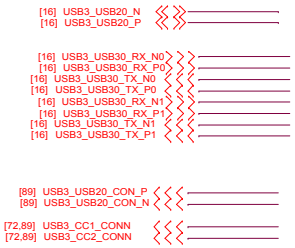
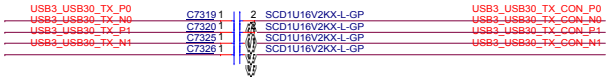
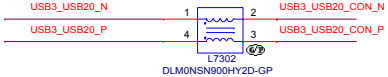
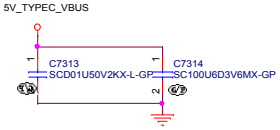
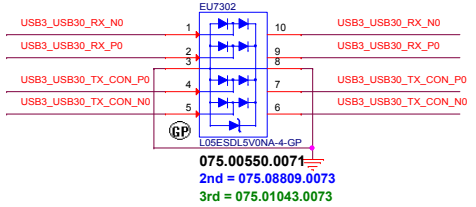
USB HOST

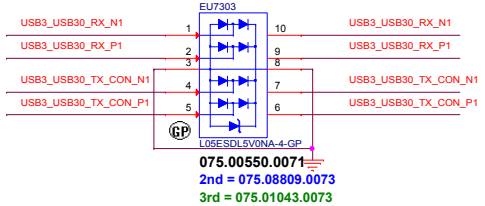


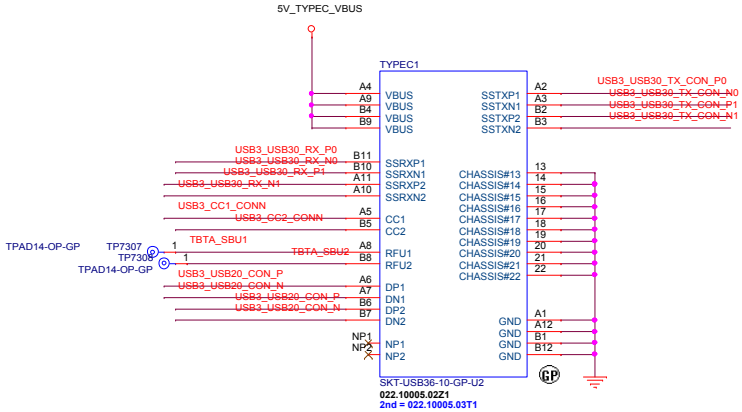


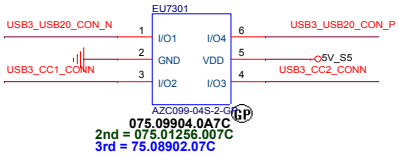












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Title

GPU (DIGITALOUT)

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Title: GPU (VRAM I/F)

Size: A4 | Document Number: Strongbow_KL | Rev: 1

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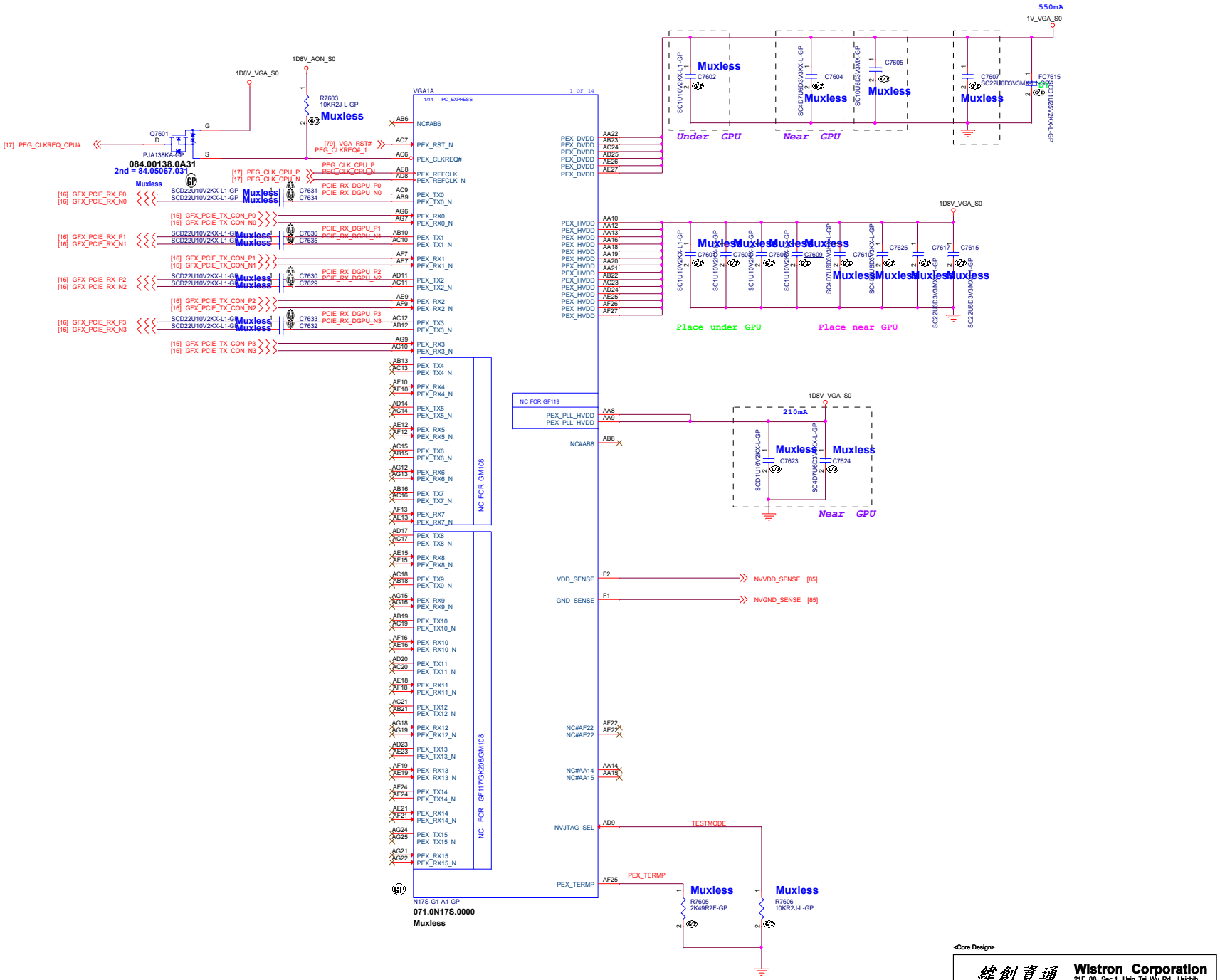

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Title: GPU(1/5) PEG

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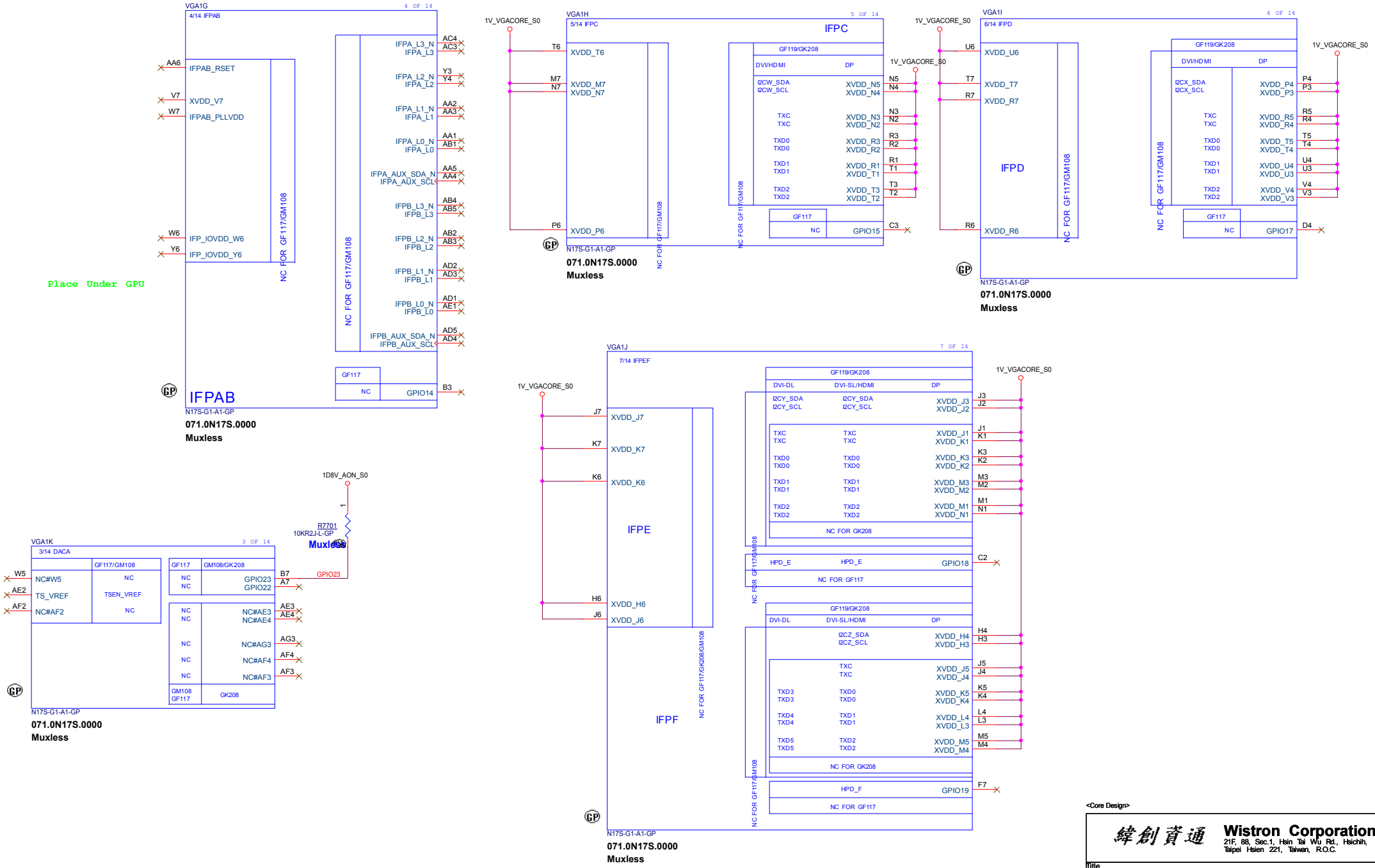

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Title: GPU (2/5) DIGITALOUT

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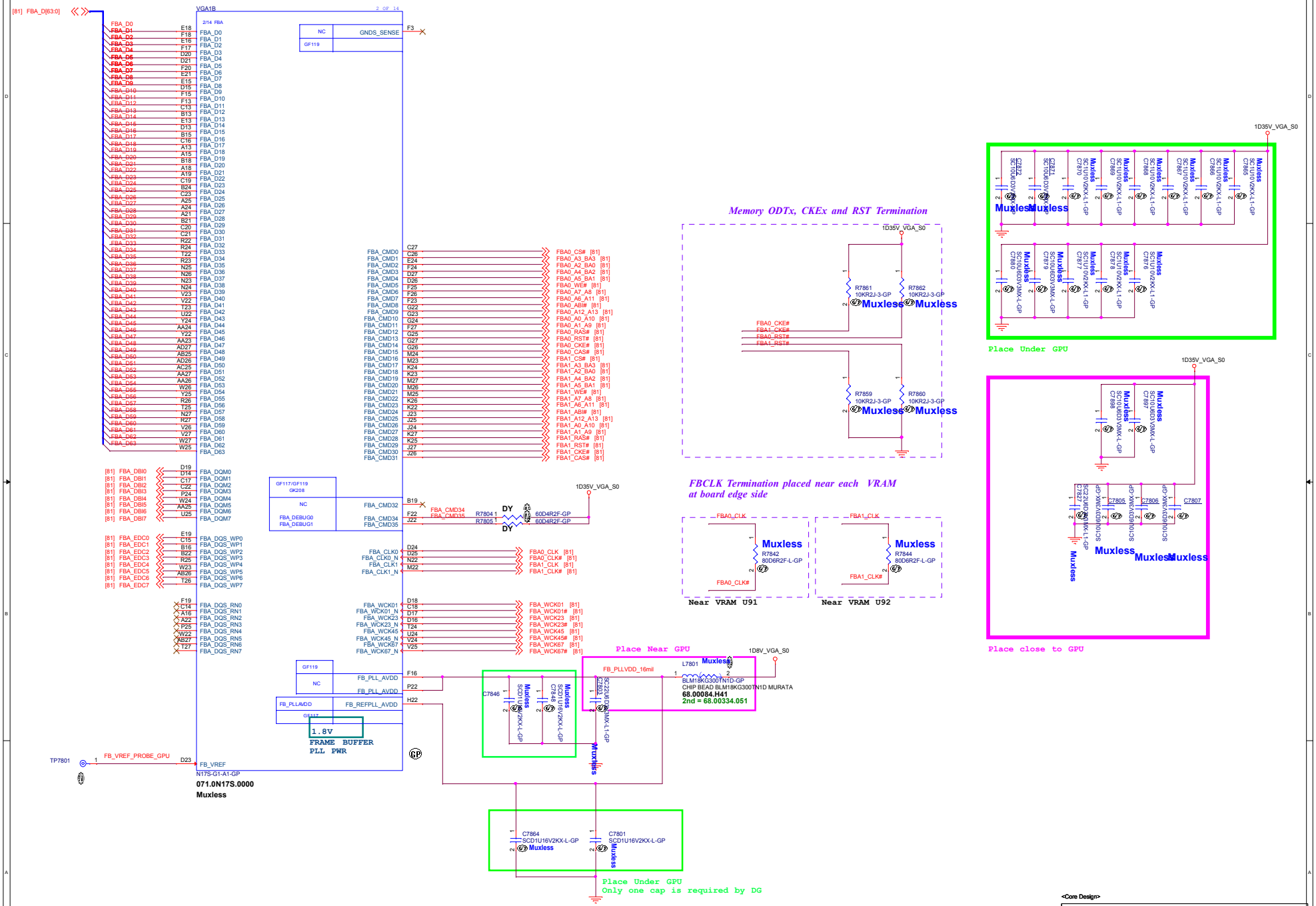
VGA1B
2/14 FBA
2_OF_14
[81] FBA_D[63:0]
FBA_D0 E18
FBA_D1 F18
FBA_D2 E16
FBA_D3 F17
FBA_D4 D20
FBA_D5 D21
FBA_D6 F20
FBA_D7 E21
FBA_D8 E15
FBA_D9 D15
FBA_D10 F15
FBA_D11 F13
FBA_D12 C13
FBA_D13 B13
FBA_D14 E13
FBA_D15 D13
FBA_D16 B15
FBA_D17 C16
FBA_D18 A13
FBA_D19 A15
FBA_D20 B18
FBA_D21 A18
FBA_D22 A19
FBA_D23 C19
FBA_D24 B24
FBA_D25 C23
FBA_D26 A25
FBA_D27 A24
FBA_D28 A21
FBA_D29 B21
FBA_D30 C20
FBA_D31 C21
FBA_D32 R22
FBA_D33 R24
FBA_D34 T22
FBA_D35 R23
FBA_D36 N25
FBA_D37 N26
FBA_D38 N23
FBA_D39 N24
FBA_D40 V23
FBA_D41 V22
FBA_D42 T23
FBA_D43 U22
FBA_D44 Y24
FBA_D45 AA24
FBA_D46 Y22
FBA_D47 AA23
FBA_D48 AD27
FBA_D49 AB25
FBA_D50 AD26
FBA_D51 AC25
FBA_D52 AA27
FBA_D53 AA26
FBA_D54 W26
FBA_D55 Y25
FBA_D56 R26
FBA_D57 T25
FBA_D58 N27
FBA_D59 R27
FBA_D60 V26
FBA_D61 V27
FBA_D62 W27
FBA_D63 W25
NC
GF119
GNDS_SENSE F3
FBA_CMD0 C27
FBA_CMD1 C26
FBA_CMD2 E24
FBA_CMD3 F24
FBA_CMD4 D27
FBA_CMD5 D26
FBA_CMD6 F25
FBA_CMD7 F26
FBA_CMD8 F23
FBA_CMD9 G22
FBA_CMD10 G23
FBA_CMD11 G24
FBA_CMD12 F27
FBA_CMD13 G25
FBA_CMD14 G27
FBA_CMD15 G26
FBA_CMD16 M24
FBA_CMD17 M23
FBA_CMD18 K24
FBA_CMD19 K23
FBA_CMD20 M27
FBA_CMD21 M26
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FBA_CMD23 K22
FBA_CMD24 J23
FBA_CMD25 J25
FBA_CMD26 J24
FBA_CMD27 K27
FBA_CMD28 K25
FBA_CMD29 J27
FBA_CMD30 J26
FBA_CMD31 J25
FBA0_CS# [81]
FBA0_A3_BA3 [81]
FBA0_A2_BA0 [81]
FBA0_A4_BA2 [81]
FBA0_A5_BA1 [81]
FBA0_WE# [81]
FBA0_A7_A8 [81]
FBA0_A6_A11 [81]
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FBA0_A12_A13 [81]
FBA0_A0_A10 [81]
FBA0_A1_A9 [81]
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[81] FBA_DBI7 U25
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FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
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[81] FBA_EDC3 B22
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[81] FBA_EDC5 W23
[81] FBA_EDC6 AB26
[81] FBA_EDC7 T26
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FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
F19 FBA_DQS_RN0
C14 FBA_DQS_RN1
A16 FBA_DQS_RN2
A22 FBA_DQS_RN3
P25 FBA_DQS_RN4
W22 FBA_DQS_RN5
AB27 FBA_DQS_RN6
T27 FBA_DQS_RN7
GF117/GF119
GK208
NC
FBA_DEBUG0
FBA_DEBUG1
FBA_CMD32 B19
FBA_CMD34 F22
FBA_CMD35 J22
FBA_CMD32
FBA_CMD34
FBA_CMD35
R7804 1 DY 2 60D4R2F-GP
R7805 1 DY 2 60D4R2F-GP
1D35V_VGA_S0
FBA_CLK0 D24
FBA_CLK0_N D25
FBA_CLK1 N22
FBA_CLK1_N M22
FBA0_CLK [81]
FBA0_CLK# [81]
FBA1_CLK [81]
FBA1_CLK# [81]
FBA_WCK01 D18
FBA_WCK01_N C18
FBA_WCK23 D17
FBA_WCK23_N D16
FBA_WCK45 T24
FBA_WCK45_N U24
FBA_WCK67 V24
FBA_WCK67_N V25
FBA_WCK01 [81]
FBA_WCK01# [81]
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FBA_WCK23# [81]
FBA_WCK45 [81]
FBA_WCK45# [81]
FBA_WCK67 [81]
FBA_WCK67# [81]
GF119
NC
FB_PLL_AVDD F16
FB_PLL_AVDD P22
FB_PLLAVDD
FB_REFPLL_AVDD H22
GF117
1.8V
FRAME BUFFER
PLL PWR
Place Near GPU
1D8V_VGA_S0
FB_PLLVDD_16mil
L7801 Muxless
BLM18KG300TN1D-GP
CHIP BEAD BLM18KG300TN1D MURATA
68.00084.H41
2nd = 68.00334.051
C7846 SCD1U16V2KX-L-GP Muxless
C7848 SCD1U16V2KX-L-GP Muxless
C7803 SC220U6D3VM-L1-GP Muxless
TP7801
FB_VREF_PROBE_GPU
D23 FB_VREF
N17S-G1-A1-GP
071.0N17S.0000
Muxless
C7864 SCD1U16V2KX-L-GP Muxless
C7801 SCD1U16V2KX-L-GP Muxless
Place Under GPU
Only one cap is required by DG
Memory ODTx, CKEx and RST Termination
1D35V_VGA_S0
R7861 10KR2J-3-GP Muxless
R7862 10KR2J-3-GP Muxless
R7859 10KR2J-3-GP Muxless
R7860 10KR2J-3-GP Muxless
FBA0_CKE#
FBA1_CKE#
FBA0_RST#
FBA1_RST#
FBCLK Termination placed near each VRAM at board edge side
FBA0_CLK
FBA0_CLK#
R7842 80D6R2F-L-GP Muxless
Near VRAM U91
FBA1_CLK
FBA1_CLK#
R7844 80D6R2F-L-GP Muxless
Near VRAM U92
1D35V_VGA_S0
C7872 SC10U6D3VM-L-GP Muxless
C7870 SCU10V2KX-L1-GP Muxless
C7869 SCU10V2KX-L1-GP Muxless
C7868 SCU10V2KX-L1-GP Muxless
C7867 SCU10V2KX-L1-GP Muxless
C7866 SCU10V2KX-L1-GP Muxless
C7865 SCU10V2KX-L1-GP Muxless
C7880 SC10U6D3VM-L-GP Muxless
C7879 SCU10V2KX-L1-GP Muxless
C7877 SCU10V2KX-L1-GP Muxless
C7878 SCU10V2KX-L1-GP Muxless
C7876 SCU10V2KX-L1-GP Muxless
Place Under GPU
1D35V_VGA_S0
C7898 SC10U6D3VM-L-GP Muxless
C7897 SC10U6D3VM-L-GP Muxless
C7827 SC22U6D3VM-L1-GP Muxless
C7805 SCD1U10V2KX-L1-GP Muxless
C7806 SCD1U10V2KX-L1-GP Muxless
C7807 SCD1U10V2KX-L1-GP Muxless
Muxless
Muxless
Muxless
Muxless
Place close to GPU
<Core Design>
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU (3/5) VRAM I/F
Size Custom
Document Number
Strongbow_KL
Rev 1
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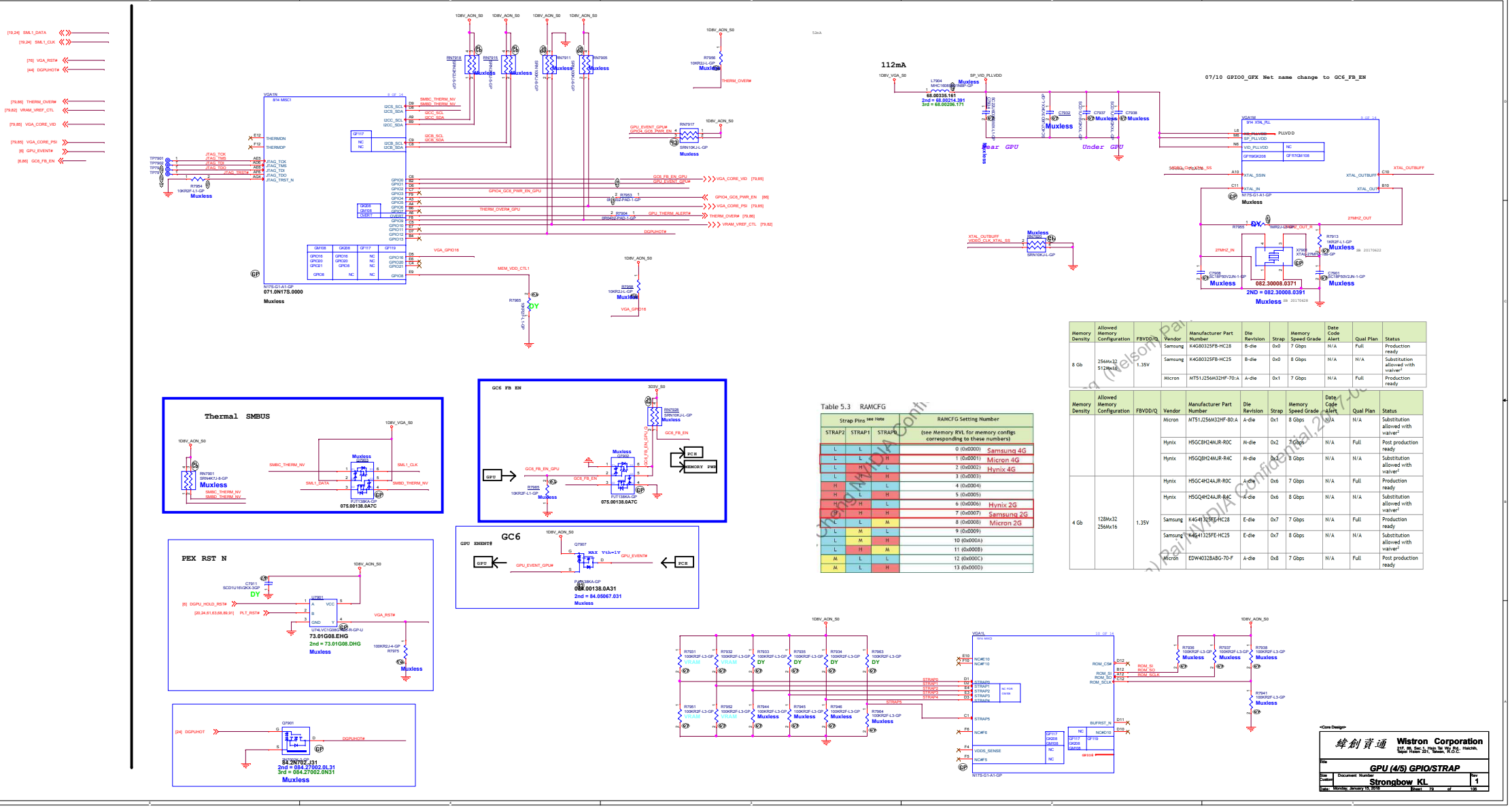

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
4 Gb	128Mx32 256Mx16	1.35V	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production ready

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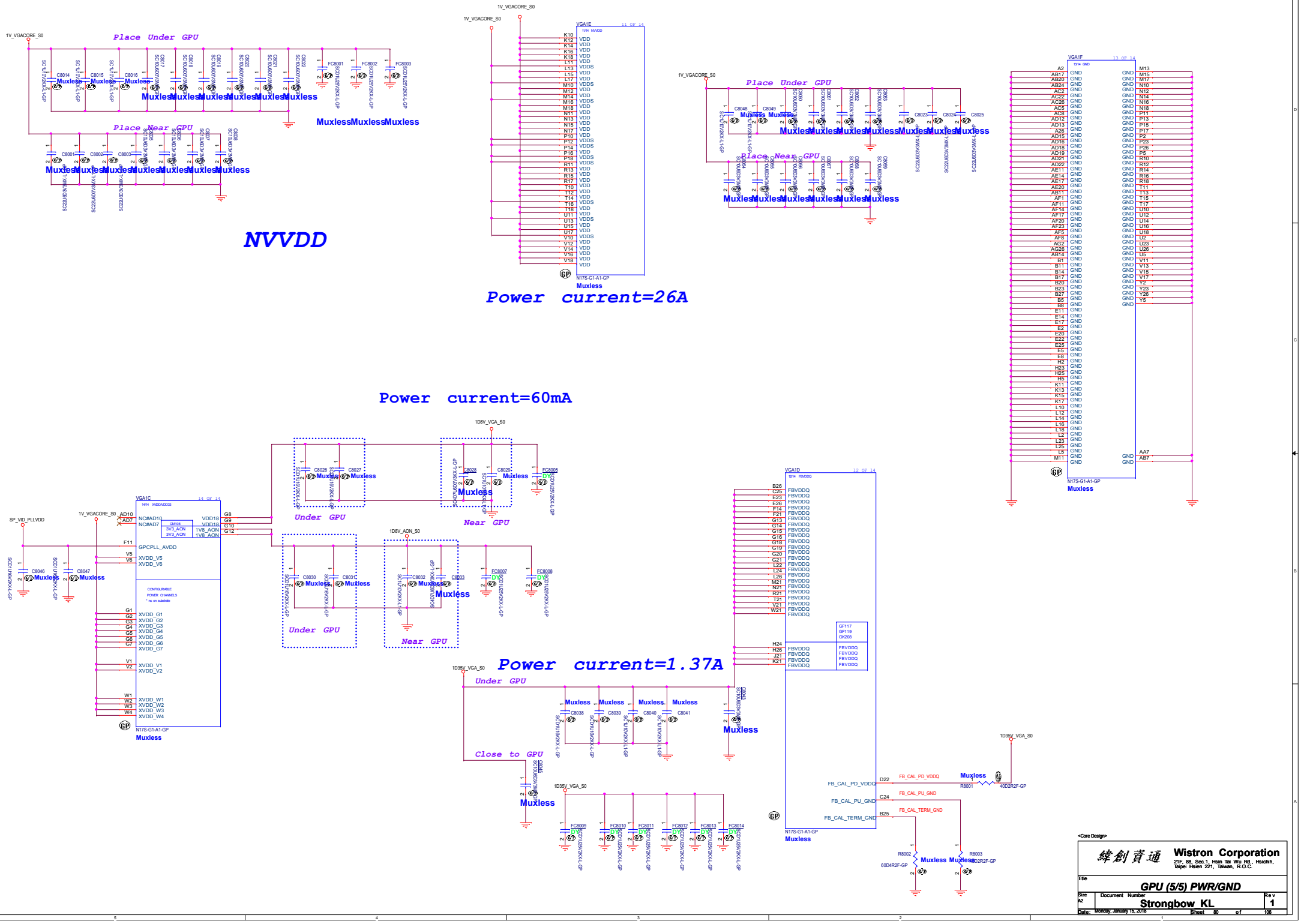
GPU (4/5) GPIO/STRAP

Strongbow_KL

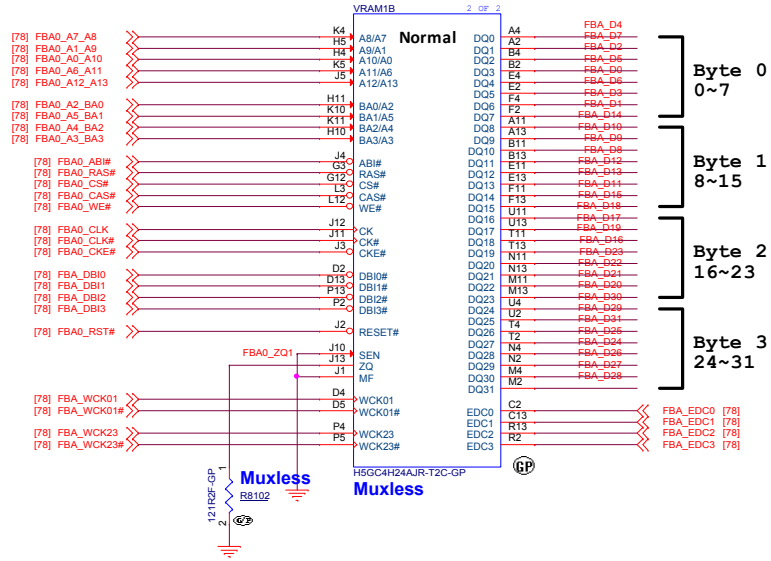
Monday, January 15, 2018

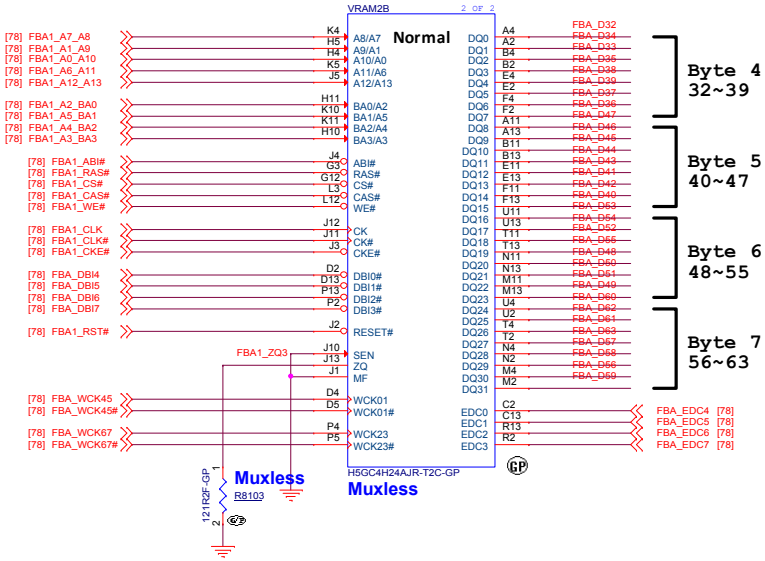

Place Under GPU
Place Near GPU
NVVDD
Power current=26A
Power current=60mA
Under GPU
Near GPU
Power current=1.37A
Close to GPU
Muxless
Wistron Corporation
GPU (5/5) PWR/GND
Strongbow_KL

[78] FBA_D[63:0]

TABLE
GDDR5 VIDEO MEMORY

	072.05424.0A0U	072.44132.000U	072.04032.000N
	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1 VRAM2	H5GC4H24AJR-T2C	K4G41325FC-HC03	EDW4032BABG-60-F-D





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Title: VRAM CHANNEL-A

Size	Document Number	Rev
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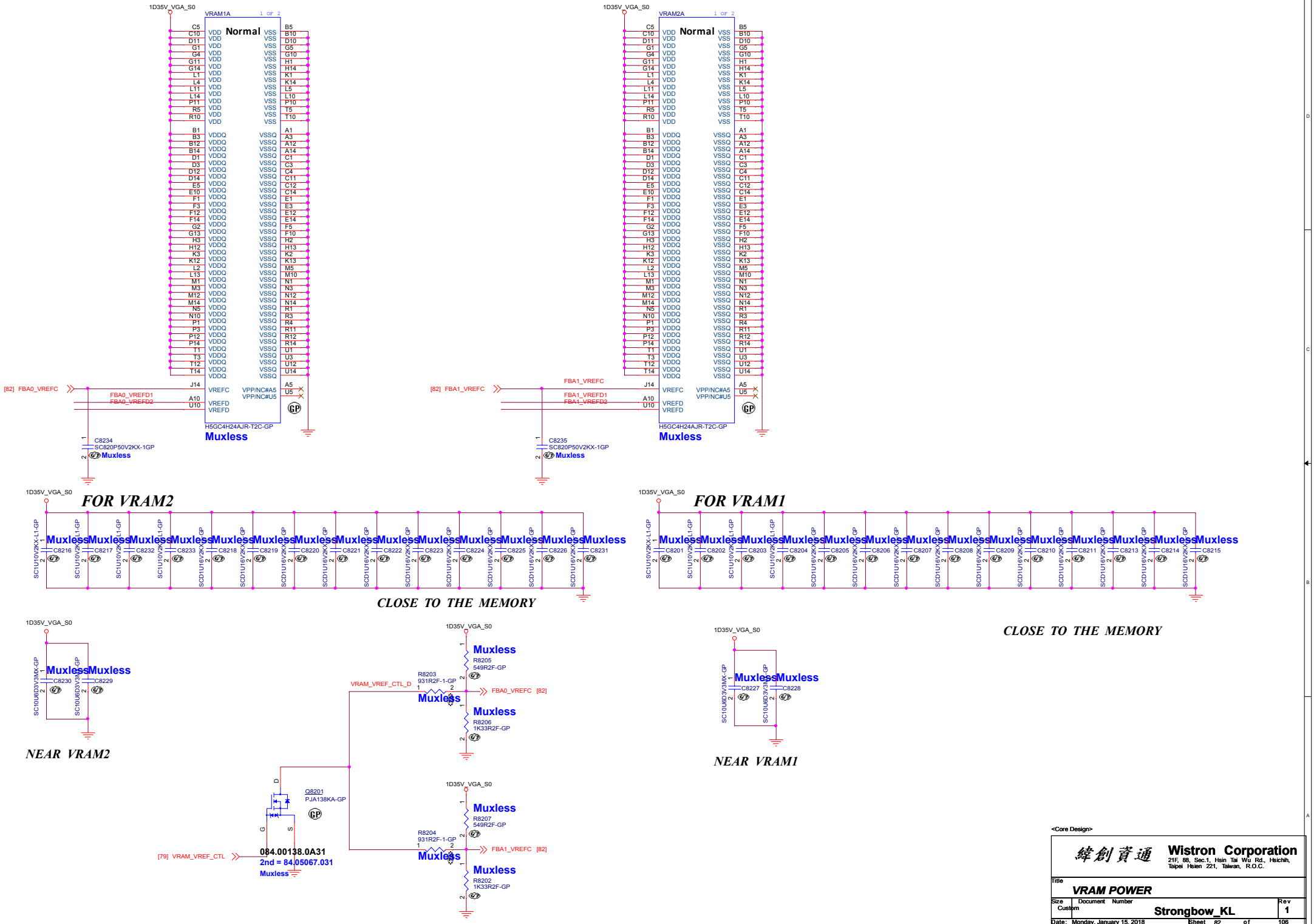

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Title: VRAM POWER

Size	Document Number	Rev
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Title: ***VRAM CHANNEL-B***

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Title
MEMORY TERMINATION

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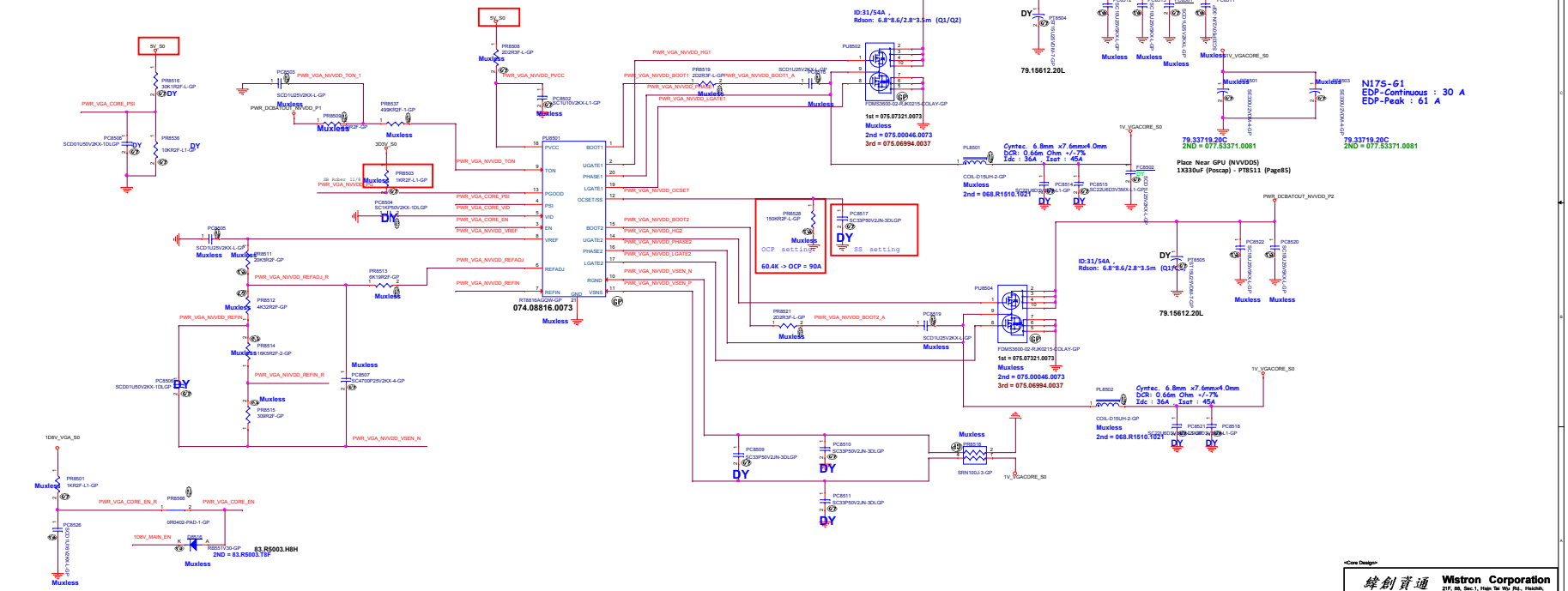
OFFPAGE

RT8816A For NVVDD

N17S-G1
EDP-Continuous : 30 A
EDP-Peak : 61 A



<Core Design>

Wistron Corporation		
Title	RT8816A/RT8813D VGA CORE	
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SSID = PWR.Plane.Regulator_1p0v

SSID = PWR.Plane.Regulator_1p35v

IC	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
COM			
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 for 1D35V

TDC : 8.6A
Peak : 10.3A

Cyntec 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

2nd = 68.1R01E.10C

Vo=0.8x(1+R1/R2)
=1.35

SYW232 for 1D8V_AON

VGA_CORE&1D05V_VGA_S0 Discharge Circuit

3D3V_S5 to 1D8V_AON_S0

20150821 R8615 change to PAD

N17 EE Change

20150824 DY PR8621 for GPU power sequence

N17 change to ANPEC APL3526/B

Cyntec 2.5 x 2.0 x 1.2mm
DCR: 37~43 mOhm
Idc : 2.6A , Isat : 2.7A

TDC: 1.5A
OCP>3.5A

Vo=0.6x(1+R1/R2)
=0.6x(1+100/49.9)
=1.8024

SYW232 for 1D05V
Enable=1.5V
Disable=0.4V

SYW232 for 1D8V_MAIN

73.01G08.EHG
2nd = 73.01G08.DHG

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Title: AOZ2262_1D35V_VRAM

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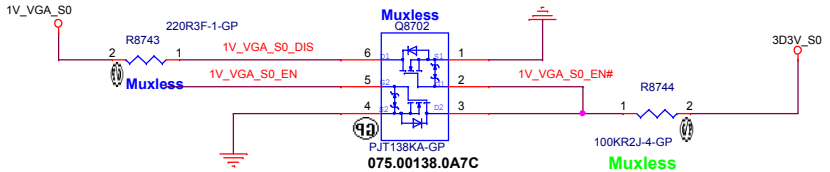
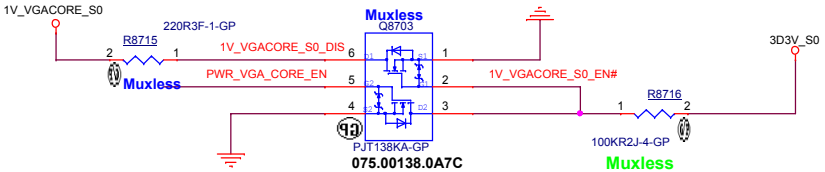
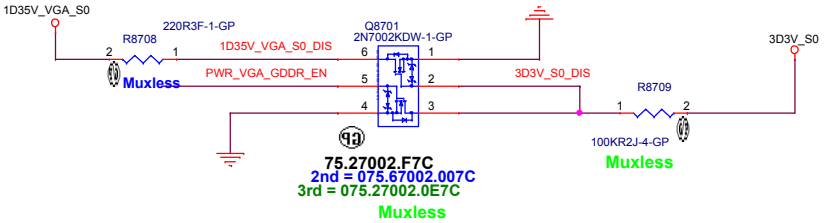
[86] 1V_VGA_S0_EN

[85] PWR_VGA_CORE_EN

[86] PWR_VGA_GDDR_EN







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Title: Discharge

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Title	***N16 Power***	
Size: Custom	Document Number: **Strongbow_KL**	Rev: 1
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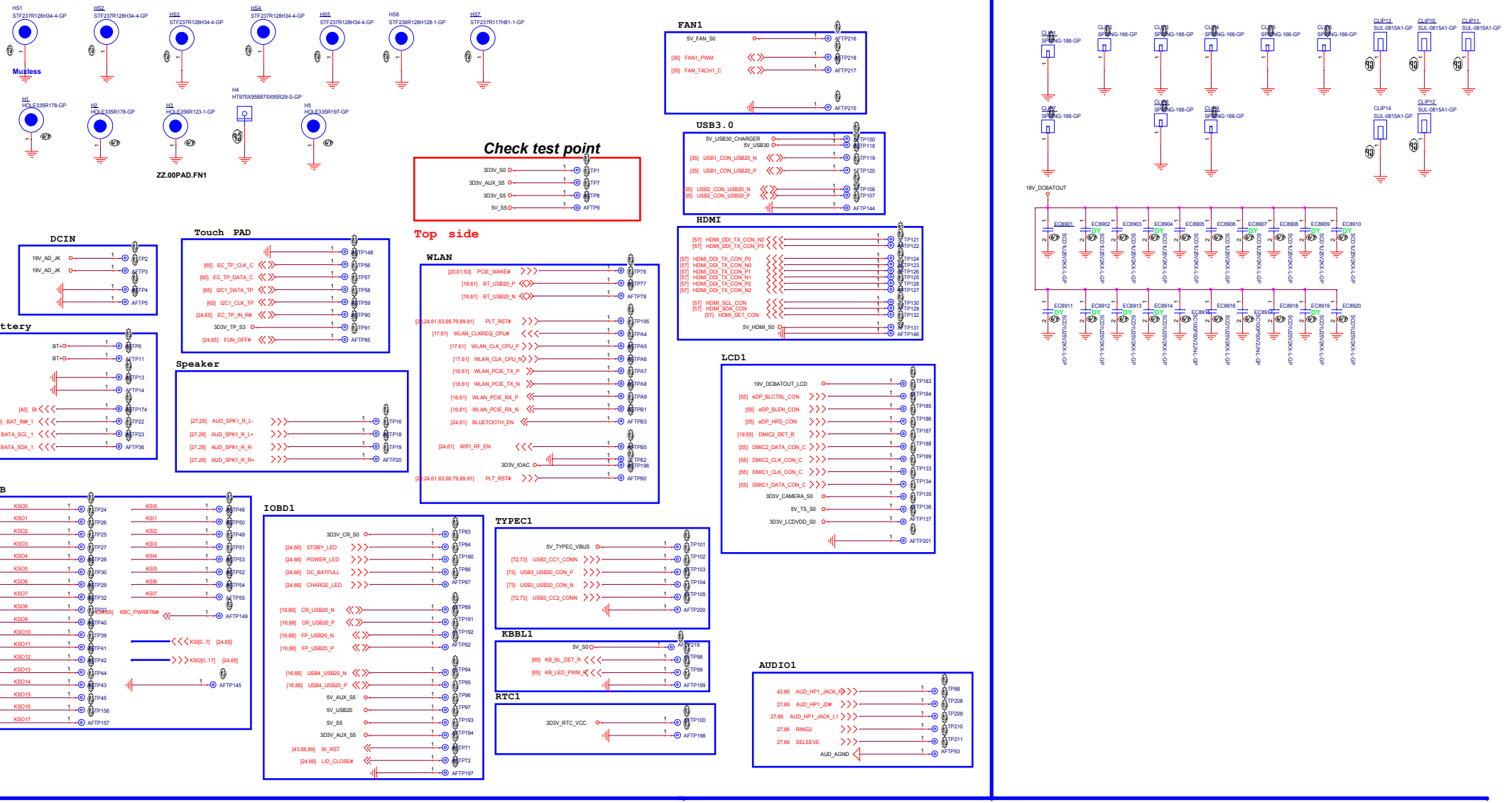

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Title: UNUSED PARTS/EMI Capacitors

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
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[19,24,68] LPC_AD_CPU_P0
[19,24,68] LPC_AD_CPU_P1
[19,24,68] LPC_AD_CPU_P2
[19,24,68] LPC_AD_CPU_P3

[19] LPC_CLK_TPM
[19,24,68] LPC_FRAME#_CPU
[20,24,61,63,68,79,89] PLT_RST#
[19,24,68] INT_SERIRQ
[19,24] PM_CLKRUN#_EC

[20,24,40,60] PM_SLP_S0#

3D3V_S5 3D3V_S0

C9101 SCD1U16V2KX-L-GP
C9102 SC10U6D3V3KX-L-GP
C9103 SCD1U16V2KX-L-GP
C9104 SCD1U16V2KX-L-GP

TPM TPM TPM TPM

3D3V_S0

R9103 4K7R2J-L-GP DY
TPM_PP
R9104 4K7R2J-L-GP
TPM

3D3V_S0

R9107 0R0402-PAD

3D3V_S5

R9105 0R0402-PAD

U9101

3D3V_TPM_VDD
VDD
VHIO
VHIO
VSBD
VSB

LPC_AD_CPU_P0
LPC_AD_CPU_P1
LPC_AD_CPU_P2
LPC_AD_CPU_P3
LAD0/MISO
LAD1/MOSI
LAD2/SPI_IRQ#
LAD3

PLT_RST#
LPC_CLK_TPM
LPC_FRAME#_CPU
INT_SERIRQ
LRESET#/SPI_RST#/SRESET#
LCLK/SCLK
LFRAME#/SCS#
SERIRQ

TP9101
LPCPD#
LPCPD#

TPM_PP
PP
TEST

SDA/GPIO0
GPIO1/SCL
GPX/GPIO2
GPIO3/BADD
CLKRUN#/GPIO4/SINT#
RESERVED#12

NC#2
NC#7
NC#10
NC#11
NC#25
NC#26
NC#31

GND GND GND GND GND

GPX/GPIO2 R9106 0R0402-PAD-1-GP PM_SLP_S0#
PM_CLKRUN#_EC

NPCT650ABBYX-GP

TPM

071.00650.0N03

<Core Design>

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Title	TPM	
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Title
Reserved

Size	Document Number	Rev
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Title

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Title

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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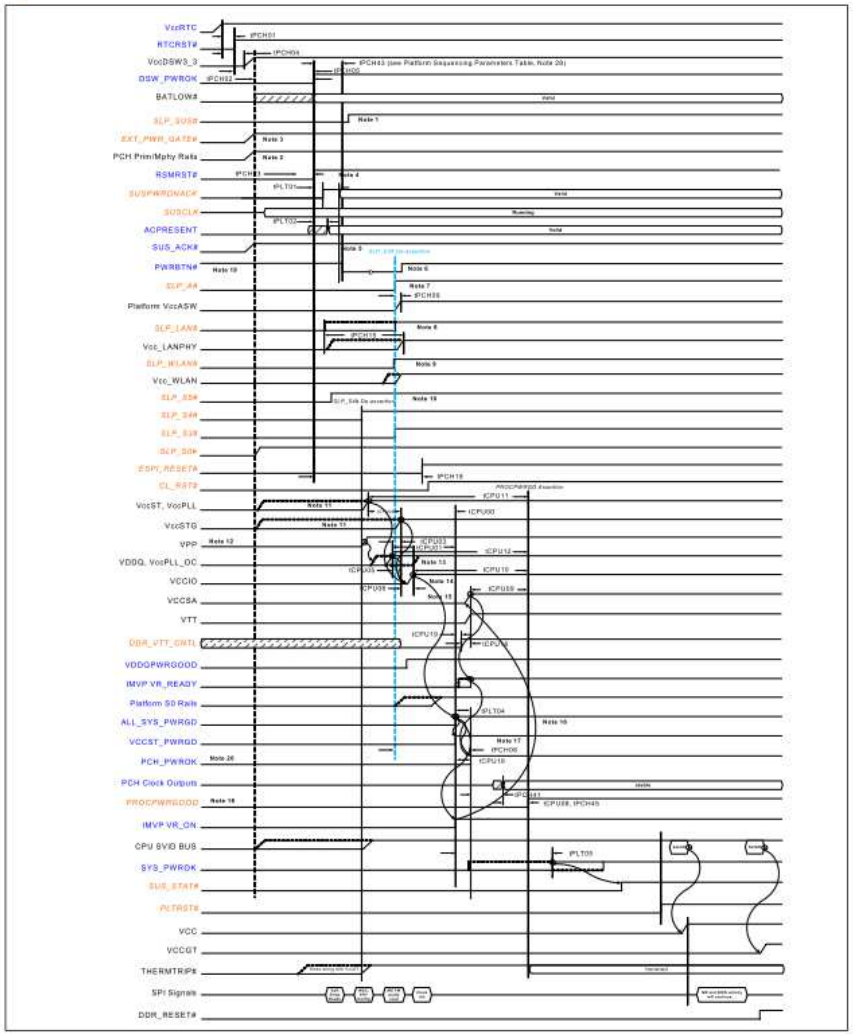
Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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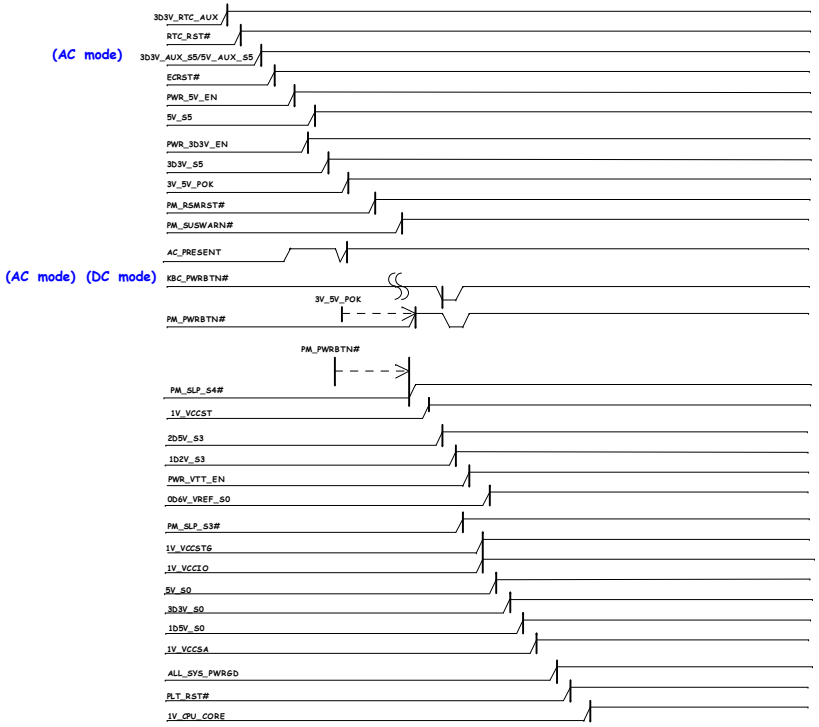
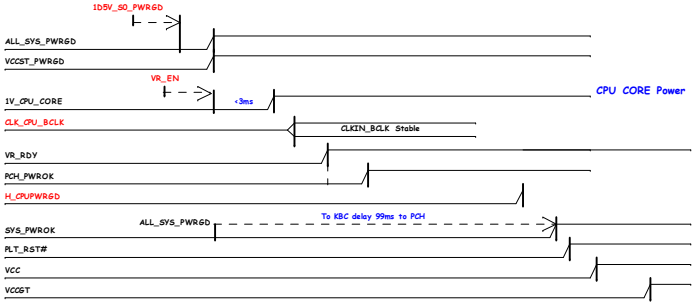
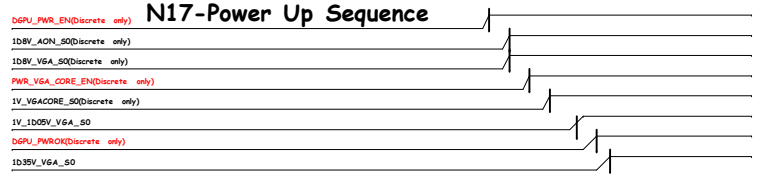
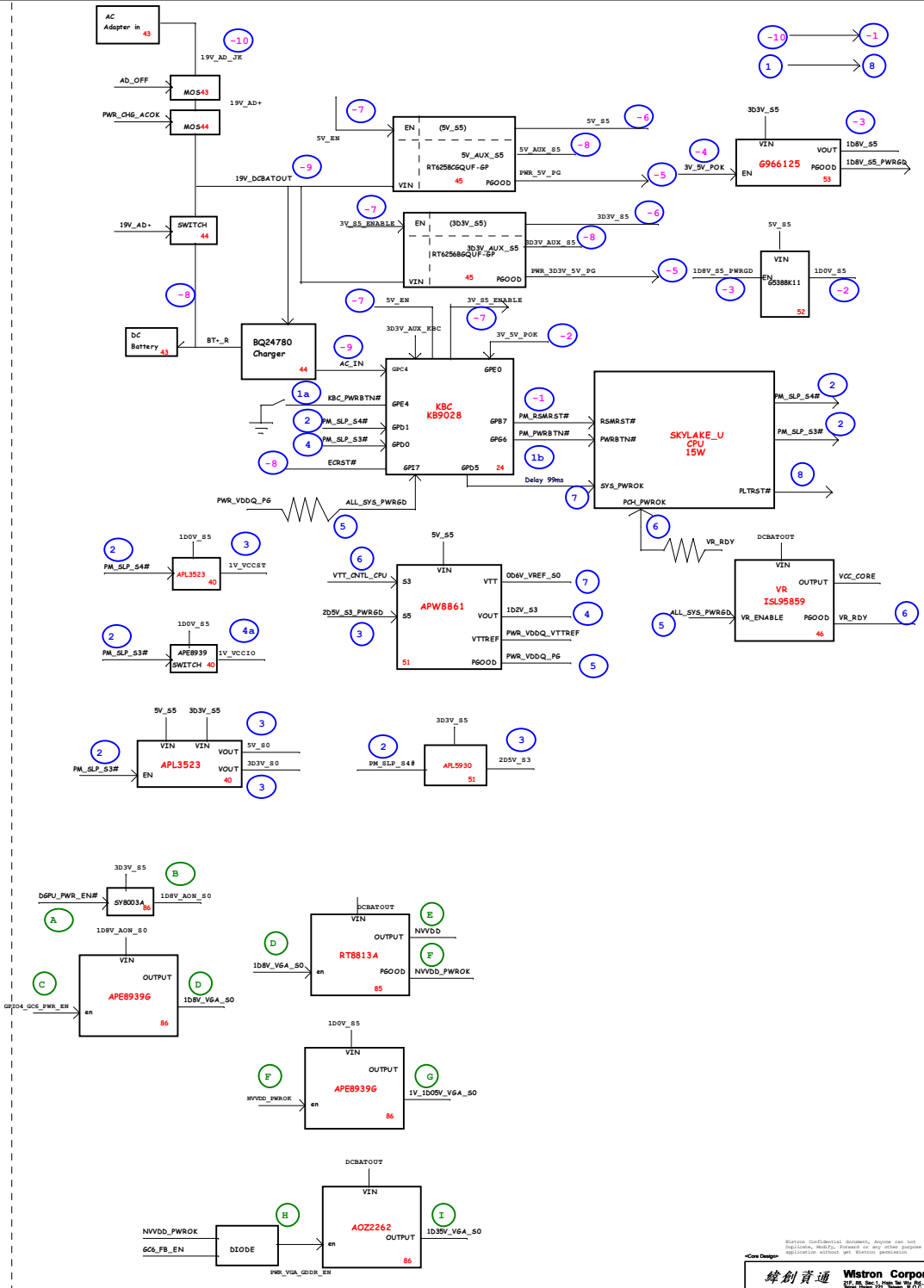
Intel-Power Up Sequence





N17-Power Up Sequence





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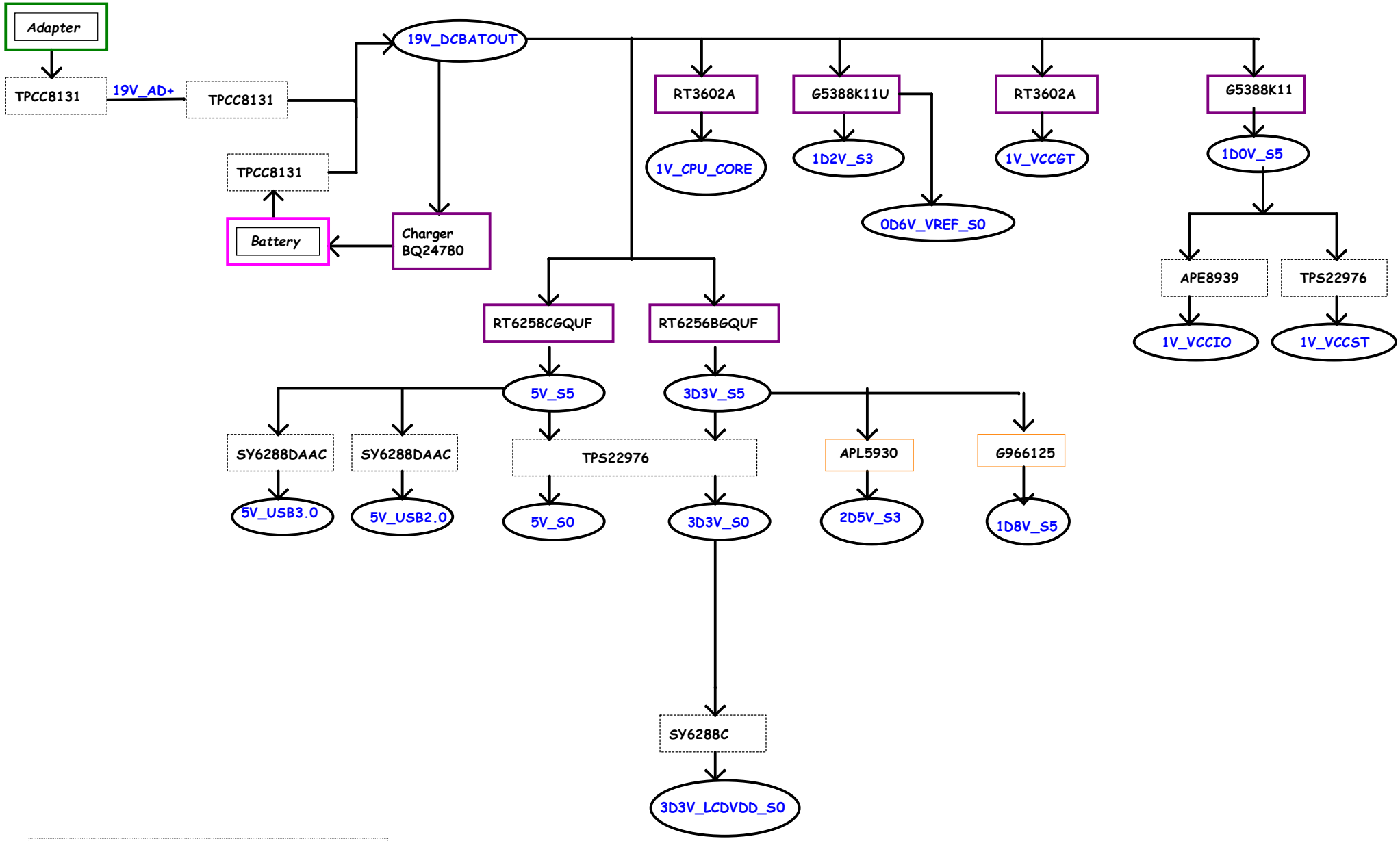

Power Shape

Regulator	LDO	Switch

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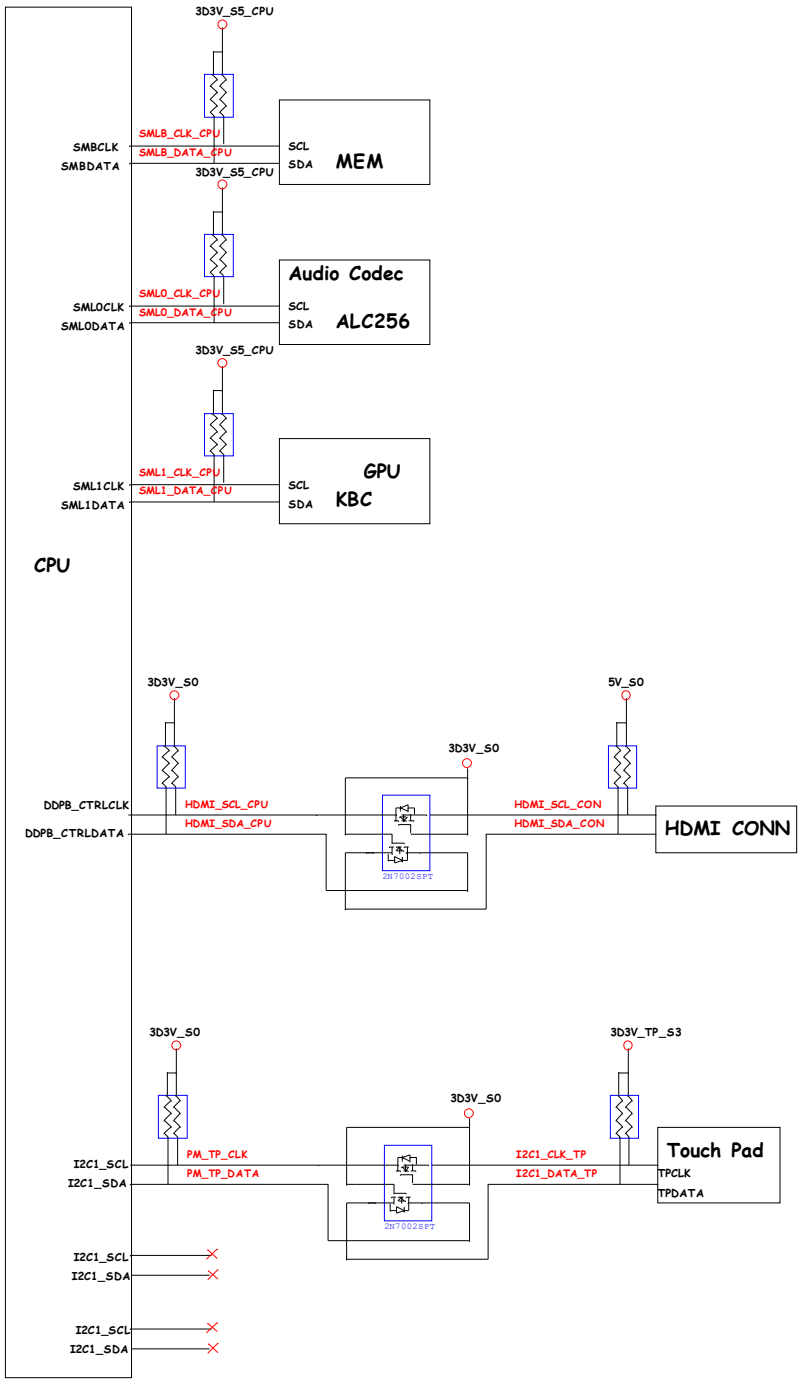
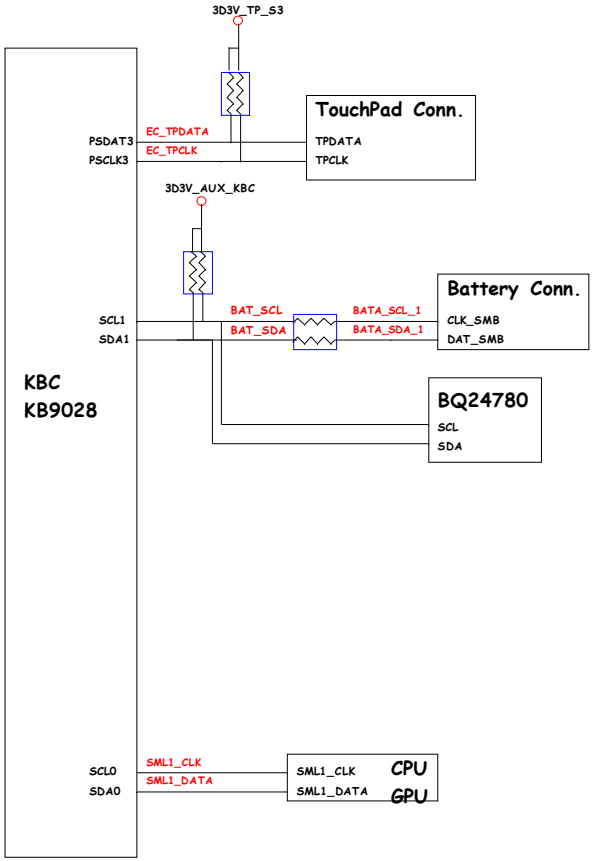
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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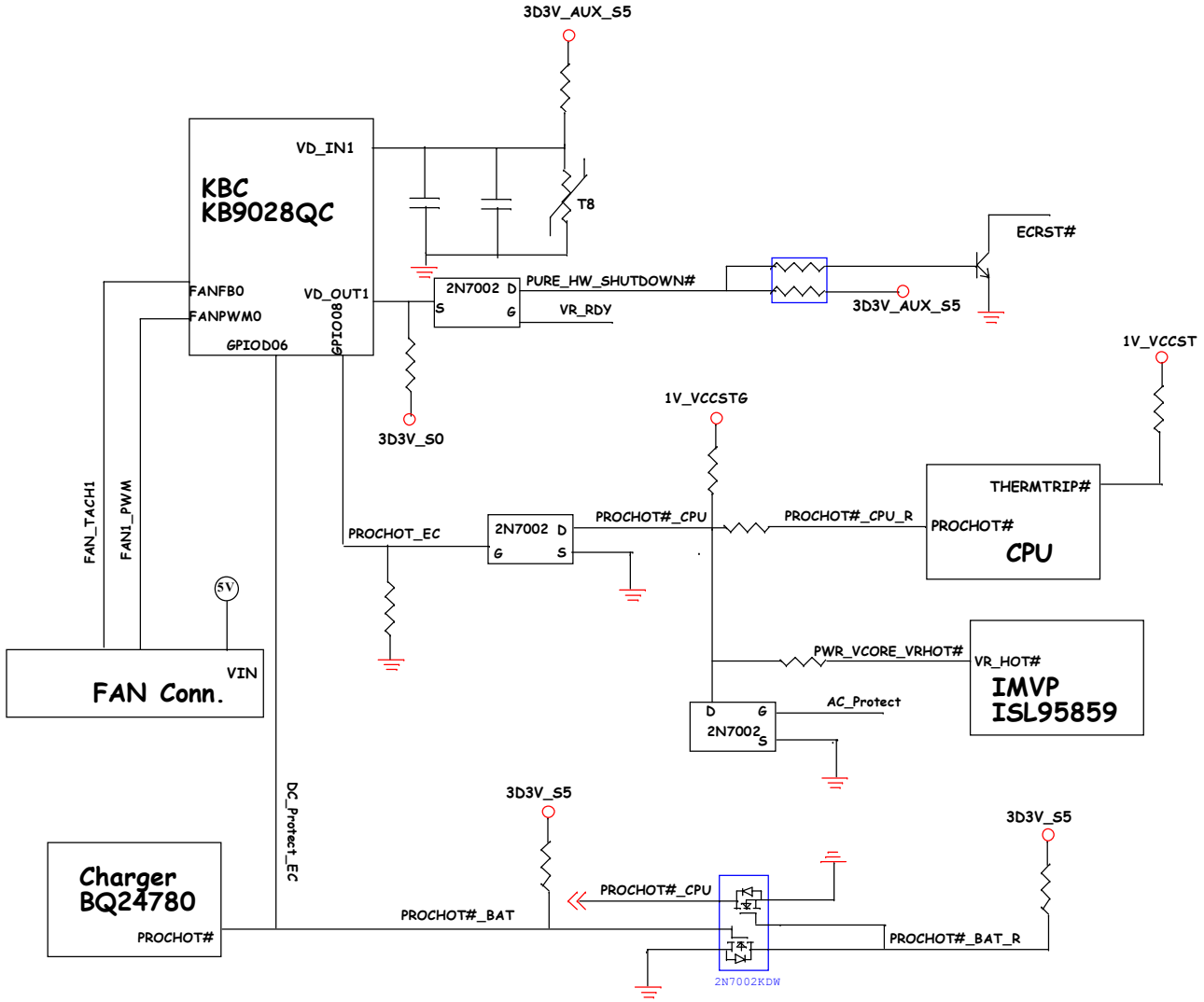
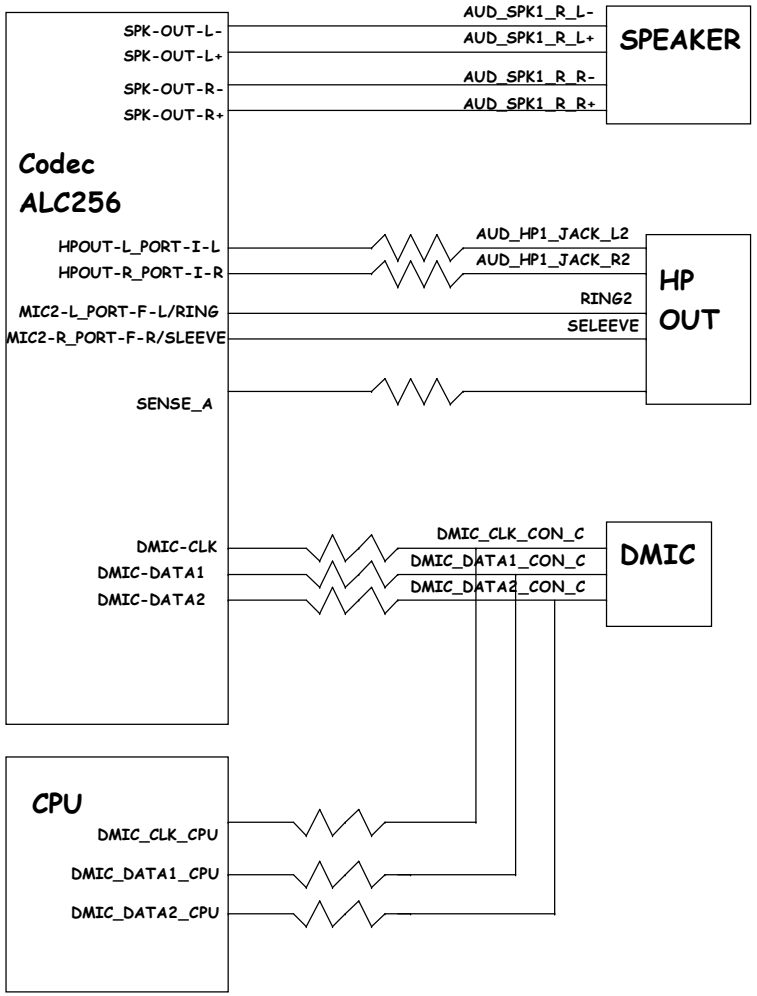
Thermal Block Diagram



Audio Block Diagram



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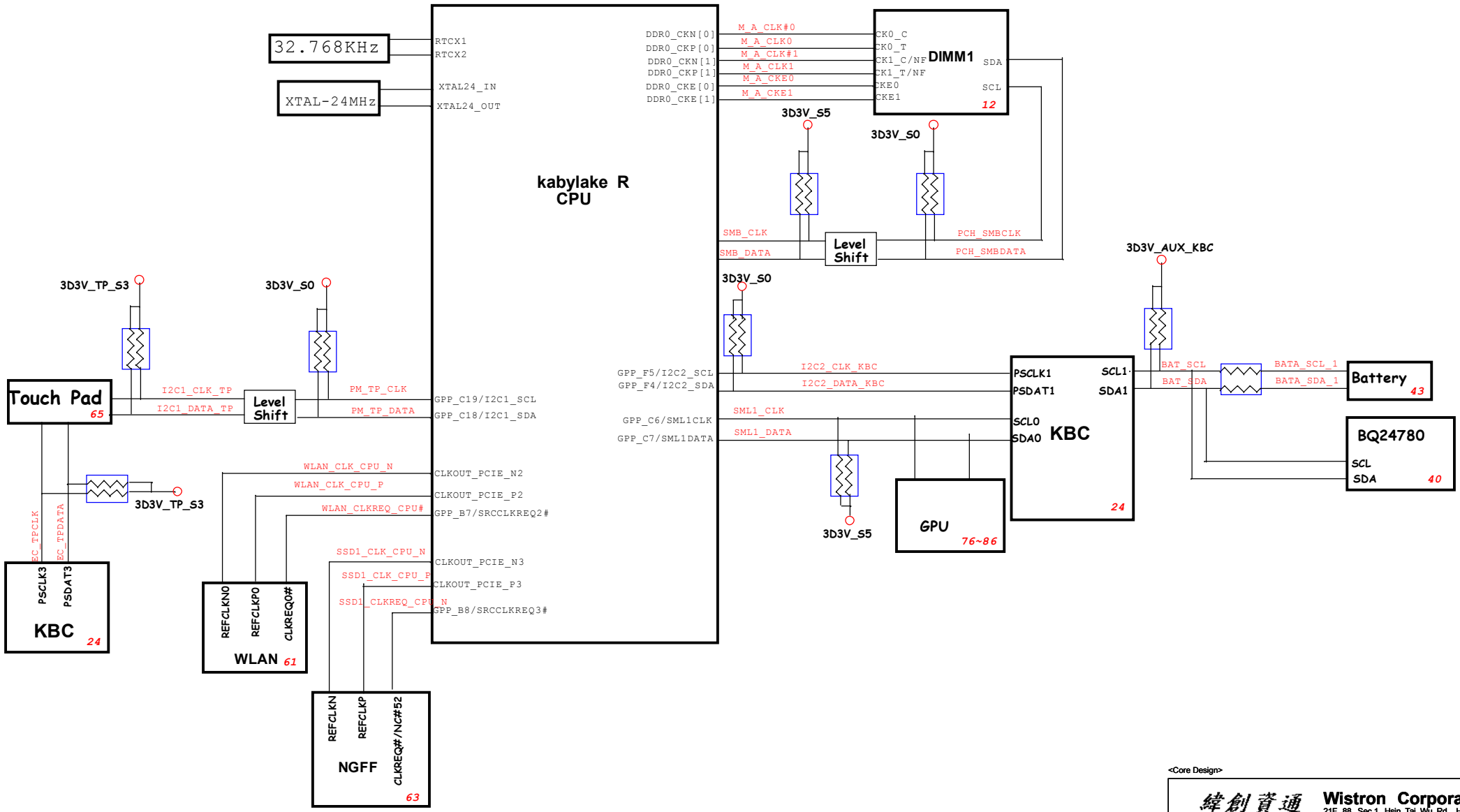
CLOCK BLOCK DIAGRAM



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Title: CLK Block

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