Project Name :GK5CxxT

Platform : CFL-H+N18E-Gx+Thunderbolt3

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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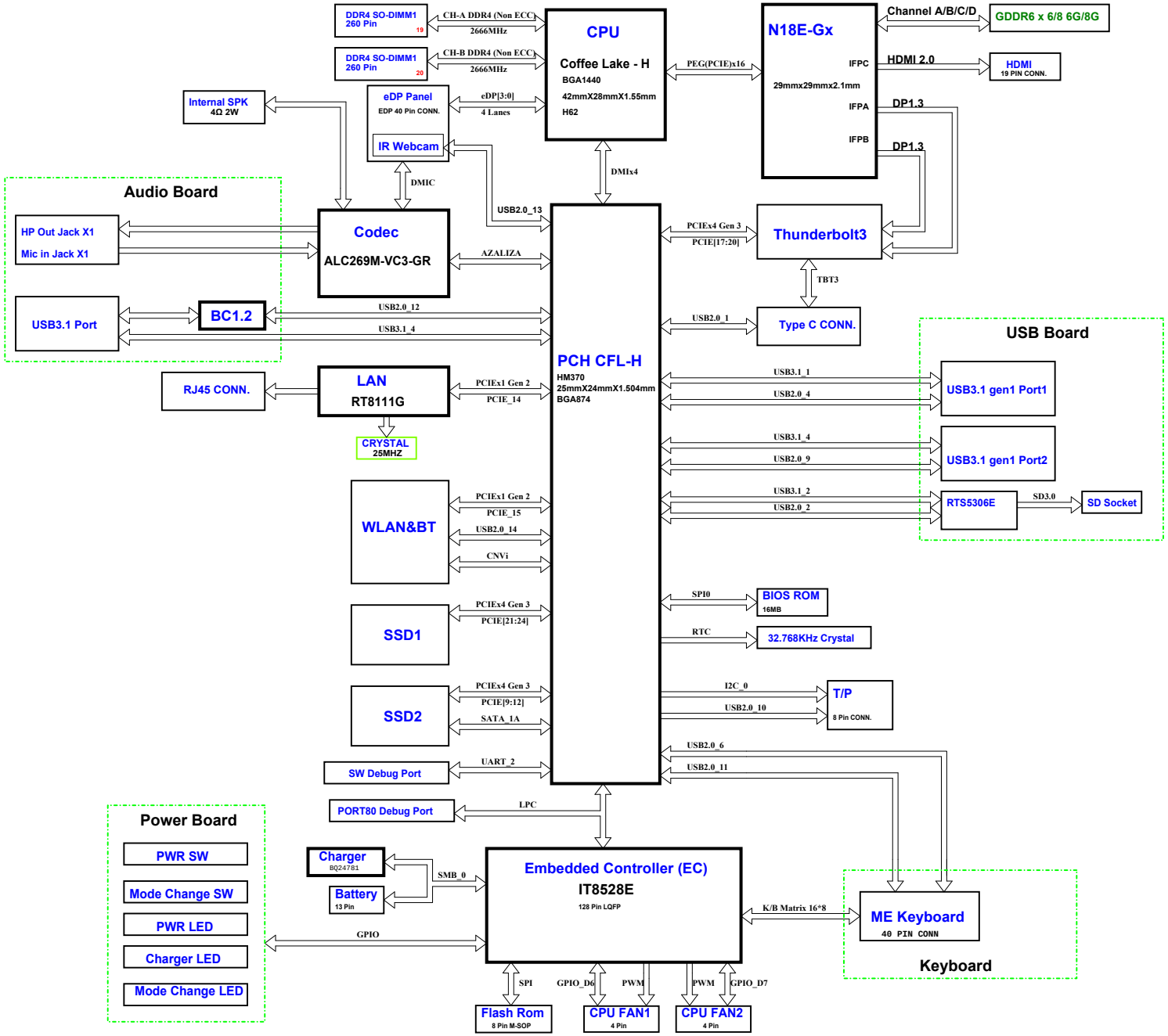
Title: 01_INDEX

Size: Custom | Document Number: GK5CXXT | Rev: 1.0

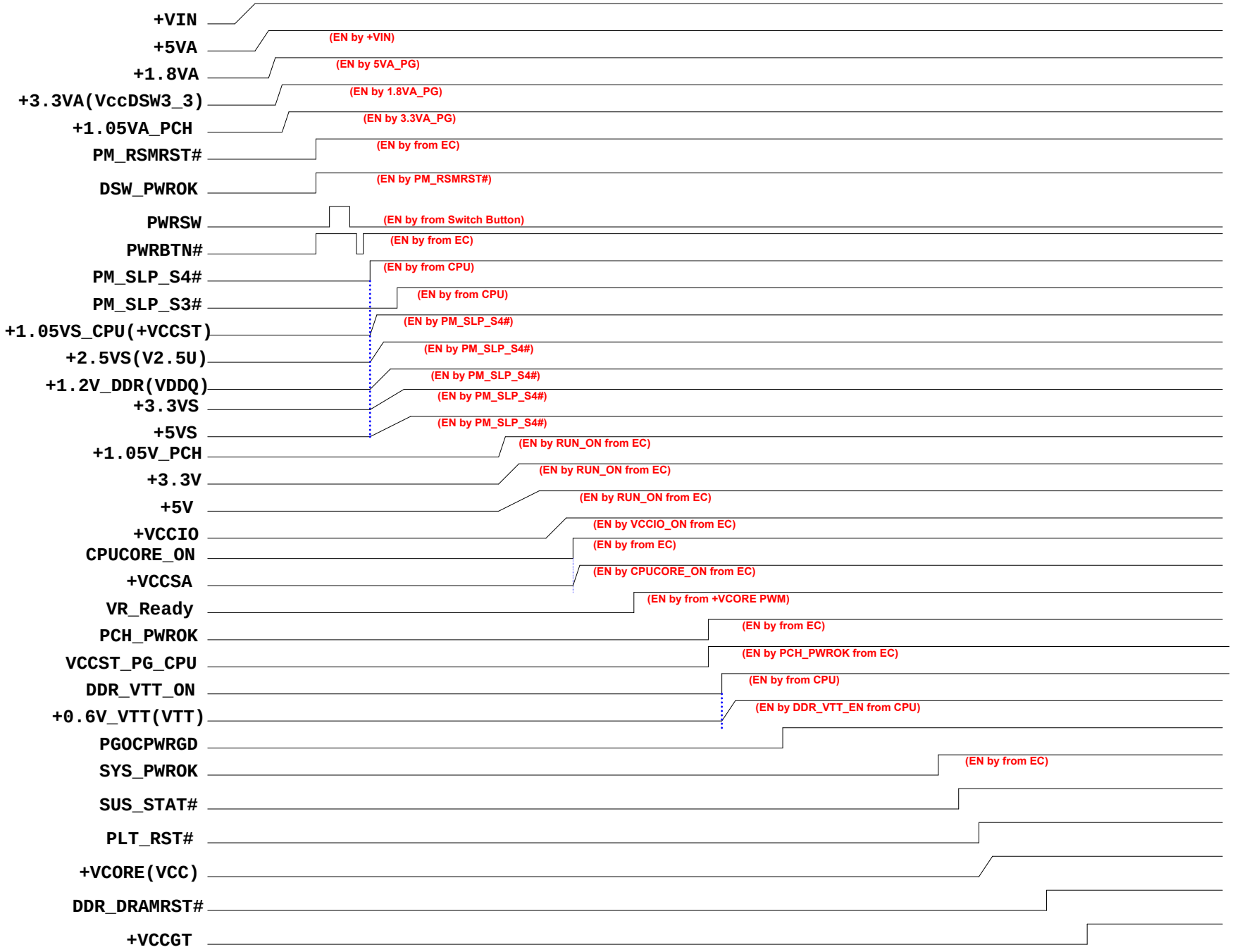
Date: Wednesday, May 08, 2019 | Sheet 1 of 70

SYSTEM BLOCK DIAGRAM



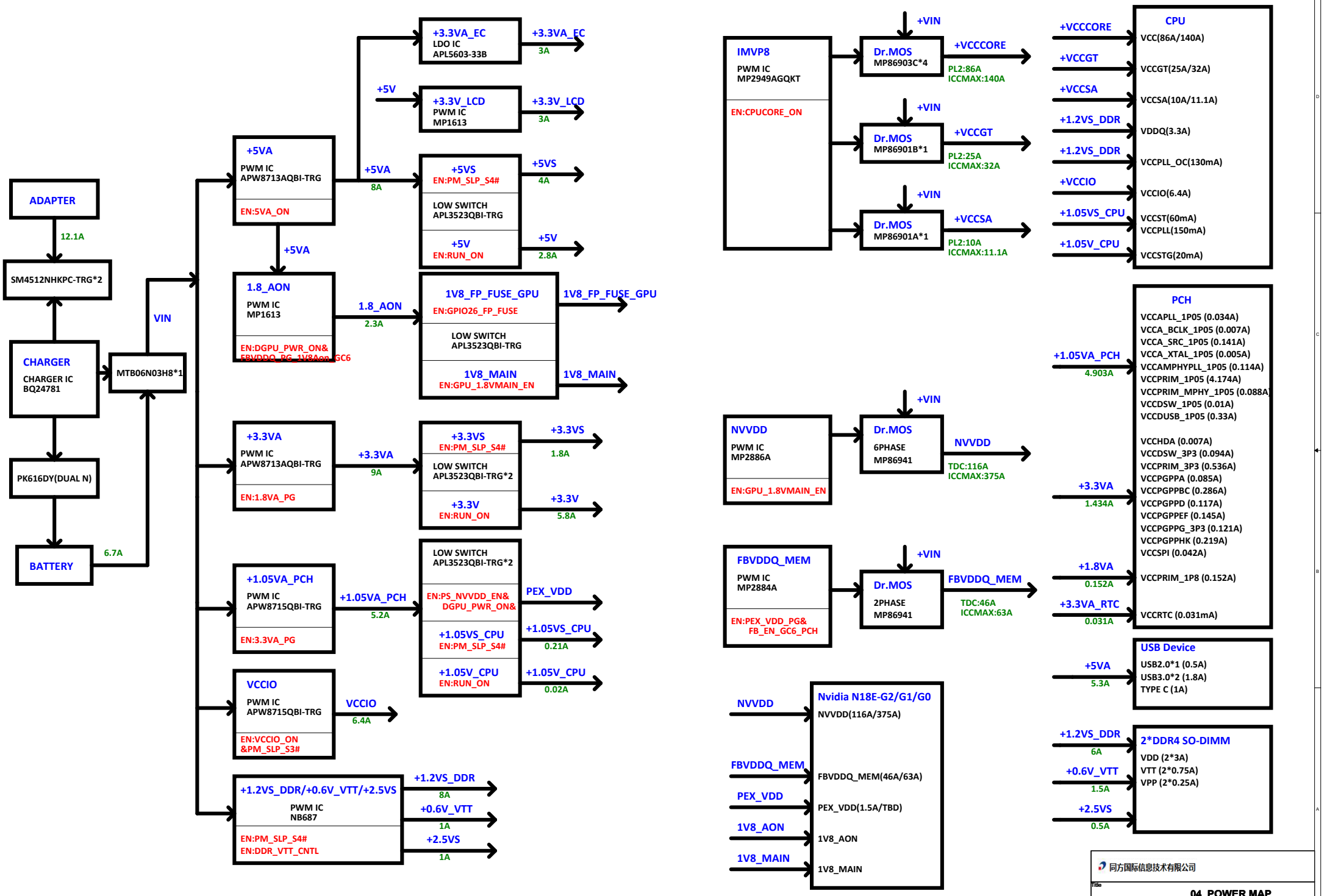
同方国际信息技术有限公司		
Title: 02_SYSTEM BLOCK		
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 2 of 70	

POWER ON SEQUENCE



同方国际信息技术有限公司

Title	03_POWER SEQUENCE	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 3 of 70	



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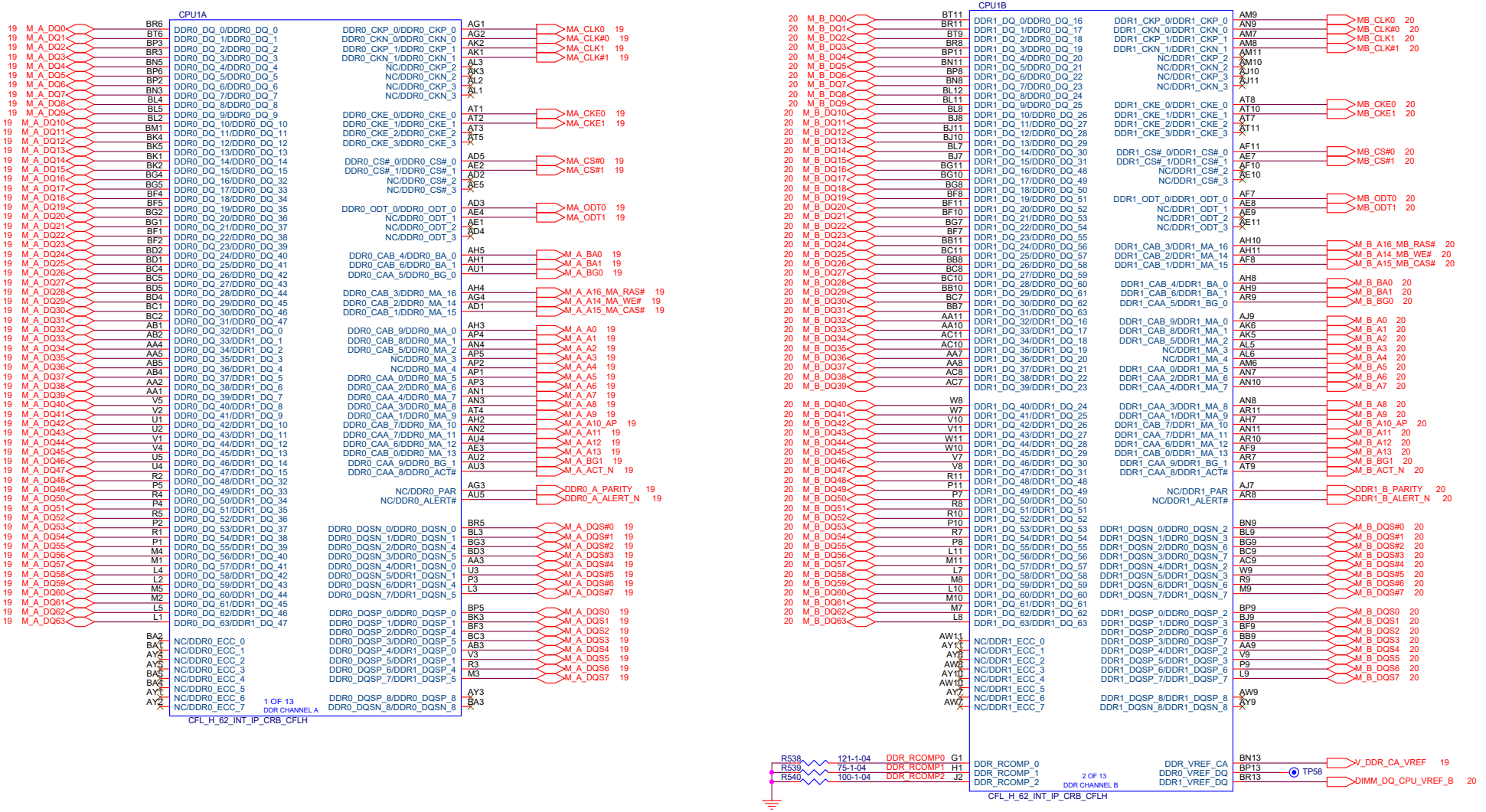
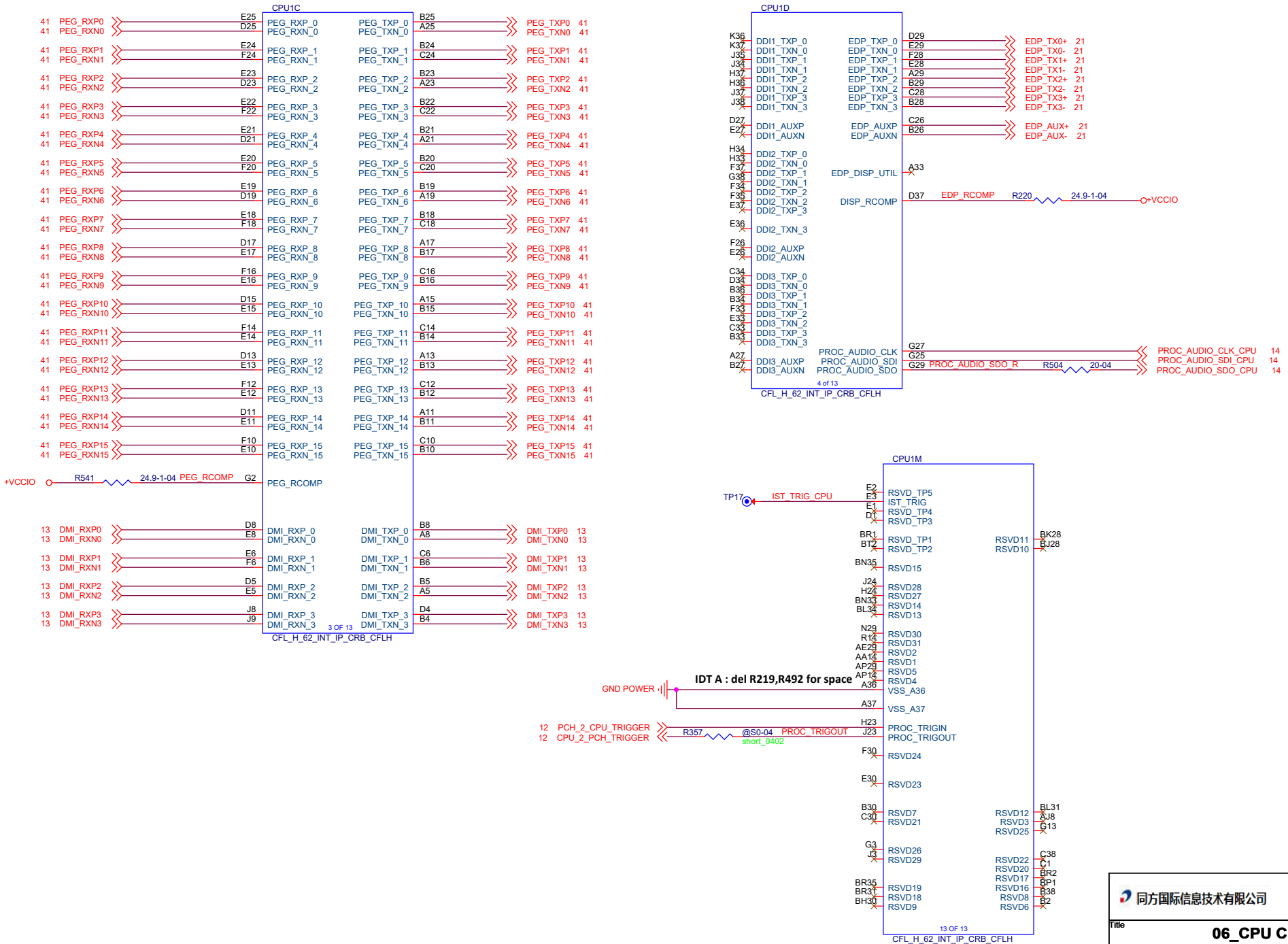
Title	04_POWER MAP	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 4 of 70	



同方国际信息技术有限公司

Title	05_CPU CFL-H DDR4	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 5 of 70	


CPU1C
PEG_RXP0 PEG_RXN0 PEG_TXP0 PEG_TXN0
PEG_RXP1 PEG_RXN1 PEG_TXP1 PEG_TXN1
PEG_RXP2 PEG_RXN2 PEG_TXP2 PEG_TXN2
PEG_RXP3 PEG_RXN3 PEG_TXP3 PEG_TXN3
PEG_RXP4 PEG_RXN4 PEG_TXP4 PEG_TXN4
PEG_RXP5 PEG_RXN5 PEG_TXP5 PEG_TXN5
PEG_RXP6 PEG_RXN6 PEG_TXP6 PEG_TXN6
PEG_RXP7 PEG_RXN7 PEG_TXP7 PEG_TXN7
PEG_RXP8 PEG_RXN8 PEG_TXP8 PEG_TXN8
PEG_RXP9 PEG_RXN9 PEG_TXP9 PEG_TXN9
PEG_RXP10 PEG_RXN10 PEG_TXP10 PEG_TXN10
PEG_RXP11 PEG_RXN11 PEG_TXP11 PEG_TXN11
PEG_RXP12 PEG_RXN12 PEG_TXP12 PEG_TXN12
PEG_RXP13 PEG_RXN13 PEG_TXP13 PEG_TXN13
PEG_RXP14 PEG_RXN14 PEG_TXP14 PEG_TXN14
PEG_RXP15 PEG_RXN15 PEG_TXP15 PEG_TXN15
+VCCIO R541 24.9-1-04 PEG_RCOMP
PEG_RCOMP
DMI_RXP0 DMI_RXN0 DMI_TXP0 DMI_TXN0
DMI_RXP1 DMI_RXN1 DMI_TXP1 DMI_TXN1
DMI_RXP2 DMI_RXN2 DMI_TXP2 DMI_TXN2
DMI_RXP3 DMI_RXN3 DMI_TXP3 DMI_TXN3
3 OF 13
CFL_H_62_INT_IP_CRB_CFLH
CPU1D
DDI1_TXP_0 DDI1_TXN_0 DDI1_TXP_1 DDI1_TXN_1 DDI1_TXP_2 DDI1_TXN_2 DDI1_TXP_3 DDI1_TXN_3
EDP_TXP_0 EDP_TXN_0 EDP_TXP_1 EDP_TXN_1 EDP_TXP_2 EDP_TXN_2 EDP_TXP_3 EDP_TXN_3
EDP_TX0+ EDP_TX0- EDP_TX1+ EDP_TX1- EDP_TX2+ EDP_TX2- EDP_TX3+ EDP_TX3-
DDI1_AUXP DDI1_AUXN EDP_AUXP EDP_AUXN
EDP_AUX+ EDP_AUX-
DDI2_TXP_0 DDI2_TXN_0 DDI2_TXP_1 DDI2_TXN_1 DDI2_TXP_2 DDI2_TXN_2 DDI2_TXP_3 DDI2_TXN_3
EDP_DISP_UTIL
DISP_RCOMP D37 EDP_RCOMP R220 24.9-1-04 +VCCIO
DDI2_AUXP DDI2_AUXN
DDI3_TXP_0 DDI3_TXN_0 DDI3_TXP_1 DDI3_TXN_1 DDI3_TXP_2 DDI3_TXN_2 DDI3_TXP_3 DDI3_TXN_3
PROC_AUDIO_CLK PROC_AUDIO_SDI PROC_AUDIO_SDO
DDI3_AUXP DDI3_AUXN
PROC_AUDIO_SDO_R R504 20-04
PROC_AUDIO_CLK_CPU PROC_AUDIO_SDI_CPU PROC_AUDIO_SDO_CPU
4 of 13
CFL_H_62_INT_IP_CRB_CFLH
CPU1M
TP17 IST_TRIG_CPU
RSVD_TP5 IST_TRIG RSVD_TP4 RSVD_TP3
RSVD_TP1 RSVD_TP2
RSVD11 RSVD10
RSVD15
RSVD28 RSVD27 RSVD14 RSVD13
RSVD30 RSVD31 RSVD2 RSVD1 RSVD5 RSVD4
IDT A : del R219,R492 for space
GND POWER
VSS_A36 VSS_A37
12 PCH_2_CPU_TRIGGER 12 CPU_2_PCH_TRIGGER R357 @S0-04 short_0402 PROC_TRIGOUT
PROC_TRIGIN PROC_TRIGOUT
RSVD24 RSVD23
RSVD7 RSVD21
RSVD12 RSVD3 RSVD25
RSVD26 RSVD29
RSVD22 RSVD20 RSVD17 RSVD16 RSVD8 RSVD6
RSVD19 RSVD18 RSVD9
13 OF 13
CFL_H_62_INT_IP_CRB_CFLH
同方国际信息技术有限公司
Title
06_CPU CFL-H eDP/PEX/DMI/RSV
Size Custom
Document Number
GK5CXXT
Rev 1.0
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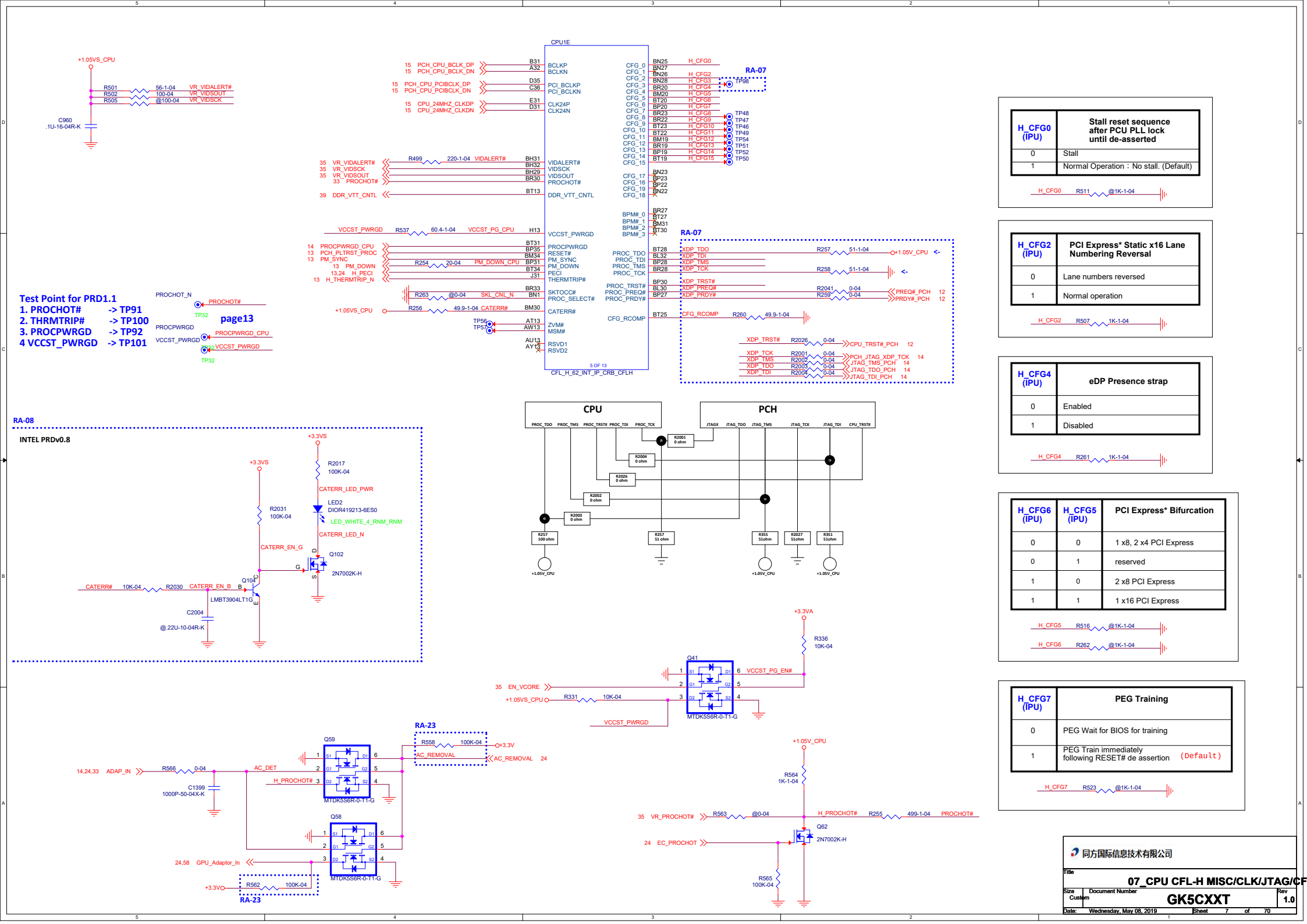
Test Point for PRD1.1
1. PROCHOT# -> TP91
2. THRMTRIP# -> TP100
3. PROCPWRGD -> TP92
4 VCCST_PWRGD -> TP101
page13
CPU1E
CFL_H_62_INT_IP_CRB_CFLH
RA-07
RA-08
RA-23
INTEL PRDv0.8
CPU
PCH
H_CFG0 (IPU) | Stall reset sequence after PCU PLL lock until de-asserted
0 | Stall
1 | Normal Operation：No stall. (Default)
H_CFG2 (IPU) | PCI Express* Static x16 Lane Numbering Reversal
0 | Lane numbers reversed
1 | Normal operation
H_CFG4 (IPU) | eDP Presence strap
0 | Enabled
1 | Disabled
H_CFG6 (IPU) | H_CFG5 (IPU) | PCI Express* Bifurcation
0 | 0 | 1 x8, 2 x4 PCI Express
0 | 1 | reserved
1 | 0 | 2 x8 PCI Express
1 | 1 | 1 x16 PCI Express
H_CFG7 (IPU) | PEG Training
0 | PEG Wait for BIOS for training
1 | PEG Train immediately following RESET# de assertion (Default)
同方国际信息技术有限公司
07_CPU CFL-H MISC/CLK/JTAG/CF
GK5CXXT
Size: Custom
Rev: 1.0
Date: Wednesday, May 08, 2019
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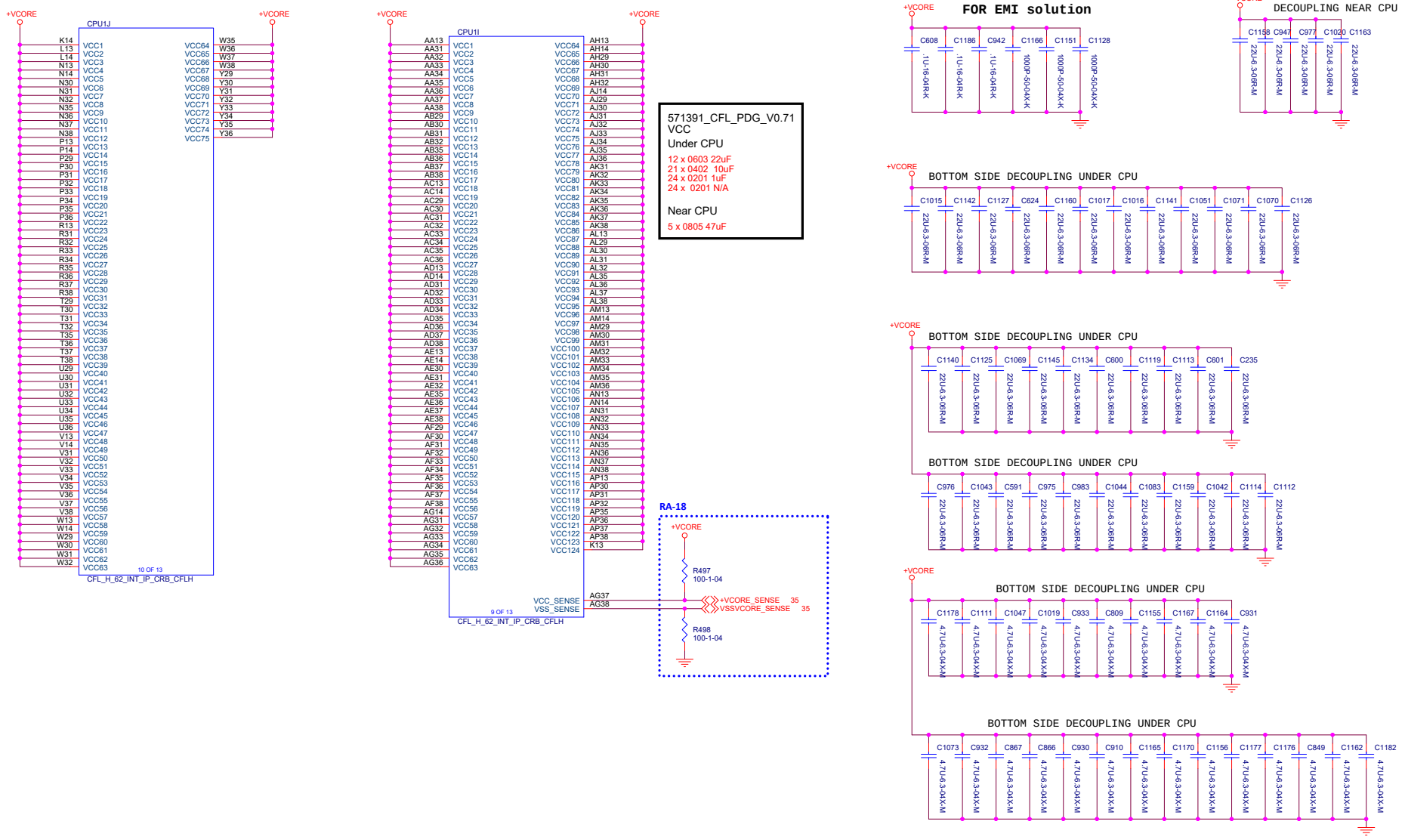

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Title	08_CPU CFL-H VCORE	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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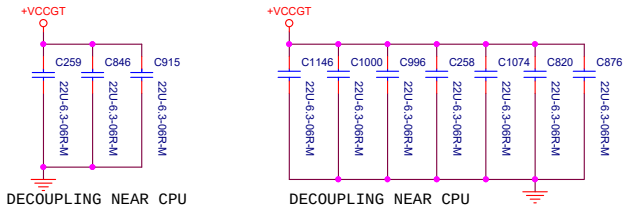
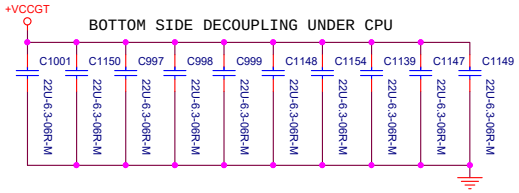
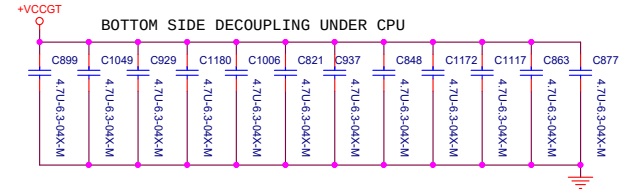
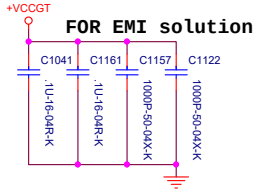








571391_CFL_PDG_V0.71
VCCGT

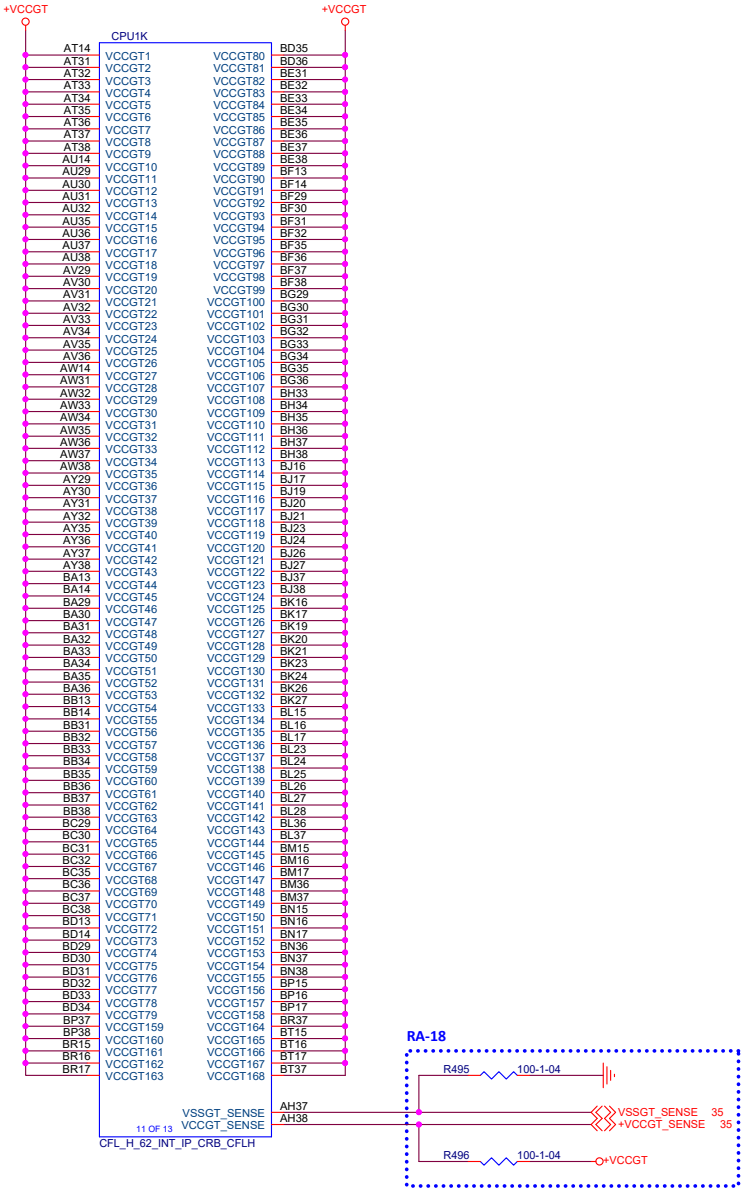
Under CPU

10 x 0402 10uF
12 x 0201 1uF

Near CPU

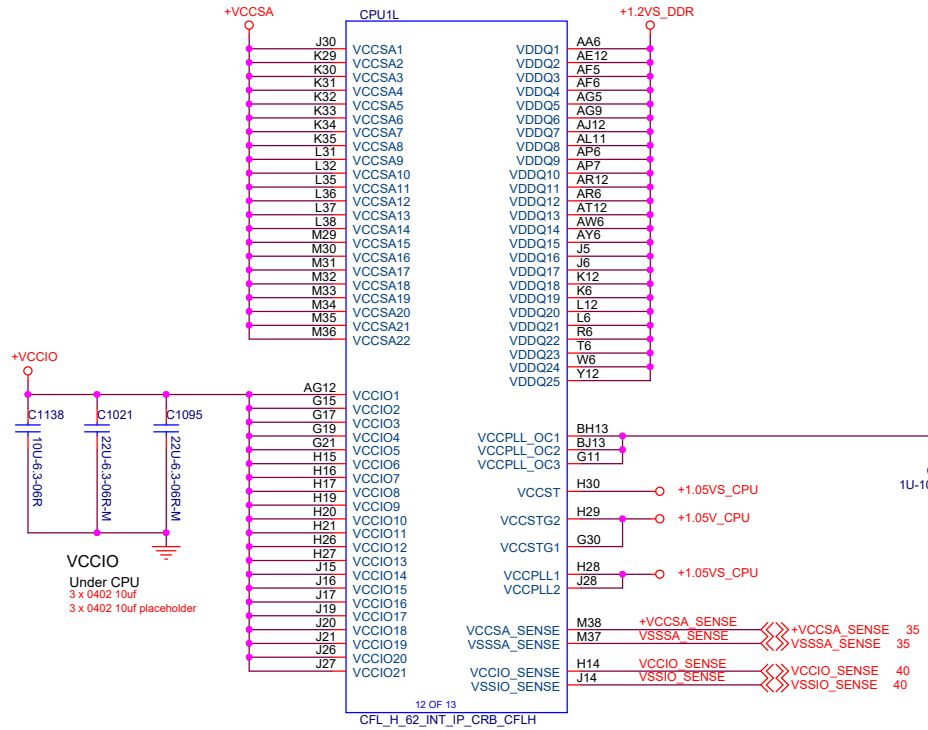
3 x 0805 47uF
7 x 0603 22uF

GT
Page 9 : 22u * 20 + 4.7u * 12 = 496.4uF
Page 36 : 22u*6 =132uF
Tatal : 628.4uF (spec : 990uF)



同方国际信息技术有限公司

Title	09_CPU CFL-H VCCGT	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 9 of 70	



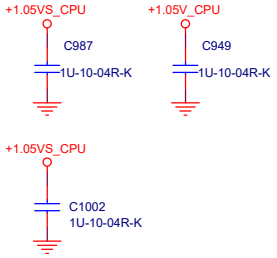
VCCIO
Under CPU
3 x 0402 10uf
3 x 0402 10uf placeholder

VCCST
Under CPU
1 x 0201 1uF

VCCSTG
Under CPU
1 x 0201 1uF

VCCPLL
Under CPU
1 x 0201 1uF

VCCPLL_OC
Under CPU
2 x 0201 1uF



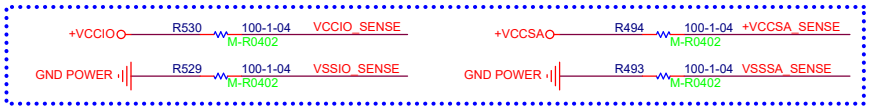
VCCPLL_OC:
CPU digital PLL power rails
VCCPLL:
CPU PLL power rails

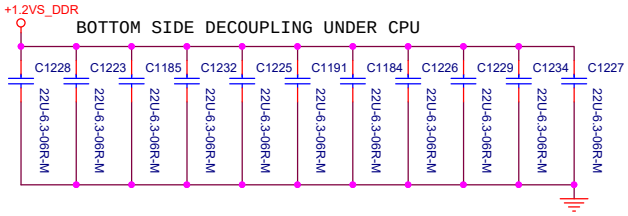
VCCST:
Sustain voltage for processor
in Standby modes
VCCSTG:
Gated version of VCCST

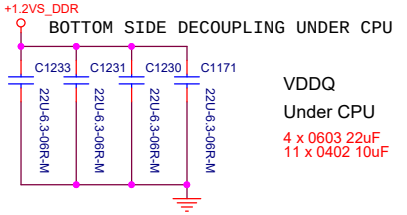
(1)VCCPLL is allowed to be OFF in S3, but it is generally assumed to be ON since it is powered from the same source as VCCST.

(2) VCCPLL_OC is allowed to be turned off during S3 if it is not powered directly from VDDQ

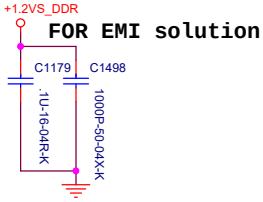
RA-18

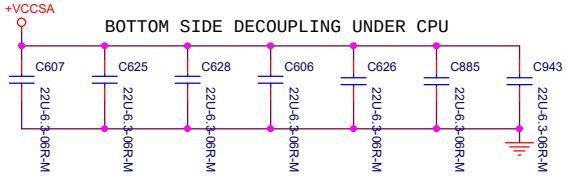




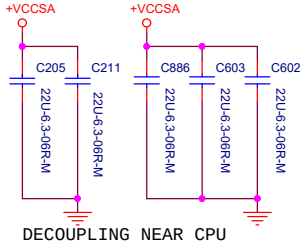


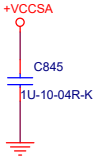
VDDQ
Under CPU
4 x 0603 22uF
11 x 0402 10uF

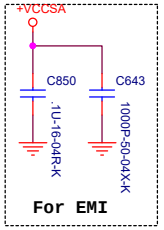




VCCSA
Under CPU
7 x 0402 10uF
1 x 0201 1uF
Near CPU
2 x 0805 47uF
7 x 0603 22uF







SA
Page 10 : 22u * 12 =264uF
Page 36 : 22u * 4 =88uF
Tatal : 352uF (spec : 220uF)

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Title	10_CPU CFL-H VCCSA/VCCIO/VDD	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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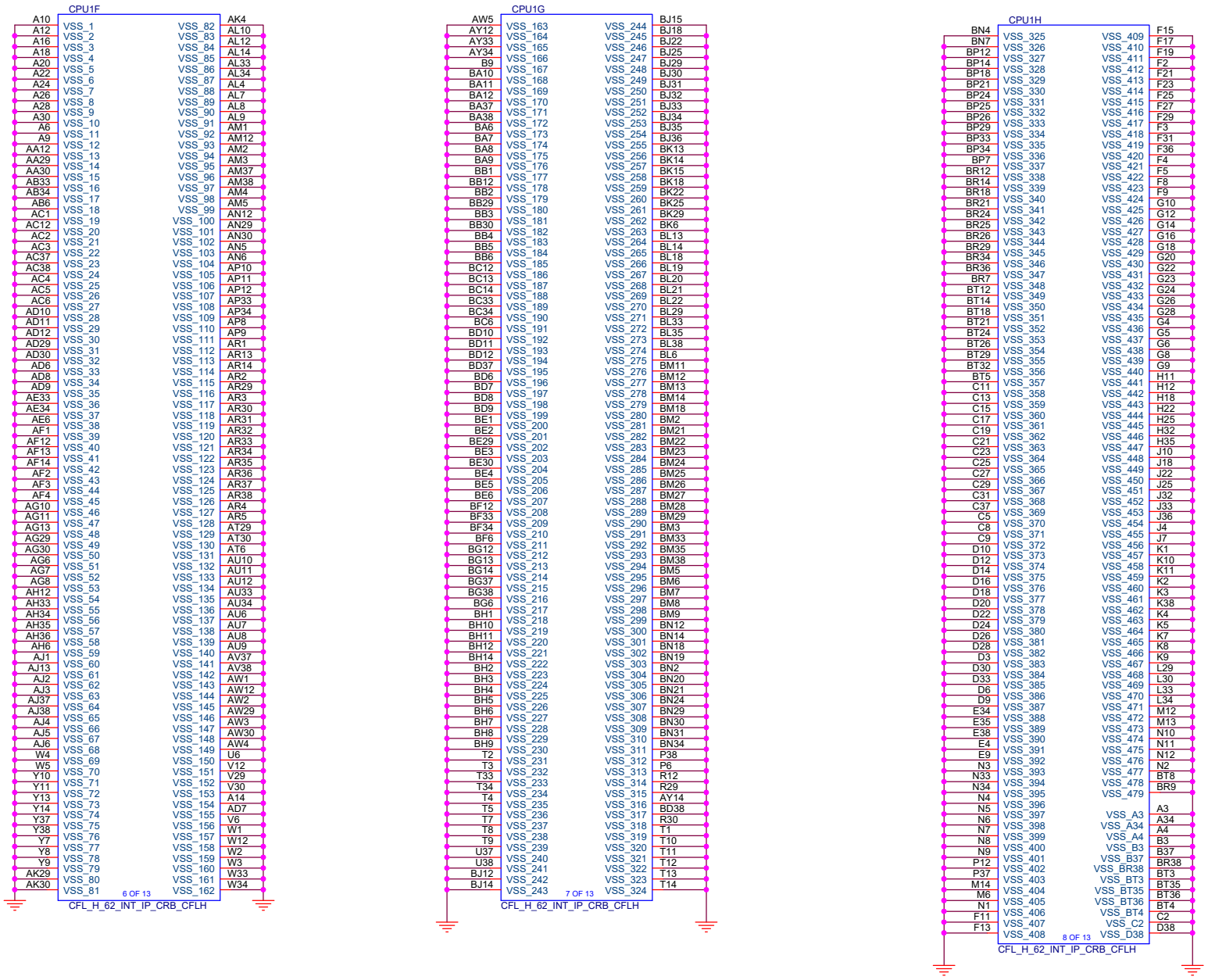

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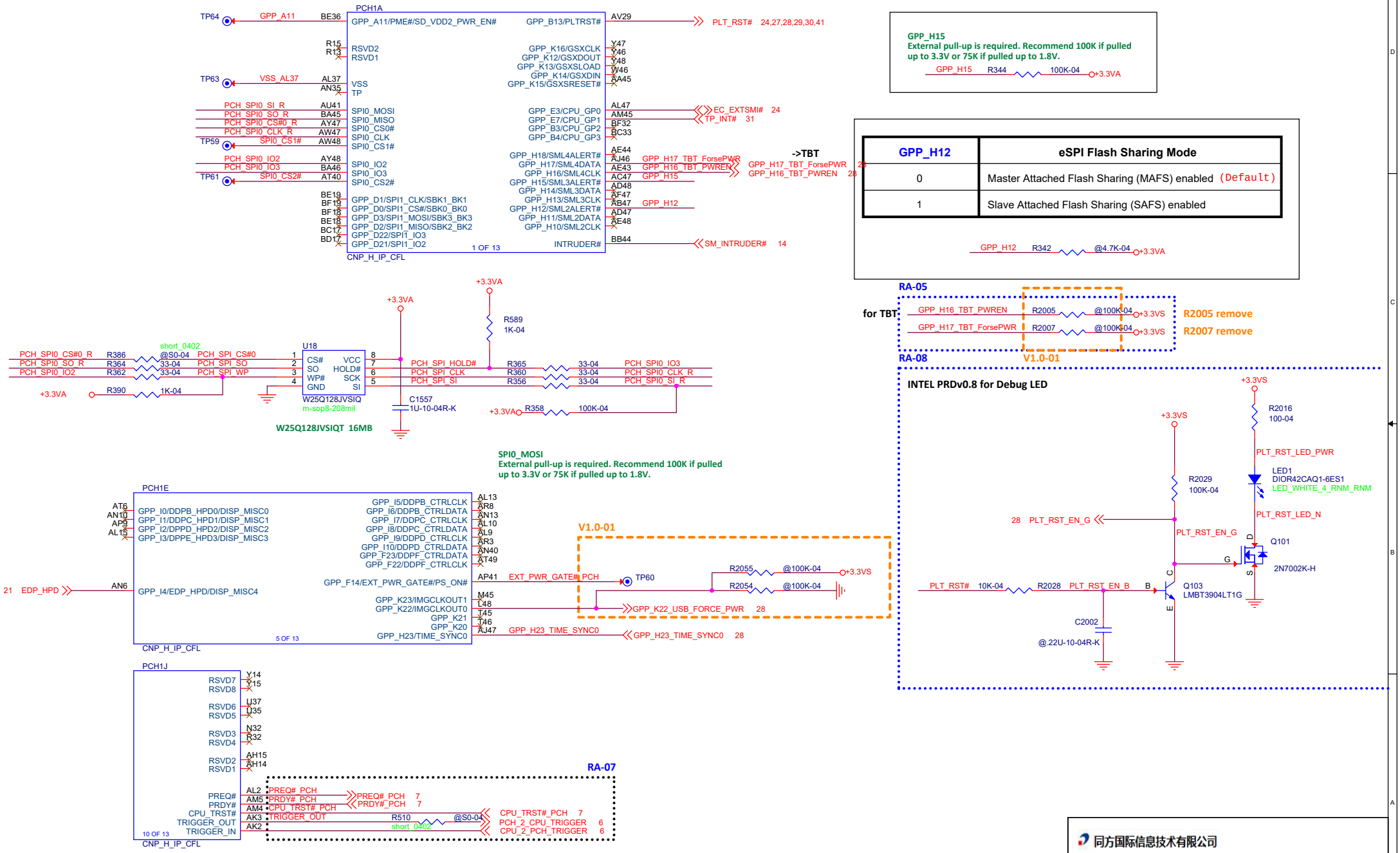
Title	11_CPU CFL-H GND	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 11 of 70	



GPP_H12	eSPI Flash Sharing Mode
0	Master Attached Flash Sharing (MAFS) enabled (Default)
1	Slave Attached Flash Sharing (SAFS) enabled

同方国际信息技术有限公司

Title	12_PCH CFL-H SPI/DDI CTRL/RSVD	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Monday, May 13, 2019	Sheet 12 of 70	

USB2.0 Configuration Table	
USB1	TYPE-C Port
USB2	CardReader on USB3.0 DB
USB3	N/A
USB4	USB3.0 Port1 on USB3.0 DB
USB5	N/A
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	USB3.0 Port2 on USB3.0 DB
USB10	N/A
USB11	N/A
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

PCIE Configuration Table		
PCIE9		
PCIE10	SSD2	RST PCIE*4
PCIE11		
PCIE12		
PCIE13	SATA0B	
PCIE14	LAN	
PCIE15	WLAN	
PCIE16	N/A	
PCIE17		
PCIE18	Thunderbolt	PCIE*4
PCIE19		
PCIE20		
PCIE21		
PCIE22	SSD1	RST PCIE*4
PCIE23		
PCIE24		

No function
USB31_9-10
PCIE_1-8
HM370

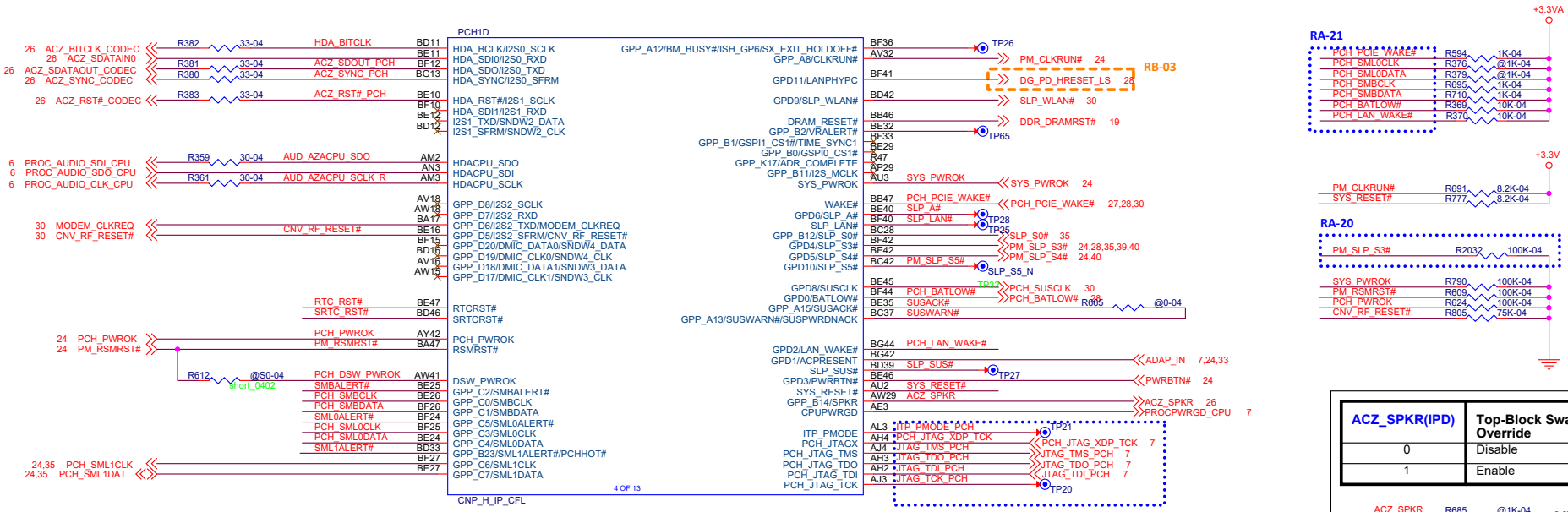
don't use (change to thunderbolt3)

GPD7 Reserved
External pull-up is required. Recommend 100K.

SSD1
SSD2
LAN
HDD
SSD2
Thunderbolt
SSD2
WIFI
Thunderbolt

Title	13_PCH CFL-H DMI/PCIE/USB2/SAT
Size: Custom	Document Number: GK5CXXT
Rev	1.0
Date: Wednesday, May 08, 2019	Sheet 13 of 70

同方国际信息技术有限公司



HDA_SDO (IPD)	Flash Descriptor Security Override
0	ME Enable security (Default)
1	ME Disabled security

ACZ_SPKR(IPD)	Top-Block Swap Override
0	Disable
1	Enable

SMBALERT#(IPD)	Intel ME Crypto Transport Layer Security Confidentiality (TLS)
0	Disable (Default)
1	Enable

SML0ALERT#(IPD)	eSPI&LPC Select
0	LPC (Default)
1	eSPI

SML1ALERT#(IPD)	IntelR DCI-OOB
0	Disable (Default)
1	Enable

SUS Battery

CLEAR CMOS

Test Point for PRD1.1

5. SYS_PWROK ->TP93
6. PCH_PWROK ->TP94
7. DSW_PWROK ->TP95
8. SLP_S0# ->TP96
9. SLP_S3# ->TP99
10. SLP_S4# ->TP97
11. SLP_S5# ->TP30
12. CPU_C10_GATE# ->TP24

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page16

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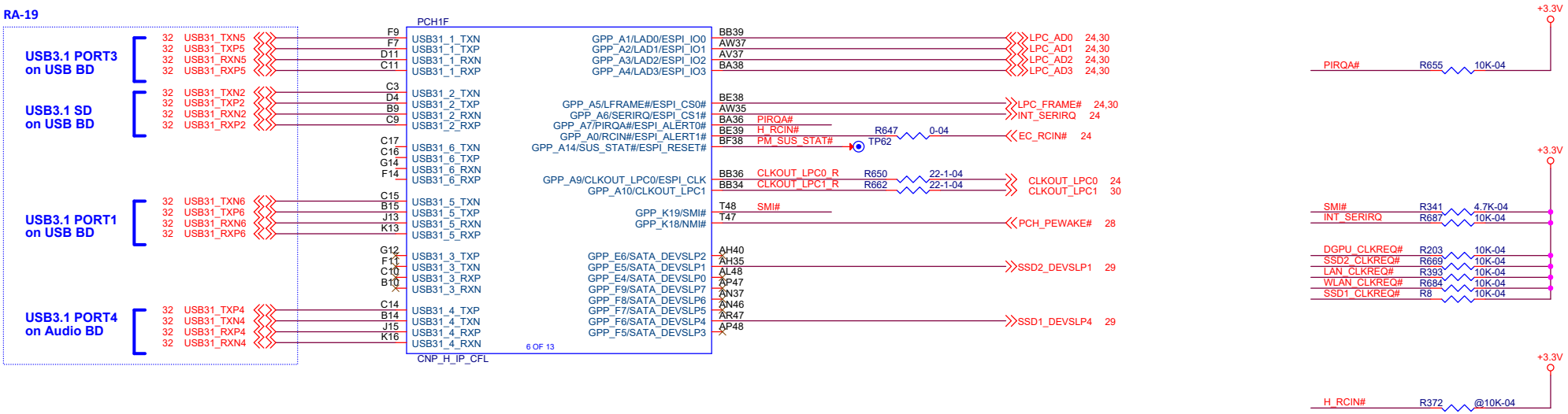
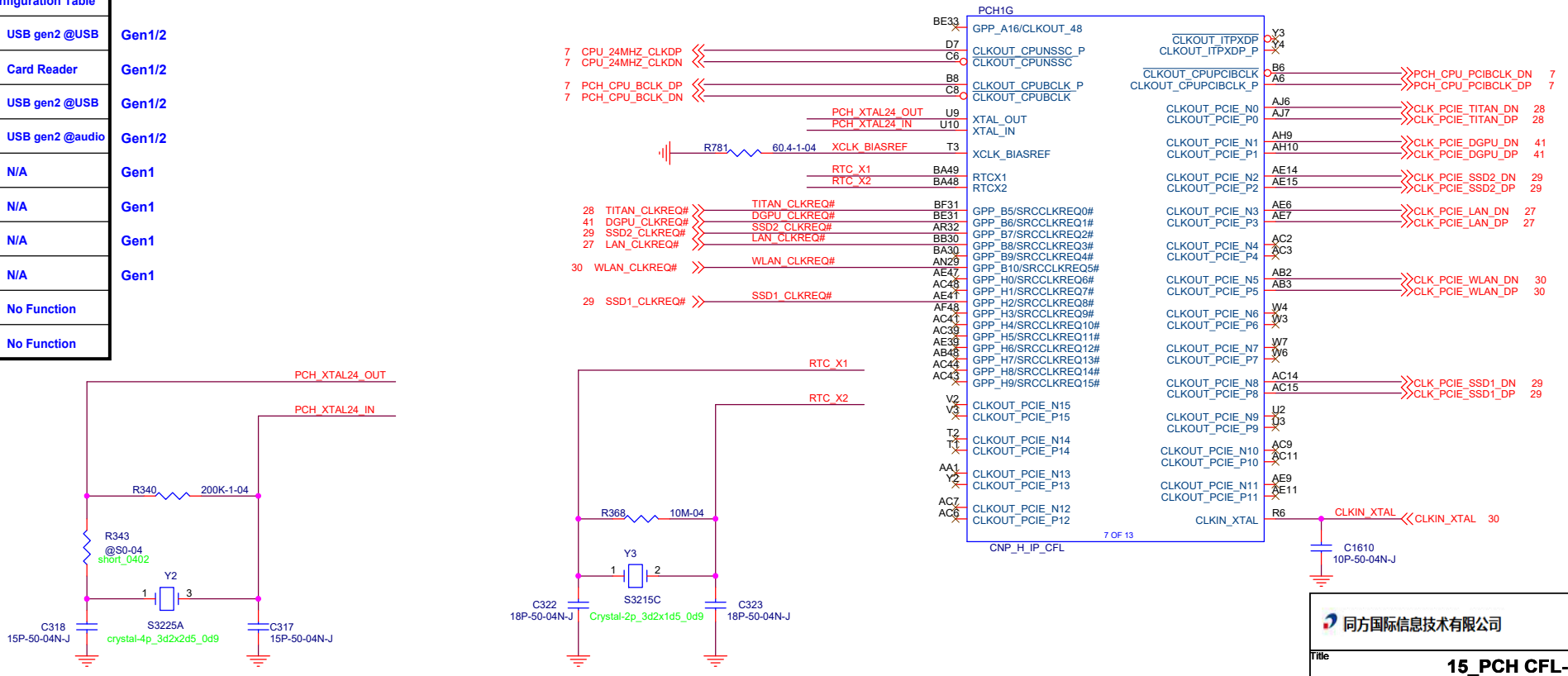
Title	14_PCH CFL-H PM/HDA/SMBUS/RT	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 14 of 70	



USB3.0 Configuration Table		
USB3_1	USB gen2 @USB	Gen1/2
USB3_2	Card Reader	Gen1/2
USB3_3	USB gen2 @USB	Gen1/2
USB3_4	USB gen2 @audio	Gen1/2
USB3_5	N/A	Gen1
USB3_6	N/A	Gen1
USB3_7	N/A	Gen1
USB3_8	N/A	Gen1
USB3_9	No Function	
USB3_10	No Function	



同方国际信息技术有限公司

Title	15_PCH CFL-H CLK/USB3/LPC	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 15 of 70	

GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Destination
0	SPI (Default)
1	LPC

+3.3V R694 @150K-04 PCH_GSPI1_SI_R

GPP_B18/GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable

+3.3V R373 @4.7K-04 GPP_B18

CNV_BRI_DT (IPD)	XTAL Frequency Select
0	38.4MHz XTAL frequency
1	24MHz XTAL frequency (Default)

+VCCPRIM_1P8 R796 10K-04 CNV_BRI_DT_PCH

CNV_RGI_DT	M.2 CNV Mode Select
0	Integrated CNVi enable
1	Integrated CNVi disable

+VCCPRIM_1P8 R795 20K-04 CNV_RGI_DT_PCH

R366 @100K-04

Close to CNVi module

GPP_J9	VCCPSPI Rail select
0	VCCSPI is connected to 3.3V
1	VCCSPI is connected to 1.8V

+VCCPRIM_1P8 R753 @4.7K-04 GPP_J9

PCH1K

39 MEM_OVERCLK_EN R865 @S0-04 short_0402 PCH_GSPI1_SI_R

67 OVRM_TGP_SEL R862 @S0-04 short_0402 GPP_B18

24 SMC_WAKE_SCI#

64,66 FBVDDQ_PG_1V8Aon_GC6

24,66 DGPU_PWR_ON

30 UART2_DEBUG_TXD

30 UART2_DEBUG_RXD

58 GPU_EVENT#_GC6

41 DGPU_RST#

31 TP_I2C0_SCL

31 TP_I2C0_SDA

R732 100K-04

GPP_B22/GSPI1_MOSI, GPP_B21/GSPI1_MISO, GPP_B20/GSPI1_CLK, GPP_B19/GSPI1_CS0#

GPP_B18/GSPI0_MOSI, GPP_B17/GSPI0_MISO, GPP_B16/GSPI0_CLK, GPP_B15/GSPI0_CS0#

GPP_C9/UART0_TXD, GPP_C8/UART0_RXD, GPP_C11/UART0_CTS#, GPP_C10/UART0_RTS#

GPP_C15/UART1_CTS#/ISH_UART1_CTS#, GPP_C14/UART1_RTS#/ISH_UART1_RTS#, GPP_C13/UART1_TXD/ISH_UART1_TXD, GPP_C12/UART1_RXD/ISH_UART1_RXD

GPP_C23/UART2_CTS#, GPP_C22/UART2_RTS#, GPP_C21/UART2_TXD, GPP_C20/UART2_RXD

GPP_C19/I2C1_SCL, GPP_C18/I2C1_SDA, GPP_C17/I2C0_SCL, GPP_C16/I2C0_SDA

GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4, GPP_D23/ISH_I2C2_SCL/I2C3_SCL

11 OF 13

CNP_H_IP_CFL

GPP_D9/ISH_SPI_CS#/GSPI2_CS0#, GPP_D10/ISH_SPI_CLK/GSPI2_CLK, GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO, GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI

GPP_D16/ISH_UART0_CTS#/CNV_WCEN, GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN, GPP_D14/ISH_UART0_TXD/I2C2_SCL, GPP_D13/ISH_UART0_RXD/I2C2_SDA

TBT_SML1CLK 28

TBT_SML1DAT 28

GPP_H20/ISH_I2C0_SCL, GPP_H19/ISH_I2C0_SDA

GPP_H22/ISH_I2C1_SCL, GPP_H21/ISH_I2C1_SDA

GPP_A23/ISH_GP5, GPP_A22/ISH_GP4, GPP_A21/ISH_GP3, GPP_A20/ISH_GP2, GPP_A19/ISH_GP1, GPP_A18/ISH_GP0

GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7

BIOS_LOCKDOWN

BIOS_NORMAL

R2042 100K-1-04

R2043 100K-1-04

BIOS Security	NORMAL	Lockdown	Recovery
GPP_A18	1	0	0
GPP_A19	0	1	0

RA-11

+3.3V +3.3VA

R759 10K-04

R783 @10K-04

R2044 @0-04

CNBIOS1

BIOS_NORMAL

BIOS_LOCKDOWN

CONRCC0034-A8S1

CON header 3p2 H5.4 190115 ACES

PCH1M

GPP_G0/SD_CMD, GPP_G1/SD_D0, GPP_G2/SD_D1, GPP_G3/SD_D2, GPP_G4/SD_D3, GPP_G5/SD_CD#, GPP_G6/SD_CLK, GPP_G7/SD_WP

GPP_I11/M2_SKT2_CFG0, GPP_I12/M2_SKT2_CFG1, GPP_I13/M2_SKT2_CFG2, GPP_I14/M2_SKT2_CFG3

GPP_J0/CNV_PA_BLANKING, GPP_J1/CPU_VCCIO_PWR_GATE#, GPP_J11/A4WP_PRESENT, GPP_J10, GPP_J_2, GPP_J_3, GPP_J_4_CNV_BRI_DT_UART0_RTSB, GPP_J5/CNV_BRI_RSP/UART0_RXD, GPP_J6/CNV_RGI_DT/UART0_TXD, GPP_J7/CNV_RGI_RSP/UART0_CTS#, GPP_J8/CNV_MFUART2_RXD, GPP_J9/CNV_MFUART2_TXD

13 OF 13

CNP_H_IP_CFL

+VCCPRIM_1P8

R855 20K-04 CNV_BRI_RSP

R854 20K-04 CNV_RGI_RSP

CPU_C10_GATE_N VCCIO_PWR_GATE#

30 CNV_BRI_DT R363 33-04 CNV_BRI_DT_PCH

30 CNV_BRI_RSP

30 CNV_RGI_DT R367 33-04 CNV_RGI_DT_PCH

30 CNV_RGI_RSP

GPP_J9

CNV_WR_CLKN, CNV_WR_CLKP

CNV_WR_D0N, CNV_WR_D0P, CNV_WR_D1N, CNV_WR_D1P

CNV_WT_CLKN, CNV_WT_CLKP

CNV_WT_D0N, CNV_WT_D0P, CNV_WT_D1N, CNV_WT_D1P

CNV_WT_RCOMP R780 150-1-04

PCIE_RCOMPN, PCIE_RCOMPP R338 100-1-04

SD_RCOMP_1P8 R779 200-1-04

SD_RCOMP_3P3 R760 200-1-04

GPPJ_RCOMP_1P8 R778 200-1-04

GPPJ_RCOMP_1P81, GPPJ_RCOMP_1P82, GPPJ_RCOMP_1P83

RSVD2, RSVD3, RSVD1, TP

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Title	16_PCH CFL-H CNVi/UART/I2C	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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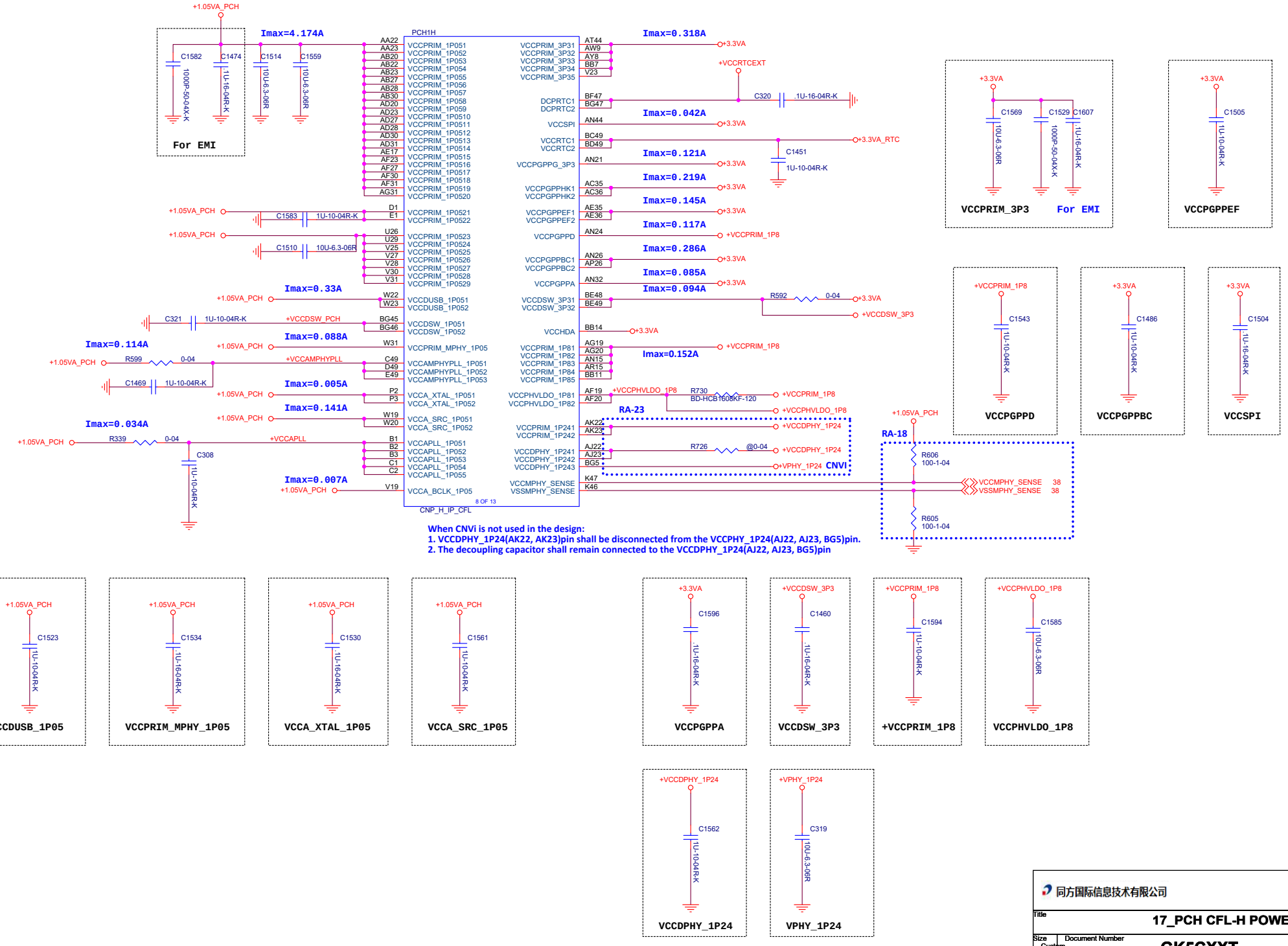

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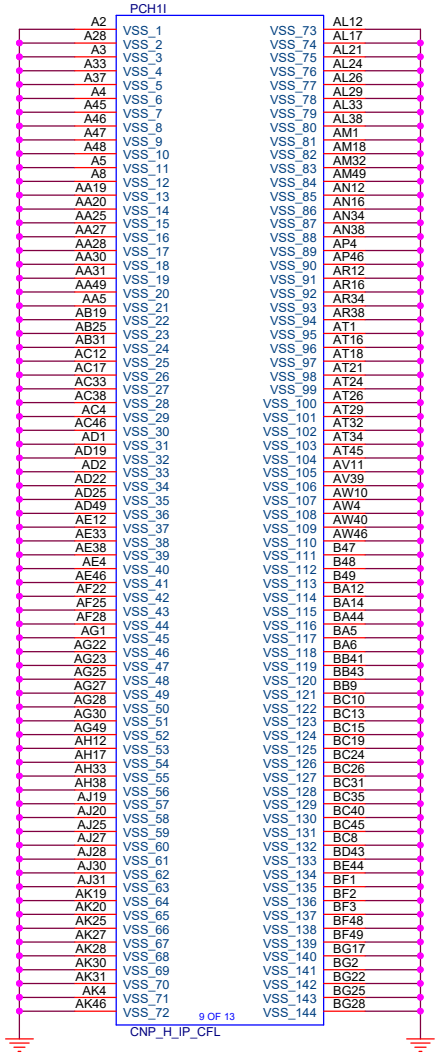
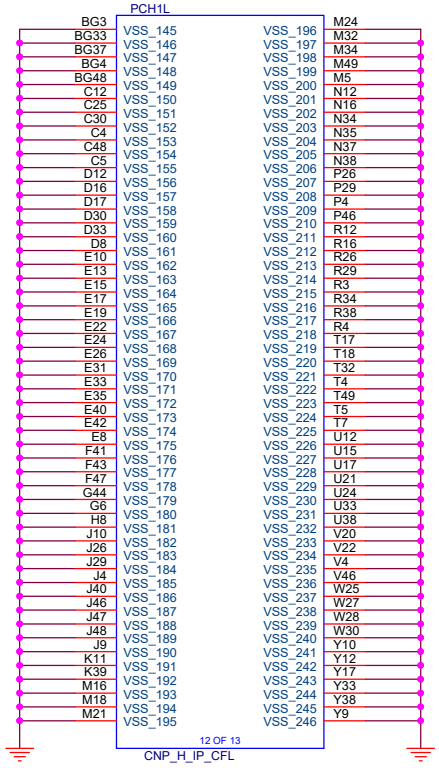
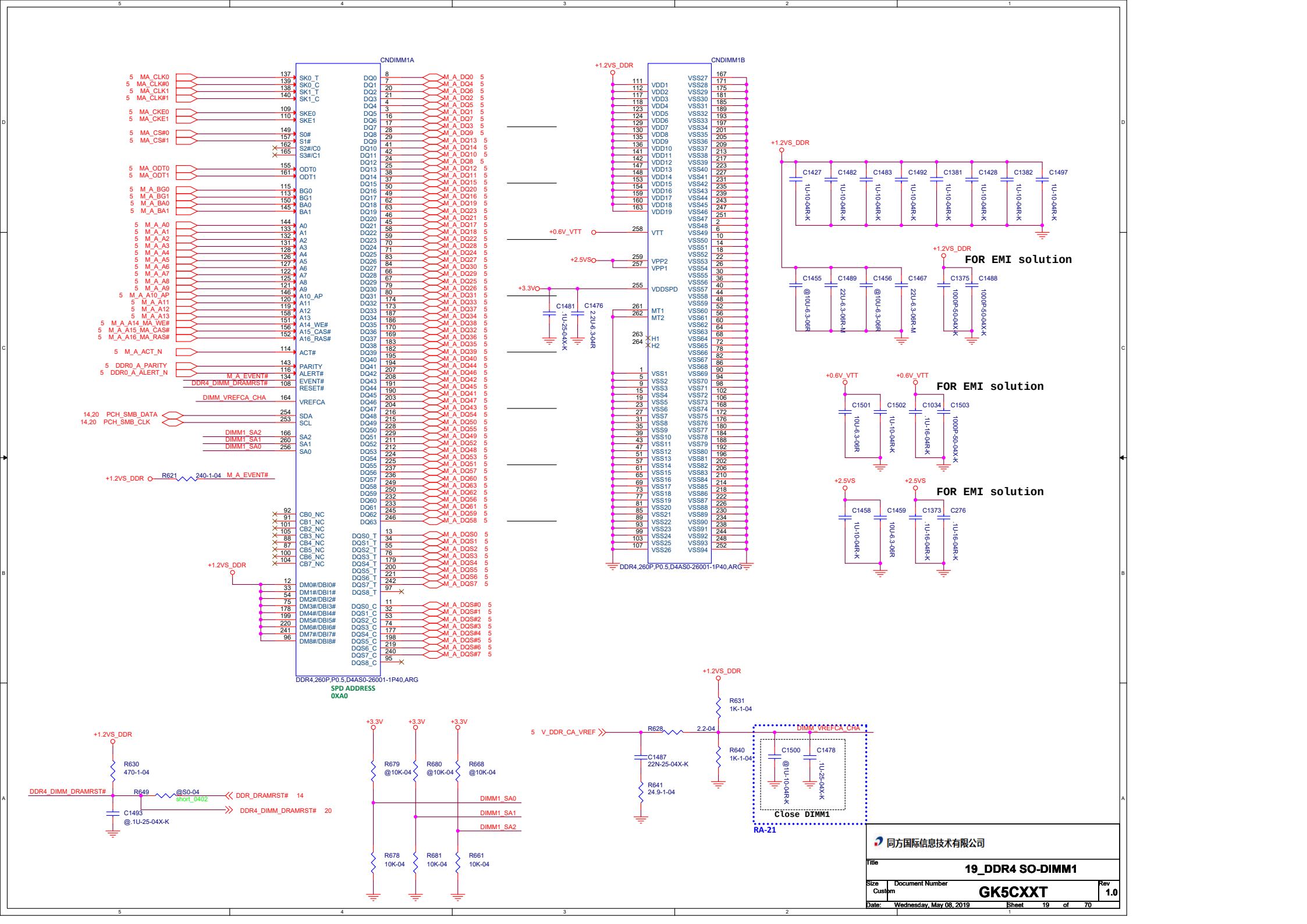
Title	17_PCH CFL-H POWER	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 17 of 70	

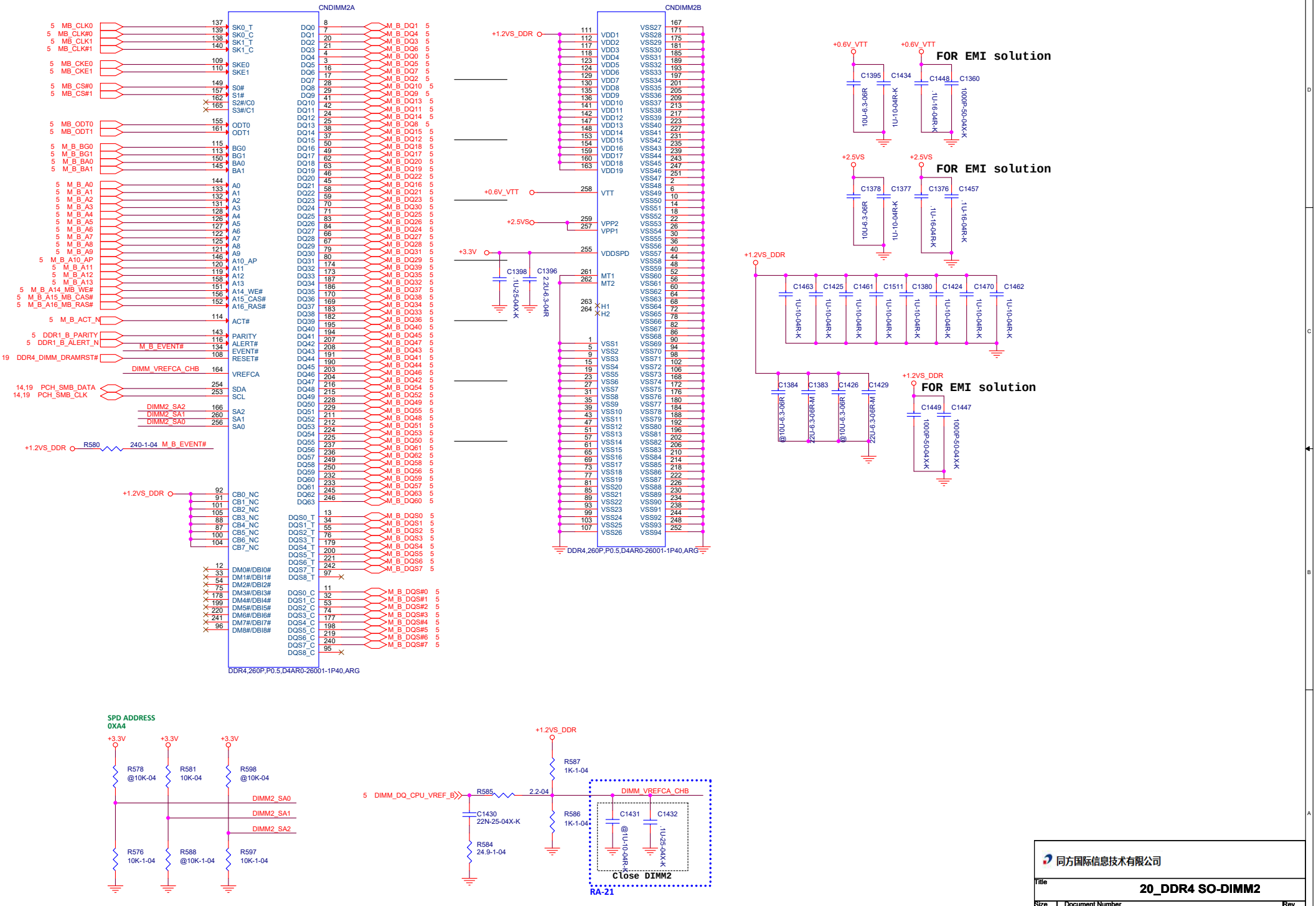




同方国际信息技术有限公司

Title	18_PCH CFL-H GND	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 18 of 70	


CNDIMM1A
CNDIMM1B
DDR4,260P,P0.5,D4AS0-26001-1P40,ARG
SPD ADDRESS
0XA0
FOR EMI solution
FOR EMI solution
FOR EMI solution
Close DIMM1
RA-21
同方国际信息技术有限公司
19_DDR4 SO-DIMM1
GK5CXXT
1.0
Wednesday, May 08, 2019
19
70



同方国际信息技术有限公司	
Title	20_DDR4 SO-DIMM2
Size: Custom	Document Number: GK5CXXT
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EMFA0P02J MOS SPEC
ID=-3A, 100 miniOHM@Pulse width=300us

+5VA
Q55
EMFA0P02J
A_Cover LED_BL
R450 100K-04
C540 33P-50-04N-J
Q54 2N7002K-H
A_COVER_LED 24

6 EDP_TX3- C196 .1U-16-04R-K EDP_TXN3_CONN
6 EDP_TX3+ C195 .1U-16-04R-K EDP_TXP3_CONN
6 EDP_TX2- C190 .1U-16-04R-K EDP_TXN2_CONN
6 EDP_TX2+ C187 .1U-16-04R-K EDP_TXP2_CONN
6 EDP_TX1- C184 .1U-16-04R-K EDP_TXN1_CONN
6 EDP_TX1+ C180 .1U-16-04R-K EDP_TXP1_CONN
6 EDP_TX0- C176 .1U-16-04R-K EDP_TXN0_CONN
6 EDP_TX0+ C168 .1U-16-04R-K EDP_TXP0_CONN
6 EDP_AUX- C163 .1U-16-04R-K EDP_AUXN_CONN
6 EDP_AUX+ C158 .1U-16-04R-K EDP_AUXP_CONN

12 EDP_HPD
R472 100K-04
+VIN_LCD
R1.0-03
PS1 SPR-P260T
+VIN_LCD_CN

+3.3V
24 EC_BL_ON
13,24 PCH_LCDBKL_EN
U21 74AHC1G08GW
BL_ON
R459 100K-04

26 DMIC_DATA_L B19 FCM1005KF-301T01 DMIC_DATA_L_CN
26 DMIC_CLK_L B20 FCM1005KF-301T01 DMIC_CLK_L_CN

13 USB_PP13
13 USB_PN13
R453 @0-04
L37 QTCW2012EH4-120-LF
R454 @0-04
WEBCAM_USB+
WEBCAM_USB-

RA-10
CNEDP1
EDP_TXN3_CONN
EDP_TXP3_CONN
EDP_TXN2_CONN
EDP_TXP2_CONN
EDP_TXN1_CONN
EDP_TXP1_CONN
EDP_TXN0_CONN
EDP_TXP0_CONN
EDP_AUXN_CONN
EDP_AUXP_CONN
S1
S2
+3.3V_LCD
edp 3.3V gnd
EDP_HPD
BL GND
BL_ON
A_Cover LED_BL
PCH_LCDBKL_PWM
+VIN_LCD_CN
DMIC_DATA_L_CN
DMIC_CLK_L_CN
+3.3VO
D-MIC DB 3.3V POWER
Camera GND
WEBCAM_USB+
WEBCAM_USB-
+WEBCAM_PWR
TP72
C574 33P-50-04N-J
FFC,40P,P0.5H1.75,5151704001001,ACES
CON_FFC_40R05-51517_ACES

+3.3V
+3.6V_LCD
B23 @BD-HCB1608KF-300T30
B22 BD-HCB1608KF-300T30
+3.3V_LCD
C571 22U-6.3-04R
C565 22U-6.3-04R
C552 .1U-16-04R-K

RA-10
+3.3VA
R218 @100K-04
Q30
21,24,40 RUN_ON
+3.3VO
R217 @0-04
@MTDK5S6R-0-T1-G

+3.3VA
R481 100K-04
Q57
21,24,40 RUN_ON
+3.3V_LCD
R483 10-04
MTDK5S6R-0-T1-G
RA-10

+5VO
+3.3V
B21 @0-06
PS2 SPR-P110-6V-1.1A-0805
+WEBCAM_PWR

IDT A : del R473 for space
13 PCH_LCDBKL_PWM
PCH_LCDBKL_PWM
S15 @SCON2S
EDP_HPD
S16 @SCON2S

+VIN
B18 BD-HCB1608KF-300T30
+VIN_LCD_IN
Q51 MTP5103N3
+VIN_LCD
R447 10K-1-04
R448 10K-1-04
R452 100-1-04
C537 1U-25-0MX-K
C531 1U-25-06R-K
VIN_LCD DISCHARGE

24,38 LVDS_VIN
R449 220K-1-04
Q53 MTDK5S6R-0-T1-G
C525 1U-10-04R-K
LVDS_VIN#

DMIC_DATA_L_CN
DMIC_CLK_L_CN
DMIC_DATA_L
DMIC_CLK_L
C539 @1U-16-04R-K
C538 @1U-16-04R-K
TVS5 ESD5302N

WEBCAM_USB-
WEBCAM_USB+
TVS6 ESD5302N

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Title	21_eDP Pannel/CAMERA	
Size C	Document Number GK5CXXT	Rev 1.0
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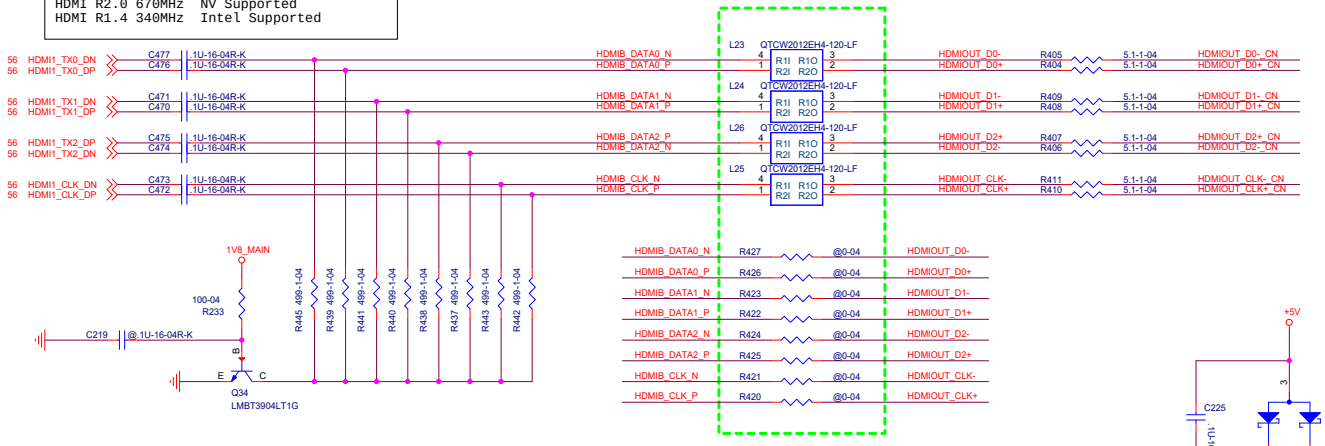
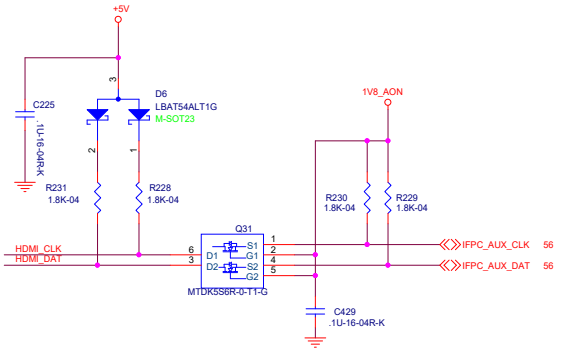
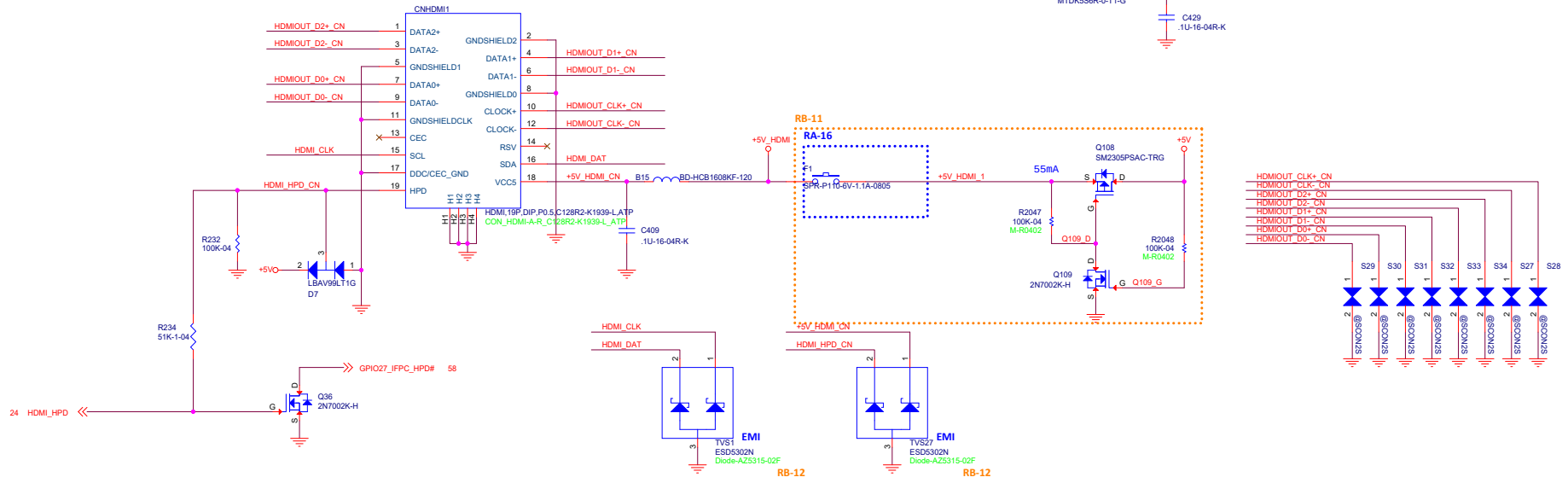
HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

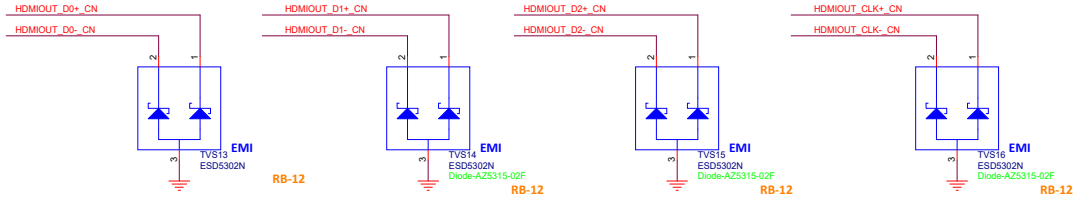
HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported





HDMI CONN





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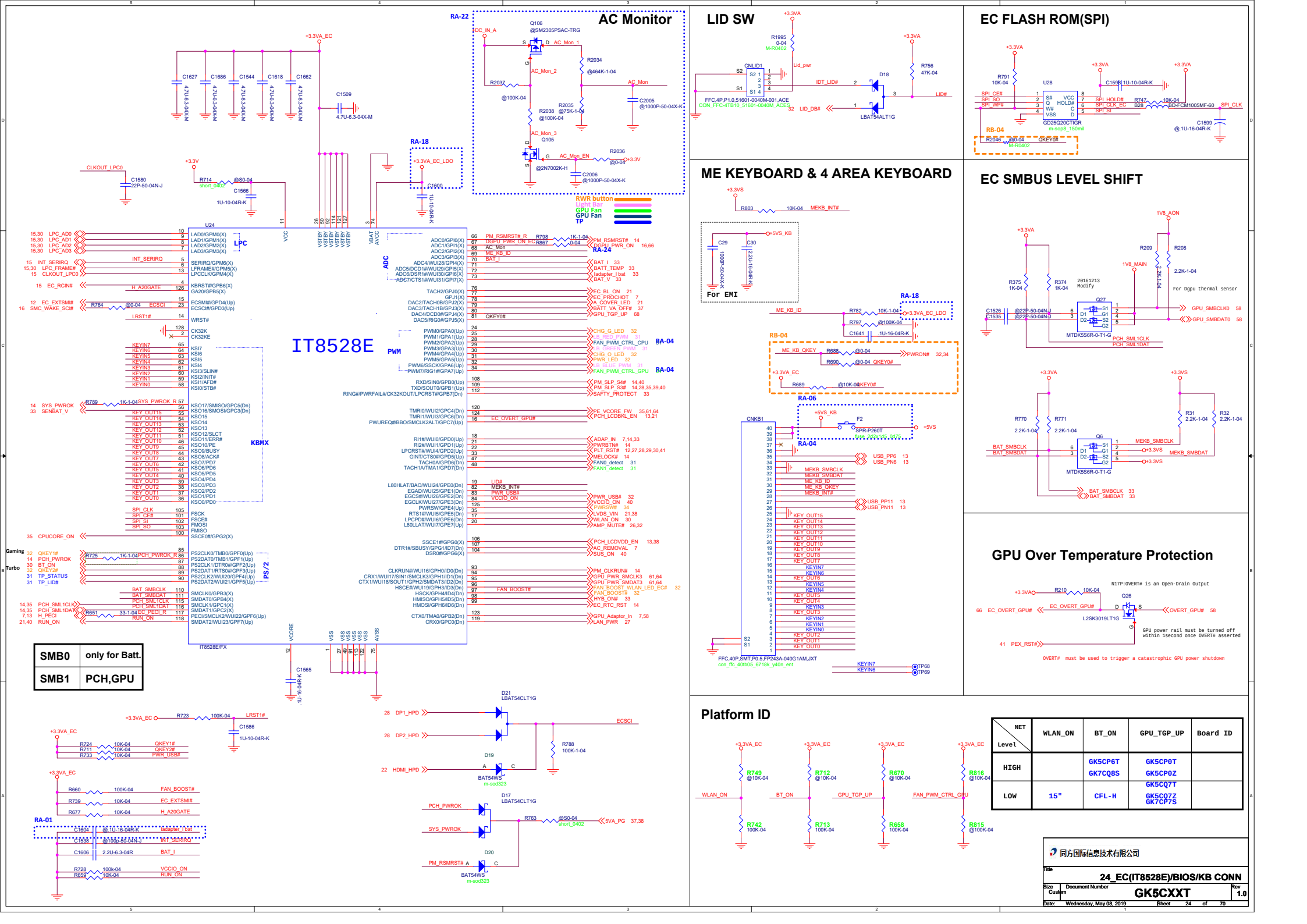
Title	22_HDMI	
Size C	Document Number GK5CXXT	Rev 1.0
Date: Tuesday, May 14, 2019	Sheet 22 of 70	

[redacted]

Size: A	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 1 of 1	


AC Monitor
LID SW
EC FLASH ROM(SPI)
ME KEYBOARD & 4 AREA KEYBOARD
EC SMBUS LEVEL SHIFT
GPU Over Temperature Protection
Platform ID
IT8528E
LPC
KBMX
PS/2
ADC
PWM
RA-22
RA-18
RA-24
RA-04
RA-06
RB-04
RA-01
RWR button
Light Bar
GPU Fan
GPU Fan
TP
For EMI
For Dgpu thermal sensor
SMB0 only for Batt.
SMB1 PCH,GPU
同方国际信息技术有限公司
24_EC(IT8528E)/BIOS/KB CONN
GK5CXXT
1.0
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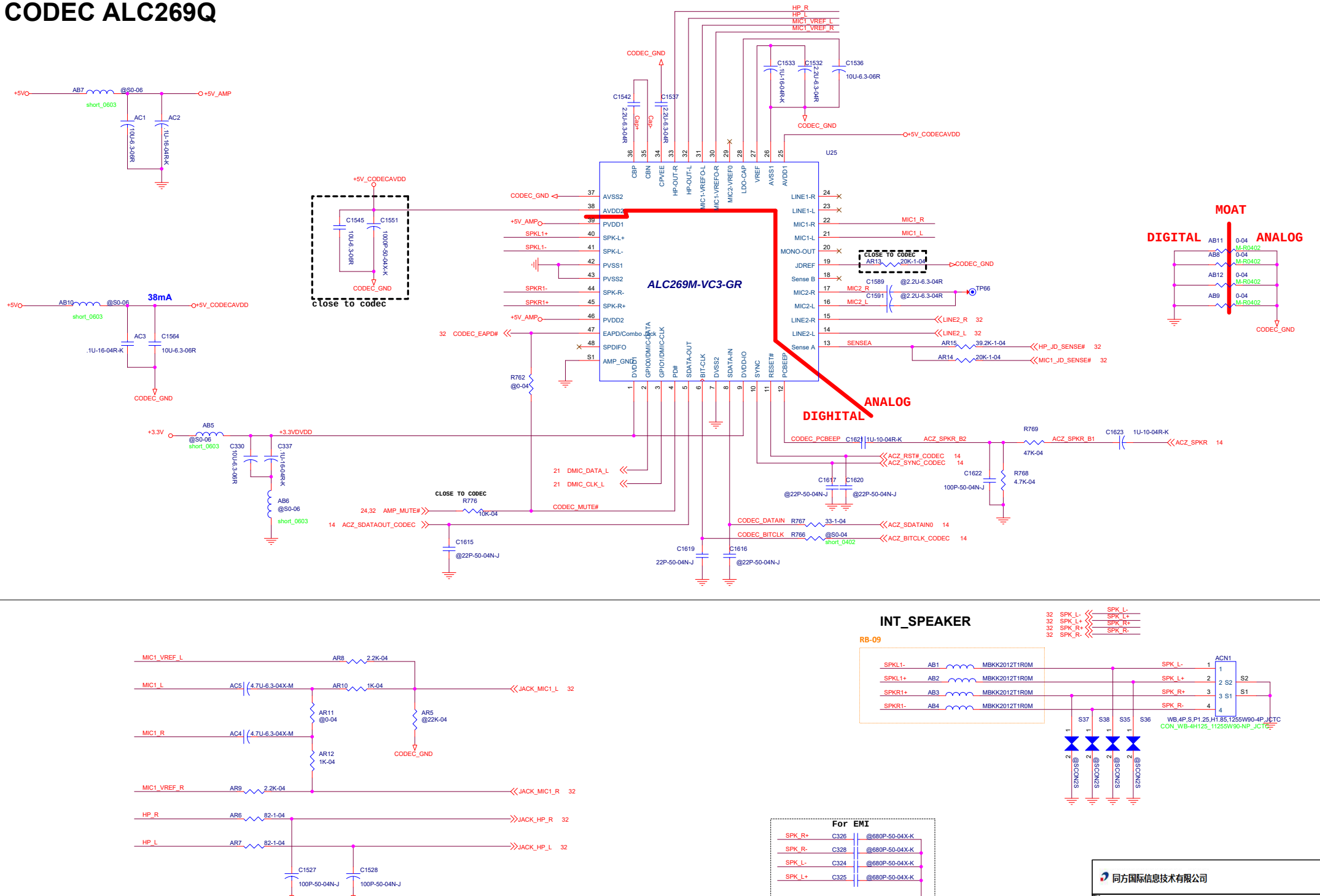
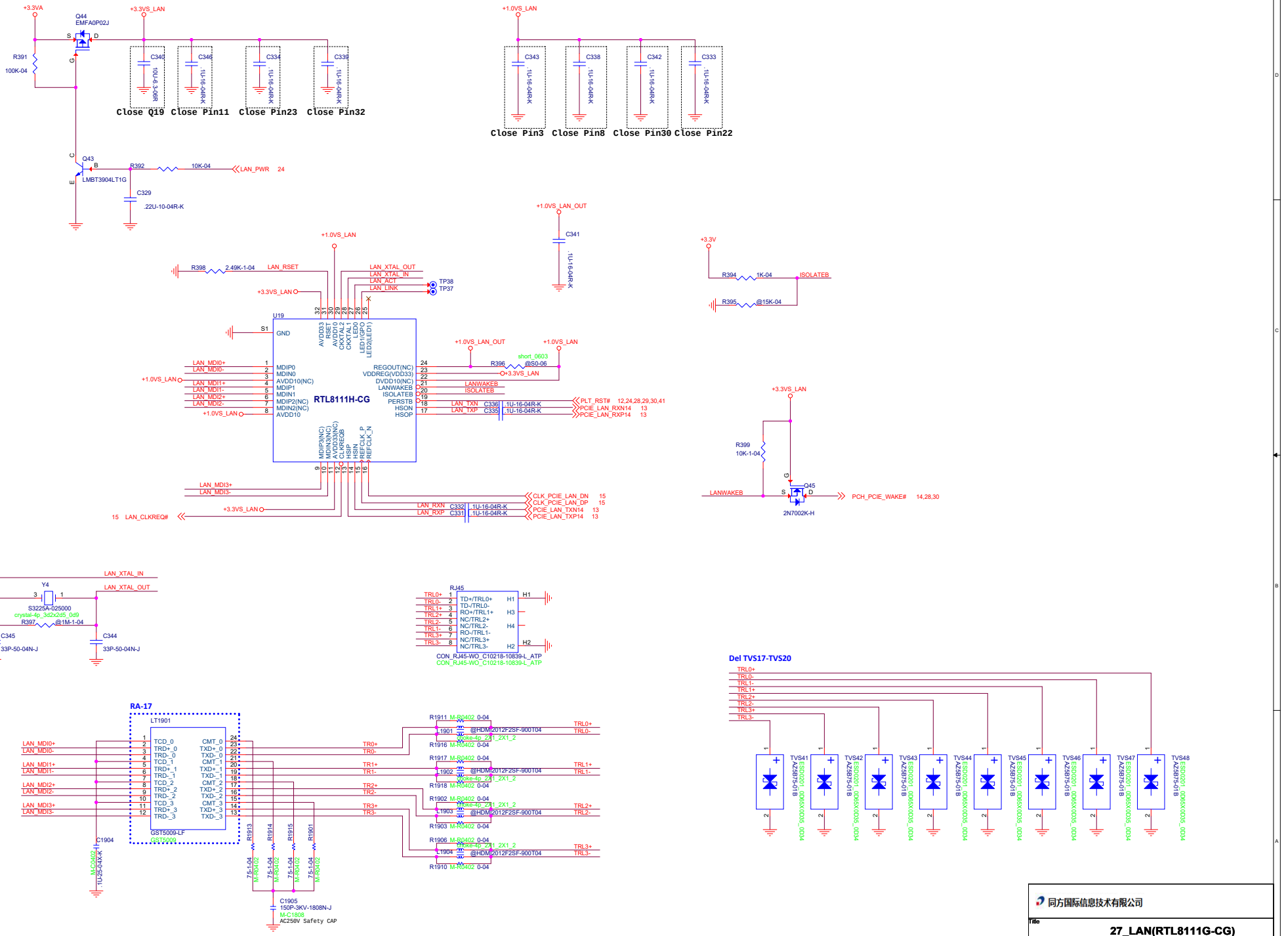
Title	25 ME KB ESD	
Size A	Document Number GK5CXXT	Rev 1.0
Date: Wednesday, May 08, 2019	Sheet 25 of 70	

CODEC ALC269Q





同方国际信息技术有限公司

Title	27_LAN(RTL8111G-CG)	
Size C	Document Number GK5CXXT	Rev 1.0
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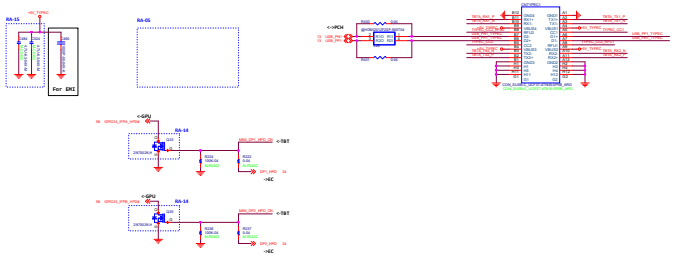
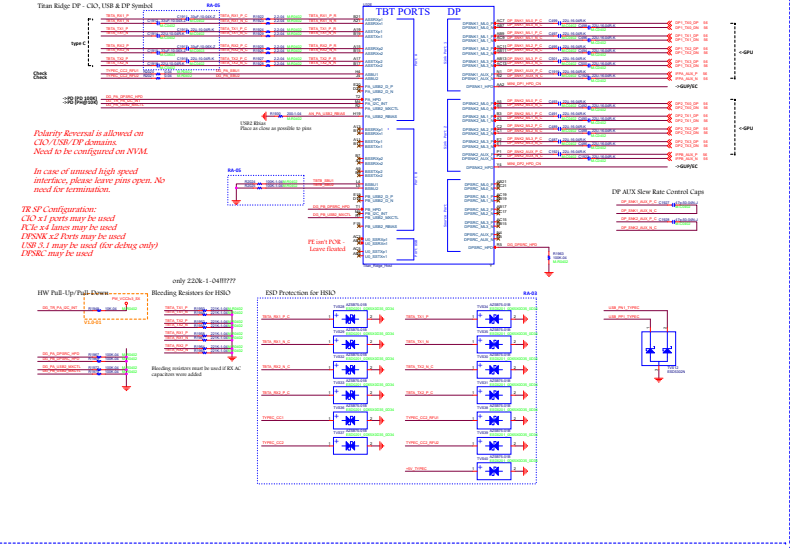
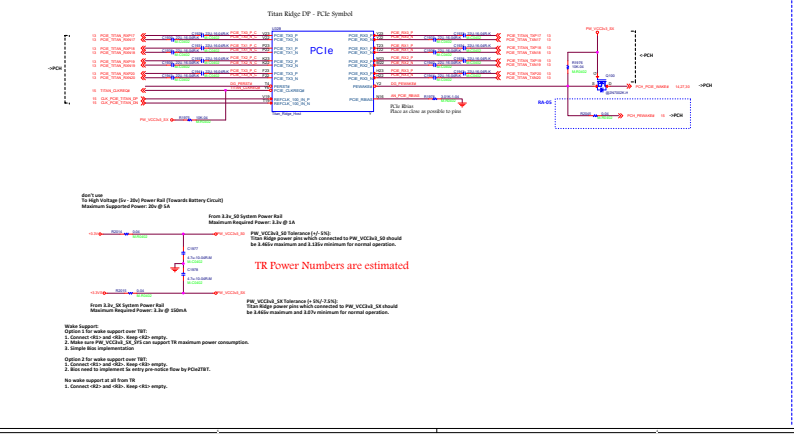
TYPE-C



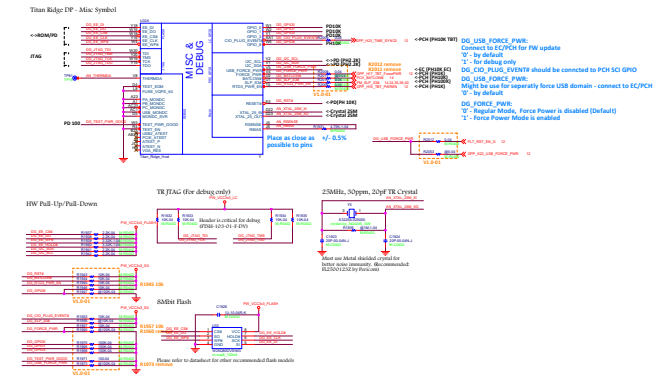
Titan Ridge SP - High Speed (CIO, USB, DP and PCIe) Parts



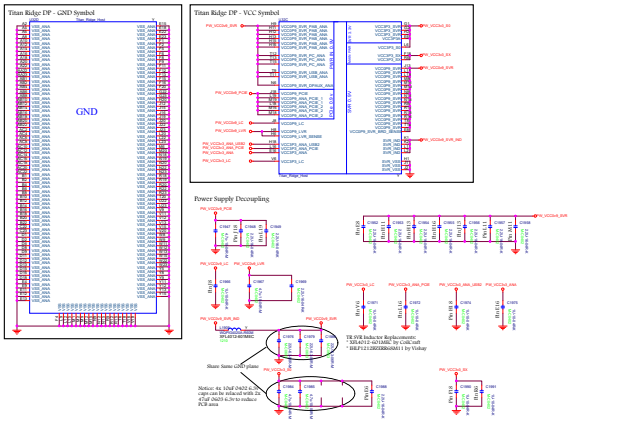
Titan Ridge SP - PCIe



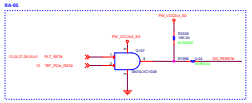
Titan Ridge SP - Misc Part



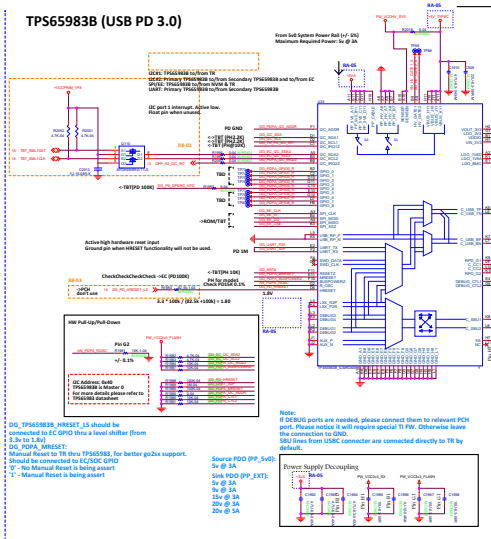
Titan Ridge SP - Power Supply & GND Parts



Titan Ridge SP - RTD3



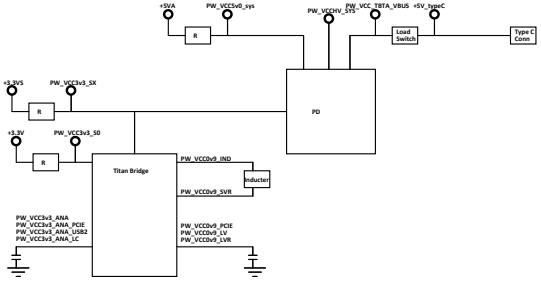
TPS65983B (USB PD 3.0)



Thunderbolt™ High Speed Interface

Interface	Description	Bit Rate
TBT	Thunderbolt™ 20Gbps channel	20.625 Gb/s
USB3.1	USB3.1 10Gbps channel	10 Gb/s
PCIe* Gen3	Used for PCIe root complex connection	8 GT/s
DisplayPort* 1.2a	Used for DP Sink connection	5.4 Gb/s
DisplayPort* 1.4[1]	Used for DP Sink connection	8.1 Gb/s
USB* 2	Used for USB 2.0connection	480 Mb/s

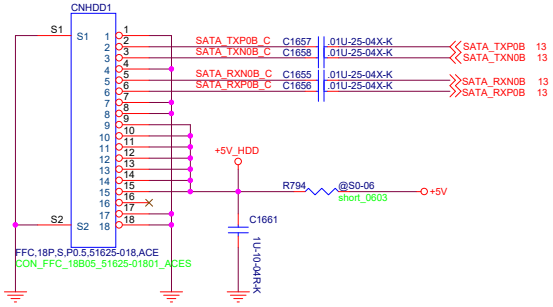
Note: 1. 8.1Gbps is only supported on Titan Ridge



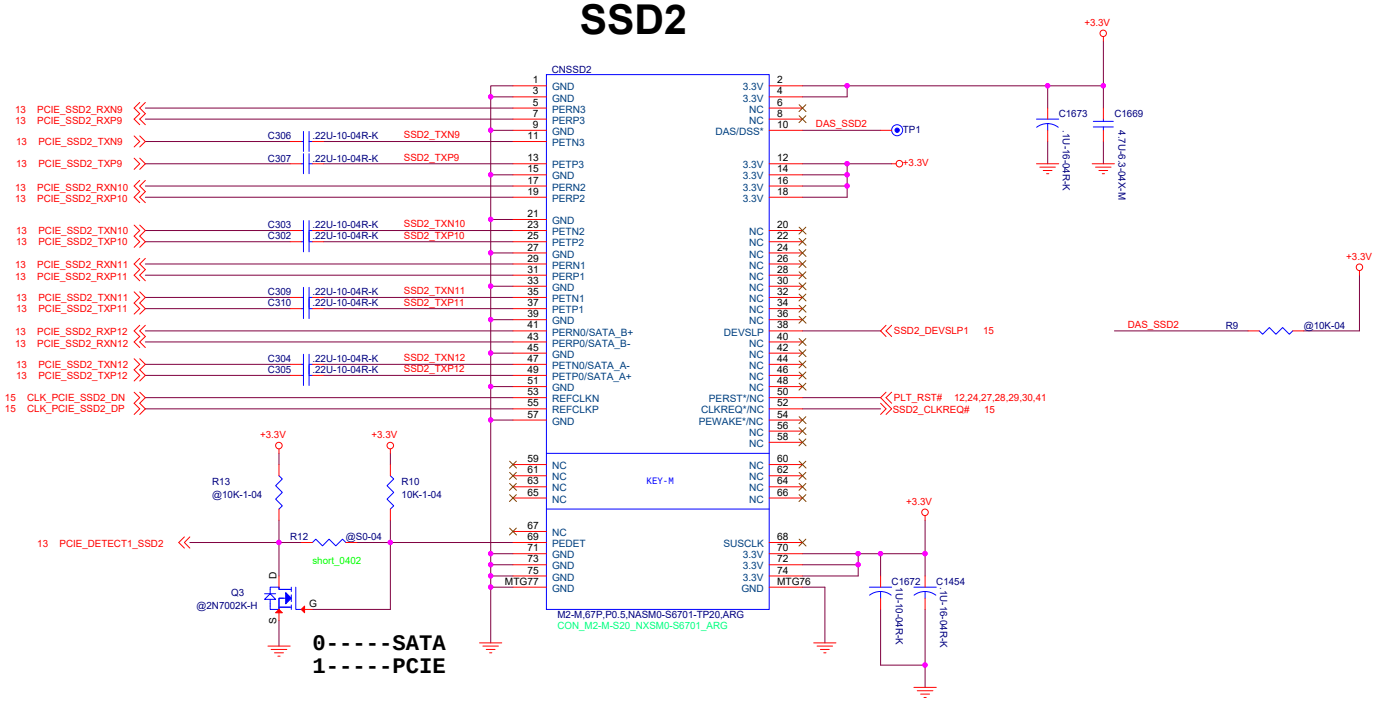
2B_Thunderbolt TYPE-C

GK5CXXT

SATA-HDD

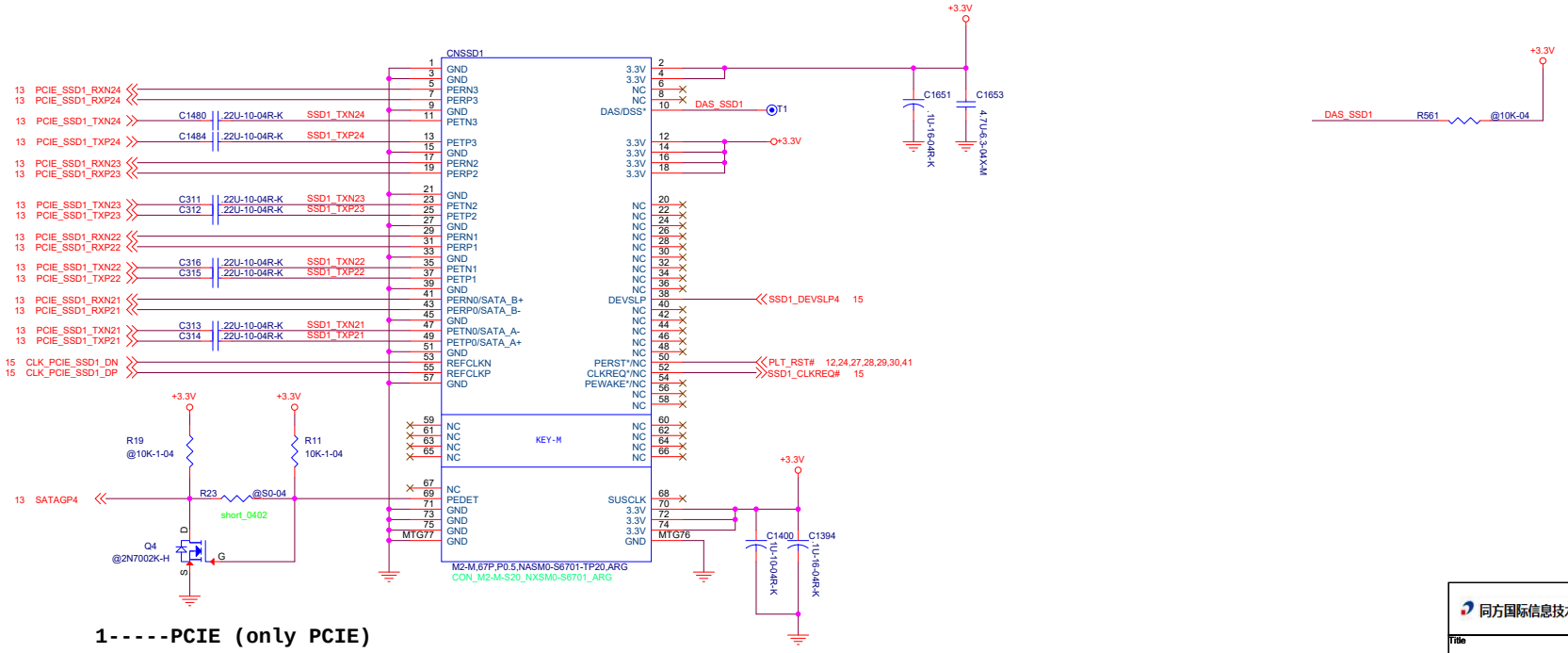


SSD2



0-----SATA
1-----PCIE

SSD1



1-----PCIE (only PCIE)

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Title	29_HDD/SSD	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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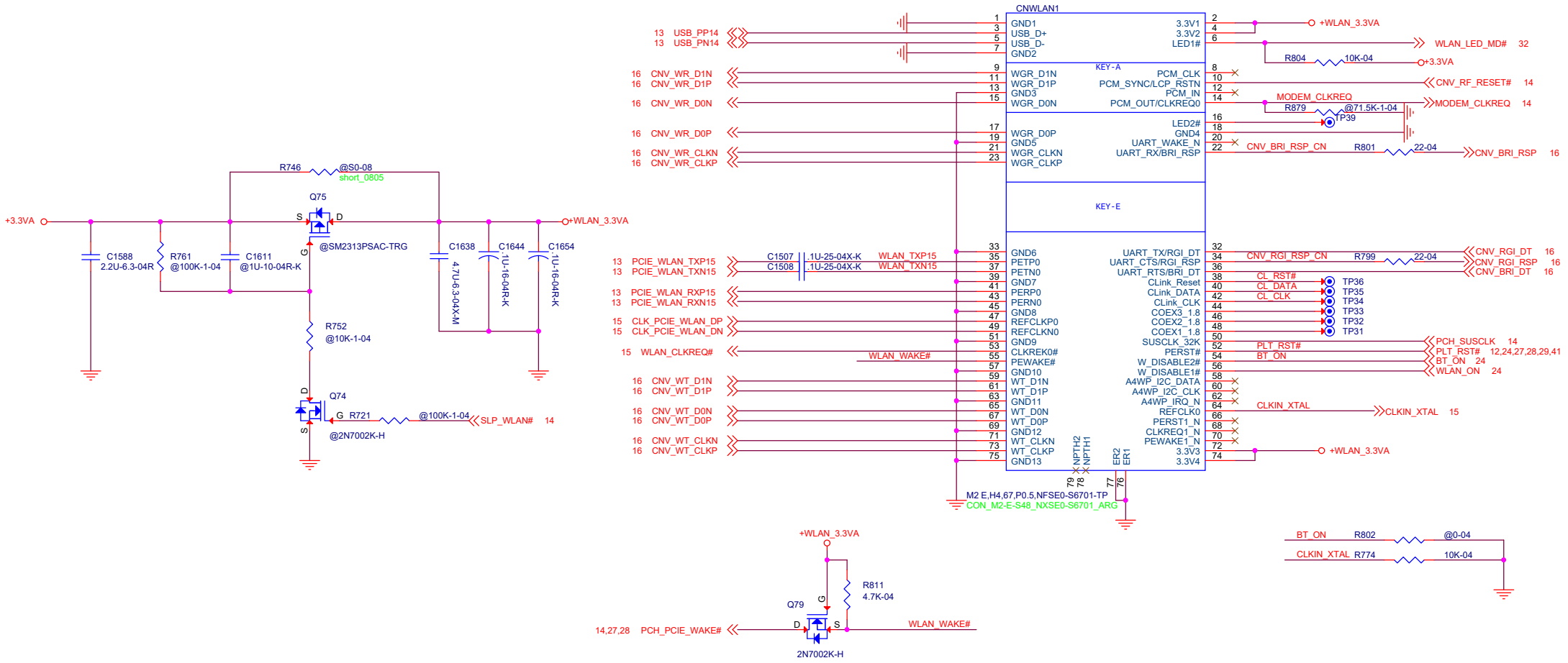
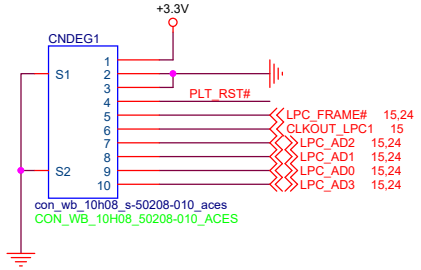
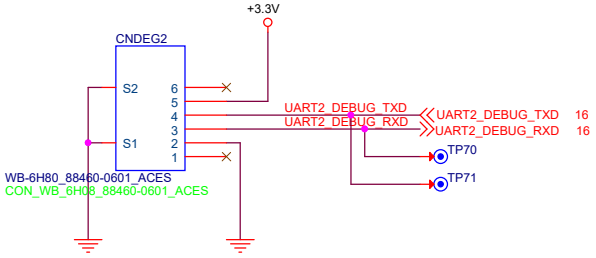
WLAN CONN

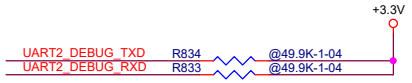


LPC debug port



UART debug port





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Title	30_WLAN/UART DEBUG/LPC DEBUG	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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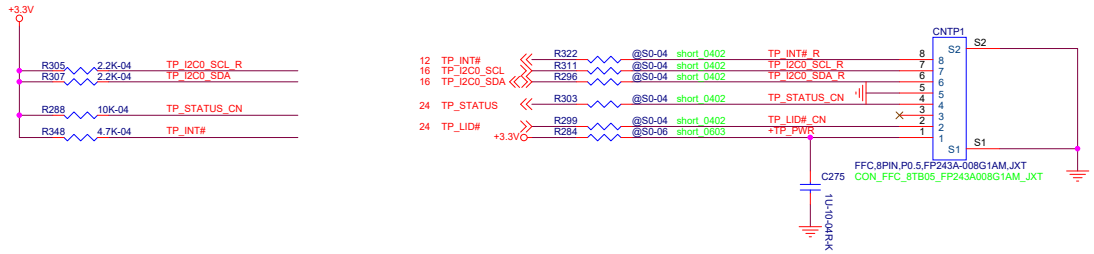
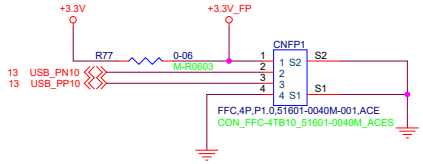
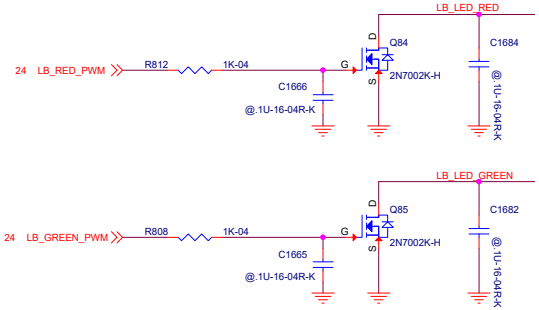
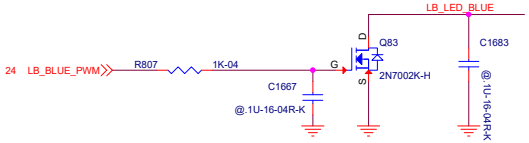
Touch Pad&Finger Print

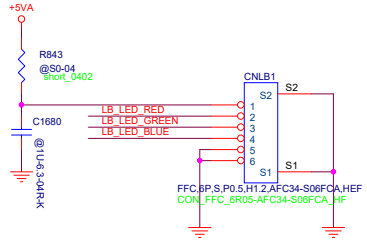




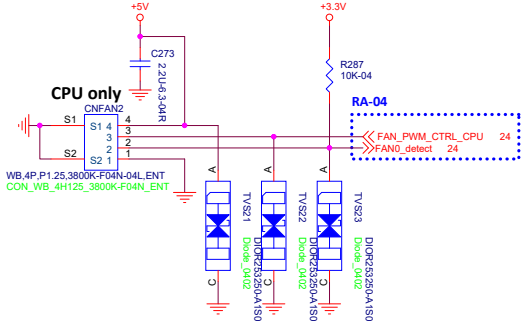
Light bar Control

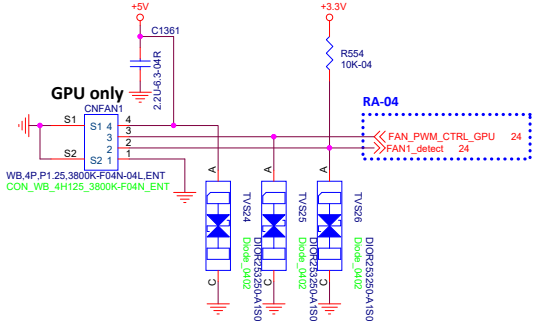






FAN CONTROLLER





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Title	31_TP/CP/FAN/LB/FP	
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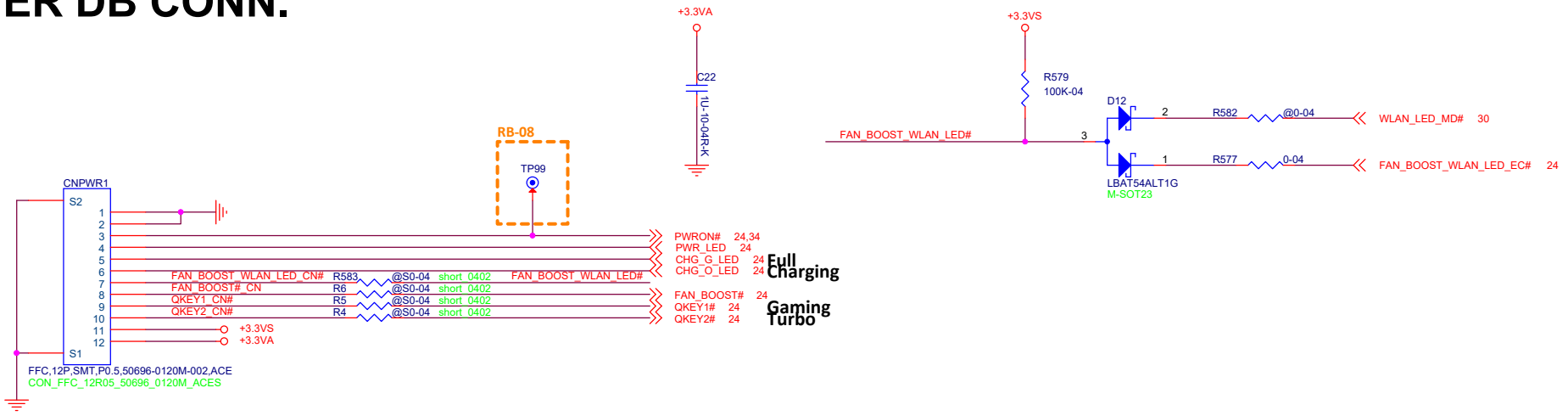
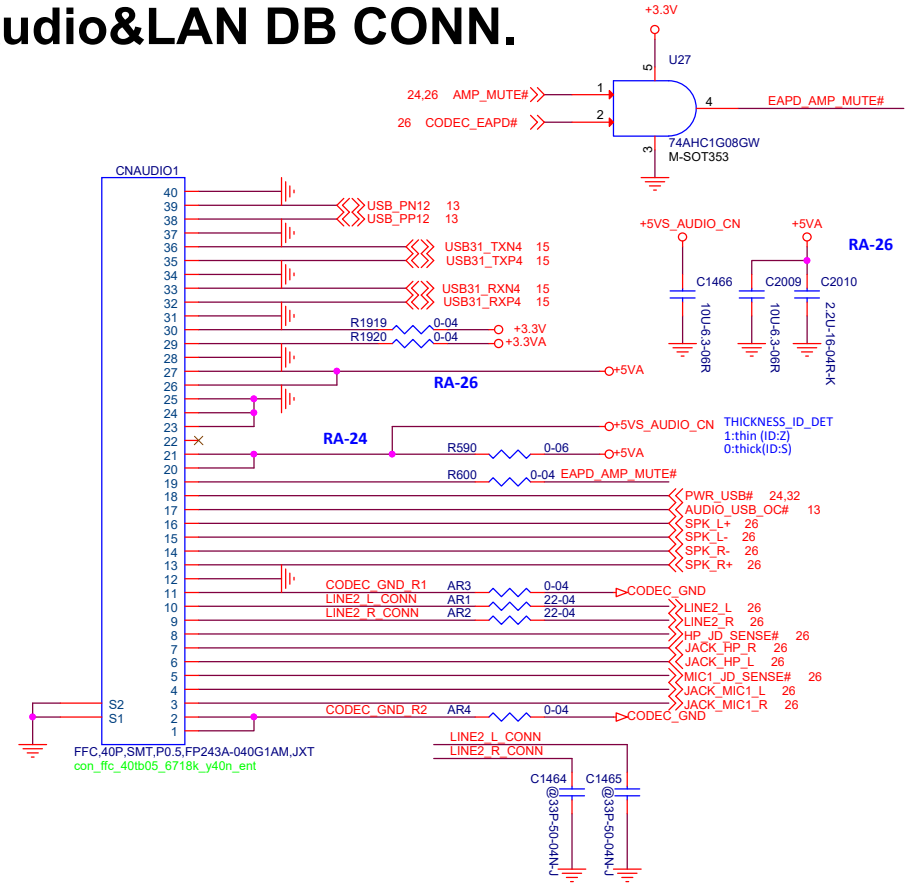
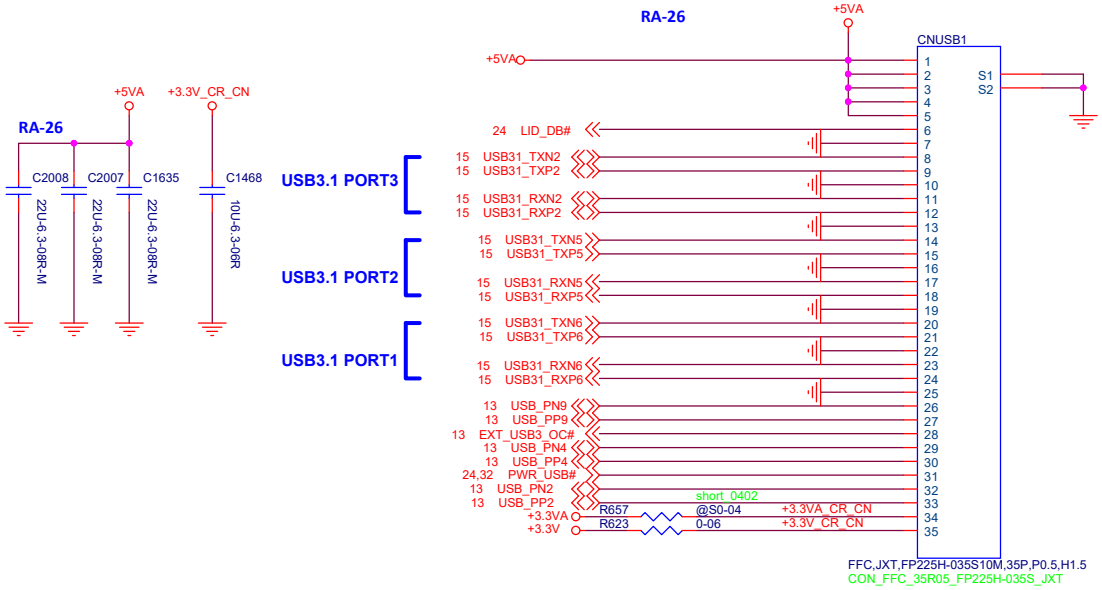
POWER DB CONN.



Audio&LAN DB CONN.



USB3.0 DB CONN.



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Title	32_PWR_DB/USB3.0 DB/Audio DB	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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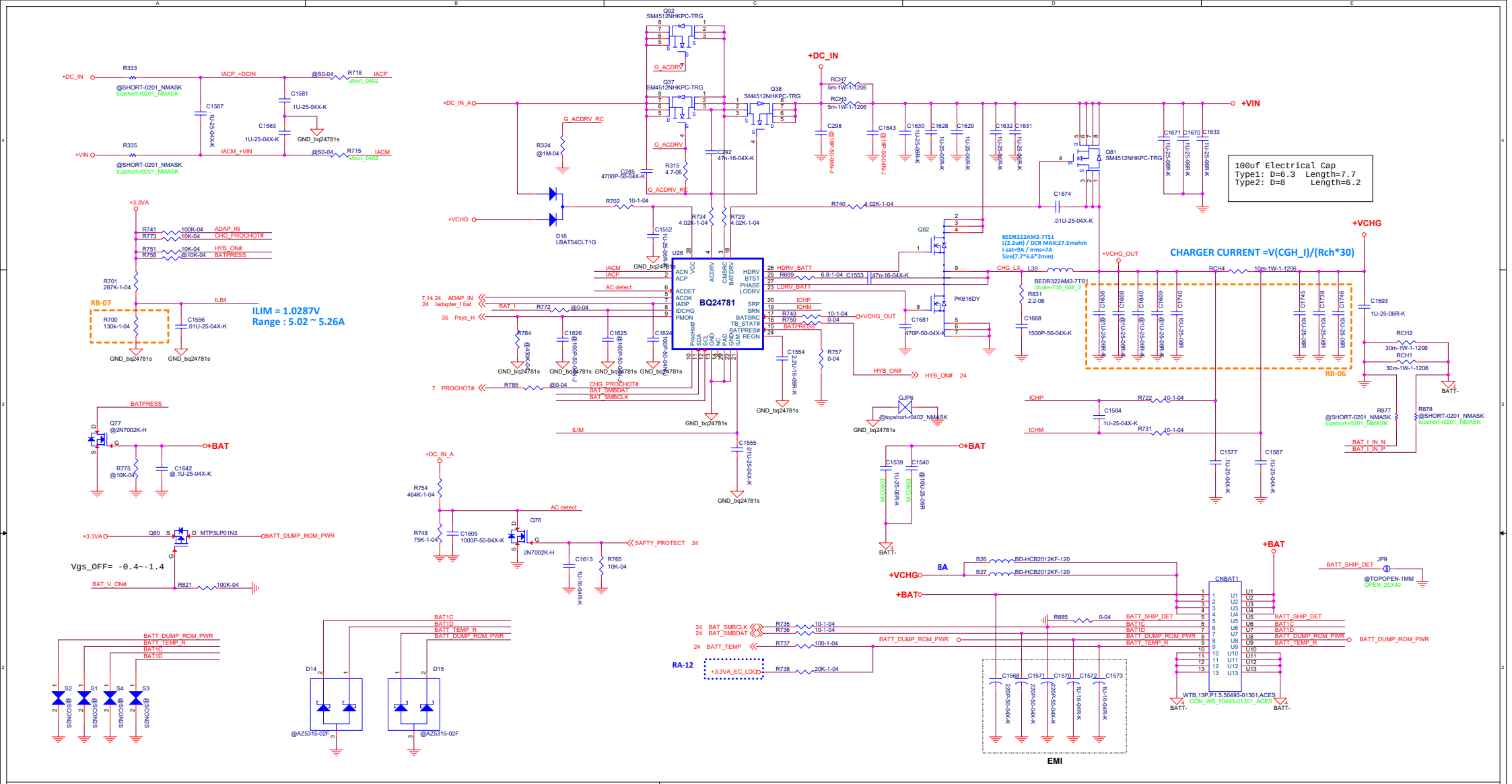
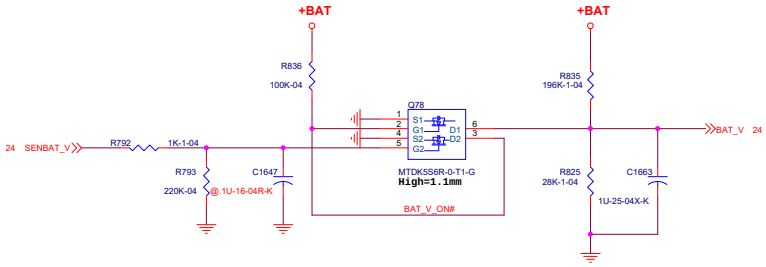
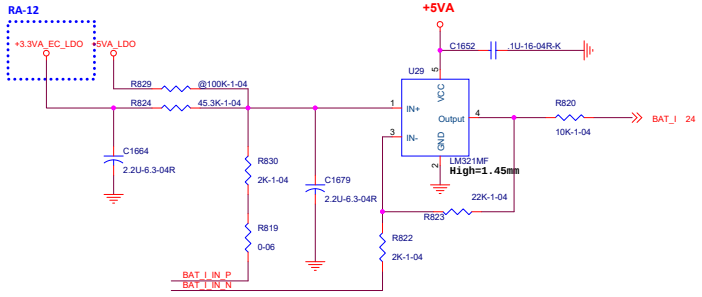


Battery Voltage Detect



Battery Current Detect



RCH1 //RCH2 =15mohm

BAT_I	ICHG (0.1724V/1A)
2.3640V	4A
2.0192V	2A
1.8468V	1A
1.6744V	0A
1.5020V	-1A
1.3296V	-2A
0.9848V	-4A
0.6400V	-6A
0.2952V	-8A
0.1228V	-9A

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Title	33_BATT IN/CHARGER(BQ24781)		
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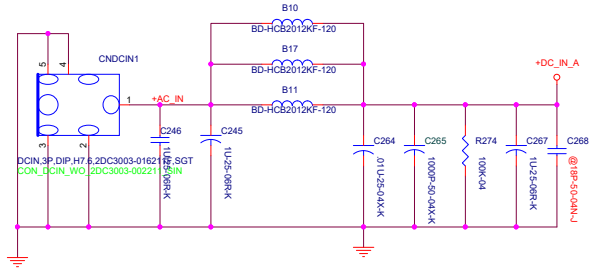
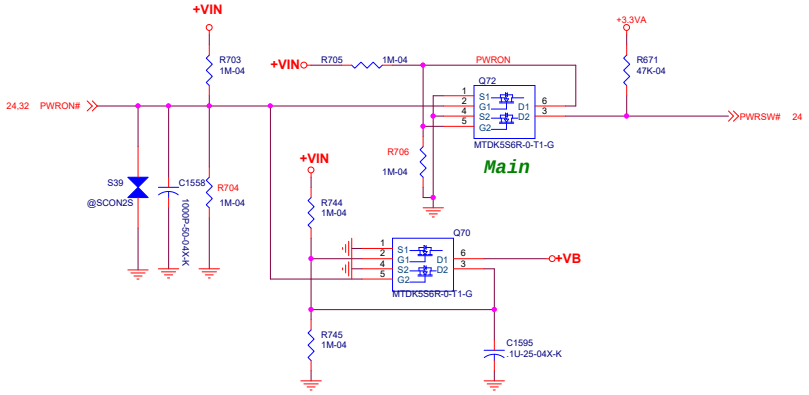
+DC_IN

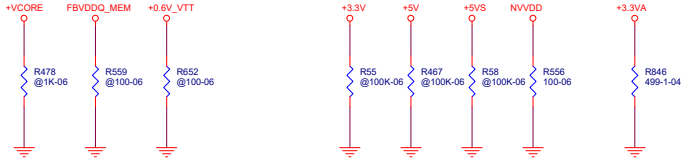



```
EMB20NP3V
ID=-13A  TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt  0.1ms
```

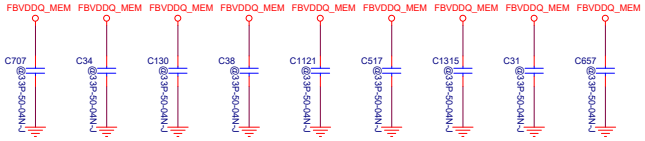
POWER SW



Discharge Resistor

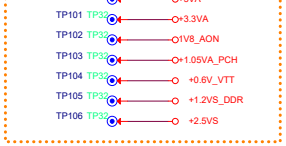


For RF

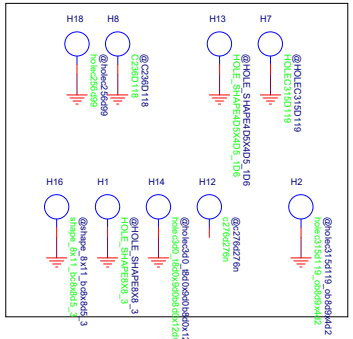


RB-10

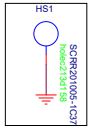
For SMT

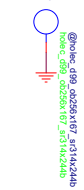


PCB HOLE

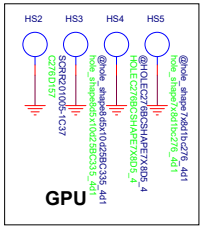


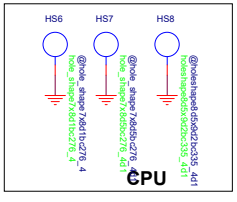
WLAN HOLE

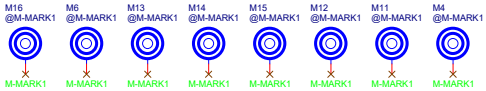




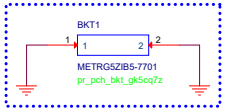
THERMAL HOLE







RA-12



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Title	34_DC IN/PWR_SW/H-S CAP/SCREW		
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Loaline:
VCORE: 1.8m ohm
VCCGT: 2.7m ohm
VCCSA= 10.3m ohm

Rdroop=RLL/(2*Kcs*Kdroop)

Kcs=10uA/A ; Kdroop=0.0625

Address = 20H

Rpsys=0.8/Pin_max * Isys

Psys setting base on charger spec:
1. uA/W information
2. Pmax

Iccmax:	IPL2
VCORE: 140A	VCORE: 86A
VCCGT: 32A	VCCGT: 25A
VCCSA=11.1A	VCCSA=10A

RImon=(32*VImon_max)/(Iccmax*Kcs)

VImon_max =1.1636V ; Kcs =10uA/A

MP2949AGQKT_1040

Title	35_POWER VR CONTROLLER
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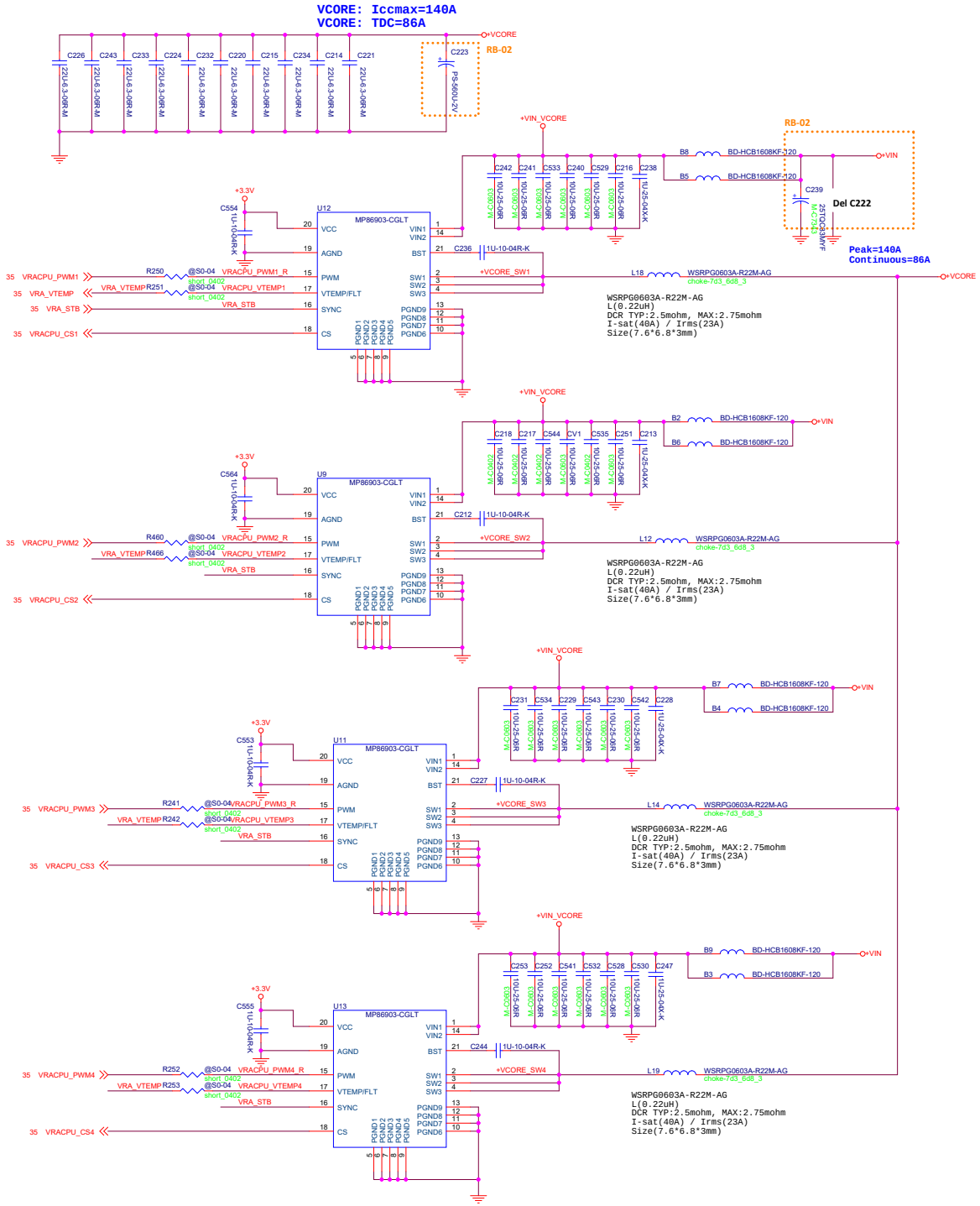
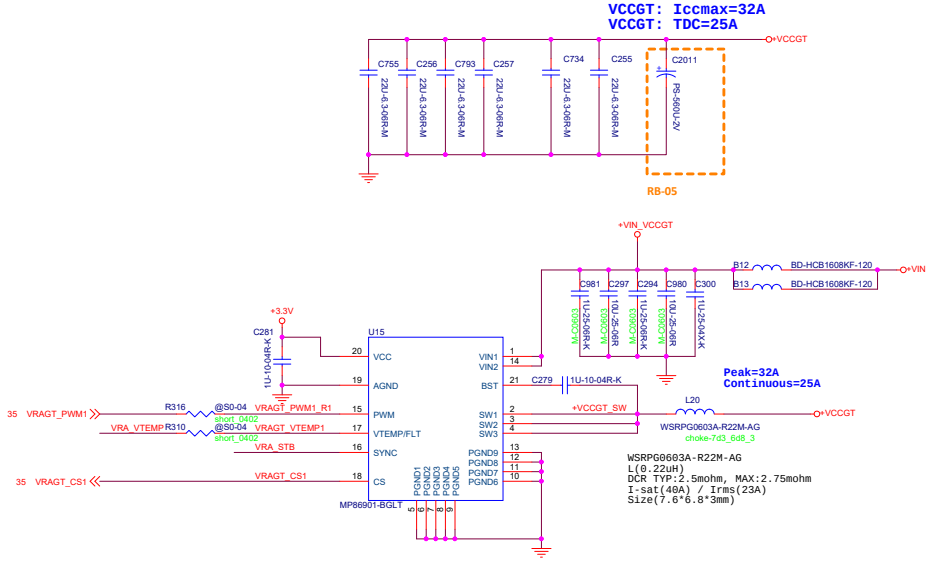
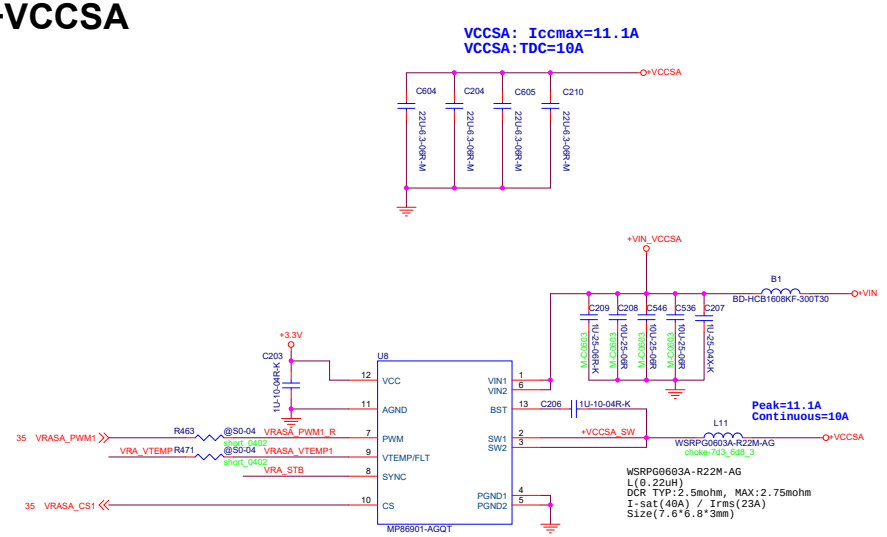
+VCORE



+VCCGT



+VCCSA



同方国际信息技术有限公司

Title	36_POWER VCORE/VCCGT/VCCSA		
Size: Custom	Document Number: GK5CXXT		Rev: 1.0
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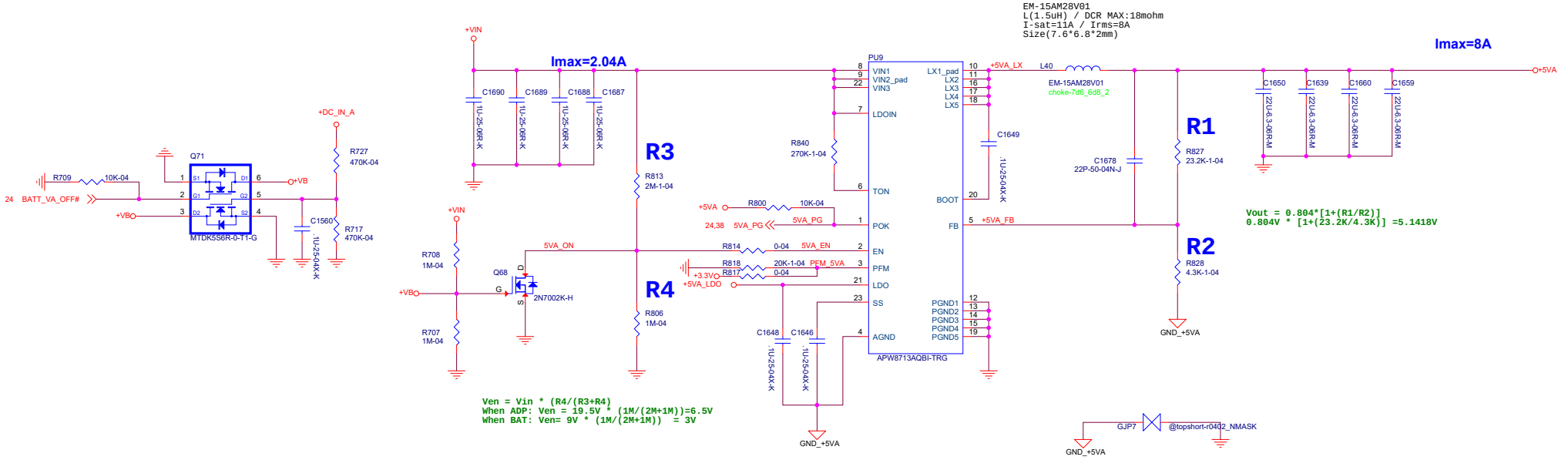
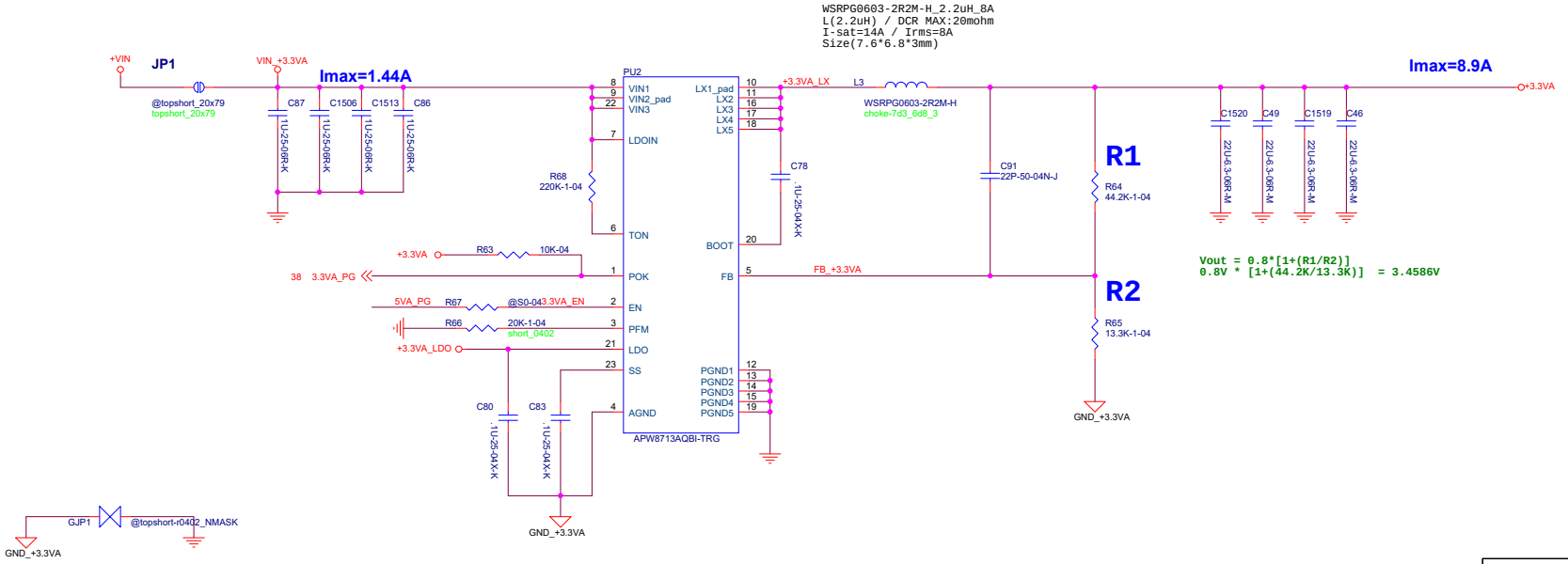
+5VA



+3.3VA



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Title	37_POWER +5VA/+3.3VA	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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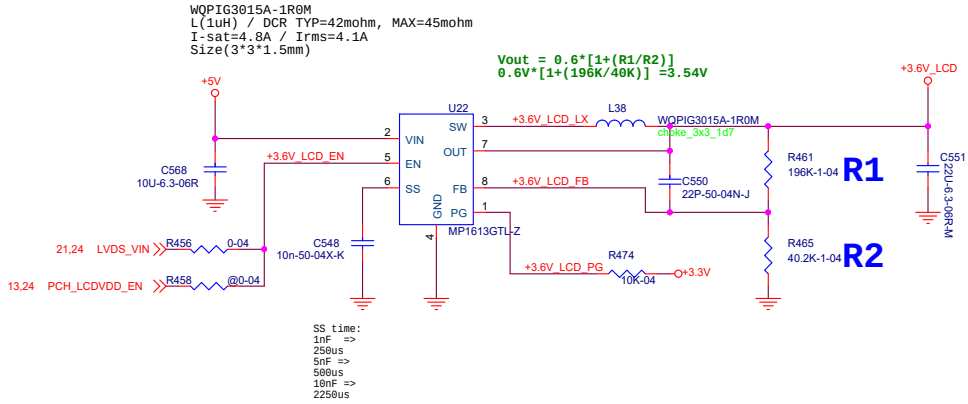
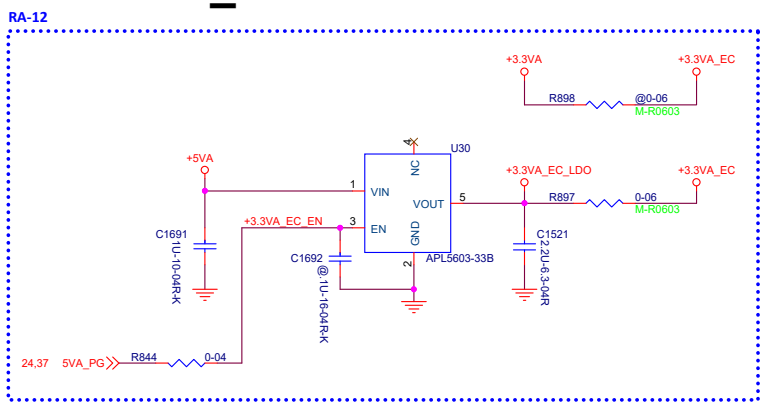
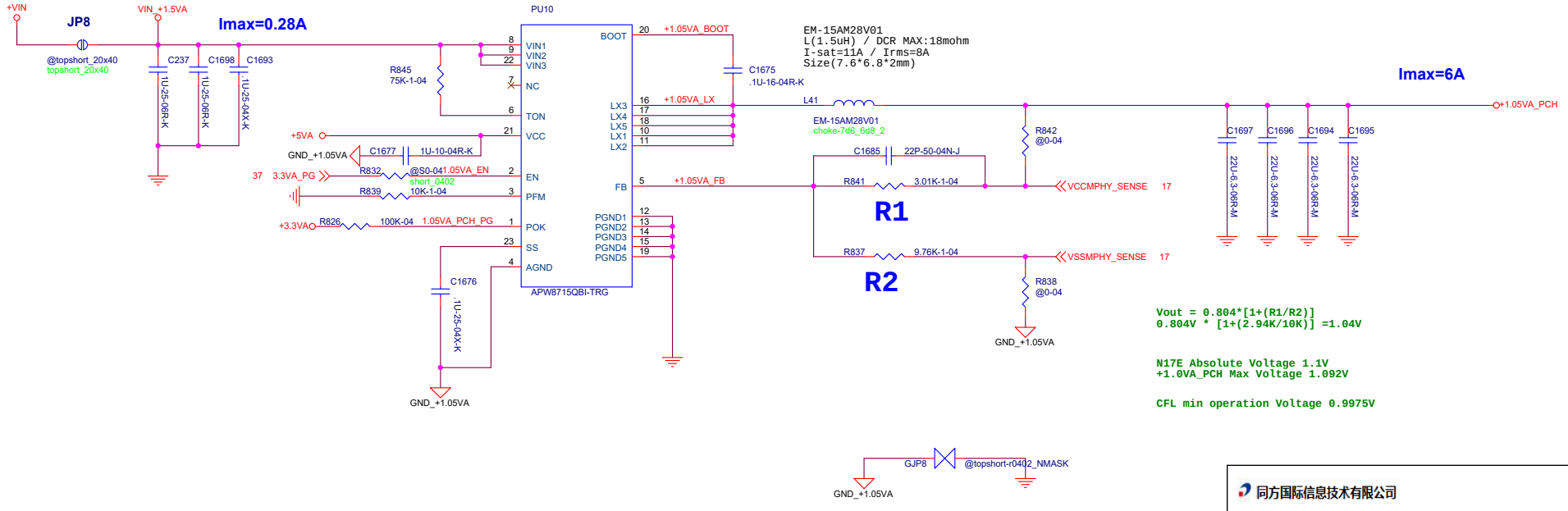
+3.6V_LCD



+3.3VA_EC



+1.05VA_PCH



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Title	38_POWER +1.05VA_PCH/+3.6_LCD	
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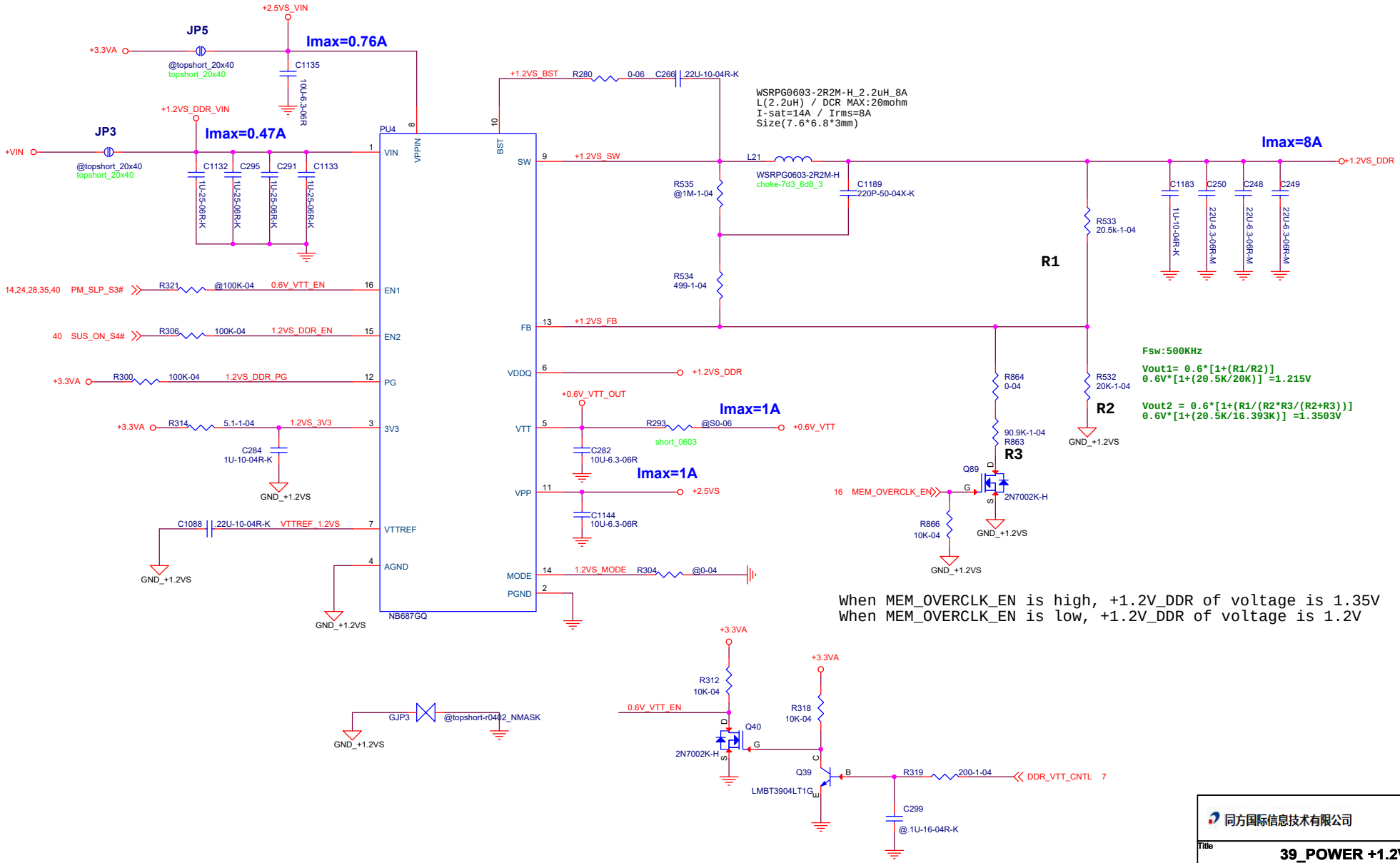
+1.2VS_DDR/+2.5VS/+0.6V_VTT



When MEM_OVERCLK_EN is high, +1.2V_DDR of voltage is 1.35V
When MEM_OVERCLK_EN is low, +1.2V_DDR of voltage is 1.2V

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Title	39_POWER +1.2VS/2.5VS/VTT	
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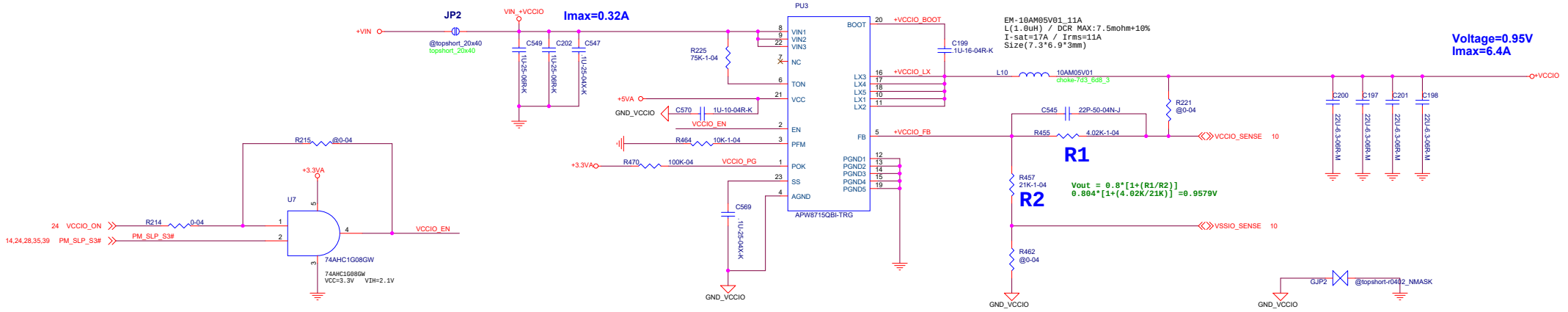
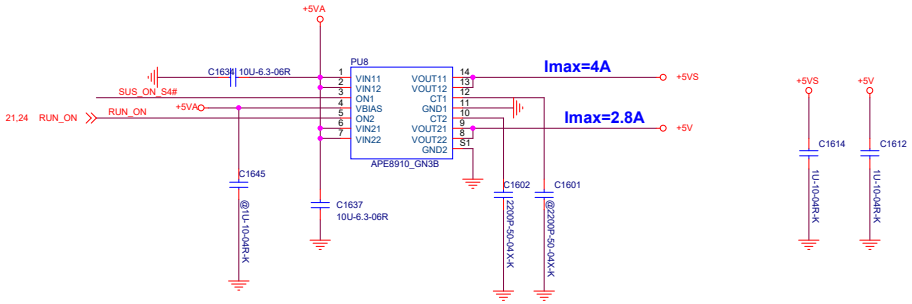
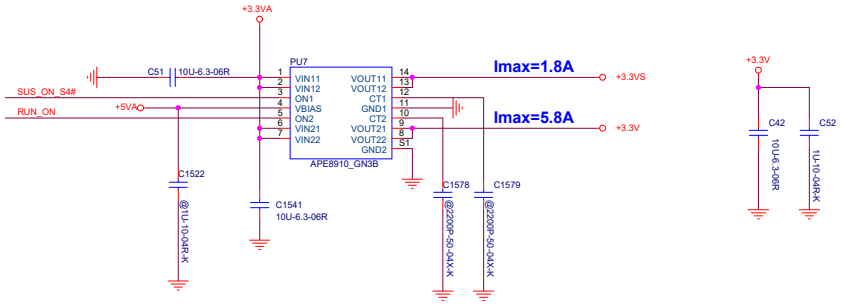
+VCCIO



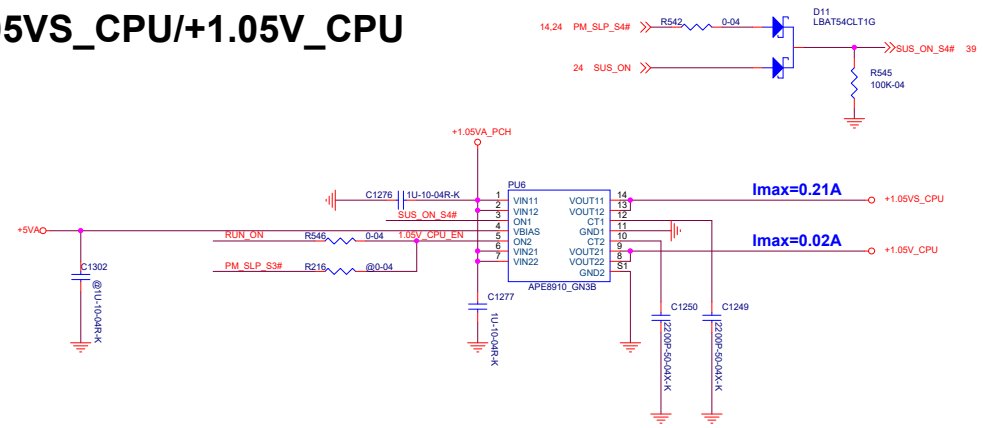
+5VS/+5V

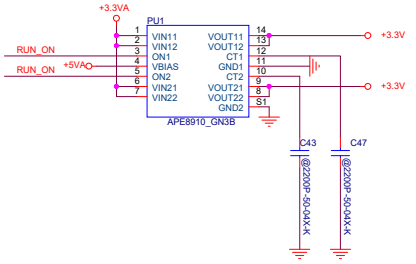


+3.3VS/+3.3V



+1.05VS_CPU/+1.05V_CPU





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Title	40_POWER +VCCIO/+VS PWR/+V PWR		
Size: Custom	Document Number: GK5CXXT		Rev: 1.0
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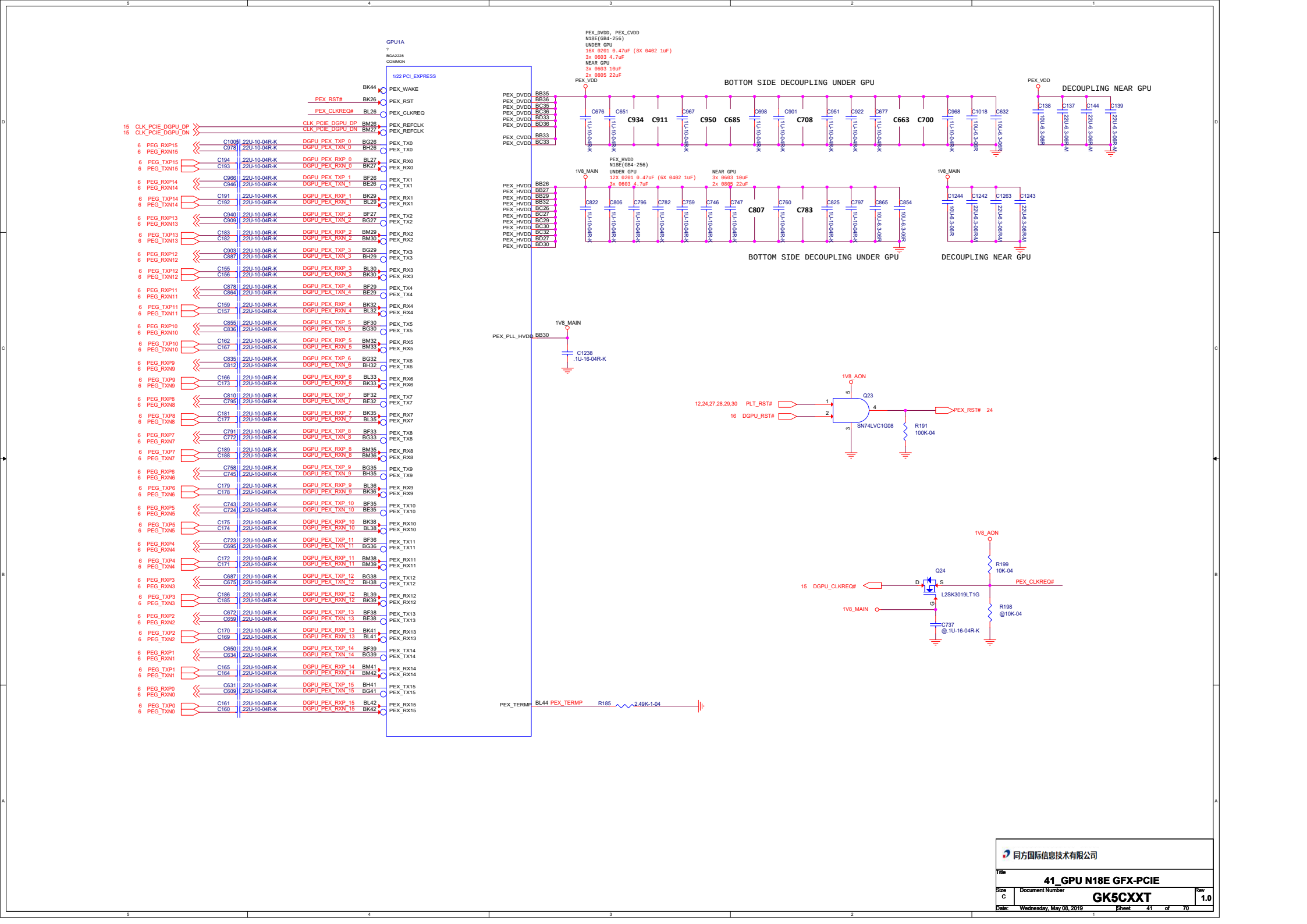
GPU1A
BGA2228
COMMON
1/22 PCI_EXPRESS
PEX_DVDD, PEX_CVDD
N18E(GB4-256)
UNDER GPU
16X 0201 0.47uF (8X 0402 1uF)
3x 0603 4.7uF
NEAR GPU
3x 0603 10uF
2x 0805 22uF
BOTTOM SIDE DECOUPLING UNDER GPU
DECOUPLING NEAR GPU
PEX_HVDD
N18E(GB4-256)
UNDER GPU
12X 0201 0.47uF (6X 0402 1uF)
3x 0603 4.7uF
NEAR GPU
3x 0603 10uF
2x 0805 22uF
BOTTOM SIDE DECOUPLING UNDER GPU
DECOUPLING NEAR GPU
1V8_MAIN
1V8_AON
PEX_VDD
PEX_PLL_HVDD
PEX_TERMP
R185 2.49K-1-04
SN74LVC1G08
L2SK3019LT1G
PLT_RST#
DGPU_RST#
DGPU_CLKREQ#
PEX_RST#
PEX_CLKREQ#
同方国际信息技术有限公司
41_GPU N18E GFX-PCIE
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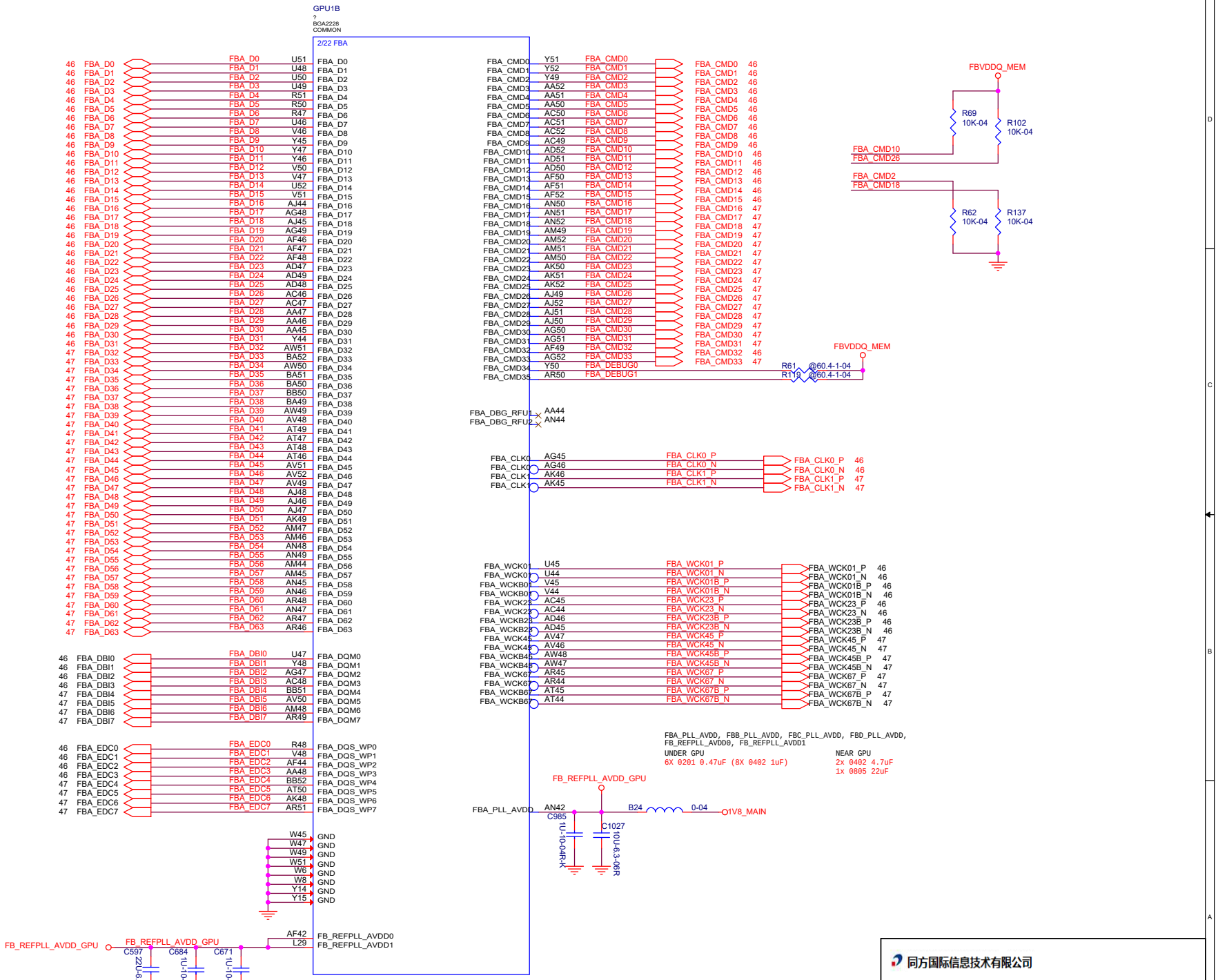

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Title	42_GPU N18E FrameBuffer A	
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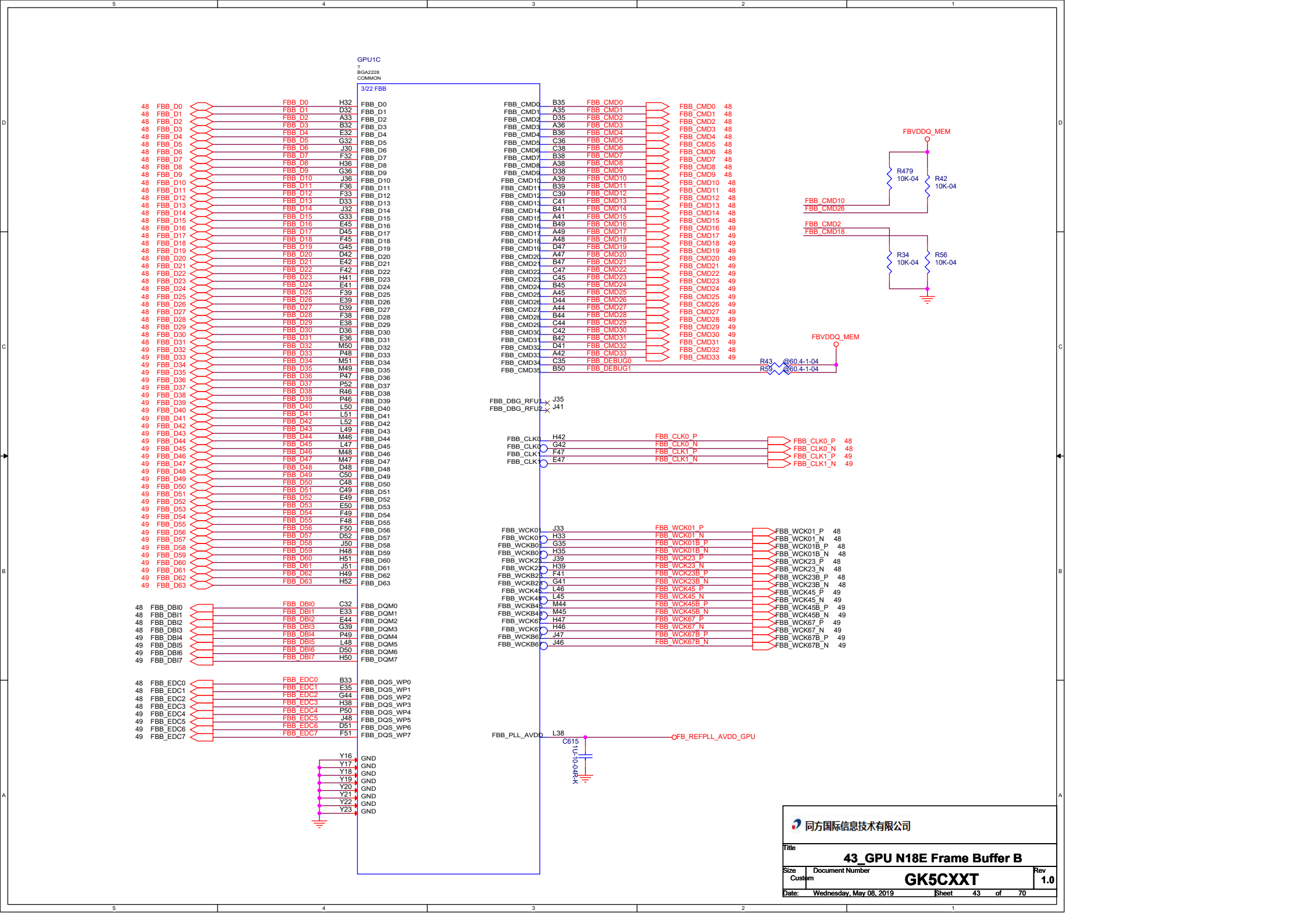
GPU1C
?
BGA2228
COMMON
3/22 FBB
FBB_D0 H32
FBB_D1 D32
FBB_D2 A33
FBB_D3 B32
FBB_D4 E32
FBB_D5 G32
FBB_D6 J30
FBB_D7 F32
FBB_D8 H36
FBB_D9 G36
FBB_D10 J36
FBB_D11 F36
FBB_D12 F33
FBB_D13 D33
FBB_D14 J32
FBB_D15 G33
FBB_D16 E45
FBB_D17 D45
FBB_D18 F45
FBB_D19 G45
FBB_D20 D42
FBB_D21 E42
FBB_D22 F42
FBB_D23 H41
FBB_D24 E41
FBB_D25 F39
FBB_D26 E39
FBB_D27 D39
FBB_D28 F38
FBB_D29 E38
FBB_D30 D36
FBB_D31 E36
FBB_D32 M50
FBB_D33 P48
FBB_D34 M51
FBB_D35 M49
FBB_D36 P47
FBB_D37 P52
FBB_D38 R46
FBB_D39 P46
FBB_D40 L50
FBB_D41 L51
FBB_D42 L52
FBB_D43 L49
FBB_D44 M46
FBB_D45 L47
FBB_D46 M48
FBB_D47 M47
FBB_D48 D48
FBB_D49 C50
FBB_D50 C48
FBB_D51 C49
FBB_D52 E49
FBB_D53 E50
FBB_D54 F49
FBB_D55 F48
FBB_D56 F50
FBB_D57 D52
FBB_D58 J50
FBB_D59 H48
FBB_D60 H51
FBB_D61 J51
FBB_D62 H49
FBB_D63 H52
FBB_DBI0 C32
FBB_DBI1 E33
FBB_DBI2 E44
FBB_DBI3 G39
FBB_DBI4 P49
FBB_DBI5 L48
FBB_DBI6 D50
FBB_DBI7 H50
FBB_EDC0 B33
FBB_EDC1 E35
FBB_EDC2 G44
FBB_EDC3 H38
FBB_EDC4 P50
FBB_EDC5 J48
FBB_EDC6 D51
FBB_EDC7 F51
Y16 GND
Y17 GND
Y18 GND
Y19 GND
Y20 GND
Y21 GND
Y22 GND
Y23 GND
FBB_CMD0 B35
FBB_CMD1 A35
FBB_CMD2 D35
FBB_CMD3 A36
FBB_CMD4 B36
FBB_CMD5 C36
FBB_CMD6 C38
FBB_CMD7 B38
FBB_CMD8 A38
FBB_CMD9 D38
FBB_CMD10 A39
FBB_CMD11 B39
FBB_CMD12 C39
FBB_CMD13 C41
FBB_CMD14 B41
FBB_CMD15 A41
FBB_CMD16 B49
FBB_CMD17 A49
FBB_CMD18 A48
FBB_CMD19 D47
FBB_CMD20 A47
FBB_CMD21 B47
FBB_CMD22 C47
FBB_CMD23 C45
FBB_CMD24 B45
FBB_CMD25 A45
FBB_CMD26 D44
FBB_CMD27 A44
FBB_CMD28 B44
FBB_CMD29 C44
FBB_CMD30 C42
FBB_CMD31 B42
FBB_CMD32 D41
FBB_CMD33 A42
FBB_DEBUG0 C35
FBB_DEBUG1 B50
FBVDDQ_MEM
R479 10K-04
R42 10K-04
R34 10K-04
R56 10K-04
R43 @60.4-1-04
R59 @60.4-1-04
FBB_DBG_RFU1 J35
FBB_DBG_RFU2 J41
FBB_CLK0 H42
FBB_CLK0 G42
FBB_CLK1 F47
FBB_CLK1 E47
FBB_WCK01 J33
FBB_WCK01 H33
FBB_WCK01B G35
FBB_WCK01B H35
FBB_WCK23 J39
FBB_WCK23 H39
FBB_WCK23B F41
FBB_WCK23B G41
FBB_WCK45 L46
FBB_WCK45 L45
FBB_WCK45B M44
FBB_WCK45B M45
FBB_WCK67 H47
FBB_WCK67 H46
FBB_WCK67B J47
FBB_WCK67B J46
FBB_PLL_AVDD L38
FB_REFPLL_AVDD_GPU
C615 1-U-10-04R-K
同方国际信息技术有限公司
Title
43_GPU N18E Frame Buffer B
Size Custom
Document Number GK5CXXT
Rev 1.0
Date: Wednesday, May 08, 2019
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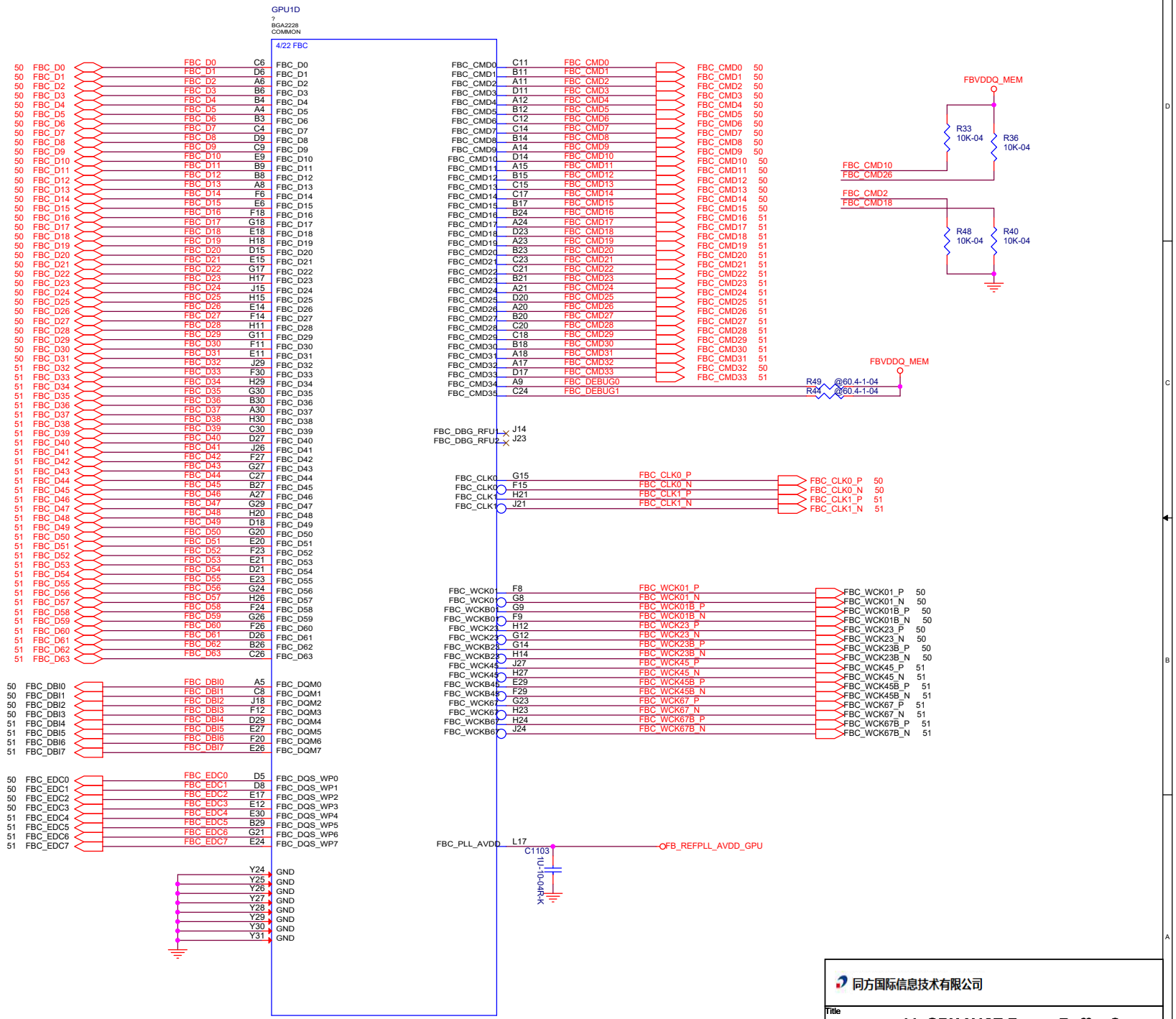
GPU1D
?
BGA2228
COMMON
4/22 FBC
FBC_D0 C6 FBC_D0
FBC_D1 D6 FBC_D1
FBC_D2 A6 FBC_D2
FBC_D3 B6 FBC_D3
FBC_D4 B4 FBC_D4
FBC_D5 A4 FBC_D5
FBC_D6 B3 FBC_D6
FBC_D7 C4 FBC_D7
FBC_D8 D9 FBC_D8
FBC_D9 C9 FBC_D9
FBC_D10 E9 FBC_D10
FBC_D11 B9 FBC_D11
FBC_D12 B8 FBC_D12
FBC_D13 A8 FBC_D13
FBC_D14 F6 FBC_D14
FBC_D15 E6 FBC_D15
FBC_D16 F18 FBC_D16
FBC_D17 G18 FBC_D17
FBC_D18 E18 FBC_D18
FBC_D19 H18 FBC_D19
FBC_D20 D15 FBC_D20
FBC_D21 E15 FBC_D21
FBC_D22 G17 FBC_D22
FBC_D23 H17 FBC_D23
FBC_D24 J15 FBC_D24
FBC_D25 H15 FBC_D25
FBC_D26 E14 FBC_D26
FBC_D27 F14 FBC_D27
FBC_D28 H11 FBC_D28
FBC_D29 G11 FBC_D29
FBC_D30 F11 FBC_D30
FBC_D31 E11 FBC_D31
FBC_D32 J29 FBC_D32
FBC_D33 F30 FBC_D33
FBC_D34 H29 FBC_D34
FBC_D35 G30 FBC_D35
FBC_D36 B30 FBC_D36
FBC_D37 A30 FBC_D37
FBC_D38 H30 FBC_D38
FBC_D39 C30 FBC_D39
FBC_D40 D27 FBC_D40
FBC_D41 J26 FBC_D41
FBC_D42 F27 FBC_D42
FBC_D43 G27 FBC_D43
FBC_D44 C27 FBC_D44
FBC_D45 B27 FBC_D45
FBC_D46 A27 FBC_D46
FBC_D47 G29 FBC_D47
FBC_D48 H20 FBC_D48
FBC_D49 D18 FBC_D49
FBC_D50 G20 FBC_D50
FBC_D51 E20 FBC_D51
FBC_D52 F23 FBC_D52
FBC_D53 E21 FBC_D53
FBC_D54 D21 FBC_D54
FBC_D55 E23 FBC_D55
FBC_D56 G24 FBC_D56
FBC_D57 H26 FBC_D57
FBC_D58 F24 FBC_D58
FBC_D59 G26 FBC_D59
FBC_D60 F26 FBC_D60
FBC_D61 D26 FBC_D61
FBC_D62 B26 FBC_D62
FBC_D63 C26 FBC_D63
FBC_DBI0 A5 FBC_DQM0
FBC_DBI1 C8 FBC_DQM1
FBC_DBI2 J18 FBC_DQM2
FBC_DBI3 F12 FBC_DQM3
FBC_DBI4 D29 FBC_DQM4
FBC_DBI5 E27 FBC_DQM5
FBC_DBI6 F20 FBC_DQM6
FBC_DBI7 E26 FBC_DQM7
FBC_EDC0 D5 FBC_DQS_WP0
FBC_EDC1 D8 FBC_DQS_WP1
FBC_EDC2 E17 FBC_DQS_WP2
FBC_EDC3 E12 FBC_DQS_WP3
FBC_EDC4 E30 FBC_DQS_WP4
FBC_EDC5 B29 FBC_DQS_WP5
FBC_EDC6 G21 FBC_DQS_WP6
FBC_EDC7 E24 FBC_DQS_WP7
Y24 GND
Y25 GND
Y26 GND
Y27 GND
Y28 GND
Y29 GND
Y30 GND
Y31 GND
FBC_CMD0 C11 FBC_CMD0
FBC_CMD1 B11 FBC_CMD1
FBC_CMD2 A11 FBC_CMD2
FBC_CMD3 D11 FBC_CMD3
FBC_CMD4 A12 FBC_CMD4
FBC_CMD5 B12 FBC_CMD5
FBC_CMD6 C12 FBC_CMD6
FBC_CMD7 C14 FBC_CMD7
FBC_CMD8 B14 FBC_CMD8
FBC_CMD9 A14 FBC_CMD9
FBC_CMD10 D14 FBC_CMD10
FBC_CMD11 A15 FBC_CMD11
FBC_CMD12 B15 FBC_CMD12
FBC_CMD13 C15 FBC_CMD13
FBC_CMD14 C17 FBC_CMD14
FBC_CMD15 B17 FBC_CMD15
FBC_CMD16 B24 FBC_CMD16
FBC_CMD17 A24 FBC_CMD17
FBC_CMD18 D23 FBC_CMD18
FBC_CMD19 A23 FBC_CMD19
FBC_CMD20 B23 FBC_CMD20
FBC_CMD21 C23 FBC_CMD21
FBC_CMD22 C21 FBC_CMD22
FBC_CMD23 B21 FBC_CMD23
FBC_CMD24 A21 FBC_CMD24
FBC_CMD25 D20 FBC_CMD25
FBC_CMD26 A20 FBC_CMD26
FBC_CMD27 B20 FBC_CMD27
FBC_CMD28 C20 FBC_CMD28
FBC_CMD29 C18 FBC_CMD29
FBC_CMD30 B18 FBC_CMD30
FBC_CMD31 A18 FBC_CMD31
FBC_CMD32 A17 FBC_CMD32
FBC_CMD33 D17 FBC_CMD33
FBC_DEBUG0 A9
FBC_DEBUG1 C24
FBC_CMD0 50
FBC_CMD1 50
FBC_CMD2 50
FBC_CMD3 50
FBC_CMD4 50
FBC_CMD5 50
FBC_CMD6 50
FBC_CMD7 50
FBC_CMD8 50
FBC_CMD9 50
FBC_CMD10 50
FBC_CMD11 50
FBC_CMD12 50
FBC_CMD13 50
FBC_CMD14 50
FBC_CMD15 50
FBC_CMD16 51
FBC_CMD17 51
FBC_CMD18 51
FBC_CMD19 51
FBC_CMD20 51
FBC_CMD21 51
FBC_CMD22 51
FBC_CMD23 51
FBC_CMD24 51
FBC_CMD25 51
FBC_CMD26 51
FBC_CMD27 51
FBC_CMD28 51
FBC_CMD29 51
FBC_CMD30 51
FBC_CMD31 51
FBC_CMD32 50
FBC_CMD33 51
FBVDDQ_MEM
R33 10K-04
R36 10K-04
FBC_CMD10
FBC_CMD26
FBC_CMD2
FBC_CMD18
R48 10K-04
R40 10K-04
FBVDDQ_MEM
R49 @60.4-1-04
R47 @60.4-1-04
FBC_DBG_RFU1 J14
FBC_DBG_RFU2 J23
FBC_CLK0 G15
FBC_CLK0 F15
FBC_CLK1 H21
FBC_CLK1 J21
FBC_CLK0_P
FBC_CLK0_N
FBC_CLK1_P
FBC_CLK1_N
FBC_CLK0_P 50
FBC_CLK0_N 50
FBC_CLK1_P 51
FBC_CLK1_N 51
FBC_WCK01 F8
FBC_WCK01 G8
FBC_WCKB01 G9
FBC_WCKB01 F9
FBC_WCK23 H12
FBC_WCK23 G12
FBC_WCKB23 G14
FBC_WCKB23 H14
FBC_WCK45 J27
FBC_WCK45 H27
FBC_WCKB45 E29
FBC_WCKB45 F29
FBC_WCK67 G23
FBC_WCK67 H23
FBC_WCKB67 H24
FBC_WCKB67 J24
FBC_WCK01_P
FBC_WCK01_N
FBC_WCK01B_P
FBC_WCK01B_N
FBC_WCK23_P
FBC_WCK23_N
FBC_WCK23B_P
FBC_WCK23B_N
FBC_WCK45_P
FBC_WCK45_N
FBC_WCK45B_P
FBC_WCK45B_N
FBC_WCK67_P
FBC_WCK67_N
FBC_WCK67B_P
FBC_WCK67B_N
FBC_WCK01_P 50
FBC_WCK01_N 50
FBC_WCK01B_P 50
FBC_WCK01B_N 50
FBC_WCK23_P 50
FBC_WCK23_N 50
FBC_WCK23B_P 50
FBC_WCK23B_N 50
FBC_WCK45_P 51
FBC_WCK45_N 51
FBC_WCK45B_P 51
FBC_WCK45B_N 51
FBC_WCK67_P 51
FBC_WCK67_N 51
FBC_WCK67B_P 51
FBC_WCK67B_N 51
FBC_PLL_AVDD L17
FB_REFPLL_AVDD_GPU
C1103
1U-10-04R-K
同方国际信息技术有限公司
Title
44_GPU N18E Frame Buffer C
Size Custom
Document Number
GK5CXXT
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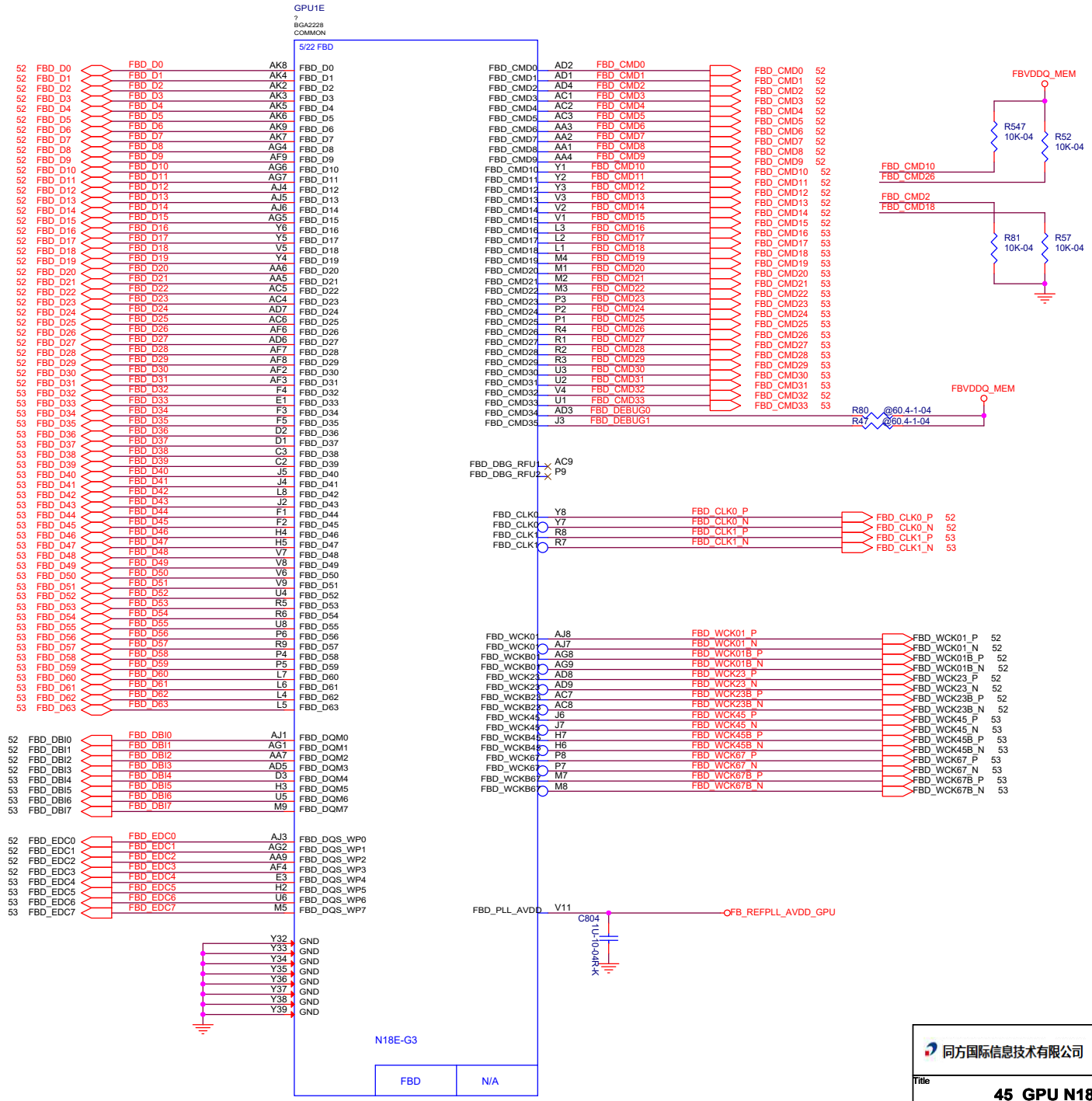

同方国际信息技术有限公司

Title	45_GPU N18E Frame Buffer D	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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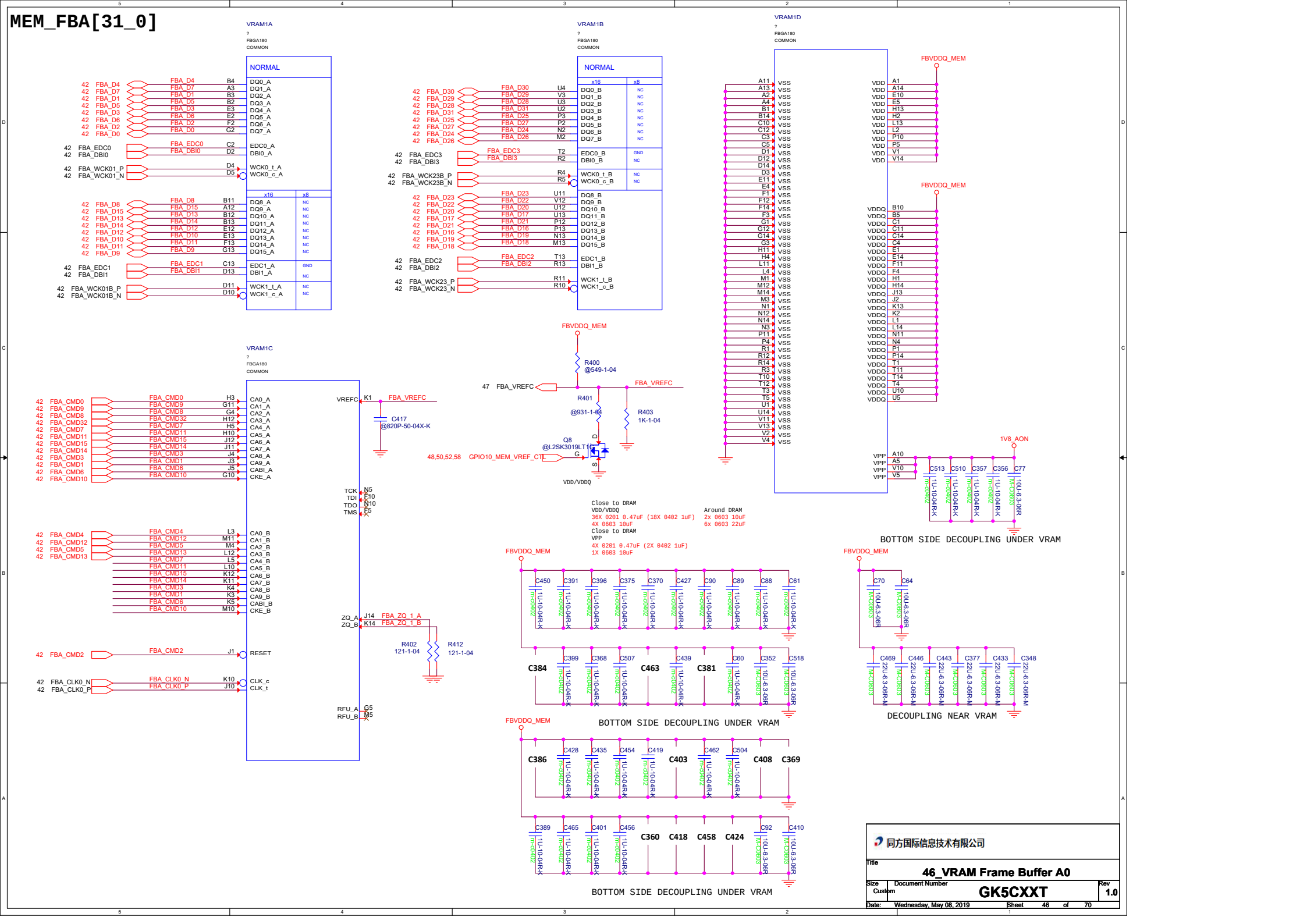
MEM_FBA[31_0]


VRAM1A
VRAM1B
VRAM1C
VRAM1D
FBGA180
COMMON
NORMAL
x16
x8
FBVDDQ_MEM
1V8_AON
R400
@549-1-04
R401
@931-1-04
R403
1K-1-04
Q8
@L2SK3019LT1G
C417
@820P-50-04X-K
Close to DRAM
VDD/VDDQ
36X 0201 0.47uF (18X 0402 1uF)
4X 0603 10uF
Close to DRAM
VPP
4X 0201 0.47uF (2X 0402 1uF)
1X 0603 10uF
Around DRAM
2x 0603 10uF
6x 0603 22uF
BOTTOM SIDE DECOUPLING UNDER VRAM
DECOUPLING NEAR VRAM
同方国际信息技术有限公司
Title
46_VRAM Frame Buffer A0
Size
Custom
Document Number
GK5CXXT
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1.0
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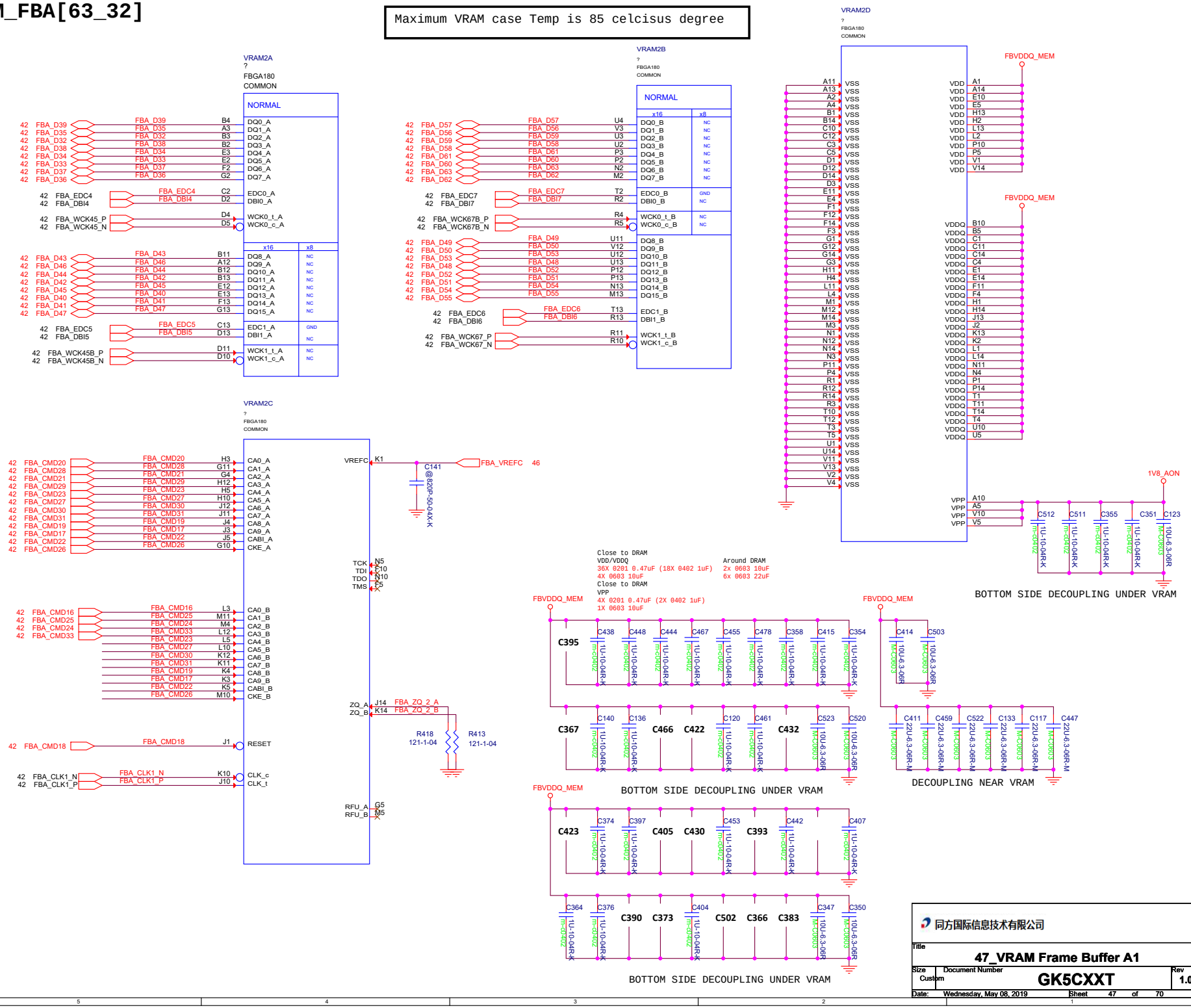
70

MEM_FBA[63_32]

Maximum VRAM case Temp is 85 celcisus degree



同方国际信息技术有限公司

Title	47_VRAM Frame Buffer A1	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
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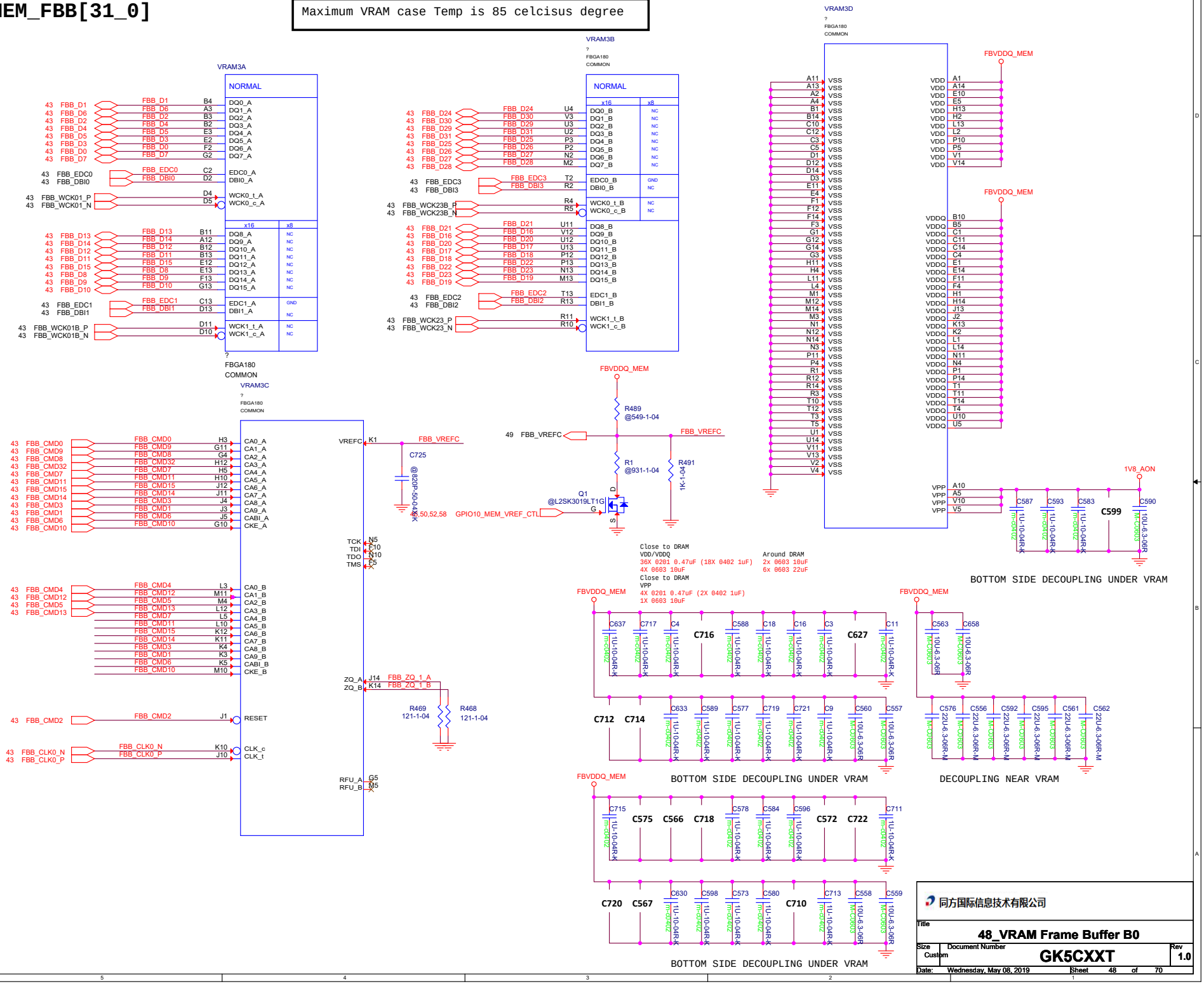
MEM_FBB[31_0]

Maximum VRAM case Temp is 85 celcisus degree



同方国际信息技术有限公司

Title	48_VRAM Frame Buffer B0	
Size: Custom	Document Number: GK5CXXT	Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 48 of 70	

MEM_FBB[63_32]

Maximum VRAM case Temp is 85 celcisus degree

VRAM4A ? FBGA180 COMMON

VRAM4B ? FBGA180 COMMON

VRAM4C ? FBGA180 COMMON

VRAM4D ? FBGA180 COMMON

FBVDDQ_MEM

1V8_AON

Close to DRAM
VDD/VDDQ
36X 0201 0.47uF (18X 0402 1uF)
4X 0603 10uF
Close to DRAM
VPP
4X 0201 0.47uF (2X 0402 1uF)
1X 0603 10uF

Around DRAM
2x 0603 10uF
6x 0603 22uF

BOTTOM SIDE DECOUPLING UNDER VRAM

DECOUPLING NEAR VRAM

同方国际信息技术有限公司	
Title	49_VRAM Frame Buffer B1
Size: Custom	Document Number: GK5CXXT
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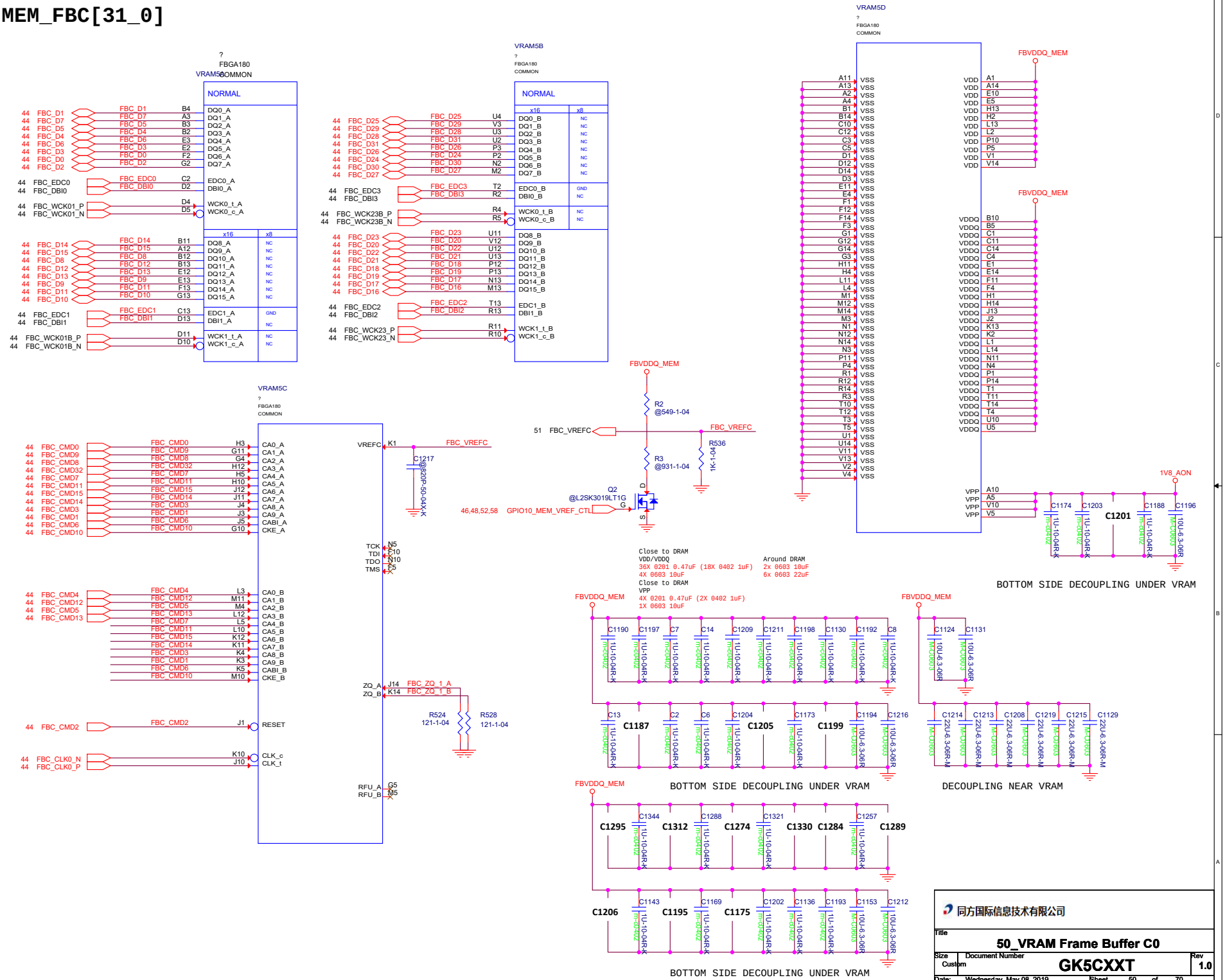
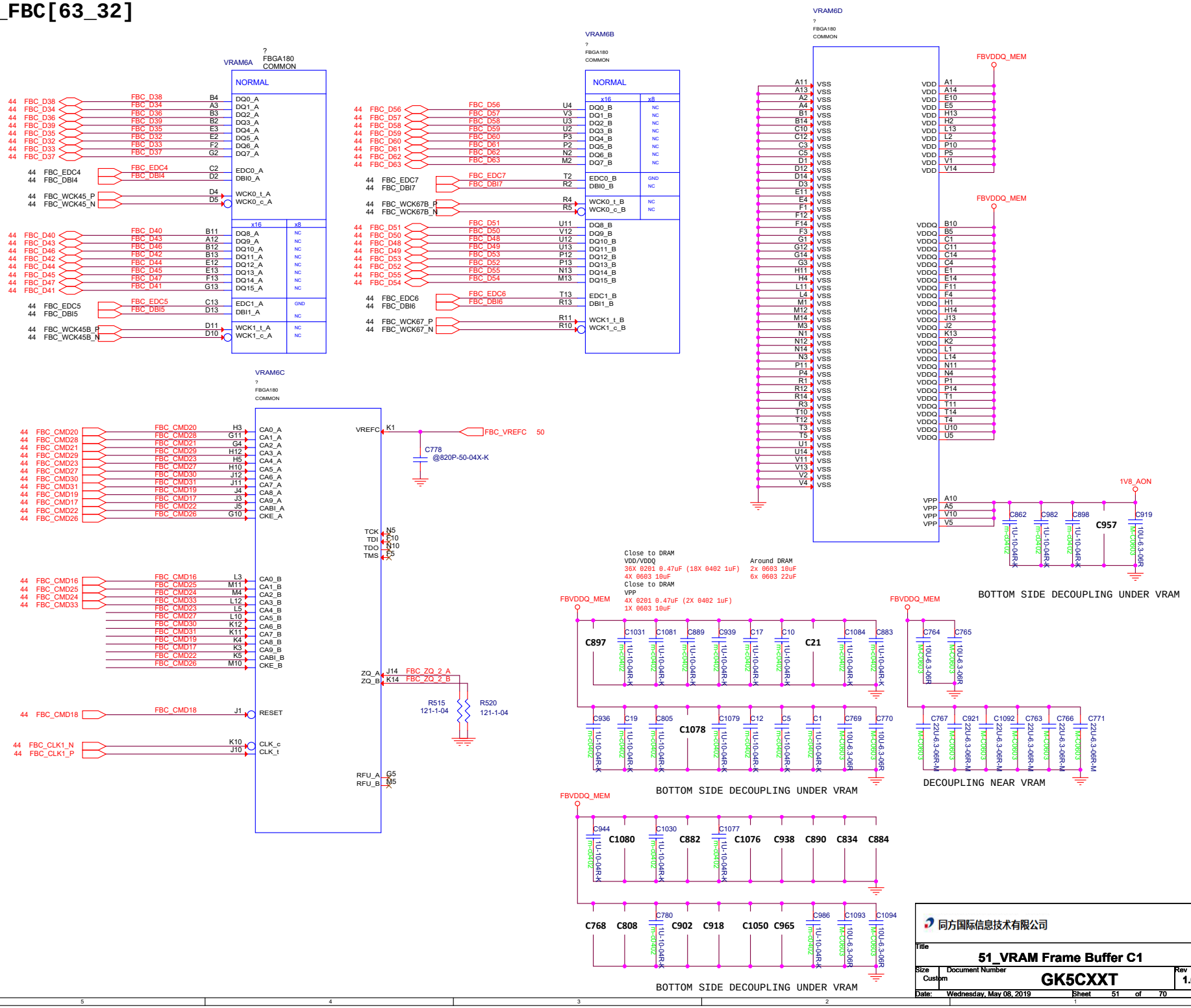
MEM_FBC[31_0]



同方国际信息技术有限公司

Title	50_VRAM Frame Buffer C0		
Size: Custom	Document Number: GK5CXXT		Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 50 of 70		

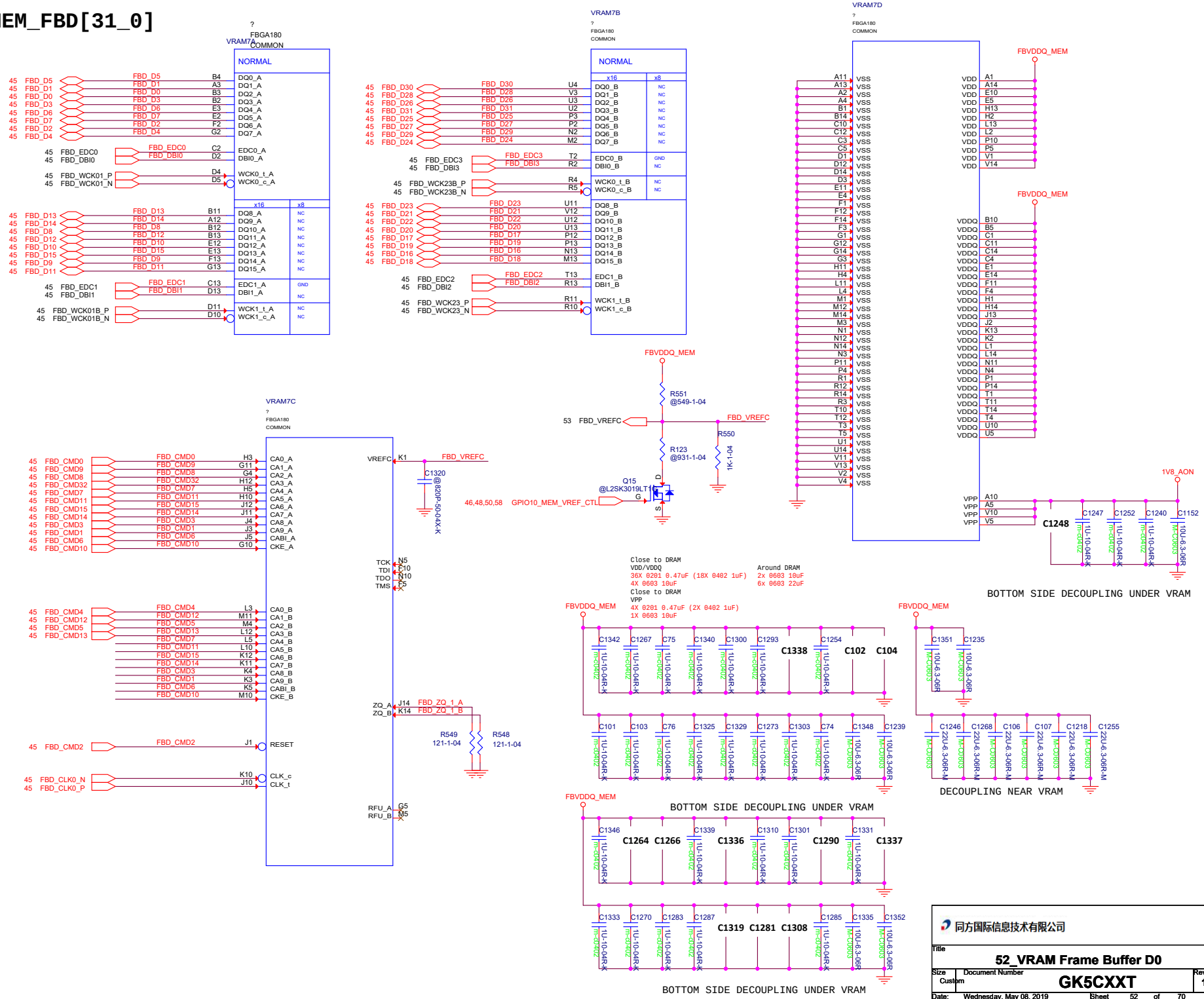
MEM_FBC[63_32]



同方国际信息技术有限公司

Title	51_VRAM Frame Buffer C1		
Size: Custom	Document Number: GK5CXXT		Rev: 1.0
Date: Wednesday, May 08, 2019	Sheet 51 of 70		

MEM_FBD[31_0]



同方国际信息技术有限公司

Title	52_VRAM Frame Buffer D0		
Size: Custom	Document Number: GK5CXXT		Rev: 1.0
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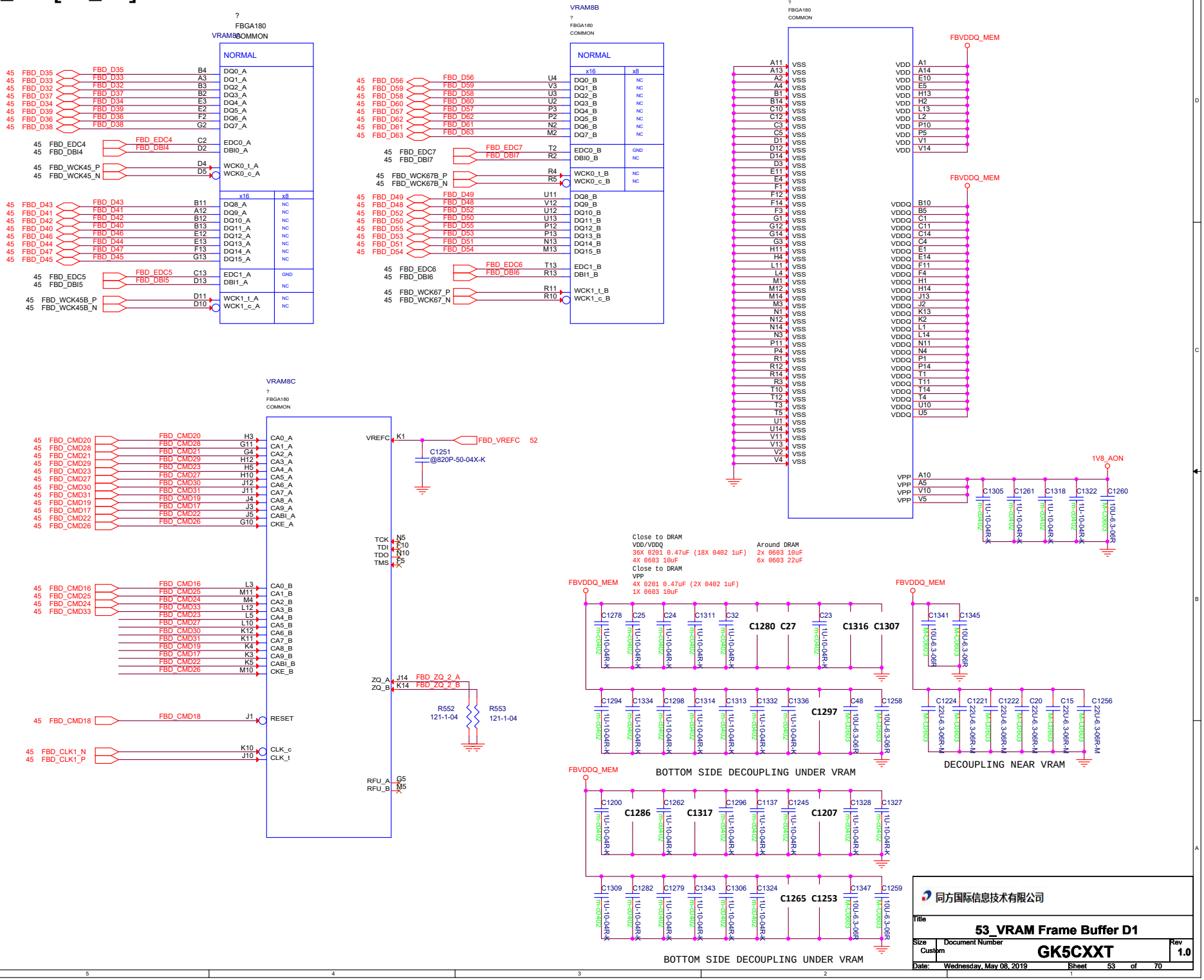
MEM_FBC[63_32]



同方国际信息技术有限公司

Title	53_VRAM Frame Buffer D1		
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N17E(GB4-256)
UNDER GPU
185X 0201 0.47uF (93X 0402 1uF)
23X 0603 10uF
4X 0805 22uF
3X 0805 47uF

NEAR GPU
2x 470uF

GPU1I
BGA2228
COMMON
17/22 VDD_1/3

GPU1M
BGA2228
COMMON
22/22 VDD_3/3

GPU1J
BGA2228
COMMON
18/22 VDD_2/3

NVVDD_SENSE
GND_SENSE
GPU_NVVDD_SENSE 61
GPU_GND_SENSE 61

PLACE UNDER GPU

BOTTOM SIDE DECOUPLING UNDER GPU

DECOUPLING NEAR GPU

同方国际信息技术有限公司

Title: 54_GPU N18E PWR NVVDD

Size: C | Document Number: GK5CXXT | Rev: 1.0

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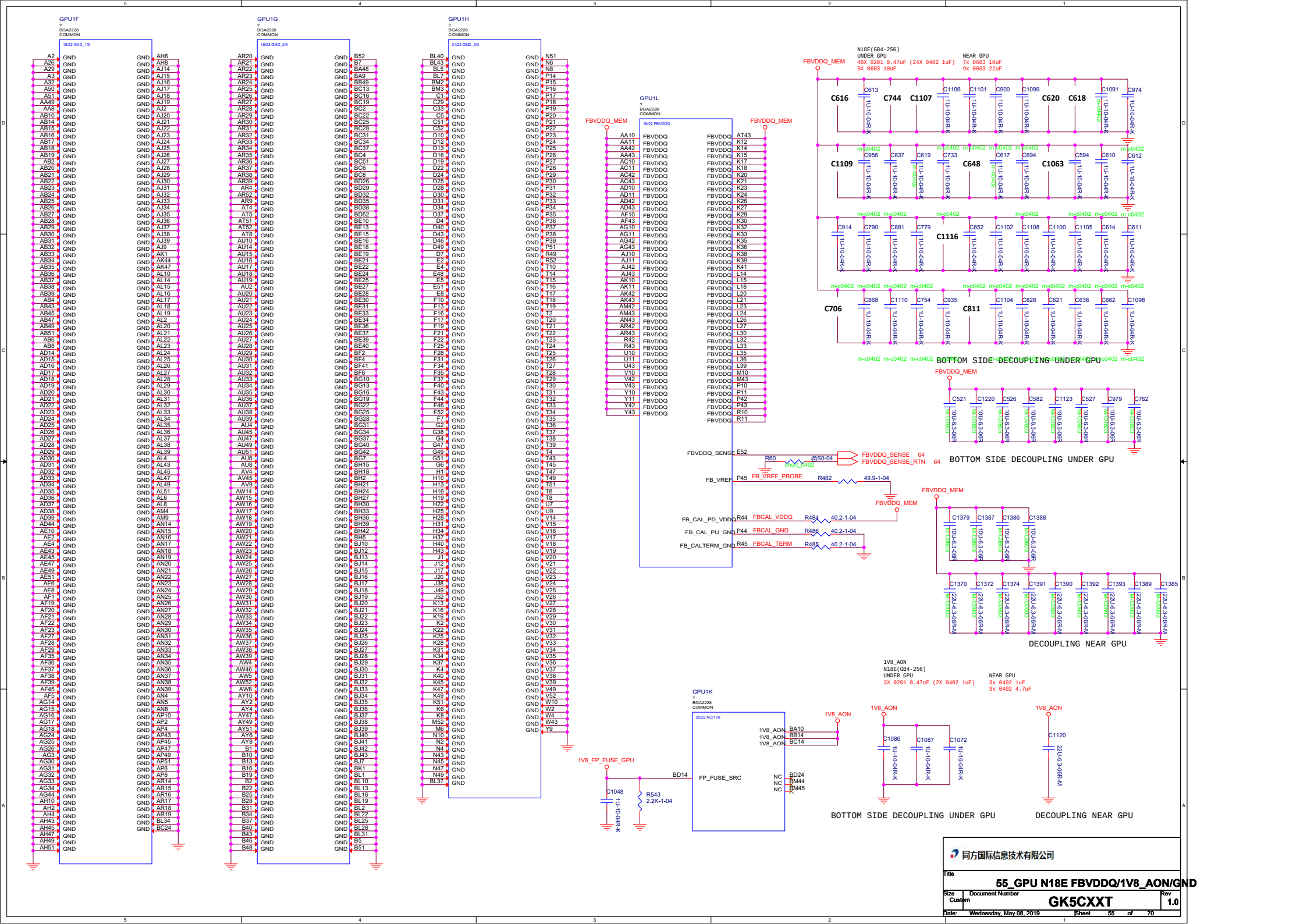
GPU1F
BGA2228
COMMON
GPU1G
BGA2228
COMMON
GPU1H
BGA2228
COMMON
GPU1L
BGA2228
COMMON
GPU1K
BGA2228
COMMON
FBVDDQ_MEM
N18E(GB4-256)
UNDER GPU
48X 0201 0.47uF (24X 0402 1uF)
5X 0603 10uF
NEAR GPU
7x 0603 10uF
9x 0603 22uF
BOTTOM SIDE DECOUPLING UNDER GPU
DECOUPLING NEAR GPU
FBVDDQ_SENSE
FBVDDQ_SENSE_RTN
FB_VREF
FB_VREF_PROBE
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CALTERM_GND
1V8_AON
1V8_FP_FUSE_GPU
FP_FUSE_SRC
同方国际信息技术有限公司
55_GPU N18E FBVDDQ/1V8_AON/GND
GK5CXXT
Wednesday, May 08, 2019

Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used, it should be NC
including power rail and signal and references
associated with LINKX

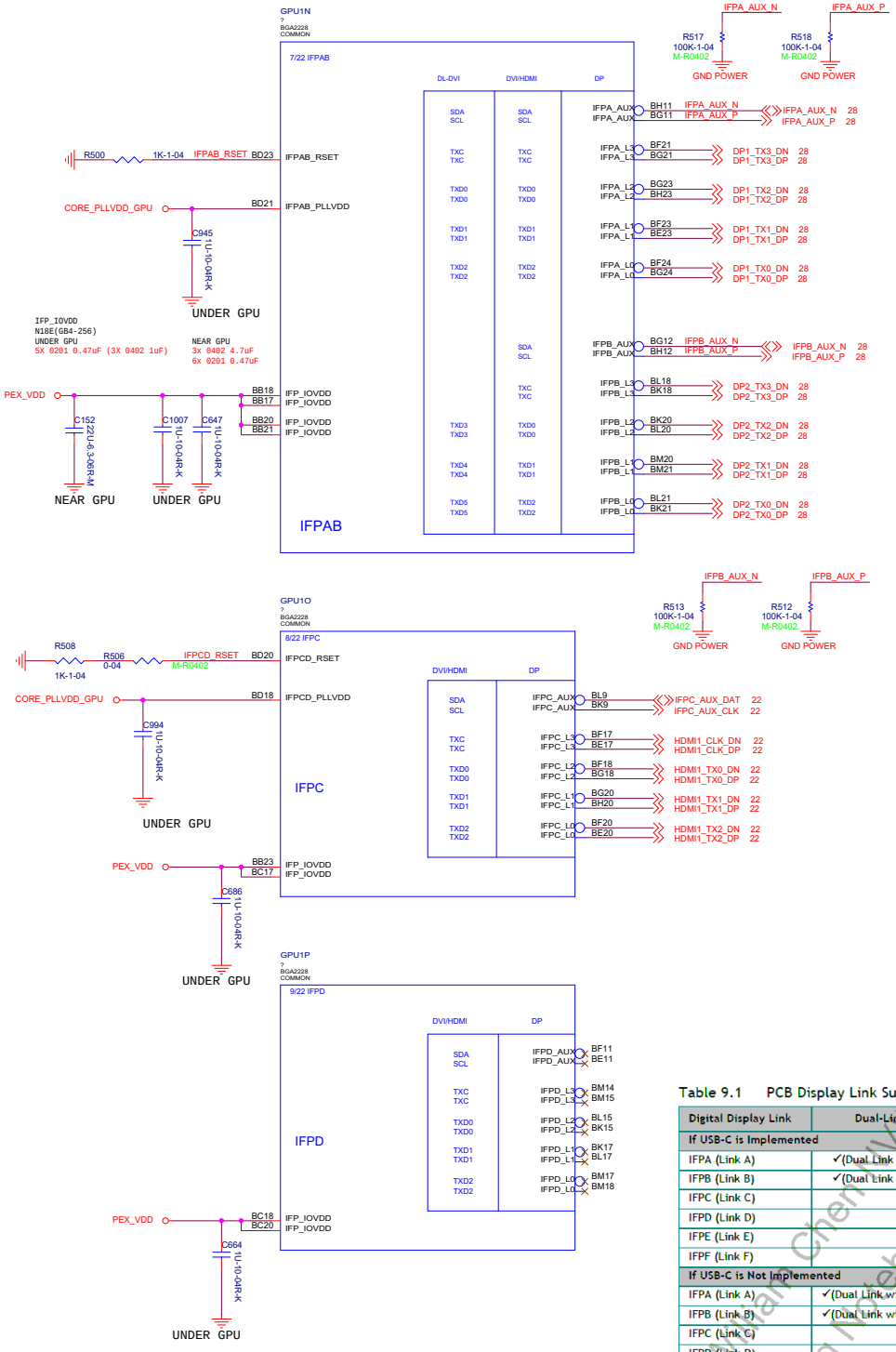

Table 9.1 PCB Display Link Summary (GB4B-256 packages)

Digital Display Link	Dual-Link DVI	HDMI / eDP	DisplayPort	USBC
If USB-C is Implemented				
IFPA (Link A)	✓(Dual Link with IFPB)		✓	
IFPB (Link B)	✓(Dual Link with IFPA)			
IFPC (Link C)		✓	✓	
IFPD (Link D)		✓	✓	
IFPE (Link E)		✓	✓	
IFPF (Link F)				✓
If USB-C is Not Implemented				
IFPA (Link A)	✓(Dual Link with IFPB)		✓	
IFPB (Link B)	✓(Dual Link with IFPA)		✓	
IFPC (Link C)		✓	✓	
IFPD (Link D)		✓		
IFPE (Link E)		✓	✓	
IFPF (Link F)			✓	

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Title: 56_GPU N18E_IPFA_B_C_D_E_F

Size: Custom | Document Number: GK5CXXT | Rev: 1.0

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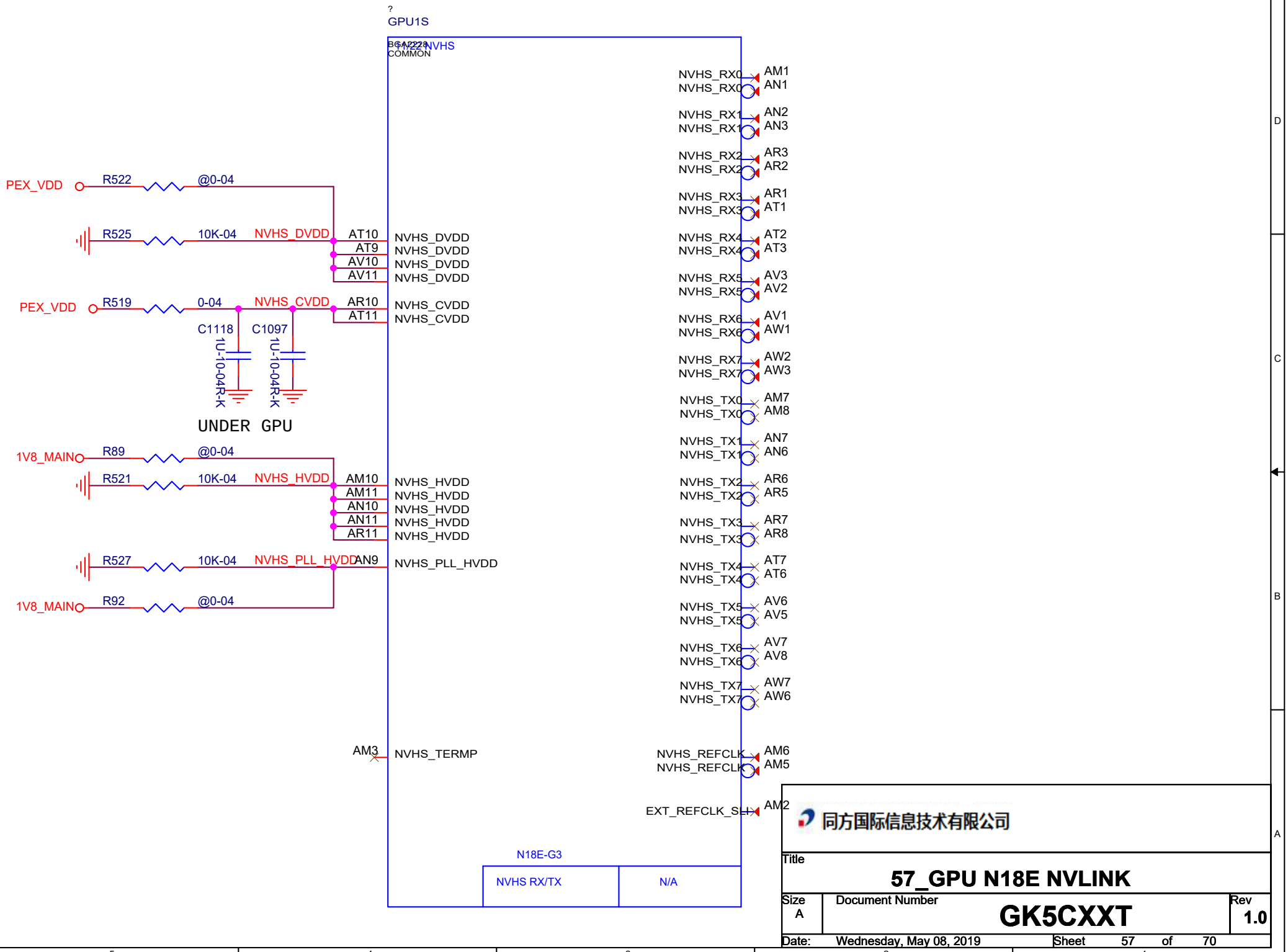

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Title: 57_GPU N18E NVLINK

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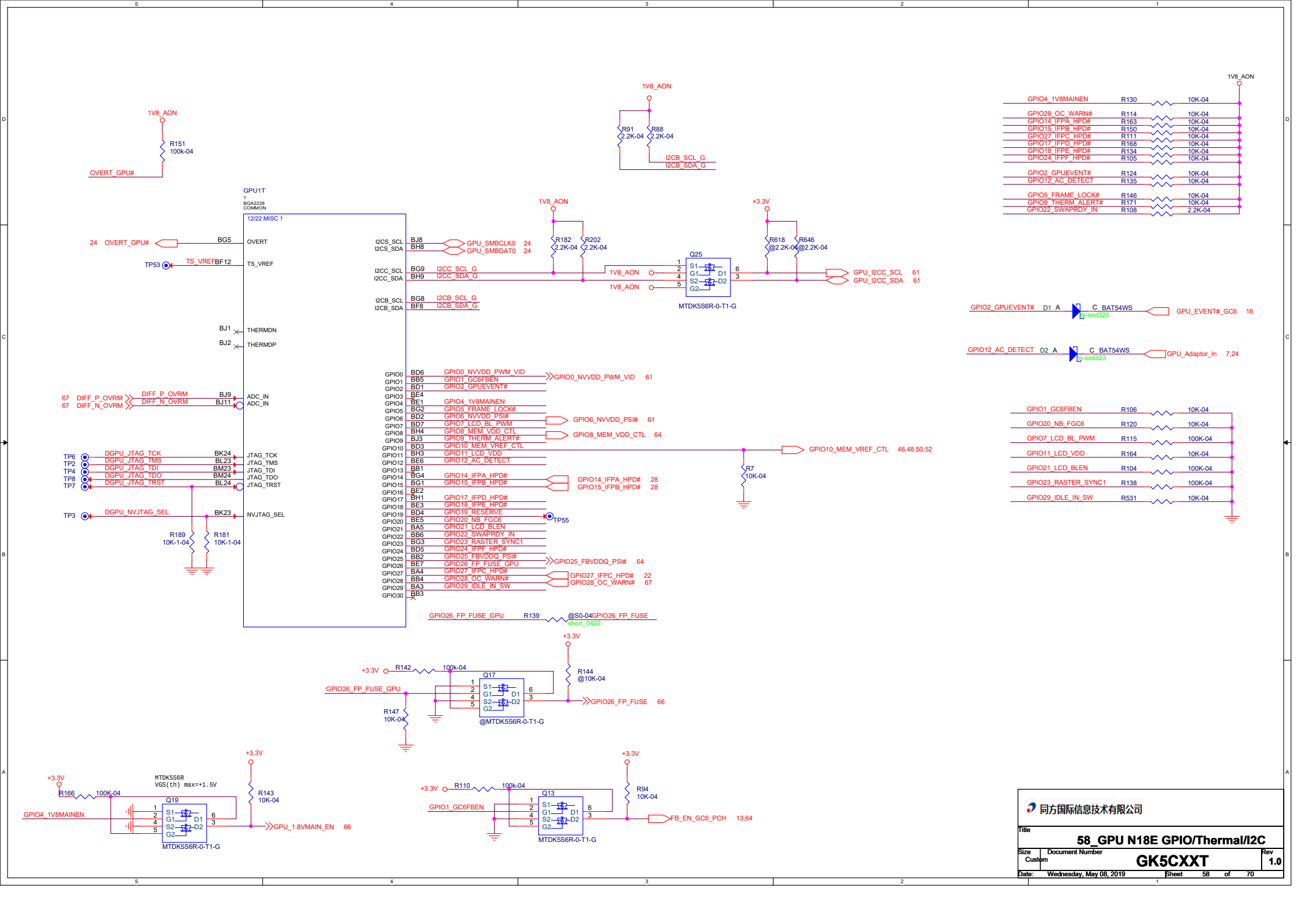
1V8_AON
R151
100k-04
OVERT_GPU#
GPU1T
BGA2228
COMMON
12/22 MISC 1
24 OVERT_GPU#
BG5 OVERT
TP53
TS_VREF BF12 TS_VREF
BJ1 THERMDN
BJ2 THERMDP
67 DIFF_P_OVRM
67 DIFF_N_OVRM
DIFF_P_OVRM BJ9 ADC_IN
DIFF_N_OVRM BJ11 ADC_IN
TP6 DGPU_JTAG_TCK BK24 JTAG_TCK
TP2 DGPU_JTAG_TMS BL23 JTAG_TMS
TP4 DGPU_JTAG_TDI BM23 JTAG_TDI
TP8 DGPU_JTAG_TDO BM24 JTAG_TDO
TP7 DGPU_JTAG_TRST BL24 JTAG_TRST
TP3 DGPU_NVJTAG_SEL BK23 NVJTAG_SEL
R189
10K-1-04
R181
10K-1-04
I2CS_SCL BJ8 GPU_SMBCLK0 24
I2CS_SDA BH8 GPU_SMBDAT0 24
I2CC_SCL BG9 I2CC_SCL_G
I2CC_SDA BH9 I2CC_SDA_G
I2CB_SCL BG8 I2CB_SCL_G
I2CB_SDA BF8 I2CB_SDA_G
1V8_AON
R91
2.2K-04
R88
2.2K-04
I2CB_SCL_G
I2CB_SDA_G
1V8_AON
R182
2.2K-04
R202
2.2K-04
Q25
MTDK5S6R-0-T1-G
+3.3V
R618
@2.2K-04
R646
@2.2K-04
GPU_I2CC_SCL 61
GPU_I2CC_SDA 61
GPIO0 BD6 GPIO0_NVVDD_PWM_VID
GPIO1 BB5 GPIO1_GC6FBEN
GPIO2 BD1 GPIO2_GPUEVENT#
GPIO3 BE4
GPIO4 BE1 GPIO4_1V8MAINEN
GPIO5 BG2 GPIO5_FRAME_LOCK#
GPIO6 BD2 GPIO6_NVVDD_PSI#
GPIO7 BD7 GPIO7_LCD_BL_PWM
GPIO8 BH4 GPIO8_MEM_VDD_CTL
GPIO9 BJ3 GPIO9_THERM_ALERT#
GPIO10 BD3 GPIO10_MEM_VREF_CTL
GPIO11 BH3 GPIO11_LCD_VDD
GPIO12 BE6 GPIO12_AC_DETECT
GPIO13 BB1
GPIO14 BG4 GPIO14_IFPA_HPD#
GPIO15 BG1 GPIO15_IFPB_HPD#
GPIO16 BE2
GPIO17 BH1 GPIO17_IFPD_HPD#
GPIO18 BE3 GPIO18_IFPE_HPD#
GPIO19 BD4 GPIO19_RESERVE
GPIO20 BE5 GPIO20_NB_FGC6
GPIO21 BA5 GPIO21_LCD_BLEN
GPIO22 BB6 GPIO22_SWAPRDY_IN
GPIO23 BG3 GPIO23_RASTER_SYNC1
GPIO24 BD5 GPIO24_IFPF_HPD#
GPIO25 BB2 GPIO25_FBVDDQ_PSI#
GPIO26 BE7 GPIO26_FP_FUSE_GPU
GPIO27 BA4 GPIO27_IFPC_HPD#
GPIO28 BB4 GPIO28_OC_WARN#
GPIO29 BA3 GPIO29_IDLE_IN_SW
GPIO30 BB3
GPIO0_NVVDD_PWM_VID 61
GPIO6_NVVDD_PSI# 61
GPIO8_MEM_VDD_CTL 64
GPIO10_MEM_VREF_CTL 46,48,50,52
R7
10K-04
GPIO14_IFPA_HPD# 28
GPIO15_IFPB_HPD# 28
TP55
GPIO25_FBVDDQ_PSI# 64
GPIO27_IFPC_HPD# 22
GPIO28_OC_WARN# 67
GPIO26_FP_FUSE_GPU R139 @S0-04 GPIO26_FP_FUSE
short_0402
+3.3V
R142 100k-04
Q17
@MTDK5S6R-0-T1-G
R144
@10K-04
R147
10K-04
GPIO26_FP_FUSE 66
+3.3V
R166 100k-04
MTDK5S6R
VGS(th) max=+1.5V
Q19
MTDK5S6R-0-T1-G
R143
10K-04
GPIO4_1V8MAINEN
GPU_1.8VMAIN_EN 66
+3.3V
R110 100k-04
Q13
MTDK5S6R-0-T1-G
R94
10K-04
GPIO1_GC6FBEN
FB_EN_GC6_PCH 13,64
1V8_AON
GPIO4_1V8MAINEN R130 10K-04
GPIO28_OC_WARN# R114 10K-04
GPIO14_IFPA_HPD# R163 10K-04
GPIO15_IFPB_HPD# R150 10K-04
GPIO27_IFPC_HPD# R111 10K-04
GPIO17_IFPD_HPD# R168 10K-04
GPIO18_IFPE_HPD# R134 10K-04
GPIO24_IFPF_HPD# R105 10K-04
GPIO2_GPUEVENT# R124 10K-04
GPIO12_AC_DETECT R135 10K-04
GPIO5_FRAME_LOCK# R146 10K-04
GPIO9_THERM_ALERT# R171 10K-04
GPIO22_SWAPRDY_IN R108 2.2K-04
GPIO2_GPUEVENT# D1 A
C BAT54WS
D-sod323
GPU_EVENT#_GC6 16
GPIO12_AC_DETECT D2 A
C BAT54WS
D-sod323
GPU_Adaptor_In 7,24
GPIO1_GC6FBEN R106 10K-04
GPIO20_NB_FGC6 R120 10K-04
GPIO7_LCD_BL_PWM R115 100K-04
GPIO11_LCD_VDD R164 10K-04
GPIO21_LCD_BLEN R104 100K-04
GPIO23_RASTER_SYNC1 R138 100K-04
GPIO29_IDLE_IN_SW R531 10K-04
同方国际信息技术有限公司
Title
58_GPU N18E GPIO/Thermal/I2C
Size
Custom
Document Number
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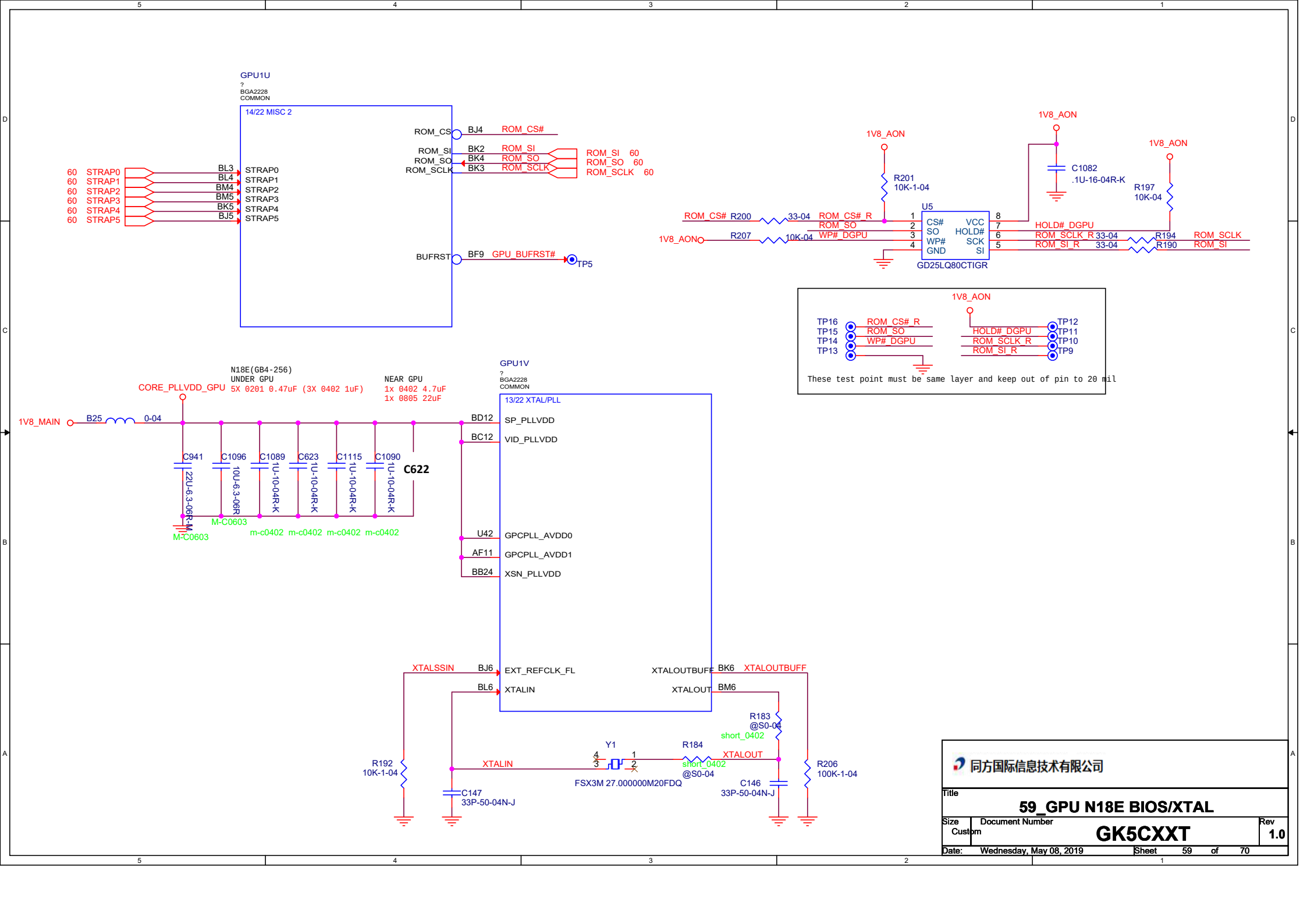

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Title	59_GPU N18E BIOS/XTAL	
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	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

Table 11.4 FS_OVERT* Strap Enablement

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note that configurations other than the two listed in Table 11.4 must be avoided, as otherwise damage to strap inputs may result.

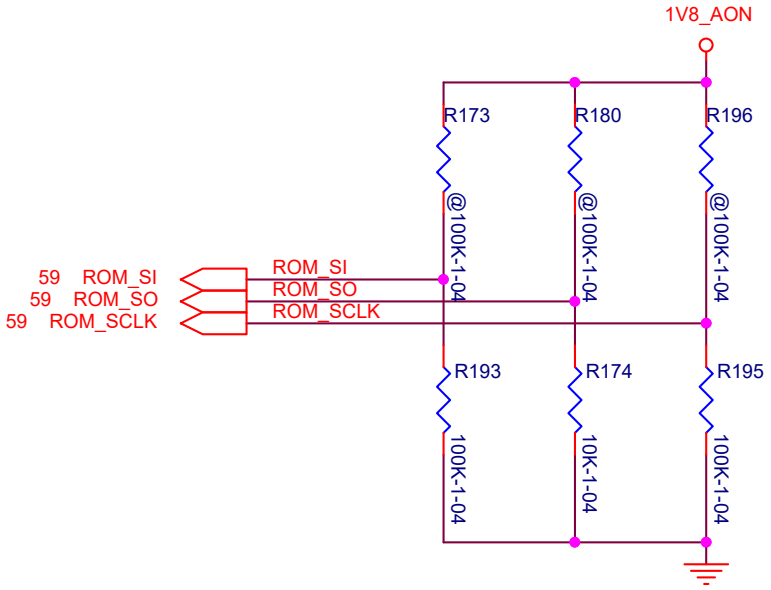
For N18x GPUs the hardware (on-PCB) SOR_EXPOSED straps are redacted; ROM_SO, ROM_SI and ROM_SCLK straps are no longer provided. The register-based method for configuring audio for display links is the only method provided. This method is implemented in VBIOS settings.

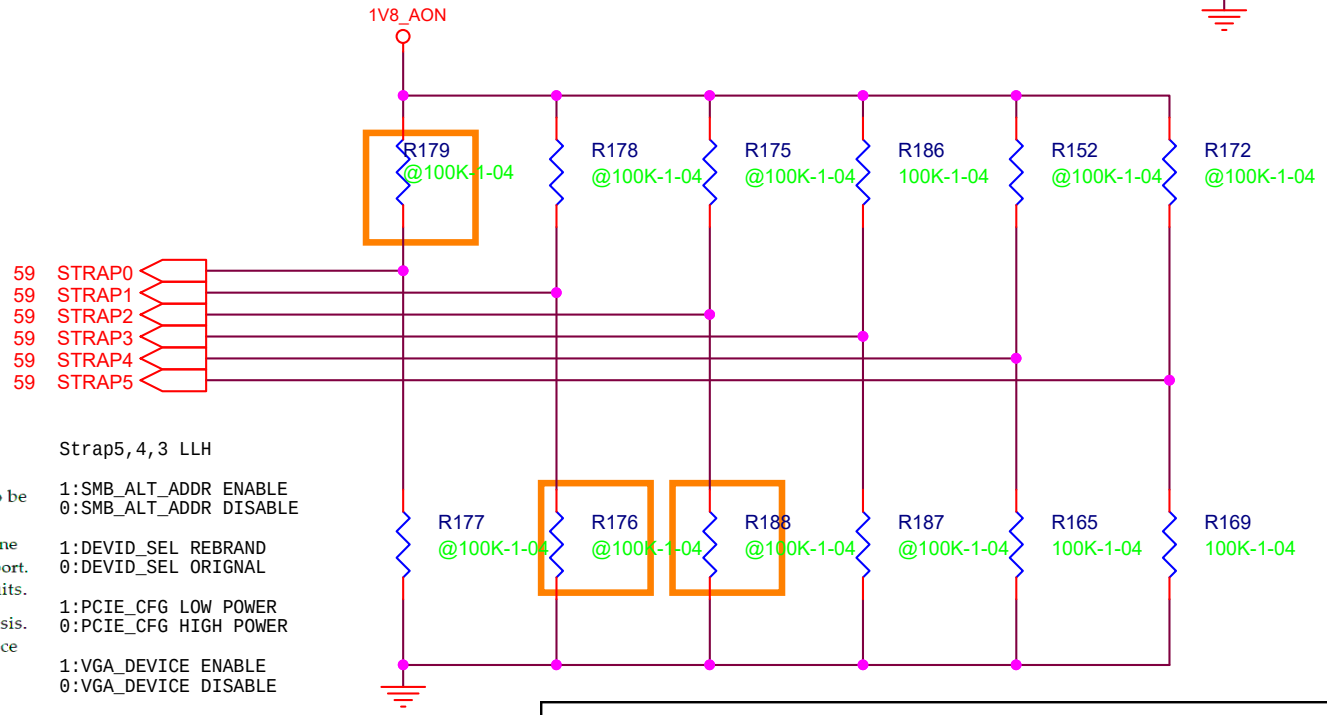
Based on RVL_07916_001_V10 JUNE 2017

GDDR5						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H
8Gb	Hynix	H56C8H24MJR-S4C M-die	0X2	L	H	L
4Gb	Samsung		0X7	H	H	H
4Gb	Hynix		0X6	H	H	L
4Gb	Micron					

POWER

1.25V/1.35V
1.25V/1.35V
1.25V/1.35V N18E-G2 only





Strap5,4,3 LLH

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

- **SMB_ALT_ADDR Enable**: This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits.
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG**: This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N18x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits (consult NVIDIA for details on proper bit setting for MS-Hybrid solutions).

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Title	60_GPU N18E STRAP	
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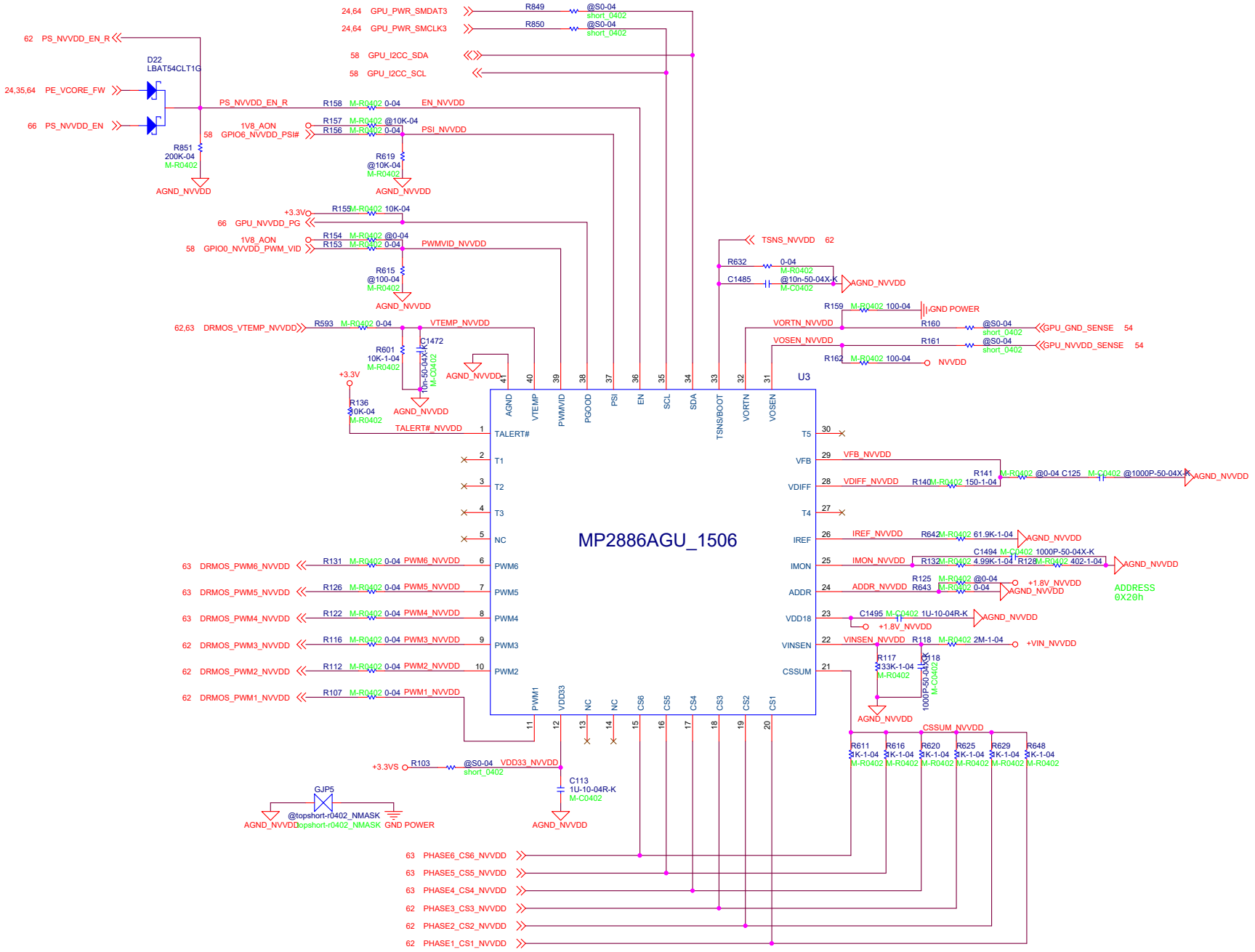

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Title: 61_POWER N18E NVVDD CONTROLLER

Size: Custom | Document Number: GK5CXXT | Rev: 1.0

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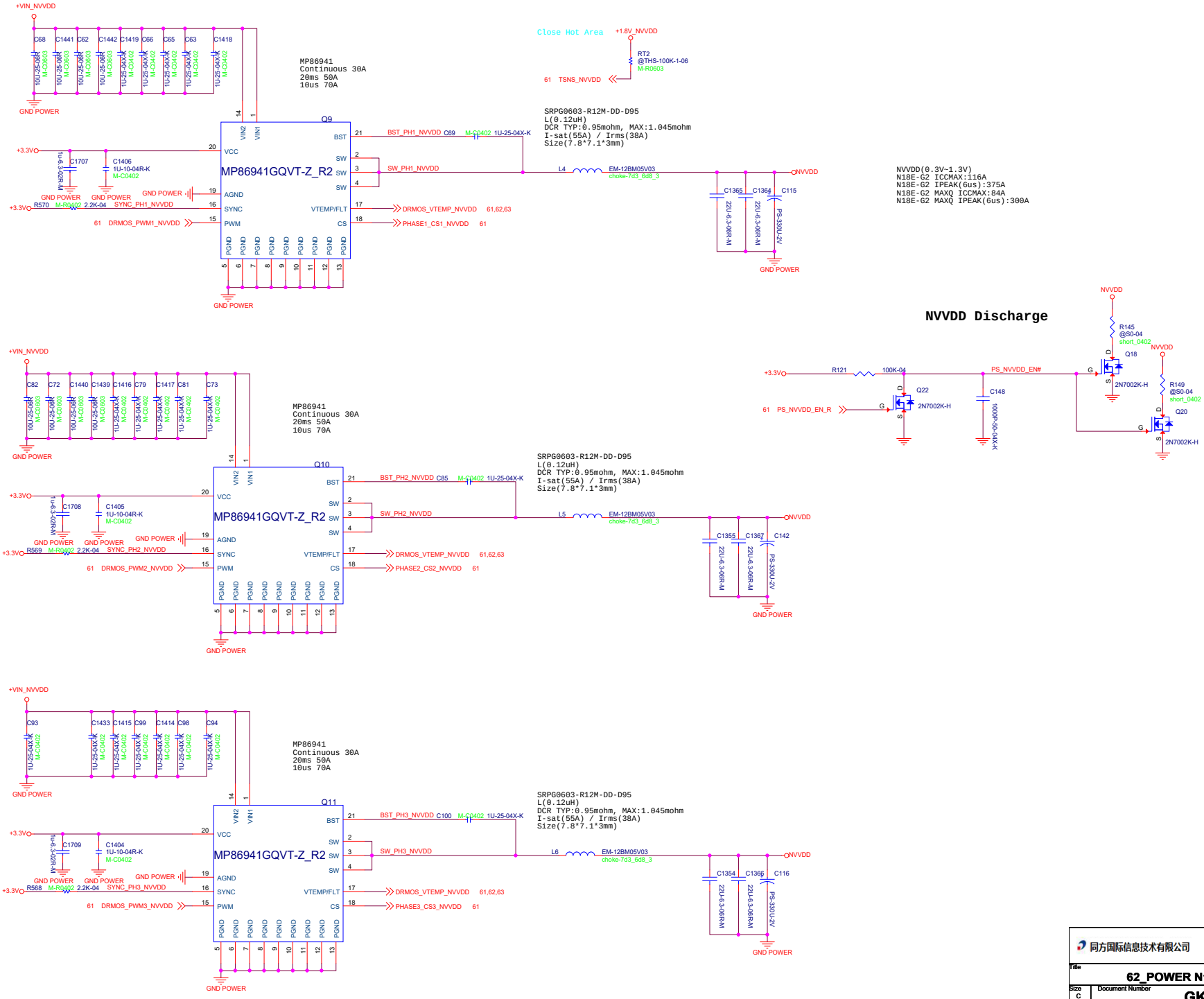
+VIN_NVVDD
C68 C1441 C62 C1442 C1419 C66 C65 C63 C1418
GND POWER
MP86941
Continuous 30A
20ms 50A
10us 70A
Close Hot Area
+1.8V_NVVDD
RT2
@THS-100K-1-06
M-R0603
61 TSNS_NVVDD
Q9
MP86941GQVT-Z_R2
VIN2 VIN1 BST SW SW SW VCC AGND SYNC VTEMP/FLT PWM CS PGND
BST_PH1_NVVDD C69 M-C0402 1U-25-04X-K
SW_PH1_NVVDD
SRPG0603-R12M-DD-D95
L(0.12uH)
DCR TYP:0.95mohm, MAX:1.045mohm
I-sat(55A) / Irms(38A)
Size(7.8*7.1*3mm)
L4 EM-12BM05V03 choke-7d3_6d8_3
+3.3V
C1707 1u-6.3-02R-M
C1406 1U-10-04R-K M-C0402
R570 M-R0402 2.2K-04
SYNC_PH1_NVVDD
61 DRMOS_PWM1_NVVDD
DRMOS_VTEMP_NVVDD 61,62,63
PHASE1_CS1_NVVDD 61
C1365 C1364 C115
22U-6.3-06R-M
PS-330U-2V
NVVDD
NVVDD(0.3V~1.3V)
N18E-G2 ICCMAX:116A
N18E-G2 IPEAK(6us):375A
N18E-G2 MAXQ ICCMAX:84A
N18E-G2 MAXQ IPEAK(6us):300A
NVVDD Discharge
R121 100K-04
PS_NVVDD_EN#
61 PS_NVVDD_EN_R
Q22 2N7002K-H
C148 1000P-50-04X-K
R145 @S0-04 short_0402
Q18 2N7002K-H
R149 @S0-04 short_0402
Q20 2N7002K-H
Q10
C1708 1u-6.3-02R-M
C1405 1U-10-04R-K M-C0402
R569 M-R0402 2.2K-04
SYNC_PH2_NVVDD
61 DRMOS_PWM2_NVVDD
BST_PH2_NVVDD C85 M-C0402 1U-25-04X-K
SW_PH2_NVVDD
L5 EM-12BM05V03 choke-7d3_6d8_3
C1355 C1367 C142
Q11
C1709 1u-6.3-02R-M
C1404 1U-10-04R-K M-C0402
R568 M-R0402 2.2K-04
SYNC_PH3_NVVDD
61 DRMOS_PWM3_NVVDD
BST_PH3_NVVDD C100 M-C0402 1U-25-04X-K
SW_PH3_NVVDD
L6 EM-12BM05V03 choke-7d3_6d8_3
C1354 C1366 C116
同方国际信息技术有限公司
Title
62_POWER N18E NVVDD 3PHASE_1/2
Size C
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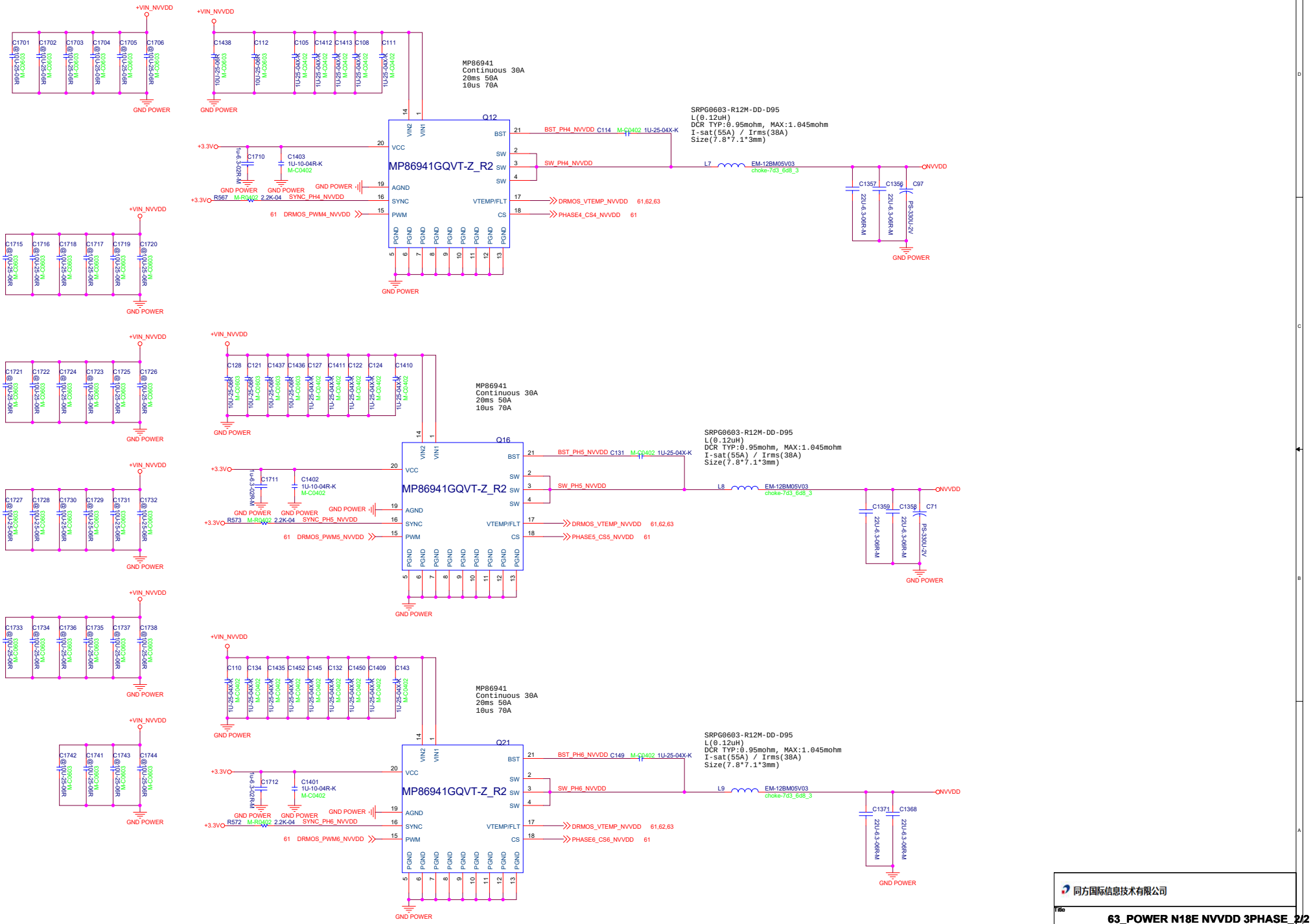

同方国际信息技术有限公司

Title	63_POWER N18E NVVDD 3PHASE_2/2	
Size C	Document Number GK5CXXT	Rev 1.0
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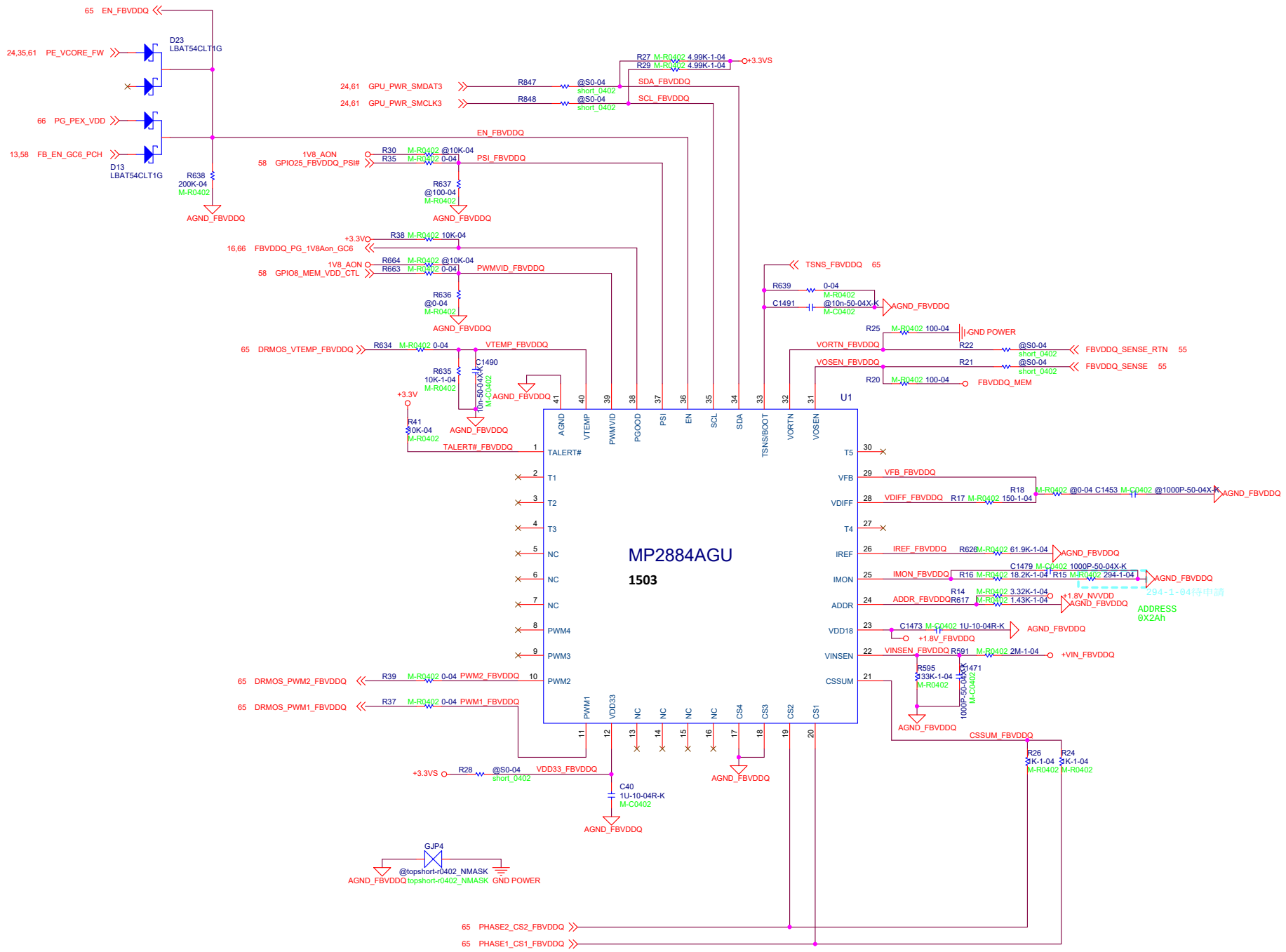

同方国际信息技术有限公司

Title: 64_POWER N18E FBVDDQ CONTROLLER

Size	Document Number	Rev
Custom	GK5CXXT	1.0

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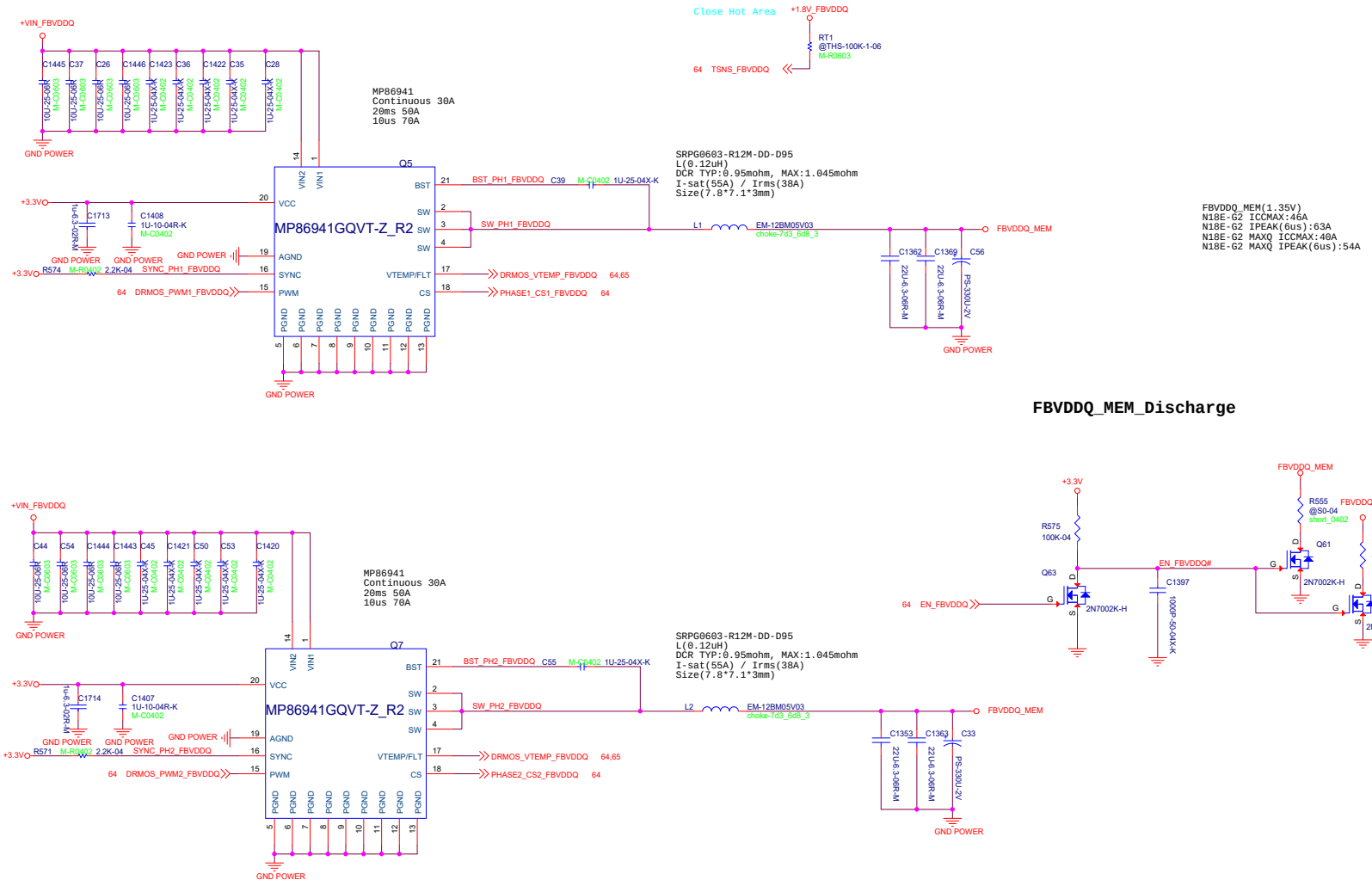

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Title	65_POWER N18E FBVDDQ 2PHASE	
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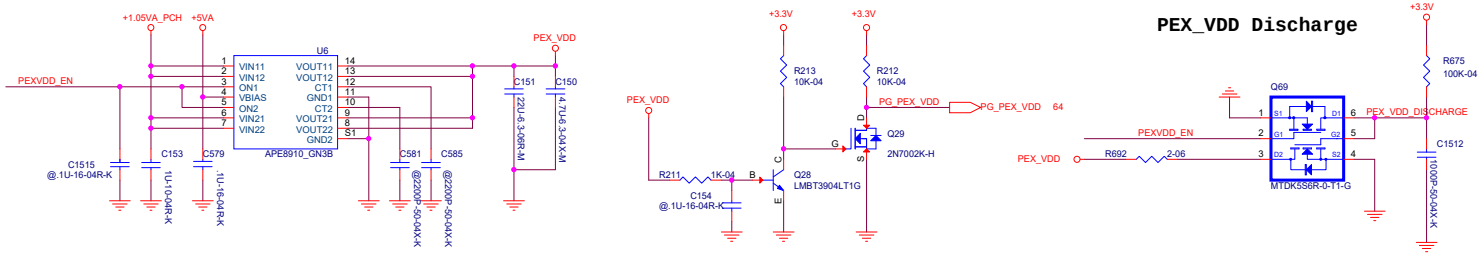
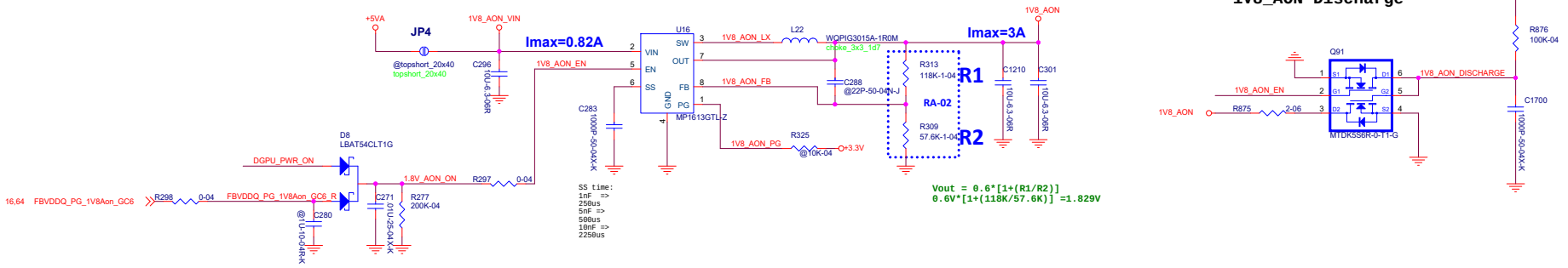
PEX_VDD SW

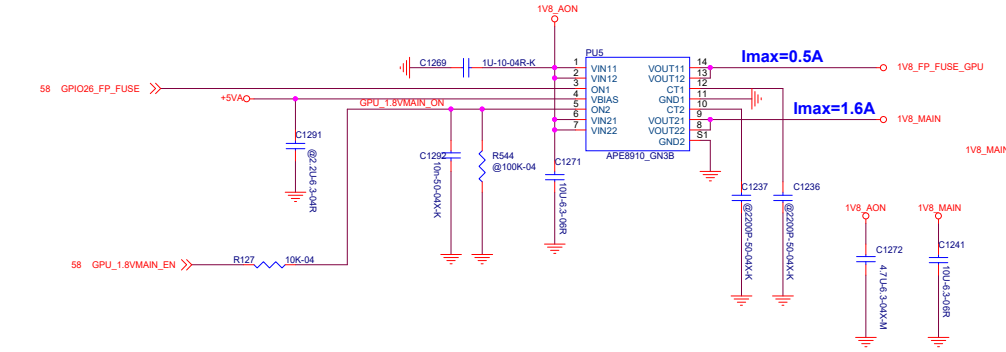


1V8_AON/1V8_MAIN

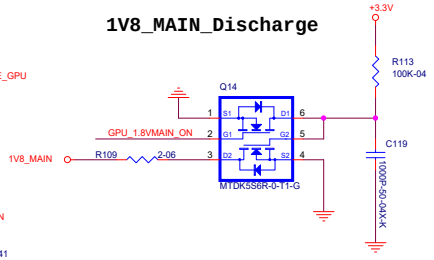
WQPIG3015A-1R0M
L(1uH) / DCR TYP=42mohm, MAX=45mohm
I-sat=4.8A / Irms=4.1A
Size(3*3*1.5mm)

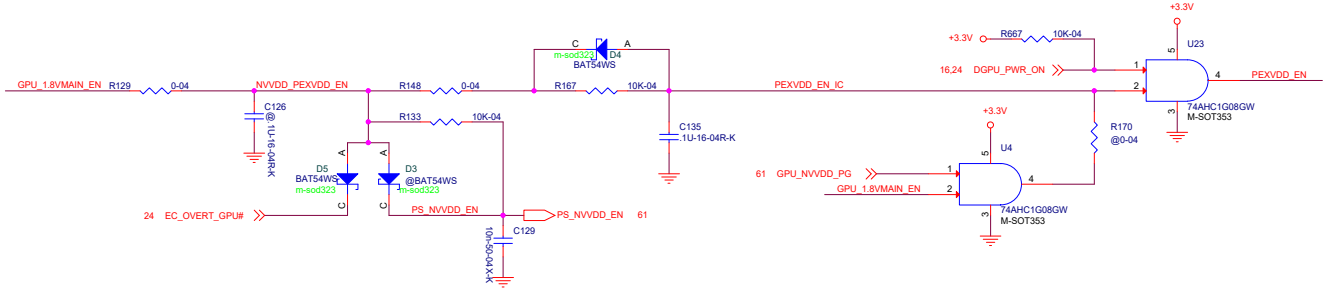


1V8_AON Discharge



1V8_MAIN_Discharge





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Title	66_POWER N18E PEX_VDD/1V8_AON	
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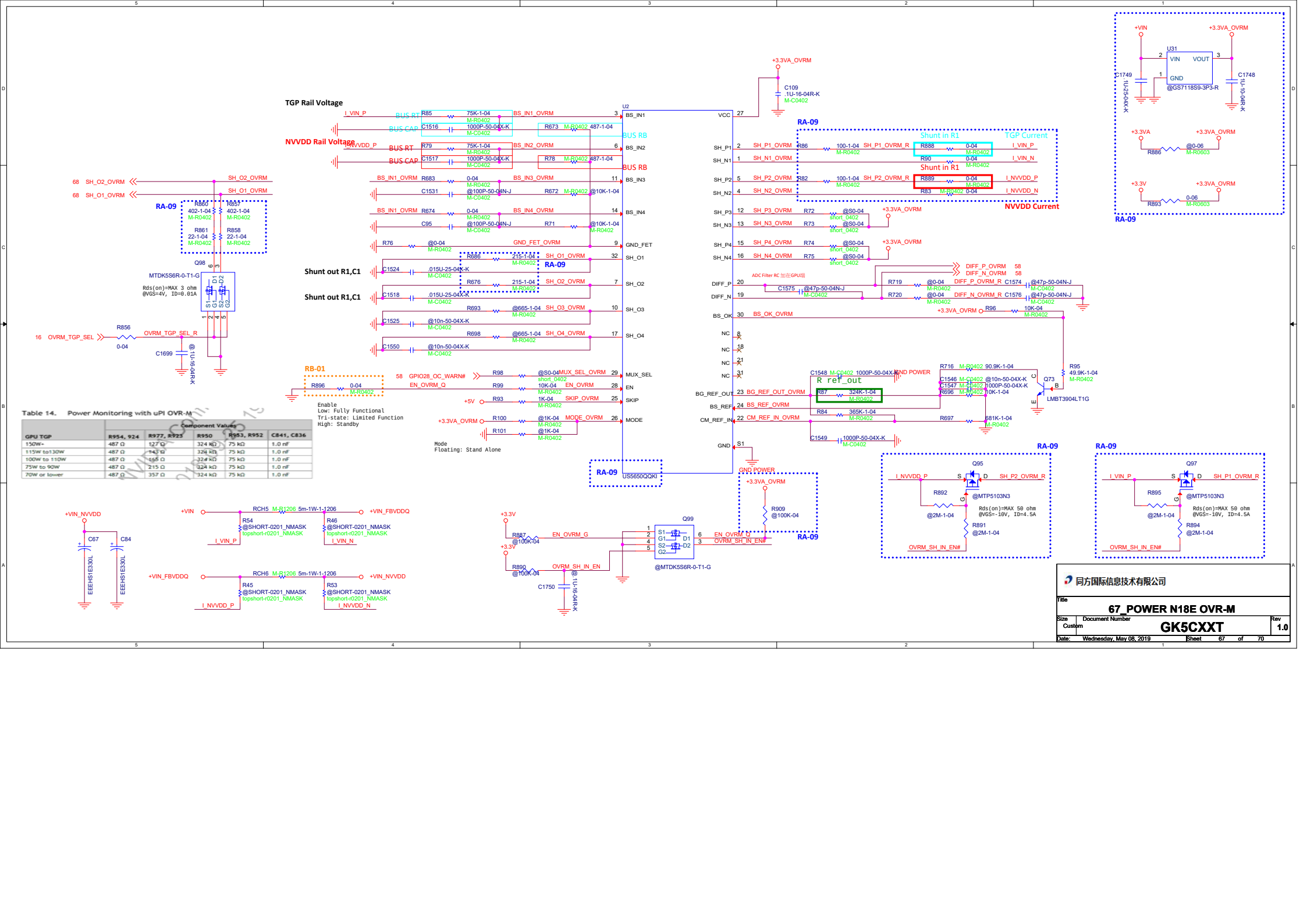
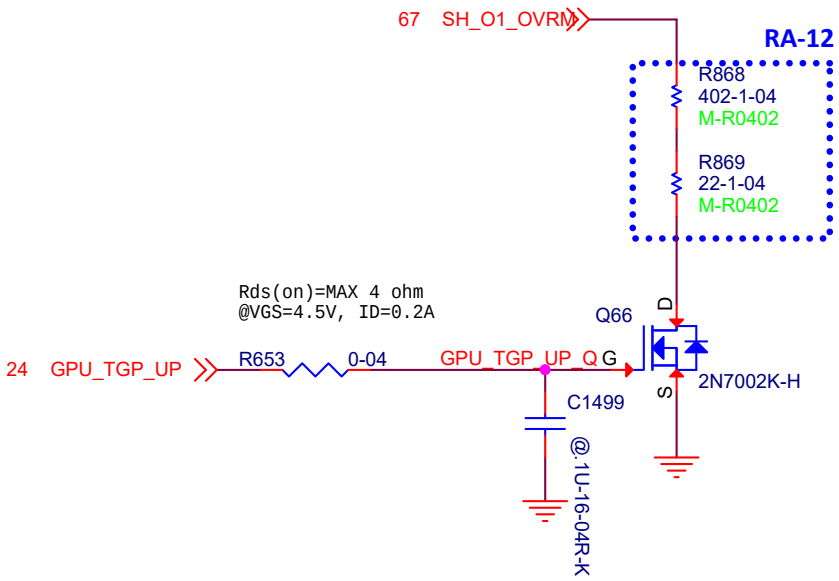
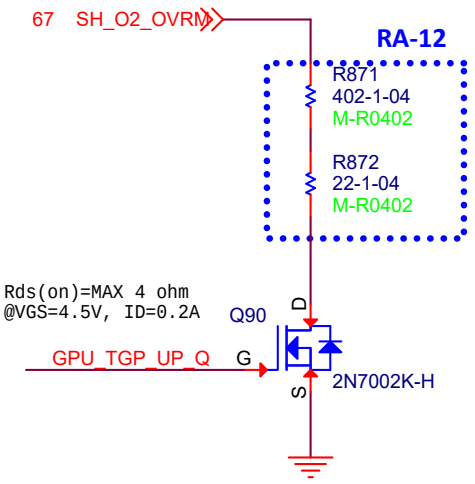


Table 14. Power Monitoring with uPI OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	487 Ω	127 Ω	324 kΩ	75 kΩ	1.0 nF
115W to130W	487 Ω	143 Ω	324 kΩ	75 kΩ	1.0 nF
100W to 110W	487 Ω	165 Ω	324 kΩ	75 kΩ	1.0 nF
75W to 90W	487 Ω	215 Ω	324 kΩ	75 kΩ	1.0 nF
70W or lower	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF





TGP Control / TGP Watt	GPU_TGP_UP	OVRM_TGP_SEL
OVER 130W	High	High
100W to 110W	High	Low
115W to 130W (7S)	Low	High
75W to 90W (7Z)	Low	Low

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Title: 68_POWER N18E TGP OFFSET

Size	Document Number	Rev
A	GK5CXXT	1.0

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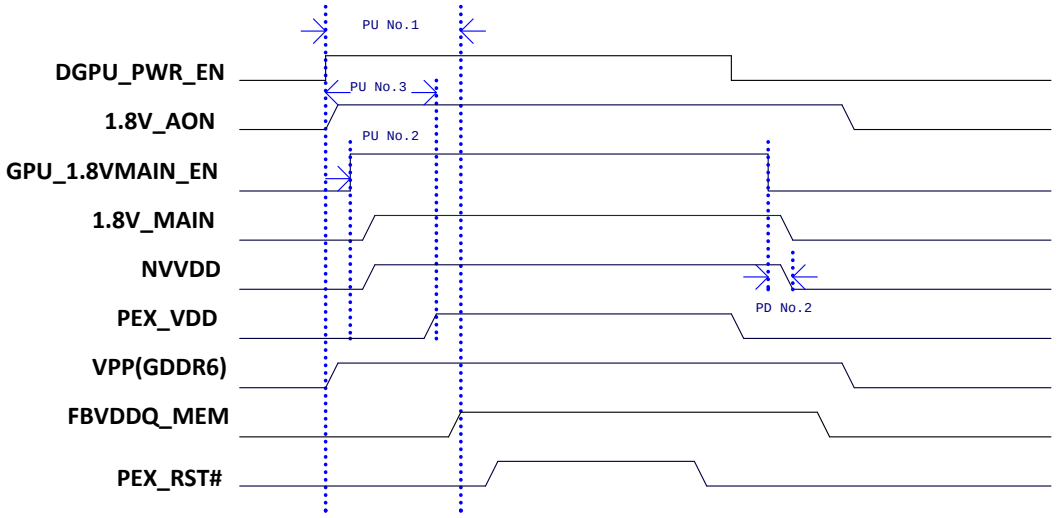
DGPU POWER SEQUENCE



POWER UP sequence is required:1.8V_AON->1.8V_MAIN->NVVDD->/PEX_DVDD->FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.Delay From GPU_1.8VMAIN_EN to PEX_DVDD/PG_PEX_VDD) must NOT exceed 4ms.
3.Delay From 1.8V_AON to PEX_DVDD/PG_PEX_VDD) must NOT exceed 20ms.
4.The ramp-up overshoot should not exceed the silicon reliability limit voltage
5.Power up NVVDD must be 90% before PEX_DVDD and NVVDDS can start ramp up.
6.Power up 1.8V_AON must be 90% before NV 3.3V ramp up.
7.All 3.3V devices that connect to the GPU must be powered after 1.8V_AON ; GPU can't have any 3.3V leakage path before 1.8V_AON present.
8.FBVDDQ.USB_VPP and 1.8_AON don't need power cycle for GC6

POWER DOWN sequence is required
1.PEX_DVDD must ramp down before NVVDD.
2.The propagation delay between GPU_1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 1ms during both power down.
3.For GDDR6,VPP must be equal to or higher than FBVDDQ at all time ; use gate logic and discharge circuit as needed.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power dow
5.Power down PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down NV 3.3V must be less than 10% before +1.8V_AON can start ramp down.

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Title: 69_GPU POWER SEQUENCE		
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Version A to B change list

1. Remove C1604 for adapter detect accuracy
2. R313 from 270k-1-04 to 118K-1-04, R309 from 133K-1-04 to 57.6K-1-04 for 1V8_AON issue
3. Modify ESD solution for Thunderbolt
4. remove MEKB_PWM_LED_BDID, add EC(PWM7) FAN_PWM_CTRL_GPU, change EC(PWM2j) FAN_PWM_CTRL_CPU for thermal request
5. Base on Thunderbolt3 design guild
   Add R2024, R2025 100K-1-04 to GND for TBTB_BSUB1/2
   Remove R238, R239, R2022, R2023 and connector to CC pin on typeC connector
   Modify C1913, C1914, C1916, C1918 from .33uF-10-04X-Z to .22U-10-04R-K
   Add RTD3 function as below
   Add R2045 0ohm for PEWRKAKE#(TBT) to PCH_PEWAKE#(PCH)
   Add Q107 for AND gate PLT_RST#&TBT_PCIe_RST#(PCH) to DG_RERST#(TBT)
   Remove R1979 for excess component
   PW_VCC5v0_SYS for 3A current
   PW_VCC5v0_SYS net name change to +5VA
   Remove B30,R2018
   PW_VCC_TBTA_VBUS net name change to +5V_TYPEC
6. Add F2 fuse for safety request
7. Modify Jteg function
   Modify R257 from 100-1-04 to 51-04
   Modify R257 from 100-04 to 51-04
   Connect PREQ# from PCH to CPU
   Connect PRDY# from CPU to PCH
   Connect TRST# from CPU to PCH
   Add TP for H_CFG3
8. Base Intel PRD1.1
   Add Amber LED1 for PLT_RST#, Red LED2 for CATERR#
9. Modify OVR-M circuit for New version UPI IC
10. EDP CONN modify
    CNEDP1 from CON_WB_40V100_87216_400406_ACS change to FFC,40P,P0.5H1.75,5151704001001,ACES
11. Add BIOS Security Header
    Add CNPWR2, R759, R783
12. PCH bracket for strain gauge
    Add PCHBKT1
13. Charge IC support 7A charging
    L39 BEDR333AM0-7TS1 -> WSRPG0603-2R2M-H
    Add C1740, C1745, C1739, C1746 1U-25-06R-K
14. DP Hot plug modify
    Q33,Q35 LMBT3904LT1G -> 2N7002K-H
15. +5V_TYPEC MLCC voltage rating change for 20V design
    C524,C484 4.7u-10-04R-M -> 1U-25-04X-K
16. Add D401 for HDMI monitor leadage
17. Modify transformer for EMI solution
18. Modify power for noise
19. Modify USB bus for BIOS request
20. Add PD 100K for SLP_S3#
21. Modify R for layout guide
22. Add adapter monitor circuit for PRD1.1
    update : remove from BOM
23. Modify R558, R562 for power consumption

Version B to 1.0 change list

1. Add R896 for OVR-M enable
2. Modify C223, C239 of voltage range
3. Add R1980 for TBT reset issue, and base on CRB that modify I2C bus
4. Add R2046 for EC wp# protect
5. Add C2011 for iMVP 8 test
6. Remove C1636/C1608/C1640/C1609, and add C17/40/C1745/C1739/C1746 for charger cuttent
7. Modify R700 for charge currcent of 5A
8. Add TP99 for TE request
9. Modify choke of speaker for Audio gain
10. Add test point for SMT
11. Modify Power of HDMI_5V for leakage currnet of monitor

Version 1.0 to 1.1 change list

1. Modify TBT3 circuit