MS-7C52 Ver:1.0

CPU:
AMD AM4

System Chipset:
Promontory A320
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

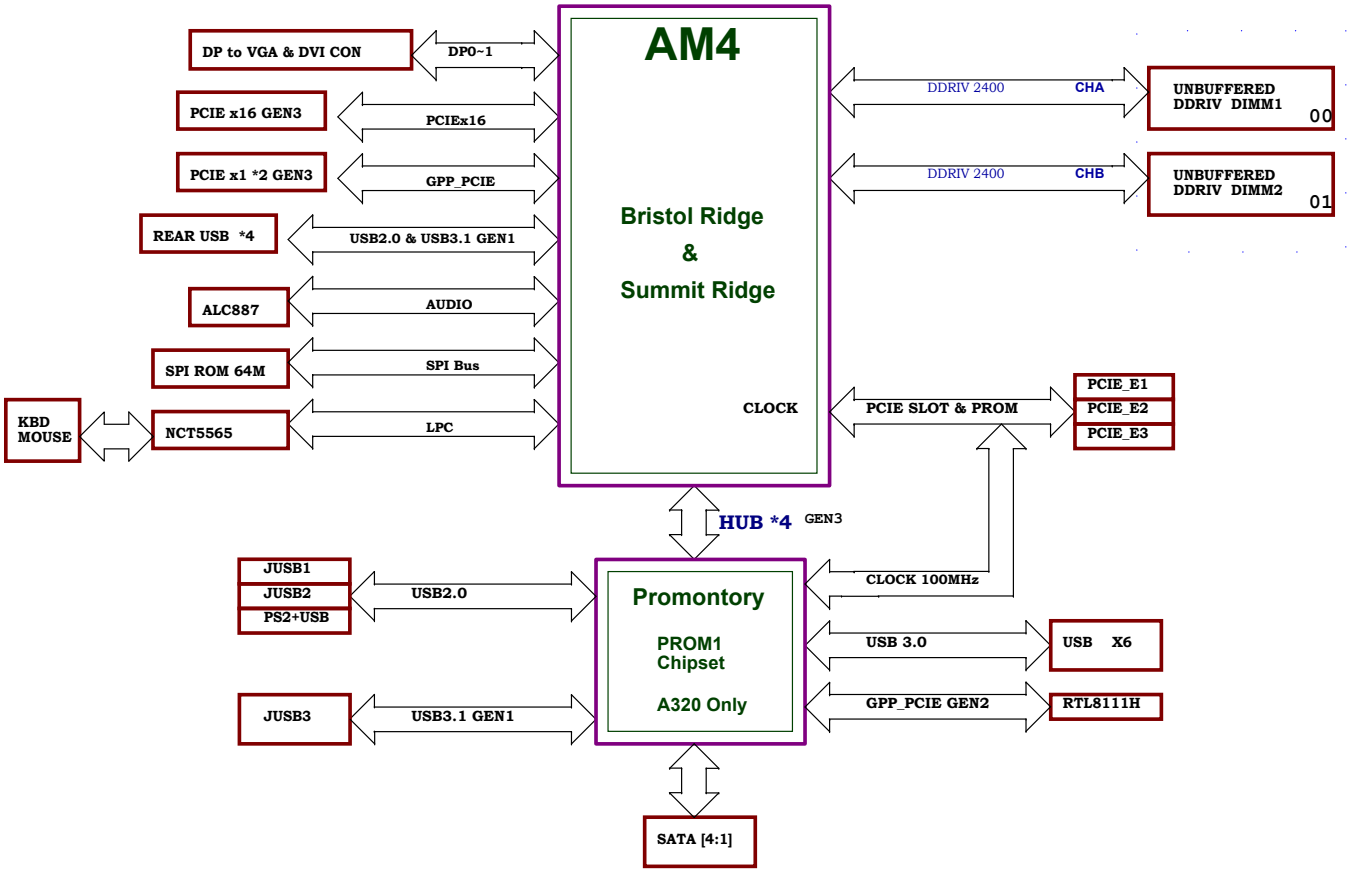
VRM
uP9505 3+2

On Board Chipset:
LPC Super I/O --NCT5565
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

OCP IC:
UP6273

FUSION BLOCK DIAGRAM



MICRO-STAR INT'L CO.,LTD.
Title: Block Diagram
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AMD AM4

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23 / 24 Audio ALC887	
25 USB Rear PS2+USB2.0	
26 USB Rear LAN+USB3.1 GEN1	
27 USB Front Side	
28 SATA Connector	
29 DVI Connector	
30 DP to VGA ITE6516	
31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTT-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	

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Title: COVER SHEET

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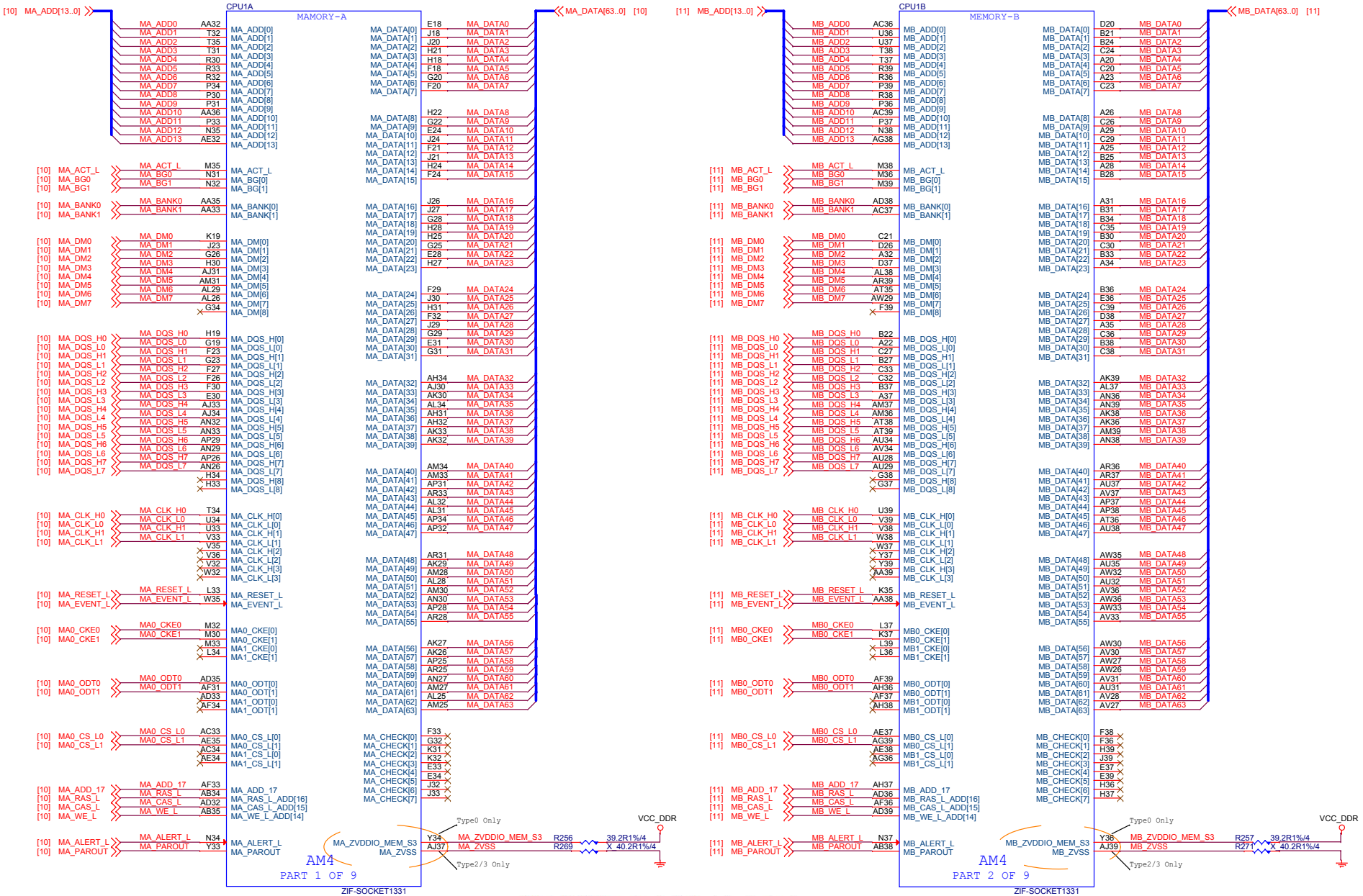

Table 6. DRAM Memory Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
MA_ZVDDIO_MEM_S3, MB_ZVDDIO_MEM_S3	A	Compensation Resistor to VDDIO_MEM_S	X				
MA_ZVSS, MB_ZVSS	A	DRAM Compensation Resistor to VSS		X	X	X	X

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Title: AM4 DDR4 I/F

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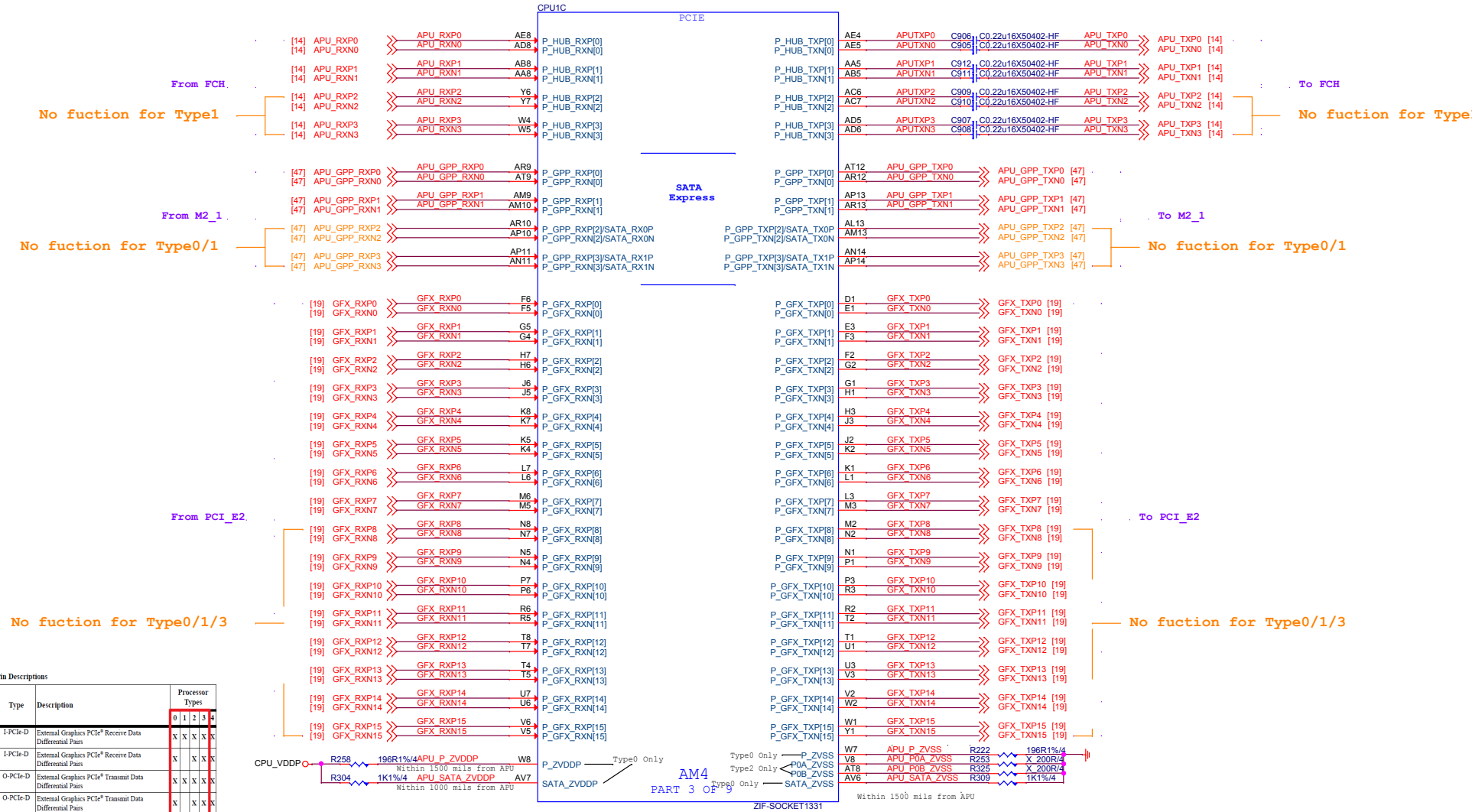

Table 3. PCI Express® Interface Pin Descriptions

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
P_GFX_RXP[3:0], P_GFX_RXN[3:0]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_GFX_RXP[7:4], P_GFX_RXN[7:4]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs	X		X	X	X
P_GFX_TXP[3:0], P_GFX_TXN[3:0]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_GFX_TXP[7:4], P_GFX_TXN[7:4]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs	X		X	X	X
P_GFX_RXP[15:8], P_GFX_RXN[15:8]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs			X		X
P_GFX_TXP[15:8], P_GFX_RXN[15:8]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs			X		X
P_GPP_RXP[1:0], P_GPP_RXN[1:0]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_GPP_TXP[1:0], P_GPP_TXN[1:0]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_GPP_RXP[2]/SATA_RX0P, P_GPP_RXN[2]/SATA_RX0N	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs			X	X	X
P_GPP_TXP[2]/SATA_TX0P, P_GPP_TXN[2]/SATA_TX0N	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs			X	X	X
P_GPP_RXP[3]/SATA_RX1P, P_GPP_RXN[3]/SATA_RX1N	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs			X	X	X
P_GPP_TXP[3]/SATA_TX1P, P_GPP_TXN[3]/SATA_TX1N	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs			X	X	X
P_HUB_RXP[1:0], P_HUB_RXN[1:0]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_HUB_RXP[3:2], P_HUB_RXN[3:2]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X		X	X	X
P_HUB_TXP[1:0], P_HUB_TXN[1:0]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_HUB_TXP[3:2], P_HUB_TXN[3:2]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X		X	X	X
PCIE_RST_L/EGPIO26	O-IO33S5-S	PCI Host Bus Reset. Asserted during transition to S3/S5.	X	X	X	X	X

Table 3. PCI Express® Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
P0A_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive			X		X
P0B_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive			X		X
P_ZVDDP	A	Compensation Resistor to VDDP	X				
P_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive	X				

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Title: AM4 PCIE/SATAE

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Table 4. Digital Display Interface (DDI) Pin Descriptions

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
DP0_TXP[3:0], DP0_TXN[3:0] DP1_TXP[3:0], DP1_TXN[3:0] DP2_TXP[1:0], DP2_TXN[1:0]	O-PCIe-D	DisplayPort Differential Transmitter	X	X		X	
DP2_TXP[3:2], DP2_TXN[3:2]	O-PCIe-D	DisplayPort Differential Transmitter	X			X	
DP0_AUXP, DP0_AUXN DP1_AUXP, DP1_AUXN DP2_AUXP, DP2_AUXN[1]	B-IO18-D	DisplayPort Auxiliary Channel	X	X		X	
DP0_HPD, DP1_HPD, DP2_HPD[2]	I-IO18-S	DisplayPort Hot Plug Detect	X	X		X	
DP_AUX_ZVSS	A	Compensation Resistor to VSS	X				
DP_ZVSS	A	Compensation Resistor to VSS	X				

Notes:

1. *DisplayPort Auxiliary Channel pins are dual-mode pins and are 3.3V tolerant. In I2C mode AUXP pins change to SCL, and AUXN pins change to SDA. During this operation the pin type is B-IO33-OD.*
2. *Hot Plug Detect pins are 3.3V tolerant.*

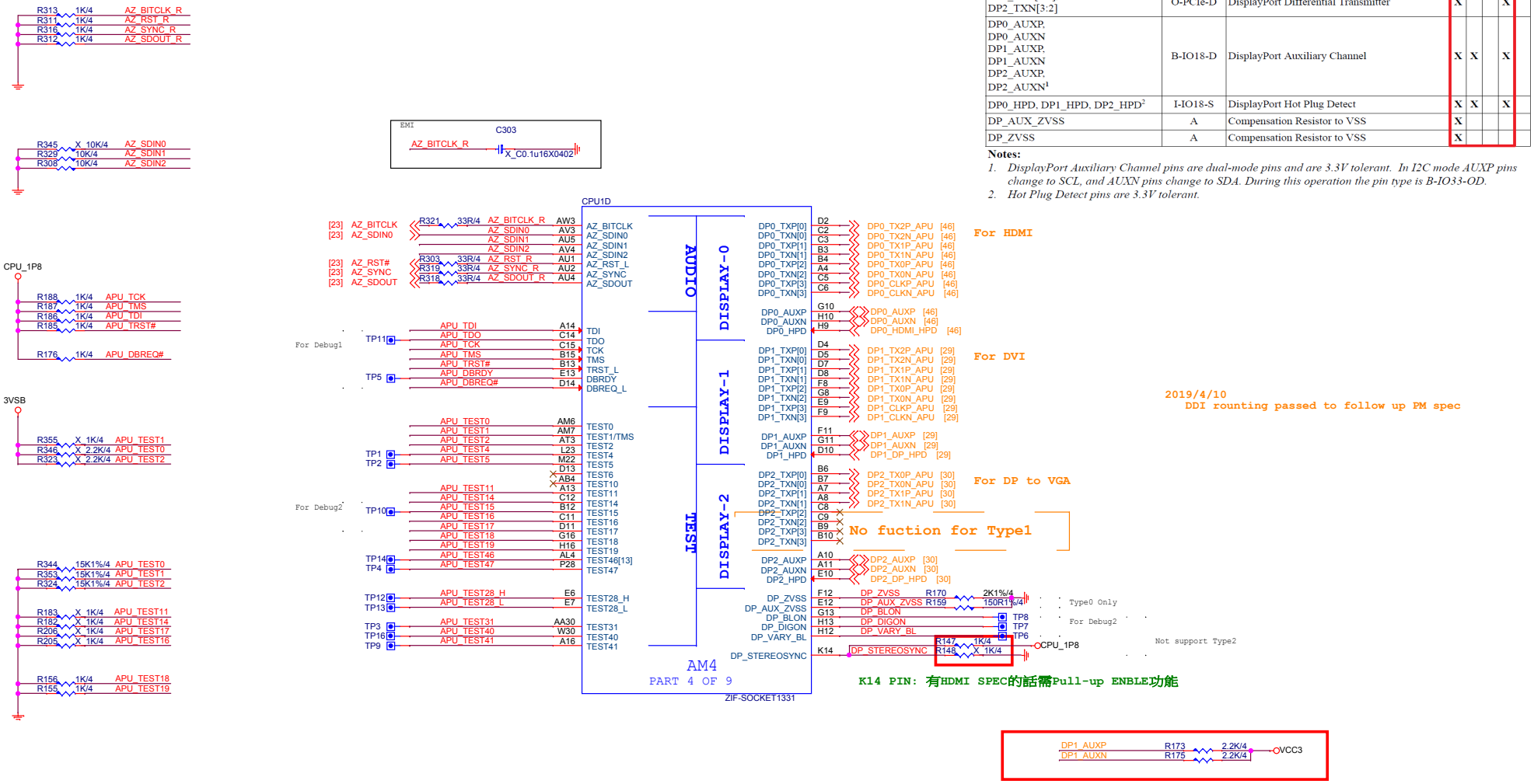

Table 5. LCD Power Interface Pin Descriptions

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
DP_BLON	O-IO18-S	Display Panel Backlight Enable	X	X		X	
DP_DIGON	O-IO18-S	Display Panel Power Enable	X	X		X	
DP_STEREOSYNC	B-IO18-S	Signal used to drive active shutter glasses for stereoscopic 3D viewing on 120-Hz panels.	X	X		X	
DP_VARY_BL	O-IO18S	Display Backlight Brightness Control	X	X		X	

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Title: AM4 DISPLAY/AUDIO

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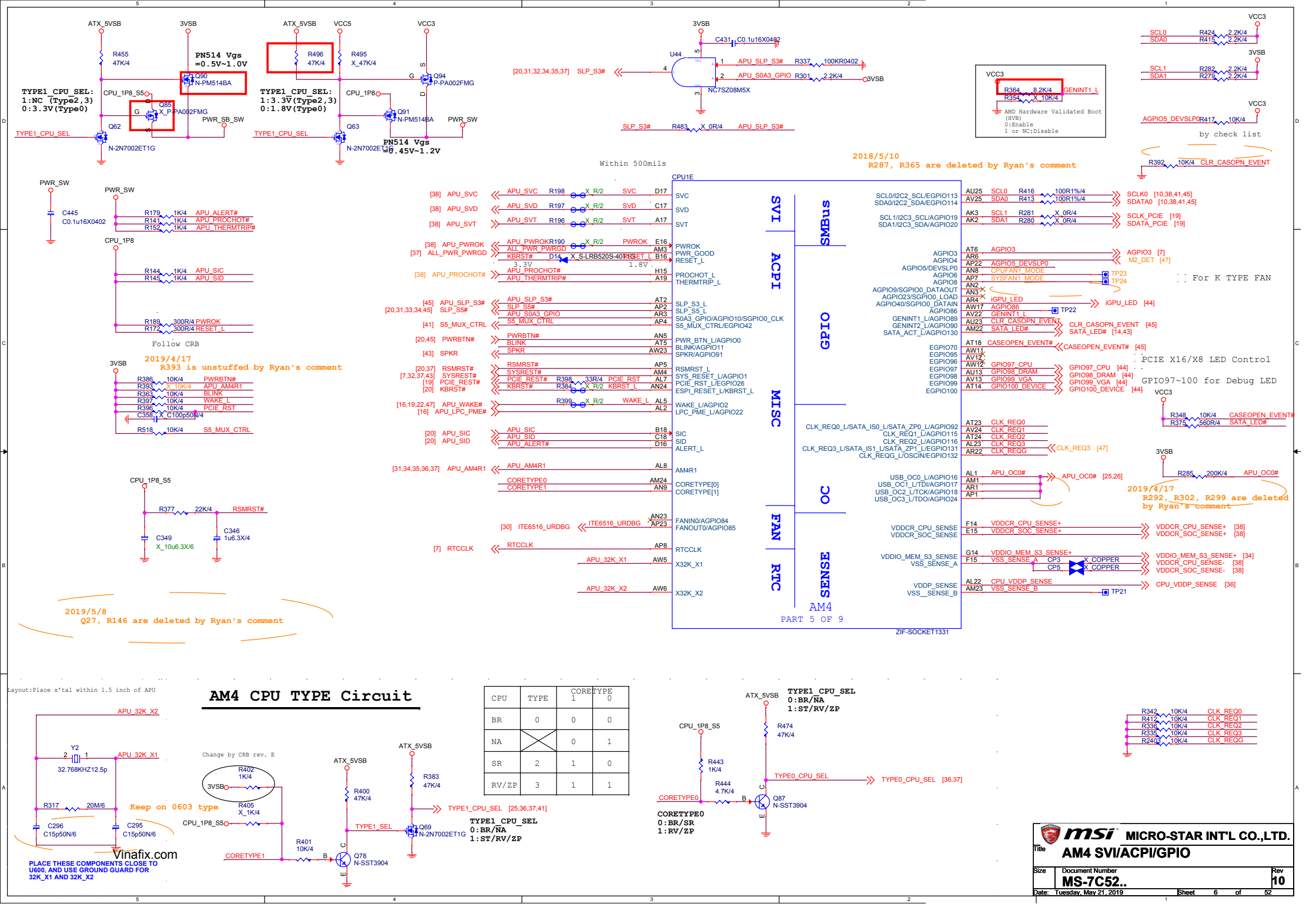
ATX_5VSB
3VSB
R455 47K/4
PN514 Vgs =0.5V~1.0V
Q90 N-PM514BA
TYPE1_CPU_SEL: 1:NC (Type2,3) 0:3.3V(Type0)
CPU_1P8_S5
Q85 X_P-PA002FMG
Q62
N-2N7002ET1G
PWR_SB_SW
TYPE1_CPU_SEL
ATX_5VSB
VCC5
VCC3
R496 47K/4
R495 X_47K/4
Q94 P-PA002FMG
TYPE1_CPU_SEL: 1:3.3V(Type2,3) 0:1.8V(Type0)
CPU_1P8
Q91 N-PM514BA
PWR_SW
Q63
N-2N7002ET1G
PN514 Vgs =0.45V~1.2V
3VSB
C431 C0.1u16X0402
U44
APU_SLP_S3#
R337 100KR0402
APU_S0A3_GPIO
R301 2.2K/4
3VSB
NC7SZ08M5X
[20,31,32,34,35,37] SLP_S3#
SLP_S3#
R483 X_0R/4
APU_SLP_S3#
VCC3
R364 8.2K/4
GENINT1_L
R354 X_10K/4
AMD Hardware Validated Boot (HVB)
0:Enable
1 or NC:Disable
SCL0 R424 2.2K/4
SDA0 R415 2.2K/4
SCL1 R282 2.2K/4
SDA1 R279 2.2K/4
AGPIO5_DEVSLP0 R417 10K/4
by check list
R392 10K/4 CLR_CASOPN_EVENT
PWR_SW
C445 C0.1u16X0402
R179 1K/4 APU_ALERT#
R141 1K/4 APU_PROCHOT#
R152 1K/4 APU_THERMTRIP#
CPU_1P8
R144 1K/4 APU_SIC
R145 1K/4 APU_SID
R189 300R/4 PWROK
R172 300R/4 RESET_L
Follow CRB
2019/4/17
R393 is unstuffed by Ryan's comment
3VSB
R386 10K/4 PWRBTN#
R393 X_10K/4 APU_AM4R1
R363 10K/4 BLINK
R397 10K/4 WAKE_L
R396 10K/4 PCIE_RST
C358 X_C100p50N/4
R518 10K/4 S5_MUX_CTRL
CPU_1P8_S5
R377 22K/4 RSMRST#
C349 X_10u6.3X/6
C346 1u6.3X/4
2019/5/8
Q27, R146 are deleted by Ryan's comment
Within 500mils
2018/5/10
R287, R365 are deleted by Ryan's comment
CPU1E
SVI
ACPI
GPIO
MISC
OC
FAN
RTC
SMBus
SENSE
[38] APU_SVC
APU_SVC R198 X_R/2 SVC D17
SVC
[38] APU_SVD
APU_SVD R197 X_R/2 SVD C17
SVD
[38] APU_SVT
APU_SVT R196 X_R/2 SVT A17
SVT
[38] APU_PWROK
APU_PWROK R190 X_R/2 PWROK E16
PWROK
[37] ALL_PWR_PWRGD
ALL_PWR_PWRGD AM3
PWR_GOOD
KBRST# D14 X_S-LRB520S-40T1G RESET_L B16
RESET_L
3.3V
1.8V
[38] APU_PROCHOT#
APU_PROCHOT# H15
PROCHOT_L
APU_THERMTRIP# A19
THERMTRIP_L
[45] APU_SLP_S3#
APU_SLP_S3# AT2
SLP_S3_L
[20,31,33,34,45] SLP_S5#
SLP_S5# AP2
SLP_S5_L
APU_S0A3_GPIO AR3
S0A3_GPIO/AGPIO10/SGPIO0_CLK
[41] S5_MUX_CTRL
S5_MUX_CTRL AP4
S5_MUX_CTRL/EGPIO42
[20,45] PWRBTN#
PWRBTN# AN5
PWR_BTN_L/AGPIO0
[43] SPKR
BLINK AT5
BLINK/AGPIO11
SPKR AW23
SPKR/AGPIO91
[20,37] RSMRST#
RSMRST# AP5
RSMRST_L
[7,32,37,43] SYSRESET#
SYSRESET# AM4
SYS_RESET_L/AGPIO1
[19] PCIE_REST#
PCIE_REST# R398 33R/4 PCIE_RST AL7
PCIE_RST_L/EGPIO26
[20] KBRST#
KBRST# R384 X_R/2 KBRST_L AN24
ESPI_RESET_L/KBRST_L
[16,19,22,47] APU_WAKE#
R399 X_R/2 WAKE_L AL5
WAKE_L/AGPIO2
[16] APU_LPC_PME#
AL2
LPC_PME_L/AGPIO22
[20] APU_SIC
APU_SIC B18
SIC
[20] APU_SID
APU_SID C18
SID
APU_ALERT# D16
ALERT_L
[31,34,35,36,37] APU_AM4R1
APU_AM4R1 AL8
AM4R1
CORETYPE0 AM24
CORETYPE[0]
CORETYPE1 AN9
CORETYPE[1]
[30] ITE6516_URDBG
ITE6516_URDBG AN23
FANIN0/AGPIO84
AP23
FANOUT0/AGPIO85
[7] RTCCLK
RTCCLK AP8
RTCCLK
APU_32K_X1 AW5
X32K_X1
APU_32K_X2 AW6
X32K_X2
AM4
PART 5 OF 9
ZIF-SOCKET1331
SCL0/I2C2_SCL/EGPIO113
SDA0/I2C2_SDA/EGPIO114
AU25 SCL0 R416 100R1%/4
AV25 SDA0 R413 100R1%/4
SCLK0 [10,38,41,45]
SDATA0 [10,38,41,45]
SCL1/I2C3_SCL/AGPIO19
SDA1/I2C3_SDA/AGPIO20
AK3 SCL1 R281 X_0R/4
AK2 SDA1 R280 X_0R/4
SCLK_PCIE [19]
SDATA_PCIE [19]
AGPIO3
AGPIO4
AGPIO5/DEVSLP0
AGPIO6
AGPIO8
AGPIO9/SGPIO0_DATAOUT
AGPIO23/SGPIO0_LOAD
AGPIO40/SGPIO0_DATAIN
AGPIO86
GENINT1_L/AGPIO89
GENINT2_L/AGPIO90
SATA_ACT_L/AGPIO130
AT6 AGPIO3
AR6
AP22 AGPIO5_DEVSLP0
AN8 CPUFAN1_MODE
AP7 SYSFAN1_MODE
AN2
AN3
AR4 iGPU_LED
AW17 AGPIO86
AV22 GENINT1_L
AU23 CLR_CASOPN_EVENT
AM22 SATA_LED#
AGPIO3 [7]
M2_DET [47]
TP23
TP24
For K TYPE FAN
iGPU_LED [44]
TP22
CLR_CASOPN_EVENT [45]
SATA_LED# [14,43]
EGPIO70
EGPIO95
EGPIO96
EGPIO97
EGPIO98
EGPIO99
EGPIO100
AT18 CASEOPEN_EVENT#
AW11
AV12
AW12 GPIO97_CPU
AU13 GPIO98_DRAM
AV13 GPIO99_VGA
AT14 GPIO100_DEVICE
CASEOPEN_EVENT# [45]
GPIO97_CPU [44]
GPIO98_DRAM [44]
GPIO99_VGA [44]
GPIO100_DEVICE [44]
PCIE X16/X8 LED Control
GPIO97~100 for Debug LED
VCC3
R348 10K/4 CASEOPEN_EVENT#
R375 560R/4 SATA_LED#
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
CLK_REQG_L/OSCIN/EGPIO132
AT23 CLK_REQ0
AV24 CLK_REQ1
AT24 CLK_REQ2
AL23 CLK_REQ3
AR22 CLK_REQG
CLK_REQ3 [47]
USB_OC0_L/AGPIO16
USB_OC1_L/TDI/AGPIO17
USB_OC2_L/TCK/AGPIO18
USB_OC3_L/TDO/AGPIO24
AL1 APU_OC0#
AM1
AR1
AP1
APU_OC0# [25,26]
3VSB
R285 200K/4 APU_OC0#
2019/4/17
R292, R302, R299 are deleted by Ryan's comment
VDDCR_CPU_SENSE
VDDCR_SOC_SENSE
F14 VDDCR_CPU_SENSE+
E15 VDDCR_SOC_SENSE+
VDDCR_CPU_SENSE+ [38]
VDDCR_SOC_SENSE+ [38]
VDDIO_MEM_S3_SENSE
VSS_SENSE_A
G14 VDDIO_MEM_S3_SENSE+
F15 VSS_SENSE_A
CP3
CP5
X_COPPER
X_COPPER
VDDIO_MEM_S3_SENSE+ [34]
VDDCR_CPU_SENSE- [38]
VDDCR_SOC_SENSE- [38]
VDDP_SENSE
VSS_SENSE_B
AL22 CPU_VDDP_SENSE
AM23 VSS_SENSE_B
TP21
CPU_VDDP_SENSE [36]
Layout:Place x'tal within 1.5 inch of APU
AM4 CPU TYPE Circuit
APU_32K_X2
Y2
32.768KHZ12.5p
APU_32K_X1
R317 20M/6
C296 C15p50N/6
C295 C15p50N/6
Keep on 0603 type
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
Vinafix.com
Change by CRB rev. E
3VSB
R402 1K/4
R405 X_1K/4
CPU_1P8_S5
CORETYPE1
R401 10K/4
Q78 N-SST3904
ATX_5VSB
R400 47K/4
TYPE1_SEL
R383 47K/4
Q69 N-2N7002ET1G
TYPE1_CPU_SEL [25,36,37,41]
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
CPU TYPE CORETYPE 1 0
BR 0 0 0
NA X 0 1
SR 2 1 0
RV/ZP 3 1 1
ATX_5VSB
CPU_1P8_S5
R474 47K/4
R443 1K/4
R444 4.7K/4
CORETYPE0
Q87 N-SST3904
TYPE0_CPU_SEL
TYPE0_CPU_SEL [36,37]
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
CORETYPE0
0:BR/SR
1:RV/ZP
R342 10K/4 CLK_REQ0
R412 10K/4 CLK_REQ1
R336 10K/4 CLK_REQ2
R335 10K/4 CLK_REQ3
R240 10K/4 CLK_REQG
MSI MICRO-STAR INT'L CO.,LTD.
Title
AM4 SVI/ACPI/GPIO
Size
Document Number
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10
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Strapping Options

2019/5/14
R349 & R343 passed to follow up PM's spec

	R349	R343
01S	X	●
02S	●	X
03S	●	X

	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ?????	LPC ROM

	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

2019/5/2
R2387 is added by Ryan's comment

CPU1F
LPC/SPI/USB/CLOCK
AM4
PART 6 OF 9
ZIF-SOCKET1331

Vinafix.com

Table 7. Clock Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types 0	1	2	3	4
GFX_CLKP, GFX_CLKN	O-IOGFX-D	PCIe® Graphic Slot Clock	X	X	X	X	X
GPP_CLK0P, GPP_CLK0N	B-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X			X
	B-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
GPP_CLK1P, GPP_CLK1N	B-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X			X
	B-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
GPP_CLK2P, GPP_CLK2N	O-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X			X
	O-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
GPP_CLK3P, GPP_CLK3N	O-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X			X
	O-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
X48M_X1	I-IOVP55-S	48-MHz Crystal Clock 1 Note: Power rail may be tied to 50-55 or 50-53.	X	X	X	X	X
X48M_X2	I-IOVP55-S	48-MHz Crystal Clock 2 Note: Power rail may be tied to 50-55 or 50-53.	X	X	X	X	X
X32K_X1	I-RTC-S	32-kHz Real Time Clock Crystal Oscillator Input 1 Note: Input must be active at all times.	X	X	X	X	X
X32K_X2	I-RTC-S	32-kHz Real Time Clock Crystal Oscillator Input 2 Note: Input must be active at all times.	X	X	X	X	X
RTCCLK	O-IO33S5-S	Real Time Clock 32-kHz Output	X				
	O-IO18S5-S	Real Time Clock 32-kHz Output		X	X	X	X

Table 8. USB Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types 0	1	2	3	4
48M_OSC	B-IO33S5-S	48-MHz USB Clock	X				
	B-IO18S5-S	48-MHz USB Clock		X	X	X	X
USB_ZVSS,	A	USB Compensating Resistor to VSS	X				
USB[3:0]_ZVSS,	A	USB Compensating Resistor to VSS		X	X	X	
USB_SS_ZVSS	A	USB SS Compensation Resistor to VSS	X				
USB_SS_ZVDDP	A	Compensation Resistor to USB SS Power Supply	X				

SPI ROM(1.8V)

2019/5/8
R492, R525 are changed to 0ohm to short copper by cost reduction.

SPI CS# < 20pF
D0G-0402510-SI0

AVL:M31-2512883-W03

2019/4/11
The footprint of SPI1 is chnaged to SIC8_SST_S2A_COLAY_T by 16M/32M colay by PM spec

P.S Close to JSPI1

Layout:Place x'tal within 1.5 inch of APU

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

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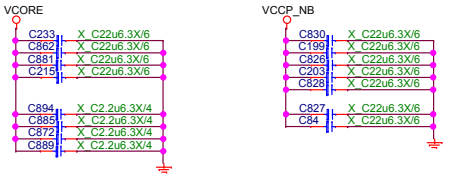
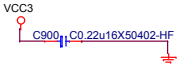
VDDIO_AUDIO Circuit

2019/4/11
R537, C397, C459, U49, R529, C456, C464, R536, R535, C453 are deleted by Ryan's comment

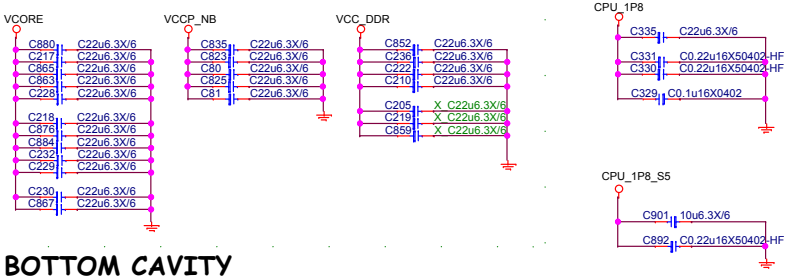
1.5V
0.25A

TOP SIDE

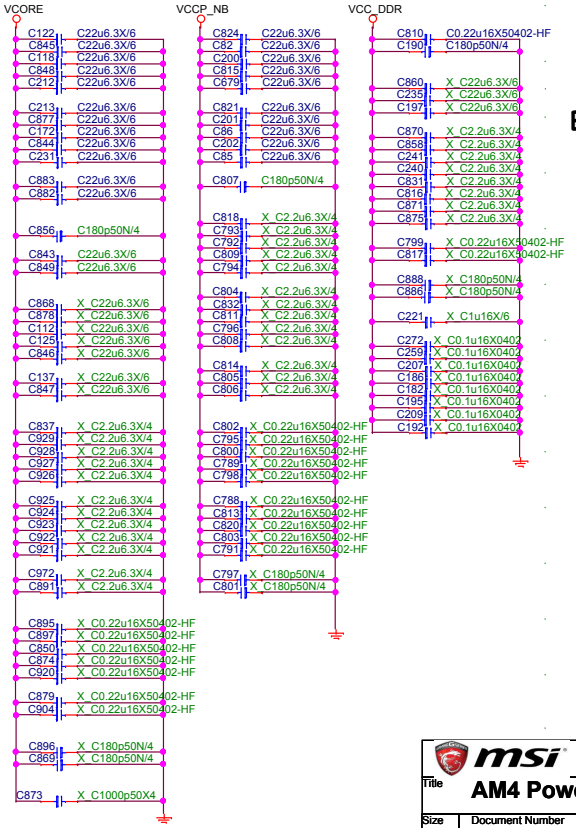




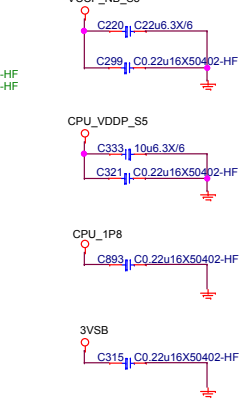
TOP CAVITY

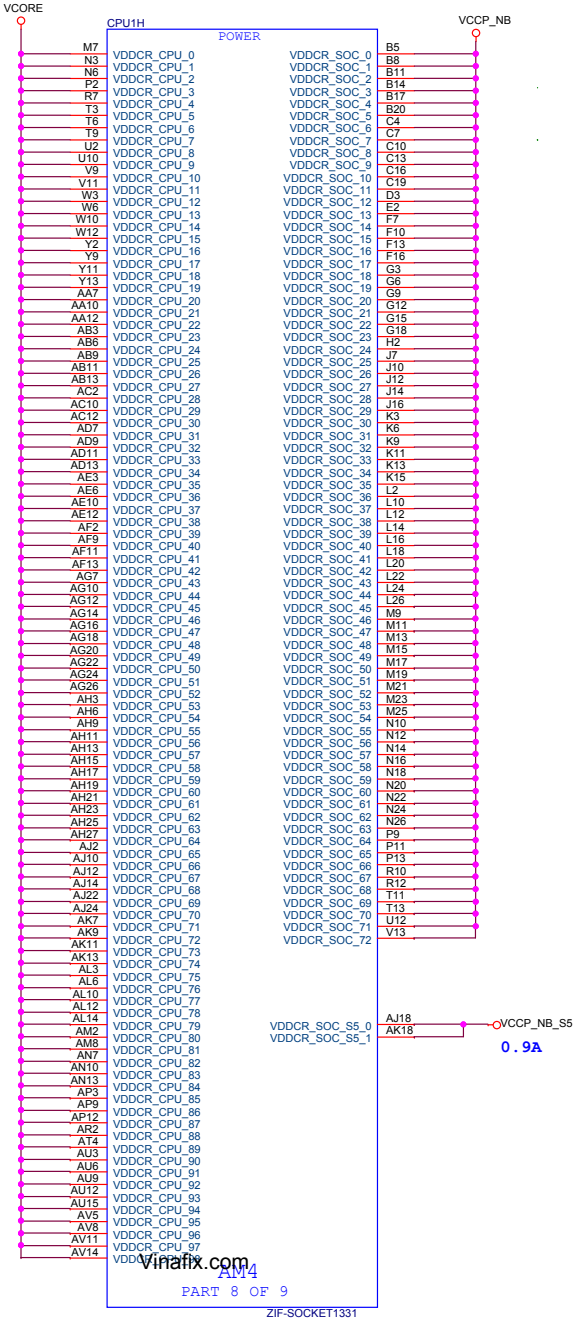


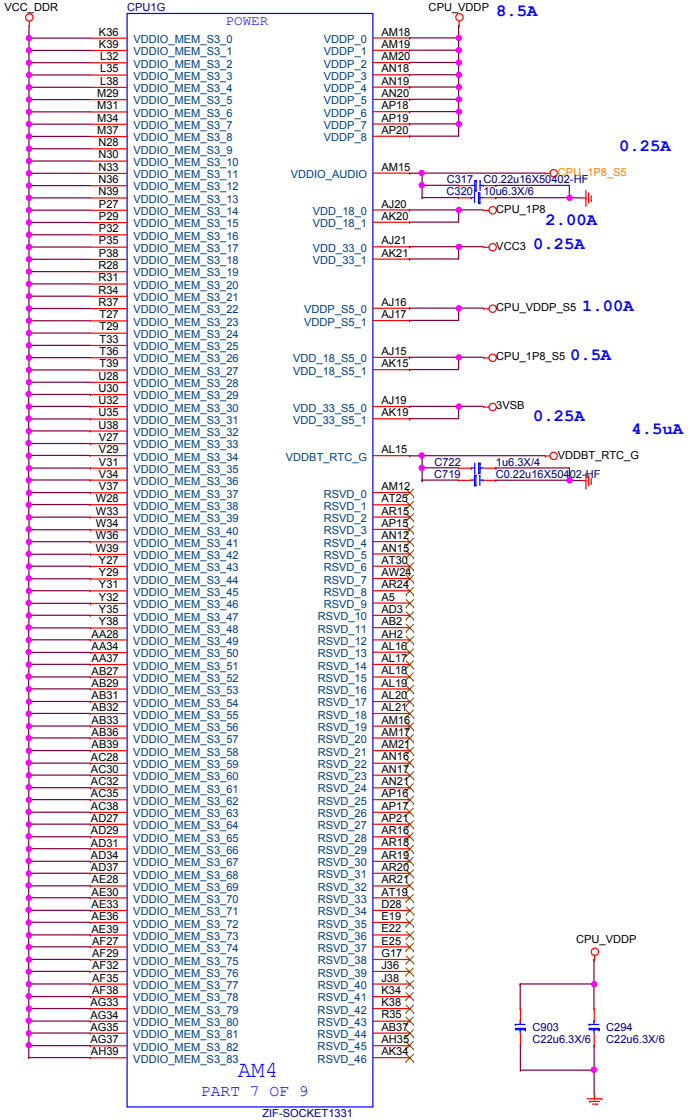
BOTTOM CAVITY



BOTTOM SIDE







MSI MICRO-STAR INT'L CO.,LTD.

Title: AM4 Power/RTC Power

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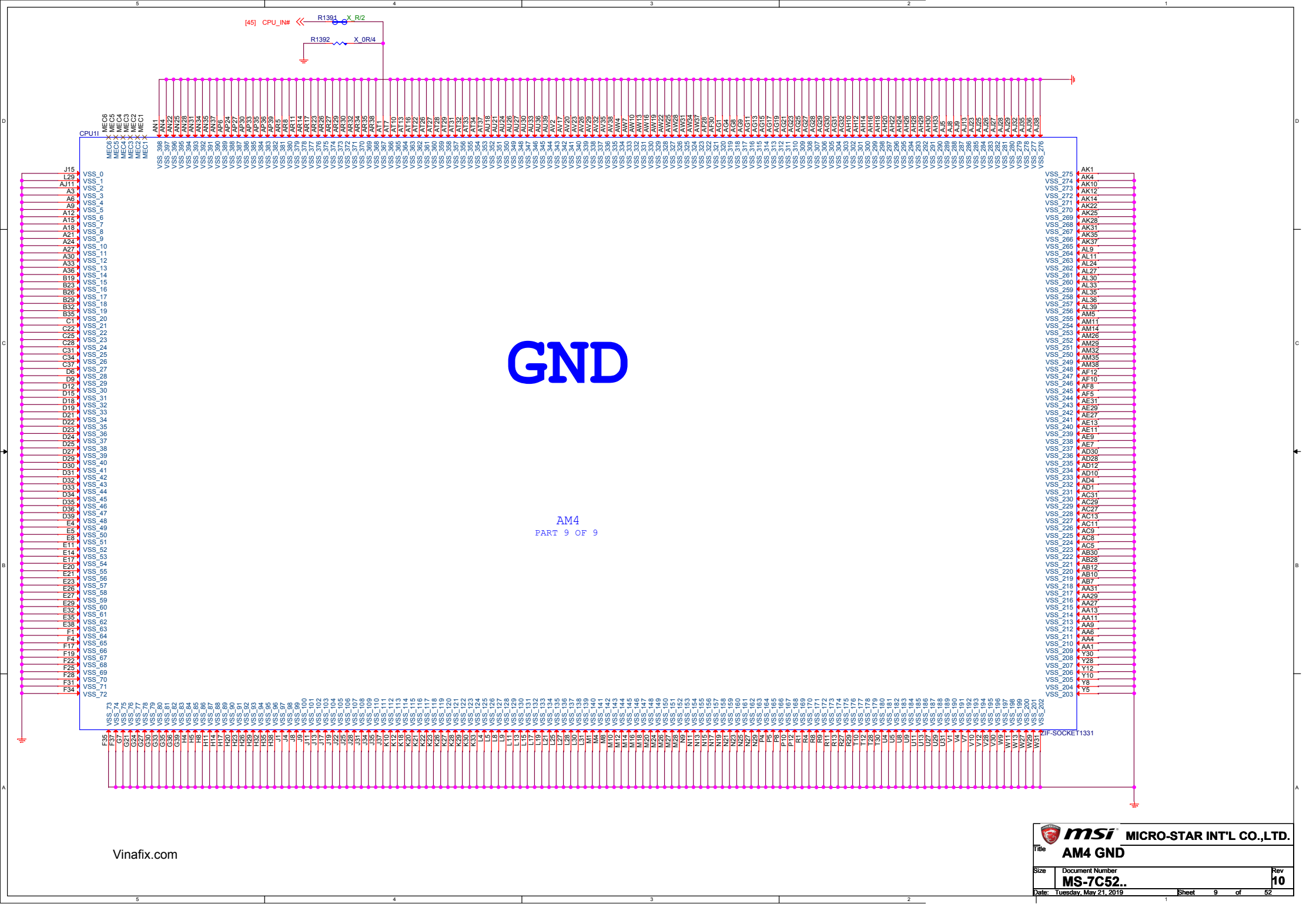
[45] CPU_IN#
R1391 X_R/2
R1392 X_0R/4
CPU1I
J15
VSS_0
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
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VSS_275
AK1
AK4
AK10
AK12
AK14
AK22
AK25
AK28
AK31
AK35
AK37
AL9
AL11
AL24
AL27
AL30
AL33
AL35
AL36
AL39
AM5
AM11
AM14
AM26
AM29
AM32
AM35
AM38
AF12
AF10
AF8
AF5
AE31
AE29
AE27
AE13
AE11
AE9
AE7
AD30
AD28
AD12
AD10
AD4
AD1
AC31
AC29
AC27
AC13
AC11
AC9
AC8
AC5
AB30
AB28
AB12
AB10
AB7
AA31
AA29
AA27
AA13
AA11
AA9
AA6
AA4
AA1
Y30
Y28
Y12
Y10
Y8
Y5
ZIF-SOCKET1331
GND
AM4
PART 9 OF 9
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MICRO-STAR INT'L CO.,LTD.
Title
AM4 GND
Size
Document Number
MS-7C52..
Rev
10
Date: Tuesday, May 21, 2019
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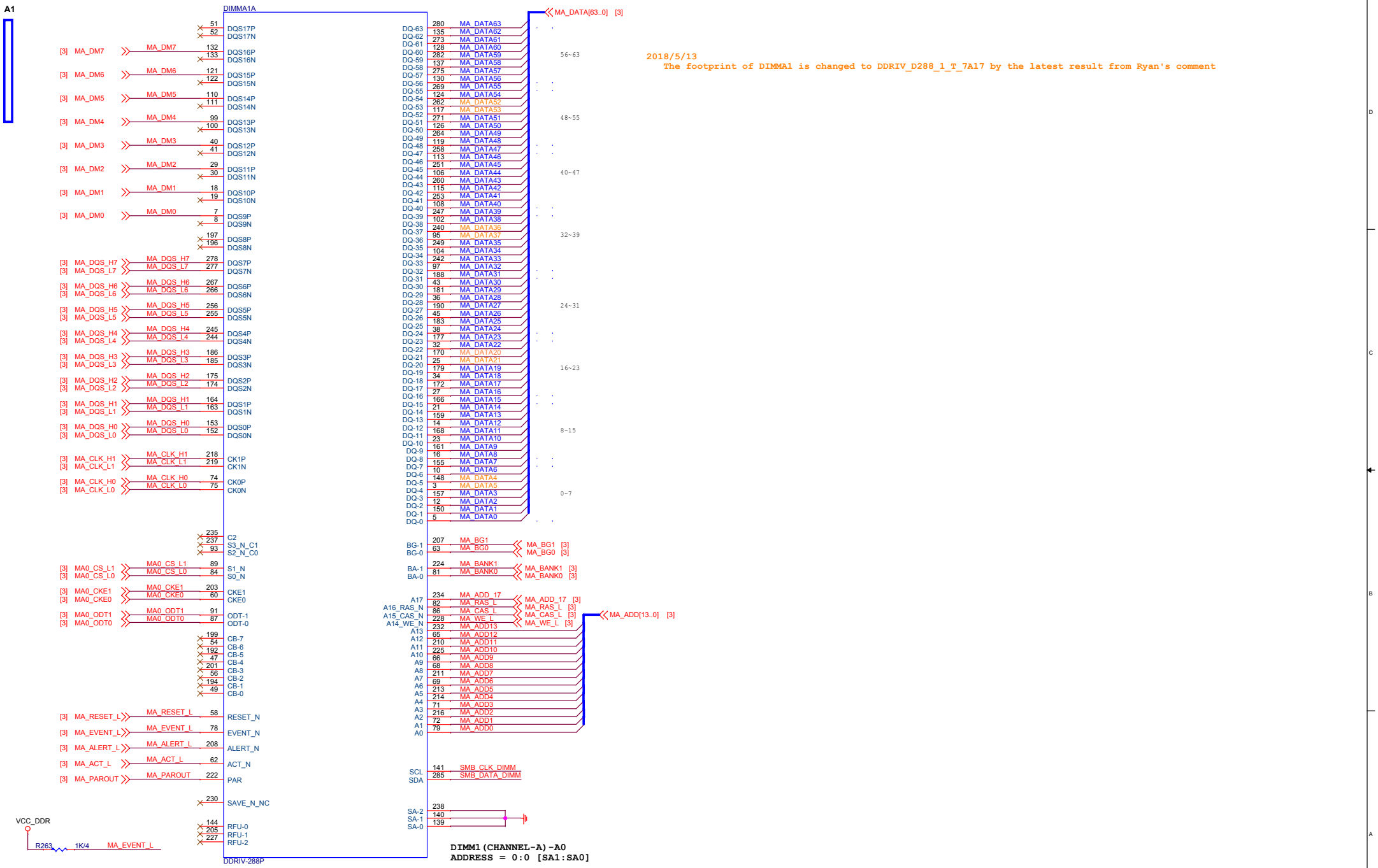
A1
DIMMA1A
DDRIV-288P
MA_DATA[63..0] [3]
MA_ADD[13..0] [3]
2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
VCC_DDR
R263 1K/4 MA_EVENT_L
Vinafix.com
MICRO-STAR INT'L CO.,LTD.
Title
DDR4 DIMM CH-A
Size
Document Number
MS-7C52..
Rev
10
Date: Tuesday, May 21, 2019
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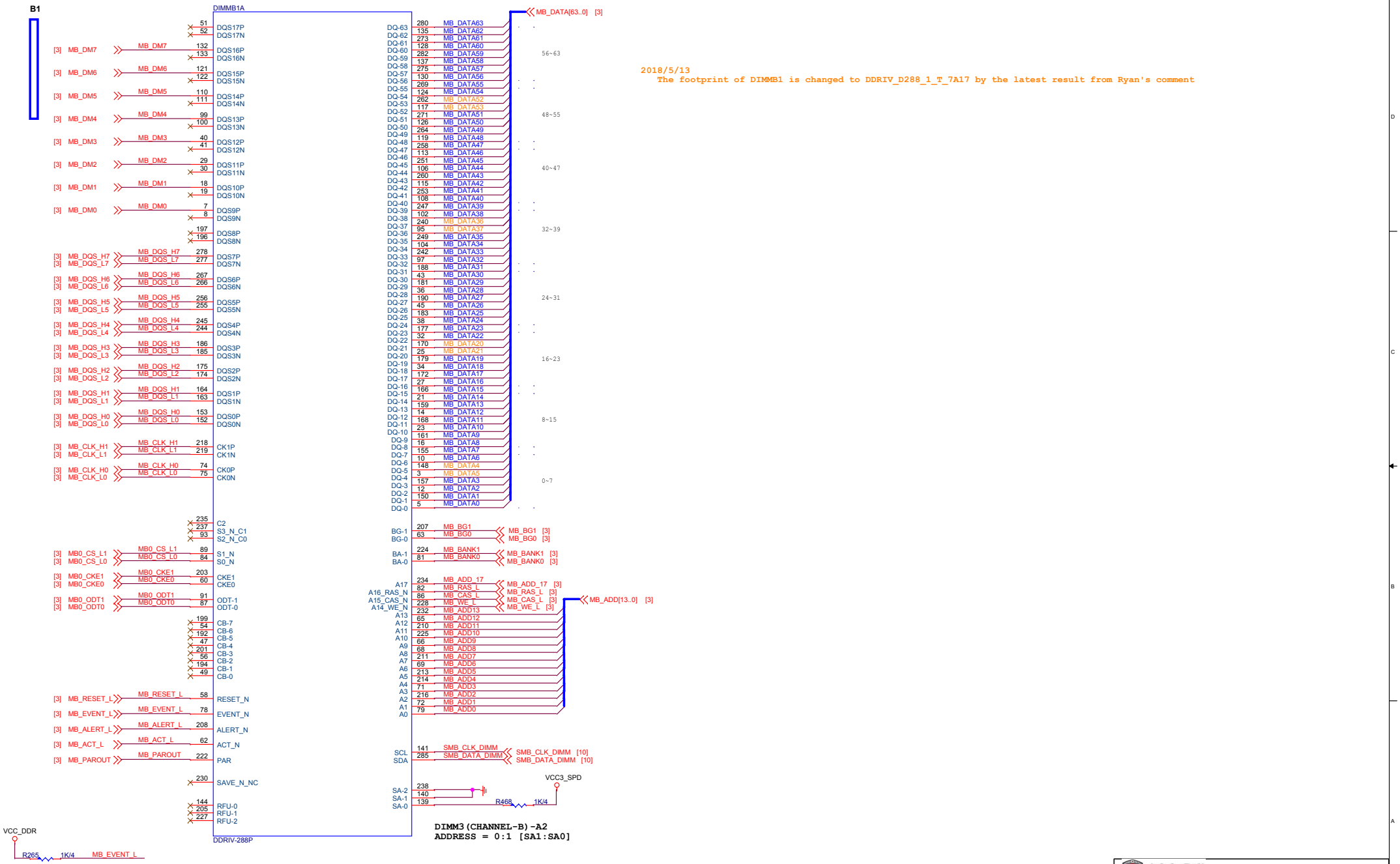

MICRO-STAR INT'L CO.,LTD.	
Title	DDR4 DIMM CH-B
Size	Document Number: MS-7C52.. Rev: 10
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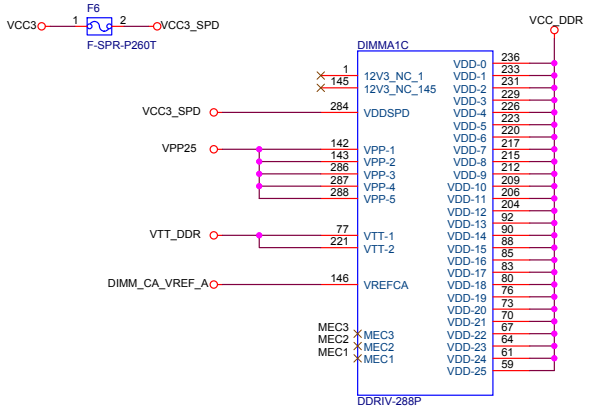
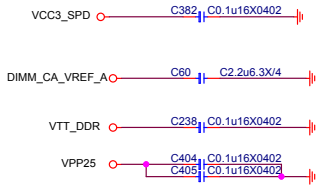
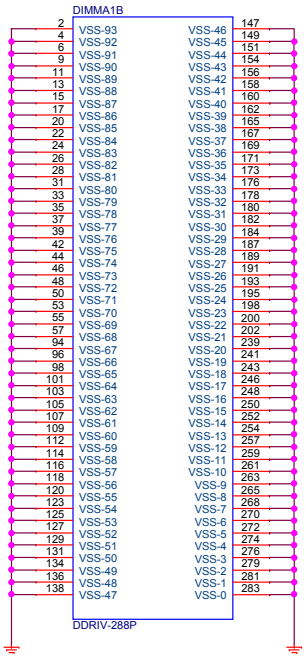


2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment



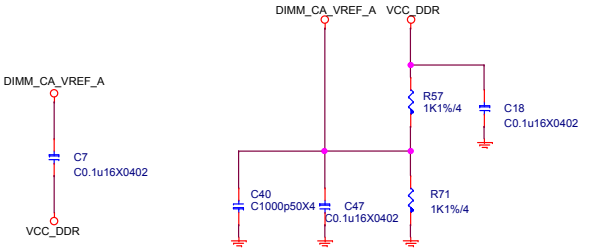


Vinafix.com

2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

DDR VREF

(place resistors close to DIMMs)



MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-1

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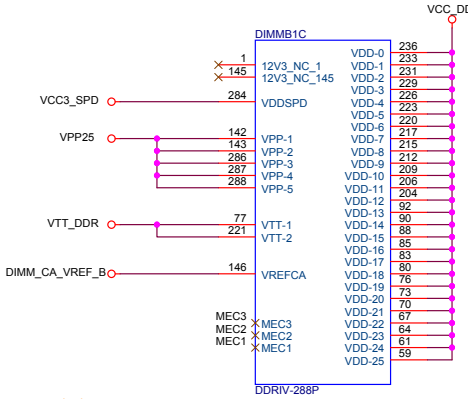
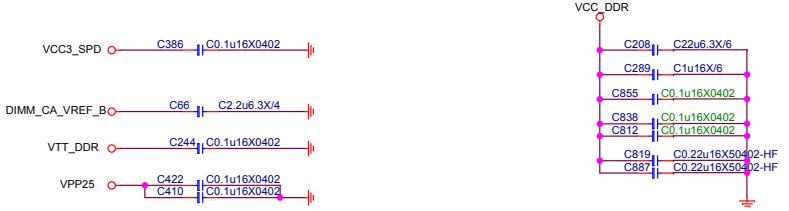
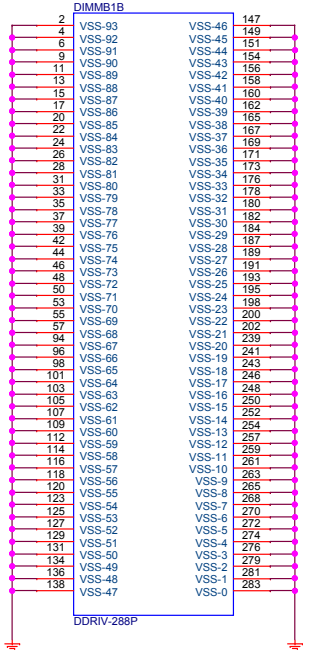


2018/5/13
The footprint of DIMMB1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment



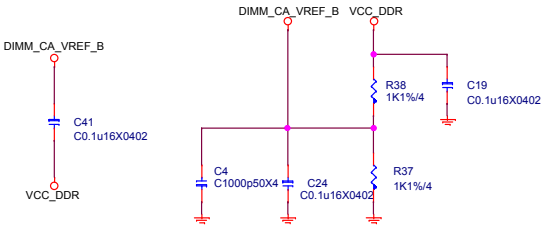


Vinafix.com

2018/5/13
The footprint of DIMMB1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

DDR VREF

(place resistors close to DIMMs)



MICRO-STAR INT'L CO.,LTD.

Title	DDR4-POWER/GND-2	
Size	Document Number MS-7C52..	Rev 10
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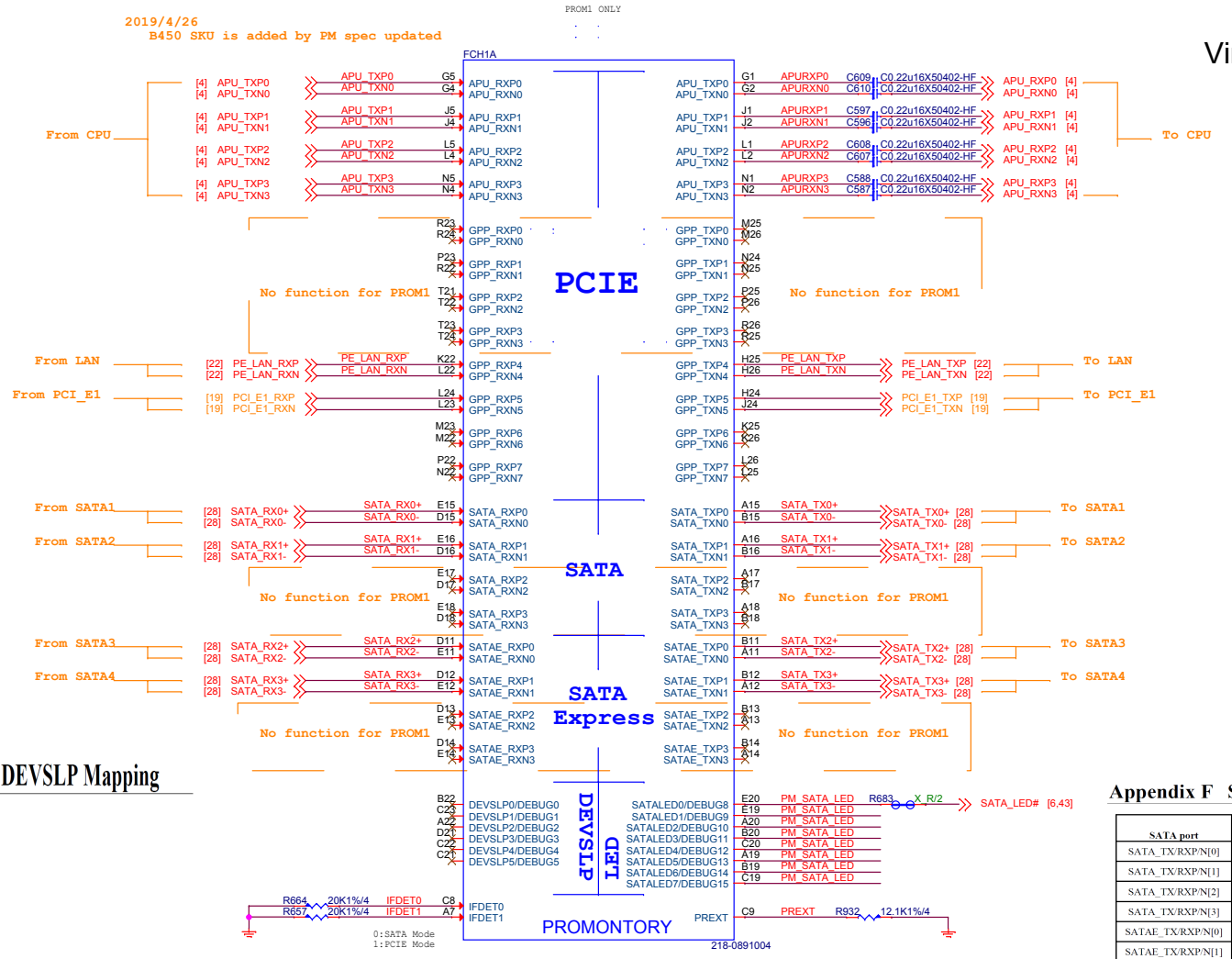

Vinafix.com

AMD 300-Series Chipsets, "Promontory" Sub-Family Data Sheet 55553 Rev. 1.10 May 2018

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

Appendix G SATA Port to DEVSLP Mapping

SATA port	DEVSLP signal
SATA_TX/RXP/N[0]	DEVSLP0
SATA_TX/RXP/N[1]	DEVSLP1
SATA_TX/RXP/N[2]	DEVSLP2
SATA_TX/RXP/N[3]	DEVSLP3
SATAE_TX/RXP/N[0]	SATAE_CLKREQ0N
SATAE_TX/RXP/N[1]	DEVSLP4
SATAE_TX/RXP/N[2]	SATAE_CLKREQ1N
SATAE_TX/RXP/N[3]	DEVSLP5

Appendix F SATA Port to SATA LED Mapping

SATA port	SATA LED
SATA_TX/RXP/N[0]	SATALED0
SATA_TX/RXP/N[1]	SATALED1
SATA_TX/RXP/N[2]	SATALED2
SATA_TX/RXP/N[3]	SATALED3
SATAE_TX/RXP/N[0]	SATALED4
SATAE_TX/RXP/N[1]	SATALED5
SATAE_TX/RXP/N[2]	SATALED6
SATAE_TX/RXP/N[3]	SATALED7

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MICRO-STAR INT'L CO.,LTD.

Title: Promontory-PCIE/SATA/SATAE

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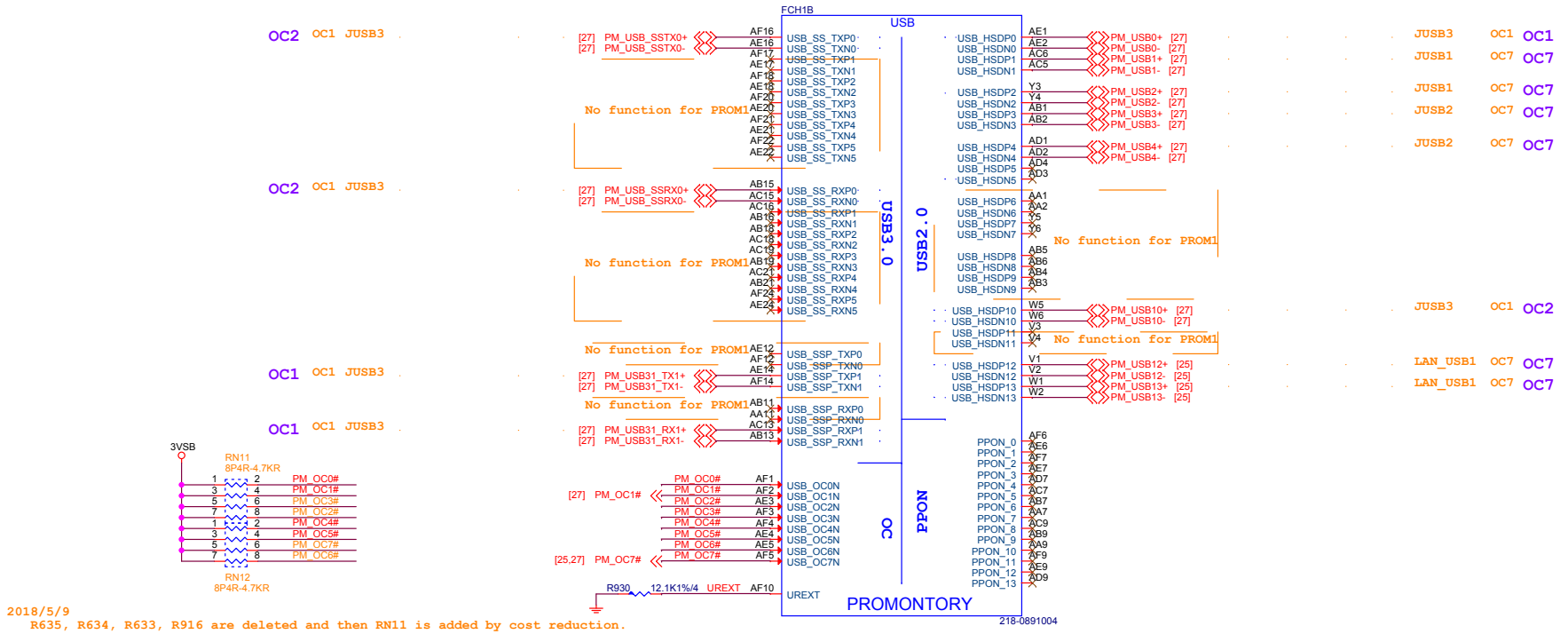
2019/4/30
B450 SKU is added by PM spec updated



2018/5/9
R635, R634, R633, R916 are deleted and then RN11 is added by cost reduction.

2018/5/9
R917, R632, R918, R631 are deleted and then RN12 is added by cost reduction.

Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

MICRO-STAR INT'L CO.,LTD.
Title: Promontory-USB/OC
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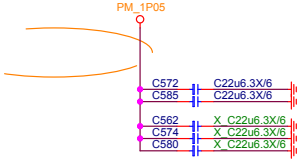
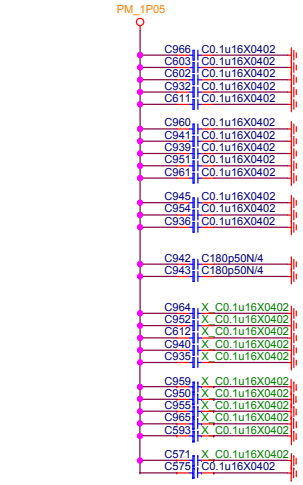
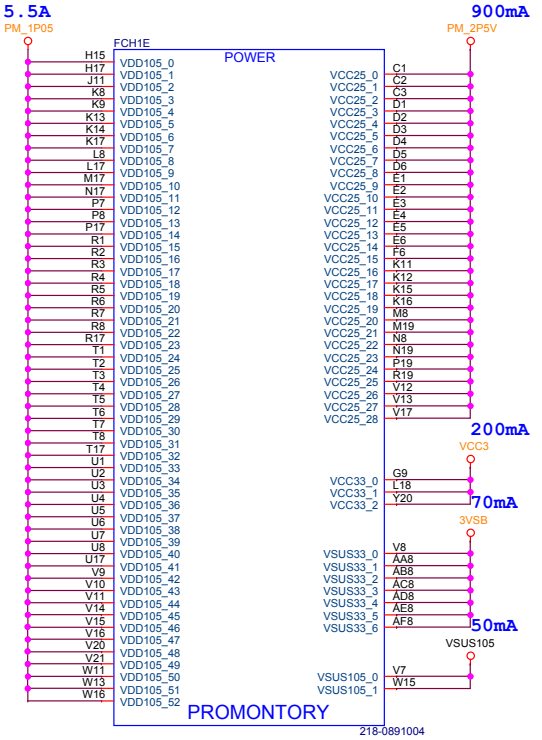
2019/4/30
L24, L23, L25, L30, L26, L28 are changed to 0ohm by Ryan's comment.

2019/4/30
B450 SKU is added by PM spec updated

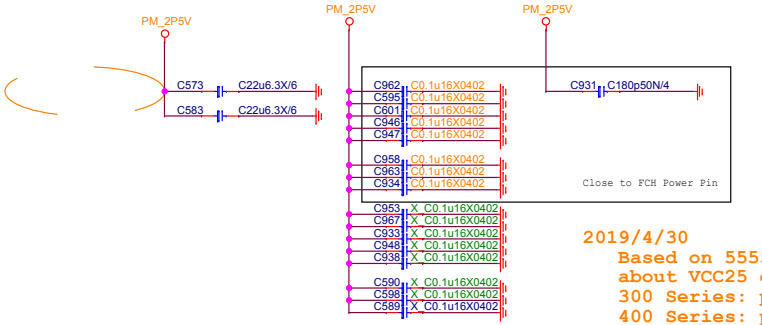
2019/5/8
L24, L23 are deleted by cost reduction





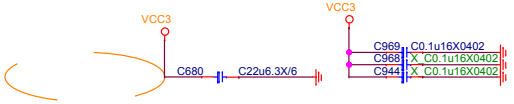


2019/5/8
L25 is deleted by cost reduction

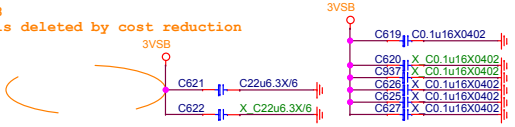


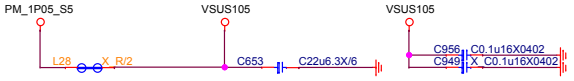
2019/4/30
Based on 55551 v1.08,
about VCC25 decoupling
300 Series: put 0.1uF
400 Series: put 1uF

2019/5/8
L30 is deleted by cost reduction



2019/5/8
L26 is deleted by cost reduction





2019/5/8
L28 is changed to 0ohm to short copper
by cost reduction.

Chapter 17 Power and Decoupling Requirements

Note: Unless otherwise specified, recommended capacitor dielectric material is X5R, X6S, X7R, or X7S ceramic. Designers may replace a larger capacitor body size with a smaller body size. Transposed body sizes are acceptable and preferred.

No.	Y/N/V	Group	Explanation	Qty	Value	Units	Size/Tol	Comments
17-5		VDD105	Ceramic capacitors.	6	22	µF	0805	
17-10			Ceramic capacitors.	25	1	µF	0402	
17-15		VCC25	Ceramic capacitors.	4	22	µF	0805	
17-20			300 Series: Ceramic capacitors.	12	0.1	µF	0402	
17-21			400 Series: Ceramic capacitors.	12	1	µF	0402	
17-25		VCC33	Ceramic capacitor.	1	22	µF	0805	
17-30			Ceramic capacitors.	1	0.1	µF	0402	
17-35		VSUS33	Ceramic capacitors.	1	22	µF	0805	
17-40			Ceramic capacitors.	1	0.1	µF	0402	
17-45		VSUS105	Ceramic capacitor.	1	22	µF	0805	
17-50			Ceramic capacitors.	2	0.1	µF	0402	

MICRO-STAR INT'L CO.,LTD.

Title: Promontory-Power

Size | Document Number: MS-7C52.. | Rev: 10

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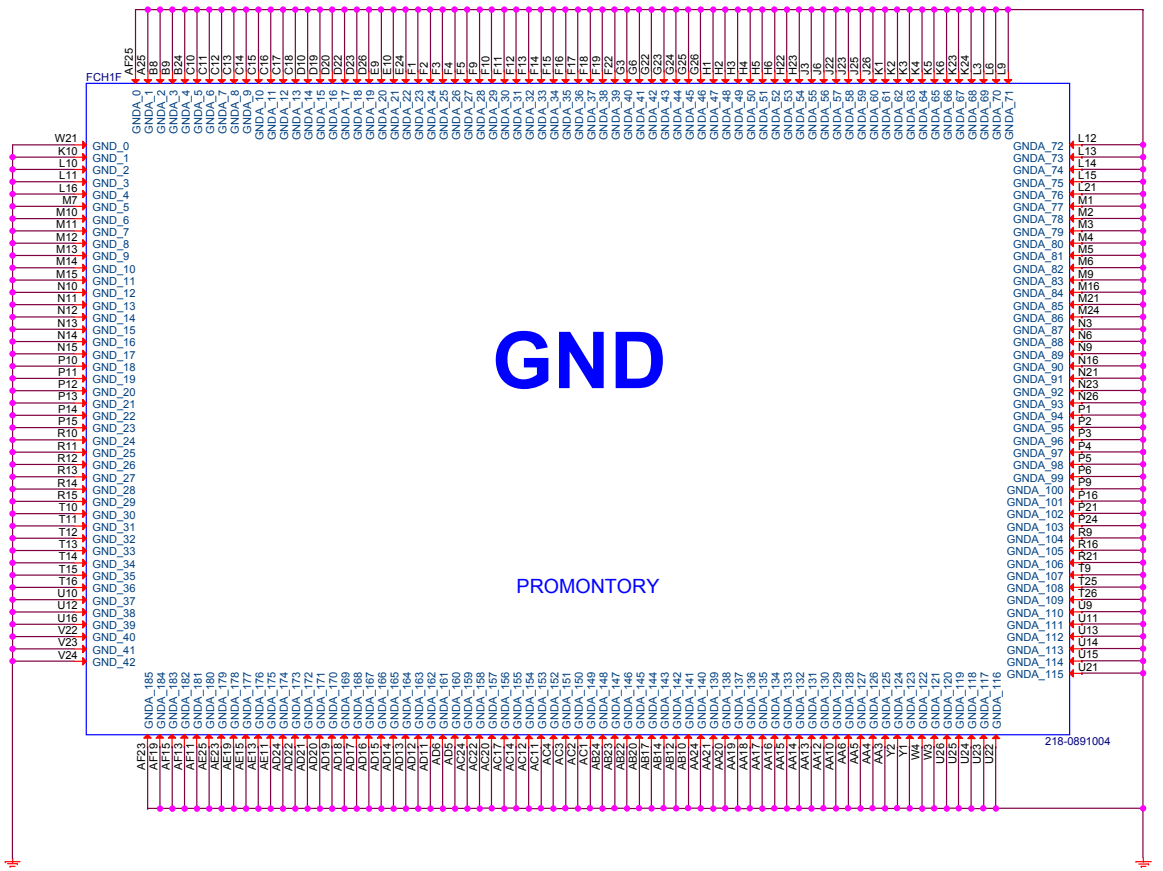
2019/4/30
B450 SKU is added by PM spec updated



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MICRO-STAR INT'L CO.,LTD.			
Title: Promontory-GND			
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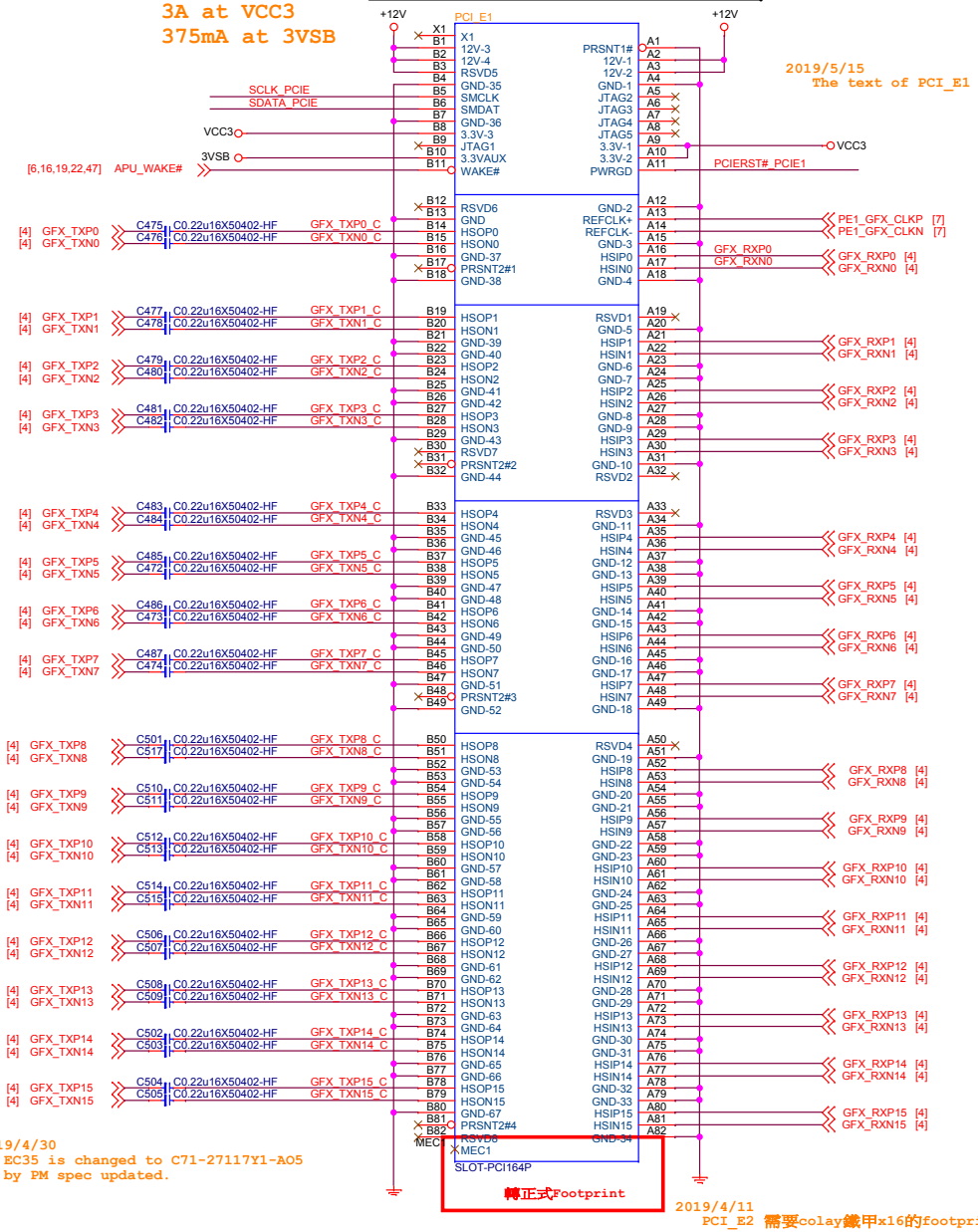
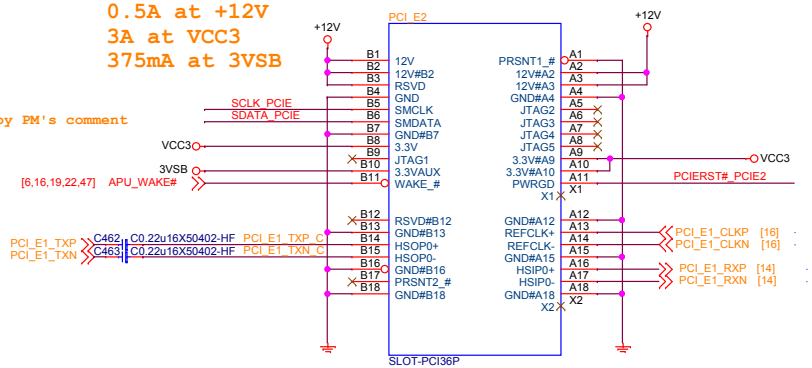
PCI EXPRESS x16 Slot

5.5A at +12V
3A at VCC3
375mA at 3VSB

0.5A at +12V
3A at VCC3
375mA at 3VSB

2019/5/15
The text of PCI_E1 & PCI_E2 are swapped by PM's comment



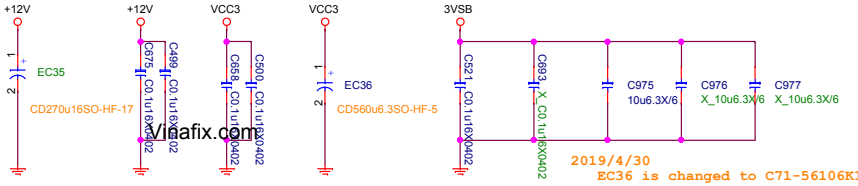


2019/4/15
PCI_E3, C647, C648, R800 are deleted by PM spec.

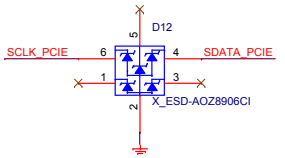
2019/4/30
EC35 is changed to C71-27117Y1-AO5
by PM spec updated.

轉正式Footprint

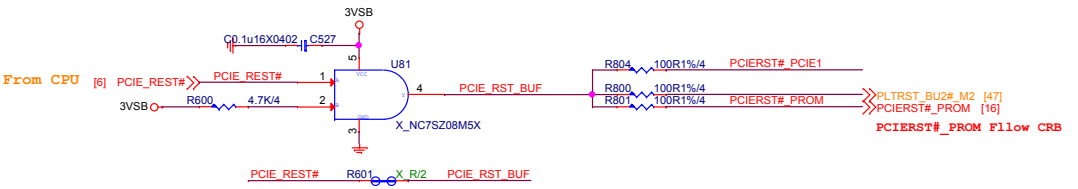
2019/4/11
PCI_E2 需要colay鐵甲x16的footprint，P/N:N11-1641491-L06)



2019/4/30
EC36 is changed to C71-56106K1-AO5
by PM spec updated



within 500mil

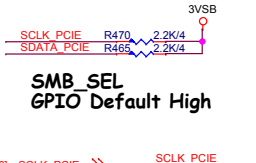


PROM RESET

From SIO
From FCH

Co-lay FCH Reset for meet FCH sequence. See 55553.

SMBus separate circuit



MICRO-STAR INT'L CO.,LTD.

Title: PCIE X16(X1*2) SLOT

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GP70 的GPIO可以選成GRN_LED ，所以有呼吸燈的功能 ，但有兩項要注意 :
1, GRN_LED在您的案子應該會是PWR LED (LED VCC).
2, GP70有DSW_EN的hardware strapping ，所以外部會有 pull-up 到SIO_3VA.

U46

ESPI/LPC Interface
PLTRST#/LRESET#
ESPI_CLK/LCLK
ESPI_RST#/LDRQ#
SERIRQ
ESPI_CS#/LFRAME#
ESPI_IO0/LAD0
ESPI_IO1/LAD1
ESPI_IO2/LAD2
ESPI_IO3/LAD3

UART SIR
RIA#/GP87
DCDA#/GP86
(TESTMODE1_EN)SOUTA/GP85
SINA/GP84
(FANOUT_DEF_EN)DTRA#/GP83
(2E_4E_SEL)RTSA#/GP82
DSRA#/GP81
CTSA#/GP80

KBC Function
KBRST#
(ESPI_EN)GA20M
AUXFANIN2/GP20/KDAT
CIRRX/AUXFANOU2/GP21/KCLK
AUXFANIN3/GP22/MDAT
AUXFANOUT3/GP23/MCLK

DSW Interface
GP54/SLP_SUS#
DPWROK
DEEP_S5_1/CASEOPEN1#
USBEN/3VSBSW/PWROK/ATXPGDO

Hardware Monitor
VIN2
VIN1
VIN0
CPUVCORE
VREF
AUXTIN0/VIN4
CPUTIN

FAN Control
CPUFANIN
CPUFANOUT
SYSFANIN
SYSFANOUT

ACPI Function
RSMRST#
PSIN#
PSOUT#
SLP_S3#
SLP_S5#
PSON#
ATXPGD
PWROK
RSTOUT0#/GP74
GP57/AUXFANIN2
GP56/AUXFANOUT2

Power Pin
PWR_FAULT#GP26/TSIC
PECI/TSID
GPO/GP73/CUT_VBAT
(DSW_EN)GP70
VIN7/AUXTIN3/ATX_5VSB
PAD_CAP
PCHVSB
VTT
VBAT
3VSB
AVSB
3VCC
PAD_VDD
VSS
CPUD-/AGND

NCT5565D

Change P/N

2018/5/10
R2386 is deleted by Ryan's comment

20181029
update to G3下可clean CMOS.

default Push-Pull

Stuff for New version IO

1.5V

=1.527V

<1.2V DPWROK LOW FOR AC POWER LOSS

close to PIN11

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HW Monitor - Voltage

VCORE R350 10K1%/4 CPUVcore
R368 X_10K1%/4 C356 10u6.3X/6

+12V R369 220K1%/4 VIN0
R370 20K1%/4 C344 C0.1u16X0402

VCC5 R372 12K1%/4 VIN1
R359 3K1%/4 C351 C0.1u16X0402

VCCP_NB R362 10K1%/4 VIN2
R407 X_10K1%/4 C316 10u6.3X/6

default Push-Pull
PLTRST_BU1#_R R462 4.7K/4
CHIP_PWGD R390 1K/4
R374 X_4.7K/4
CPUTIN R385 X_1K/4
PWRBTIN R356 10K1%/4
C384 C0.1u16X0402
HM_VREF C391 4.7u6.3X/6

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C388 10u6.3X/6 C406 1u6.3X/4
close to pin3

C396 10u6.3X/6 C370 1u6.3X/4
close to pin24

Thermal Monitor

For CPU Under Socket
HM_VREF
R719 10K1%/4
CPUTIN
RT5 10KT1%/4
C684 C2200p50X/4
GNDHM

For System Close to SIO
SYSTIN
Q52 P-PMBS3906
C379 C2200p50X/4
GNDHM

SIO_3VA
DEEP_S5 R814 47K/4

3V Analog Power

SIO_3VA CP24 X_COPPER AVCC3
C415 C0.1u16X0402 C318 10u6.3X/6

COM PORT

VCC3
R841 X_2.7K/4 SINA
R819 X_2.7K/4 CTSA#
R836 X_2.7K/4 RIA#
R835 X_2.7K/4 DCDA#
R827 X_2.7K/4 DSRA#
NO USE UART PORT1

C738 X_C0.1u16X0402
VCC5
U70 GD75232DBR
NRIA NCTSA# NDSRA# NSINA NDCDA#
RTSA# DTRA# SOUTA
VCC RA1 RA2 RA3 RA4 RA5
DA1 DA2 DA3 GND
VDD RY1 RY2 RY3 RY4 RY5
DY1 DY2 DY3 VSS
+12V_COM RIA# CTSA# DSRA# SINA DCDA#
NRTSA NDTRA NSOUTA -12V_COM

C739 C0.1u16X0402
D42 1N4148W +12V
D45 1N4148W -12V
C750 C0.1u16X0402

JCOM1 H2X5[10]M
NDCDA# NSOUTA NRTSA NRIA NSINA NDTRA NDSRA# NCTSA#

CN2 X_8P4C-470p50X/6
NRTSA NDSRA# NCTSA# NRIA

CN1 X_8P4C-470p50X/6
NDCDA# NSOUTA NSINA NDTRA

POWER ON STRAPPING PIN FOR NCT5565D

PIN	5563D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%.	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN

VCC3
R371 X_1K/4 RTSA#
R381 1K/4 DTRA#
R387 1K/4 SOUTA
R498 1K/4
R486 X_1K/4
R503 X_1K/4

SIO_3VA
R619 1K/4 GA20M
R620 1K/4 DSW_EN
AMD Platform
R499 X_1K/4
R485 X_1K/4

MSI MICRO-STAR INT'L CO.,LTD.
Title: SIO NCT5565
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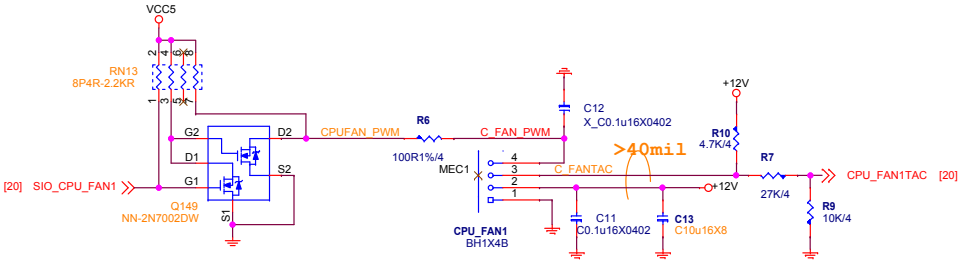
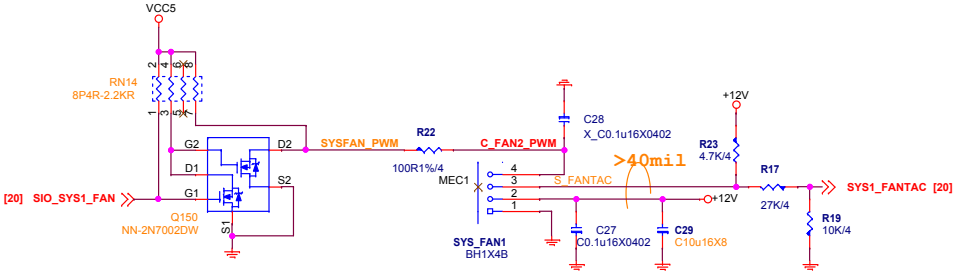
FAN(direct PWM mode_)



2019/4/15
U2, C5, R8, C9, C23 are deleted; R1517, R1518, Q149 are added; R4 is changed to 2.2Kohm by PM spec.

2019/4/15
C13 is changed from 22uF to 10uF; D5, C10, C6 are deleted by the latest module circuit

2018/5/9
R1517, R1518, R4 are deleted and then RN13 is added by cost reduction.



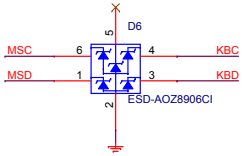
2019/4/15
U3, C14, R21, C20, C32 are deleted; Q150, R1520, R1519 are added; R20 is changed to 2.2Kohm by PM spec

2019/4/15
C29 is changed from 22uF to 10uF; D8, C21, C15 are deleted by the latest module circuit

2018/5/9
R1520, R1519, R20 are deleted and then RN14 is added by cost reduction.

PS2

TVS P/N:
D0G-45B0510-I14



layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

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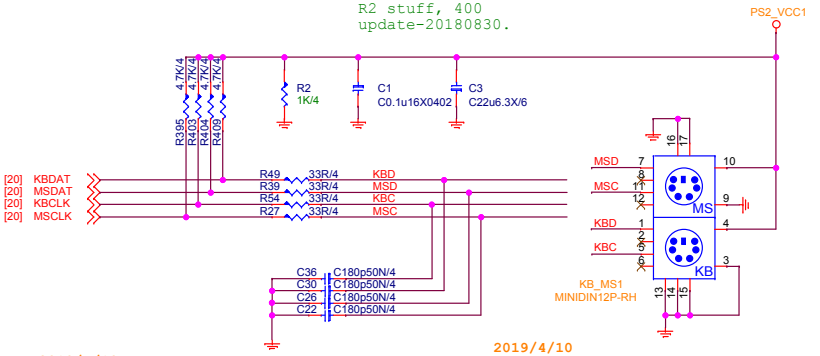
20181026:
R2 stuff, 400
update-20180830.



2019/4/10
About PS2 circuit move from the page 25

2019/4/10
KB_MS1 is changed to N56-12F0151-H06 by PM spec.

MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN Control

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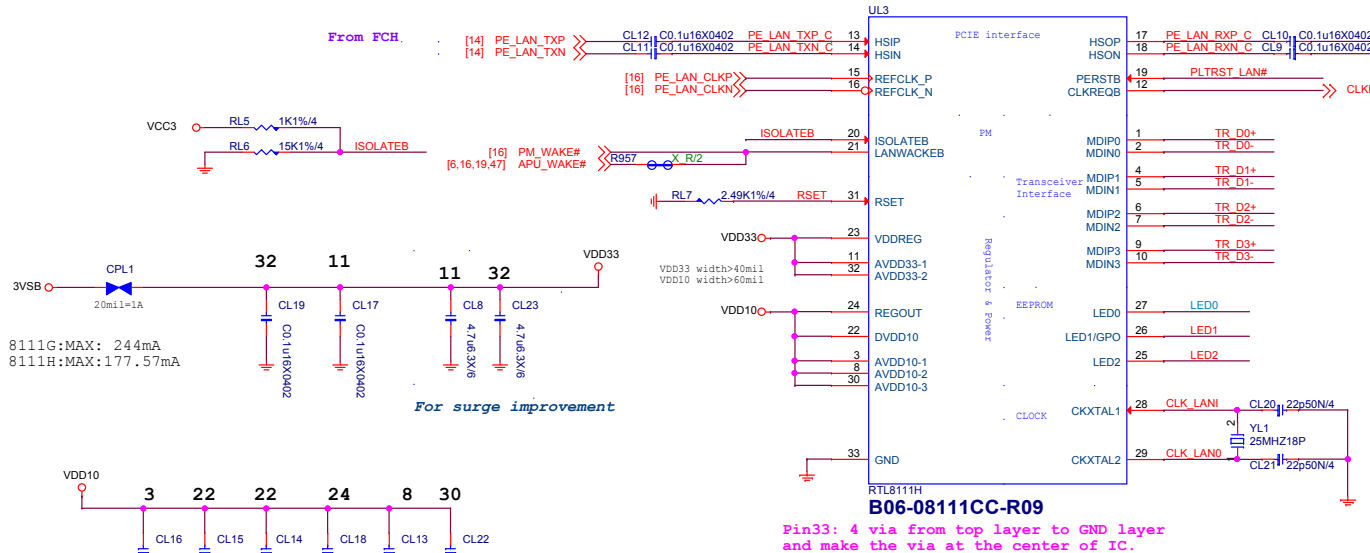
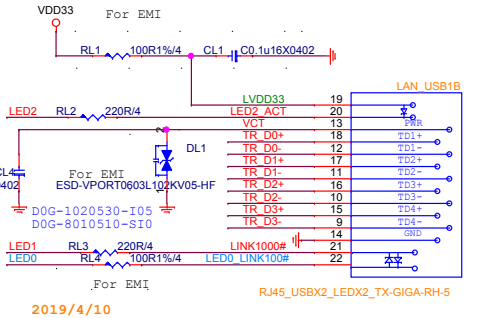
RTL8111G/RTL8111H Giga LAN

LAN Connector

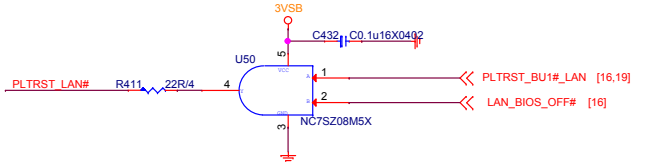
8111H:B06-08111CC-R09
8111G:B06-081116C-R09



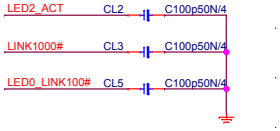


2019/4/10
LAN_USB1B is changed to N58-22F0731-F02 by PM spec.

2019/5/8
U50.5 is changed from VCC3 to 3VSB by Ryan's comment

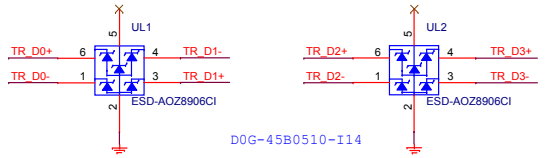


2015.06.22



ESD Protect

UL2&UL3 close to connector



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-STAR INT'L CO.,LTD.

Title: LAN-RTL8111H

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Type B:
ALC892/887

Follow APU power well

CA14 closed PIN25
CA31 closed PIN38
CA30 closed PIN38

11mA
Closed Codec
Closed PIN9
CPU_1P8_S5
VCC3
CA28 X_10u6.3X/6
CA18 C0.1u16X0402
VOUT
CA30 C0.1u16X0402
CA14 C22u6.3X/6
CA31 10u6.3X/6

11mA
Closed PIN1
VCC3
CA20 10u6.3X/6
CA19 C0.1u16X0402

UA1

[24] EAPD
EAPD
EAPD/SPDIFI
SPDIF-OUT
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2

[5] AZ_SDOUT
[5] AZ_SDIN0
[5] AZ_SYNC
[5] AZ_RST#
RA21 33R/4 SDIN0
SDATA-OUT
SDATA-IN
SYNC
RESET#

[5] AZ_BITCLK
BCLK

AZ_SDIN0
CA22 X_10p50N/4
REGREF
CA24 10u6.3X/6
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF

SENSE_A
SENSE_B
SENSE A
SENSE B

MIC1_V_R
MIC2_VREFO
MIC1_V_L
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L

45.8mA
LDOVDD
LINE2_VREFO
VREF_AUDIO
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
SENSE C
JDREF

CA16 X_C0.1u16X0402
CA17 10u6.3X/6
Closed Codec
JDREF
RA23 20K1%/4
BEEP
GPIO1/DMIC-DATA
DVSS
AVSS
AVSS
ALC892-CG-RH

CA16.CA17 close to Pin27

FRONT-R
FRONT-L
A_LOUT_R ECA3 1+ 2 CD100u10EL5-RH-2 LOUT_R
A_LOUT_L ECA4 1+ 2 CD100u10EL5-RH-2 LOUT_L

SURR-R
SURR-L

CENTER
LFE

SIDE-R
SIDE-L

LINE1-R
LINE1-L
A_LINE_IN_R CA8 10u6.3X/6 LINE_IN_R
A_LINE_IN_L CA9 10u6.3X/6 LINE_IN_L

LINE2-R
LINE2-L
A_LINE2_R ECA1 1+ 2 CD100u10EL5-RH-2 LINE2_R
A_LINE2_L ECA2 1+ 2 CD100u10EL5-RH-2 LINE2_L

MIC1-R
MIC1-L
A_MIC1_R CA10 10u6.3X/6 MIC1_R
A_MIC1_L CA11 10u6.3X/6 MIC1_L

MIC2-R
MIC2-L
A_MIC2_R CA12 10u6.3X/6 MIC2_R
A_MIC2_L CA13 10u6.3X/6 MIC2_L

CD-R
CD-GND
CD-L

2019/4/11
ECA1, ECA2, ECA3, ECA4 are changed to C91-1011021-N07 by PM spec
2019/4/30
ECA1, ECA2, ECA3, ECA4 are changed to C91-1011041-P01 by PM spec

2019/4/18
CA8, CA9, CA10, CA11, CA12, CA13 are changed from 4.7uF/0805 to 4.7uF/0603 by "PN_190325" rule

2019/5/2
UA1 is changed to ALC892 from ALC887 by PM spec updated.

2019/5/8
CA8, CA9, CA10, CA11, CA12, CA13 are changed from 4.7uF to 10uF by module circuit

LIN_OUT
LOUT_R RA9 75R/4 LOUT_RA
LOUT_L RA12 75R/4 LOUT_LA
FRONT_JD
AUDIO1B
DA1 ESD-MLVS0402L04
DA2 ESD-MLVS0402L04
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
N54-13F0591-F02

2019/4/10
AUDIO is changed to N54-13F0591-F02 by PM spec.

LIN_IN
LINE_IN_R RA5 75R/4 LINE_IN_RA
LINE_IN_L RA7 75R/4 LINE_IN_LA
LINE1_JD
AUDIO1A
CA3 ESD-MLVS0402L04
CA4 ESD-MLVS0402L04
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
N54-13F0591-F02

2.2k for better recording quality

MIC1_V_L RA6 2.2K/4 MIC1_LA
MIC1_V_R RA2 2.2K/4 MIC1_RA
MIC1_R RA8 75R/4 MIC1_RA
MIC1_L RA3 75R/4 MIC1_LA
MIC1_JD
MIC1
AUDIO1C
CA1 ESD-MLVS0402L04
CA2 ESD-MLVS0402L04
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
N54-13F0591-F02

for rear I/O 6port: 887VD/892:1k
for rear I/O 3port: 887VD/892:75R

D LIN_IN
E LIN_OUT
F MIC1
N54-13F0271-K06

[24] LOUT_LA
[24] LOUT_RA
LOUT_LA RA4 22K/4
LOUT_RA RA1 22K/4

EMI
CA6 X_C0.1u16X0402
CA5 X_1000p50N/4
CPA1 X_COPPER
CPA2 X_COPPER

Closed Codec
SENSE_A
RA17 5.1K1%/4 FRONT_JD
RA18 10K1%/4 LINE1_JD
RA16 20K1%/4 MIC1_JD

2019/5/2
LA1 is unstuffed; LA8 is added; DA3 is connected from ATX_5VSB to LDOVDD by Robert's comment

Digital Analog
ATX_5VSB
LA1 X_0R/8
LA8 0R/8
5VDUAL
DA3 X_S-RB521S30
CA32
CA33 10u6.3X/6
C0.1u16X0402
LDOVDD

CA32,CA33 close to LA1

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DA8
LINE2_VREFO_Z
S-BAT54ALT1G
DA4
MIC2_VREFO_Z
S-BAT54ALT1G

RN15 8P4R-4.7KR

2018/5/9
RA579, RA578, RA581, RA583 are deleted and then RN15 is added by cost reduction.

MIC2_R RA28 75R/4 F_MIC2_R
MIC2_L RA24 75R/4 F_MIC2_L
LINE2_L RA34 75R/4 F_LINE2_L
LINE2_R RA32 75R/4 F_LINE2_R

JAUD1
F_MIC2_L
F_MIC2_R
F_LINE2_R
SENSE_B
F_LINE2_L
MIC
MICPWR
FLINE OUTR
HPON
FLINE OUTL
GND
PRESENCE#
LINE NEXT R
LINE NEXT L
MIC2_JD
LINE2_JD
H2X5[8]M
N31-2051411-H06
RA26 47R/4
CA35 C1000p50X4
RA27 39.2K1%/4
RA25 20K1%/4
DA5 DA6 DA7 DA9 ESD-MLVS0402L04

Close to Front panel
For HDA/AC97 front cable.

[24] F_LINE2_L
[24] F_LINE2_R
F_LINE2_L RA33 22K/4
F_LINE2_R RA31 22K/4

Varister --> cap for cost down
D0G-2710510-I05
D0G-2950500-SI0
Close to Jack

MSI MICRO-STAR INT'L CO.,LTD.
Title: Audio ALC892-1
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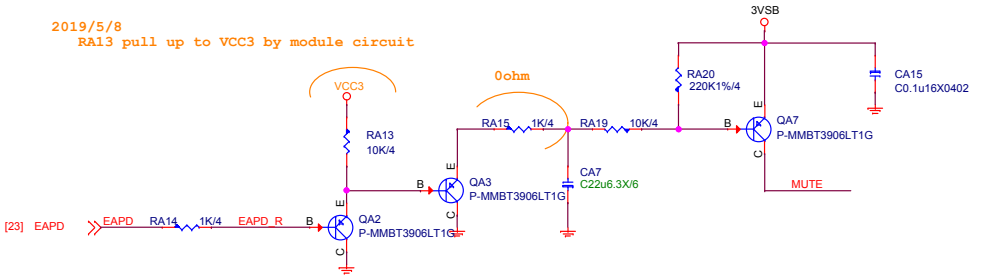
Rear Line OUT De-POP circuit

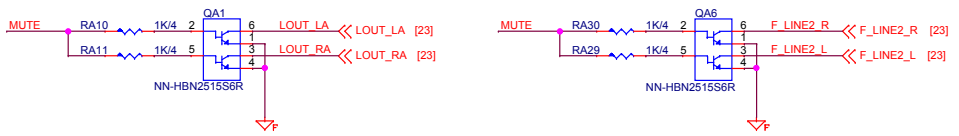
De-pop circuit for Rear Line out & Front Headphone out)

2019/5/8
RA13 pull up to VCC3 by module circuit



Digital

Analog



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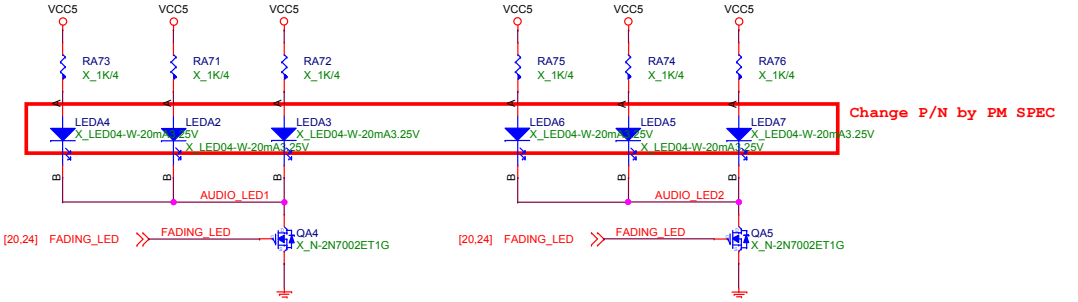
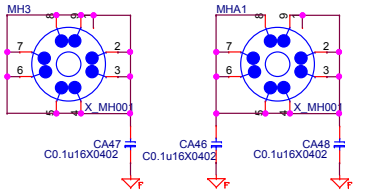
20181203
使用測光LED
Remove Audio LED,
RA73、RA71、RA72、RA74、RA75、RA76、LEDA4、LEDA2、LEDA3、LEDA6、LEDA5、LEDA7、QA4、QA5 unstuff.





2019/4/26
The pin1 of MH3, MHA1 are changed to GND by CND rule

MICRO-STAR INT'L CO.,LTD.

Title	Audio ALC892-2	
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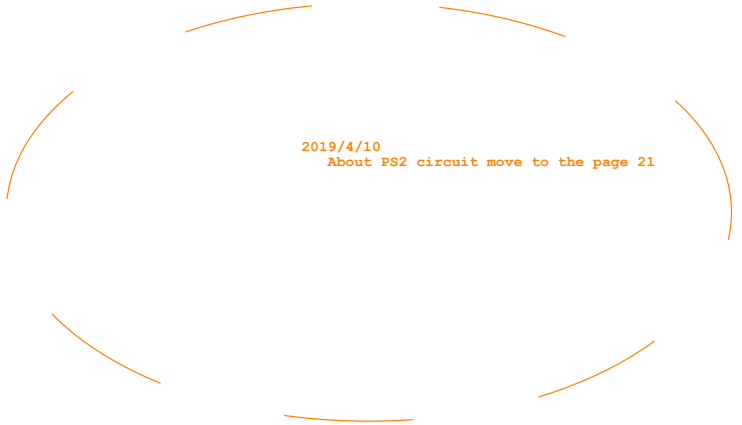
USB



2019/4/10
About PS2 circuit move to the page 21

[15] PM_USB12+
[15] PM_USB12-
L1
4P2R-0R0402
PMUSB12+
PMUSB12-

[15] PM_USB13+
[15] PM_USB13-
L2
4P2R-0R0402
PMUSB13+
PMUSB13-

D9
ESD-AOZ8906CI

USB20_LAN
LAN_USB1A
UP
DOWN
RJ45_USBX2_LEDX2_TX-GIGA-RH-5

2019/4/10
LAN_USB1A is changed to N58-22F0731-F02 by PM spec.

VCC5
R92
10K/4
Q16
NN-2N7002DW
PM_OC7# [15,27]
USB20_LAN
R93
10K/4

USB20_LAN
C65
C0.1u16X0402

2019/4/30
EC2 is changed to C71-56106K1-AO5
by PM spec updated
2019/5/3
EC2 is deleted by cost reduction

2019/5/3
R2401, R2394, U25, R2395, Q154, R2399,
R2396, R2397, Q155, R2400, R2398 are added
by Ryan's comment

USB Power

5V_FUSB
C71 X_C0.1u16X0402
C72 X_C0.1u16X0402
C73 X_C0.1u16X0402

ATX_5VSB
[31] DIMM_SBDRV
DIMM_SBDRV
Q137
P-P06P03LCGA
C755
X_C0.1u16X0402

[31] DIMM_VCCDRV
DIMM_VCCDRV
Q134
N-SM4503NHKPC-TRG_DFN5x6-8-HF
D03-4503N0C-ST8
VCC5

~~8.9A~~ 9.4A

2019/5/8
F1, F2 are changed to D08-0101700-P16 by Ryan's comment

5V_FUSB
F2
F-SPR-P110-HF
PS2_VCC1
~~1.5A (USB2.0*2+PS2)~~ 1A (PS2 * 2)

F1
F-SPR-P110-HF
USB20_LAN
1A (USB 2.0 * 2)
LAN_USB1

EC12 CD560u6.3SO-HF-5
F3
F-SPR-P260T
USB30_VCC1
1.8A
USB1

EC30 CD560u6.3SO-HF-5
F4
F-SPR-P260T
USB30_VCC3
1.8A
USB2

2019/5/3
EC12, EC30 are moved from page26 by cost reduction

F5
F-SPR-P260T
USB20_VCC1
2A
JUSB1, JUSB2

EC37 CD560u6.3SO-HF-5
F7
F-SPR-P260T
USB30_VCC2
1.8A
JUSB3

2019/5/3
EC37 is moved from page27 by cost reduction

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APU_USB_OC

USB_XOR0
R2401 X_0R/4
APU_OC0#

3VSB
R2394
10K/4
USB_XOR0
U25
[6,36,37,41] TYPE1_CPU_SEL
APU_OC0# [6,26]
SN74LVC1G86DCKR_SC70-5-RH

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP

VCC5
R2395
10K/4
Q154
NN-2N7002DW
R2399 15K1%/4
USB_XOR0
USB30_VCC1
R2396 10K/4
USB1

VCC5
R2397
10K/4
Q155
NN-2N7002DW
R2400 15K1%/4
USB30_VCC3
R2398 10K/4
USB2

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	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MICRO-STAR INT'L CO.,LTD.

Title: USB Rear PS2+USB2.0

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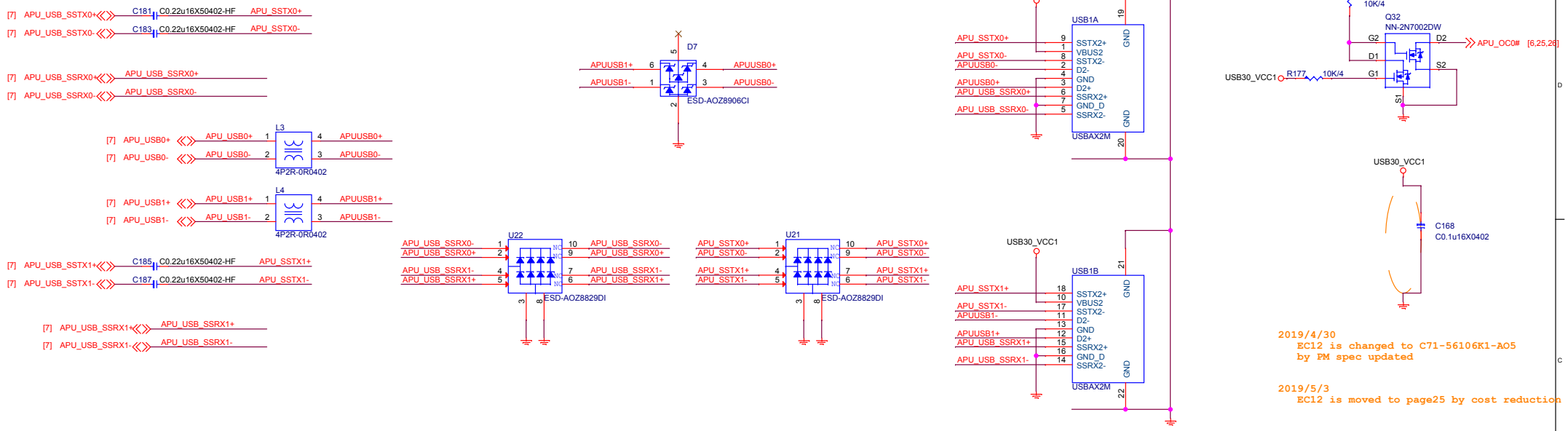
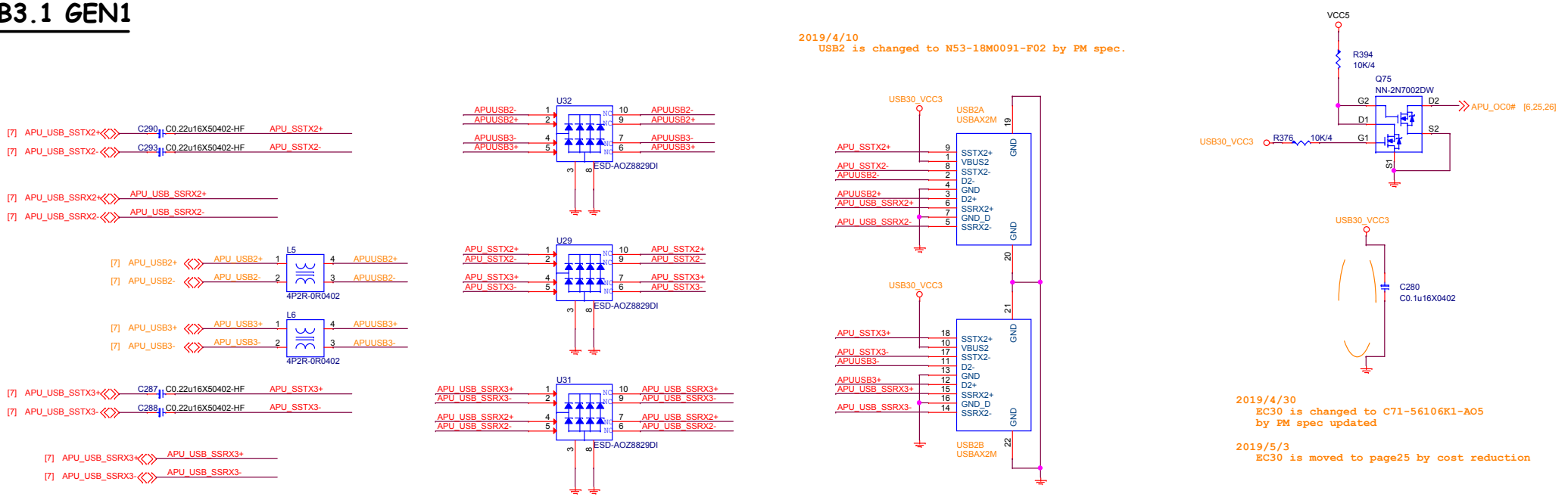
USB 3.1 GEN1



USB3.1 GEN1



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MICRO-STAR INT'L CO.,LTD.

Title	USB Rear LAN+USB3.1 GEN1	
Size	Document Number MS-7C52..	Rev 10
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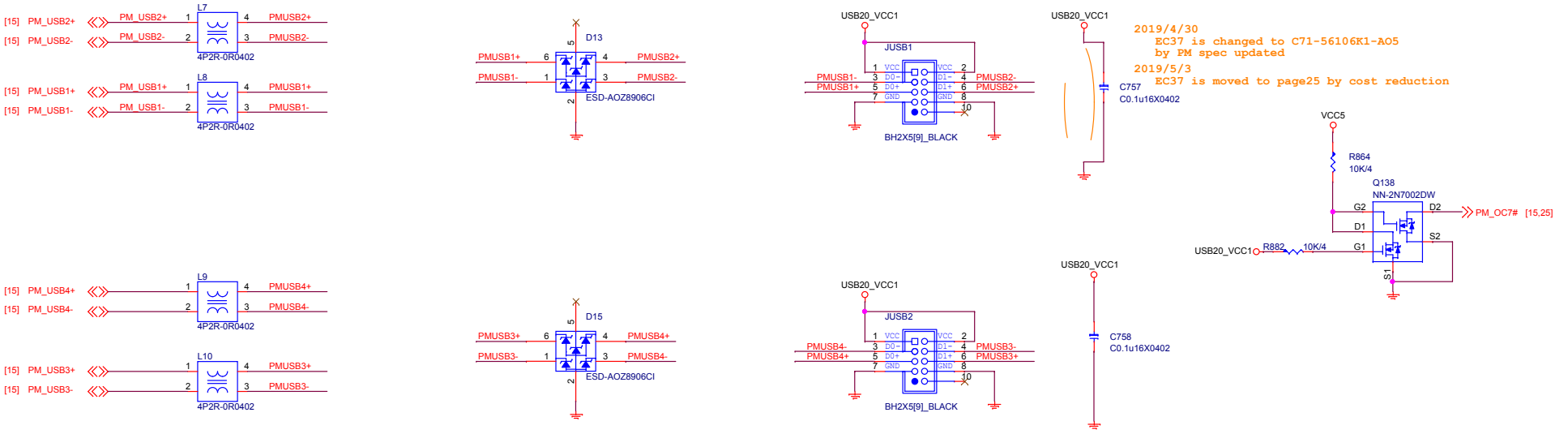
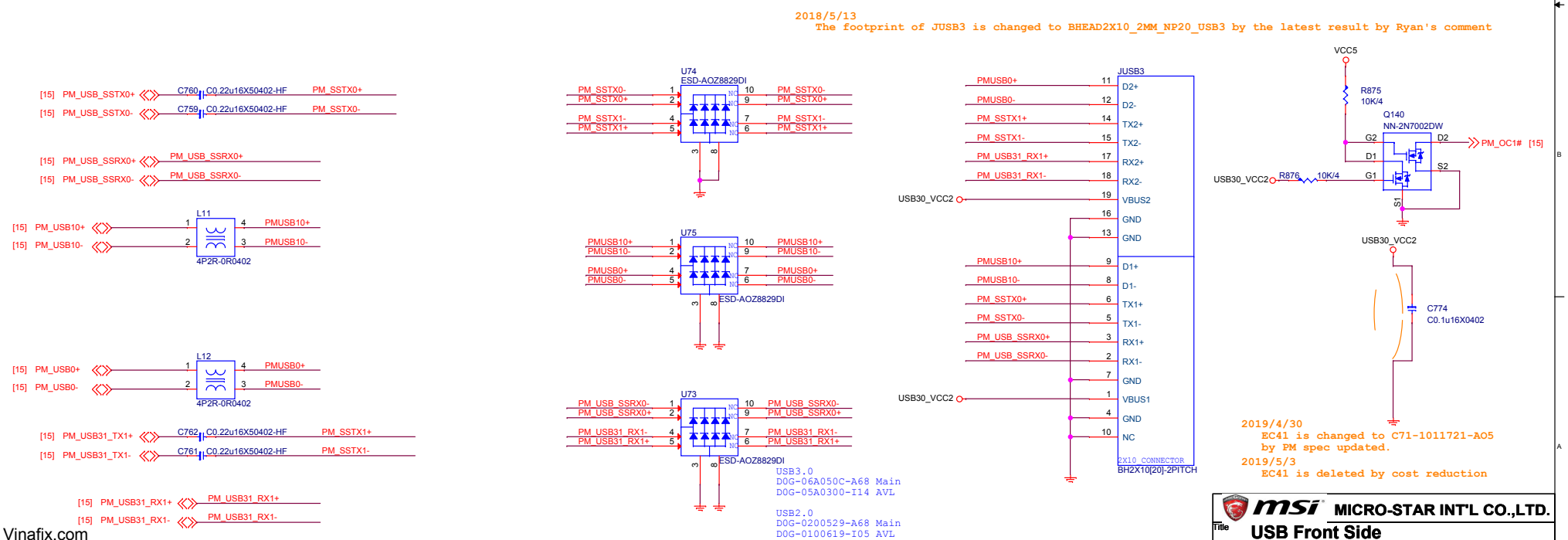
Front USB2.0



Front USB3.1 GEN1



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MICRO-STAR INT'L CO.,LTD.

Title: USB Front Side

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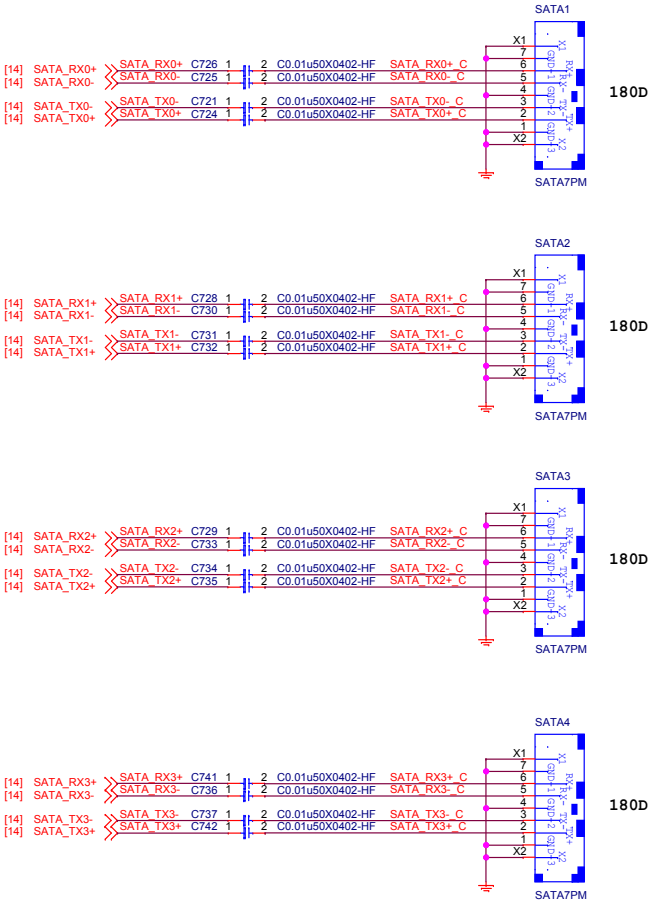
SATA Connector



MICRO-STAR INT'L CO.,LTD.

Title	SATA Connector	
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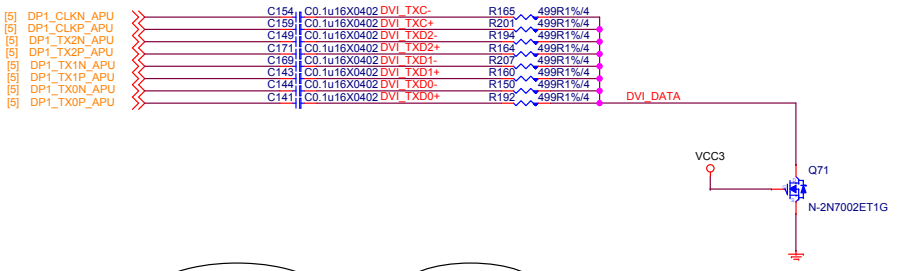
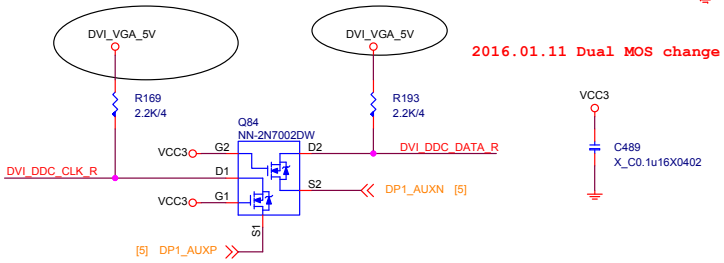
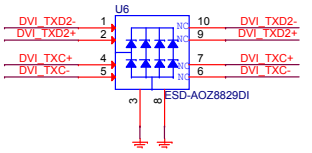
DVI level shifter

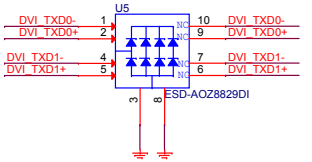
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



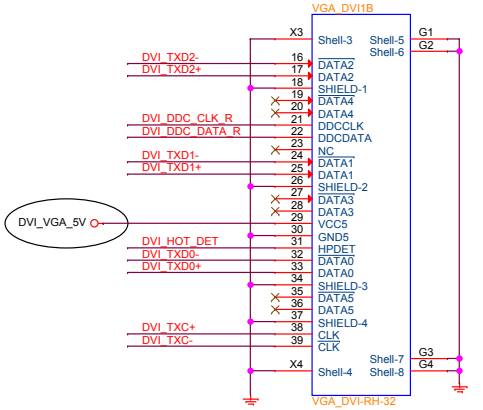


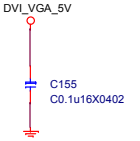
2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

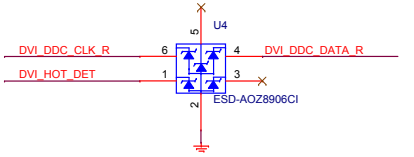


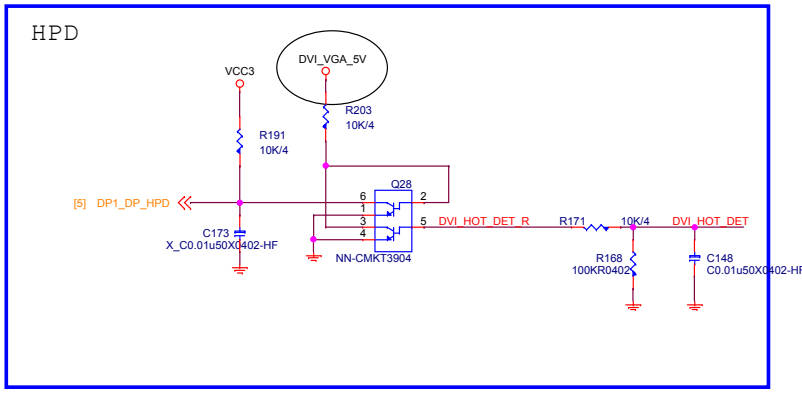


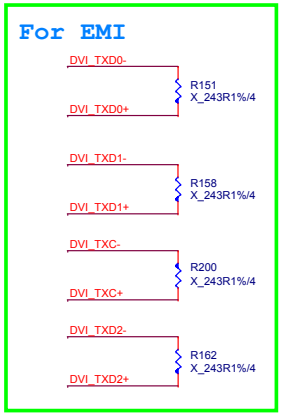
2019/4/10
VGA_DVI1 is changed to N58-43F0111-EB6 by PM spec.

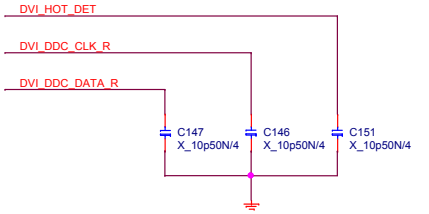












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MICRO-STAR INT'L CO.,LTD.

Title: DVI Connector

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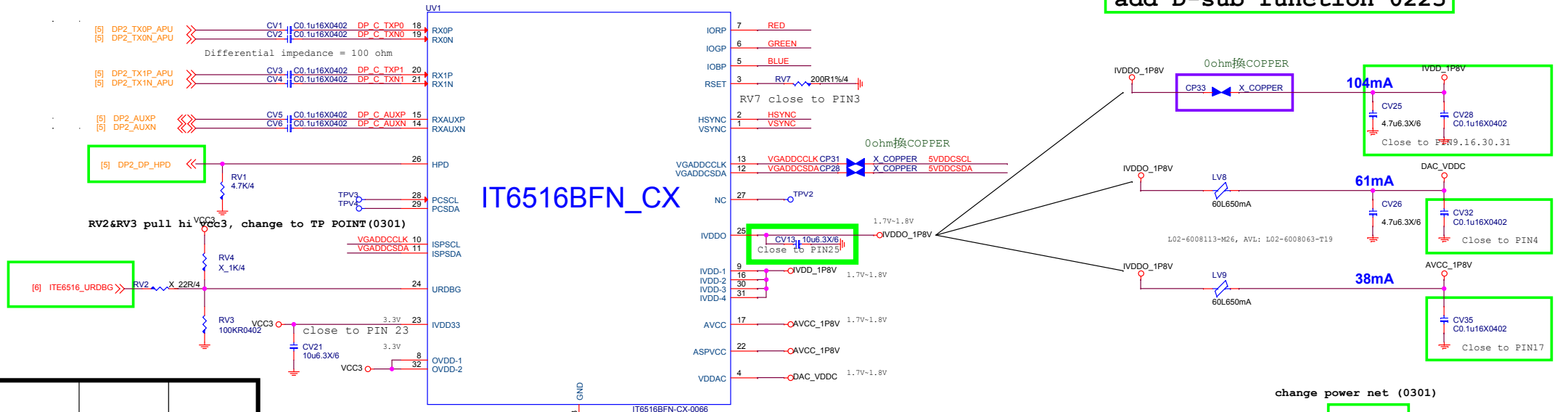
2019/5/8

Note: 7C52-02S are all no unstuff expect for DV1, FSV1, CV38, VGA_DVI1

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

20181203:
UV1 change to B0B-6516B3C-I15, FW改善省電.

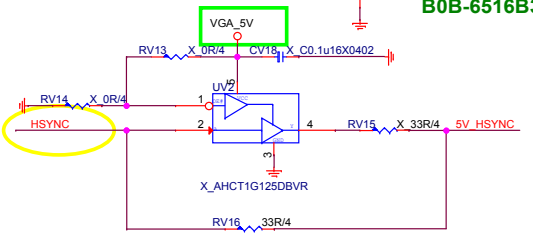
add D-sub function 0225



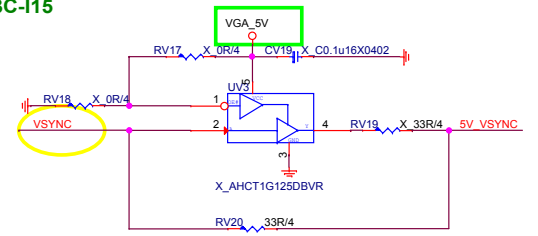
System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

B0B-6516B3C-I15

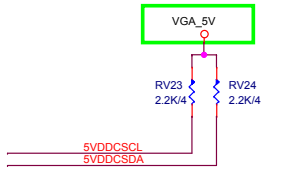
change power net (0301)



change power net (0301)

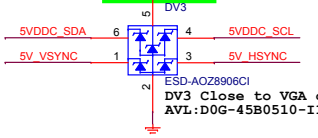


change power net (0301)



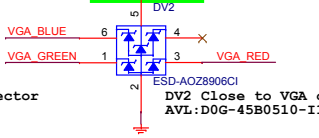
remove 3.3V-to-5V level shifter (0301)

PIN 5 NC 20160525



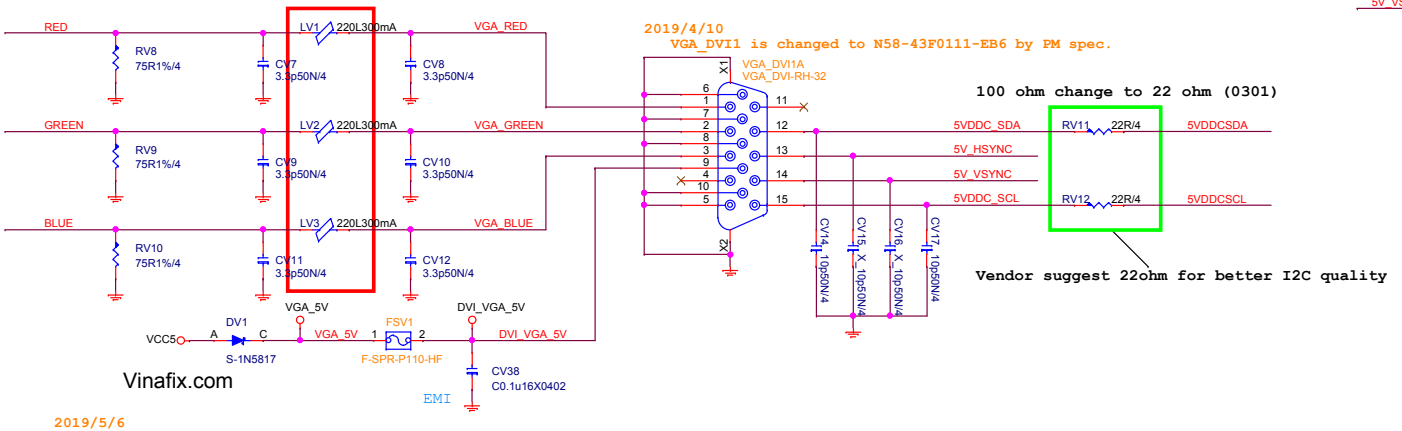
DV3 Close to VGA connector
AVL:D0G-45B0510-I14

PIN 5 NC 20160525



DV2 Close to VGA connector
AVL:D0G-45B0510-I14

P/N Change for VESA 1.2 SPEC PASS



2019/4/10
VGA_DVI1 is changed to N58-43F0111-EB6 by PM spec.

100 ohm change to 22 ohm (0301)

Vendor suggest 22ohm for better I2C quality

2019/5/6
FSV1 is changed to D08-0101700-P16 by Ivy's comment

Title	MSI MICRO-STAR INT'L CO.,LTD. DP to VGA ITE6516		
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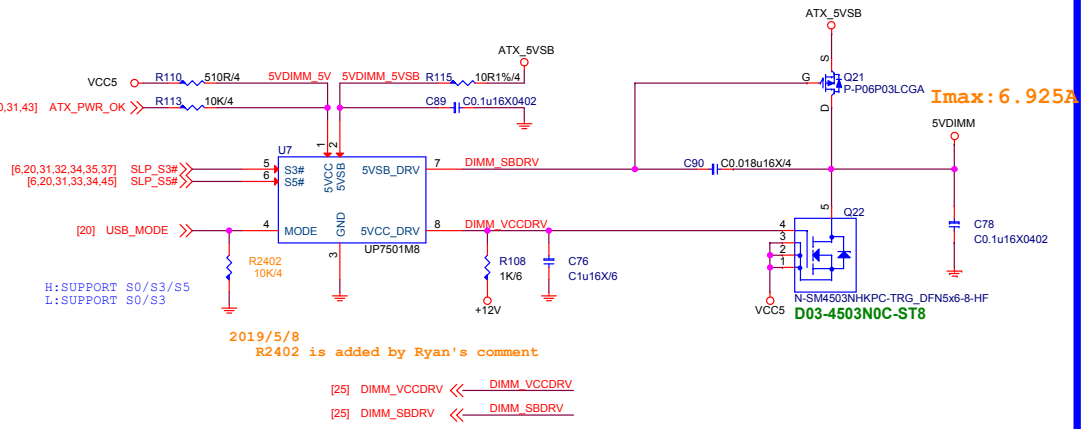
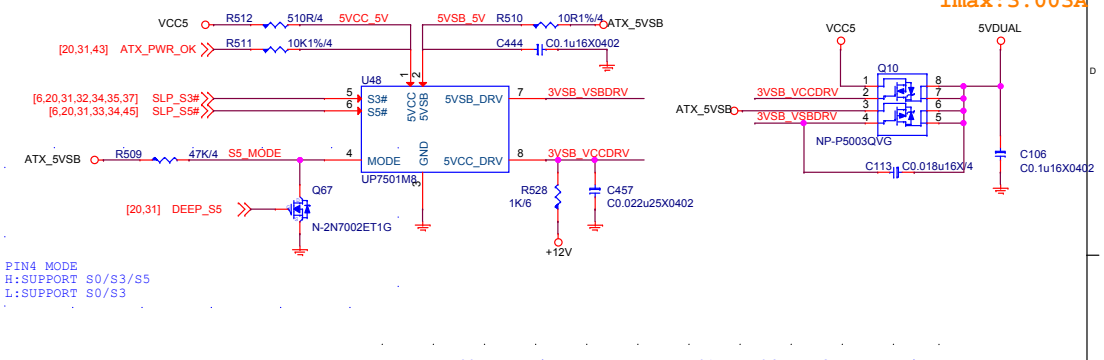
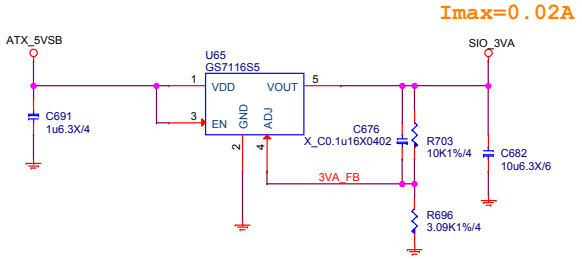
5VDIMM FOR DDR



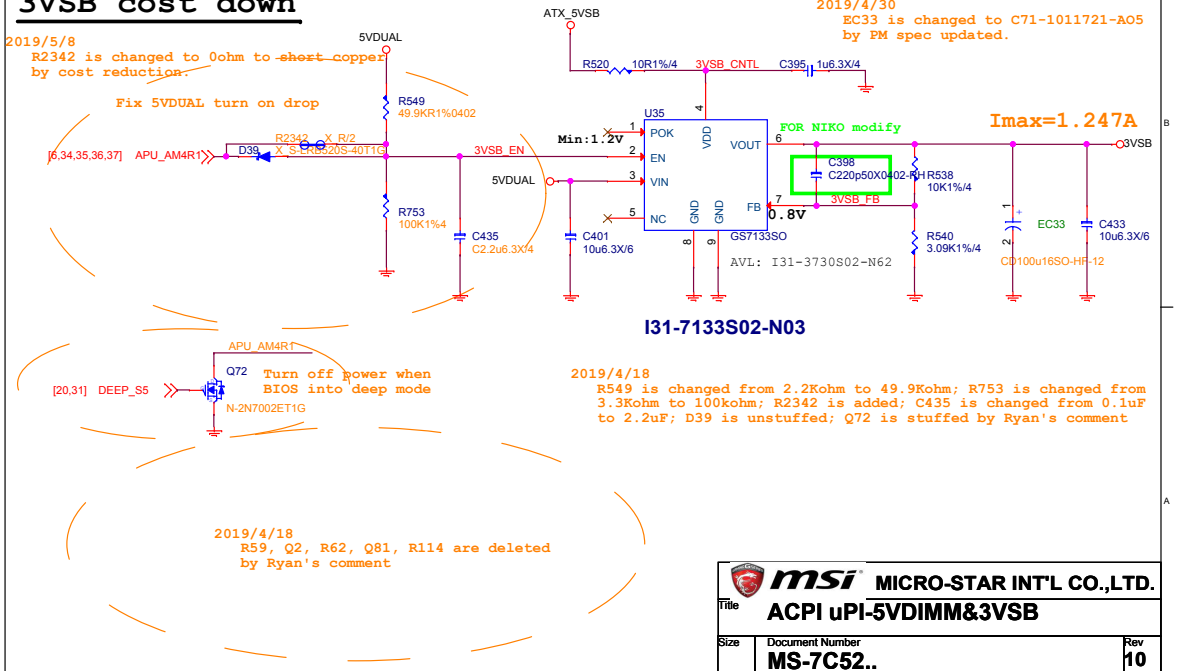
5VDUAL For 3VSB、CPU 1.8V 、 VDDP



SIO_3VA



3VSB cost down



Vinafix.com

MICRO-STAR INT'L CO.,LTD.

Title: ACPI uPI-5VDIMM&3VSB

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Promontory 1.05V_S0

2019/4/12
U58 is changed to SY8288; CHOKE15 is changed to 1R0; L22, L39 are deleted; CHOKE24, C1975, CP71, C605, C1977, C1512, R610 are added; R573 is changed to 39kohm; C519 is changed to 0.1uF; R582 is changed to 1.33Kohm; R781, R791, C1974 are reserved by Ryan's comment

2019/4/12
U58 is changed to SY8286; R2345, R2343, R2344 are added by Ryan's comment

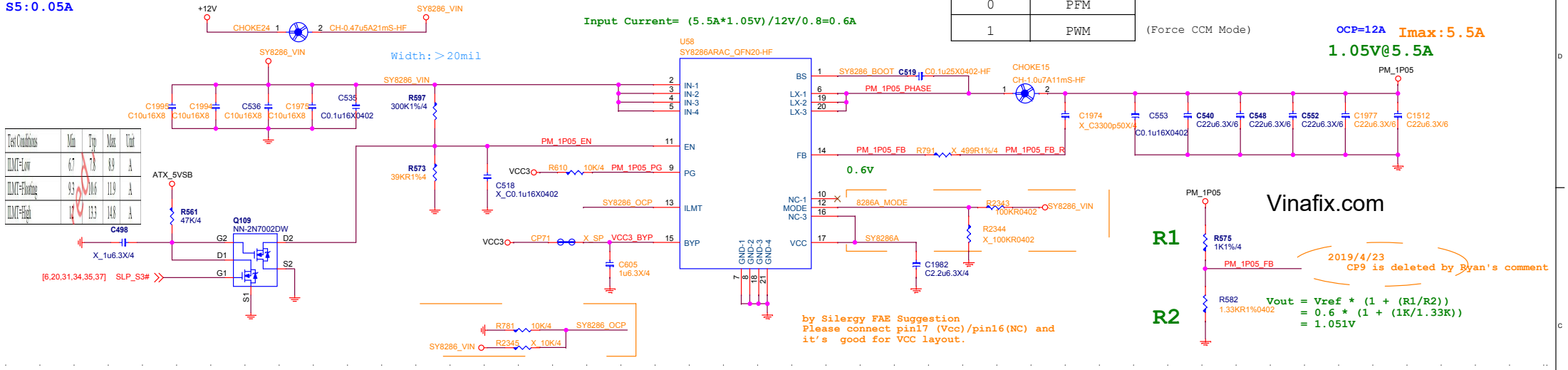
1.05V
S0:5.5A
S5:0.05A

8286A_MODE	Operating mode
0	PFM
1	PWM

(Force CCM Mode)

Input Current= (5.5A*1.05V)/12V/0.8=0.6A

OCP=12A Imax:5.5A
1.05V@5.5A



Test Conditions	Min	Typ	Max	Unit
ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A

by Silergy FAE Suggestion
Please connect pin17 (Vcc)/pin16(NC) and it's good for VCC layout.

2019/4/23
CP9 is deleted by Ryan's comment

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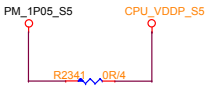
FOR Promontory 1.05V_S5

0.05A



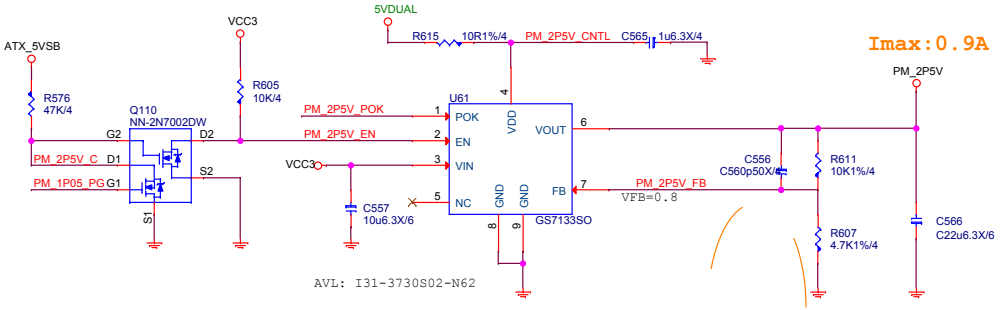
2019/4/16
R2341 is added; R663, C636, C629, U63, R675, R672, C645 are unstuffed by Ryan's comment

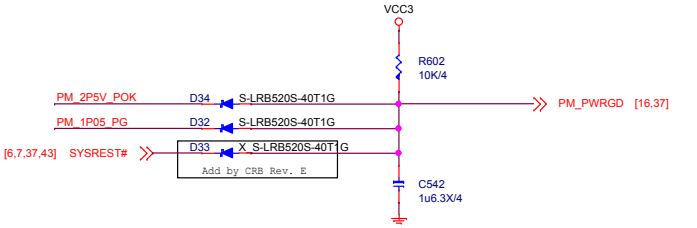
2019/4/25
R663, C636, C629, Q73, U63, C646, R675, R672, C645 are deleted by Ryan's comment

Promontory-2.5V

2.5V; 900mA

Imax:0.9A





2019/4/23
CP10 is deleted by Ryan's comment

Vinafix.com

MSI MICRO-STAR INT'L CO.,LTD.

Title	Promontory-1.05V/GS7133-2.5V	
Size	Document Number MS-7C52..	Rev 10
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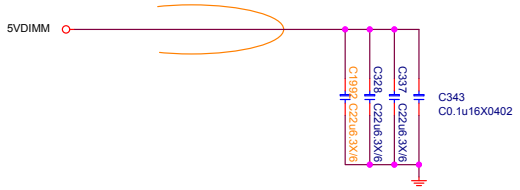
2DIMM :1.12A FOR DDR VPP2.5V

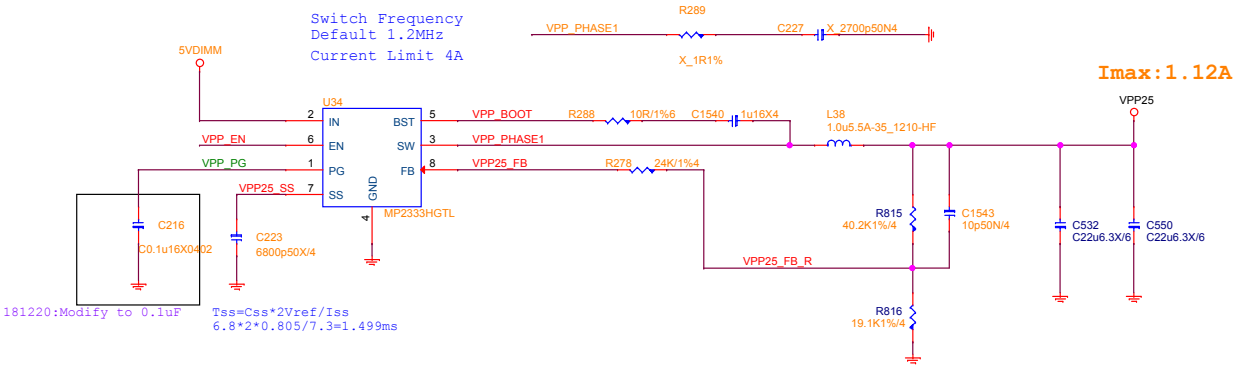
2019/4/12
U34 is changed from MP2143 to MP2333; L29, C443 are deleted and C1992 is added by Ryan's comment

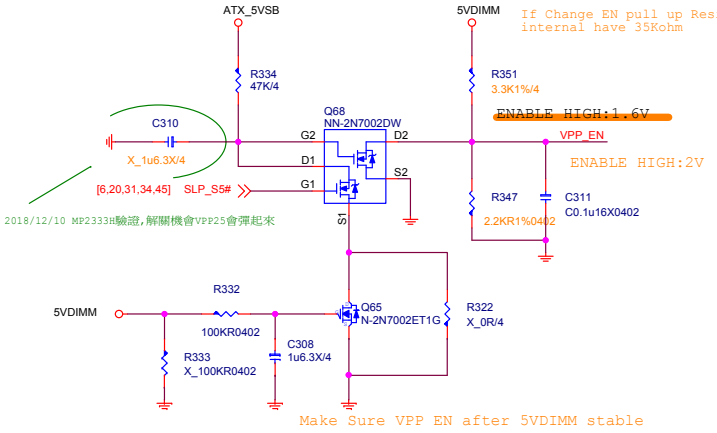
Input Current= Iout*SQRT((Vout/Vin)*(1-Vout/Vin))=1.5A



Switch Frequency
Default 1.2MHz
Current Limit 4A

Imax:1.12A





2019/4/12
R351 is changed from 2.2Kohm to 100Kohm; R347 is changed from 3.3Kohm to 82kohm; C310 is unstuffed by MP2333 solution

2019/5/7
R351 is changed from 100kohm to 3.3Kohm; R347 is changed from 82Kohm to 2.2Kohm by Ryan's comment

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 40µA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V VIN, I_{Zener} = (12V - 2.8V) / (604kΩ + 35kΩ) = 14µA.

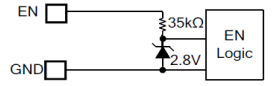
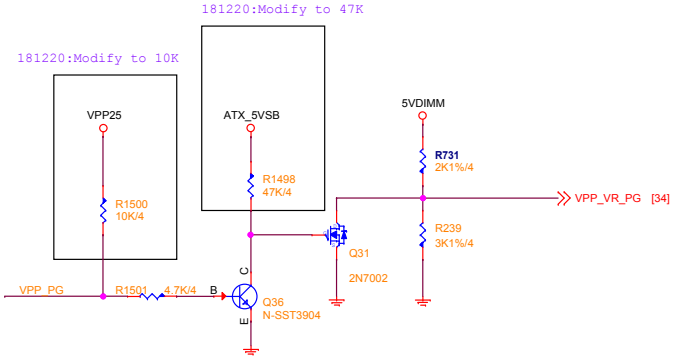


Figure 2: Zener Diode between EN and GND



2019/4/12
R1500, R1501, R1498, Q36, Q31, R731, R239 are added by MP2333 solution

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Title	DDR PWR VPP25	
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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT

R178: 280K，OCP實測28.8A.

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675
L	0.75

5VDIMM
R99
100KR0402
DDR_PWRGD

5VDIMM
R174
5.1R1%/4
C164
1u6.3X/4
[35,37] DDR_PWRGD
2V
R178 280K1%/4
Rd(on)=5.1m, OCP:27.45A
[33] VPP_VR_PG
[6,20,31,32,35,37] SLP_S3#
VCC_DDR
C162 C3300p50X/4
VTT_DDR
C153 10u6.3X/6
C157 10u6.3X/6
U26
VID
VDD
CS
PGOOD
S5
S3
VDDQ
VLDOIN
VTTREF
VTT
VTTSNS
VTTGND
VTT LDO
RT8231AGQW
TON
UGATE
BOOT
PHASE
LGATE
FB
PGND
GND
PGND-1
f:400KHz
R180 620K1%/4
DDR_UG1
DDR_BOOT1
DDR_PH1
DDR_LG1
DDR_FB
FB:0.75V
CP21
X_COPPER
DDR_OV
[41] DDR_OV
I32-8231A0C-R11

5VDIMM
By layout modify
CHOKE16
CH-0.22u8A9m
C95 1u6.3X/4
C179 X_1u6.3X/4
EC6 CD560M6.3SC-HF-5
C136 C0.1u16X0402
C107 C22u6.3X/6
C115 C22u6.3X/6
C1538 C22u6.3X/6
5VDIMM_IN
OCP:27.5A
Imax: 20.85A

2019/4/11
EC5 is deleted ;C115 is stuffed, C1538 is stuffed by Ryan's comment

2019/4/30
EC6 is changed to C71-56106K1-AO5 by PM spec updated

VCC_DDR
R249 10R1%/4 close to DIMM side
R195 1K1%/4
R63 0R/4
VDDIO_MEM_S3_SENSE+ [6]
C165 X_68p10N/4
R181 1.62KR1%0402
C167 X_C0.1u16X0402
Default = 1.21V

2019/4/17
R181 is changed from 1.24kohm to 1.62Kohm by same as 400 series from Ryan's comment

[6,31,35,36,37] APU_AM4R1
D11 S-LRB520S-40T1G
VPP_VR_PG

Close to PIN19
VCC_DDR
C441 10u6.3X/6

ATX_5VSB
R202 47K/4
Q26 NN-2N7002DW
G2 D2 VPP_VR_PG
D1
[6,20,31,33,45] SLP_S5# G1 S2
S1

5VDIMM_IN
20181031
VCC_DDR由上2下2改成上1下1.
DDR_UG1
DDR_BOOT1
DDR_PH1
DDR_LG1
Q107
N-SM4337NSKPC-TRG_DFN5x6-8-HF
D03-4337N0C-ST8
C139 C0.1u25X0402-HF
Q111
N-SM4503NHKPC-TRG_DFN5x6-8-HF
D03-4503N0C-ST8
R149 X_1R1%
C138 X_C3300p50X/4
CHOKE9
CH-1.1u32A1.8m
EC18 CD560M6.3SC-HF-5
EC19 CD560M6.3SC-HF-5
C851 C0.1u16X0402
VCC_DDR
Imax:20.85A
1.2V

0.1uFx1 per dimm
VTT_DDR
C242 X_C0.1u16X0402
C253 X_C0.1u16X0402
VCC_DDR
C263
VTT_DDR
C0.22u16X0402-HF

UPI VOLTAGE CONSOLE
0x26:RH=18K,RL=13K

2019/4/30
EC18, EC19 are changed to C71-56106K1-AO5 by PM spec updated.

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MICRO-STAR INT'L CO.,LTD.
Title: DDR Power-RT8231AGQW
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FOR CPU 1.8V S5

0.5A

FOR VCCP_SOC_S5

0.9A

0.5A + 2.0A +
0.9A =3.4A

CPU 1P8V S5

CPU: VDD_18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A

CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A

2019/4/12
L19, R479, R469, C423, C394 are deleted; R451 is changed from 2.2Kohm to 10Kohm; R445 is unstuffed; R472 is unstuffed; R1503, C1544, C1545, C1546, R1505 C1983 are added; U42 is changed to MP2329; R1504, R1508, C1551 are reseverd; C387 is changed from 0.1uF to 22uF by Ryan's comment

Input Current=
(2.75A*1.8V)/5V/0.8=1.2375A

5VDUAL
C1983 C434
C430
C0.1u16X0402

CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

Imax:4.7A

U42
MP2329CGG-Z_QFN11-HF
VIN, SW, BST, EN, PG, FB, VCC, AGND, PGND-1, PGND-2, PGND-3

C1545 0.22u16X4
L17 CH-1.0u7A11mS-HF
R1504 X_887KR1%0402-HF
R1505 499R1%/4
C1546 C220p50X0402-HH
R448 1K1%/4
R449 487R1%/4
R472 X_47K/4
R1503 100KR0402
C1544 1u6.3X/4
C372 C377 C387 C419 C0.1u16X0402

CPU_1P8_S5_EN
[37,41] CPU_1P8_S5_PG
VFB=0.6V
VCC=3.65V

[6,31,34,36,37] APU_AM4R1 D21 S-LRB520S-40T1G CPU_1P8_S5_EN

CP8 X_COPPER CPU_1P8_S5_FB_R [41]

Vfb:
=10uA(sinking)*1KR=10mV

Vout = Vref * (1 +(R364/R363))
= 0.6 * (1 +(1K/0.487K))
= 1.83V OK

3VSB
R451 10K/4
ENABLE HIGH:1.4V
ENABLE HIGH:1.6V
CPU_1P8_S5_EN
R445 X_3.3K1%/4
C400 C0.1u16X0402

2019/4/18
Q82 is deleted by Ryan's comment

CPU_1P8_PHASE R1508 X_1R1% C1551 X_2700p50N4
reserve snubber

FOR CPU 1.8V S0

2.0A

ATX_5VSB
R379 47K/4
C352 X_1u6.3X/4
Q77 NN-2N7002DW
[6,20,31,32,34,37] SLP_S3#
[34,37] DDR_PWRGD

Q89 NN-2N7002DW
[36] CPU_VDDP_EN
VCC3
R389 10K/4
CPU_1P8_EN
C357 C0.1u16X0402

DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8

CPU_1P8_S5
U33 TPS22976DPUR
C1514 C22u6.3X/6
C1515 X_C22u6.3X/6
CPU_1P8_EN
VCC3
C1516 C0.1u16X0402
C342 C4700p50X0402

Imax:2A

CPU_1P8
C1517 X_C22u6.3X/6
C339 X_C22u6.3X/6
C332 1u6.3X/4

Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)

MICRO-STAR INT'L CO.,LTD.

Title: CPU Power 1P8V-MP2147

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CPU_VDDP

CPU: VDDP@8.5A

Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A

L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH

Isat: 22A

0.9V@8.5A
OCP=13A Imax:8.5A

CPU_VDDP need to confirm 1.05V

L04-47B7930-M26

Internal 3.3V Input

VFB=0.6V

R823、R344、C822 stuff for stability

2019/4/25
CHOKE13 is changed to L04-68B7350-T15
by Ryan's comment

20180822
fix PG glitch when VCC3 ramp up, C386 stuff.

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

Vout=Vref*(1/[R450*(1/R438+1/R1492)]+1}
=0.6*{1/[1.33k*(1/1k+1/1m)]+1}
=1.0506v

CPU_VDDP_S5

CPU: VDDP_S5@1A

2019/4/18
Q98 is deleted by Ryan's comment

2019/4/16
R490, C436, Q95, R464 are unstuffed by Ryan's comment

Imax:1A
0.9V@1A

0.9W

AM4_CPU_SEL
0:Type 0/1
1:Type 2/3

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

Vout = Vref * (1+R489/R488)
= 0.8 * (1+1K/3.16K)
= 1.053v

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Title	CPU Power VDDP-RT8125E
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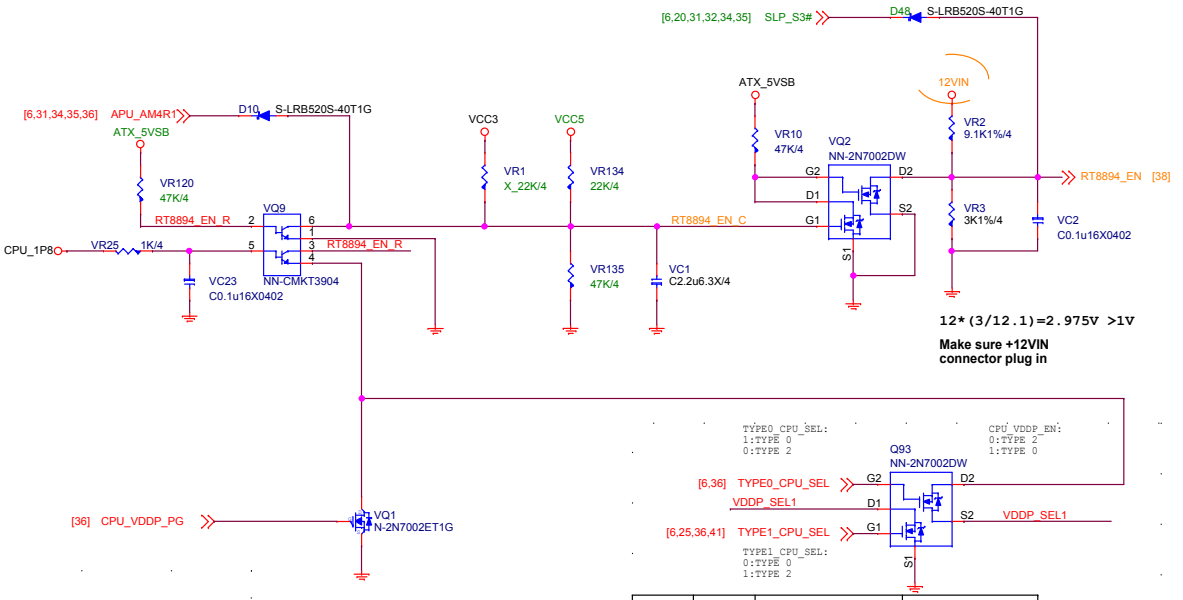
MICRO-STAR INT'L CO.,LTD.

VRM_Enable circuit

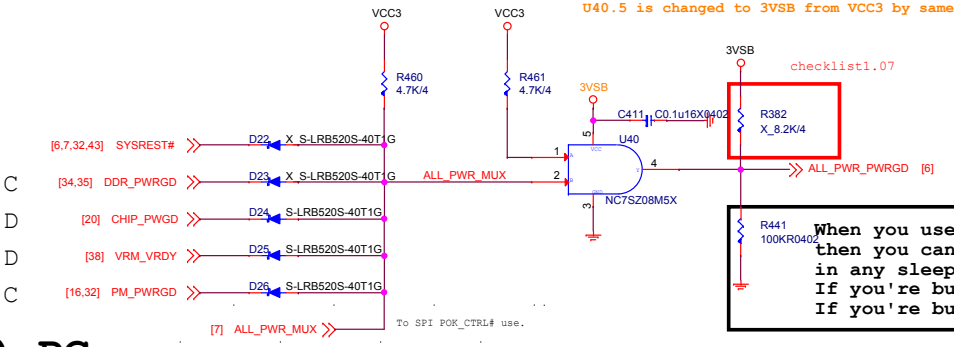


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

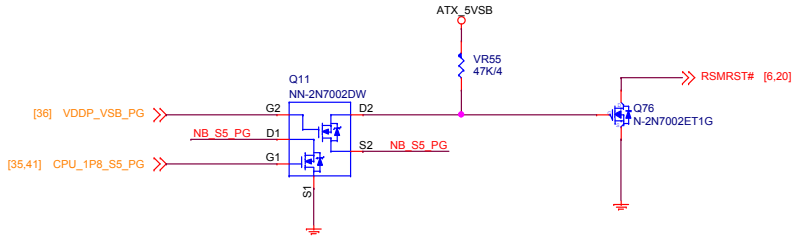
2019/4/9
U40.5 is changed to 3VSB from VCC3 by same as X570.



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



2019/5/20
Q11.G2 and Q11.G1 are swapped by Ryan's comment

MICRO-STAR INT'L CO.,LTD.

Title: CPU PWR-IR3599

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Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

2019/4/10
VRM solution passed to follow up PM spec
2019/4/12
VR15, VR12, VR29, VR24, VR36, VR57, VR33, VR41, VR46, VR47, VR84, VR63, VR73 are changed to 0ohm to short copper; VC28, VC29 are unstuffed by vendor's suggestion
2019/4/25
VR34 is changed to 46.4Kohm; VR32 is changed to 620ohm; VC10 is changed to 150pF, VC24 is changed to 47pF; VR44 is changed to 39Kohm; VR45 is changed to 6.04Kohm; VC16 is changed to 220pF; VR85 is changed to 910ohm; VR64 is changed to 1.62Kohm; VR80 is changed to 910ohm; VR79 is changed to 1.62Kohm; VR82 is changed to 10.7Kohm; VR66 is changed to 280ohm; VR70 is changed to 14Kohm; VR71 is changed to 110ohm; VR83 is changed to 2.26Kohm; VR81 is changed to 100ohm; VR16, VR60 are changed to 110Kohm; VR76 is changed to 60.4Kohm; VR121 is changed to 2.1Kohm; VR78 is changed to 22.1Kohm; VR122 is changed to 133ohm; VR137 is added to 316ohm; VR69 is changed to 2Kohm; VR138 is added to 191ohm; VR65 is changed to 22.6Kohm; VR68 is changed to 200ohm; VR74 is changed to 16Kohm; VR75 is changed to 3.48Kohm; VR72 is changed to 9,53Kohm; VR73 is changed to 10ohm by Vendor's suggestion.

2019/4/18
VC3, VC27 are changed from 1uF/6.3V to 1uF/16V; VC5 is changed from 0603 type to 0402 type by "PN_190325" rule

2019/5/8
VR21 is changed to 100ohm to short copper by cost reduction.

2019/5/8
VR36, VR41 are deleted by cost reduction

2019/5/8
VR59, VR42, VR37, VR40 are changed to 0ohm to short copper by cost reduction.

2019/5/8
VR86 is unstuffed by Ryan's comment

RT8894A

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation

SMB Address: 0X40

VCORE IccMAX: 125A =>OCP=>140A
VCC_NB IccMAX: 75A =>OCP=> 90A

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Title	MSI MICRO-STAR INT'L CO.,LTD. CPU Power RT8894 3+2 Phase		
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VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

2019/4/10
VRM passed to follow up PM spec

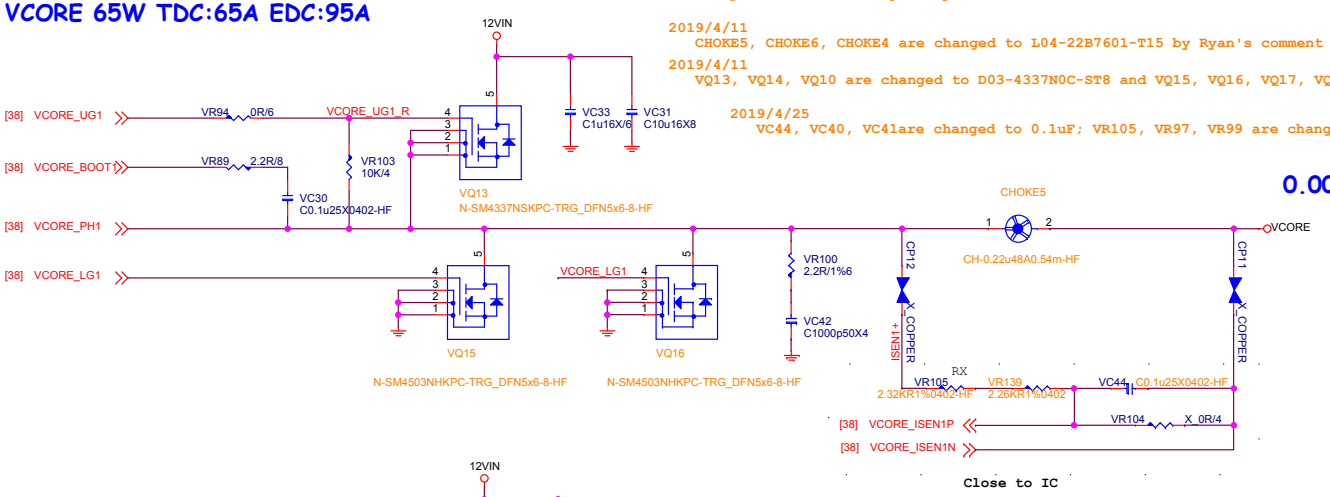
2019/4/11
CHOKE5, CHOKE6, CHOKE4 are changed to L04-22B7601-T15 by Ryan's comment

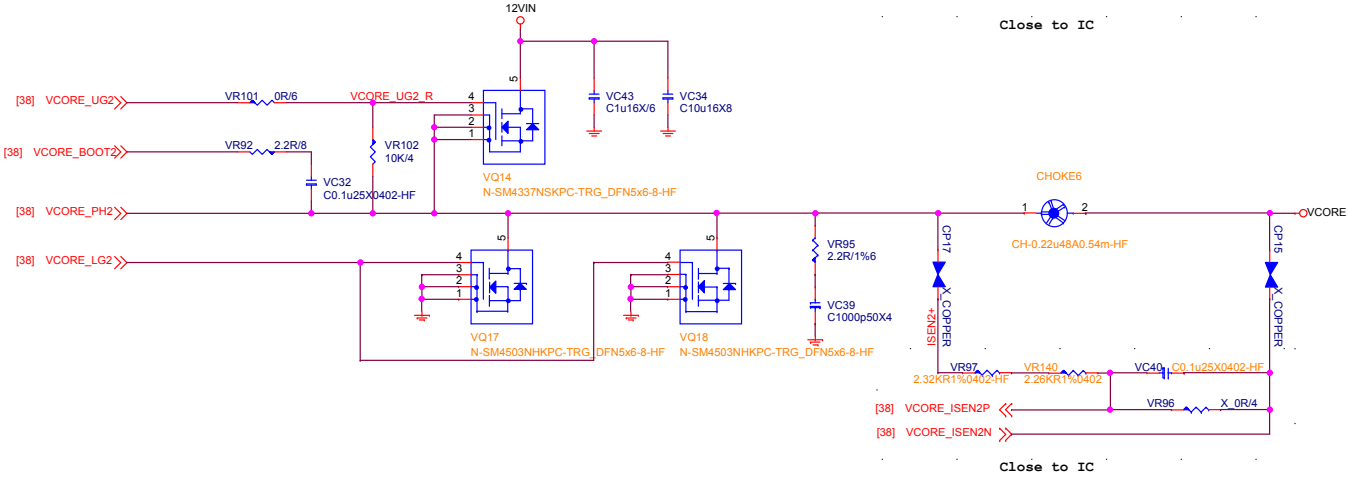
2019/4/11
VQ13, VQ14, VQ10 are changed to D03-4337N0C-ST8 and VQ15, VQ16, VQ17, VQ18, VQ11, VQ12 are changed to D03-4503N0C-ST8 by Ryan's comment(same as 7A36-3.0)

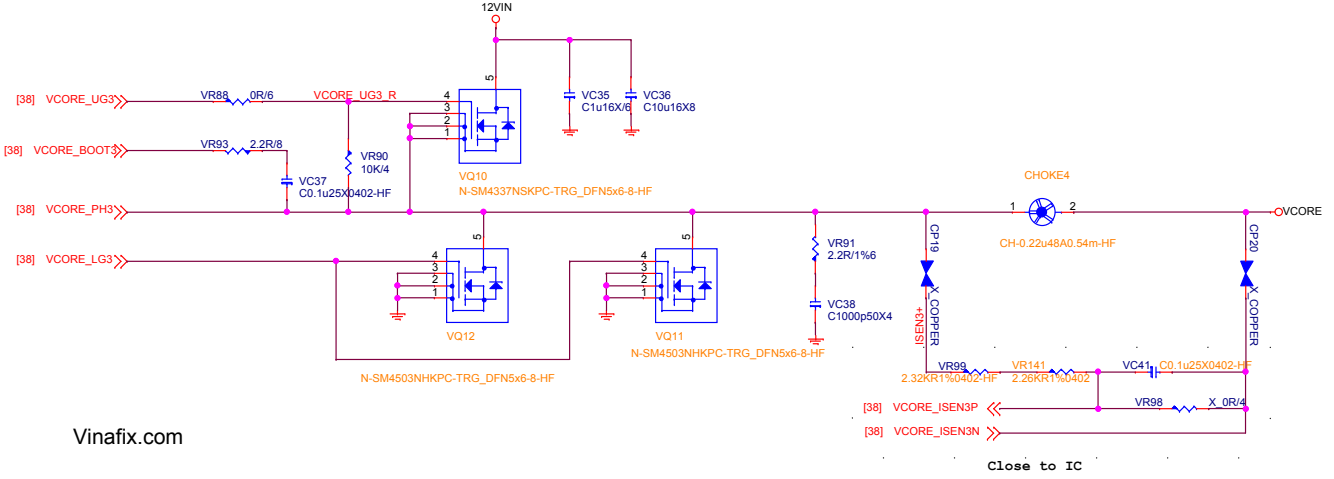
2019/4/25
VC44, VC40, VC41are changed to 0.1uF; VR105, VR97, VR99 are changed to 2.32Kohm; VR139, VR140, VR141 are added to 2.26Kohm by vendor's suggestion

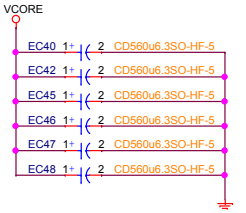
0.00625V~1.55V

Imax:125A









2019/4/30
EC40, EC42, EC45, EC46, EC47, EC48 are changed to C71-56106K1-AO5 by PM spec updated

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MICRO-STAR INT'L CO.,LTD.

Title: CPU Power Phase 1-3

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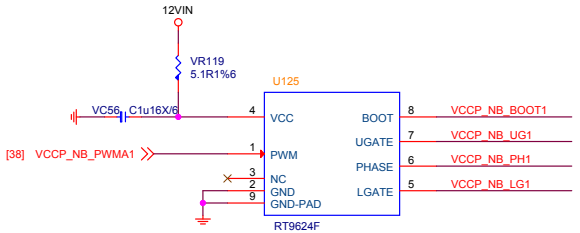
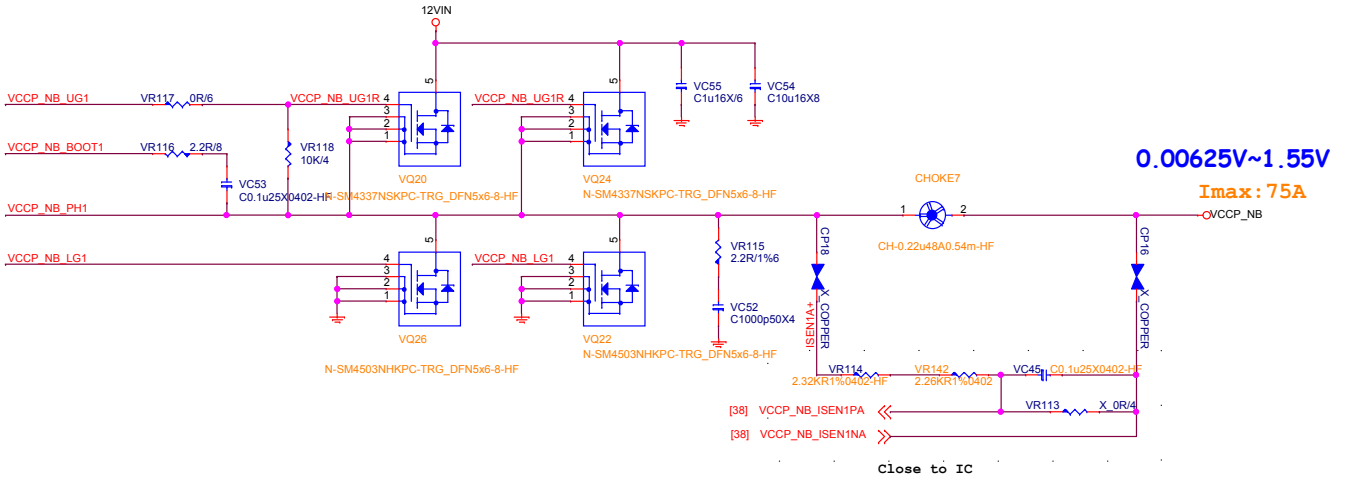
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

2019/4/10
VRM passed to follow up PM spec

2019/4/11
CHOKE7, CHOKE8 are changed to L04-22B7601-T15 by Ryan's comment

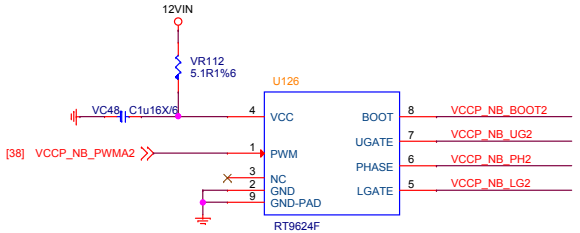
2019/4/11
VQ20, VQ24, VQ21, VQ25 are changed to D03-4337N0C-ST8 and VQ22, VQ26, VQ19, VQ23 are changed to D03-4503N0C-ST8 by Ryan's comment(same as 7A36-3.0)

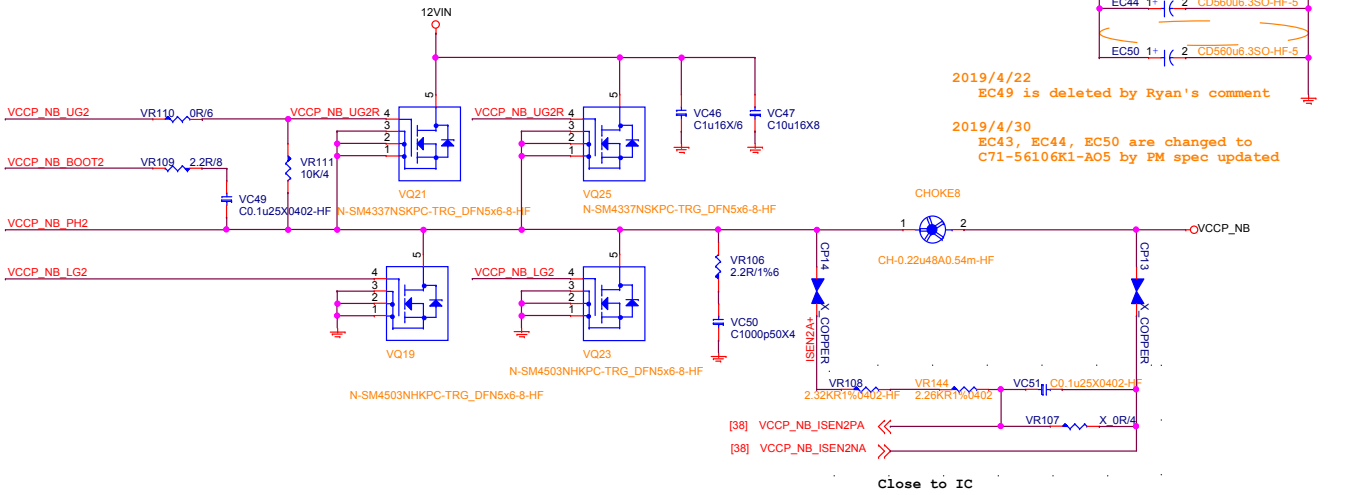


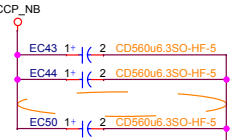


0.00625V~1.55V
Imax:75A

2019/4/25
VC45, VC51 are changed to 0.1uF; VR114, VR108 are changed to 2.32Kohm; VR142, VR144 are added to 2.26Kohm by vendor's suggestion







2019/4/22
EC49 is deleted by Ryan's comment

2019/4/30
EC43, EC44, EC50 are changed to C71-56106K1-A05 by PM spec updated

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MICRO-STAR INT'L CO.,LTD.

Title	CPU Power NB Phase 1-2	
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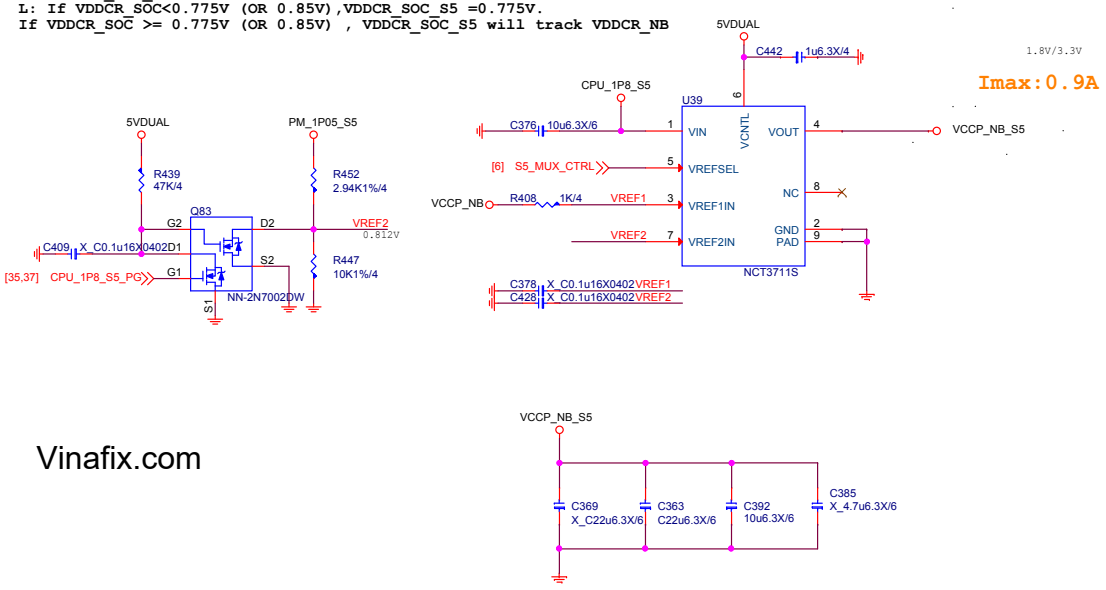
FOR VCCP_SOC_s5
0.9A

TYPE0 Only

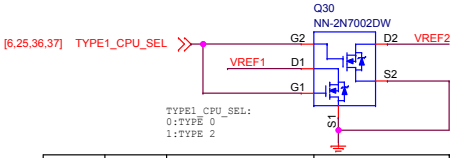
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)Bristol Ridge TYPE0



Vinafix.com



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

2019/4/23
U62, R616, R614 are deleted by Ryan's comment

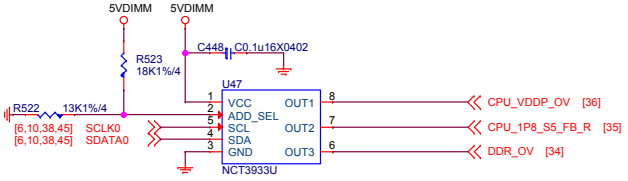
除非超壓對功能有任何幫助,否則不上NCT3933與開超壓選項

2019/4/11
U64, C570, R618, R621 are deleted by Ryan's comment

0x26:RH=18K,RL=13K

0x20:RH=10K,RL=OPEN

0x2A:RH=OPEN,RL=10K



Vinafix.com

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

MICRO-STAR INT'L CO.,LTD.

Title: CPU Power NB Sw/NCT3933 OV

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uP6273 CURRENT SENSE

20181107
cost down-remove 12VIN OCP

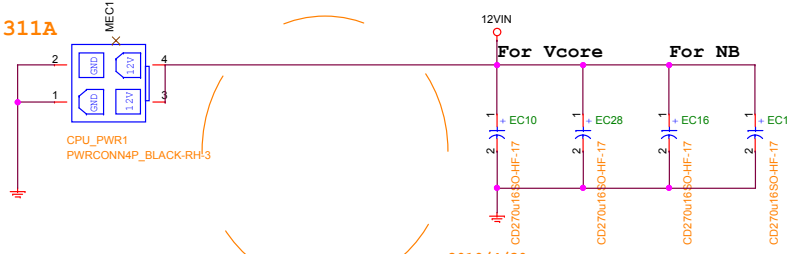
2019/4/11
R1083, R1080, C973, R1079, U101, C914, C915, R1060, C919, C916, R1071, R1072, C917, C918, R1066, R43, Q6, Q12, R61 are deleted by Ryan's comment

VCORE EDC MAX 125A
NB EDC MAX75A

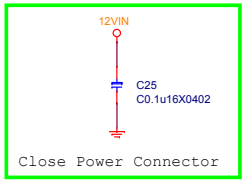
CPU POWER CONNECTOR

2019/4/11
CPU_PWR1 is changed to N93-04M0441-H06 by PM spec.
2019/4/11
CHOKE1, SP1, SP2 are deleted by Ryan's comment

Imax:27.311A



2019/4/30
EC1, EC10, EC16, EC28 are changed to C71-27117Y1-A05 by PM spec updated.



Vinafix.com

Irms = Iout * SQRT{D/N- (D)^2]}

CORE:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=3
=125A*SQRT(0.0388-0.0136)
=19.8A

NB:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=2
=75A*SQRT(0.0583-0.0136)
=15.8A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.5	> output Vcore
D	=	0.125	

I o = Icore(max)*0.8			
I core(max)	=	125	> Vcore current
I avg.	=	100	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	3	phase
I ripple	=	11.02396	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	3	pcs.

For Vcore

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.2	> output Vcore
D	=	0.1	

I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	9	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

For NB

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Title: CPU PWR CONN

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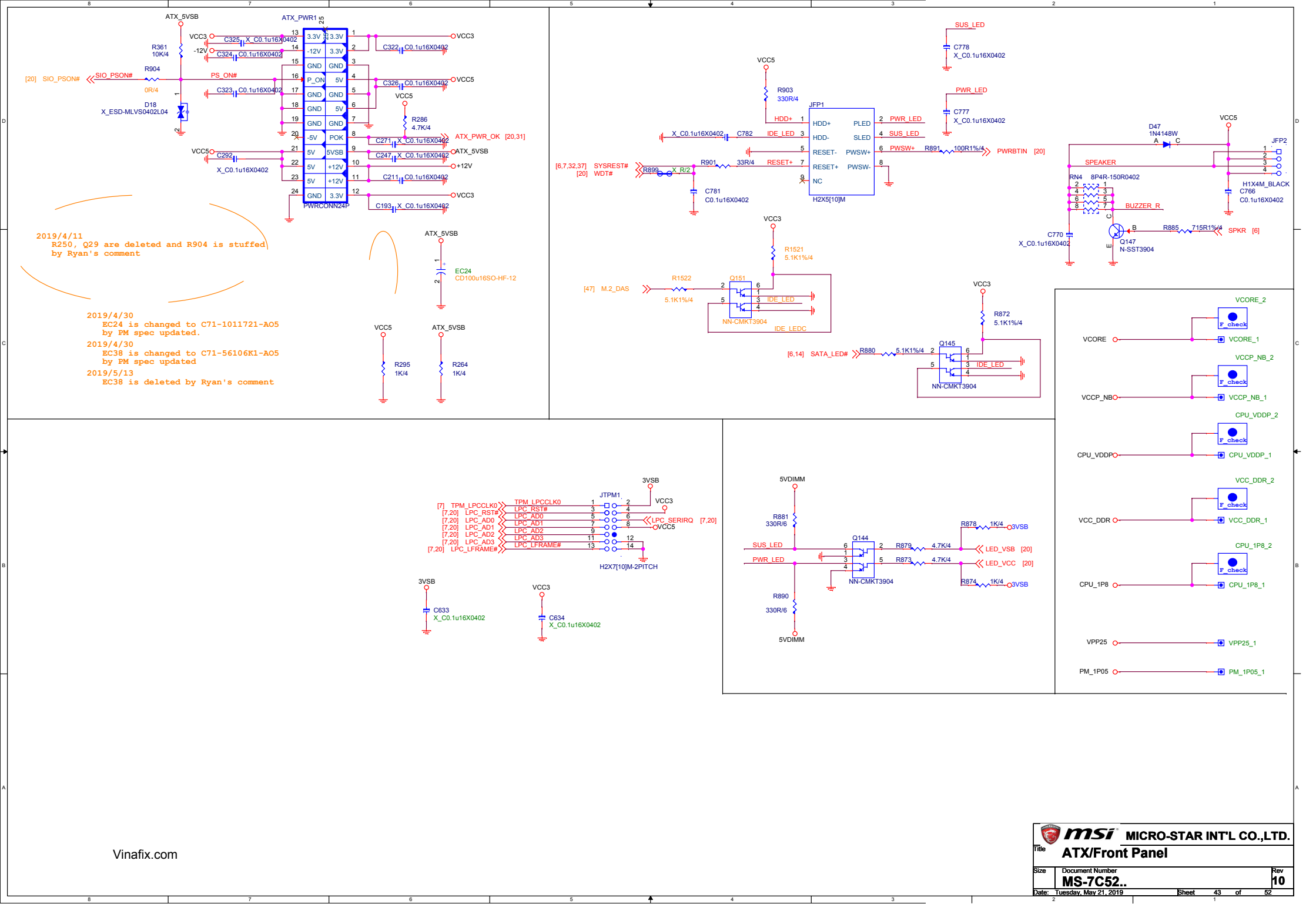

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Title: ATX/Front Panel

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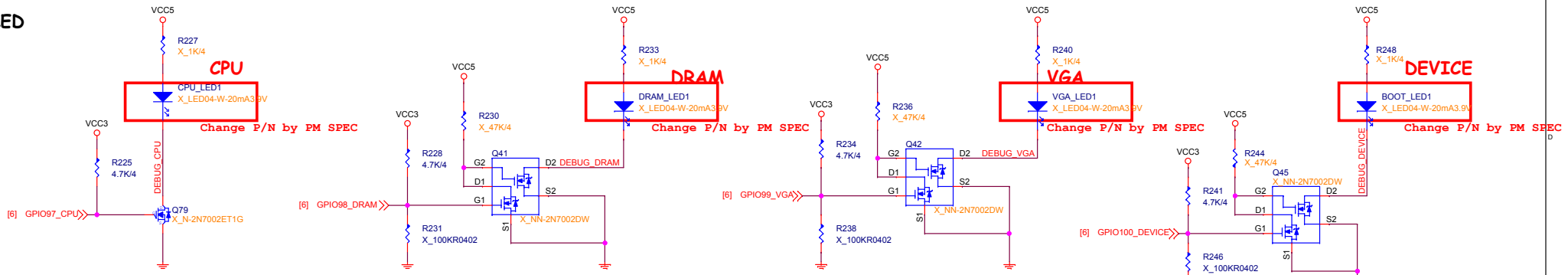
EZ Debug LED



LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

2019/5/2
R227, CPU_LED1, Q79, R223, DRAM_LED1, Q41, R230, R240, VGA_LED1, Q42, R236, R248, BOOT_LED1, Q45, R244 are unstuffed by PM spec updated.

LED Control by SIO

1.0 SPEC Removed

DDR LED

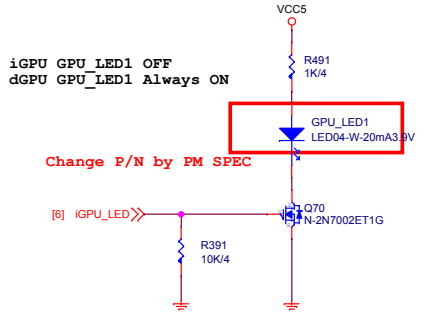
Removed P/N by PM SPEC

PCI Express LED Control

Removed P/N by PM SPEC

LED	x16	x8	x4
PCIE2	Red	White	White

AM4 APU Detect LED Circuit



Bottom LED

Removed P/N by PM SPEC

LED \ GPIO	EGPIO95	EGPIO96
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

MICRO-STAR INT'L CO.,LTD.

Title: ALL LED Control

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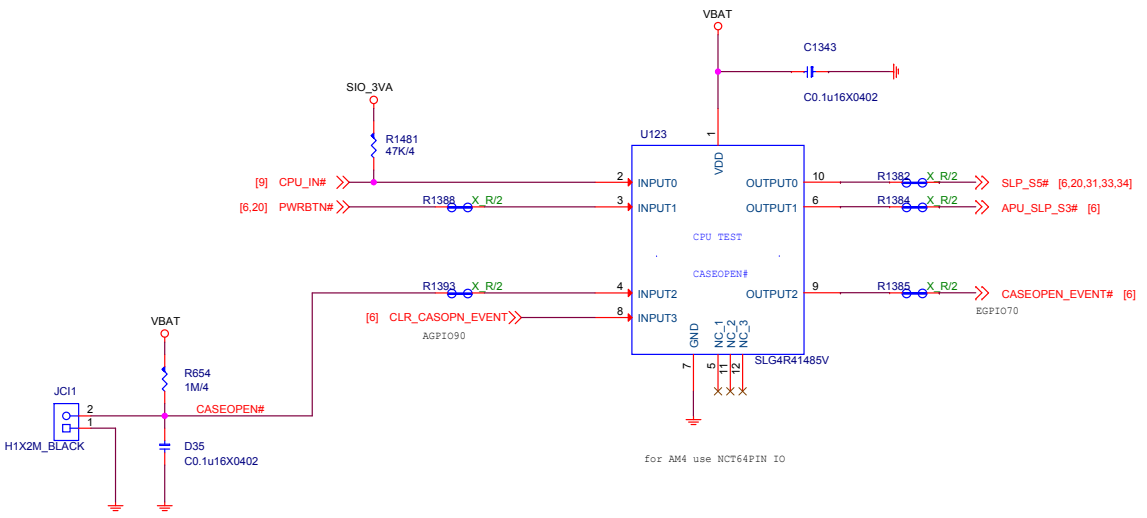
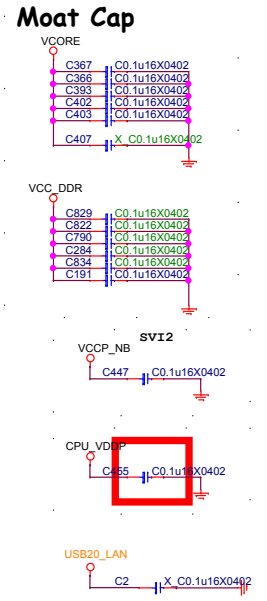
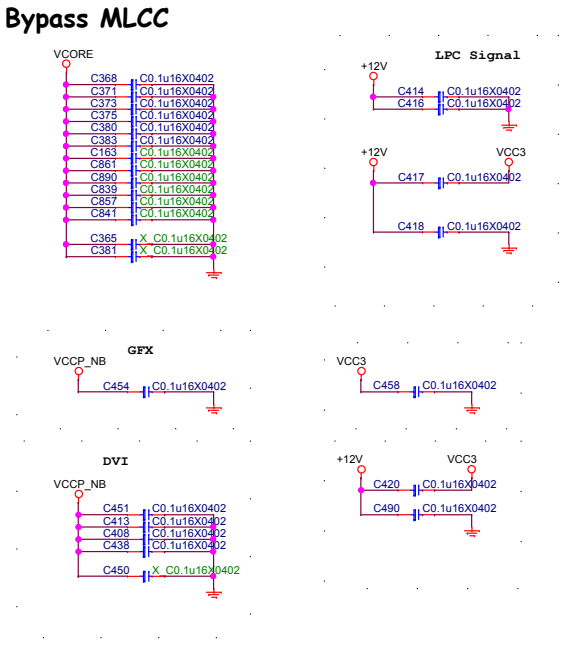
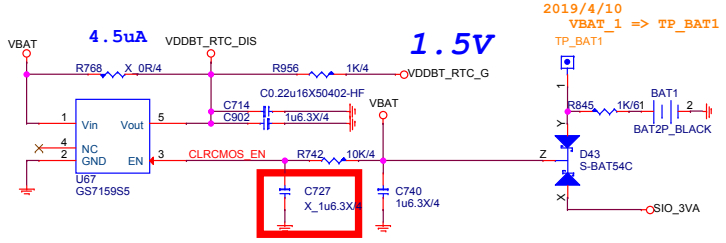


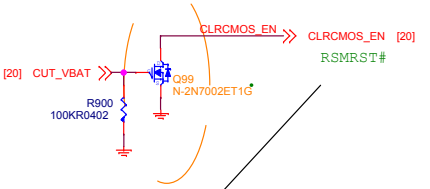


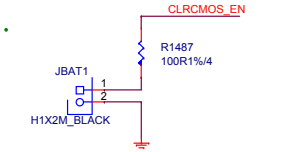


RTC & Clear CMOS Circuit

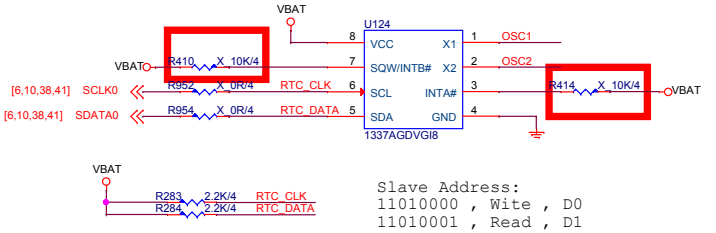


2019/4/11
Q99 is changed to D03-7002E89-005 and R960, R25, C744 are deleted by Ryan's comment

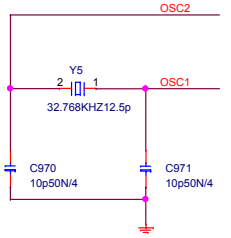


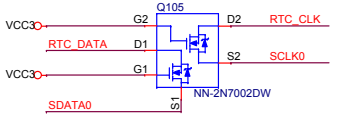


20181029
update to G3 clean CMOS.



Slave Address:
11010000 , Wite , D0
11010001 , Read , D1





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MICRO-STAR INT'L CO.,LTD.

Title	RTC Circuit	
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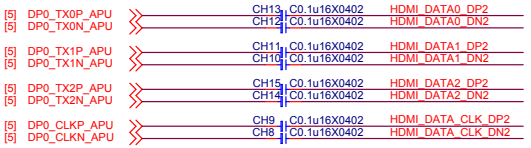
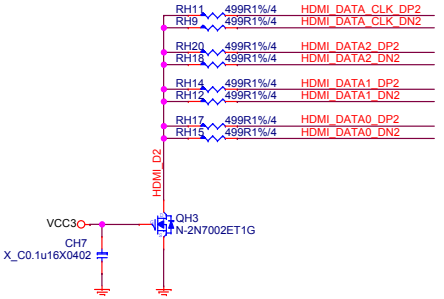
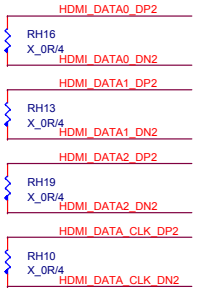
HDMI CONNECTOR

For HDMI 1.4

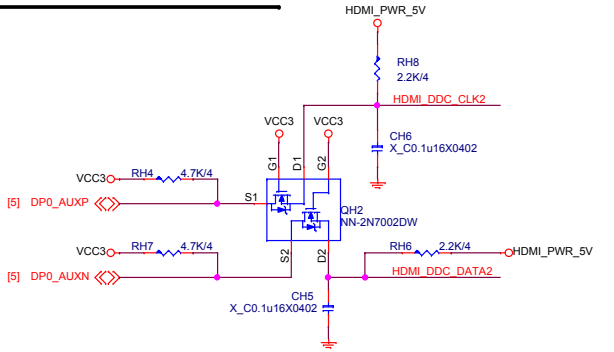
2019/4/10
HDMI is added by PM spec.



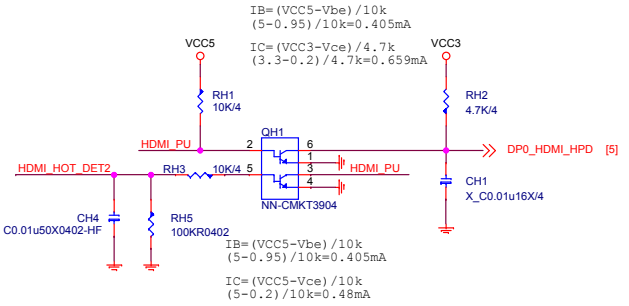




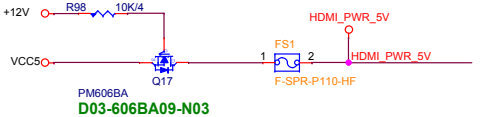
AUX Level Shifter



HPD Circuit



Connector Power

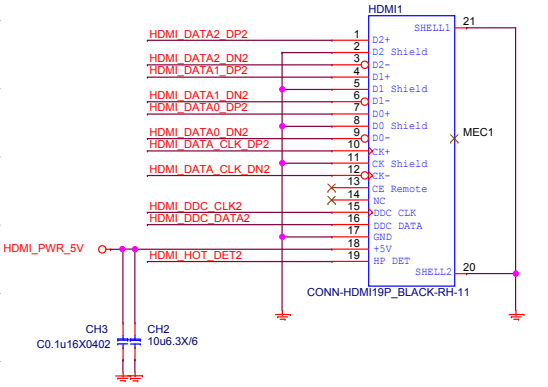


D03-606BA09-N03

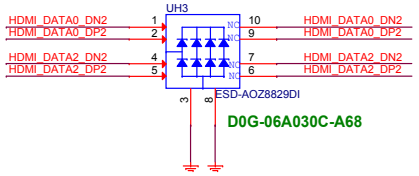
如果用DIODE SA測試電壓會不過

2019/5/6
FS1 is changed to D08-0101700-P16 by Ivy's comment

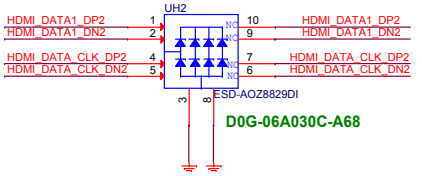
Connector



For EMI

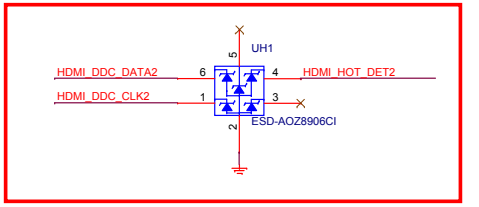


D0G-06A030C-A68



D0G-06A030C-A68

20170426



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Title: HDMI Connector

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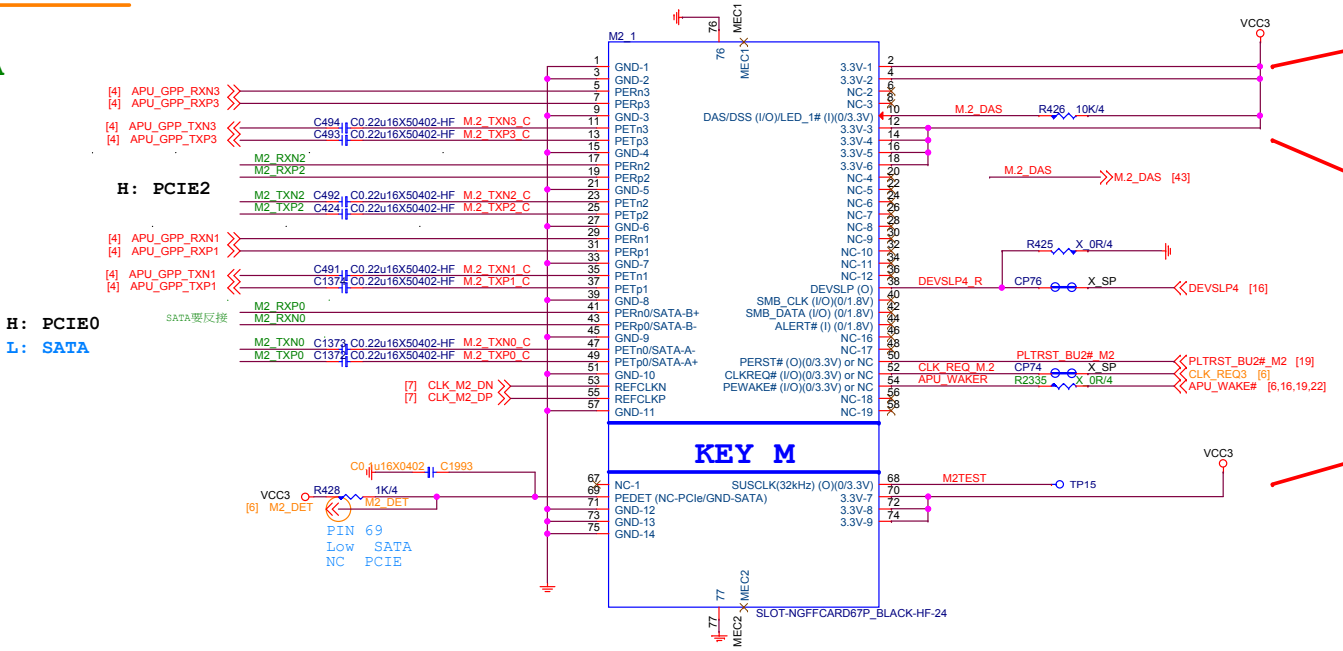
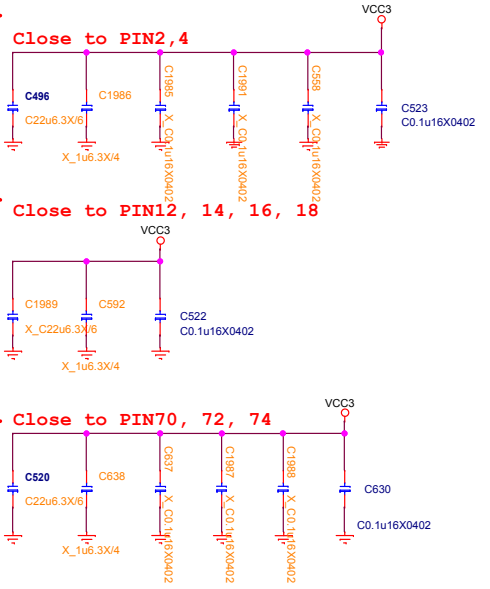
M.2 Connector

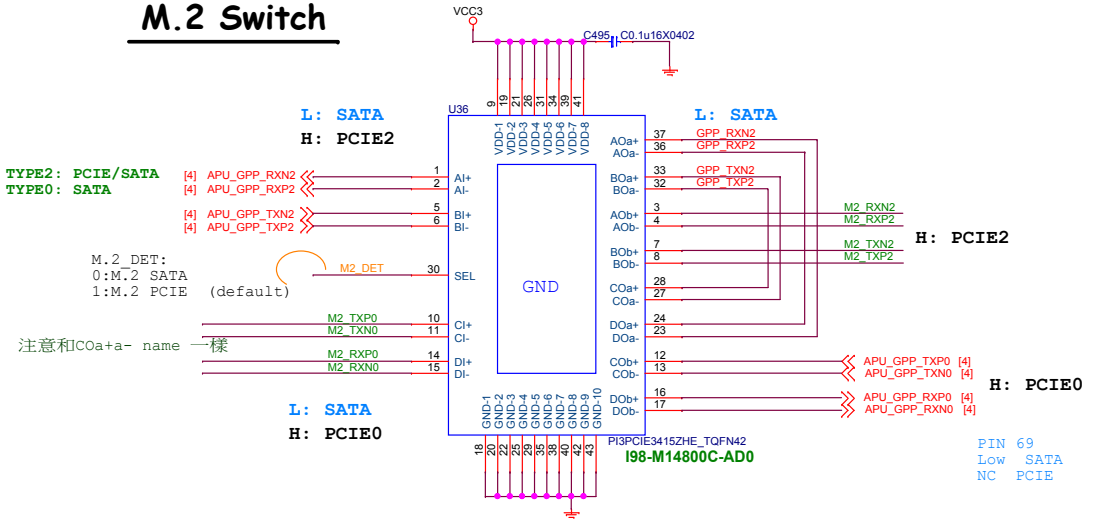
3.3V@2.5A

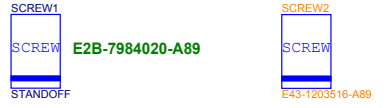


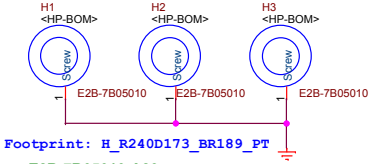


2019/5/21
SCREW2 is add by PM request

M.2 Switch







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Title	M2	
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HEAT SINK

OK

PM_HS1

MEC1

MEC2

HS-0408690

2019/4/30
B450 SKU is added by PM spec updated

B450

X_AMD-218-0891011-RH

B450_1UF_5020

X_1u6.3X/4

CPU Socket

CPU2

E95-0000022-C22

E95-0000022-C22

Simulation

X_JS3

SIM1

X_PIN1*2

X_JS4

SIM2

X_PIN1*2

2019/5/8
SPI_32 is added by PM spec updated

SPI_32

X_W25Q256JWEIQT-HF

2019/5/8
DVI1 is added by PM spec updated

DVI1

X_DVI24P_BLACK-RH-19

MANUAL PART

OK

UEFI1

G51-M1SPXXA-A09

BAT1_X1

BAT-BCR2032P

2019/5/21
MKT1, MKT2, MKT3 are modified by PM updated

MKT1

G51-M1SPP43-Q13

MKT2

X_G51-M1SPP42-Q13

MKT3

X_G51-M1SPP44-Q13

PCB1

PK0-07C5210-G37

PK0-07C5210-G37,精成
AVL PK0-07C5210-E48,競華

2019/4/26
The pin1 of MH4, MH6, MH1, MH2 are changed to GND by CND rule

Optics Orientation Holes

MH4

X_MH001

MH6

X_MH001

MH1

X_MH001

MH2

X_MH001

5010

FM3 X_FM120

FM2 X_FM120

FM8 X_FM120

FM6 X_FM120

5020

FM1 X_FM120

FM4 X_FM120

FM7 X_FM120

FM5 X_FM120

OPT	Configure	BOM	Function

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Title: BOM OPTION

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