MS-7C52 Ver:1.1

CPU:
AMD AM4

System Chipset:
Promontory A320 / B450
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

VRM
RT8894 3+2

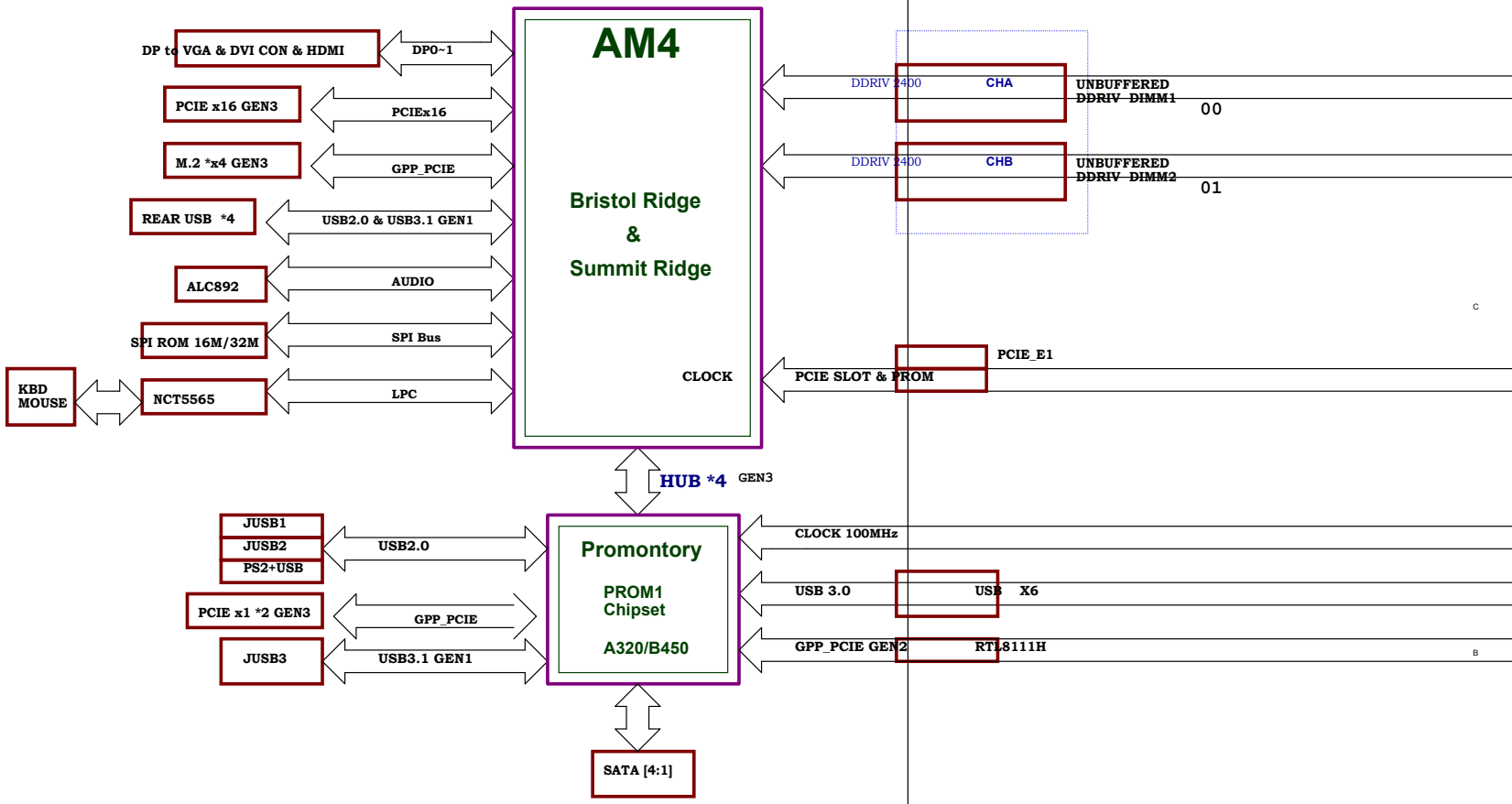
On Board Chipset:
LPC Super I/O --NCT5565
LAN RTL8111H
Azalia CODEC - Realtek ALC892

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1

M.2 Slot * 1

OCP IC:
UP6273

FUSION BLOCK DIAGRAM



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Title: Block Diagram

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AMD AM4

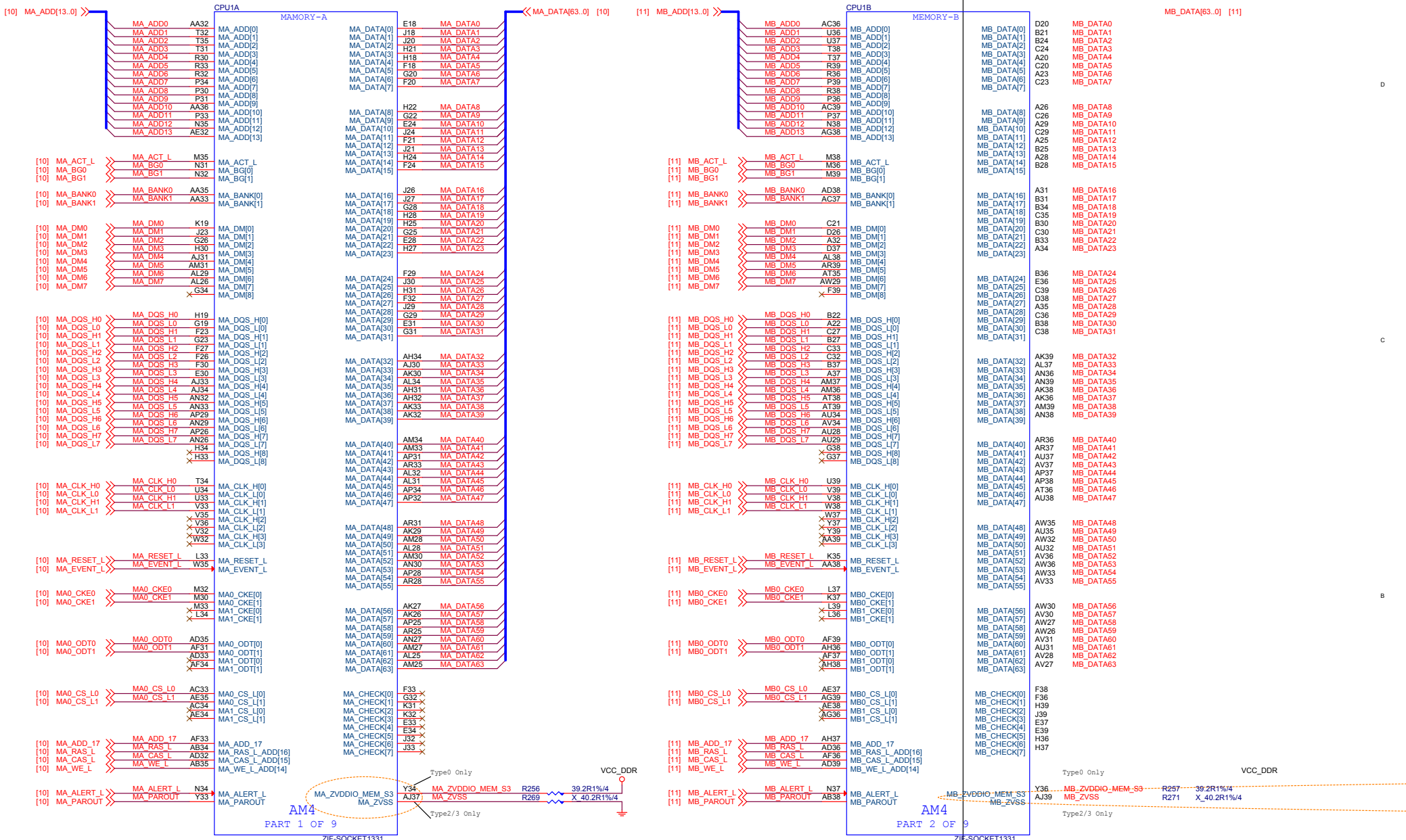

Table 6. DRAM Memory Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
MA_ZVDDIO_MEM_S3, MB_ZVDDIO_MEM_S3	A	Compensation Resistor to VDDIO_MEM_S	X				
MA_ZVSS, MB_ZVSS	A	DRAM Compensation Resistor to VSS		X	X	X	X

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Title: AM4 DDR4 I/F

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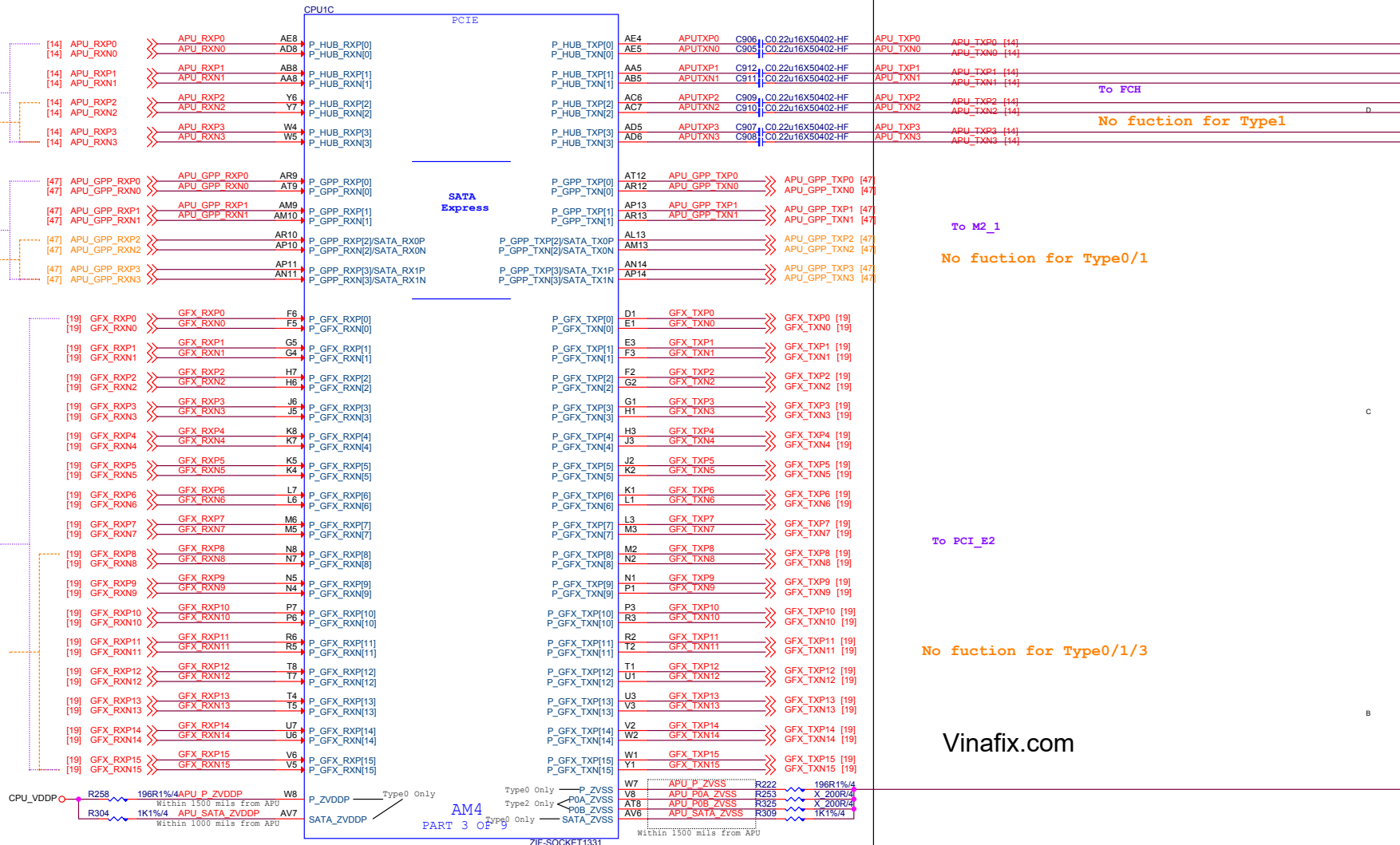

Table 3. PCI Express® Interface Pin Descriptions

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
P_GFX_RXP[3:0], P_GFX_RXN[3:0]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_GFX_RXP[7:4], P_GFX_RXN[7:4]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs	X		X	X	X
P_GFX_TXP[3:0], P_GFX_TXN[3:0]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_GFX_TXP[7:4], P_GFX_TXN[7:4]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs	X		X	X	X
P_GFX_RXP[15:8], P_GFX_RXN[15:8]	I-PCIe-D	External Graphics PCIe® Receive Data Differential Pairs			X		X
P_GFX_TXP[15:8], P_GFX_RXN[15:8]	O-PCIe-D	External Graphics PCIe® Transmit Data Differential Pairs			X		X
P_GPP_RXP[1:0], P_GPP_RXN[1:0]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_GPP_TXP[1:0], P_GPP_TXN[1:0]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_GPP_RXP[2]/SATA_RX0P, P_GPP_RXN[2]/SATA_RX0N	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs			X	X	X
P_GPP_TXP[2]/SATA_TX0P, P_GPP_TXN[2]/SATA_TX0N	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs			X	X	X
P_GPP_RXP[3]/SATA_RX1P, P_GPP_RXN[3]/SATA_RX1N	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs			X	X	X
P_GPP_TXP[3]/SATA_TX1P, P_GPP_TXN[3]/SATA_TX1N	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs			X	X	X
P_HUB_RXP[1:0], P_HUB_RXN[1:0]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X	X	X	X	X
P_HUB_RXP[3:2], P_HUB_RXN[3:2]	I-PCIe-D	General Purpose External PCIe® Receive Data Differential Pairs	X		X	X	X
P_HUB_TXP[1:0], P_HUB_TXN[1:0]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X	X	X	X	X
P_HUB_TXP[3:2], P_HUB_TXN[3:2]	O-PCIe-D	General Purpose External PCIe® Transmit Data Differential Pairs	X		X	X	X
PCIE_RST_L/EGPIO26	O-IO33S5-S	PCI Host Bus Reset. Asserted during transition to S3/S5.	X	X	X	X	X

Table 3. PCI Express® Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
P0A_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive			X		X
P0B_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive			X		X
P_ZVDDP	A	Compensation Resistor to VDDP	X				
P_ZVSS	A	Compensation Resistor to VSS / PCIe® Calibration Positive	X				

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Title: AM4 PCIE/SATAE

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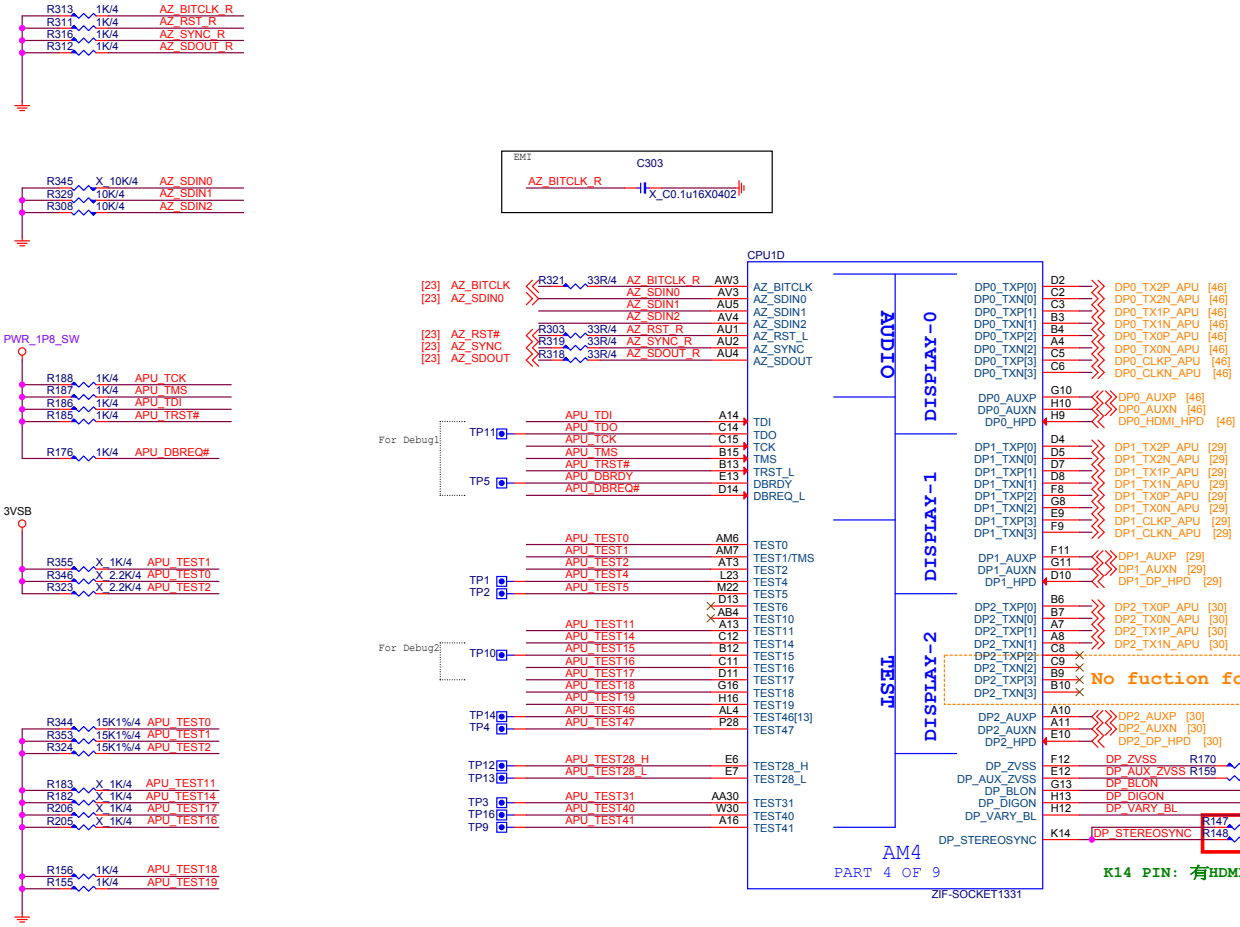
Table 4. Digital Display Interface (DDI) Pin Descriptions

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
DP0_TXP[3:0], DP0_TXN[3:0] DP1_TXP[3:0], DP1_TXN[3:0] DP2_TXP[1:0], DP2_TXN[1:0]	O-PCIe-D	DisplayPort Differential Transmitter	X	X		X	
DP2_TXP[3:2], DP2_TXN[3:2]	O-PCIe-D	DisplayPort Differential Transmitter	X			X	
DP0_AUXP, DP0_AUXN DP1_AUXP, DP1_AUXN DP2_AUXP, DP2_AUXN[1]	B-IO18-D	DisplayPort Auxiliary Channel	X	X		X	
DP0_HPD, DP1_HPD, DP2_HPD[2]	I-IO18-S	DisplayPort Hot Plug Detect	X	X		X	
DP_AUX_ZVSS	A	Compensation Resistor to VSS	X				
DP_ZVSS	A	Compensation Resistor to VSS	X				

Notes:

1. *DisplayPort Auxiliary Channel pins are dual-mode pins and are 3.3V tolerant. In I2C mode AUXP pins change to SCL, and AUXN pins change to SDA. During this operation the pin type is B-IO33-OD.*
2. *Hot Plug Detect pins are 3.3V tolerant.*



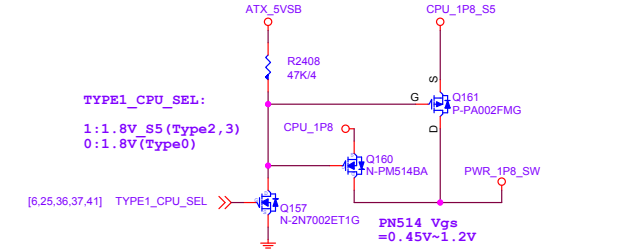


Table 5. LCD Power Interface Pin Descriptions

Signal Name	Type	Description	Processor Types				
			0	1	2	3	4
DP_BLON	O-IO18-S	Display Panel Backlight Enable	X	X		X	
DP_DIGON	O-IO18-S	Display Panel Power Enable	X	X		X	
DP_STEREOSYNC	B-IO18-S	Signal used to drive active shutter glasses for stereoscopic 3D viewing on 120-Hz panels.	X	X		X	
DP_VARY_BL	O-IO18S	Display Backlight Brightness Contro	X	X		X	

MSI MICRO-STAR INT'L CO.,LTD.

Title: AM4 DISPLAY/AUDIO

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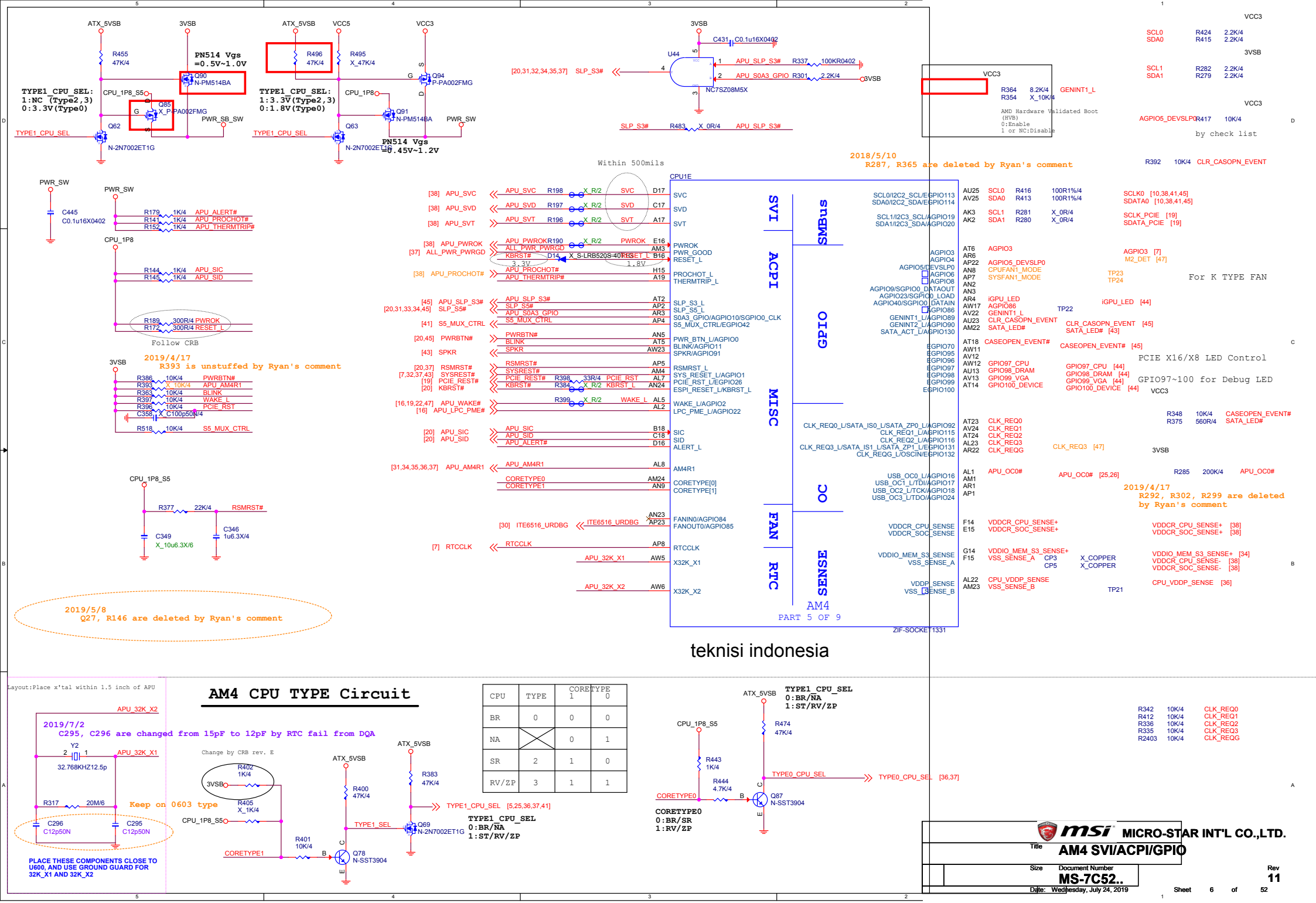

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

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MICRO-STAR INT'L CO.,LTD.

Title: AM4 SVI/ACPI/GPIO

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Strapping Options

2019/5/2
R2387 is added by Ryan's comment

2019/5/14
R349 & R343 passed to follow up PM's spec

	R349	R343
01S	X	●
02S	●	X
03S	●	X

	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled (Default)	Configured for Internal clock generator (Default)	SPI ROM
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ?????	LPC ROM

	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

RTCCLK

R378 10K/4	PULL HIGH	RTC Coin Battery is on board (Default)
R373 X_2K1%/4	PULL LOW	RTC Coin Battery is not on board

[6] RTCCLK

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Table 7. Clock Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types 0	1	2	3	4
GFX_CLKP, GFX_CLKN	O-IOGFX-D	PCIe® Graphic Slot Clock	X	X	X	X	X
GPP_CLK0P, GPP_CLK0N	B-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X		X	
	B-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
GPP_CLK1P, GPP_CLK1N	B-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X		X	
	B-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
GPP_CLK2P, GPP_CLK2N	O-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X		X	
	O-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
GPP_CLK3P, GPP_CLK3N	O-IOVP-D	PCIe® Expansion 100-MHz Reference Clock	X	X		X	
	O-PCIe-D	PCIe® Expansion 100-MHz Reference Clock			X		X
X48M_X1	I-IOVP55-S	48-MHz Crystal Clock 1 **Note:** *Power rail may be tied to S0-S5 or S0-S3.*	X	X	X	X	X
X48M_X2	I-IOVP55-S	48-MHz Crystal Clock 2 **Note:** *Power rail may be tied to S0-S5 or S0-S3.*	X	X	X	X	X
X32K_X1	I-RTC-S	32-kHz Real Time Clock Crystal Oscillator Input 1 **Note:** *Input must be active at all times.*	X	X	X	X	X
X32K_X2	I-RTC-S	32-kHz Real Time Clock Crystal Oscillator Input 2 **Note:** *Input must be active at all times.*	X	X	X	X	X
RTCCLK	O-IO33S5-S	Real Time Clock 32-kHz Output	X				
	O-IO18S5-S	Real Time Clock 32-kHz Output		X	X	X	X

Table 8. USB Interface Pin Descriptions (Continued)

Signal Name	Type	Description	Processor Types 0	1	2	3	4
48M_OSC	B-IO33S5-S	48-MHz USB Clock	X				
	B-IO18S5-S	48-MHz USB Clock		X	X	X	X
USB_ZVSS,	A	USB Compensating Resistor to VSS	X				
USB[3:0]_ZVSS,	A	USB Compensating Resistor to VSS		X	X	X	
USB_SS_ZVSS	A	USB SS Compensation Resistor to VSS	X				
USB_SS_ZVDDP	A	Compensation Resistor to USB SS Power Supply	X				

SPI ROM(1.8V)

2019/5/8
R492, R525 are changed to 0ohm to short copper by cost reduction.

2019/4/11
The footprint of SPI1 is chnaged to SIC8_SST_S2A_COLAY_T by 16M/32M colay by PM spec

SPI CS# < 20pF
D0G-0402510-SI0

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

P.S Close to JSPI1

VDDIO_AUDIO Circuit

2019/4/11
R537, C397, C459, U49, R529, C456, C464, R536, R535, C453 are deleted by Ryan's comment

1.5V
0.25A

TOP SIDE

VCORE

C233	X_C22u6.3X/6
C862	X_C22u6.3X/6
C881	X_C22u6.3X/6
C215	X_C22u6.3X/6
C894	X_C2.2u6.3X/4
C885	X_C2.2u6.3X/4
C872	X_C2.2u6.3X/4
C889	X_C2.2u6.3X/4

VCCP_NB

C830	X_C22u6.3X/6
C199	X_C22u6.3X/6
C826	X_C22u6.3X/6
C203	X_C22u6.3X/6
C828	X_C22u6.3X/6
C827	X_C22u6.3X/6
C84	X_C22u6.3X/6

VCC3

C900	C0.22u16X50402-HF

TOP CAVITY

VCORE

C880	C22u6.3X/6
C217	C22u6.3X/6
C865	C22u6.3X/6
C863	C22u6.3X/6
C228	C22u6.3X/6
C218	C22u6.3X/6
C876	C22u6.3X/6
C884	C22u6.3X/6
C232	C22u6.3X/6
C229	C22u6.3X/6
C230	C22u6.3X/6
C867	C22u6.3X/6

VCCP_NB

C835	C22u6.3X/6
C823	C22u6.3X/6
C80	C22u6.3X/6
C825	C22u6.3X/6
C81	C22u6.3X/6

VCC_DDR

C852	C22u6.3X/6
C236	C22u6.3X/6
C222	C22u6.3X/6
C210	C22u6.3X/6
C205	X_C22u6.3X/6
C219	X_C22u6.3X/6
C859	X_C22u6.3X/6

CPU_1P8

C335	C22u6.3X/6
C331	C0.22u16X50402-HF
C330	C0.22u16X50402-HF
C329	C0.1u16X0402

CPU_1P8_S5

C901	10u6.3X/6
C892	C0.22u16X50402-HF

BOTTOM CAVITY

VCORE

C122	C22u6.3X/6
C845	C22u6.3X/6
C118	C22u6.3X/6
C848	C22u6.3X/6
C212	C22u6.3X/6
C213	C22u6.3X/6
C877	C22u6.3X/6
C172	C22u6.3X/6
C844	C22u6.3X/6
C231	C22u6.3X/6
C883	C22u6.3X/6
C882	C22u6.3X/6
C856	C180p50N/4
C843	C22u6.3X/6
C849	C22u6.3X/6
C868	X_C22u6.3X/6
C878	X_C22u6.3X/6
C112	X_C22u6.3X/6
C125	X_C22u6.3X/6
C846	X_C22u6.3X/6
C137	X_C22u6.3X/6
C847	X_C22u6.3X/6
C837	X_C2.2u6.3X/4
C929	X_C2.2u6.3X/4
C928	X_C2.2u6.3X/4
C927	X_C2.2u6.3X/4
C926	X_C2.2u6.3X/4
C925	X_C2.2u6.3X/4
C924	X_C2.2u6.3X/4
C923	X_C2.2u6.3X/4
C922	X_C2.2u6.3X/4
C921	X_C2.2u6.3X/4
C972	X_C2.2u6.3X/4
C891	X_C2.2u6.3X/4
C895	X_C0.22u16X50402-HF
C897	X_C0.22u16X50402-HF
C850	X_C0.22u16X50402-HF
C874	X_C0.22u16X50402-HF
C920	X_C0.22u16X50402-HF
C879	X_C0.22u16X50402-HF
C904	X_C0.22u16X50402-HF
C896	X_C180p50N/4
C869	X_C180p50N/4
C873	X_C1000p50X4

VCCP_NB

C824	C22u6.3X/6
C82	C22u6.3X/6
C200	C22u6.3X/6
C815	C22u6.3X/6
C679	C22u6.3X/6
C821	C22u6.3X/6
C201	C22u6.3X/6
C86	C22u6.3X/6
C202	C22u6.3X/6
C85	C22u6.3X/6
C807	C180p50N/4
C818	X_C2.2u6.3X/4
C793	X_C2.2u6.3X/4
C792	X_C2.2u6.3X/4
C809	X_C2.2u6.3X/4
C794	X_C2.2u6.3X/4
C804	X_C2.2u6.3X/4
C832	X_C2.2u6.3X/4
C811	X_C2.2u6.3X/4
C796	X_C2.2u6.3X/4
C808	X_C2.2u6.3X/4
C814	X_C2.2u6.3X/4
C805	X_C2.2u6.3X/4
C806	X_C2.2u6.3X/4
C802	X_C0.22u16X50402-HF
C795	X_C0.22u16X50402-HF
C800	X_C0.22u16X50402-HF
C789	X_C0.22u16X50402-HF
C798	X_C0.22u16X50402-HF
C788	X_C0.22u16X50402-HF
C813	X_C0.22u16X50402-HF
C820	X_C0.22u16X50402-HF
C803	X_C0.22u16X50402-HF
C791	X_C0.22u16X50402-HF
C797	X_C180p50N/4
C801	X_C180p50N/4

VCC_DDR

C810	C0.22u16X50402-HF
C190	C180p50N/4
C860	X_C22u6.3X/6
C235	X_C22u6.3X/6
C197	X_C22u6.3X/6
C870	X_C2.2u6.3X/4
C858	X_C2.2u6.3X/4
C241	X_C2.2u6.3X/4
C240	X_C2.2u6.3X/4
C831	X_C2.2u6.3X/4
C816	X_C2.2u6.3X/4
C871	X_C2.2u6.3X/4
C875	X_C2.2u6.3X/4
C886	X_C180p50N/4
C799	X_C0.22u16X50402-HF
C817	X_C0.22u16X50402-HF
C888	X_C180p50N/4
C221	X_C1u16/6
C272	X_C0.1u16X0402
C259	X_C0.1u16X0402
C207	X_C0.1u16X0402
C186	X_C0.1u16X0402
C182	X_C0.1u16X0402
C195	X_C0.1u16X0402
C209	X_C0.1u16X0402
C192	X_C0.1u16X0402

VCCP_NB_S5

C220	C22u6.3X/6
C299	C0.22u16X50402-HF

CPU_VDDP_S5

C333	10u6.3X/6
C321	C0.22u16X50402-HF

CPU_1P8

C893	C0.22u16X50402-HF

3VSB

C315	C0.22u16X50402-HF

BOTTOM SIDE

CPU1H

POWER

M7	VDDCR_CPU_0	VDDCR_SOC_0	B5
N3	VDDCR_CPU_1	VDDCR_SOC_1	B8
N6	VDDCR_CPU_2	VDDCR_SOC_2	B11
P2	VDDCR_CPU_3	VDDCR_SOC_3	B14
R7	VDDCR_CPU_4	VDDCR_SOC_4	B17
T3	VDDCR_CPU_5	VDDCR_SOC_5	B20
T6	VDDCR_CPU_6	VDDCR_SOC_6	C4
T9	VDDCR_CPU_7	VDDCR_SOC_7	C7
U2	VDDCR_CPU_8	VDDCR_SOC_8	C10
U10	VDDCR_CPU_9	VDDCR_SOC_9	C13
V9	VDDCR_CPU_10	VDDCR_SOC_10	C16
V11	VDDCR_CPU_11	VDDCR_SOC_11	C19
W3	VDDCR_CPU_12	VDDCR_SOC_12	D3
W6	VDDCR_CPU_13	VDDCR_SOC_13	E2
W10	VDDCR_CPU_14	VDDCR_SOC_14	F7
W12	VDDCR_CPU_15	VDDCR_SOC_15	F10
Y2	VDDCR_CPU_16	VDDCR_SOC_16	F13
Y9	VDDCR_CPU_17	VDDCR_SOC_17	F16
Y11	VDDCR_CPU_18	VDDCR_SOC_18	G3
Y13	VDDCR_CPU_19	VDDCR_SOC_19	G6
AA7	VDDCR_CPU_20	VDDCR_SOC_20	G9
AA10	VDDCR_CPU_21	VDDCR_SOC_21	G12
AA12	VDDCR_CPU_22	VDDCR_SOC_22	G15
AB3	VDDCR_CPU_23	VDDCR_SOC_23	G18
AB6	VDDCR_CPU_24	VDDCR_SOC_24	H2
AB9	VDDCR_CPU_25	VDDCR_SOC_25	J7
AB11	VDDCR_CPU_26	VDDCR_SOC_26	J10
AB13	VDDCR_CPU_27	VDDCR_SOC_27	J12
AC2	VDDCR_CPU_28	VDDCR_SOC_28	J14
AC10	VDDCR_CPU_29	VDDCR_SOC_29	J16
AC12	VDDCR_CPU_30	VDDCR_SOC_30	K3
AD7	VDDCR_CPU_31	VDDCR_SOC_31	K6
AD9	VDDCR_CPU_32	VDDCR_SOC_32	K9
AD11	VDDCR_CPU_33	VDDCR_SOC_33	K11
AD13	VDDCR_CPU_34	VDDCR_SOC_34	K13
AE3	VDDCR_CPU_35	VDDCR_SOC_35	K15
AE6	VDDCR_CPU_36	VDDCR_SOC_36	L2
AE10	VDDCR_CPU_37	VDDCR_SOC_37	L10
AE12	VDDCR_CPU_38	VDDCR_SOC_38	L12
AF2	VDDCR_CPU_39	VDDCR_SOC_39	L14
AF9	VDDCR_CPU_40	VDDCR_SOC_40	L16
AF11	VDDCR_CPU_41	VDDCR_SOC_41	L18
AF13	VDDCR_CPU_42	VDDCR_SOC_42	L20
AG7	VDDCR_CPU_43	VDDCR_SOC_43	L22
AG10	VDDCR_CPU_44	VDDCR_SOC_44	L24
AG12	VDDCR_CPU_45	VDDCR_SOC_45	L26
AG14	VDDCR_CPU_46	VDDCR_SOC_46	M9
AG16	VDDCR_CPU_47	VDDCR_SOC_47	M11
AG18	VDDCR_CPU_48	VDDCR_SOC_48	M13
AG20	VDDCR_CPU_49	VDDCR_SOC_49	M15
AG22	VDDCR_CPU_50	VDDCR_SOC_50	M17
AG24	VDDCR_CPU_51	VDDCR_SOC_51	M19
AG26	VDDCR_CPU_52	VDDCR_SOC_52	M21
AH3	VDDCR_CPU_53	VDDCR_SOC_53	M23
AH6	VDDCR_CPU_54	VDDCR_SOC_54	M25
AH9	VDDCR_CPU_55	VDDCR_SOC_55	N10
AH11	VDDCR_CPU_56	VDDCR_SOC_56	N12
AH13	VDDCR_CPU_57	VDDCR_SOC_57	N14
AH15	VDDCR_CPU_58	VDDCR_SOC_58	N16
AH17	VDDCR_CPU_59	VDDCR_SOC_59	N18
AH19	VDDCR_CPU_60	VDDCR_SOC_60	N20
AH21	VDDCR_CPU_61	VDDCR_SOC_61	N22
AH23	VDDCR_CPU_62	VDDCR_SOC_62	N24
AH25	VDDCR_CPU_63	VDDCR_SOC_63	N26
AH27	VDDCR_CPU_64	VDDCR_SOC_64	P9
AJ2	VDDCR_CPU_65	VDDCR_SOC_65	P11
AJ10	VDDCR_CPU_66	VDDCR_SOC_66	P13
AJ12	VDDCR_CPU_67	VDDCR_SOC_67	R10
AJ14	VDDCR_CPU_68	VDDCR_SOC_68	R12
AJ22	VDDCR_CPU_69	VDDCR_SOC_69	T11
AJ24	VDDCR_CPU_70	VDDCR_SOC_70	T13
AK7	VDDCR_CPU_71	VDDCR_SOC_71	U12
AK9	VDDCR_CPU_72	VDDCR_SOC_72	V13
AK11	VDDCR_CPU_73		
AK13	VDDCR_CPU_74		
AL3	VDDCR_CPU_75		
AL6	VDDCR_CPU_76		
AL10	VDDCR_CPU_77		
AL12	VDDCR_CPU_78		
AL14	VDDCR_CPU_79	VDDCR_SOC_S5_0	AJ18
AM2	VDDCR_CPU_80	VDDCR_SOC_S5_1	AK18
AM8	VDDCR_CPU_81		
AN7	VDDCR_CPU_82		
AN10	VDDCR_CPU_83		
AN13	VDDCR_CPU_84		
AP3	VDDCR_CPU_85		
AP9	VDDCR_CPU_86		
AP12	VDDCR_CPU_87		
AR2	VDDCR_CPU_88		
AT4	VDDCR_CPU_89		
AU3	VDDCR_CPU_90		
AU6	VDDCR_CPU_91		
AU9	VDDCR_CPU_92		
AU12	VDDCR_CPU_93		
AU15	VDDCR_CPU_94		
AV5	VDDCR_CPU_95		
AV8	VDDCR_CPU_96		
AV11	VDDCR_CPU_97		
AV14	VDDCR_CPU_98		

VCCP_NB_S5
0.9A

AM4
PART 8 OF 9
ZIF-SOCKET1331

CPU1G

POWER

K36	VDDIO_MEM_S3_0	VDDP_0	AM18
K39	VDDIO_MEM_S3_1	VDDP_1	AM19
L32	VDDIO_MEM_S3_2	VDDP_2	AM20
L35	VDDIO_MEM_S3_3	VDDP_3	AN18
L38	VDDIO_MEM_S3_4	VDDP_4	AN19
M29	VDDIO_MEM_S3_5	VDDP_5	AN20
M31	VDDIO_MEM_S3_6	VDDP_6	AP18
M34	VDDIO_MEM_S3_7	VDDP_7	AP19
M37	VDDIO_MEM_S3_8	VDDP_8	AP20
N28	VDDIO_MEM_S3_9		
N30	VDDIO_MEM_S3_10		
N33	VDDIO_MEM_S3_11	VDDIO_AUDIO	AM15
N36	VDDIO_MEM_S3_12		
N39	VDDIO_MEM_S3_13		
P27	VDDIO_MEM_S3_14	VDD_18_0	AJ20
P29	VDDIO_MEM_S3_15	VDD_18_1	AK20
P32	VDDIO_MEM_S3_16		
P35	VDDIO_MEM_S3_17	VDD_33_0	AJ21
P38	VDDIO_MEM_S3_18	VDD_33_1	AK21
R28	VDDIO_MEM_S3_19		
R31	VDDIO_MEM_S3_20		
R34	VDDIO_MEM_S3_21		
R37	VDDIO_MEM_S3_22	VDDP_S5_0	AJ16
T27	VDDIO_MEM_S3_23	VDDP_S5_1	AJ17
T29	VDDIO_MEM_S3_24		
T33	VDDIO_MEM_S3_25		
T36	VDDIO_MEM_S3_26	VDD_18_S5_0	AJ15
T39	VDDIO_MEM_S3_27	VDD_18_S5_1	AK15
U28	VDDIO_MEM_S3_28		
U30	VDDIO_MEM_S3_29		
U32	VDDIO_MEM_S3_30	VDD_33_S5_0	AJ19
U35	VDDIO_MEM_S3_31	VDD_33_S5_1	AK19
U38	VDDIO_MEM_S3_32		
V27	VDDIO_MEM_S3_33		
V29	VDDIO_MEM_S3_34	VDDBT_RTC_G	AL15
V31	VDDIO_MEM_S3_35		
V34	VDDIO_MEM_S3_36		
V37	VDDIO_MEM_S3_37		AM12
W28	VDDIO_MEM_S3_38	RSVD_0	AT25
W33	VDDIO_MEM_S3_39	RSVD_1	AR15
W34	VDDIO_MEM_S3_40	RSVD_2	AP15
W36	VDDIO_MEM_S3_41	RSVD_3	AN12
W39	VDDIO_MEM_S3_42	RSVD_4	AN15
Y27	VDDIO_MEM_S3_43	RSVD_5	AT30
Y29	VDDIO_MEM_S3_44	RSVD_6	AW24
Y31	VDDIO_MEM_S3_45	RSVD_7	AR24
Y32	VDDIO_MEM_S3_46	RSVD_8	A5
Y35	VDDIO_MEM_S3_47	RSVD_9	AD3
Y38	VDDIO_MEM_S3_48	RSVD_10	AB2
AA28	VDDIO_MEM_S3_49	RSVD_11	AH2
AA34	VDDIO_MEM_S3_50	RSVD_12	AL16
AA37	VDDIO_MEM_S3_51	RSVD_13	AL17
AB27	VDDIO_MEM_S3_52	RSVD_14	AL18
AB29	VDDIO_MEM_S3_53	RSVD_15	AL19
AB31	VDDIO_MEM_S3_54	RSVD_16	AL20
AB32	VDDIO_MEM_S3_55	RSVD_17	AL21
AB33	VDDIO_MEM_S3_56	RSVD_18	AM16
AB36	VDDIO_MEM_S3_57	RSVD_19	AM17
AB39	VDDIO_MEM_S3_58	RSVD_20	AM21
AC28	VDDIO_MEM_S3_59	RSVD_21	AN16
AC30	VDDIO_MEM_S3_60	RSVD_22	AN17
AC32	VDDIO_MEM_S3_61	RSVD_23	AN21
AC35	VDDIO_MEM_S3_62	RSVD_24	AP16
AC38	VDDIO_MEM_S3_63	RSVD_25	AP17
AD27	VDDIO_MEM_S3_64	RSVD_26	AP21
AD29	VDDIO_MEM_S3_65	RSVD_27	AR16
AD31	VDDIO_MEM_S3_66	RSVD_28	AR18
AD34	VDDIO_MEM_S3_67	RSVD_29	AR19
AD37	VDDIO_MEM_S3_68	RSVD_30	AR20
AE28	VDDIO_MEM_S3_69	RSVD_31	AR21
AE30	VDDIO_MEM_S3_70	RSVD_32	AT19
AE33	VDDIO_MEM_S3_71	RSVD_33	D28
AE36	VDDIO_MEM_S3_72	RSVD_34	E19
AE39	VDDIO_MEM_S3_73	RSVD_35	E22
AF27	VDDIO_MEM_S3_74	RSVD_36	E25
AF29	VDDIO_MEM_S3_75	RSVD_37	G17
AF32	VDDIO_MEM_S3_76	RSVD_38	J36
AF35	VDDIO_MEM_S3_77	RSVD_39	J38
AF38	VDDIO_MEM_S3_78	RSVD_40	K34
AG33	VDDIO_MEM_S3_79	RSVD_41	K38
AG34	VDDIO_MEM_S3_80	RSVD_42	R35
AG35	VDDIO_MEM_S3_81	RSVD_43	AB37
AG37	VDDIO_MEM_S3_82	RSVD_44	AH35
AH39	VDDIO_MEM_S3_83	RSVD_45	AK34
		RSVD_46	

AM4
PART 7 OF 9
ZIF-SOCKET1331

CPU_VDDP 8.5A
0.25A
CPU_1P8 2.00A
VCC3 0.25A
CPU_VDDP_S5 1.00A
CPU_1P8_S5 0.5A
3VSB 0.25A
4.5uA

C317 C0.22u16X50402-HF
C320 10u6.3X/6
C722 1u6.3X/4
C719 C0.22u16X50402-HF
C903 C22u6.3X/6
C294 C22u6.3X/6

Title	MICRO-STAR INT'L CO.,LTD.
	AM4 Power/RTC Power
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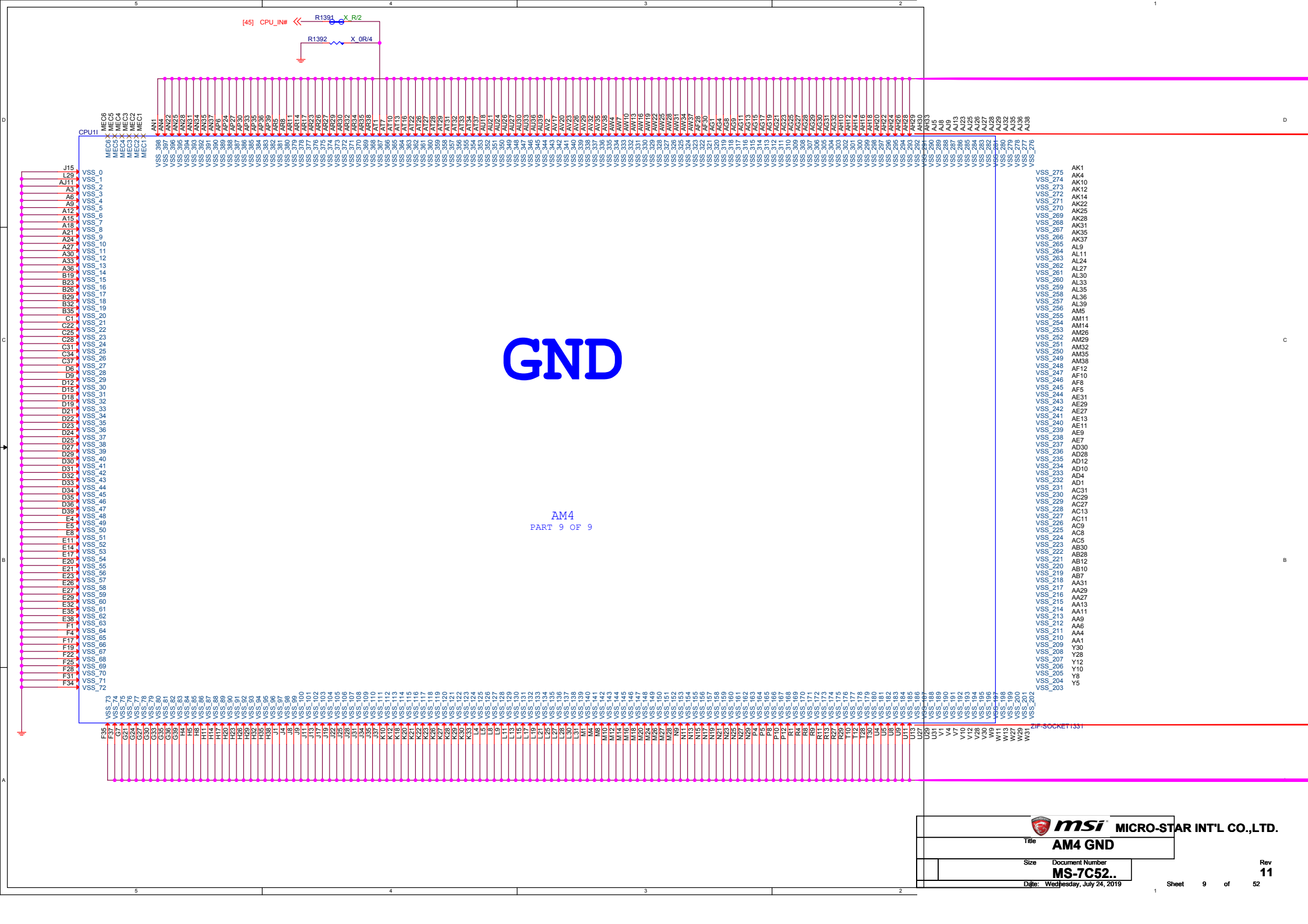

MICRO-STAR INT'L CO.,LTD.	
Title	AM4 GND
Size	Document Number: MS-7C52..
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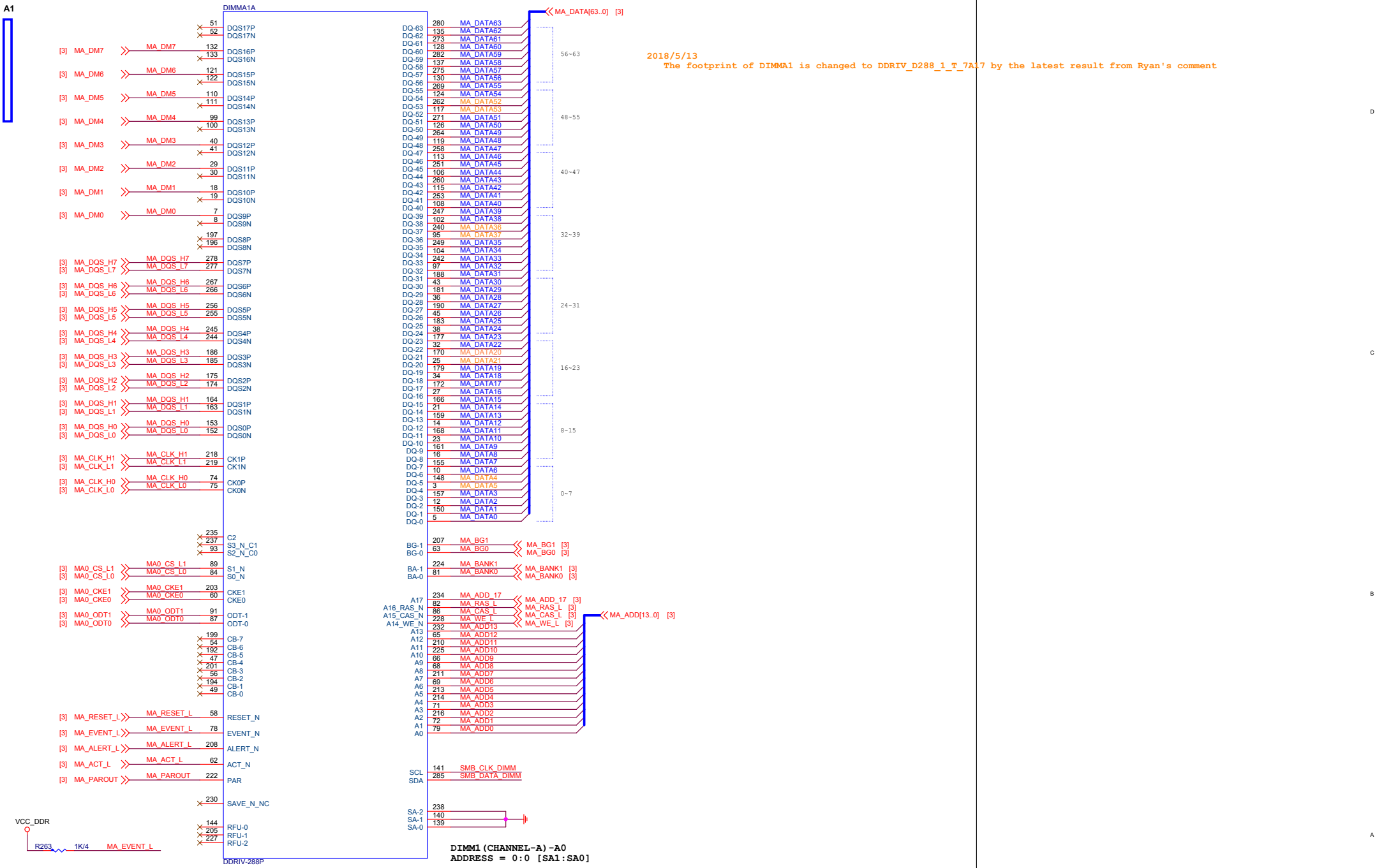

MICRO-STAR INT'L CO.,LTD.

Title: DDR4 DIMM CH-A

Size: Document Number: MS-7C52.. Rev: 11

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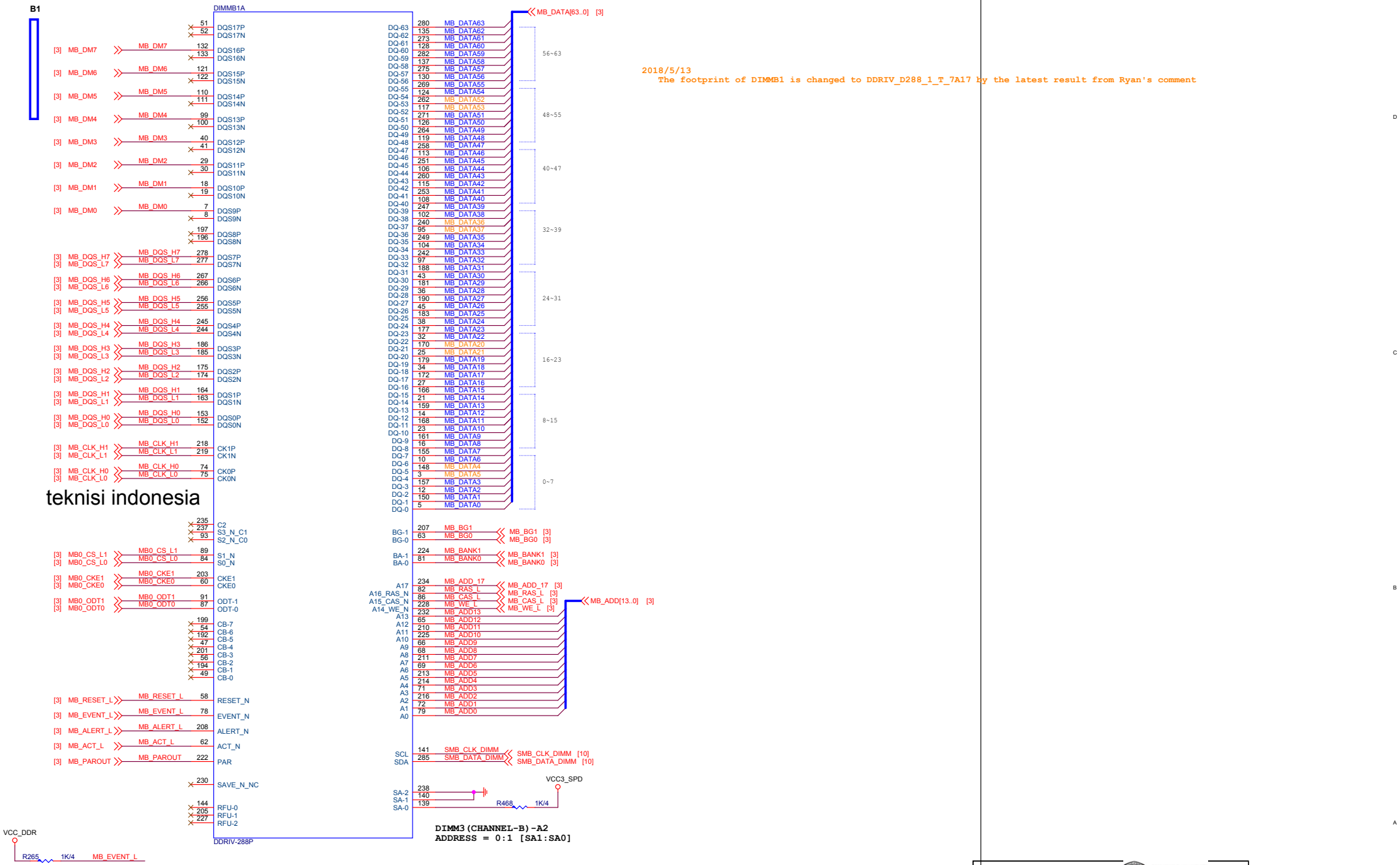

Title	DDR4 DIMM CH-B
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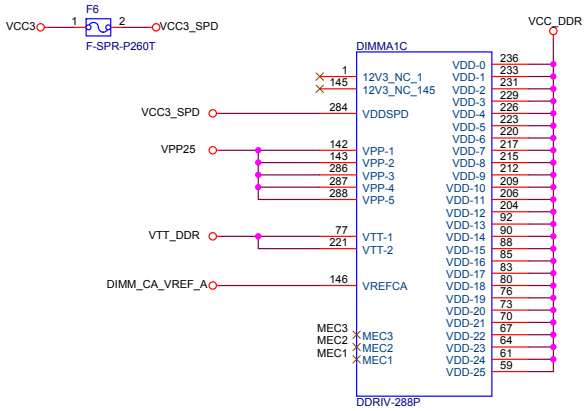
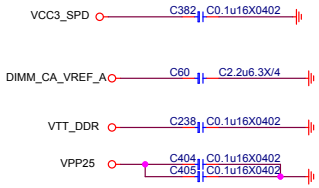
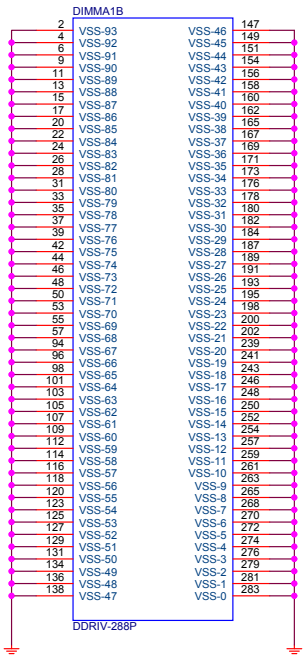
MICRO-STAR INT'L CO.,LTD.



2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

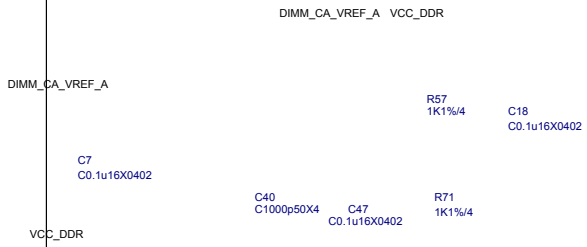




2018/5/13
The footprint of DIMMA1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

DDR VREF

(place resistors close to DIMMs)



MICRO-STAR INT'L CO.,LTD.

Title	DDR4-POWER/GND-1	
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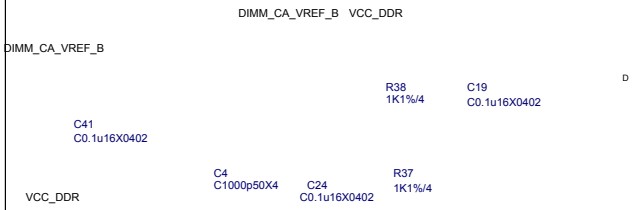
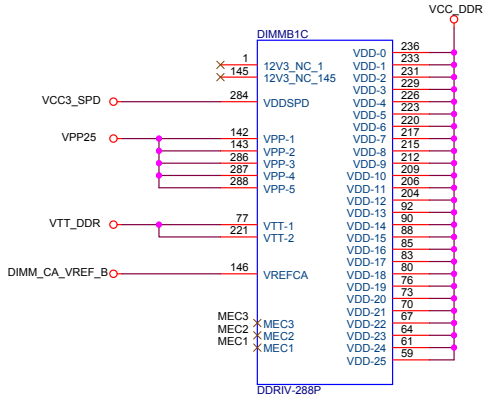
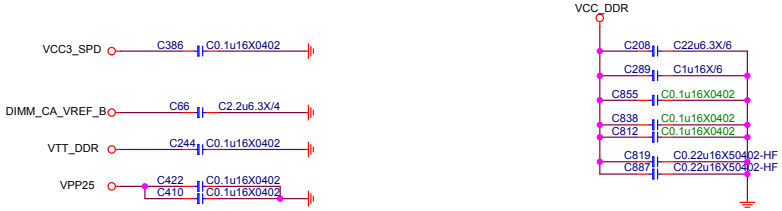
DDR VREF

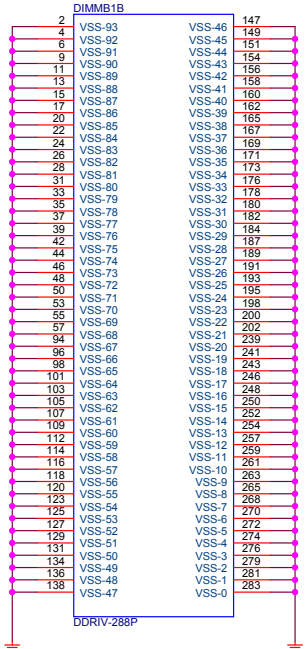
(place resistors close to DIMMs)





2018/5/13
The footprint of DIMMB1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment





2018/5/13
The footprint of DIMMB1 is changed to DDRIV_D288_1_T_7A17 by the latest result from Ryan's comment

MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-2

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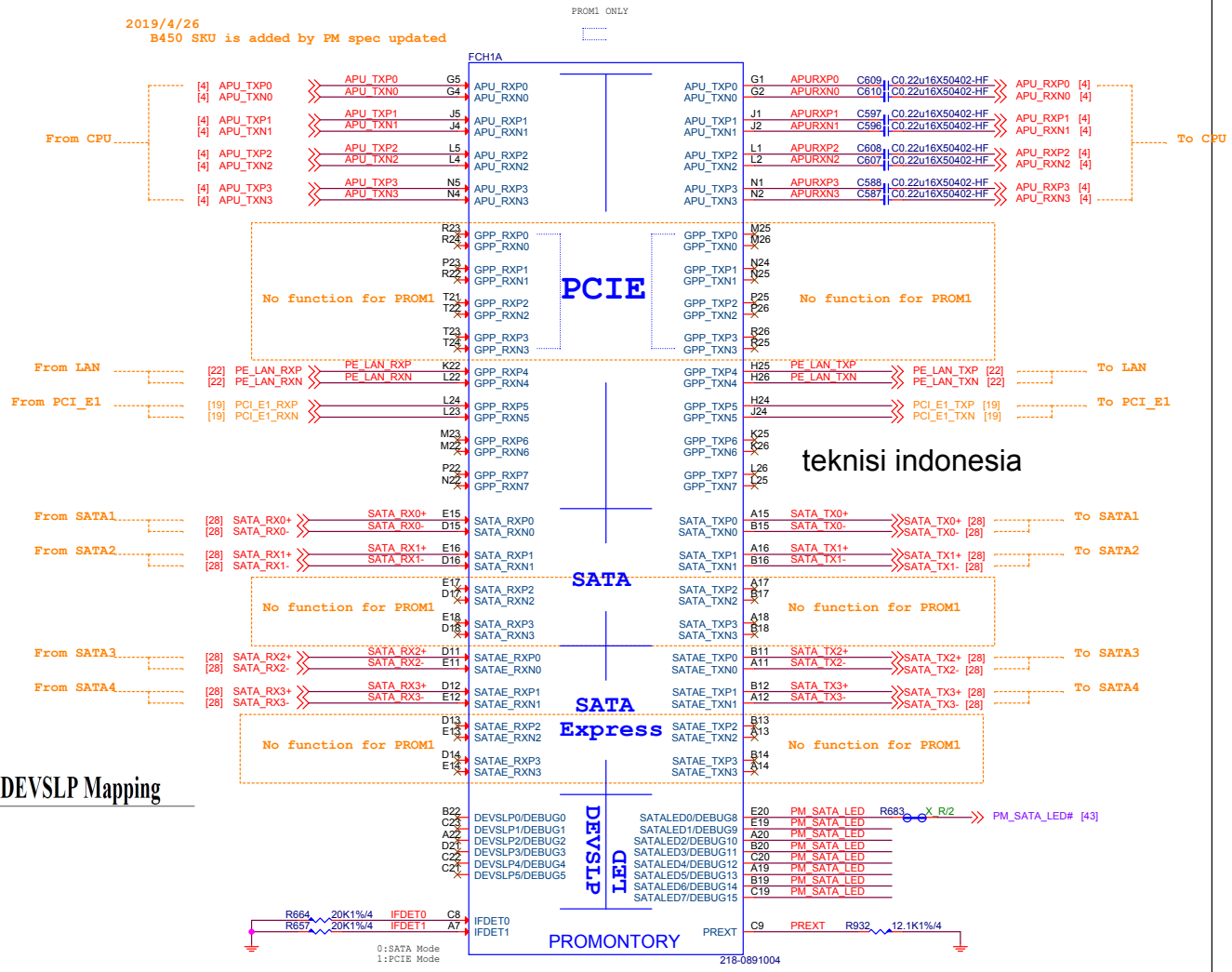

2019/7/18 (1.1 only)
The name of net is changed from SATA_LED# to PM_SATA_LED# by SATA_ACT_L function fails with Matisse

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

Appendix F SATA Port to SATA LED Mapping

SATA port	SATA LED
SATA_TX/RXP/N[0]	SATALED0
SATA_TX/RXP/N[1]	SATALED1
SATA_TX/RXP/N[2]	SATALED2
SATA_TX/RXP/N[3]	SATALED3
SATAE_TX/RXP/N[0]	SATALED4
SATAE_TX/RXP/N[1]	SATALED5
SATAE_TX/RXP/N[2]	SATALED6
SATAE_TX/RXP/N[3]	SATALED7

Appendix G SATA Port to DEVSLP Mapping

SATA port	DEVSLP signal
SATA_TX/RXP/N[0]	DEVSLP0
SATA_TX/RXP/N[1]	DEVSLP1
SATA_TX/RXP/N[2]	DEVSLP2
SATA_TX/RXP/N[3]	DEVSLP3
SATAE_TX/RXP/N[0]	SATAE_CLKREQ0N
SATAE_TX/RXP/N[1]	DEVSLP4
SATAE_TX/RXP/N[2]	SATAE_CLKREQ1N
SATAE_TX/RXP/N[3]	DEVSLP5

MICRO-STAR INT'L CO.,LTD.
Title: Promontory-PCIE/SATA/SATAE
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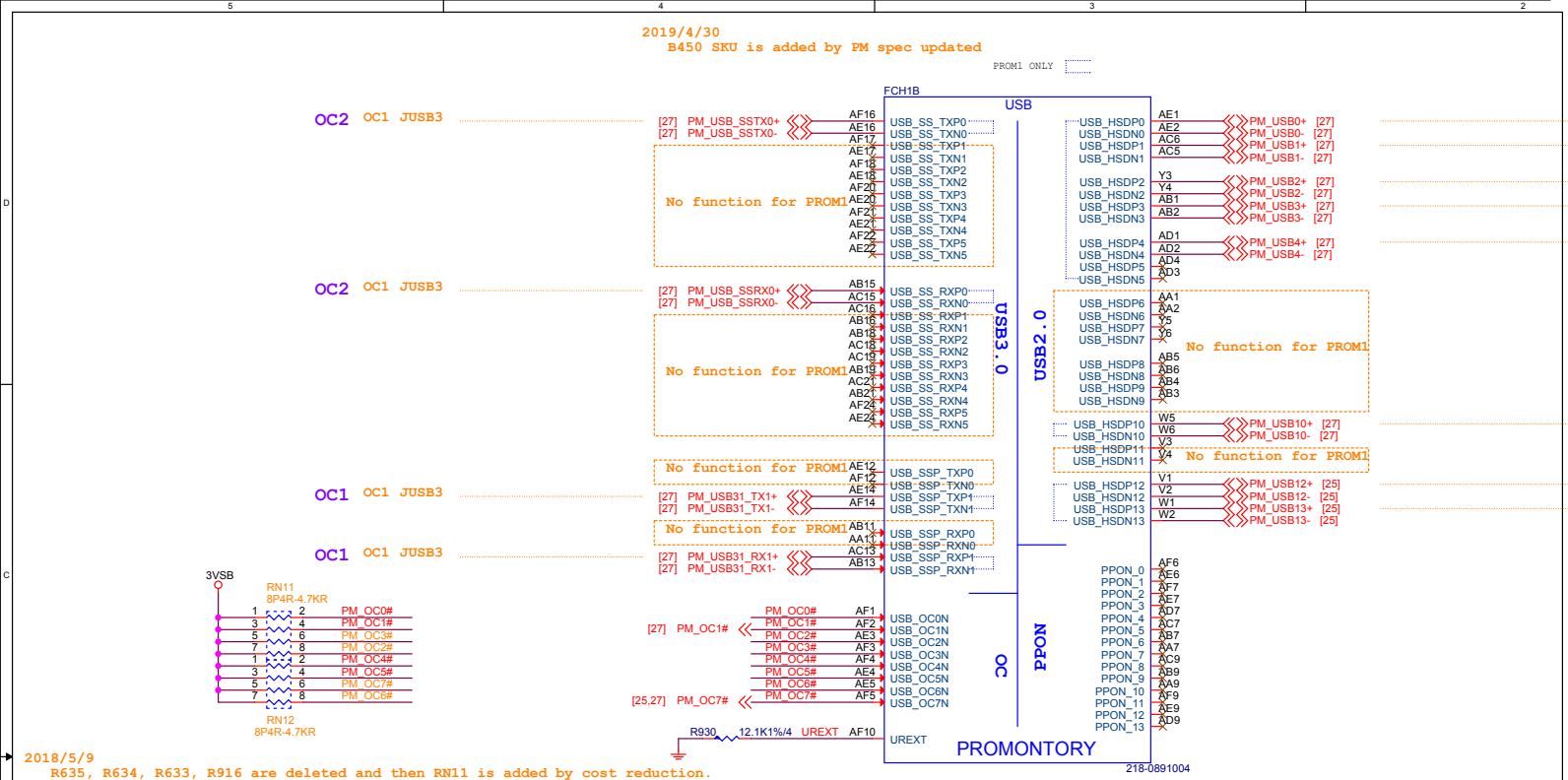

Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

MICRO-STAR INT'L CO.,LTD.
Title: Promontory-USB/OC
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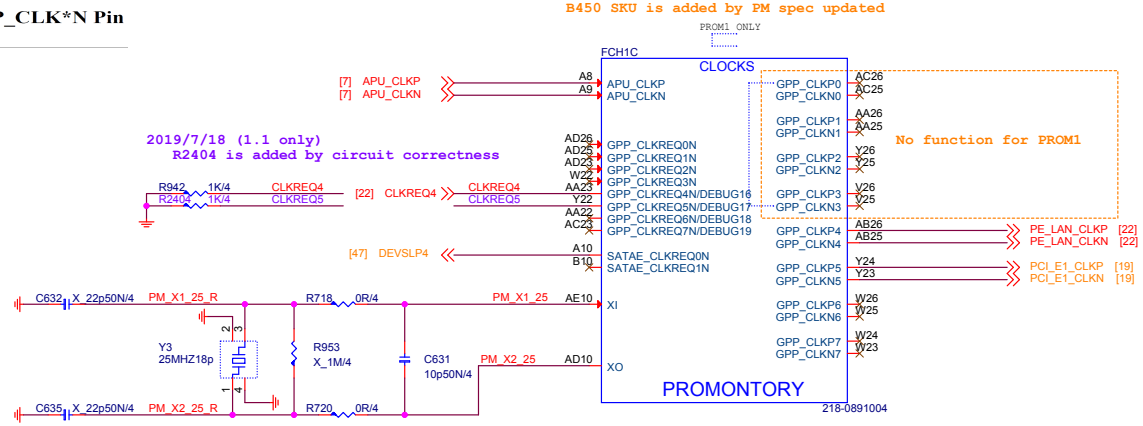
Appendix E GPP Port to GPP_CLK*N Pin Mapping

GPP Clock	CLKREQ#
GPP_CLKP/N[0]	GPP_CLKREQ0N
GPP_CLKP/N[1]	GPP_CLKREQ1N
GPP_CLKP/N[2]	GPP_CLKREQ2N
GPP_CLKP/N[3]	GPP_CLKREQ3N
GPP_CLKP/N[4]	GPP_CLKREQ4N
GPP_CLKP/N[5]	GPP_CLKREQ5N
GPP_CLKP/N[6]	GPP_CLKREQ6N
GPP_CLKP/N[7]	GPP_CLKREQ7N

2019/4/30
B450 SKU is added by PM spec updated

2019/7/18 (1.1 only)
R2404 is added by circuit correctness



Vinafix.com

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

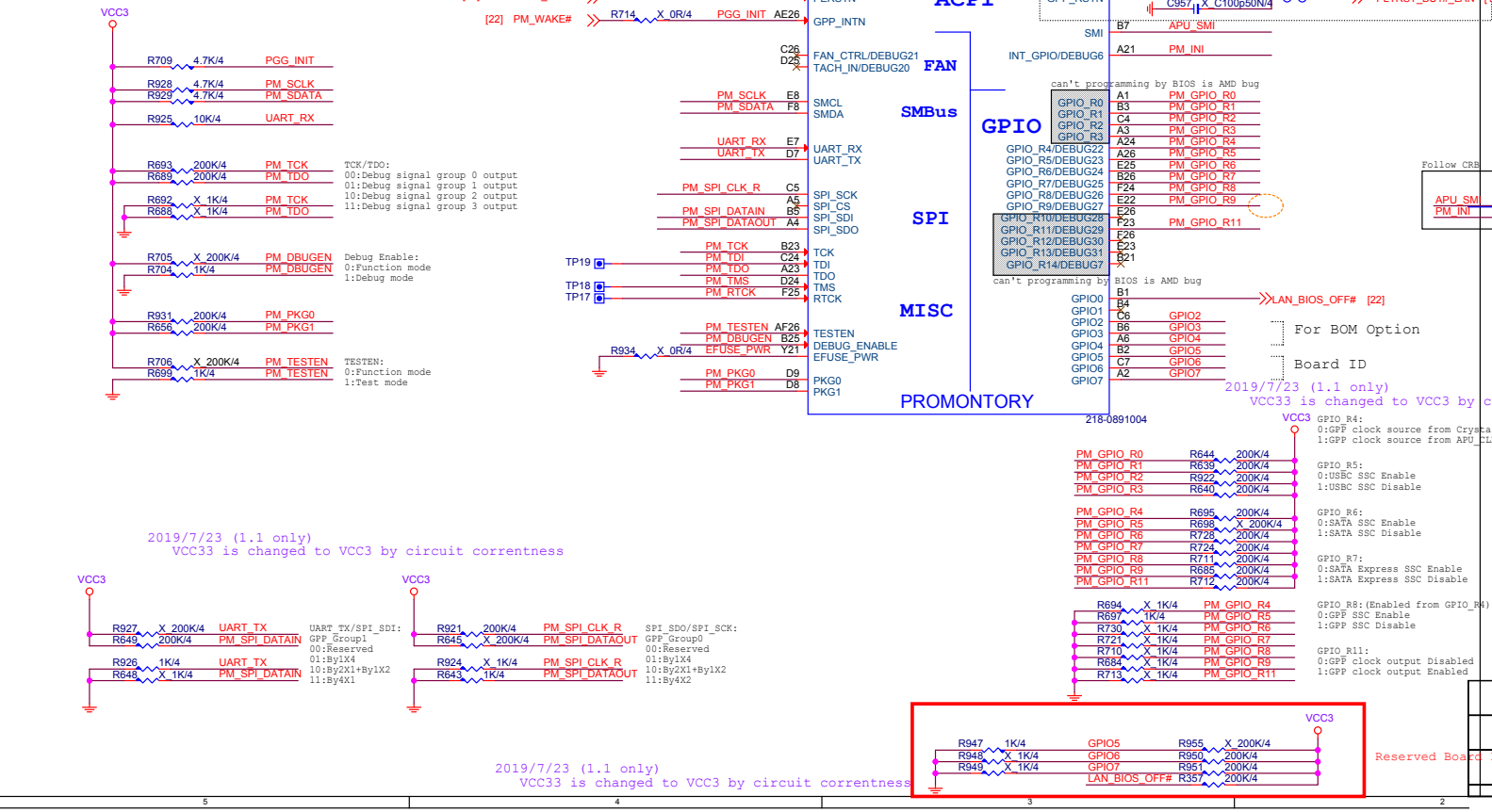
BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM3	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

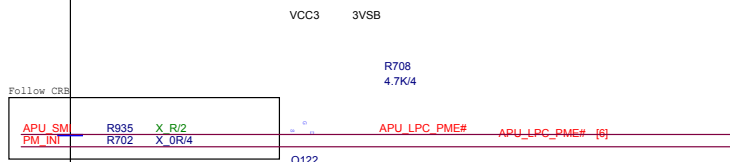
2019/4/30
B450 SKU is added by PM spec updated

2019/5/8
R933 is changed to 0ohm to short copper by cost reduction.

2019/7/23 (1.1 only)
VCC33 is changed to VCC3 by circuit correntness

Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.





2019/7/23 (1.1 only)
VCC33 is changed to VCC3 by circuit correntness

2019/7/23 (1.1 only)
VCC33 is changed to VCC3 by circuit correntness

BOM OPTION

VCC3

R629	10K/4	GPIO2	R630	10K/4
R642	10K/4	GPIO3	R641	10K/4
R652	X_10K/4	GPIO4	R655	10K/4

	01S	02S	03S
GPIO2	0	1	0	1
GPIO3	0	0	1	1
GPIO4	0	0	0	0

2019/7/23 (1.1 only)
VCC33 is changed to VCC3 by circuit correntness

MSI MICRO-STAR INT'L CO.,LTD.

Title: Promontory-CLK/ACPI/GPIO

Size: Document Number: MS-7C52..

Rev: 11

Date: Wednesday, July 24, 2019

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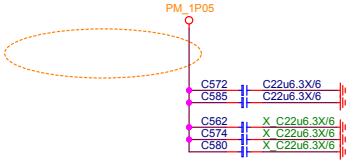
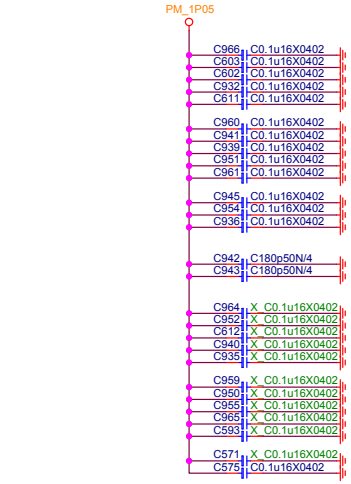
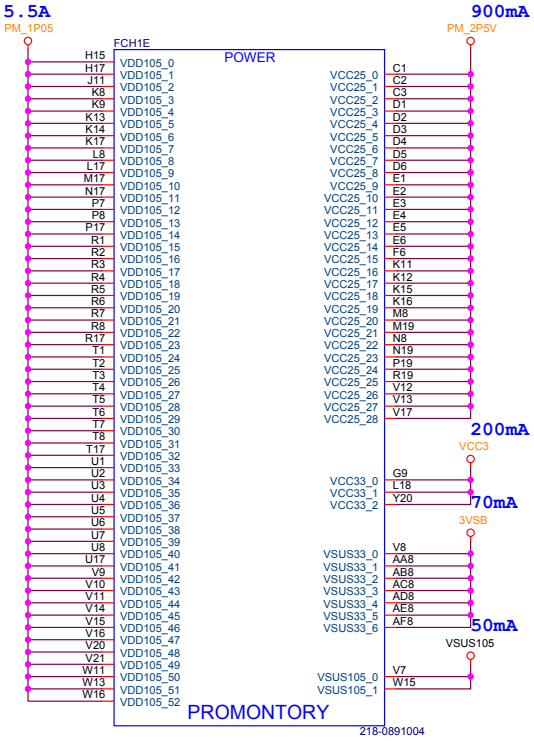
2019/4/30
L24, L23, L25, L30, L26, L28 are changed to 0ohm by Ryan's comment.

2019/4/30
B450 SKU is added by PM spec updated

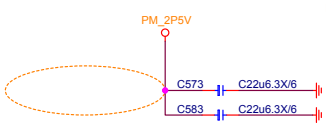
2019/5/8
L24, L23 are deleted by cost reduction

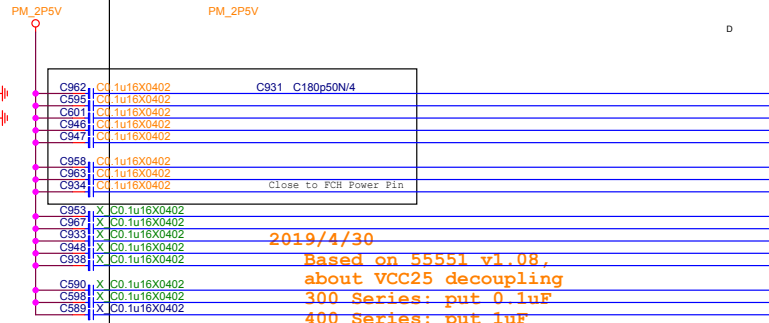






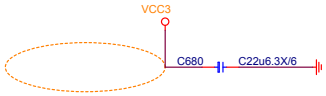
2019/5/8
L25 is deleted by cost reduction

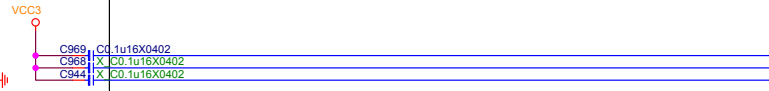




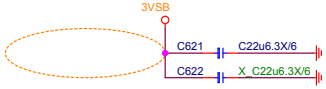
2019/4/30
Based on 55551 v1.08,
about VCC25 decoupling
300 Series: put 0.1uF
400 Series: put 1uF

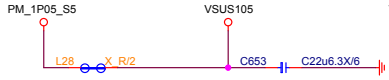
2019/5/8
L30 is deleted by cost reduction





2019/5/8
L26 is deleted by cost reduction





2019/5/8
L28 is changed to 0ohm to short copper
by cost reduction.

Chapter 17 Power and Decoupling Requirements

Note: Unless otherwise specified, recommended capacitor dielectric material is X5R, X6S, X7R, or X7S ceramic. Designers may replace a larger capacitor body size with a smaller body size. Transposed body sizes are acceptable and preferred.

No.	Y/N/V	Group	Explanation	Qty	Value	Units	Size/Tol	Comments
17-5		VDD105	Ceramic capacitors.	6	22	µF	0805	
17-10			Ceramic capacitors.	25	1	µF	0402	
17-15		VCC25	Ceramic capacitors.	4	22	µF	0805	
17-20			300 Series: Ceramic capacitors.	12	0.1	µF	0402	
17-21			400 Series: Ceramic capacitors.	12	1	µF	0402	
17-25		VCC33	Ceramic capacitor.	1	22	µF	0805	
17-30			Ceramic capacitors.	1	0.1	µF	0402	
17-35		VSUS33	Ceramic capacitors.	1	22	µF	0805	
17-40			Ceramic capacitors.	1	0.1	µF	0402	
17-45		VSUS105	Ceramic capacitor.	1	22	µF	0805	
17-50			Ceramic capacitors.	2	0.1	µF	0402	

MICRO-STAR INT'L CO.,LTD.

Title: Promontory-Power

Size: Document Number: MS-7C52.. Rev: 11

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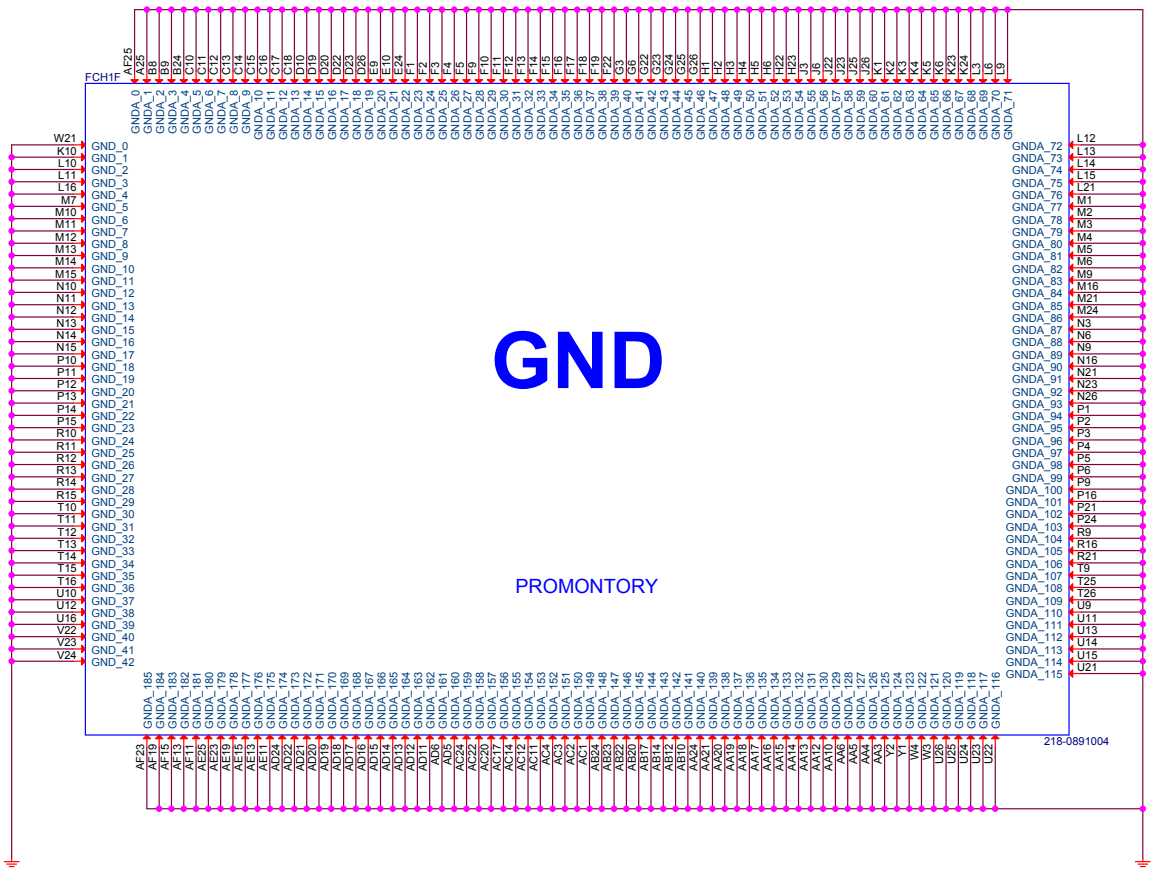
2019/4/30
B450 SKU is added by PM spec updated



Title	Promontory-GND
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MICRO-STAR INT'L CO.,LTD.

PCI EXPRESS x16 Slot

5.5A at +12V
3A at VCC3
375mA at 3VSB

0.5A at +12V
3A at VCC3
375mA at 3VSB

2019/5/15
The text of PCI_E1 & PCI_E2 are swapped by PM's comment

2019/4/15
PCI_E3, C647, C648, R800 are deleted by PM spec.

2019/7/25
C527, R600 are unstuffed by U81 unstuffed

within 500mil

2019/4/30
EC35 is changed to C71-27117Y1-AO5
by PM spec updated.

轉正式Footprint

2019/4/11
PCI_E2 需要colay鐵甲 16的footprint，P/N:N11-1641491-L06)

2019/4/30
EC36 is changed to C71-56106K1-AO5
by PM spec updated

PROM RESET

From SIO
From FCH

Co-lay FCH Reset for meet FCH sequence. See 55553.

SMBus separate circuit

SMB_SEL
GPIO Default High

MICRO-STAR INT'L CO.,LTD.

Title: PCIE X16(X1*2) SLOT

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GP70 的GPIO可以選成GRN_LED ，所以有呼吸燈的功能 ， 但有兩項要注意 ：
1, GRN_LED在您的案子應該會是PWR LED (LED VCC).
2, GP70有DSW_EN的hardware strapping ， 所以外部會有 pull-up 到SIO_3VA.

U46

ESPI/LPC Interface
PLTRST#/LRESET#
ESPI_CLK/LCLK
ESPI_RST#/LDRQ#
SERIRQ
ESPI_CS#/LFRAME#
ESPI_IO0/LAD0
ESPI_IO1/LAD1
ESPI_IO2/LAD2
ESPI_IO3/LAD3

UART SIR
RIA#/GP87
DCDA#/GP86
(TESTMODE1_EN)SOUTA/GP85
SINA/GP84
(FANOUT_DEF_EN)DTRA#/GP83
(2E_4E_SEL)RTSA#/GP82
DSRA#/GP81
CTSA#/GP80

KBC Function
KBRST#
(ESPI_EN)GA20M
AUXFANIN2/GP20/KDAT
CIRRX/AUXFANOU2/GP21/KCLK
AUXFANIN3/GP22/MDAT
AUXFANOUT3/GP23/MCLK

DSW Interface
GP54/SLP_SUS#
DPWROK
DEEP_S5_1/CASEOPEN1#
USBEN/3VSBSW/PWROK/ATXPGDO

Hardware Monitor
VIN2
VIN1
VIN0
CPUVCORE
VREF
AUXTIN0/VIN4
CPUTIN

FAN Control
CPUFANIN
CPUFANOUT
SYSFANIN
SYSFANOUT

ACPI Function
RSMRST#
PSIN#
PSOUT#
SLP_S3#
SLP_S5#
PSON#
ATXPGD
PWROK
RSTOUT0#/GP74
GP57/AUXFANIN2
GP56/AUXFANOUT2

Power Pin
PWR_FAULT#GP26/TSIC
PECI/TSID
GPO/GP73/CUT_VBAT
(DSW_EN)GP70
VIN7/AUXTIN3/ATX_5VSB
PAD_CAP
PCHVSB
VTT
VBAT
3VSB
AVSB
3VCC
PAD_VDD
VSS
CPUD-/AGND

NCT5565D

Change P/N

2018/5/10
R2386 is deleted by Ryan's comment

20181029
update to G3下可clean CMOS.

Stuff for New version IO

1.5V
=1.527V
<1.2V DPWROK LOW FOR AC POWER LOSS

close to PIN11

COM PORT

NO USE UART PORT1

GD75232DBR

JCOM1
CN2
CN1
H2X5[10]M
X_8P4C-470p50X/6

POWER ON STRAPPING PIN FOR NCT5565D

PIN	5563D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%.	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN

HW Monitor - Voltage

VCORE R350 10K1%/4 CPUVcore
R368 X_10K1%/4 C356 10u6.3X/6
+12V R369 220K1%/4 VIN0
R370 20K1%/4 C344 C0.1u16X0402
VCC5 R372 12K1%/4 VIN1
R359 3K1%/4 C351 C0.1u16X0402
VCCP_NB R362 10K1%/4 VIN2
R407 X_10K1%/4 C316 10u6.3X/6

3V Analog Power

SIO_3VA DEEP_S5 R814 47K/4
SIO_3VA CP24 X_COPPER AVCC3 AVCC3
C415 C0.1u16X0402 C318 10u6.3X/6

Thermal Monitor

For CPU Under Socket
HM_VREF R719 10K1%/4 CPUTIN RT5 10KT1%/4 C684 C2200p50X/4 GNDHM

For System Close to SIO
SYSTIN Q52 P-PMBS3906 C379 C2200p50X/4 GNDHM

default Push-Pull
PLTRST_BU1#_R R462 4.7K/4
CHIP_PWGD R390 1K/4
R374 X_4.7K/4
CPUTIN R385 X_1K/4
PWRBTIN R356 10K1%/4 C384 C0.1u16X0402
HM_VREF C391 4.7u6.3X/6

C388 10u6.3X/6 C406 1u6.3X/4
close to pin3

C396 10u6.3X/6 C370 1u6.3X/4
close to pin24

AMD Platform

MICRO-STAR INT'L CO.,LTD.
Title: SIO NCT5565
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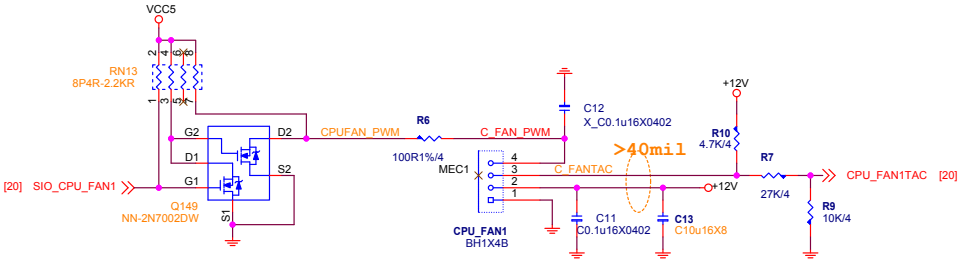
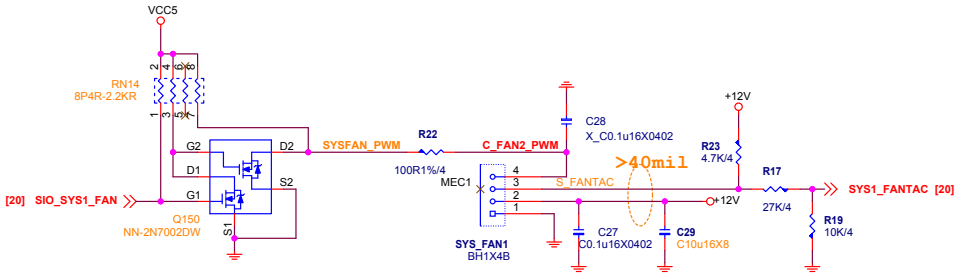
FAN(direct PWM mode)



2019/4/15
U2, C5, R8, C9, C23 are deleted; R1517, R1518, Q149 are added; R4 is changed to 2.2Kohm by PM spec.

2019/4/15
C13 is changed from 22uF to 10uF; D5, C10, C6 are deleted by the latest module circuit

2018/5/9
R1517, R1518, R4 are deleted and then RN13 is added by cost reduction.



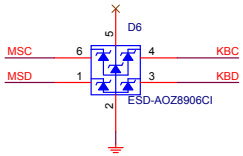
2019/4/15
U3, C14, R21, C20, C32 are deleted; Q150, R1520, R1519 are added; R20 is changed to 2.2Kohm by PM spec

2019/4/15
C29 is changed from 22uF to 10uF; D8, C21, C15 are deleted by the latest module circuit

2018/5/9
R1520, R1519, R20 are deleted and then RN14 is added by cost reduction.

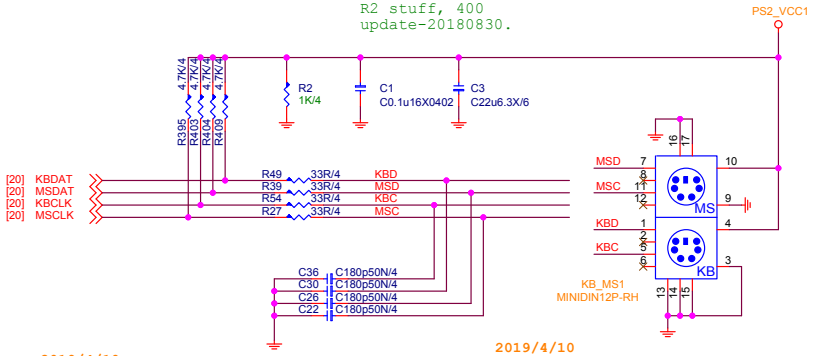
PS2

TVS P/N:
D0G-45B0510-I14



layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

20181026:
R2 stuff, 400
update-20180830.



2019/4/10
About PS2 circuit move from the page 25

2019/4/10
KB_MS1 is changed to N56-12F0151-H06 by PM spec.

MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN Control

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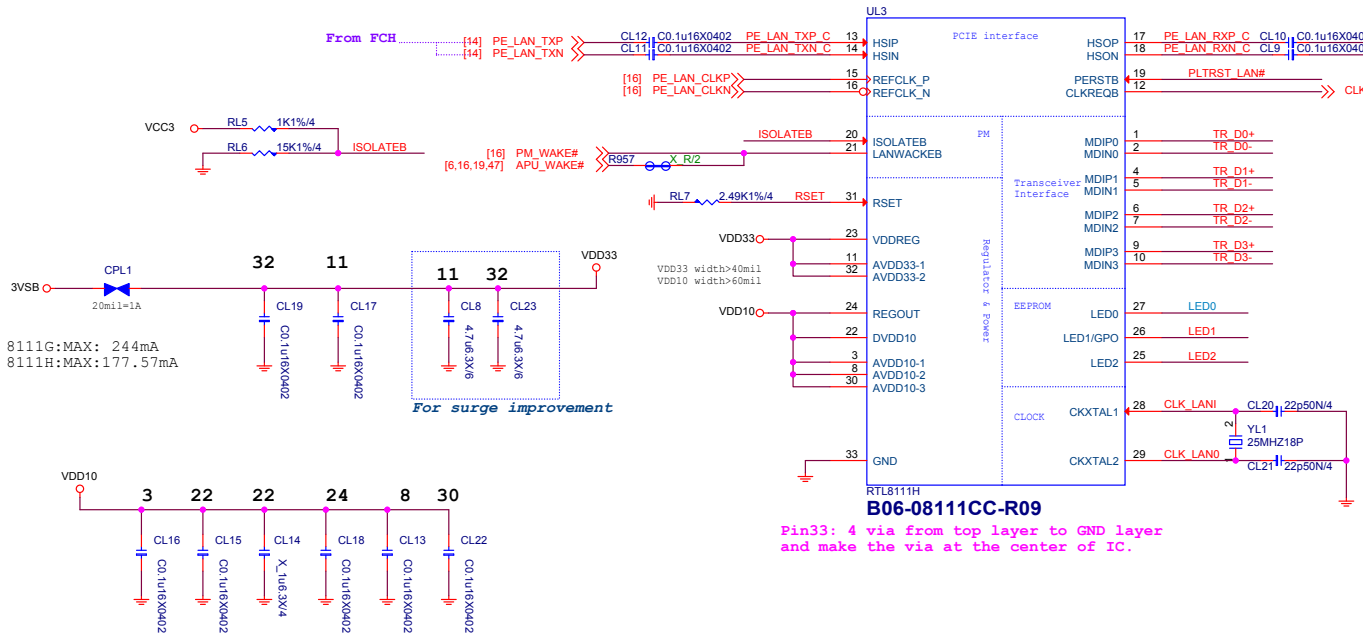
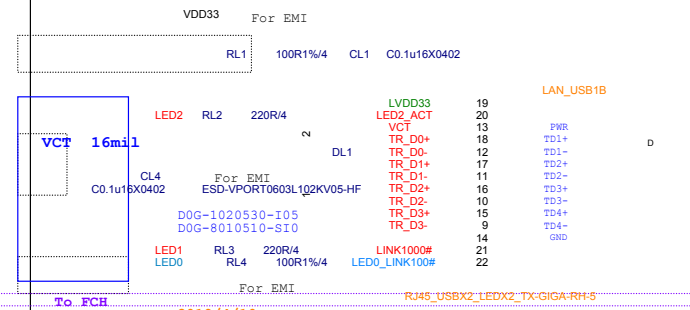
RTL8111G/RTL8111H Giga LAN

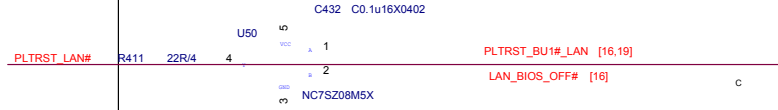


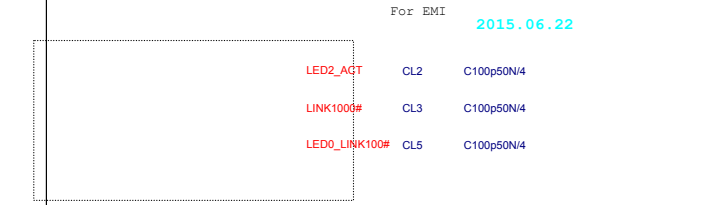
LAN Connector

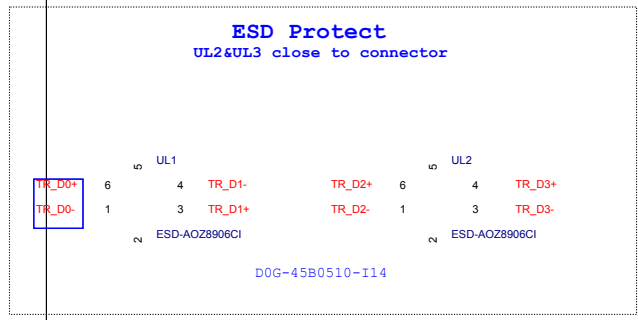


2019/4/10
LAN_USB1B is changed to N58-22F0731-F02 by PM spec.

2019/5/8
U50.5 is changed from VCC3 to 3VSB by Ryan's comment







Vinafix.com

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-STAR INT'L CO.,LTD.

Title: LAN-RTL8111H

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Type B: ALC892/887

Follow APU power well

CA14 closed PIN25
CA31 closed PIN38
CA30 closed PIN38

11mA
CPU_1P8_S5
Closed Codec
Closed PIN9
CA28 X_10u6.3X/6
CA18 C0.1u16X0402
VCC3
VOUT
CA30 C0.1u16X0402
CA14 C22u6.3X/6
CA31 10u6.3X/6

11mA
Closed PIN1
VCC3
CA20 10u6.3X/6
CA19 C0.1u16X0402

UA1

[24] EAPD
EAPD 47 EAPD/SPDIFI
48 SPDIF-OUT
DVDD DVDD-IO
LDO-OUT1 LDO-OUT2

[5] AZ_SDOUT
[5] AZ_SDIN0
[5] AZ_SYNC
[5] AZ_RST#
RA21 33R/4 SDIN0
8 SDATA-OUT
SDATA-IN
10 SYNC
11 RESET#
[5] AZ_BITCLK
6 BCLK

AZ_SDIN0
CA22 X_10p50N/4
REGREF
CA24 10u6.3X/6
2 3 GPIO0/DMIC-CLK/SPDIF-OUT2 REGREF
SENSE_A 13 SENSE A
SENSE_B 34 SENSE B

MIC1_V_R 32 MIC1-VREFO-R
MIC2_VREFO 30 MIC2-VREFO
MIC1_V_L 28 MIC1-VREFO-L
37 PIN37-VREFO
29 LDO-IN
45.8mA LDOVDD
LINE2_VREFO 31 LINE2-VREFO
VREF_AUDIO 27 VREF
33 SENSE C
JDREF 40 JDREF
CA16 X_C0.1u16X0402
CA17 10u6.3X/6
RA23 20K1%/4
12 BEEP
Closed Codec
GPIO1/DMIC-DATA DVSS AVSS AVSS
4 7 26 42 ALC892-CG-RH

CA16.CA17 close to Pin27

FRONT-R 36 A_LOUT_R ECA3 1+ 2 CD100u10EL5-RH-2 LOUT_R
FRONT-L 35 A_LOUT_L ECA4 1+ 2 CD100u10EL5-RH-2 LOUT_L
SURR-R 41
SURR-L 39
CENTER 43
LFE 44
SIDE-R 46
SIDE-L 45
LINE1-R 24 A_LINE_IN_R CA8 10u6.3X/6 LINE_IN_R
LINE1-L 23 A_LINE_IN_L CA9 10u6.3X/6 LINE_IN_L
LINE2-R 15 A_LINE2_R ECA1 1+ 2 CD100u10EL5-RH-2 LINE2_R
LINE2-L 14 A_LINE2_L ECA2 1+ 2 CD100u10EL5-RH-2 LINE2_L
MIC1-R 22 A_MIC1_R CA10 10u6.3X/6 MIC1_R
MIC1-L 21 A_MIC1_L CA11 10u6.3X/6 MIC1_L
MIC2-R 17 A_MIC2_R CA12 10u6.3X/6 MIC2_R
MIC2-L 16 A_MIC2_L CA13 10u6.3X/6 MIC2_L
CD-R 20
CD-GND 19
CD-L 18

2019/4/11
ECA1, ECA2, ECA3, ECA4 are changed to C91-1011021-N07 by PM spec
2019/4/30
ECA1, ECA2, ECA3, ECA4 are changed to C91-1011041-P01 by PM spec

2019/4/18
CA8, CA9, CA10, CA11, CA12, CA13 are changed from 4.7uF/0805 to 4.7uF/0603 by "PN_190325" rule

2019/5/2
UA1 is changed to ALC892 from ALC887 by PM spec updated.

2019/5/8
CA8, CA9, CA10, CA11, CA12, CA13 are changed from 4.7uF to 10uF by module circuit

LIN_OUT
LOUT_R RA9 75R/4 LOUT_RA 6
LOUT_L RA12 75R/4 LOUT_LA 9
FRONT_JD 7
8
AUDIO1B
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
DA1 ESD-MLVS0402L04
DA2 ESD-MLVS0402L04
N54-13F0591-F02

2019/4/10
AUDIO is changed to N54-13F0591-F02 by PM spec.

LIN_IN
LINE_IN_R RA5 75R/4 LINE_IN_RA 10
LINE_IN_L RA7 75R/4 LINE_IN_LA 13
LINE1_JD 11
12
3
AUDIO1A
15 14 16
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
CA3 ESD-MLVS0402L04
CA4 ESD-MLVS0402L04
N54-13F0591-F02

2.2k for better recording quality

MIC1
MIC1_V_L RA6 2.2K/4 MIC1_LA
MIC1_V_R RA2 2.2K/4 MIC1_RA
MIC1_R RA8 75R/4 MIC1_RA 1
MIC1_L RA3 75R/4 MIC1_LA 5
MIC1_JD 2
4
AUDIO1C
17 18
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
CA1 ESD-MLVS0402L04
CA2 ESD-MLVS0402L04
N54-13F0591-F02

for rear I/O 6port: 887VD/892:1k
for rear I/O 3port: 887VD/892:75R

[24] LOUT_LA
[24] LOUT_RA
LOUT_LA RA4 22K/4
LOUT_RA RA1 22K/4

EMI
CA6 X_C0.1u16X0402
CA5 X_1000p50N/4
CPA1 X_COPPER
CPA2 X_COPPER

Closed Codec
SENSE_A
RA17 5.1K1%/4 FRONT_JD
RA18 10K1%/4 LINE1_JD
RA16 20K1%/4 MIC1_JD

2019/5/2
LA1 is unstuffed; LA8 is added; DA3 is connected from ATX_5VSB to LDOVDD by Robert's comment

Digital Analog
ATX_5VSB
LA1 X_0R/8
LA8 0R/8
5VDUAL
DA3 X_S-RB521S30
LDOVDD
CA32 C0.1u16X0402
CA33 10u6.3X/6

CA32,CA33 close to LA1

[24] F_LINE2_L
[24] F_LINE2_R
F_LINE2_L RA33 22K/4
F_LINE2_R RA31 22K/4

DA8
LINE2_VREFO_Z
S-BAT54ALT1G
DA4
MIC2_VREFO_Z
S-BAT54ALT1G
RN15 8P4R-4.7KR

2018/5/9
RA579, RA578, RA581, RA583 are deleted and then RN15 is added by cost reduction.

MIC2_R RA28 75R/4 F_MIC2_R
MIC2_L RA24 75R/4 F_MIC2_L
LINE2_L RA34 75R/4 F_LINE2_L
LINE2_R RA32 75R/4 F_LINE2_R

JAUD1
F_MIC2_L 1 MIC GND 2
F_MIC2_R 3 MICPWR PRESENCE# 4
F_LINE2_R 5 FLINE OUTR LINE NEXT R 6 MIC2_JD
SENSE_B 7 HPON 8
F_LINE2_L 9 FLINE OUTL LINE NEXT L 10 LINE2_JD
H2X5[8]M
N31-2051411-H06
RA26 47R/4
CA35 C1000p50X4
RA27 39.2K1%/4
RA25 20K1%/4
DA5 DA6 DA7 DA9 ESD-MLVS0402L04

Close to Front panel
For HDA/AC97 front cable.

Varister --> cap for cost down
D0G-2710510-I05
D0G-2950500-SI0
Close to Jack

MICRO-STAR INT'L CO.,LTD.
Title: Audio ALC892-1
Size: Document Number: MS-7C52..
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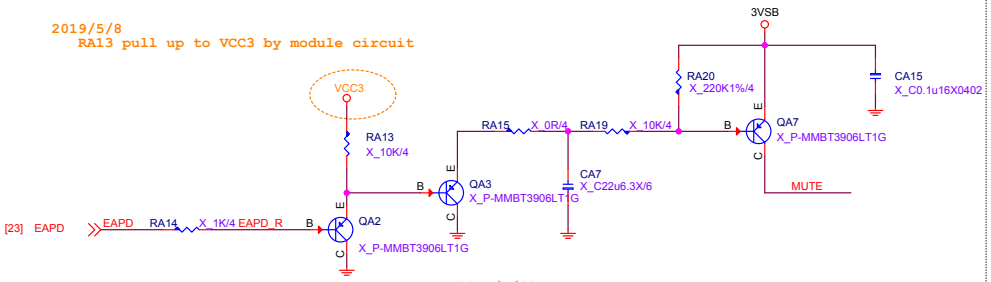
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

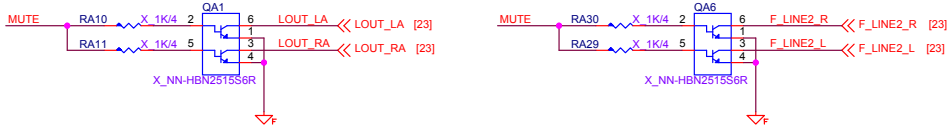
2019/5/8
RA13 pull up to VCC3 by module circuit



2019/5/23
RA15 is changed from 1Kohm to 0ohm by module circuit

Digital

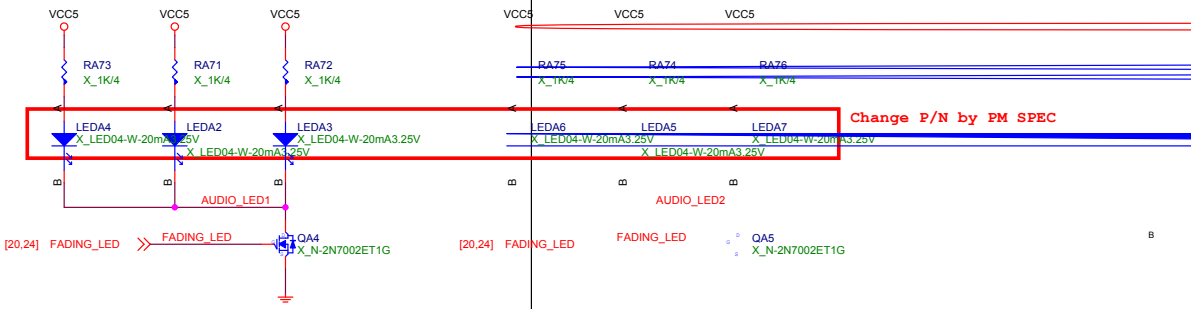
Analog

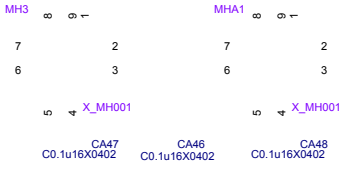


2019/7/25
RA14, RA13, QA2, QA3, RA15, CA7, RA19, RA20, QA7, CA15, RA10, RA11, QA1, RA30, RA29, QA6 are unstuffed by PM request(2019/7/24)

20181203
Remove Audio LED,
RA73、RA71、RA72、RA74、RA75、RA76、LEDA4、LEDA2、LEDA3、LEDA6、LEDA5、LEDA7、QA4、QA5 unstuff.

使用测光LED





2019/4/26
The pin1 of MH3, MHA1 are changed to GND by CND rule

2019/7/19 (1.1 only)
The pootprint of MH3, MHA1 are changed from HOLES_4S to Holes_4s_CND by Eric's comment(2019/7/17)

MICRO-STAR INT'L CO.,LTD.

Title	Audio ALC892-2	
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USB

2019/4/10
About PS2 circuit move to the page 21

[15] PM_USB12+ → L1 → PMUSB12+
[15] PM_USB12- → L1 → PMUSB12-
4P2R-0R0402

[15] PM_USB13+ → L2 → PMUSB13+
[15] PM_USB13- → L2 → PMUSB13-
4P2R-0R0402

D9
PMUSB12+ / PMUSB12- / PMUSB13+ / PMUSB13-
ESD-AOZ8906CI

USB20_LAN
LAN_USB1A
PMUSB12- / PMUSB12+ / PMUSB13- / PMUSB13+
UP / DOWN
RJ45_USBX2_LEDX2_TX-GIGA-RH-5

2019/4/10
LAN_USB1A is changed to N58-22F0731-F02 by PM spec.

VCC5
R92 10K/4
Q16 NN-2N7002DW
USB20_LAN → R93 10K/4 → G1
D2 → PM_OC7# [15,27]
S2
S1

USB20_LAN
C65 C0.1u16X0402

2019/4/30
EC2 is changed to C71-56106K1-AO5 by PM spec updated
2019/5/3
EC2 is deleted by cost reduction

2019/5/3
R2401, R2394, U25, R2395, Q154, R2399, R2396, R2397, Q155, R2400, R2398 are added by Ryan's comment

USB Power

~~8.9A~~ 9.4A

2019/5/8
F1, F2 are changed to D08-0101700-P16 by Ryan's comment

5V_FUSB
F2 F-SPR-P110-HF → PS2_VCC1 ~~1.5A (USB2.0*2+PS2)~~ 1A (PS2 * 2)

F1 F-SPR-P110-HF → USB20_LAN 1A (USB 2.0 * 2) LAN_USB1

EC12 CD560u6.3SO-HF-5
F3 F-SPR-P260T → USB30_VCC1 1.8A USB1

EC30 CD560u6.3SO-HF-5
F4 F-SPR-P260T → USB30_VCC3 1.8A USB2

2019/5/3
EC12, EC30 are moved from page26 by cost reduction

5V_FUSB
C71 X_C0.1u16X0402
C72 X_C0.1u16X0402
C73 X_C0.1u16X0402

ATX_5VSB
[31] DIMM_SBDRV → DIMM_SBDRV → G
Q137 P-P06P03LCGA
S
D
C755 X_C0.1u16X0402

[31] DIMM_VCCDRV → DIMM_VCCDRV
Q134
N-SM4503NHKPC-TRG_DFN5x6-8-HF
D03-4503N0C-ST8
VCC5

F5 F-SPR-P260T → USB20_VCC1 2A JUSB1, JUSB2

EC37 CD560u6.3SO-HF-5
F7 F-SPR-P260T → USB30_VCC2 1.8A JUSB3

2019/5/3
EC37 is moved from page27 by cost reduction

APU_USB_OC

USB_XOR0 R2401 X_0R/4 APU_OC0#
3VSB
R2394 10K/4
U25
USB_XOR0
APU_OC0# [6,26]
[5,6,36,37,41] TYPE1_CPU_SEL
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
SN74LVC1G86DCKR_SC70-5-RH

VCC5
R2395 10K/4
Q154 NN-2N7002DW
R2399 15K1%/4 → G2
D2 → USB_XOR0
D1
S2
USB30_VCC1 → R2396 10K/4 → G1
USB1

VCC5
R2397 10K/4
Q155 NN-2N7002DW
R2400 15K1%/4 → G2
D2
D1
S2
USB30_VCC3 → R2398 10K/4 → G1
USB2

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

MICRO-STAR INT'L CO.,LTD.
Title: USB Rear PS2+USB2.0
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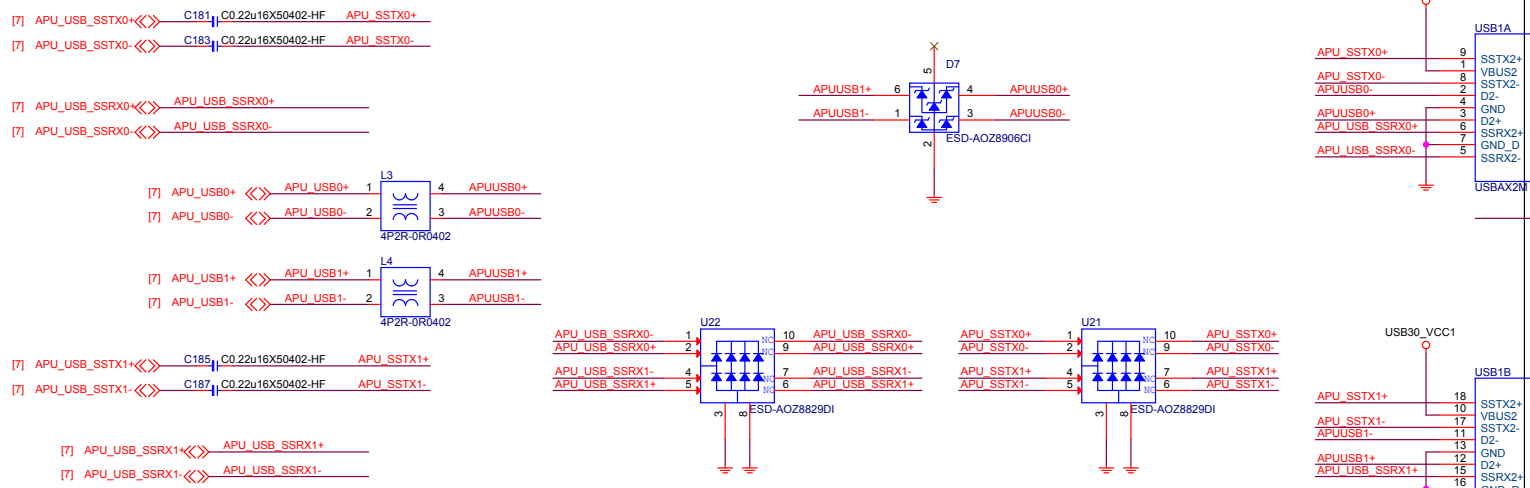
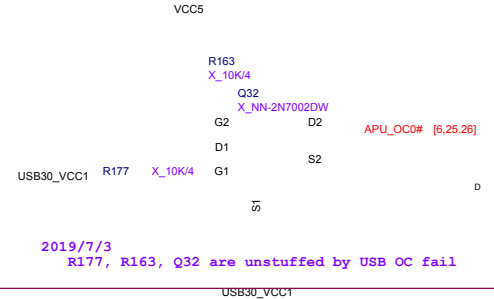
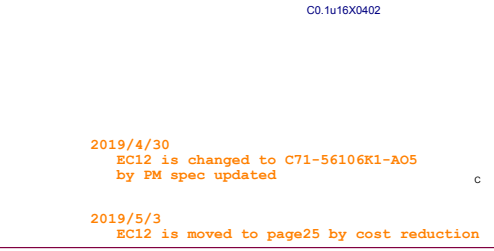
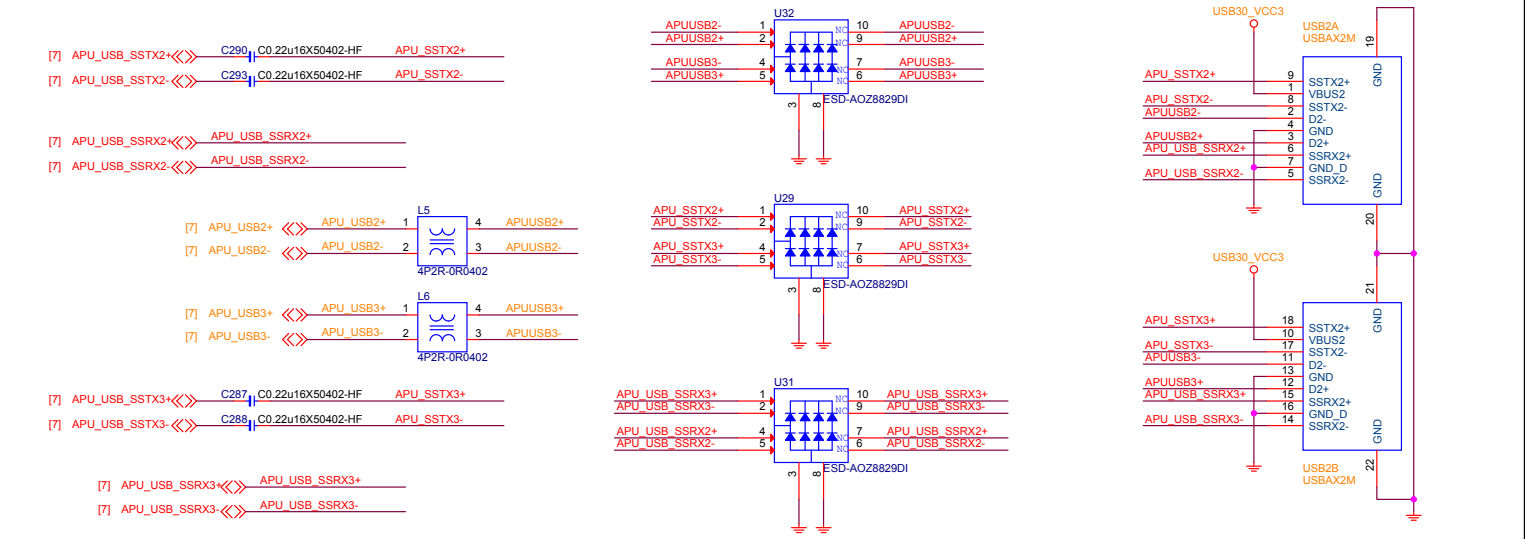
USB 3.1 GEN1



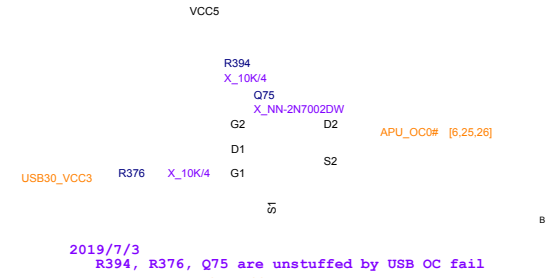




USB3.1 GEN1



2019/4/10
USB2 is changed to N53-18M0091-F02 by PM spec.



MICRO-STAR INT'L CO.,LTD.

Title: USB Rear LAN+USB3.1 GEN1

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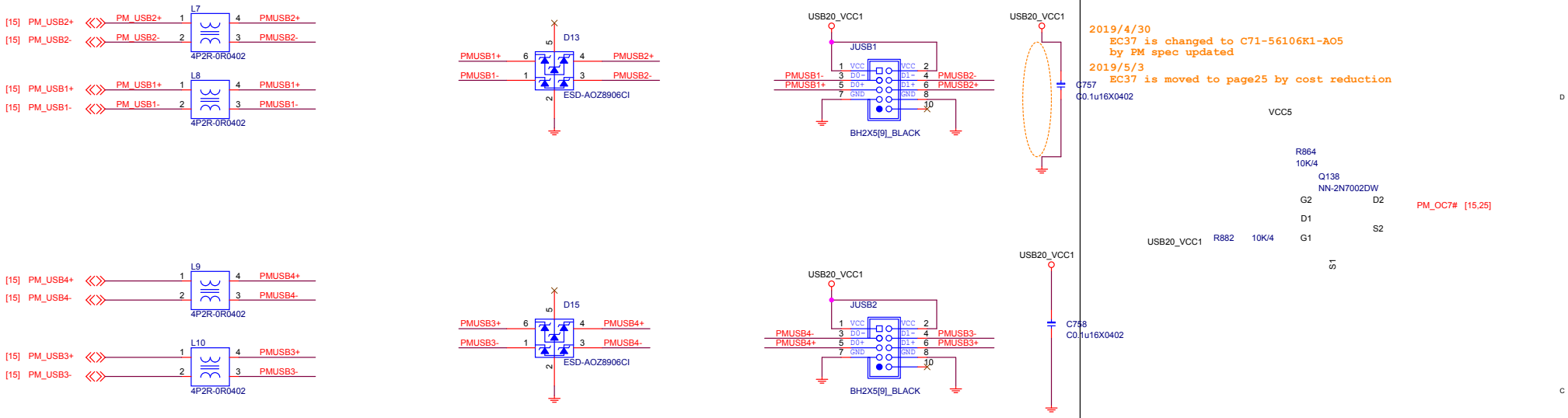
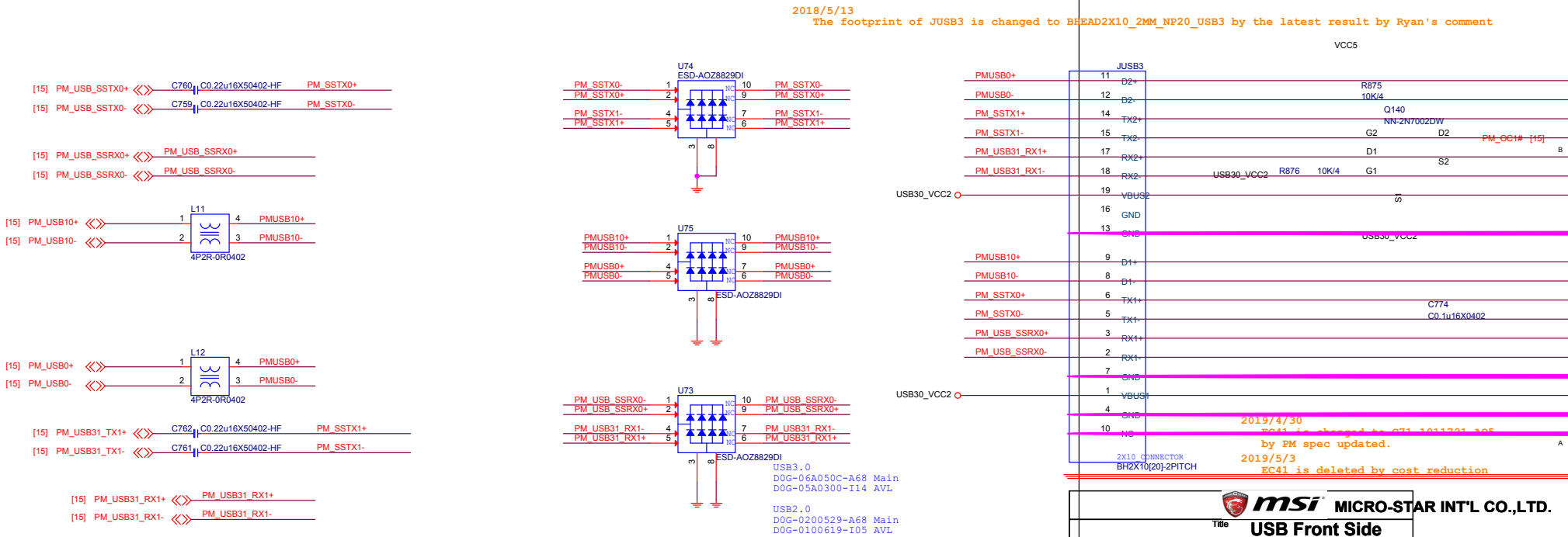
Front USB2.0



Vinafix.com

Front USB3.1 GEN1



MICRO-STAR INT'L CO.,LTD.

Title: USB Front Side

Size: Document Number: MS-7C52..

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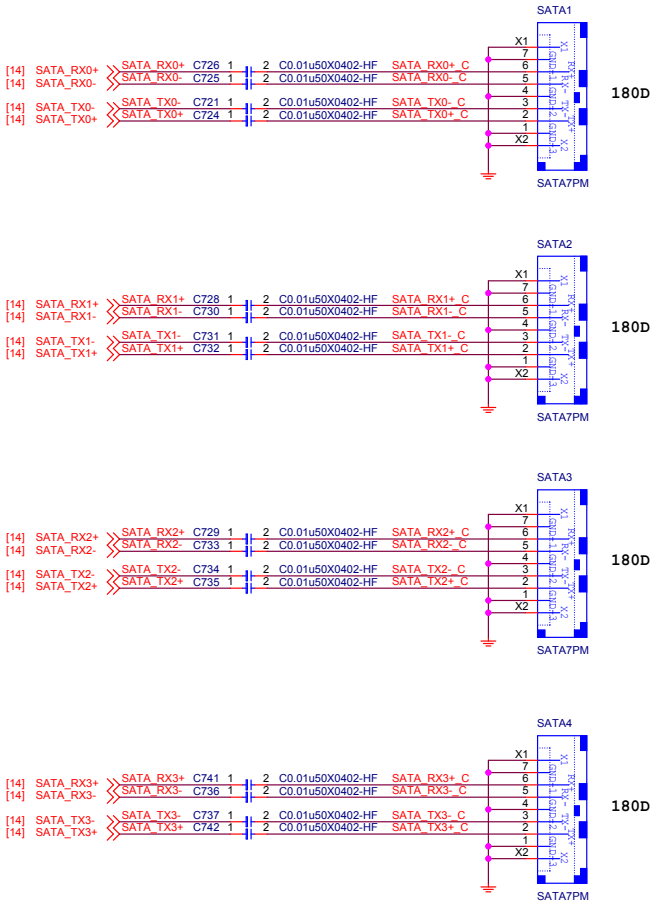
SATA Connector



MICRO-STAR INT'L CO.,LTD.

Title: SATA Connector

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DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

[5] DP1_CLKN_APU
[5] DP1_CLKP_APU
[5] DP1_TX2N_APU
[5] DP1_TX2P_APU
[5] DP1_TX1N_APU
[5] DP1_TX1P_APU
[5] DP1_TX0N_APU
[5] DP1_TX0P_APU

C154 C0.1u16X0402 DVI_TXC- R165 499R1%/4
C159 C0.1u16X0402 DVI_TXC+ R201 499R1%/4
C149 C0.1u16X0402 DVI_TXD2- R194 499R1%/4
C171 C0.1u16X0402 DVI_TXD2+ R164 499R1%/4
C169 C0.1u16X0402 DVI_TXD1- R207 499R1%/4
C143 C0.1u16X0402 DVI_TXD1+ R160 499R1%/4
C144 C0.1u16X0402 DVI_TXD0- R150 499R1%/4
C141 C0.1u16X0402 DVI_TXD0+ R192 499R1%/4

DVI_DATA

VCC3
Q71
N-2N7002ET1G

DVI_VGA_5V
R169 2.2K/4
Q84 NN-2N7002DW
VCC3 G2 D2 DVI_DDC_DATA_R
DVI_DDC_CLK_R D1
VCC3 G1 S2 DP1_AUXN [5]
S1
[5] DP1_AUXP

DVI_VGA_5V
R193 2.2K/4

2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

VCC3
C489 X_C0.1u16X0402

HPD

VCC3
DVI_VGA_5V
R203 10K/4
R191 10K/4
[5] DP1_DP_HPD
Q28
C173 X_C0.01u50X0402-HF
DVI_HOT_DET_R
R171 10K/4 DVI_HOT_DET
NN-CMKT3904
R168 100KR0402
C148 C0.01u50X0402-HF

2019/4/10
VGA_DVI1 is changed to N58-43F0111-EB6 by PM spec.

U6
DVI_TXD2- DVI_TXD2+ DVI_TXC+ DVI_TXC-
ESD-AOZ8829DI
DVI_TXD2- DVI_TXD2+ DVI_TXC+ DVI_TXC-

U5
DVI_TXD0- DVI_TXD0+ DVI_TXD1- DVI_TXD1+
ESD-AOZ8829DI
DVI_TXD0- DVI_TXD0+ DVI_TXD1- DVI_TXD1+

DVI_VGA_5V

VGA_DVI1B
X3
Shell-3 Shell-5 G1 Shell-6 G2
16 DVI_TXD2- DATA2
17 DVI_TXD2+ DATA2
18 SHIELD-1
19 DATA4
20 DATA4
21 DVI_DDC_CLK_R DDCCLK
22 DVI_DDC_DATA_R DDCDATA
23 NC
24 DVI_TXD1- DATA1
25 DVI_TXD1+ DATA1
26 SHIELD-2
27 DATA3
28 DATA3
29 VCC5
30 GND5
31 DVI_HOT_DET HPDET
32 DVI_TXD0- DATA0
33 DVI_TXD0+ DATA0
34 SHIELD-3
35 DATA5
36 DATA5
37 SHIELD-4
38 DVI_TXC+ CLK
39 DVI_TXC- CLK
X4
Shell-7 G3 Shell-4 Shell-8 G4
VGA_DVI-RH-32

DVI_VGA_5V

C155
C0.1u16X0402

U4
DVI_DDC_CLK_R 6 4 DVI_DDC_DATA_R
DVI_HOT_DET 1 3
ESD-AOZ8906CI

DVI_HOT_DET
DVI_DDC_CLK_R
DVI_DDC_DATA_R

C147 X_10p50N/4
C146 X_10p50N/4
C151 X_10p50N/4

For EMI
DVI_TXD0- DVI_TXD0+ R151 X_243R1%/4
DVI_TXD1- DVI_TXD1+ R158 X_243R1%/4
DVI_TXC- DVI_TXC+ R200 X_243R1%/4
DVI_TXD2- DVI_TXD2+ R162 X_243R1%/4

MICRO-STAR INT'L CO.,LTD.

Title	DVI Connector	
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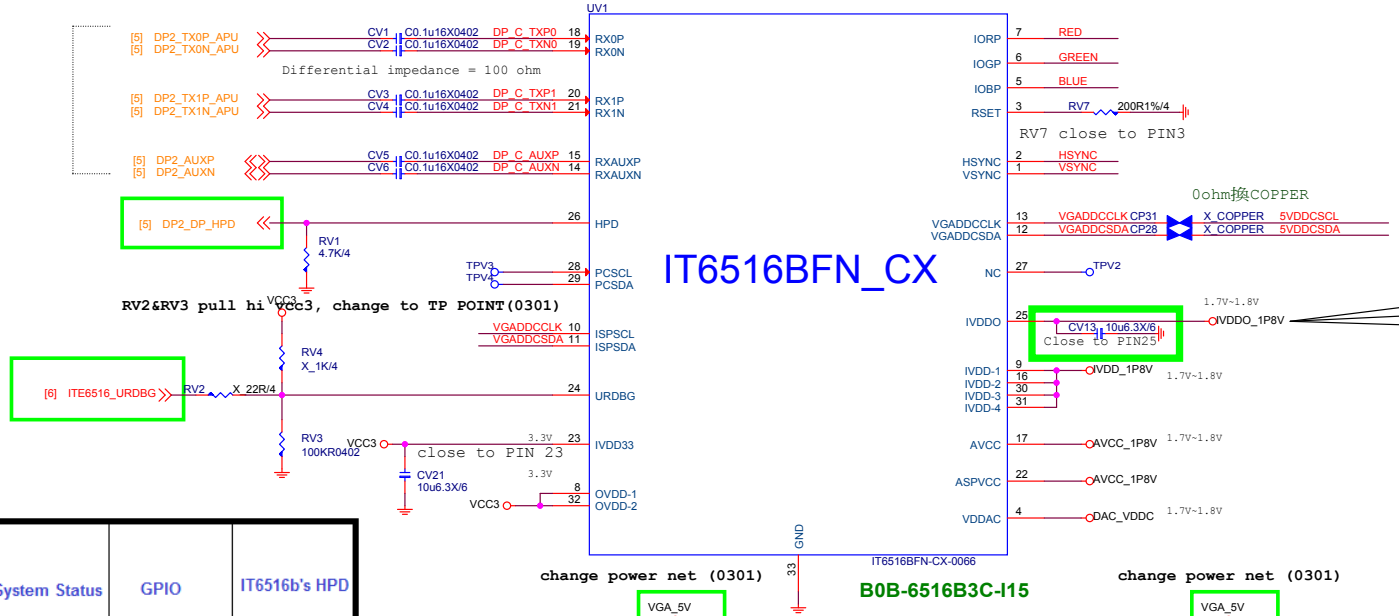
2019/5/8

Note: 7C52-02S are all no unstuff expect for DV1, FSV1, CV38, VGA_DVI1

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

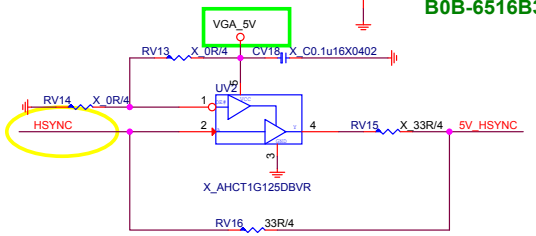
20181203:
UV1 change to B0B-6516B3C-I15, FW改善省電.



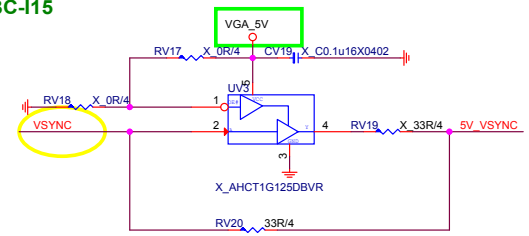
B0B-6516B3C-I15

System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

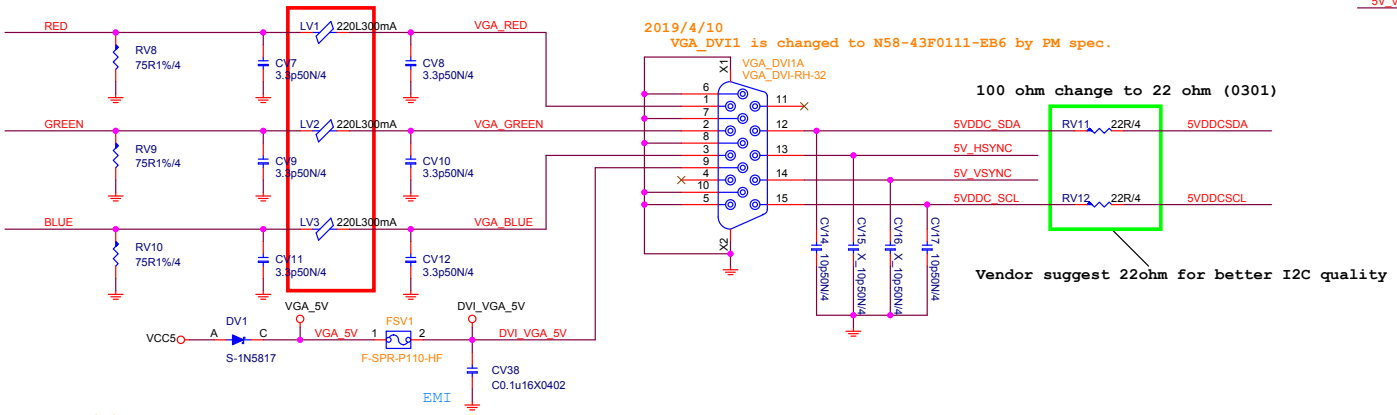
change power net (0301)



change power net (0301)



P/N Change for VESA 1.2 SPEC PASS



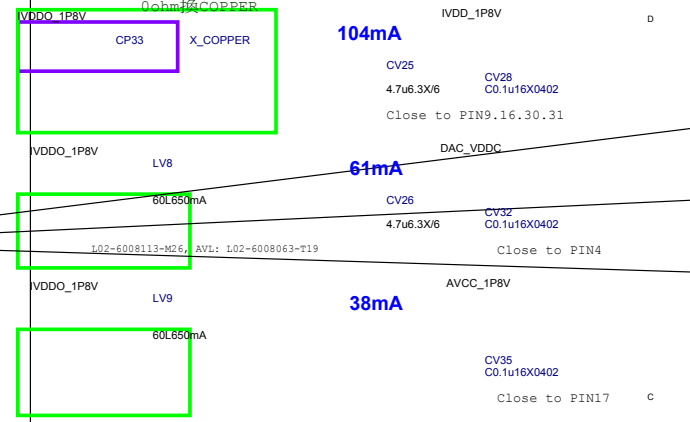
2019/4/10
VGA_DVI1 is changed to N58-43F0111-EB6 by PM spec.

100 ohm change to 22 ohm (0301)

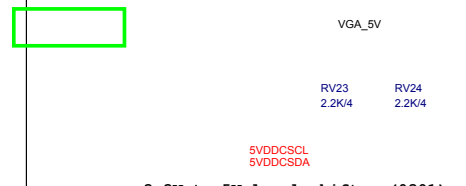
Vendor suggest 22ohm for better I2C quality

2019/5/6
FSV1 is changed to D08-0101700-P16 by Ivy's comment

add D-sub function 0225



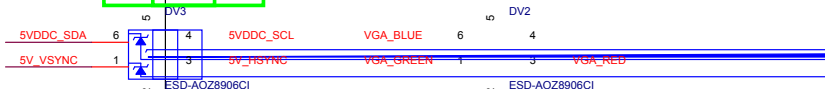
change power net (0301)



remove 3.3V-to-5V level shifter (0301)

PIN 5 NC 20160525

PIN 5 NC 20160525



DV3 Close to VGA connector
AVL:D0G-45B0510-I14

DV2 Close to VGA connector
AVL:D0G-45B0510-I14

MICRO-STAR INT'L CO.,LTD.

Title: DP to VGA ITE6516

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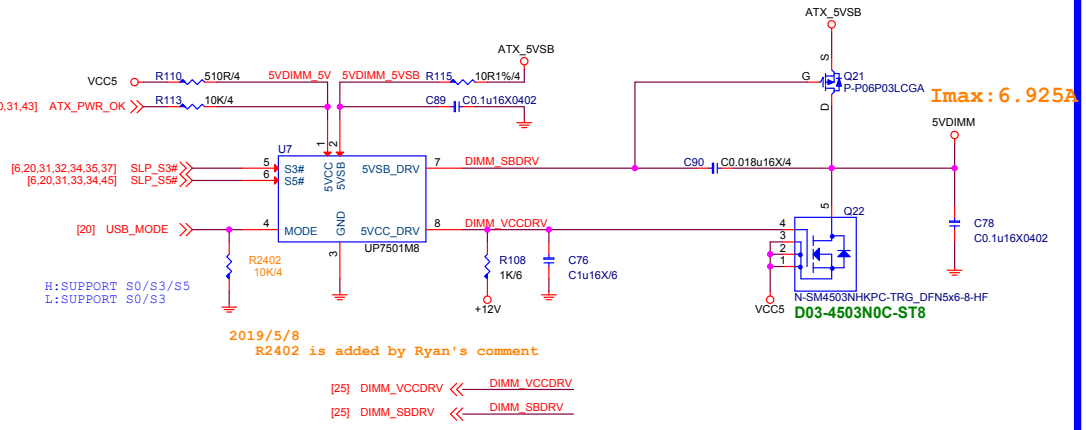
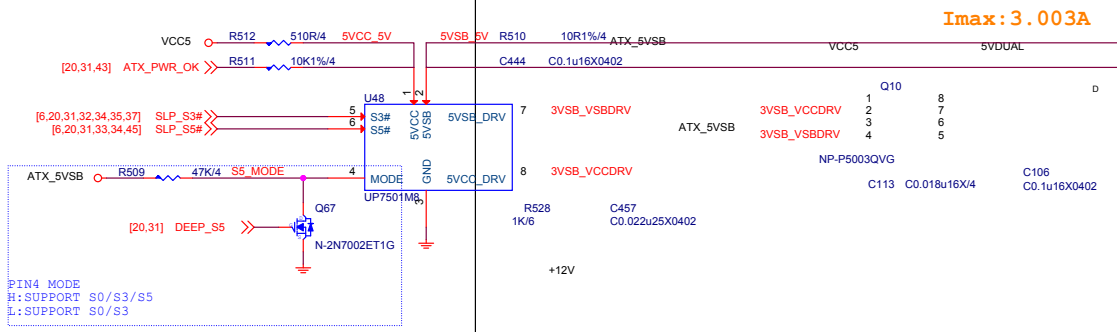
5VDIMM FOR DDR



2019/5/8
R2402 is added by Ryan's comment

[25] DIMM_VCCDRV
[25] DIMM_SBDRV

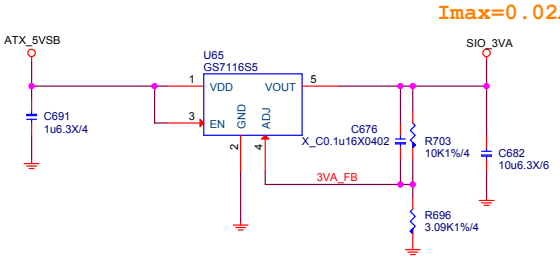
5VDUAL For 3VSB、CPU 1.8V 、 VDDP



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

2019/4/17
R60, C79, Q9, R55, C67 are deleted by Ryan's comment

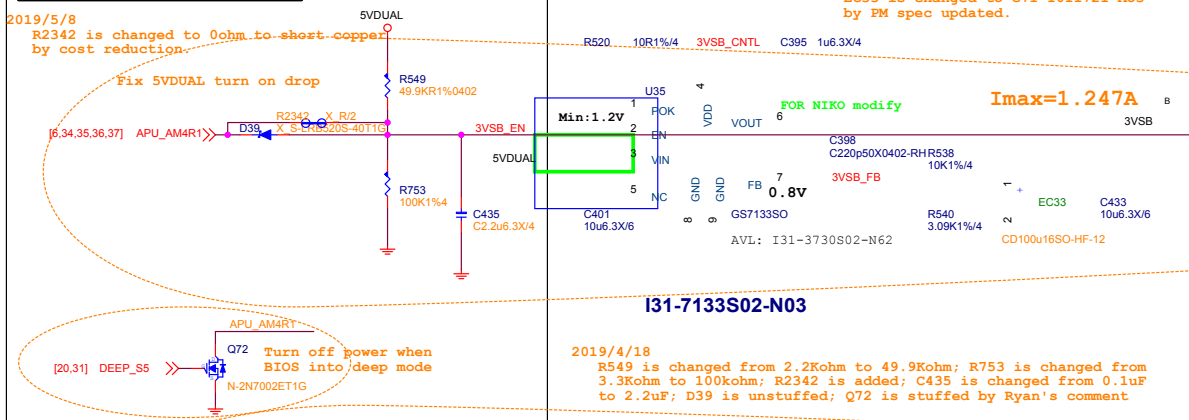
SIO_3VA



3VSB cost down

2019/5/8
R2342 is changed to 0ohm to short copper by cost reduction.

Fix 5VDUAL turn on drop



2019/4/30
EC33 is changed to C71-1011721-AO5 by PM spec updated.

I31-7133S02-N03

2019/4/18
R549 is changed from 2.2Kohm to 49.9Kohm; R753 is changed from 3.3Kohm to 100kohm; R2342 is added; C435 is changed from 0.1uF to 2.2uF; D39 is unstuffed; Q72 is stuffed by Ryan's comment

2019/4/18
R59, Q2, R62, Q81, R114 are deleted by Ryan's comment

MICRO-STAR INT'L CO.,LTD.

Title: ACPI uPI-5VDIMM&3VSB

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Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

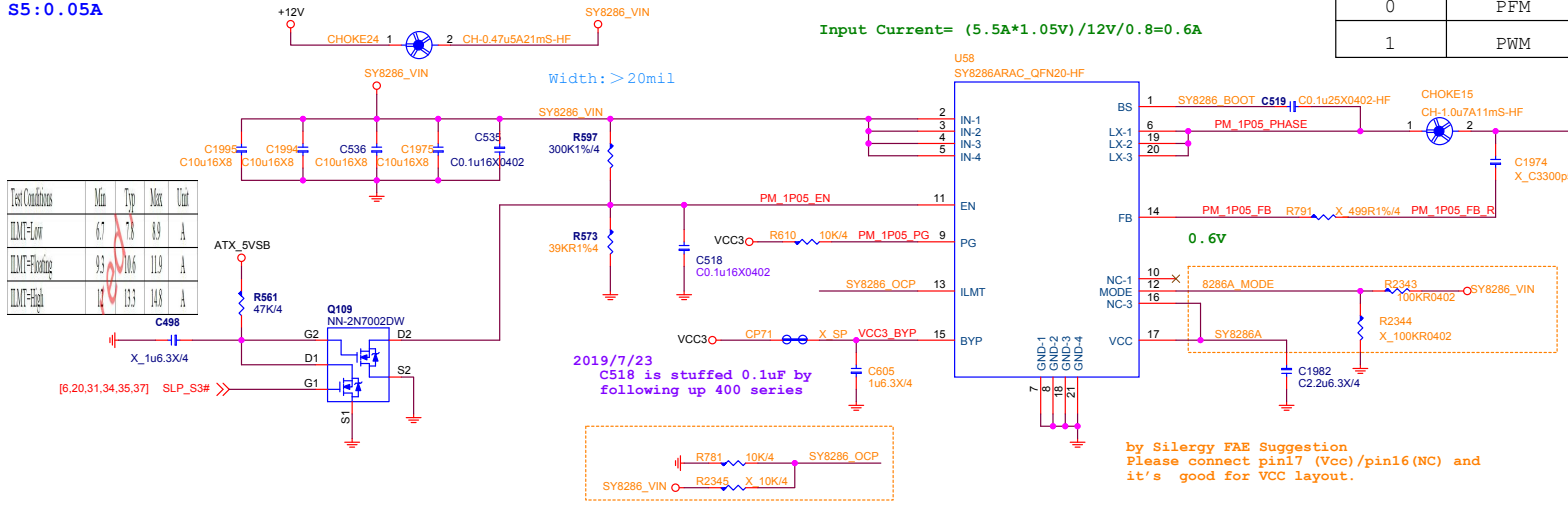
2019/4/12
U58 is changed to SY8288; CHOKE15 is changed to 1R0; L22, L39 are deleted; CHOKE24, C1975, CP71, C605, C1977, C1512, R610 are added; R573 is changed to 39kohm; C519 is changed to 0.1uF; R582 is changed to 1.33Kohm; R781, R791, C1974 are reserved by Ryan's comment

2019/4/12
U58 is changed to SY8286; R2345, R2343, R2344 are added by Ryan's comment

8286A_MODE	Operating mode
0	PFM
1	PWM (Force CCM Mode)

OCP=12A Imax:5.5A
1.05V@5.5A

Input Current= (5.5A*1.05V)/12V/0.8=0.6A



Test Conditions	Min	Typ	Max	Unit
ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A

2019/7/23
C518 is stuffed 0.1uF by following up 400 series

by Silergy FAE Suggestion
Please connect pin17 (Vcc)/pin16(NC) and it's good for VCC layout.

R1
R575 1K1%/4
PM_1P05_FB

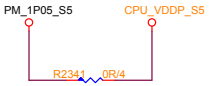
R2
R582 1.33KR1%0402

Vout = Vref * (1 + (R1/R2))
= 0.6 * (1 + (1K/1.33K))
= 1.051V

2019/4/23
CP9 is deleted by Ryan's comment

FOR Promontory 1.05V_S5

0.05A



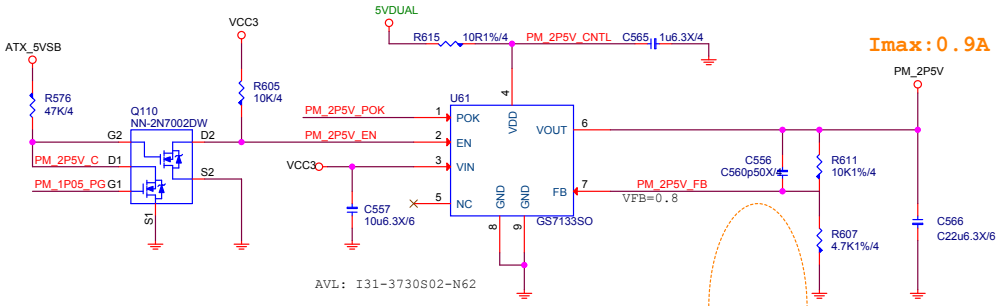
2019/4/16
R2341 is added; R663, C636, C629, U63, R675, R672, C645 are unstuffed by Ryan's comment

2019/4/25
R663, C636, C629, Q73, U63, C646, R675, R672, C645 are deleted by Ryan's comment

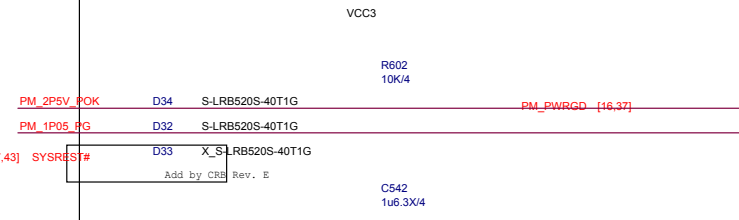
teknisi indonesia

Promontory-2.5V

2.5V; 900mA



2019/4/23
CP10 is deleted by Ryan's comment



MSI MICRO-STAR INT'L CO.,LTD.

Title: Promontory-1.05V/GS7133-2.5V

Size: Document Number: MS-7C52.. Rev: 11

Date: Wednesday, July 24, 2019 Sheet 32 of 52

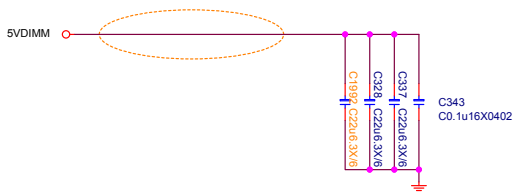
2DIMM :1.12A FOR DDR VPP2.5V

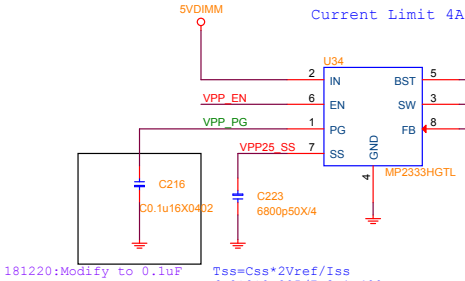
2019/4/12
U34 is changed from MP2143 to MP2333; L29, C443 are deleted and C1992 is added by Ryan's comment

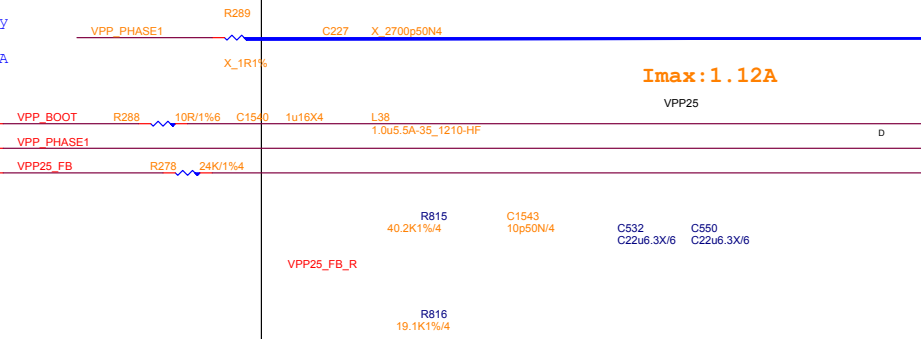
Input Current= Iout*SQRT((Vout/Vin)*(1-Vout/Vin))=1.5A

Switch Frequency
Default 1.2MHz
Current Limit 4A

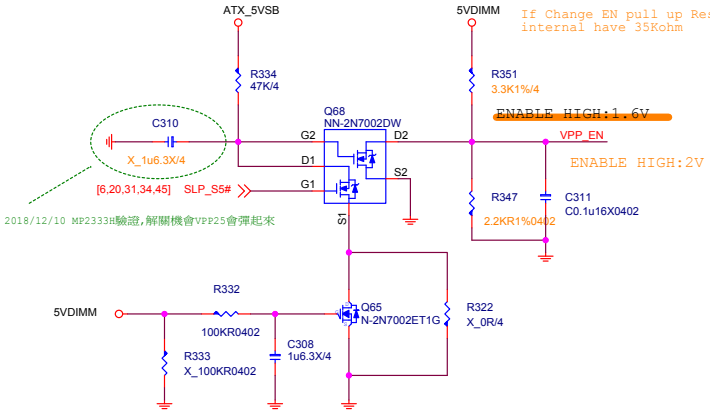
Imax:1.12A







Tss=Css*2Vref/Iss
6.8*2*0.805/7.3=1.499ms



2019/4/12
R351 is changed from 2.2Kohm to 100Kohm; R347 is changed from 3.3Kohm to 82kohm; C310 is unstuffed by MP2333 solution

2019/5/7
R351 is changed from 100kohm to 3.3Kohm; R347 is changed from 82Kohm to 2.2Kohm by Ryan's comment

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 40µA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V VIN, I_{Zener} = (12V - 2.8V) / (604kΩ + 35kΩ) = 14µA.

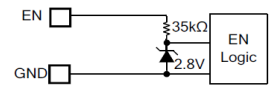
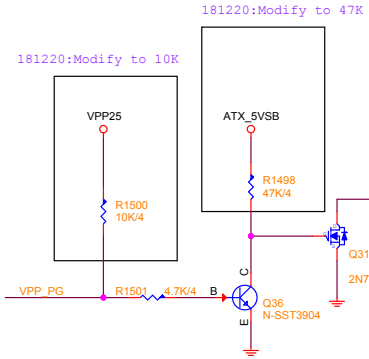
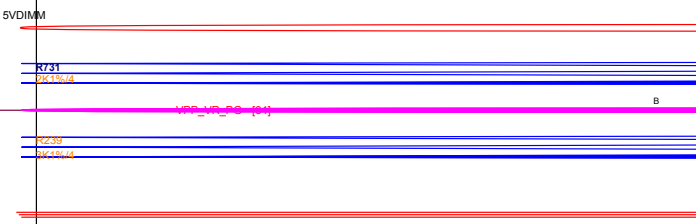


Figure 2: Zener Diode between EN and GND





2019/4/12
R1500, R1501, R1498, Q36, Q31, R731, R239 are added by MP2333 solution

MICRO-STAR INT'L CO.,LTD.

Title: DDR PWR VPP25

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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT

R178: 280K，OCP實測28.8A.

Choose a current limit setting resistor via the following equation :

$R_{LIMIT} = I_{LIMIT} \times R_{DS(ON)} \times 10/5\mu A$

Iin=(Iocp*Vout)/(0.8*Vin)
=(27.105A*1.21)/(0.8*5)
=8.199A

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 20.85 * SQRT(0.183436)
= 8.929936A

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

Iocp =20.85A*1.3=27.105A
Rlimit =Iocp*Rdson(low)x10/5u
=27.105x3.9m*10/5u
=211.419Kohm

VID	Reference Voltage (V)
H	0.675
L	0.75

2V

f:400KHz

By layout modify

2019/4/11
EC5 is deleted ;C115 is stuffed, C1538 is stuffed by Ryan's comment

2019/4/30
EC6 is changed to C71-56106K1-AO5 by PM spec updated

OCP:27.5A
Imax: 20.85A

Close to PIN19

I32-8231A0C-R11

Default = 1.21V

$V_{VDDQ\ (Valley)} = V_{REF} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$

Vout=Vrefx(1+R1/R2)
=0.75x(1+1/1.62)
=1.213v

2019/4/17
R181 is changed from 1.24kohm to 1.62Kohm by same as 400 series from Ryan's comment

$L = \frac{t_{ON} \times (V_{IN} - V_{VDDQ})}{L_{IR} \times I_{LOAD(MAX)}}$

L=tON*(VIN-VDDQ)/(LIR*ILOAD(MAX))
tON=636.4456ns
LIR:20%~40%
L:0.63uH~1.27uH????

Imax:20.85A
1.2V

0.1uFx1 per dimm

20181031
VCC_DDR由上2下2改成上1下1.

SM4503NHKPC-TRG Rdson(low)
4.5V:3.9mohm~5.1mohm

UPI VOLTAGE CONSOLE
0x26:RH=18K,RL=13K

2019/4/30
EC18, EC19 are changed to C71-56106K1-AO5 by PM spec updated.

MICRO-STAR INT'L CO.,LTD.
Title: DDR Power-RT8231AGQW
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FOR CPU 1.8V S5

0.5A

FOR VCCP_SOC_S5

0.9A

0.5A + 2.0A +
0.9A =3.4A

CPU_1P8V_S5

CPU: VDD_18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A

CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A

2019/4/12
L19, R479, R469, C423, C394 are deleted; R451 is changed from 2.2Kohm to 10Kohm; R445 is unstuffed; R472 is unstuffed; R1503, C1544, C1545, C1546, R1505 C1983 are added; U42 is changed to MP2329; R1504, R1508, C1551 are reseverd; C387 is changed from 0.1uF to 22uF by Ryan's comment

Input Current=
(2.75A*1.8V)/5V/0.8=1.2375A

5VDUAL
C1983 C434
C430
C0.1u16X0402
C22u6.3X6
C22u6.3X6

CPU_1P8_BST、CPU_1P8_BST_R >50 mils.

Imax:4.7A

CPU_1P8_BST
C1545
0.22u16X4
L17
CH-1.0u7A11mS-HF
CPU_1P8_S5
U42
VIN
SW
BST
EN
PG
FB
VCC
AGND
PGND-1
PGND-2
PGND-3
CPU_1P8_PHASE
R1504
C1546 C220p50X0402-RH
R1505
X_887KR1%0402-HF
499R1%/4
R448
1K1%/4
R449
487R1%/4
C372
C377
C387
C22u6.3X6
C22u6.3X6
C22u6.3X6
CPU_1P8_S5_FB
C419
C0.1u16X0402
R472
X_47K/4
CPU_1P8_S5_EN
[37,41] CPU_1P8_S5_PG
R1503
100KR0402
VFB=0.6V
VCC=3.65V
C1544
1u6.3X/4
MP2329CGG-Z_QFN11-HF
CP8
X_COPPER
CPU_1P8_S5_FB_R [41]
Vfb:
=10uA(sinking)*1KR=10mV

[6,31,34,36,37] APU_AM4R1
D21
S-LRB520S-40T1G
CPU_1P8_S5_EN

Vout = Vref * (1 +(R364/R363))
= 0.6 * (1 +(1K/0.487K))
= 1.83V OK

3VSB
R451
10K/4
ENABLE HIGH:1.4V
ENABLE HIGH:1.6V
CPU_1P8_S5_EN
R445
X_3.3K1%/4
C400
C0.1u16X0402

CPU_1P8_PHASE
R1508
X_1R1%
C1551
X_2700p50N4
reserve snubber

2019/4/18
Q82 is deleted by Ryan's comment

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FOR CPU 1.8V S0

2.0A

ATX_5VSB
R379
47K/4
C352
X_1u6.3X/4
Q77
NN-2N7002DW
[6,20,31,32,34,37] SLP_S3#
[34,37] DDR_PWRGD

VCC3
R389
10K/4
Q89
NN-2N7002DW
[36] CPU_VDDP_EN
CPU_1P8_EN
C357
C0.1u16X0402

DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8

Imax:2A

CPU_1P8_S5
U33
C1514
C1515
C22u6.3X/6
X_C22u6.3X/6
VIN1-1
VIN1-2
VIN2-1
VIN2-2
ON1
ON2
VBIAS
VOUT1-1
VOUT1-2
VOUT2-1
VOUT2-2
CT1
CT2
GND
Thermal Pad
TPS22976DPUR
C1516
C0.1u16X0402
CPU_1P8_EN
VCC3
CPU_1P8
C342
C4700p50X0402
CPU_1P8

Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)

C1517
X_C22u6.3X/6
C339
X_C22u6.3X/6
C332
1u6.3X/4

MICRO-STAR INT'L CO.,LTD.
Title: CPU Power 1P8V-MP2147
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CPU_VDDP

CPU: VDDP@8.5A

Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A

L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH

Isat: 22A

0.9V@8.5A
OCP=13A Imax:8.5A

CPU_VDDP need to confirm 1.05V

L04-47B7930-M26

Internal 3.3V Input

VFB=0.6V

R823、R344、C822 stuff for stability

2019/4/25
CHOKE13 is changed to L04-68B7350-T15
by Ryan's comment

20180822
fix PG glitch when VCC3 ramp up, C386 stuff.

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

Vout=Vref*(1/[R450*(1/R438+1/R1492)]+1}
=0.6*{1/[1.33k*(1/1k+1/1m)]+1}
=1.0506v

CPU_VDDP_S5

CPU: VDDP_S5@1A

2019/7/19
D28 is unstuffed by 7B86 v4.0 refered

2019/4/18
Q98 is deleted by Ryan's comment

2019/4/16
R490, C436, Q95, R464 are unstuffed by Ryan's comment

Imax:1A
0.9V@1A

0.9W

Vout = Vref * (1+R489/R488)
= 0.8 * (1+1K/3.16K)
= 1.053v

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

Title	CPU Power VDDP-RT8125E
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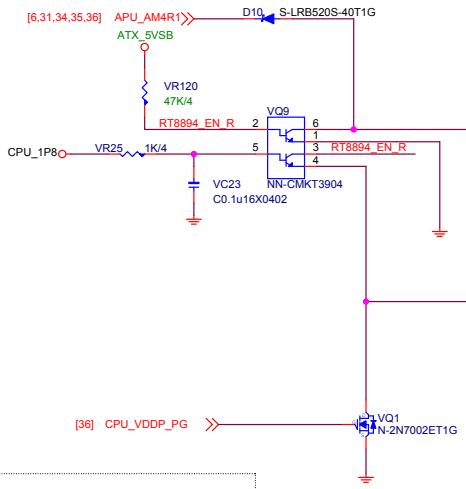
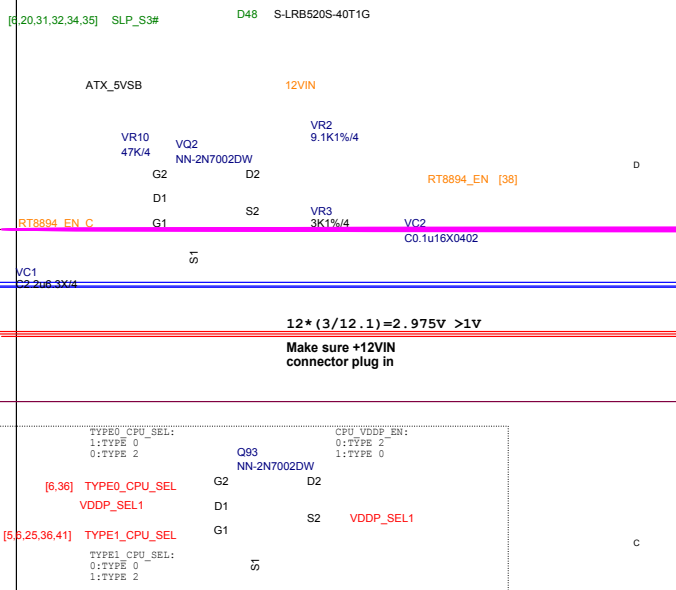
VRM_Enable circuit

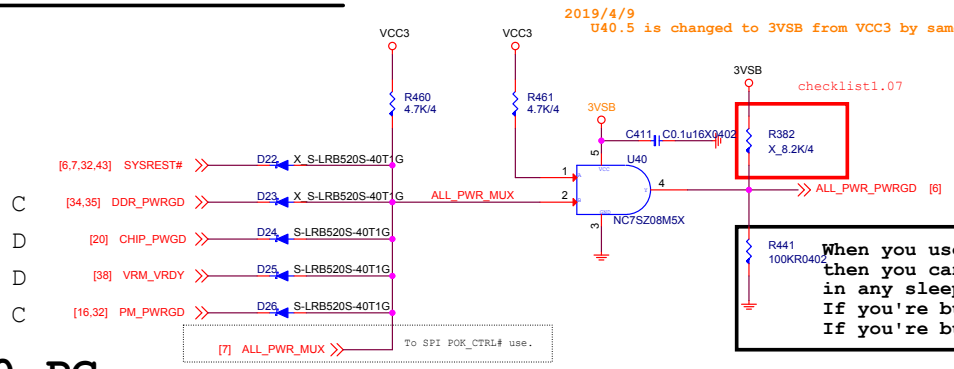




CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

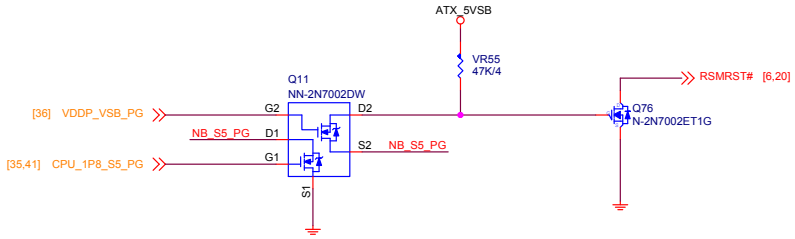
ALL POWER GOOD MUX



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



2019/5/20
Q11.G2 and Q11.G1 are swapped by Ryan's comment

MICRO-STAR INT'L CO.,LTD.

Title: CPU PWR-IR3599

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Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

2019/4/10
VRM solution passed to follow up PM spec
2019/4/12
VR15, VR12, VR29, VR24, VR36, VR57, VR33, VR41, VR46, VR47, VR84, VR63, VR73 are changed to 0ohm to short copper; VC28, VC29 are unstuffed by vendor's suggestion
2019/4/25
VR34 is changed to 46.4Kohm; VR32 is changed to 620ohm; VC10 is changed to 150pF, VC24 is changed to 47pF; VR44 is changed to 39Kohm; VR45 is changed to 6.04Kohm; VC16 is changed to 220pF; VR85 is changed to 910ohm; VR64 is changed to 1.62Kohm; VR80 is changed to 910ohm; VR79 is changed to 1.62Kohm; VR82 is changed to 10.7Kohm; VR66 is changed to 280ohm; VR70 is changed to 14Kohm; VR71 is changed to 110ohm; VR83 is changed to 2.26Kohm; VR81 is changed to 100ohm; VR16, VR60 are changed to 110Kohm; VR76 is changed to 60.4Kohm; VR121 is changed to 2.1Kohm; VR78 is changed to 22.1Kohm; VR122 is changed to 133ohm; VR137 is added to 316ohm; VR69 is changed to 2Kohm; VR138 is added to 191ohm; VR65 is changed to 22.6Kohm; VR68 is changed to 200ohm; VR74 is changed to 16Kohm; VR75 is changed to 3.48Kohm; VR72 is changed to 9,53Kohm; VR73 is changed to 10ohm by Vendor's suggestion.

2019/4/18
VC3, VC27 are changed from 1uF/6.3V to 1uF/16V; VC5 is changed from 0603 type to 0402 type by "PN_190325" rule

2019/5/8
VR21 is changed to 100ohm to short copper by cost reduction.

2019/5/8
VR36, VR41 are deleted by cost reduction

2019/5/8
VR59, VR42, VR37, VR40 are changed to 0ohm to short copper by cost reduction.

2019/5/8
VR86 is unstuffed by Ryan's comment

2019/7/8
VR85 is changed from 910 ohm 750ohm and VR64 is changed from 1.62Kohm to 1.27Kohm

2019/7/3
VR80 is changed from 910ohm to 1.3kohm and VR79 is changed from 1.62Kohm to 2.21kohm

2019/6/11
VR70 is changed to 12.1Kohm; VR71 is changed to 130ohm; VR82 is changed to 10Kohm; VR66 is changed to 430ohm; VR83 is changed to 2.8Kohm; VR81 is changed to 110ohm; VR34 is changed to 41.2Kohm; VR32 is changed to 1.27Kohm by VCORE OCP=155A

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation

SMB Address: 0X40

VCORE IccMAX: 125A =>OCP=>155A
VCC_NB IccMAX: 75A =>OCP=> 90A

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Title	CPU Power RT8894 3+2 Phase
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VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

2019/4/10
VRM passed to follow up PM spec

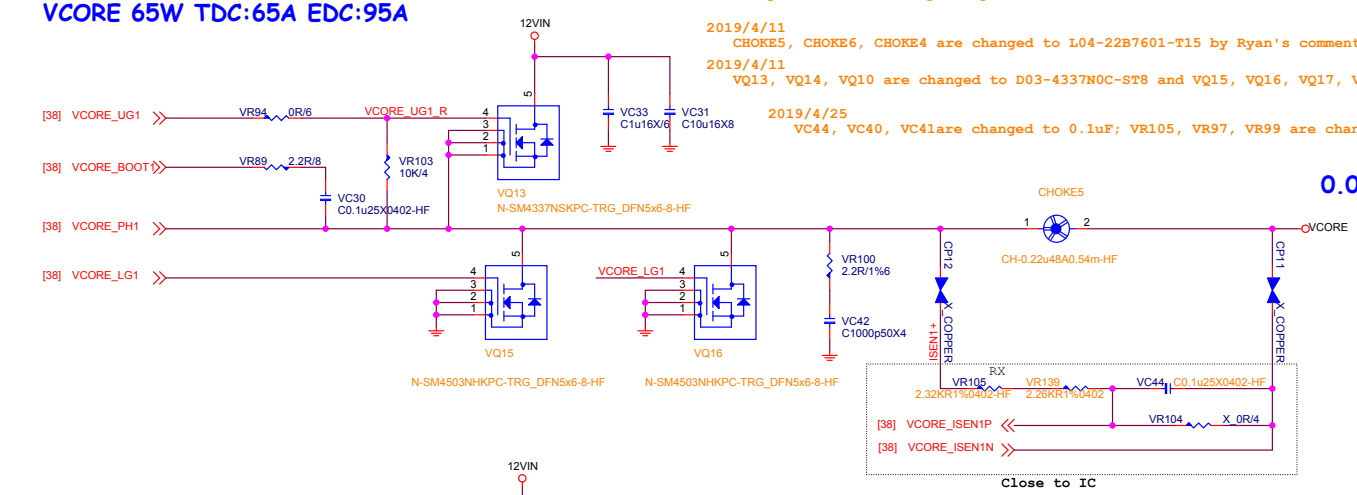
2019/4/11
CHOKE5, CHOKE6, CHOKE4 are changed to L04-22B7601-T15 by Ryan's comment

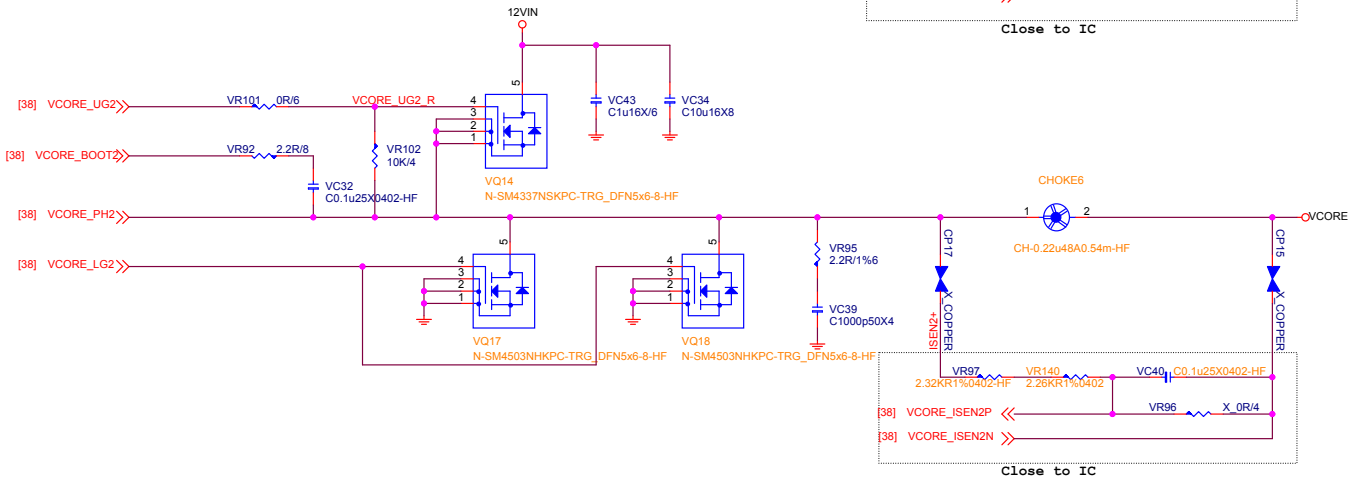
2019/4/11
VQ13, VQ14, VQ10 are changed to D03-4337N0C-ST8 and VQ15, VQ16, VQ17, VQ18, VQ11, VQ12 are changed to D03-4503N0C-ST8 by Ryan's comment(same as 7A36-3.0)

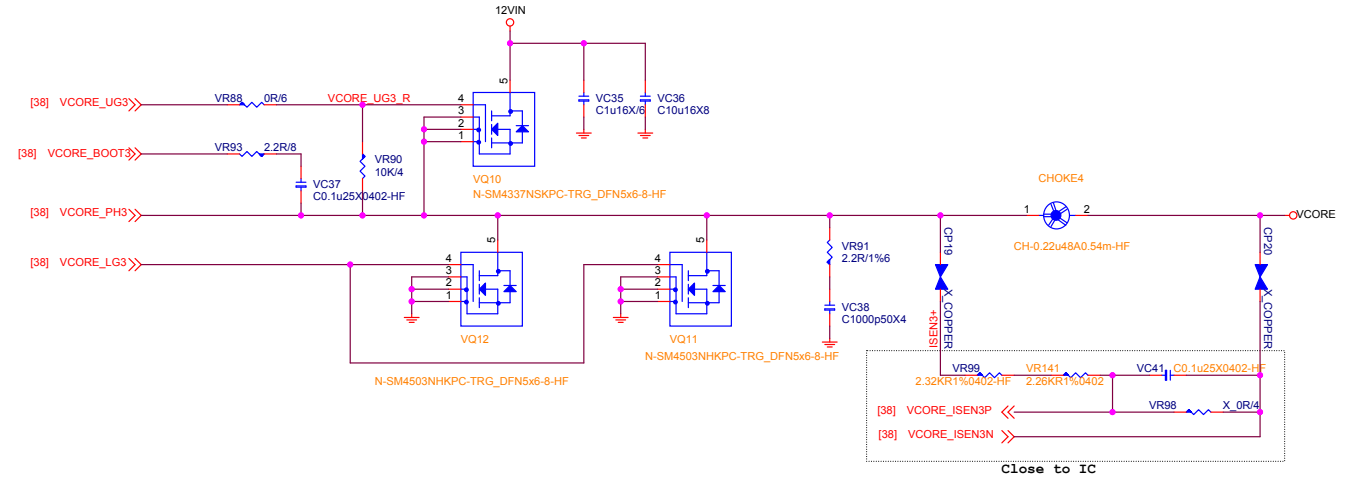
2019/4/25
VC44, VC40, VC41are changed to 0.1uF; VR105, VR97, VR99 are changed to 2.32Kohm; VR139, VR140, VR141 are added to 2.26Kohm by vendor's suggestion

0.00625V~1.55V

Imax:125A







VCORE

EC40	1+	2	CD560u6.3SO-HF-5
EC42	1+	2	CD560u6.3SO-HF-5
EC45	1+	2	CD560u6.3SO-HF-5
EC46	1+	2	CD560u6.3SO-HF-5
EC47	1+	2	CD560u6.3SO-HF-5
EC48	1+	2	CD560u6.3SO-HF-5

2019/4/30
EC40, EC42, EC45, EC46, EC47, EC48 are changed to C71-56106K1-A05 by PM spec updated

MICRO-STAR INT'L CO.,LTD.

Title: CPU Power Phase 1-3

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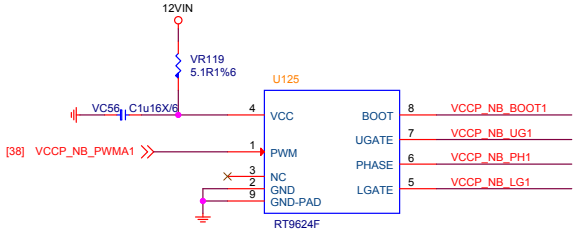
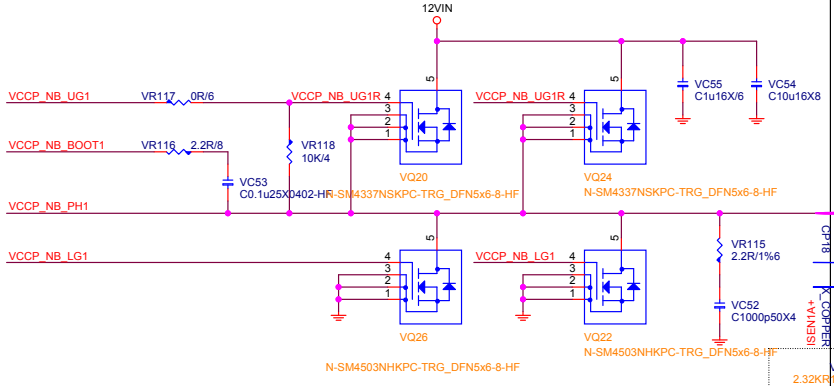
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

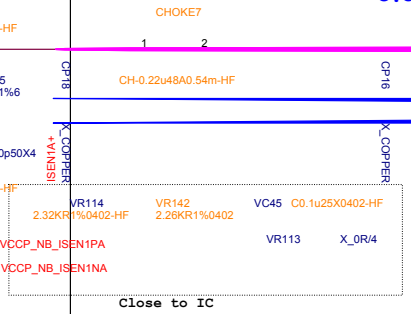
2019/4/10
VRM passed to follow up PM spec

2019/4/11
CHOKE7, CHOKE8 are changed to L04-22B7601-T15 by Ryan's comment

2019/4/11
VQ20, VQ24, VQ21, VQ25 are changed to D03-4337N0C-ST8 and VQ22, VQ26, VQ19, VQ23 are changed to D03-4503N0C-ST8 by Ryan's comment(same as 7A36-3.0)

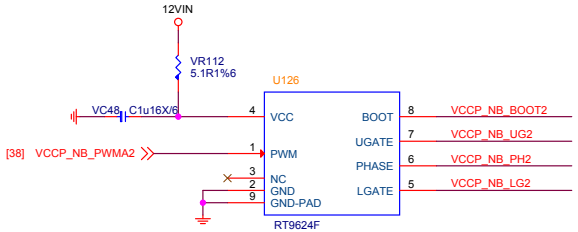


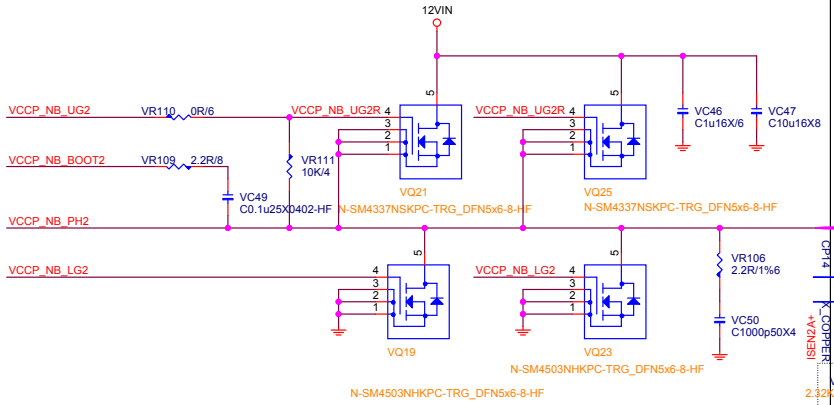


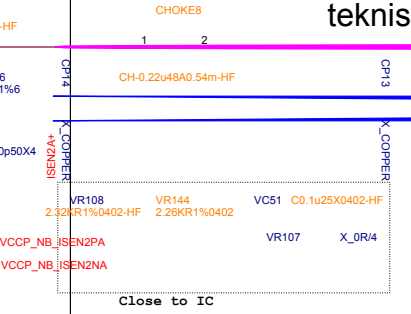


0.00625V~1.55V
Imax:75A

2019/4/25
VC45, VC51 are changed to 0.1uF; VR114, VR108 are changed to 2.32Kohm; VR142, VR144 are added to 2.26Kohm by vendor's suggestion







VCCP_NB

EC43 1+ 2 CD560u6.3SO-HF-5
EC44 1+ 2 CD560u6.3SO-HF-5
EC50 1+ 2 CD560u6.3SO-HF-5

2019/4/22
EC49 is deleted by Ryan's comment

2019/4/30
EC43, EC44, EC50 are changed to C71-56106K1-A05 by PM spec updated

MICRO-STAR INT'L CO.,LTD.
Title: CPU Power NB Phase 1-2
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Date: Wednesday, July 24, 2019
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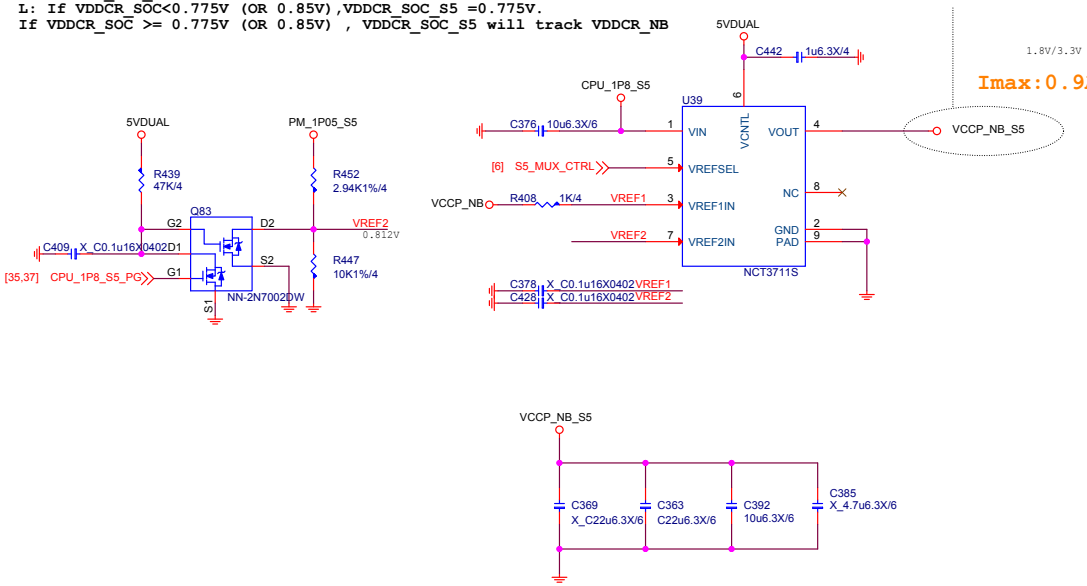
FOR VCCP_SOC_s5
0.9A

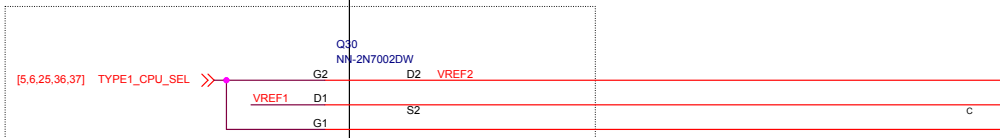
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)Bristol Ridge TYPE0





CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

2019/4/23
U62, R616, R614 are deleted by Ryan's comment

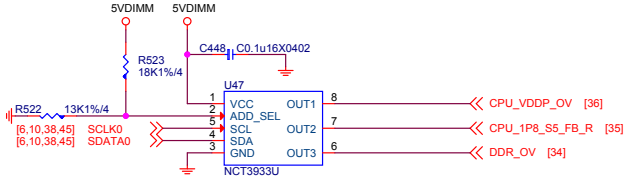
除非超壓對功能有任何幫助,否則不上NCT3933與開超壓選項

2019/4/11
U64, C570, R618, R621 are deleted by Ryan's comment

0x26:RH=18K,RL=13K

0x20:RH=10K,RL=OPEN

0x2A:RH=OPEN,RL=10K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

MICRO-STAR INT'L CO.,LTD.

Title: CPU Power NB Sw/NCT3933 OV

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uP6273 CURRENT SENSE

20181107
cost down-remove 12VIN OCP

2019/4/11
R1083, R1080, C973, R1079, U101, C914, C915, R1060, C919, C916, R1071, R1072, C917, C918, R1066, R43, Q6, Q12, R61 are deleted by Ryan's comment

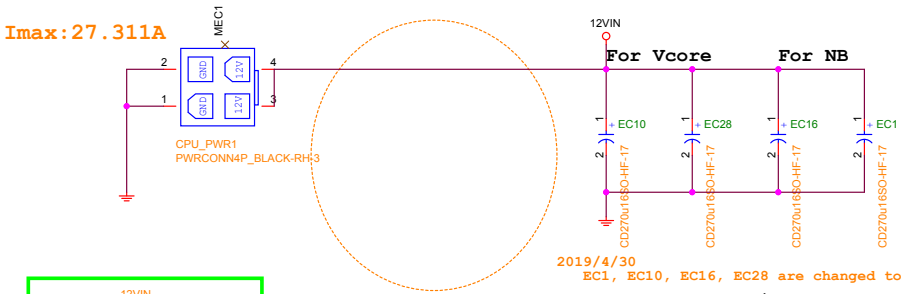
VCORE EDC MAC 125A
NB EDC MAX75A

CPU POWER CONNECTOR

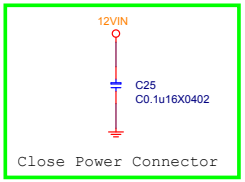
2019/4/11
CPU_PWR1 is changed to N93-04M0441-H06 by PM spec.

2019/4/11
CHOKE1, SP1, SP2 are deleted by Ryan's comment

Imax:27.311A



2019/4/30
EC1, EC10, EC16, EC28 are changed to C71-27117Y1-A05 by PM spec updated.



Irms = Iout * SQRT{D/N- (D)^2]}

CORE:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=3
=125A*SQRT(0.0388-0.0136)
=19.8A

NB:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=2
=75A*SQRT(0.0583-0.0136)
=15.8A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.5	> output Vcore
D	=	0.125	

I o = Icore(max)*0.8			
I core(max)	=	125	> Vcore current
I avg.	=	100	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	3	phase
I ripple	=	11.02396	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	3	pcs.

For Vcore

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.2	> output Vcore
D	=	0.1	

I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	9	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

For NB

MICRO-STAR INT'L CO.,LTD.

Title: CPU PWR CONN

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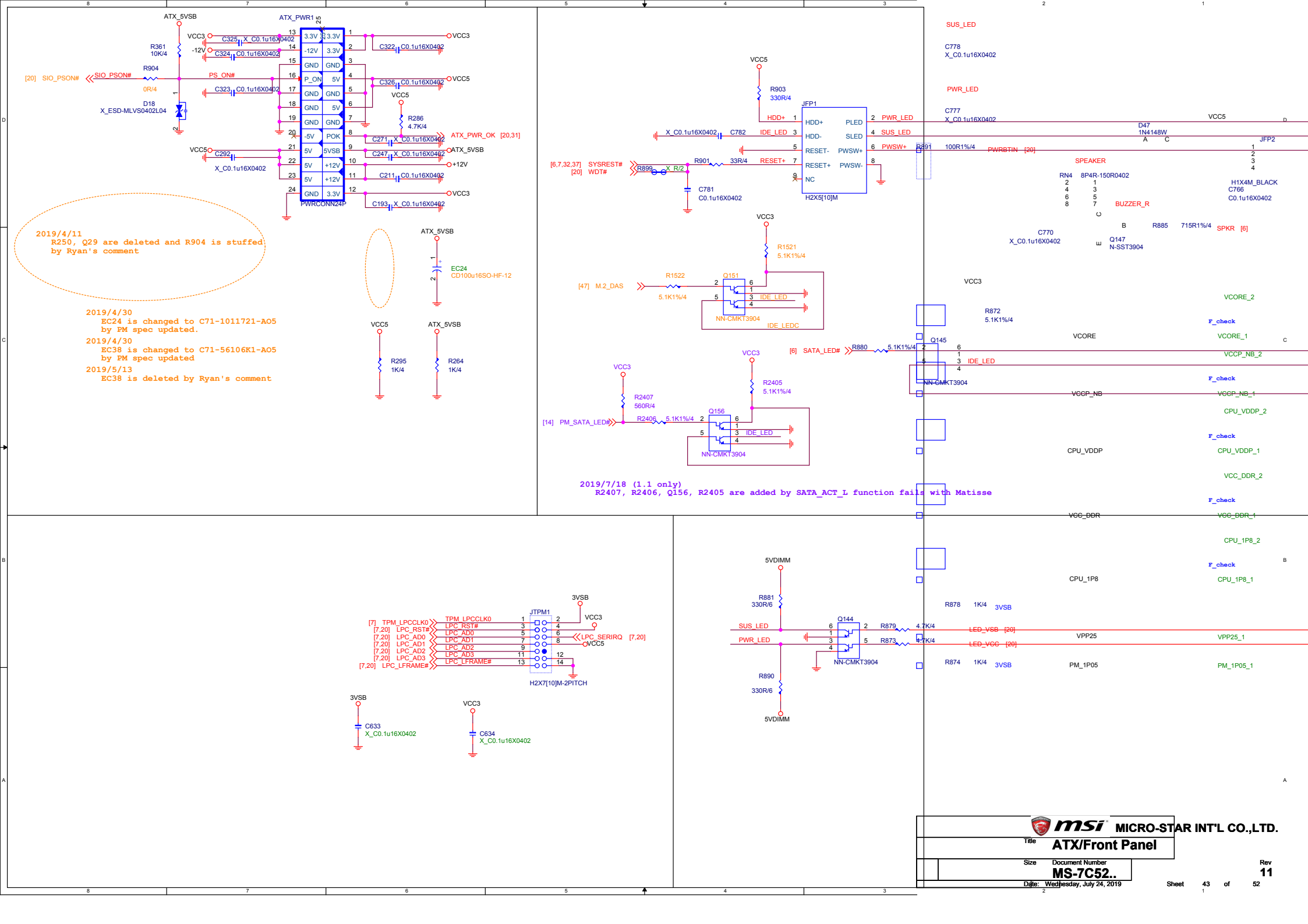

MICRO-STAR INT'L CO.,LTD.

Title: ATX/Front Panel

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Rev: 11

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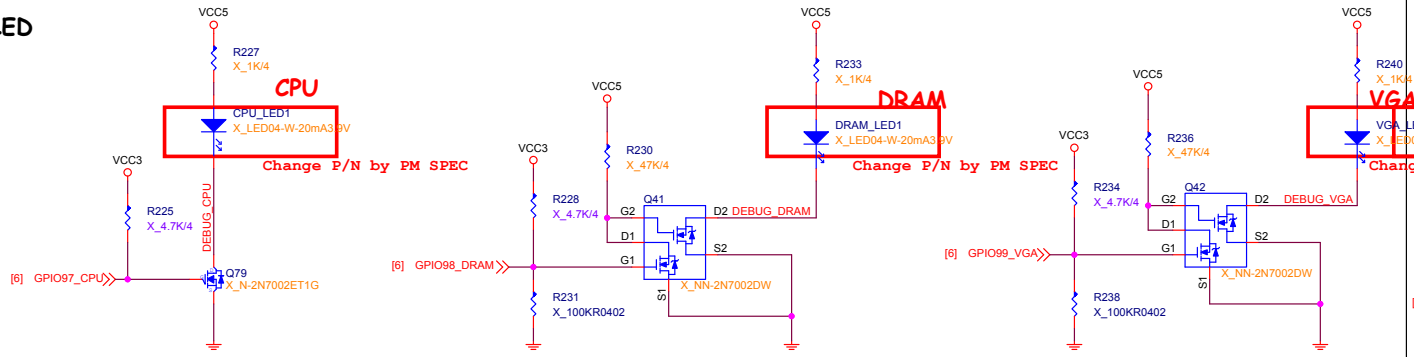
EZ Debug LED



LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

2019/5/2
R227, CPU_LED1, Q79, R223, DRAM_LED1, Q41, R230, R240, VGA_LED1, Q42, R236, R248, BOOT_LED1, Q45, R244 are unstuffed by PM spec updated.

2019/6/21
R225, R228, R234, R241 are unstuffed by PM request

LED Control by SIO

1.0 SPEC Removed

DDR LED

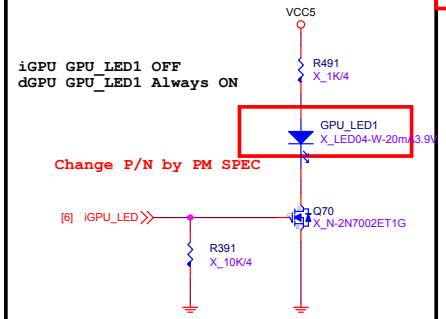
Removed P/N by PM SPEC

PCI Express LED Control

Removed P/N by PM SPEC

2019/6/21
R491, GPU_LED1, Q70, R391 are unstuffed by PM request

AM4 APU Detect LED Circuit



Bottom LED

Removed P/N by PM SPEC

LED	x16	x8	x4
PCIE2	Red	White	White

LED \ GPIO	EGPIO95	EGPIO96
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

MSI MICRO-STAR INT'L CO.,LTD.

Title: ALL LED Control

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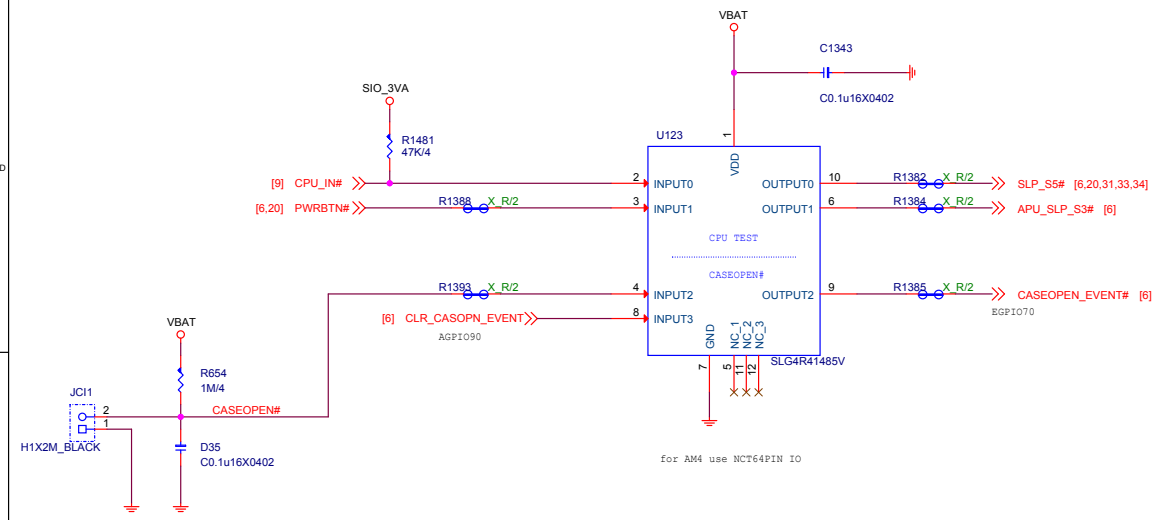
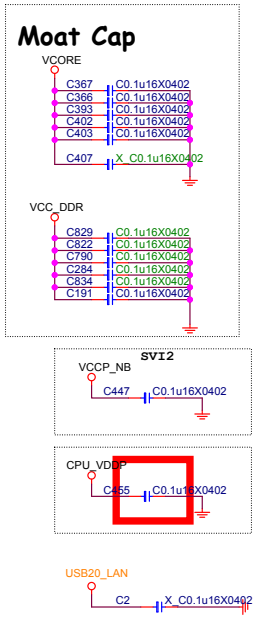
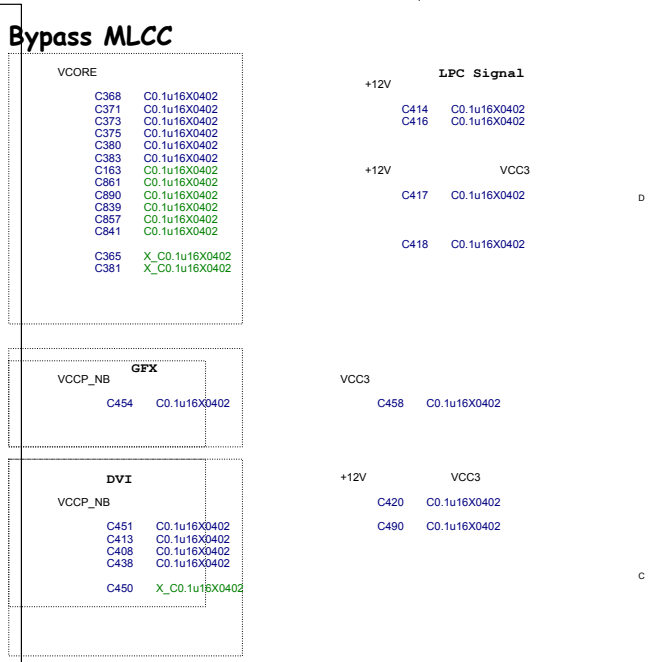
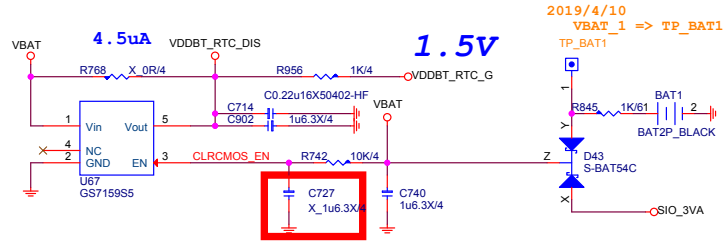


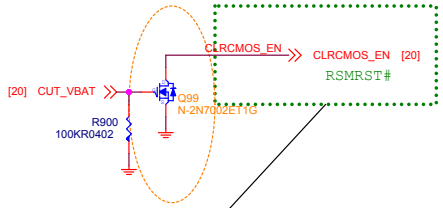


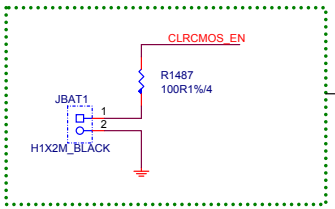


RTC & Clear CMOS Circuit

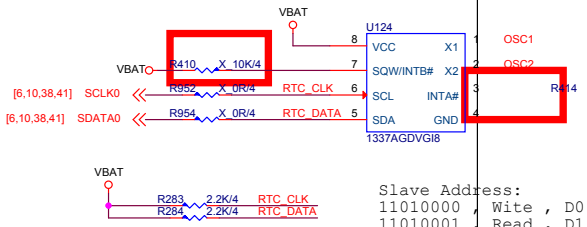


2019/4/11
Q99 is changed to D03-7002E89-005 and R960, R25, C744 are deleted by Ryan's comment

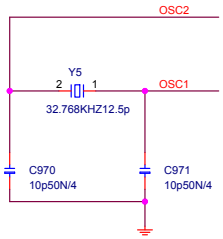




20181029
update to G3 clean CMOS.



Slave Address:
11010000 , Wite , D0
11010001 , Read , D1



MICRO-STAR INT'L CO.,LTD.

Title: RTC Circuit

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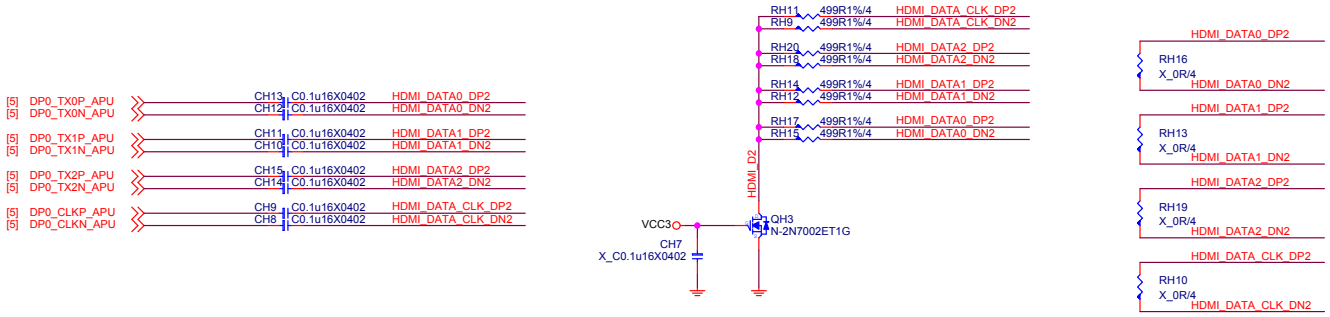
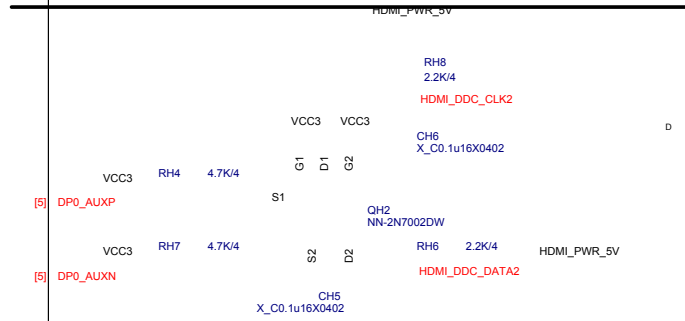
HDMI CONNECTOR

2019/4/10
HDMI is added by PM spec.

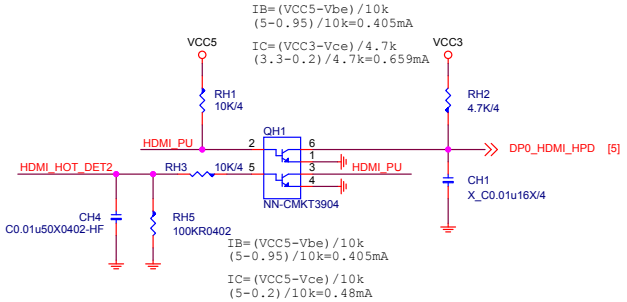
For HDMI 1.4



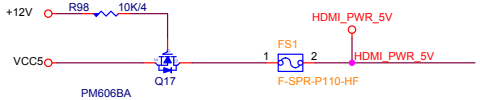
AUX Level Shifter



HPD Circuit



Connector Power

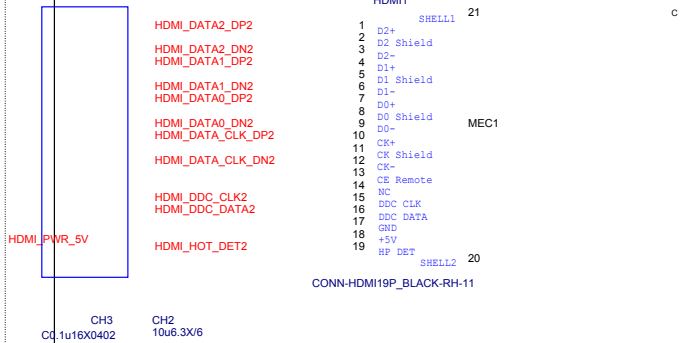


D03-606BA09-N03

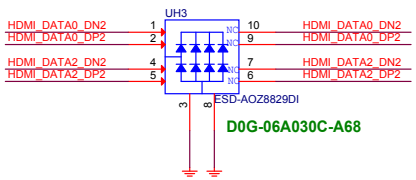
如果用DIODE SA測試電壓會不過

2019/5/6
FS1 is changed to D08-0101700-P16 by Ivy's comment

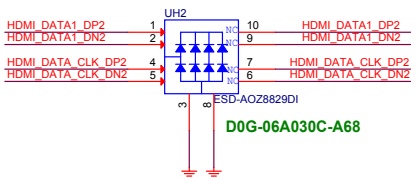
Connector



For EMI

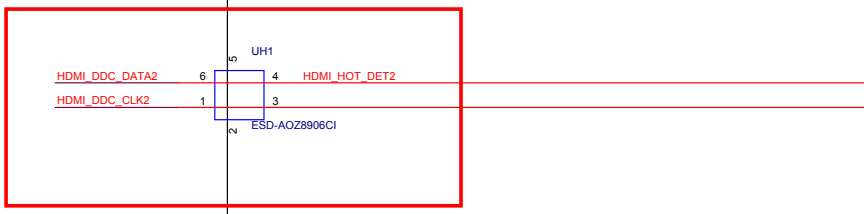


D0G-06A030C-A68



D0G-06A030C-A68

20170426



MICRO-STAR INT'L CO.,LTD.

Title: HDMI Connector

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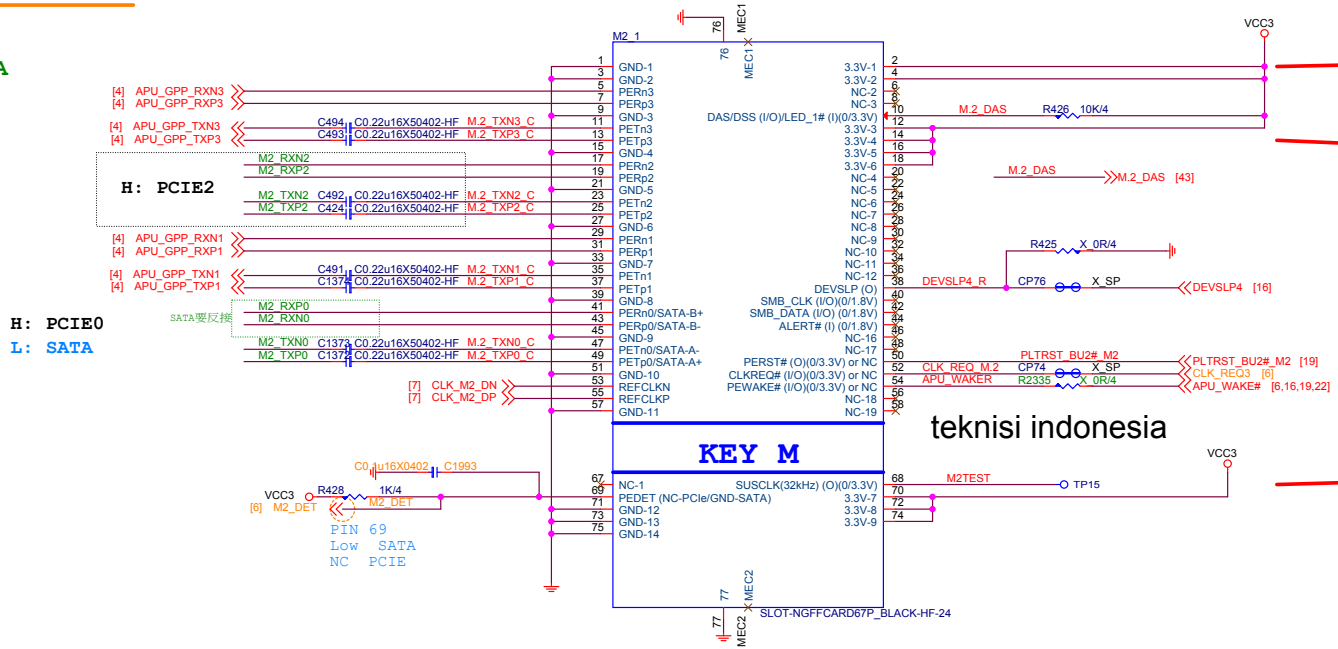
M.2 Connector

3.3V@2.5A



2019/5/21
SCREW2 is add by PM request

SCREW1 SCREW2

SCREW E2B-7984020-A89 SCREW

STANDOFF E43-1203516-A89

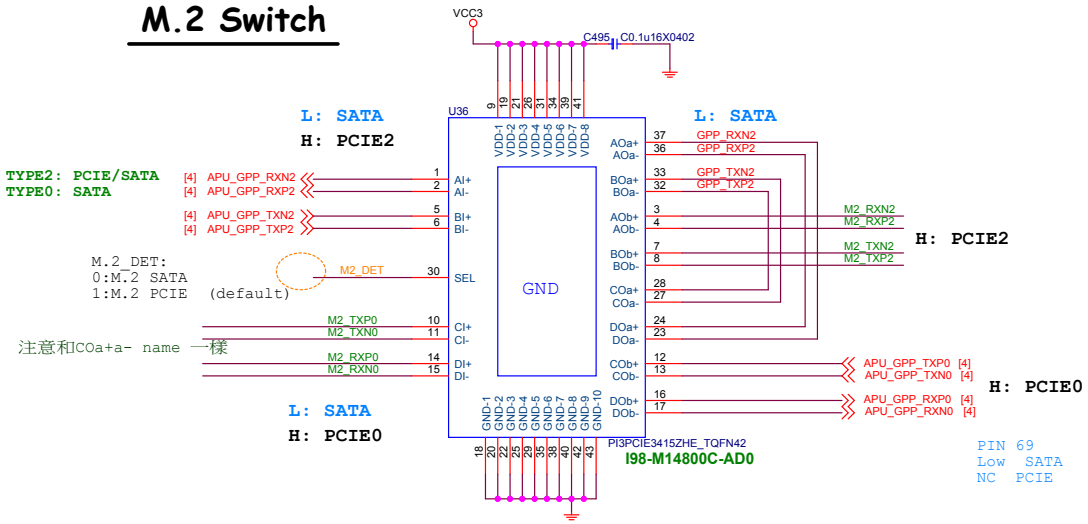
H1 <HP-BOM> H2 <HP-BOM> H3 <HP-BOM>

Screw E2B-7B05010 Screw E2B-7B05010 Screw E2B-7B05010

Footprint: H_R240D173_BR189_PT

E2B-7B05010-A89 E2B-7B05010-A89 E2B-7B05010-A89

M.2 Switch



MICRO-STAR INT'L CO.,LTD.

Title M2

Size Document Number MS-7C52.. Rev 11

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HEAT SINK

PM_HS1_Silver

X_HS-0408691-RH

2019/7/19 (1.1 MP only)
PM_HS1_Silver 導入 05/06 的 MP BOM by PM request

OK

PM_HS1

MEC1

MEC2

HS-0408690

2019/4/30
B450 SKU is added by PM spec updated

B450

X_AMD-218-0891011-RH

B450_1UF_5020

X_1u6.3X/4

CPU Socket

CPU2

E95-0000022-C22

E95-0000022-C22

2019/5/8
SPI_32 is added by PM spec updated

SPI_32

X_W25Q256JWEIQT-HF

2019/5/8
DVI1 is added by PM spec updated

DVI1

X_DVI24P_BLACK-RH-19

Simulation

X_JS3

SIM1

X_PIN1*2

X_JS4

SIM2

X_PIN1*2

MANUAL PART

2019/5/21
MKT1, MKT2, MKT3 are modified by PM updated

OK

UEFI1

G51-M1SPXXA-A09

MKT1

G51-M1SPP43-Q13

MKT2

X_G51-M1SPP42-Q13

MKT3

X_G51-M1SPP44-Q13

BAT1_X1

BAT-BCR2032P

PCB1

PK0-07C5211-G37

PK0-07C5211-G37, 精成
AVL PK0-07C5211-E48, 競華

2019/4/26
The pin1 of MH4, MH6, MH1, MH2 are changed to GND by CND rule

2019/7/19 (1.1 only)
The pootprint of MH4, MH6, MH1, MH2 are changed from HOLES_4S to Holes_4s_CND by Eric' s comment(2019/7/17)

Optics Orientation Holes

MH4

MH6

X_MH001

5010

FM3 FM2 FM8 FM6

X_FM120 X_FM120 X_FM120 X_FM120

MH1

5020

MH2

FM1 FM4 FM7 FM5

X_FM120 X_FM120 X_FM120 X_FM120

OPT	Configure	BOM	Function

MICRO-STAR INT'L CO.,LTD.

Title: BOM OPTION

Size: Document Number: MS-7C52..

Rev: 11

Date: Thursday, July 25, 2019

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