MODEL NAME : Maple
PCB NO : DA8000WL000 LA-B012PR01

Dell / Compal Confidential

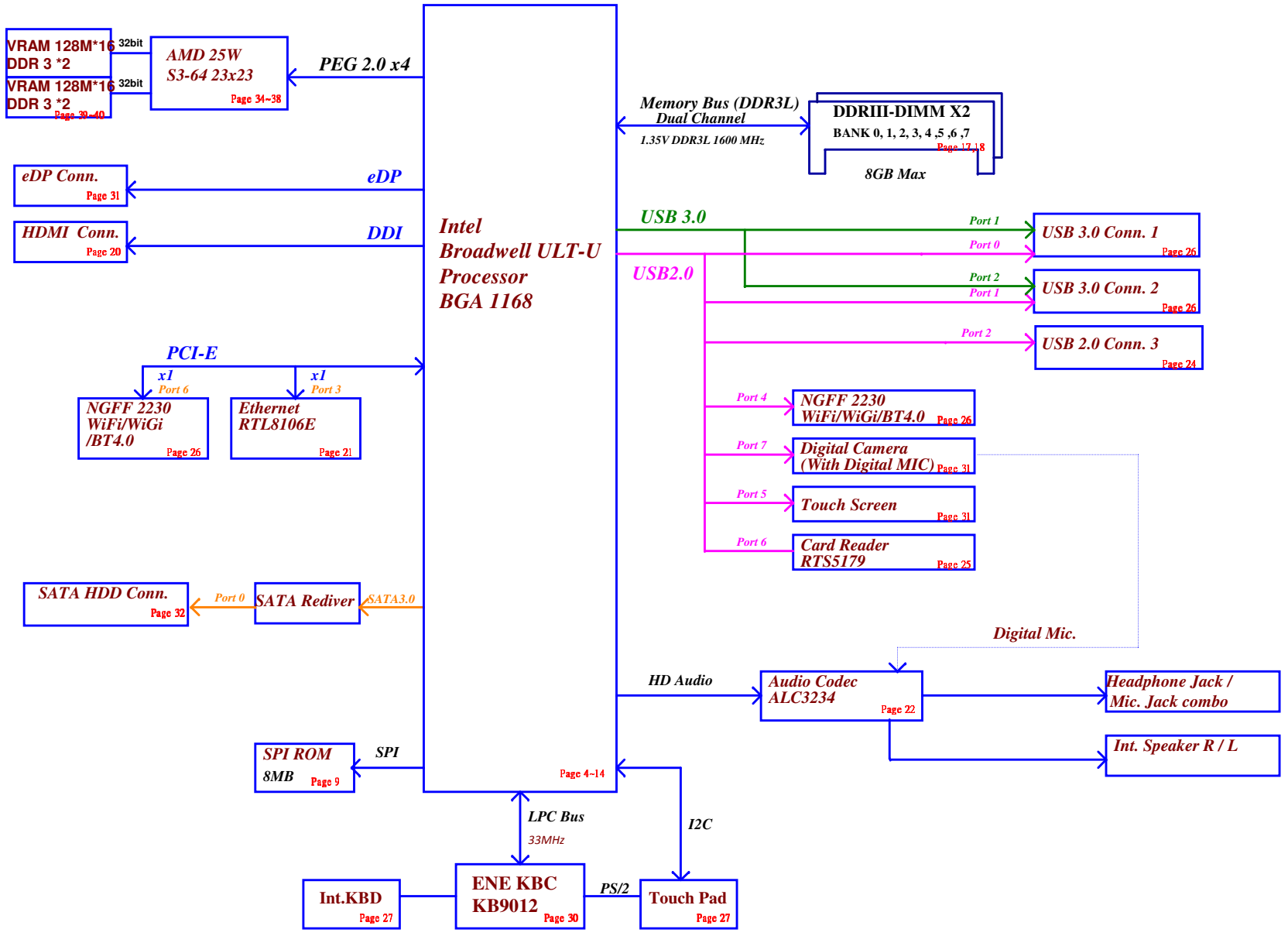
Schematic Document

Intel Shark Bay ULT
Maple 14"/15" Value
UMA / DIS AMD 25W/S3+DDR3x4

2014-01-21 Rev: 1.0

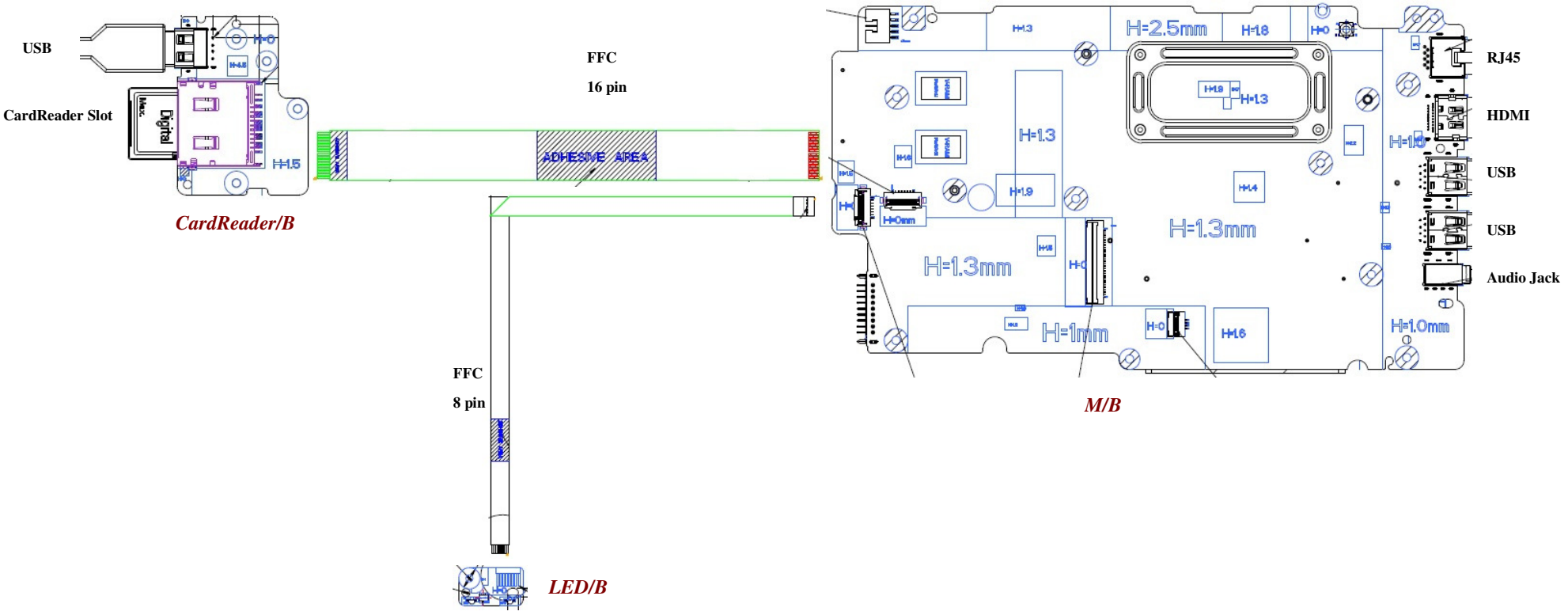
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.		
Title: MCP(1,2/19) eDP,XDP,MISC		
Size	Document Number: LA-B012P	Rev: 1.0
Date: Tuesday, August 05, 2014	Sheet 1 of 55	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/01/20	Deciphered Date	2015/01/19
Title	MCP(1,2/19) eDP,XDP,MISC		
Size	Document Number		Rev
	LA-B012P		1.0
Date:	Tuesday, August 05, 2014	Sheet	2 of 55

Compal Confidential
File Name : LA-B012P



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Issued Date	2014/01/20	Deciphered Date 2015/01/19	Title: MCP(1,2/19) eDP,XDP,MISC
			Size / Document Number: LA-B012P / Rev: 1.0
			Date: Tuesday, August 05, 2014 / Sheet 3 of 55

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)
0	SSI		
1		SSI	
2			SSI
3	PT		
4		PT	
5			PT
6	ST		
7		ST	
8			ST
9	1.0		
10		1.0	
11			1.0

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)
0	Pre-SSI		
1		Pre-SSI	
2			Pre-SSI
3	SSI		
4		SSI	
5			SSI
6	PT		
7		PT	
8			PT
9	ST		
10		ST	
11			ST
12	1.0		
13		1.0	
14			1.0

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XDP	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V	V		V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Link

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT	USB3.0	
	Port1	USB connector 1
	Port2	USB connector 2
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 1
	Port1	USB connector 2
	Port2	USB connector 3 (D/B)
	Port3	
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (AMD JET/TOBAZ)
	Lane 6	
	SATA	
	SATA0	HDD
	SATA1	
	SATA2	
	SATA3	

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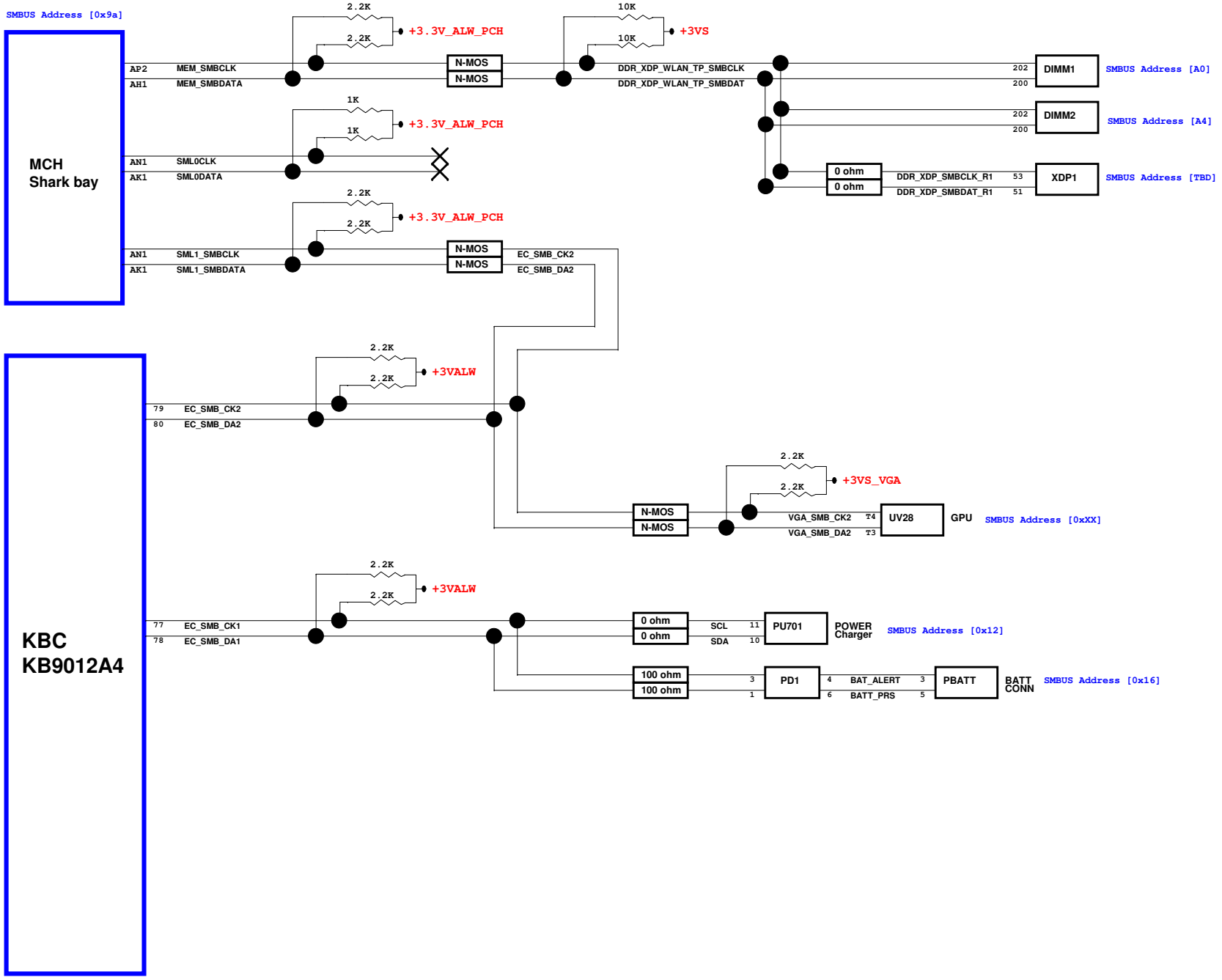
Title: MCP(1,2/19) eDP,XDP,MISC

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 4 of 55



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Compal Electronics, Inc.			
Title: MCP(1,2/19) eDP,XDP,MISC			
Size	Document Number: LA-B012P		Rev: 1.0
Date: Tuesday, August 05, 2014	Sheet 5 of 55		

i3-4020U-15W-GT2-MP

UC1 I3R1@ — CL8064701552800 QEZ5 D0 1.8G — SA00007MG0L

UC2 I3R3@ — CL8064701478202 SR16Q C1 1.7G A31! — SA00006SX2L TBD

i5-4210U-15W-GT2-MP

UC4 I5R1@ — CL8064701477802 QEAK D0 1.7G — SA00007LO0L

UC5 I5R3@ — CL8064701477702 SR170 C1 1.6G A31! — SA00006SM3L TBD

i7-4510U-15W-GT2-MP

UC7 I7R1@ — CL8064701477301 QEAF D0 2G BGA — SA00007M70L

UC8 I7R3@ — CL8064701477202 SR16Z C1 1.8G A31! — SA00006SL2L TBD

Broadwell

UC6 QG21@ — CL8065801674128 QG21 C0 1.2G — SA00007OS0L

UC9 QFSY@ — CL8064701614813 QFSY C0 1.6G — SA00007AM0L

UC10 QG22@ — CL8065801675027 QG22 C0 1.2G — SA00007OT0L

UC3A HASWELL_MCP_E — DDI — EDP — 1 OF 19 — Rev1p2

DDI1_LANE_N0 C54 DDI1_TXN0
DDI1_LANE_P0 C55 DDI1_TXP0
DDI1_LANE_N1 B58 DDI1_TXN1
DDI1_LANE_P1 C58 DDI1_TXP1
DDI1_LANE_N2 B55 DDI1_TXN2
DDI1_LANE_P2 A55 DDI1_TXP2
DDI1_LANE_N3 A57 DDI1_TXN3
DDI1_LANE_P3 B57 DDI1_TXP3

C51 DDI2_TXN0
C52 DDI2_TXP0
C56 DDI2_TXN1
B53 DDI2_TXP1
C49 DDI2_TXN2
B51 DDI2_TXP2
A53 DDI2_TXN3
B52 DDI2_TXP3

EDP_TXN0 C45 EDP_TX0# <31>
EDP_TXP0 B46 EDP_TX0 <31>
EDP_TXN1 A47 EDP_TX1# <31>
EDP_TXP1 B47 EDP_TX1 <31>
EDP_TXN2 C47
EDP_TXP2 C46
EDP_TXN3 C49
EDP_TXP3 B49
EDP_AUXN A45 EDP_AUX# <31>
EDP_AUXP B45 EDP_AUX <31>
EDP_RCOMP D20 EDP_COMP
EDP_DISP_UTIL A43 EDP_DISP_UTIL — RC1 0_0402_5% — EDP_BIA_PWM <10,31>

COMPENSATION PU FOR eDP

+VCCIOA_OUT — RC2 24.9_0402_1%~D

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

+3VS — CC1 0.1U_0402_10V7K

UC11 @ — 74CBTLV3126BQ_DHVQFN14_2P5X3

PCH_JTAG_TDO	RC3 0_0402_1%	TDO_XDP	XDP_TDO
PCH_JTAG_TDI	RC4 0_0402_1%	TDI_XDP	XDP_TDI
	RC5 0_0402_1%	TDI_XDP_R	
PCH_JTAG_TMS	RC6 0_0402_1%	TMS_XDP	XDP_TMS
		TRST#_XDP	XDP_TRST#
RUNPWROK		RUNPWROK	

1OE 2OE 3OE 2A 3A 4A 4OE 1A VCC GND GND PAD

RUNPWROK — CC5 ESD@ 0.1U_0402_10V7K — Place CC29 close to UC4

+1.05VS_PCH — CC2 0.1U_0402_10V7K — Place near JXDP1

JXDP1 — SAMTE_BSH-030-01-L-D-A — CONN@

XDP_PREQ#		CFG17	CFG17 <16>
XDP_PRDY#		CFG16	CFG16 <16>
CFG0		CFG8	CFG8 <16>
CFG1		CFG9	CFG9 <16>
CFG2		CFG10	CFG10 <16>
CFG3		CFG11	CFG11 <16>
XDP_OBS0_R		CFG19	CFG19 <16>
XDP_OBS1_R		CFG18	CFG18 <16>
CFG4		CFG12	CFG12 <16>
CFG5		CFG13	CFG13 <16>
CFG6		CFG14	CFG14 <16>
CFG7		CFG15	CFG15 <16>
H_CPUPWRGD	RC7 1K_0402_5%	H_VCCST_PWRGD_XDP	
PBTN_OUT#	RC9 0_0402_5%	CFD_PWRBTN#_XDP	
CPU_PWR_DEBUG#	RC11 0_0402_5%	CPU_PWR_DEBUG#_R	
SYS_PWROK	RC12 0_0402_5%	SYS_PWROK_XDP	
DDR_XDP_WLAN_TP_SMBDAT	RP1 0_8P4R_5%	DDR_XDP_SMBDAT_R1	
DDR_XDP_WLAN_TP_SMBCLK		DDR_XDP_SMBCLK_R1	
PCH_JTAG_TCK		XDP_TCLK	

CLK_XDP RC8 0_0402_5% — CLK_CPU_ITP <9>
CLK_XDP# RC10 0_0402_5% — CLK_CPU_ITP# <9>
XDP_RST#_R — PLT_RST# <10,21,26,30,34>
XDP_DBRESET# — RC13 1K_0402_5% — +3VS
TDO_XDP
TRST#_XDP
TDI_XDP
TMS_XDP
CFG3_R — RC15 1K_0402_5% — RC14 1K_0402_1% — CC6 0.1U_0402_10V7K

PLT_RST# — CC4 ESD@ 0.047U_0402_16V4Z — Place CC30 close to RC51.1

reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0

+1.05VS_PCH — RC16 49.9_0402_1% H_CATERR# — RC18 62_0402_5% H_PROCHOT#

PCH_JTAG_RST#	RC17 0_0402_1%	XDP_TRST#
PCH_JTAG_JTAGX	RC21 0_0402_1%	XDP_TCLK
	RC22 0_0402_5% XDP@	TDO_XDP
PCH_JTAG_TDO	RC23 0_0402_5% XDP@	TDI_XDP_R
PCH_JTAG_TCK	RC24 0_0402_5% XDP@	XDP_TCLK

+3VALW_PCH — RC19 1K_0402_5% — SYS_PWROK_XDP — CC7 0.1U_0402_10V7K ESD@ — Place near JXDP1.47

XDP_DBRESET# — RC20 0_0402_1% — SYS_RESET# — SYS_RESET# <10>

H_CPUPWRGD — RC25 10K_0402_5% — CC8 100P_0402_50V8J @EMI@ — ESD solution

CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115

UC3B HASWELL_MCP_E — MISC — JTAG — THERMAL — PWR — DDR3 — 2 OF 19 — Rev1p2

PECI_EC	H_CATERR#	D61	PROC_DETECT
	PECI_EC	K61	CATERR
		N62	PECI
H_PROCHOT#	RC26 56_0402_5% H_PROCHOT#_R	K63	PROCHOT
H_CPUPWRGD		C61	PROCPWRGD
SM_RCOMP0		AU60	SM_RCOMP0
SM_RCOMP1		AV60	SM_RCOMP1
SM_RCOMP2		AU61	SM_RCOMP2
DDR3_DRAMRST#_CPU		AV15	SM_DRAMRST
DDR_PG_CTRL		AV61	SM_PG_CNTL1

PRDY J62 XDP_PRDY#
PREQ K62 XDP_PREQ#
PROC_TCK E60 XDP_TCK
PROC_TMS E61 XDP_TMS
PROC_TRST# E59 XDP_TRST#
PROC_TDI F63 XDP_TDI
PROC_TDO F62 XDP_TDO

PCH_JTAG_RST# — R1 0_0402_5% — PCH_JTAG_RST# <8>

XDP_OBS0_R J60 — RC27 0_0402_1% — XDP_OBS1_R H60

BPM#0 H61 T1
BPM#1 H62 T2
BPM#2 K59 T3
BPM#3 H63 T4
BPM#4 K60 T5
BPM#5 J61 T6
BPM#6
BPM#7

PU/PD for JTAG signals

XDP_TMS	RP2 51_8P4R_5%	XDP_TDI
XDP_PREQ#		TDO_XDP
XDP_TDO	RP3 51_8P4R_5%	XDP_TCK
XDP_TRST#		

DDR3 COMPENSATION SIGNALS

200_0402_1%	RC28	SM_RCOMP0
120_0402_1%	RC29	SM_RCOMP1
100_0402_1%	RC30	SM_RCOMP2

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

DDR3_DRAMRST#_CPU — CC10 @ESD@ 0.047U_0402_16V4Z — Place CC35 on BOT

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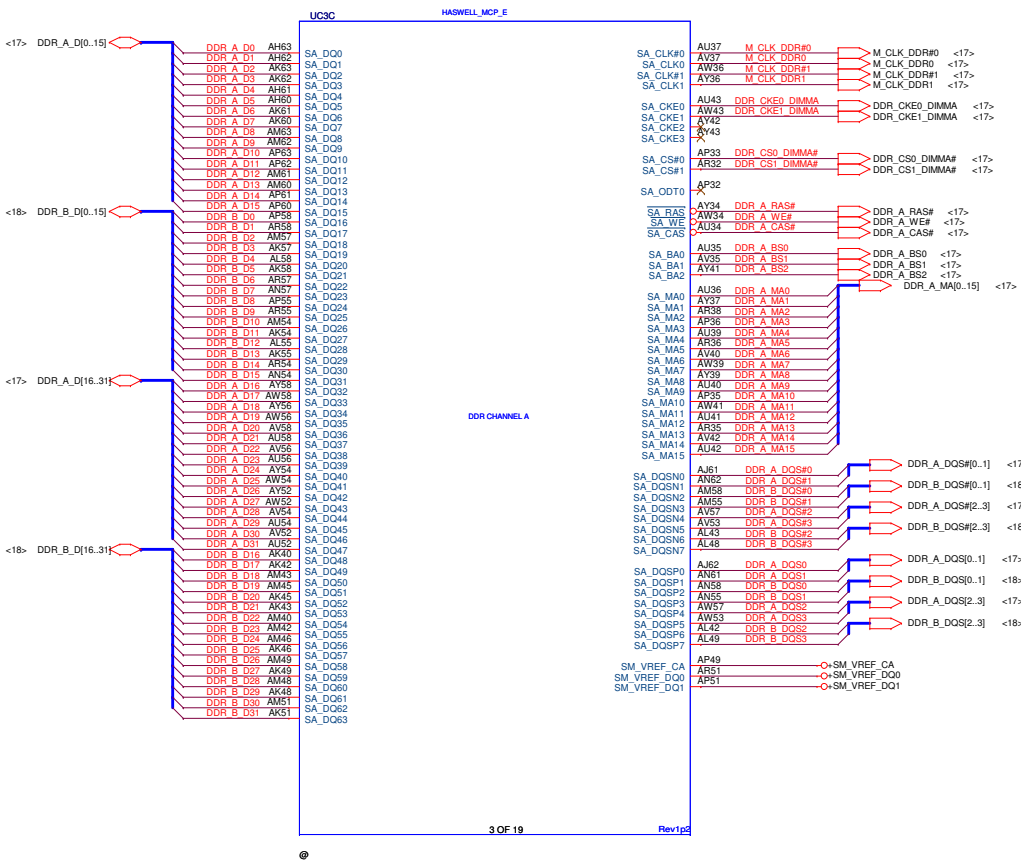
Compal Electronics, Inc.

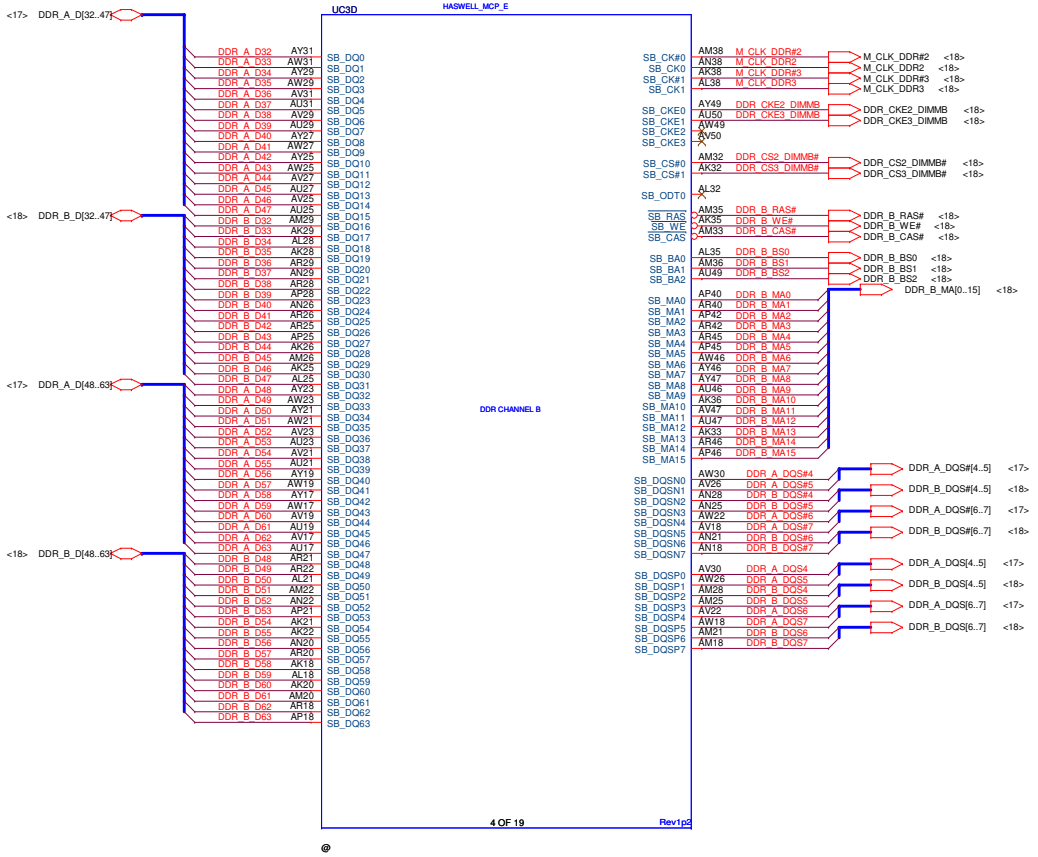
Title: MCP(1,2/19) eDP,XDP,MISC

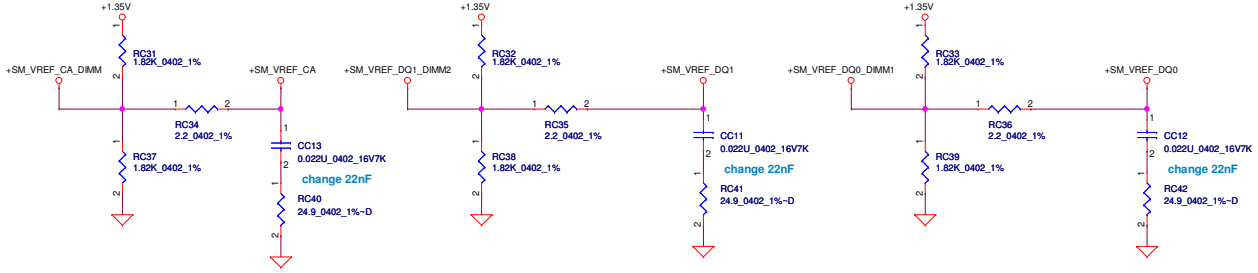
Size: — Document Number: LA-B012P — Rev: 1.0

Date: Tuesday, August 05, 2014 — Sheet 6 of 55

Interleaved Memory







confirm by intel request PDG P141

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Issued Date	2014/01/20	Deciphered Date	2015/01/19

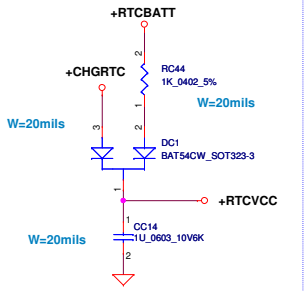
Compal Electronics, Inc.

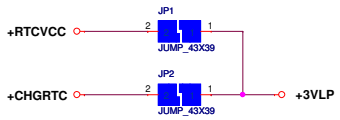
Title: MCP(3,4/19) DDR3

Size: | Document Number: LA-B012P | Rev: 1.0

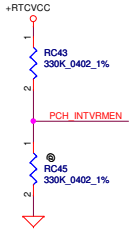
Date: Tuesday, August 05, 2014 | Sheet 7 of 55

RTC Battery



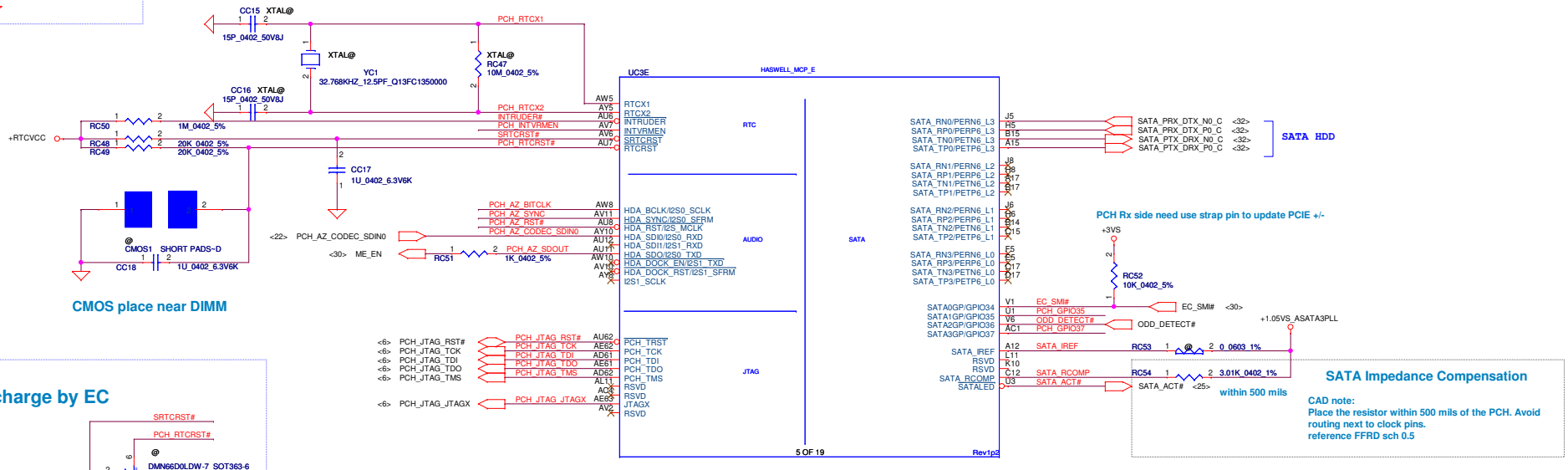


For GCLK



INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

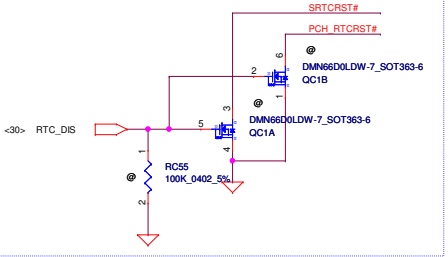
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED



SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
reference FFRD sch 0.5

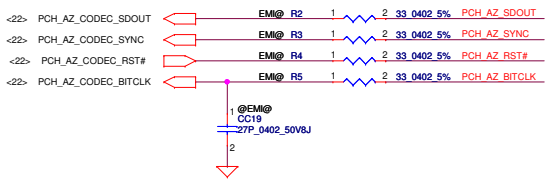
RTC discharge by EC



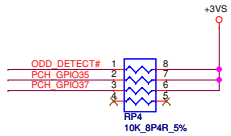
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

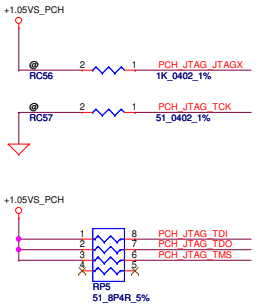
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec



EMI depop location





Security Classification	Compal Secret Data		
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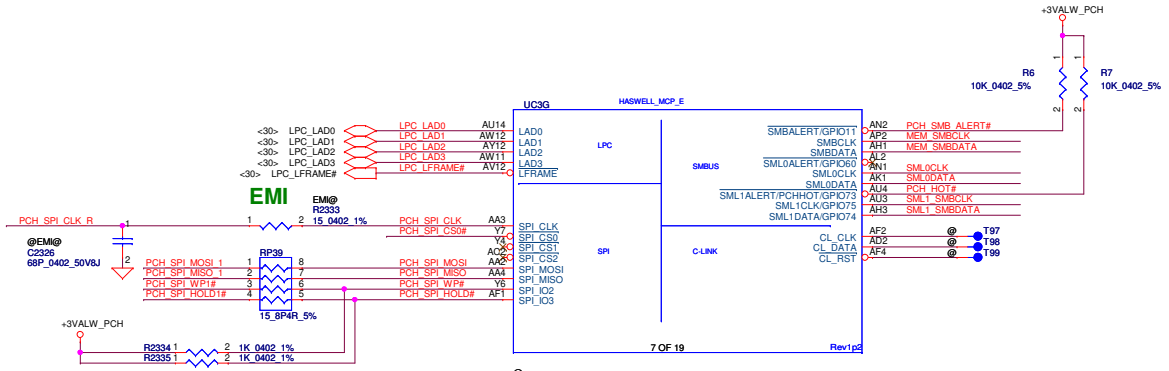
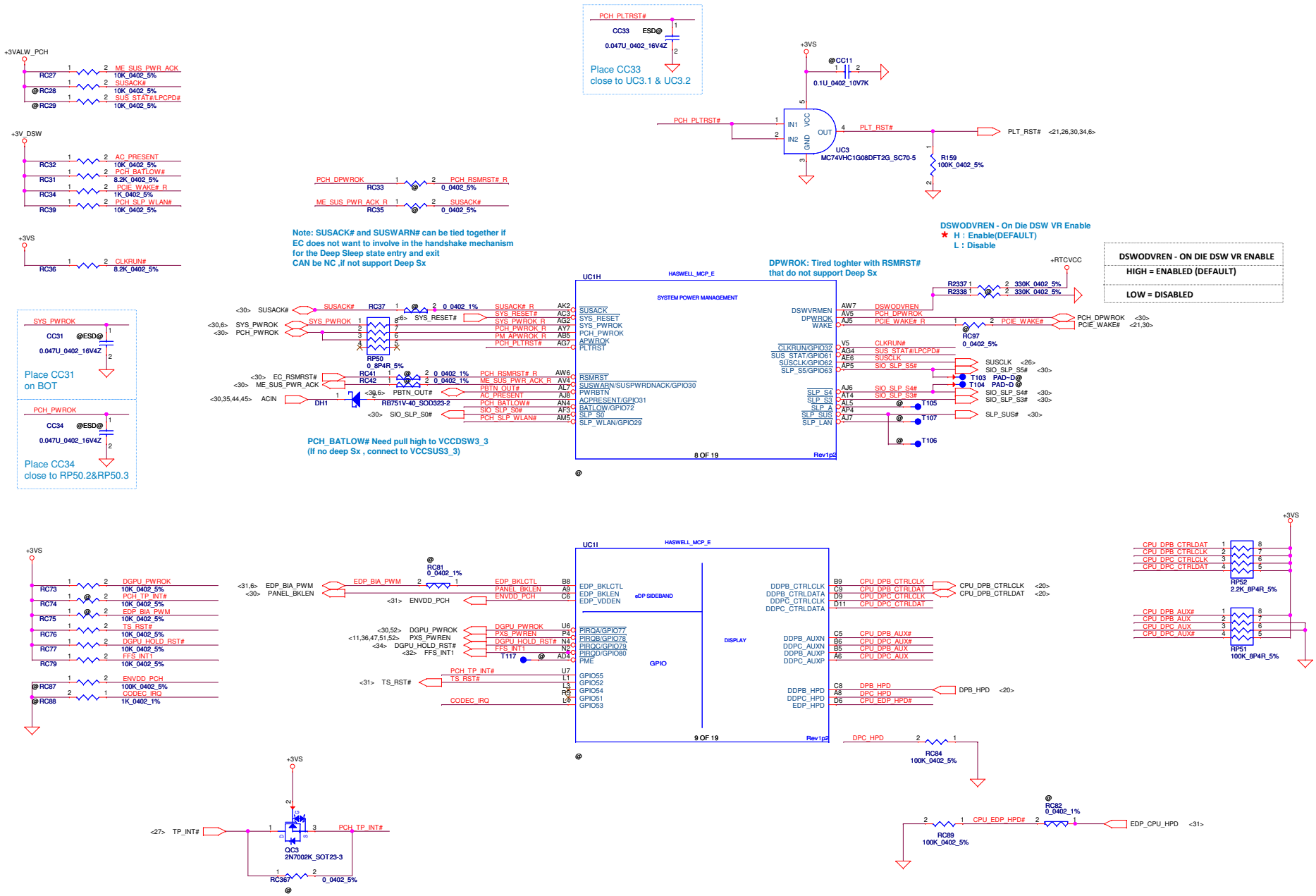
Compal Electronics, Inc.			
Title	MCP(5/19) RTC,SATA,HDA,JTAG		
Size	Document Number		Rev
	LA-B012P		1.0
Date:	Tuesday, August 05, 2014	Sheet	8 of 55



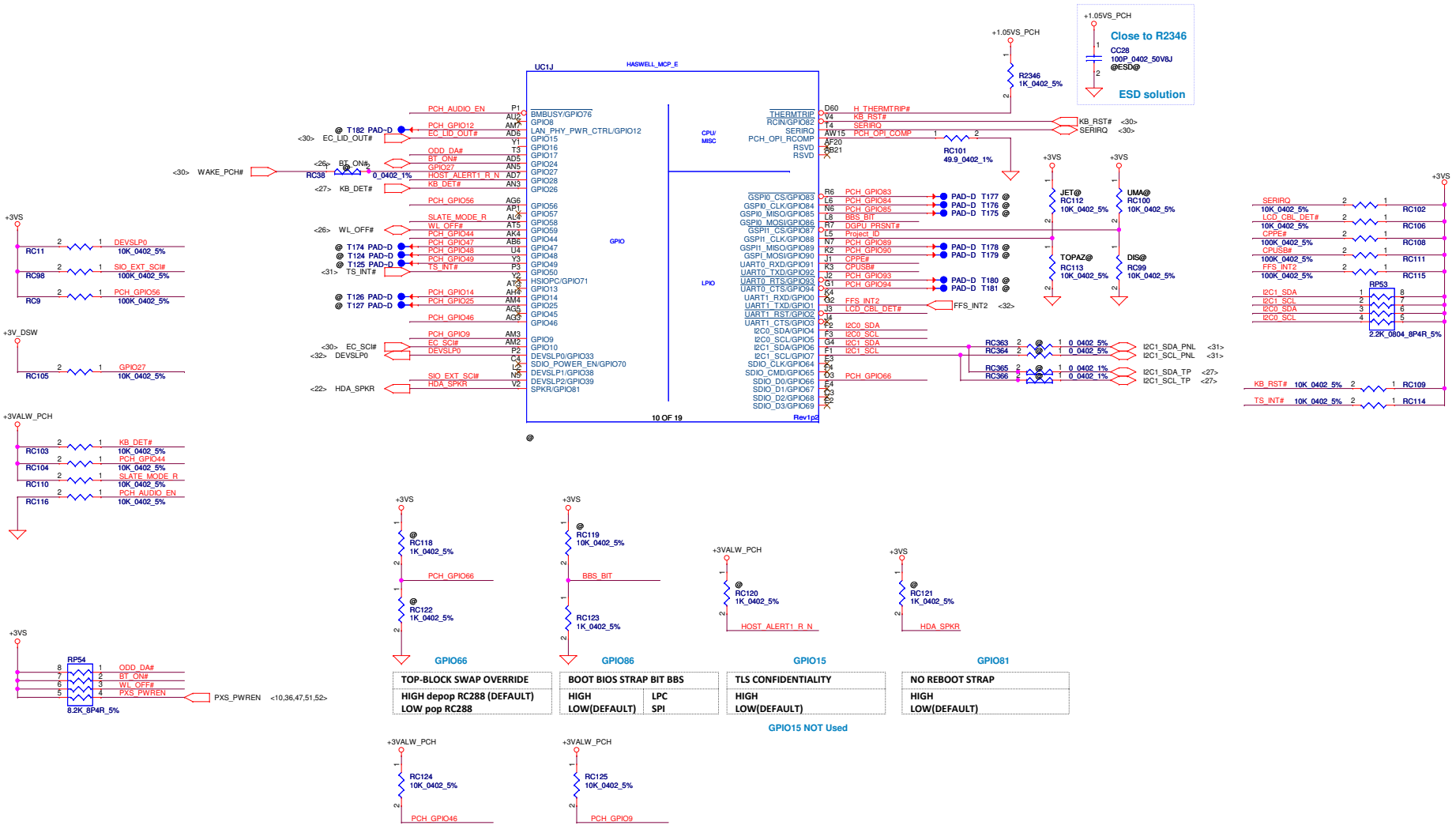
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title: MCP(6,7/19) CLK,SMB,SPI,LPC			
Size	Document Number: LA-B012P		Rev: 1.0
Date: Tuesday, August 05, 2014	Sheet 9 of 55		



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title	MCP(8,9/19) DDI,EDP,GPIO		
Size	Document Number LA-B012P		Rev 1.0
Date: Tuesday, August 05, 2014	Sheet 10 of 55		



Security Classification	Compal Secret Data		
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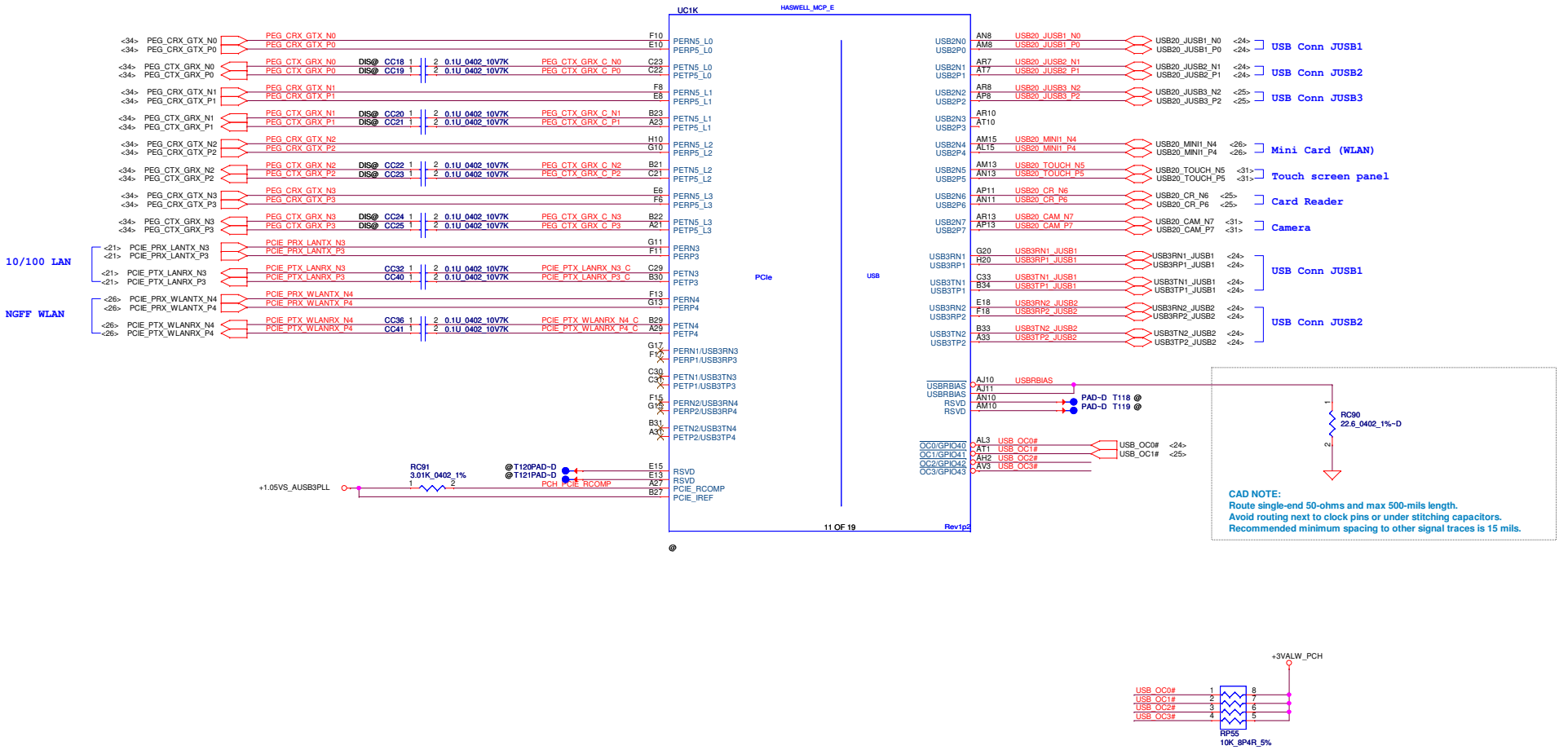
Compal Electronics, Inc.			
Title	MCP(10/19) GPIO,LPIO,MISC		
Size	Document Number LA-B012P		Rev 1.0
Date: Tuesday, August 05, 2014	Sheet 11 of 55		



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Compal Electronics, Inc.			
Title	MCP(11/19) PCIE,USB		
Size	Document Number	LA-B012P	Rev 1.0
Date:	Tuesday, August 05, 2014	Sheet 12 of 55	

VCCST_PG_EC
C79 ESD@
220P_0402_50V8J
Place C79 between R286 and UC1
+1.05VS_PCH
R286 10K_0402_5%
<30> VCCST_PG_EC
VCCST_PG_EC
Define EC OD pin, need double confirm.

+CPU_CORE
+1.35V
C40
22U_0603_6.3V6M
@ESD@
ESD solution

SVID ALERT
+1.05VS_PCH
R252 75_0402_5%
Place the PU resistors close to CPU
R254 43_0402_1%
<50> VR_SVID_ALRT#
H_CPU_SVIDALRT#

SVID DATA
SVID_DAT need to pull-up double side (PWR_VR & CPU)
+1.05VS_PCH
Place the PU resistors close to CPU
R256 130_0402_1%
@ R257 0_0402_1%
<50> VR_SVID_DAT
H_CPU_SVIDDATA

VR_ON
C80 ESD@
0.1U_0402_10V7K
Place C80 close to R250.1

UC1L HASWELL_MCP_E
12 OF 19
HSW ULT POWER
+1.35V
+VCCIO_OUT
+CPU_CORE
R245 @ 0_0603_5%
VCCSENSE
T38 @
+VCCIO_OUT_R
+VCCIOA_OUT
<50> VR_SVID_CLK
R248 0_0402_1%
H_CPU_SVIDCLK
H_CPU_SVIDDATA
<30,50> VR_ON
<50> H_VR_READY
R250 0_0402_1%
R251 0_0402_1%
VR12.5_VR_ON_R
VR_READY_R
<6> CPU_PWR_DEBUG#
CPU_PWR_DEBUG#
VCCST_PG_EC
VR_EN
VR_READY
VIDALERT
VIDSCLK
VIDSOUT
VCCST_PWRGD
RSVD_TP
VCC
VCCST
VSS
PWR_DEBUG
RSVD
Rev1p5

RF
RF@
C5212
68P_0402_50V8J
H_CPU_SVIDCLK

+1.05VS_PCH
@ R253 150_0402_1%
R253
INTEL Check list , XDP use only
CPU_PWR_DEBUG#
@ R255 10K_0402_5%

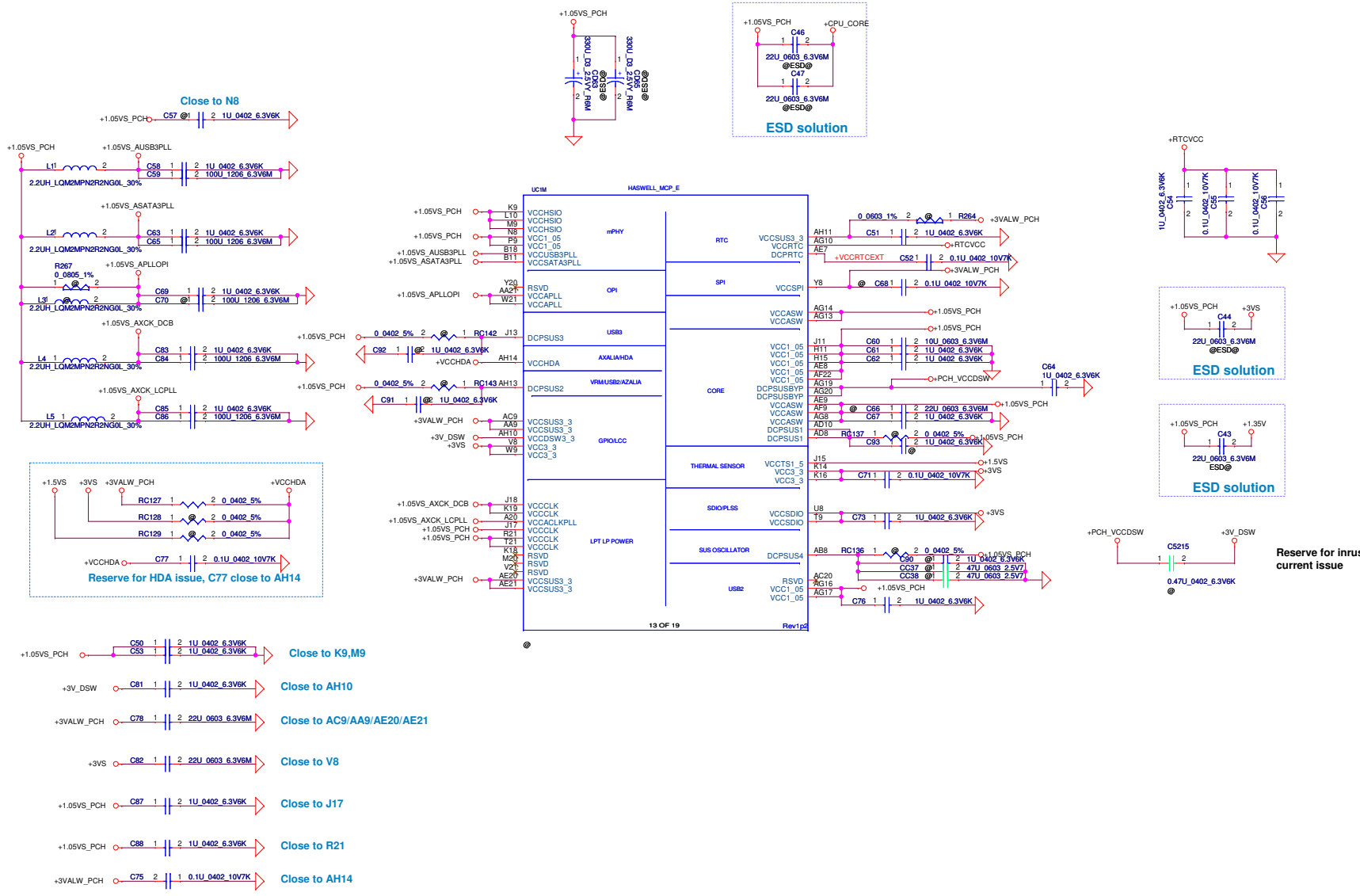
+CPU_CORE
R1 100_0402_1%
<50> VCCSENSE
VCCSENSE
CAD Note: PU resistor on HW side
<15,50> VSSSENSE
VSSSENSE
CAD Note: PD resistor on HW side
R2 100_0402_1%

+1.35V
VDDQ DECOUPLING
C35 2.2U_0402_6.3V6M
C36 2.2U_0402_6.3V6M
C37 2.2U_0402_6.3V6M
C38 2.2U_0402_6.3V6M
C39 10U_0603_6.3V6M
C41 10U_0603_6.3V6M
C72 10U_0603_6.3V6M
C42 10U_0603_6.3V6M
C45 10U_0603_6.3V6M
C74 10U_0603_6.3V6M

+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

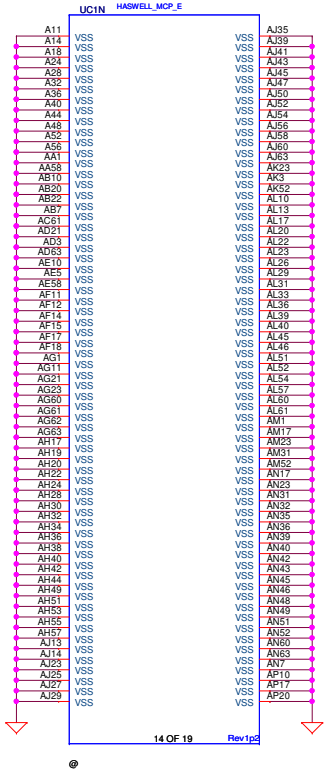
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

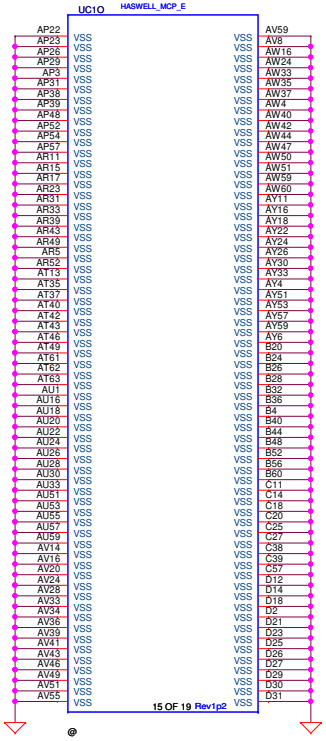
Compal Electronics, Inc.
Title: MCP(12/19) Power
Size: Document Number: LA-B012P
Rev: 1.0
Date: Tuesday, August 05, 2014
Sheet 13 of 55

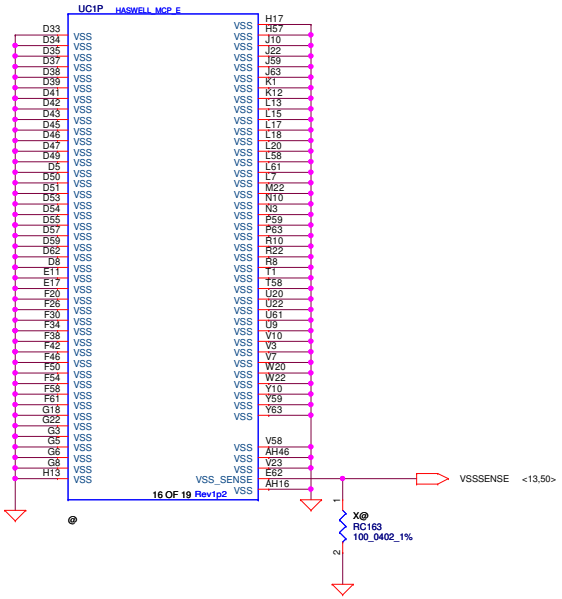


Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.	
Title	MCP(13/19) Power
Size	Document Number: LA-B012P
Rev	1.0
Date:	Tuesday, August 05, 2014
Sheet	14 of 55







CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

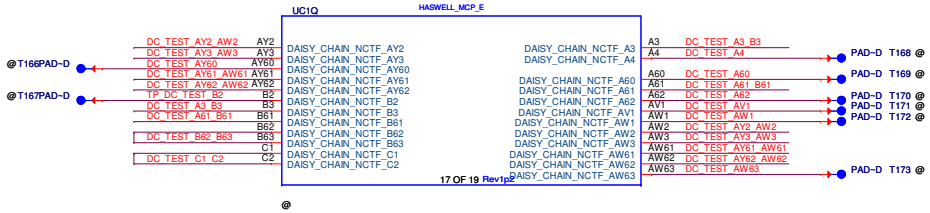
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

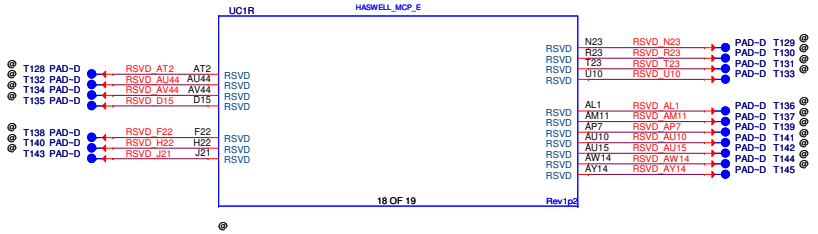
Compal Electronics, Inc.

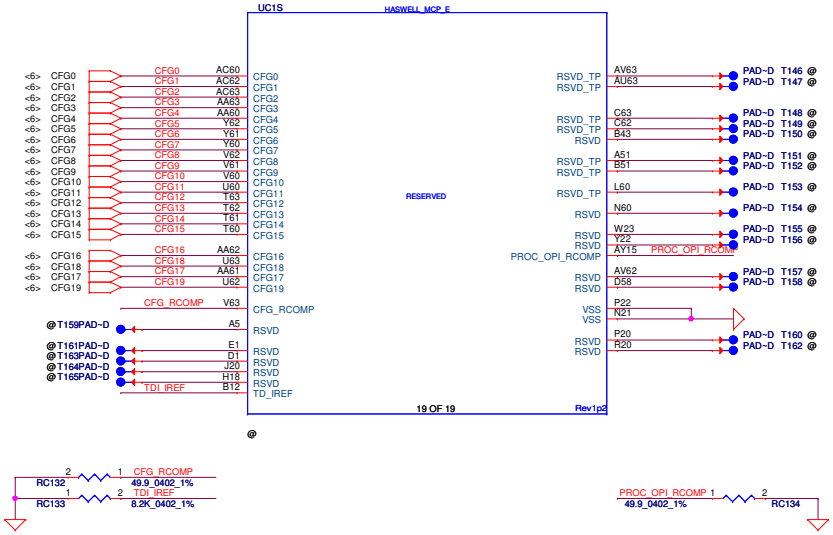
Title: MCP(14,15,16/19) VSS

Size: | Document Number: LA-B012P | Rev: 1.0

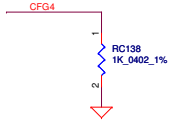
Date: Tuesday, August 05, 2014 | Sheet 15 of 55







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Size: Document Number: LA-B012P

Rev: 1.0

Date: Tuesday, August 05, 2014 Sheet 16 of 55

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

Place CC31 between QD2 and R2349

ESD solution

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 17 of 55

H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_MA[0..15]

Layout Note: Place near JDIMM2

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

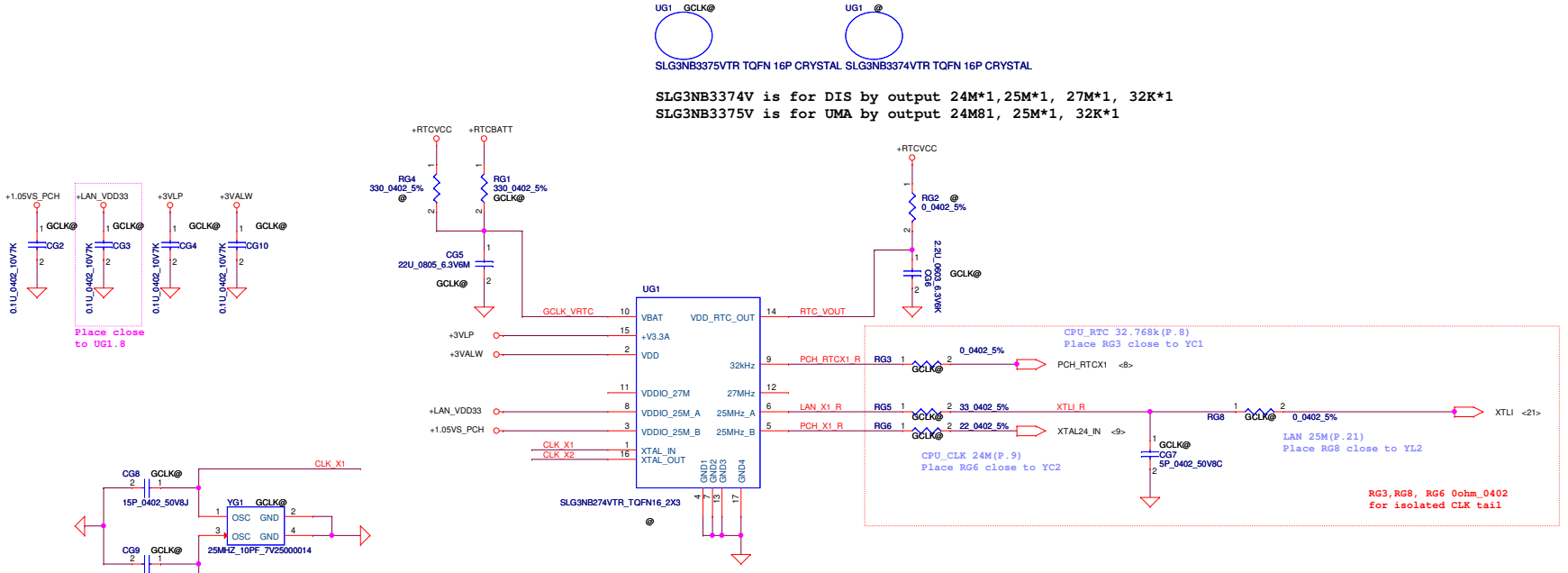
Layout Note: Place near JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

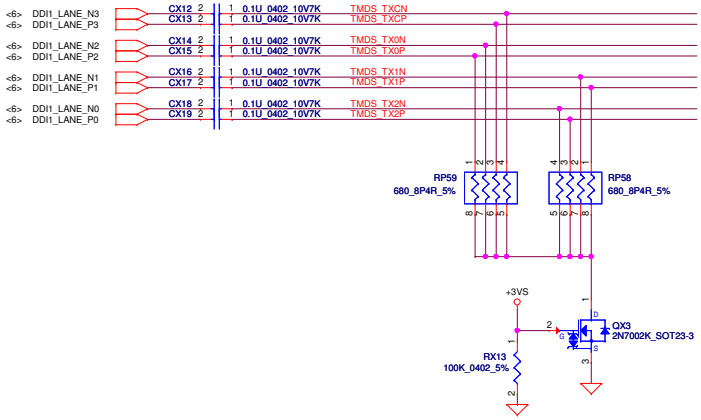
Compal Electronics, Inc.

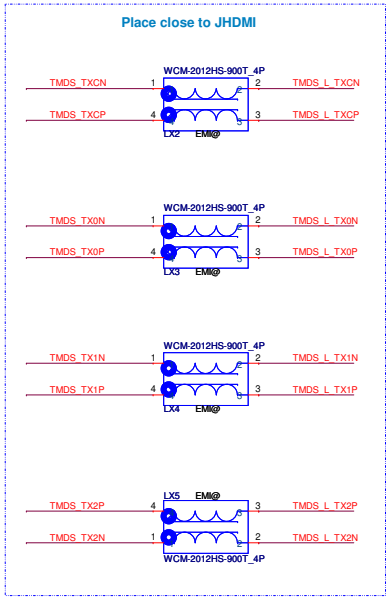
Title: DDRIII DIMMB
Size: Document Number: LA-B012P
Rev: 1.0
Date: Tuesday, August 05, 2014
Sheet 18 of 55

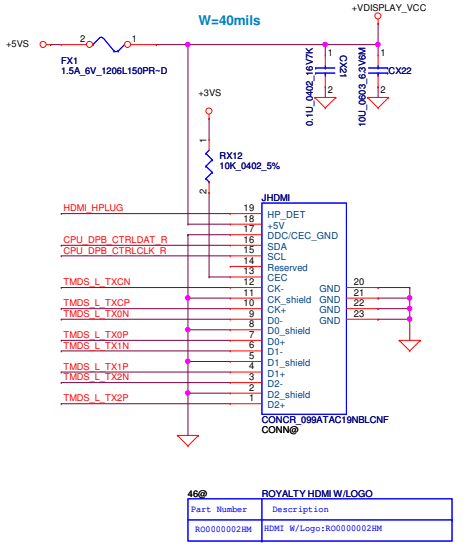


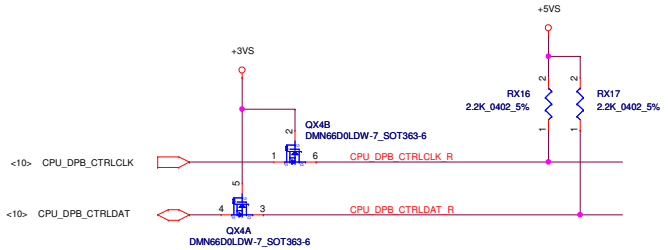
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

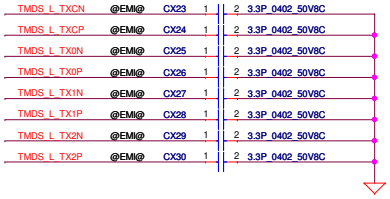
Compal Electronics, Inc.			
Title: Green CLK			
Size	Document Number: LA-B012P		Rev: 1.0
Date: Tuesday, August 05, 2014	Sheet 19 of 55		

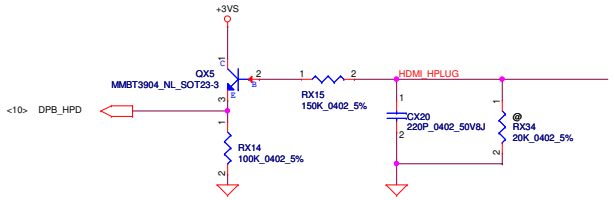












Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: HDMI

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 20 of 55

W=40mils

+LAN_IO rising time : >1ms and <100ms

W=40mils

W=40mils

1.5A

60mils_3via

40mils_2via

APL3512 PIN 4 tire to VIN

RTL8111G(LDO mode)

RTL8111GS(SWR mode)

Place close to each VDD10 pin

These caps close to UL1: Pin 11,32

+LAN_VDD33 Rising time (10%~90%) >1mS and <100mS

CL30, CL31 close to UL1 Pin 17, 18

S X'FORM_ NS14Y LF LAN

SP050007J00

Place close to TCT pin

For GCLK

XTAL

Reserve 10K pull LAN_IO

RTL8106E-CG QFN 32P E-LAN CTRL

CONN@

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: LAN RTL8106EUS

Size: Custom | Document Number: LA-B012P | Rev: 1.0

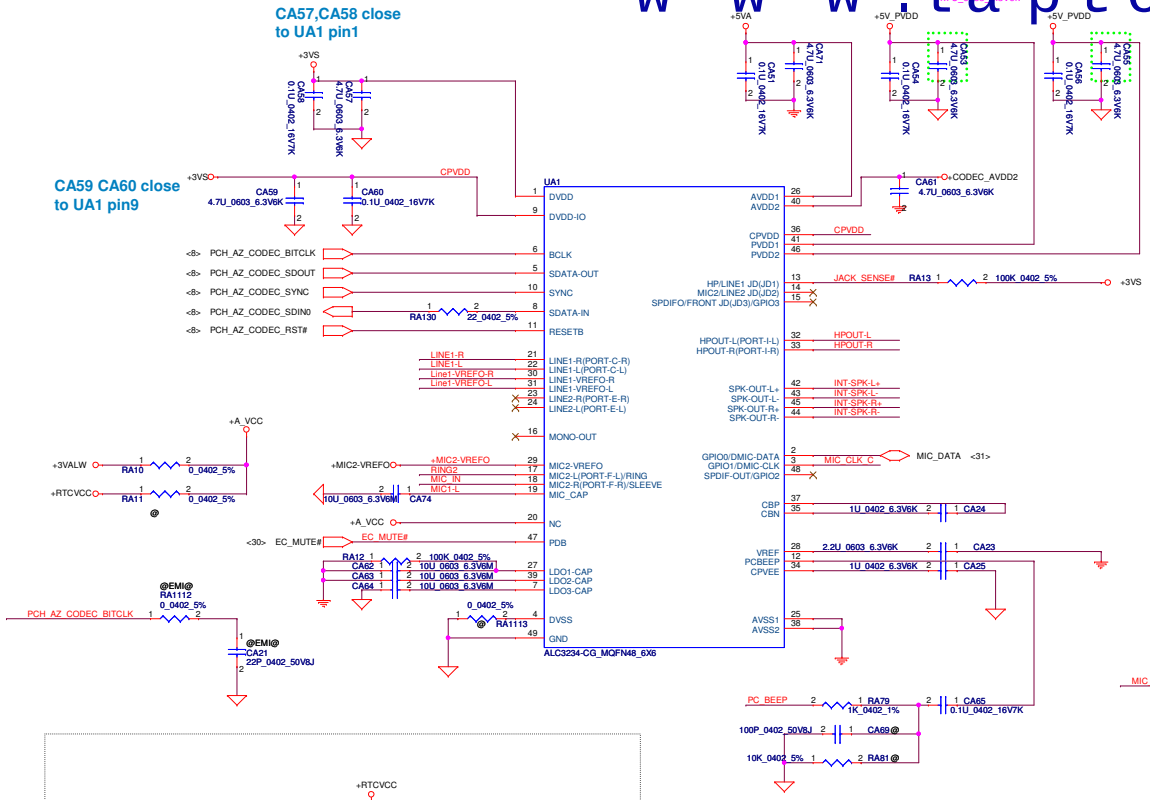
Date: Tuesday, August 05, 2014 | Sheet 21 of 55

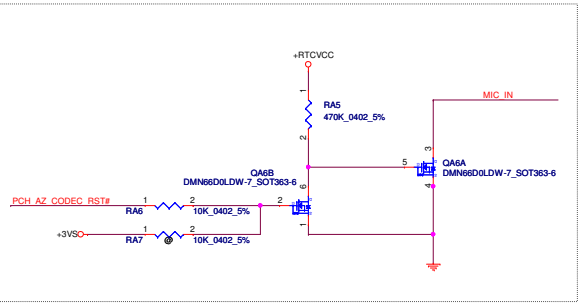
CA57,CA58 close to UA1 pin1

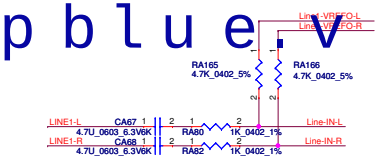
CA59 CA60 close to UA1 pin9

CA61, CA51 place close to Pin 26

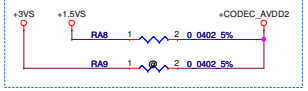
CA53, CA55 change Value from 1U_0603_6.3V6K to 4.7U_0603_6.3V6K



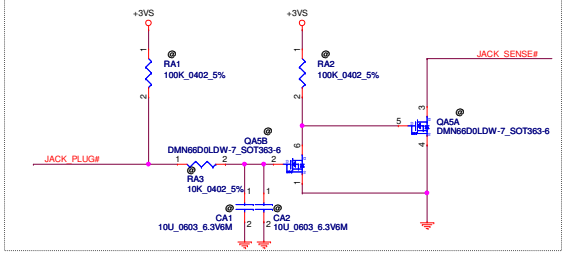


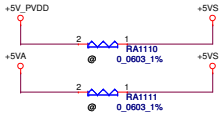


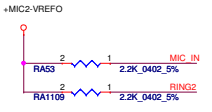
Reserve for HDA issue



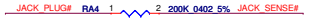
JACK_PLUG Delay circutis

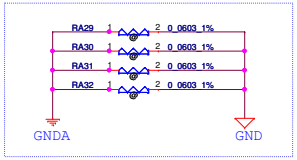




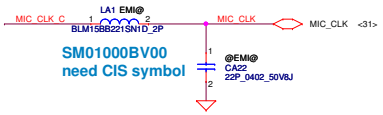


Reserve for cancel Delay circutis

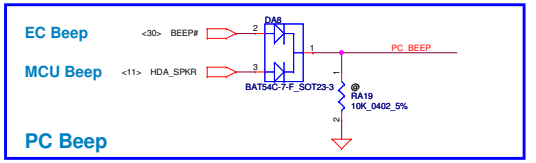




Place on the moat between GND & GNDA.

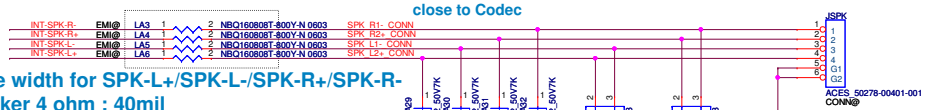


SM01000BV00 need CIS symbol



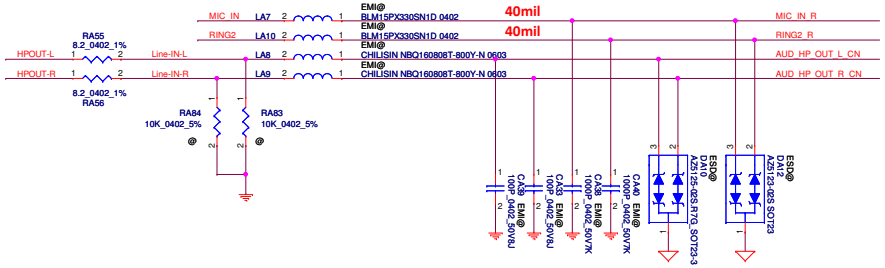
Close to UA1 Pin11,13,14,16

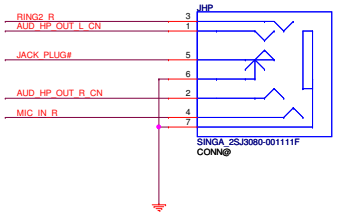
close to Codec



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack





Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: Audio Codec ALC3234

Size: B | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 22 of 55

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

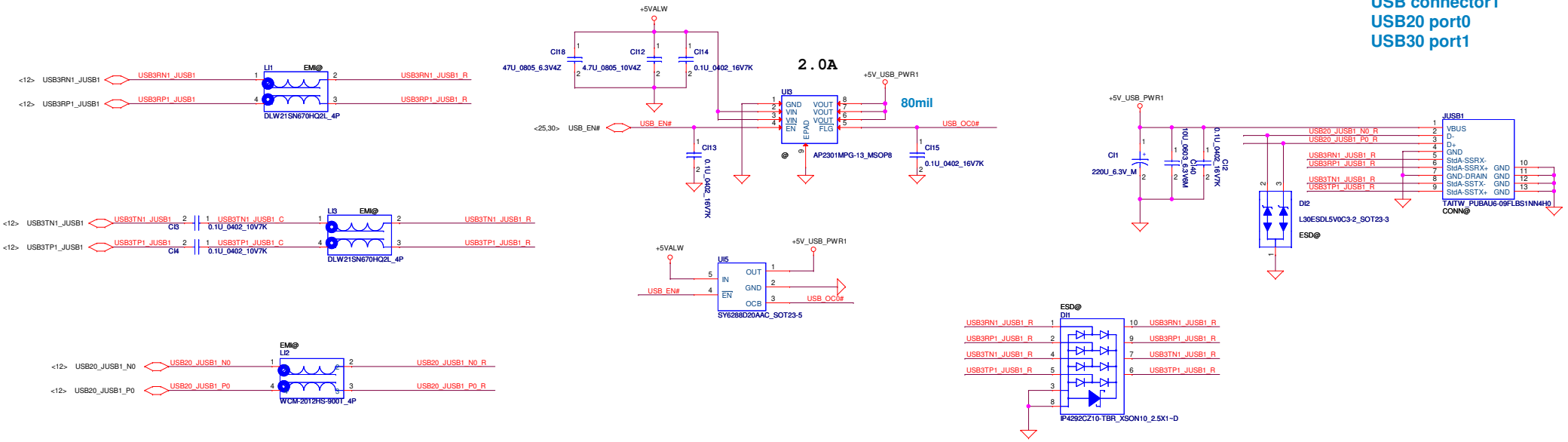
Compal Electronics, Inc.

Title: **Reserved Page**

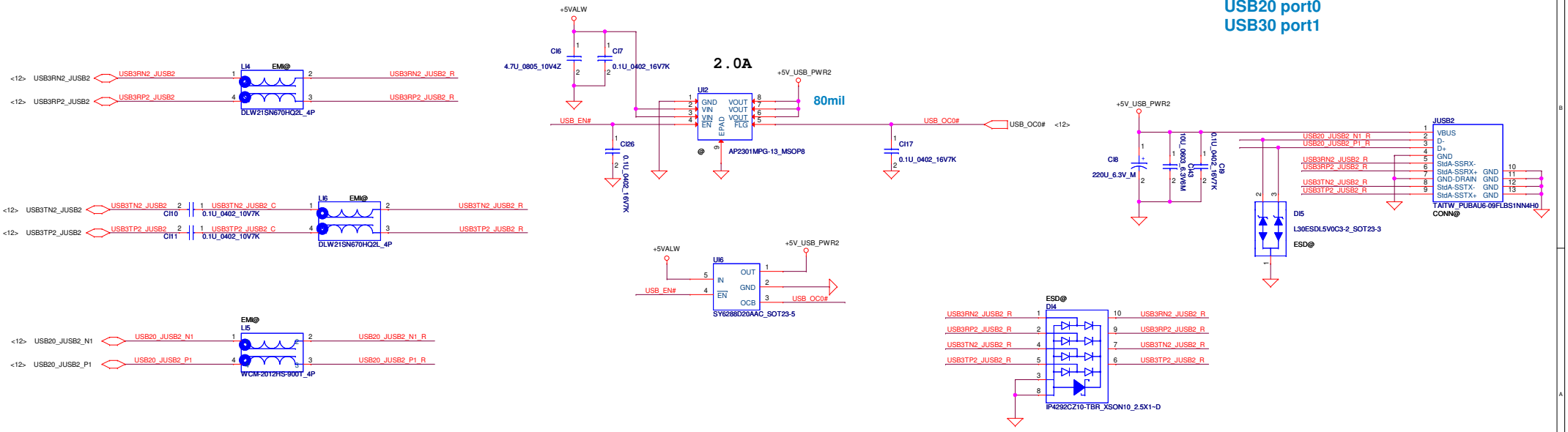
Size | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 23 of 55

USB connector1
USB20 port0
USB30 port1



USB connector2
USB20 port0
USB30 port1



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

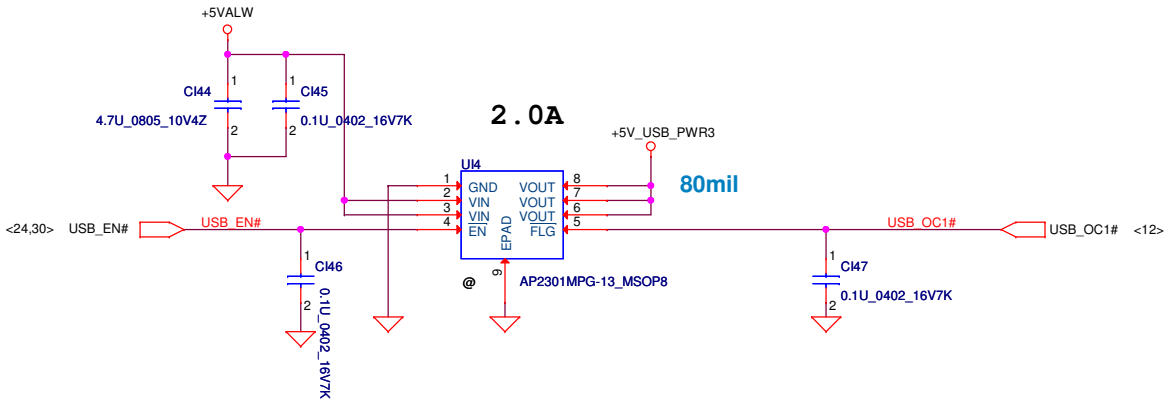
Compal Electronics, Inc.

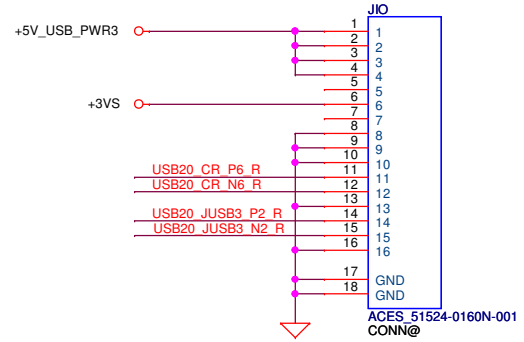
Title: USB3.0

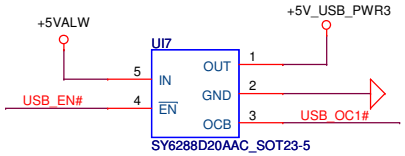
Size | Document Number: LA-B012P | Rev: 1.0

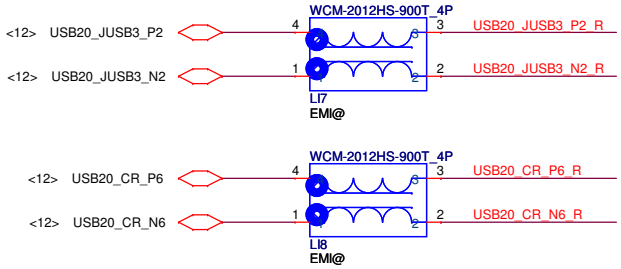
Date: Tuesday, August 05, 2014 | Sheet 24 of 55

IO to MB CONN
Substitute:SP01001FS00

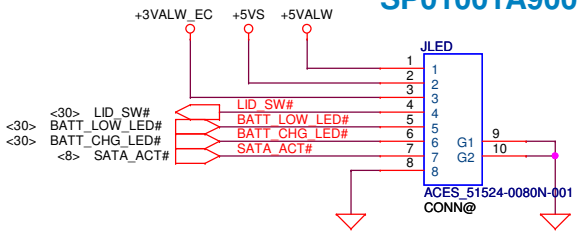








LED/B TO M/B
SP01001A900



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

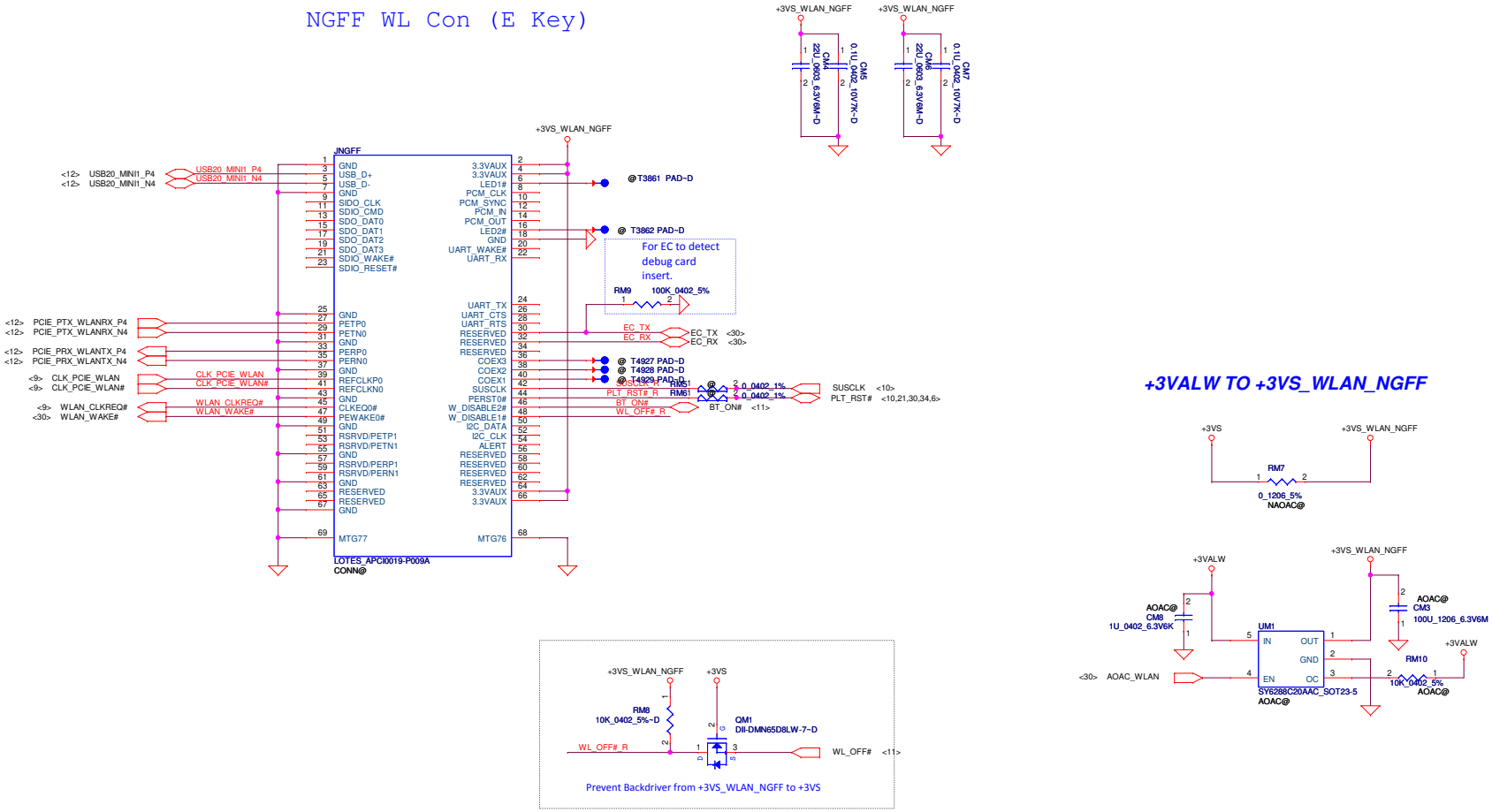
Title: *IO/B, LED/B*

Size: B | Document Number: *LA-B012P* | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 25 of 55

closed to pin 2, 4 closed to pin 64, 66

NGFF WL Con (E Key)



+3VALW TO +3VS_WLAN_NGFF

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: NGFF WLAN

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 26 of 55

Power ON Circuit

ON/OFF switch

TOP Side

SW1 SMT1-05-A 4P

+3VLP

RE49 100K_0402_5%

ON/OFFBTN# <30>

CE20 0.1U_0402_16V7K

@ESD@ L03ESDL5V0CC3-2_SOT23-3 DE2

FAN Control circuit

+FAN_POWER

40mil

CE22 2.2U_0603_6.3V6K

CE23 1000P_0402_50V7K

+5VS

CE25 2.2U_0603_6.3V6K

UE3 APE8875M SOP 8P

<30> EN_DFAN1

EN_DFAN1

RE50 10K_0402_5%

<30> FAN_SPEED1

CE24 0.01U_0402_16V7K

JFAN ACES_88231-03041 CONN@

HE1 place around FAN area.

+3VALW +3VLP

RE332 13.7K_0402_1% AOAC@

RE333 13.7K_0402_1%

<30> VCIN0_PH2

HE1 100K_0402_1%_TSM0B104F4251RZ

AOAC@

J519 short

RE330 0_0603_5%

+3VALW +V_TP

RE331 0_0603_5%

+3VS

J519 JUMP_43X39

UE4 TPS22967DSGR_SON8_2X2

<30> TP_EN

CE60 2200P_0402_25V7K

CE59 0.1U_0402_10V6K

CE61 1U_0402_6.3V6K

For Test,
APE8937(SA000070L00)
AOZ1336(SA00006U600)
TPS22967(SA000070S00)

INT_KBD Connector

JKB HB_A823020-SBHR21 CONN@

KSI[0..7]

KSO[0..16]

RE60 240_0402_1%

<30> CAPS_LED

KB_CAPS_PWR

* Key Board Back Light

+5VS FE1 KBBL@ +5VS_KBL

0.75A_24V_1812L075-24DR-OK

20mil

RE59 0_0805_5%

CE56 1U_0603_10V6K

CE57 10U_0603_6.3V6M

KBBL@

<11> KB_DET#

RE68 10K_0402_5%

QE4 2N7002KW 1N SOT323-3 KBBL@

KB_BL_PWM

RE58 100K_0402_5% KBBL@

JKBBL ACES_50524-00401-P01 CONN@

QE5 AP2606AGY-HF 1N SOT26-6 KBBL@

<30> KB_LED_PWM

Touch pad

+3VS_TOUCH

RE340 10K_0402_5%

RC78 10K_0402_5%

RE329 100K_0402_5%

<11> I2C1_SDA_TP

<11> I2C1_SCL_TP

<30> EC_TP_INT#

RE336 2.0_0402_1%

RE337 2.0_0402_1%

RE338 0_0402_5%

PTP@

<10> TP_INT#

<30> PTP_DIS#

<30> TP_DATA

<30> TP_CLK

I2C1_SDA_TP_R

I2C1_SCL_TP_R

TP_INT#

PTP_DIS#

JTP ACES_51524-0080N-001 CONN@

CE58 1U_0402_6.3V6K-D

PTP

JTP1 ACES_51524-0100N-001 CONN@

<30> PTP_KBBL#

RE339 10K_0402_5%

QE6 Circuit

+3VS +3VS_TOUCH

RE334 10K_0402_5%

RE335 10K_0402_5%

I2C1_SDA_TP I2C1_SDA_TP_R

I2C1_SCL_TP I2C1_SCL_TP_R

QE6B DMN66D0LDW-7_SOT363-6

QE6A DMN66D0LDW-7_SOT363-6

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

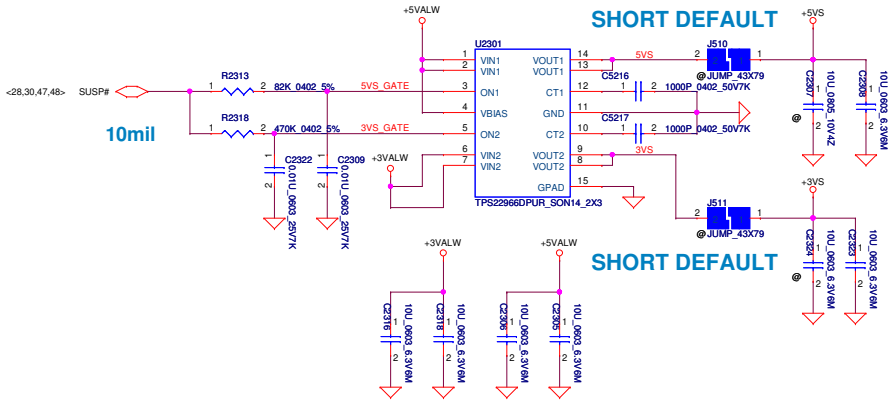
Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

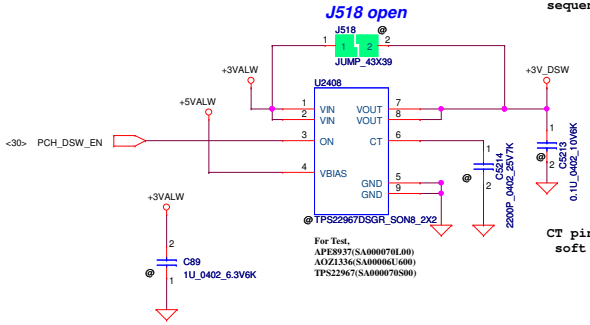
Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 27 of 55

+5VS and +3VS switch



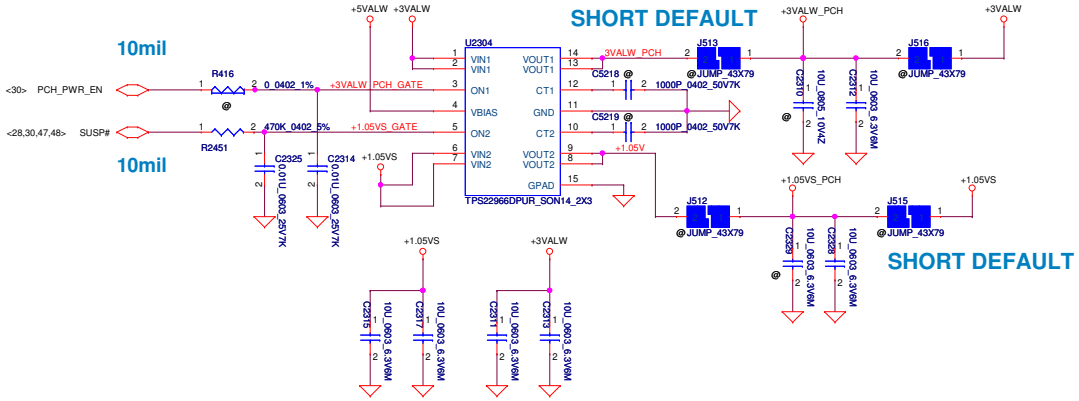
+3VALW TO +3V_DSW

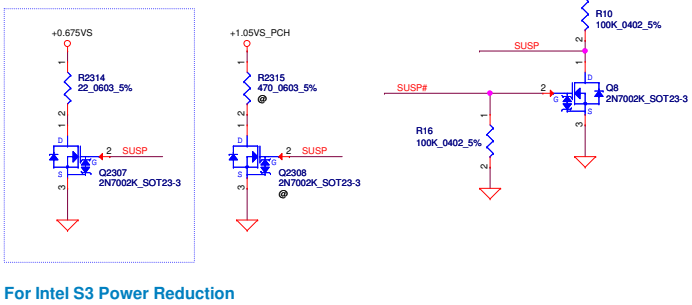


+3V_DSW have soft start sequence: +3V_DSW stable > +3VALW_PCH > 0ms

CT pin use 2200pf for soft start tuning

+3VALW_PCH switch





For Intel S3 Power Reduction

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: DC/DC Interface

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 28 of 55

Screw Hole

ZZZ

PCB 13P LA-B011P REV0 M/B

DA60013U000

H1 H_2P8N @
H20 H_2P8N @
H21 H_2P8N @
H22 H_2P8X3P3N @
H23 H_2P8X4P8N @

H2 H_2P8 @
H3 H_2P8 @
H4 H_2P8 @
H5 H_2P8 @
H6 H_2P8 @
H7 H_2P8 @
H8 H_2P8 @
H9 H_2P8 @

H10 H_3P0 @

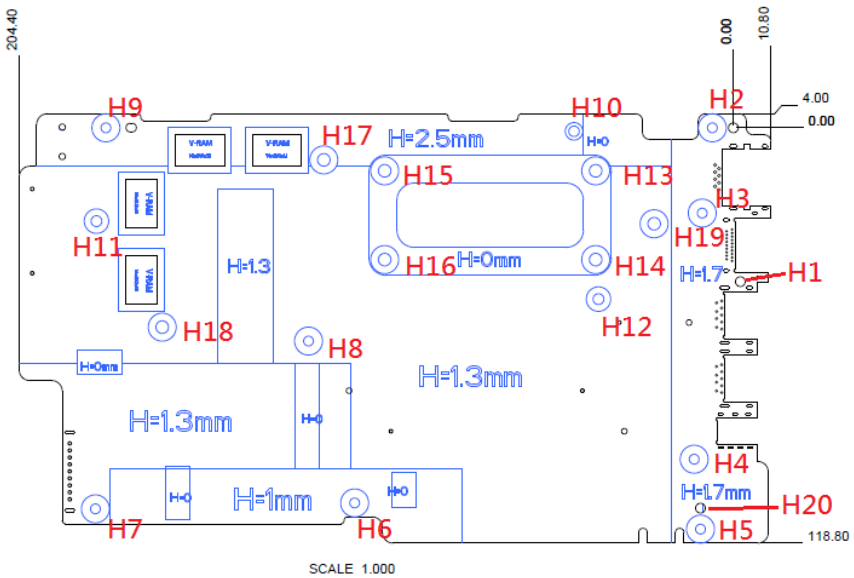
H11 H_2P8 @
H12 H_2P8 @

H13 H_3P6 @
H14 H_3P6 @
H15 H_3P6 @
H16 H_3P6 @
CPU bracket

H17 H_3P3 @
H18 H_3P3 @
VGA stand-off

H19 H_3P3 @
NGFF stand-off

FD1 @FIDUCAL
FD2 @FIDUCIAL
FD3 @FIDUCAL
FD4 @FIDUCIAL



SCALE 1.000

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

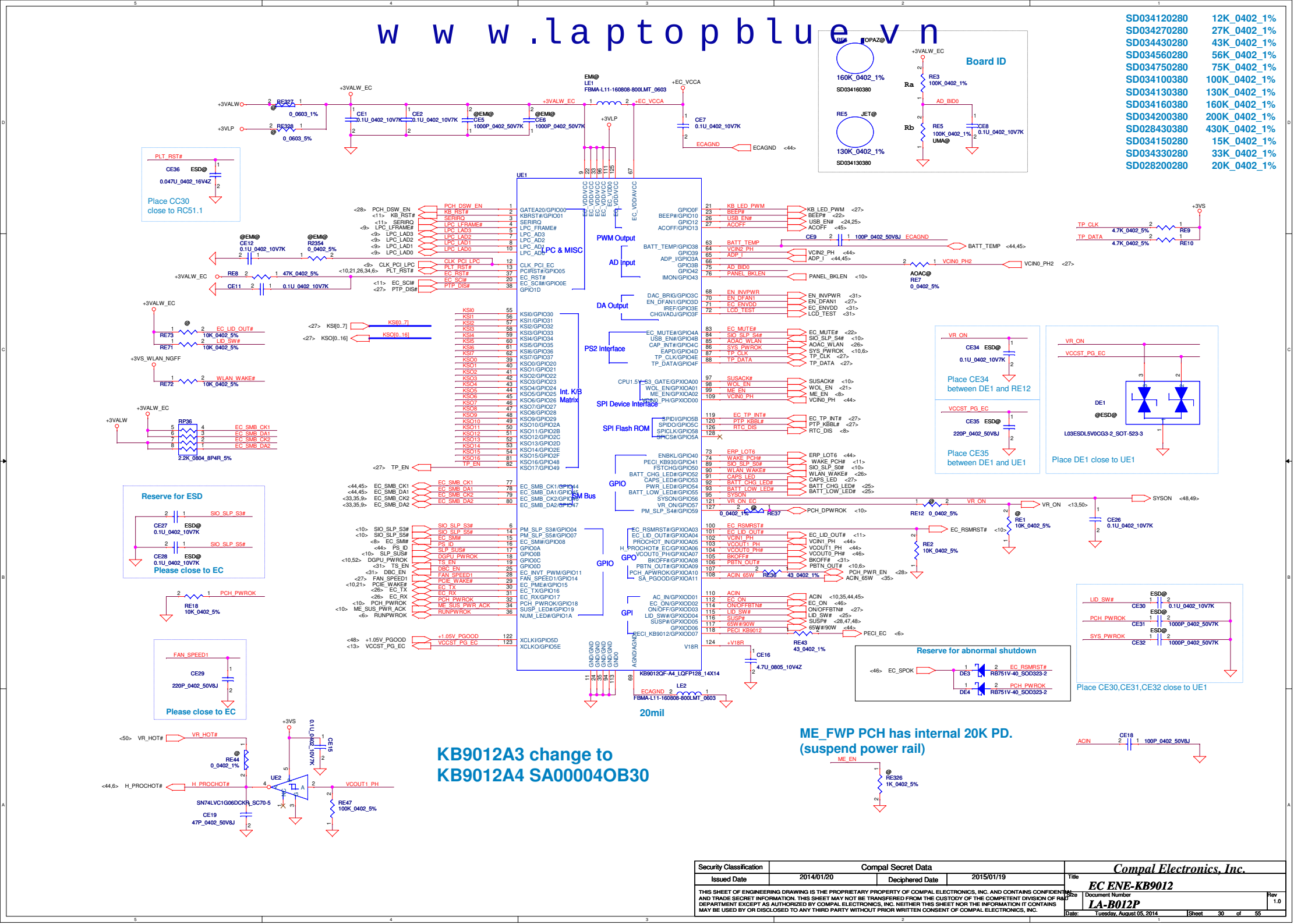
Compal Electronics, Inc.

Title: Screw Hole

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 29 of 55

SD034120280	12K_0402_1%
SD034270280	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD028430380	430K_0402_1%
SD034150280	15K_0402_1%
SD034330280	33K_0402_1%
SD028200280	20K_0402_1%



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

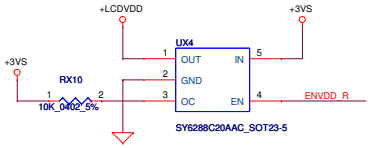
Compal Electronics, Inc.

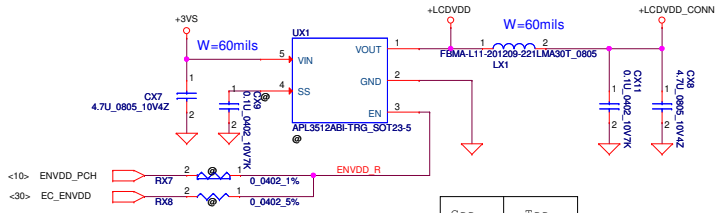
Title: EC ENE-KB9012

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 30 of 55

LCD PWR CTRL

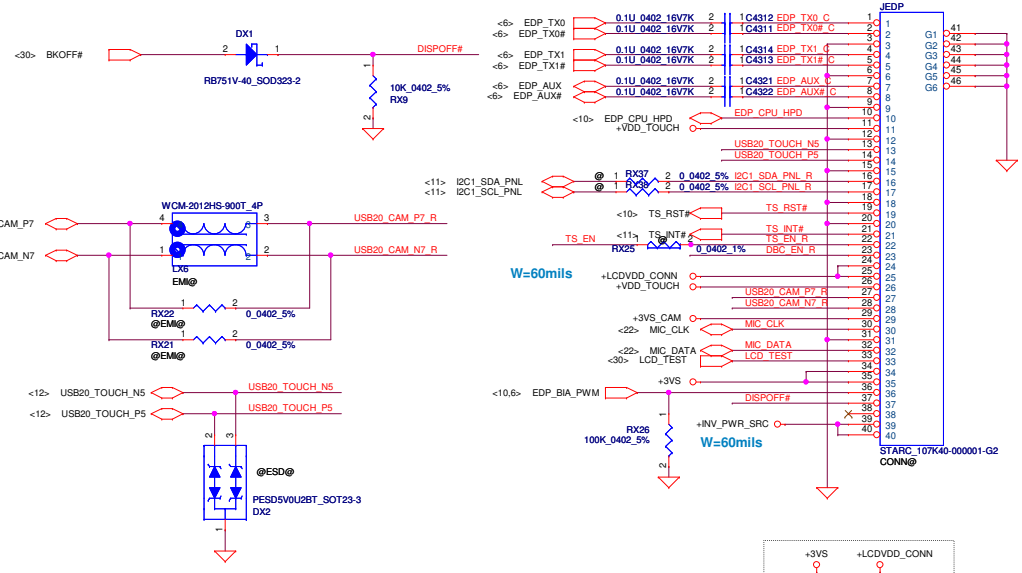




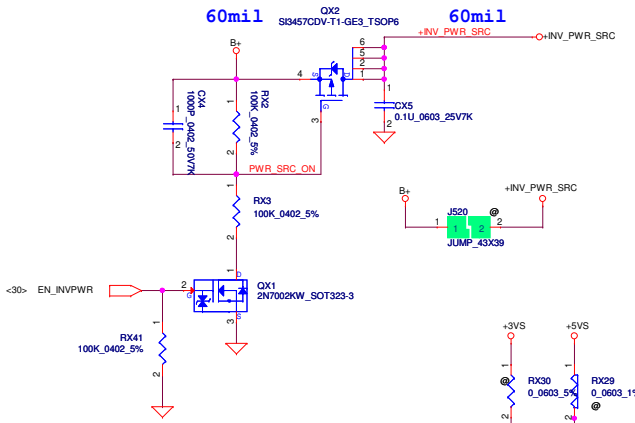
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

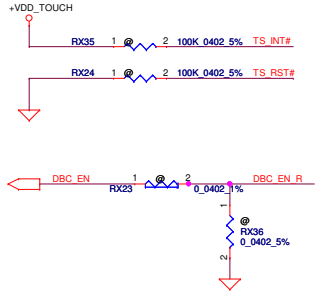
SS table

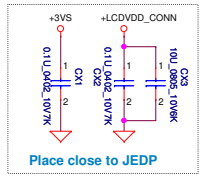
eDP Connector



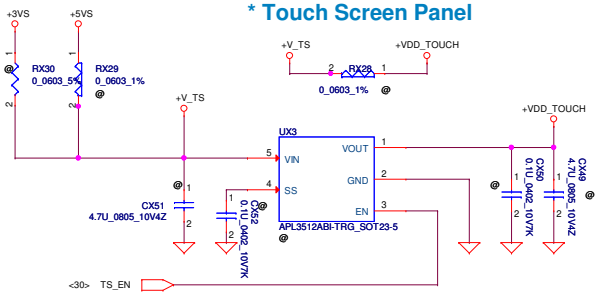
LCD backlight PWR CTRL



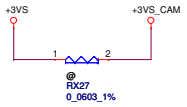


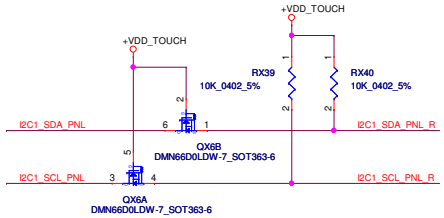


* Touch Screen Panel



Webcam PWR CTRL





Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

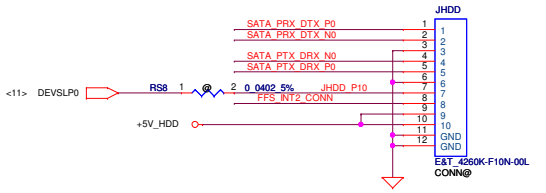
Compal Electronics, Inc.

Title: eDP / webcam / TouchScreen

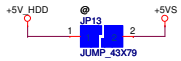
Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 31 of 55

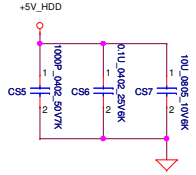
SATA HDD Connector

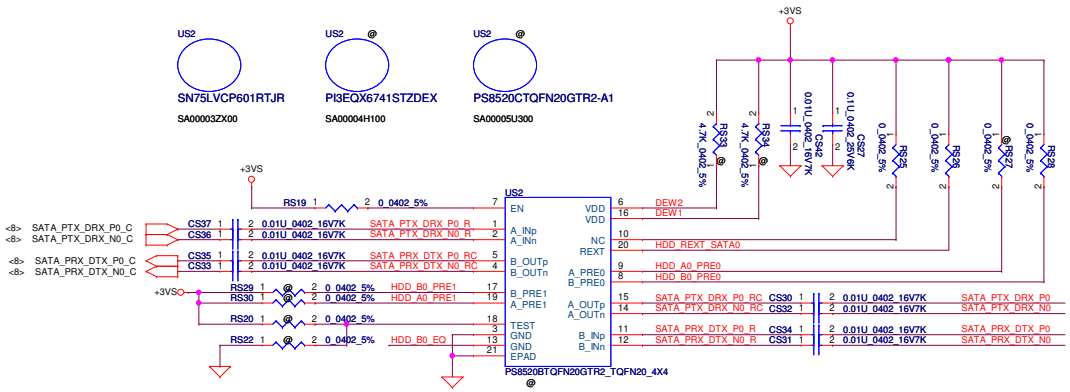


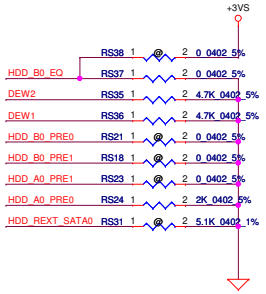
+5V_HDD Source



SHORT DEFAULT







Pin 20:
PARADE PS8250B:
Depop RS26

PERICOM PI3EQX6741ST:
Pop RS26

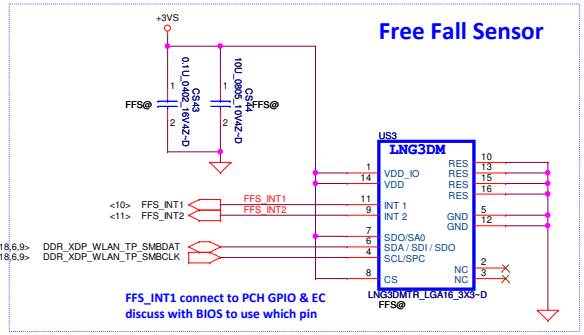
ASMEDIA ASM1466:
Pop RS26

Pin 9:
PARADE PS8250B:
Depop RS24.

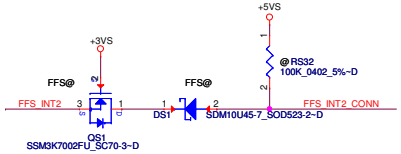
PERICOM PI3EQX6741ST:
Depop RS24

ASMEDIA ASM1466:
Pop RS24 to pull down

Free Fall Sensor



FFS_INT1 connect to PCH GPIO & EC
discuss with BIOS to use which pin



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

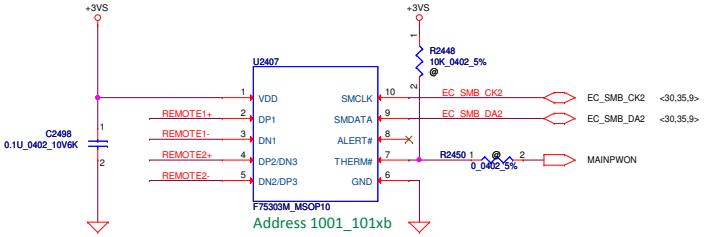
Compal Electronics, Inc.

Title: HDD

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 32 of 55

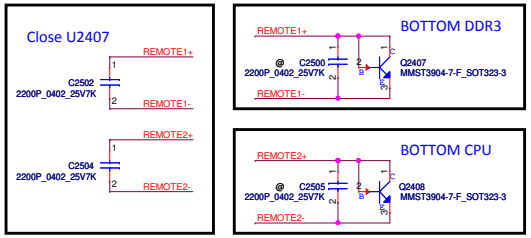
Fintek thermal sensor
placed near by TOP DDR3



Address 1001_101xb

2nd source

SA000029210-->EMC1403-2-AIZL-TR



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

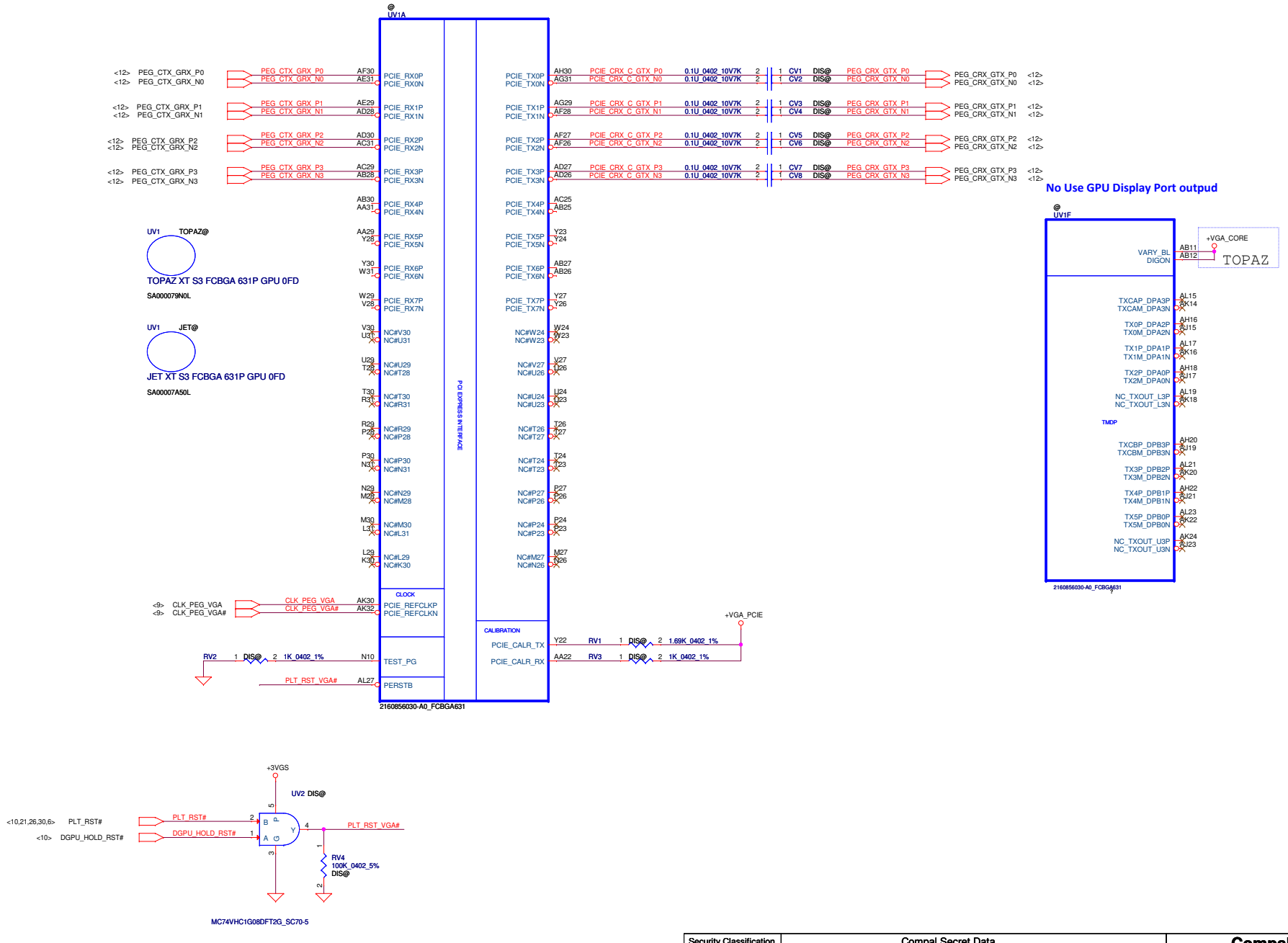
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: Thermal Sensor

Size	Document Number	Rev
	LA-B012P	1.0

Date: Tuesday, August 05, 2014 Sheet 33 of 55



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: TOPAZ_PCIE/DP

Size: Custom | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 34 of 55

Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=000
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=00

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

RV15 4.53K_0402_1% SD034453180
RV16 4.99K_0402_1% SD034499180

Memory ID	P/N	Vendor	Configuration	Size
000	SA000068U0L	SAMSUNG	K4W2G1646Q-BC1A	1GB
(default) 001	SA00006H40L	HYNIX	H5TC2G63FFR-11C	1GB
010	SA00006750L	Micron	MT41J128M16JT-093G	1GB
011	SA000076P0L	SAMSUNG	K4W4G1646B-HC11	2GB
(default) 100	SA00006E80L	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077K0L	Micron	MT41J256M16HA-093G	2GB

3.3V TO 1.8V LEVEL SHIF
For JET/SUN to support SVI2 reaulator
DNI for TOPAZ

U1 CPN is phase out

Topaz SVI2

Enable MLPS

13mA

Peak Current Control (PCC) CKT
Reversed

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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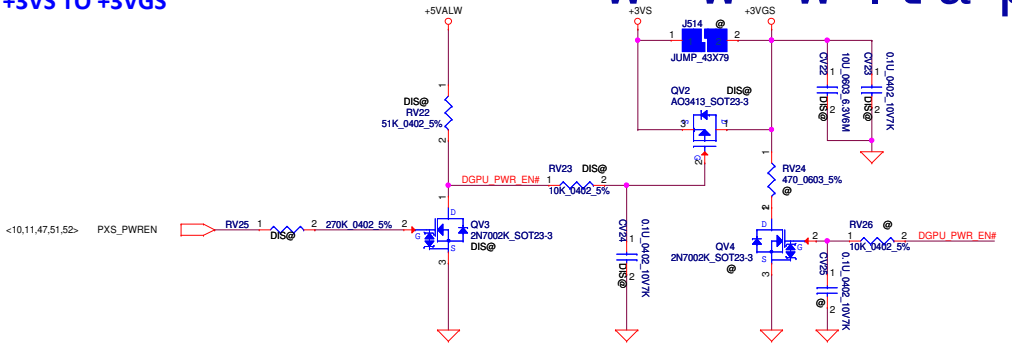
Compal Electronics, Inc.
Title: TOPAZ_MSIC
Size: Custom | Document Number: LA-B012P | Rev: 1.0
Date: Tuesday, August 05, 2014 | Sheet 35 of 55

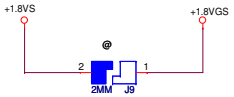
+3VS TO +3VGS



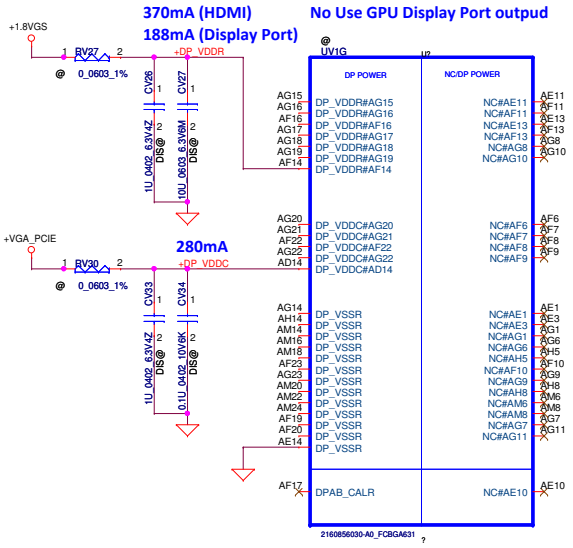
+1.35VS_VGA TO +1.35V_MEM_GFX

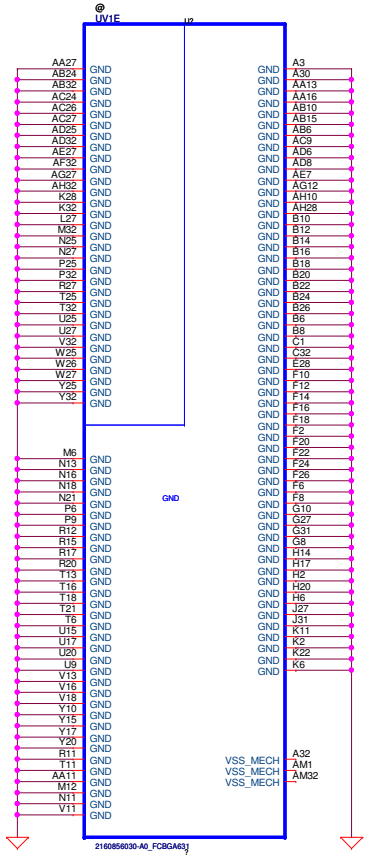
SHORT DEFAULT

+1.8VS TO +1.8VGS



SHORT DEFAULT





Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: TOPAZ_Power/GND

Size: Custom | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 36 of 55

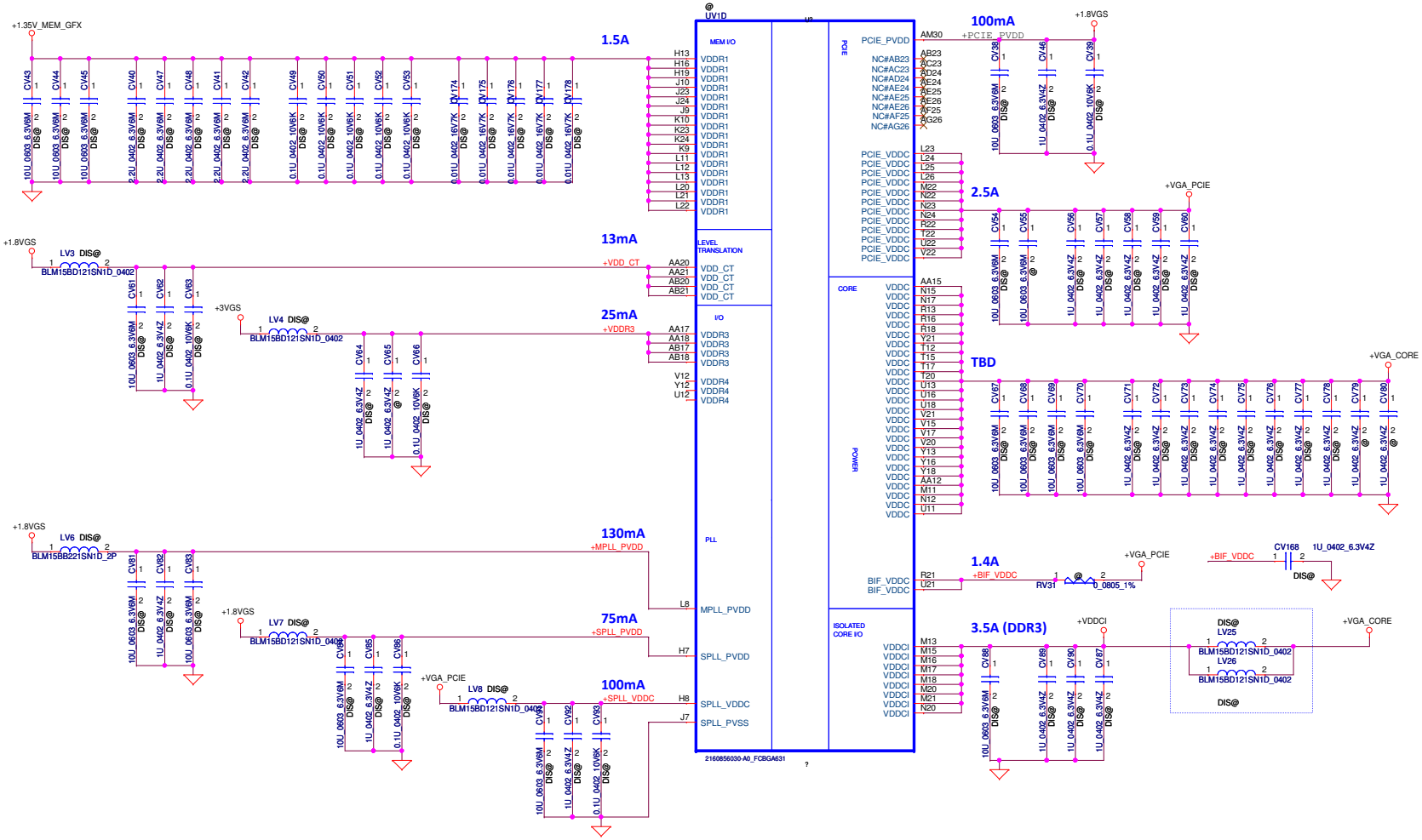
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+VGA_PCIE		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	1	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX		10uF	2.2uF	0.1uF	0.01uF
VDDR1	1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



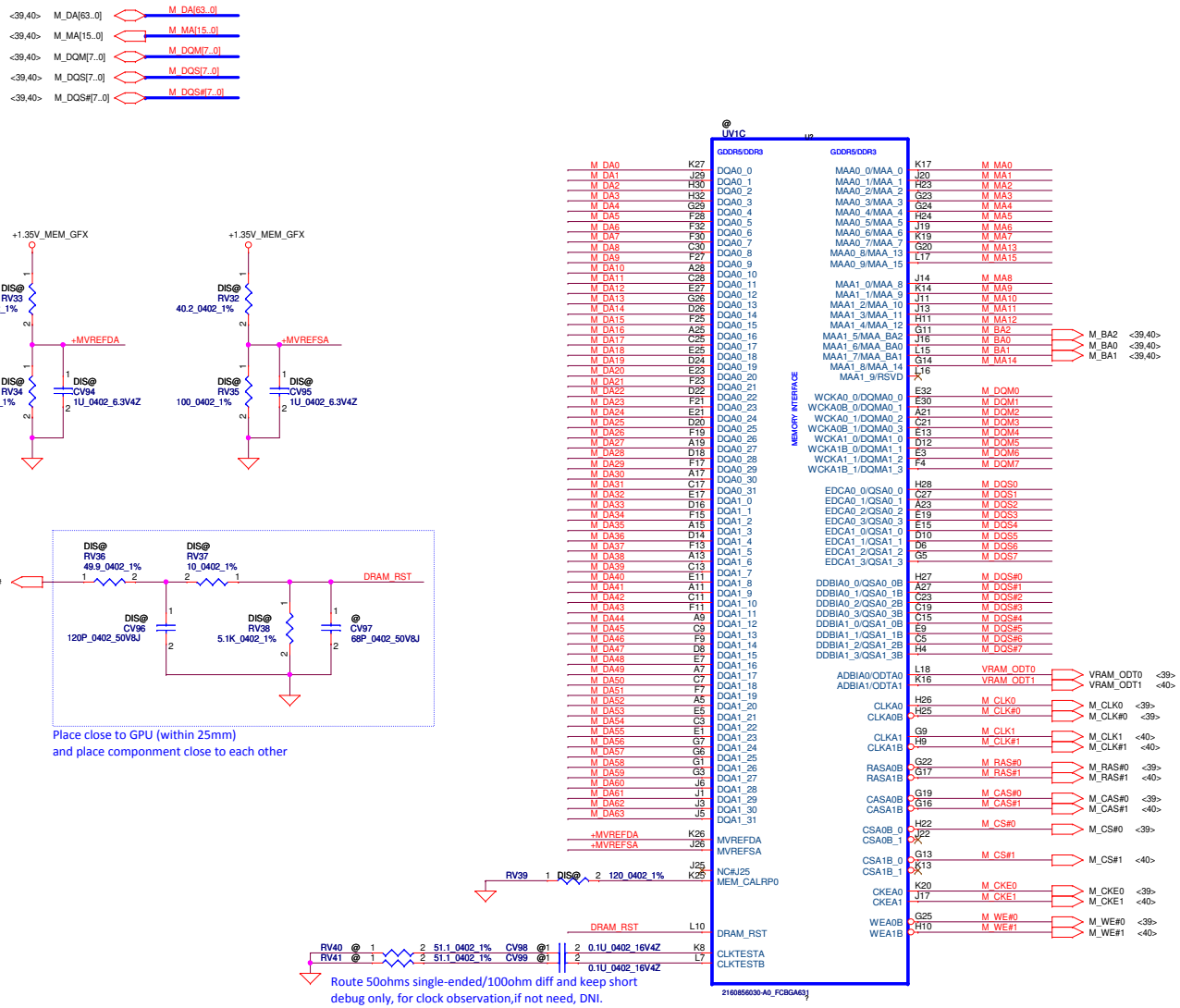
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: TOPAZ_Power

Size: Custom | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 37 of 55



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

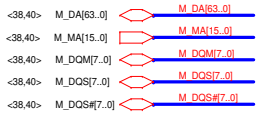
Compal Electronics, Inc.

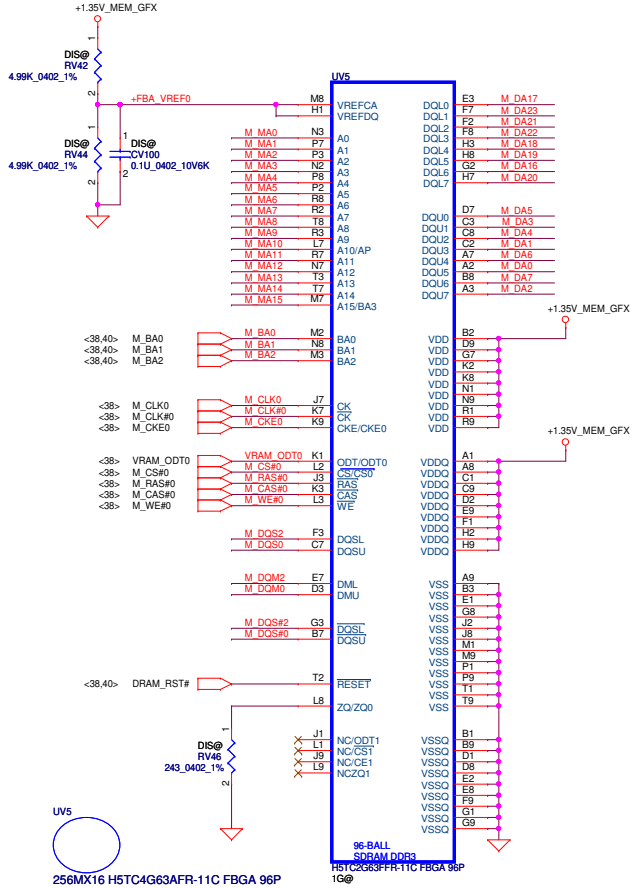
Title: **TOPAZ_MEM**

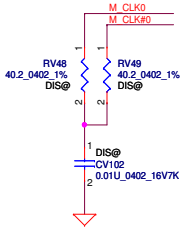
Size: Custom | Document Number: **LA-B012P** | Rev: 1.0

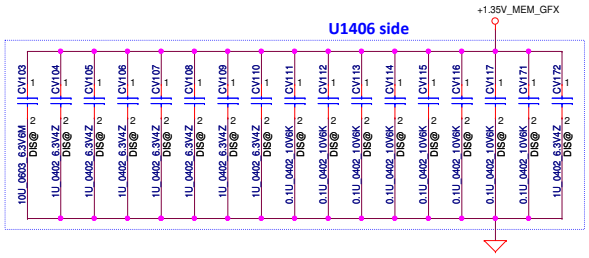
Date: Tuesday, August 05, 2014 | Sheet 38 of 55

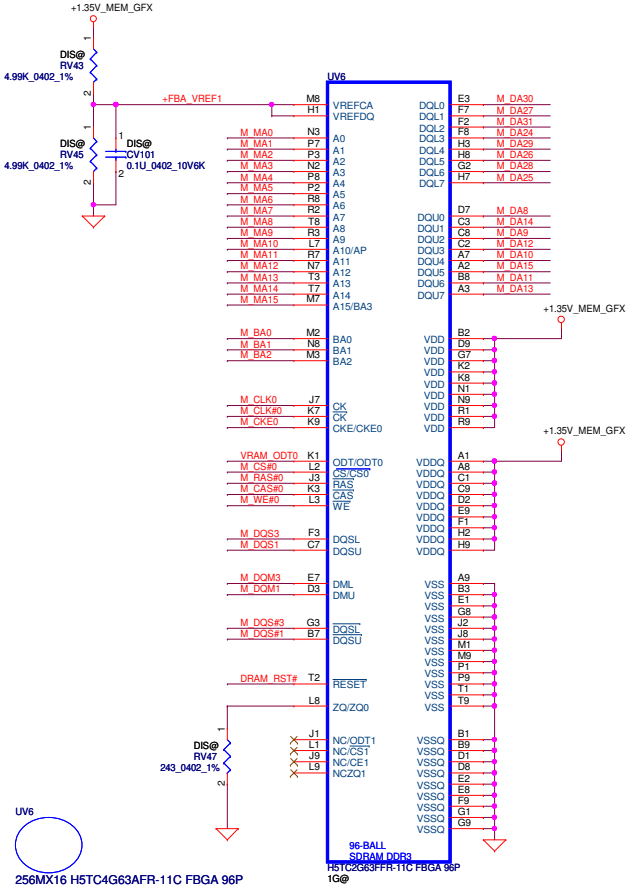
Memory Partition A - Lower 32 bits

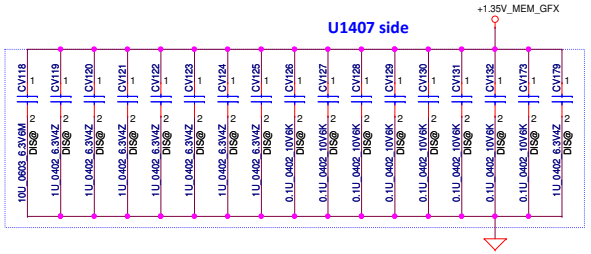












Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

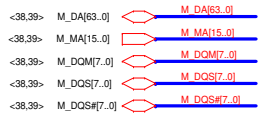
Compal Electronics, Inc.

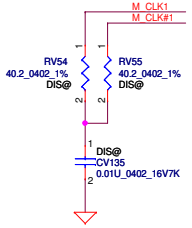
Title: TOPAZ_VRAM A Lower

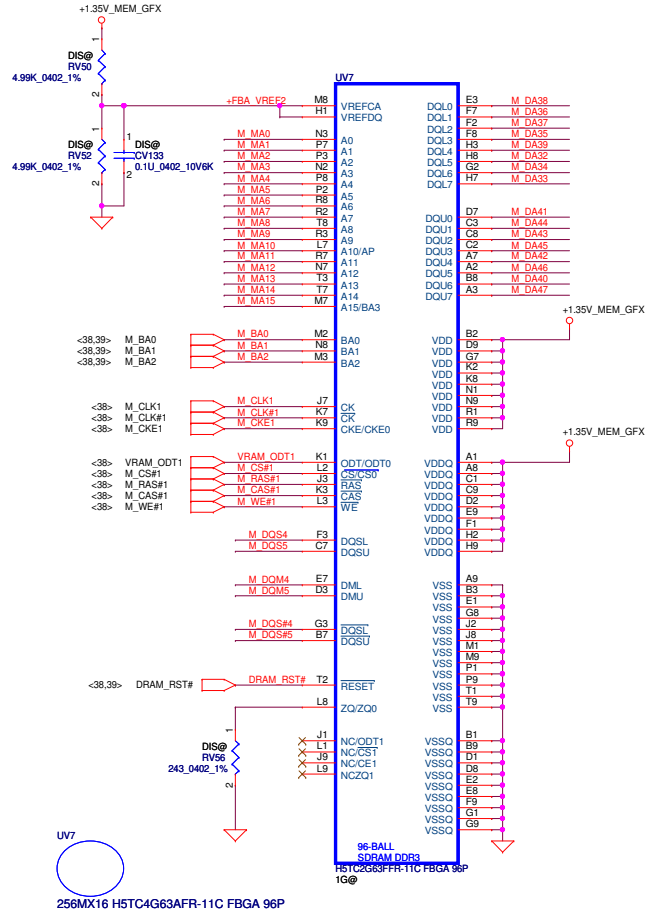
Size: Custom | Document Number: LA-B012P | Rev: 1.0

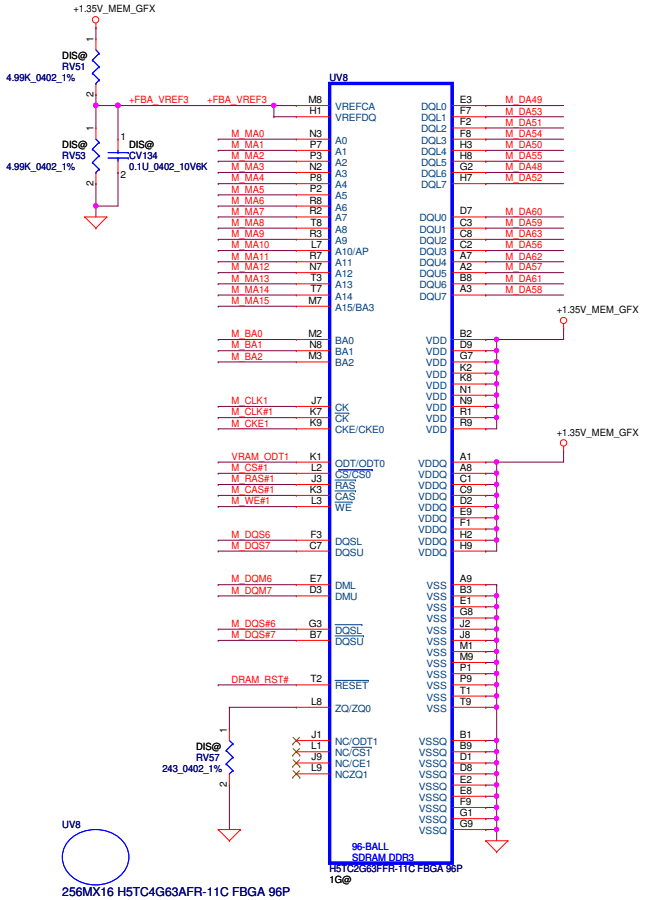
Date: Tuesday, August 05, 2014 | Sheet 39 of 55

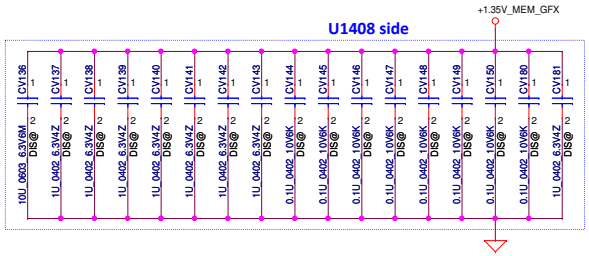
Memory Partition A - Upper 32 bits

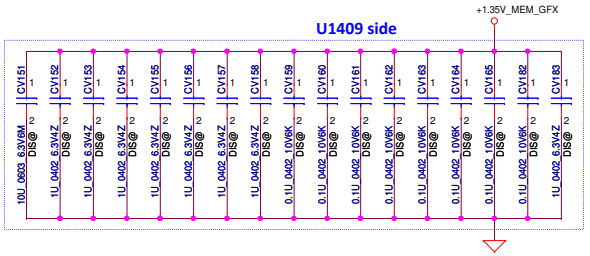












Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: TOPAZ_VRAM A Upper

Size: Custom | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 40 of 55

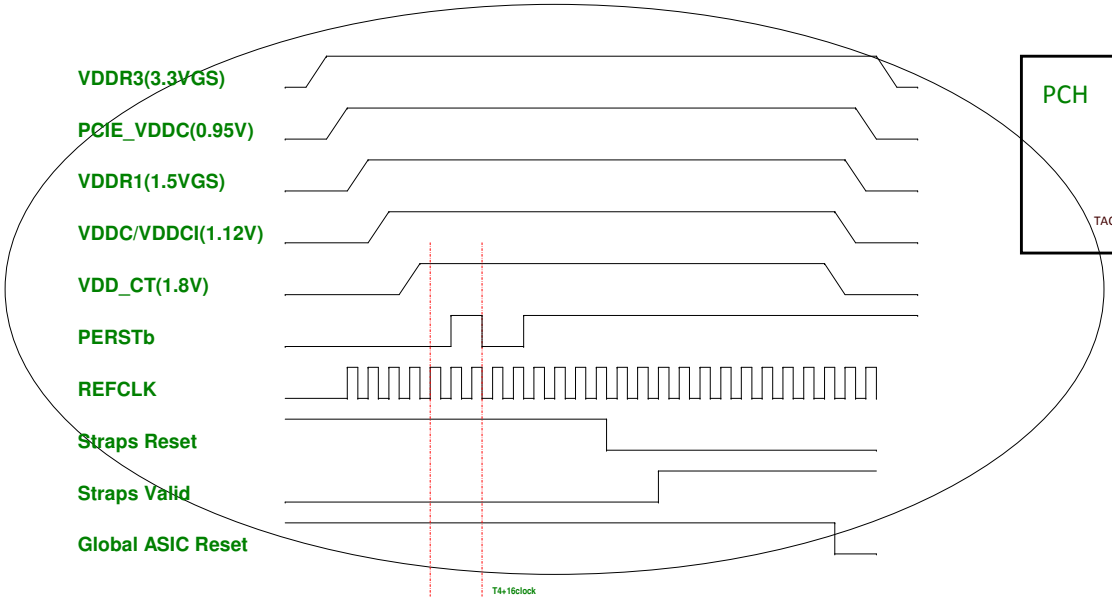
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

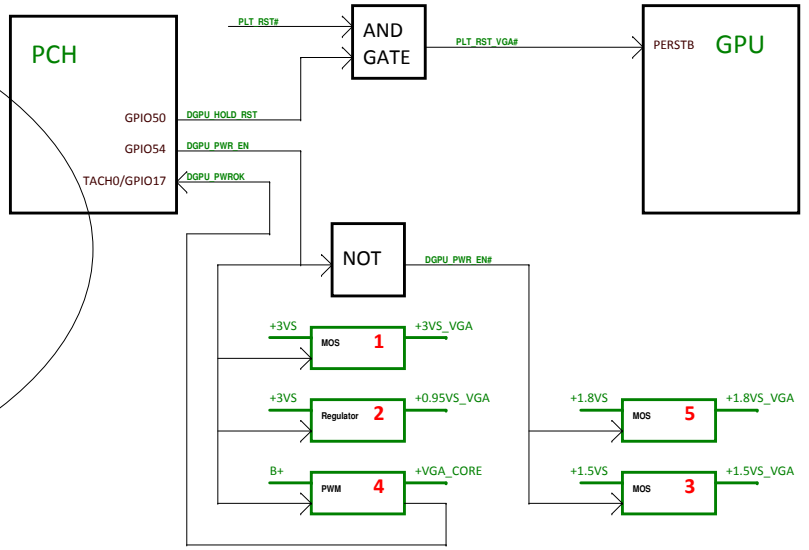
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: TOPAZ_NOTE

Size: | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 41 of 55

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: **Reserved Page**

Size | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 42 of 55

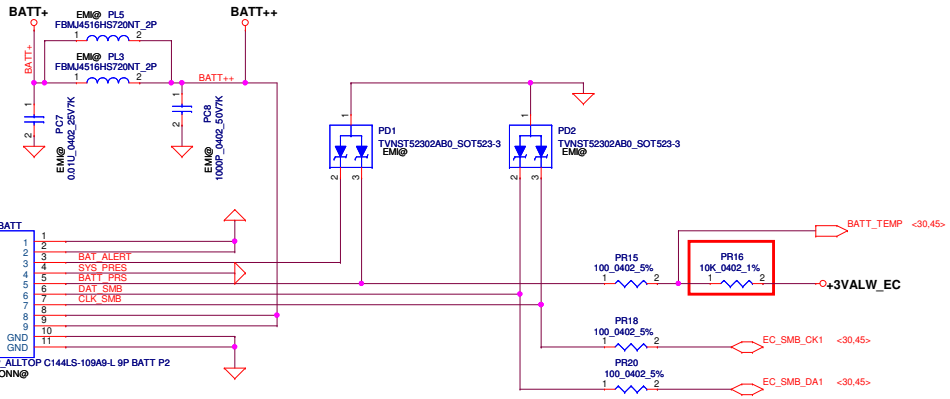
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: **Reserved Page**

Size | Document Number: **LA-B012P** | Rev: 1.0

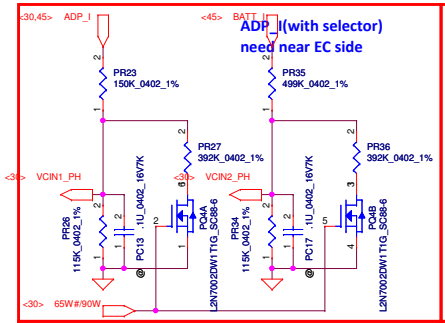
Date: Tuesday, August 05, 2014 | Sheet 43 of 55



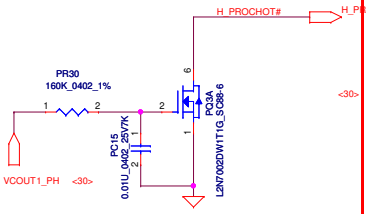
SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

Other component (37.1)

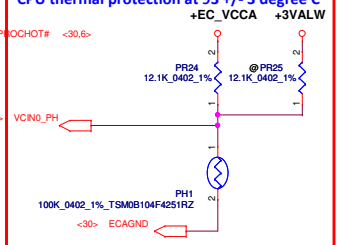
ADP_I(with selector) need near EC side



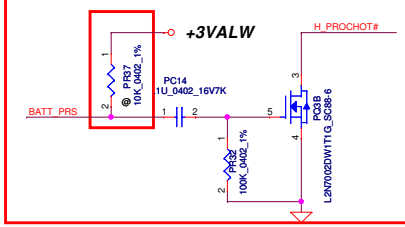
Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition



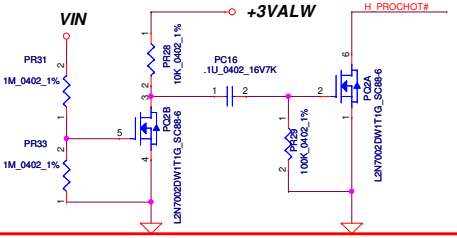
PH1 under CPU bottem side : CPU thermal protection at 93 +/- 3 degree C



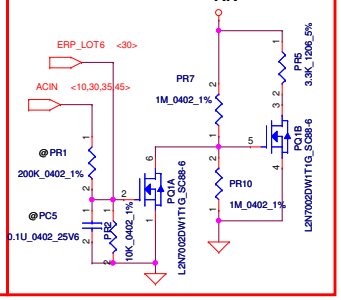
Adapter protection:
if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

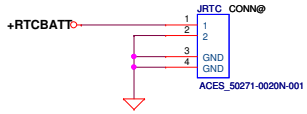


Battery protection:
asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



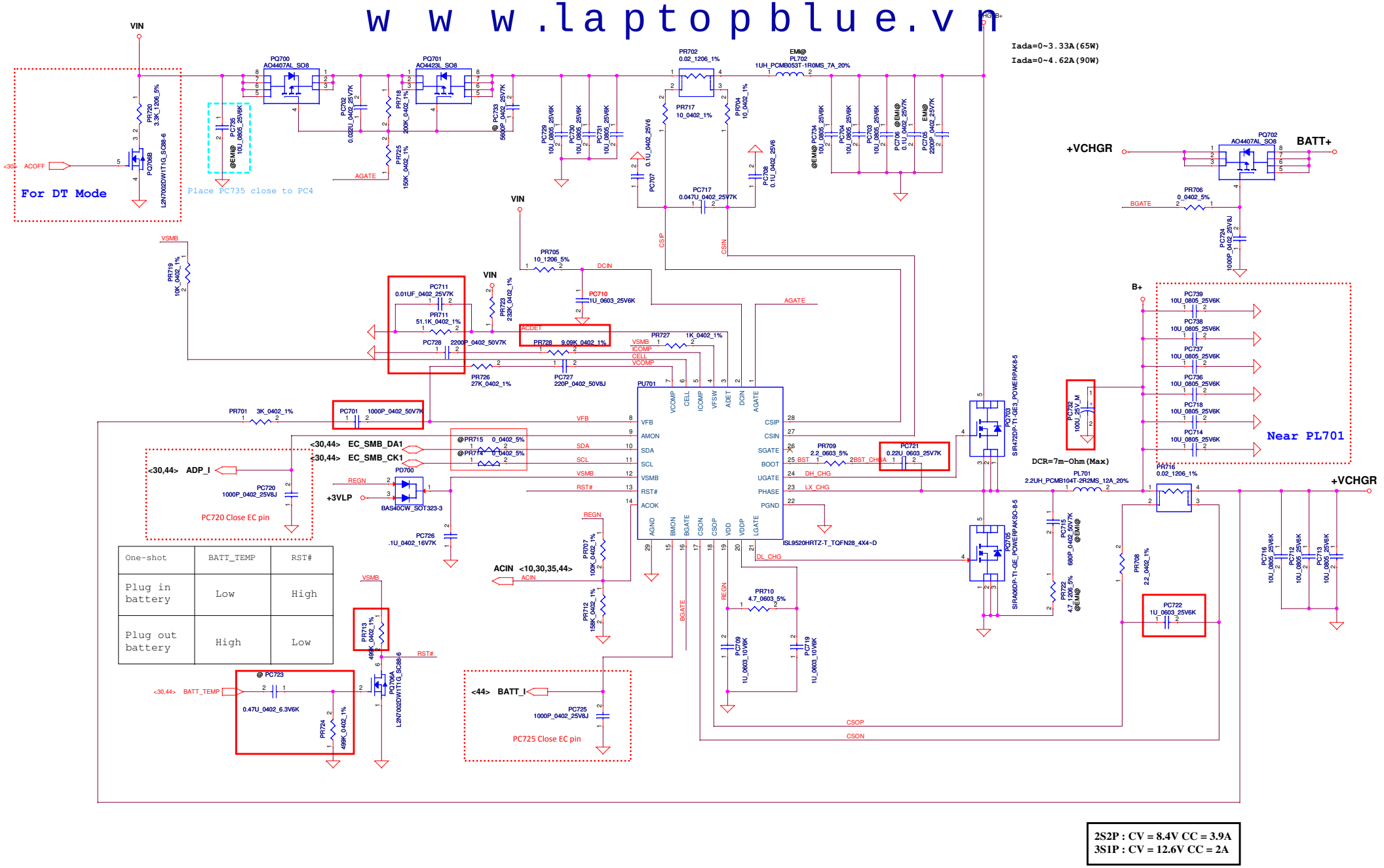
Erp lot6 Circuit





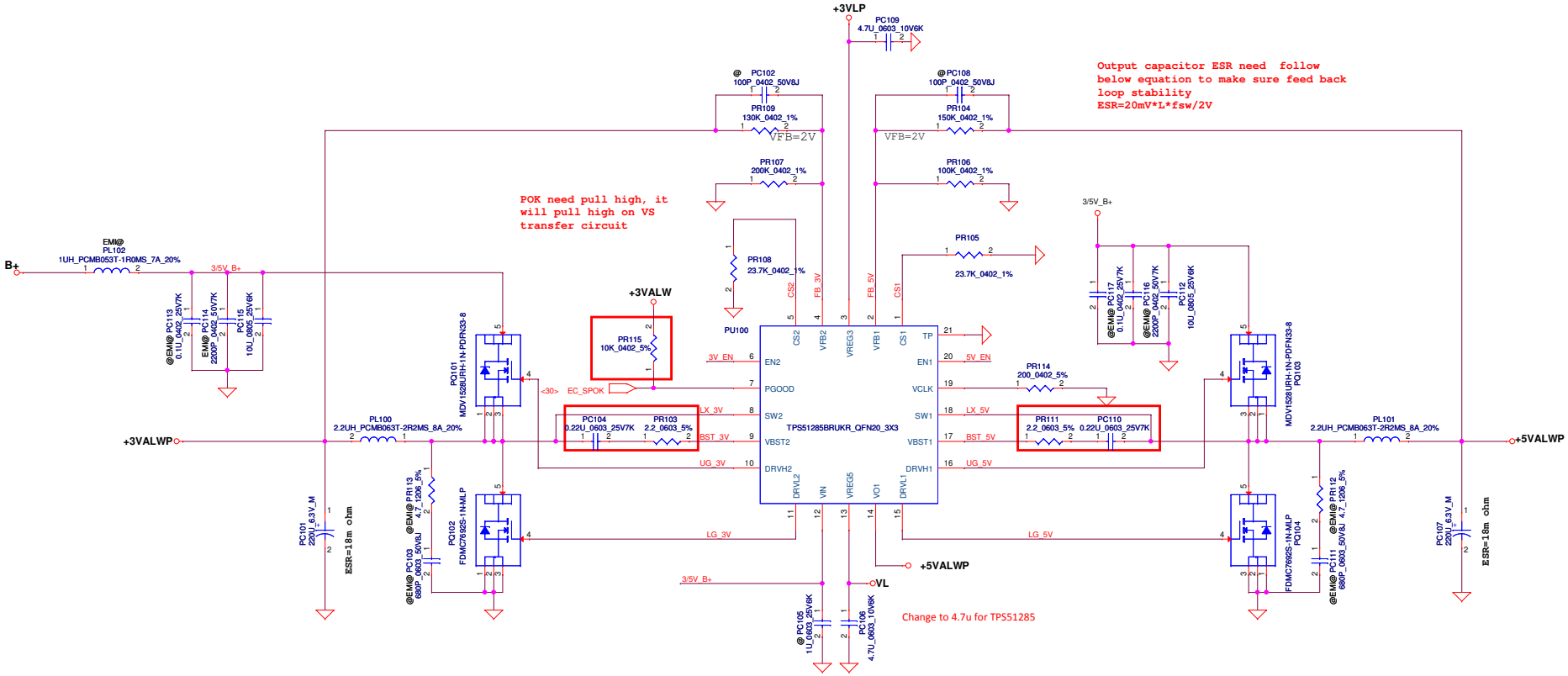
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.	
Title	PWR_DCIN/BATT CONN/OTP
Size	Document Number: LA-B012P
Rev	1.0
Date: Tuesday, August 05, 2014	Sheet 44 of 55



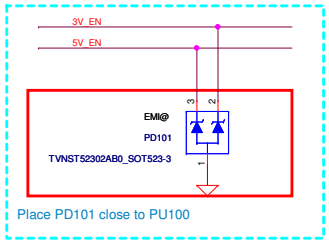
One-shot	BATT_TEMP	RST#
Plug in battery	Low	High
Plug out battery	High	Low

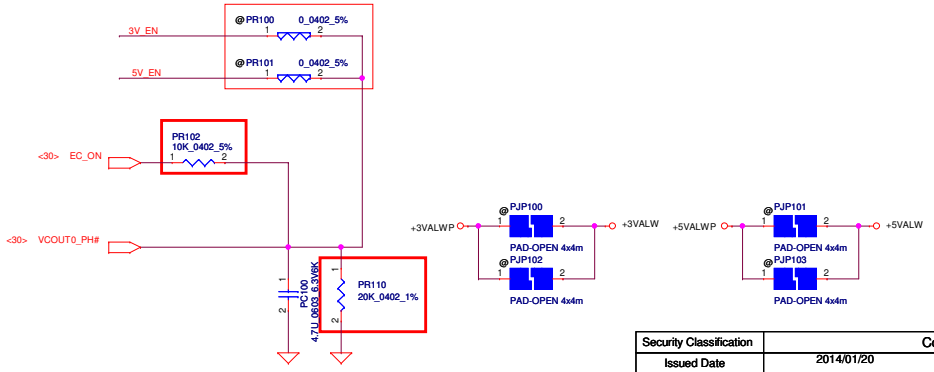
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/01/20	Deciphered Date 2015/01/19	Title: PWR_CHARGER
			Size: Document Number: LA-B012P Rev: 1.0
			Date: Tuesday, August 05, 2014 Sheet 45 of 55



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm





5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

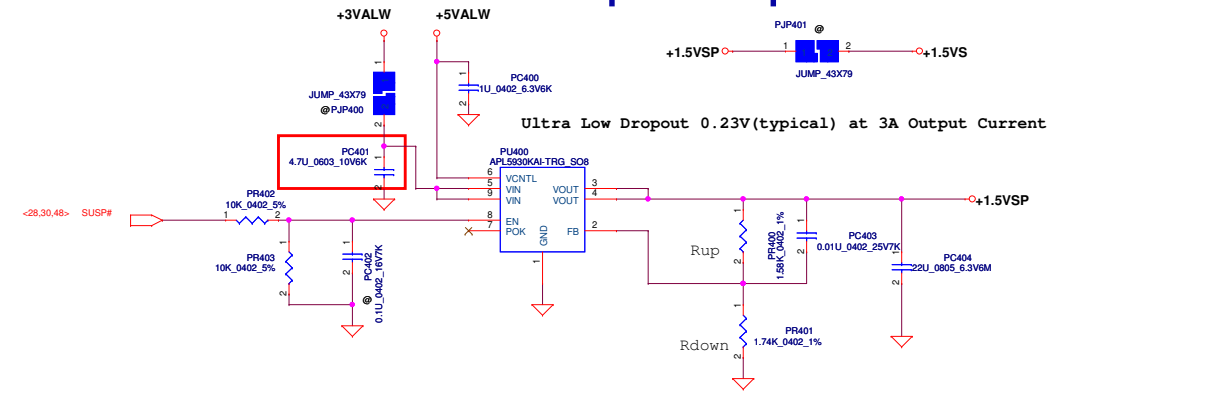
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

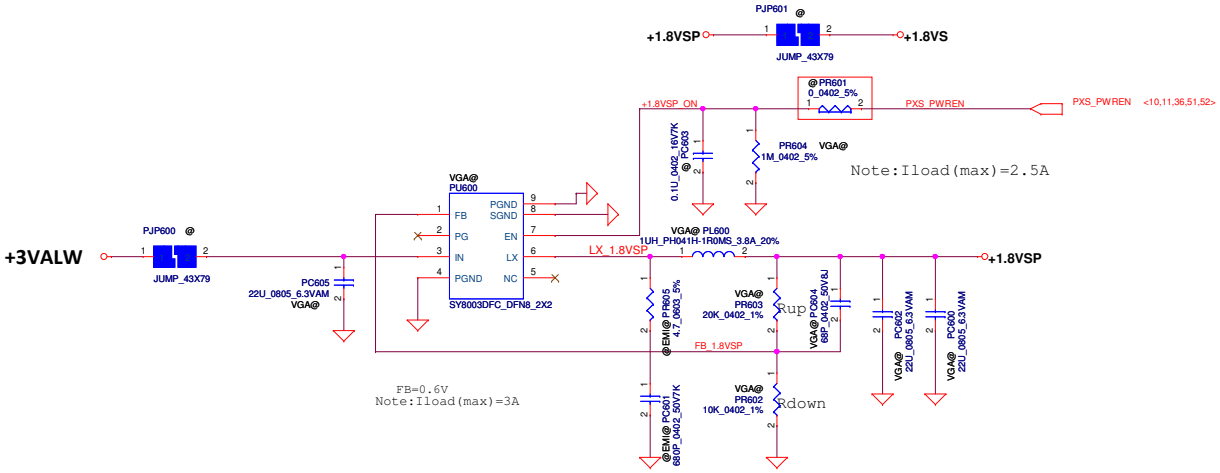
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size: | Document Number: LA-B012P | Rev: 1.0

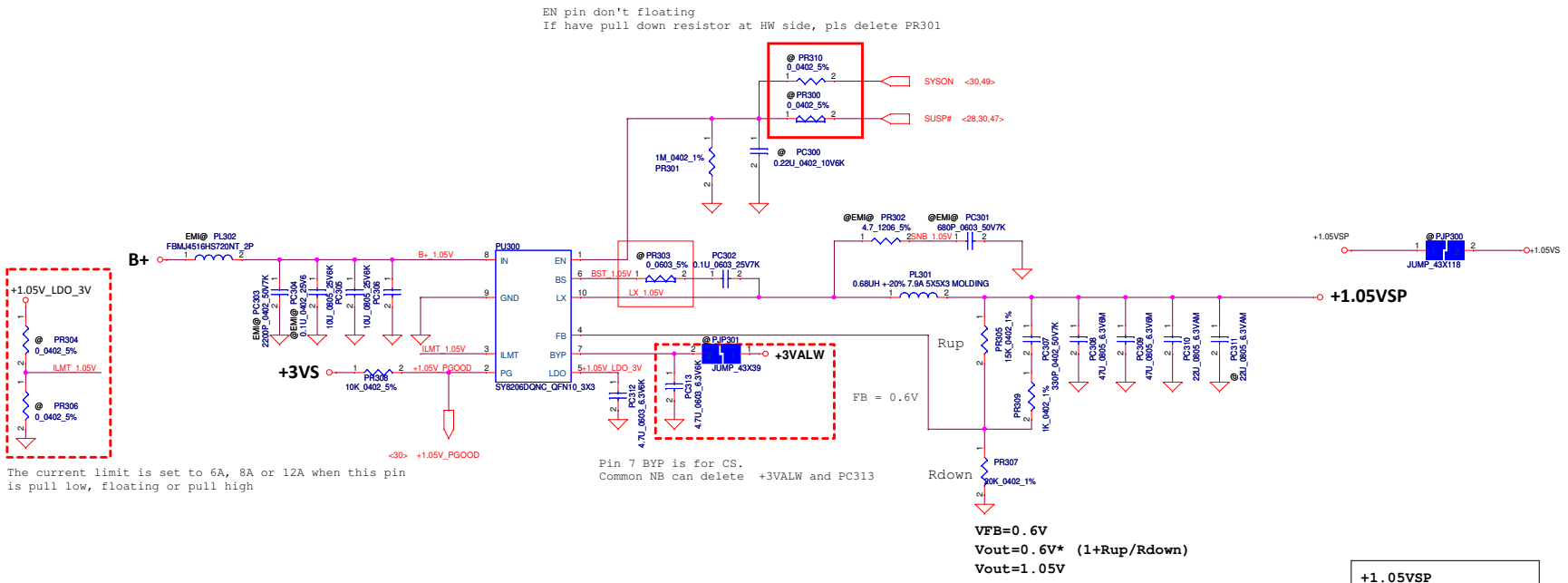
Date: Tuesday, August 05, 2014 | Sheet 46 of 55





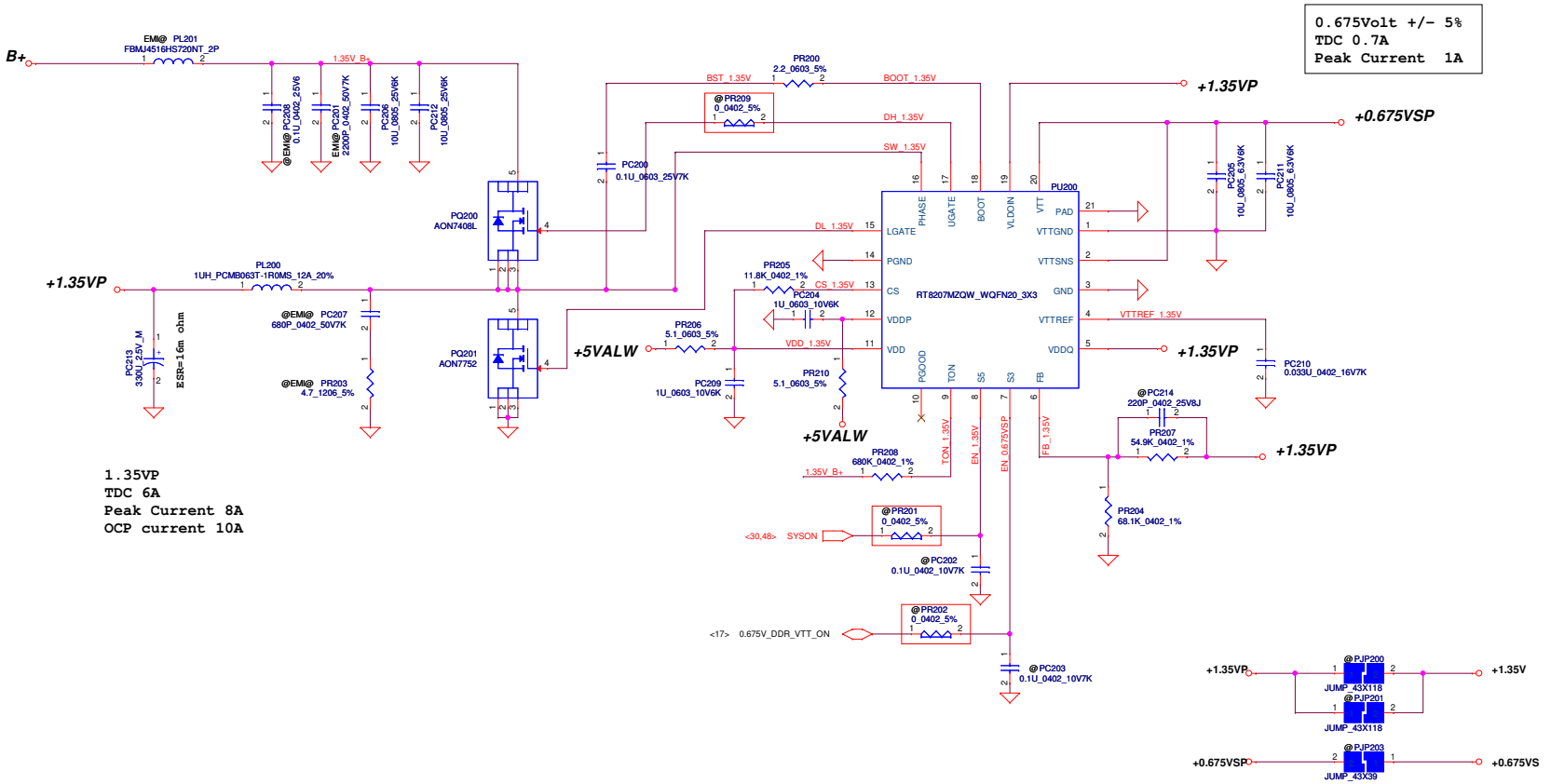
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title	PWR_1.5VSP / 1.8VSP		
Size	Document Number		Rev
	LA-B012P		1.0
Date:	Tuesday, August 05, 2014	Sheet	47 of 55



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

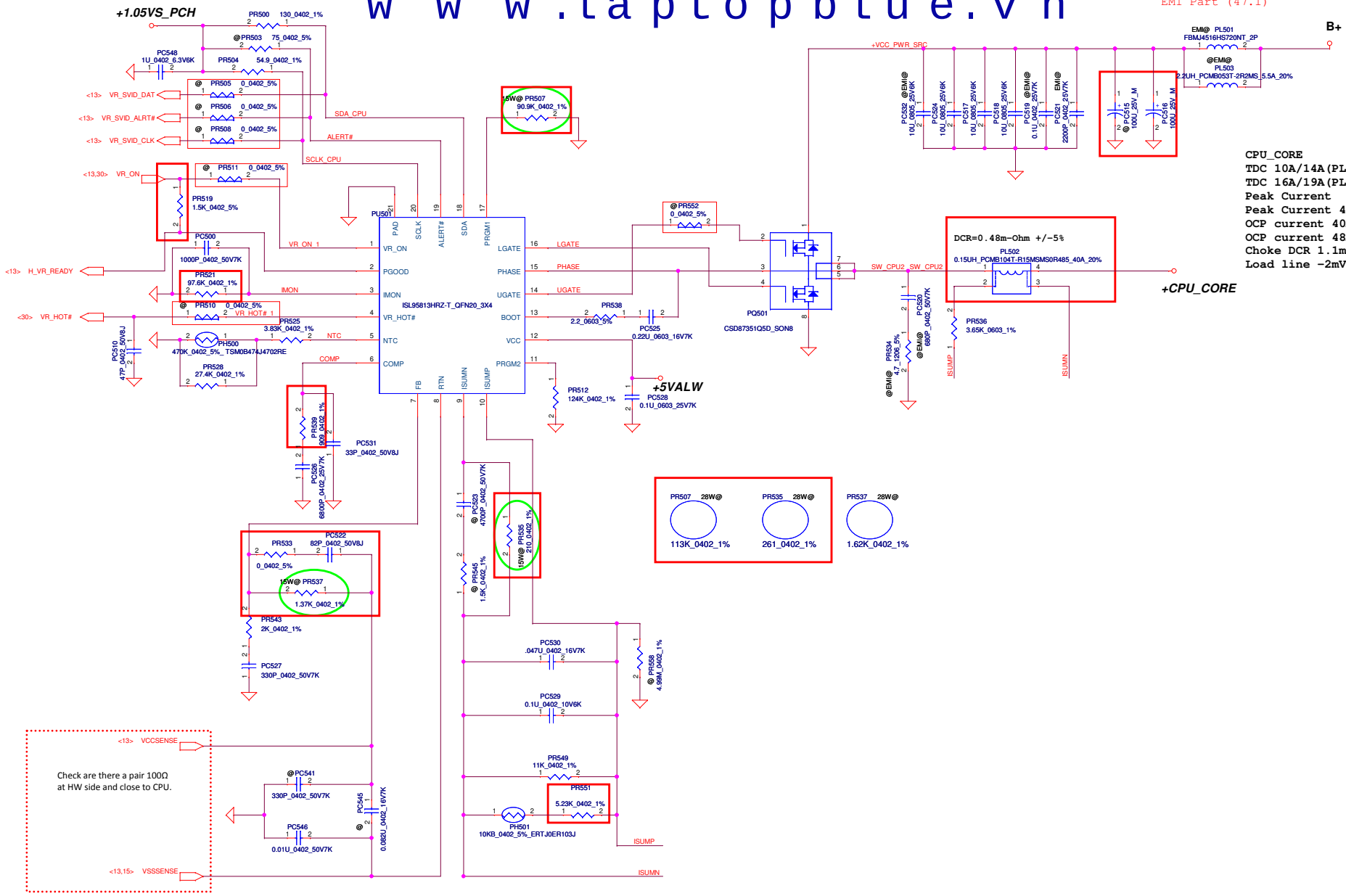
Compal Electronics, Inc.			
Title	PWR_+VCCIO		
Size C	Document Number LA-B012P		Rev 1.0
Date: Tuesday, August 05, 2014	Sheet 48 of 55		



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title: PWR_+1.35VP/0.675VSP			
Size	Document Number: LA-B012P		Rev: 1.0
Date: Tuesday, August 05, 2014	Sheet 49 of 55		

EMI Part (47.1)



CPU_CORE
TDC 10A/14A(PL2)@15W CPU
TDC 16A/19A(PL2)@28W CPU
Peak Current 32A@15W CPU
Peak Current 40A@28W CPU
OCP current 40A@15w
OCP current 48A@28W
Choke DCR 1.1m-Ohm(Max)
Load line -2mV/A

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

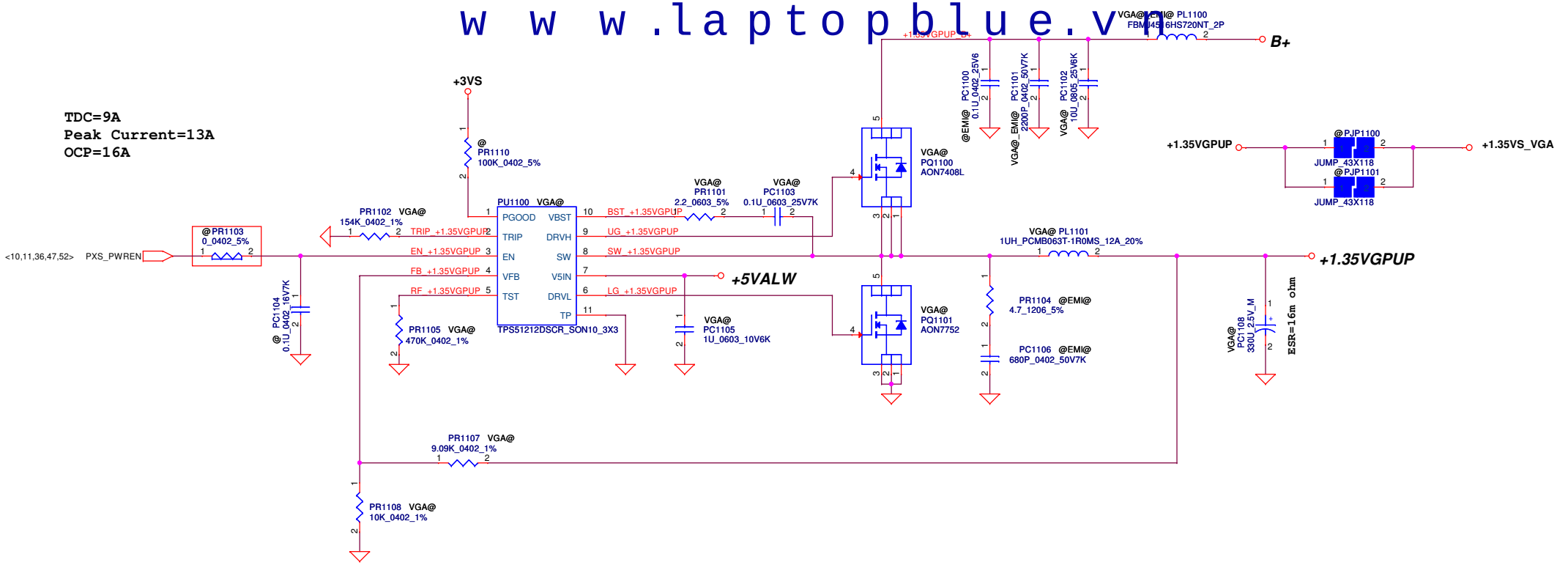
Compal Electronics, Inc.

Title: PWR_VCORE

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 50 of 55

TDC=9A
Peak Current=13A
OCP=16A



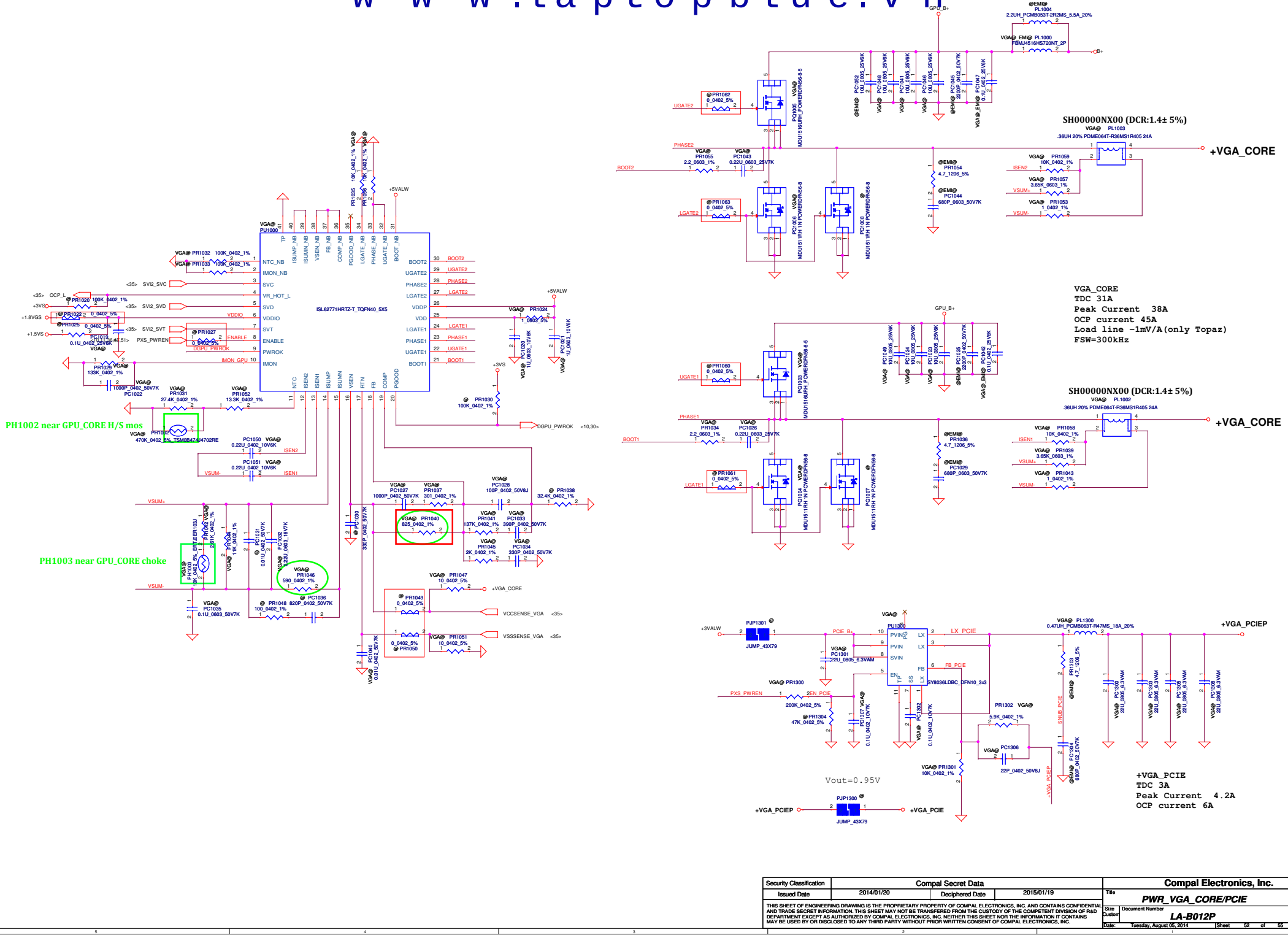
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: PWR_+1.35VGPU

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 51 of 55



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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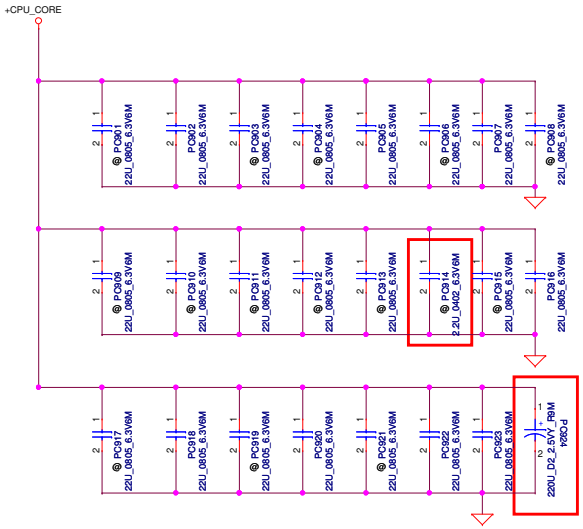
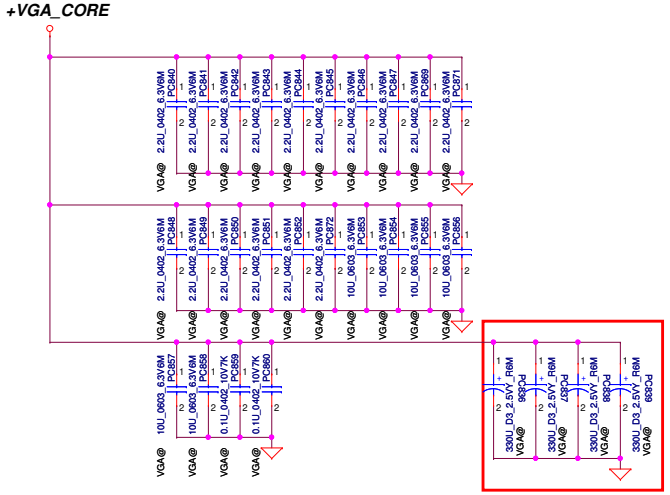
Compal Electronics, Inc.	
Title	PWR_VGA_CORE/PCIE
Size: Custom	Document Number: LA-B012P
Rev	1.0
Date: Tuesday, August 05, 2014	Sheet 52 of 55

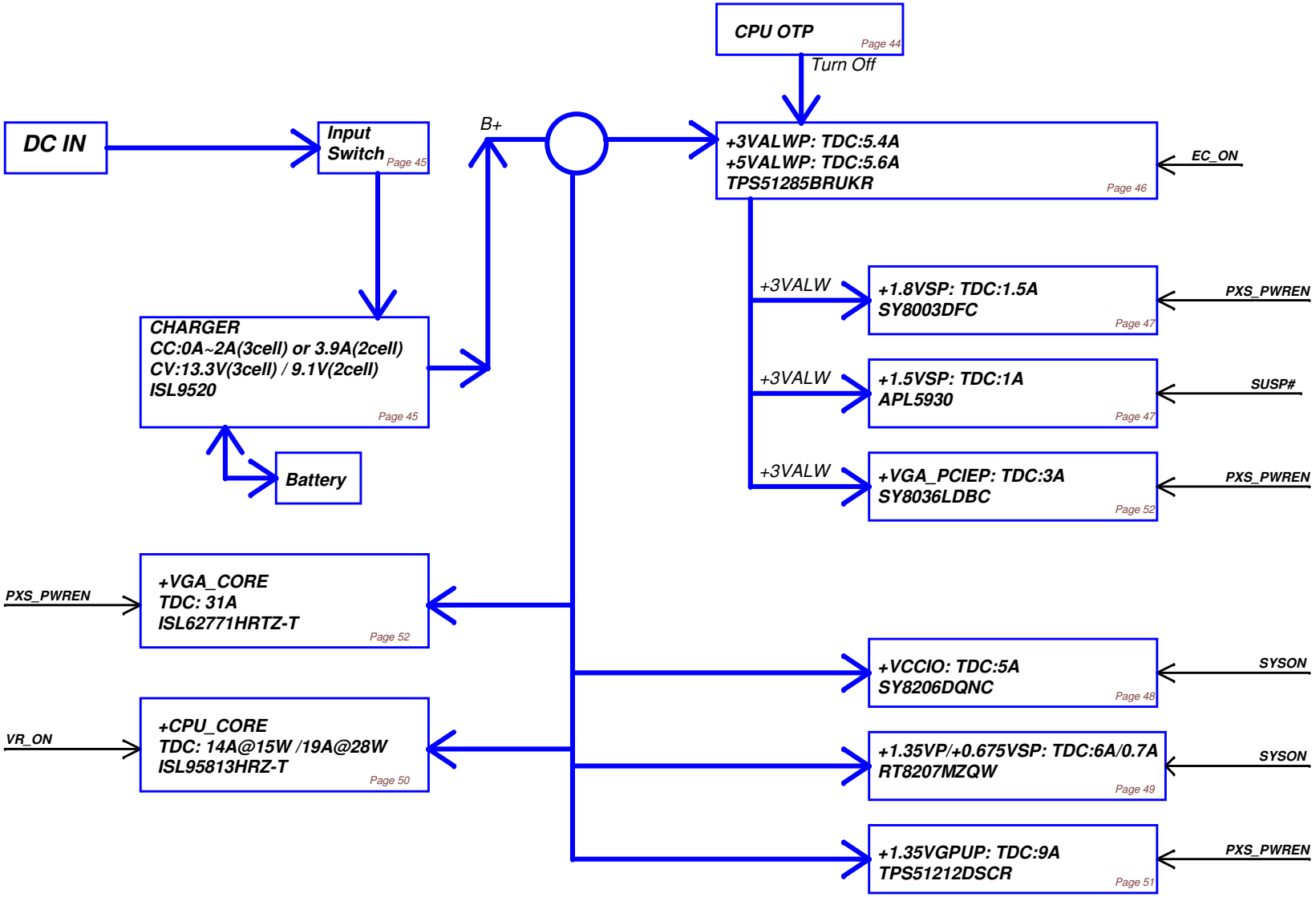




Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title: PWR_PROCESSOR DECOUPLING			
Size	Document Number: LA-B012P		Rev: 1.0
Date: Tuesday, August 05, 2014	Sheet 53 of 55		

Power block



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev
	LA-B012P		1.0
Date:	Tuesday, August 05, 2014	Sheet	54 of 55

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF000005100 to SF000004M00 change PL502 from SH00000NM00 to SH00000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

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Date: Tuesday, August 05, 2014 | Sheet 55 of 55