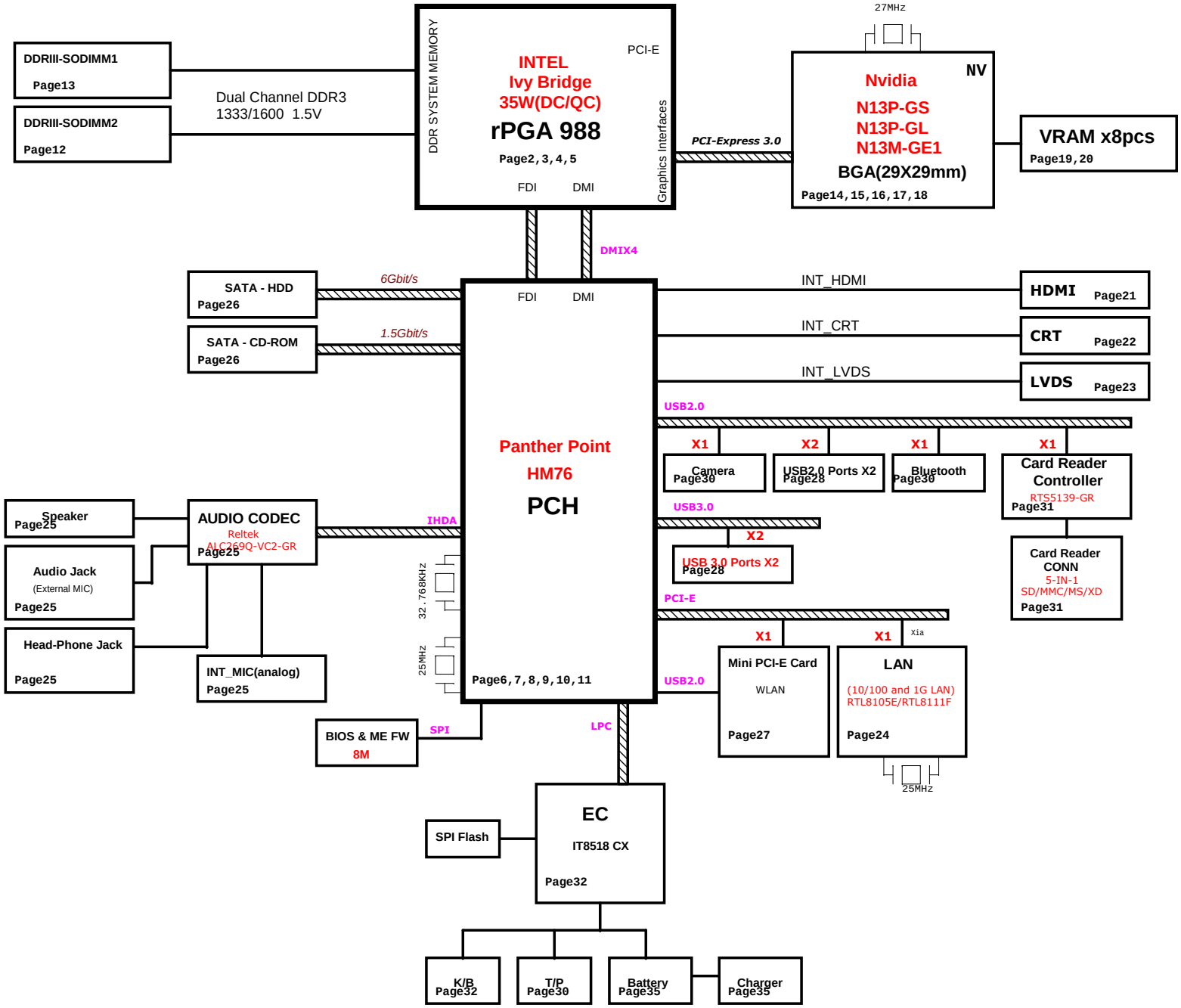
LZ2/LZ2A (Z480) Intel Chief River Platform (Optimus) Block Diagram



FAN / THERMAL
Page29

REGULATOR (DDR3)
1.5VSUS, 0.75VSMDDR_VTERM,1.5V
1.5V_GPU,1.5V_CPU Page37

REGULATOR
+1.05V_VTT,+1.8V Page38

DC/DC
3VPCU, 5VPCU, +15V
Page36 PG 42

CPU Core
Page41 PG 43

VGA Core Discrete
Page42,43 PG 44

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Front page	1A

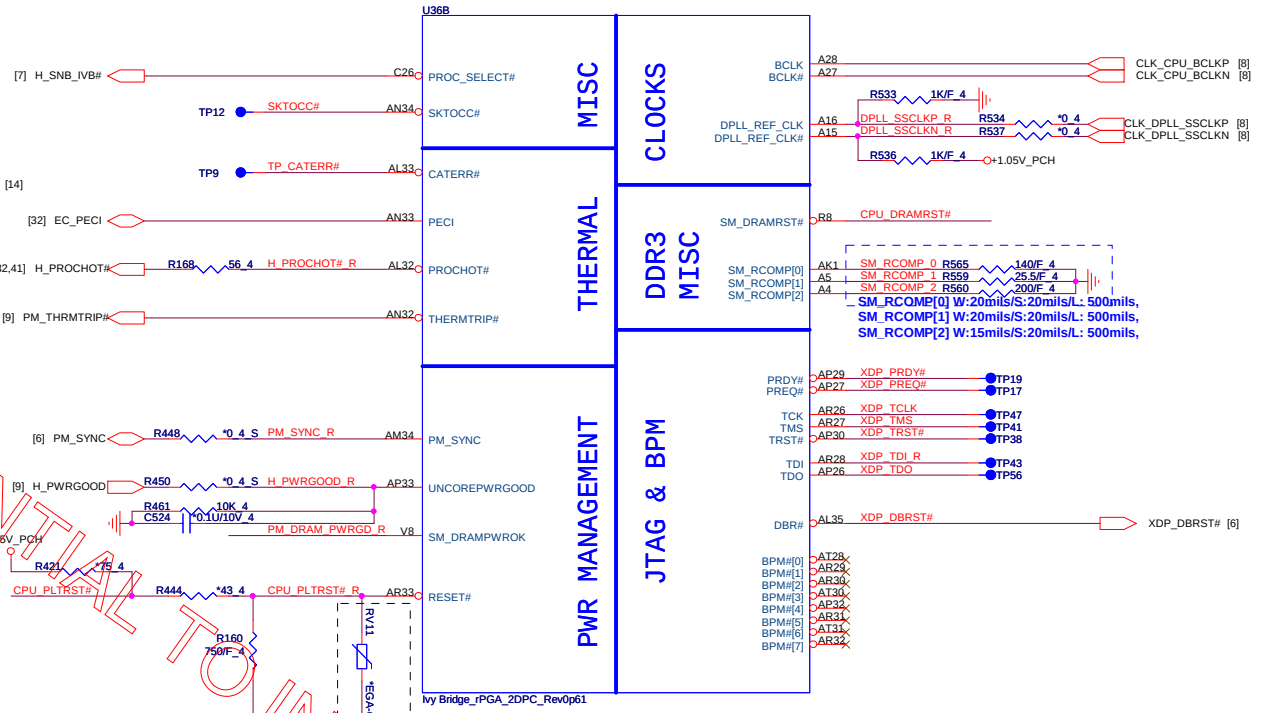
Date: Wednesday, November 30, 2011 Sheet 1 of 45

Ivy Bridge Processor (DMI,PEG,FDI)

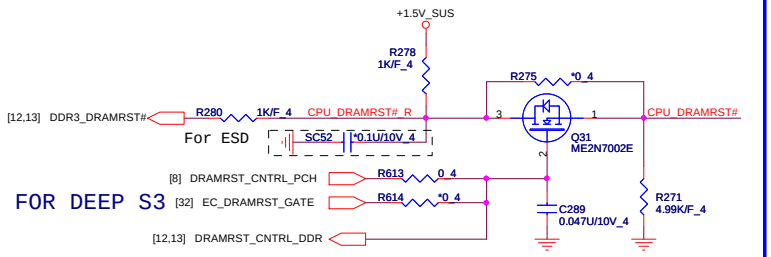
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

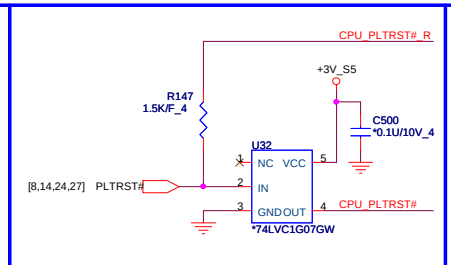
eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils. eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

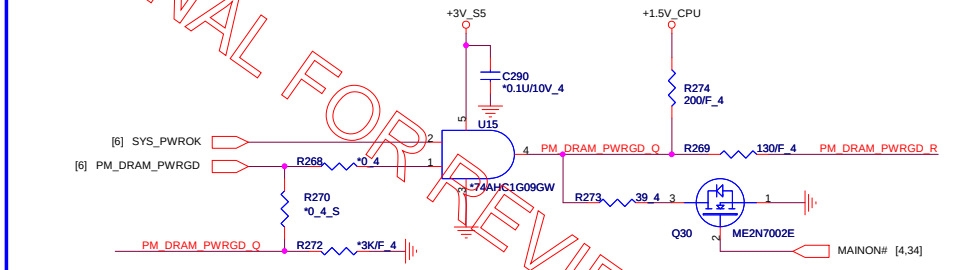
Ivy Bridge Processor (CLK,MISC,JTAG)



SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,







PEG x16 (UMA Non-stuff)

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXP[0..15] [14]

PEG_TXP0_C	C499	DIS@0.1U/10V/X5R_4 PEG_TXP0
PEG_TXP1_C	C475	DIS@0.1U/10V/X5R_4 PEG_TXP1
PEG_TXP2_C	C513	DIS@0.1U/10V/X5R_4 PEG_TXP2
PEG_TXP3_C	C493	DIS@0.1U/10V/X5R_4 PEG_TXP3
PEG_TXP4_C	C487	DIS@0.1U/10V/X5R_4 PEG_TXP4
PEG_TXP5_C	C508	DIS@0.1U/10V/X5R_4 PEG_TXP5
PEG_TXP6_C	C477	DIS@0.1U/10V/X5R_4 PEG_TXP6
PEG_TXP7_C	C504	DIS@0.1U/10V/X5R_4 PEG_TXP7
PEG_TXP8_C	C478	DIS@0.1U/10V/X5R_4 PEG_TXP8
PEG_TXP9_C	C502	DIS@0.1U/10V/X5R_4 PEG_TXP9
PEG_TXP10_C	C481	DIS@0.1U/10V/X5R_4 PEG_TXP10
PEG_TXP11_C	C494	DIS@0.1U/10V/X5R_4 PEG_TXP11
PEG_TXP12_C	C483	DIS@0.1U/10V/X5R_4 PEG_TXP12
PEG_TXP13_C	C491	DIS@0.1U/10V/X5R_4 PEG_TXP13
PEG_TXP14_C	C484	DIS@0.1U/10V/X5R_4 PEG_TXP14
PEG_TXP15_C	C497	DIS@0.1U/10V/X5R_4 PEG_TXP15

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXN[0..15] [14]

PEG_TXN0_C	C498	DIS@0.1U/10V/X5R_4 PEG_TXN0
PEG_TXN1_C	C474	DIS@0.1U/10V/X5R_4 PEG_TXN1
PEG_TXN2_C	C514	DIS@0.1U/10V/X5R_4 PEG_TXN2
PEG_TXN3_C	C492	DIS@0.1U/10V/X5R_4 PEG_TXN3
PEG_TXN4_C	C486	DIS@0.1U/10V/X5R_4 PEG_TXN4
PEG_TXN5_C	C509	DIS@0.1U/10V/X5R_4 PEG_TXN5
PEG_TXN6_C	C476	DIS@0.1U/10V/X5R_4 PEG_TXN6
PEG_TXN7_C	C503	DIS@0.1U/10V/X5R_4 PEG_TXN7
PEG_TXN8_C	C479	DIS@0.1U/10V/X5R_4 PEG_TXN8
PEG_TXN9_C	C501	DIS@0.1U/10V/X5R_4 PEG_TXN9
PEG_TXN10_C	C480	DIS@0.1U/10V/X5R_4 PEG_TXN10
PEG_TXN11_C	C495	DIS@0.1U/10V/X5R_4 PEG_TXN11
PEG_TXN12_C	C482	DIS@0.1U/10V/X5R_4 PEG_TXN12
PEG_TXN13_C	C490	DIS@0.1U/10V/X5R_4 PEG_TXN13
PEG_TXN14_C	C485	DIS@0.1U/10V/X5R_4 PEG_TXN14
PEG_TXN15_C	C496	DIS@0.1U/10V/X5R_4 PEG_TXN15

DP & PEG Compensation

+1.05V_PCH R527 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

+1.05V_PCH R532 *10K_4 INT_eDP_HPD_Q

+1.05V_PCH R528 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

+1.05V_PCH

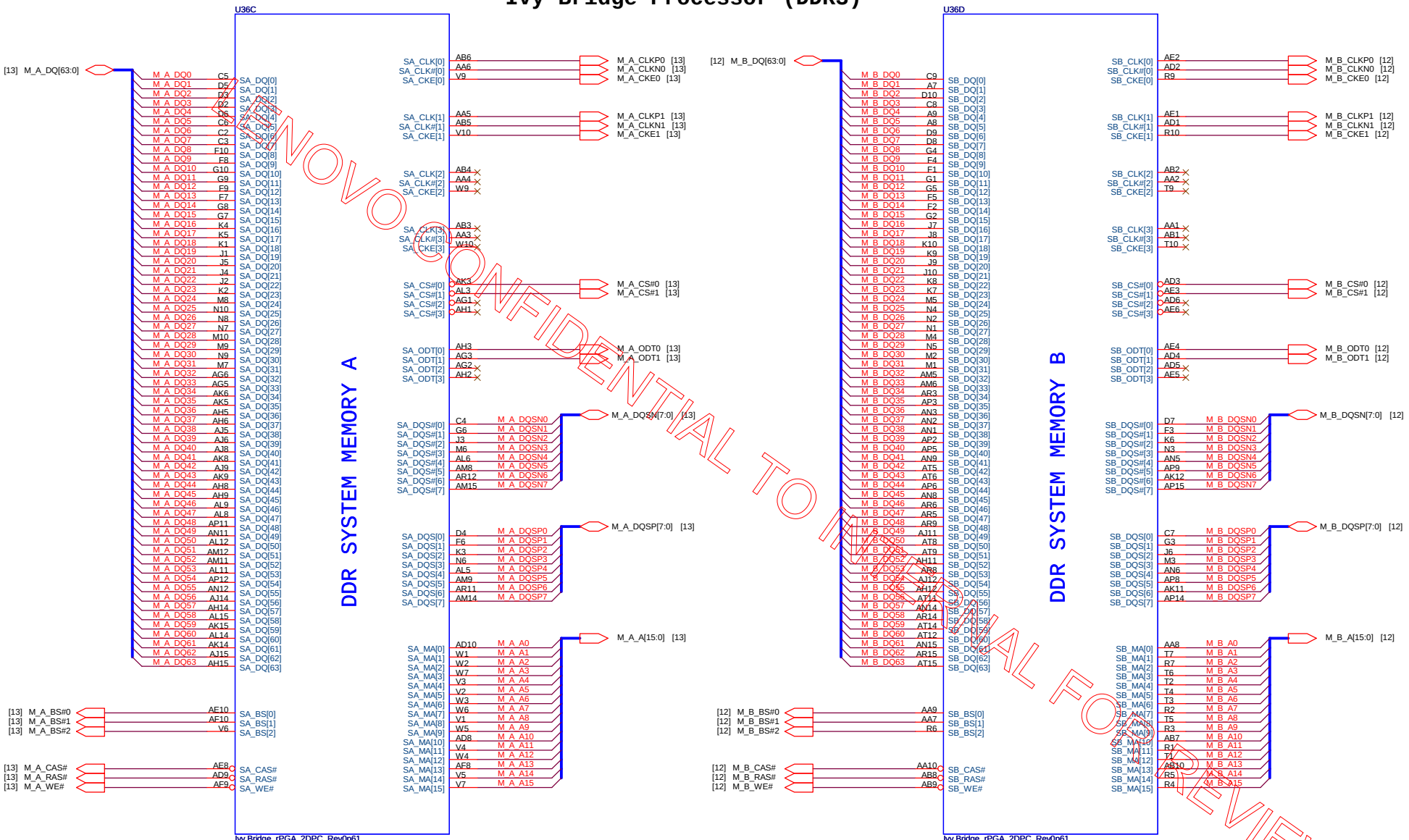
H_PROCHOT#	R164	62/F_4
XDP_TDO	R178	51_4
XDP_TMS	R480	51_4
XDP_TDI_R	R477	51_4
XDP_PREQ#	R172	*51_4
XDP_TCLK	R487	51_4
XDP_TRST#	R470	51_4

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	IVY Bridge 1/4	1A

Date: Wednesday, November 30, 2011 Sheet 2 of 45

Ivy Bridge Processor (DDR3)



PROJECT :	LZ2A
Quanta Computer Inc.	
Size	Document Number: IVY Bridge 2/4 — Rev: 1A
Date: Wednesday, November 30, 2011	Sheet 3 of 45

Ivy Bridge Processor (GRAPHIC POWER)

04

[33,41] +VCC_CORE
[2,6,7,8,10,33,34,38,43] +1.05V_PCH
[34] MAINON_15V
[2,10,12,13,33,34,37,43] +1.5V_SUS
[2,33] +1.5V_CPU
[10,27] +1.5V
[7,10,33,34,40] +1.8V
[33,34,39] +0.85V
[33,41] +VCC_GFX

POWER

U36F

CORE SUPPLY

+VCC_CORE

SNB: 55A
IVY: 55A

22uF_8 x8 Socket TOP cavity

C218 22U/6.3V_8 C219 22U/6.3V_8 C216 22U/6.3V_8 C220 22U/6.3V_8
C222 22U/6.3V_8 C221 22U/6.3V_8 C230 22U/6.3V_8 C217 22U/6.3V_8
C519 22U/6.3V_8 C198 22U/6.3V_8 C193 22U/6.3V_8 C175 22U/6.3V_8
C517 22U/6.3V_8 C516 22U/6.3V_8 C520 22U/6.3V_8 C518 22U/6.3V_8

10uF_8 x10 Socket BOT cavity

C583 10U/6.3V_8 C576 10U/6.3V_8 C591 10U/6.3V_8 C592 10U/6.3V_8
C582 10U/6.3V_8 C568 10U/6.3V_8 C574 10U/6.3V_8 C573 10U/6.3V_8
C575 10U/6.3V_8 C584 10U/6.3V_8

+VCC_CORE:
22uF_8 x8 TOP Socket cavity
22uF_8 x8 TOP Socket edge
10uF_8 x10 BOT Socket cavity

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

PEG AND DDR

+1.05V_PCH

SNB: 8.5A
IVY: 8.5A

C246 22U/6.3V_8 C251 22U/6.3V_8 C247 22U/6.3V_8 C245 22U/6.3V_8 C244 22U/6.3V_8 C243 22U/6.3V_8

C598 22U/6.3V_8 C597 22U/6.3V_8 C596 22U/6.3V_8 C248 22U/6.3V_8

22uF_8 x7 TOP Socket cavity
22uF_8 x5 BOT Socket cavity

C602 22U/6.3V_8 C601 22U/6.3V_8 C252 *22U/6.3V_8 C249 *22U/6.3V_8 C600 *22U/6.3V_8

22uF (Reserved)

C593 *22U/6.3V_8 C250 *22U/6.3V_8 C262 *22U/6.3V_8 C599 *22U/6.3V_8

J23 +1.05V_PCH_10 R526 *0_4_S +1.05V_PCH

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

SVID

VIDALERT# A J29 H_CPU_SVIDALRT#
VIDSCLK A J30 H_CPU_SVIDCLK
VIDSOUT A J28 H_CPU_SVIDDAT

SENSE LINES

VCC_SENSE A J35 R455 100_4 +VCC_CORE
VSS_SENSE A J34 R454 100_4
VCC_SENSE [41]
VSS_SENSE [41]

VCCIO_SENSE B10 VTT_SENSE
VSS_SENSE_VCCIO A10 VSSP_SENSE
VTT_SENSE [38]
VSSP_SENSE [38]

+1.05V_PCH
VTT_SENSE R550 10/F_4
VSSP_SENSE R556 10/F_4

Ivy Bridge_rPGA_2DPC_Rev0p61

POWER

U36G

GRAPHICS

SNB: 21.5A
IVY: 33A

+VCC_GFX

C580 22U/6.3V_8 C586 22U/6.3V_8 C590 22U/6.3V_8 C210 22U/6.3V_8
C226 22U/6.3V_8 C232 22U/6.3V_8 C236 22U/6.3V_8 C239 22U/6.3V_8
C237 22U/6.3V_8 C565 22U/6.3V_8 C241 22U/6.3V_8 C240 22U/6.3V_8

+VCC_GFX:
22uF_8 x2 TOP Socket cavity
22uF_8 x4 TOP Socket edge
22uF_8 x2 BOT Socket cavity
22uF_8 x4 BOT Socket edge

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

1.8V RAIL

+1.8V

C280 10U/6.3V_6 C603 1U/6.3V_4 C605 1U/6.3V_4 +C284 *330U/2.5V_7343

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

CPU VCCPL
SNB 45W:1.5A
330uF/7mohm x 1
10uF x 1
1uF x 2

Ivy Bridge_rPGA_2DPC_Rev0p61

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34
TP34 R423 100/F_4 +VCC_GFX
R425 100/F_4 TP36
VCC_AXG_SENSE [41]
VSS_AXG_SENSE [41]

VREF

SM_VREF AL1 +VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1
SMDDR_VREF_DQ0_M3 [13]
SMDDR_VREF_DQ1_M3 [12]
R561 *1K_4
R564 *1K_4

DDR3 -1.5V RAILS

SNB: 5A
IVY: 5A

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

+1.5V_CPU
C282 10U/6.3V_6 C287 10U/6.3V_6 C281 10U/6.3V_6 C283 10U/6.3V_6
330uF x1, 10uF_8 x6 Socket BOT edge.
C279 10U/6.3V_6 C286 10U/6.3V_6 +C285 220U/2.5V_7343

SA RAIL

SNB: 6A
IVY: 6A

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

+0.85V
C231 10U/6.3V_6 C572 10U/6.3V_6 C566 10U/6.3V_6
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE H23 R610 *0_4_S VCCSUSA_SENSE [39]
VCCSA_SEL0 [39]
VCCSA_VID[0] C22 R241 1K_4
VCCSA_VID[1] C24 R235 1K_4
VCCSA_SEL [39]
VCCIO_SEL A19 R521 *0_4 H_VTTVID1 [38]

Ivy Bridge_rPGA_2DPC_Rev0p61

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
+1.05V_PCH
Close to VR
R484 54.9/F_4
H_CPU_SVIDCLK R169 *0_4_S VR_SVID_CLK [41]

Place PU resistor close to CPU
+1.05V_PCH
R158 130/F_4

SVID DATA
+1.05V_PCH
Close to VR
R469 130/F_4
H_CPU_SVIDDAT R171 *0_4_S VR_SVID_DATA [41]

Place PU resistor close to CPU
+1.05V_PCH
R157 75_4

SVID ALERT
H_CPU_SVIDALRT# R156 *0_4_S VR_SVID_ALERT# [41]

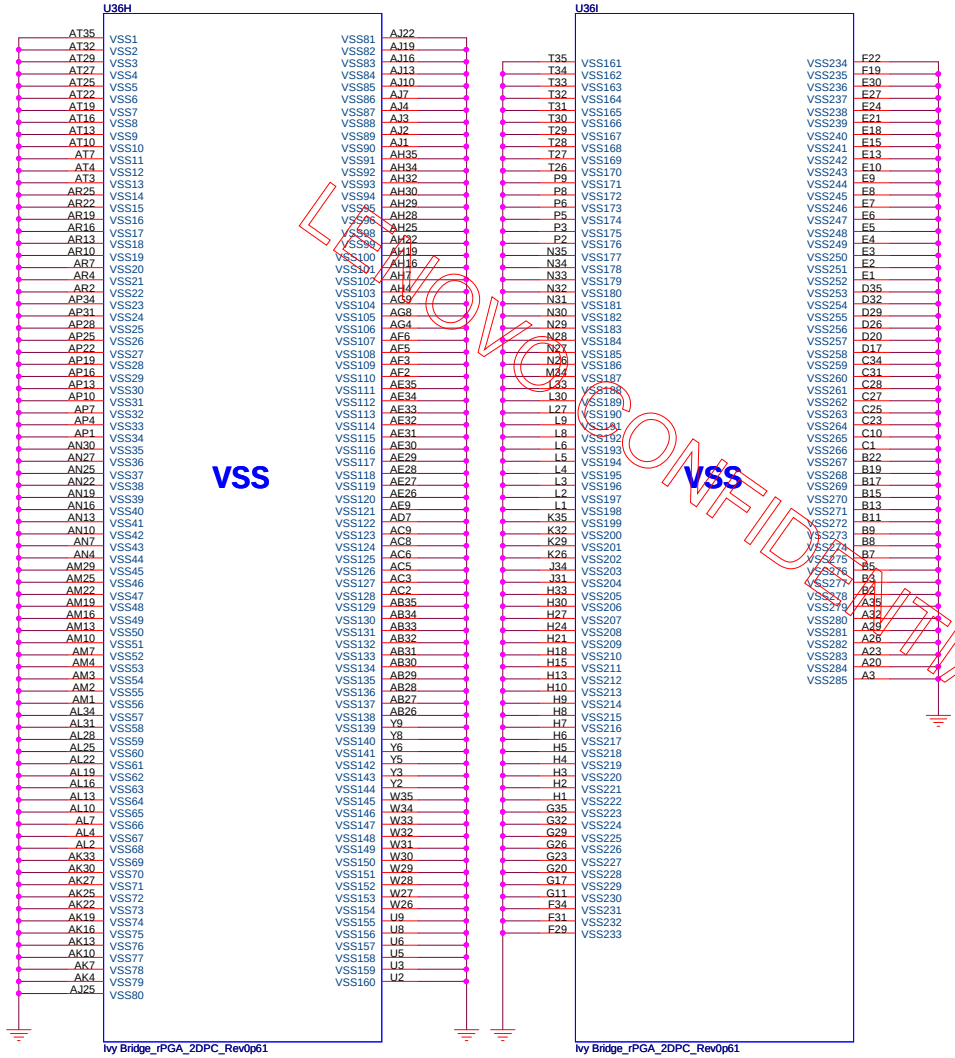
+VDDR_REF_CPU
[12,13,37] SMDDR_VREF R566 *0_8
Q51 ME2N7002E
[34] MAINON_15V R563 100K_4

+1.5V_CPU +1.5V
R276 *0_8_S
40mile routing

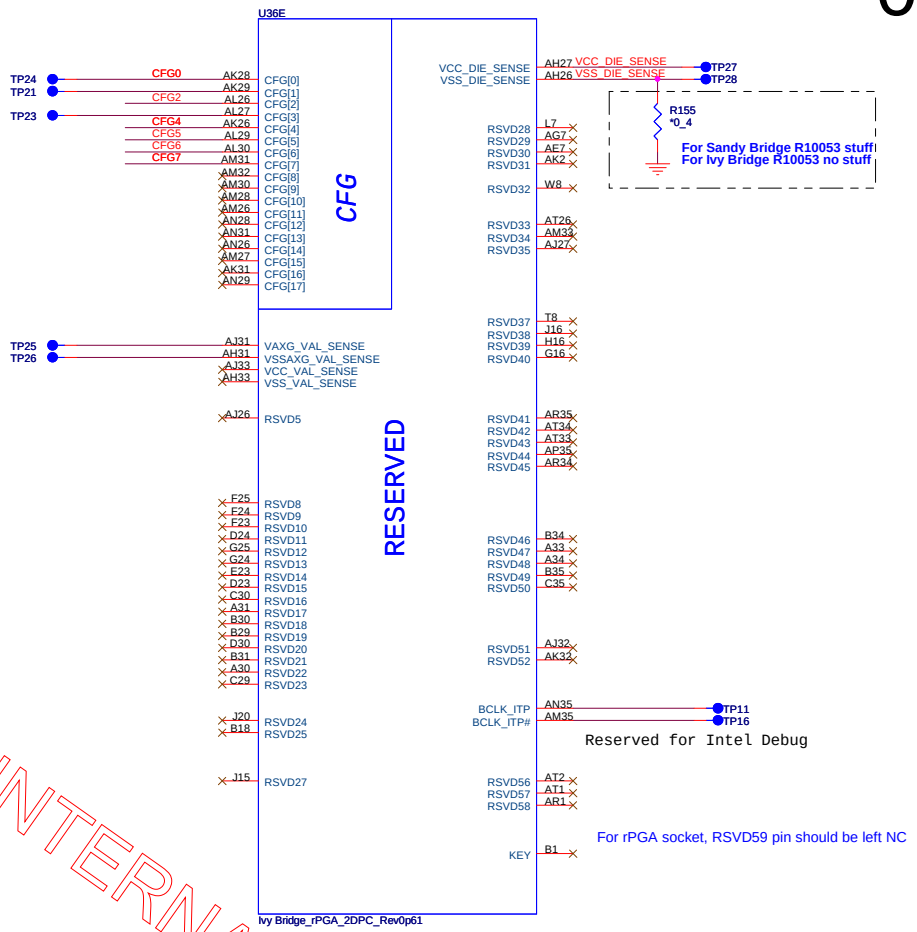
+1.5V_SUS 5A +1.5V_CPU +1.5V_SUS
Q35 AON7406
[34] MAINON_15V
C288 470P/50V/X7R_4
R277 220_8
[2,34] MAINON#
Q36 ME2N7002E
C293 0.1U/10V_4
C294 0.1U/10V_4
C291 0.1U/10V_4
C292 0.1U/10V_4
Placement close to CPU.

PROJECT : LZ2A
Quanta Computer Inc.
Size
Document Number IVY Bridge 3/4
Rev 1A
Date: Wednesday, November 30, 2011 Sheet 4 of 45

Ivy Bridge Processor (GND)



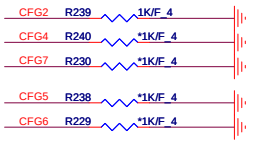
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	IVY Bridge 4/4	1A
Date: Wednesday, November 30, 2011	Sheet 5 of 45	

[2,4,7,8,10,33,34,38,43] +1.05V_PCH
[7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,7,8,9,10,27,31,34] +3V_S5
[7,10,32] +3V_RTC

Cougar Point/Panther Point (DMI,FDI,PM)

U13C

DMI0RXN BC24 ← [2] DMI_RXN0
DMI1RXN BE20 ← [2] DMI_RXN1
DMI2RXN BG18 ← [2] DMI_RXN2
DMI3RXN BG20 ← [2] DMI_RXN3
DMI0RXP BE24 ← [2] DMI_RXP0
DMI1RXP BC20 ← [2] DMI_RXP1
DMI2RXP BJ18 ← [2] DMI_RXP2
DMI3RXP BJ20 ← [2] DMI_RXP3
DMI0TXN AW24 → [2] DMI_TXN0
DMI1TXN AW20 → [2] DMI_TXN1
DMI2TXN BB18 → [2] DMI_TXN2
DMI3TXN AY18 → [2] DMI_TXN3
DMI0TXP AY24 → [2] DMI_TXP0
DMI1TXP AY20 → [2] DMI_TXP1
DMI2TXP AY18 → [2] DMI_TXP2
DMI3TXP AU18 → [2] DMI_TXP3
DMI_ZCOMP BJ24
DMI_IRCOMP BG25 ← DMI_COMP ← R543 49.9/F_4 ← +1.05V_PCH
DMI2RBIAS BH21 ← DMI_RBIAS ← R260 750/F_4

DMI

FDI_RXN0 BJ14 → FDI_TXN0 [2]
FDI_RXN1 AY14 → FDI_TXN1 [2]
FDI_RXN2 BE14 → FDI_TXN2 [2]
FDI_RXN3 BH13 → FDI_TXN3 [2]
FDI_RXN4 BC12 → FDI_TXN4 [2]
FDI_RXN5 BJ12 → FDI_TXN5 [2]
FDI_RXN6 BG10 → FDI_TXN6 [2]
FDI_RXN7 BG9 → FDI_TXN7 [2]
FDI_RXP0 BG14 → FDI_TXP0 [2]
FDI_RXP1 BB14 → FDI_TXP1 [2]
FDI_RXP2 BF14 → FDI_TXP2 [2]
FDI_RXP3 BG13 → FDI_TXP3 [2]
FDI_RXP4 BE12 → FDI_TXP4 [2]
FDI_RXP5 BG12 → FDI_TXP5 [2]
FDI_RXP6 BJ10 → FDI_TXP6 [2]
FDI_RXP7 BH9 → FDI_TXP7 [2]
FDI_INT AW16 → FDI_INT [2]
FDI_FSYNC0 AV12 → FDI_FSYNC0 [2]
FDI_FSYNC1 BC10 → FDI_FSYNC1 [2]
FDI_LSYNC0 AV14 → FDI_LSYNC0 [2]
FDI_LSYNC1 BB10 → FDI_LSYNC1 [2]

FDI

FOR DEEP S3
[32] SUSACK# → SUSACK# R620 0_4 → SUSWARN#_R R436 *0_4 → C12 SUSACK#
[2] XDP_DBRST# → XDP_DBRST# K3 SYS_RESET#
SYS_PWROK → C522 *1U/6.3V_4, R451 *0_4_S → SYS_PWROK_R P12 SYS_PWROK
[32] EC_PWROK → R426 *0_4, R460 *0_4_S → EC_PWROK_R L22 PWROK
EC_PWROK_R → R428 *0_4_S → APWROK_R L10 APWROK
[2] PM_DRAM_PWRGD → PM_DRAM_PWRGD B13 DRAMPWROK
[32] RSMRST# → RSMRST# C21 RSMRST#
FOR DEEP S3
[32] SUSWARN# → R410 0_4 → SUSWARN#_R K16 SUSWARN#/SUSPWRDNACK/GPIO30
[32] SIO_PWRBTN# → E20 PWRBTN#
[17,32] AC_PRESENT → R459 *0_4_S → AC_PRESENT_R H20 ACPRESENT / GPIO31
PM_BATLOW# E10 BATLOW# / GPIO72
PM_RI# A10 RI#

System Power Management

+3V_S5 +3V_S5 +3V_S5 +3V_S5 +3V_S5 DSW +3V_S5 +3V_S5

DSWVRMEN A18 ← DSWVREN
DPWROK E22 ← R615 *0_4 DPWROK, R124 0_4 RSMRST# ← RSMRST# [32]
WAKE# B9 ← PCIE_WAKE# ← PCIE_WAKE# [24,27,32]
CLKRUN# / GPIO32 N3 ↔ CLKRUN# [32]
SUS_STAT# / GPIO61 G8 → LPC_PD# → T18
SUSCLK / GPIO62 N14 → PCH_SUSCLK → T21
SLP_S5# / GPIO63 D10 → SLP_S5# → T17
SLP_S4# H4 → PM_SLP_S4# [32]
SLP_S3# F4 → SIO_SLP_S3# [32]
SLP_A# G10 → SLP_A# → T16
SLP_SUS# G16 → FOR DEEP S3 SLP_SUS# [10,32]
PMSYNCH AP14 → PM_SYNC [2]
SLP_LAN# / GPIO29 K14 → WLAN_AOAC_ON [27]

CPT_PPT_Rev_0p5

Cougar Point/Panther Point (LVDS,DDI)

U13D

[23] INT_LVDS_BLON → J47 L_BKLTEN
[23] INT_LVDS_VDDEN → M45 L_VDD_EN
[23] PCH_BRIGHT_PWM → P45 L_BKLTCTL
[23] INT_EDIDCLK → T40 L_DDC_CLK
[23] INT_EDIDDAT → K47 L_DDC_DATA
+3V → R496 2.2K_4, R489 2.2K_4 → T45 L_CTRL_CLK, P39 L_CTRL_DATA
R511 2.37K/F_4 → LVD_IBG → T22 → AF37 LVD_IBG, AF36 LVD_VBG
AE48 LVD_VREFH, AE47 LVD_VREFL

LVDS

[23] INT_TXLCLKOUTN → AK39 LVDSA_CLK#
[23] INT_TXLCLKOUTP → AK40 LVDSA_CLK
[23] INT_TXLOUTN0 → AN48 LVDSA_DATA#0
[23] INT_TXLOUTN1 → AM47 LVDSA_DATA#1
[23] INT_TXLOUTN2 → AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
[23] INT_TXLOUTP0 → AN47 LVDSA_DATA0
[23] INT_TXLOUTP1 → AM49 LVDSA_DATA1
[23] INT_TXLOUTP2 → AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3
AF40 LVDSB_CLK#
AF39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

R place close to PCH
R183 150/F_4 INT_CRT_BLU
R193 150/F_4 INT_CRT_GRE
R192 150/F_4 INT_CRT_RED

CRT

[22] INT_CRT_BLU → N48 CRT_BLUE
[22] INT_CRT_GRE → P49 CRT_GREEN
[22] INT_CRT_RED → T49 CRT_RED
[22] INT_DDCCLK → T39 CRT_DDC_CLK
[22] INT_DDCDAT → M40 CRT_DDC_DATA
[22] INT_CRT_HSYNC → R176 33_4 → INT_CRT_HSYNC_R → M47 CRT_HSYNC
[22] INT_CRT_VSYNC → R182 33_4 → INT_CRT_VSYNC_R → M49 CRT_VSYNC
DAC_IREF → T43 DAC_IREF
R506 1K/F_4 → T42 CRT_IRTN

Digital Display Interface

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 → INT_HDMI_SCL [21]
SDVO_CTRLDATA M39 → INT_HDMI_SDA [21]

INT. HDMI

DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 ← INT_HDMI_HPD_Q
DDPB_0N AV42 → INT_HDMI_TXDN2 [21]
DDPB_0P AV40 → INT_HDMI_TXDP2 [21]
DDPB_1N AV45 → INT_HDMI_TXDN1 [21]
DDPB_1P AV46 → INT_HDMI_TXDP1 [21]
DDPB_2N AU48 → INT_HDMI_TXDN0 [21]
DDPB_2P AU47 → INT_HDMI_TXDP0 [21]
DDPB_3N AV47 → INT_HDMI_TXCN [21]
DDPB_3P AV49 → INT_HDMI_TXCP [21]
DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38 ← DDPC_HPD_PU R548 10K_4 ← +3V
Follow PDG eDP disable guide
DDPC_0N AV47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49

INT. DP

DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41 ← DDPD_HPD_PU R547 10K_4 ← +3V
Follow PDG eDP disable guide
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

CPT_PPT_Rev_0p5

INT_HDMI_HPD_Q → R535 *0_4_S → INT_HDMI_HPD [21]
R523 *100K_4
R540 100K_4

DPWROK FOR DSW (DEEP S3)

FOR DEEP S3
+3V_DSW +3VPCU +3VPCU
+3V_S5 → D28 *RB500V-40 → R616 *10K_4 → DPWROK
+3VPCU → D29 *RB500V-40 → R617 *10K_4 → DPWROK
Q55 *LTC044EUBFS8TL
Q56 *2N7002
C665 *0.1U/10V/X5R_4 add cap to timing tune

System PWR_OK(CLG)

+3V_S5 → C171 0.1U/10V_4
U7 TC7SH08FU
[2] SYS_PWROK → SYS_PWROK → DELAY_VR_PWRGOOD [41]
EC_PWROK → R112 100K_4
R117 *0_4

+3V_RTC → R127 330K_4 → DSWVREN → R140 *330K_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PCH Pull-high/low(CLG)

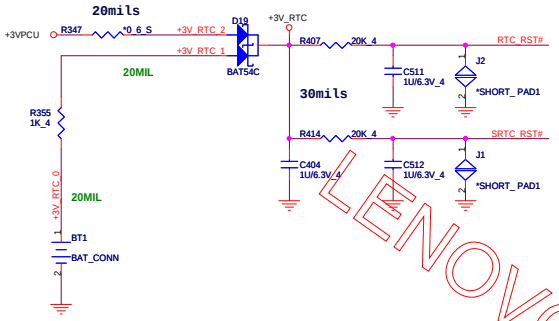
+3V +3V_S5
CLKRUN# R198 8.2K_4 → PM_RI# R142 10K_4
XDP_DBRST# R180 1K_4 → PM_BATLOW# R445 8.2K_4
R173 *1K_4 → PCIE_WAKE# R146 10K_4
RSMRST# R139 10K_4 → WLAN_AOAC_ON R418 10K_4 For AOAC
SYS_PWROK R457 100K_4 → SUSWARN# R409 10K_4
AC_PRESENT R442 10K_4
PM_DRAM_PWRGD R435 *200/F_4

PROJECT : LZ2A
Quanta Computer Inc.

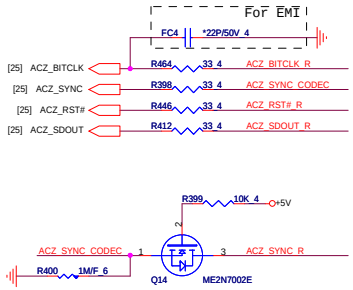
Size	Document Number	Rev
	Panther Point 1/6	1A

Date: Wednesday, November 30, 2011 Sheet 6 of 45

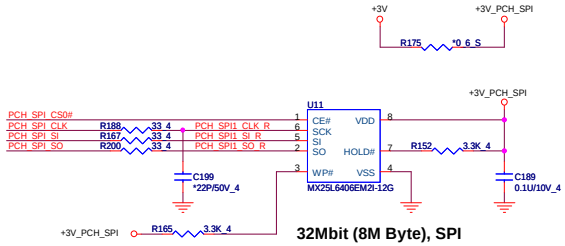
RTC Circuitry(RTC)



HDA Bus(CLG)

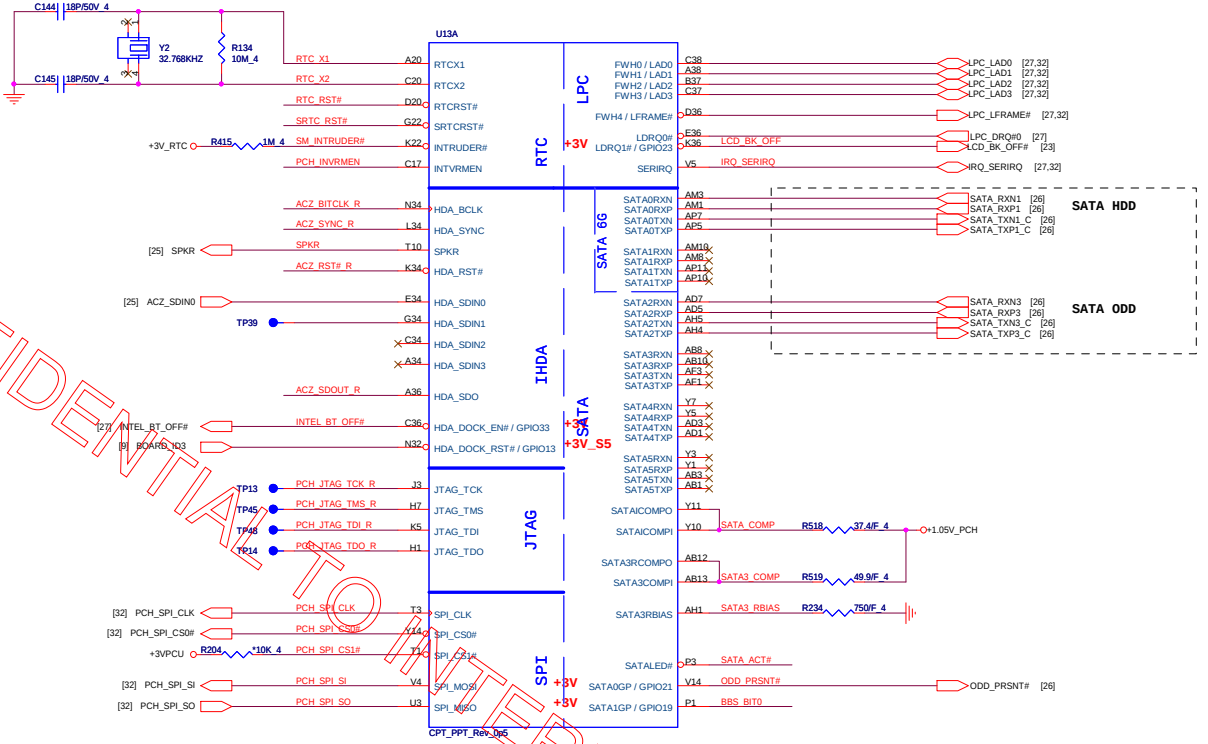


PCH Dual SPI (CLG)



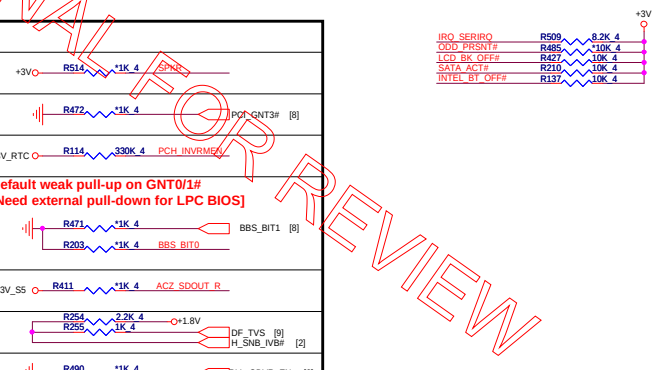
32Mbit (8M Byte), SPI

Cougar Point/Panther Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)

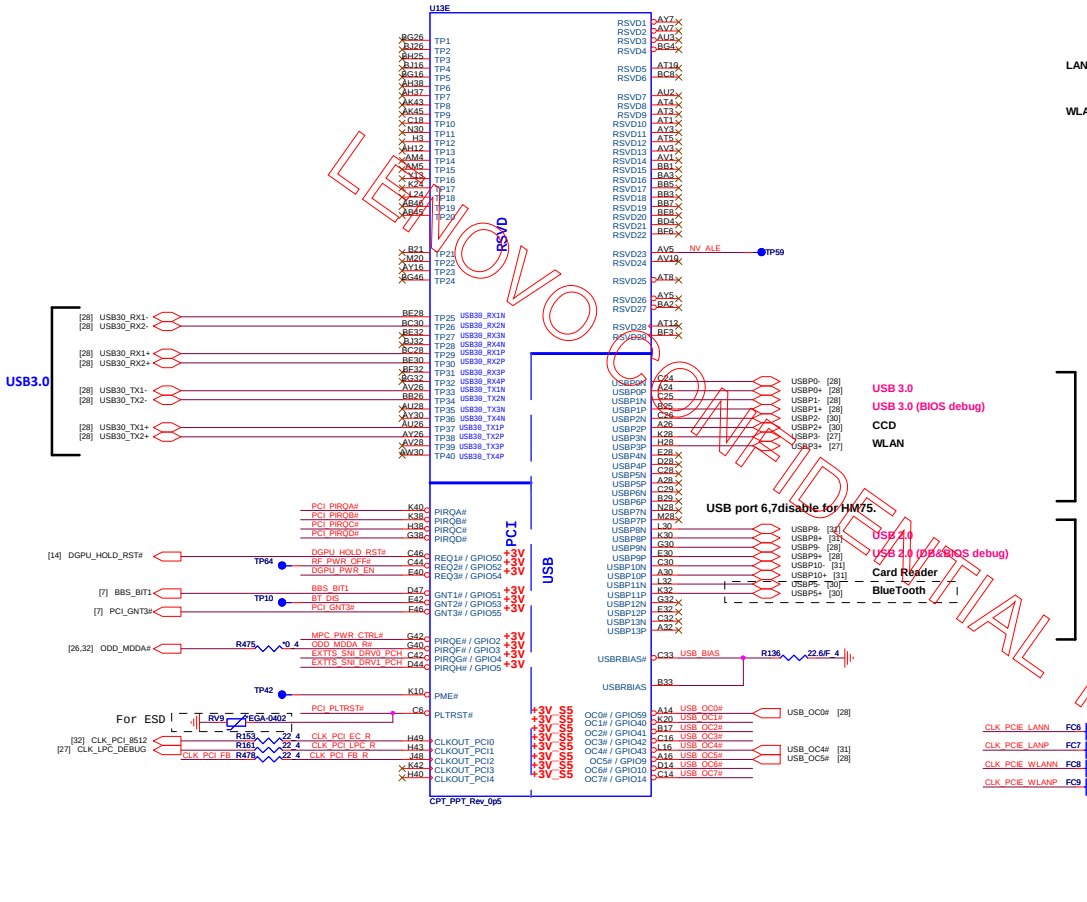


PROJECT : LZ2A
Quanta Computer Inc.

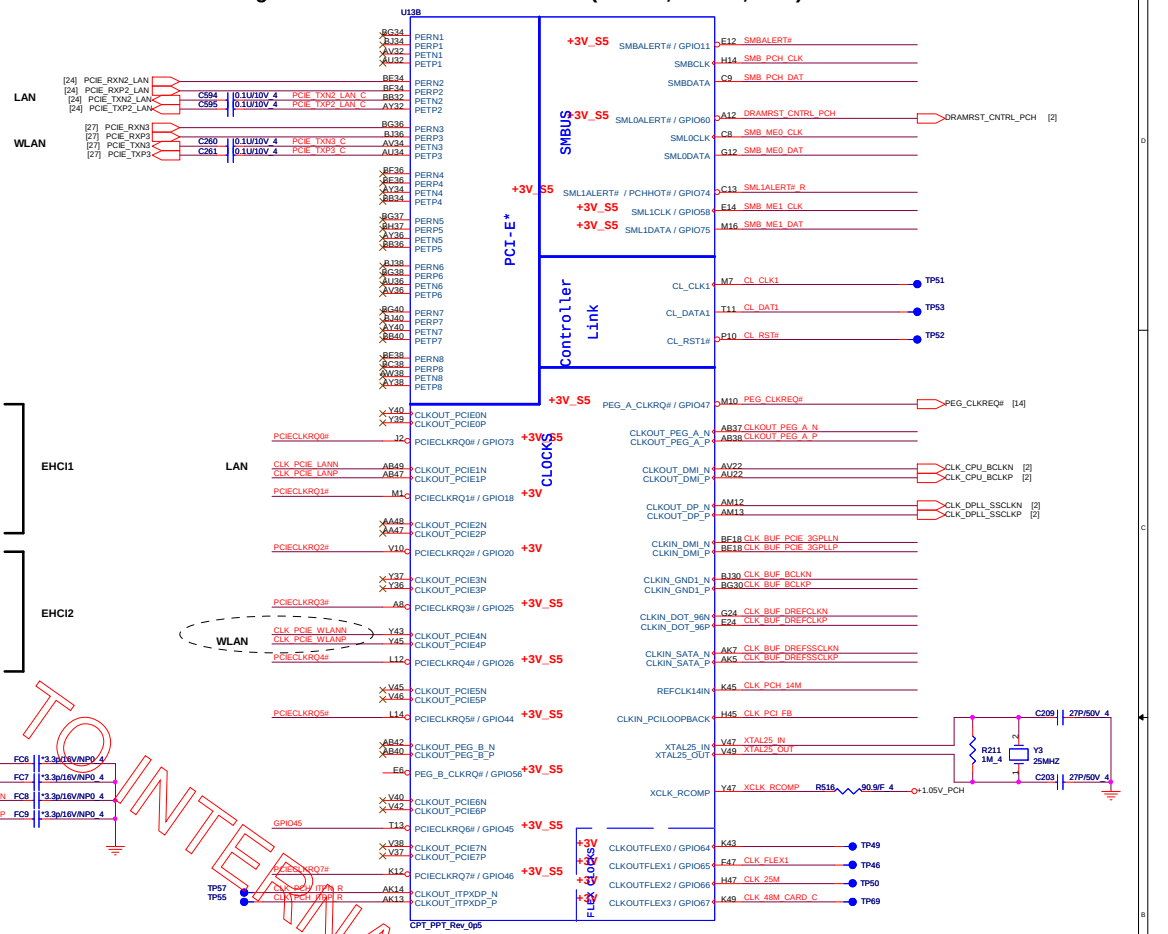
Size	Document Number	Rev
	Panther Point 2/6	1A

Date: Wednesday, November 30, 2011 Sheet 7 of 45

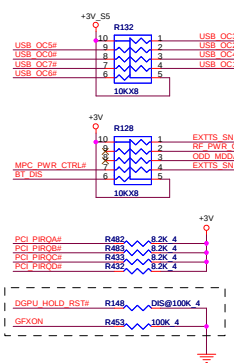
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



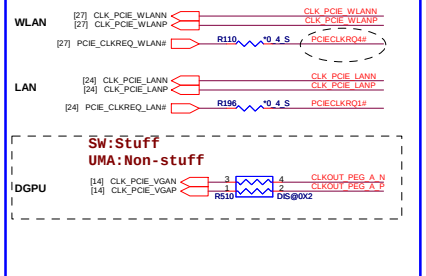
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



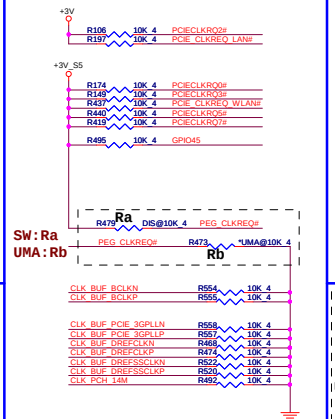
PCI/USBOC# Pull-up(CLG)



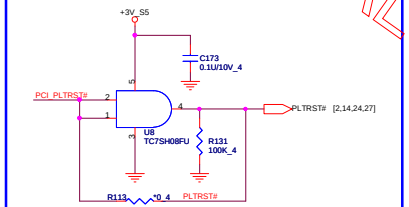
PCIE CLOCK



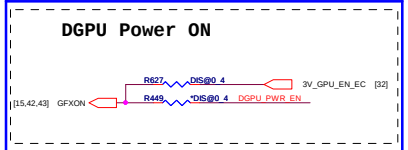
CLK_REQ/Strap Pin(CLG)



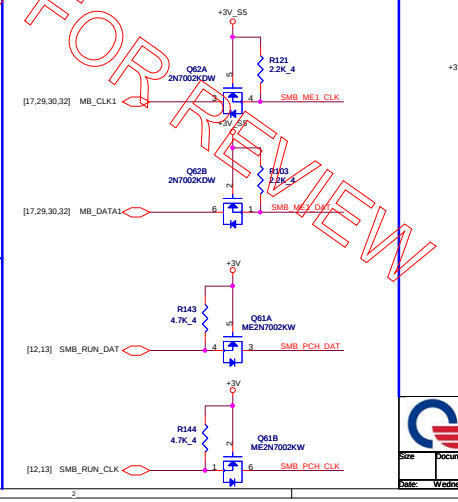
PLTRST#(CLG)



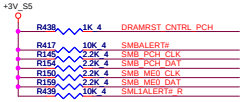
DGPU Power ON



SMBus(CLK)



SMBus/Pull-up(CLG)



MPC Switch Control

MPC_PWR_CTRL#	LOw = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R465 *1K_4

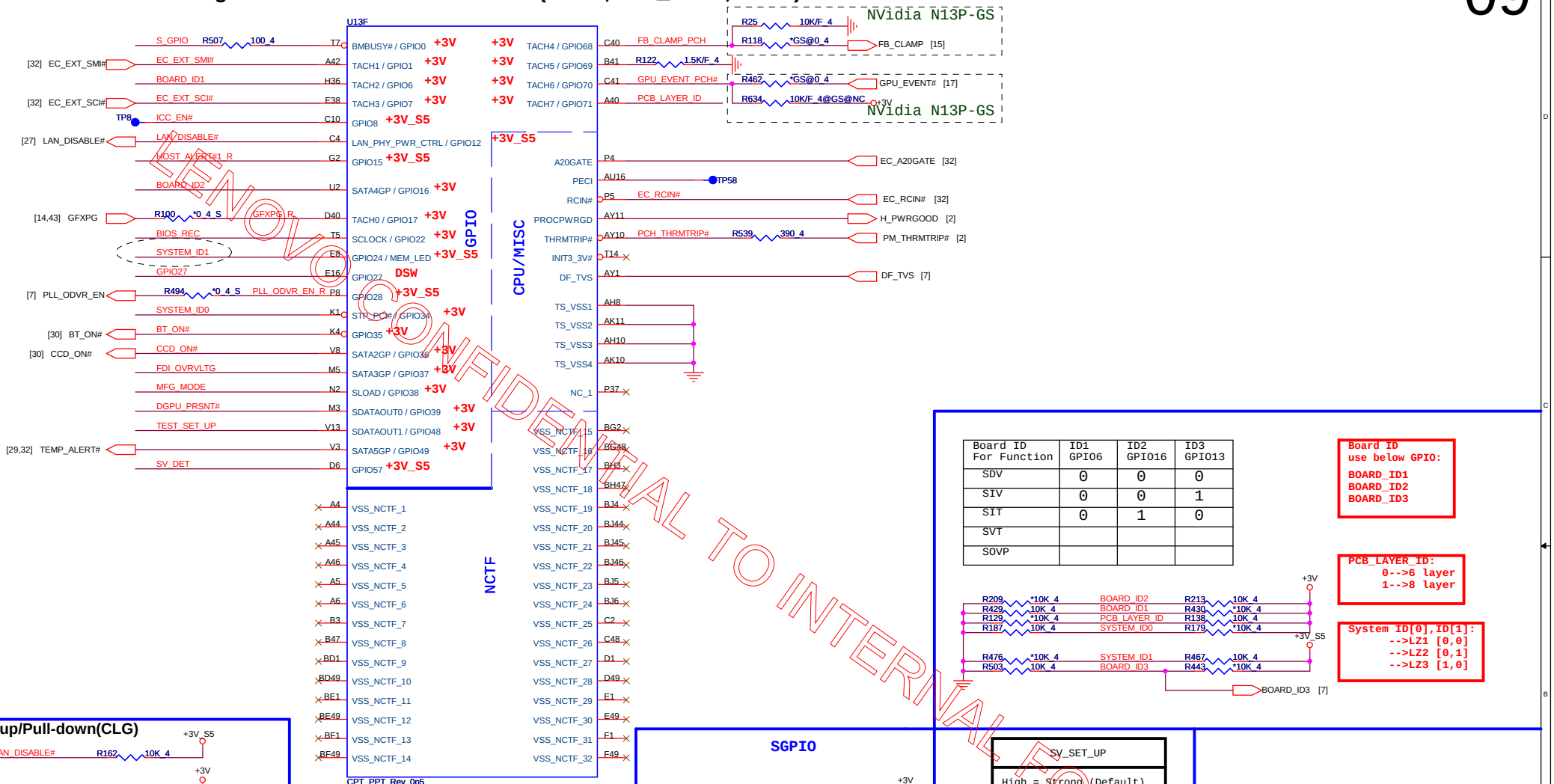
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Panther Point 3/6	1A
Date: Wednesday, November 30, 2011	Sheet 8 of 45	

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

09

[2,6,7,8,10,27,31,34] +3V_S5
[6,7,8,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V



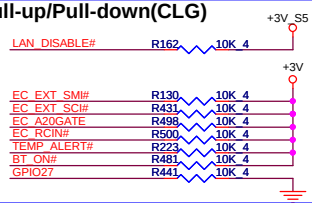
Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

Board ID use below GPIO:
BOARD_ID1
BOARD_ID2
BOARD_ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

System ID[0],ID[1]:
-->LZ1 [0,0]
-->LZ2 [0,1]
-->LZ3 [1,0]

GPIO Pull-up/Pull-down(CLG)

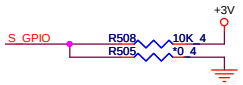


SATA2GP/GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

SGPIO

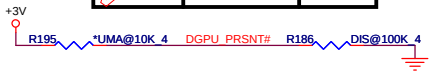


BIOS RECOVERY	High = Disable (Default) Low = Enable

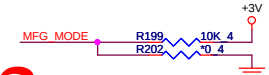
SV_SET_UP
High = Strong (Default)

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

	SWITCHABLE	UMA
Stuff	R186	R195
No Stuff	R195	R186



MFG-TEST

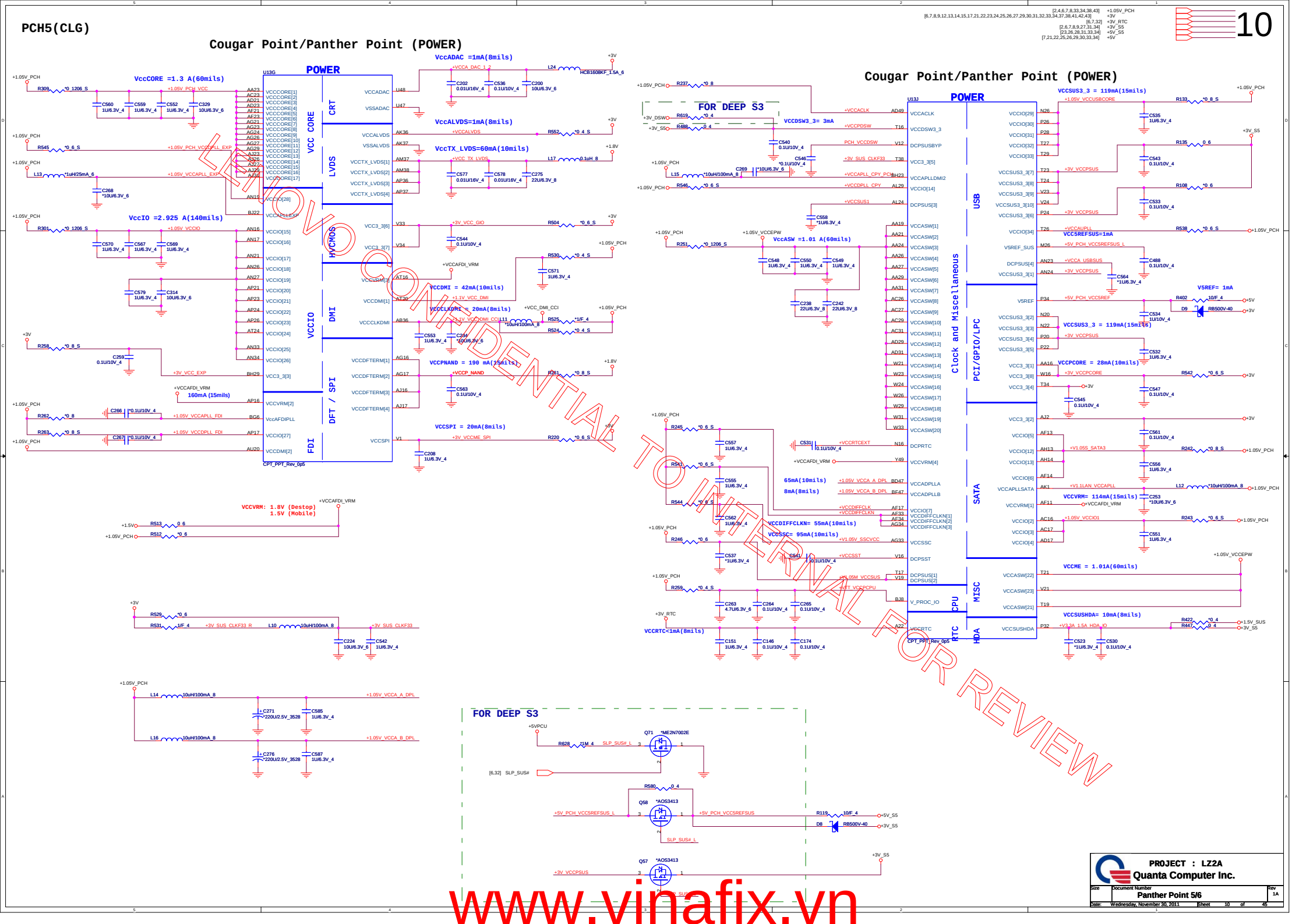


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Panther Point 4/6	1A

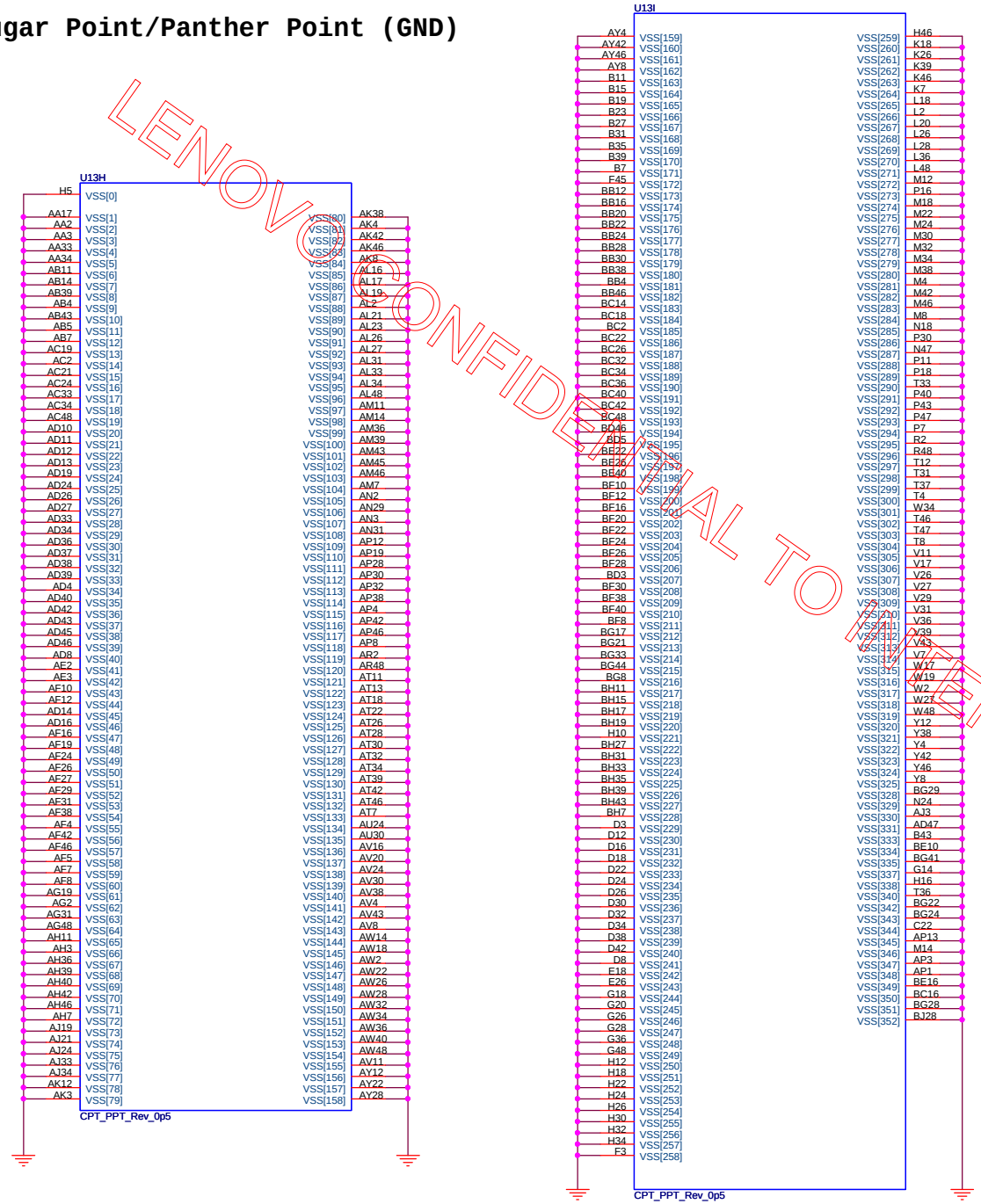
Date: Wednesday, November 30, 2011 Sheet 9 of 45

Cougar Point/Panther Point (POWER)



PROJECT : LZ2A
Quanta Computer Inc.
Size | Document Number: Panther Point 5/6 | Rev: 1A
Date: Wednesday, November 30, 2011 | Sheet 10 of 45

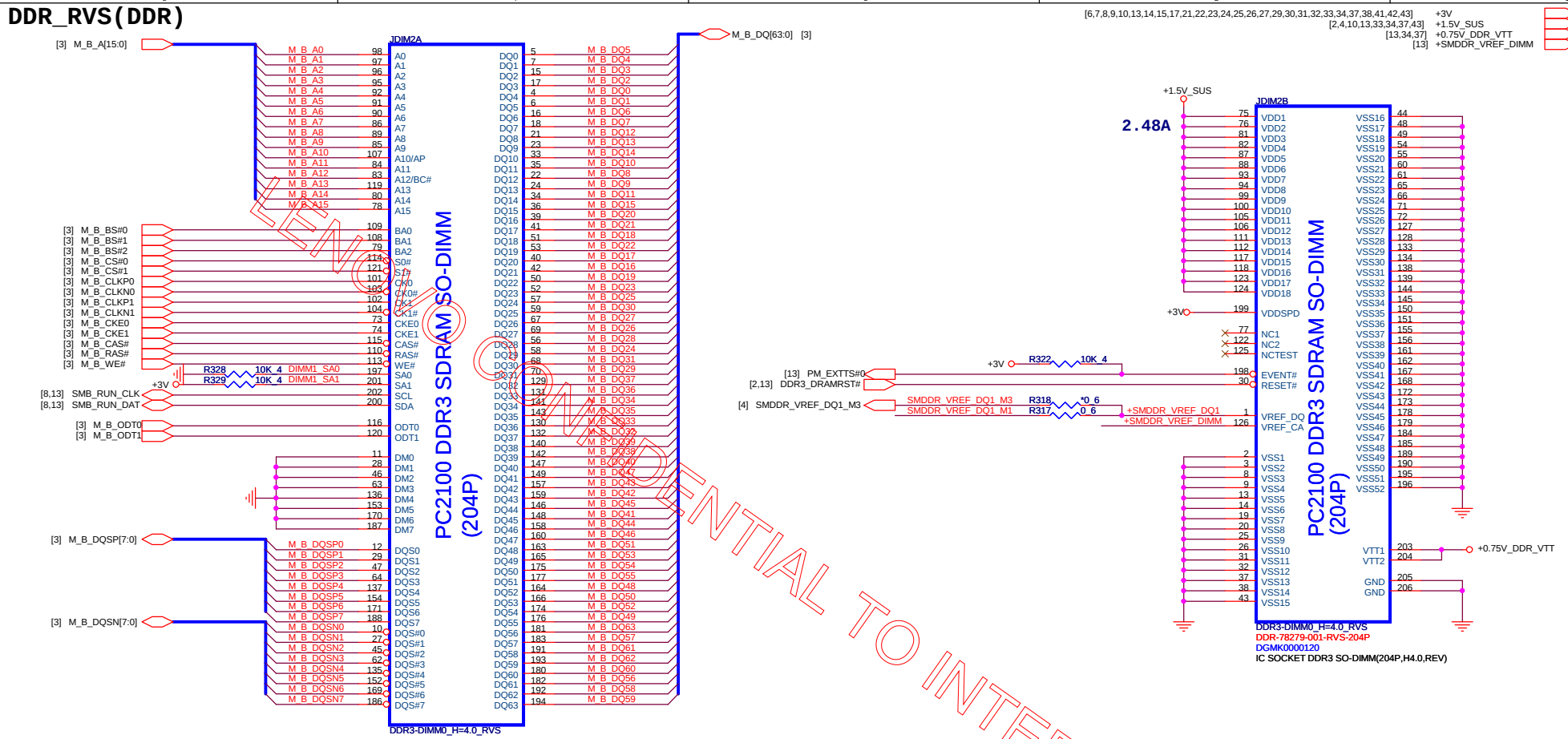
Cougar Point/Panther Point (GND)

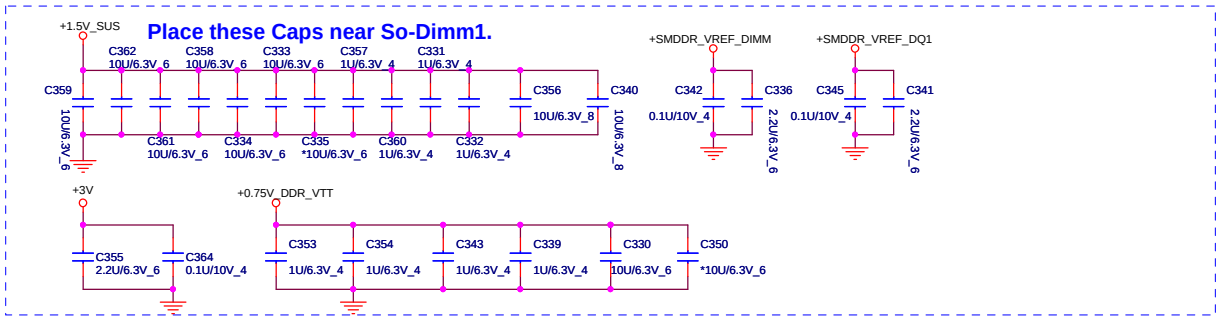


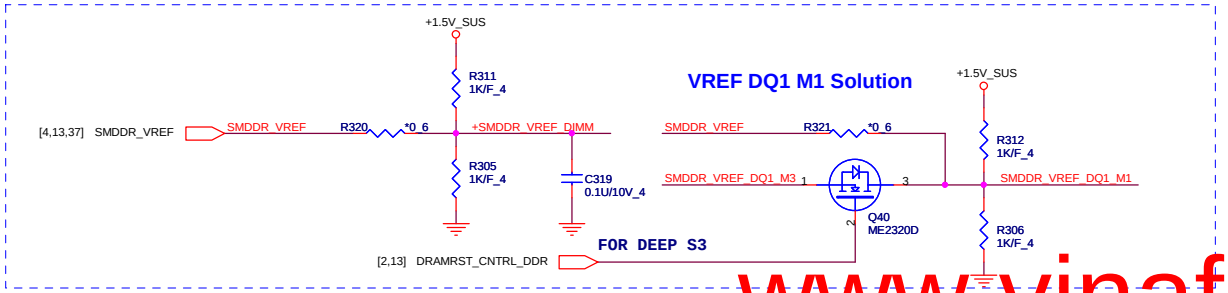
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Panther Point 6/6	1A
Date: Wednesday, November 30, 2011	Sheet 11 of 45	

DDR_RVS(DDR)





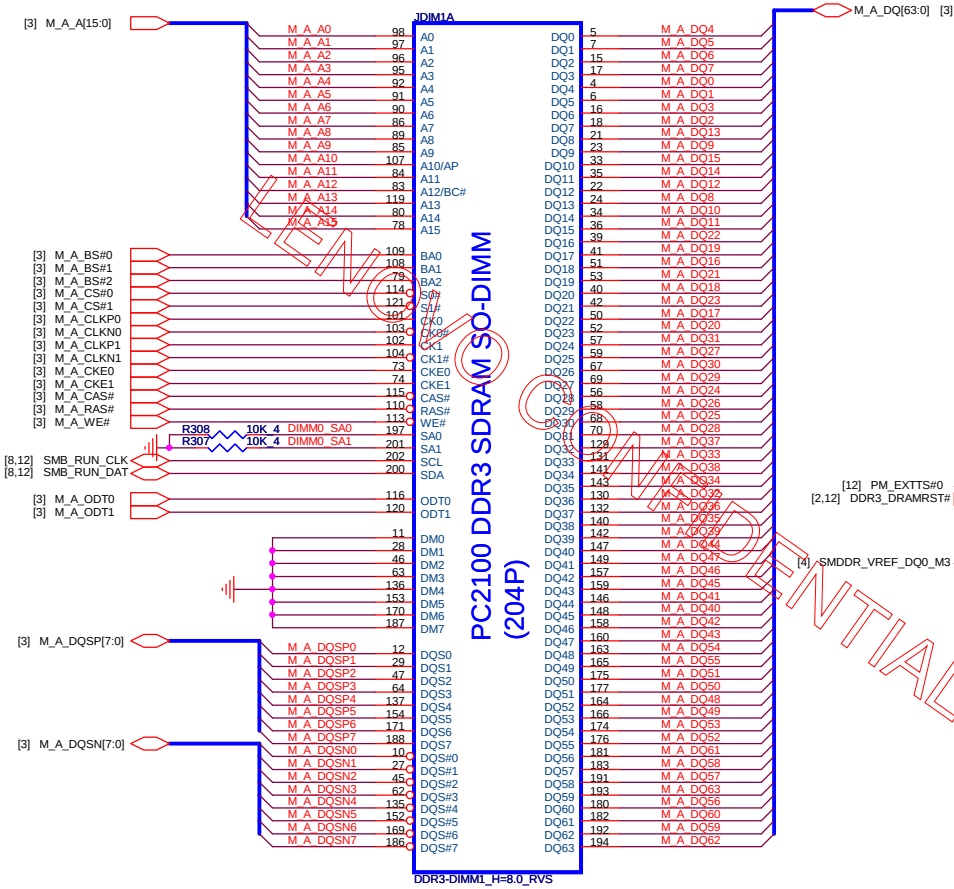


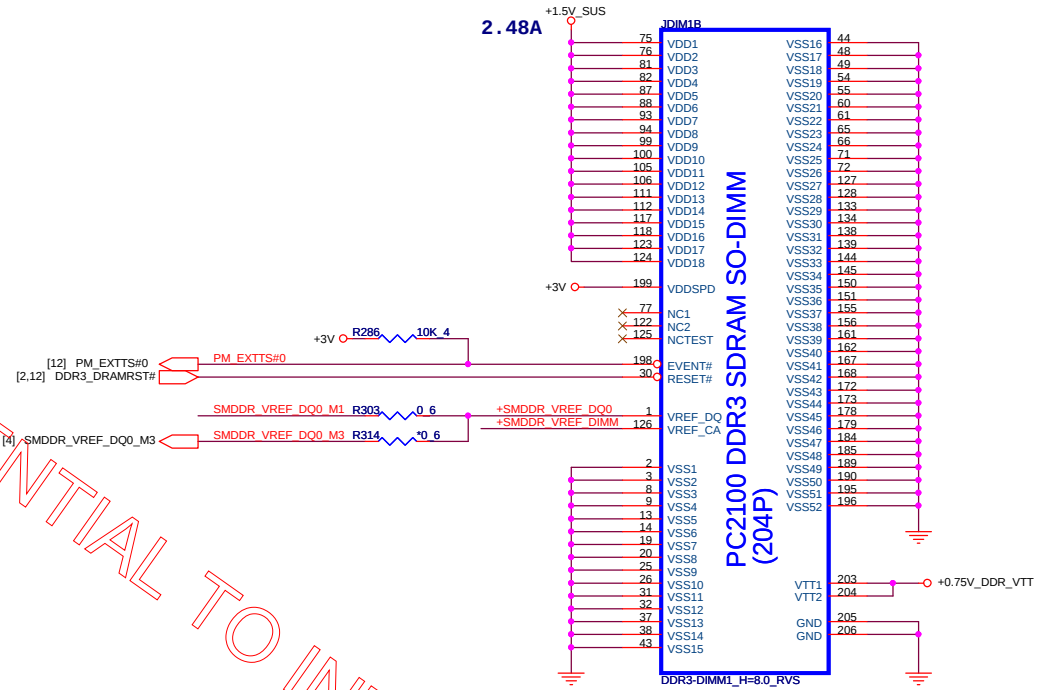
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A

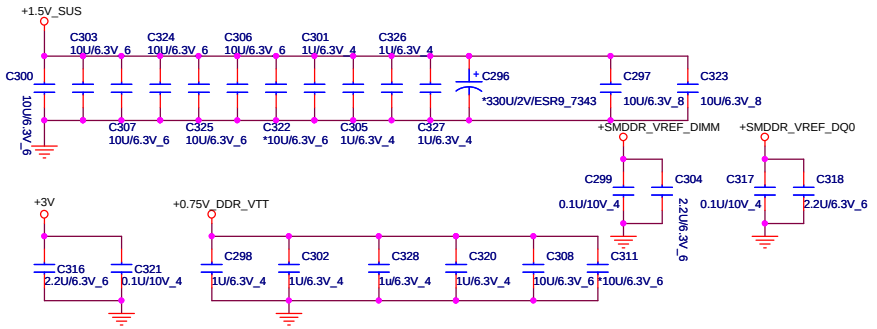
Date: Wednesday, November 30, 2011 Sheet 12 of 45

[6,7,8,9,10,12,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,4,10,12,33,34,37,43] +1.5V_SUS
[12,34,37] +0.75V_DDR_VTT
[12] +SMDDR_VREF_DIMM

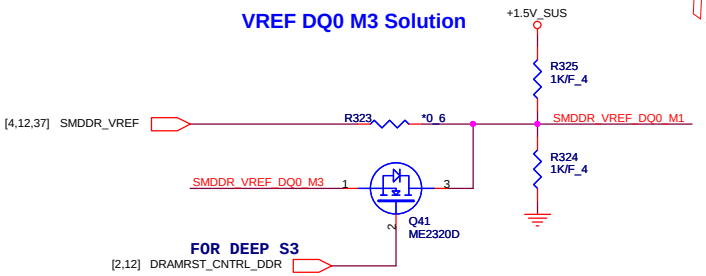




Place these Caps near So-Dimm0.



VREF DQ0 M3 Solution



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

Date: Wednesday, November 30, 2011 Sheet 13 of 45

[15,16,33,43] +1.05V_GFX_PCIE
[16,17,18,43] +3V_GPU
[15,19,20,33,43] +1.5V_GPU
[6,7,8,9,10,12,13,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[18,33,42] GFX_CORE

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >3.45A

U30A

N13P-GS

To be placed no further from the GPU than bewteen the PS and GPU

PLACE UNDER BGA

PLACE NEAR BALLS

+1.05V_GFX_PCIE

C94 C149 C108 C150 C105 C116 C117

DIS@22U/6.3V_8 DIS@22U/6.3V_8 DIS@10U/6.3V_8 DIS@10U/6.3V_8 DIS@4.7U/6.3V_6 DIS@1U/6.3V_4 DIS@1U/6.3V_4

AG19 AG21 AG22 AG24 AH21 AH25 PEX_IOVDD

C106 C130 C107 C138 C104 C120 C113

DIS@22U/6.3V_8 DIS@22U/6.3V_8 DIS@10U/6.3V_8 DIS@10U/6.3V_8 DIS@4.7U/6.3V_6 DIS@1U/6.3V_4 DIS@1U/6.3V_4

AG13 AG15 AG16 AG18 AG25 AH15 AH18 AH26 AH27 AJ27 AK27 AL27 AM28 AN28 PEX_IOVDDQ

CAP CLOSE TO BGA

12~16 mils width 210mA

+3V_GPU PLACE NEAR BGA

+PEX_SVDD_3V3 R86 *GS@0_4 AH12 PEX_PLL_HVDD

C467 DIS@0.1U/10V_4
C77 DIS@4.7U/6.3V_6
C118 DIS@4.7U/6.3V_6

AG12 PEX_SVDD_3V3

0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108) N13M-GE1 (GF119)	unstuff

[42] GPU_VCCSENSE L4 VDD_SENSE

[42] GPU_VSSSENSE L5 GND_SENSE

16 mils width for 110mA

P8 3V3AUX_NC

R90 *DIS@200/F_4 PEX_TSTCLK AJ26 PEX_TSTCLK_OUT
PEX_TSTCLK# AK26 PEX_TSTCLK_OUT*

150mA

+1.05V_GFX_PCIE L5 DIS@0_6 PLACE UNDER GPU

C127 DIS@1U/6.3V_4

C112 DIS@0.1U/10V_4

C129 DIS@1U/6.3V_4
C136 DIS@4.7U/6.3V_6

PLACE NEAR BGA

+PEX_PLLVDD AG26 PEX_PLLVDD

TESTMODE AK11 TESTMODE

R94 DIS@10K_4

PEX_TERMP AP29 PEX_TERMP

R98 DIS@2.49K/F_4

bga908-nvidia-n13p-gs-a1

1/19 PCI_EXPRESS

PEG Capacitance	
N13P-GS (GK107)	CH4222K9B04: CAP CHIP 0.22U 10V(+-10%,X5R,0402)
N13P-GL (GF108) N13M-GE1 (GF119)	CH41002KB93: CAP CHIP 0.1U 10V(+-10%,X5R,0402)

GPU RST#(CLG)

+3V C510 DIS@0.1U/10V_4

[2,8,24,27] PLTRST#

[8] DGPU_HOLD_RST#

U9 DIS@TC7SH08FU

GPU_RST#

PEX_WAKE AJ11

PEX_RST AJ12 GPU_RST#

PEX_CLKREQ AK12 R405 DIS@10K_4 +3V_GPU

PEX_CLKREQ#

PEX_REFCLK AL13 CLK_PCIE_VGAP [8]
PEX_REFCLK AK13 CLK_PCIE_VGAN [8]

PEX_TX0	AK14	PEG_RXP15_C	C143	DIS@0.1U/10V_4	PEG_RXP15 [2]
PEX_TX0	AJ14	PEG_RXN15_C	C141	DIS@0.1U/10V_4	PEG_RXN15 [2]
PEX_RX0	AN12				PEG_TXP15 [2]
PEX_RX0	AM12				PEG_TXN15 [2]
PEX_TX1	AH14	PEG_RXP14_C	C195	DIS@0.1U/10V_4	PEG_RXP14 [2]
PEX_TX1	AG14	PEG_RXN14_C	C196	DIS@0.1U/10V_4	PEG_RXN14 [2]
PEX_RX1	AN14				PEG_TXP14 [2]
PEX_RX1	AM14				PEG_TXN14 [2]
PEX_TX2	AK15	PEG_RXP13_C	C166	DIS@0.1U/10V_4	PEG_RXP13 [2]
PEX_TX2	AJ15	PEG_RXN13_C	C167	DIS@0.1U/10V_4	PEG_RXN13 [2]
PEX_RX2	AP14				PEG_TXP13 [2]
PEX_RX2	AP15				PEG_TXN13 [2]
PEX_TX3	AL16	PEG_RXP12_C	C186	DIS@0.1U/10V_4	PEG_RXP12 [2]
PEX_TX3	AK16	PEG_RXN12_C	C187	DIS@0.1U/10V_4	PEG_RXN12 [2]
PEX_RX3	AN15				PEG_TXP12 [2]
PEX_RX3	AM15				PEG_TXN12 [2]
PEX_TX4	AK17	PEG_RXP11_C	C152	DIS@0.1U/10V_4	PEG_RXP11 [2]
PEX_TX4	AJ17	PEG_RXN11_C	C153	DIS@0.1U/10V_4	PEG_RXN11 [2]
PEX_RX4	AN17				PEG_TXP11 [2]
PEX_RX4	AM17				PEG_TXN11 [2]
PEX_TX5	AH17	PEG_RXP10_C	C164	DIS@0.1U/10V_4	PEG_RXP10 [2]
PEX_TX5	AG17	PEG_RXN10_C	C165	DIS@0.1U/10V_4	PEG_RXN10 [2]
PEX_RX5	AP17				PEG_TXP10 [2]
PEX_RX5	AP18				PEG_TXN10 [2]
PEX_TX6	AK18	PEG_RXP9_C	C184	DIS@0.1U/10V_4	PEG_RXP9 [2]
PEX_TX6	AJ18	PEG_RXN9_C	C185	DIS@0.1U/10V_4	PEG_RXN9 [2]
PEX_RX6	AN18				PEG_TXP9 [2]
PEX_RX6	AM18				PEG_TXN9 [2]
PEX_TX7	AL19	PEG_RXP8_C	C163	DIS@0.1U/10V_4	PEG_RXP8 [2]
PEX_TX7	AK19	PEG_RXN8_C	C162	DIS@0.1U/10V_4	PEG_RXN8 [2]
PEX_RX7	AN20				PEG_TXP8 [2]
PEX_RX7	AM20				PEG_TXN8 [2]
PEX_TX8	AK20	PEG_RXP7_C	C183	DIS@0.1U/10V_4	PEG_RXP7 [2]
PEX_TX8	AJ20	PEG_RXN7_C	C182	DIS@0.1U/10V_4	PEG_RXN7 [2]
PEX_RX8	AP20				PEG_TXP7 [2]
PEX_RX8	AP21				PEG_TXN7 [2]
PEX_TX9	AH20	PEG_RXP6_C	C161	DIS@0.1U/10V_4	PEG_RXP6 [2]
PEX_TX9	AG20	PEG_RXN6_C	C160	DIS@0.1U/10V_4	PEG_RXN6 [2]
PEX_RX9	AN21				PEG_TXP6 [2]
PEX_RX9	AM21				PEG_TXN6 [2]
PEX_TX10	AK21	PEG_RXP5_C	C180	DIS@0.1U/10V_4	PEG_RXP5 [2]
PEX_TX10	AJ21	PEG_RXN5_C	C181	DIS@0.1U/10V_4	PEG_RXN5 [2]
PEX_RX10	AN23				PEG_TXP5 [2]
PEX_RX10	AM23				PEG_TXN5 [2]
PEX_TX11	AL22	PEG_RXP4_C	C158	DIS@0.1U/10V_4	PEG_RXP4 [2]
PEX_TX11	AK22	PEG_RXN4_C	C159	DIS@0.1U/10V_4	PEG_RXN4 [2]
PEX_RX11	AP23				PEG_TXP4 [2]
PEX_RX11	AP24				PEG_TXN4 [2]
PEX_TX12	AK23	PEG_RXP3_C	C157	DIS@0.1U/10V_4	PEG_RXP3 [2]
PEX_TX12	AJ23	PEG_RXN3_C	C156	DIS@0.1U/10V_4	PEG_RXN3 [2]
PEX_RX12	AN24				PEG_TXP3 [2]
PEX_RX12	AM24				PEG_TXN3 [2]
PEX_TX13	AH23	PEG_RXP2_C	C179	DIS@0.1U/10V_4	PEG_RXP2 [2]
PEX_TX13	AG23	PEG_RXN2_C	C178	DIS@0.1U/10V_4	PEG_RXN2 [2]
PEX_RX13	AN26				PEG_TXP2 [2]
PEX_RX13	AM26				PEG_TXN2 [2]
PEX_TX14	AK24	PEG_RXP1_C	C155	DIS@0.1U/10V_4	PEG_RXP1 [2]
PEX_TX14	AJ24	PEG_RXN1_C	C154	DIS@0.1U/10V_4	PEG_RXN1 [2]
PEX_RX14	AP26				PEG_TXP1 [2]
PEX_RX14	AP27				PEG_TXN1 [2]
PEX_TX15	AL25	PEG_RXP0_C	C176	DIS@0.1U/10V_4	PEG_RXP0 [2]
PEX_TX15	AK25	PEG_RXN0_C	C177	DIS@0.1U/10V_4	PEG_RXN0 [2]
PEX_RX15	AN27				PEG_TXP0 [2]
PEX_RX15	AM27				PEG_TXN0 [2]

All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD > 0
- tFBVDDQ > 0
- tPEX_VDD > 0
- tIFPx_IOVDD ≥ 0
- tIFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.

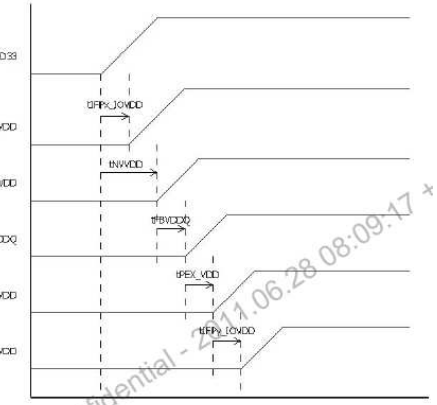


Figure 17. Recommended Power On Sequencing Order

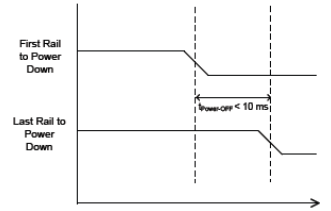


Figure 18. Recommended Power Off Sequencing Order

For power-down sequency

+3V_GPU +1.5V_GPU +3V_GPU GFX_CORE +3V_GPU +1.05V_GFX_PCIE

D1 DIS@RB500V-40 D2 DIS@RB500V-40 D25 DIS@RB500V-40

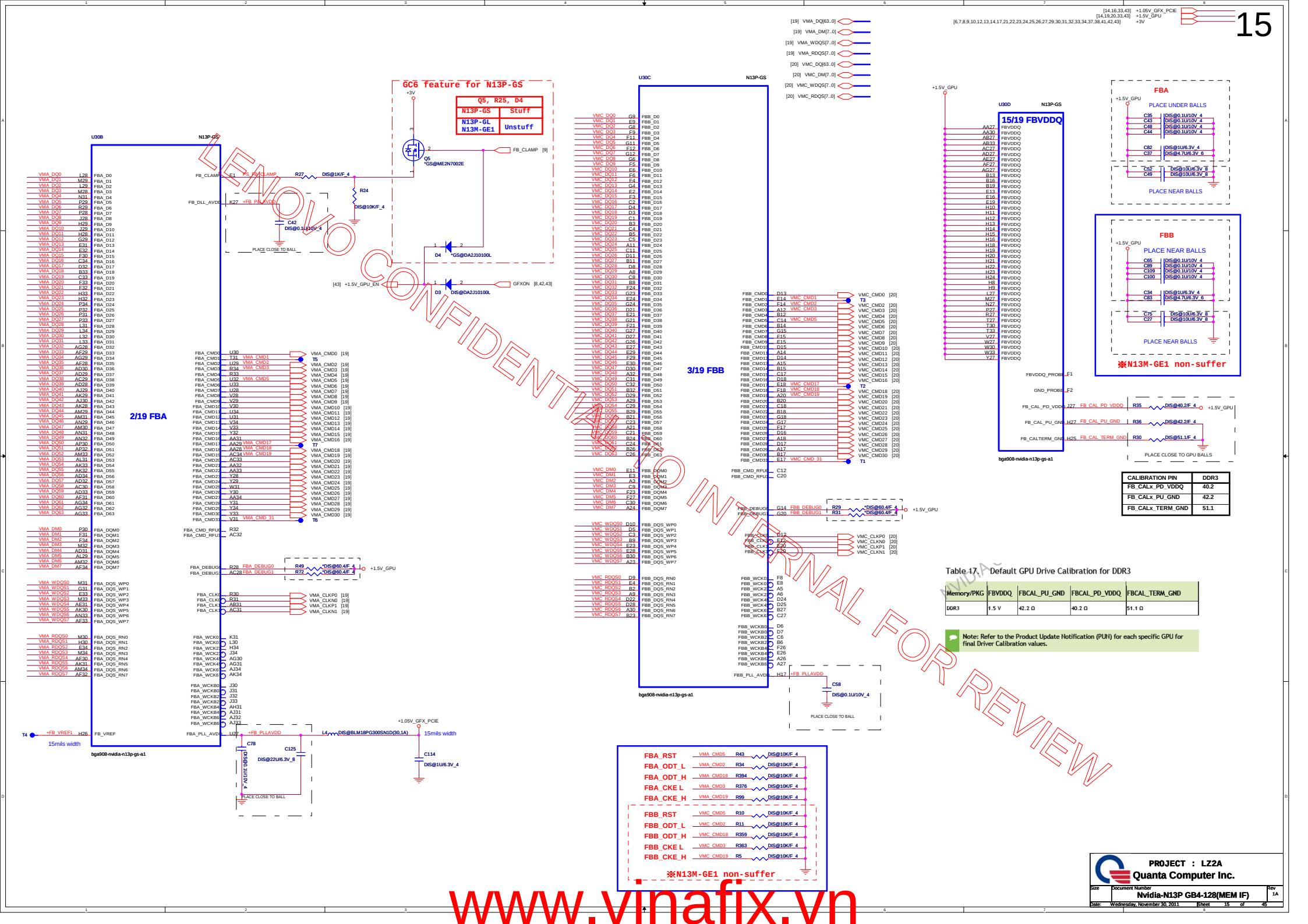
PEG CLK detect

GFXPG [9,43]

[8] PEG_CLKREQ# PEX_CLKREQ#

Q15 DIS@ME2N7002E

PROJECT : LZ2A
Quanta Computer Inc.
Size Document Number Nvidia-N13P GB4-128(PCIe) Rev 1A
Date: Wednesday, November 30, 2011 Sheet 14 of 45



[14,15,33,43] +1.05V_GFX_PCIE

50 mA

160 mA+160 mA

200 mA

U30J N13P-GS

6/19 IFPAB

ALL PINS NC FOR GF117

IFPAB_RSET AJ8

+IFPAB_PLLVDD AH8 IFPAB_PLLVDD

R91 DIS@10K/F_4

+IFPAB_IOVDD AG8 IFPA_IOVDD AG9 IFPB_IOVDD

R83 DIS@10K/F_4

IFPA_TXC AN6 IFPA_TXC AM6

IFPA_TXD0 AN3 IFPA_TXD0 AP3

IFPA_TXD1 AM5 IFPA_TXD1 AN5

IFPA_TXD2 AK6 IFPA_TXD2 AL6

IFPA_TXD3 AH6 IFPA_TXD3 AJ6

IFPB_TXC AH9 IFPB_TXC AJ9

IFPB_TXD0 AP5 IFPB_TXD0 AP6

IFPB_TXD1 AL7 IFPB_TXD1 AM7

IFPB_TXD2 AM8 IFPB_TXD2 AN8

IFPB_TXD3 AL8 IFPB_TXD3 AK8

IFPAB

GPIO14 N4

bga908-nvidia-n13p-gs-a1

U30K N13P-GS

7/19 IFPC

ALL PINS NC FOR GF117

IFPC_RSET AF8

+IFPCD_PLLVDD AF7 IFPC_PLLVDD

R79 DIS@10K/F_4

+IFPCD_IOVDD AF6 IFPC_IOVDD

R84 DIS@10K/F_4

DVI/HDMI DP

I2CW_SDA I2CW_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

IFPC_AUX AG2 IFPC_AUX AG3

IFPC_L3 AG4 IFPC_L3 AG5

IFPC_L2 AH4 IFPC_L2 AH3

IFPC_L1 AJ2 IFPC_L1 AJ3

IFPC_L0 AJ1 IFPC_L0 AK1

IFPC

GPIO15 P2

bga908-nvidia-n13p-gs-a1

U30L N13P-GS

8/19 IFPD

ALL PINS NC FOR GF117

IFPD_RSET AN2

+IFPCD_PLLVDD AG7 IFPD_PLLVDD

+IFPCD_IOVDD AG6 IFPD_IOVDD

DVI/HDMI DP

I2CX_SDA I2CX_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

IFPD_AUX AK2 IFPD_AUX AK3

IFPD_L3 AK5 IFPD_L3 AK4

IFPD_L2 AL4 IFPD_L2 AL3

IFPD_L1 AM4 IFPD_L1 AM3

IFPD_L0 AM2 IFPD_L0 AM1

IFPD

GPIO17 M6

bga908-nvidia-n13p-gs-a1

U30M N13P-GS

9/19 IFPEF

ALL PINS NC FOR GF117

R60 DIS@10K_4 +IFPEF_PLLVDD AB8 IFPEF_PLLVDD

AD6 IFPEF_RSET

R61 DIS@10K_4 +IFPEF_IOVDD AC8 IFPF_IOVDD AC7 IFPE_IOVDD

DVI-DL DVI-SL/HDMI DP

I2CY_SDA I2CY_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

HPD_E

IFPE_AUX AB4 IFPE_AUX AB3

IFPE_L3 AC5 IFPE_L3 AC4

IFPE_L2 AC3 IFPE_L2 AC2

IFPE_L1 AC1 IFPE_L1 AD1

IFPE_L0 AD3 IFPE_L0 AD2

GPIO18 R1

IFPE

I2CZ_SDA I2CZ_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

HPD_F

IFPF_AUX AF2 IFPF_AUX AF3

IFPF_L3 AF1 IFPF_L3 AG1

IFPF_L2 AD5 IFPF_L2 AD4

IFPF_L1 AF5 IFPF_L1 AF4

IFPF_L0 AE4 IFPF_L0 AE3

GPIO19 P3

IFPF

bga908-nvidia-n13p-gs-a1

U30N N13P-GS

R78 DIS@10K_4

TP29

TP31

GF108/GKx GF117

DACA_VDD AG10

DACA_VREF AP9

DACA_RSET AP8

NC

TSEN_VREF

GF117 GF108/GKx

NC NC I2CA_SCL R4 EV_CRTDCLK R630 DIS@2.2K_4 +3V_GPU

NC I2CA_SDA R5 EV_CRTDDAT R631 DIS@2.2K_4

NC DACA_HSYNC AM9 TP6

DACA_VSYNC AN9 TP30

NC DACA_RED AK9 TP4

NC DACA_GREEN AL10 TP3

NC DACA_BLUE AL9 TP5

4/19 DACA

bga908-nvidia-n13p-gs-a1

60mA 12~16 mil

90mA 12~16 mil

+1.05V_GFX_PCIE

L2 DIS@BLM18PG300SN1D(30,1A)

PLACE CLOSE TO BGA

C122 DIS@22U/6.3V_8

C96 DIS@0.1U/10V_4

PLACE UNDER BGA

+PLLVDD

+1.05V_GFX_PCIE

L3 DIS@HCB1608KF(180,1.5A)_6

+NV_PLLVDD

C126 DIS@1U/6.3V_4

C111 DIS@22U/6.3V_8

C101 DIS@4.7U/6.3V_6

C98 DIS@0.1U/10V_4

C97 DIS@0.1U/10V_4

C99 DIS@0.1U/10V_4

U30Q N13P-GS

12/19 XTAL_PLL

AD8 PLLVDD

AE8 SP_PLLVDD

AD7 VID_PLLVDD

NC

GF108/GKx GF117

XTALSSIN H1

XTALIN H3

XTALOUTBUFF J4

XTALOUT H2

XTAL_SSIN R33 DIS@10K_4

BXTALOUT R38 DIS@10K_4

XTALI_27M Y1 XTALO_27M

C39 DIS@27P/50V_4

DIS@27MHZ

C41 DIS@33P/50V/NPO_4

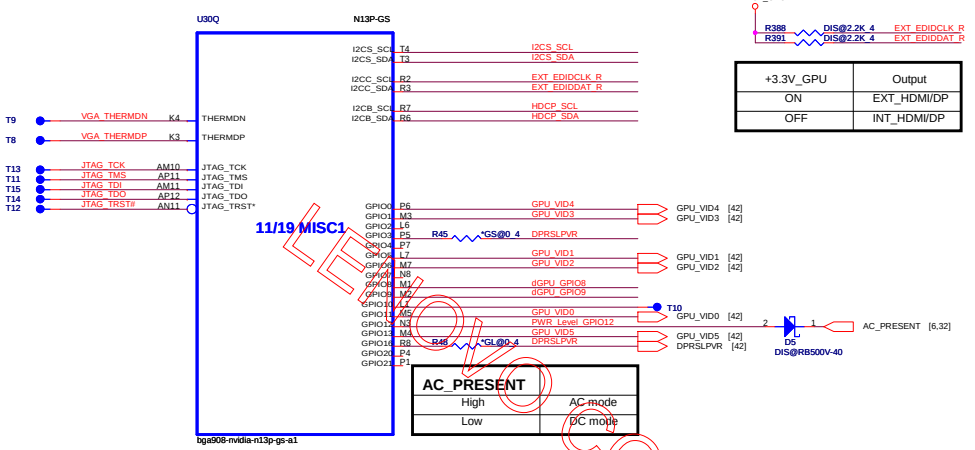
bga908-nvidia-n13p-gs-a1

PROJECT : LZ2A

Quanta Computer Inc.

Size | Document Number: Nvidia-N13P GB4-128(Display) | Rev: 1A

Date: Wednesday, November 30, 2011 Sheet 16 of 45



AC_PRESENT	
High	AC mode
Low	DC mode

+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24992FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS31002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS31502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS32002FB29	RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4	CS32492FB16	RES CHIP 24.9K 1/16W +-1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +-1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +-1% (0402)

VRAM Configuration Table

※ROM_SI Strap Bit for RAM Mapping

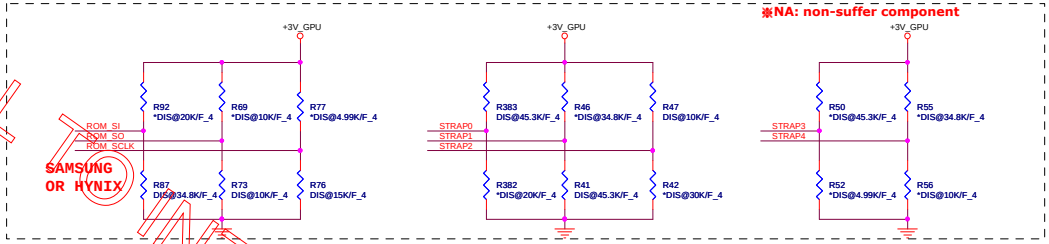
VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGGT500		K4W1G1646G-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C	0x2(0010)	R87 (15K ohm)

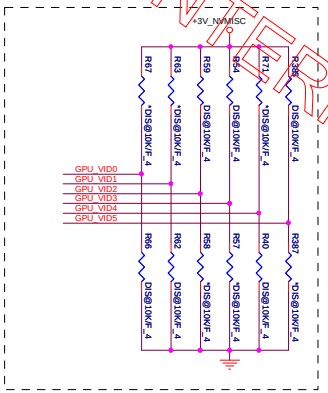
Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU Model Strap Table

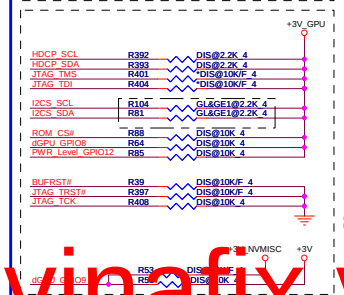
GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD

※NA: non-suffer component

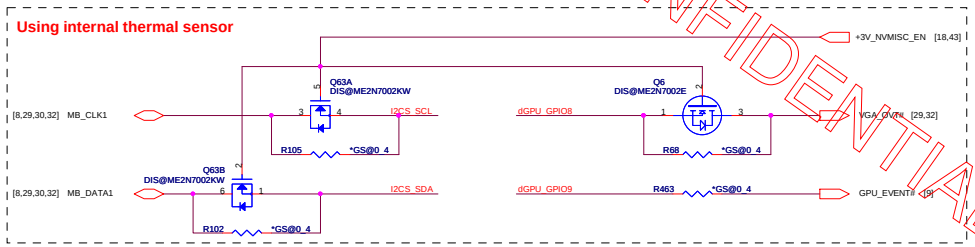




NVVDD Table	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
	NVVDD (0.9V)	NVVDD (0.95V)	NVVDD (0.9V)
GPU_VID0	0 (R66)	0 (R66)	0 (R66)
GPU_VID1	0 (R62)	0 (R62)	0 (R62)
GPU_VID2	0 (R58)	1 (R59)	0 (R58)
GPU_VID3	0 (R57)	1 (R54)	0 (R57)
GPU_VID4	1 (R71)	0 (R40)	1 (R71)
GPU_VID5	1 (R385)	1 (R385)	1 (R385)



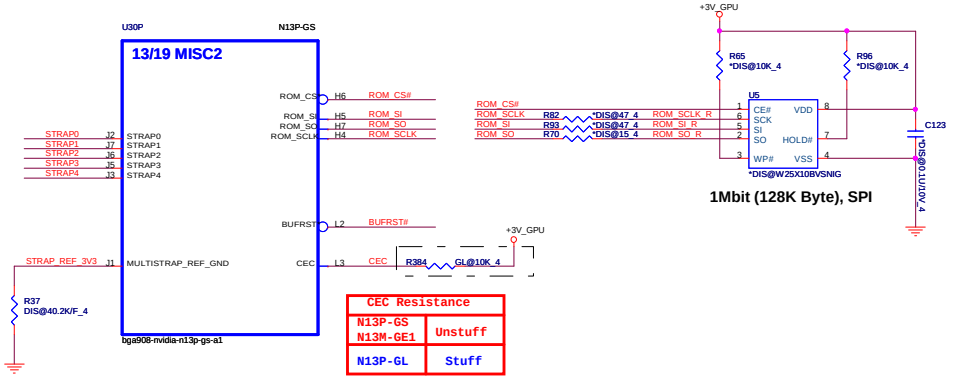
Using internal thermal sensor



	Q6,Q63, R81,R104	R68,R102, R105,R463
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor



CEC Resistance	
N13P-GS N13M-GE1	Unstuff
N13P-GL	Stuff

Table 2. GB4-128 Ballout Compatibility

Ball Number	N13P-PES/-GL/-NS1 Signal Names	N13M-GE1 Signal Names	N13P-GV / N13M-GS Signal Names	N13P-GT/-GS/-LP and N14P-Q1/-Q3 Signal Names	Comment
L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PES/-GL/-NS1.

GPIO ASSIGNMENTS

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: Nvidia-N13P GB4-128(GPIO/STRAP) Rev 1A
Date: Wednesday, November 30, 2011 Sheet 17 of 45

[14,16,17,43] +3V_GPU
[17] +3V_NVMISC
[14,33,42] GFX_CORE

U30E N13P-GS

14/19 NVVDD

GFX_CORE

VDD AA12, AA14, AA16, AA19, AA21, AA23, AB13, AB15, AB17, AB18, AB20, AB22, AC12, AC14, AC16, AC19, AC21, AC23, M12, M14, M16, M19, M21, M23, N13, N15, N17, N18, N20, N22, P12, P14, P16, P19, P21, P23, R13, R15, R17, R18, R20, R22, T12, T14, T16, T19, T21, T23, U13, U15, U17, U18, U20, U22, V13, V15, V17, V18, V20, V22, W12, W14, W16, W19, W21, W23, Y13, Y15, Y17, Y18, Y20, Y22

bga908-nvidia-n13p-gs-a1

GFX_CORE

PLACE UNDER BALLS

C85 DIS@0.1U/10V_4
C54 DIS@0.1U/10V_4
C46 DIS@0.1U/10V_4
C47 DIS@0.1U/10V_4
C59 DIS@4.7U/6.3V_6
C68 DIS@4.7U/6.3V_6
C79 DIS@4.7U/6.3V_6
C72 DIS@4.7U/6.3V_6
C80 DIS@4.7U/6.3V_6
C71 DIS@4.7U/6.3V_6
C63 DIS@4.7U/6.3V_6
C67 DIS@4.7U/6.3V_6
C50 DIS@4.7U/6.3V_6
C88 DIS@4.7U/6.3V_6

GFX_CORE

PLACE NEAR BALLS

C93 DIS@22U/6.3V_8
C66 DIS@47U/6.3V_8
C61 DIS@4.7U/6.3V_6
C73 DIS@4.7U/6.3V_6
C74 DIS@4.7U/6.3V_6
C90 DIS@4.7U/6.3V_6
C87 DIS@4.7U/6.3V_6
C76 *DIS@330U/2V/ESR9_7343

U30G N13P-GS

16/19 GND_1/2

GND A2, AA17, AA18, AA20, AA22, AB12, AB14, AB16, AB19, AB2, AB21, A33, AB23, AB28, AB30, AB32, AB5, AB7, AC13, AC15, AC17, AC18, AA13, AC20, AC22, AE2, AE28, AE30, AE32, AE33, AE5, AE7, AH10, AA15, AH13, AH16, AH19, AH2, AH22, AH24, AH28, AH29, AH30, AH32, AH33, AH5, AH7, AJ7, AK10, AK7, AL12, AL14, AL15, AL17, AL18, AL2, AL20, AL21, AL23, AL24, AL26, AL28, AL30, AL32, AL33, AL5, AM13, AM16, AM19, AM22, AM25, AN1, AN10, AN13, AN16, AN19, AN22, AN25, AN30, AN34, AN4, AN7, AP2, AP33, B1, B10, B22, B25, B28, B31, B34, B4, B7, C10, C13, C19, C22, C25, C28, C7, D2, D31, D33, E10, E22, E25, E5, E7, F28, F7, G10, G13, G16, G19, G2, G22, G25, G28, G3, G30, G32, G33, G5, G7, K2, K28, K30, K32, K33, K5, K7, M13, M15, M17, M18, M20, M22, N12, N14, N16

bga908-nvidia-n13p-gs-a1

U30I N13P-GS

17/19 GND_2/2

GND N19, N2, N21, N23, N28, N30, N32, N33, N5, N7, P13, P15, P17, P18, P20, P22, R12, R14, R16, R19, R21, R23, T13, T15, T17, T18, T2, T20, T22, AG11, T28, T32, T5, T7, U12, U14, U16, U19, U21, U23, V12, V14, V16, V19, V21, V23, W13, W15, W17, W18, W20, W22, W28, Y12, Y14, Y16, Y19, Y21, Y23, AH11

Optional CMD GNDs (2)
NC for 4-Lyr cards

GND_OPT C16
GND_OPT W32

bga908-nvidia-n13p-gs-a1

To be configured as needed on the PCB

U30H N13P-GS

CONFIGURABLE POWER CHANNELS

10/19 XVDD

XVDD U1, U2, U3, U4, U5, U6, U7, U8, V1, V2, V3, V4, V5, V6, V7, V8, W2, W3, W4, W5, W7, W8, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, AA1, AA2, AA3, AA4, AA5, AA6, AA7, AA8

bga908-nvidia-n13p-gs-a1

+3V_NVMISC

PLACE NEAR BALLS

C55 DIS@0.1U/10V_4
C53 DIS@0.1U/10V_4

+3V_NVMISC_EN [17,43]

Q12
*CSD@AO3404(30V 5.8A)

R74 DIS@0_6

U30F N13P-GS

18/19 NC/VDD33

NC AC6, AJ28, AJ4, AJ5, AL11, C15, D19, D20, D23, D26, H32, T9, V32

N13P-GT N13P-GS N13P-LP N14P-Q1 N14P-Q3	Other N13M N13P
3V3MISC	VDD33 J8
3V3MISC	VDD33 K8
	VDD33 L8
	VDD33 M8

bga908-nvidia-n13p-gs-a1

C64 DIS@0.1U/10V_4
C69 DIS@0.1U/10V_4

PLACE NEAR BALLS

C84 DIS@1U/6.3V_4
C56 DIS@4.7U/6.3V_6

PLACE NEAR BGA

+3V_GPU

	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

PROJECT : LZ2A
Quanta Computer Inc.

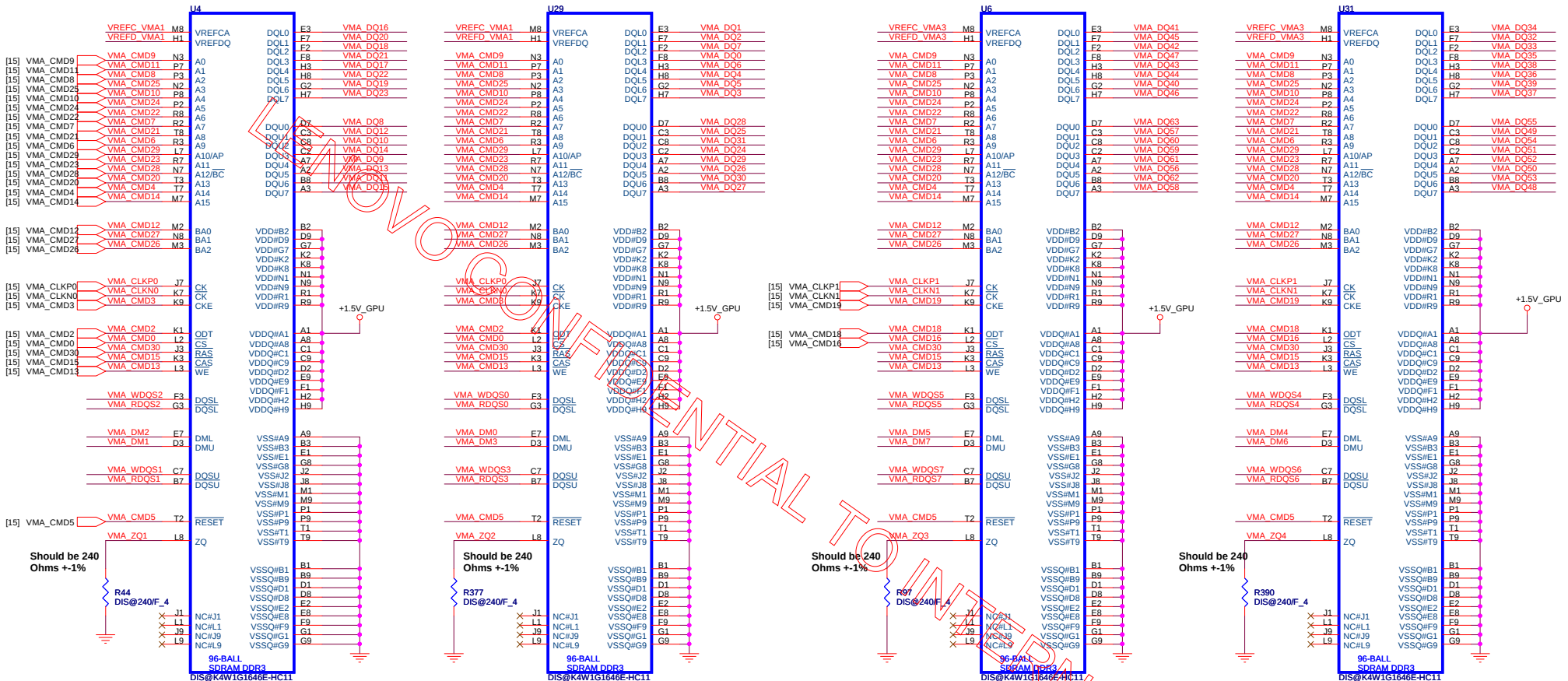
Size	Document Number	Rev
	Nvidia-N13P GB4-128(POWER)	1A

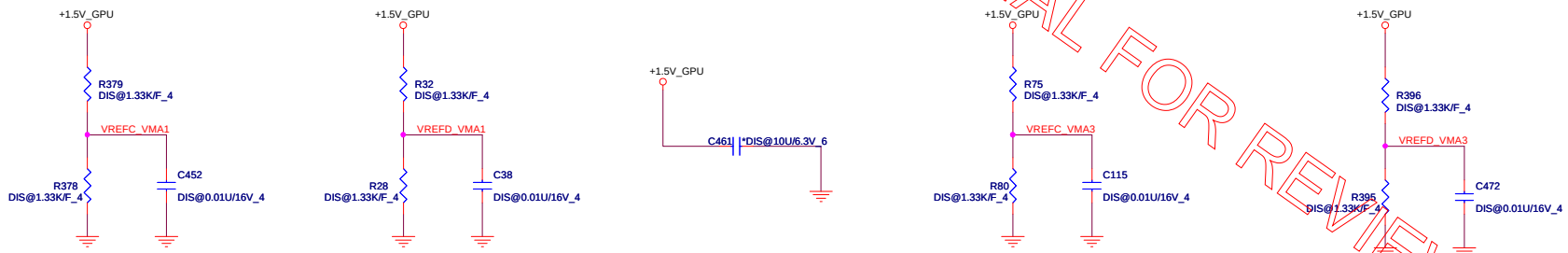
Date: Wednesday, November 30, 2011 Sheet 18 of 45

[14,15,20,33,43] +1.5V_GPU

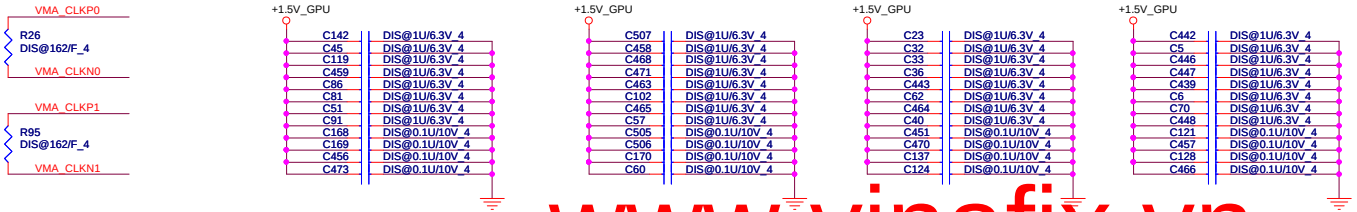
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3





Placement has to be close to VRAM



PROJECT : LZ2A
Quanta Computer Inc.

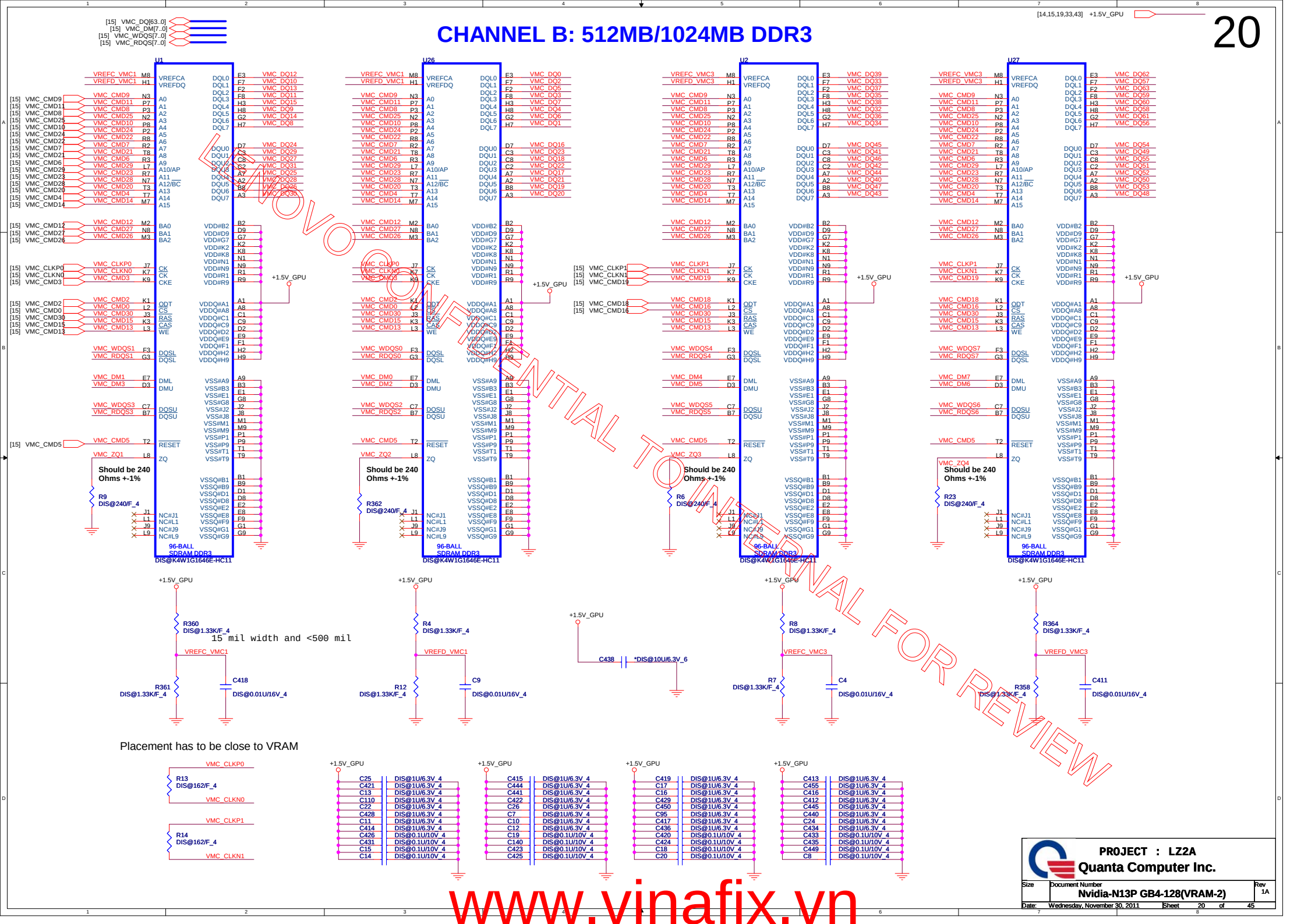
Size	Document Number	Rev
	Nvidia-N13P GB4-128(VRAM-1)	1A

Date: Wednesday, November 30, 2011 Sheet 19 of 45

CHANNEL B: 512MB/1024MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

[14,15,19,33,43] +1.5V_GPU



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(VRAM-2)	1A

Date: Wednesday, November 30, 2011 Sheet 20 of 45

[6,7,8,9,10,12,13,14,15,17,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,22,25,26,29,30,33,34] +5V

Change to KL6/BC HDMI CONN

[6] INT_HDMI_TXDP2 — C620 0.1U/10V_4 — HDMI_TX2+
[6] INT_HDMI_TXDN2 — C619 0.1U/10V_4 — HDMI_TX2-
[6] INT_HDMI_TXDP1 — C618 0.1U/10V_4 — HDMI_TX1+
[6] INT_HDMI_TXDN1 — C617 0.1U/10V_4 — HDMI_TX1-
[6] INT_HDMI_TXDP0 — C616 0.1U/10V_4 — HDMI_TX0+
[6] INT_HDMI_TXDN0 — C615 0.1U/10V_4 — HDMI_TX0-
[6] INT_HDMI_TXCP — C613 0.1U/10V_4 — HDMI_CLK+
[6] INT_HDMI_TXCN — C611 0.1U/10V_4 — HDMI_CLK-

[6] INT_HDMI_SCL — INT_HDMI_SCL
[6] INT_HDMI_SDA — INT_HDMI_SDA
[6] INT_HDMI_HPD — INT_HDMI_HPD

+3V
R316 2.2K_4
R297 2.2K_4
INT_HDMI_SCL
INT_HDMI_SDA
Q43 DMN5L06K-7
Q39 DMN5L06K-7
+5V
R313 2.2K_4
R568 2.2K_4
C668 *68p/50V_4
C669 *68p/50V_4
+5V
F2
FUSE_1.1A_8V_POLY
C667 0.1U/10V_4
HDMIC_5V
HP_DET
HDMI_DDC_CLK
HDMI_DDC_DAT

CN16
HDMI_TX2+ 1 D2+
HDMI_TX2- 2 D2 Shield
HDMI_TX1+ 3 D2-
4 D1+
HDMI_TX1- 5 D1 Shield
HDMI_TX0+ 6 D1-
7 D0+
HDMI_TX0- 8 D0 Shield
HDMI_CLK+ 9 D0-
10 CK+
HDMI_CLK- 11 CK Shield
12 CK-
13 CE Remote
14 NC
HDMI_DDC_CLK 15 DDC CLK
HDMI_DDC_DAT 16 DDC DATA
17 GND
HDMIC_5V 18 +5V
HP_DET 19 HP DET
SHELL1 20
SHELL2 21
SHELL3 22
SHELL4 23
CONN_HDMI

R315 590/F_4 — HDMI_TX2+
R310 590/F_4 — HDMI_TX2-
R304 590/F_4 — HDMI_TX1+
R302 590/F_4 — HDMI_TX1-
R300 590/F_4 — HDMI_TX0+
R298 590/F_4 — HDMI_TX0-
R294 590/F_4 — HDMI_CLK+
R291 590/F_4 — HDMI_CLK-
SC51 *0.1U/10V_4
3HDMI_LF
Q42 2N7002K
+5V

+3V
R551 10K_4
INT_HDMI_HPD
Q69A ME2N7002DKW-G
+3V
R553 10K_4
HP_DET
Q69B ME2N7002DKW-G
R549 20K_4
Place close to PCH

For ESD

U39 *CM1225
HDMI_TX2+ 6 NC CH4 5 HDMI_TX2+
HDMI_TX2- 7 NC CH3 4 HDMI_TX2-
8 GND GND 3
HDMI_TX1+ 9 NC CH2 2 HDMI_TX1+
HDMI_TX1- 10 NC CH1 1 HDMI_TX1-

U38 *CM1225
HDMI_TX0+ 6 NC CH4 5 HDMI_TX0+
HDMI_TX0- 7 NC CH3 4 HDMI_TX0-
8 GND GND 3
HDMI_CLK+ 9 NC CH2 2 HDMI_CLK+
HDMI_CLK- 10 NC CH1 1 HDMI_CLK-

U37 *CM1225
HDMI_DDC_DAT 6 NC CH4 5 HDMI_DDC_DAT
HDMI_DDC_CLK 7 NC CH3 4 HDMI_DDC_CLK
8 GND GND 3
HDMIC_5V 9 NC CH2 2 HDMIC_5V
HP_DET 10 NC CH1 1 HP_DET

For EMI

HDMI_TX2+ — R574 150/F_4
HDMI_TX2-
HDMI_TX1+ — R573 150/F_4
HDMI_TX1-
HDMI_TX0+ — R572 150/F_4
HDMI_TX0-
HDMI_CLK+ — R569 150/F_4
HDMI_CLK-

PROJECT : LZ2A
Quanta Computer Inc.
Size: Custom
Document Number: Madison_LVDS/HDMI/CRT switchable
Rev: 1A
Date: Wednesday, November 30, 2011
Sheet 21 of 45

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

[6] INT_CRT_RED
[6] INT_CRT_GRE
[6] INT_CRT_BLU
[6] INT_CRT_VSYNC
[6] INT_CRT_HSYNC
[6] INT_DDCCLK
[6] INT_DDCDAT

D22 RB500V-40
CRT_VCC
C526 0.1U/10V_4
+5V
C527 0.1U/10V_4
F1 FUSE_1.1A_8V_POLY
CRT_VCC_R

L7 BLM15BA470SS1D CRT_R1
L8 BLM15BA470SS1D CRT_G1
L9 BLM15BA470SS1D CRT_B1

R231 150/F_4
R232 150/F_4
R228 150/F_4
C212 5.6P/50V/COG_4
C214 5.6P/50V/COG_4
C225 5.6P/50V/COG_4
C215 5.6P/50V/COG_4
C213 5.6P/50V/COG_4
C211 5.6P/50V/COG_4
TP15

CN12 CRT_CONN

ESD PROTECTION
U35 *IP4220CZ6
U12 *IP4220CZ6

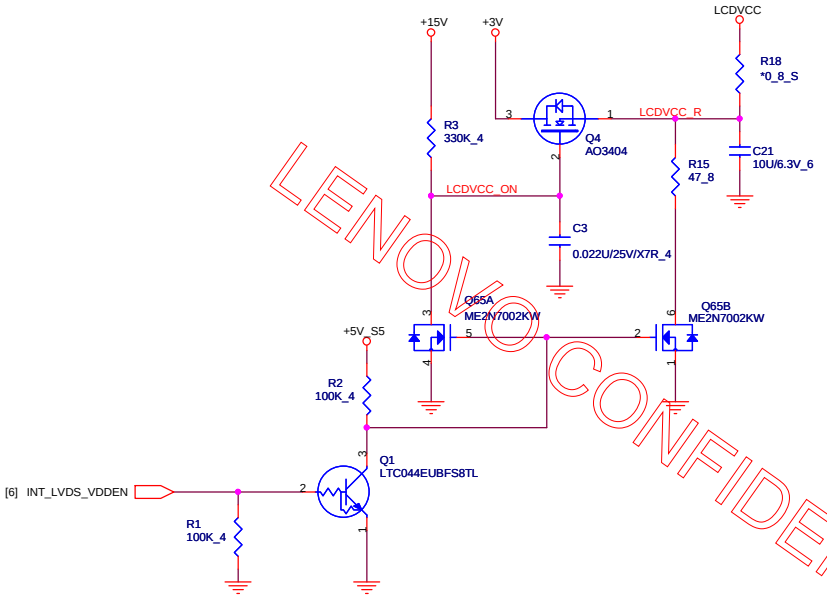
U33 AHCT1G125DCH
U34 AHCT1G125DCH
C554 0.1U/10V_4
VGAVSYNC_R
VGAHSYNC_R
R493 10_4
R502 10_4
Place near U37,U38 < 200 mil
CRTVSYNC1
CRTHSYNC1
C538 *10P/50V/COG_4
C529 *10P/50V/COG_4
L25 BK1608HS121-T
L26 BK1608HS121-T
CRTVSYNC
CRTHSYNC
C539 10P/50V/COG_4
C528 10P/50V/COG_4
Place near CN5002 connector < 200 mil

+3V
R201 2.2K_4
R163 2.2K_4
Q64A ME2N7002DKW-G
Q64B ME2N7002DKW-G
R191 4.7K_4
R177 4.7K_4
DDCCLK
DDCDAT
C201 *10P/50V/COG_4
C194 *10P/50V/COG_4
For EMI

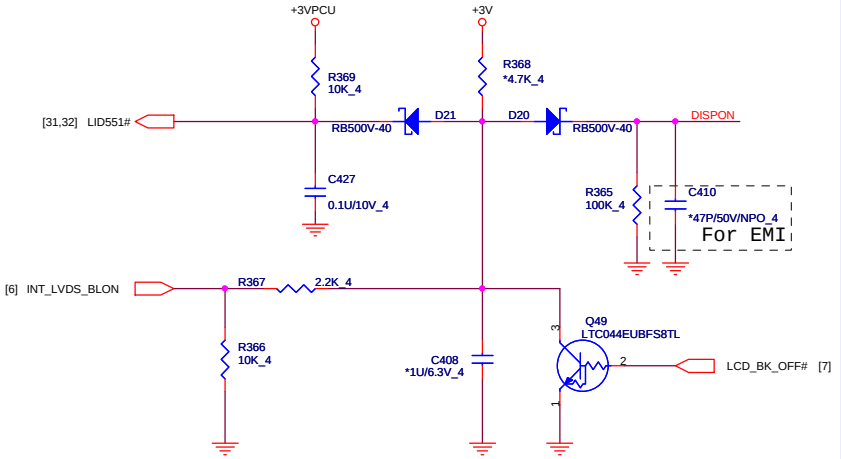
PROJECT : LZ2A
Quanta Computer Inc.
Size: Custom
Document Number: CRT CONN
Rev: 1A
Date: Wednesday, November 30, 2011
Sheet 22 of 45

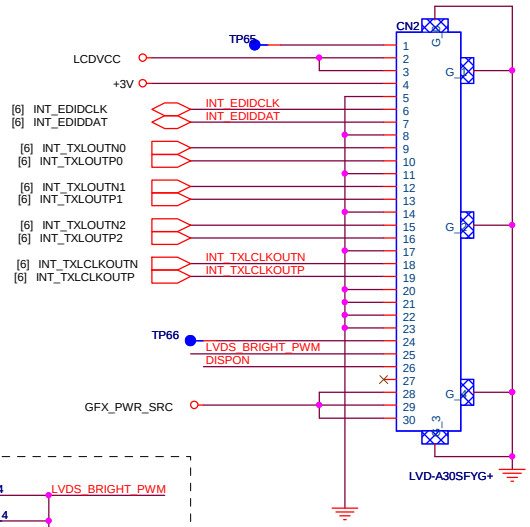
[26,30,34,36,43] +15V
[6,7,8,9,10,12,13,14,15,17,21,22,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,26,28,31,33,34] +5V_S5
[6,7,24,26,27,31,32,34,35,36,40] +3VPCU
[33,35,36,37,38,39,41,42] VIN

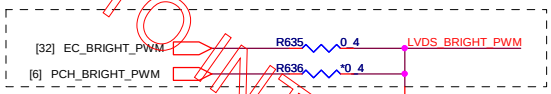
LCDVCC

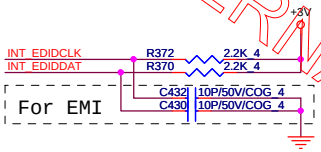


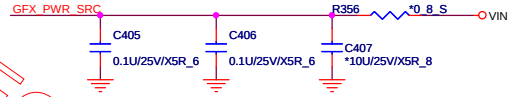
Back Light

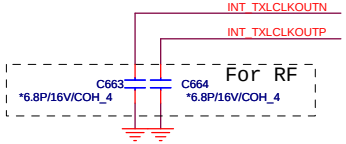












PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A

Date: Wednesday, November 30, 2011 Sheet 23 of 45

[6,7,23,26,27,31,32,34,35,36,40] +3VPCU
[33,34] LANVCC
[6,7,8,9,10,12,13,14,15,17,21,22,23,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V

LANVCC

* R594 open when use RTL8105E

U45 RTL81111F/RTL8105E

* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.

* C476 and C472 are for U24 LAN_EVDD12 pin 21.

* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Tramsformer

Reserve for Surge
Line to Line TVS

*UCLAMP2512T.TCT

TST1284R LF

Layout:All termination signal should have 30 mil trace

Gas Tube Discharge _ Reserve for Surge

Reserve for Surge
Line to GND Gas Tube Discharge

*CM1293A-04SO

*LAN1G@CM1293A-04SO

10/100 non-stuff

Reserve for Surge
Line to GND TVS

*LAN1G@UCLAMP2512T.TCT

Reserve for Surge
Line to Line TVS

RJ45 Connector

EMI:close RJ45

Orange LED

GREEN LED

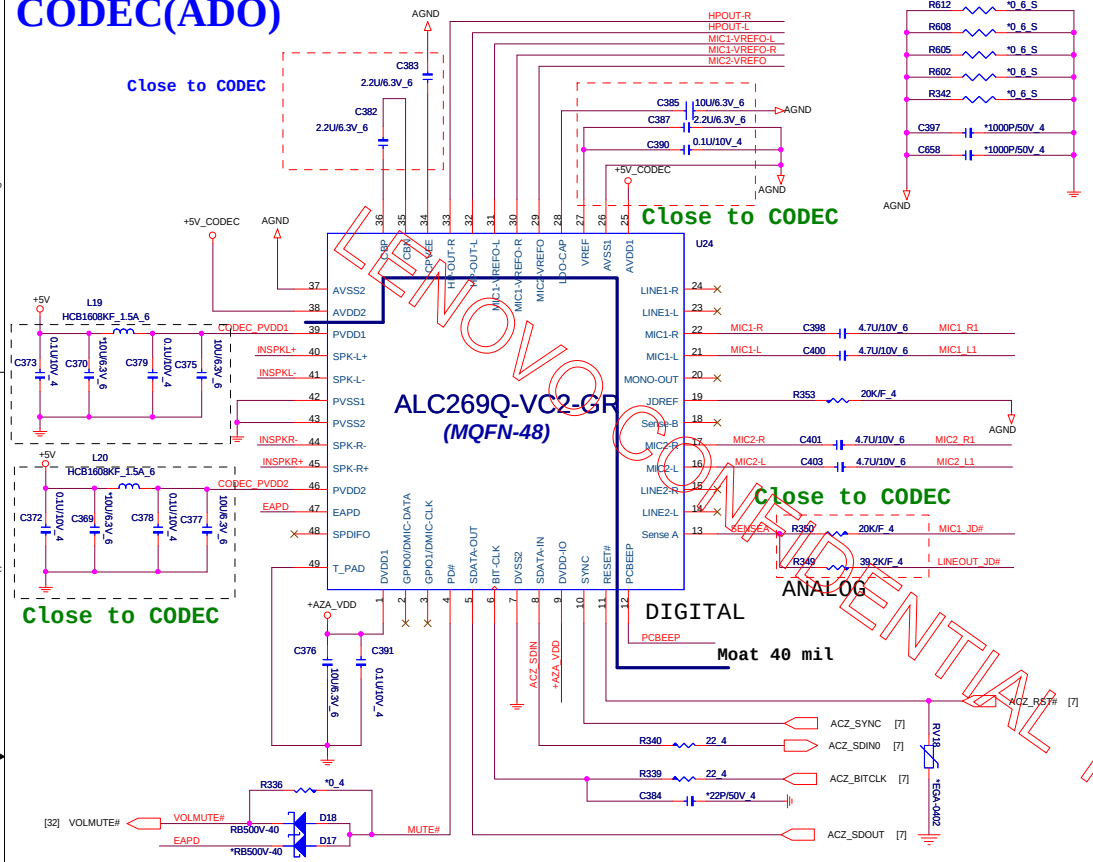
EMI:close RJ45

PROJECT : LZ2A
Quanta Computer Inc.

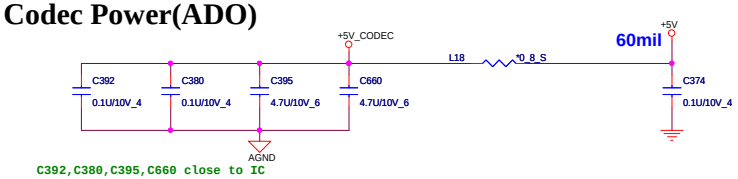
Size	Document Number	Rev
Custom	RTL81111F/RTL8105E	1A

Date: Wednesday, November 30, 2011 Sheet 24 of 45

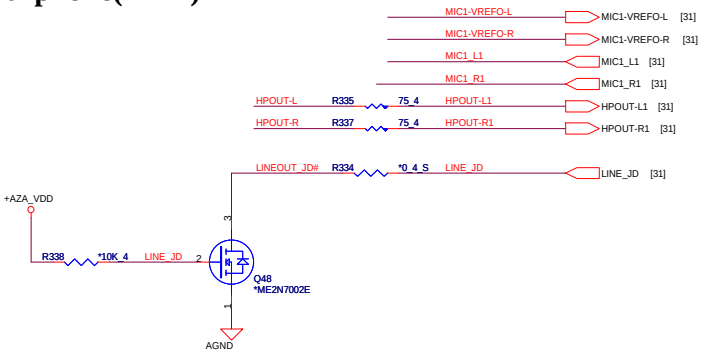
CODEC(ADO)



Codec Power(ADO)

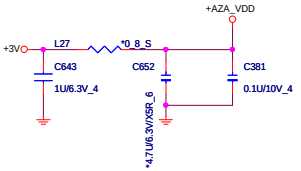


Earphone(AMP)

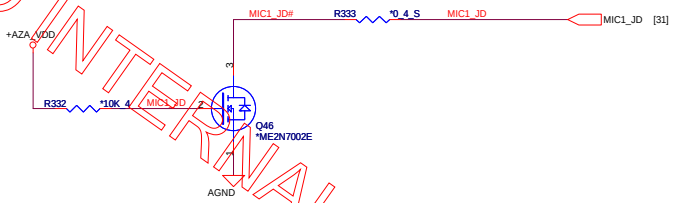


HDA Power(ADO)

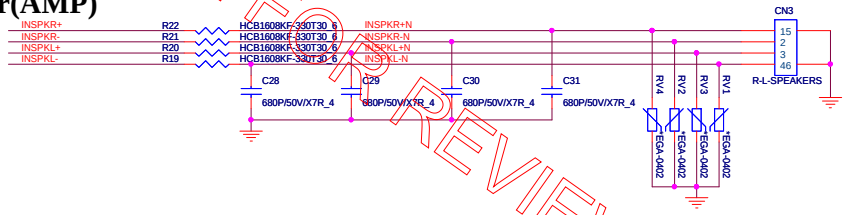
*Intel HDA Either +1.5V_S5 or +3V_S5



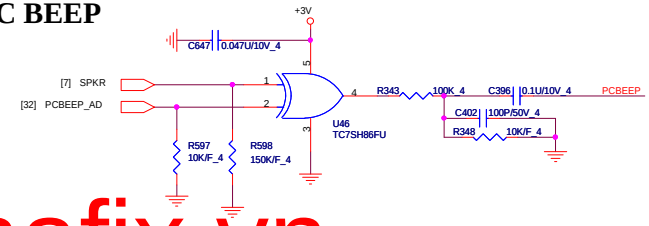
System MIC(AMP)



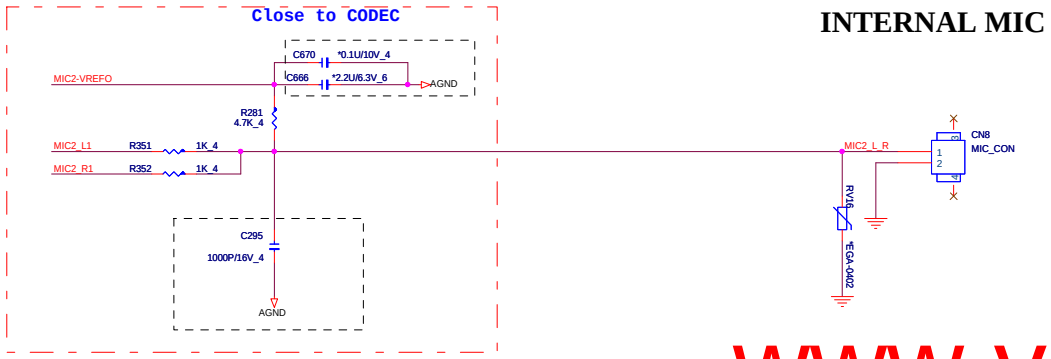
Speaker(AMP)



PC BEEP

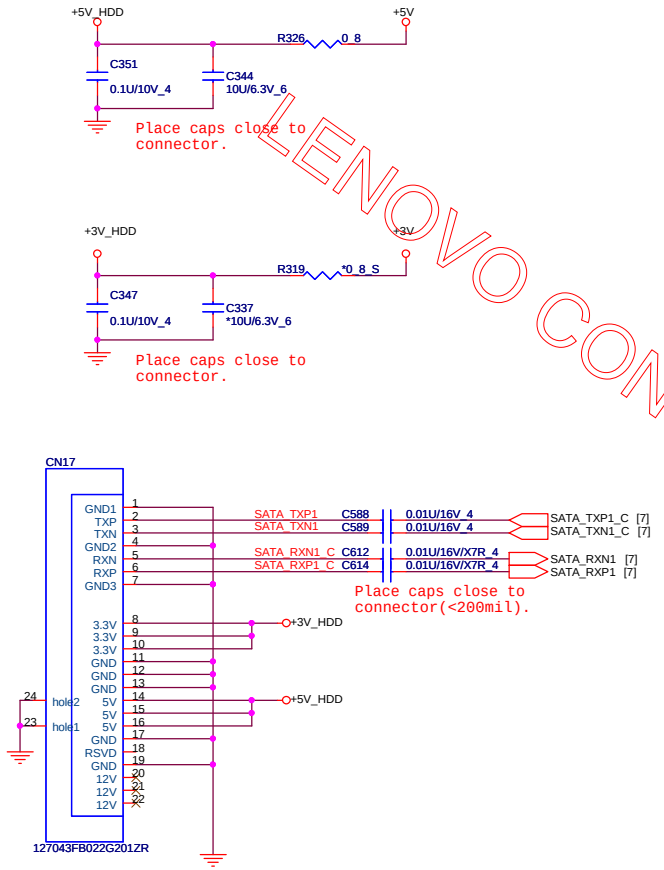


INTERNAL MIC



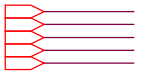
PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: ALC269/MIC/Line out	Rev: 1A
Date: Wednesday, November 30, 2011	Sheet 25 of 45	

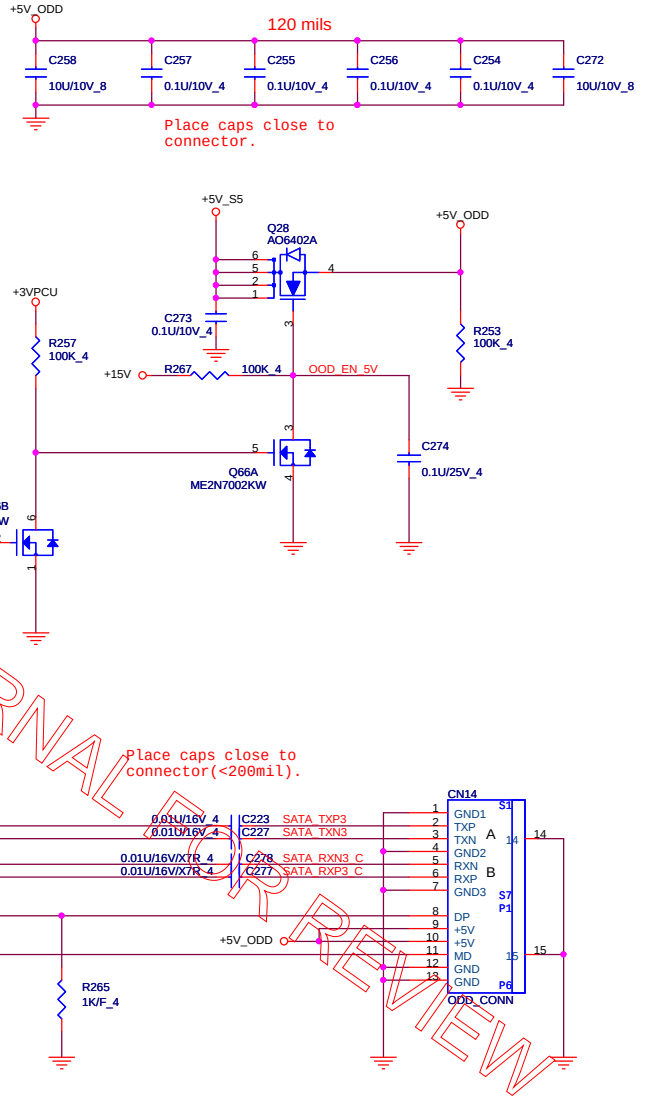
SATA HDD Connector.



SATA ODD Connector.

[7,10,21,22,25,29,30,33,34] +5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,34,35,36,37,38,39,40,41,42,43] +5VPCU
[6,7,23,24,27,31,32,34,35,36,40] +3VPCU
[23,30,34,36,43] +15V





PROJECT : LZ2A
Quanta Computer Inc.

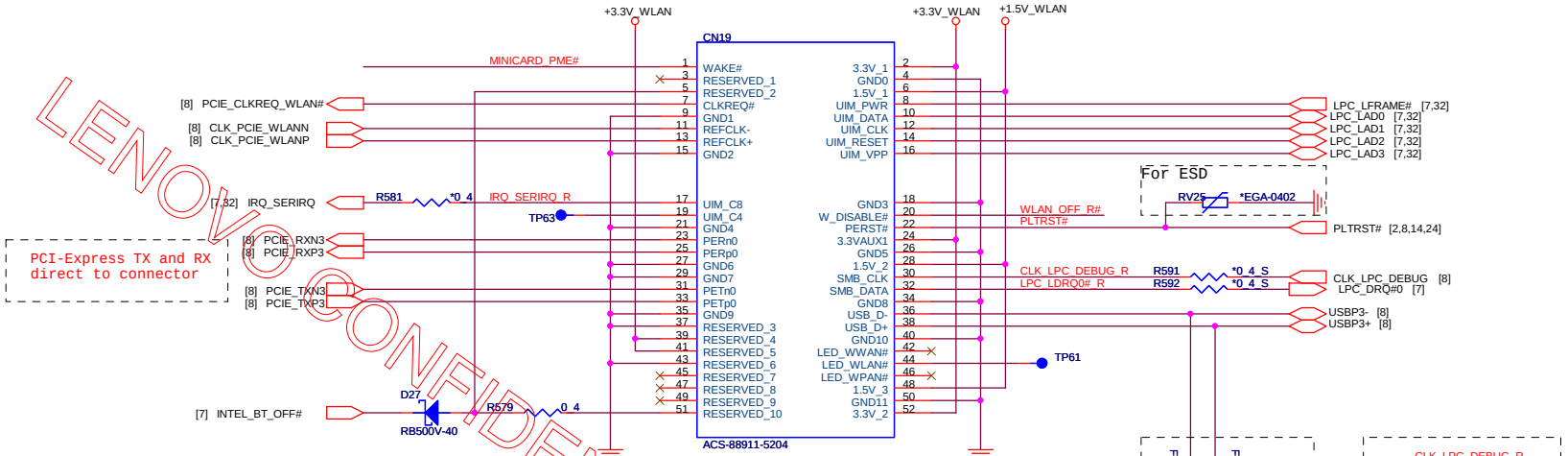
Size	Document Number	Rev
Custom	SATA HDD/CD-ROM	1A

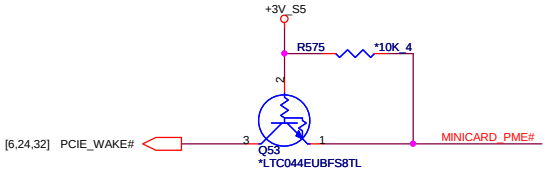
Date: Wednesday, November 30, 2011 Sheet 26 of 45

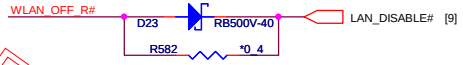
MiniCard WLAN connector

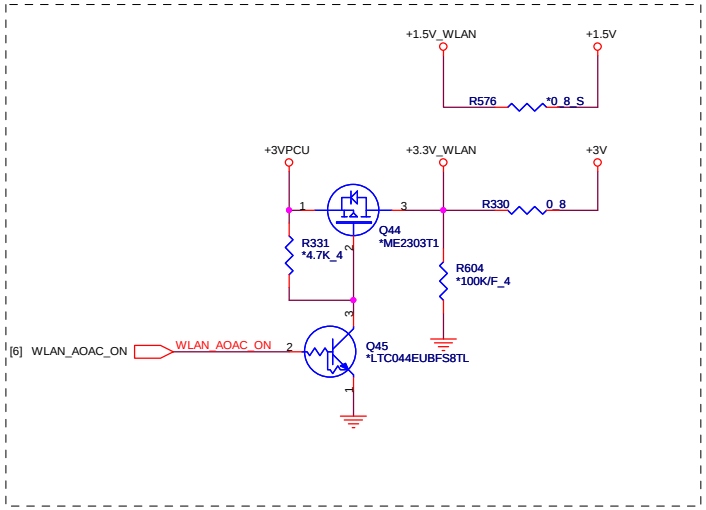
[2,6,7,8,9,10,31,34] +3V_S5
[4,10] +1.5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,29,30,31,32,33,34,37,38,41,42,43] +3V

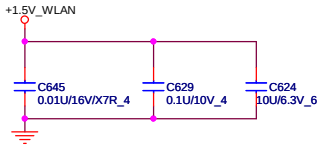
27

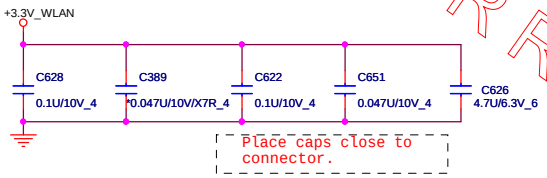










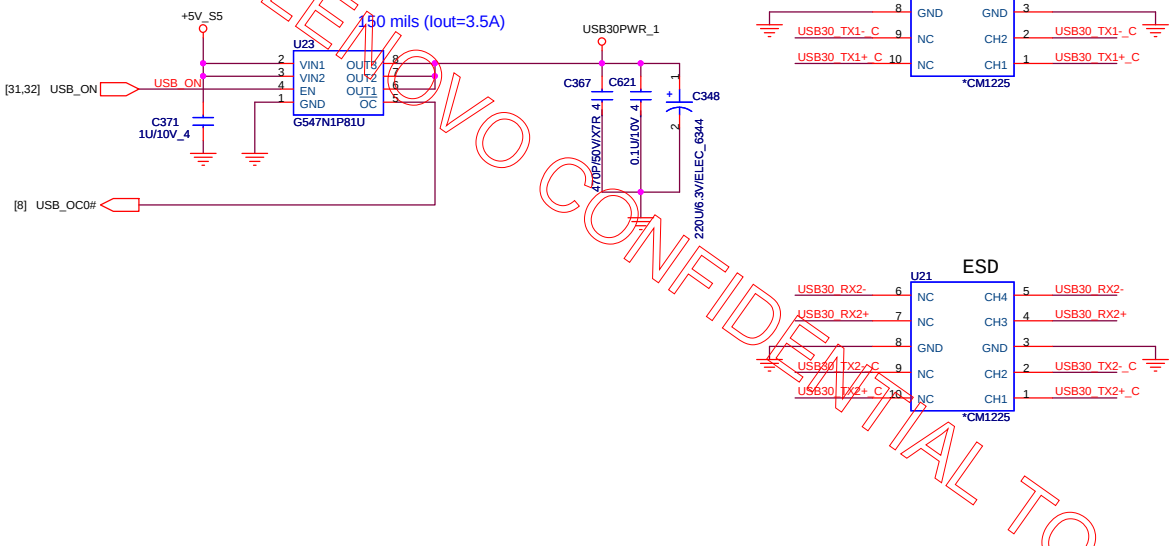


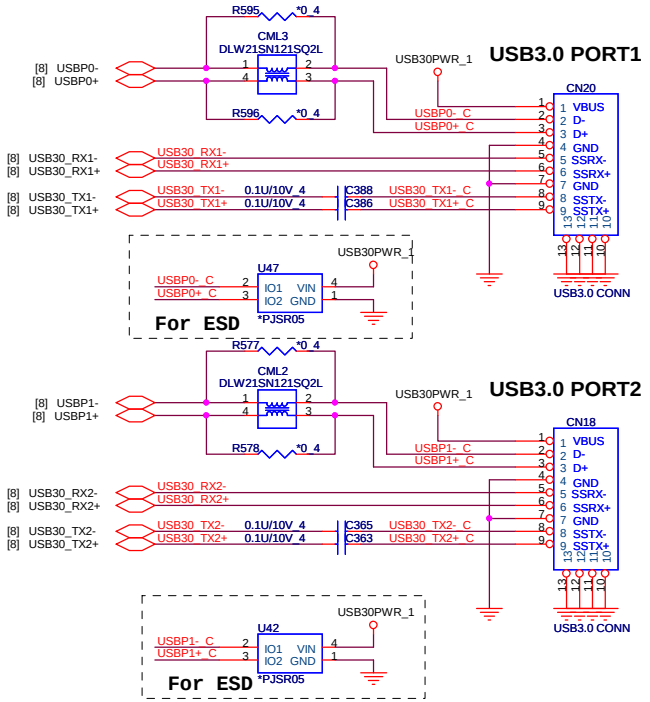
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB2.0*2/WLAN/BT	1A

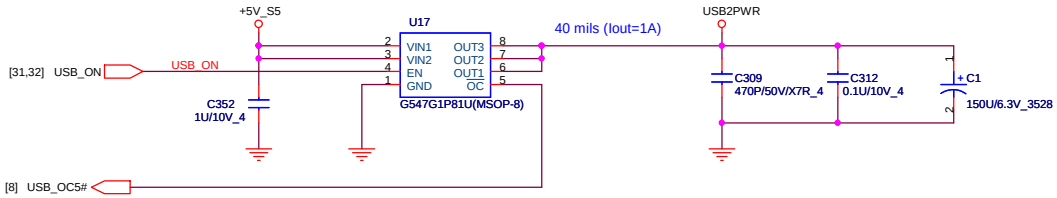
Date: Wednesday, November 30, 2011 Sheet 27 of 45

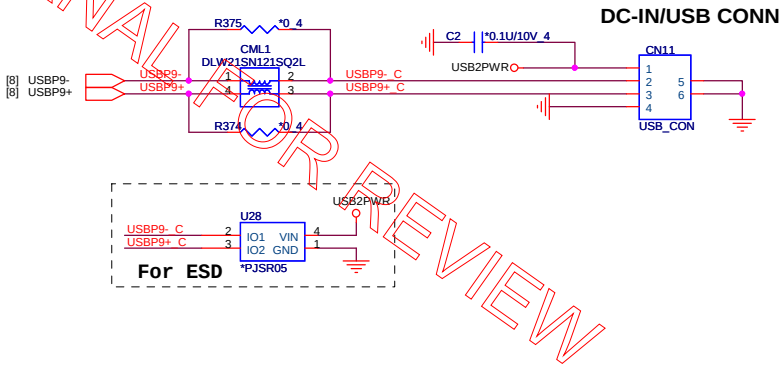
USB3.0*2





USB2.0*1





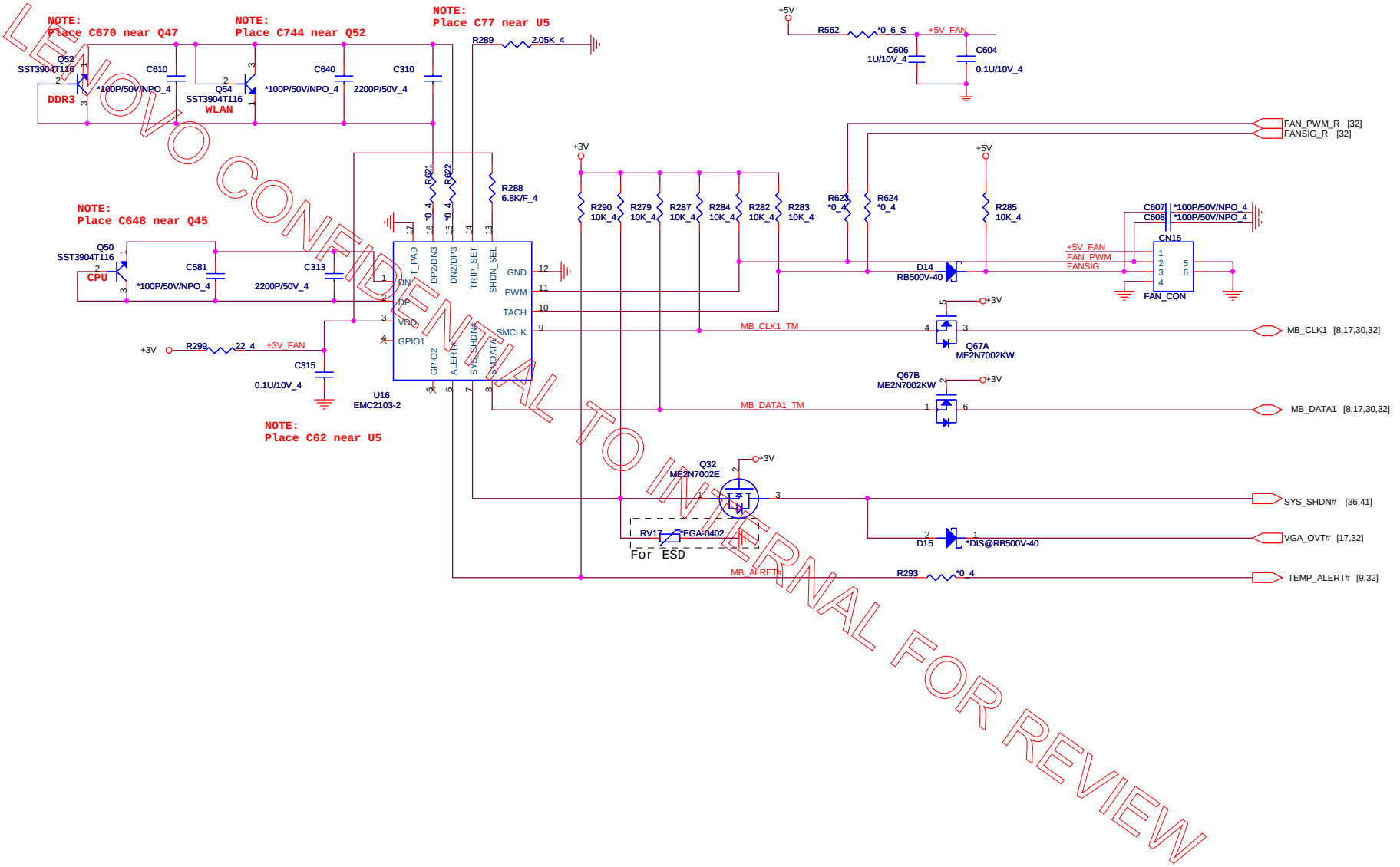
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB3.0 *1	1A

Date: Wednesday, November 30, 2011 Sheet 28 of 45

[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,21,22,25,26,30,33,34] +5V

FAN CONTROL



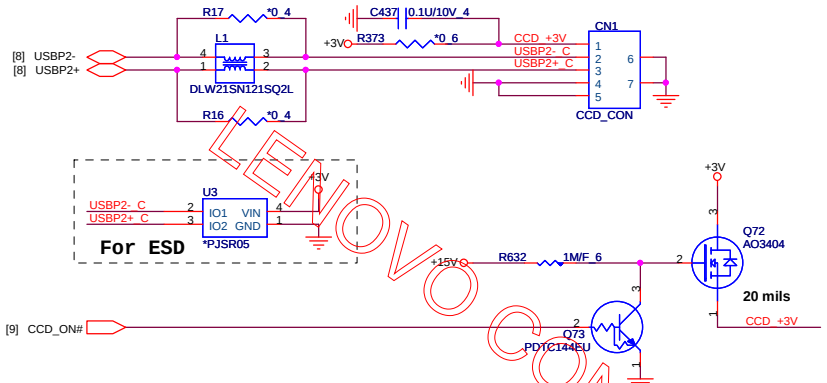
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A

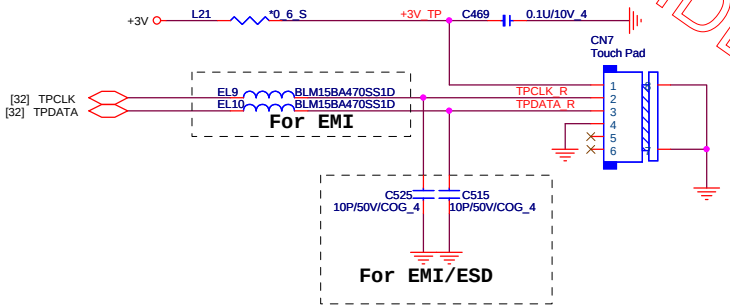
Date: Wednesday, November 30, 2011 Sheet 29 of 45

[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,31,32,33,34,37,38,41,42,43] +3V
[7,10,21,22,25,26,29,33,34] +5V
[23,26,34,36,43] +15V

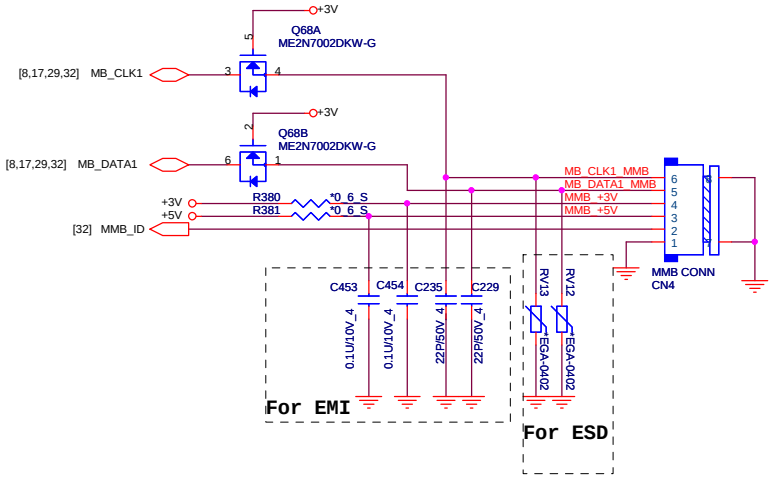
CCD BOARD



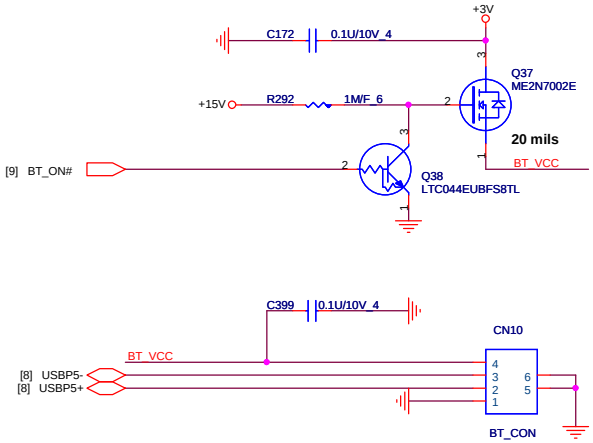
Touch pad



MMB



BLUETOOTH

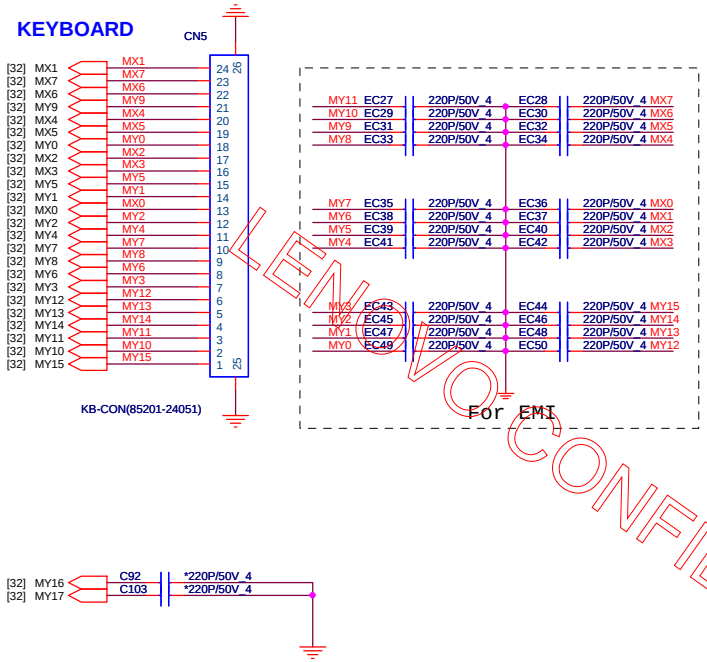


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CCD/TP/BT/MMB	1A

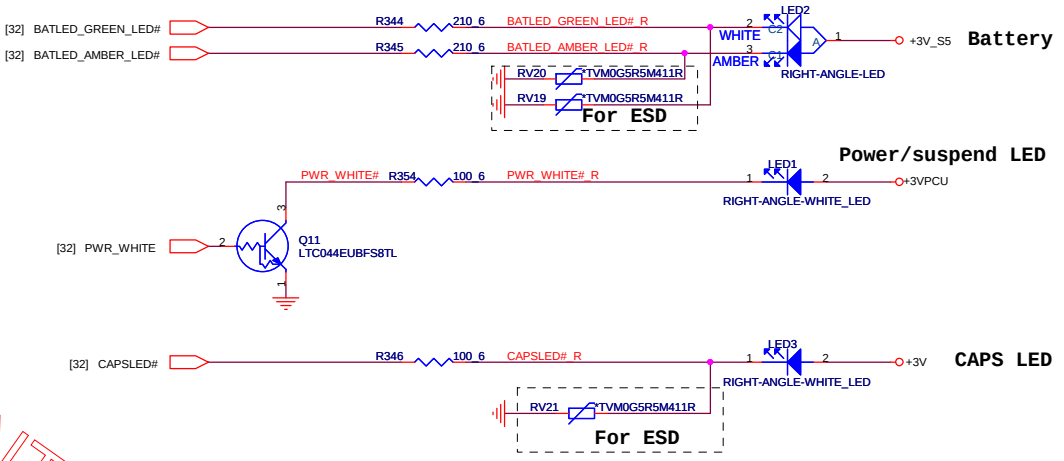
Date: Wednesday, November 30, 2011 Sheet 30 of 45

KEYBOARD

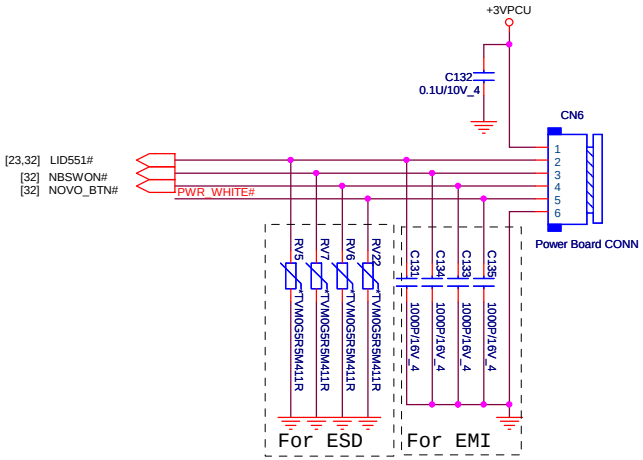


LED

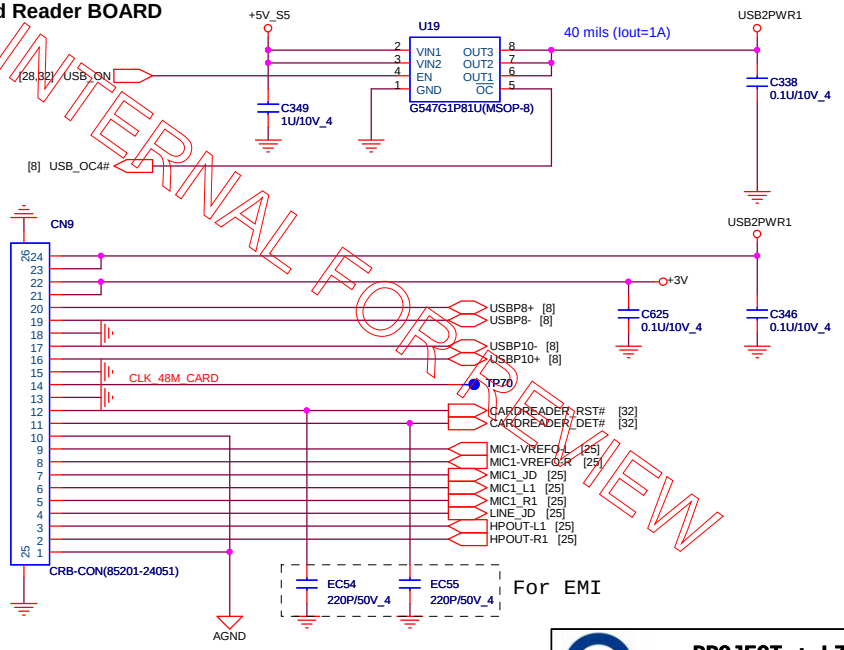
[6,7,23,24,26,27,32,34,35,36,40] +3VPCU
[10,23,26,28,33,34] +5V_S5
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,32,33,34,37,38,41,42,43] +3V
[2,6,7,8,9,10,27,34] +3V_S5



POWER BOARD



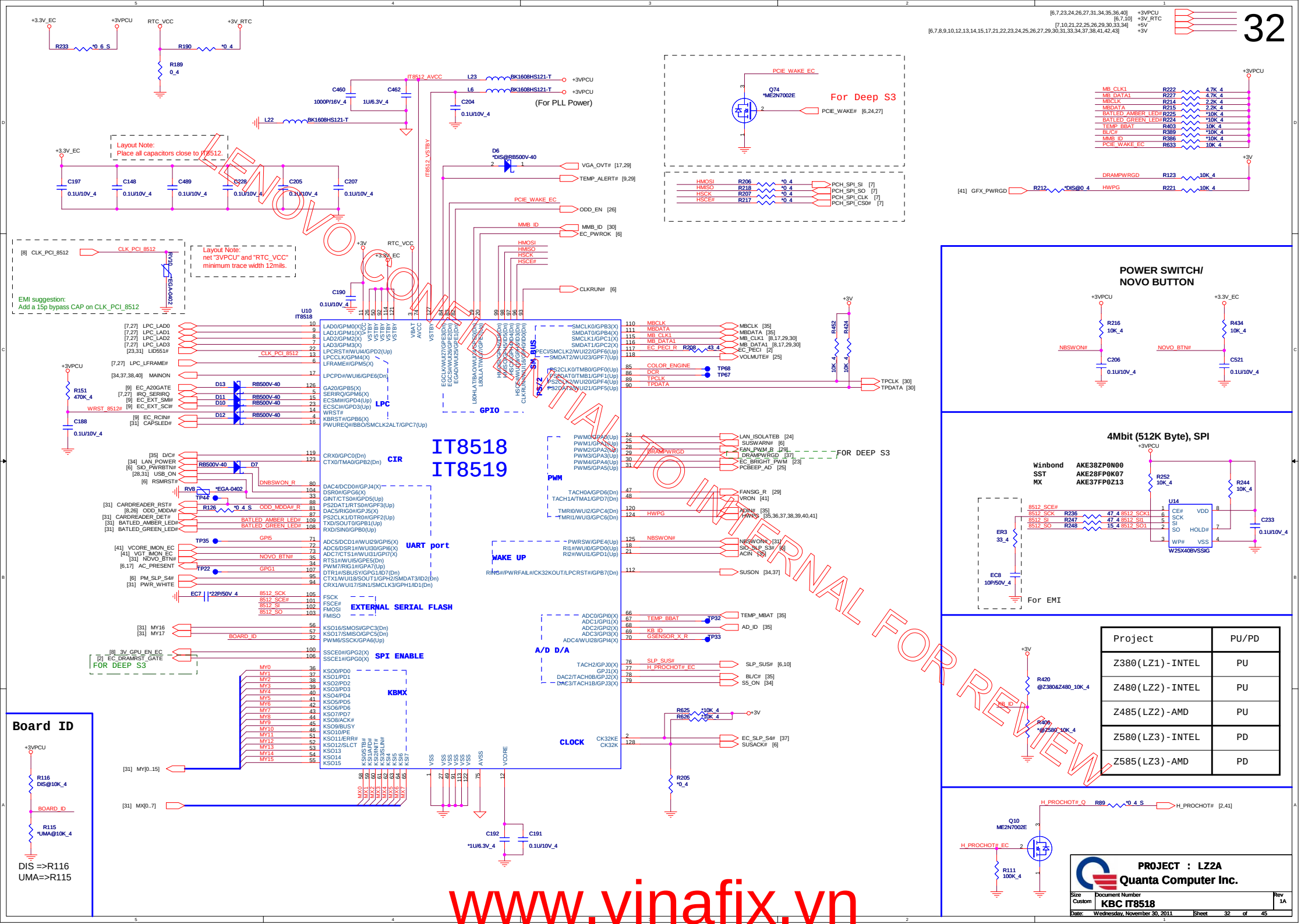
Card Reader BOARD



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PB/LED/CRB	1A

Date: Wednesday, November 30, 2011 Sheet 31 of 45



Screw for ME

SPAD1 *SPAD-Z480-1
SPAD3 *SPAD-Z480-1
SPAD4 *SPAD-Z480-2
SPAD2 *SPAD-Z480-2

VGA
HOLE12 DIS@H-TC5_5BC4I3D3P2
HOLE13 H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

HOLE8 *HG-TC276BC315D106P2
HOLE10 *HG-TC276BC315D106P2
HOLE6 *HG-TC256BC315D106P2
HOLE11 *HG-TC276BC315D106P2

CPU BKT

HOLE4 *H-C86D86N
HOLE7 *C142D102N
HOLE3 *H-TC217BC256D118P2
HOLE14 *H-TC7IC3_7BC8D2_7P2
HOLE9 *H-C87D87N
HOLE5 *H-O316X276ID91P2
HOLE2 *H-O316X276ID91P2
HOLE1 *H-TC6_3IC3_7BC8D2_7P2

For ESD

+0.85V +1.8V SC23 SC24 *0.1U/10V_4
+1.05V_GFX_PCIE +1.05V_PCH SC31 SC32 *0.1U/10V_4
+0.85V +1.5V_CPU SC11 SC13 SC12 SC27 SC26 *0.1U/10V_4
+5V_S5 SC42 *0.1U/10V_4
+5V_S5 SC41 *0.1U/10V_4
+1.5V_SUS +1.5V_CPU SC29 SC28 *0.1U/10V_4
+1.5V_SUS VIN SC40 SC39 0.1U/25V_4
+3V +5V SC33 SC30 0.1U/10V_4
+VCC_CORE VIN SC9 SC46 0.1U/25V_4
+VCC_GFX SC15 SC18 *0.1U/10V_4
+5V SC38 SC25 SC37 0.1U/10V_4
+1.05V_GFX_PCIE GFX_CORE SC4 *0.1U/10V_4
+VCC_GFX SC17 SC16 SC14 SC20 SC19 SC21 SC49 SC22 SC50 SC47 SC48 SC6 SC5 *0.1U/10V_4
+1.05V_PCH
+1.05V_PCH
+1.05V_GFX_PCIE
+VCC_CORE SC8 SC10 *0.1U/10V_4
+1.5V_GPU SC2 SC43 SC3 *0.1U/10V_4
+1.5V_GPU SC7 SC45 *0.1U/10V_4
+1.5V_GPU SC44 SC1 *0.1U/10V_4
+1.5V_SUS SC35 SC34 SC36 *0.1U/10V_4

For EMI

VIN EC6 EC20 EC12 EC25 EC1 EC18 EC2 EC21 EC5 EC3 EC16 0.1U/25V_4
LANVCC EC11 0.1U/10V_4
VBATT EC22 0.1U/25V_4
+1.5V_SUS FC2 3.3p/16V/NP0_4
+1.5V_SUS FC1 3.3p/16V/NP0_4
+1.5V_WLAN FC5 47P/50V/NPO_4
+3.3V_WLAN FC3 47P/50V/NPO_4
+5V EC51 EC52 0.1U/10V_4 *0.1U/10V_4

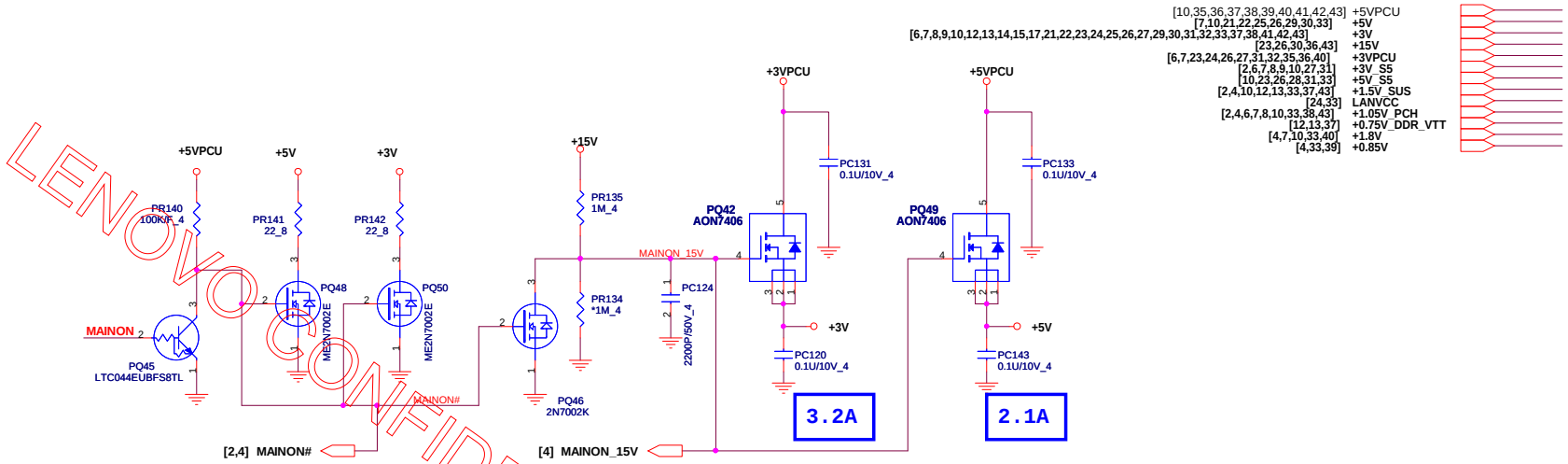
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
B	HOLD/SKEW/ESD/EMI	1A

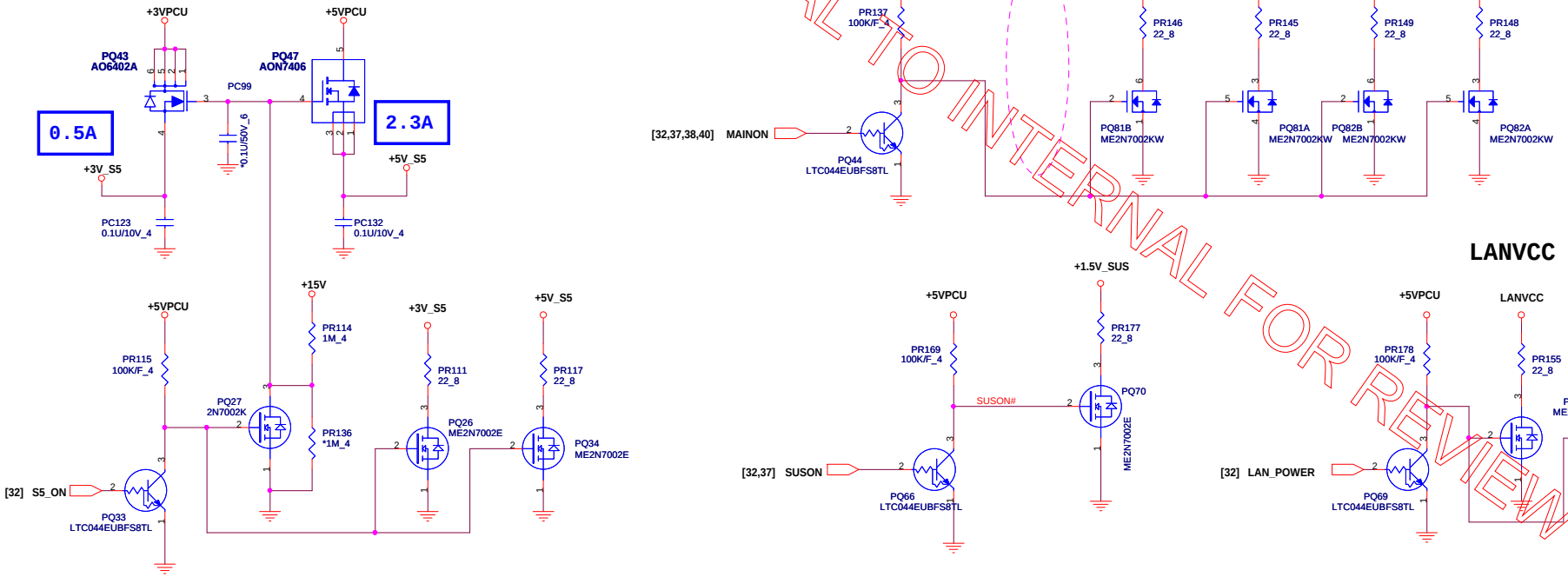
Date: Wednesday, November 30, 2011 Sheet 33 of 45

DISCHARGE

+3V, +5V



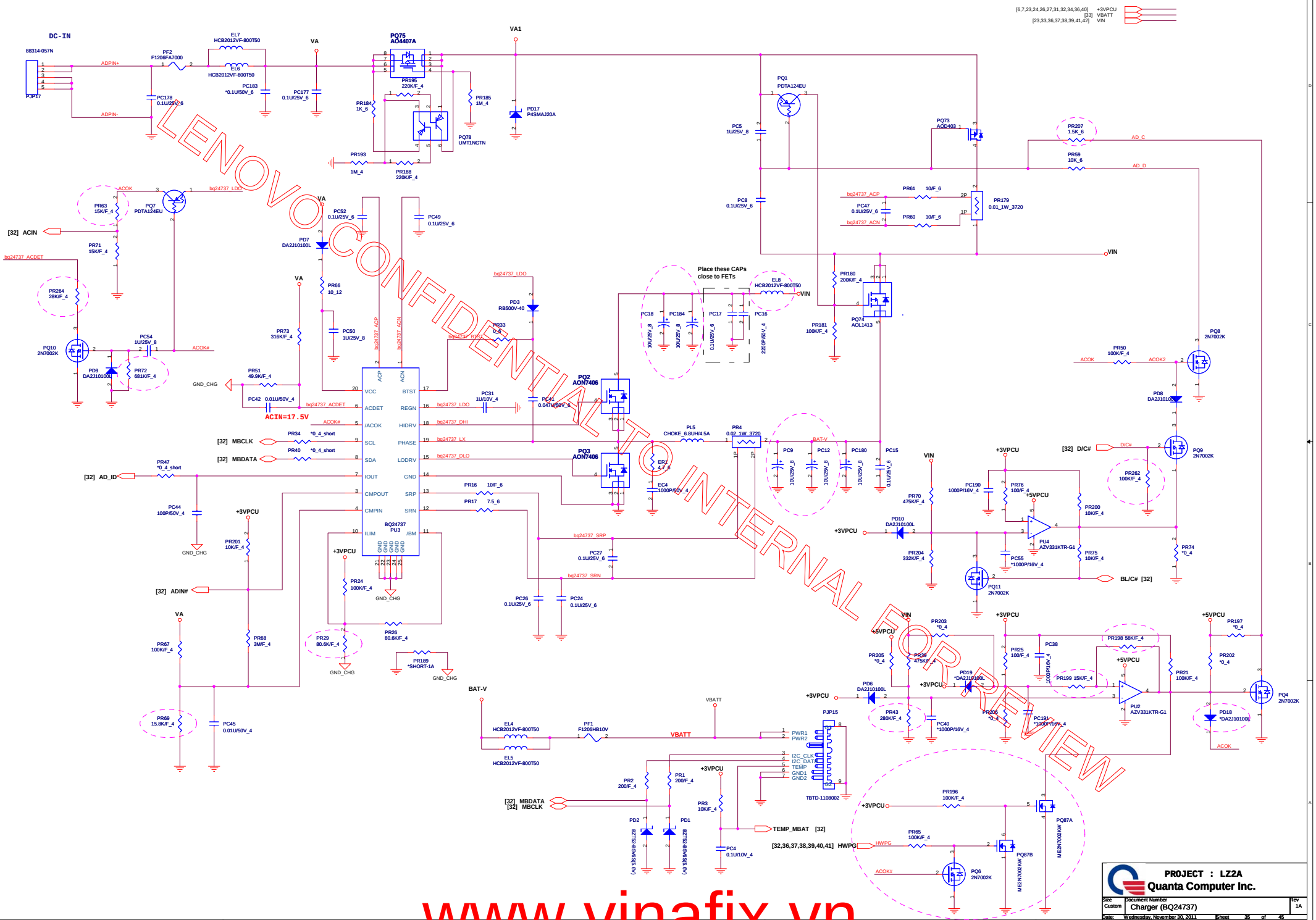
3V_S5, 5V_S5

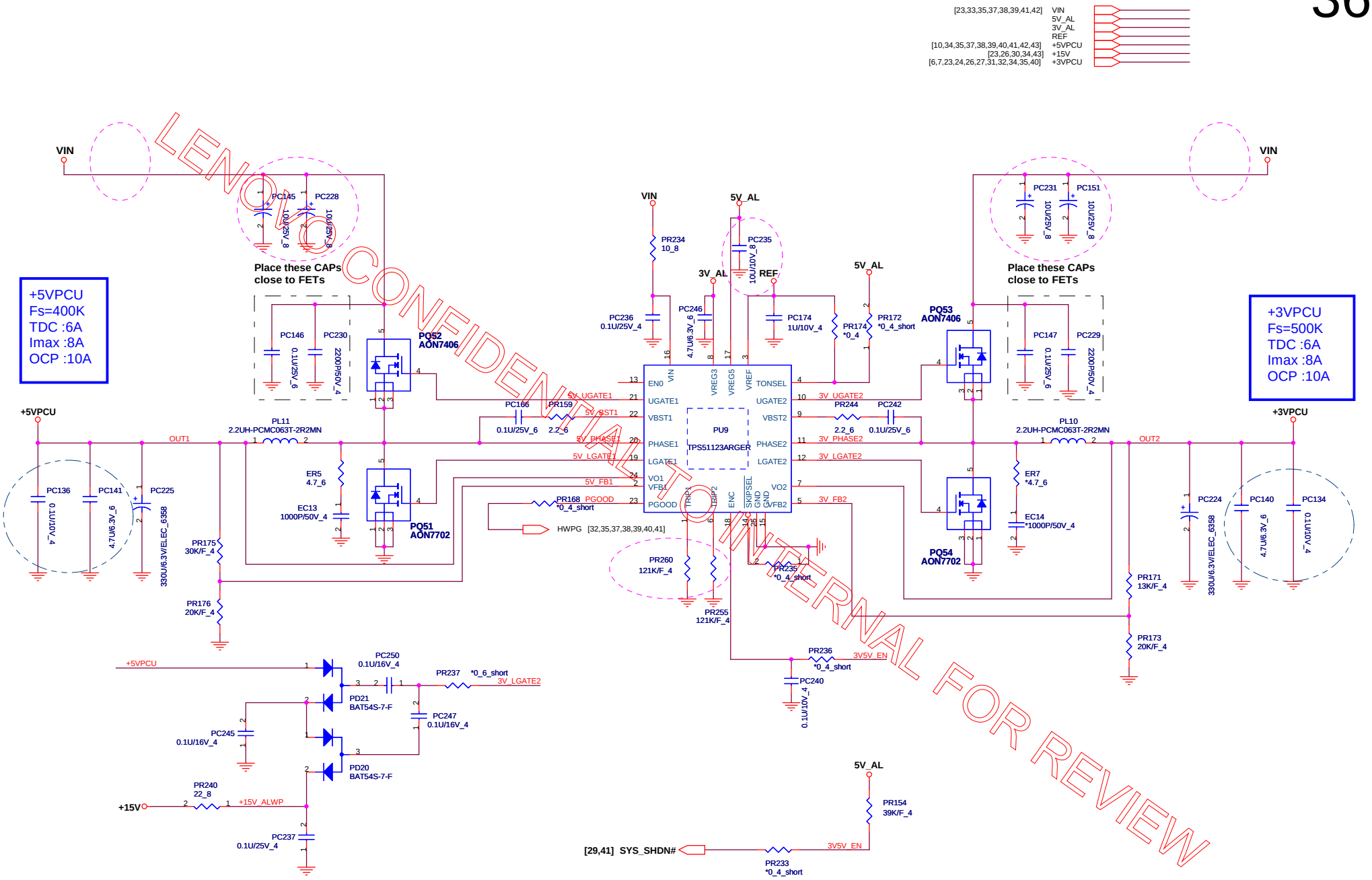


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	

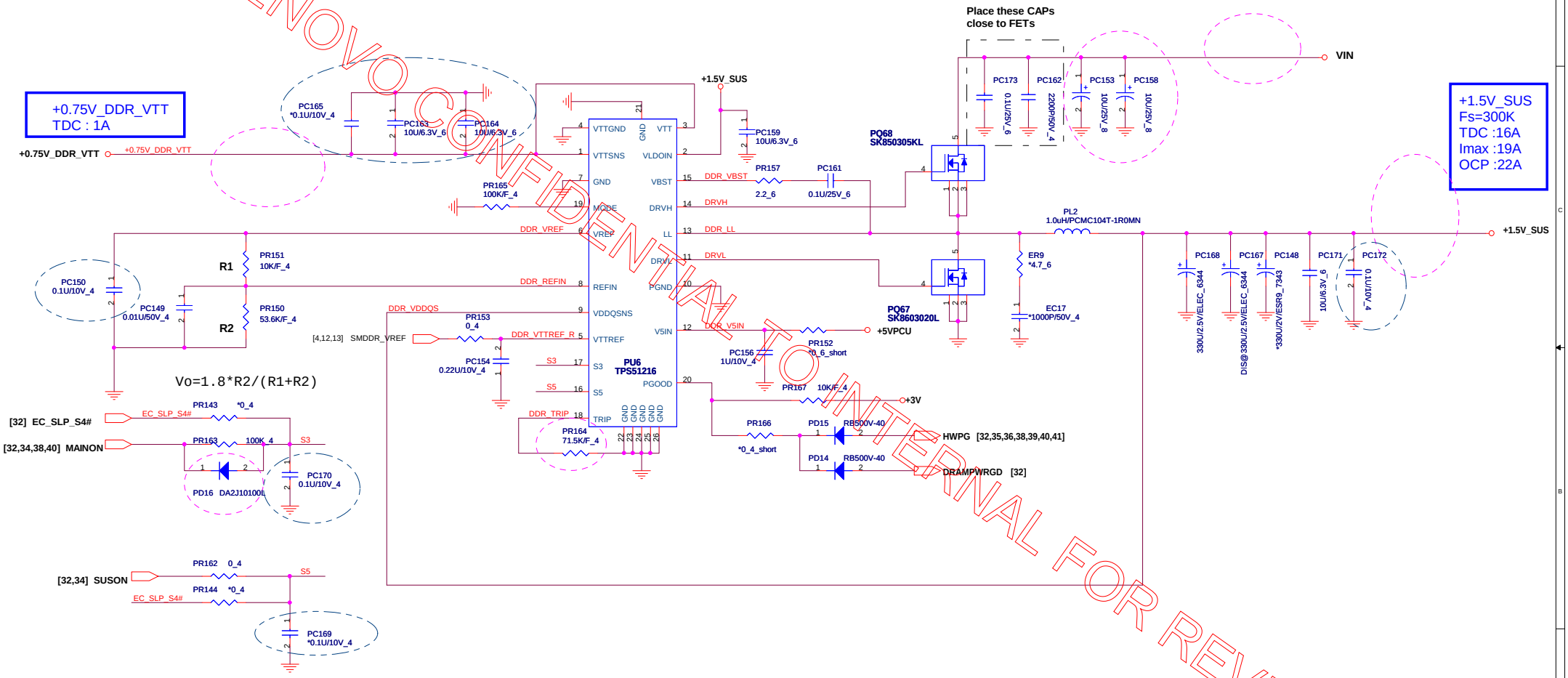
Date: Wednesday, November 30, 2011 Sheet 34 of 45



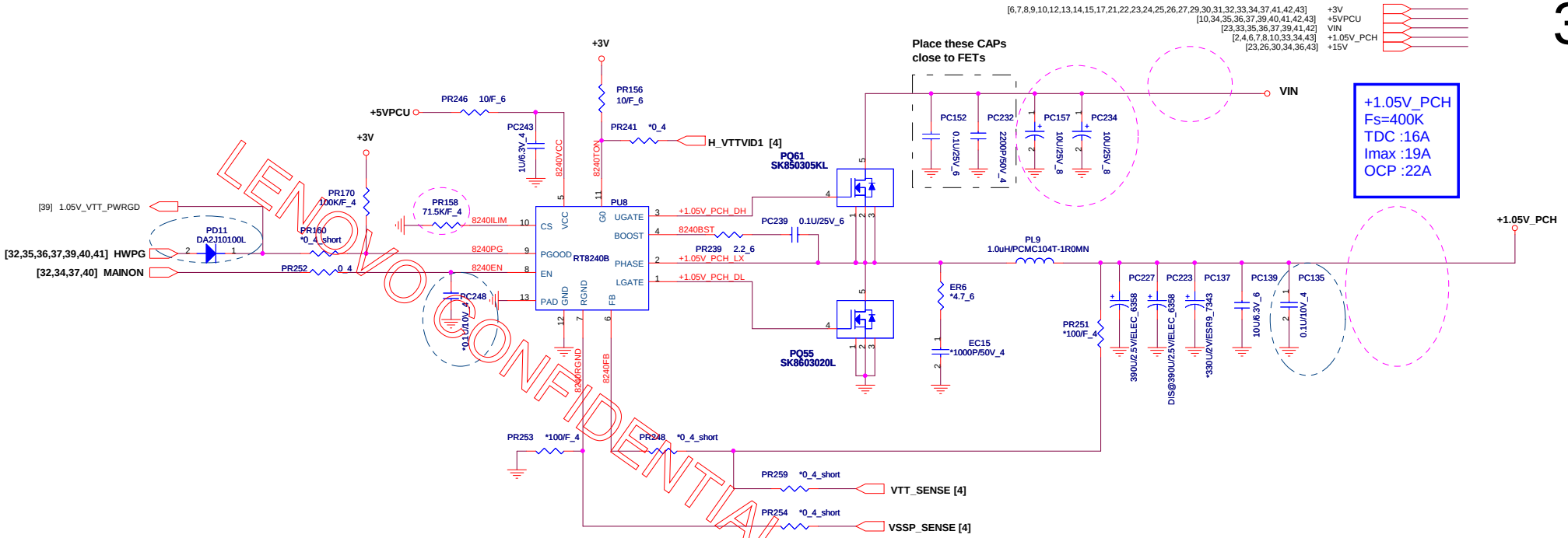


PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number		Rev
	3V/5V (TPS51123ARGER)		
Date: Wednesday, November 30, 2011	Sheet 36	of 45	

[12,13,34] +0.75V_DDR_VTT
[23,33,35,36,38,39,41,42] VIN
[2,4,10,12,13,33,34,43] +1.5V_SUS



PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: DDR3/0.75V (TPS51216)	Rev
Date: Wednesday, November 30, 2011	Sheet 37 of 45	

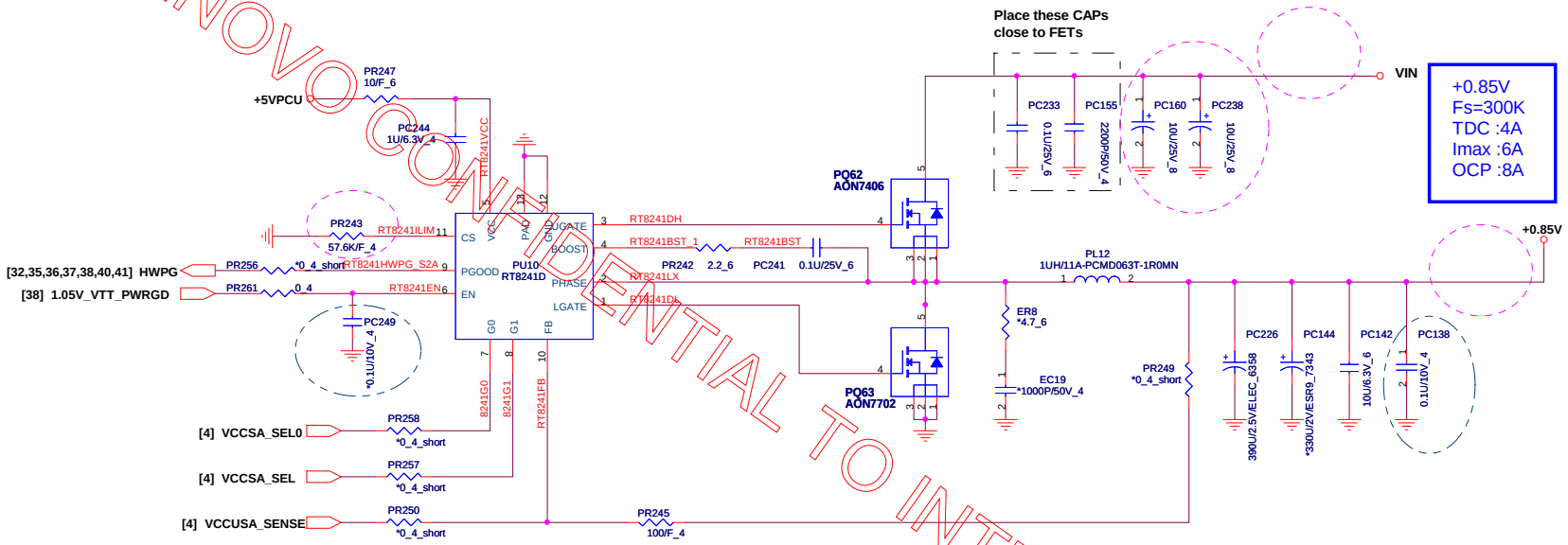


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V_PCH	

Date: Wednesday, November 30, 2011 Sheet 38 of 45

[10,34,35,36,37,38,40,41,42,43] +5VPCU
[23,33,35,36,37,38,41,42] VIN
[4,33,34] +0.85V



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

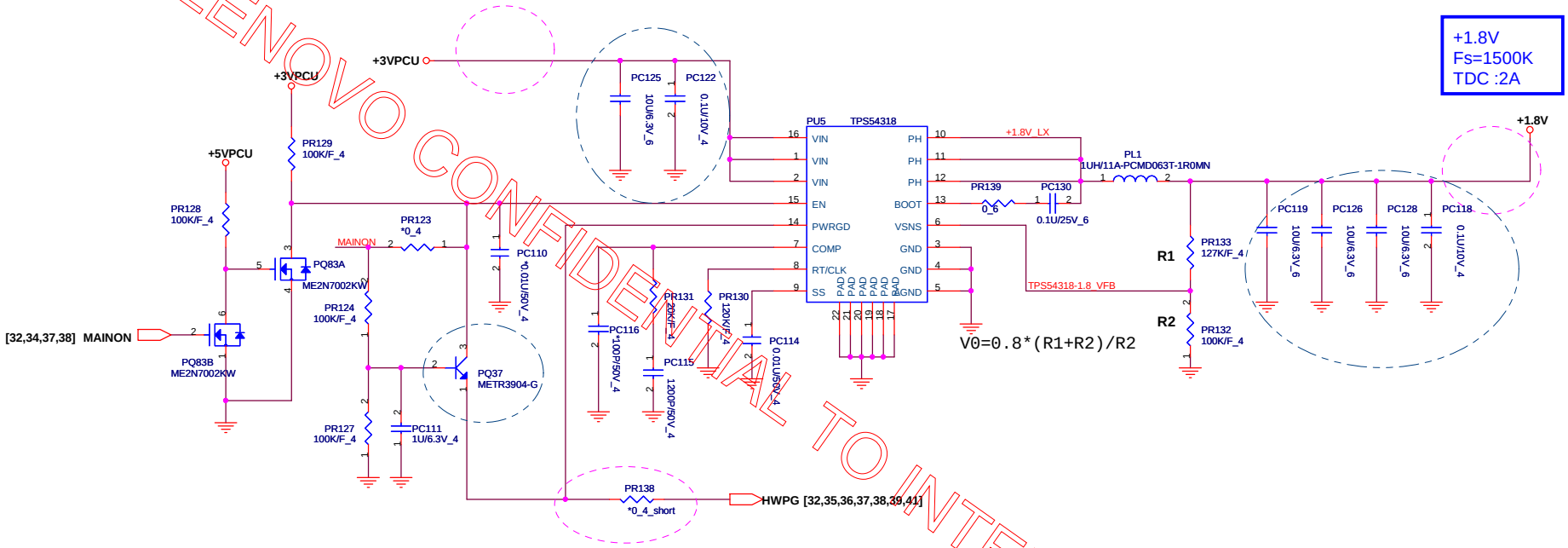
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	VCCSA (RT8241A)	

Date: Wednesday, November 30, 2011 Sheet 39 of 45

[10,34,35,36,37,38,39,41,42,43] +5VPCU
[6,7,23,24,26,27,31,32,34,35,36] +3VPCU
[4,7,10,33,34] +1.8V

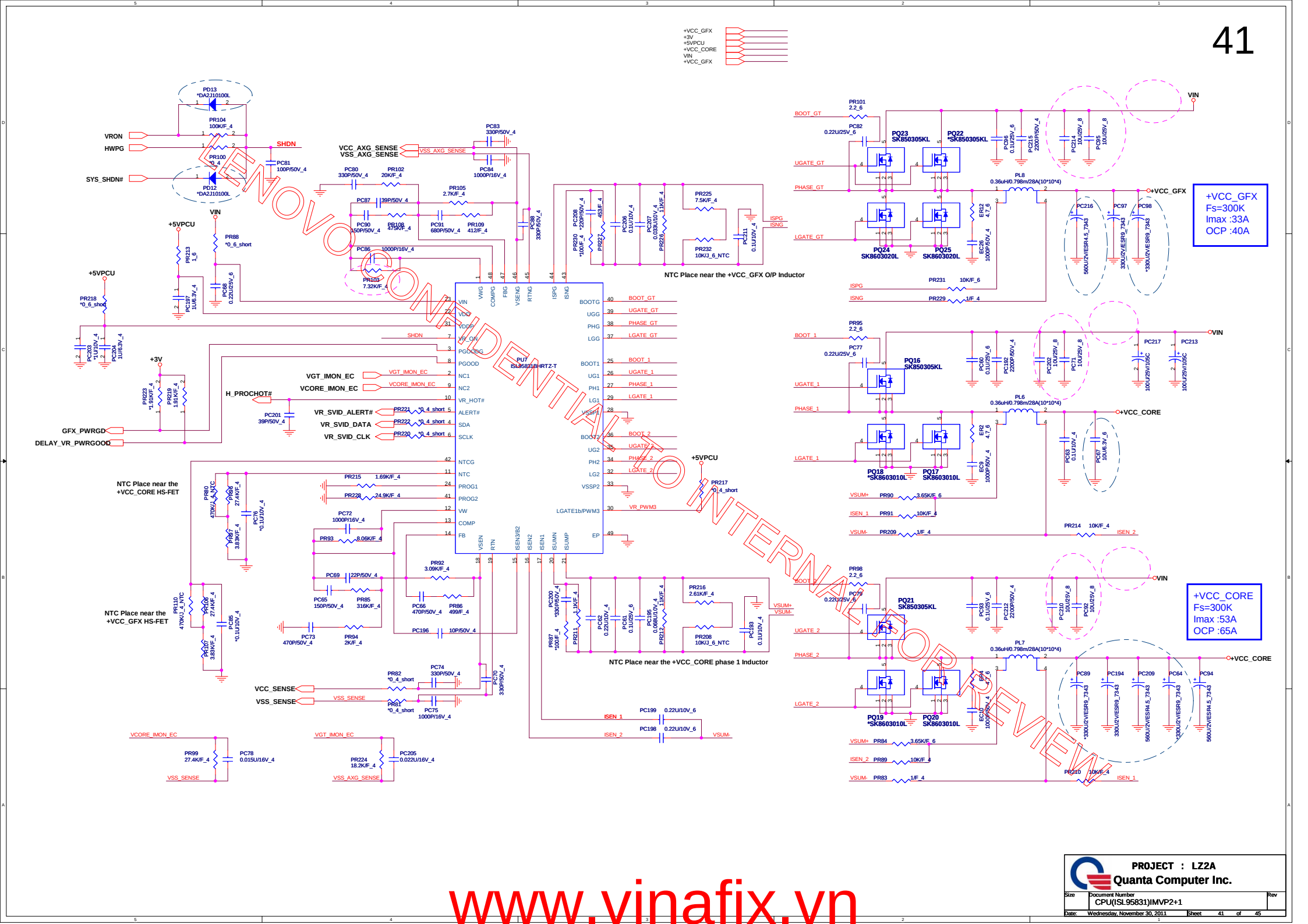
+1.8V
Fs=1500K
TDC :2A

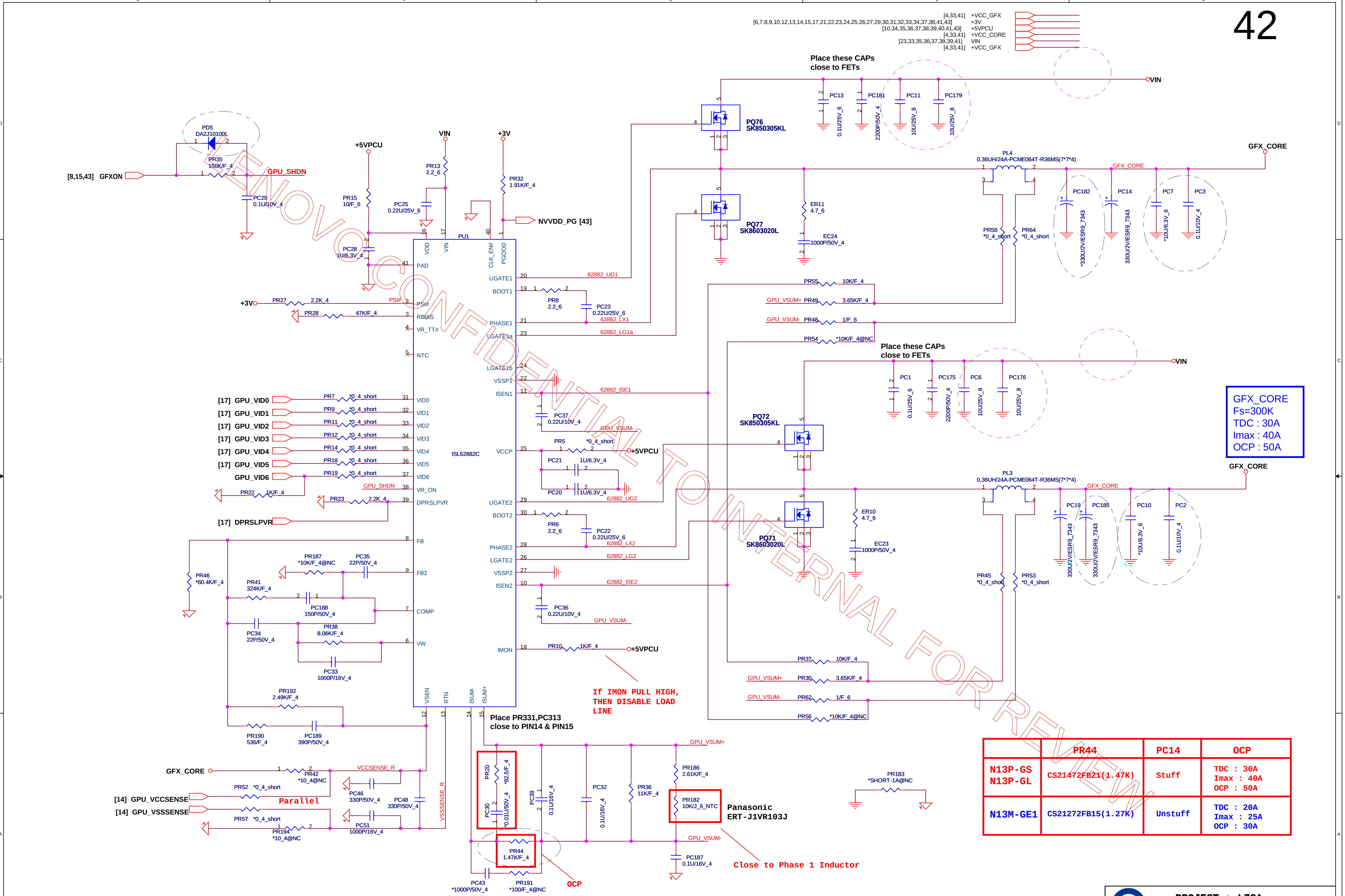


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	1.8V (TPS54318)	

Date: Wednesday, November 30, 2011 Sheet 40 of 45





	PR44	PC14	OCP
N13P-GS N13P-GL	CS21472FB21(1.47K)	Stuff	TDC : 30A Imax : 40A OCP : 50A
N13M-GE1	CS21272FB15(1.27K)	Unstuff	TDC : 20A Imax : 25A OCP : 30A

PROJECT : LZ2A

Quanta Computer Inc.

Size | Document Number: DGPU (ISL62882C) 2 Phase | Rev

Date: Wednesday, November 30, 2011 | Sheet 42 of 45

[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42] +3V
[14,16,17,18] +3V_GPU
[10,34,35,36,37,38,39,40,41,42] +5VPCU
[14,15,19,20,33] +1.5V_GPU
[23,26,30,34,36] +15V
[2,4,10,12,13,33,34,37] +1.5V_SUS
[14,15,16,33] +1.05V_GFX_PCIE
[2,4,6,7,8,10,33,34,38] +1.05V_PCH

5.5A

PQ40 DIS@SK8603020L

PC112 DIS@10U/6.3V_6 · PC117 DIS@10U/6.3V_6 · PC107 DIS@10U/6.3V_6 · PC106 DIS@10U/6.3V_6 · PC101 *330U/2.5V/9m_3528 · PC102 *0.1U/10V_4

PR79 DIS@22_8 · PR77 DIS@1M_4 · PR78 DIS@100K/F_4 · PQ85A · PQ85B ME2N7002KW · PQ14 DIS@ME2N7002E · R688 100K_4 · [15] +1.5V_GPU_EN · PC100 DIS@0.022U/25V/X7R_4

R109 EV@10K/F_4 · R141 EV@10K/F_4 · GFXPG · GFXPG [9,14] · Q16 METR3904-G · Q18 METR3904-G · Q17 METR3904-G · R120 EV@10K/F_4 · C147 *EV@1000P/50V_4@NC · R107 EV@10K/F_4 · C139 *EV@1000P/50V_4@NC

1.4A

PQ15 DIS@AO6402A

PR113 DIS@22_8 · PR125 DIS@1M_4 · PR118 DIS@100K/F_4 · PQ28 DIS@ME2N7002E · PQ84A 2N7002DW · PQ84B 2N7002DW · PC59 DIS@10U/6.3V_6 · PC57 DIS@10U/6.3V_6 · PC58 *0.1U/10V_4 · PC56 *2200P/50V_4 · +3V_GPU [14,16,17,18] · +3V_NVMISC_EN [17,18] · [8,15,42] GFXON

3.9A

PQ41 DIS@AON7406

PC121 DIS@10U/6.3V_6 · PC127 DIS@10U/6.3V_6 · PC104 DIS@10U/6.3V_6 · PC105 DIS@10U/6.3V_6 · PC108 *330U/2.5V/9m_3828 · PC113 *DIS@0.1U/10V_4

PR116 DIS@22_8 · PR265 DIS@1M_4 · PR266 DIS@100K/F_4 · PQ32 DIS@ME2N7002E · PQ86A · PQ86B ME2N7002KW · PC109 *0.022U/25V_4 · [42] NVVDD_PG

PROJECT : LZ2A
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Size	Document Number	Rev
	GPU	
Date: Wednesday, November 30, 2011	Sheet 43 of 45	

LZ2 / Z480 Chief River Schematic EC Tracking Record B (for SDV --> SIV,B)OCT. 07, 2011

EC #	Page	CMVC #	Description	Date	Part Affected
B-00	15		To change D3 pin 2's connection from NVVDD_PG to GFXON for Deep_S3.	0921	
B-01	43		Add PR122 and D26 for +1.05V_GFX_PCIE discharge.	0921	
B-02	17		To change D5 pin1's connection from ACIN to AC_PRESENT for GPU Enable.	0922	
B-03	37		Change PR163 from 0R to 100K form Deep_S3	0922	
B-04	37		Add PD16 1SS355 for Deep_S3	0922	
B-05	32		Add Net EC_DRAMRST_GATE to connect U10's pin 106 and R614.	0925	
B-06	6		Add R615, Q55, Q56, D28 , D29 and Net DPWROK for Deep_S3.	0925	
B-07	10		Add Q57, Q58 and Net SLP_SUS# for Deep_S3.	0925	
B-08	32		Change U10 pin 76's net name from AB_CHARGING to SLP_SUS# for Deep_S3.	0925	
B-09	32		Change U10 pin 83's net name from RF_SW# to PCIE_WAKE#for Deep_S3.	0925	
B-10	32		Change U10 pin 100's connection from PCH to Net GFXON for Deep_S3.	1005	

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EC Tracking Record

LZ2 / Z480 Chief River Schematic EC Tracking Record C (for SDV --> SIV,C)Nov. 27, 2011

EC #	Page	CMVC #	Description	Date	Part Affected
C-00	24		Change LAN trandformer from dual mode to signal mode.	1126	
C-01	24		Change R295 and R296 to 0R.	1126	
C-02	24		Add D30,D31,D32,D33 for surge.	1126	
C-03	30		Net "CCD ON#" change connection from EC to PCH.	1120	
C-04	30		Change Bluetooth connection from USB PORT 5 to USB PORT 11 of PCH.	1118	
C-05	23		Add R635,636 fro brightness control.	1126	
C-06					
C-07					
C-08					
C-09					
C-10					

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EC Tracking Record