LV550 TGL-U Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

Properties

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

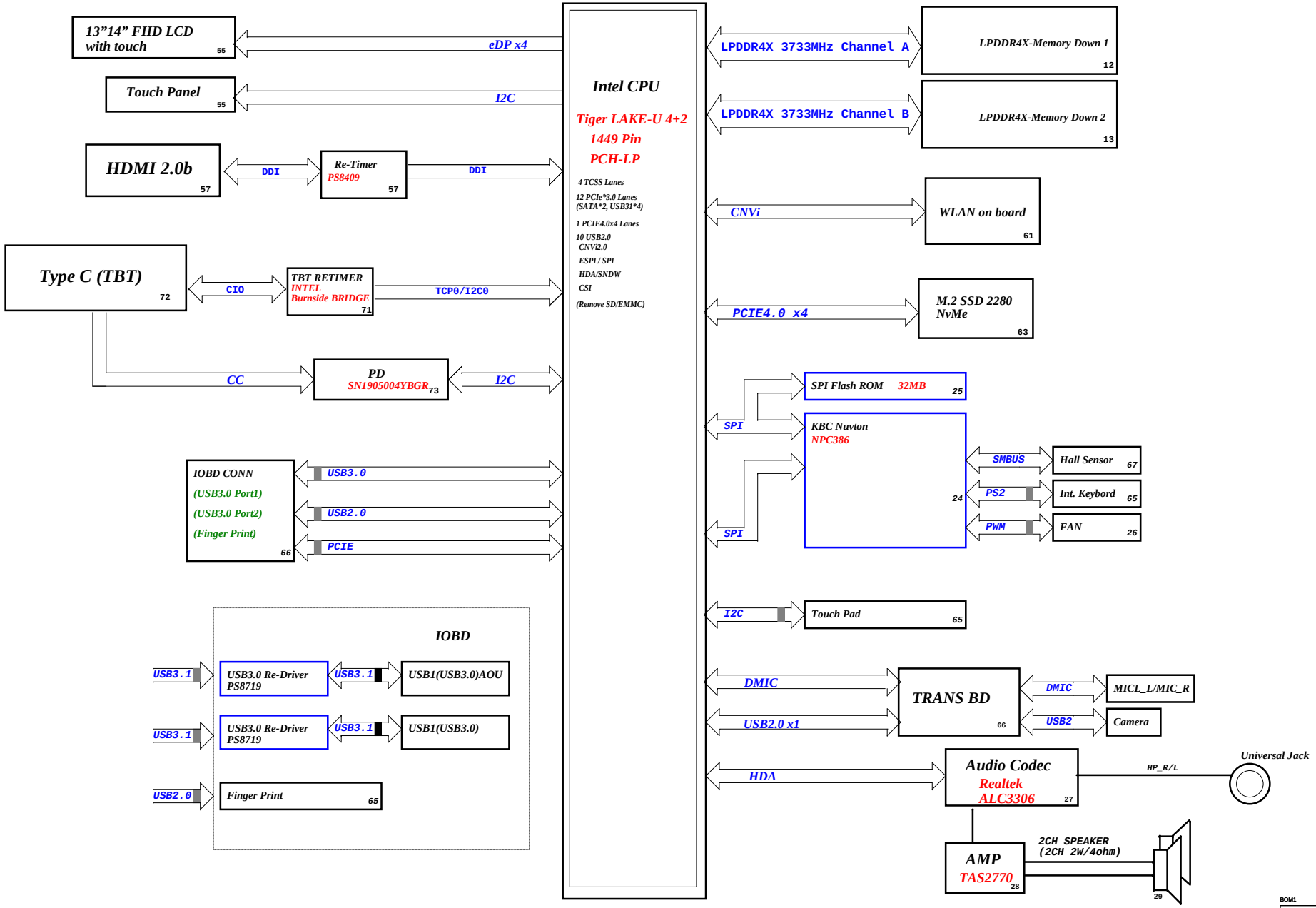
Title: **Cover Page**

Size: A3 | Document Number: **V550_TGL** | Rev: **-1**

Date: Monday, July 27, 2020 | Sheet 1 of 106

Project code: 13"-4PD0LX010001
14"-4PD0LY010001
PCB P/N: 19869
Revision:-1

LV550 TGL Block Diagram



PCB Layer Stackup

L1 : Signal
L2: GND\POWER
L3: Signal
L4: Signal
L5: GND\POWER
L6: Signal
L7: GND\POWER
L8: Signal
L9: GND
L8: Signal

Battery Charger/Selector BQ25710 44	
19V_AD_JK	19V_DCBATOUT BT+
System DC/DC TPS51395PRJER 45	
19V_DCBATOUT	5V_S5 5V_AUX_S5
System DC/DC TPS51393PRJER 45	
19V_DCBATOUT	3D3V_AUX_S5
CPU_VCORE RT3613EEGQW 46	
DC/DC VCCCPUCORE AOZ5516QI 47	
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCAUX RT6543AGQW 50	
19V_DCBATOUT	1D8V_VCCIN_AUX
DC/DC 1D1V_S3 TPS51487XRJER 51	
19V_DCBATOUT	1D1V_S3
DC/DC 0D6V_S3 TPS51487XRJER 51	
19V_DCBATOUT	0D6V_S3
DC/DC 1D8V_S3 TPS51487XRJER 51	
19V_DCBATOUT	1D8V_S3
DC/DC 1D8V_S5 RT5797ALGQW 53	
3D3V_S5	1D8V_S5
DC/DC 8V_AMP TPS54302DDCR 54	
19V_DCBATOUT	8V_AMP

BOM1

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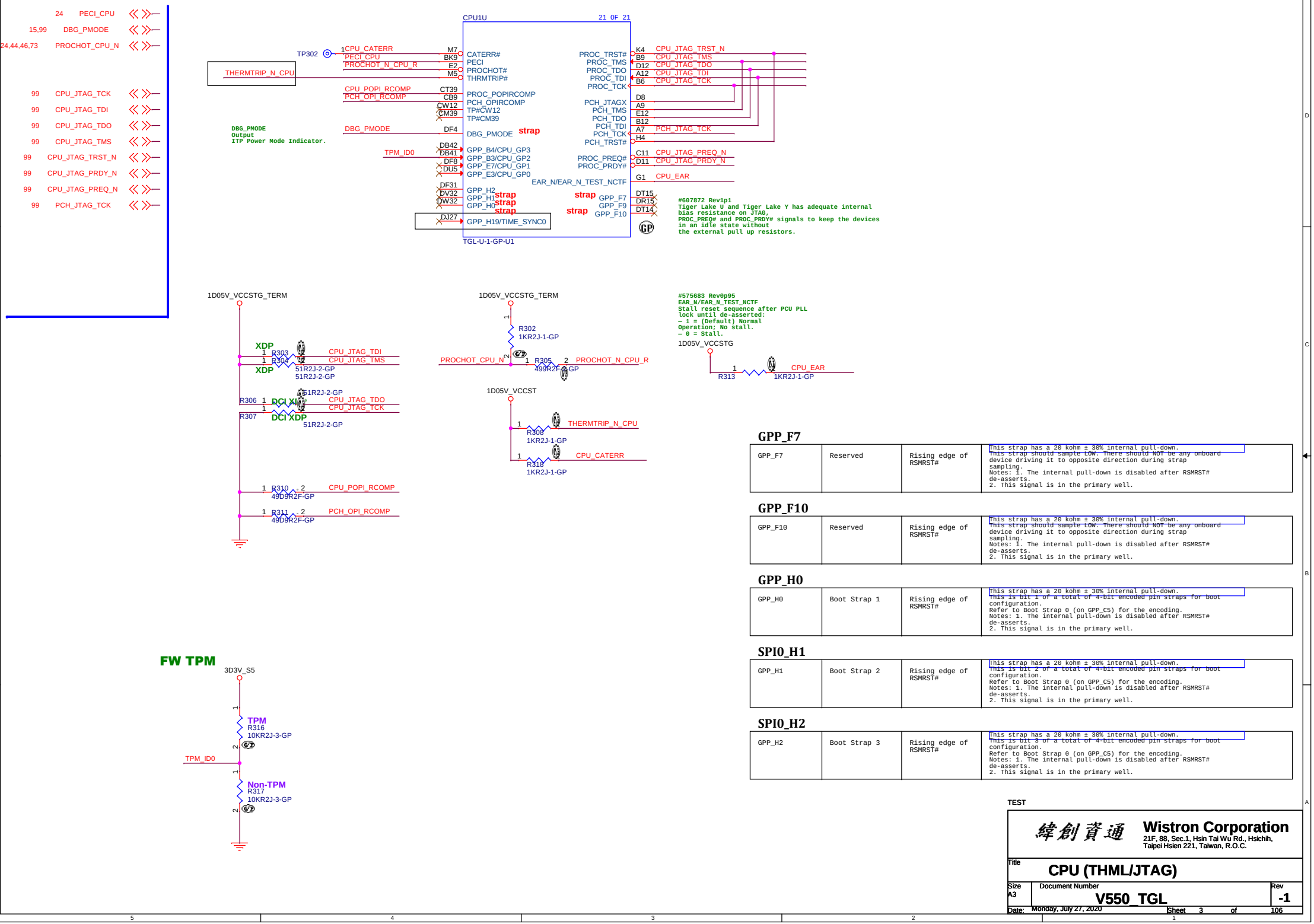
Title: Block Diagram

Size	Document Number	Rev
A2	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 2 of 106



GPP_F7

GPP_F7	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_F10

GPP_F10	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H0

GPP_H0	Boot Strap 1	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 1 of a total of 4-bit encoded pin straps for boot configuration. Refer to Boot Strap 0 (on GPP_C5) for the encoding. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SPI0_H1

GPP_H1	Boot Strap 2	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 2 of a total of 4-bit encoded pin straps for boot configuration. Refer to Boot Strap 0 (on GPP_C5) for the encoding. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SPI0_H2

GPP_H2	Boot Strap 3	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 3 of a total of 4-bit encoded pin straps for boot configuration. Refer to Boot Strap 0 (on GPP_C5) for the encoding. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

TEST

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Title: CPU (THML/JTAG)

Size: A3 | Document Number: V550_TGL | Rev: -1

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eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
24 eDP_BLEN_CPU
40,55 eDP_VDDEN_CPU
55 eDP_BLCTRL_CPU
55 eDP_HPD_CPU

TBT

71 TBT_TCSS_TX_P0
71 TBT_TCSS_TX_N0
71 TBT_TCSS_TX_P1
71 TBT_TCSS_TX_N1
71 TBT_TCSS_RX_P0
71 TBT_TCSS_RX_N0
71 TBT_TCSS_RX_P1
71 TBT_TCSS_RX_N1
71 TBT_TCSS_AUX_P
71 TBT_TCSS_AUX_N

71 TBT_LSX2_TXD
15,71 TBT_LSX2_RXD

HDMI

57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_HPD_CPU
57 HDMI_CLK_CPU
57 HDMI_DATA_CPU

Others

15 TBT_LSX1_VCC_CONFIG
15 TBT_LSX3_VCC_CONFIG

15 TBT_LSX1_RXD
73 USB_OC1_N

CPU1A — 1 OF 21

eDP_TX_CPU_P3 AC2 DDIA_TXP3
eDP_TX_CPU_N3 AC1 DDIA_TXN3
eDP_TX_CPU_P2 AD2 DDIA_TXP2
eDP_TX_CPU_N2 AD1 DDIA_TXN2
eDP_TX_CPU_P1 AF1 DDIA_TXP1
eDP_TX_CPU_N1 AF2 DDIA_TXN1
eDP_TX_CPU_P0 AG2 DDIA_TXP0
eDP_TX_CPU_N0 AG1 DDIA_TXN0

eDP_AUX_CPU_P AJ2 DDIA_AUX_P
eDP_AUX_CPU_N AJ1 DDIA_AUX_N

3D3V_S0 — 1 R401 2 2K2R2J-L1-GP — DDPA_DATA

DDPA_DATA DN4 DT6 GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA

eDP_HPD_CPU DR5 GPP_E14/DDSP_HPDA/DISP_MISCA

eDP_HPD_CPU 100K PD as LCD page.

HDMI_DDI_TX_P3 T12 DDIB_TXP3
HDMI_DDI_TX_N3 T11 DDIB_TXN3
HDMI_DDI_TX_P2 Y11 DDIB_TXP2
HDMI_DDI_TX_N2 Y9 DDIB_TXN2
HDMI_DDI_TX_P1 T9 DDIB_TXP1
HDMI_DDI_TX_N1 P9 DDIB_TXN1
HDMI_DDI_TX_P0 V11 DDIB_TXP0
HDMI_DDI_TX_N0 V9 DDIB_TXN0

AB9 DDIB_AUX_P
AD9 DDIB_AUX_N

HDMI_CLK_CPU DM29 GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
HDMI_DATA_CPU DK27 GPP_H17/DDPB_CTRLDATA

HDMI_DATA_CPU 2.2K PU as HDMI page.

HDMI_HPD_CPU DG43 GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

HDMI_HPD_CPU 100K PD as HDMI page.

DG47 GPP_A21/DDPC_CTRLCLK/I2S5_TXD
DJ47 GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT_LSX1_RXD DU8 DV8 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD — strap

TBT_LSX1_VCC_CONFIG DF6 DD6 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD — strap

TBT_LSX2_TXD DN23
TBT_LSX2_RXD DM23
GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK — strap

DK23
TBT_LSX3_VCC_CONFIG DN21
GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI — strap

3D3V_S5 — 1 R402 2 10KR2J-3-GP To PD — USB_OC1_N

DF43 GPP_A17/DISP_MISCC/I2S4_TXD
DF45 GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
DF47 GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

USB_OC1_N DH52 DK45 GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

eDP_VDDEN_CPU DM8 EDP_VDDEN
eDP_BLEN_CPU DN8 EDP_BKLTEN
eDP_BLCTRL_CPU DG10 EDP_BKLTCTL

TGL-U-1-GP-U1

TCP0_TXRX_P1 AY2
TCP0_TXRX_N1 AY1
TCP0_TXRX_P0 BB1
TCP0_TXRX_N0 BB2
TCP0_TX_P1 AM5
TCP0_TX_N1 AM7
TCP0_TX_P0 AT7
TCP0_TX_N0 AT5
TCP0_AUX_P AP7
TCP0_AUX_N AP5

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX_N AF5

TCP2_TXRX_P1 BF1 TBT_TCSS_RX_P1
TCP2_TXRX_N1 BF2 TBT_TCSS_RX_N1
TCP2_TXRX_P0 BE2 TBT_TCSS_RX_P0
TCP2_TXRX_N0 BE1 TBT_TCSS_RX_N0
TCP2_TX_P1 BD7 TBT_TCSS_TX_P1
TCP2_TX_N1 BD5 TBT_TCSS_TX_N1
TCP2_TX_P0 AY5 TBT_TCSS_TX_P0
TCP2_TX_N0 AY7 TBT_TCSS_TX_N0
TCP2_AUX_P BB5 TBT_TCSS_AUX_P
TCP2_AUX_N BB7 TBT_TCSS_AUX_N

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7

TC_RCOMP_P AN2 TCSS_RCOMP_P
TC_RCOMP_N AN1 TCSS_RCOMP_N — 1 R405 2 150R2F-4-L-GP

DSI_DE_TE_2 M8

DDI_RCOMP AB1 DISP_RCOMP — 2 R406 1 150R2F-1-GP

DISP_UTILS/DSI_DE_TE_1 CE4

DISP_UTILS
Output
embedded DisplayPort Utility: Output control signal used for brightness correction of embedded LCD displays with backlight modulation.

NOTE:
"eDP_HPD_CPU"
"eDP_VDDEN_CPU"
"eDP_BLEN_CPU"
PD 100K to LCD side

TEST

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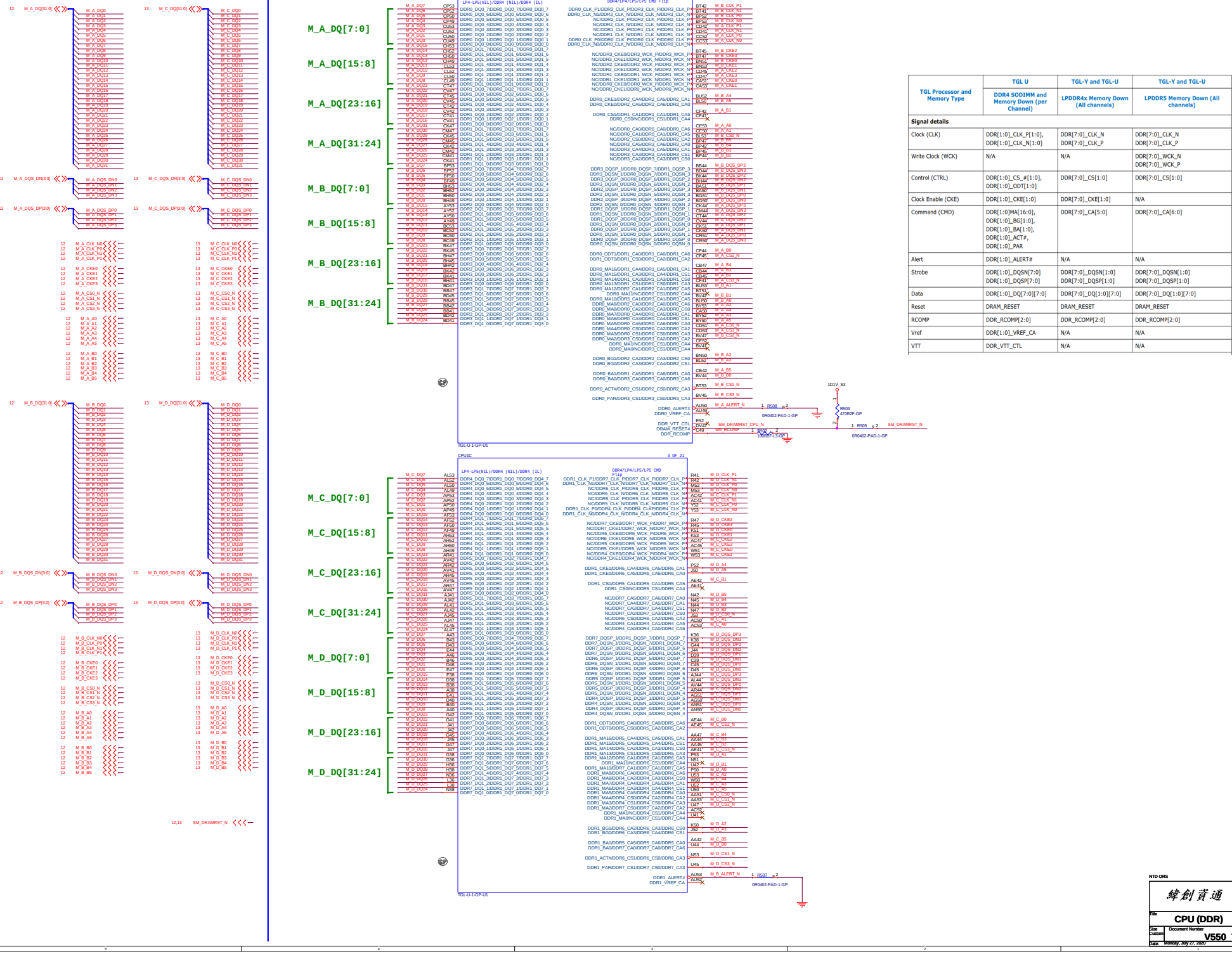
Title: CPU (DDI/EDP/TBT/TPC/)

Size	Document Number	Rev
A3	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 4 of 106



TGL Processor and Memory Type	TGL U DDR4 SODIMM and Memory Down (per Channel)	TGL-Y and TGL-U LPDDR4x Memory Down (All channels)	TGL-Y and TGL-U LPDDR5 Memory Down (All channels)
Signal details			
Clock (CLK)	DDR[1:0]_CLK_P[1:0], DDR[1:0]_CLK_N[1:0]	DDR[7:0]_CLK_N DDR[7:0]_CLK_P	DDR[7:0]_CLK_N DDR[7:0]_CLK_P
Write Clock (WCK)	N/A	N/A	DDR[7:0]_WCK_N DDR[7:0]_WCK_P
Control (CTRL)	DDR[1:0]_CS_#[1:0], DDR[1:0]_ODT[1:0]	DDR[7:0]_CS[1:0]	DDR[7:0]_CS[1:0]
Clock Enable (CKE)	DDR[1:0]_CKE[1:0]	DDR[7:0]_CKE[1:0]	N/A
Command (CMD)	DDR[1:0]MA[16:0], DDR[1:0]_BG[1:0], DDR[1:0]_BA[1:0], DDR[1:0]_ACT#, DDR[1:0]_PAR	DDR[7:0]_CA[5:0]	DDR[7:0]_CA[6:0]
Alert	DDR[1:0]_ALERT#	N/A	N/A
Strobe	DDR[1:0]_DQSN[7:0] DDR[1:0]_DQSP[7:0]	DDR[7:0]_DQSN[1:0] DDR[7:0]_DQSP[1:0]	DDR[7:0]_DQSN[1:0] DDR[7:0]_DQSP[1:0]
Data	DDR[1:0]_DQ[7:0][7:0]	DDR[7:0]_DQ[1:0][7:0]	DDR[7:0]_DQ[1:0][7:0]
Reset	DRAM_RESET	DRAM_RESET	DRAM_RESET
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]
Vref	DDR[1:0]_VREF_CA	N/A	N/A
VTT	DDR_VTT_CTL	N/A	N/A

NTD ORS

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Title: CPU (DDR)

Size	Document Number	Rev
Custom	V550 TGL	-1

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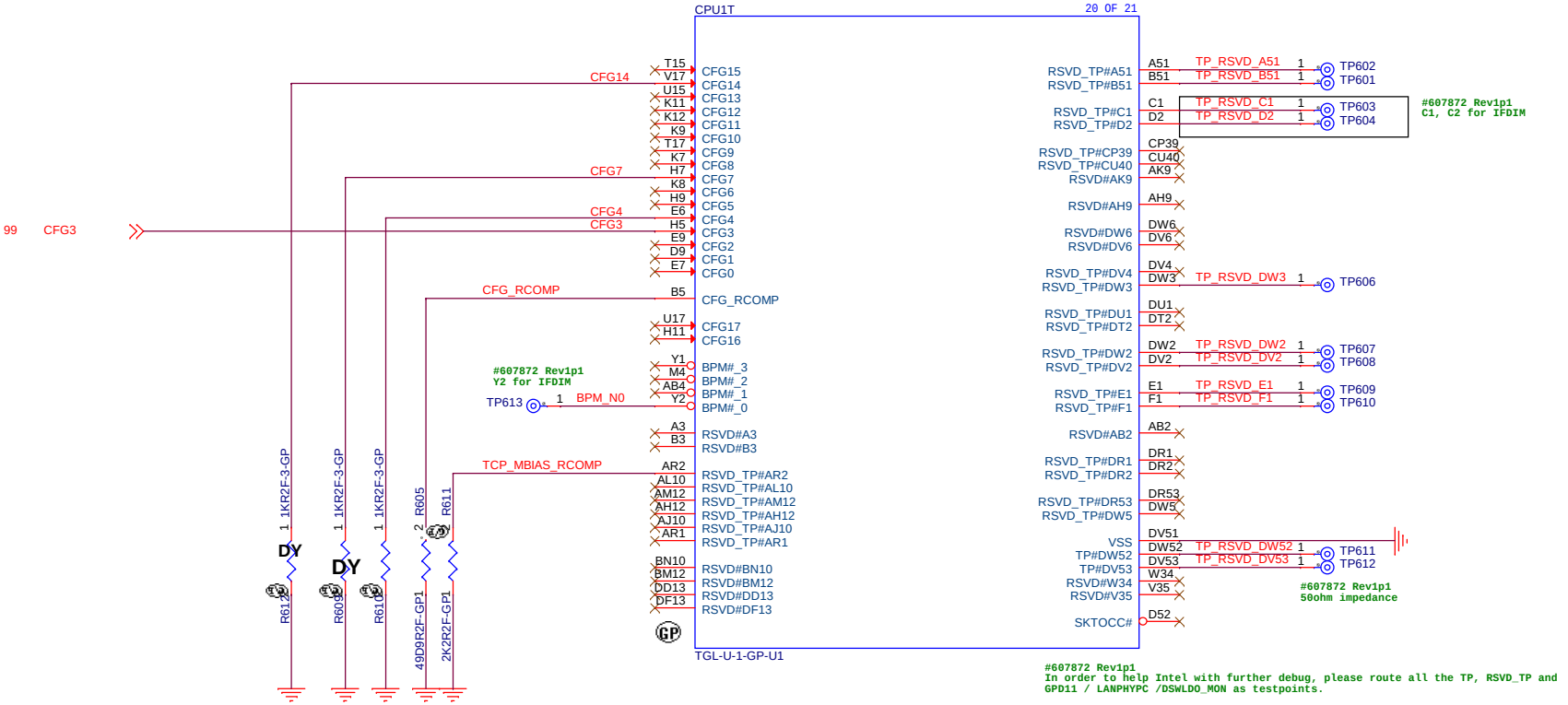
#575683 Rev0p95
CFG[17:0]
Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.
• CFG[3], CFG[0]: Reserved configuration lane.
• CFG[2]: TGL UP4/UP3 Reserved
• CFG[2]: TGL H PCI Express*
Static x16 Lanes Numbering Reversal.Reserved
• CFG[4]: eDP enable:
– 1 = Disabled.
– 0 = Enabled.
• CFG[6:5]: TGL UP4/UP3 Reserved
• CFG[6:5]: TGL H PCI Express* Bifurcation
– 00 = 1 x8, 2 x4 PCI Express*
– 01 = reserved
– 10 = 2 x8 PCI Express*
– 11 = 1 x16 PCI Express*
• CFG[7]: PEG Training:
– 1 = (default) PEG Train immediately following RESET# de assertion.
– 0 = PEG Wait for BIOS for training.
• CFG[13:8]: Reserved configuration lanes.
• CFG[14]: PEG60 (PCIE4) Lane Reversal:
– 1 - (Default) Normal
– 0 - Reversed
• CFG[17:15]: Reserved configuration lanes.



TEST

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Title: CPU (CFG/IST)		
Size: B	Document Number: V550_TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 6 of 106	

46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_ALERT_CPU_N
46 SVID_CLK_CPU
46 SVID_DATA_CPU

VCCIN
Input
Input FIVR, Processor IA Cores and Graphics Power Rail.

1V_CPU_CORE
(55A)

CPU1M
13 0F 21

A24	VCCIN	VCCIN	G32
A26	VCCIN	VCCIN	H24
A29	VCCIN	VCCIN	H26
A30	VCCIN	VCCIN	H30
A33	VCCIN	VCCIN	H32
A35	VCCIN	VCCIN	J1
AY39	VCCIN	VCCIN	J2
B24	VCCIN	VCCIN	K1
B26	VCCIN	VCCIN	K2
B29	VCCIN	VCCIN	K24
B30	VCCIN	VCCIN	K26
B33	VCCIN	VCCIN	K30
B35	VCCIN	VCCIN	K32
BA10	VCCIN	VCCIN	L24
BA40	VCCIN	VCCIN	L26
BB39	VCCIN	VCCIN	L30
BB9	VCCIN	VCCIN	L32
BC10	VCCIN	VCCIN	N24
BC40	VCCIN	VCCIN	N26
BD39	VCCIN	VCCIN	N30
BD9	VCCIN	VCCIN	N32
BE10	VCCIN	VCCIN	P24
BE40	VCCIN	VCCIN	P26
BF9	VCCIN	VCCIN	P28
BG10	VCCIN	VCCIN	P30
BG40	VCCIN	VCCIN	P32
BH12	VCCIN	VCCIN	T21
BH39	VCCIN	VCCIN	T23
BH9	VCCIN	VCCIN	T25
BJ10	VCCIN	VCCIN	T27
BJ40	VCCIN	VCCIN	T31
BK39	VCCIN	VCCIN	U23
BL10	VCCIN	VCCIN	U27
BL40	VCCIN	VCCIN	U29
BM39	VCCIN	VCCIN	U31
BN40	VCCIN	VCCIN	U33
BP12	VCCIN	VCCIN	V23
BP39	VCCIN	VCCIN	V25
BR10	VCCIN	VCCIN	V27
BR40	VCCIN	VCCIN	V29
BT12	VCCIN	VCCIN	V31
BT39	VCCIN	VCCIN	V33
BU10	VCCIN	VCCIN	W22
BU40	VCCIN	VCCIN	W24
BV12	VCCIN	VCCIN	W28
BY12	VCCIN	VCCIN	W32
CA10	VCCIN	VCCIN	
CB12	VCCIN	R38	VCCCORE_SENSE
D24	VCCIN	VCCIN_SENSE	
D26	VCCIN	R37	VSSCORE_SENSE
D29	VCCIN	VSSIN_SENSE	
D30	VCCIN	M12	SVID_DATA_CPU
D33	VCCIN	VIDSOUT	
D35	VCCIN	M11	SVID_CLK_CPU
E24	VCCIN	VIDSCK	
E26	VCCIN	P12	SVID_ALERT_N_CPU_R
E27	VCCIN	VIDALERT#	
E29	VCCIN		
E30	VCCIN		
E32	VCCIN		
E33	VCCIN		
G2	VCCIN		
G24	VCCIN		
G26	VCCIN		
G30	VCCIN		

TGL-U-1-GP-U1

1V_CPU_CORE

SVID DATA

1D05V_VCCST
R701 100R2F-L1-GP-U
SVID_DATA_CPU

SVID ALERT

1D05V_VCCST
R702 56R2J-4-GP
SVID_ALERT_CPU_N
R703 0R0402-PAD-1-GP
SVID_ALERT_N_CPU_R

Layout note:
3.Length matchin 25mil, and close SOC in 2inch "

1V_CPU_CORE
R704 100R2F-L1-GP-U
VCCCORE_SENSE
R705 100R2F-L1-GP-U
VSSCORE_SENSE

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

TEST

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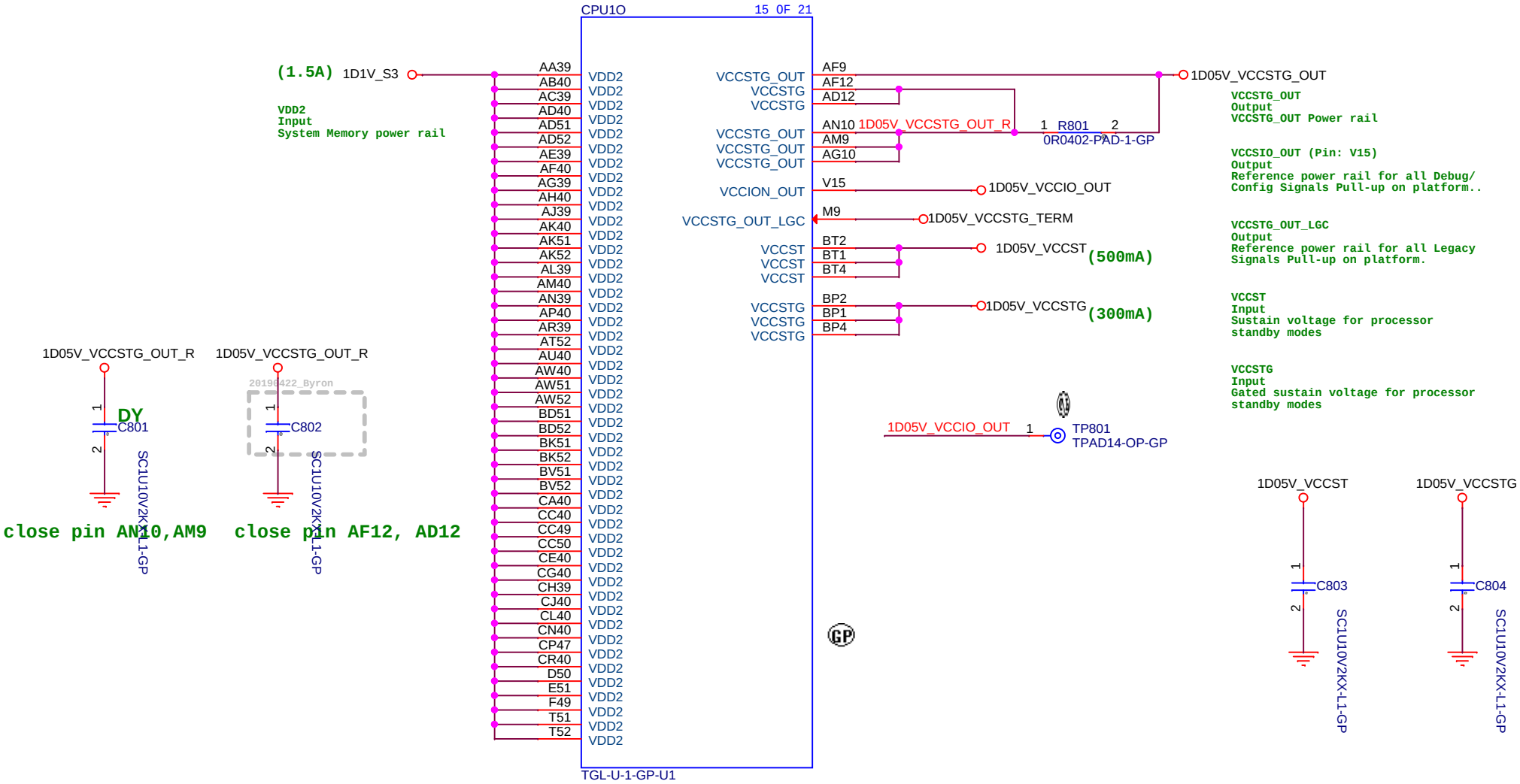
Title: **CPU (VCCIN/VID)**

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 7 of 106



Lack of VCCPLL_OC / VCC1P8A / VCCPLL

TEST

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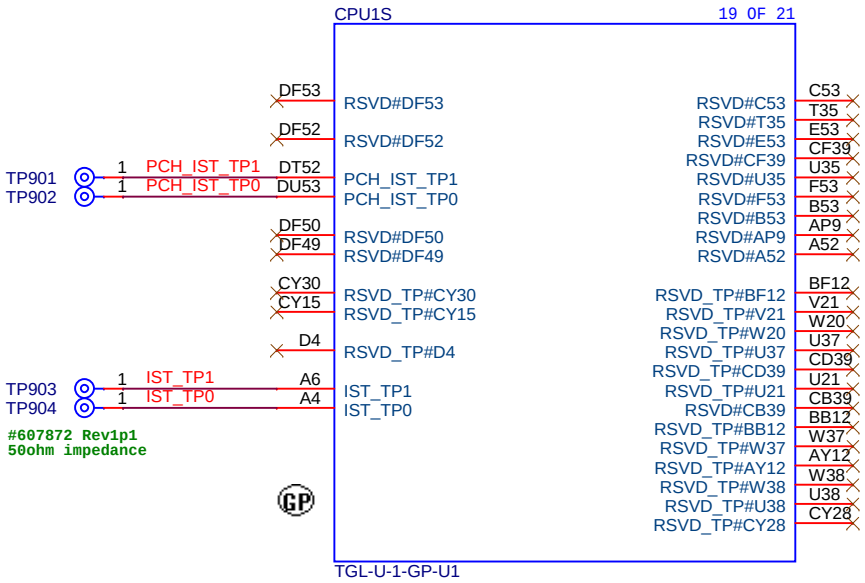
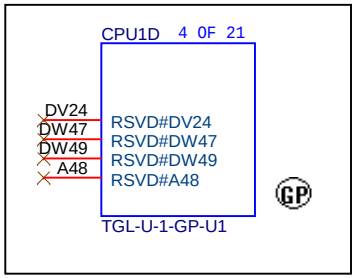
Title: CPU (VDDQ/VCC/VCCST)		
Size: A4	Document Number: V550_TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 8 of 106	





#607872 Rev1p1
Impedance Spectrum Tool (IST/IFDIM) Testing
Requirements and Recommendations

NOTE
IST/IFDIM is not directly available to customers, Intel will need these trigger points to support debug of customer issues at Intel validation labs. Intel recommends customers implement the IST tool requirements from this section.

TEST

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Title: CPU (RSVD)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 9 of 106

Main Func = CPU

VCORE

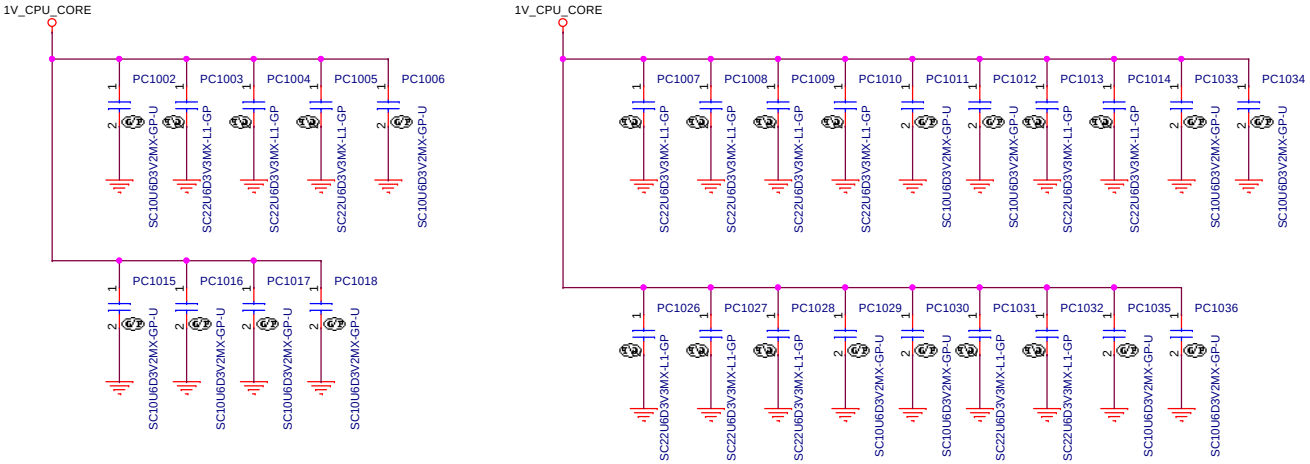
ICL_U42/TGL_U42_28W

U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	15	330uF*1

#607872 Rev1p1
Power Map
UP3 4+2 28W VCCIN Max: 65A
UP3 4+2 15W VCCIN Max: 55A

PDG
0402 10UF 12PCS (Secondary side)
7343 220UF 2PCS
0606 22UF 8PCS



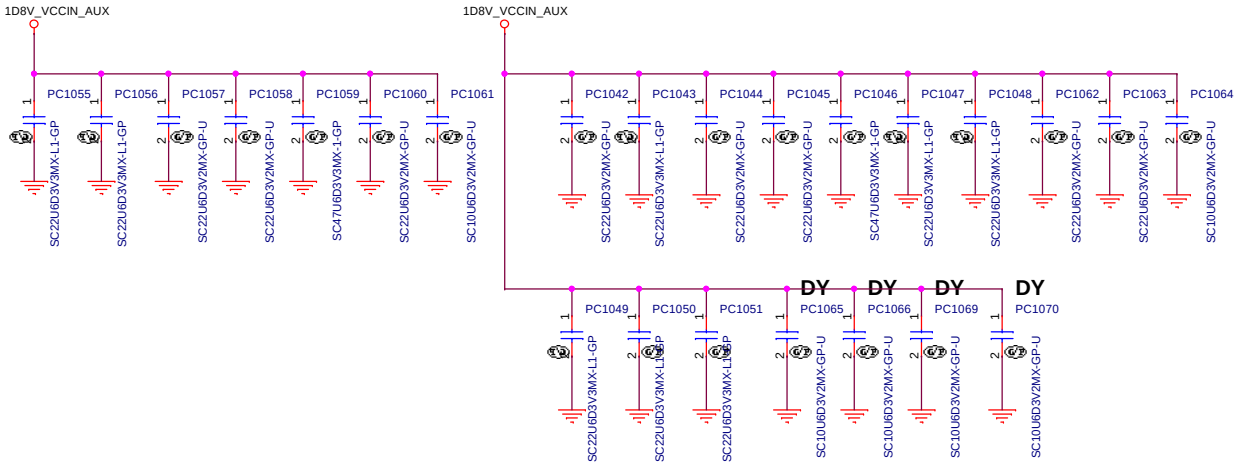
VCCINAUX

MP2941

22uF	PCS	Cap
U42	9	330uF*1

#607872 Rev1p1
PDG VCCINAUX
7343 220UF 1PCS
0805 47UF 3PCS
0603 22UF 12PCS
0402 10UF 15PCS

0402 10UF 10PCS (Secondary side)



STD

緯創資通 Wistron Corporation
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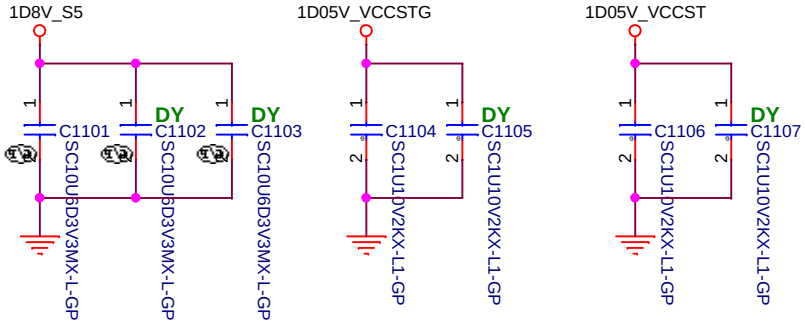
Taipei Hsien 221, Taiwan, R.O.C.

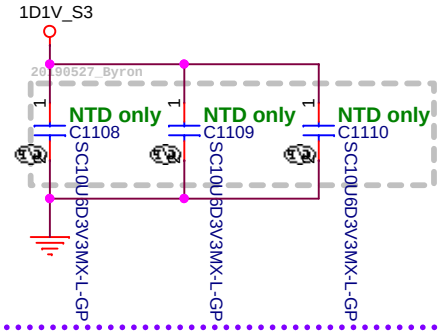
Title	CPU_(Power CAP1)	
Size A3	Document Number V550_TGL	Rev -1
Date: Monday, July 27, 2020	Sheet 10 of 106	



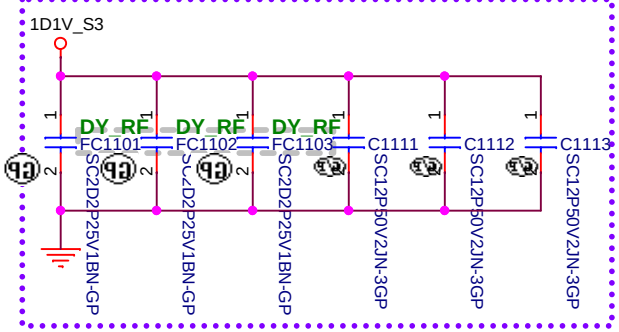
#607872 Rev1p1
PDG VCCST
0402 1UF 2PCS

#607872 Rev1p1
PDG VCCSTG
0402 1UF 2PCS

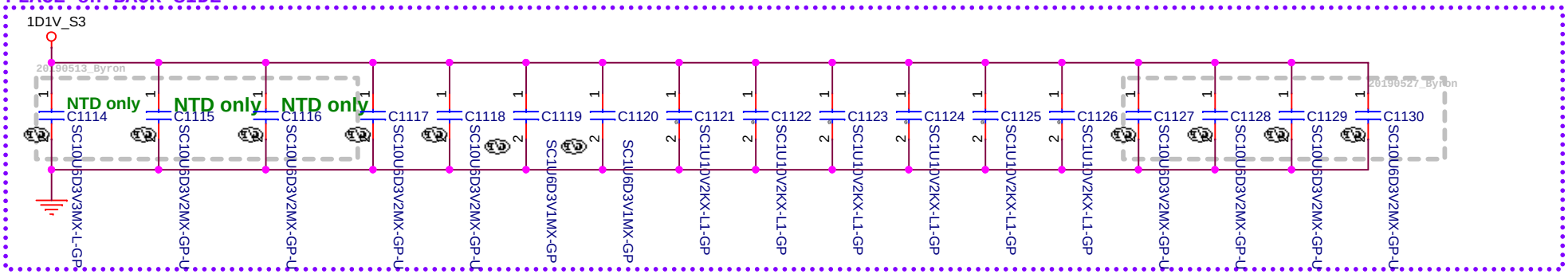
PLACE on CPU Same Side



EMC CAPS - PLACE <4mm FROM SOC VDDQ, WITH EACH PAIR <12mm APART



PLACE on BACK SIDE



#607872 Rev1p1
PDG VDD2
0603 47UF 2PCS
0402 1UF 8PCS

0402 10UF 8PCS (Secondary side)

TEST

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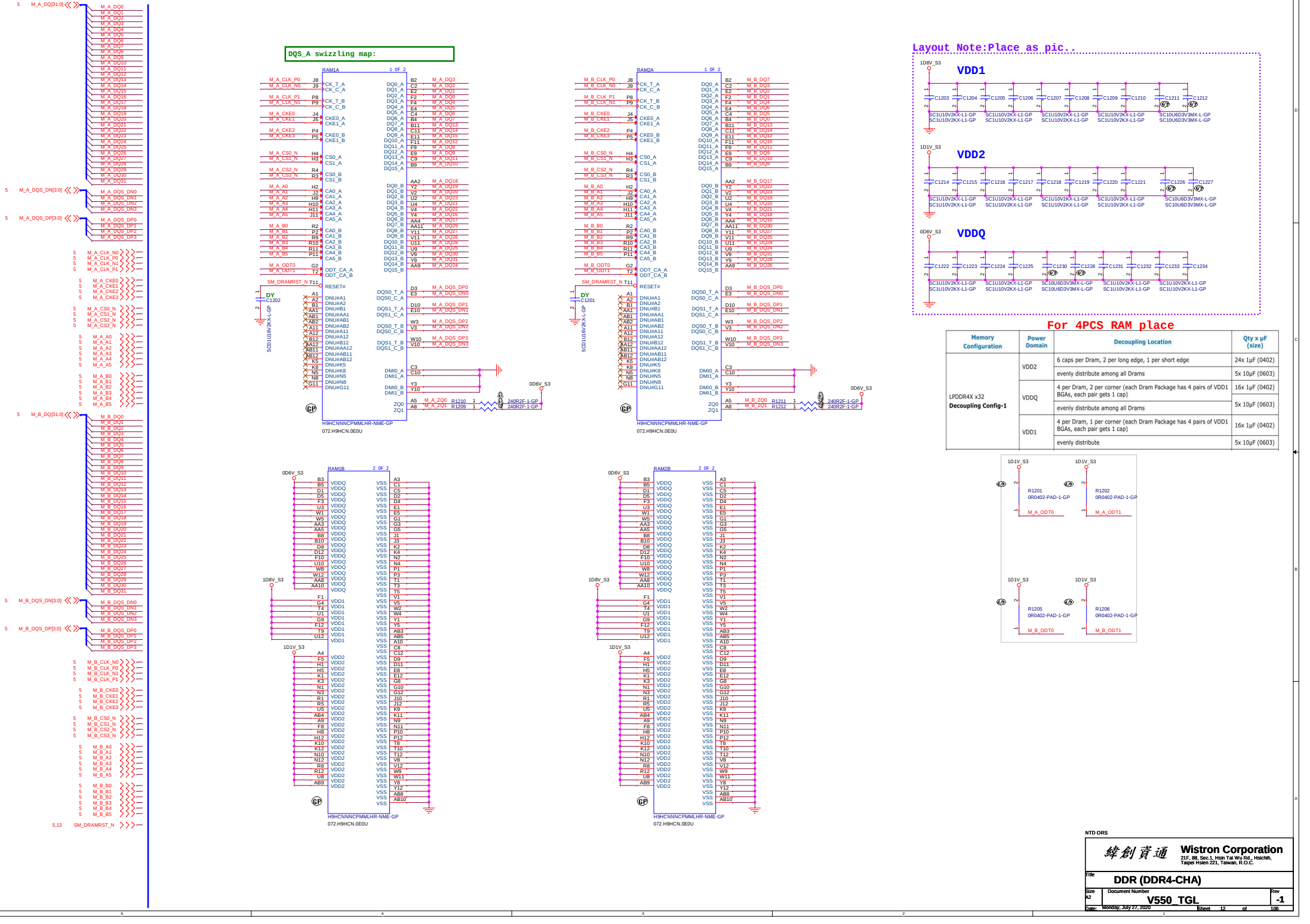
Title	CPU (Power Cap2)	
Size A4	Document Number V550_TGL	Rev -1
Date: Monday, July 27, 2020	Sheet 11 of 106	



Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

NTD ORS

緯創資通 **Wistron Corporation**
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Title: **DDR (DDR4-CHA)**

Size	Document Number	Rev
A2	V550_TGL	-1

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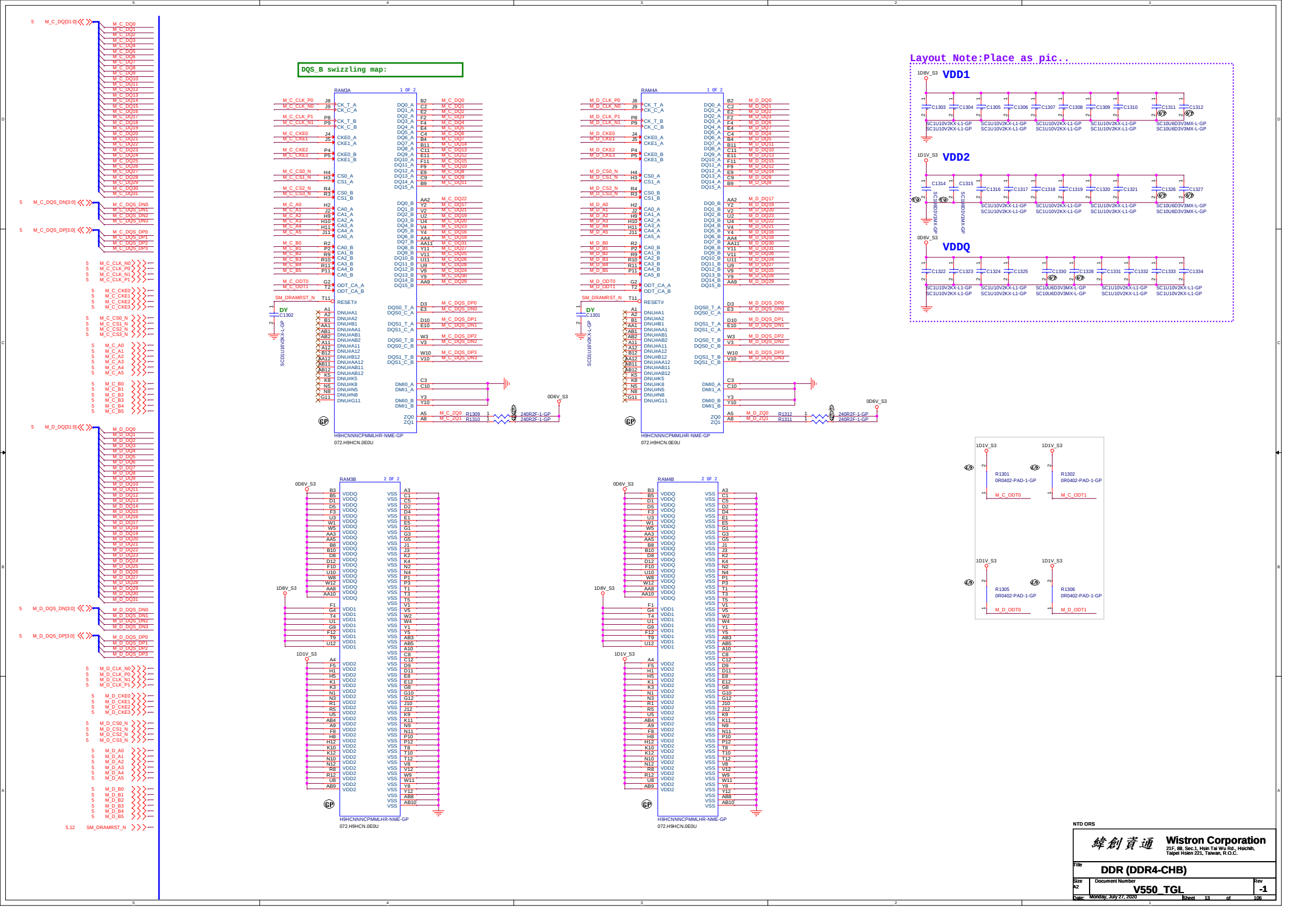
DQS_B swizzling map:
Layout Note:Place as pic..
VDD1
VDD2
VDDQ
RAM3A
RAM4A
RAM3B
RAM4B
H9HCNNNCPMMLHR-NME-GP
072.H9HCN.0E0U
M_C_DQ[31:0]
M_D_DQ[31:0]
M_C_DQS_DN[3:0]
M_C_DQS_DP[3:0]
M_D_DQS_DN[3:0]
M_D_DQS_DP[3:0]
SM_DRAMRST_N
M_C_ODT0
M_C_ODT1
M_D_ODT0
M_D_ODT1
NTD ORS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR (DDR4-CHB)
V550_TGL
-1
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106

BLANK

TEST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DDR (RSVD) (DDR4-CHA1)**
Size: A4	Document Number: **V550_TGL**
Rev: **-1**	
Date: Monday, July 27, 2020	Sheet 14 of 106

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
		Move to Page 25			Move to Page 25		
GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10 / GPP_E11
Schematic	E19	E21		D12	Move to Page 25		1D8V_S5 R1518 20KR2J-L3-GP GPP_E10; 1D8V_S5 R1519 20KR2J-L3-GP GPP_E11

Why GPP_E10, GPP_E11 need PU?

GPP_C5

GPP_C5 / SML0ALERT#	Boot Strap 0	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration. This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively). 4-bit boot strap configuration encodings: 0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is enabled 0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled 0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI 1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device). 1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI. Others: Reserved Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1501 4K7R2J-L-GP — GPP_C5_SML0ALERT_N

GPP_D10

GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / GSPI2_CLK	DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 1.8V 1 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 3.3V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1520 4K7R2J-L-GP — TBT_LSX2_RXD

GPP_D12

GPP_D12 / ISH_SPI_MOSI / DDP4_CTRLDATA / CAS_SPIM_MOSI / TBT_LSX3_RXD	DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V 1 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 3.3 Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1515 4K7R2J-L-GP — TBT_LSX3_VCC_CONFIG

GPP_R2

GPP_R2 / HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This strap has a 20 kohm ± 30% internal pull-down. 0=> Enable security measures defined in the Flash Descriptor. (Default) 1=> Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

ME_UNLOCK — R1511 1KR2J-1-GP — HDA_SDOUT_CPU
EC control.

GPP_F2

GPP_F2 / CNV_RGI_DT / UART0_TXD	M.2 CNVi Mode Select	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=>Integrated CNVi enabled. 1=>Integrated CNVi disabled Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

1D8V_S5 — R1505 100KR2J-1-GP — CNV_RGI_DT

GPP_E6

GPP_E6	JTAG ODT Disable	Rising edge of RSMRST#	This strap does not have an internal pull-up or pull-down. External pull-up is recommended 0=> JTAG ODT is disabled 1=> JTAG ODT is enabled

1D8V_S5 — R1503 100KR2J-1-GP — GPP_E6_JTAG_ODT; DY R1509 4K7R2J-L-GP

GPP_E19

GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD	DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V 1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1513 4K7R2J-L-GP — TBT_LSX1_RXD

GPP_E21

GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD	DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins VCC configuration	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 1.8V 1 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 3.3V Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5 — DY R1514 4K7R2J-L-GP — TBT_LSX1_VCC_CONFIG

DBG_PMODE

DBG_PMODE	Reserved	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-up. This strap should sample high. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

1D05V_S5_OUT — XDP R1517 1KR2J-1-GP — DBG_PMODE

TEST

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
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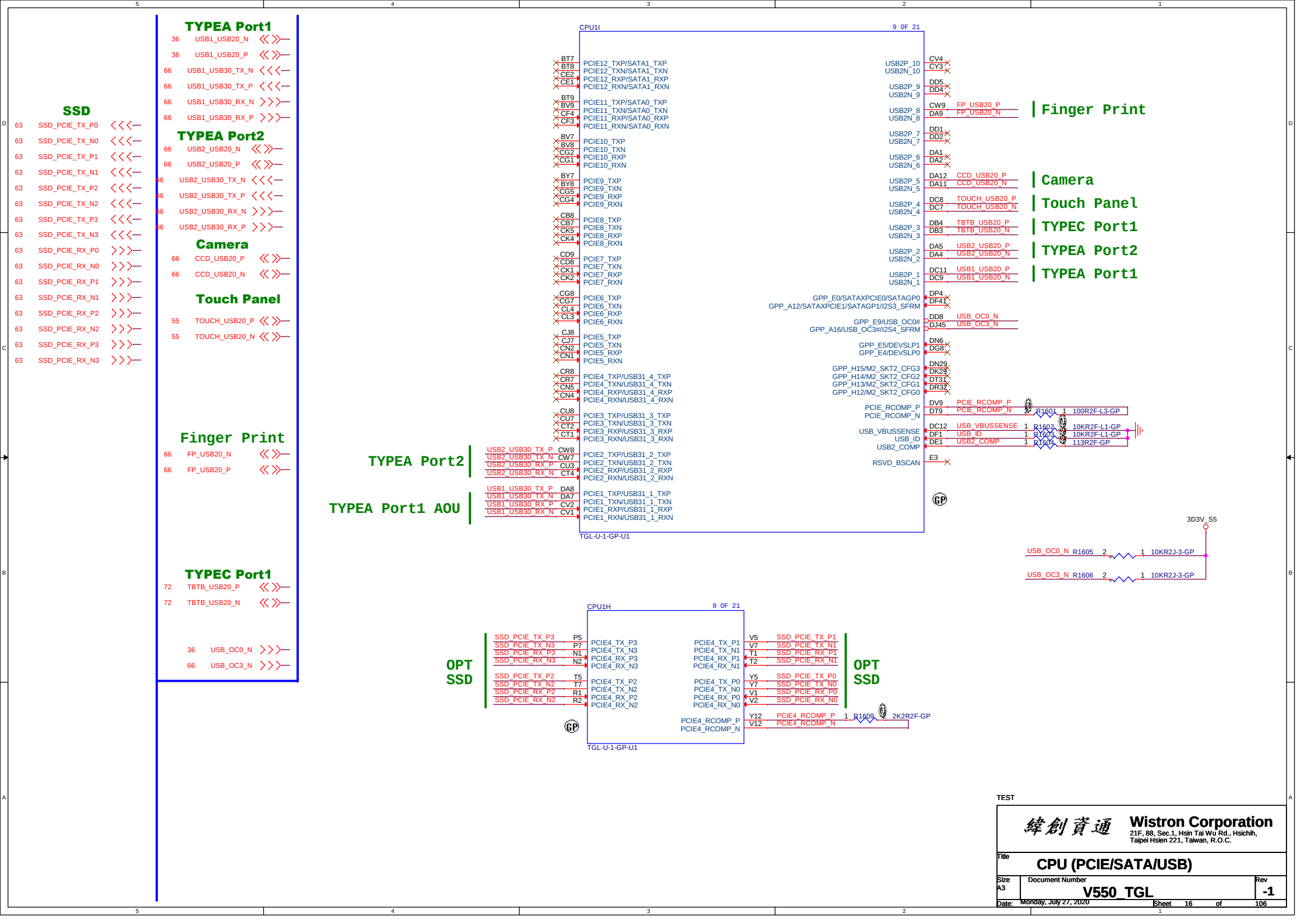
SSD
63 SSD_PCIE_TX_P0
63 SSD_PCIE_TX_N0
63 SSD_PCIE_TX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_RX_P0
63 SSD_PCIE_RX_N0
63 SSD_PCIE_RX_P1
63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P2
63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P3
63 SSD_PCIE_RX_N3
TYPEA Port1
36 USB1_USB20_N
36 USB1_USB20_P
66 USB1_USB30_TX_N
66 USB1_USB30_TX_P
66 USB1_USB30_RX_N
66 USB1_USB30_RX_P
TYPEA Port2
66 USB2_USB20_N
66 USB2_USB20_P
66 USB2_USB30_TX_N
66 USB2_USB30_TX_P
66 USB2_USB30_RX_N
66 USB2_USB30_RX_P
Camera
66 CCD_USB20_P
66 CCD_USB20_N
Touch Panel
55 TOUCH_USB20_P
55 TOUCH_USB20_N
Finger Print
66 FP_USB20_N
66 FP_USB20_P
TYPEC Port1
72 TBTB_USB20_P
72 TBTB_USB20_N
36 USB_OC0_N
66 USB_OC3_N
CPU1I
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PCIE12_TXP/SATA1_TXP
PCIE12_TXN/SATA1_TXN
PCIE12_RXP/SATA1_RXP
PCIE12_RXN/SATA1_RXN
PCIE11_TXP/SATA0_TXP
PCIE11_TXN/SATA0_TXN
PCIE11_RXP/SATA0_RXP
PCIE11_RXN/SATA0_RXN
PCIE10_TXP
PCIE10_TXN
PCIE10_RXP
PCIE10_RXN
PCIE9_TXP
PCIE9_TXN
PCIE9_RXP
PCIE9_RXN
PCIE8_TXP
PCIE8_TXN
PCIE8_RXP
PCIE8_RXN
PCIE7_TXP
PCIE7_TXN
PCIE7_RXP
PCIE7_RXN
PCIE6_TXP
PCIE6_TXN
PCIE6_RXP
PCIE6_RXN
PCIE5_TXP
PCIE5_TXN
PCIE5_RXP
PCIE5_RXN
PCIE4_TXP/USB31_4_TXP
PCIE4_TXN/USB31_4_TXN
PCIE4_RXP/USB31_4_RXP
PCIE4_RXN/USB31_4_RXN
PCIE3_TXP/USB31_3_TXP
PCIE3_TXN/USB31_3_TXN
PCIE3_RXP/USB31_3_RXP
PCIE3_RXN/USB31_3_RXN
PCIE2_TXP/USB31_2_TXP
PCIE2_TXN/USB31_2_TXN
PCIE2_RXP/USB31_2_RXP
PCIE2_RXN/USB31_2_RXN
PCIE1_TXP/USB31_1_TXP
PCIE1_TXN/USB31_1_TXN
PCIE1_RXP/USB31_1_RXP
PCIE1_RXN/USB31_1_RXN
USB2P_10
USB2N_10
USB2P_9
USB2N_9
USB2P_8
USB2N_8
USB2P_7
USB2N_7
USB2P_6
USB2N_6
USB2P_5
USB2N_5
USB2P_4
USB2N_4
USB2P_3
USB2N_3
USB2P_2
USB2N_2
USB2P_1
USB2N_1
GPP_E0/SATAXPCIE0/SATAGP0
GPP_A12/SATAXPCIE1/SATAGP1/I2S3_SFRM
GPP_E9/USB_OC0#
GPP_A16/USB_OC3#/I2S4_SFRM
GPP_E5/DEVSLP1
GPP_E4/DEVSLP0
GPP_H15/M2_SKT2_CFG3
GPP_H14/M2_SKT2_CFG2
GPP_H13/M2_SKT2_CFG1
GPP_H12/M2_SKT2_CFG0
PCIE_RCOMP_P
PCIE_RCOMP_N
USB_VBUSSENSE
USB_ID
USB2_COMP
RSVD_BSCAN
FP_USB20_P
FP_USB20_N
CCD_USB20_P
CCD_USB20_N
TOUCH_USB20_P
TOUCH_USB20_N
TBTB_USB20_P
TBTB_USB20_N
USB2_USB20_P
USB2_USB20_N
USB1_USB20_P
USB1_USB20_N
USB_OC0_N
USB_OC3_N
R1601 100R2F-L3-GP
R1602 10KR2F-L1-GP
R1603 10KR2F-L1-GP
R1604 113R2F-GP
Finger Print
Camera
Touch Panel
TYPEC Port1
TYPEA Port2
TYPEA Port1
TGL-U-1-GP-U1
TYPEA Port2
USB2_USB30_TX_P
USB2_USB30_TX_N
USB2_USB30_RX_P
USB2_USB30_RX_N
TYPEA Port1 AOU
USB1_USB30_TX_P
USB1_USB30_TX_N
USB1_USB30_RX_P
USB1_USB30_RX_N
3D3V_S5
USB_OC0_N R1605 10KR2J-3-GP
USB_OC3_N R1606 10KR2J-3-GP
CPU1H
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SSD_PCIE_TX_P3
SSD_PCIE_TX_N3
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
SSD_PCIE_TX_P2
SSD_PCIE_TX_N2
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
PCIE4_TX_P3
PCIE4_TX_N3
PCIE4_RX_P3
PCIE4_RX_N3
PCIE4_TX_P2
PCIE4_TX_N2
PCIE4_RX_P2
PCIE4_RX_N2
PCIE4_TX_P1
PCIE4_TX_N1
PCIE4_RX_P1
PCIE4_RX_N1
PCIE4_TX_P0
PCIE4_TX_N0
PCIE4_RX_P0
PCIE4_RX_N0
PCIE4_RCOMP_P
PCIE4_RCOMP_N
R1609 2K2R2F-GP
OPT SSD
OPT SSD
TGL-U-1-GP-U1
TEST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PCIE/SATA/USB)
Size A3
Document Number
V550_TGL
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Date: Monday, July 27, 2020
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24,63,91 PLTRST_CPU_N
24,40 PM_SLP_SUS_N
24,40,54,57 PM_SLP_S3_N
24,40 PM_SLP_S4_N
24 PM_PWRBTN_N
24,40 ALL_SYS_PWRGD
99 SYS_RESET_N
50 VCCIN_AUX_PWRGD
24,99 RSMRST_N_KBC
24 DSW_PWROK
40 PCH_PWROK
24 S0_PWRGD
24 AC_PRESENT
40 VCCST_OVERRIDE
71 RT_PERST_N
40 CPU_C10_GATE_N
73 PMC_ALERT_CPU_N

CPU1L
12 OF 21
TGL-U-1-GP-U1

PM_SLP_SUS_N DV49 SLP_SUS#
PM_SLP_S4_N DJ41 GPD10/SLP_S5#
PM_SLP_S3_N DJ43 GPD5/SLP_S4#
DM43 GPD4/SLP_S3#
DR41 GPD6/SLP_A#
DT44 GPD9/SPL_WLAN#
TP1904 TPAD14-OP-GP
TP1703 TPAD14-OP-GP
PM_SLP_S0_N DD42 GPP_B12/SLP_S0#
DN39 SLP_LAN#
PM_RSMRST_N DM35 RSMRST#
SYS_RESET_N DD10 SYS_RESET#
PLTRST_CPU_N DD41 GPP_B13/PLTRST#
R1701 0R0402-PAD-1-GP
S0_PWRGD
PCH_PWROK
R1704 0R0402-PAD-1-GP
DSW_PWROK_R DK35 DSW_PWROK
SYS_PWROK DF10 SYS_PWROK
PCH_PWROK_R DN35 PCH_PWROK
RTC_INTRUDER_N DM37 INTRUDER#
SPI_VCC_SEL DT49 SPIVCCIOSEL
strap

PROCPWRGD BM9
GPD3/PWRBTN# DK41 PM_PWRBTN_N
GPD0/BATLOW# DN41 PM_BATLOW_N
GPD1/ACPRESENT DK43 AC_PRESENT
GPP_B11/PMCALERT# CW40 PMC_ALERT_CPU_N
GPP_H18/CPU_C10_GATE# DN27 CPU_C10_GATE_N
GPP_H3/SX_EXIT_HOLDOFF# DG31
WAKE# DK39 PCIE_WAKE_N
GPD2/LAN_WAKE# DM41 LAN_WAKE_N
GPD11/LANPHYPC/DSWLDO_MON DT41 TP_GPG11
TP1702
strap GPD7 DN43 RT_PERST_N_GPD7
VCCSTPWRGOOD_TCSS CE5 VCCSTPWRGOOD_TCSS
VCCST_PWRGD BP8 VCCST_PWRGD_R
VCCST_OVERRIDE BP9 VCCST_OVERRIDE_R
GPP_F20/EXT_PWR_GATE# DR12
GPP_F21/EXT_PWR_GATE2# DW12

3D3V_S5
R1734 10KR2J-3-GP
R1703 0R0402-PAD-1-GP VCCST_OVERRIDE
R1705 0R0402-PAD-1-GP VCCST_OVERRIDE

VCCST_OVERRIDE
VccST Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability.

3D3V_S0
R1706 10KR2J-3-GP SYS_RESET_N

3D3V_S5
R1737 10KR1J-GP LAN_WAKE_N
R1710 10KR2J-3-GP PM_BATLOW_N
R1709 1KR2J-1-GP PCIE_WAKE_N
R1715 100KR2J-1-GP VCCST_OVERRIDE
R1717 100KR2J-1-GP PCH_PWROK_R
R1720 100KR2J-1-GP SYS_PWROK

ALL_SYS_PWRGD
R1726 100KR2J-1-GP
VCCST_PWRGD_R
R1727 47KR2F-GP
C1702 SCD1U16V2KX-1-GP
DY

SPI SELECT STRAP
Cap LOW → 3.3V
Cap DY → 1.8V

SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V

3D3V_RTC_AUX
R1707 1MR2F-GP
RTC_INTRUDER_N
C1701 SCD1U16V2KX-1-GP
R1711 1MR2F-GP
DY
SPI_VCC_SEL
R1712 4K7R2J-L-GP

PLTRST_CPU_N R1735 0R0402-PAD-1-GP
RT_PERST_N_GPD7 R1736 0R2J-L-GP RT_PERST_N
DY

From EC Control
DSW_PWROK_R R1723 0R0402-PAD-1-GP DSW_PWROK
R1724 100KR2J-1-GP
Delay 3D3V_S5 over 10ms.

Q1701 LSK3541G1ET2L-1-GP
084.03541.M001
S D PM_RSMRST_N R1721 1KR2J-1-GP RSMRST_N_KBC
R1725 100KR2J-1-GP
G
3D3V_S5
R1718 100KR2J-1-GP
3D3V_S5
3V_5V_POK_C R1722 0R0402-PAD-1-GP VCCIN_AUX_PWRGD
G
R1719 10KR2J-3-GP
3V_5V_POK_N
D S
Q1702 LSK3541G1ET2L-1-GP
084.03541.M001

GPD7

GPD7	Reserved	Rising edge of DSW_PWROK	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after DSW_PWROK is high. 2. This signal is in the DSW well.

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: B
Document Number: V550_TGL
Rev: -1
Date: Monday, July 27, 2020
Sheet 17 of 106

SPI ROM

25	SPI_WP_CPU	
25	SPI_HOLD_CPU	
25	SPI_CLK_CPU	
25	SPI_CS_CPU_N0	
91	SPI_CS_CPU_N2	
25	SPI_SI_CPU	
25	SPI_SO_CPU	

WLAN

SSD

63	SSD_CLK_CPU_N	
63	SSD_CLK_CPU_P	
63	SSD_CLKREQ_CPU_N	

ESPI

24,68	ESPI_CPU_IO0	
24,68	ESPI_CPU_IO1	
24,68	ESPI_CPU_IO2	
24,68	ESPI_CPU_IO3	
24,68	ESPI_CPU_CS_N	
24,68	ESPI_CPU_RST_N	
24,68	ESPI_CPU_CLK	

OTHER

15	GPP_C5_SML0ALERT_N	
61	SUS_CLK	
24	RTCRST_ON	
15	GPP_E6_JTAG_ODT	
73	CPU_SMB_SCL_P0	
73	CPU_SMB_SDA_P0	
15	GPP_E10	
15	GPP_E11	

CPU1E — 5 OF 21 — TGL-U-1-GP-U1

CPU1K — 11 OF 21 — TGL-U-1-GP-U1

To TBT

Q1801 LSK3541G1ET2L-1-GP 084.03541.M001

Q1802 LSK3541G1ET2L-1-GP 084.03541.M001

	C1802(Cg)	C1803(Cd)
EPSON 082.30003.0191	15pF	15pF
SEIKO 082.30003.0301	15pF	15pF
NDK 082.30003.0221	15pF	12pF

	C1801(Cg)	C1804(Cd)
HARMONY 082.30040.0091	15pF	15pF
HOSONIC 082.30040.0101	12pF	12pF
HOSONIC 082.30040.0161	12pF	12pF

Memory Configuration

10: 16Gb
11: 32Gb

Memory Supplier

00: Samsung
01: Micron
10: SK Hynix
11: (Reserve)

GPP_F15	GPP_F14	GPP_F13	GPP_F12	GPP_F11				
MEM_ID4	MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	Vendor PN	Wisrton PN	Vendor	Density
1	0	0	1	0	MT53E512M32D2NP-046 WT:F	SM30E51328	Micron	16GB
1	0	1	0	0	H9HCNNNBKMMLXR-NEE	SM30N76602	SK Hynix	16GB
1	0	0	0	0	K4U6E3S4AA-MGCR	SM30N76677	Samsung	16GB
1	1	0	1	0	MT53E1G32D2NP-046 WT:A	SM30N76681	Micron	32GB
1	1	1	0	0	H9HCNNNCPMMLXR-NEE	SM30N76603	SK Hynix	32GB
1	1	0	0	0	K4UBE3D4AA-MGCR	SM30N76678	Samsung	32GB

0=L ,1=H

GPP_B23

GPP_B23 / SML1ALERT# / PCHHOT# / GSPI1_CS1#	CPUNSSC Clock Frequency	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0 = 38.4 MHz clock (direct from crystal) (default) 1 = 19.2 MHz clock (derived from 38.4 MHz crystal) Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. 3. This signal is in the primary well.

SPI0_MOSI

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling. Follow #607872 SchChk Rev1p1 PU 100K

SPI0_IO2

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.

SPI0_IO3

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.

GPP_C2

GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. 0=Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1=Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

TEST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)

Size: A2 | Document Number: V550_TGL | Rev: -1

Date: Monday, July 27, 2020 | Sheet 18 of 106

27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
27 HDA_SDIN0_CPU
15 HDA_SDOUT_CPU
61 CNV_CLKREQ
61 CNV_RF_RST_N

91 PIRQA_N
66 DMIC_SCL0_CPU
66 DMIC_SDA0_CPU

61 BLUETOOTH_EN
71,73 RT_FORCE_PWR

7 OF 21

CPU1G

20190510_Byron

HDA_BITCLK_CODEC 1 R1901 2 20R2J-2-GP HDA_BITCLK_CPU
HDA_SYNC_CODEC 1 R1902 2 20R2J-2-GP HDA_SYNC_CPU
HDA_SDOUT_CODEC 1 R1903 2 20R2J-2-GP HDA_SDOUT_CPU

DR38	GPP_R0/HDA_BCLK/I2S0_SCLK	
DU37	GPP_R1/HDA_SYNC/I2S0_SFRM	
DT37	GPP_R2/HDA_SDO/I2S0_TXD	
DV37	GPP_R3/HDA_SDI0/I2S0_RXD	strap
DV41	GPP_R4/HDA_RST#	
DL53	GPP_A7/I2S2_SCLK/DMIC_CLK_A0	
DG51	GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0	
DG50	GPP_A10/I2S2_RXD/DMIC_DATA1	
DL49	GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1	
DL52	GPP_A11/PMC_I2C_SDA/I2S3_SCLK	
DH49	GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0	
DF33	SNDW_RCOMP	

PIRQA_N
CNV_RF_RST_N
CNV_CLKREQ
BLUETOOTH_EN
SNDW_RCOMP

R1904 1 200R2F-L1-GP

DW15	GPP_F8_I2S_MCLK2_INOUT	
DW24	GPP_D19/I2S_MCLK1	
DG41	GPP_A23/I2S1_SCLK	RT_FORCE_PWR
DT38	GPP_R7/I2S1_SFRM	
DV38	GPP_R6/I2S1_TXD	
DW38	GPP_R5/HDA_SDI1/I2S1_RXD	
DN31	GPP_S6/SNDW3_CLK/DMIC_CLK_A0	DMIC_SCL0
DM31	GPP_S7/SNDW3_DATA/DMIC_DATA0	DMIC_DATA0
DK33	GPP_S4/SNDW2_CLK/DMIC_CLK_A1	
DK31	GPP_S5/SNDW2_DATA/DMIC_DATA1	
DW35	GPP_S2/SNDW1_CLK/DMIC_CLK_B0	
DV35	GPP_S3/SNDW1_DATA/DMIC_CLK_B1	
DT32	GPP_S0/SNDW0_CLK	
DR35	GPP_S1/SNDW0_DATA	

TGL-U-1-GP-U1

R1905 2 1 33R2J-2-GP DMIC_SCL0_CPU
R1906 2 1 33R2J-2-GP DMIC_SDA0_CPU

DY C1902 SC33P50V2JN-3GP
DY C1901 SC33P50V2JN-3GP

HDA_BITCLK_CODEC

DY EC1901 SCD1U16V1KX-GP

TEST

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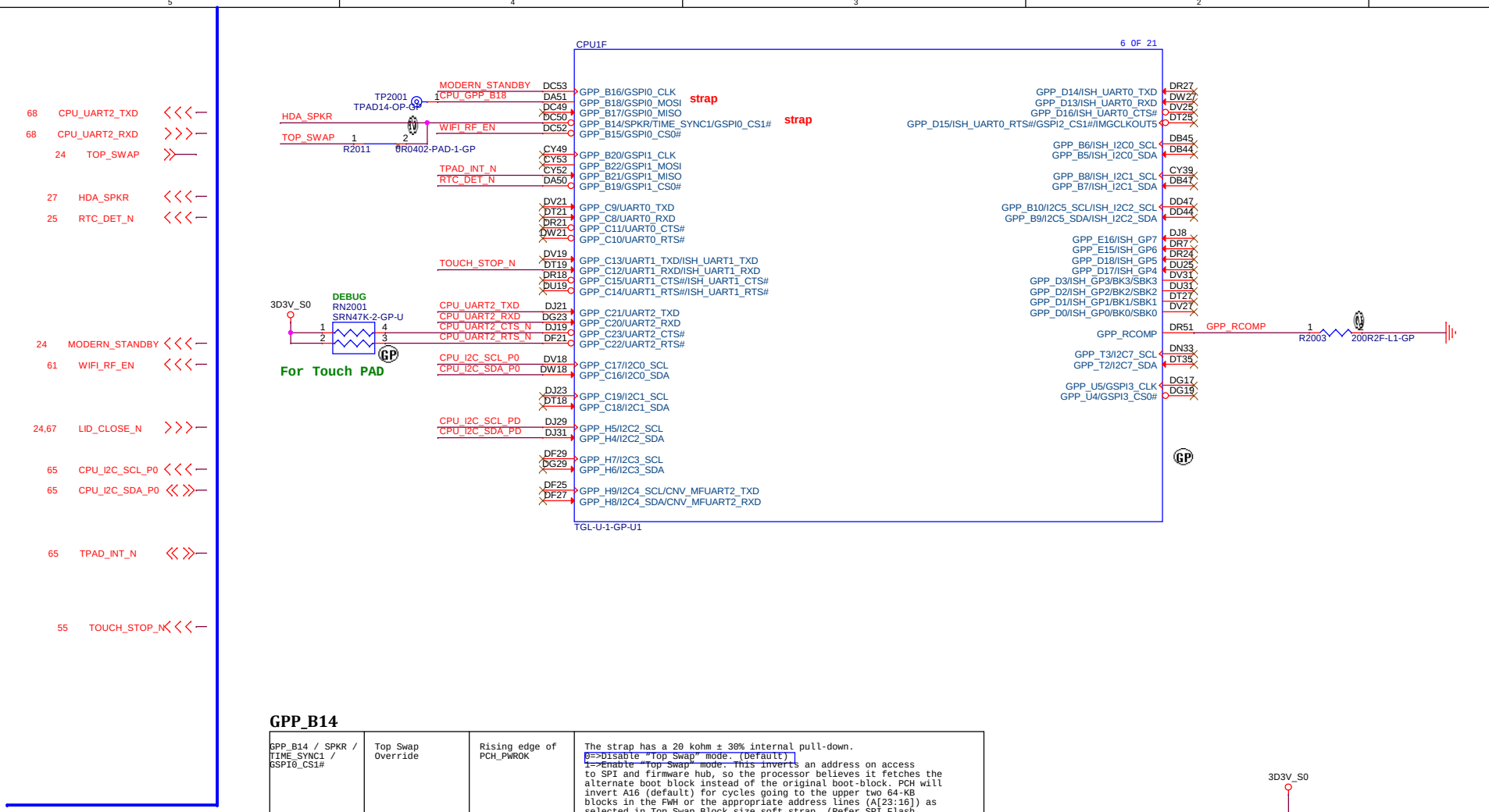
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)

Size	Document Number	Rev
A3	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 19 of 106

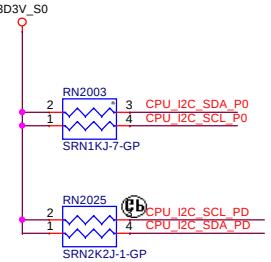


GPP_B14

GPP_B14 / SPKR / TIME_SYNC1 / GSPI0_CS1#	Top Swap Override	Rising edge of PCH_PWROK	The strap has a 20 kohm ± 30% internal pull-down. 0=>Disable "Top Swap" mode. (Default) 1=>Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap. (Refer SPI Flash Programming Guide). Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

GPP_B18

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The strap has a 20 kohm ± 30% internal pull-down. 0=>Disable "No Reboot" mode. (Default) 1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



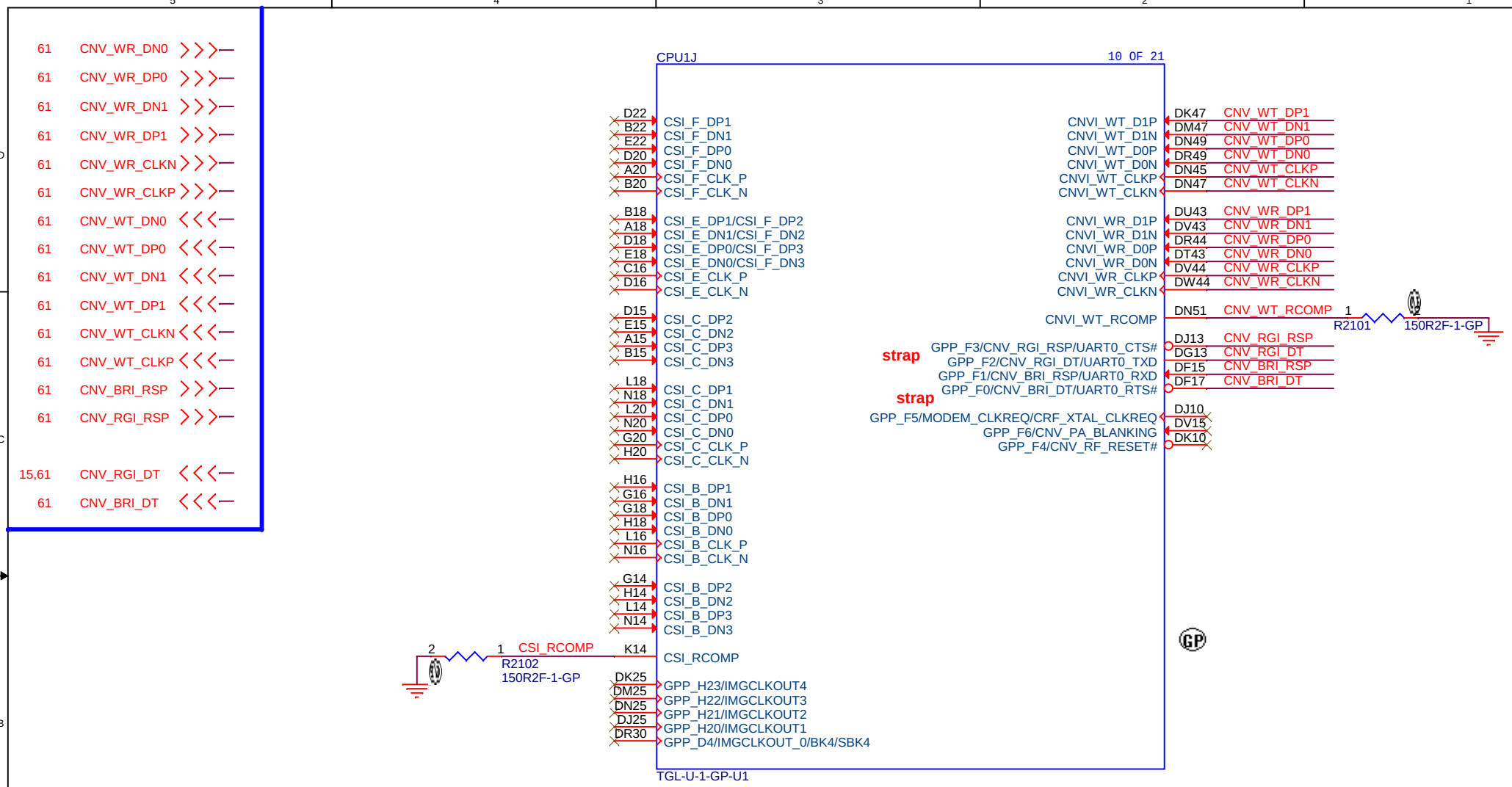
TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size: A3 | Document Number: V550_TGL | Rev: -1

Date: Monday, July 27, 2020 | Sheet 20 of 106



GPP_F0

GPP_F0 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Selection	Rising edge of RSMRST#	This strap has a 20 kohm ± 30% internal pull-down. This strap should not be pulled high since 24 MHz crystal is not supported on the PCH. 0 = 38.4 MHz (default) 1 = 24 MHz Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

TEST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CSI/EMMC/CNVi)**

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 21 of 106

50 VCCAUX_SENSE
50 VSSAUX_SENSE
40,50 VCCIN_AUX_VID0
40,50 VCCIN_AUX_VID1

1D8V_VCCIN_AUX (27A)

CPU1N 14 OF 21

AB12 AC10 AE10 AK2 AR10 AT12 AU10 AW10 BV1 BV39 BW40 BY39 CC1 CD12 CF10 CG12 CH10 CJ1 CJ12 CK10 CL12 CM10 CP1 CP10 CR12 CT10 CU12 CY1 AK1 — VCCIN_AUX

PH/PL 100R at VR side.

VSSAUX_SENSE AV9 — VCCIN_AUX_VSSSENSE
VCCAUX_SENSE AT9 — VCCIN_AUX_VCCSENSE

TP2203 TPAD14-OP-GP — VCC_VNNEXT_1P05 DD17 — VCC_VNNEXT_1P05
DD18 — VCC_VNNEXT_1P05

TP2202 TPAD14-OP-GP — VCC_V1P05EXT_1P05 DA15 — VCC_V1P05EXT_1P05
DA17 — VCC_V1P05EXT_1P05

3D3V_S5 — R2206 10KR1J-GP — VRALERT_N DB39 — GPP_B2/VRALERT#
DV12 — GPP_F22/VNN_CTRL
DT12 — GPP_F23/V1P05_CTRL

VCCIN_AUX_VID0 DB37 — GPP_B0/CORE_VID0
VCCIN_AUX_VID1 DB38 — GPP_B1/CORE_VID1

TGL-U-1-GP-U1

(1.3A) 1D8V_S5_VCCPRIM — 1D8V_S5
CY18 CY20 CY24 CY26 DA18 DA20 DA22 DA24 DA26 DC18 DC20 DC22 DC24 DC26 DD20 DD22 DV22 — VCCPRIM_1P8
1 R2201 2 0R0805-PAD-1-GP-U

(202mA) 3D3V_S5_VCCPRIM — 3D3V_S5
DA35 DC28 DC30 DD30 — VCCPRIM_3P3
1 R2202 2 0R0402-PAD-1-GP

DV34 — DCPRTC — 3D3V_RTC_EXT

DV46 — VCCLDOSTD_0P85 — 0D85V_S5_VCCLDOSTD_OUT

DV16 DC15 — VCCA_CLKLDO_1P8 — 1D8V_S5_CLKLDO (165mA) Analog supply for internal clocks

DV28 — VCCDPHY_1P24 — 1D24V_S5_VCCDPHY_OUT

DD38 — VCCDSW_1P05 — 1D05V_S5_VCCDSW_OUT

BR3 BR4 BT5 — VCC1P05 — 1D05V_S5_OUT (0.8A) Supply to VCCST & VCCSTG
VCC1P05_OUT_FET

DA31 DC33 DC31 — VCCPRIM1P05_OUT_PCH — 1D05V_S5_VCCPRIM_OUT for CNVi and other internal I/O blocks.

DC35 — VCCRTC — 3D3V_RTC_AUX (5mA)
DD37 — VCCDSW_3P3 — 3D3V_S5 (3mA)
DA28 — VCCPGPPR — 3D3V_GPPR_S5 — R2204 — 0R0402-PAD-1-GP — 1D8V_S5 (17.5mA)
VCCPGPPR is for Audio Power.

CY31 CY33 CV39 — VCCPRIM_3P3 — 3D3V_S5_VCCPRIM
VCCPRIM_1P8 — 1D8V_S5_VCCPRIM

AP12 — RSVD#AP12 — TP_VCCANA_EHV 1 — TP2201

VCCGPPR
3.3V or 1.8V

#607872 Rev1p1
PDG VCCPRIM_1P8
0402 Placeholder 1PCS

#607872 Rev1p1
PDG VCCPRIM_3P3
0402 Placeholder 1PCS
0402 Placeholder 1PCS

#607872 Rev1p1
PDG VCCRTCEXT (Pin DV34)
0402 0.1UF 1PCS

#607872 Rev1p1
PDG VCCLDOSTD_0P85
0402 2.2UF 1PCS

#607872 Rev1p1
PDG VCCDPHY_1P24
0402 4.7UF 1PCS

#607872 Rev1p1
PDG VCCDSW_1P05
0402 1UF 1PCS

#607872 Rev1p1
PDG VCCRTC
0402 0.1UF 1PCS
0402 1UF 1PCS

#607872 Rev1p1
PDG VCCDSW_3P3
0402 Placeholder 1PCS

Trace width > 40mil
1D05V_S5_VCCDSW_OUT — C2201 SC1U6D3V1MX-GP

Place cap within 3mm from SOC edge.
1D24V_S5_VCCDPHY_OUT — For CNVi — C2202 SC4D7U6D3V2MX-GP-U

Place cap within 3mm from SOC edge
0D85V_S5_VCCLDOSTD_OUT — C2203 SC2D2U6D3V2MX-GP

Must take care this power layout and add shield GND.
(165mA) 1D8V_S5 — 1D8V_S5_CLKLDO
1 R2205 2 0R0402-PAD-1-GP
C2204 SC22U6D3V3MX-L1-GP — C2205 SC22U6D3V3MX-L1-GP

#607872 Rev1p1
PDG VCCA_CLKLDO_1P8
680nF
0603 00HM 1PCS
0603 47UF 1PCS

PH Same as SPI Programming Guide for details

3D3V_S5 — RN2201 SRN10KJ-5-GP — 1 2 4 3 — VCCIN_AUX_VID0 VCCIN_AUX_VID1
CORE_VID0/1 can PU to VCCPRIM_1P8 or 3P3.

(1.3A) 1D8V_S5_VCCPRIM — DY C2206 SC1U10V2KX-L1-GP — DY C2207 SC1U10V2KX-L1-GP

3D3V_S5_VCCPRIM — DY C2208 SC1U10V2KX-L1-GP — C2209 SCD1U16V2KX-L-GP

3D3V_RTC_AUX — C2210 SC1U10V2KX-L1-GP — C2211 SCD1U16V2KX-L-GP

3D3V_RTC_EXT — C2212 SCD1U16V2KX-L-GP

1D05V_S5_VCCPRIM_OUT — DY C2213 SC1U10V2KX-L1-GP

1D05V_S5_OUT — DY C2216 SC1U10V2KX-L1-GP

3D3V_S5 — C2217 SC1U10V2KX-L1-GP

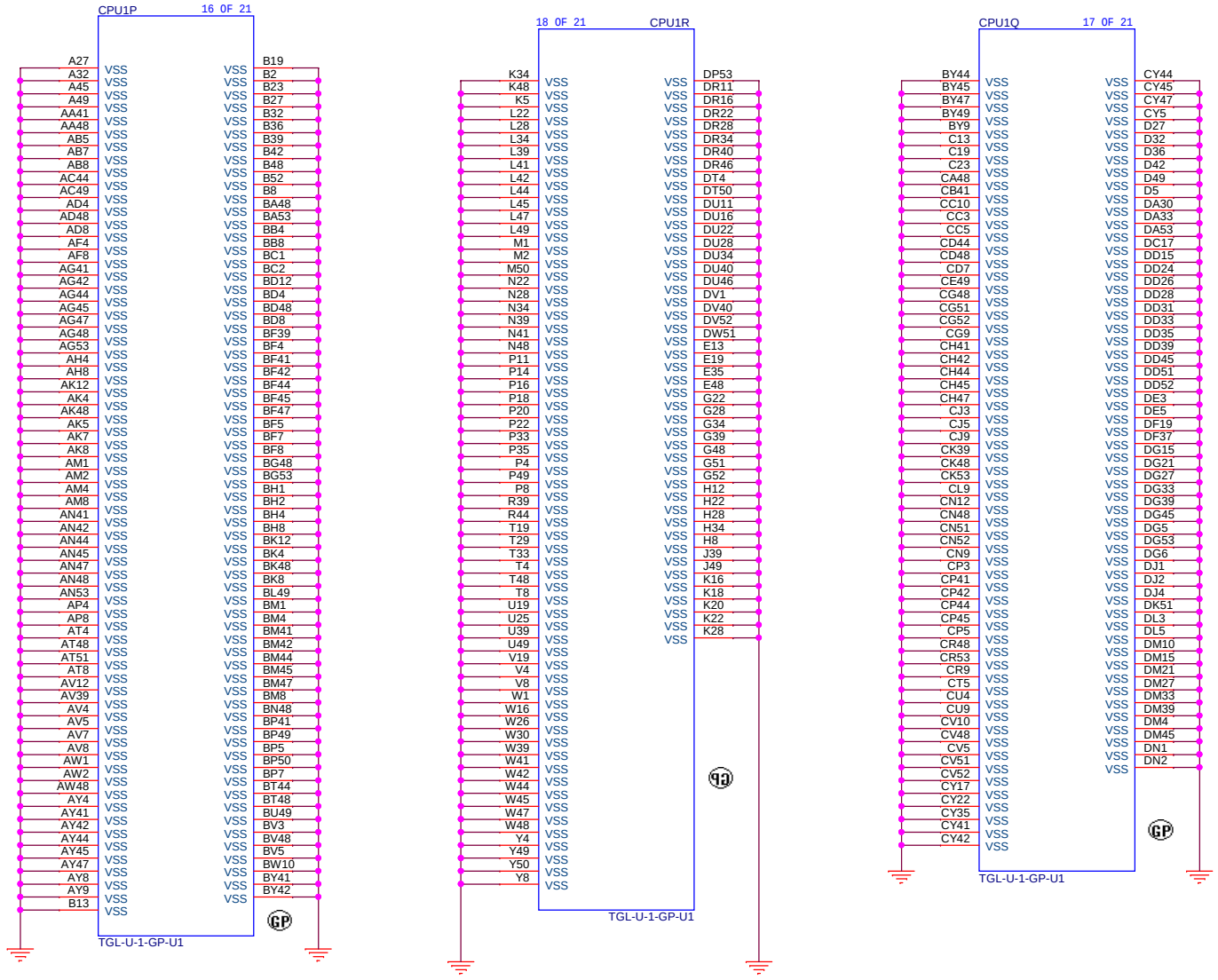
3D3V_GPPR_S5 — DY C2218 SCD1U16V2KX-L-GP

Close to pin DD37

TEST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)
Size: A3 | Document Number: V550_TGL | Rev: -1
Date: Monday, July 27, 2020 | Sheet 22 of 106



TEST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (VSS)		
Size: B	Document Number: V550 TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 23 of 106	

SSID = KBC

Model_ID_BOM Ctrl

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
13"	100.0K	10.0K	64.10025.L0L	3.0V
14"	100.0K	20.0K	64.20025.L0L	2.75V
NA	100.0K	33.0K	64.33025.L0L	2.48V
NA	100.0K	47.0K	64.47025.6DL	2.24V
NA	100.0K	64.9K	64.64925.6DL	2.0V
NA	100.0K	76.8K	64.76825.6DL	1.87V
NA	100.0K	215.0K	64.21535.6DL	1.048V

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-1M	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

KBC PWR supply at PSL mode.

Wireless charge

1st_BATTERY / CHARGER

TBT

THERM2

THERM1

PSL

CHECK

STRAP **ESPI_STRAP**. These two bits are strapped values of LPC_eSPI_Strap1 and LPC_eSPI_Strap0.
Mode indication:
00: Intel eSPI Interface with eSPI Flash share structure.
01: eSPI Interface with Share Flash structure.
10: AMD eSPI Interface with SPI (eSPI pins) Flash share structure.
11: LPC Interface with Share Flash structure.

Prevent BIOS data loss solution

Q2401 84.03906.G11->84.T3906.E11(main)

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

EC GPIO PH

EC GPIO PL

EC_GPIO47 High Active

Wistron Corporation
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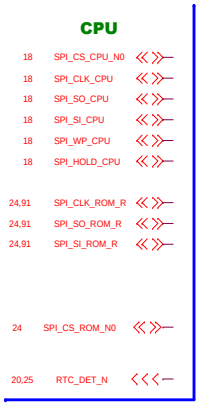
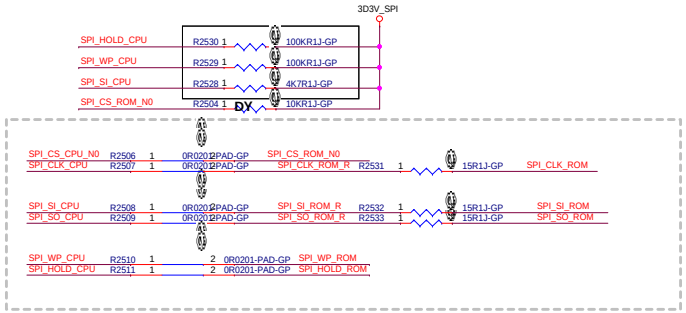
Taipei Hsien 221, Taiwan, R.O.C.

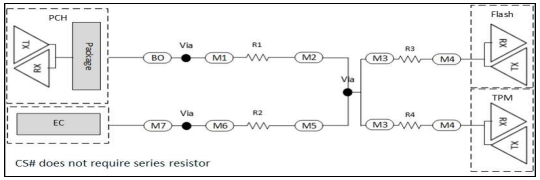
Title: ECIO (NUVOTON_NPCE386)

Size: A1 | Document Number: V550_TGL | Rev: -1

Date: Monday, July 27, 2020 | Sheet 24 of 105







SPI0 2 load topology with EC Wired-OR Flash Sharing (1 flash and 1 TPM):

R1 is required 0Ω placeholder for 1.8V and 0Ω for 3.3V.

R2 is required 50Ω for 1.8V and 100Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI.

R2 is required 50Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_IO_2 and SPI0_IO_3. If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.

R3 is required 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI.

R3 is required 33Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_IO_2 and SPI0_IO_3. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation.

R4 is required 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If TPM use SPI0_IO_2 and SPI0_IO_3, R4 value shall follow MISO and MOSI recommendation

SPI ROM 32M

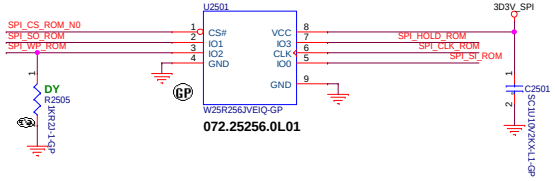
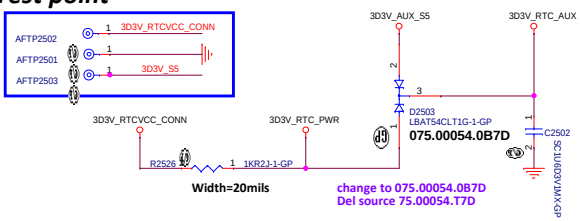


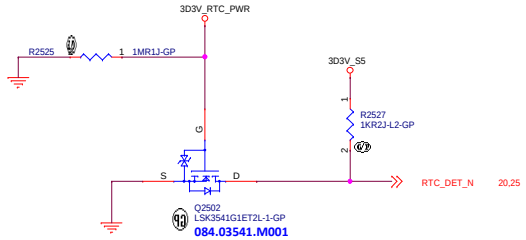
TABLE BIOS1
32MB (256Mb) 8x6mm WSON8

Vender	Vender P/N	Wistron P/N
WINBOND	W25R256JVEIQ	072.25256.0L01
MACRONIX	MX77L25650FZ4I42	072.77256.0003
GIGADEVICE	GD25R256DYIGR	072.25256.0H03

SSID = RBATT

Test point





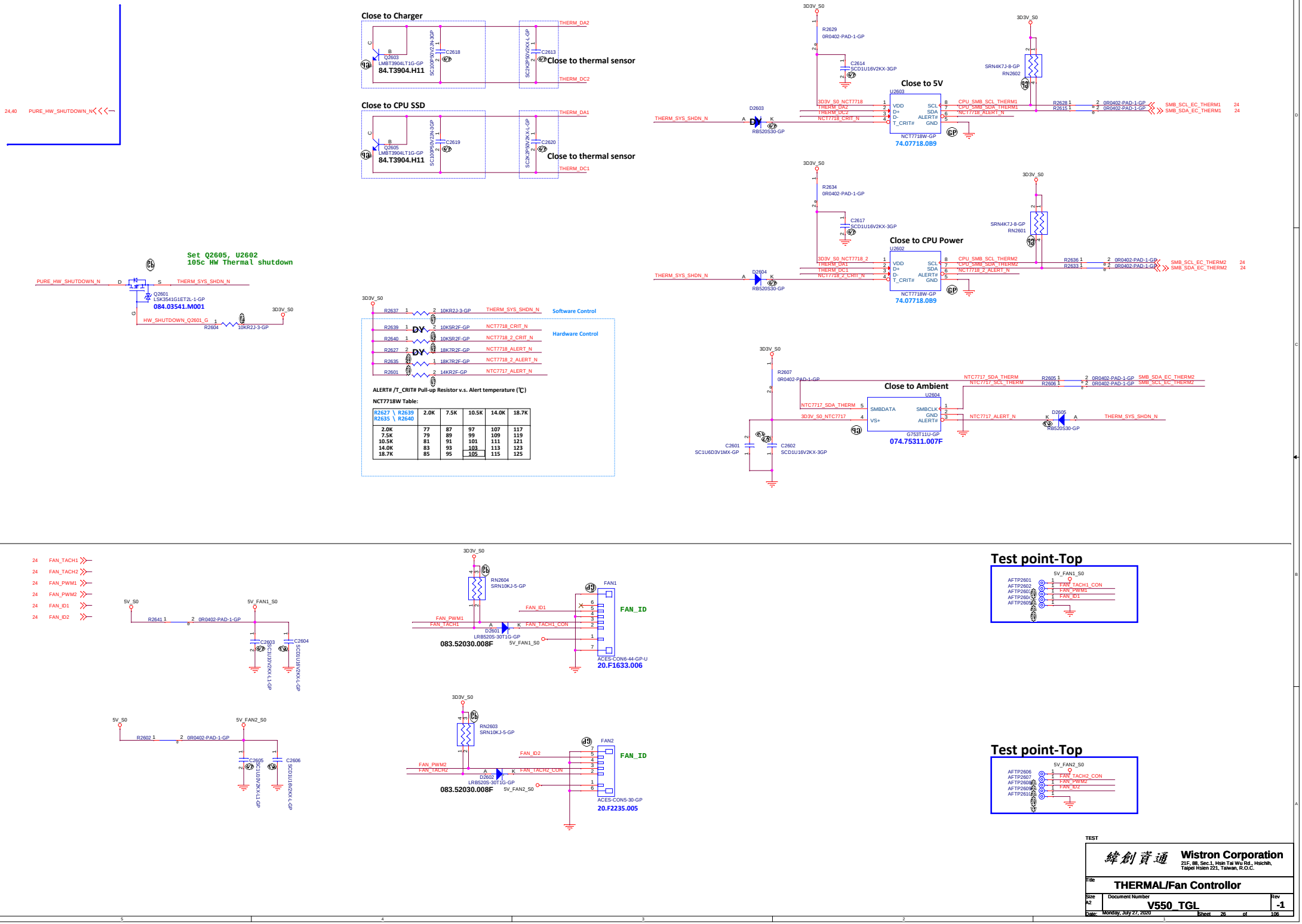
TEST

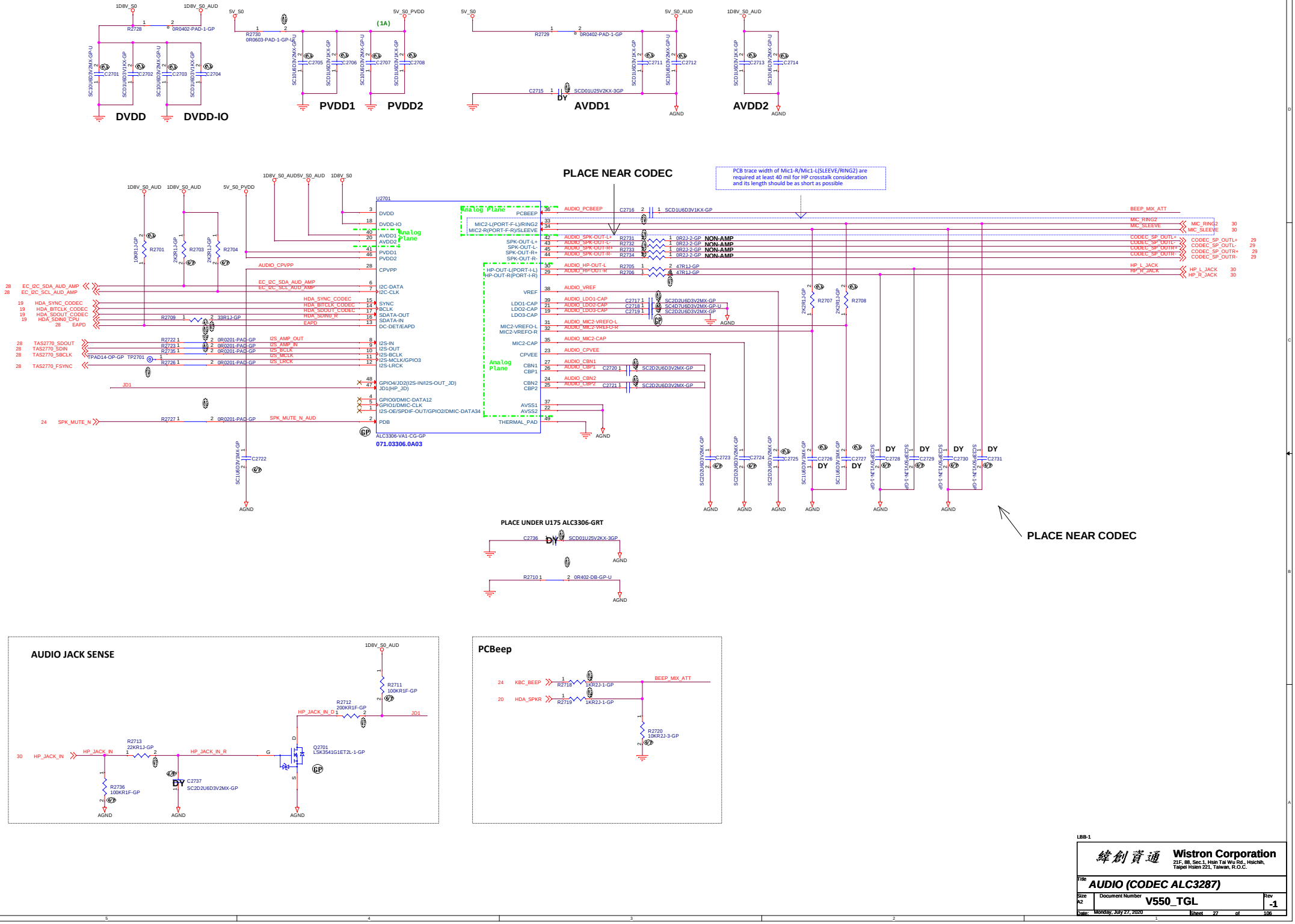
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**

Size	Document Number	Rev
C	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 25 of 106


24.40 PURE_HW_SHUTDOWN_N
Close to Charger
Q2603
LMBT3904LT1G-GP
84.T3904.H11
C2618
C2613
THERM_DA2
THERM_DC2
Close to thermal sensor
Close to CPU SSD
Q2605
LMBT3904LT1G-GP
84.T3904.H11
C2619
C2620
THERM_DA1
THERM_DC1
Close to thermal sensor
3D3V_S0
R2629
0R0402-PAD-1-GP
C2614
SCD1U16V2KX-3GP
SRN4K7J-8-GP
RN2602
Close to 5V
U2603
NCT7718W-GP
74.07718.089
D2603
RB520S30-GP
THERM_SYS_SHDN_N
3D3V_S0_NCT7718
THERM_DA2
THERM_DC2
NCT7718_CRIT_N
CPU_SMB_SCL_THERM1
CPU_SMB_SDA_THERM1
NCT7718_ALERT_N
SMB_SCL_EC_THERM1
SMB_SDA_EC_THERM1
R2634
0R0402-PAD-1-GP
C2617
SCD1U16V2KX-3GP
SRN4K7J-8-GP
RN2601
Close to CPU Power
U2602
NCT7718W-GP
74.07718.089
D2604
RB520S30-GP
THERM_SYS_SHDN_N
3D3V_S0_NCT7718_2
THERM_DA1
THERM_DC1
NCT7718_2_CRIT_N
CPU_SMB_SCL_THERM2
CPU_SMB_SDA_THERM2
NCT7718_2_ALERT_N
SMB_SCL_EC_THERM2
SMB_SDA_EC_THERM2
Set Q2605, U2602
105c HW Thermal shutdown
PURE_HW_SHUTDOWN_N
THERM_SYS_SHDN_N
Q2601
LSK3541G1ET2L-1-GP
084.03541.M001
HW_SHUTDOWN_Q2601_G
R2604
10KR2J-3-GP
3D3V_S0
R2637 10KR2J-3-GP THERM_SYS_SHDN_N
R2639 10K5R2F-GP NCT7718_CRIT_N
R2640 10K5R2F-GP NCT7718_2_CRIT_N
R2627 18K7R2F-GP NCT7718_ALERT_N
R2635 18K7R2F-GP NCT7718_2_ALERT_N
R2601 14KR2F-GP NTC7717_ALERT_N
DY
DY
Software Control
Hardware Control
ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)
NCT7718W Table:
R2627 \ R2639
R2635 \ R2640
2.0K 7.5K 10.5K 14.0K 18.7K
2.0K 77 87 97 107 117
7.5K 79 89 99 109 119
10.5K 81 91 101 111 121
14.0K 83 93 103 113 123
18.7K 85 95 105 115 125
3D3V_S0
R2607
0R0402-PAD-1-GP
Close to Ambient
U2604
G753T11U-GP
074.75311.007F
NTC7717_SDA_THERM
NTC7717_SCL_THERM
3D3V_S0_NTC7717
NTC7717_ALERT_N
D2605
RB520S30-GP
THERM_SYS_SHDN_N
C2601
SC1U6D3V1MX-GP
C2602
SCD1U16V2KX-3GP
24 FAN_TACH1
24 FAN_TACH2
24 FAN_PWM1
24 FAN_PWM2
24 FAN_ID1
24 FAN_ID2
5V_S0
5V_FAN1_S0
R2641 0R0402-PAD-1-GP
C2603
C2604
SCD1U16V2KX-1-GP
5V_S0
5V_FAN2_S0
R2602 0R0402-PAD-1-GP
C2605
C2606
SCD1U16V2KX-1-GP
3D3V_S0
RN2604
SRN10KJ-5-GP
FAN1
FAN_ID
FAN_ID1
FAN_PWM1
FAN_TACH1
FAN_TACH1_CON
D2601
LRB520S-30T1G-GP
083.52030.008F
5V_FAN1_S0
ACES-CON6-44-GP-U
20.F1633.006
3D3V_S0
RN2603
SRN10KJ-5-GP
FAN2
FAN_ID
FAN_ID2
FAN_PWM2
FAN_TACH2
FAN_TACH2_CON
D2602
LRB520S-30T1G-GP
083.52030.008F
5V_FAN2_S0
ACES-CON5-30-GP
20.F2235.005
Test point-Top
5V_FAN1_S0
AFTP2601
AFTP2602
AFTP2603
AFTP2604
AFTP2605
FAN_TACH1_CON
FAN_PWM1
FAN_ID1
Test point-Top
5V_FAN2_S0
AFTP2606
AFTP2607
AFTP2608
AFTP2609
AFTP2610
FAN_TACH2_CON
FAN_PWM2
FAN_ID2
TEST
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
THERMAL/Fan Controllor
Size A2
Document Number V550_TGL
Rev -1
Date: Monday, July 27, 2020
Sheet 26 of 106



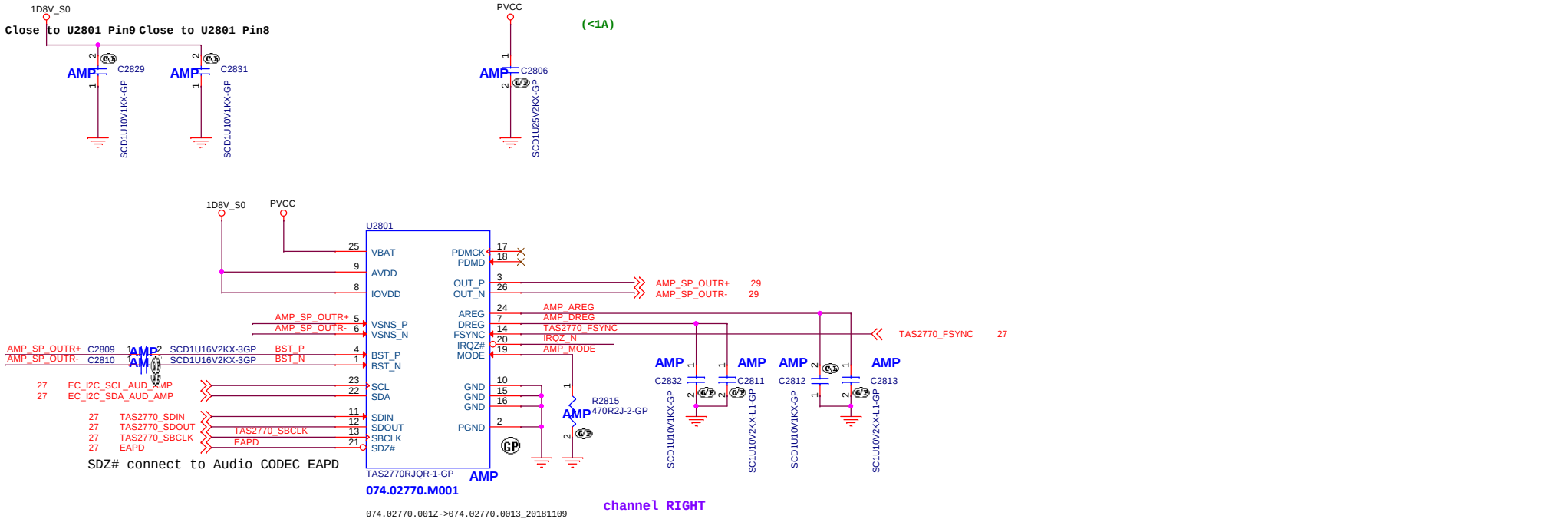
LBB-1

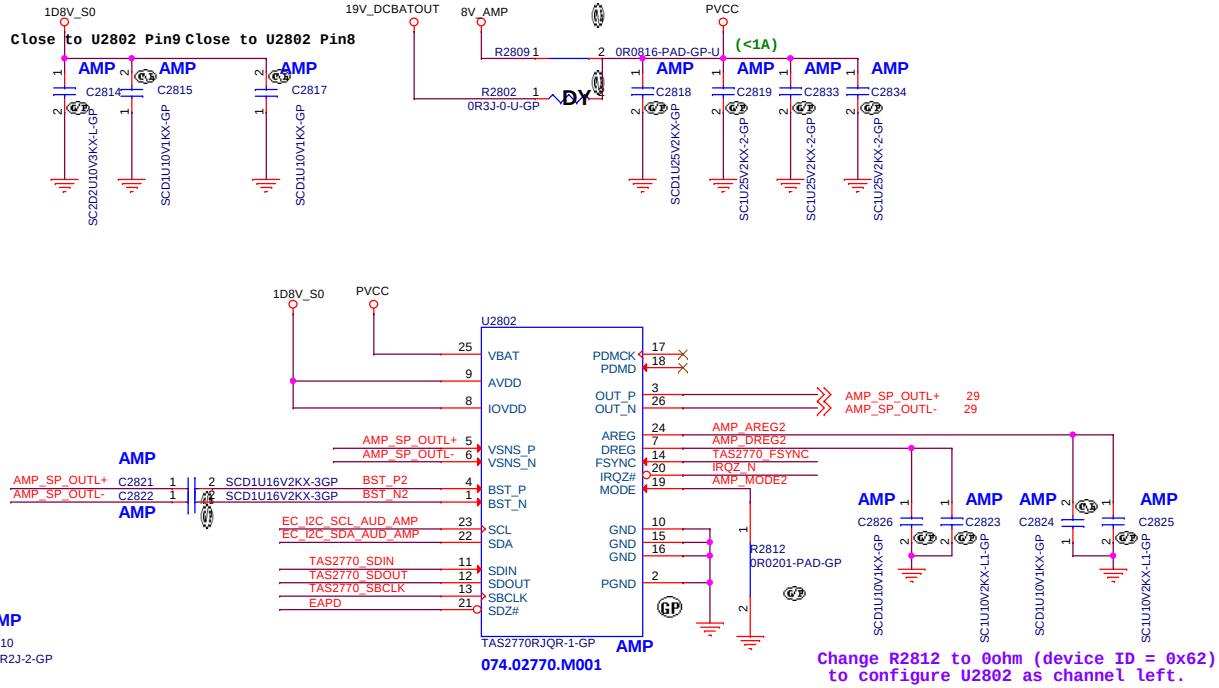
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (CODEC ALC3287)**

Size	Document Number	Rev
A2	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 27 of 106

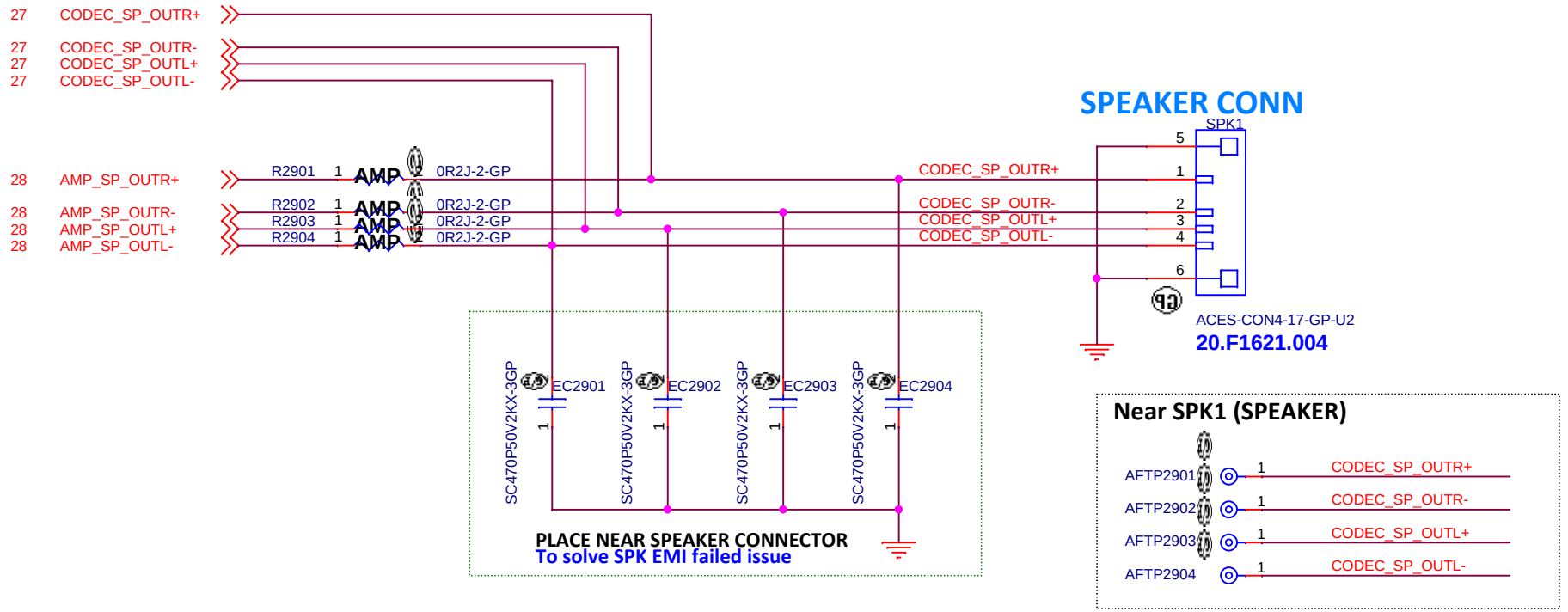




LBB-1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO (MIC I/F)		
Size: A3	Document Number: V550_TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 28 of 106	

Main Func = AUDIO



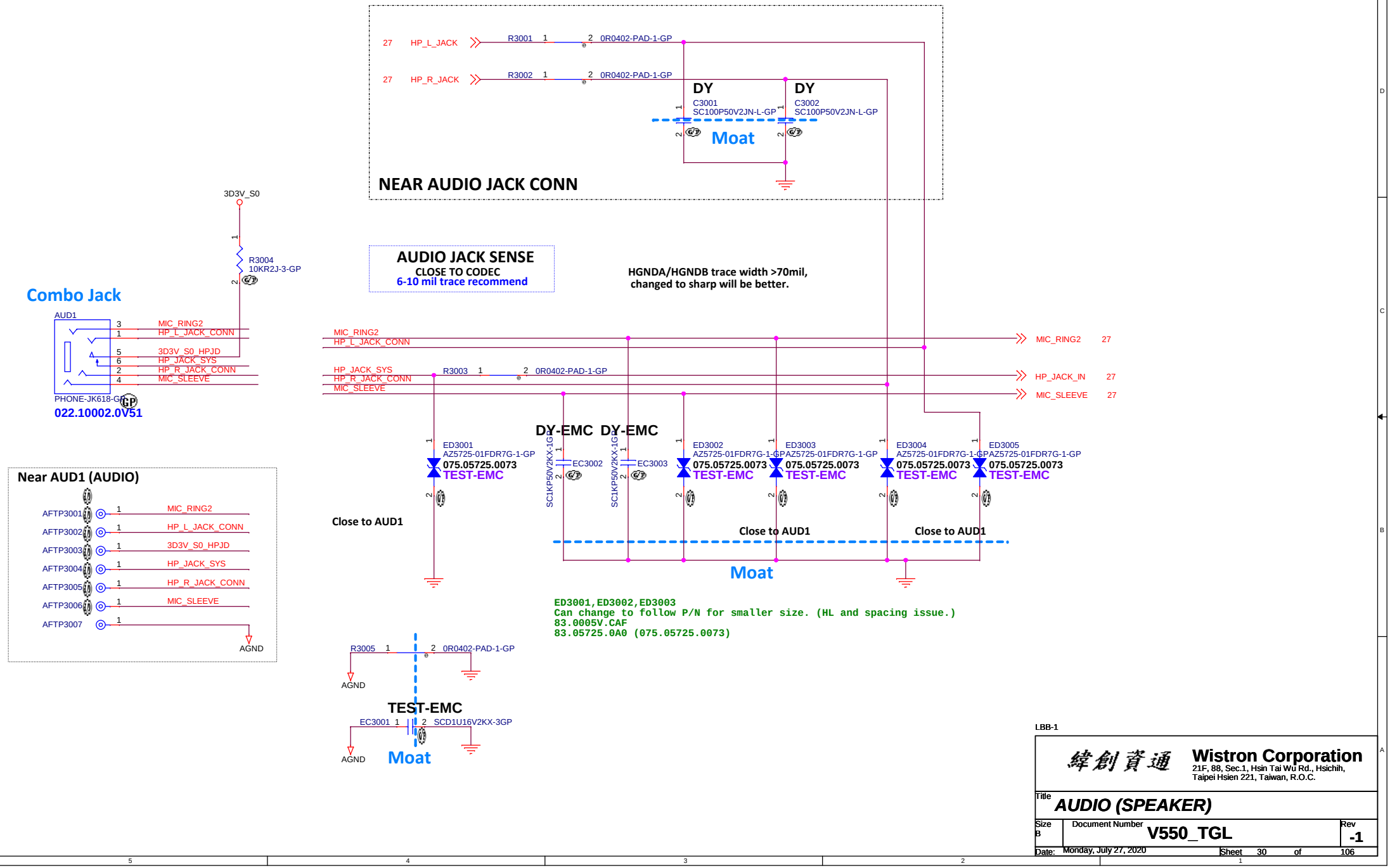
LBB-1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (AUDIO JACK)***

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 29 of 106



LBB-1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (SPEAKER)***

Size	Document Number	Rev
B	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 30 of 106

BOM1

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN RTL8111H

Size	Document Number	Rev
A3	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 31 of 106

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RJ45

Size	Document Number	Rev
Custom	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 32 of 106

(Blanking)

LAR-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER (SDIO/CONN)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 33 of 106

(Blanking)

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD) (USB2.0 CONN)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 34 of 106

BOM1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

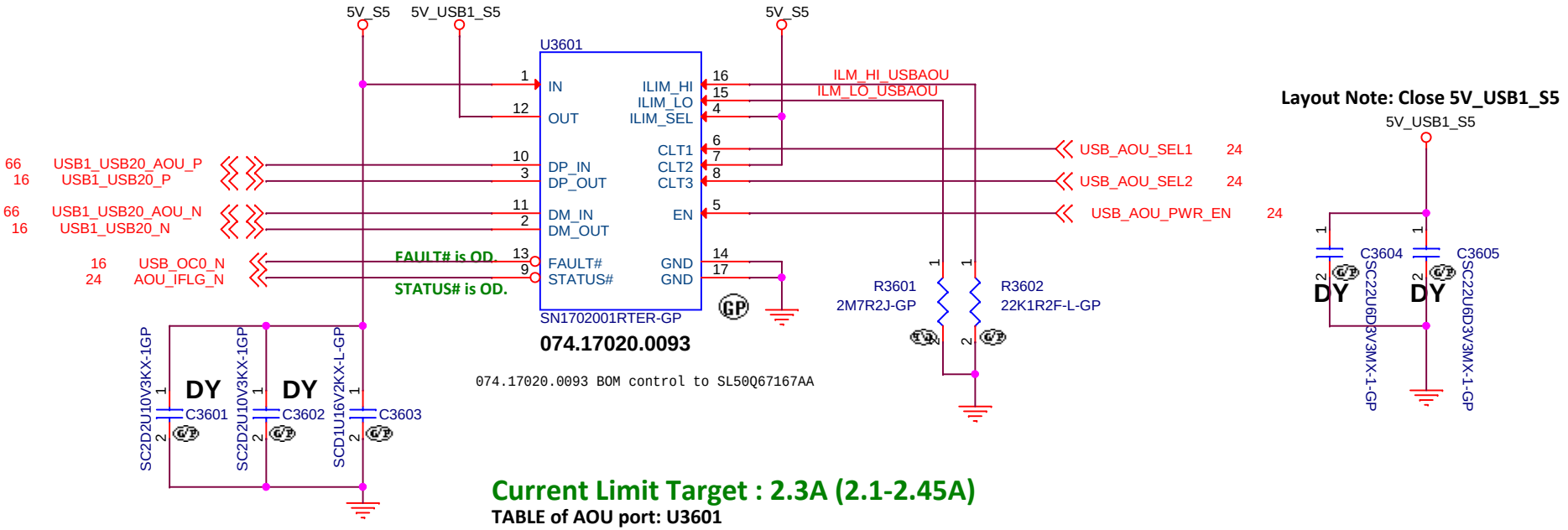
USB (USB3.0 Conn)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 35 of 106

Main Func = USB Charger

For USB3.0 System Port1 (For AOU)



Layout Note: Close 5V_USB1_S5

Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3601

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER	SL50Q67167AA
2nd	DIODES	PI5USB2546HZHEX	SL50Q67168AA

SN1702001RTER is not equivalent device of TPS2546RTER

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB(USB Charger)***

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 36 of 106

(Blanking)

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD) (PCIE to USB3.0)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 37 of 106

Main Func = USB3.0 Re-driver

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB (USB Redriver/Hub)*

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 38 of 106

TEST

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sequence (RSVD)

Size	Document Number	Rev
A4	V550_TGL	-1

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RUN Power

17,24 PM_SLP_S4_N
17,24,54,57 PM_SLP_S3_N
17,24 PM_SLP_SUS_N
17,24,63,91 PLTRST_CPU_N
46 PWR_VCORE_VR_EN
17 PCH_PWROK
45 PWR_VDDQ_PG
22,50 VCCIN_AUX_VID0
22,50 VCCIN_AUX_VID1

17 VCCST_OVERRIDE
17,24 ALL_SYS_PWRGD
46 VCORE_READY
17 CPU_C10_GATE_N
24,26 PURE_HW_SHUTDOWN_N

45 1D8V_S5_EN
45,50 1D8V_S5_PWRGD

17,50 VCCIN_AUX_PWRGD

4,55 eDP_VDDEN_CPU

45 PWR_VTT_EN

45 PWR_VDDQ_EN

RUN Power

5V_S0/3D3V_S0

U4001 G2898KD1U-GP
074.02898.0093
074.22976.0091
5V_S0 (2.5A)
3D3V_S0 (2A)

For CODEC / 3D3V_LCD

U4003 G2898KD1U-GP
074.02898.0093
074.22976.0091
1D8V_S0 (150mA)

U4002 G2898KD1U-GP
074.02898.0093
074.22976.0091
3D3V_S5 (2A)

S5_ENABLE → D4006 LRB520S-30T1G-GP → PURE_HW_SHUTDOWN_N

6A/Rds(on):4.5mOhm/Tr:7~20us

U4004 G5027CRD1D-GP-U
1D05V_VCCSTG_FIP (300mA)

D4001 BAT54C-12-GP
VCCIN_AUX_VID0 / VCCIN_AUX_VID1 → VCCST_READY
VCCST_OVERRIDE_3D3V → VCCST_OVERRIDE
PM_SLP_S3_N → VCCST_EN
VCCST_READY → VCCST_EN
CPU_C10_GATE_N → VCCSTG_EN
VCCST_READY → VCCSTG_EN

6A/Rds(on):4.5mOhm/Tr:7~20us

U4005 G5027CRD1D-GP-U
1D05V_VCCST_FIP (500mA)

Power Sequence / Pull High PWRGD

3D3V_S0 → R4014 10KR2J-3-GP → VCORE_READY → PCH_PWROK
PM_SLP_SUS_N → R4013 → 1D8V_S5_EN
3D3V_S5 → R4022 20KR2J-L3-GP → 1D8V_S5_PWRGD
3D3V_S0 → R4021 1KR2J-1-GP → D4005 LRB520S-30T1G-GP
PM_SLP_S3_N, PWR_VDDQ_PG → ALL_SYS_PWRGD
PWR_VCORE_VR_EN

3D3V_S5 → R4018 10KR2J-1-GP → VCCST_OVERRIDE_Q1 → Q4002 LSI1012LT1G-GP 084.01012.0031 → (1.05V) VCCST_OVERRIDE
3D3V_S5 → R4017 10KR2J-1-GP → VCCST_OVERRIDE_3D3V → Q4003 LSK3541G1ET2L-1-GP 084.03541.M001

For LPDDR4x only: 0D6V_S3 Power on to after 1D1V_S3

PWR_VDDQ_PG, PM_SLP_S4_N → PWR_VTT_EN

PM_SLP_S4_N → PWR_VDDQ_EN

For PWR_VDDQ_EN RC delay
Layout Note:Place Close to PU5101

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (Power Plane Enabl
Size: A2
Document Number: V550_TGL
Rev: -1
Date: Monday, July 27, 2020
Sheet 40 of 106

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

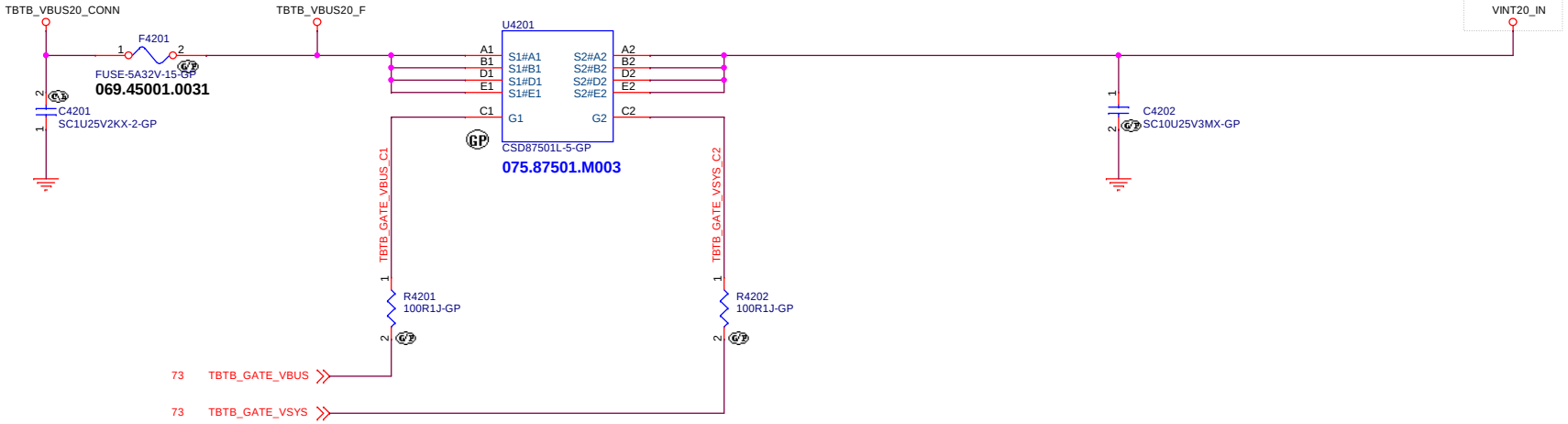
Title

Sequence (RSVD) (DS3/S0ix)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 41 of 106

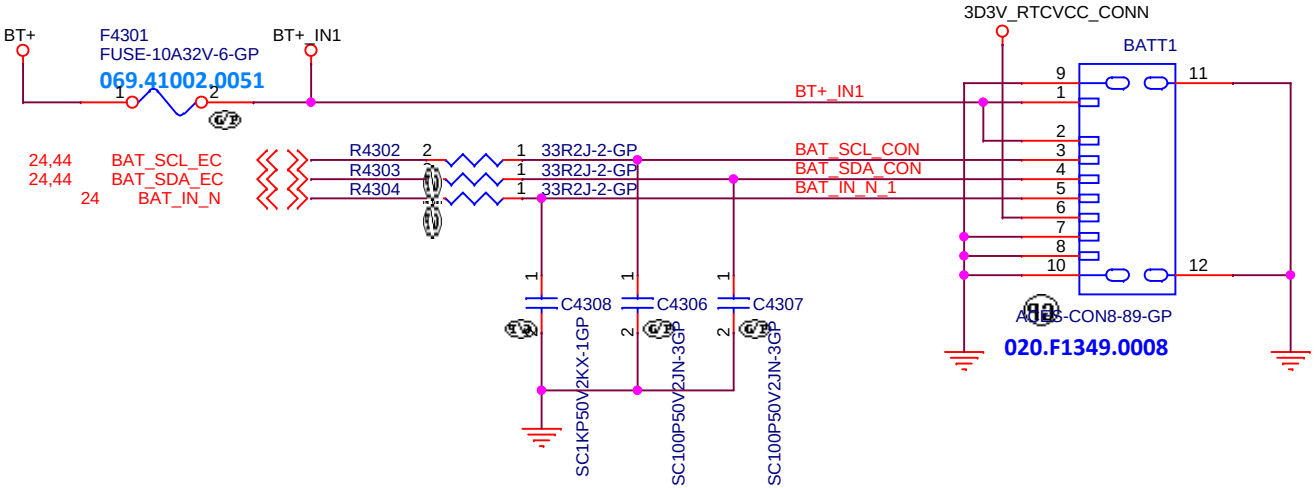
(65W ADT: 20V, 3.25A)
(95W ADT: 20V, 4.75A)

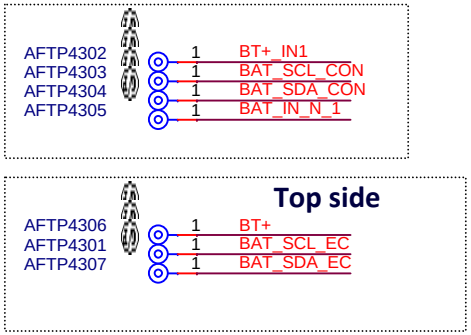


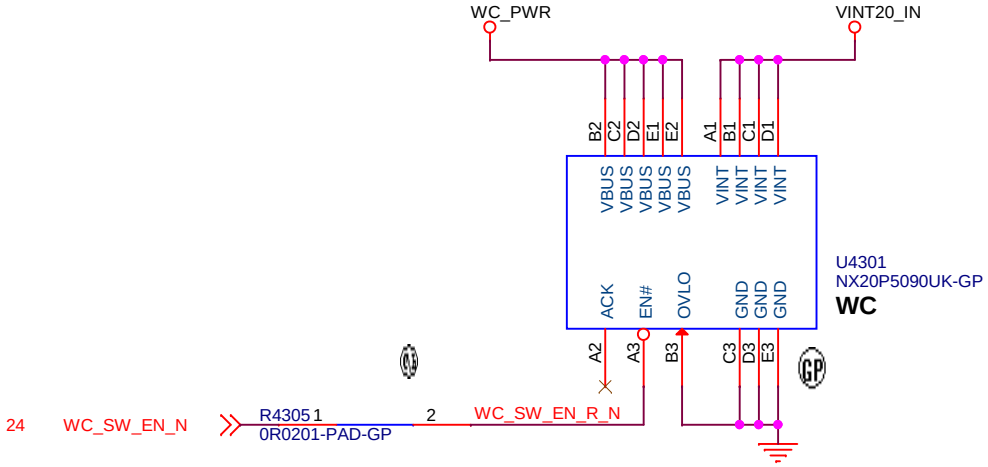
TEST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: INT IO (RSVD)		
Size: A3	Document Number: V550_TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 42 of 106	

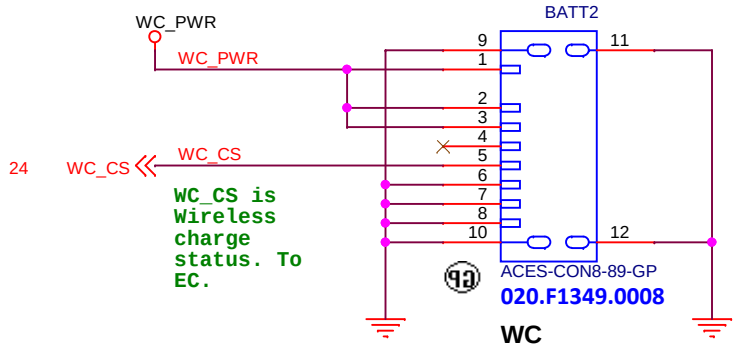
Main Battery Connector







BATT2 is for Wireless Charge. ("WC" default DY)



TEST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**INT IO (ATX/ DC/ BATT Conn)**	
Size A4	Document Number **V550_TGL**	Rev **-1**
Date: Monday, July 27, 2020	Sheet 43 of 106	

OFFPAGE - PIC - EE

PH on EE Side

24,43 BAT_SCL_EC → BAT_SCL_EC

24,43 BAT_SDA_EC → BAT_SDA_EC

PH on EE Side

24,46,73 PROCHOT_CPU_N → PROCHOT_CPU_N

46 CHGR_PSYS_IMVP → CHGR_PSYS_IMVP

24 PWR_AC_IN_N → PWR_AC_IN_N

24 PWR_CHG_IMON → PWR_CHG_IMON

Device will be transition from normal Buck-Boost operation to PTM operation by:
- Set REG0x17[7] = 0, to disable the EN_EXIT ILIM.
- Set REG0x30[0] = 1
- Set REG0x30[2] = 1
- Ground ILIM_HIZ pin

Device will transition out of PTM mode with host control by:
- Set REG0x30[2] = 0
- Pull ILIM_HIZ pin to high.
- Device exits PTM to buck-boost operation if tripping VinDPM or IinDPM.
- Device exits PTM to buck-boost operation under fault conditions (ACOC, TSHUT, BATOC).

BAT_SCL_EC ↔ PWR_CHG_SCL

BAT_SDA_EC ↔ PWR_CHG_SDA

PWR_CHG_IMON ↔ PWR_CHG_IADP

PROCHOT_CPU_N ↔ PWR_PROCHOT#_CPU

CHGR_PSYS_IMVP ↔ CHGR_CHG_PSYS

For Adapter IN
Confirm with EE

	PR4465	PR4464
TypeC+Tradition	上件	DY
Non-TypeC	DY	上件

VAP support for BQ25710

075.00046.0073

075.00046.0073

2.2uH,
DCR=14-16.5mohm,
Idc=10A, Isat=13A
10.3*11.3*3mm

	V(ILIM)	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

Reserve for Power test

Reserve for PTM
If it hasn't more GPIO

# of CELL	VCELL_PRES	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

$V_{PSYS} = R_{PSYS} \times K_{PSYS}(V_{ACP} \times I_{IN} + V_{BAT} \times I_{BAT})$

84.2N702.J31
2nd = 84.2N702.W31
3rd = 84.2N702.031

0505
buyer: 7"

STD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BQ25710R_Charger

Size: A1 | Document Number: V550_TGL | Rev: -1

Date: Monday, July 27, 2020 | Sheet 64 of 105

OFFPAGE-Signal

PWR_3D3V_LDO — R4502 0R0402-PAD-1-GP — PWR_3D3V_EN

PH on EE Side

PWR_3D3V_PG

24 5V_EN — R4503 0R0402-PAD-1-GP — PWR_5V_EN

PH on EE Side

PWR_5V_PG

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_3D3V

PG4515 GAP-CLOSE-PWR-3-GP
PG4516 GAP-CLOSE-PWR-3-GP
PG4517 GAP-CLOSE-PWR-3-GP
PG4518 GAP-CLOSE-PWR-3-GP

3D3V_AUX_S5 — PWR_3D3V

PG4519 GAP-CLOSE-PWR-3-GP
PG4520 GAP-CLOSE-PWR-3-GP
PG4521 GAP-CLOSE-PWR-3-GP
PG4522 GAP-CLOSE-PWR-3-GP
PG4523 GAP-CLOSE-PWR-3-GP
PG4524 GAP-CLOSE-PWR-3-GP

19V_DCBATOUT — PWR_DCBATOUT_5V

PG4552 GAP-CLOSE-PWR-3-GP
PG4553 GAP-CLOSE-PWR-3-GP
PG4555 GAP-CLOSE-PWR-3-GP
PG4557 GAP-CLOSE-PWR-3-GP
PG4559 GAP-CLOSE-PWR-3-GP
PG4561 GAP-CLOSE-PWR-3-GP

5V_S5 — PWR_5V

PG4551 GAP-CLOSE-PWR-3-GP
PG4554 GAP-CLOSE-PWR-3-GP
PG4556 GAP-CLOSE-PWR-3-GP
PG4558 GAP-CLOSE-PWR-3-GP
PG4560 GAP-CLOSE-PWR-3-GP
PG4563 GAP-CLOSE-PWR-3-GP
PG4564 GAP-CLOSE-PWR-3-GP
PG4566 GAP-CLOSE-PWR-3-GP

5V_AUX_S5 — PWR_5V_LDO

PG4565 GAP-CLOSE-PWR-3-GP

IDC : 6A
OCP : 8A

Hybrid/NVDC4串BT Need Change Solution

Vin Operating range : 4~24V
Vin_Max : 26V

Ilimt : 8A

PWR_3D3V_LDO — PR4516 0R2J-2-GP — PWR_3D3V_VCC

PR4501 0R0603-PAD-1-GP-U — PWR_3D3V_BOOT — PWR_3D3V_BOOT_A — PC4506 SCD1U25V2KX-L-GP

PC4522 SC2D2U10V3KX-L-GP

PWR_DCBATOUT_3D3V

Close to PU4501

PC4503 SC10U6D3V3KX-L-GP
PC4502 SC10U6D3V3KX-L-GP
PC4513 SCD1U25V2KX-L-GP

PU4501 TPS51393PRJER-GP

VIN, VIN, VIN, VIN — VCC
SW#6, SW#19, SW#20 — PWR_3D3V_PH
NC#10, LDO, NC#16 — PWR_3D3V_LDO_A
EN, ENLDO — PWR_3D3V_EN, PWR_3D3V_EN2
BOOT, PGOOD, FB, VOUT — PWR_3D3V_BOOT, PWR_3D3V_PG, PWR_3D3V_FB
GND, GND, GND, GND

PL4501 IND-1D5UH-22-GP-U

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PR4515 0R0402-PAD-1-GP — PWR_3D3V_LDO

PC4507 SC10U6D3V3MX-L-GP

PWR_3D3V

PC4509 PC4510 PC4511 PC4512 SC22U6D3V3MX-L-GP
PC4514 SC22U6D3V3MX-L-GP

PR4514 PR4R2J-1-GP

Place another side , make GND plan bigger

	TPS51393	JW5068B
PR4515	上件	DY
PR4516	DY	上件

EN rating :5 .5V
ENLDO Rising Threshold :1.5V
ENLDO Falling Threshold : 0.8V
EN Rising Threshold :1.3V
EN Falling Threshold : 1.12V

PWR_DCBATOUT_3D3V — PR4512 300KR2J-GP — PR4513 100KR2J-1-GP

DY PR4505 100KR2J-1-GP — 3D3V_AUX_S5

Trace used 10 mil

PWR_3D3V_VOUT

Close to PC4511

PG4530 GAP-CLOSE-PWR-3-GP

PC4526 SC470P50V2KX-L-GP — PWR_3D3V_FB2 — PR4506 240KR2F-L-GP

PWR_3D3V_PH

DY PR4517 2D2R6J-3-GP

PWR_3D3V_SNB

DY PC4527 SC1500P50V2KX-2GP

IDC:8A

Vin Operating range : 4~24V
Vin_Max : 26V

Ilimt : 8A

Hybrid/NVDC4串BT Need Change Solution

5V_AUX_S5 — PR4552 100KR2J-1-GP DY

Place another side , make GND plan bigger

PWR_DCBATOUT_5V

Close to PU4551

PC4555 SC10U25V5KX-L-GP
PC4554 SC10U25V5KX-L-GP
PC4564 SCD1U25V2KX-L-GP

PU4551 TPS51395PRJER-GP

VIN, VIN, VIN, VIN — PGOOD — PWR_5V_PG
BOOT — PWR_5V_BOOT
SW#6, SW#19, SW#20 — PWR_5V_PH
NC#10, NC#16
VOUT — PWR_5V_VOUT
FB — PWR_5V_FB
LDO — PWR_5V_LDO
VCC — PWR_5V_VCC
EN — PWR_5V_EN
ENLDO — PWR_5V_EN2
GND, GND, GND, GND

PR4554 0R0603-PAD-1-GP-U — PC4553 SCD1U25V2KX-L-GP — PWR_5V_BOOT_A

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PL4551 IND-1D5UH-23-GP-U

PWR_5V

PC4556 PC4557 PC4558 PC4559 PC4560 PC4561 SC22U6D3V3MX-L1-GP

Trace used 10 mil

PG4562 GAP-CLOSE-PWR-3-GP

PC4563 SC1KP50V2KX-L-1-GP — PWR_5V_FB_A — PR4555 324KR2F-GP — PWR_5V_LDO

PC4562 SC2D2U10V3KX-L-GP

PR4556 1MR2J-1-GP

PWR_DCBATOUT_5V — PR4511 300KR2J-GP — PR4510 100KR2J-1-GP

PC4551 SC10U6D3V3MX-L-GP

PWR_5V_PH

DY PR4557 2D2R6J-3-GP

PWR_5V_SNB

DY PC4566 SC1500P50V2KX-2GP

EN rating :5 .5V
ENLDO Rising Threshold :1.5V
ENLDO Falling Threshold : 0.8V
EN Rising Threshold :1.3V
EN Falling Threshold : 1.12V

STD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51393/TPS51395R_5V/3D3V

Size: A2 | Document Number: V550_TGL | Rev: -1

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OFFPAGE

PH on CPU side
PROCHOT_CPU_N
SVID_CLK_CPU
SVID_DATA_CPU
SVID_ALERT_CPU_N
PWR_VCORE_VR_EN
VCORE_PG
PH on CPU side
VCORE_READY
PWR_VCORE_VR_READY
VSSCORE_SENSE
VCCCORE_SENSE
CHGR_PSYS_IMVP
EE side Link
SVID Pull High V
1D05V_VCCST
PWR_VCORE_VCCST

Reserve for Power test

ICL
VBOOT=1.8V
Fsw=568kHz@VIN=7.4V
ICCMAX=72A
Disable QR
Disable DVID LIFT

TGL
VBOOT=0V
Fsw=568kHz@VIN=7.4V
ICCMAX=66A
Disable QR
Disable DVID LIFT

	ICL IccMax=72A	TGL IccMax=66A
PR4619	3.57K	1.4K
PR4666	357	0
PR4624	3.48K	1.02K
PR4669	100	100

TGL_28W測試單板 VBOOT = 1.8V
PR4666 = 2.74kohm
PR4624 = 3.24kohm

TGL_15W單板測試VBOOT = 1.8V
PR4619 = 1.4 kohm
PR4666 = 3.92 kohm
PR4624 = 2.87 kohm
PR4669 = 10 ohm

VR_HOT Thermal_Alert#	100C/97C	Lily 120C/100C
PR4627	24.9K	36.5K
PR4622	12.4K	17.8K
PR4701	110K	3.48K

	電感3/而 0.9mohm	電感4/而 0.66mohm
PR4628 PR4633	2K	2K
PR4655 PR4646	2K	2K
PR4662 PR4665	2.61K	4.64K

0603 Size

0603 Size

電感3/而 0.9mohm	ICL IccMax=72A	TGL IccMax=66A
PR4640	31.6K	34K

LL/IMON Compesation
NCP15XH103F03RC
Need confirm with RT If you change Chock
Close to PL4701
B = 4250

電感3/而 0.9mohm	ICL IccMax=72A	TGL IccMax=66A
PR4601	26.7K	30.1K
PR4665	2.87K	2.05K
PR4643	17.8K	18.7K

C550

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT3612EB_VCORE(1/2))

Size: N1 | Document Number: V550_TGL | Rev:

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OFFPAGE

19V_DCBATOUT
PWR_DCBATOUT_VCOREA
PG4702 GAP-CLOSE-PWR-3-GP
PG4703 GAP-CLOSE-PWR-3-GP
PG4704 GAP-CLOSE-PWR-3-GP
PG4705 GAP-CLOSE-PWR-3-GP
PG4706 GAP-CLOSE-PWR-3-GP
PG4707 GAP-CLOSE-PWR-3-GP
PT4703 ST22U25VBM-GP

19V_DCBATOUT
PWR_DCBATOUT_VCOREB
PG4710 GAP-CLOSE-PWR-3-GP
PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP
PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP
PG4715 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCOREA
PC4704 SC10U25V3MX-GP
PC4705 SC10U25V3MX-GP
PC4706 SC10U25V3MX-GP
PC4707 SC10U25V3MX-GP

PR4701 3K40R2F-GP
PR4703 NTC-100K-12-GP-U
B = 4250
Close to Phase1 Mosfet
46 PWR_VCORE_TSEN_A
PWR_VCORE_TSEN 46

5V_S5
PR4702 2D2R2F-GP
PWR_VCORE_VCCA
PC4731 SC1U10V2KX-L1-GP
PC4702 SC1U10V2KX-L1-GP

PU4701 AOZ5516QI-GP
VCC PVCC VIN VIN VIN VIN
NC#31 PWM FCCM NC#30 NC#6 GL#27 GL#35
NC#4 PGND
BOOT PHASE
VSWH#16 VSWH#17 VSWH#18 VSWH#19 VSWH#20 VSWH#21 VSWH#22 VSWH#23 VSWH#24 VSWH#25 VSWH#26

PR4707 0R0402-PAD-1-GP
PWR_VCORE_PWMA
PR4708 0R0402-PAD-1-GP
PWR_VCORE_ZCD_EN#A
46 PWR_VCORE_PWM1
46,47 PWR_VCORE_DRVEN

PWR_VCORE_BOOTA
PC4703 SCD22U25V3KX-GP
PWR_VCORE_BOOTA_A
PR4706 2D2R3-1-U-GP
PWR_VCORE_PHA
Cyntec. 6.8*7.6*2.4
DCR: 0.92 +- 7% mOhm
Idc : 37A , Isat : 41A
PL4701 COIL-D15UH-8-GP
1V_CPU_CORE
PG4708 GAP-CLOSE-PWR-3-GP
PG4709 GAP-CLOSE-PWR-3-GP
PT4701 ST470U2D5VDM-14-GP
46 PWR_VCORE_ISEN1P_A
46 PWR_VCORE_ISEN1N_A

PWR_VCORE_PHA
DY PR4709 2D2R5J-1-GP
PWR_VCORE_SNBA
DY PC4701 SC1KP50V2KX-L-1-GP

Design Current=39A
Icc(max)=70A
OCP>93A

PWR_DCBATOUT_VCOREB
PC4710 SC10U25V3MX-GP
PC4711 SC10U25V3MX-GP
PC4712 SC10U25V3MX-GP
PC4713 SC10U25V3MX-GP

5V_S5
PR4710 2D2R2F-GP
PWR_VCORE_VCCB
PC4734 SC1U10V2KX-L1-GP
PC4708 SC1U10V2KX-L1-GP

PU4702 AOZ5516QI-GP
VCC PVCC VIN VIN VIN VIN
NC#31 PWM FCCM NC#30 NC#6 GL#27 GL#35
NC#4 PGND
BOOT PHASE
VSWH#16 VSWH#17 VSWH#18 VSWH#19 VSWH#20 VSWH#21 VSWH#22 VSWH#23 VSWH#24 VSWH#25 VSWH#26

PR4712 0R0402-PAD-1-GP
PWR_VCORE_PWMB
PR4713 0R0402-PAD-1-GP
PWR_VCORE_ZCD_EN#B
46 PWR_VCORE_PWM2
46,47 PWR_VCORE_DRVEN

PWR_VCORE_BOOTB
PC4709 SCD22U25V3KX-GP
PWR_VCORE_BOOTB_A
PR4711 2D2R3-1-U-GP
PWR_VCORE_PHB
Cyntec. 6.8*7.6*2.4
DCR: 0.92 +- 7% mOhm
Idc : 37A , Isat : 41A
PL4702 COIL-D15UH-8-GP
1V_CPU_CORE
PG4701 GAP-CLOSE-PWR-3-GP
PG4716 GAP-CLOSE-PWR-3-GP
46 PWR_VCORE_ISEN2P_A
46 PWR_VCORE_ISEN2N_A

PWR_VCORE_PHB
DY PR4714 2D2R5J-1-GP
PWR_VCORE_SNBB
DY PC4714 SC1KP50V2KX-L-1-GP

C550

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (AOE6936_VCORE(2/2))
Size: A2 | Document Number: V550_TGL | Rev:
Date: Monday, July 27, 2020 | Sheet 47 of 106

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (VCCIN_AUX_CPUCORE(3/3))

Size	Document Number	Rev
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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Power (RSVD)

Size	Document Number	Rev
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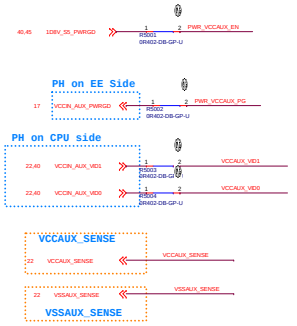
OFFPAGE



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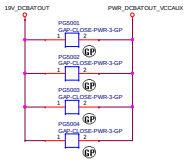

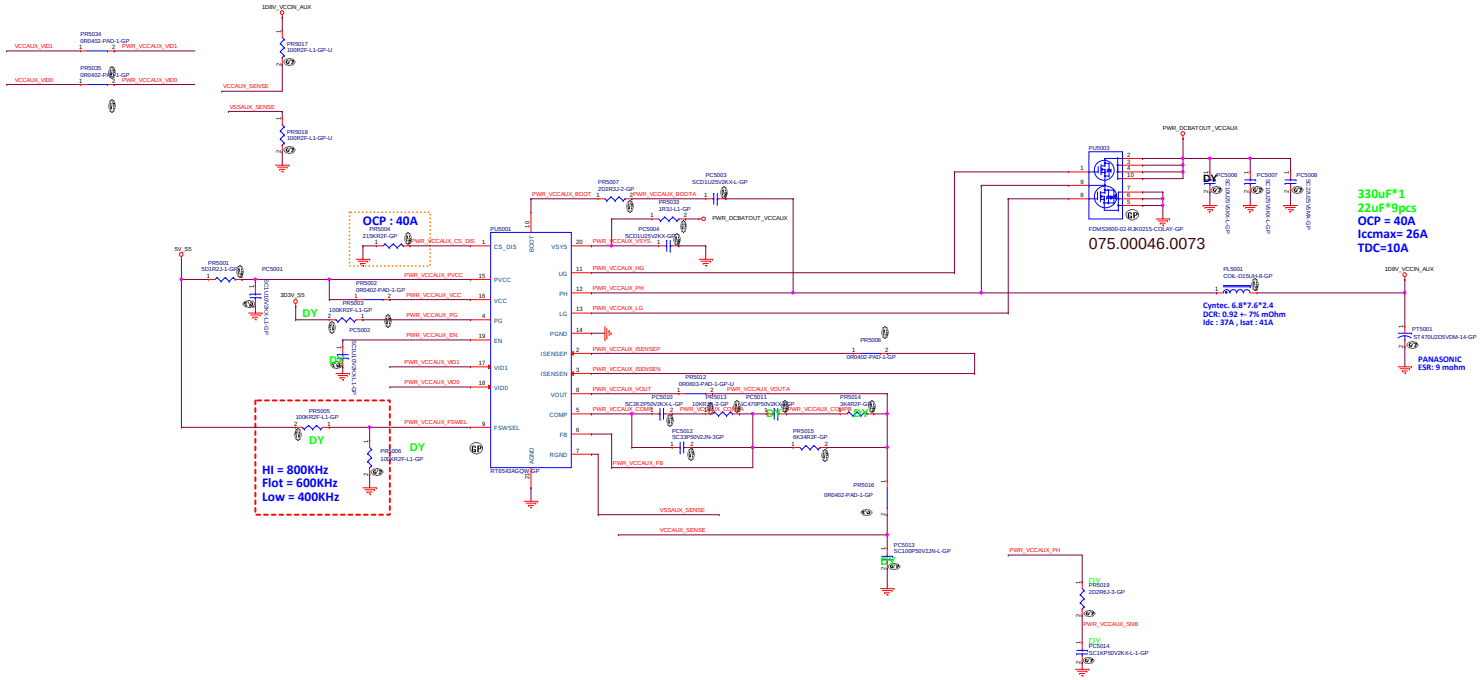

STD

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT6543_VCCAUX		
Size: A1	Document Number: V550_TGL	Rev: -1
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OFFPAGE

S5
40 PWR_VDDQ_EN → PWR_VDDQ_EN

S3(VTT_CNTL)
40 PWR_VTT_EN → R5102 0R402-DB-GP-U → PWR_VDDQVTT_EN

PH on EE Side
40 PWR_VDDQ_PG → PWR_VDDQ_PG

OFFPAGE_GAP

19V_DCBATOUT → PG5119 GAP-CLOSE-PWR-3-GP → PWR_DCBATOUT_VDDQ
PG5123 GAP-CLOSE-PWR-3-GP
PG5127 GAP-CLOSE-PWR-3-GP

1D1V_S3 → PG5131 GAP-CLOSE-PWR-3-GP → PWR_VDDQ
PG5132 GAP-CLOSE-PWR-3-GP
PG5121 GAP-CLOSE-PWR-3-GP
PG5120 GAP-CLOSE-PWR-3-GP
PG5125 GAP-CLOSE-PWR-3-GP
PG5122 GAP-CLOSE-PWR-3-GP
PG5129 GAP-CLOSE-PWR-3-GP
PG5130 GAP-CLOSE-PWR-3-GP

1D1V_S3 → PG5124 GAP-CLOSE-PWR-3-GP → PWR_VDDQ_VLDOIN

0D6V_S3 → R5103 0R402-DB-GP-U → PG5128 GAP-CLOSE-PWR-3-GP → PWR_VDDQVTT

1D8V_S3 → PG5126 GAP-CLOSE-PWR-3-GP → PWR_VDDQ1D8V

PWR_DCBATOUT_VDDQ
EC5102 SCD1U25V2KX-L-GP
PC5101 SC10U25V5KX-L-GP
PC5102 SC10U25V5KX-L-GP
PC5117 SCD1U25V2KX-L-GP

PWR_VDDQ_BOOT_A
PR5109 5D1R3J-GP
PC5108 SCD1U25V2KX-L-GP
PWR_VDDQ_BOOT

PWR_VDDQ_VLDOIN
PC5103 SC10U6D3V3MX-L-GP

5V_S5
PR5110 0R0402-PAD-1-GP
PR5107 0R0402-PAD-1-GP
PWR_VDDQ_VCC
PC5116 SC1U10V2KX-L1-GP
PWR_VDDQ_VDD1
PC5104 SC10U6D3V3MX-L-GP
PC5118 SCD1U16V2KX-L-GP
PC5118 put as close as TPS51487 pin14
PWR_VDDQ_PG
PWR_VDDQ_EN
PWR_VDDQVTT_EN

PU5101
PVIN
VLDOIN
VCC_5V
PIN_VDD1
PG
VDDEN
VDDQEN
BST
SW
VDD2SNS
VDDQ
VDDQSNS
VDDQREF
SW_VDD1
VDD1SNS
PGND_VDD1
PGND
AGND
*PWR_VDDQ_PH
*PWR_VDDQ_SENSE
*PWR_VDDQVTT_SENSE
*PWR_VDDQ_VDDQREF
*PWR_VDDQ1D8V_PH
*PWR_VDDQ1D8V_SENSE
TPS51487XRJER-GP

Cyntec, 6.6 x 7.3 x 3.0 mm
DCR: 4.8~5.3 mOhm
Idc : 16 A , Isat : 17 A
PL5101 COIL-D68UH-9-GP
PWR_VDDQ
PC5109 SC5C22E60J6MX-L1-GP
PC5110 SC5C22E60J6MX-L1-GP
PC5111 SC5C22E60J6MX-L1-GP
PC5112 SC5C22E60J6MX-L1-GP
PC5115 SC5C22E60J6MX-L1-GP
PR5106 2D2R3J-2-GP
PWR_VDDQ_SNB
PC5114 SC1500P50V2KX-2GP
PG5133 GAP-CLOSE-PWR-3-GP

PWR_VDDQVTT
PC5107 SC10U6D3V3MX-L-GP
PR5104 0R0402-PAD-1-GP
PC5106 SC1U10V2KX-L1-GP

Murata, 2.5 x 2.0 x 1.2 mm
DCR:240m Ohm
Idc : 1.3 A , Isat : 1.5 A
PL5103 IND-4D7UH-352-GP
PWR_VDDQ1D8V
PC5105 SC5C22E60J6MX-L1-GP
PR5103 0R0402-PAD-1-GP

STD

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51487_VDDQ/VTT/VPP		
Size: A2	Document Number: V550_TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 51 of 106	

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RSVD

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PH on EE Side

40,50 1D8V_S5_PWRGD — R5301 0R402-DB-GP-U — PWR_1D8V_PG

40 1D8V_S5_EN — R5302 0R402-DB-GP-U — PWR_1D8V_EN

OFFPAGE_GAP

3D3V_S5 — PG5301 GAP-CLOSE-PWR-3-GP — PWR_1D8V_VIN

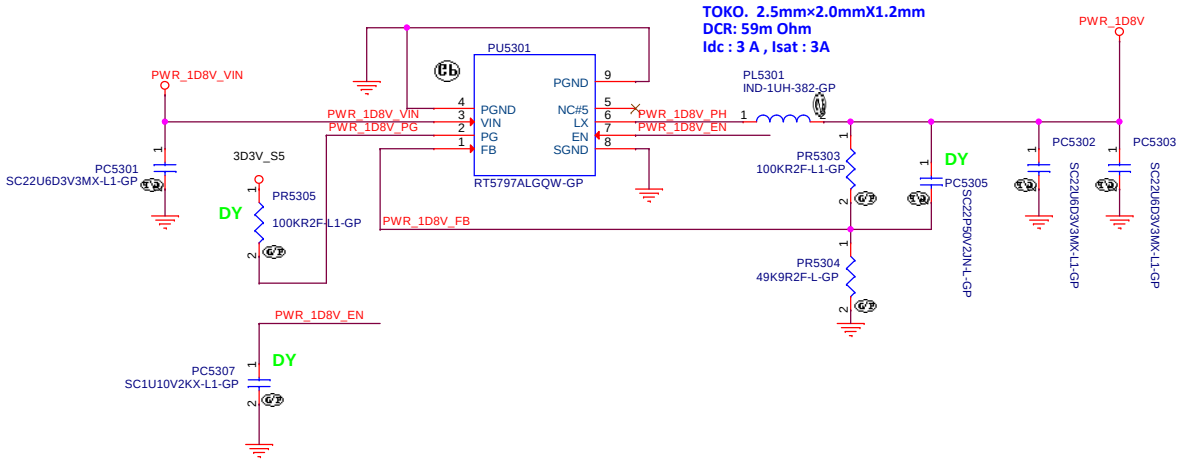
PG5302 GAP-CLOSE-PWR-3-GP

1D8V_S5 — PG5303 GAP-CLOSE-PWR-3-GP — PWR_1D8V

PG5304 GAP-CLOSE-PWR-3-GP

PG5305 GAP-CLOSE-PWR-3-GP

TDC=2A
Imax= 3A



STD

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT5797_1D8V		
Size: A3	Document Number: V550_TGL	Rev: -1
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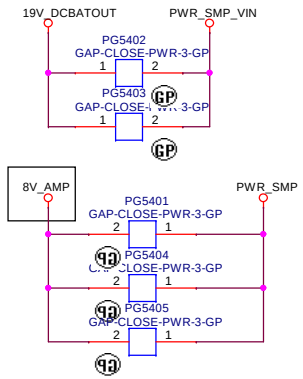
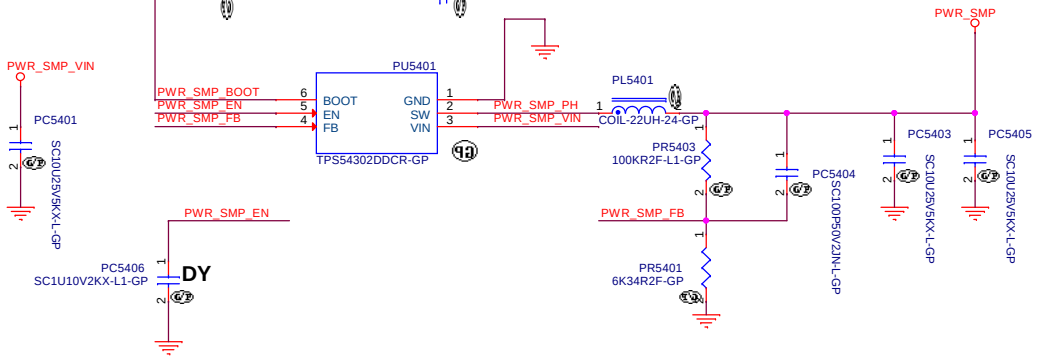
OFFPAGE

17,24,40,57 PM_SLP_S3_N — R5402 0R0402PAD-1-GP — PWR_SMP_EN

OFFPAGE_GAP



TDC=0.7A
Imax= 2.25A



C550

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER TPS54302D		
Size: A3	Document Number: V550_TGL	Rev:
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EDP

4 eDP_AUX_CPU_P
4 eDP_AUX_CPU_N
4 eDP_TX_CPU_N3
4 eDP_TX_CPU_P3
4 eDP_TX_CPU_N2
4 eDP_TX_CPU_P2
4 eDP_TX_CPU_N1
4 eDP_TX_CPU_P1
4 eDP_TX_CPU_N0
4 eDP_TX_CPU_P0

4 eDP_HPD_CPU
4,55 eDP_BLCTRL_CPU
24 LCD_BLEN_CON

INVERTER POWER

19V_DCBATOUT
F5501 FUSE-3A32V-29-GP
69.43001.491
19V_DCBATOUT_LCD
(500mA, Peak 1.5A)
C5501 SCD1U25V2KX-1-GP
C5502 SCU25V2KX-2-GP
C5523 SCU25V2KX-2-GP

3D3V_S0
DY
R5523 1KR2J-1-GP
R5524 33R2J-2-GP
4,55 eDP_BLCTRL_CPU
LCD_BRIGHTNESS
C5518 SC100P50V2JN-L-GP

Discharge circuit

3D3V_S5
R5525 10KR2F-2-GP
DISC_3D3V_LCD_ON
Q5501 LTC024EUB-FS8-GP
84.00024.A1K
4,40 eDP_VDDEN_CPU

3D3V_LCD_S0
R5526 10R3J-3-GP
DISC_3D3V_LCD
Q5502 2N7002K-2-GP
84.2N702.J31

3D3V_LCD_S0
R5527 DY 10KR2F-2-GP LCD_BLEN_CON
R5528 DY 100KR1J-GP LCD_BLEN_CON
R5502 100KR1J-GP eDP_HPD_CPU
R5505 DY 100KR1J-GP eDP_BLCTRL_CPU

3D3V_LCD_S0 Layout 40 mil.
3D3V_LCD_S0 19V_DCBATOUT_LCD
LCD1 ACES-CON40-18-GP
LCD_BRIGHTNESS
LCD_BLEN_CON
eDP_HPD_CON R5510 0R0201-PAD-GP eDP_HPD_CPU
eDP_AUX_CON_N C5507 SCD1U16V2KX-3GP eDP_AUX_CPU_N
eDP_AUX_CON_P C5509 SCD1U16V2KX-3GP eDP_AUX_CPU_P
eDP_TX_CON_P0 C5506 SCD1U16V2KX-3GP eDP_TX_CPU_P0
eDP_TX_CON_N0 C5505 SCD1U16V2KX-3GP eDP_TX_CPU_N0
eDP_TX_CON_P1 C5504 SCD1U16V2KX-3GP eDP_TX_CPU_P1
eDP_TX_CON_N1 C5503 SCD1U16V2KX-3GP eDP_TX_CPU_N1
eDP_TX_CON_P2 C5521 SCD1U16V2KX-3GP eDP_TX_CPU_P2
eDP_TX_CON_N2 C5522 SCD1U16V2KX-3GP eDP_TX_CPU_N2
eDP_TX_CON_P3 C5519 SCD1U16V2KX-3GP eDP_TX_CPU_P3
eDP_TX_CON_N3 C5520 SCD1U16V2KX-3GP eDP_TX_CPU_N3

Touch

16 TOUCH_USB20_P
16 TOUCH_USB20_N
20 TOUCH_STOP_N
24 TOUCH_PWR_EN

(300mA)
3D3V_TOUCH_S0
3V_TOUCH_S0_FIP
R5521 0R402-DB-GP-U
Max 2A
U5502 G517F1T12U-GP
074.51712.009F
OUT GND OC# IN EN
3D3V_AUX_S5
TOUCH_PWR_EN
C5515 SC68D3V2MX-GP-U
C5516 SCD1U16V2KX-1-GP
C5517 SC4D7U6D3V2MX-GP-U

3D3V_TOUCH_S0
TOUCH1 HRS-CON6-15-GP
020.K0237.0006
TOUCH_STOP_N
TOUCH_USB20_N
TOUCH_USB20_P
DY-EMC ED5502 AZ5725-01FDRTG1-GP
DY-EMC ED5501 AZ5725-01FDRTG1-GP

TEST

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Inverter)
Size: C
Document Number: V550_TGL
Rev: -1
Date: Monday, July 27, 2020
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TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RSVD

Size	Document Number	Rev
A4	V550_TGL	-1

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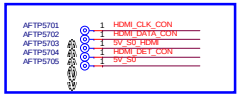
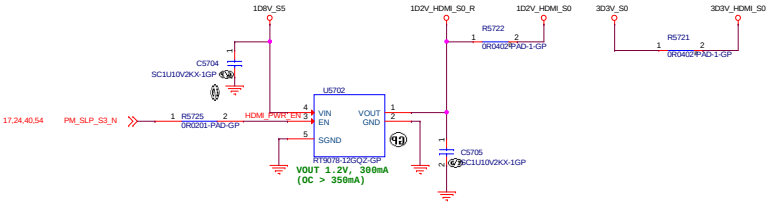
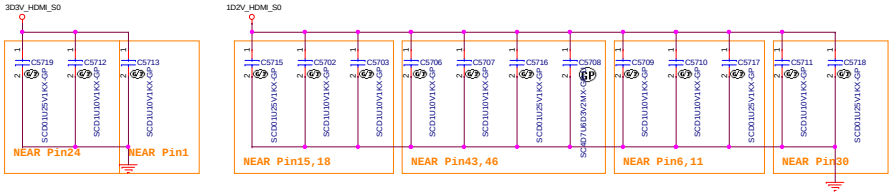
SSID = HDMI

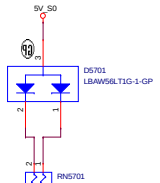
HDMI CONNECTOR

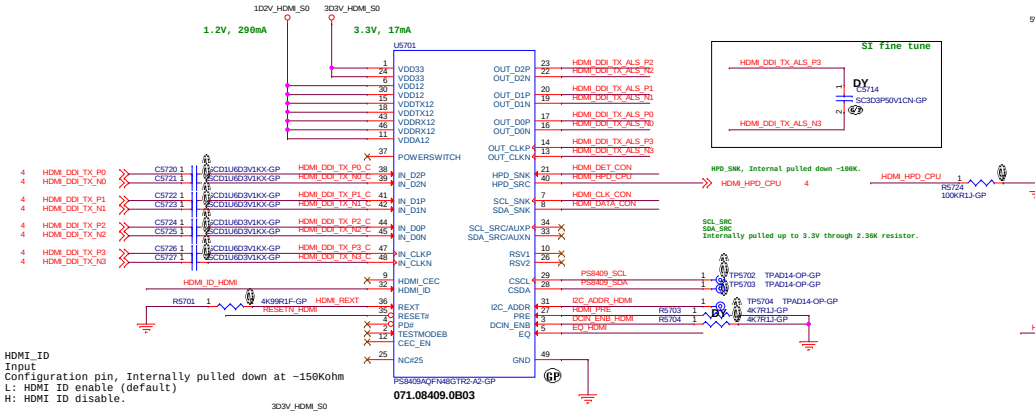
Test point

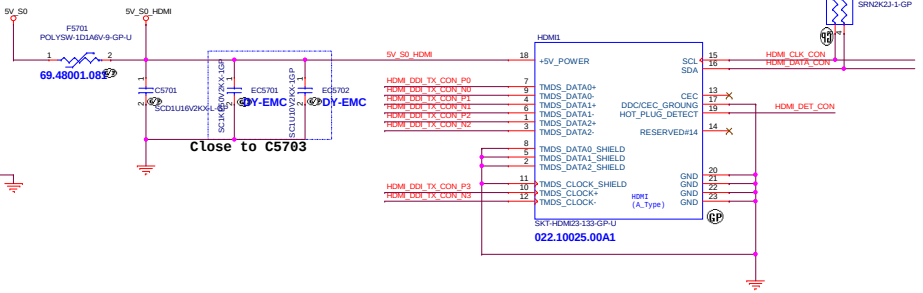






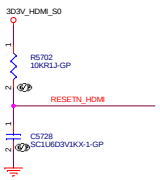






HDMI_ID
Input
Configuration pin, Internally pulled down at ~150Kohm
L: HDMI ID enable (default)
H: HDMI ID disable.

RESETB
Input
Reset, ACTIVE LOW. Internally pulled up at ~150Kohm.

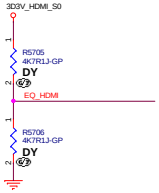


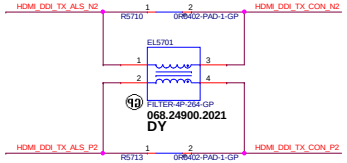
I2C_ADDR
Input
I2C address selection. Internally pulled down at ~150K.
L: Slave address 0x10-0x2F (default)
H: Slave address 0x90-0x9F; 0xD0-0xDF

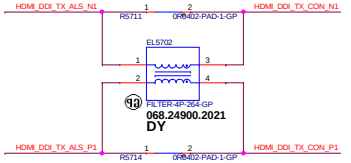
PRE
Input
Output pre-emphasis setting. Internally pulled up at ~150K.
L: Programmable pre-emphasis to 2.5dB.
H: No pre-emphasis (default)

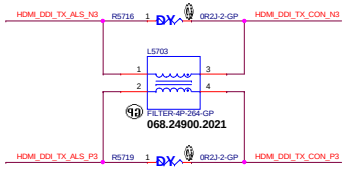
DCIN_ENB
Input
DC coupling enable. Internally pulled up at ~150K.
L: DC coupling input
H: AC coupling input (default)

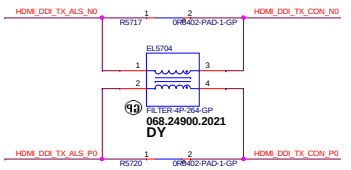
EQ
Input
Receiver equalization setting. Internally pulled up at ~150K.
L: Programmable EQ for channel loss up to 13dB
H: Programmable EQ for channel loss up to 17dB (default)
M: Programmable EQ for channel loss up to 11dB

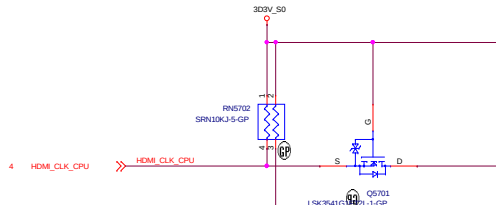




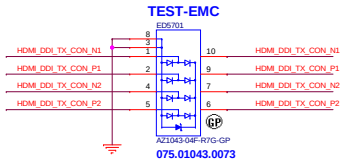




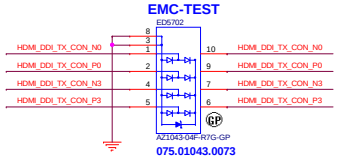




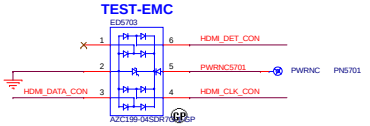
TEST-EMC



EMC-TEST



TEST-EMC



(Amazing 075.00199.007C/AOS 075.08105.007C)

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI CONN		
Size: Custom	Document Number: V550 TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 57 of 106	

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Display (RSVD) DP

Size	Document Number	Rev
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TEST

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Title

Display (RSVD) DVI

Size	Document Number	Rev
A4	V550_TGL	-1

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SSID = SATA

BOM1

緯創資通

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Title

HDD

Size	Document Number	Rev
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Main Func = WLAN

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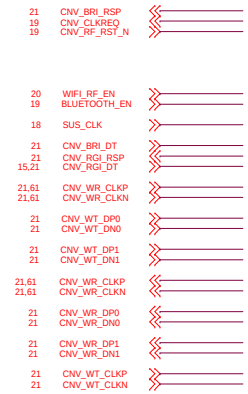

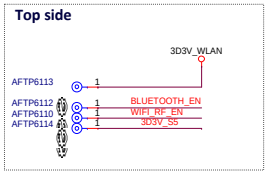

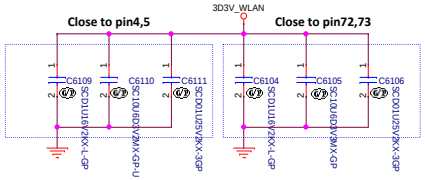

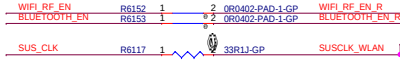

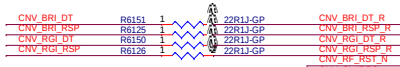

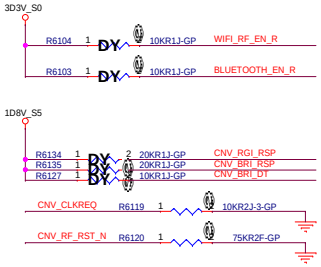

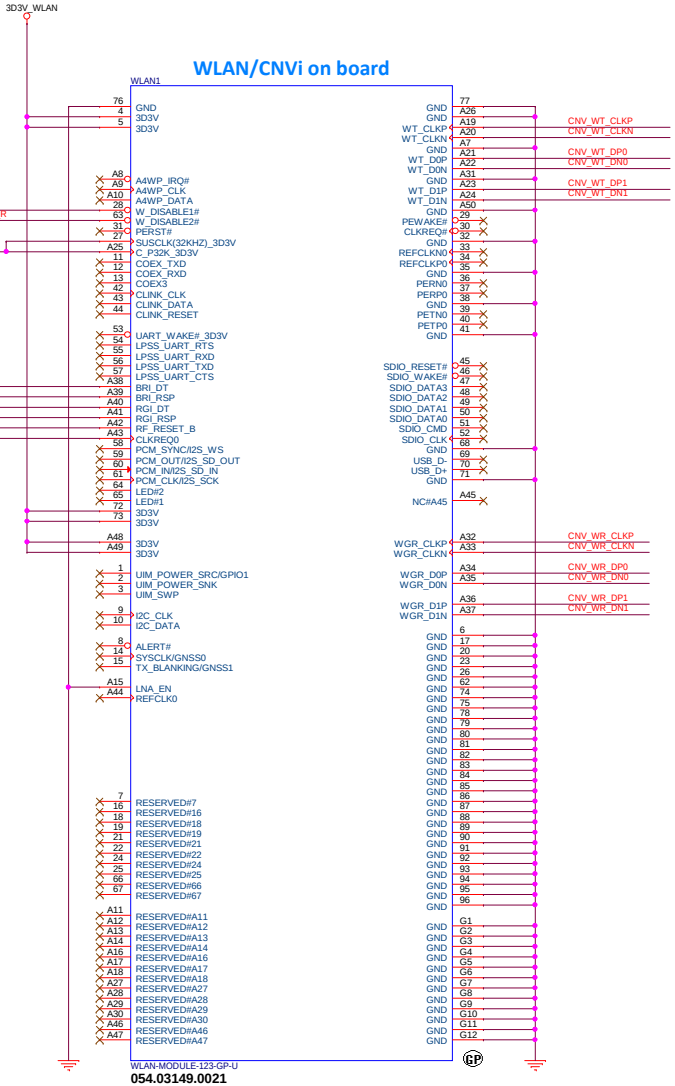

TEST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2)

Size: C | Document Number: V550_TGL | Rev: -1

Date: Monday, July 27, 2020 | Sheet 61 of 106

<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WWAN)

Size	Document Number	Rev
A3	V550_TGL	-1

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Main M.2 SSD

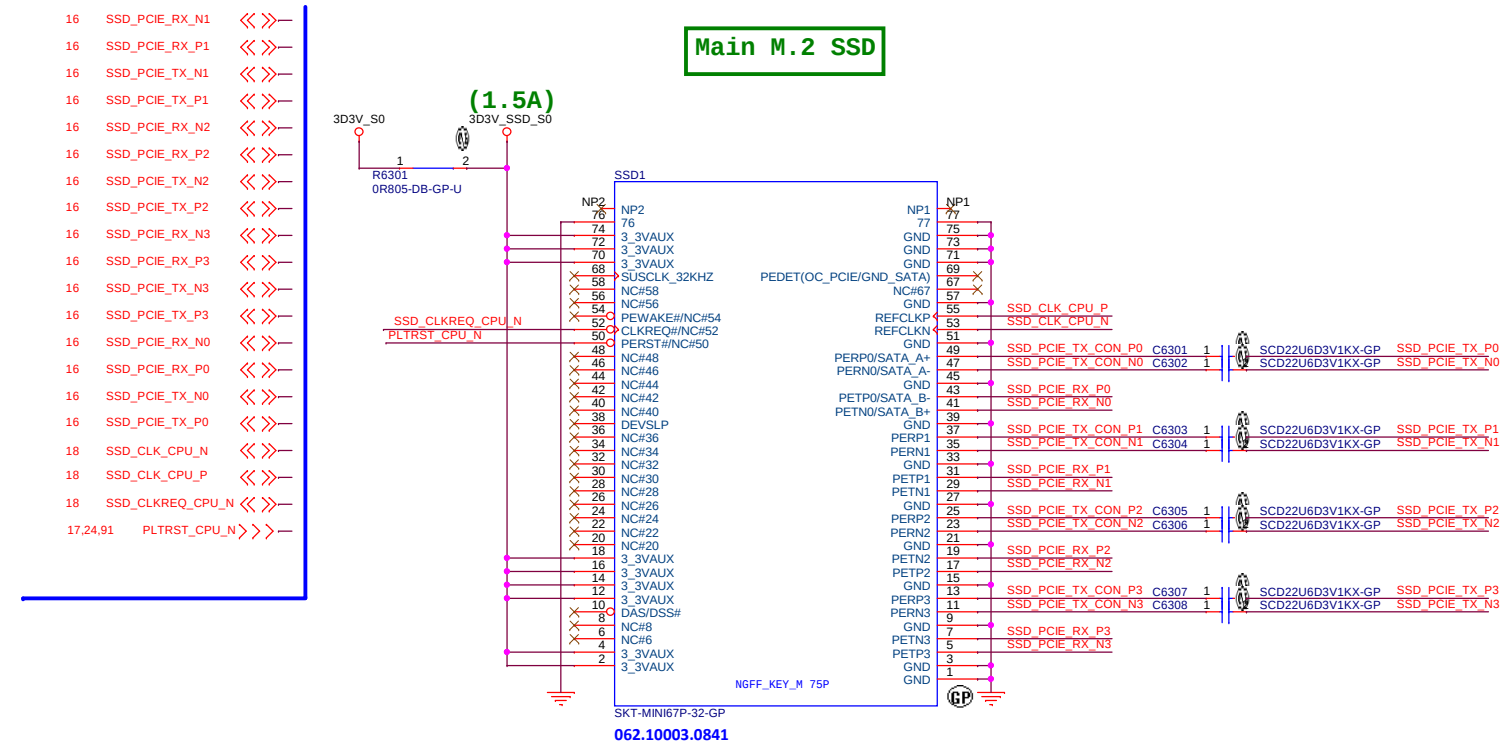

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
		N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

TEST

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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2/ eMMC)

Size: Custom | Document Number: V550_TGL | Rev: -1

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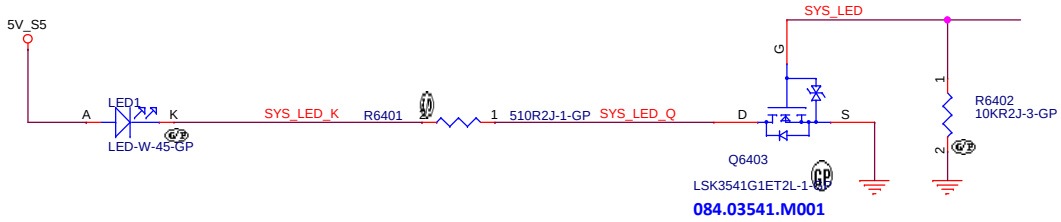
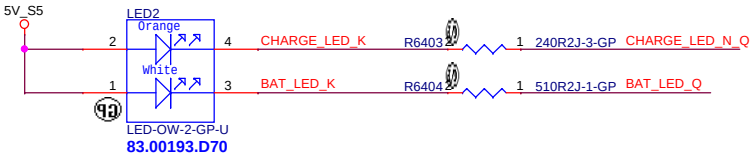
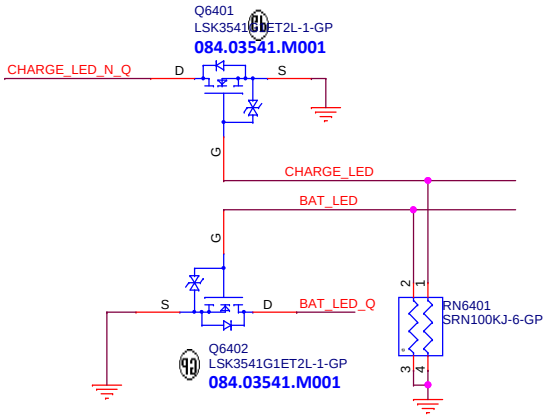
24 BAT_LED
24 SYS_LED
24 CHARGE_LED

SYS LED

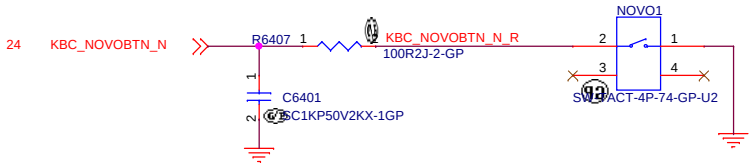


Charge LED





NOVO BUTTON



TEST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED / Button / Power Button		
Size: B	Document Number: V550 TGL	Rev: -1
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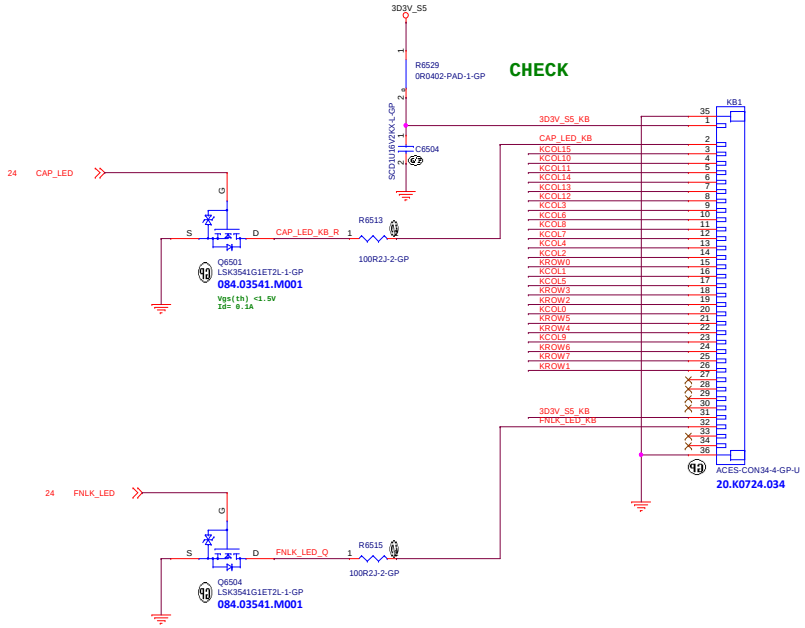
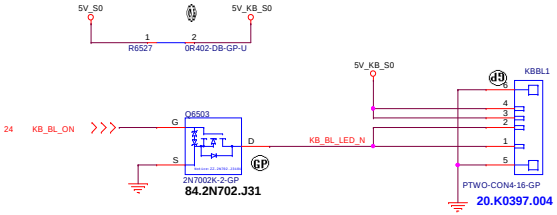
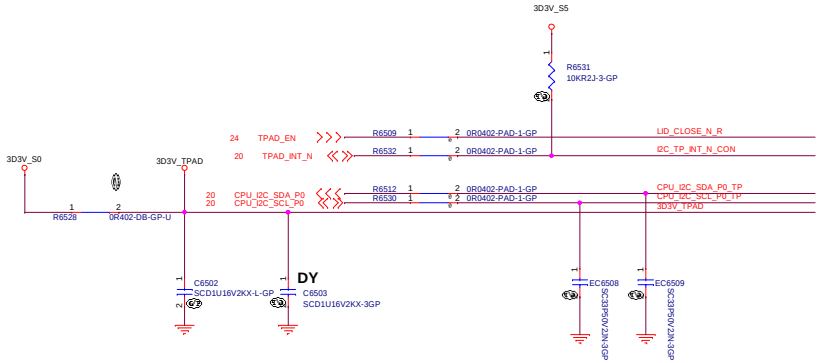
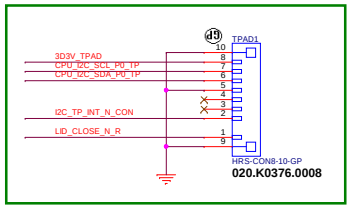
24 KCOL[15:0]

24 KROW[7:0]









TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)

Size: A2 | Document Number: V550_TGL | Rev: -1

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TYPEA Port1 AOU

16 USB1_USB30_TX_N
16 USB1_USB30_TX_P
16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
36 USB1_USB20_AOU_P
36 USB1_USB20_AOU_N

TYPEA Port2

16 USB2_USB30_TX_N
16 USB2_USB30_TX_P
16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB20_P
16 USB2_USB20_N

FP

24 PWR_LED
24 FP_LED
16 FP_USB20_P
16 FP_USB20_N
24 FP_RESETN
24 FP_GPIO_AL0
24 FP_DELINK

Other

24 USB_PWR_EN
16 USB_OC3_N
24 KBC_PWRBTN_N

3D3V_FP — R6605 1 — DY — 0R2J-2-GP — 3D3V_S5
3D3V_FP — R6606 1 — 0R2J-2-GP — 3D3V_AUX_S5

IOBD1
5V_S5 5V_USB1_S5 3D3V_FP 3D3V_S5
41 1 2 3 4 5 6 7 8 9
10 KBC_PWRBTN_N
11
12 FP_RESETN
13 FP_GPIO_AL0
14 FP_DELINK
15 FP_LED
16 PWR_LED
17 USB_PWR_EN
18 USB_OC3_N
19
20 FP_USB20_P
21 FP_USB20_N
22
23 USB1_USB20_AOU_N
24 USB1_USB20_AOU_P
25
26 USB1_USB30_RX_N
27 USB1_USB30_RX_P
28
29 USB1_USB30_TX_N
30 USB1_USB30_TX_P
31
32 USB2_USB20_N
33 USB2_USB20_P
34
35 USB2_USB30_RX_N
36 USB2_USB30_RX_P
37
38 USB2_USB30_TX_N
39 USB2_USB30_TX_P
40
42
KYO-CON8-10-GP
020.K3074.0040

To EC.

KBC_PWRBTN_N — 1 — AFTP6601 AFTE14P-GP

G6601 GAP-OPEN
G6602 GAP-OPEN
TOP

Top side
5V_S5
AFTP6607 AFTP6602 AFTP6603 AFTP6604 AFTP6605 AFTP6606
USB2_USB20_N
USB2_USB20_P
FP_USB20_P
FP_USB20_N

MB to TRANS BD

16 CCD_USB20_P — CCD_USB20_P — R6603 1 — 0R0402-PAD-1-GP — Co-layout — CCD_USB20_CON_P
16 CCD_USB20_N — CCD_USB20_N — R6604 1 — 0R0402-PAD-1-GP — CCD_USB20_CON_N
EL6601
DY-EMC
DLM0NSN900HY2D-GP
068.09002.2001

3D3V_S0 — R6601 1 — 0R402-DB-GP-U — 3D3V_TRANS_S0
(300mA)
C6601 SC4D7U6D3V2MX-GP-U

1D8V_S0 — R6602 1 — 0R402-DB-GP-U — 1D8V_TRANS_S0
3D3V_TRANS_S0
19 DMIC_SDA0_CPU
19 DMIC_SCL0_CPU
CCD_USB20_CON_P
CCD_USB20_CON_N
LCDDB1
HRS-CON8-10-GP
020.K0376.0008

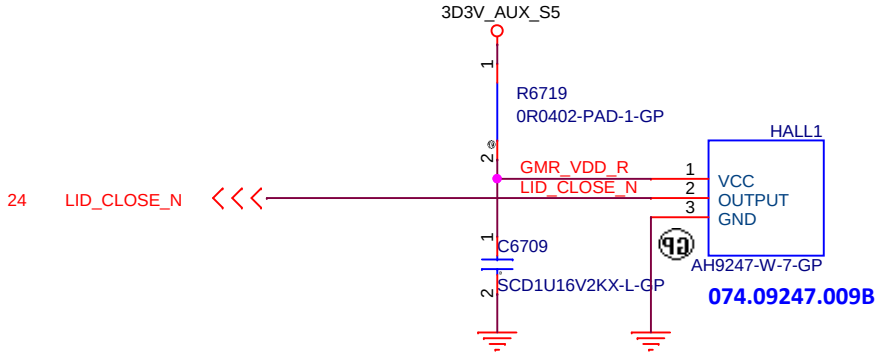
ED6601
CCD_USB20_CON_N 1 — 10 CCD_USB20_CON_N
CCD_USB20_CON_P 2 — 9 CCD_USB20_CON_P
DMIC_SCL0_CPU 4 — 7 DMIC_SCL0_CPU
DMIC_SDA0_CPU 5 — 6 DMIC_SDA0_CPU
AZ1043-04F-R7G-GP
075.01043.0073

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Conn (RSVD)
Size: Custom
Document Number: V550 TGL
Rev: -1
Date: Monday, July 27, 2020
Sheet 66 of 106

Hall Sensor

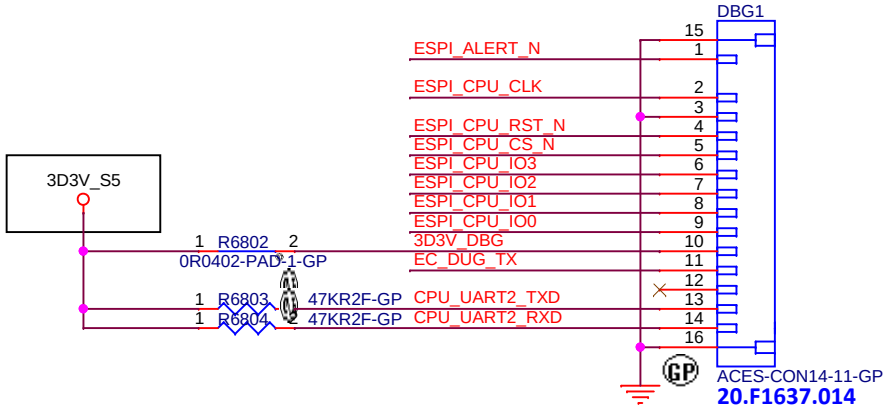


TEST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Sensor (Hall-Sensor)		
Size: A4	Document Number: V550_TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 67 of 106	

18,24 ESPI_CPU_IO0
18,24 ESPI_CPU_IO1
18,24 ESPI_CPU_IO2
18,24 ESPI_CPU_IO3
18,24 ESPI_CPU_CS_N
18,24 ESPI_CPU_CLK
18,24 ESPI_CPU_RST_N
24 ESPI_ALERT_N
24 EC_DUG_TX
20 CPU_UART2_TXD
20 CPU_UART2_RXD
17,24,40,54,57 PM_SLP_S3_N
17,24,40 PM_SLP_S4_N
17,99 SYS_RESET_N

eSPI DEBUG PORT



Why don't have pin12, EC_DUG_RX from EC?
Refer to LC550.

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (eSPI conn)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 68 of 106

TEST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

EAR PHONE

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 69 of 106

TEST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Sensor (G-sensor)

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 70 of 106

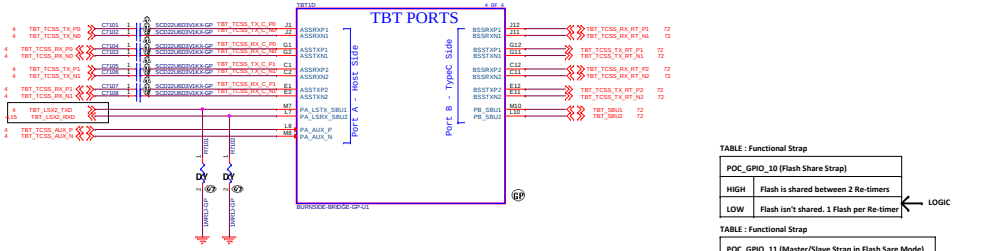


TABLE : Functional Strap

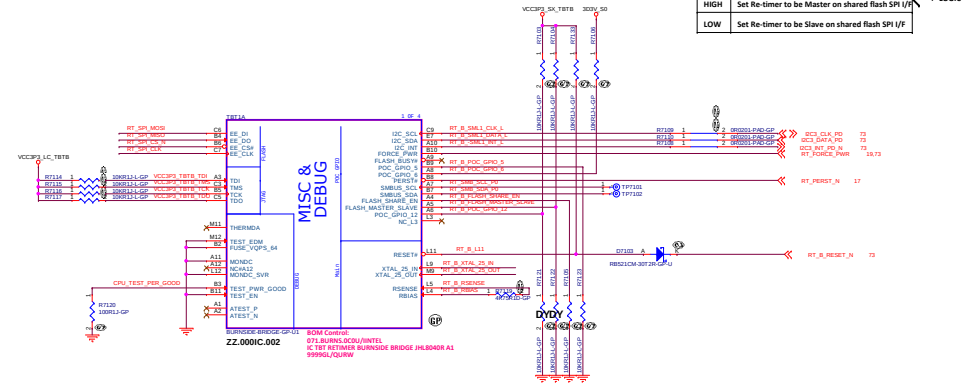
POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

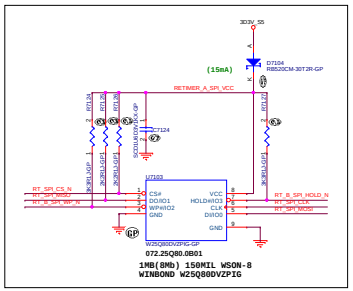
LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

LOGIC





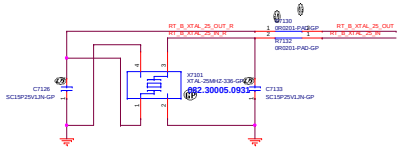
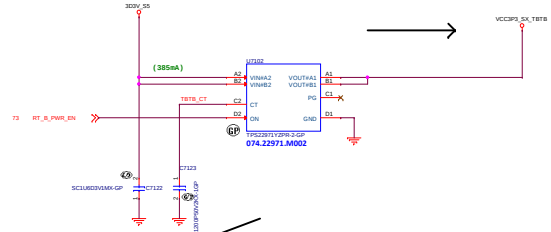
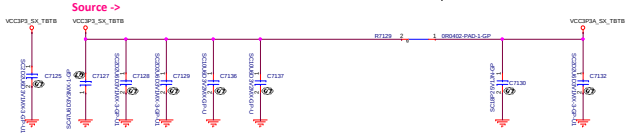
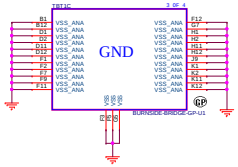


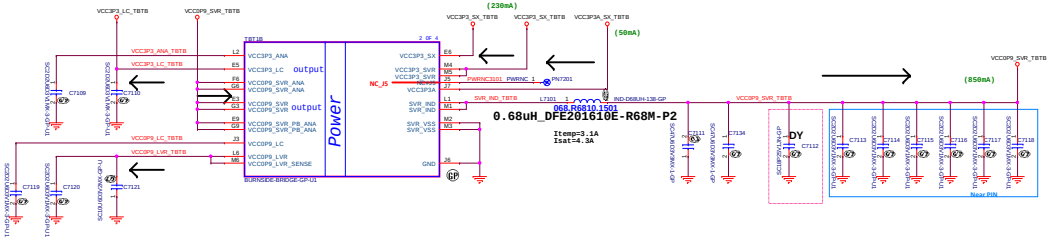
TABLE of X7101 :

Vender	Vender P/N	Wistron P/N
[illegible]	[illegible]	[illegible]
MURATA	XRCGB25M000F2P40R0	082.30005.0911
HOSONIC	E1FB25E000005E	082.30005.0B21









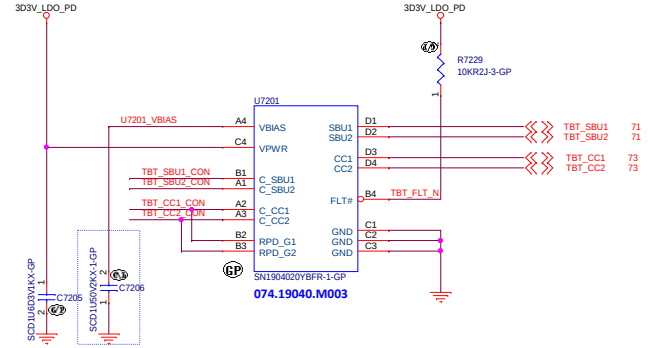
TEST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

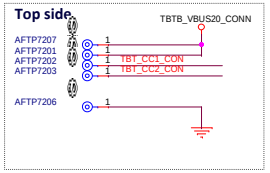
Title: THUNDERBOLT RE TIMER

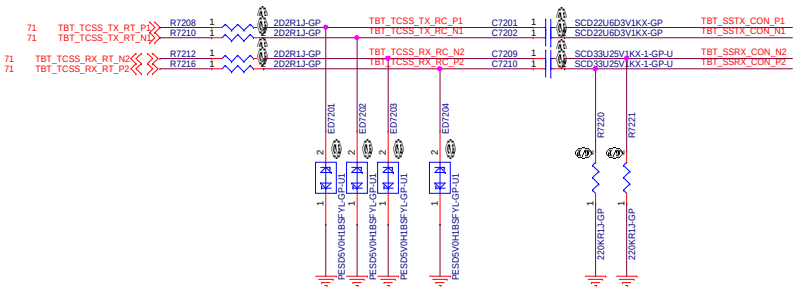
Size	Document Number	Rev
Custom	V550_TGL	-1

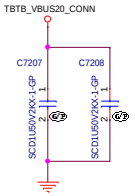
Date: Monday, July 27, 2020 Sheet 71 of 108

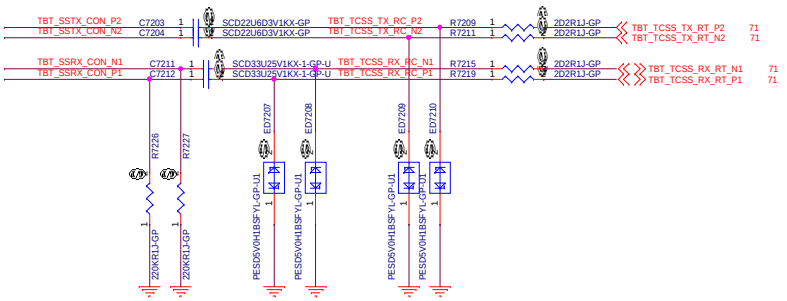


The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.



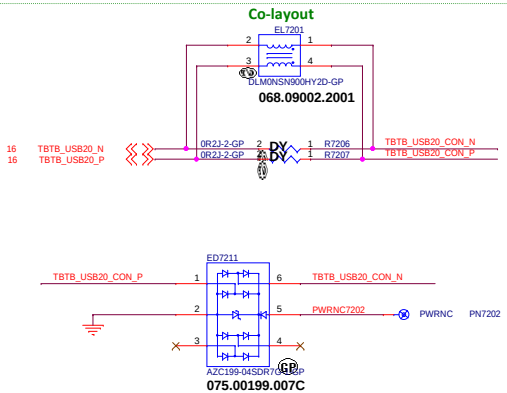






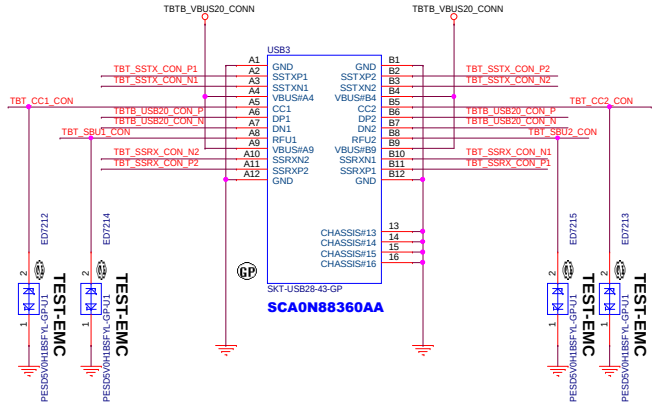
close USB3

Co-layout



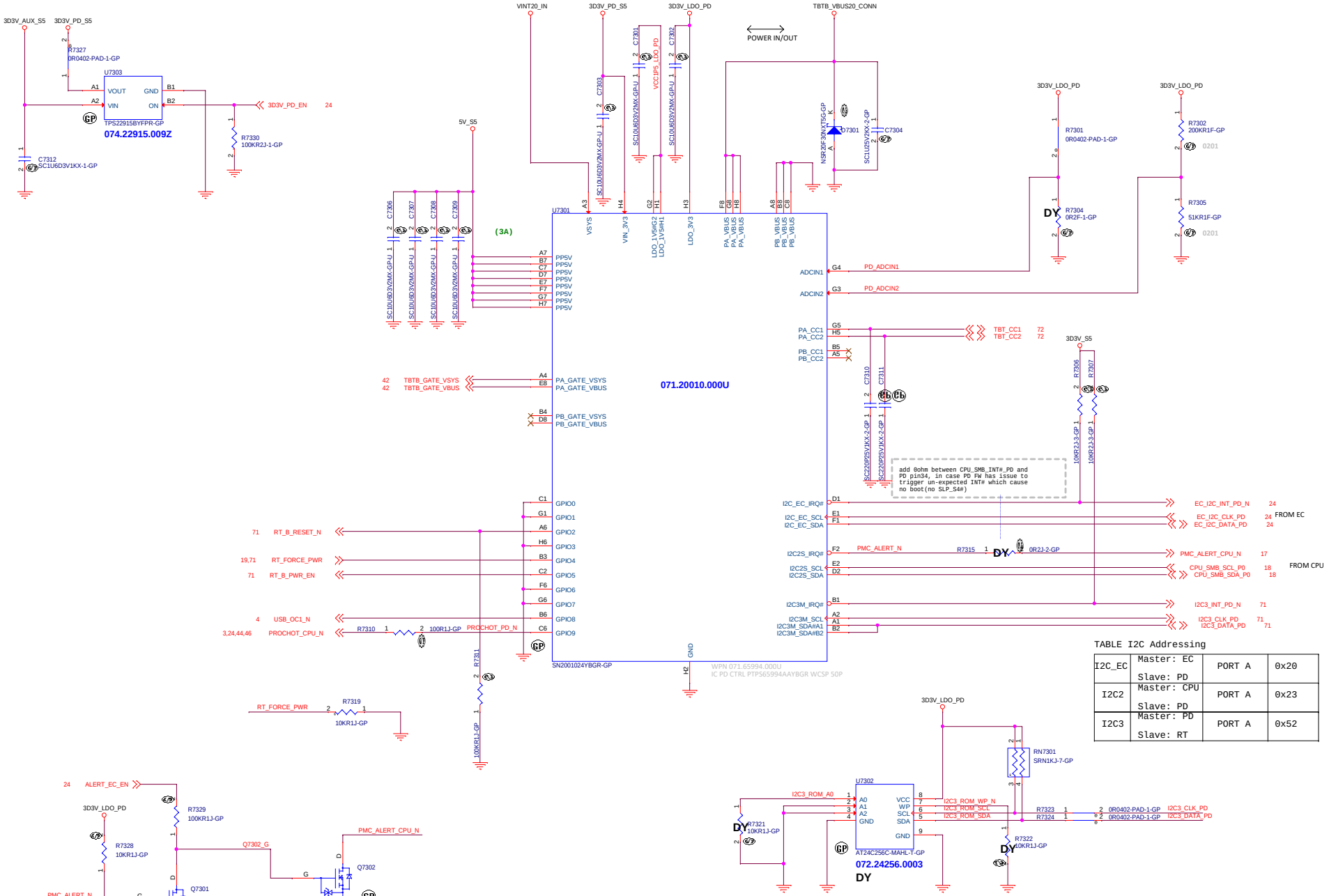
TPC Port2 (TBT/USB3.1/DP/PD)

(65W ADT: 20V, 3.25A)
(95W ADT: 20V, 4.75A)



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: THUNDERBOLT CONNECTOR		
Size: C	Document Number: V550_TGL	Rev: -1
Date: Monday, July 27, 2020	Sheet 72 of 106	


3D3V_AUX_S5
3D3V_PD_S5
R7327
0R0402-PAD-1-GP
U7303
VOUT
VIN
GND
ON
TPS22915BYFPR-GP
074.22915.009Z
C7312
SC1U6D3V1KX-1-GP
3D3V_PD_EN 24
R7330
100KR2J-1-GP
VINT20_IN
3D3V_PD_S5
3D3V_LDO_PD
TBTB_VBUS20_CONN
POWER IN/OUT
C7301
C7302
C7303
VCC1P5_LDO_PD
SC10U6D3V2MX-GP-U
D7301
NSR20F30NXT5G-GP
SC1U25V2KX-2-GP
C7304
5V_S5
(3A)
C7306
C7307
C7308
C7309
U7301
VSYS
VIN_3V3
LDO_1V5IG2
LDO_1V5IM1
LDO_3V3
PA_VBUS
PB_VBUS
PP5V
ADCIN1
ADCIN2
PD_ADCIN1
PD_ADCIN2
R7301
0R0402-PAD-1-GP
R7302
200KR1F-GP
0201
R7304
0R2F-1-GP
DY
R7305
51KR1F-GP
PA_CC1
PA_CC2
PB_CC1
PB_CC2
TBT_CC1
TBT_CC2
C7310
C7311
SC220P25V1KX-2-GP
3D3V_S5
R7306
R7307
10KR2J-3-GP
add 0ohm between CPU_SMB_INT#_PD and PD pin34, in case PD FW has issue to trigger un-expected INT# which cause no boot(no SLP_S4#)
TBTB_GATE_VSYS
TBTB_GATE_VBUS
PA_GATE_VSYS
PA_GATE_VBUS
PB_GATE_VSYS
PB_GATE_VBUS
071.20010.000U
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
RT_B_RESET_N
RT_FORCE_PWR
RT_B_PWR_EN
USB_OC1_N
PROCHOT_CPU_N
R7310
100R1J-GP
PROCHOT_PD_N
R7311
100KR1J-GP
SN2001024YBGR-GP
WPN 071.65994.000U
IC PD CTRL PTPS65994AAYBGR WCSP 50P
I2C_EC_IRQ#
I2C_EC_SCL
I2C_EC_SDA
I2C2S_IRQ#
I2C2S_SCL
I2C2S_SDA
I2C3M_IRQ#
I2C3M_SCL
I2C3M_SDA#A1
I2C3M_SDA#B2
EC_I2C_INT_PD_N
EC_I2C_CLK_PD
EC_I2C_DATA_PD
FROM EC
PMC_ALERT_N
R7315
0R2J-2-GP
PMC_ALERT_CPU_N
CPU_SMB_SCL_P0
CPU_SMB_SDA_P0
FROM CPU
I2C3_INT_PD_N
I2C3_CLK_PD
I2C3_DATA_PD
TABLE I2C Addressing
I2C_EC | Master: EC Slave: PD | PORT A | 0x20
I2C2 | Master: CPU Slave: PD | PORT A | 0x23
I2C3 | Master: PD Slave: RT | PORT A | 0x52
RT_FORCE_PWR
R7319
10KR1J-GP
ALERT_EC_EN
R7329
100KR1J-GP
R7328
10KR1J-GP
Q7301
LSK3511G1ET2L-1-GP
084.03541.M001
Q7302_G
Q7302
PMC_ALERT_CPU_N
084.03541.M001
RN7301
SRN1KJ-7-GP
U7302
I2C3_ROM_A0
I2C3_ROM_WP_N
I2C3_ROM_SCL
I2C3_ROM_SDA
R7321
10KR1J-GP
R7322
10KR1J-GP
R7323
R7324
0R0402-PAD-1-GP
AT24C256C-MAHL-T-GP
072.24256.0003
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title TYPEC PD SN1905004
Size C
Document Number V550_TGL
Rev -1
Date: Monday, July 27, 2020
Sheet 73 of 106

TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TBT Re-Timer-2)

Size	Document Number	Rev
Custom	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 74 of 109

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***THUNDERBOLT CONNECTOR C***

Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 75 of 106

NTD ORS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (PEG 1/5)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (DIGITAL 2/5)

Size	Document Number	Rev
A	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 77 of 106

NTD ORS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM 3/5)

Size	Document Number	Rev
A	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 78 of 106

NTD ORS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (GPIO 4/5)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (PWR/GND 5/5)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM1,2 1/4)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM3,4 2/4)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

GPU (RSVD) (VRAM5,6 3/4)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM7,8 4/4)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VGA_CORE)

Size	Document Number	Rev
A	V550_TGL	-1

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NTD ORS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (Sequence)

Size	Document Number	Rev
A	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 86 of 106

NTD ORS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (Sequence)

Size	Document Number	Rev
A	V550_TGL	-1

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TEST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

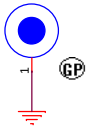
Title

UNUSED PARTS (FIP)

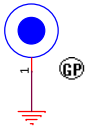
Size	Document Number	Rev
A4	V550_TGL	-1

Date: Monday, July 27, 2020 Sheet 88 of 106

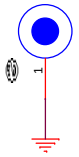
H2
HOLE296R158-GP
ZZ.PAD01.V71



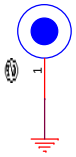
H5
HOLE296R158-GP
ZZ.PAD01.V71



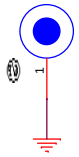
HS1
STF237R113H62-4-GP
34.4SE26.001



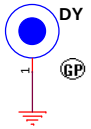
HS2
STF237R113H62-4-GP
34.4SE26.001



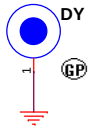
HS3
STF237R113H62-4-GP
34.4SE26.001



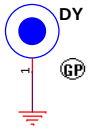
HOLE1
HOLET297X262B420X288R138-S
HOLET297X262B420X288R138-S



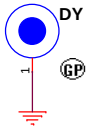
HOLE3
HOLET325X276B691X394R119-S
HOLET325X276B691X394R119-S



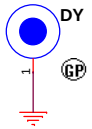
HOLE4
HOLET348X276B499X526R119-2P-S
HOLET348X276B499X526R119-2P-S



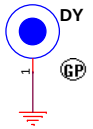
HOLE5
HOLE473X355R158-S
HOLE473X355R158-S



HOLE6
HOLE473X355R158-S1
HOLE473X355R158-S1



HOLE7
HOLE355X296R158-S
HOLE355X296R158-S



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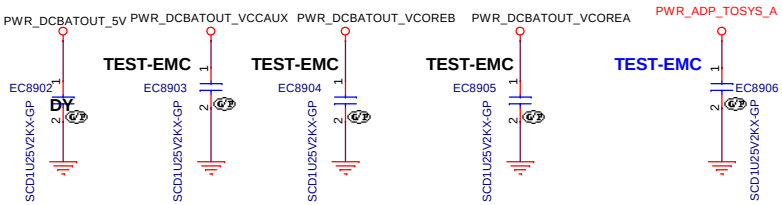

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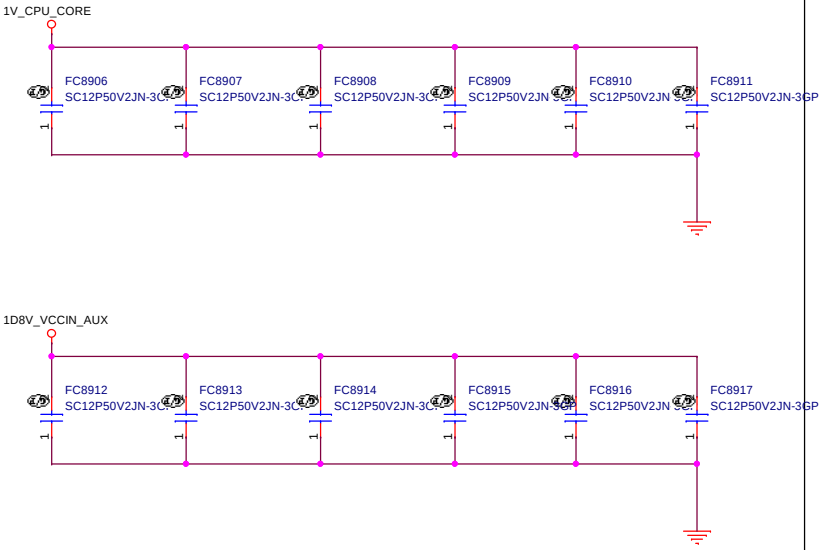

TEST

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Title: **UNUSED PARTS (RF/EMI Capacitors)**

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
INT IO (M.2 Myraid X VPU/ 2nd SSD)

Size	Document Number	Rev
A4	V550_TGL	-1
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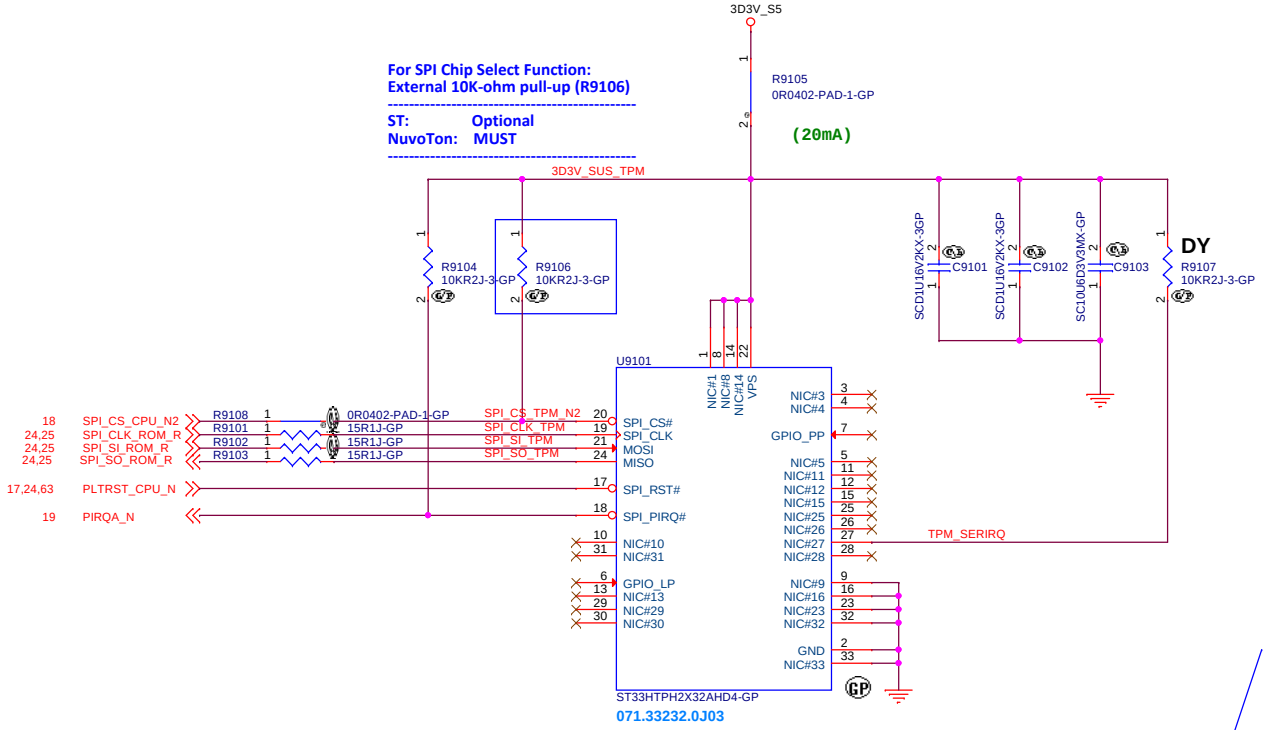

For SPI Chip Select Function:
External 10K-ohm pull-up (R9106)

ST: **Optional**
NuvoTon: **MUST**

SPI Chip Select Pin:
ST **(SPI_CS#)** **Internal pull-up**
NuvoTon **(SCS#)** **Internal pull-up is disabled if the pin is part of the recognized host interface**

TPM TABLE

1st	ST33HTPH2X32AHD4	071.33232.0J03
2nd	NPCT750LADYX	071.00750.0H03

China TCM TABLE

1st	Z32H330TC-SQN-751	071.32330.0B03

TABLE 071.33232.0H03 071.00750.0D03 ~~071.09670.0I03~~

Pin No	TCG PTP Spec(V38)	ST Micro ST33HTPH2E32AHC0	NuvoTon NPCT750LABYX	Infineon SLB9670VQ2.0 FW7.63
1	VDD	NC	VSB	VDD
2	GND	GND	NC	GND
3	NC	NC	NC	NC
4	GPIO	PP	GPIO/PP	NC
5	NC	NC	NC	NC
6	GPIO	NC	GPIO3	GPIO
7	GPIO	GPIO	NC	PP
8	VDD	NC	VHIO	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	NC	GPIO4	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	NC
17	SPI_RST#	SPI_RST#	RST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	NC	SDA/GPIO0	NC
30	SDA/GPIO0	NC	SCL/GPIO1	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND

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Title: **INT IO (TPM)**

Size: A3 | Document Number: **V550_TGL** | Rev: **-1**

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Title

INT IO (RSVD) (Finger Printer)

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Title: EXT IO (Function Key)

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Title
EXT IO (RSVD) (Smart Card/COM/PS2)

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Title

EXT IO (RSVD) (Docking/LPT)

Size	Document Number	Rev
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Title: **Commercial (RSVD) (SW GFX eDP)**

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Title: **Consumer (RSVD) (LAN)**

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Title

Consumer (RSVD) (LAN Switch)

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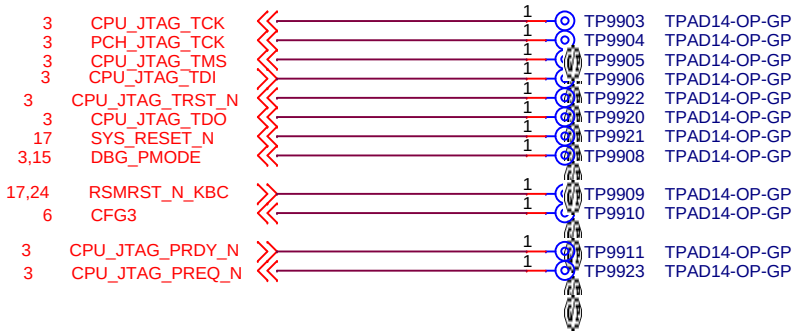

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Title: **Debug (XDP/HDT conn)**

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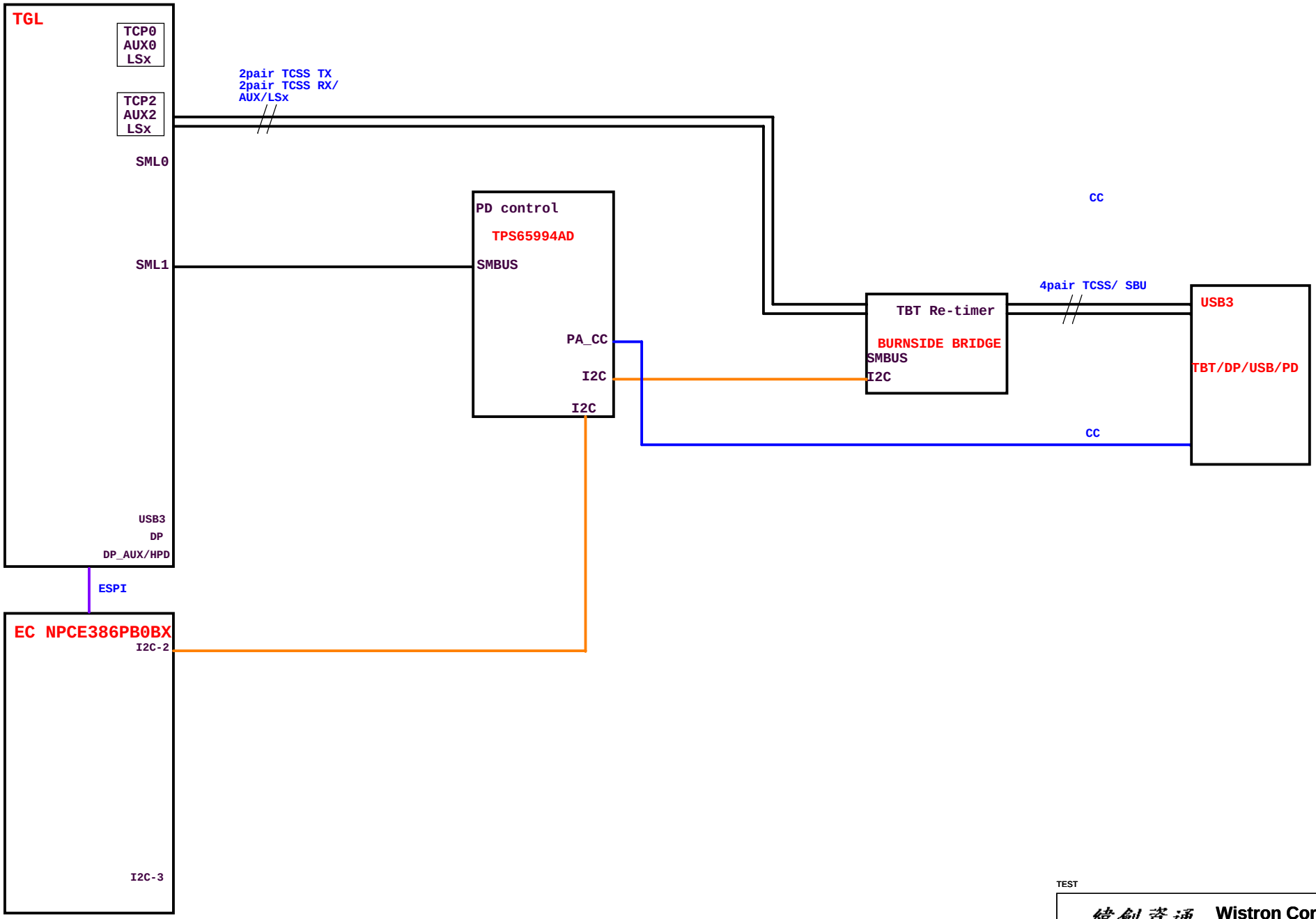
LV550 TYPE-C Block Diagram



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Title: Table of Content		
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Not Stuffed-AMP :ZZ,DY,DY-EMC,DY_RF,NON-AMP,DEBUG

Not Stuffed-NON AMP :ZZ,DY,DY-EMC,DY_RF,AMP,DEBUG

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Title: **SMT memo**

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A4	V550_TGL	-1

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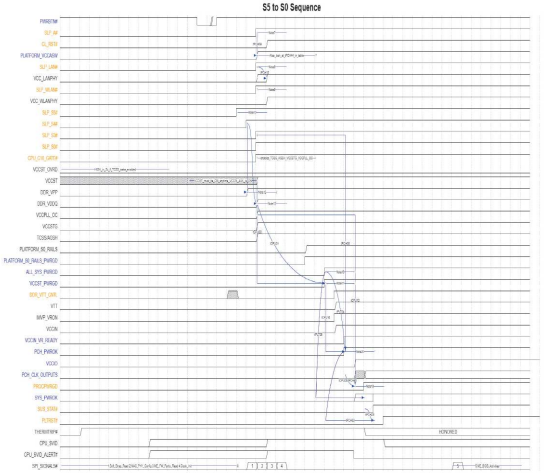
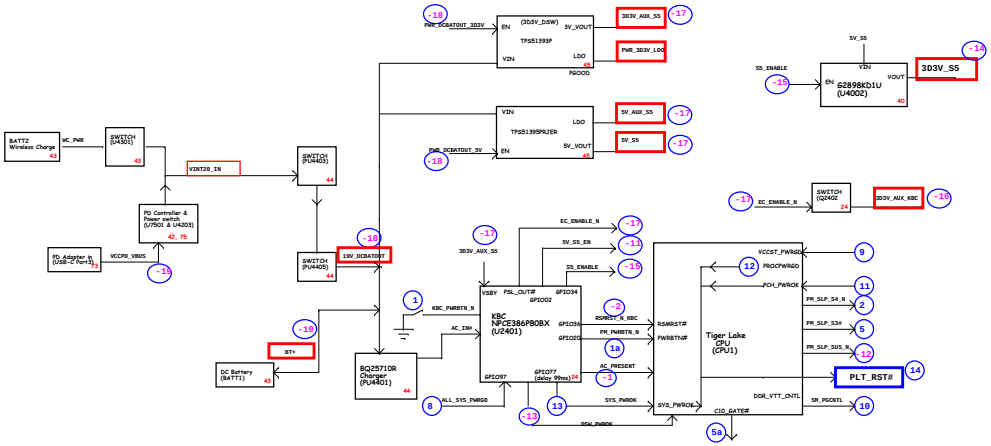
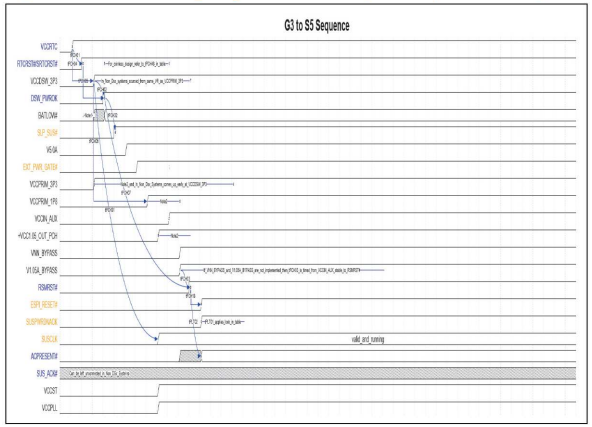
Intel-Power Up Sequence



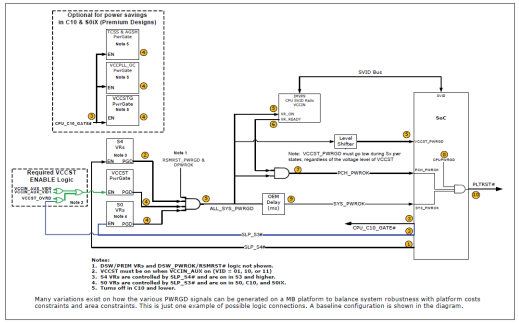
Tiger Lake U POWER UP SEQUENCE DIAGRAM



Tiger Lake-Y and U Timing Diagram for G3 to S0[Non-Deep Sx Platform]



ure 267. Tiger Lake Y and U (Premium) PWROK Generation Flow Diagram



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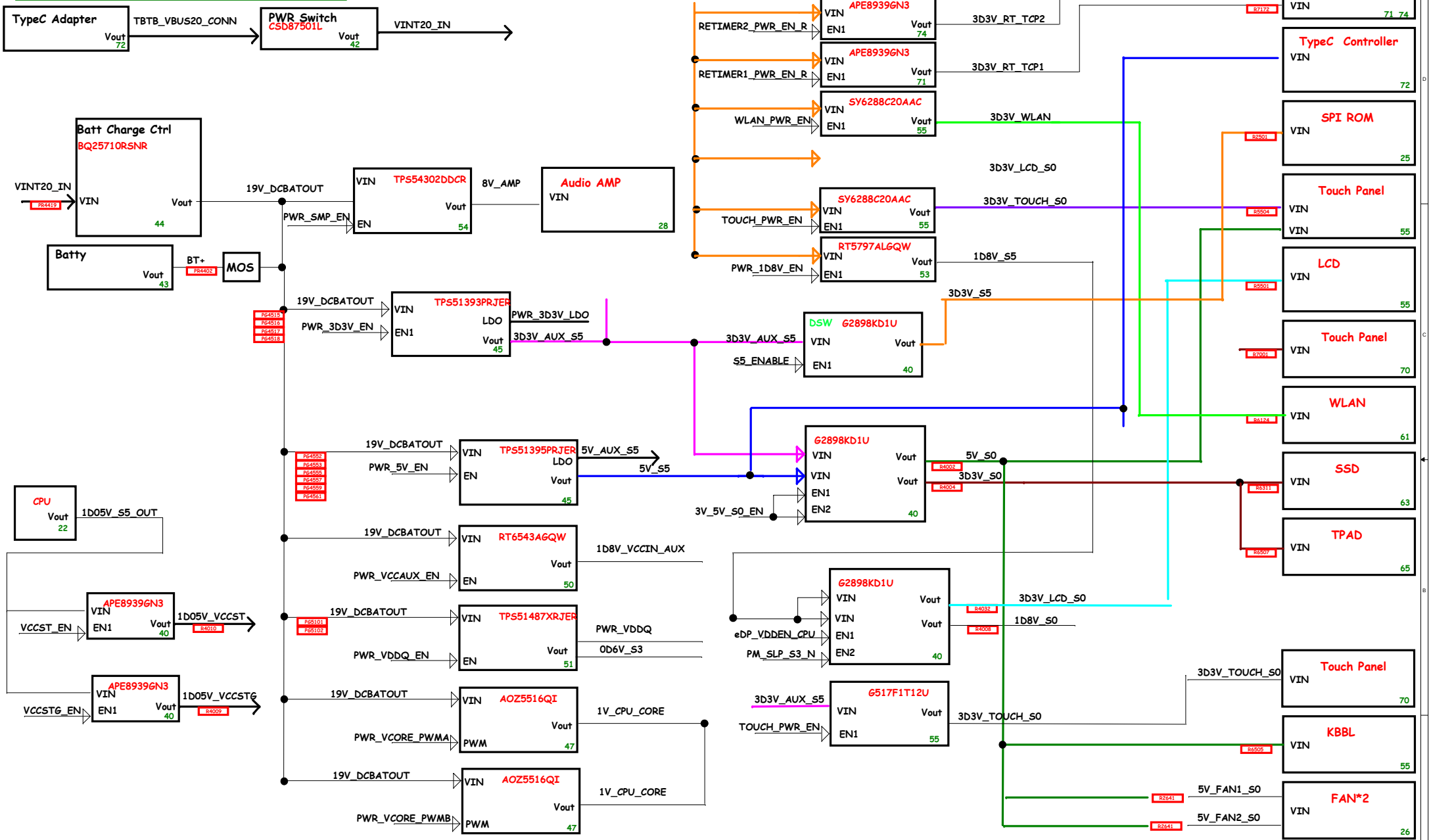
Power Sequence

V550_TGL

POWER BLOCK DIAGRAM



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Title: Power Block Diagram

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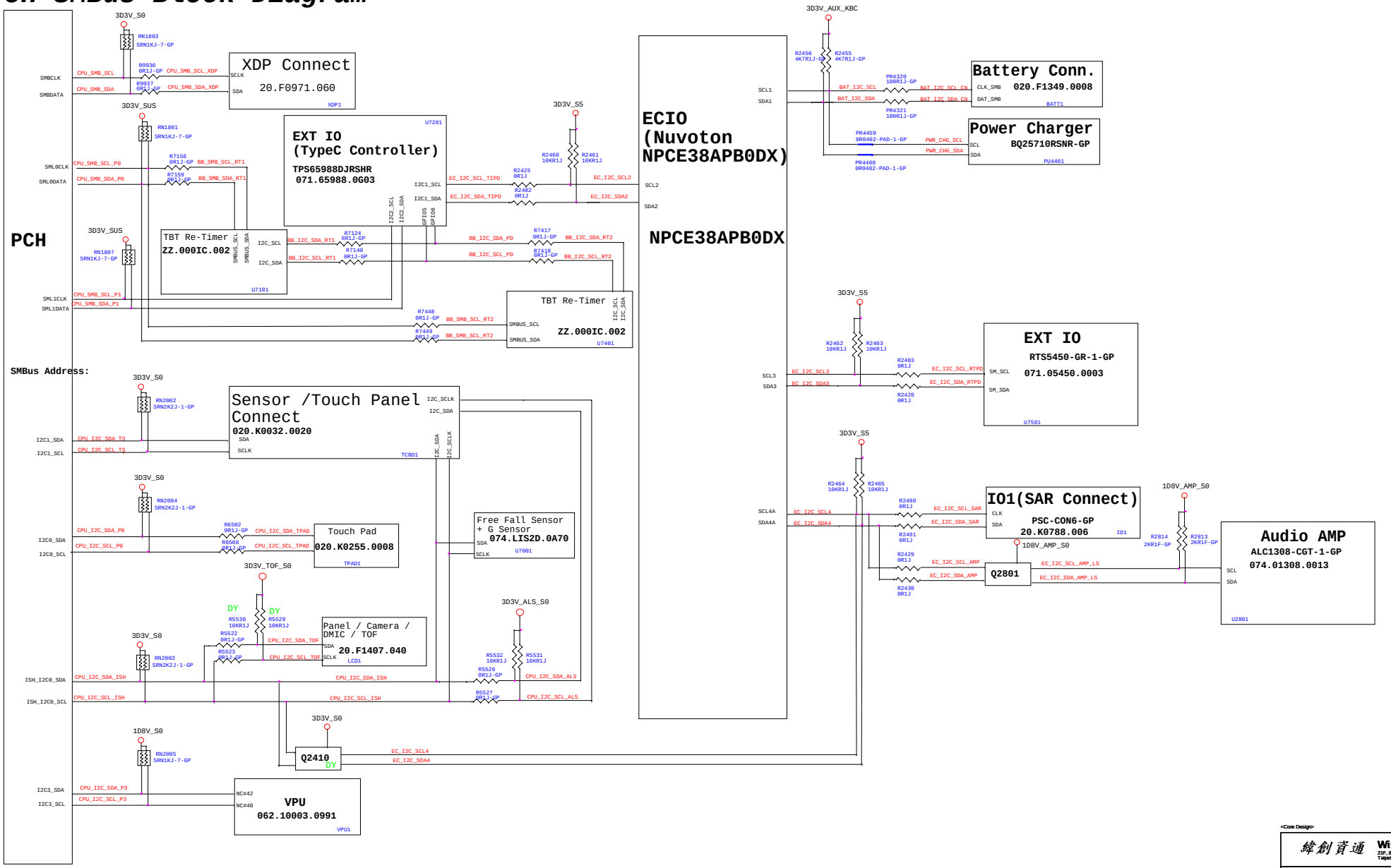
PCH SMBus Block Diagram



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File: SMBUS/I2C BLOCK DIAGRAM

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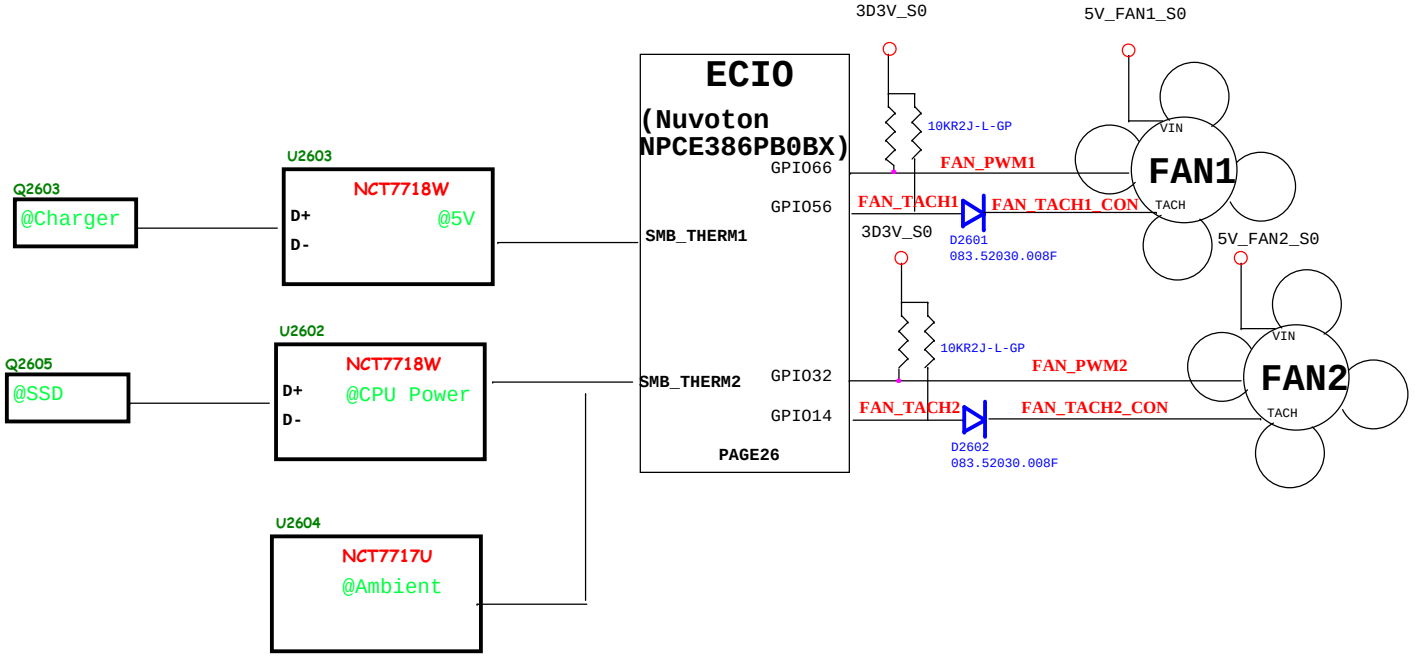
Thermal Block Diagram



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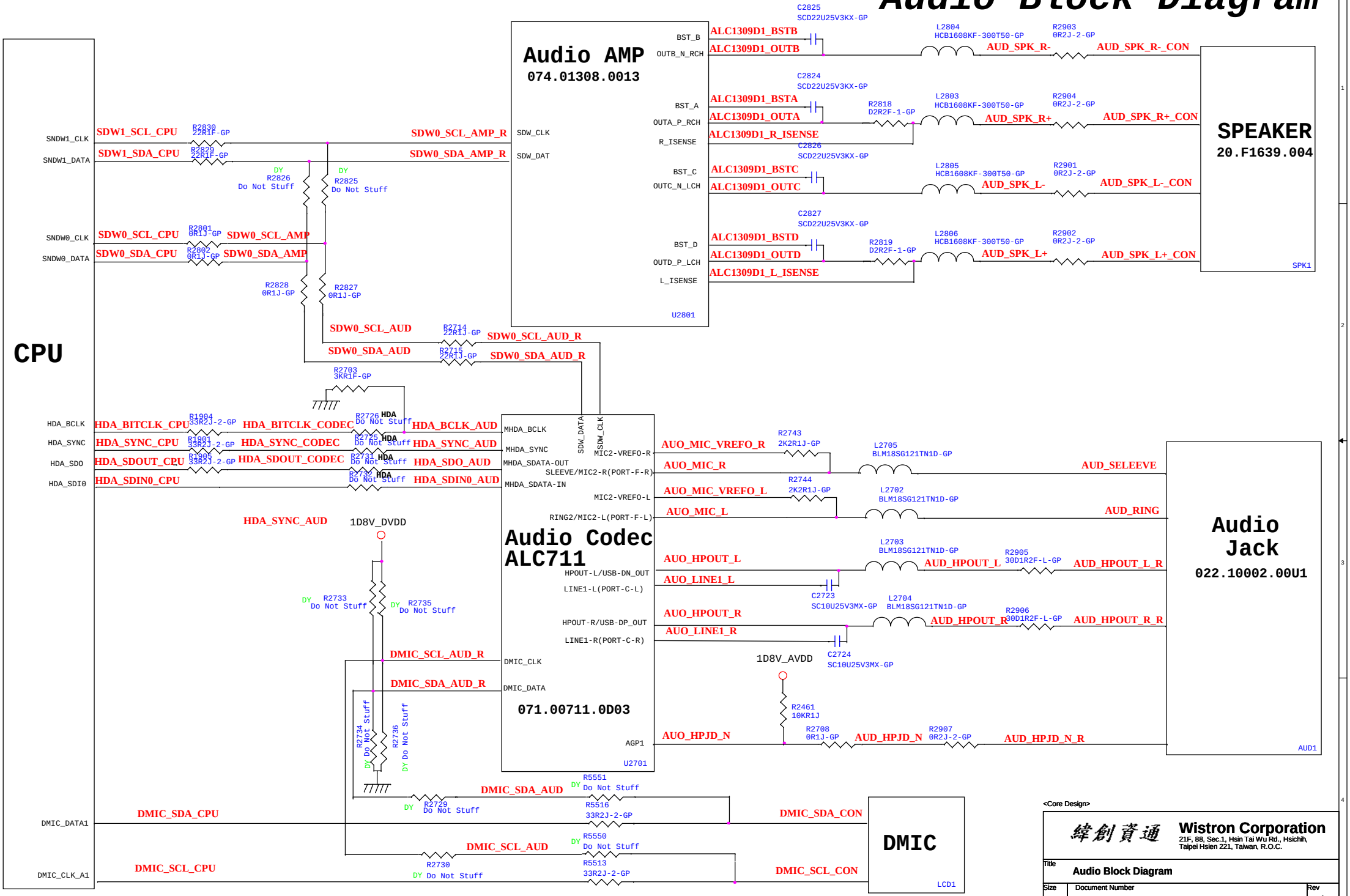
Audio Block Diagram



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Title	Audio Block Diagram	
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