Compal Confidential

Model Name : A4DBH
File Name : LA-B731P
BOM P/N:43

ZZZ1
LA-B731P
DAA0008X000
DA2@

ZZZ2
LS-A131P
DA4001PG010
DA2@

ZZZ3
LS-B733P
DA60018L000
DA2@

ZZZ4
LS-A133P
DA600101010
DA2@

ZZZ5
LS-A134P
DA4001PH010
DA2@

ZZZ6
LS-B734P
DA6001B8000
DA2@

ZZZ7
HDMI LOGO
RO0000003HM
HDMI@

ZZZ8
LS-B732P
DA4001YF00S
DA2@

ZZZZ1
PCB
DAZ18000300
DAZ@

Compal Confidential

A4DBH M/B Schematics Document

Broadwell ULT Processor + LP PCH+Nvidia N15S-GT

2014-09-25

Rev:0.4

Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

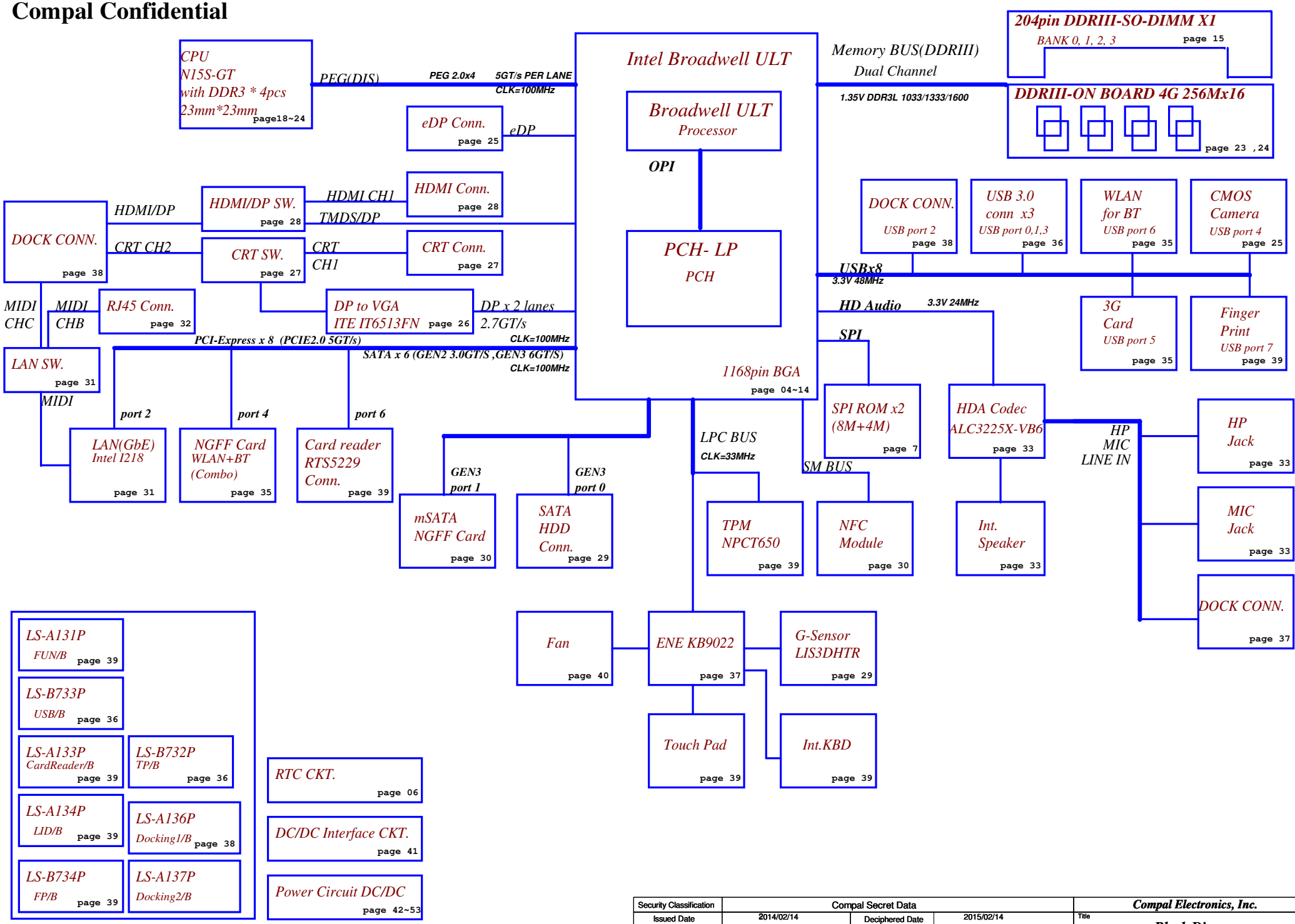
Compal Electronics, Inc.

Title: Cover Page

Size: Custom | Document Number: LA-B731P | Rev: 0.1

Date: Thursday, September 25, 2014 | Sheet 1 of 56

Compal Confidential



Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.

Title: **Block Diagrams**

Size	Document Number	Rev
Custom	LA-B731P	0.1

Date: Wednesday, September 17, 2014 | Sheet 2 of 56

Voltage Rails

Power Plane	Description	AC S0	AC S3	AC S4	AC S5	DC S3	DC S4	DC S5
+RTCVCC	RTC power	ON	ON	ON	ON	ON	ON	ON
VIN	Adapter power supply (19V)	N/A	ON	ON	ON	OFF	OFF	OFF
BATT+	Battery power supply (9V or 19V)	N/A	N/A	N/A	N/A	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW	+3VALW always on power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH	ON	ON	ON	ON	ON	ON	ON
+3VM	+3VALW to +3VM power rail for PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VM	+1.05VS_VTT to +1.05VM switched power rail for CPU & PCH	ON	ON*	ON*	ON*	ON*	ON*	ON*
+1.05VS_VTT	+1.05VSP to +1.05VS_VTT switched power rail for CPU & PCH	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.35V	+1.35VP to +1.35V switched power rail for DDR terminator	ON	ON	OFF	OFF	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VS_VGA_AON	+3VS to +3VS_VGA_AON power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+3VS_VGA_MAIN	+3VS to +3VS_VGA_MAIN power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VSDGPU	B+ to +1.5VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.05V_VGA	+1.05VS_VTT to +1.5VS_VGA switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+3V_LAN	LAN CHIP POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+3VS_WLAN	WLAN MODULE POWER RAIL	ON*	ON*	ON*	OFF	OFF	OFF	OFF
+USB3_VCCA	USB Charger PORT0 & PORT9 POWER POWER RAIL	ON	ON	ON	ON	ON*	ON*	ON*

Note : ON* WILL DEPEND ON SLP_A# TO TURN ON OR OFF(ME FIRMWARE CONTROL)

Note : ON* WILL DEPEND ON BATTERY CAPACITY TO TURN ON OR OFF

Note : ON** Depend on Optimus ON/OFF.

Note : ON* Depend on LAN wake SPEC

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
charger IC	0001 001X b
GPU	1001 111X b

EC SM Bus2 address

Device	Address
On Board Thermal Senser(CPU)	1001_101xb
PCH	1001_011xb

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000Xb	On Board RAM(SPD)
ChannelB	DIMM0	A4	1010 010Xb	JDIMM1(SPD)
G-sensor			0011 000xb	

PCH SM Bus0 address

Device	Address
LAN	1100_100xb
NFC	0010_100xb

CPU BOM Config

RAM BOM Config

HYNIX	256*16	SA00005AV50(H5TC4G63AFR-PBA)	X76SHYNIX0@
ELPDA	256*16	SA00005HT80(EDJ4216EFBG-GNL-F FBGA)	X76SELP0@

GPU BOM Config

N15S-GT	SA00007GJ00 (S IC N15S-GT-S-A2 BGA 595P GPU)

VRAM BOM Config

HYNIX	256*16	SA00006E800(H5TC4G63AFR-11C FBGA 96P)	X76VHYNIX0@
SAMSUNG	256*16	SA000076P00(K4W4G1646D-BC1A FBGA 96P)	X76VSAM0@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

+3VALW_EC	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

USB Port Table

USB 2.0	Port	USB Port
EHCI	0	USB Port 3.0 (I/O board)
	1	USB port 3.0 (Left side)
	2	DOCK USB3.0
	3	USB Port 3.0 (I/O board)
	4	Camera
	5	Mini Card(3G)
	6	Mini Card(WLAN+BT)
	7	Finger Print

USB 3.0	Port	
XHCI	1	USB Port 3.0 (I/O board)
	2	USB3 (Left side)

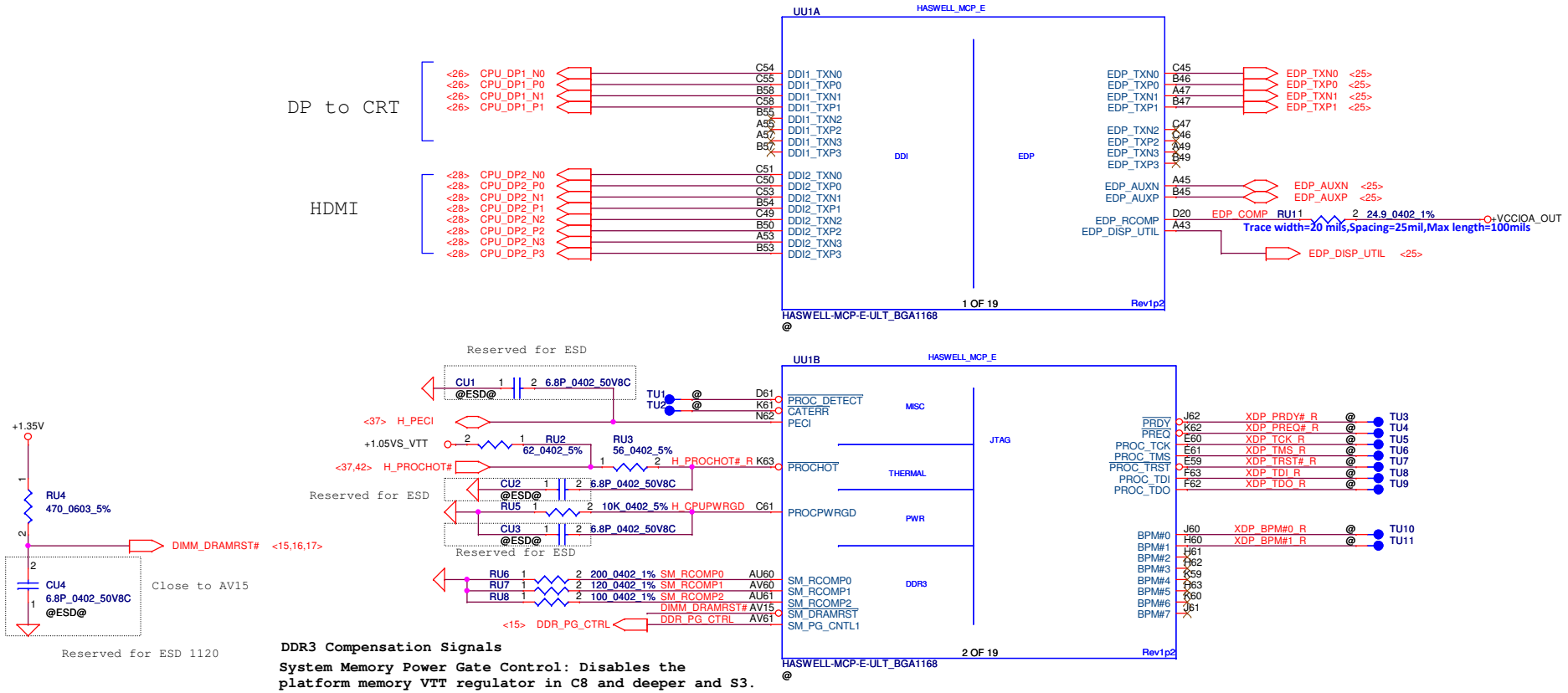
PCIE Table

Port	PCI Express Port
1	USB 3.0 DOCK
2	USB 3.0 (I/O board)
3	LAN
4	WLAN
5-L0	VGA
5-L1	
5-L2	
5-L3	
6-L0	CardReader

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA Only	UMA@
DISCRETE	VGA@
DRAM ELPIDA	X76SELP0@
DRAM HYNIX	X76SHYNIX0@
NFC Function	NFC@
3G Function	3G@
VPRO Function	VPRO@
NO VPRO Function	NOVPRO@
EMI SOLUTION	EMI@
UMA Part Count	PC@
SATA RE-DRIVER	SD@
ESD SOLUTION	ESD@
VRAM HYNIX	X76VHYNIX0@
VRAM SAMSUNG	X76VSAM0@
EC 9012	9012@
EC 9022	9022@
GC6 Function	GC6@
No GC6 Function	NOGC6@
TI re-driver	X76TI@
Parade re-driver	X76PAR@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/14	Deciphered Date 2015/02/14	Title: Notes List
			Size: Custom; Document Number: LA-B731P; Rev: 1A
			Date: Friday, September 19, 2014; Sheet 3 of 56



UU1 NON-VPRO CPU_QG21 QG21@ SA00007OS10

UU1 NON-VPRO CPU_QFSY QFSY@ SA00007AM00

UU1 NON-VPRO CPU_QG22 QG22@ SA00007OT10

UU1 VPRO CPU_QGHA QGHA@ SA00007UG20

UU1 VPRO CPU_QGH9 QGH9@ SA00007U920

UU1 VPRO CPU_QGHB QGHB@ SA00007UH20

DVT CPU BOM OPTION

UU1 NON-VPRO CPU_QH15 QH15@ SA000083A10

UU1 NON-VPRO CPU_QH17 QH17@ SA000083C10

UU1 VPRO CPU_QEK1 QEK1@ SA00006SS30

UU1 VPRO CPU_QH14 QH14@ SA000083930

UU1 VPRO CPU_QH16 QH16@ SA000083B30

PVT CPU BOM OPTION

UU1 VPRO CPU_QH3D QH3D@ SA00008AC20

UU1 Ci75500U non-VPRO CPU_QH3E QH3E@ SA000089A50

UU1 VPRO CPU_QH3F QH3F@ SA00008AA20

UU1 Ci55200U non-VPRO CPU_QH3G QH3G@ SA000089950

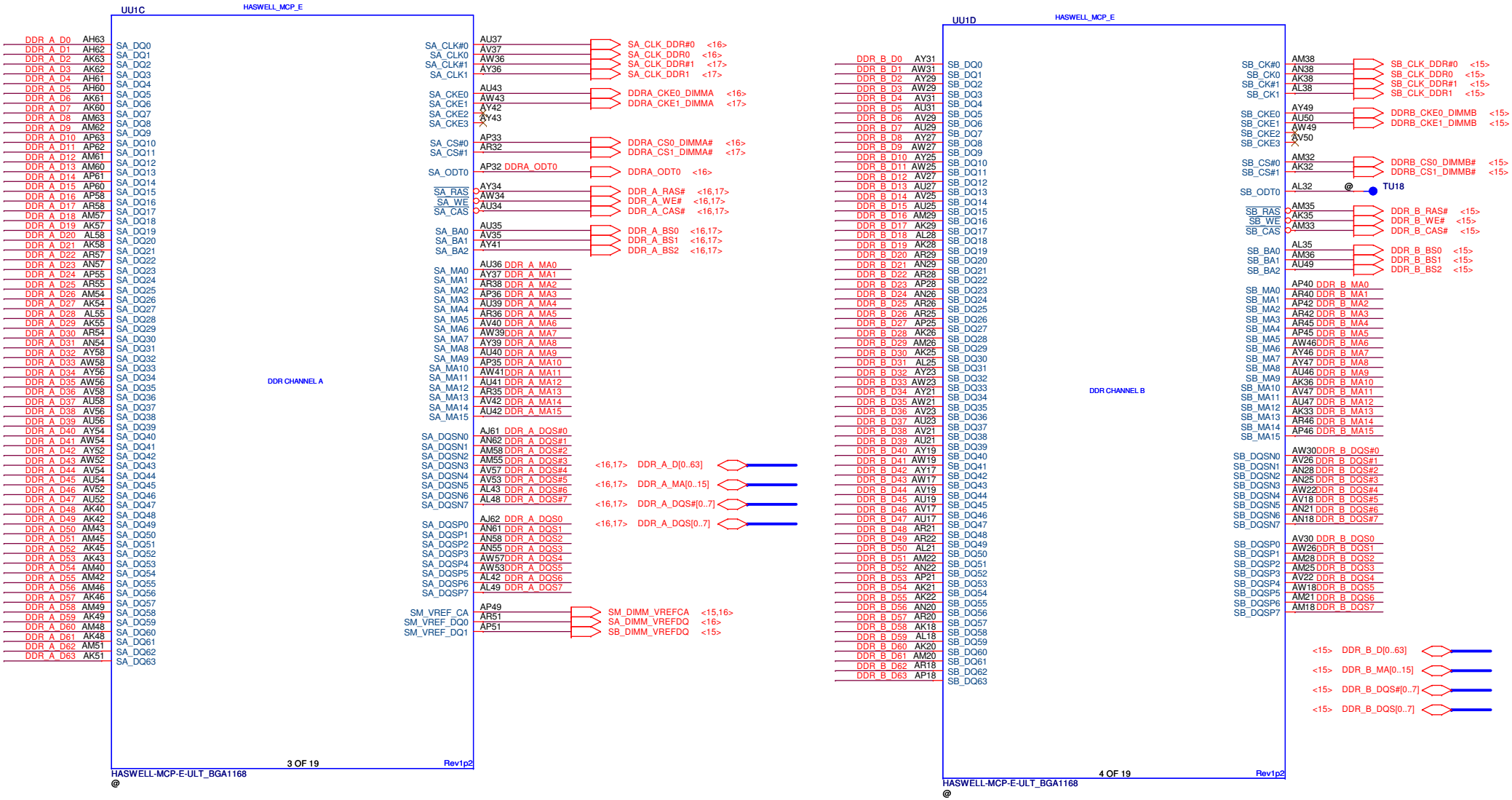
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.

Title: HSW MCP(1/11) DDI,MSIC,XDP

Size	Document Number	Rev
Custom	LA-B731P	1.0

Date: Thursday, September 25, 2014 Sheet 4 of 56



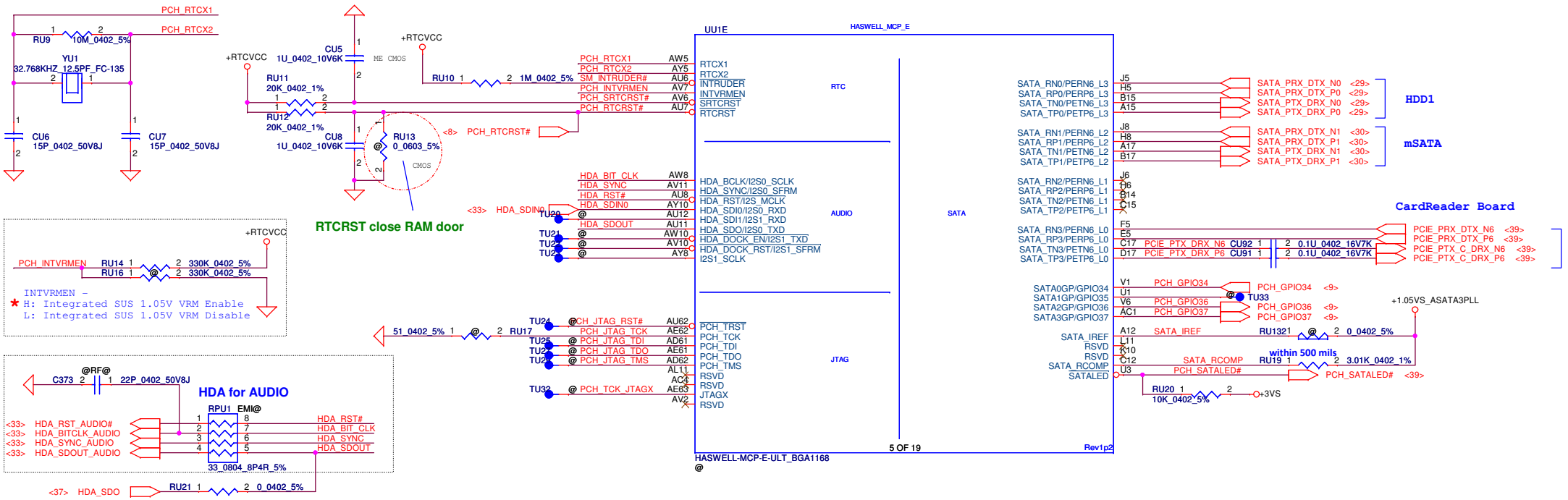
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.

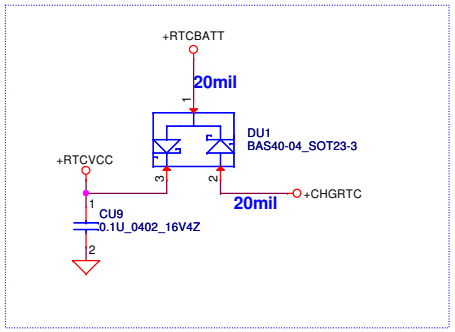
Title: **HSW MCP(2/11) DDRIII**

Size	Document Number	Rev
Custom	LA-B731P	1A

Date: Wednesday, September 17, 2014 | Sheet 5 of 56



ME Debug (internal pull-down)
1: Disable Flash Descriptor Security (override)



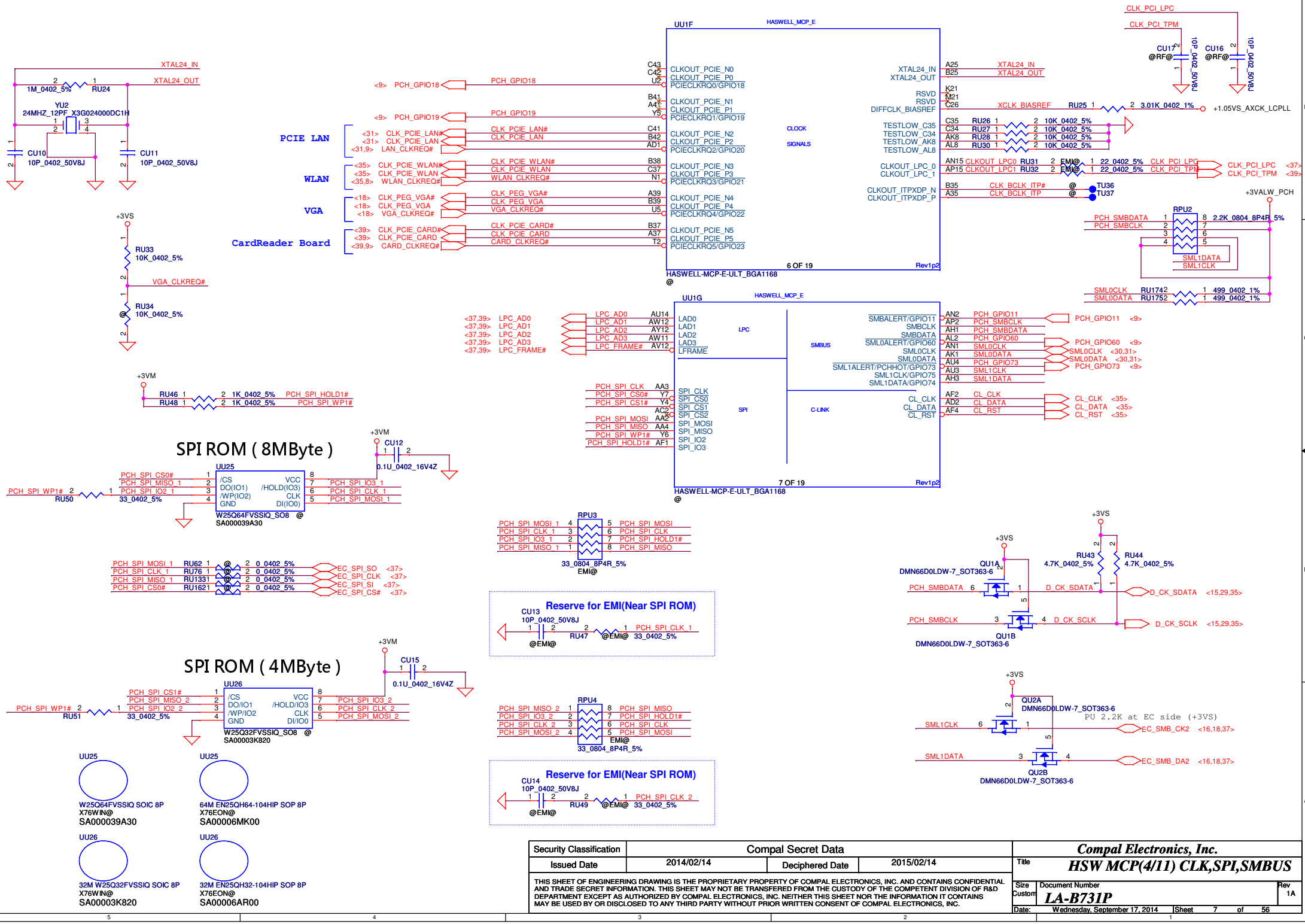
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.

Title: HSW MCP(3/11) RTC,SATA,XDP

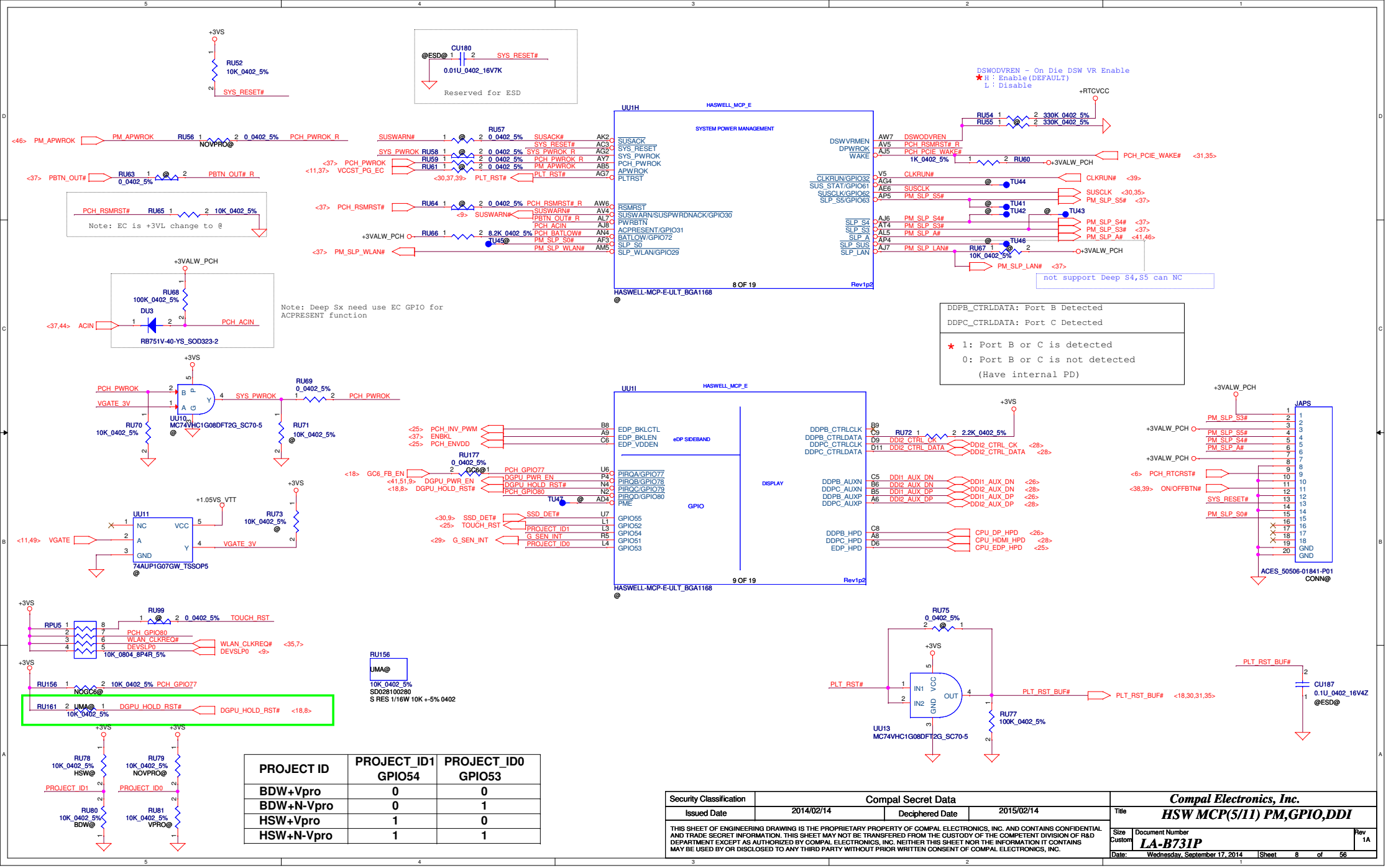
Size	Document Number	Rev
Custom	LA-B731P	1A

Date: Wednesday, September 17, 2014 Sheet 6 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.			
Title	HSW MCP(4/11) CLK,SPI,SMBUS		
Size: Custom	Document Number: LA-B731P		Rev: 1A
Date: Wednesday, September 17, 2014	Sheet 7 of 56		



PROJECT ID	PROJECT_ID1 GPIO54	PROJECT_ID0 GPIO53
BDW+Vpro	0	0
BDW+N-Vpro	0	1
HSW+Vpro	1	0
HSW+N-Vpro	1	1

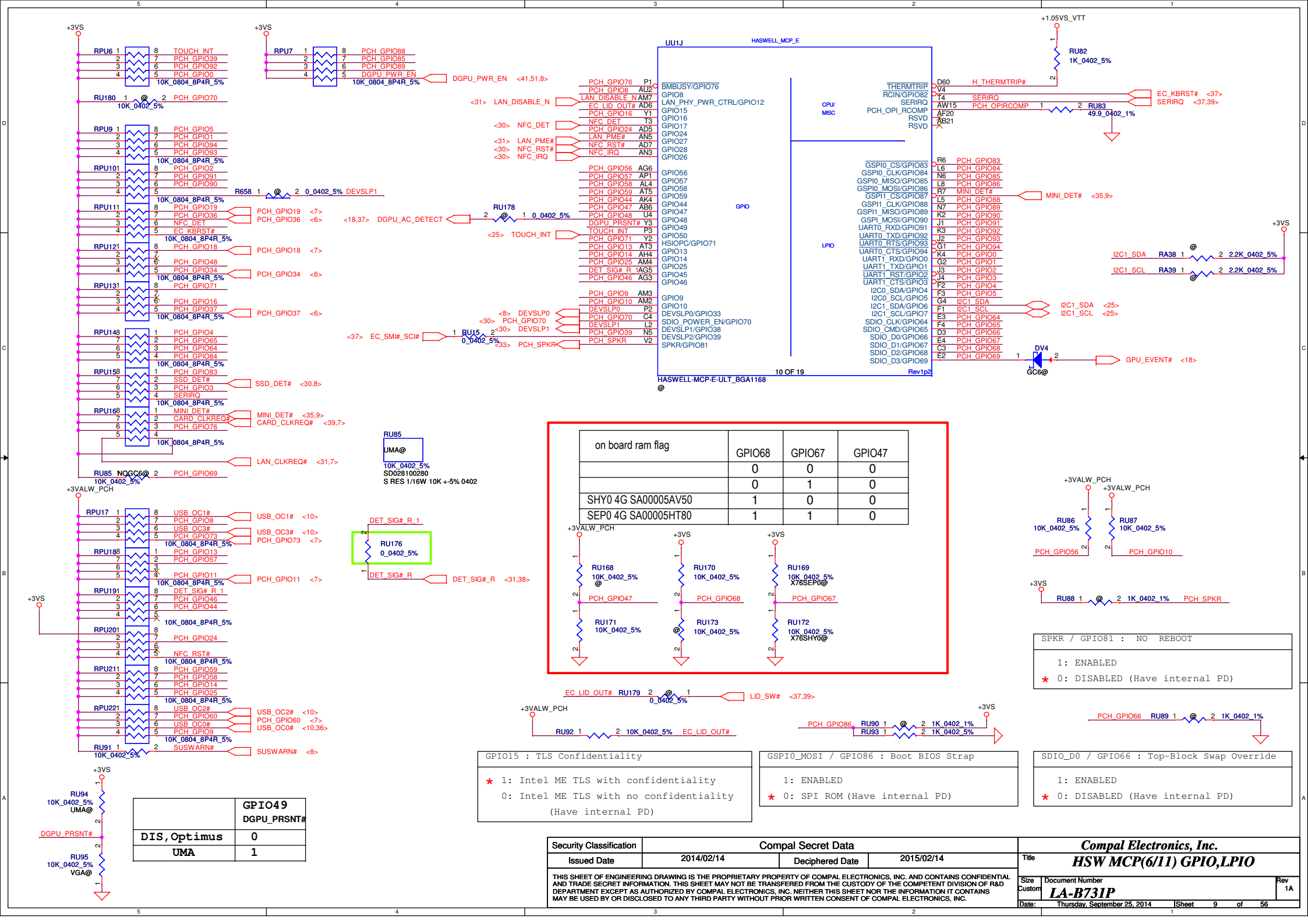
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.

Title: HSW MCP(5/11) PM,GPIO,DDI

Size	Document Number	Rev
Custom	LA-B731P	1A

Date: Wednesday, September 17, 2014 Sheet 8 of 56



on board ram flag	GPIO68	GPIO67	GPIO47
	0	0	0
	0	1	0
SHY0 4G SA00005AV50	1	0	0
SEP0 4G SA00005HT80	1	1	0

	GPIO49 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

SPKR / GPIO81 : NO REBOOT

1: ENABLED

* 0: DISABLED (Have internal PD)

GPIO15 : TLS Confidentiality

* 1: Intel ME TLS with confidentiality

0: Intel ME TLS with no confidentiality (Have internal PD)

GSPI0_MOSI / GPIO86 : Boot BIOS Strap

1: ENABLED

* 0: SPI ROM (Have internal PD)

SDIO_D0 / GPIO66 : Top-Block Swap Override

1: ENABLED

* 0: DISABLED (Have internal PD)

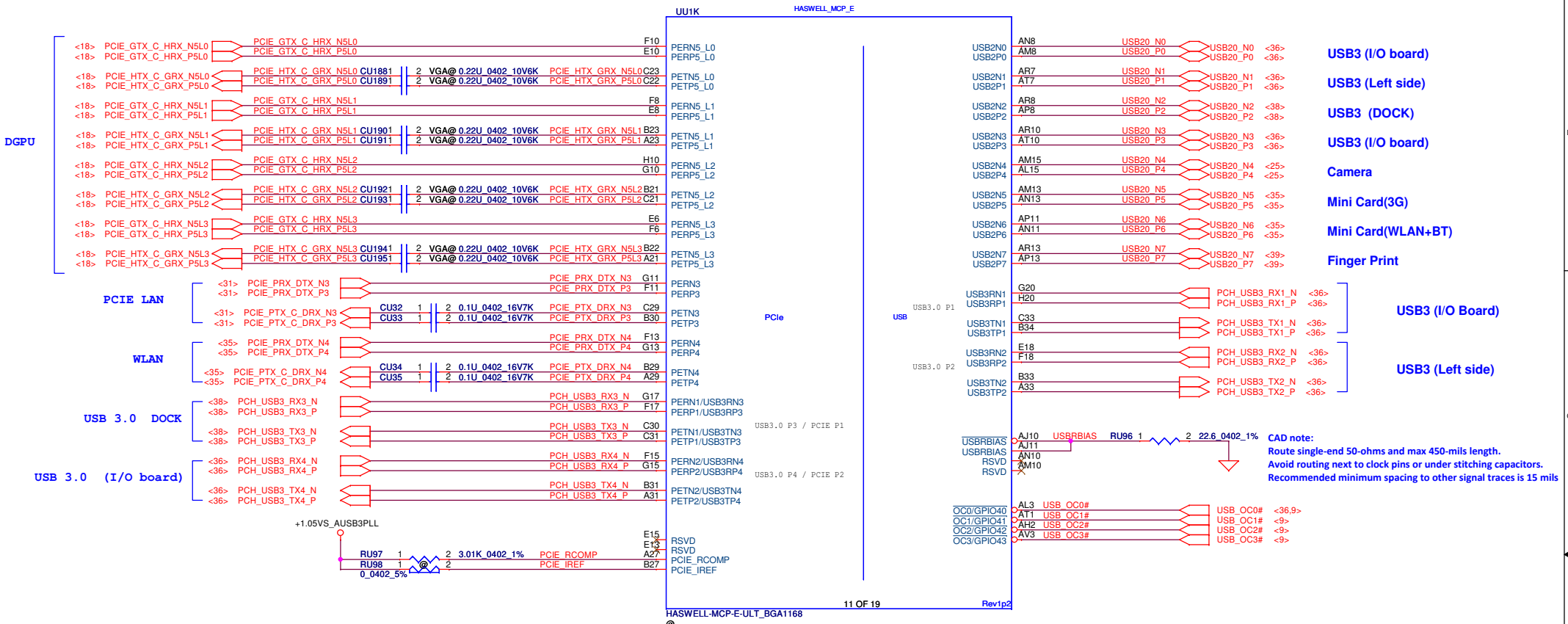
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.

Title: HSW MCP(6/11) GPIO,LPIO

Size: Custom | Document Number: LA-B731P | Rev: 1A

Date: Thursday, September 25, 2014 | Sheet 9 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.	
Title	HSW MCP(7/11) PCIE,USB
Size: Custom	Document Number: LA-B731P
Rev	1A
Date:	Wednesday, September 17, 2014
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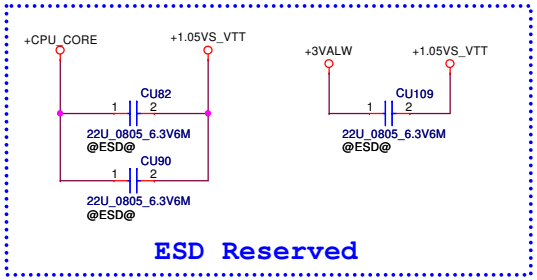
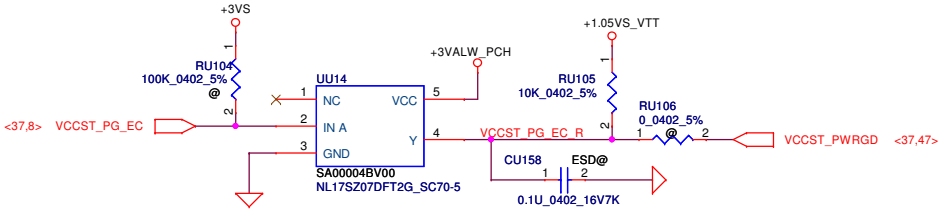
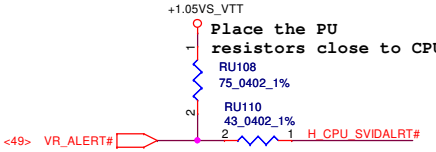
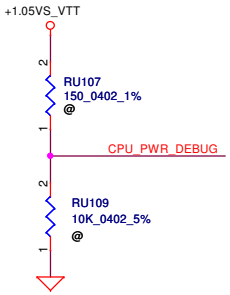


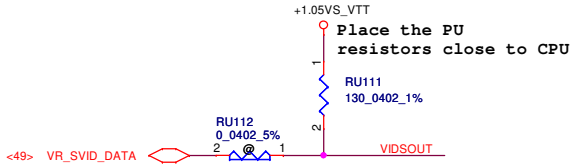


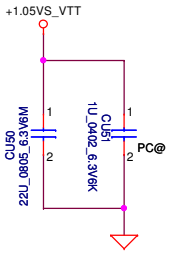
SVID ALERT

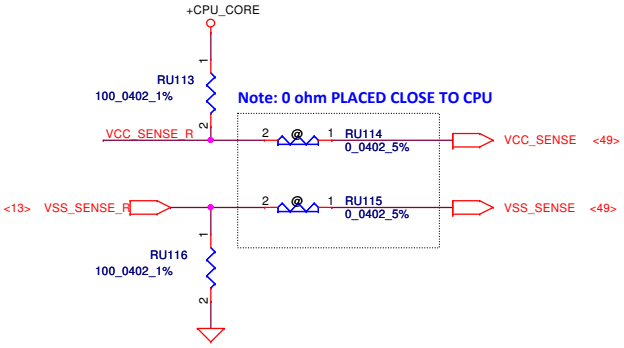


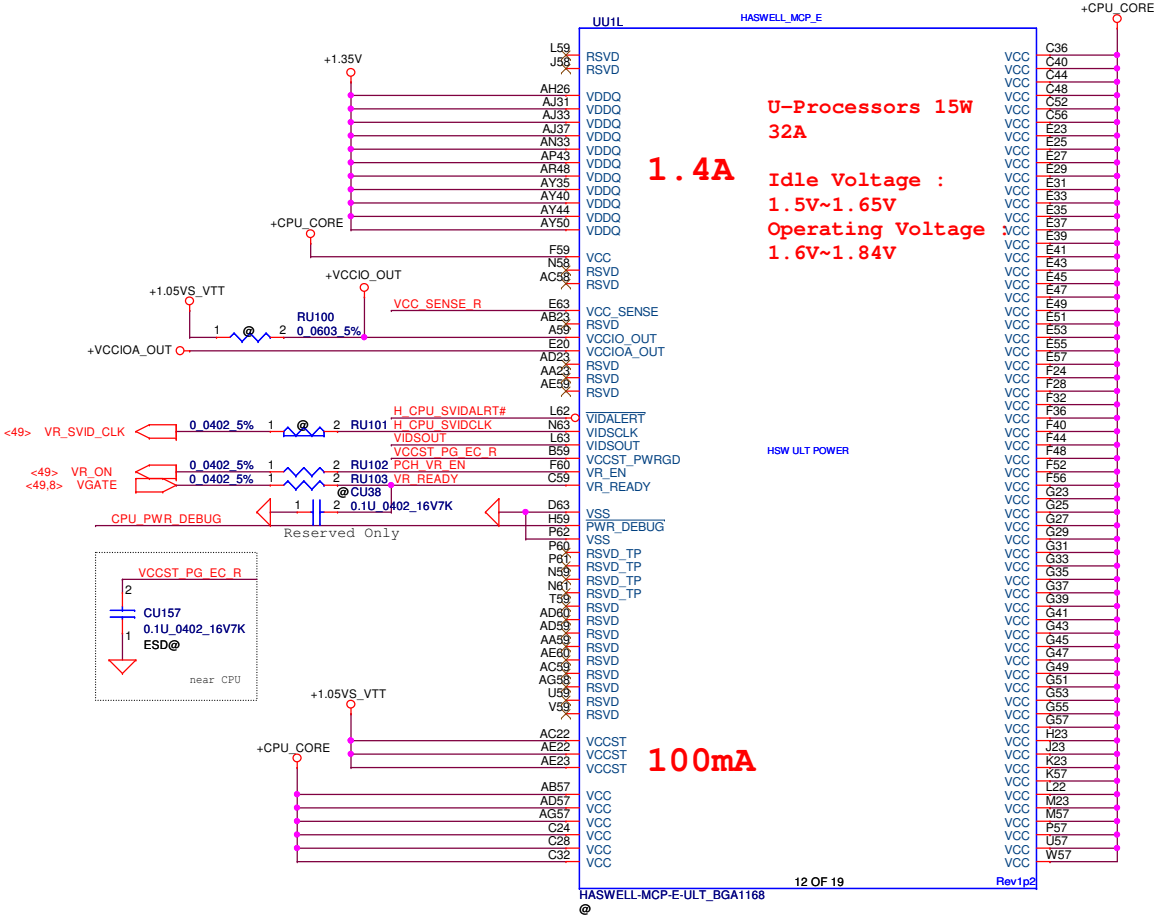


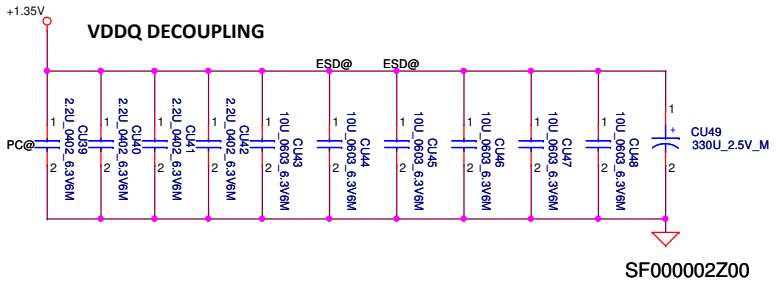
SVID DATA









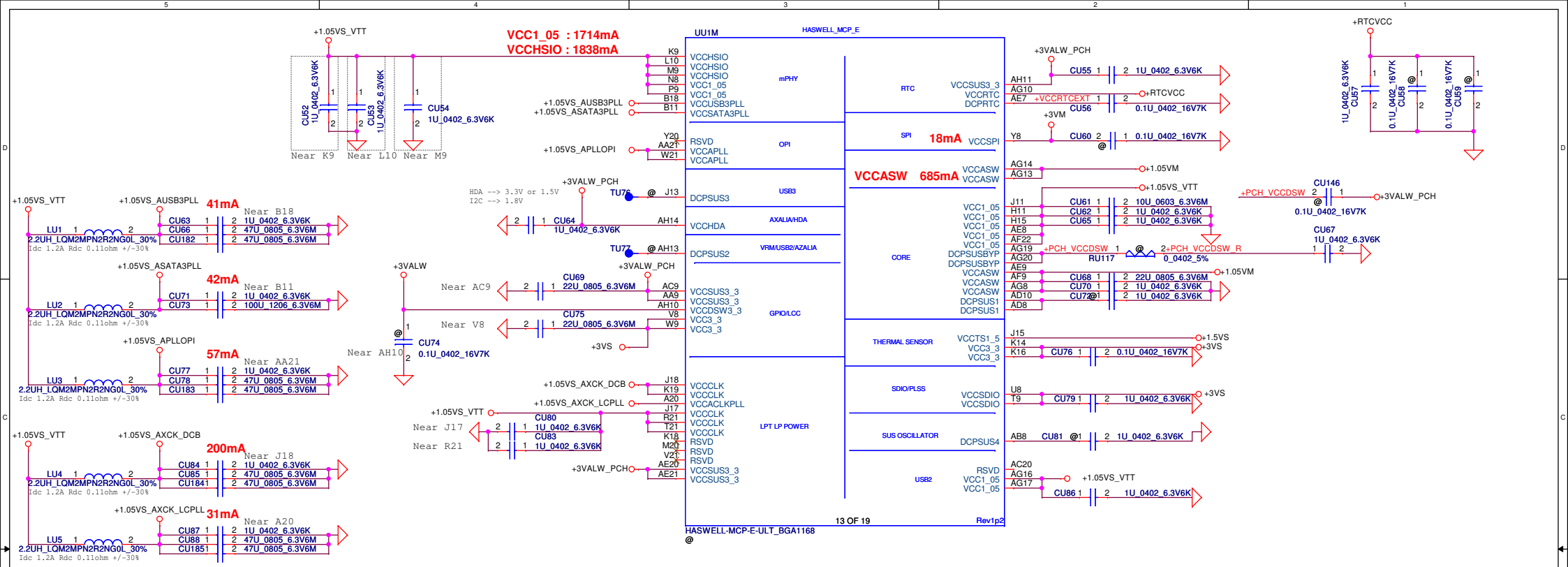


SF000002Z00

+1.35V : 470UF/2V/7343 *2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

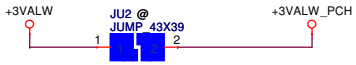
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.			
Title	HSW MCP(8/11) Power		
Size: Custom	Document Number: LA-B731P		Rev: 1A
Date: Wednesday, September 17, 2014	Sheet 11 of 56		



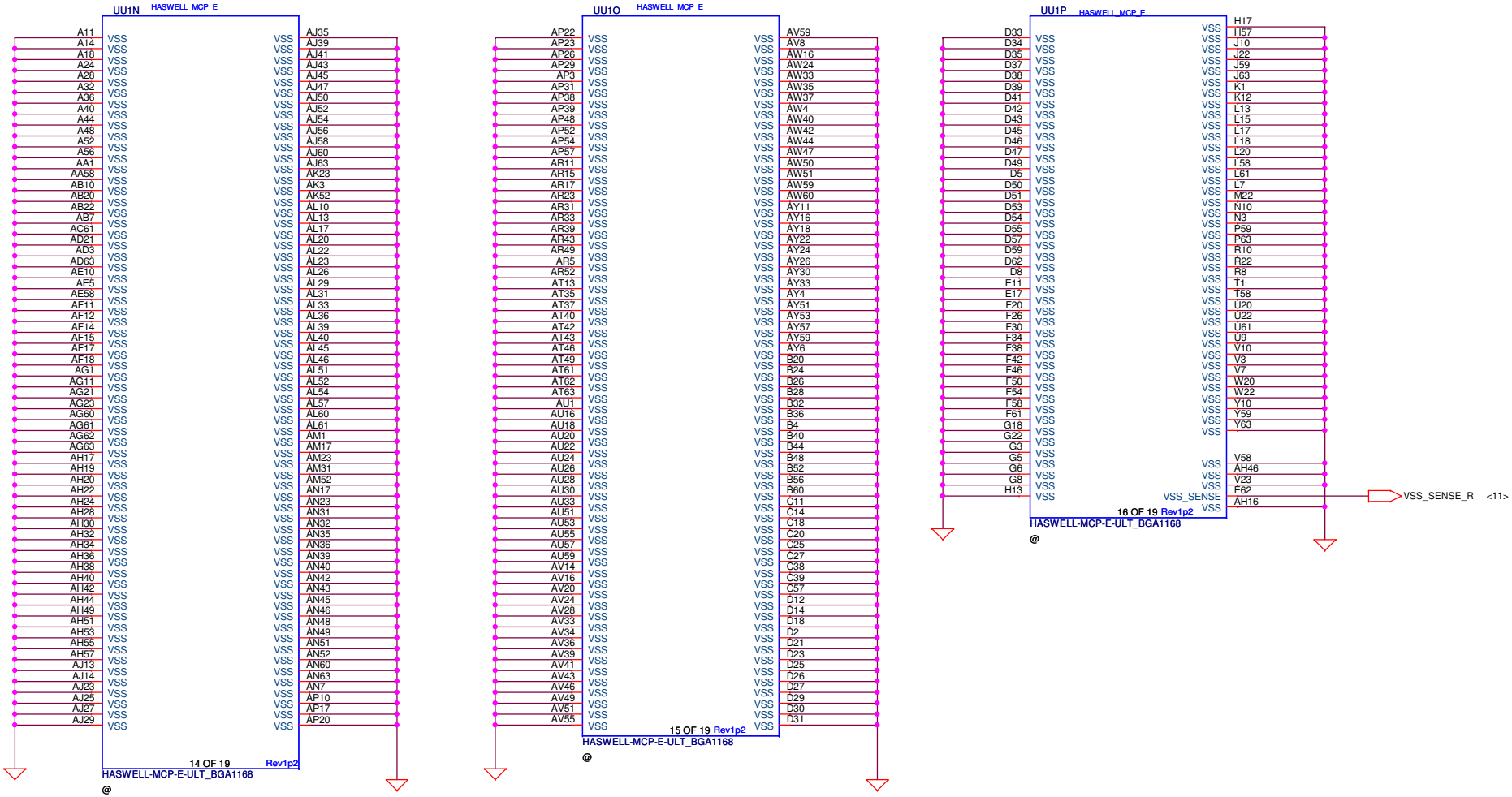
+3VALW TO +3VALW(PCH AUX Power)

Short J5 for PCH VCCSUS3.3



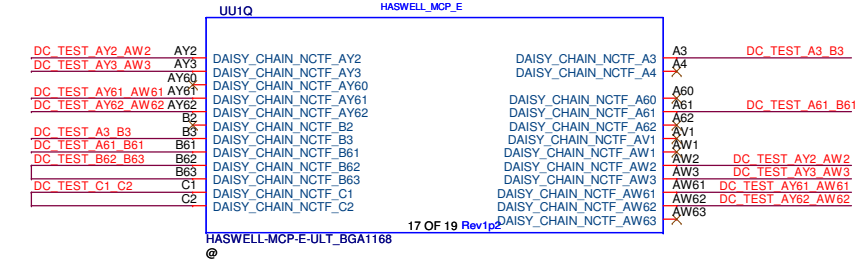
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

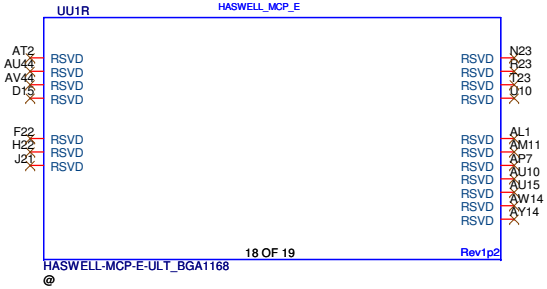
Compal Electronics, Inc.			
Title: HSW MCP(9/11) Power			
Size: Custom	Document Number: LA-B731P		Rev: 1A
Date: Wednesday, September 17, 2014	Sheet 12 of 56		

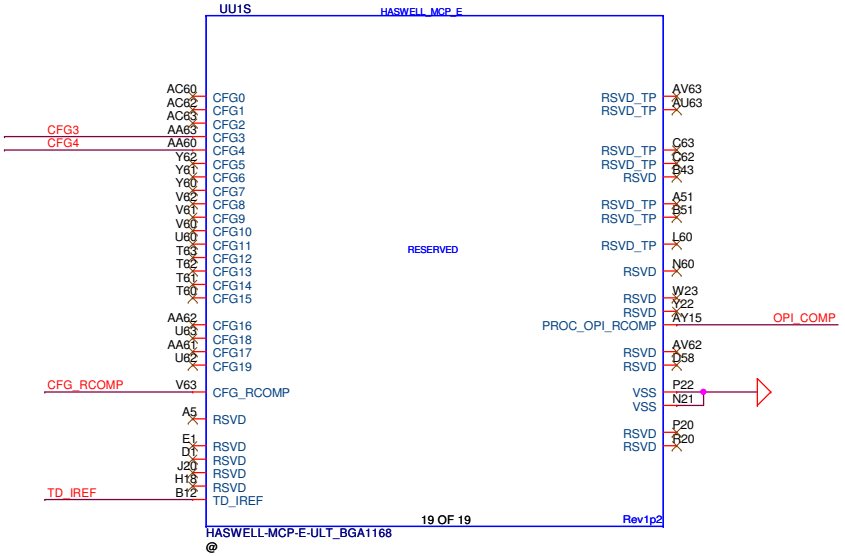


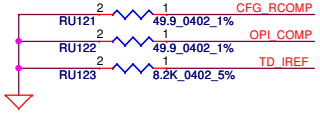
Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.			
Title	HSW MCP(10/11) GND		
Size: Custom	Document Number: LA-B731P		Rev: 1A
Date: Wednesday, September 17, 2014	Sheet 13 of 56		

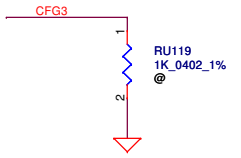




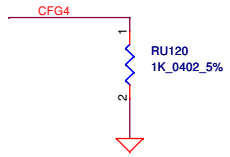




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.			
Title: HSW MCP(11/11) RSVD			
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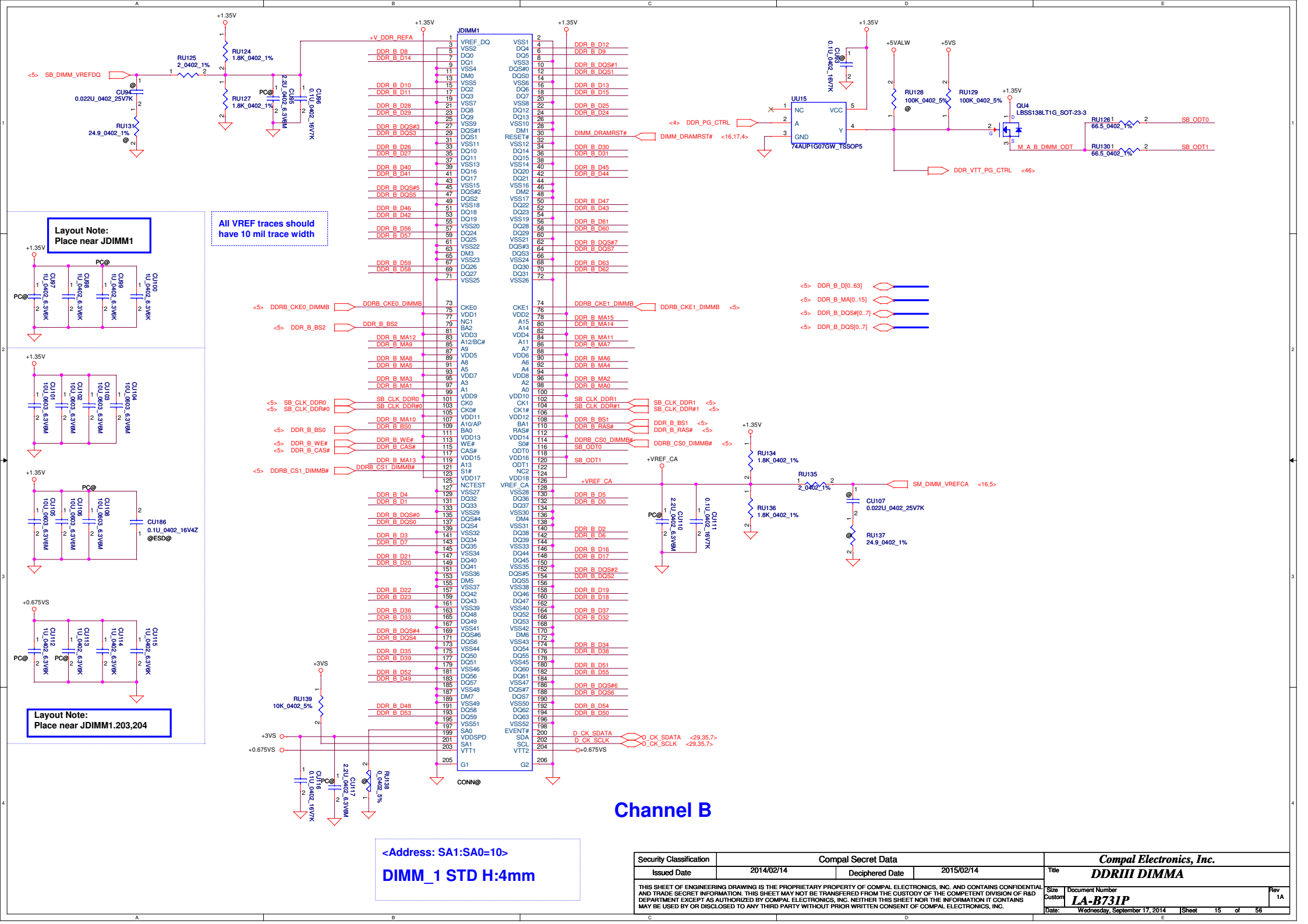

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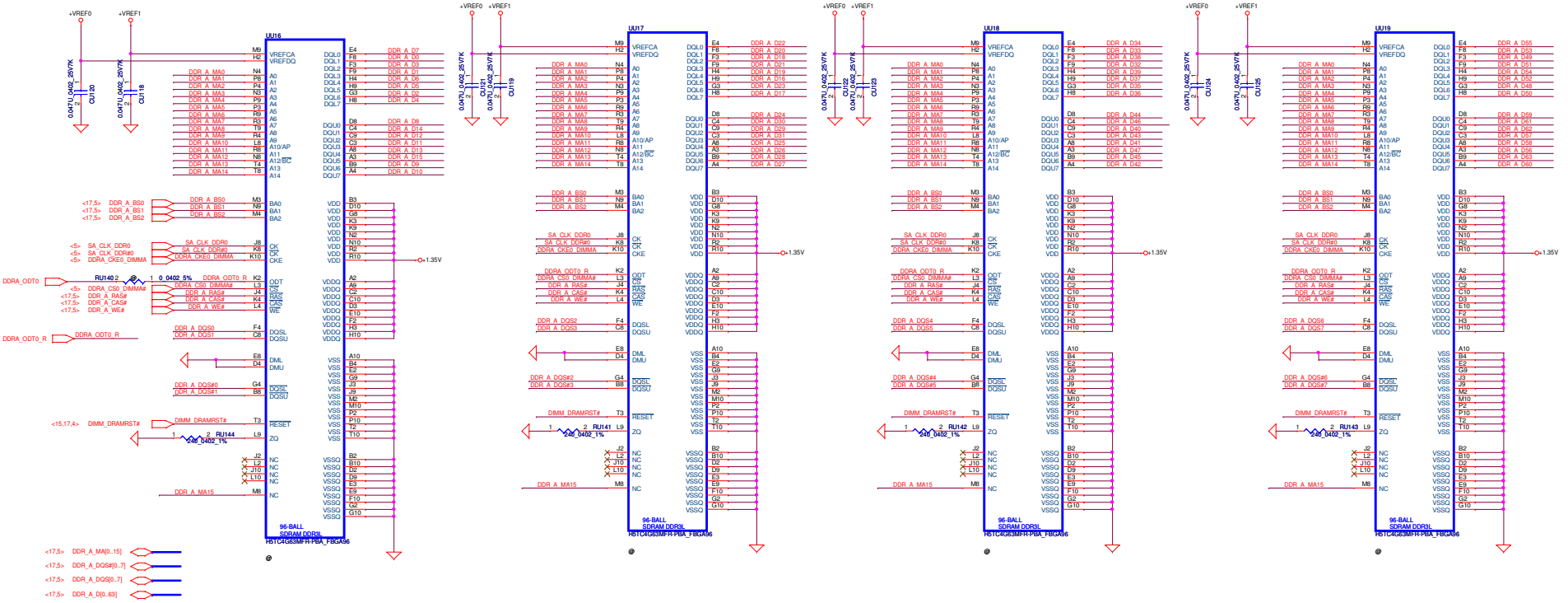
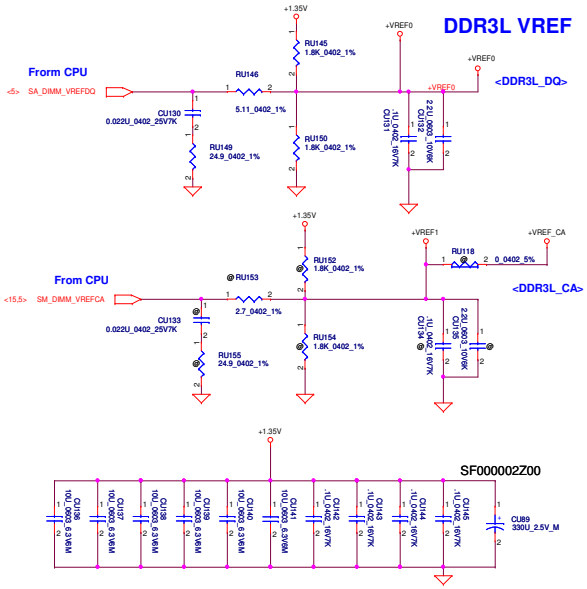


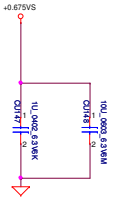
R Value = 34.8 Ohm

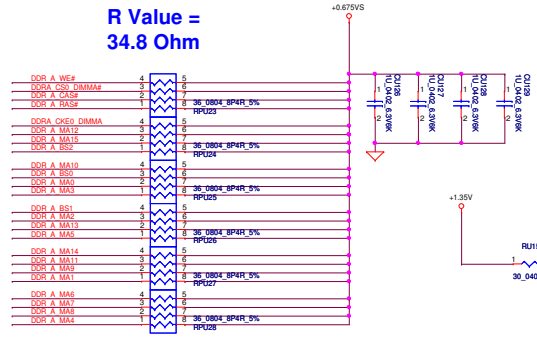
DDR3L VREF

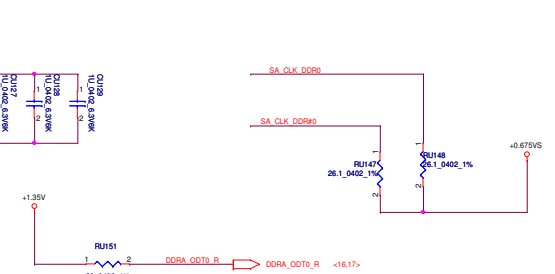
From CPU



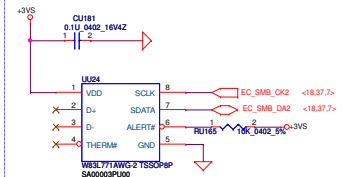
From CPU







External DDR Thermal Sensor



SA00003PU00
S IC W83L771AWG-2 TSSOP 8P SENSOR

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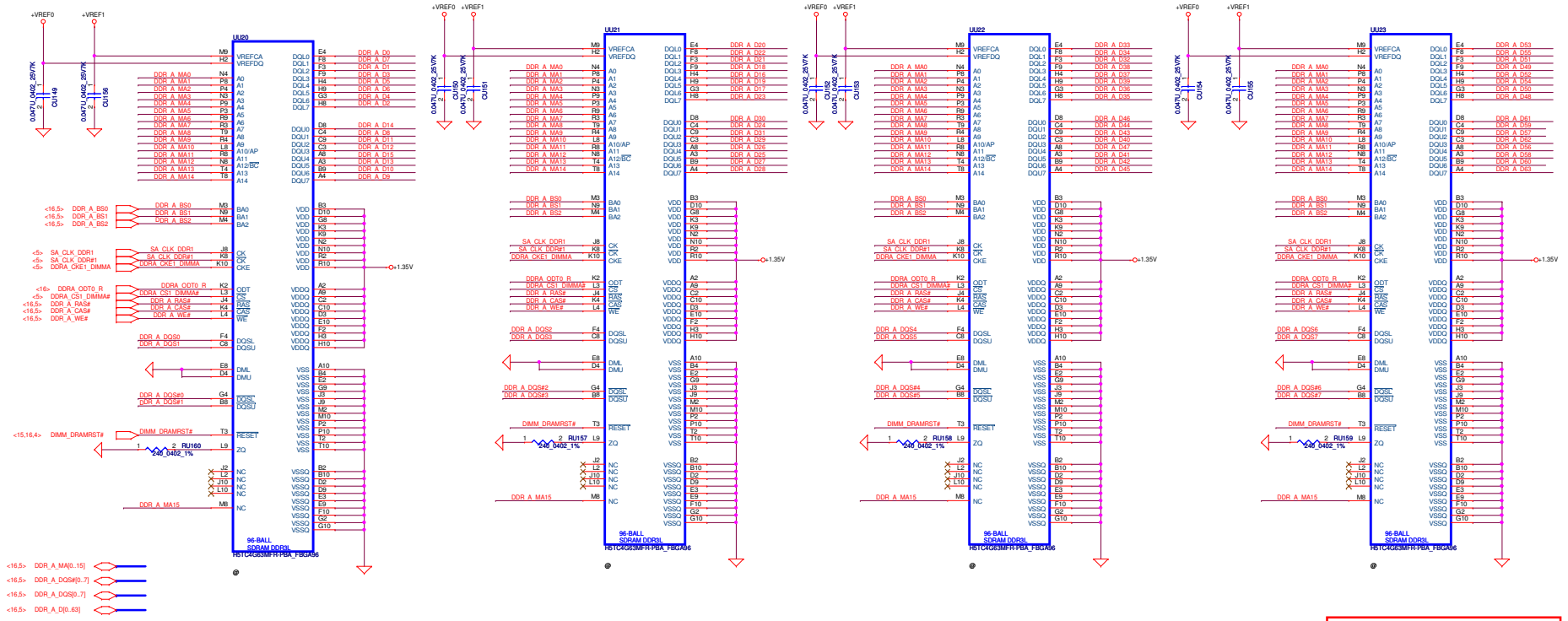
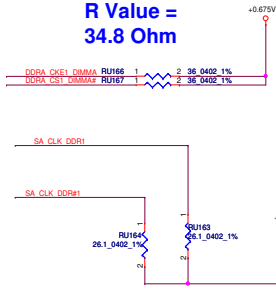
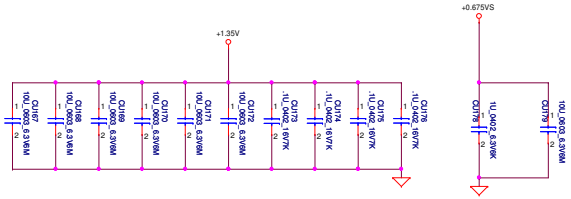


R Value = 34.8 Ohm





UU16 X76SHY0@ SA00005AV50	UU20 X76SHY0@ SA00005AV50	UU17 X76SHY0@ SA00005AV50	UU21 X76SHY0@ SA00005AV50
UU18 X76SHY0@ SA00005AV50	UU22 X76SHY0@ SA00005AV50	UU19 X76SHY0@ SA00005AV50	UU23 X76SHY0@ SA00005AV50

H5TC4G63AFR-PBA ABO!

UU16 X76SEP0@ SA00005HT80	UU20 X76SEP0@ SA00005HT80	UU17 X76SEP0@ SA00005HT80	UU21 X76SEP0@ SA00005HT80
UU18 X76SEP0@ SA00005HT80	UU22 X76SEP0@ SA00005HT80	UU19 X76SEP0@ SA00005HT80	UU23 X76SEP0@ SA00005HT80

EDJ4216EFBG-GNL-F FBGA 96P ABO !

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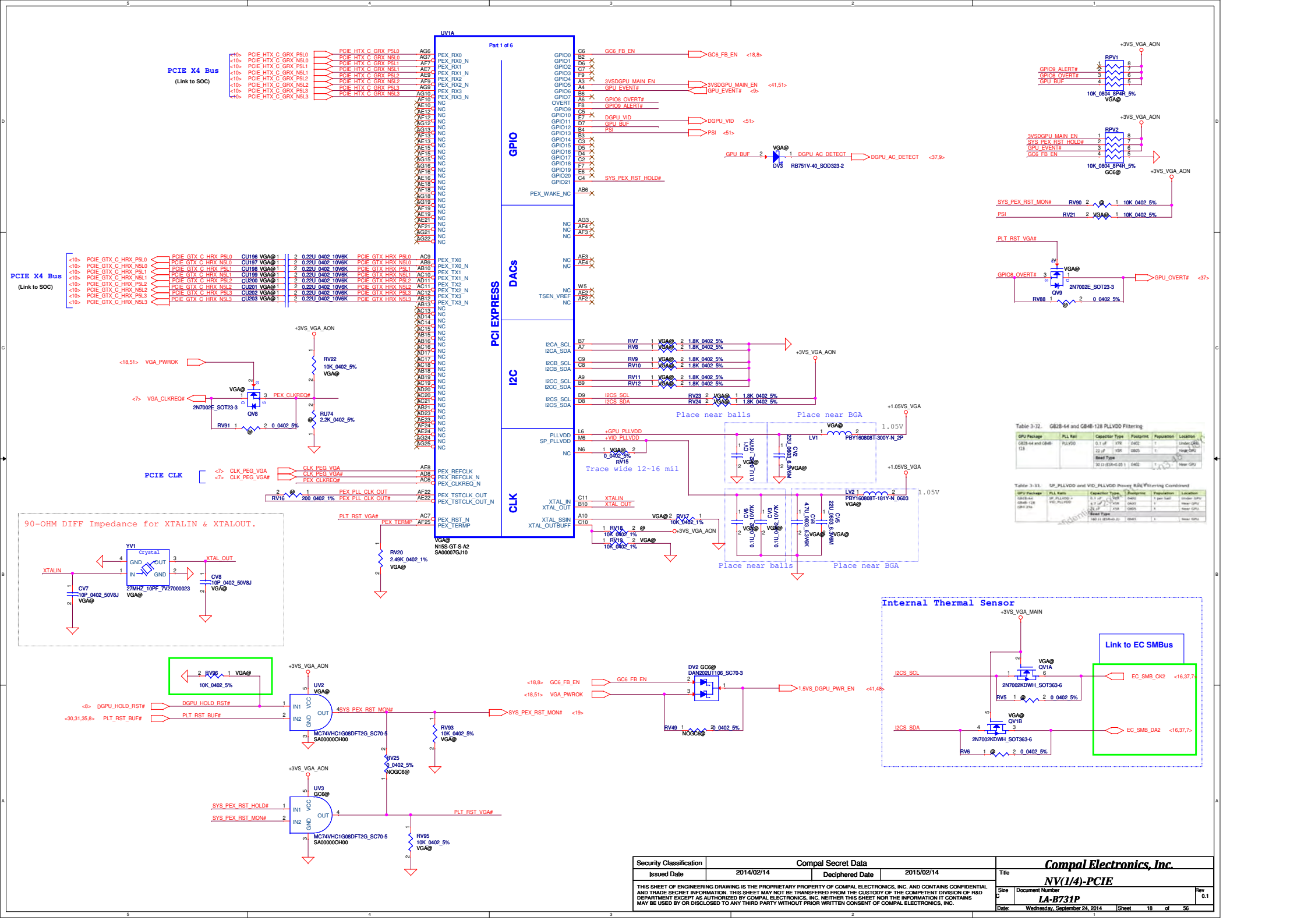

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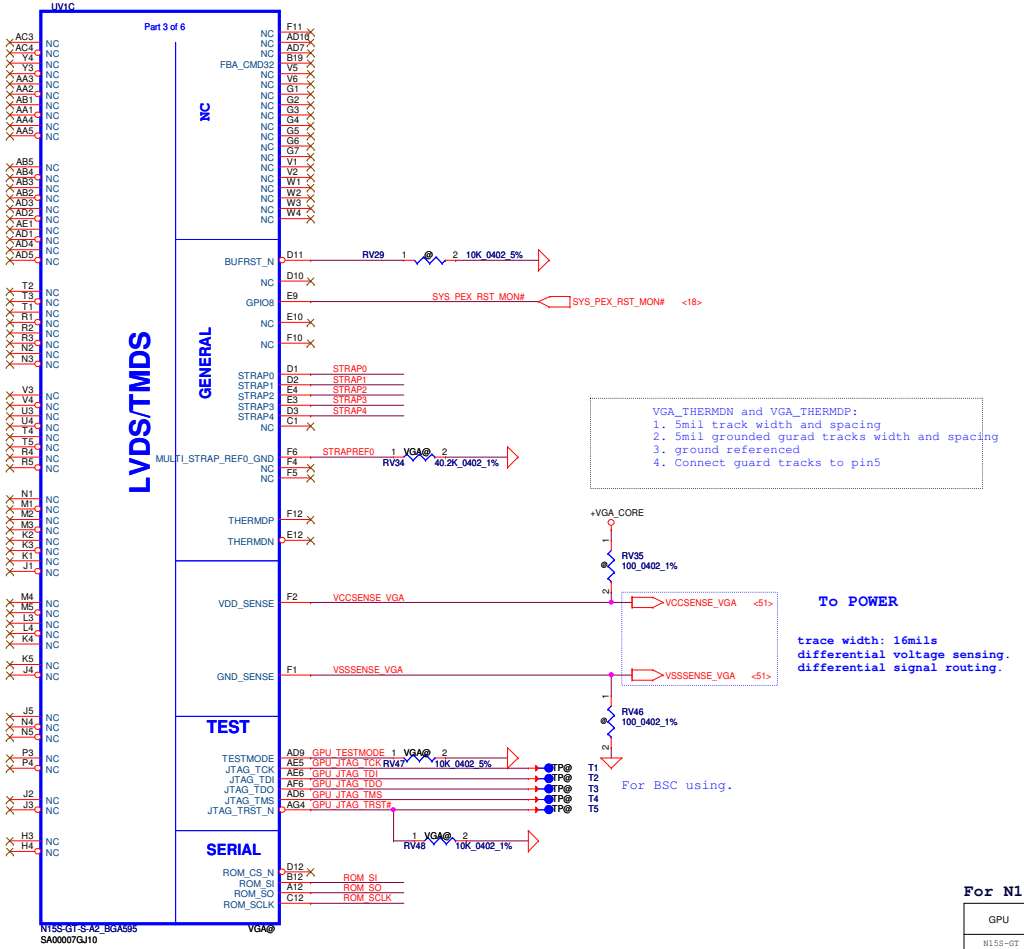
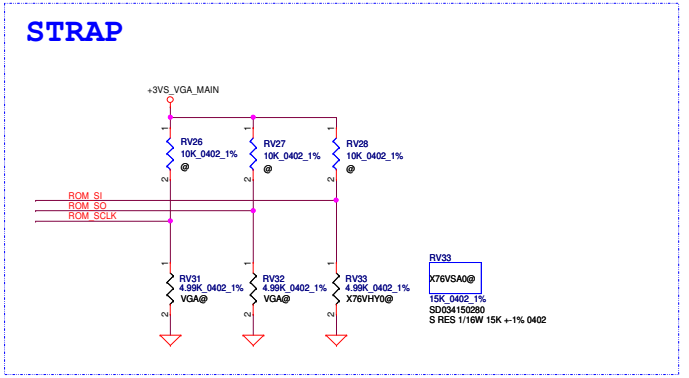


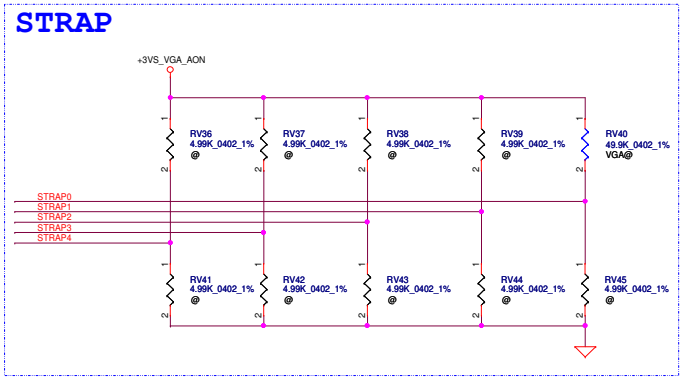
VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

To POWER

trace width: 16mils
differential voltage sensing.
differential signal routing.

For BSC using.





For N15S-GTstrap table

GPU	Frenq.	Memory Size	Memory Config	Strap	BitX	ROM_SI
N15S-GT	1000 MHz	256M* 16* 4 2G	Hynix H5TC4G63AFR-11C	0x0	0 0 0 0	R PD 4.99K
N15S-GT	1000 MHz	256M* 16* 4 2GB	Samsung K4W4G1646D-BC1A	0x2	0 0 1 0	R PD 15K

GB2B-64 Multi-Level Mode

Strap Pin Name	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_MAIN	SOR3_EXPOSED(*0)	SOR2_EXPOSED(*0)	SOR1_EXPOSED(*0)	SOR0_EXPOSED(*0)
ROM_SI	+3VS_MAIN	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_MAIN	DEVID_SEL(*0)	PCIE_CFG(*0)	SMB_ALT_ADDR(0*)	VGA_DEVICE(*0)
STRAP0	Keep foot print for pull up to 3V3_AON an pull down to GND and stuff 50 k ohm pull up				
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull up to 3V3_AON an pull down to GND for forward compatibility				

Resistor Values(1%)	Pull-up to +3VS_MAIN	Pull-down to Gnd
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

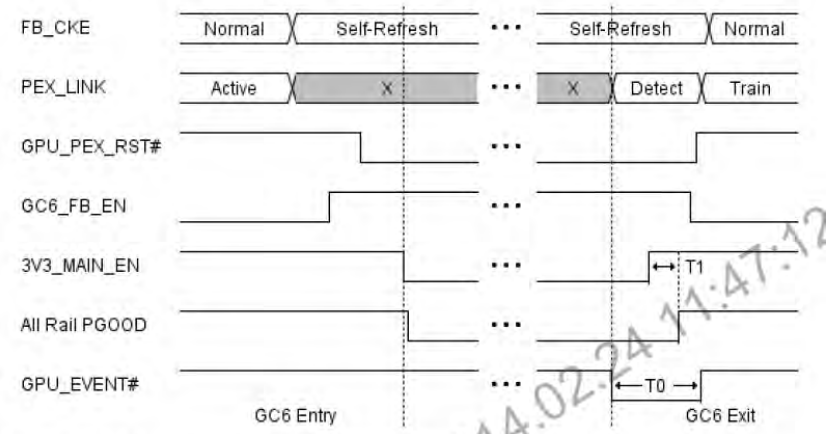


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

2014.02.24 11:47:12

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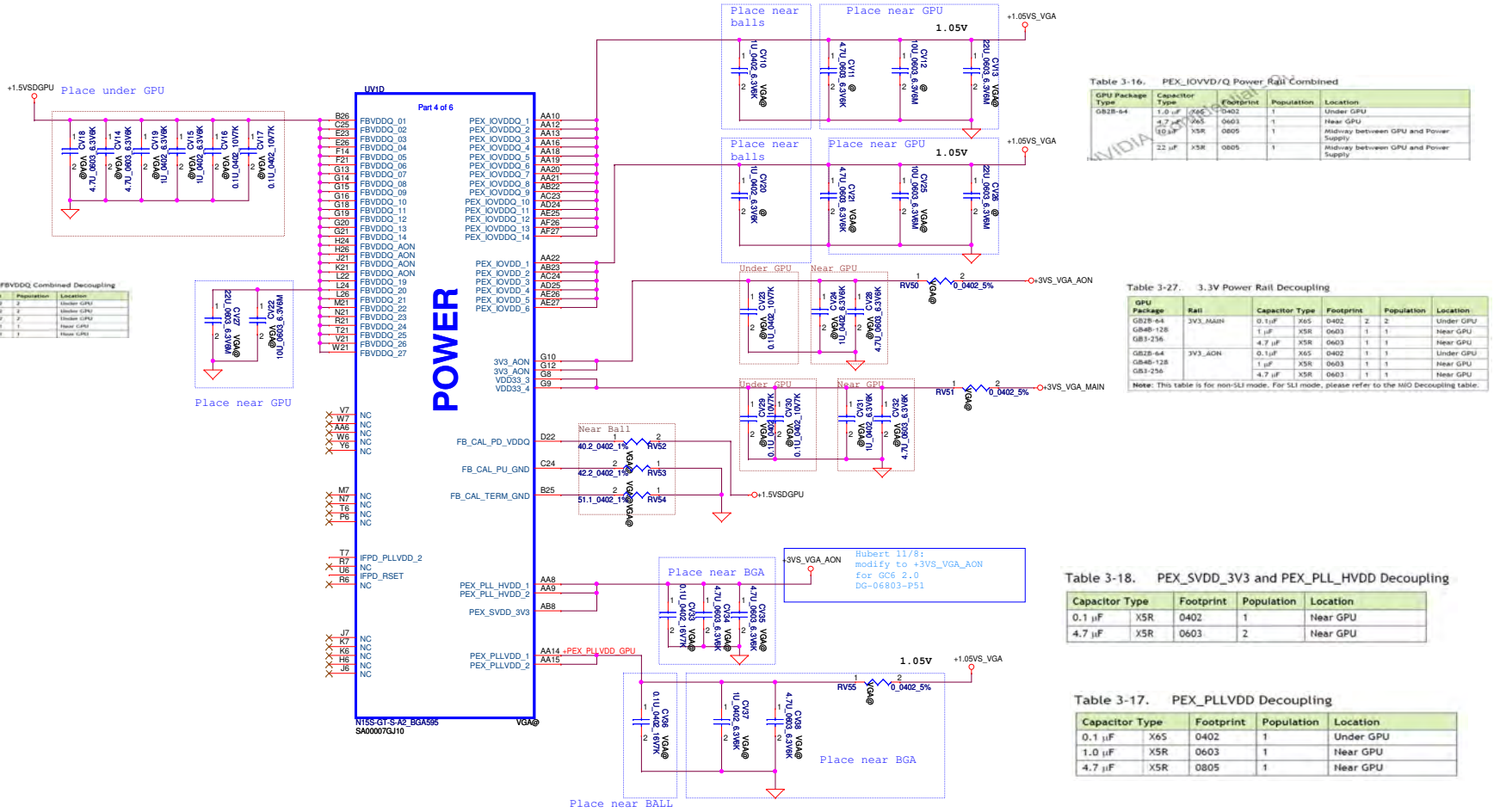

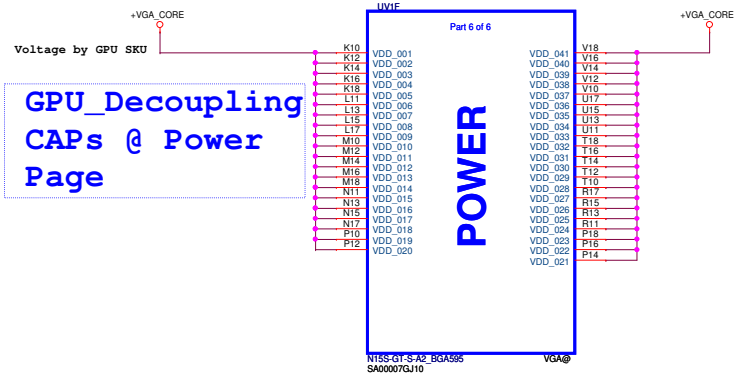

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Title: NV(3/4)-POWER

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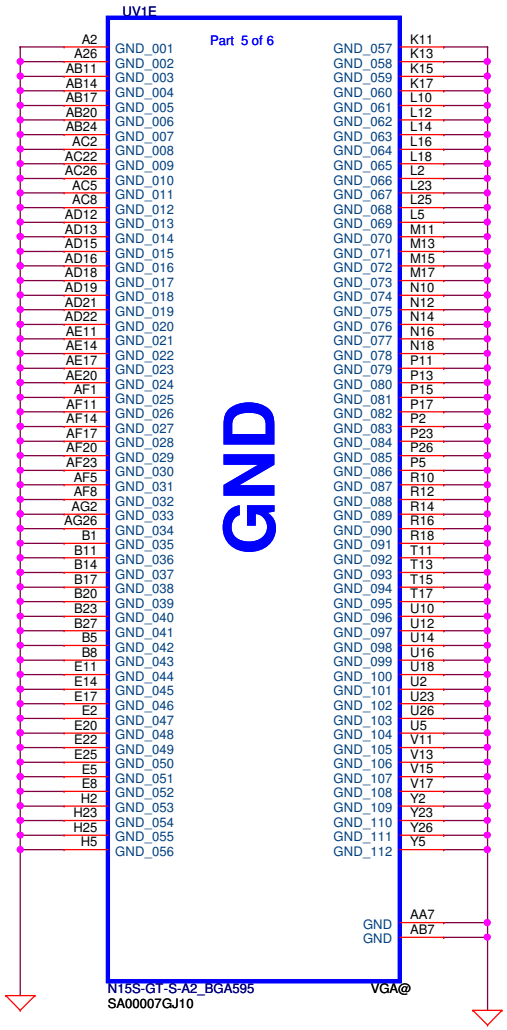

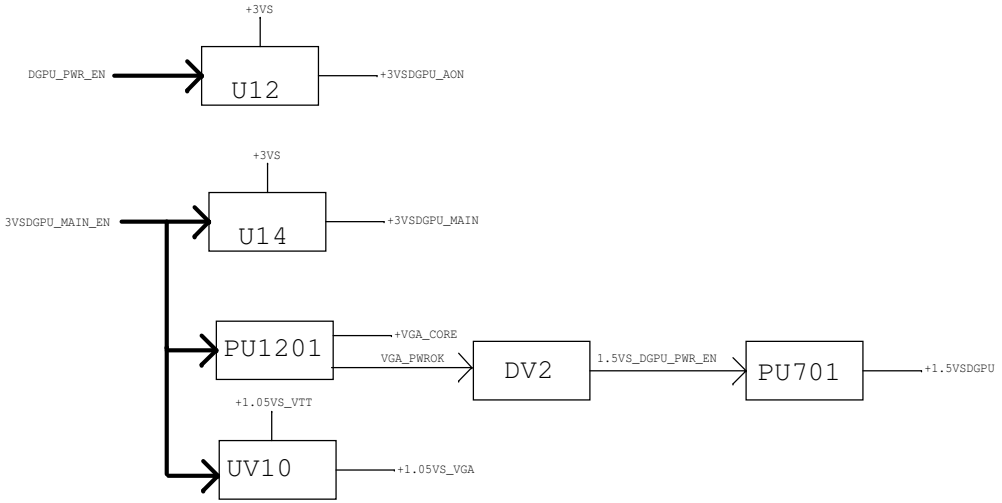

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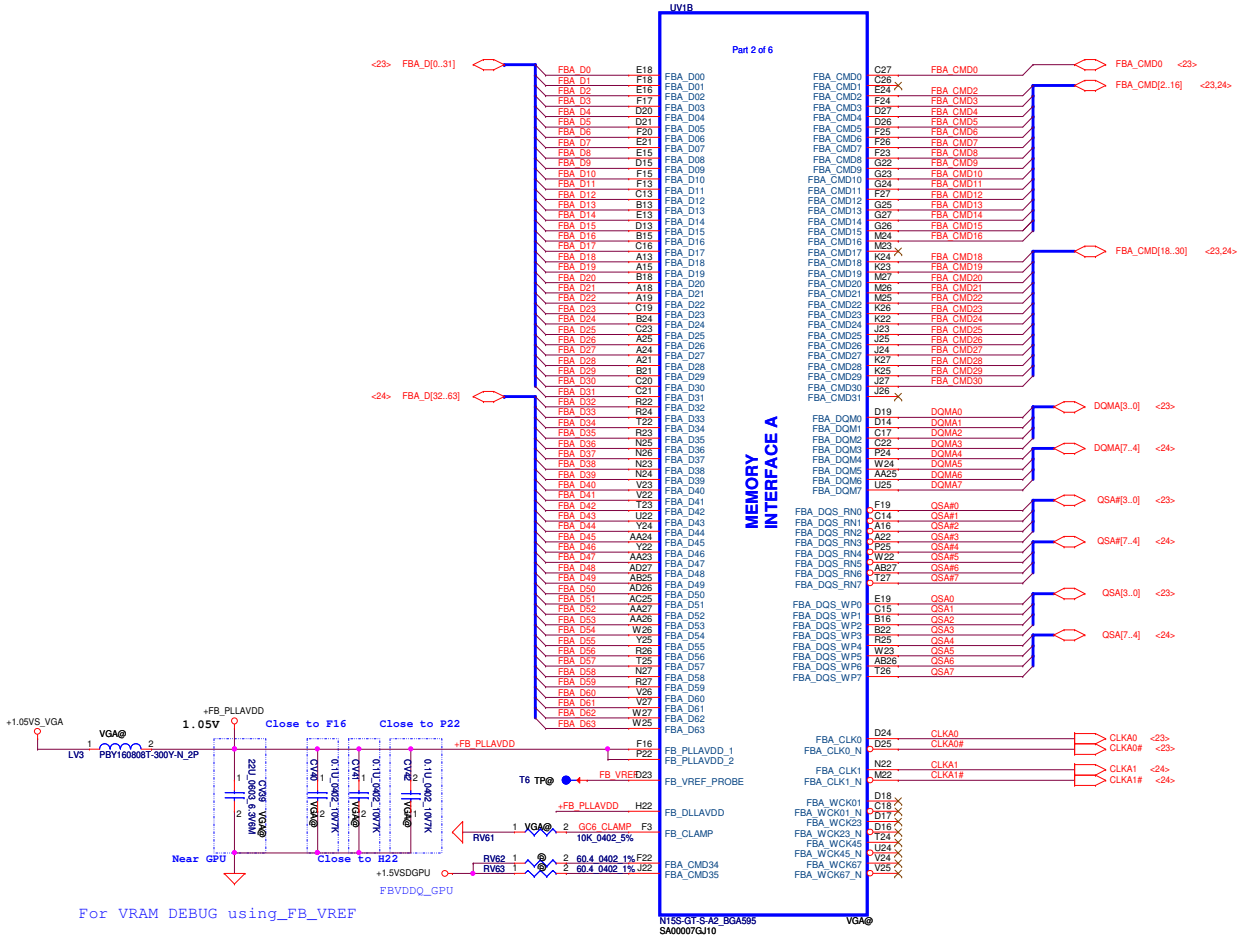

6.1.10 Memory ODTx, CKEx, and RST Termination

DDR3 requires Memory Termination on CKEx, ODTx and Memory Reset (RST). Table 6-8 describes the required termination.

Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 k
CKEx	10 k
RST	10 k
CS*	No Termination

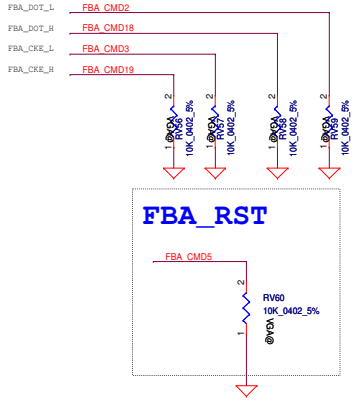

Table 3-14. FBx_PLL_AVDD and FB_DLL_AVDD Filtering

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

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Title: NV(4/4)-MEMORY FBA

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Memory Partition A – Lower 32 bits [31..0]

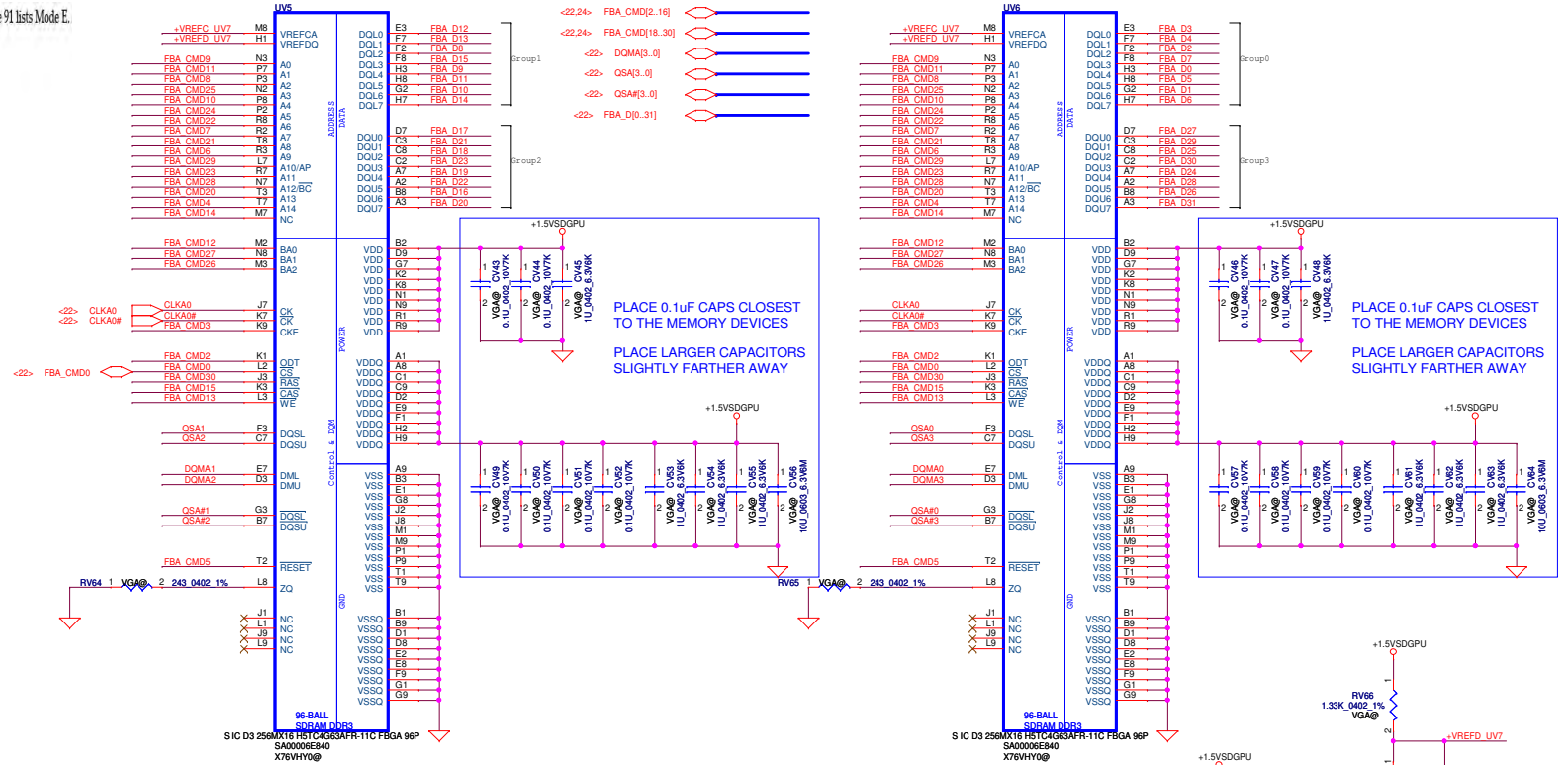
Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

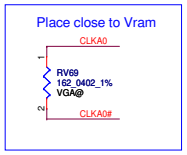
Table 6-3. Mode D Command Mapping

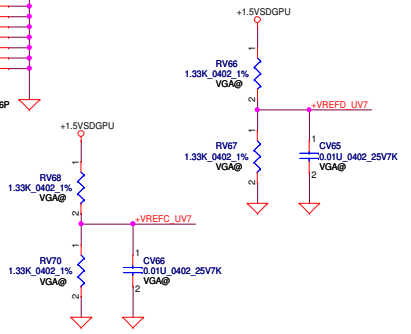
N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11







6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for N15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers[1]. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

Note: [1]Not including two additional layers for power planes.

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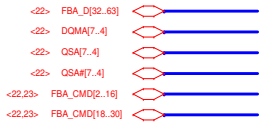
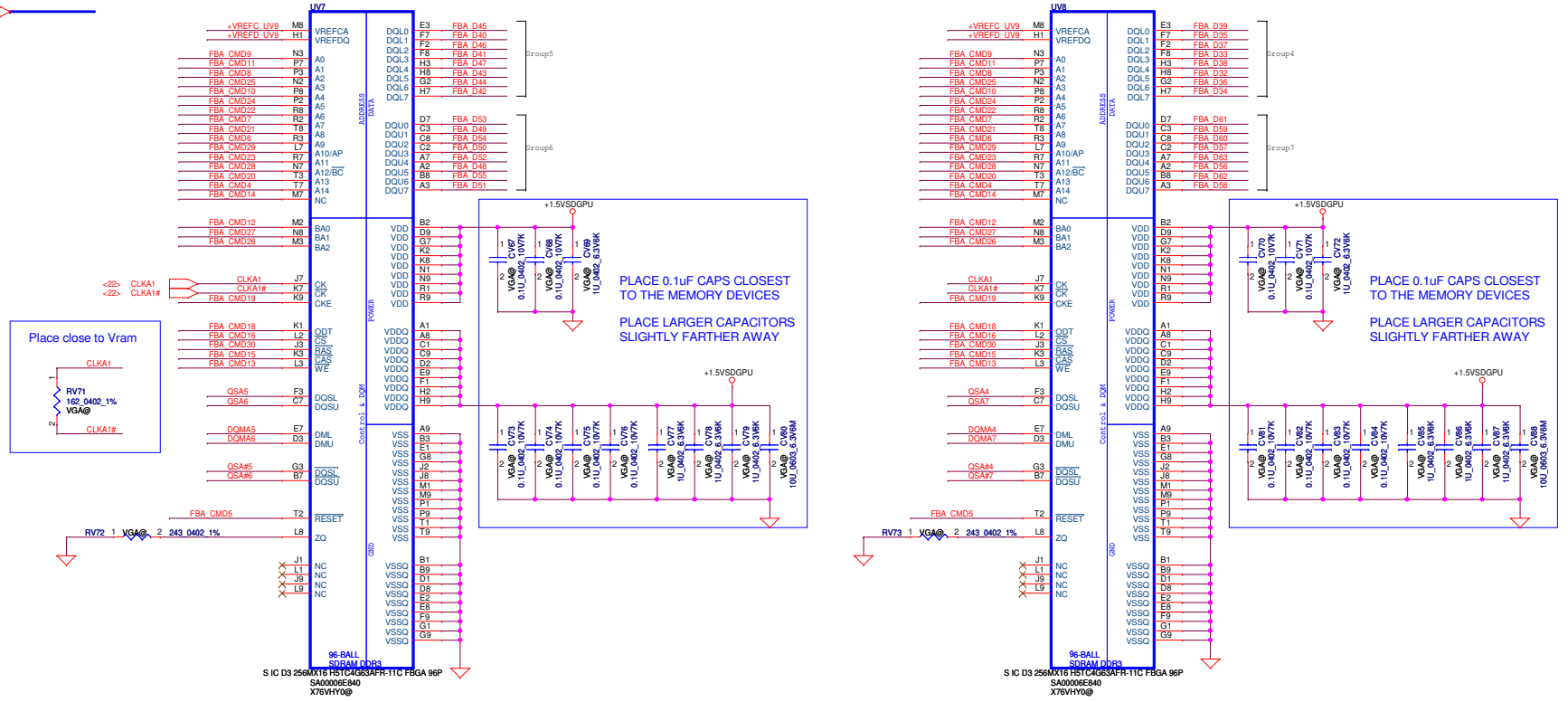
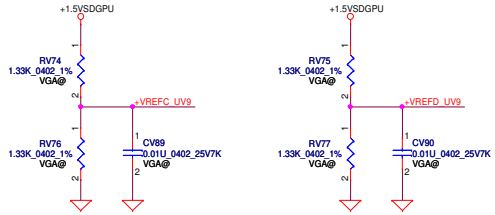
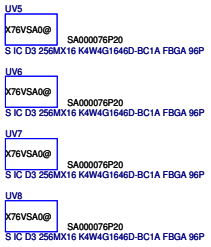
Memory Partition A - Upper 32 bits [64..32]









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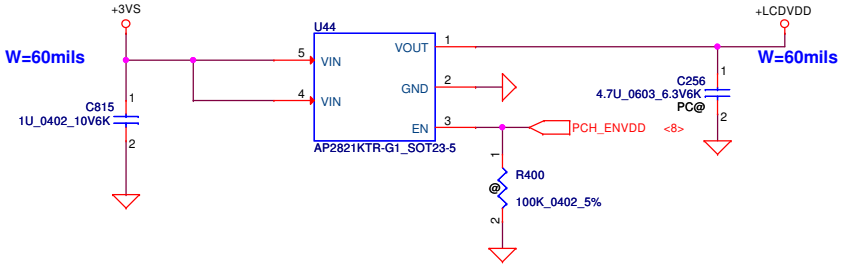
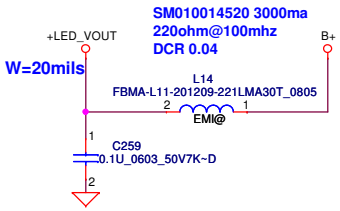
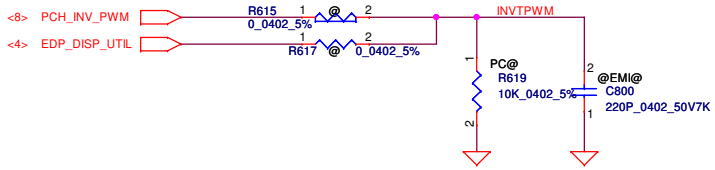
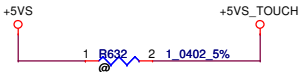
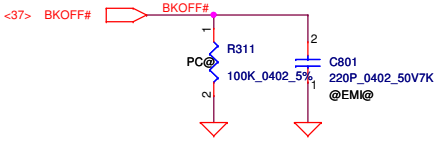
LCD POWER CIRCUIT

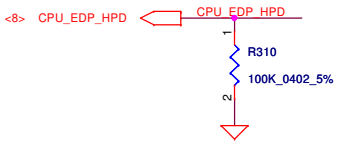


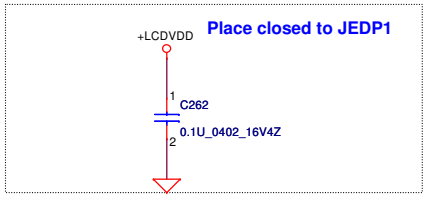




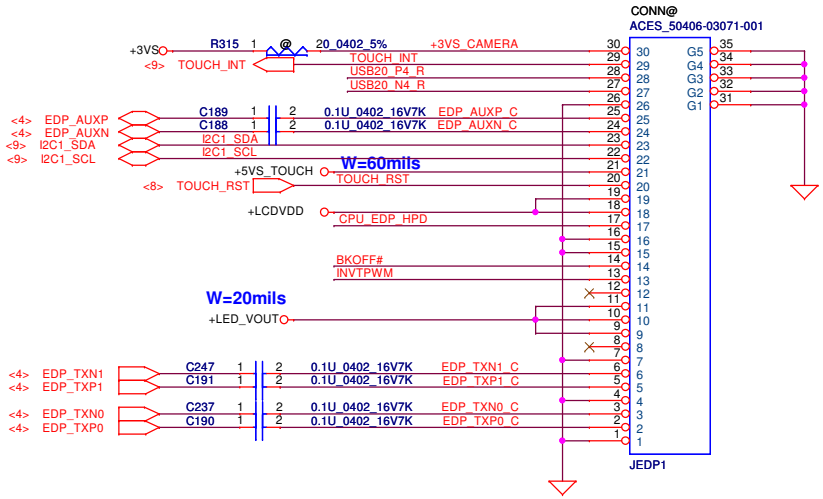




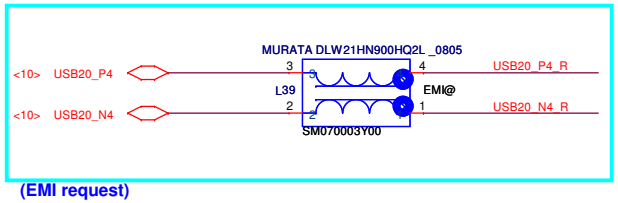




eDP PANEL Conn.



Camera



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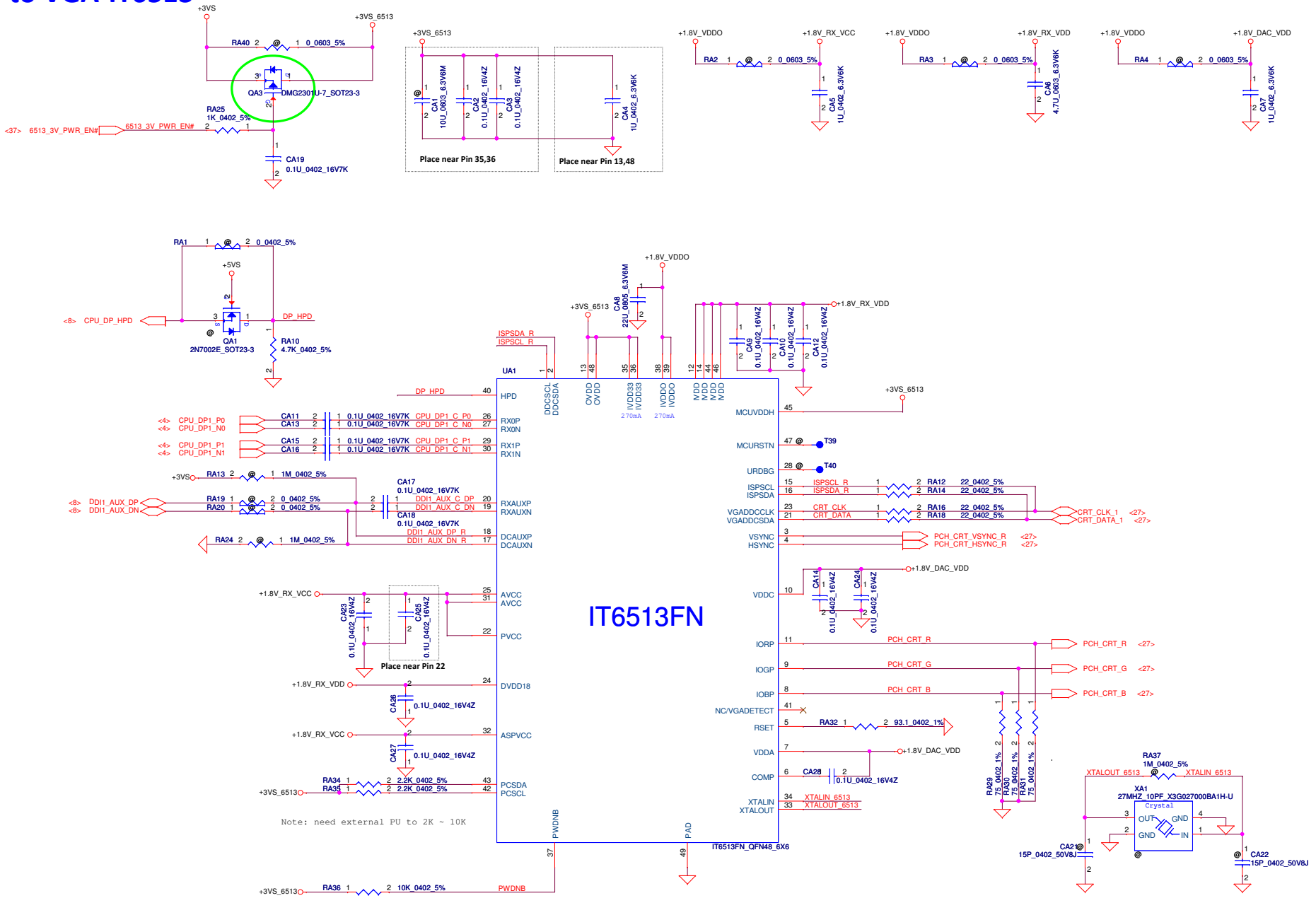
DP to VGA-IT6513



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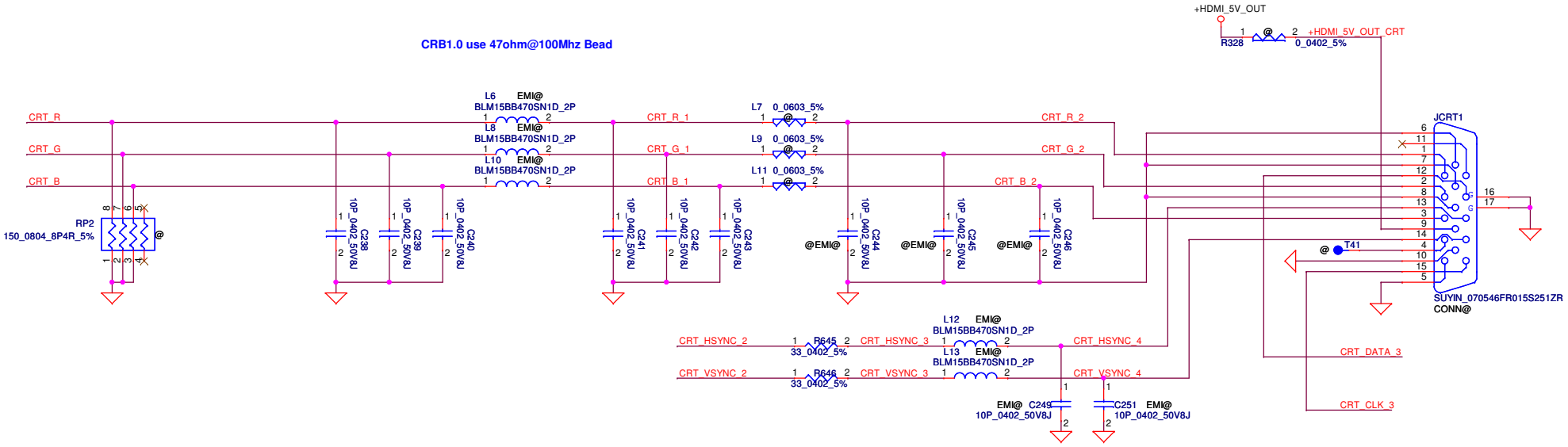
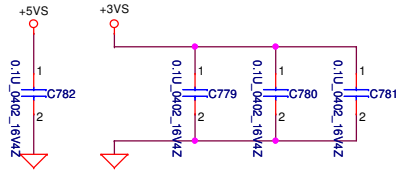
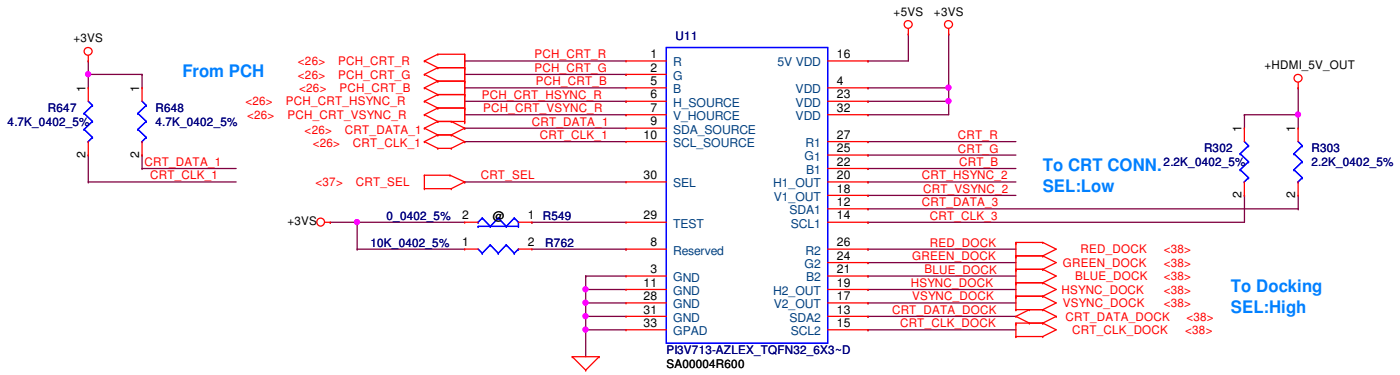
Title: ITE IT6513FN			
Size: Custom	Document Number: LA-B731P		Rev: 1A
Date: Wednesday, September 17, 2014	Sheet 26 of 56		

CRT Connector





SELx	Function
L	port 1 is chose
H	port 2 is chose



Compal Electronics, Inc.

Title: CRT CONN.

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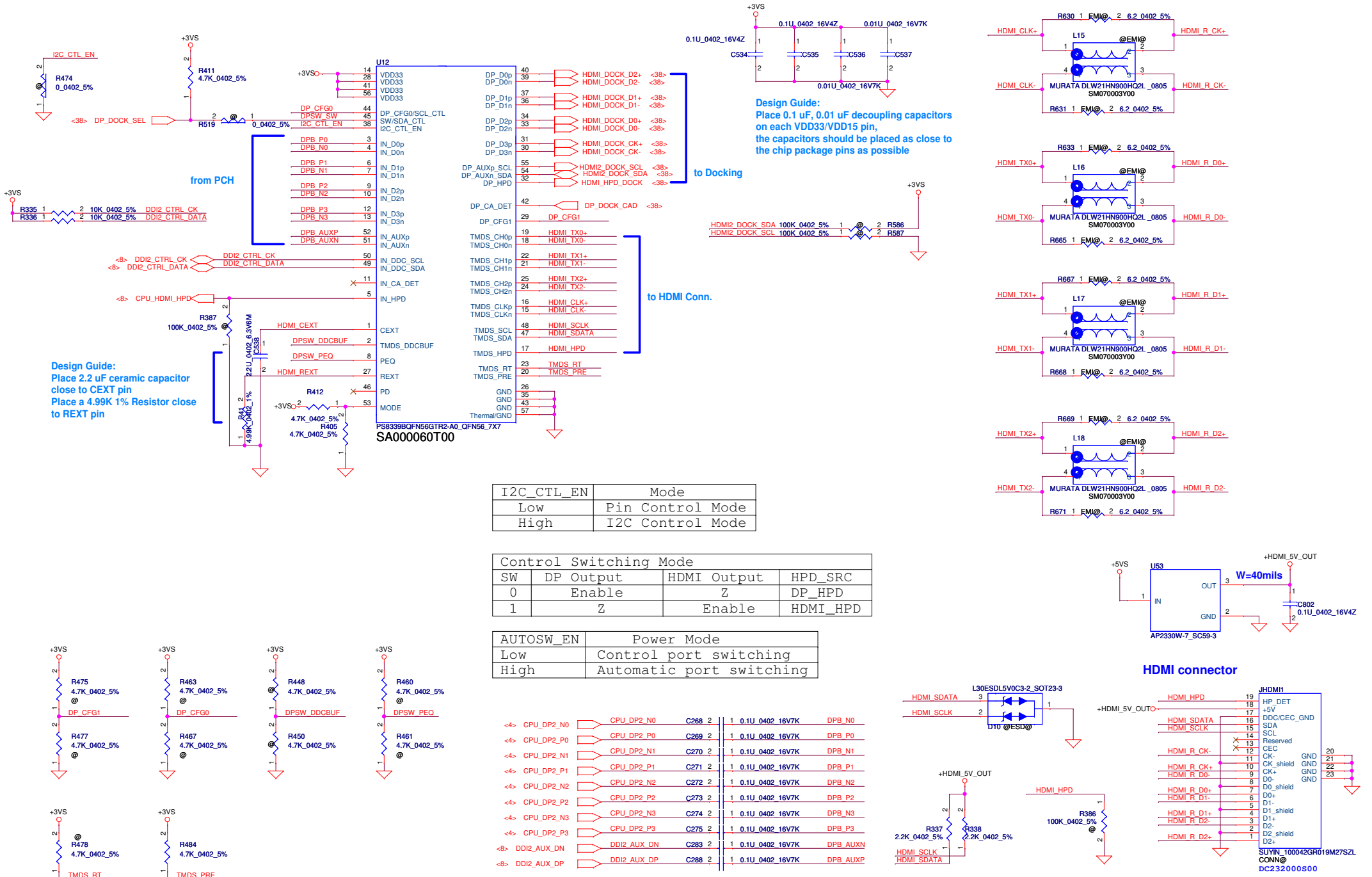

I2C_CTL_EN	Mode
Low	Pin Control Mode
High	I2C Control Mode

Control Switching Mode			
SW	DP Output	HDMI Output	HPD_SRC
0	Enable	Z	DP_HPD
1	Z	Enable	HDMI_HPD

AUTOSW_EN	Power Mode
Low	Control port switching
High	Automatic port switching

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Title	HDMI CONN.
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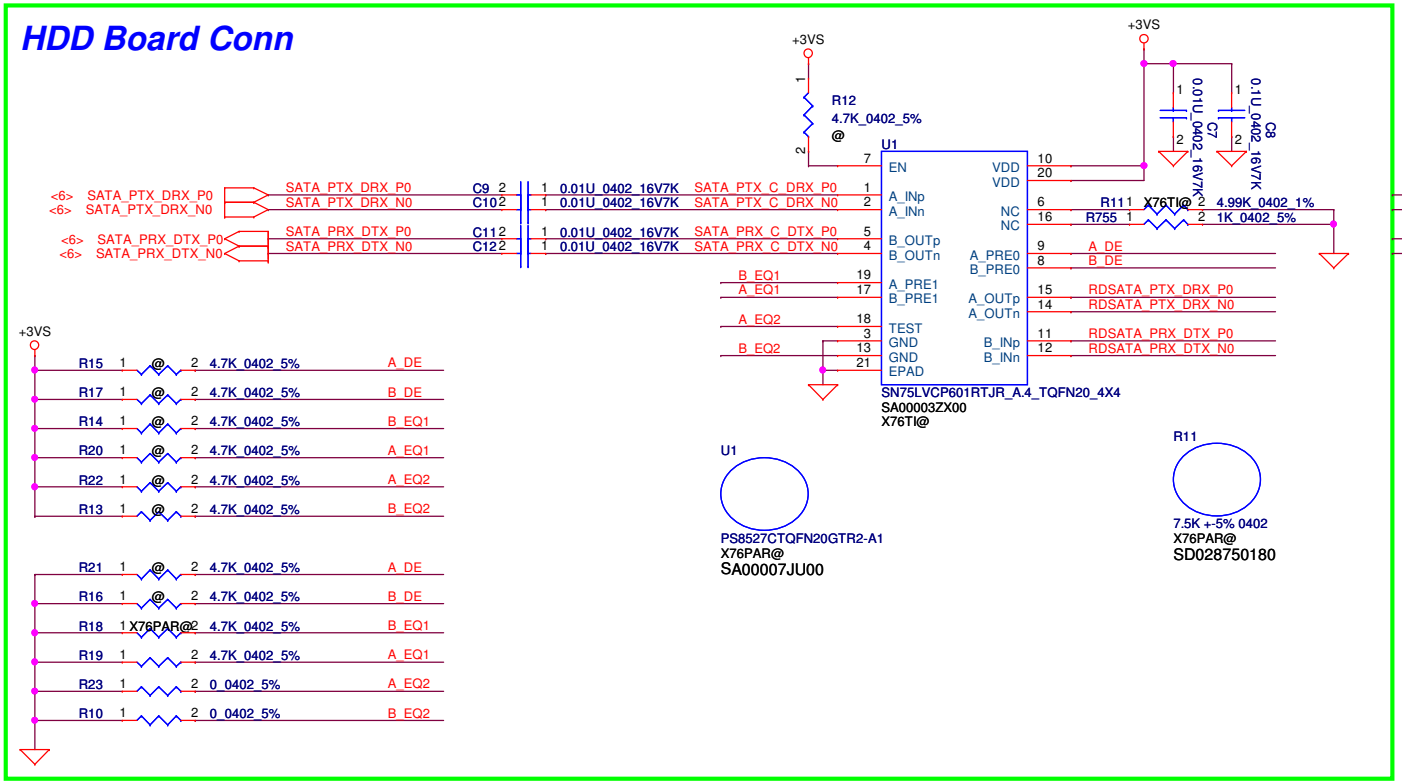
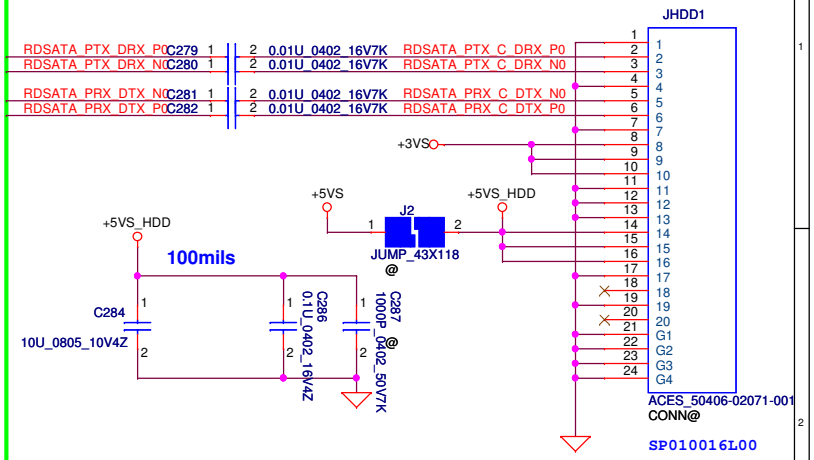
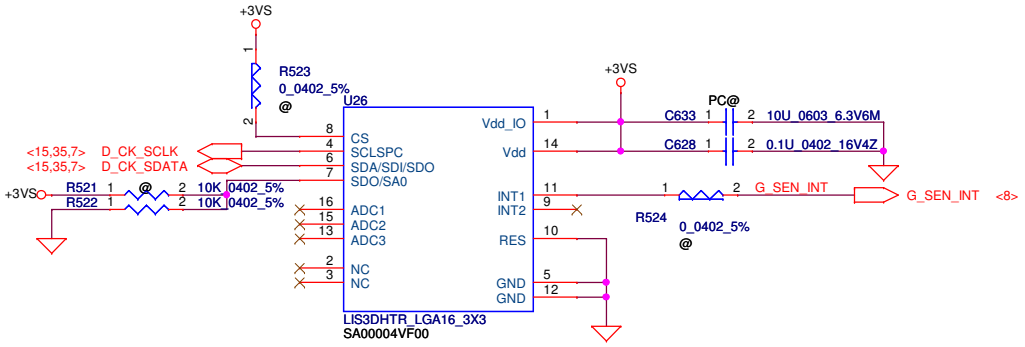
HDD Board Conn





APS G-Sensor



LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

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Compal Electronics, Inc.

Title: HDD & G-Sensor

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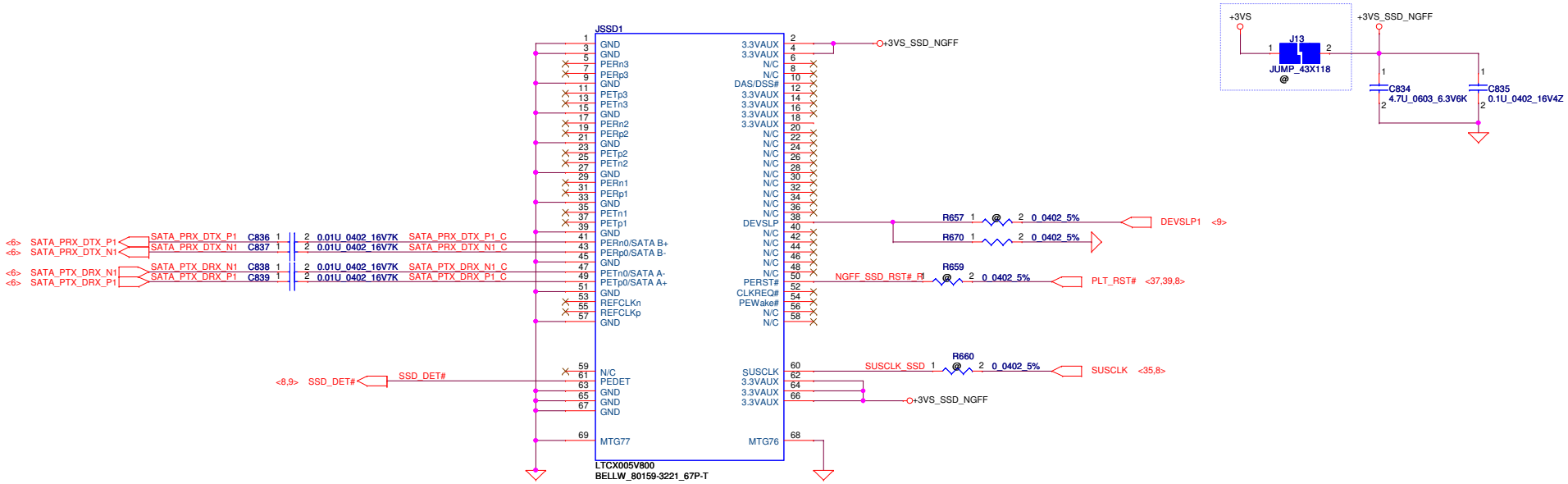

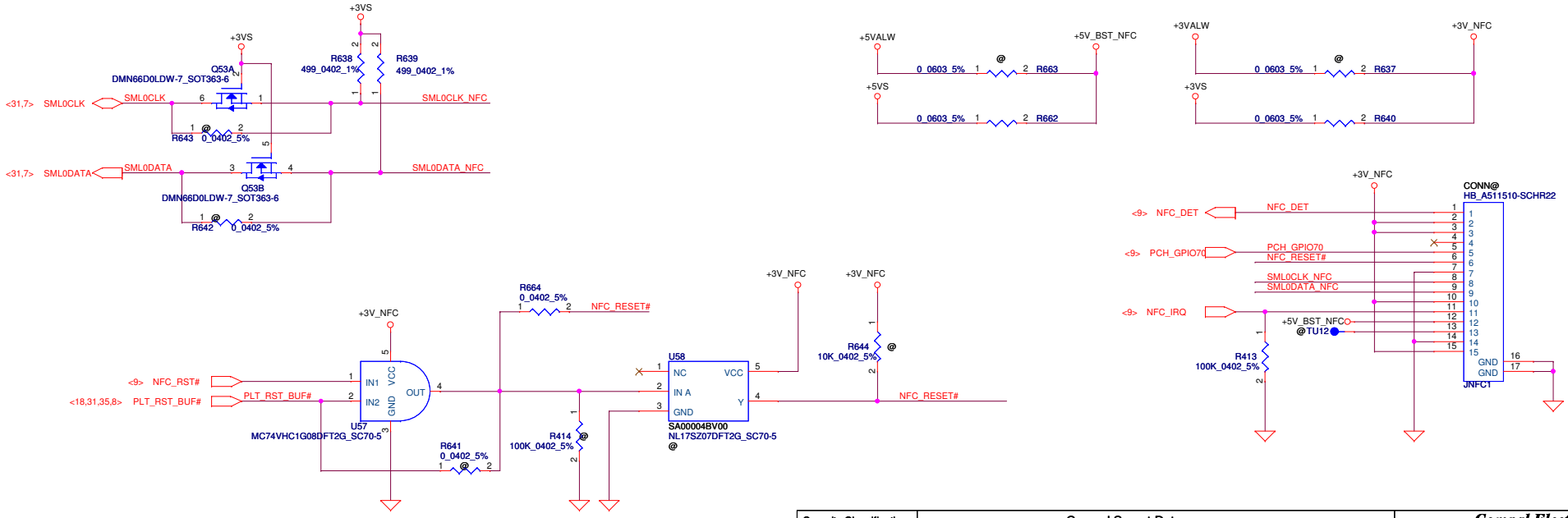

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Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.

Title: **mSATA & NFC**

Size	Document Number	Rev
Custom	LA-B731P	1A

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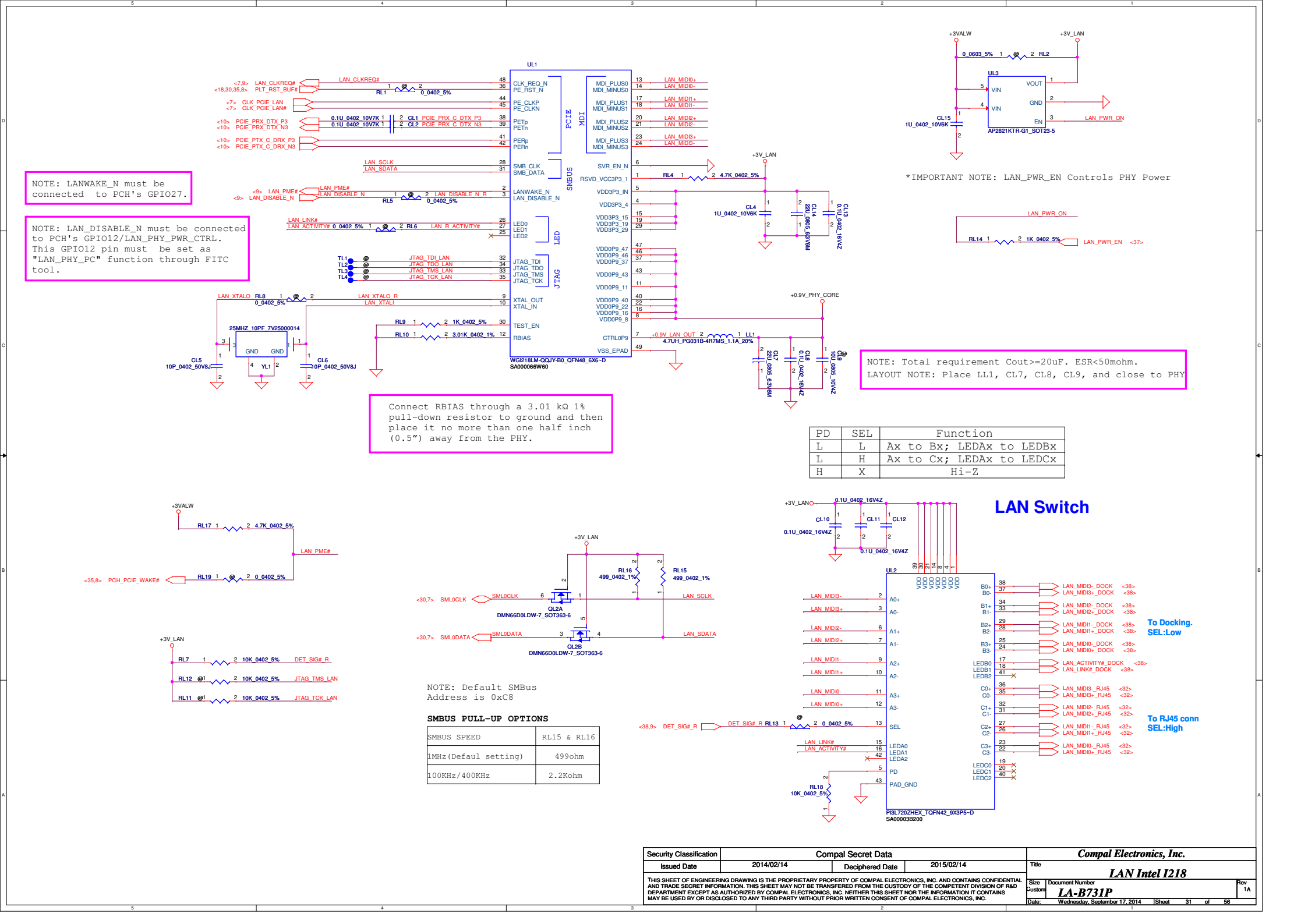
NOTE: LANWAKE_N must be connected to PCH's GPIO27.
NOTE: LAN_DISABLE_N must be connected to PCH's GPIO12/LAN_PHY_PWR_CTRL. This GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.
UL1
WGI218LM-QQJY-B0_QFN48_6X6-D
SA000066W60
Connect RBIAS through a 3.01 kΩ 1% pull-down resistor to ground and then place it no more than one half inch (0.5") away from the PHY.
*IMPORTANT NOTE: LAN_PWR_EN Controls PHY Power
AP2821KTR-G1_SOT23-5
NOTE: Total requirement Cout>=20uF. ESR<50mohm.
LAYOUT NOTE: Place LL1, CL7, CL8, CL9, and close to PHY
PD SEL Function
L L Ax to Bx; LEDAx to LEDBx
L H Ax to Cx; LEDAx to LEDCx
H X Hi-Z
LAN Switch
PI3L720ZHEX_TQFN42_9X3P5-D
SA00003B200
To Docking. SEL:Low
To RJ45 conn SEL:High
NOTE: Default SMBus Address is 0xC8
SMBUS PULL-UP OPTIONS
SMBUS SPEED RL15 & RL16
1MHz(Defaul setting) 499ohm
100KHz/400KHz 2.2Kohm
Security Classification Compal Secret Data
Issued Date 2014/02/14 Deciphered Date 2015/02/14
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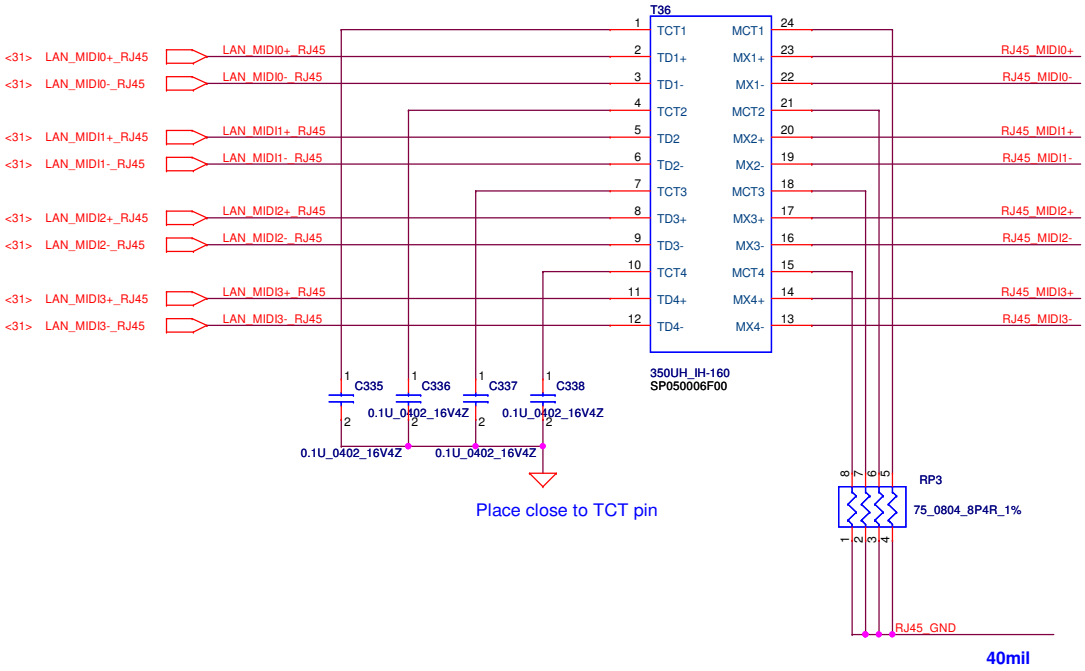
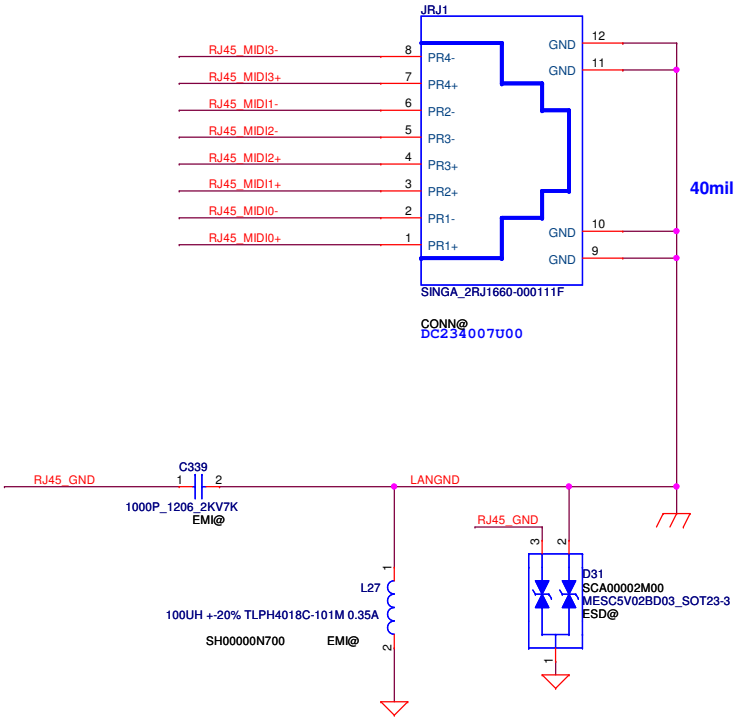
Compal Electronics, Inc.
Title LAN Intel I218
Size Custom Document Number LA-B731P Rev 1A
Date: Wednesday, September 17, 2014 Sheet 31 of 56

LAN Connector





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Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size	Document Number	Rev
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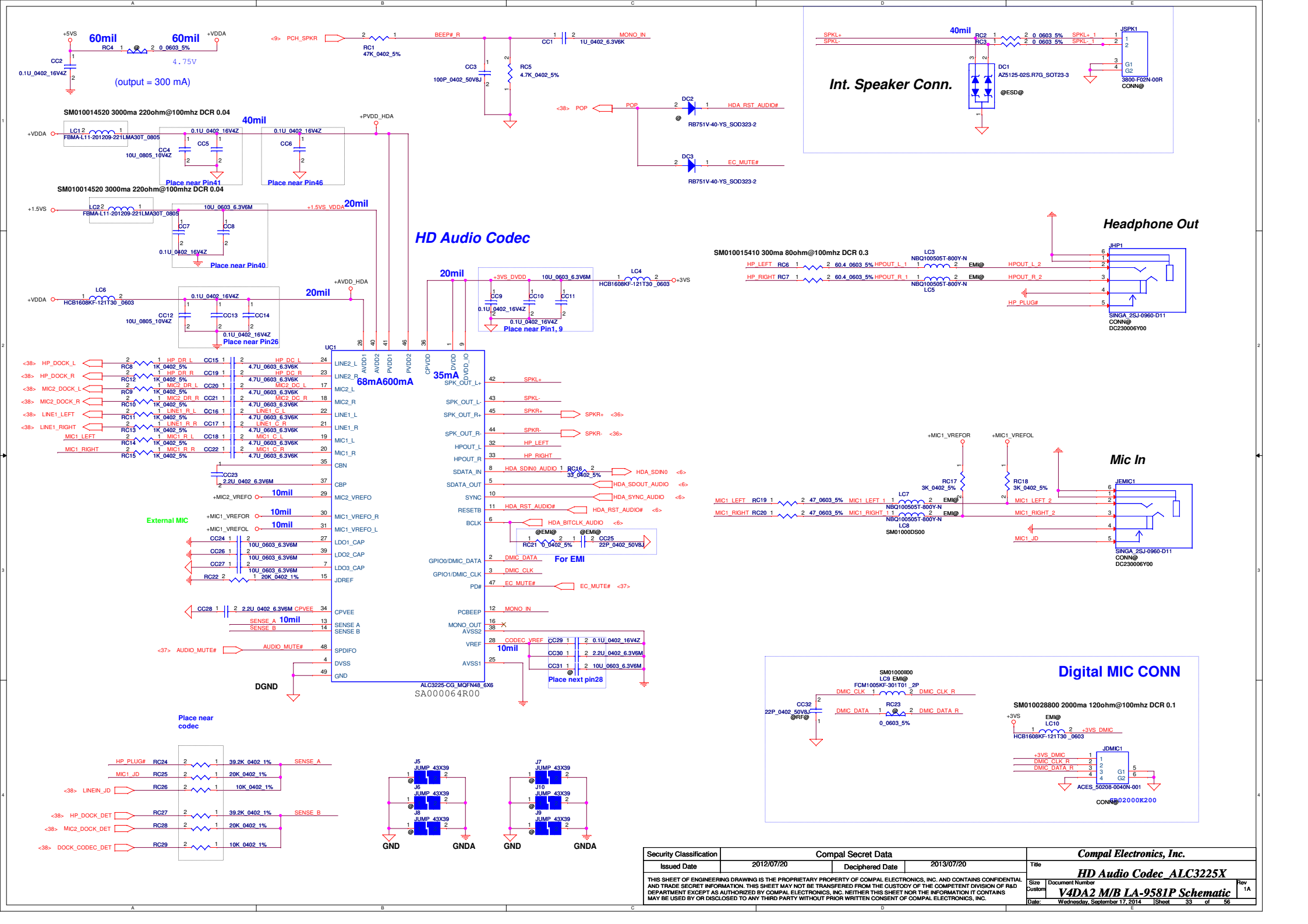
HD Audio Codec
Int. Speaker Conn.
Headphone Out
Mic In
Digital MIC CONN
UC1
ALC3225-CG_MQFN48_6X6
SA000064R00
68mA600mA
35mA
External MIC
For EMI
DGND
GND
GNDA
Place near codec
Place near Pin41
Place near Pin46
Place near Pin40
Place near Pin26
Place near Pin1, 9
Place next pin28
SM010014520 3000ma 220ohm@100mhz DCR 0.04
SM010015410 300ma 80ohm@100mhz DCR 0.3
SM010028800 2000ma 120ohm@100mhz DCR 0.1
(output = 300 mA)
4.75V
Compal Secret Data
2012/07/20
2013/07/20
Compal Electronics, Inc.
HD Audio Codec_ALC3225X
V4DA2 M/B LA-9581P Schematic
Wednesday, September 17, 2014
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Compal Electronics, Inc.

Title: ***SPACE***

Size	Document Number	Rev
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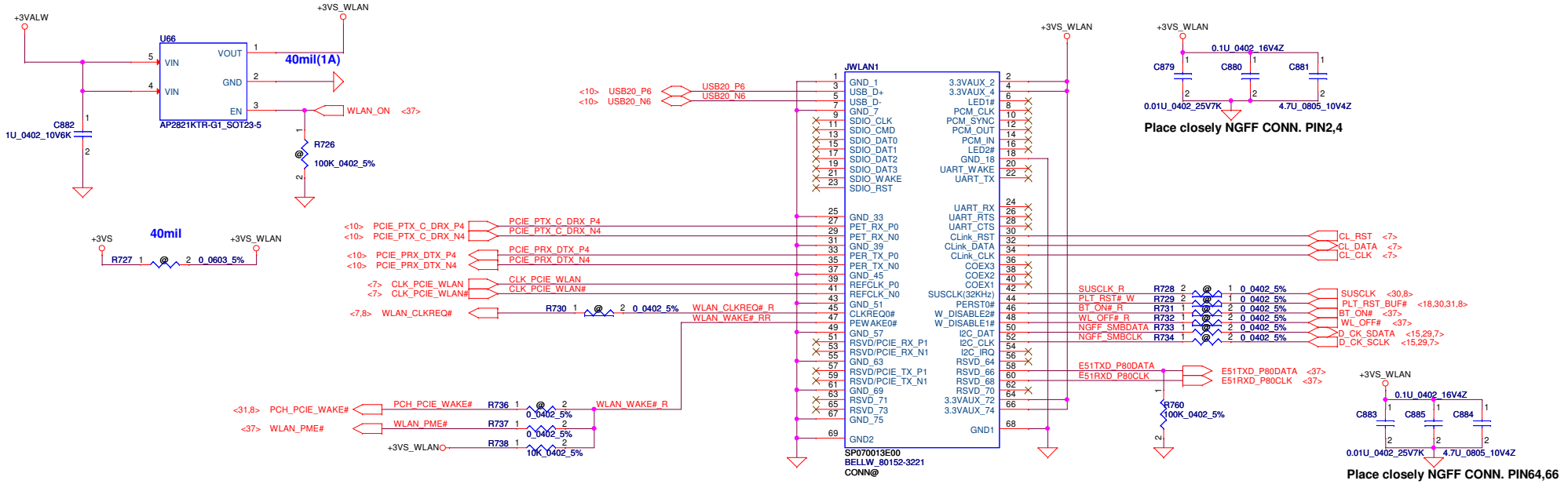
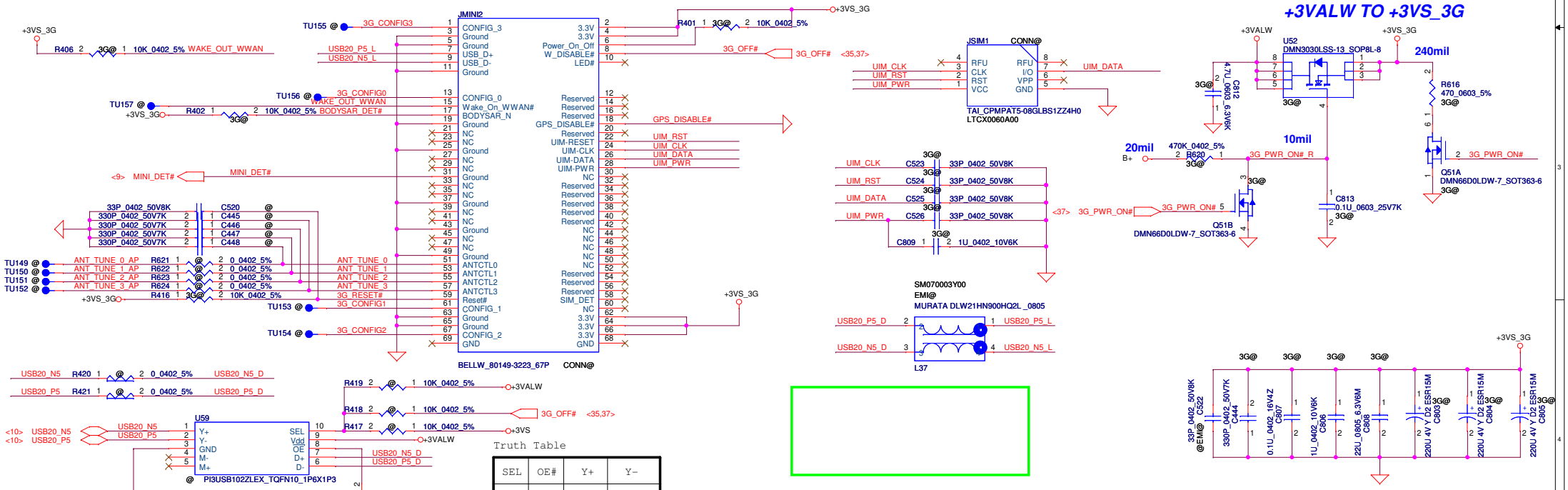
NGFF(Wireless LAN & BT)



+3VALW TO +3VS_3G



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Compal Electronics, Inc.	
Title	mini Card & 3G/SSD CONN.
Size: Custom	Document Number: LA-B731P
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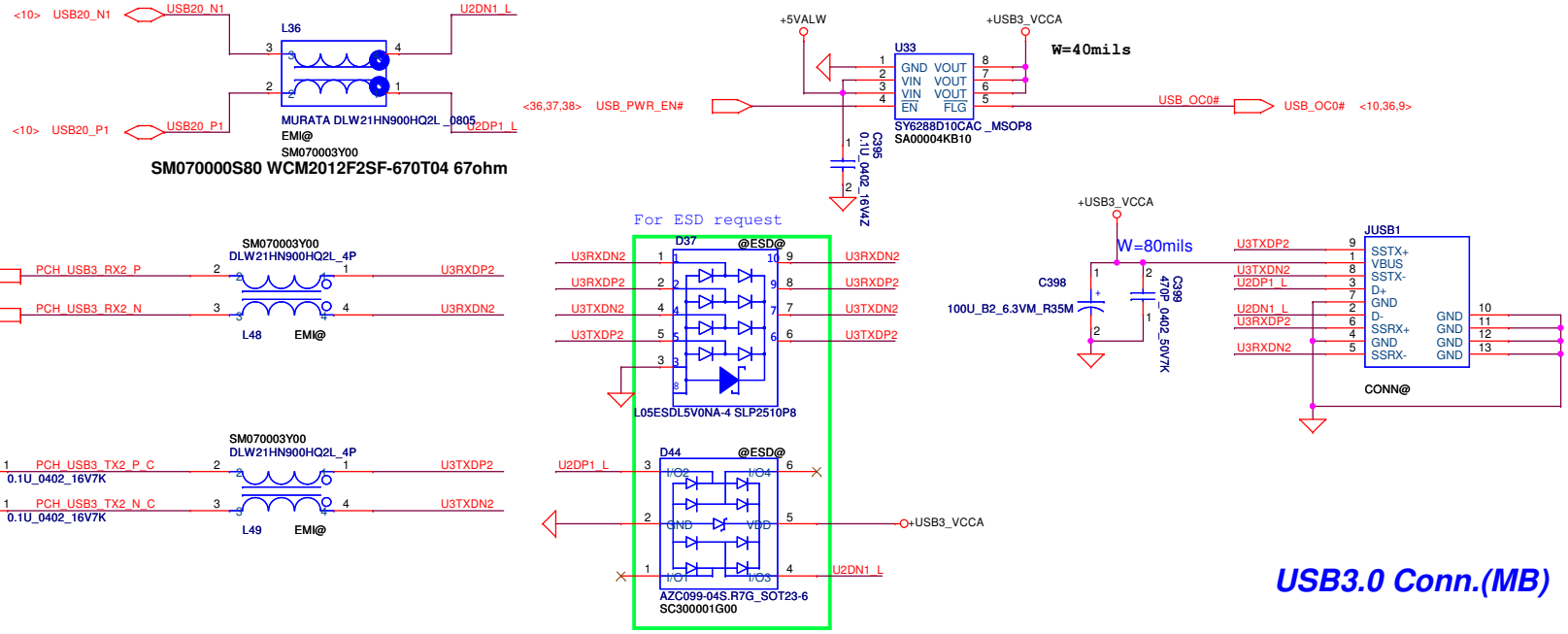

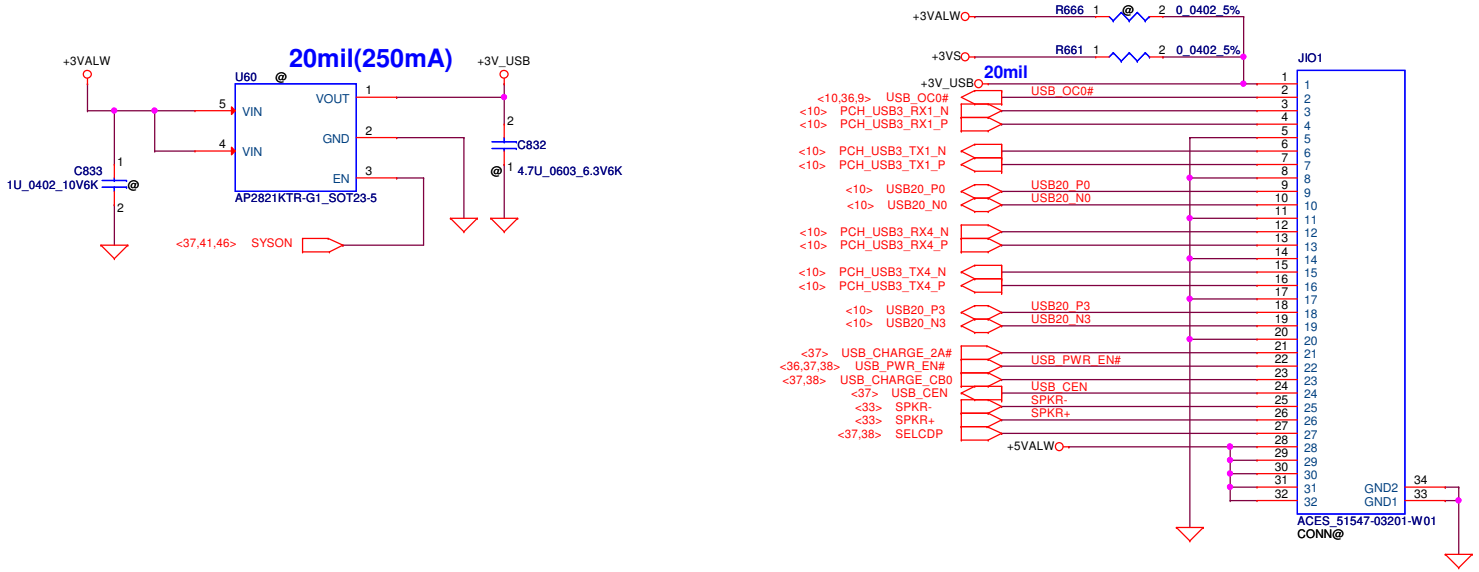

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Compal Electronics, Inc.

Title: USB3.0 & SSD

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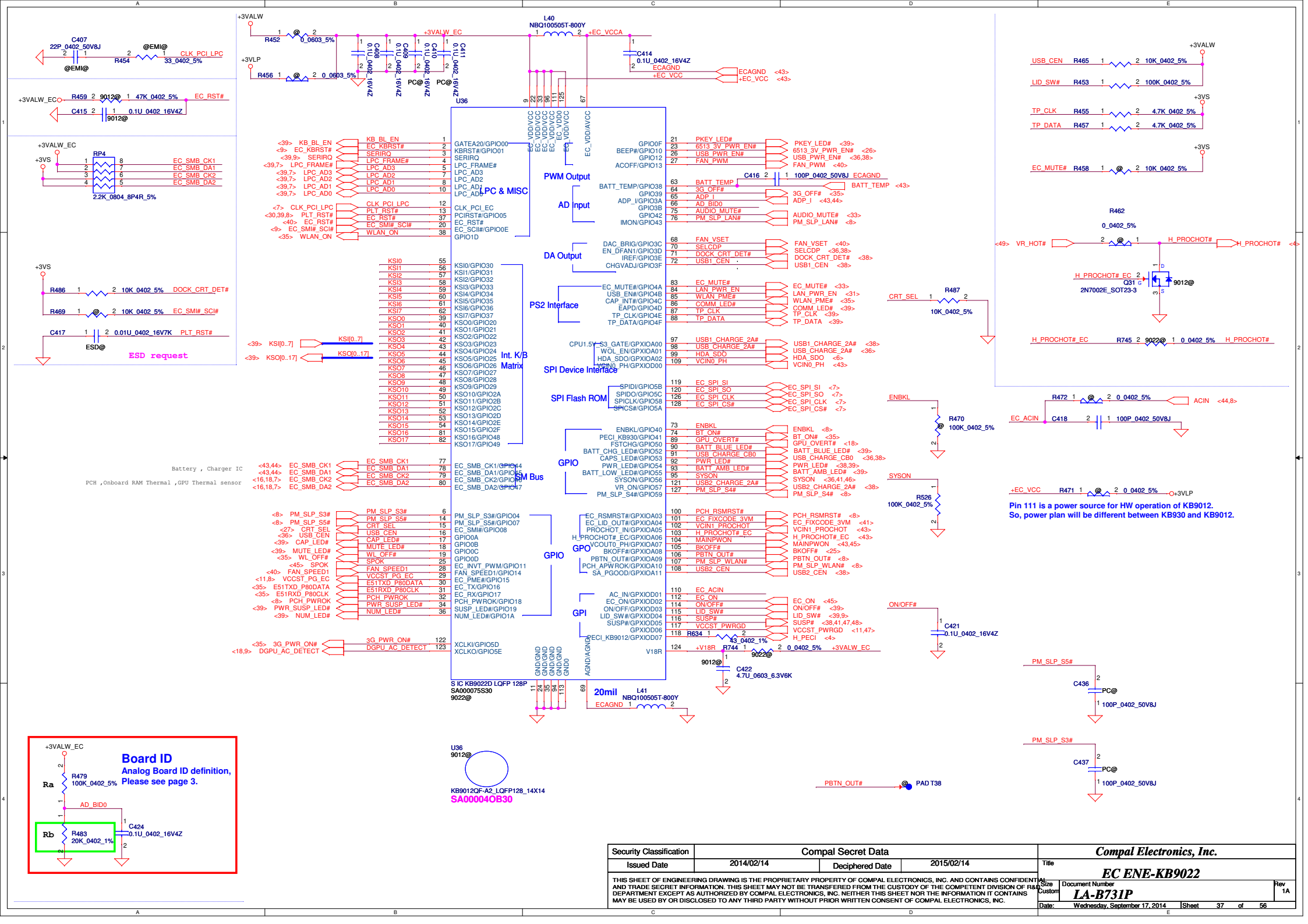

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Compal Electronics, Inc.	
Title	EC ENE-KB9022
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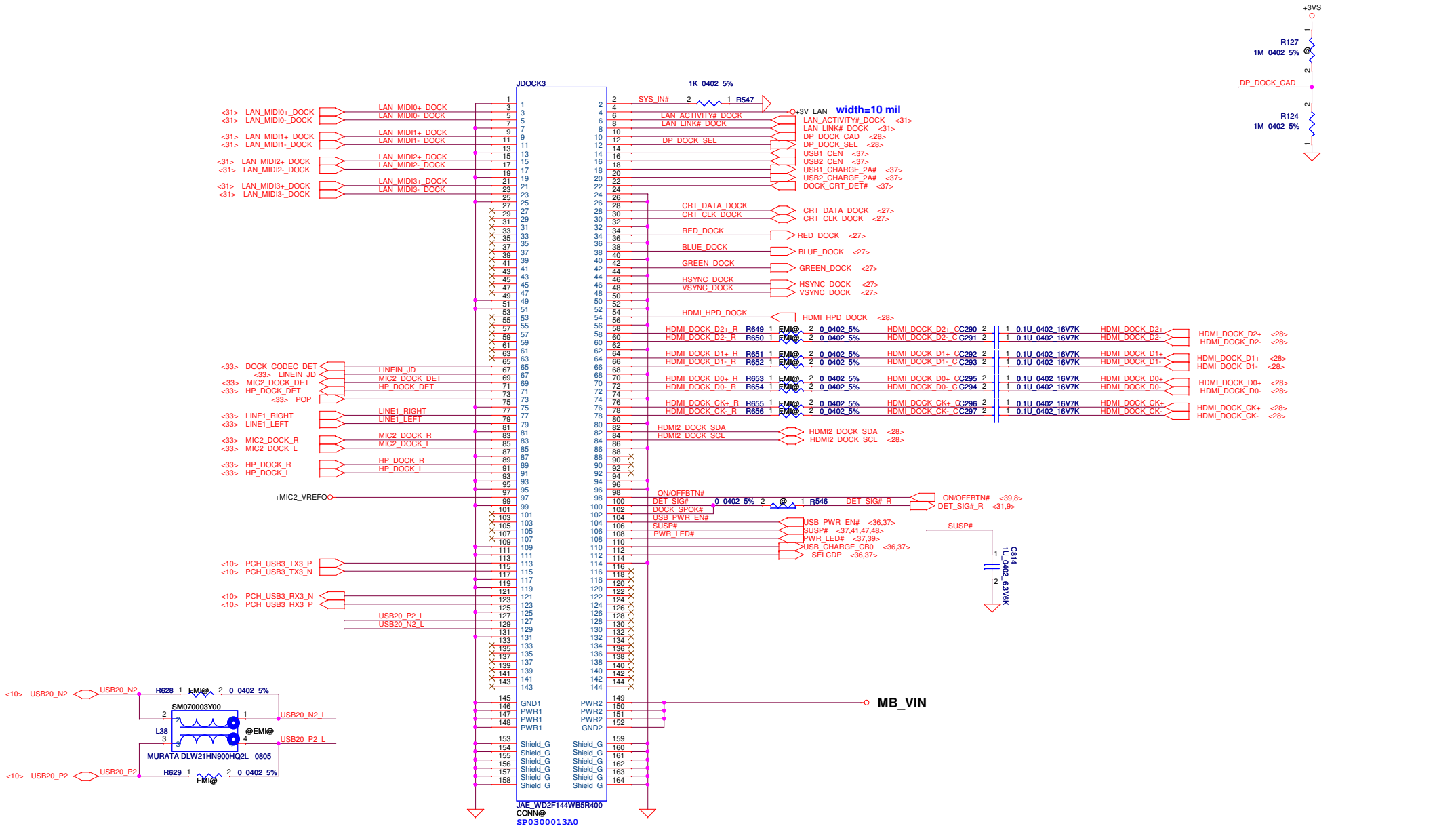

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Size: Custom	Document Number: LA-B731P		Rev: 1A
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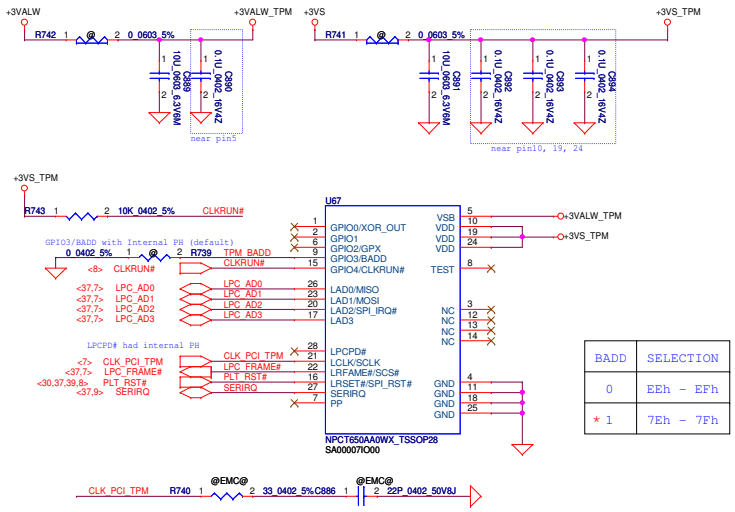
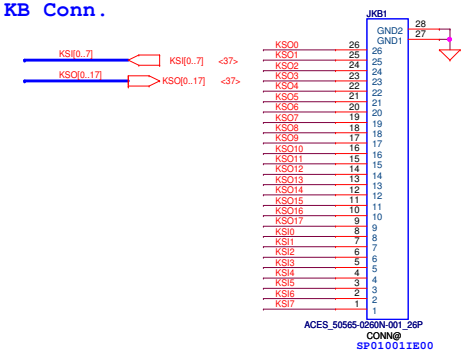
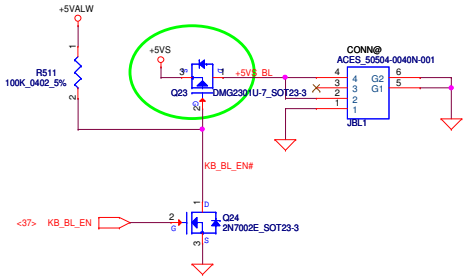
TPM



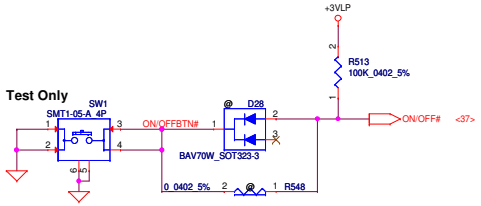
KB Conn.



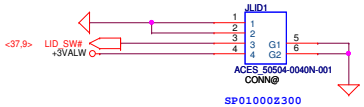
KB Backlight Conn



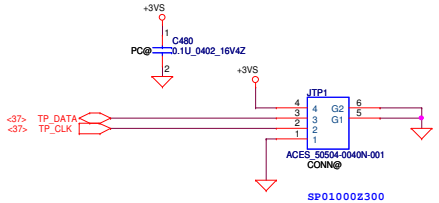
ON/OFF BTN



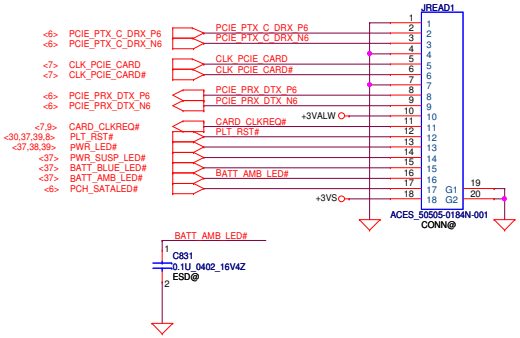
Lid Switch/B
(Hall Effect Switch)



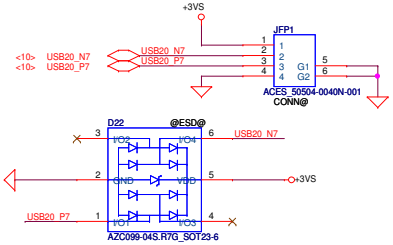
TP Conn.



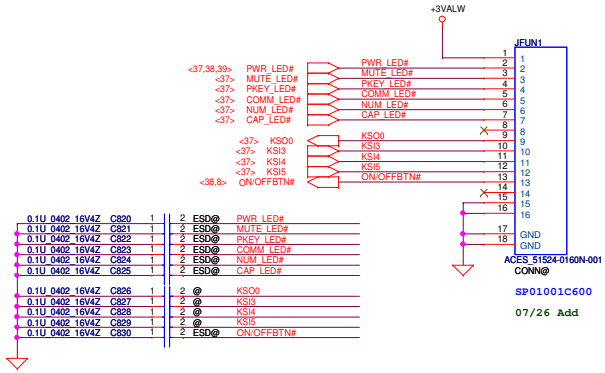
CardReader Board



FP Board



Function Board



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Compal Electronics, Inc.			
Title	KB/TP/LID/TPM/FUN/FP/CARD		
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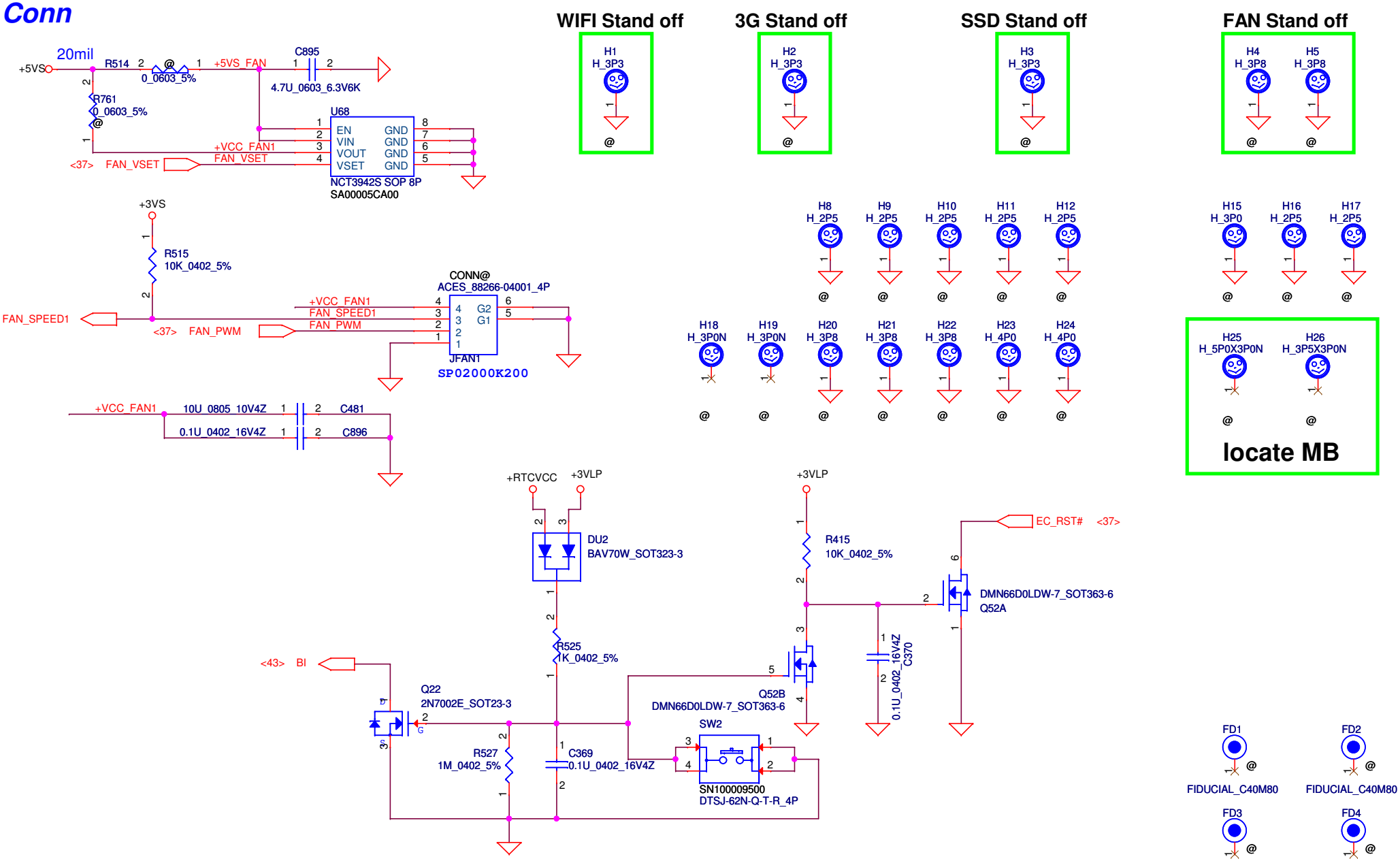
FAN Conn



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Issued Date	2014/02/14	Deciphered Date	2015/02/14

Compal Electronics, Inc.			
Title: FAN & Screw			
Size: Custom	Document Number: LA-B731P		Rev: 1A
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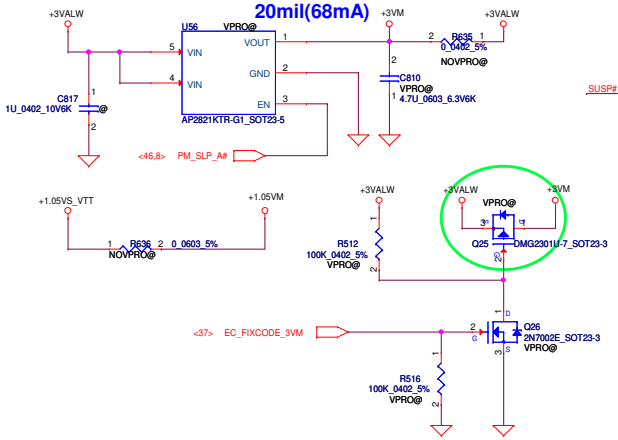
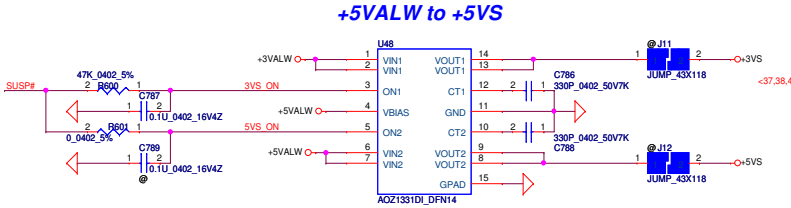
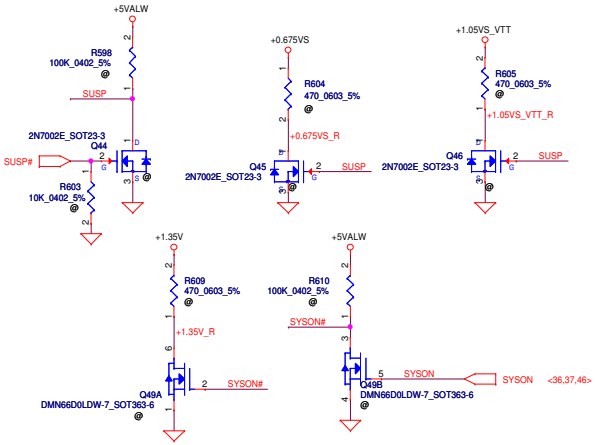
+3VALW to +3VM for Intel AMT

20mil(68mA)

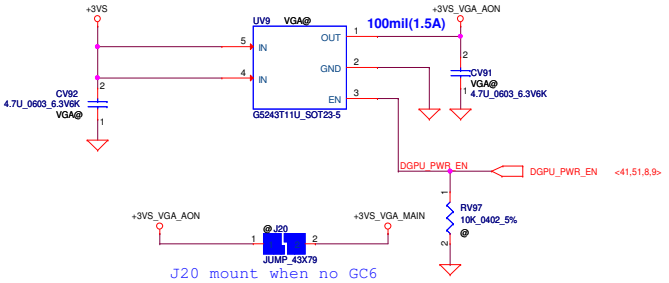


+3VALW to +3VS
+5VALW to +5VS

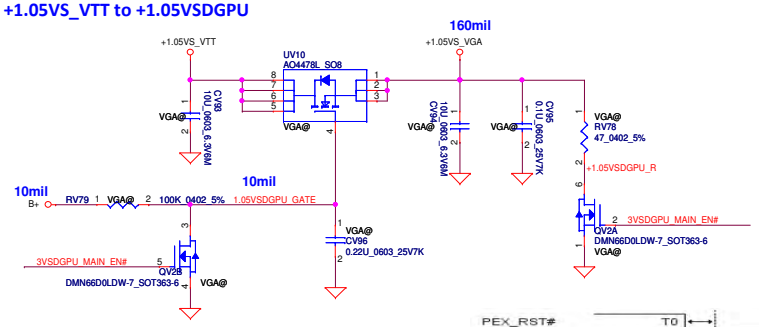




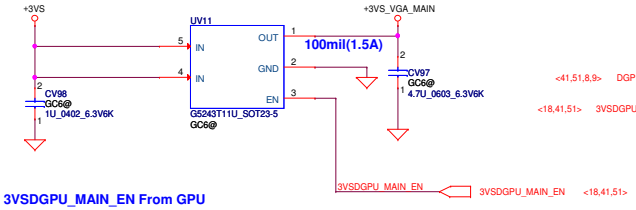
+3VS to +3VSDGPU_AON for GPU

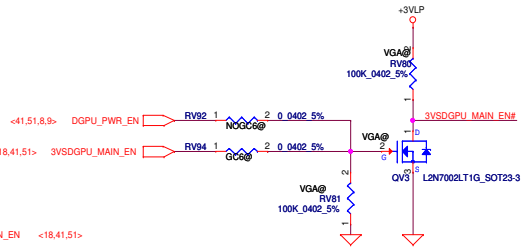


+1.05VS_VTT to +1.05VSDGPU



+3VS to +3VSDGPU_MAIN for GC6-2.0





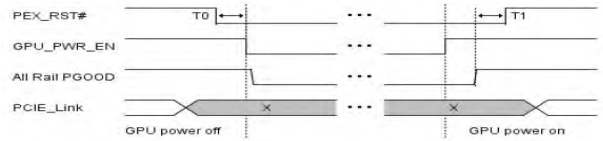
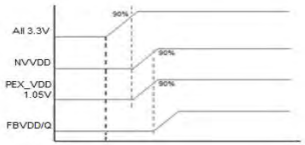


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

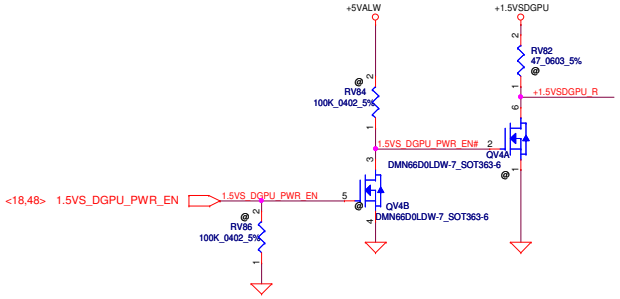
Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

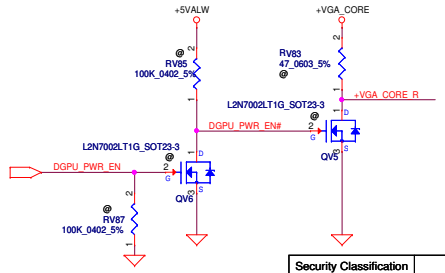


Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
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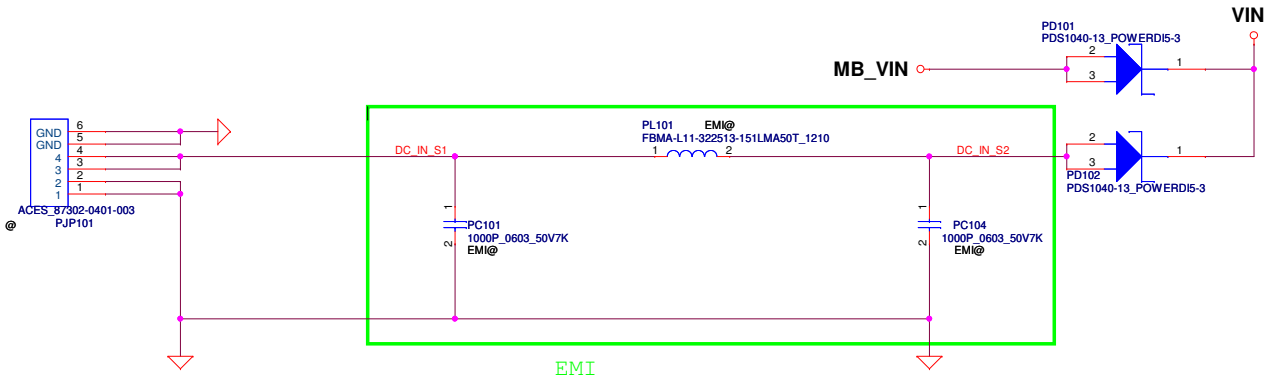
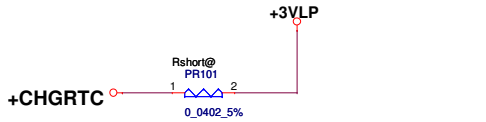
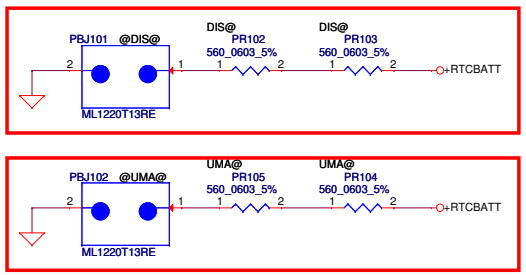


BOM Config

DDR3L	UMA	EMI@
	DIS	EMI@/VGA@/VGAEMI@





2014/9/17

DIS: RTC at FAN

UMA: RTC at Docking

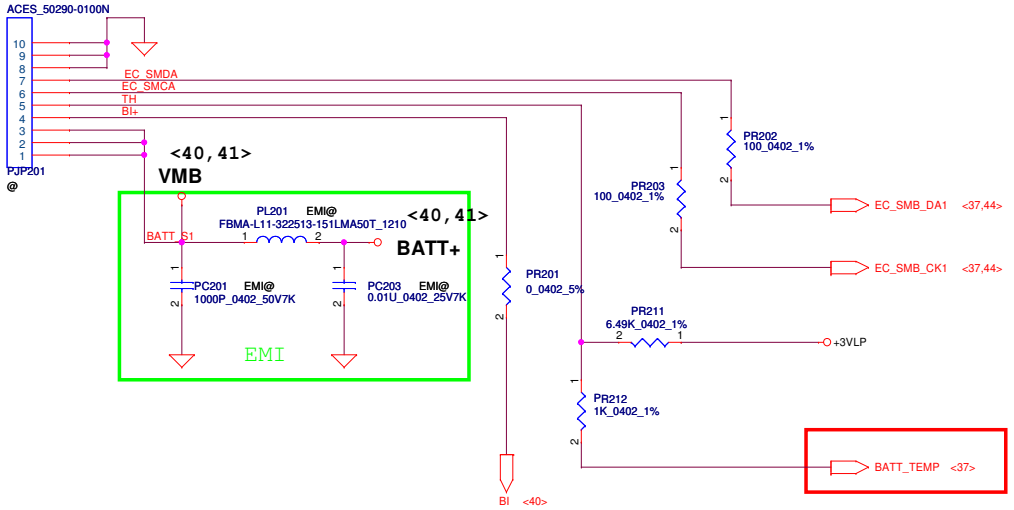
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

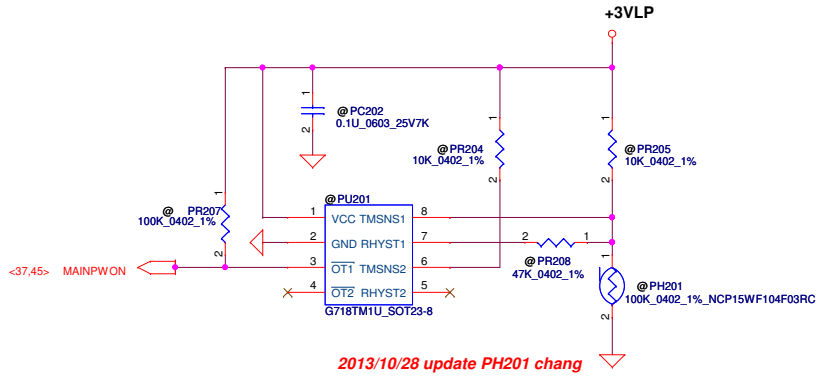
Compal Electronics, Inc.

Title: **DCIN**

Size: Custom | Document Number: *V4DA2 LAA131P Schematic* | Rev: 0.1

Date: Wednesday, September 17, 2014 | Sheet 42 of 55





2013/10/28 update PH201 chang
Common part SL200002H00

2013/10/14 update

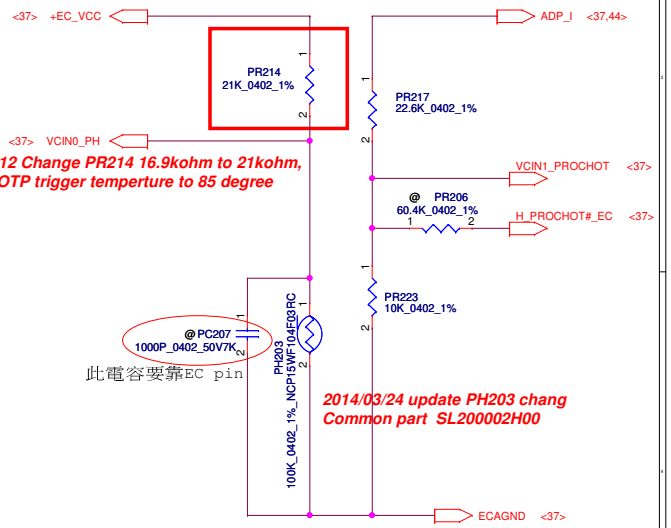
For KB9022 sense 20mΩ	Active	Recovery
40W PR202 10K ohm	52W,0.54V	40W,0.42V
65W PR202 22.6K ohm	84.5W,0.54V	65W,0.42V

For 65W adapter===>action 84.5W, recovery 65W
65W:
Iada=0~3.42A (65W/19v=3.42A)
ADP_I=20*Iada*Rsense
=20*3.42*0.02=1.368V
VCIN1_PROCHOT=1.368*10/(10+22.6)=0.42V

84.5W:
Iada=0~4.447A (84.5W/19v=4.447A)
ADP_I=20*Iada*Rsense
=20*4.447*0.02=1.788V
VCIN1_PROCHOT=1.788*10/(10+22.6)=0.55V

CPU thermal protection at 92 degree C
PH203 under CPU botten side :
(92 degree = 7.3K ohm) => VCIN0_PH = 1V
(56 degree = 26.11k ohm) => VCIN0_PH = 2V

3.3*7.3/(7.3+16.9)=1
3.3*26.11/(26.11+16.9)=2



2014/09/12 Change PR214 16.9kohm to 21kohm, change OTP trigger temperture to 85 degree

2014/03/24 update PH203 chang
Common part SL200002H00

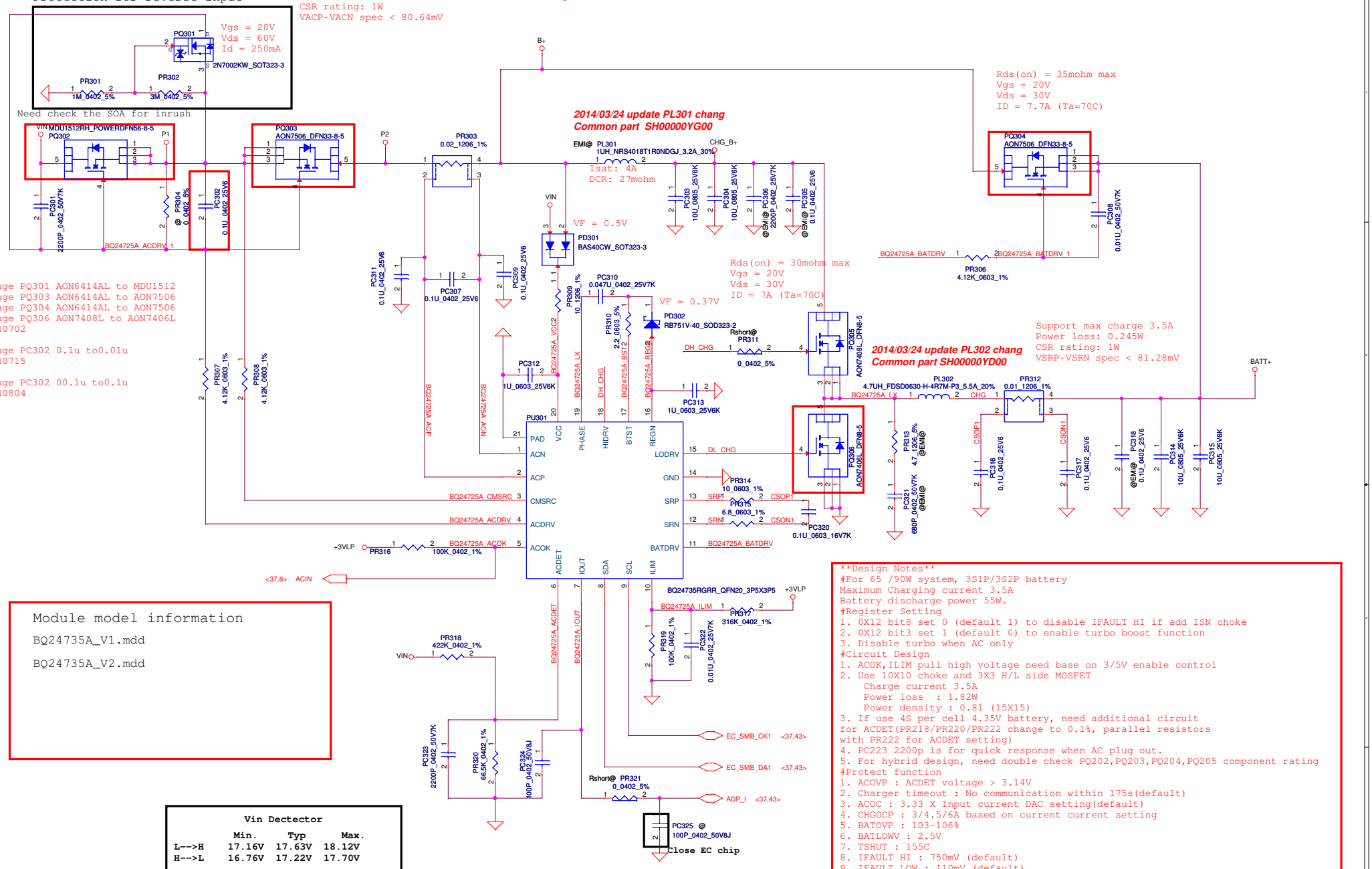
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	*V4DA2 LAA131P Schematic*	0.1

Date: Wednesday, September 17, 2014 | Sheet 43 of 55



Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

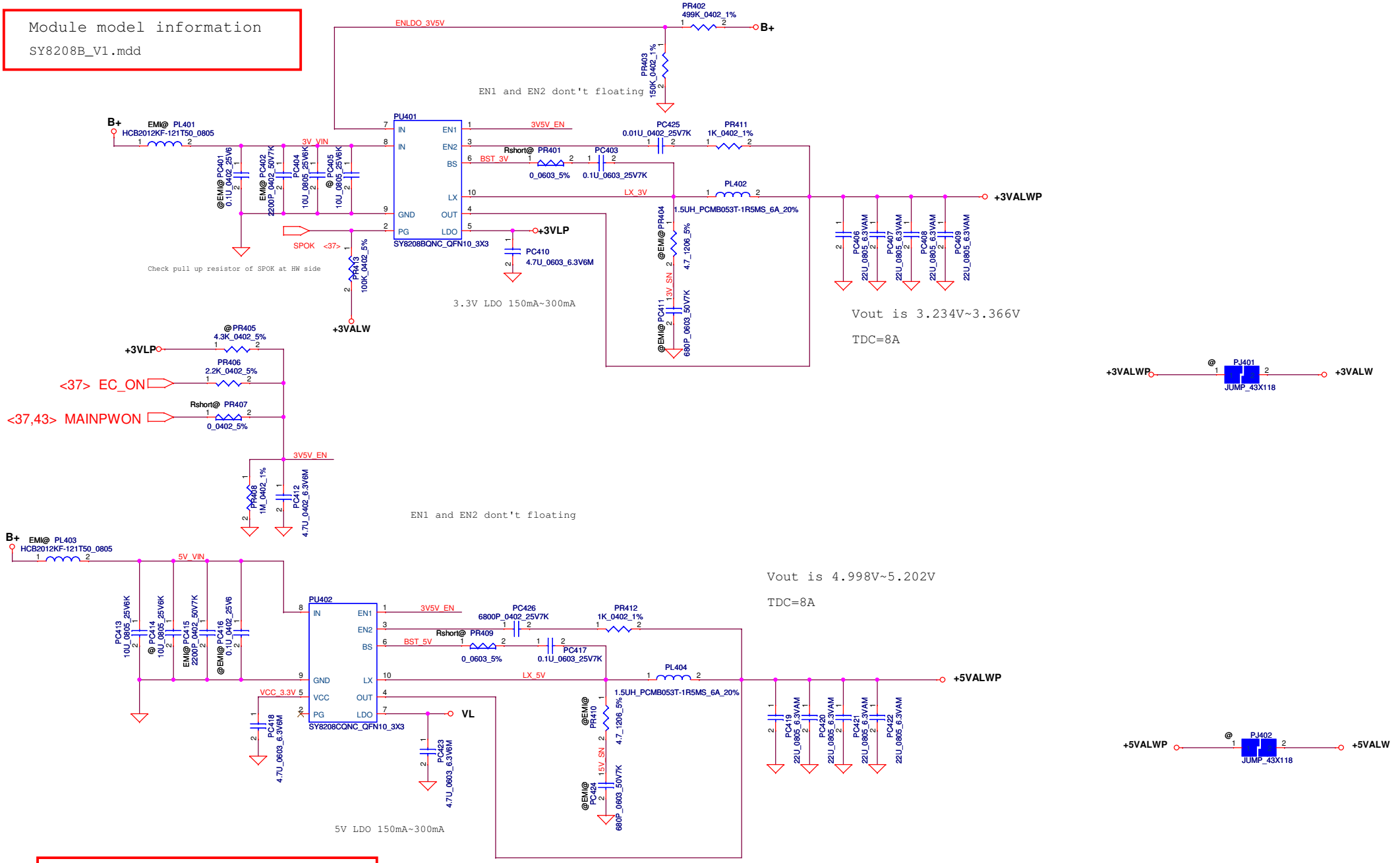
Title: **CHARGER**

Size: Custom | Document Number: Z4DBH M/B LA-B731P Schematic | Rev: 0.1

Date: Wednesday, September 17, 2014 | Sheet 44 of 55

Module model information

SY8208B_V1.mdd



Module model information

SY8208C_V1.mdd

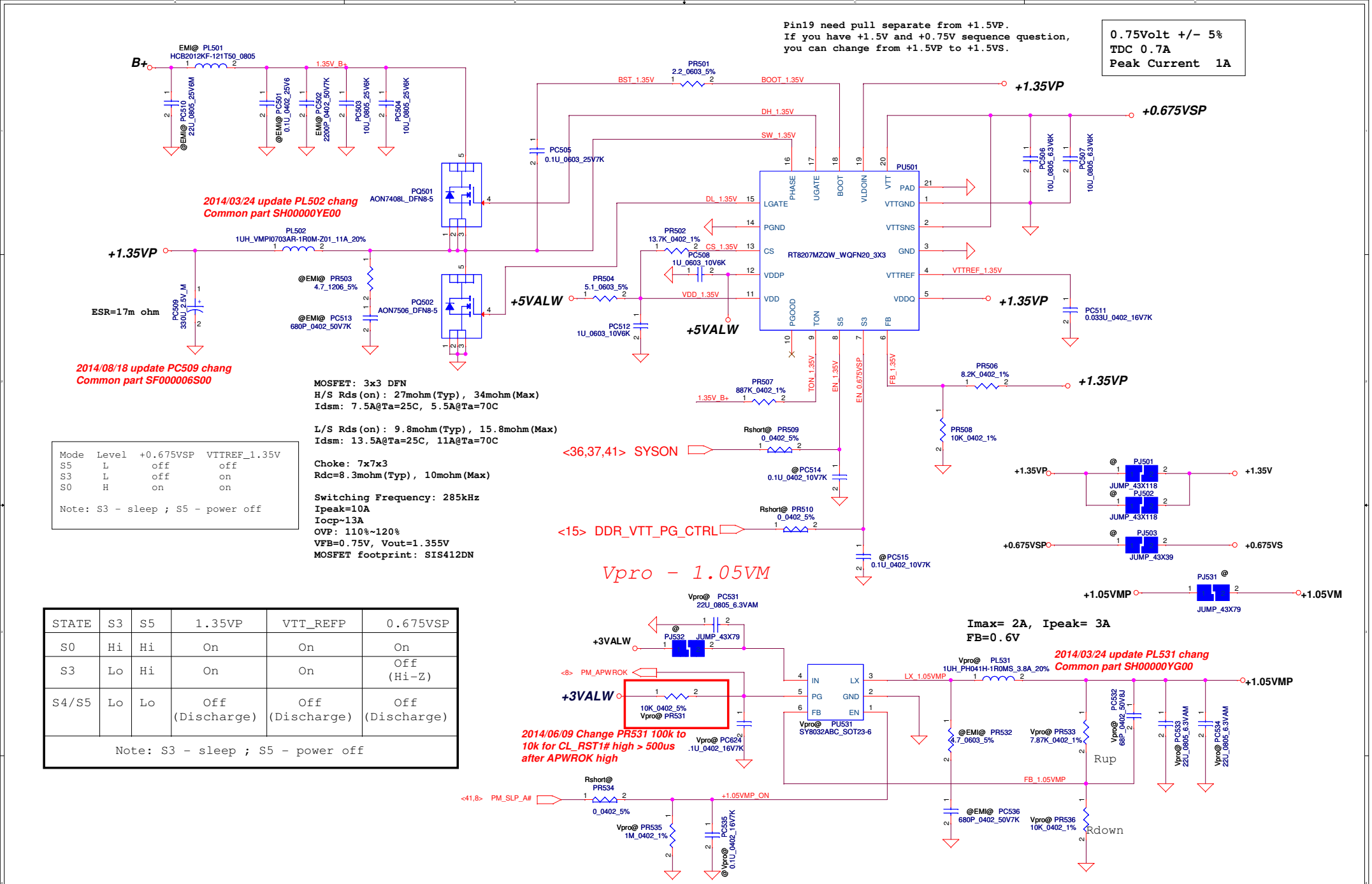
Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 0.1

Date: Wednesday, September 17, 2014 | Sheet 45 of 55



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

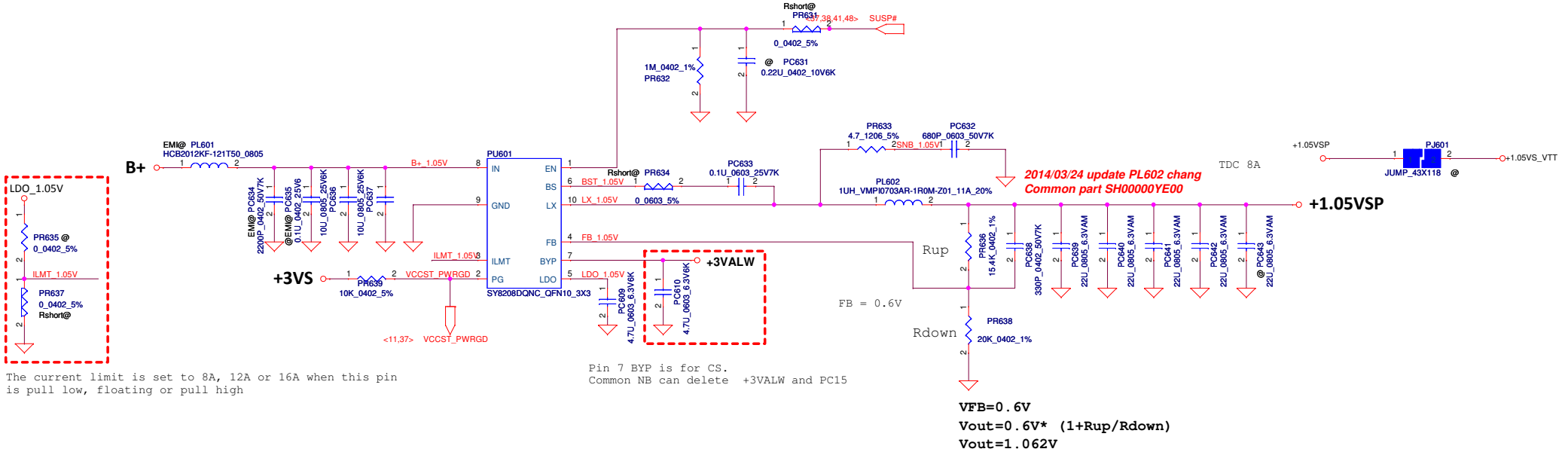
Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Title: 1.35VP/0.675VSP/1.05VMP

Size	Document Number	Rev
Custom	V4DA2 LAA131P Schematic	0.1

Date: Wednesday, September 17, 2014 Sheet 46 of 55



Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: 1.05VSP

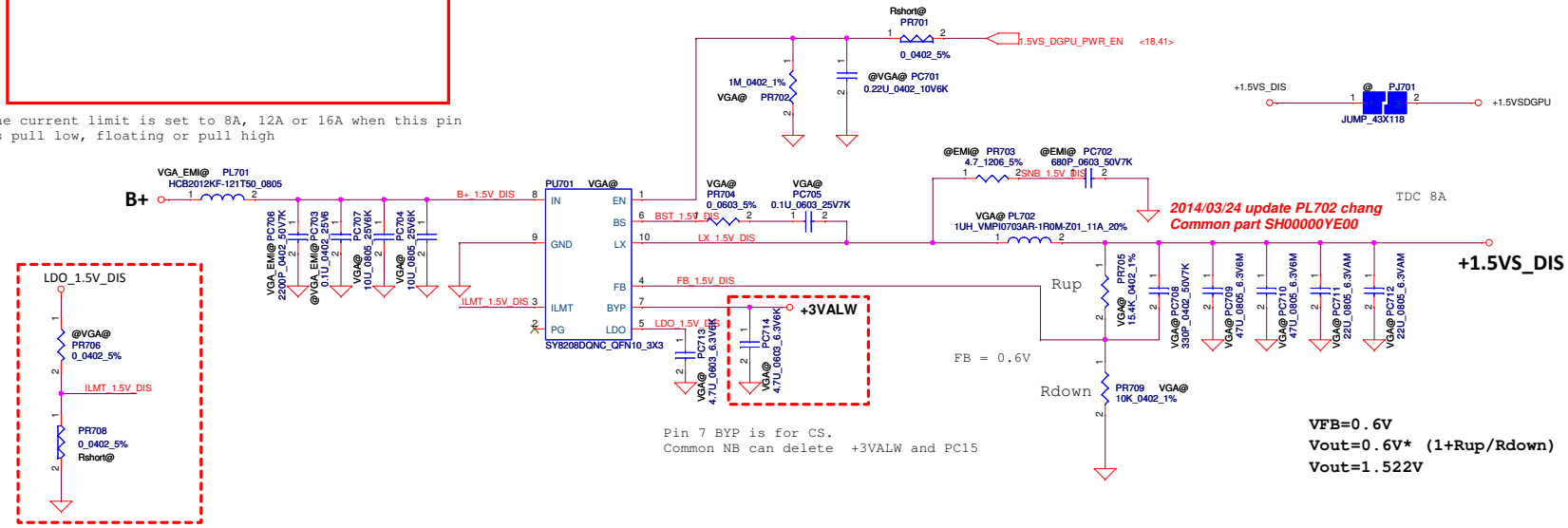
Size: Custom | Document Number: V4DA2 LAA131P Schematic | Rev: 0.1

Date: Wednesday, September 17, 2014 | Sheet 47 of 55

Module model information

TPS51212_V1.mdd for Single layer
TPS51212_V2.mdd for Dual layer

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.522V

+1.2V

Switching Frequency: 290kHz
Imax=8A
OCP~10.5A
OVP: 120%~130%
VFB=0.704V, Vout=1.207V

+1.05V

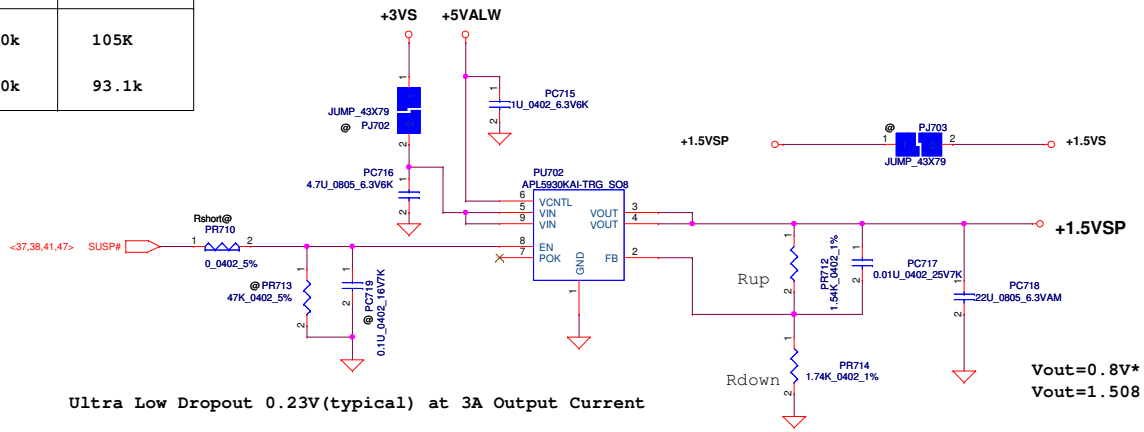
Switching Frequency: 290kHz
Imax=5.4A
Ipeak=6.5A
Iocp=7.8A
OVP: 120%~130%
VFB=0.704V, Vout=1.055V

Vout	PR1007	PR1008	PR1003
+1.5V	11.5k	10k	
+1.35V	9.31k	10k	
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
L/S Rds(on): 22mohm(Typ), 13.5mohm(Max)

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Switching Frequency: 290kHz
Ipeak=10A
Delta I =2.16A
Iocp=12.14~16.67A
OVP: 120%~130%
VFB=0.704V, Vout=1.51V



Vout=0.8V* (1+Rup/Rdown)
Vout=1.508

Ultra Low Dropout 0.23V(typical) at 3A Output Current

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/06/19	Deciphered Date	2012/07/31
Title	1.5VSDGPUP/1.5VS		
Size	Document Number		Rev
	Z4DBH M/B LA-B731P Schematic		0.1
Date:	Wednesday, September 17, 2014	Sheet	48 of 55

Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73			
Location	15W TDC 14A MAX 32A OCP 38.4A Loadline=-2.0mv/A	28W TDC 19A MAX 40A OCP 48A Loadline=-2.0mv/A	Note
PR850	392 Ohm	499Ohm	OCP
PR839	1.27kOhm	1.58kOhm	Droop
PC828	0.033uF	0.022uF	RC Match
PR845	90.9kOhm	113kOhm	PROG1
PC834	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

-->20130828
Choke: 0.15UH (Size:7*7*4)
SH00000U300
Rdc=0.66mohm +-7%
Heat Rating Current=36A
Saturation Current=45A

+1.05VS_VTT
Follow intel guideline
PR843 130_0402_1%
PC840 1U_0402_6.3V6K
PR848 54.9_0402_1%

Note:
VR_SVID_ALRT# Pull high on HW side

<11> VR_SVID_DATA
<11> VR_ALERT#
<11> VR_SVID_CLK
<11> VR_ON
PR832 1.91K_0402_1%
<11,8> VGATE
PC833 1000P_0402_50V7K
PR854 102K_0402_1%
<37> VR_HOT#
PR804 470K_0402_5%_ TSM0B474J4702RE
PR836 27.4K_0402_1%
PR834 3.83K_0402_1%
PC838 47P_0402_50V8J

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

2013/10/28 update PH804 chang
Common part SL200002E00

Update for cpu transient, 20140416
PR833, 1.91k ohm to 3.65k ohm
PR835, 4.99M ohm to 10M ohm
PR850, 392 ohm to 475 ohm
PR852, 2.61k ohm to 10k ohm
PR854, 121k ohm to 102k ohm
PC828, 0.033u F to 0.022u F

PU803
ISL95813HRZ-T_QFN20_3X4
PAD, SCLK, ALERT#, SDA, PRGM1
VR_ON, PGOOD, IMON, VR_HOT#, NTC, COMP, FB, RTN, ISUMN, ISUMP
LGATE, PHASE, UGATE, BOOT, VCC, PRGM2

15W@ PR845 90.9K_0402_1%
28W@ PR845 113K_0402_1%
Note:
PR845=113K
=>Icc(max)=40A
fsw=700KHz

PR844 0_0603_5%
PQ801 AON7518_DFN8-5
PR849 2.2_0603_5%
PC832 0.22U_0603_16V7K
+5VS
PC834 0.1U_0402_25V6
PQ803 AON6554_DFN5X6-8-5
28W@ PQ802 AON6554_DFN5X6-8-5
PR840 124K_0402_1%

Note:
PR812=124K
=>Slew rate=53mV/us
Vboot = 1.7V

PC824 10U_0805_25V6K
PC820 10U_0805_25V6K
@EMI@ PC818 0.01U_0402_50V7K
@EMI@ PC825 2200P_0402_50V7K
PC806 33U_25V_M
PC807 33U_25V_M
CPU_B+
EMI@ PL803 HCB2012KF-121T50_0805
B+
Height 8 mm
100u_SF000000I80
Height 6 mm
68u_SF000000W00

2014/01/21 update PL804 change
Common part SH000011H00
PL804
+CPU_CORE
0.22UH 20% FDUE0640J -H 25A
@EMI@ PR842 4.7_1206_5%
@EMI@ PC829 680P_0603_50V7K
PR838 3.65K_0603_1%

PR833 3.65K_0402_1%
33P_0402_50V8J PC837
PC823 6800P_0402_25V7K
PR851 2K_0402_1%
@ PR841 10_0402_1%
@PC822 330P_0402_50V7K
@PC830 390P_0402_50V7K
15W@ PR839 1.27K_0402_1%
Droop
28W@ PR839 1.58K_0402_1%

PR835 10M_0402_5%
RC Match
15W@ PC828 0.022U_0402_16V7K
28W@ PC828 0.022U_0402_16V7K
PC827 0.1U_0402_16V4Z
PR853 11K_0402_1%
PR852 10K_0402_1%
PH803 10KB_0402_5%_ERTJ0ER103J
2013/10/28 update PH803 chang
Common part SL200002G00

28W@ PR850 499_0402_1%
OCP Setting
15W: 38A
28W: 48A
15W@ PR850 475_0402_1%
@PC821 4700P_0402_25V7K
@PR847 1.5K_0402_1%

<11> VCC_SENSE
@PC839 330P_0402_50V7K
PC836 0.01U_0402_50V7K
@PC826 0.082U_0402_16V7K
<11> VSS_SENSE

Local sense put on HW site

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Title	CPU_CORE		
Size: Custom	Document Number		Rev: 0.1
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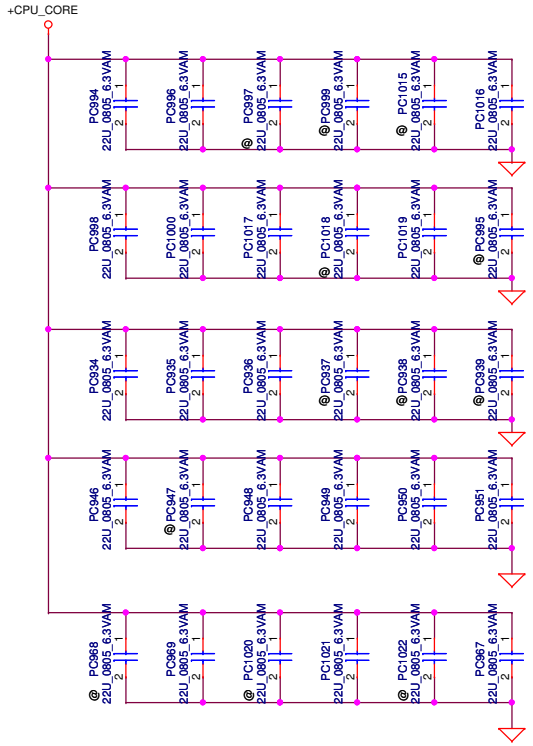

CPU LL=2m ohm dedign 22uF *18, 22uF*12(un-pop)

Compal Electronics, Inc.

Title: CPU_CORE_CAP

Size	Document Number	Rev
Custom	V4DA2 LAA131P Schematic	0.1

Date: Wednesday, September 17, 2014 | Sheet 50 of 55

Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR1206	20K	39K	27K
Rref1	PR1208	20K	30K	7.5K
Rboot	PR1233	2K	3K	0
Rref2=PR1209 +PR1212	PR1209	18K	24K	6.2K
	PR1212	0	3K	1.74K
C	PC1210	2.7nf	1.8nf	5.6nf
		N15S-GT	N15V-GL	N15V-GM

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(19-0.9)*0.9/
(304.89Khz*0.36u*19)=7.811A

OCP=54A/2=27A per phase
Ivalley=27A-7.811A/2=23.1A

H-side MOS:AON6552
Rds(on):
5.6mohm@Vgs=10V
6.7mohm@Vgs=4.5V
Id :20A@Ta=25 degC

L-side MOS:AON6554
Rds(on):
3.2mohm@Vgs=10V
3~3.8mohm@Vgs=4.5V
Id :85A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
Rdc=0.97mohm +-5%
Heat Rating Current=34A
Saturation Current=25A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

PSI Pull high on HW side

Pull high on HW side

Reserve Location
For NV power sequence change
PR1227 and PC1222 20140401

+VGA_CORE
EDP-Continuous 31A
EDP-Peak 60A
OCP min 72A

2013/12/13 update PL1202 PL1203 change to Common part SH000011H00

1. VSNS Soft-Start time (Internal) is 0.7ms (PC1213 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms (PC1213 pop)

2. Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=304.89Khz

3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PR23=VTSNS/Rth

	T_min	T_typical	T_max
PR1221=18.7K	96.73C	100C	103.1C
PR1221=13K	106.38C	110C	113.4C

2013/10/28 update PH1201 chang Common part SL200002E00

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: VGA_CORE

Size: C | Document Number | Rev: 0.1

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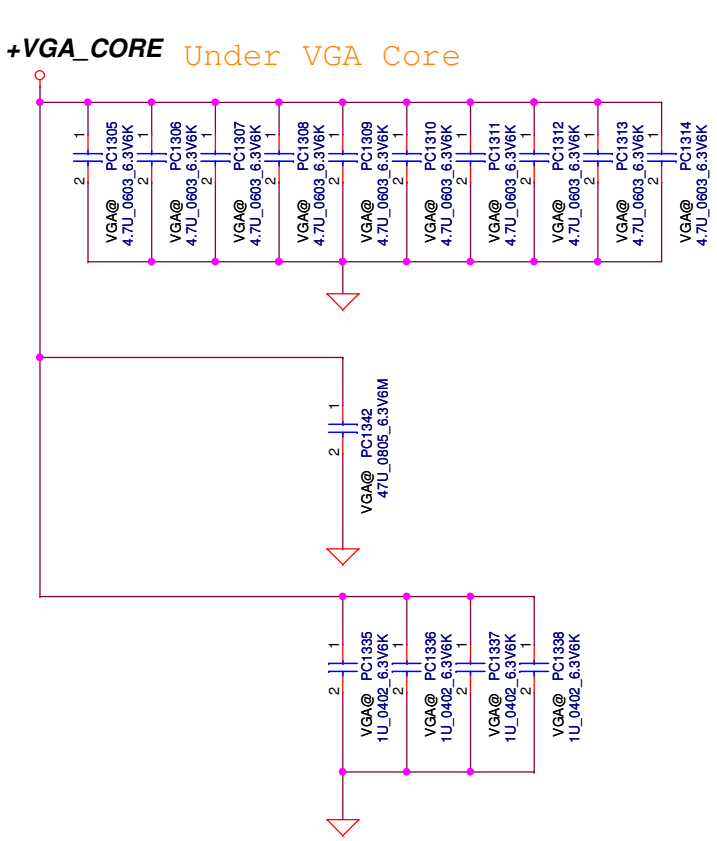
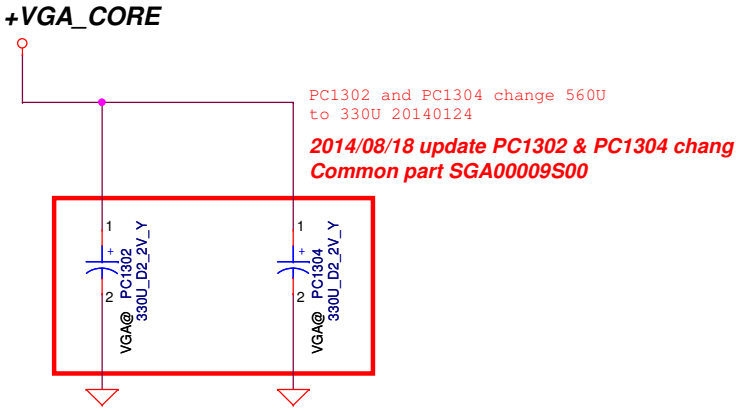
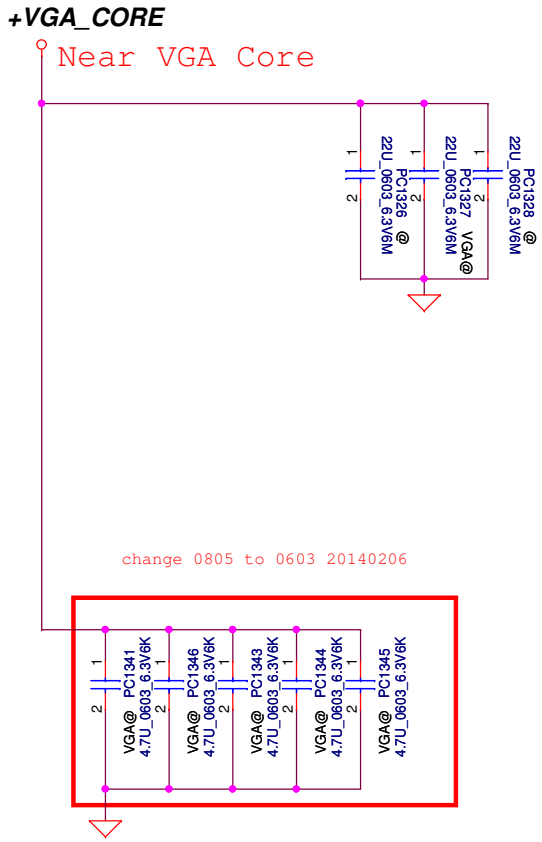
Z4DBH M/B LA-B731P Schematic







N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/07
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: VGA_CORE CAP

Size: Custom | Document Number: Z4DBH M/B LA-B731P Schematic | Rev: 0.1

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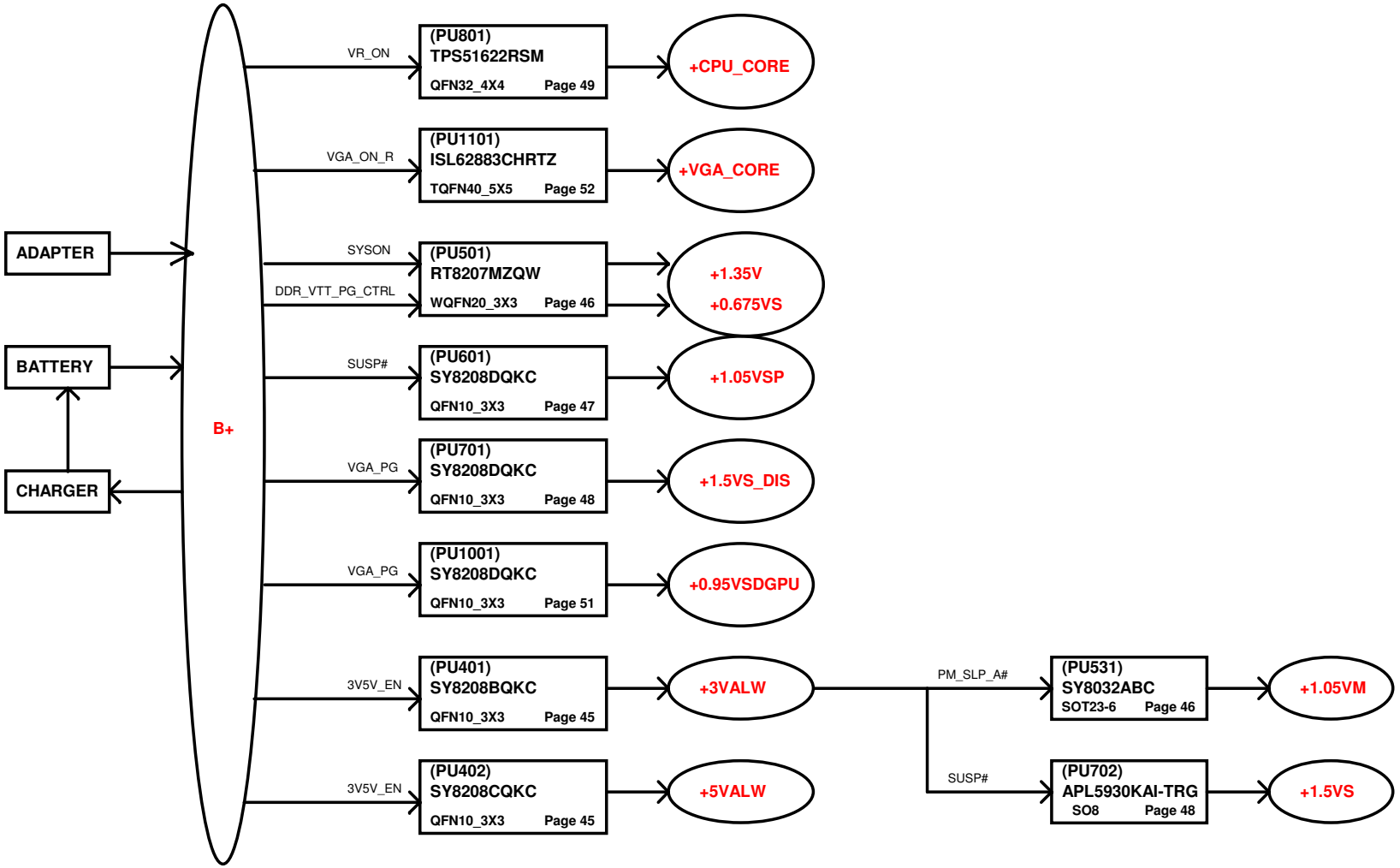

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: Power Tree

Size: Custom | Document Number: Z4DBH M/B LA-B731P Schematic | Rev: 0.1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	Design Change for common part circuit	0.2	46	Delete PR505 resister	2014/03/24	DVT
02	Design Change.	Design Change for CPU transient test	0.2	49	Change PR833, 1.91k ohm to 3.65k ohm		
03	Design Change.	Design Change for CPU transient test	0.2	49	Change PR835, 4.99M ohm to 10M ohm		
04	Design Change.	Design Change for CPU transient test	0.2	49	Change PR850, 392 ohm to 475 ohm		
05	Design Change.	Design Change for CPU transient test	0.2	49	Change PR852, 2.61k ohm to 10k ohm		
06	Design Change.	Design Change for CPU transient test	0.2	49	Change PR854, 121k ohm to 102k ohm		
07	Design Change.	Design Change for CPU transient test	0.2	49	Change PC828, 0.033u F to 0.022u F		
08	Design Change.	Design Change for Efficiency test	0.2	47	Change PC639, 47u F to 22u F		
09	Design Change.	Design Change for Efficiemcy test	0.2	47	Change PC640, 47u F to 22u F		
10	Design Change.	Design Change for Efficiemcy test	0.2	47	Add PC643 22u F		
11	Design Change.	Design Change for 1.05VMP circuit	0.2	46	Change PR531 100k to 10k for CL_RST1# high > 500us after APWROK high		
12	Design Change.	Design Change for charger circuit	0.2	44	Change PQ302 AON6414AL to MDU1512		
13	Design Change.	Design Change for charger circuit	0.2	44	Change PQ303 AON6414AL to AON7506		
14	Design Change.	Design Change for charger circuit	0.2	44	Change PQ304 AON6414AL to AON7506		
15	Design Change.	Design Change for charger circuit	0.2	44	Change PQ306 AON7408 to AON7406		
16	Design Change.	Design Change for charger circuit	0.2	44	Change PC302 0.1uF to 0.01uF		
17	Design Change.	Design Change for charger circuit	0.2	44	Change PC302 0.01uF to 0.1uF		
18	Design Change.	Design Change for 3VALW 5VALW	0.2	45	Del PR405 4.3k ohm		
19	Design Change.	Design Change for DCIN circuit	0.2	42	Del PQ101, PD103, PD104, PR107, PR109, PC107, PC106, PR108, PR105, PU101, PC105, PR104, PR109		
20	Design Change.	Design Change for Battery Conn & OTP	0.2	43	Change PR214 16.9kohm to 21kohm, change OTP trigger temperture to 85 degree		

Security Classification	Compal Secret Data		
Issued Date	2012/06/19	Deciphered Date	2012/07/31

Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom	V4DA2 LAA131P Schematic	0.1

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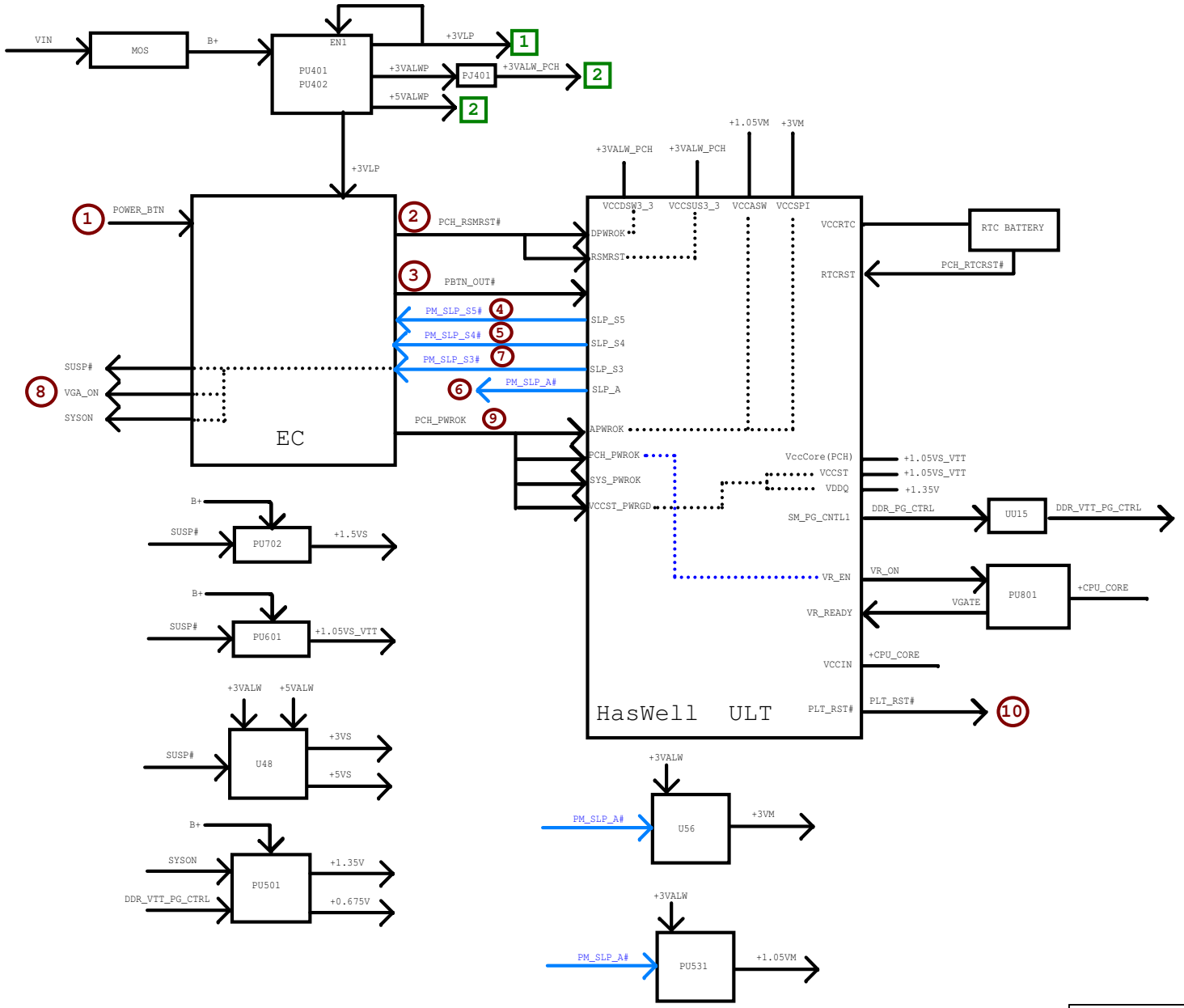

Title	Power Block	
Size B	Document Number <Doc>	Rev
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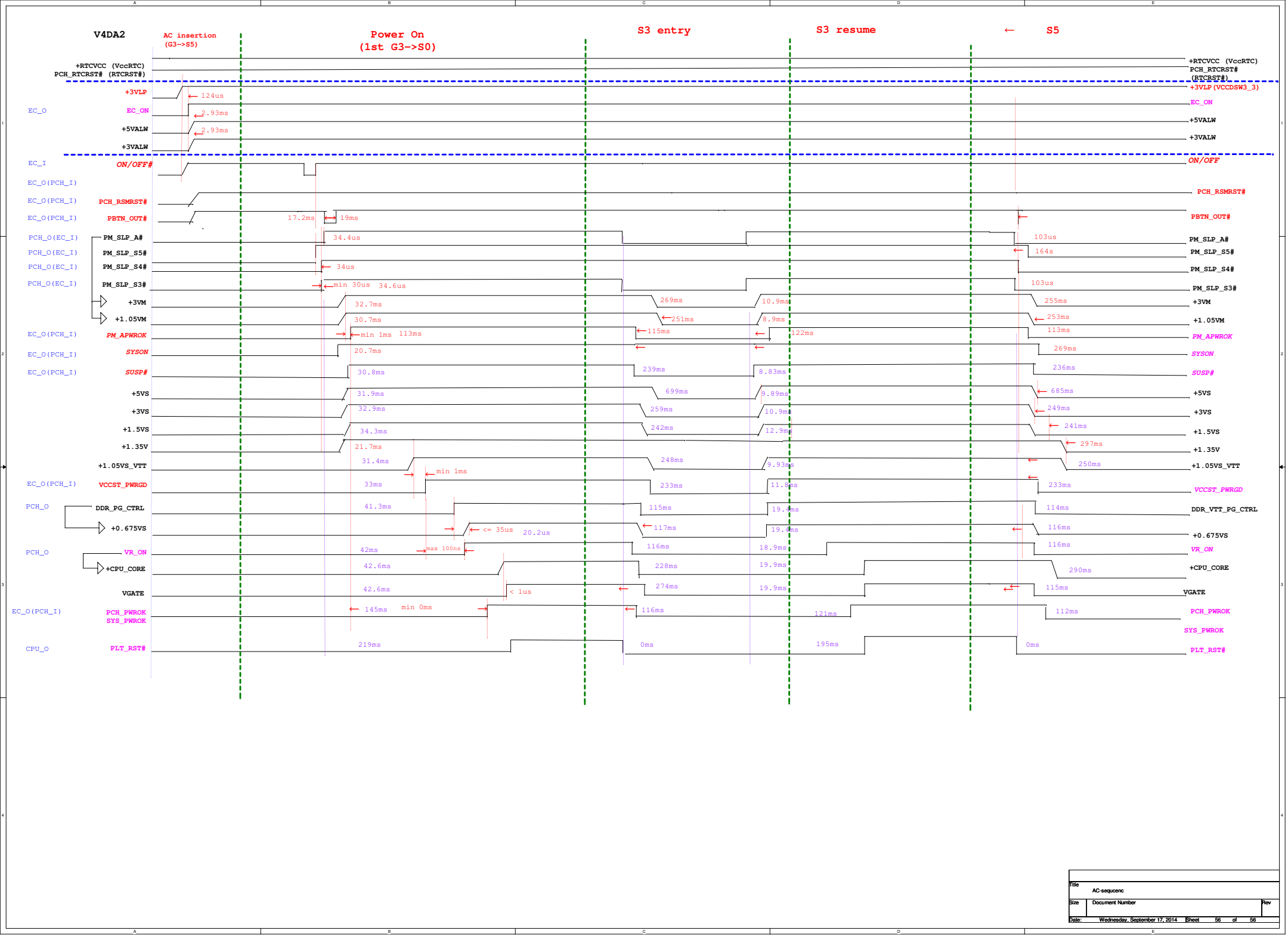

Title	AC-sequenc	
Size	Document Number	Rev
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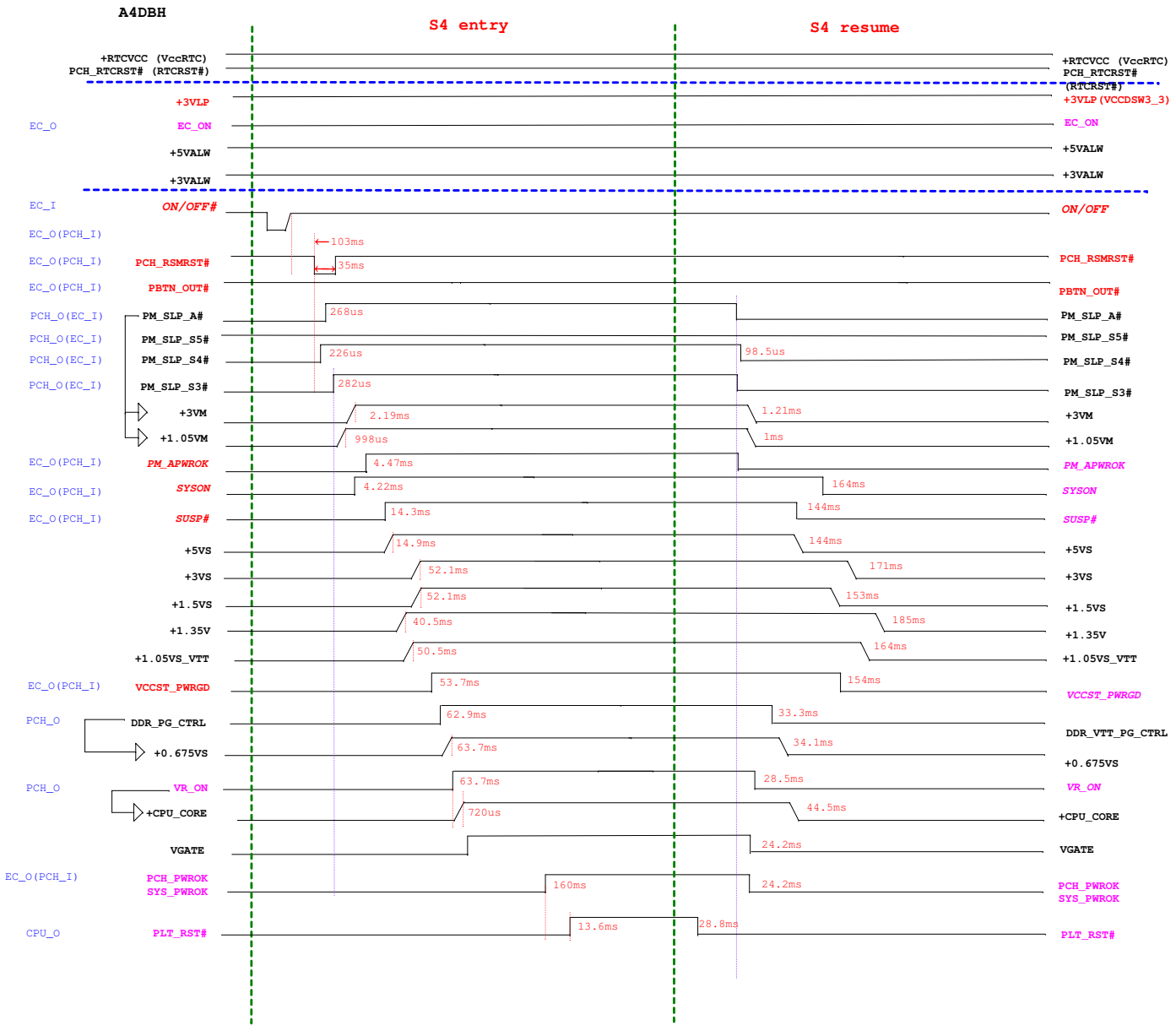

Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
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EVT2-->DVT

1.Page 40, Add Fan driver IC
2.Page 18, Remove Alert of GPU
3.Page 37,Update EC version to D
4.Page 28,R633,R665,R667,R668,R669,R671,R630,R631 change to 6.2ohm
5.Page 28,L15~L18 change to @EMI@
6.Page 31,Add RL18 for second source
7.Page 35,Add CLP1 and CLP2 for 3G door
8.Page 37,R483 change to 15K for EC ID
9.Page 29,remove R746~R749,R757~R759
10.Page 11, Add CU157 and CU158 for ESD@
11.Page 37,Remove JDB1
12.Page 27,Add R762
13.Page 4,Update CPU BOM option

DVT-->PVT

1.Page 35, remove CLP1 and CLP2
2.Page 41,U48 change PN to SA00006U300
3.Page 18, GPU thermal SMBUS connect change to EC SMBUS_2
4.Page 18,DGPU_HOLD_RST# change to Pull-Low
5.QA3 and Q23 and Q25 change PN to SB00000PJ00
6.Page 36, D37 and D44 change to @ESD@
7.Page 37,EC Board ID, R483 change to 20K
8.Page 8, RU161 BOM structure change to UMA@
9.Page1,change DAZ number to DAZ18000300
10.Page 1,LS-A135P change to LS-B734P (Finger Print)
11.Page 29,Create X76PAR@ and X76TI@
12.Page 4, Add CPU BOM option
13.Page ,C520,C522,C523,C524,C525,C526 form SE068330K80 change to SE071330J80
14.Page9 ,RU176 change to mount

Title: <Title>		
Size: A	Document Number: <Doc>	Rev: <RevCode>
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