Bitland Confidential

M/B Schematics Document

Intel Braswell-M Platform

V1.2

2015-04-15

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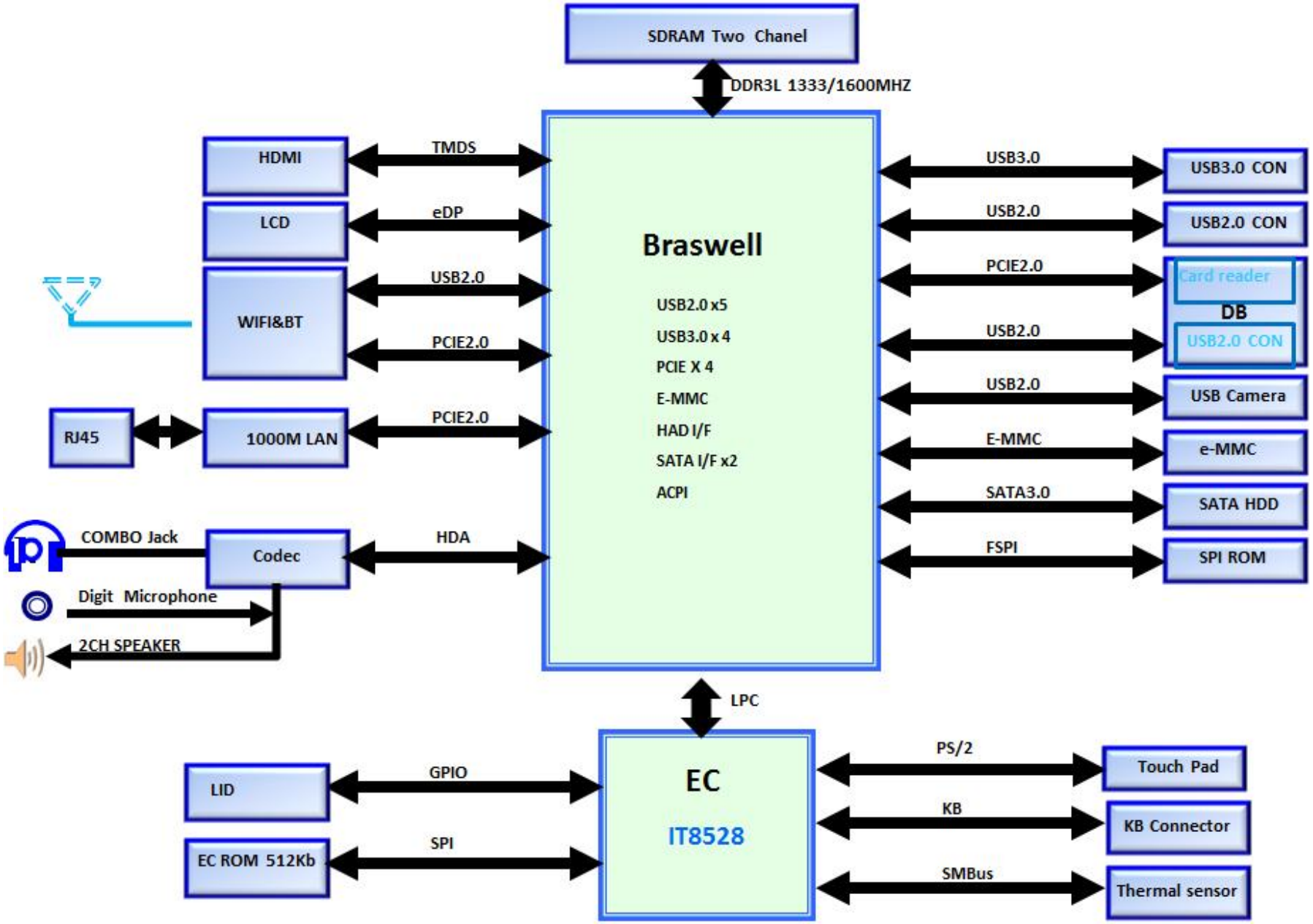

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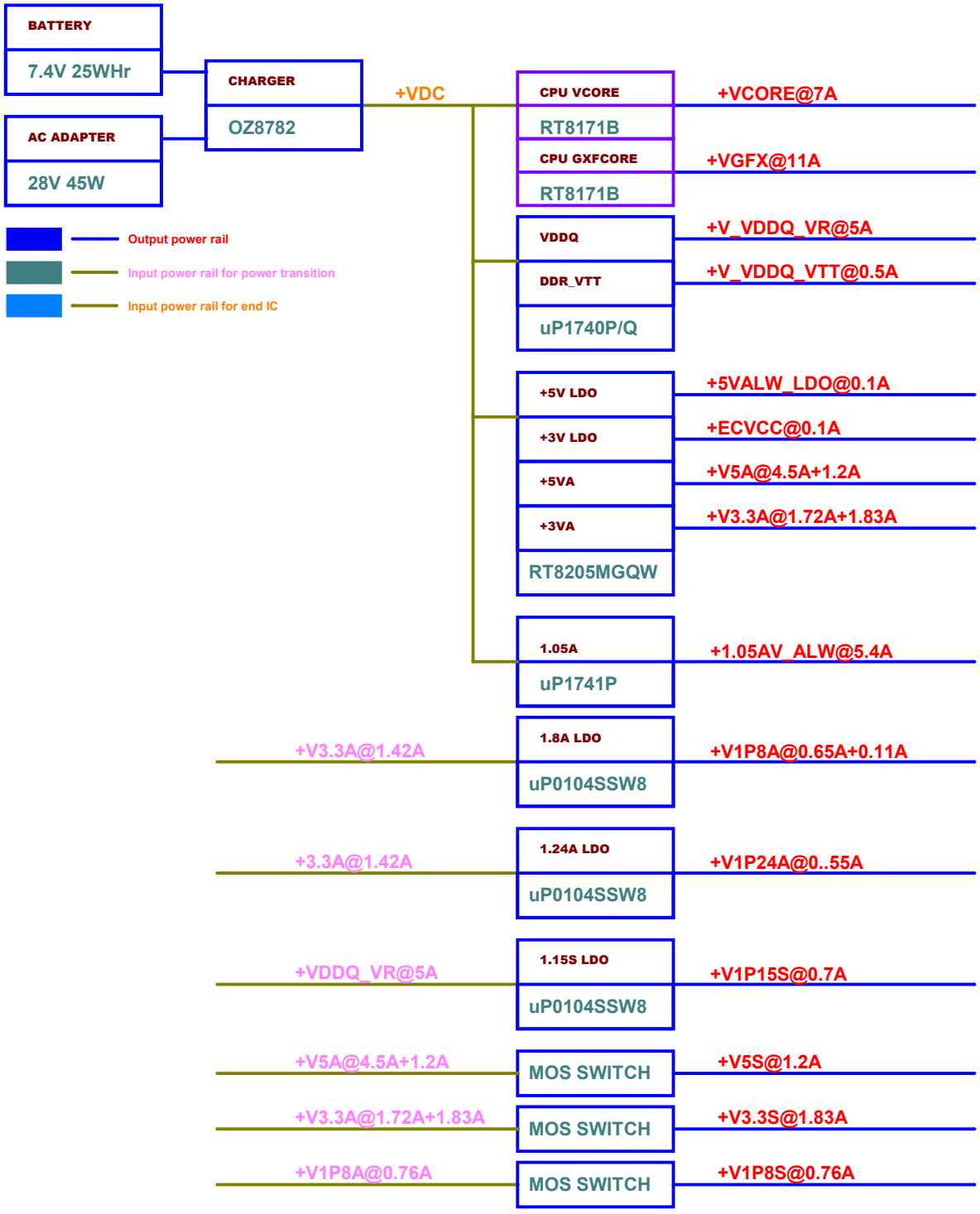

Power States

Power Rail	On S0	On S3	On S4/S5	On G3
VRTC	ON	ON	ON	ON
VCore1/0	ON	OFF	OFF	OFF
VGG	ON	OFF	OFF	OFF
VDDQ_VTT	ON	OFF	OFF	OFF
+V1.8S	ON	OFF	OFF	OFF
+V3.3S	ON	OFF	OFF	OFF
+V5S	ON	OFF	OFF	OFF
+V1.15S	ON	OFF	OFF	OFF
VDDQ_VR	ON	ON	OFF	OFF
+V3.3A_PRIME	ON	ON	ON	OFF
+V1.8A	ON	ON	ON	OFF
+V1.24A	ON	ON	ON	OFF
+V1.05A	ON	ON	ON	OFF
+V3.3A	ON	ON	ON	OFF
+V5A	ON	ON	ON	OFF

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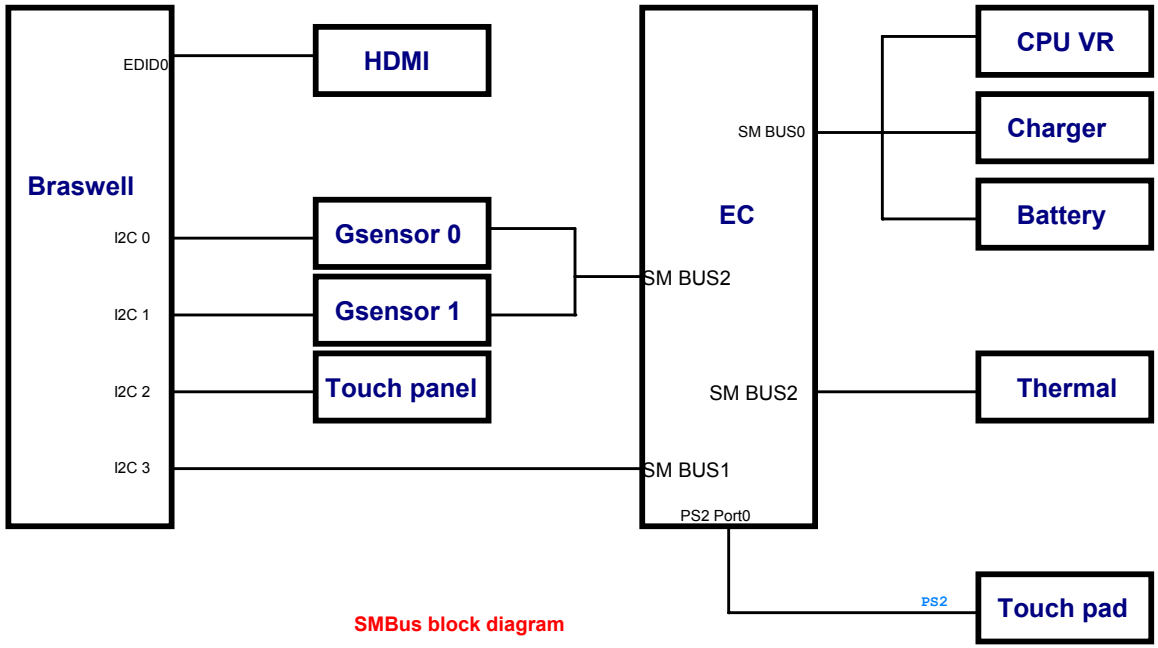
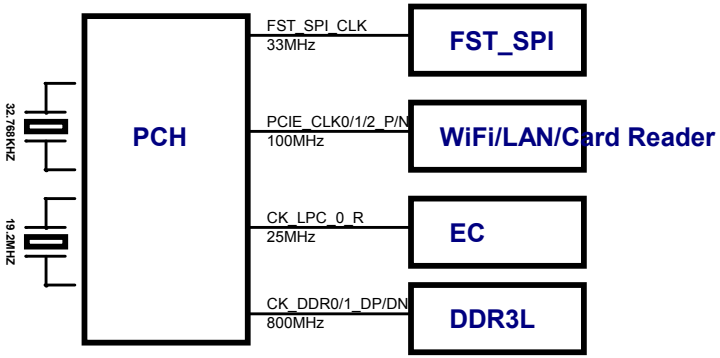


SMBus block diagram



Clock block diagram

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+VDIMM
+V3.3S
14,18,19,40,41
8,14,20,23,24,26..28,31,32,34,44
+V3.3A
+V1.8A
10,12,20,24,26..28,33,34,37..44
8..12,14,16,20,23..25,27,31,39,44
U1A
CHV_MCP_EDS
DDR0
M_A_A15
M_A_A[14:0]
M_A_DQ[63:0]
M_A_BS2
M_A_BS1
M_A_BS0
M_A_CAS_N
M_A_RAS_N
M_A_WE_N
M_A_DIM0_CS1_N
M_A_DIM0_CS0_N
M_A_DIM0_CKE1
M_A_DIM0_CK_DDR0_DP
M_A_DIM0_CK_DDR0_DN
M_A_DIM0_CKE0
MA_MON1P
MA_MON1N
M_A_DIM0_ODT0
M_A_DIM0_ODT1
MA_OCAVREF
MA_ODQVREF
MA_DRAMRST_N
DDR3_DRAM_S4_PWROK
M_A_DM[7..0]
M_A_DQS_N[7:0]
M_A_DQS_P[7:0]
EMC add C337
Add R37 for RC filter 0415
0.8Ver CRB 182Ohm
CHV_MCP_EDS/BGA
1 OF 13
U1B
DDR1
M_B_A15
M_B_A[14:0]
M_B_DQ[63:0]
M_B_BS2
M_B_BS1
M_B_BS0
M_B_CAS_N
M_B_RAS_N
M_B_WE_N
M_B_DIM0_CS1_N
M_B_DIM0_CS0_N
M_B_DIM0_CKE1
M_B_DIM0_CK_DDR0_DP
M_B_DIM0_CK_DDR0_DN
M_B_DIM0_CKE0
MB_MON1P
MB_MON1N
M_B_DIM0_ODT0
M_B_DIM0_ODT1
MB_OCAVREF
MB_ODQVREF
MB_DRAMRST_N
DDR3_VCCA_PWROK
Add R37 for RC filter 0415
EMC add C336
M_B_DQS_N[7..0]
M_B_DQS_P[7..0]
PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACE
PLACE 0.1UF CAP CLOSE TO CPU
SLP_S4_EC_N
Q55A L2N7002DW1T1G
Q55B L2N7002DW1T1G
VDDQ_PWRGD
D16 0.37V_30mA_LRB751V-40T1G sod323
add 0.1UF FOR EMI 1028
10K change to 1K from checklist0.92 1011
DDR3_VCCA_PWROK_3P3
PLTRST_N
PLT_RST#
Q33 LMBT3904DW1T1G SOT363
EMC add C284 0627
EMC add 1029
follow CRB0.9 1008wls
PLACE THE RESISTORS AS CLOSE AS POSSIBLE TO SOC,ROUTE THEM AS SINGLE ENDED LINES

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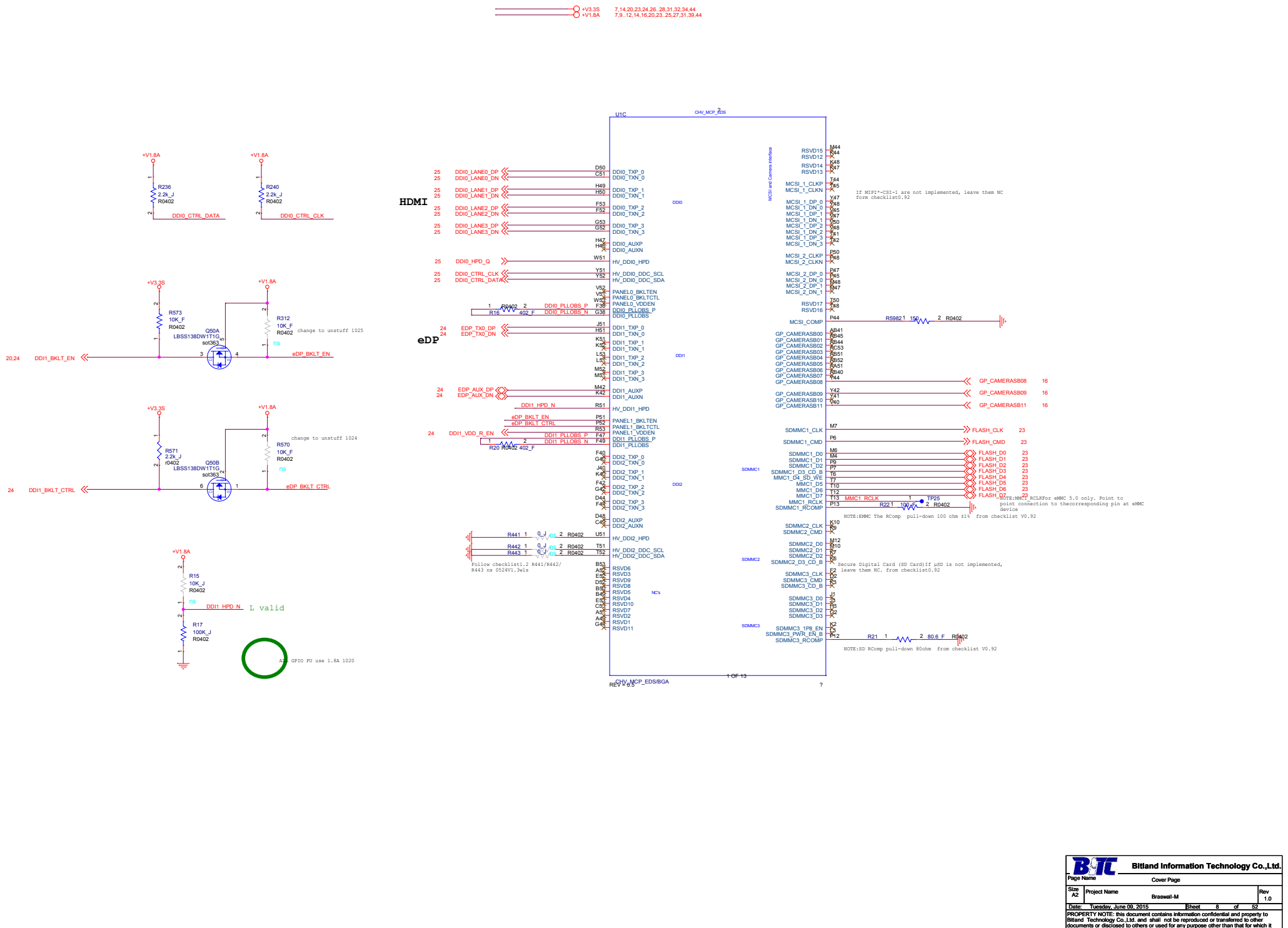
+V3.3S 7,14,20,23,24,26..28,31,32,34,44
+V1.8A 7,9..12,14,16,20,23..25,27,31,39,44
HDMI
eDP
U1C
CHV_MCP_EDS
CHV_MCP_EDS/BGA
1 OF 13
REV = 0.5
DDI0_CTRL_DATA
DDI0_CTRL_CLK
DDI1_BKLT_EN
eDP_BKLT_EN
change to unstuff 1025
DDI1_BKLT_CTRL
eDP_BKLT_CTRL
change to unstuff 1024
DDI1_HPD_N
L valid
If MIPI*-CSI-1 are not implemented, leave them NC form checklist0.92
NOTE:EMMC The RComp pull-down 100 ohm ±1% from checklist V0.92
Secure Digital Card (SD Card)If µSD is not implemented, leave them NC. from checklist0.92
NOTE:SD RComp pull-down 80ohm from checklist V0.92
NOTE:MMC1_RCLKFor eMMC 5.0 only. Point to point connection to thecorresponding pin at eMMC device
Follow checklist1.2 R441/R442/ R443 ns 0524V1.3wls
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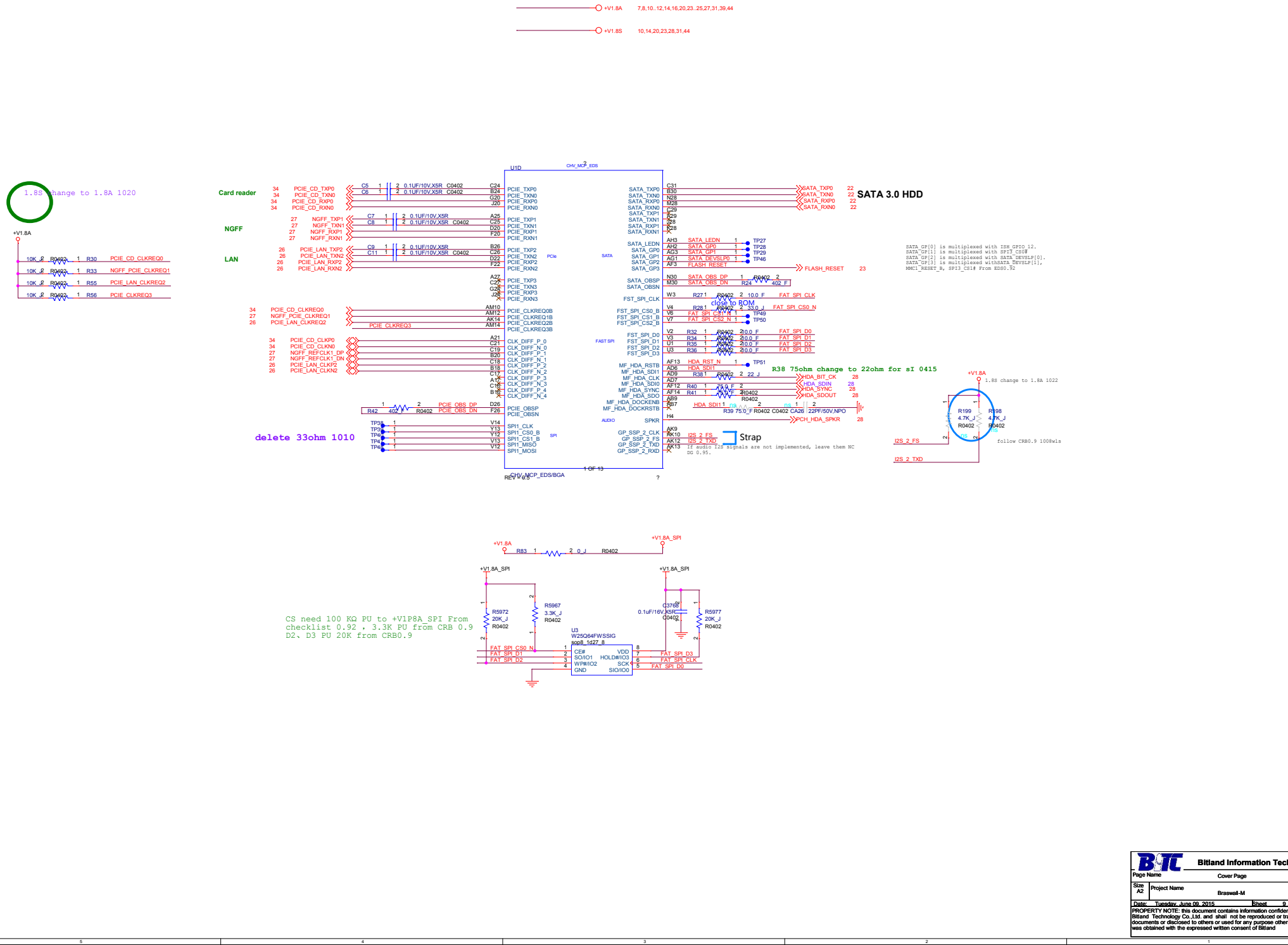

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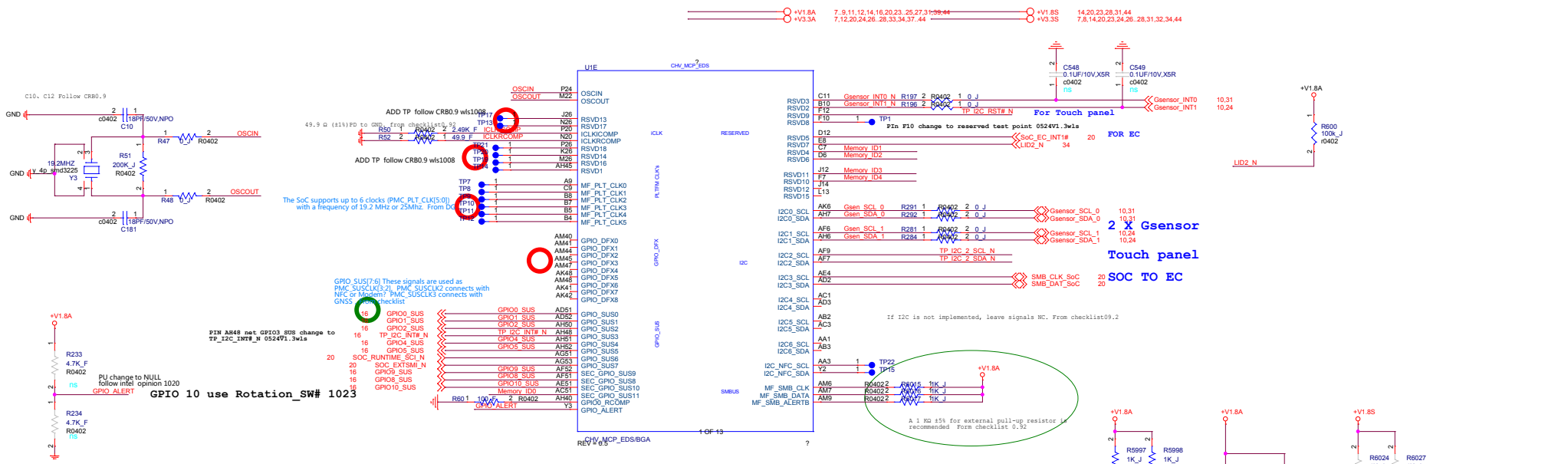

Memory_ID1	Memory_ID2	Memory_ID3	Memory_ID4	SDRAM Configuration
0(R294)	0(R296)	0(R298)	0(R301)	Hynix H5TC4G63AFR-PBA
0(R294)	0(R296)	0(R298)	1(R302)	Hynix H5TC8G63AMR-PBA
0(R294)	0(R296)	1(R300)	0(R301)	Micron MT41K256M16HA-125:E
0(R294)	0(R296)	1(R300)	1(R302)	Micron MT41K512M16TNA-125:E
0(R294)	1(R297)	0(R298)	0(R301)	Elpida EDJ4216EFBG-GN-F
0(R294)	1(R297)	0(R298)	1(R302)	Elpida EDJ8416E6MB-GN-F
0(R294)	1(R297)	1(R300)	0(R301)	Samsung K4B4G1646Q-HYK0
0(R294)	1(R297)	1(R300)	1(R302)	Samsung K4B8G1646Q-MYK0
1(R295)	0(R296)	0(R298)	0(R301)	Hynix H5TC2G63FFR-PBA
1(R295)	0(R296)	0(R298)	1(R302)	Micron MT41K128M16JT-125K
1(R295)	0(R296)	1(R300)	0(R301)	Samsung K4B2G1646Q-BYK0

add memory_ID_101xx

Memory_ID0	Channel Configuration
1(R293)	Single
0(R288)	Double

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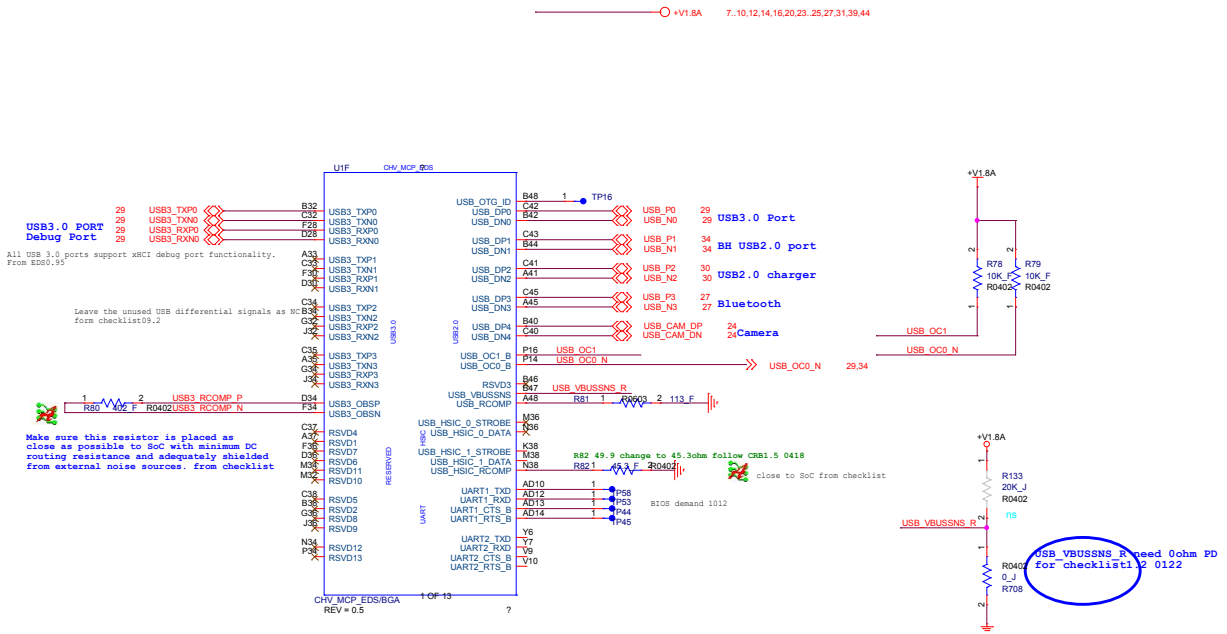

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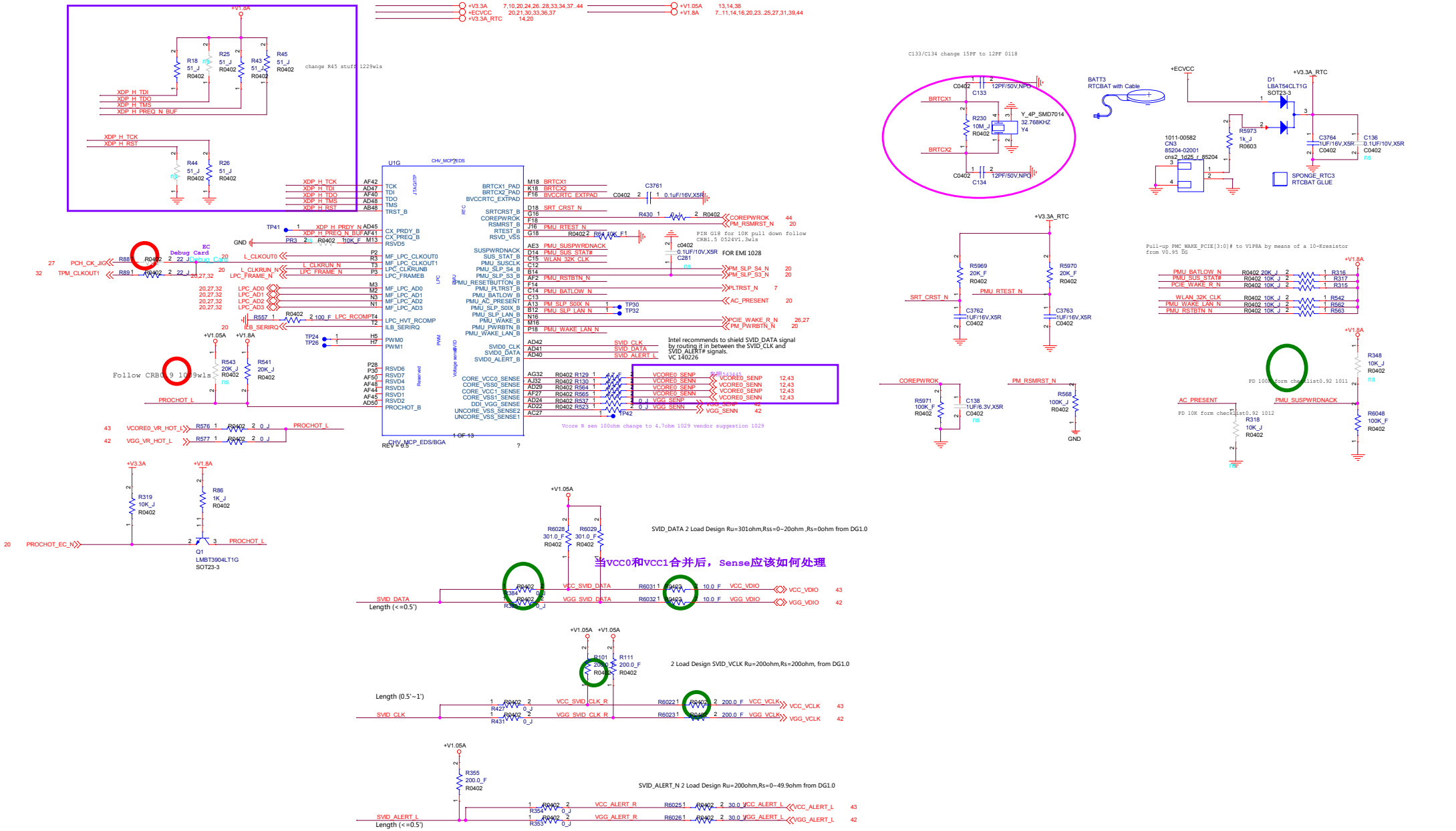

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+VCORE0 43
+VGG 42

+V1.15S 41
+V1.05A 12,14,38

+VNN change to +V1.05A

5x 0402 1 µF
3x 0603 22 µF

3x 0402 4.7 µF
2x 0603 22 µF

3x 0402 4.7 µF
2x 0603 22 µF

5x 0402 10 µF

10UF 0603 change to 4.7uf 0402 for layout 1028

4x 0402 1 µF
2x 0402 1 µF

3x 0402 1 µF
2x 0402 1 µF

1x 0402 1 µF Back Side Cap to be placed at outside of package die shadow
2x 0603 22 µF

0805 0ohm change to PJ44 1020
delete C23 C33 for layout 1029

Place STICHING CAPS IF necessary

change to NC from 553578 1022

CAD NOTE:
PLACE CLOSE TO PIN 1 OF RA

CAD NOTE:
PLACE CLOSE TO PIN 1 OF RA

U1H CHV_MCP_EDS

1 OF 13

CHV_MCP_EDS/BGA

REV = 0.5

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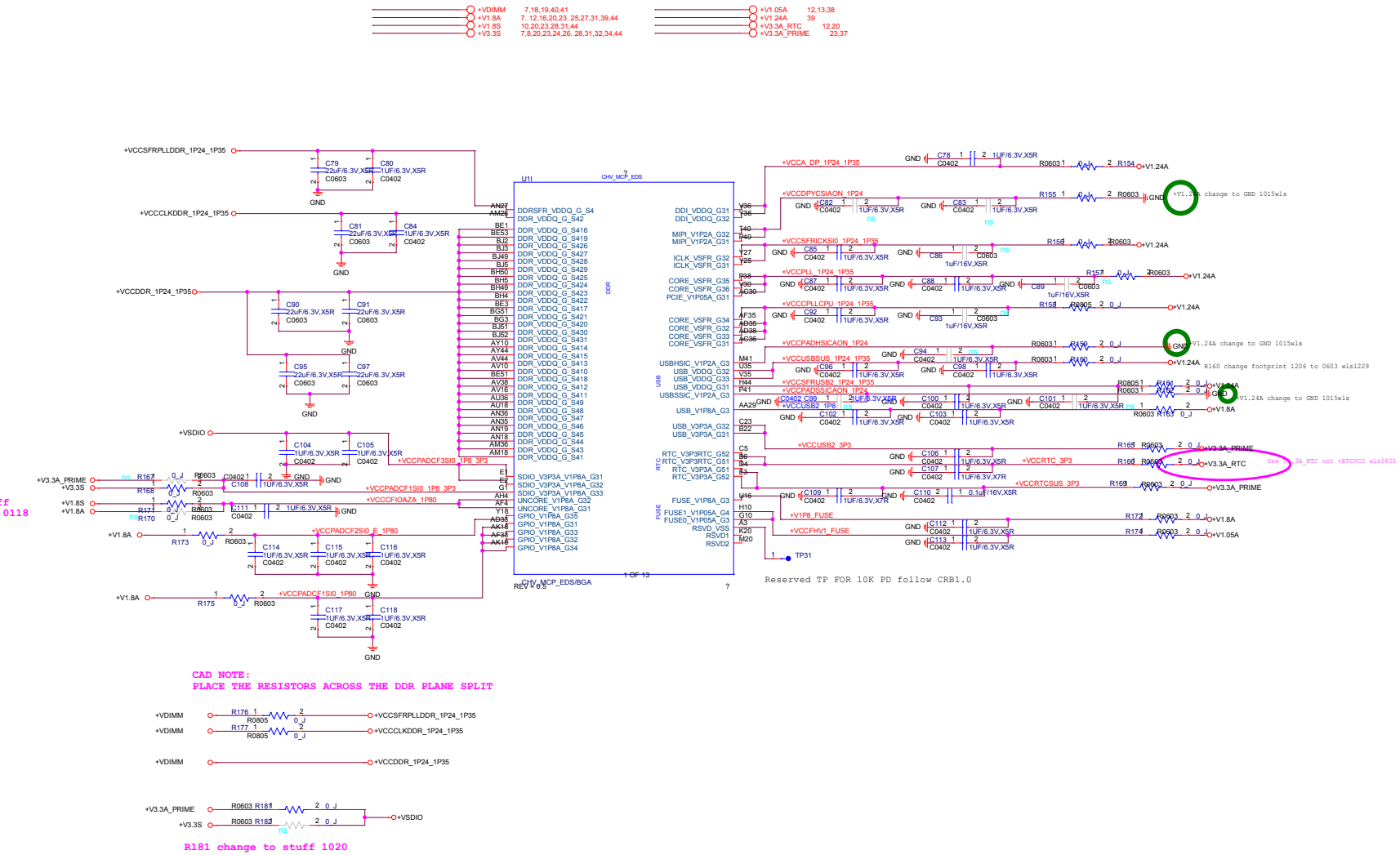

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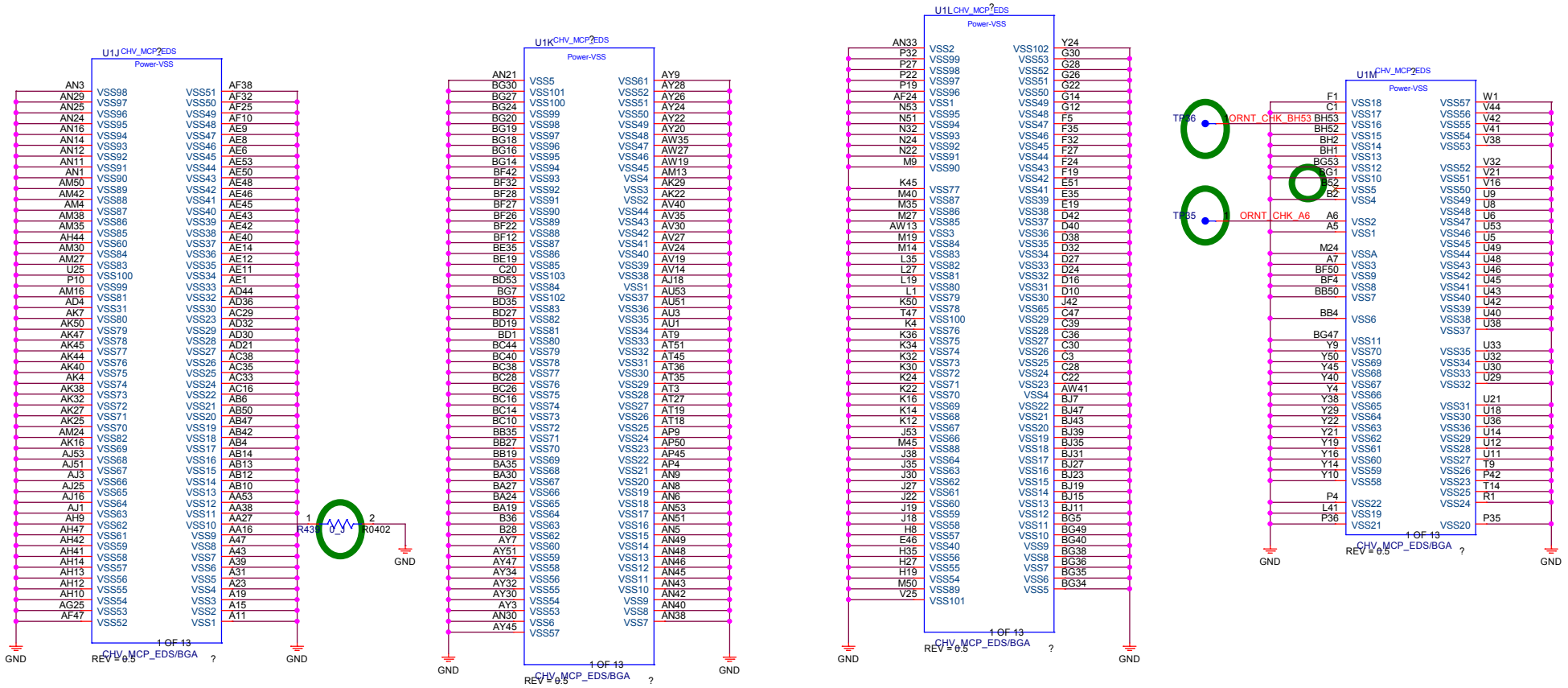

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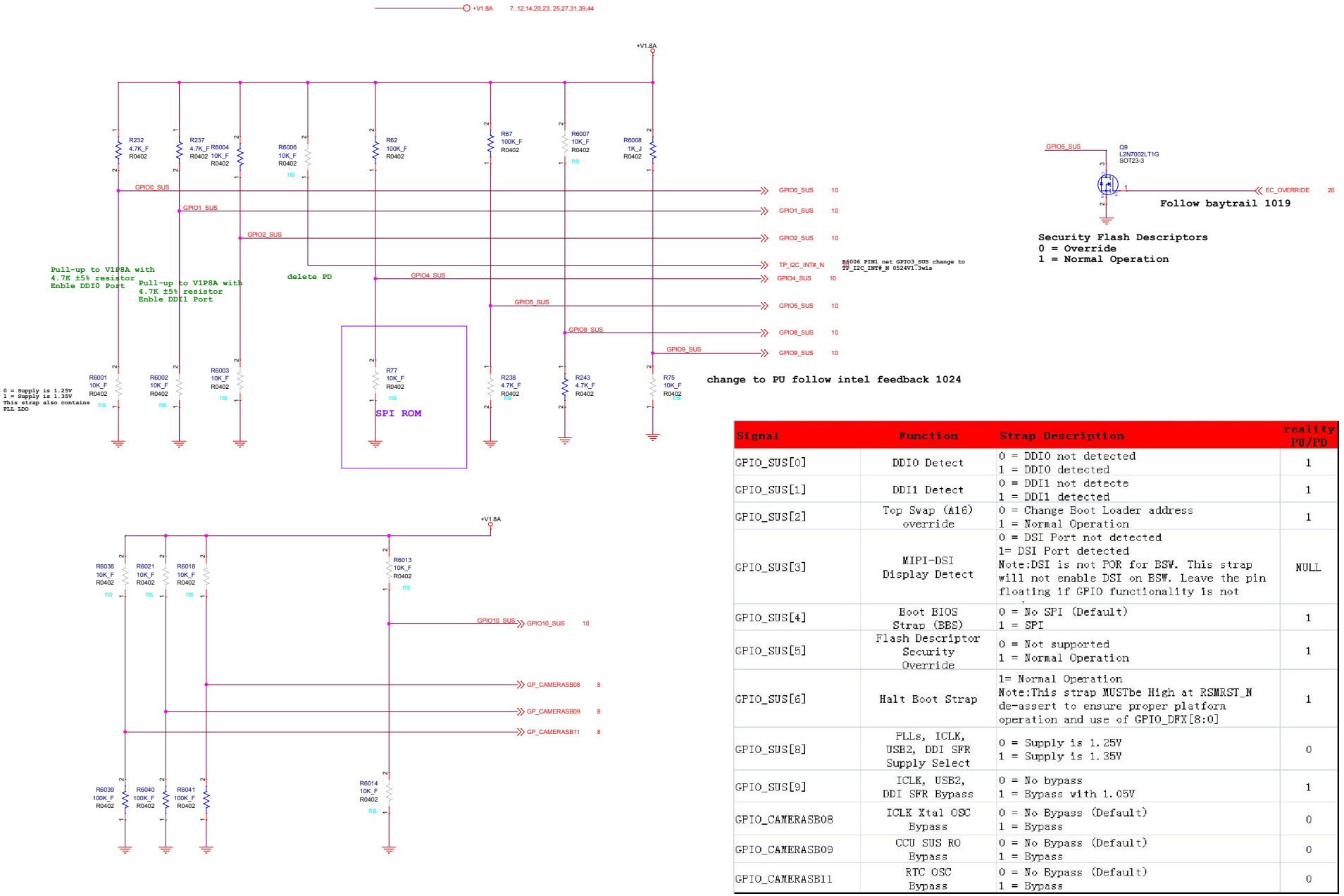

Signal	Function	Strap Description	reality PU/PD
GPIO_SUS[0]	DDI0 Detect	0 = DDI0 not detected 1 = DDI0 detected	1
GPIO_SUS[1]	DDI1 Detect	0 = DDI1 not detecte 1 = DDI1 detected	1
GPIO_SUS[2]	Top Swap (A16) override	0 = Change Boot Loader address 1 = Normal Operation	1
GPIO_SUS[3]	MIPI-DSI Display Detect	0 = DSI Port not detected 1= DSI Port detected Note:DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not	NULL
GPIO_SUS[4]	Boot BIOS Strap (BBS)	0 = No SPI (Default) 1 = SPI	1
GPIO_SUS[5]	Flash Descriptor Security Override	0 = Not supported 1 = Normal Operation	1
GPIO_SUS[6]	Halt Boot Strap	1= Normal Operation Note:This strap MUSTbe High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]	1
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	0 = Supply is 1.25V 1 = Supply is 1.35V	0
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	0 = No bypass 1 = Bypass with 1.05V	1
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	0 = No Bypass (Default) 1 = Bypass	0
GPIO_CAMERASB09	CCU SUS RO Bypass	0 = No Bypass (Default) 1 = Bypass	0
GPIO_CAMERASB11	RTC OSC Bypass	0 = No Bypass (Default) 1 = Bypass	0

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+VDIMM 7,14,19,40,41

+VTT_DDR 19,40

M_A_DQ[63:0] 7

M_A_DQS_[7:0] 7

M_A_DQS_N[7:0] 7

U17

NT5CB64M16DP-CF

U16

NT5CB64M16DP-CF

U19

NT5CB64M16DP-CF

U18

NT5CB64M16DP-CF

1UF Cap Place as close to DRAM as possible

FOR EMI 0122

Ctt for CAC/CLK = 80 ± 5%
Ctt = 0.1 uF, Cterm = 0.2 pF
From Memor Down DG

Note: Place these Caps near to respective DIMM Pins

change filter cap to 0.1uF
divider res change to 4.7K_F
add C217 C248

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+VDIMM 7,14,18,40,41

+VTT_DDR 18,40

M_B_DQ[63:0] 7

U72

U73

U74

U75

NT5CB64M16DP-CF

+V_VREF_DQ_DIMM1 19

+V_VREF_CA_DIMM1 19

+VTT_DDR

Att For CAC/CLK = 80 ± 5%
CCC = 0.1 μF, Cterm = 0.2 pF
From Memor Down DQ

Note: Place these Caps near to respective DIMM Pins

change filter cap to 0.1uF
divider res change to 4.7K_F
add C217 C248

FOR EMI 0122

1UF Cap Place as close to DRAM as possible

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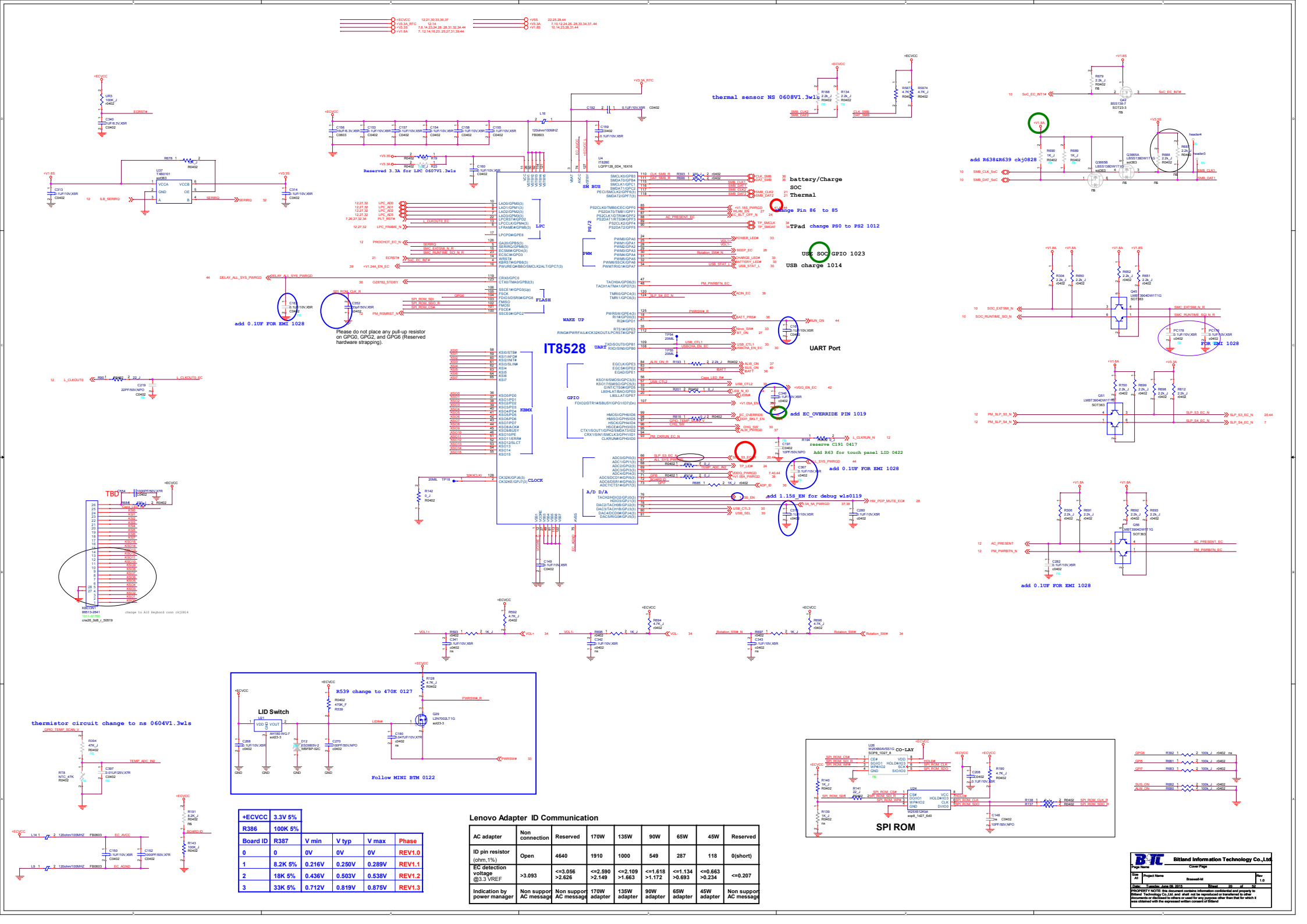

+ECVCC	3.3V 5%				
R386	100K 5%				
Board ID	R387	V min	V typ	V max	Phase
0	0	0V	0V	0V	REV1.0
1	8.2K 5%	0.216V	0.250V	0.289V	REV1.1
2	18K 5%	0.436V	0.503V	0.538V	REV1.2
3	33K 5%	0.712V	0.819V	0.875V	REV1.3

Lenovo Adapter ID Communication

AC adapter	Non connection	Reserved	170W	135W	90W	65W	45W	Reserved
ID pin resistor (ohm,1%)	Open	4640	1910	1000	549	287	118	0(short)
EC detection voltage @3.3 VREF	>3.093	<=3.056 >2.626	<=2.590 >2.149	<=2.109 >1.663	<=1.618 >1.172	<=1.134 >0.693	<=0.663 >0.234	<=0.207
Indication by power manager	Non support AC message	Non support AC message	170W adapter	135W adapter	90W adapter	65W adapter	45W adapter	Non support AC message

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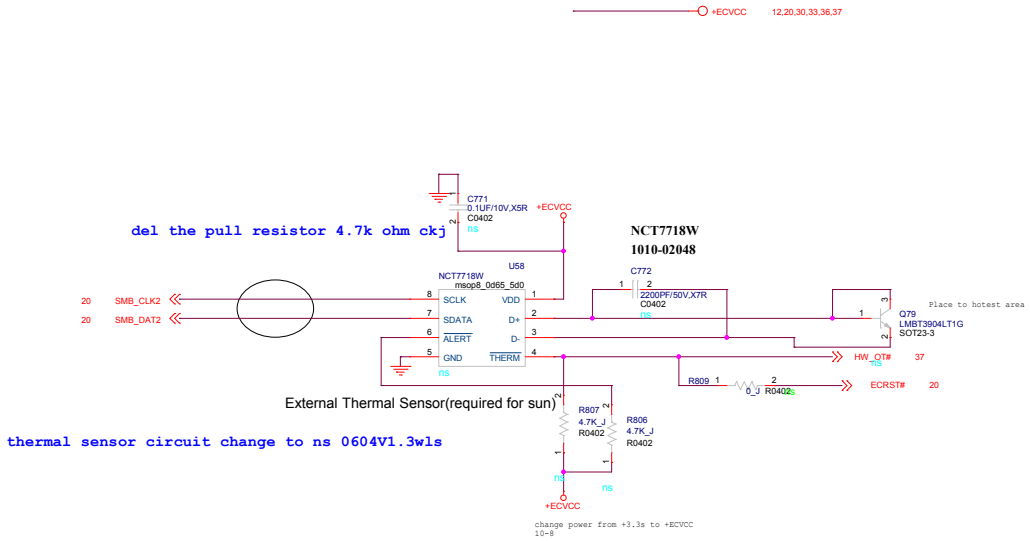

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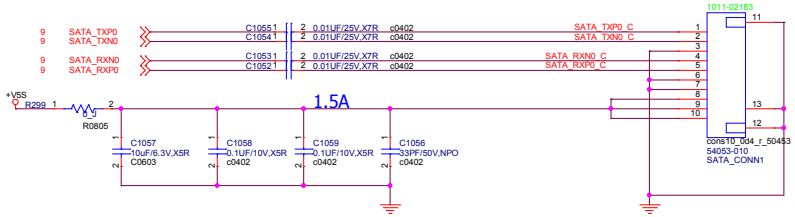
+V5S 25,28,44

Add CHK2 CHK5 R23 R19 R31 R29 FOR EMC 0415



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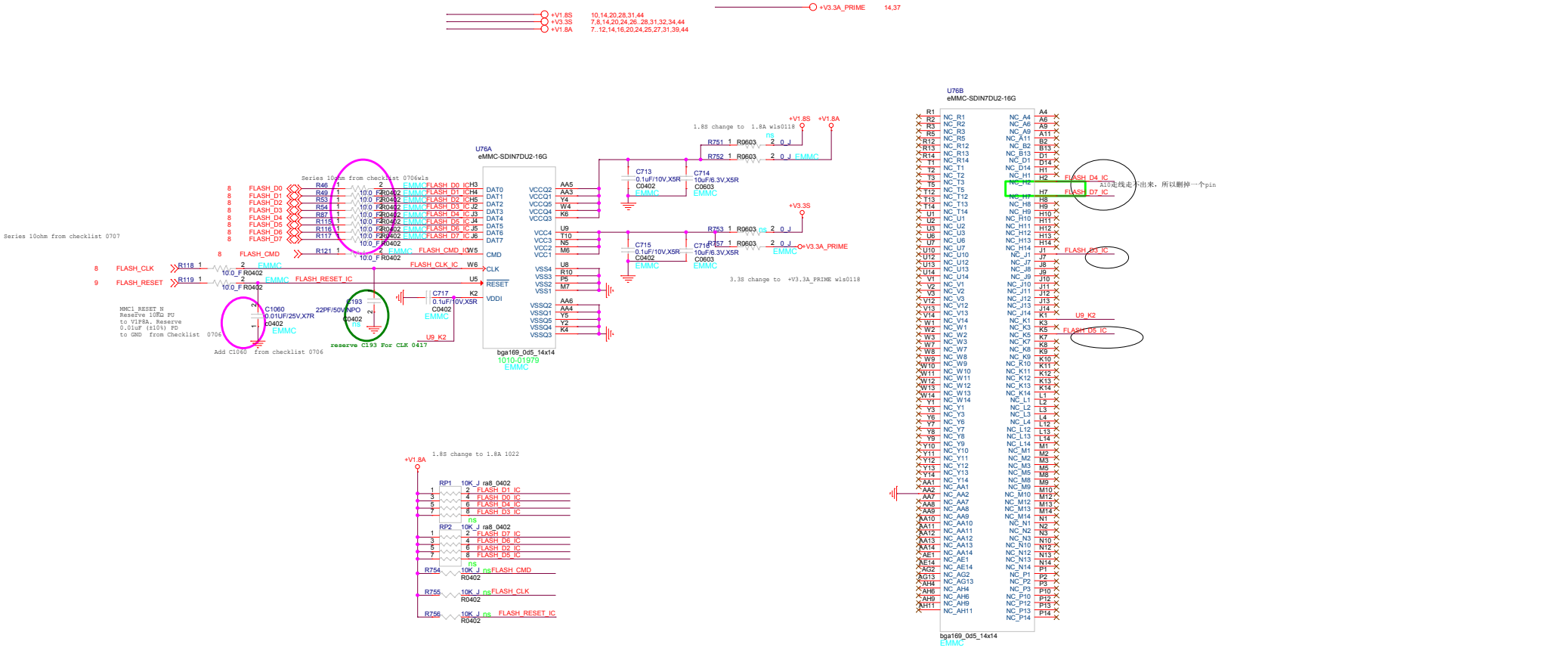

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+VDC 36..38,40,42..44
+V3.3S 7,8,14,20,23,26..28,31,32,34,44
+V3.3A 7..10,12,20,26..28,33,34,37..44
+V1.8A 7..12,14,16,20,23,25,27,31,39,44
+V1.8S 10,14,20,23,28,31,44

AUX Channel

8 EDP_AUX_DN C212 1 2 0.1UF/10V,X5R C0402 eDP_AUXN_C
8 EDP_AUX_DP C213 1 2 0.1UF/10V,X5R C0402 eDP_AUXP_C
R264 100K_F R0402 ns
R267 100K_F R0402 ns
CRB v1.0 unstuff
+V3.3S

LVDS_CLK-
LVDS_CLK+
LVDS_DATA0-
LVDS_DATA0+
LVDS_DATA1-
LVDS_DATA1+
LVDS_DATA2-
LVDS_DATA2+

Backlight control

20 EC_BLT_OFF_N From EC
8,20 DDI1_BKLT_EN From SOC
D4 LBAT54ALT1G SOT23-3
R270 10K_J R0402
C224 100PF/50V,NPO C0402 ns
R272 100K_J R0402
BKLT_ON

8 DDI1_BKLT_CTRL From PCH R274 1 2 0_J R0402 BKLT_PWM
R275 10K_J R0402
C225 1000PF/50V,X7R C0402 ns
EMC c169 nc->1000pf

Q8 EMF21P02V dfn8_0455_3x3
Q8 change to use QFN8 footfrint MOS 0420
500mA
C229 1UF/6.3V,X5R C0402
C190 0.1UF/16V,X5R C0402
C230 0.1UF/10V,X5R C0402 ns
R285 2 1 100K R0402
R0402 1K_J R286
R286 10K change to 1K 0524V1.3wls
R282 1 2 0_J R0805
500mA
C231 22UF/6.3V,X5R C0805 ns
C232 4.7UF/6.3V,X5R c0603
C233 0.1UF/10V,X5R C0402
C234 33PF/50V,NPO C0402
eDP_VDD
R283 75.0_J R0603 ns
Co_lay
R283 62ohm 0402 change to 75ohm 0603footprint 0418
R287 100K_J R0402 ns
Q14A L2N7002DW1T1G SOT363 ns
Q14B L2N7002DW1T1G SOT363 ns
8 DDI1_VDD_R_EN R289 2 1 1K_J R0402
Q11 LMBT3904LT1G sot23-3
R290 100K_J R0402

Screen backlight

PC15 0.1uF/25V,X7R C0603
+VDCO
eDP_VDD
LCD_CN15 Pitch=0.5mm_40Pin cns40_0d5_r_51540

Touch panel power

+V3.3AO
ns c0402 330pF/50V,X7R C546
ns c0402 330pF/50V,X7R C547
C207 4.7UF/6.3V,X5R C0603
C537 0.1UF/10V,X5R c0402
8 EDP_TX0_DN C251 1 2 0.1UF/10V,X5R C0402 eDP_TXN0_C
8 EDP_TX0_DP C298 1 2 0.1UF/10V,X5R C0402 eDP_TXP0_C
eDP_AUXP_C
eDP_AUXN_C
BKLT_PWM
BKLT_ON

Add 3.3A PU 1024

10 TP_I2C_2_SCL
10 TP_I2C_2_SDA
10 TP_I2C_RST#
10 TP_I2C_INT#
TP_I2C_RST#
TP_I2C_INT#
C545 0.1UF/10V,X5R c0402 ns
C544 0.1UF/10V,X5R c0402 ns
Gsensor_Power
GsensorIO1_Power
+V1.8AO
C15 0.1UF/10V,X5R C0402
C23 0.1UF/10V,X5R C0402

10 Gsensor_SCL_1
10 Gsensor_SDA_1
Gsensor_SCL_1
Gsensor_SDA_1
10 Gsensor_INT1
Gsensor_INT1

CAM_Power

+V3.3AO
C368 0.1UF/10V,X5R C0402
C250 4.7UF/6.3V,X5R C0603
+V3.3SO
+VDMIC
C538 0.1UF/10V,X5R c0402
USB_CAM_DP
USB_CAM_DN
DMIC_CLK
DMIC_DAT
20 TP_LID#
C195 150pF/50V,NPO C0402
C194 150pF/50V,NPO C0402

Gsensor_SCL_1
Gsensor_SDA_1
C145 150pF/50V,NPO C0402 ns
C23 150pF/50V,NPO C0402 ns
FOR EMI 0122

USB_CAM_DN 11
USB_CAM_DP 11

delete colay 0ohm 0605V1.3 wls

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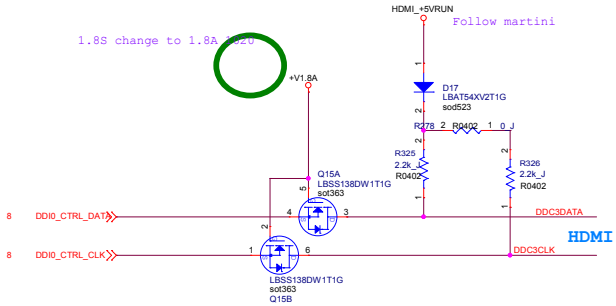
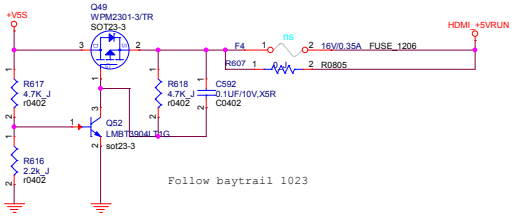
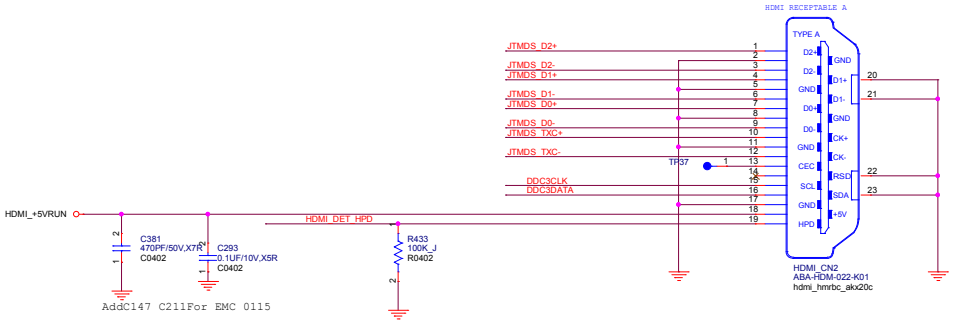
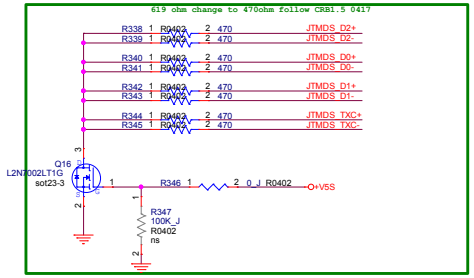
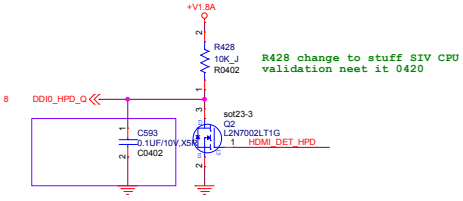




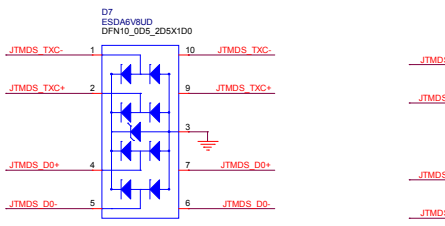
delete colay 0ohm 0605V1.3 wls

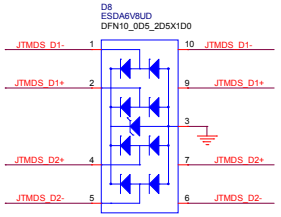


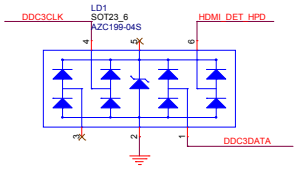




HDMI







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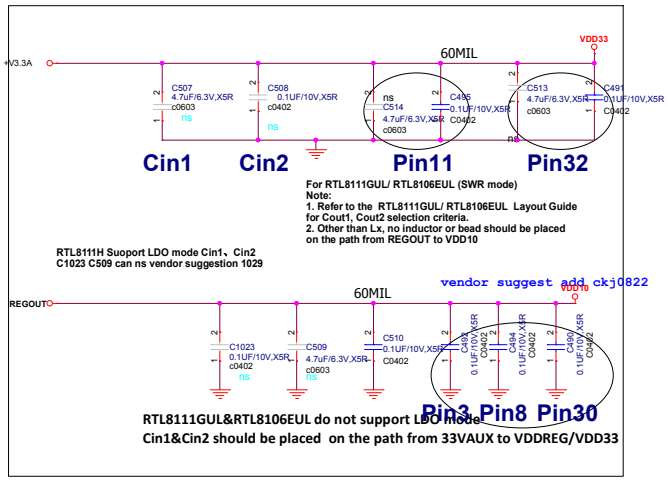
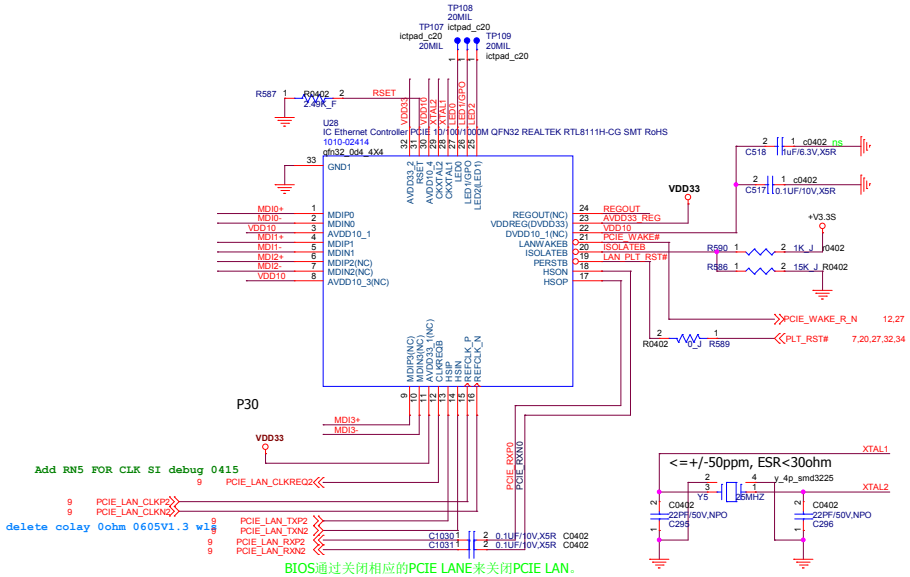
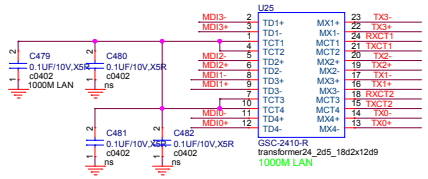
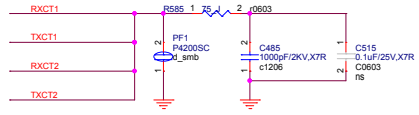
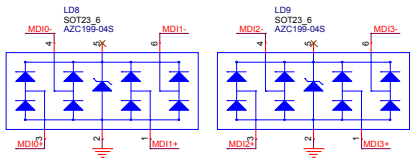
+V3.3A 7,10,12,20,24,27,28,33,34,37..44
+V3.3S 7,8,14,20,23,24,27,28,31,32,34,44

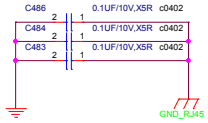


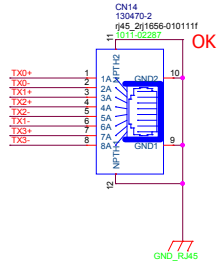












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+V3.3A 7,10,12,20,24,26,28,33,34,37..44
+V3.3S 7,8,14,20,23,24,26,28,31,32,34,44
+V1.8A 7..12,14,16,20,23..25,31,39,44

3.3V is available during the system's stand-by/suspend state to support wake event processing on the communications card.

+V3.3S +V3.3A ns R358 2 0_J R0805 place near Pin2 Pin72

C319 10UF/6.3V,X5R C0603
C320 0.1UF/10V,X5R C0402
C321 10UF/6.3V,X5R C0603
C322 0.1UF/10V,X5R C0402
C323 0.1UF/10V,X5R C0402
C324 10UF/6.3V,X5R C0603

WLAN_+3_3V

use 3.3S for WLAN 0122

WLAN_+3_3V change to 1.8A 0126

+V1.8A

WLAN_+3_3V

R569 3.3k_J r0402
R572 3.3k_J r0402

Q3677A LBSS138DW1T1G sot363
Q3677B LBSS138DW1T1G sot363

12,26 PCIE_WAKE_R_N PCIE_WAKE_R_N
9 NGFF_PCIE_CLKREQ1 NGFF_PCIE_CLKREQ1
PCIE_WAKE_R_N_NGFF
NGFF_PCIE_CLKREQ1_N

Reserved 3.3K vendor suggestion1210

Add Level_Shifter 1022

12,20,32 LPC_AD0 R0402 0_J R207 LAD0
12,20,32 LPC_AD1 R0402 0_J R208 LAD1
12,20,32 LPC_AD2 R0402 0_J R210 LAD2
12,20,32 LPC_AD3 R0402 0_J R212 LAD3
12,20,32 LPC_FRAME_N R0402 0_J R213 LFRAME#

PLACE near signal devided 10-15

WLAN_+3_3V

WIFI_CN5
NGFF SlotA-SD KeyE
ngff_conn_80152-2121

NGFF SlotA-SD

74	3.3Vaux3	GND1	75
72	3.3Vaux2	RESERVED1	73 LFRAME# LAD3
70	RESERVED3	RESERVED2	71
68	RESERVED4	GND2	69
66	RESERVED5	Reserved6/PERn1	67 PCH_CK_JIG 12
64	NFC Reset# (MGPIO7)/RESERVED	Reserved7/PERp1	65
62	NFC I2C IRQ (MGPIO5)/ALERT	GND3	63
60	NFC I2C SM CLK/I2C CLK	Reserved8/PETn1	61
58	NFC I2C SM DATA/I2C DATA	Reserved9/PETp1	59
56	W_DISABLE#1(WIFI)	GND4	57
54	Reserved/W_DISABLE#2(BT)	PEWake0#	55 PCIE_WAKE_R_N_NGFF
52	PERST0#	CLKRQ0#	53 R0402 R361 1 2 0_J ns NGFF_PCIE_CLKREQ1_N
50	SUSCLK	GND5	51
48	COEX1	REFCLKN0	49 NGFF_REFCLK1_DN NGFF_REFCLK1_DN 9
46	COEX2	REFCLKP0	47 NGFF_REFCLK1_DP NGFF_REFCLK1_DP 9
44	COEX3	GND6	45
42	CLINK_CLK/RESERVED	PERn0	43 NGFF_RXN1 9 pcie_RXN
40	CLINK_DATA/RESERVED	PERp0	41 NGFF_RXP1 9 pcie_RXP
38	CLINK_RST/RESERVED	GND7	39
36	UART RTS	PETn0	37 NGFF_TXN1 9 pcie_TXN
34	UART CTS	PETp0	35 NGFF_TXP1 9 pcie_TXP
32	UART Tx	GND8	33

KEY E

22	UART Rx	SDIO_RST	23
20	UART Wake	SDIOWAKE	21
18	GND9	SDIODAT3	19
16	LED#2	SDIODAT2	17
14	PCM_OUT	SDIODAT1	15
12	PCM_IN	SDIODAT0	13
10	PCM_SYNC	SDIOCMD	11
8	PCM_CLK	SDIOCLK	9
6	LED#1	GND10	7
4	3.3Vaux1	USB_D-	5 USB_N3 USB_N3 11
2	3.3Vaux0	USB_D+	3 USB_P3 USB_P3 11
		GND11	1
		GND12	76
		GND13	77
		P0	78
		P1	79

LAD2 LAD1 LAD0

20 WLAN_EN R360 2 2.2k_J 1 R0402 BT_DIABLE
20,27 BT_ON R362 2 0_J 1 R0402 PCIE_RST#_S
7,20,26,32,34 PLT_RST#

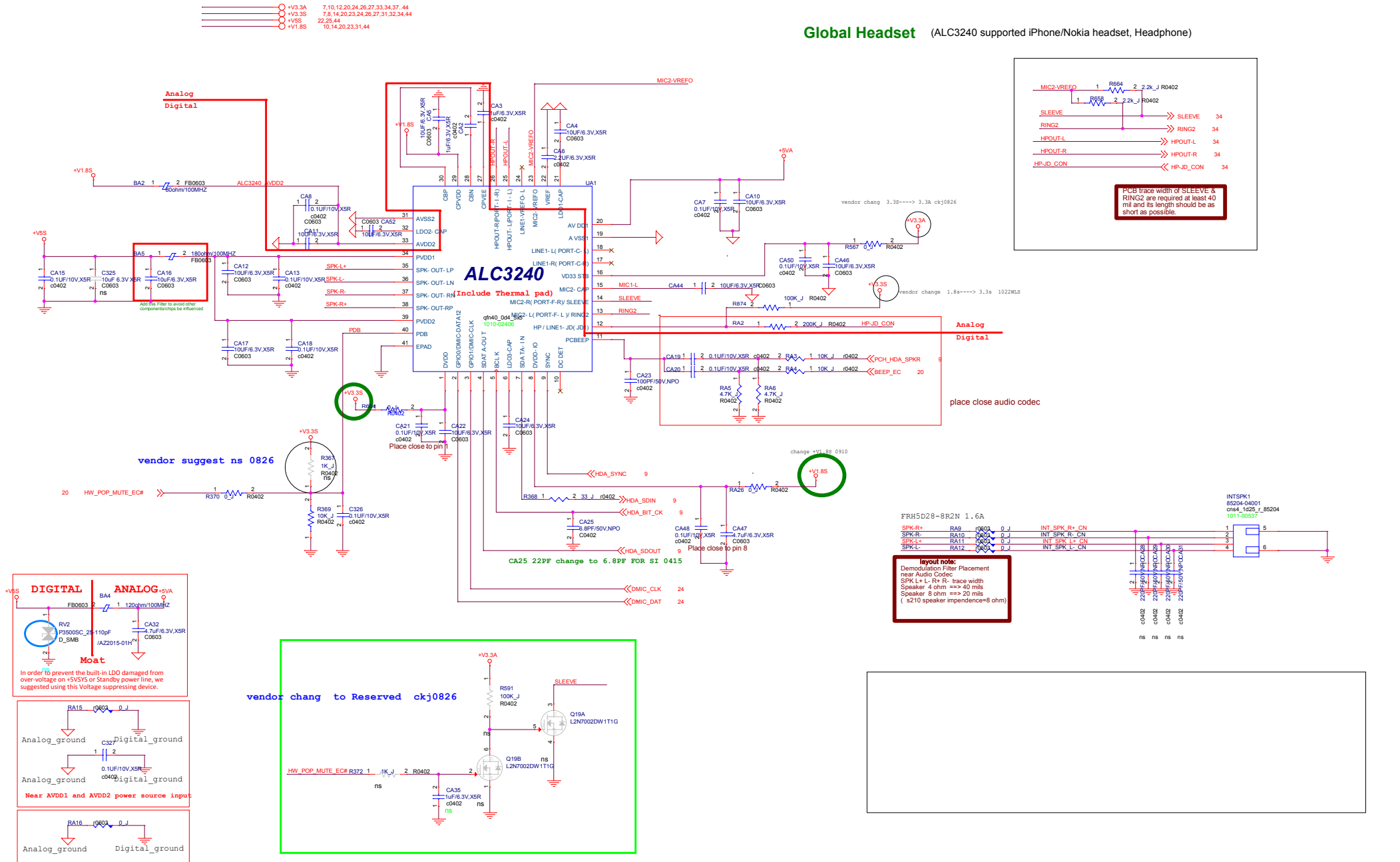
WLAN_+3_3V

R363 1M_J R0402 ns

Q18 2N7002LT1G sot23-3 ns

20,27 BT_ON 3 BT_DIABLE

Global Headset (ALC3240 supported iPhone/Nokia headset, Headphone)



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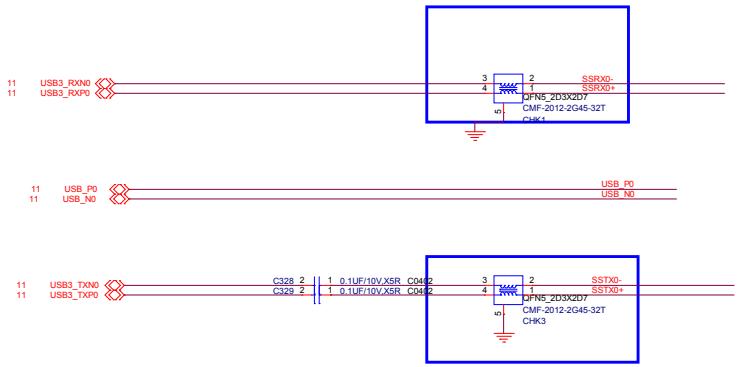
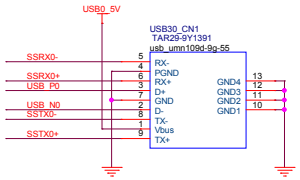
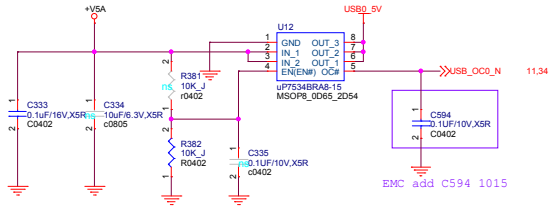
+V5A 30,34,37..44

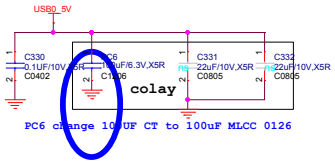
chk1 chk3 FOR EMI SIV 0122

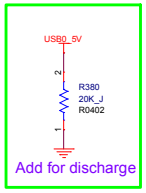


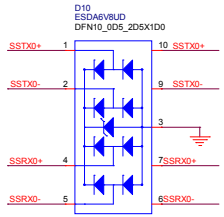


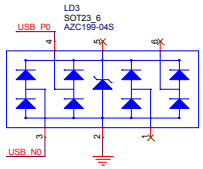
Intel recommends each USB3.0 slot be capable of supplying a minimum of 0.9 A











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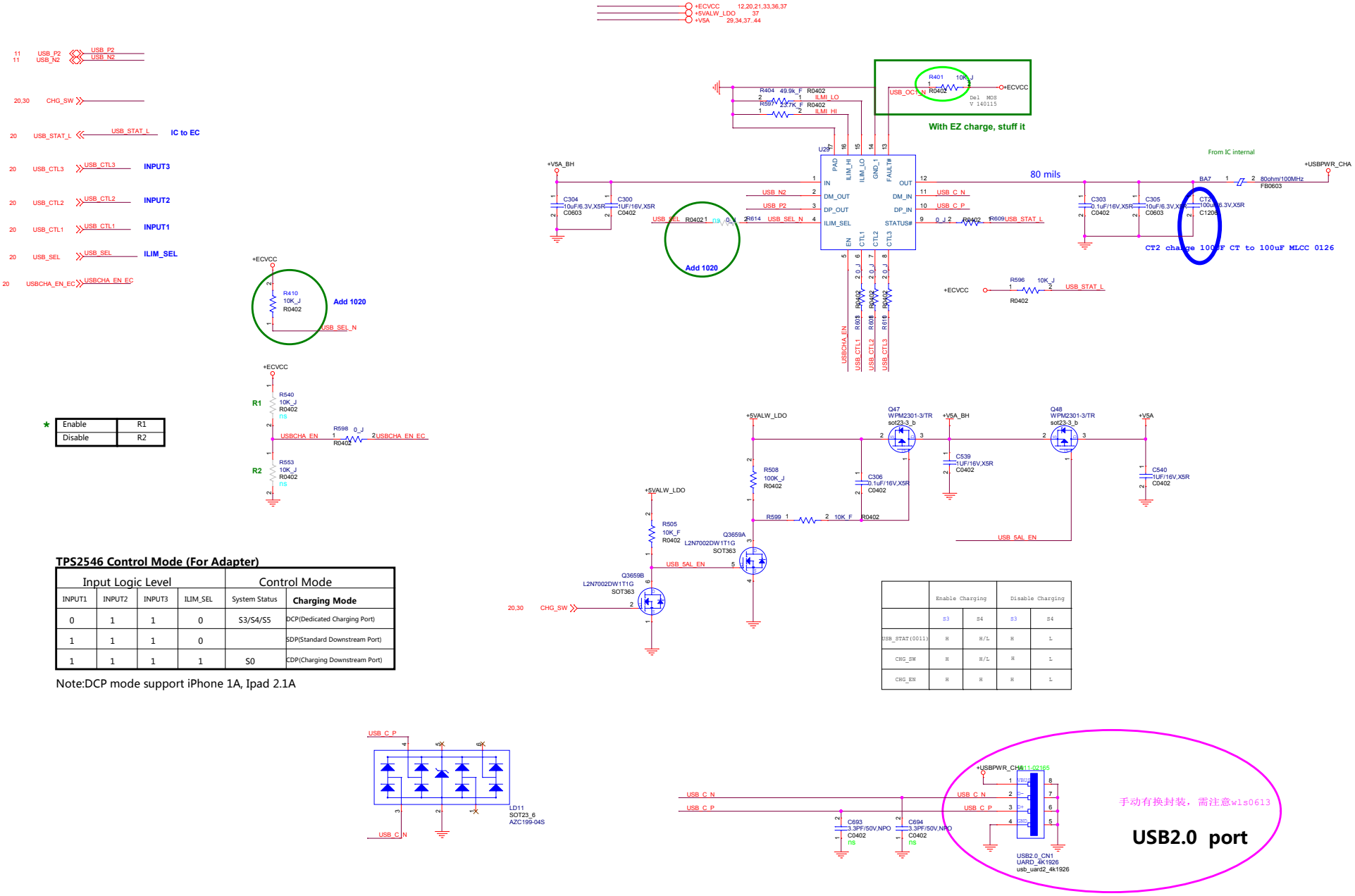

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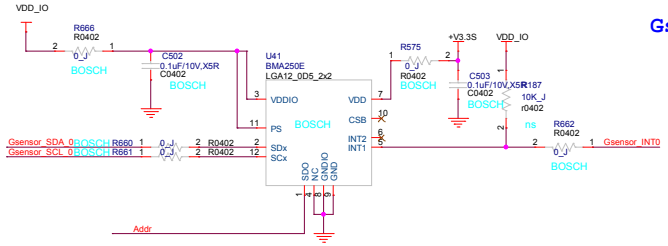
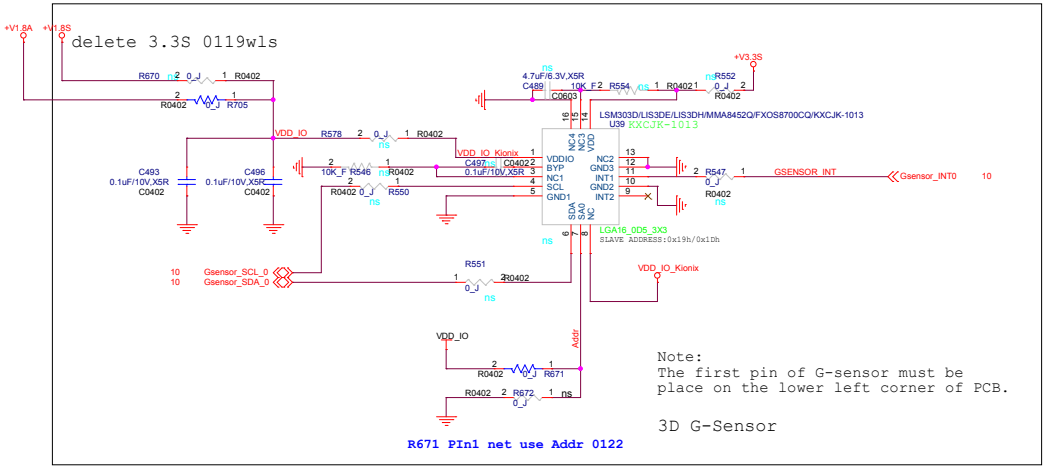
+V1.8S 10,14,20,23,28,44
+V3.3S 7,8,14,20,23,24,26..28,32,34,44
+V1.8A 7..12,14,16,20,23..25,27,39,44

Bosh G sensor change to 250E no part number 1010wls

Gsensor One





R671 PIn1 net use Addr 0122

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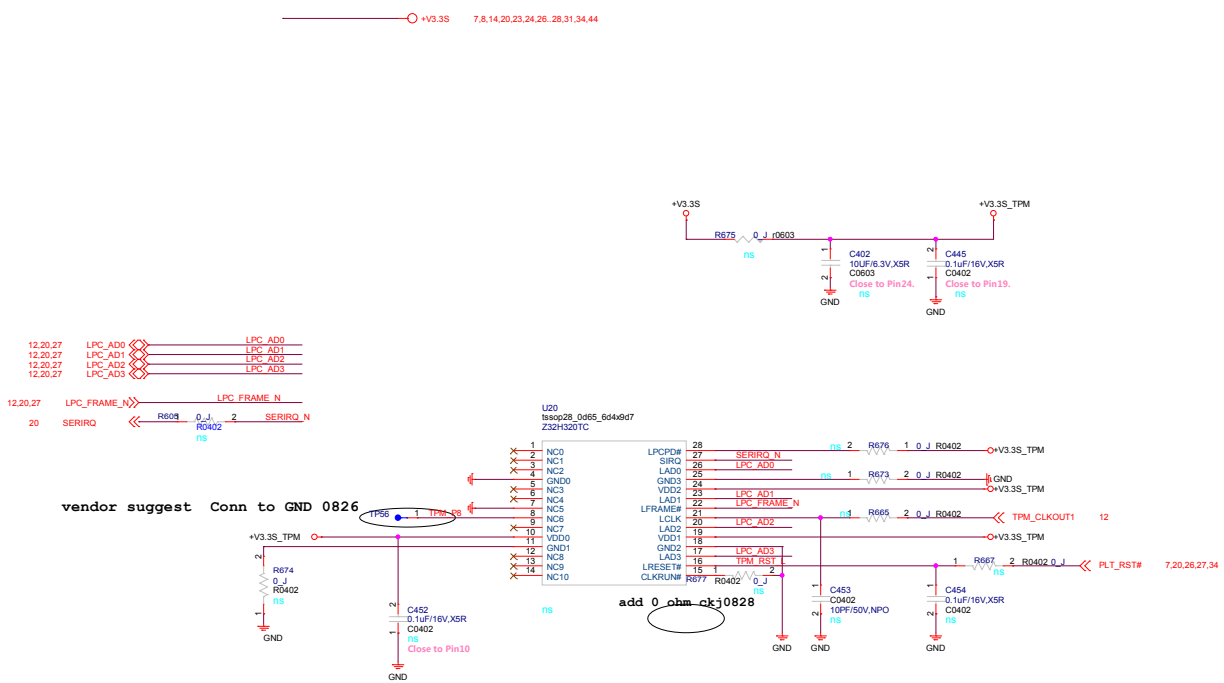

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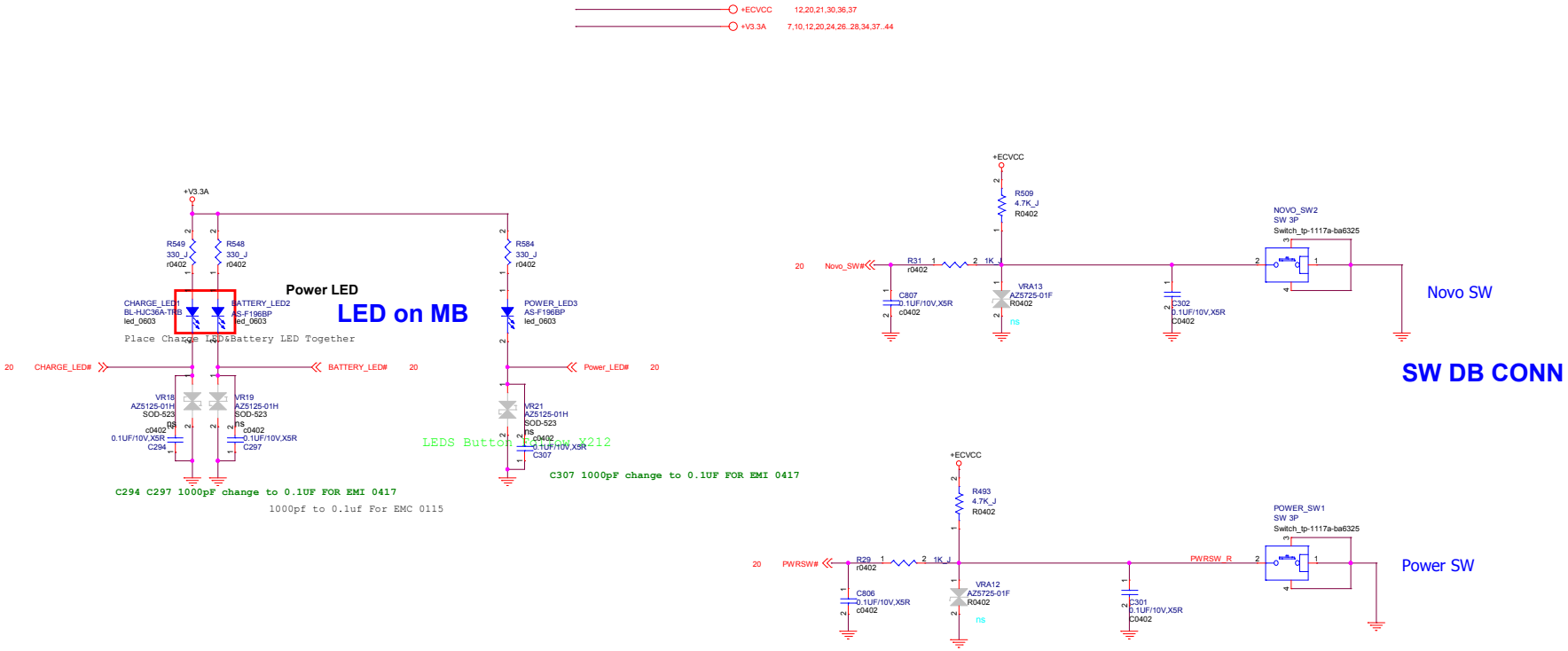

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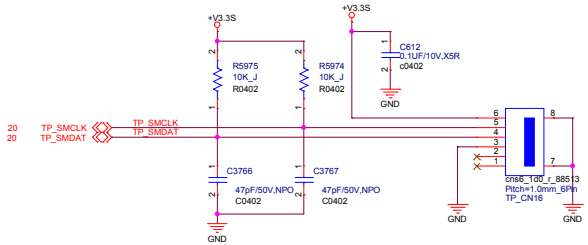
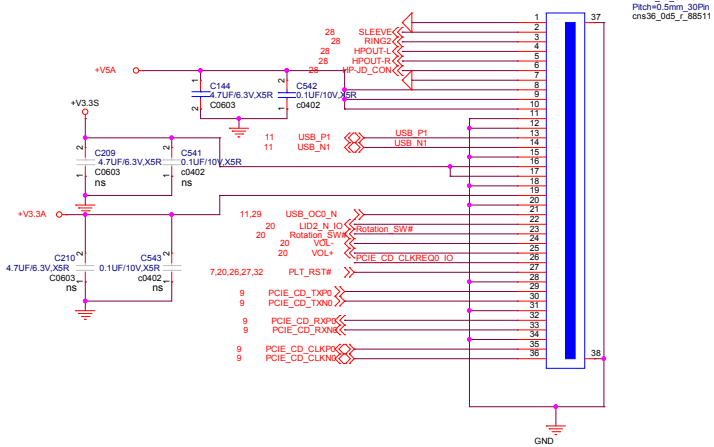
Tocuh pad



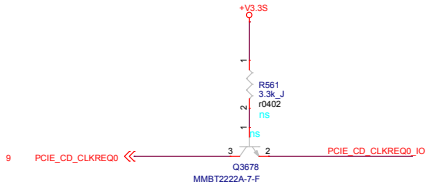
J1 Pin Assignments and Definitions

Pin Number	Pin Name	Description
1	VDD	Power Supply Voltage
2	PS2_CLK	PS/2 Clock
3	PS2_DATA	PS/2 Data
4	GND	Ground
5	SMBCLK	SMBus + Clock
6	SMBDAT	SMBus + Data

BM连接BH PIN顺序TBD



reserve LID2 to SOC



reserve Add Level_Shifter 1022

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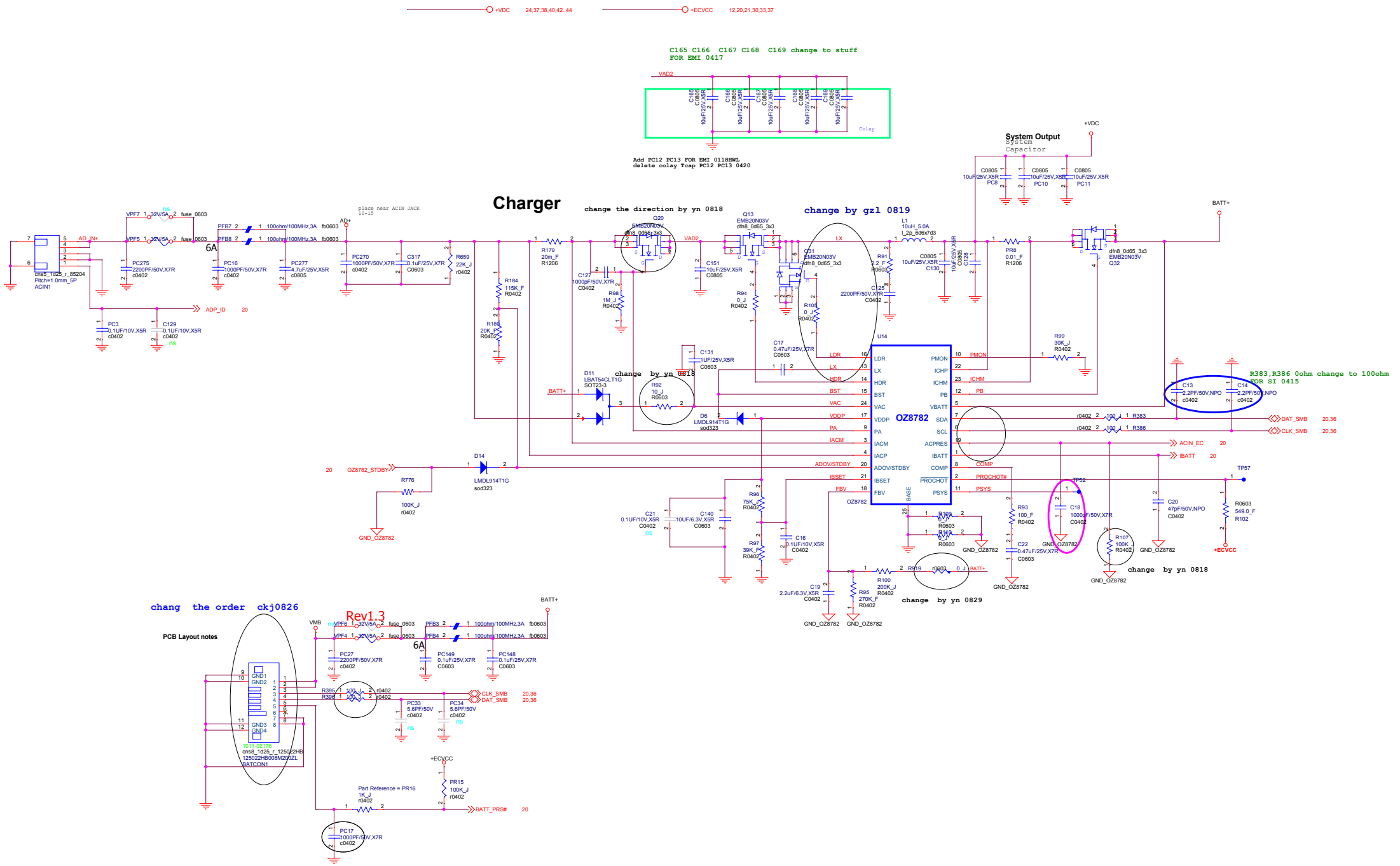

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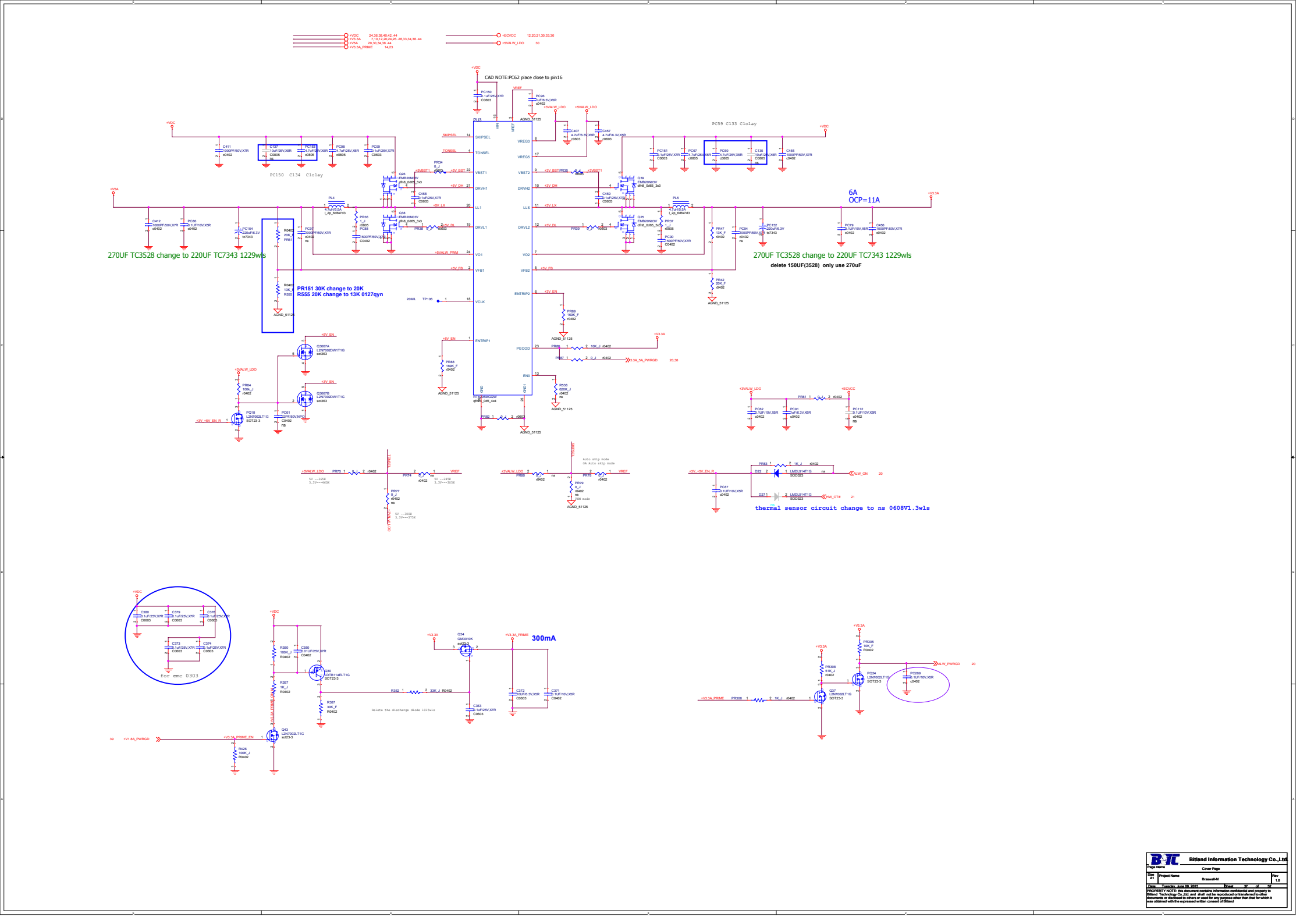
+VDC 24,36,38,40,42,44
+V3.3A 7,10,12,20,24,26,28,33,34,38,44
+V5A 29,30,34,38,44
+V3.3A_PRIME 14,23
+ECVCC 12,20,21,30,33,36
+5VALW_LDO 30
CAD NOTE:PC62 place close to pin16
PC59 C133 Clolay
PC150 C134 Clolay
6A
OCP=11A
270UF TC3528 change to 220UF TC7343 1229wls
270UF TC3528 change to 220UF TC7343 1229wls
delete 150UF(3528) only use 270uF
PR151 30K change to 20K
R555 20K change to 13K 0127qyn
thermal sensor circuit change to ns 0608V1.3wls
300mA
for emc 0303
Delete the discharge diode 1015wls
Auto skip mode
OA Auto skip mode
PWM mode
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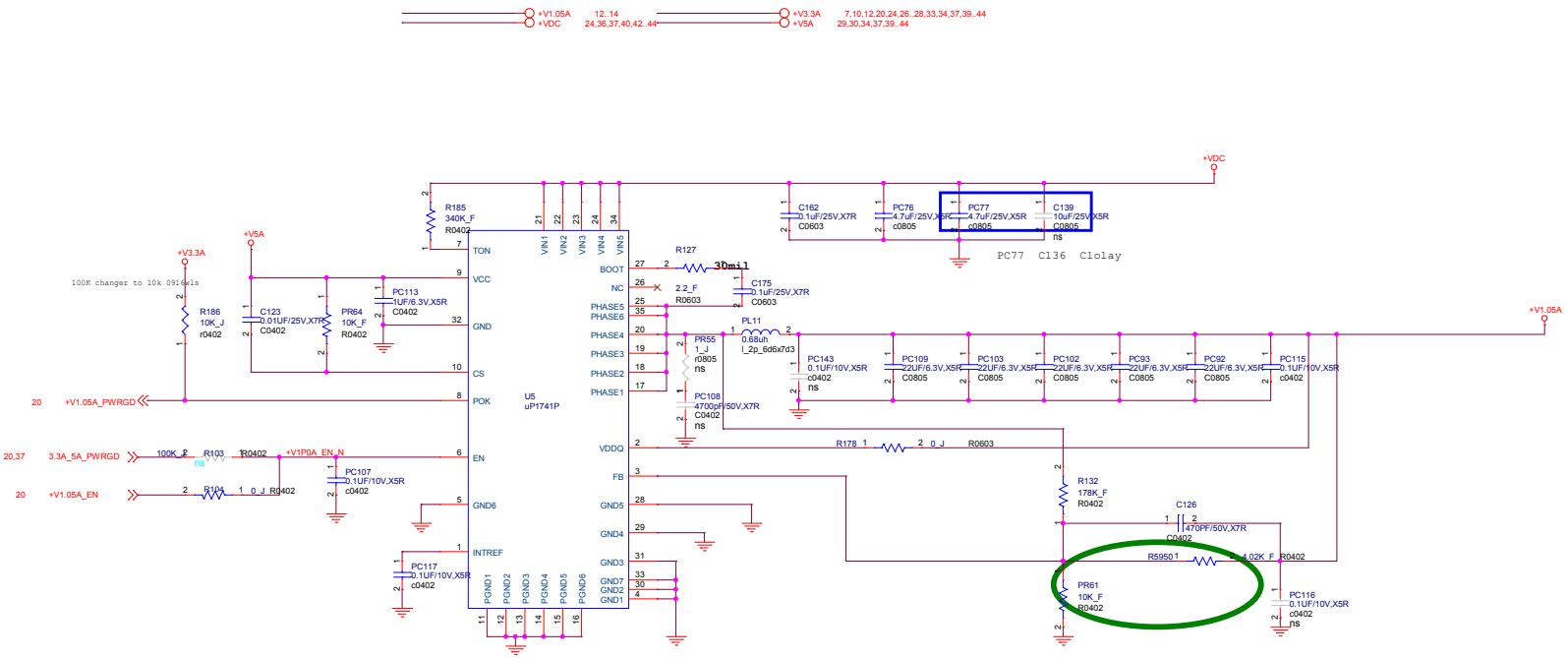

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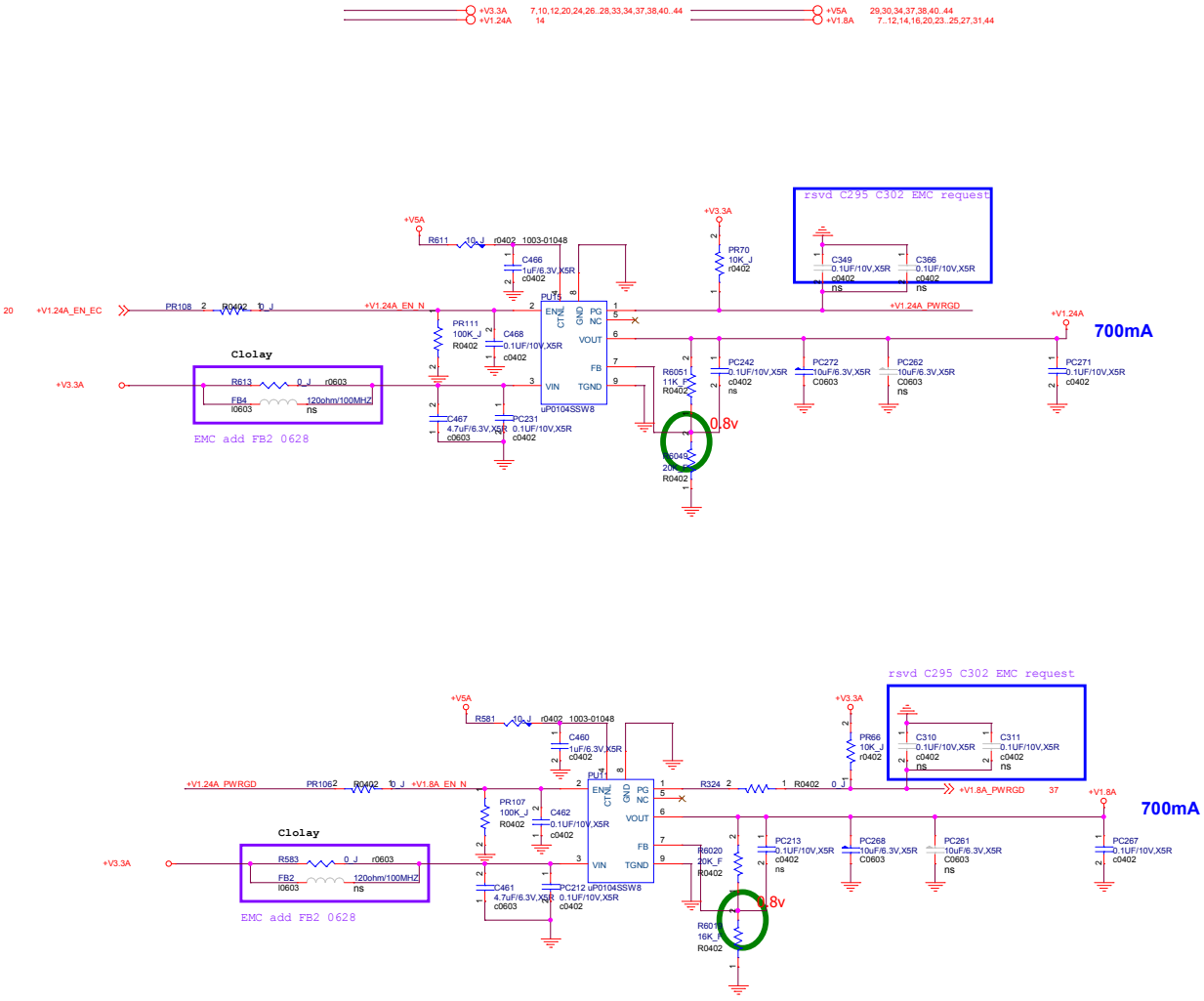

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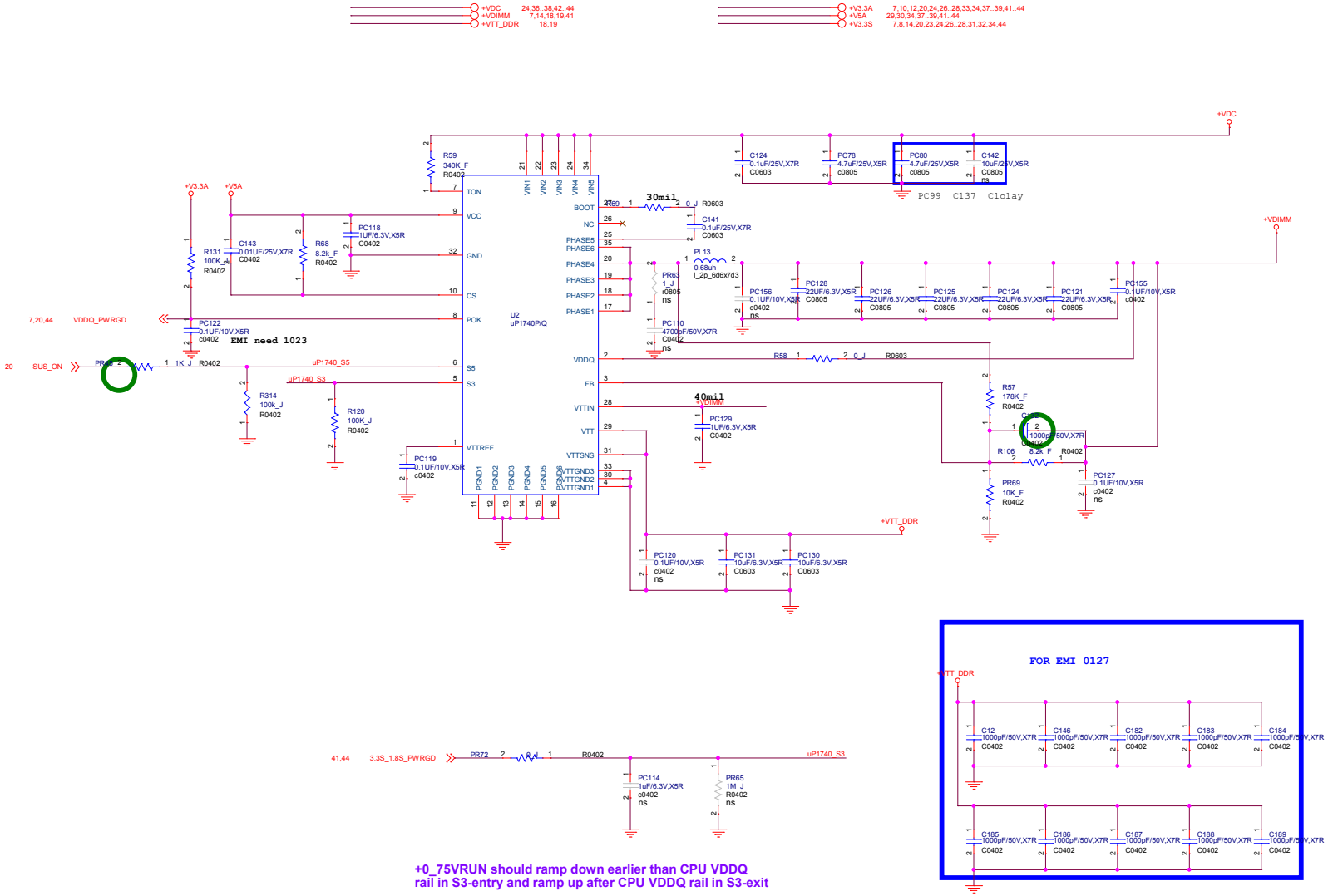

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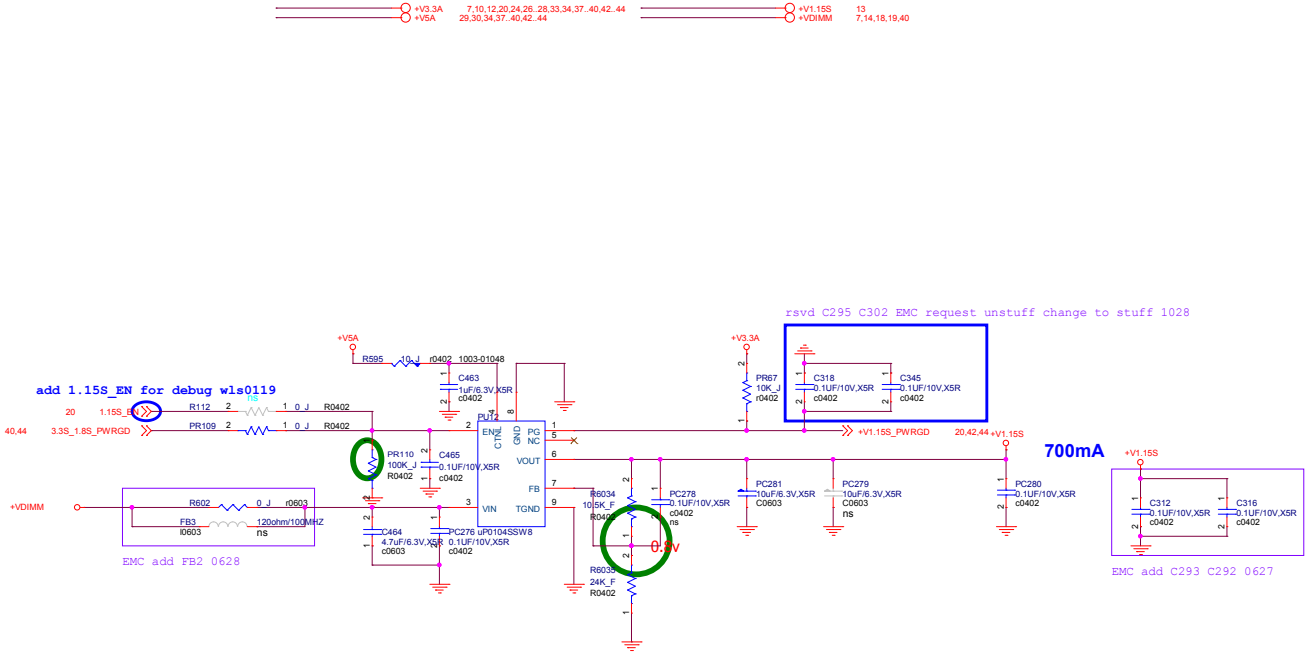

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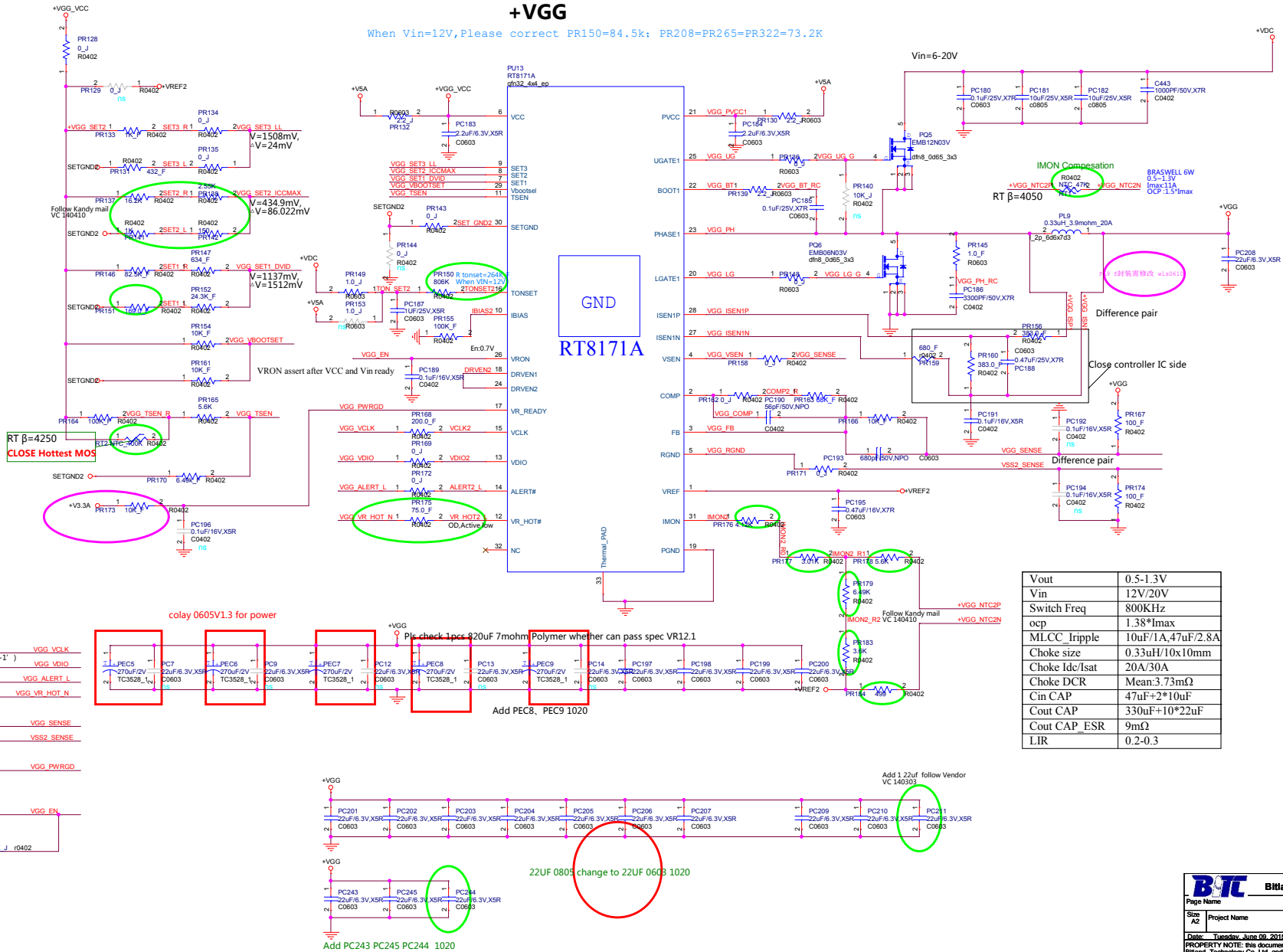
+VGG

When Vin=12V,Please correct PR150=84.5k; PR208=PR265=PR322=73.2K



Vout	0.5-1.3V
Vin	12V/20V
Switch Freq	800KHz
ocp	1.38*Imax
MLCC_Iripple	10uF/1A,47uF/2.8A
Choke size	0.33uH/10x10mm
Choke Idc/Isat	20A/30A
Choke DCR	Mean:3.73mΩ
Cin CAP	47uF+2*10uF
Cout CAP	330uF+10*22uF
Cout CAP_ESR	9mΩ
LIR	0.2-0.3

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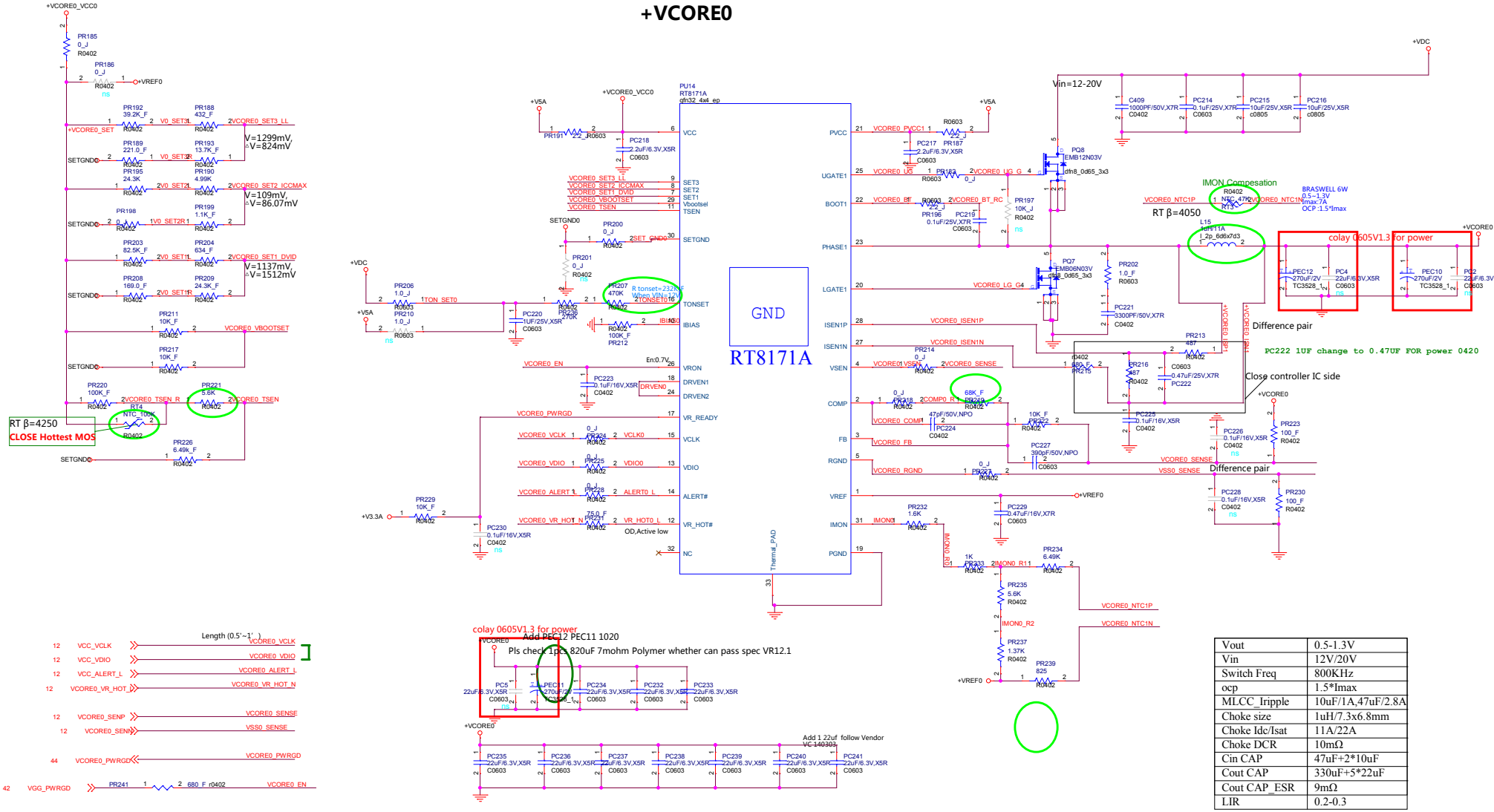
+VCORE0



Vout	0.5-1.3V
Vin	12V/20V
Switch Freq	800KHz
ocp	1.5*Imax
MLCC_Iripple	10uF/1A,47uF/2.8A
Choke size	1uH/7.3x6.8mm
Choke Idc/Isat	11A/22A
Choke DCR	10mΩ
Cin CAP	47uF+2*10uF
Cout CAP	330uF+5*22uF
Cout CAP_ESR	9mΩ
LIR	0.2-0.3

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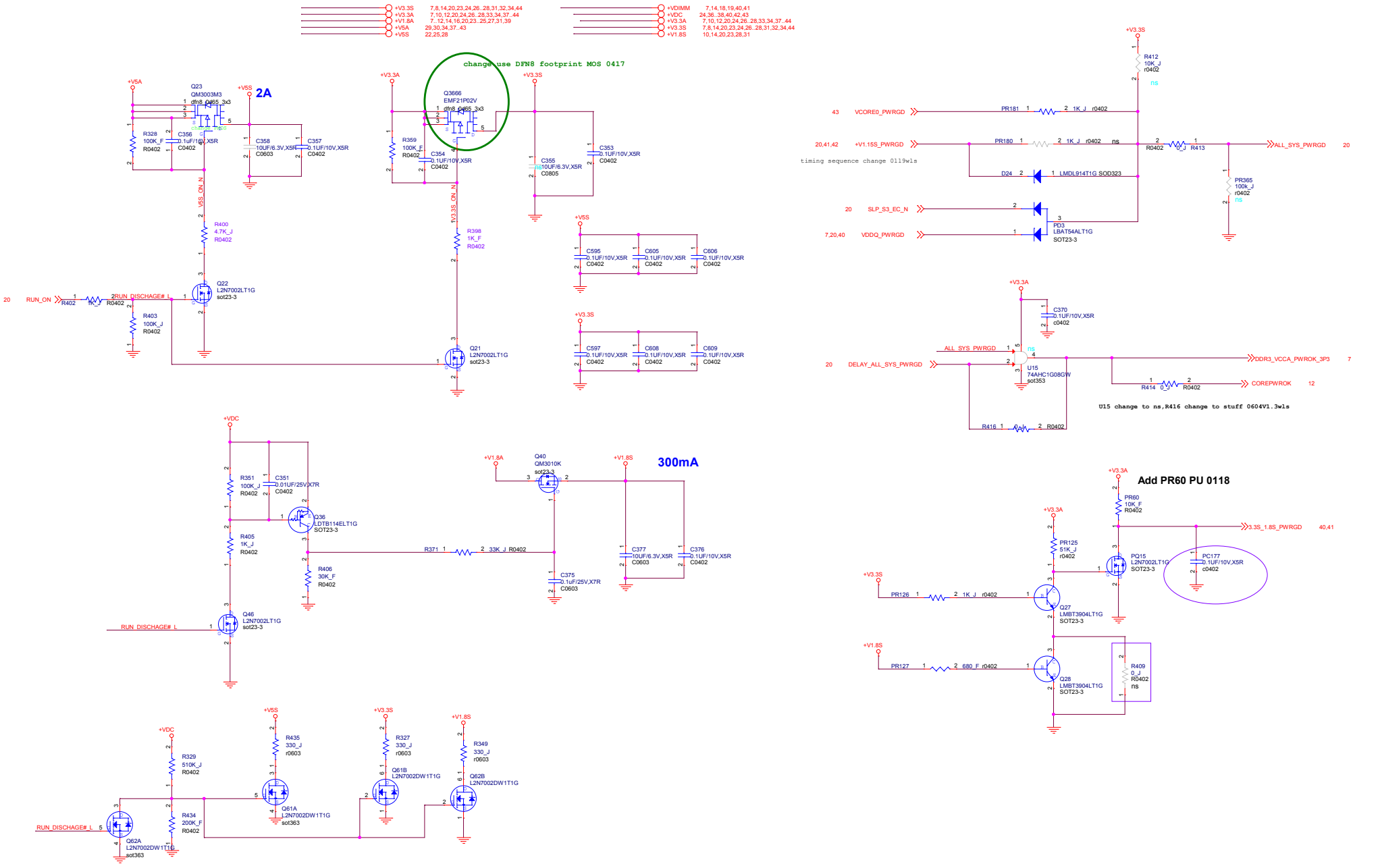

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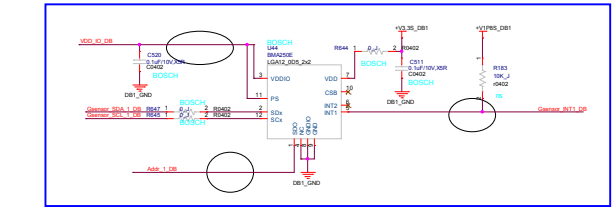
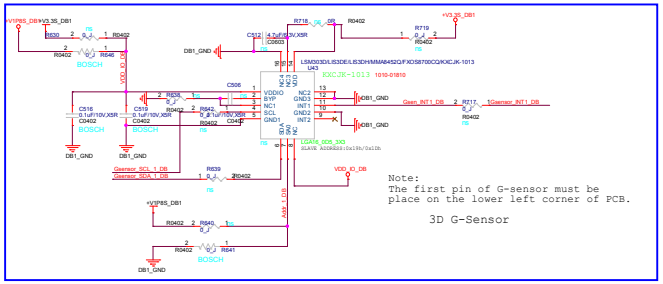
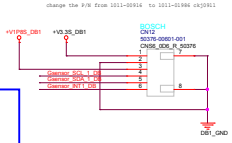
Gsensor Two







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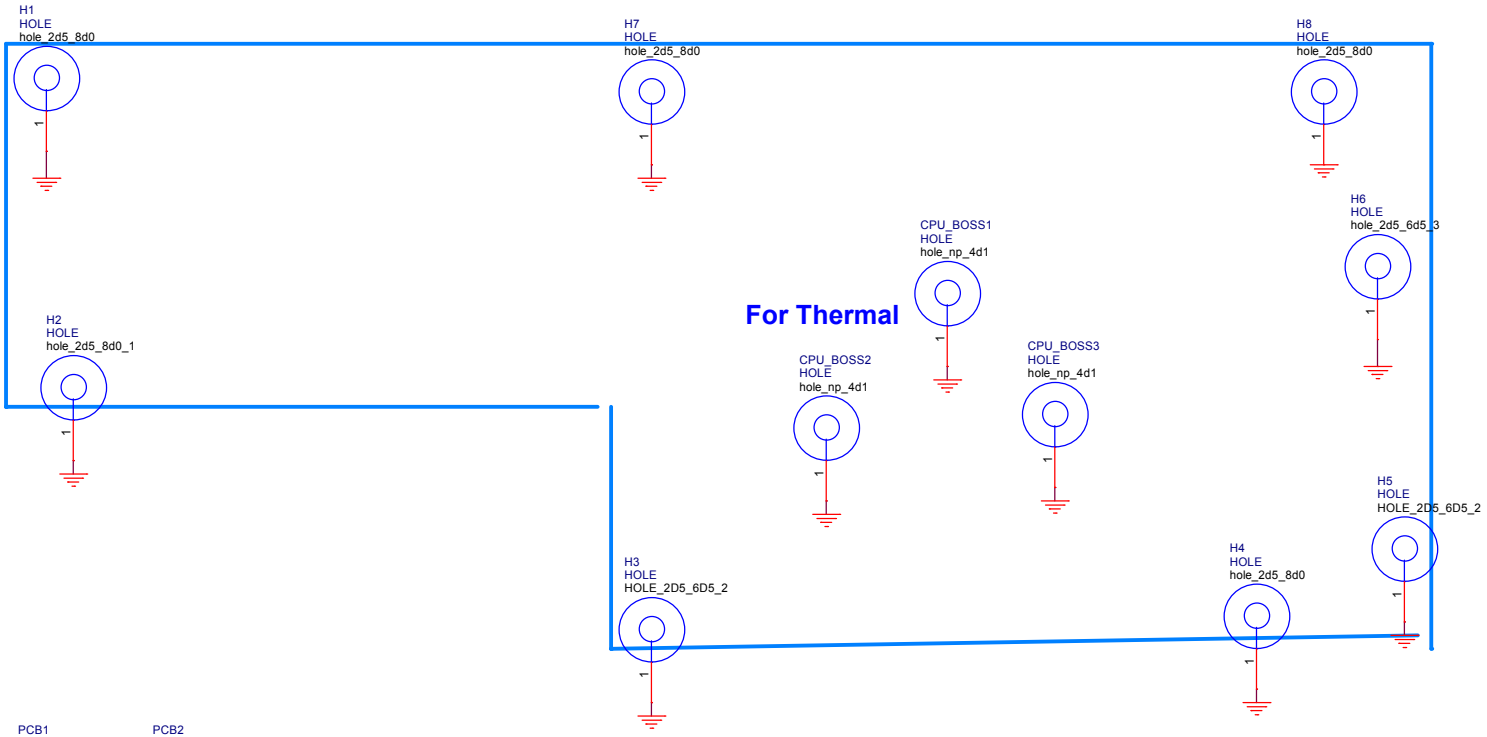

PCB1
MB
BM5334
PCB PN

PCB2
MB
BM5334
PCB PN

SW1
EC code
BIOS PN

SW2
BIOS code
EC PN

WHITE BARCODE1
WHITE
1301-02021

MK1 FMARKS fmarks ns
MK2 FMARKS fmarks ns
MK3 FMARKS fmarks ns
MK4 FMARKS fmarks ns
MK5 FMARKS fmarks ns
MK6 FMARKS fmarks ns
MK7 FMARKS fmarks ns
MK8 FMARKS fmarks ns

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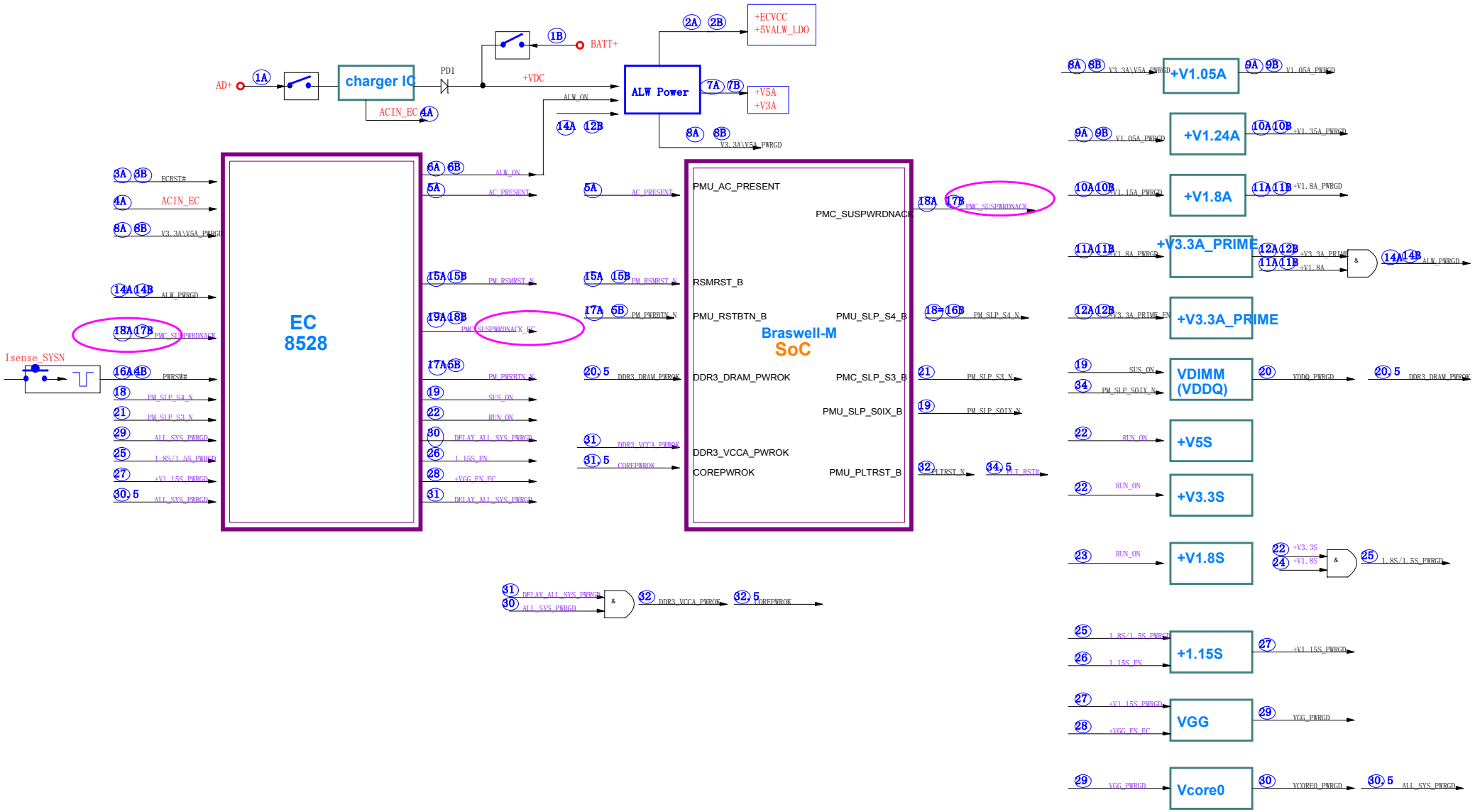

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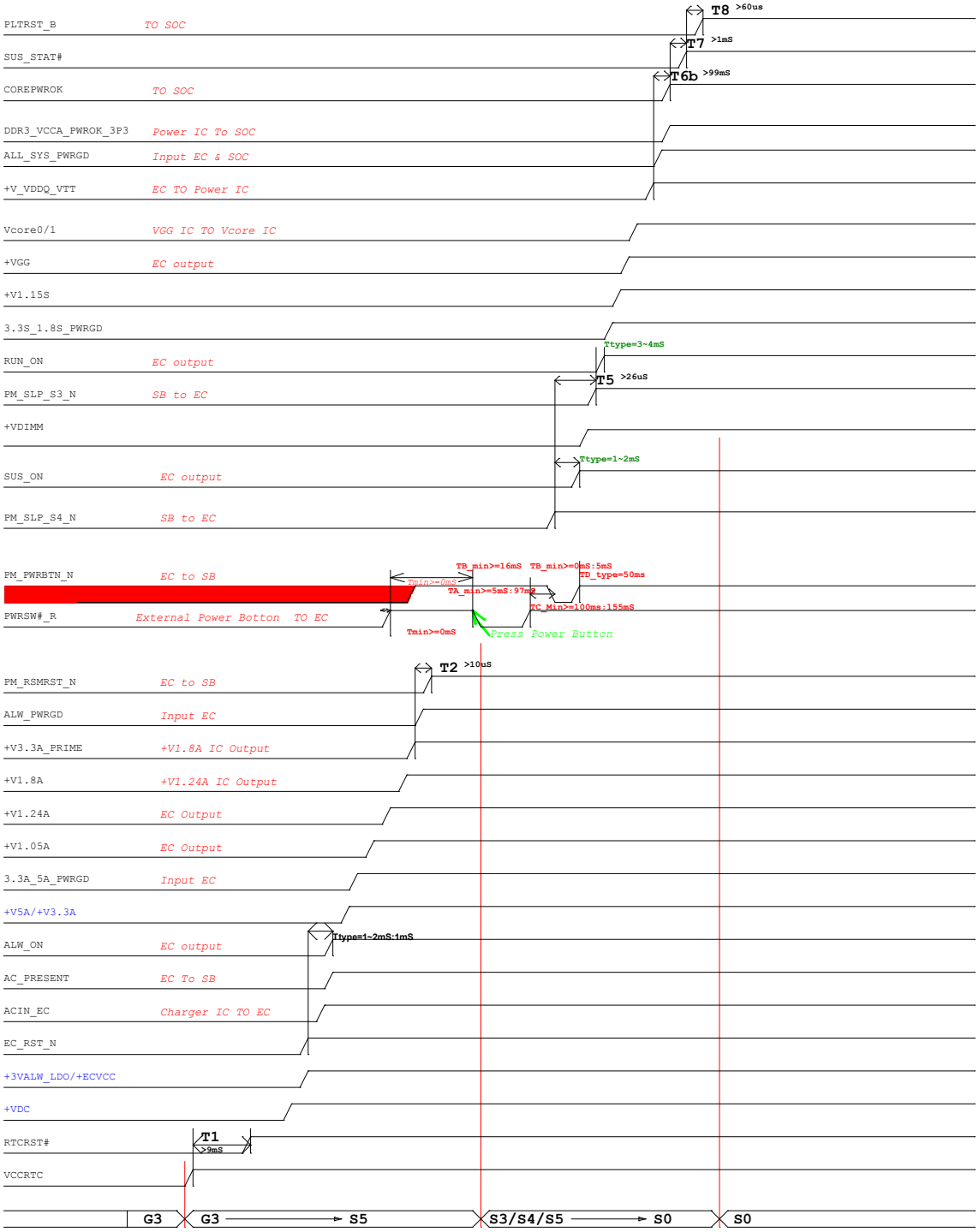
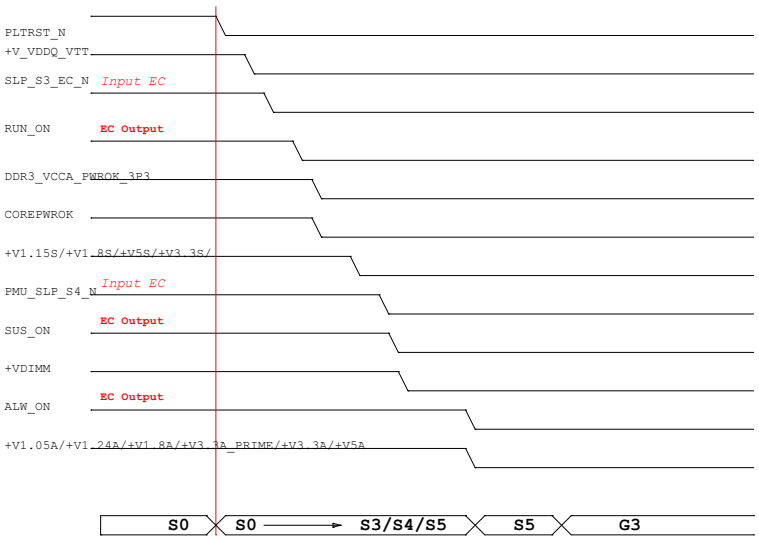
Power On/Off Sequence Specification(Adapter Mode) G3-S5-S4-S3-S0





条纹填充区域表示在这段时间任意一个时间点达到要求电平都OK

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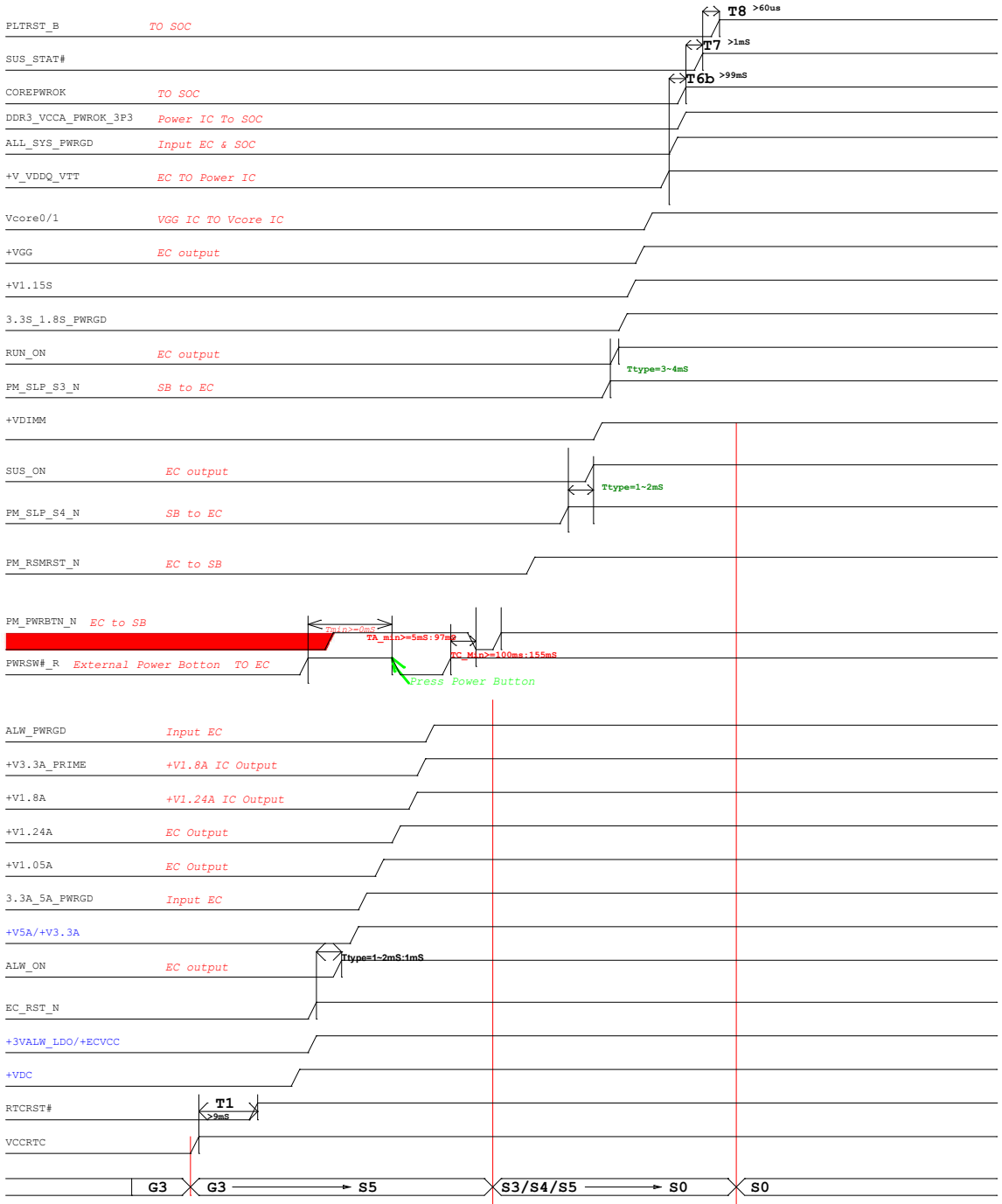
Power On/Off Sequence Specification(Battery Mode) G3-S5-S4-S3-S0



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Change History

Version	Notes	Date
V1.0	Initial release	2014.10.11
V1.1	SIV	
V1.2	SIT	
V1.3	SVT	

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