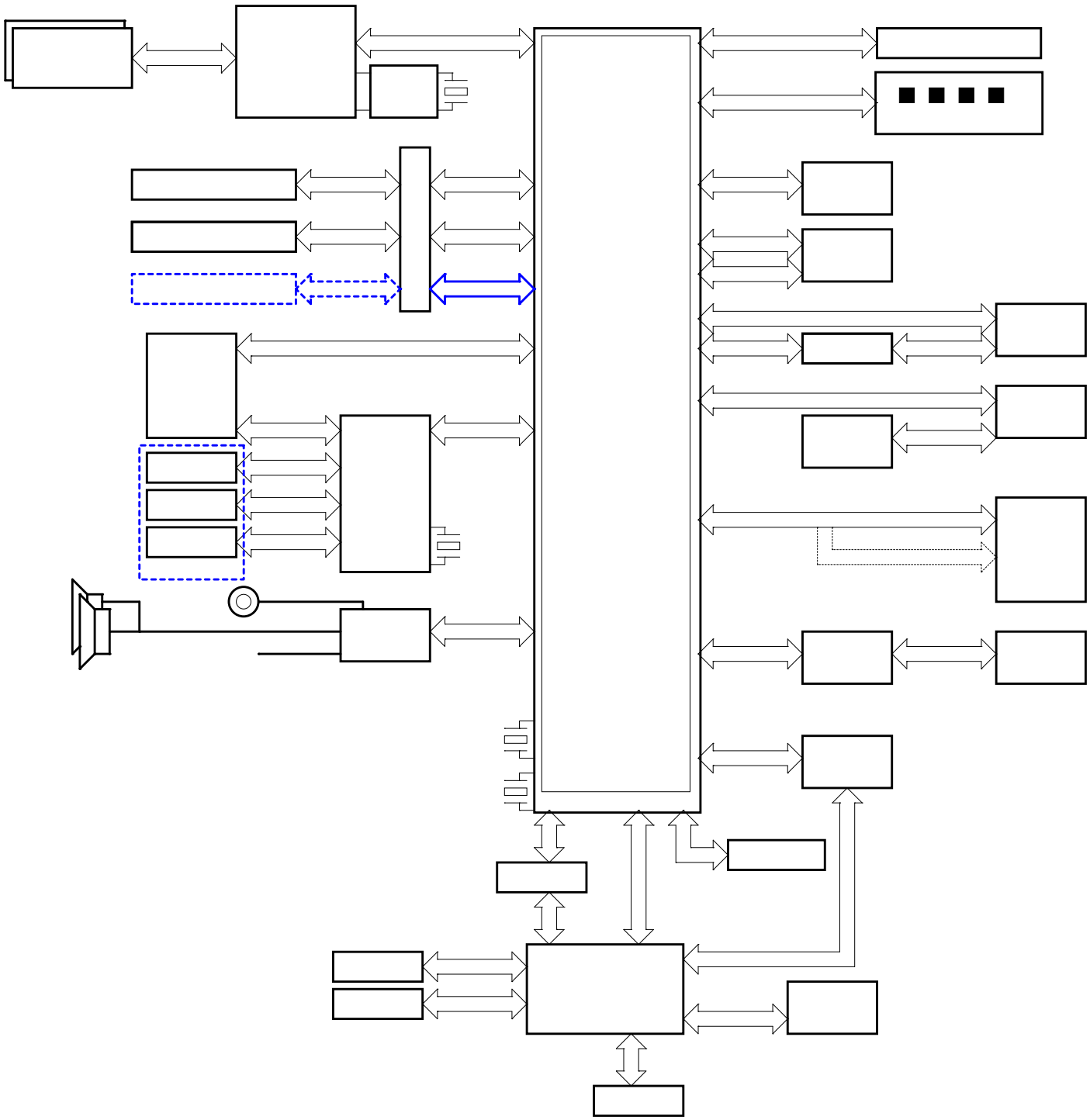
Strongbow_PK

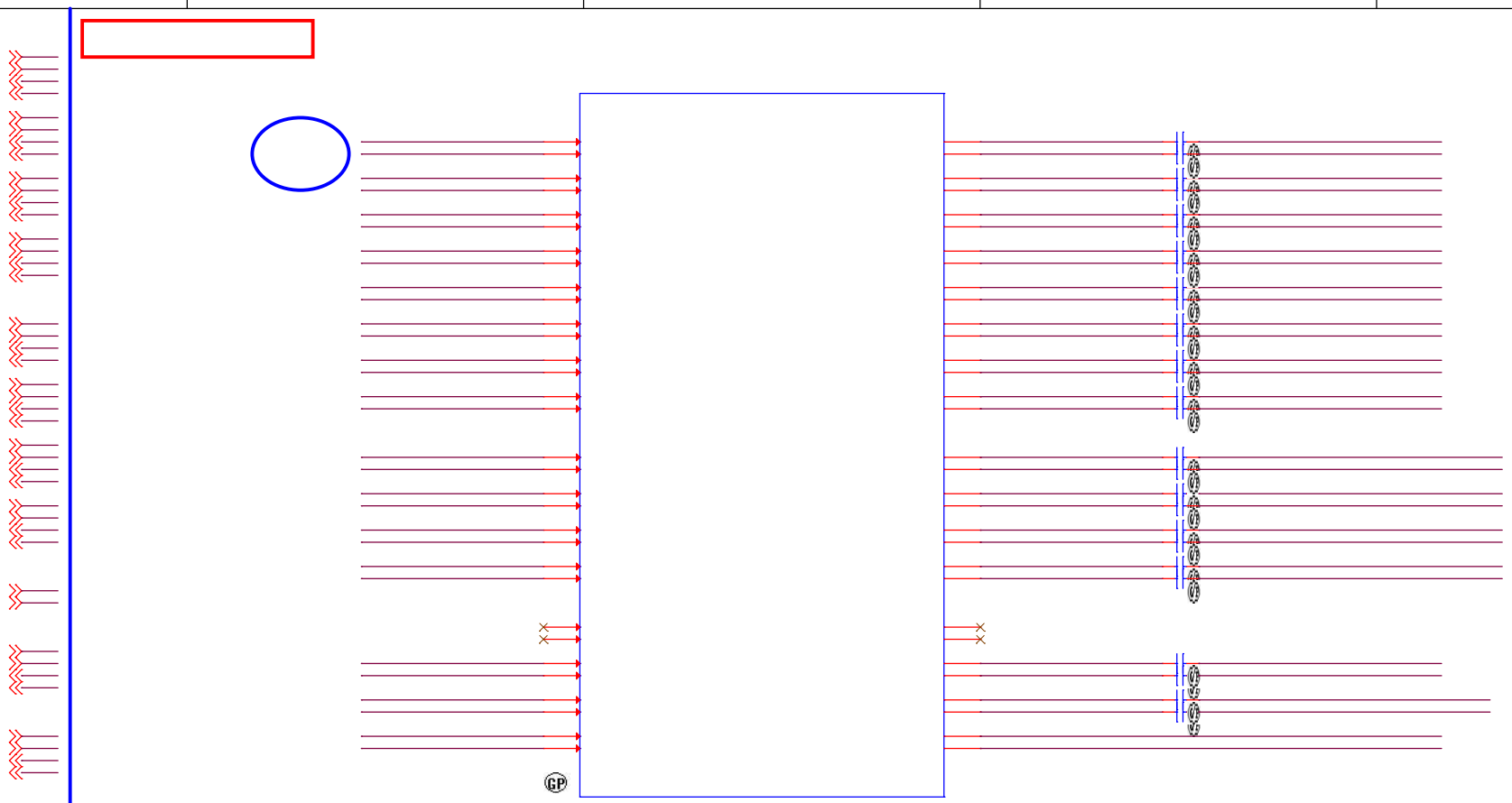
Schematics Document

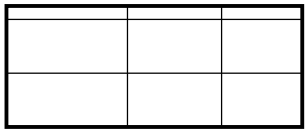
DY : None Installed
UMA: UMA only Installed
PX: DISCRTE OPTIMUS Installed

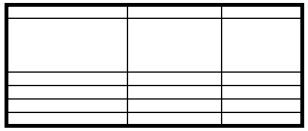
緯創資通



緯創資通







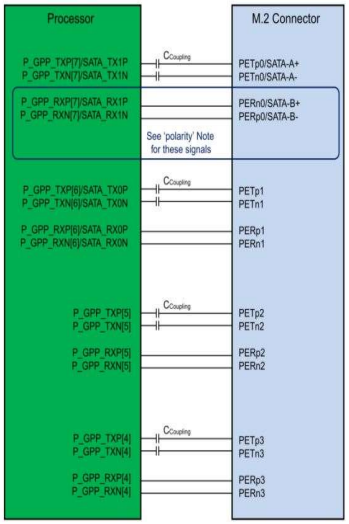


Figure 53. Block Diagram—PCI Express® and SATA to M.2 Connector (PCIe SSDs and SATA SSDs Supported)

緯創資通

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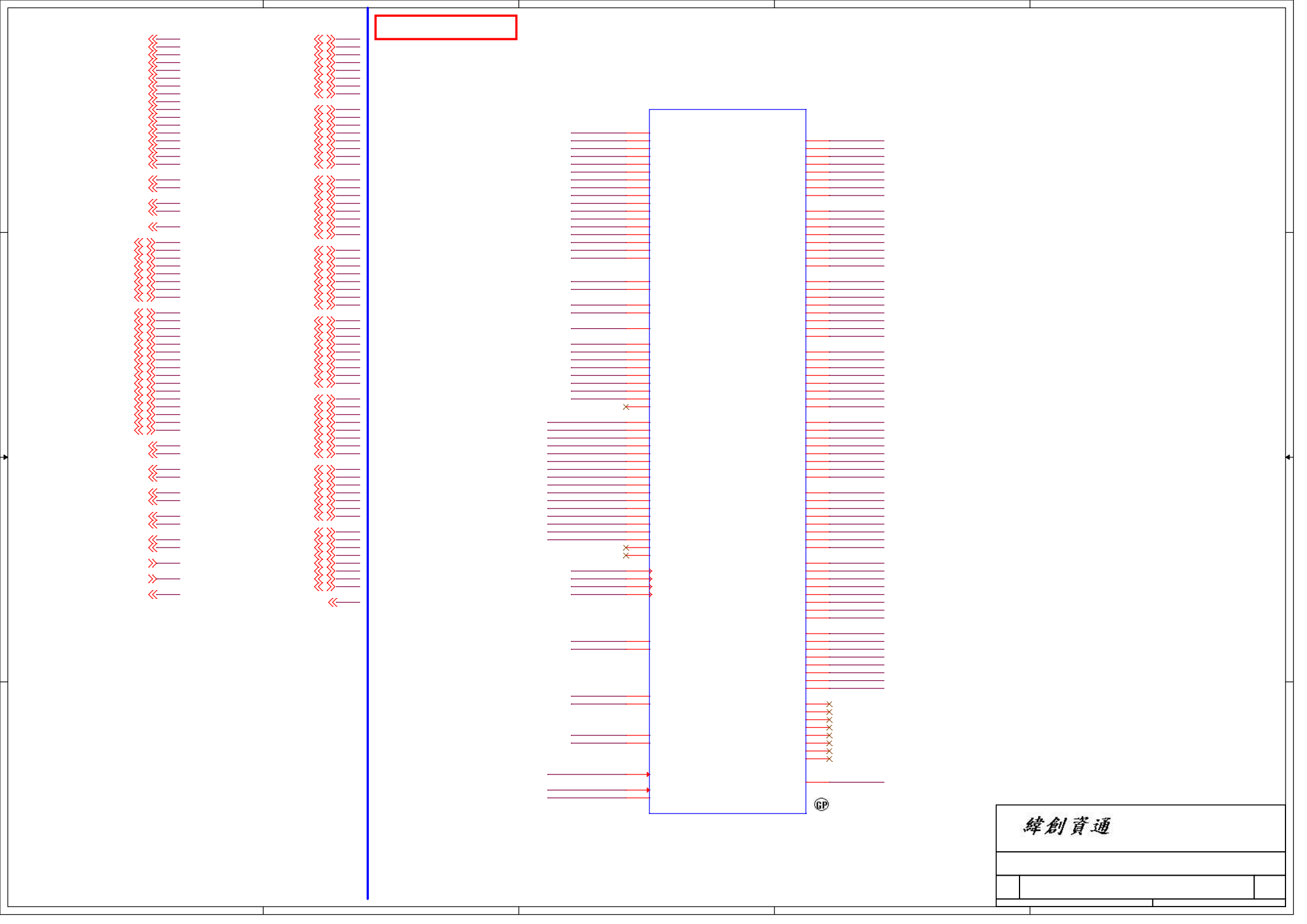
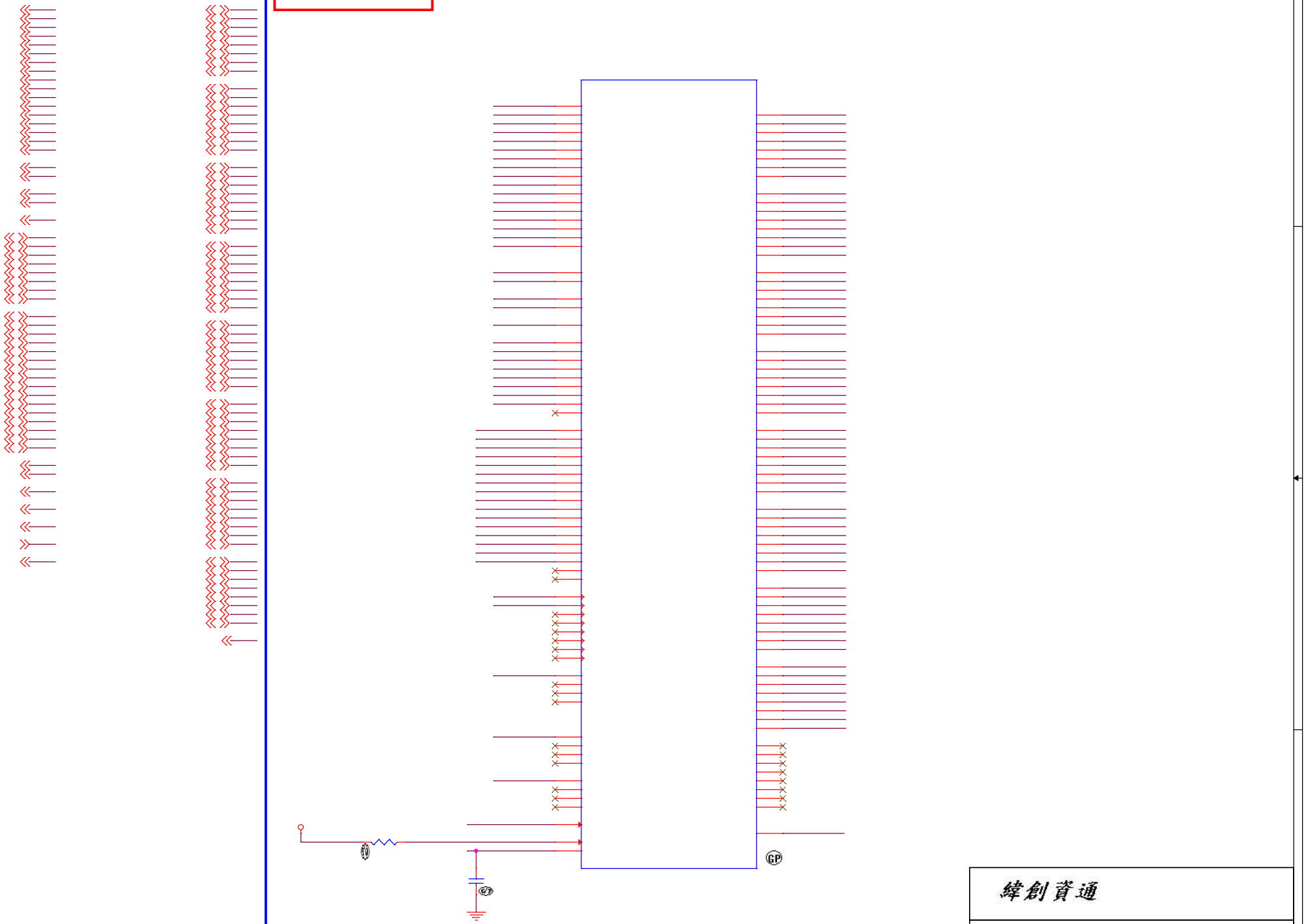
緯創資通



緯創資通



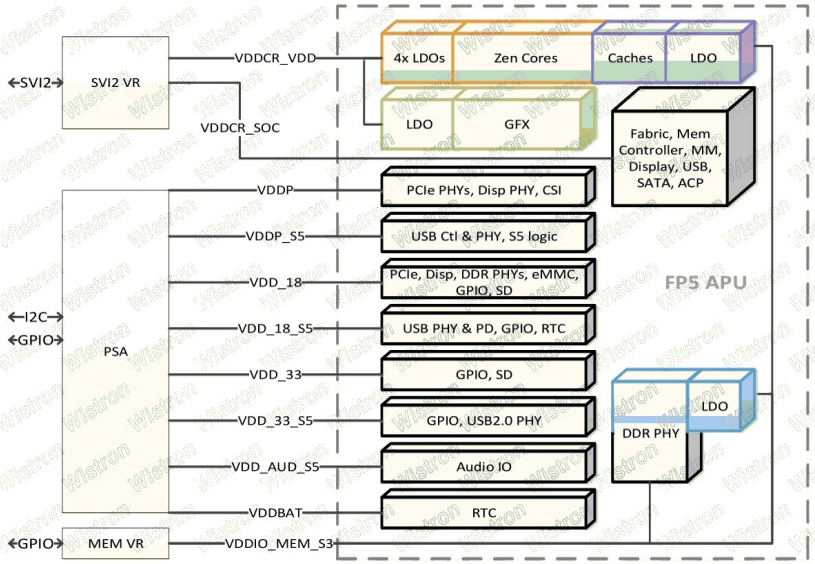
緯創資通

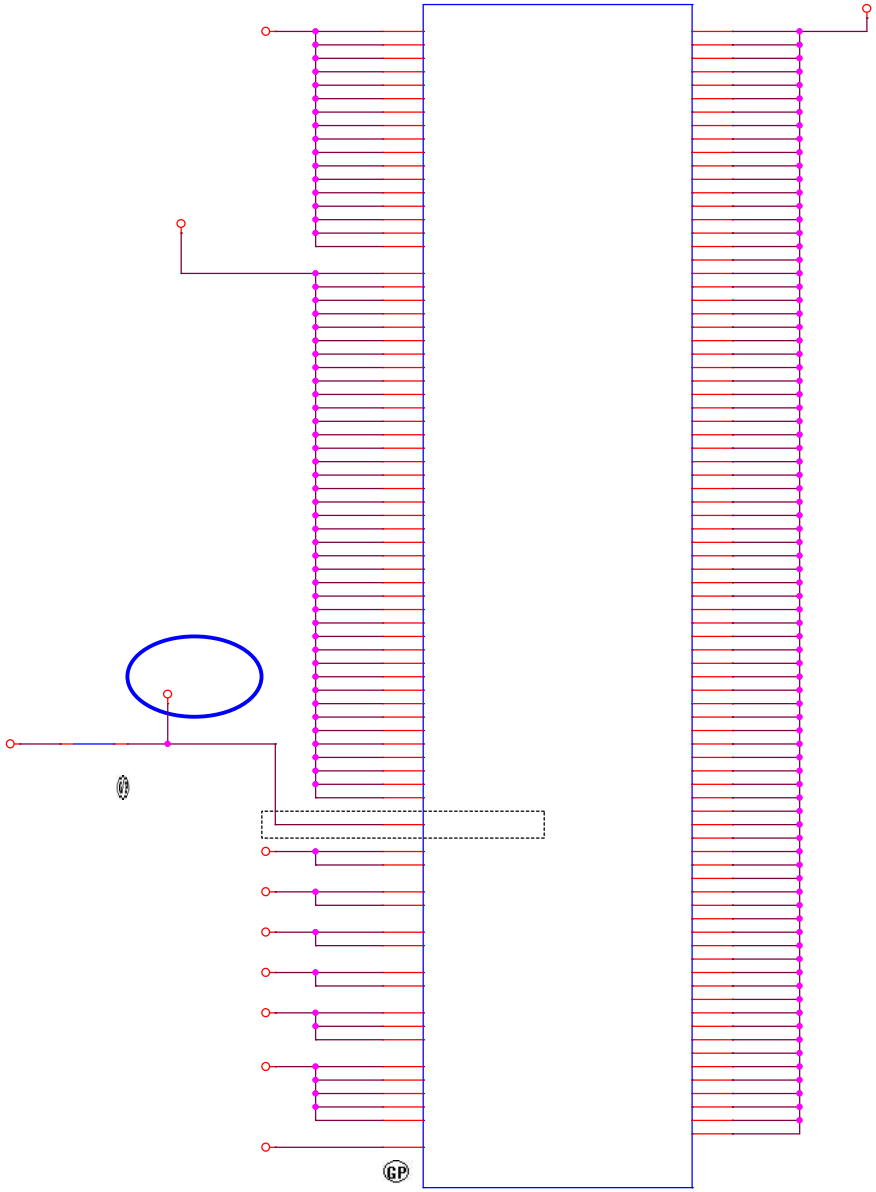
SVI	FP4 – Bristol Ridge	FP5 – Raven Ridge
Supply 1	VDDCR_CPU – x86 Cores	VDDCR_VDD – x86 Cores, GPU
Supply 2	VDDCR_NB – Rest Of Chip	VDDCR_SOC – Rest Of Chip
Supply 3	VDDCR_GFX – GPU	N/A
Sum@15W	TDC: 56A, EDC: 87A	TDC: 45A, EDC: 58A

Table 5. FP5 Processor Voltage Supply Currents

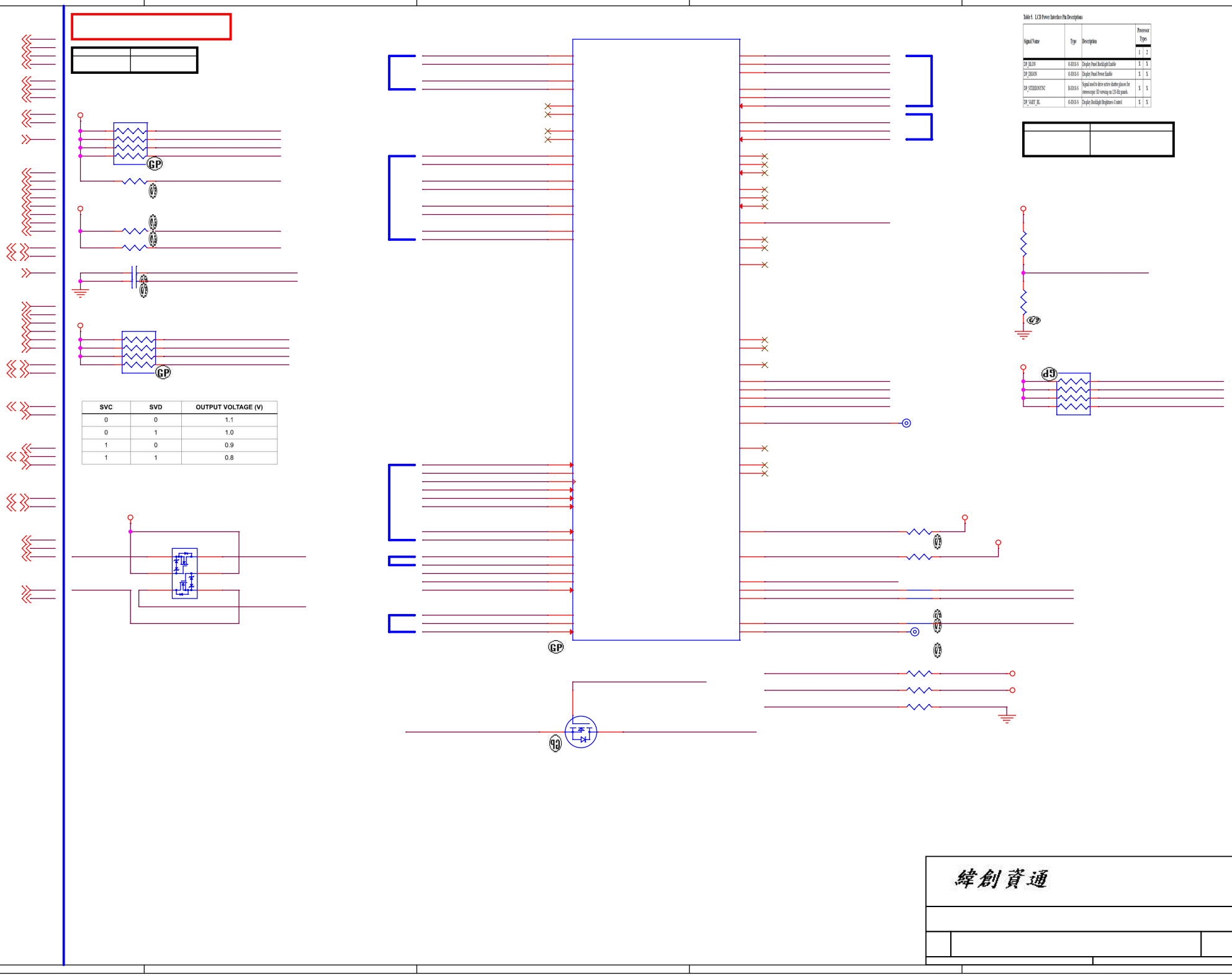
Supply [1]	Nominal Voltage at Pkg Ball (V) [2]	Condition	SYSTEM_CONFIGURATION 1 12W	2 15W	3 25W	4 35W	5 45W	6 54W
VDDCR_VDD	Variable (0.65–TBD)[5]	TDC [3]	29	35		53	65	
		EDC	38	45		70	85	
		Max Loadstep [4]	35	35		56	68	
VDDCR_SOC	Variable (0.72–TBD)[5]	TDC [3]	10					
		EDC	13					
		Max Loadstep [4]	10					
VDDIO_MEM_S3	1.20	TDC	6.00					
VDDP[6]	0.80	TDC	4.00					
	0.90	TDC	4.00					
VDDP_S5[6,7]	0.80	TDC	1.00					
	0.90	TDC	1.00					
VDD_18	1.80	TDC	2.00					
VDD_18_S5	1.80	TDC	0.50					
VDD_33	3.30	TDC	0.25					
VDD_33_S5	3.30	TDC	0.25					
VDDIO_AUDIO	1.20	TDC	0.20					
	1.50	TDC	0.20					
	1.80	TDC	0.20					
VDDBT_RTC_G	1.50	TDC	4.5µA					

RAVEN RIDGE FP5 POWER DELIVERY





緯創資通

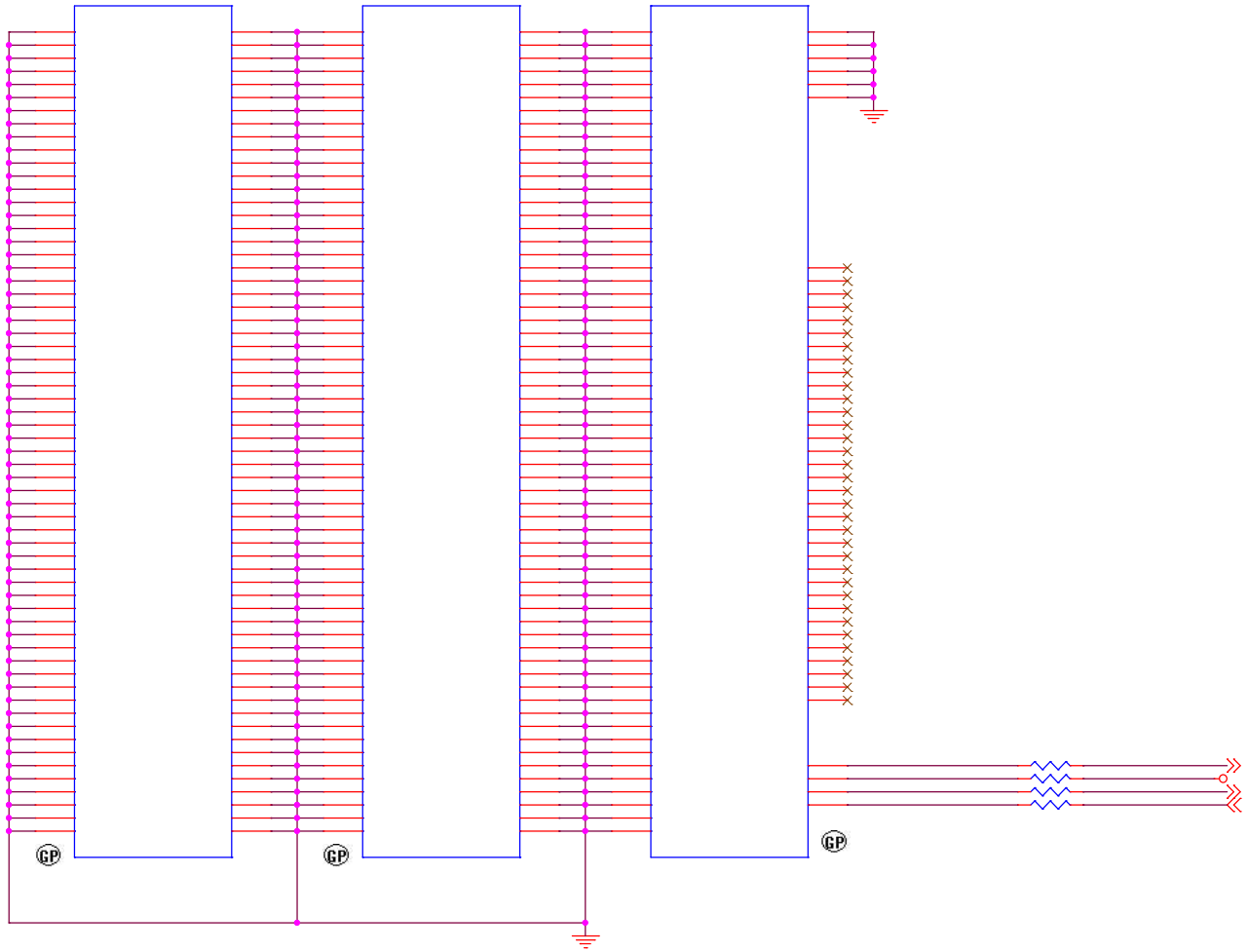


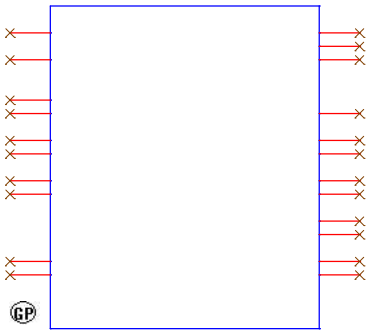
SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

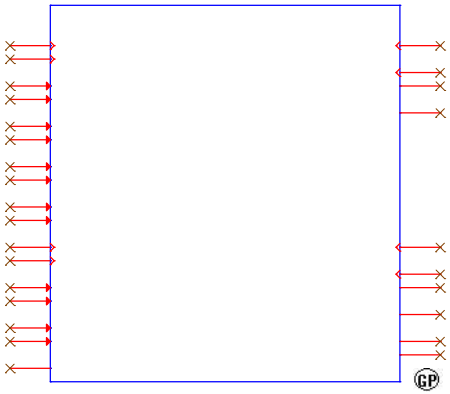
Table 6. LCD Power Interface Pin Descriptions

Signal Name	Type	Description	Processor Types	
			1	2
DP_BLON	O,3V3,S	Display Panel Backlight Enable	X	X
DP_DIGON	O,3V3,S	Display Panel Power Enable	X	X
DP_STEREOSYNC	B,3V3,S	Signal used to drive active shutter glasses for stereoscopic 3D viewing on 120 Hz panels.	X	X
DP_VARY_BL	O,3V3,S	Display Backlight Brightness Control	X	X

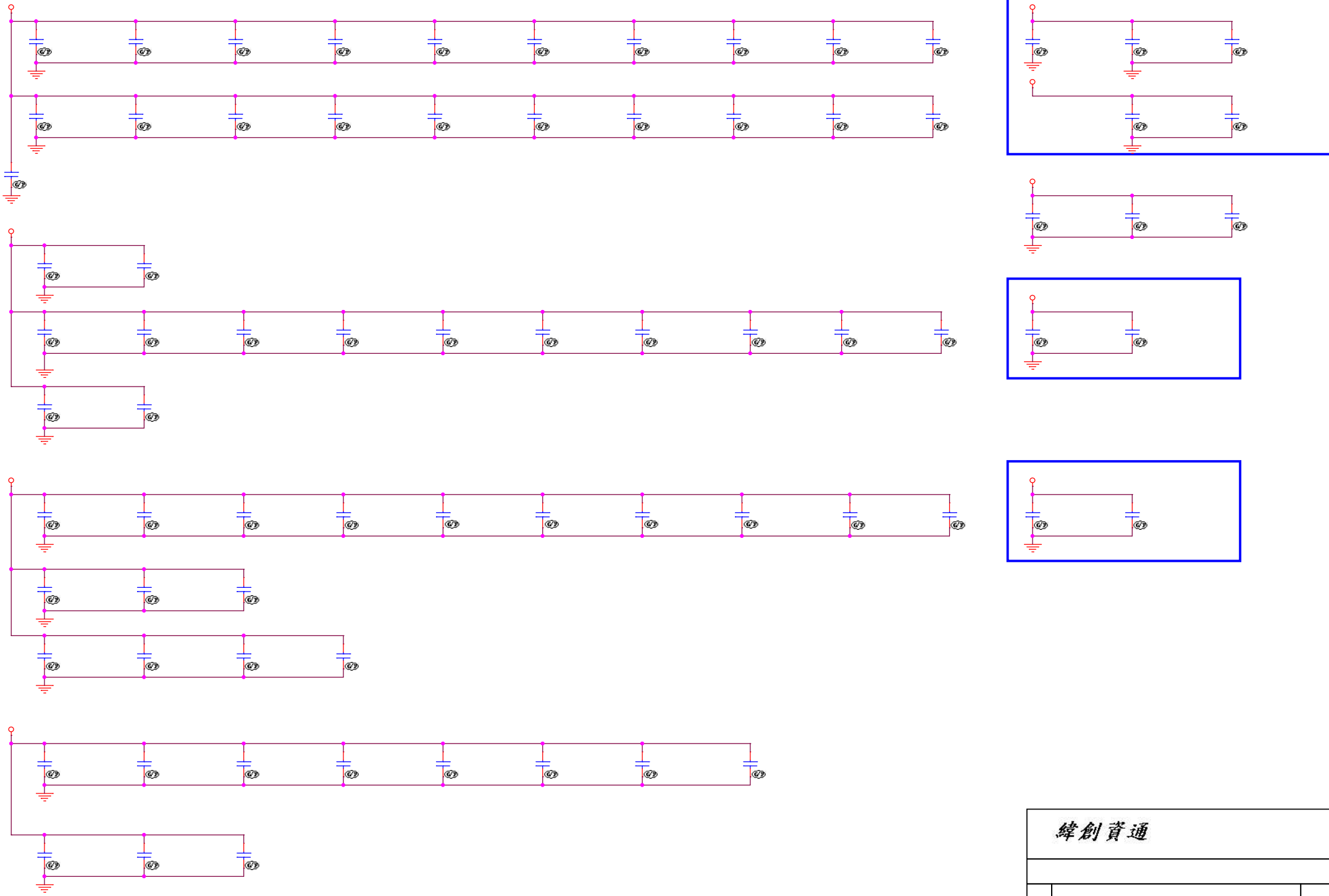
緯創資通







緯創資通



緯創資通

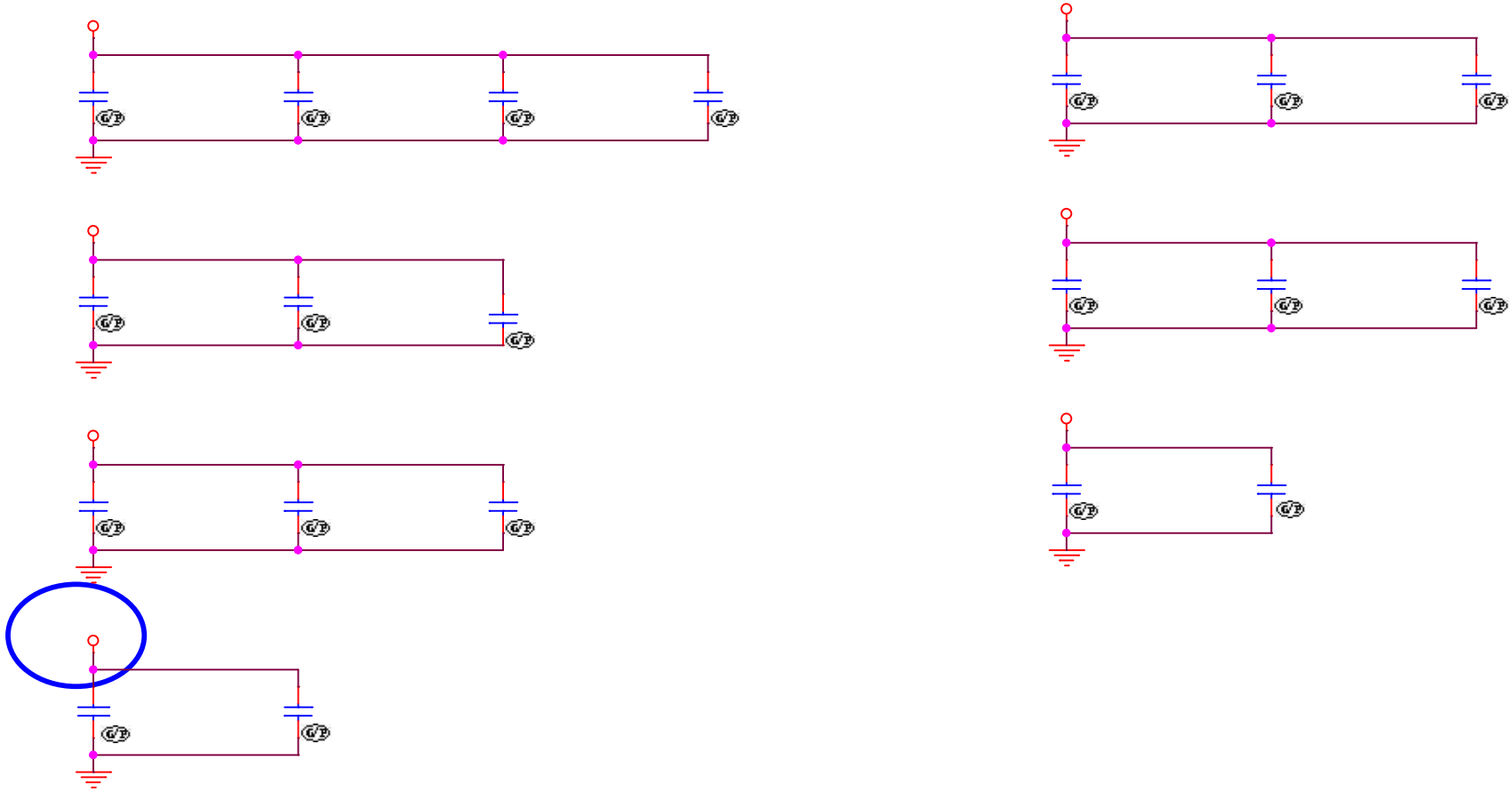
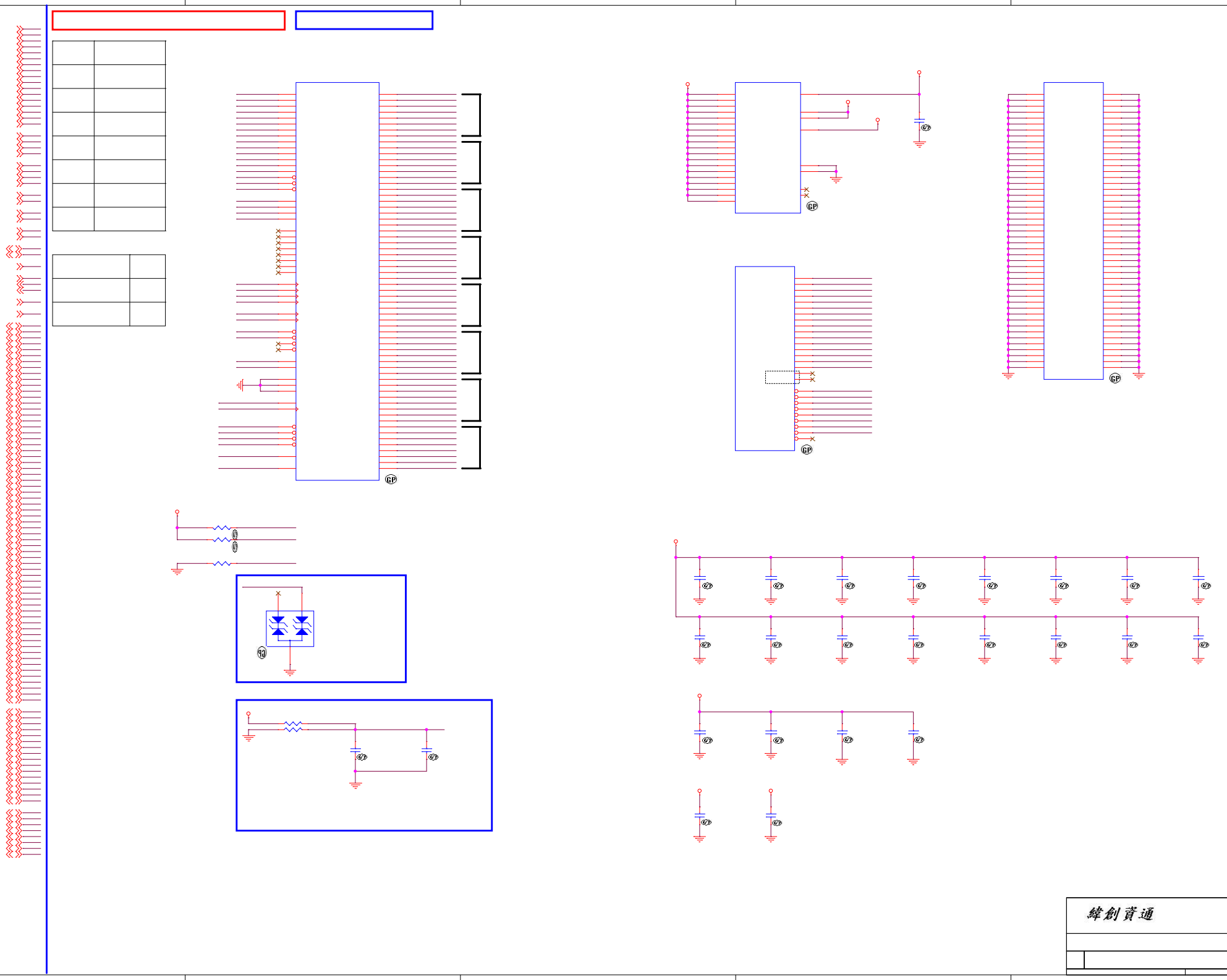


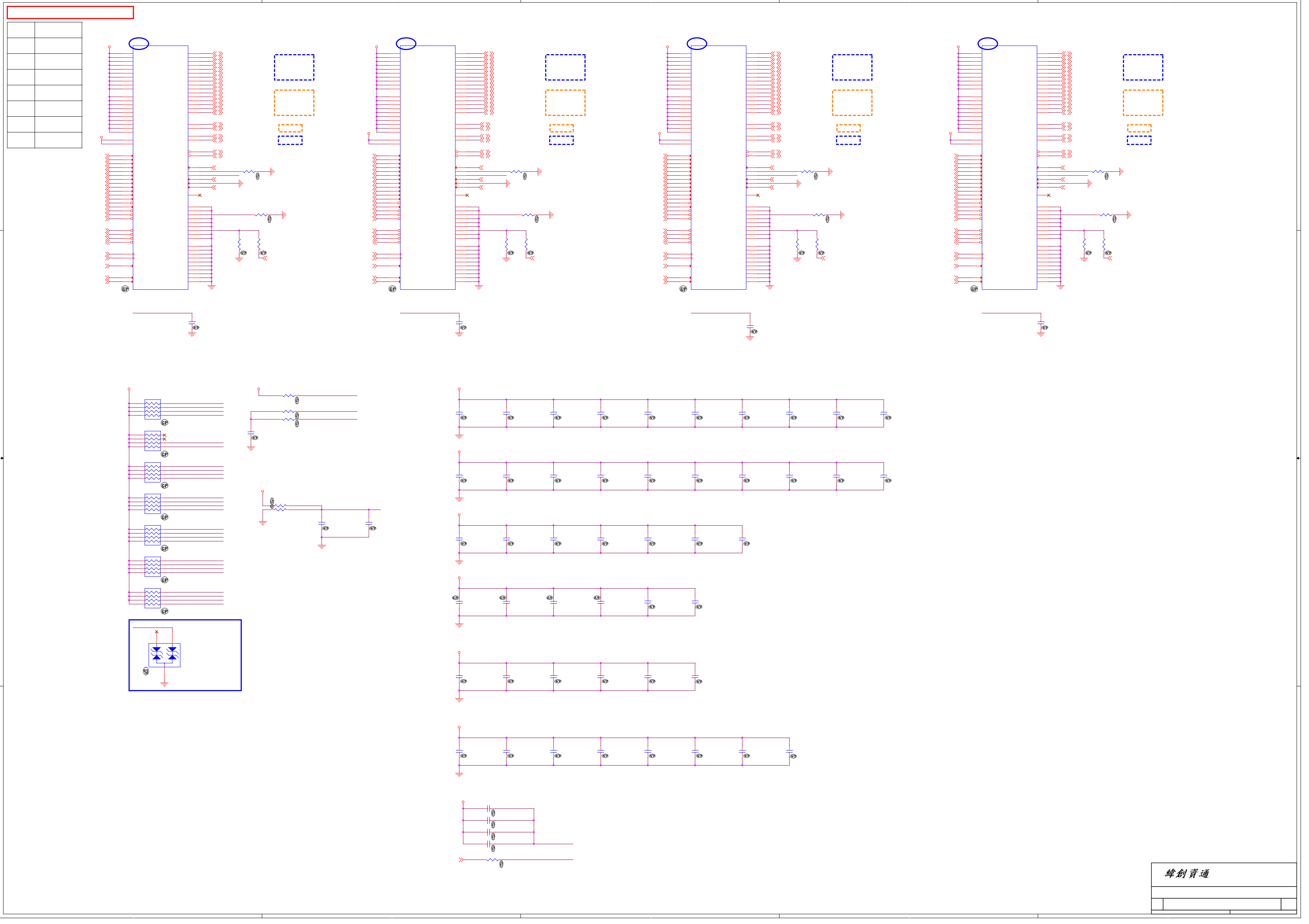
Table 110. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S3[1, 2]	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 µF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 µF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 µF	0402 X5R	-	-	4(split)	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2(split)	1BU	-	-	-	-	-	-	-

緯創資通



緯創資通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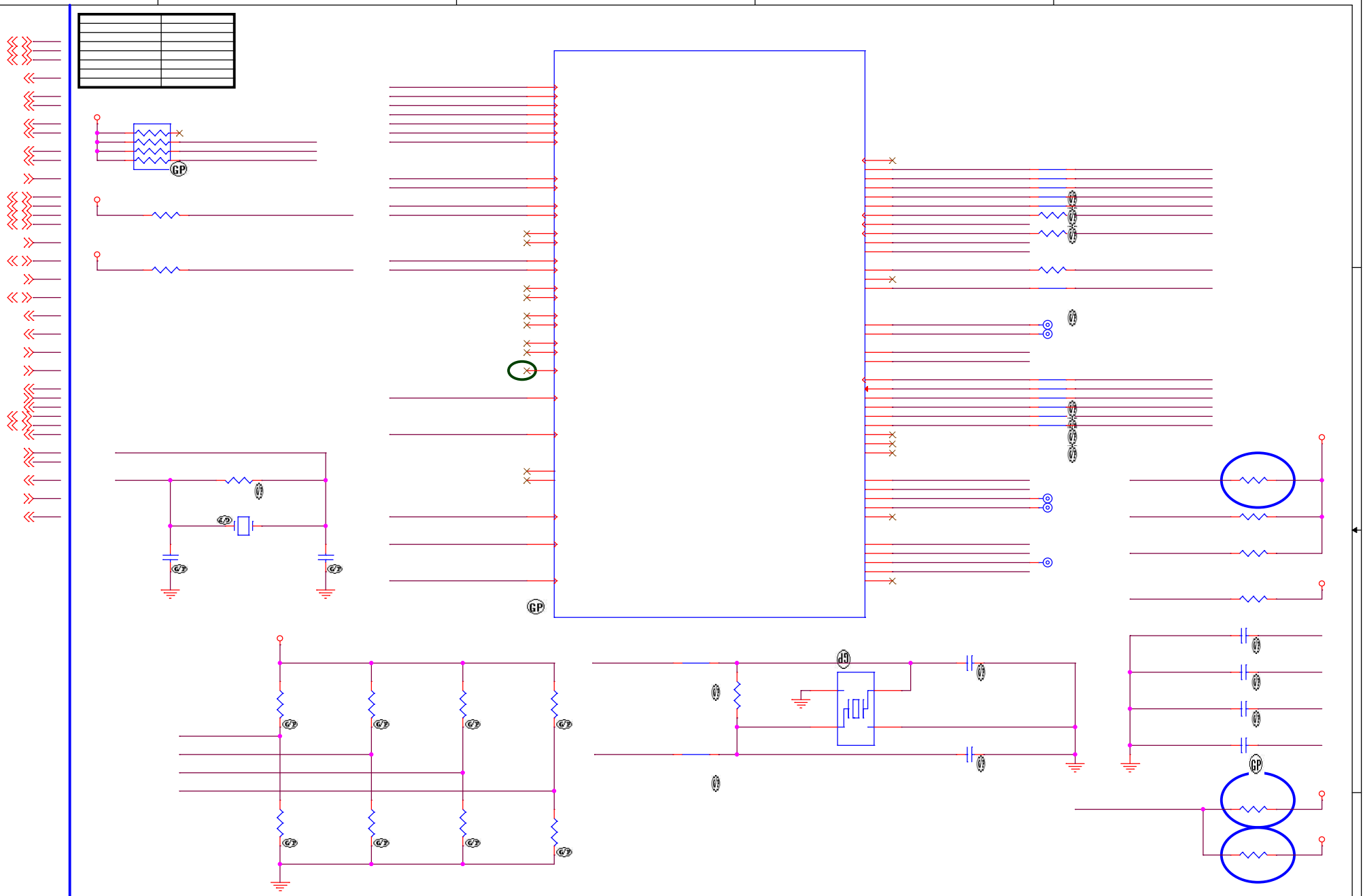

Vendor	ID3	ID2	ID1	ID0	WISTRON PN	Vendor PN	Capacity	Channel	DDP/SDP
MICRON	Reserve	0	0	0	KN.8GB04.027	MT40A512M16LY-075:E	8Gb	B	SDP
HYNIX	Reserve	0	0	1	KN.8GB0G.061	H5AN8G6NCJR-VKC	8Gb	B	SDP
	Reserve	0	1	0	TBD				
	Reserve	0	1	1	TBD				
	Reserve	1	0	0	TBD				
	Reserve	1	0	1	TBD				
	Reserve	1	1	0	TBD				
	Reserve	1	1	1	TBD				

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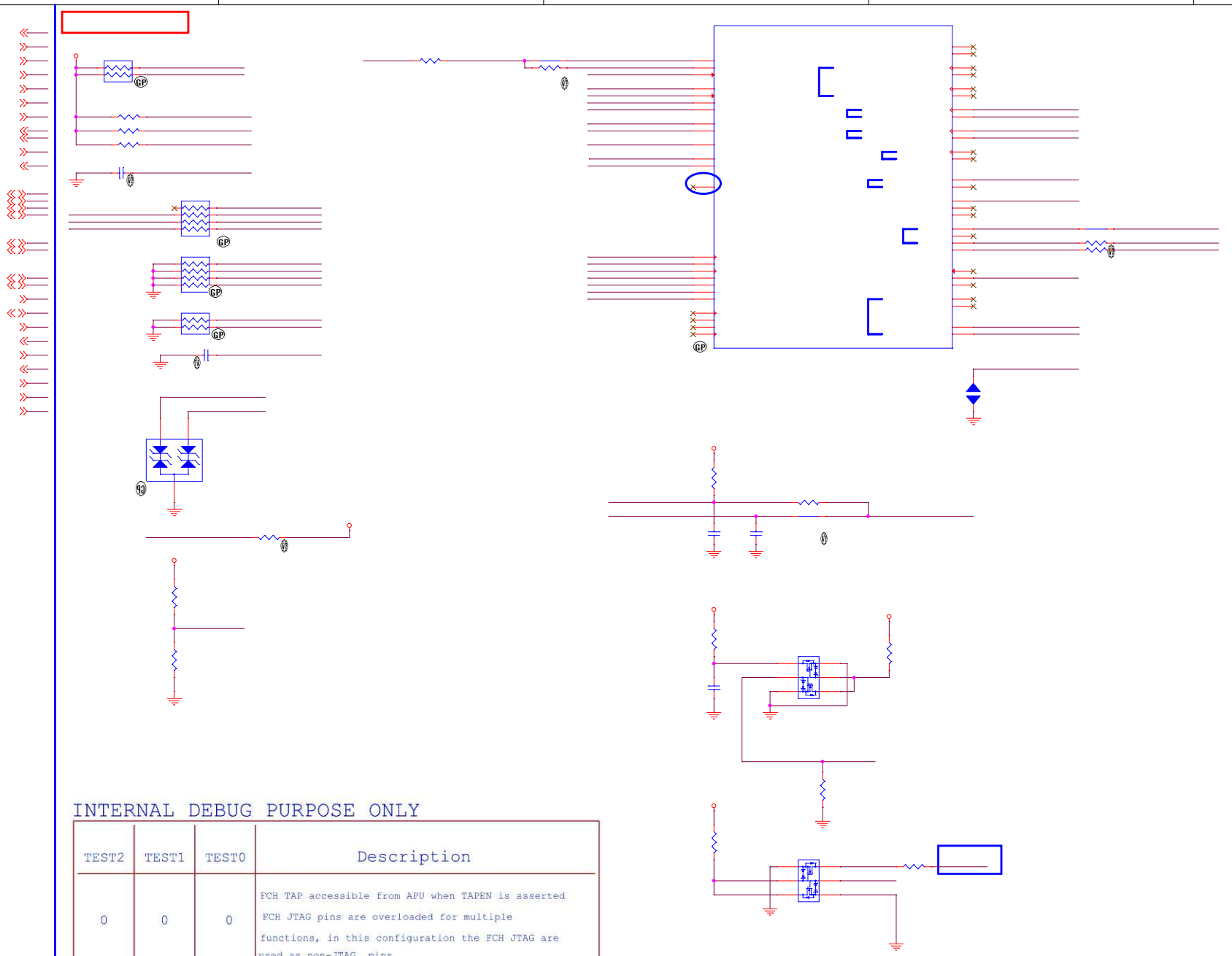
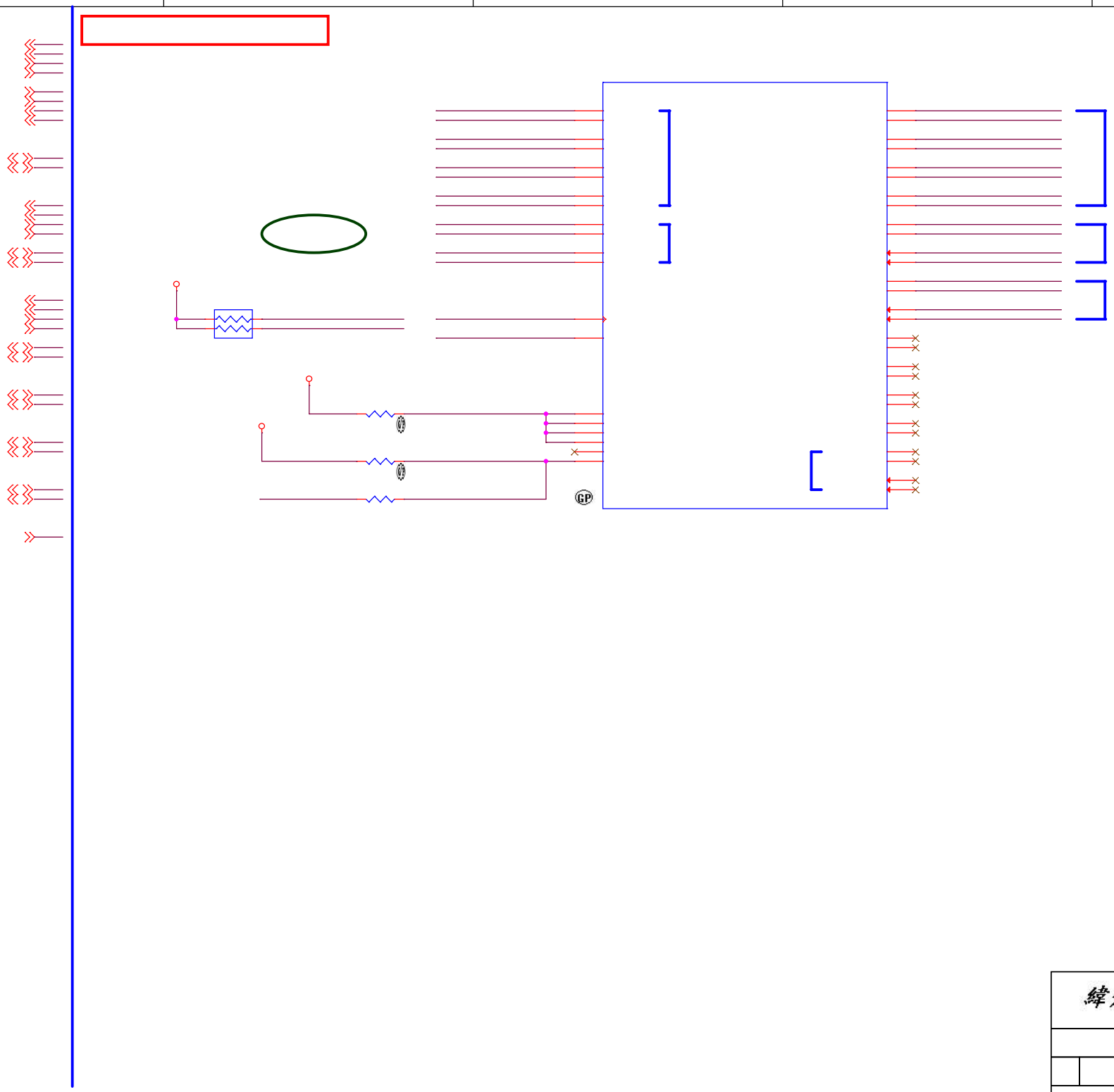


INTERNAL DEBUG PURPOSE ONLY

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

緯創資通



緯創資通

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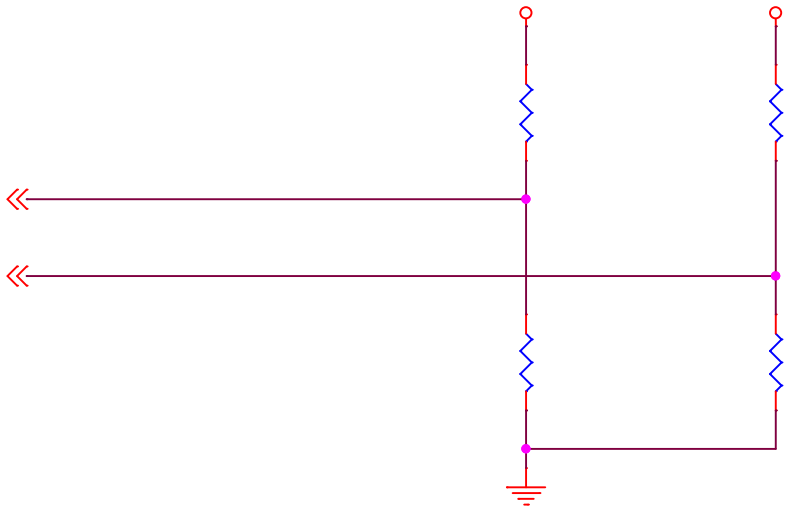
STRAP PINS



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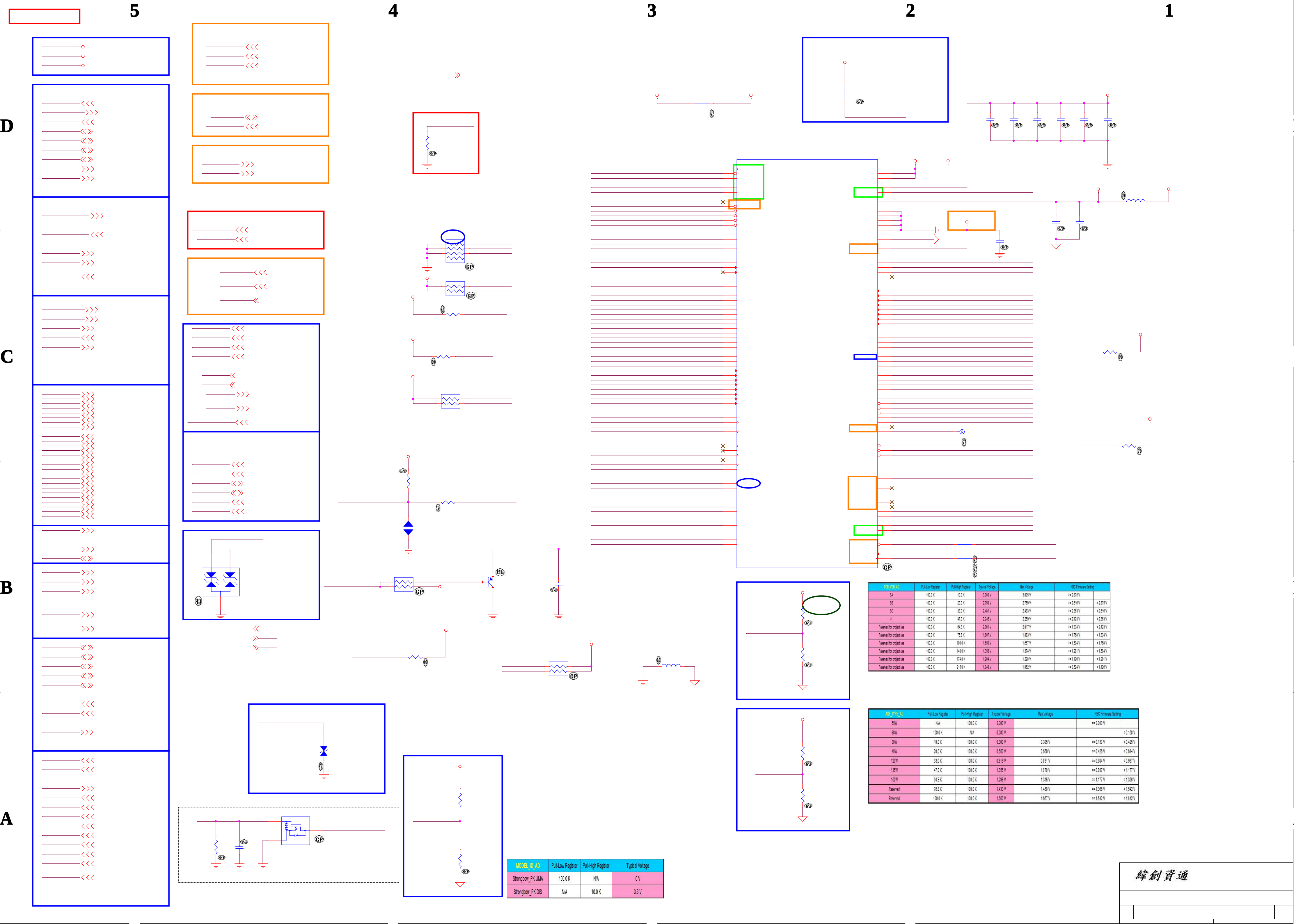
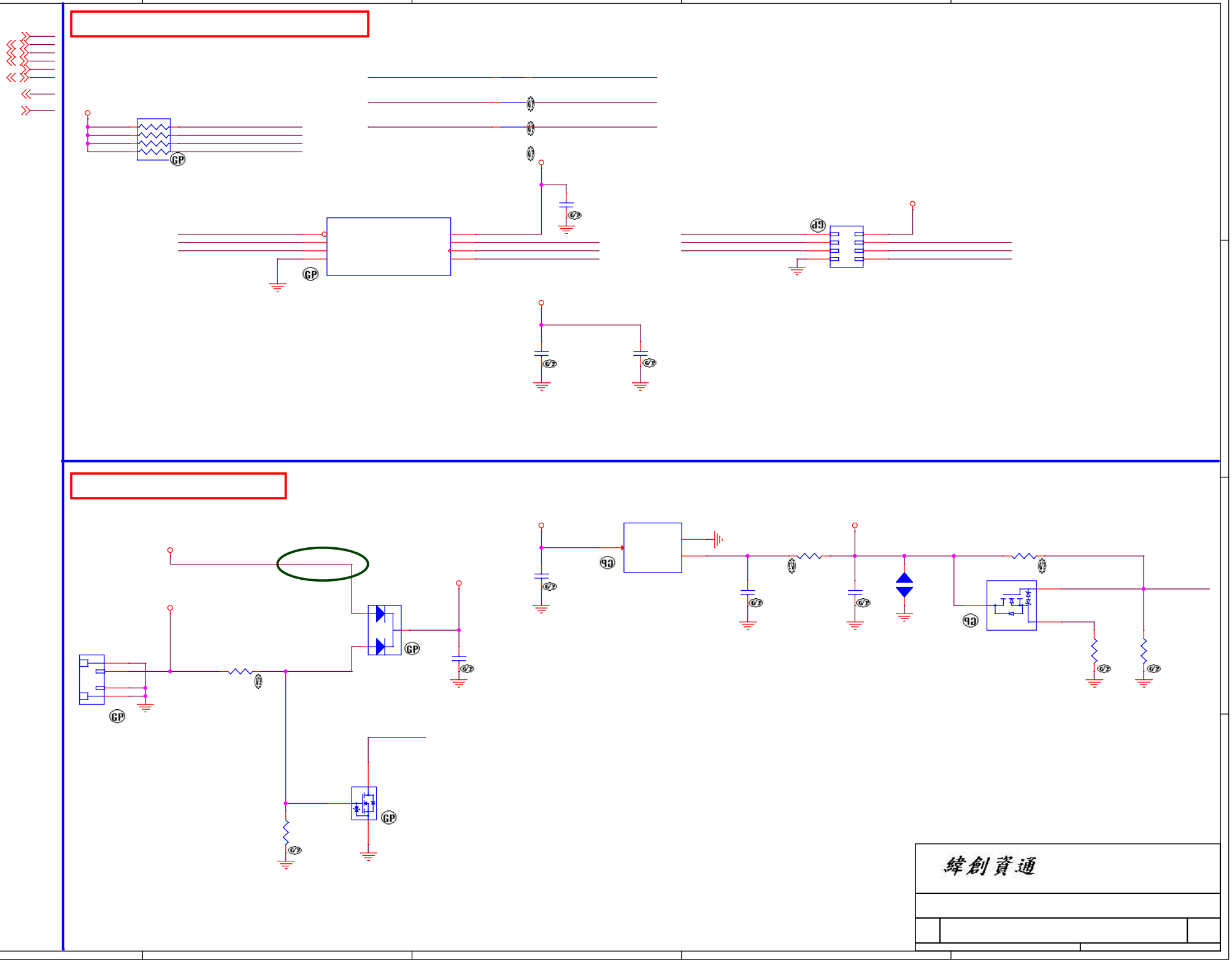


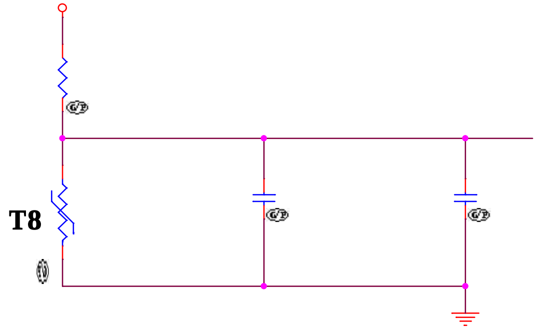
PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

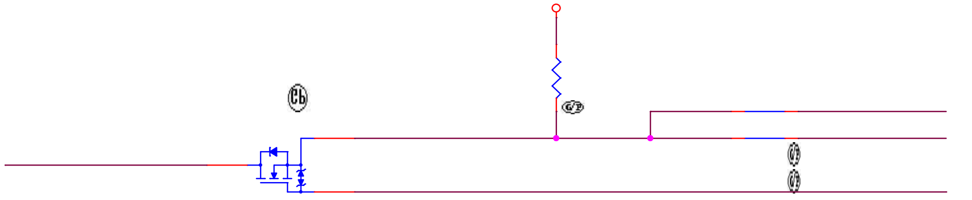
ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Strongbow_PK UMA	100.0 K	N/A	0 V
Strongbow_PK DIS	N/A	10.0 K	3.3 V


緯創資通

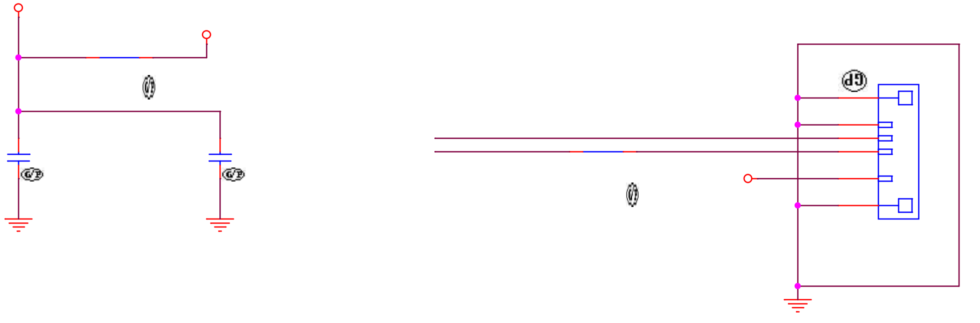
SSID = Thermal

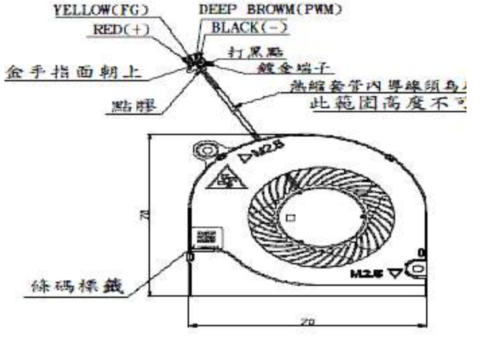




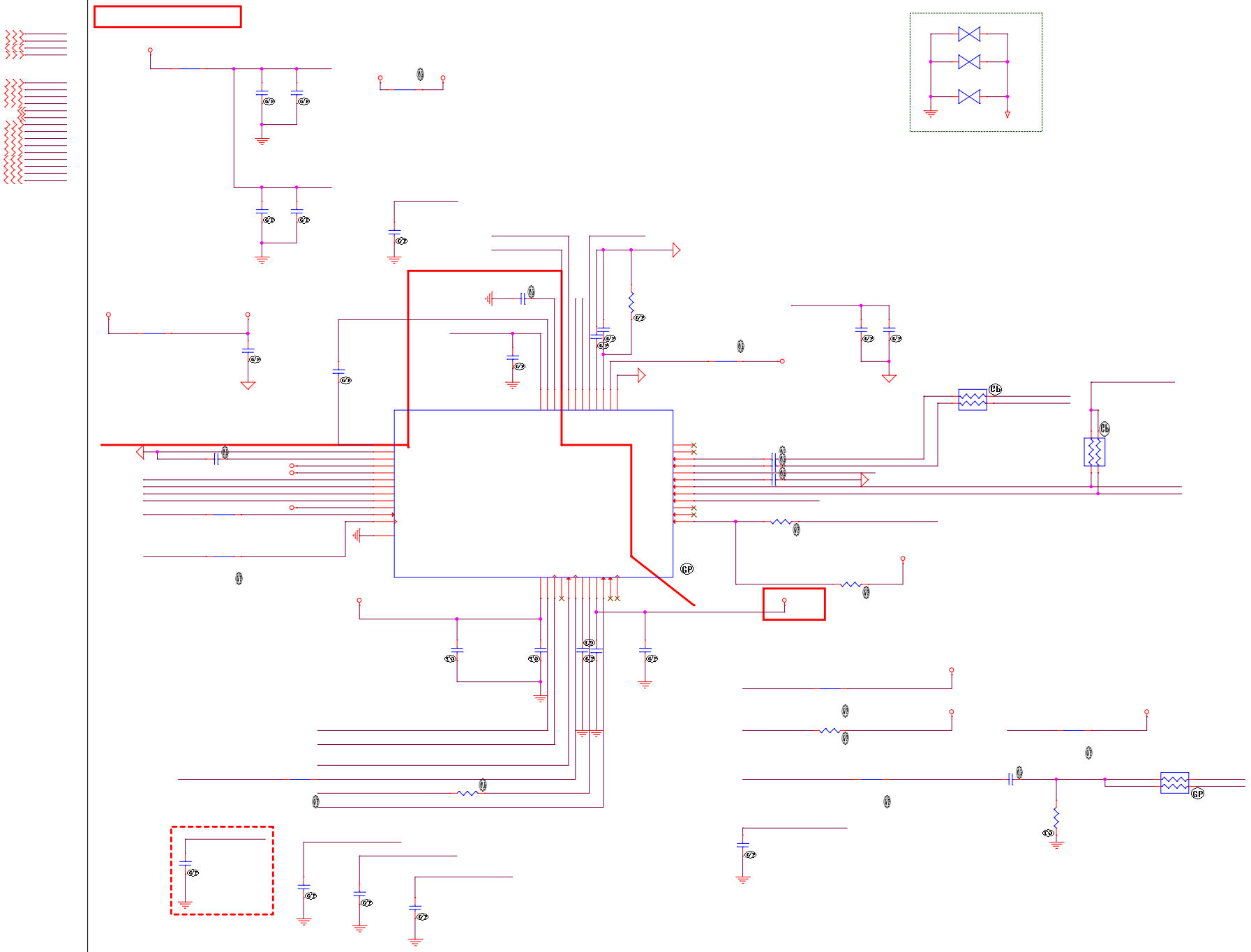
RT2601 close CPU and Vcore choke
VD_IN1 trace 10 mil

Layout: 15 mil





緯創資通 **Wistron Corporation**



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Blanking

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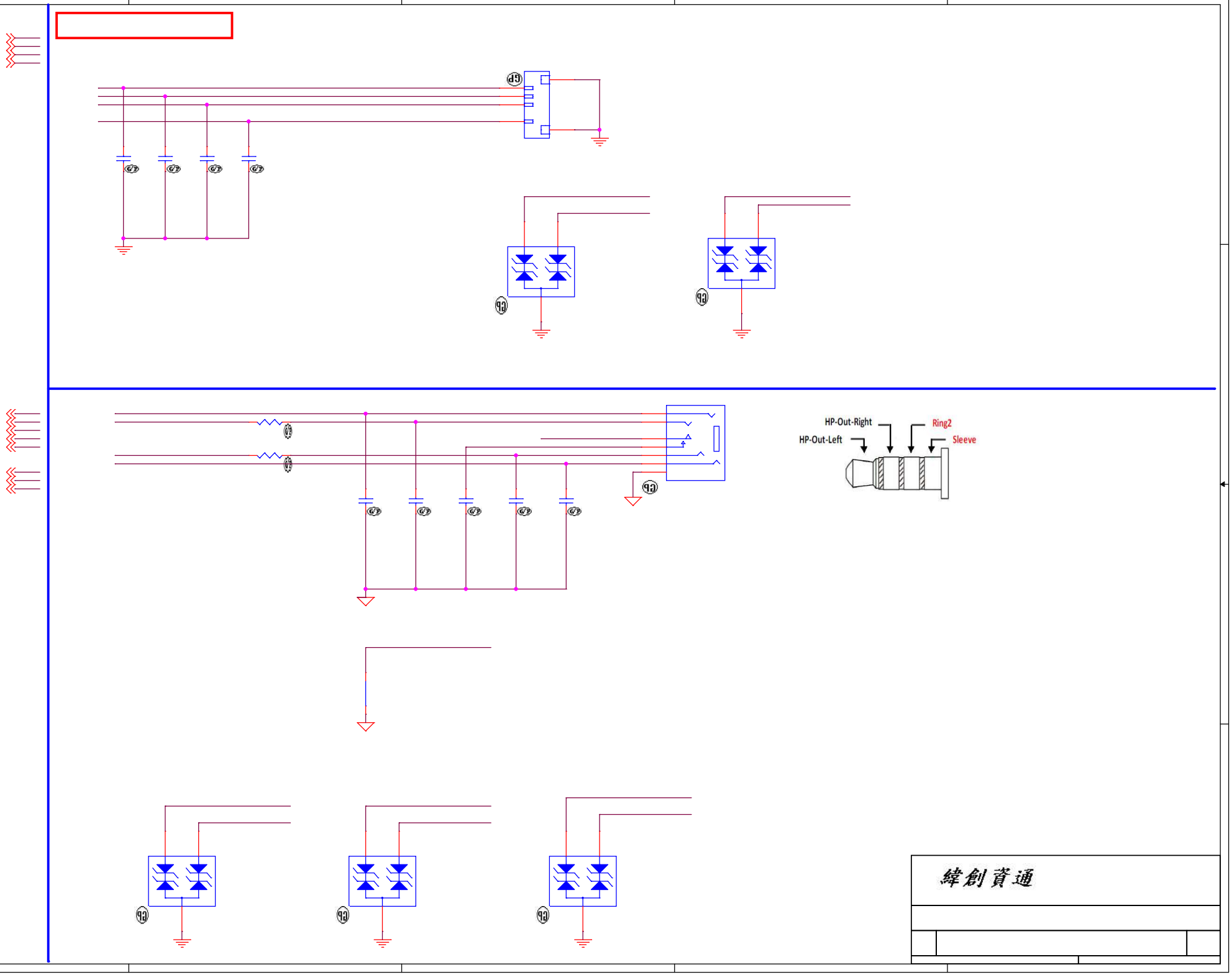
HP-Out-Right
HP-Out-Left
Ring2
Sleeve
緯創資通

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Blanking

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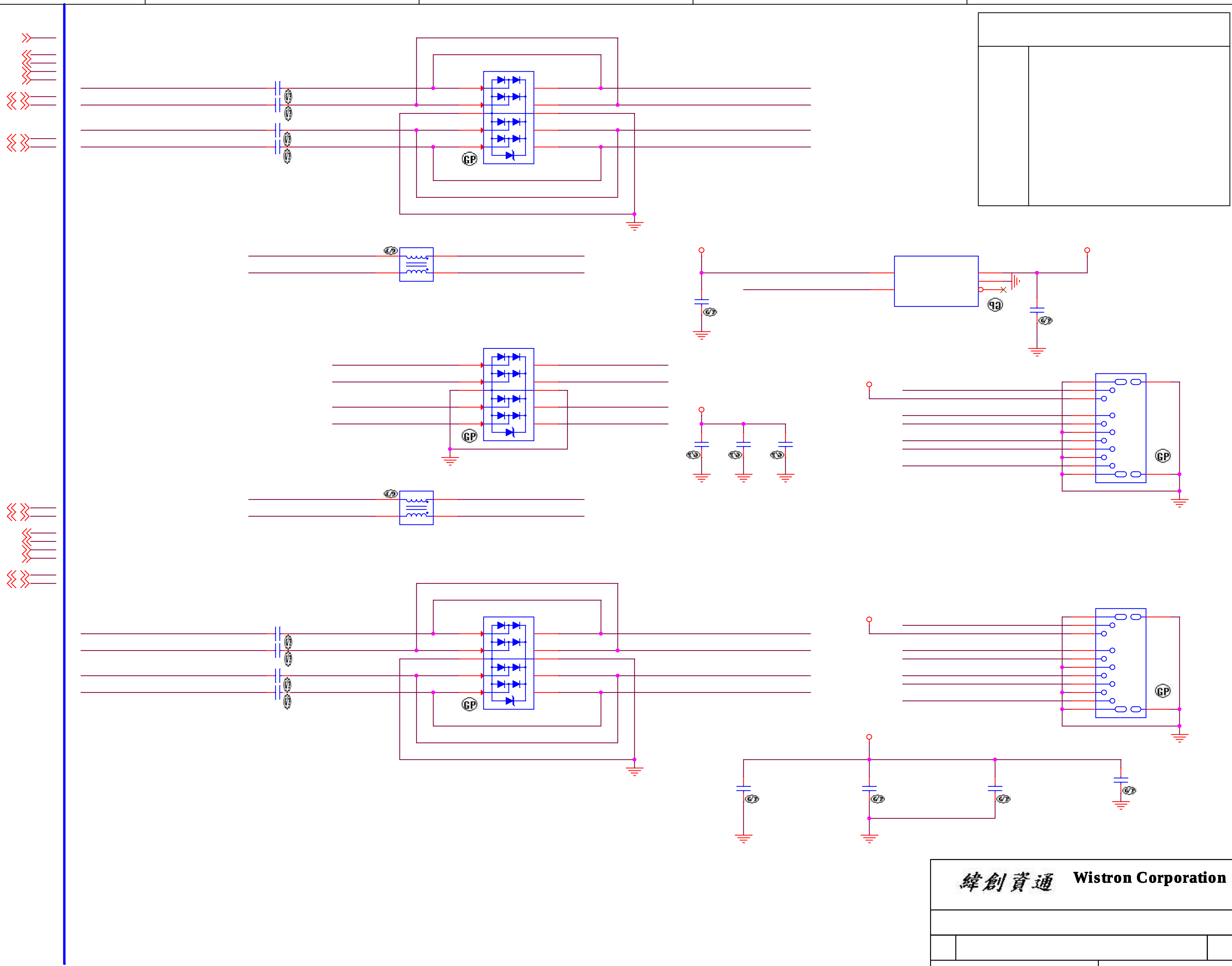
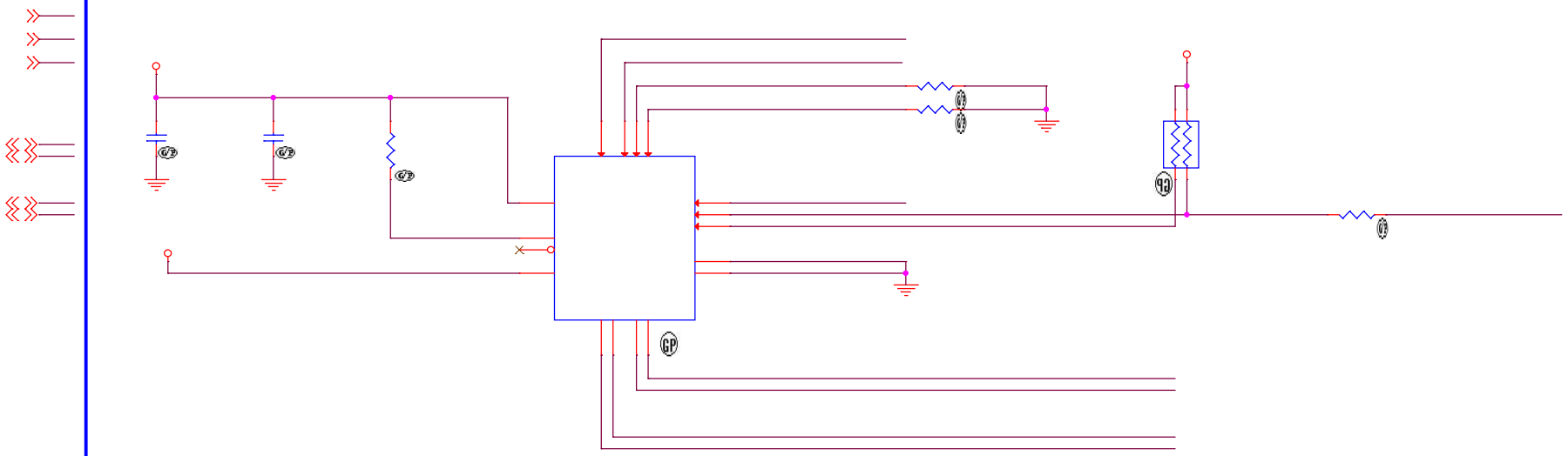


緯創資通 Wistron Corporation



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

緯創資通

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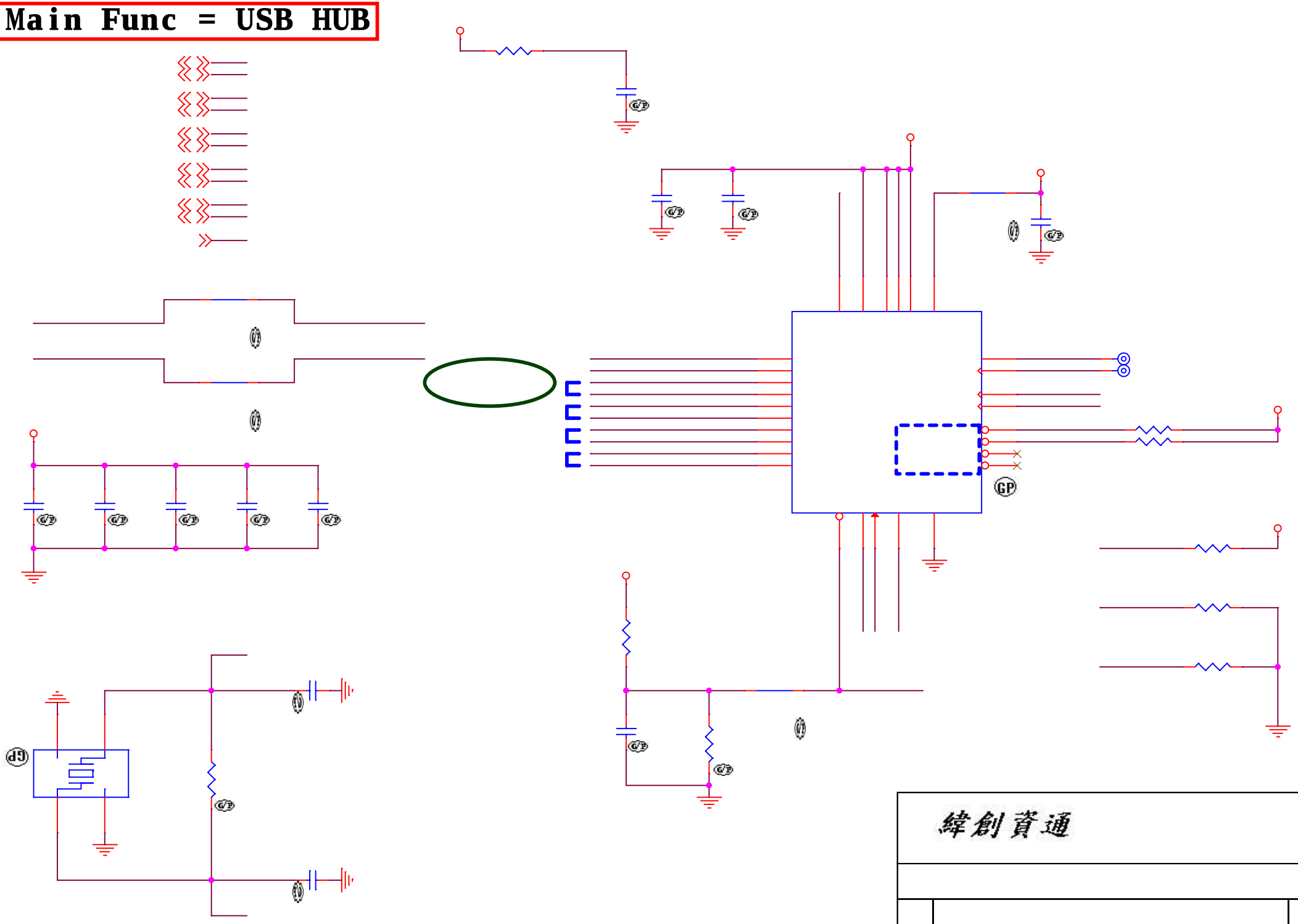
緯創資通

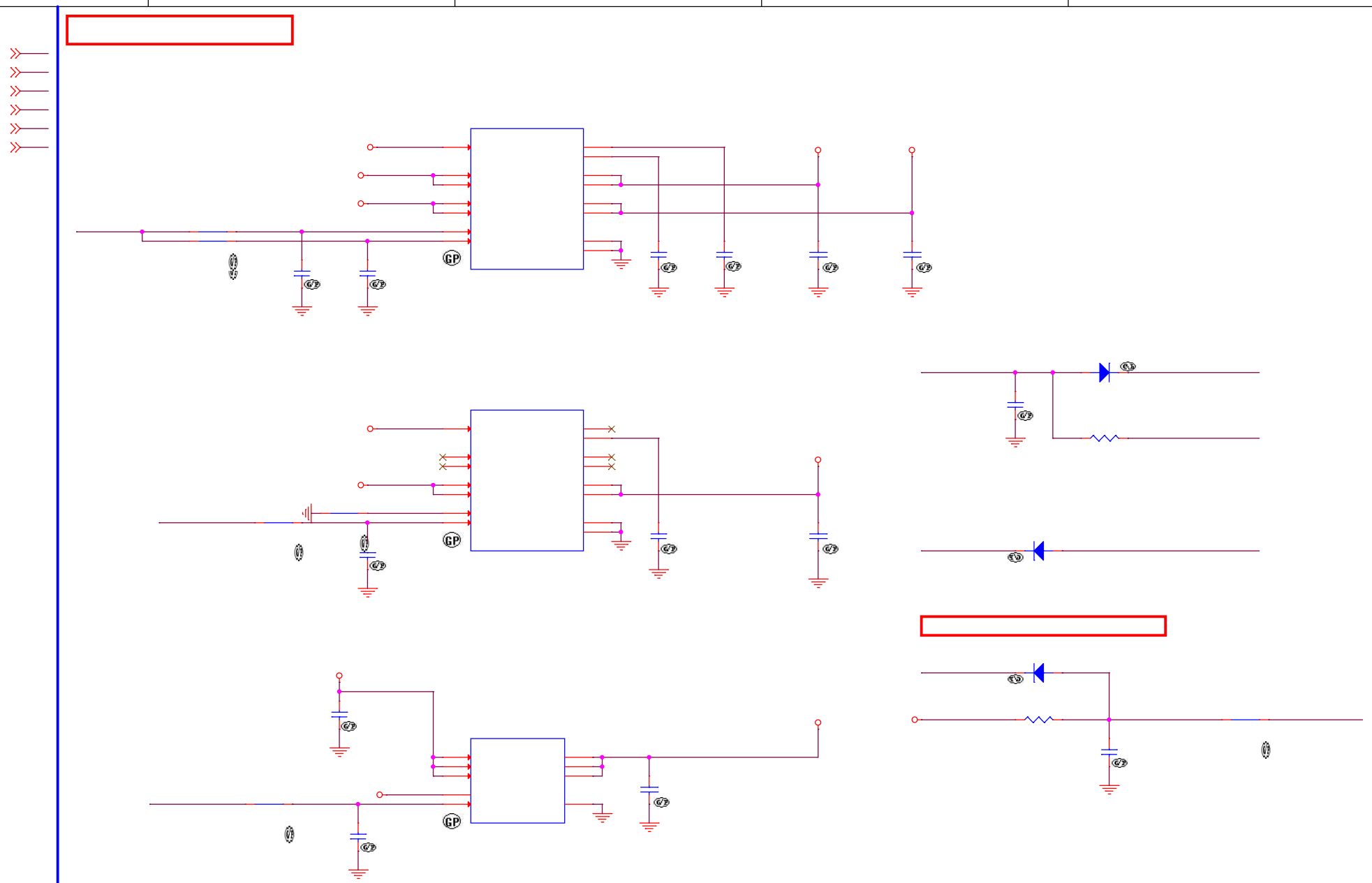
Main Func = USB HUB



緯創資通

Blanking

緯創資通



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Blanking

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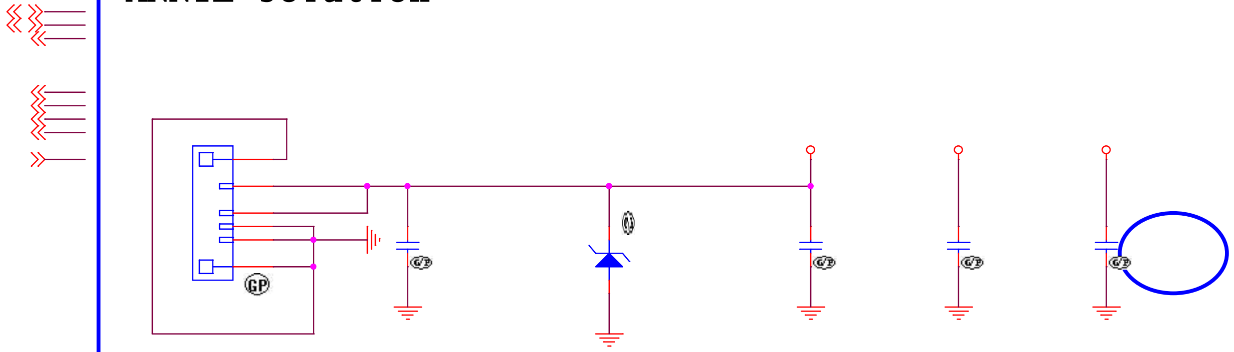
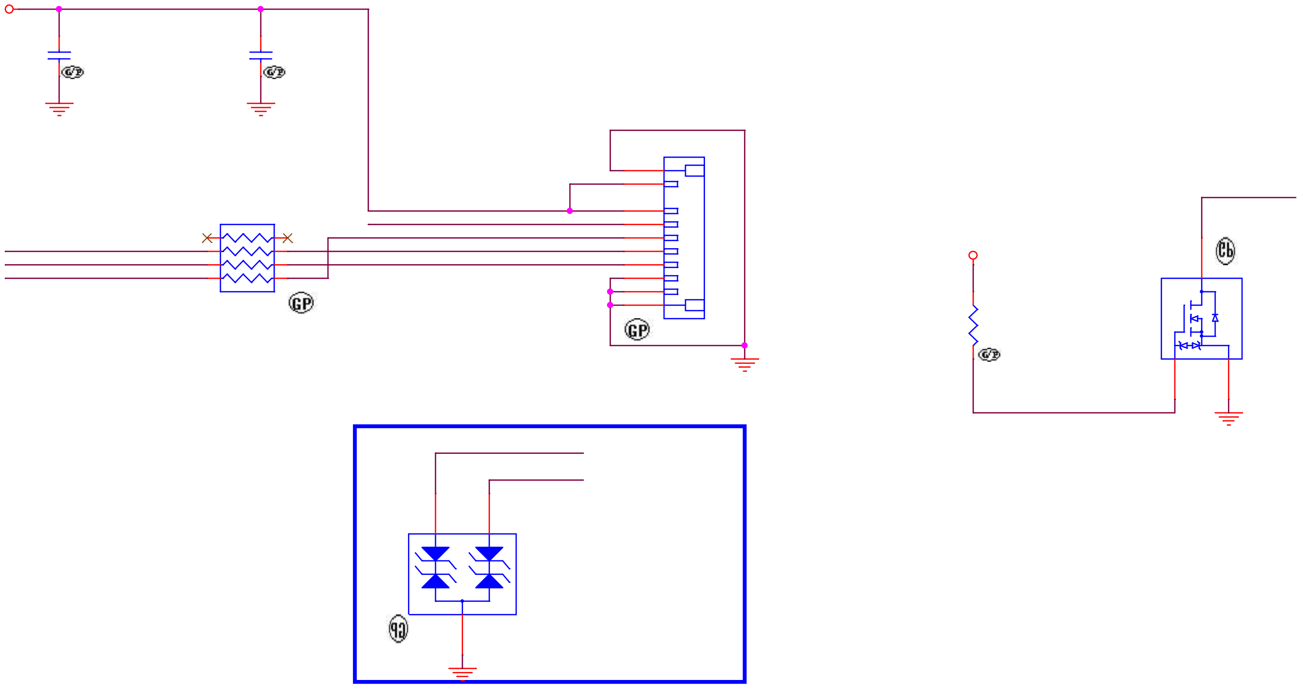
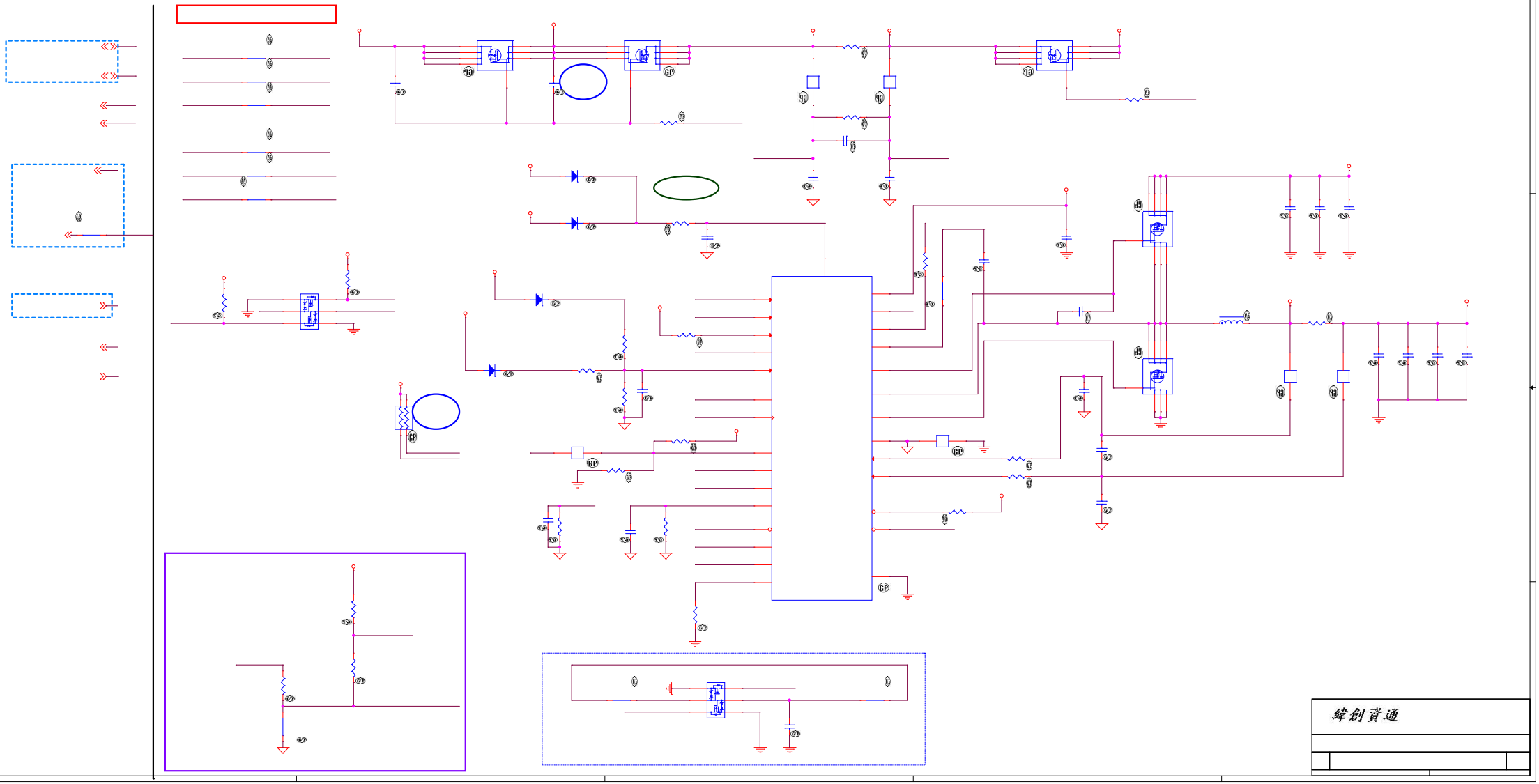
ANNIE solution

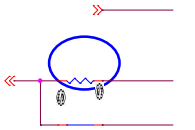


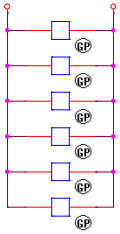
BATTERY CONNECTOR

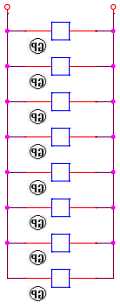


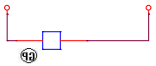
緯創資通 **Wistron Corporation**

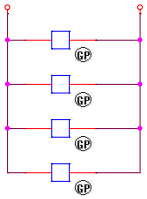

緯創資通

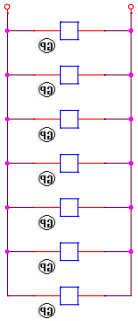


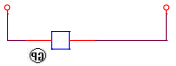


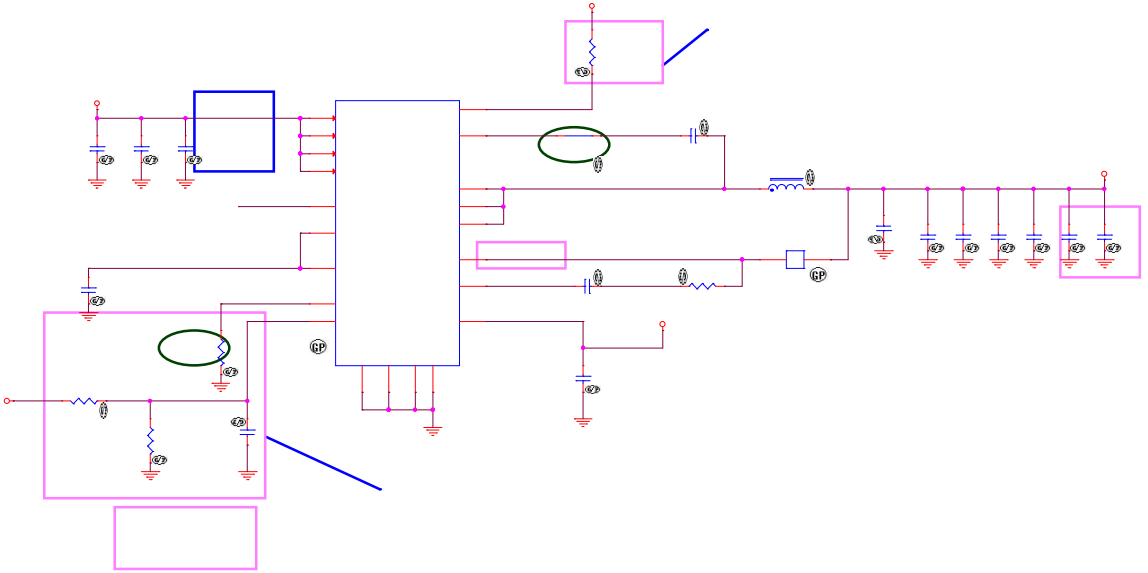


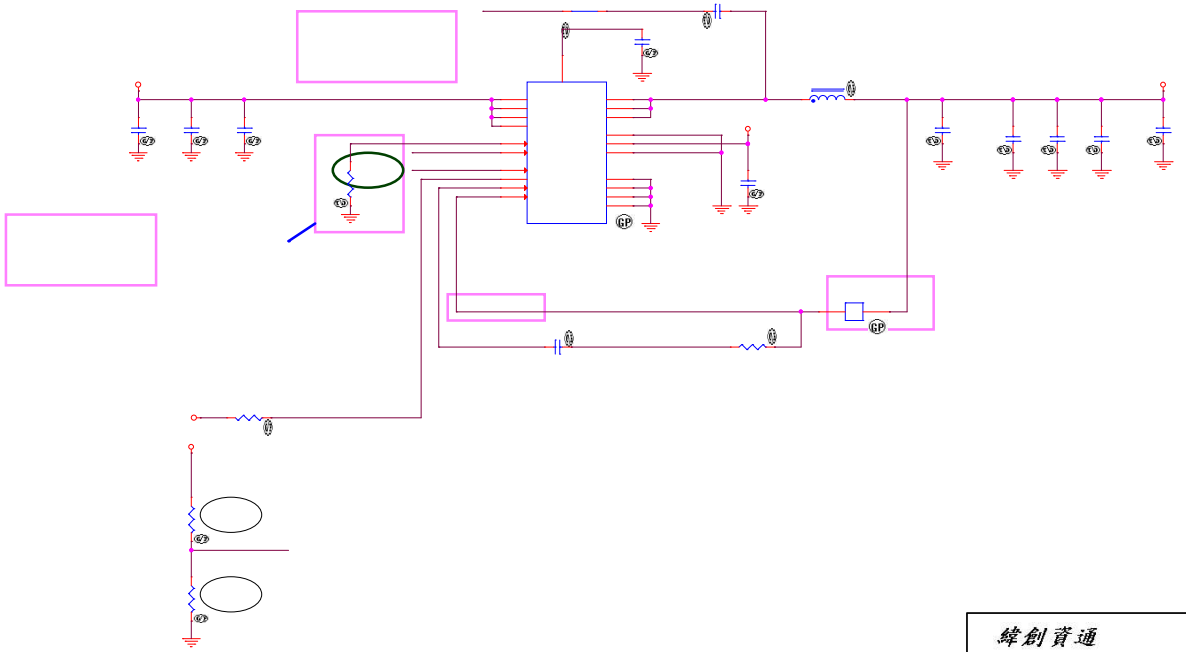




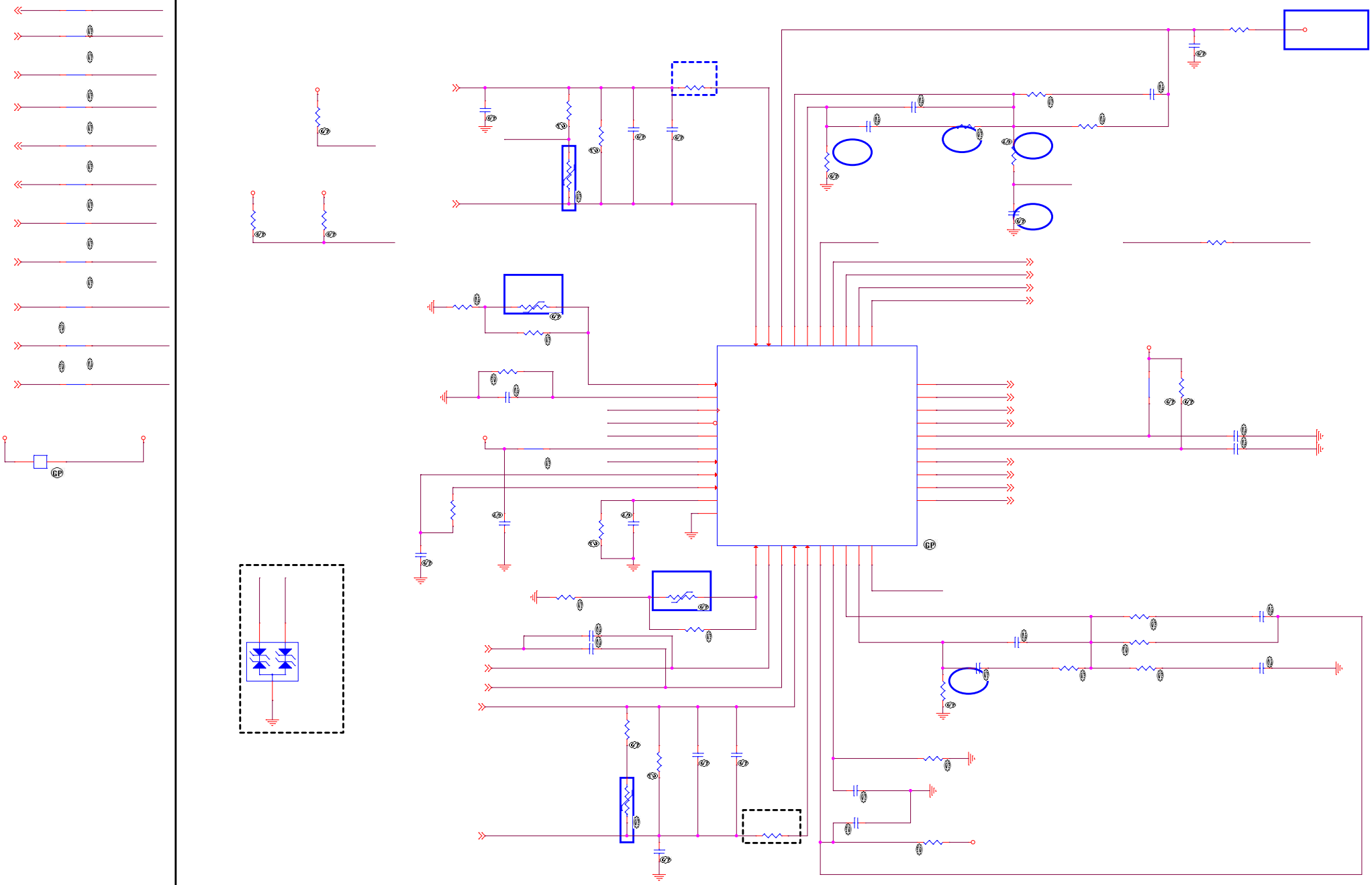






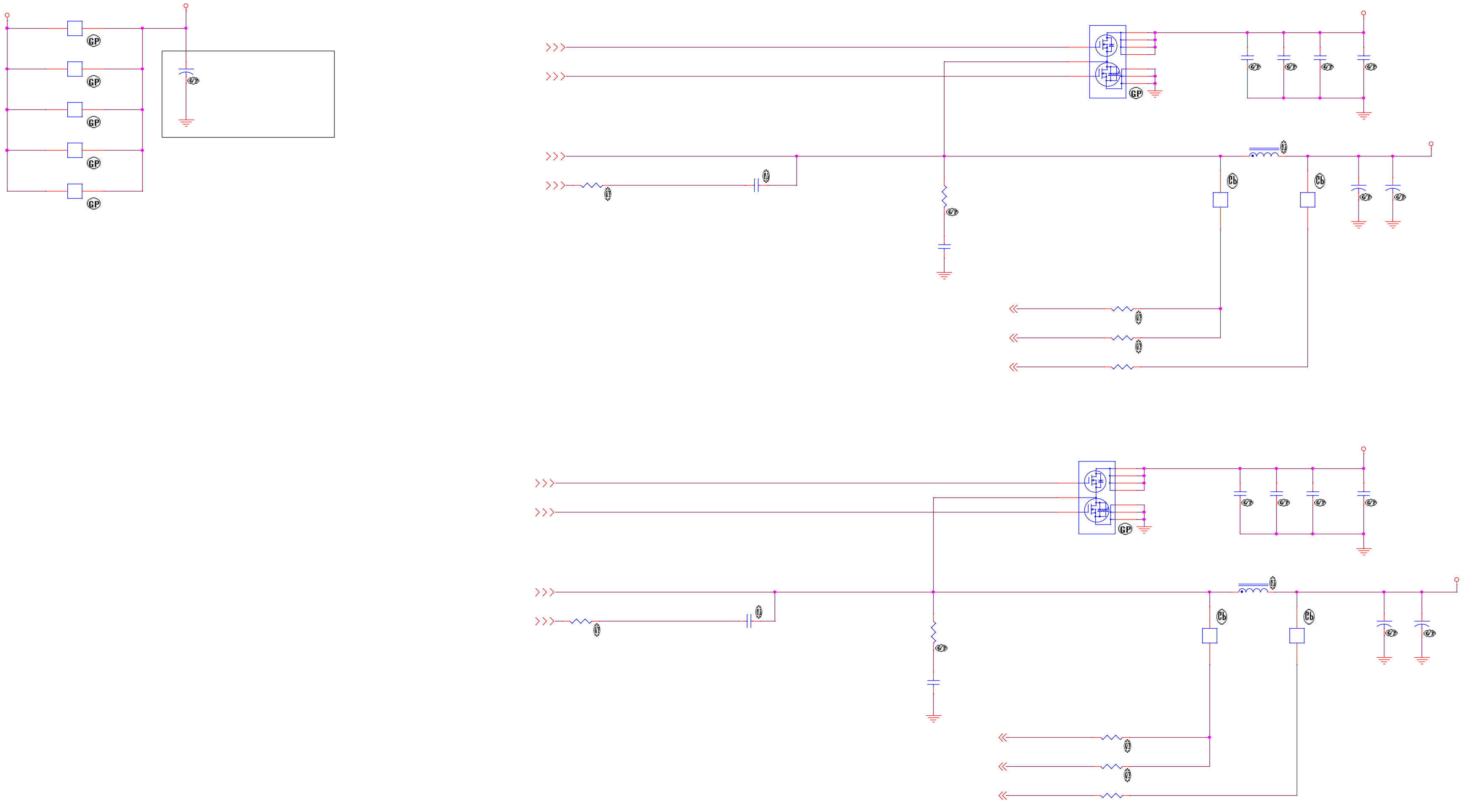


緯創資通



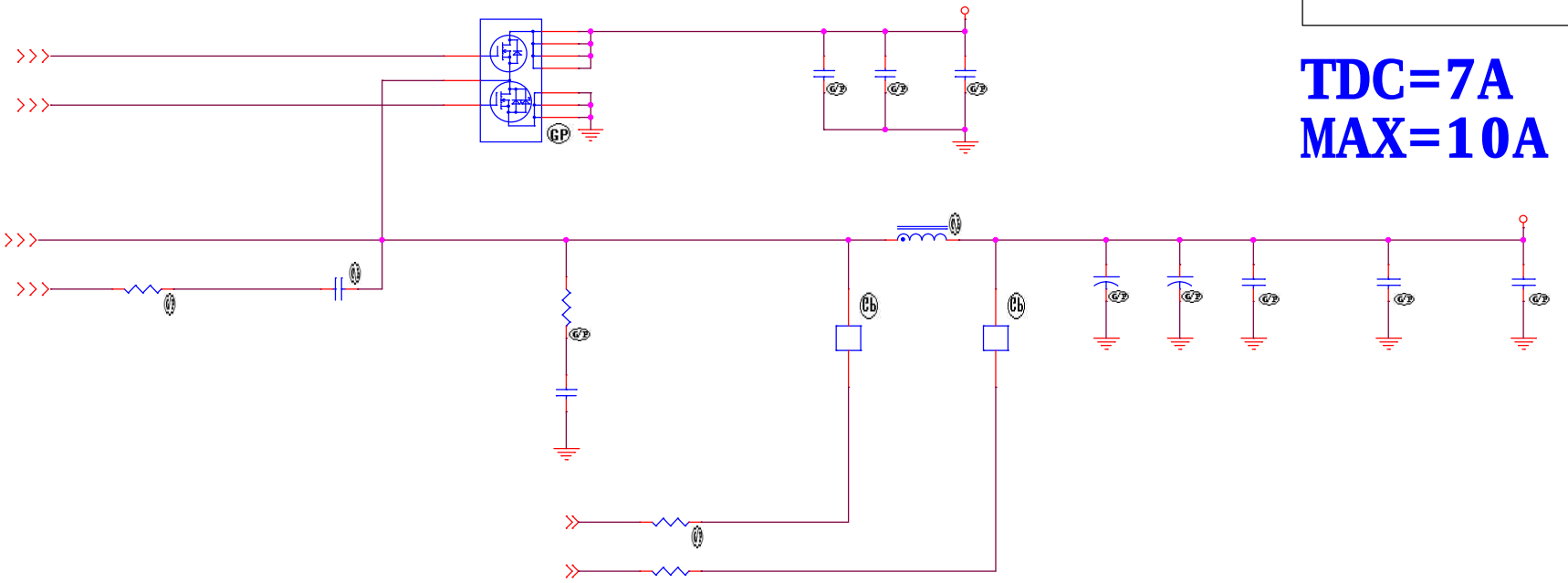
緯創資通

Main Func = APU VDDCR_VDD 2ph H/LS MosFET and Output LC



TDC=24.5A
EDC=35A

緯創資通



TDC=7A
MAX=10A

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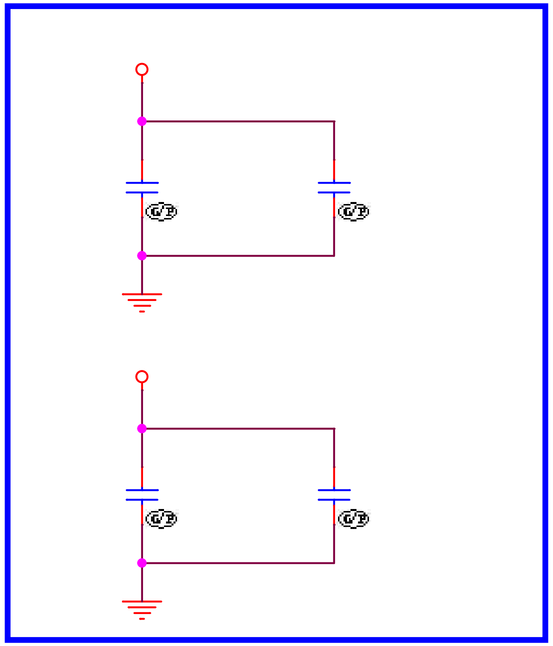
Low Noise MLCC



Blanking

緯創資通

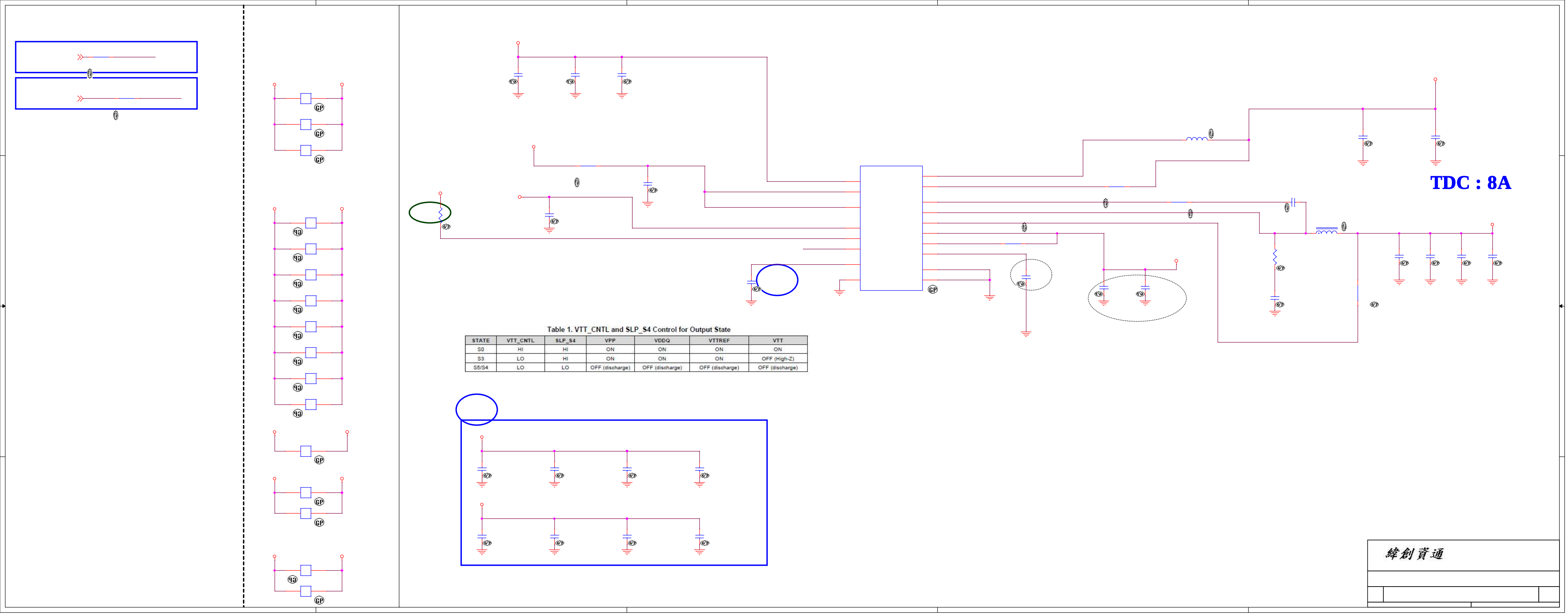


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

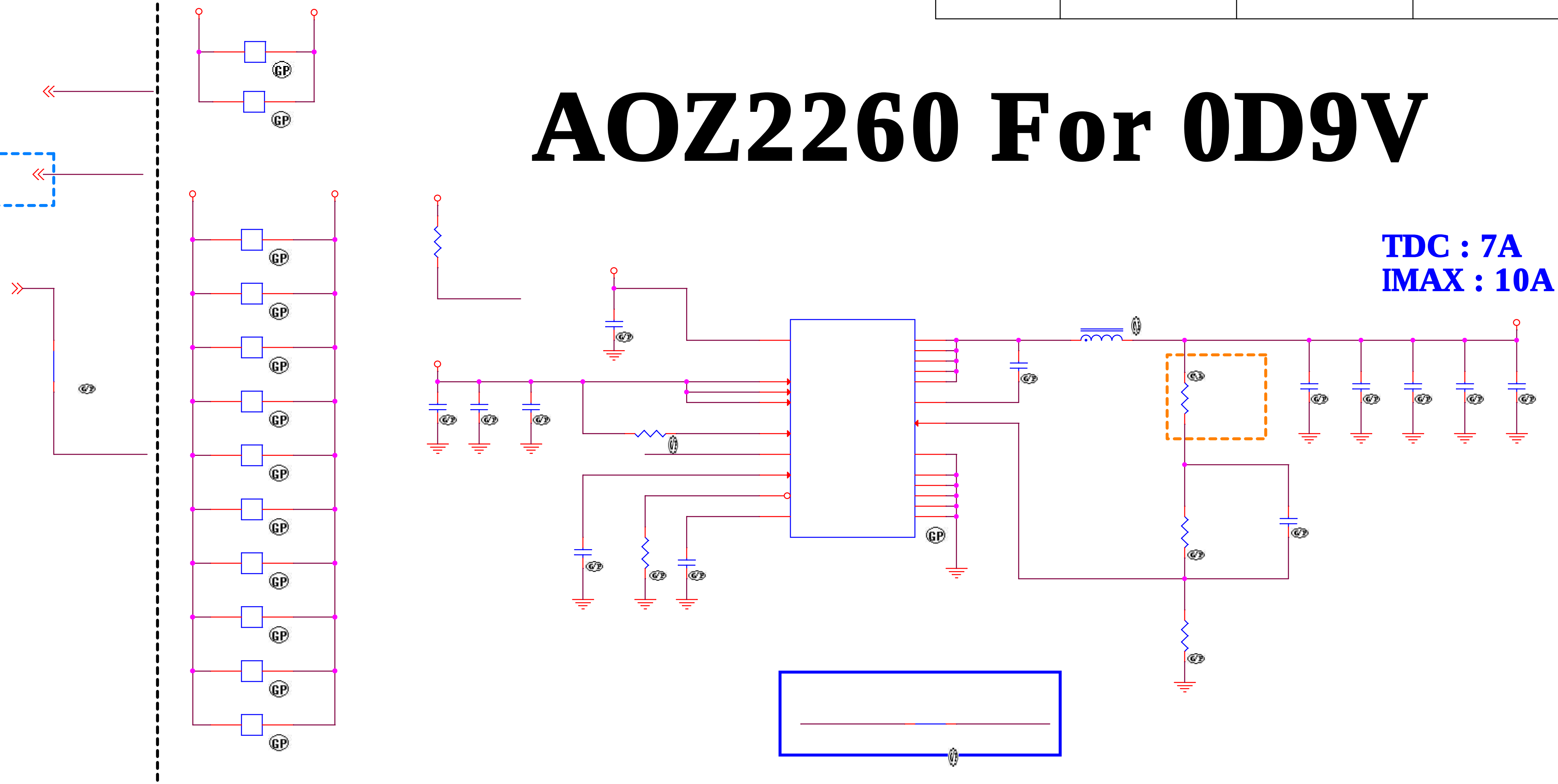
SSID = PWR.Plane.Regulator_0D9V

OFFPAGE-Signal

OFFPAGE-GAP

COM \ IC	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043

AOZ2260 For 0D9V



TDC : 7A
IMAX : 10A

緯創資通 Wistron Corporation

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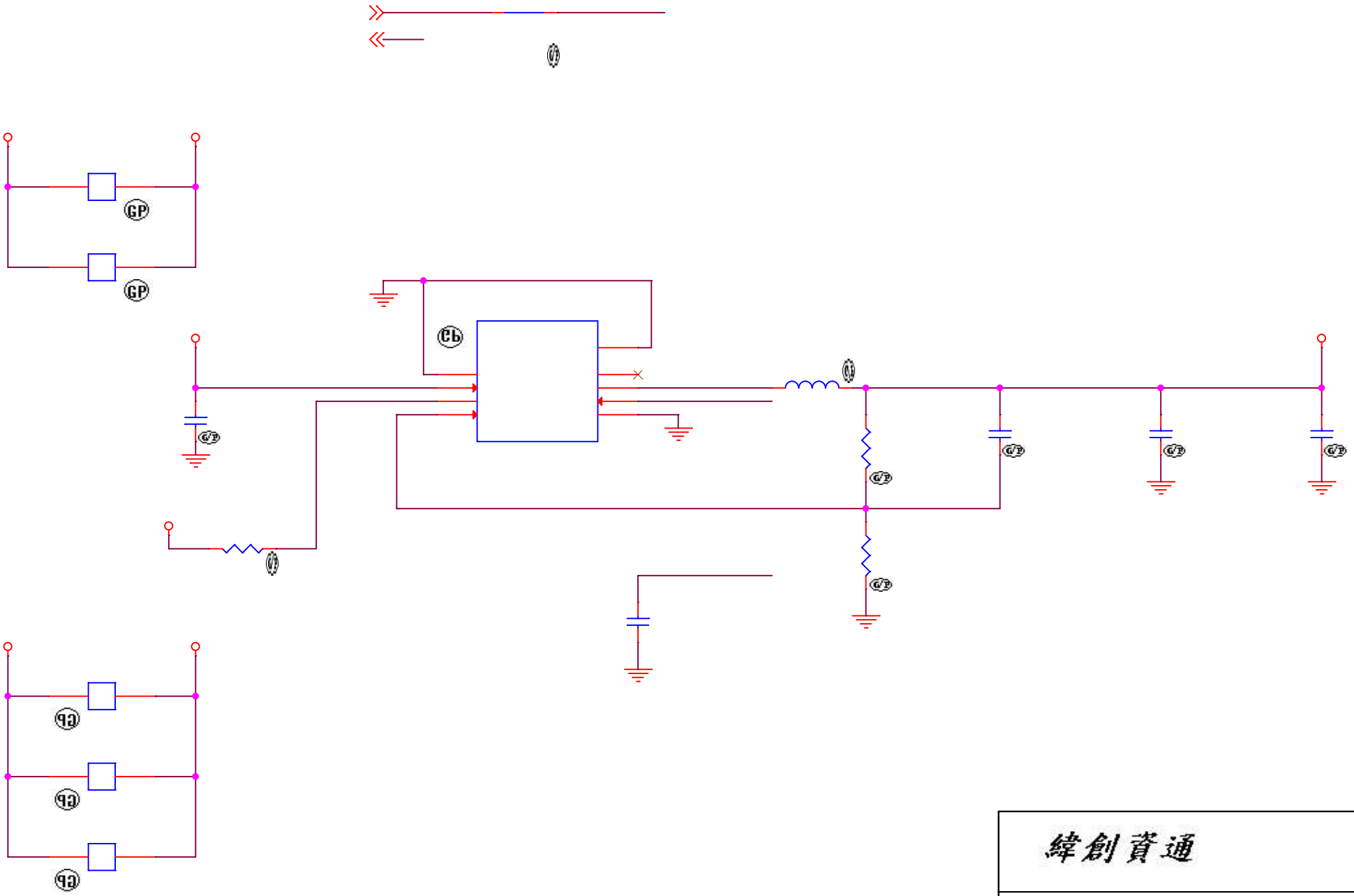
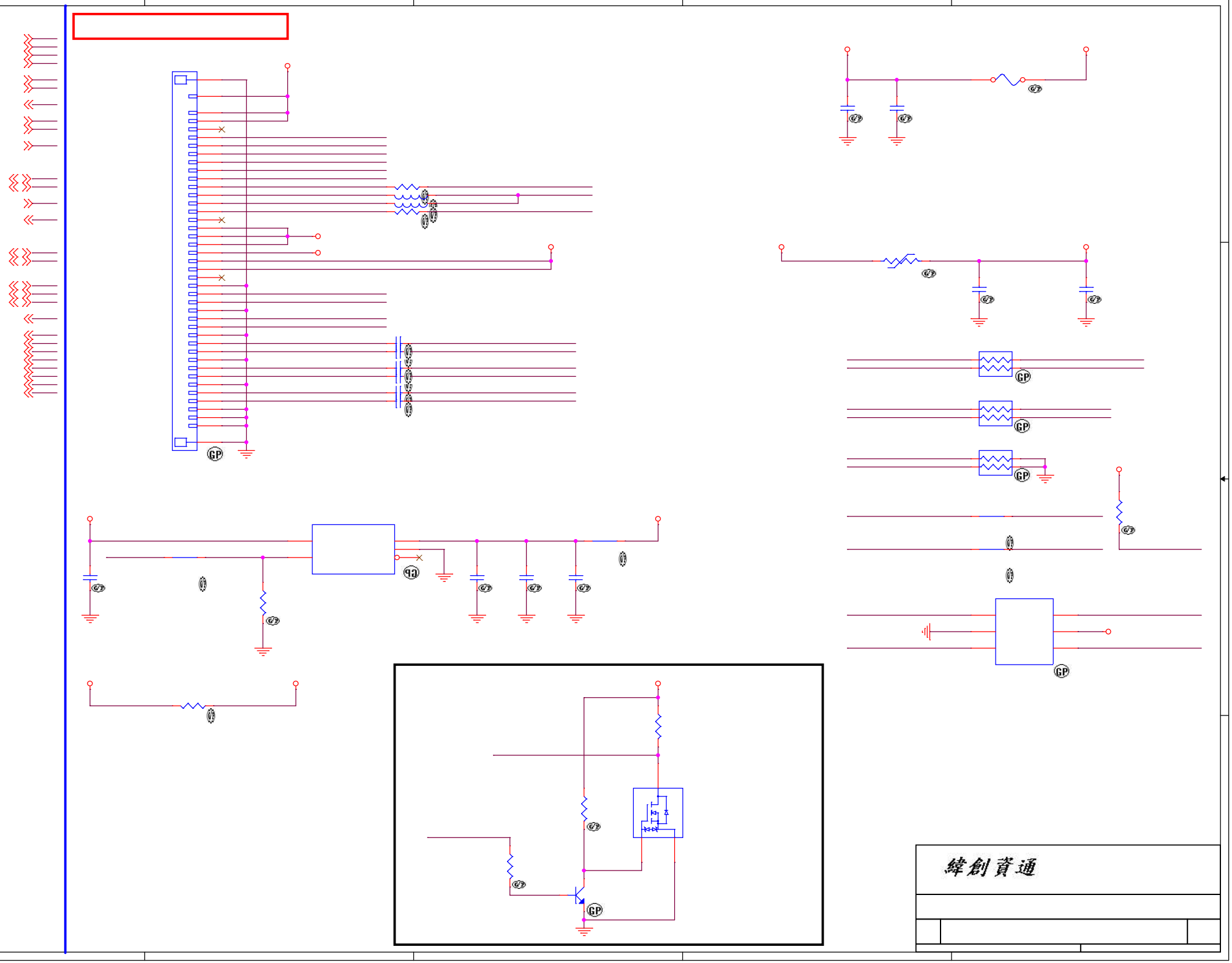
SSID = PWR.Plane.Regulator_1D8V



緯創資通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Blanking

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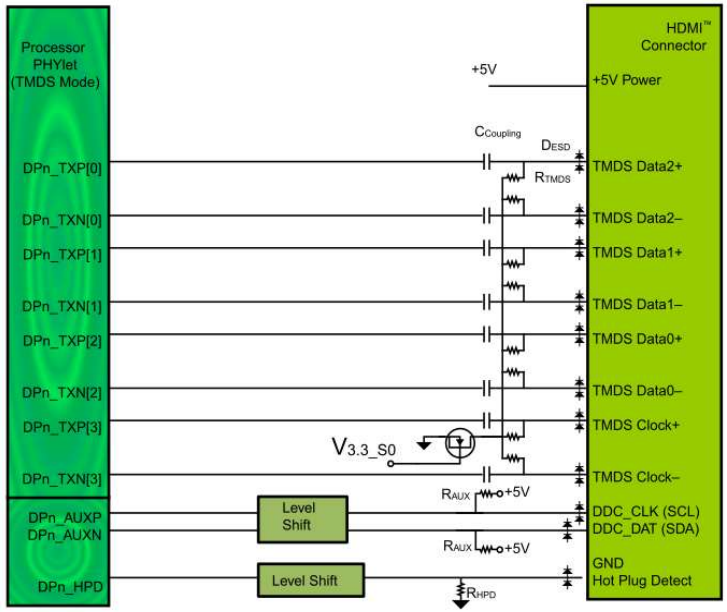

Figure 79. Schematic Diagram—HDMI™ Interface

Table 62. Component Table—Display Interface to HDMI™ Connector

Ref	Value	Tolerance	Package	Comments
$C_{Coupling}$	100 nF	10%	0402	Allowable Range: 75 to 200 nF Recommended Value: 100 nF Place as pairs[1, 2]
R_{TMDS}	499Ω	1%	0402	Value includes R_{DS-ON} of FET
R_{Aux}	2.2 kΩ (can be part of Level Shift circuit)	5%	0402	Pull-up resistor to +5 V
R_{HPD}	100 kΩ	5%	0603	VSS
D_{ESD}[3]	8 kV	–	–	Required: ESD-specific device placed close to the connector. See Layout Guidelines—DisplayPort ML to DVI or HDMI Connector for details.
FET	–	–	SOT-23	$R_{DS-ON\ (max)}$ = 20Ω, $V_{GS-TH\ (max)}$ = 4 V

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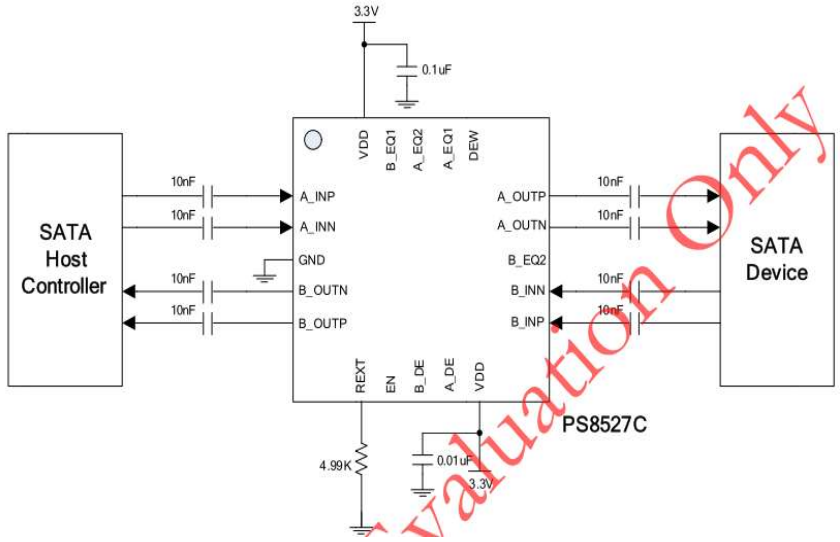

9	A_DE	I	Programmable output de-emphasis level setting for channel A. Internally tied to VDD/2(M status). A_DE / De_Emphasis M / -3.5dB(Default) L / 0dB H / -6dB

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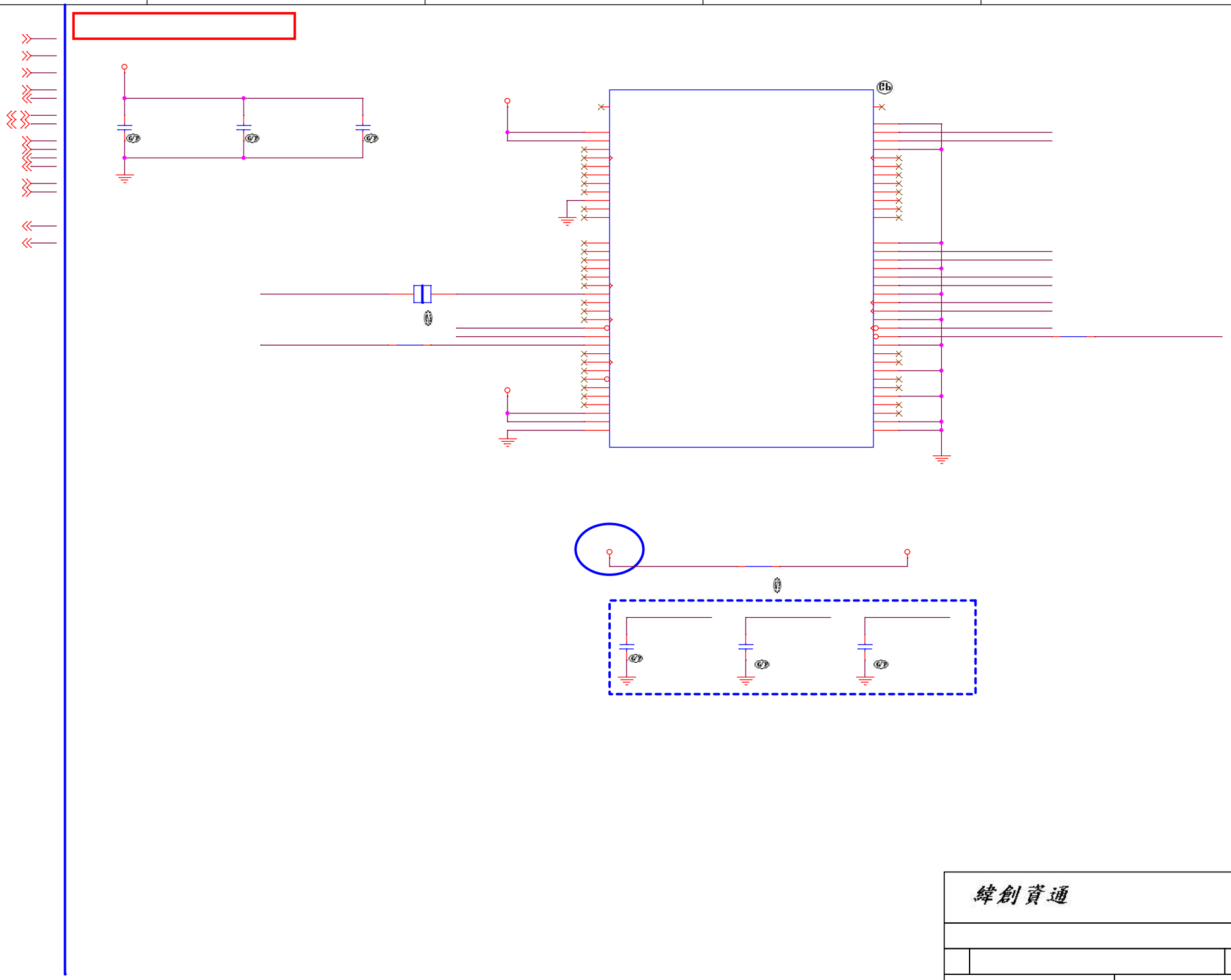
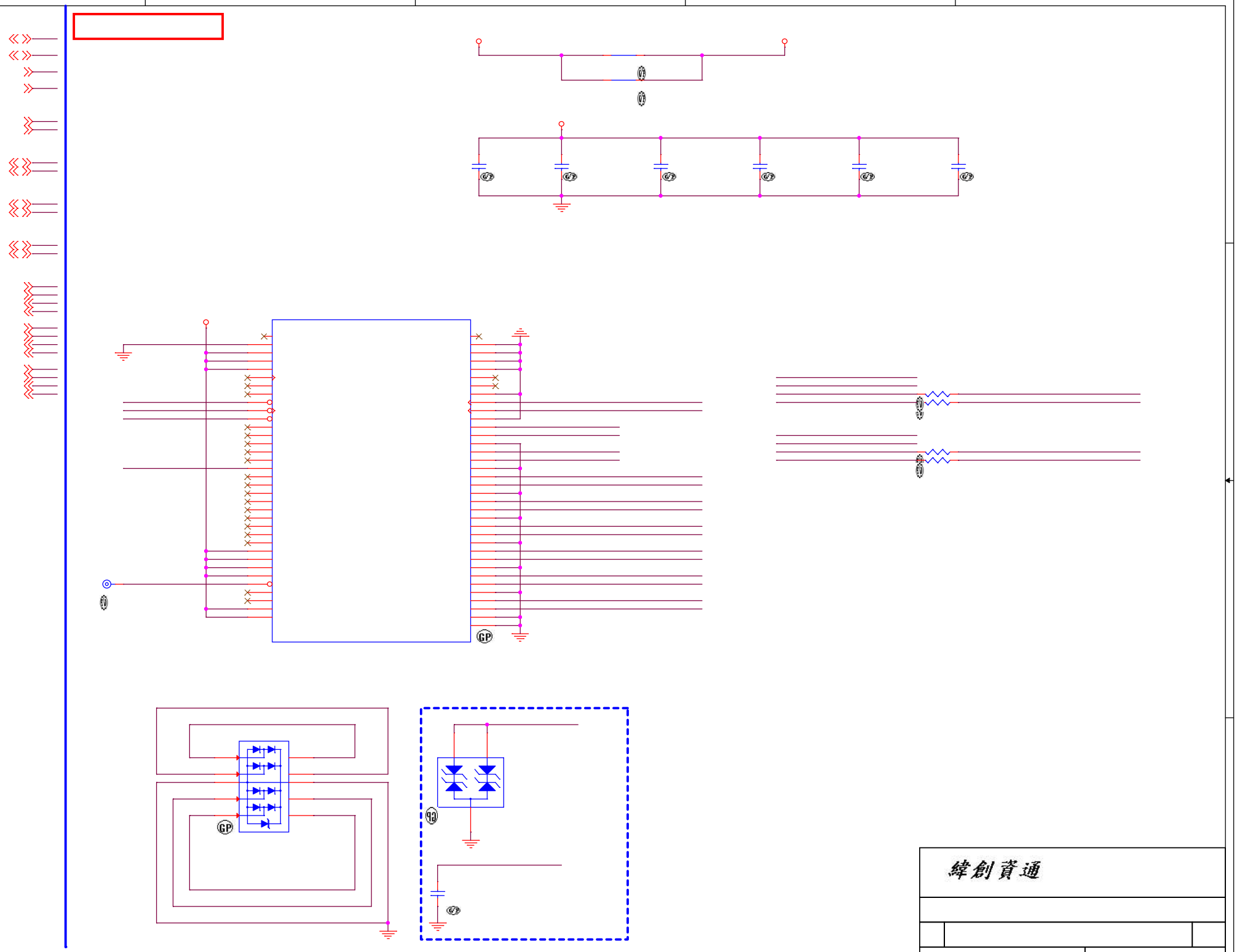


緯創資通

Blanking

緯創資通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GP
GP
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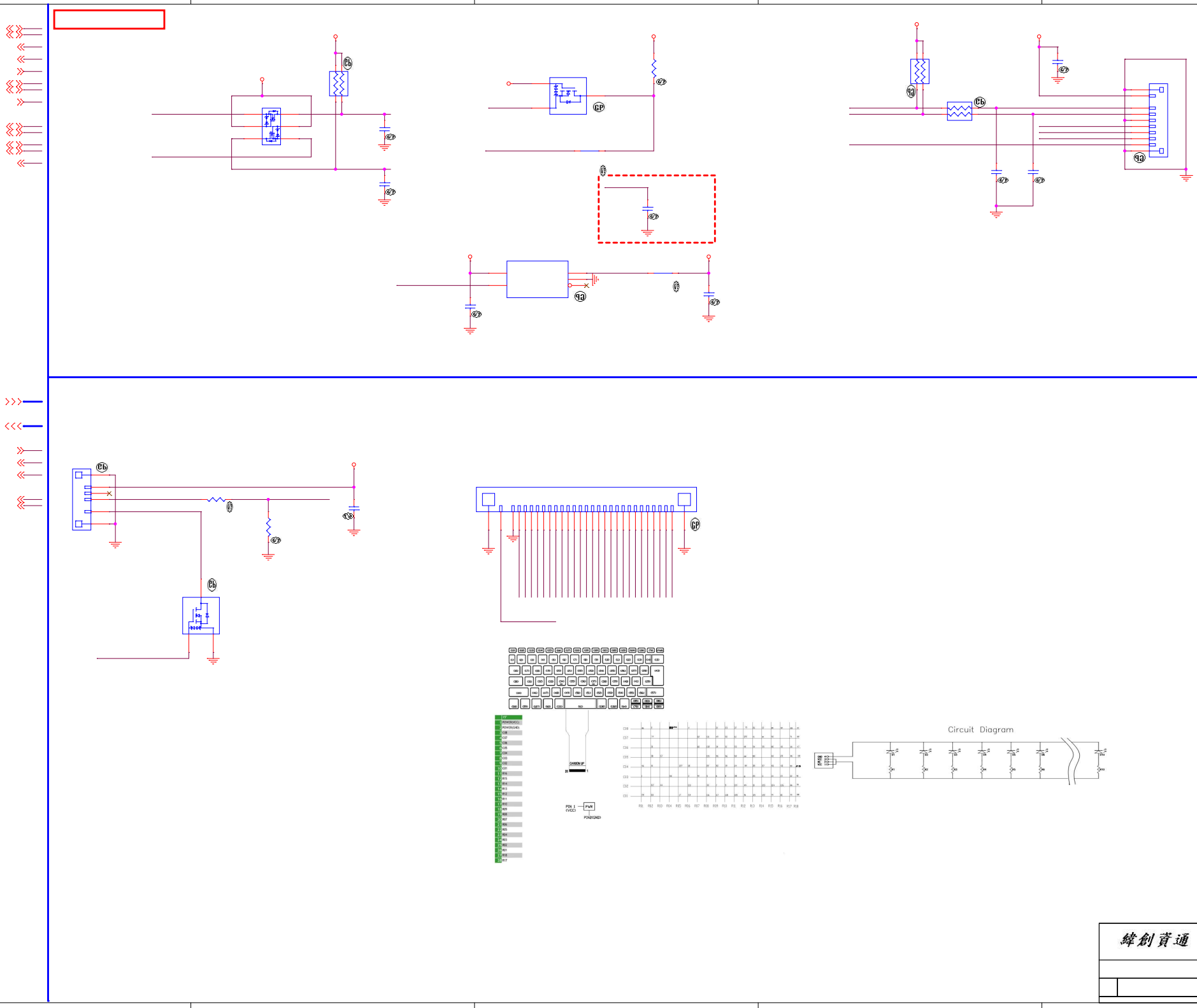
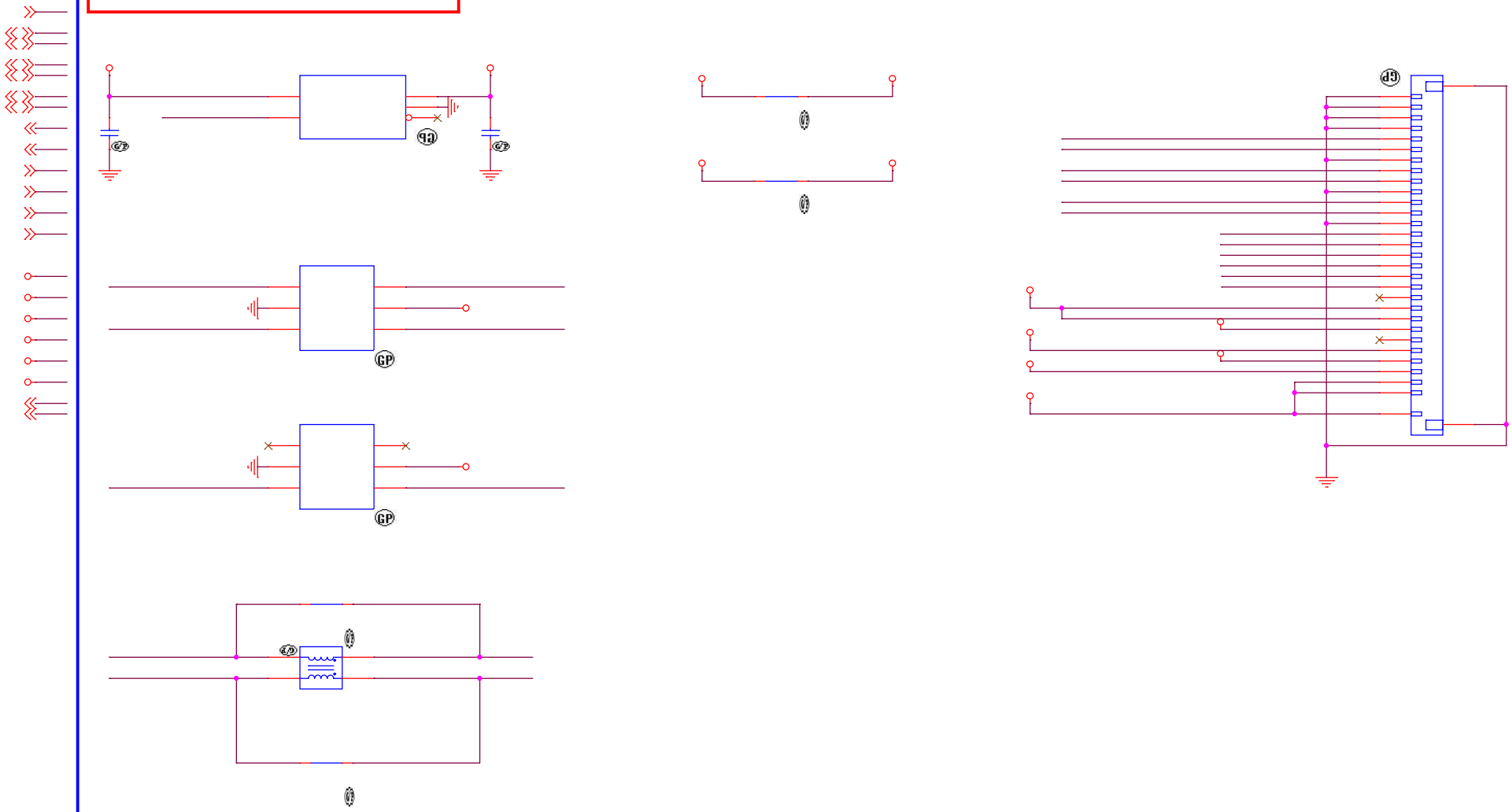
Blanking

緯創資通



緯創資通



緯創資通

Blanking

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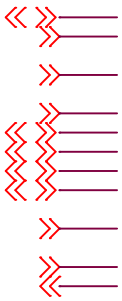

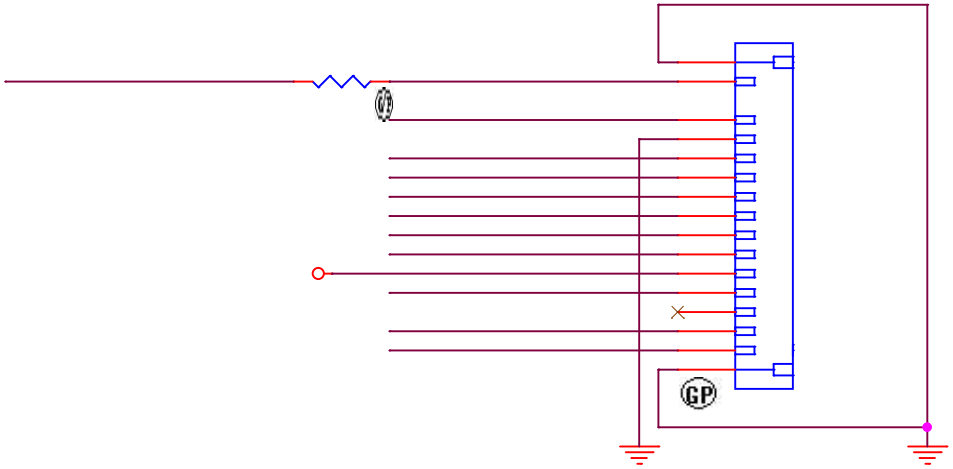

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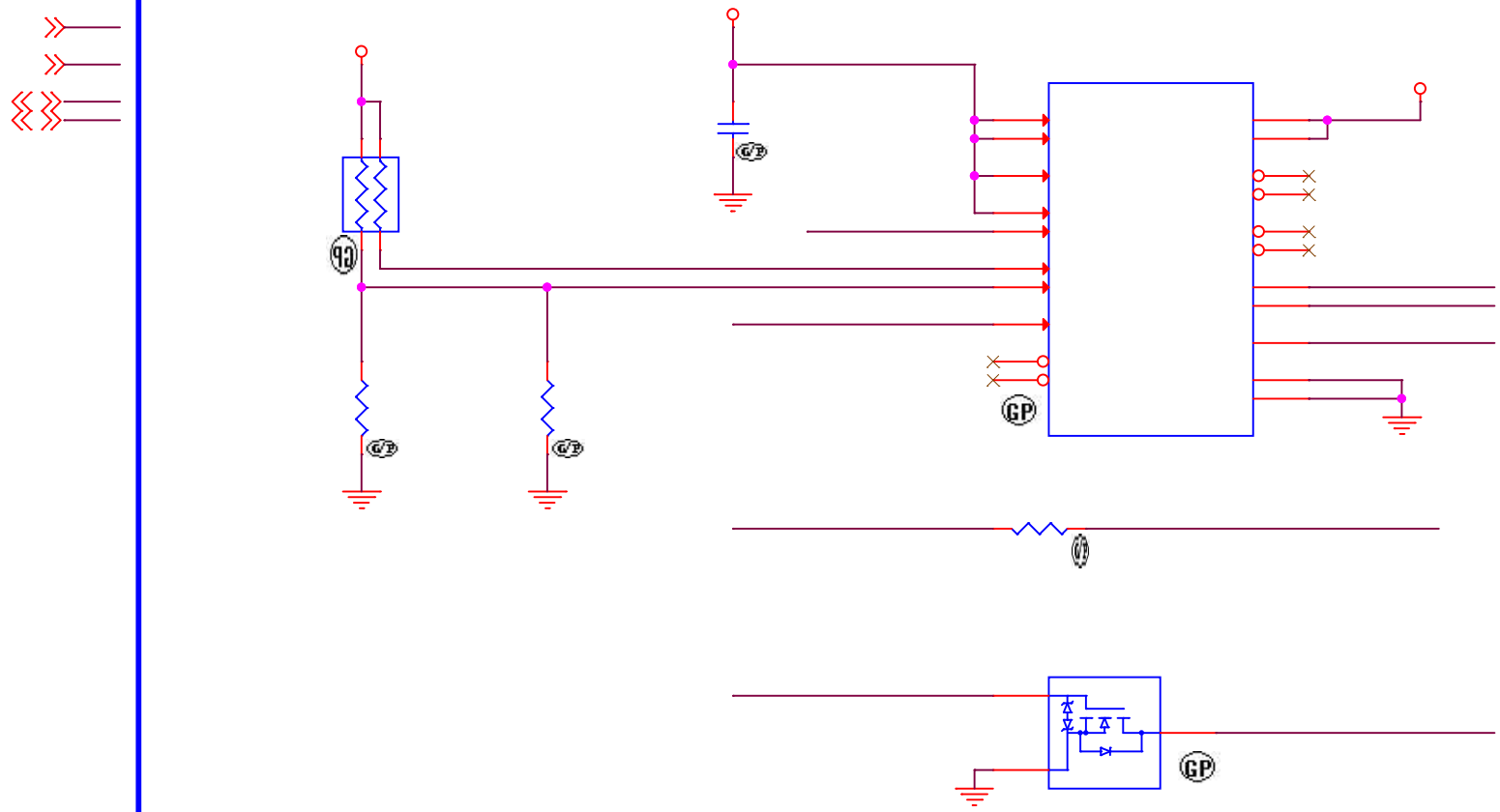

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

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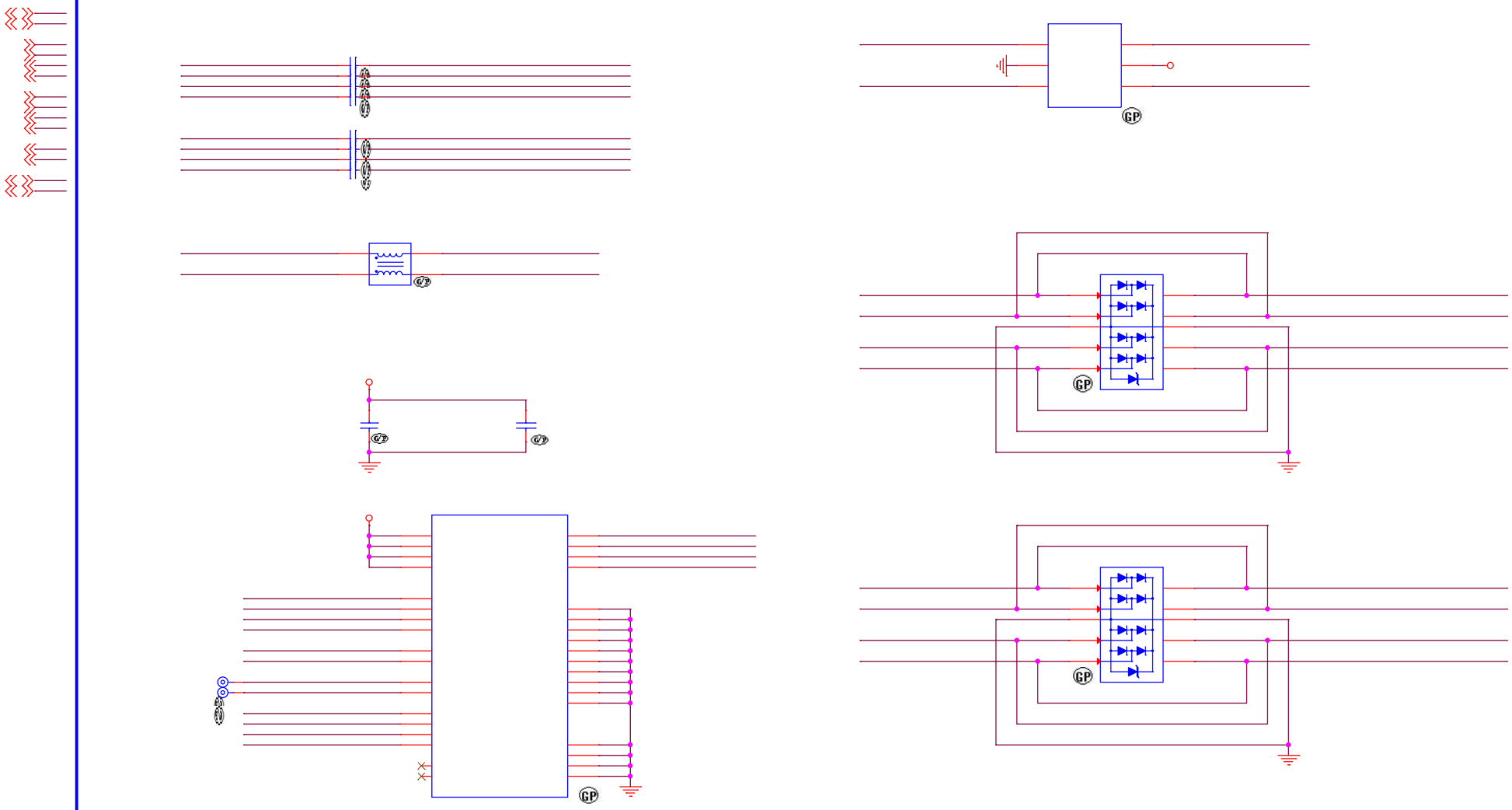

緯創資通

Blanking

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Blanking

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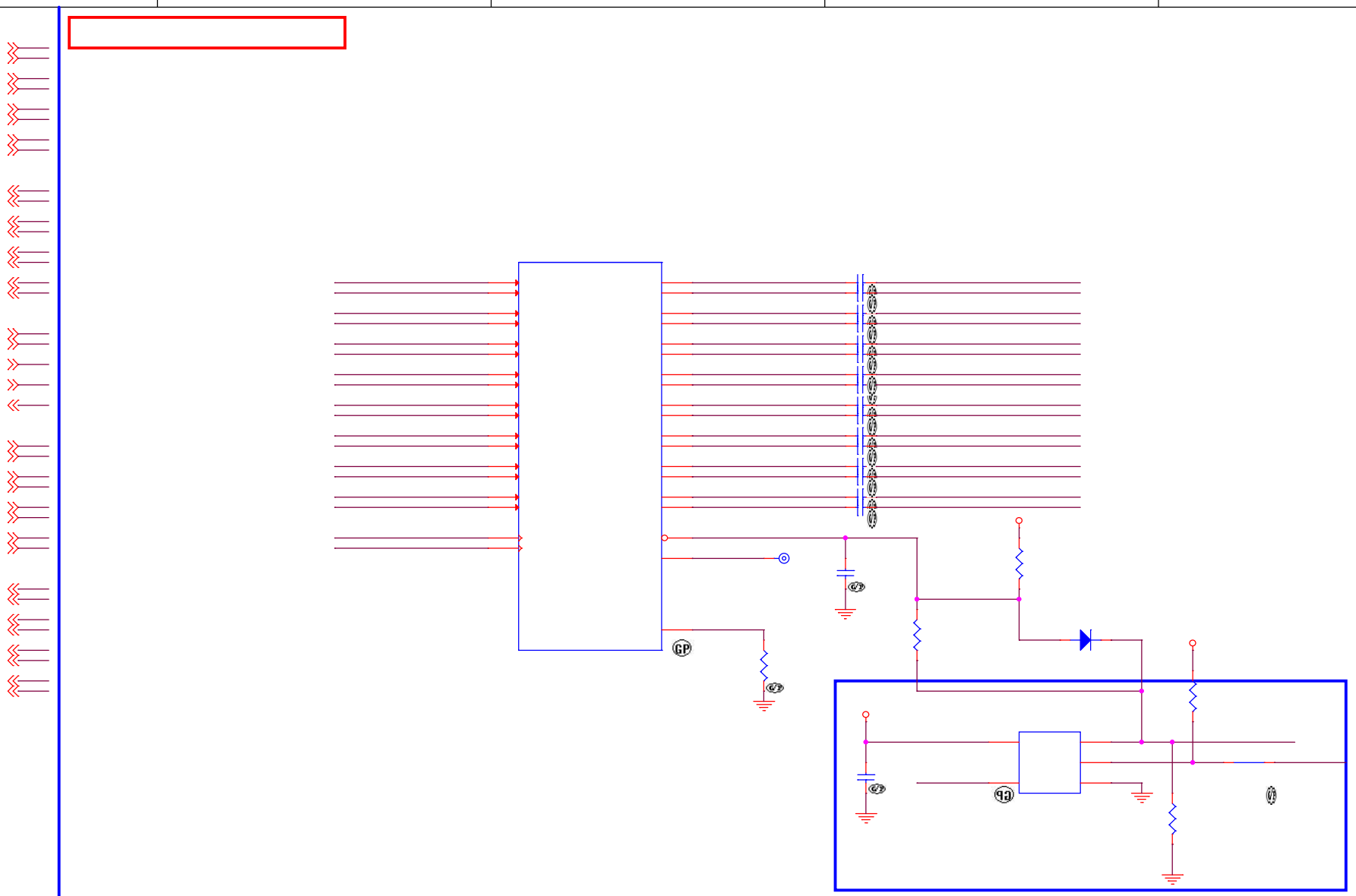
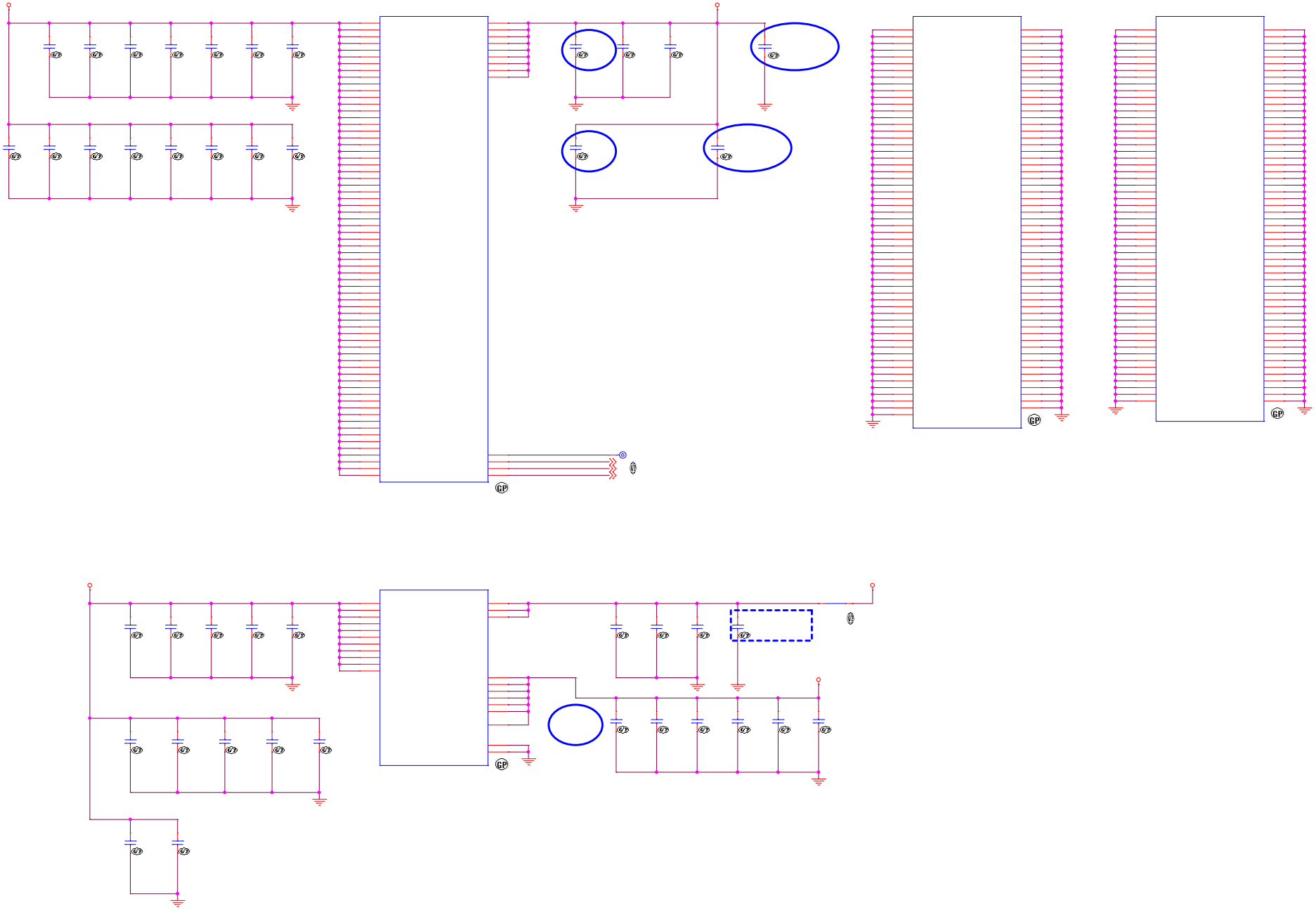
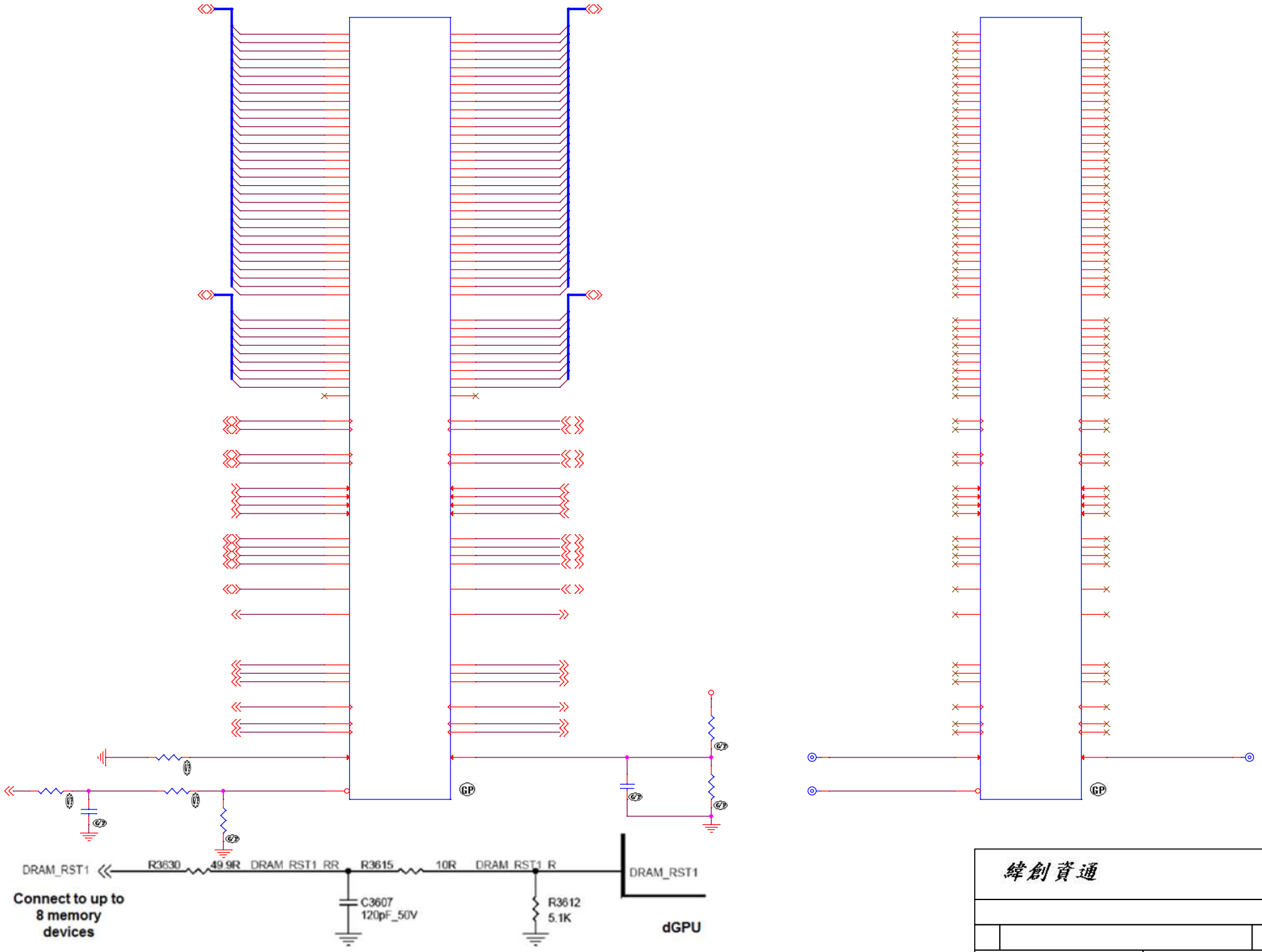


緯創資通



緯創資通


DRAM_RST1
R3630
49.9R
DRAM_RST1_RR
R3615
10R
DRAM_RST1_R
DRAM_RST1
Connect to up to 8 memory devices
C3607
120pF_50V
R3612
5.1K
dGPU
GP
GP
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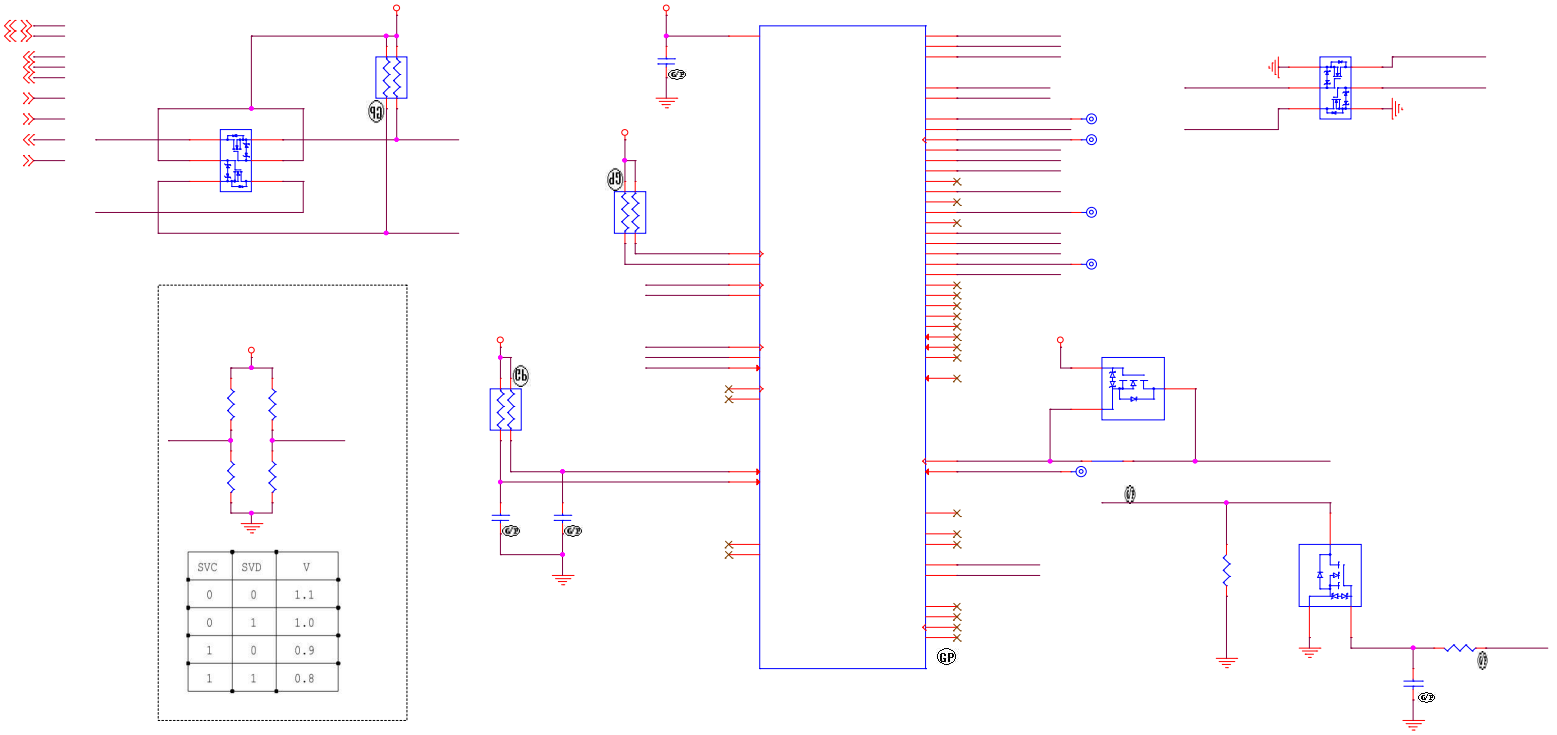
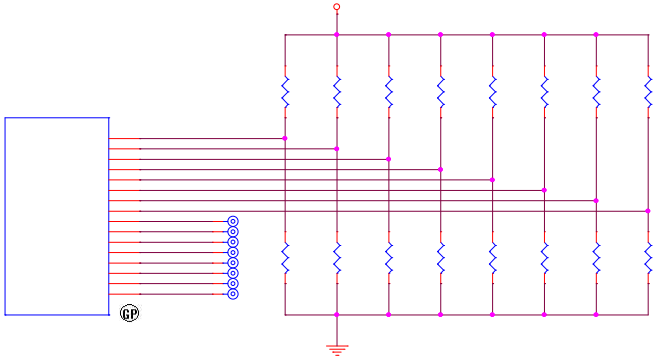
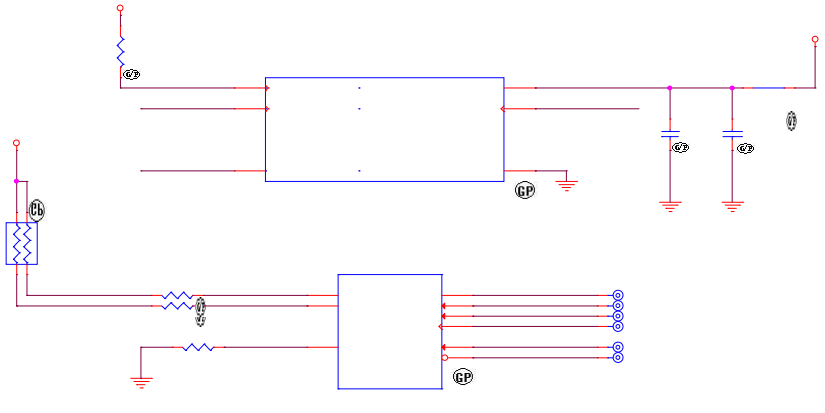


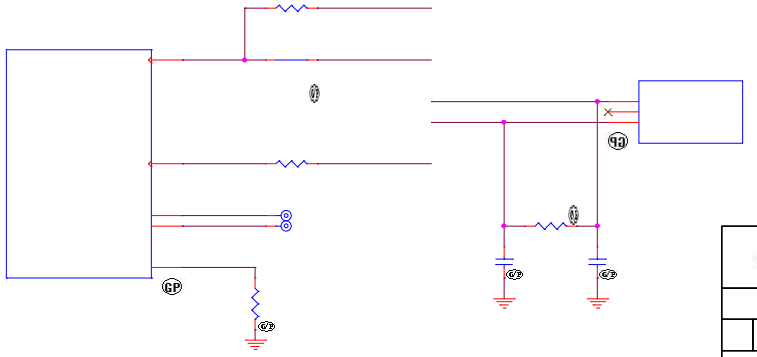
SVC	SVD	V
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

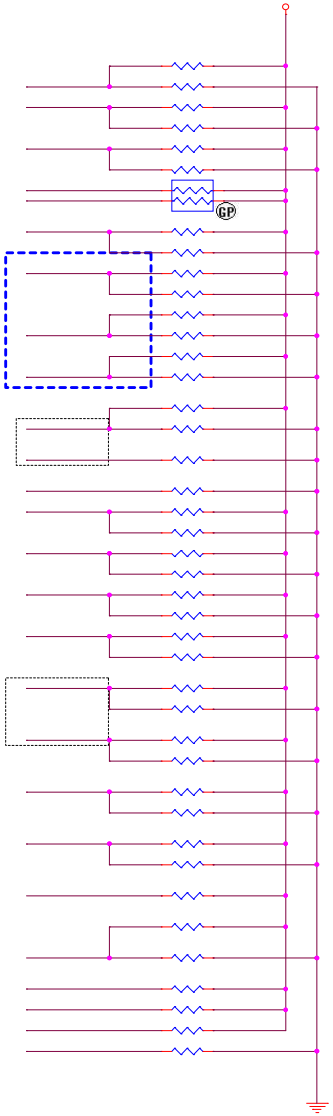


MLPS Memory ID setting:

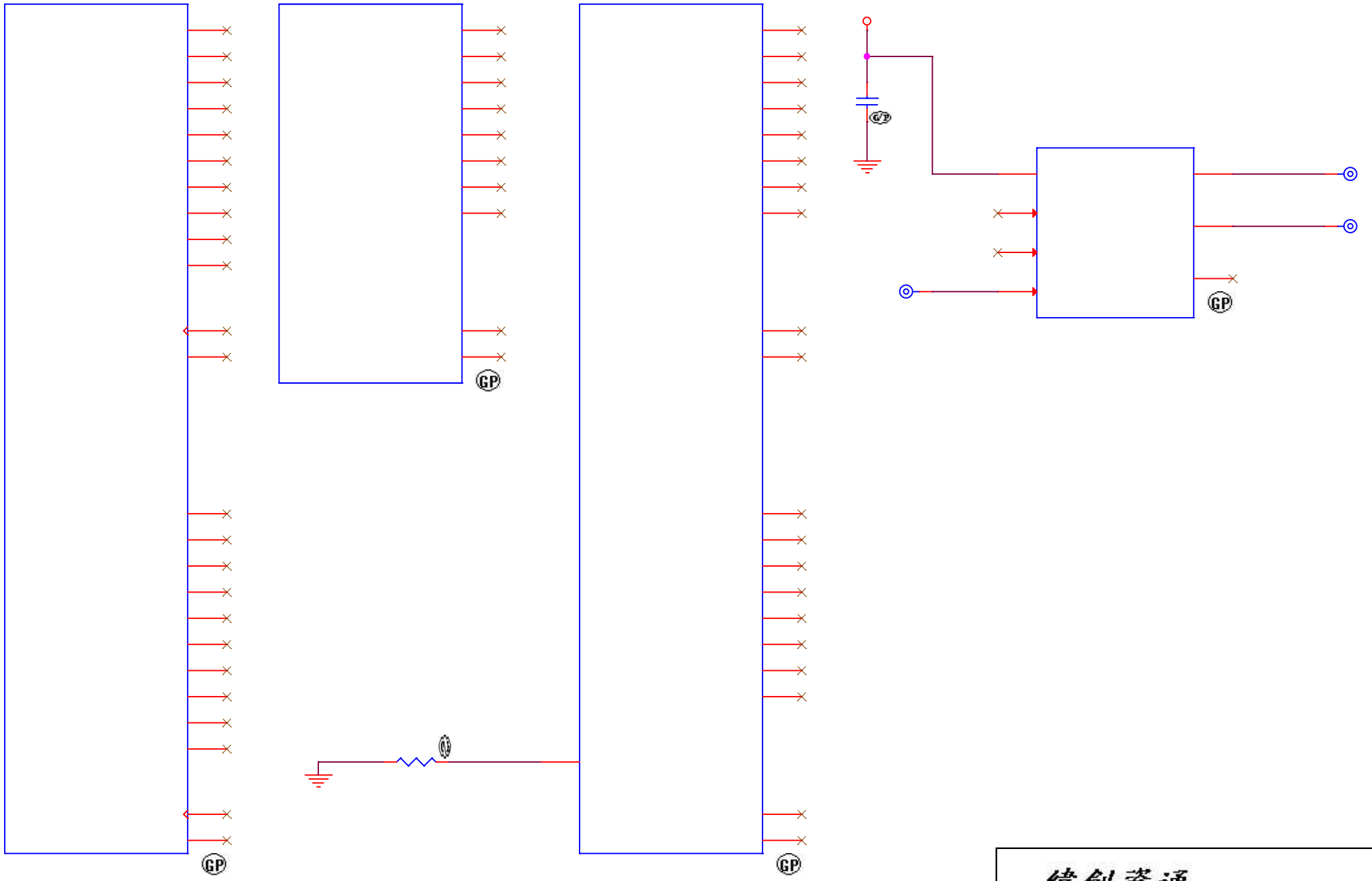
BOARD_CONFIG[2:0] =DBGDATA 5/4/3		Memory Type	Configuration	Speed	Die	hannel Siz	Vendor P/N	Voltage	SMT quantity
ID	[2:0]	EX: Samsung-GDDR5	256M × 32 4PCS,	8.0 Gbps	B-die	4GB	K4G80325FB-HC25	1.55 V	4 pcs
0	000								
1	001	SK hynix-GDDR5	256M × 32 2PCS	6.0 Gbps	A-die	2GB	H5GC8H24AJR-R0C	1.35V	2 pcs
2	010	SK hynix-GDDR5	256M × 32 2PCS	5.0 Gbps	M-die	2GB	H5GC8H24MJR-T2C	1.35V	2 pcs



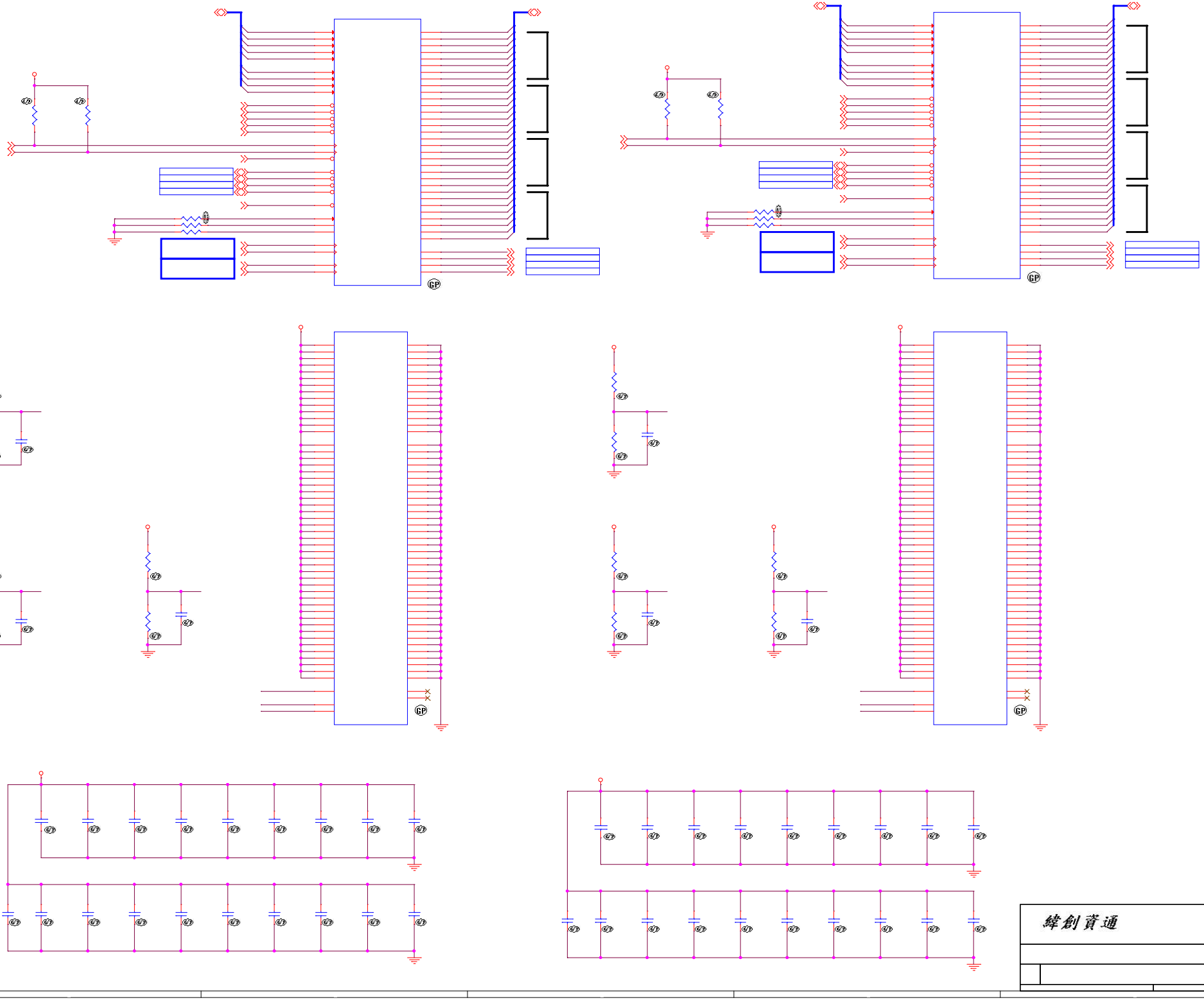




緯創資通



緯創資通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Blanking

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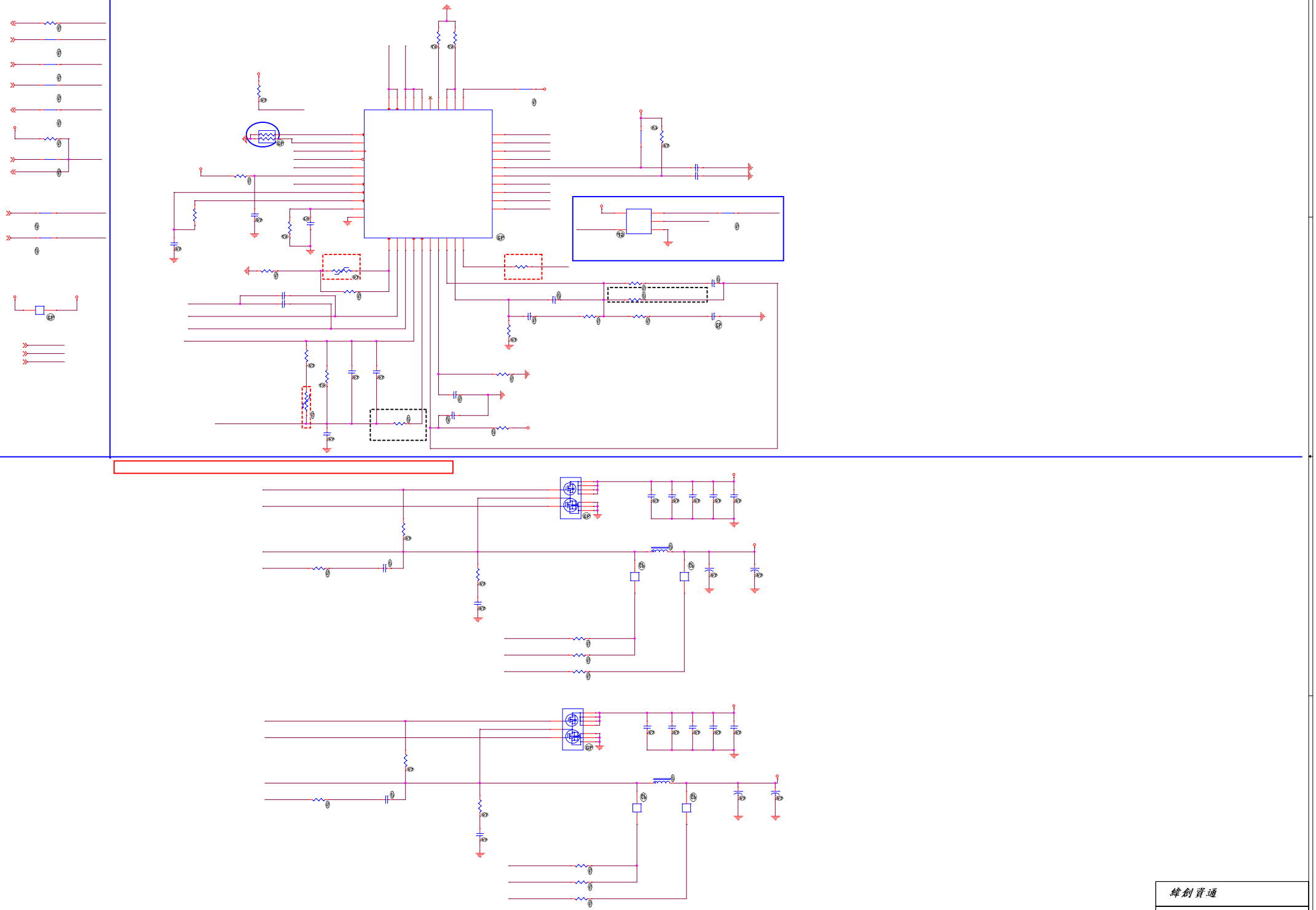
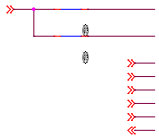
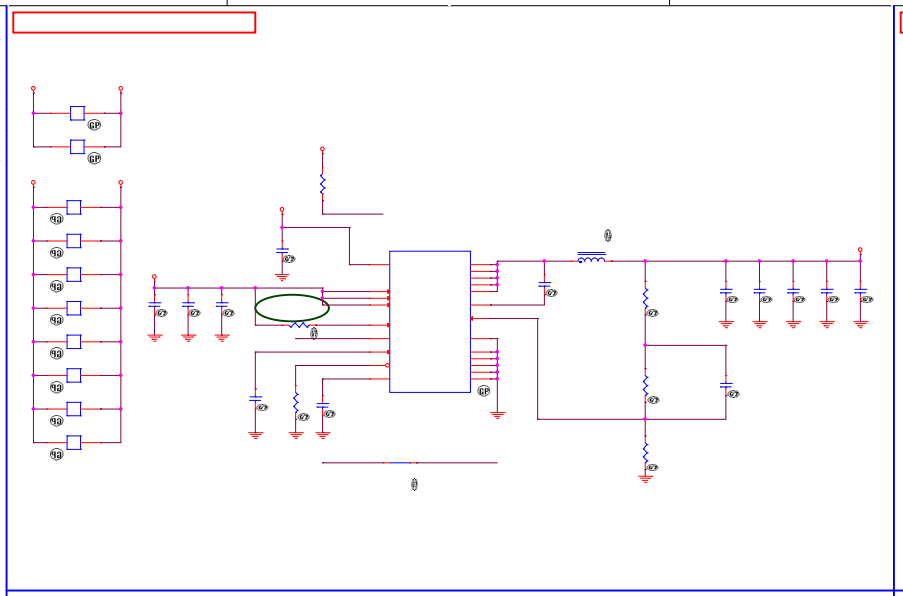
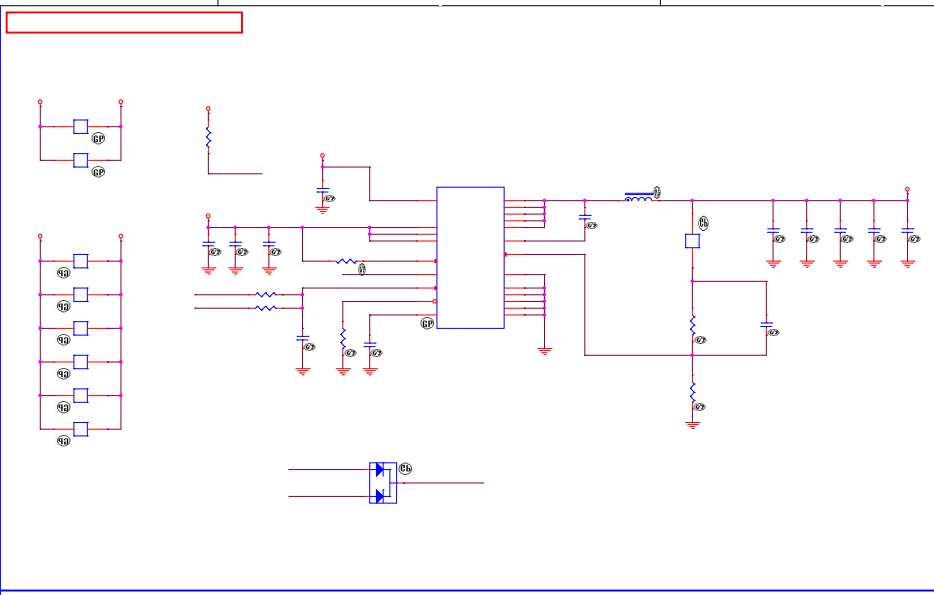
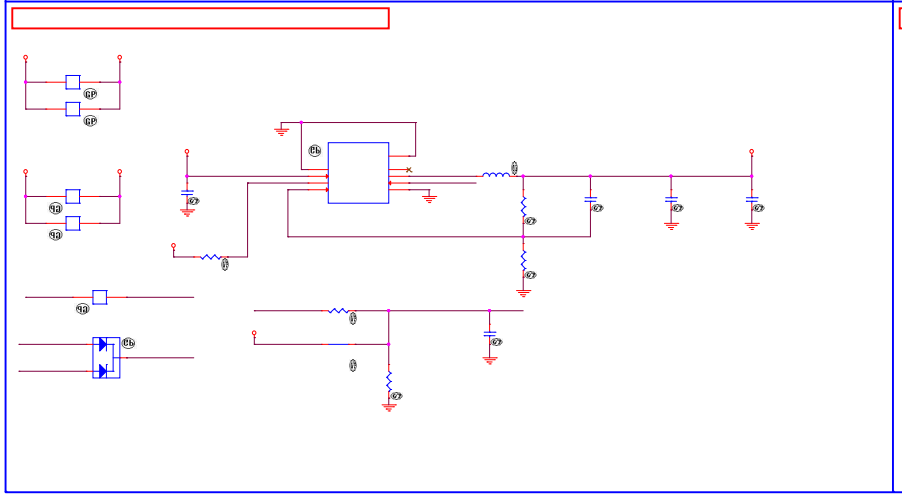


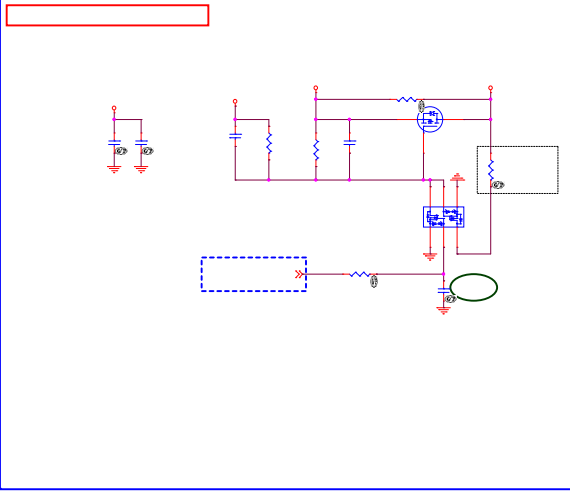
緯創資通











"R19M-P25-50/R19M-P25-70/R19M-P18-50/R19M-M18-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

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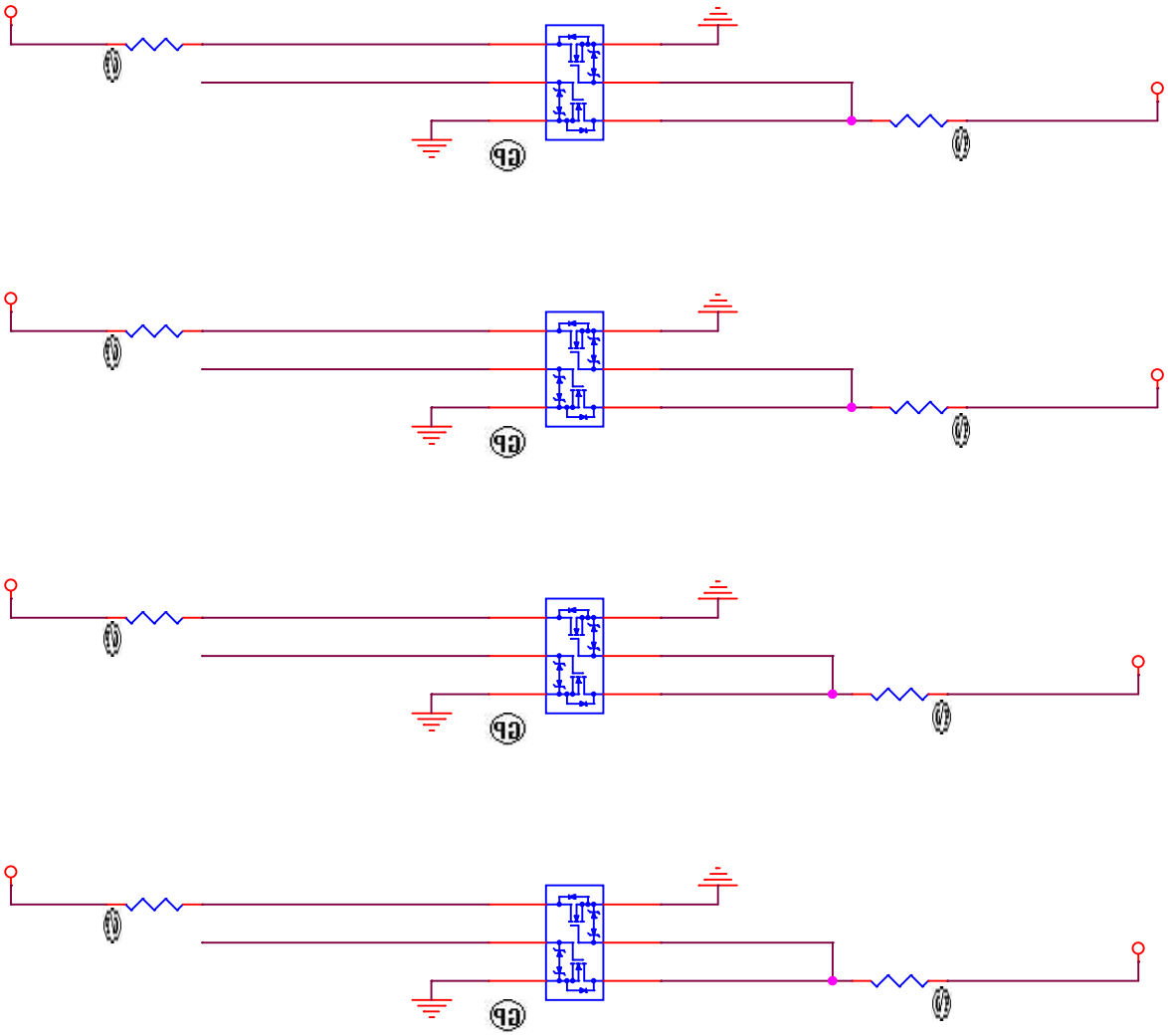

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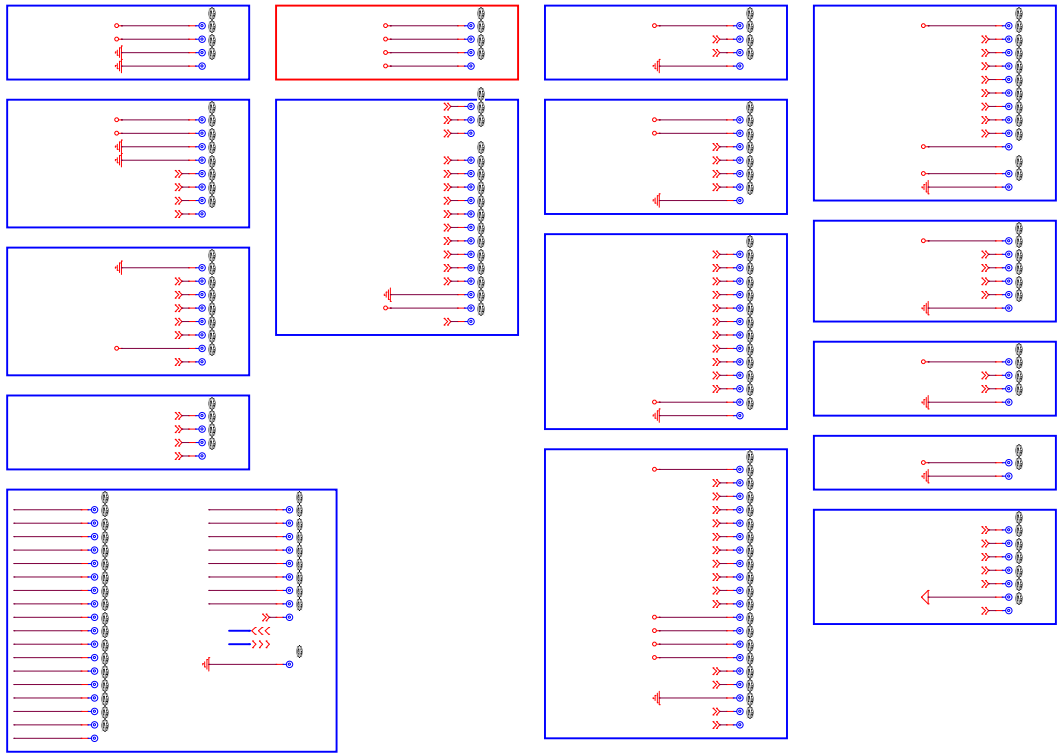

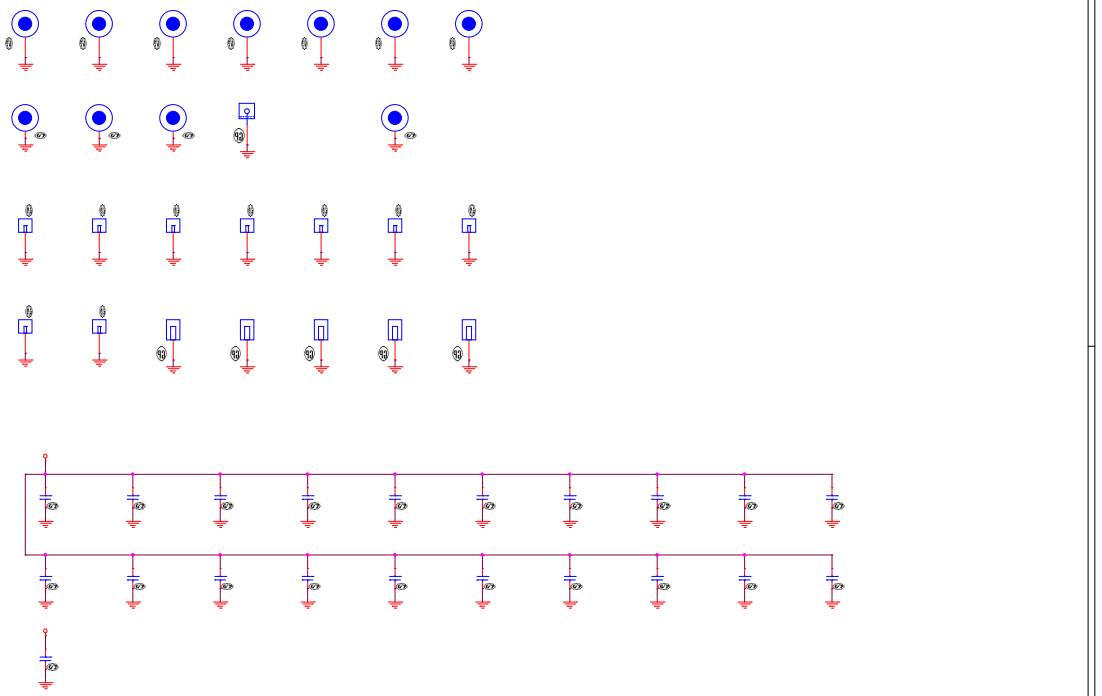

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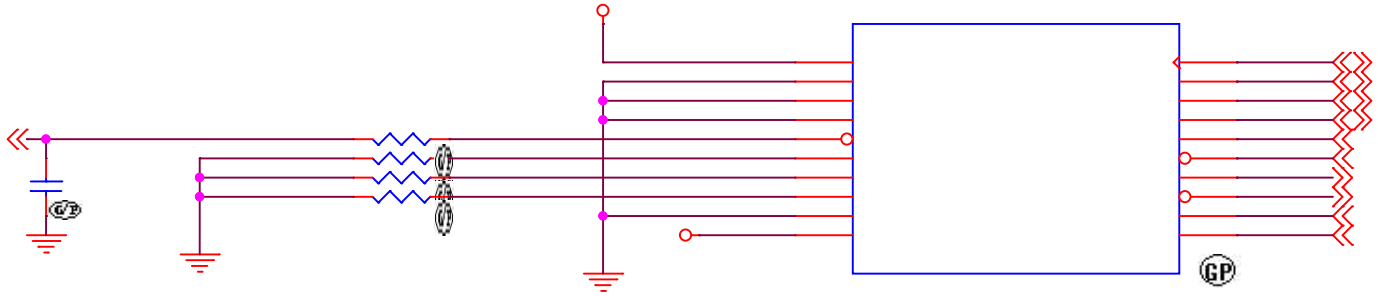

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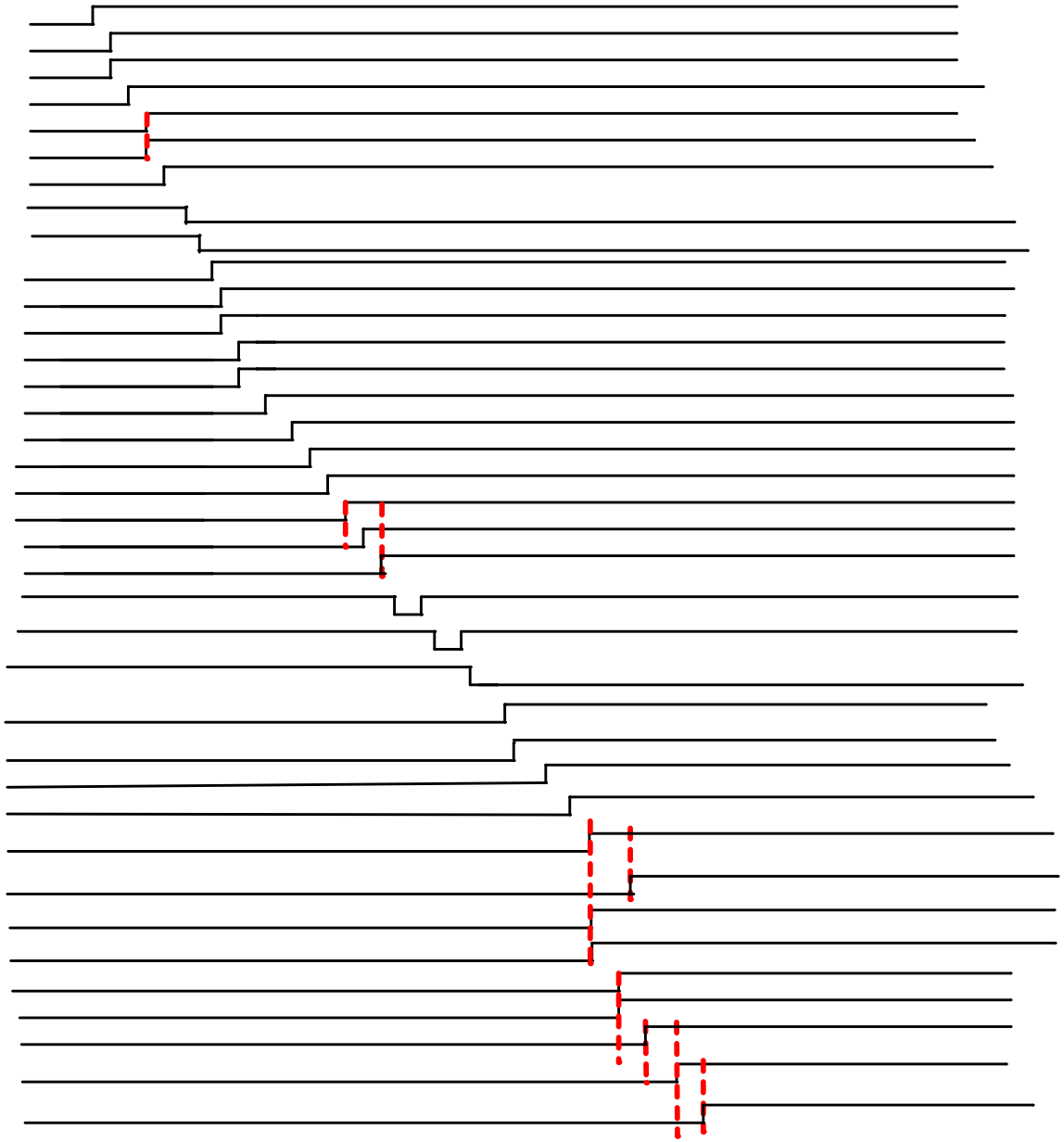
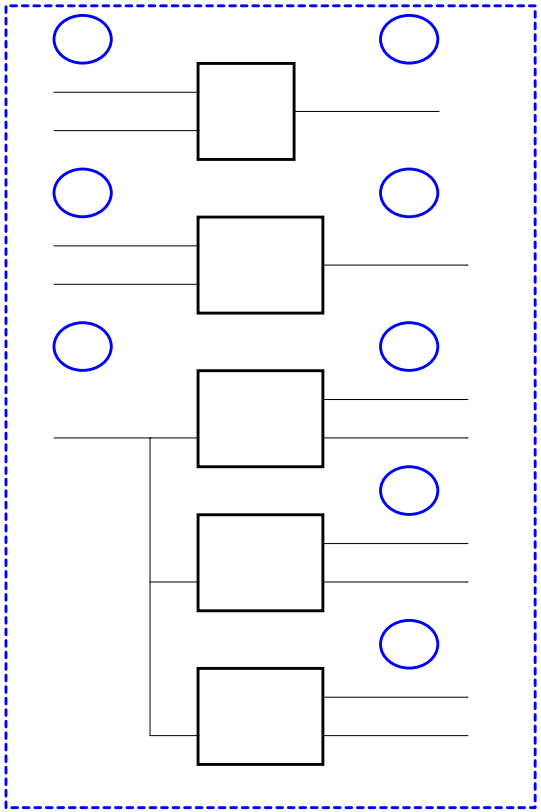
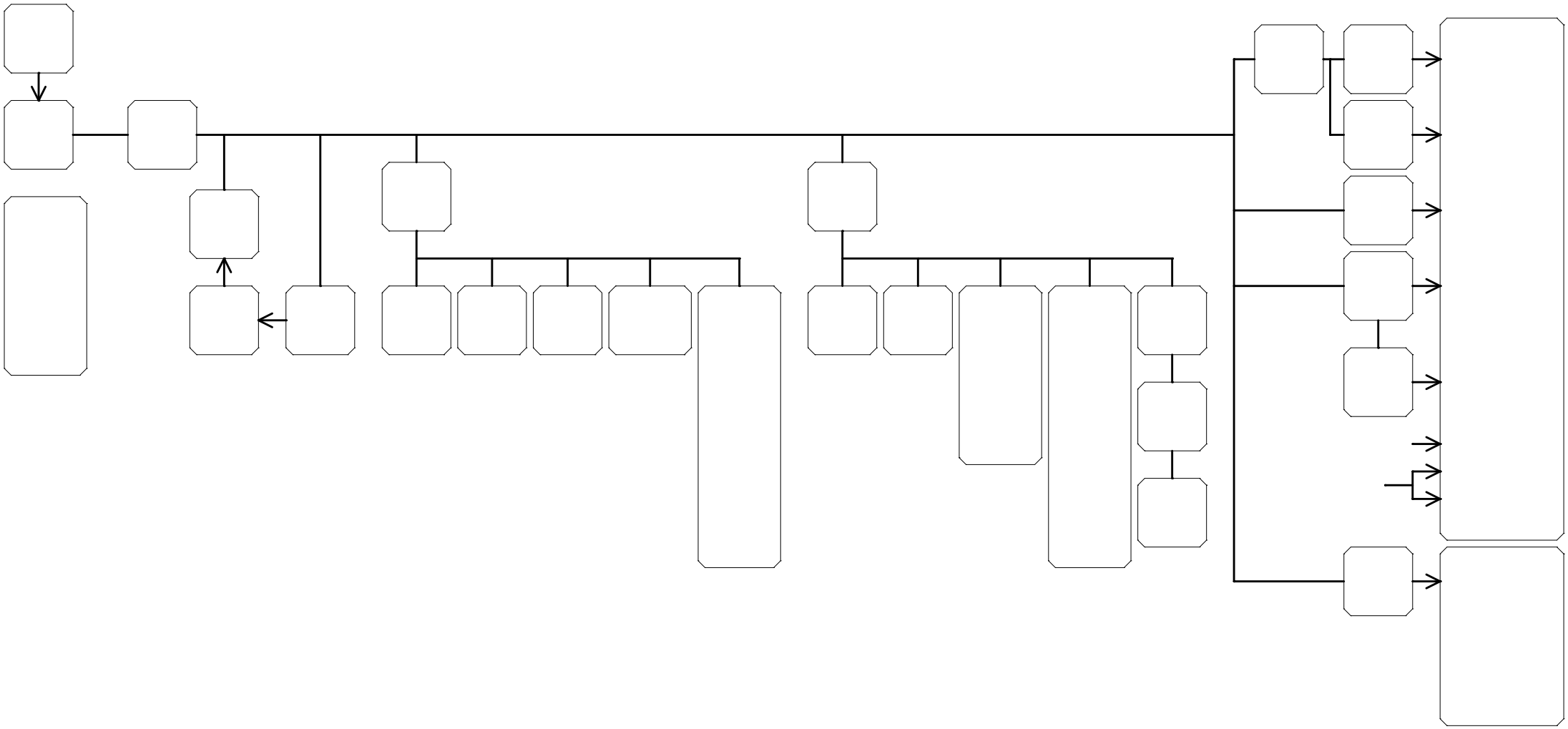
PRODUCT			CONFIGURATION									
MODEL	OPN	cTDP RANGE	CORES	THREADS	GPU CU	GPU Model	CPU CLK GHz (max/base)	GPU Clock MHz (max)	DID	RID	Processor Type[3]	Display Pipe
AMD Ryzen™ 7 3700U	2M370SC4T4MFB(ES) ZM370SC4T4MFG(PC) YM3700C4T4MFG(PR)	12-35w	4	8	10	AMD Radeon™ RX Vega 10 Graphics	4.0/2.3[8]	1400[5]	15D8	C1	Type1	4
AMD Ryzen™ 5 3500U	ZM350SC4T4MFG(PC) YM3500C4T4MFG(PR)	12-35w	4	8	8	AMD Radeon™ Vega 8 Graphics	3.7/2.1[8]	1200[5]	15D8	C2	Type1	4
AMD Ryzen™ 3 3300U	ZM330SC4T4MFG(PC) YM3300C4T4MFG(PR)	12-35w	4	4	6	AMD Radeon™ Vega 6 Graphics	3.5/2.1[8]	1200[5]	15D8	C3	Type1	4
AMD Ryzen™ 3 3200U	ZM320SC4T2OFG(PC) YM3200C4T2OFG(PR)	12-25w	2	4	3	AMD Radeon™ Vega 3 Graphics	3.5/2.6[8]	1200[5]	15D8	C4	Type2	3
AMD Athlon™ 300U[4]	ZM300SC4T2OFG(PC) YM300UC4T2OFG(PR)	12-25W	2	4	3	AMD Radeon™ Vega 3 Graphics	3.3/2.4[8]	1000[5]	15D8	C5	Type2	3

緯創資通

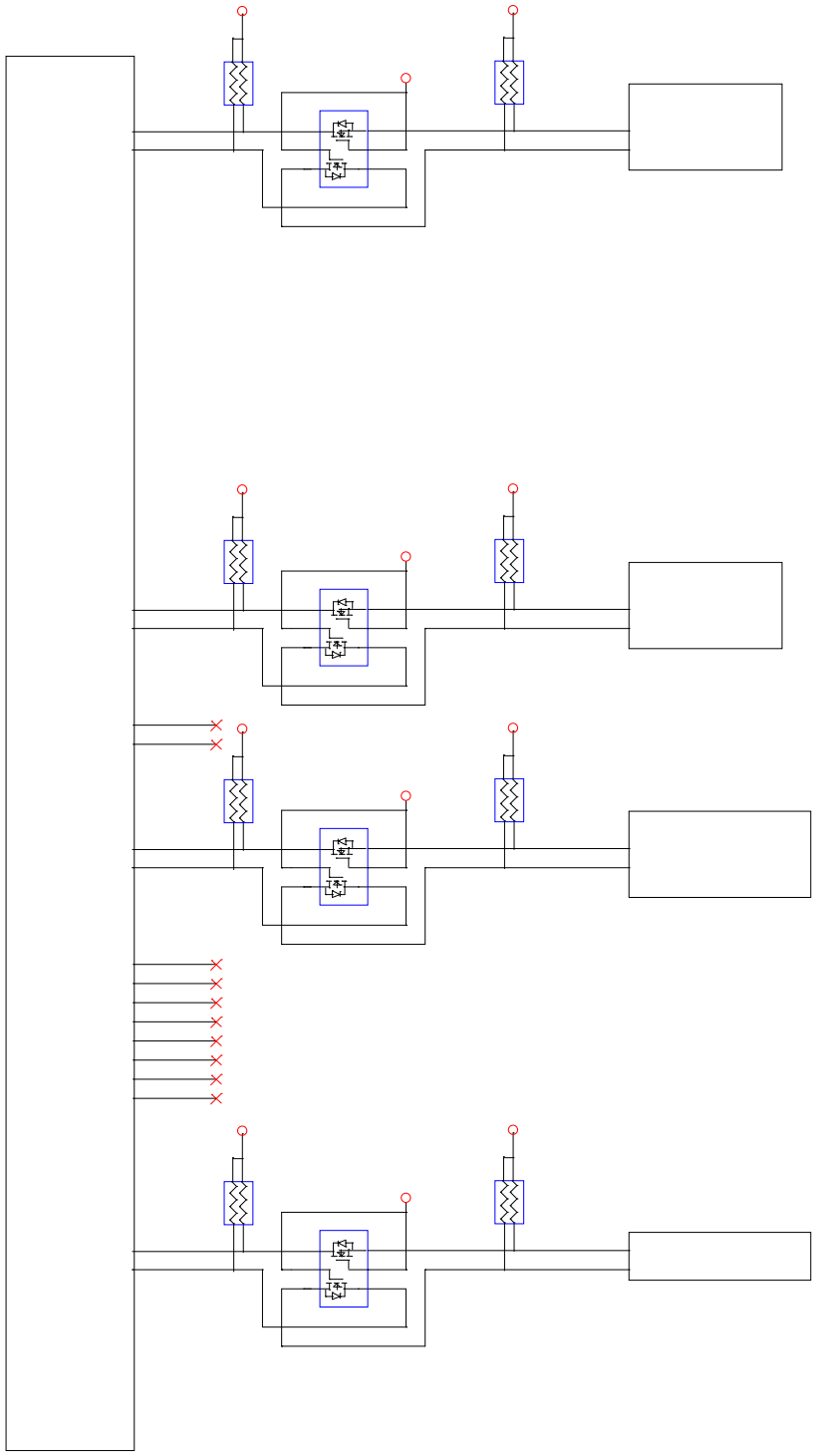


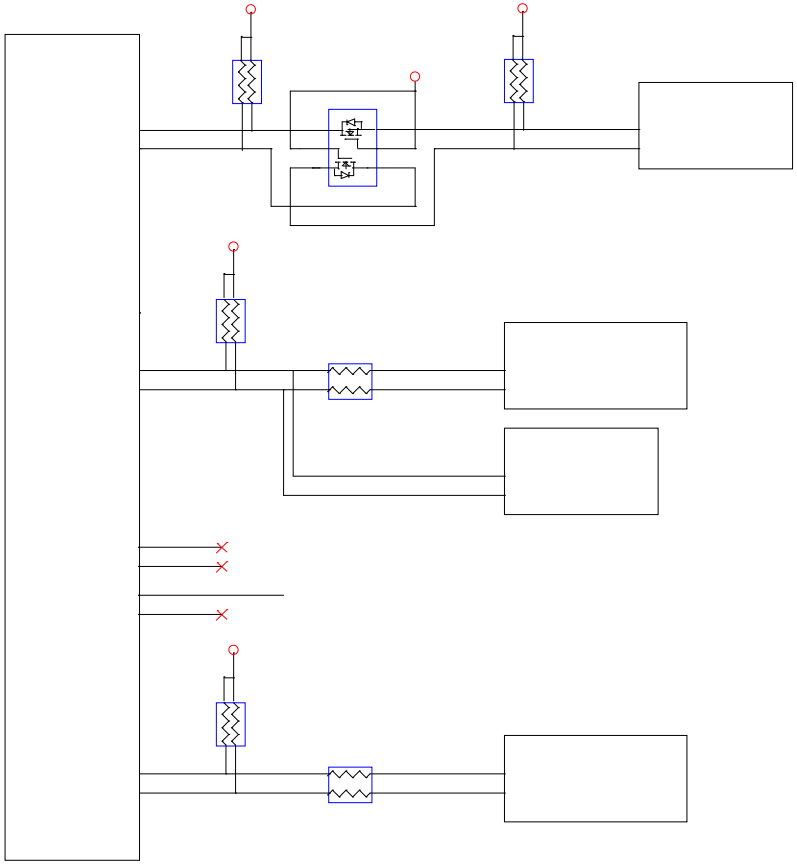


緯創資通



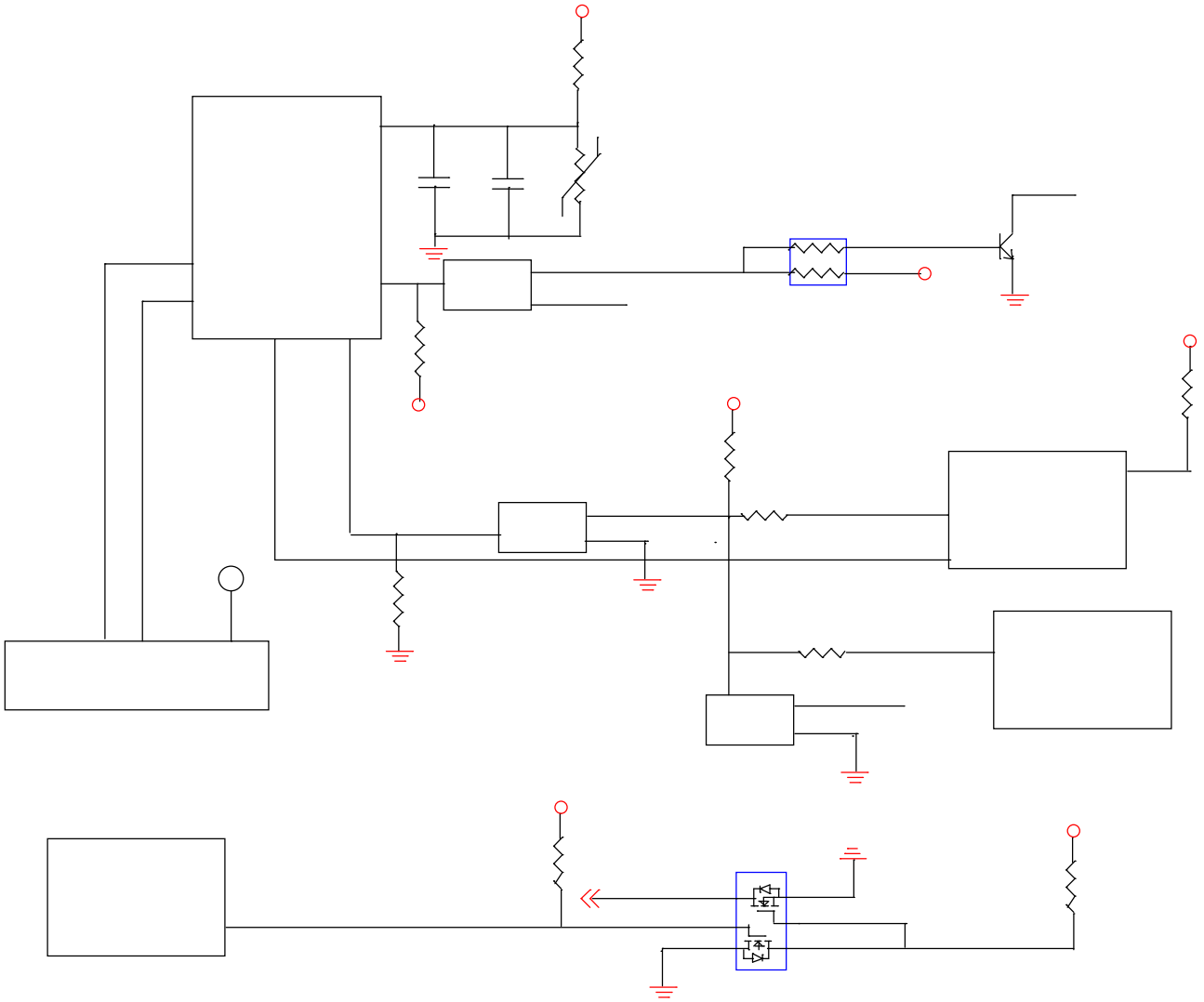
緯創資通



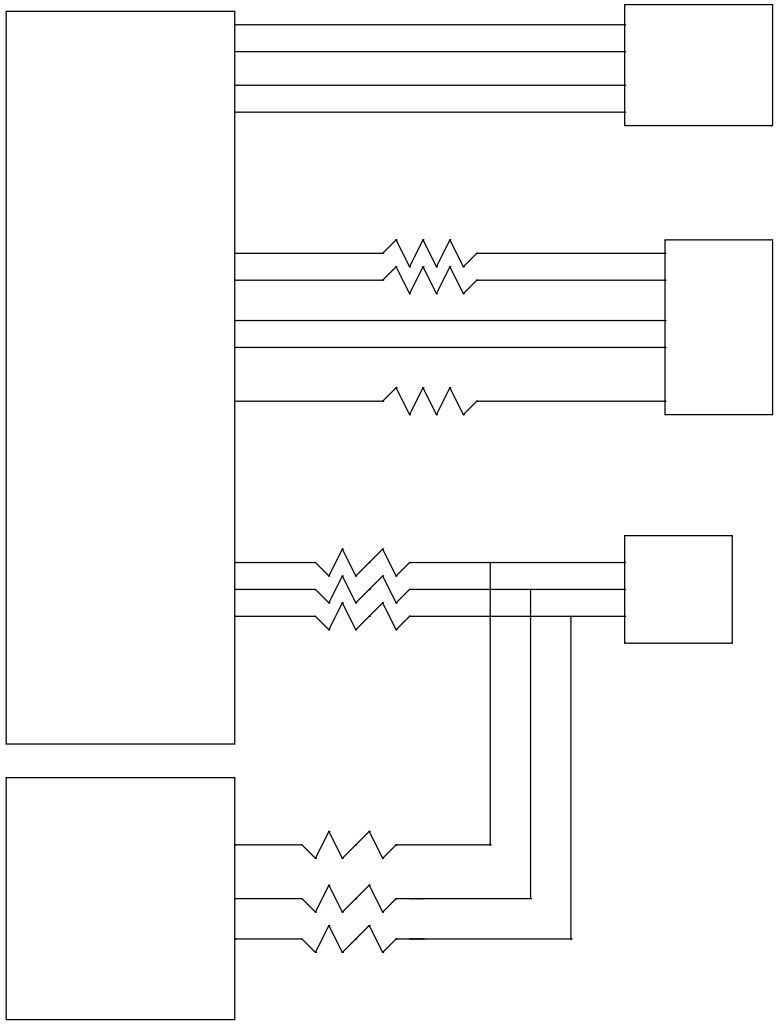


緯創資通

Thermal Block Diagram

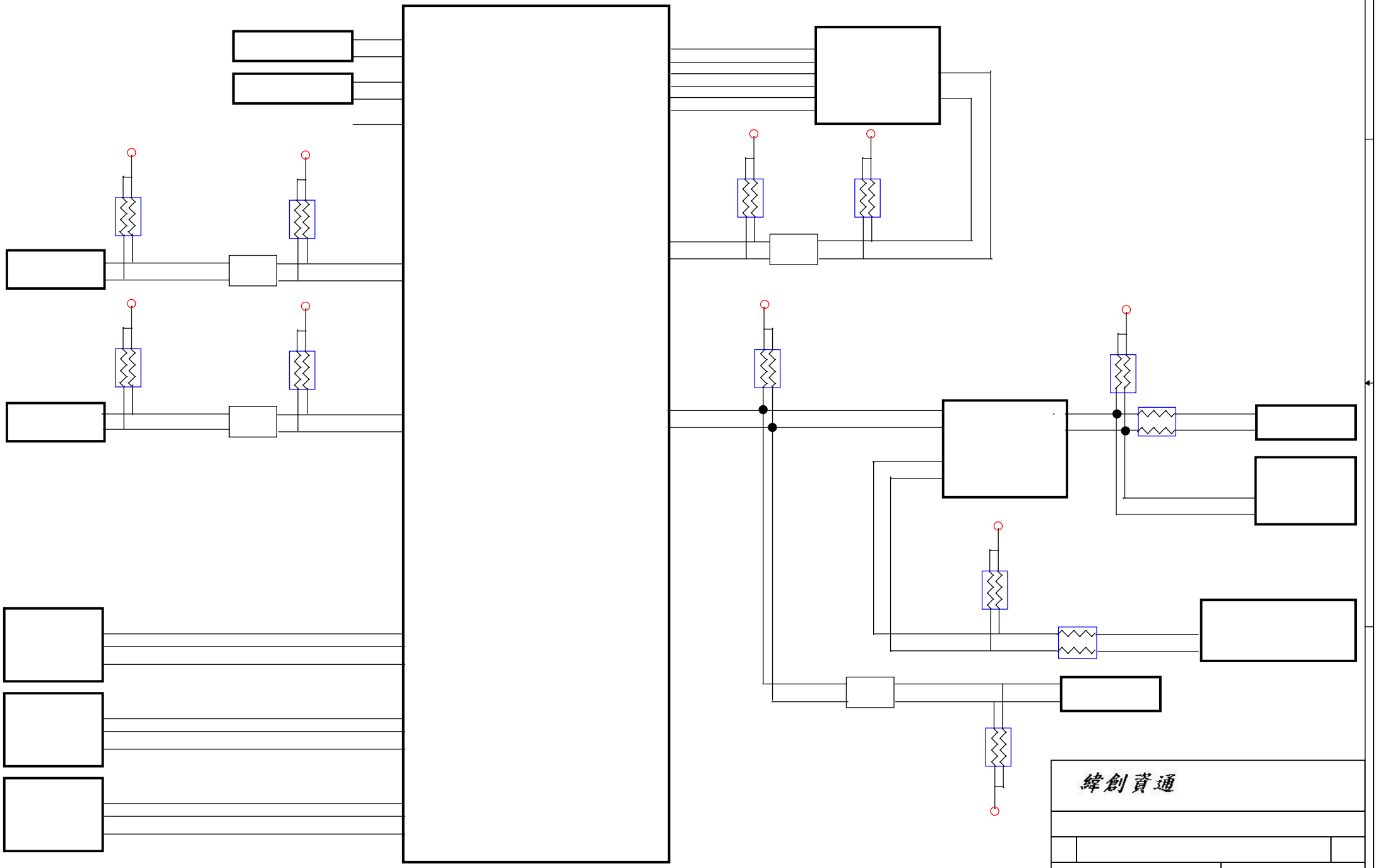


Audio Block Diagram



緯創資通

CLOCK BLOCK DIAGRAM



緯創資通