MS-7C89

ATX
Ver: 1.1

CML Platform

CPU:

Comet lake S 65W

System Chipset:

H410 PCH_V

Onboard Chip:

HD Audio Codec : ALC892
LAN : INTEL I219
SIO : NTC5887
Flash ROM: SPI 128 MB X1

VGA Output:

HDMI Port
DVI Port
VGA Port

Main Memory:

*DDRIV (2666MHz) * 2*

PWM:

IMVP8 -RT3607BC

ACPI:

LDO

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 1*
*M.2 Slot * 1*
*Intel WIFI * 1*

Other:

*SATA3.0 *4*
*PS2 * 1*
*REAL USB3.1 *2*
REAL USB2.0 LAN_USB
*FRONT USB3.1 *2*
*FRONT USB2.0 *4*

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Custom	Cover Sheet	1.1

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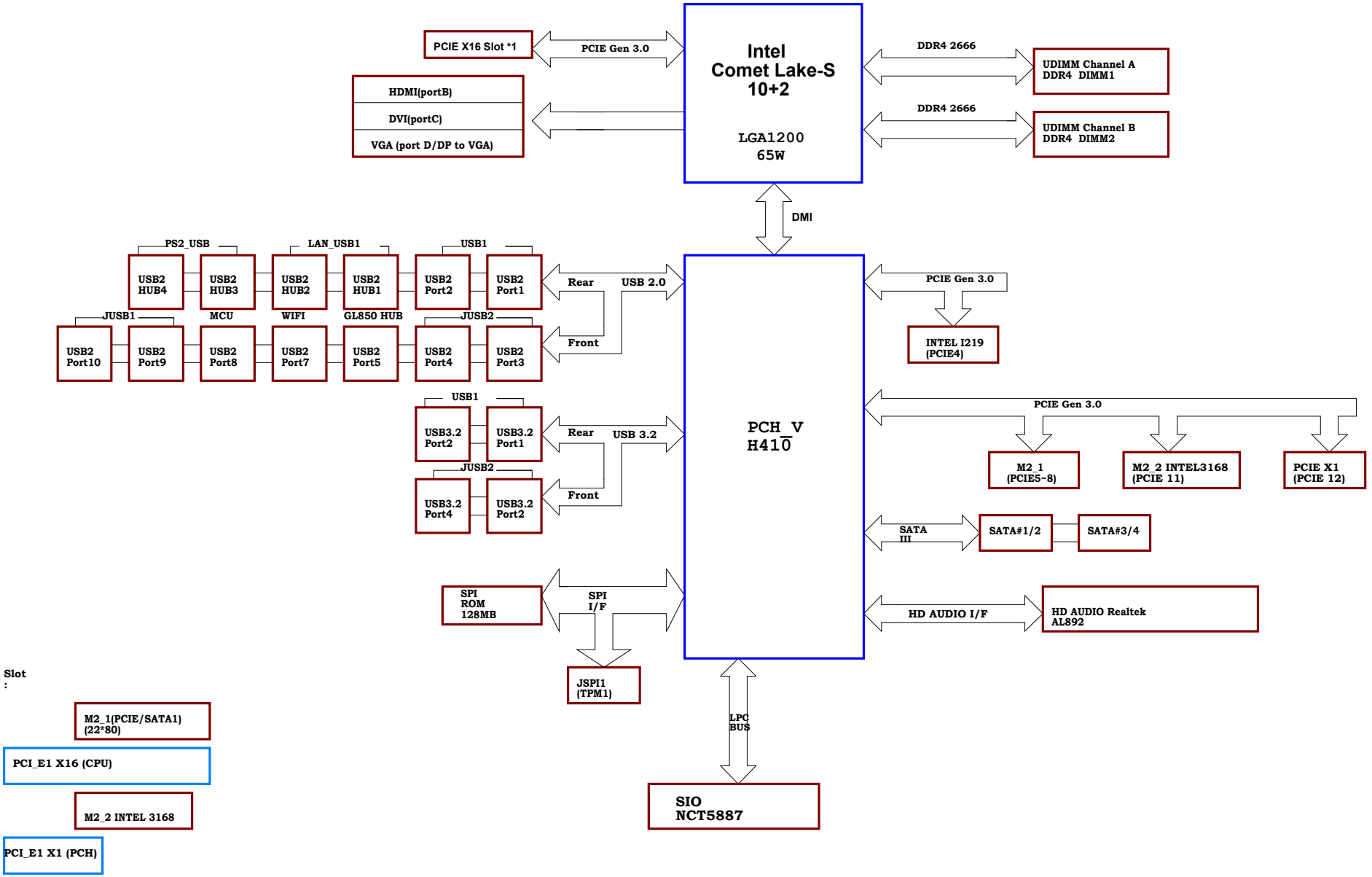
MS-7C86 Block Diagram



Slot
:

- M2_1(PCIE/SATA1) (22*80)
- PCI_E1 X16 (CPU)
- M2_2 INTEL 3168
- PCI_E1 X1 (PCH)

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Custom	Block Diagram	1.1

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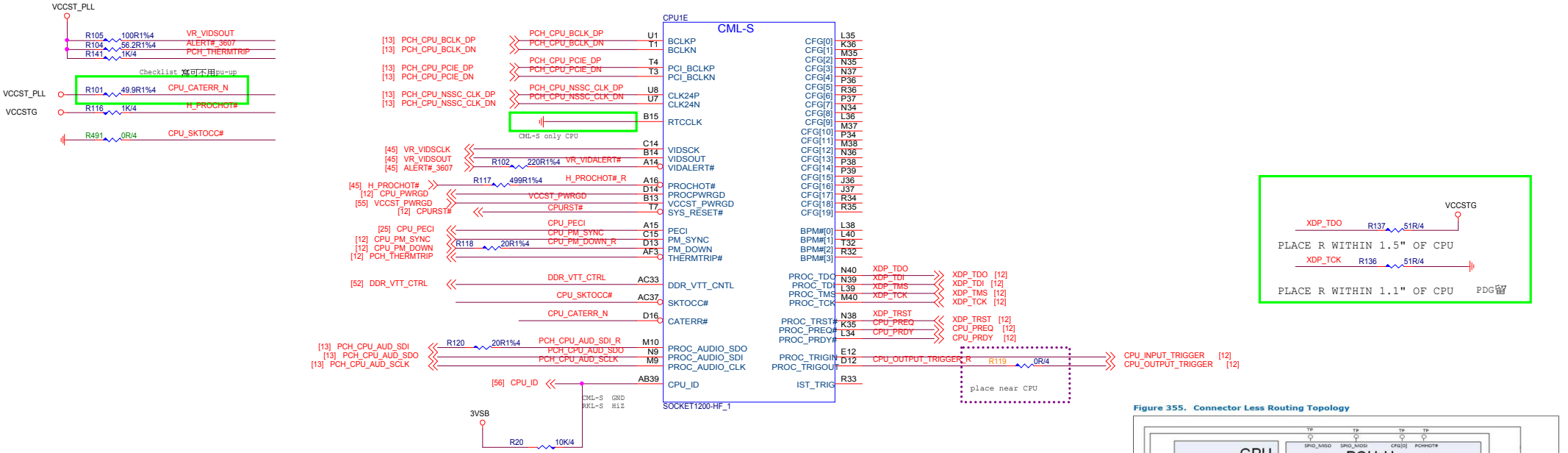
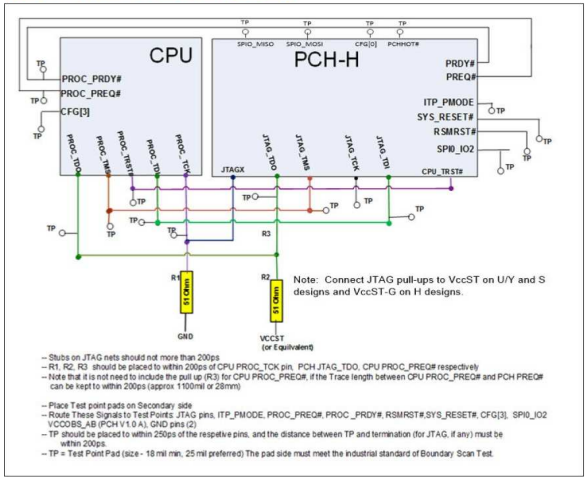


Figure 355. Connector Less Routing Topology



CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No stall	Stall	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5			PCIE Bifurcation
6			PCIE Bifurcation
7	Follow RESET#	Wait for BIOS	PEG TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

CFG5 CFG6

ENABLE#		SLOT	SLOT	SLOT
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	RSVD	RSVD	RSVD
1	1	X16	X0	X0

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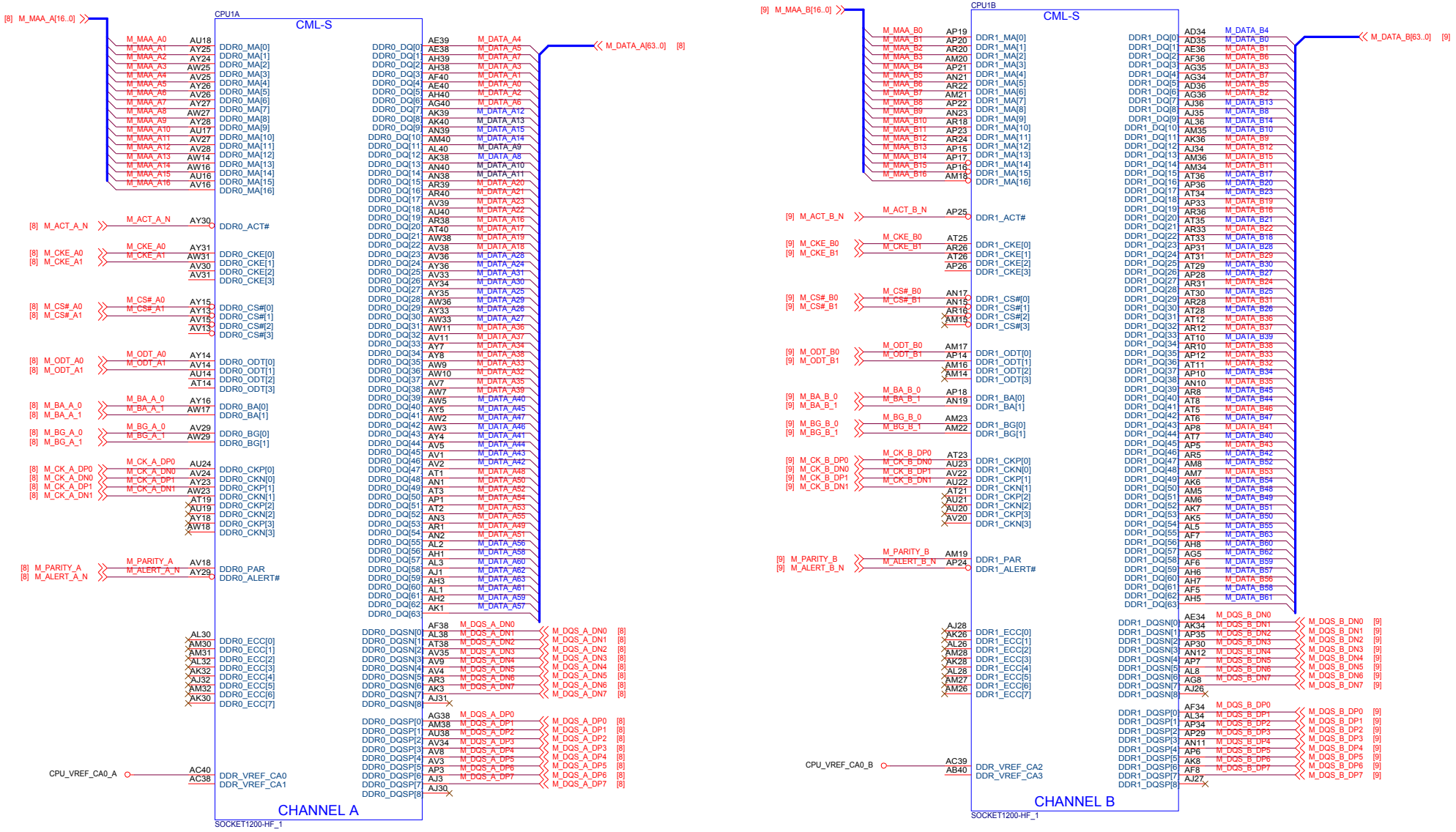

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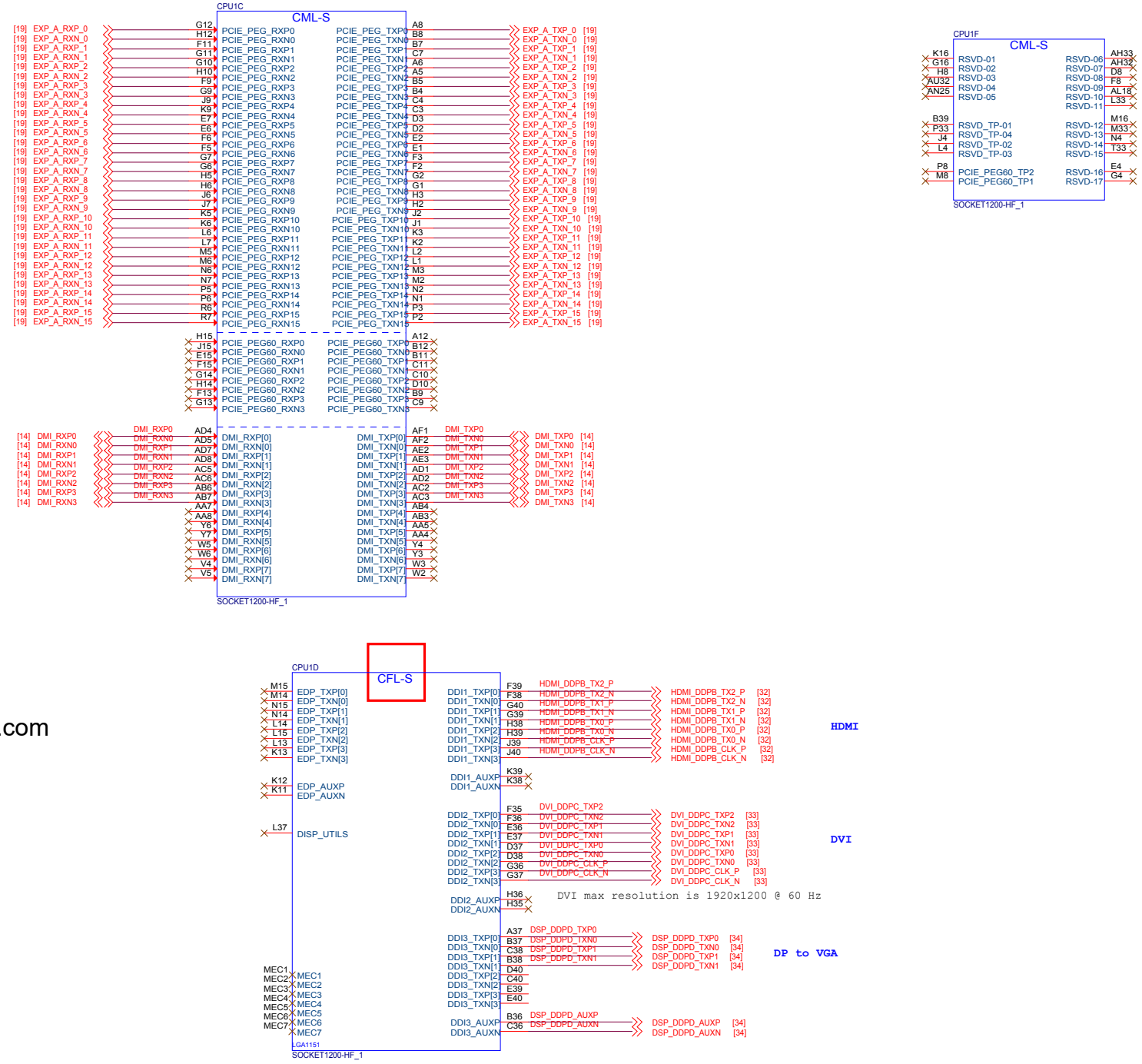

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Size: Custom	Document Description: CPU-PEG/Display/RSD	Rev: 1.1
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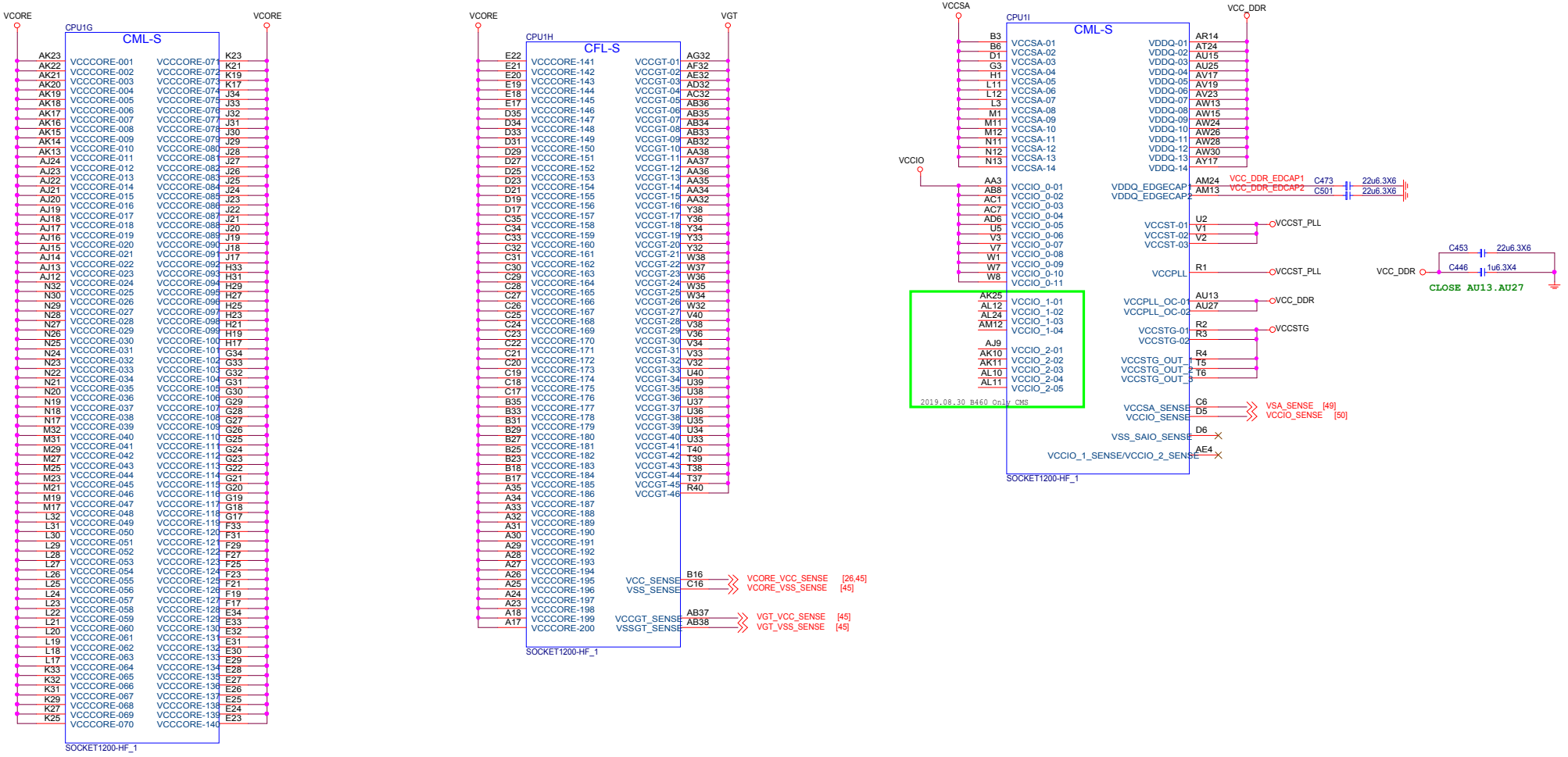
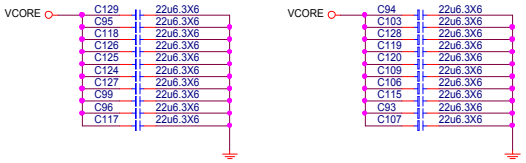
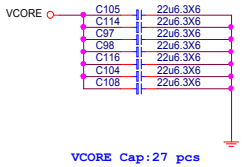
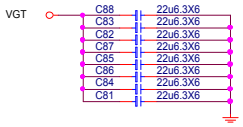


TOP Side Socket Cavity

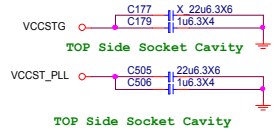


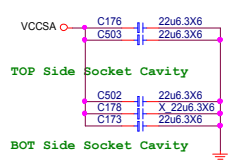


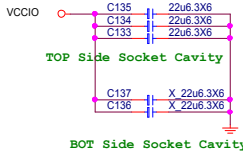
VCORE Cap:27 pcs



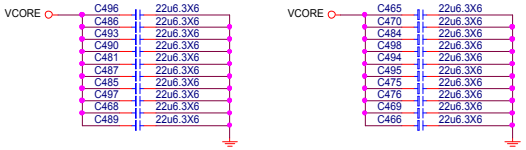
VGT Cap:8 pcs

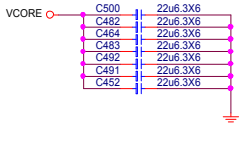


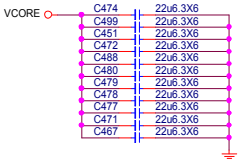




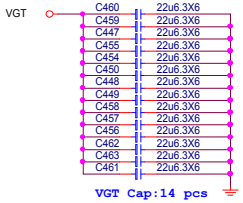
BOT Side Socket Cavity







VCORE Cap:38 pcs



VGT Cap:14 pcs

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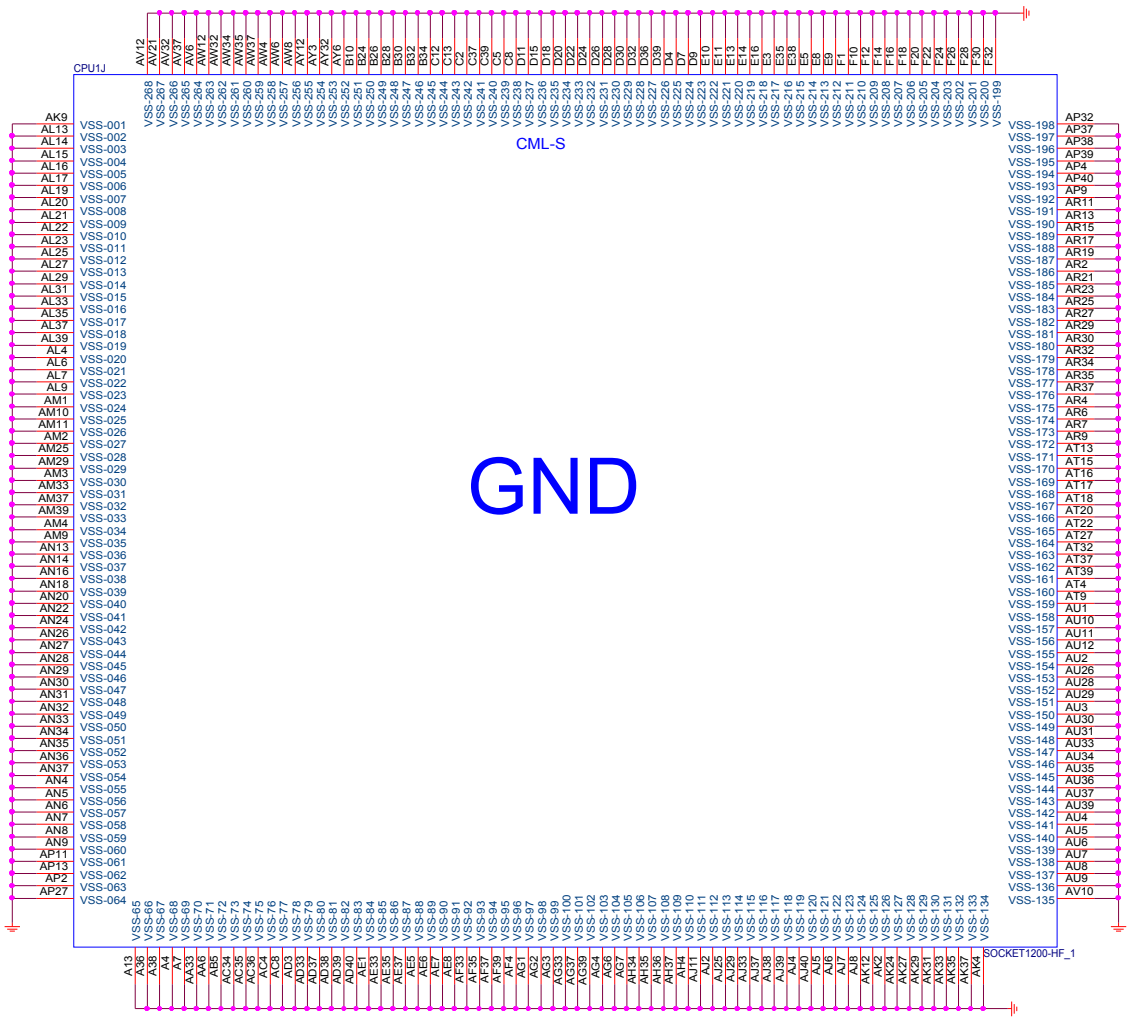

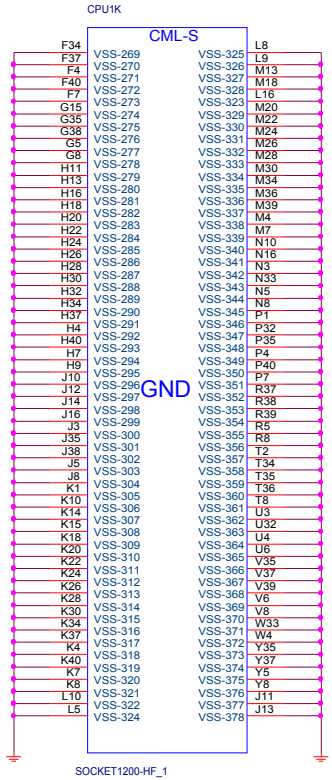

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Size: Custom	Document Description: CPU-GND	Rev: 1.1
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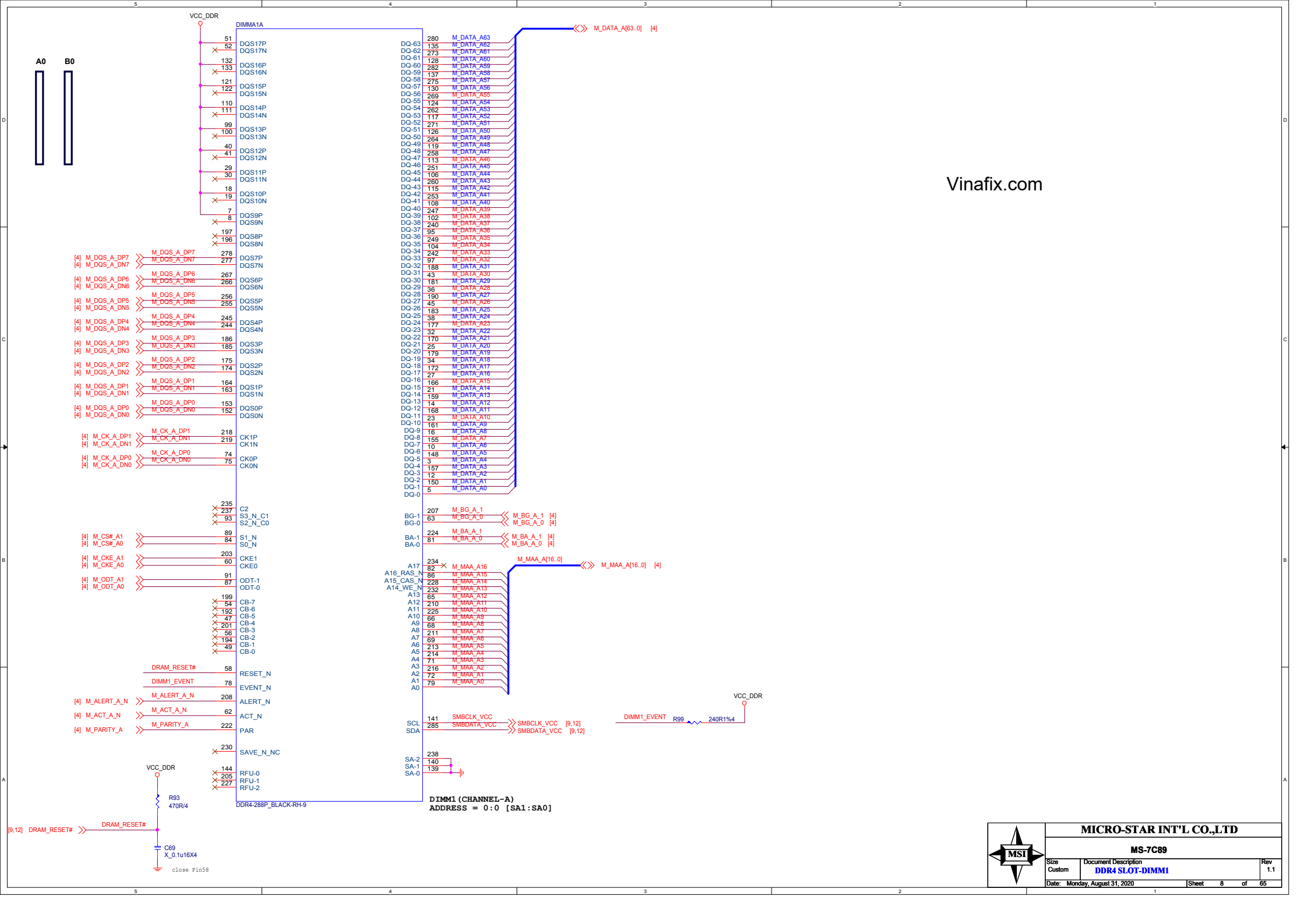
A0
B0
VCC_DDR
DIMMA1A
DDR4-288P_BLACK-RH-9
M_DATA_A[63..0]
M_MAA_A[16..0]
M_BG_A_1
M_BG_A_0
M_BA_A_1
M_BA_A_0
SMBCLK_VCC
SMBDATA_VCC
DIMM1_EVENT
R99
240R1%4
R93
470R/4
C69
X_0.1u16X4
close Pin58
DRAM_RESET#
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
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MS-7C89
Size
Custom
Document Description
DDR4 SLOT-DIMM1
Rev
1.1
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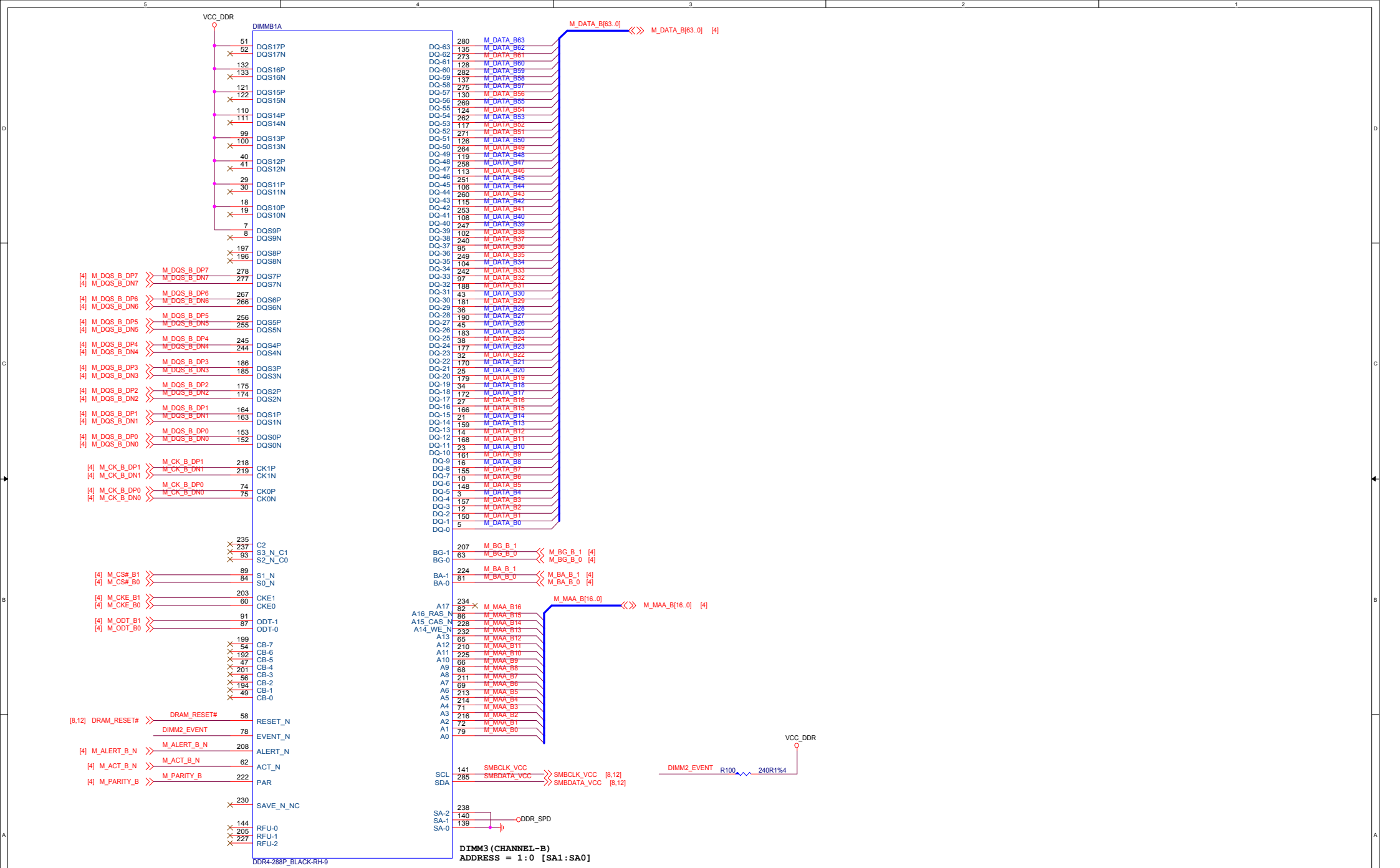

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Size: Custom	Document Description: DDR4 SLOT-DIMM2
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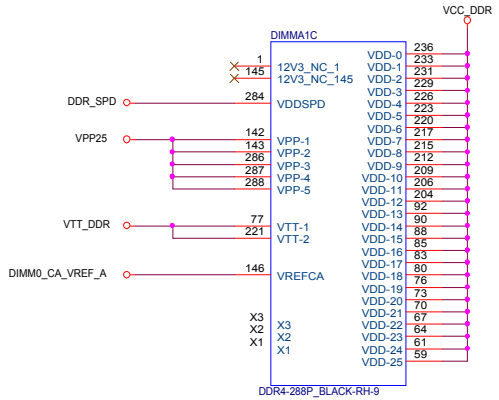

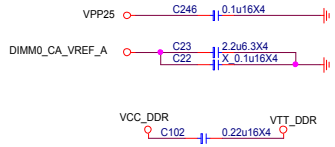

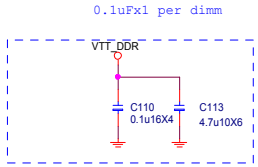

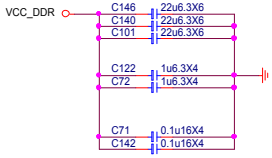

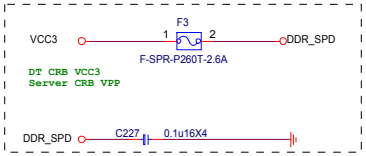

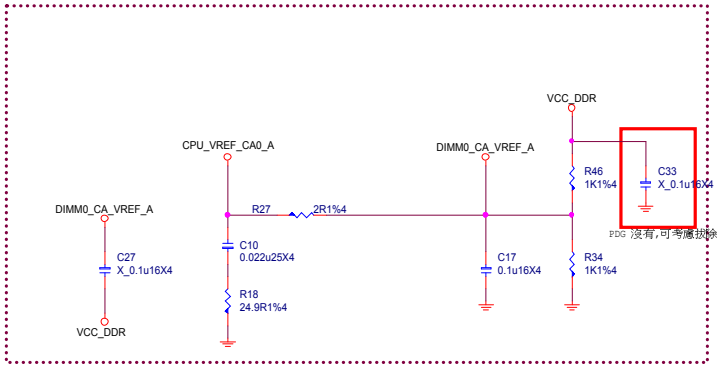

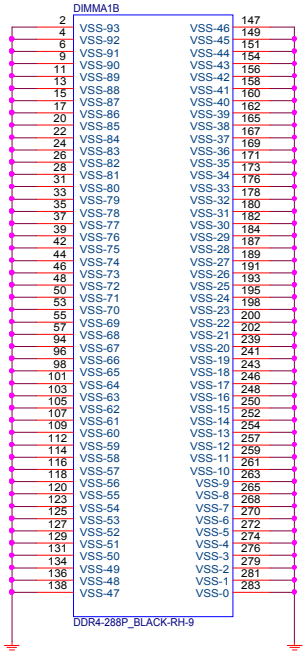

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MS-7C89		
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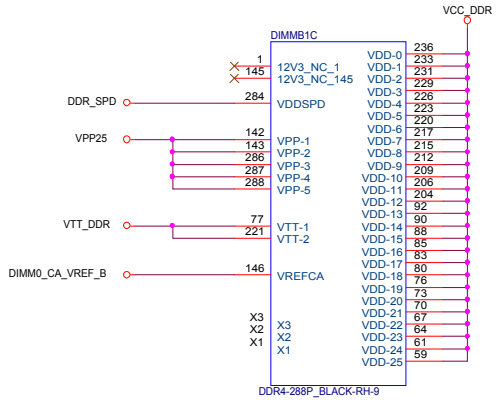
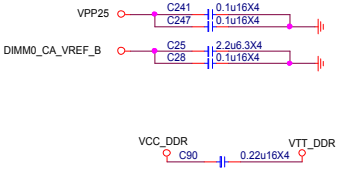
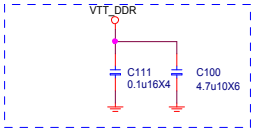
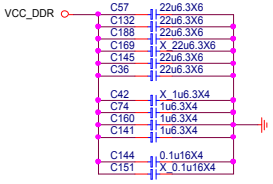
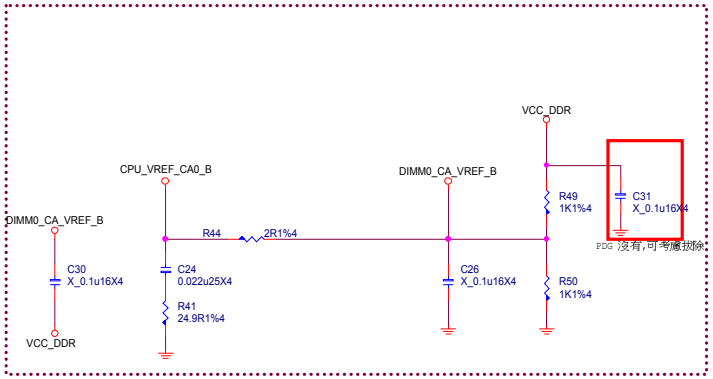


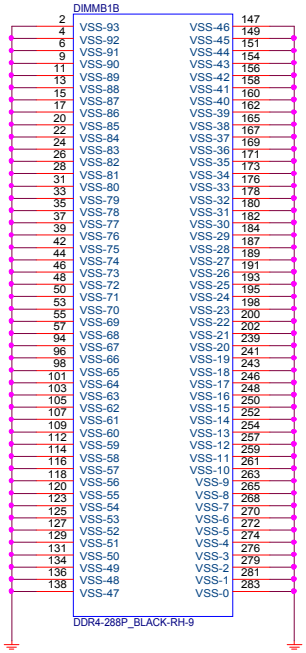


0.1uFx1 per dimm









MICRO-STAR INT'L CO.,LTD			
MS-7C89			
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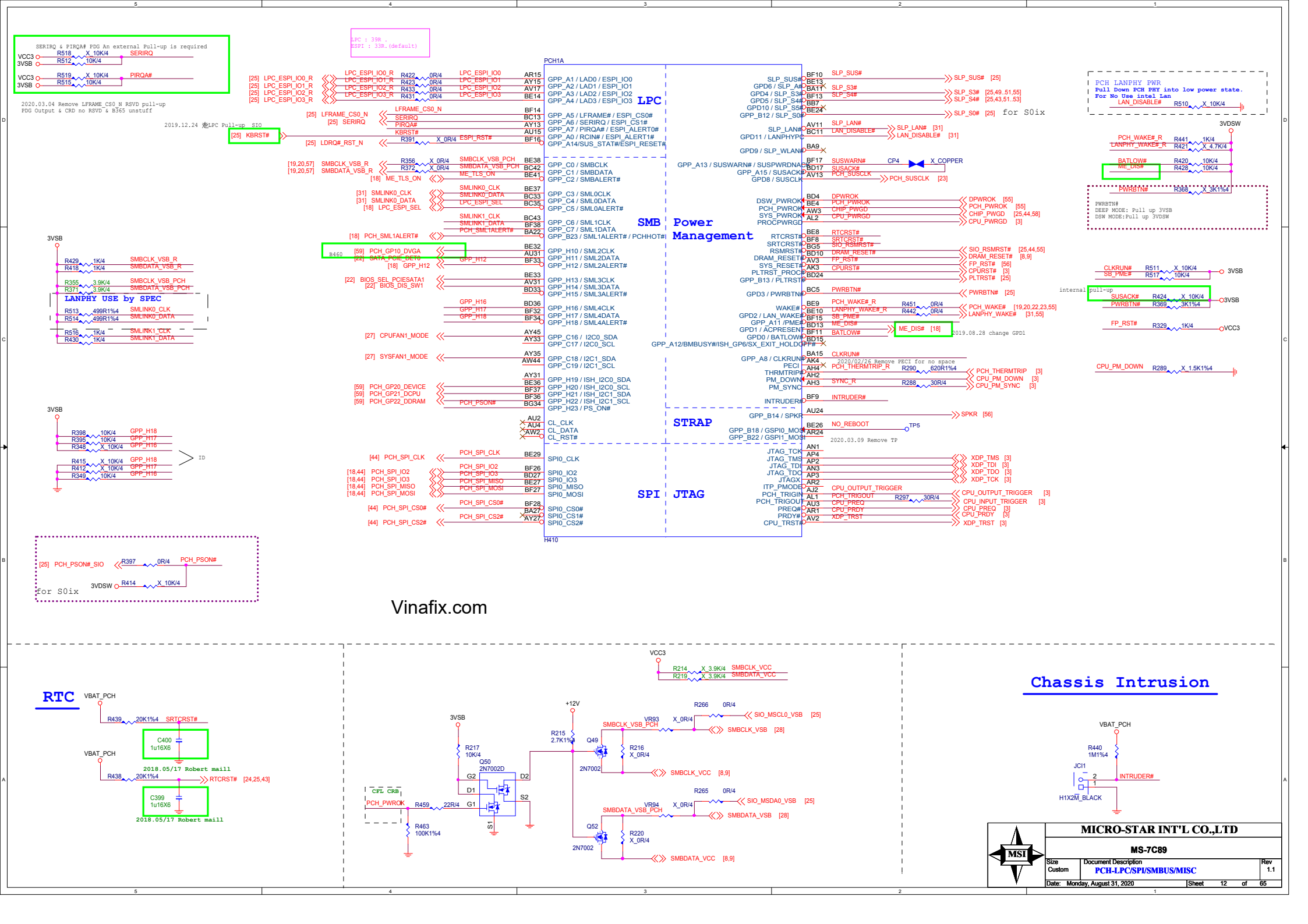
SERIRQ & PIRQA# PDG An external Pull-up is required
2020.03.04 Remove LFRAME_CS0_N RSVD pull-up
PDG Output & CRD no RSVD & B365 unstuff
2019.12.24 change LPC Pull-up SIO
LPC : 33R .
ESPI : 33R.(default)
PCH1A
LPC
SMB
Power Management
STRAP
SPI
JTAG
H410
LANPHY USE by SPEC
for S0ix
2019.08.28 change GPD1
2020.02/26 Remove PECI for no space
2020.03.09 Remove TP
PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
internal pull-up
PWRBTN#
DEEP MODE: Pull up 3VSB
DSW MODE:Pull up 3VDSW
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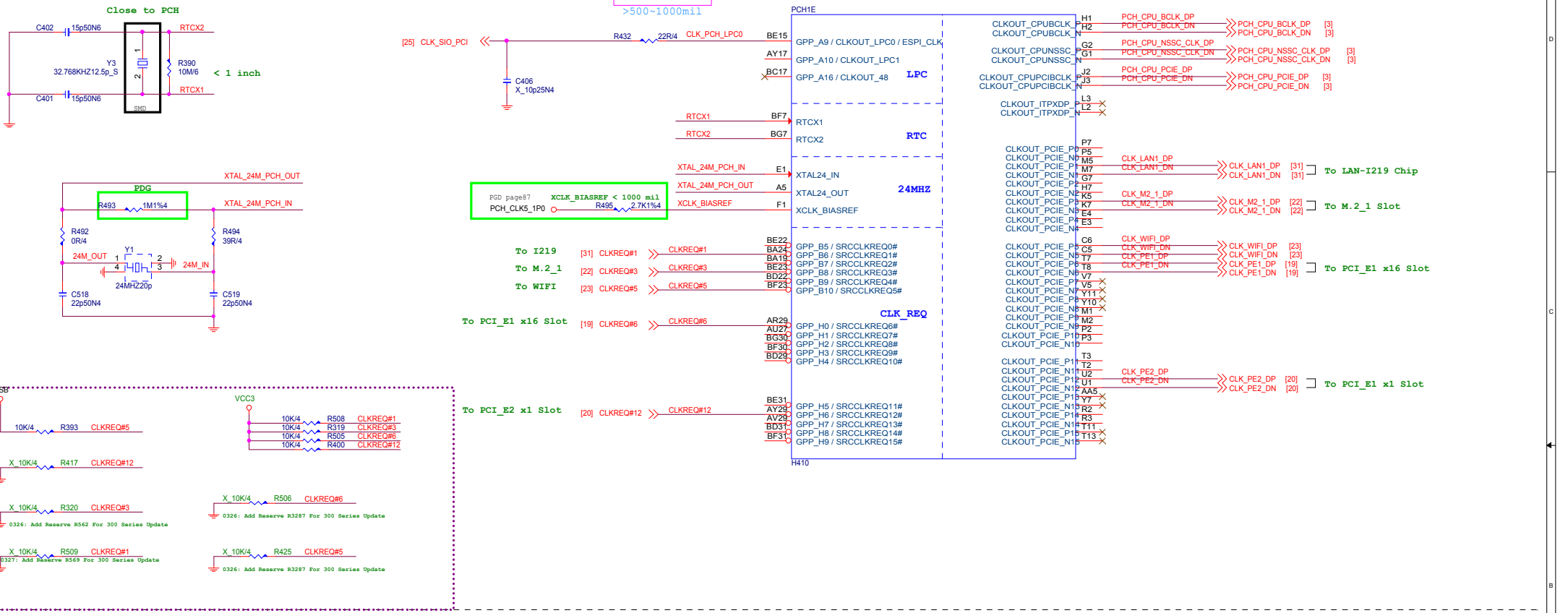
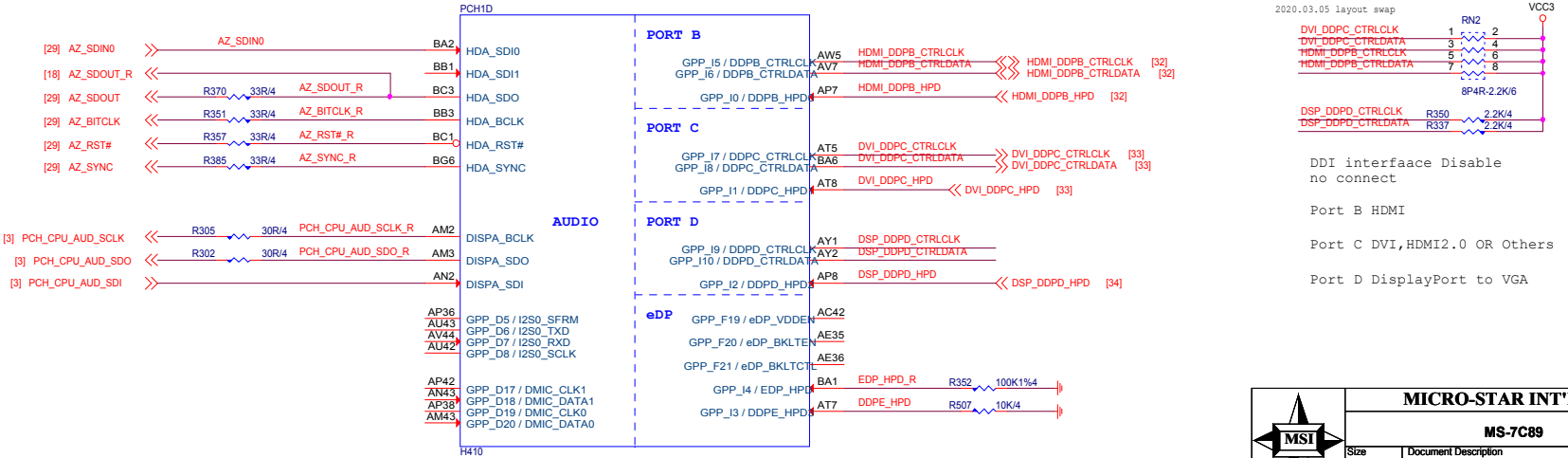
RTC
2018.05/17 Robert maill
CFL CRB
Chassis Intrusion
MICRO-STAR INT'L CO.,LTD
MS-7C89
PCH-LPC/SPI/SMBUS/MISC
Monday, August 31, 2020

PCH_CLK



PCH_AUDIO



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Custom	PCH-Clock/Audio	1.1

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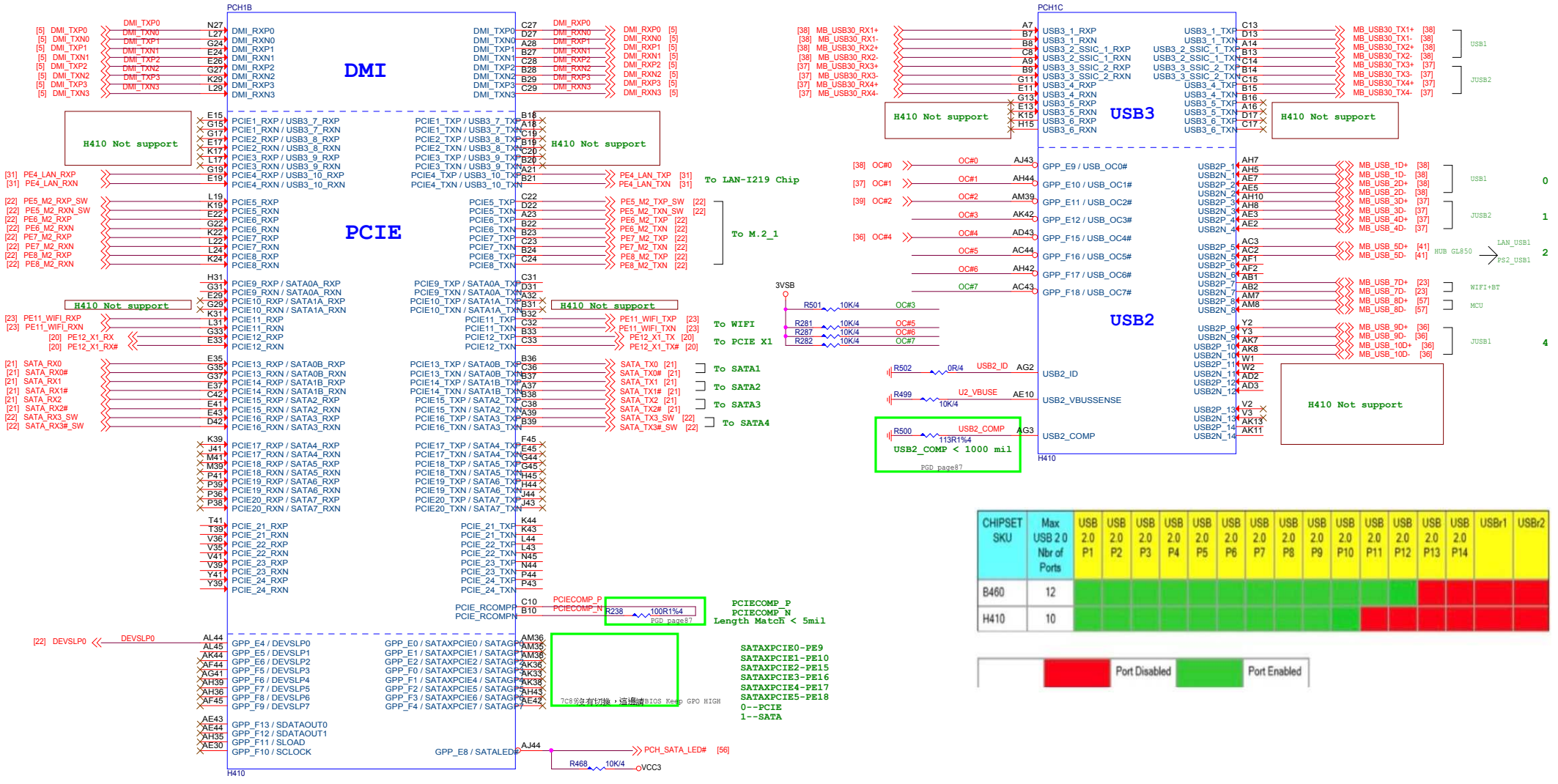

CHIPSET SKU	Max USB 2.0 Nbr of Ports	USB 2.0 P1	USB 2.0 P2	USB 2.0 P3	USB 2.0 P4	USB 2.0 P5	USB 2.0 P6	USB 2.0 P7	USB 2.0 P8	USB 2.0 P9	USB 2.0 P10	USB 2.0 P11	USB 2.0 P12	USB 2.0 P13	USB 2.0 P14	USBr1	USBr2
B460	12																
H410	10																

Port Disabled Port Enabled

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Size: Custom	Document Description: PCH-DMI/PCIE/USB/SATA
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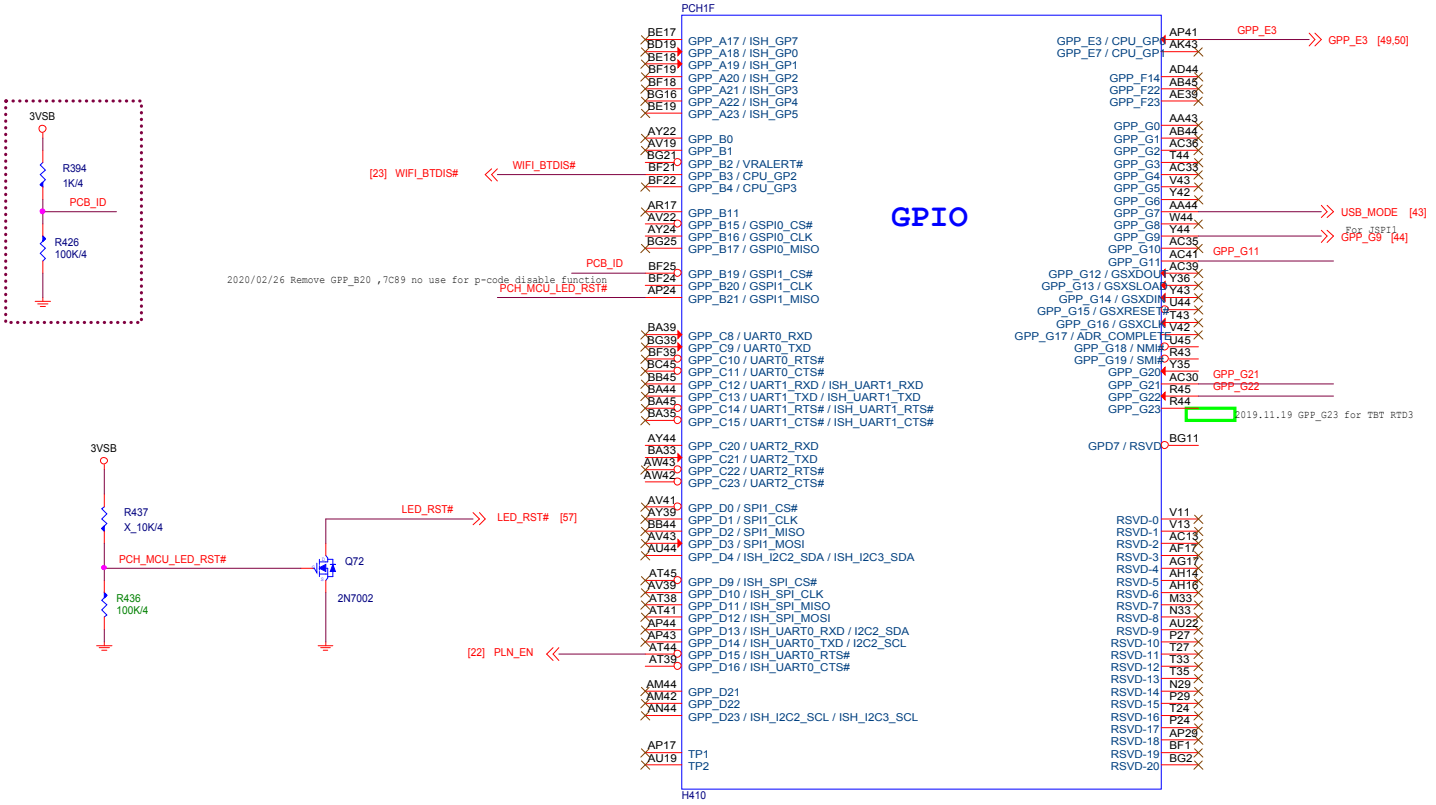
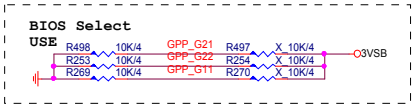
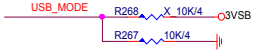
	GPP_G21	GPP_G22	GPP_G11
H410M PRO	0	0	0
H410M-A PRO	0	0	1
H410M BOMBER	0	1	1
H410M PRO-VH	0	1	0







MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: PCH-GPIO/RSVD | Rev: 1.1

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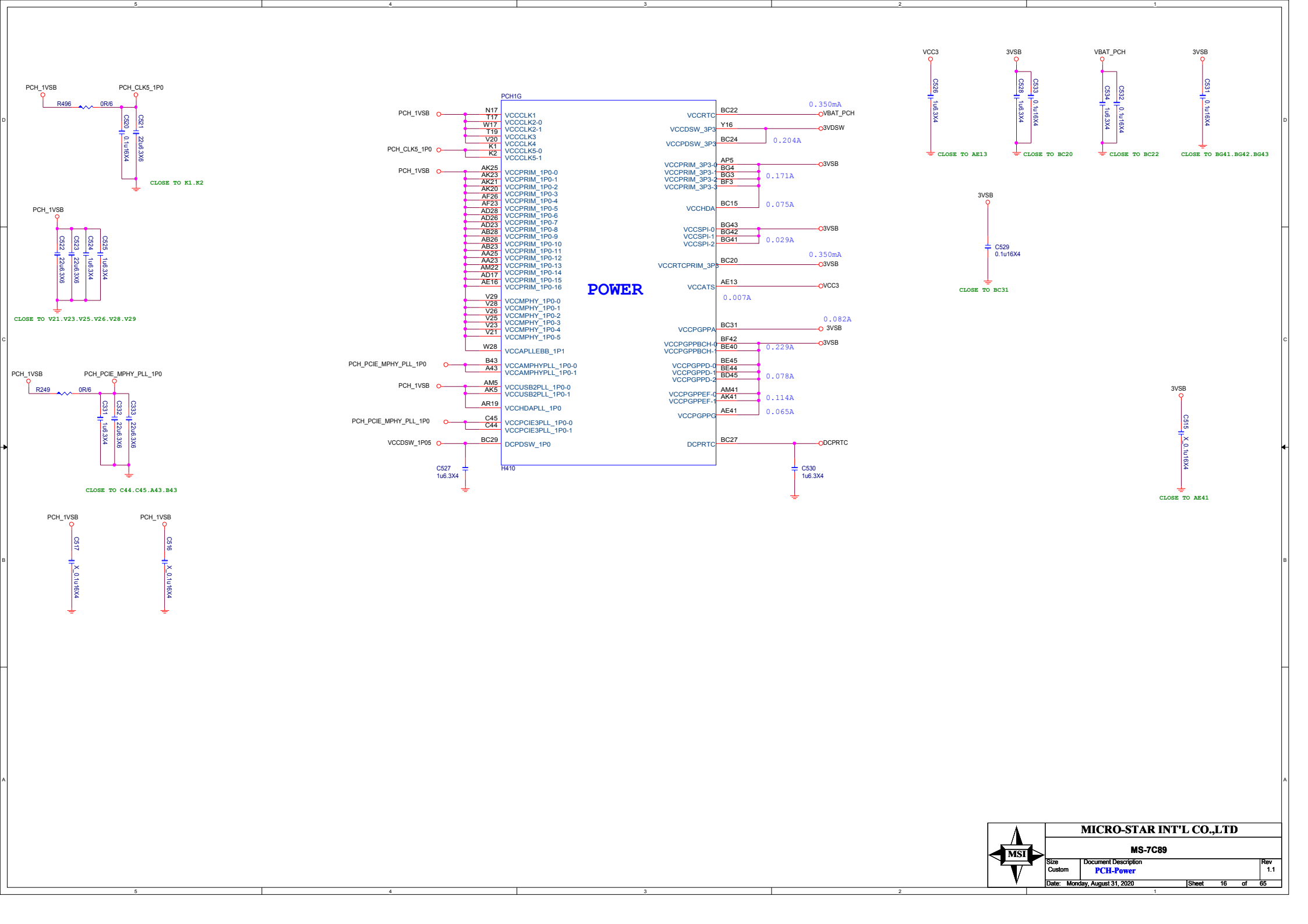

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Size: Custom	Document Description: PCH-Power
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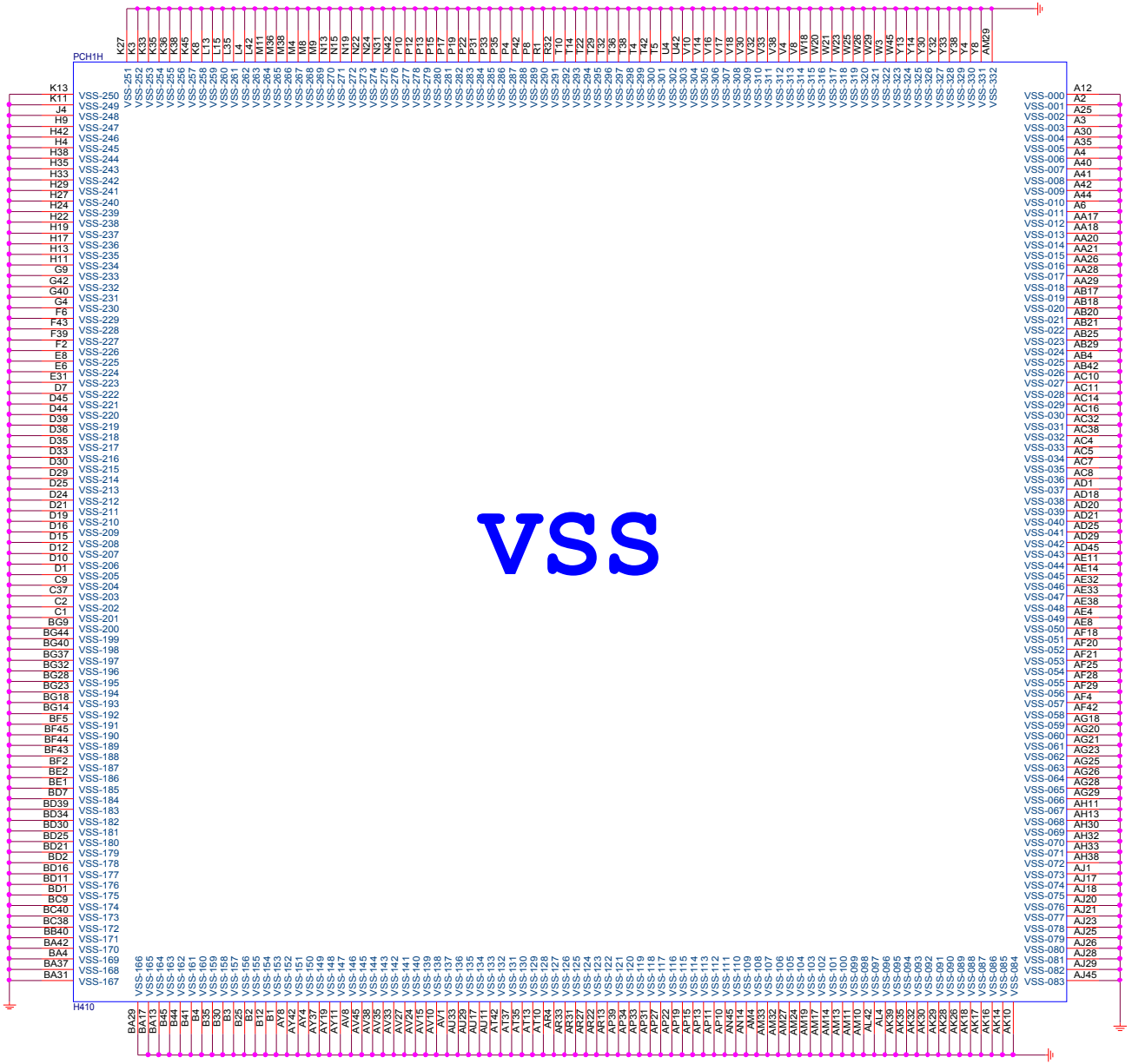

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TOP Swap

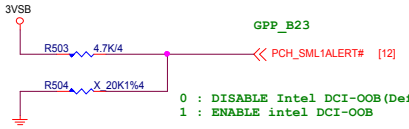
GPP_B14

2020/02/26 Follow 7C82 remove

0 : DISABLE (Default)
1 : ENABLE

Internal Pull-down is disabled after PCH_PWROK is high.

DCI Enable

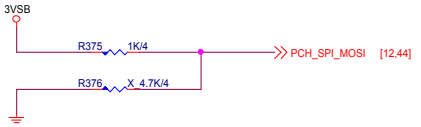


0 : DISABLE Intel DCI-OOB(Default)
1 : ENABLE intel DCI-OOB

Internal Pull-down is disabled after RSMRST# de-assert.

Reserved

CRB



Internal Pull-up

No Reboot

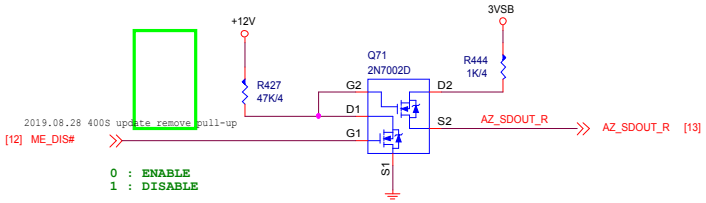
GPP_B18

2020/02/26 Follow 7C82 remove

0 : DISABLE (Default)
1 : ENABLE

Internal Pull-down is disabled after PCH_PWROK is high.

Flash Descriptor Security Override



0 : ENABLE
1 : DISABLE

0 : Enable security measures defined in the Flash Descriptor. (Default)
1 : DISABLE:Flash Descritior Decurity(Override).

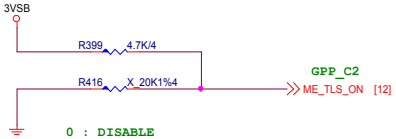
Internal Pull-down is disabled after PCH_PWROK is high.

Reserved

CRB

Internal Pull-up

TLS confidentiality

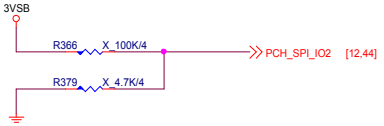


0 : DISABLE
1 : ENABLE (Default)

Internal Pull-down is disabled after RSMRST# de-assert.

Reserved

CRB



Internal Pull-up

Boot BIOS

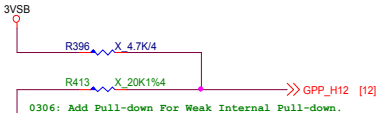
GPP_B22

2020/02/26 Follow 7C82 remove

0 : SPI (Default)
1 : LPC

Internal Pull-down is disabled after PCH_PWROK is high.

ESPI FLASH SHARING MODE



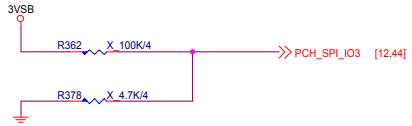
0306: Add Pull-down For Weak Internal Pull-down.

0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal Pull-down is disabled after RSMRST# de-assert.

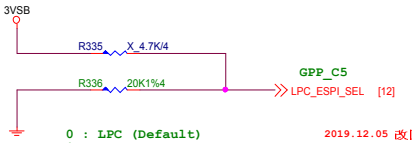
Reserved

CRB



Internal Pull-up

LPC eSPI Mode



0 : LPC (Default)
1 : eSPI

2019.12.05 改回LPC Mode internal pull-down

Internal Pull-down is disabled after RSMRST# de-assert.

MICRO-STAR INT'L CO.,LTD

MS-7C89

Size	Document Description	Rev
Custom	PCH-Strap	1.1

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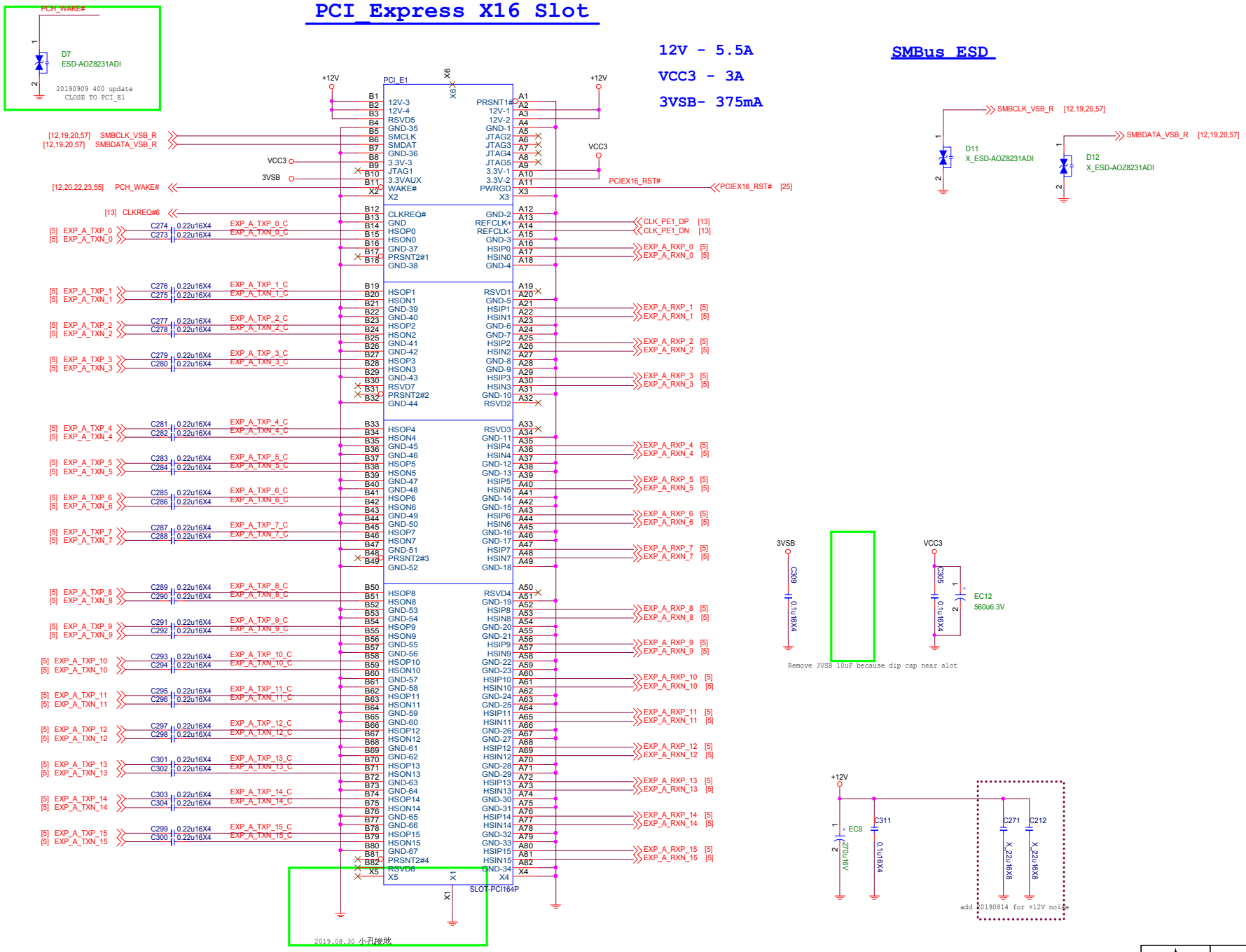
PCI Express X16 Slot

12V - 5.5A

VCC3 - 3A

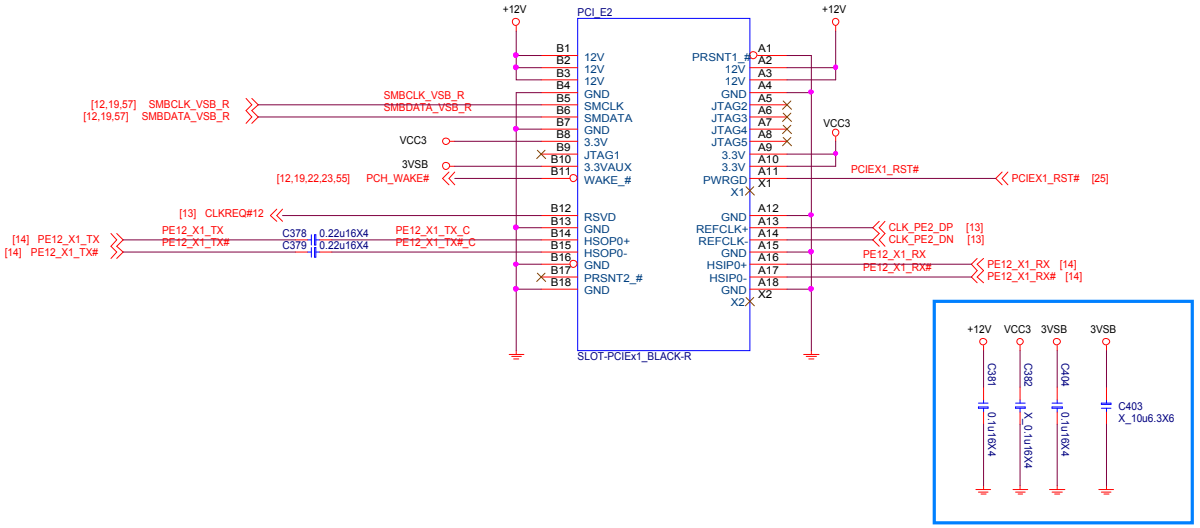
3VSB- 375mA

SMBus ESD



MICRO-STAR INT'L CO.,LTD	
MS-7C89	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 1.1	
Date: Monday, August 31, 2020	Sheet 19 of 65

PCIE X1



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C89	
Size: Custom	Document Description: M.2-SLOT2	Rev: 1.1
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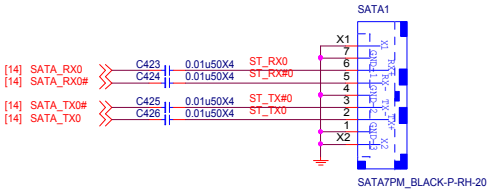
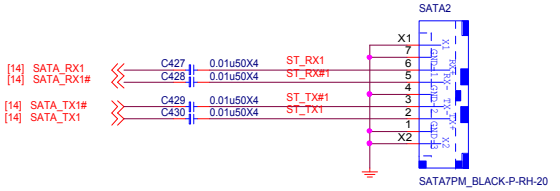
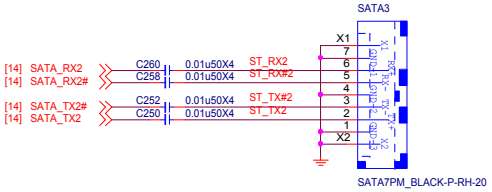
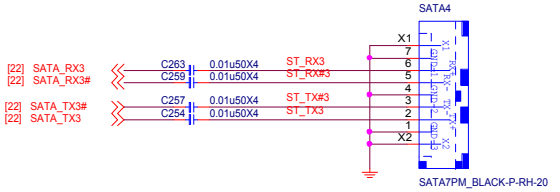
SATA Connector









MICRO-STAR INT'L CO.,LTD

MS-7C89

Size	Document Description	Rev
Custom	SATA Connector	1.1

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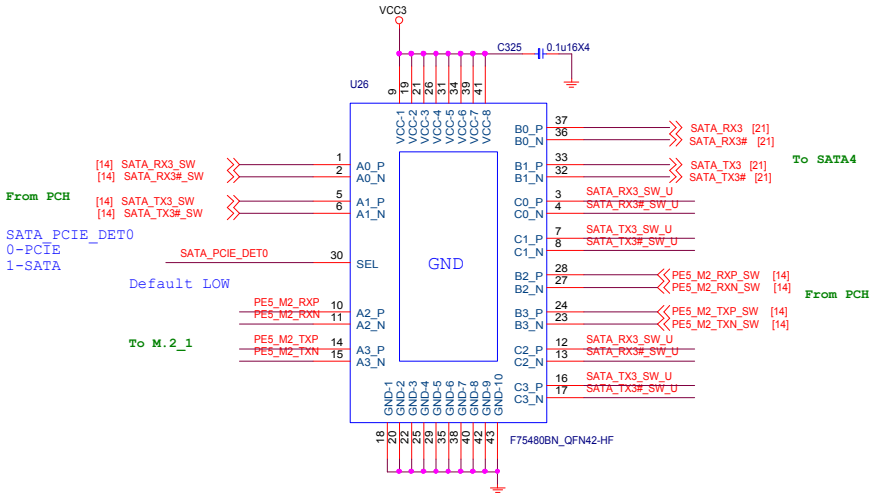
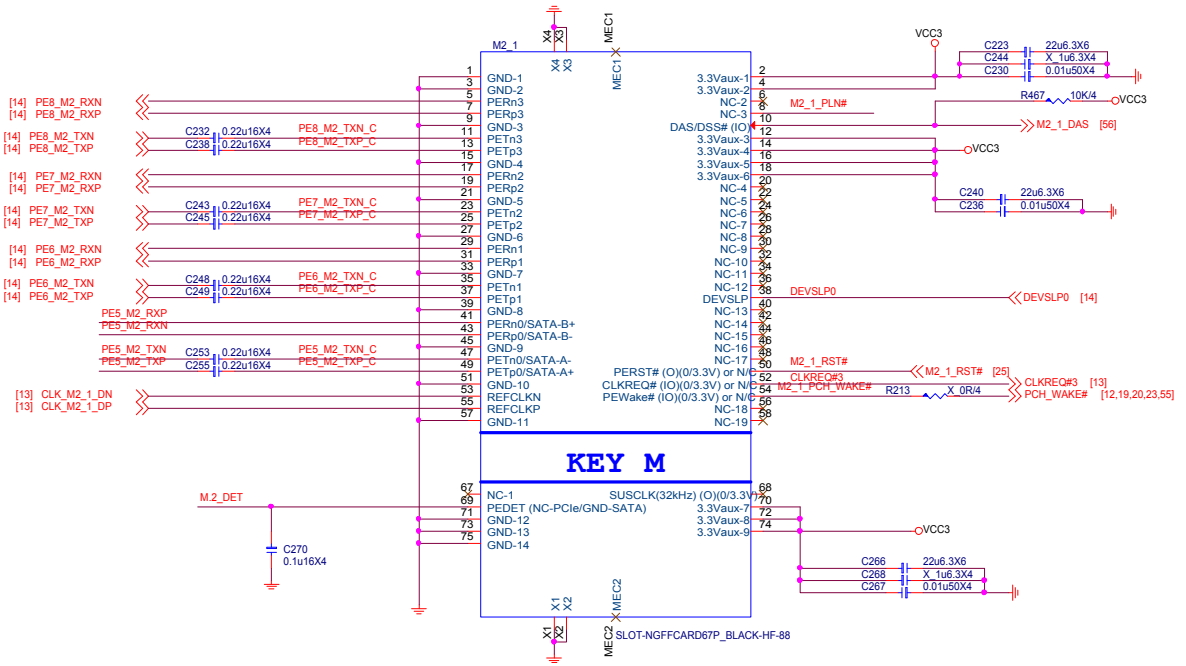
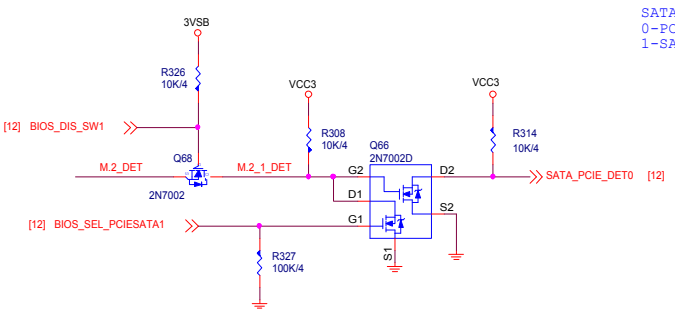
M2_1



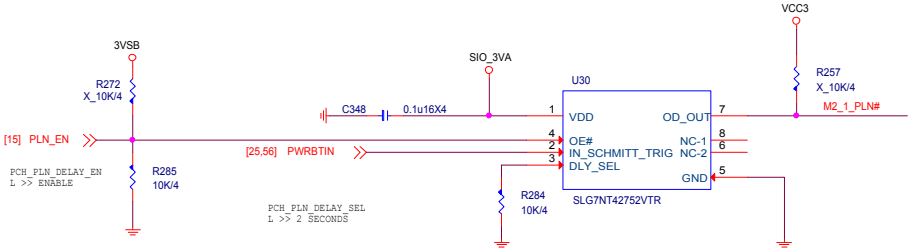




SATA_PCIE_DET0
0-PCIE
1-SATA

BIOS_MODE

GPP_H14	GPP_H13		GPP_H11
BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode	SATA_PCIE_DET0
0	1	M2-SATA	1
0	0	M2-PCIE	0
GPI(1)	GPI(0)	AUTO	



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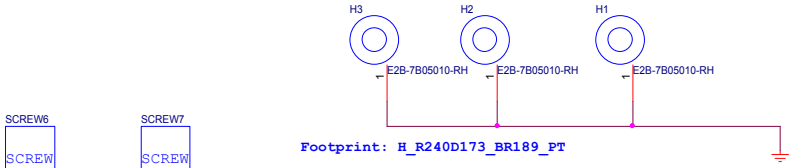

SCREW6 SCREW — E2B-7984020-A89

SCREW7 SCREW — E43-1203514-A89

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MS-7C89		
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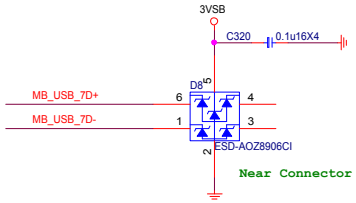
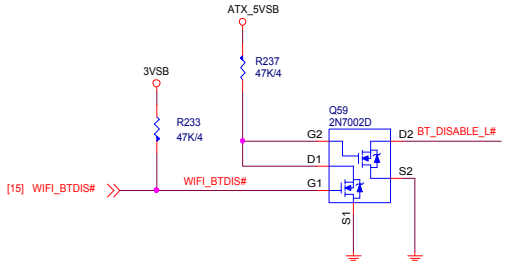
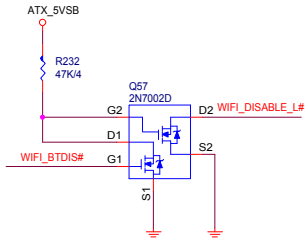
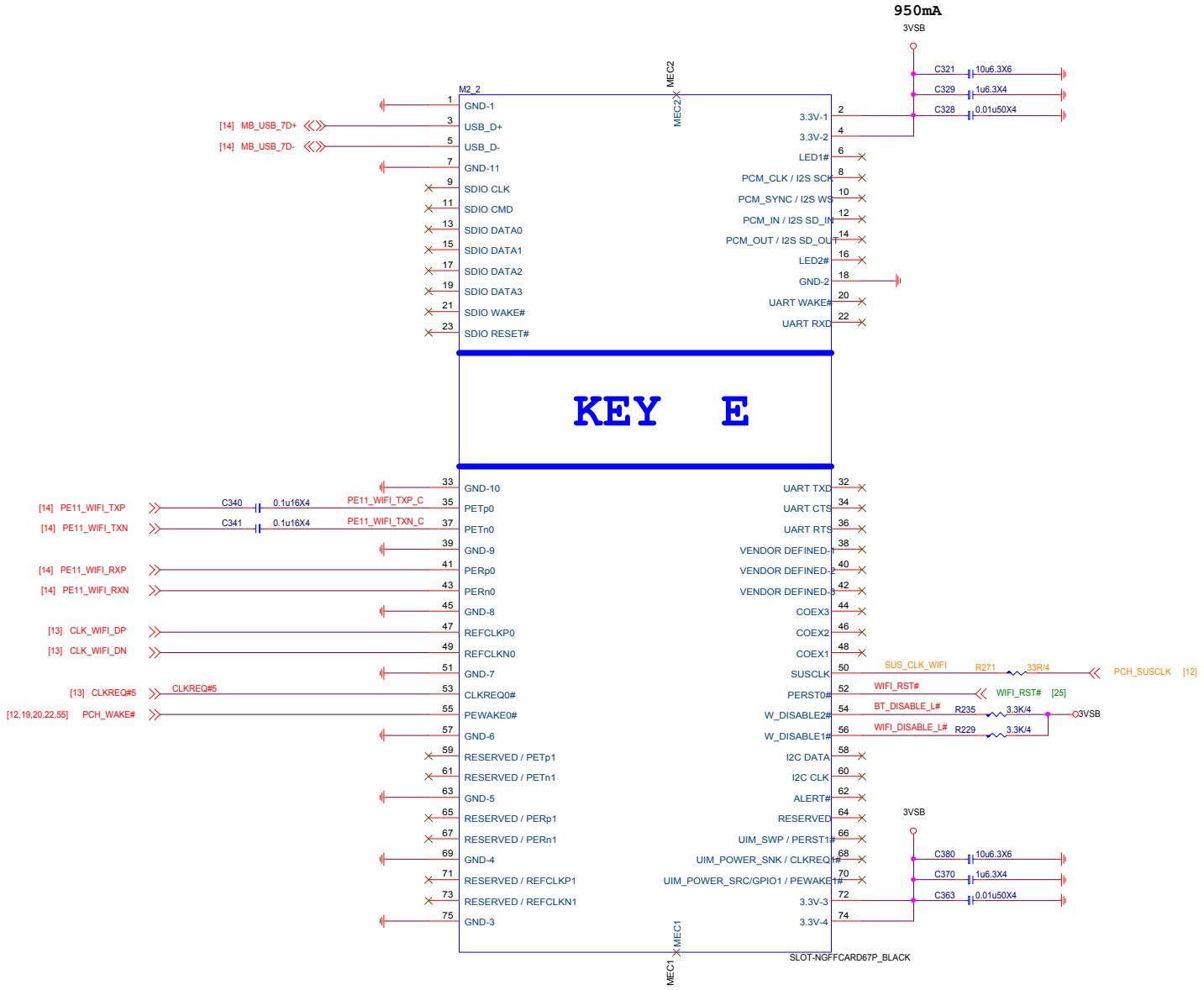
M2_2

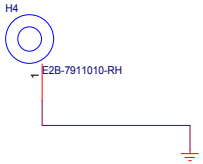






950mA





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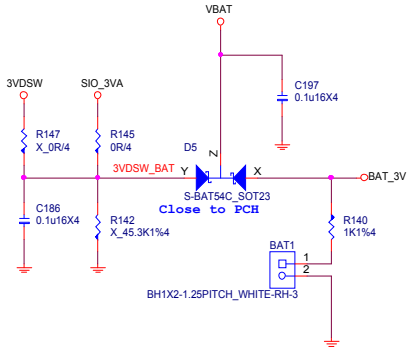
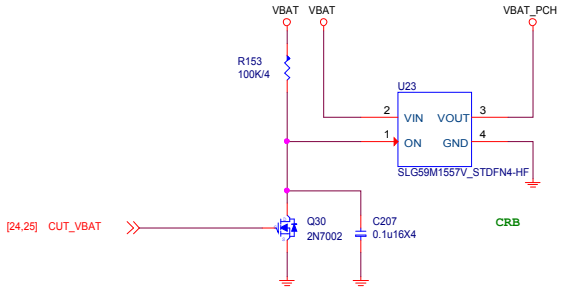
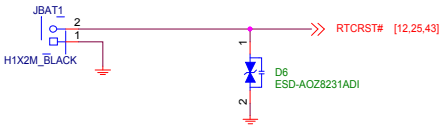
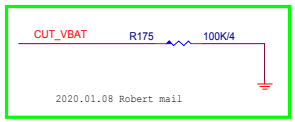
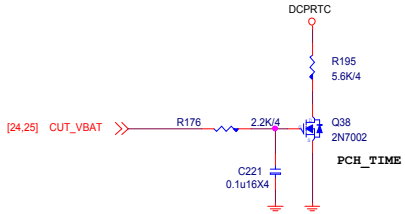
VBAT











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MS-7C89		
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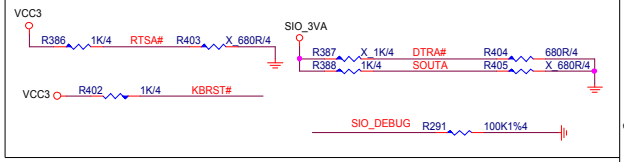
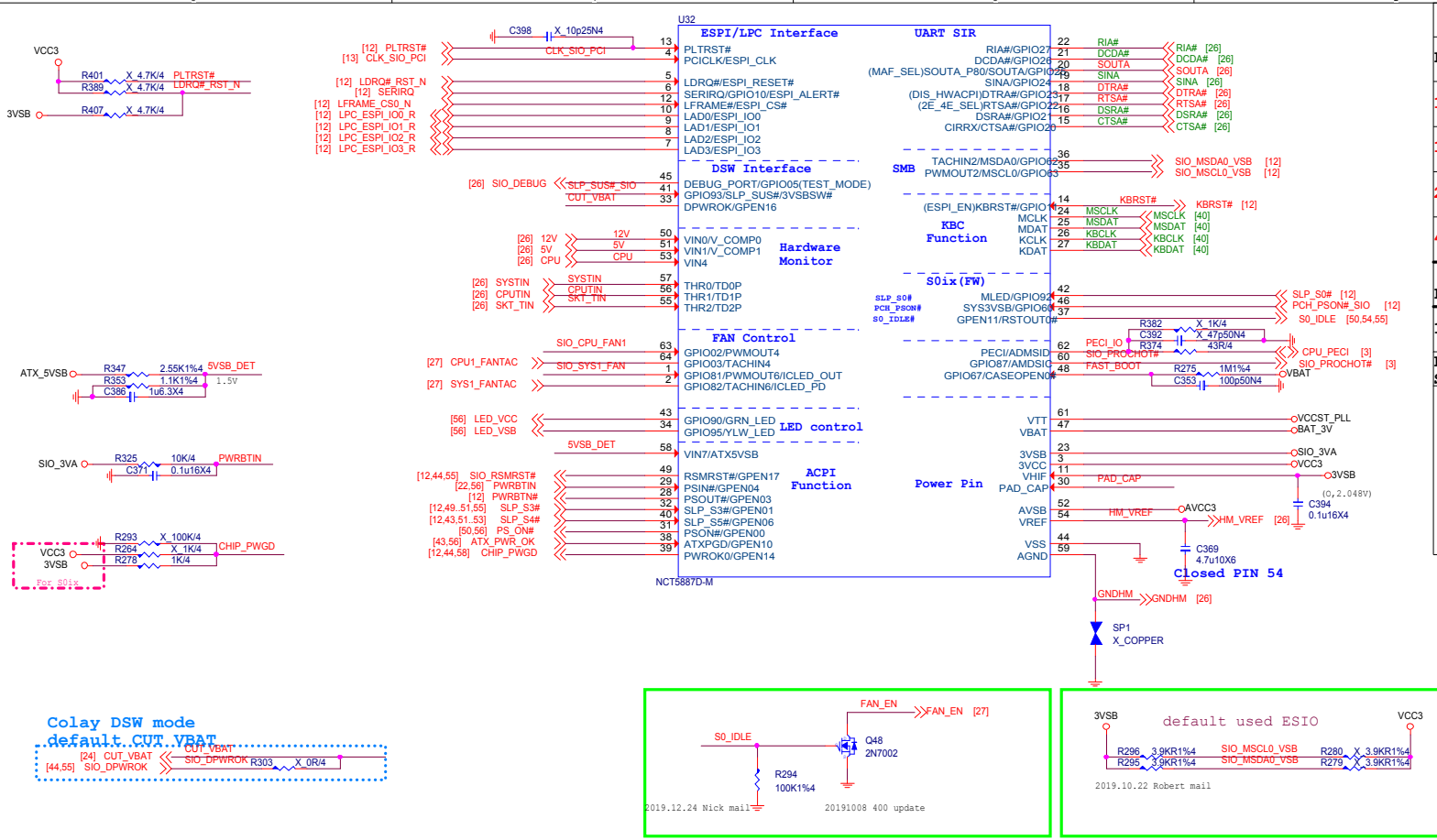
POWER ON STRAPPING PIN FOR NCT5887

PIN	NAME	Circuit NAME	0	1	Strap Point
17	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	VCC3
18	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
20	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
45	Test mode	SIO_DEBUG	Pull down 100K	-	NA

PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
14	ESPI_EN	KBRST#	LPC(VCC3)	ESPI(3VA)	VCC3 3VA

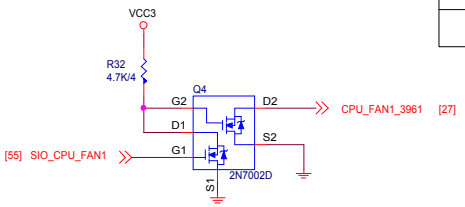
FW SEL: DSW_EN default disable

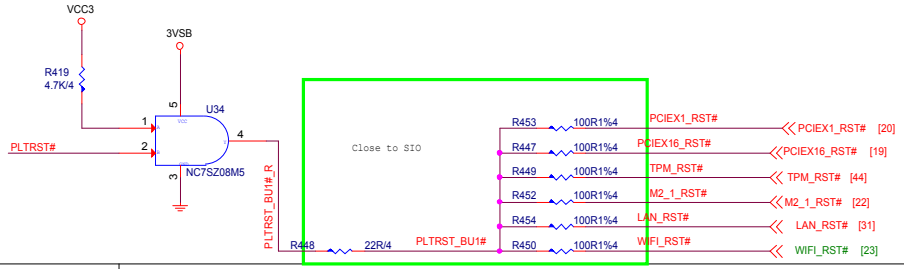




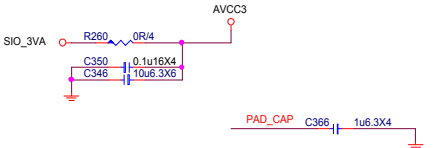
SIO_WAKE

S5	S3	S0
SIO_WAKE#		FAN



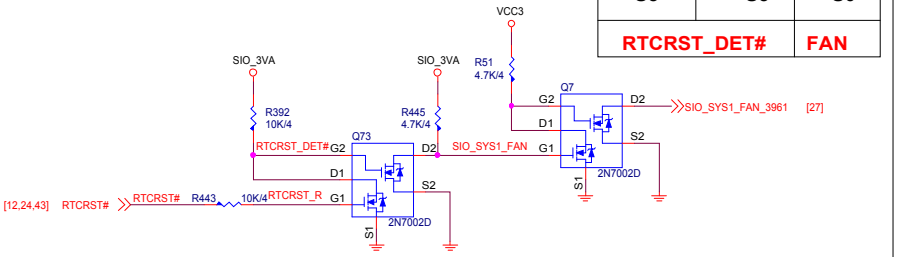


3V Analog Power



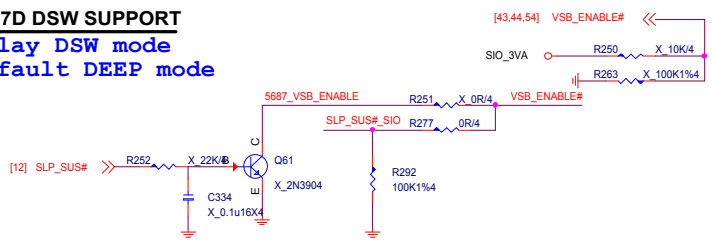
RTCRST DET

S5	S3	S0
RTCRST_DET#		FAN

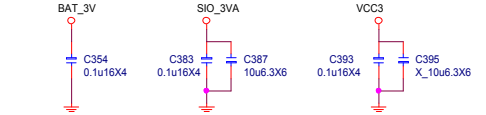


5887D DSW SUPPORT

Colay DSW mode
default DEEP mode



Closed PIN99 Closed PIN46,85 Closed PIN1



MICRO-STAR INT'L CO.,LTD

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Custom	SIO-NCT5687-1	1.1

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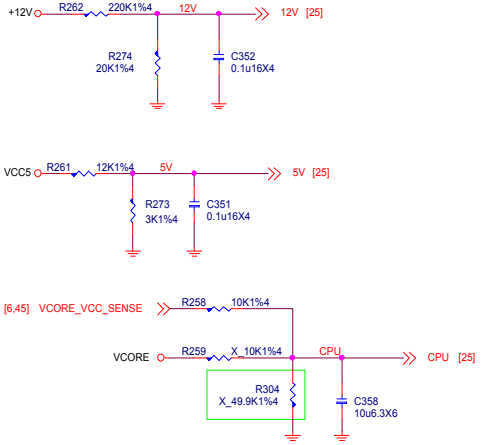
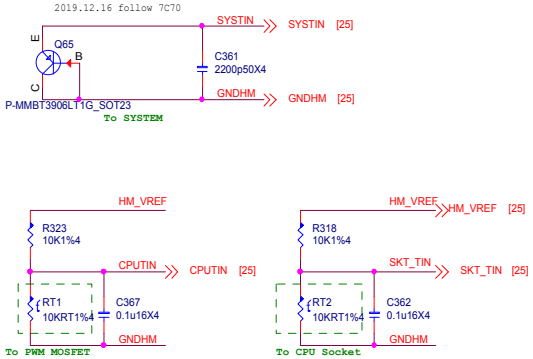
HW Monitor - Voltage

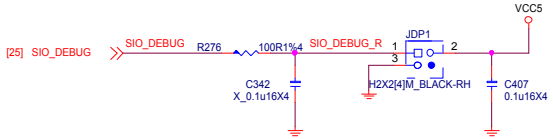
SIO HM Voltage Over 2V will Not Detect



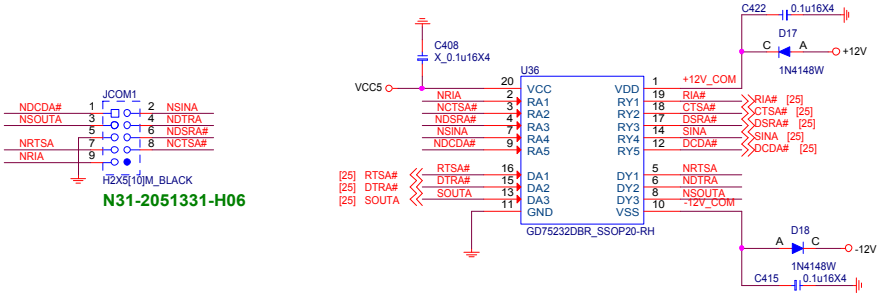
Thermal



DEBUG PORT



COM Port



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MS-7C89		
Size: Custom	Document Description: SIO-NCT5687-2	Rev: 1.1
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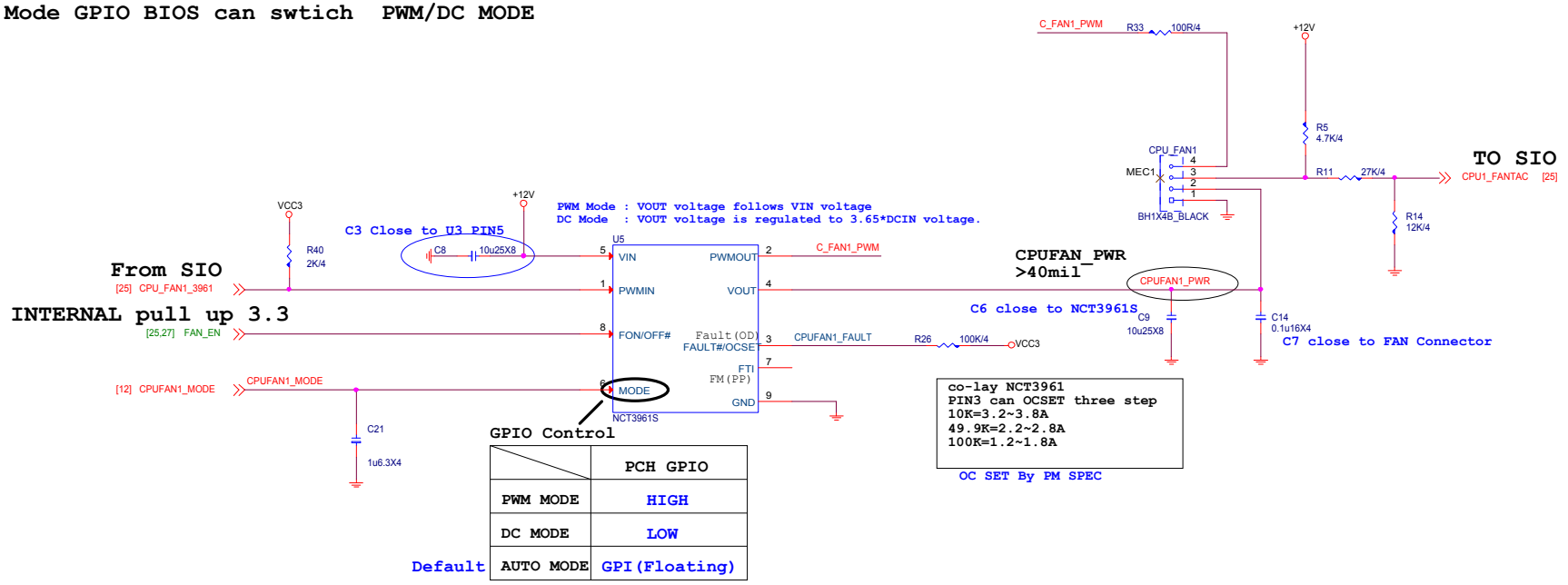
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

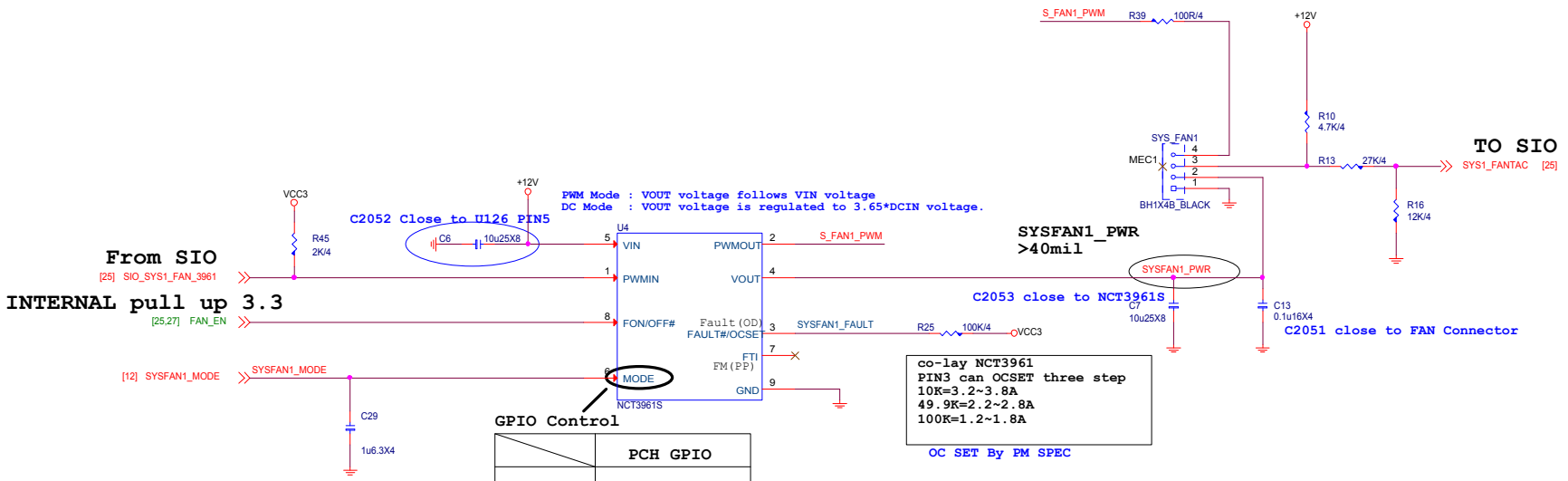
1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C89

Size	Document Description	Rev
Custom	CPU and PUMP FAN	1.1

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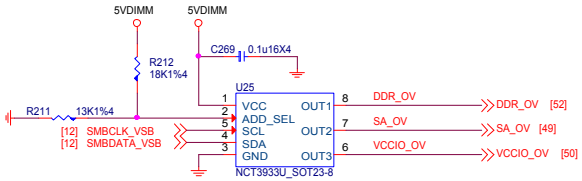
VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



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MICRO-STAR INT'L CO.,LTD

MS-7C89

Size	Document Description	Rev
Custom	NCT3933	1.1

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ALC892

follow PCH power well

3VSB

CA16 10u6.3X6 CA15 0.1u16X4 Closed PIN9

CA21.CA23 closed PIN25
CA14 close to PIN38

VCC3 CA20 10u6.3X6 CA19 0.1u16X4 Closed PIN1

CA21 0.1u16X4 CA23 22u6.3X6 CA14 10u6.3X6

UA1

EAPD/SPDIFI
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
SENSE A
SENSE B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
SENSE C
JDREF
BEEP
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L
GPIO1/DMIC-DATA
DVSS
AVSS
AVSS
ALC892-CG-RH

[30] EAPD
[13] AZ_SDOUT
[13] AZ_SDIN0
[13] AZ_SYNC
[13] AZ_RST#
[13] AZ_BITCLK
RA15 33R/4 SDIN0

Closed Pin3 CA18 10u6.3X6 REGREF

[30] SENSE_B SENSE_A SENSE_B

[30] MIC2_VREFO MIC1_V_R MIC1_V_L

LDOVDD
[30] LINE2_VREFO VREF

CA17 X_0.1u16X4 CA13 10u6.3X6 Closed Pin 27

JDREF RA18 20K1%4

C91-1011051-N07
ECA1 ECA3 2 100u10EL5
A_LOUT_R A_LOUT_L ALOUT_R ALOUT_L [30]

C91-1011051-N07
ECA4 ECA2 2 100u10EL5
A_LINE2_R A_LINE2_L LINE2_R LINE2_L [30]

A_LINE_IN_R A_LINE_IN_L CA12 CA11 10u6.3X6 LINE_IN_R LINE_IN_L

A_MIC1_R A_MIC1_L CA7 CA8 10u6.3X6 MIC1_R MIC1_L

A_MIC2_R A_MIC2_L CA9 CA10 10u6.3X6 MIC2_R MIC2_L [30]

[30] LOUT_L [30] LOUT_R LOUT_L LOUT_R

LIN_OUT

LOUT_R LOUT_L RA10 RA9 75R/4 LOUT_RA LOUT_LA FRONT_JD

DA1 ESD-MLVS0402L04 DA2 ESD-MLVS0402L04
D0G-2710510-I05 D0G-2710510-I05

AUDIO1B JACK-AUDIOX3F_PK/LIME/LIGHT BU-RH

LIN_IN

LINE_IN_R LINE_IN_L RA6 RA5 75R/4 LINE_IN_RA LINE_IN_LA LINE1_JD

CA4 100p50N4 CA3 100p50N4

AUDIO1A JACK-AUDIOX3F_PK/LIME/LIGHT BU-RH

MIC1_V_L MIC1_V_R RA2 RA1 2.2K/4 MIC1_LA MIC1_RA

MIC1

MIC1_R MIC1_L RA7 RA8 75R/4 MIC1_RA MIC1_LA MIC1_JD

CA1 CA2 100p50N4

AUDIO1C JACK-AUDIOX3F_PK/LIME/LIGHT BU-RH

for rear I/O 6port:
887VD/892:1k

for rear I/O 3port:
887VD/892:75R

D LIN_IN
E LIN_OUT
F MIC1
N54-13F0271-K06

129mA

5VDUAL LA1 0R/8 R11-0000034-W08

LDOVDD

CA22 ESD-MLVS0402L04 CA24 0.1u16X4 CA25 10u6.3X6

CA35,CA36 close to pin29

Closed Codec

SENSE_A
RA13 5.1K1%4 FRONT_JD
RA12 10K1%4 LINE1_JD
RA14 20K1%4 MIC1_JD

CA6 X_0.1u16X4 CA5 X_1000p50X/4 For EMI

CPA2 X_COPPER CPA1 X_COPPER

LOUT_RA LOUT_LA RA4 RA3 22K/4

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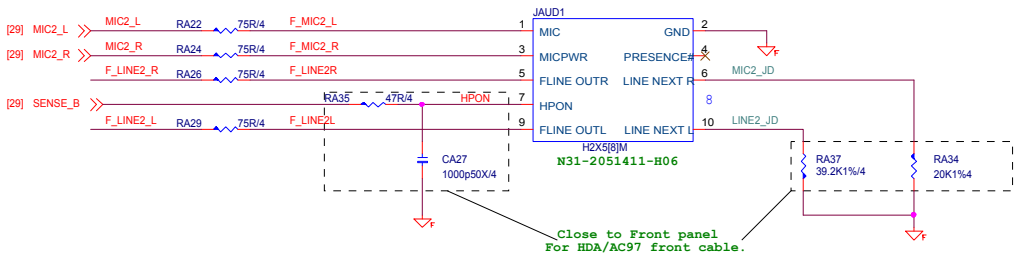
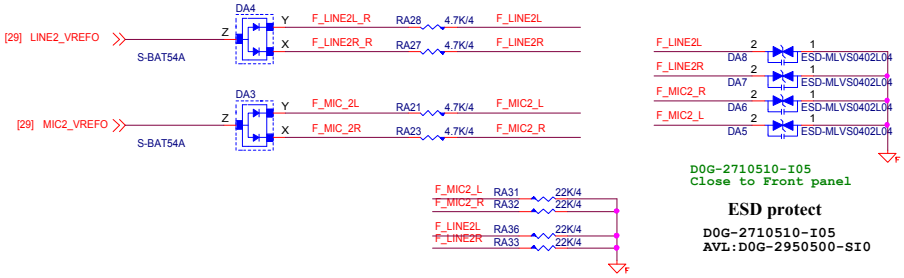
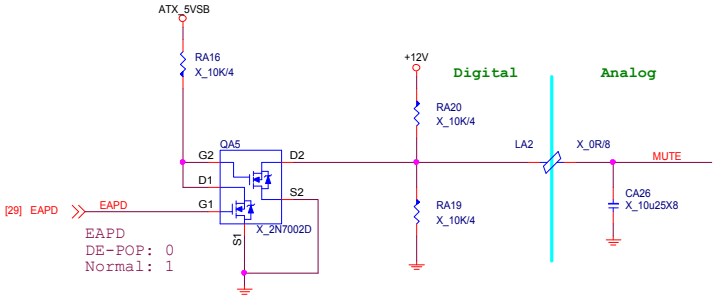
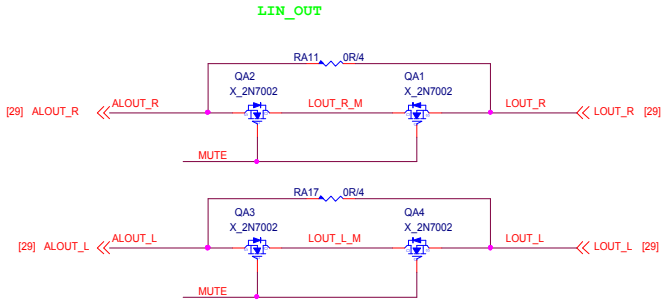
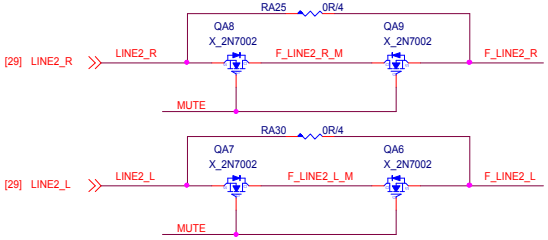




De-POP circuit







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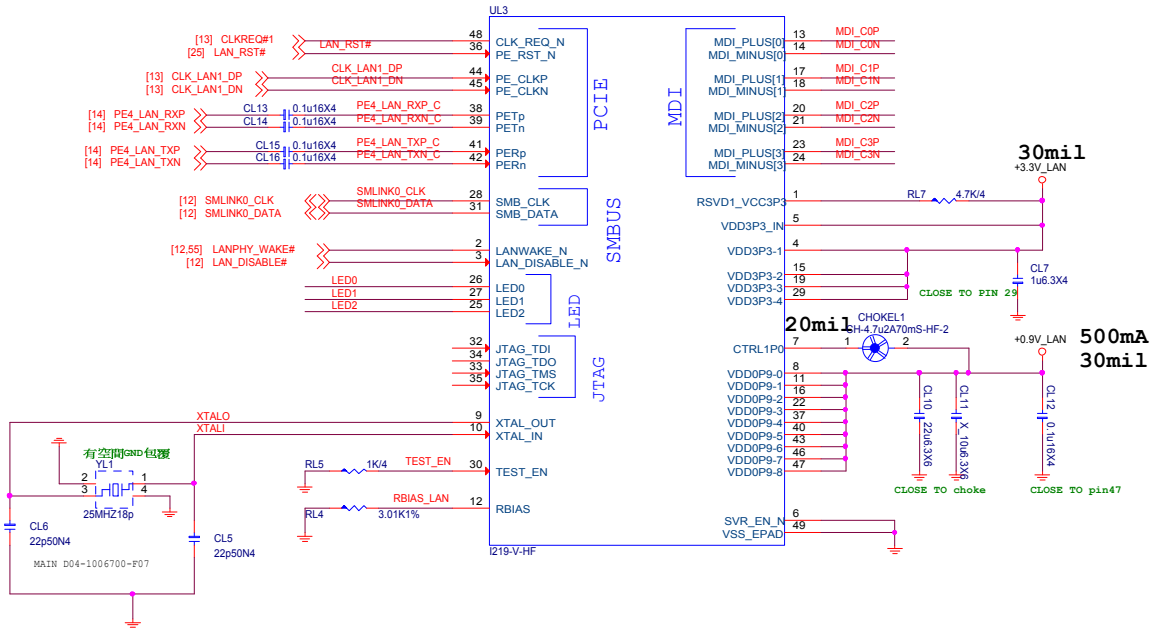
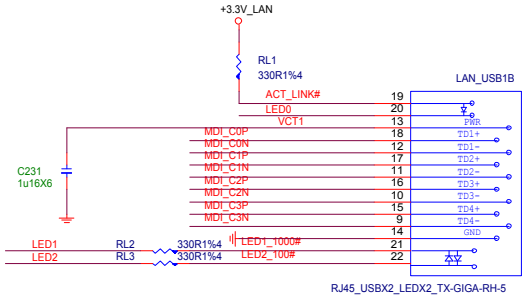
INTEL LAN - I219

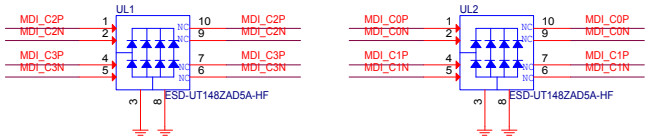


LAN Connector



ESD Protect

UL1 & UL2 close to connector



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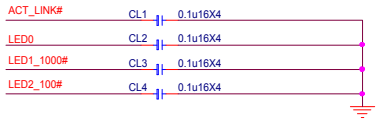
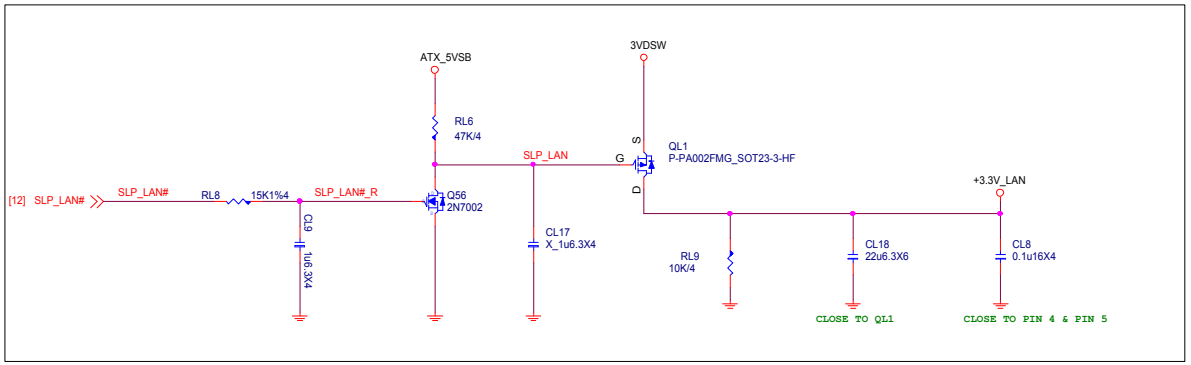


support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



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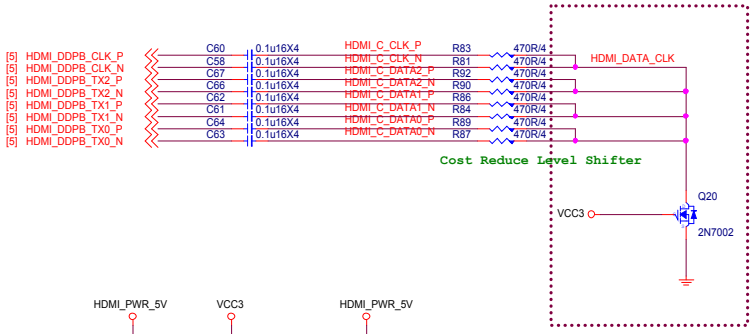
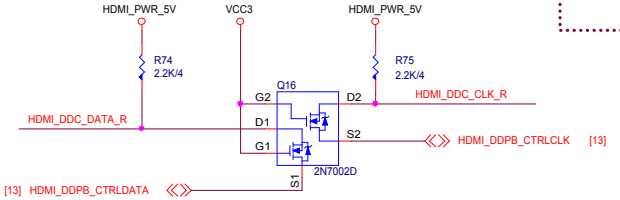
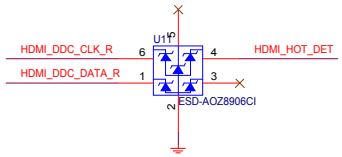
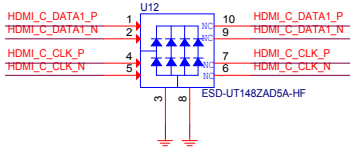
HDMI 1.4b

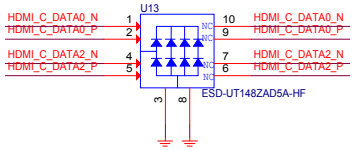
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

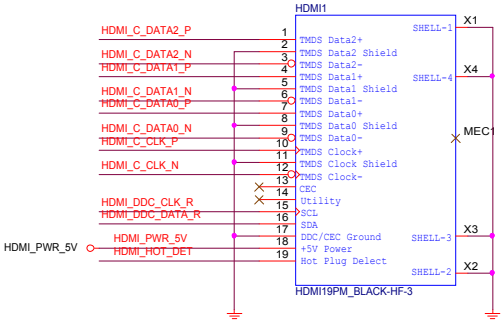




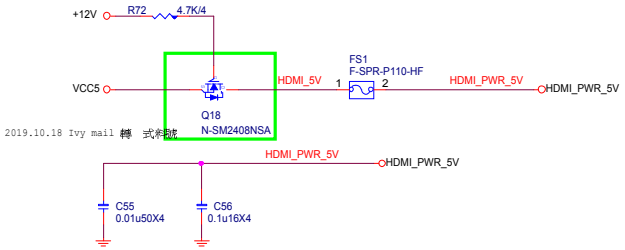




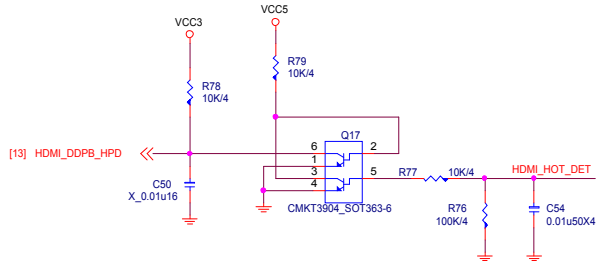




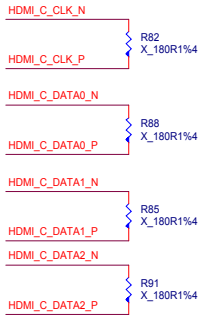
Vinafix.com



Hot Plug



For EMI



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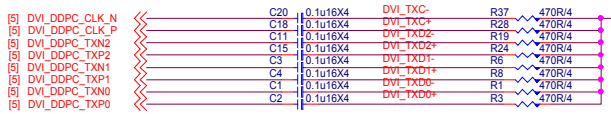
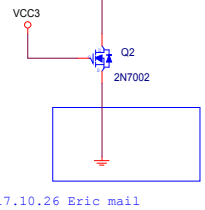
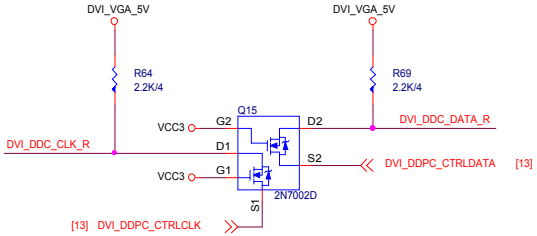
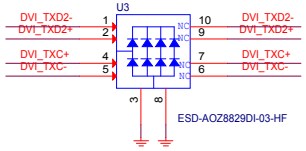
DVI

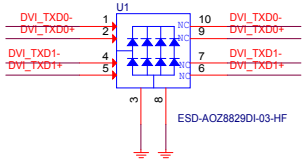


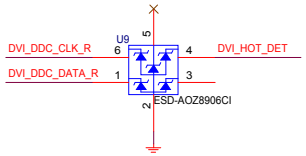


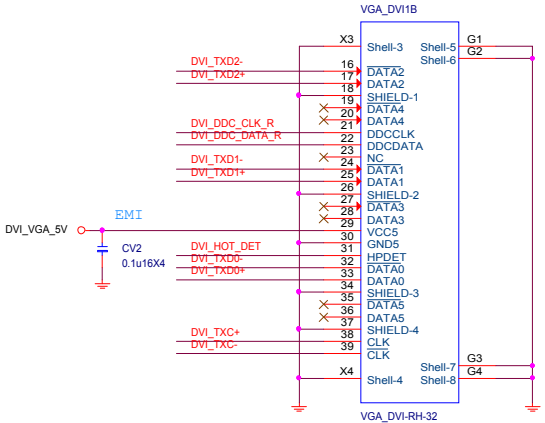
2017.10.26 Eric mail

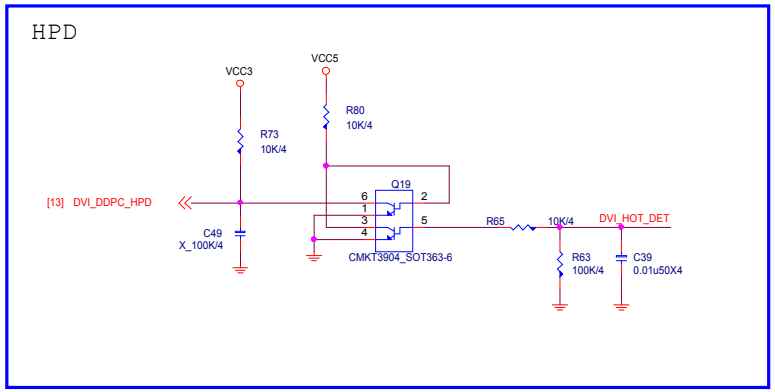


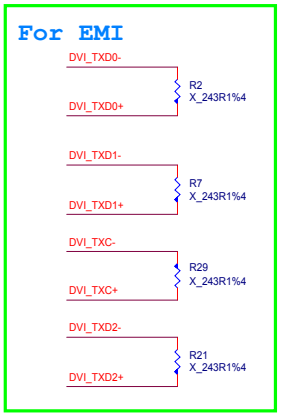


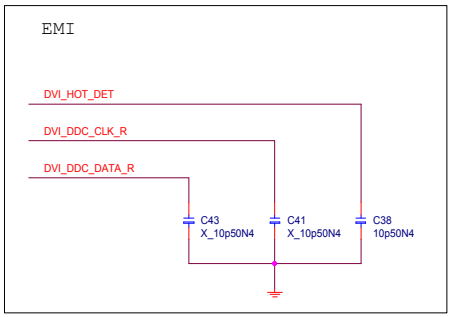












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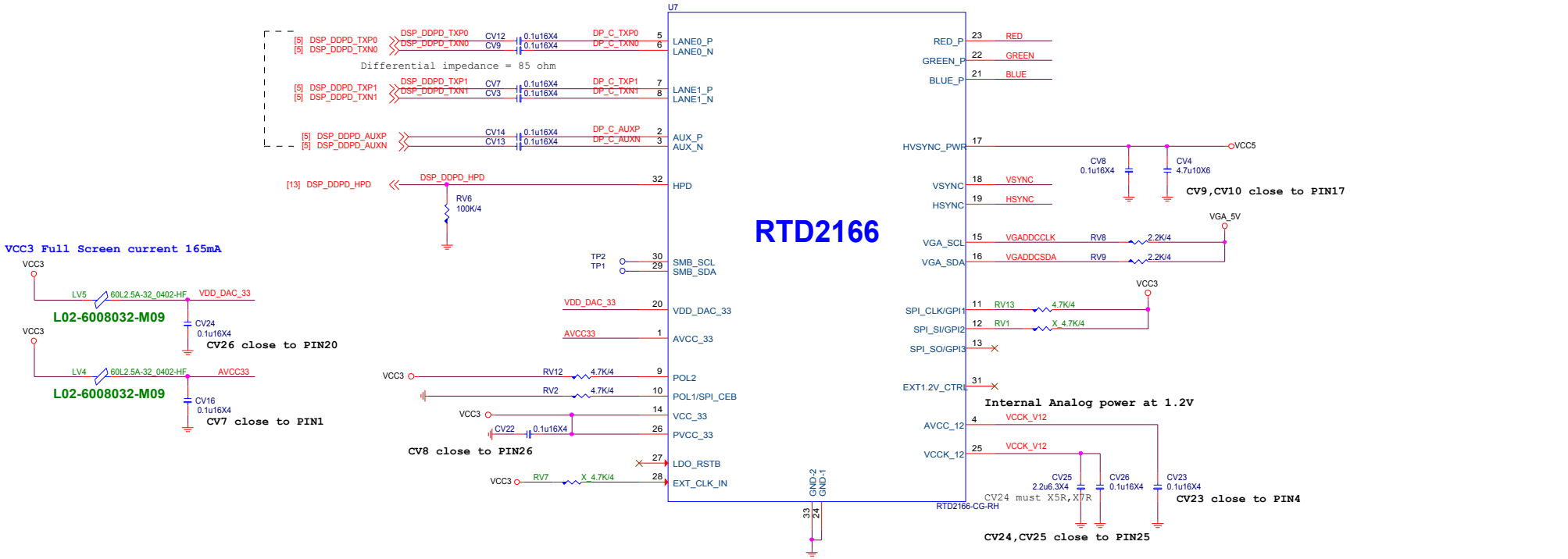
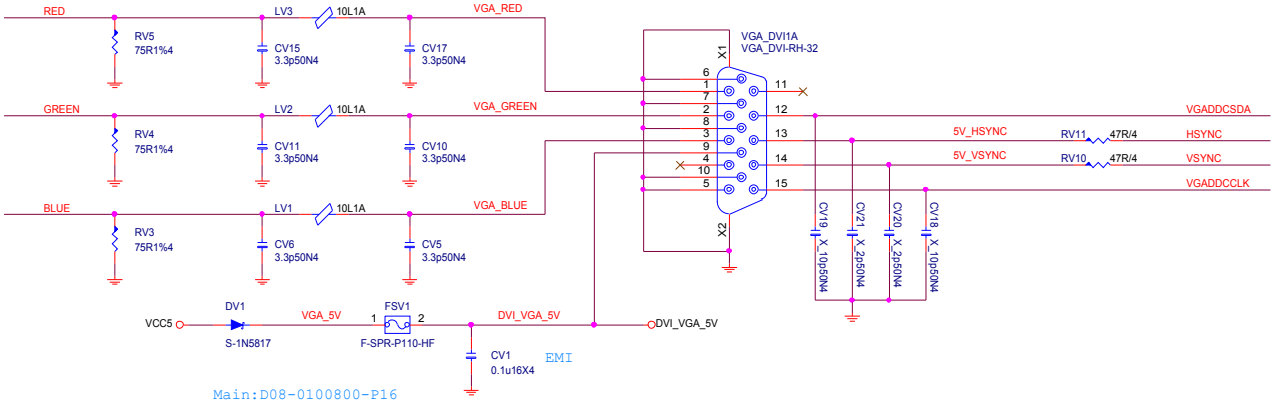
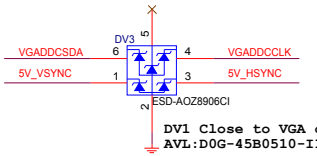
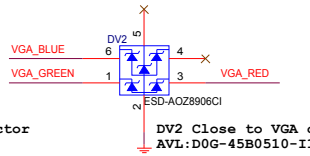
Note: If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining









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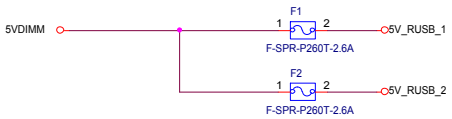
USB Port Power

Total:7.1A

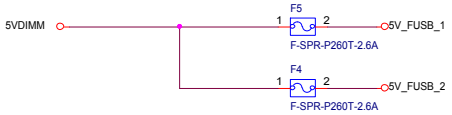
Total:4.3A



USB1: 1.8A

LAN_USB1+PS2_USB1 :0.5+1+1=2.5A

Total:2.8A



JUSB1 : 1A

JUSB2: 1.8A

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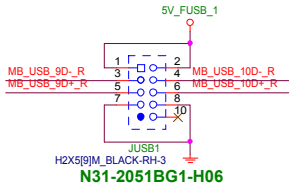
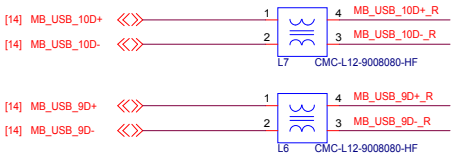
Front USB2.0

USB2.0 Port9.10

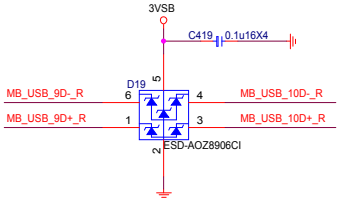
2A

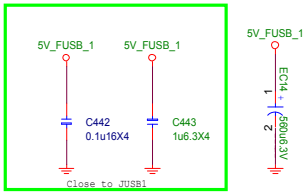


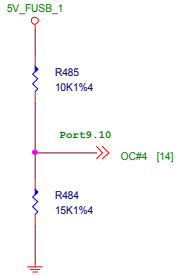
N31-2051BG1-H06



Vinafix.com







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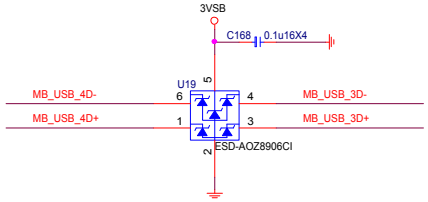
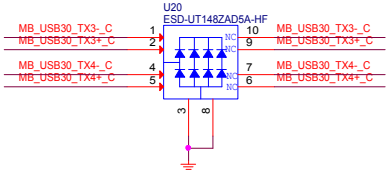
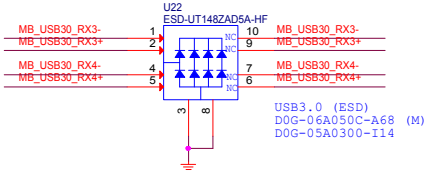
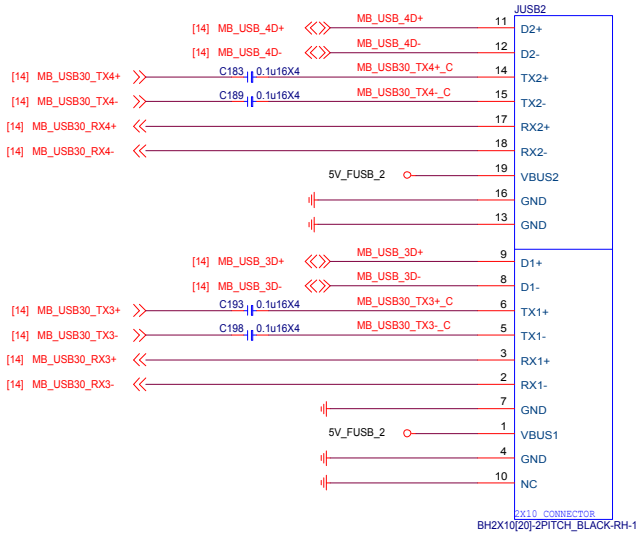
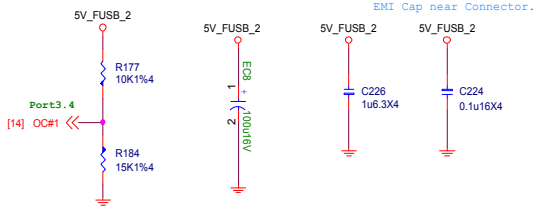
Front USB3.1 Gen1











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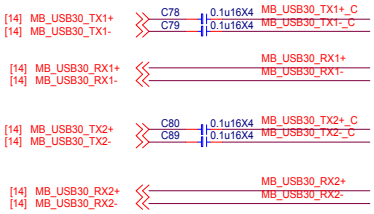
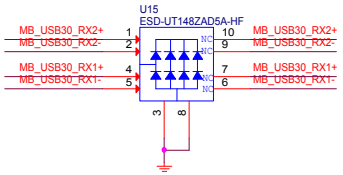
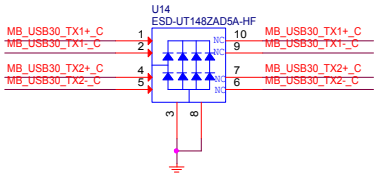
Rear USB3.0

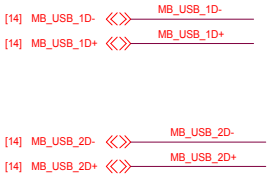
USB3.0 Port1.2
USB2.0 Port1.2

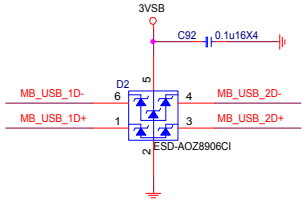
1.8A

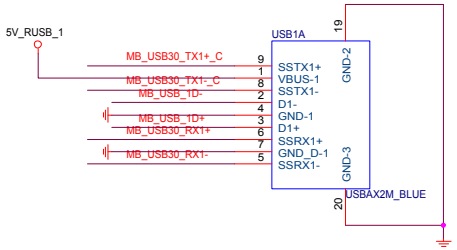


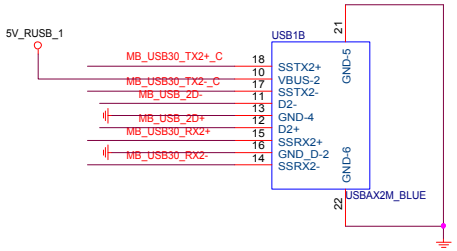


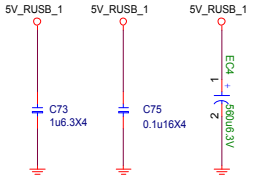


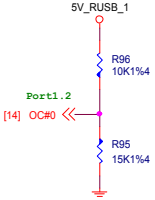












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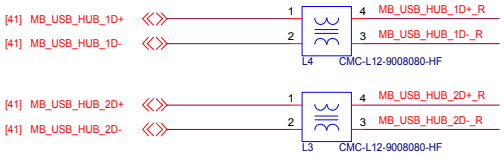
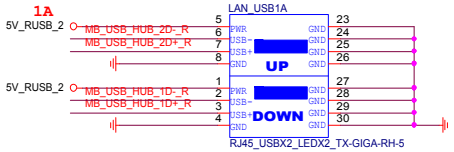
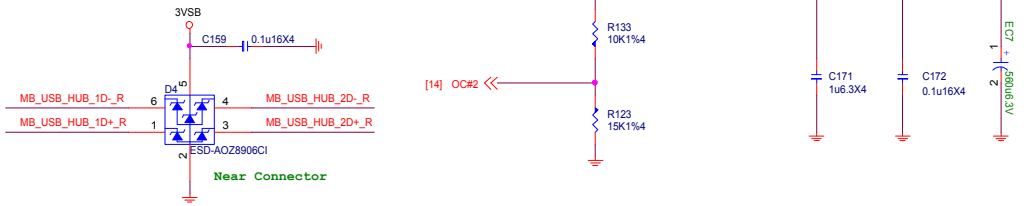
Rear LAN USB2.0

1A

JUSB1 HUB 1 . 2







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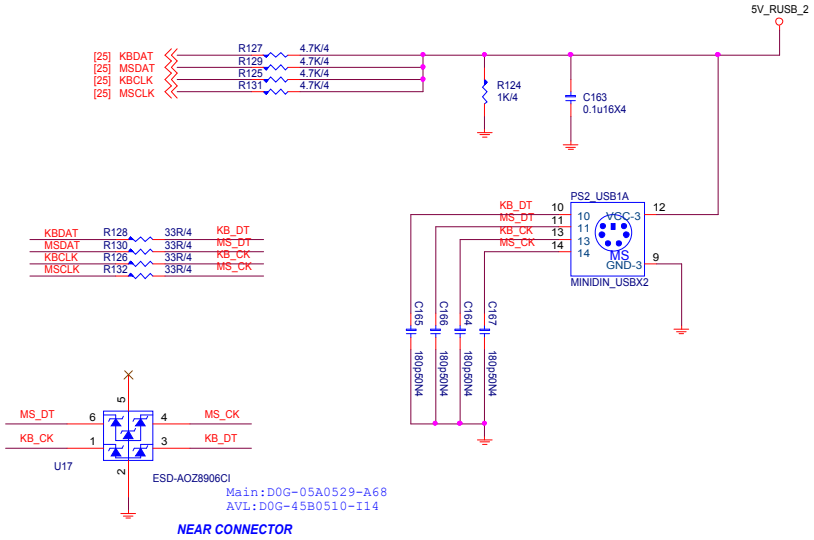
PS2 Connector



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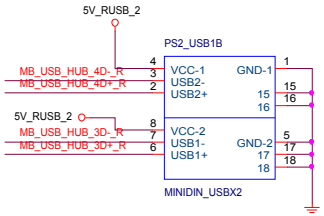
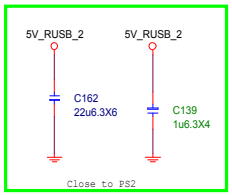
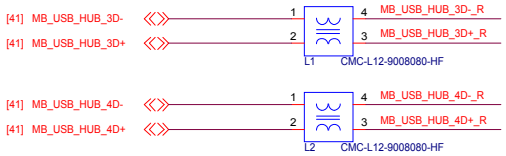
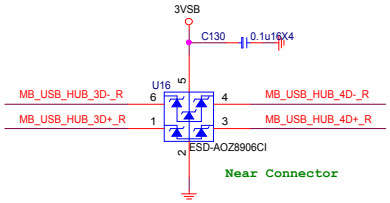
PS2 USB Connector

JUSB2 HUB 3.4









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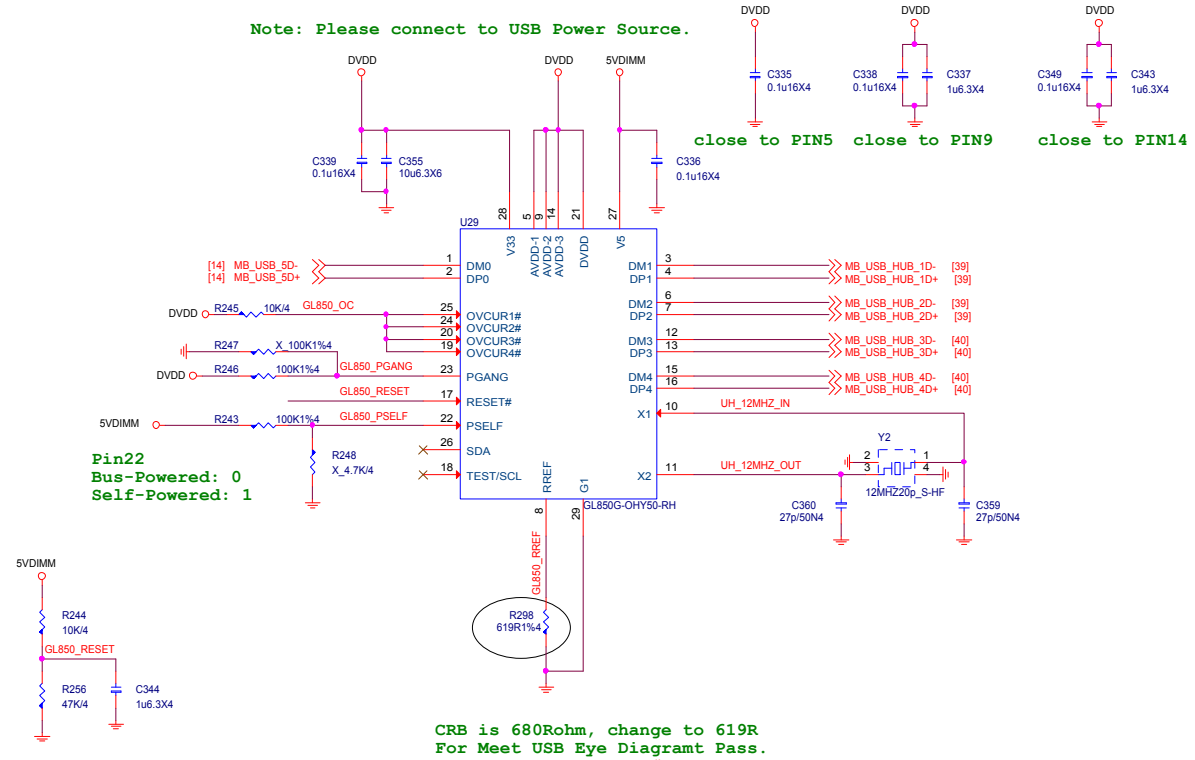
Rear USB2.0 HUB

Note: Please connect to USB Power Source.



Pin23
Gang input:1
Individual input:0

Pin22
Bus-Powered: 0
Self-Powered: 1

CRB is 680Rohm, change to 619R
For Meet USB Eye Diagramt Pass.

Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

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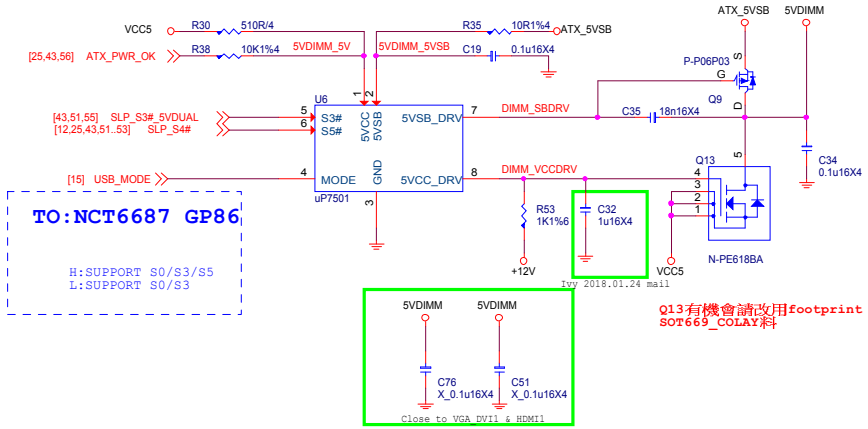
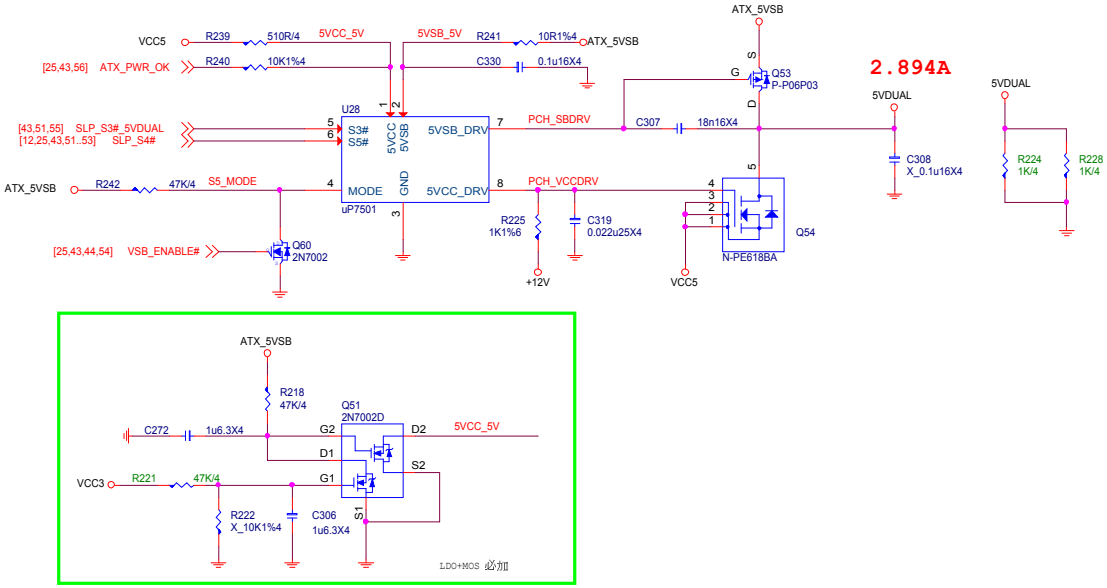
5VDIMM FOR DDR

10.98A



5VDUAL

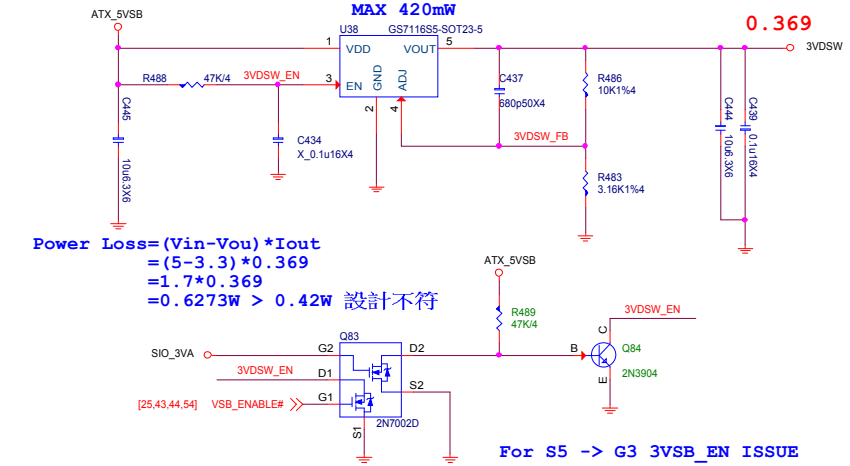
2.894A



3VDSW

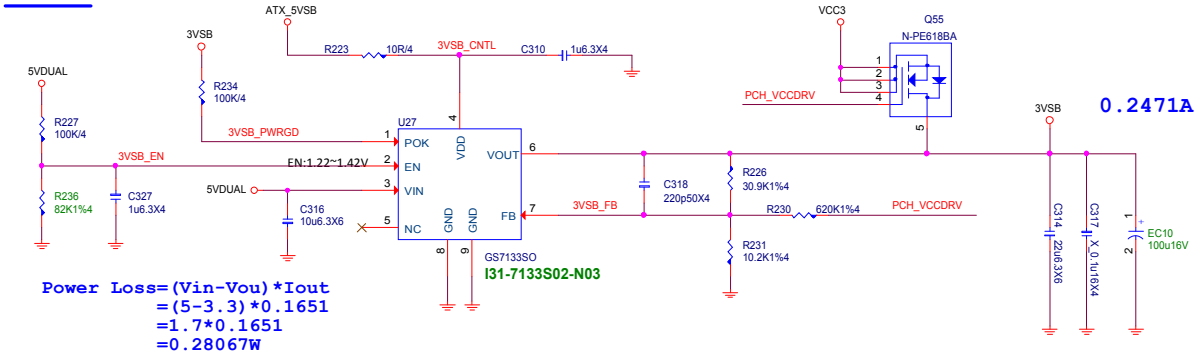
MAX 420mW

0.369



3VSB

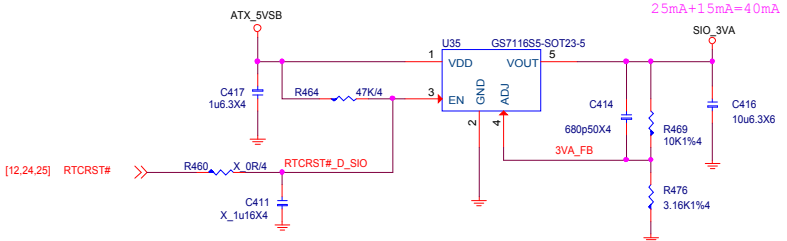
0.2471A

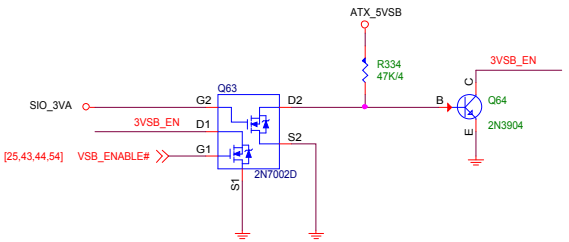


SIO_3VA

Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.04
=1.7*0.04
=0.068W

25mA+15mA=40mA





For S5 -> G3 3VSB_EN ISSUE

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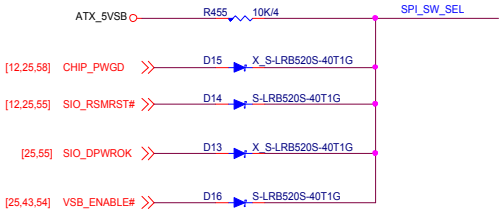
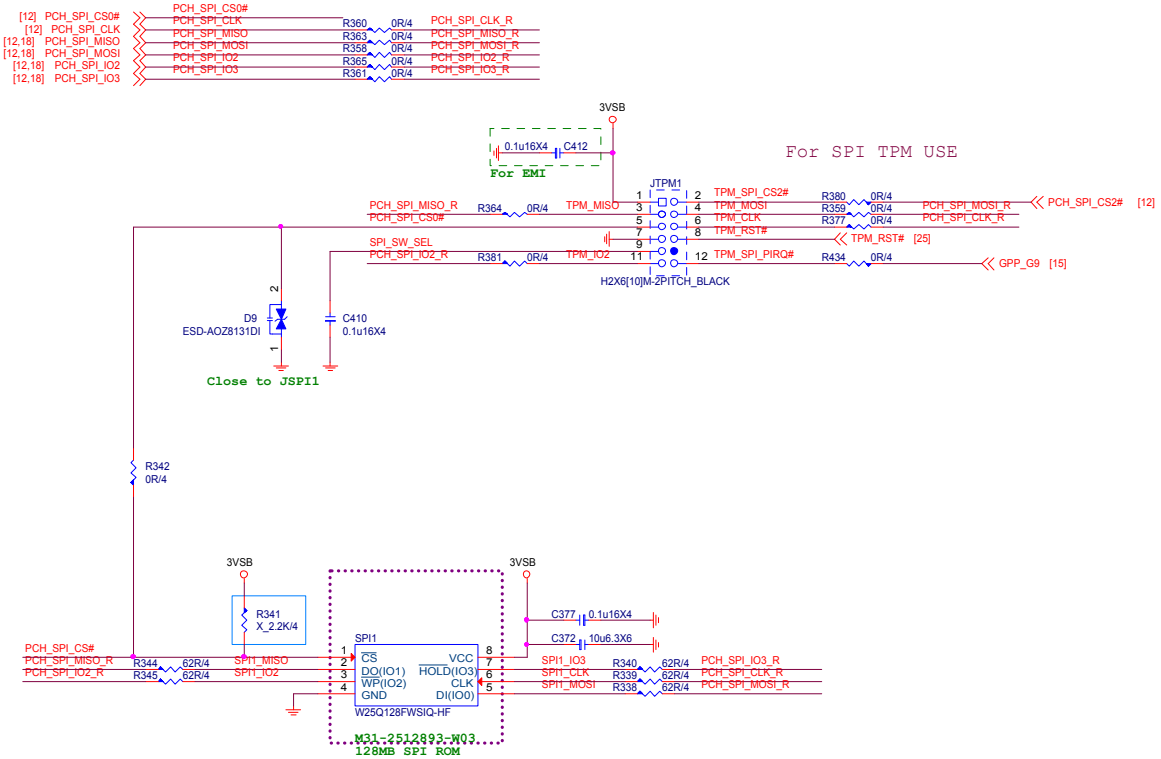
Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.



For TL624-1.
DEEP Mode : Stuff D48/R2517
DSW Mode : Stuff D48/D49/R2517



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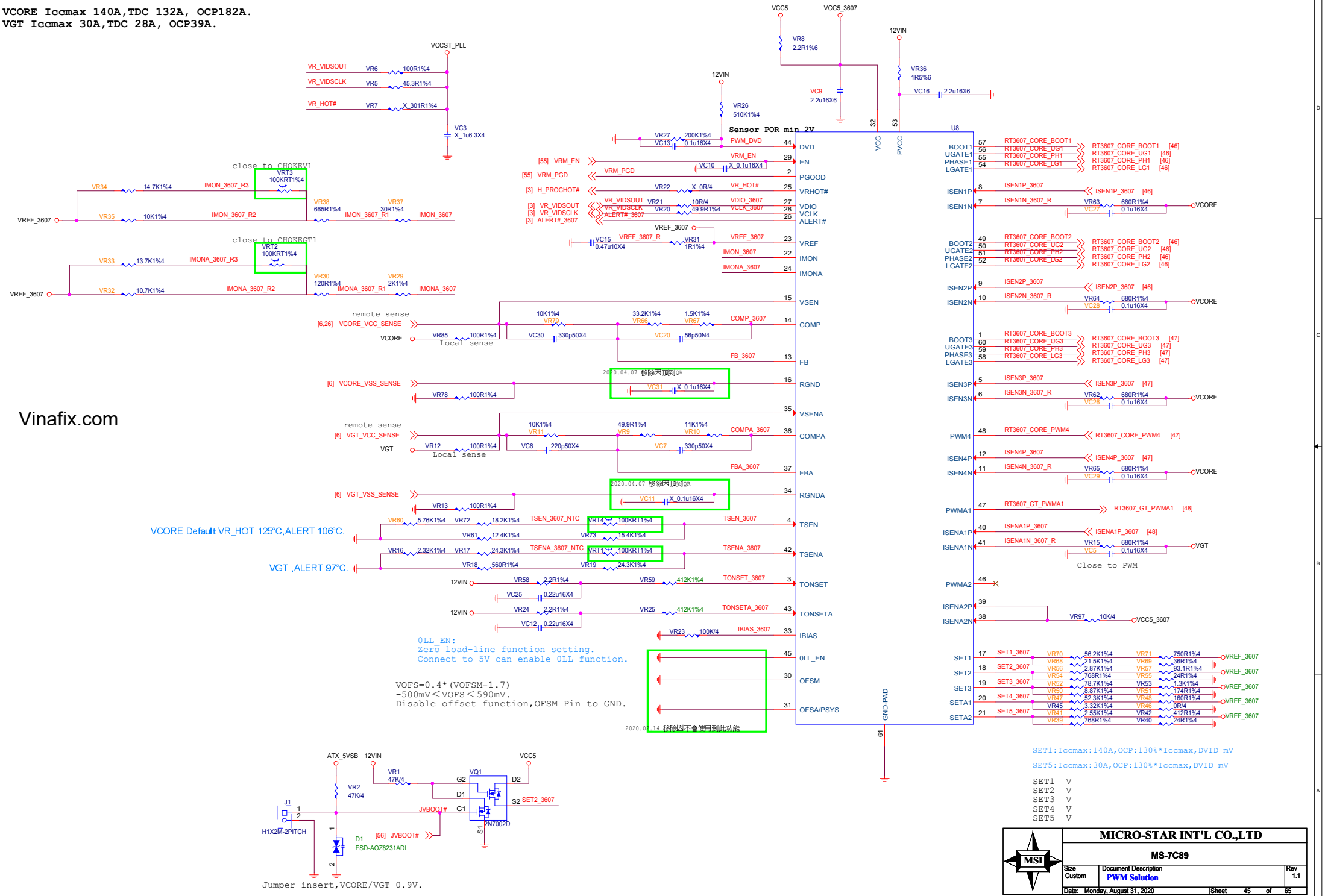
VCORE Iccmax 140A,TDC 132A, OCP182A.
VGT Iccmax 30A,TDC 28A, OCP39A.



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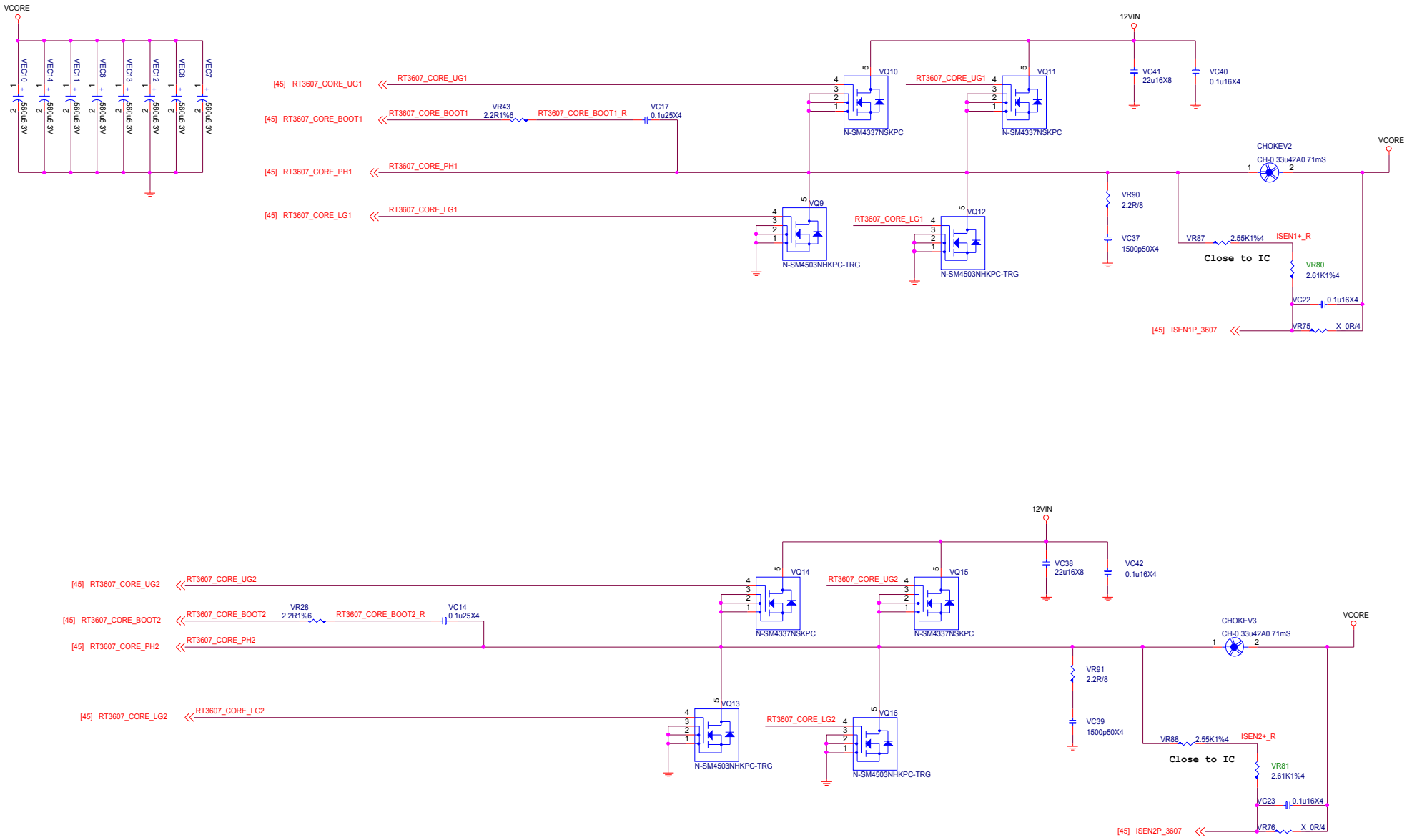

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Size: Custom	Document Description: VCORE MOS-PHASE 1~2	Rev: 1.1
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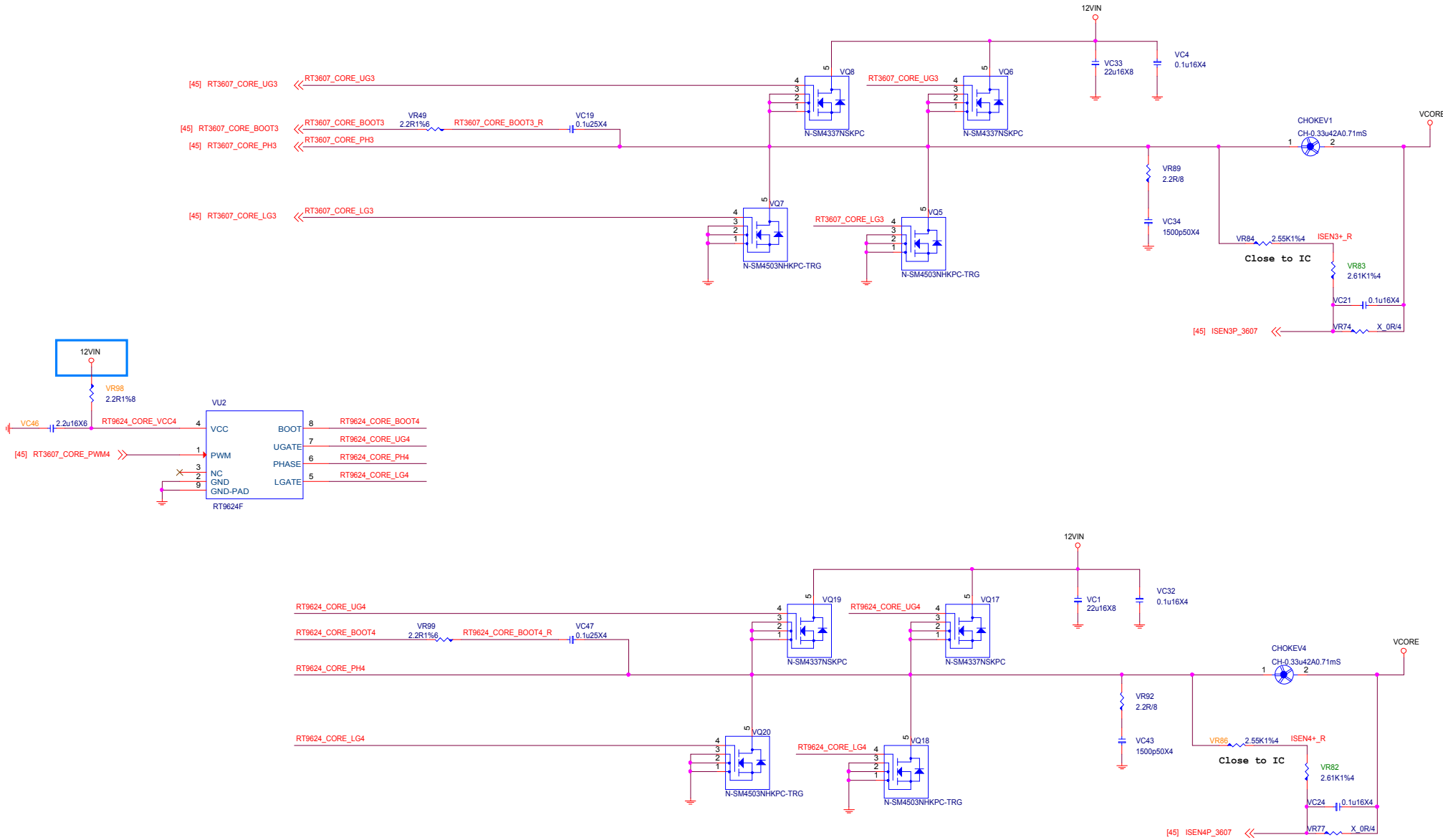

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Size: Custom	Document Description: VCORE MOS-PHASE 3~4	Rev: 1.1
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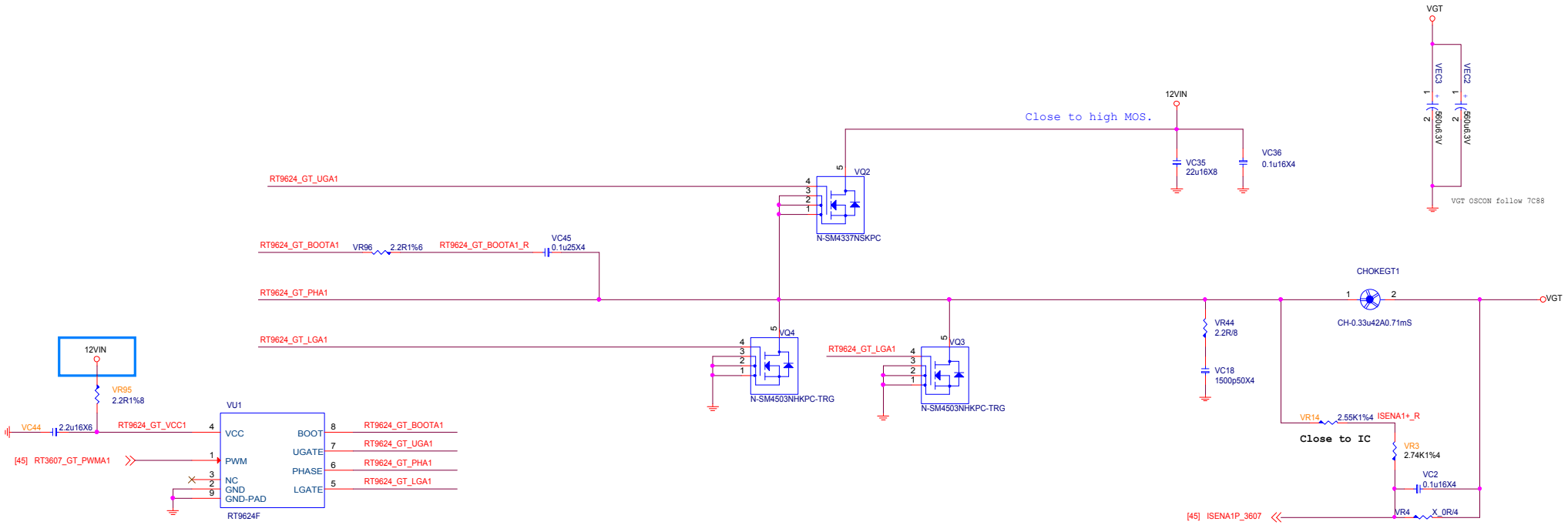
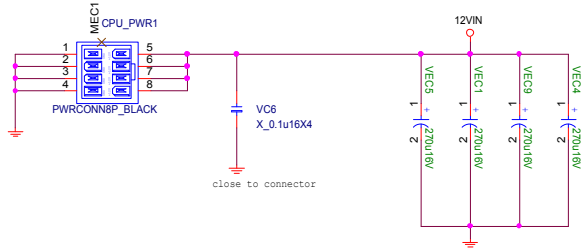


12VIN CONNECTOR



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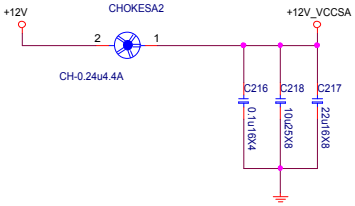
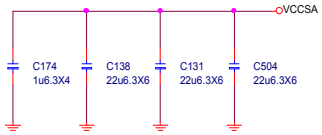
SA Power:1.05V,11.1A

Current limit: 13A~18A, TYP=15A

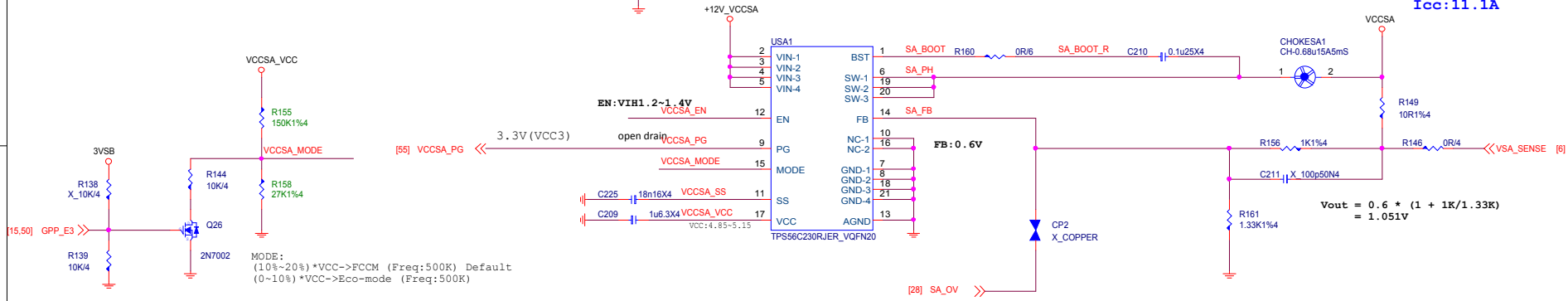
OCP real 16A



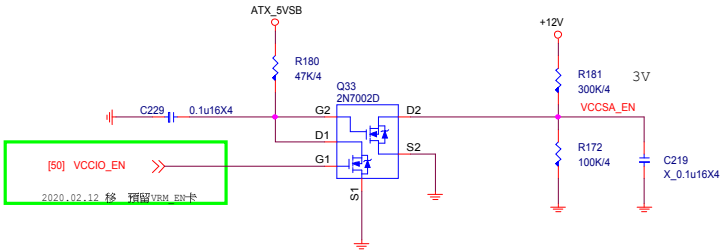
Irms1 = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1 * 0.2825
= 3.136A

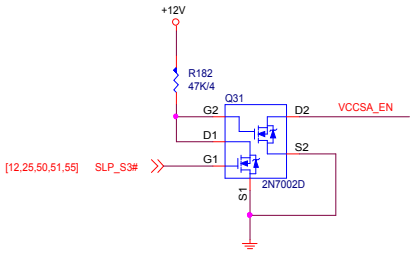


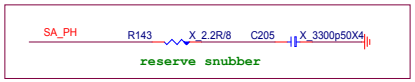
1.05V
Icc:11.1A



MODE:
(10%~20%)*VCC->FCCM (Freq:500K) Default
(0~10%)*VCC->Eco-mode (Freq:500K)







SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

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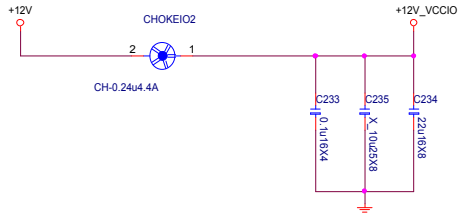
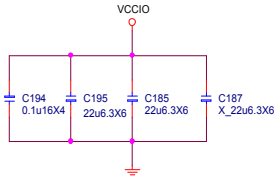
VCCIO Power 0.95,6.4A

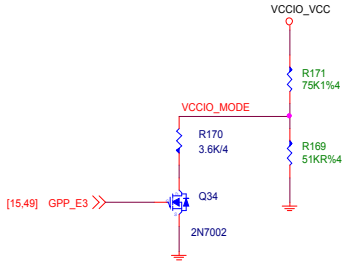
0.95V Icc:6.4A

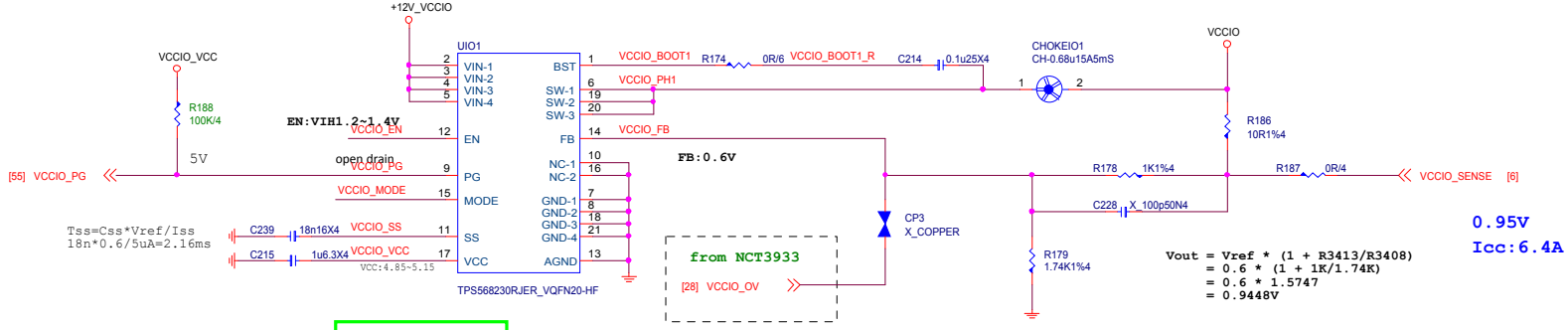
OCP real 10.5A



Irms1 = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 6.4 * 0.27
= 1.728A



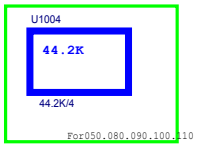


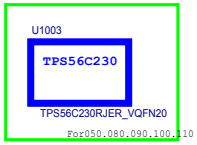


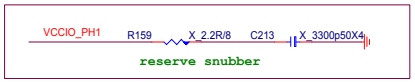
Vout = Vref * (1 + R3413/R3408)
= 0.6 * (1 + 1K/1.74K)
= 0.6 * 1.5747
= 0.9448V

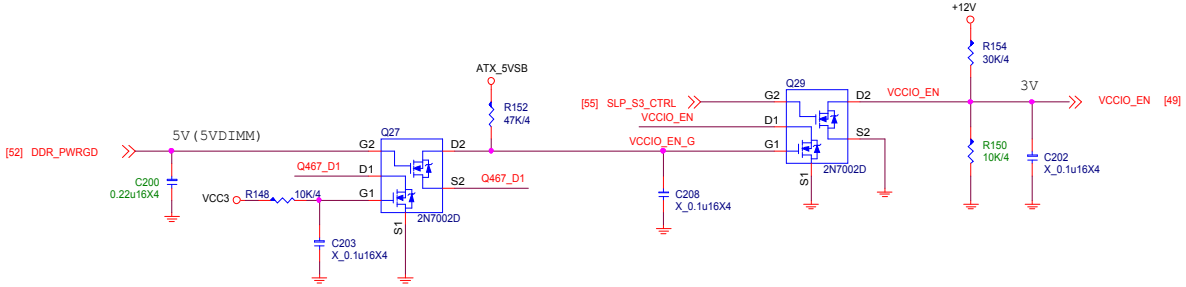
0.95V
Icc:6.4A

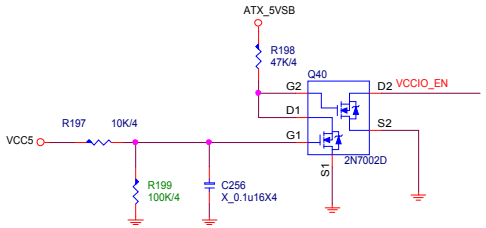
MODE:
RM_H:75K,RM_L:51K->FCCM (Freq:800K) Default
RM_H:330K,RM_L:15K->Eco-mode (Freq:800K)

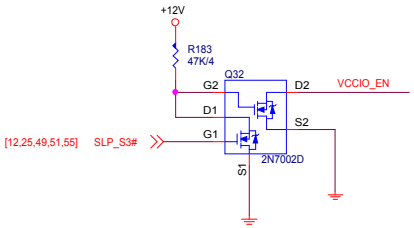


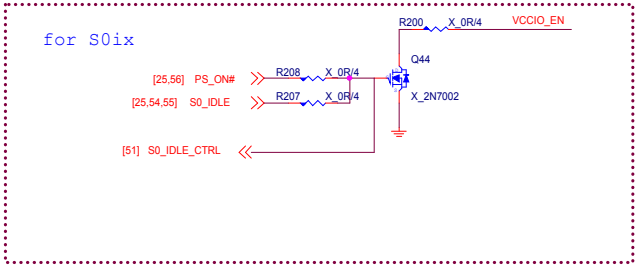












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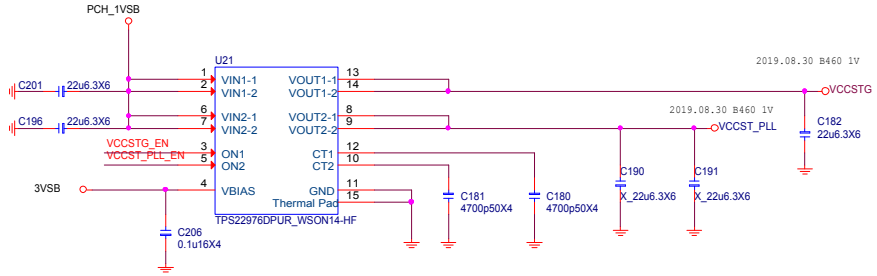
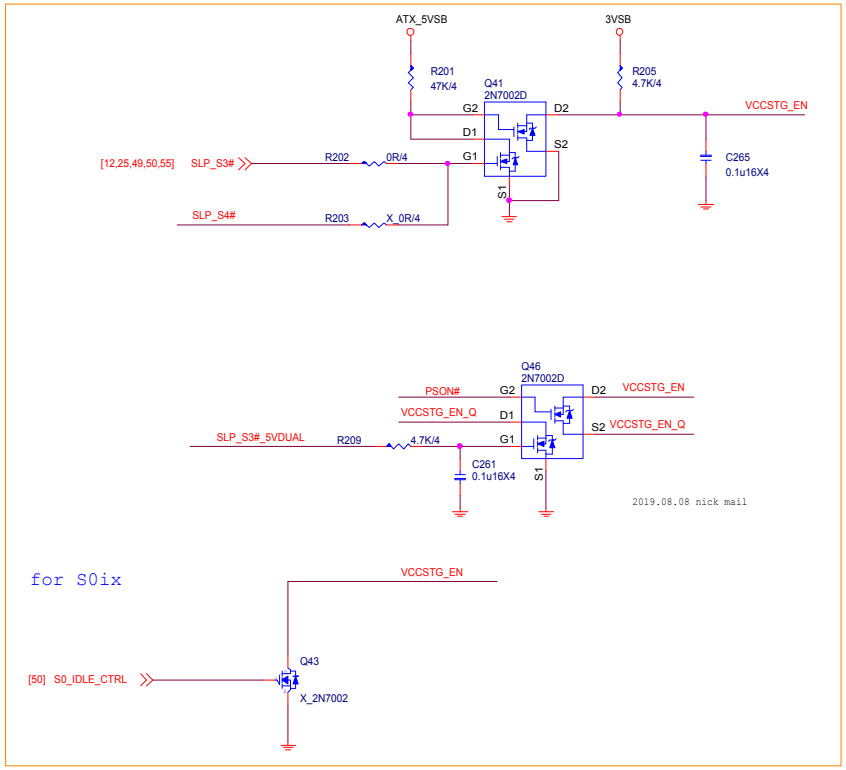
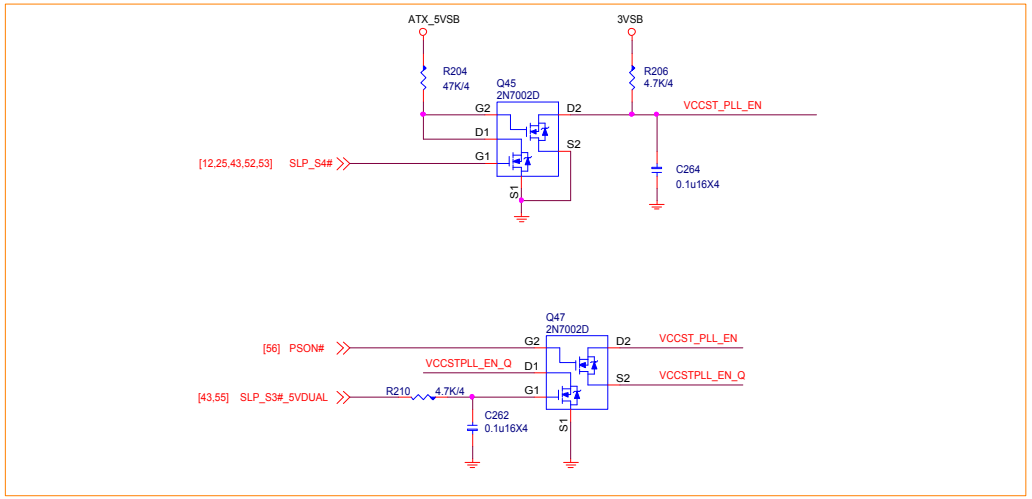
VCCST PLL 1.0V; 0.45A
VCCSTG 1.0V; 0.2A

Power Loss1=(I*I)*Rds(on)
=(0.45*0.45)*0.022
=0.2025*0.022
=4.455mW

Power Loss2=(I*I)*Rds(on)
=(0.2*0.2)*0.022
=0.04*0.022
=0.88mW







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DDR4 Power:1.2V,8.77A

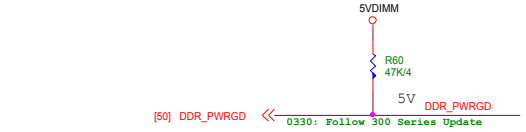
3.7A For CPU
0.225A For CPU(VCCSTPLL)
4.6A For 2DIMM
0.375A For DDR VTT

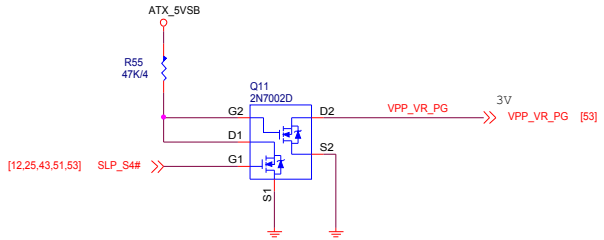
OCP = 12.5~16.6A; Choke Isat=32A

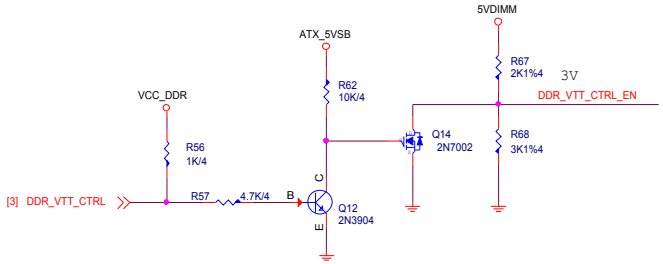
*Rlimit = Llimit * Rds * 10 /5uA*
*= 15.8*3.9*10/5 = 123.24K*

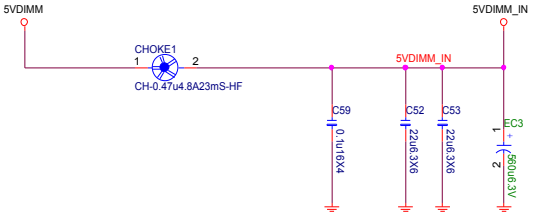
*0.4V<=Rlimit *5uA<=3V*
*123.24*0.005=0.6162*

D03-4503N0C-ST8
*Current limit= 124K*5uA/10/5.1mohm)=12.16A*
*Current limit= 124K*5uA/10/3.9mohm)=15.9A*

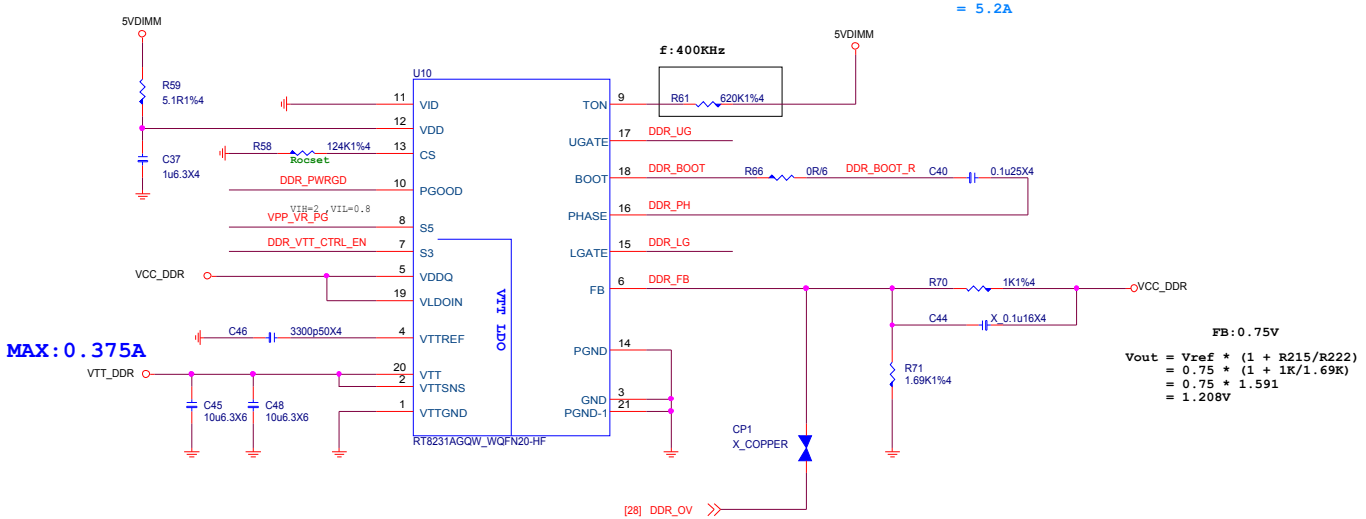








Irms = Iout * SQRT((Vout/Vin) * (1-(Vout/Vin)))
=12.15* 0.427
= 5.2A

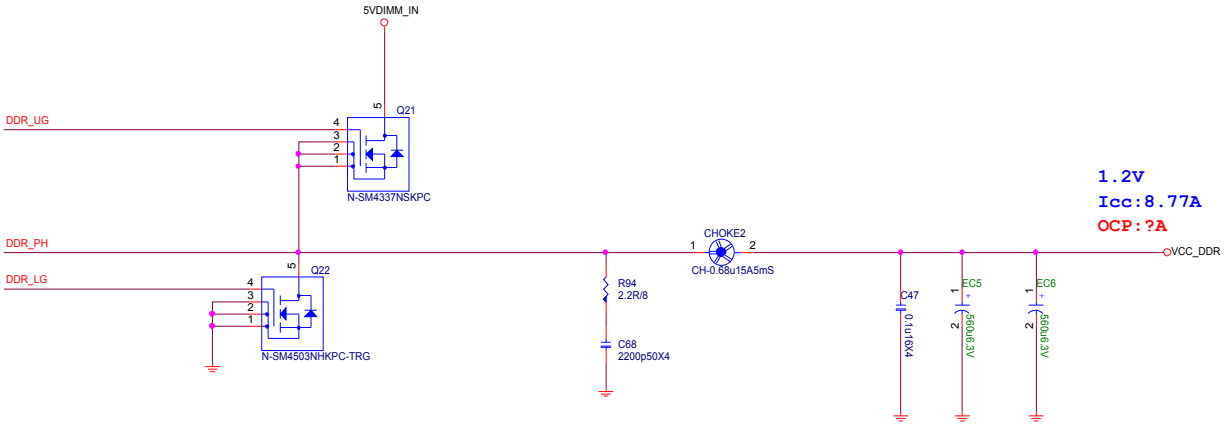


MAX:0.375A

FB:0.75V

Vout = Vref * (1 + R215/R222)
= 0.75 * (1 + 1K/1.69K)
= 0.75 * 1.591
= 1.208V

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 13.5* 0.427
= 5.765A



1.2V
Icc:8.77A
OCP:?A

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VPP2.5V Power:2.5V,3A

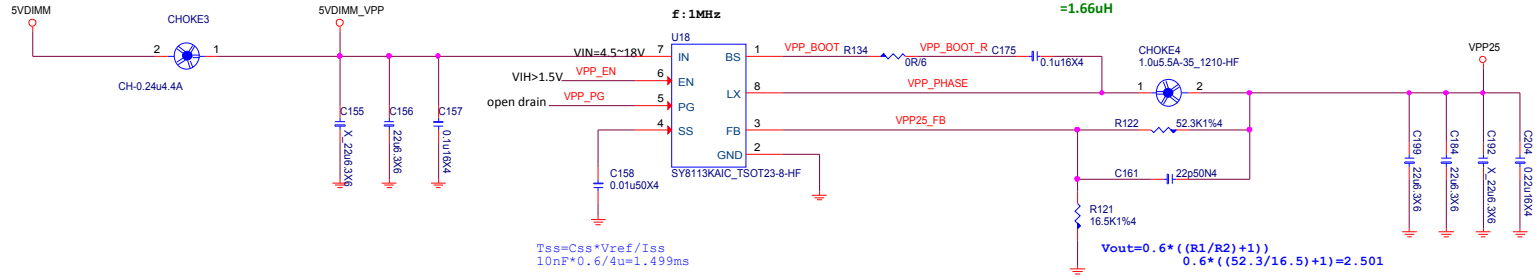
IC OCP:4.6

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 3 * 0.5
     = 1.5A
```

OCP real 3.8A

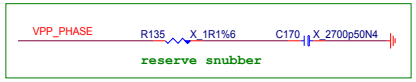
L=(Vout-(1-Vout/Vin))/(Fsw*Iout*0.4)
=1.66uH

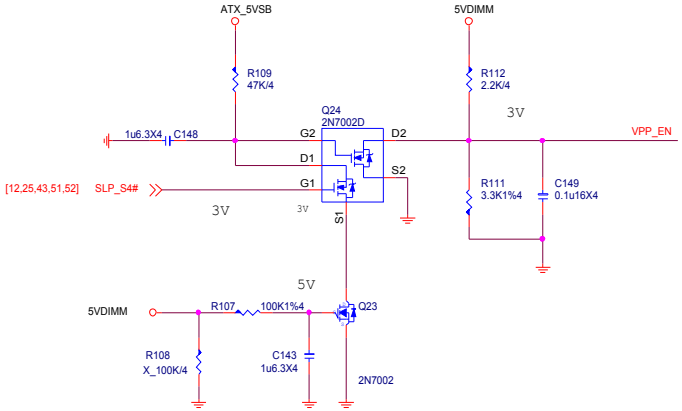
f:1MHz

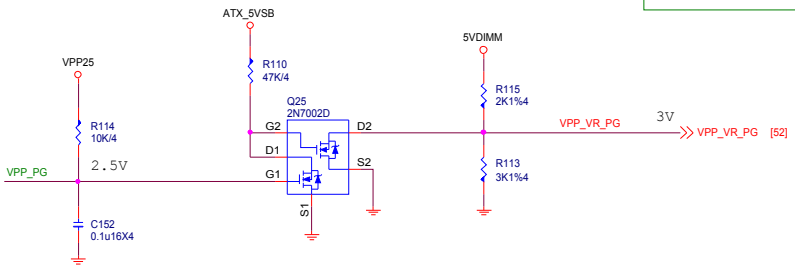


Tss=Css*Vref/Iss
10nF*0.6/4u=1.499ms

Vout=0.6*((R1/R2)+1))
0.6*((52.3/16.5)+1)=2.501







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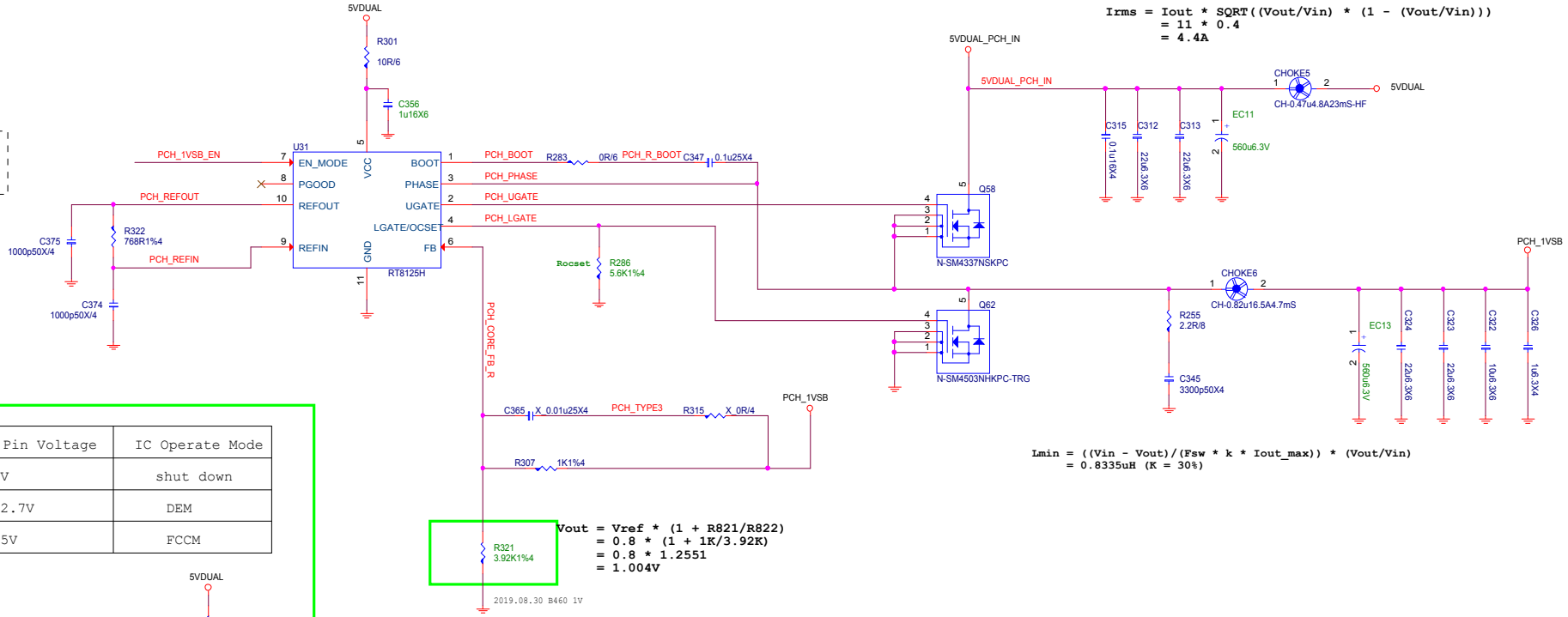
PCH_1VSB Power:1V,9.208+0.65=9.858A

OCP = 11.66~15.55A

```
Iocp =Rocset* Iocset /Rdson(low)
      =5.6K*10uA/3.9m
      =14.36A
Iocp =Rocset* Iocset /Rdson(max)
      =5.6K*10uA/5.1m
      =10.98A
```

Rdson(Low Side) 5V
D03-4503N0C-ST8:3.9 ~5.1 mohm

Note: Rocset(min)=5K

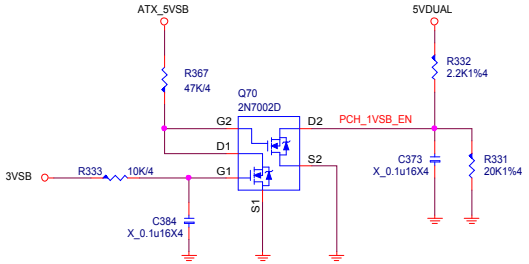


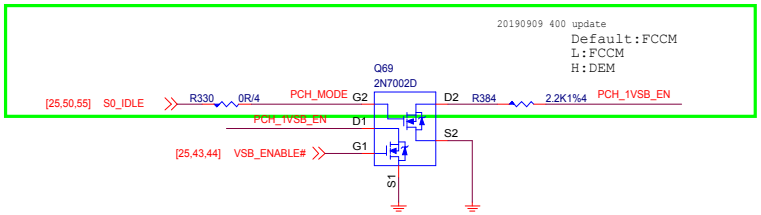

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 11 * 0.4
     = 4.4A
```

```
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
     = 0.8335uH (K = 30%)
```

```
Vout = Vref * (1 + R821/R822)
     = 0.8 * (1 + 1K/3.92K)
     = 0.8 * 1.2551
     = 1.004V
```

EN_MODE Pin Voltage	IC Operate Mode
<0.4V	shut down
2.1~2.7V	DEM
4.3~5V	FCCM





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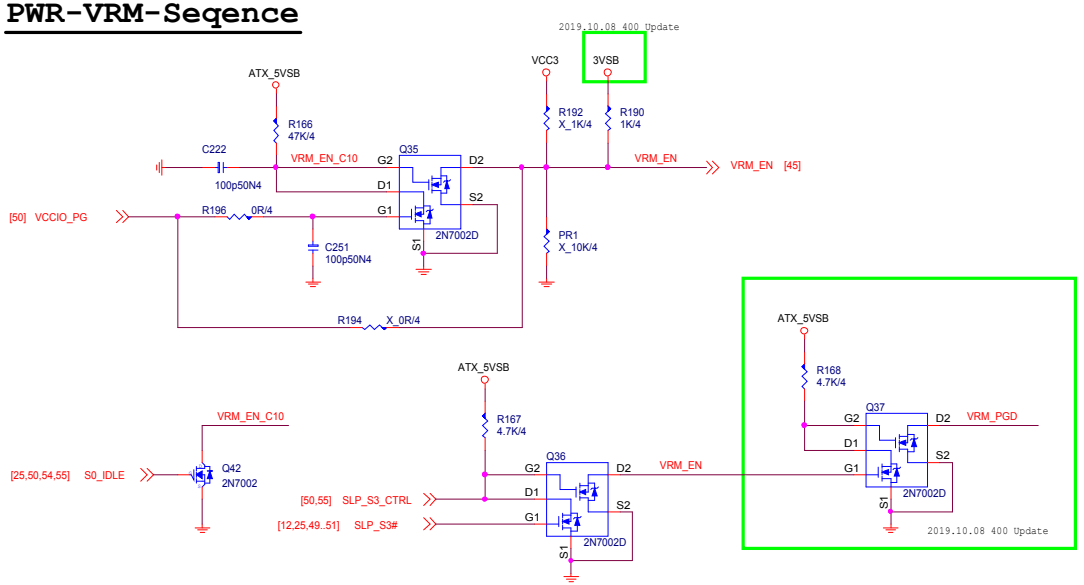
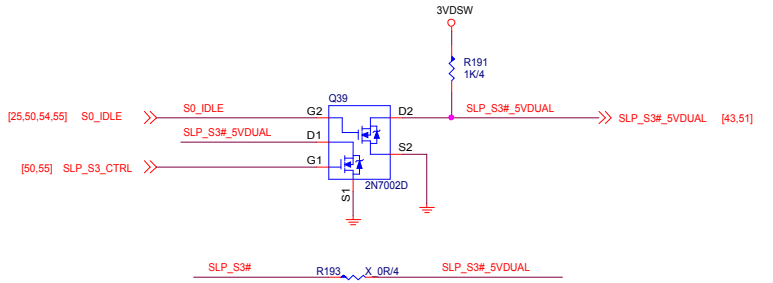
PWR-VRM-Seqence

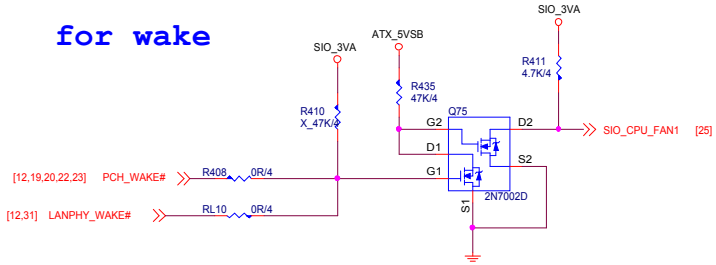


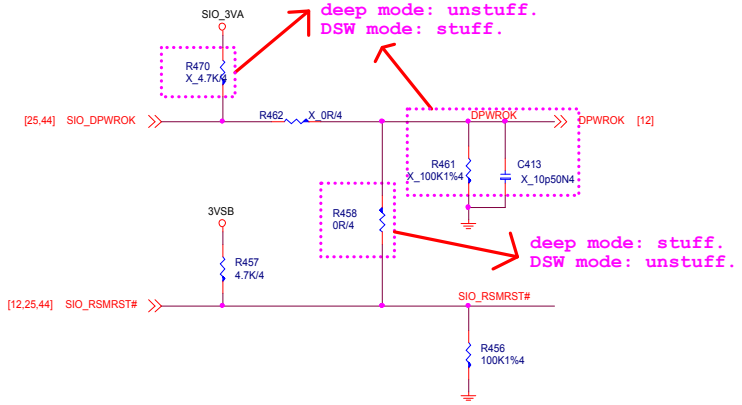
for 5VDIMM and 5VDUAL

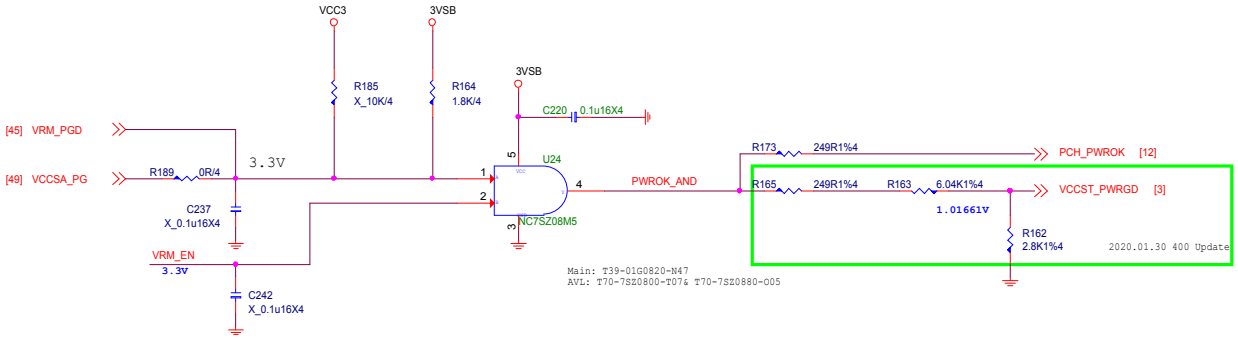
for S0ix



for wake







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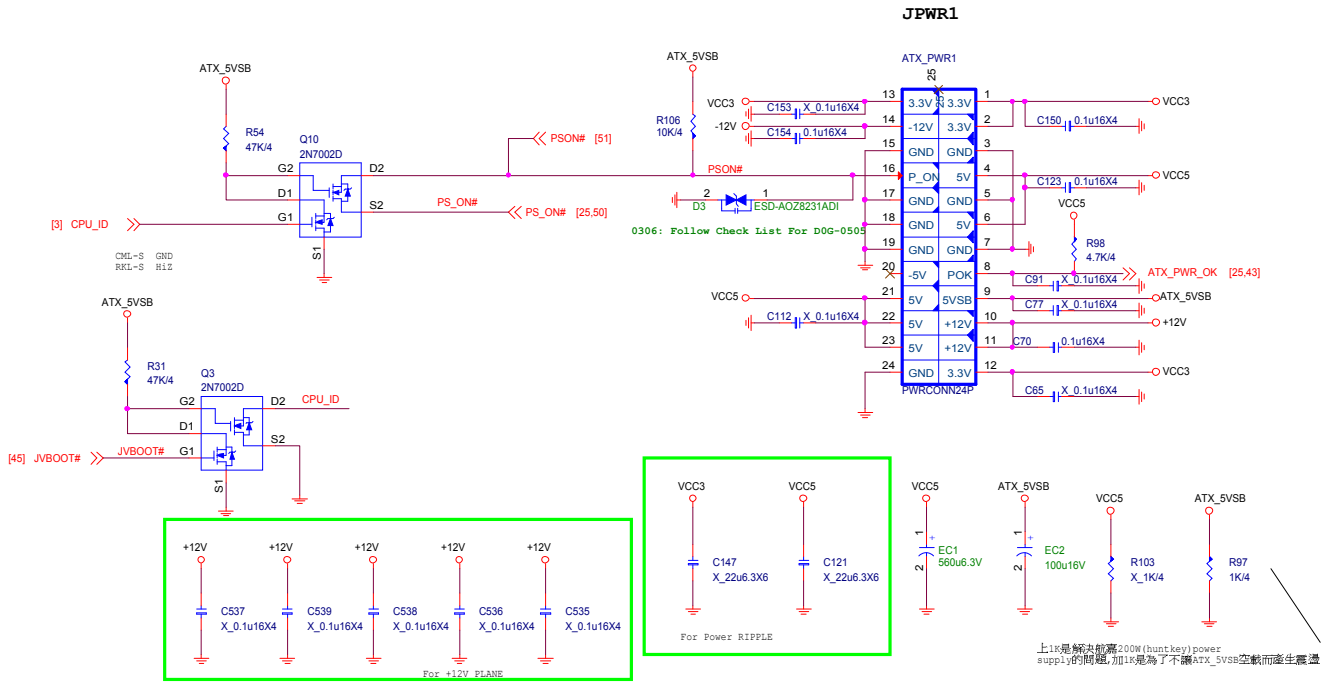
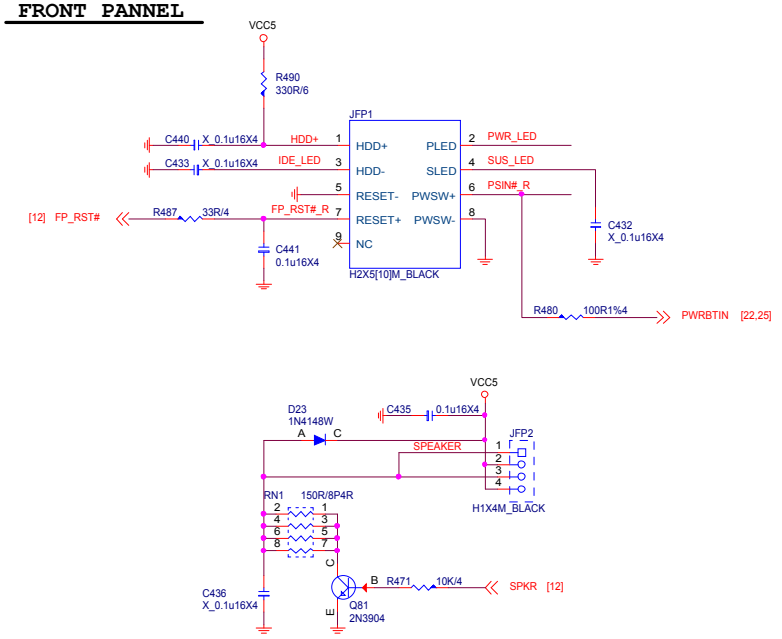
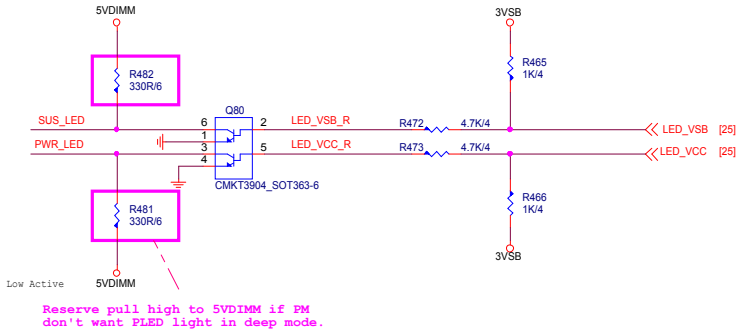
ATX POWER CONNECTOR

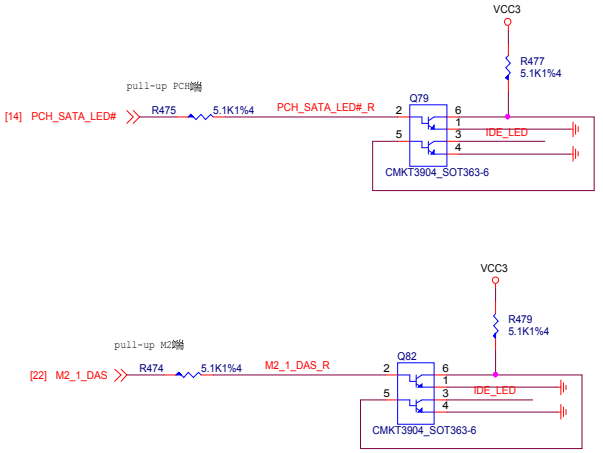


FRONT PANNEL



Front Panel LED





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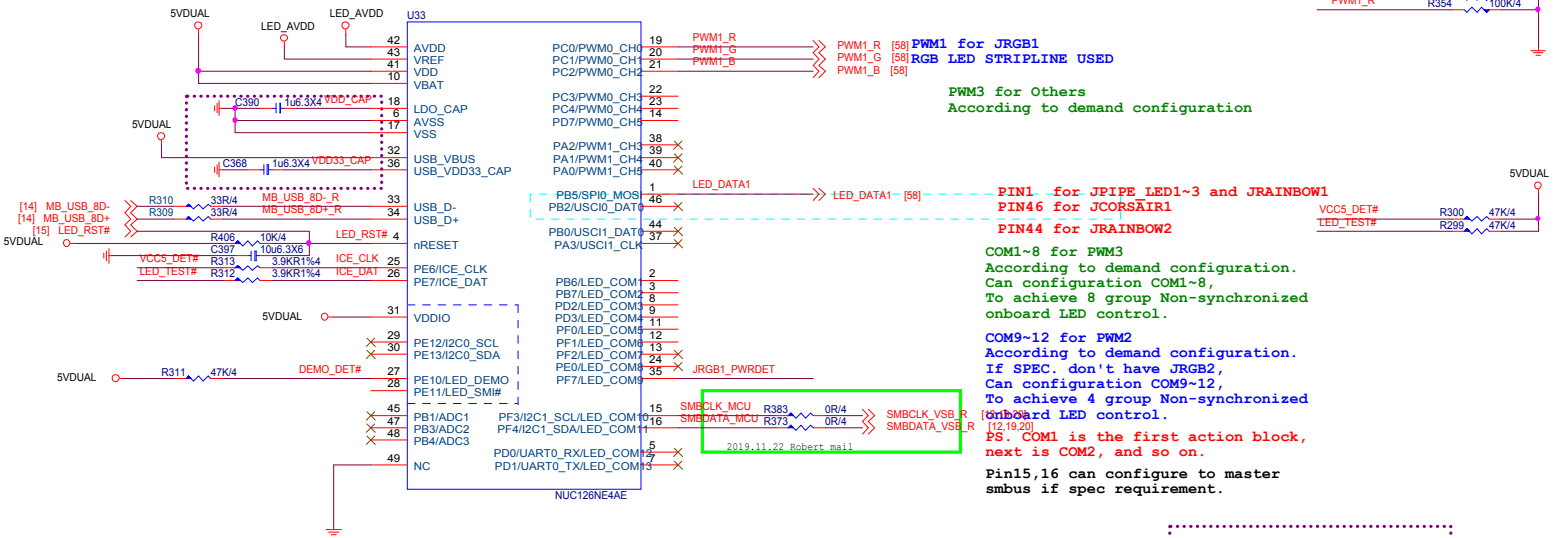
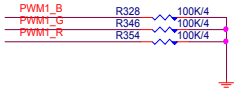
LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.



PWM1 for JRGB1
RGB LED STRIPLINE USED

PWM3 for Others
According to demand configuration



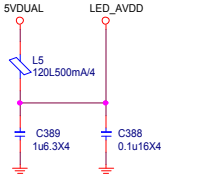
PIN1 for JPIPE_LED1~3 and JRAINBOW1
PIN46 for JCORSAIR1
PIN44 for JRAINBOW2

COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.

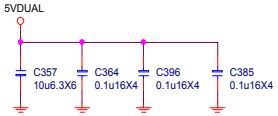
COM9~12 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~12,
To achieve 4 group Non-synchronized
onboard LED control.
PS. COM1 is the first action block,
next is COM2, and so on.

Pin15,16 can configure to master
smbus if spec requirement.

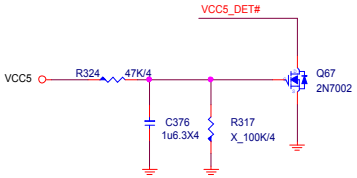
Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1
Board Side LED	COM 1~8	No Use
Board Side LED	COM 9~16	No Use

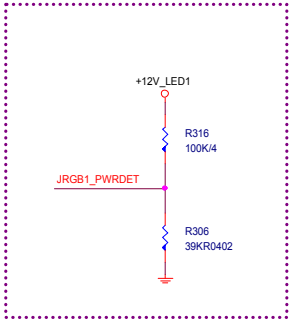


C702 & C2076 near AVDD Pin.



C2075 & C2074 near VDD Pin.
C2073 near VBAT Pin.
C2070 near VDDIO & USB VBUS Pin.

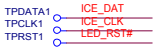




IF no JPWRLED1 & JPIPE_LED spec

MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JT1 for FW update



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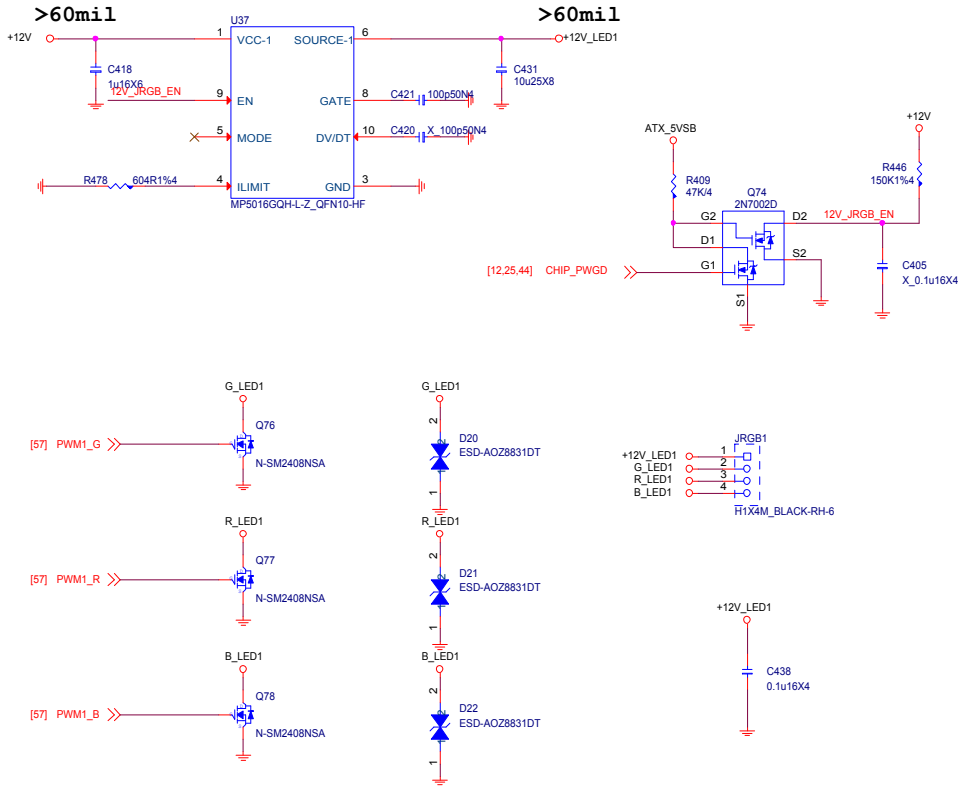
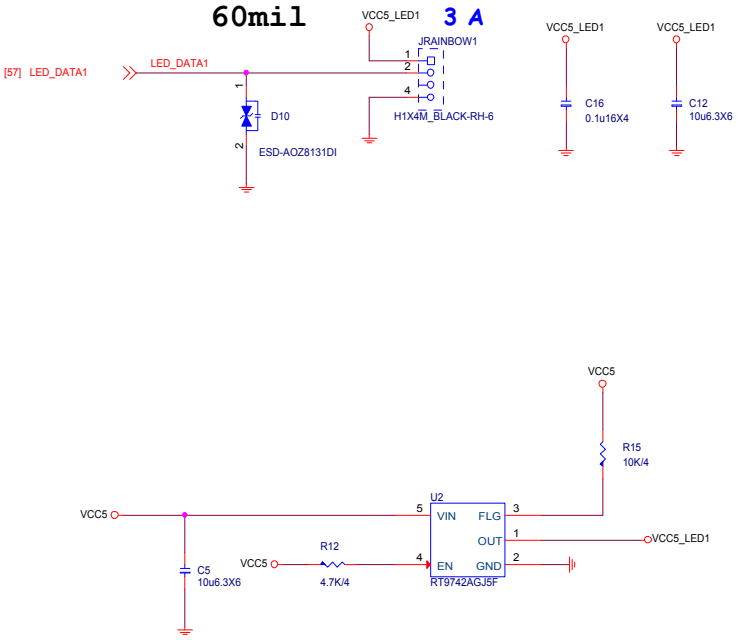
JRGB1



JRAINBOW1 LED



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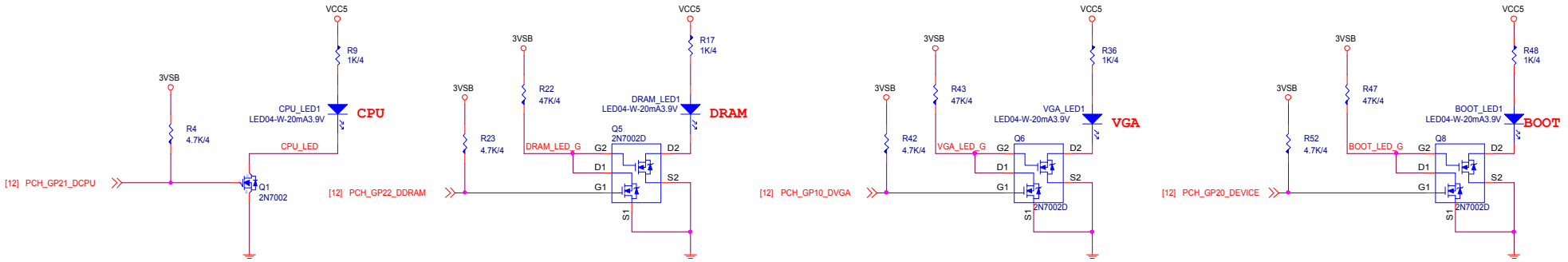
EZ Debug LED



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	MS-7C89	
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PCB1

7C89-1.2

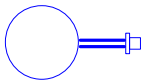
PK0-07C8912-G37
PK0-07C8912-E48

CPU_H1

CPU
鐵座

CPU_H1

BAT1_X2



BAT-CR2032

Heat Sink

HS_PCH1

PCH
Shink

MCE1
MCE2

E31-0409430-K08

BIOS_LA1

AMI

AMI

HDMI_LA1

HDMI VIRTUAL

HDMI LABEL

CFOS_LA1

CFOS VIRTUAL

CFOS LABEL

MKT_LA1

H410M-
PRO MIA

MKT

MKT_LA3

H410M-
A PRO

MKT

MKT_LA4

H410M
BOMBER

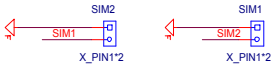
MKT

MKT_LA5

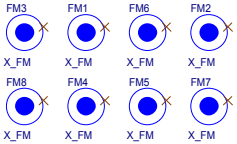
H410M
PRO-VH

MKT

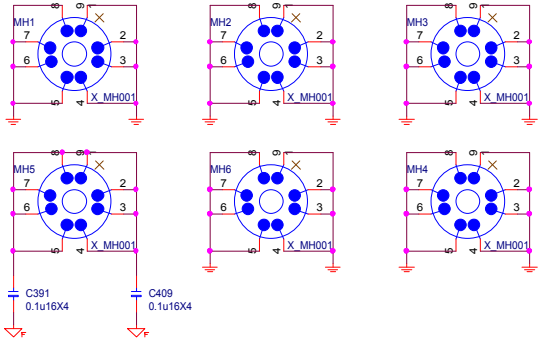
Simulation



Optical Fiducial Marks-120



Mounting Holes



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