B450 AORUS ELITE V2

Revision : 1.1

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2015.12.30--B.L

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Model Name:B450 AORUS ELITE V2

Component value change history

Version: 1.1

P-Code: U98126-0

Date	Change Item		Reason
2018.07.12	10 P-BOM Release.	PCB: 1.0	1. ECR50 for FAN_0_RPM PULL UP 2. MAR6/AR52/AR47/PR8 change to short-pad 3. KB_MS_USB 用料限制用-14R用料
2018.07.12	10B F-BOM Release.	PCB: 1.0	1. 修改ATX connect 用料,9t高溫料[11NH4-020024-Z1R_11NH4-020024-Z2R]
2018.08.20	10G D-BOM Release.	PCB:1.01	1. Vcore SENSE 位置 2. C125 10u change to 22u 3. VINA0 change to APU_PWRGD(for summit / Pinnacle 不上DIMM時,僅亮CPU DEBUD LED,應改為亮DDR DEBUG LED) 4. BRN1 change to 1K
2018.09.21	10G SKIP PVTRelease.	PCB:1.01	SKIP PVT
2019.05.21 2019.07.08	10H SKIP PVTRelease.	PCB:1.01	1. UPDATE NEW EC FW V684.BIN
2019.11.12	10H ECN	PCB:1.01	1. Location :AIO_SHIELD 11AIO-0C0013-02R 加替料11AIO-0C0013-12R
2020.06.22	10M ECN	PCB:1.05	1. Vcore choke Footprint 自動插件修改
2020.06.22	10L ECN	PCB:1.05	1. 新增替代 料 - IT8795 (10HP2-118795-10R) , 統一使用 IT8795 以利後續備料
2020.07.23	10P MP	PCB:1.05	1. SIO CX-->DX(10HP2-118686-40R) 2. BOM : 9MB45ARSE-00-10P(與10L並存)
2020.08.04	10A EVT	PCB:1.0	1. CHANGE PWM 2. SOC CHOKE CHANGR 11LC5-M5300C-01C 3. BOM : 9MB45AET2-00-10A
	10B PVT	PCB:1.01	1. DR19-->3.83K , DR46/DR47-->3.09K , DR16-->3.32K , DR44/DR45-->2.22K 2. Location: DU1 -->10TA1-63567B-07R 3. BOM : 9MB45AET2-00-10B
2020.08.04	10B ECN	PCB:1.01	1. Location:DEL1,DFL1 新增11LC5-F5300C-08R自動插件料號
2020.08.19	10C F-BOM	PCB:1.01	1. PCIE GEN3 SWITCH , REMOVE ASMEDIA用料 2.BOM : 9MB45AET2-00-10C
2020.12.01	11A E-BOM	PCB:1.1	1. Codec ALC892 change to ALC897/ACL88 colay. 2.BOM : 9MB45AET2-00-11A
2020.12.01	11A P-BOM	PCB:1.1	1. PR76 1K-->10K , PBC20 0.1U-->1U

Circuit or PCB layout change for next version

Date	Change Item	Reason
		1. Add USB 3.1 2nd re-driver. 2. Fix VDDCR_SOC_S5 power issue. 3. PWM/DRIVER change to 12V. 4. LAN, R_USB30_1 signal swap. 5. CPU side 0603 10u change to 0805 22u. 6. Add POS CAP 470U DEC3. 7. Debug port turn to left. 8. KB/MS EMI CAP change to 0402. 9. Update PWM choke (P/N not done). 10. Update PWM OV (current dac)

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Title	BOM & PCB HISTORY	
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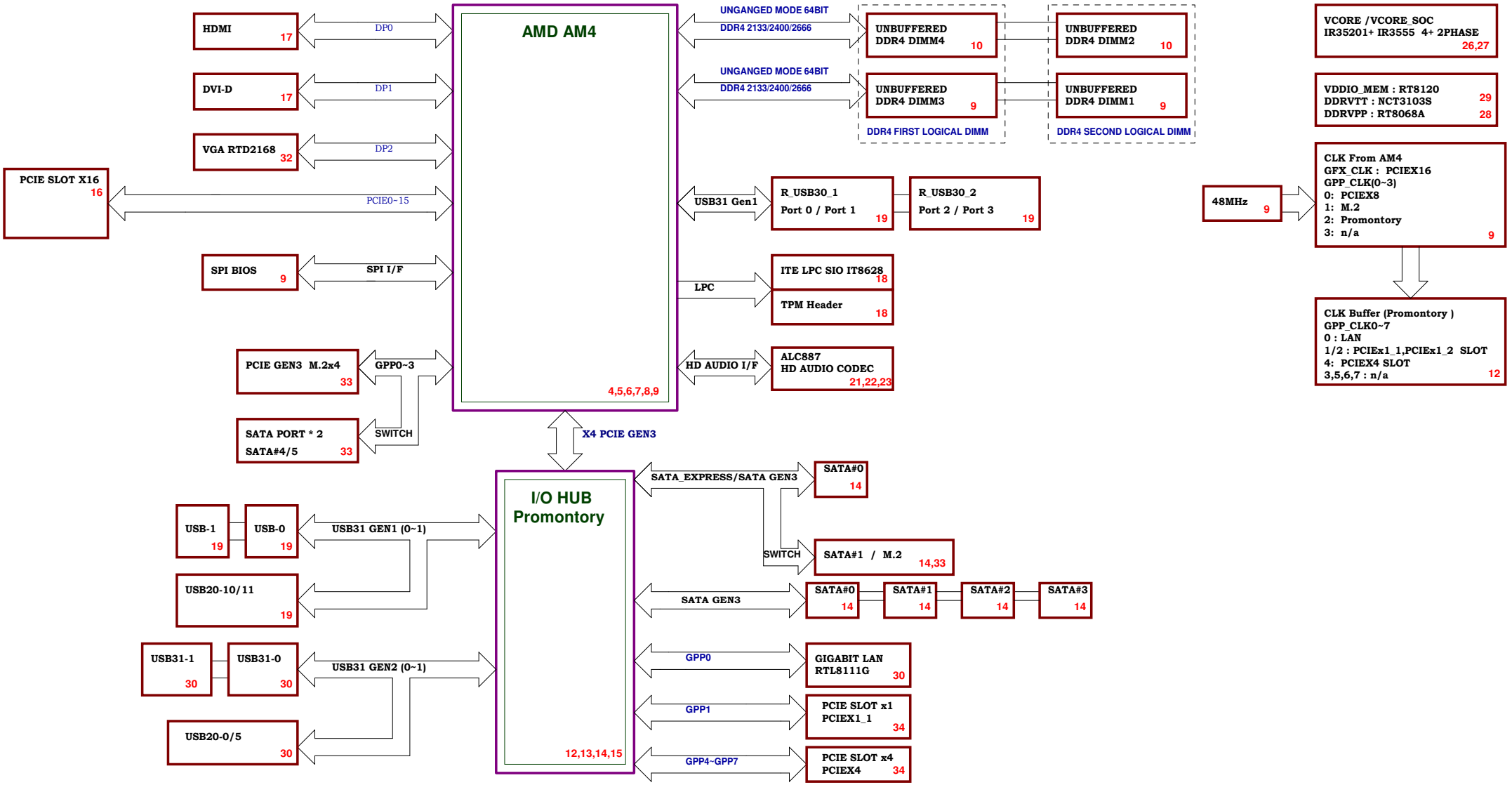
Date: Wednesday, January 20, 2021	Sheet 2 of 39	



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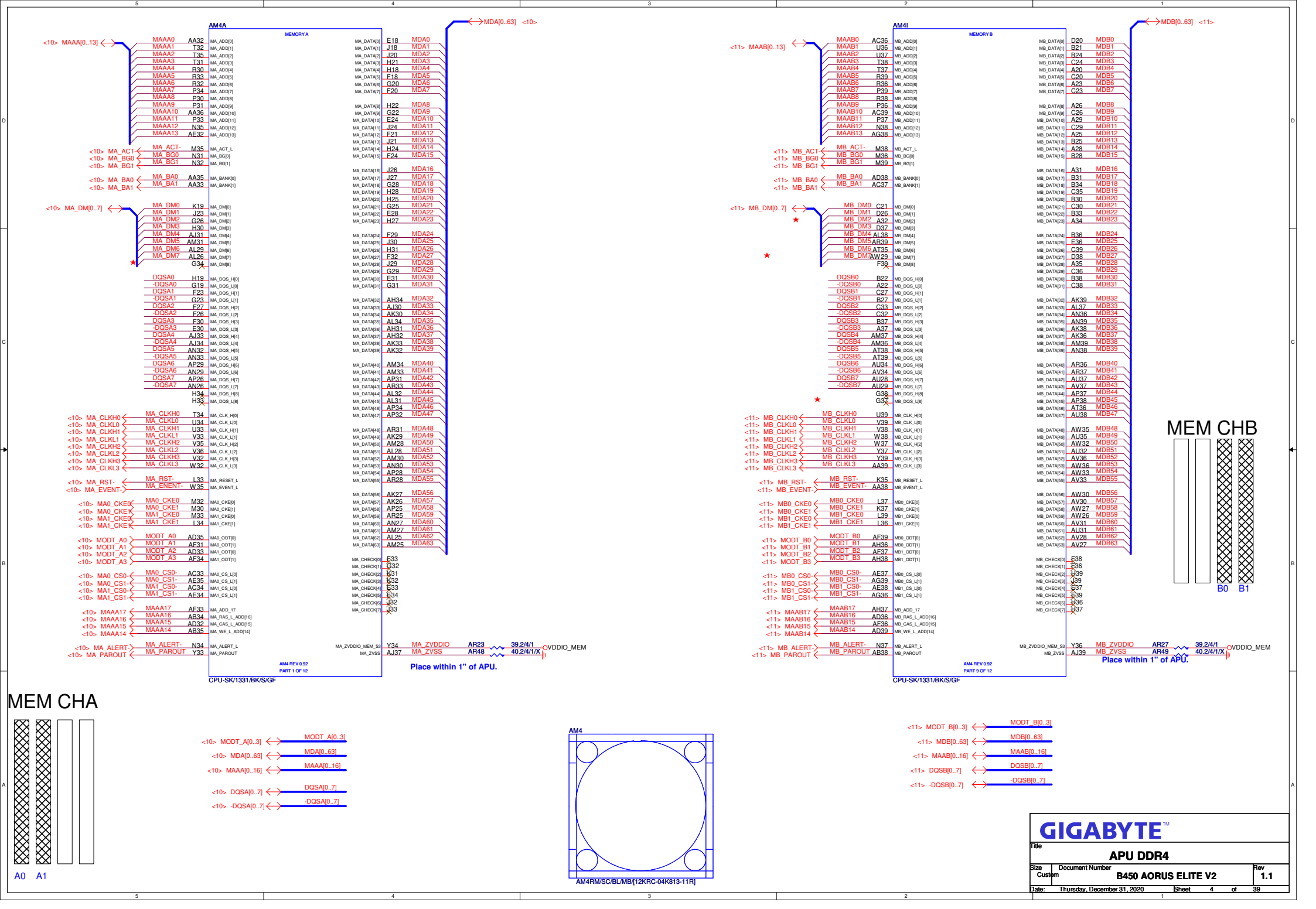
Title	BLOCK DIAGRAM	
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
Date: Thursday, December 31, 2020	Sheet 3 of 39	


AM4A
MEMORY A
CPU-SK/1331/BK/S/GF
AM4 REV 0.92
PART 1 OF 12
AM4I
MEMORY B
CPU-SK/1331/BK/S/GF
AM4 REV 0.92
PART 9 OF 12
MEM CHA
A0
A1
MEM CHB
B0
B1
Place within 1" of APU.
Place within 1" of APU.
AM4
AM4RM/SC/BL/MB/[12KRC-04K813-11R]
GIGABYTE
APU DDR4
B450 AORUS ELITE V2
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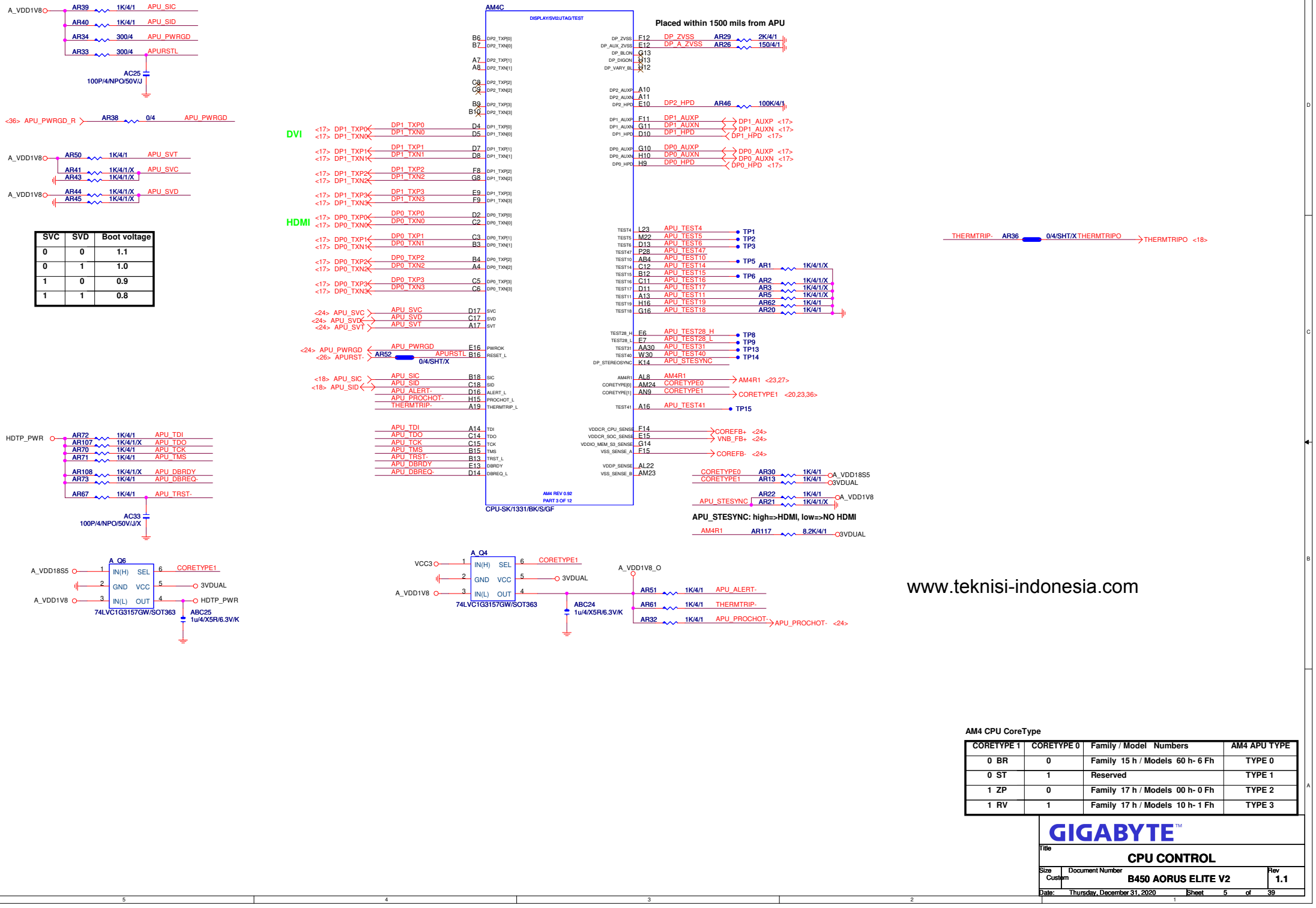
39



AM4 CPU CoreType

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh	TYPE 3

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Title	CPU CONTROL	
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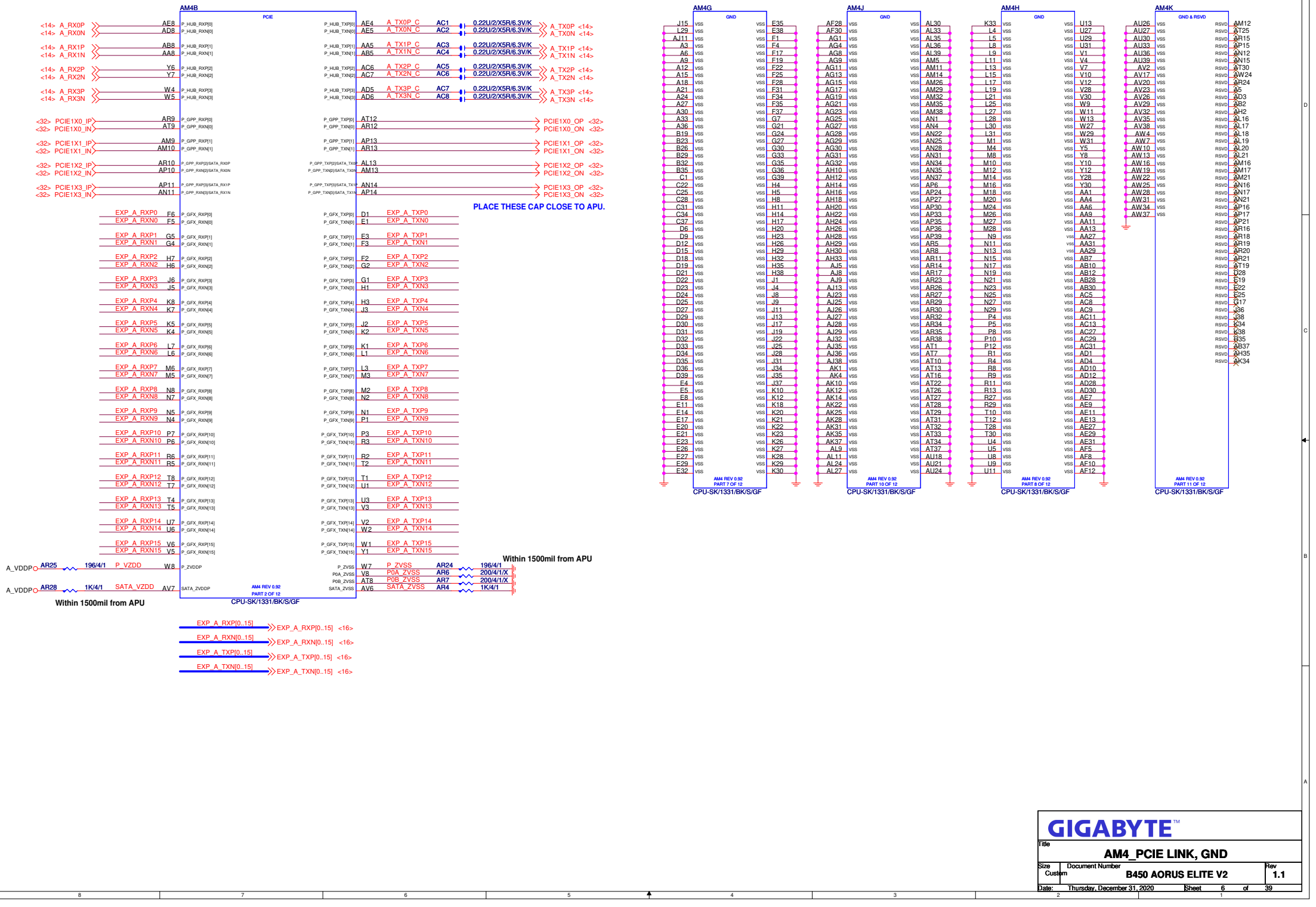

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Title	AM4_PCIE LINK, GND		
Size: Custom	Document Number: B450 AORUS ELITE V2		Rev: 1.1
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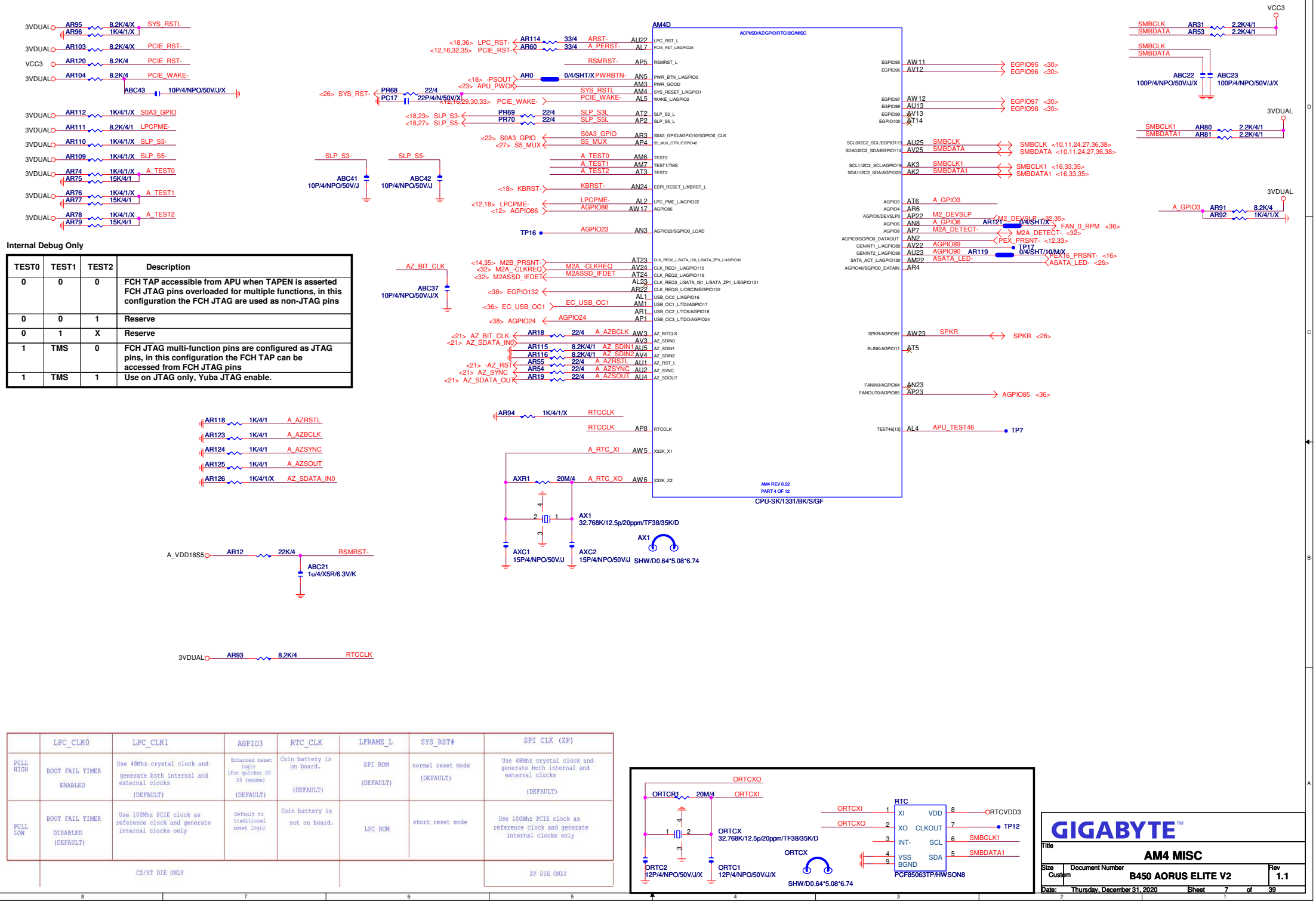
AM4D
ACPI/SD/AZ/GPIO/RTC/I2C/MISC
CPU-SK/1331/BK/S/GF
AM4 REV 0.92
PART 4 OF 12
AM4 MISC
B450 AORUS ELITE V2
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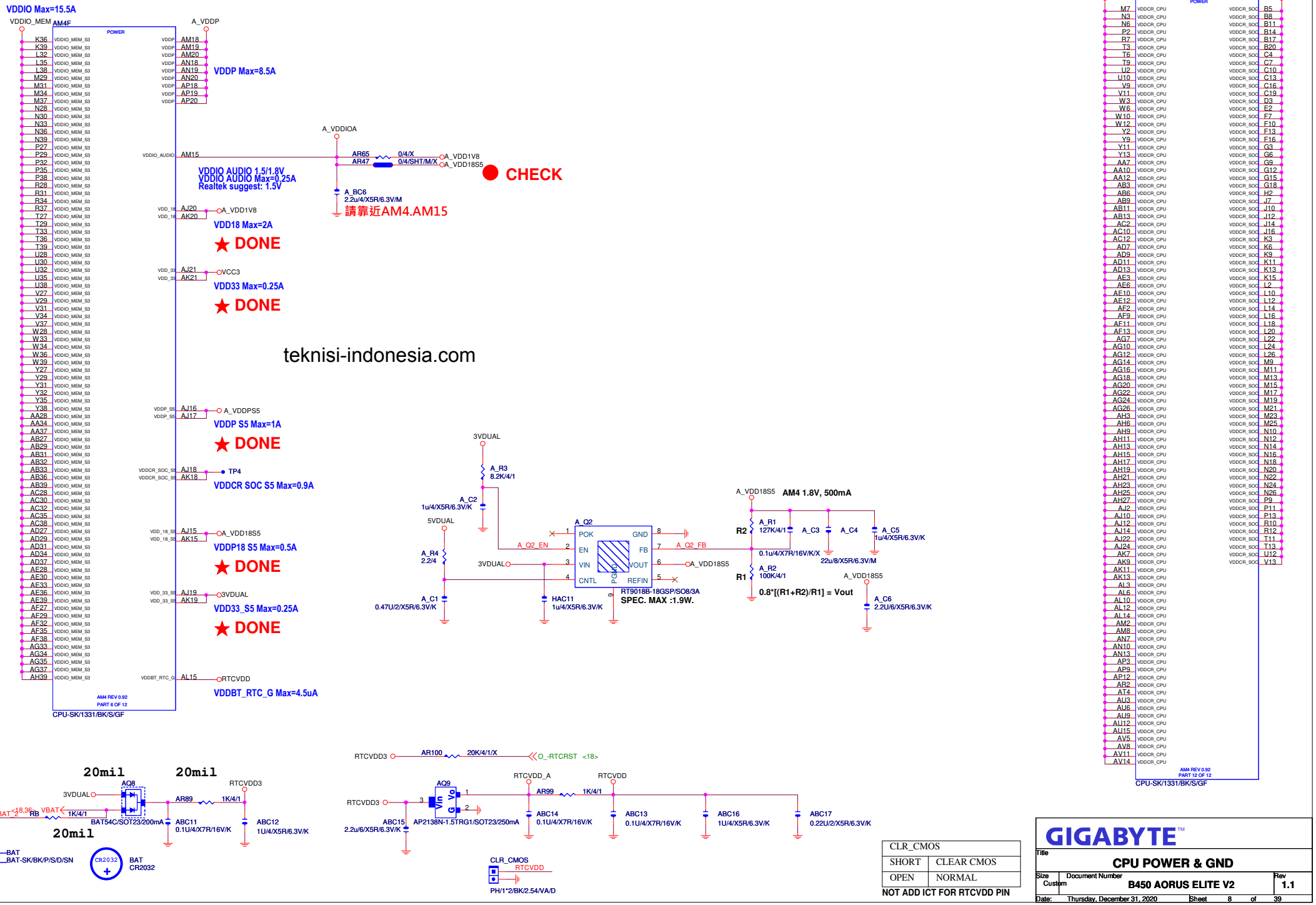
Internal Debug Only
TEST0 TEST1 TEST2 Description
0 0 0 FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0 0 1 Reserve
0 1 X Reserve
1 TMS 0 FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1 TMS 1 Use on JTAG only, Yuba JTAG enable.
LPC_CLK0 LPC_CLK1 AGPIO3 RTC_CLK LFRAME_L SYS_RST# SPI CLK (ZP)
PULL HIGH
BOOT FAIL TIMER ENABLED
Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)
Coin battery is on board. (DEFAULT)
SPI ROM (DEFAULT)
normal reset mode (DEFAULT)
Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW
BOOT FAIL TIMER DISABLED (DEFAULT)
Use 100Mhz PCIE clock as reference clock and generate internal clocks only
Default to traditional reset logic
Coin battery is not on board.
LPC ROM
short reset mode
Use 100Mhz PCIE clock as reference clock and generate internal clocks only
CZ/ST DIE ONLY
ZP DIE ONLY
RTC
PCF85063TP/HWSON8
SHW/D0.64*5.08*6.74
SHW/D0.64*5.08*6.74


VDDIO Max=15.5A
VDDIO_MEM
AM4F
POWER
A_VDDP
VDDP Max=8.5A
A_VDDIOA
VDDIO_AUDIO
AM15
AR65
AR47
0/4/X
0/4/SHT/M/X
A_VDD1V8
A_VDD18S5
CHECK
A_BC6
2.2u/4/X5R/6.3V/M
請靠近AM4.AM15
VDDIO AUDIO 1.5/1.8V
VDDIO AUDIO Max=0.25A
Realtek suggest: 1.5V
AJ20
AK20
A_VDD1V8
VDD18 Max=2A
DONE
AJ21
AK21
VCC3
VDD33 Max=0.25A
DONE
teknisi-indonesia.com
AJ16
AJ17
A_VDDPS5
VDDP S5 Max=1A
DONE
AJ18
AK18
TP4
VDDCR SOC S5 Max=0.9A
AJ15
AK15
A_VDD18S5
VDDP18 S5 Max=0.5A
DONE
AJ19
AK19
3VDUAL
VDD33_S5 Max=0.25A
DONE
AL15
RTCVDD
VDDBT_RTC_G Max=4.5uA
AM4 REV 0.92
PART 6 OF 12
CPU-SK/1331/BK/S/GF
3VDUAL
A_R3
8.2K/4/1
A_C2
1u/4/X5R/6.3V/K
5VDUAL
A_R4
2.2/4
A_C1
0.47U/2/X5R/6.3V/K
A_Q2
POK
EN
VIN
CNTL
GND
FB
VOUT
REFIN
PGND
A_Q2_EN
A_Q2_FB
A_VDD18S5
HAC11
1u/4/X5R/6.3V/K
RT9018B-18GSP/SO8/3A
SPEC. MAX :1.9W.
A_VDD18S5
AM4 1.8V, 500mA
R2
A_R1
127K/4/1
A_C3
0.1u/4/X7R/16V/K/X
A_C4
22u/8/X5R/6.3V/M
A_C5
1u/4/X5R/6.3V/K
R1
A_R2
100K/4/1
0.8*[(R1+R2)/R1] = Vout
A_VDD18S5
A_C6
2.2U/6/X5R/6.3V/K
Vcore EDC =125A
Vcore 0.75~1.5V
Vcore SOC EDC=75A
Vcore SOC 0.75~1.2V
VCORE
AM4L
POWER
VCORE_SOC
AM4 REV 0.92
PART 12 OF 12
CPU-SK/1331/BK/S/GF
20mil
20mil
20mil
3VDUAL
AQ8
BAT54C/SOT23/200mA
AR89
1K/4/1
RTCVDD3
VBAT
RB
1K/4/1
ABC11
0.1U/4/X7R/16V/K
ABC12
1U/4/X5R/6.3V/K
BAT
BAT-SK/BK/P/S/D/SN
CR2032
BAT
CR2032
RTCVDD3
AR100
20K/4/1/X
O_-RTCRST <18>
RTCVDD_A
RTCVDD
AQ9
AP2138N-1.5TRG1/SOT23/250mA
AR99
1K/4/1
ABC15
2.2u/6/X5R/6.3V/K
ABC14
0.1U/4/X7R/16V/K
ABC13
0.1U/4/X7R/16V/K
ABC16
1U/4/X5R/6.3V/K
ABC17
0.22U/2/X5R/6.3V/K
CLR_CMOS
RTCVDD
PH/1*2/BK/2.54/VA/D
CLR_CMOS
SHORT
CLEAR CMOS
OPEN
NORMAL
NOT ADD ICT FOR RTCVDD PIN
GIGABYTE
Title
CPU POWER & GND
Size
Custom
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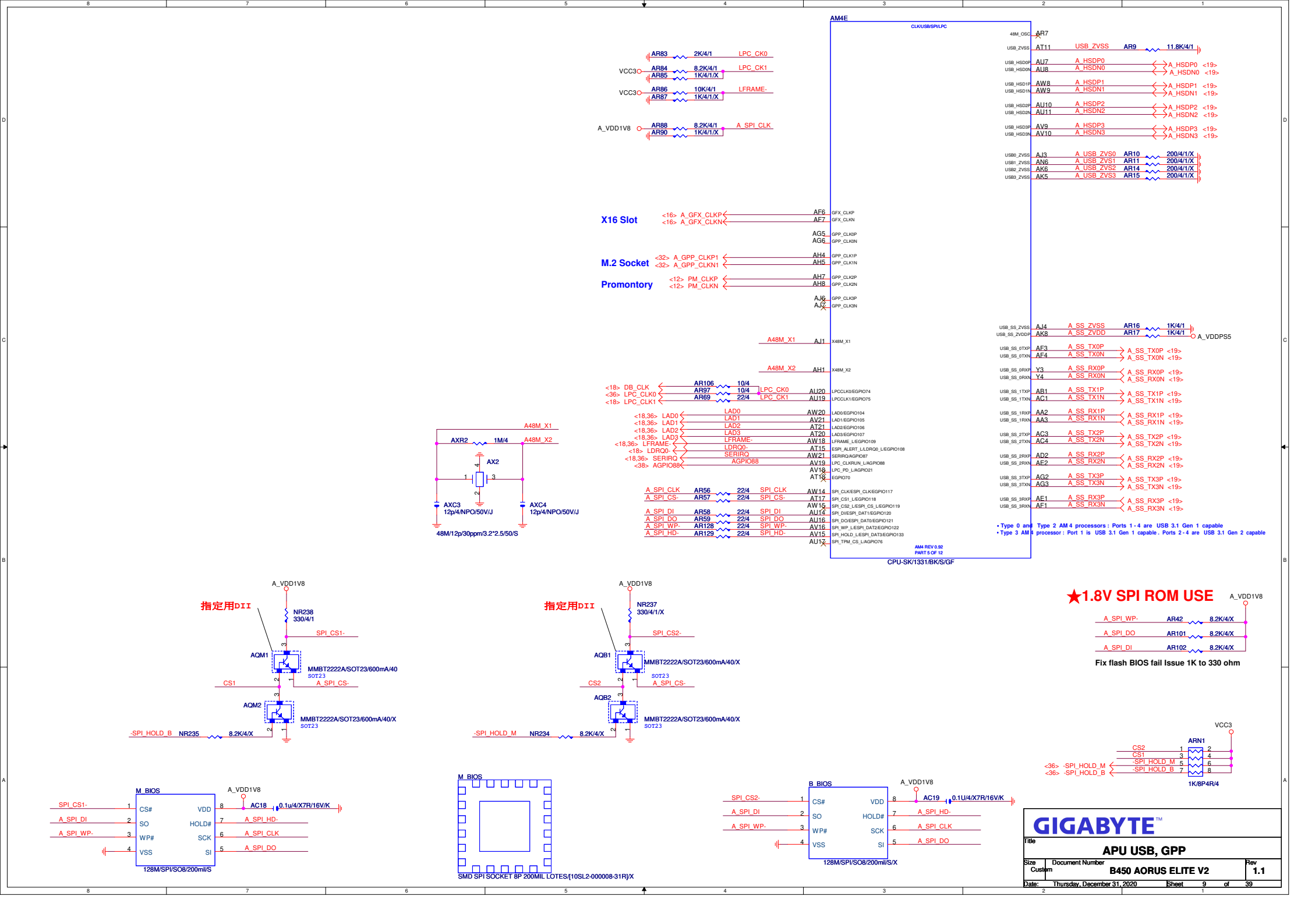
AM4E
CLK/USB/SPI/LPC
X16 Slot
M.2 Socket
Promontory
CPU-SK/1331/BK/S/GF
AM4 REV 0.92
PART 5 OF 12
• Type 0 and Type 2 AM4 processors : Ports 1 - 4 are USB 3.1 Gen 1 capable
• Type 3 AM4 processor : Port 1 is USB 3.1 Gen 1 capable. Ports 2 - 4 are USB 3.1 Gen 2 capable
48M/12p/30ppm/3.2*2.5/50/S
★1.8V SPI ROM USE
Fix flash BIOS fail Issue 1K to 330 ohm
指定用DII
NR238 330/4/1
NR237 330/4/1/X
AQM1
AQM2
AQB1
AQB2
MMBT2222A/SOT23/600mA/40/X
M_BIOS
B_BIOS
128M/SPI/SO8/200mil/S
128M/SPI/SO8/200mil/S/X
SMD SPI SOCKET 8P 200MIL LOTES/[10SL2-000008-31R]/X
1K/8P4R/4
GIGABYTE
APU USB, GPP
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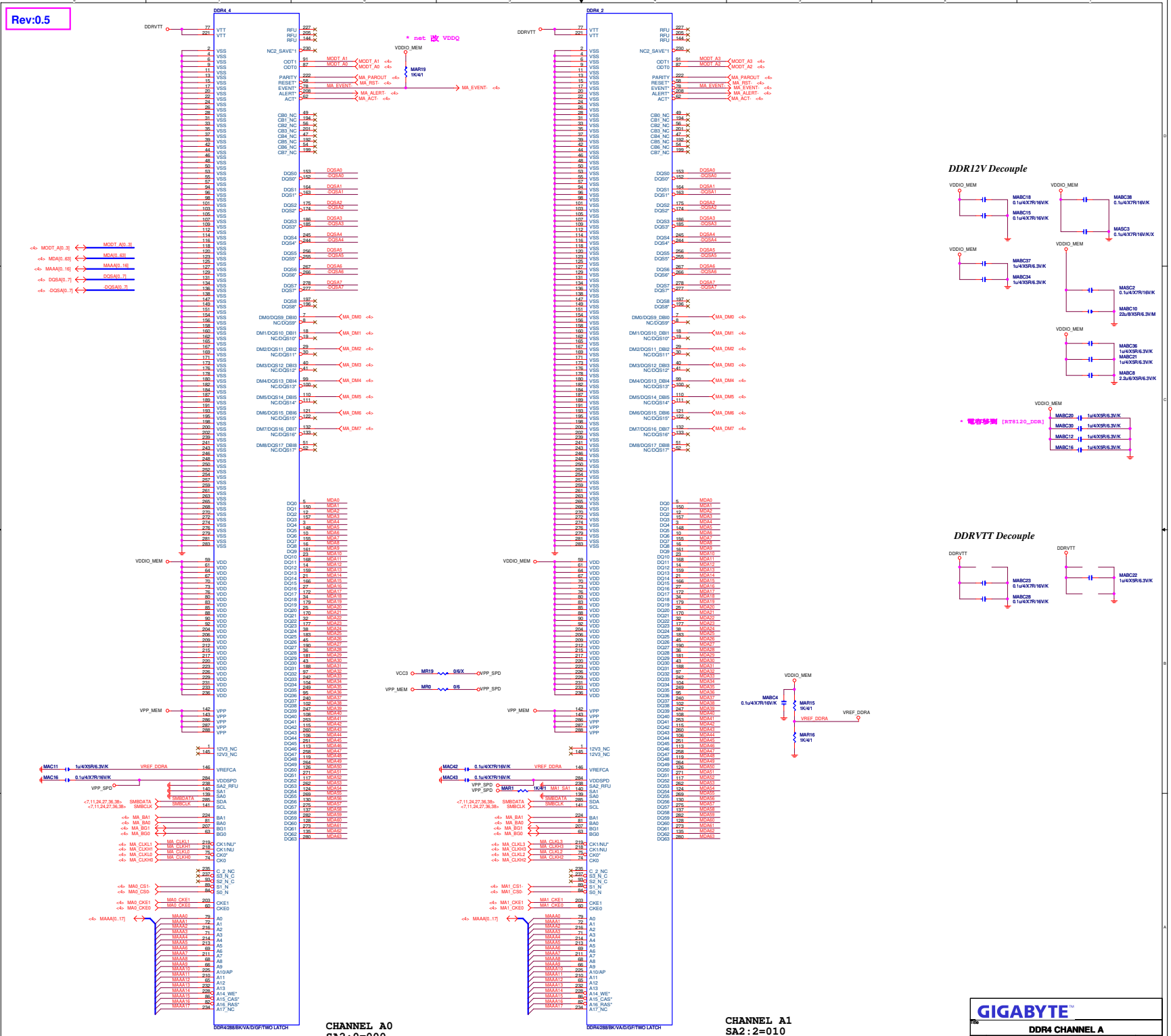

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Title	DDR4 CHANNEL A		
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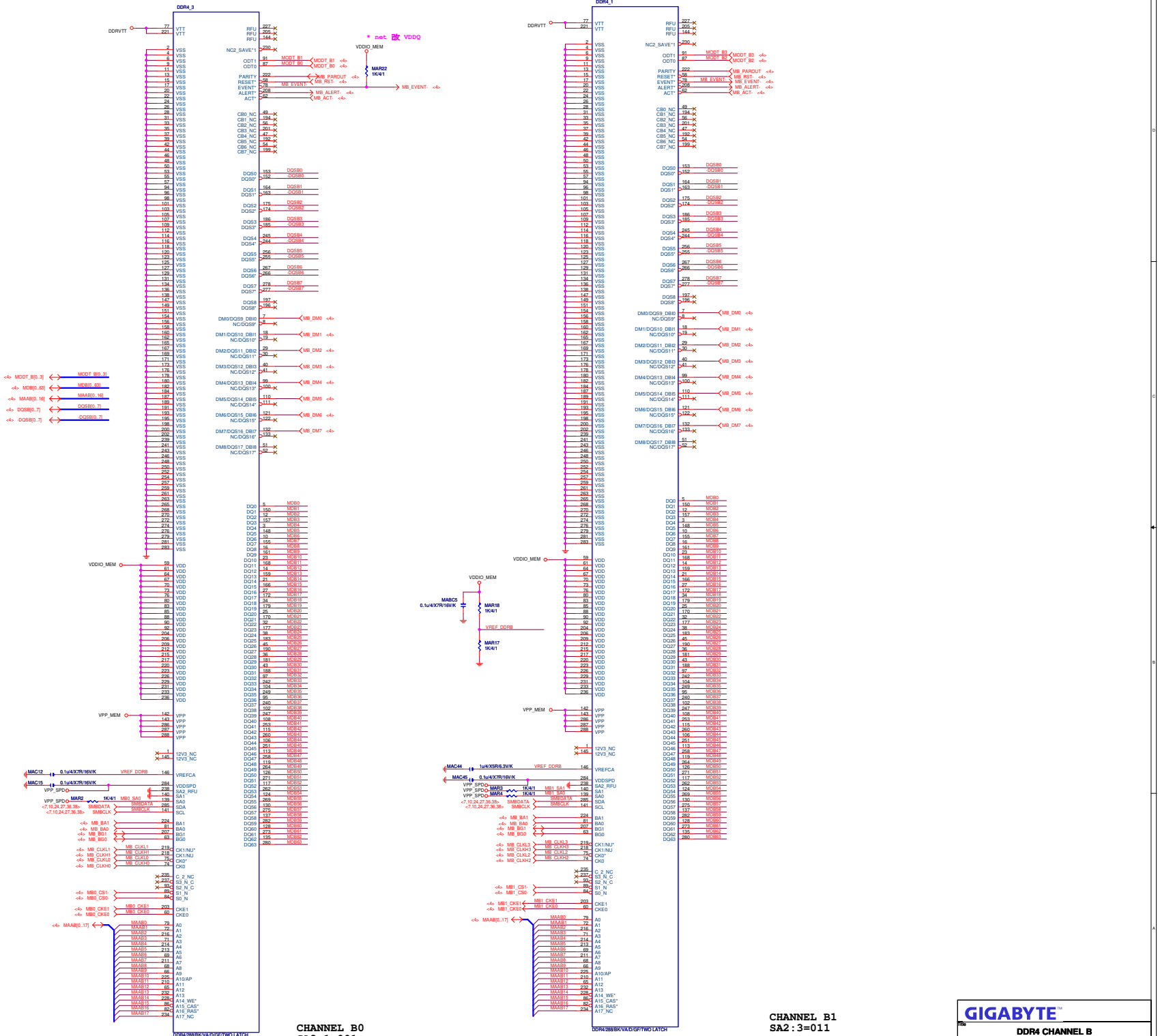

CHANNEL B0
SA2:1=001

CHANNEL B1
SA2:3=011

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Title: DDR4 CHANNEL B			
Size: Custom	Document Number: B450 AORUS ELITE V2		Rev: 1.1
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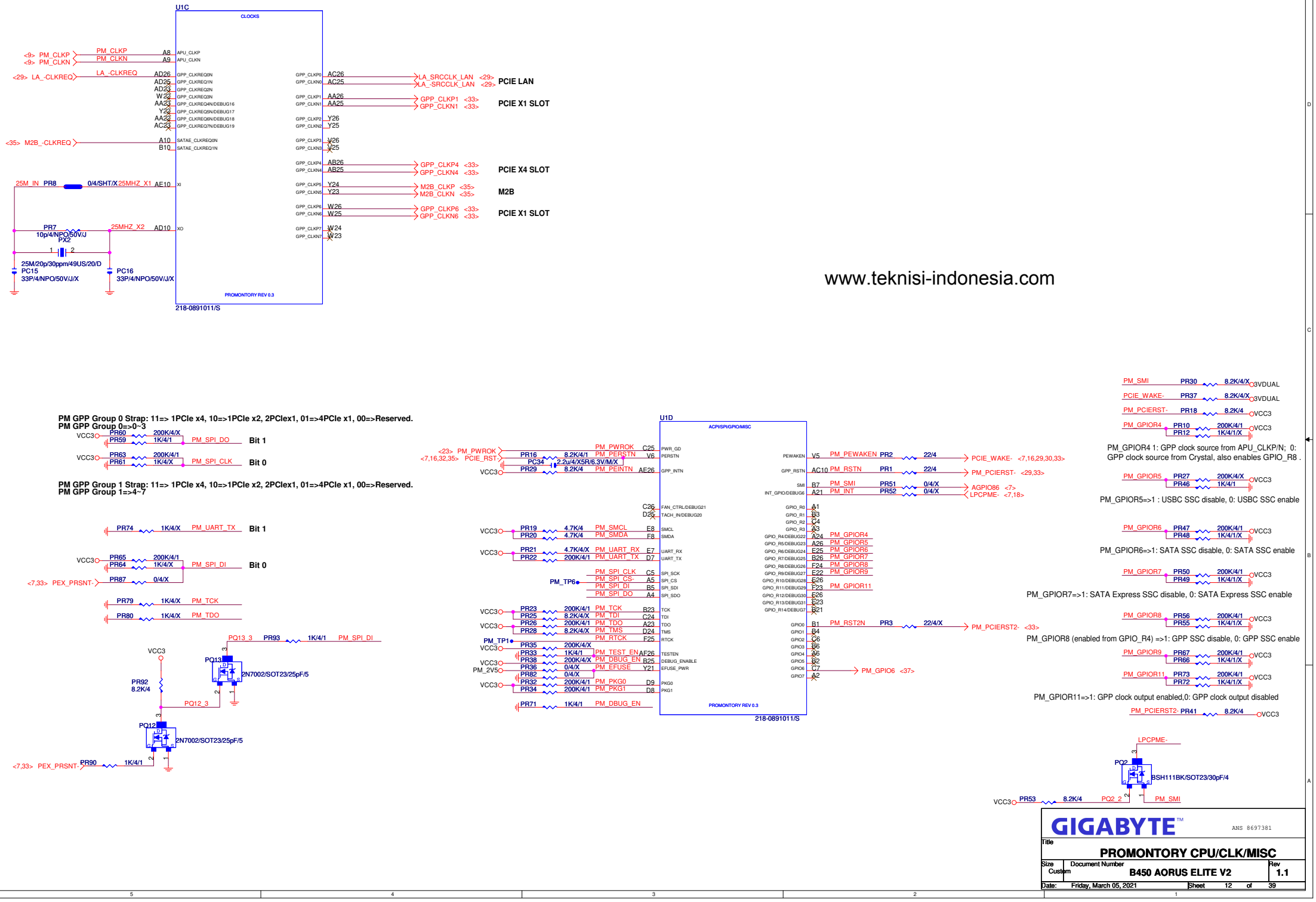
U1C
CLOCKS
PROMONTORY REV 0.3
218-0891011/S
PM_CLKP
PM_CLKN
LA_-CLKREQ
M2B_-CLKREQ
25M_IN
PR8
0/4/SHT/X
25MHZ_X1
25MHZ_X2
PR7
10p/4/NPO/50V/J
PX2
25M/20p/30ppm/49US/20/D
PC15
33P/4/NPO/50V/J/X
PC16
33P/4/NPO/50V/J/X
PCIE LAN
PCIE X1 SLOT
PCIE X4 SLOT
M2B
PCIE X1 SLOT
www.teknisi-indonesia.com
PM GPP Group 0 Strap: 11=> 1PCIe x4, 10=>1PCIe x2, 2PClex1, 01=>4PCIe x1, 00=>Reserved.
PM GPP Group 0=>0~3
Bit 1
Bit 0
PM GPP Group 1 Strap: 11=> 1PCIe x4, 10=>1PCIe x2, 2PClex1, 01=>4PCIe x1, 00=>Reserved.
PM GPP Group 1=>4~7
Bit 1
Bit 0
2N7002/SOT23/25pF/5
2N7002/SOT23/25pF/5
U1D
ACPI/SPI/GPIO/MISC
PROMONTORY REV 0.3
218-0891011/S
PM_GPIOR4 1: GPP clock source from APU_CLKP/N; 0: GPP clock source from Crystal, also enables GPIO_R8 .
PM_GPIOR5=>1 : USBC SSC disable, 0: USBC SSC enable
PM_GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable
PM_GPIOR7=>1: SATA Express SSC disable, 0: SATA Express SSC enable
PM_GPIOR8 (enabled from GPIO_R4) =>1: GPP SSC disable, 0: GPP SSC enable
PM_GPIOR11=>1: GPP clock output enabled,0: GPP clock output disabled
BSH111BK/SOT23/30pF/4
GIGABYTE
ANS 8697381
PROMONTORY CPU/CLK/MISC
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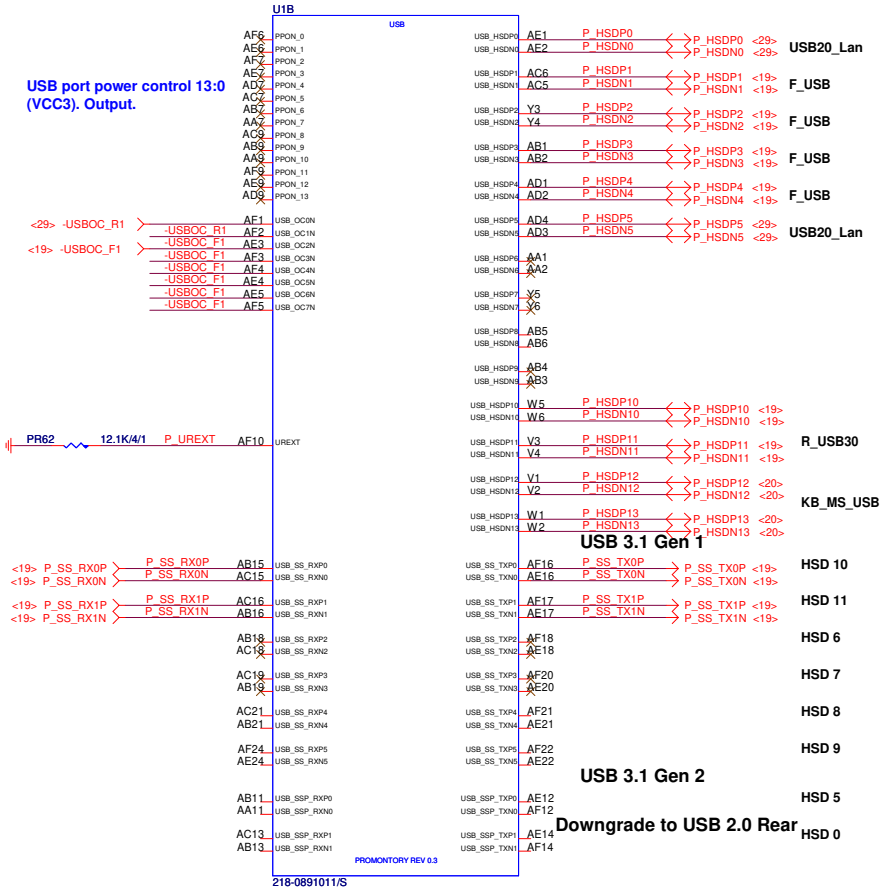

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

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Title: PM USB

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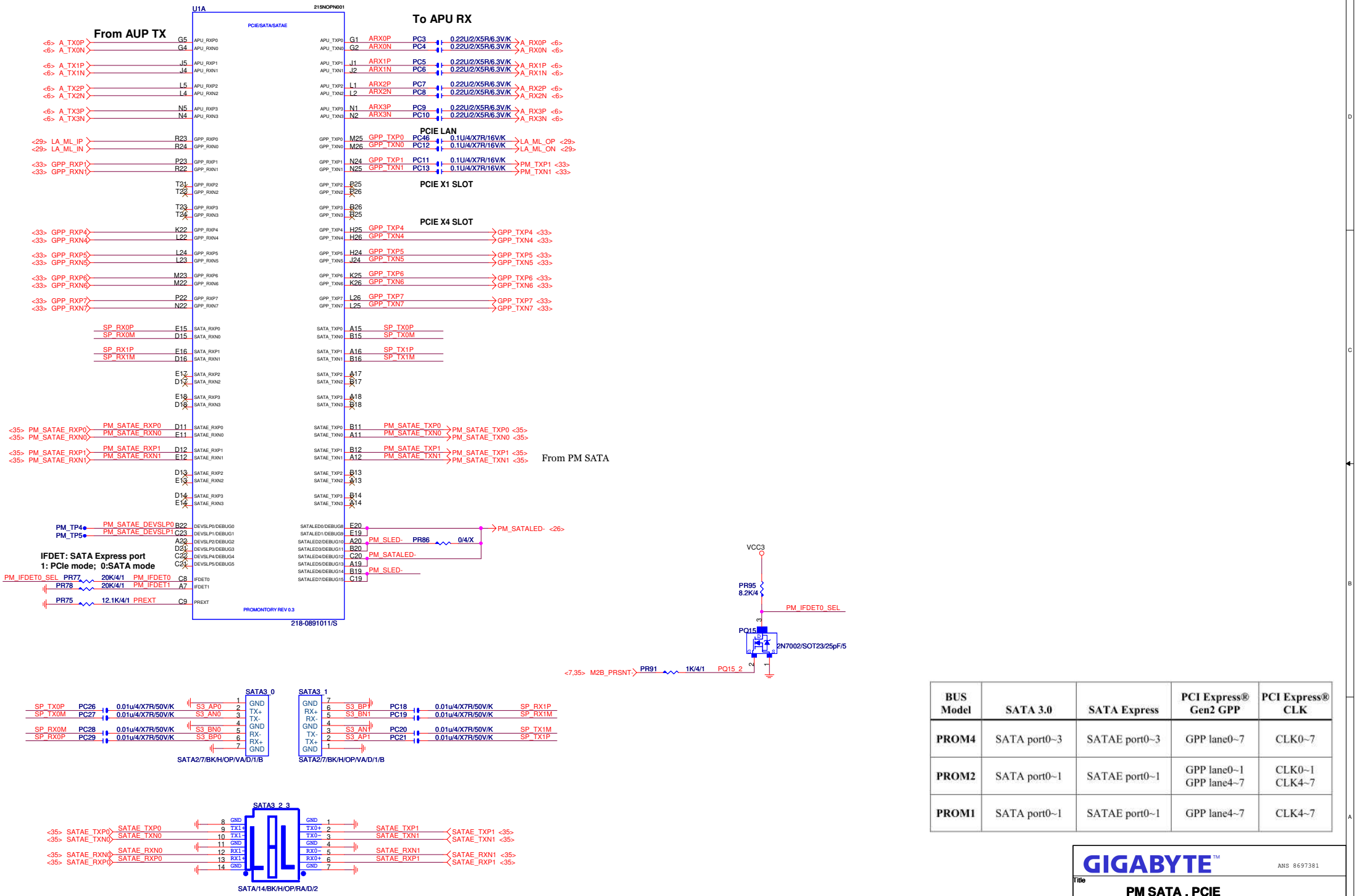

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

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Title: PM SATA , PCIE

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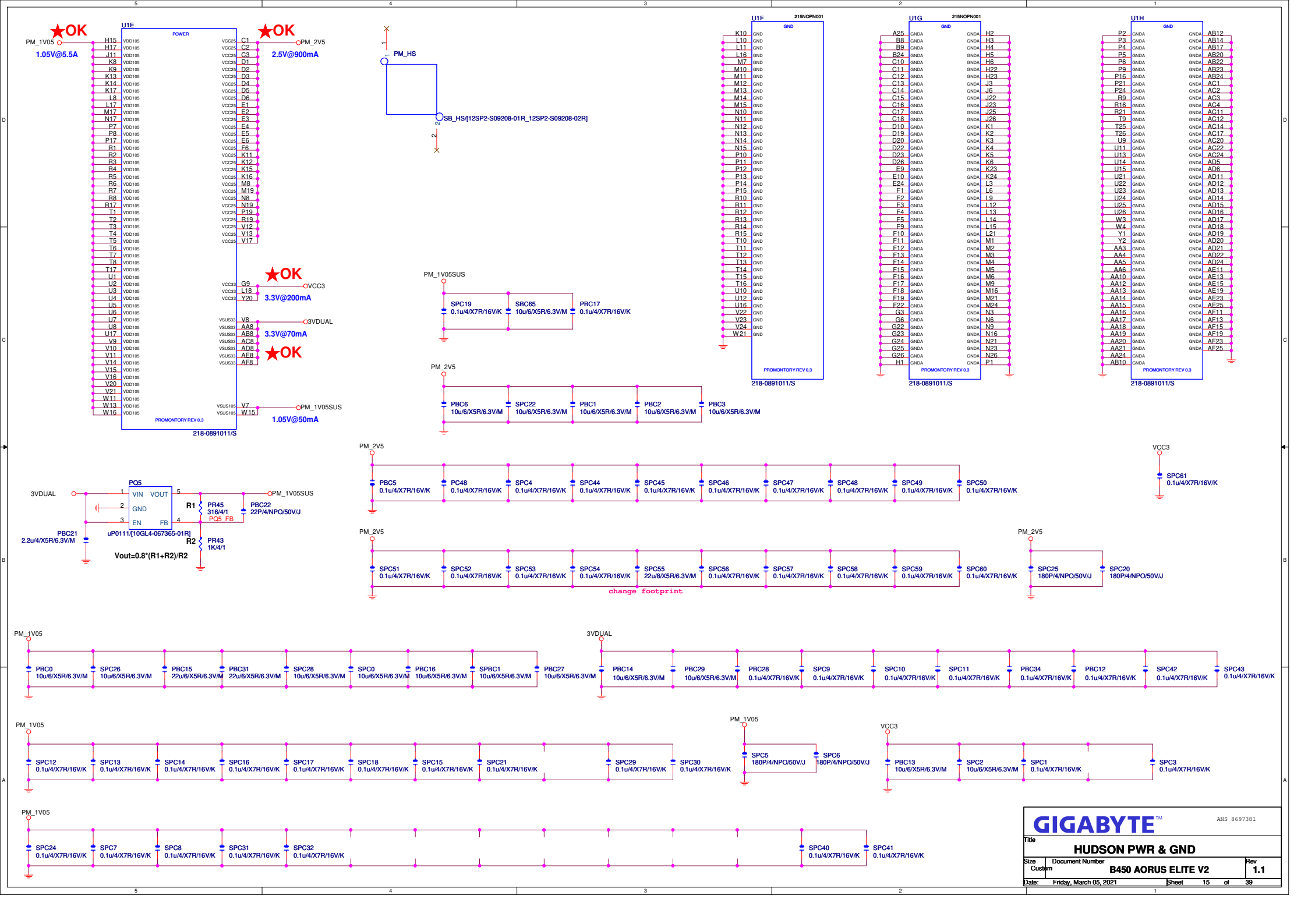
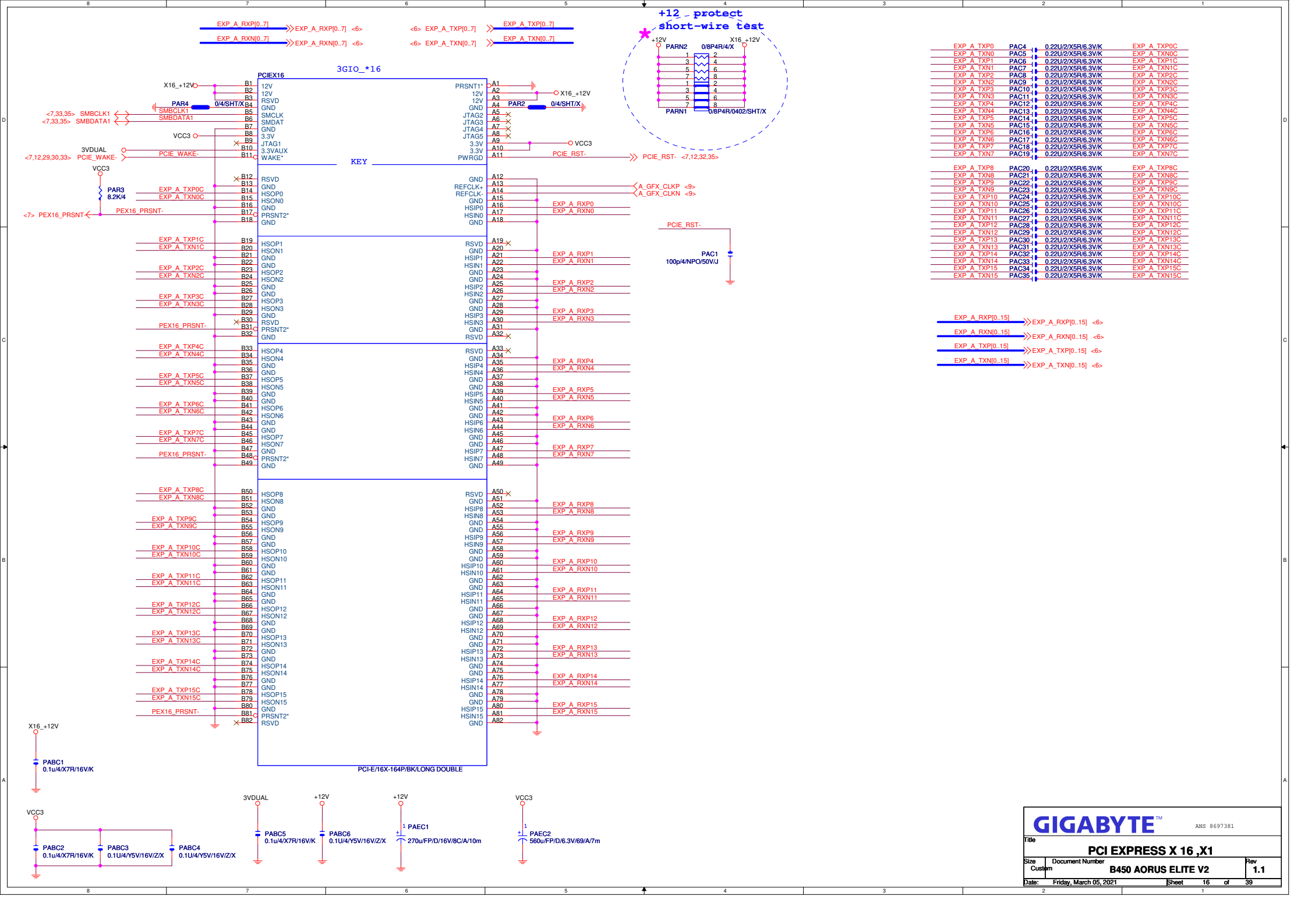

U1E
POWER
PM_1V05
1.05V@5.5A
OK
PM_2V5
2.5V@900mA
VCC3
3.3V@200mA
3VDUAL
3.3V@70mA
PM_1V05SUS
1.05V@50mA
PROMONTORY REV 0.3
218-0891011/S
PM_HS
SB_HS/[12SP2-S09208-01R_12SP2-S09208-02R]
U1F
U1G
U1H
215NOPN001
GND
SPC19 0.1u/4/X7R/16V/K
SBC65 10u/6/X5R/6.3V/M
PBC17 0.1u/4/X7R/16V/K
PBC6 10u/6/X5R/6.3V/M
SPC22 10u/6/X5R/6.3V/M
PBC1 10u/6/X5R/6.3V/M
PBC2 10u/6/X5R/6.3V/M
PBC3 10u/6/X5R/6.3V/M
PQ5
3VDUAL
VIN
VOUT
GND
EN
FB
R1
PR45 316/4/1
PQ5_FB
R2
PR43 1K/4/1
PBC21 2.2u/4/X5R/6.3V/M
PBC22 22P/4/NPO/50V/J
uP0111/[10GL4-067365-01R]
Vout=0.8*(R1+R2)/R2
PBC5 0.1u/4/X7R/16V/K
PC48 0.1u/4/X7R/16V/K
SPC4 0.1u/4/X7R/16V/K
SPC44 0.1u/4/X7R/16V/K
SPC45 0.1u/4/X7R/16V/K
SPC46 0.1u/4/X7R/16V/K
SPC47 0.1u/4/X7R/16V/K
SPC48 0.1u/4/X7R/16V/K
SPC49 0.1u/4/X7R/16V/K
SPC50 0.1u/4/X7R/16V/K
SPC61 0.1u/4/X7R/16V/K
SPC51 0.1u/4/X7R/16V/K
SPC52 0.1u/4/X7R/16V/K
SPC53 0.1u/4/X7R/16V/K
SPC54 0.1u/4/X7R/16V/K
SPC55 22u/8/X5R/6.3V/M
SPC56 0.1u/4/X7R/16V/K
SPC57 0.1u/4/X7R/16V/K
SPC58 0.1u/4/X7R/16V/K
SPC59 0.1u/4/X7R/16V/K
SPC60 0.1u/4/X7R/16V/K
change footprint
SPC25 180P/4/NPO/50V/J
SPC20 180P/4/NPO/50V/J
PBC0 10u/6/X5R/6.3V/M
SPC26 10u/6/X5R/6.3V/M
PBC15 22u/6/X5R/6.3V/M
PBC31 22u/6/X5R/6.3V/M
SPC28 10u/6/X5R/6.3V/M
SPC0 10u/6/X5R/6.3V/M
PBC16 10u/6/X5R/6.3V/M
SPBC1 10u/6/X5R/6.3V/M
PBC27 10u/6/X5R/6.3V/M
PBC14 10u/6/X5R/6.3V/M
PBC29 10u/6/X5R/6.3V/M
PBC28 0.1u/4/X7R/16V/K
SPC9 0.1u/4/X7R/16V/K
SPC10 0.1u/4/X7R/16V/K
SPC11 0.1u/4/X7R/16V/K
PBC34 0.1u/4/X7R/16V/K
PBC12 0.1u/4/X7R/16V/K
SPC42 0.1u/4/X7R/16V/K
SPC43 0.1u/4/X7R/16V/K
SPC12 0.1u/4/X7R/16V/K
SPC13 0.1u/4/X7R/16V/K
SPC14 0.1u/4/X7R/16V/K
SPC16 0.1u/4/X7R/16V/K
SPC17 0.1u/4/X7R/16V/K
SPC18 0.1u/4/X7R/16V/K
SPC15 0.1u/4/X7R/16V/K
SPC21 0.1u/4/X7R/16V/K
SPC29 0.1u/4/X7R/16V/K
SPC30 0.1u/4/X7R/16V/K
SPC5 180P/4/NPO/50V/J
SPC6 180P/4/NPO/50V/J
PBC13 10u/6/X5R/6.3V/M
SPC2 10u/6/X5R/6.3V/M
SPC1 0.1u/4/X7R/16V/K
SPC3 0.1u/4/X7R/16V/K
SPC24 0.1u/4/X7R/16V/K
SPC7 0.1u/4/X7R/16V/K
SPC8 0.1u/4/X7R/16V/K
SPC31 0.1u/4/X7R/16V/K
SPC32 0.1u/4/X7R/16V/K
SPC40 0.1u/4/X7R/16V/K
SPC41 0.1u/4/X7R/16V/K
GIGABYTE
ANS 8697381
Title
HUDSON PWR & GND
Size
Custom
Document Number
B450 AORUS ELITE V2
Rev
1.1
Date: Friday, March 05, 2021
Sheet 15 of 39


EXP_A_RXP[0..7]
EXP_A_RXN[0..7]
EXP_A_TXP[0..7]
EXP_A_TXN[0..7]
+12 protect
short-wire test
3GIO_*16
PCIEX16
KEY
PCI-E/16X-164P/BK/LONG DOUBLE
PAR4
PAR2
PAR3
8.2K/4
PAR1
PAR2
0/8P4R/4/X
0/8P4R/0402/SHT/X
PAC1
100p/4/NPO/50V/J
PABC1
0.1u/4/X7R/16V/K
PABC2
0.1u/4/X7R/16V/K
PABC3
0.1U/4/Y5V/16V/Z/X
PABC4
0.1U/4/Y5V/16V/Z/X
PABC5
0.1u/4/X7R/16V/K
PABC6
0.1U/4/Y5V/16V/Z/X
PAEC1
270u/FP/D/16V/8C/A/10m
PAEC2
560u/FP/D/6.3V/69/A/7m
PAC4 PAC5 PAC6 PAC7 PAC8 PAC9 PAC10 PAC11 PAC12 PAC13 PAC14 PAC15 PAC16 PAC17 PAC18 PAC19
PAC20 PAC21 PAC22 PAC23 PAC24 PAC25 PAC26 PAC27 PAC28 PAC29 PAC30 PAC31 PAC32 PAC33 PAC34 PAC35
0.22U/2/X5R/6.3V/K
GIGABYTE
ANS 8697381
PCI EXPRESS X 16 ,X1
B450 AORUS ELITE V2
1.1
Friday, March 05, 2021
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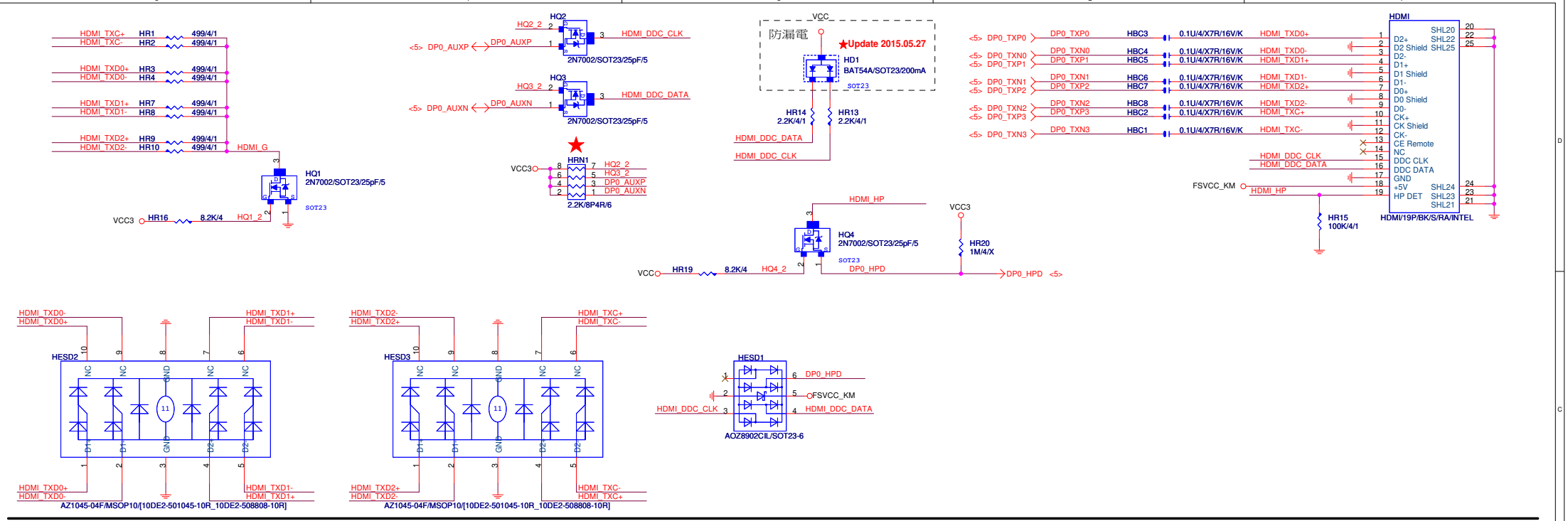
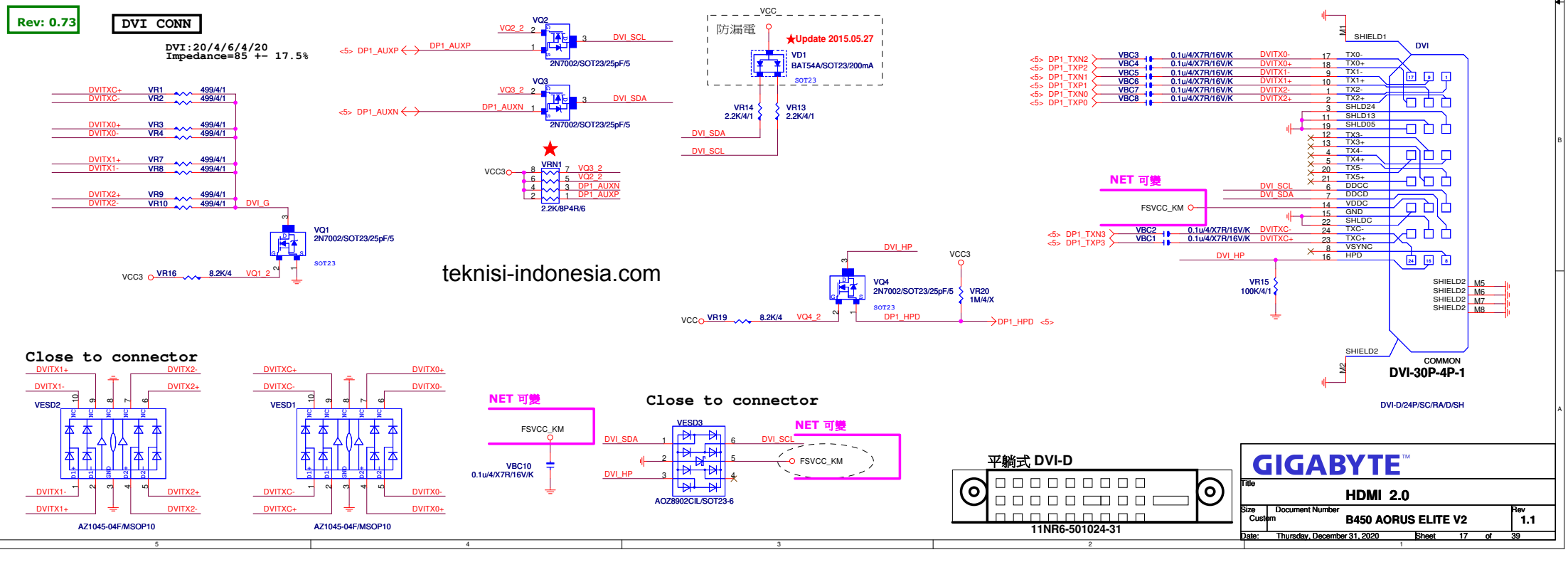

HDMI_TXC+ HR1 499/4/1
HDMI_TXC- HR2 499/4/1
HDMI_TXD0+ HR3 499/4/1
HDMI_TXD0- HR4 499/4/1
HDMI_TXD1+ HR7 499/4/1
HDMI_TXD1- HR8 499/4/1
HDMI_TXD2+ HR9 499/4/1
HDMI_TXD2- HR10 499/4/1
HDMI_G
HQ1
2N7002/SOT23/25pF/5
VCC3 HR16 8.2K/4 HQ1_2
HQ2
HQ2_2
<5> DP0_AUXP DP0_AUXP
HDMI_DDC_CLK
HQ3
HQ3_2
<5> DP0_AUXN DP0_AUXN
HDMI_DDC_DATA
2N7002/SOT23/25pF/5
HRN1
HQ2_2
HQ3_2
DP0_AUXP
DP0_AUXN
2.2K/8P4R/6
VCC
防漏電
★Update 2015.05.27
HD1
BAT54A/SOT23/200mA
SOT23
HR14 2.2K/4/1
HR13 2.2K/4/1
HDMI_DDC_DATA
HDMI_DDC_CLK
HDMI_HP
HQ4
2N7002/SOT23/25pF/5
VCC3
HR20 1M/4/X
VCC HR19 8.2K/4 HQ4_2
DP0_HPD
<5> DP0_HPD
<5> DP0_TXP0 DP0_TXP0 HBC3 0.1U/4/X7R/16V/K HDMI_TXD0+
<5> DP0_TXN0 DP0_TXN0 HBC4 0.1U/4/X7R/16V/K HDMI_TXD0-
<5> DP0_TXP1 DP0_TXP1 HBC5 0.1U/4/X7R/16V/K HDMI_TXD1+
<5> DP0_TXN1 DP0_TXN1 HBC6 0.1U/4/X7R/16V/K HDMI_TXD1-
<5> DP0_TXP2 DP0_TXP2 HBC7 0.1U/4/X7R/16V/K HDMI_TXD2+
<5> DP0_TXN2 DP0_TXN2 HBC8 0.1U/4/X7R/16V/K HDMI_TXD2-
<5> DP0_TXP3 DP0_TXP3 HBC2 0.1U/4/X7R/16V/K HDMI_TXC+
<5> DP0_TXN3 DP0_TXN3 HBC1 0.1U/4/X7R/16V/K HDMI_TXC-
HDMI
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
SHL20 SHL22 SHL25 SHL24 SHL23 SHL21
HDMI_DDC_CLK
HDMI_DDC_DATA
FSVCC_KM
HDMI_HP
HR15 100K/4/1
HDMI/19P/BK/S/RA/INTEL
HESD2
HDMI_TXD0- HDMI_TXD0+ HDMI_TXD1+ HDMI_TXD1-
NC NC GND NC NC
D1+ D1- GND D2+ D2-
AZ1045-04F/MSOP10/[10DE2-501045-10R_10DE2-508808-10R]
HESD3
HDMI_TXD2- HDMI_TXD2+ HDMI_TXC+ HDMI_TXC-
AZ1045-04F/MSOP10/[10DE2-501045-10R_10DE2-508808-10R]
HESD1
DP0_HPD
FSVCC_KM
HDMI_DDC_CLK
HDMI_DDC_DATA
AOZ8902CIL/SOT23-6


Rev: 0.73
DVI CONN
DVI:20/4/6/4/20
Impedance=85 +- 17.5%
DVITXC+ VR1 499/4/1
DVITXC- VR2 499/4/1
DVITX0+ VR3 499/4/1
DVITX0- VR4 499/4/1
DVITX1+ VR7 499/4/1
DVITX1- VR8 499/4/1
DVITX2+ VR9 499/4/1
DVITX2- VR10 499/4/1
DVI_G
VQ1
2N7002/SOT23/25pF/5
VCC3 VR16 8.2K/4 VQ1_2
VQ2
VQ2_2
<5> DP1_AUXP DP1_AUXP
DVI_SCL
VQ3
VQ3_2
<5> DP1_AUXN DP1_AUXN
DVI_SDA
2N7002/SOT23/25pF/5
VRN1
VQ3_2
VQ2_2
DP1_AUXN
DP1_AUXP
2.2K/8P4R/6
VCC
防漏電
★Update 2015.05.27
VD1
BAT54A/SOT23/200mA
SOT23
VR14 2.2K/4/1
VR13 2.2K/4/1
DVI_SDA
DVI_SCL
DVI_HP
VQ4
2N7002/SOT23/25pF/5
VCC3
VR20 1M/4/X
VCC VR19 8.2K/4 VQ4_2
DP1_HPD
<5> DP1_HPD
<5> DP1_TXN2 VBC3 0.1u/4/X7R/16V/K DVITX0-
<5> DP1_TXP2 VBC4 0.1u/4/X7R/16V/K DVITX0+
<5> DP1_TXN1 VBC5 0.1u/4/X7R/16V/K DVITX1-
<5> DP1_TXP1 VBC6 0.1u/4/X7R/16V/K DVITX1+
<5> DP1_TXN0 VBC7 0.1u/4/X7R/16V/K DVITX2-
<5> DP1_TXP0 VBC8 0.1u/4/X7R/16V/K DVITX2+
<5> DP1_TXN3 VBC2 0.1u/4/X7R/16V/K DVITXC-
<5> DP1_TXP3 VBC1 0.1u/4/X7R/16V/K DVITXC+
NET 可變
FSVCC_KM
DVI_SCL
DVI_SDA
DVI_HP
VR15 100K/4/1
M1 SHIELD1
DVI
TX0- TX0+ TX1- TX1+ TX2- TX2+ SHLD24 SHLD13 SHLD05 TX3- TX3+ TX4- TX4+ TX5- TX5+ DDCC DDCD VDDC GND SHLDC TXC- TXC+ VSYNC HPD
SHIELD2 M5
SHIELD2 M6
SHIELD2 M7
SHIELD2 M8
SHIELD2 M2
COMMON
DVI-30P-4P-1
DVI-D/24P/SC/RA/D/SH
teknisi-indonesia.com
Close to connector
VESD2
DVITX1+ DVITX2- DVITX1- DVITX2+
NC NC NC NC NC
D1+ D1- GND D2+ D2-
AZ1045-04F/MSOP10
VESD1
DVITXC+ DVITX0+ DVITXC- DVITX0-
AZ1045-04F/MSOP10
NET 可變
FSVCC_KM
VBC10 0.1u/4/X7R/16V/K
Close to connector
VESD3
DVI_SDA DVI_SCL
DVI_HP
FSVCC_KM
NET 可變
AOZ8902CIL/SOT23-6
平鋪式 DVI-D
11NR6-501024-31
GIGABYTE
Title
HDMI 2.0
Size Custom
Document Number
B450 AORUS ELITE V2
Rev 1.1
Date: Thursday, December 31, 2020
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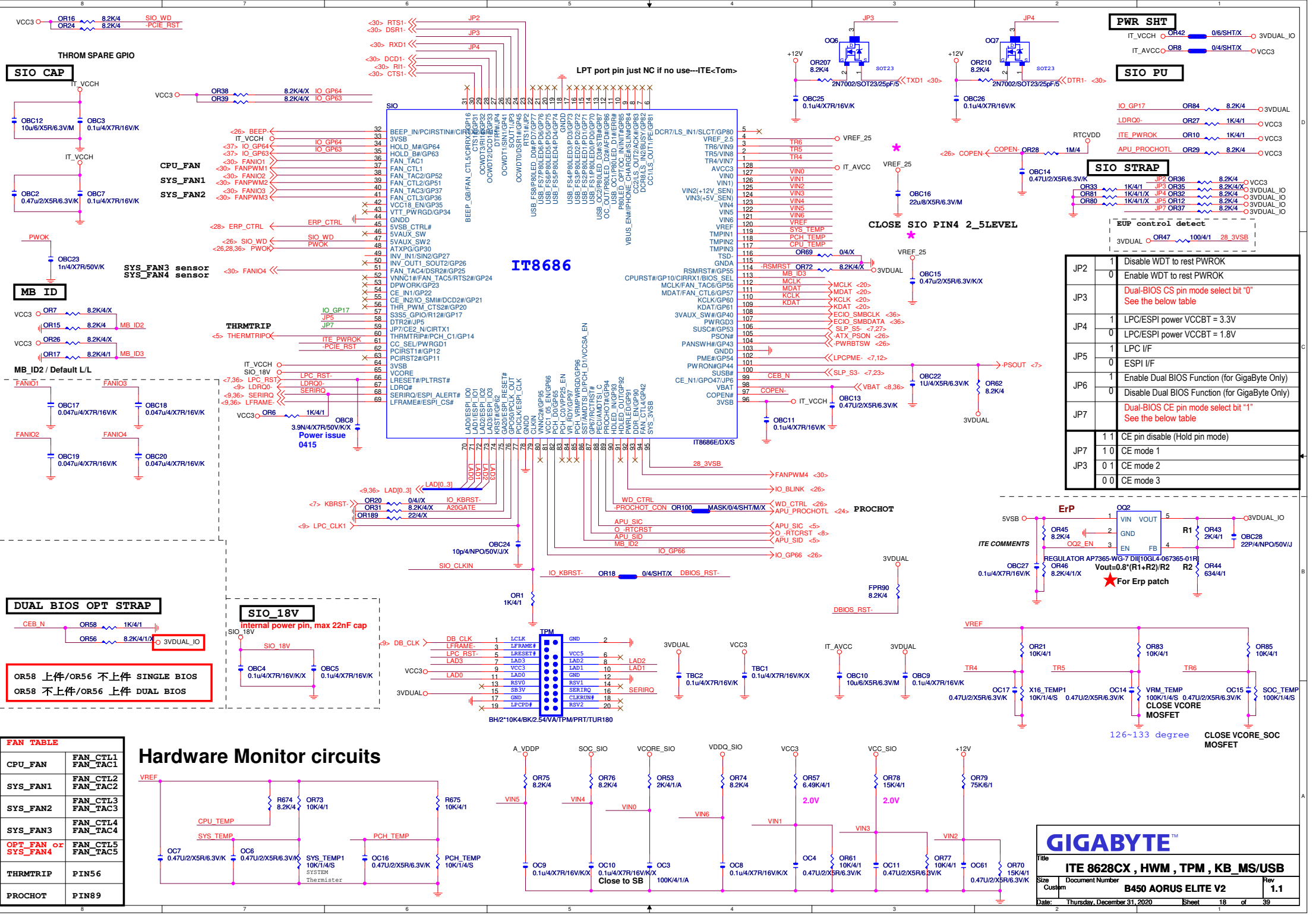

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7 JP3	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3

GIGABYTE™

Title	ITE 8628CX , HWM , TPM , KB_MS/USB	
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
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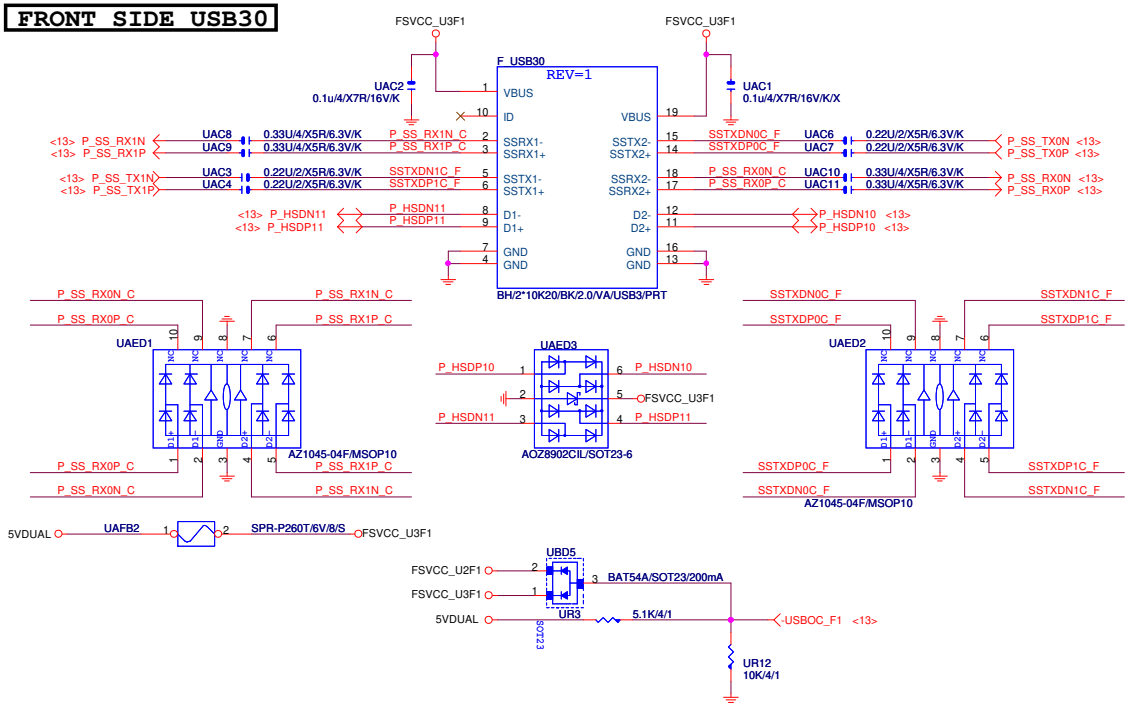
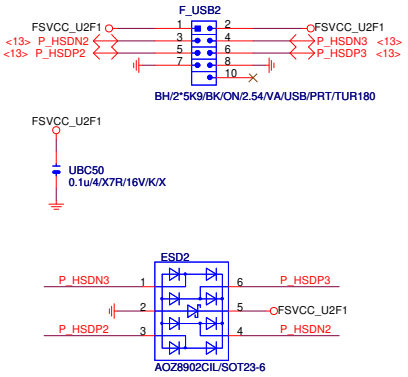
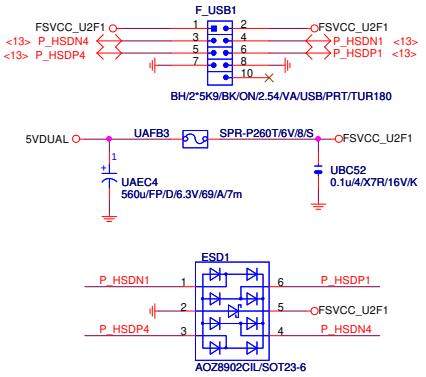
FRONT SIDE USB30



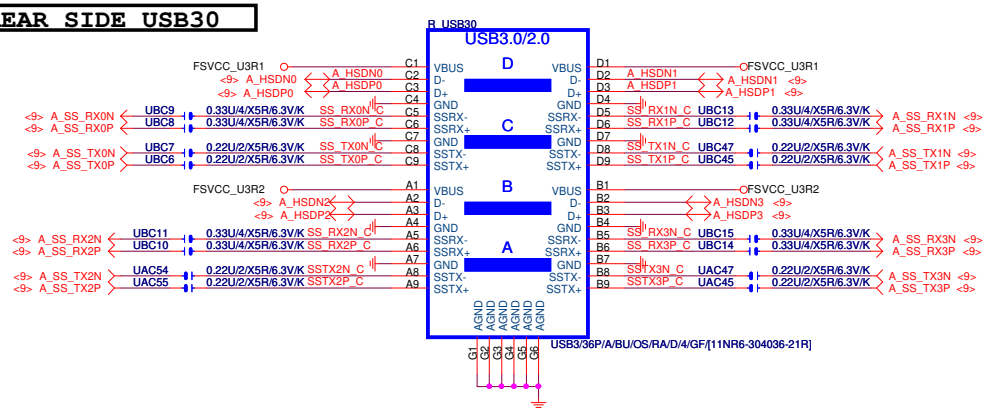
FRONT SIDE USB2

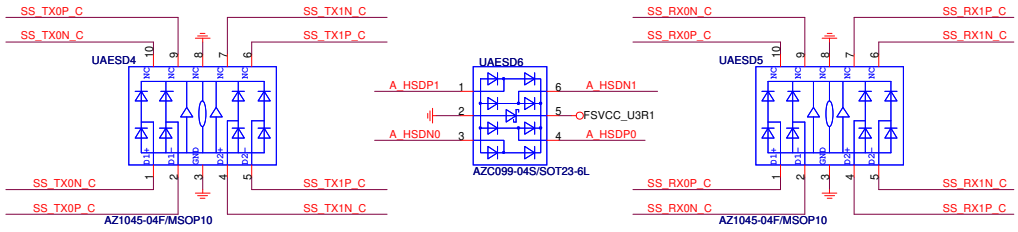


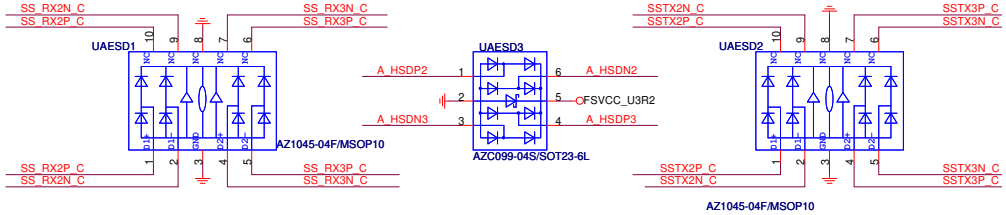
FRONT SIDE USB1

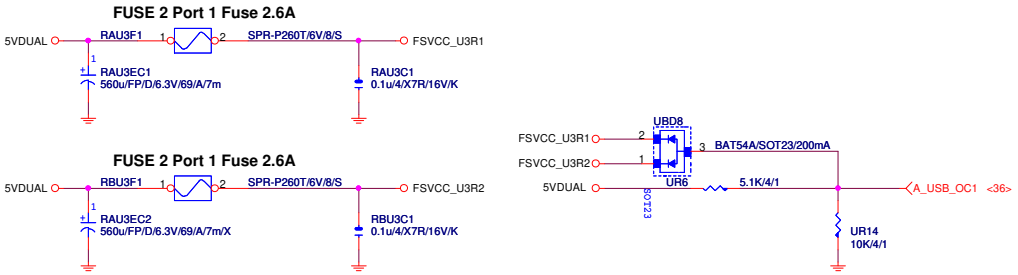


REAR SIDE USB30









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Title	F_USB, R_USB CONN	
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
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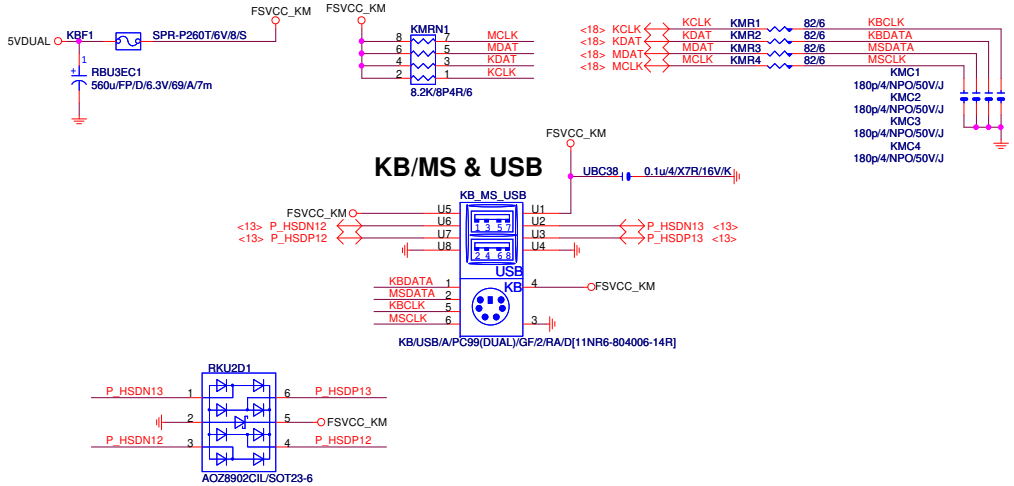
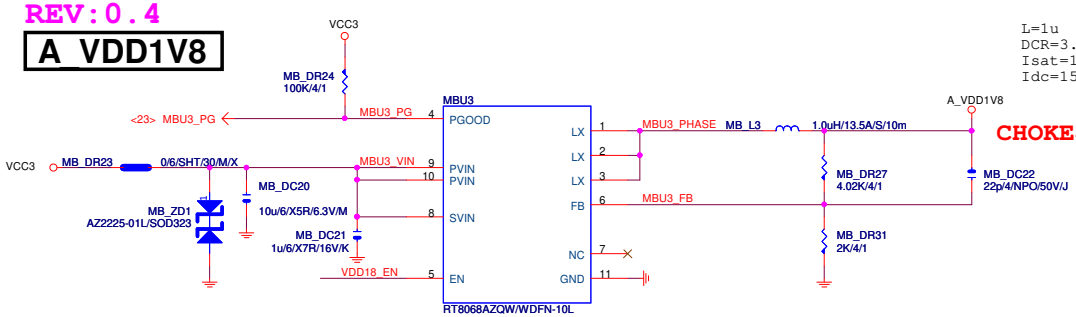


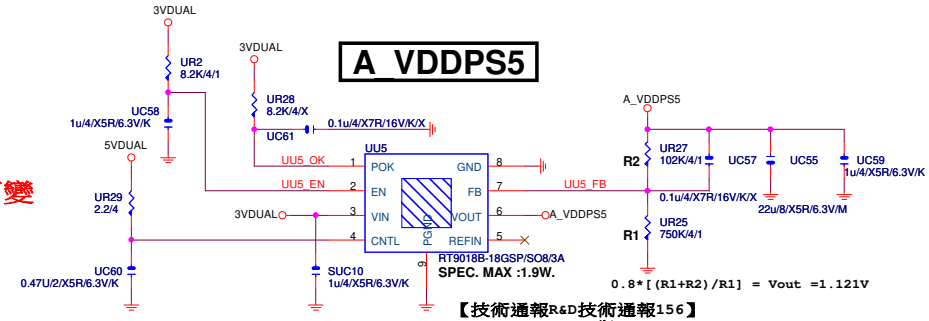
REV:0.4

A_VDD1V8



CHOKE與CAP料號可變

A_VDDPS5



【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
(R1/R2)須做修改為100K以上電阻值

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

PWR SEQ

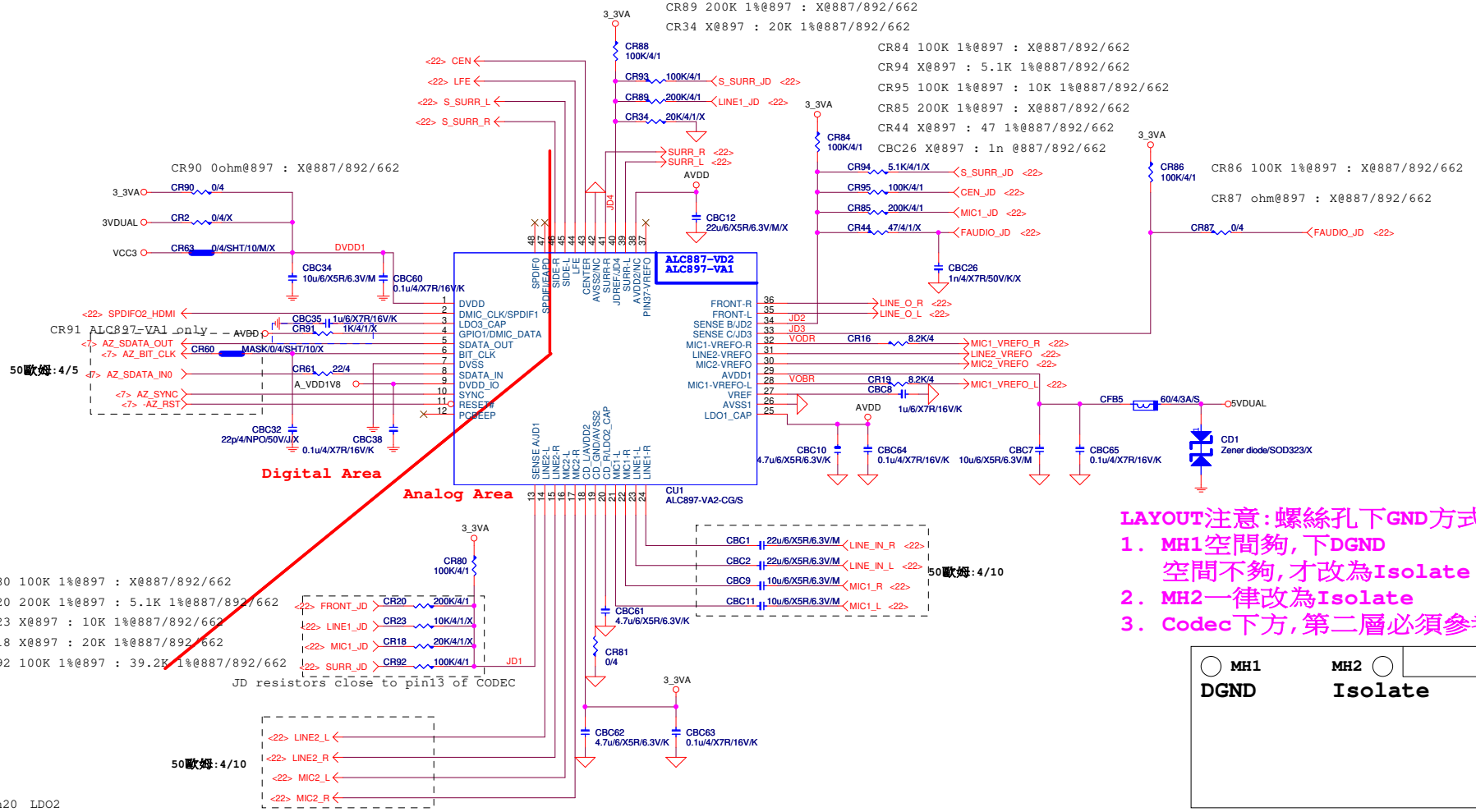
上件

* 刪 MA_DR32

VPP CAP

* 大電容 x0

22u*1PCS



		897	887/892/662
Pin03	LDO3	1uF	10uF
Pin09	DVDD-IO	0.1uF	1uF
Pin18	AVDD2	4.7uF/0.1uF	NC
CR81	AVDD2	0ohm	NC
Pin20	LDO2	4.7uF	NC
Pin25	LDO1	4.7uF	22uF
Pin27	VREF	1uF	10uF
Pin38	AVDD2	NC	22uF

BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
空間不夠,才改為Isolate
2. MH2一律改為Isolate
3. Codec下方,第二層必須參考GND

MH1 DGND MH2 Isolate

LAYOUT注意:要加
GND切割線
音效區域印刷

GIGABYTE

Title	ALC897 CODEC		
Size: Custom	Document Number: B450 AORUS ELITE V2		Rev: 1.1
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Rev 6.0

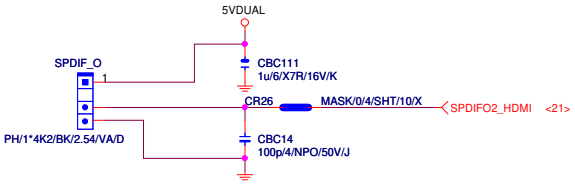
* MOATR1 MASK/0/4/SHT/10/X, MOATC1 0.1u/4/X7R/16V/K/X → Near F_AUDIO

* MOATR2 MASK/0/4/SHT/10/X, MOATC2 0.1u/4/X7R/16V/K/X → Near Codec

MOATR3 0/4/X, MOATC3 0.1u/4/X7R/16V/K/X → Under Audio jack

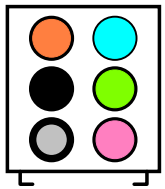
* MOATR4 0/6/SHT/30/M/X → Audio jack - LAN

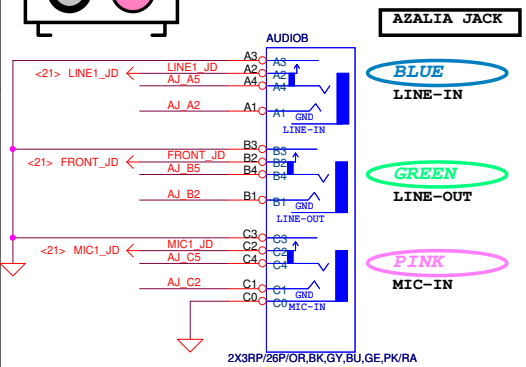
*量產前,MOATR1/MOATR2/MOATR4 ....0ohm改short pad

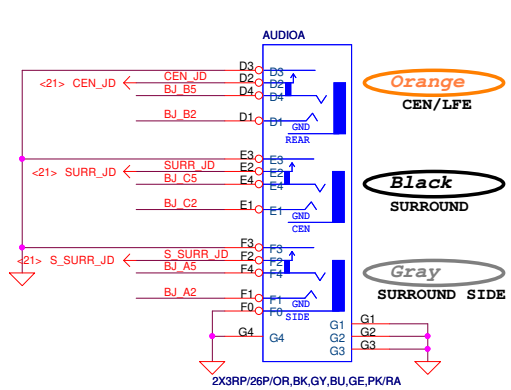


For HDMI SPDIF (依SPEC保留或移除)

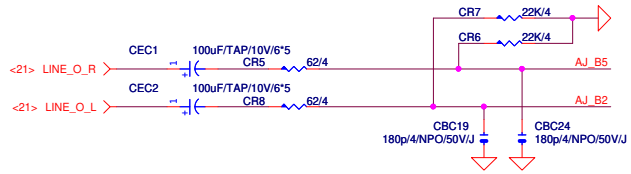
AZALIA JACK



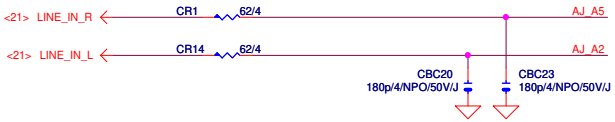




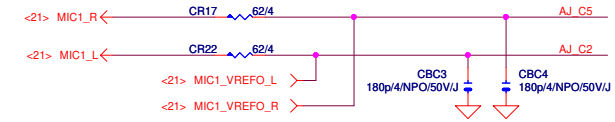
LINE-OUT



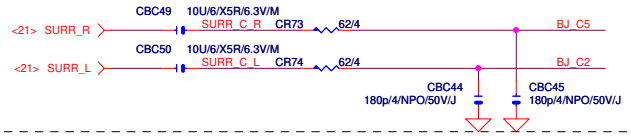
LINE-IN



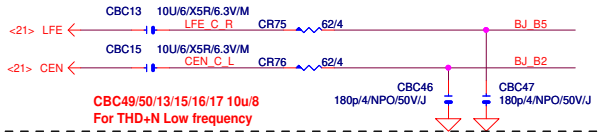
MIC-IN



SURROUND

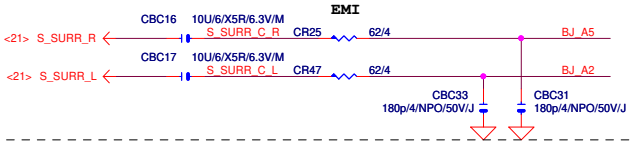


CEN/LFE

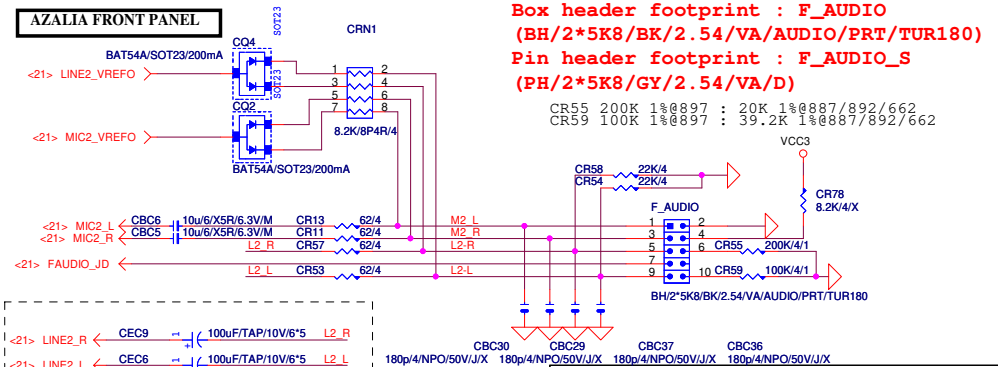


CBC49/50/13/15/16/17 10u/8
For THD+N Low frequency

SURR BACK



AZALIA FRONT PANEL



Box header footprint : F_AUDIO
(BH/2*5K8/BK/2.54/VA/AUDIO/PRT/TUR180)
Pin header footprint : F_AUDIO_S
(PH/2*5K8/GY/2.54/VA/D)

CR55 200K 1%@897 : 20K 1%@887/892/662
CR59 100K 1%@897 : 39.2K 1%@887/892/662

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Title: AUDIO JACK		
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
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PWR SEQ

5VDUAL NPR1 2.2/6 NPU1_VCC
NPC4 1u/6/X7R/16V/K
NPR19 100K/4/1
PCH_1V0_GD
NPU1
<20> MBU3_PG NPR18 0/4/SHT/10/M/X AVDDP_EN
AVDDP_ADJ
EN PGOOD VCC BOOT UGATE PHASE FB CS RF GND LGATE
NPC2 0.1u/6/X7R/25V/K
UGATE_A PHASE_A LGATE_A
RT8237C/D/DFN-10L
NPU1_RF NPR21 470K/4/1 PCH_1V0_GD
NPR12 280K/4/1
NPR20 470K/4/1/X FS=290K OCP=30A
RF: low=>DEM mode, high=>CCM mode.

+12V
NPL1 BEAD 47/4030/15A/S P1V0_VIN
NPC1 0.1u/4/X7R/16V/K Close Choke
NPC3 1u/6/X7R/16V/K Close MOS
NPEC1 100u/OS/D/16V/69/A/35m
CHOKE與CAP料號可變
NPQ1
NTTFS4C10NTAG/WDFN8/993pF/7.4m
UGATE_A NPR2 2.2/6
NPR4 8.2K/4
PHASE_A
LGATE_A
NPQ2
NPR6 2.2/6
NPC7 1n/4/X7R/50V/K
NTTFS4C10NTAG/WDFN8/993pF/7.4m
NPL2 1.0uH/13.5A/S/10m
L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A
A_VDDP
A_VDDP 0.9V or 1.05V
NPC8 22p/4/NPO/50V/J/X
AVDDP_ADJ
0.704*(1+RS/RO) = Vout
RS NPR8 2K/4/1
RO NPR13 7.15K/4/1
NPC11 22u/8/X5R/6.3V/M
NPEC2 560u/FP/D/6.3V/69/A/7m

A_VDDP
NPC10 22u/8/X5R/6.3V/M
請放置CHOKE一出來的地方

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

Remote sense請從最重的負載端點拉回
AVDDP_ADJ NPR3 9.31K/4/1
VCC3 PR84 1K/4/1
NPQ5 2N7002/SOT23/25pF/5
NPQ5_2
NPQ7 MMBT2222A/SOT23/600mA/40
<5,20,36> CORETYPE1 CORETYPE1 PR85 8.2K/4 NPQ7_2

VCC3
SQR1 8.2K/4
<7,18> SLP_S3- SLP_S3- SQD1
<7> S0A3_GPIO S0A3_GPIO
GLOBE_S3- GLOBE_S3- <20,27,28>
BAT54A/SOT23/200mA SQC2 0.1U/4/X7R/16V/K/X

VCC3
SQR2 39K/4/1/A
<24> VR_RDY SQD2
PCH_1V0_GD
APU_PWOK <7>
SQR3 100K/4/1
SQC1 2.2u/4/X5R/6.3V/M
PM_PWROK SQD3
VDDIO_MEM_PG
<27> VPP_MEM_PG SQD4
BAT54A/SOT23/200mA

OK
3VDUAL
CPUVDD_EN <24>
Q66 2N7002/SOT23/25pF/5
R361 8.2K/4
Q66_2
Q65 MMBT2222A/SOT23/600mA/40
VDDIO_MEM R348 1K/4/1 Q65_2
R365 8.2K/4/1/X
<5,27> AM4R1 D47
BAT54A/SOT23/200mA C226 2.2u/4/X5R/6.3V/M/X

VCC3
R1 8.2K/4
VDDIO_MEM_PG
Q1 2N7002/SOT23/25pF/5
Q66_2

VCC3
PR83 8.2K/4
PM_PWROK <12>
5VDUAL
R360 8.2K/4
Q64 2N7002/SOT23/25pF/5
Q64_2
Q63 MMBT2222A/SOT23/600mA/40
PM_1V05 R347 10K/4/1 Q63_2
R363 1K/4/1/X
C227 2.2u/4/X5R/6.3V/M
Q67 MMBT2222A/SOT23/600mA/40
PM_2V5 R349 2.49K/4/1 Q67_2
R364 1K/4/1
C228 2.2u/4/X5R/6.3V/M/X

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Title	POWER SEQUENCE	
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
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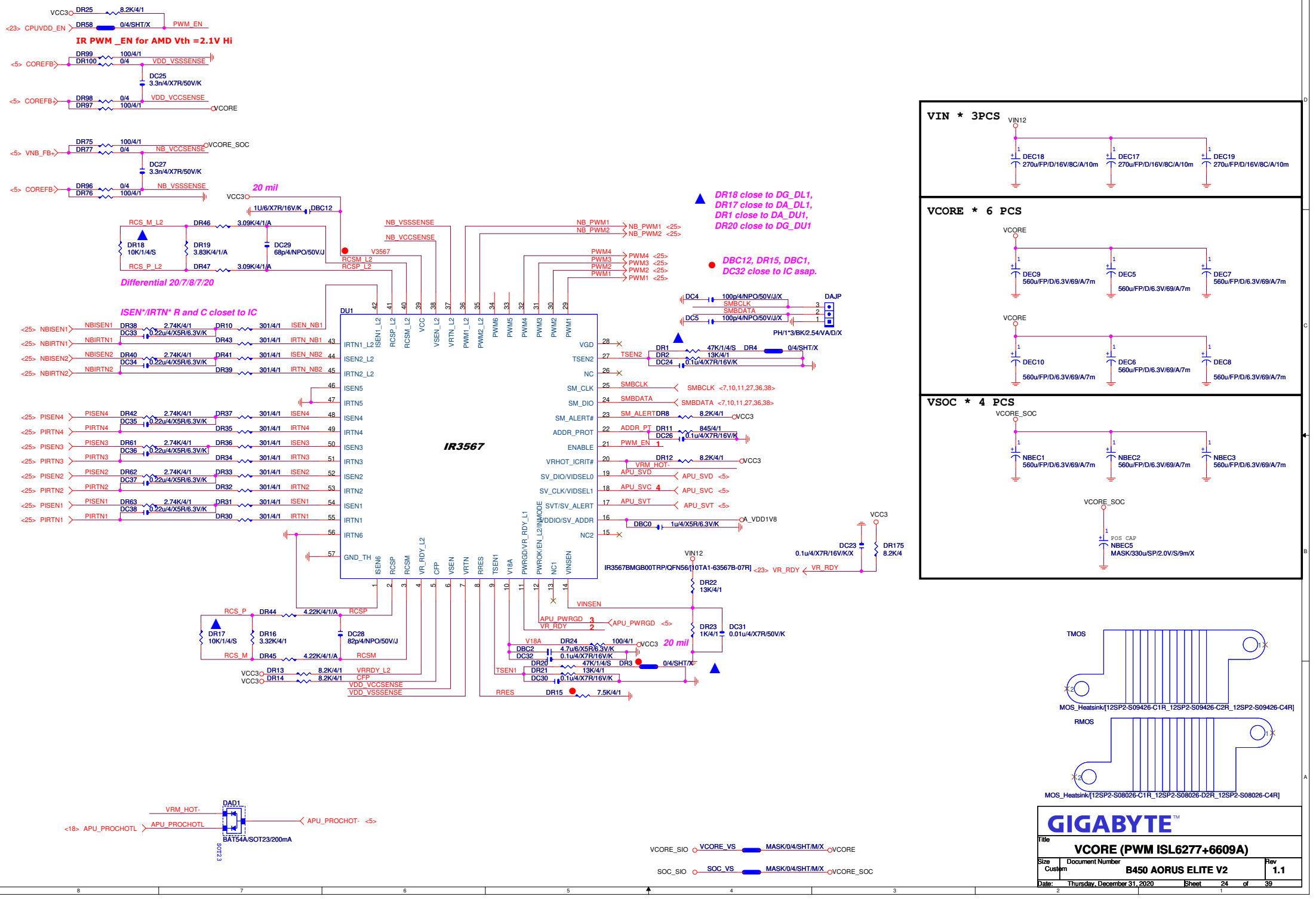
IR PWM _EN for AMD Vth =2.1V Hi
20 mil
Differential 20/7/8/7/20
ISEN*/IRTN* R and C closet to IC
DR18 close to DG_DL1,
DR17 close to DA_DL1,
DR1 close to DA_DU1,
DR20 close to DG_DU1
DBC12, DR15, DBC1,
DC32 close to IC asap.
IR3567
IR3567BMGB00TRP/QFN56/[10TA1-63567B-07R]
VIN * 3PCS
VCORE * 6 PCS
VSOC * 4 PCS
TMOS
RMOS
MOS_Heatsink/[12SP2-S09426-C1R_12SP2-S09426-C2R_12SP2-S09426-C4R]
MOS_Heatsink/[12SP2-S08026-C1R_12SP2-S08026-D2R_12SP2-S08026-C4R]
BAT54A/SOT23/200mA
GIGABYTE
VCORE (PWM ISL6277+6609A)
B450 AORUS ELITE V2
1.1
Thursday, December 31, 2020
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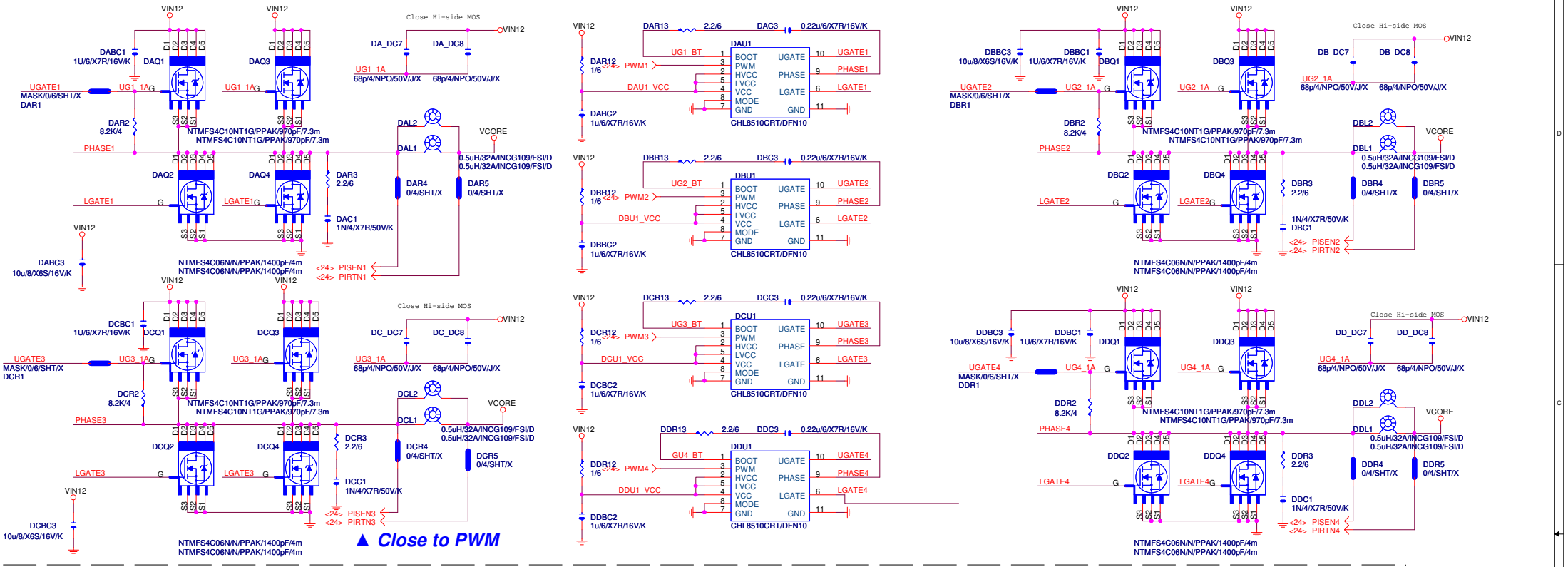

GIGABYTE™

Title	VCORE MOS	
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
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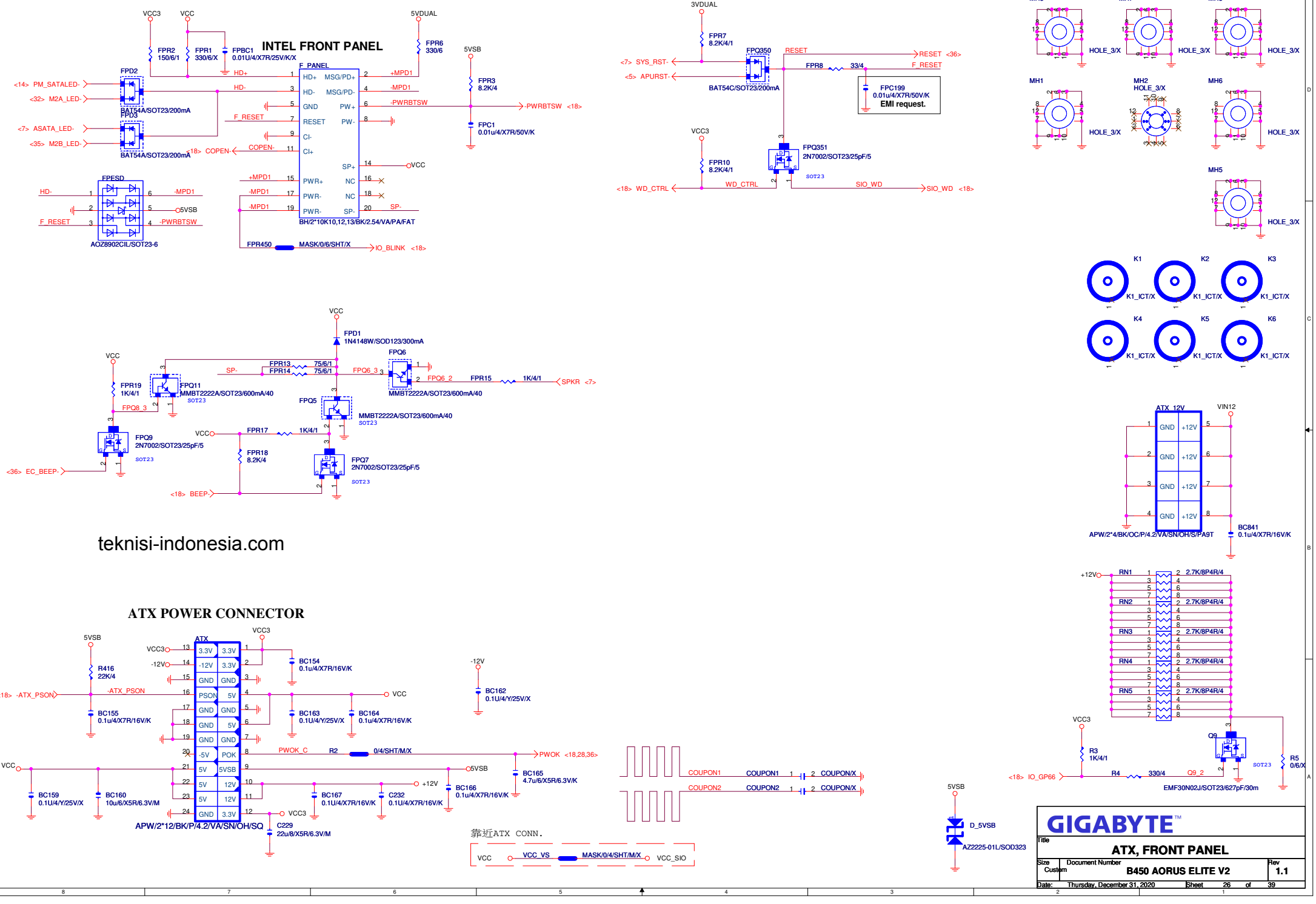
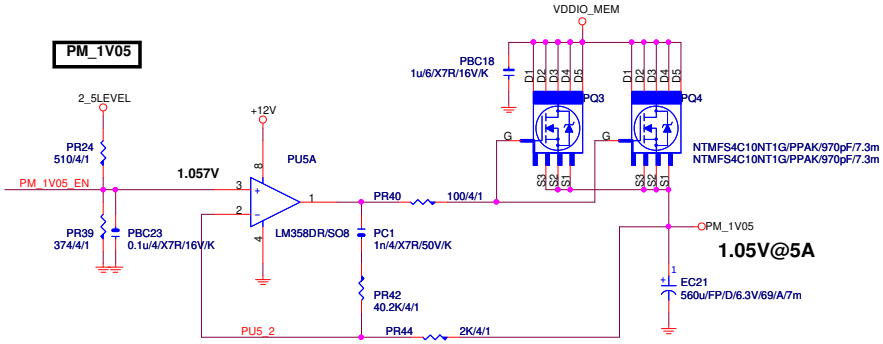
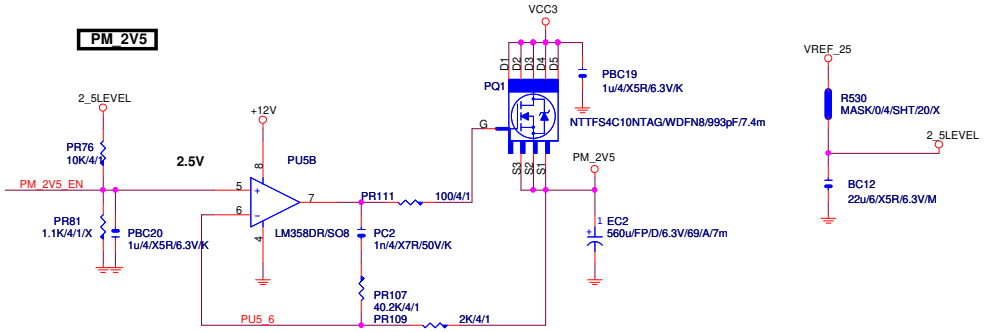
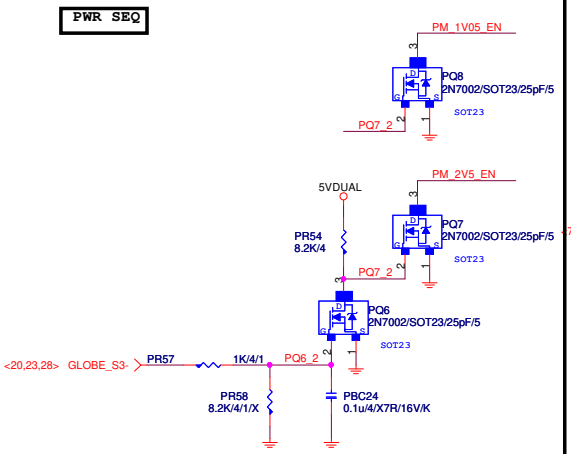
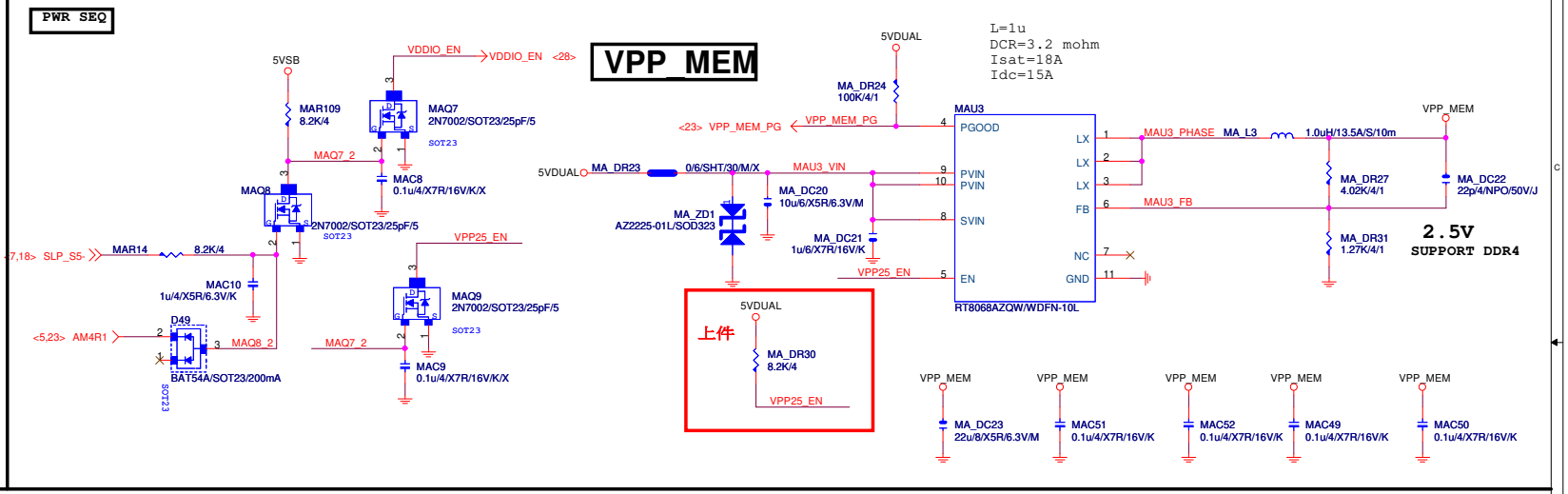










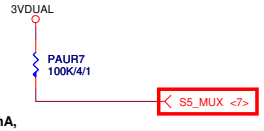
VDDCR_SOC_S5

S5_MUX: S0-->High, S5-->Low

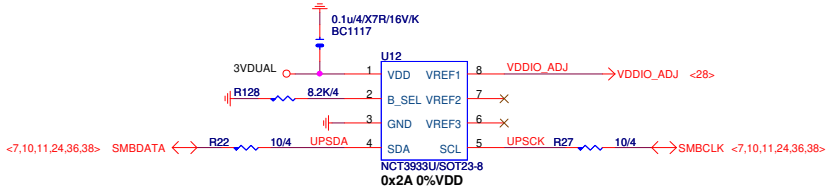
H: VDDCR_SOC_S5 will track VCORE_SOC.

L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.

If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.



AM4 S5: 0.775V, 200mA,
S0:VAR, 900mA.



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Title	PM POWER	
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
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5VDUAL

+12V
R341 8.2K/4
5VDUAL_GATE
5VSB
R97 8.2K/4
D2 2N7002/SOT23/25pF/5 SOT23
PWOK_L
D3 2N7002/SOT23/25pF/5
C8 0.1u/4/X7R/16V/K/X
<18,26,36> PWOK
R351 1K/4/1 PWOK_H
5VDUAL
VCC
Q32 NTMFS4C10NT1G/PPAK/970pF/7.3m
5VSB
R95 1K/4/1
P_GATE
Q31 P2003ED/P/TO252/30m
C7 0.1u/4/X7R/16V/K
EC31 100u/OS/D/6.3V/66/A/35m
EC24 100u/OS/D/6.3V/66/A/35m
Q280 2N7002/SOT23/25pF/5
PWOK_L
5VSB
R100 8.2K/4/1
Q279 2N7002/SOT23/25pF/5
<18> ERP_CTRL
ERP_CTRL
C10 0.1u/4/X7R/16V/K/X

3VDUAL

5VDUAL
C234 0.1u/4/X7R/16V/K
3VDUAL
C236 0.1u/4/X7R/16V/K
EC40 560u/FP/D/6.3V/69/A/7m
Q36 L1085DG/TO252/5A
3VDUAL
R1735 301/4/1
R1737 510/4/1
1.25*(1+510/301)=3.36V

VDDIO_MEM

0.022u/4/X7R/25V/K
MC3
MC2 22P/4/NPO/50V/J
MR5 16.2K/4/1
DDR12V_PHASE
MU1
PHASE BOOT
COMP/SD UG
FB GND
VCC LG/OCSET
BGND
RT8120DGS/SOP8
<27> VDDIO_EN
MU1_GU
MR3 2.2/6
DDR12VU_G
MU1_FB
MQ3 BAT54C/SOT23/200mA
MR4 2.2/6
MBC3 1U/6/X7R/16V/K
RT8120DGS VREF is 0.8V
MR2 11.8K/4/1
MR9 8.2K/4
MC5 0.1u/6/X7R/25V/K
5VDUAL
MBC2 0.1u/4/X7R/16V/K
ML1 47/4030/15A/S
MQ1 NTMFS4C10NT1G/PPAK/970pF/7.3m
MBC1 1u/6/X7R/16V/K
MEC1 560u/FP/D/6.3V/69/A/7m
MEC2 560u/FP/D/6.3V/69/A/7m
1.2V@20A
ML2 1uH/35A/IMD109/BP/D
MQ2 NTMFS4C10NT1G/PPAK/970pF/7.3m
DDR12VL_G
MR8 2.2/6
MC4 1n/4/X7R/50V/K
MR14 220/4
MC6 0.022u/4/X7R/25V/K
MR6 1K/4/1
MC1
MEC3 560u/FP/D/6.3V/69/A/7m
MEC4 560u/FP/D/6.3V/69/A/7m
MEC5 560u/FP/D/6.3V/69/A/7m
MR7 1.91K/4/1
MU1_FB
<27> VDDIO_ADJ
VDDIO_ADJ
MR1 0/4/SHT/X
Default: 1.60V
0.8*(1+1K/2K)=1.2V
VDDIO_MEM
MBC9 1u/4/X5R/6.3V/K
MBC10 1u/4/X5R/6.3V/K
MBC11 1u/4/X5R/6.3V/K
VDDQ_SIO
DDR_VS
MASK/0/4/SHT/M/X
VDDIO_MEM

DDRVTT

★ NEW
★ Check
VDDIO_MEM
5VDUAL
MAC2 1u/4/X5R/6.3V/K
MAR5 1K/4/1
MAU1
VIN NC
GND EN2
VREF VCNTL
VOUT EN1
GND
NCT3103S/SOP8/2A
1.1A MAX
MA_VTT_REF
DDRVTT
MAC1 0.01u/4/X7R/50V/K
MAR7 1K/4/1
DDRVTT_EN
MAC7 10u/6/X5R/6.3V/M
DDRVTT
MAC5 10u/6/X5R/6.3V/M
DDR12V_PHASE
MQ4 NTMFS4C10NT1G/PPAK/970pF/7.3m
DDR12VL_G
<20,23,27> GLOBE_S3-
GLOBE_S3-
MAR6 0/4/SHT/X
DDRVTT_EN

GIGABYTE™

Title	DDR PWR, 5VDUAL, 3VDUAL	
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LAN:RTL8118 R2.03

LAR12 2.49K/4/1

LAU1

RTL8111G(S)/8106E

RTL8118-CG/S[10HP2-408118-20R]

LA_XTALI
LAX1
25M/16p/30ppm/49US/20/D
LAC5 20p/4/NPO/50V/J
LAC6 20p/4/NPO/50V/J

FOR ERP WAKEUP
MASK/0/6/SHT/M/X

SRCCLK-->50歐姆:[18/4/10/4/18]

LA_ ML-->80歐姆:[15/5/5/5/15]

L1+CLK REQ# 節能:
需對應LA_SRCCLK_LAN之CLKREQ#

MDI ESD

LAESD1
LAESD2
AZC399-04S.R7G/SOT23-6L/[10DEF-510399-10R]

LAN POWER

(CLOSE LAU1 PIN22,30,3,8)

LABC2:1U CLOSE PIN22[REALTEK REQ]

(CLOSE LAU1 PIN23)

(CLOSE LAU1 PIN:11,32)

PWR SURGE

LABC18,27:CLOSE PIN11[REALTEK SURGE]
LABC14,20:CLOSE PIN32[REALTEK SURGE]

(CLOSE LAU1 PIN24)

可變

USB_LAN

RAU3D3
AOZ8902CIL/SOT23-6

USB_LAN CONNECTOR

LAN 100 Ohm
USB 90 Ohm

USB+LAN/1G/GO,Y/OS/RA/D/12C/ES/[11NR6-702009-Z1R_11NR6-702009-R3R]

UBD2
BAT54A/SOT23/200mA

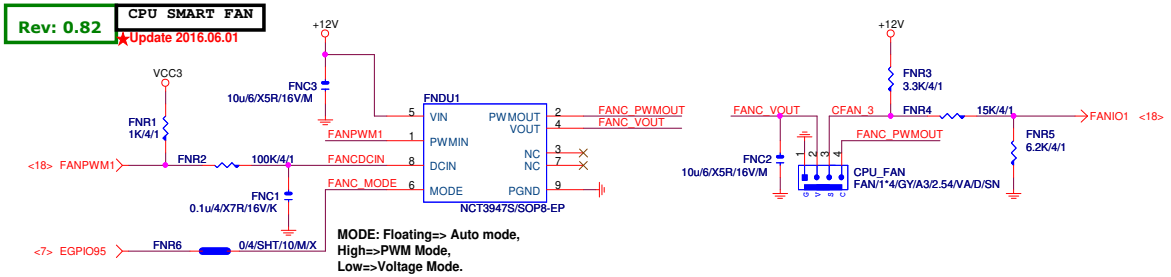
EMI SHORT PAD

PS:視EMI需求

Rev: 0.82

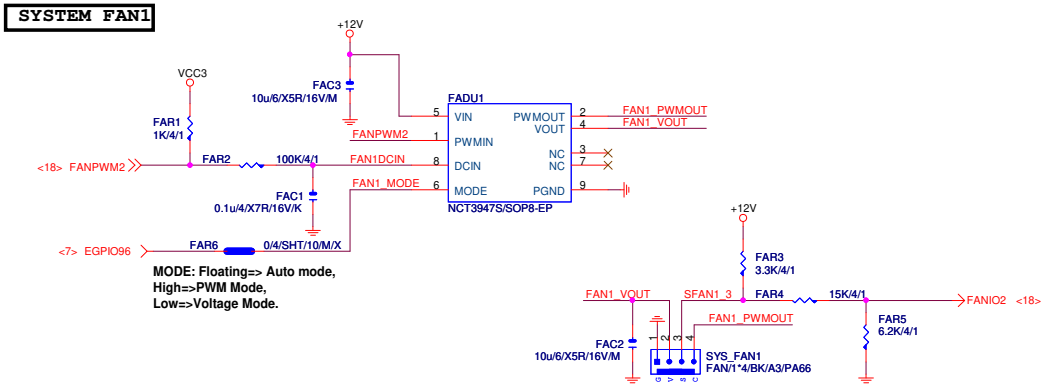
CPU SMART FAN

★Update 2016.06.01



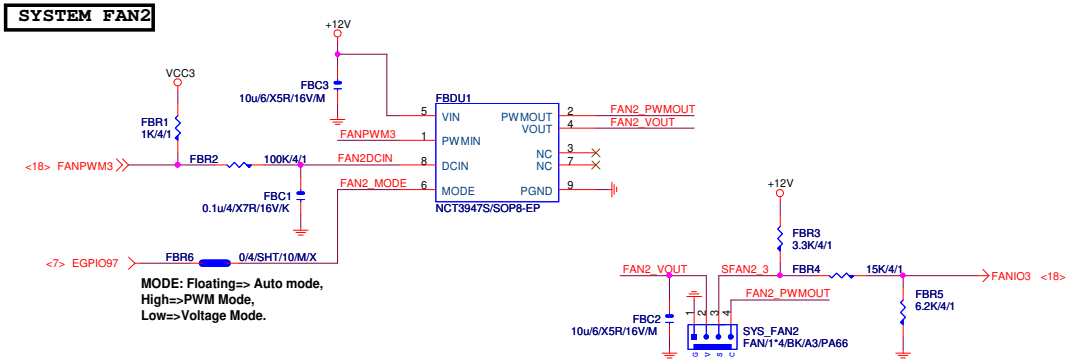
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

SYSTEM FAN1



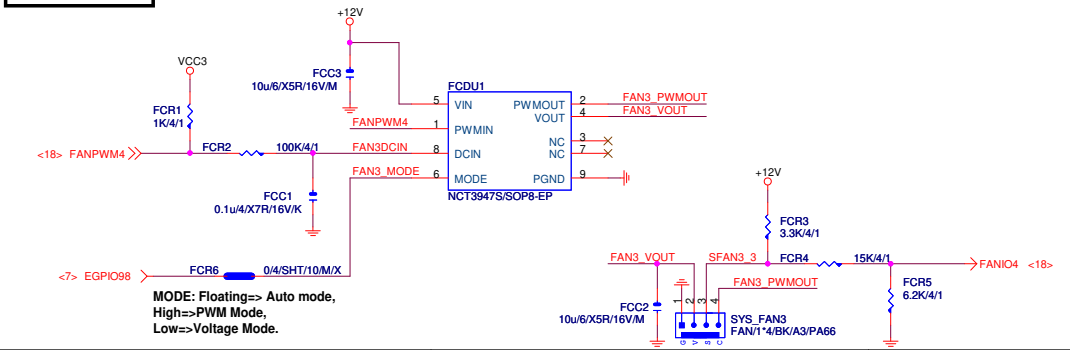
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

SYSTEM FAN2



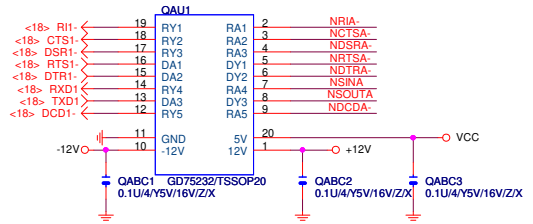
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

SYSTEM FAN3

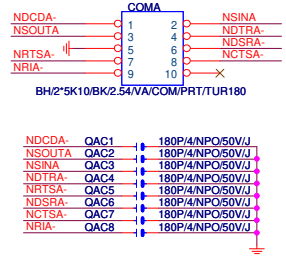


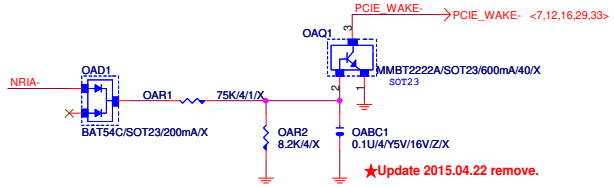
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

COM PORT



COMA





★Update 2015.04.22 remove.

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GIGABYTE™

Title	PCIE X8, SWITCH	
Size: Custom	Document Number: B450 AORUS ELITE V2	Rev: 1.1
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GIGABYTE™

Title: DP to VGA

Size	Document Number	Rev
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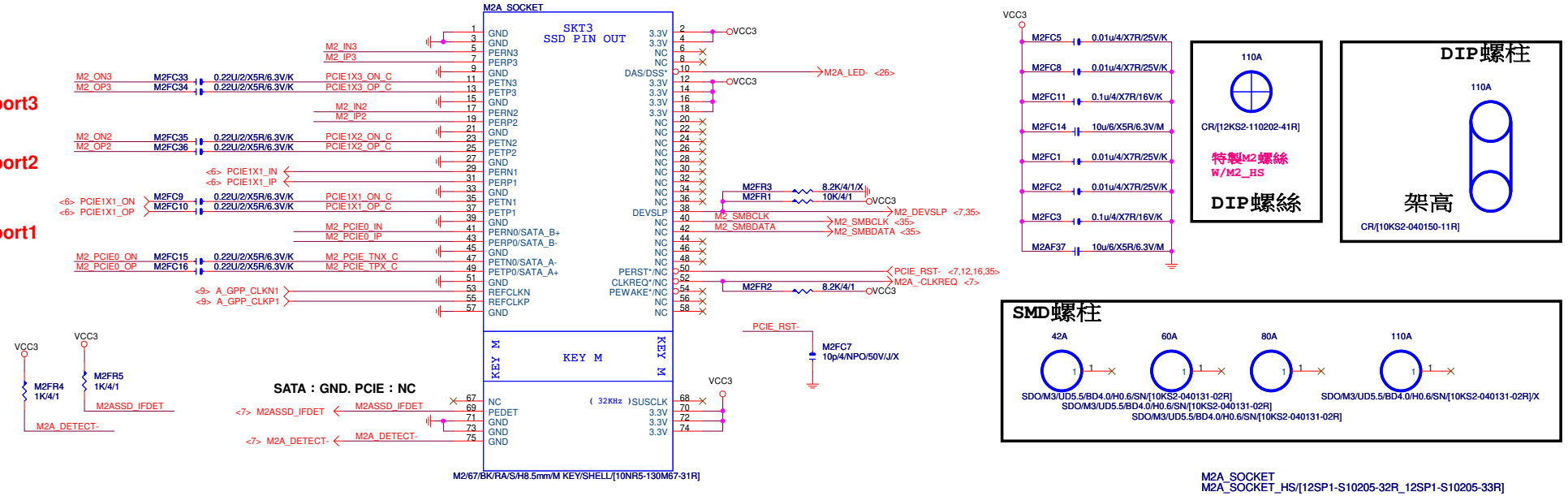
Rev 0.5

M.2 Lane4 from AM4 port3

M.2 Lane4 from AM4 port2

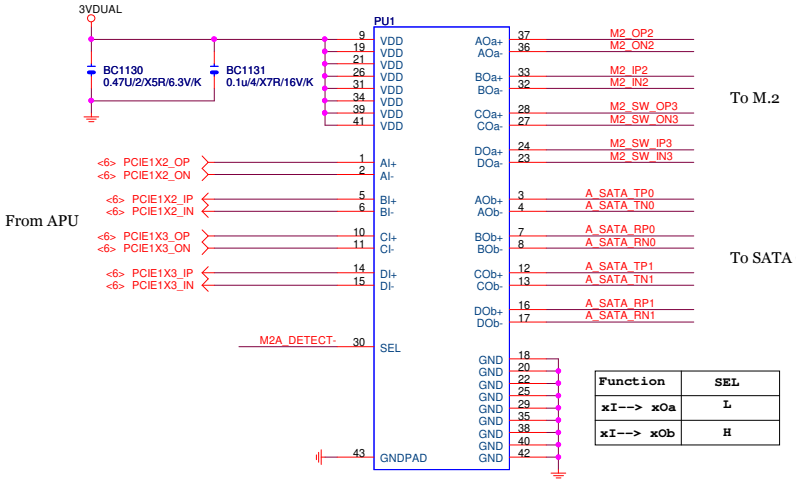
M.2 Lane4 from AM4 port1

by SWITCH Select



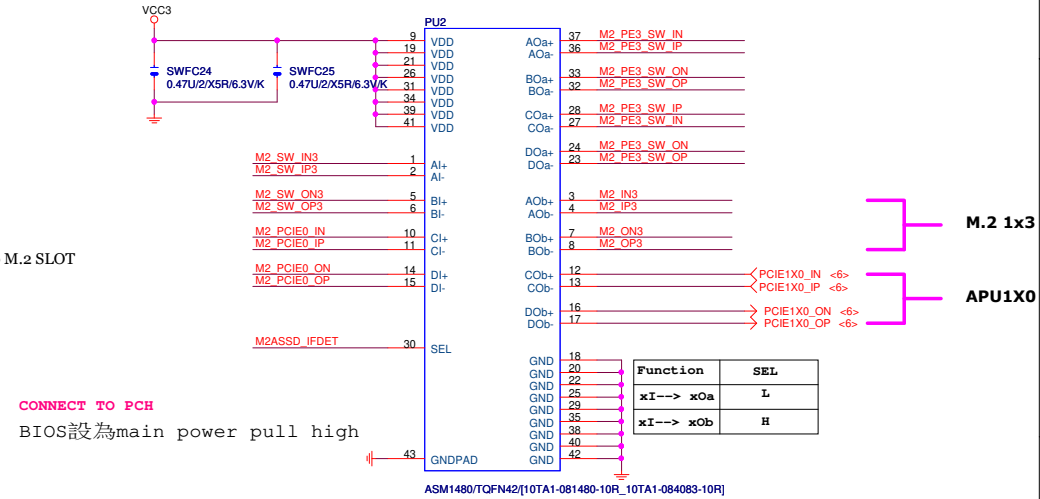
M2A_SOCKET
M2A_SOCKET_HS/[12SP1-S10205-32R_12SP1-S10205-33R]

M2 HEATSINK

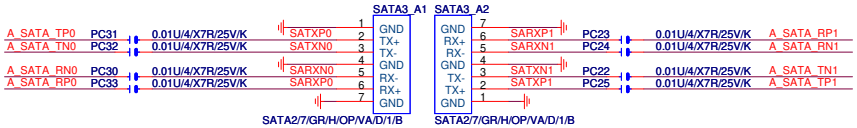


PCIE GEN3 SW CBTL04083BBS/HVQFN32[10TA1-081480-10R_10TA1-084083-10R]

GEN3 :CBTL04083BBS/HVQFN32[10TA1-084083-10R]



ASM1480/TQFN42/[10TA1-081480-10R_10TA1-084083-10R]



SATA2/7/GR/H/OP/VA/D/1/B

SATA2/7/GR/H/OP/VA/D/1/B

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Title: M.2 SOCKET

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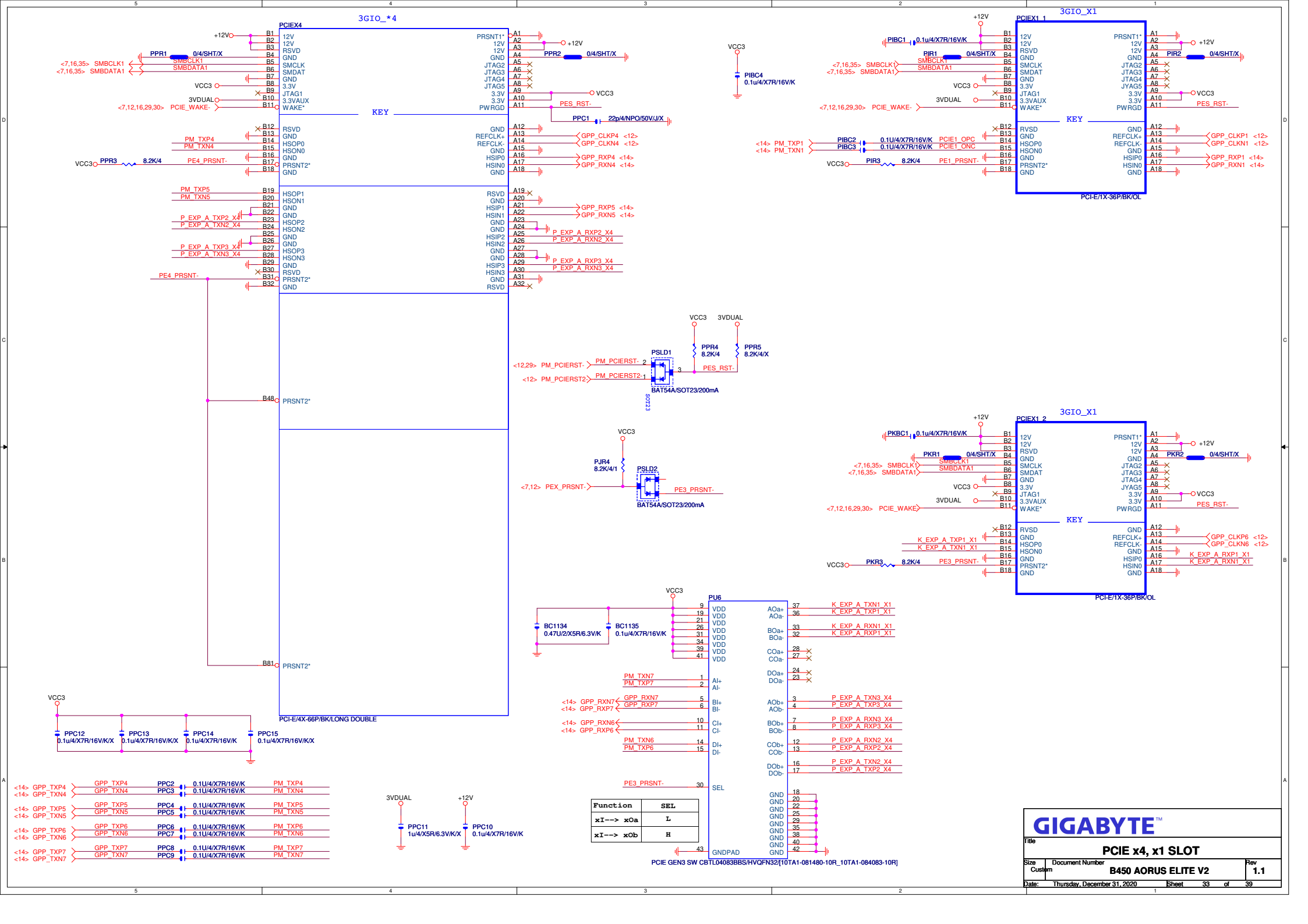
3GIO_*4
PCIEX4
PCI-E/4X-66P/BK/LONG DOUBLE
KEY
3GIO_X1
PCIEX1_1
PCI-E/1X-36P/BK/OL
PCIEX1_2
PCI-E/1X-36P/BK/OL
PU6
PCIE GEN3 SW CBTL04083BBS/HVQFN32[10TA1-081480-10R_10TA1-084083-10R]
PSLD1
PSLD2
BAT54A/SOT23/200mA
Function
SEL
xI--> xOa
L
xI--> xOb
H
GIGABYTE
Title
PCIE x4, x1 SLOT
Size
Custom
Document Number
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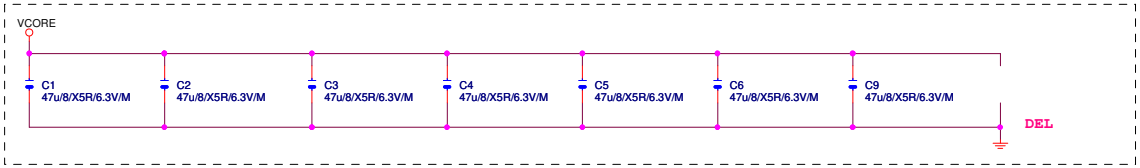

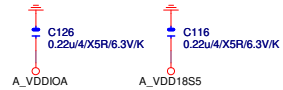

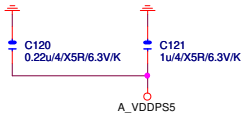

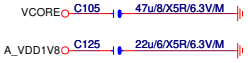

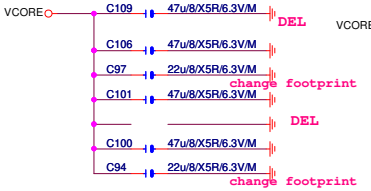

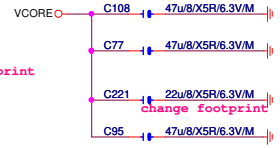

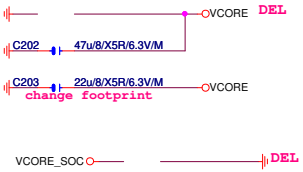

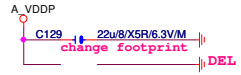

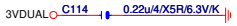

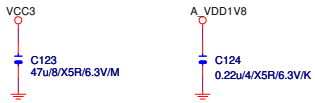

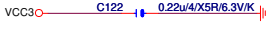

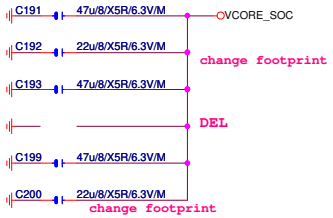

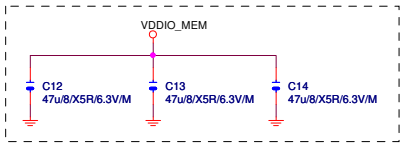

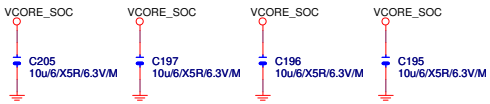

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CPU TOP CAVITY

VCORE C70 47u/8/X5R/6.3V/M
VCORE C223 22u/8/X5R/6.3V/M change footprint
VCORE C63 47u/8/X5R/6.3V/M
VCORE DEL
VCORE C65 47u/8/X5R/6.3V/M
VCORE C62 22u/6/X5R/6.3V/M
C18 47u/8/X5R/6.3V/M VDDIO_MEM

VCORE C64 47u/8/X5R/6.3V/M
VCORE C225 22u/8/X5R/6.3V/M change footprint
VCORE C224 47u/8/X5R/6.3V/M
VCORE DEL
C53 47u/8/X5R/6.3V/M VCORE
C17 47u/8/X5R/6.3V/M VDDIO_MEM

C52 47u/8/X5R/6.3V/M VCORE_SOC
C26 22u/8/X5R/6.3V/M VCORE_SOC change footprint
C27 47u/8/X5R/6.3V/M VCORE_SOC
VCORE_SOC DEL
C93 47u/8/X5R/6.3V/M VCORE_SOC
C25 22u/6/X5R/6.3V/M VCORE_SOC
VDDIO_MEM C20 47u/8/X5R/6.3V/M

Cross Plane CAP
VCORE EMC3 0.1u/4/X7R/16V/K VCORE_SOC
EMC5 0.1u/4/X7R/16V/K
EMC7 0.1u/4/X7R/16V/K
EMC8 0.1u/4/X7R/16V/K
EMC9 0.1u/4/X7R/16V/K
EMC10 0.1u/4/X7R/16V/K
EMC11 0.1u/4/X7R/16V/K

VCORE EMC12 0.1u/4/X7R/16V/K
EMC13 0.1u/4/X7R/16V/K
EMC23 0.1u/4/X7R/16V/K

80B
CR[12KS2-110202-41R]
特製M2螺絲
W/M2_HS
DIP螺絲

DIP螺柱 80B
架高
CR[10KS2-040150-11R]

SMD螺柱
42B 60B 80B
SDO/M3/UD5.5/BD4.0/H0.6/SN/[10KS2-040131-02R]
SDO/M3/UD5.5/BD4.0/H0.6/SN/[10KS2-040131-02R]/X

M2B_SOCKET
M2B_SOCKET_HS/[12SP1-S07205-72R_12SP1-S07205-73R]/X

M2 HEATSINK

Rev 0.5

M2B_SOCKET
SKT3
SSD PIN OUT
KEY M

M2_PCIE_IN18_SW
M2_PCIE_IP18_SW
M2_PCIE_TN18_SW M2BC17 0.22u/2/X5R/6.3V/K M2_PCIE_TN18_SWC
M2_PCIE_TP18_SW M2BC13 0.22u/2/X5R/6.3V/K M2_PCIE_TP18_SWC
M2_PCIE_IN17_SW
M2_PCIE_IP17_SW
M2_PCIE_TN17_SW M2BC18 0.22u/2/X5R/6.3V/K M2_PCIE_TN17_SWC
M2_PCIE_TP17_SW M2BC19 0.22u/2/X5R/6.3V/K M2_PCIE_TP17_SWC
<12> M2B_CLKN
<12> M2B_CLKP

M2BR3 8.2K/4/1/X
M2BR1 10K/4/1
M2_SMBCLK
M2_SMBDATA
M2BR6 8.2K/4/1/X
M2BR2 8.2K/4/1
PCIE_RST- <7,12,16,32>
M2B_CLKREQ <12>
M2_DEVSLP <7,32> CHECK
M2B_LED- <26>
PCIE_RST-
M2BC7 10p/4/NPO/50V/J/X

支援 M.2 function only

VCC3
M2BR4 1K/4/1
M2B_DETECT-
M2BR5 0/4/SHT/M/X
M2B_PRSNT- <7,14>
CHECK
M2/67/BK/RA/S/H8.5mm/M KEY/SHELL/[10NR5-130M67-31R]

VCC3
M2MC1 0.01u/4/X7R/50V/K
M2MC2 0.01u/4/X7R/50V/K
M2MC3 0.1u/4/X7R/16V/K
M2MC37 10u/6/X5R/6.3V/M
M2MC5 0.01u/4/X7R/50V/K
M2MC8 0.01u/4/X7R/50V/K
M2MC11 0.1u/4/X7R/16V/K
M2MC14 10u/6/X5R/6.3V/M

SMBDATA1 <7,16,33>
M2AQ2 EMF30N02J/SOT23/627pF/30m/K
A_VDD1V8 M2AR14 8.2K/4/X
<32> M2_SMBDATA
M2_SMBDATA M2AR12 8.2K/4/X A_VDD1V8
M2AD2 BAT54FN2/DFN2L/0.2A/[10DKM-320542-01R_10DKM-770070-01R]/X
Footprint : DIODE_DFN2L

SMBCLK1 <7,16,33>
M2AD1 BAT54FN2/DFN2L/0.2A/[10DKM-320542-01R_10DKM-770070-01R]/X
Footprint : DIODE_DFN2L
<32> M2_SMBCLK
M2_SMBCLK M2AR9 8.2K/4/X A_VDD1V8

VCC3
SWFC26 0.47U/2/X5R/6.3V/K
SWFC27 0.47U/2/X5R/6.3V/K

PU3
VDD AOa+ AOa- BOa+ BOa- COa+ COa- DOa+ DOa-
AI+ AI- BI+ BI- CI+ CI- DI+ DI-
SEL
GND GNDPAD
ASM1480/TQFN42/[10TA1-081480-10R_10TA1-084083-10R]

From PM SATAE
<14> PM_SATAE_RXN0 PM_SATAE_RXP0
<14> PM_SATAE_TXN0 PM_SATAE_TXP0
<14> PM_SATAE_RXP1 PM_SATAE_RXN1
<14> PM_SATAE_TXN1 PM_SATAE_TXP1

M2_PCIE_IN17_SW M2_PCIE_IP17_SW
M2_PCIE_TN17_SW M2_PCIE_TP17_SW
M2_PCIE_IP18_SW M2_PCIE_IN18_SW
M2_PCIE_TN18_SW M2_PCIE_TP18_SW

To M.2B PCIE Mode

SATAE_RXN0 <14> SATAE_RXP0 <14>
SATAE_TXN0 <14> SATAE_TXP0 <14>
SATAE_RXP1 <14> SATAE_RXN1 <14>
SATAE_TXN1 <14> SATAE_TXP1 <14>

To SATA CONN

M2B_DETECT-

Function	SEL
xI--> xOa	L
xI--> xOb	H

CONNECT TO PCH
BIOS設為main power pull high

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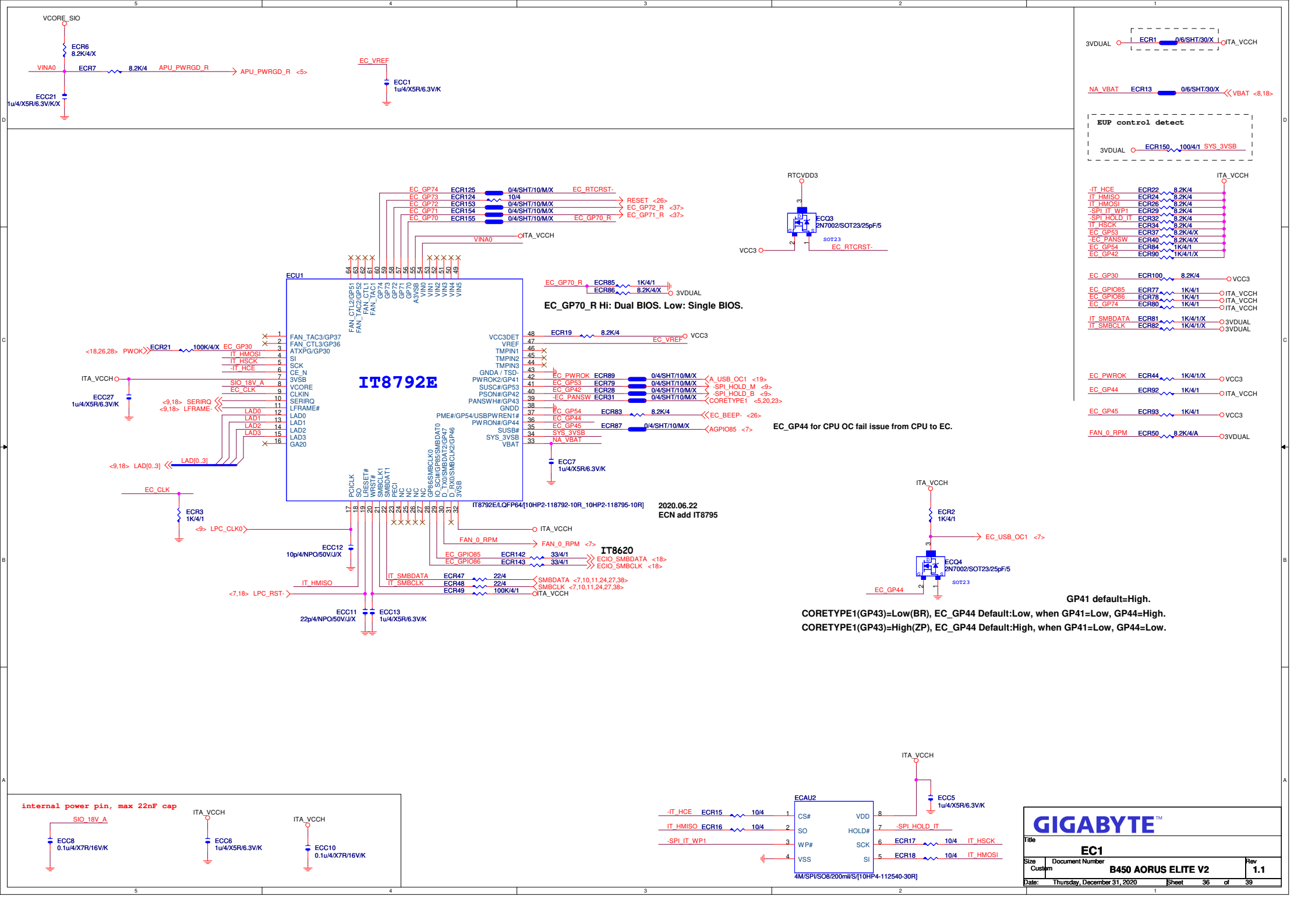
VCORE_SIO
ECR6 8.2K/4/X
VINA0
ECR7 8.2K/4 APU_PWRGD_R
APU_PWRGD_R <5>
ECC21 1u/4/X5R/6.3V/K/X
EC_VREF
ECC1 1u/4/X5R/6.3V/K
3VDUAL
ECR1 0/6/SHT/30/X
ITA_VCCH
NA_VBAT
ECR13 0/6/SHT/30/X
VBAT <8,18>
EUP control detect
3VDUAL
ECR150 100/4/1 SYS_3VSB
RTCVDD3
ECQ3 2N7002/SOT23/25pF/5
SOT23
VCC3
EC_RTCRST-
EC_GP74 ECR125 0/4/SHT/10/M/X EC_RTCRST-
EC_GP73 ECR124 10/4 RESET <26>
EC_GP72 ECR153 0/4/SHT/10/M/X EC_GP72_R <37>
EC_GP71 ECR154 0/4/SHT/10/M/X EC_GP71_R <37>
EC_GP70 ECR155 0/4/SHT/10/M/X EC_GP70_R
VINA0
ITA_VCCH
ECU1
IT8792E
EC_GP70_R ECR85 1K/4/1
ECR86 8.2K/4/X 3VDUAL
EC_GP70_R Hi: Dual BIOS. Low: Single BIOS.
<18,26,28> PWOK ECR21 100K/4/X EC_GP30
IT_HMOSI
IT_HSCK
-IT_HCE
SIO_18V_A
EC_CLK
<9,18> SERIRQ
<9,18> LFRAME-
LAD0
LAD1
LAD2
LAD3
<9,18> LAD[0..3]
LAD[0..3]
ECC27 1u/4/X5R/6.3V/K
ECR19 8.2K/4
EC_VREF
VCC3
EC_PWROK ECR89 0/4/SHT/10/M/X A_USB_OC1 <19>
EC_GP53 ECR79 0/4/SHT/10/M/X -SPI_HOLD_M <9>
EC_GP42 ECR28 0/4/SHT/10/M/X -SPI_HOLD_B <9>
-EC_PANSW ECR31 0/4/SHT/10/M/X CORETYPE1 <5,20,23>
EC_GP54 ECR83 8.2K/4 EC_BEEP- <26>
EC_GP45 ECR87 0/4/SHT/10/M/X AGPIO85 <7>
SYS_3VSB
NA_VBAT
ECC7 1u/4/X5R/6.3V/K
EC_GP44 for CPU OC fail issue from CPU to EC.
IT8792E/LQFP64/[10HP2-118792-10R_10HP2-118795-10R]
2020.06.22
ECN add IT8795
EC_CLK
ECR3 1K/4/1
<9> LPC_CLK0
ECC12 10p/4/NPO/50V/J/X
ITA_VCCH
FAN_0_RPM
FAN_0_RPM <7>
IT8620
EC_GPIO85 ECR142 33/4/1 ECIO_SMBDATA <18>
EC_GPIO86 ECR143 33/4/1 ECIO_SMBCLK <18>
IT_SMBDATA ECR47 22/4 SMBDATA <7,10,11,24,27,38>
IT_SMBCLK ECR48 22/4 SMBCLK <7,10,11,24,27,38>
ECR49 100K/4/1
IT_HMISO
<7,18> LPC_RST-
ECC11 22p/4/NPO/50V/J/X
ECC13 1u/4/X5R/6.3V/K
-IT_HCE ECR22 8.2K/4
IT_HMISO ECR24 8.2K/4
IT_HMOSI ECR26 8.2K/4
-SPI_IT_WP1 ECR29 8.2K/4
-SPI_HOLD_IT ECR32 8.2K/4
IT_HSCK ECR34 8.2K/4
EC_GP53 ECR37 8.2K/4/X
-EC_PANSW ECR40 8.2K/4/X
EC_GP54 ECR84 1K/4/1
EC_GP42 ECR90 1K/4/1/X
EC_GP30 ECR100 8.2K/4 VCC3
EC_GPIO85 ECR77 1K/4/1 ITA_VCCH
EC_GPIO86 ECR78 1K/4/1 ITA_VCCH
EC_GP74 ECR80 1K/4/1 ITA_VCCH
IT_SMBDATA ECR81 1K/4/1/X 3VDUAL
IT_SMBCLK ECR82 1K/4/1/X 3VDUAL
EC_PWROK ECR44 1K/4/1/X VCC3
EC_GP44 ECR92 1K/4/1 ITA_VCCH
EC_GP45 ECR93 1K/4/1 VCC3
FAN_0_RPM ECR50 8.2K/4/A 3VDUAL
ECR2 1K/4/1
EC_USB_OC1 <7>
ECQ4 2N7002/SOT23/25pF/5
SOT23
EC_GP44
GP41 default=High.
CORETYPE1(GP43)=Low(BR), EC_GP44 Default:Low, when GP41=Low, GP44=High.
CORETYPE1(GP43)=High(ZP), EC_GP44 Default:High, when GP41=Low, GP44=Low.
internal power pin, max 22nF cap
SIO_18V_A
ECC8 0.1u/4/X7R/16V/K
ITA_VCCH
ECC6 1u/4/X5R/6.3V/K
ITA_VCCH
ECC10 0.1u/4/X7R/16V/K
ECAU2
-IT_HCE ECR15 10/4
IT_HMISO ECR16 10/4
-SPI_IT_WP1
CS#
SO
WP#
VSS
VDD
HOLD#
SCK
SI
-SPI_HOLD_IT
ECR17 10/4 IT_HSCK
ECR18 10/4 IT_HMOSI
ECC5 1u/4/X5R/6.3V/K
4M/SPI/SO8/200mil/S/[10HP4-112540-30R]
GIGABYTE
Title
EC1
Size Custom
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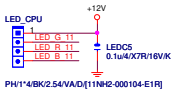
Rev 2.05

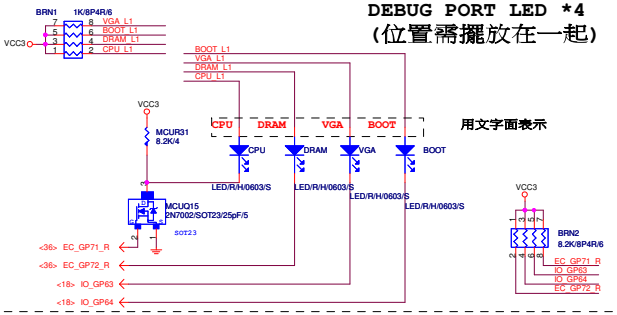
第一區 LED

FOR CPU 正發光 LED*4
(在CPU CHOKE之間,MOS_HS下方,不外露)

AMD CPU_FAN LED connector



DEBUG PORT LED *4
(位置需擺放在一起)



EC_GP71	CPU DEBUG
EC_GP72	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEVICE DEBUG
PM_GPIO6	software beat mode control
N_GPP_A22	
N_GPP_D12	

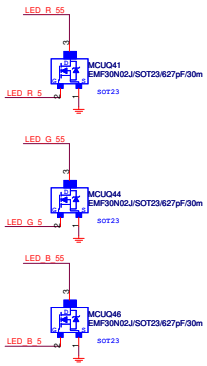
第二區 LED

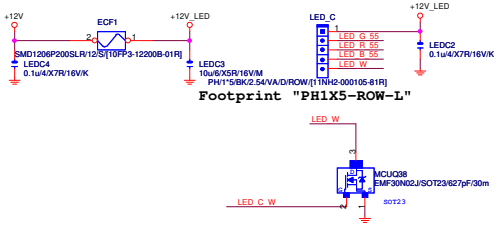
FOR DIMM 側發光 LED*12
(位置在DIMM兩側)

第五區 LED

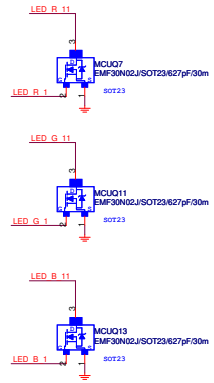
燈條 LED (LED_C1放在PCB左邊板邊位置)

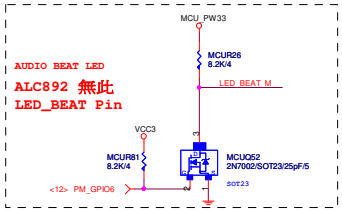
第五區 LED CONTROL

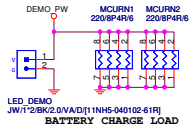


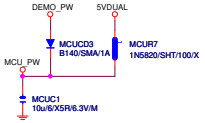


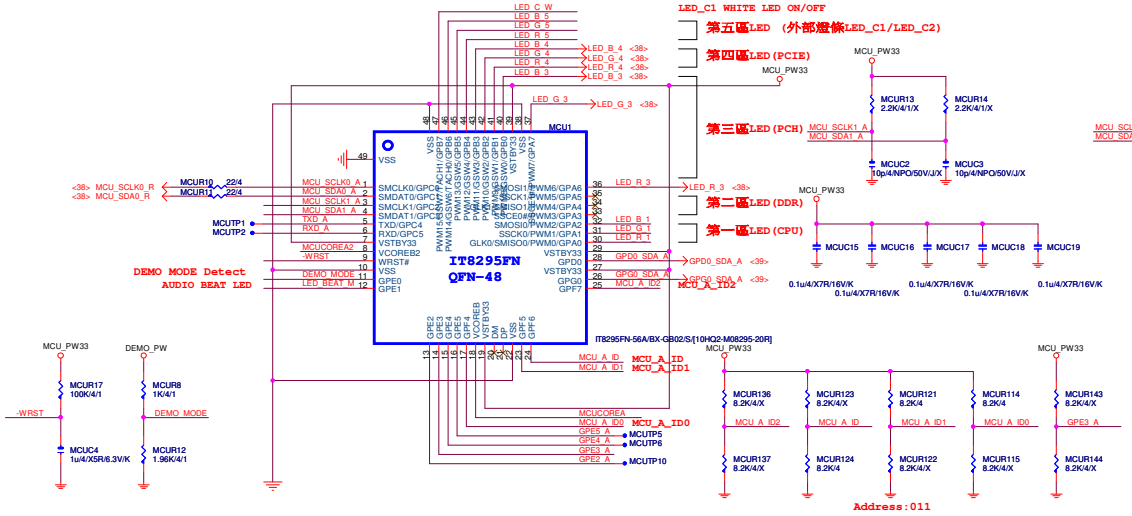
第一區 LED CONTROL











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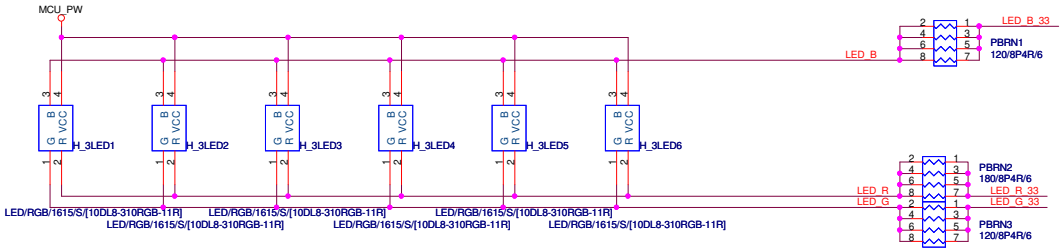
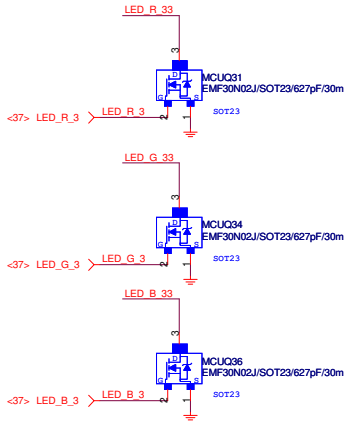
第三區 LED

FOR PCH 正發光 LED*6 (位置在正板,依據PCH_HS設計擺放)



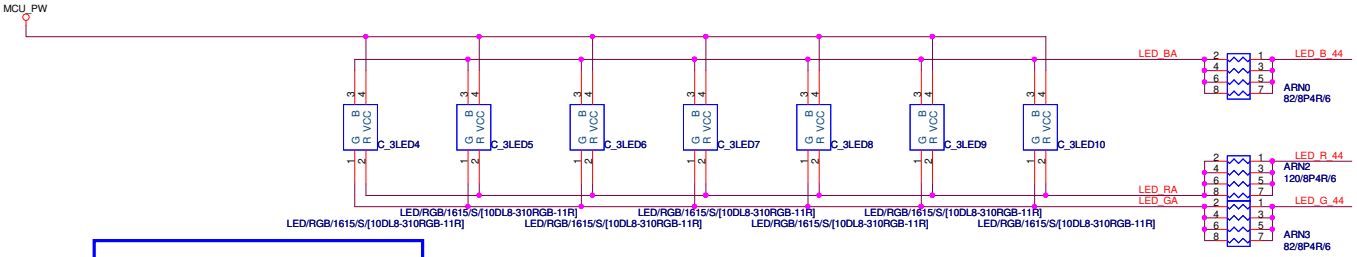
FOOTPRINT:LED-4P-RGB

第三區 LED CONTROL



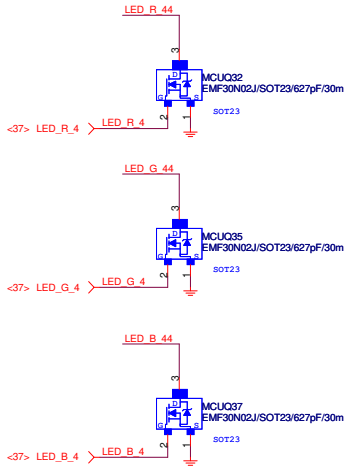
第四區 LED

FOR AUDIO 正發光 LED*10 C_3LED1~10)

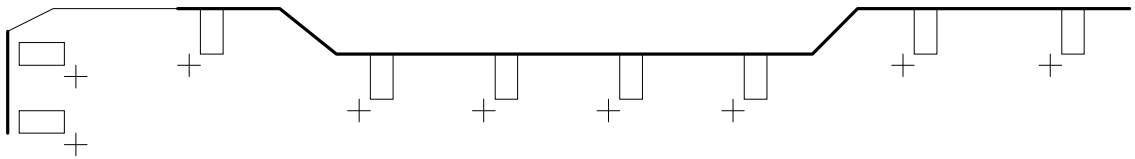


FOOTPRINT:LED-4P-RGB

第四區 LED CONTROL



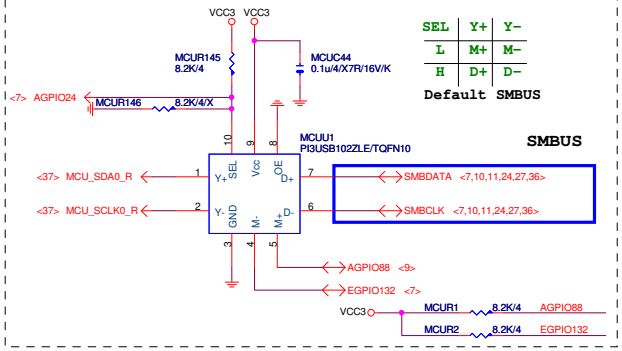
Audio Ground切割線+背面 RGB LED



RGB LED LAYOUT 注意事項 :

1. **Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)**
2. **背板 RGB LED 方向整板請統一如下**
   (整板正極可統一朝下或朝上)
3. **正板 RGB LED 統一方向即可**
4. **MCU_PW & MCU_PW33電源一律走20mils**
5. **ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗**
6. **MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1 .....**
7. **LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11,LED_W.....**
   (包含從晶體到排阻到LED的net)
8. **Digital LED NET rule W/S=4/8 mils**
   GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC

For AMD MCU update



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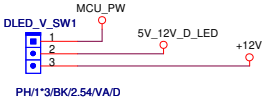
第六區 LED （靠近左上板邊位置）

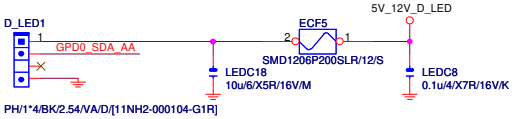


PH/1*3/BK/2.54/VA/D

DLED_V_SW1	
1-2	5V
2-3	12V

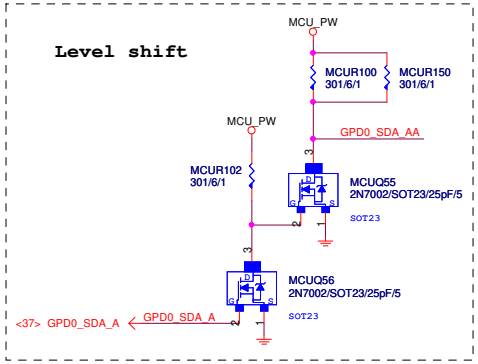
JP/1*2/BK/H/2.54/C/GF/[11NH1-000102-V1R]:[1-2]CLOSE

Digital LED Strip1

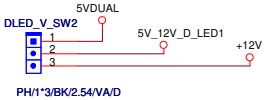


PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint "PH1X4-CUT3-LED-L"



第七區 LED （靠近右下DDR板邊位置）

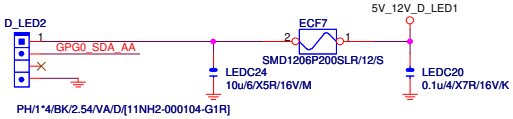


PH/1*3/BK/2.54/VA/D

DLED_V_SW2	
1-2	5V
2-3	12V

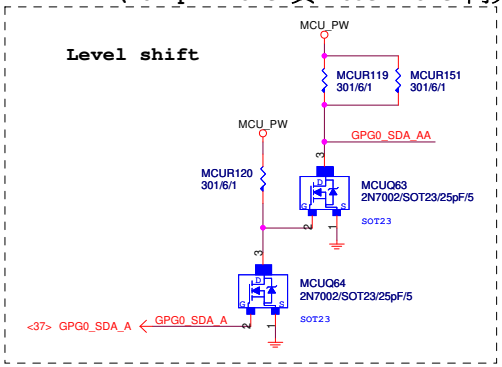
JP/1*2/BK/H/2.54/C/GF/[11NH1-000102-V1R]:[1-2]CLOSE

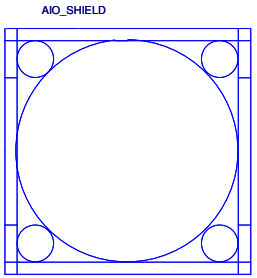
Digital LED Strip2



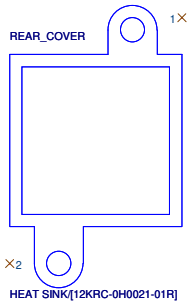
PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint "PH1X4-CUT3-LED-L"
(for pin-name 與 model-name 同方向)





IO SH/SUS 430/t=0.2mm AJOHO/[11AIO-0C0013-12R]



HEAT SINK/[12KRC-0H0021-01R]

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