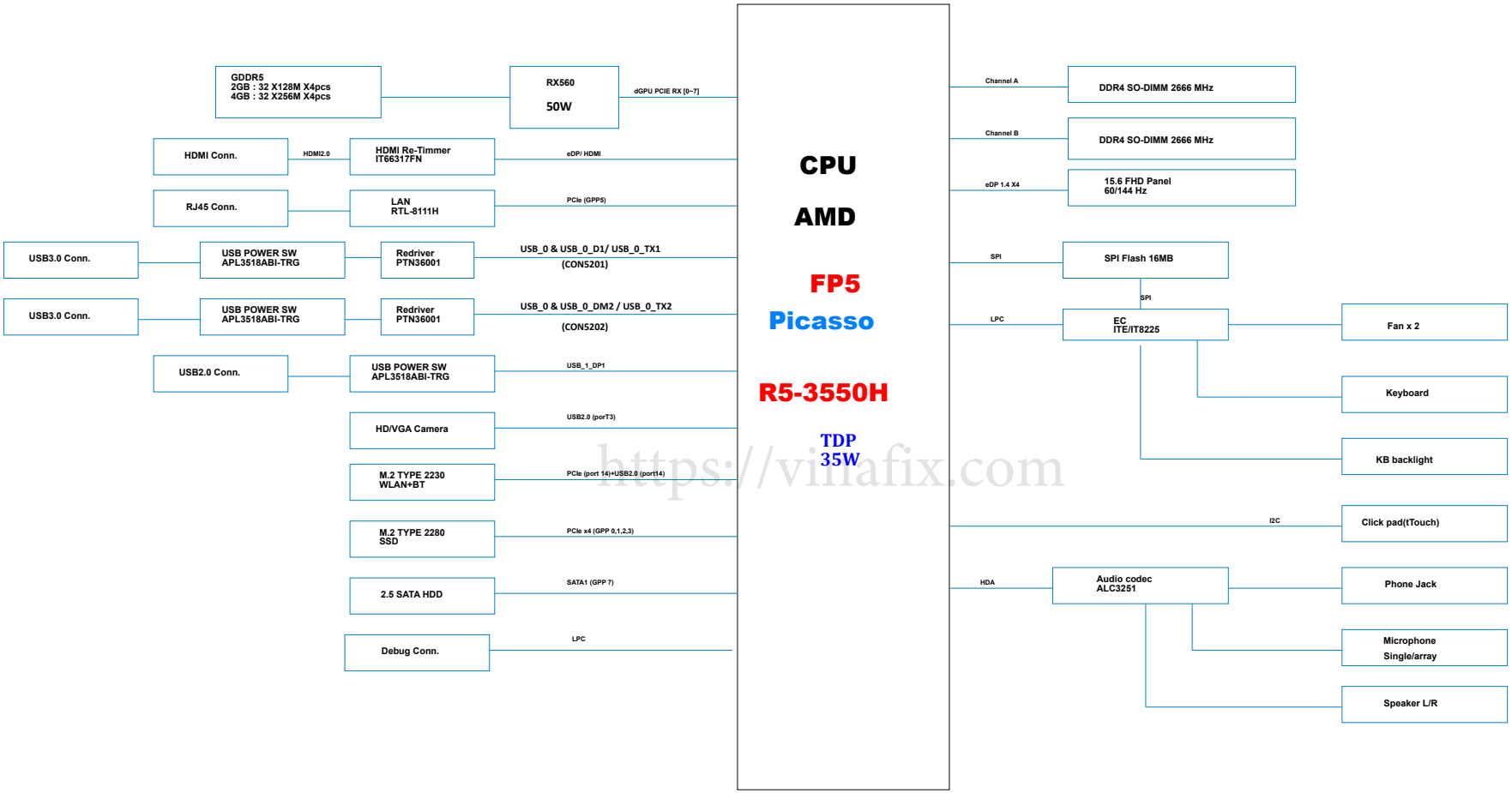
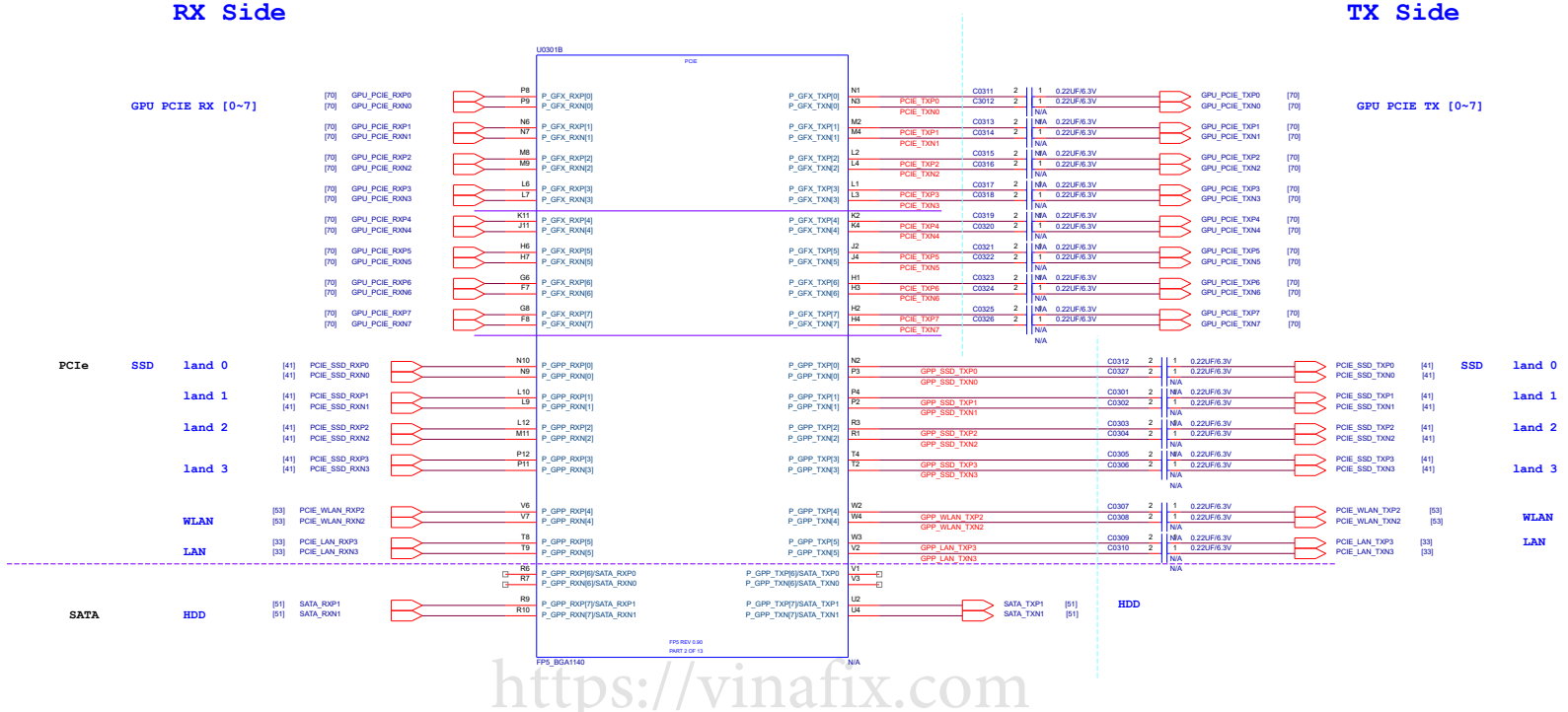
FX505DY AMD Block Diagram

before PR3: PICASSO R5 3500H
After PR3: PICASSO R5 3550H



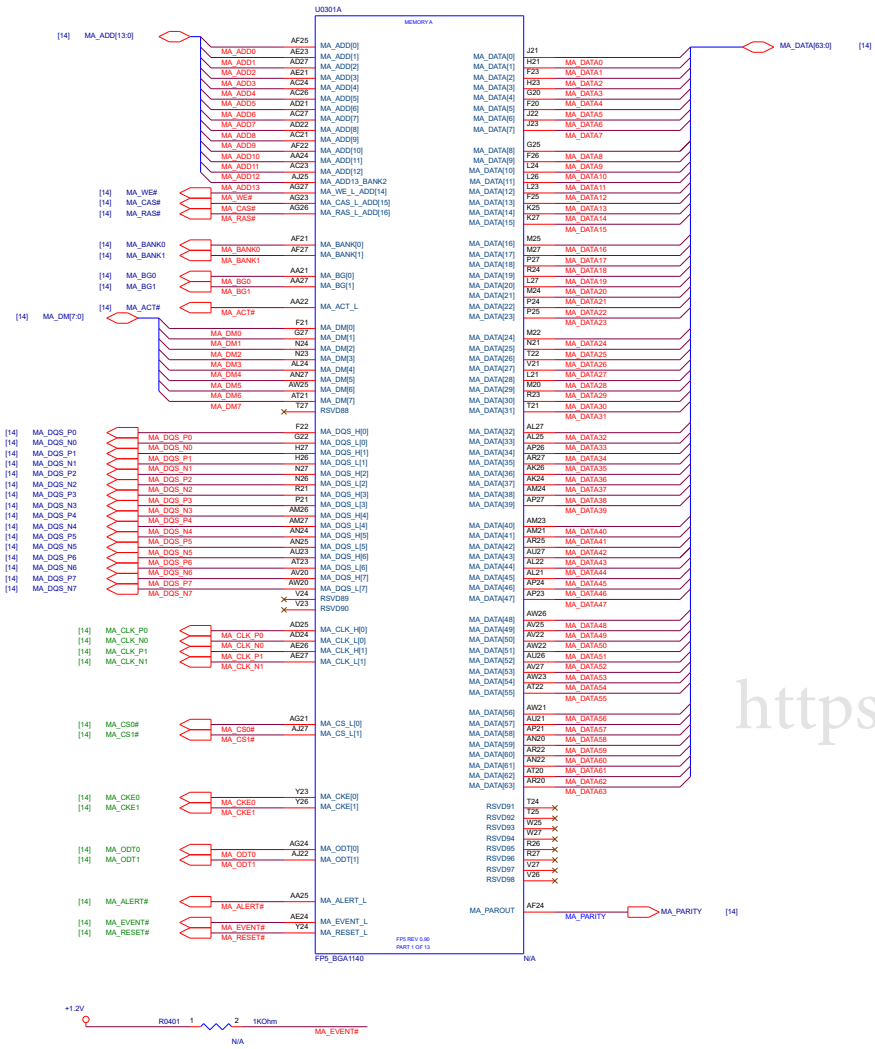
ASUS	Project Name: FX505DY		Rev: R1.4
Title :	AMD Block Diagram_R1.4		
Size: Custom	Doc# :	Engineer:	NB1 RD2 EE1
Date: Thursday, November 29, 2018	Sheet	of	

PCIE/WLAN/LAN/SSD

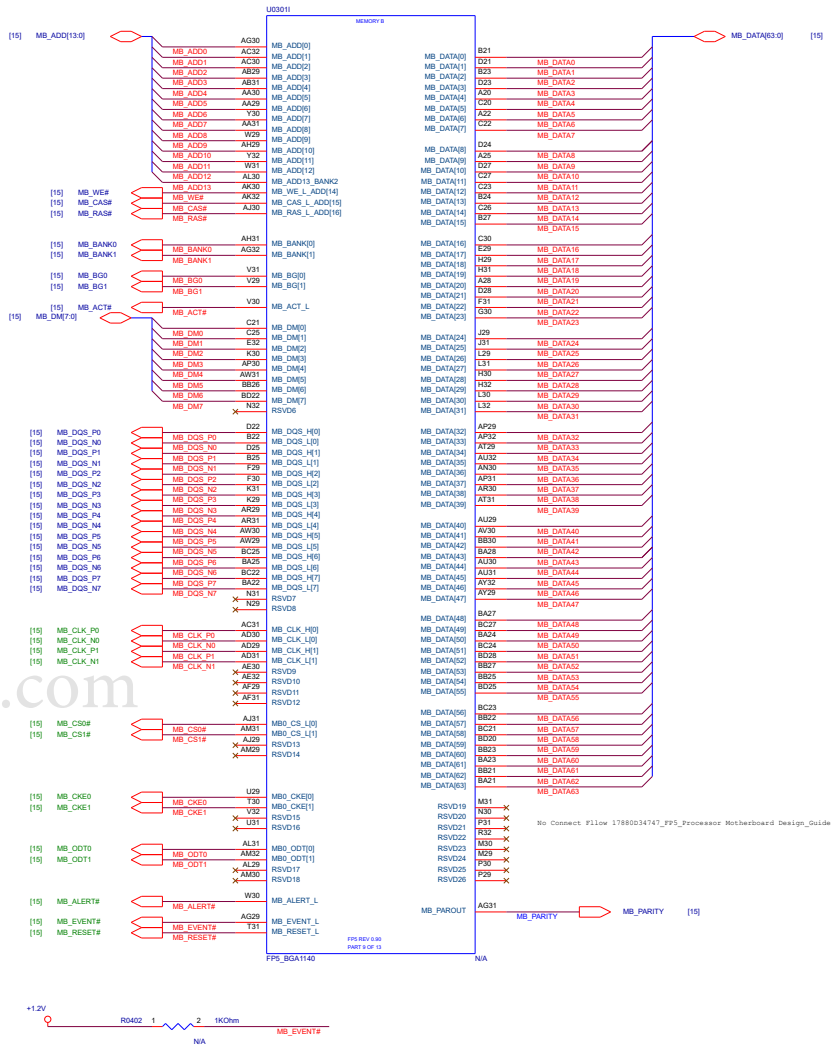


Project Name: FX505DY			Rev: R1.0
Title: CFL-H_CPU_DMI,PEG,FDI,eDP,DDI_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Thursday, November 29, 2018	Sheet 3 of 103		

Memory Channel A



Memory Channel B

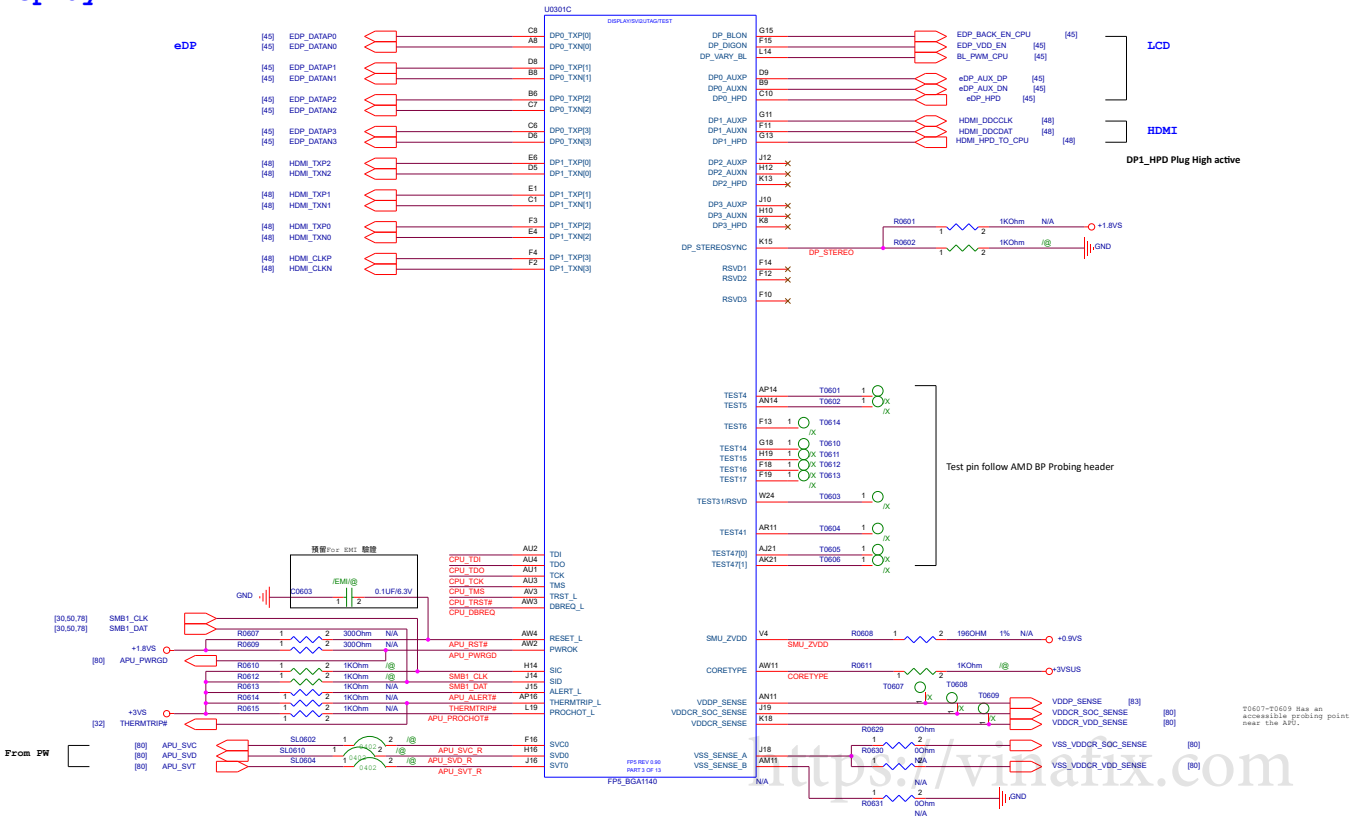


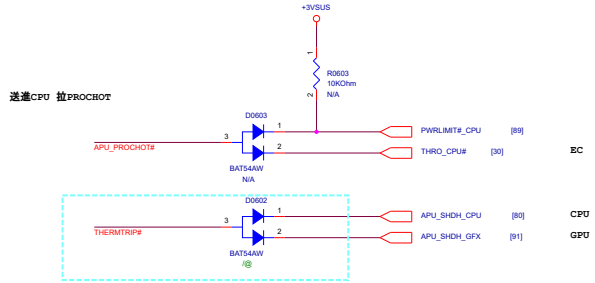
Main Board

拉線OK，有幾Pin訊號待確認是否會使用到

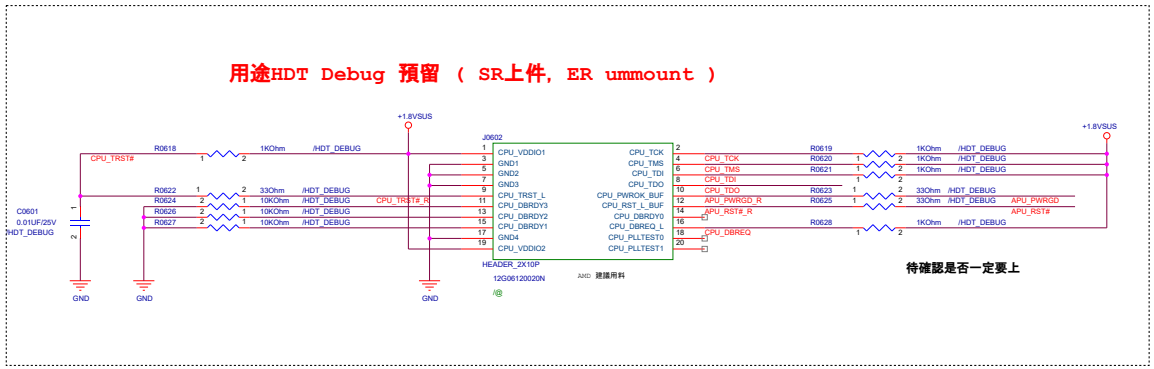
ASUS	Project Name: FX505DY		Rev: R1.0
Title : AMD_CPU_DDR4			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD EE	
Date: Thursday, November 29, 2018	Sheet 4 of 103		

Display





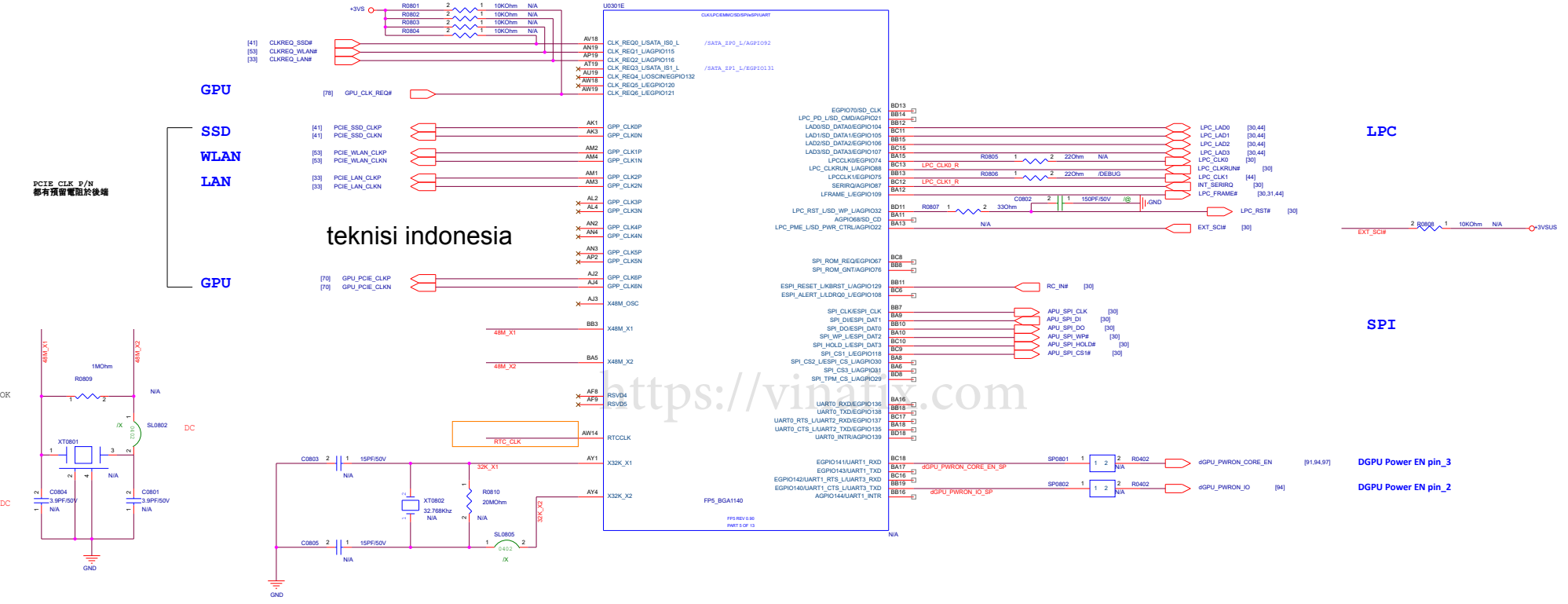
PR modify 1031B_Change D0602.3 APU_PROCHOT# to THERMTRIP# @PY

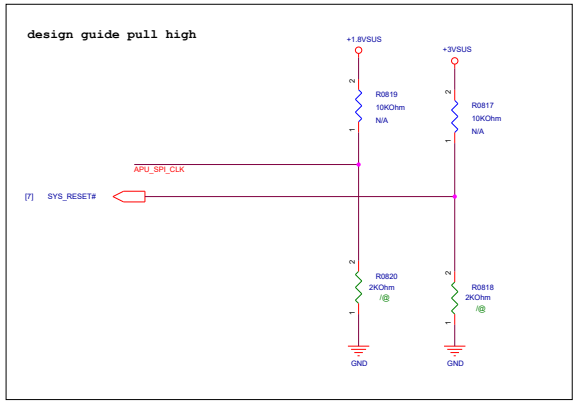


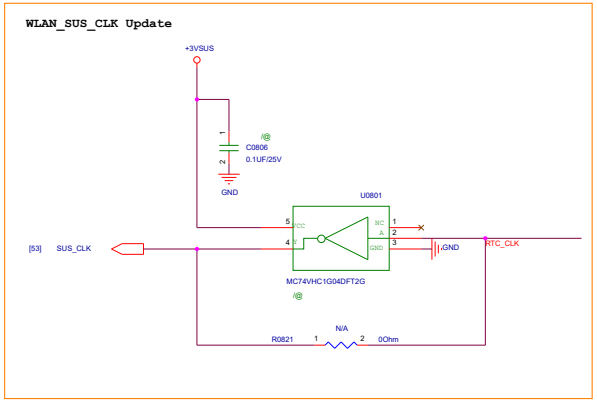
<variant_name>

Project Name: FX505DY		Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Thursday, November 29, 2018	Sheet 6 of 103	

CPU CLK







<variant_name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Thursday, November 29, 2018	Sheet 8 of 103	

I2C/RST/GPIO/AZ

EGPIO27: internal pull down by software.

PR modify 1106A Change NI

PR modify 1031B Change DNI

U0301D

ACPI/AUDIO/I2C/GPIO/MISC

FP5 REV 0.90
PART 4 OF 13

FP5_BGA1140

DDR4_SPD_CLK/DATA

DDR4

Tocuh pad

EXT_SMI# => EC發給CPU

AMD Suggest

Audio

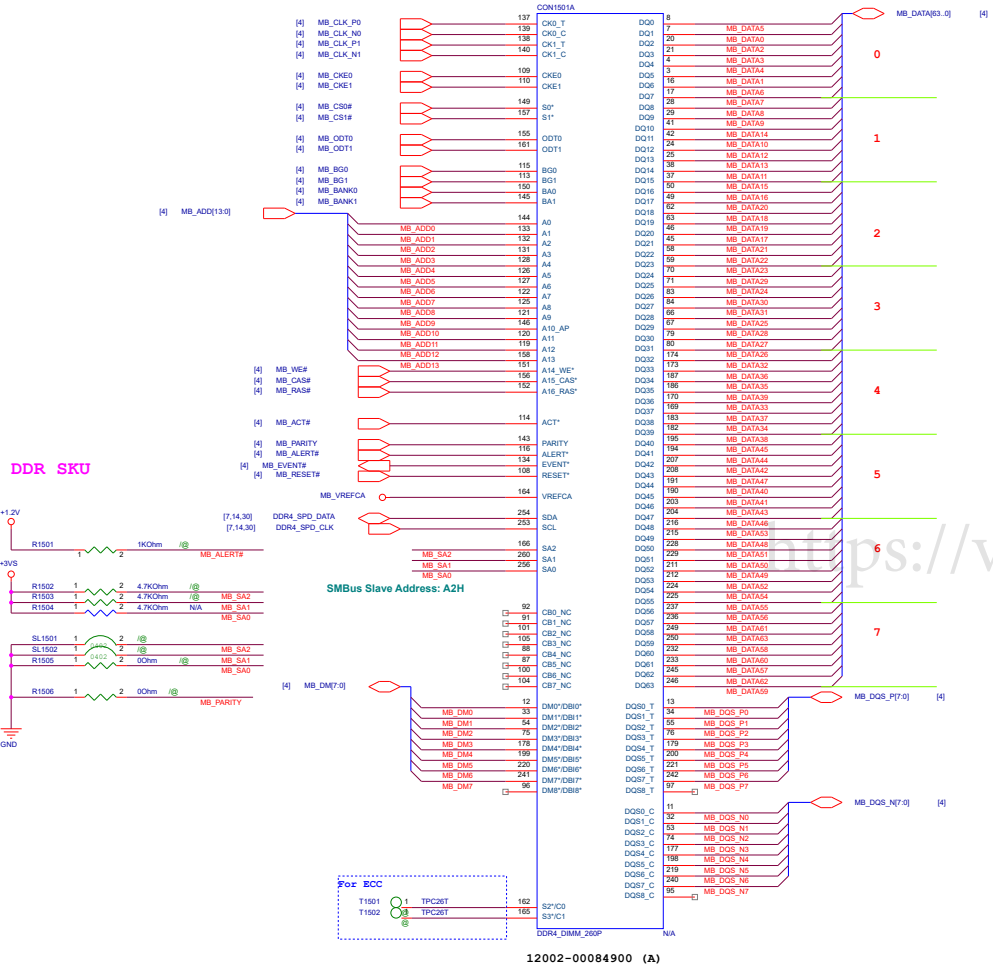
DGPU

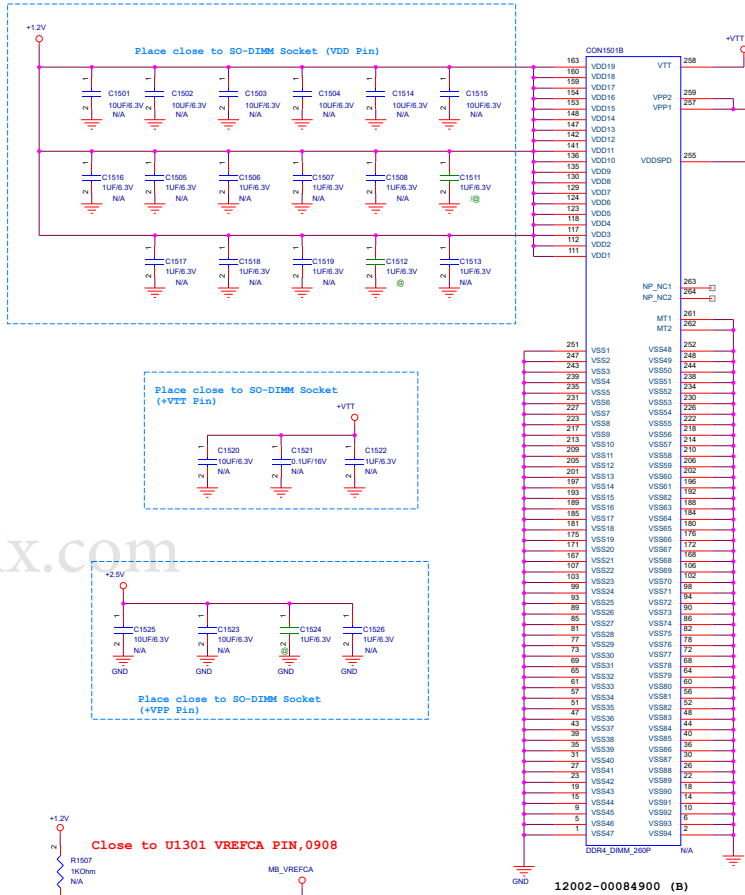
DGPU Power EN pin_1

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: B	Dept.: NB-SZ-RD3	Engineer:
Date: Thursday, November 29, 2018	Sheet 7 of 103	

DDR4 SO-DIMM B rev 12002-00084900 5.2H STD

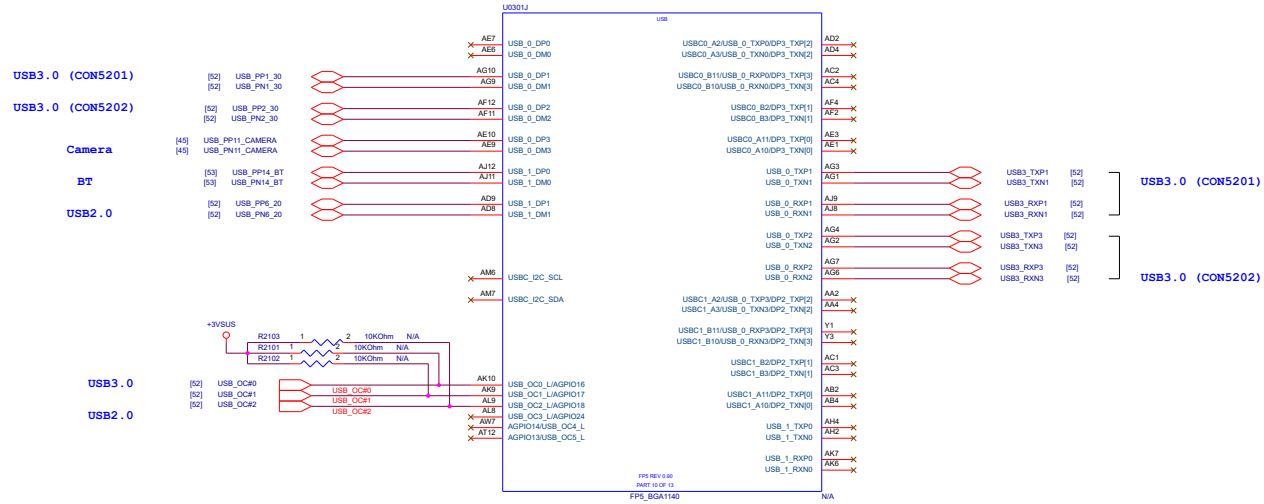




Vinafix.com

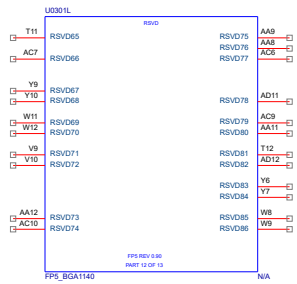
ASUSTeK COMPUTER INC. NB1	Title :	DDR4 SO-DIMM_B	
	Engineer:	EE	
Size: C	Project Name: FX505DY		Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 15 of 103		

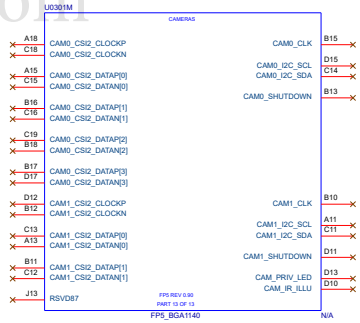
CPU_USB



AMD Design check

AGPIO13. If unused, enable internal pull down by software.

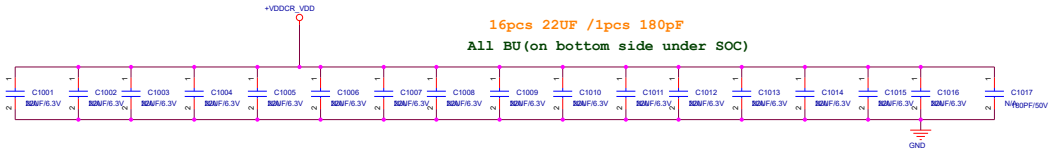


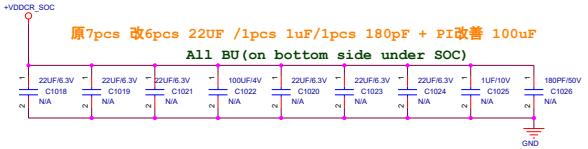


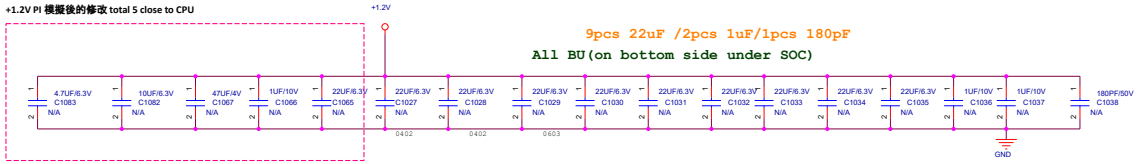
<Variant Name>

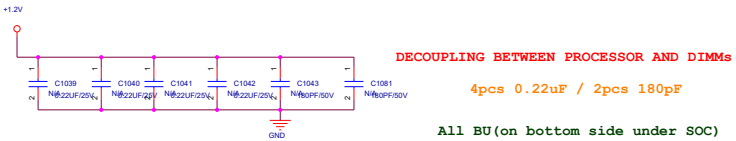
ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Thursday, November 29, 2018	Sheet 21 of 103	

CPU_CAP

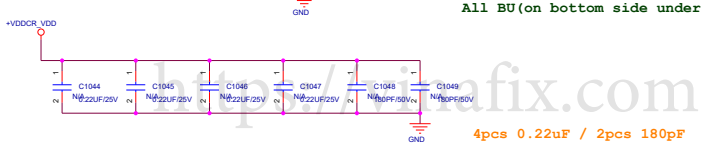






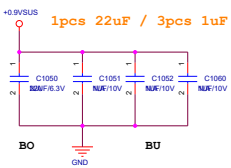


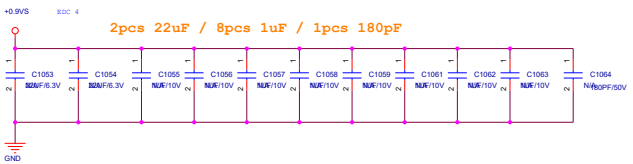
If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

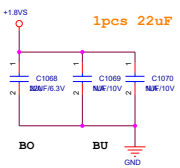


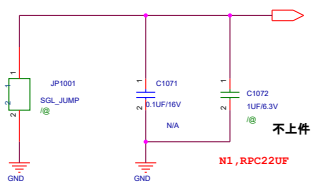
DECOUPLING BETWEEN PROCESSOR AND DIMMs ACROSS VDDIO AND VSS SPLIT

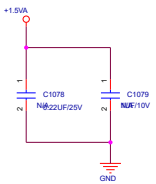
POWER RAIL			
CPU	CPU_FP5	FX505ZD	CRB線路
Power rail	VDDCR_SOC	+VDDCR_SOC	+APU_VDDSOC_RUN
	VDDIO_MEM_S3	+1.2V	+APU_VDDIO_SUS
	VDDIO_AUDIO	+1.8VS	+VDD_AUD_ALW
	VDD_33	+3VS	+3.3V_RUN
	VDD_18	+1.8VS	+1.8V_RUN
	VDD_18_S5	+1.8VSUS	+1.8V_ALW
	VDD_33_S5	+3VSUS	+3.3V_ALW
	VDDP_S5	+0.9VSUS	+VDDP_ALW
	VDDP	+0.9VS	+VDDP_RUN
	VDDBT_RTC	+1.5VA	+VDDBT_RTC
	VDDCR	+VDDCR_VDD	+APU_VDDCORE_RUN



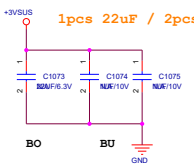


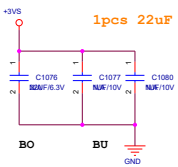






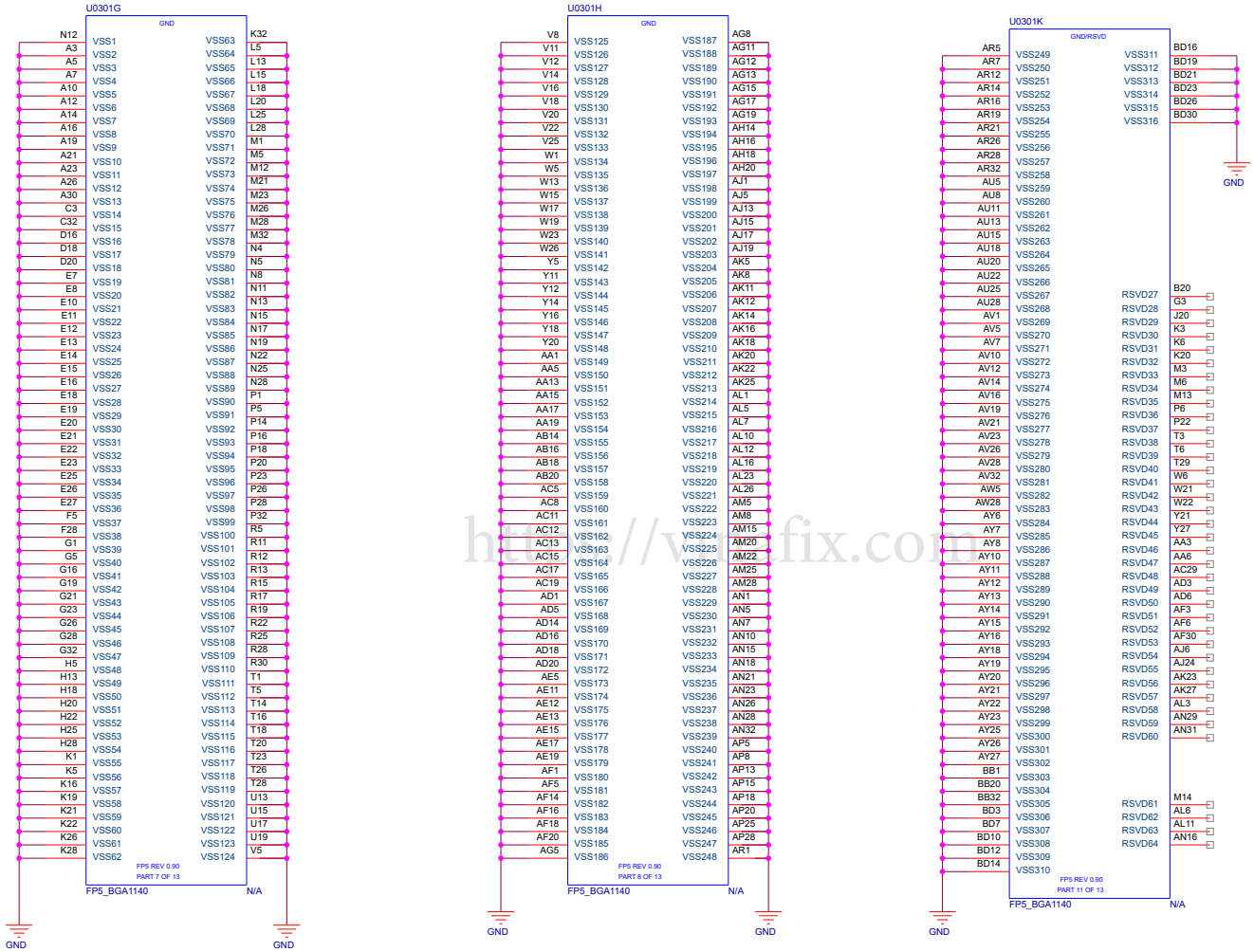
1pcs 0.22uF / 1pcs 1uF





ASUS	Project Name: FX505DY		Rev: R1.0
Title : CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Thursday, November 29, 2018	Sheet 10 of 103		

CPU_GND



ASUS	Project Name: FX505DY	Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Thursday, November 29, 2018	Sheet 5 of 103	

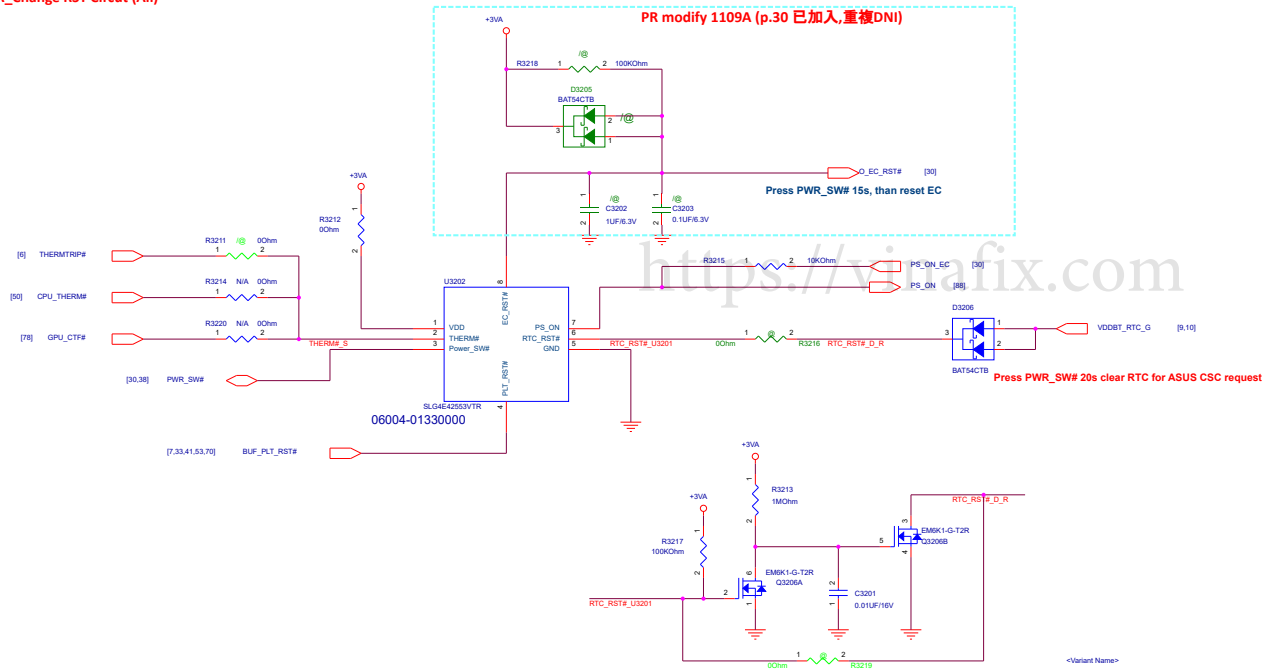
Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

UX362FA R1.3 board will verify this circuit 7/E

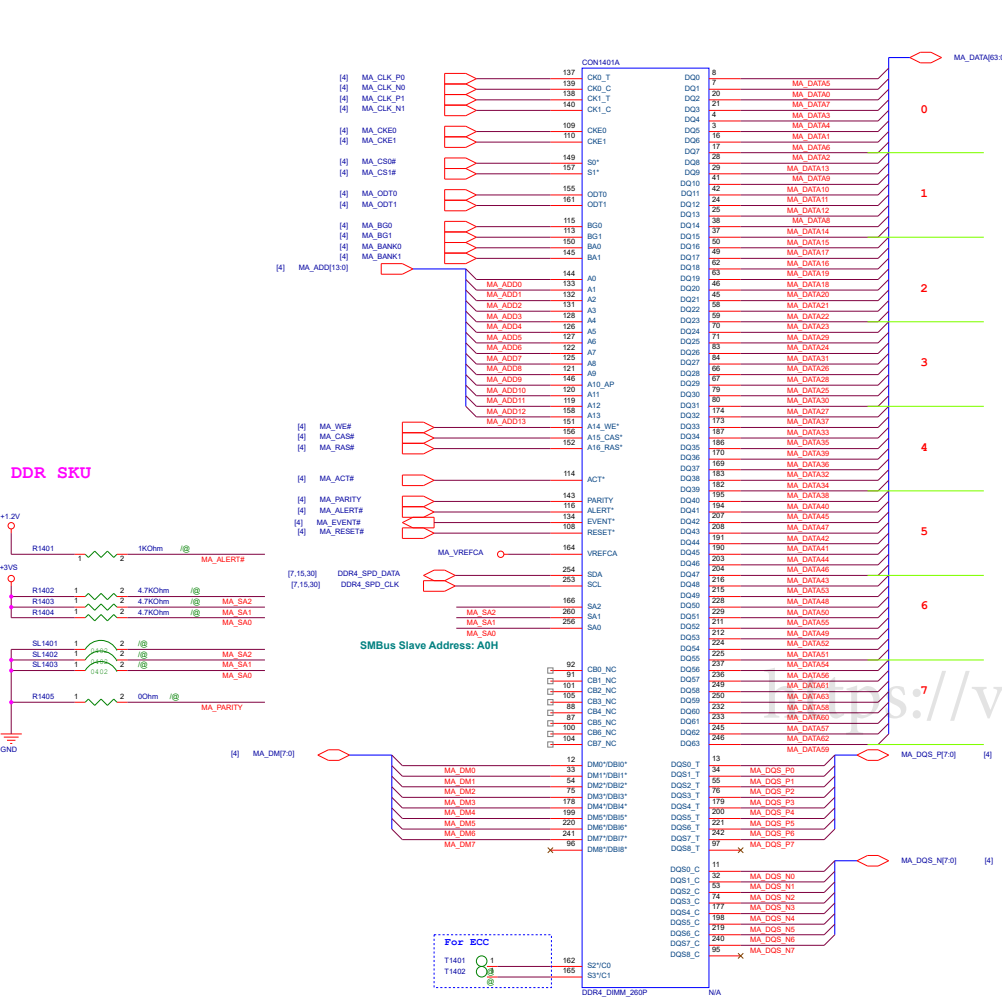
PR modify 1031A_Change RST Circut (All)

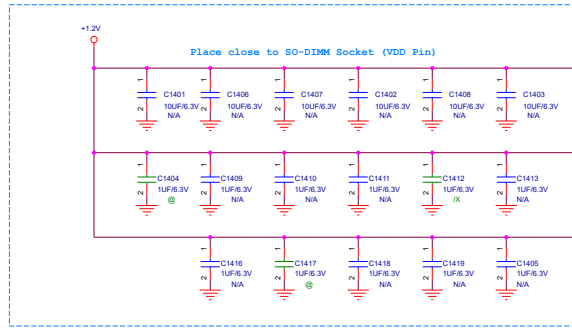


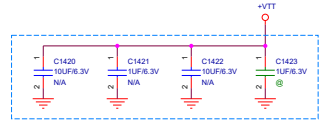
<Variant Name>

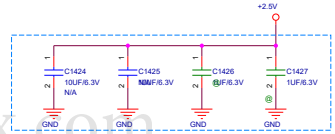
ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: SZNB1	
Size: B	Project Name: FX505DY	Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 32 of 103	

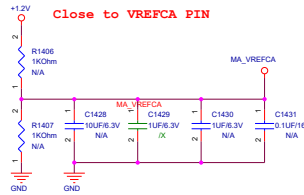
DDR4 SO-DIMM 5.2H REV 12002-00085000

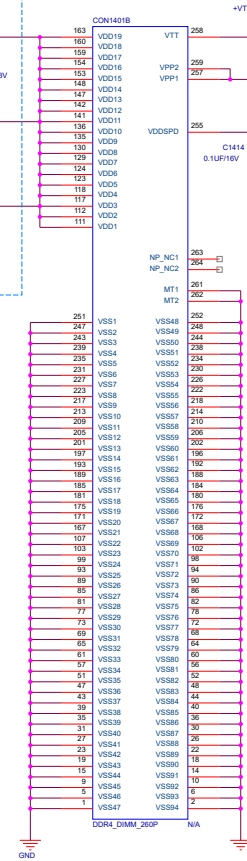




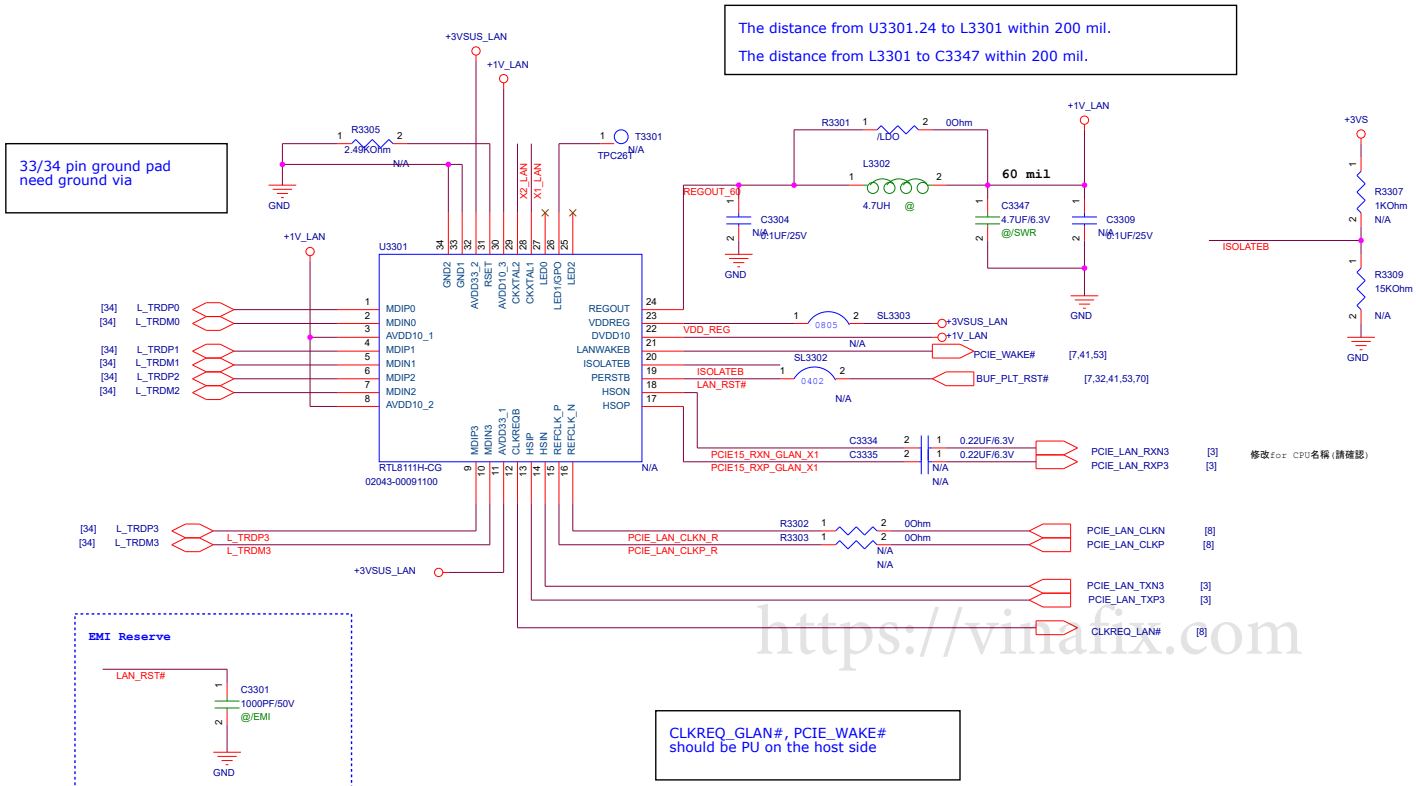


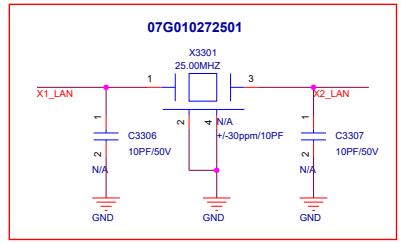






ASUSTeK COMPUTER INC.	Title : DDR4_SO-DIMM-A			
	Engineer: EE			
Size: C	Project Name: FX505DY			Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 14 of 103			



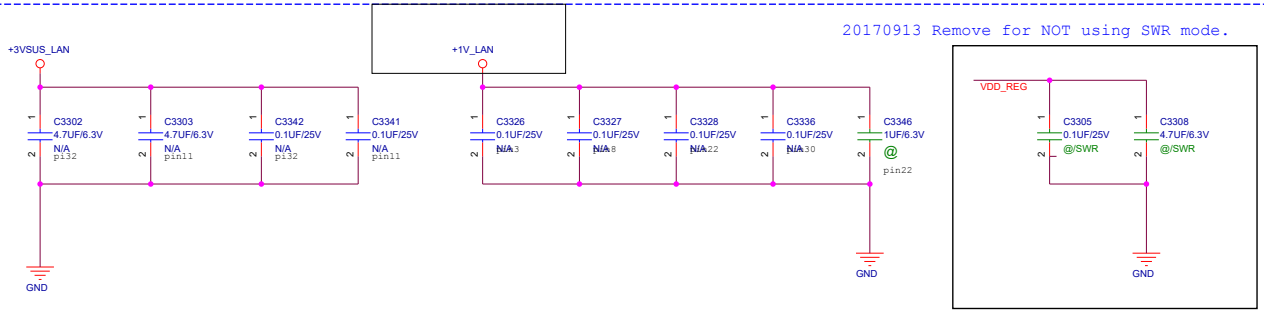


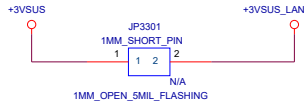
X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

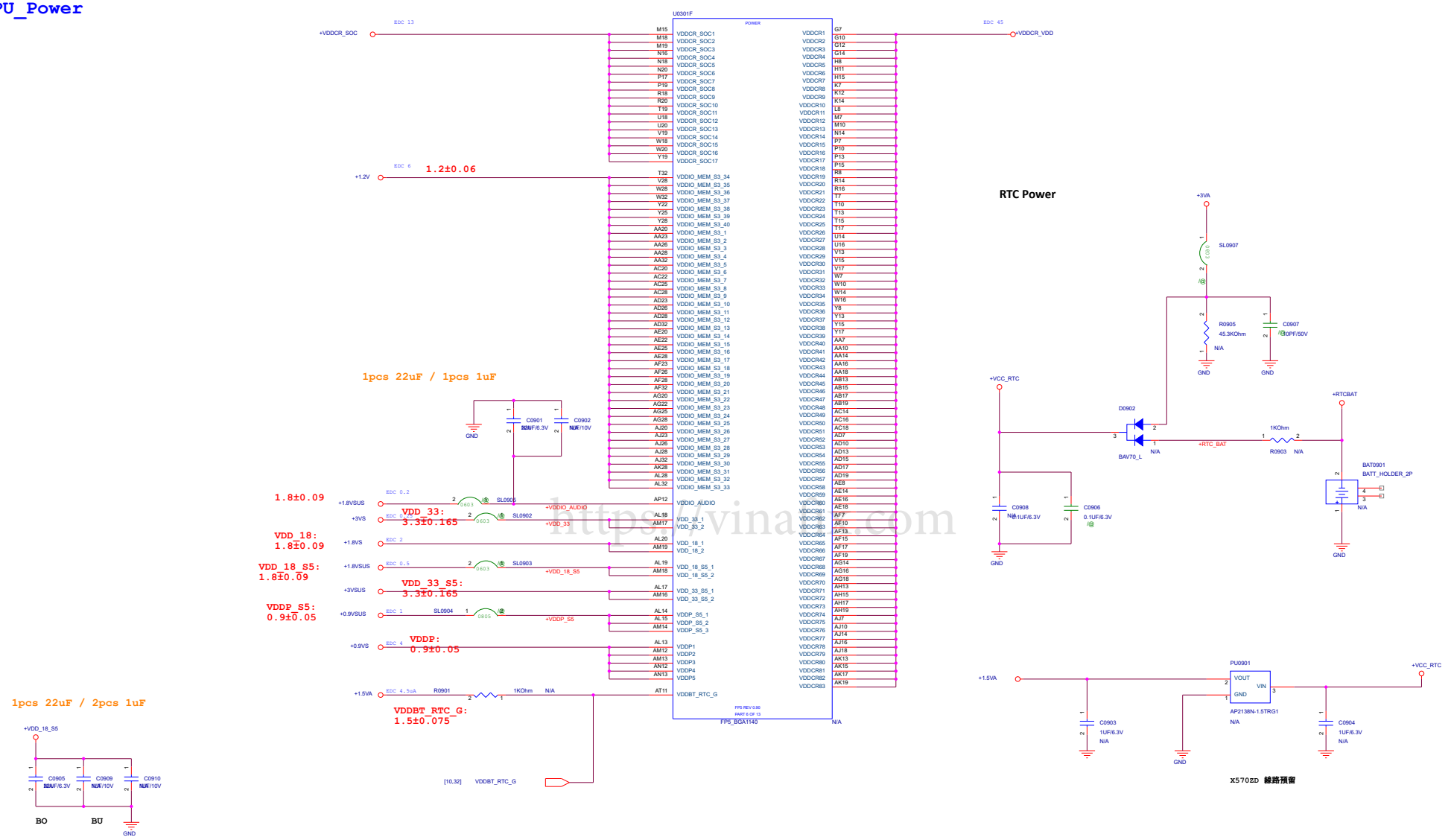
LAN 1V的電? 要確認由誰給的



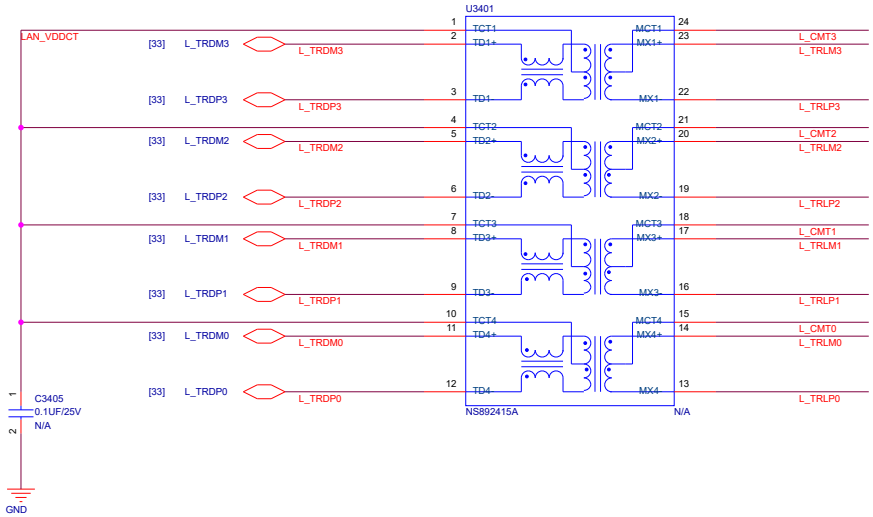


ASUS	Project Name: FX505DY		Rev: R1.0
Title : LAN RTL8111GUX-CG			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Thursday, November 29, 2018		Sheet 33 of 103	

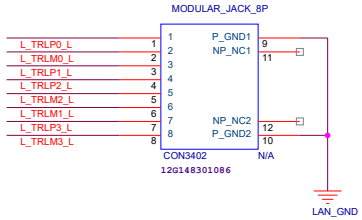
CPU_Power

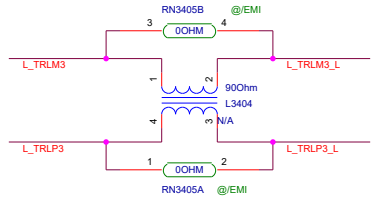


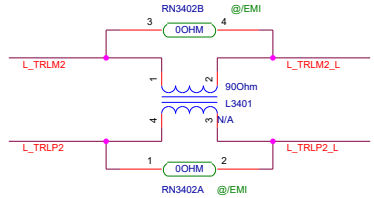
Project Name: FX505DY			Rev: R1.0
Title: CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Thursday, November 29, 2018	Sheet 9 of 103		

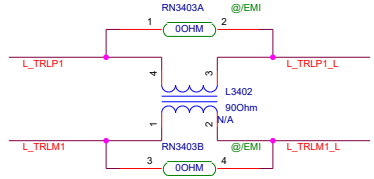


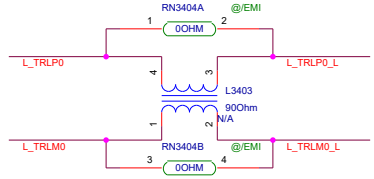
LAN Connector

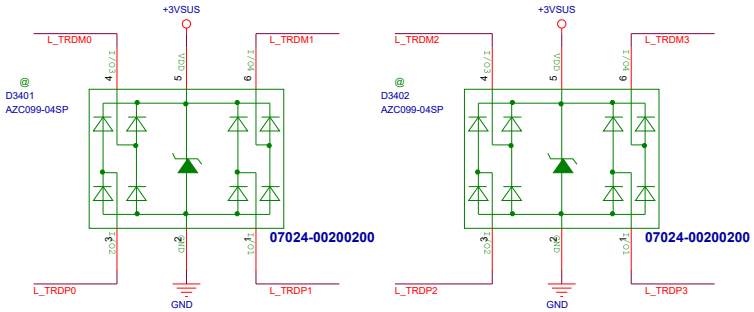








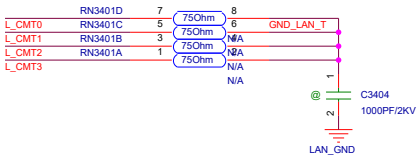




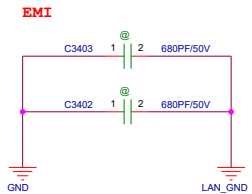
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



GND_LAN_T 上禁止加任何零件



Place near chassis GND

teknisi indonesia

ASUS	Project Name: FX505DY	Rev: R1.0
Title : LAN RJ45 Conn.		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Thursday, November 29, 2018	Sheet 34 of 103	

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	ACIN#	Native	AC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_48CPCI_PCH_R1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_R1			
GPP_A11	PME#	GPO	(N.C)			
GPP_A12	GPI	GPO	(N.C)			
GPP_A13	SUSWARN0#	Native	WL_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	(N.C)			
GPP_A17	GPI	GPO	(N.C)			
GPP_A18	GPI	GPO	(N.C)			
GPP_A19	GPI	GPO	(N.C)			
GPP_A20	GPI	GPO	(N.C)			
GPP_A21	GPI	GPO	TATA_MASSET(Reserved)			
GPP_A22	GPI	GPO	PCH_BTO3_CTO_PWR_EN		PU 10K	+VCC3V3_SX
GPP_A23	GPI	GPO	PCH_BTO3_USB_PWR_EN		PD 100K	

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPI	TBT_I2C_INT_PCH		PU 10K	+3VSUS
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K(@)	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K(@)	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLK_REQ5#/CLKREQ5_TBT #		PU 10K	+3VSUS
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP814	PD		
GPP_B15	GPI	GPI	PCH_GPP815/KB_LANG_ID0		PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPP816/KB_LANG_ID1		PU 10K	+3VS
GPP_B17	GPI	GPO	PCH_GPP817/SMIH_WAKE		PU 10K	
GPP_B18	GPO	Strap	PCH_GPP818	PD		
GPP_B19	GPI	GPO	PCH_GPP819/BT_ON_PCH		PU 10K(@)	
GPP_B20	GPI	GPO	PCH_GPP820/GPIOEVENT# PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP821/GPIOFREN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPP822	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2 BT_UART_WAKE_N	PD	PU 4.7K	+3VSUS
GPP_C3	SMLOCLK	Native	SML0_CLK (Reserved)		PU 2.2K	+3VSUS
GPP_C4	SMLOGATA	Native	SML0_DAT (Reserved)		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	SML1CLK	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	SML1DATA	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	(N.C)			
GPP_C9	GPI	GPO	(N.C)			
GPP_C10	GPI	GPO	(N.C)			
GPP_C11	GPI	GPO	(N.C)			
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NFC_IO		PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS_WU
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPO	(N.C)			
GPP_D3	GPI	GPO	(N.C)			
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	Native3	PCH_PPVOS/M_2_BT_PCMSYN_CRF_RST_N		PD 75K	
GPP_D6	GPI	Native3	PCH_PPVOS/M_2_BT_PCMOUT_CLKREQ		PD 75K(@)	
GPP_D7	GPI	GPO	PCH_PPVOS/M_2_BT_PCMIN		PD 100K(@)	
GPP_D8	GPI	GPO	PCH_PPVOS/M_2_BT_PCMCLK			
GPP_D9	GPI	GPO	(N.C)			
GPP_D10	GPI	GPO	(N.C)			
GPP_D11	GPI	GPO	(N.C)			
GPP_D12	GPI	GPO	(N.C)			
GPP_D13	GPI	GPO	(N.C)			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	SATAXPCIE_DET0		PU 10K(@)	+3VS
GPP_E1	GPI	Native	SATAXPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	Native	SATAXPCIE_DET2		PU 10K(@)	+3VS
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPI	Native	SATA0_ADO1 DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_HGPF3_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	HGPF3_DEVSLP		PU 10K(@)	+3VSUS
GPP_E7	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	Native	SATAXPCIE_DET3		PU 10K(@)	+3VS
GPP_F1	GPI	Native	SATAXPCIE_DET4		PU 10K	+3VS
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	(N.C)			
GPP_F6	GPI	GPO	(N.C)			
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPO	(N.C)			
GPP_F20	GPI	GPO	(N.C)			
GPP_F21	GPI	GPO	(N.C)			
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	PCH_GPPF23		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPO	(N.C)			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLK_REQ6#/CLKREQ6_NGFF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#/CLKREQ7_NGFF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#/CLKREQ8_NGFF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K(@)	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K(@)	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K(@)	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K(@)	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K(@)	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K(@)	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K(@)	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD	PD 20K(@)	
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	SML3ALERT#		PU 100K	+3VSUS
GPP_H16	GPI	GPI	HSIO_0			
GPP_H17	GPI	GPI	HSIO_1			
GPP_H18	GPI	GPI	HSIO_2			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	(N.C)			
GPP_I1	GPI	GPO	(N.C)			
GPP_I2	GPI	GPO	(N.C)			
GPP_I3	GPI	GPO	(N.C)			
GPP_I4	GPI	GPO	(N.C)			
GPP_I5	GPI	GPO	(N.C)			
GPP_I6	GPI	GPO	(N.C)			
GPP_I7	GPI	GPO	(N.C)			
GPP_I8	GPI	GPO	(N.C)			
GPP_I9	GPI	GPO	(N.C)			
GPP_I10	GPI	GPO	(N.C)			
GPP_I11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPI	GPO	(N.C)			
GPP_J1	PM_SLP_SUS_GATE#	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPI	GPO	(N.C)			
GPP_J3	GPI	GPO	(N.C)			
GPP_J4	CNV_BRI_DT	Native	CNV_BRI_DT		PU 4.7K	+1.8VSUS
GPP_J5	CNV_BRI_RSP	Native	CNV_BRI_RSP		PU 20K(@)	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		PU 75K	
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J8	GPI	GPO	(N.C)			
GPP_J9	GPO	GPO	(N.C)			
GPP_J10	GPI	GPO	(N.C)			
GPP_J11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPI	GPO	GPIO_3_FORCE_PWR		PU 100K	
GPP_K1	GPI	GPI	PCH_IO1		PU 10K	
GPP_K2	GPI	GPI	PCH_IO1		PU 10K	
GPP_K3	GPI	GPO	GPP_K3/WLAN_BT_LED		PU 100K	
GPP_K4	GPI	GPO	GPP_K4/WLAN_LED		PU 100K	
GPP_K5	GPI	GPO	VOL_DOWN#(N.C)			
GPP_K6	GPI	GPO	VOL_UP#(N.C)			
GPP_K7	GPI	GPO	GPP_K7/TBT_RST#		PU 10K	+3VS
GPP_K8	GPI	GPO	GPP_K8/DGPU_PWR_EN#		PU 10K(@)	+3VS
GPP_K9	GPI	GPO	WLAN_ON#		PD 100K	
GPP_K10	Reserved	GPO	GPP_K10/HDA1_RST#		PU 10K	+3VS
GPP_K11	Reserved	GPO	GPP_K11/SP_MUX#		PU 10K	+3VS
GPP_K12	GPI	GPO	(N.C)			
GPP_K13	GPI	GPO	(N.C)			
GPP_K14	GPI	GPO	(N.C)			
GPP_K15	GPI	GPO	(N.C)			
GPP_K16	GPI	GPO	(N.C)			
GPP_K17	GPI	GPO	(N.C)			
GPP_K18	GPI	GPO	(N.C)			
GPP_K19	GPI	GPO	(N.C)			
GPP_K20	Reserved	GPO	(N.C)			
GPP_K21	Reserved	GPO	(N.C)			
GPP_K22	GPI	GPO	(N.C)			
GPP_K23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_R1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#(N.C)		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A# (N.C)			
GPD7	GPO	GPO	PCH_GPD7		PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN# (N.C)			
GPD10	SLP_S5#	Native	SLP_S5# (N.C)			
GPD11	LANPHYPC	GPO	LAN_PHYEN (N.C)		PU 10K(@)	+3VA_DSW

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	0	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	0	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	0	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	0	GPO	EC_GPB5/KBKey_WAIT	PU 10K	
GPB6	OD	GPO	EC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	0	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	0	GPO	PM_PWRBTN#	PU 10K(@)	+3VSUS
GPC4	I	GPI	EC_GPC4/PM_SUS3#	PU 100K	
GPC5	I	GPI	PM_SUS3#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	0	GPO	EC_GPC7/NKEY_PWR_EN	PU 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPO	EC_GPD0/EC_CV_DSR		
GPD1	0	GPO	EC_GPD1/MB_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	0	GPO	EC_GPD5/GP_SD#		
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	0	GPO	EC_GPE0/SUSS_EC#	PU 4.7K	
GPE1	0	GPO	EC_GPE1/SUSC_EC#	PU 4.7K	
GPE2	0	GPO	5.2V_ON		
GPE3	0	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	0	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	0	GPO	CAP_LED#		
GPF1	0	GPO	NUM_LED#		
GPF2	Alt	SMBus	P_SMB2_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB2_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PU 10K(@)	
GPF7	0	GPO	PCH_SPI_CS		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	0	GPO	DGPU_LIMIT		
GPG1	0	GPO	PCH_RSTBACK#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	0	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	0	GPO	PM_RSMRST#	PU 10K	
GPH4	0	GPO	DPBRDG_EC	PU 10K	
GPH5	0	GPO	PM_PWROK	PU 10K	
GPH6	I	GPO	PM_SYSPWROK	PU 10K	
GPH7	0	GPO	LED_BACKUP#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#	PU 100K(@)	
GPI1	I	GPI	SYSON_PWRGD	PU 100K	+3VSUS
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	3MOFF_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#	PU 10K(@)	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 150KAD3 470K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	0	GPO	EC_GPJ0		
GPJ1	0	GPI	GC6FBEN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/PBTA_I2C_INT_EC		
GPJ3	0	GPO	EC_GPJ3/USB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_SYNUS		
GPJ5	0	GPI	EC_GPJ5/MB_USON_JACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	NKEY_INT#	PU 10K	+VTR_DSW_NKey/PWR
GPJ7	0	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EI00		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EI01		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EI02		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EI03		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EXCK		CLK_48CPCI_PCH		
GPM5	LFRAME#/EC8#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

G703GI Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
GPU SNT, Thermal sensor	98h, 9Ch
CPU Thermal Sensor	90h
TI, TAS5766M*2	98h, 9Ah
AGM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	76h, 7Ch, 7Ah, 78h, 7Eh

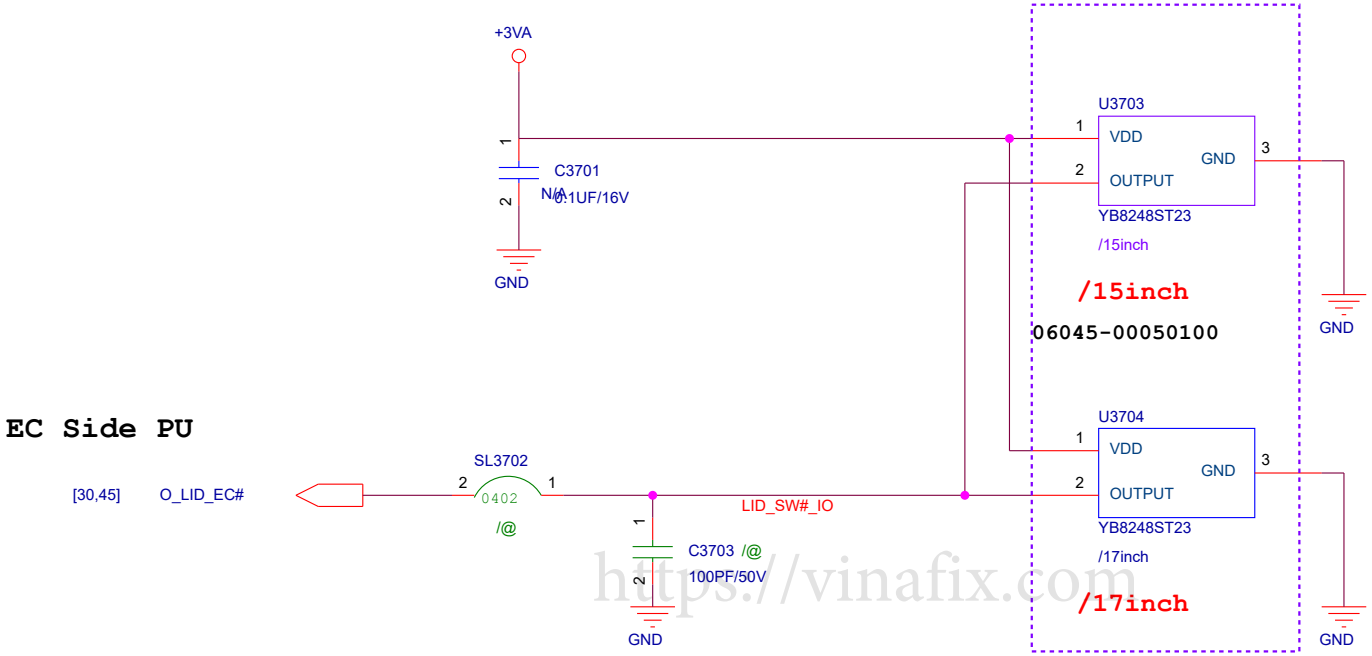
Device Identification

CPU Thermal Sensor			
1st	0000237313019	0077777U	
2nd			

SPU Thermistor			
1st	0000235448020	0781-1	
2nd			

ASUS	Project Name: G703GI		Rev: 00.xx
Title :	CFL-R System Setting_R1.0E		
Size: A3	Document Number:		Rev: 1.0
Date: Thursday, November 08, 2018	Dept.: Mobile COMPUTER BU	Engineer: NB1 RD2 EE1	
		Sheet 2 of 100	

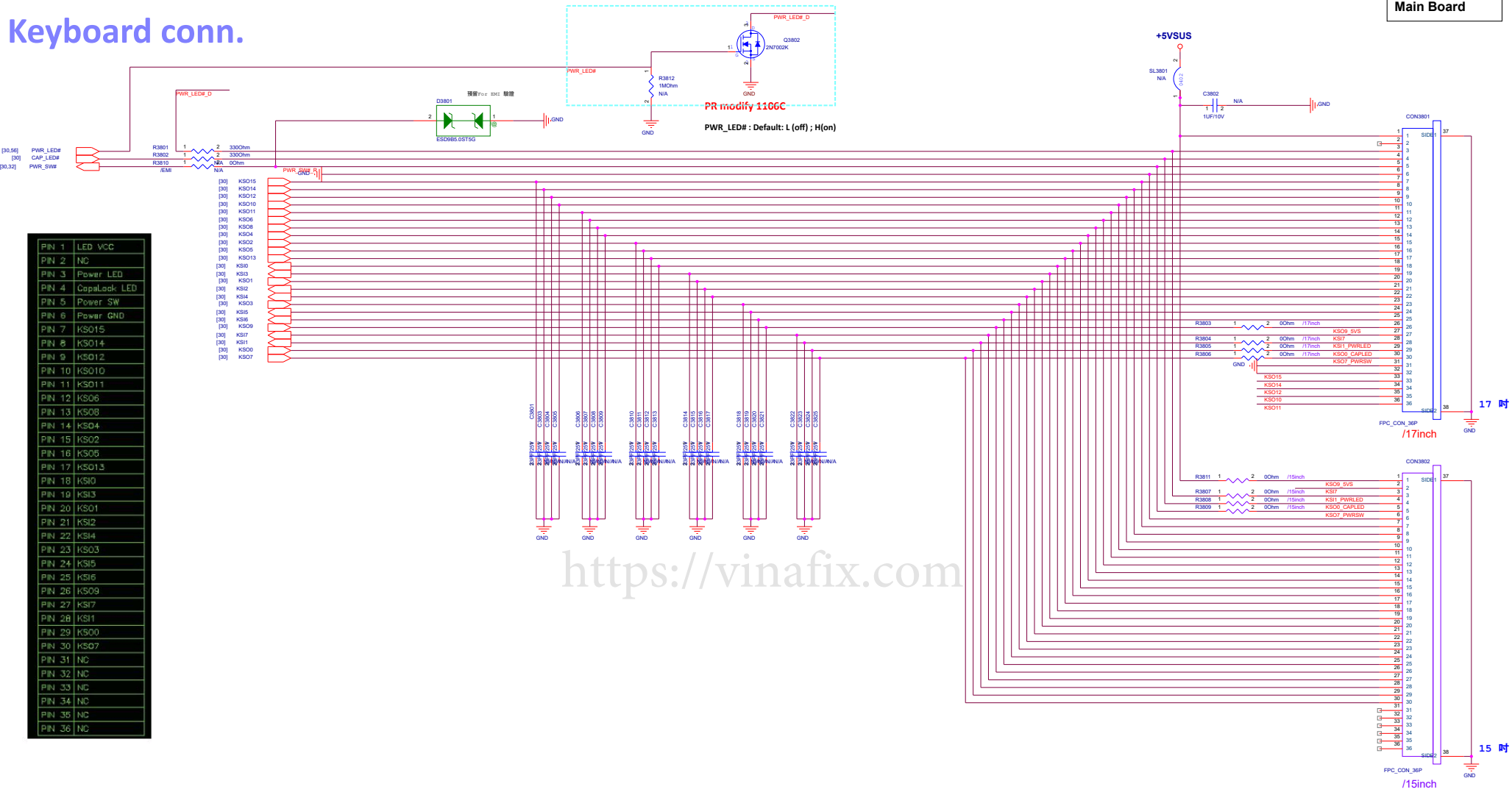
Hall Sensor



06033-00010000 另一顆料，互為替代料，目前沒3Drawing

ASUSTeK COMPUTER INC.	Title : Hall sensor	
	Engineer: EE	
Size: A	Project Name: FX505DY	Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 37 of 103	

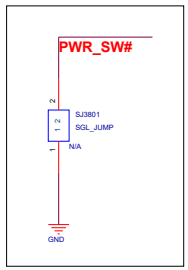
Keyboard conn.



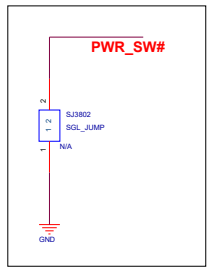
PIN 1	LED VCC
PIN 2	NC
PIN 3	Power LED
PIN 4	CapsLock LED
PIN 5	Power SW
PIN 6	Power GND
PIN 7	KSO15
PIN 8	KSO14
PIN 9	KSO12
PIN 10	KSO10
PIN 11	KSO11
PIN 12	KSO6
PIN 13	KSO8
PIN 14	KSO4
PIN 15	KSO2
PIN 16	KSO5
PIN 17	KSO13
PIN 18	KSI0
PIN 19	KSI3
PIN 20	KSO1
PIN 21	KSI2
PIN 22	KSI4
PIN 23	KSO3
PIN 24	KSI5
PIN 25	KSI6
PIN 26	KSO9
PIN 27	KSI7
PIN 28	KSI1
PIN 29	KSO0
PIN 30	KSO7
PIN 31	NC
PIN 32	NC
PIN 33	NC
PIN 34	NC
PIN 35	NC
PIN 36	NC

Power-on jumper

請放置於空曠處(TOP)



請放置於空曠處(BOTTOM)

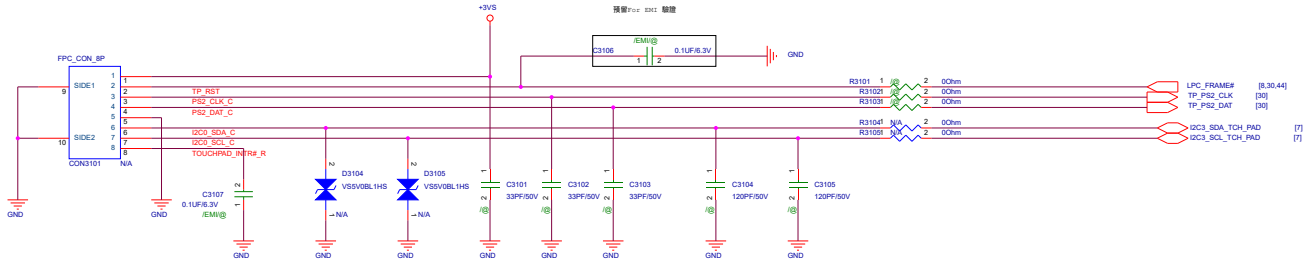


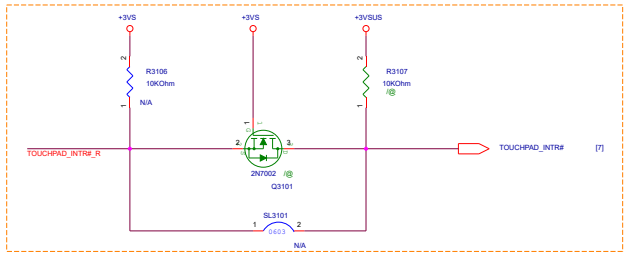
Project Name: FX505DY		Rev: R1.0
Title: AMD_CPU_GND		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date: Thursday, November 29, 2018	Sheet 38 of 103	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Thursday, November 29, 2018	Sheet 19 of 103	

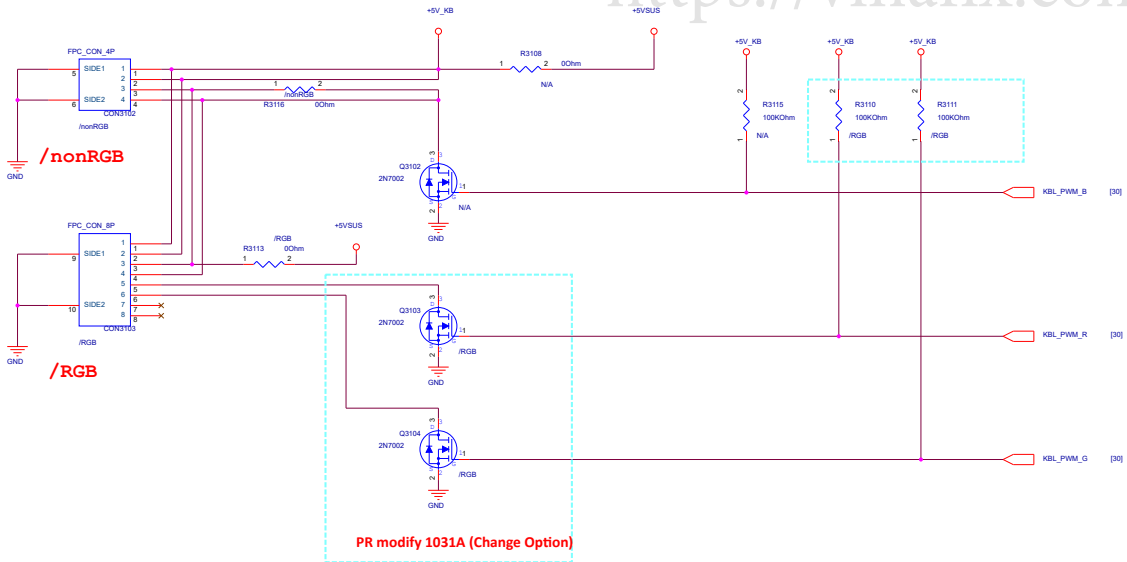
Click pad

Slave (touchpad) address: 0X15



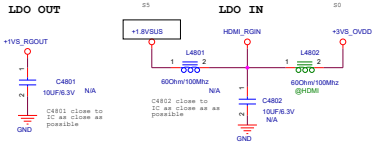


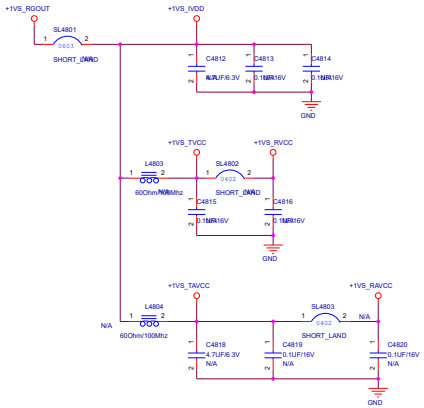
KB Backlight

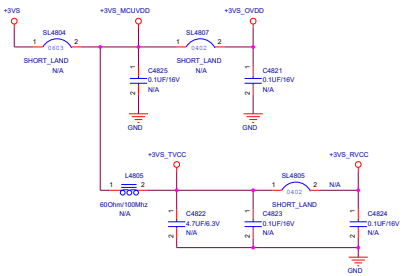


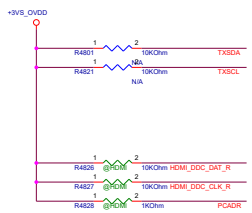
ASUS	Project Name: FX505DY	Rev: R1.0
Title : AMD_CPU_GND		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date: Thursday, November 29, 2018	Sheet 31 of 103	

Internal Regulator option

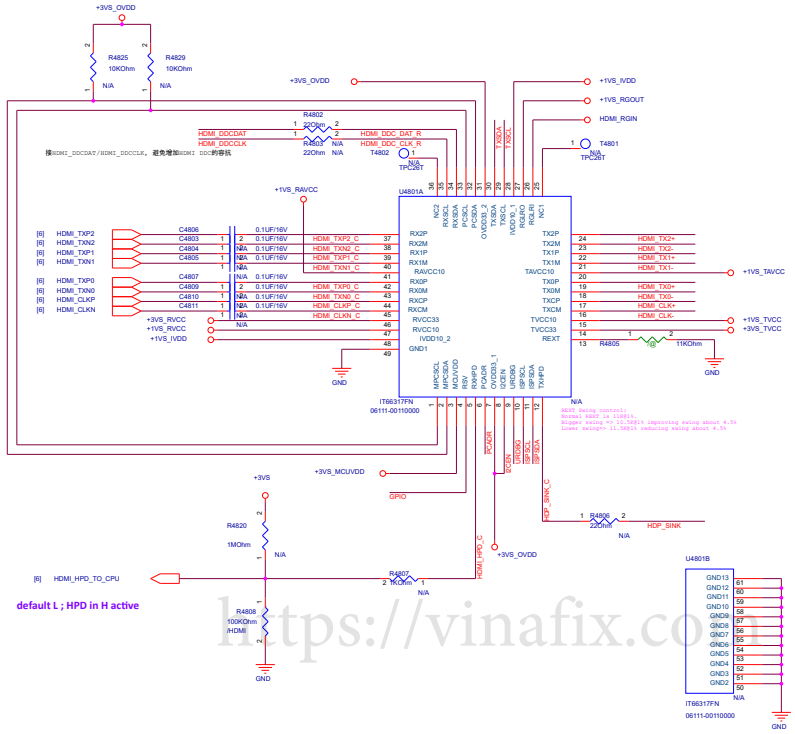




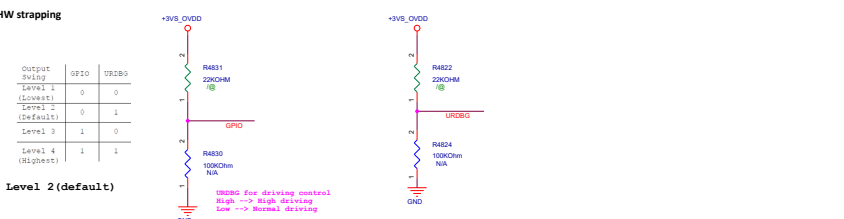




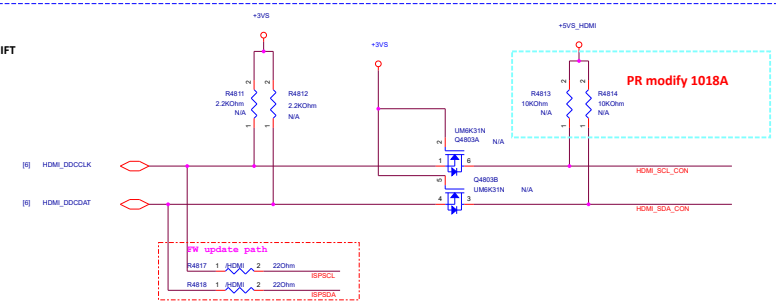
Retimer



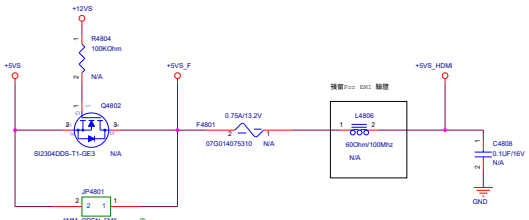
HW strapping



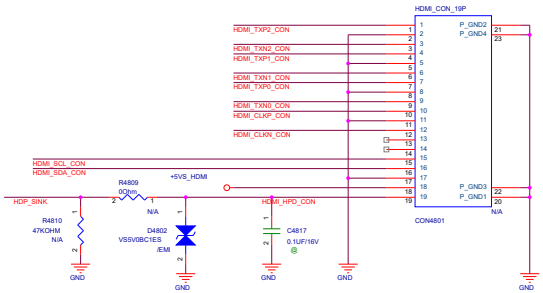
DDC LEVEL SHIFT



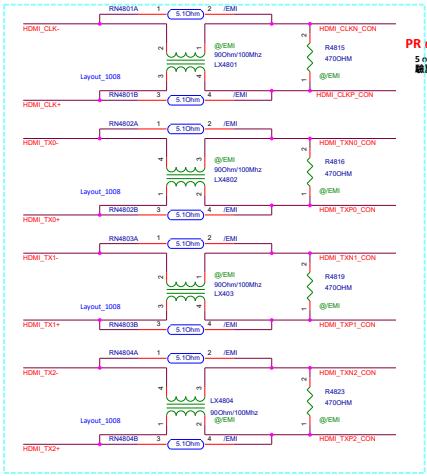
HDMI PWR_+5VS_HDMI

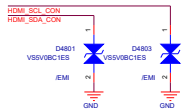


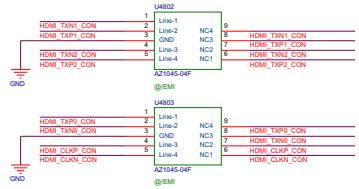
HDMI Conn.



HDMI EMI





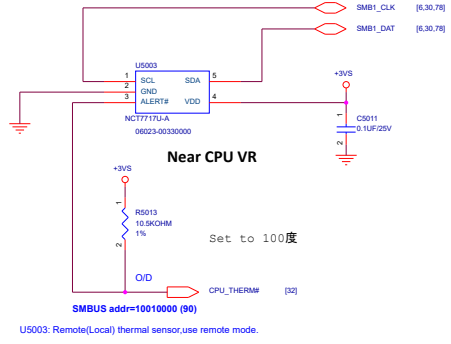


ASUS	Project Name: FX505DY		Rev: R1.0
Title : AMD_CPU_GND			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: RD2 EE3	
Date: Thursday, November 29, 2018	Sheet 48 of 103		

PR modify 1018A

Main Board

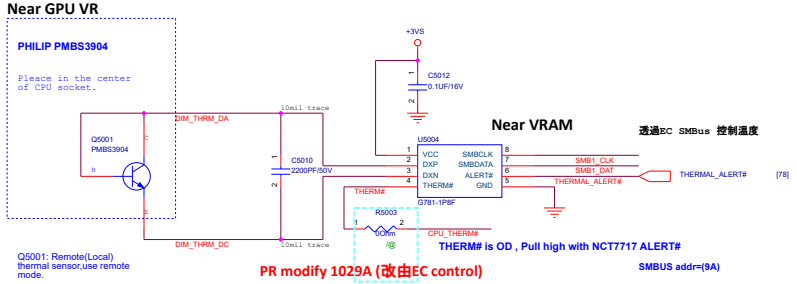
CPU Thermal Sensor (CPU OTP使用, NCT7717)



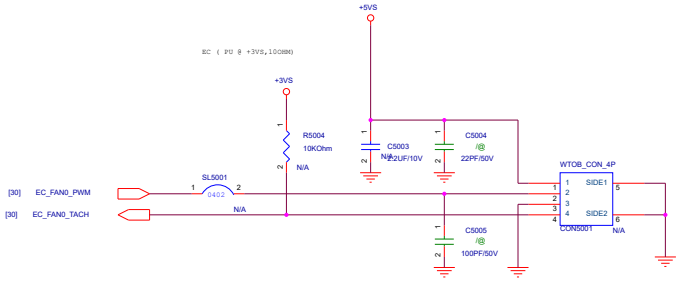
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

10/18 reserve for power noise

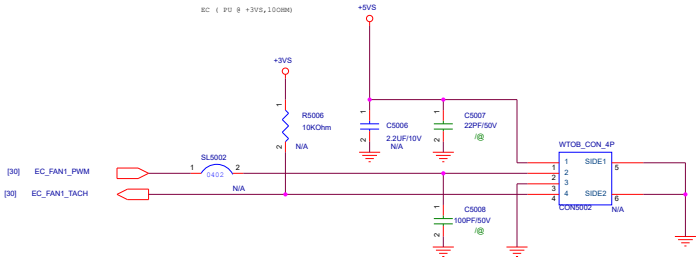
VRAM Thermal Sensor (為保護GPU VRAM使用(G781)



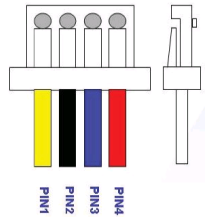
CPU FAN



GPU FAN



4Pins Fan Connector Pins Definition



Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : FAN_Thermal Sensor

Engineer: EE3

Size: Custom | Project Name: FX505DY | Rev: R1.0

Date: Thursday, November 29, 2018 | Sheet 50 of 103

SATA Conn. 2.5 HDD

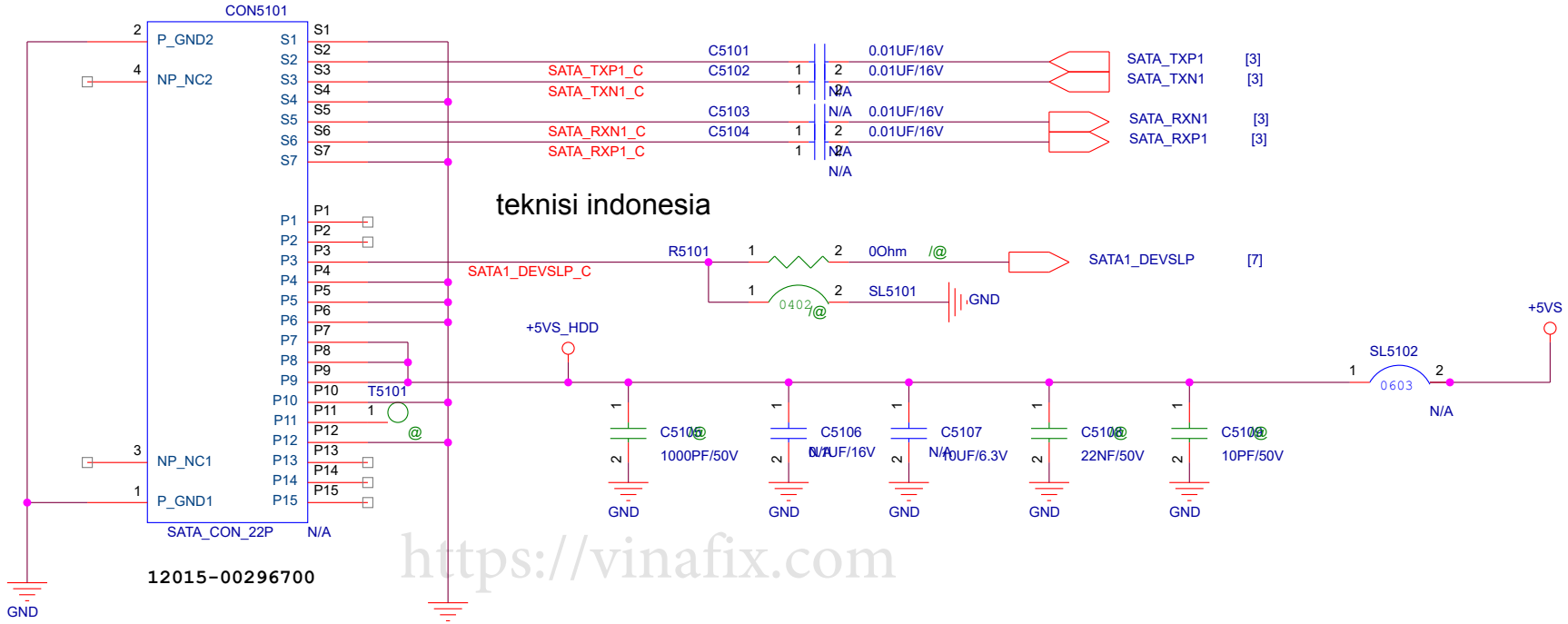
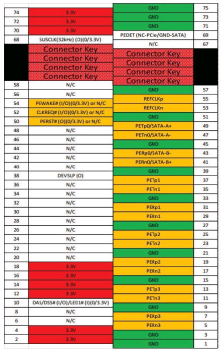
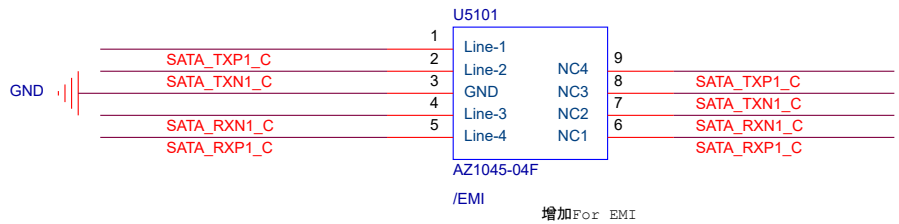


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform





<Variant Name>

ASUSTeK COMPUTER INC. NB3	Title : SATA_HDD	
	Engineer: EE3	
Size: A	Project Name: FX505DY	Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 51 of 103	

Audio codec ALC3251

Analog

Digitial

Headphone

EXT MIC Vref.

EXT MIC IN

MIC

Speak Connector

Combo Jack

Place close to pin 26

Place close audio codec

Place close to pin 1

Place close to 9

50mA

vender recommend for GS mark test on RP out

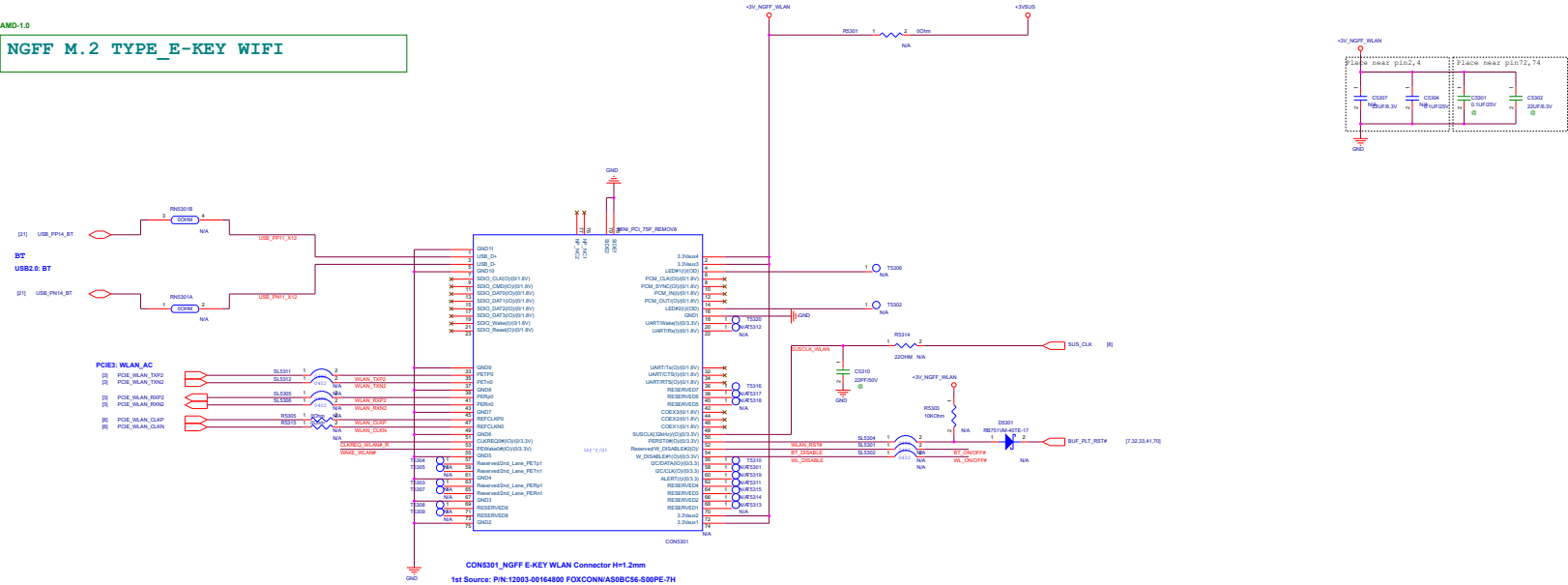
12014-00990300

12017-00930300

Project Name	FX505DY
Title :	
Dept. :	
Engineer:	
Date	Thursday, November 29, 2018

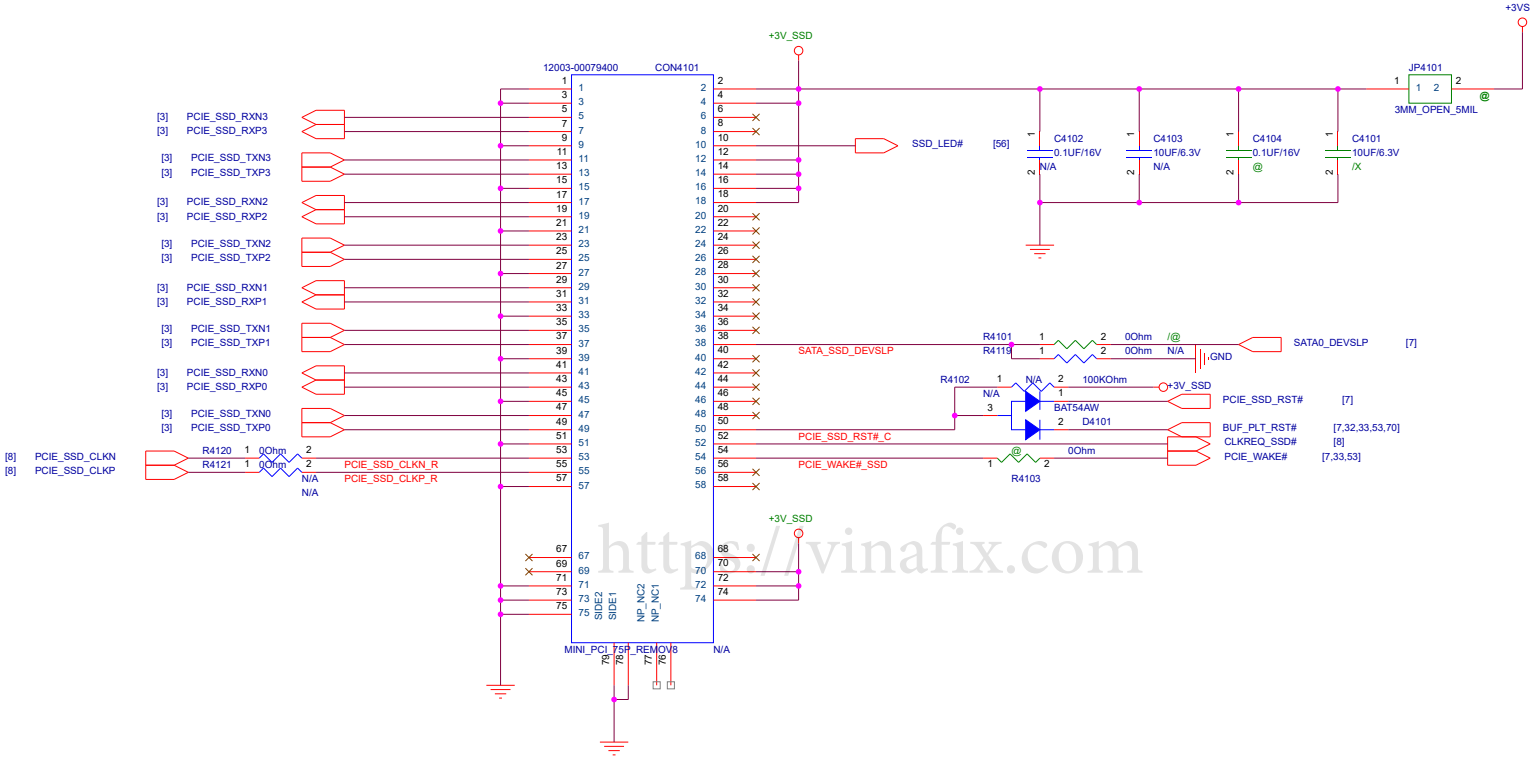
AMD-1.0

NGFF M.2 TYPE_E-KEY WIFI



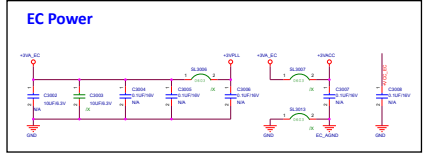
Title:	NGFF Type_WLAN&BT		
ASUSTeK COMPUTER		Engineer:	EE
Size:	Project Name:		Rev:
Custom:	FX505DY		R1.0
Date: Thursday, November 29, 2018		Sheet: 53 of 61	

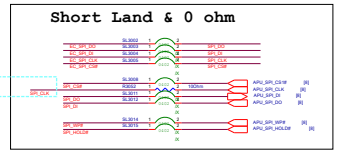
M.2 SSD

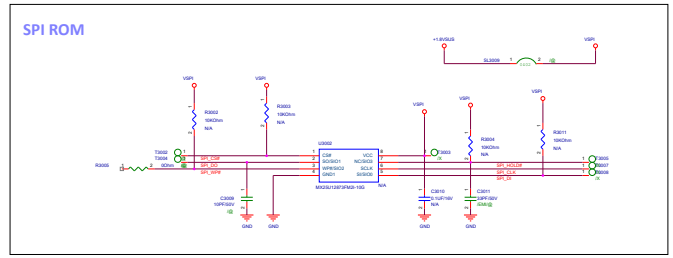


ASUSTeK COMPUTER INC. NB1	Title : NGFF SSD	
	Engineer: EE	
Size: B	Project Name: FX505DY	Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 41 of 103	

EC Chip - IT8225







VCC => +3VS system power ; LPC

VSTBY=>+3VA_EC ;Power supply of EC power

+3VACC=+3VA_EC
+3VAPLL=+3VA_EC_0906

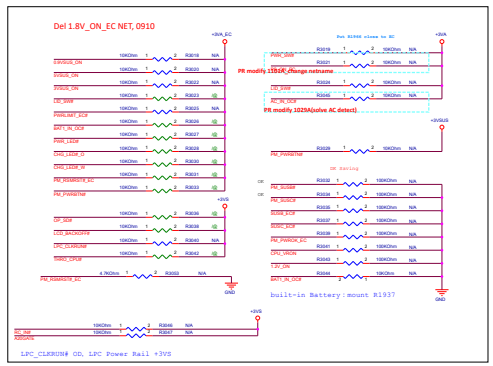
PR modify 1030A

PR modify 1031A_Change PS_ON to PS_ON_EC

PM_PWROK_EC del intersheet ref_0910

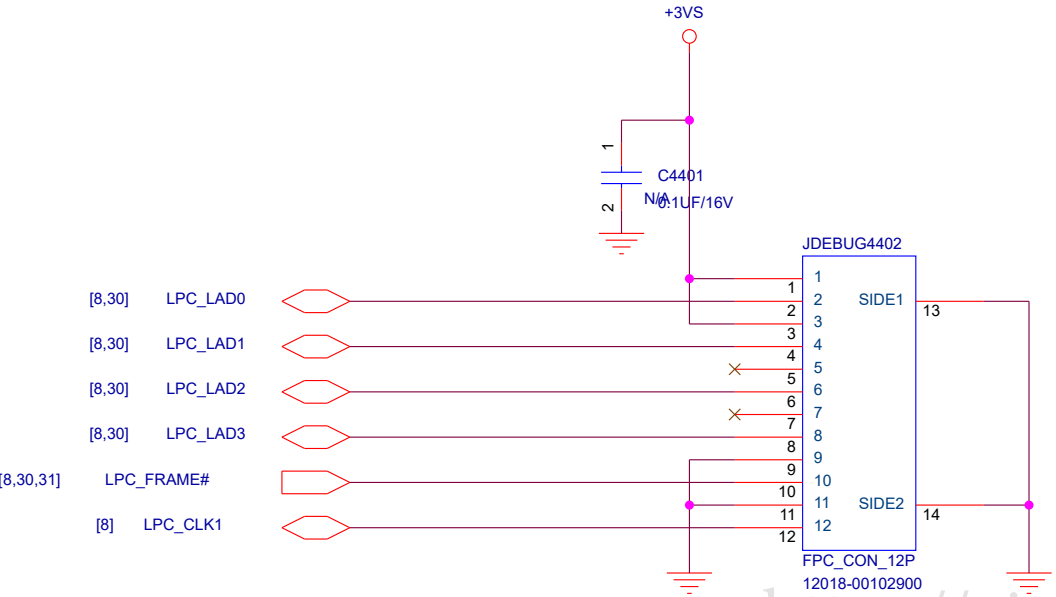
PR modify 1030A

	LED_TYPE_ID
H	RGB
L	RED



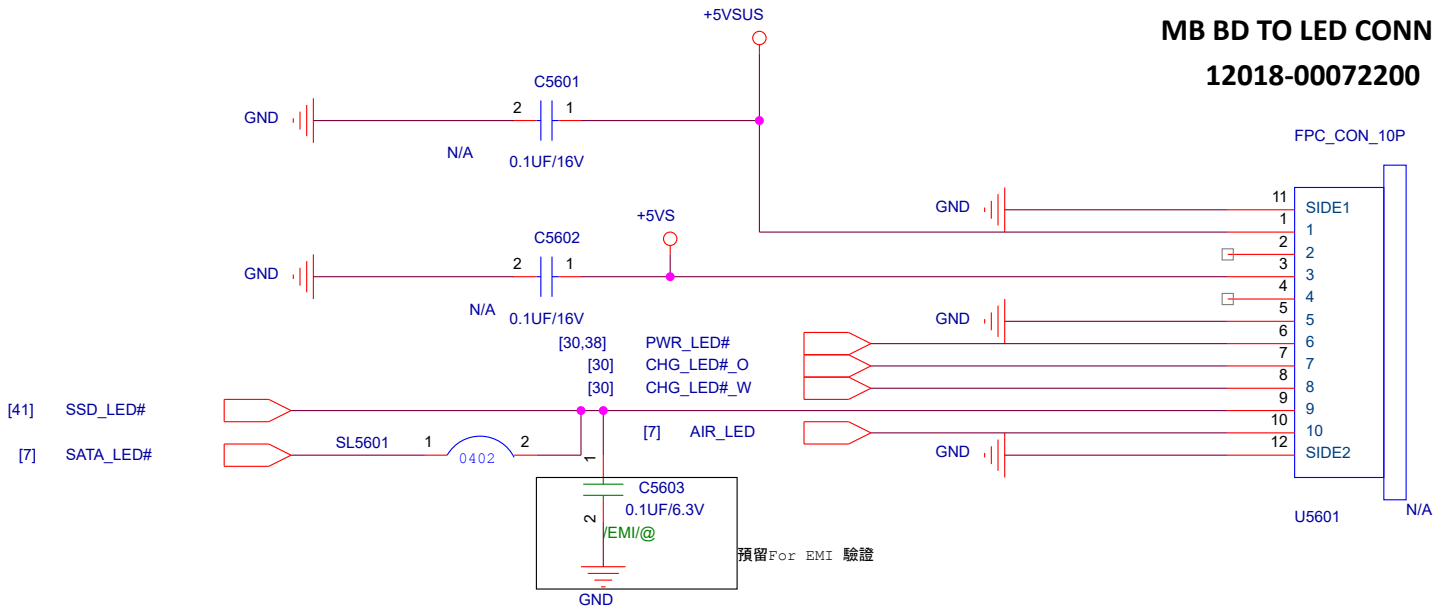
Project Name	FX505YD
Rev	R1.0
Title :	IEC
Dept.:	MB-SZ-RD3
Engineer:	
Date:	Thursday, November 29, 2018
Sheet	30 of 103

LPC Debug Port



ASUSTeK COMPUTER INC.	Title : DEBUG_LPC	
	Engineer: SZNB2	
Size: A	Project Name: FX505DY	Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 44 of 103	

MB_Side LED



Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF

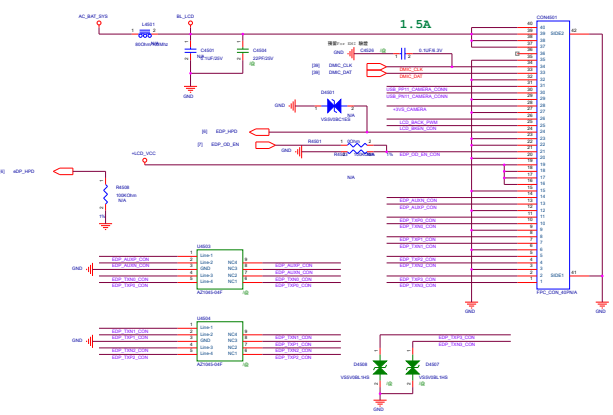
Charger LED

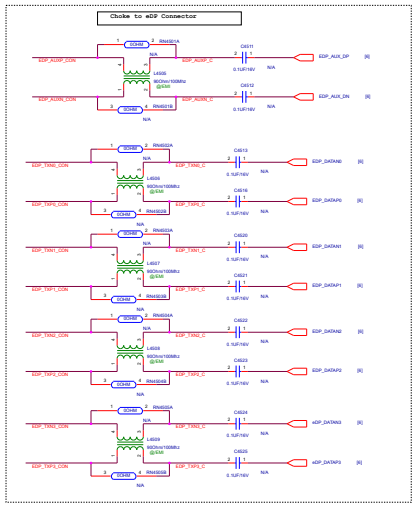
PCB/ID LOCATION

HDD LED

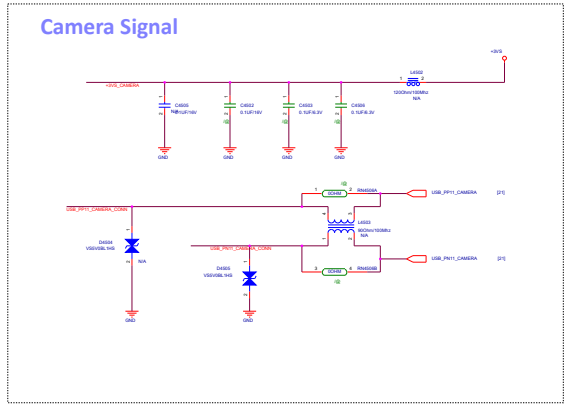
Project Name: FX505DY		Rev: R1.0
Side_LED		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date: Thursday, November 29, 2018	Sheet 56 of 103	

eDP Connector (LVDS)

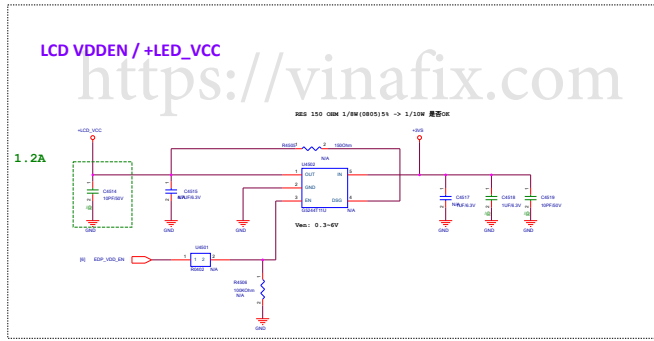




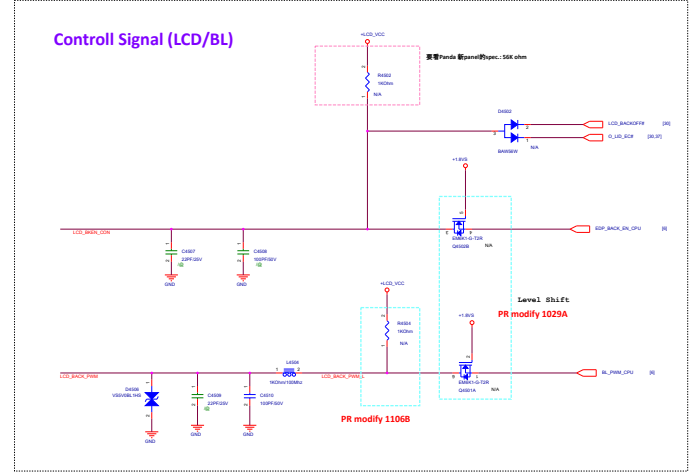
Camera Signal



LCD VDDEN / +LED_VCC

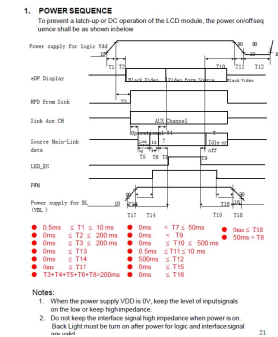


Controll Signal (LCD/BL)

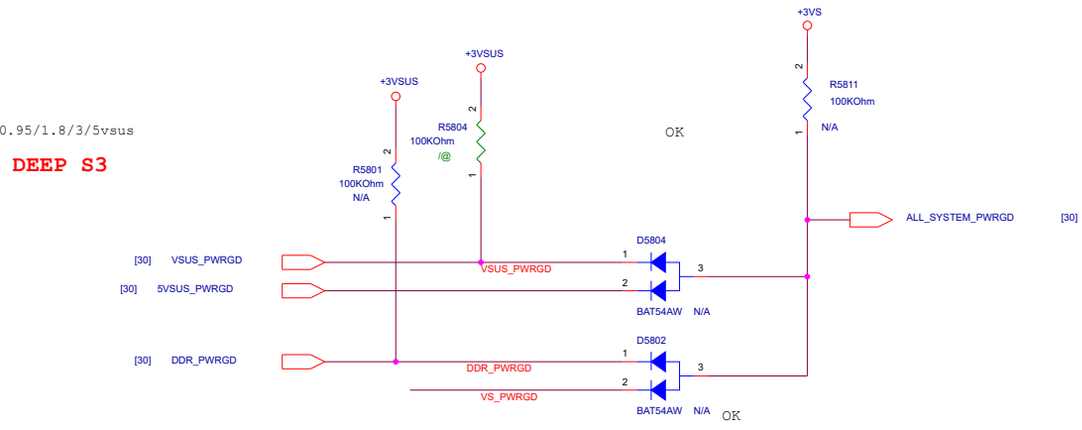


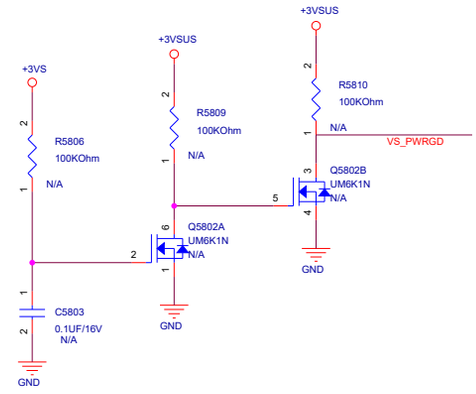
Pin Description

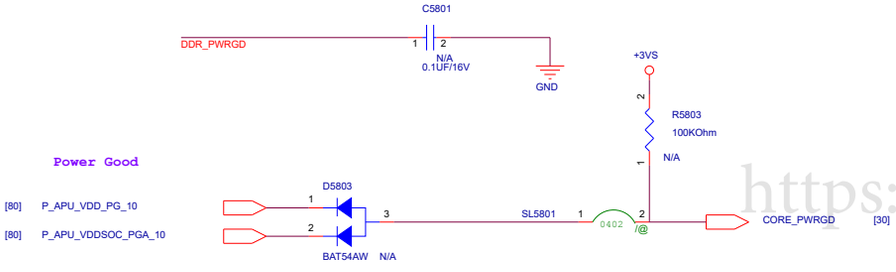
PIN	NAME	PIN FUNCTION
1	OUT	**Switch Output**: Output MOSFET Source. Typically connect to switched side of load.
2	GND	**Ground**
3	EN	**Enable**: Logic level enable input. Make sure EN pin never floating.
4	DSG	**Shutdown Discharge:** Open-drain N-MOS. It will turned on when G5244 is turned off. By connecting a resistor from DSG to OUT pin, user can discharge OUT when G5244 is shutdown.
5.	IN	**Input Supply**: Output MOSFET Drain, which also supplies IC's internal circuitry. Connect to positive supply.

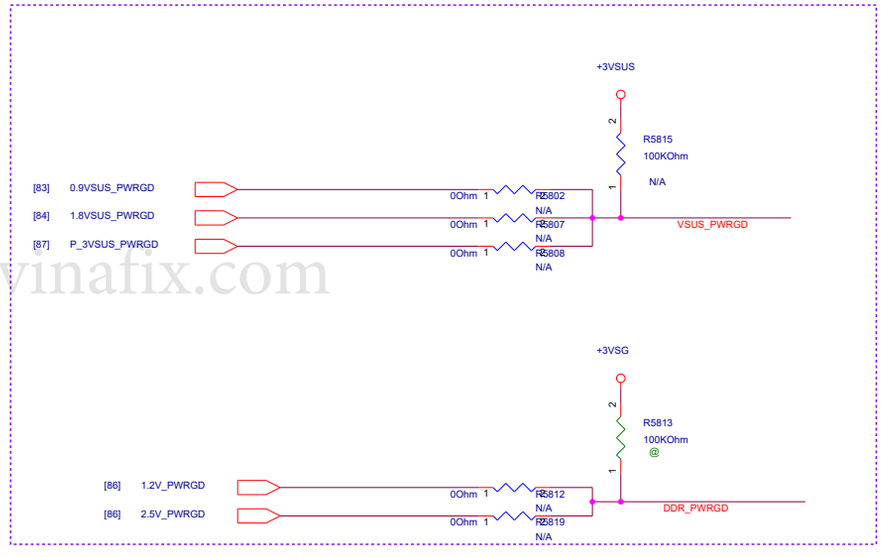


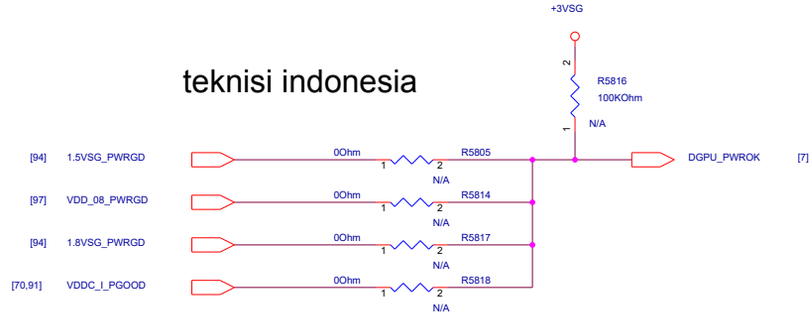
POWER GOOD DETECTER





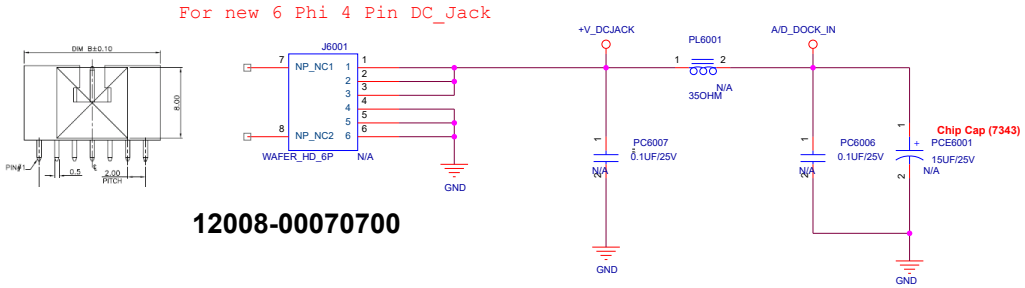






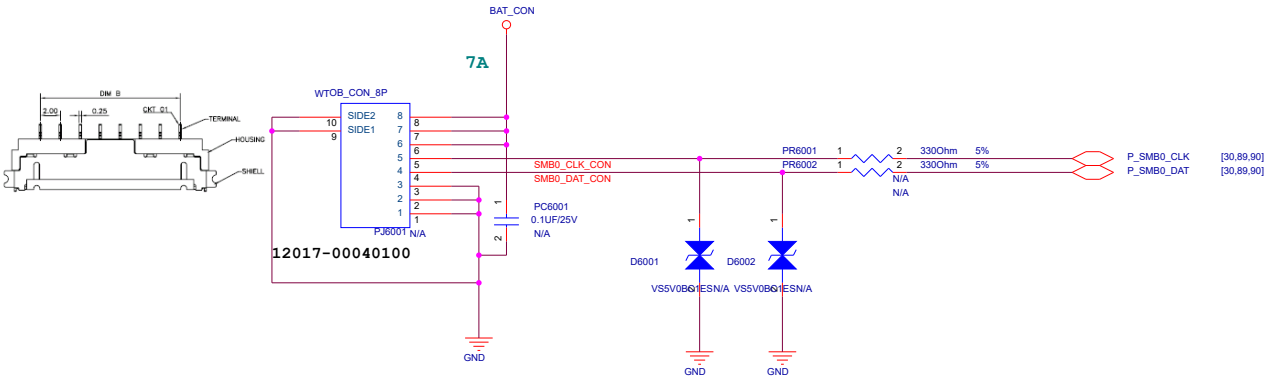
Project Name: FX505DY		Rev: R1.0
Title: POWER GOOD DETECTER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Thursday, November 29, 2018	Sheet 58 of 103	

DC-IN Connector



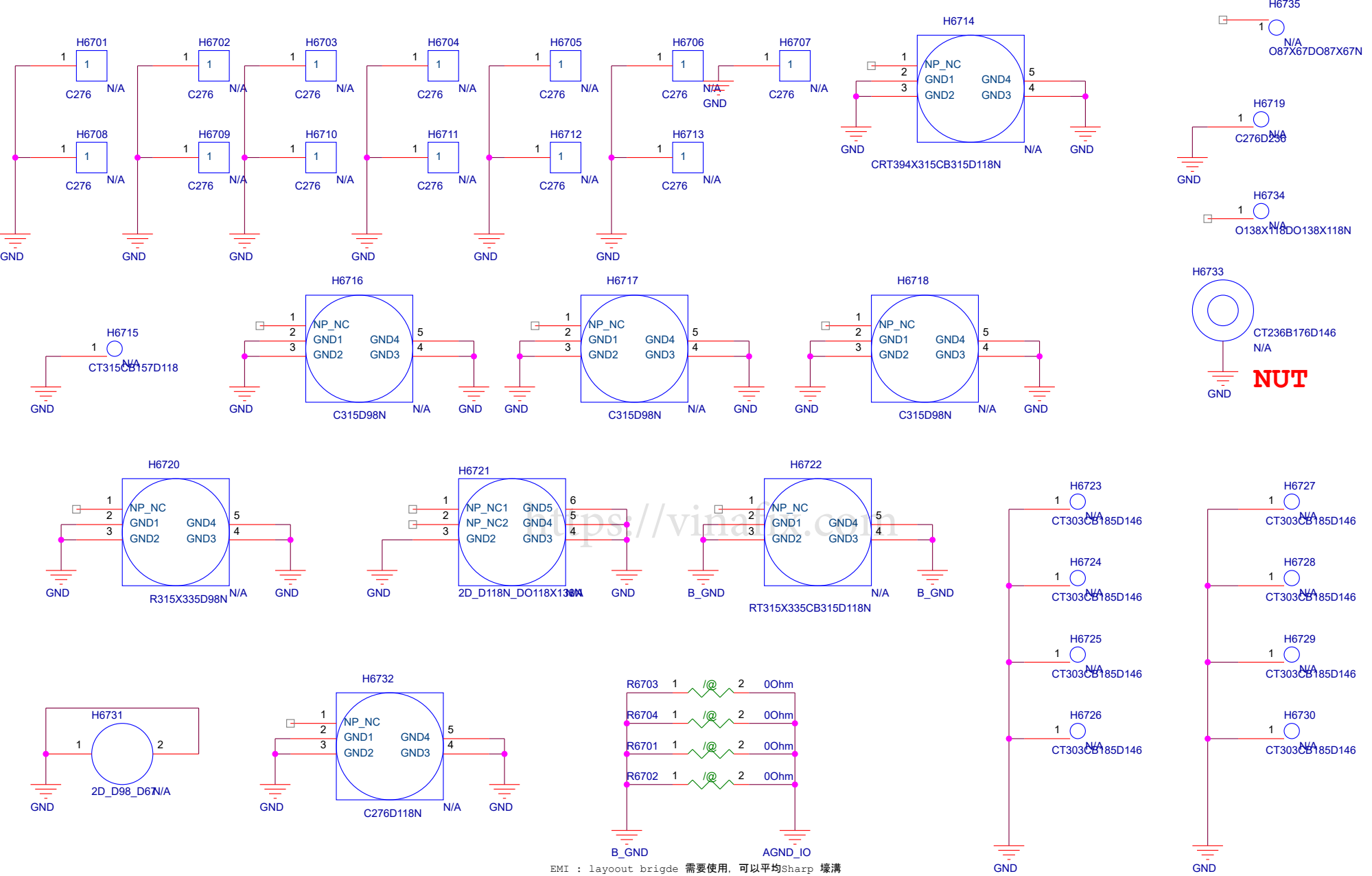
12008-00070700

Battery Connector



Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

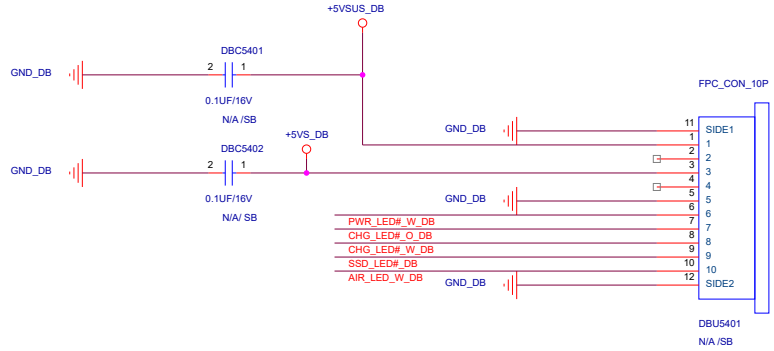
ASUS	Project Name: FX505DY		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: CS Lin	
Date: Thursday, November 29, 2018	Sheet 60 of 103		



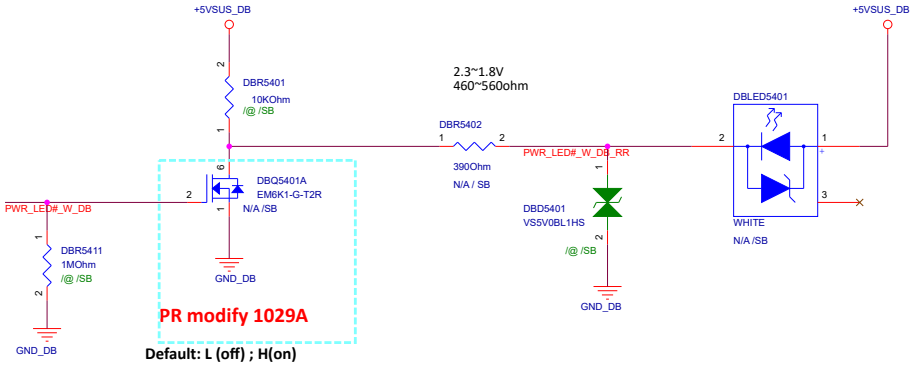
<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title : SREW HOLE	
	Engineer: EE	
Size: A	Project Name: FX505DY	Rev: R1.0
Date: Thursday, November 29, 2018	Sheet 67 of 103	

SB_Side LED

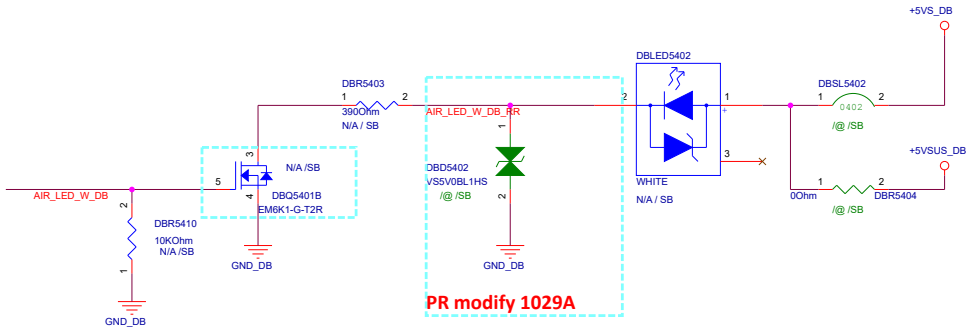


Power LED

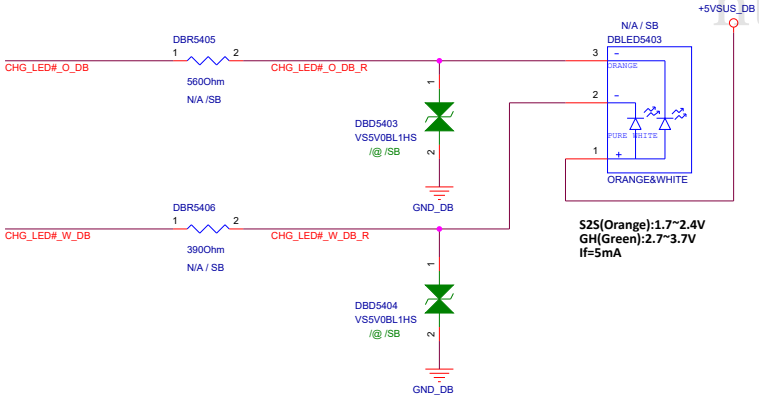


AIR PLANE LED(White)

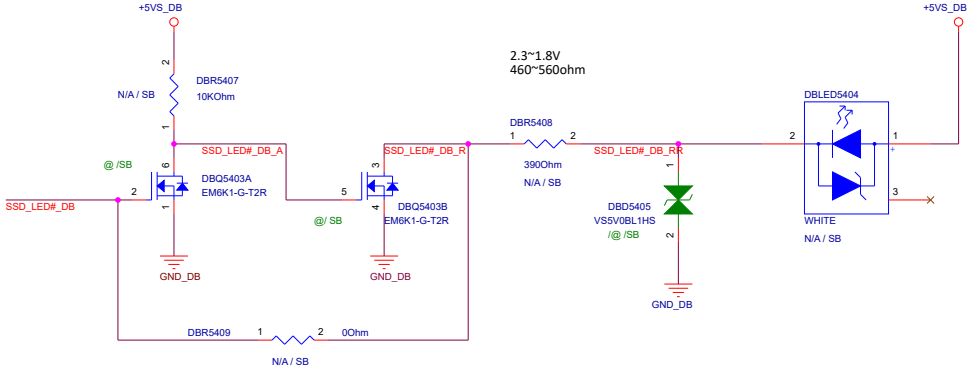
NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF



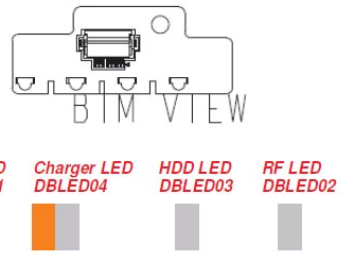
Charger LED(White/Orange)



HDD LED



PCB/ID LOCATION

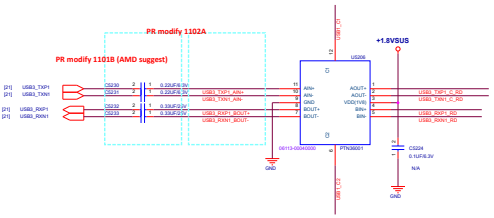


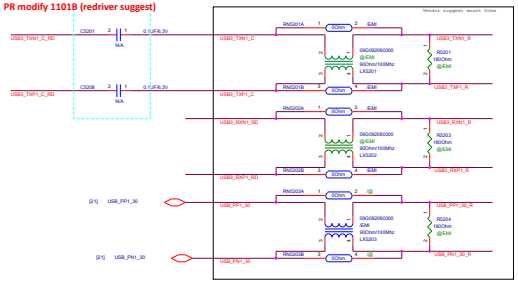
Tooling Hole

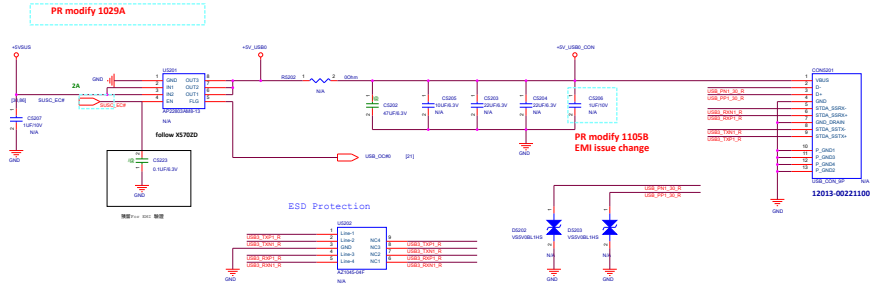
ASUS	Project Name: FX505DY	Rev: R1.0
Title : POWER GOOD DETECTER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date: Thursday, November 29, 2018	Sheet 54 of 103	

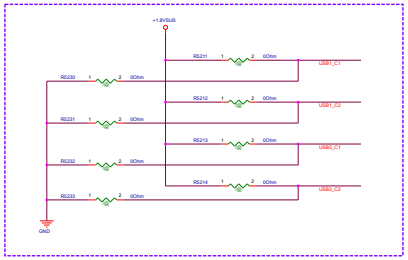
USB3.0_Port 0

EMI 建議 USB3.0 可不上Choke / USB2.0 上Choke









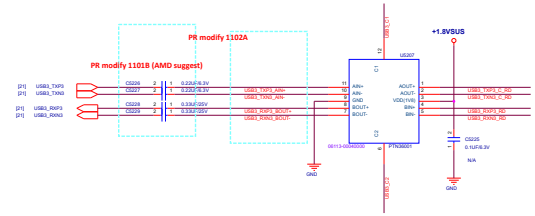
Redriver Control strap pin

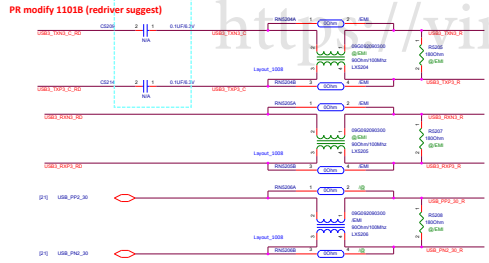
	USB1		USB3	
	USB1_C1	USB1_C2	USB3_C1	USB3_C2
PULL HIGH	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout
OPEN MEDIUM				
PULL LOW	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout

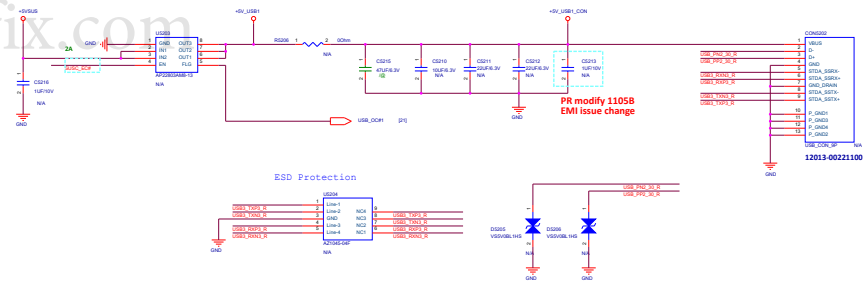
DNI: unmout
NI: mout

CPU 到 USB-redriver 長度: 11 Inch -> 建議先使用Medum (若是fail 再改Low)
Vendor layout 建議: 每一段等長要5mil 以內; 建議穿層僅能換2次 ;

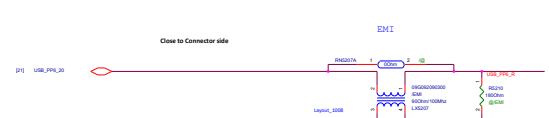
USB3.0_Port 3

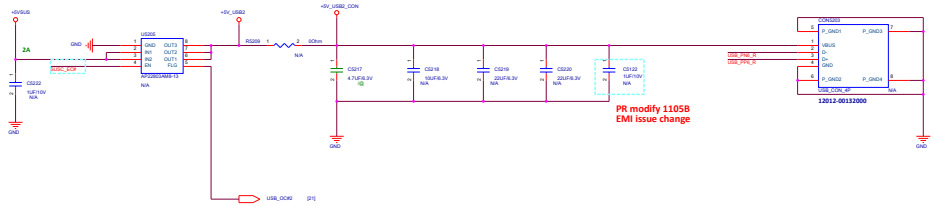


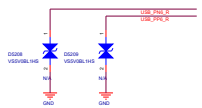


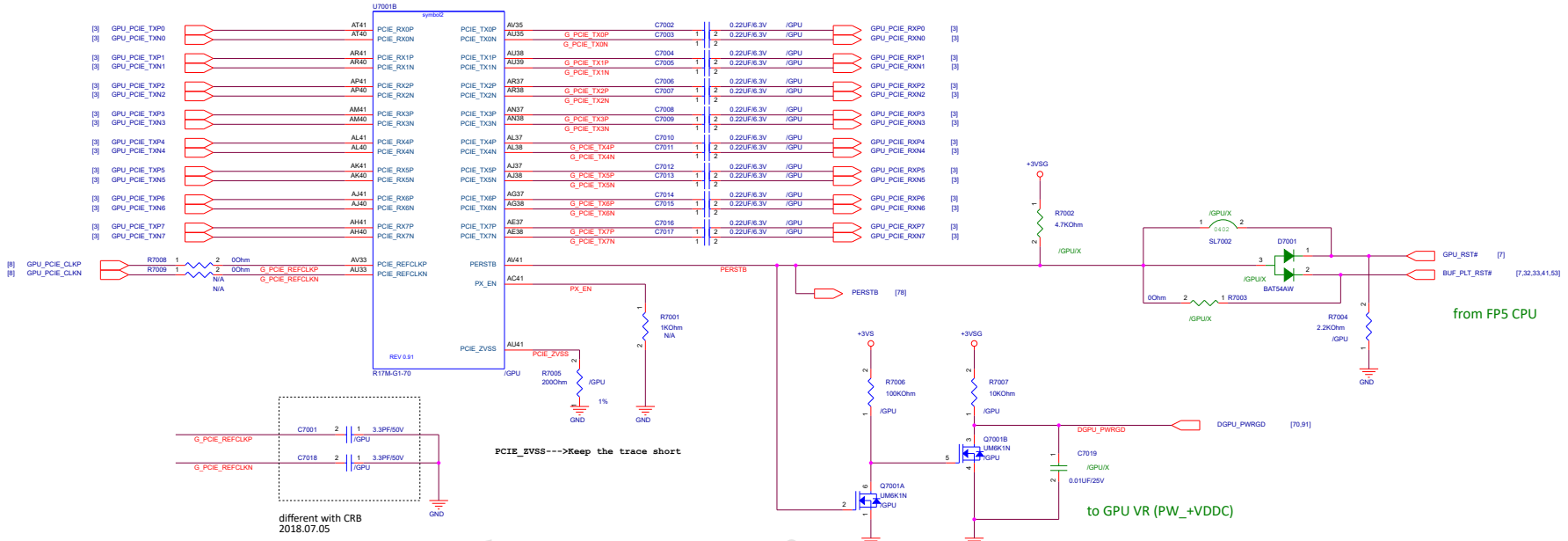


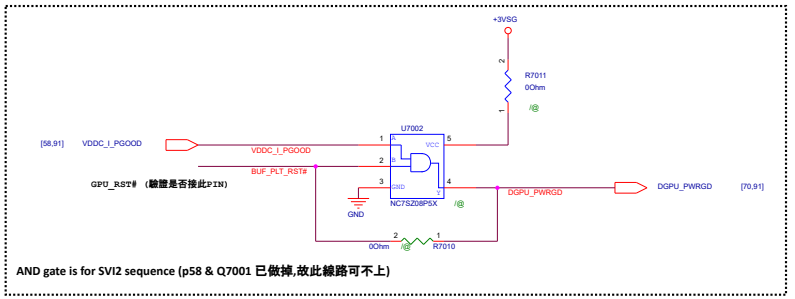
USB2.0_Port 0





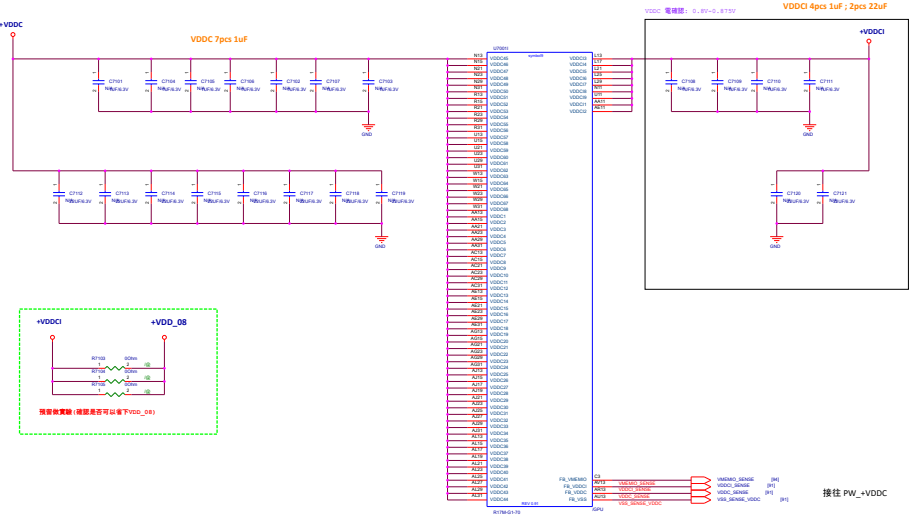


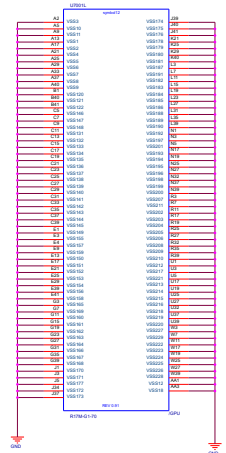




Project Name: FX505DY			Rev: R1.0
Title: DGPU_PCIE			
Size: C	Dept.: ASUSTek Computer Inc.	Engineer: RD1/EE2	
Date: Thursday, November 29, 2018	Sheet 70 of 103		

DGPU_Power





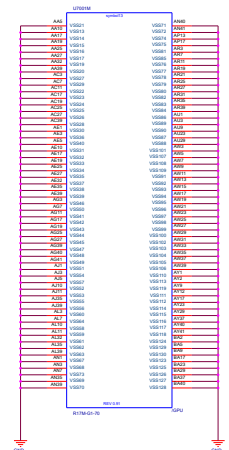
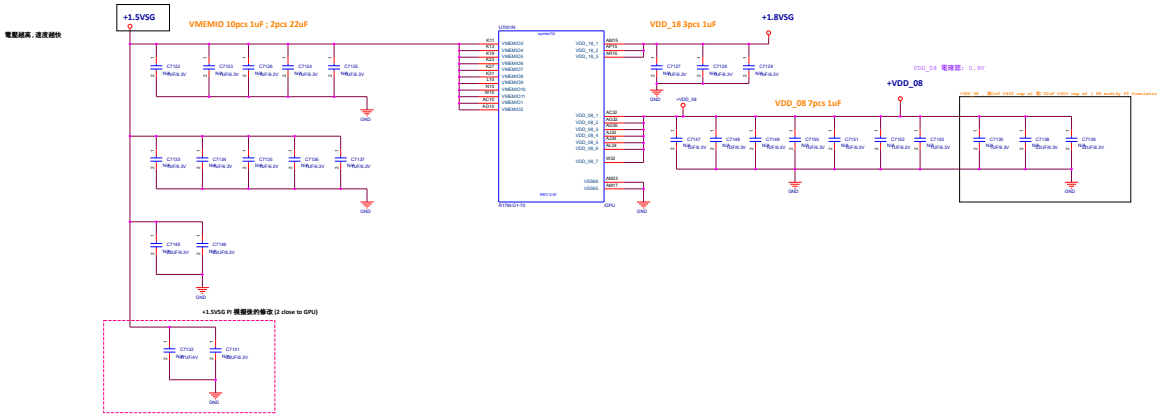
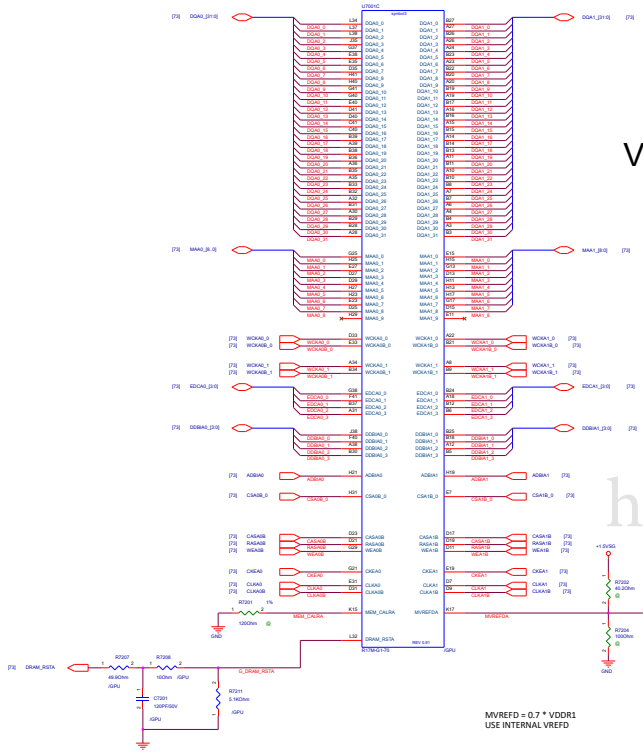


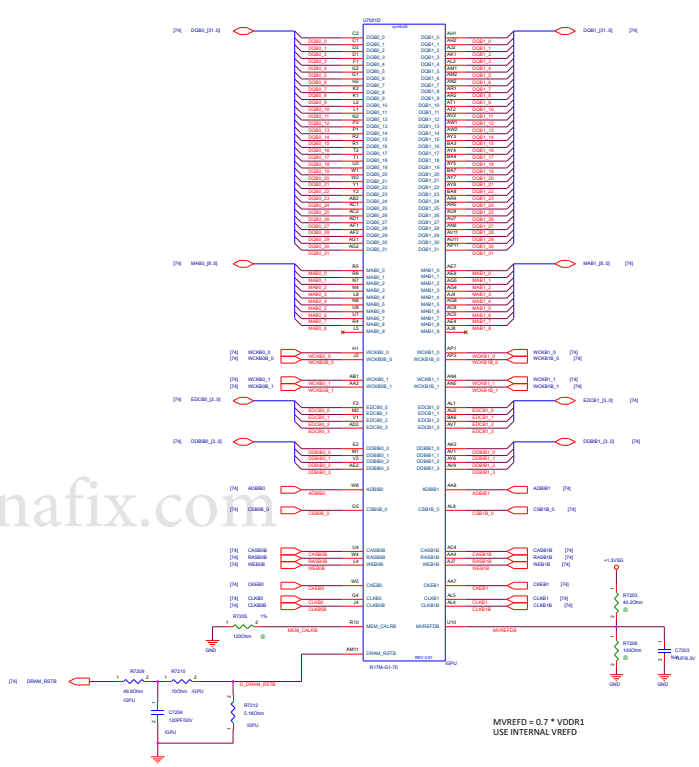
Table 5–2. Regulator Guidelines

Rail Name	Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDC	0.700 V to 1.100 V	VID_VDDC ± 1.VDDC × 0.6 mΩ ± 20 mV	Overshoot: 120 mV Undershoot: 90 mV	XT: 60 A (TDC) XT: 140 A (EDC) XL: 50 A (TDC) XL: 110 A (EDC)	1, 2, 4
VDDCI	0.800 V to 0.875 V	± 3%	± 3%	8 A (TDC)	
VDD_08	0.9 V	± 3%	± 3%	4 A (TDC)	
VMEMIO	1.5 V	± 3%	± 3%	2 A (TDC)	3

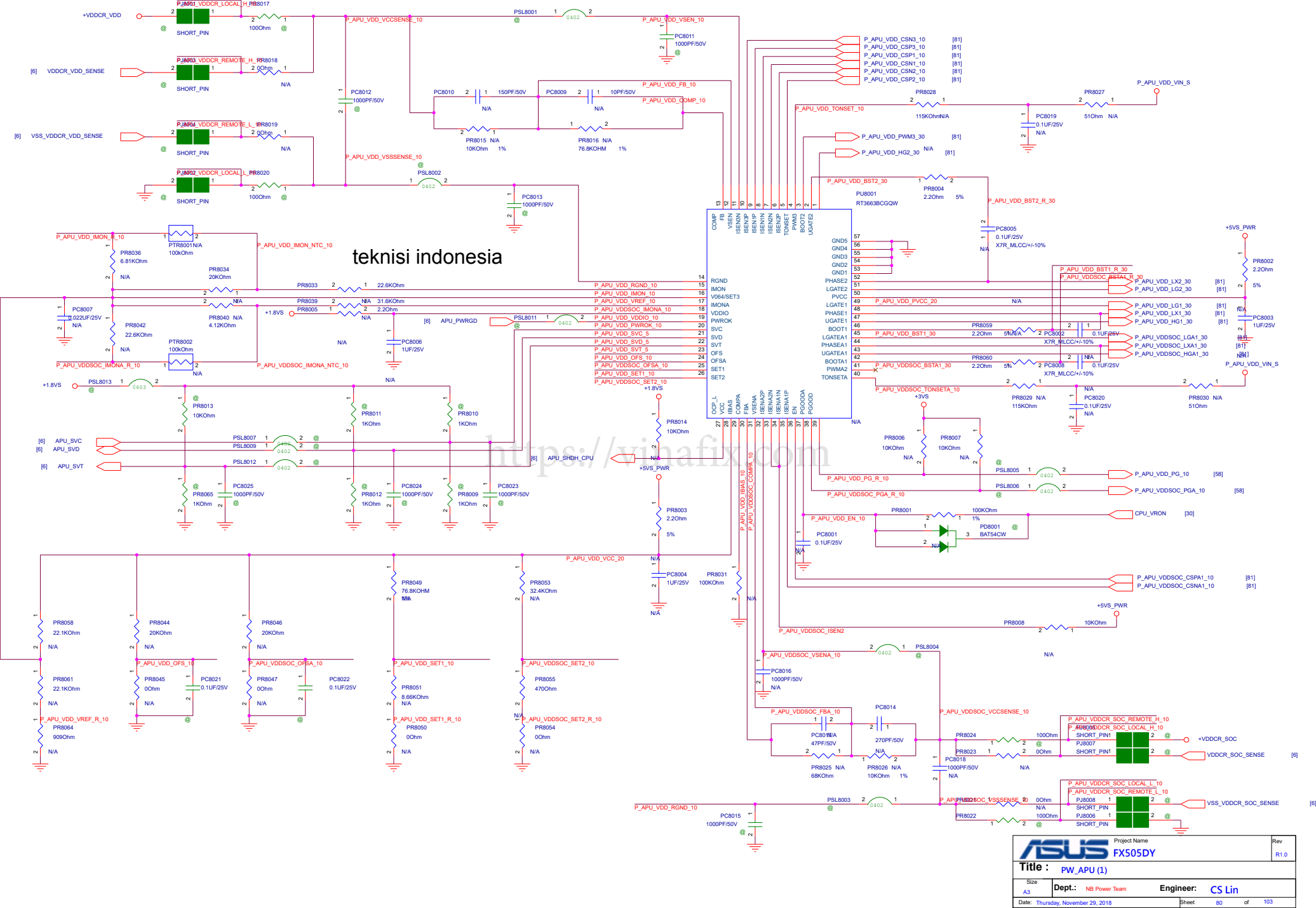


ASUS	Project Name: FX505DY		Rev: R1.0
Title : DGPU_POWER&GND			
Size: D	Dept.: ASUSTeK Computer Inc.	Engineer: RD1/EE2	
Date: Thursday, November 29, 2018	Sheet: 71 of 103		



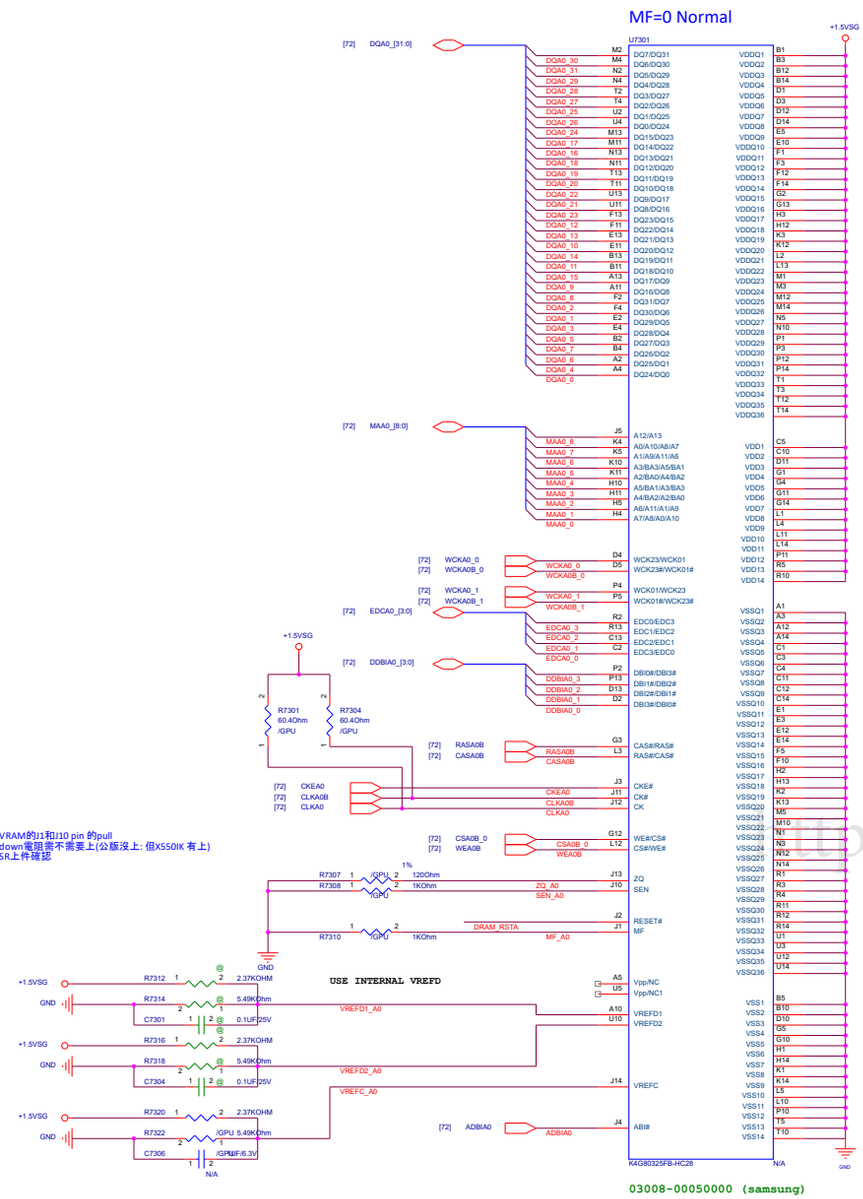


Project Name	X550IU
Rev	31.0
Title :	DGPU_DDR_INTERFACE
Size: D	Dept.: ASUSTek Computer Inc.
Engineer:	RD1/EE2
Date: Thursday, November 29, 2018	Sheet 73 of 103


teknisi indonesia
https://vinafix.com
PU8001
RT3663BCGQW
FX505DY
PW_APU (1)
CS Lin
NB Power Team
Thursday, November 29, 2018

FBA Partition Memory (1 of 2)

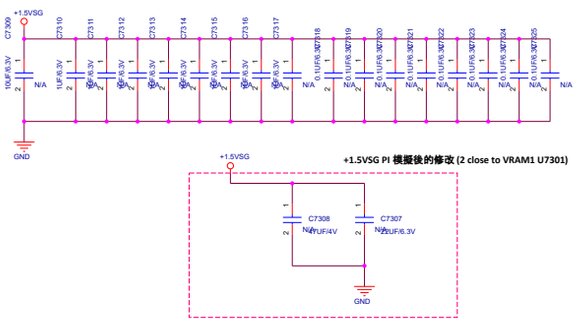
MF=0 Normal



03008-00050000 (samsung)

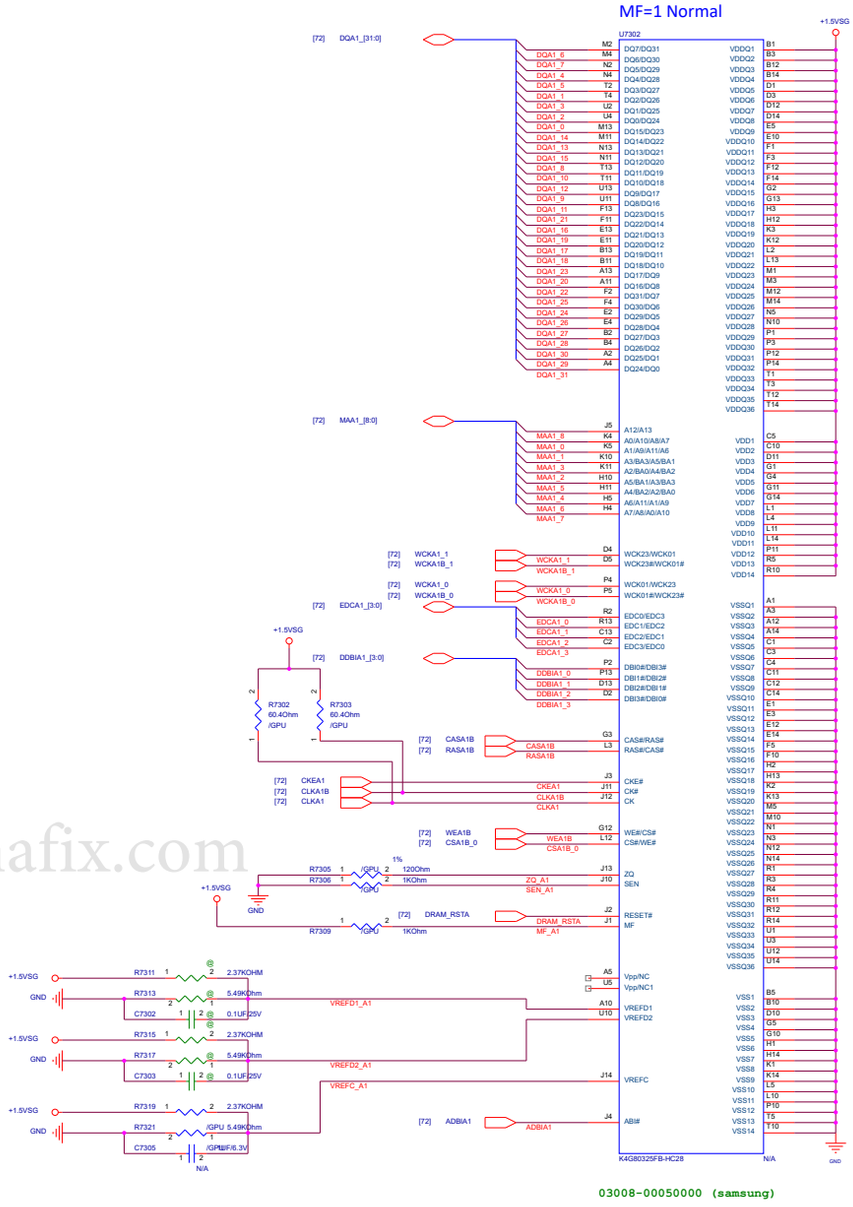
替代料號: 03008-00050400 (Micron)

VDDQ/VDD (Memory Parts) 1pcs 10uF ; 8pcs 1uF ; 10pcs 1uF



FBA Partition Memory (2 of 2)

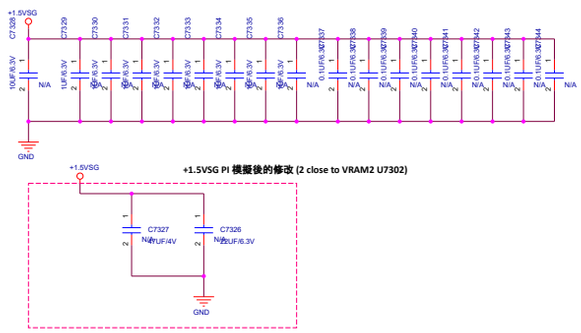
MF=1 Normal



03008-00050000 (samsung)

替代料號: 03008-00050400 (Micron)

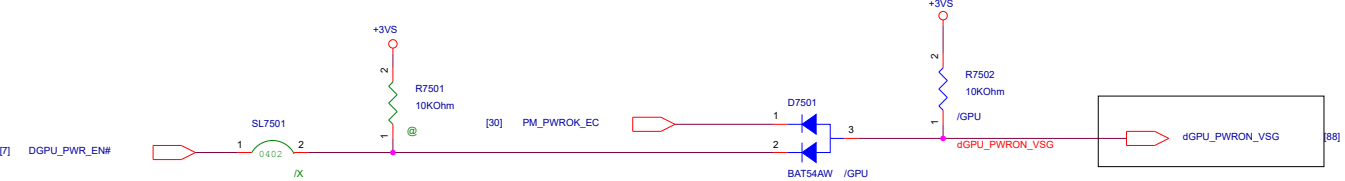
VDDQ/VDD (Memory Parts) 1pcs 10uF ; 8pcs 1uF ; 10pcs 1uF



GDDR5 256x32_7.0G (8Gb)

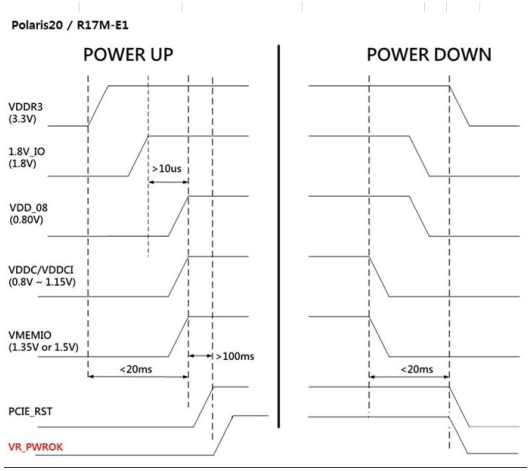
Priority	Company	Model Name	Base		Voltage	Speed	MP Schedule	ASUS P/N
1	Samsung	K4G80325FB-HC28	Samsung	256x32	1.35V/1.55V	6.0G/7.0G	MP	03008-00050000
2	Micron	MT51J256M32HF-70:A	Micron	256x32	1.35V/1.5V	6.0G/7.0G	MP	03008-00050400

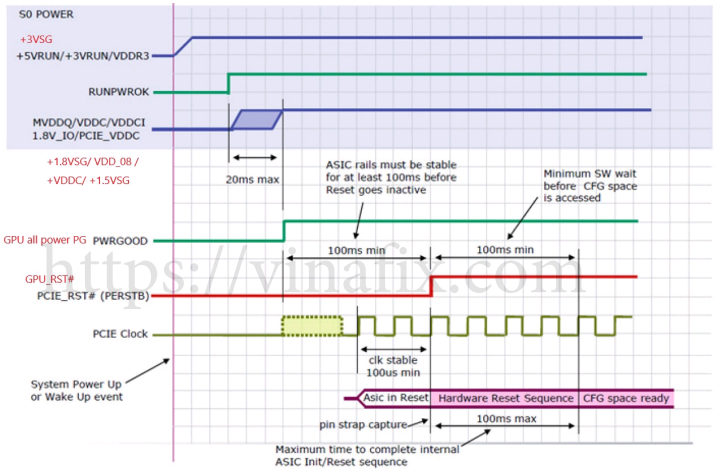
ASUS	Project Name: X550IU		Rev: R1.0
Title :	DGPU_GDDR5_1		
Size: Custom	Dept.: ASUSTek Computer Inc.	Engineer: RD1/EE2	
Date: Thursday, November 29, 2018	Sheet 73 of 103		



經LS 開 +3VSG

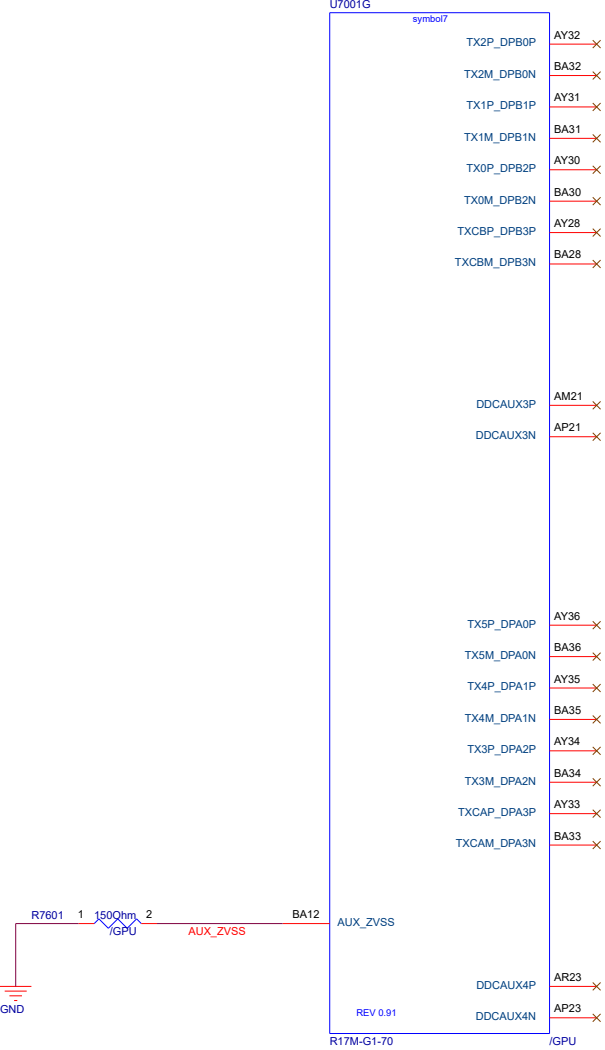
Power on sequence

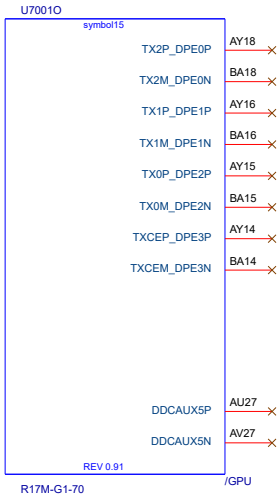




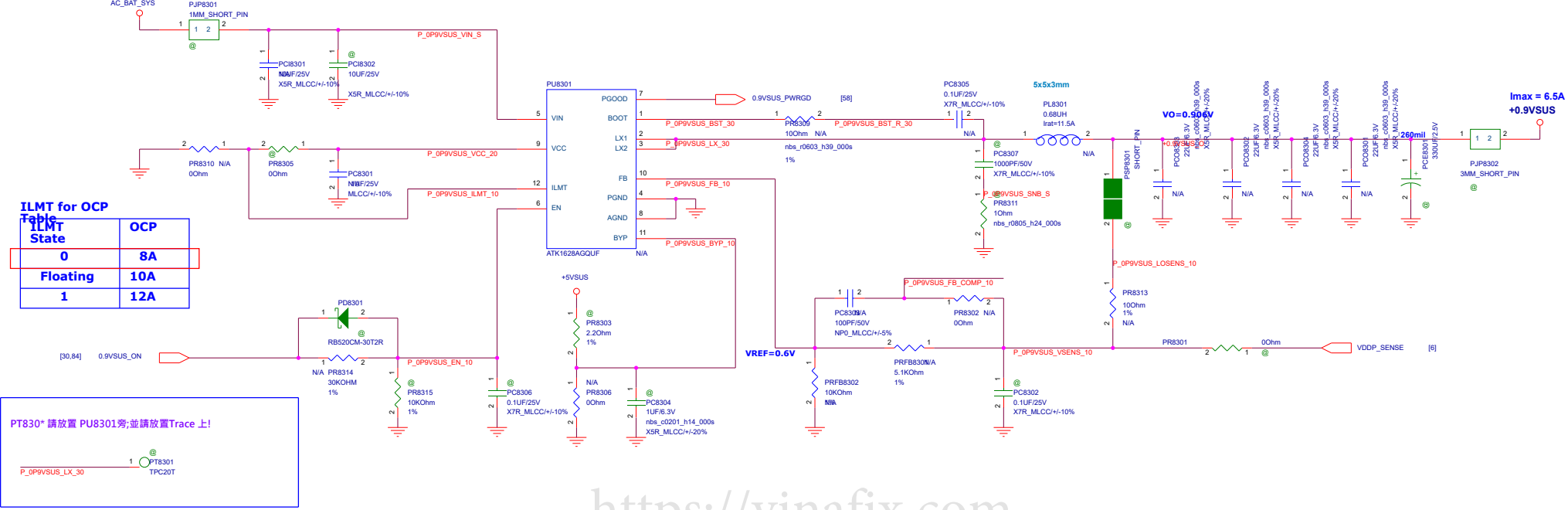
Power Up Sequence		
3-225		All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a
3-230		It is recommended that the 3.3-V rail ramp up first.
3-235		The VDD_18 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

ASUS	Project Name: X550IU	Rev: R1.0
Title : DGPU_POWER_ON_SEQUENCE		
Size: B	Dept.: ASUSTek Computer Inc.	Engineer: RD1/EE2
Date: Thursday, November 29, 2018	Sheet 75 of 103	





ASUS	Project Name: X550IU	Rev: R1.0
Title : DGPU_TMDP		
Size: B	Dept.: ASUSTek Computer Inc.	Engineer: RD1/EE2
Date: Thursday, November 29, 2018	Sheet 76 of 103	



ILMT for OCP Table

ILMT State	OCP
0	8A
Floating	10A
1	12A

PT830* 請放置 PU8301旁;並請放置Trace 上!

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title : PW_+0.9VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Thursday, November 29, 2018	Sheet 83 of 103	

U7001H

symbol8

TX2P_DPD0P	AY22
TX2M_DPD0N	BA22
TX1P_DPD1P	AY21
TX1M_DPD1N	BA21
TX0P_DPD2P	AY20
TX0M_DPD2N	BA20
TXCDP_DPD3P	AY19
TXCDM_DPD3N	BA19
AUX1P	AY11
AUX1N	BA11
DDC1CLK	AY10
DDC1DATA	BA10
TX5P_DPC0P	AY27
TX5M_DPC0N	BA27
TX4P_DPC1P	AY26
TX4M_DPC1N	BA26
TX3P_DPC2P	AY25
TX3M_DPC2N	BA25
TXCCP_DPC3P	AY24
TXCCM_DPC3N	BA24
AUX2P	AP19
AUX2N	AM19
DDC2CLK	AV19
DDC2DATA	AU19

REV 0.91

/GPU

R17M-G1-70

Project Name: X550IU		Rev: R1.0
Title : DGPU_TMDP		
Size: A	Dept.: ASUSTek Computer Inc.	Engineer: RD1/EE2
Date: Thursday, November 29, 2018	Sheet 77 of 103	

Flag code	EC SMBUS read DGPU Temperature cmd	DGPU TYPE	Remark
01	step1:82 01 04 0F 00 01 C5 step2:82 03 83 04 xx xx xx xx	R16M-M1-30 R16M-M1-20	0: 代表本 案所用到 的DGPU 型號
02	step1:82 01 04 0F 00 01 BE step2:82 02 04 CD 30 00 14 step3:82 01 04 0F 00 00 BF step4:82 03 83 xx xx xx xx	0:R16M-G1-70	

SMbus connect to EC

ADM PU

SVC & SVD to +VDDC/+VDDCI VR

SVT from +VDDC/+VDDCI VR

SVC	SVD	V	
0	0	1.1	
0	1	1.0	
1	0	0.9	DEFAULT
1	1	0.8	

to PW VDDW

PR modify 1029A

from GPU temp sensor (兩個)

PR modify 1031B

PR modify 1031B

Critical temperature fault event (CTF), 3.3V active high, default 95 degree

06011-00490000

盡可能靠近DGPU放, Net : XTALIN盡可能短

If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size

	BIOS_ROM_EN GPIO_22_ROM_CSB	BIF_MEM_AP_SIZE [2:0] GPIO_13	GPIO_12	GPIO_11	BIF_VGA_DIS on GPIO_29	TX_HALF_SWING on GPIO_0	TX_DEEMPH_EN on GPIO_20	BIF_GEN3_EN_A on GPIO_2	BIF_CLK_PM_EN on GPIO_9_ROMSO
PULL HIGH	1: Enable external BIOS ROM device	DNI (Internal PU)	DNI	DNI (Internal PU)	1: dGPU does not drive any displays (headless) DEFAULT	1: The transmitter half-swing is enabled	1: Tx de-emphasis enabled DEFAULT	DEFAULT 1: PCIe Gen3 is supported (Internal PU)	1: The CLKREQB power management capability is enabled
PULL LOW	0: Disable external BIOS ROM device. DEFAULT	Install DEFAULT	DNI (Internal PD)	DNI	0: VGA Controller capacity enabled (Internal PD)	DEFAULT 0: The transmitter full swing is enabled (Internal PD)	0: Tx de-emphasis disabled (Internal PD)	0: PCIe Gen3 is not supported	DEFAULT 0: Disabled. (Internal PD)

FOR VRAM SKU Table

	DBGDATA_7	DBGDATA_6	DBGDATA_5	DBGDATA_4	DBGDATA_3	DBGDATA_2	DBGDATA_1	DBGDATA_0	HSYNC	HSYNC	Reserved on GPIO_15	Reserved on GPIO_9_ROMSI
PULL HIGH	11:Set the SMBUS slave address 0x43 10:Set the SMBUS slave address 0x42		BOARD_CONFIG[2:0]=DB[5:3] depend on FX505DY VRAM SKU			DBGDATA[2:0] 111:No usable endpoints 110:One usable endpoint 101:Two usable endpoints 100:Three usable endpoints		DEFAULT:111	1: Special Usage		1: DNI for normal operation	1: DNI for normal operation
PULL LOW	01:Set the SMBUS slave address 0x41 DEFAULT 00:Set the SMBUS slave address 0x40 (Internal PD)		000=SAMSUNG 4G 03008-00050500 001=MICRON 4G 03008-00050400 010=HYNIX 2G 03008-00030700 011=SAMSUNG 2G 03008-00031300 (Internal PD)			011:Four usable endpoints 010:Five usable endpoints 001:Six usable endpoints 000:All endpoints are usable		(Internal PD)	DEFAULT 0: DNI (Internal PD)		0: Default (Internal PD)	0: Default (Internal PD)

SMBus slave address of GPU

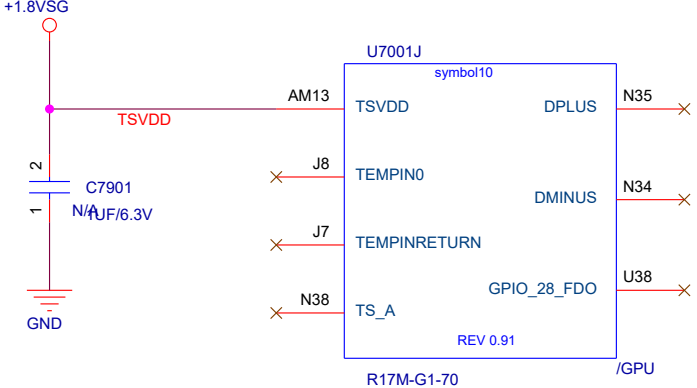
SR SKU Table
000=SAMSUNG 4G 03008-00050500 ------50W BOM
001=MICRON 4G 03008-00050400 ------60W BOM

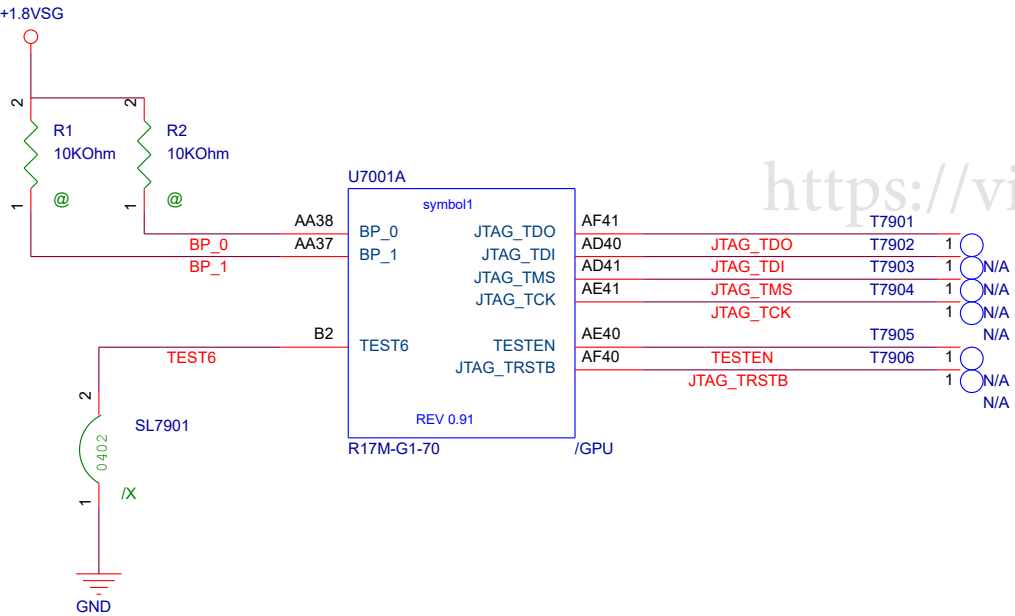
GDDR5 size	BIF_MEM_AP_SIZE [2:0]
128 MB	000
256 MB	001

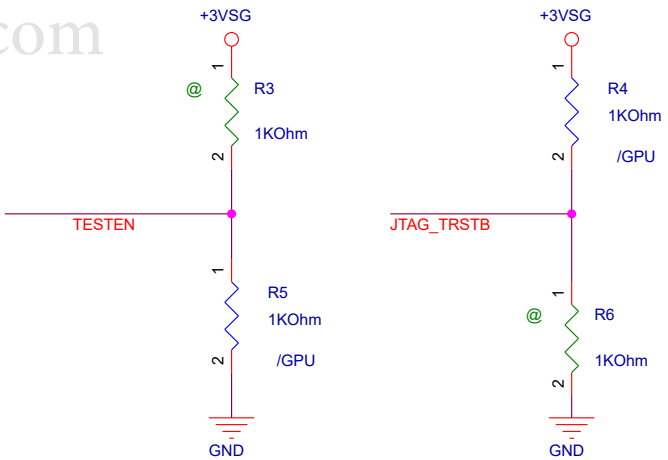
Density		ASUSP/N	Priority	Description	Vendor
VRAM	8G	03008-00050500	1	GDDR5 256M*32 7.0 1.5V FBGA170	SAMSUNG/K4G80325FB-HC28	Samsung
		03008-00050800	2	GDDR5 256*32 7.0 1.5V FBGA170	MICRON/MT51J256M32HF-70:A	Micron
	2G	03008-00030700	1	GDDR5 128M*32 7.0 1.5V BGA170	HYNIX/H5GC4G63AMR-R0C	HYNIX
		03008-00031300	2	GDDR5 128M*32 7.0 1.5V FBGA170	SAMSUNG/K4G41325FE-HC28	Samsung

GPU : Set the SMBUS slave address 0x41

Project Name	X550IU
Rev	R1.0
Title :	DGPU_GPIO85/mpa8/CLK
Size	D
Dept.:	ASUSTek Computer Inc.
Engineer:	RD1/EE2
Date:	Thursday, November 29, 2018
Sheet	78 of 103

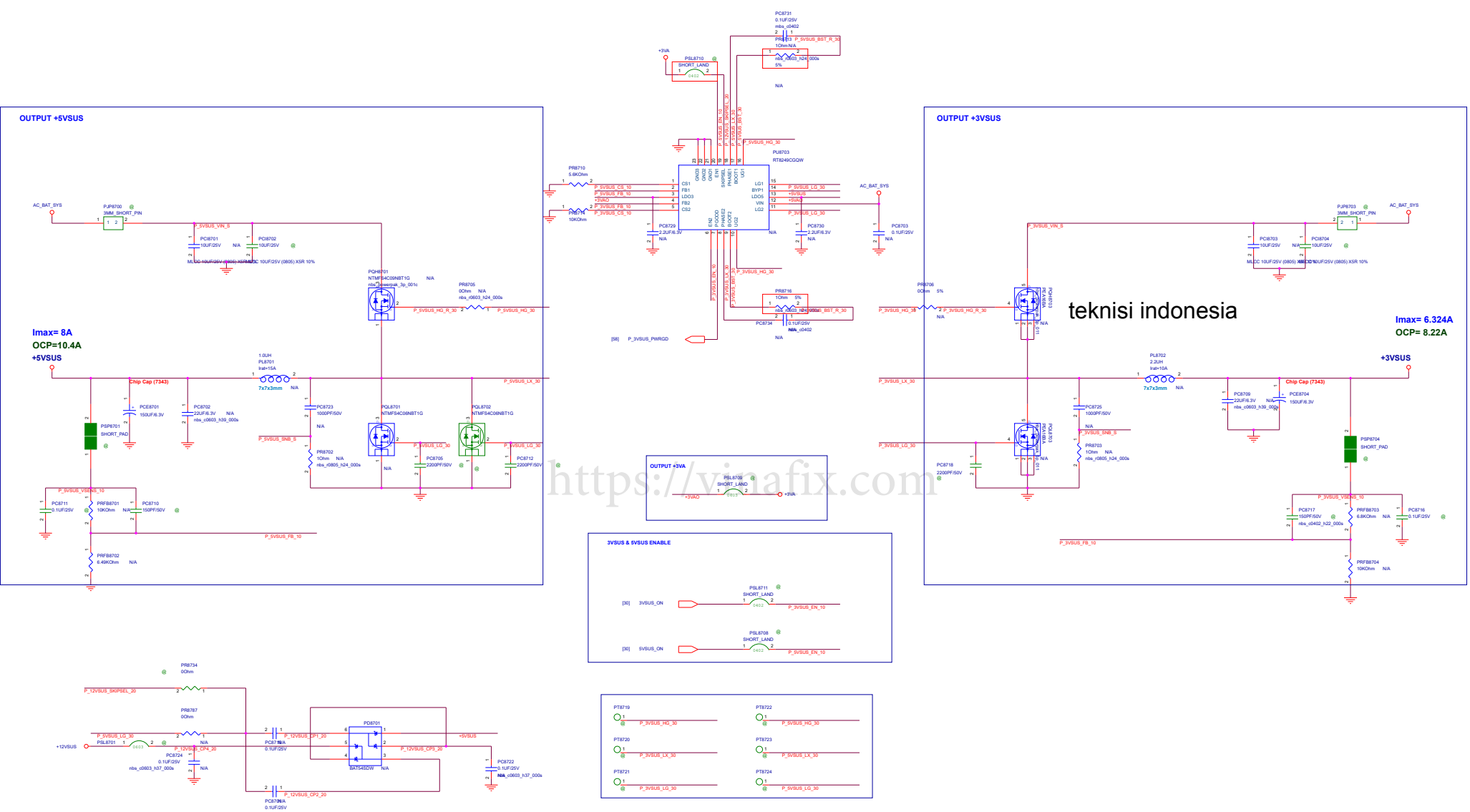




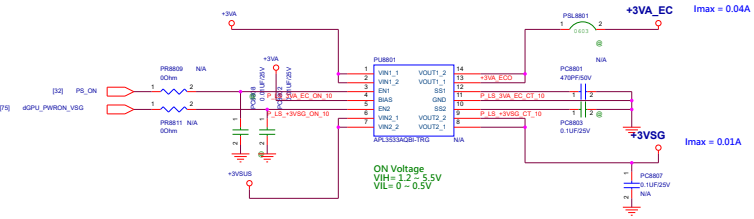


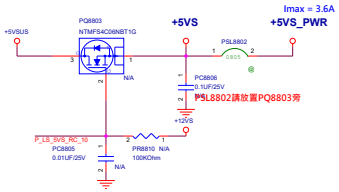
Project Name: X550IU		Rev: R1.0
Title : DGPU_Debug&Thermal		
Size: A	Dept.: ASUSTek Computer Inc.	Engineer: RD1/EE2
Date: Thursday, November 29, 2018	Sheet 79 of 103	

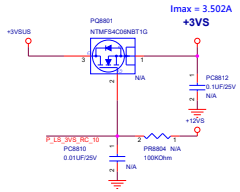
+3VA_DSW / +5VSUS [System Power]

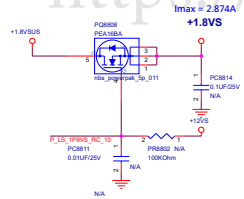


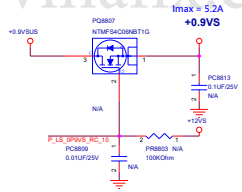
Load Switch

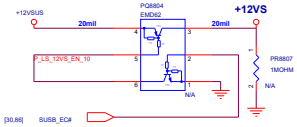








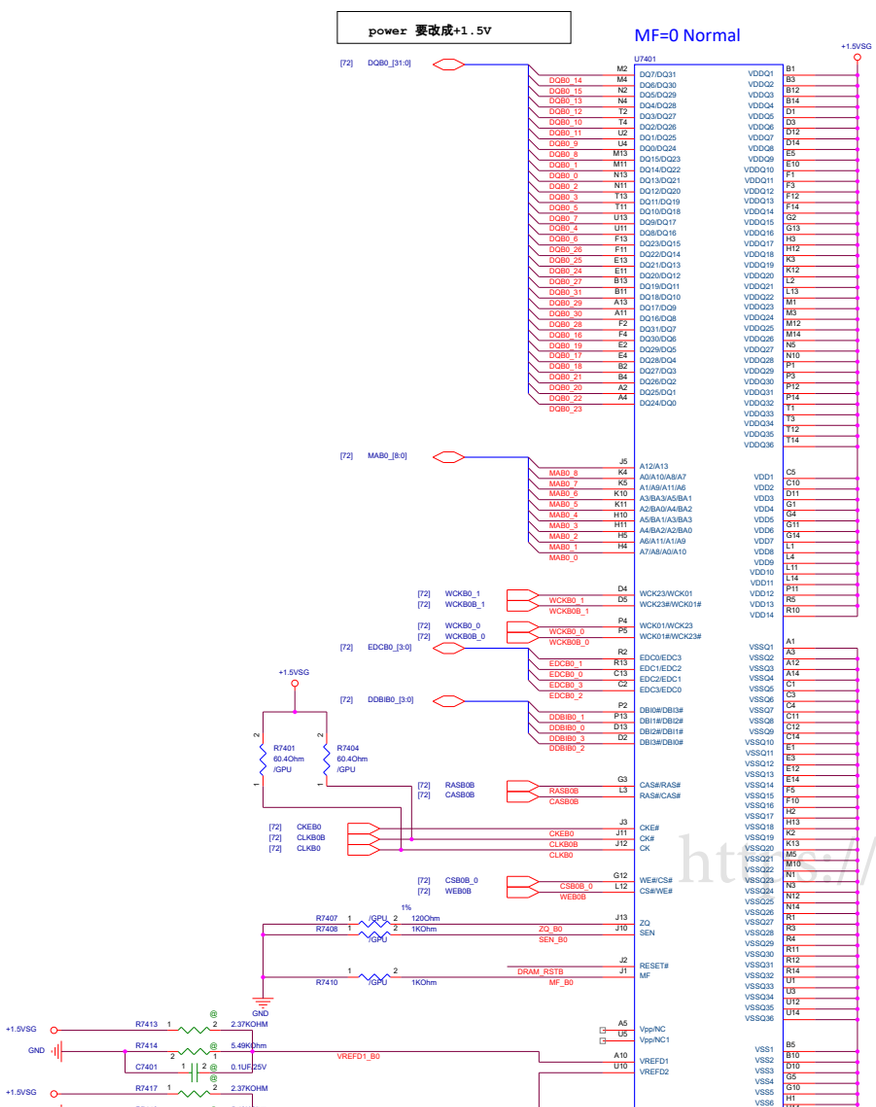


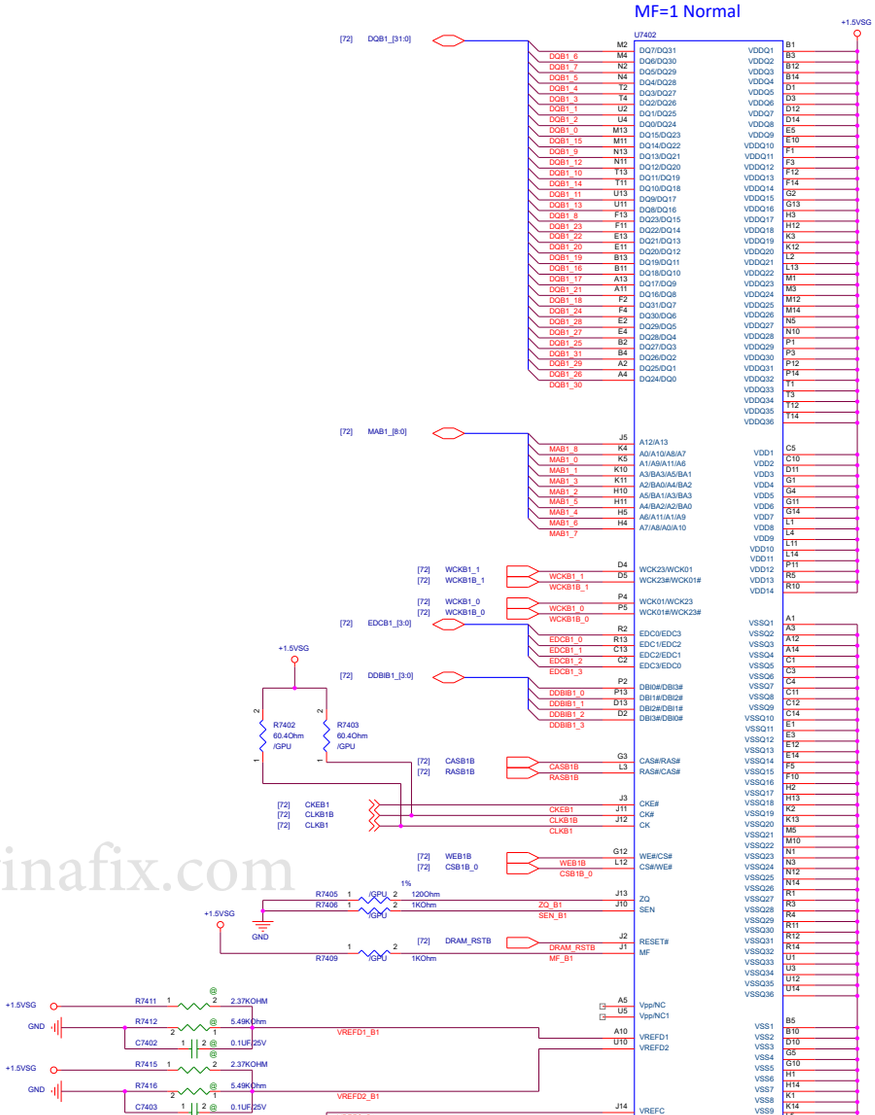


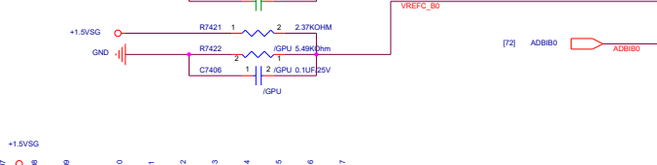
ASUS	Project Name: FX505DY		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A2	Dept.: NB Power team	Engineer: CS Lin	
Date: Thursday, November 29, 2018	Sheet 88 of 103		

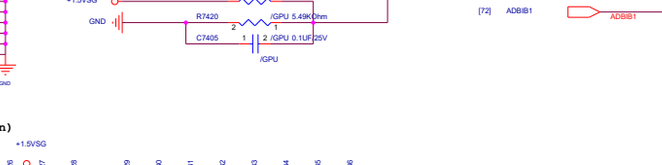
FBA Partition Memory (1 of 2)

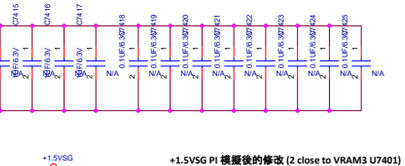
FBA Partition Memory (2 of 2)

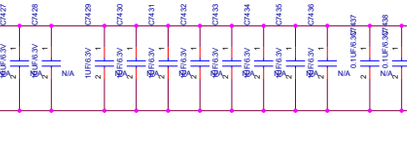








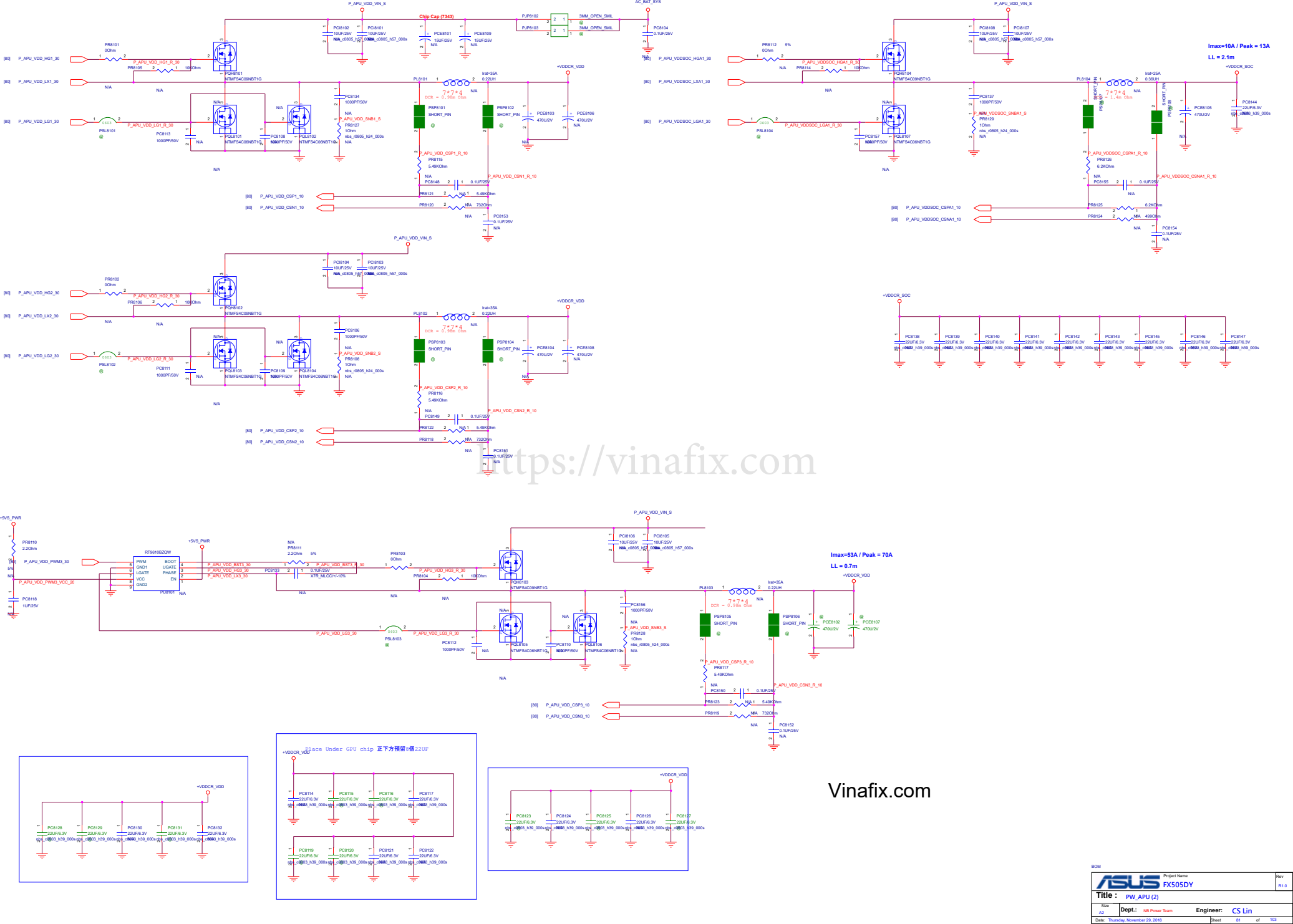


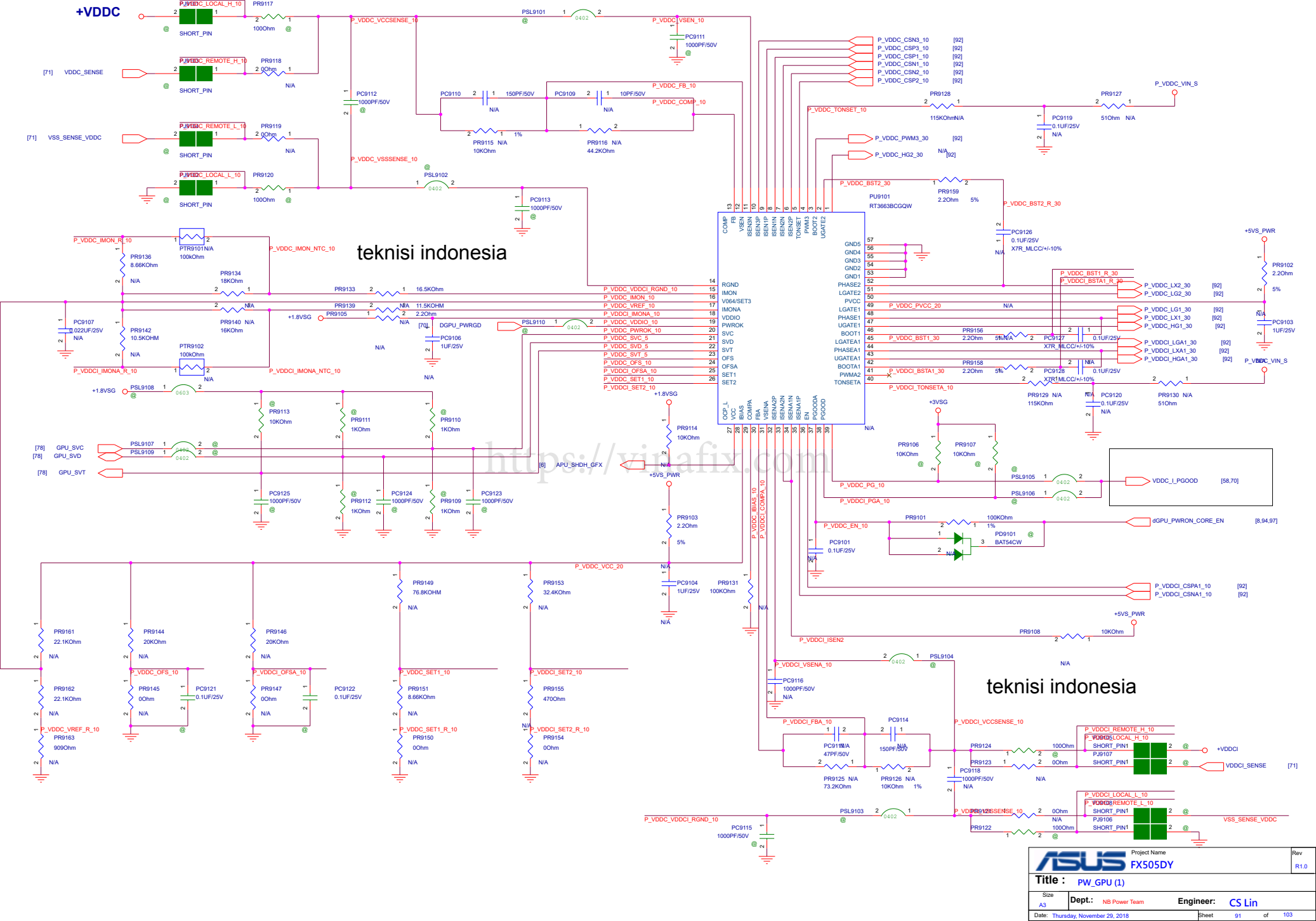


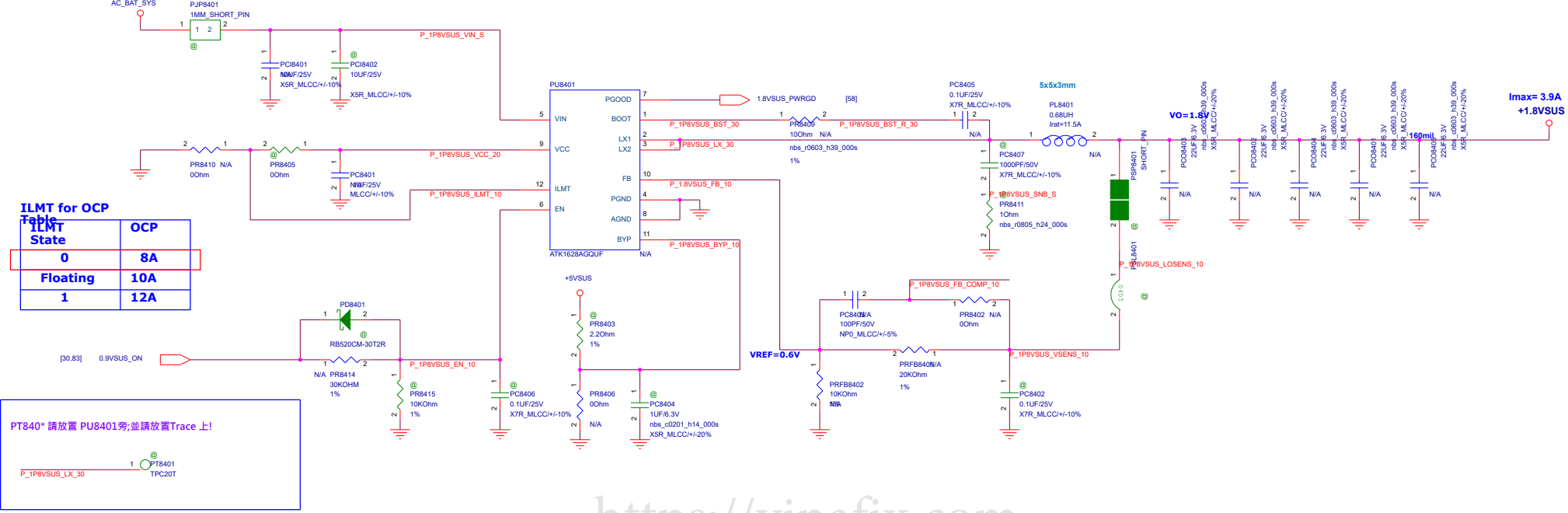
GDDR5 256x32_7.0G (8Gb)

Priority	Company	Model Name	Base		Voltage	Speed	MP Schedule	ASUS P/N
1	Samsung	K4G80325FB-HC28	Samsung	256x32	1.35V/1.55V	6.0G/7.0G	MP	03008-00050000
2	Micron	MT51J256M32HF-70:A	Micron	256x32	1.35V/1.5V	6.0G/7.0G	MP	03008-00050400

ASUS	Project Name: X550IU		Rev: R1.0
Title : DGPU_GDDR5_2			
Size: Custom	Dept.: ASUSTek Computer Inc.	Engineer: RD1/EE2	
Date: Thursday, November 29, 2018	Sheet 74 of 103		

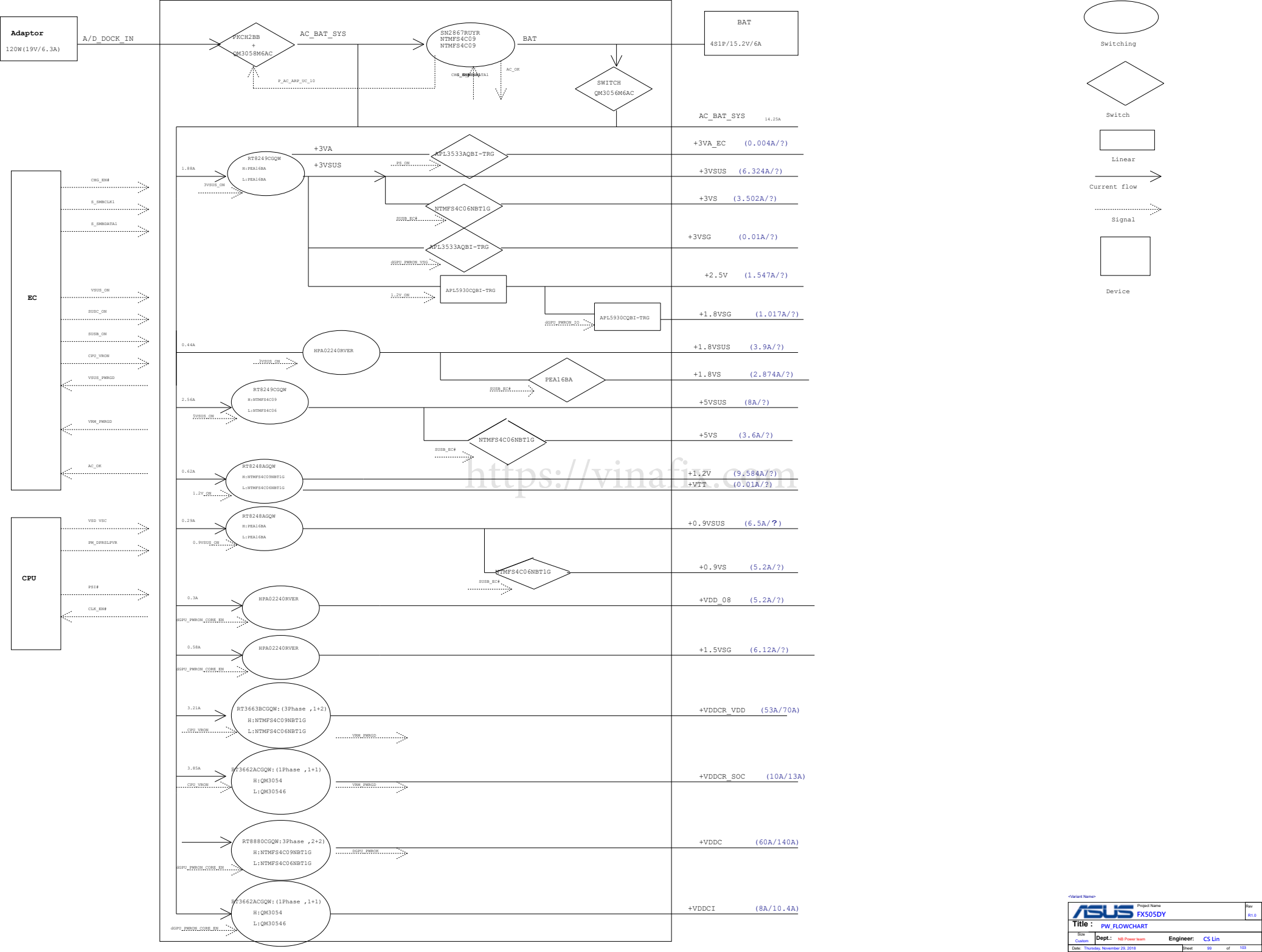

Imax=10A / Peak = 13A
LL = 2.1m
Imax=53A / Peak = 70A
LL = 0.7m
Place Under GPU chip 正下方預留8個22UF
https://vinafix.com
Vinafix.com
ASUS
Project Name
FX505DY
Rev
R1.0
Title : PW_APU (2)
Size
A2
Dept.: NB Power Team
Engineer: CS Lin
Date: Thursday, November 29, 2018
Sheet 81 of 103


+VDDC
teknisi indonesia
teknisi indonesia
https://vinafix.com
PU9101
RT3663BCGQW
Project Name
FX505DY
Rev
R1.0
Title : PW_GPU (1)
Size
A3
Dept.: NB Power Team
Engineer: CS Lin
Date: Thursday, November 29, 2018
Sheet 91 of 103



<Variant Name>

Project Name: FX505DY		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Thursday, November 29, 2018	Sheet 84 of 103	



<Variant Name>

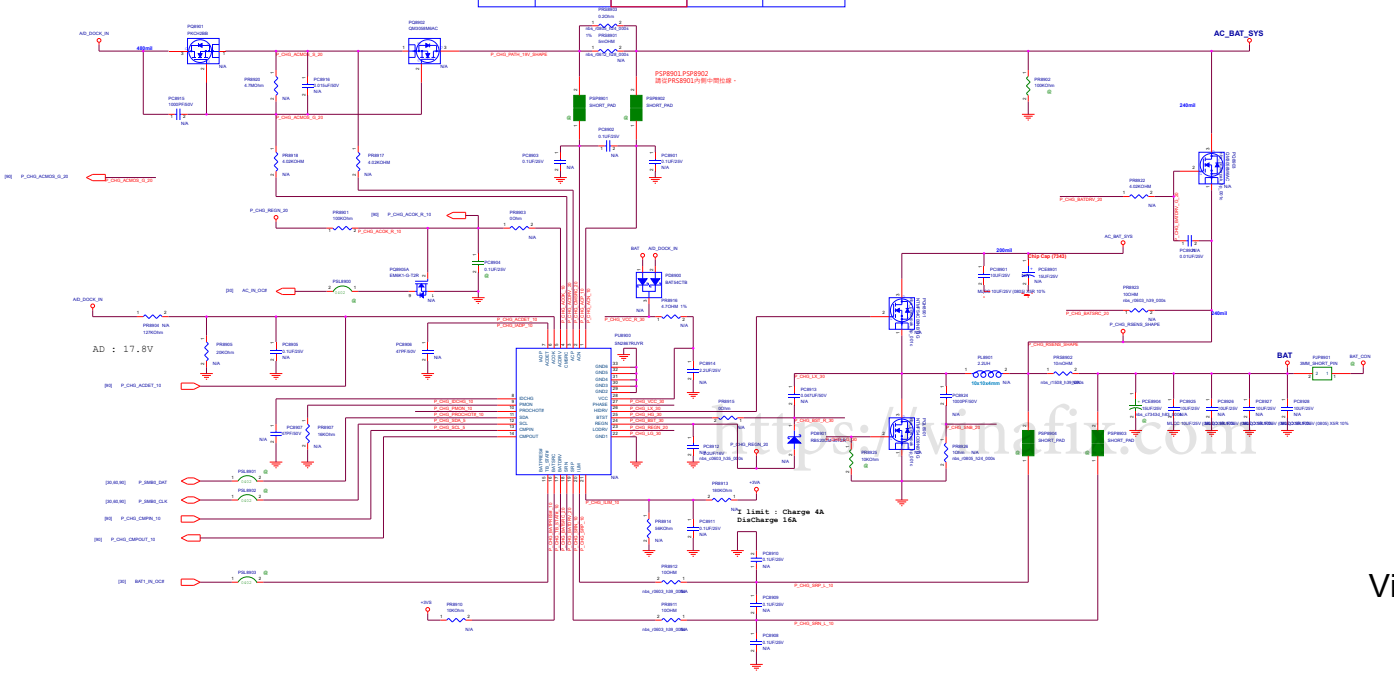
ASUS	Project Name: FX505DY	Rev: R1.0
Title : PW_FLOWCHART		
Size: Custom	Dept.: NB Power team	Engineer: CS Lin
Date: Thursday, November 29, 2018	Sheet 99 of 103	

Main Board

ASUS	Project Name: FX505DY	Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date: Thursday, November 29, 2018	Sheet 102 of 103	

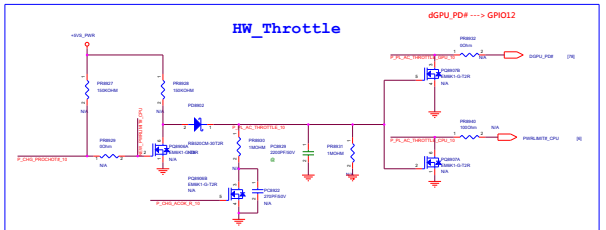
PRS8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	1002150820511010	10114-00221000	x	x	x	10114-00211000

PRS8901	<=150W	<=280W	>280W	>330W
	10m	5m	1m	2m
	1002150811151111	10125-00088100	10108-00088000	10108-00088000



Adaptor select
total power = 90% ADP

Adaptor select			
	M Series	S Series	
PR8921	10m		5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	400W



ASUS	Project Name: FX505DY		Rev: R1.0
Title :	PW_CHARGER		
Size: A2	Dept.: MB Power Team	Engineer: CS Lin	
Date: Thursday, November 29, 2018	Sheet: 85	of: 103	

PROTECTION

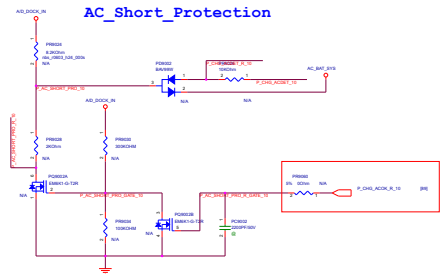
Address Selection Table

Address	0x72	0x74	0x76	0x78	0x7A	0x7C	0x7E	0x80
PR9001	10k	1.5k	0k	0.5k	3.9k	6.5k	5.1k	8k
PR9002	Open	8.2k	4.2k	2.5k	6.7k	5.6k	2.7k	2k

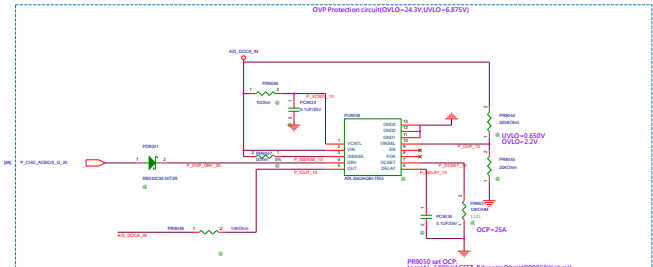
Register Address

Address	0x01	0x11	0x12	0x13	0x14	0x15	0x16
R/W	R	R	R	R	R	R	R
Function	Temp. alert threshold setting		Sensed temp. data				bit 0 = 2 bit 1 = 1 bit 6 = 1 When ALERT# asserts

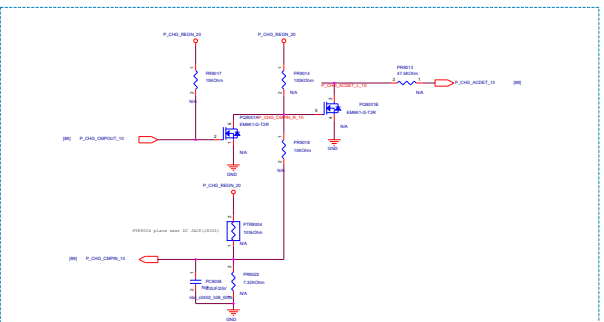
AC_Short_Protection



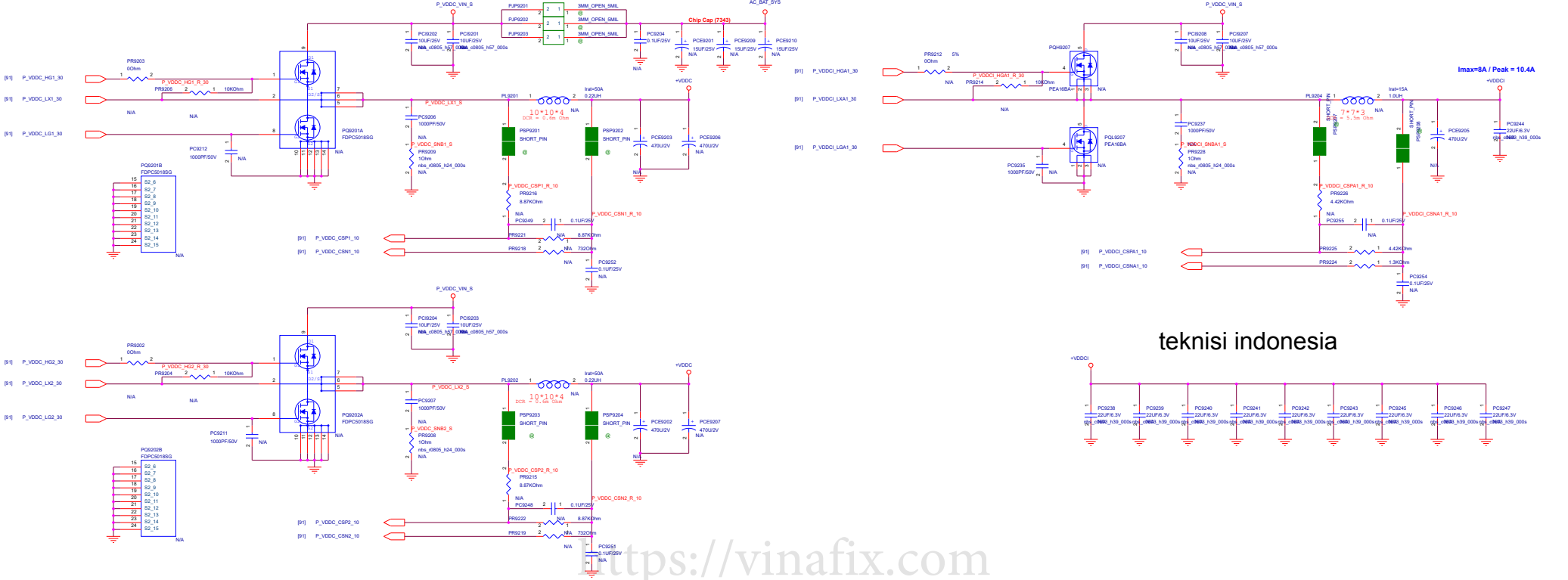
OVP Protection circuit(OVLO=24.3V,UVLO=6.875V)



PR9050 set OCP:
Iocp(A)=1000/(ACFET_Rdson(mOhm)*PR9050(Kohm))
design Iocp=~1.2*ACFET_Icont (10ms latch)
1.5*Iocp (latch immediately)
Design precaution: Iocp must not trigger Adapter 200% protection
Ex: Adapter 90W / 19V = 4.74A, ACFET 1A cont
Iocp design at 21A*1.2=25.2A =>~ 1.5*Iocp=37.8A
1.5*Iocp > Adapter 200% rating



<Variant Name>
ASUS Project Name: FX506DY
Rev: 01.0
Title: PW_PROTECTION
Size: A3
Dept.: NB Power Team
Engineer: CS Lin
Date: Thursday, November 29, 2018
Sheet 60 of 100

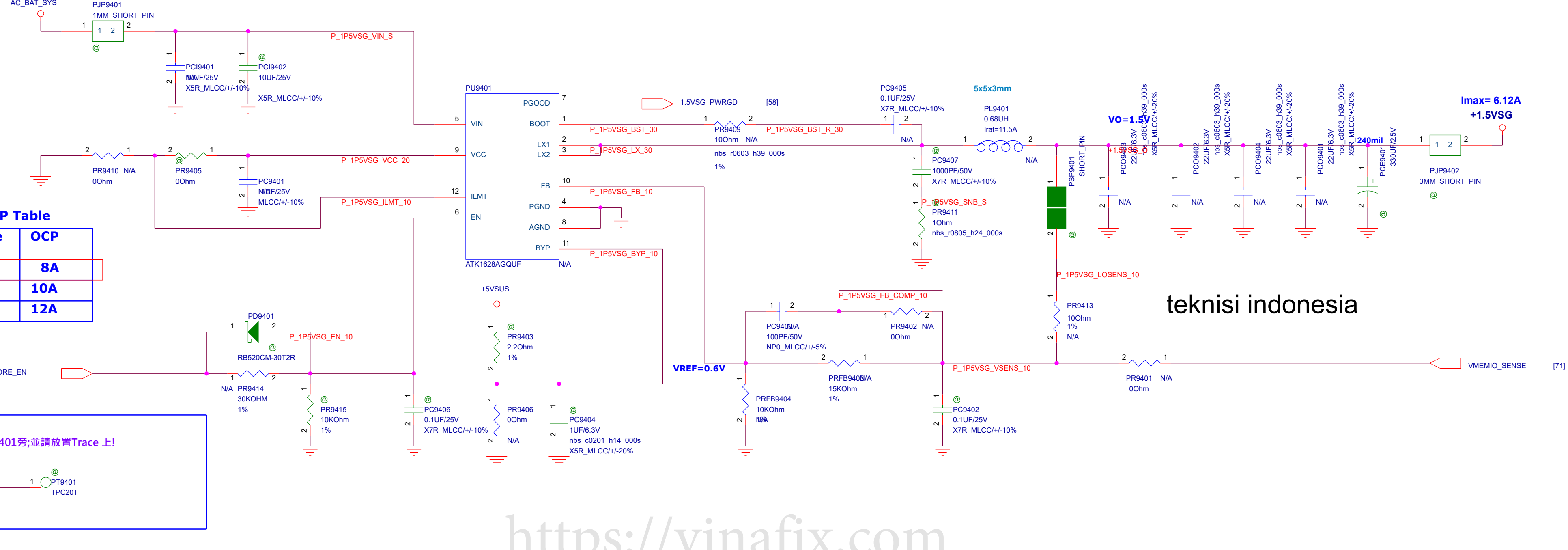


BOM

ASUS	Project Name: FX505DY	Rev: R1.0
Title : PW_GPU (2)		
Size: A2	Dept.: NB Power Team	Engineer: CS Lin
Date: Thursday, November 29, 2018	Sheet 92 of 103	

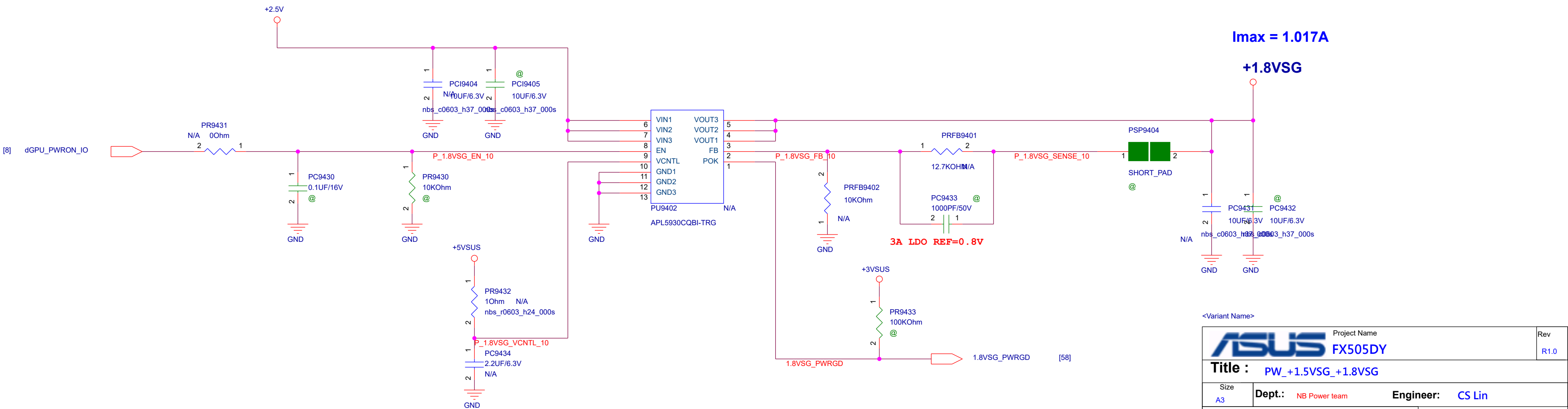
ILMT for OCP Table

ILMT State	OCP
0	8A
Floating	10A
1	12A



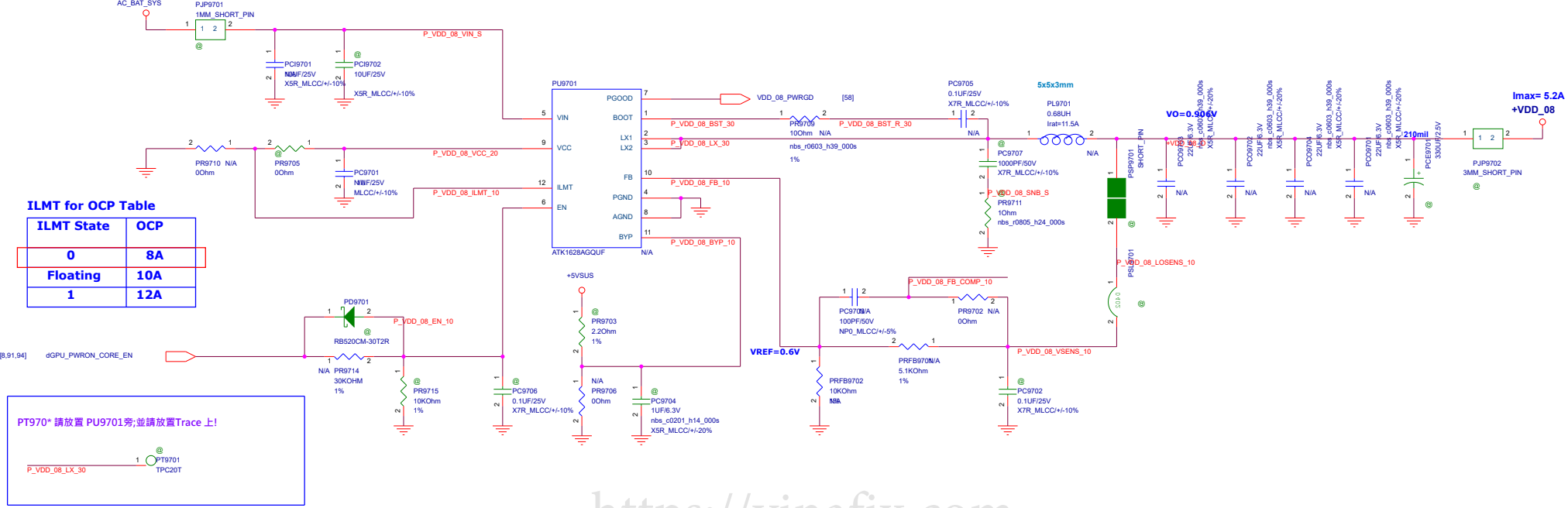
PT940* 請放置 PU9401旁;並請放置Trace 上!

P_1P5VSG_LX_30 — PT9401 TPC20T



<Variant Name>

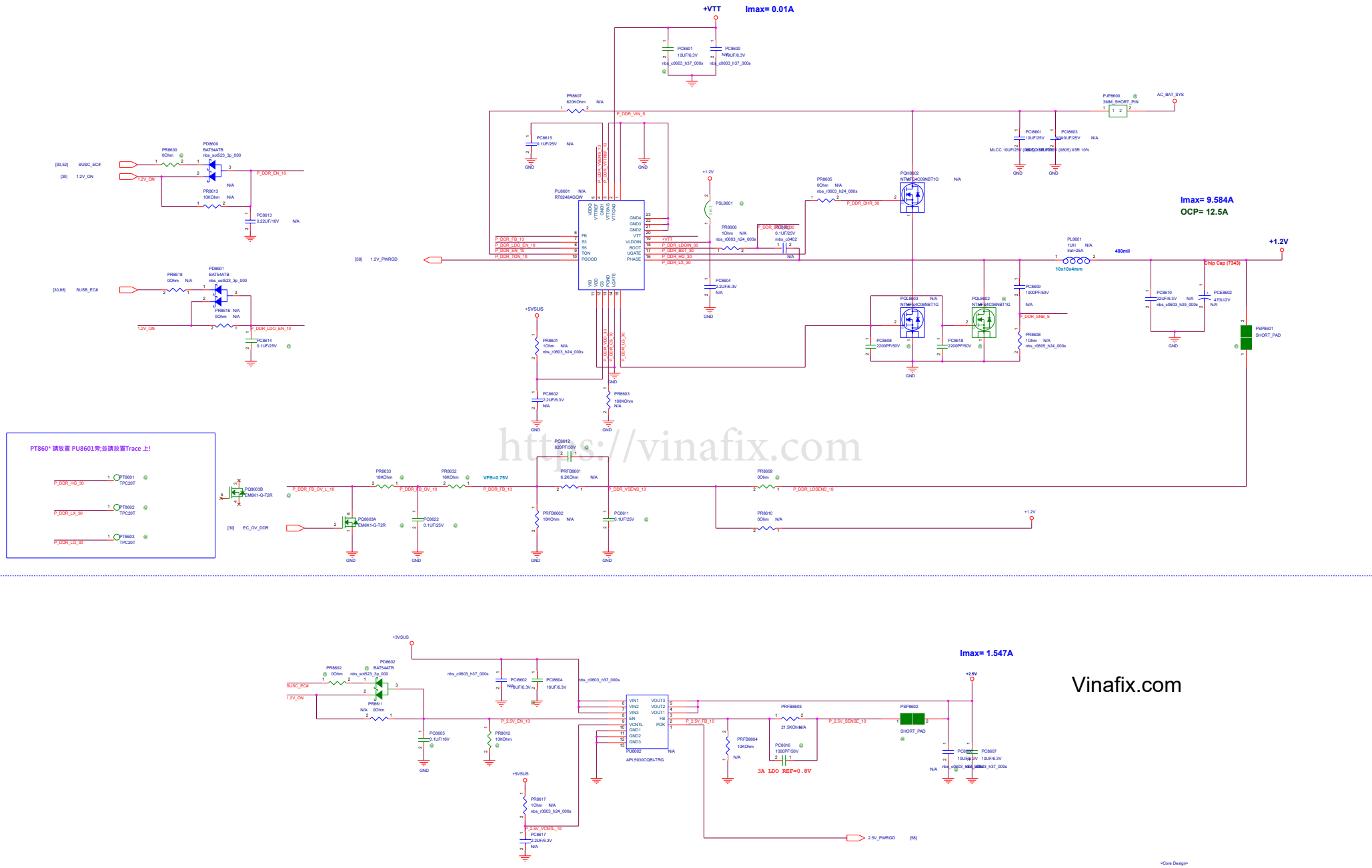
ASUS	Project Name: FX505DY	Rev: R1.0
Title :	PW_+1.5VSG_+1.8VSG	
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Thursday, November 29, 2018	Sheet 94 of 103	



<Variant Name>

Project Name: FX505DY		Rev: R1.0
Title : PW_+VDD_08		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Thursday, November 29, 2018	Sheet 97 of 103	

+1.2V / +VTT / +2.5V[For Memory]



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<Core Design>

ASUS	Project Name: FX505DY	Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V		
Size: A2	Dept.: NB Power team	Engineer: CS Lin
Date: Thursday, November 29, 2018	Sheet: 86 of 103	

ASUS	Project Name: FX505DY	Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date: Thursday, November 29, 2018	Sheet 103 of 103	