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MS-7A64

ATX

Ver: 11

Intel -Kabylake plamform B250/H270

CPU:

kabylake-S

System Chipset:

B250/H270

Onboard Chip:

HD Audio Codec:ALC1220
LAN:INTEL I219
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X4) Slot *1*
*PCI Express (X1) Slot * 2*
*PCI Slot * 2*
*M2 * 2*

Other:

SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 (B250*2/H270*4)*
*REAR USB2.0 *2*
REAR USB TYPE A+C

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MS-7A64..

Size: Custom | Document Description: Cover Sheet | Rev: 11

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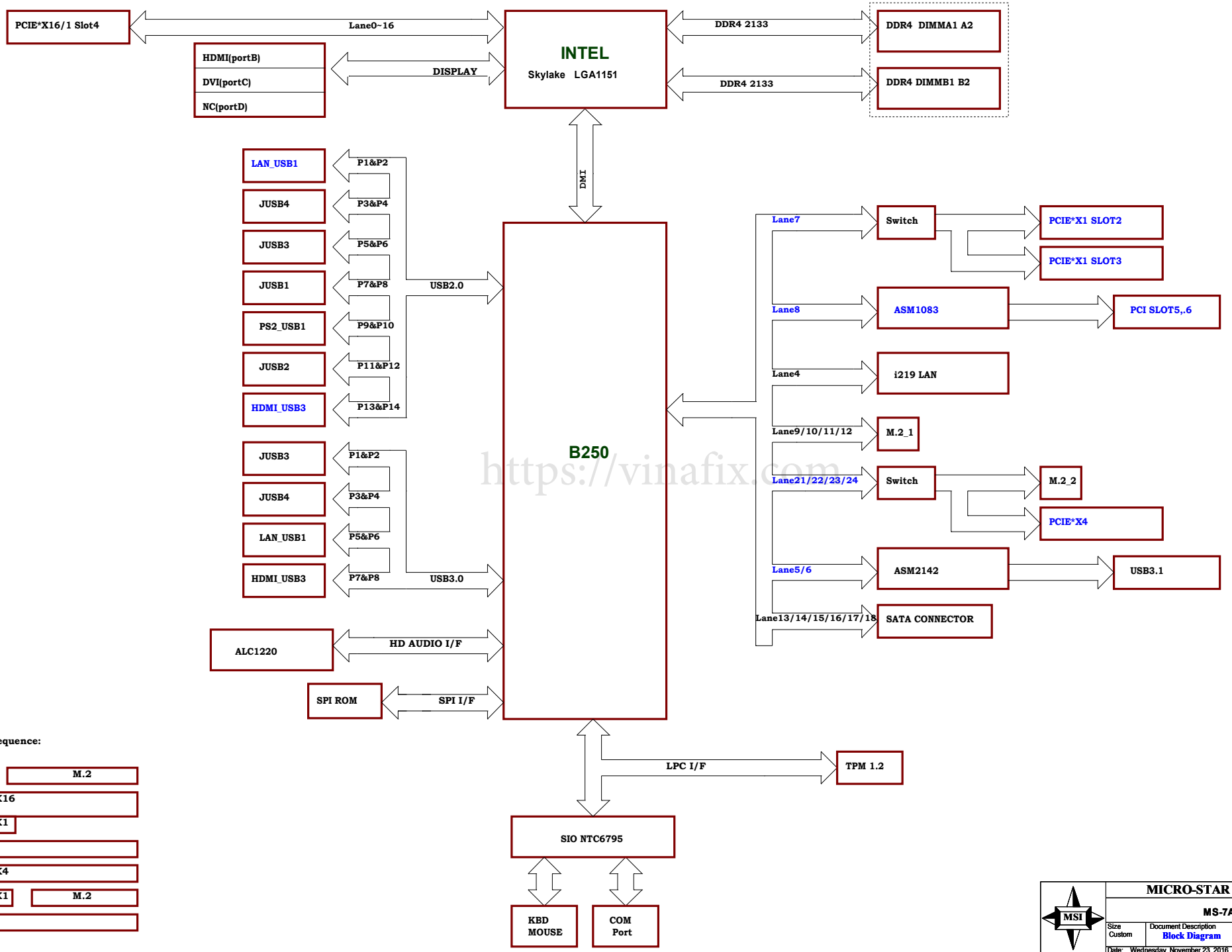
MS-7A64 Block Diagram



Slot Sequence:

- M.2
- PCIE X16
- PCIE X1
- PCI
- PCIE X4
- PCIE X1 / M.2
- PCI

MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: Block Diagram
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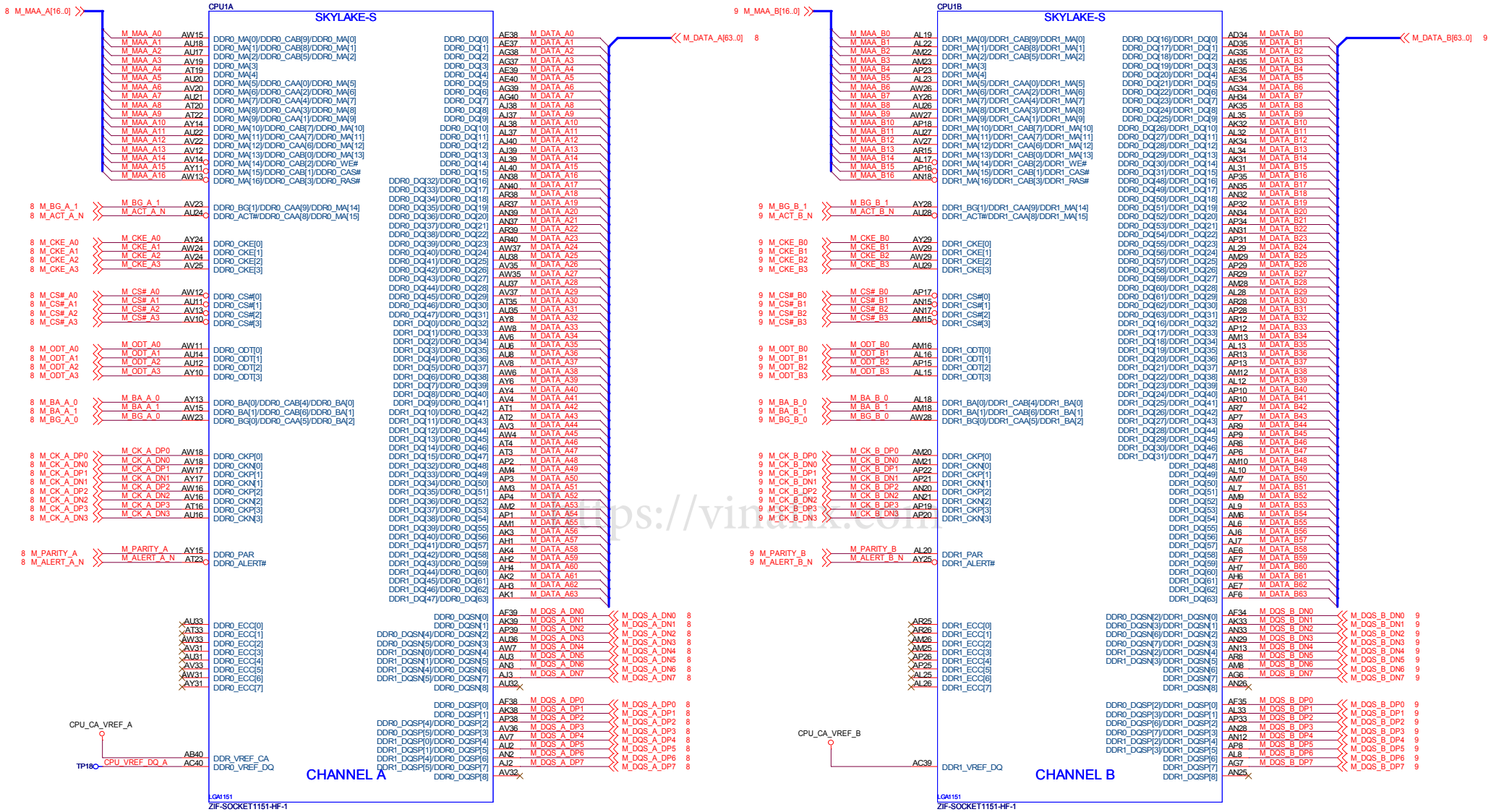

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size	Document Description	Rev
Custom	CPU-Memory	11

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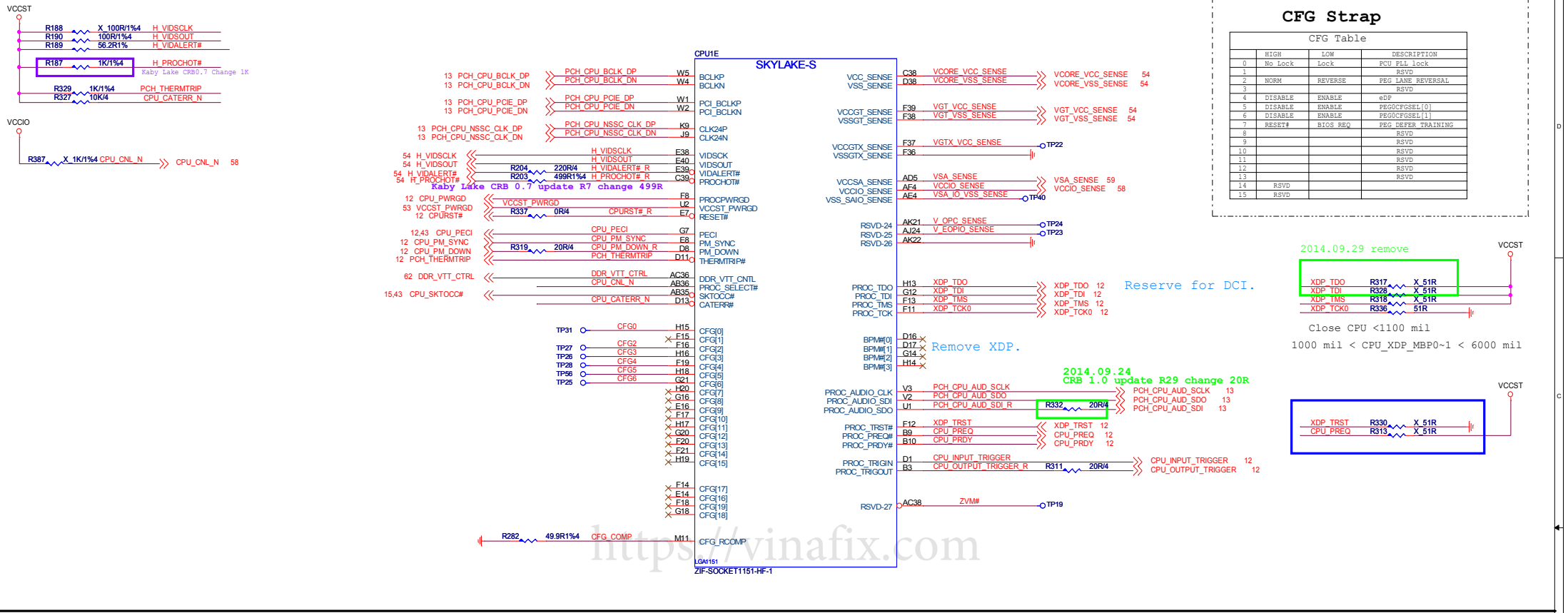
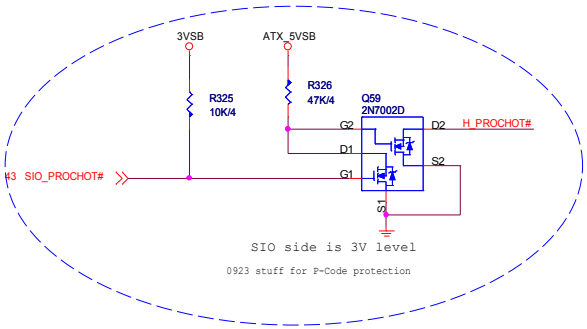


CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU_PLL_lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU_PLL_lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size: Custom | Document Description: CPU-Control/MISC/CFG/Audio | Rev: 11

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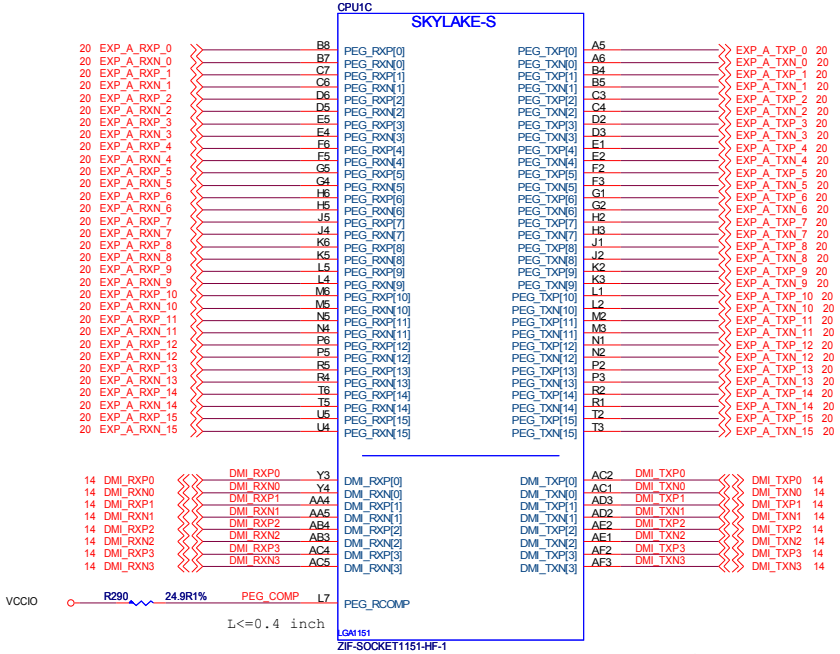

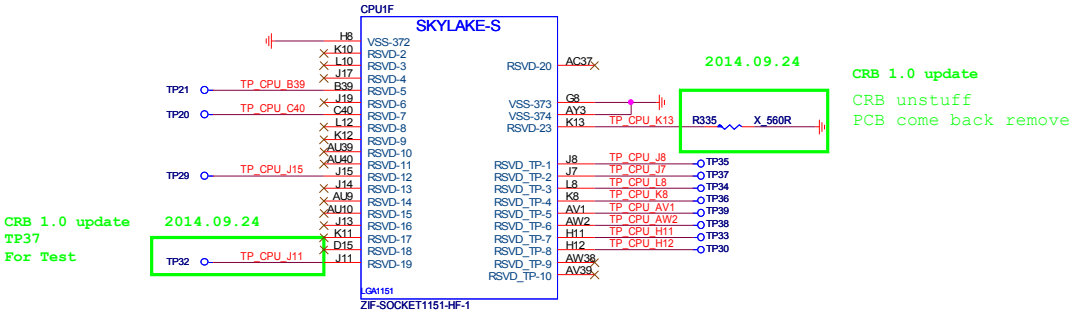

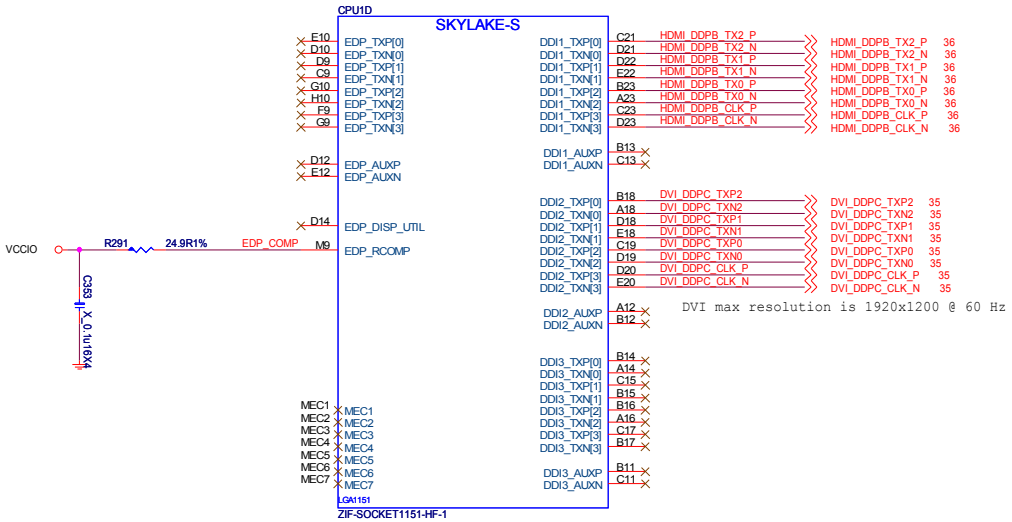

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	MS-7A64..	
Size: Custom	Document Description: CPU-PEG/Display	Rev: 11
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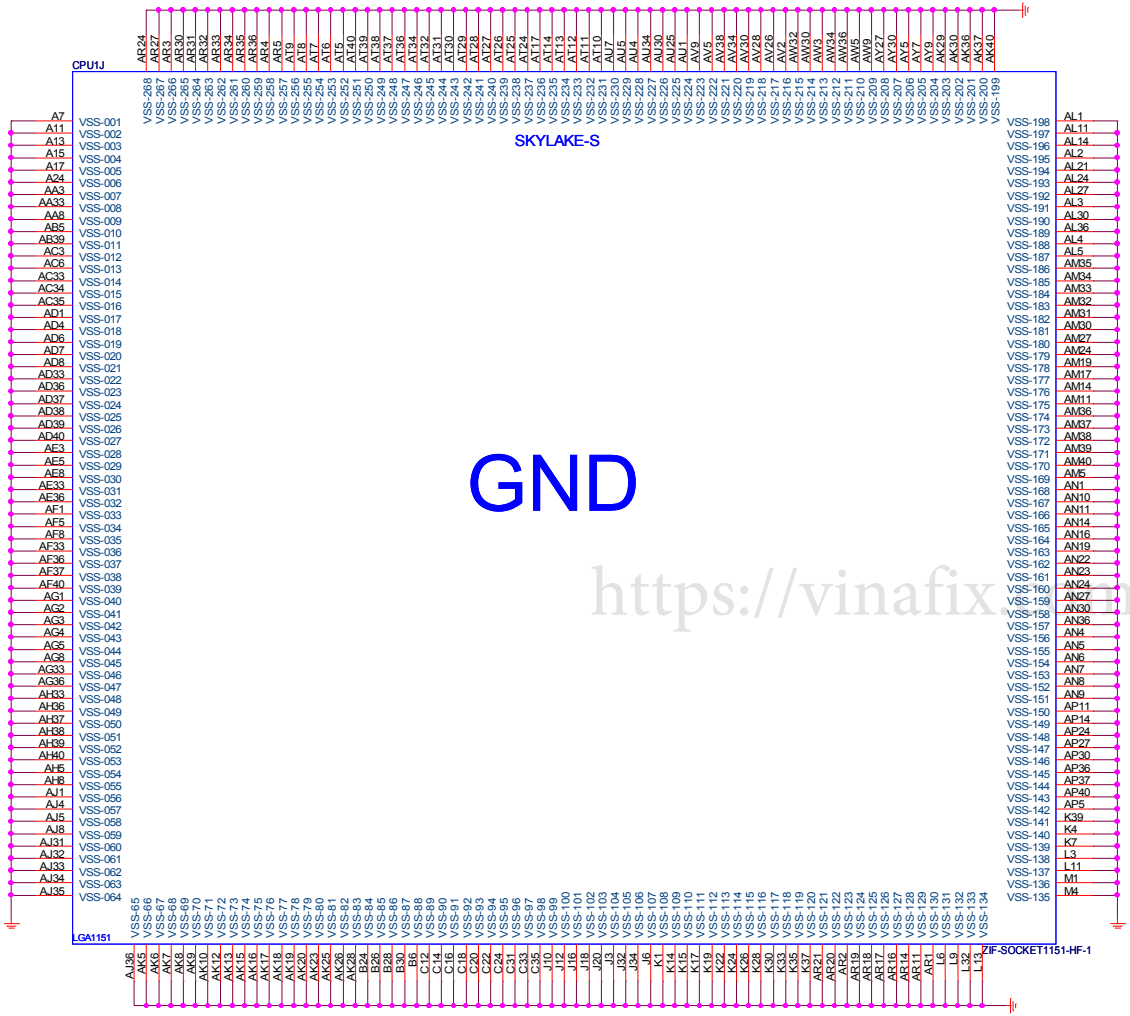

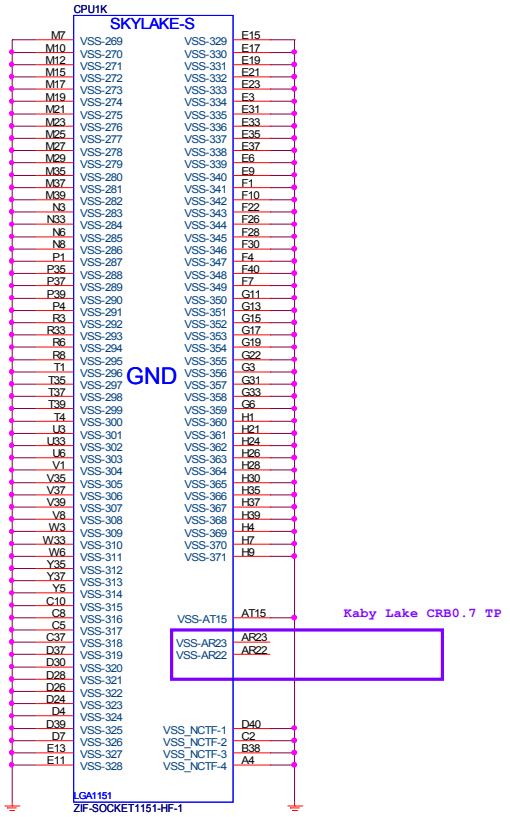

MICRO-STAR INT'L CO.,LTD			
MS-7A64..			
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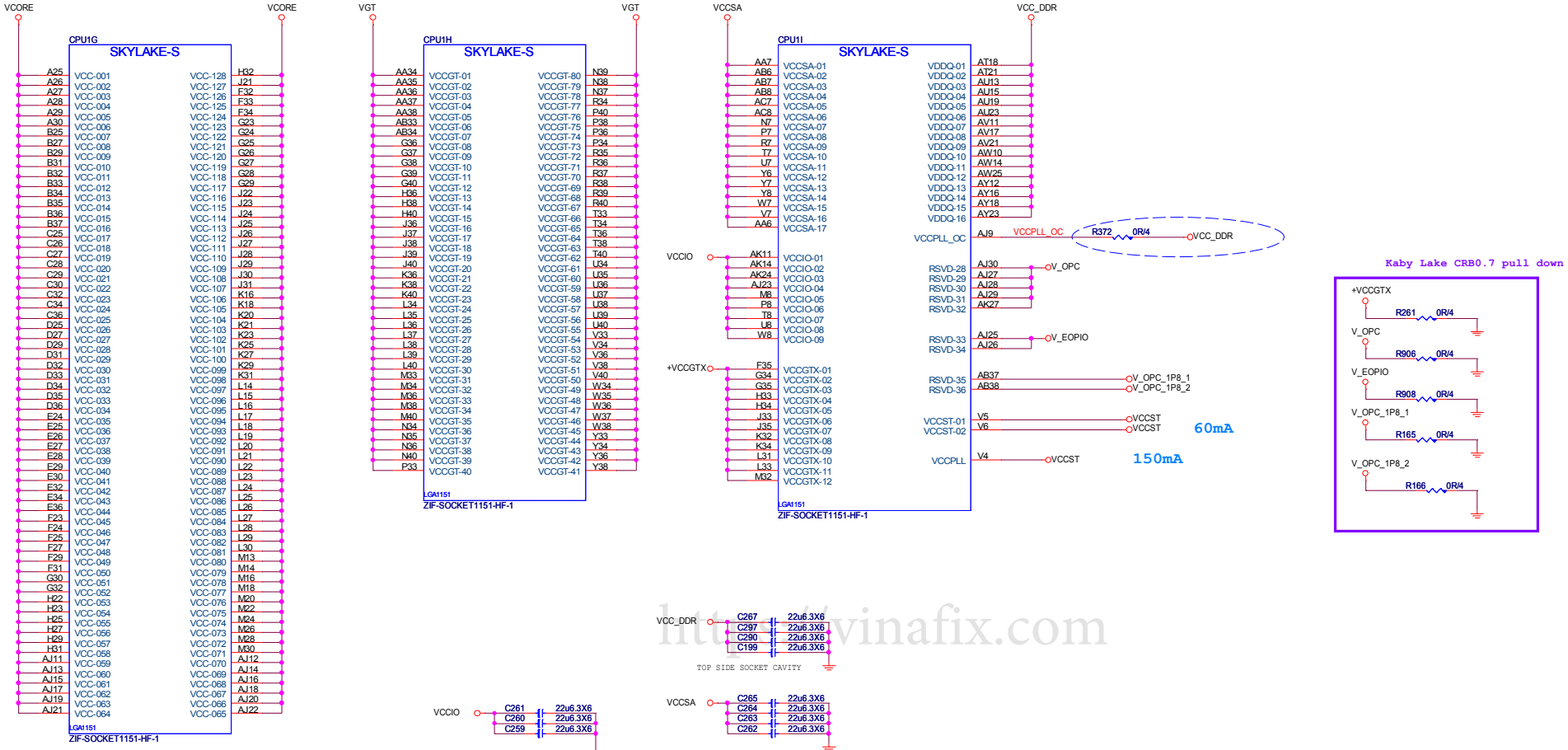
Date: Wednesday, November 23, 2016		Sheet 6 of 69	



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Size: Custom	Document Description: CPU-Power
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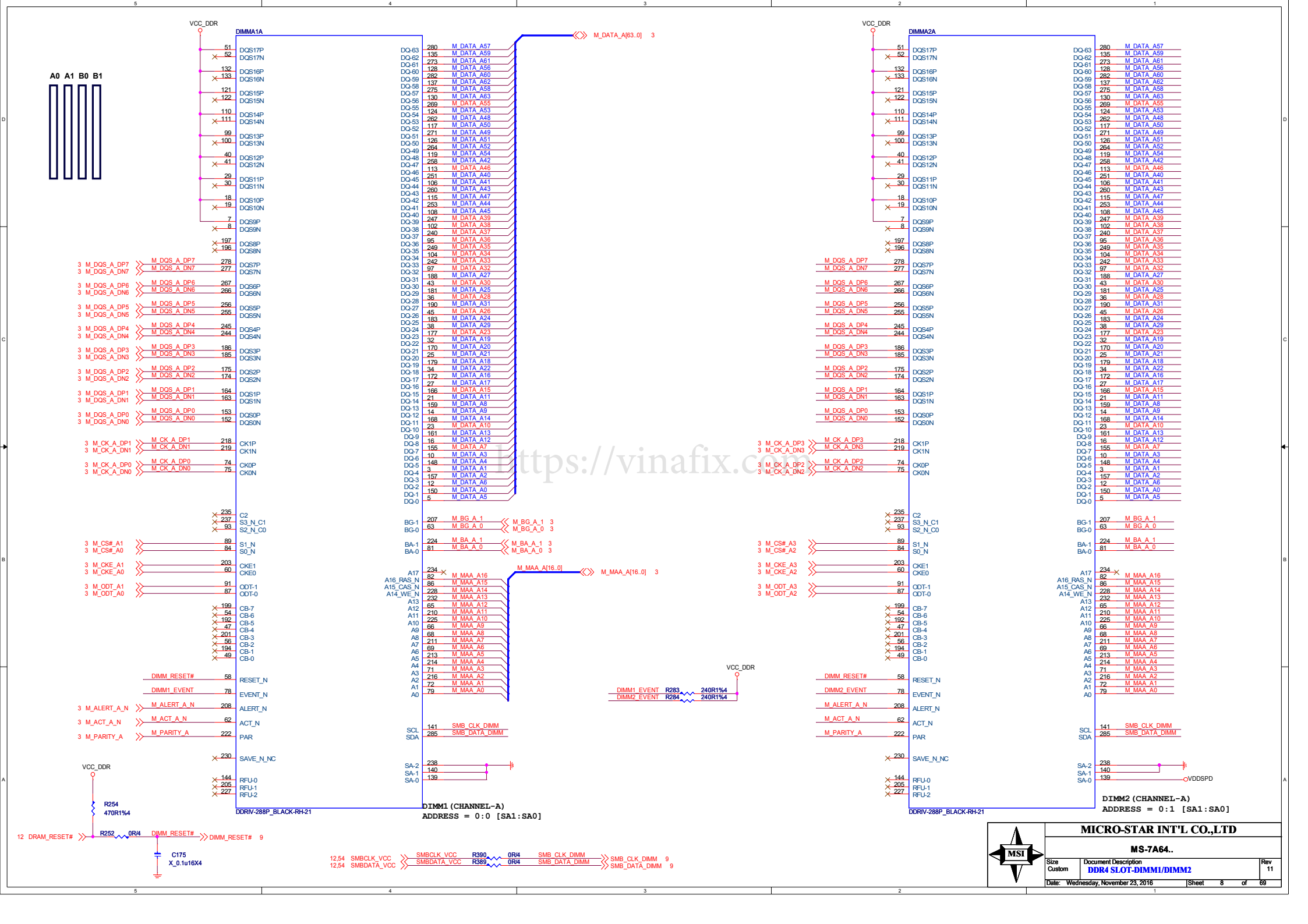

MICRO-STAR INT'L CO.,LTD	
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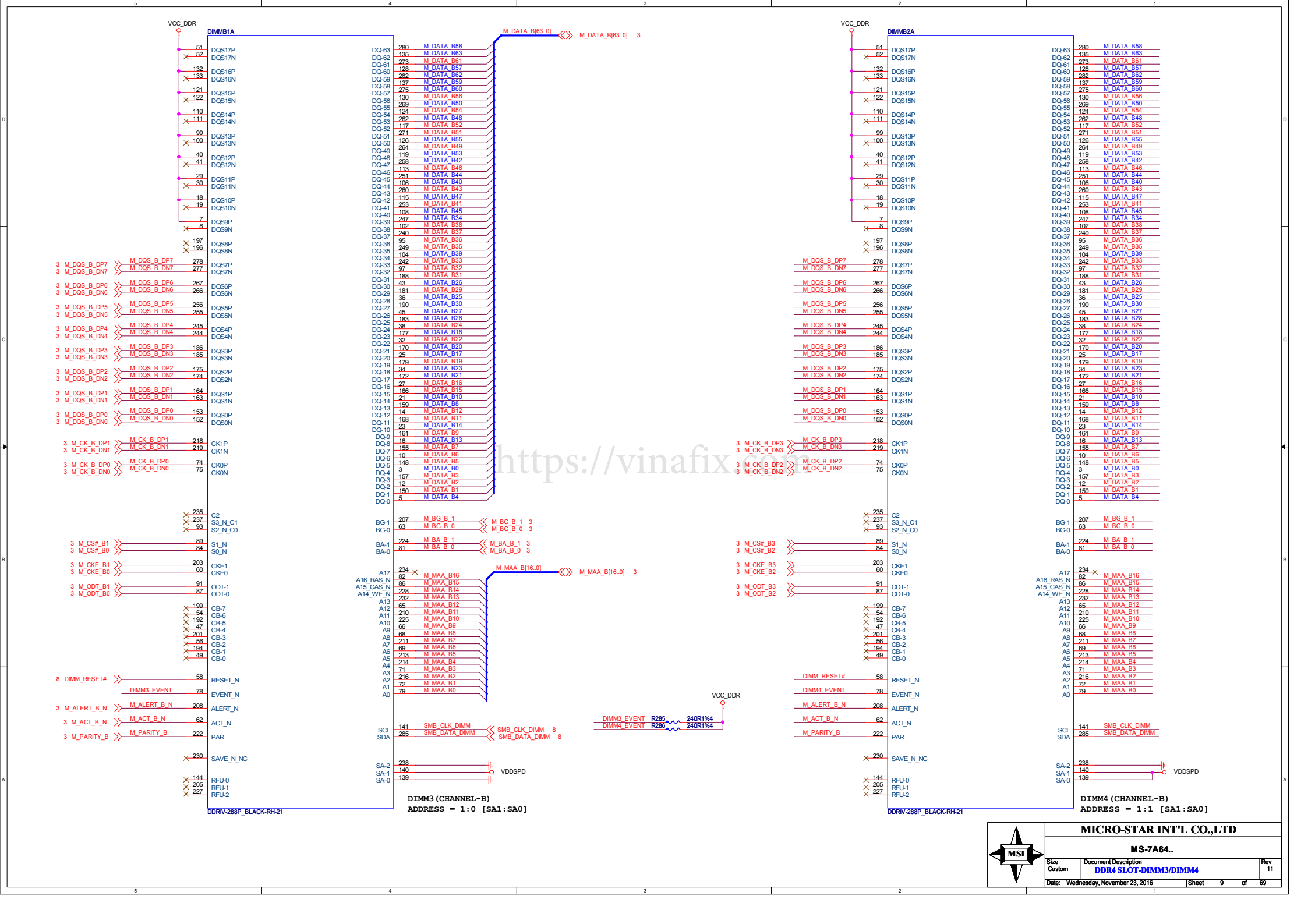
Rev: 11	
Date: Wednesday, November 23, 2016	Sheet 8 of 69


VCC_DDR
DIMMB1A
M_DATA_B[63..0]
M_DATA_B[63..0] 3
DQS17P
DQS17N
DQS16P
DQS16N
DQS15P
DQS15N
DQS14P
DQS14N
DQS13P
DQS13N
DQS12P
DQS12N
DQS11P
DQS11N
DQS10P
DQS10N
DQS9P
DQS9N
DQS8P
DQS8N
M_DQS_B_DP7
M_DQS_B_DN7
DQS7P
DQS7N
M_DQS_B_DP6
M_DQS_B_DN6
DQS6P
DQS6N
M_DQS_B_DP5
M_DQS_B_DN5
DQS5P
DQS5N
M_DQS_B_DP4
M_DQS_B_DN4
DQS4P
DQS4N
M_DQS_B_DP3
M_DQS_B_DN3
DQS3P
DQS3N
M_DQS_B_DP2
M_DQS_B_DN2
DQS2P
DQS2N
M_DQS_B_DP1
M_DQS_B_DN1
DQS1P
DQS1N
M_DQS_B_DP0
M_DQS_B_DN0
DQS0P
DQS0N
M_CK_B_DP1
M_CK_B_DN1
CK1P
CK1N
M_CK_B_DP0
M_CK_B_DN0
CK0P
CK0N
C2
S3_N_C1
S2_N_C0
M_CS#_B1
M_CS#_B0
S1_N
S0_N
M_CKE_B1
M_CKE_B0
CKE1
CKE0
M_ODT_B1
M_ODT_B0
ODT-1
ODT-0
CB-7
CB-6
CB-5
CB-4
CB-3
CB-2
CB-1
CB-0
DIMM_RESET#
RESET_N
DIMM3_EVENT
EVENT_N
M_ALERT_B_N
ALERT_N
M_ACT_B_N
ACT_N
M_PARITY_B
PAR
SAVE_N_NC
RFU-0
RFU-1
RFU-2
DQ-63
DQ-62
DQ-61
DQ-60
DQ-59
DQ-58
DQ-57
DQ-56
DQ-55
DQ-54
DQ-53
DQ-52
DQ-51
DQ-50
DQ-49
DQ-48
DQ-47
DQ-46
DQ-45
DQ-44
DQ-43
DQ-42
DQ-41
DQ-40
DQ-39
DQ-38
DQ-37
DQ-36
DQ-35
DQ-34
DQ-33
DQ-32
DQ-31
DQ-30
DQ-29
DQ-28
DQ-27
DQ-26
DQ-25
DQ-24
DQ-23
DQ-22
DQ-21
DQ-20
DQ-19
DQ-18
DQ-17
DQ-16
DQ-15
DQ-14
DQ-13
DQ-12
DQ-11
DQ-10
DQ-9
DQ-8
DQ-7
DQ-6
DQ-5
DQ-4
DQ-3
DQ-2
DQ-1
DQ-0
M_DATA_B58
M_DATA_B63
M_DATA_B61
M_DATA_B57
M_DATA_B62
M_DATA_B59
M_DATA_B60
M_DATA_B56
M_DATA_B50
M_DATA_B54
M_DATA_B48
M_DATA_B52
M_DATA_B51
M_DATA_B55
M_DATA_B49
M_DATA_B53
M_DATA_B42
M_DATA_B46
M_DATA_B44
M_DATA_B40
M_DATA_B43
M_DATA_B47
M_DATA_B41
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M_DATA_B34
M_DATA_B37
M_DATA_B36
M_DATA_B35
M_DATA_B39
M_DATA_B33
M_DATA_B32
M_DATA_B31
M_DATA_B26
M_DATA_B29
M_DATA_B25
M_DATA_B30
M_DATA_B27
M_DATA_B28
M_DATA_B24
M_DATA_B18
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M_DATA_B20
M_DATA_B17
M_DATA_B19
M_DATA_B23
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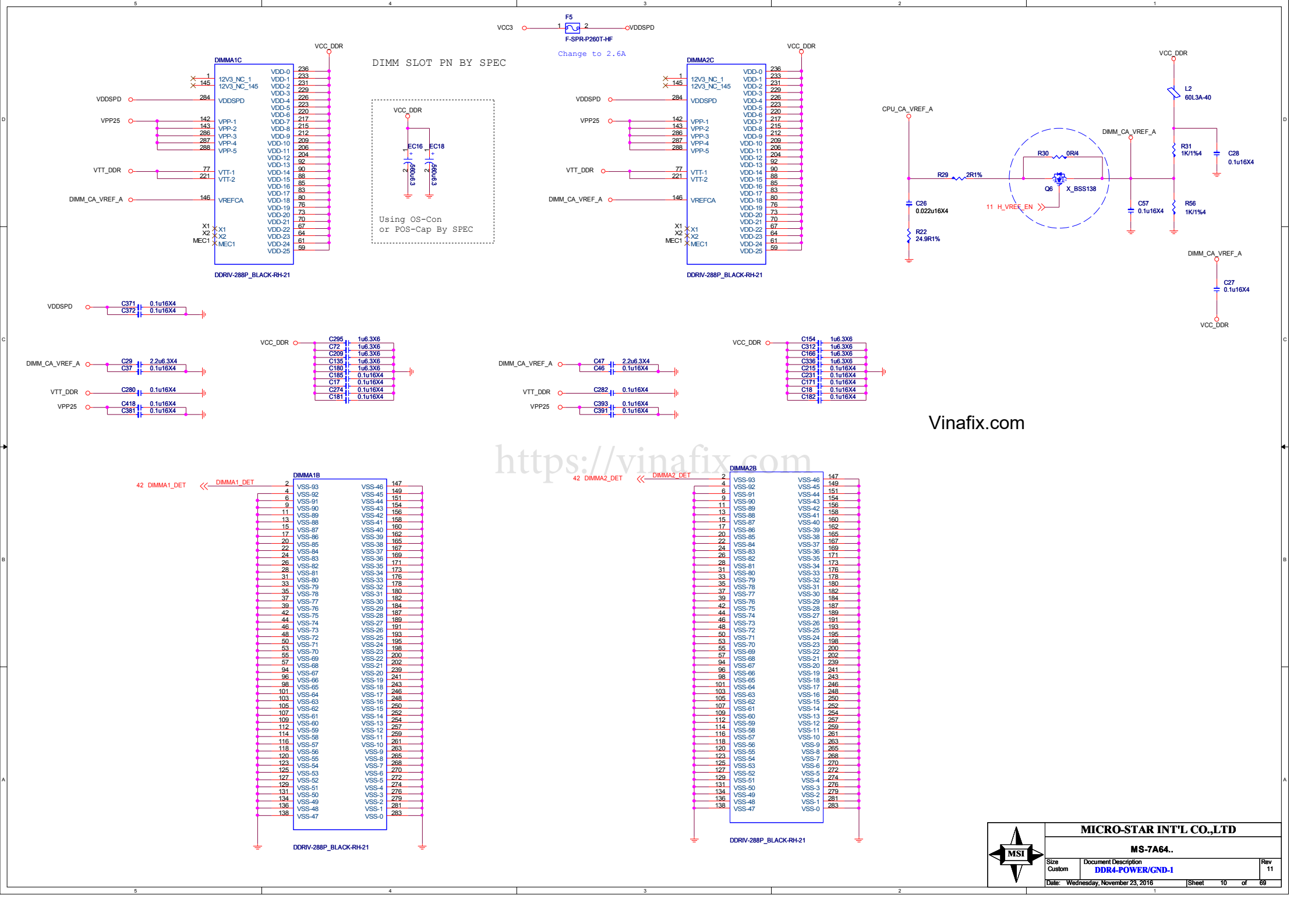
M_DATA_B15
M_DATA_B10
M_DATA_B8
M_DATA_B12
M_DATA_B11
M_DATA_B14
M_DATA_B9
M_DATA_B13
M_DATA_B7
M_DATA_B6
M_DATA_B5
M_DATA_B0
M_DATA_B3
M_DATA_B2
M_DATA_B1
M_DATA_B4
BG-1
BG-0
M_BG_B_1
M_BG_B_0
M_BG_B_1 3
M_BG_B_0 3
BA-1
BA-0
M_BA_B_1
M_BA_B_0
M_BA_B_1 3
M_BA_B_0 3
A17
A16_RAS_N
A15_CAS_N
A14_WE_N
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
M_MAA_B[16..0]
M_MAA_B[16..0] 3
M_MAA_B16
M_MAA_B15
M_MAA_B14
M_MAA_B13
M_MAA_B12
M_MAA_B11
M_MAA_B10
M_MAA_B9
M_MAA_B8
M_MAA_B7
M_MAA_B6
M_MAA_B5
M_MAA_B4
M_MAA_B3
M_MAA_B2
M_MAA_B1
M_MAA_B0
SCL
SDA
SMB_CLK_DIMM
SMB_DATA_DIMM
SMB_CLK_DIMM 8
SMB_DATA_DIMM 8
SA-2
SA-1
SA-0
VDDSPD
DDRIV-288P_BLACK-RH-21
DIMM3 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
VCC_DDR
DIMM3_EVENT R285 240R1%4
DIMM4_EVENT R286 240R1%4
VCC_DDR
DIMMB2A
DDRIV-288P_BLACK-RH-21
DIMM4 (CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]
MICRO-STAR INT'L CO.,LTD
MS-7A64..
Size
Custom
Document Description
DDR4 SLOT-DIMM3/DIMM4
Rev
11
Date: Wednesday, November 23, 2016
Sheet 9 of 69


F5
VCC3
VDDSPD
F-SPR-P260T-HF
DIMM SLOT PN BY SPEC
Change to 2.6A
DIMMA1C
DIMMA2C
DDRIV-288P_BLACK-RH-21
VCC_DDR
VDDSPD
VPP25
VTT_DDR
DIMM_CA_VREF_A
Using OS-Con
or POS-Cap By SPEC
EC16
EC18
560u6.3
CPU_CA_VREF_A
L2
60L3A-40
R30
0R4
R29
2R1%
Q6
X_BSS138
11 H_VREF_EN
R31
1K/1%4
R56
1K/1%4
C26
0.022u16X4
C57
0.1u16X4
C28
0.1u16X4
C27
0.1u16X4
R22
24.9R1%
C371
C372
0.1u16X4
C295
C72
C209
C135
C180
C185
C17
C274
C181
1u6.3X6
0.1u16X4
C29
C37
2.2u6.3X4
C280
C418
C381
C47
C46
C282
C393
C391
C154
C312
C166
C336
C215
C231
C171
C18
C182
Vinafix.com
https://vinafix.com
42 DIMMA1_DET
DIMMA1_DET
DIMMA1B
42 DIMMA2_DET
DIMMA2_DET
DIMMA2B
MICRO-STAR INT'L CO.,LTD
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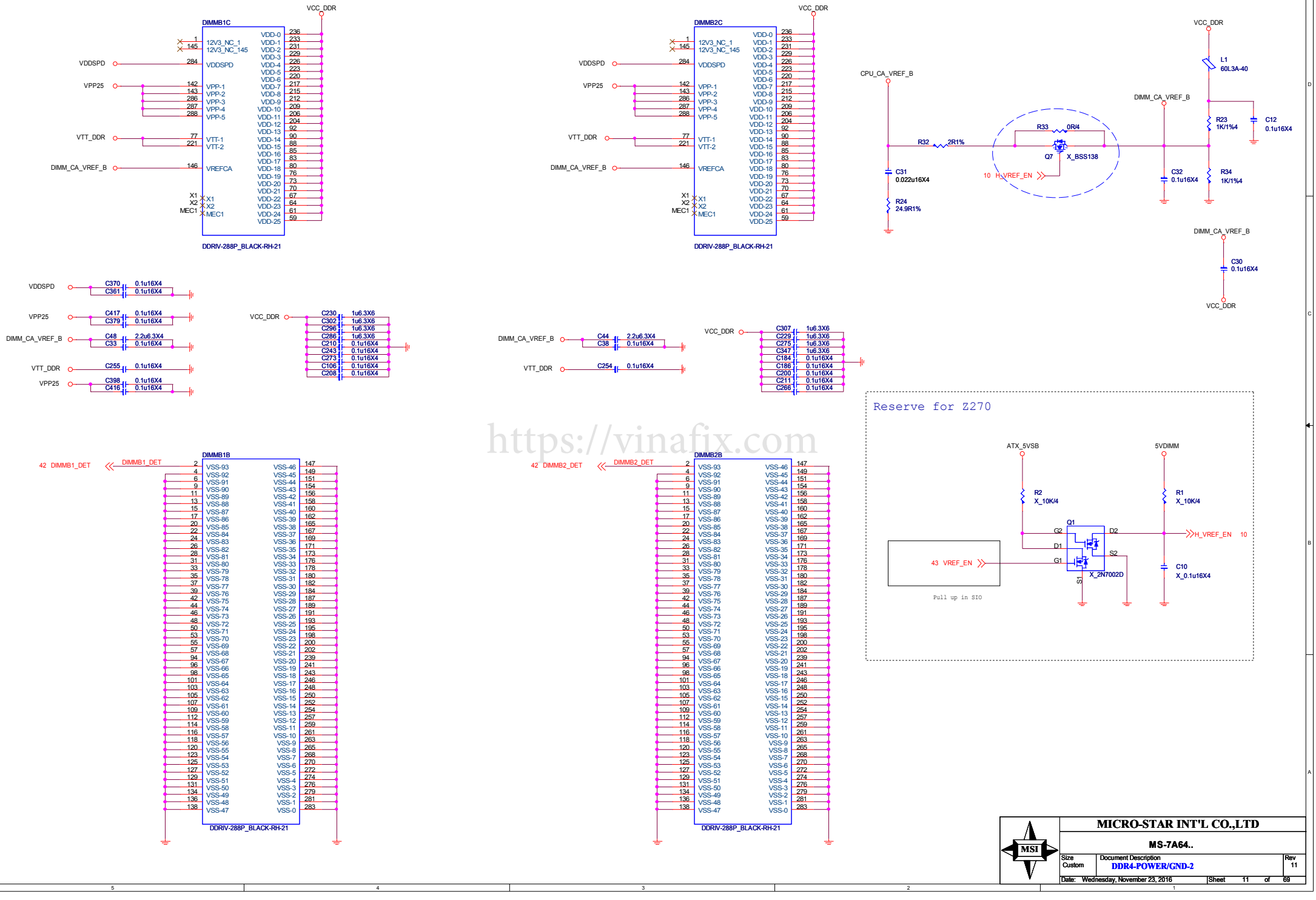
DDR4-POWER/GND-1
Rev
11
Date: Wednesday, November 23, 2016
Sheet 10 of 69



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MS-7A64..	
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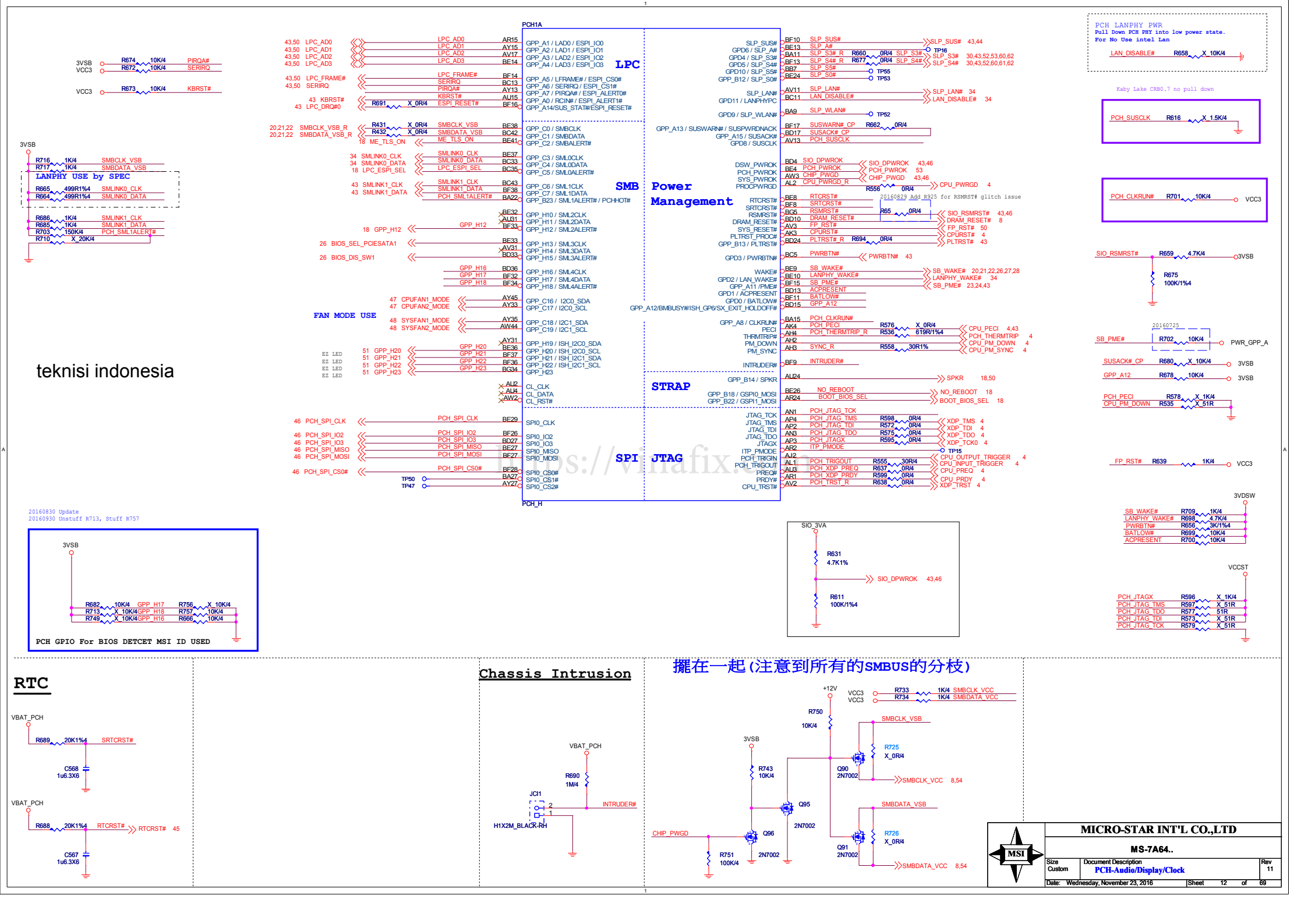
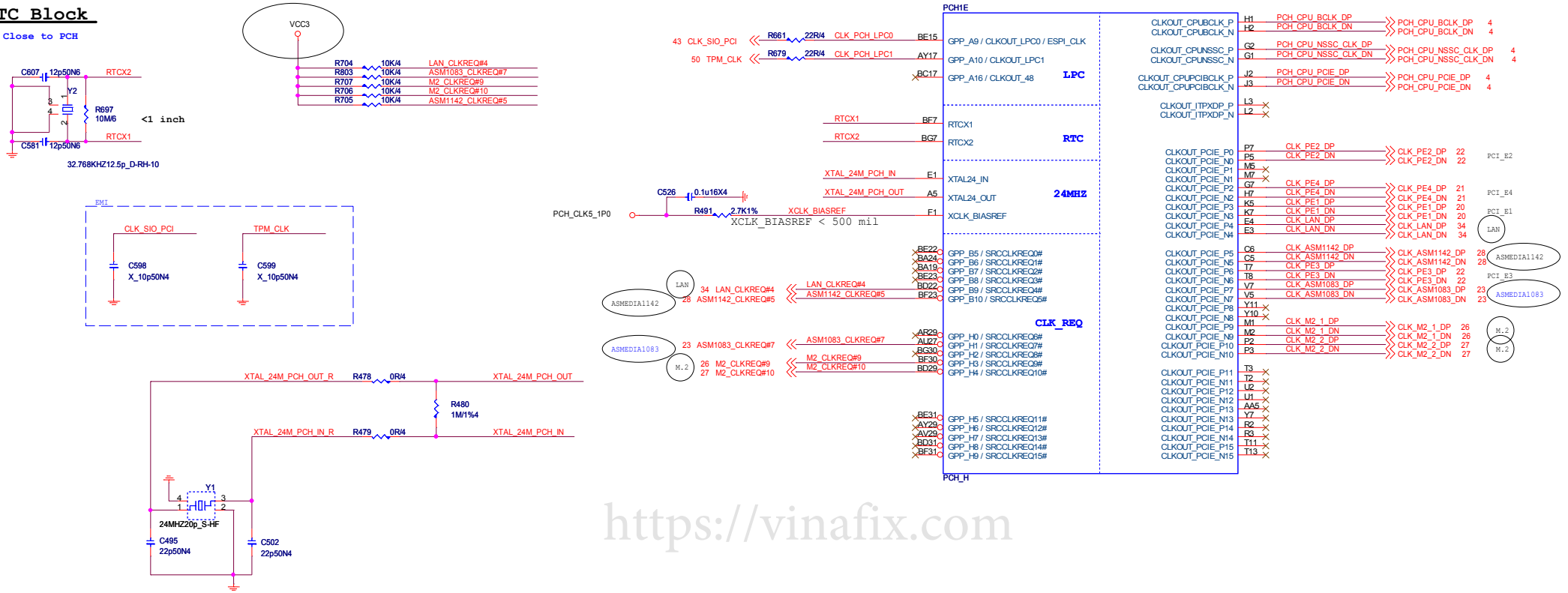
Rev: 11	
Date: Wednesday, November 23, 2016	Sheet 11 of 69

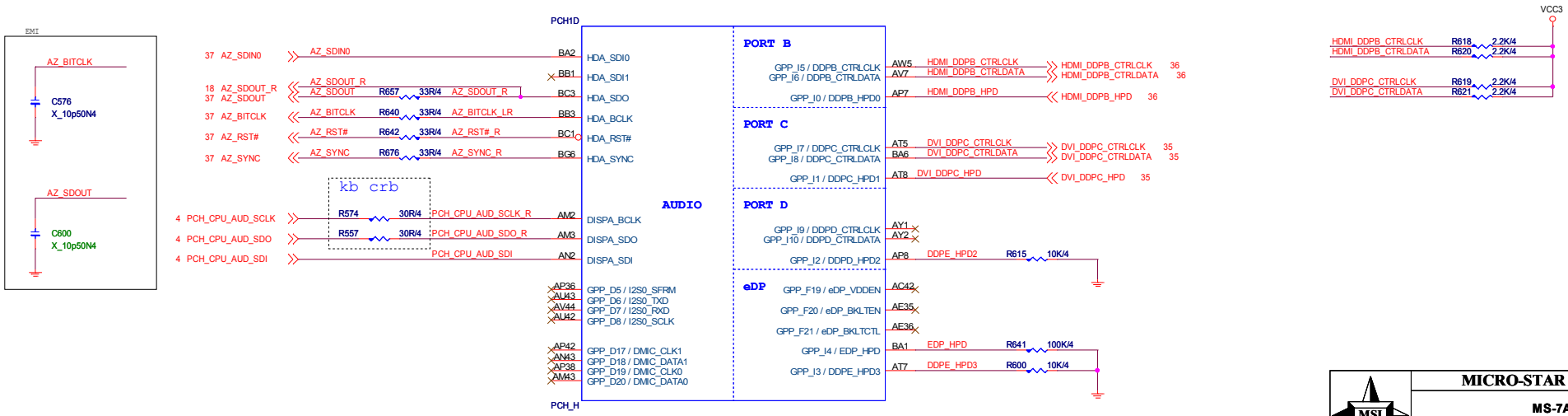

PCH1A
LPC
SMB
Power Management
STRAP
JTAG
SPI
PCH_H
FAN MODE USE
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
Kaby Lake CRB0.7 no pull down
LANPHY USE by SPEC
teknisi indonesia
20160830 Update
20160930 Unstuff R713, Stuff R757
PCH GPIO For BIOS DETCET MSI ID USED
RTC
Chassis Intrusion
擺在一起(注意到所有的SMBUS的分枝)
MICRO-STAR INT'L CO.,LTD
MS-7A64..
PCH-Audio/Display/Clock
Wednesday, November 23, 2016

PCH_CLK

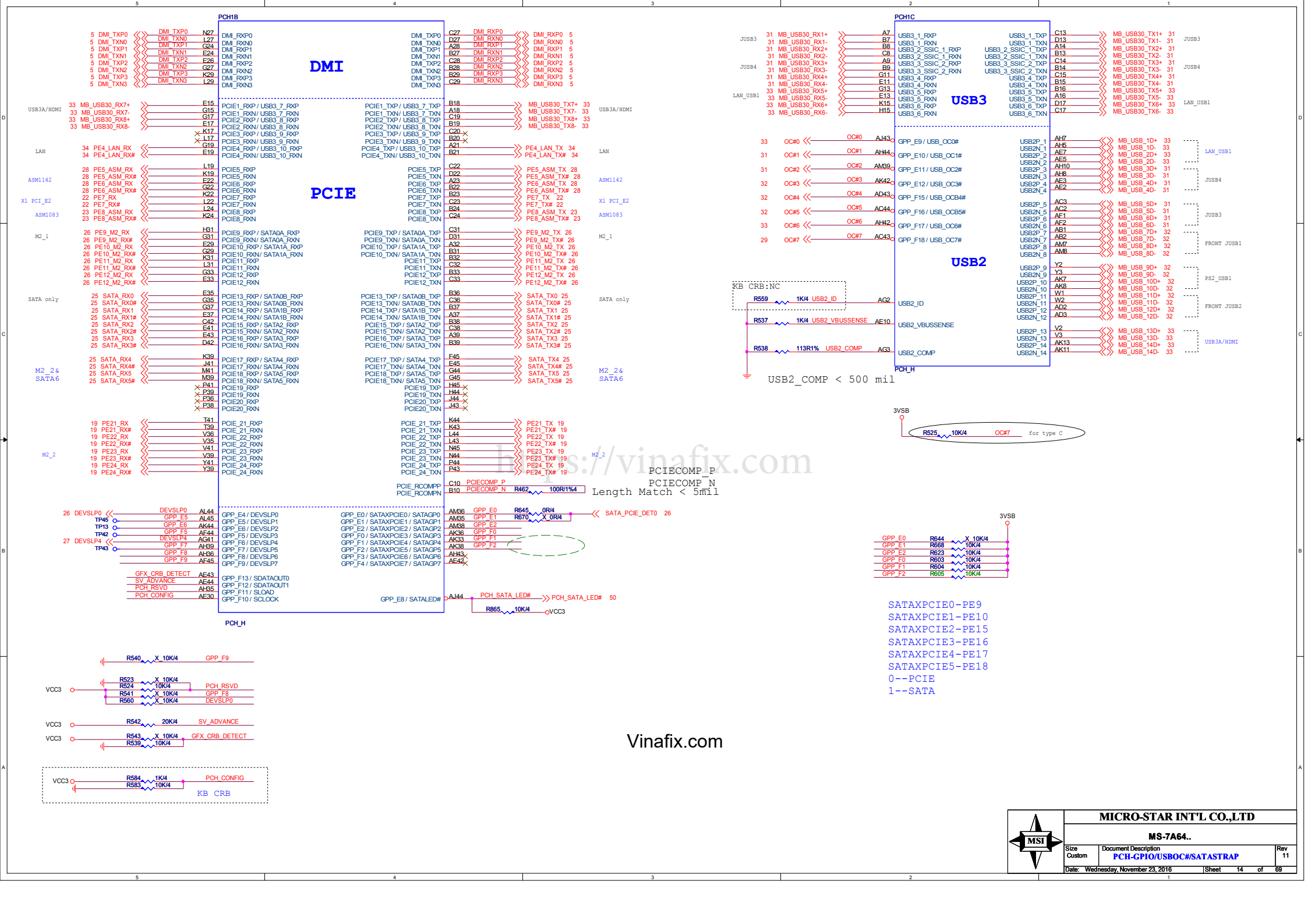
RTC_Block

Close to PCH

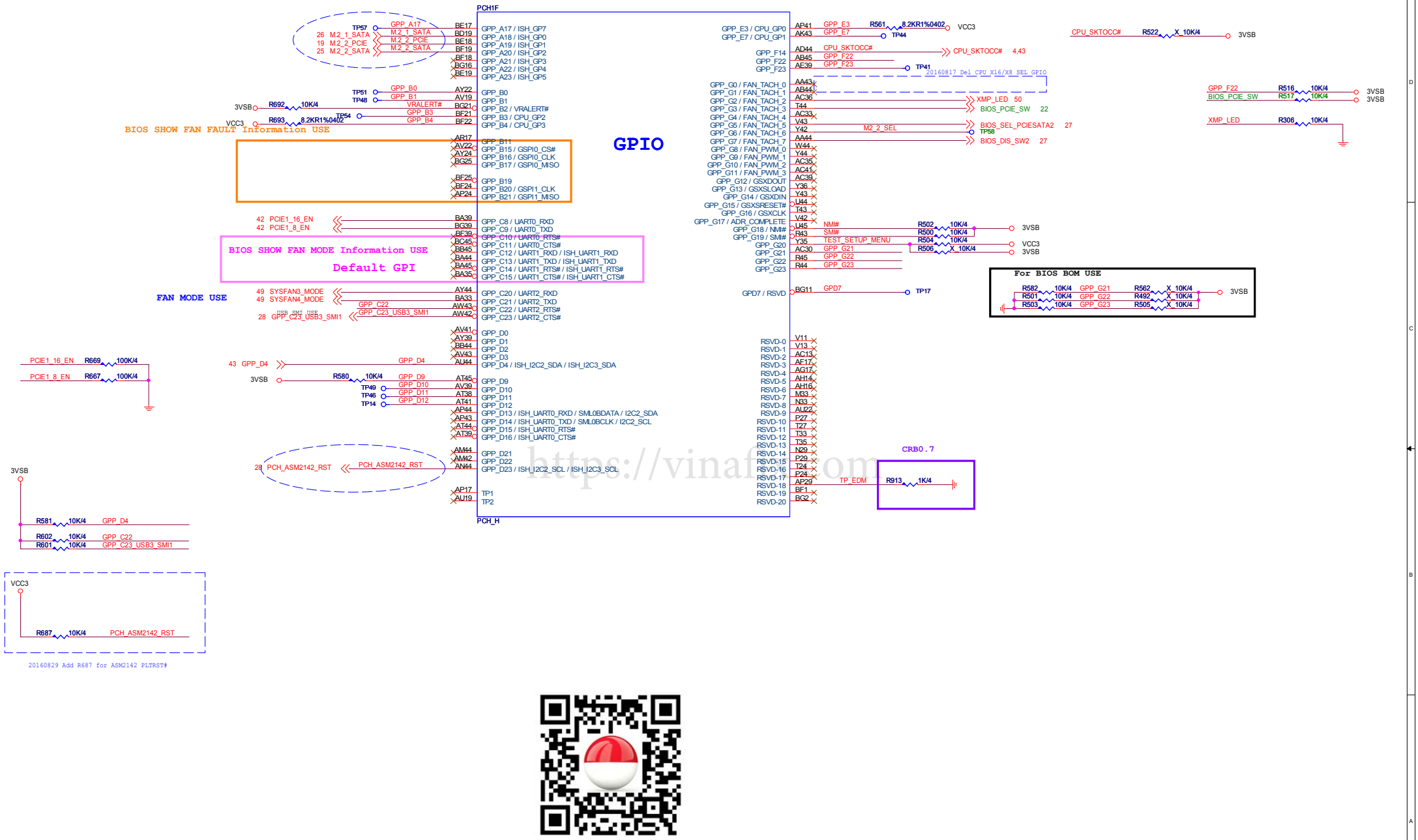




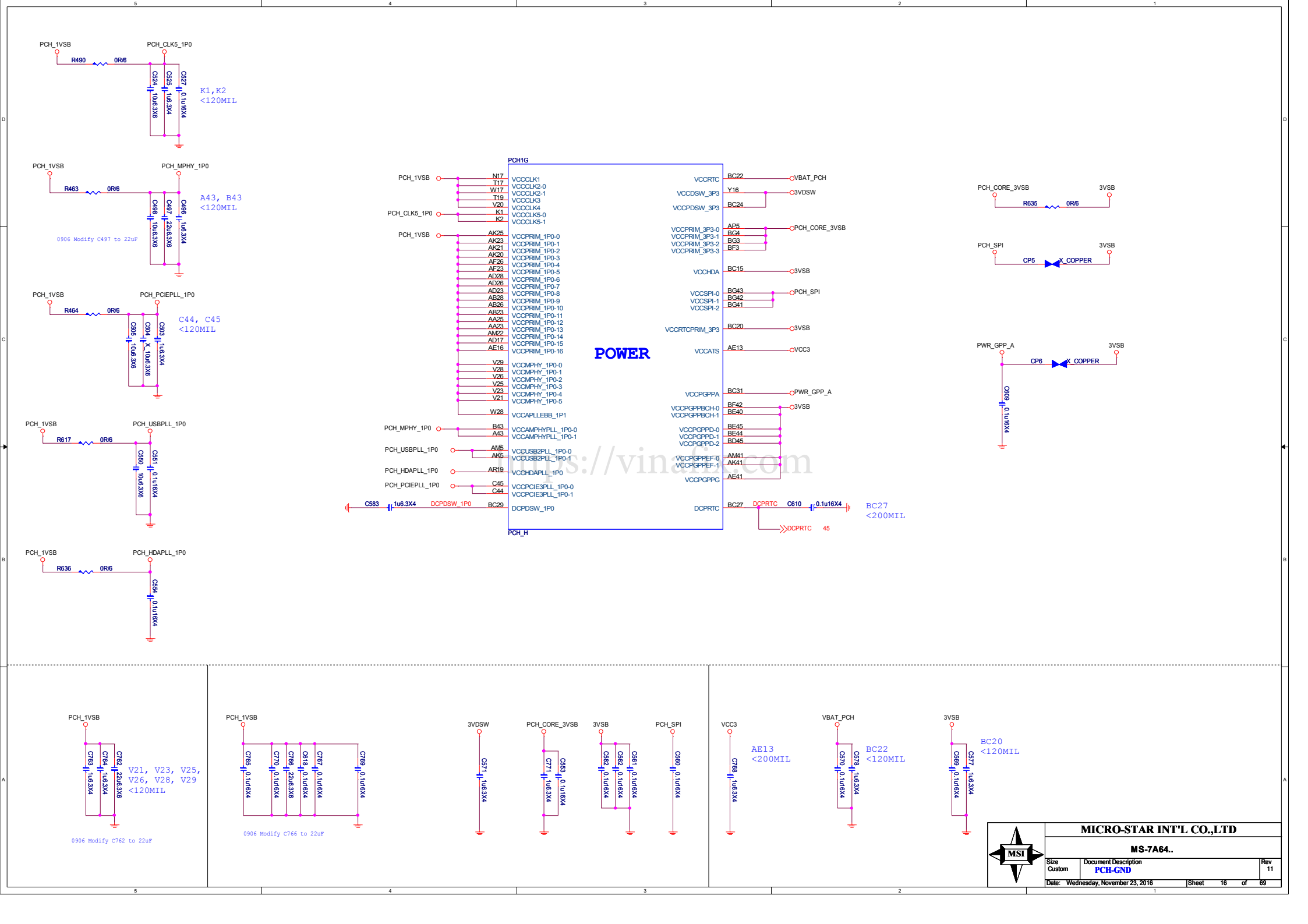
MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: PCH-USB/PCIE/DMI/SATA	Rev: 11
Date: Wednesday, November 23, 2016	Sheet 13 of 69	



MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: PCH-GPIO/USBOC#/SATASTRAP
Rev: 11	
Date: Wednesday, November 23, 2016	Sheet 14 of 69



MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC	Rev: 11
Date: Wednesday, November 23, 2016	Sheet 15 of 69	


PCH_1VSB
PCH_CLK5_1P0
R490 0R/6
C524 10u6.3X6
C525 1u6.3X4
C527 0.1u16X4
K1,K2
<120MIL
PCH_1VSB
PCH_MPHY_1P0
R463 0R/6
C498 10u6.3X6
C497 22u6.3X6
C496 1u6.3X4
A43, B43
<120MIL
0906 Modify C497 to 22uF
PCH_1VSB
PCH_PCIEPLL_1P0
R464 0R/6
C505 10u6.3X6
C504 X 10u6.3X6
C503 1u6.3X4
C44, C45
<120MIL
PCH_1VSB
PCH_USBPLL_1P0
R617 0R/6
C550 10u6.3X6
C551 0.1u16X4
PCH_1VSB
PCH_HDAPLL_1P0
R636 0R/6
C554 0.1u16X4
PCH1G
POWER
PCH_H
PCH_1VSB
PCH_CLK5_1P0
PCH_1VSB
PCH_MPHY_1P0
PCH_USBPLL_1P0
PCH_HDAPLL_1P0
PCH_PCIEPLL_1P0
C583 1u6.3X4 DCPDSW_1P0
VCCRTC
VCCDSW_3P3
VCCPDSW_3P3
VCCPRIM_3P3-0
VCCPRIM_3P3-1
VCCPRIM_3P3-2
VCCPRIM_3P3-3
VCCHDA
VCCSPI-0
VCCSPI-1
VCCSPI-2
VCCRTCPRIM_3P3
VCCATS
VCCPGPPA
VCCPGPPBCH-0
VCCPGPPBCH-1
VCCPGPPD-0
VCCPGPPD-1
VCCPGPPD-2
VCCPGPPEF-0
VCCPGPPEF-1
VCCPGPPG
DCPRTC
VBAT_PCH
3VDSW
PCH_CORE_3VSB
3VSB
PCH_SPI
3VSB
3VSB
VCC3
DCPRTC C610 0.1u16X4
DCPRTC 45
BC27
<200MIL
PCH_CORE_3VSB
3VSB
R635 0R/6
PCH_SPI
3VSB
CP5 X_COPPER
PWR_GPP_A
3VSB
CP6 X_COPPER
C609 0.1u16X4
PCH_1VSB
C763 1u6.3X4
C764 1u6.3X4
C762 22u6.3X6
V21, V23, V25,
V26, V28, V29
<120MIL
0906 Modify C762 to 22uF
PCH_1VSB
C765 0.1u16X4
C770 0.1u16X4
C766 22u6.3X6
C618 0.1u16X4
C767 0.1u16X4
C769 0.1u16X4
0906 Modify C766 to 22uF
3VDSW
C571 1u6.3X4
PCH_CORE_3VSB
C771 1u6.3X4
C553 0.1u16X4
3VSB
C582 0.1u16X4
C562 0.1u16X4
C581 0.1u16X4
PCH_SPI
C560 0.1u16X4
VCC3
C768 1u6.3X4
AE13
<200MIL
VBAT_PCH
C570 0.1u16X4
C578 1u6.3X4
BC22
<120MIL
3VSB
C569 0.1u16X4
C577 1u6.3X4
BC20
<120MIL
MICRO-STAR INT'L CO.,LTD
MS-7A64..
Size Custom
Document Description
PCH-GND
Rev 11
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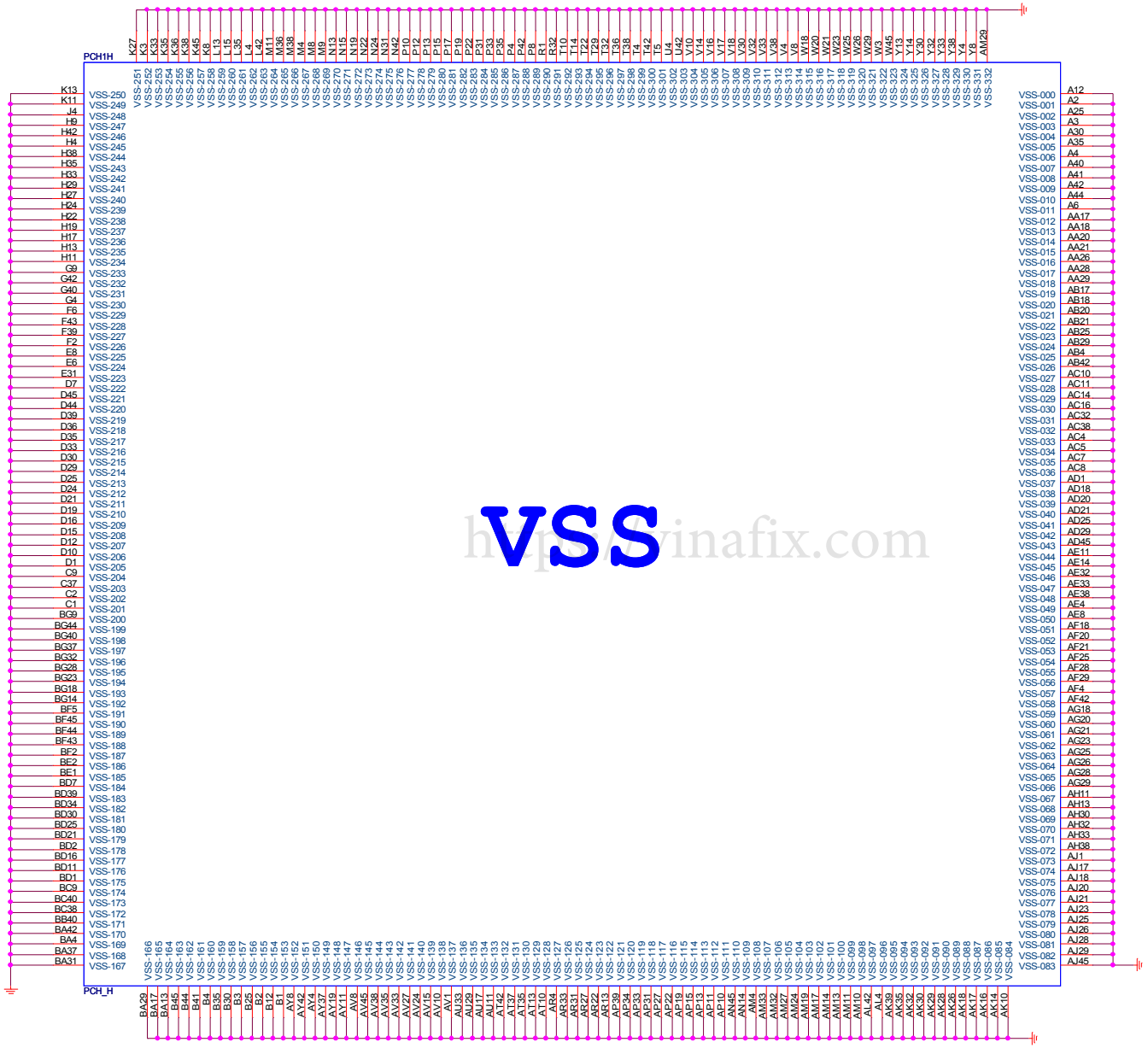

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size	Document Description	Rev
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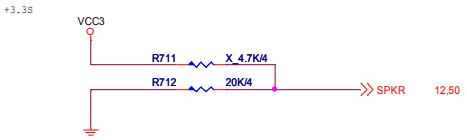
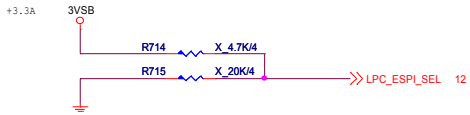
TOP Swap



Internal pull-down is disabled after PLTRST#

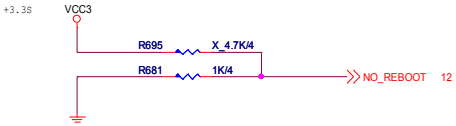
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

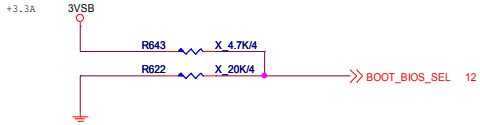
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

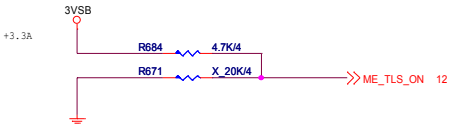
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

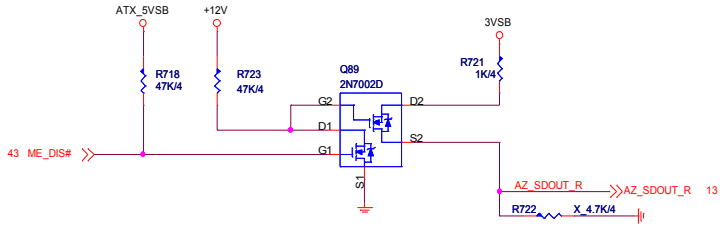
AMT and SBA with confidentiality



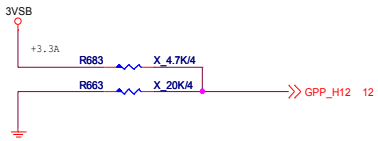
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

WW

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size	Document Description	Rev
Custom	PCH-Strap	11

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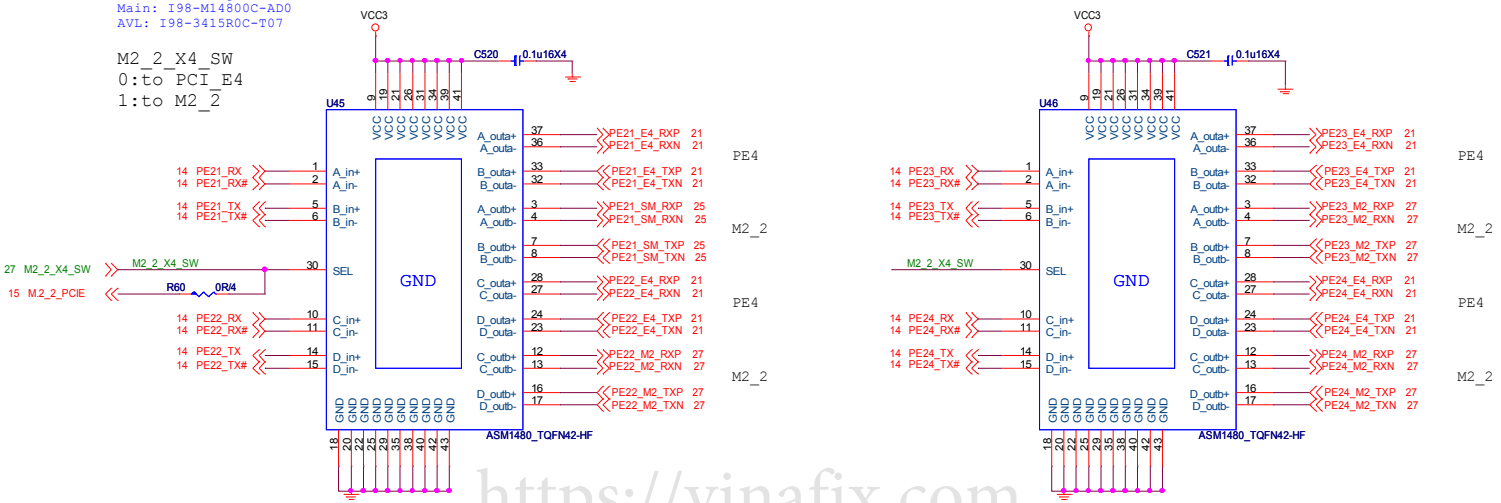
20160817 For PCI_E4 and M2_2 switch

20160804 Change Part
Main: I98-M14800C-AD0
AVL: I98-3415R0C-T07

M2_2_X4_SW
0:to PCI_E4
1:to M2_2



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
Size: Custom	Document Description: PCIE SWITCH	Rev: 11
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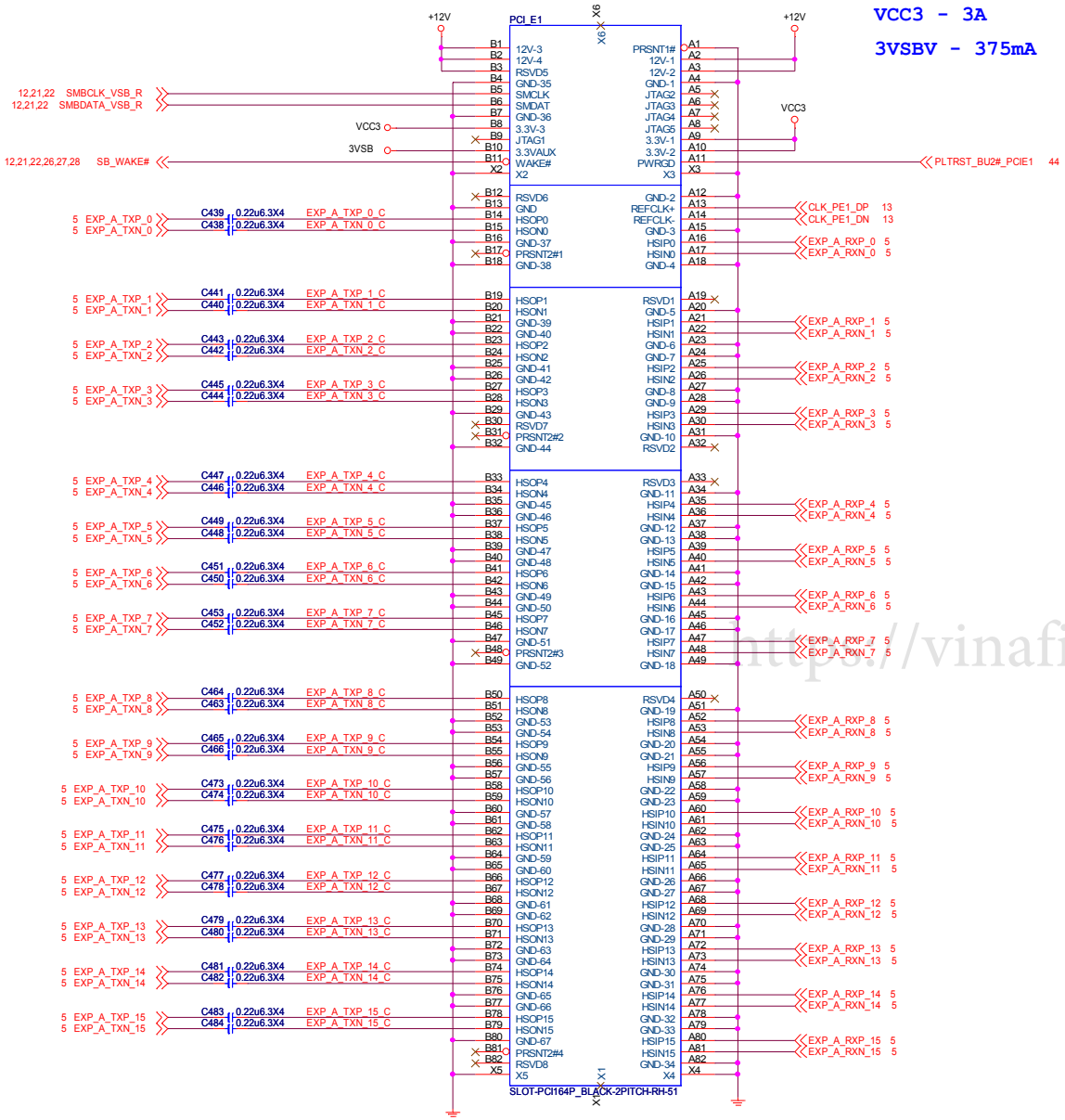
12V - 5.5A

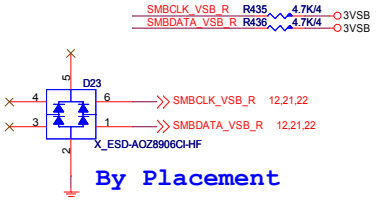
VCC3 - 3A

3VSBV - 375mA



0906 Modify PCI_E1 PIN X2.X3.X4.X5 Connect to GND

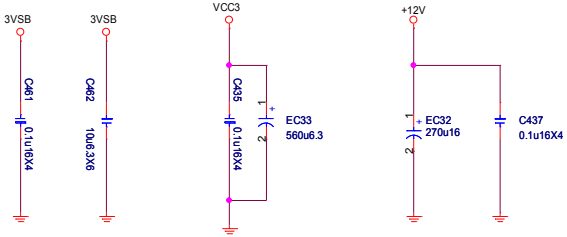
SMBUS ESD



By Placement

Main:D0G-05A0529-A68

AVL:D0G-45B0510-I14



MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 11	
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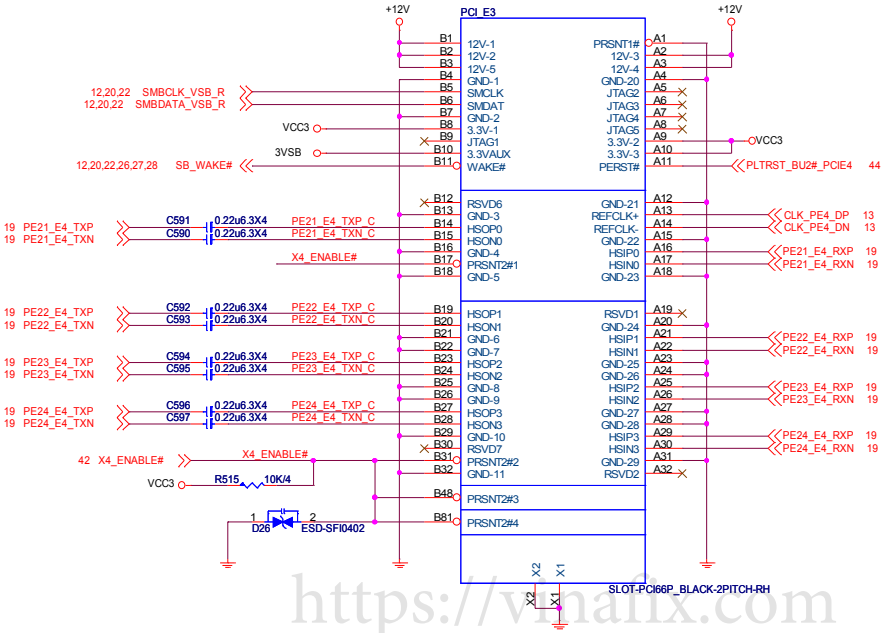
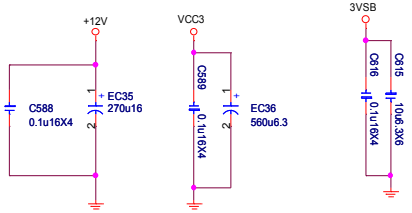
12V - 2.1A

VCC3 - 3A

3VSBV - 375mA



0909 Modify N11-1000221-L06 to N11-0660011-L06



MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: PCIE SLOT (X4)	Rev: 11
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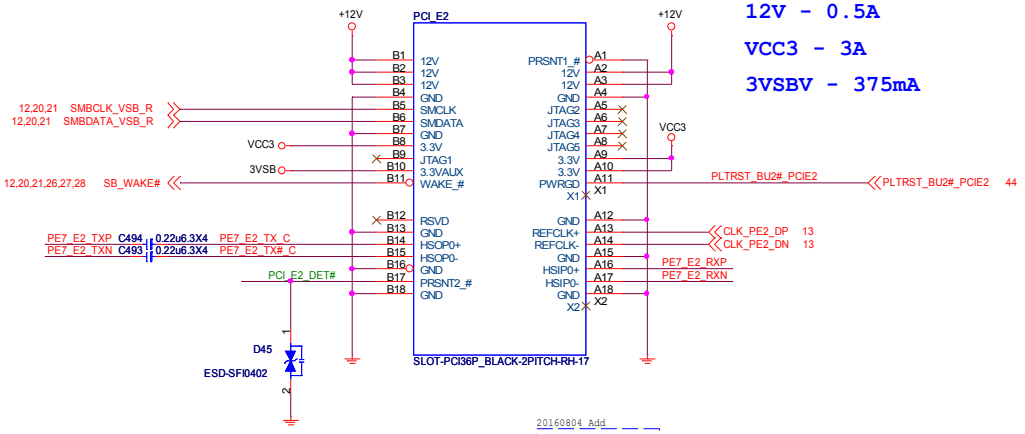
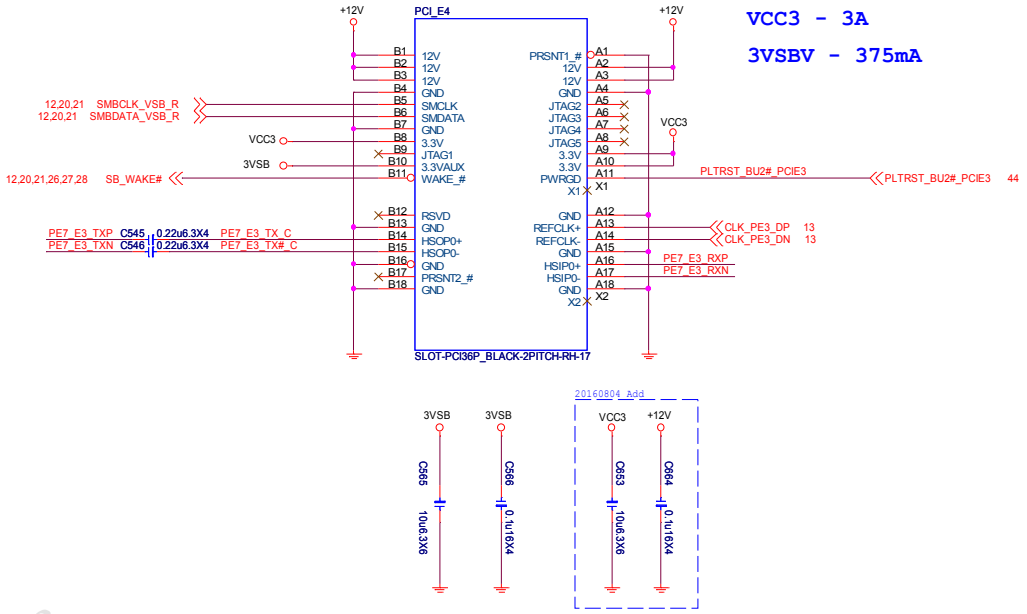
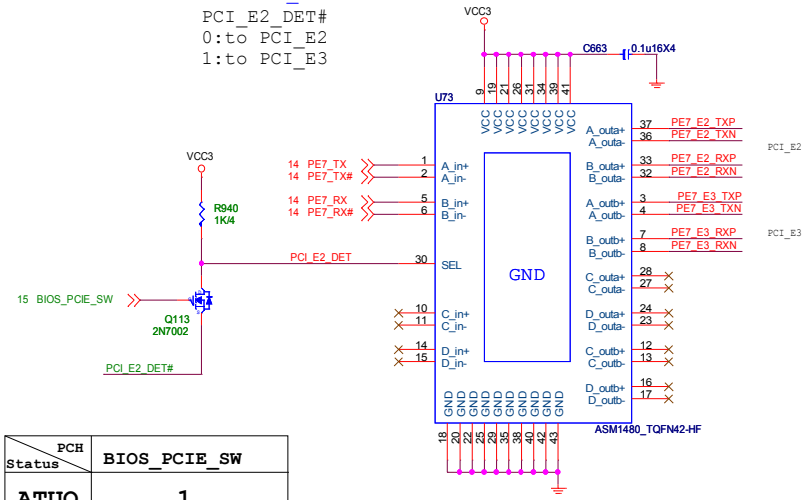




For PCI_E switch
PCI_E2_DET#
0:to PCI_E2
1:to PCI_E3



PCH / Status	BIOS_PCIE_SW
ATUO	1
BIOS	0

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size: Custom | Document Description: PCIE SLOT (X1) | Rev: 11

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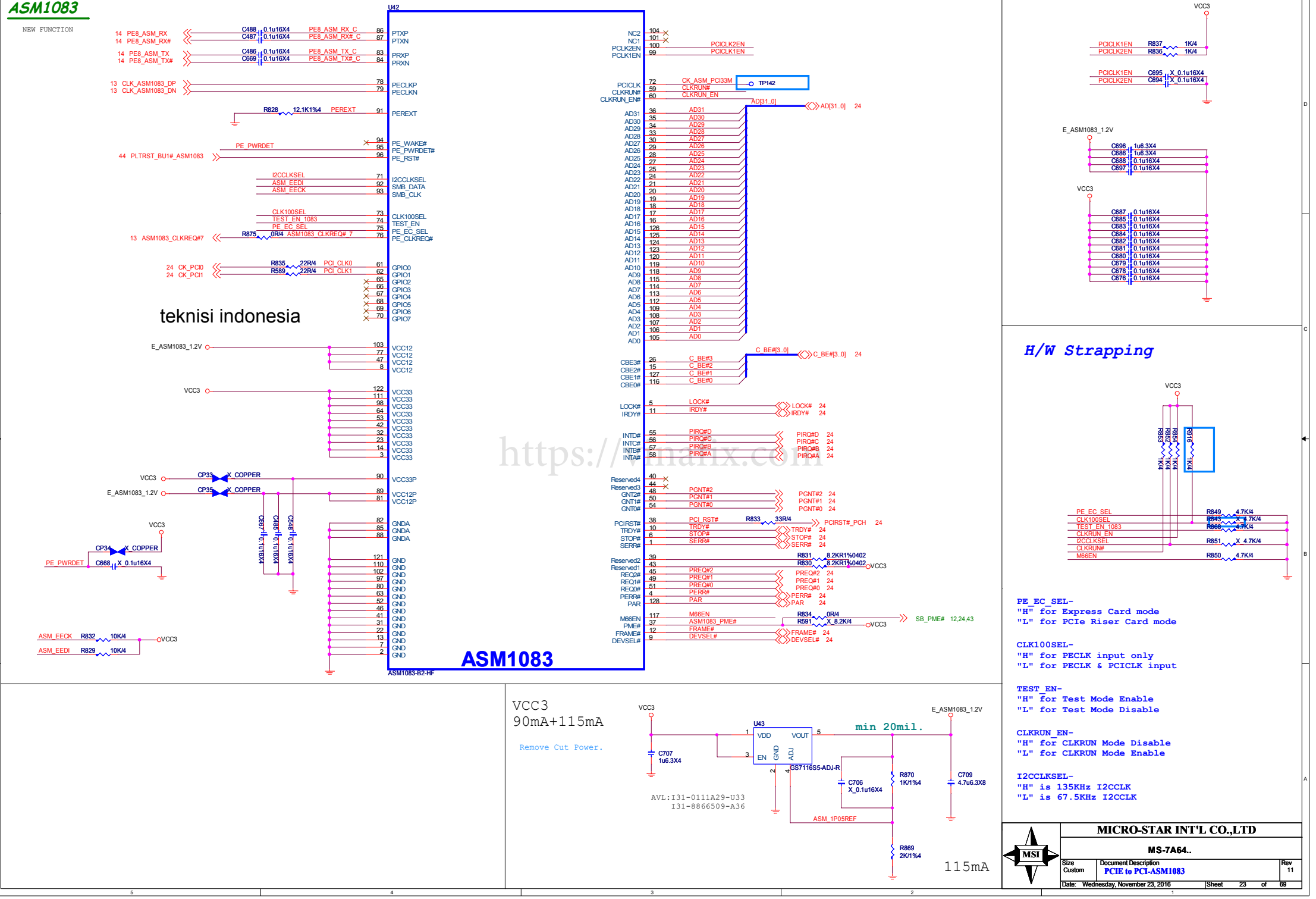
ASM1083

NEW FUNCTION



H/W Strapping

PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK

VCC3
90mA+115mA

Remove Cut Power.

AVL:I31-0111A29-U33
I31-8866509-A36

MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: PCIE to PCI-ASM1083	Rev: 11
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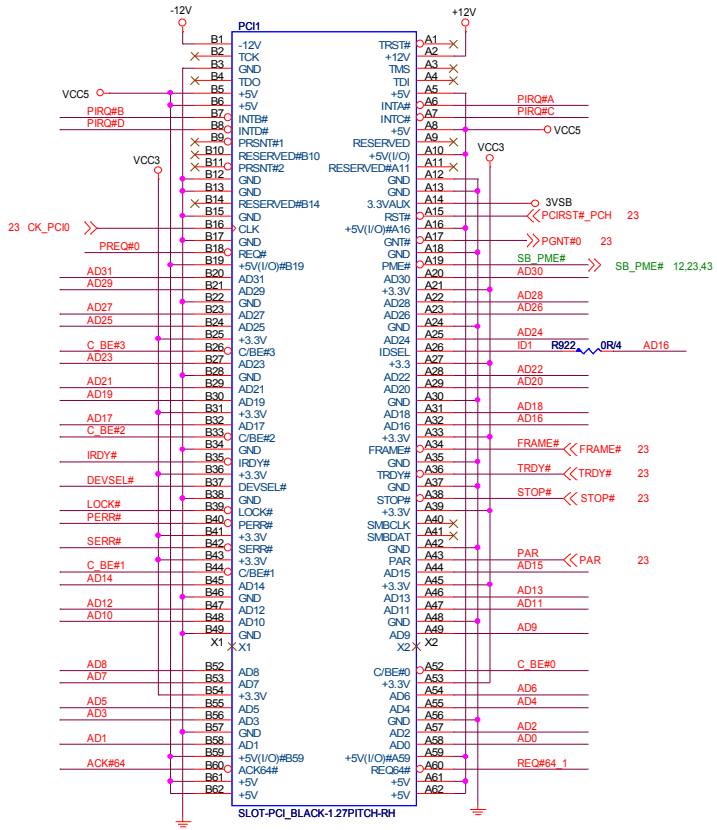
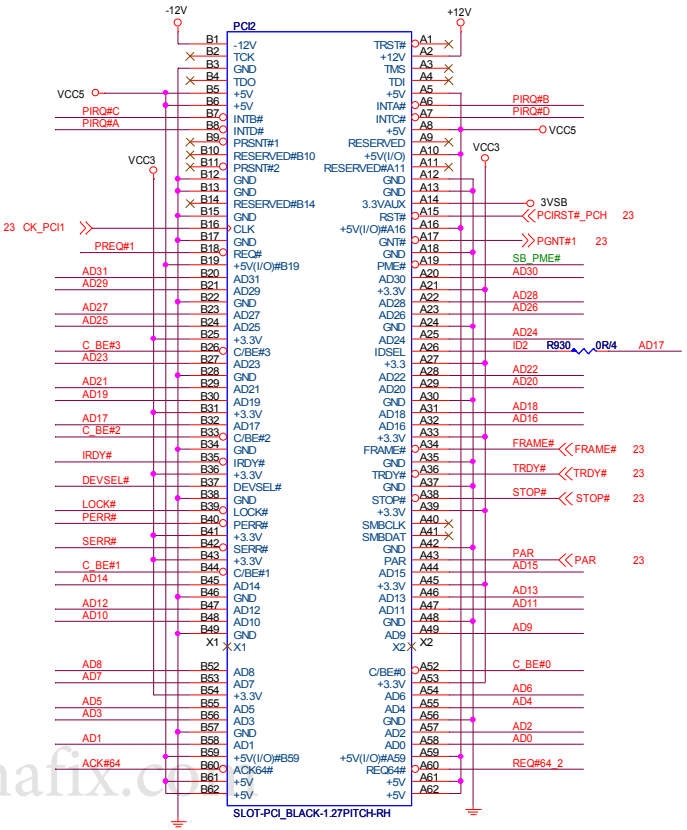


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

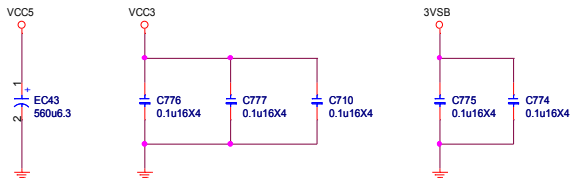


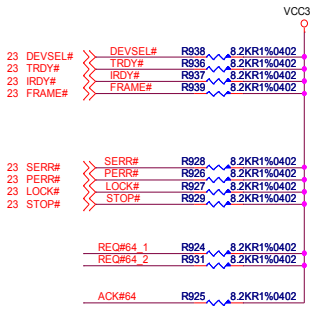
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

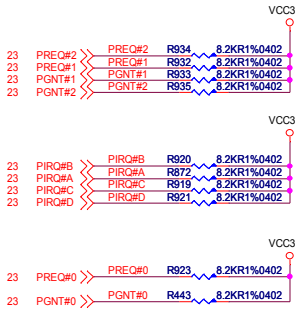
AD[31..0] AD[31..0] 23

C_BE#[3..0] C_BE#[3..0] 23

PCI PULL-UP / DOWN RESISTORS







PCI slot (X2)	
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 5A
+12V	- 500mA

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size	Document Description	Rev
Custom	PCI SLOT	11

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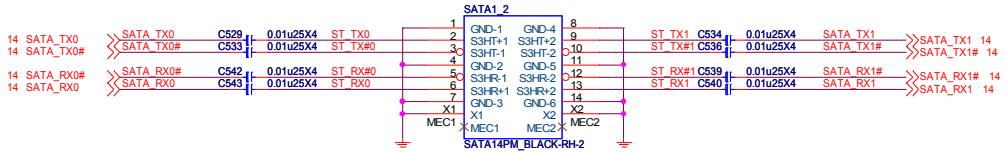

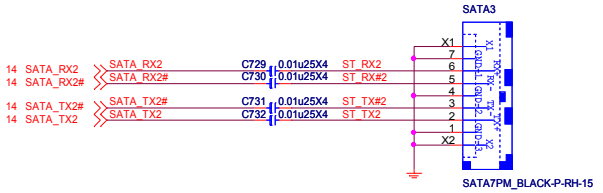

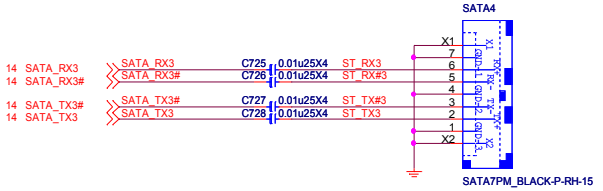

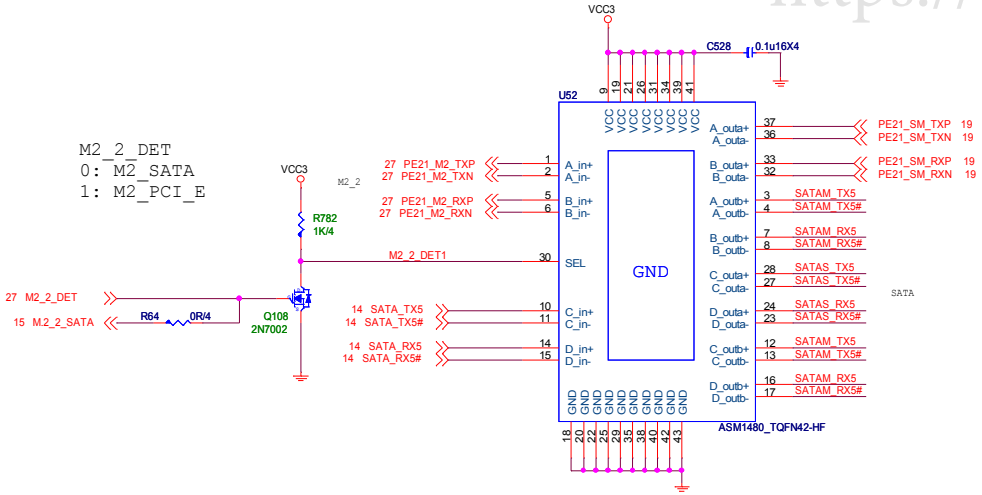

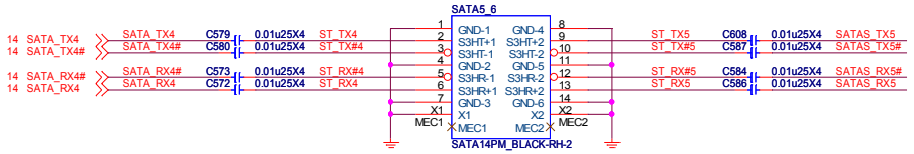

MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: SATA Connector	Rev: 11
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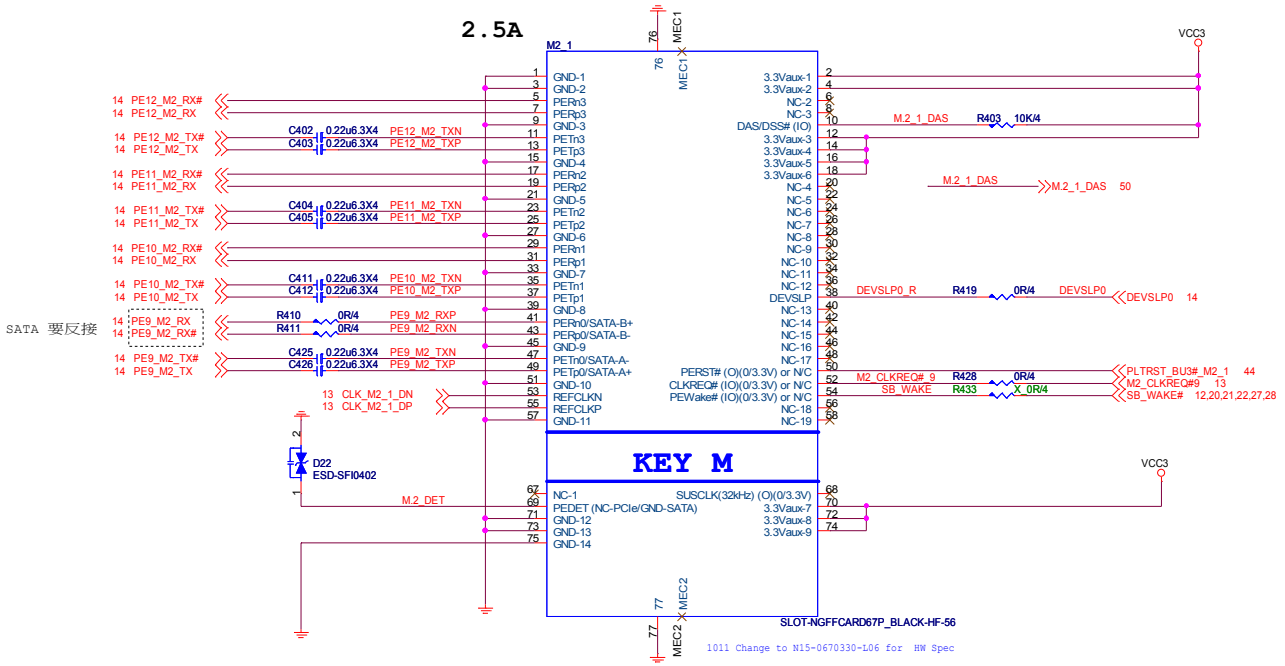
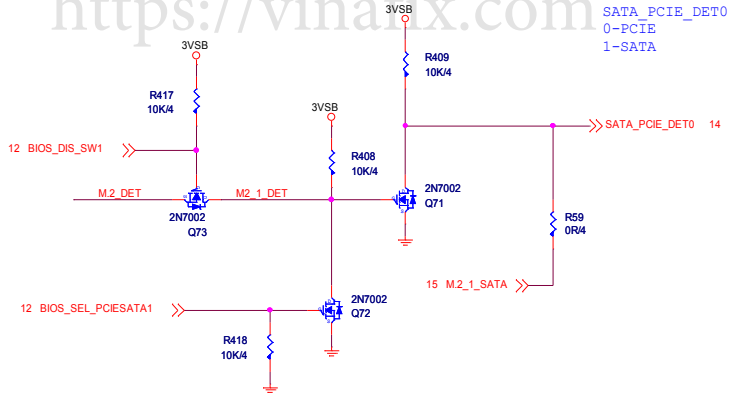
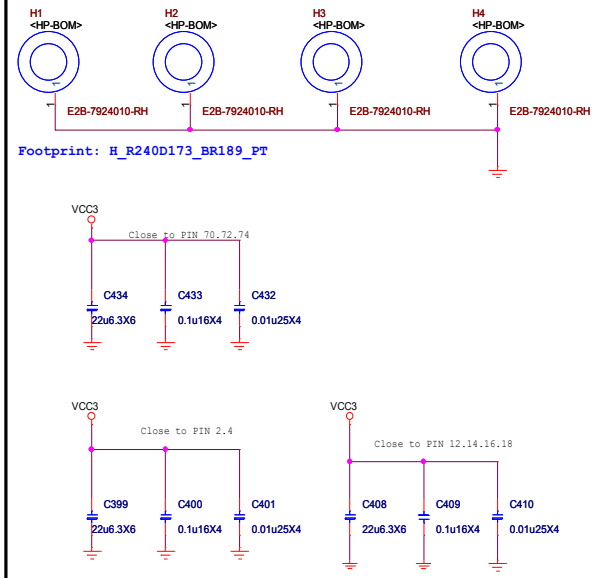




BIOS_MODE

	GPP_H15	GPP_H13	
BIOS_DIS_SW1	***BIOS_SEL_PCIESATA1***		***Mode***
0	*1*		***M2-SATA***
0	*0*		***M2-PCIE***
GPI	*GPI*		***AUTO***



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
Size: Custom	Document Description: M.2-SLOT1	Rev: 11
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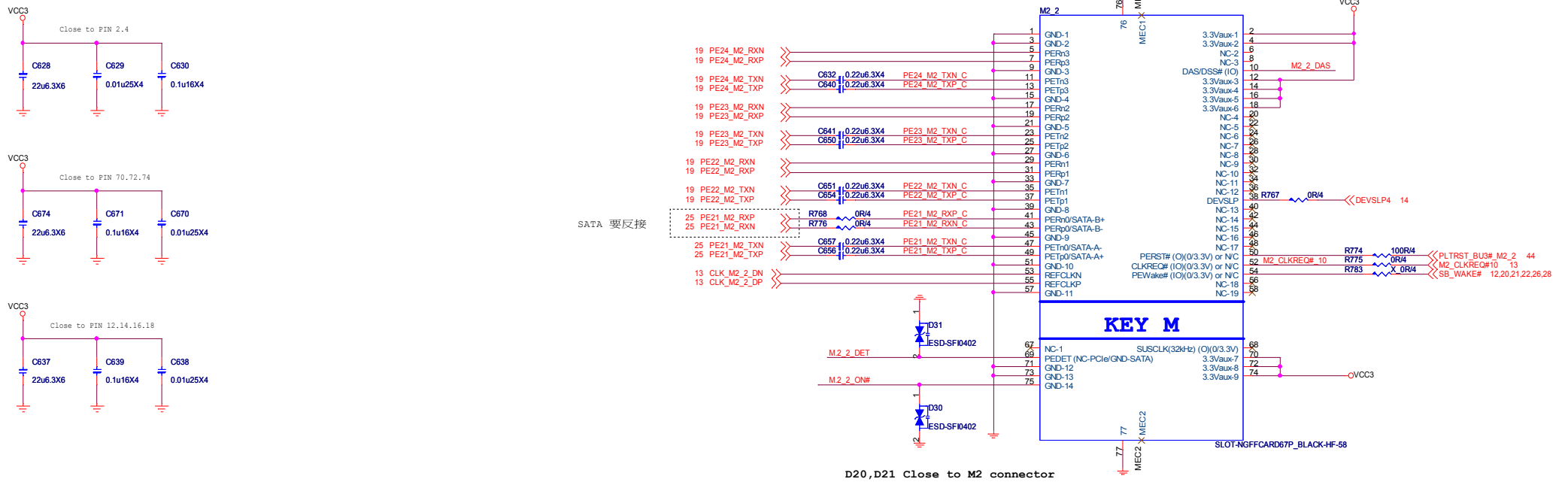
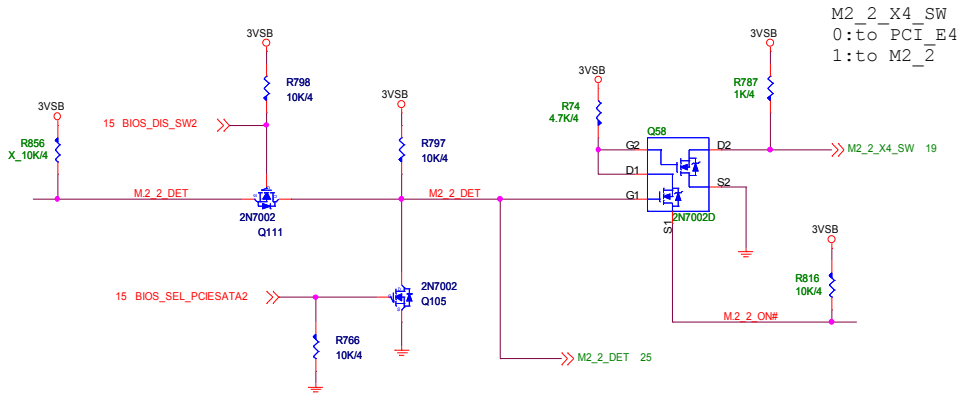
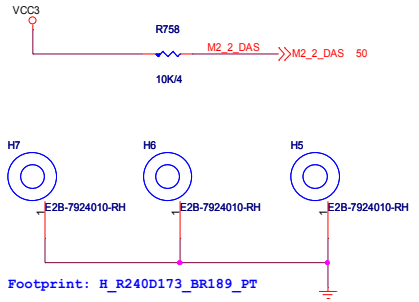




BIOS_MODE

GPP_G7 GPP_G5

BIOS_DIS_SW	*BIOS_SEL_PCIESATA2*	*Mode*
GPI(1)	*GPI(0)*	*AUTO*
1	*0*	***M2-PCIE***
0	*1*	***PCI_E X4***



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
Size: Custom	Document Description: M.2-SLOT2	Rev: 11
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Minimun gap should be greater of
>15mil with other signal.

USB HS (90Ohm-Diff) Chip to Connector ~1.5 inch.

USB SS (80Ohm-Diff)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

SMI connect to GPI which
support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

0909 Modify B02-021420C-AD0 to B02-021421C-AD0

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

atx5vsb change to vcc5

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

ASM1142 RU16 stuff RU17 unstuff
ASM2142 RU16 unstuff RU17 stuff

2016 . 8 .25 modification

ASM1142 U144 stuff RU24 unstuff
ASM1142 U144 unstuff RU24 stuff

ASM1142 RU19 stuff RU18 unstuff
ASM2142 RU19 unstuff RU18 stuff

YU1
D04-0900900-SC6(M)
D04-0901200-F07
D04-0901100-T16

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	250mA	650mA	56mA	15mA	NA	1573.8(mW)
ASM2142	4mA	470mA	9mA	10mA	220mA	TDP

teknisi indonesia

ASM1142 1.2 VCC Power

SN:L01-0107118-M26

20160829 Update

ASM1142 RU13/RU14 200K/187K 1.24V
ASM2142 RU13/RU14 196K/261K 1.05V

20160728
Change ASM1142 VDD/VDD_SUS to 1.24V from 1.2V base on data sheet R1.6 note1.

ASM1142 1.2 VSB Power

ASM1142 RU9 19.6K 1.2V
ASM2142 RU9 31.6K 1.05V

ASM1142 unstuff
ASM2142 stuff

20160720
Add SPI ROM PN
1M bit for ASM2142
512K bit for ASM1142

EEPROM

ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-25l1022-M24(1M bit)

MICRO-STAR INT'L CO.,LTD			
MS-7A64..			
Size: Custom	Document Description: ASM 2142		Rev: 11
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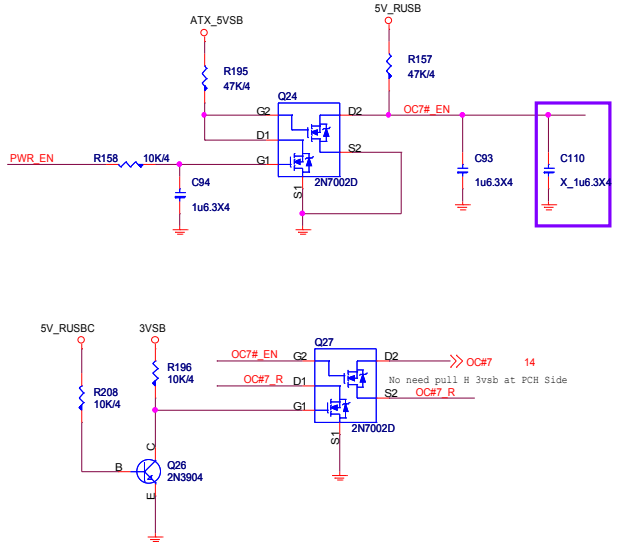
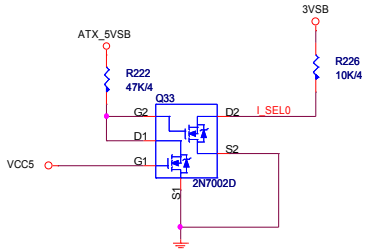
VBUS OC#



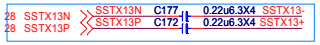
Current Mode



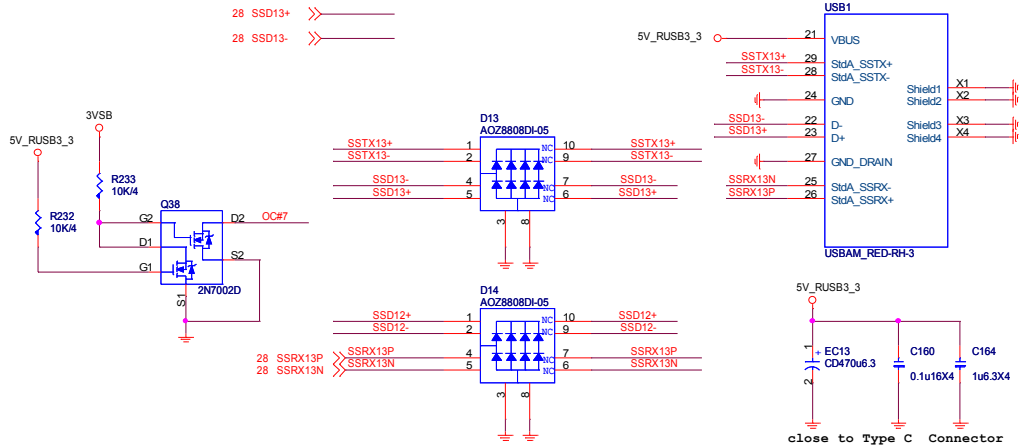
I_SEL0 : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

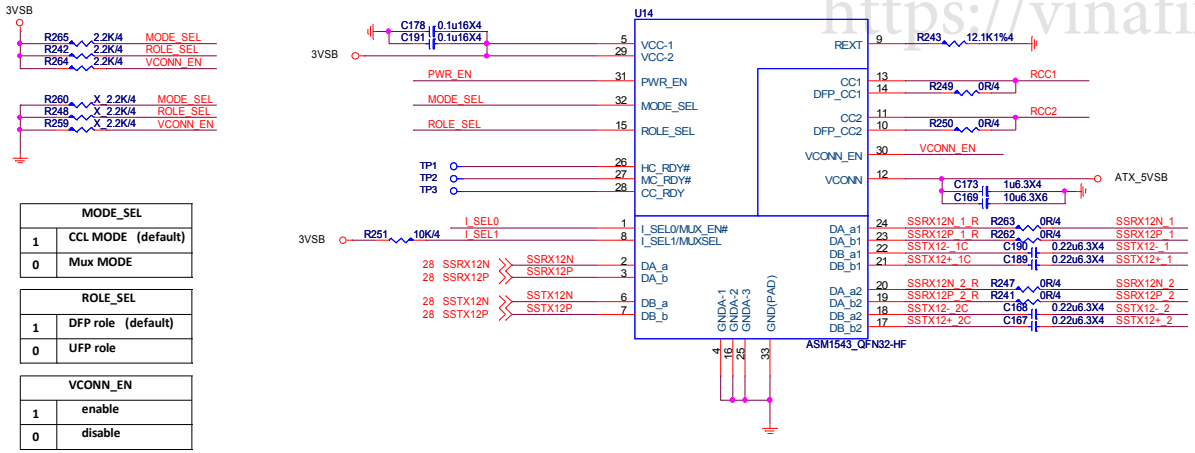
TYPE-A



0909 Modify N53-09M0861-L06 to N53-09M0591-L06



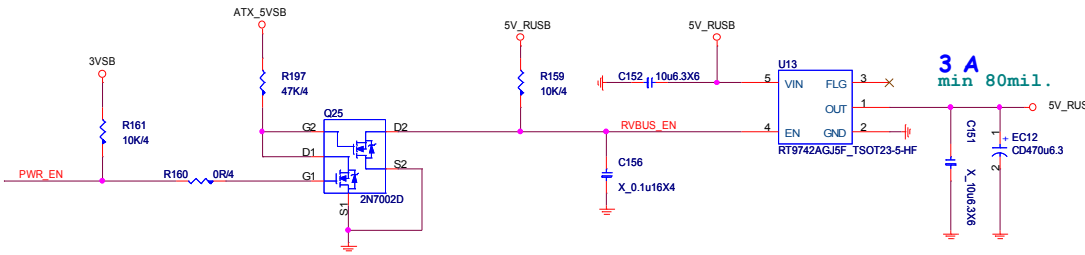
USB Type-C MUX with Configuration Channel (CC)



MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

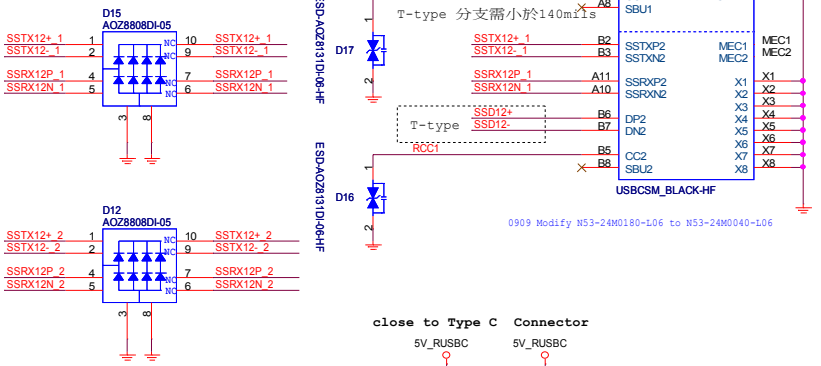
ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable



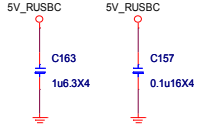
TYPE-C

OC#7



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL

close to Type C Connector



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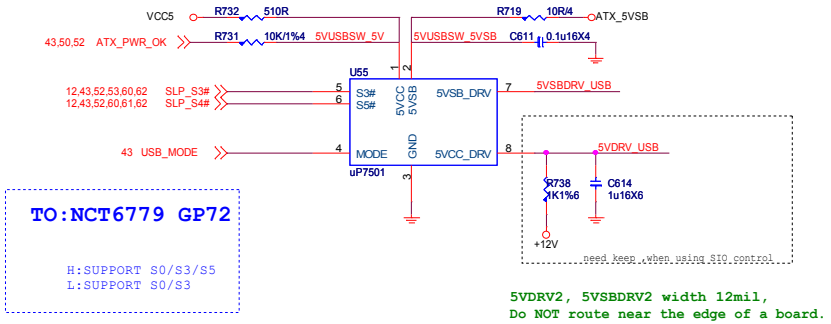
USB PORT POWER

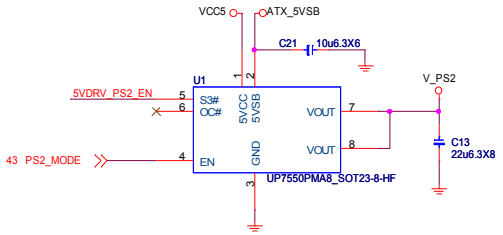


TO:NCT6779 GP72

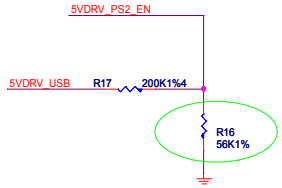
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

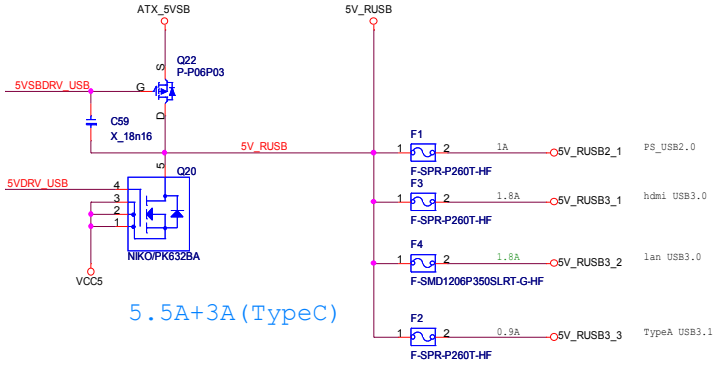
PS2 Power



USB MODE

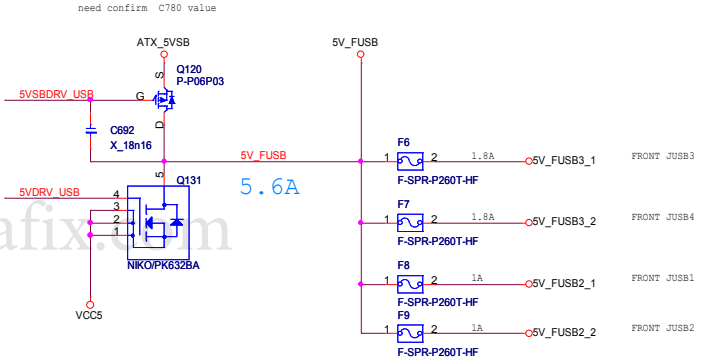


REAR USB PORT POWER



5.5A+3A(TypeC)

FRONT USB PORT POWER



5.6A

P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-0301000-P16
D08-0301100-B07

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MS-7A64..		
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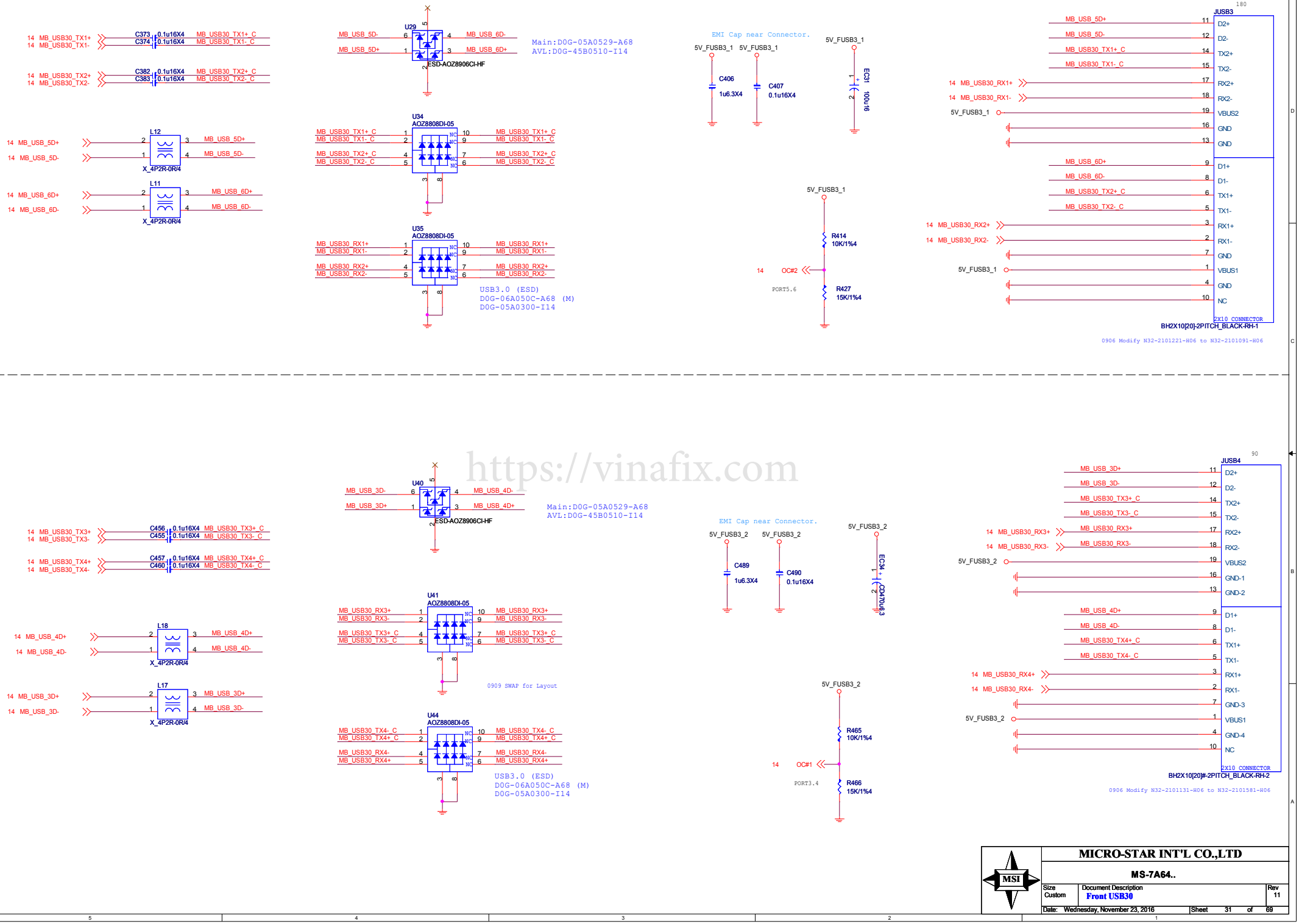

MICRO-STAR INT'L CO.,LTD

MS-7A64..

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Custom	Front USB30	11

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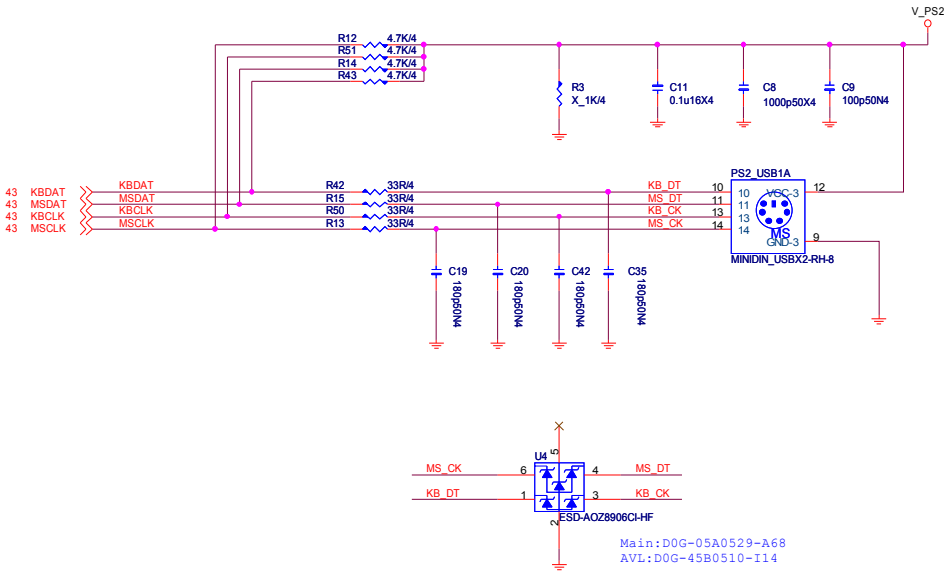
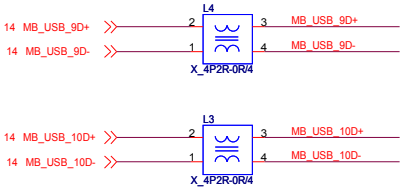
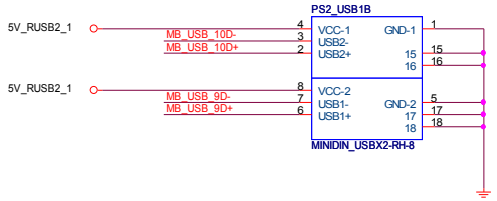
PS2 Connector

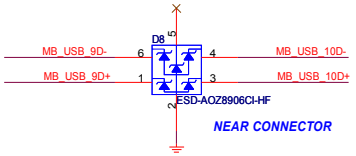


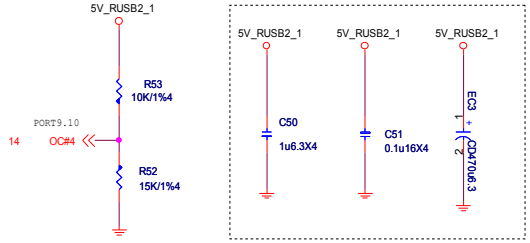
PS2 _USB

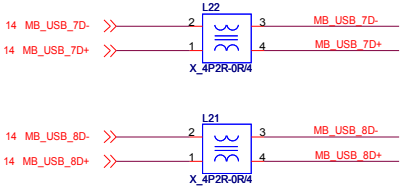


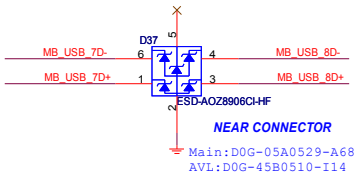


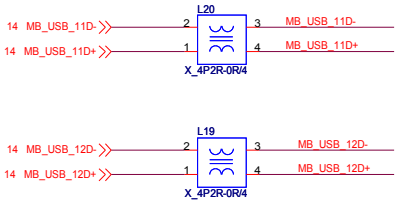
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

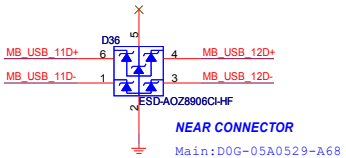


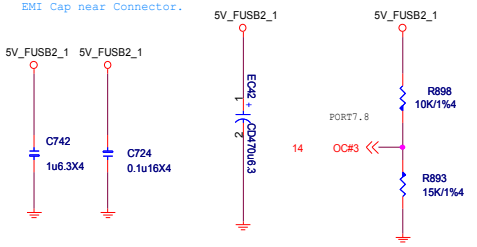


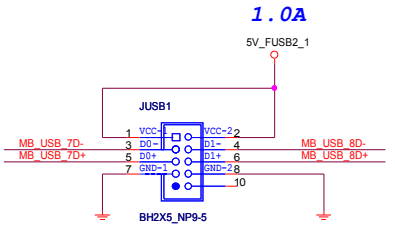


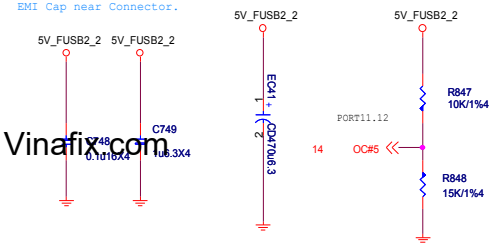


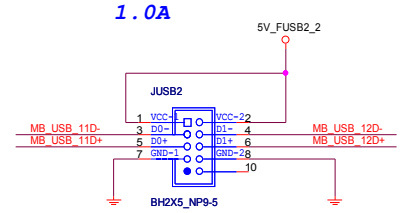












MSI	MICRO-STAR INT'L CO.,LTD	
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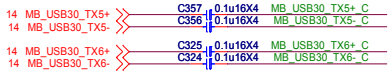
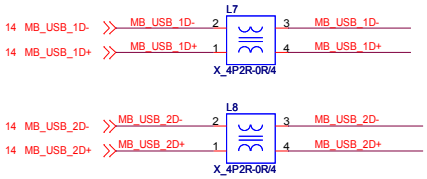
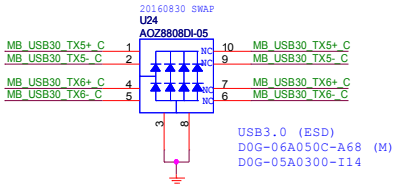
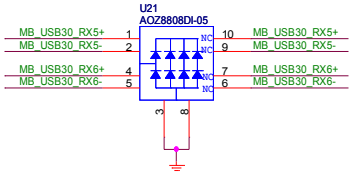
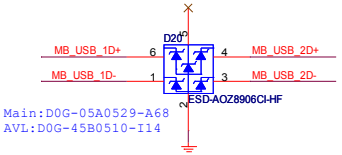
LAN USB3.0



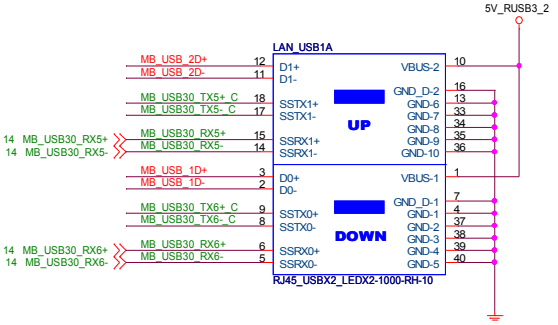


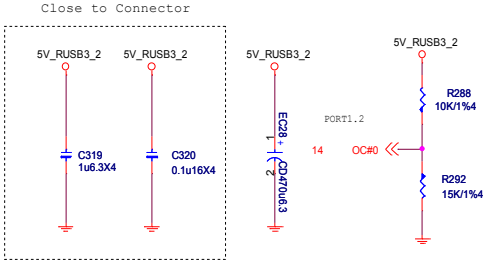




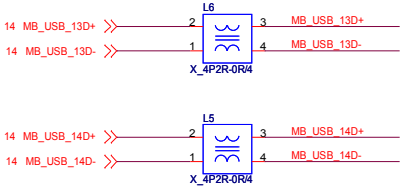


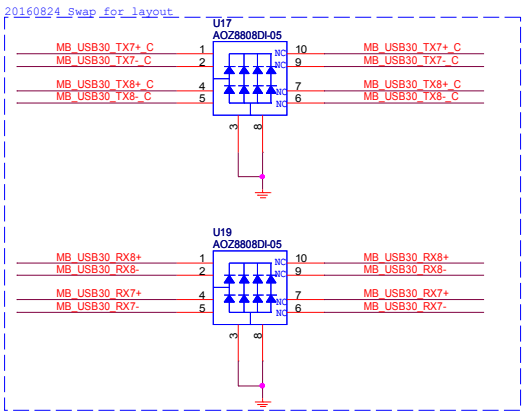
3A

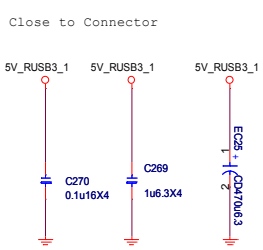


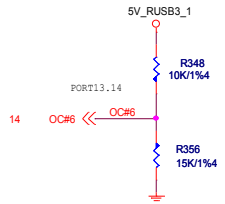


HDMI USB3.0









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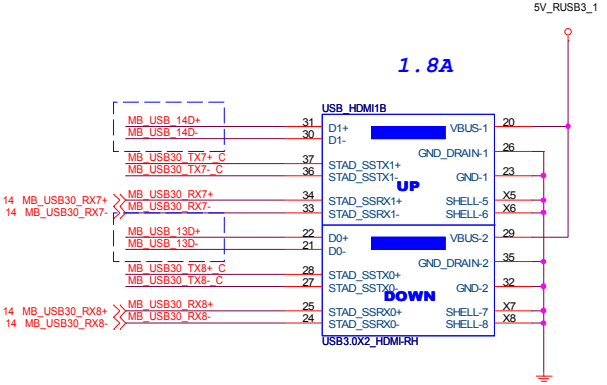

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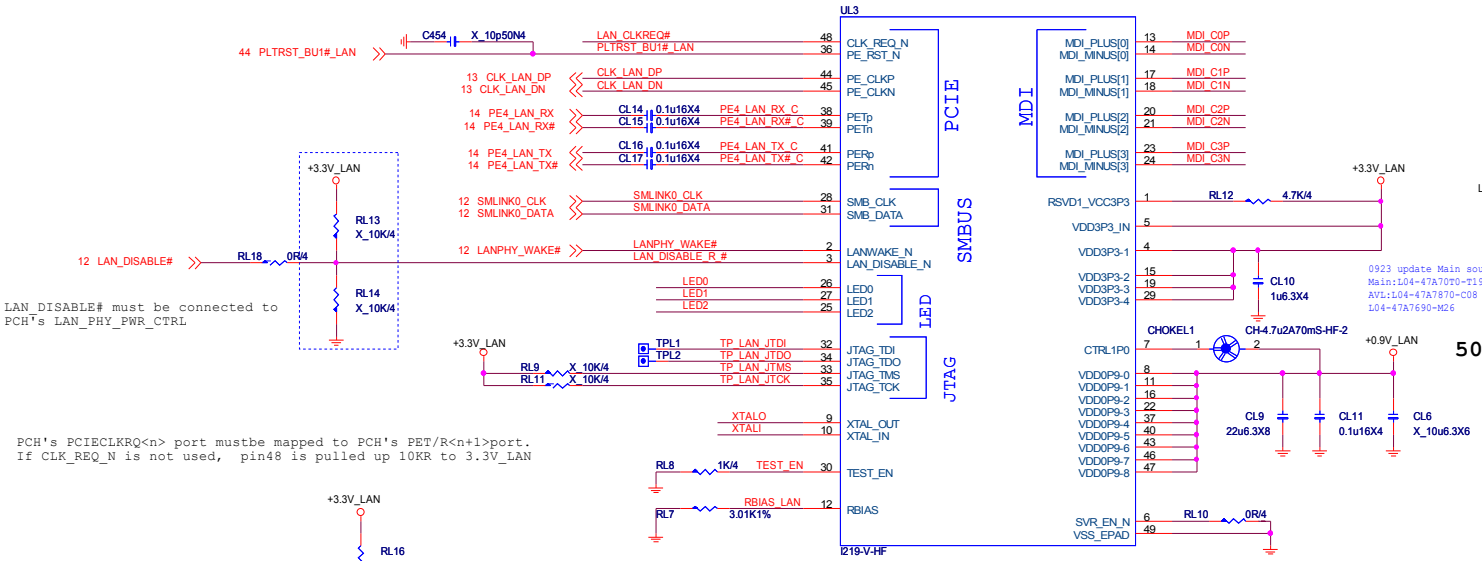
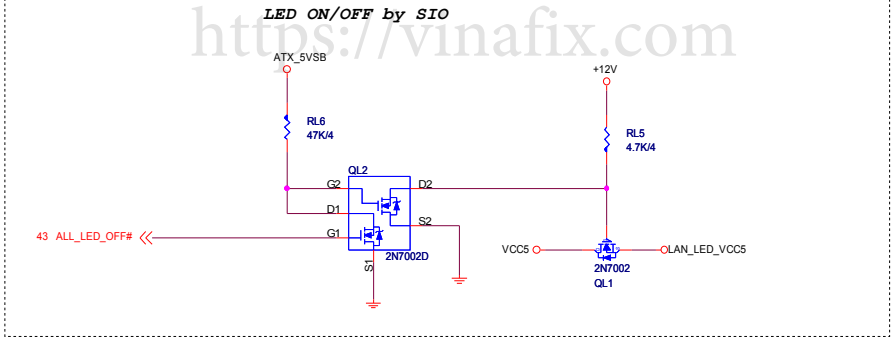
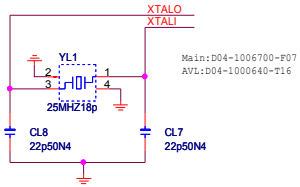
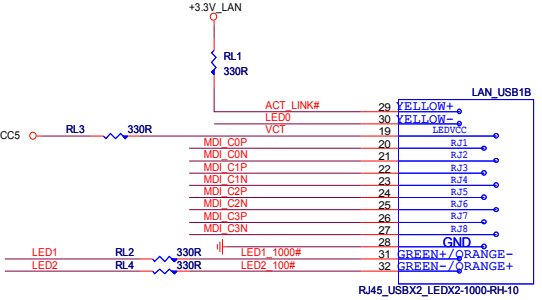
Vinafix.com

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

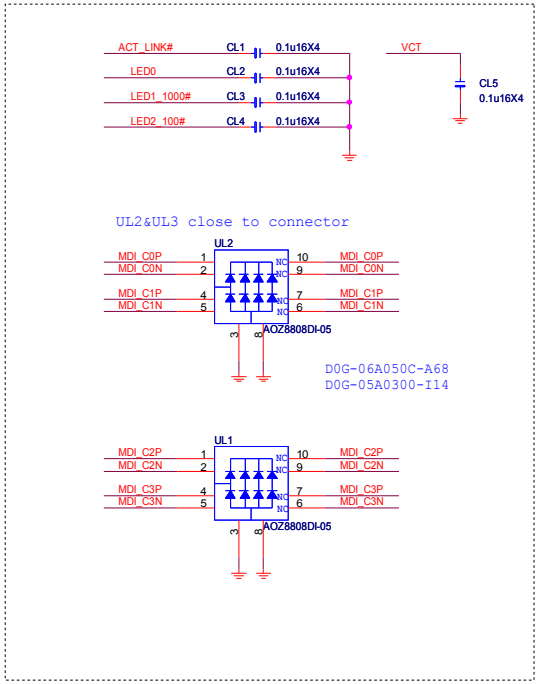




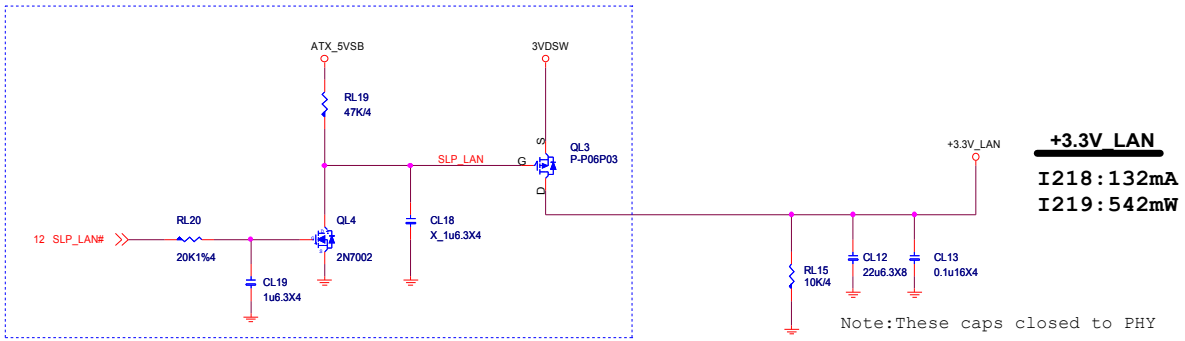




For EMI



support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



+3.3V_LAN

I218:132mA
I219:542mW

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MS-7A64..		
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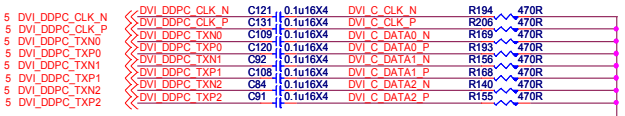
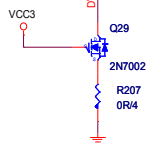
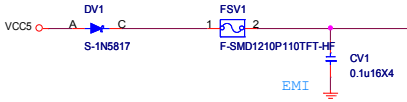
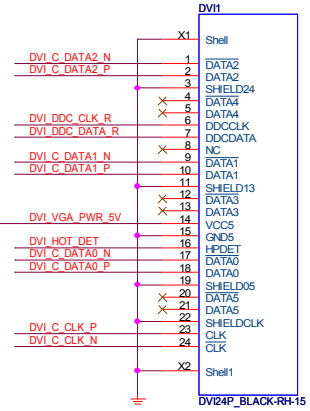
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

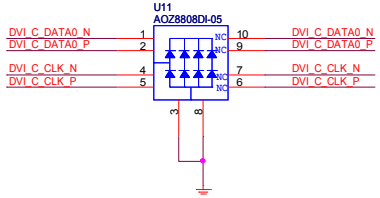








U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



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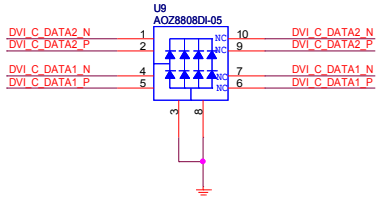
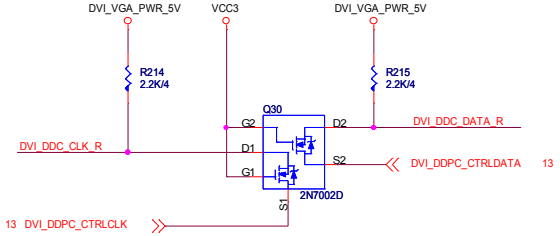
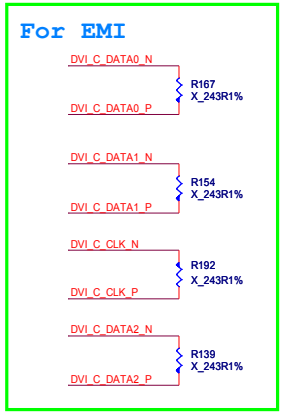
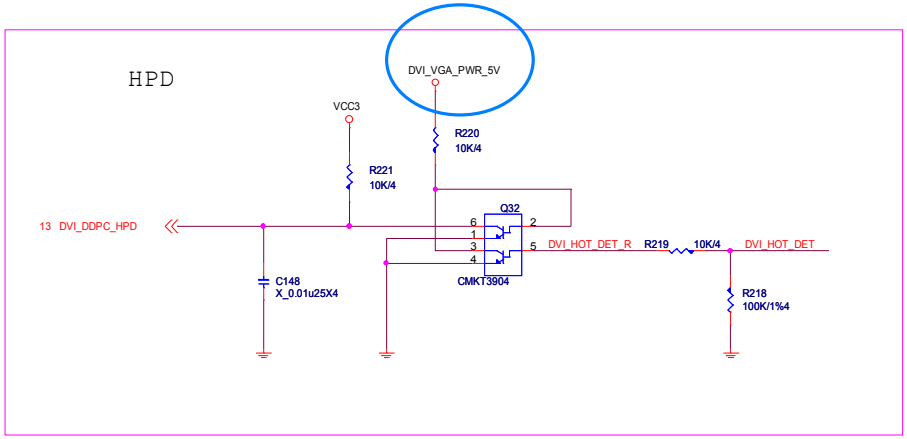
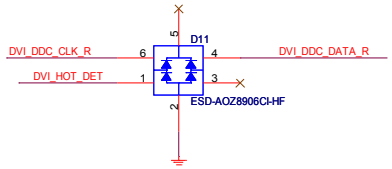
D0G-06A050C-A68











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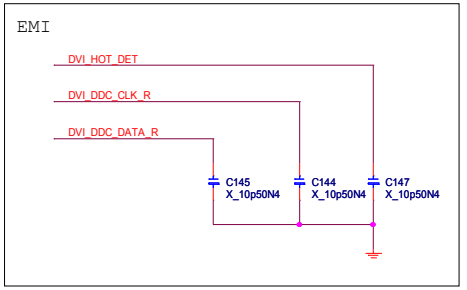
AVL:D0G-45B0510-I14



MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
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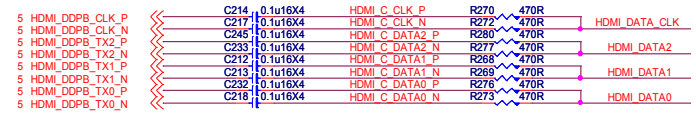
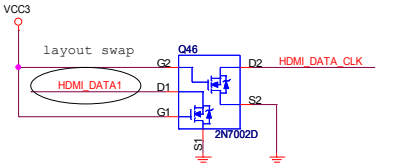
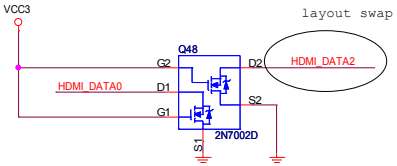
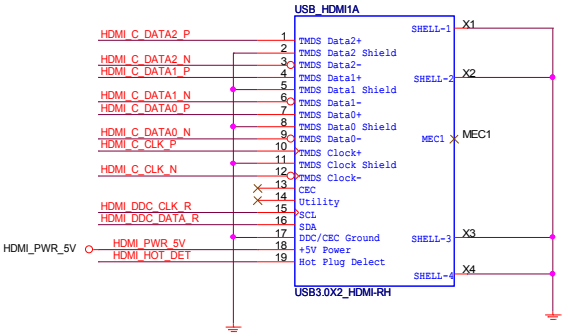
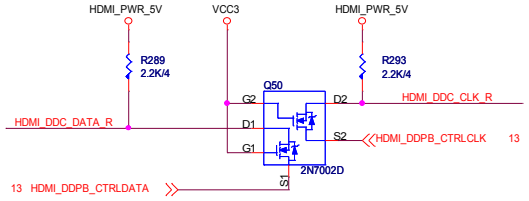
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

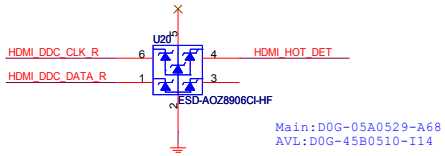


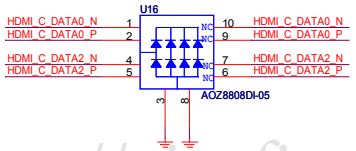


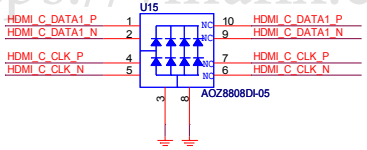


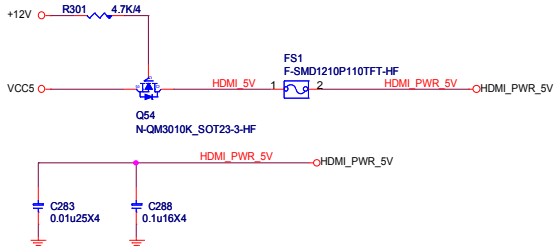




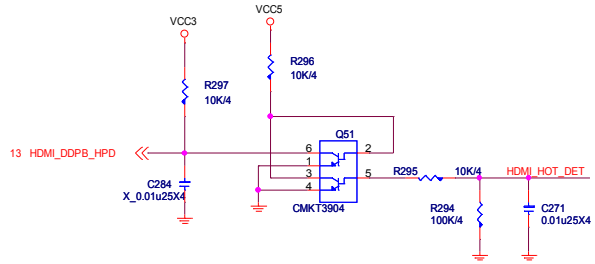




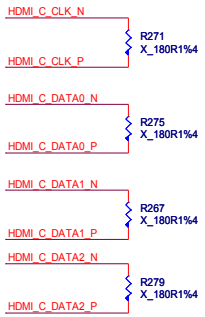




HPD



For EMI



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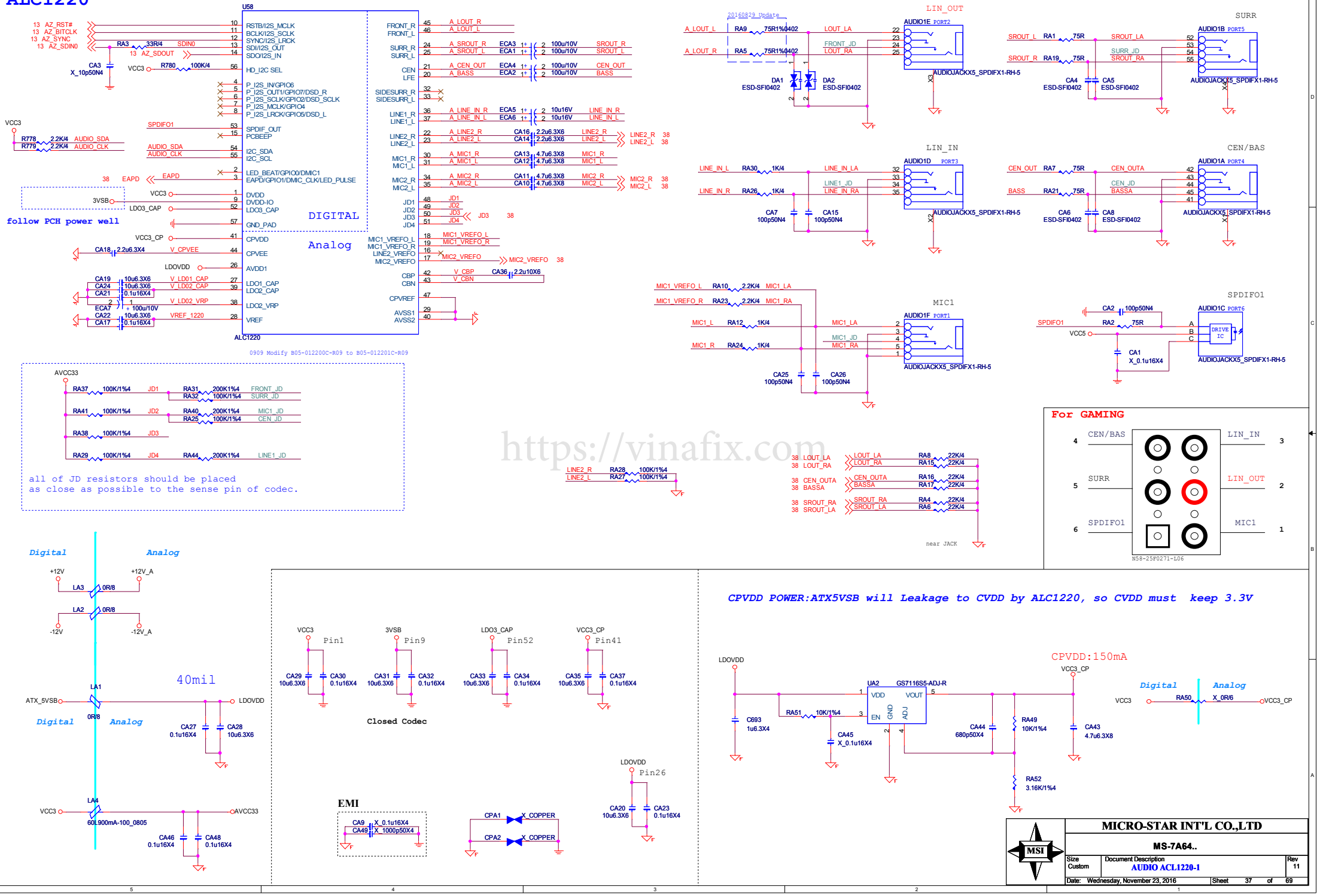
ALC1220


U58
ALC1220
DIGITAL
Analog
follow PCH power well
0909 Modify B05-012200C-R09 to B05-012201C-R09
all of JD resistors should be placed
as close as possible to the sense pin of codec.
LIN_OUT
SURR
LIN_IN
CEN/BAS
MIC1
SPDIFO1
AUDIOJACKX5_SPDIFX1-RH-5
https://vinafix.com
For GAMING
CEN/BAS
LIN_IN
SURR
LIN_OUT
SPDIFO1
MIC1
Digital
Analog
40mil
Closed Codec
EMI
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V
CPVDD:150mA
GS7116S5-ADJ-R
MICRO-STAR INT'L CO.,LTD
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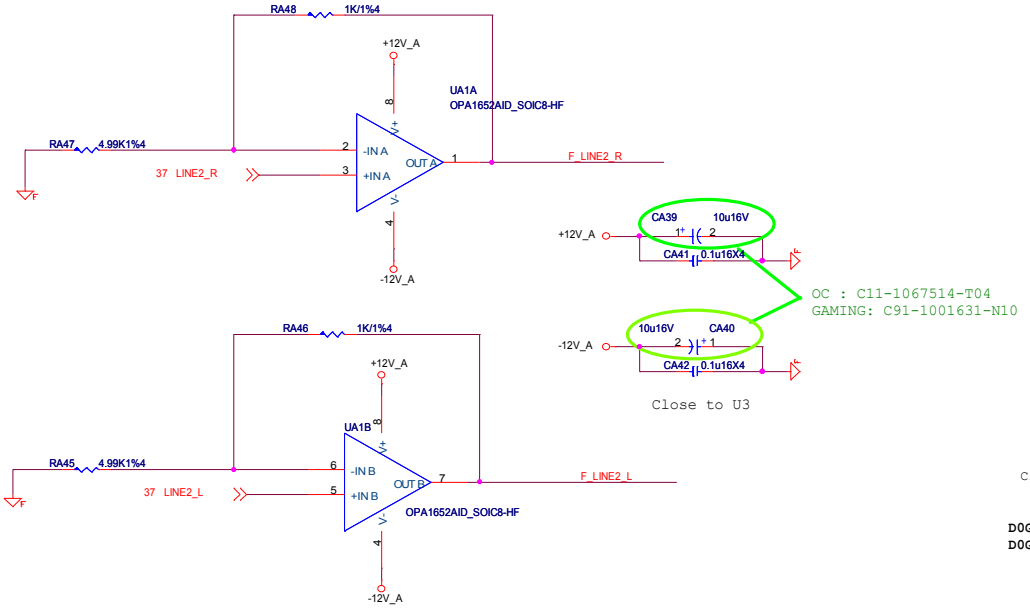
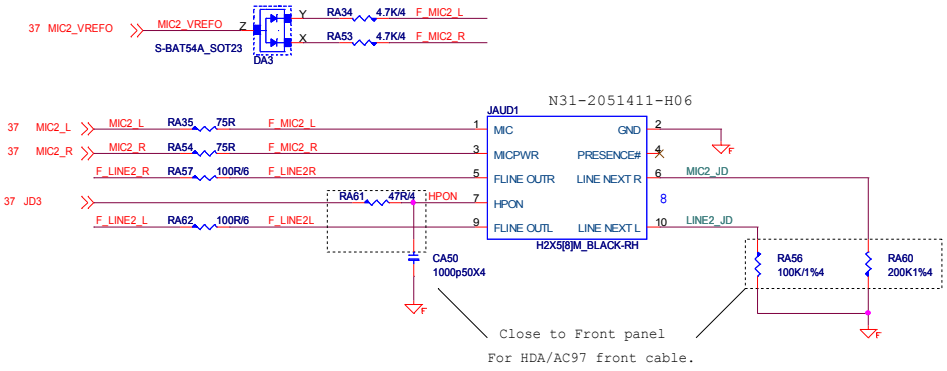
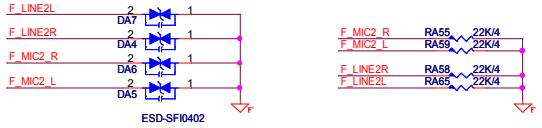




Close to Jack

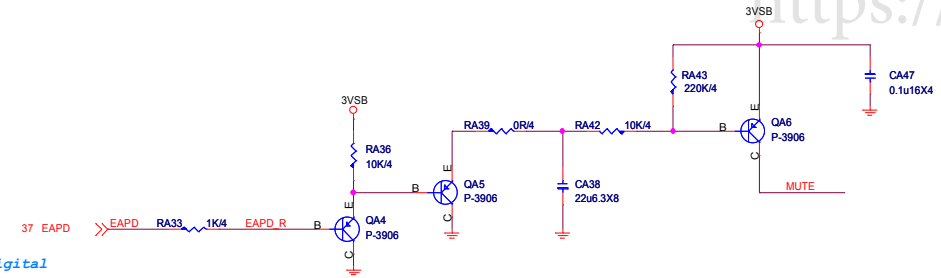
ESD protect

D0G-2710510-I05
D0G-2950500-SI0



Rear Line OUT De-POP circuit

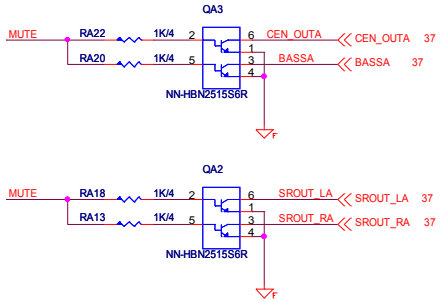
(De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA4,CA5, CA6, CA8,to TVS)



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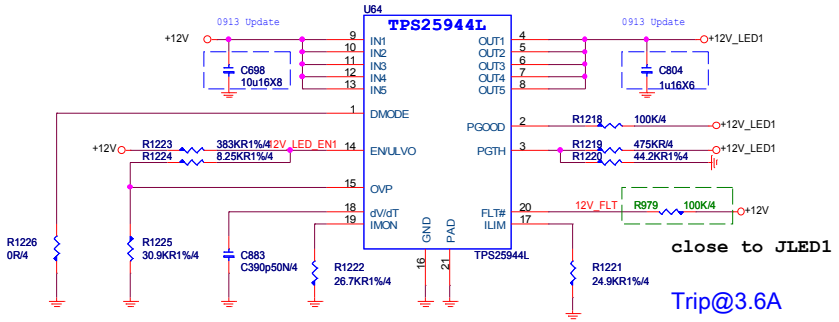
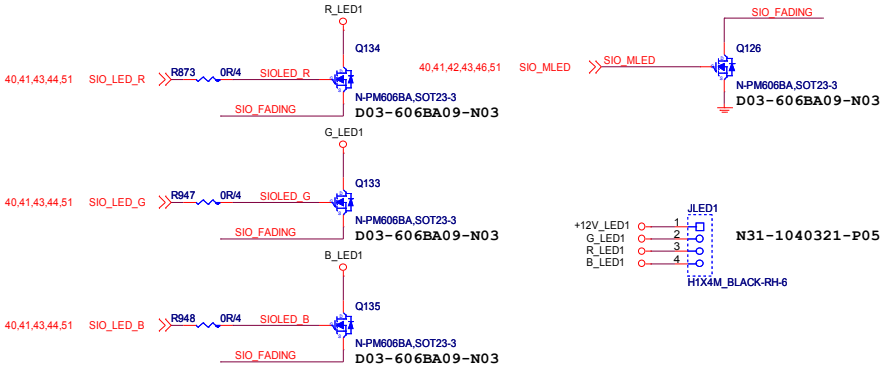
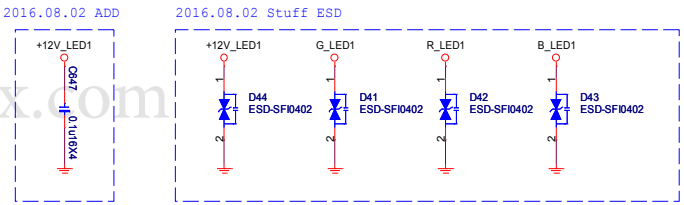
LED STRIPLINE

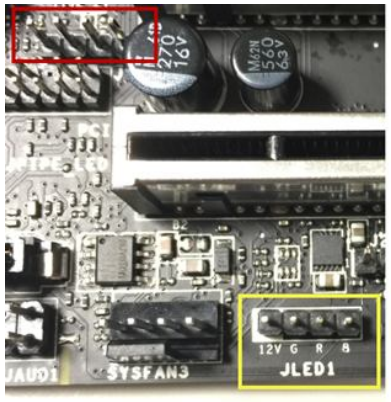
外接LED 燈條 （RGB ）
---- PCB 文字面 （JLED1）
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 （12V/G/R/B），燈條總輸出電流限制為3安培 （12 伏特），
長度限制為2公尺 （待7A20驗證）





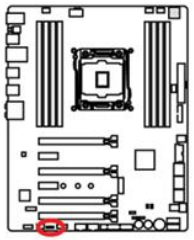
JLED1 CONNECTOR PN PLEASE CHECK PM

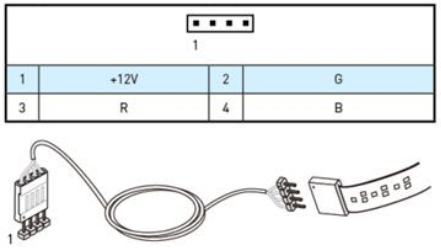




JLED1: RGB LED connector

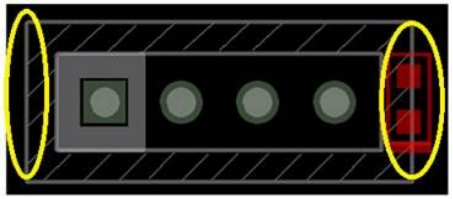
This connector allows you to connect the RGB LED strip.





Important

- *This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.*
- *Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.*
- *Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.*



JLED1電源警示燈請擺在旁側

MICRO-STAR INT'L CO.,LTD

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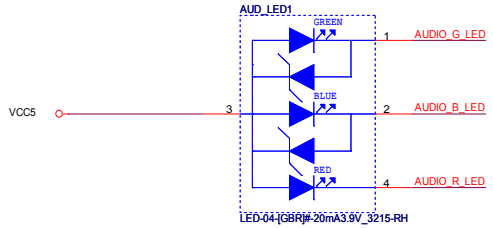
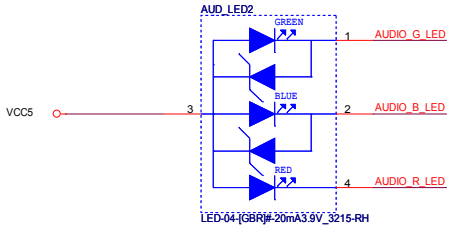
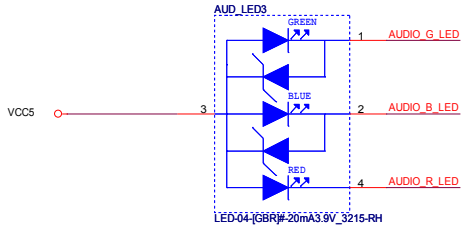
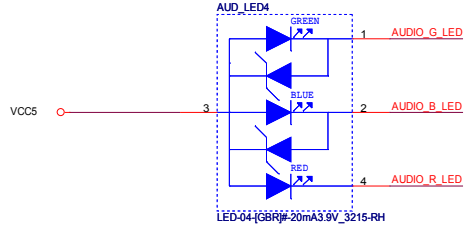
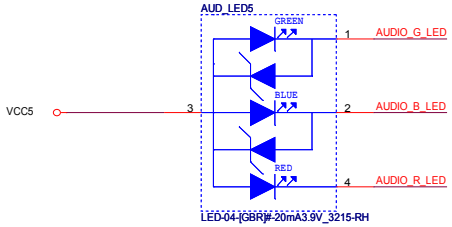
AUDIO_MOAT LED

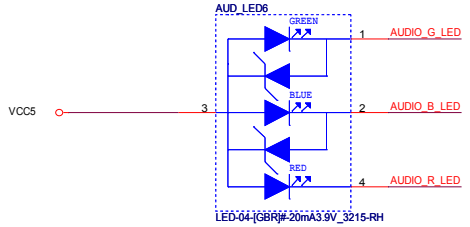


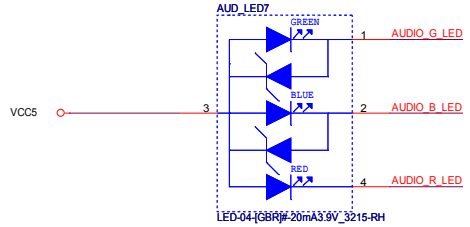


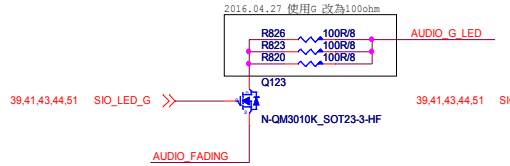




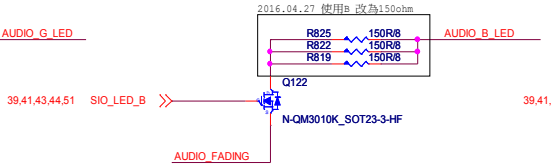




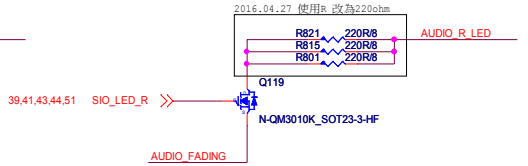




Vf=2.7 V~3.9V
5V-2.7V/33.3=0.069A
0.069A*0.069A*33.3=0.158W



Vf=2.7 V~3.9V
5V-2.7V/50=0.046A
0.046A*0.046A*50=0.105W



Vf=1.6 V~2.4V
5V-1.6V/73.3=0.046A
0.046A*0.046A*73.3=0.155W

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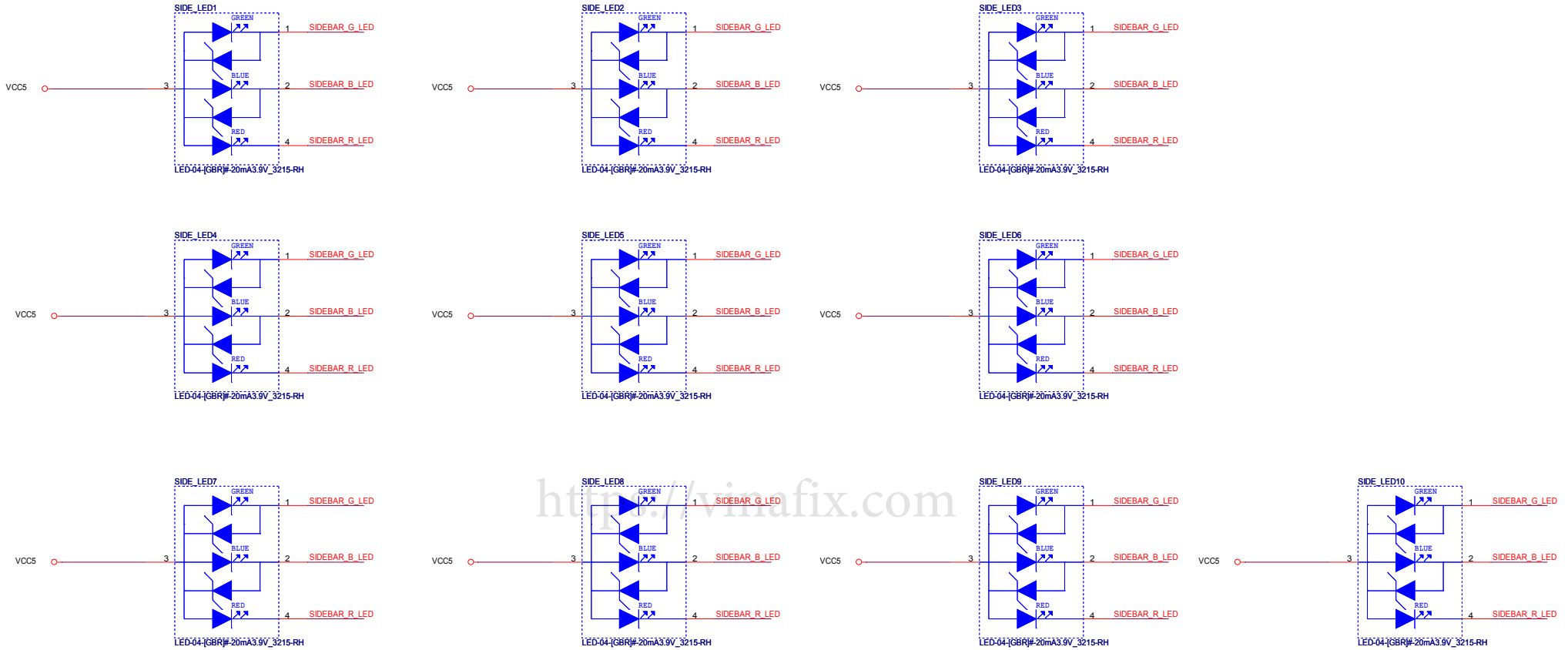
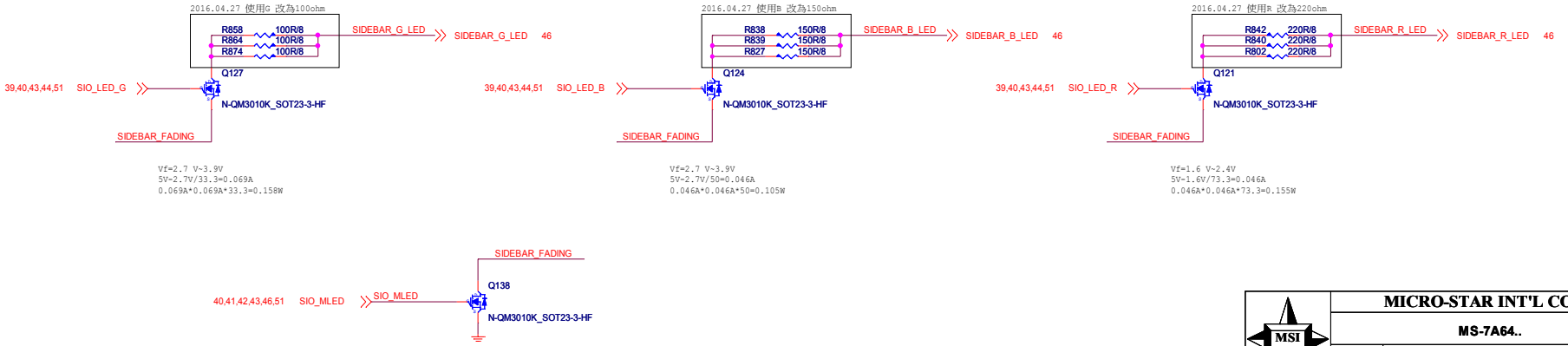
LED SIDEBAR

NEW FUNCTION





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Size: Custom	Document Description: LED SINDEBAR	Rev: 11
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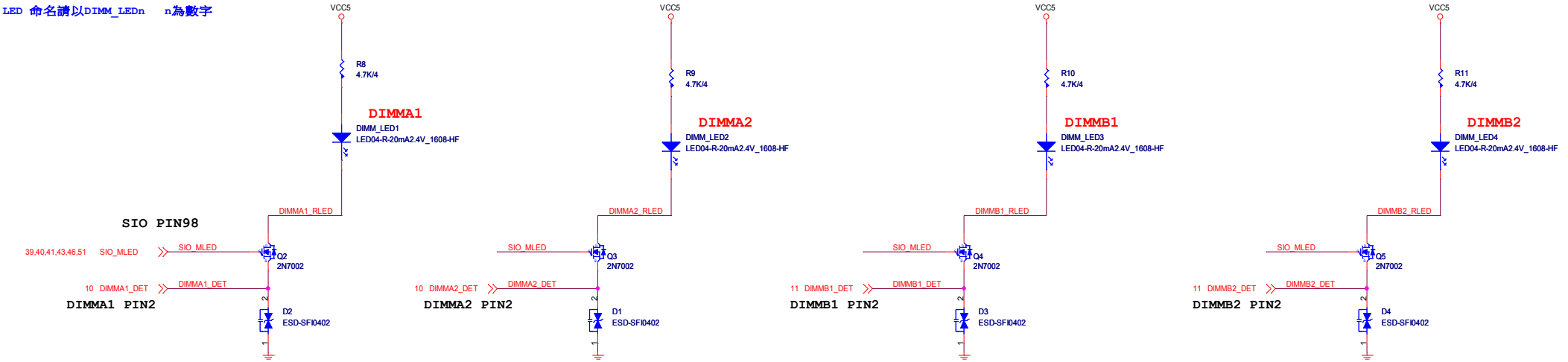
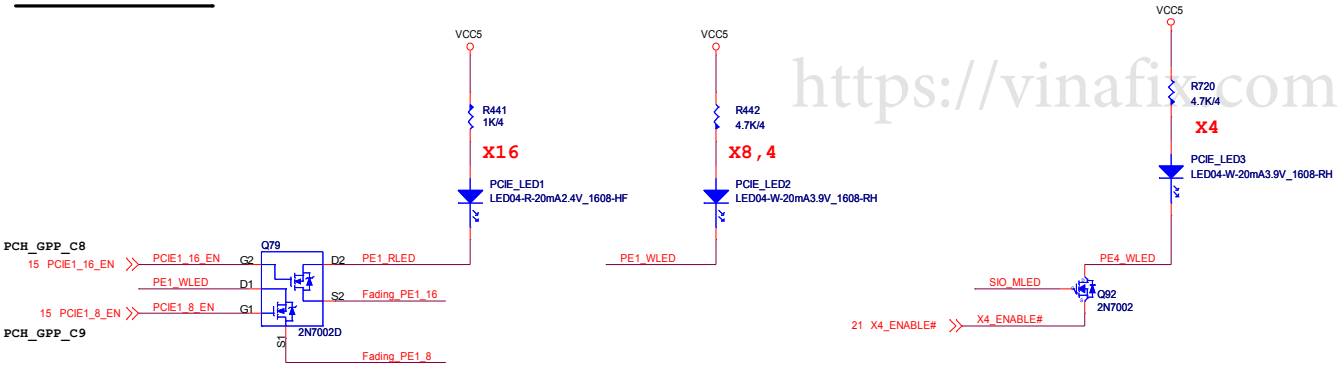
DIMM_SLOT

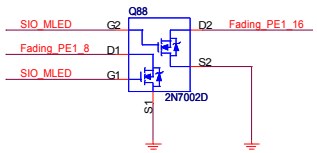
紅 : D0C-040P100-H91

LED 命名請以DIMM_LEDn n為數字



PCIE SLOT LED





MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: LED DIMM/PCIE	Rev: 11
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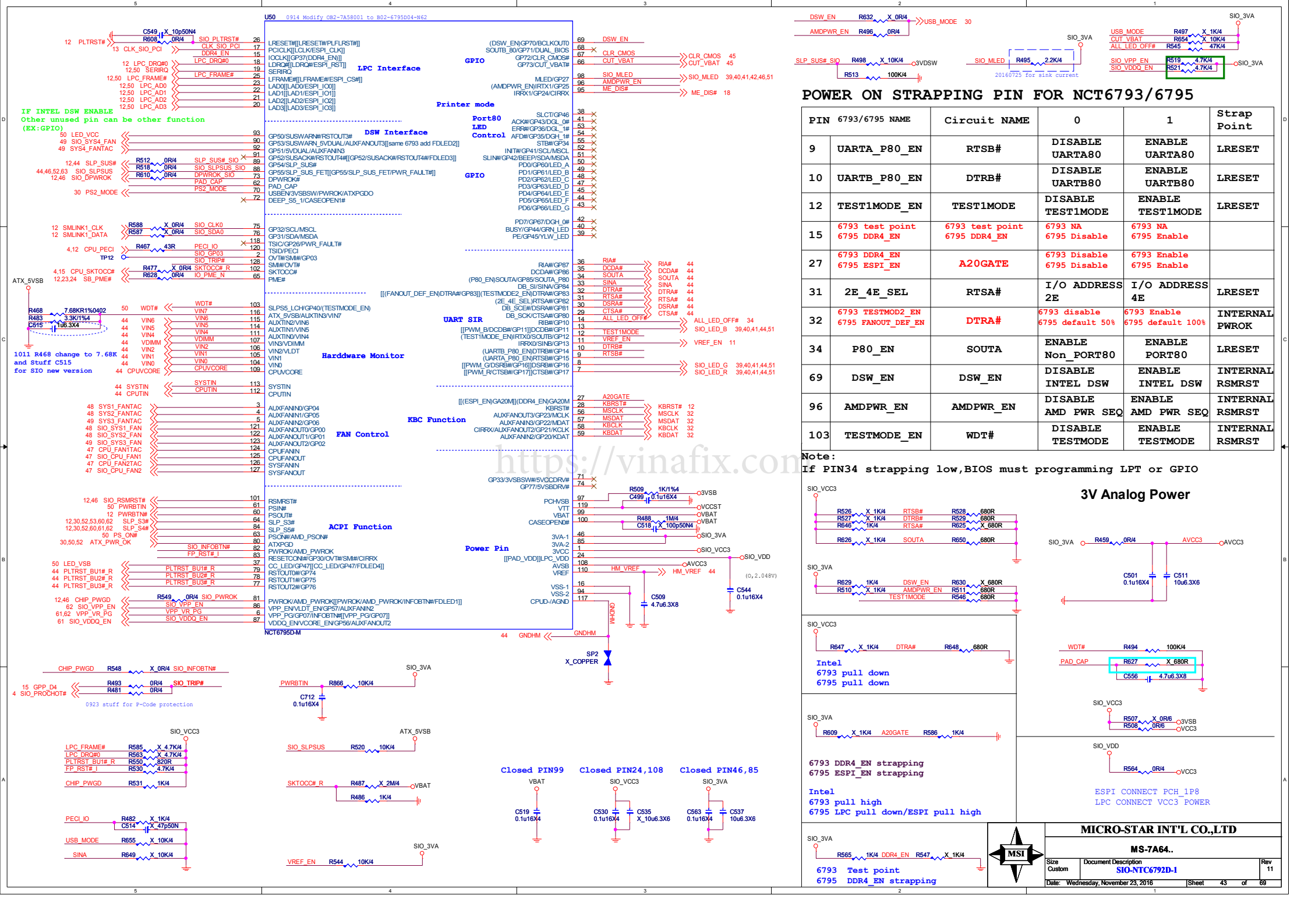

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

3V Analog Power

Intel
6793 pull down
6795 pull down

6793 DDR4_EN strapping
6795 ESPI_EN strapping

Intel
6793 pull high
6795 LPC pull down/ESPI pull high

6793 Test point
6795 DDR4_EN strapping

ESPI CONNECT PCH_1P8
LPC CONNECT VCC3 POWER

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: SIO-NTC6792D-1
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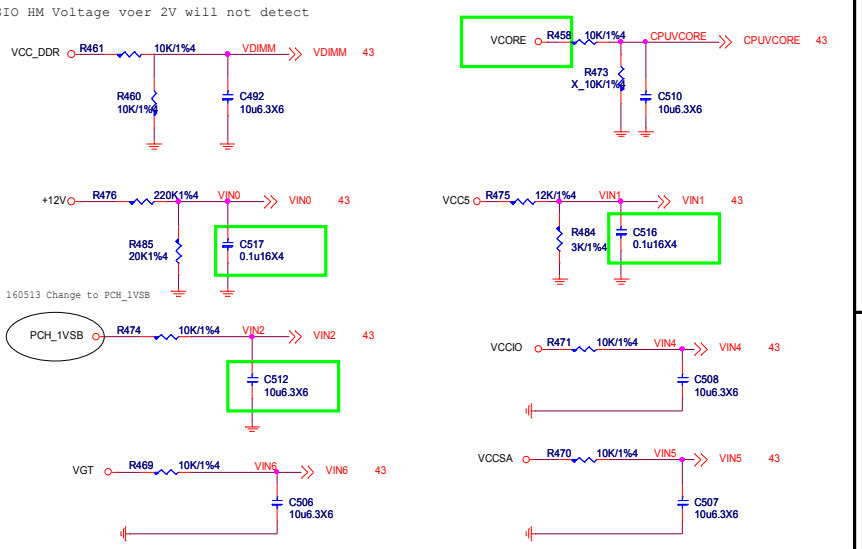
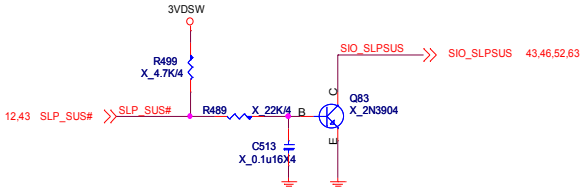
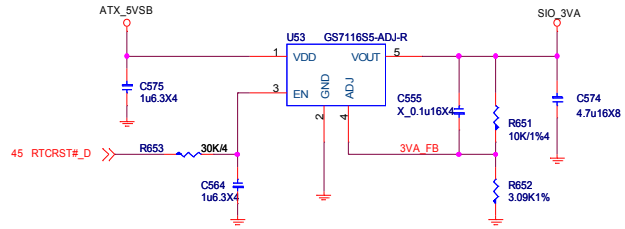
HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



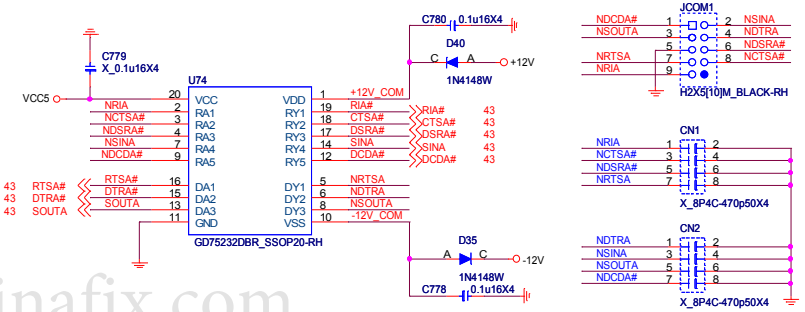
SLP_SUS Co-lay circuit



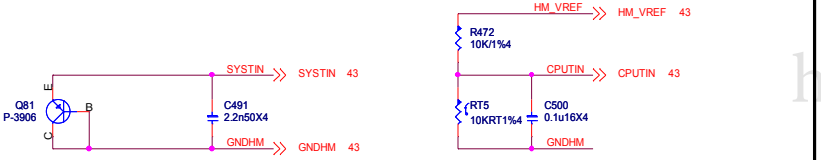


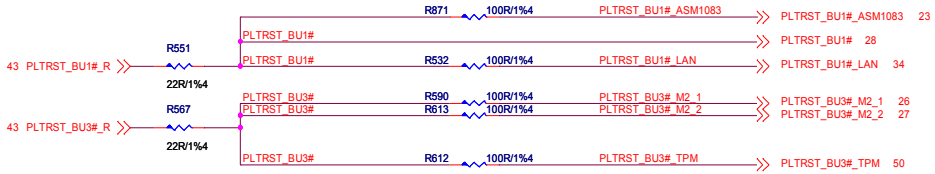
SERIAL PORT 1

NEW FUNCTION

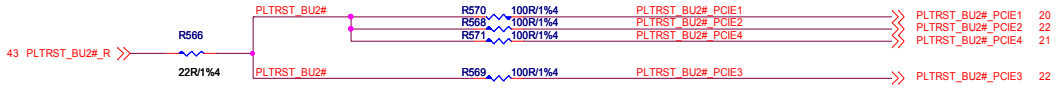


Thermal Monitor

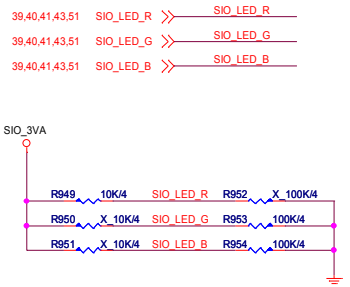




WW



RGB LED defult setting



Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

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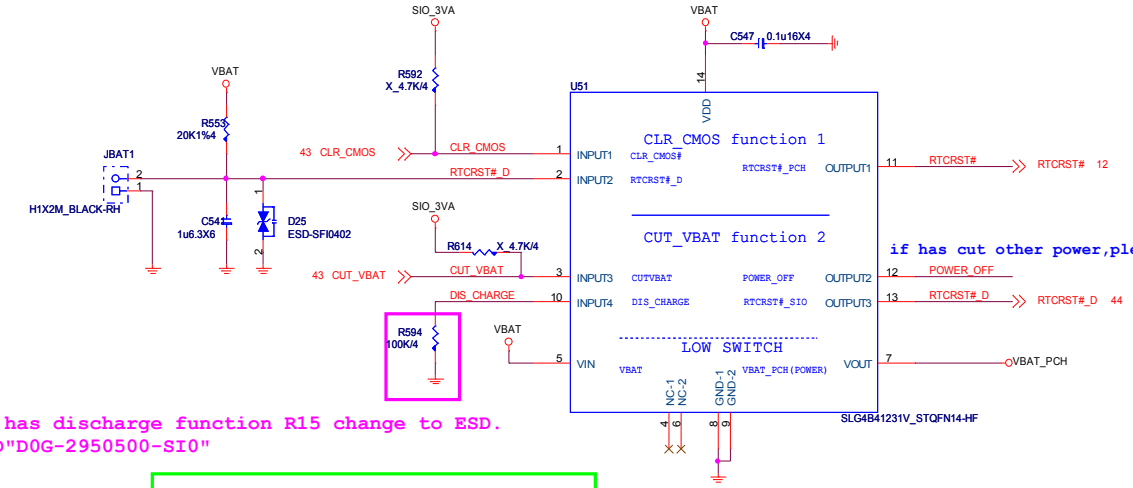
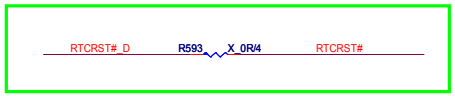
CLR_CMOS



if has cut other power,please use output 2.

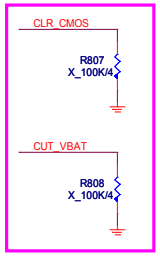
If has discharge function R15 change to ESD.
ESD"D0G-2950500-SI0"



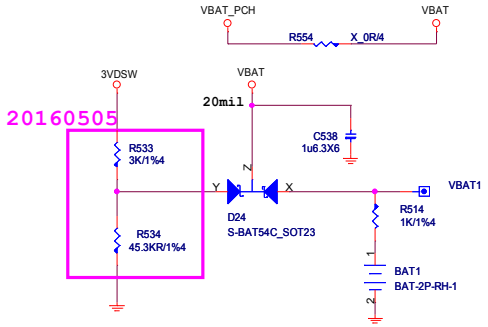
Co-Lay NOT USE U12 , R139 STUFF

If STUFF R139 Please Check RTCRST# Double Pull High

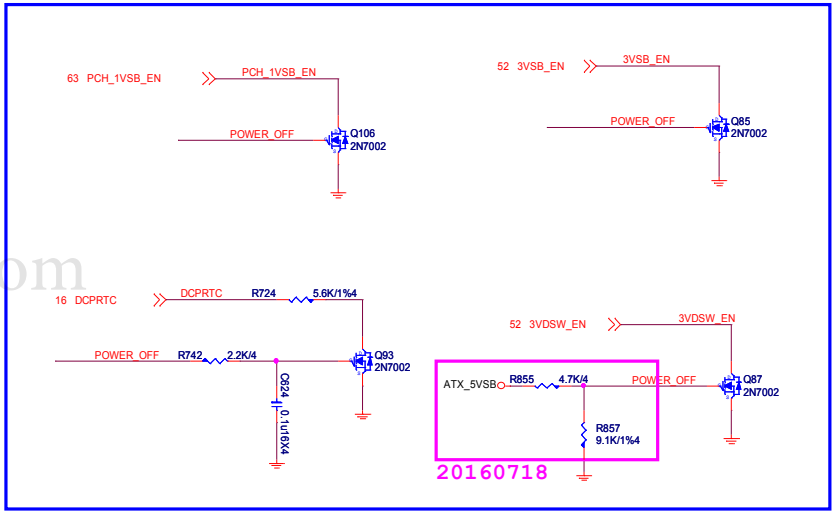
20160629



VBAT



Co-Lay NOT USE U12 , ALL UNSTUFF



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

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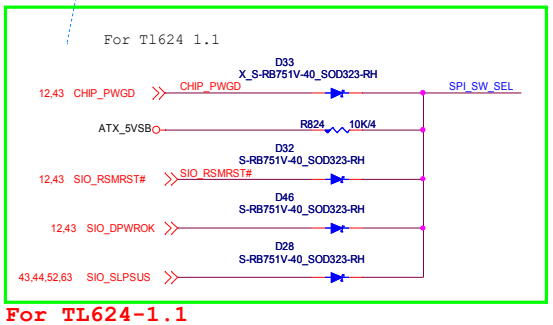
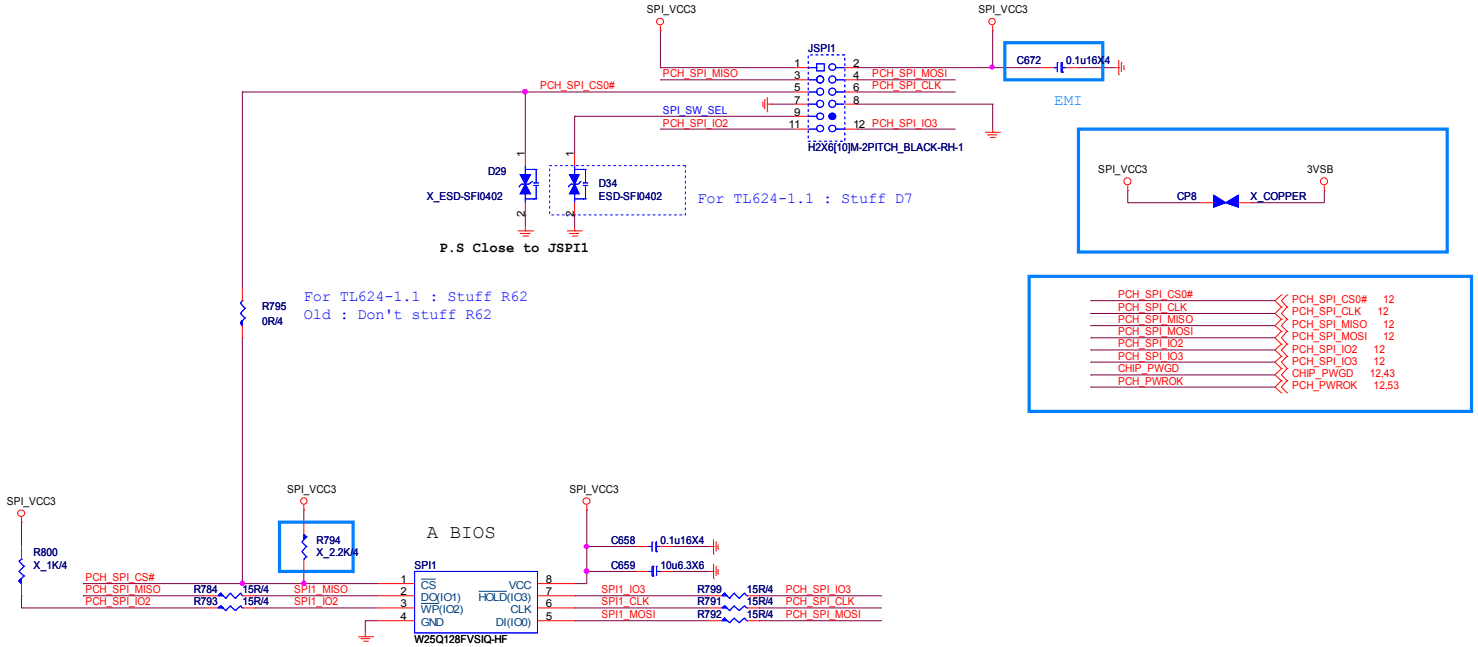
Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

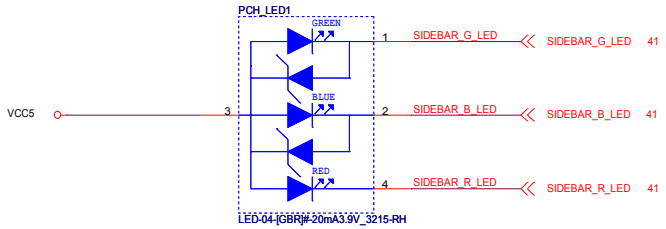


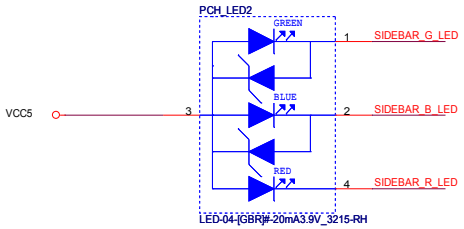
For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272

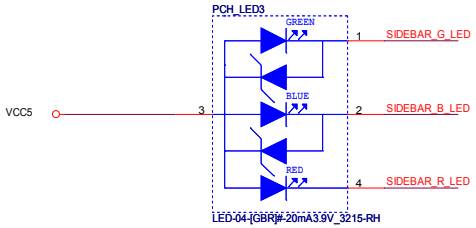


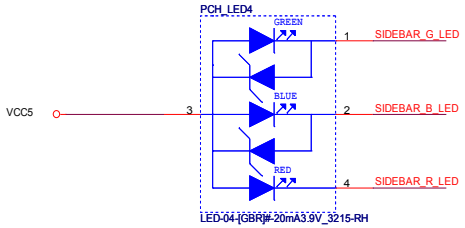
PCH LED

NEW FUNCTION









MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: BIOS	Rev: 11
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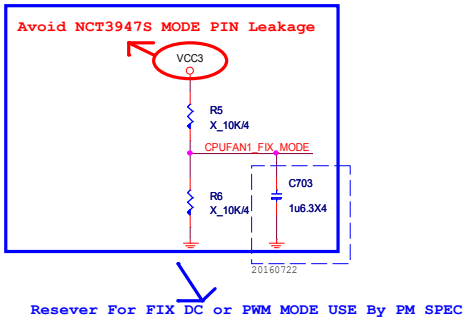
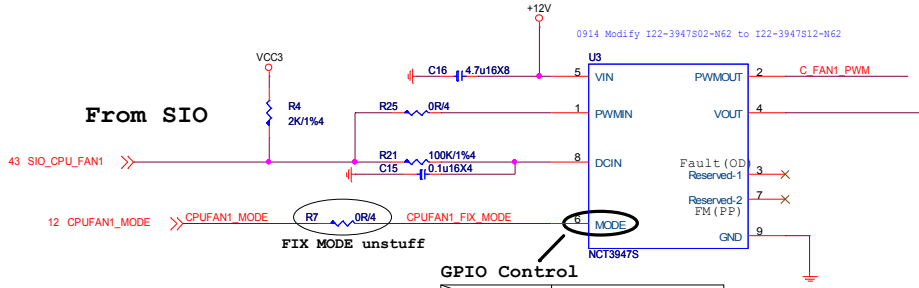
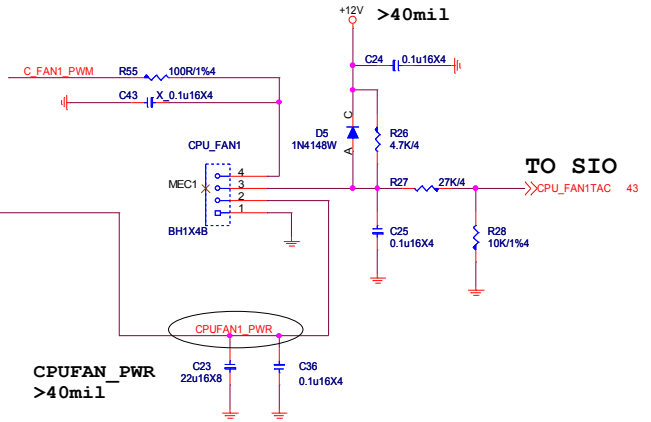
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



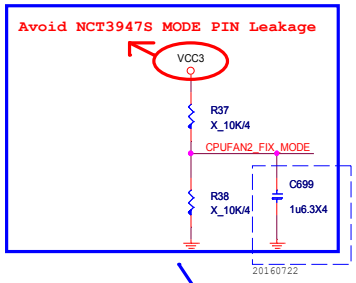


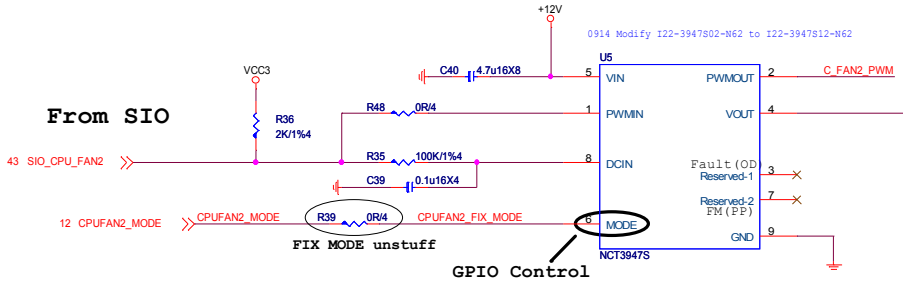
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



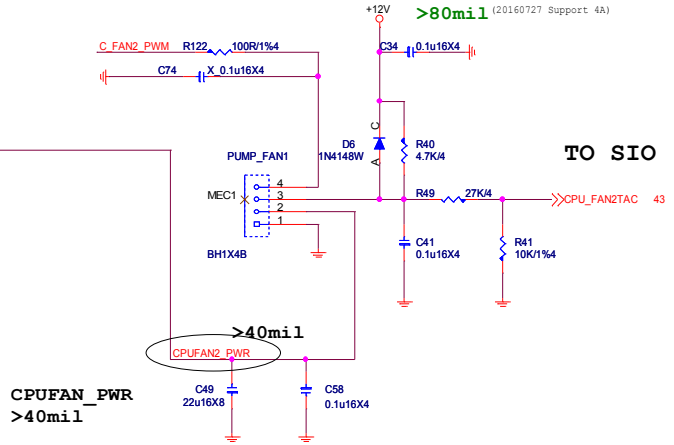
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE





	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

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Custom	CPU FAN1/PUMPFAN1	11

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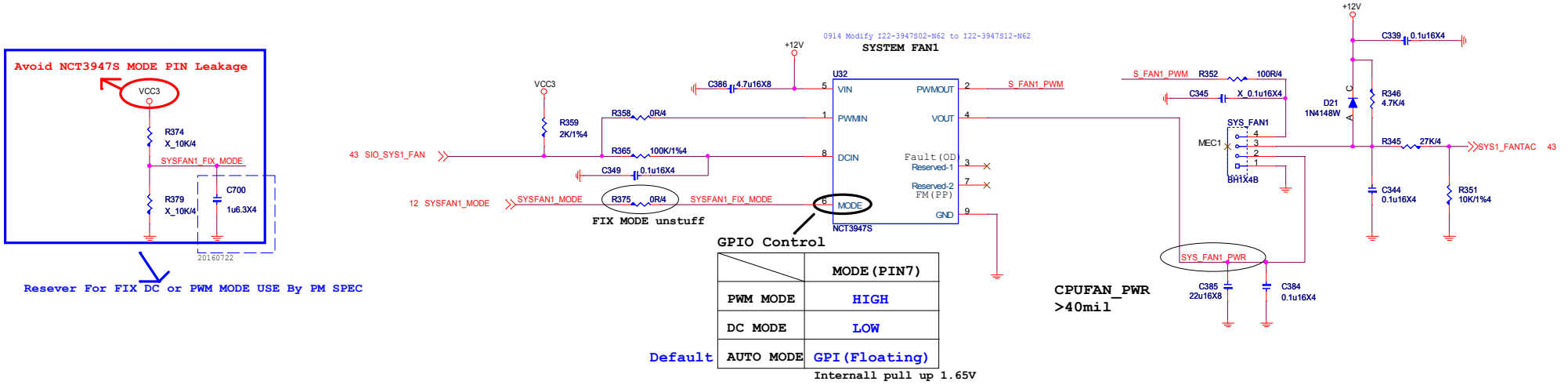
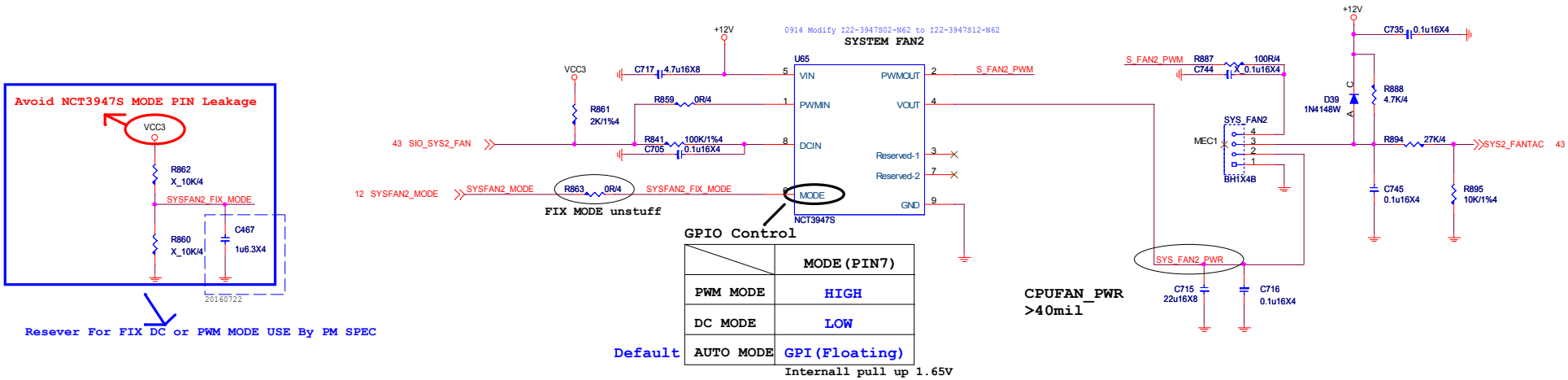
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



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MS-7A64..	
Size: Custom	Document Description: SYSTEM FAN1&2
Rev: 11	
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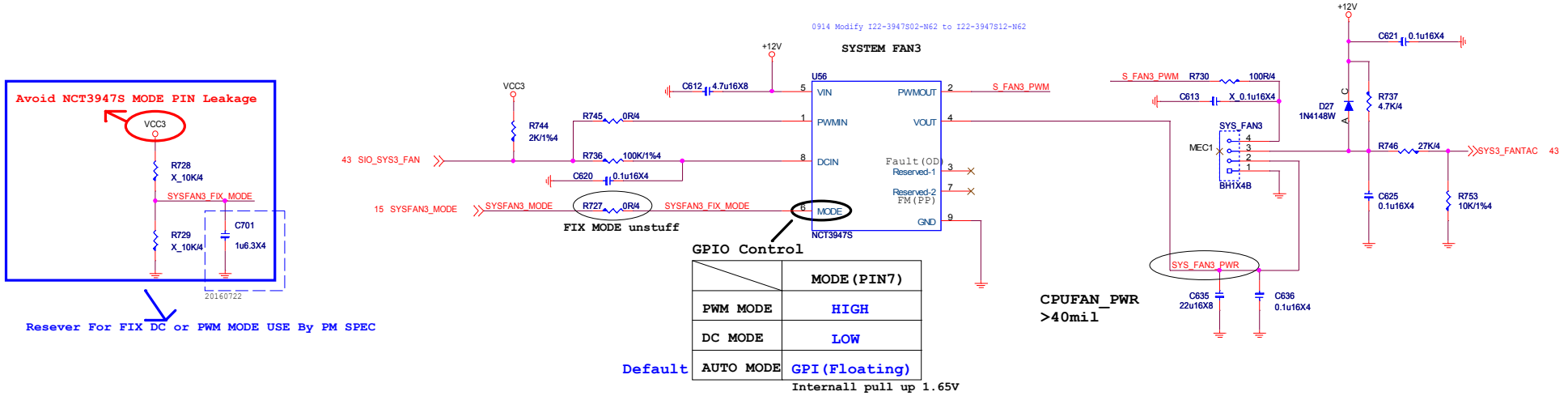
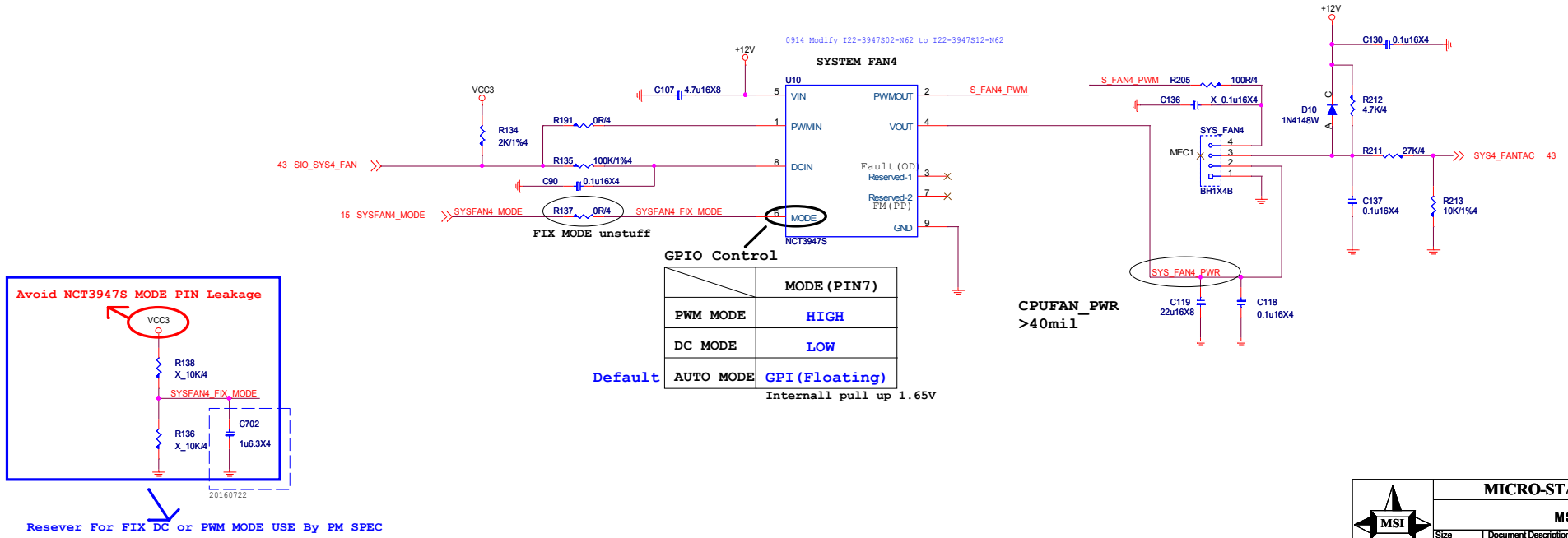
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: SYSTEM FAN3&4 — Rev: 11
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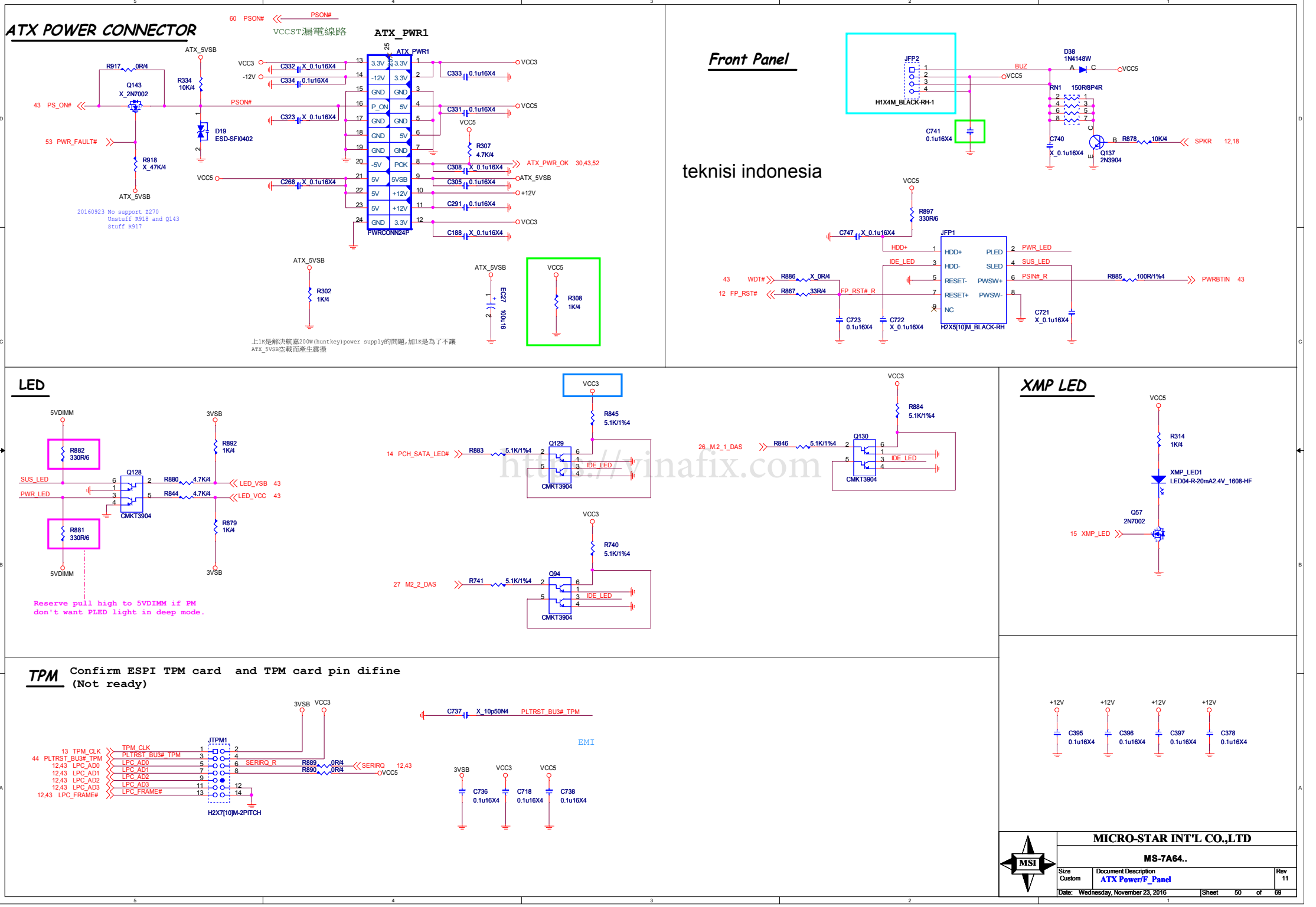
ATX POWER CONNECTOR
ATX_PWR1
PWRCONN24P
VCCST漏電線路
20160923 No support 2270
Unstuff R918 and Q143
Stuff R917
上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓
ATX_5VSB空載而產生震盪
Front Panel
teknisi indonesia
H1X4M_BLACK-RH-1
H2X5[10]M_BLACK-RH
CMKT3904
LED
Reserve pull high to 5VDIMM if PM
don't want PLED light in deep mode.
XMP LED
LED04-R-20mA2.4V_1608-HF
TPM
Confirm ESPI TPM card and TPM card pin difine
(Not ready)
H2X7[10]M-2PITCH
EMI
MICRO-STAR INT'L CO.,LTD
MS-7A64..
ATX Power/F_Panel
Wednesday, November 23, 2016
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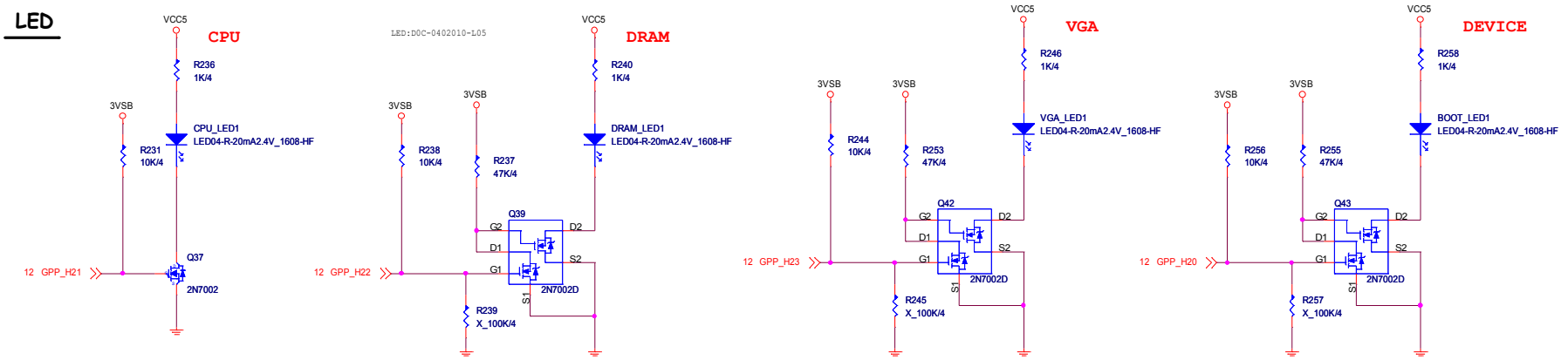
LED

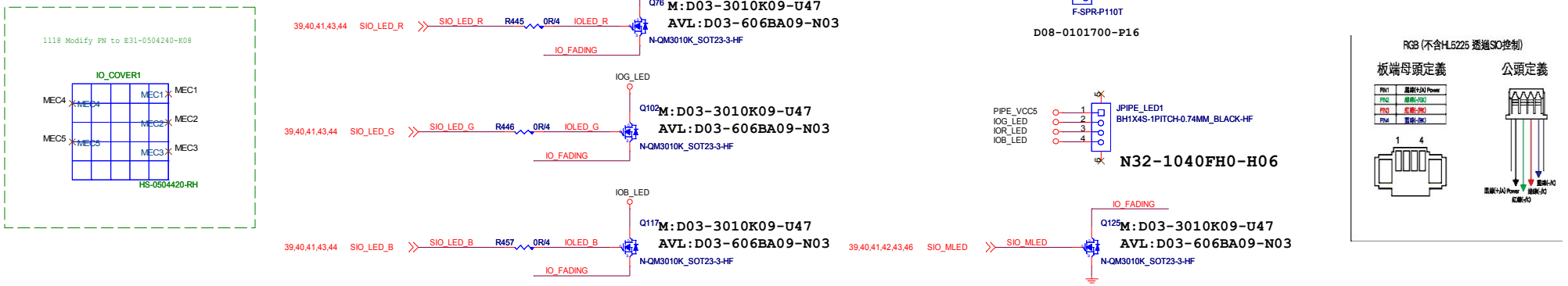


關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。
   （系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

IO Cover + RGB LED



方案二 ： MCU Solutin 置於HS 背後需與國格討論 ， LED總功率算法 ：
--- 三色 ： GRB = 使用電壓 5V*0.06 電流 x 總燈數
--- 單色 ： G、B、W = 使用電壓 3V*0.02 電流 x 總燈數
--- 單色 ： R = 使用電壓 2V*0.02 電流 x 總燈數

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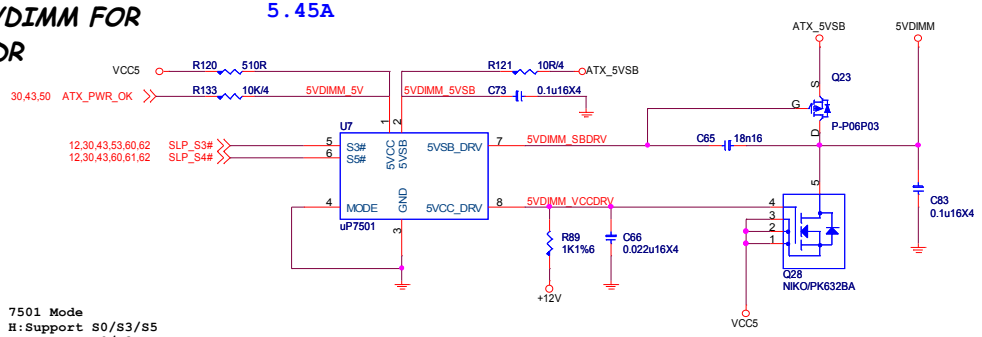
5VDIMM FOR DDR

5.45A

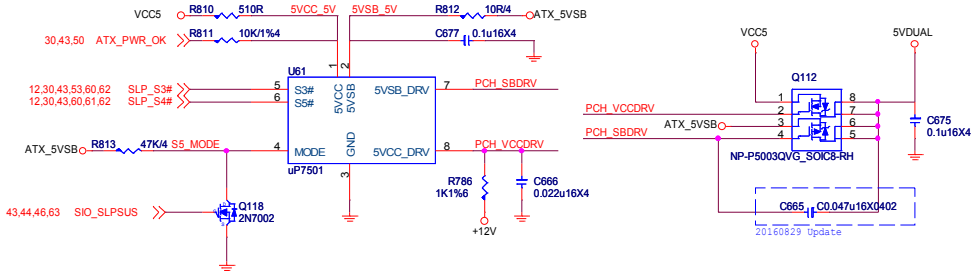


7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

5VDUAL

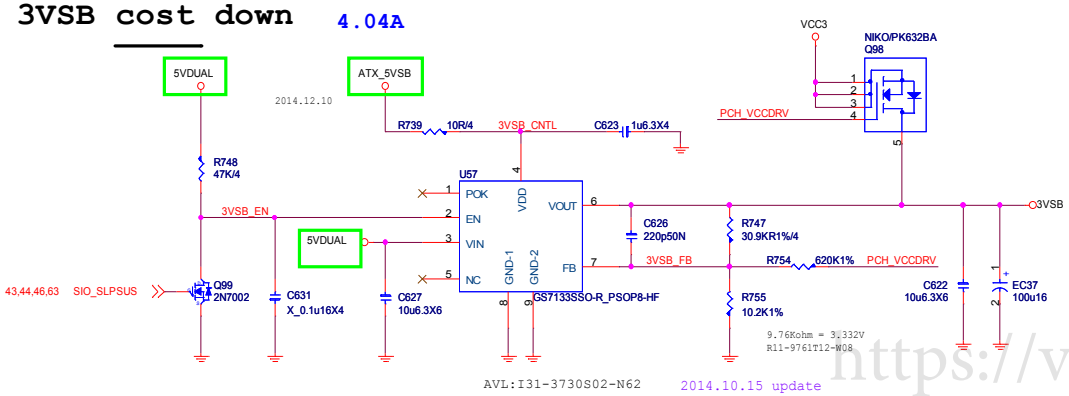
5VDUAL is power source of 1P0SB

PCH:2.95A
3VSB:4.04A
MAX:6.99A



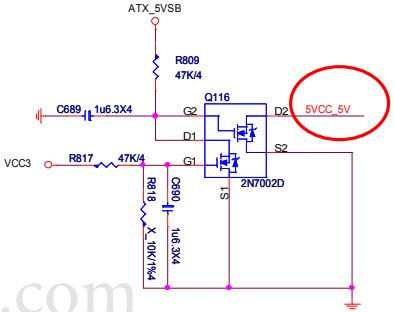
3VSB cost down

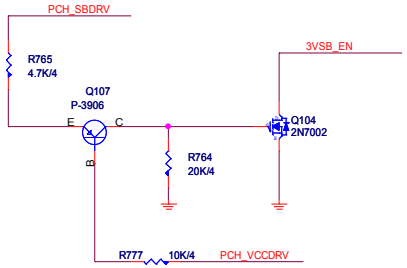
4.04A



AVL:I31-3730S02-N62 2014.10.15 update

VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.



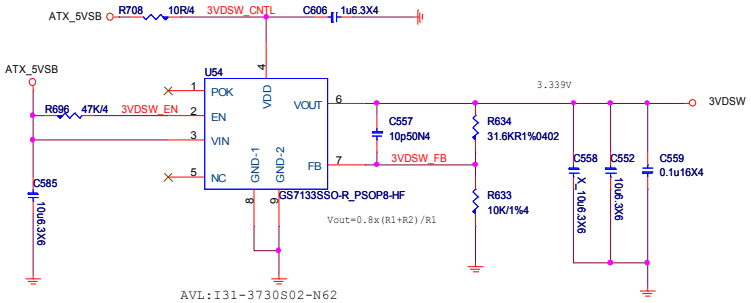


3VSB_EN → 3VSB_EN 45

防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

3VDSW

0.422A



AVL:I31-3730S02-N62

3VDSW_EN → 3VDSW_EN 45

MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
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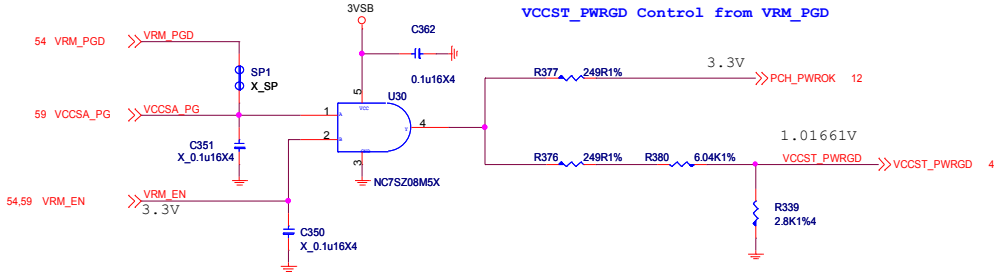
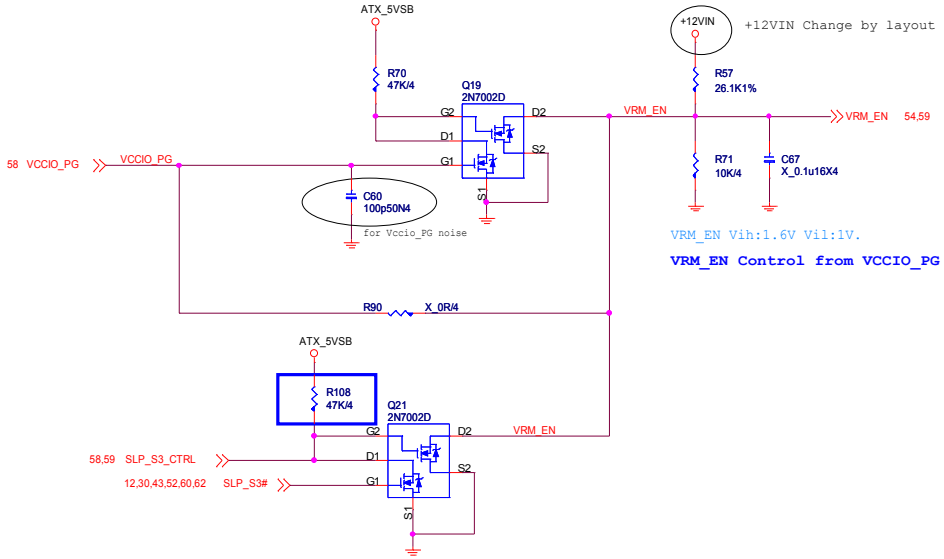
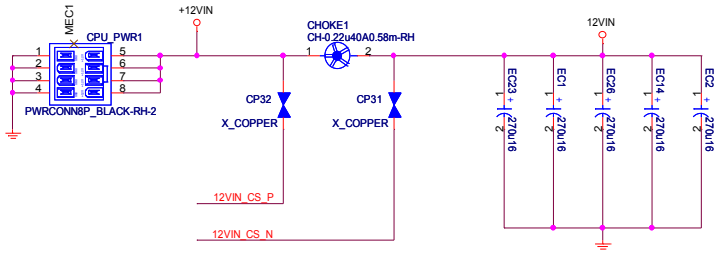
VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PGD

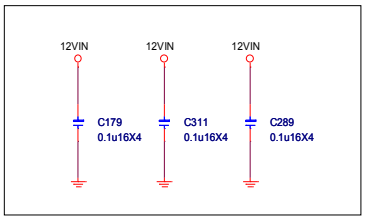


VRM_EN Control from VCCIO_PG

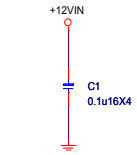




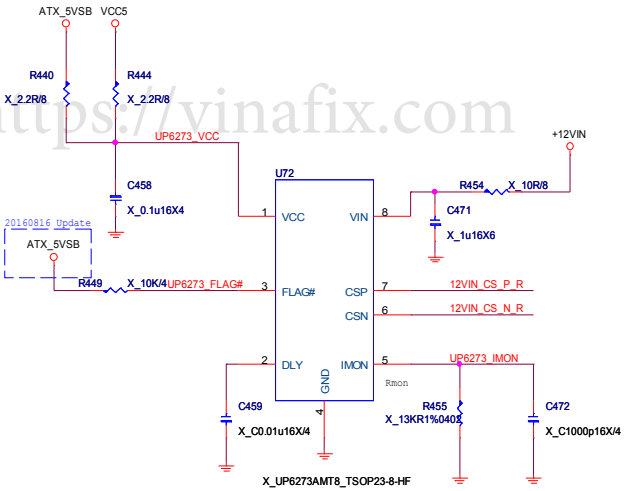
Iripple=30.95A
VCORE 18.101A
VGT 8.457A
VCCSA 4.392A



CLose to JPWR2

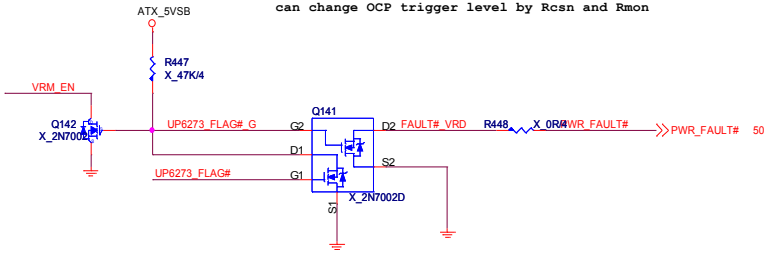


20160923 No support Z270, So unstuff

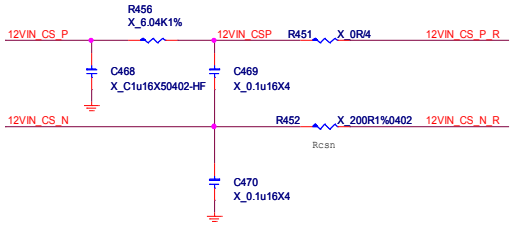


https://vinafix.com

Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon



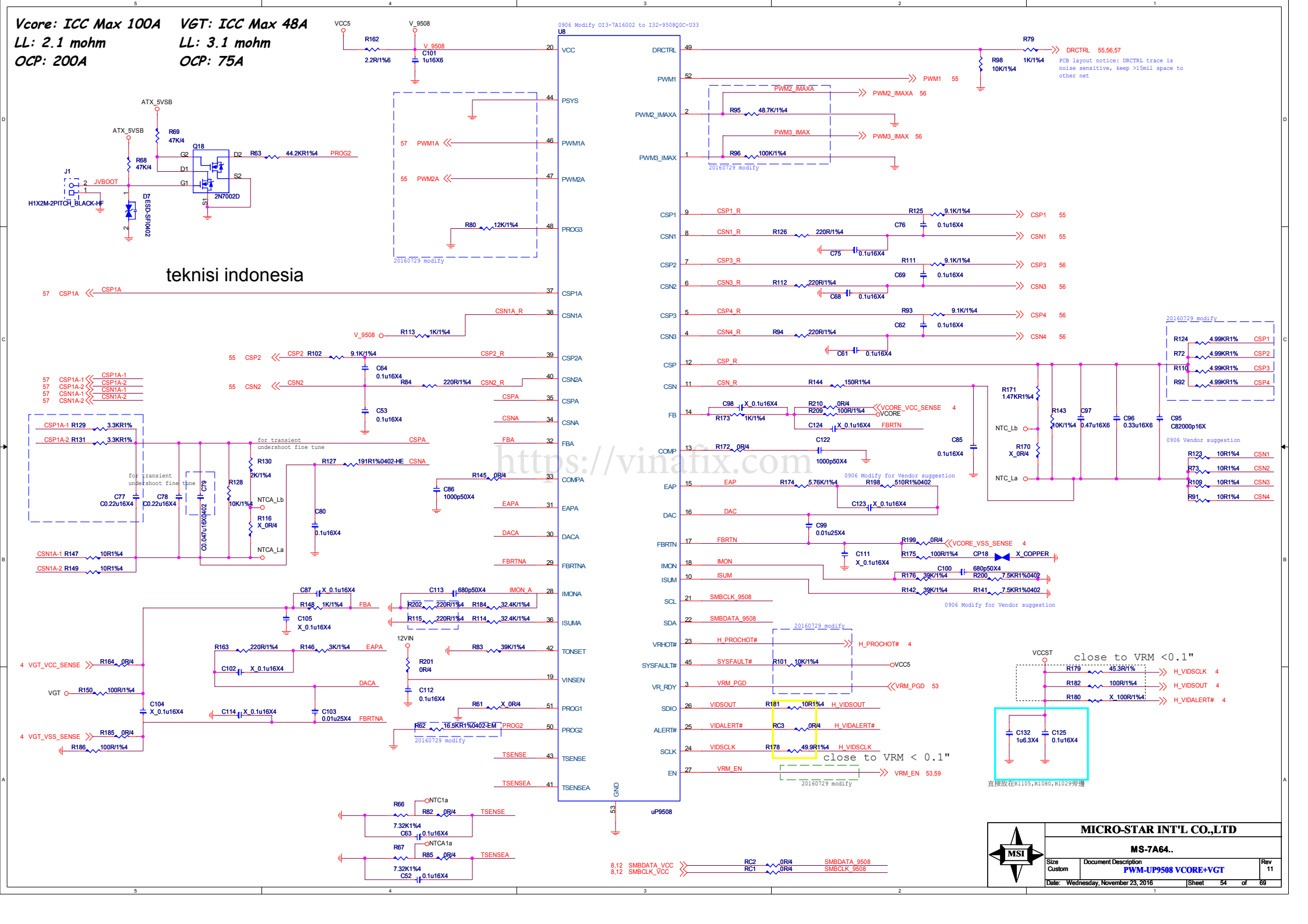
RCSP x Cap = choke(L)/choke(DCR) x 1.1K
RCSP x 0.1 = 0.42/0.72 x 1.1K
RCSP = 6.41KR

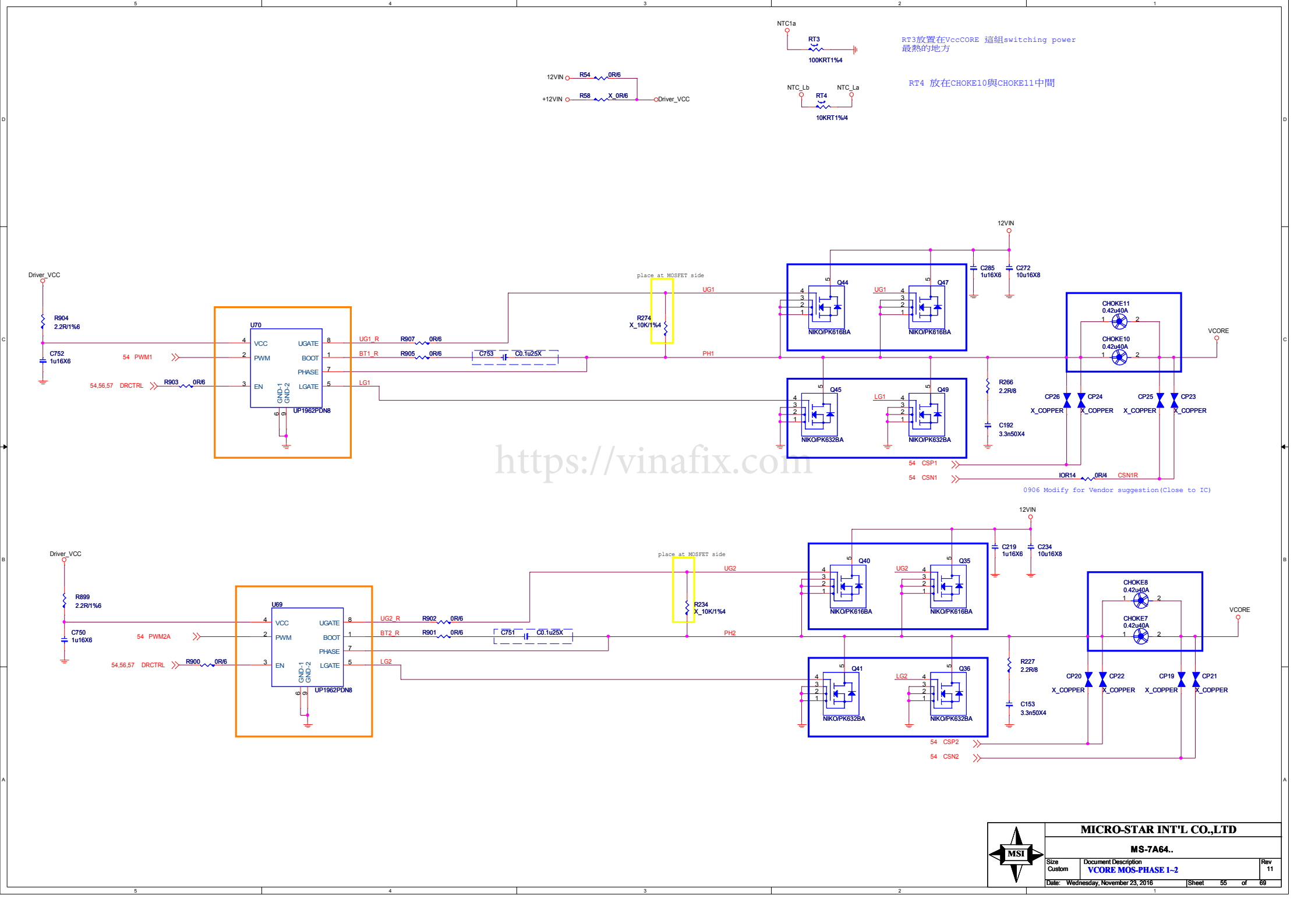


RCSN = choke(DCR) / 10
RCSN = 72R

Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 200A

VGT: ICC Max 48A
LL: 3.1 mohm
OCP: 75A





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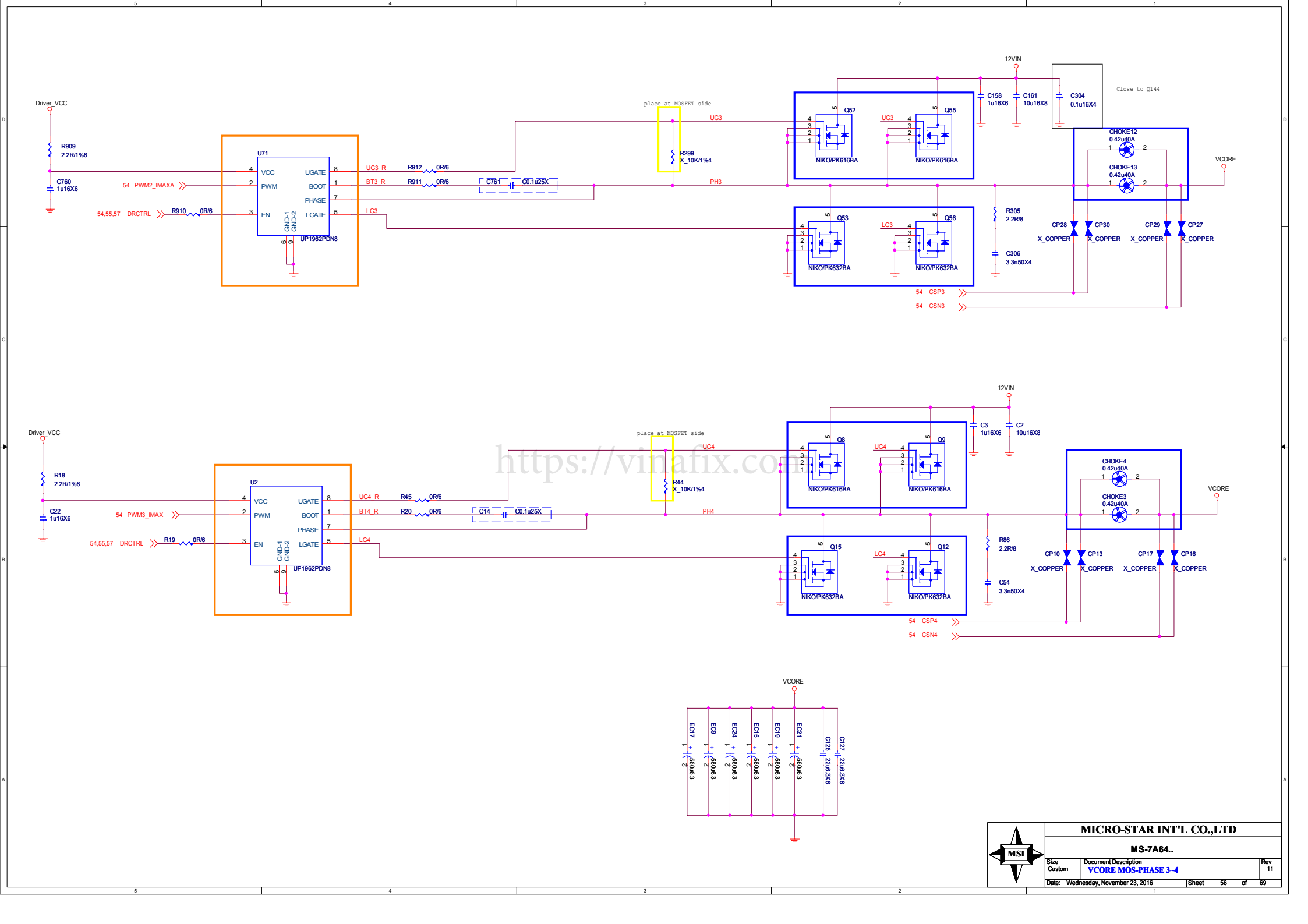

RT2 放在CHOKE5與CHOKE6中間

RT1放置在VccGT 這組switching power 最熱的地方

NTCA_Lb RT2 NTCA_La

10KRT1%/4

NTCA1a RT1

100KRT1%4

12VIN

C5 1u16X6 C4 1u16X6

place at MOSFET side

UG1A_R R106 0R/6 UG1A

R46 X_10K/1%4

Q10 NIKO/PK616BA

BT1A_R R107 0R/6 C71 C0.1u25X PH1A

CHOKE5 0.22u60A

VGT

LG1A Q13 NIKO/PK632BA Q16 NIKO/PK632BA

R87 2.2R/8 C55 3.3n50X4

CP12 X_COPPER CP15 X_COPPER

ISP1 R104 X_0R/4

ISP2 R118 0R/4 ISEN1A-1

54 CSP1A-1 R103 5.6K/1%4 CSP1A-1

C70 1000p50X4 CSN1A-1

54 CSN1A-1

12VIN

C7 10u16X8 C6 10u16X8

place at MOSFET side

UG2A_R R153 0R/6 UG2A

R47 X_10K/1%4

Q11 NIKO/PK616BA

BT2A_R R152 0R/6 C89 C0.1u25X PH2A

CHOKE6 0.22u60A

VGT

LG2A Q14 NIKO/PK632BA Q17 NIKO/PK632BA

R88 2.2R/8 C56 3.3n50X4

CP11 X_COPPER CP14 X_COPPER

ISP1 R119 0R/4

ISP2 R132 X_0R/4 ISEN1A-2

54 CSP1A-2 R117 5.6K/1%4 CSP1A-2

C81 1000p50X4 CSN1A-2

54 CSN1A-2

D9 S-BAT54A_SOT23 Y BT1A_R Z X BT2A_R

Driver_VCC

R151 2.2R/1%6

C88 1u16X6

U6 uP1961S

3	VCC	BOOT1	14
16	ISP1	UG1	13
1	ISP2	PH1	12
2	PWM0	LG1	11
15	EN	BOOT2	7
4	ISP0	UG2	8
6	NC	PH2	9
5	GND	LG2	10
17	GND		

54 PWM1A

54,55,56 DRCTRL R105 0R/6

54 CSP1A CSP1A

BT1A_R BT1A_R UG1A_R UG1A_R PH1A PH1A LG1A LG1A BT2A_R BT2A_R UG2A_R UG2A_R PH2A PH2A LG2A LG2A

0909 Modify OI3-7A16003 to I33-1961S0C-U33

EC5 EC7 EC10 EC11 EC8 560u6.3

VGT

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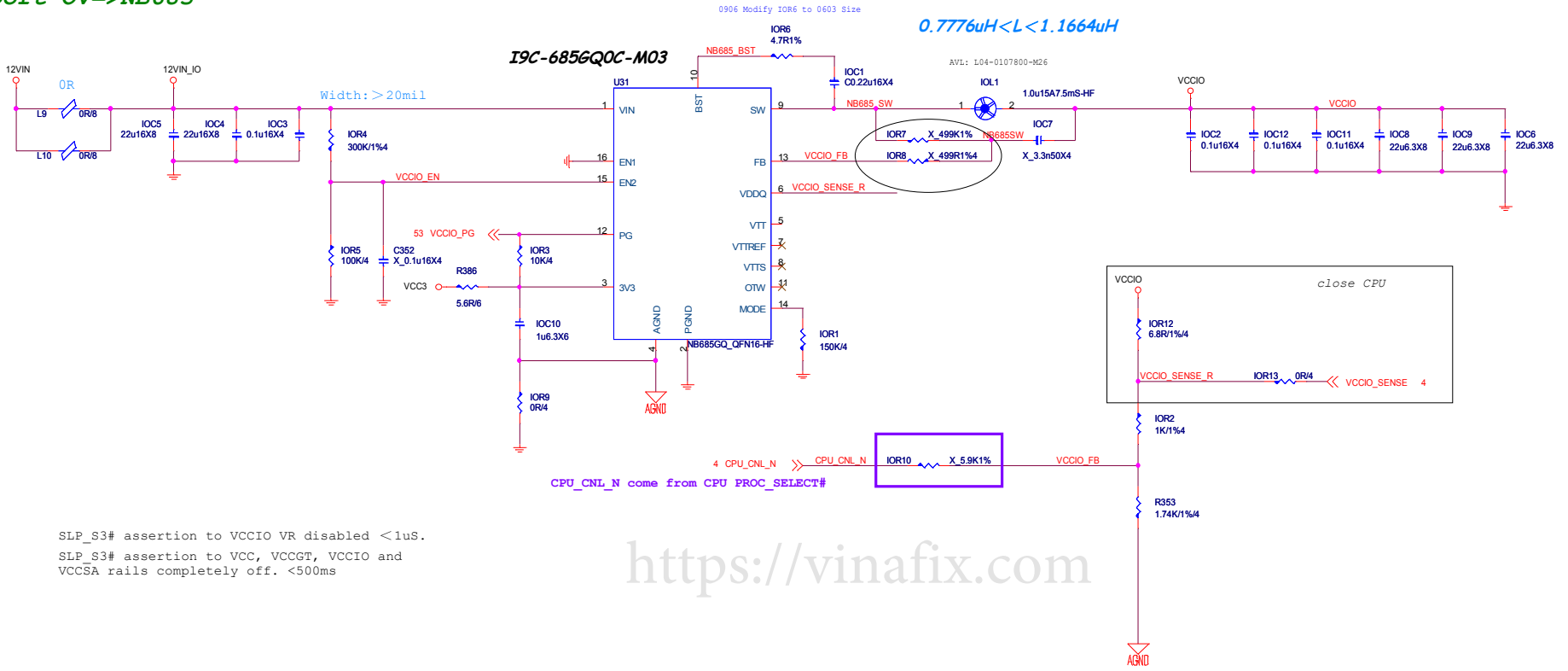
VCCIO

0.95V; 5.5A

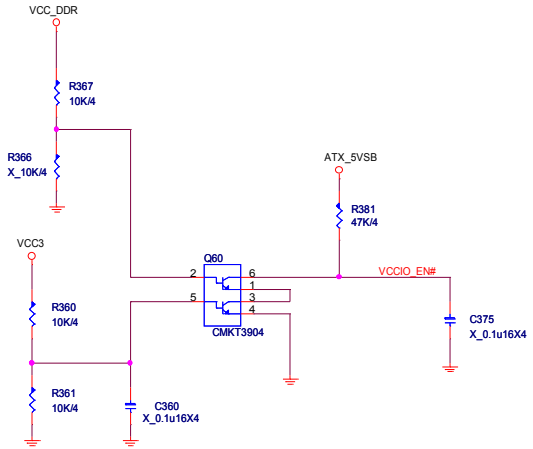
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

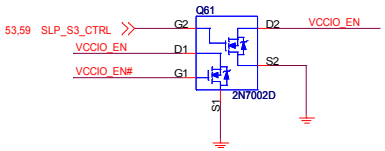
support OV=>NB685



SLP_S3# assertion to VCCIO VR disabled <1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms





SLP_S3# assertion to VR disabled max:1us

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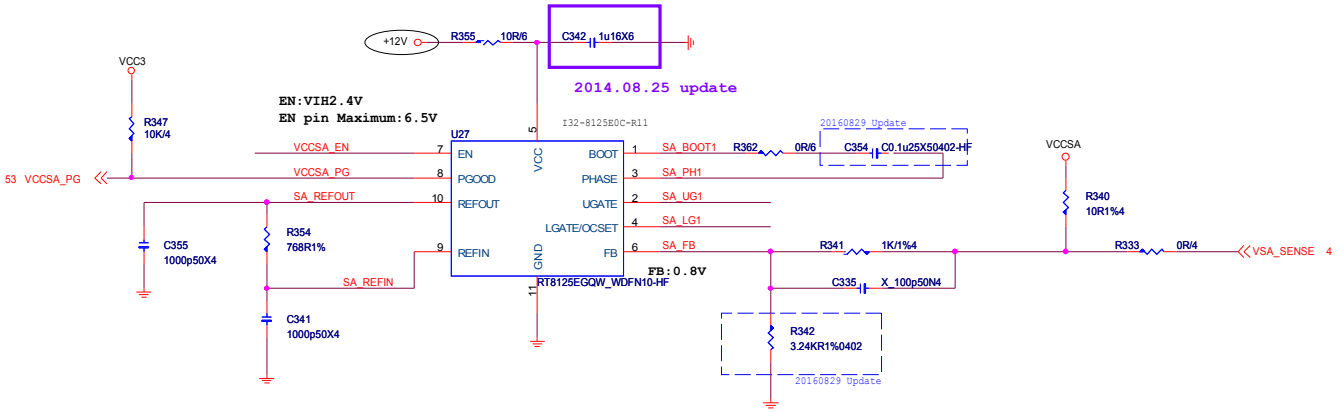
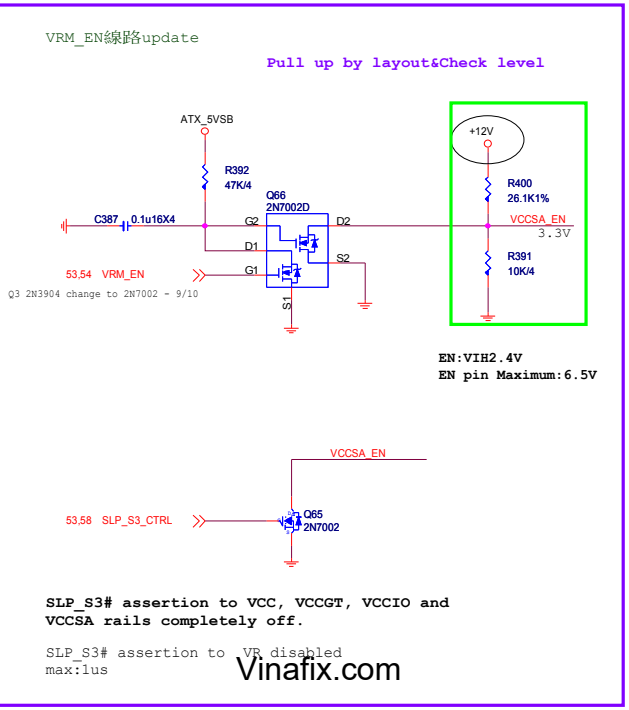
SA Power:1.05V,11.1A

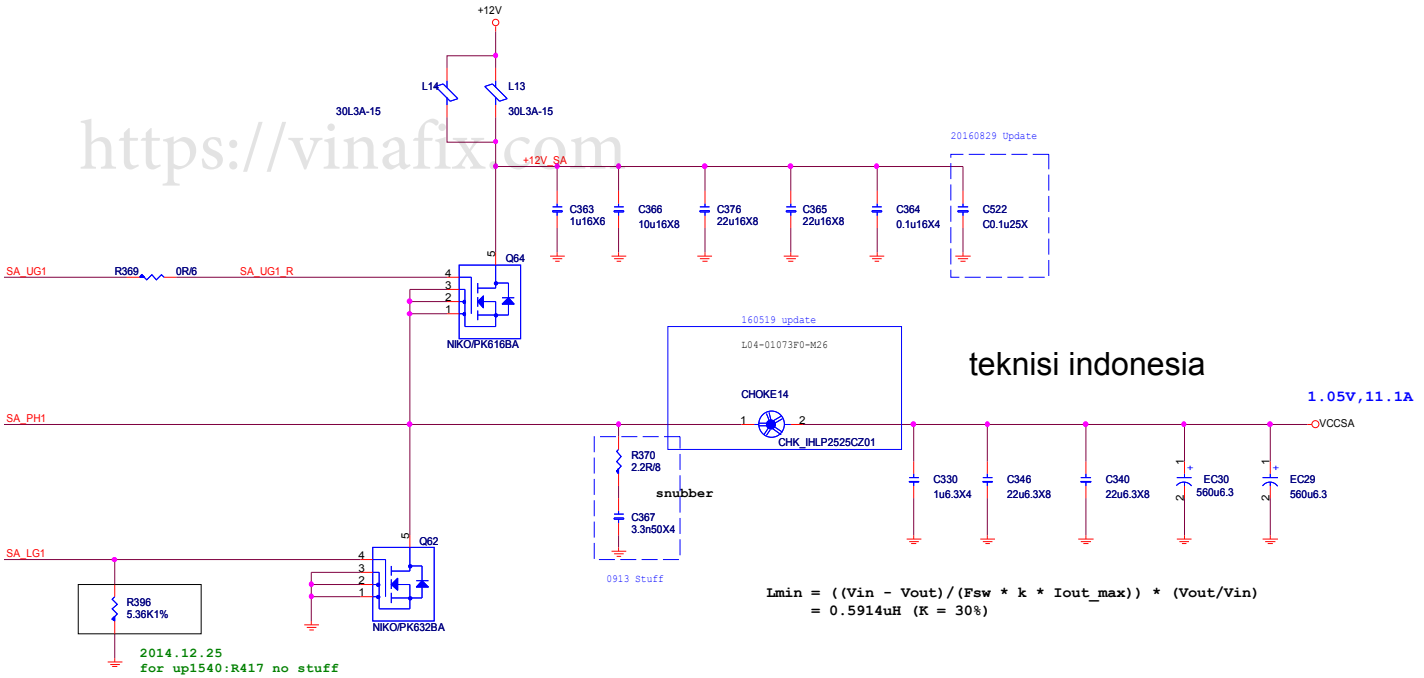
*OCP =11.1A*1.4=15.54A*
*Rocs(R417)=OCP*Rdson(Low side)3.4mohm]/10uA*
=15.54(3.4)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm







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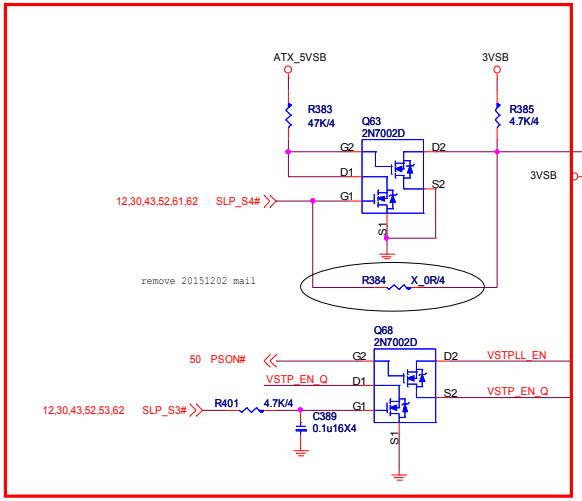
VCCST

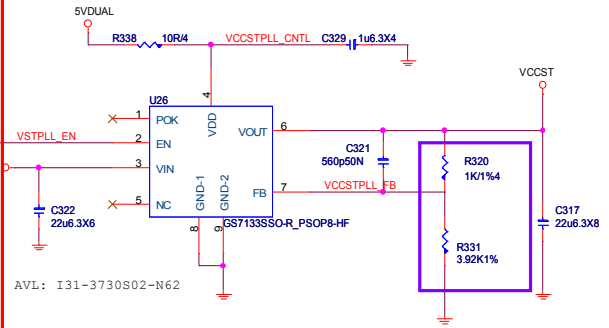
for Gaming3/5, Classic, ECO and H110

VCCST:60mA
VCCPLL:150mA

1.0V; 210mA

For Cost down VCCST&VCCPLL merge





AVL: I31-3730S02-N62

NO OV,R26->25.5K,R27->100K, C178 unstuff

VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

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DDR4_1.2V 2.5A+9.5A+1.2A=13.5A

2.8A FOR CPU

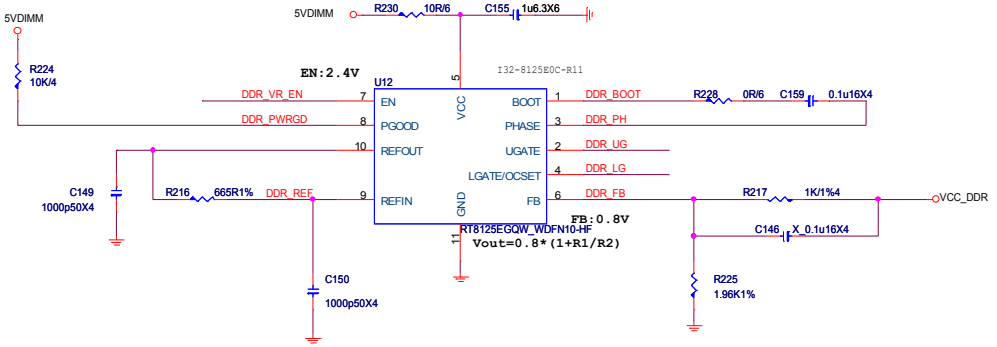
9.5A FOR 4DIMM

1.2A FOR DDR VTT

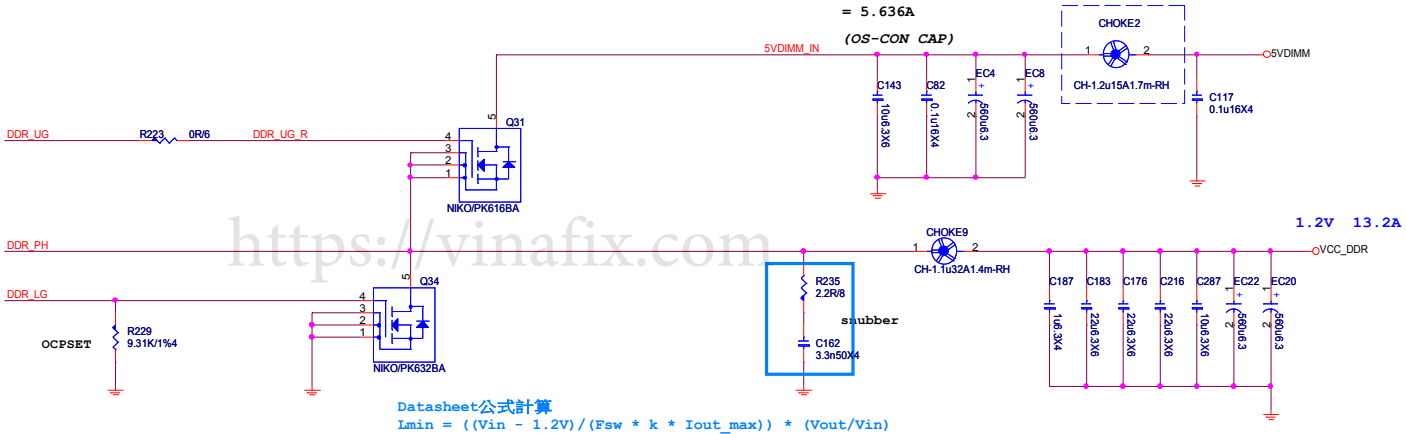
OCP =13.2A*1.5=20.25A
Rocs(R95)=OCP*Rdson[(Low side)]/10uA
=20.25A*(4.6)mohm/10uA
=9.315Kohm

Rocpset:5.1K
OCP=Rocset*Rdson[(Low side)]/10uA
=9.31K*(4.6)mohm/10uA
=20.23A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-4C05N03-005 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm



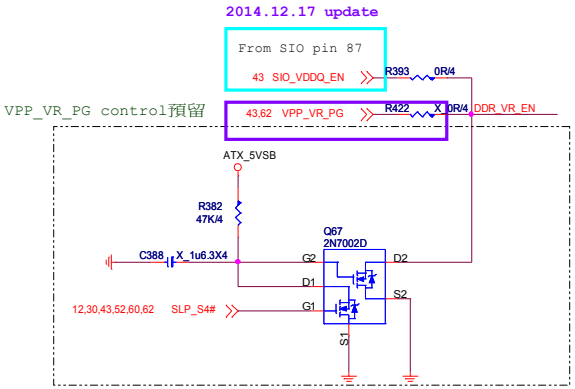
Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A



Datasheet公式計算
Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH＜L＜1.2897uH

2014.12.17 update



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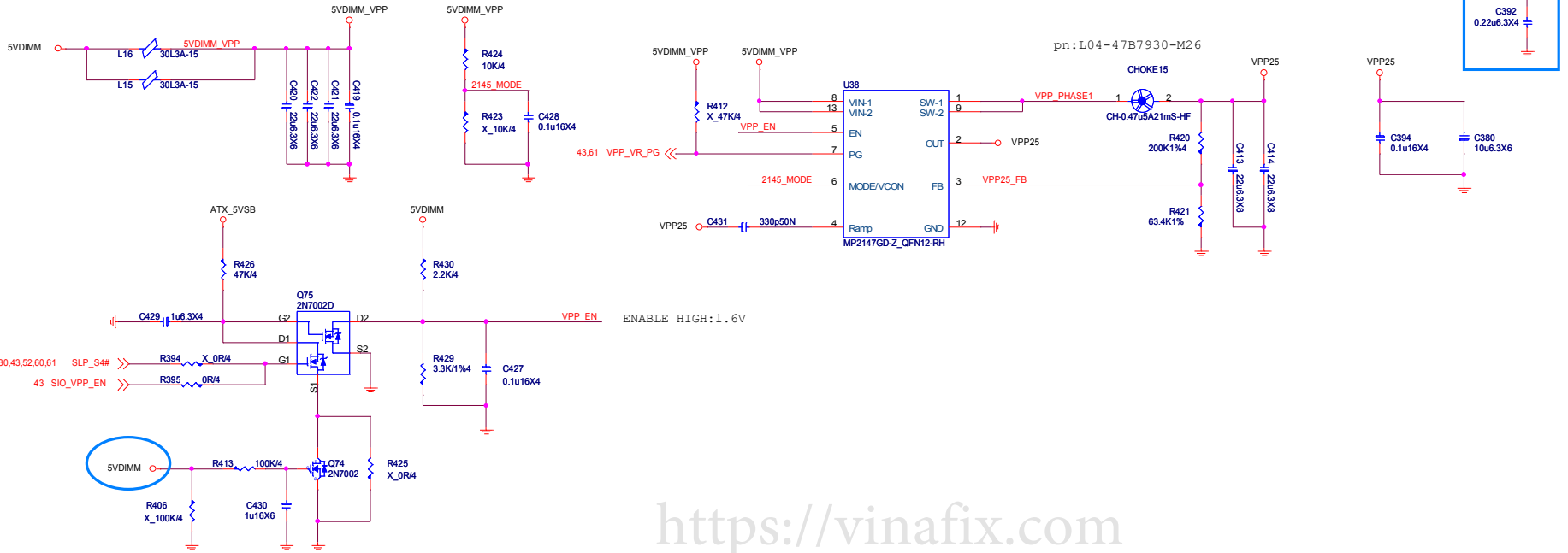
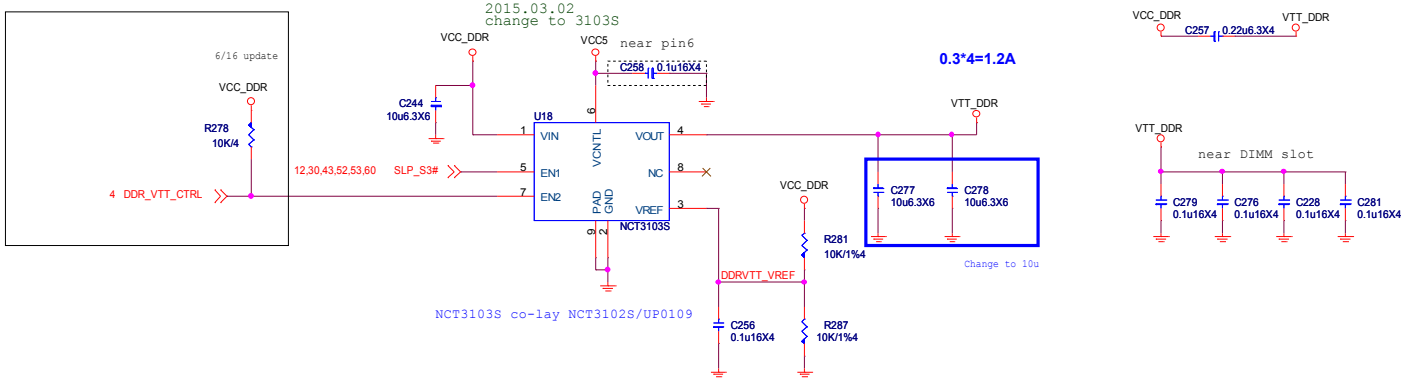
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power

2.5V; 2.24A



DDR VTT Power



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PCH_1VSB

1.0V; 11.83A

OCP = 17.745A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 11.83 * 4.6mohm / 10uA
= 8.16K

Rocs:7.87K,OCP:
D03-4C05N03-O05 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

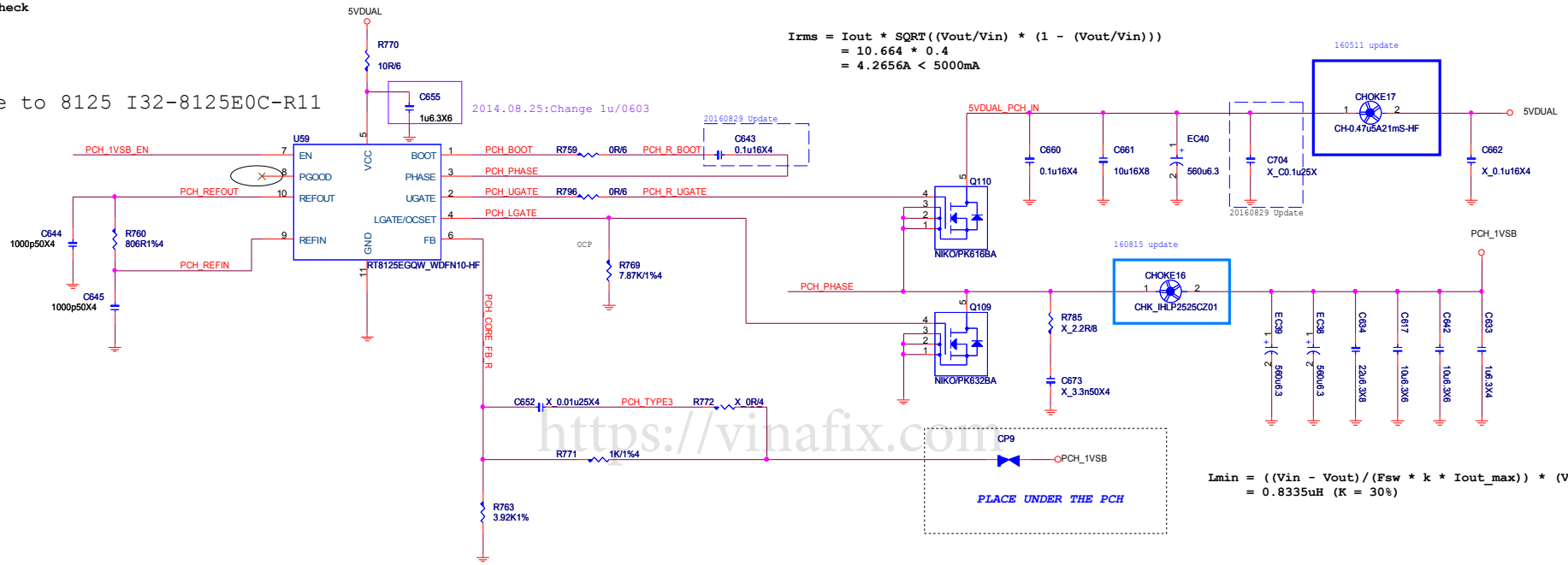
1504 change to 8125 I32-8125E0C-R11

2014.08.25:Change 1u/0603

160511 update

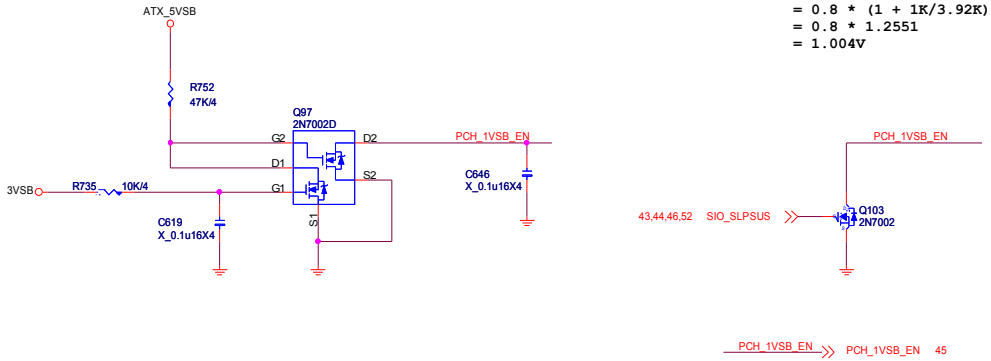
160815 update

20160829 Update



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V



Vinafix.com

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PCB

PCB1

7A64_11

PD0-07A6411-G37

PD0-07A6411-E48

MK_LABLE1 — MARKET LABLE — MK_LABLE1

AMI_LABLE — AMI_BIOS LABLE — BIOS_LABLE

HDMI_LABLE — HDMI LABLE — HDMI LABEL

CFOS_LABLE — CFOS LABLE — CFOS_LABLE

NAHIMIC_LABLE — NAHIMIC LABLE — NAHIMIC_LABLE

SSE_LABLE — SSE LABLE — SSE_LABLE

USB31 — USB3.1 LABLE — USB31_LABLE

XSPLIT_LABEL — XSPLIT LABLE — XSPLIT_LABEL

Audio Small Cover

COVER1 — Audio Cover — E21-7A62010-RH

1118 Cover1 change to E21-7A62010-A91

CPU_H1 — CPU 鐵座 — CPU_H1

BAT1_X1 — BAT-BCR2032P-RH

M2_2 SCREW — SCREW2 — SCREW

M2_1 SCREW — SCREW1 — SCREW

Mounting Holes

MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9 — X_MH001

C691 0.1u16X4

C714 0.1u16X4

1118 HS_MOS2 change to E31-0504410-K08

HS_MOS2 — MEC1 MEC2 — HS-0504410-HF

1118 PCH_HS change to E31-0408710-K08

PCH_HS — MEC1 MEC2 — HS-0408710-HF

Option BOM

Page 12~17

OPCH1 — PCH — X_B250

1011 Update to PCH MP PN

Page 33,36

OUH1 — HDMI — X_HDMI

MKLABLE2 — MARKET LABLE — X_MKLABLE_B250

Simulation

VCC5

SIM1 — X_PIN1*2

SIM2 — X_PIN1*2

Test point

VCORE — VCORE1

VGT — VGT1

VCC_DDR — VCC_DDR1

VCCSA — VCCSA1

VCCIO — VCCIO1

PCH_1VSB — PCH_1VSB1

VCCST — VCCST1

VTT_DDR — VTT_DDR1

VPP25 — VPP1

Optical Fiducial Marks-120

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8 — X_FM

EMI CAP

VCC3 — C781 X_0.1u16X4

VCC5 — C772 X_0.1u16X4

VCC5 — C773 X_0.1u16X4

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