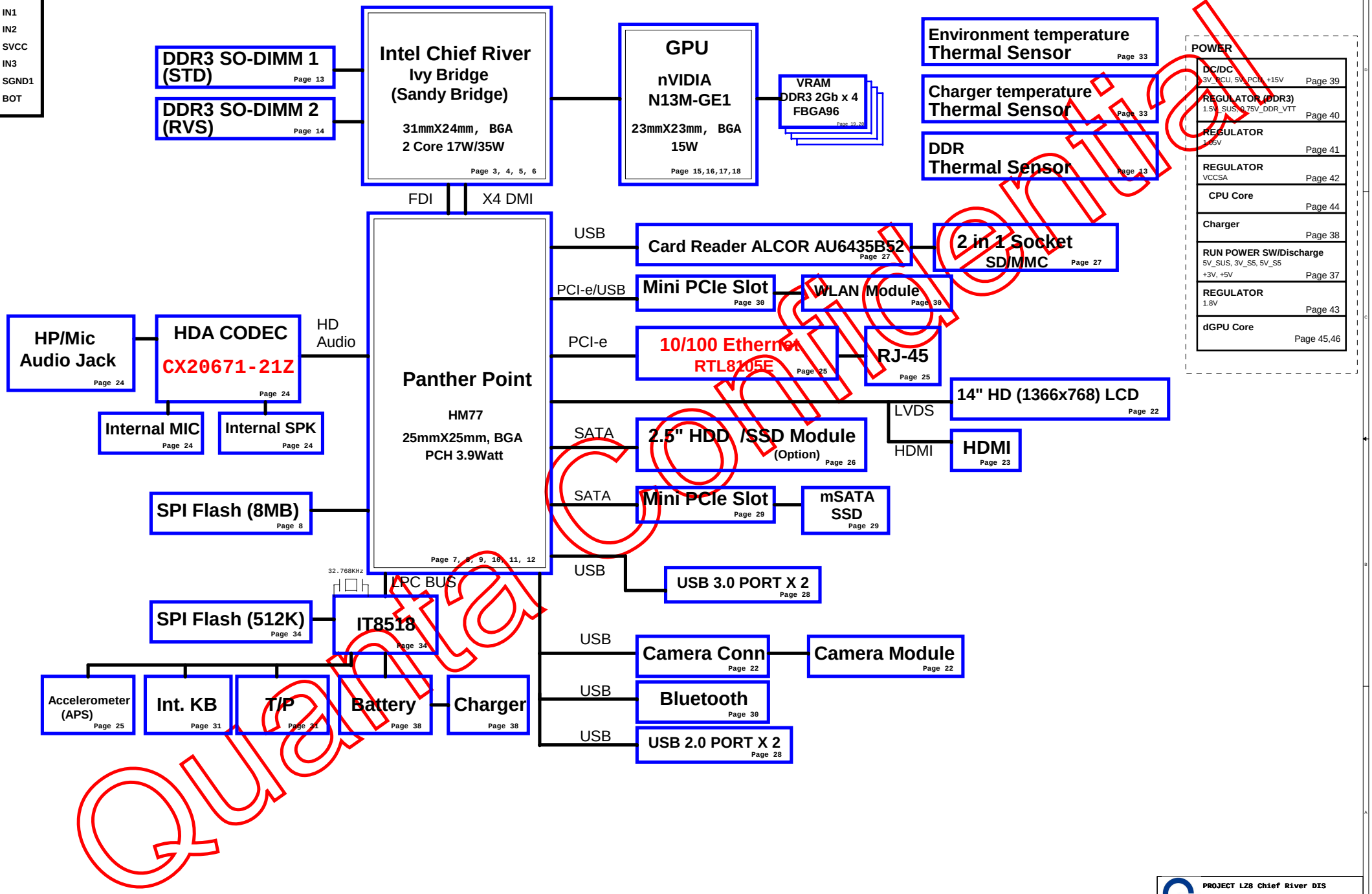
PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

LZ8 14" Block Diagram -- Intel Chief River ULV



PROJECT LZ8 Chief River DIS
Quanta Computer Inc.
Size | Document Number: System Block Diagram | Rev 1A
Date: Wednesday, December 21, 2011 | Sheet 1 of 49

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21	PS8622 LVDS converter
22	LCD/CAMERA
23	HDMI CONN
24	Audio Codec CX20672
25	LAN[RTL8105E]
26	SATA
27	Card Reader-AU6435B52-GDL
28	USB2.0 X2/USB3.0 X2
29	MINI Card (SSD)
30	WLAN/BT
31	KB/TP/LID
32	USB2.0--Audio Jack conn
33	FAN/Thermal
34	KBC IT8518
35	SW/LED
36	Screw Hole/EMI/ESD
37	Discharge
38	CHARGER (bq24725A)
39	3V/5V (TPS51123ARGER)
40	DDR3/0.75V (TPS51216)
41	1.05V_PCH(RT8240B)
42	VCCSA (RT8241A)
43	1.8V(TPS54318)
44	CPU(ISL95831)IMVP2+1
45	DGPU CORE(TPS51728)
46	GPU
47	
48	
49	
50	
51	

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	22,36,38,39,40,41,42,44,45	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,34	RTC		S0~S5
3VPCU	+3.3V	7,8,22,23,25,30,31,34,35,36,37,38,39,43,45	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	22,36,37,39,40,41,42,43,44,45,46	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
15V	+15V	22,37,39,40,46	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	25,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,24,28,32,37	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,30,35,37,45	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
1.5V_SUS	+1.5V	3,11,13,14,36,37,40,46	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,37,40	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,22,23,24,26,31,33,36,37,38	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,21,22,23,24,25,26,27 29,30,31,33,34,35,36,37,38,39 40,41,42,43,44,45,46	SLP_S3# CTRLD POWER	MAINON	S0
VCC_GFX		5,36,44	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5,37,42	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,37,43	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,21,36,37,41,46	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
VCC_CORE		5,6,36,44	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	22	LCD Power	ENVDD	S0
+3V_HDD	+3V	26	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	26	HDD Power	MAINON#	S0
BAT+V	+10V~+17V	38	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,36	DDR3 1.5V Rails	PS_S3CNTRL	S0

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

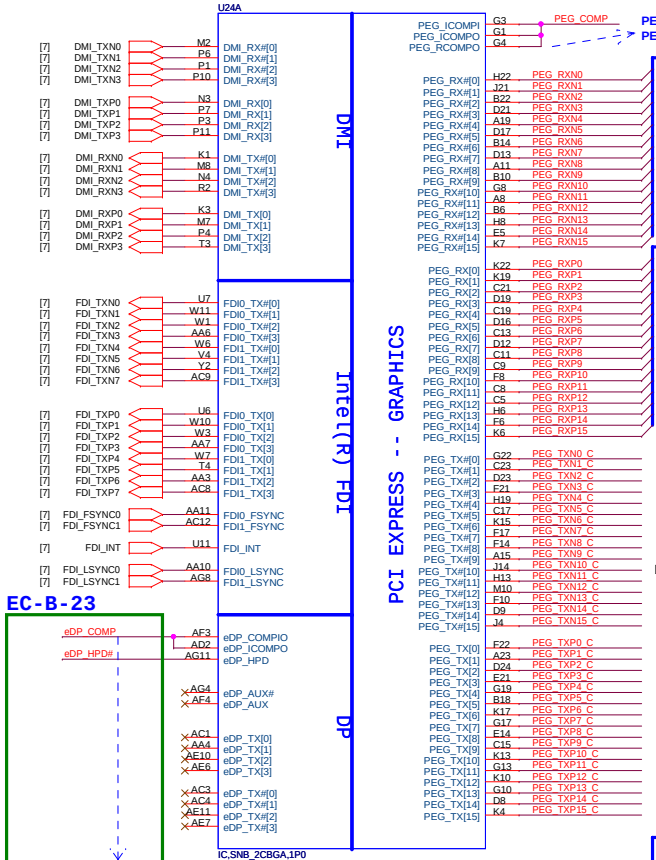
Size	Document Number	Rev
	System Block Diagram	1A

Date: Friday, November 11, 2011 Sheet 2 of 49

Ivy/Sandy Bridge Processor (DMI,PEG,FDI)

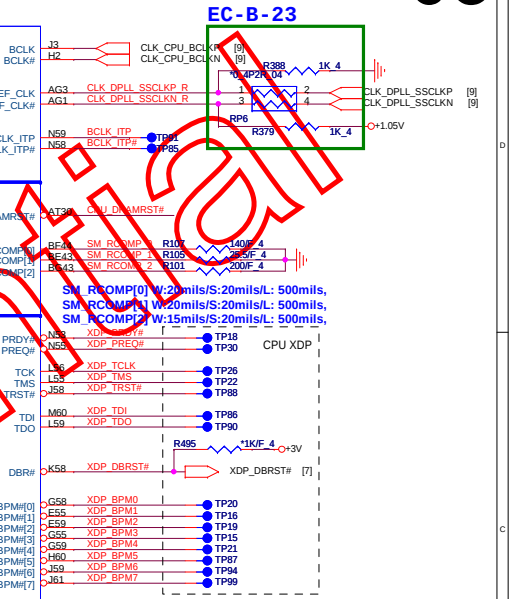
Ivy/Sandy Bridge Processor (CLK,MISC,JTAG)

03



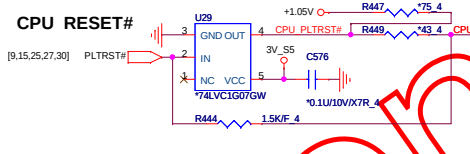
PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

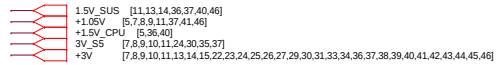
SNB_IVB# N.A at SNB EDS #27637 0.7v1

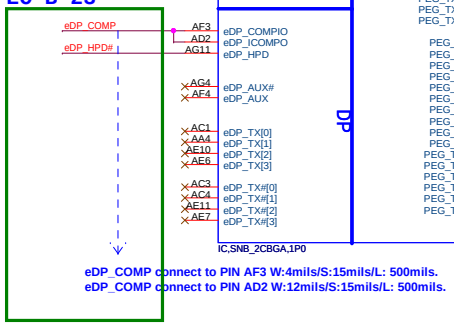


SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU RESET#

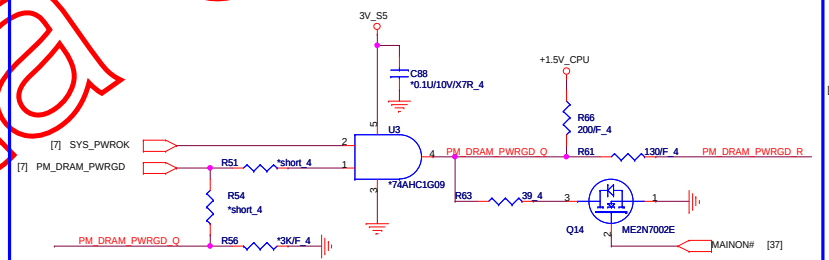




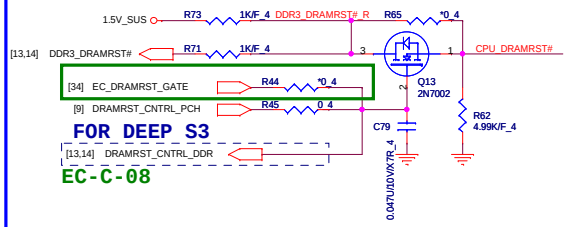


eDP_COMP connect to PIN AF3 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN AD2 W:12mils/S:15mils/L: 500mils.

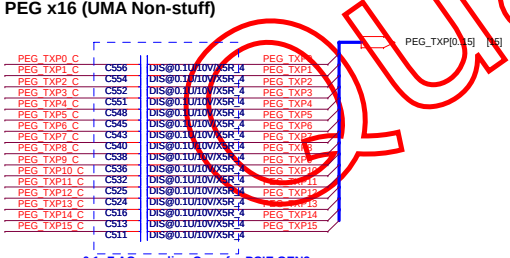
SM_DRAMPWROK Processor Input.



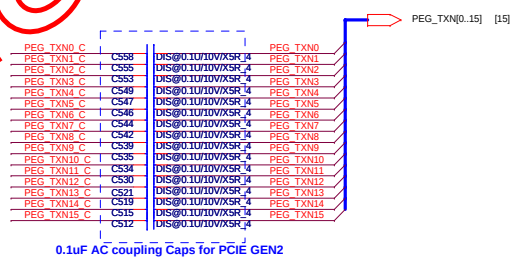
DDR3 DRAM RESET



PEG x16 (UMA Non-stuff)

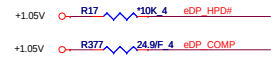


0.1uF AC coupling Caps for PCIE GEN2

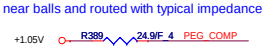


0.1uF AC coupling Caps for PCIE GEN2

DP & PEG Compensation

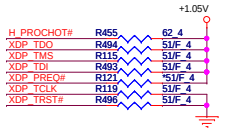


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



PROJECT	LZ8 Chief River DIS
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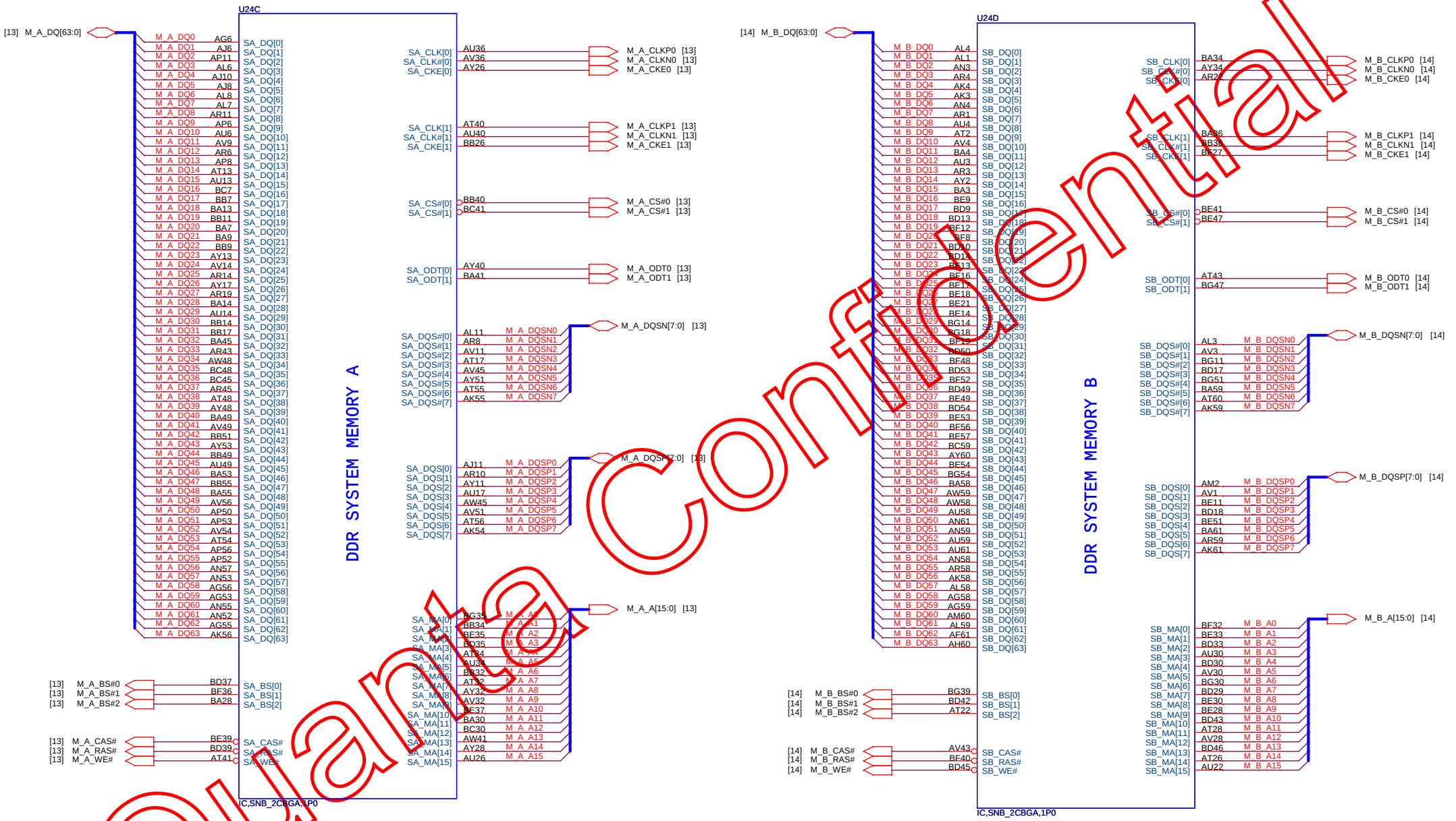
Ivy/Sandy Bridge Processor (DDR3)



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	Custom IVY 2/4 (DDR3 I/F)	1A
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Ivy/Sandy Bridge Processor (POWER)

330uF locate power side

CPU Core Power

IVY:33A

VCC_CORE

U24F

8.5A

+1.05V

C485 *330U/2V/ESR9_7343

POWER

CORE SUPPLY

PEG AND DDR

QUIET RAILS

SVID

SENSE LINES

3.3V_SUS?(PDDG p127)

SNB->NC
IVB->GND

1.2A

+1.8V

SNB:6A

EC-B-19

IC,SNB_2CBGA,1P0

Ivy/Sandy Bridge Processor (GRAPHIC POWER)

05

VCC_GFX

33A

U24G

GRAPHICS POWER

DDR3 - 1.5V RAILS

5A

+1.5V_CPU

+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SM_VREF

SMDDR_VREF [13,14,40]

MAINON_1.5V [37]

SENSE LINES 1.8V RAIL

QUIET RAILS

SA RAIL

SENSE LINES

SNB_IVB# N.A at SNB EDS #27637 0.7v1

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

SVID CLK

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

SVID DATA

Place PU resistor close to CPU

Place PU resistor close to VR

SVID ALERT

Place PU resistor close to CPU

VCC_CORE [6,36,44]
VCC_GFX [36,44]
VCCSA [37,42]
+1.05V [3,7,8,9,11,37,41,46]
+1.5V_CPU [3,36,40]
+1.8V [8,11,37,43]
SMDDR_VREF [13,14,40]

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	SNB 3/4 (POWER)	1A

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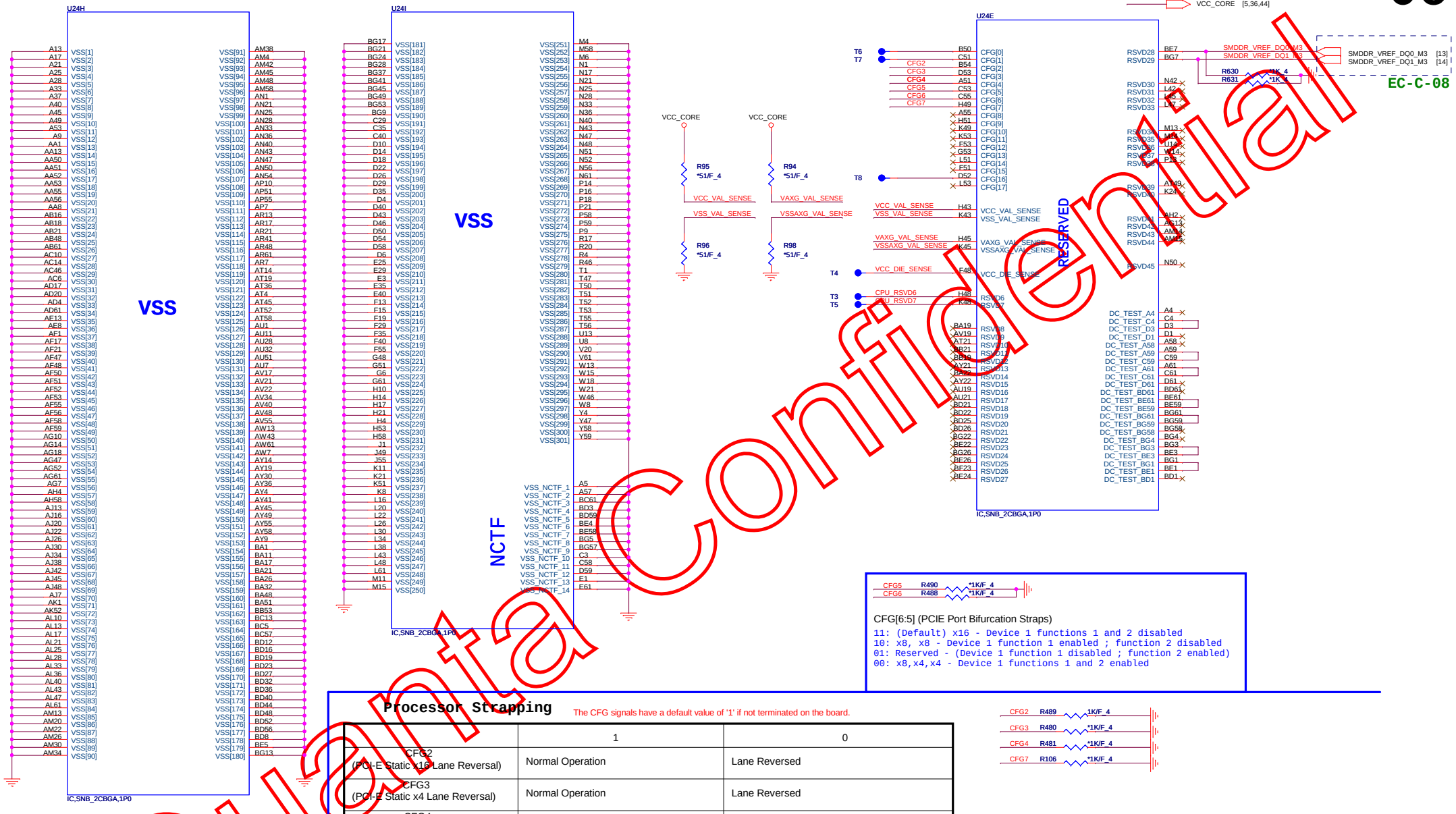
Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)

06



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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	Custom SNB 4/4 (GND)	3A

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Panther/Cougar Point (DMI,FDI,PM)

U32C

DMI0RXN DMI1RXN DMI2RXN DMI3RXN
DMI0RXP DMI1RXP DMI2RXP DMI3RXP
DMI0TXN DMI1TXN DMI2TXN DMI3TXN
DMI0TXP DMI1TXP DMI2TXP DMI3TXP
DMI_ZCOMPI
DMI_IRCOMP
DMI2RBIAS

DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3
DMI_COMP
DMI_RBIAS

FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

FDI_TXN0 FDI_TXN1 FDI_TXN2 FDI_TXN3 FDI_TXN4 FDI_TXN5 FDI_TXN6 FDI_TXN7
FDI_TXP0 FDI_TXP1 FDI_TXP2 FDI_TXP3 FDI_TXP4 FDI_TXP5 FDI_TXP6 FDI_TXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

DMI
FDI

+1.05V R470 49.9/F_4 DMI_COMP
R114 750/F_4 DMI_RBIAS

FOR DEEP S3

[34] SUSACK# R607 *0_4
SUSWARN#_R R575 0_4 SUSACK#_R
EC-B-01

[3] XDP_DBRST#
SYS_PWROK R257 *short_4 R258 *0_4 SYS_PWROK_R
[34] ECPWROK R239 *short_4 EC_PWROK_R
EC_PWROK_R R228 *short_4 APWROK_R
[3] PM_DRAM_PWRGD
[34] ICH_RSMRST#
EC-B-01
[34] SUSWARN# R589 *short_4 SUSWARN#_R
FOR DEEP S3
[34] DNBSWON# R269 *short_4 DNBSWON#_R
[18,34] AC_PRESENT R268 *short_4 AC_PRESENT_R
PM_BATLOW#
PM_RI#

SUSACK# SYS_RESET# SYS_PWROK PWROK APWROK DRAMPWROK RSMRST# SUSWARN#/SUSPWRDNACK/GPIO30 PWRBTN# ACPRESENT / GPIO31 BATLOW# / GPIO72 RI#

(+3VS5) (DSW) (+3VS5)

System Power Management

DSWVRMEN DPWROK WAKE# CLKRUN# / GPIO32 SUS_STAT# / GPIO61 SUSCLK / GPIO62 SLP_S5# / GPIO63 SLP_S4# SLP_S3# SLP_A# SLP_SUS# PMSYNCH SLP_LAN# / GPIO29

(+3V) (+3VS5) (+3VS5) (DSW) (+3VS5)

EC-B-02
R220 0_4 RSMRST#
R210 *short_4 DPWROK
FOR DEEP S3

PCIE_WAKE# [25,30,34]
PCI_CLKRUN# [34]
LPC_PD# TP113
PCH_SUSCLK_L TP56
SLP_S5 TP55
R247 *short_4 PM_SLP_S4# [34]
R555 *short_4 SIO_SLP_S3# [34]
TP53
FOR DEEP S5
SLP_SUS# [11,34]
PM_SYNC [3]
WLAN_AOAC_ON [30]

EC-B-01
R169 1K/F_4 DAC_IREF
RSMRST#
RV9 *TVM0G180M030R(18V,3p)_4

CougarPoint_R1P0

Panther/Cougar Point (LVDS,DDI)

EC-B-23

[22] INT_LVDS_BLON
[22] INT_DISP_ON
[22] INT_DPST_PWM
[22] LVDS_DDC_SCL
[22] LVDS_DDC_SDA
+3V R168 2.2K_4 L_CTRL_CLK R159 2.2K_4 L_CTRL_DATA
R510 2.37K/F_4 LVDS_IBG LVDS_VBG TP39

[22] INT_TXLCLKN [22] INT_TXLCLKP
[22] INT_TXLOUTN0 [22] INT_TXLOUTN1 [22] INT_TXLOUTN2
[22] INT_TXLOUTP0 [22] INT_TXLOUTP1 [22] INT_TXLOUTP2

U32D

L_BKLTEN L_VDD_EN L_BKLTCTL L_DDC_CLK L_DDC_DATA L_CTRL_CLK L_CTRL_DATA LVD_IBG LVD_VBG LVD_VREFH LVD_VREFL
LVDSA_CLK# LVDSA_CLK LVDSA_DATA#0 LVDSA_DATA#1 LVDSA_DATA#2 LVDSA_DATA#3 LVDSA_DATA0 LVDSA_DATA1 LVDSA_DATA2 LVDSA_DATA3
LVDSB_CLK# LVDSB_CLK LVDSB_DATA#0 LVDSB_DATA#1 LVDSB_DATA#2 LVDSB_DATA#3 LVDSB_DATA0 LVDSB_DATA1 LVDSB_DATA2 LVDSB_DATA3

LVDS

CRT_BLUE CRT_GREEN CRT_RED CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_VSYNC DAC_IREF CRT_IRTN

CRT

Digital Display Interface

SDVO_TVCLKINN SDVO_TVCLKINP SDVO_STALLN SDVO_STALLP SDVO_INTN SDVO_INTP SDVO_CTRLCLK SDVO_CTRLDATA
DDPB_AUXN DDPB_AUXP DDPB_HPD DDPB_0N DDPB_0P DDPB_1N DDPB_1P DDPB_2N DDPB_2P DDPB_3N DDPB_3P
DDPC_CTRLCLK DDPC_CTRLDATA DDPC_AUXN DDPC_AUXP DDPC_HPD DDPC_0N DDPC_0P DDPC_1N DDPC_1P DDPC_2N DDPC_2P DDPC_3N DDPC_3P
DDPD_CTRLCLK DDPD_CTRLDATA DDPD_AUXN DDPD_AUXP DDPD_HPD DDPD_0N DDPD_0P DDPD_1N DDPD_1P DDPD_2N DDPD_2P DDPD_3N DDPD_3P

Layout note:
AC coupling capacitors of DP are placed on near connector

INT_HDMI_SCL [23]
INT_HDMI_SDA [23]
DPB_HPD_Q
DPB_LANE0_N C560 0.1U/10V/X7R_4 HDMI_TX2- [23]
DPB_LANE0_P C557 0.1U/10V/X7R_4 HDMI_TX2+ [23]
DPB_LANE1_N C566 0.1U/10V/X7R_4 HDMI_TX1- [23]
DPB_LANE1_P C563 0.1U/10V/X7R_4 HDMI_TX1+ [23]
DPB_LANE2_N C572 0.1U/10V/X7R_4 HDMI_TX0- [23]
DPB_LANE2_P C571 0.1U/10V/X7R_4 HDMI_TX0+ [23]
DPB_LANE3_N C575 0.1U/10V/X7R_4 HDMI_CLK- [23]
DPB_LANE3_P C573 0.1U/10V/X7R_4 HDMI_CLK+ [23]

INT. HDMI

TP35 TP36 TP83 TP33 TP32

CougarPoint_R1P0

+1.05V [3,5,8,9,11,37,41,46]
+3V_RTC [8,11,34]
3V_S5 [3,8,9,10,11,24,30,35,37]
+3V [3,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
+3V_DSW [8,11]

PCH Pull-high/low(CLG)

3V_S5
PM_RI# R576 10K_4
PM_BATLOW# R262 8.2K_4
PCIE_WAKE# R568 10K_4
WLAN_AOAC_ON R263 10K_4
SUSWARN#_R R588 10K_4
AC_PRESENT_R R267 10K_4
PM_DRAM_PWRGD R222 *200/F_4
+3V
XDP_DBRST# R545 10K_4
PCI_CLKRUN# R537 8.2K_4
RSMRST# R571 10K_4
SYS_PWROK R206 10K_4

System PWR_OK(CLG)

3V_S5
C414 0.1U/10V/X7R_4
[3] SYS_PWROK SYS_PWROK_4
DELAY_VR_PWRGOOD [44]
ECPWROK
U13 TC7SH08FU
R238 100K_4

3V_RTC R581 330K_4 DSWVREN R597 *330K_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

INT HDMI DETECT

EC-B-24
[23] HDMI_HPD
*short_4 R129 DPB_HPD_Q
R126 100K_4

LVDS for HM76

EC-B-23

DPWROK FOR DSW (DEEP S3)

3VPCU
+3V_DSW
3V_S5
D20 *RB500V-40
D21 *RB500V-40
R533 *10K_4
R541 *10K_4
DPWROK
C687 *0.1U/10V/X5R_4
add cap to timing tune
Q45 *PDTC144EU
Q46 *2N7002

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 1/6 (DMI/FDI/VIDEO)	2A

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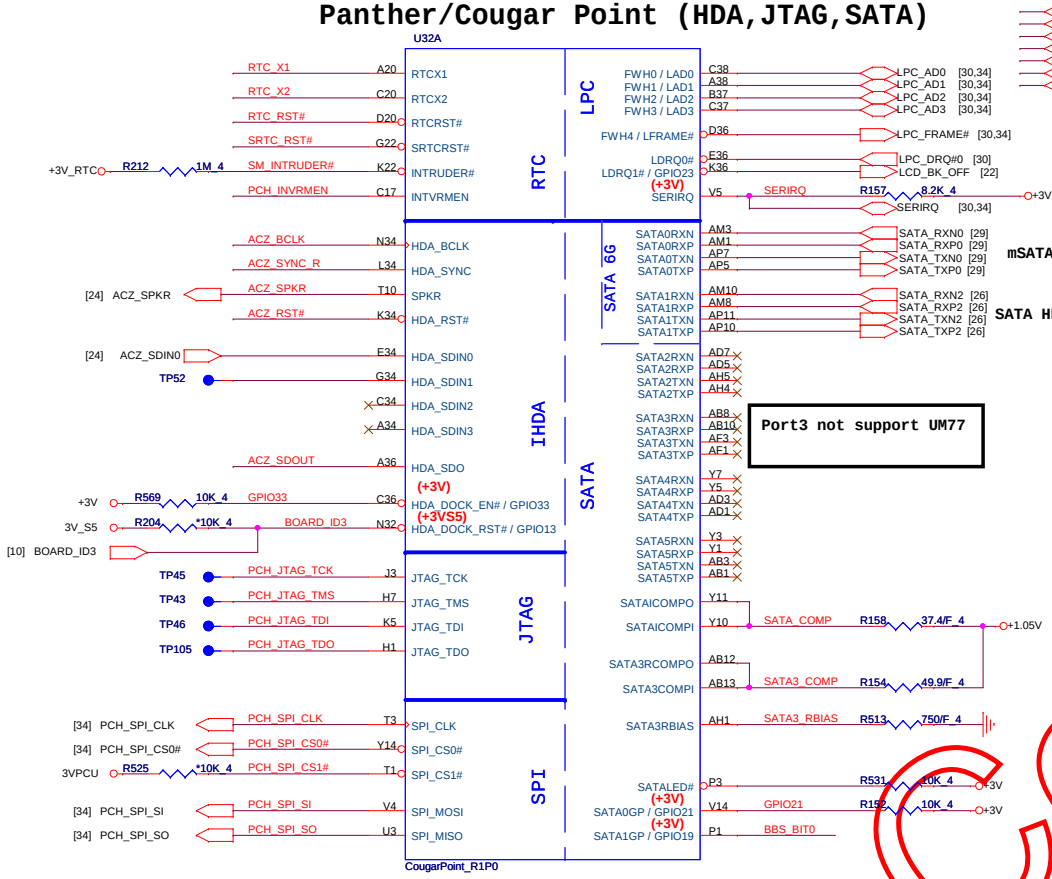
Panther/Cougar Point (HDA,JTAG,SATA)



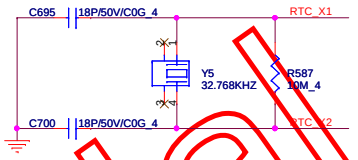
+1.05V [3,5,7,9,11,37,41,46]
+1.8V [5,11,37,43]
+3V_RTC [7,11,34]
3VPCU [7,22,25,30,31,34,35,36,37,38,39,43,45]
+3V [3,7,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
+5V [11,23,24,26,33,36,37,38]
+3V_DSW [7,11]

if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary

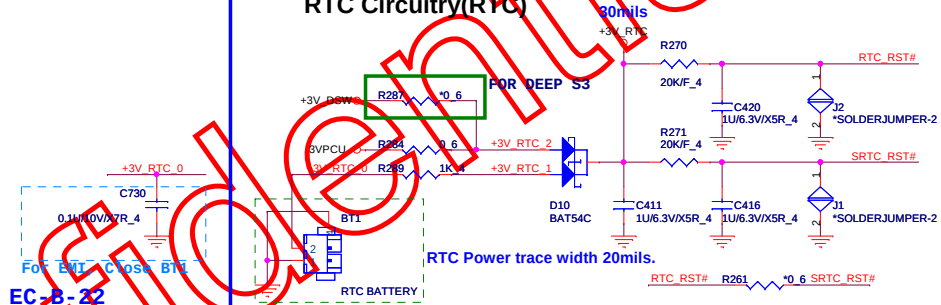
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR (Different from Calpella)	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R180 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R578 *1K_4 R561 *10K_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R564 330K_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R567 *1K_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] R530 *1K_4 BBS_BIT0 R592 *1K_4 BBS_BIT1 [9]
GPIO19 (Different from Calpella)	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm	R500 2.2K_4 +1.8V N.A at CPT EDS 0.7 [3] PROC_SELECT# R501 1K_4 DF_TVS [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R203 1K_4 ACZ_SYNC_R
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite		Low = Disable (Default) High = Enable	[10] HOST_ALERT#1_R HOST_ALERT#1_R R554 1K_4 3V_S5
GPIO28 (Different from Calpella)	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R195 *1K_4 PLL_ODVR_EN [10]
DSWVREN	0: disable 1: enable			

RTC Clock 32.768KHz



RTC Circuitry(RTC)



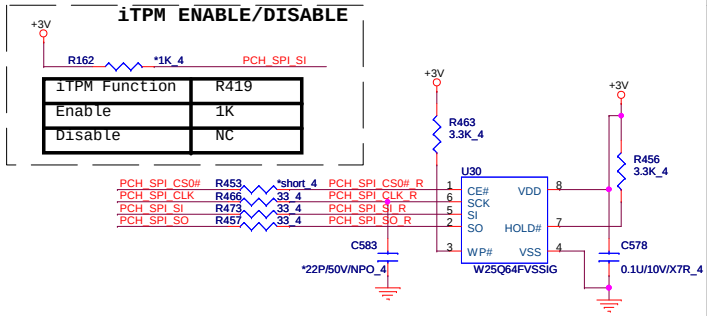
EC-B-22

EC-B- 25

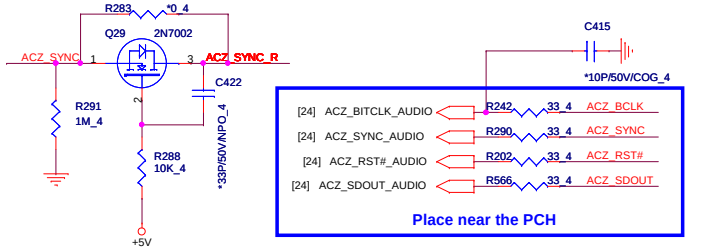
W25Q64CVSSIG: AKE3EFP0N04
MX25L6406EM2I-12G: AKE3NFP0Z00
EN25Q64-104HIP: AKE3EFN0Q00

PCH Dual SPL

64Mbit (8M Byte), SPI



HDA Bus(CLG)



PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 2/6 (SATA/HDA/SPI)	1A
Date: Tuesday, December 20, 2011	Sheet 8 of 49	

Panther/Cougar Point-M (PCI,USB,NVRAM)

Panther/Cougar Point-M (PCI-E,SMBUS,CLK)

09

PCI/USBOC# Pull-up(CLG)

+3V
PCI_PIRQA# R223 8.2K_4
PCI_PIRQB# R236 8.2K_4
PCI_PIRQC# R218 8.2K_4
PCI_PIRQD# R213 8.2K_4

+3V
RP1 10K_10P8R_6
10 MPC_PWR_CTRL#
9 PIRQF#
8 PIRQE#
7
6
PIRQH#
PWM_SELECT#
PIRQG#

3V_S5
RP12 10K_10P8R_6
10 USB_OC4#
9 USB_OC1#
8 USB_OC2#
7 USB_OC3#
6
1 USB_OC6#
2 USB_OC0#
3 USB_OC7#
4 USB_OC5#
5

USB3.0

[28] USB30_RX1- / [28] USB30_RX2-
[28] USB30_RX1+ / [28] USB30_RX2+
[28] USB30_TX1- / [28] USB30_TX2-
[28] USB30_TX1+ / [28] USB30_TX2+

U32E

RSVD

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20
TP21 TP22 TP23 TP24
TP25 USB30_RX1N
TP26 USB30_RX2N
TP27 USB30_RX3N
TP28 USB30_RX4N
TP29 USB30_RX1P
TP30 USB30_RX2P
TP31 USB30_RX3P
TP32 USB30_RX4P
TP33 USB30_TX1N
TP34 USB30_TX2N
TP35 USB30_TX3N
TP36 USB30_TX4N
TP37 USB30_TX1P
TP38 USB30_TX2P
TP39 USB30_TX3P
TP40 USB30_TX4P

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD18 RSVD19 RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27 RSVD28 RSVD29

TP34

USB

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P

USBP0- [28] USB 3.0
USBP0+ [28] USB 3.0 (BIOS debug)
USBP1- [28] CCD
USBP1+ [28] WLAN/BT
USBP2- [22]
USBP2+ [22]
USBP3- [30]
USBP3+ [30]

USB2.0/USB3.0 COMBO
USB2.0/USB3.0 COMBO
EHCI1
WLAN

USB ports 6 and 7 are disabled on 12 port SKUs(UM77).

USBP8- [32]
USBP8+ [32]
USBP9- [32]
USBP9+ [32]
USBP10- [27]
USBP10+ [27]

USB 2.0(common design for 14")
USB 2.0 (DB/MOS debug)
Card Reader
EHCI2

USB ports 12 and 13 are disabled on 10 port SKUs(UM77).

USBRBIAS#
USBRBIAS
USB_BIAS
R570 22.6/F_4

OC0# / GPIO59 (+3VS5) USB_OC0# [28] OC0# For USB3.0
OC1# / GPIO40 (+3VS5)
OC2# / GPIO41 (+3VS5)
OC3# / GPIO42 (+3VS5)
OC4# / GPIO43 (+3VS5) USB_OC4# [32] OC4# For USB2.0
OC5# / GPIO9 (+3VS5)
OC6# / GPIO10 (+3VS5)
OC7# / GPIO14 (+3VS5)

CougarPoint_R1P0

PCI

PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD#
PIRQA# PIRQB# PIRQC# PIRQD#

[15] DGPU_HOLD_RST#
DGPU_HOLD_RST# REQ2# DGPU_PWR_EN
REQ1# / GPIO50 (+3V)
REQ2# / GPIO52 (+3V)
REQ3# / GPIO54 (+3V)

[8] BBS_BIT1
TP50
[8] PCI_GNT3#
PWM_SELECT# PCI_GNT3#
GNT1# / GPIO51 (+3V)
GNT2# / GPIO53 (+3V)
GNT3# / GPIO55 (+3V)

MPC_PWR_CTRL# PIRQF# PIRQG# PIRQH#
PIRQE# / GPIO2 (+3V)
PIRQF# / GPIO3 (+3V)
PIRQG# / GPIO4 (+3V)
PIRQH# / GPIO5 (+3V)

TP114
PME#
PCI_PLTRST#
PLTRST#

[34] CLK_PCI_8512
[30] PCLK_DEBUG
R559 22_4 CLK_PCI_8512_R
R189 22_4 PCLK_DEBUG_R
CLK_PCI_FB R553 22_4 CLK_PCI_FB_R
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

C691 *15P/50V/NPO_4 CLK_PCI_8512
C400 *10P/50V/COG_4 PCLK_DEBUG

CougarPoint_R1P0

LAN

[25] PCIE_RXN2 PCIE_RXP2 PCIE_TXN2 PCIE_TXP2
C309 0.1U/10V/X7R_4 PCIE_TXN2_C
C310 0.1U/10V/X7R_4 PCIE_TXP2_C

WLAN

[30] PCIE_RXN3_LAN PCIE_RXP3_LAN PCIE_TXN3_LAN PCIE_TXP3_LAN
C321 0.1U/10V/X7R_4 PCIE_TXN3_LAN_C
C325 0.1U/10V/X7R_4 PCIE_TXP3_LAN_C

Port4-Port7 not support UM77

U32B

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

PCI-E* Link

CLOCKS

CLKOUT_PCIE0N CLKOUT_PCIE0P
PCIECLKRQ0# PCIECLKRQ0# / GPIO73
CLK_PCIE_REV1N CLK_PCIE_REV1P
CLK_PCIE_REQ1# PCIECLKRQ1# / GPIO18
CLKOUT_PCIE1N CLKOUT_PCIE1P
CLKOUT_PCIE2N CLKOUT_PCIE2P
PCIECLKRQ2# PCIECLKRQ2# / GPIO20
CLKOUT_PCIE3N CLKOUT_PCIE3P
PCIECLKRQ3# PCIECLKRQ3# / GPIO25
CLKOUT_PCIE4N CLKOUT_PCIE4P
PCIE_CLKREQ_WLAN# PCIECLKRQ4# / GPIO26
CLKOUT_PCIE5N CLKOUT_PCIE5P
CLK_PCIE_LANN CLK_PCIE_LANP
PCIE_CLKREQ_LAN# PCIECLKRQ5# / GPIO44
CLKOUT_PEG_B_N CLKOUT_PEG_B_P
CLK_PEGB_REQ# PEG_B_CLKRQ# / GPIO56
CLKOUT_PCIE6N CLKOUT_PCIE6P
PCIECLKRQ6# PCIECLKRQ6# / GPIO45
CLKOUT_PCIE7N CLKOUT_PCIE7P
PCIECLKRQ7# PCIECLKRQ7# / GPIO46
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P

TP41 TP40

[30] CLK_PCIE_WLANN [30] CLK_PCIE_WLANP
[30] PCIE_CLKREQ_WLAN#
WLAN
[25] CLK_PCIE_LANN [25] CLK_PCIE_LANP
[25] PCIE_CLKREQ_LAN#
LAN

SMBUS

(+3VS5)
SMBALERT# / GPIO11 SMBALERT#
SMBCLK SMB_PCH_CLK
SMBDATA SMB_PCH_DAT
SML0ALERT# / GPIO60 DRAMRST_CNTRL_PCH
SML0CLK SMB_ME0_CLK
SML0DATA SMB_ME0_DAT
SML1ALERT# / PCHHOT# / GPIO74 SML1ALERT#_R
SML1CLK / GPIO58 SMB_ME1_CLK
SML1DATA / GPIO75 SMB_ME1_DAT

DRAMRST_CNTRL_PCH [3]

CL_CLK1 CL_CLK_R
CL_DATA1 CL_DAT_R
CL_RST1# CL_RST#_R

CLOCKS

PEG_A_CLKRQ# / GPIO47 CLK_PEGA_REQ# [15]
CLKOUT_PEG_A_N CLK_PCIE_VGAN [15]
CLKOUT_PEG_A_P CLK_PCIE_VGAP [15]
EC-C-10
CLKOUT_DMI_N CLK_CPU_BCLKN [3]
CLKOUT_DMI_P CLK_CPU_BCLKP [3]
CLKOUT_DP_N CLK_DPLL_SSCLKN [3]
CLKOUT_DP_P CLK_DPLL_SSCLKP [3]
CLKIN_DMI_N CLK_BUF_PCIE_3GPLL#
CLKIN_DMI_P CLK_BUF_PCIE_3GPLL
CLKIN_GND1_N CLK_BUF_BCLK_N
CLKIN_GND1_P CLK_BUF_BCLK_P
CLKIN_DOT_96N CLK_BUF_DREFCLK#
CLKIN_DOT_96P CLK_BUF_DREFCLK
CLKIN_SATA_N CLK_BUF_DREFSSCLK#
CLKIN_SATA_P CLK_BUF_DREFSSCLK
REFCLK14IN CLK_PCH_14M
CLKIN_PCILOOPBACK CLK_PCI_FB
XTAL25_IN XTAL25_OUT
XCLK_RCOMP R520 90.9/F_4 +1.05V

R523 1M_4
Y4 25MHz
C660 27P/50V/NPO_4
C655 27P/50V/NPO_4

FLEX CLOCKS

(+3V)
CLKOUTFLEX0 / GPIO64 CLK_FLEX0 TP44
CLKOUTFLEX1 / GPIO65 CLK_FLEX1 TP47
CLKOUTFLEX2 / GPIO66 CLK_FLEX2 TP106
CLKOUTFLEX3 / GPIO67 CLK_48M_CARD_R R549 22_4 CLK_48M_CARD [27]
C409 *27P/50V/NPO_4
close to R2108

PLTRST#(CLG)

3V_S5
C692 *0.1U/10V/X7R_4
PCI_PLTRST# PLTRST#
U35 TC7SH08FU
R585 *short_4
R586 100K_4
PLTRST# PLTRST# [3,15,25,27,30]

DGPU Power ON

R610 DIS@0_4
R611 *DIS@0_4
3V_GPU_EN_EC [34]
DGPU_PWR_EN
[45,46] GFXON
R237 *DIS@10K_4
EC-B-03
+3V

SMBus/Pull-up(CLG)

[18,33,34] MBCLK_THRM
[18,33,34] MBDATA_THRM
2N7002KDW Q52A
Q52B 2N7002KDW
Q53A 2N7002KDW
Q53B 2N7002KDW
SMB_ME1_CLK
SMB_ME1_DAT
R272 2.2K_4
R273 2.2K_4
SMB_PCH_DAT
SMB_PCH_CLK
PDAT_SMB [13,14]
PCLK_SMB [13,14]
R280 4.7K_4
R281 4.7K_4
EC-B-17

CLK_REQ/Strap Pin(CLG)

CLK_PCIE_REQ1# R534 10K_4
PCIECLKRQ2# R164 10K_4

PCIECLKRQ0# R552 10K_4
PCIECLKRQ3# R577 10K_4
PCIE_CLKREQ_WLAN# R251 10K_4
CLK_PEGB_REQ# R250 10K_4
PCIECLKRQ6# R229 10K_4
PCIECLKRQ7# R253 10K_4
CLK_PEGA_REQ# R259 DIS@10K_4
PCIE_CLKREQ_LAN# R183 10K_4

CLK_PEGA_REQ# R240 *UMA@10K_4
CLK_BUF_BCLK_N R469 10K_4
CLK_BUF_BCLK_P R468 10K_4

CLK_BUF_PCIE_3GPLL# R124 10K_4
CLK_BUF_PCIE_3GPLL R125 10K_4
CLK_BUF_DREFCLK# R188 10K_4
CLK_BUF_DREFCLK R205 10K_4
CLK_BUF_DREFSSCLK# R134 10K_4
CLK_BUF_DREFSSCLK R139 10K_4
CLK_PCH_14M R211 10K_4

CLOCK TERMINATION for FCIM

PCIE Clock

Layout note:
PCIE_CLKREQ_LAN# layout adjacent to CLK_PEGA_REQ#

DGPU_HOLD_RST# R593 DIS@100K_4
GFXON R243 DIS@100K_4

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R198 *1K_4

SMBus/Pull-up(CLG)

3V_S5
R574 1K_4 DRAMRST_CNTRL_PCH
R252 10K_4 SMBALERT#
R583 2.2K_4 SMB_PCH_CLK
R584 2.2K_4 SMB_PCH_DAT
R562 2.2K_4 SMB_ME0_CLK
R255 2.2K_4 SMB_ME0_DAT
R254 10K_4 SMLIALERT#_R

3V_S5
R214 *10K_4 CL_CLK_R
R191 *10K_4 CL_DAT_R
R185 *10K_4 CL_RST#_R

3V_S5 [3,7,8,10,11,24,30,35,37]
+3V [3,7,8,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 3/6 (PCIE/USB/CLK)	3A

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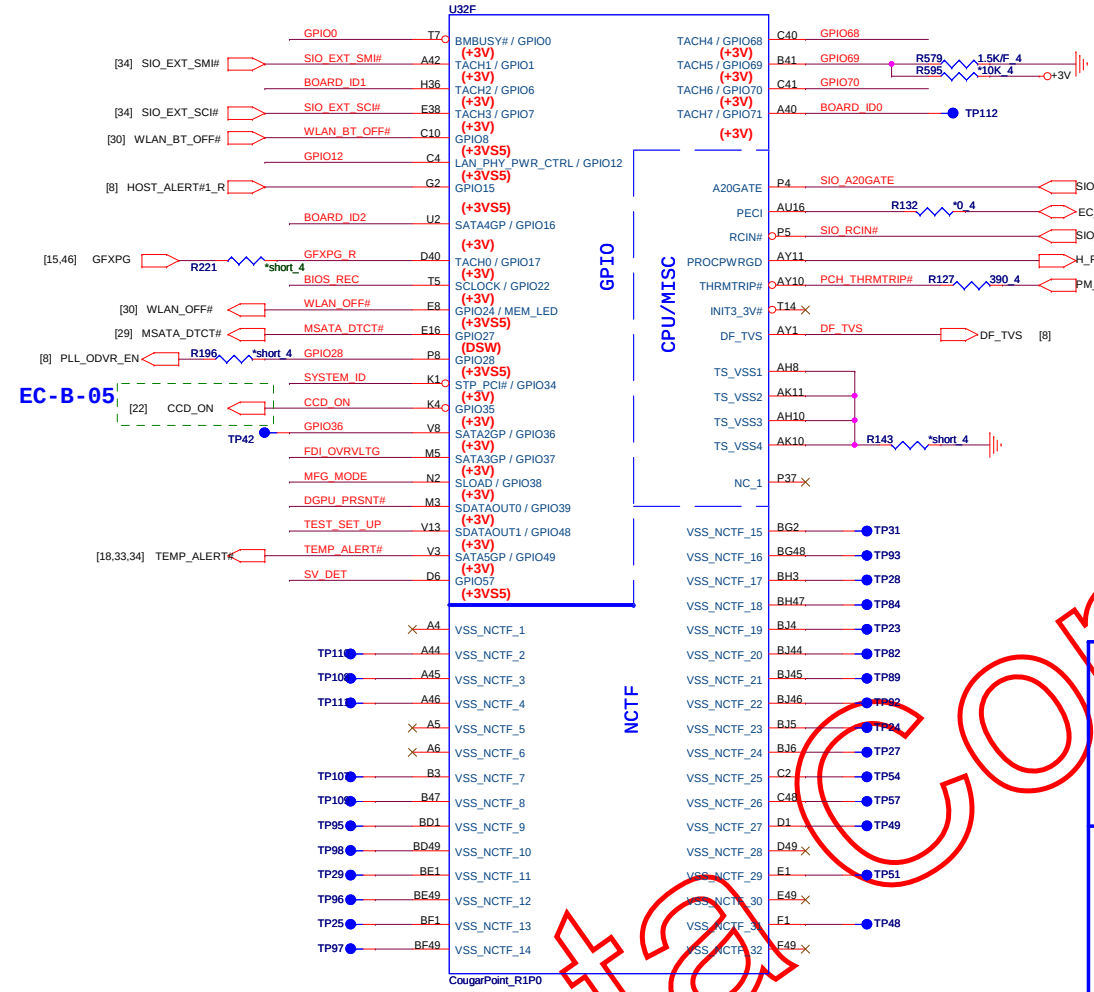
Panther/Cougar Point (GPIO,VSS_NCTF,RSVD)



3V_S5 [3,7,8,9,11,24,30,35,37]
+3V [3,7,8,9,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

BOARD ID SETTING

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

	SYSTEM_ID
LZ7	0
LZ8	1

EC-B-04
EC-C-02

GPIO Pull-up/Pull-down(CLG)

GPIO12	R556	10K_4
WLAN_BT_OFF#	R590	10K_4
MSATA_DTCT#	R264	10K_4
WLAN_OFF#	R249	10K_4

BOARD_ID0	R591	10K_4
GPIO70	R596	10K_4
GPIO0	R161	10K_4
SIO_EXT_SCI#	R230	10K_4
SIO_EXT_SMI#	R594	10K_4
GPIO68	R565	10K_4
SIO_A20GATE	R190	10K_4
SIO_RCIN#	R209	10K_4
TEMP_ALERT#	R519	10K_4
CCD_ON	R543	10K_4

GFXPG_R R207 *DIS@10K_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

GPIO36 R166 *200K/F_4

SV_SET_UP
High = Strong (Default)

TEST_SET_UP R171 10K_4, R170 *0_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW = Tx, Rx terminated to same voltage

R217 100K_4 FDI_OVRVLTG R216 *1K/F_4

3V_S5 R245 *10K_4 SV_DET R246 100K_4

MFG-TEST

MFG_MODE R535 10K_4, R536 *0_4

	Optimus	UMA
Stuff	R547	R546
No Stuff	R546	R547

R546 *UMA@10K_4 DGPU_PRSNT# R547 DIS@100K_4

BIOS_REC R182 10K_4, R181 *0_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

SYSTEM_ID R544 10K_4, R550 *10K_4

BOARD_ID1 R558 *10K_4, R526 10K_4, R572 *10K_4
BOARD_ID2 R557 10K_4, R527 *10K_4, R573 10K_4
[8] BOARD_ID3

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	3A

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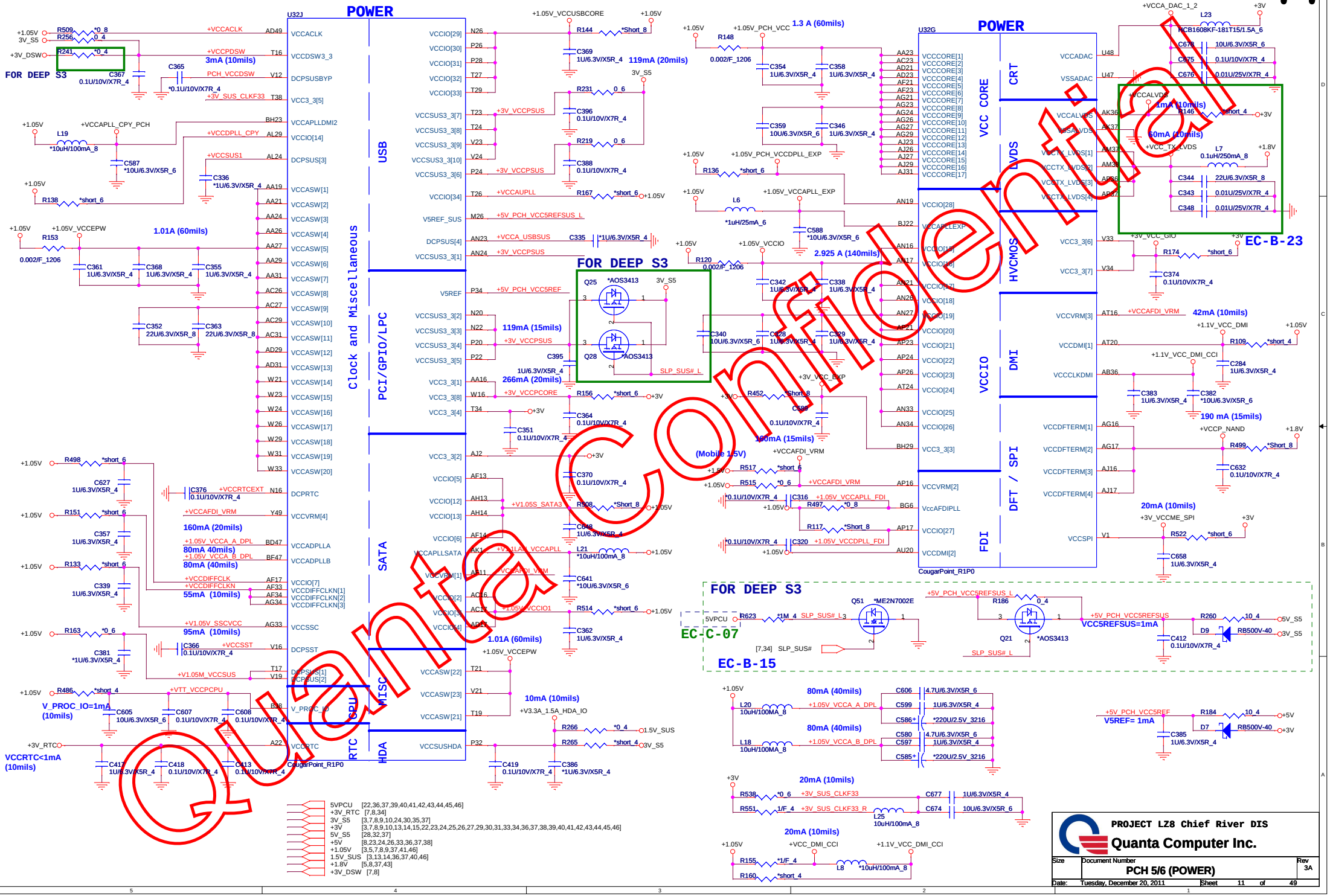
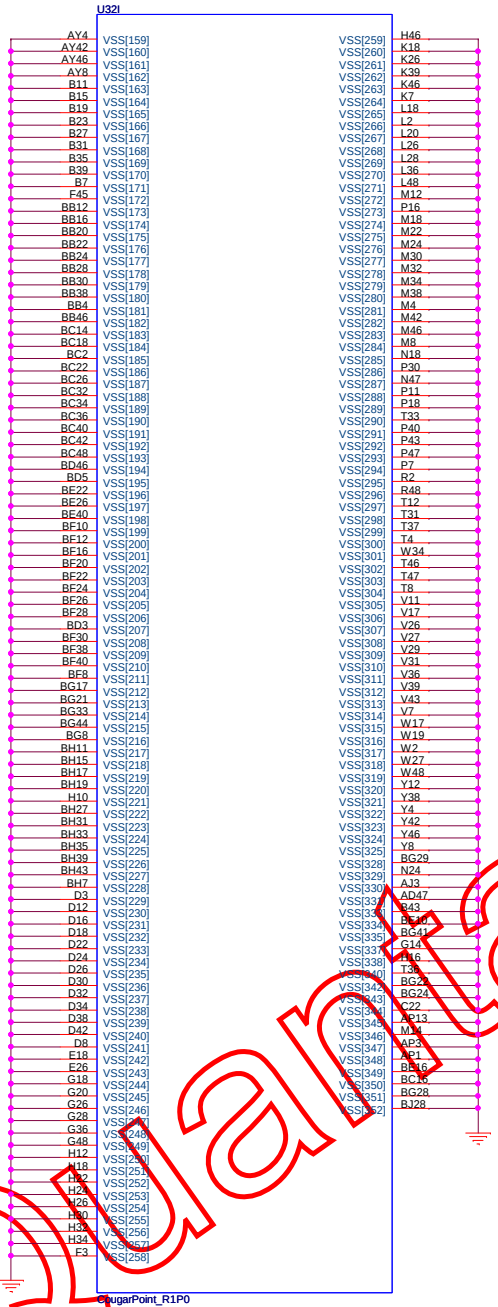
Panther/Cougar Point-M (POWER)

Panther/COUGAR POINT (POWER)



5VPCU [22,36,37,39,40,41,42,43,44,45,46]
+3V_RTC [7,8,34]
3V_S5 [3,7,8,9,10,24,30,35,37]
+3V [3,7,8,9,10,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
5V_S5 [28,32,37]
+5V [8,23,24,26,33,36,37,38]
+1.05V [3,5,7,8,9,37,41,46]
1.5V_SUS [3,13,14,36,37,40,46]
+1.8V [5,8,37,43]
+3V_DSW [7,8]

Panther/Cougar Point-M (GND)

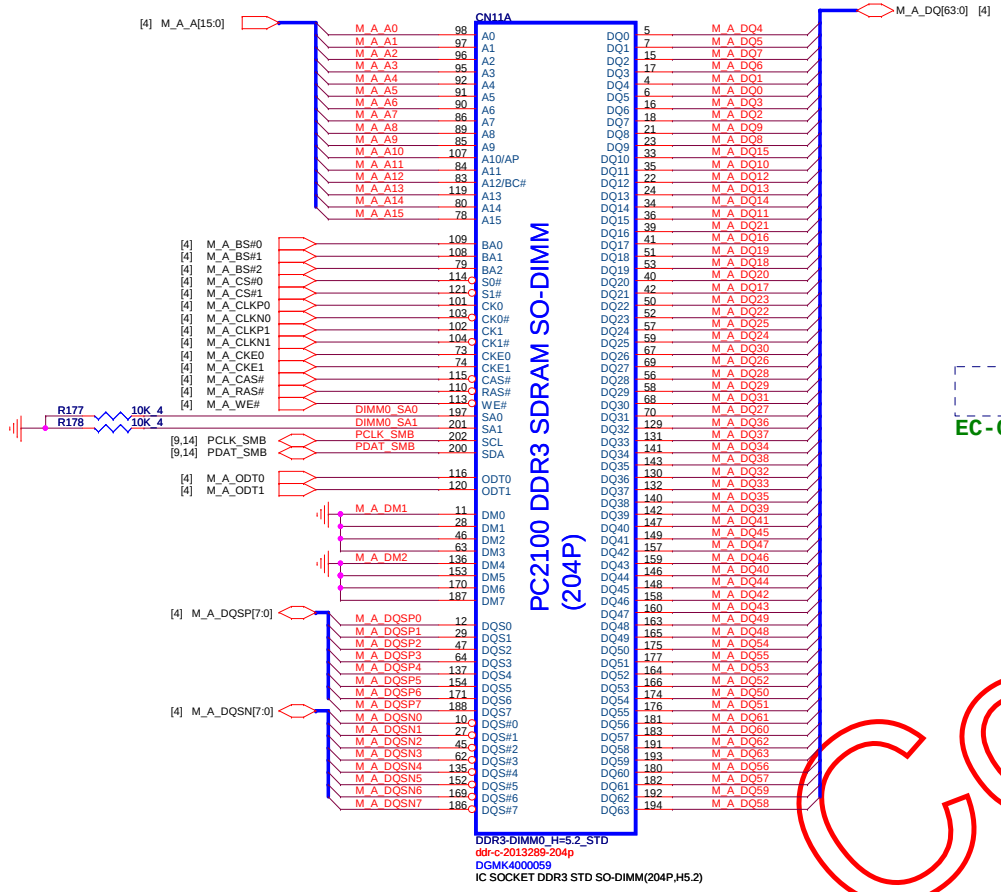


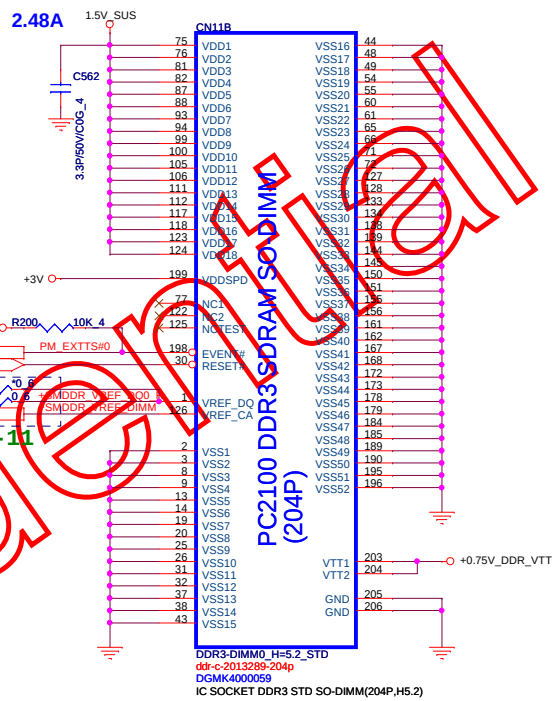
Panther/Cougar Point-M (GND)

PROJECT LZ8 Chief River DIS

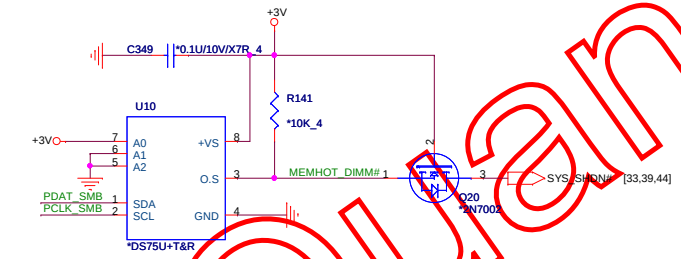
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 6/6 (GND)	1A
Date: Friday, November 11, 2011	Sheet 12 of 49	



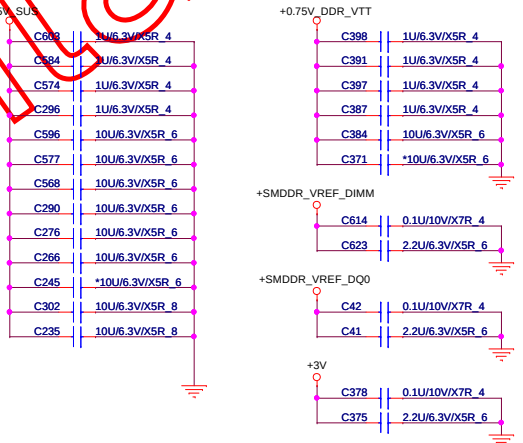


+0.75V_DDR_VTT [14,37,40]
1.5V_SUS [3,11,14,36,37,40,46]
+3V [3,7,8,9,10,11,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
SMDDR_VREF [5,14,40]

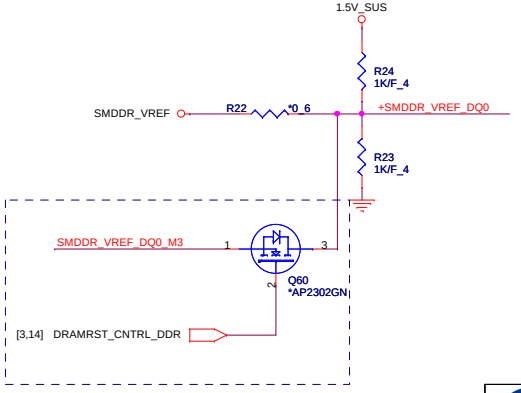


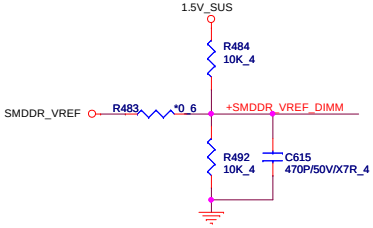
ADDRESS: 92H Close DDR3 socket CN22,CN23

Place these Caps near So-Dimm0.



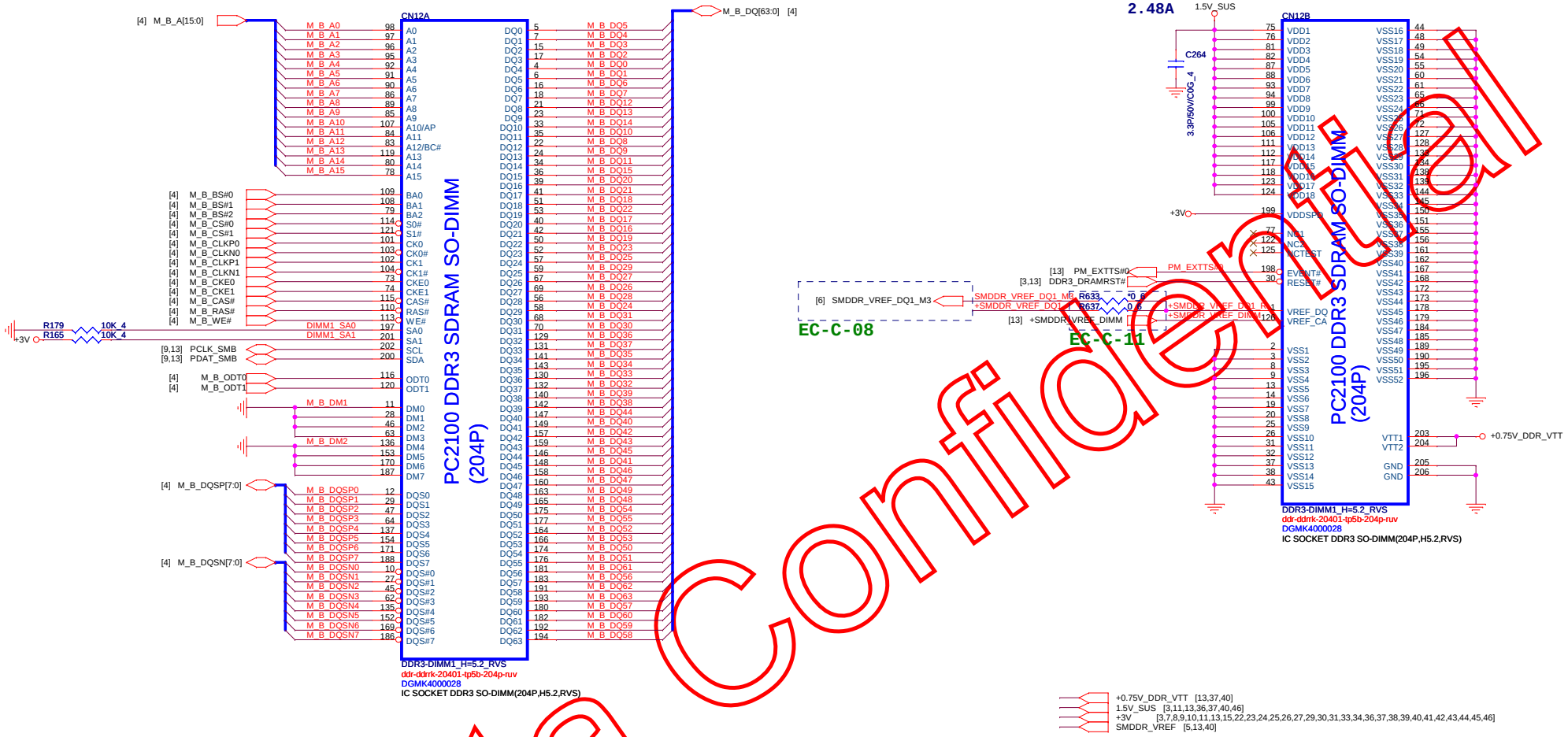
VREF DQ0 M1/M3 Solution



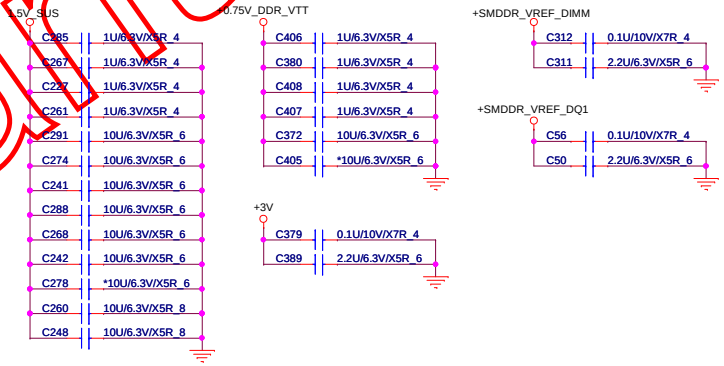


PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

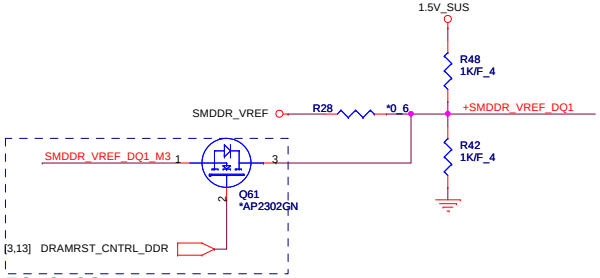
Size	Document Number	Rev
	Custom DDR3 DIMM0-STD (5.2H)	3A
Date: Tuesday, December 20, 2011	Sheet 13 of 49	



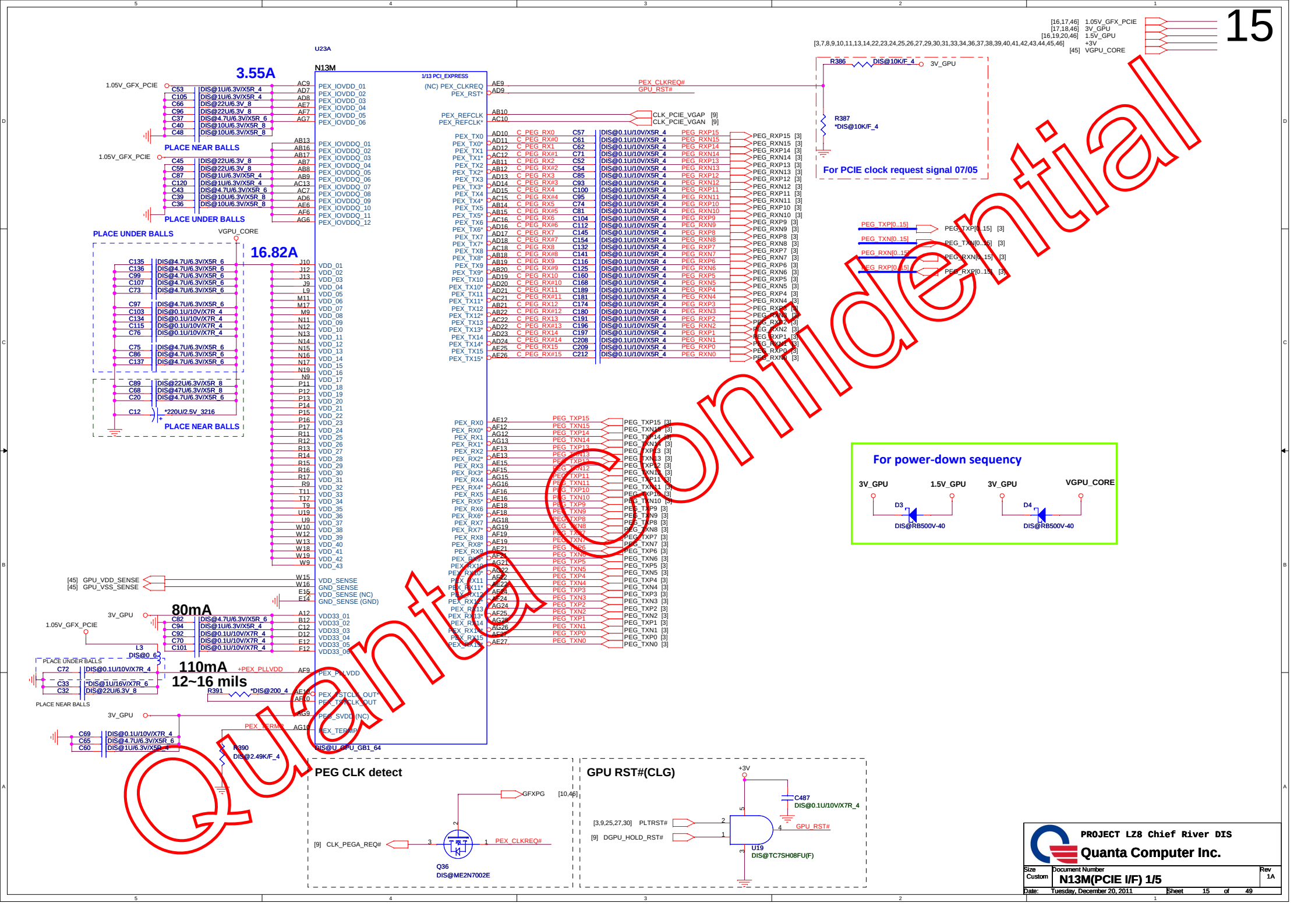
Place these Caps near So-Dimm1.



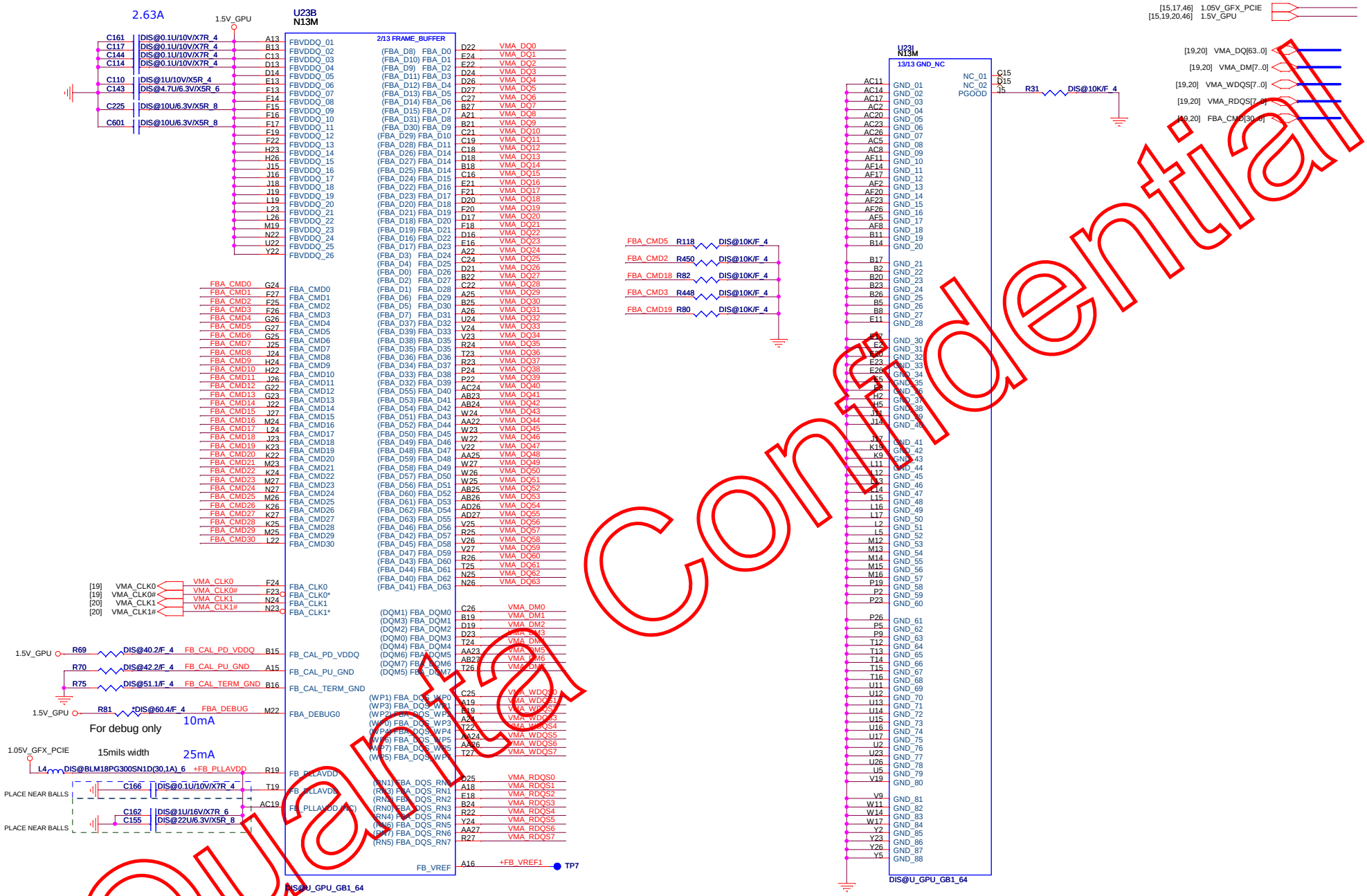
VREF DQ1 M1/M3 Solution



PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number Custom	Rev 3A
	DDR3 DIMM1-RVS (4.0H)	
Date: Tuesday, December 20, 2011	Sheet 14 of 49	



PROJECT	LZ8 Chief River DIS
Quanta Computer Inc.	
Size	Custom
Document Number	N13M(PCIE I/F) 1/5
Rev	1A
Date:	Tuesday, December 20, 2011
Sheet	15 of 49



PROJECT LZ8 Chief River DIS			
Quanta Computer Inc.			
Size: Custom	Document Number: N13M(MEMORY I/F & GND) 2/5		Rev: 1A
Date: Tuesday, December 20, 2011		Sheet 16 of 49	

[15,16,46] 1.05V_GFX_PCIE
[15,18,46] 3V_GPU

220 mA (1.05V +/- 3%)

220 mA (1.8V)

220 mA

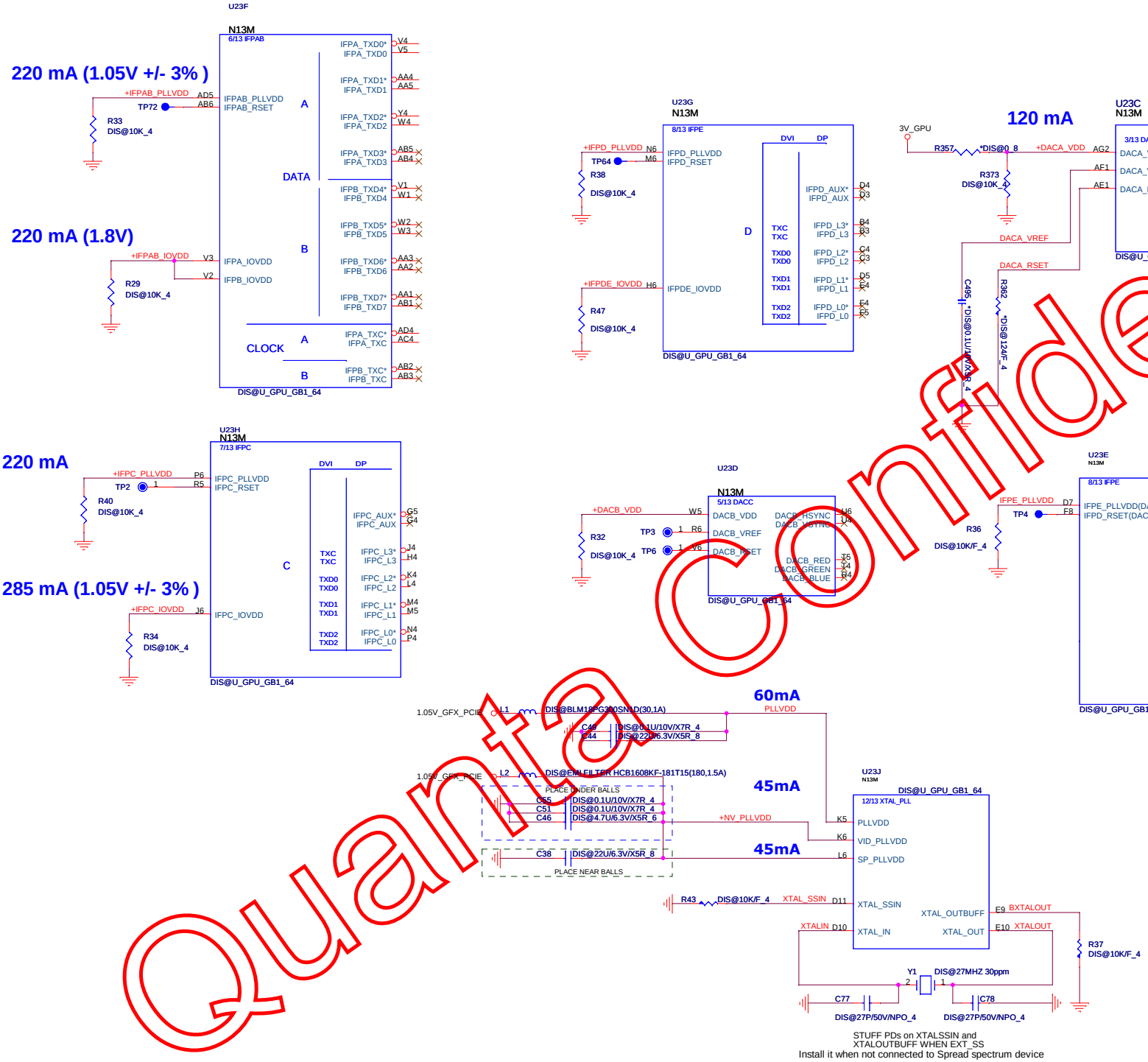
285 mA (1.05V +/- 3%)

120 mA

60mA

45mA

45mA



PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N13M(DISPLAY) 3/5	1A

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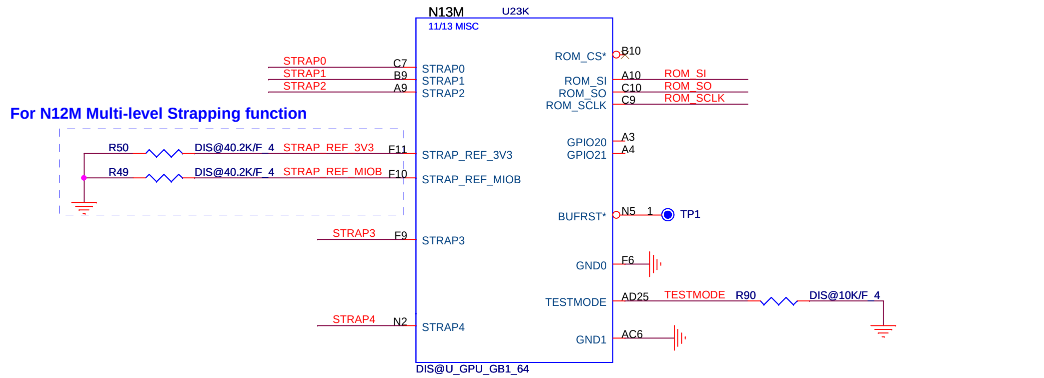
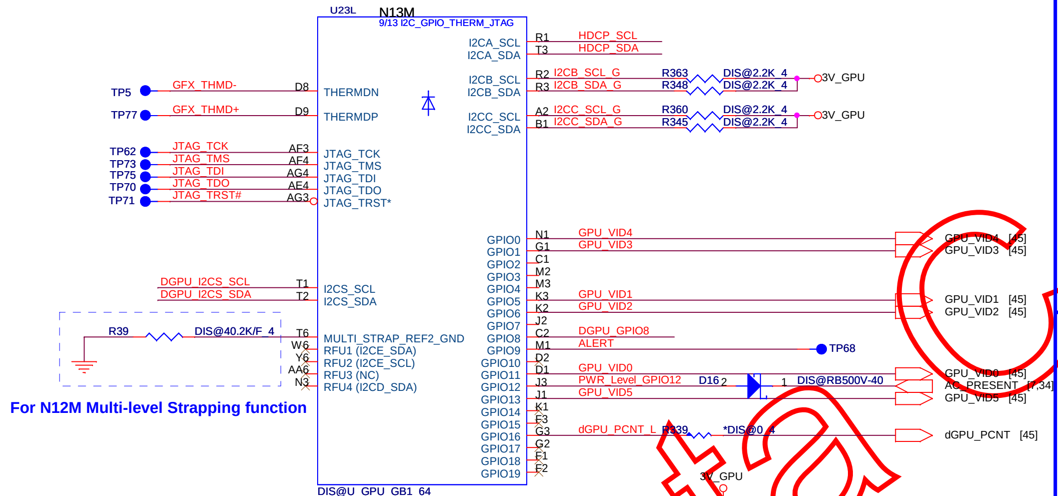
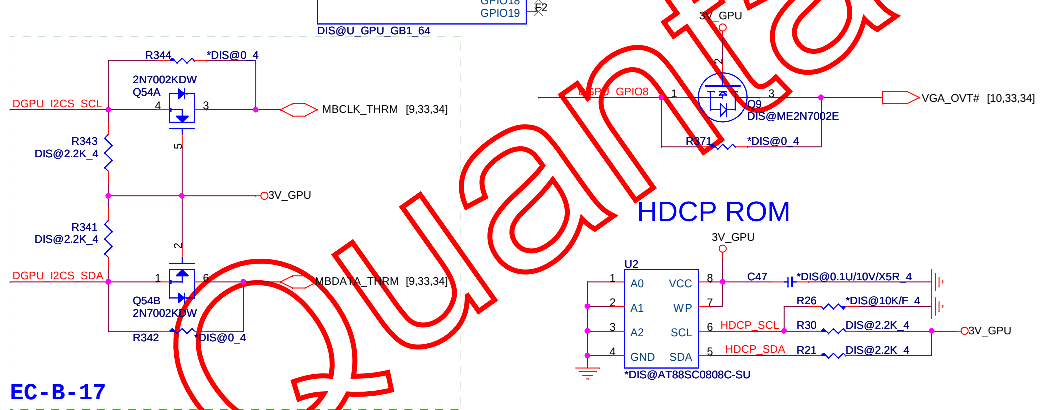
nV FAE suggest that the device ID
for N13M-GE1 is 0x1058



9.5 Unused I2C Pins

For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 kΩ resistors.routing.





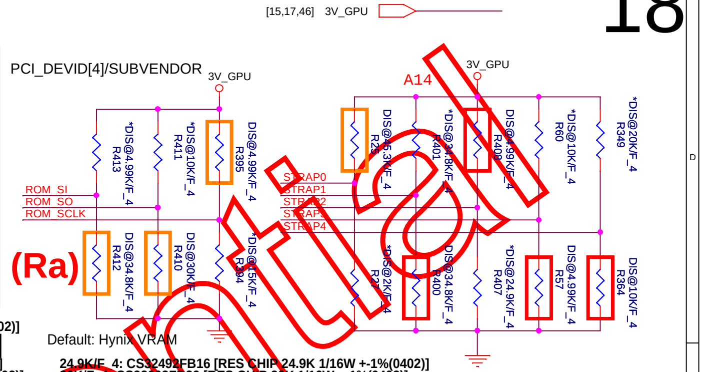
DHCP ROM	
HDCP_SCL	Low: Crypto ROM
	Hi: I2C ROM

Logical Strap Bit Mapping		
Rv	PU-VDD	PD-GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

N13M-GE1

(Ra)

PCI_DEVID[4]/SUBVENDOR



Default: Hynix VRAM

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30K/F_4: CS33002FB13 [RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4: CS33482FB22 [RES CHIP 34.8K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]
24.9K/F_4: CS32492FB16 [RES CHIP 24.9K 1/16W +-1%(0402)]
20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]

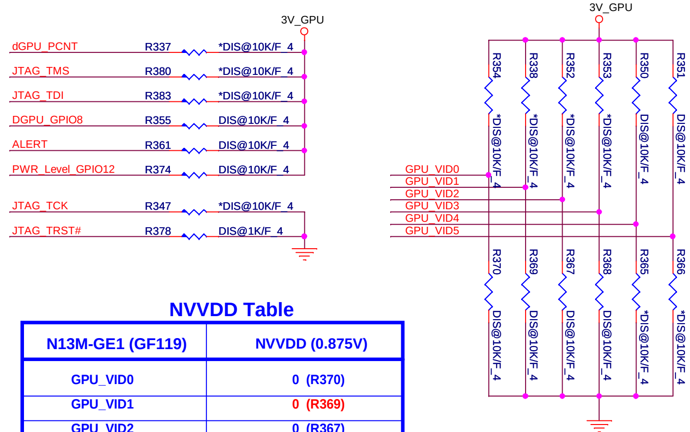
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO N13M-GE1	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0101
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001

VRAM Configuration Table

(Ra)

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001		Reserved		
0010		Reserved		
0011		Reserved		
0101		Reserved		
0110		Reserved		
0110	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	PD 34.8K/F
0111	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	PD 45.3K/F

AKD5MGWTW00
AKD5MGWT500



GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low= Battery
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

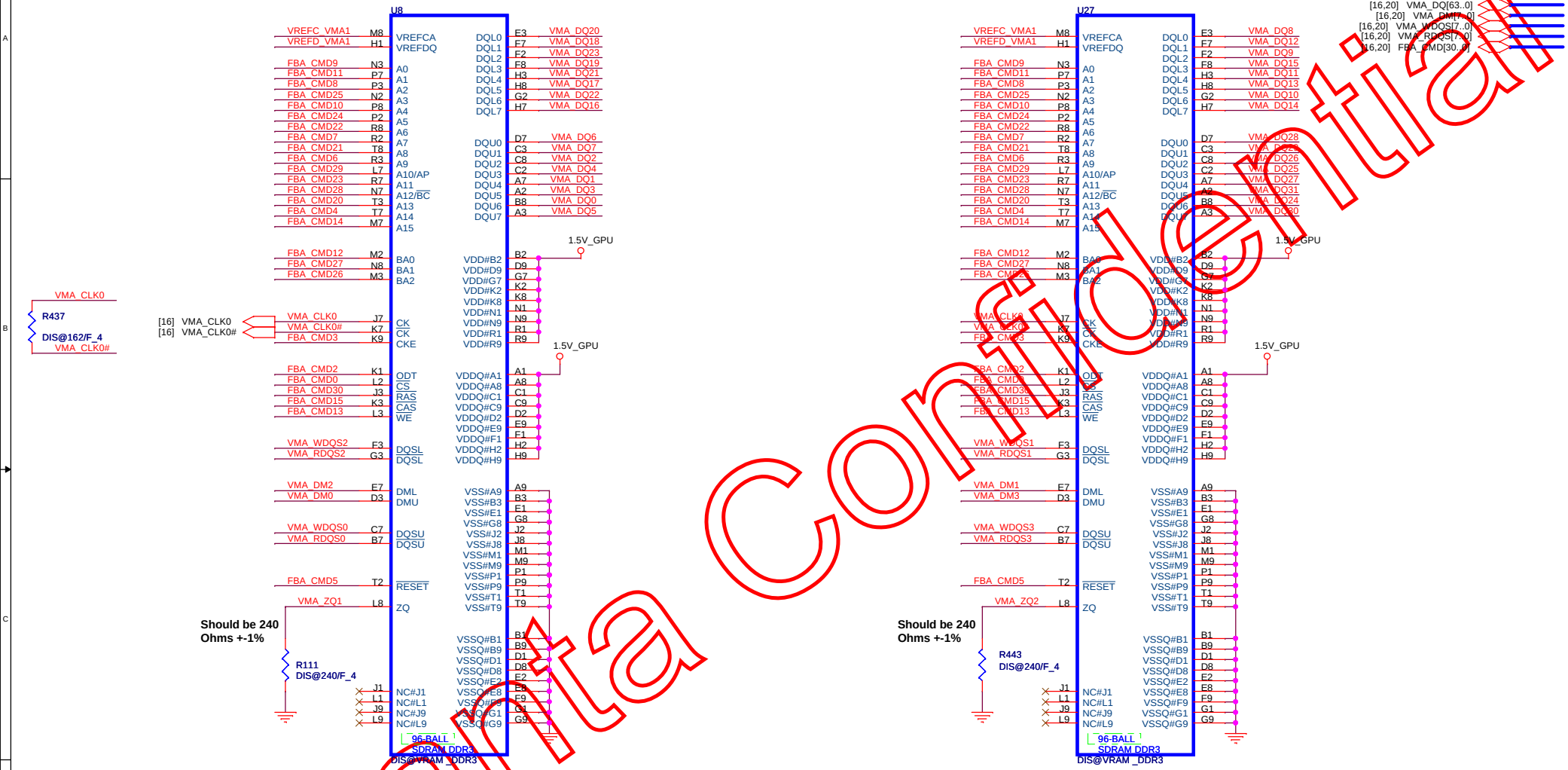
NVVDD Table

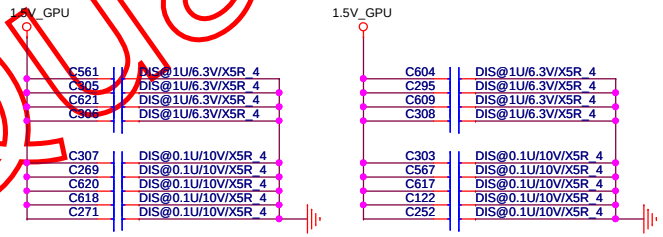
N13M-GE1 (GF119)	NVVDD (0.875V)
GPU_VID0	0 (R370)
GPU_VID1	0 (R369)
GPU_VID2	0 (R367)
GPU_VID3	0 (R368)
GPU_VID4	1 (R350)
GPU_VID5	1 (R351)

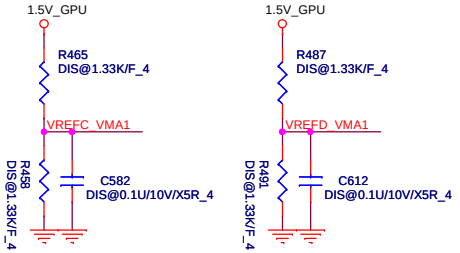
CHANNEL A: 1024MB DDR3

[15,16,20,46] 1.5V_GPU

[16,20] VMA_DQ[63..0]
[16,20] VMA_DM[7..0]
[16,20] VMA_WDQS[7..0]
[16,20] VMA_RDQS[7..0]
[16,20] FBA_CMD[30..0]







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Quanta Computer Inc.

Size	Document Number	Rev
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CHANNEL A: 1024MB DDR3

[15,16,19,46] 1.5V_GPU

[16,19] VMA_DQ[63..0]
[16,19] VMA_DM[7..0]
[16,19] VMA_WDQS[7..0]
[16,19] FBA_CMD[30..0]
[16,19] VMA_RDQS[7..0]

U9

VREFC_VMA3 M8
VREFD_VMA3 H1
VREFCA
VREFDQ

FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
BA0 BA1 BA2

VMA_CLK1 [16]
VMA_CLK1# [16]
FBA_CMD19 K9
J7 K7 K9
CK CK CKE

FBA_CMD18 K1
FBA_CMD16 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
ODT CS RAS CAS WE

VMA_WDQS5 F3
VMA_RDQS5 G3
DQSL DQSL

VMA_DM5 E7
VMA_DM4 D3
DML DMU

VMA_WDQS4 C7
VMA_RDQS4 B7
DQSU DQSU

FBA_CMD5 T2
RESET

VMA_ZQ3 L8
ZQ

Should be 240 Ohms +-1%

R122
DIS@240/F_4

J1 L1 J9 L9
NC#J1 NC#L1 NC#J9 NC#L9

96-BALL SDRAM DDR3
DIS@VRAM _DDR3

DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
E3 F7 F2 F8 H3 H8 G2 H7
VMA_DQ45 VMA_DQ41 VMA_DQ43 VMA_DQ40 VMA_DQ47 VMA_DQ44 VMA_DQ46 VMA_DQ42

DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
D7 C3 C8 C2 A7 A2 B8 A3
VMA_DQ37 VMA_DQ39 VMA_DQ32 VMA_DQ36 VMA_DQ33 VMA_DQ35 VMA_DQ34 VMA_DQ38

1.5V_GPU

VDD#B2 VDD#D9 VDD#G7 VDD#K2 VDD#K8 VDD#N1 VDD#N9 VDD#R1 VDD#R9
B2 D9 G7 K2 K8 N1 N9 R1 R9

1.5V_GPU

VDDQ#A1 VDDQ#A8 VDDQ#C1 VDDQ#C9 VDDQ#D2 VDDQ#E9 VDDQ#F1 VDDQ#H2 VDDQ#H9
A1 A8 C1 C9 D2 E9 F1 H2 H9

VSS#A9 VSS#B3 VSS#E1 VSS#G8 VSS#J2 VSS#J8 VSS#M1 VSS#M9 VSS#P1 VSS#P9 VSS#T1 VSS#T9
A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9

VSSQ#B1 VSSQ#B9 VSSQ#D1 VSSQ#D8 VSSQ#E2 VSSQ#E8 VSSQ#F9 VSSQ#G1 VSSQ#G9
B1 B9 D1 D8 E2 E8 F9 G1 G9

U28

VREFC_VMA3 M8
VREFD_VMA3 H1
VREFCA
VREFDQ

FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
BA0 BA1 BA2

VMA_CLK1
VMA_CLK1#
FBA_CMD19 K9
J7 K7 K9
CK CK CKE

FBA_CMD18 K1
FBA_CMD16 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
ODT CS RAS CAS WE

VMA_WDQS7 F3
VMA_RDQS7 G3
DQSL DQSL

VMA_DM7 E7
VMA_DM6 D3
DML DMU

VMA_WDQS6 C7
VMA_RDQS6 B7
DQSU DQSU

FBA_CMD5 T2
RESET

VMA_ZQ4 L8
ZQ

R427
DIS@240/F_4

J1 L1 J9 L9
NC#J1 NC#L1 NC#J9 NC#L9

96-BALL SDRAM DDR3
DIS@VRAM _DDR3

DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
E3 F7 F2 F8 H3 H8 G2 H7
VMA_DQ56 VMA_DQ60 VMA_DQ58 VMA_DQ57 VMA_DQ59 VMA_DQ63 VMA_DQ61 VMA_DQ62

DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
D7 C3 C8 C2 A7 A2 B8 A3
VMA_DQ51 VMA_DQ53 VMA_DQ49 VMA_DQ54 VMA_DQ48 VMA_DQ55 VMA_DQ50 VMA_DQ52

1.5V_GPU

VDD#B2 VDD#D9 VDD#G7 VDD#K2 VDD#K8 VDD#N1 VDD#N9 VDD#R1 VDD#R9
B2 D9 G7 K2 K8 N1 N9 R1 R9

1.5V_GPU

VDDQ#A1 VDDQ#A8 VDDQ#C1 VDDQ#C9 VDDQ#D2 VDDQ#E9 VDDQ#F1 VDDQ#H2 VDDQ#H9
A1 A8 C1 C9 D2 E9 F1 H2 H9

VSS#A9 VSS#B3 VSS#E1 VSS#G8 VSS#J2 VSS#J8 VSS#M1 VSS#M9 VSS#P1 VSS#P9 VSS#T1 VSS#T9
A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9

VSSQ#B1 VSSQ#B9 VSSQ#D1 VSSQ#D8 VSSQ#E2 VSSQ#E8 VSSQ#F9 VSSQ#G1 VSSQ#G9
B1 B9 D1 D8 E2 E8 F9 G1 G9

VMA_CLK1
R123
DIS@162/F_4
VMA_CLK1#

1.5V_GPU

C265 C283 C622 C581 DIS@1U/6.3V/X5R_4
C298 C297 C616 C183 C598 DIS@0.1U/10V/X5R_4

1.5V_GPU

C602 C610 C613 C619 DIS@1U/6.3V/X5R_4
C611 C272 C263 C304 C275 DIS@0.1U/10V/X5R_4

1.5V_GPU

R460
DIS@1.33K/F_4
VREFC_VMA3
R471
DIS@1.33K/F_4
C595
DIS@0.1U/10V/X5R_4

1.5V_GPU

R116
DIS@1.33K/F_4
VREFD_VMA3
R110
DIS@1.33K/F_4
C287
DIS@0.1U/10V/X5R_4

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	N13M (DDR3) 6/6	1A

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PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Blank	1A

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+3V [3,7,8,9,10,11,13,14,15,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
3VPCU [7,8,25,30,31,34,35,36,37,38,39,43,45]
15V [37,39,40,46]
VIN [36,38,39,40,41,42,44,45]
5VPCU [11,36,37,39,40,41,42,43,44,45,46]

LCDVCC

15V, +3V, +LCDVCC
R10 330K_4
Q1 AO3404
R5 47_8
C2 10U/6.3V/X5R_8
LCDVCC_ON
C9 0.027U/25V/X7R_6
EC-C-04
5VPCU
Q58A 2N7002
Q58B 2N7002
EC-C-04
R16 100K_4
Q8 PDTC144EU
[7] INT_DISP_ON
R14 10K_4

Back light

3VPCU, +3V
R12 10K_4
R2 *4.7K_4
[31,34] LID#
RB500V-40
D2
D1
RB500V-40
DISPON
C10 0.1U/10V/X7R_4
R6 100K_4
C3 *47P/50V/NPO_4
[7] INT_LVDS_BLON
R3 2.2K_4
R4 10K_4
C6 *1U/10V/X7R_6
Q7 PDTC144EU
LCD_BK_OFF [8]

EC-B-22

[34] EC_BRIGHT_PWM
R639 0_4
EC-C-06
[7] INT_DFST_PWM
R9 *0_4
VADJ_PWM
C8 *47P/50V/NPO_4
EC-B-22

GFX_PWR_SRC
C467 0.1U/25V/X7R_6
C468 0.1U/25V/X7R_6
C480 *10U/25V/X6S_12
R334 *Short_8
VIN

For EMI

INT_TXLCLKN
INT_TXLCLKP
C477 *6.8P/50V/NPO_4
C476 *6.8P/50V/NPO_4
For EMI

LVDS_DDC_SCL
LVDS_DDC_SDA
C479 *2200P/50V/X7R_4
C478 *2200P/50V/X7R_4
For EMI
For ESD

For ESD

SC1 *0.1U/10V/X7R_4
C5 *2.2U/6.3V/X5R_6
+LCDVCC
+3V
CN5

EC-B-22

[7] LVDS_DDC_SCL
[7] LVDS_DDC_SDA
[7] INT_TXLOUTN0
[7] INT_TXLOUTP0
[7] INT_TXLOUTN1
[7] INT_TXLOUTP1
[7] INT_TXLOUTN2
[7] INT_TXLOUTP2
[7] INT_TXLCLKN
[7] INT_TXLCLKP
[34] IMG_EN
[34] DCR_EN
R634 10K_4
R635 10K_4
EC-C-09

LVDS_DDC_SCL
LVDS_DDC_SDA
INT_TXLOUTN0
INT_TXLOUTP0
INT_TXLOUTN1
INT_TXLOUTP1
INT_TXLOUTN2
INT_TXLOUTP2
INT_TXLCLKN
INT_TXLCLKP
VADJ_PWM
DISPON
GFX_PWR_SRC
LVD-A30SFYG+

+3V
C475 *47P/50V/NPO_4
C474 *47P/50V/NPO_4
close to CN5
+3V
R384 2.2K_4
R385 2.2K_4
LVDS_DDC_SDA
LVDS_DDC_SCL

LVDS (14") (1024x600, 1366x768)

CAMERA CONN

CN7
+CAM_VCC
USBP2- R
USBP2+ R
VCC_3V
D-
D+
GND
GND_SHIELD
G1
G2
CAMERA_CONN

FOR ESD
[9] USBP2-
[9] USBP2+
CML3
DLW21HN900SQ2L
USBP2- R
USBP2+ R
U18
IO1 VIN
IO2 GND
PJSR05
+CAM_VCC
EC-B-18

CAMERA VCC Control

+3V
R612 10K_4
R613 10K_4
Q48 AOS3413
R7 *0_6
[10] CCD_ON
Q49 PDTC144EU
C724 2200P/50V/X7R_6
+CAM_VCC
C1 1U/6.3V/X5R_4
C4 0.1U/10V/X7R_4
EC-B-05

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

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	LCD/CAMERA	3A
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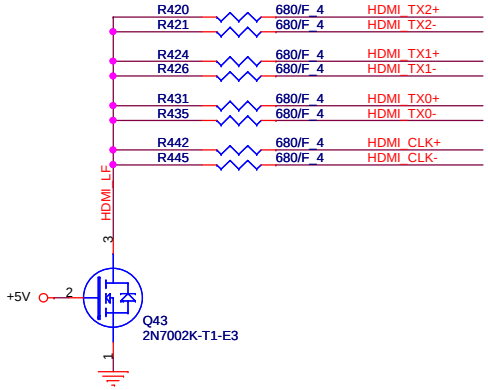
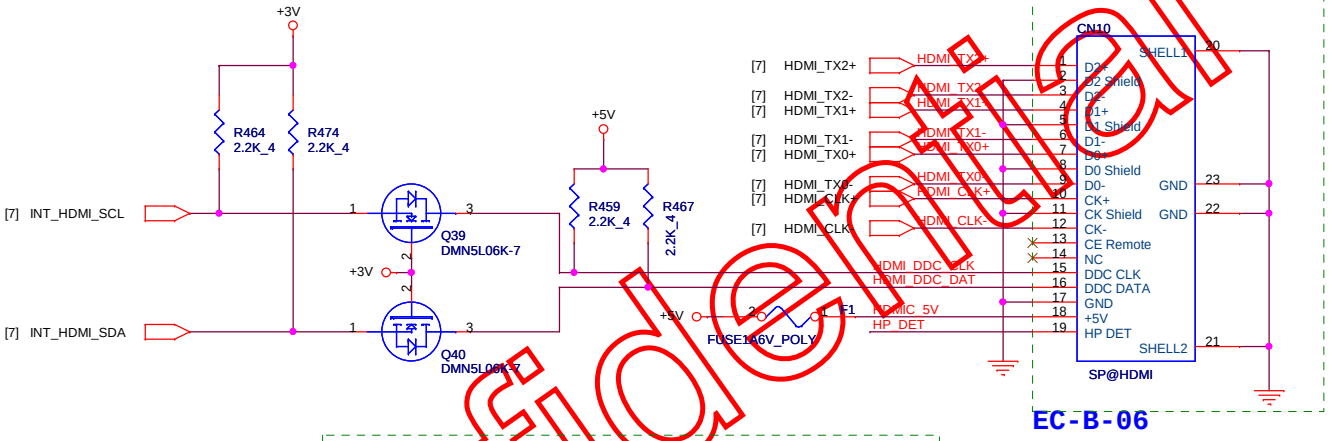
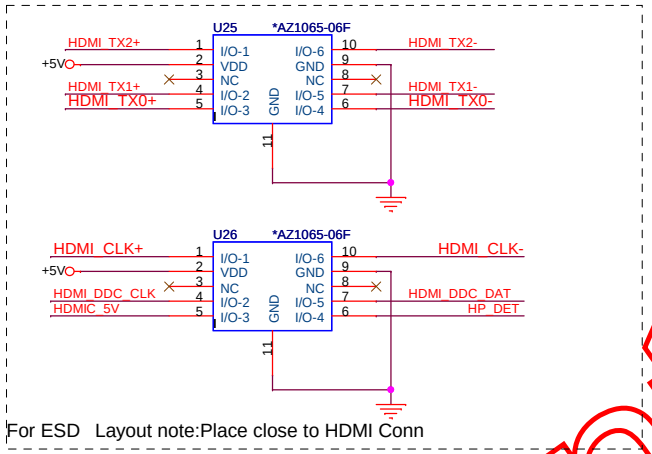
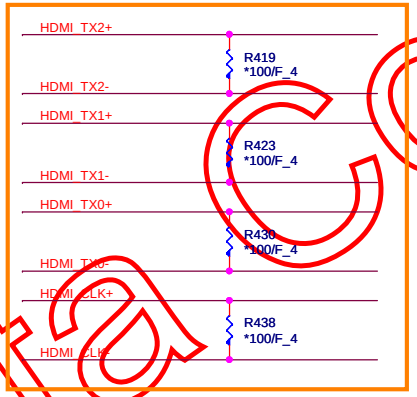
[3,7,8,9,10,11,13,14,15,22,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46] +3V
[8,11,24,26,33,36,37,38] +5V

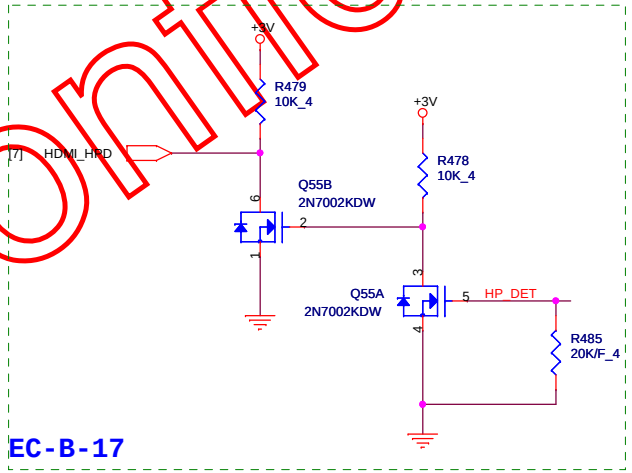


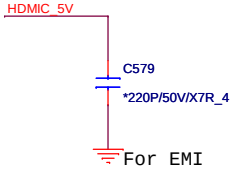




EMI reserve for HDMI







PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

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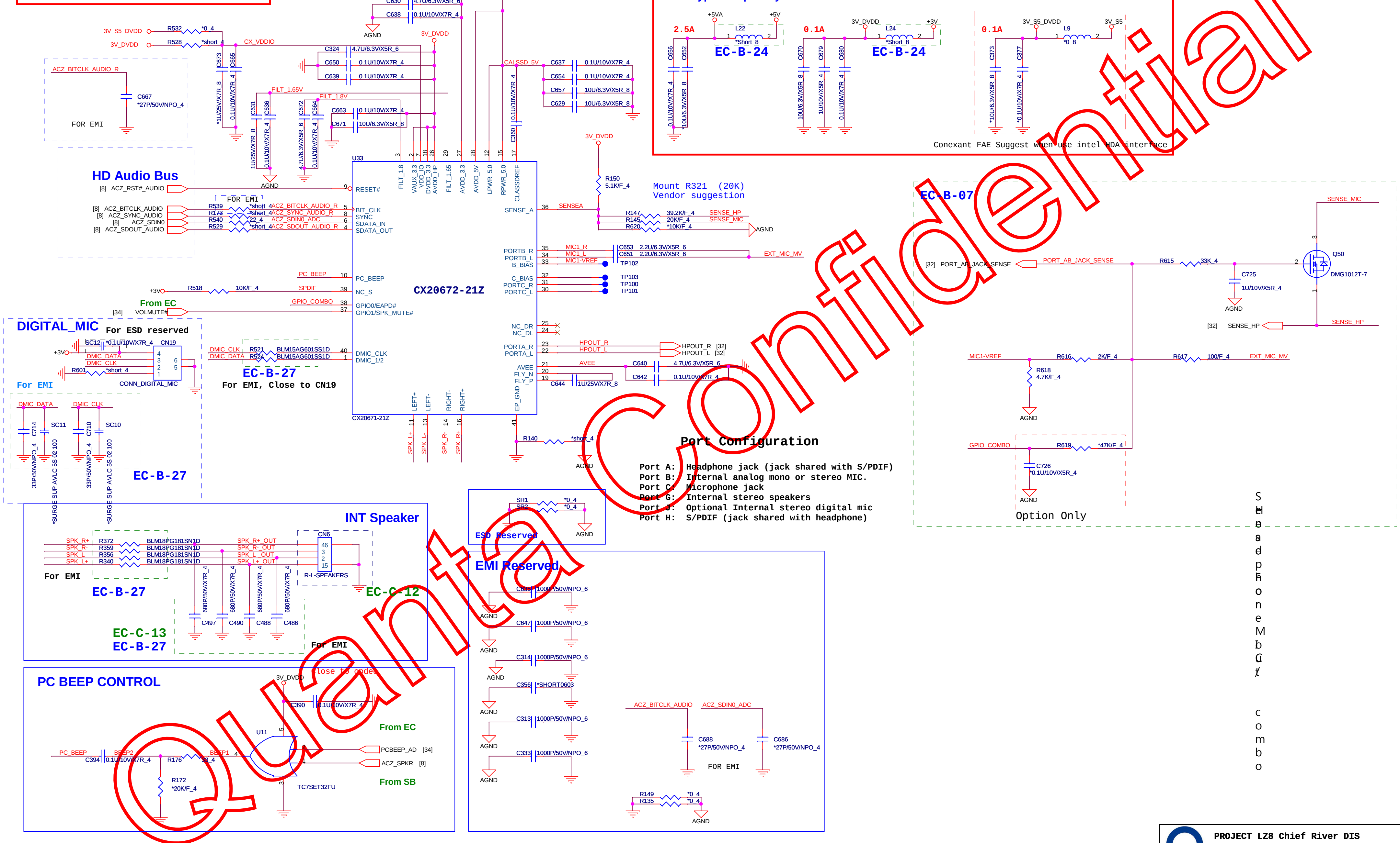
Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono or stereo MIC.
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)

Seadphone Mic combo

PROJECT LZ8 Chief River DIS
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	AUDIO CODEC CX20672	2A

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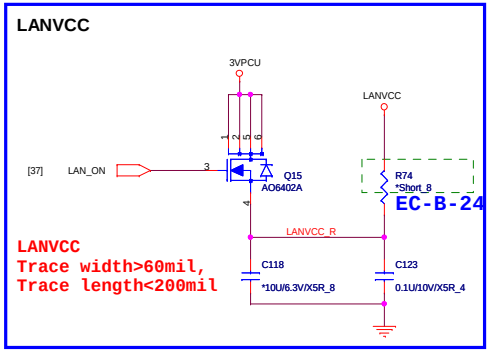
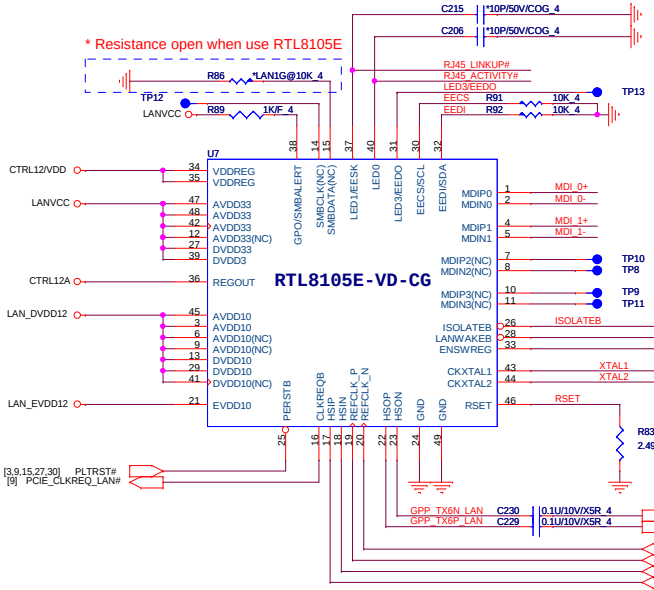
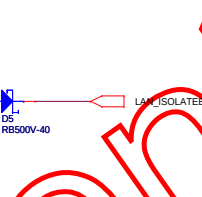
LANVCC

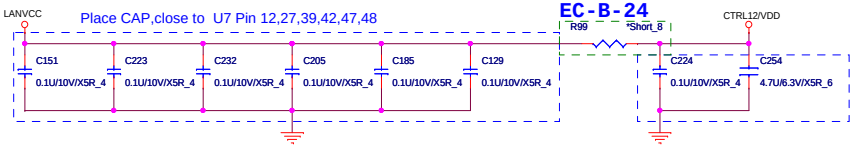


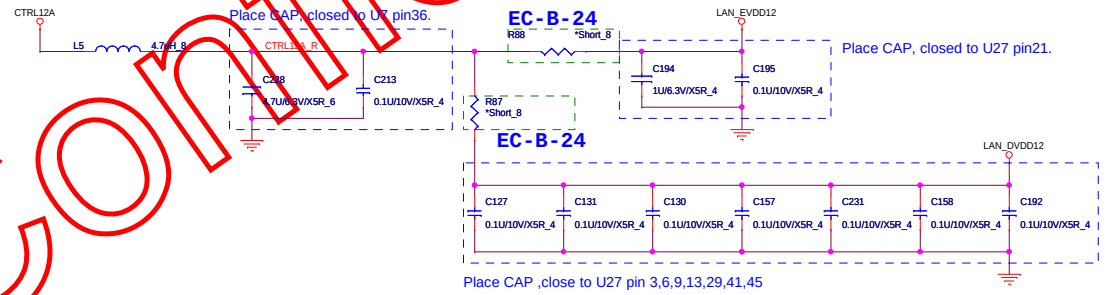
LANVCC
Trace width>60mil,
Trace length<200mil

* Resistance open when use RTL8105E

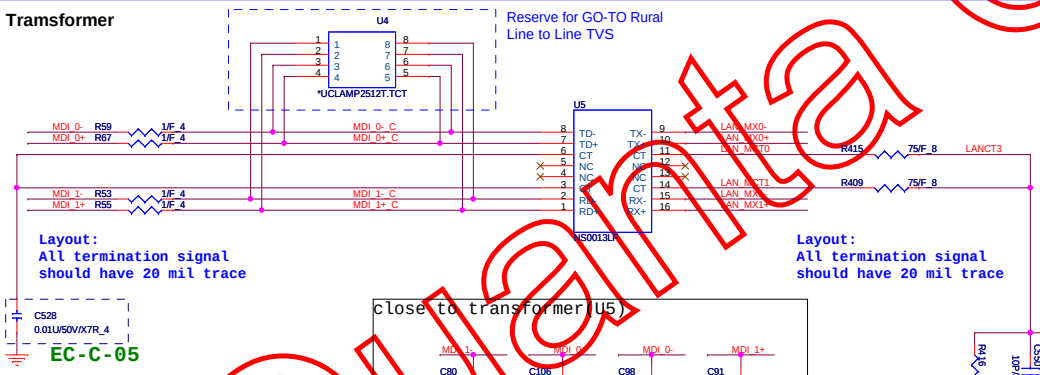




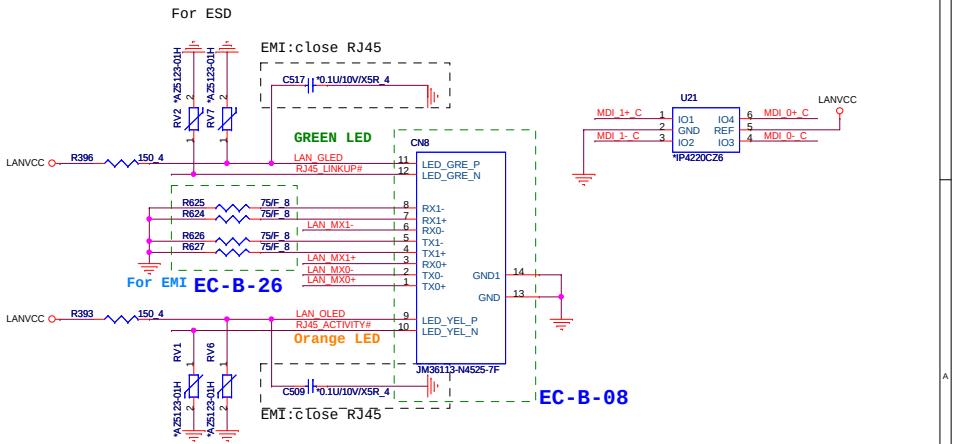




Tramsformer



RJ45 Connector



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Quanta Computer Inc.		
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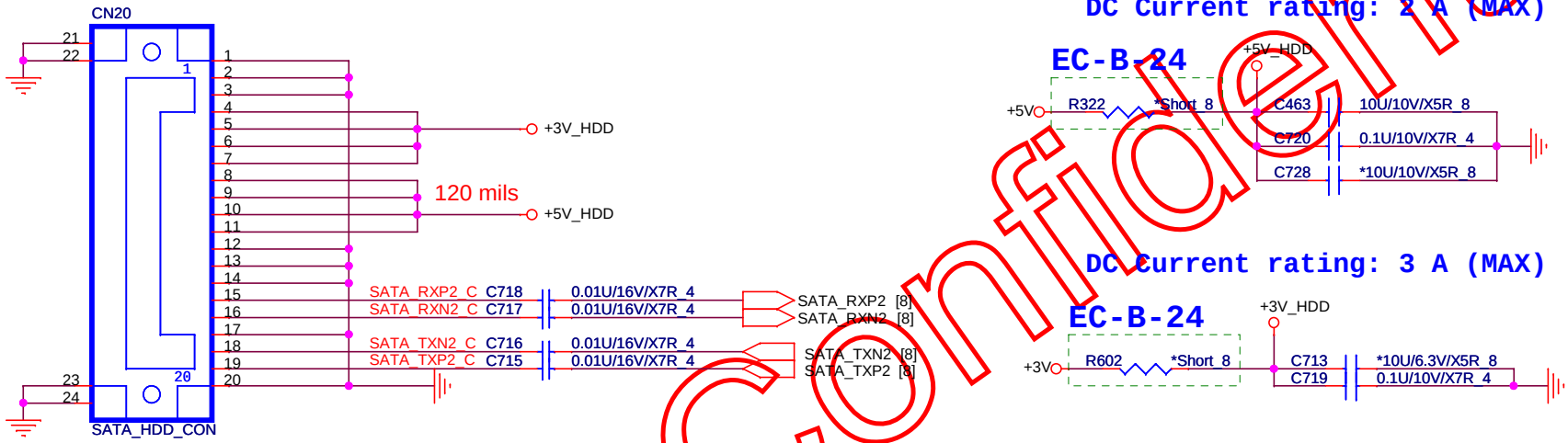
HDD

PLACE SATA AC COUPLING
CAPS CLOSE TO Connector

+3V [3,7,8,9,10,11,13,14,15,22,23,24,25,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
+5V [8,11,23,24,33,36,37,38]



PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	SATA	1A
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AU6435-GDL CARD READER Controller

[3,7,8,9,10,11,13,14,15,22,23,24,25,26,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46] +3V

R277	0	Normal mode
	1	Saving mode

option for power reset or system reset

EC-C-01

EC-B-24

EC-B-21

2 IN 1 CARD READER (SD/MMC)

QCI P/N : DFHD14MS009
TTN P/N : PSDBT4-09GLAG1004N1

Main	DFHD14MS009
Second	

Close to CNxx Pin 6

CTRL0, CRTL 1 trace length shorter and surround with GND

crystal trace width needs at least 10 mils.

Clock input selection
'1' for 48MHz input [Default]
'0' for 12MHz input

SD write protect
1:decided by SDWP[Default]
0:letting SD always write-able

for EMI

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

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	AU6435-GDL CARD READER Controller	3A

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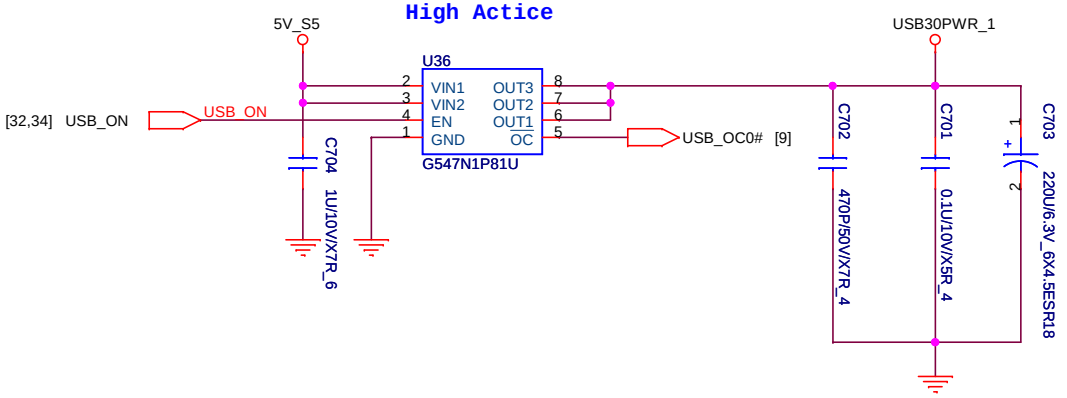
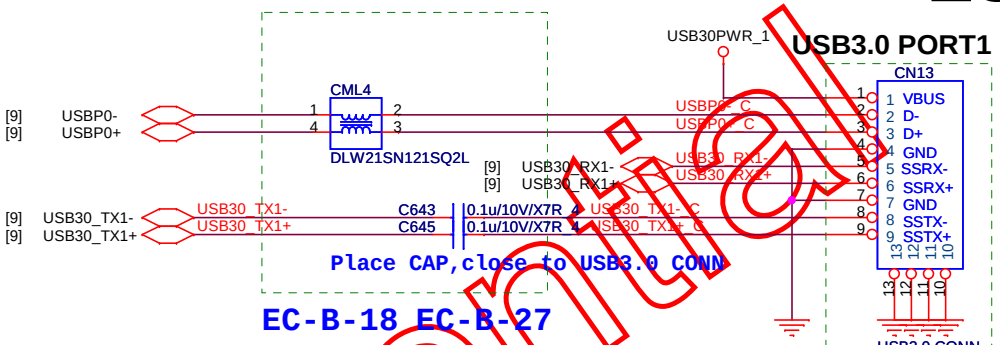
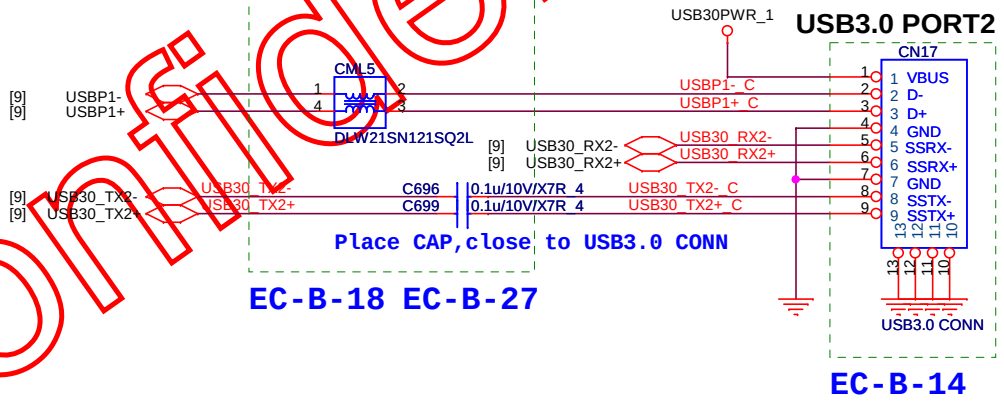
5V_S5 [11,32,37]

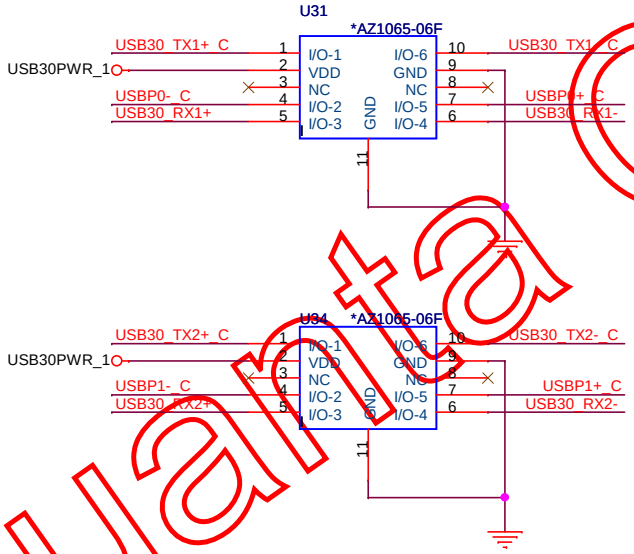
150 mils (Iout=3.5A)

High Actice









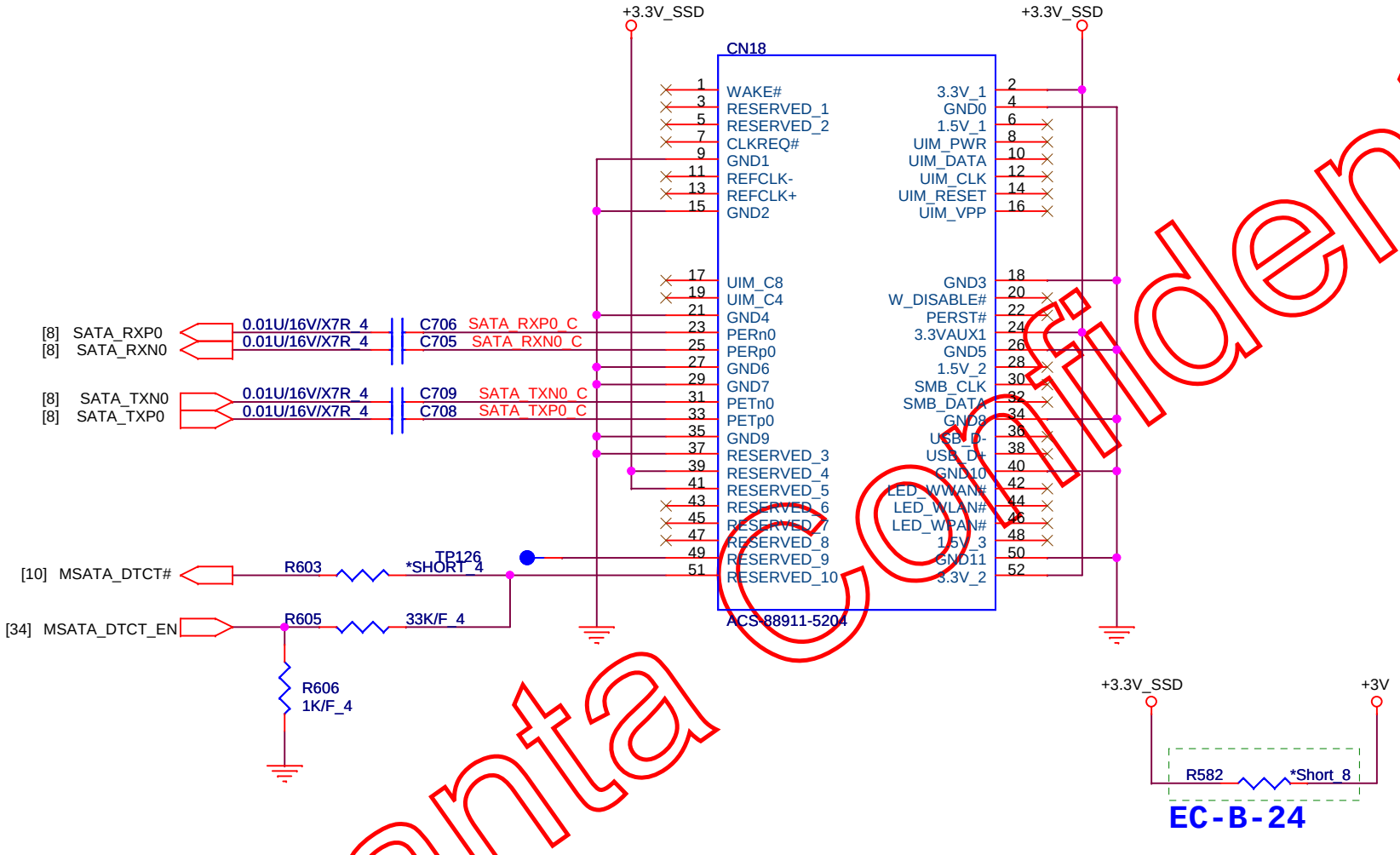
PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x2	2A
Date: Tuesday, December 20, 2011	Sheet 28 of 49	

SSD

[3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46] +3V



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI Card (SSD)	1A
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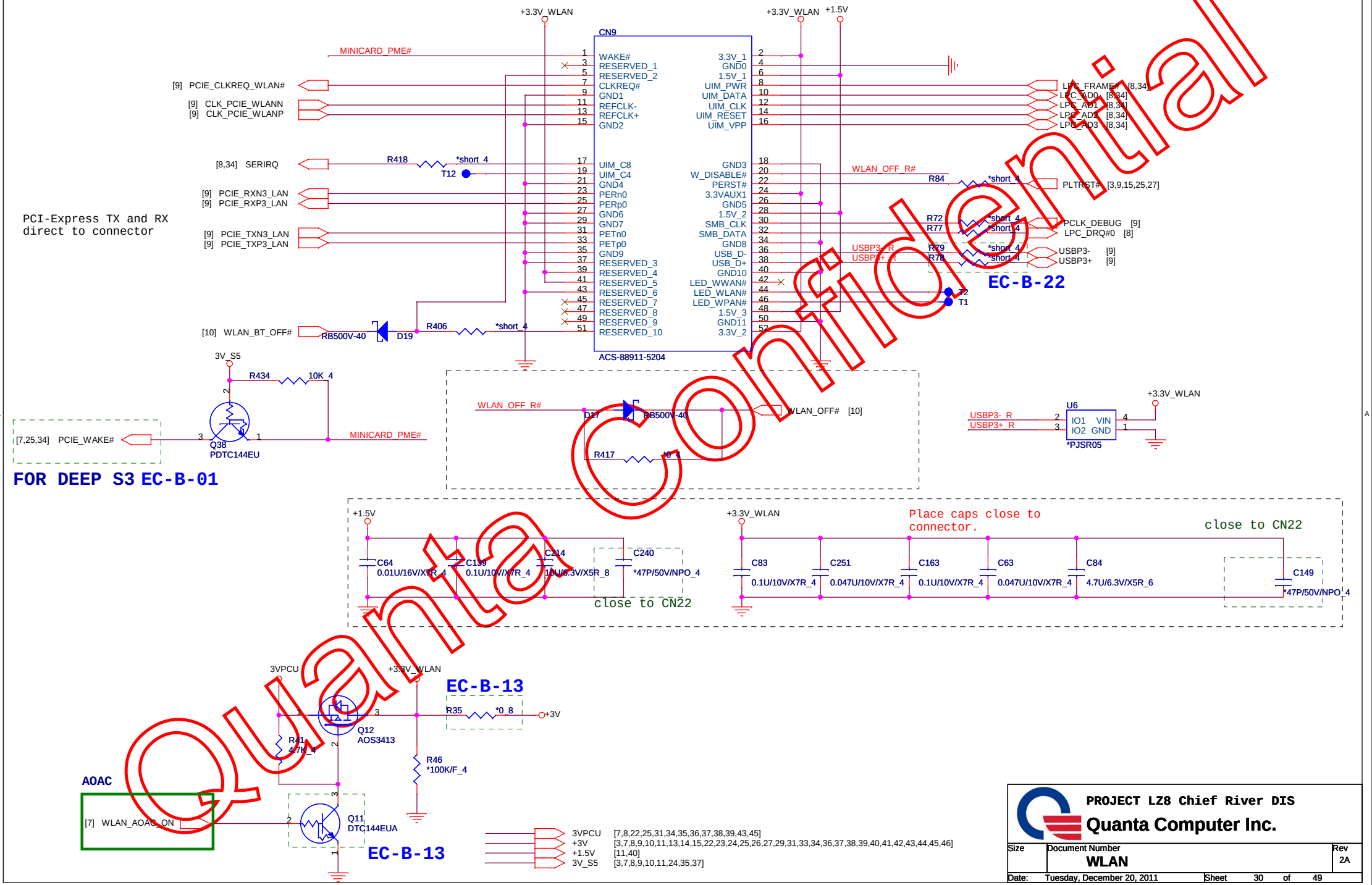
MiniCard WLAN connector



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	WLAN	2A

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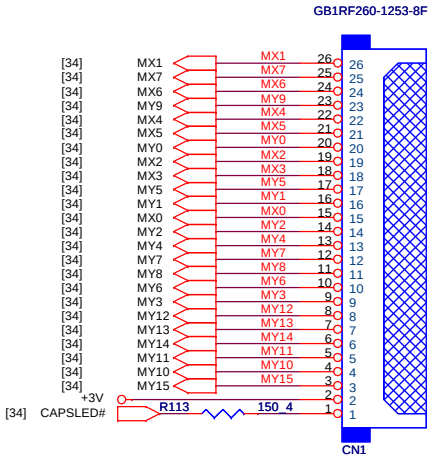
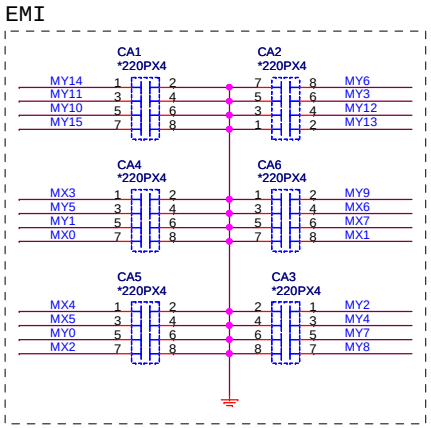
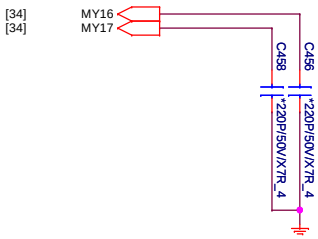
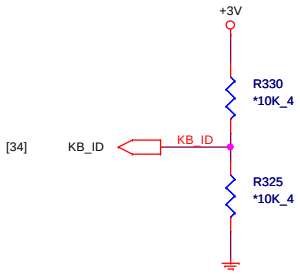
KEYBOARD

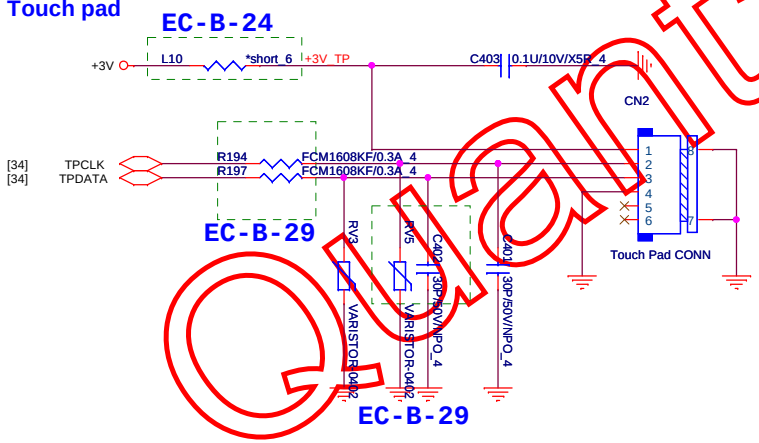




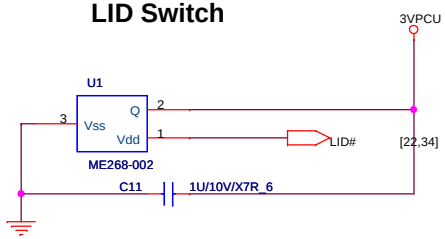




Touch pad



LID Switch



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Quanta Computer Inc.		
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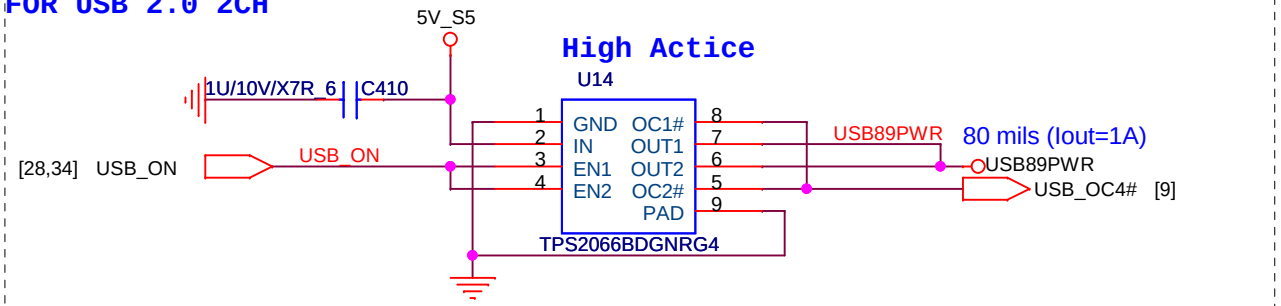
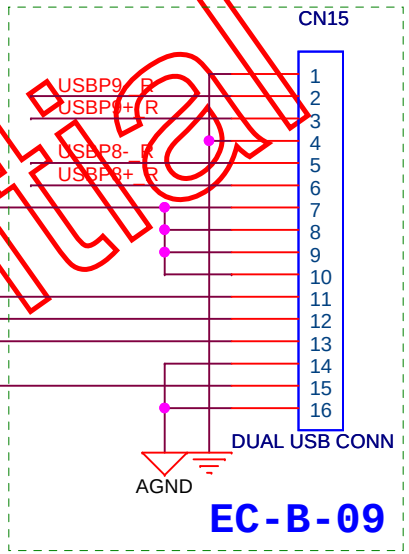
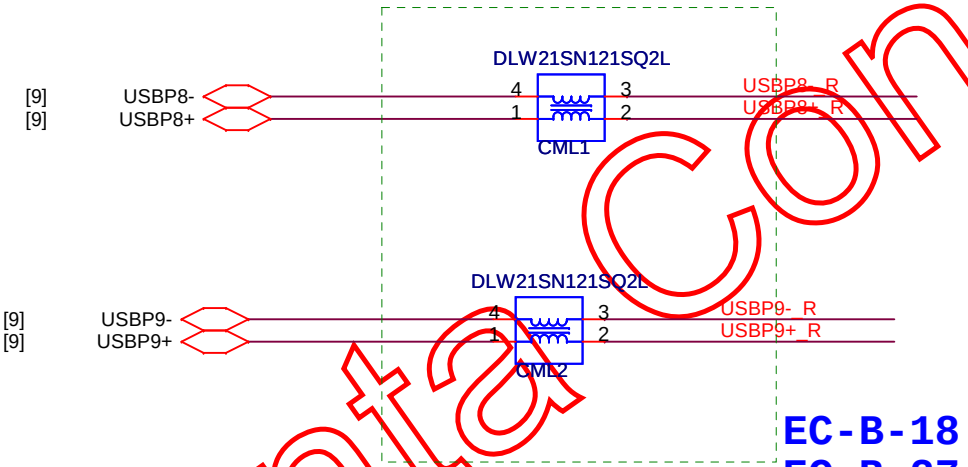
FOR USB 2.0 2CH



5V_S5 [11,28,37]





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Quanta Computer Inc.		
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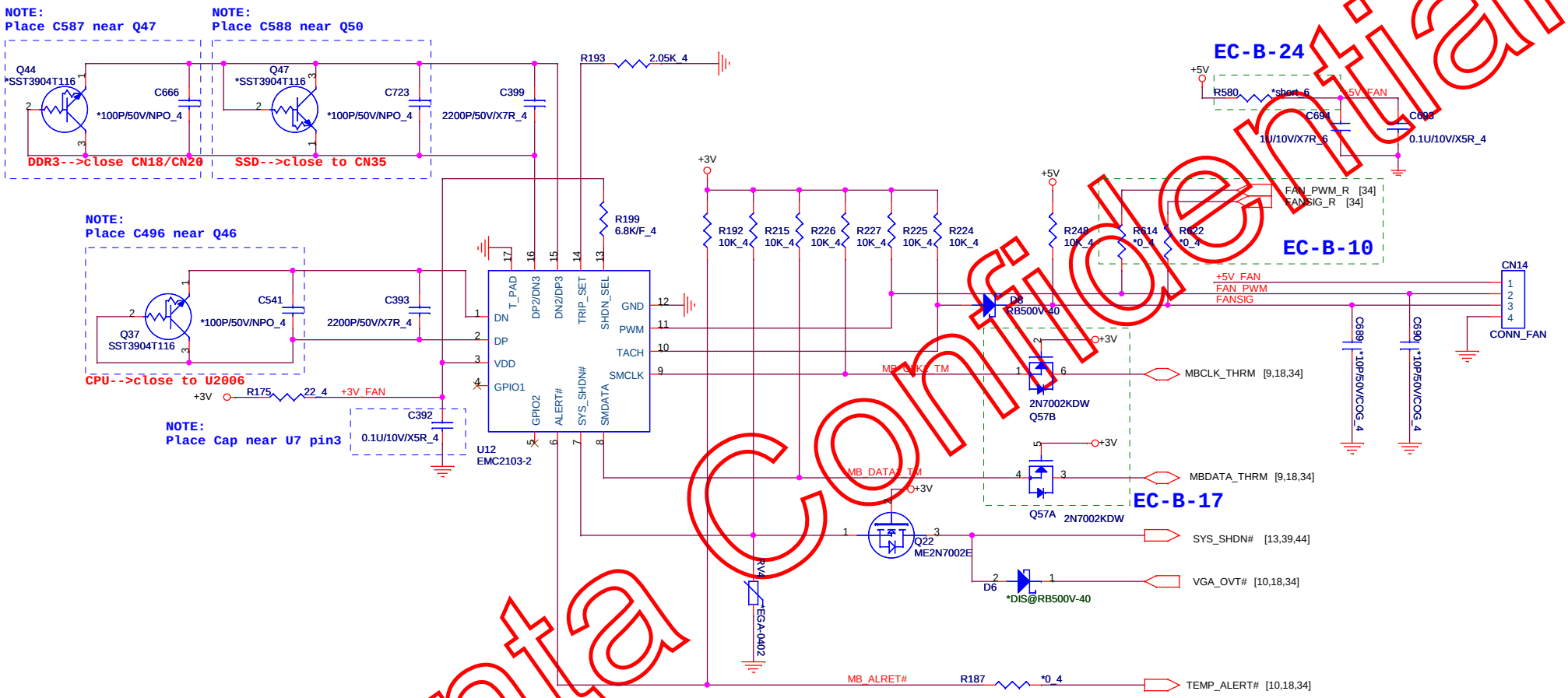
FAN CONTROL

[3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,34,36,37,38,39,40,41,42,43,44,45,46] +3V
[8,11,23,24,26,36,37,38] +5V



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal	2A

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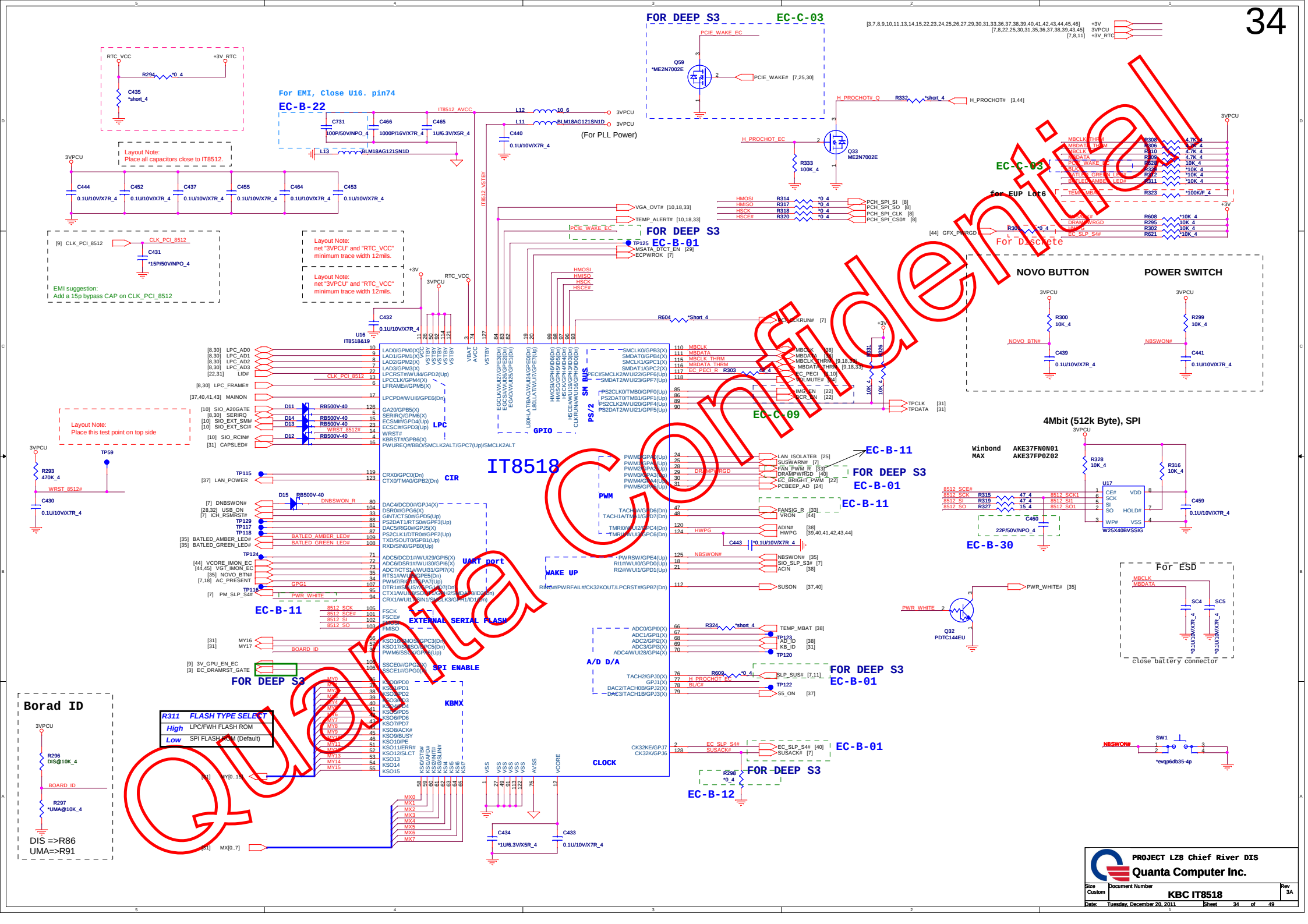
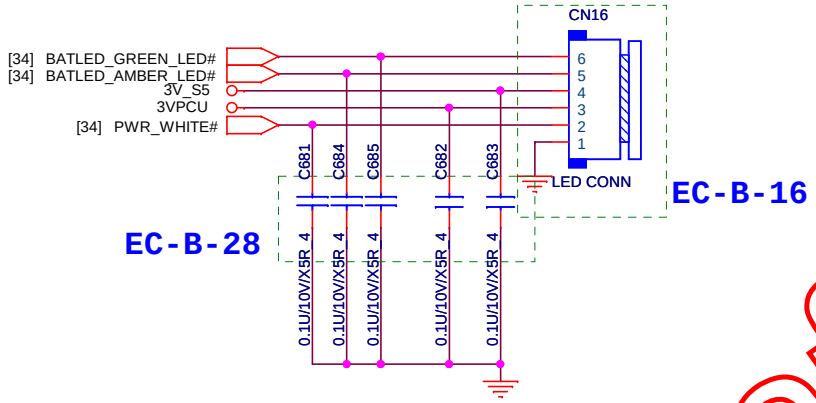
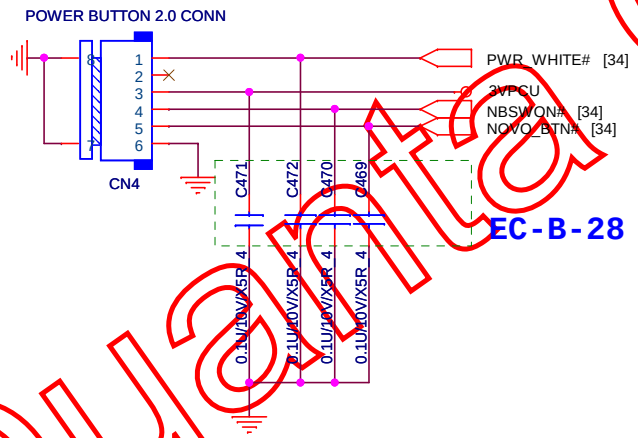


3VPCU [7,8,22,25,30,31,34,36,37,38,39,43,45]
3V_S5 [3,7,8,9,10,11,24,30,37]

LED Conn



POWER BUTTON/NOVO Button



PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	SW/LED/RFID_EEPROM	2A
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Hole for CPU support

HOLE13 *H-C181D181N
HOLE12 *H-TC217BIC142D142N
HOLE10 *H-TC236BIC142D142N
HOLE9 *H-C142D142N

MiniCard WWAN

HOLE14 H-TC217BIC142D102P2

MiniCard WLAN

HOLE11 H-TC217BIC142D102P2

SPAD3 *SPAD-LZ8-2
SPAD4 *SPAD-LZ8-3
HOLE15 *H-TBR315X350I178D98P2

Hole for GPU support

HOLE4 *H-C142D142N
HOLE5 *H-TC236BIC142D142N

Boundary Hole

HOLE8 *H-C276I146D106P2
HOLE2 *H-C276I146D106P2
HOLE1 *HG-C276I146D106P2-5
HOLE6 *HG-C276I146D106P2-5
HOLE7 *H-C86D86N

EMI

1.5V_SUS: C273, C256, C282, C270, C294, C210, C299 — 2200P/50V/X7R_4
VIN: C493, C707, C669 — 0.1U/50V/X7R_6

+3V: C67, C484, C317, C721, C482, C473, C668, C712 — 2200P/50V/X7R_4
VIN: C662, C722, C451 — 0.1U/50V/X7R_6

+5V: C34 — 1U/6.3V/X5R_4; C600, C35, C697, C646, C461 — 2200P/50V/X7R_4

Fro ESD

3VPCU [7,8,22,25,30,31,34,35,37,38,39,43,45]

+1.5V_CPU: SC2, SC3 — *0.1U/10V/X7R_4
VCC_GFX: SC7, SC6, SC9, SC8 — *0.1U/10V/X7R_4

VIN: C330 — *0.1U/10V/X7R_4 — VCC_CORE

Fro EMI

5VPCU: C319 — 1000P/50V/X7R_4; C13 — 1U/6.3V/X5R_4; C58 — 1U/6.3V/X5R_4

3VPCU: C729 — 100P/50V/NPO_4

For EMI, Close U16.PIN92

EC-B-22

+1.5V_CPU [3,5,40]
3VPCU [7,8,22,25,30,31,34,35,37,38,39,43,45]
VCC_GFX [5,44]
+3V [3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,37,38,39,40,41,42,43,44,45,46]
+5V [8,11,23,24,26,33,37,38]
1.5V_SUS [3,11,13,14,37,40,46]
5VPCU [11,22,37,39,40,41,42,43,44,45,46]
VIN [22,38,39,40,41,42,44,45]
VCC_CORE [5,6,44]
+1.05V [3,5,7,8,9,11,37,41,46]

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Quanta Computer Inc.

Size	Document Number	Rev
	Screw Hole/EMI	1A
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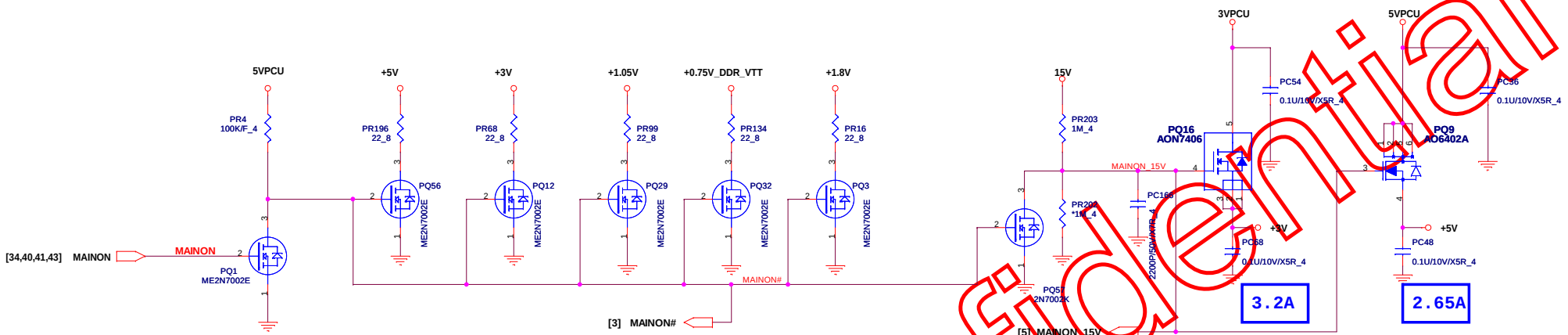
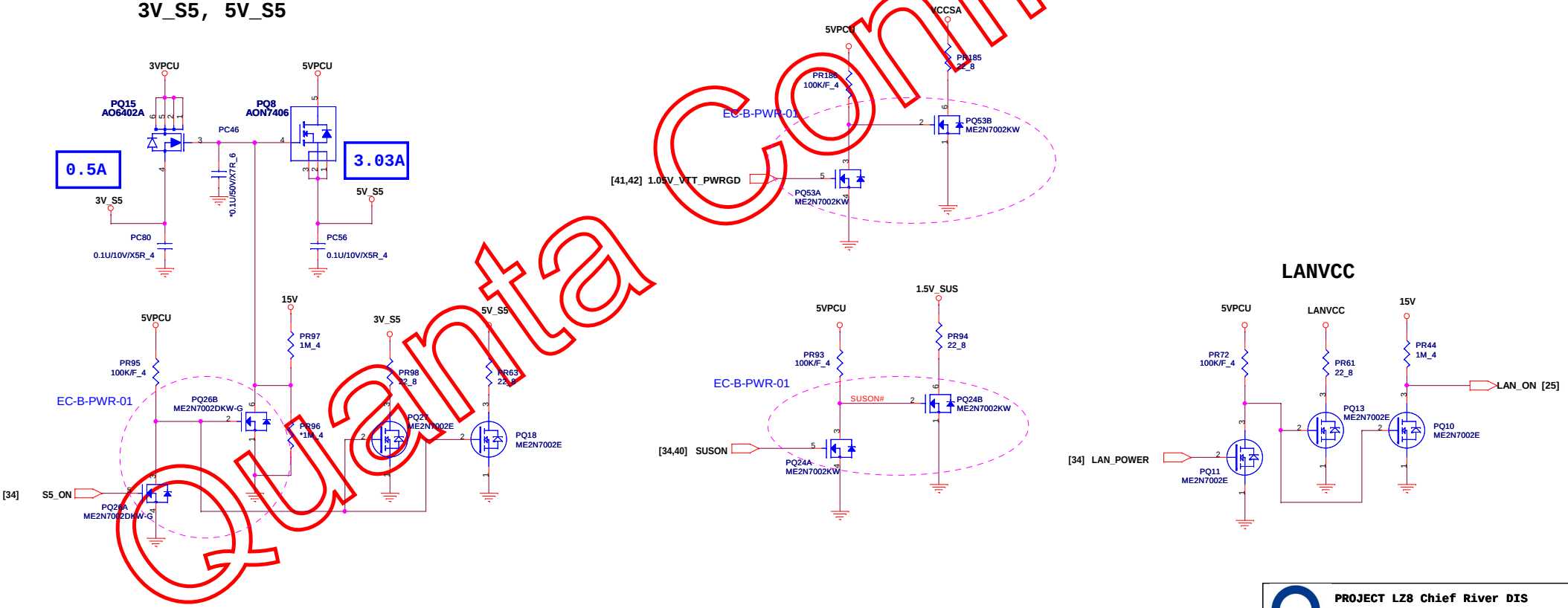
DISCHARGE

+3V, +5V,+1.5V



3V_S5, 5V_S5



LANVCC

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Quanta Computer Inc.		
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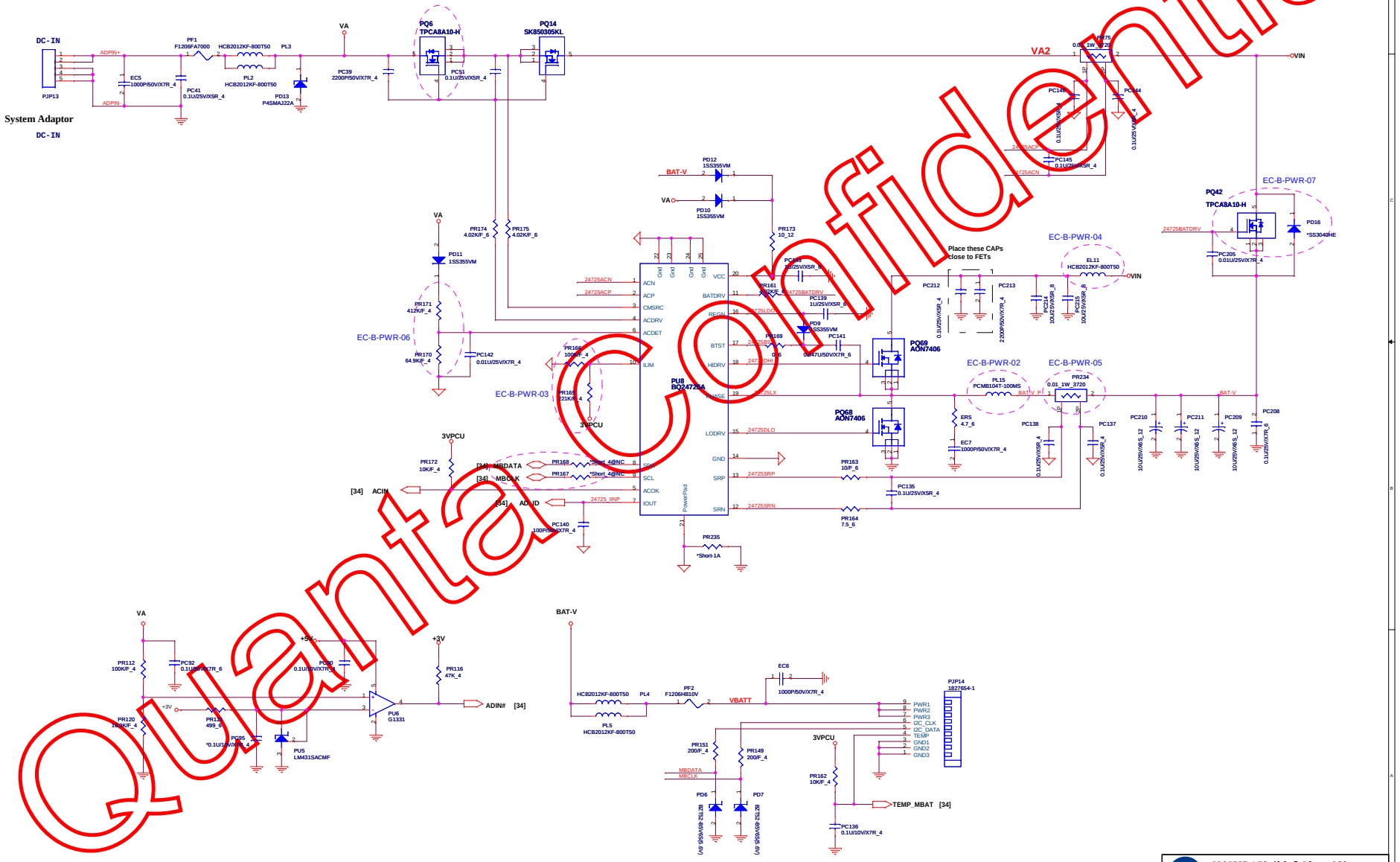

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER (BQ24725)	1A
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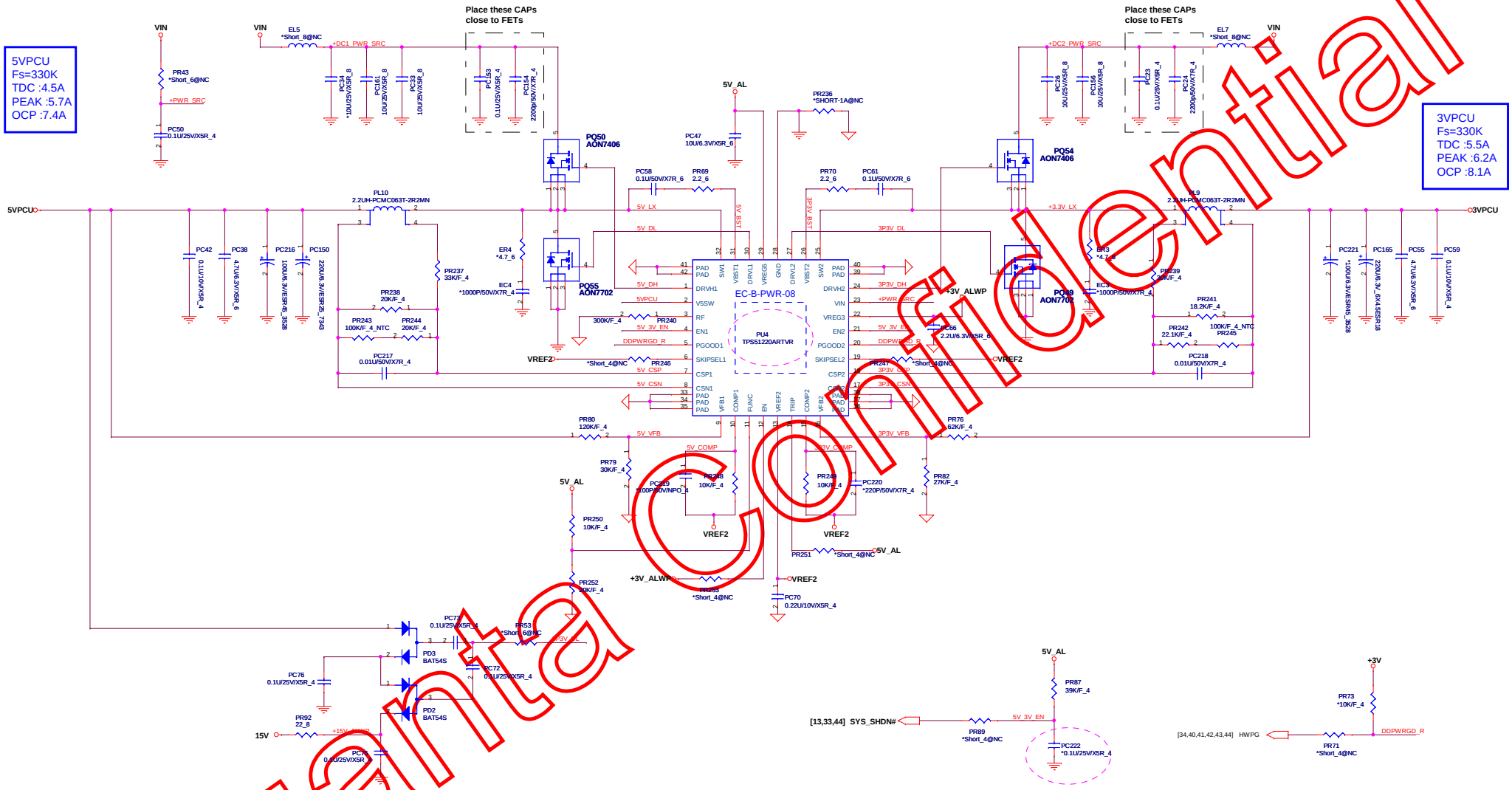

PROJECT Z Plus Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: 3V/5V (TPS51220ARTVR)	Rev: 1A
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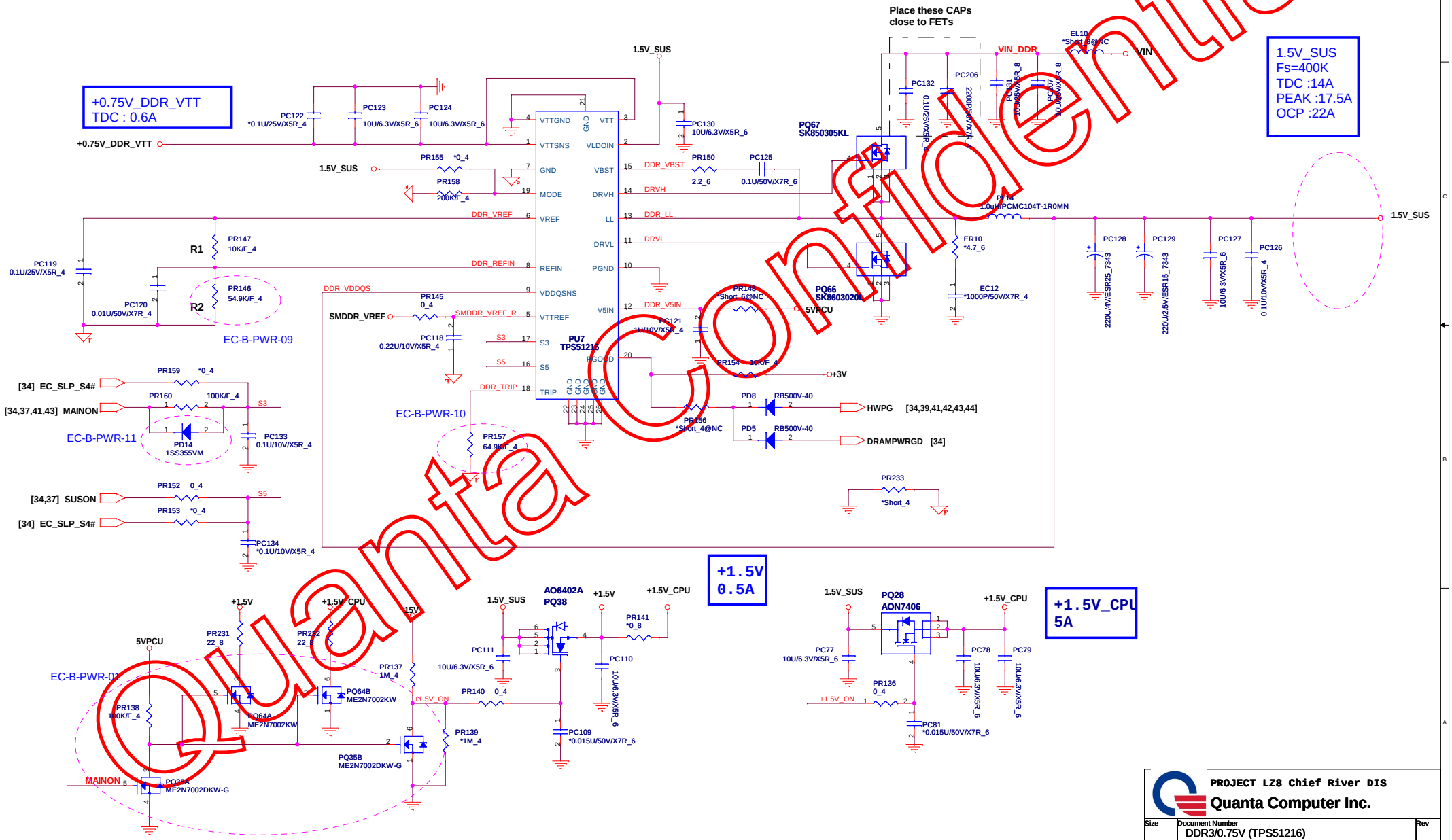

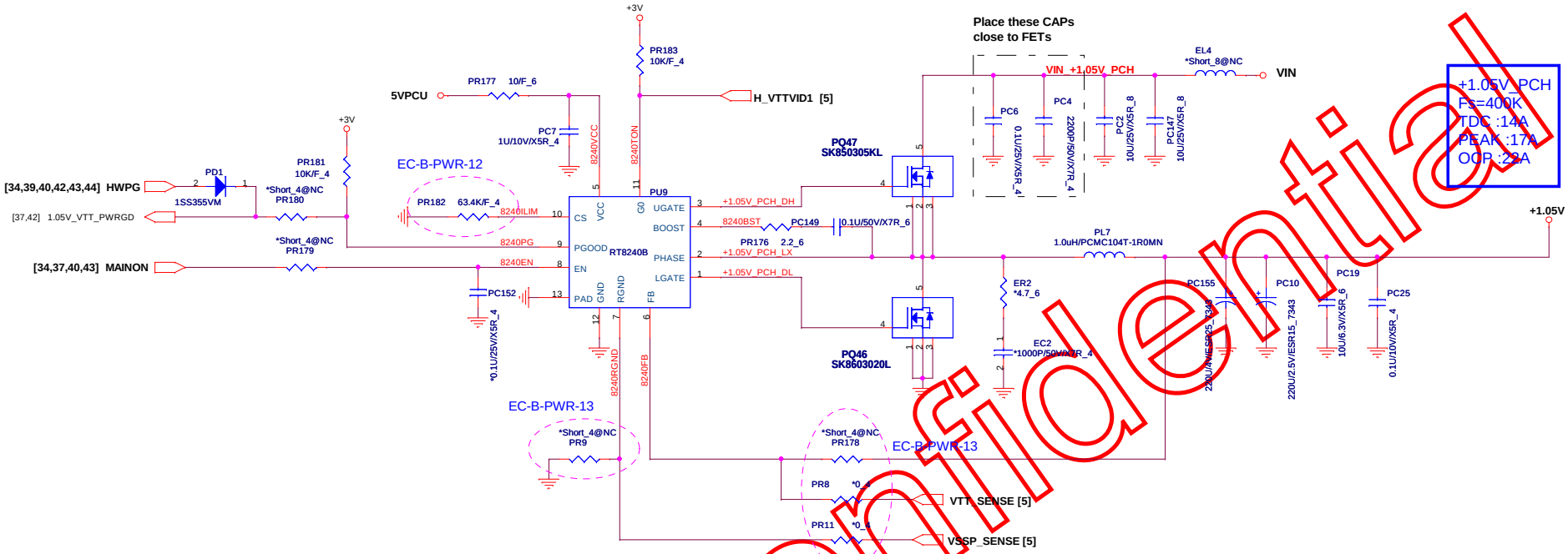

PROJECT LZ8 Chief River DIS			
Quanta Computer Inc.			
Size	Document Number		Rev
	+1.05V_VTT&+1.05V_PCH		
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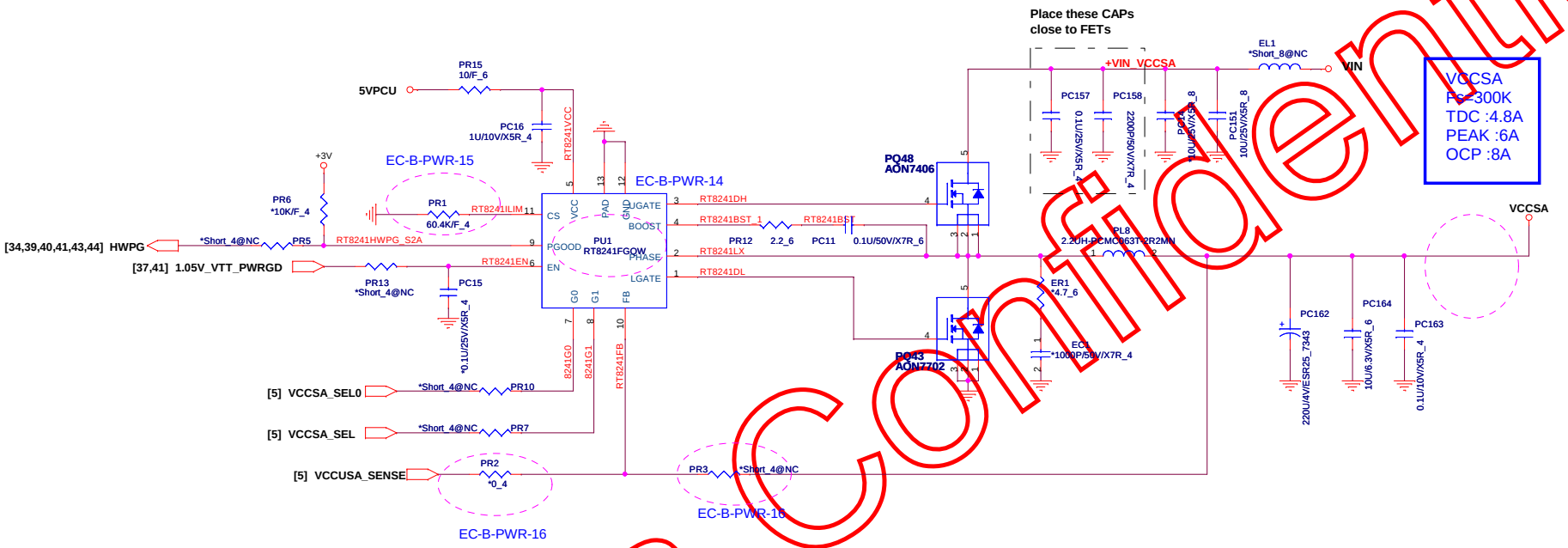

G0	G1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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	VCCSA (RT8241E)	

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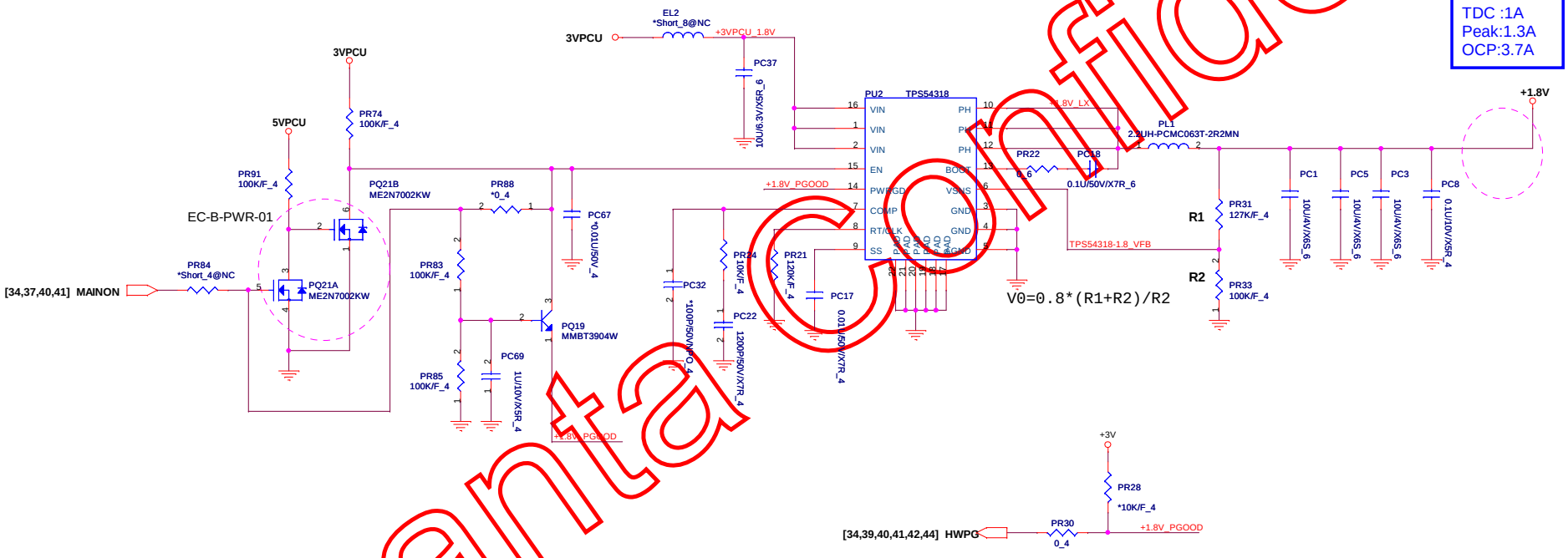
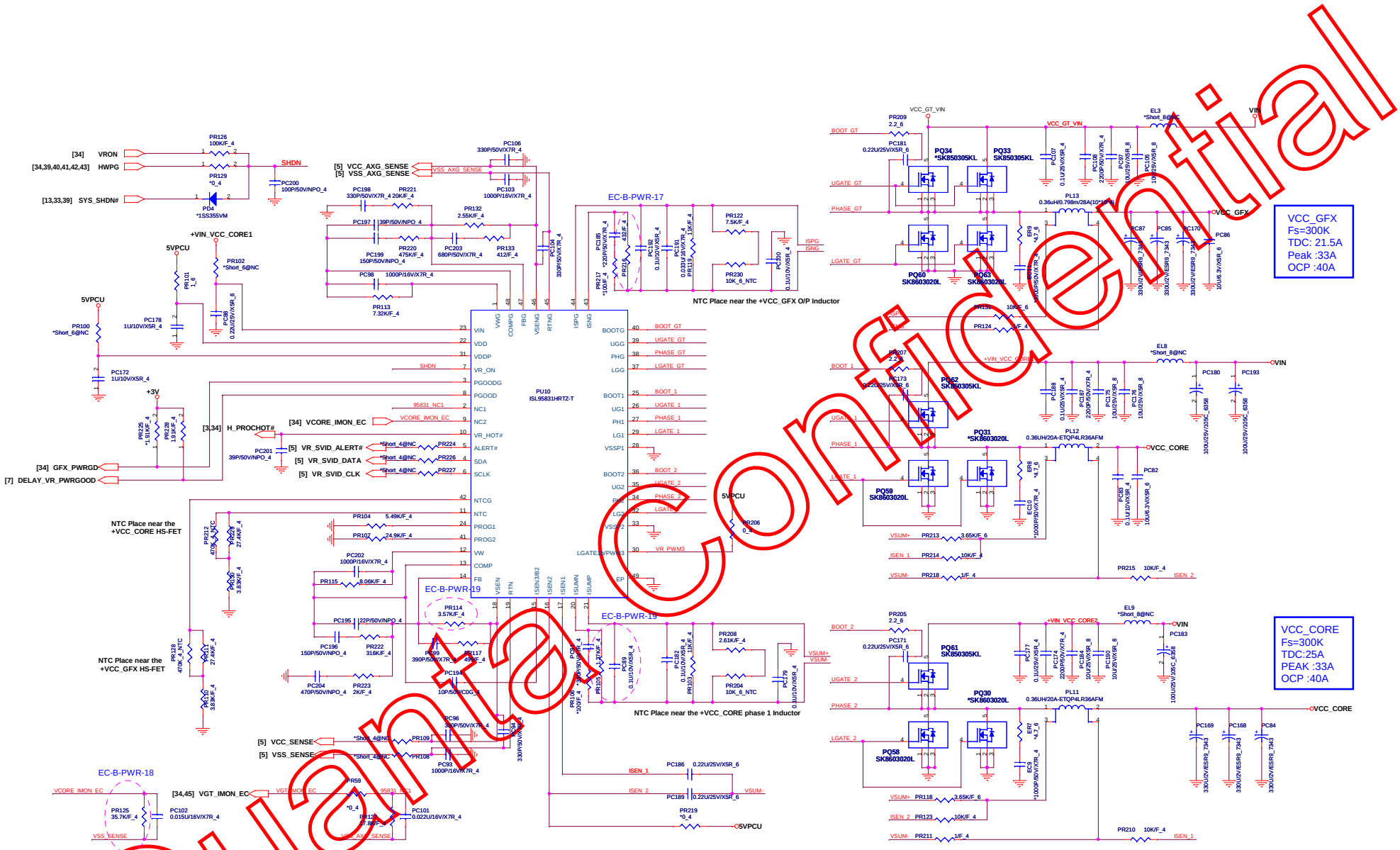


PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: 1.8V (TPS54318)	Rev
Date: Tuesday, December 20, 2011	Sheet 43 of 49	



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Size
Document Number CPU(ISL95831)IMVP2+1
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VID 1.2875V

VGPU_CORE
Fs=300k Hz
TDC:20A
Peak:25A
OCP:33A
Loadline=0mV/A

[18] dGPU_PCNT

PU3 TPS51728

EC-B-PWR-22

EC-B-PWR-21

EC-B-PWR-20

Parallel

Close to the VR side.

*SHORT-1A

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Quanta Computer Inc.

Size	Document Number	Rev
	DGPU Core (TPS51728)	1A

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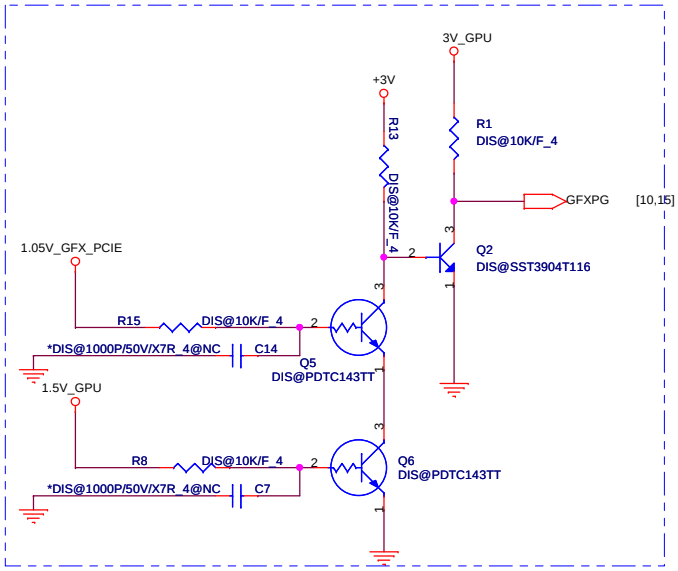

EC-B-PWR-23

6A

PQ41
DIS@AON7702

1.5V_SUS

1.5V_GPU

PC117 PC113 PC116 PC115 PC114

DIS@10U/6.3V/X5R_6

*0.1U/25V/X5R_4

1.5V_GPU

15V

PR144
DIS@22_8

PR142
DIS@1M_4

5VPCU

PR135
DIS@100K/F_4

PQ37
DIS@ME2N7002E

PR143
*Short_4@NC

PC112
DIS@8200P/50V/X7R_4

EC-B-PWR-01

PQ40B
DIS@ME2N7002DKW-G

[45] NVVDD_PG

PQ40A
DIS@ME2N7002DKW-G

EC-B-PWR-23

5A

PQ7
DIS@AON7702

+1.05V

1.05V_GFX_PCIE

PC44 PC45 PC31 PC35 PC20

DIS@10U/6.3V/X5R_6

*DIS@0.1U/25V/X5R_4

2A

PQ20
DIS@AO6402A

3V_GPU

3V_GPU [15,17,18]

PC64 PC65

*DIS@0.1U/25V/X5R_4

PR19
DIS@470K_4

PC30
DIS@8200P/50V/X7R_4

3V_GPU

1.05V_GFX_PCIE

15V

+3V

PR189
0_4

PR54
DIS@22_8

PR17
DIS@22_8

PR20
DIS@510k_4

PC71

PR90
*Short_4@NC

PC74

*2200P/50V/X7R_4

5VPCU

EC-B-PWR-01

PR18
DIS@100K/F_4

PQ17
DIS@ME2N7002E

PQ2A
DIS@ME2N7002DKW-G

PQ2B
DIS@ME2N7002DKW-G

[9,45] GFXON

GFXON

PQ4
DIS@ME2N7002E

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Quanta Computer Inc.		
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ECN	PG	DATE yy/mm/dd	PART	DESCRIPTION
EC-B-01	7,11,34	11/10/13	Add R607,R608,R621 and no ASM	Add DEEP S3 function
EC-B-02	7	11/10/13	R210	R210 chnage to short pad
EC-B-03	9	11/10/13	R610 no ASM,R611 ASM,	For DGPU power enable sequence
EC-B-04	10	11/10/13	R573 no ASM,R572 ASM	Change Board ID for SIV stage
EC-B-05	10,22	11/10/13	Q49,R613,C724,R612,Q48 add and ASM	Change CCD control by PCH GPIO35
EC-B-06	23	11/10/13	CN10	Change CN10 to correct footprint
EC-B-07	24	11/10/13		Change Audio detect schematic
EC-B-08	25	11/10/13	CN8	Change CN8 to correct footprint
EC-B-09	32	11/10/13	CN15	Change CN25 Pin define
EC-B-10	33	11/10/13	Add R614,R622 no ASM	Add EC detect Fan speed schematic
EC-B-11	34	11/10/13	DELR321	Change EC pin define,PIN94 connect to PWR_WHITE,PIN28 connect to FAN_PWM_R,PIN47 connect to FANSIG_R
EC-B-12	34	11/10/13	R298 no ASM	EC can output CLOCK by itself
EC-B-13	30	11/10/13	R35 no ASM,Q11ASM	input AOAC function
EC-B-14	28	11/10/13	CN13,CN17	Change CN13,CN17 to correct footprint
EC-B-15	28	11/10/13	add Q51,R623 no ASM	Add DEEP S3 function
EC-B-16	35	11/10/13	CN16	Change CN16 footprint for ME request
EC-B-17	9,18,22 23,33	11/10/14	Q30,Q31,Q26,Q27,Q34,Q35,Q3,Q4, Q41,Q42,Q23,Q24 DEL Add Q52,Q53,Q54,Q55,Q56,Q57 and ASM	Change MOS to Dual MOS
EC-B-18	21	11/10/19	Add Q58	For PS8622 flash ROM by EC ROM
EC-B-19	05	11/10/19	Add C727	Add a 10UF CAP for INTEL suggestion
EC-B-20	21	11/10/19	L14,L15,L16	Change footprint to 0603
EC-B-21	27	11/10/20	CN3	Change footprint for ME request
EC-B-22	36	11/10/24	Add C729,C730,C731	For EMI request
EC-B-23	3,7,11	11/10/24		Change LVDS singal by PCH provide
EC-B-24	7,24,25 26,27,29 30,31,33	11/10/24	R602,R322,R274,R305,R582,R580, L10,R129,R88,R87,R99,R79,R78, L22,L24	Change to short PAd
EC-B-25	8	11/10/24	BT1	Change BT1 footprint
EC-B-26	25	11/10/24	CN8	CN8 PIN4,5,7,8 connect to GND
EC-B-27	11,15	11/10/24	CML1,CML2,CML4,CML5 ASM R505,R502,R560,R563,R232,R233 R234,R235,C486,C488,C490,C497	for EMI request
EC-B-28	35	11/10/25	C472, C471, C470,C469,C681, C682 C683, C684,C685 ASM 0.1U	for EMI request
EC-B-29	35	11/10/25	RV5,C402 ASM 30P R194,R197 change to Bead	for EMI request
EC-B-30	35	11/10/26	C460 ASM 22P	for EMI request

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Quanta Computer Inc.

Size	Document Number	Rev
	Change List for B	2A

Date: Friday, December 09, 2011 Sheet 47 of 49

ECN NO	PG	DATE yy/mm/dd	PART	DESCRIPTION
EC-C-01	27	11/12/05	R277 ASM	Change Card reader to normal mode for pre load image
EC-C-02	10	11/12/05	R526 ASM,R527 no ASM,R573 ASM, R572 no ASM	Chaneg Board ID
EC-C-03	34	11/12/05	Add Q59 no ASM, and R628 ASM	For Deep S3
EC-C-04	22	11/12/05	Add Q58 and ASM	Chaneg to Dual MOS
EC-C-05	28	11/12/05	C528 change to raiting to 50V	for China 家電下鄉
EC-C-06	22	11/12/05	Add R629	For PWM control by EC
EC-C-07	11	11/12/05	Change R623 connect to 5VPCU	For Deep S3
EC-C-08	3,6,13,14	11/12/05	Add DDR M3 solution	DDR M3 solution for Deep S3
EC-C-09	22,34	11/12/05	Add R634,R635	Add color engine/dynamtic control function
EC-C-10	9	11/12/10	DEL RP7	Connect VGA CLK to PCH directly
EC-C-11	13,14	11/12/10	ADD R636,R637	to differentiate between M1 and M3 solution
EC-C-12	24	11/12/14	CN6	Change CN6 footprint for follow PDC suggestion
EC-C-13	24	11/12/14	C486,C488,C490,C497	Change to 680P for Vendor suggestion

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Quanta Computer Inc.

Size	Document Number	Rev
	Change List for C	3A

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ECN NO.	PG	DATE yy/mm/dd	PART	DESCRIPTION
EC-B-PWR-01	37, 40, 43, 46	11/10/31	PQ26, PQ24, PQ53, PQ35, PQ64, PQ21, PQ2, PQ40	Change to dual 2N7002
EC-B-PWR-02	38	11/10/31	PL15	Change PL15 to 10u H, size 10*10
EC-B-PWR-03	38	11/10/31	PR165, PR166	Change charger ILIM resistors
EC-B-PWR-04	38	11/10/31	EL11	Add EL11
EC-B-PWR-05	38	11/10/31	PR234	Change Charger resistor
EC-B-PWR-06	38	11/10/31	PR170, PR171	Change charger ACDET res
EC-B-PWR-07	38	11/10/31	PQ42	Change MOSFET with Schottky
EC-B-PWR-08	39	11/10/31	PU4 and so on	Change 3V/5V IC and schematic
EC-B-PWR-09	40	11/10/31	PR146	Change voltage setting resistor
EC-B-PWR-10	40	11/10/31	PR157	Change 1.5V_SUS OCP resistor
EC-B-PWR-11	40	11/10/31	PD14	Add PD14 to improve sequence
EC-B-PWR-12	41	11/10/31	PR182	Change 1.05V OCP resistor
EC-B-PWR-13	41	11/10/31	PR8, PR9, PR11, PR178	Improve 1.05V feedback
EC-B-PWR-14	42	11/10/31	PU1	Change VCCSA IC to AL008241003
EC-B-PWR-15	42	11/10/31	PR1	Change VCCSA OCP resistor
EC-B-PWR-16	42	11/10/31	PR2, PR3	Improve VCCSA feedback
EC-B-PWR-17	44	11/10/31	PR216	Change GFXcore OCP resistor
EC-B-PWR-18	44	11/10/31	PR125	Change VCC_core IMON resistor
EC-B-PWR-19	44	11/10/31	PC89, PR114, PR105	Change VCC_core OCP and Loadline
EC-B-PWR-20	45	11/10/31	PR60	Change DGPU IMON resistor
EC-B-PWR-21	45	11/10/31	PR26, PR27, PR14, PR58	Change DGPU OCP resistors
EC-B-PWR-22	45	11/10/31	PC52, PC53, PR41	Improve function
EC-B-PWR-23	46	11/10/31	PQ7, PQ41	Improve function

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	Power Change List	1A

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