16924 Woody/Buzz_UMA KBL

Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

Count

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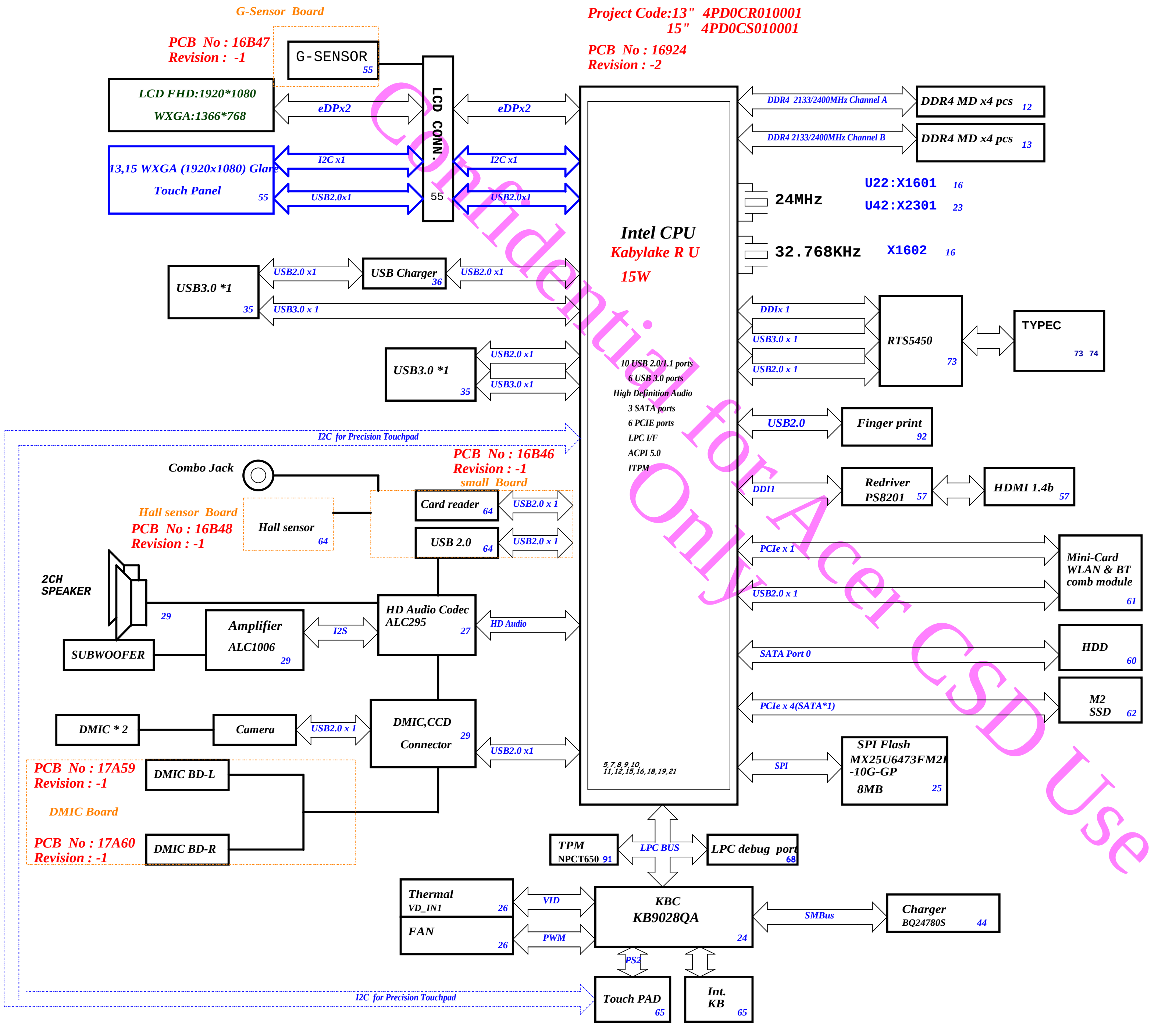
Title: *Cover Page*

Size: A3 | Document Number: Woody/Buzz_KBL | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 1 of 106



CHARGER BQ24780S		44
INPUTS	OUTPUTS	
AD+ BT+	19V_DCBATOUT	
SYSTEM DC/DC RT6228		45
INPUTS	OUTPUTS	
19V_DCBATOUT	5V_AUX_S5 5V_S5	
SYSTEM DC/DC RT6226		45
INPUTS	OUTPUTS	
19V_DCBATOUT	3D3V_AUX_S5 3D3V_S5	
CPU DC/DC RT3602		46-47
INPUTS	OUTPUTS	
19V_DCBATOUT	1V_CPU_CORE	
CPU DC/DC AOZ5049		48
INPUTS	OUTPUTS	
19V_DCBATOUT	1V_VCCGT	
CPU DC/DC RT9610B		50
INPUTS	OUTPUTS	
5V_S5	1V_VCCSA	
CPU DC/DC G5388K1		51 52
INPUTS	OUTPUTS	
5V_S5	PWR_VDDQ	
3D3V_S5	PWR_1D0V	
SYSTEM DC/DC 9661-25ADJ		53
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
SYSTEM DC/DC S-1339D15		53
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
SYSTEM Load switch TPS22976		40
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
5V_S5	5V_S0	
1D0V_S5	1V_VCCST	
1D8V_S5	1D8V_S0	
SYSTEM Load switch APE8939		40
INPUTS	OUTPUTS	
1D0V_S5	1V_VCCIO	

Count

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Title: Block Diagram

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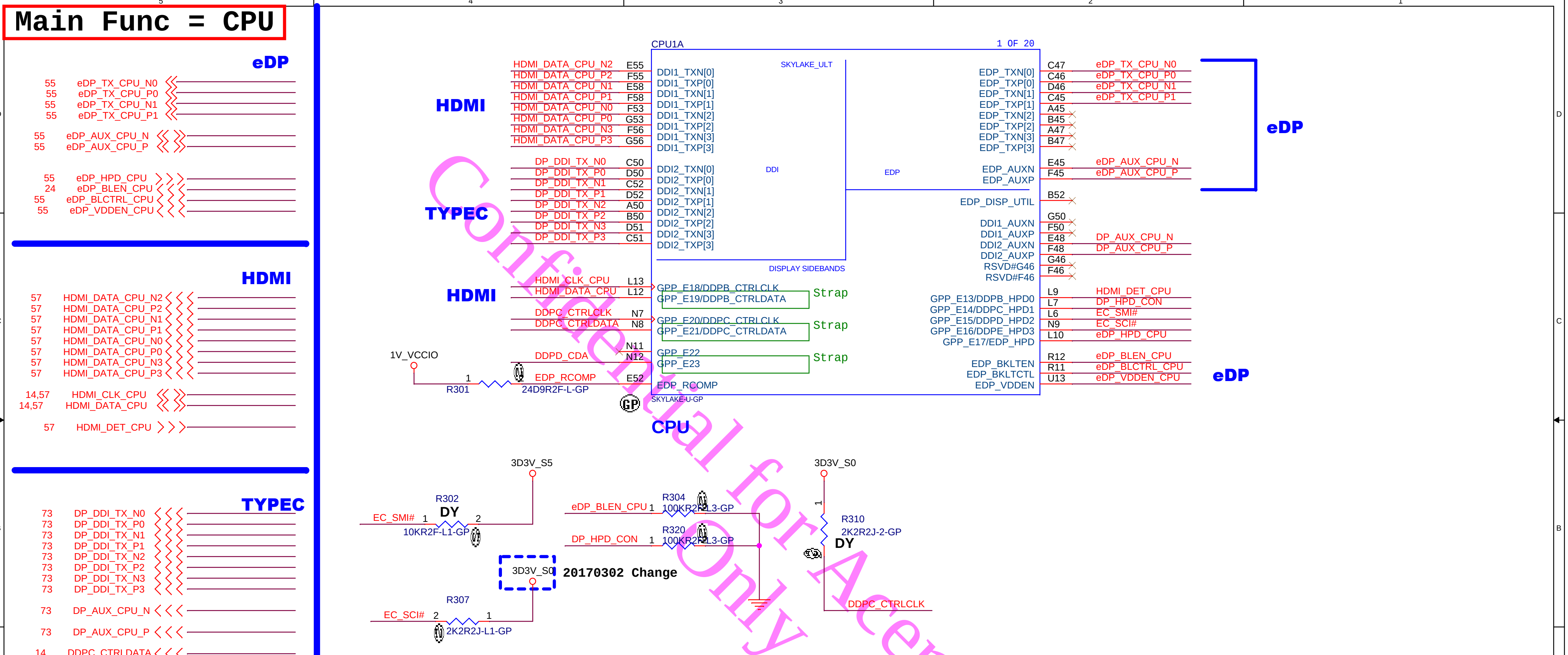

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

Count

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Title: CPU_(DISPLAY)

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Main Func = CPU

DDR4 ball type:NON Interleaved Type

Count

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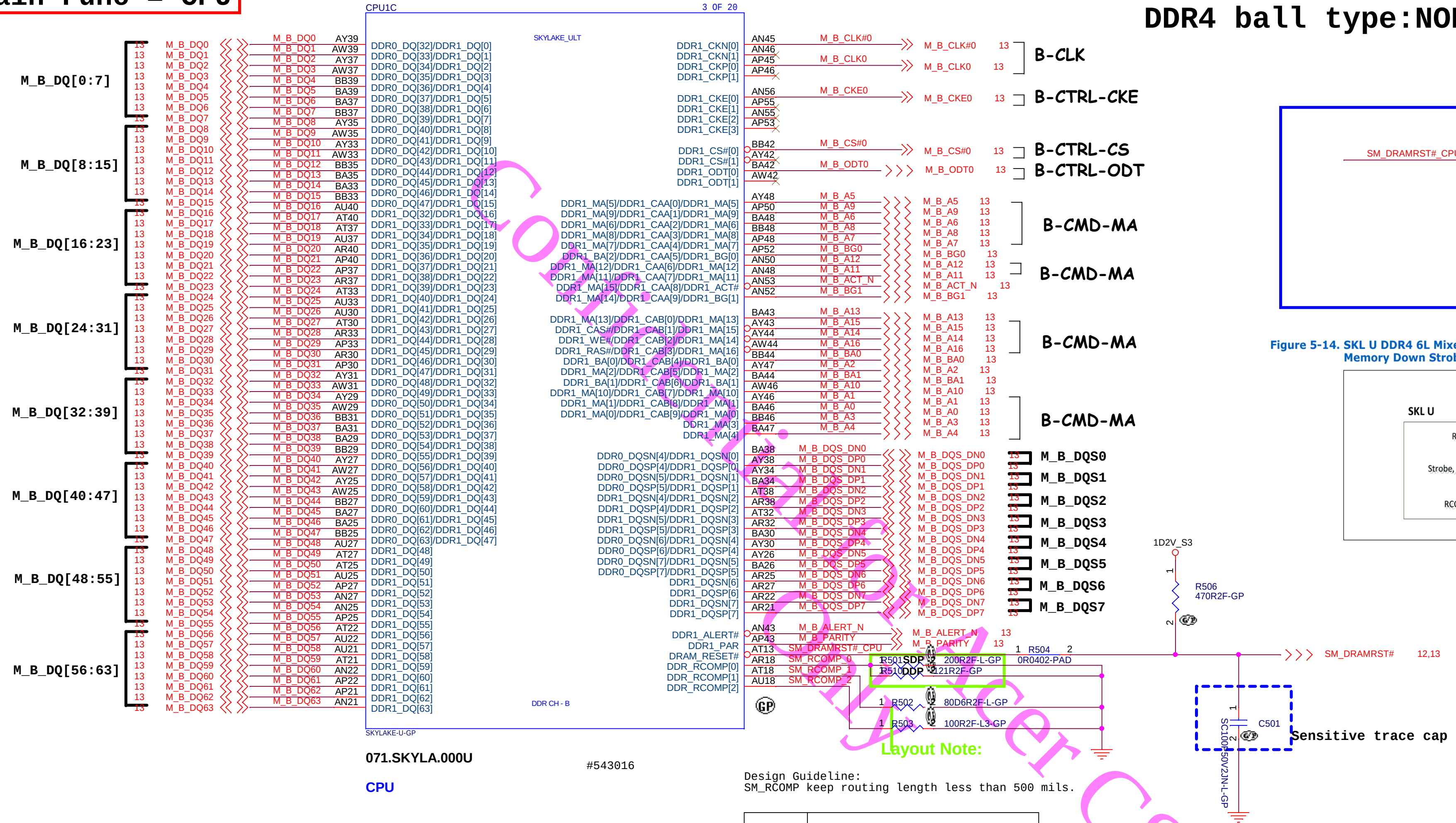
Title	CPU_(DDR)
Size: Custom	Document Number: Woody/Buzz_KBL
Rev	-2
Date:	Tuesday, July 25, 2017
Sheet	4 of 106

Main Func = CPU

DDR4 ball type:NON Interleaved Type



071.SKYLA.000U

#543016

CPU

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

	R501
DDP	121ohm(64.12105.6DL)
SDP	200ohm(64.20005.6DL)

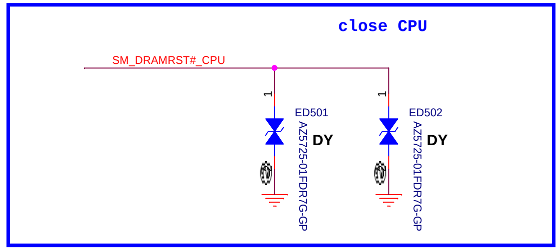
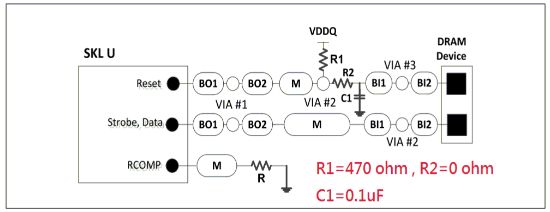


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology Memory Down Strobe/Data/Reset/RCOMP Signal Topologies



Count

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Title	CPU_(DDR)
Size Custom	Document Number Woody/Buzz_KBL — Rev -2
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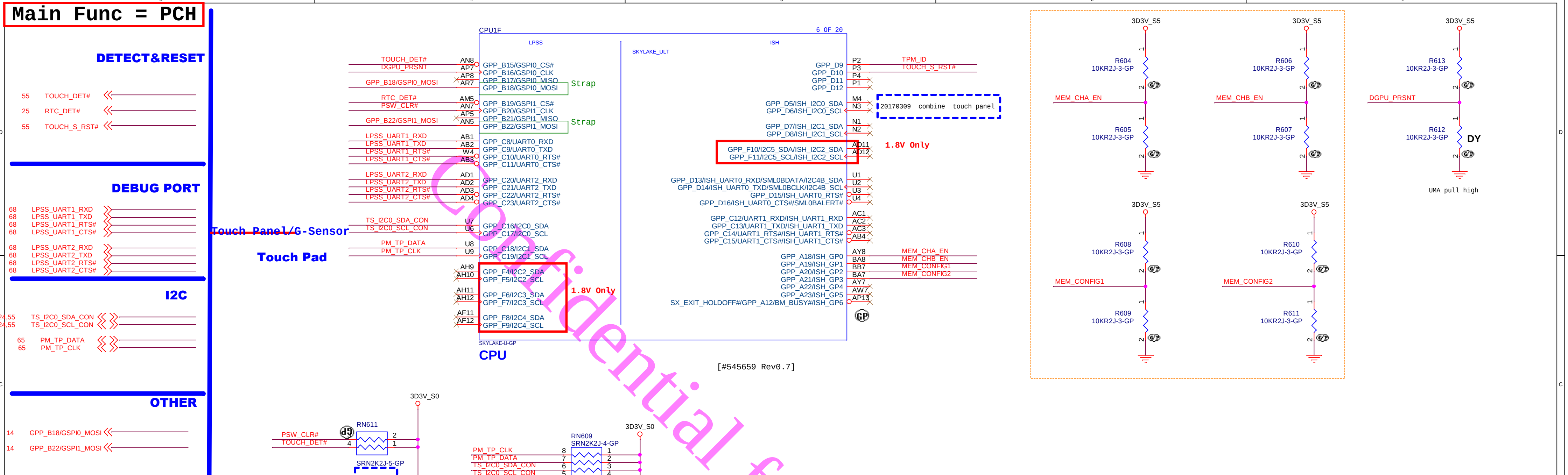
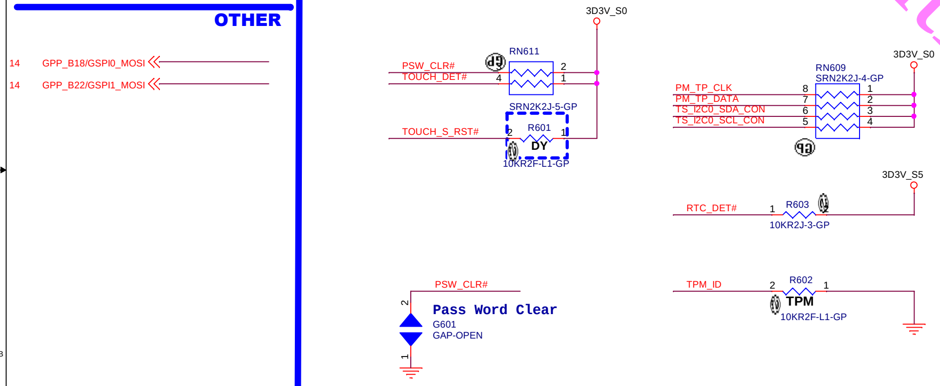
Main Func = PCH





Vendor	GONFIG4 (GPP_A19)	CONFIG3 (GPP_A18)	CONFIG2 (GPP_A21)	CONFIG1 (GPP_A20)	Mfr.PN	Wistron PN	Capacity	DDP/SDP
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	KN.8GB0G.049	8Gb	SDP
MICRON	0	0	0	1	MT40A512M16JY-083E:B	KN.8GB04.013	8Gb	SDP
SAMSUNG	0	0	1	0	K4A8G165WB-BCRC	KN.8GB0B.048	8Gb	SDP
HYNIX	0	0	1	1	H5AN4G6NAFR-TF	KN.0040G.015	4Gb	SDP
HYNIX	0	1	0	0	H5AN4G6NAFR-UHC	KN.0040G.016	4Gb	SDP
MICRON	0	1	0	1	MT40A256M16GE-083E:B	KN.00404.010	4Gb	SDP
SAMSUNG	0	1	1	0	K4A4G165WE-BCRC	KN.0040B.014	4Gb	SDP
HYNIX	0	1	1	1	H5ANAG6NAMR-UHC	KN.0160G.010	16Gb	DDP
MICRON	1	0	0	0	MT40A1G16WBU-083E:B	KN.01604.001	16Gb	DDP

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

Count

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Title: CPU_(LPSS/ISH)

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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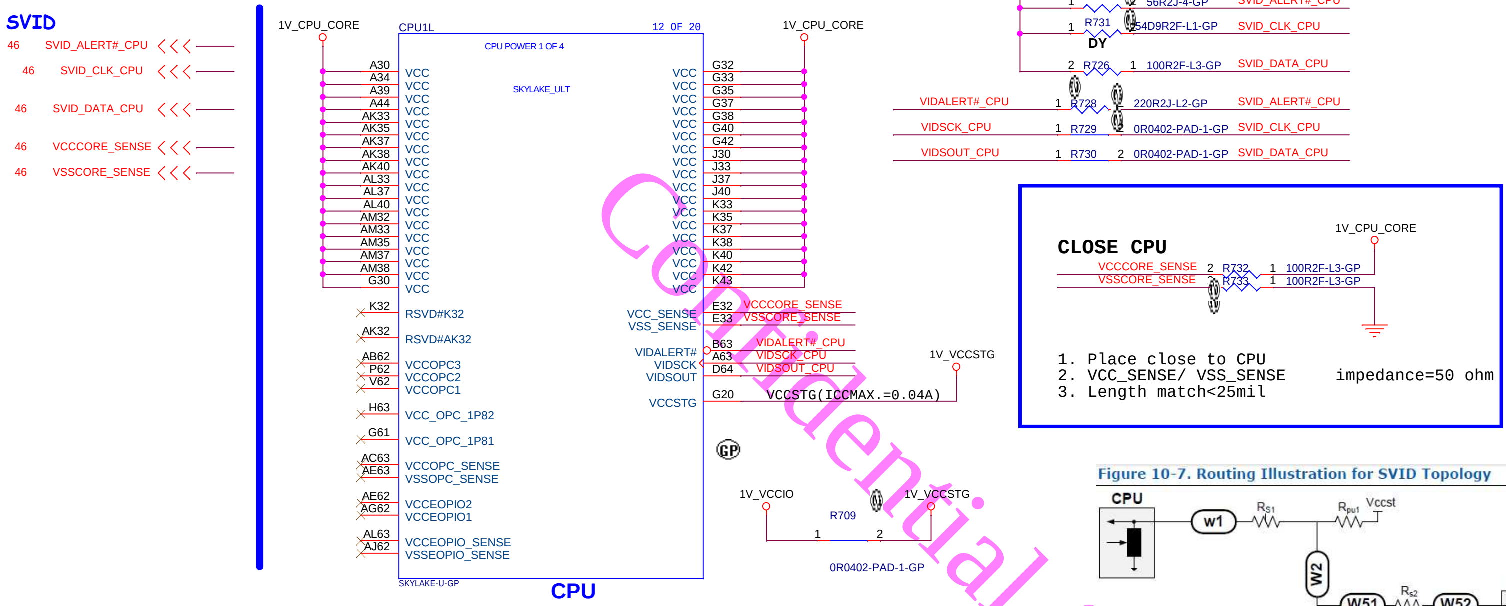
Main Func = CPU



Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology

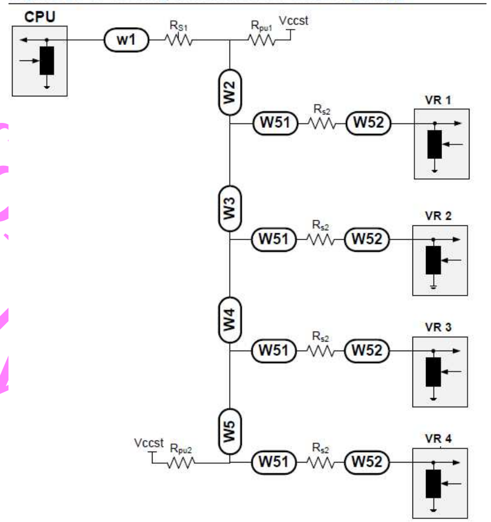


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Count

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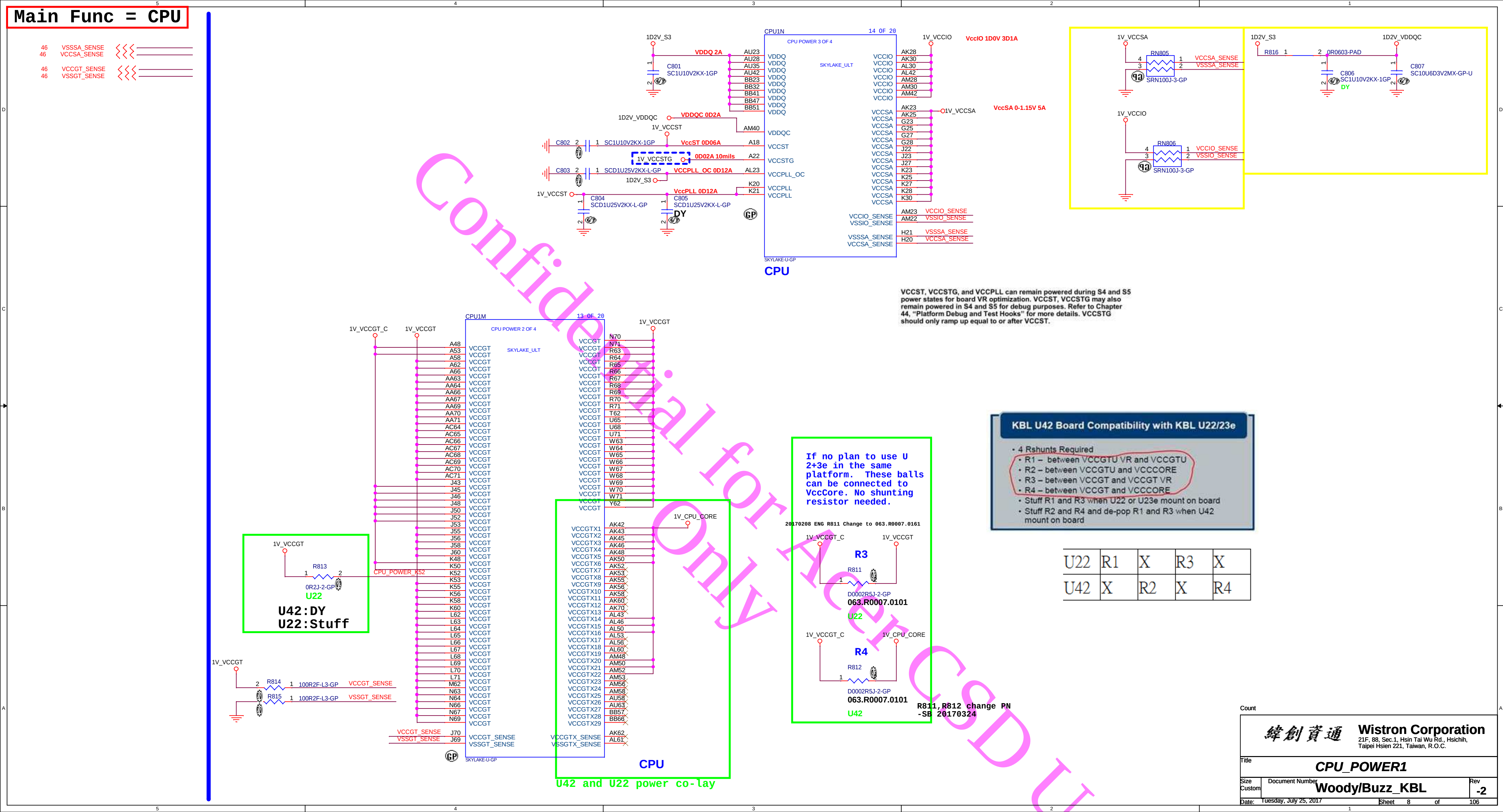
Title	CPU_POWER1	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 7 of 106	



U22	R1	X	R3	X
U42	X	R2	X	R4

Count

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Title: CPU_POWER1

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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Blanking

Count

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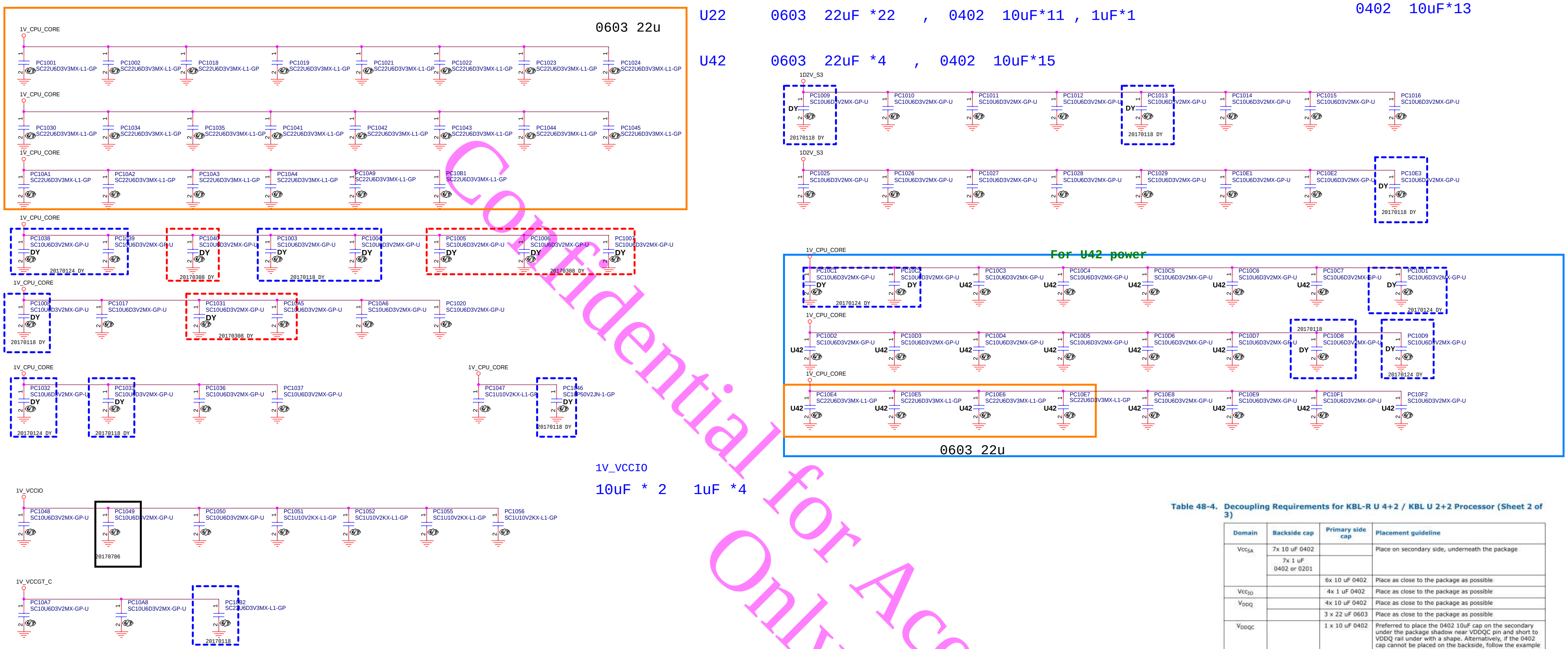
Title	***Reserved***	
Size A4	Document Number **Woody/Buzz_KBL**	Rev **-2**
Date: Tuesday, July 25, 2017	Sheet 9 of 106	

Main Func = CPU



Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)		Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

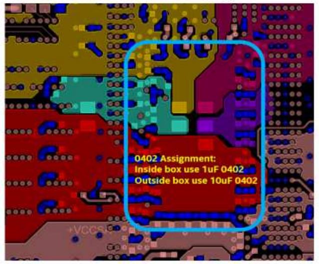
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/Vcc_{GT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible. Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{ST} closest adjacent layer over any power net other than ground. For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.
Vcc_{PLL_OC}		1x 1 uF 0201	
Vcc_{ST}		1x 1 uF 0402	

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.

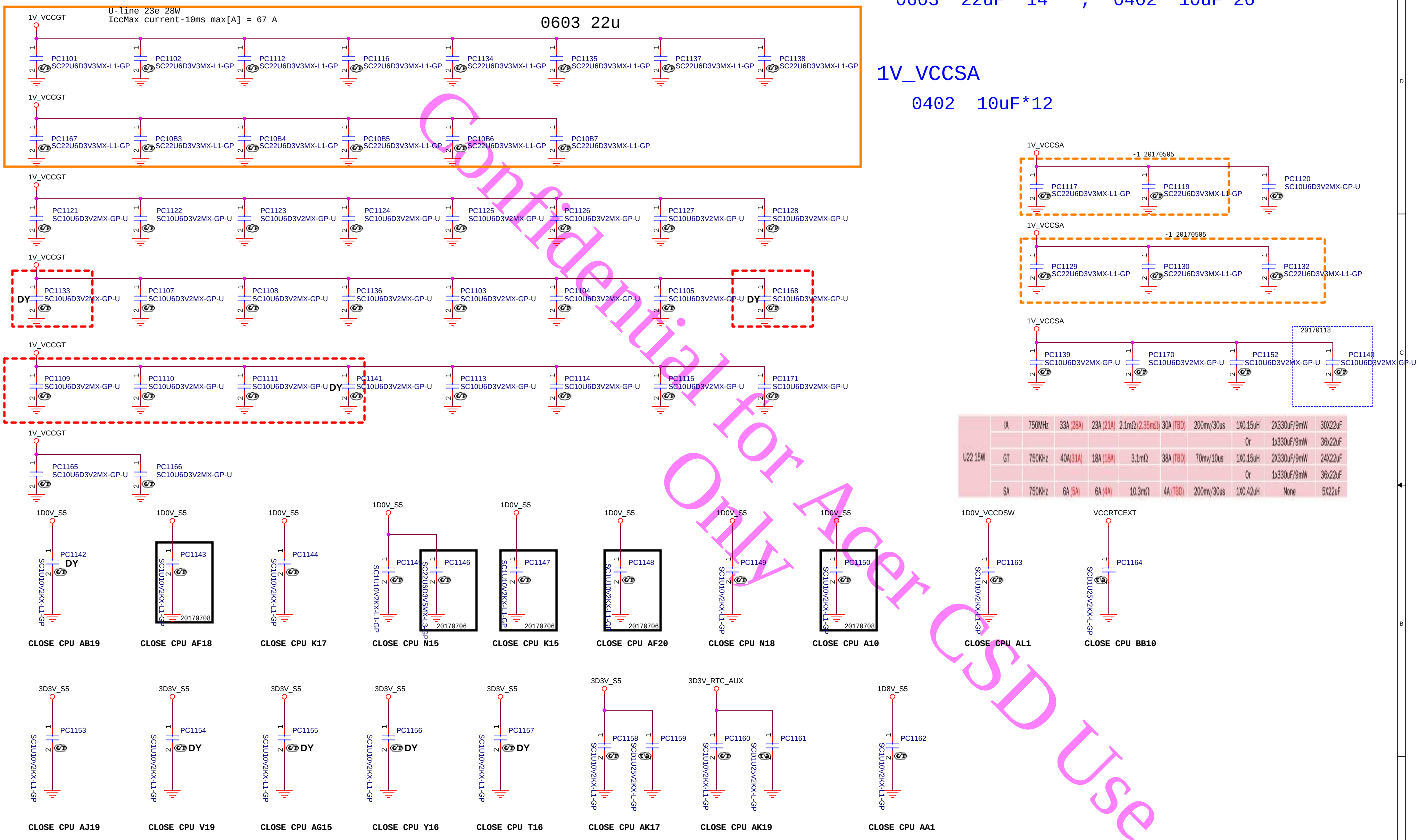


Main Func = CPU

SLICED GT

1V_VCCGT
0603 22uF *14 , 0402 10uF*26

1V_VCCSA
0402 10uF*12



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

Count

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Title: CPU_(Power CAP2)

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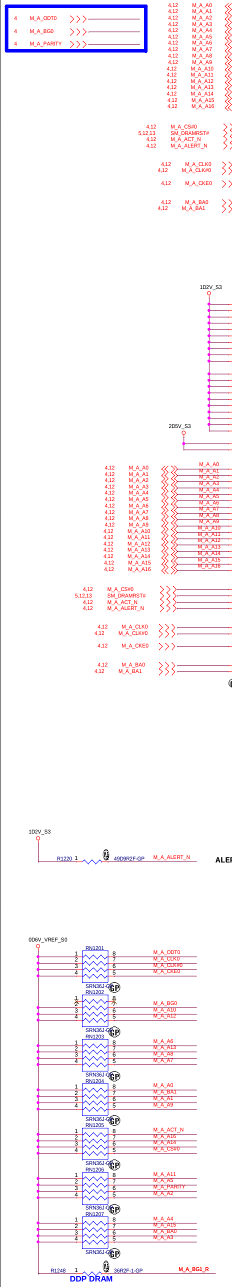
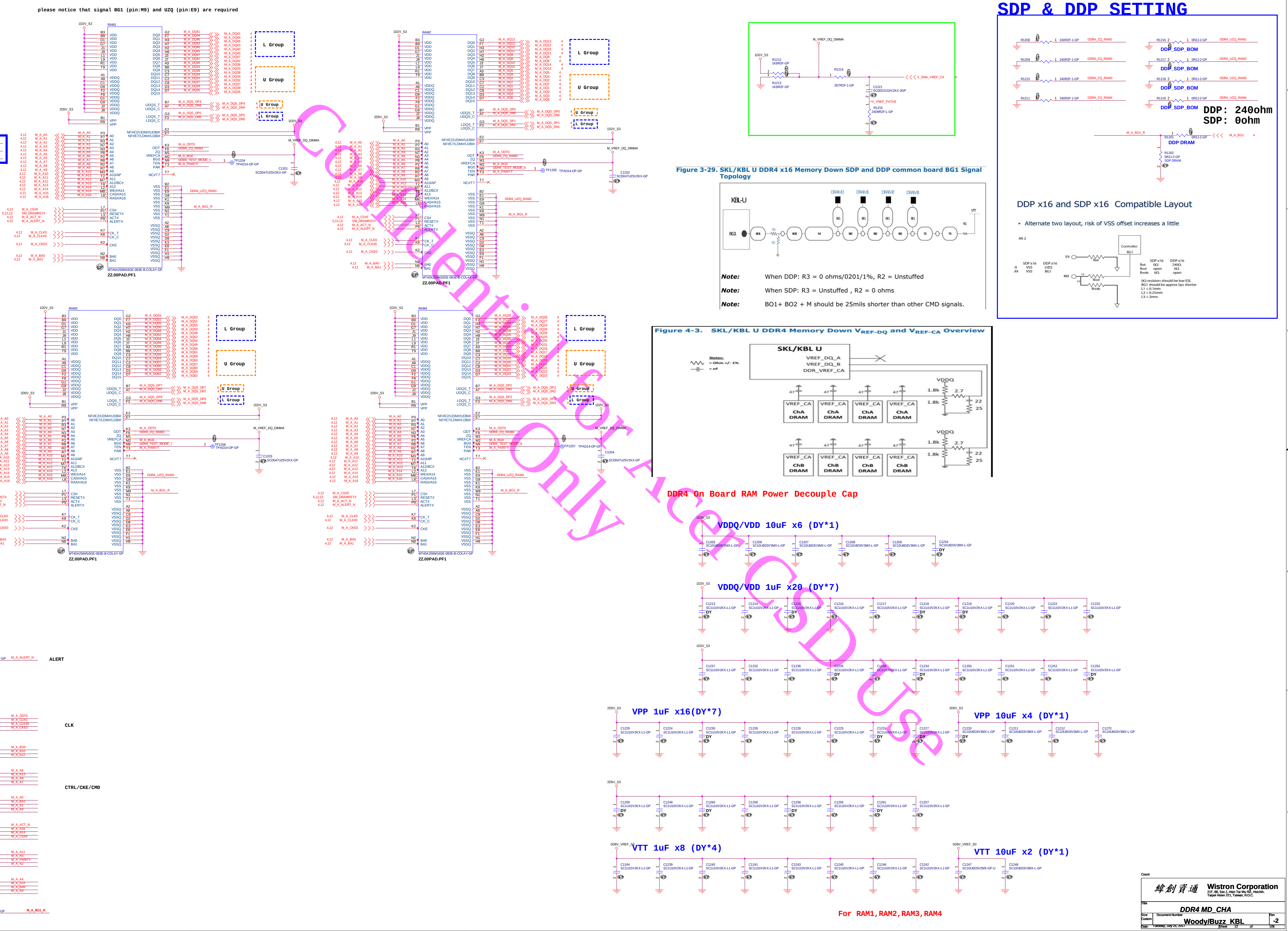
SSID = LPDDR3 CHA

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63





Wistron Corporation

DDR4 MD_CHA

Woody/Buzz_KBL

Rev -2

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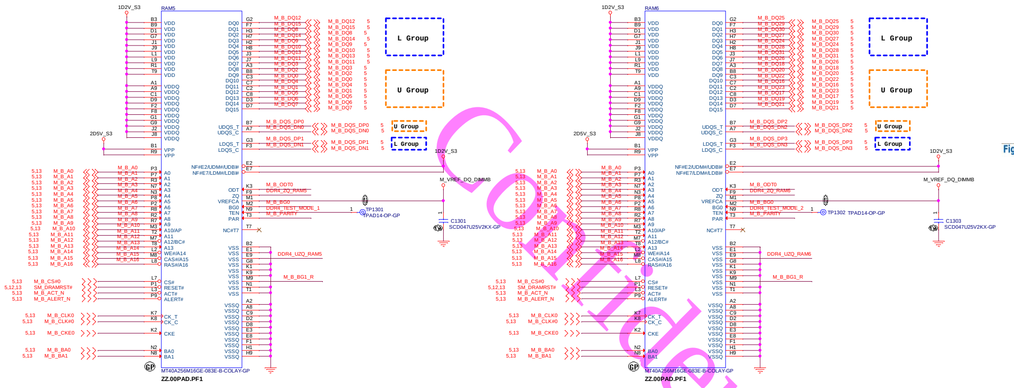
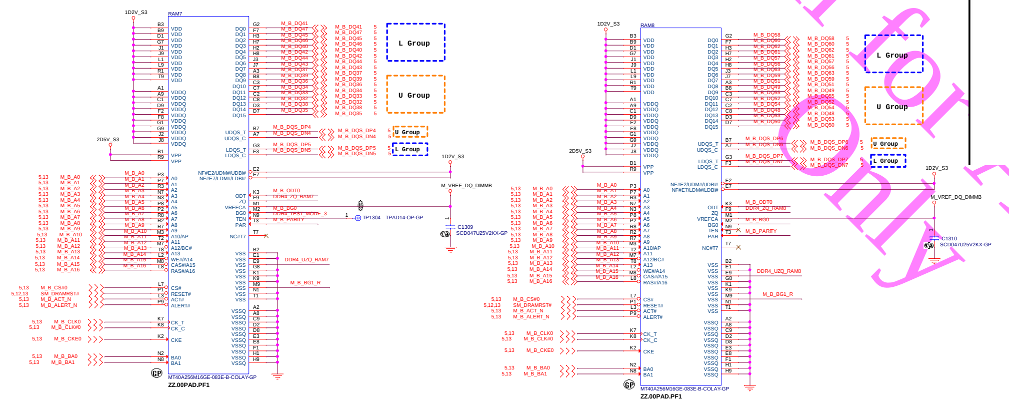
SSID = LPDDR3 CHB

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required





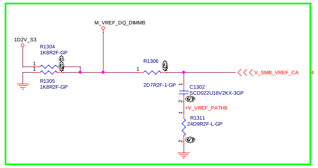
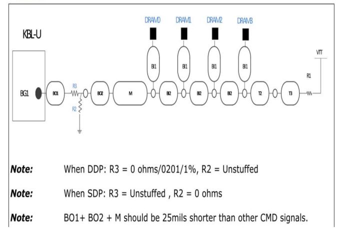
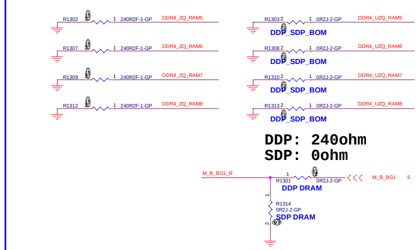


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology



SDP & DDP SETTING



DDP: 240ohm
SDP: 0ohm

DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

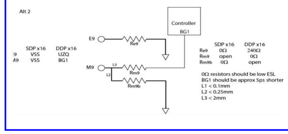
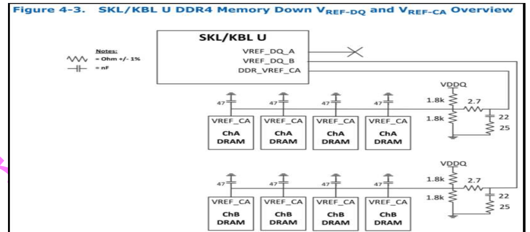
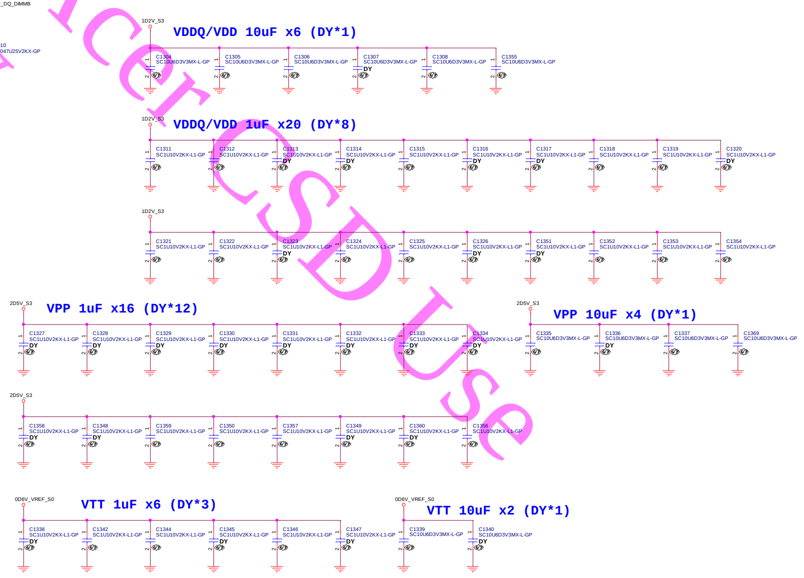
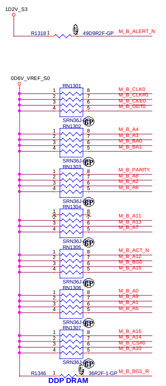


Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



DDR4 On Board RAM Power Decouple Cap





ALERT

CLK

CTRL/CKE/CMD

4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic	3D3V_S0 RN1401 SRN2K2J-5-GP HDMI_DATA_CPU 3,57 HDMI_CLK_CPU 3,57	3D3V_S0 R1401 2K2R2J-2-GP DDPC_CTRLDATA 3	3D3V_S5 R1441 10KR2J-3-GP DY SPI_SO_CPU 18	3D3V_S0 R1407 1KR2J-L2-GP DY GPP_B18/GSPI0_MOSI 6	3D3V_S0 R1408 1KR2J-L2-GP DY GPP_B22/GSPI1_MOSI 6		3D3V_S0 R1443 10KR2J-3-GP DY DDPD_CDA 3
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic	3D3V_S0 R1415 1KR2J-L2-GP DY HDA_SPKR 17,27	3D3V_S5 R1435 10KR2J-3-GP DY SPI_SI_CPU 18	3D3V_S5 R1436 1KR2J-L2-GP SPI_HOLD_ROM_R 25	3D3V_S5 R1437 1KR2J-L2-GP SPI_WP_ROM_R 25	3D3V_S5 R1438 10KR2J-3-GP DY GPP_C2/SMBALERT# 18	3D3V_S5 R1439 10KR2J-3-GP DY GPP_C5/SML0ALERT# 18	3D3V_S5 R1440 150KR2J-GP DY GPP_B23/SML1ALERT# 18
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

Signal	Usage	When Sampled	Comment
DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit 10** — **Boot BIOS Destination** 0 — SPI 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default	NMI or SMI Capable	Note
		Input	Output				
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts
GPP_B23	20K PD (see note)	Yes	No	SML1ALERT#/ PCHHOT#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts

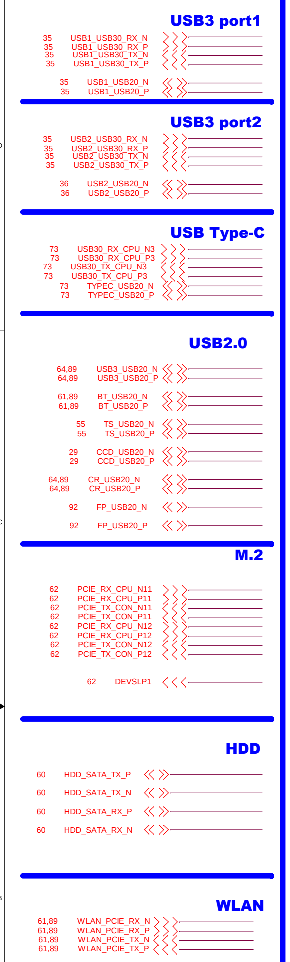
Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio Interface					
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLK	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Driven Low		OFF
HDA_SDI[1:0]	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

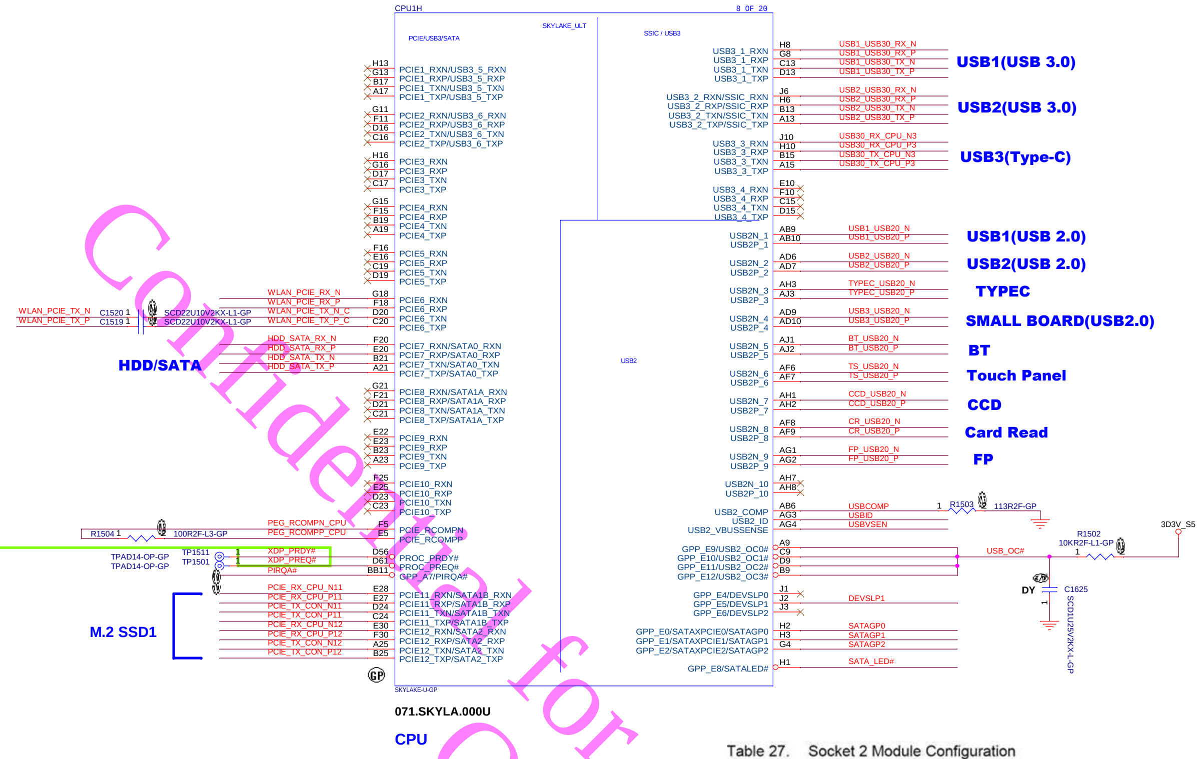
Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	Off
SPI0_MOSI	Primary	Internal Pull up/ Pull-down (See Note 1 &2)	Driven Low	Driven Low	Off
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	Off
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	Off
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	Off
SPI1_CLK	Primary	Undriven	Undriven	Undriven	Off
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	Off
SPI1_MISO	Primary	Undriven	Undriven	Undriven	Off
SPI1_CS#	Primary	Undriven	Undriven	Undriven	Off
SPI_IO[2:3]	Primary	Undriven	Undriven	Undriven	Off

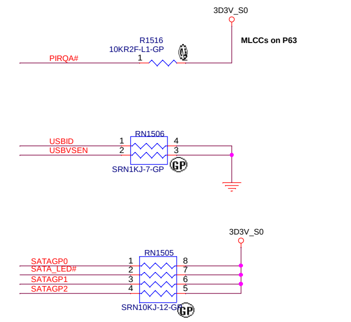
Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

Main Func = PCH

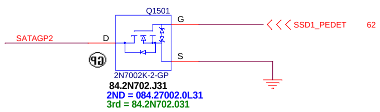


Layout Note:
1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.





M.2 auto detection



Pin define from PCH and socket side.

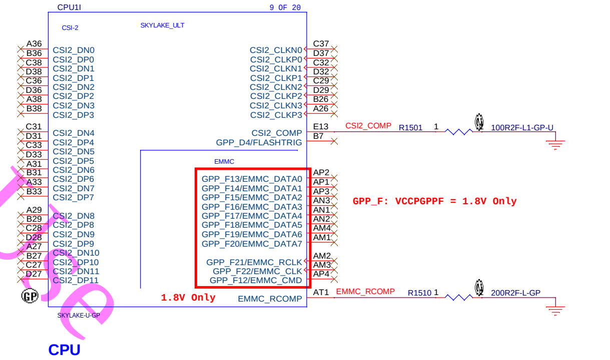
	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

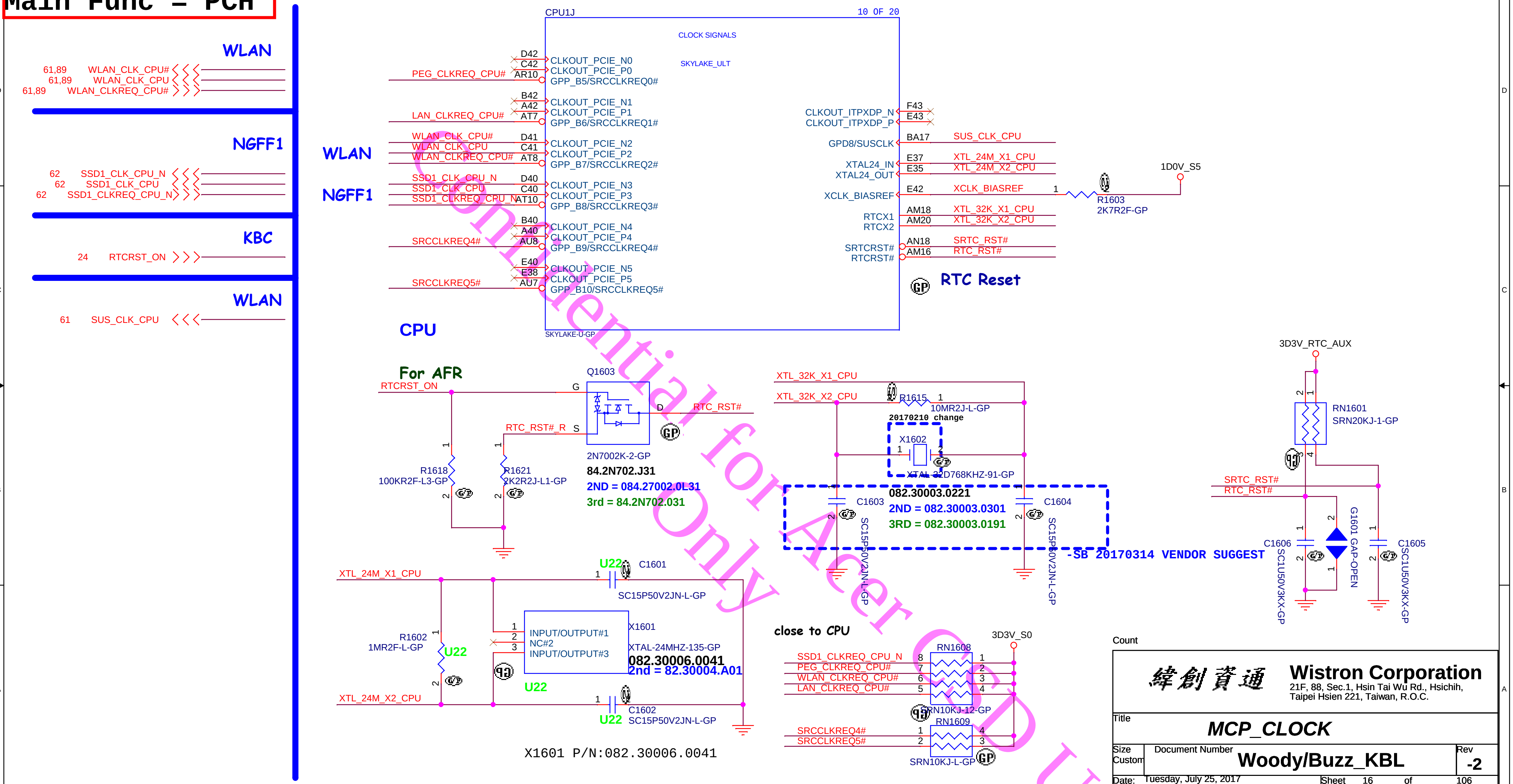
Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

	KBL Premium U		Acer 2015		2017 R15(Premium)		2017 R15(base)
Lane1	USB3 Port1		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane2	USB3 Port2		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane3	USB3 Port3		USB 3 (I/O)		USB 3 Type-C (I/O)		USB 3 Type-C (I/O)
Lane4	USB3 Port4						
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU		dGPU		dGPU
Lane6	USB3 Port6 (Premium)	PCIe Port2					
Lane7		PCIe Port3					
Lane8		PCIe Port4					
Lane9		PCIe Port5	LAN				
Lane10		PCIe Port6	WIFI		WIFI		WIFI
Lane11	SATA0 (Base/Premium)	PCIe Port7 (Premium)	HDD		HDD		HDD
Lane12	SATA1 (Base/Premium)	PCIe Port8 (Premium)	ODD				
Lane13		PCIe Port9	NA	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal		M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal
Lane14		PCIe Port10					
Lane15	SATA1 (Premium)	PCIe Port11					
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x1)		M.2 SSD SATA		
	USB2 Port1		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port2		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port3		USB 3 (I/O)		USB 2 Type-C (I/O)		USB 2 Type-C (I/O)
	USB2 Port4		USB 2 (I/O) / Sensor Hub		USB 2 (I/O)		USB 2 (I/O)
	USB2 Port5		BT		BT		BT
	USB2 Port6		TS		TS		TS
	USB2 Port7		CCD		CCD		CCD
	USB2 Port8		CR (USB) / FP		CR		CR
	USB2 Port9		3G		FP		FP
	USB2 Port10						



Main Func = PCH



Count

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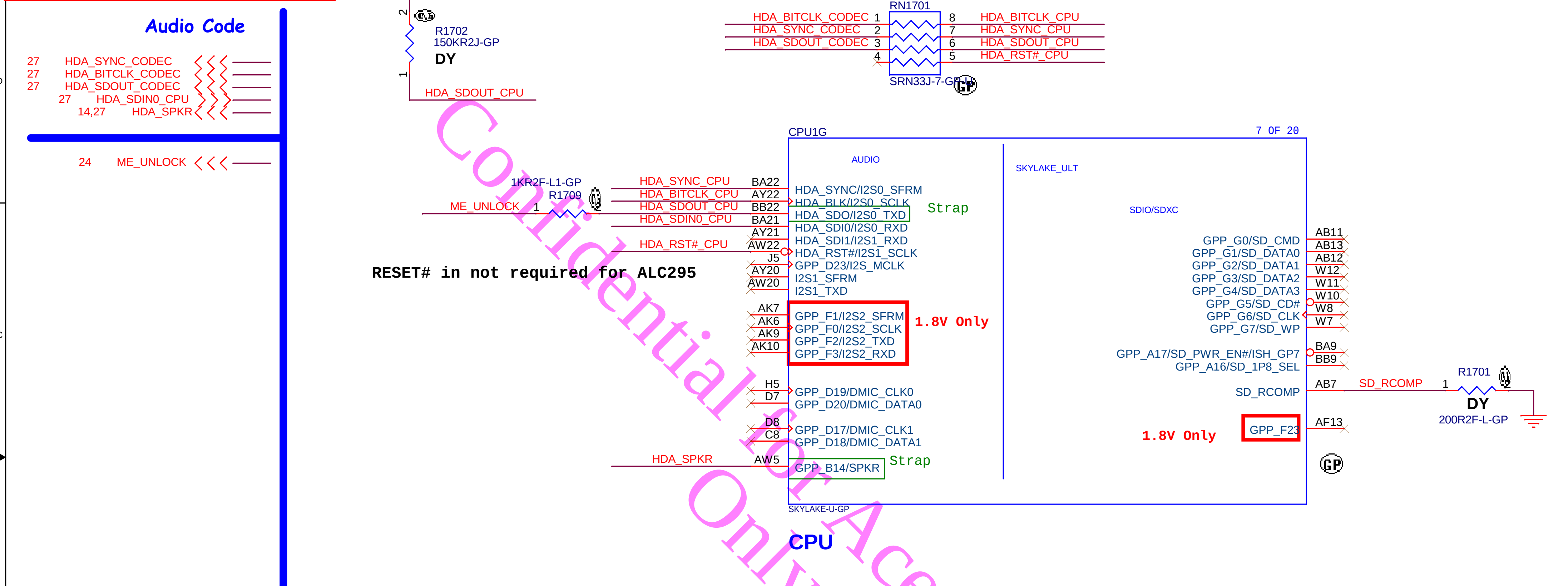
Title	MCP_CLOCK	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 16 of 106	

Main Func = PCH



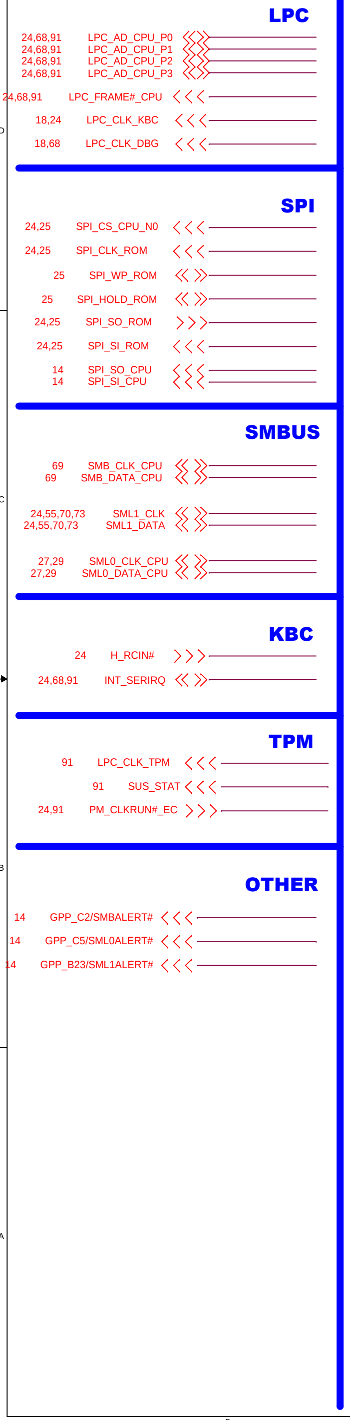
18.3 Terminating Unused SDXC Signals

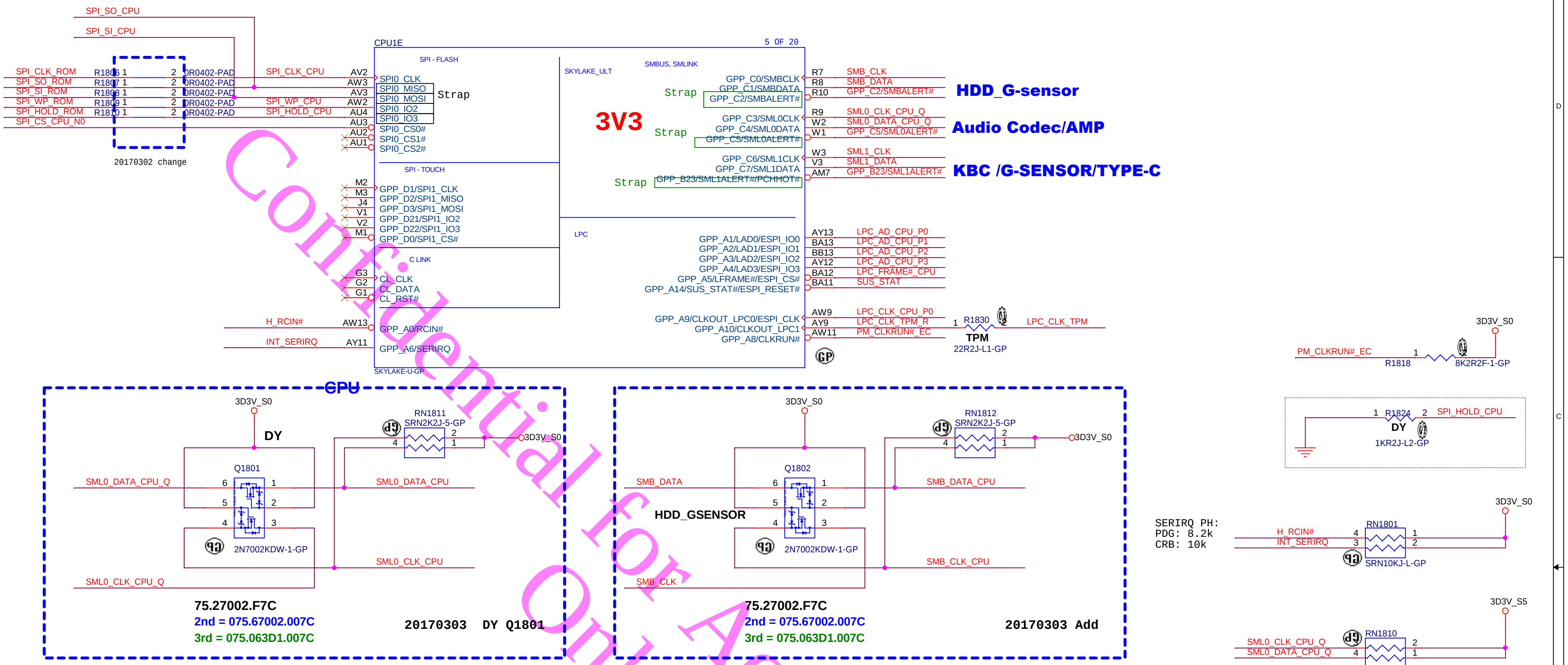
SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

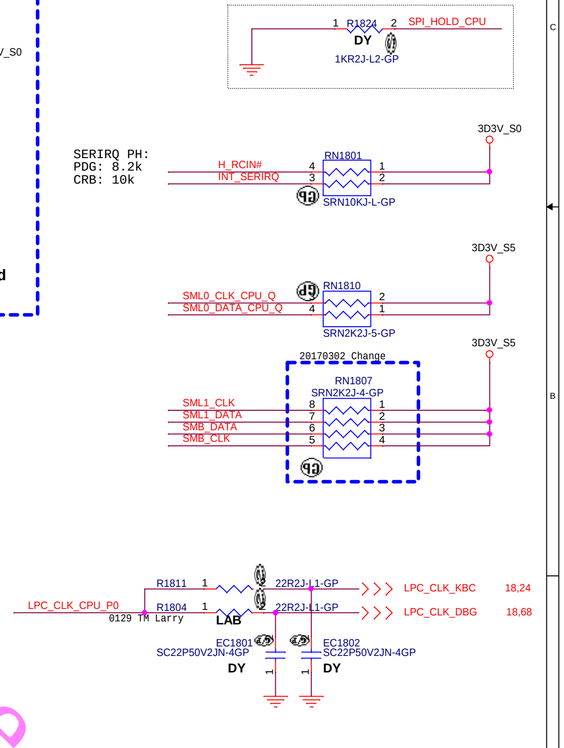
Count	緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_(AUDIO/SDIO/SDXC)
Size: Custom	Document Number: Woody/Buzz_KBL — Rev: -2
Date: Tuesday, July 25, 2017	Sheet 17 of 106

Main Func = PCH





Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.



20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

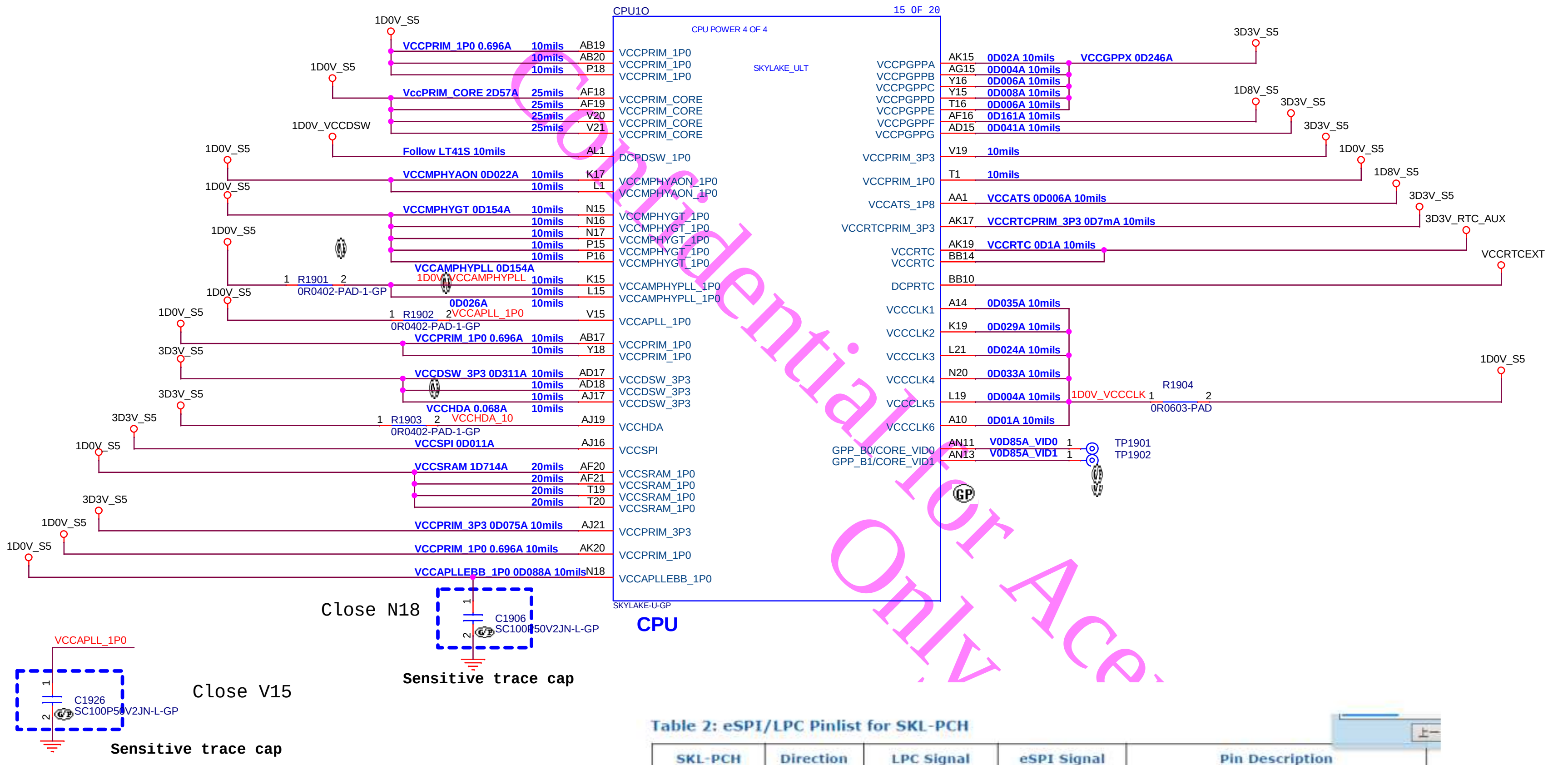


Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM L0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

Count

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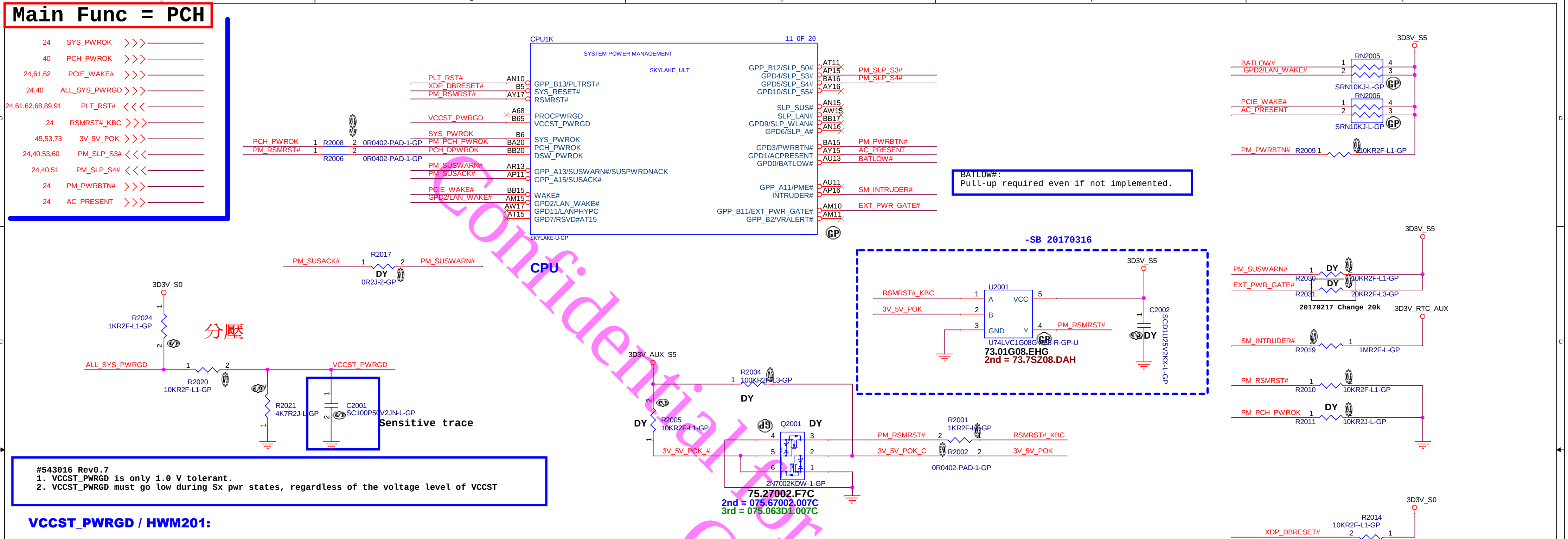
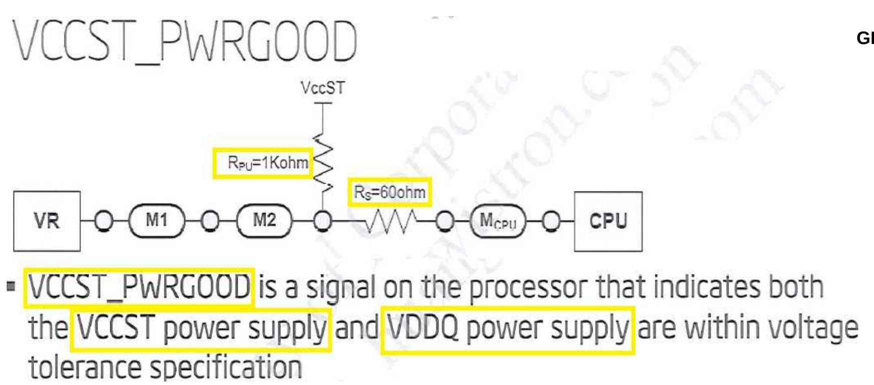
Title	CPU_(CS-2/EMMC)
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 19 of 106

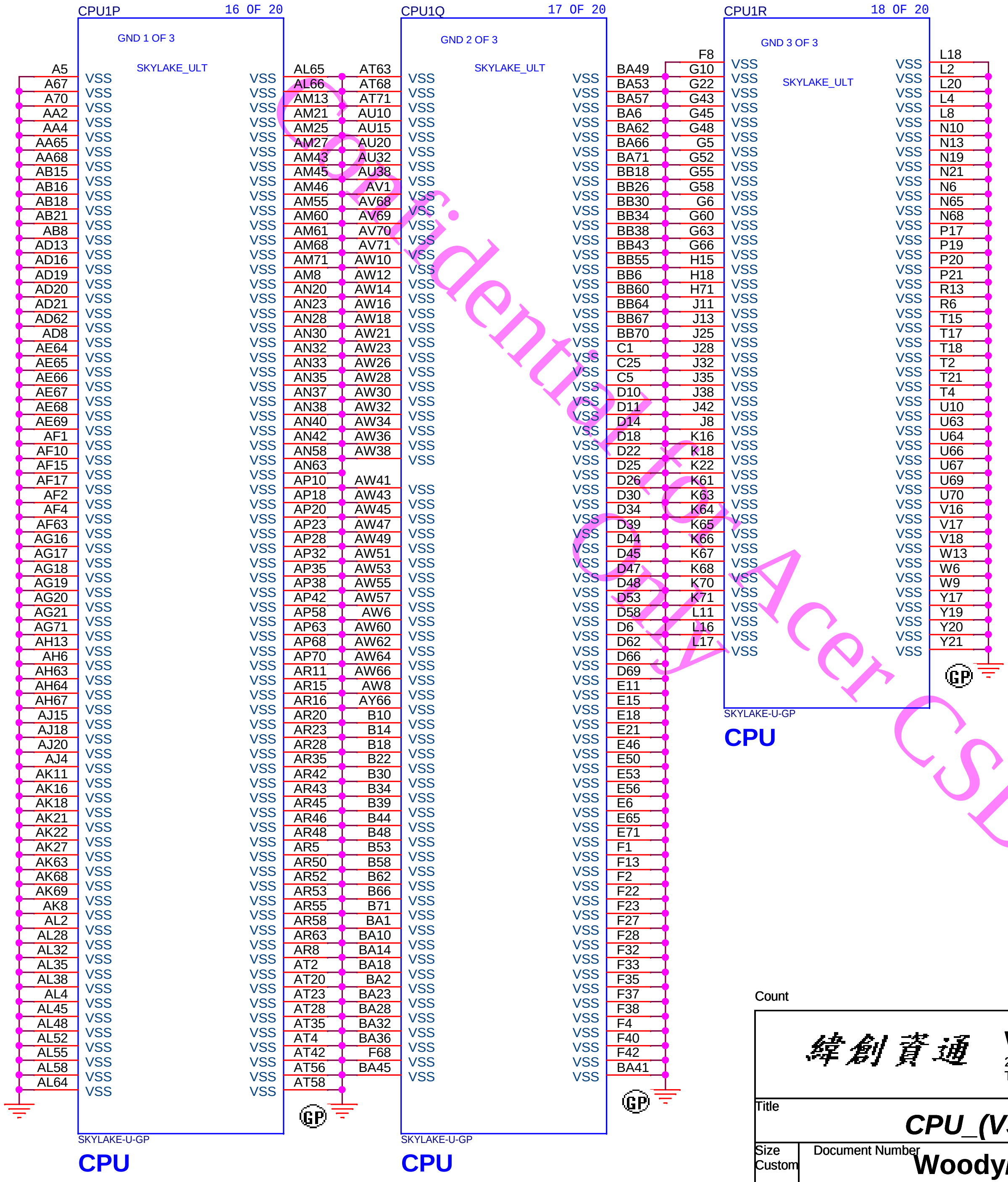




GPP_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2) Input	Output	Multiplexed With	Default
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

Main Func = PCH



Count

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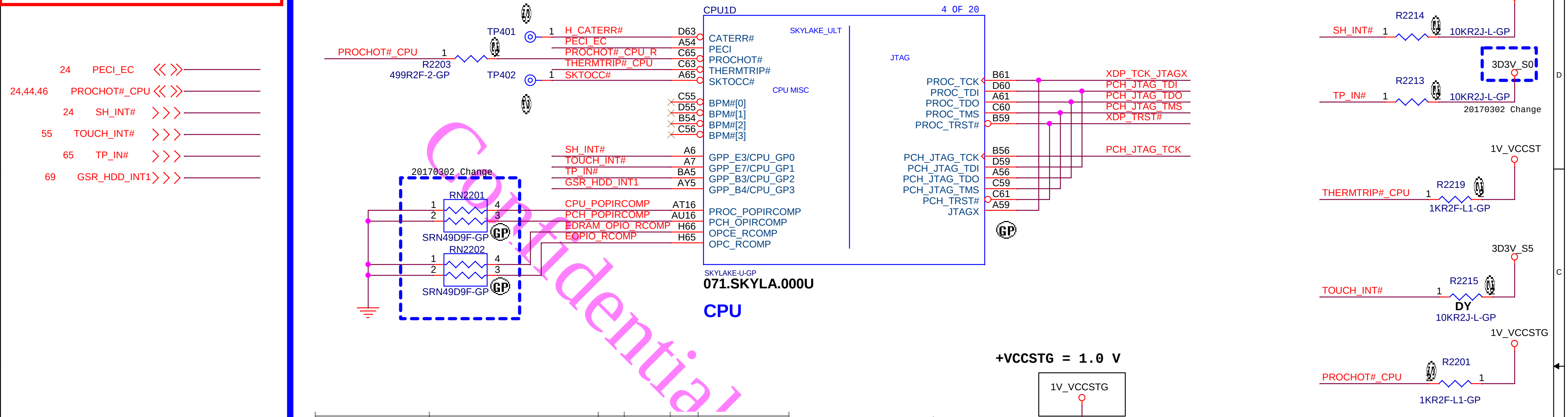
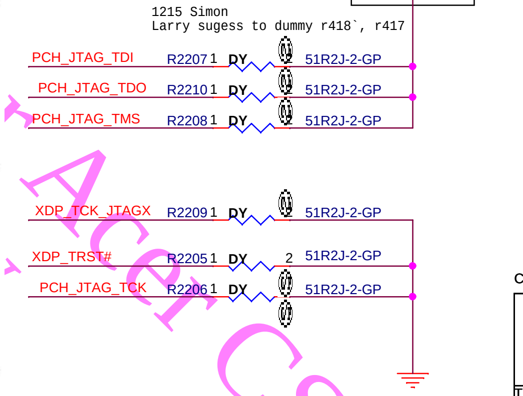
Title	CPU_(VSS)	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 21 of 106	

Main Func = CPU



PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines



Count

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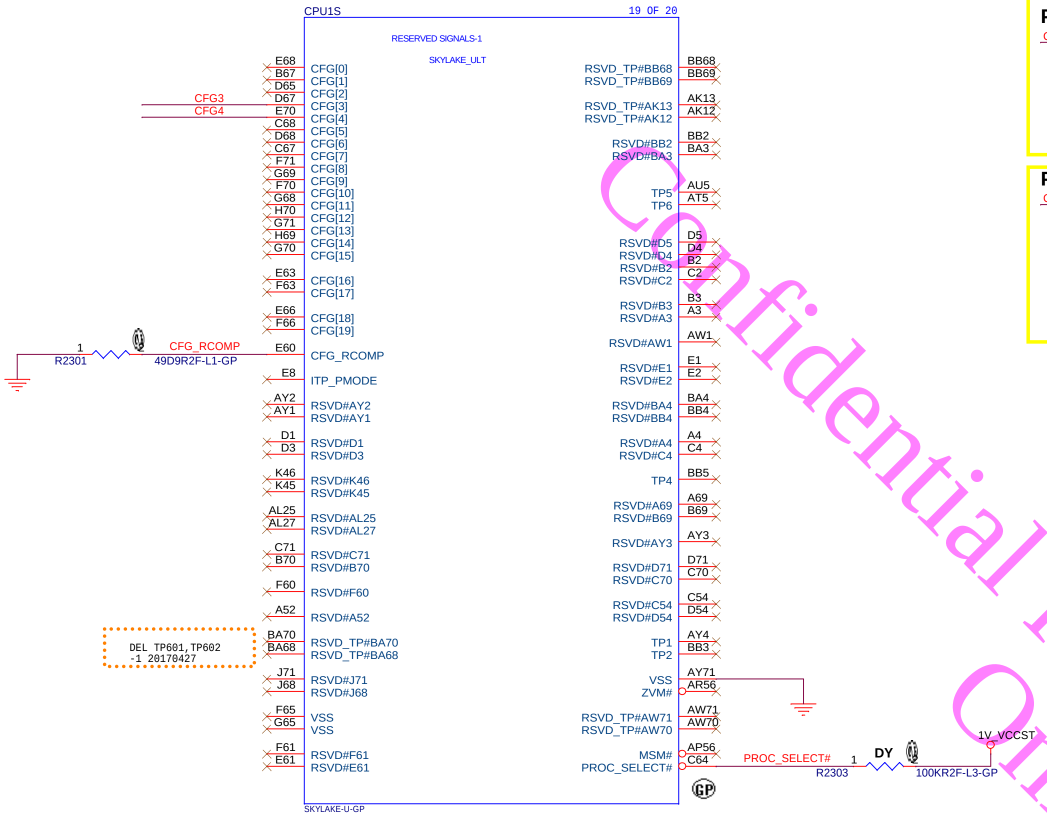
Title: **CPU_(JTAG/CPU SIDE BAND)**

Size: Custom | Document Number: **Woody/Buzz_KBL** | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 22 of 106

Main Func = CPU



CPU

PCH strap pin:

CFG3
R2305
1KR2J-1-GP
DY

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

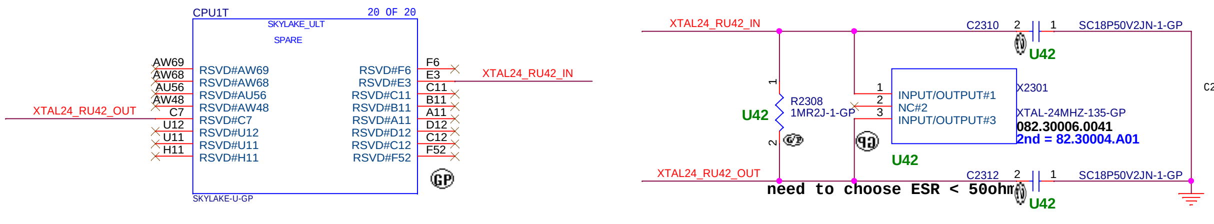
PCH strap pin:

CFG4
R2304
1KR2J-1-GP

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]**: Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines

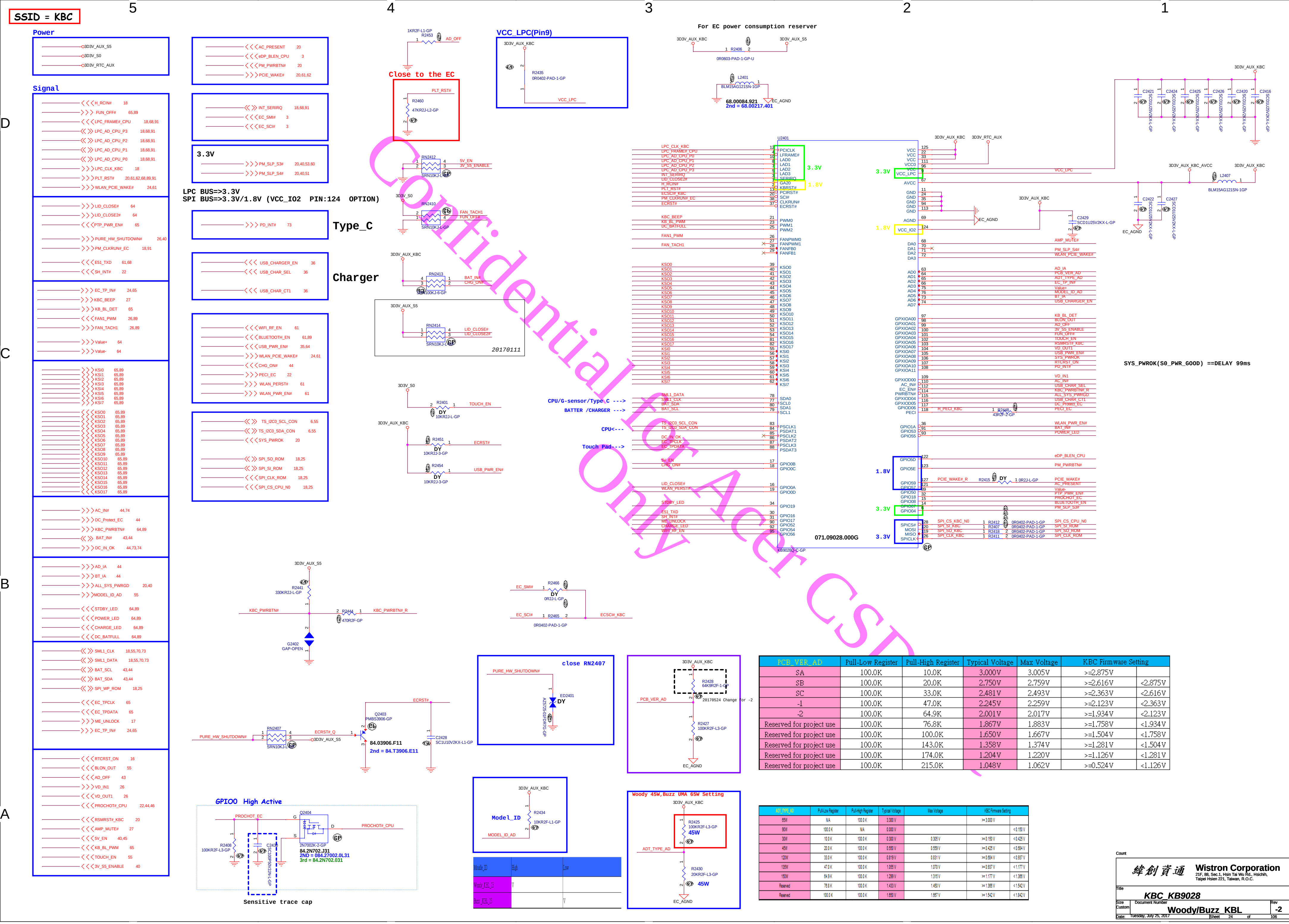


CPU

C2310,C2312 changed 20170510 -1

P/N: 082.30006.0041

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: CPU_RESERVED,CFG			
Size: Custom	Document Number: Woody/Buzz_KBL		Rev: -2
Date: Tuesday, July 25, 2017	Sheet 23 of 106		



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0K	10.0K	3.000V	3.005V	>=2.875V	
SB	100.0K	20.0K	2.750V	2.759V	>=2.616V	<2.875V
SC	100.0K	33.0K	2.481V	2.493V	>=2.363V	<2.616V
-1	100.0K	47.0K	2.245V	2.259V	>=2.123V	<2.363V
-2	100.0K	64.9K	2.001V	2.017V	>=1.934V	<2.123V
Reserved for project use	100.0K	76.8K	1.867V	1.883V	>=1.758V	<1.934V
Reserved for project use	100.0K	100.0K	1.650V	1.667V	>=1.504V	<1.758V
Reserved for project use	100.0K	143.0K	1.358V	1.374V	>=1.281V	<1.504V
Reserved for project use	100.0K	174.0K	1.204V	1.220V	>=1.126V	<1.281V
Reserved for project use	100.0K	215.0K	1.048V	1.062V	>=0.524V	<1.126V

Moudle_ID	High	Low
Woody_KBL_13	V	
Buzz _KBL_15		V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.368 V
Reserved	78.8 K	100.0 K	1.433 V	1.450 V	>= 1.368 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

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Title: KBC_KB9028
Size: Custom
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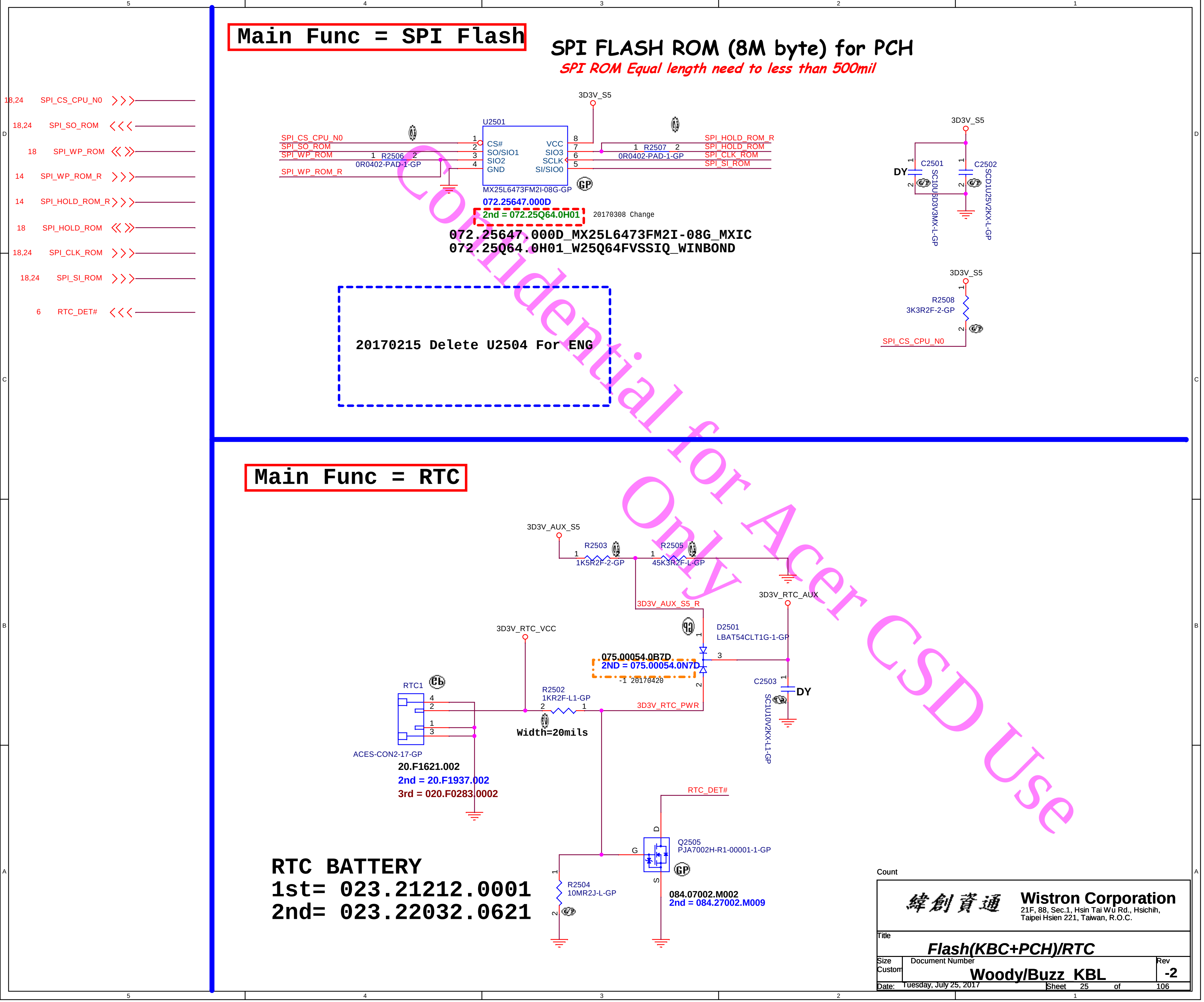
Main Func = SPI Flash
SPI FLASH ROM (8M byte) for PCH
SPI ROM Equal length need to less than 500mil
18,24 SPI_CS_CPU_N0
18,24 SPI_SO_ROM
18 SPI_WP_ROM
14 SPI_WP_ROM_R
14 SPI_HOLD_ROM_R
18 SPI_HOLD_ROM
18,24 SPI_CLK_ROM
18,24 SPI_SI_ROM
6 RTC_DET#
3D3V_S5
U2501
CS#
SO/SIO1
SIO2
GND
VCC
SIO3
SCLK
SI/SIO0
SPI_CS_CPU_N0
SPI_SO_ROM
SPI_WP_ROM
SPI_WP_ROM_R
R2506
0R0402-PAD-1-GP
R2507
0R0402-PAD-1-GP
SPI_HOLD_ROM_R
SPI_HOLD_ROM
SPI_CLK_ROM
SPI_SI_ROM
MX25L6473FM2I-08G-GP
GP
072.25647.000D
2nd = 072.25Q64.0H01
20170308 Change
072.25647.000D_MX25L6473FM2I-08G_MXIC
072.25Q64.0H01_W25Q64FVSSIQ_WINBOND
3D3V_S5
DY
C2501
SC10U6D3V3MX-L-GP
C2502
SCD1U25V2KX-L-GP
3D3V_S5
R2508
3K3R2F-2-GP
SPI_CS_CPU_N0
20170215 Delete U2504 For ENG
Main Func = RTC
3D3V_AUX_S5
R2503
1K5R2F-2-GP
R2505
45K3R2F-L-GP
3D3V_AUX_S5_R
3D3V_RTC_AUX
D2501
LBAT54CLT1G-1-GP
075.00054.0B7D
2ND = 075.00054.0N7D
-1 20170420
C2503
DY
SC1U10V2KX-L1-GP
3D3V_RTC_VCC
RTC1
R2502
1KR2F-L1-GP
3D3V_RTC_PWR
Width=20mils
ACES-CON2-17-GP
20.F1621.002
2nd = 20.F1937.002
3rd = 020.F0283.0002
RTC_DET#
Q2505
PJA7002H-R1-00001-1-GP
GP
R2504
10MR2J-L-GP
084.07002.M002
2nd = 084.27002.M009
RTC BATTERY
1st= 023.21212.0001
2nd= 023.22032.0621
Count
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Flash(KBC+PCH)/RTC
Size Custom
Document Number
Woody/Buzz_KBL
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Date: Tuesday, July 25, 2017
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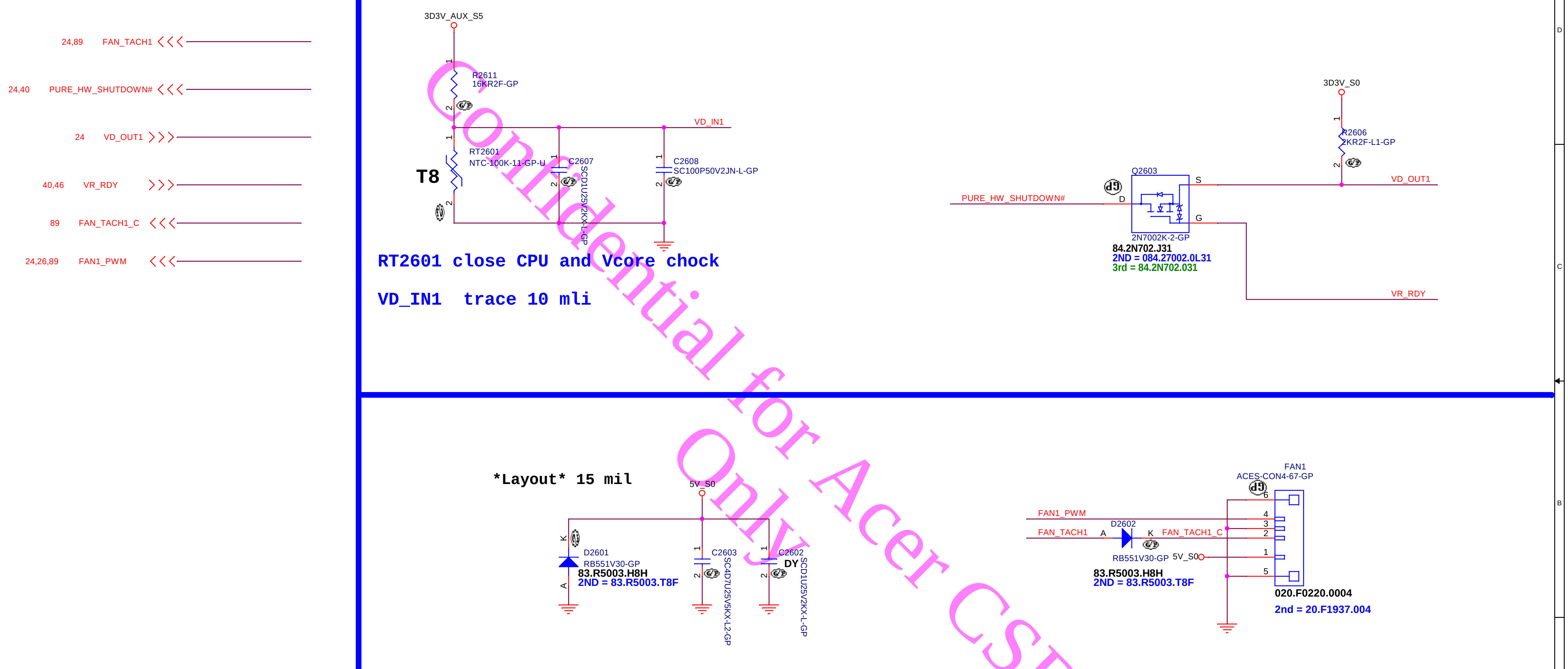
SSID = Thermal



Count

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Title		
Thermal 7718/Fan Controllor P2793		
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
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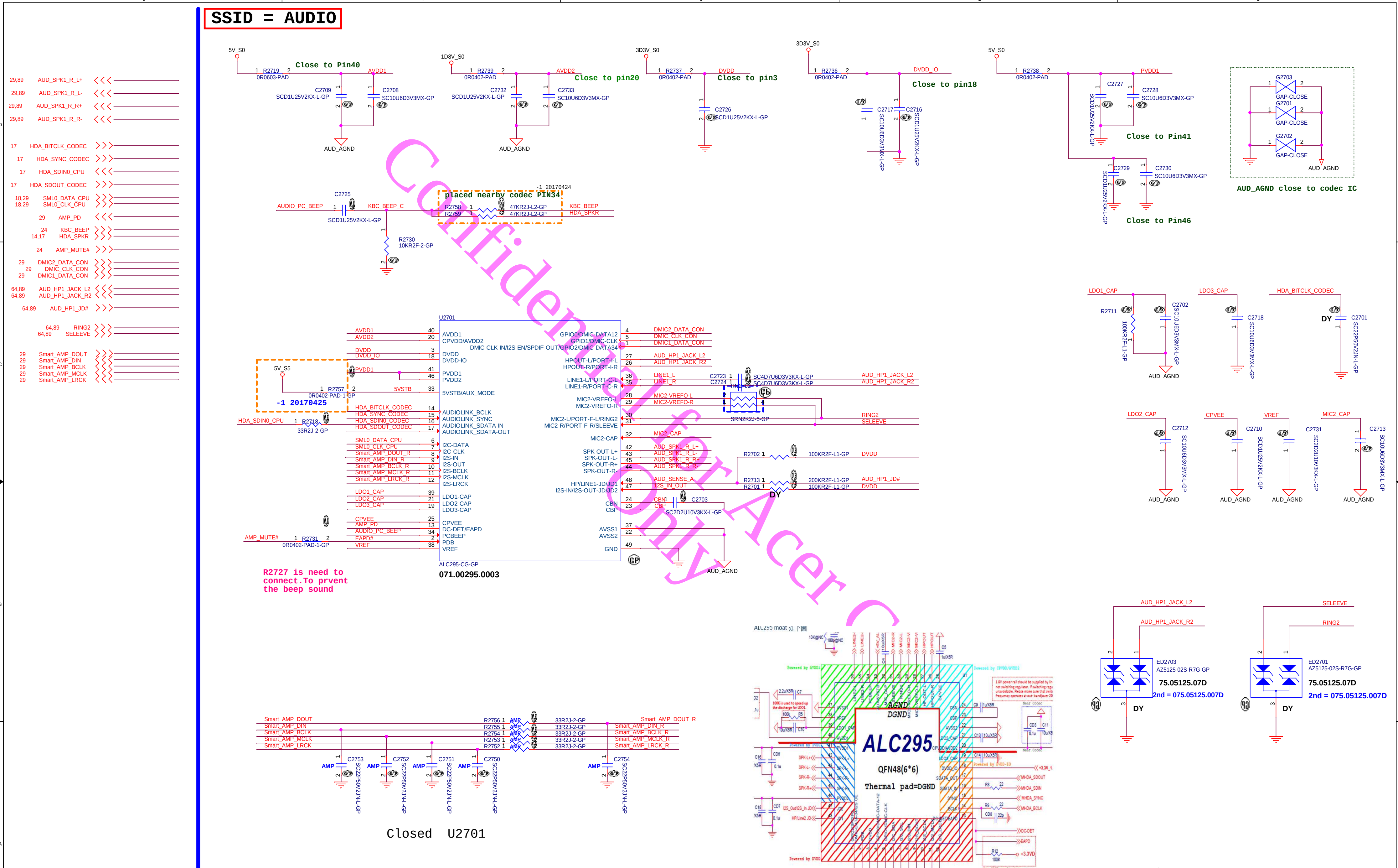

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Title	Audio Codec ALC295	
Size Custom	Document Number Woody/Buzz_KBL	Rev -2
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Blanking

Count

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Title	***Reserved***
Size A4	Document Number **Woody/Buzz_KBL** Rev **-2**
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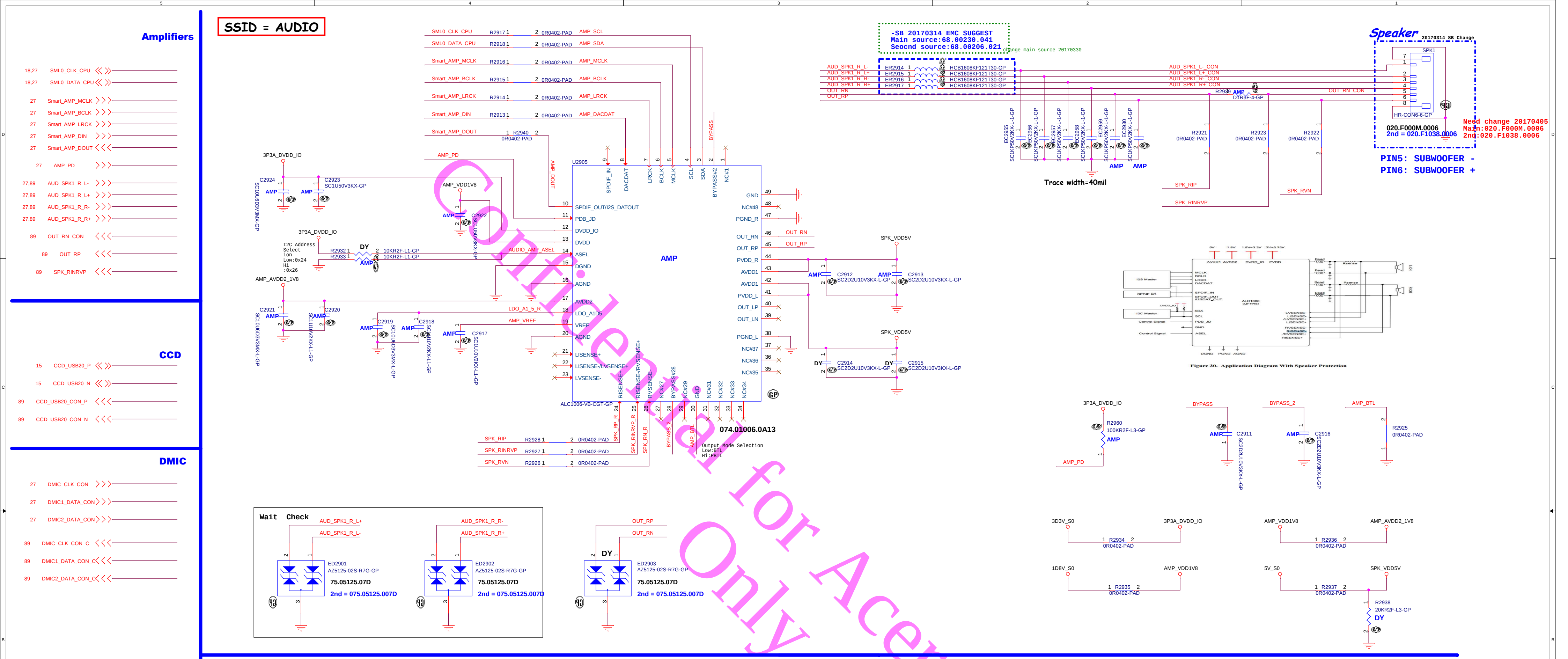

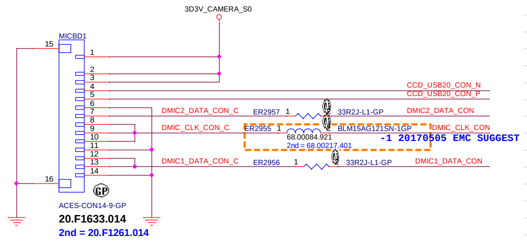

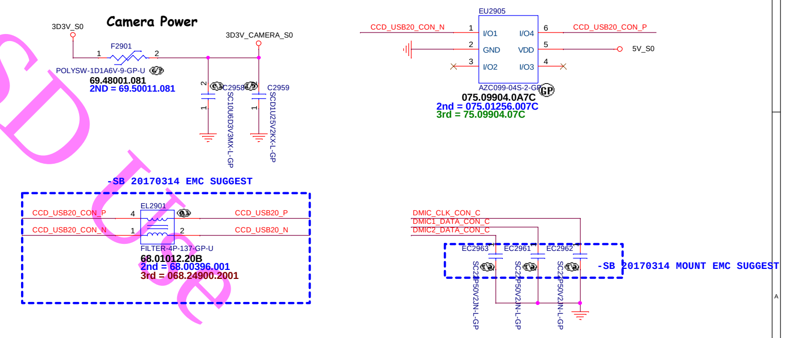

A. Pin define

Note

CCD Module

MB Connecter		CCD connector pin	MIC-R PCB	MIC-L PCB
Pin 1	3D3V_CAMERA_S0	1		
Pin 2	3D3V_CAMERA_S0		1	
Pin 3	3D3V_CAMERA_S0			1
Pin 4	CCD_USB20_CON_N	2		
Pin 5	CCD_USB20_CON_P	3		
Pin 6	GND	4		
Pin 7	DMIC2_DATA_CON	6		
Pin 8	DMIC_CLK_CON	5		
Pin 9	DMIC_CLK_CON		3	
Pin 10	DMIC_CLK_CON			3
Pin 11	GND		4	
Pin 12	DMIC1_DATA_CON		2	
Pin 13	DMIC1_DATA_CON			2
Pin 14	GND			4

MB Connecter | CCD Connecter

Blanking

Count

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Title	***Reserved***
Size A4	Document Number **Woody/Buzz_KBL** — Rev **-2**
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Count

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Title	***Reserved***	
Size A4	Document Number **Woody/Buzz_KBL**	Rev **-2**
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Count

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Title	***Reserved***
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Blanking

Count

Blanking

Count

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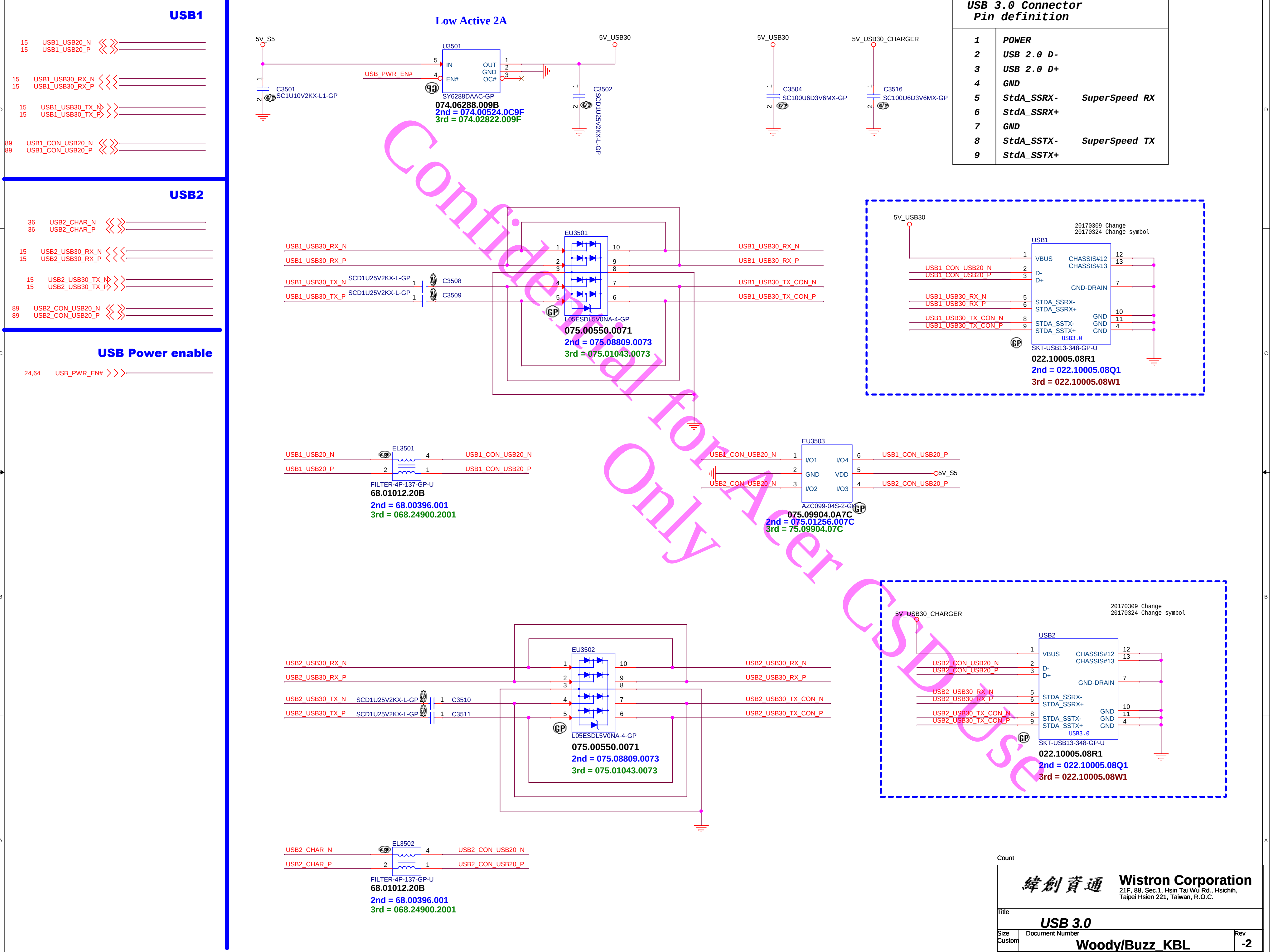
USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



Count

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Title: **USB 3.0**

Size: Custom | Document Number: **Woody/Buzz_KBL** | Rev: -2

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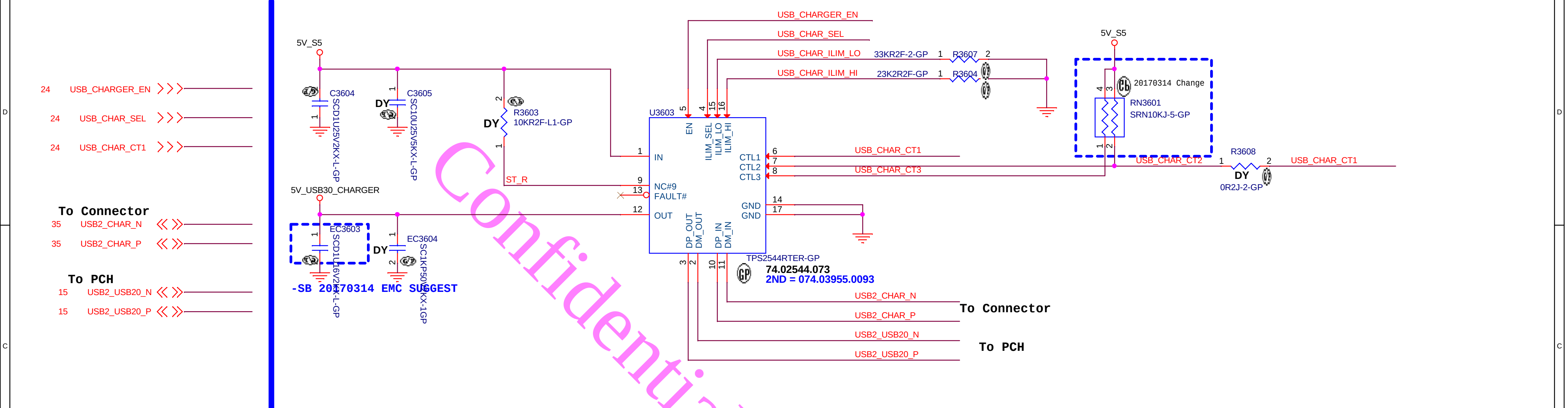

CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

Count

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Title: **USB CHARGER**

Size: Custom | Document Number: **Woody/Buzz_KBL** | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 36 of 106

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Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **Woody/Buzz_KBL**	Rev **-2**
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Count

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Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
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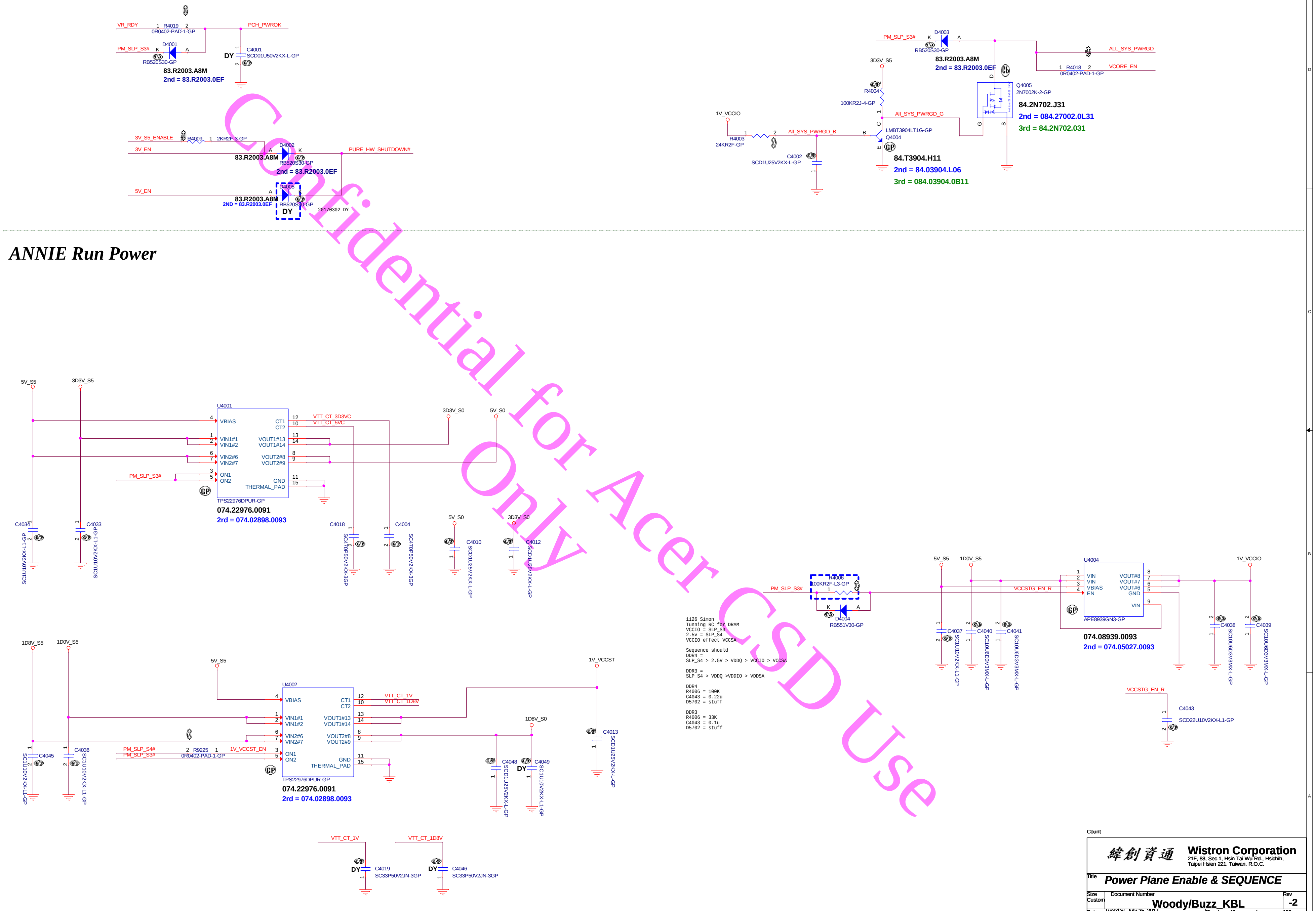
Power Sequence

26,46 VR_RDY
20 PCH_PWROK
20,24,40,53,60 PM_SLP_S3#
24 3V_S5_ENABLE
45 3V_EN
24,45 5V_EN
24,26 PURE_HW_SHUTDOWN#
20,24 ALL_SYS_PWRGD
46 VCORE_EN

Run Power

20,24,51 PM_SLP_S4#
20,24,40,53,60 PM_SLP_S3#

Power Sequence



ANNIE Run Power

1126 Simon
Tunning RC for DRAM
VCCIO = SLP_S3
2.5v = SLP_S4
VCCIO effect VCCSA

Sequence should
DDR4 =
SLP_S4 > 2.5V > VDDQ > VCCIO > VCCSA

DDR3 =
SLP_S4 > VDDQ >VDDIO > VDDSA

DDR4
R4006 = 100K
C4043 = 0.22u
D5702 = stuff

DDR3
R4006 = 33K
C4043 = 0.1u
D5702 = stuff

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Power Plane Enable & SEQUENCE
Size: Custom	Document Number: Woody/Buzz_KBL
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Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **Woody/Buzz_KBL** — Rev **-2**
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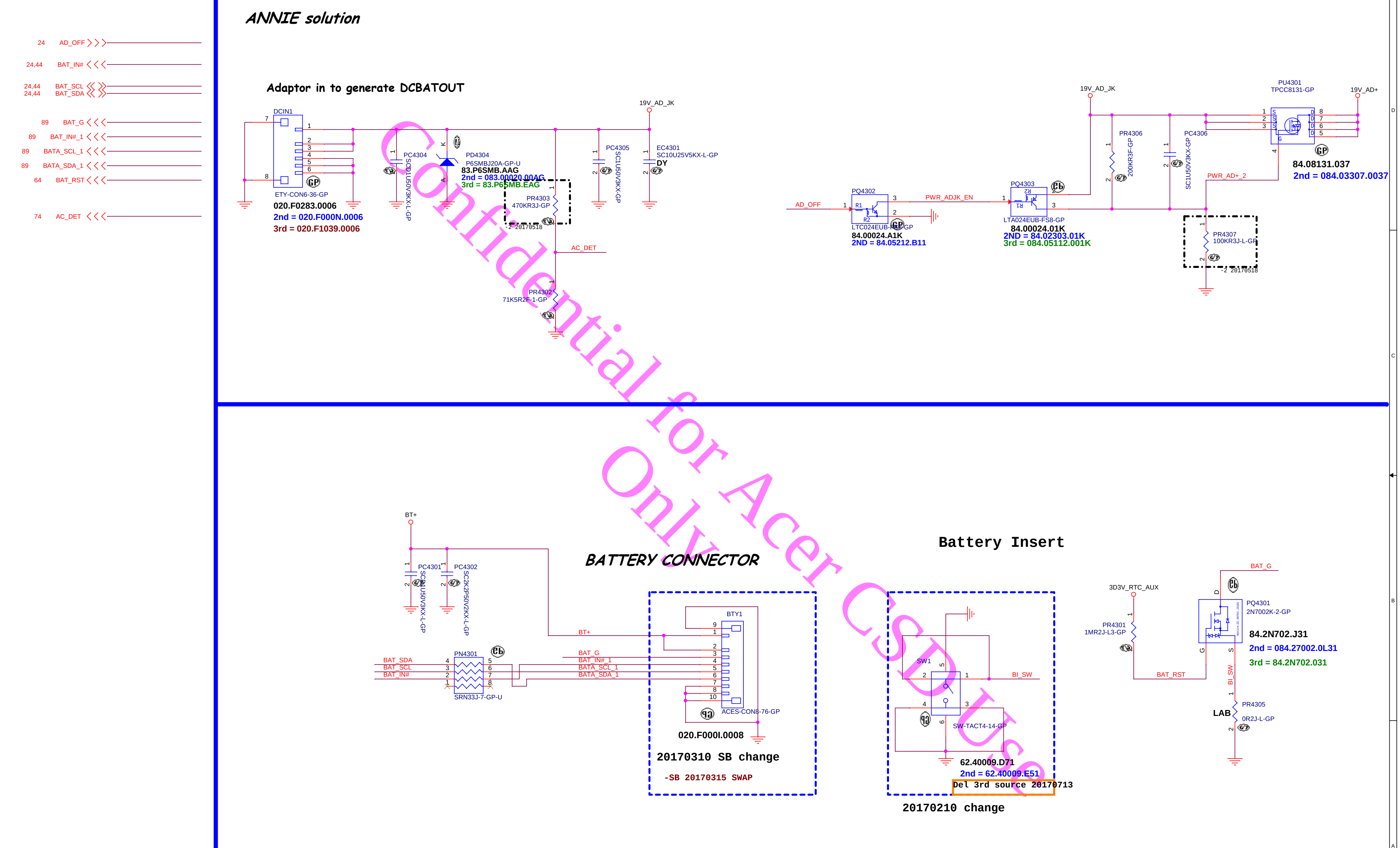
Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **Woody/Buzz_KBL** — Rev **-2**
Date: Tuesday, July 25, 2017	Sheet 42 of 106

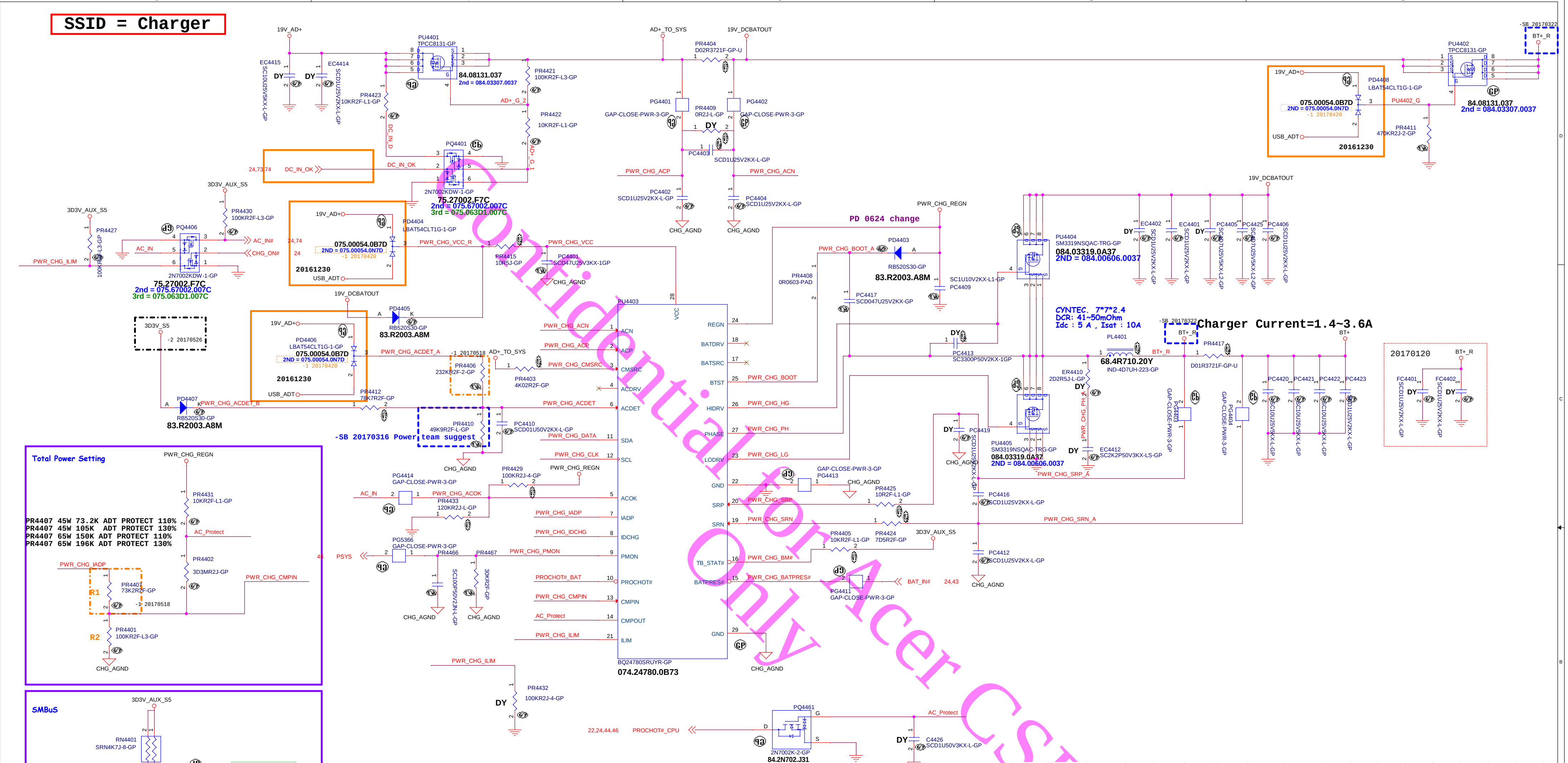


Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

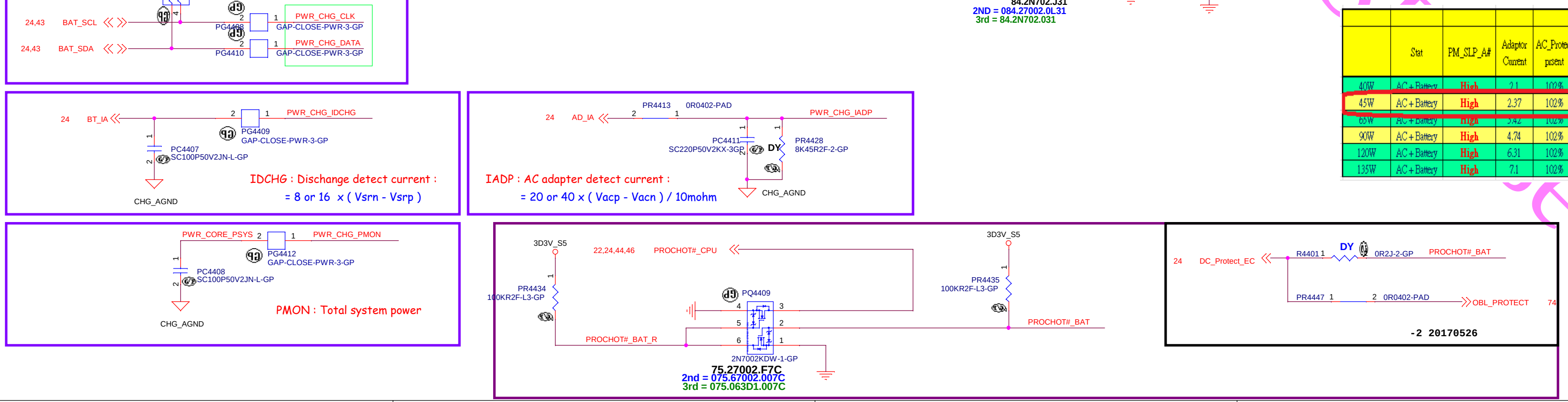
Title	BATT CONN	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 43 of 106	

SSID = Charger



						PR4404	0x12H_Bit 4	0x3BH_Bit 7		R1	R2
	Stat	PM_SLP_A#	Adaptor Current	AC_Protect prsent	AC_Protect Current	Sense resistor	IADP GAIN	CM_VREF	Current to Voltage	PR4407	PR4401
40W	AC+Battery	High	2.1	102%	2.142	20	40	1.2 V	1.7136	41.2	100
45W	AC+Battery	High	2.37	102%	2.4174	20	40	1.2 V	1.93392	60.4	100
65W	AC+Battery	High	3.42	102%	3.4884	10	40	1.2 V	1.39536	16.2	100
90W	AC+Battery	High	4.74	102%	4.8348	10	40	1.2 V	1.93392	60.4	100
120W	AC+Battery	High	6.31	102%	6.4362	10	40	1.2 V	2.57448	113	100
135W	AC+Battery	High	7.1	102%	7.242	10	40	1.2 V	2.8968	180	100

CAL			
Vcomp	Vsense	R1	R2
1.213598	1.7136	41.2	100
1.205686	1.93392	60.4	100
1.200826	1.39536	16.2	100
1.205686	1.93392	60.4	100
1.208676	2.57448	113	100
1.207	2.8968	140	100



緯創資通 Wistron Corporation
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Title: CHARGER HPA02224

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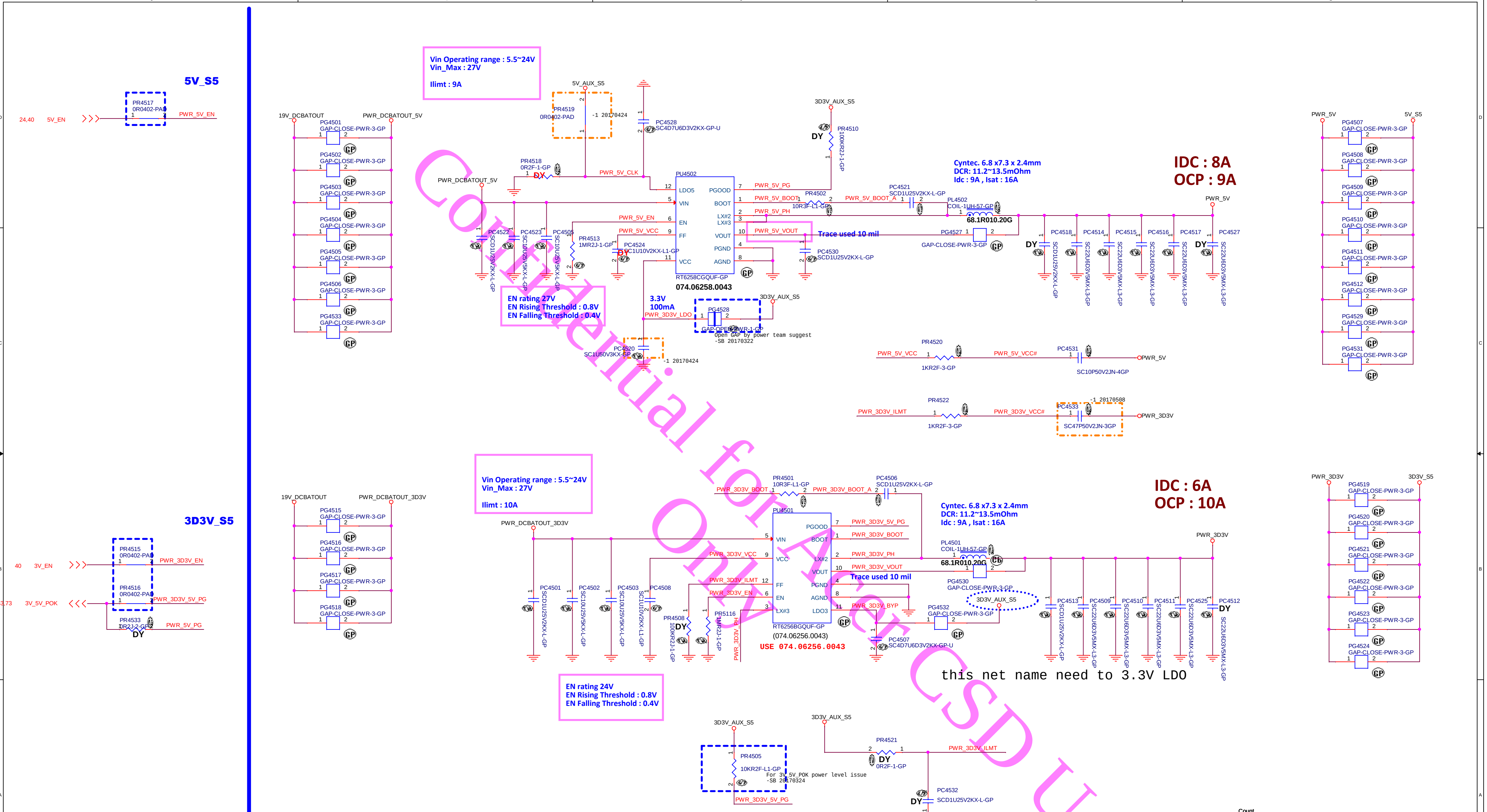

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT6226 5V/3D3V		
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
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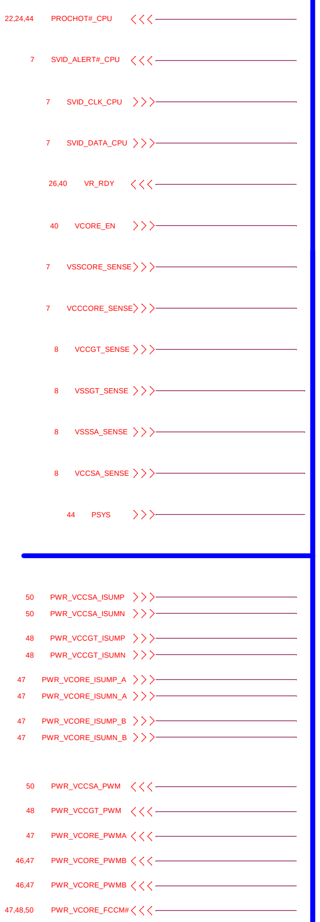
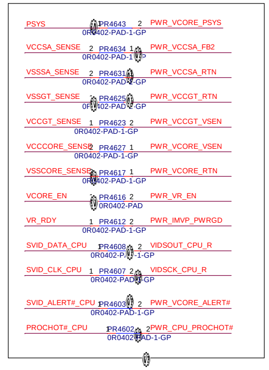
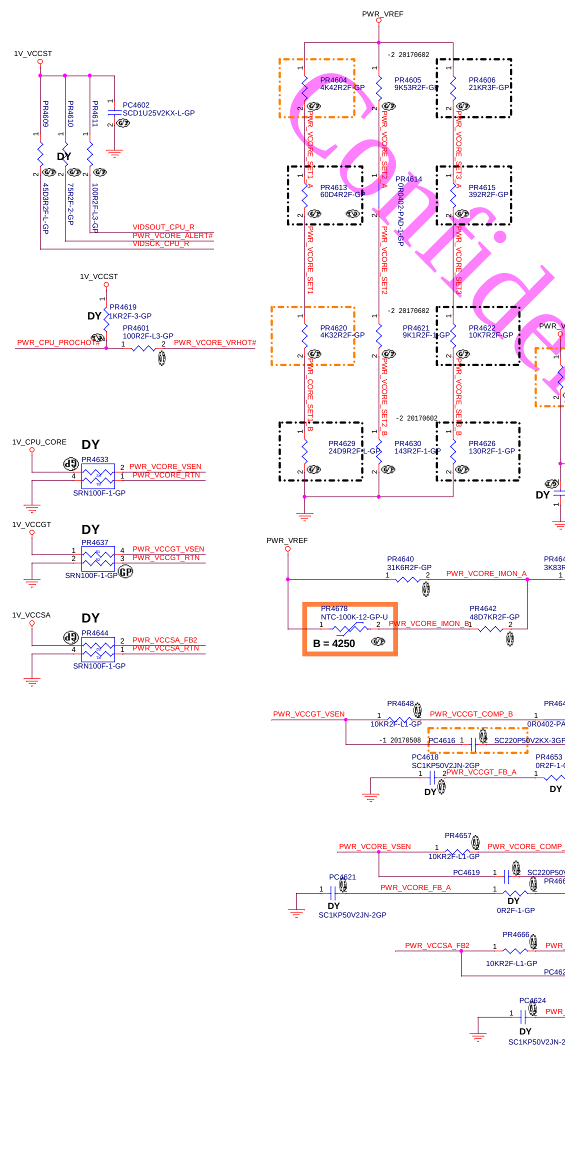
Main Func = CPU_CORE

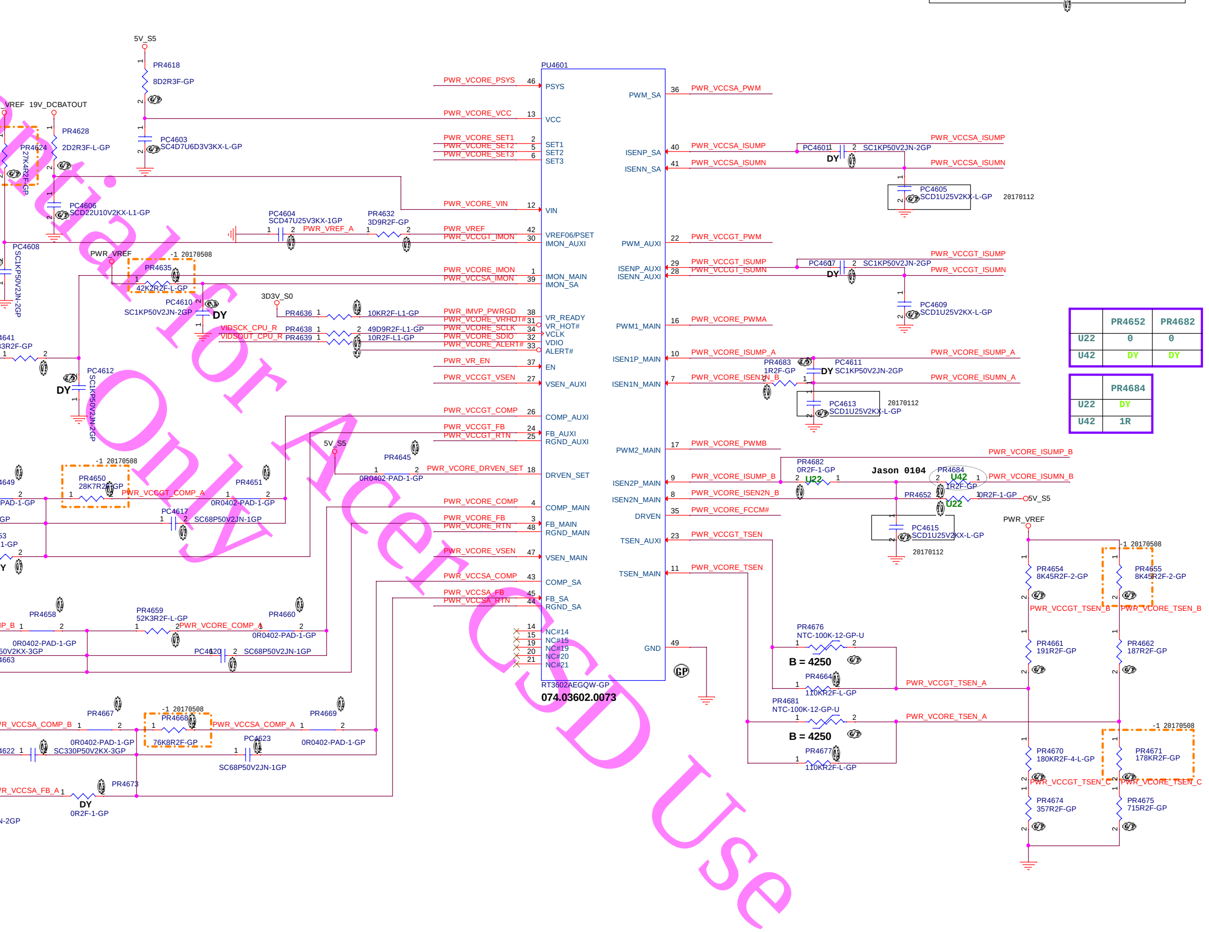
BOM control				
Location	U22		U42	
PR4604	4.42K	64.44215.6DL	4.42K	64.44215.6DL
PR4605	9.53K	64.95315.6DL	26.1K	64.26125.6DL
PR4606	18K	64.18025.55L	18K	64.18025.55L
PR4615	665ohm	64.66505.6DL	665ohm	64.66505.6DL
PC4616	220PF	78.22124.2FL	220PF	78.22124.2FL
PR4620	4.32K	64.43215.6DL	4.32K	64.43215.6DL
PR4621	9.1K	64.91015.6DL	5.62K	64.56215.6DL
PR4622	8.66K	64.86615.6DL	8.66K	64.86615.6DL
PR4624	27.4K	64.27425.6DL	27.4K	64.27425.6DL
PR4635	42.2K	64.42225.6DL	42.2K	64.42225.6DL
PR4640	28K	64.28025.6DL	31.6K	64.31625.6DL
PR4650	28.7K	64.28725.6DL	28.7K	64.28725.6DL
PR4655	8.45K	64.84515.6DL	8.45K	64.84515.6DL
PR4659	47.5k	64.47525.6DL	52.3K	64.52325.6DL
PR4668	76.8K	64.76825.6DL	76.8K	64.76825.6DL
PR4671	178K	64.17835.6DL	178K	64.17835.6DL

OFFPAGE









	PR4652	PR4682
U22	0	0
U42	DY	DY

	PR4684
U22	DY
U42	1R

Count

緯創資通 **Wistron Corporation**
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Title	CPU_VCORE(1/3)	
Size Custom	Document Number Woody/Buzz_KBL	Rev -2
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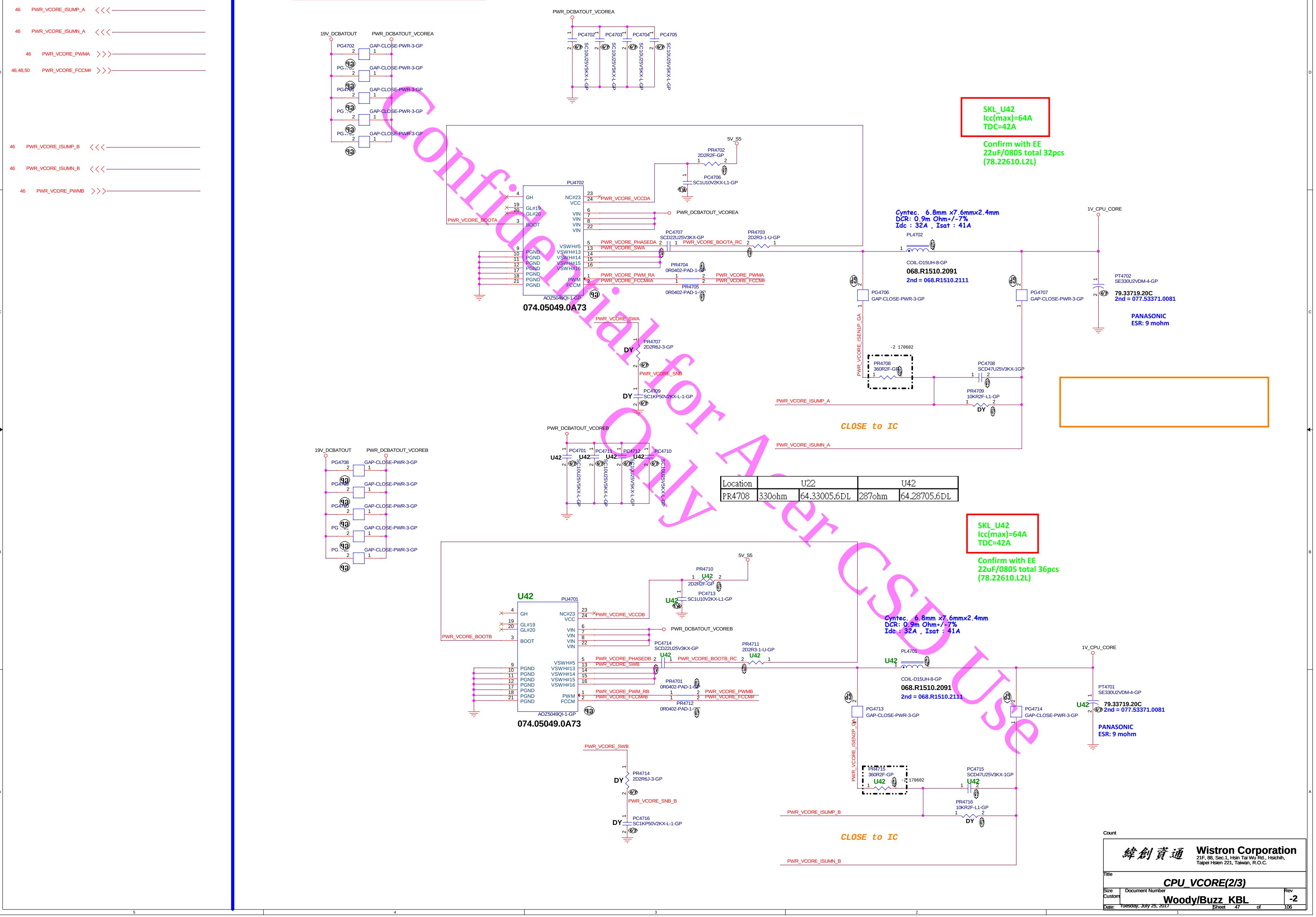
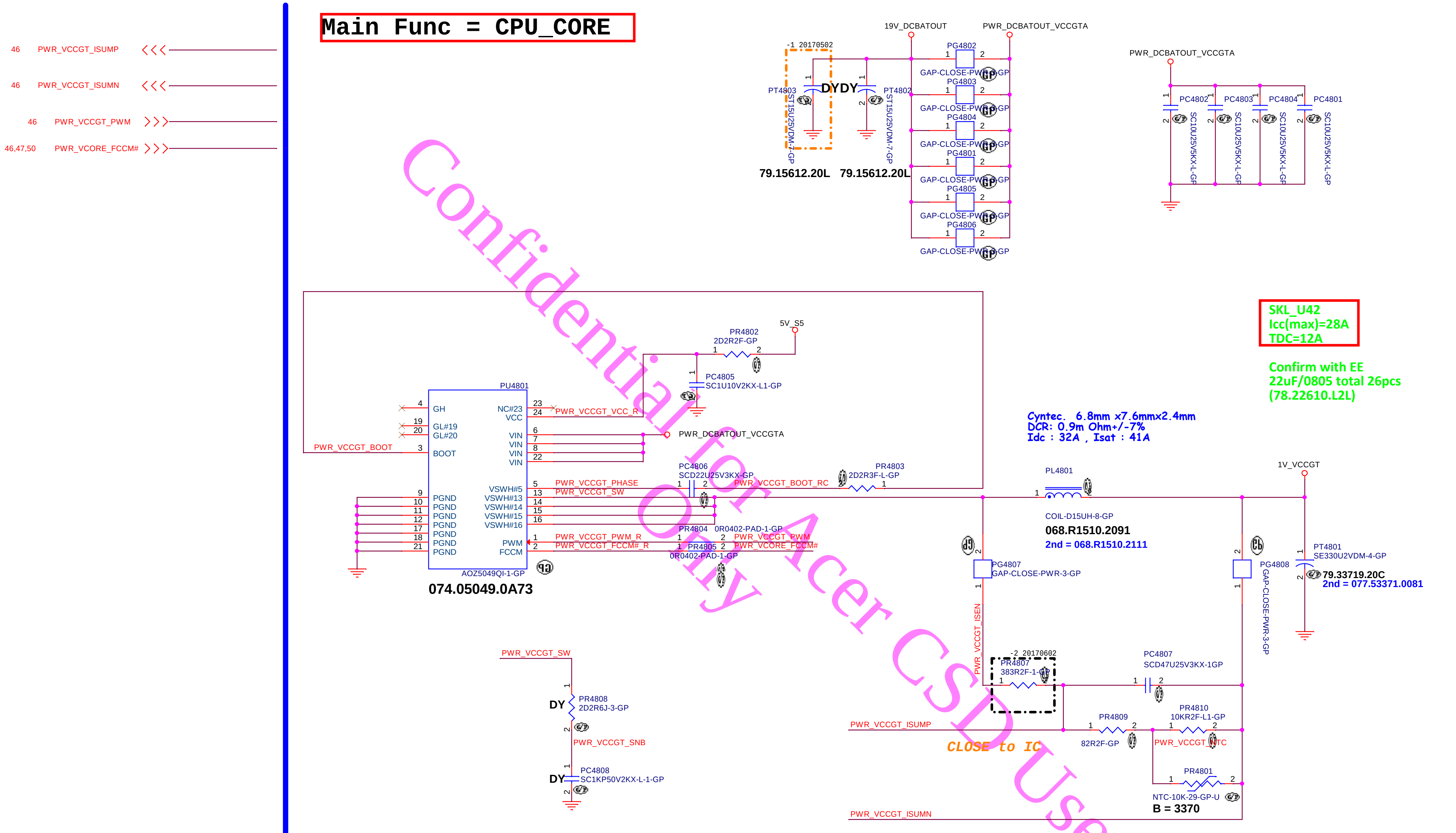
Main Func = CPU_CORE



Location	U22		U42	
PR4708	330ohm	64.33005.6DL	287ohm	64.28705.6DL

Main Func = CPU_CORE



Location	U22		U42	
PR4807	430ohm	64.43005.6DL	324ohm	64.32405.6DL

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_VCCGT(3/3)**

Size: A3 | Document Number: **Woody/Buzz_KBL** | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 48 of 106

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **Woody/Buzz_KBL** — Rev **-2**
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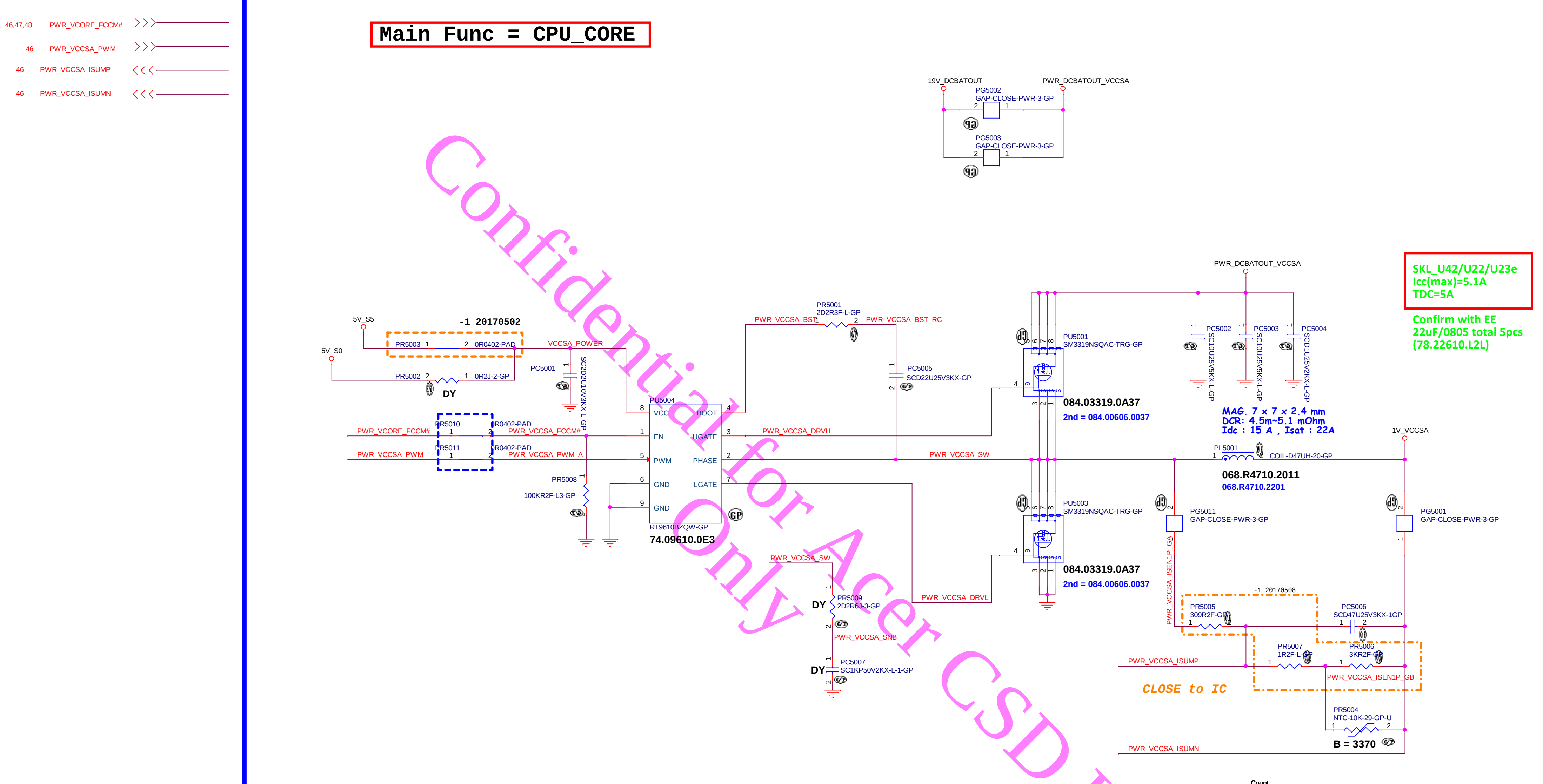
Main Func = CPU_CORE



Count

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA	
Size Custom	Document Number Woody/Buzz_KBL	Rev -2
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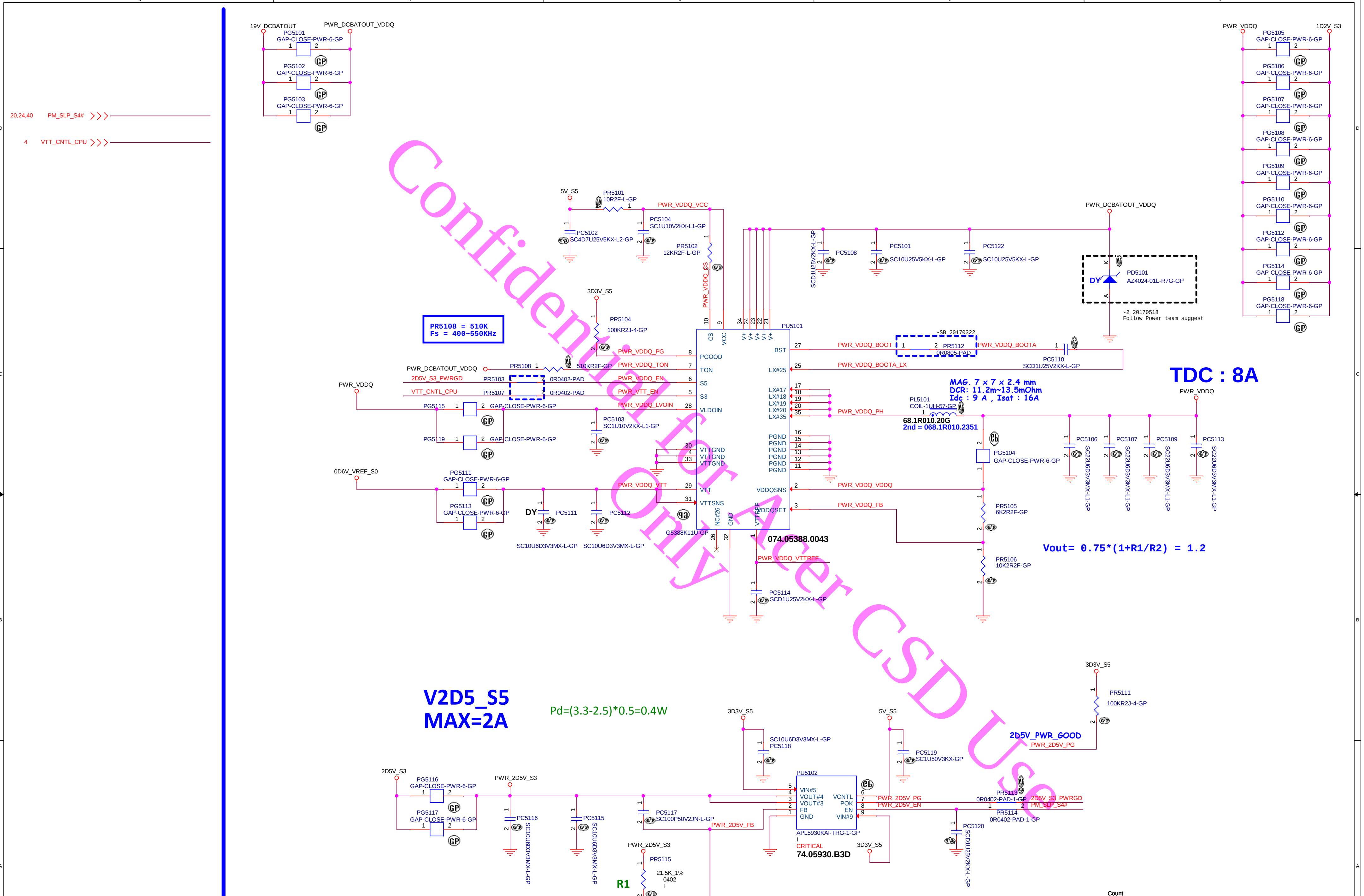

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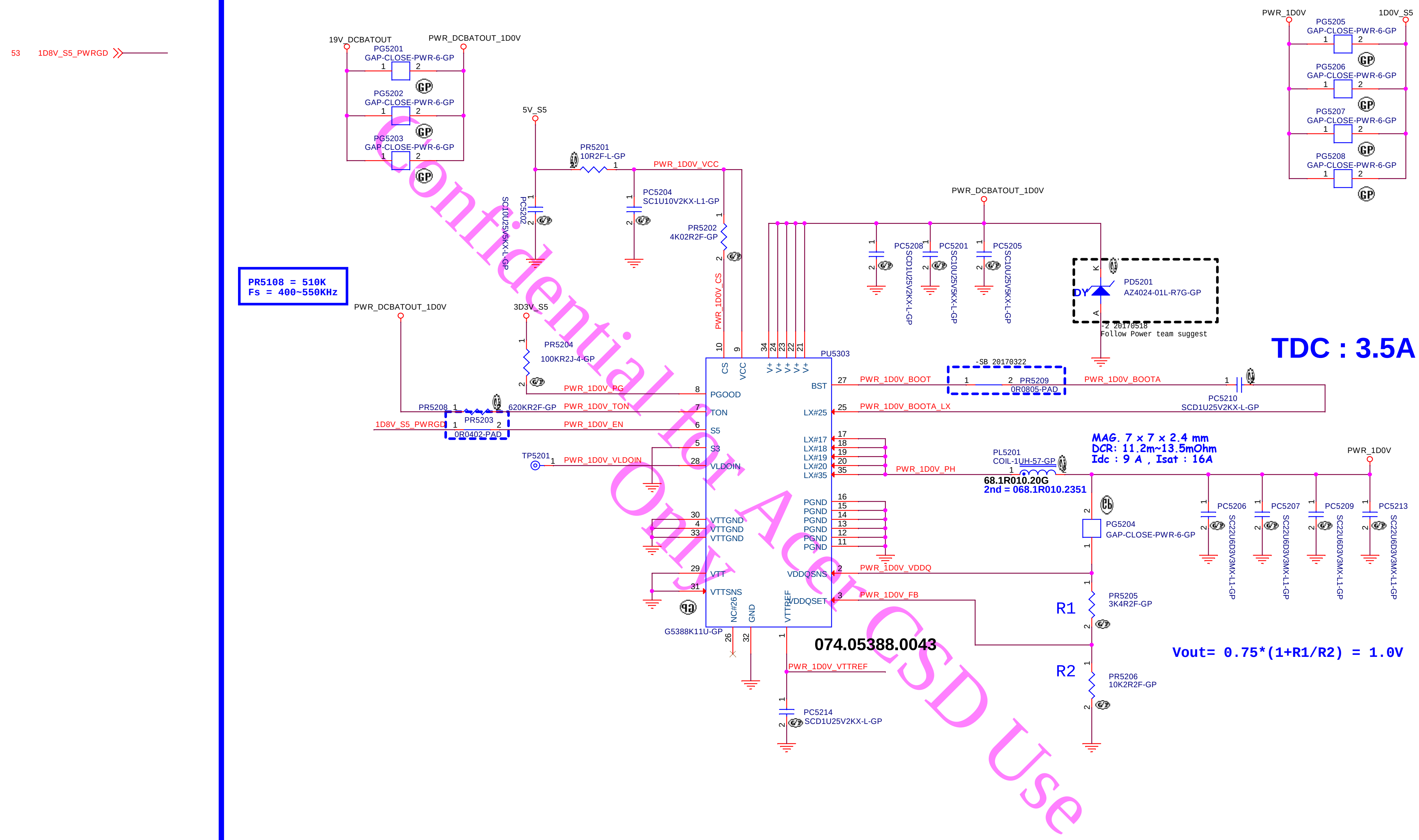
Title: G5388K&RT8068A_VDDQ/VTT

Size	Document Number	Rev
Custom	Woody/Buzz_KBL	-2

Date: Tuesday, July 25, 2017 Sheet 51 of 106



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Title	G5388K_1D0V	
Size A3	Document Number: Woody/Buzz_KBL	Rev -2
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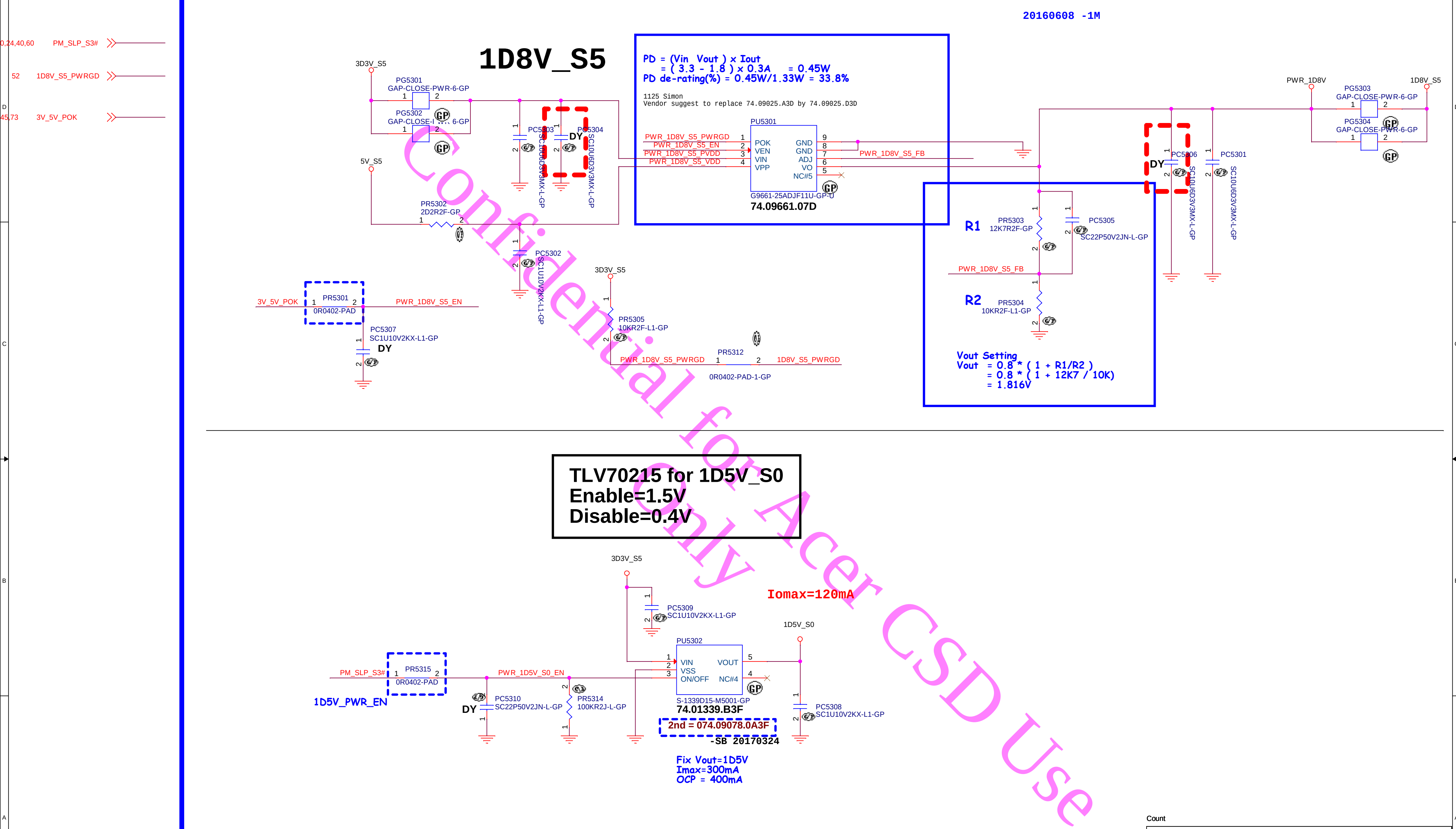

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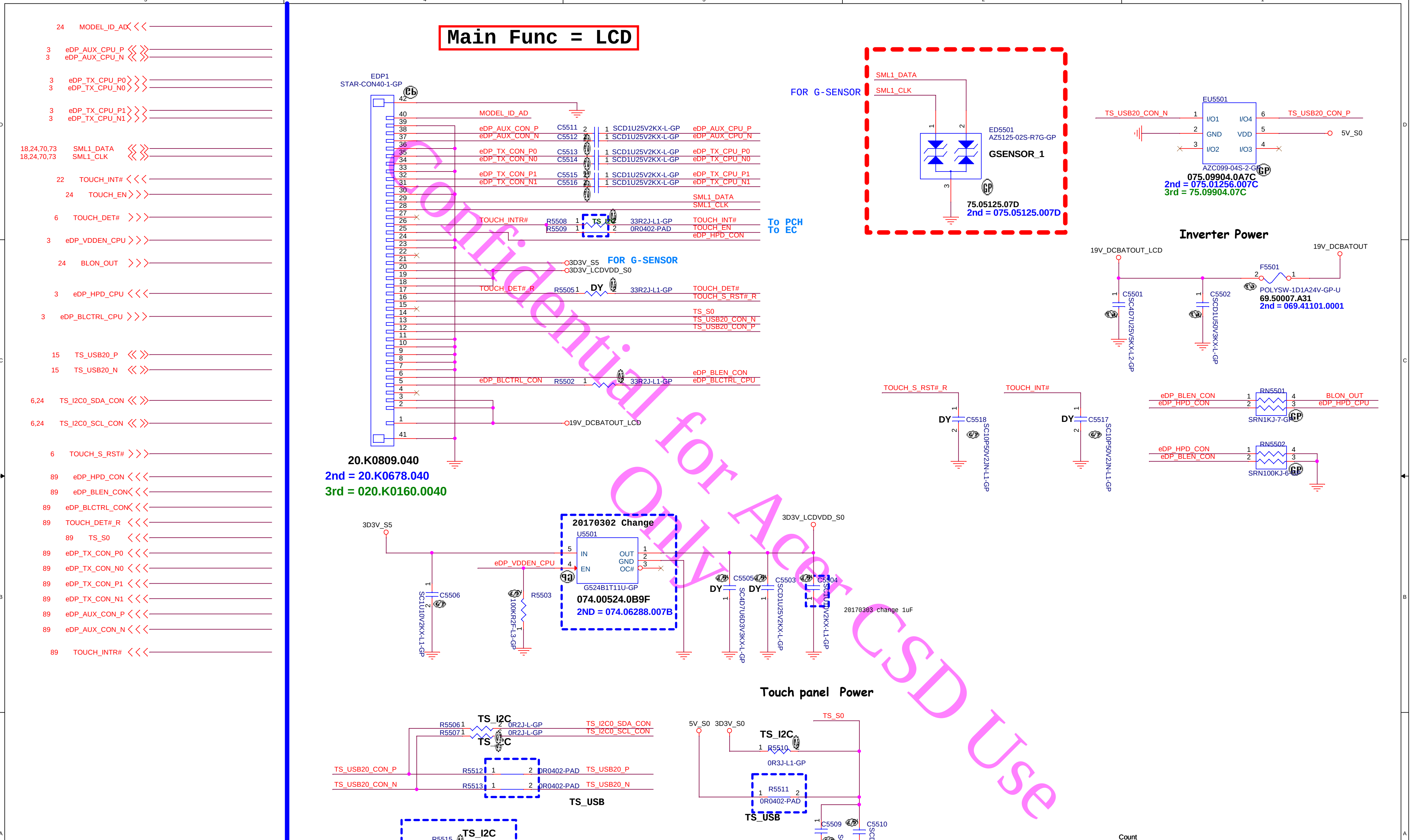

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Size Custom	Document Number Woody/Buzz_KBL		Rev -2
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Title	***Reserved***
Size A4	Document Number **Woody/Buzz_KBL** — Rev **-2**
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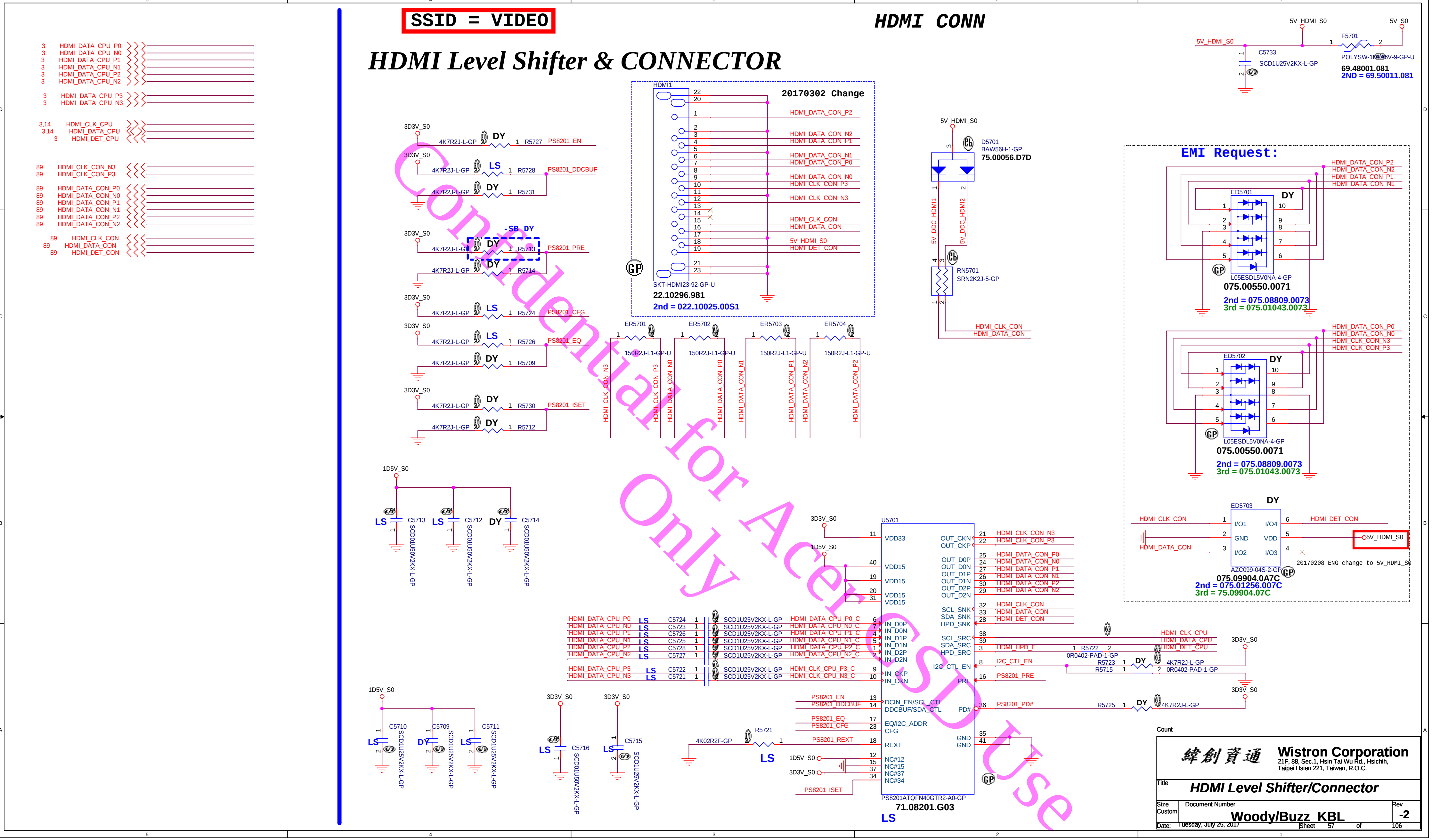

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Title: HDMI Level Shifter/Connector

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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Size A4	Document Number **Woody/Buzz_KBL** Rev **-2**
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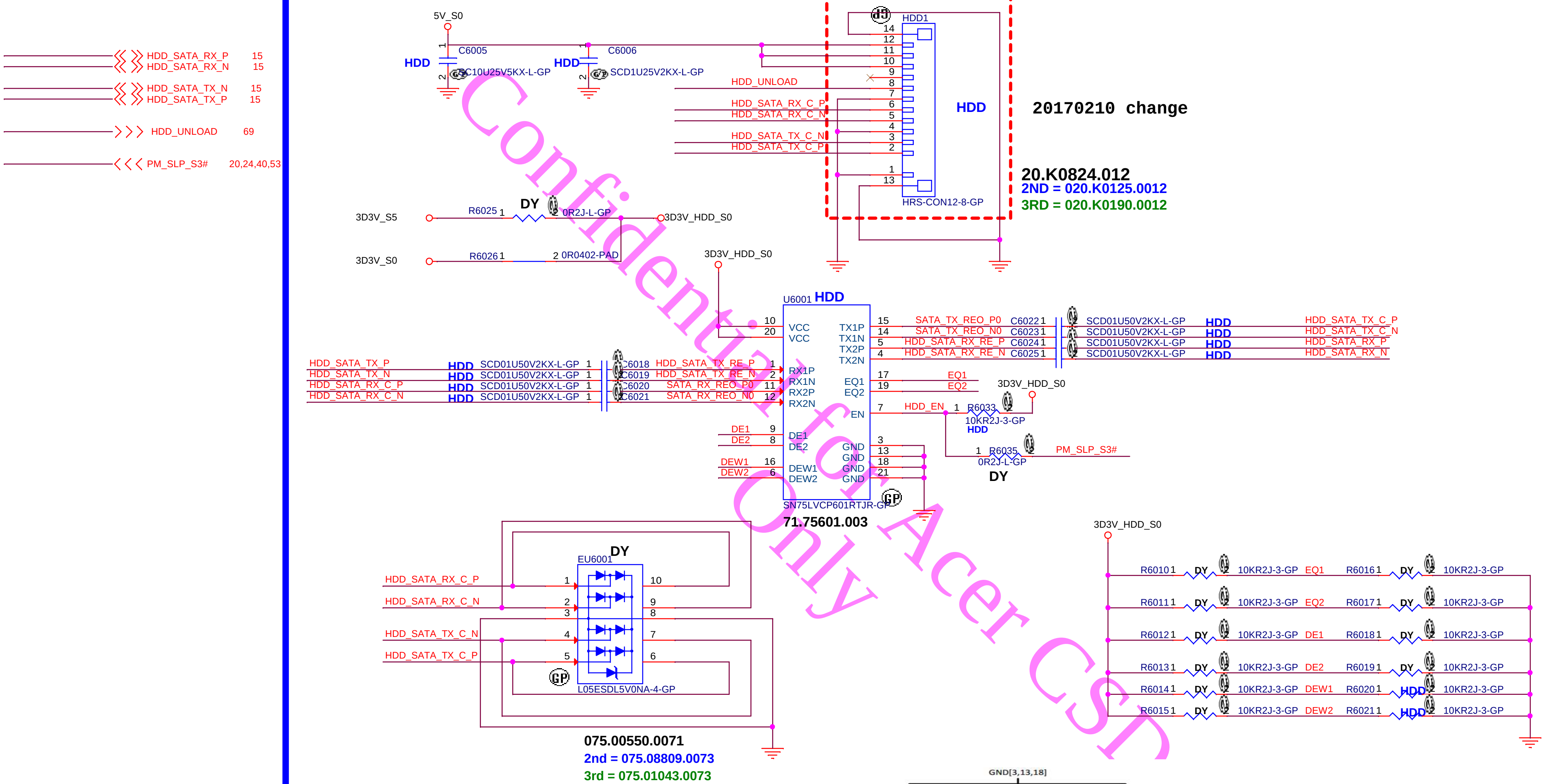
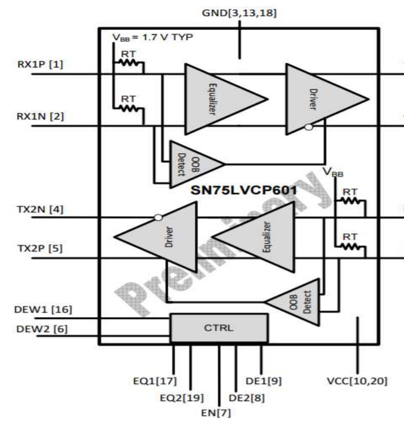
SATA HDD Connector

SSID = SATA





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Title	HDD_GSENSOR	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
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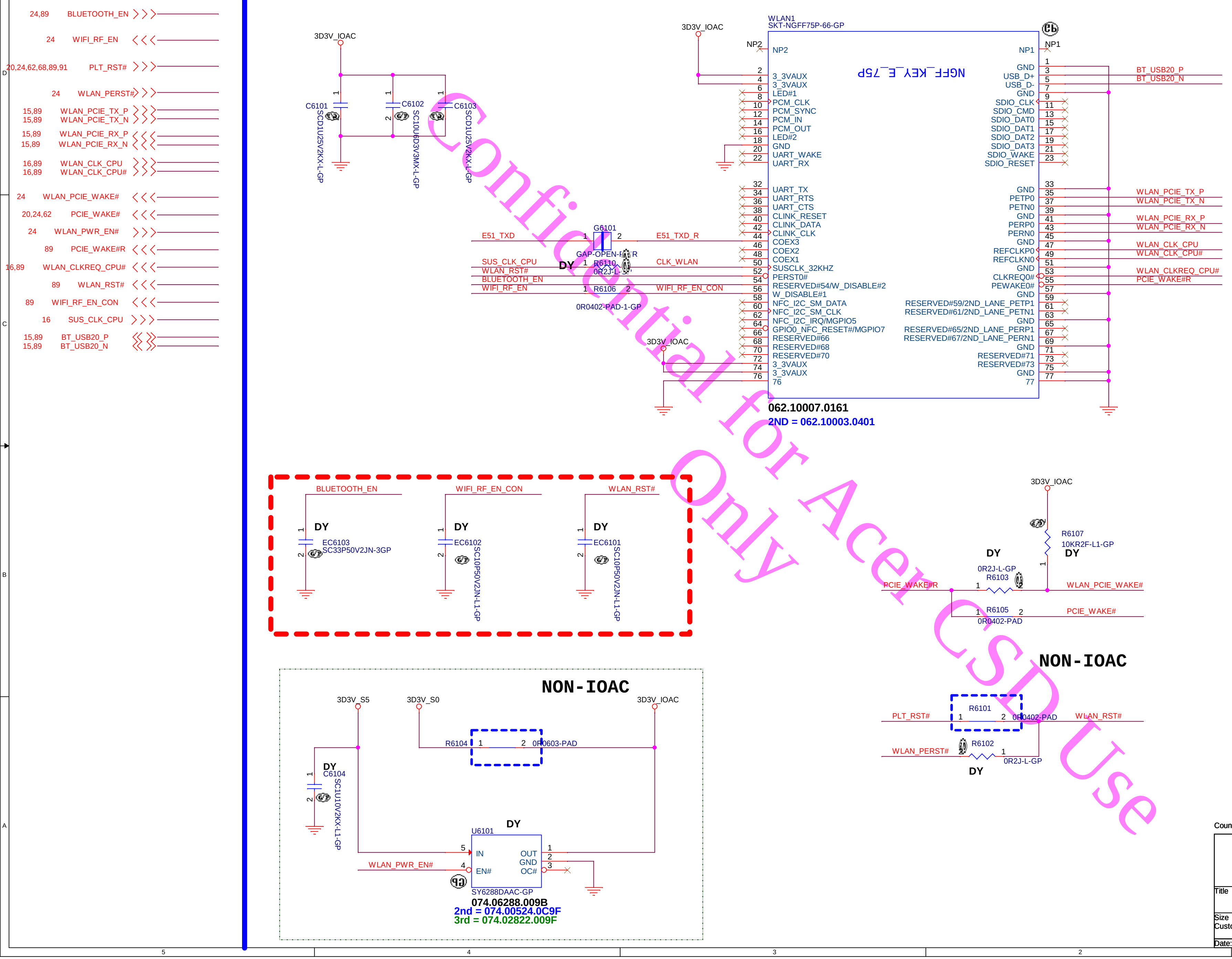
SSID = Wireless Mini Card Connector(802.11a/b/g/n)



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Title	Mini Card-WLAN
Size Custom	Document Number: Woody/Buzz_KBL
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SSID = mSATA

Mini Card Connector(mSATA)

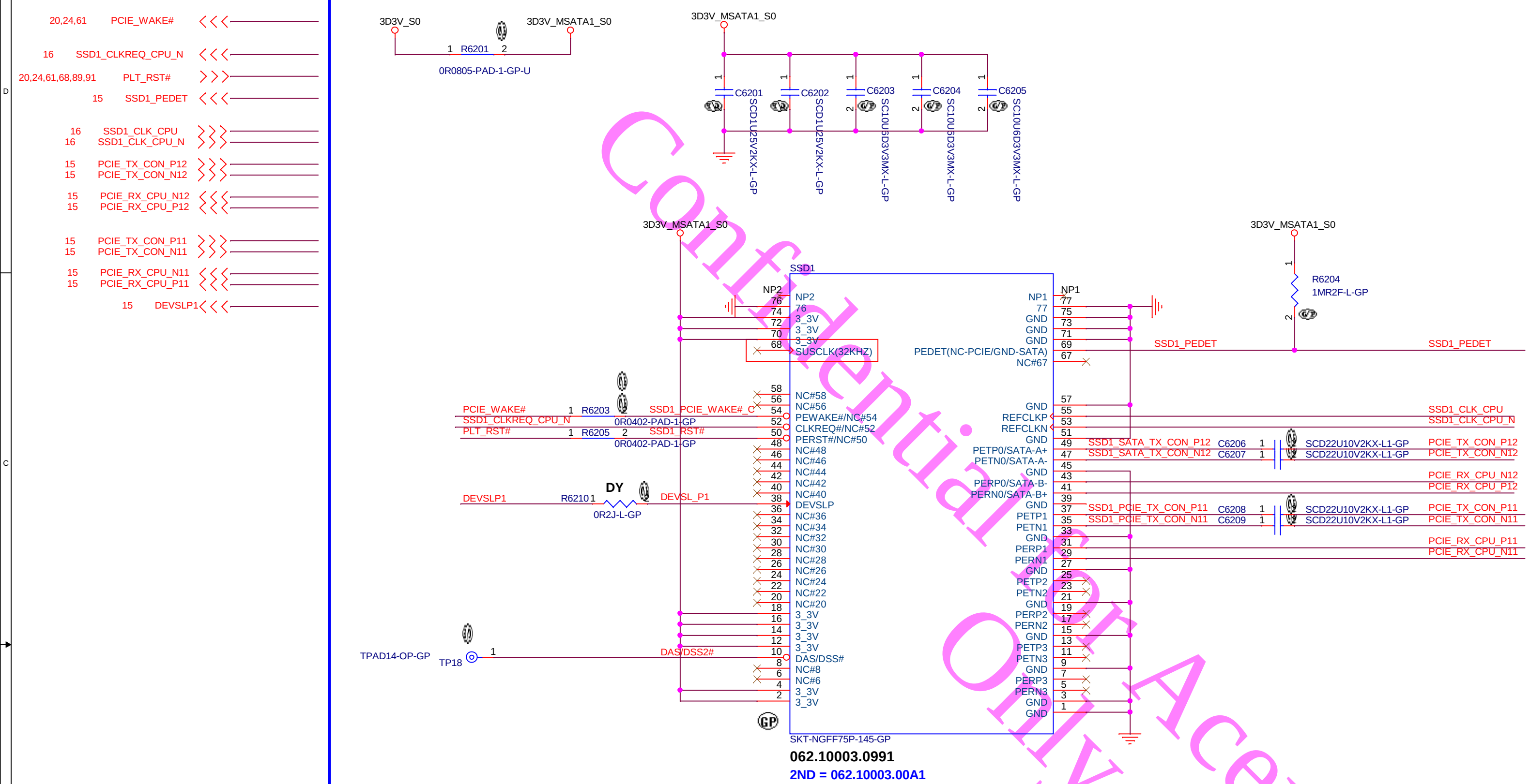

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
	Flex I/O Lane #	5	6	7	8	9	10	11	12	13	14	15	16
	PCIe* Lane #	1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1				RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12
Premium-Y	1x4	RP 1				RP 5							
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9			
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9			
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5				RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10		

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

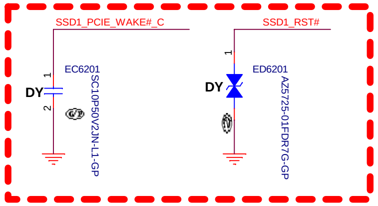

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes: CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

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Size A4	Document Number **Woody/Buzz_KBL**
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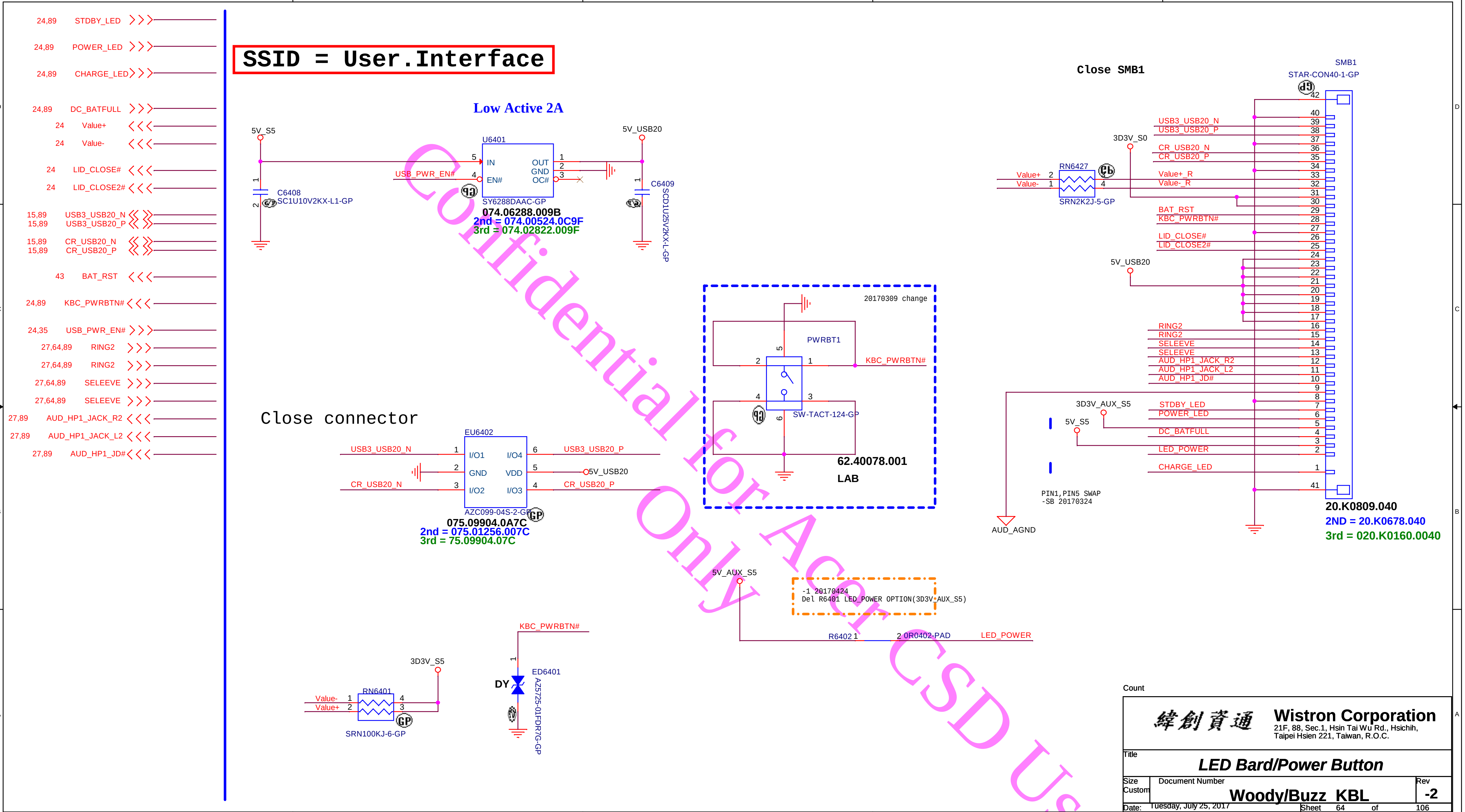

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Title	**LED Bard/Power Button**	
Size Custom	Document Number **Woody/Buzz KBL**	Rev **-2**
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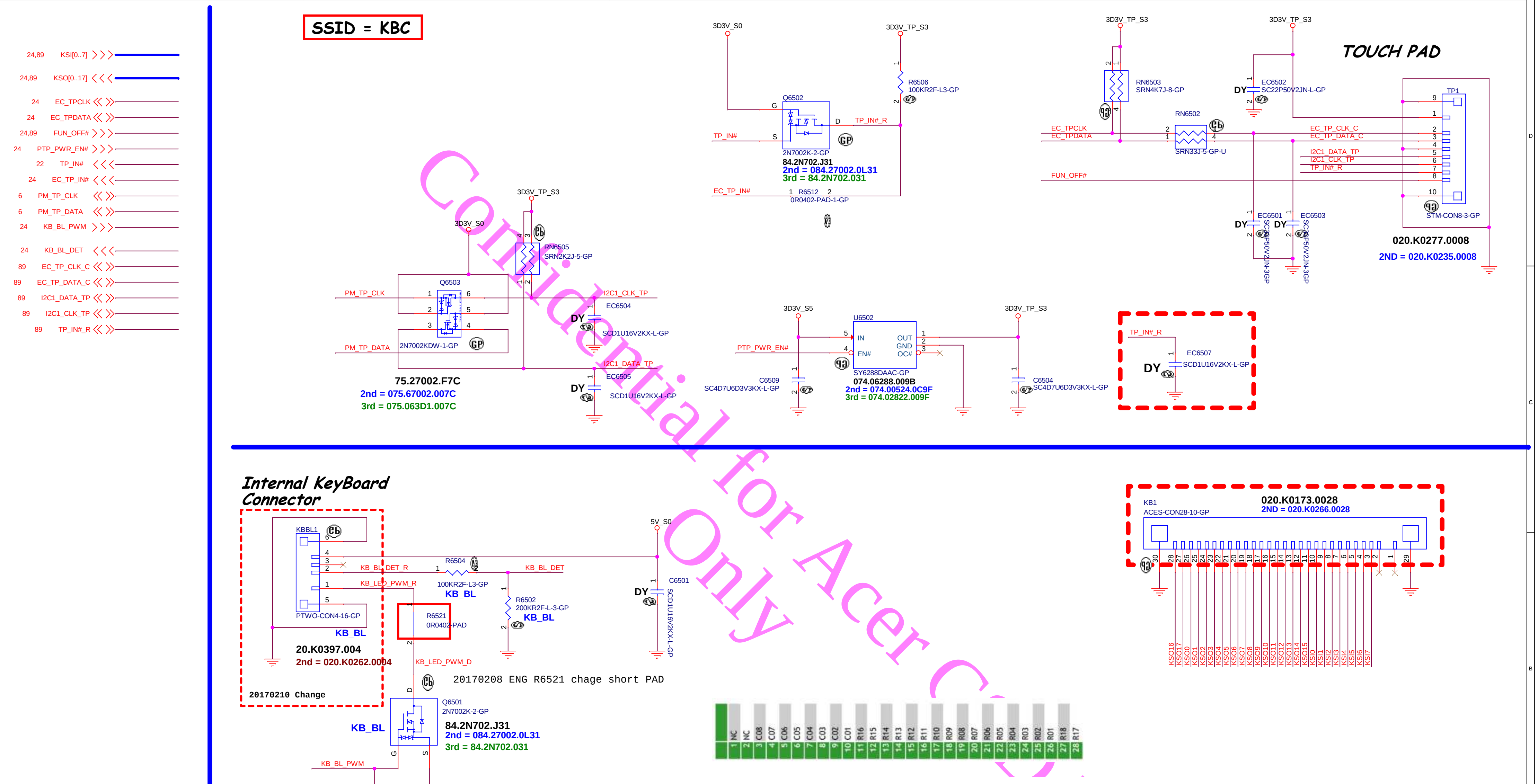

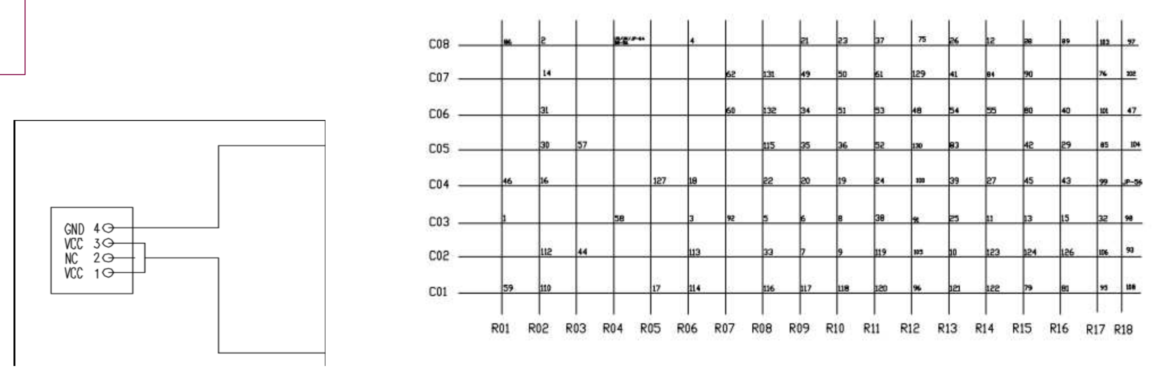

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Title: **Key Board/Touch Pad**

Size	Document Number	Rev
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Size A4	Document Number **Woody/Buzz_KBL** Rev **-2**
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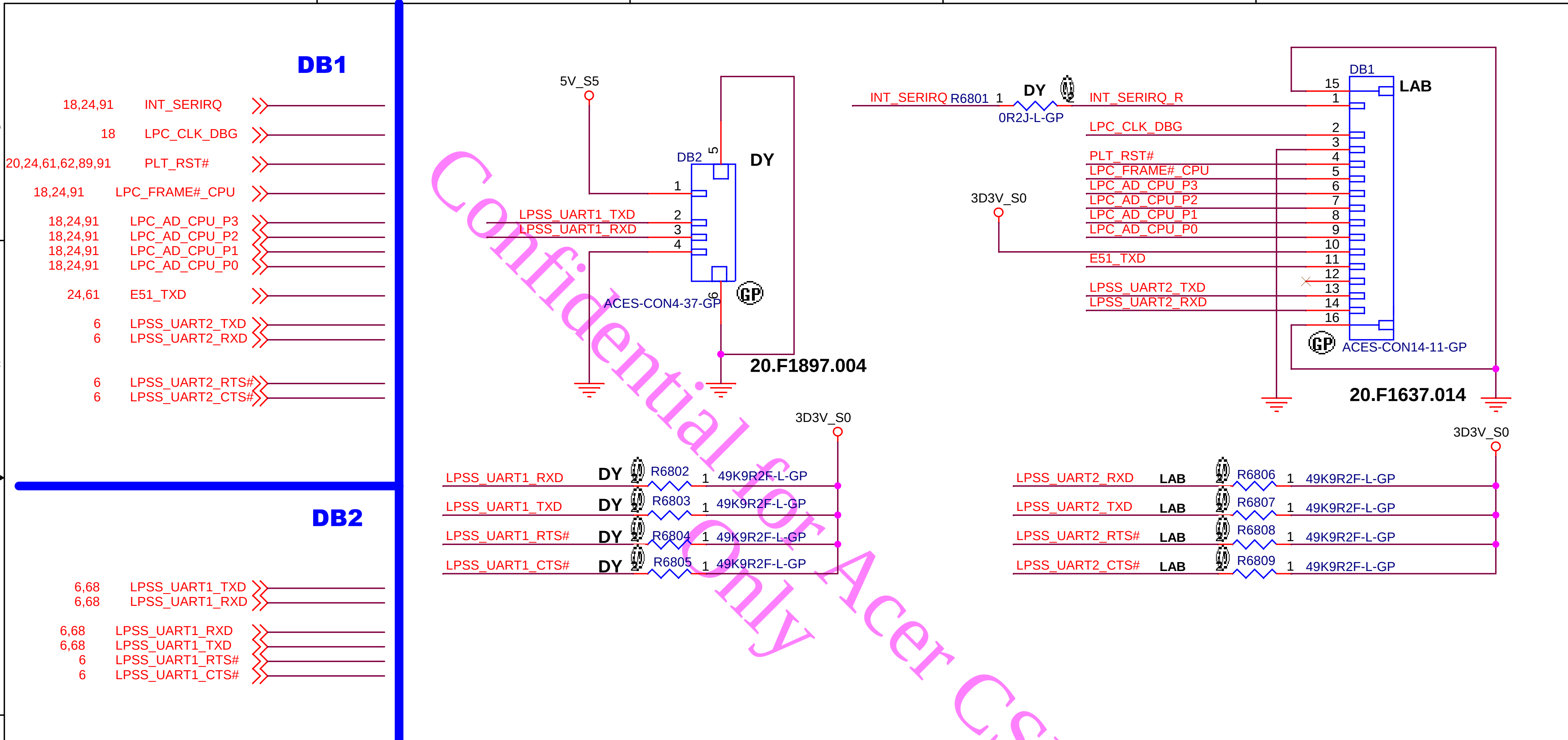

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Size: Custom	Document Number: **Woody/Buzz_KBL**	Rev: **-2**
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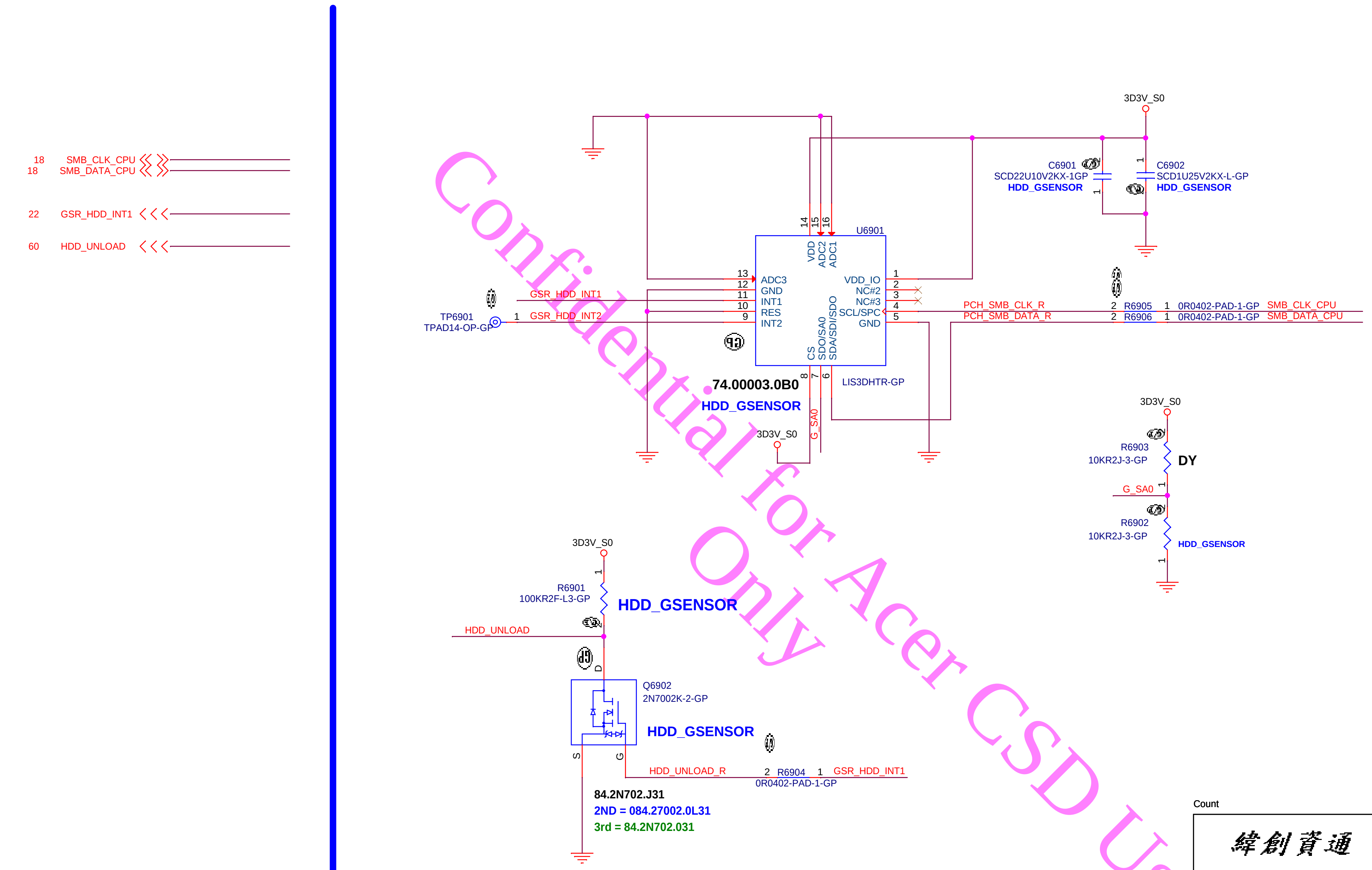

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Title	HDD_G_Sensor	
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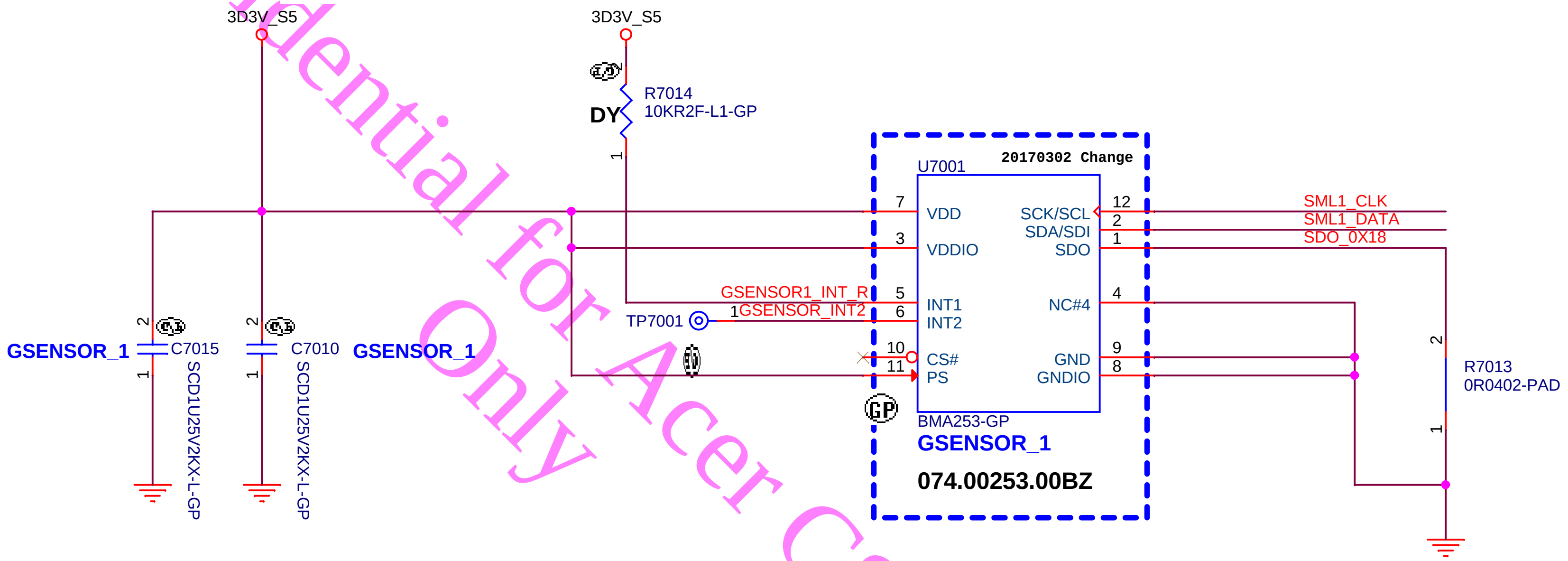
18,24,55,73 SML1_CLK
18,24,55,73 SML1_DATA

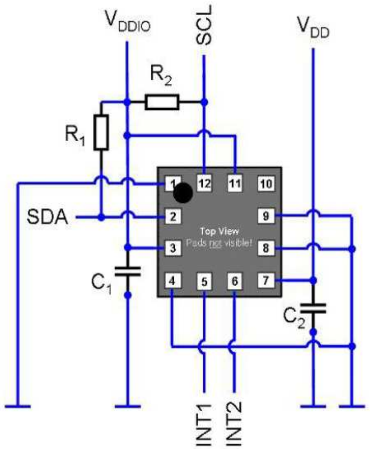
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SSID = User.Interface

G Sensor

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.





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G SENSOR		
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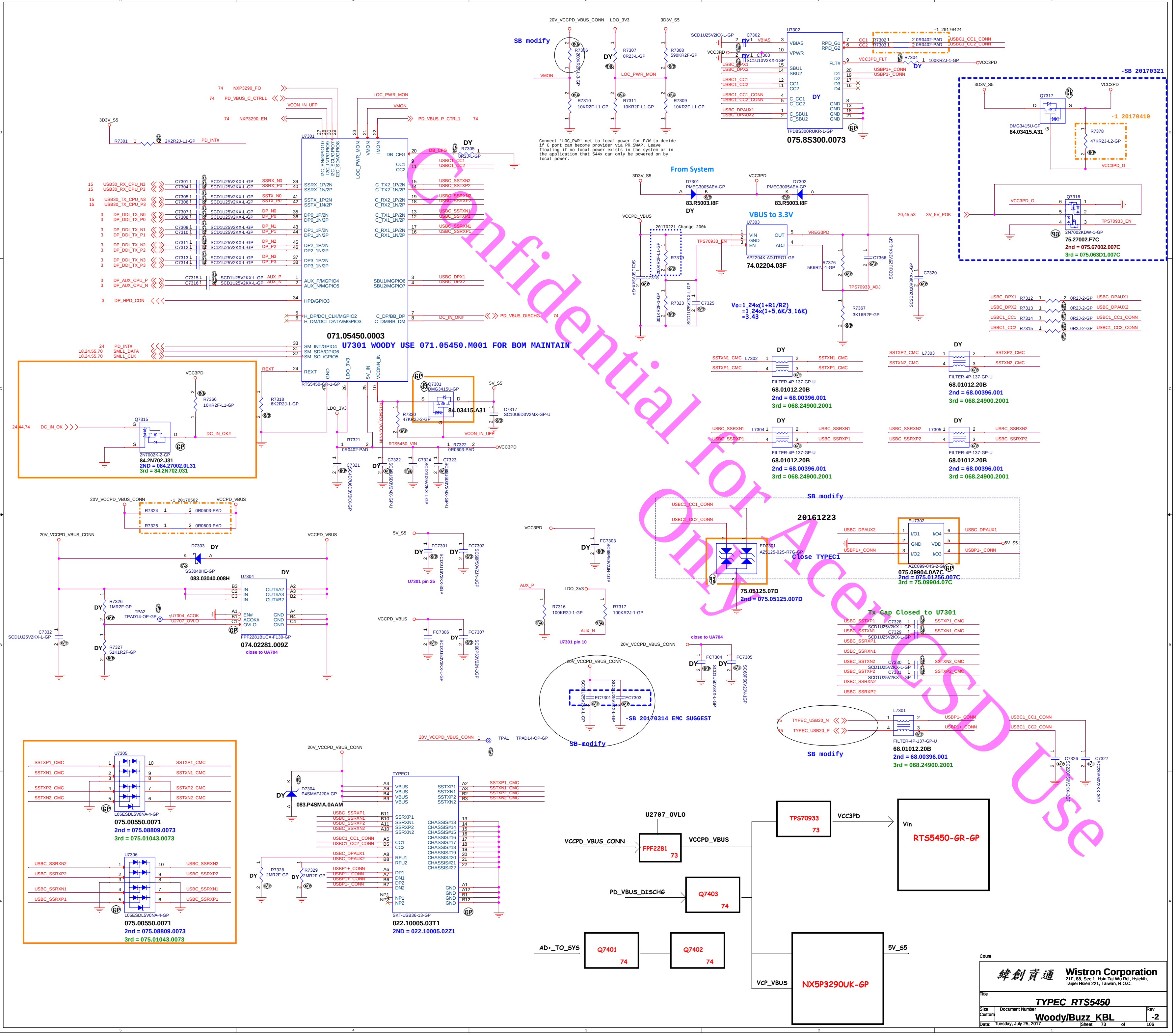

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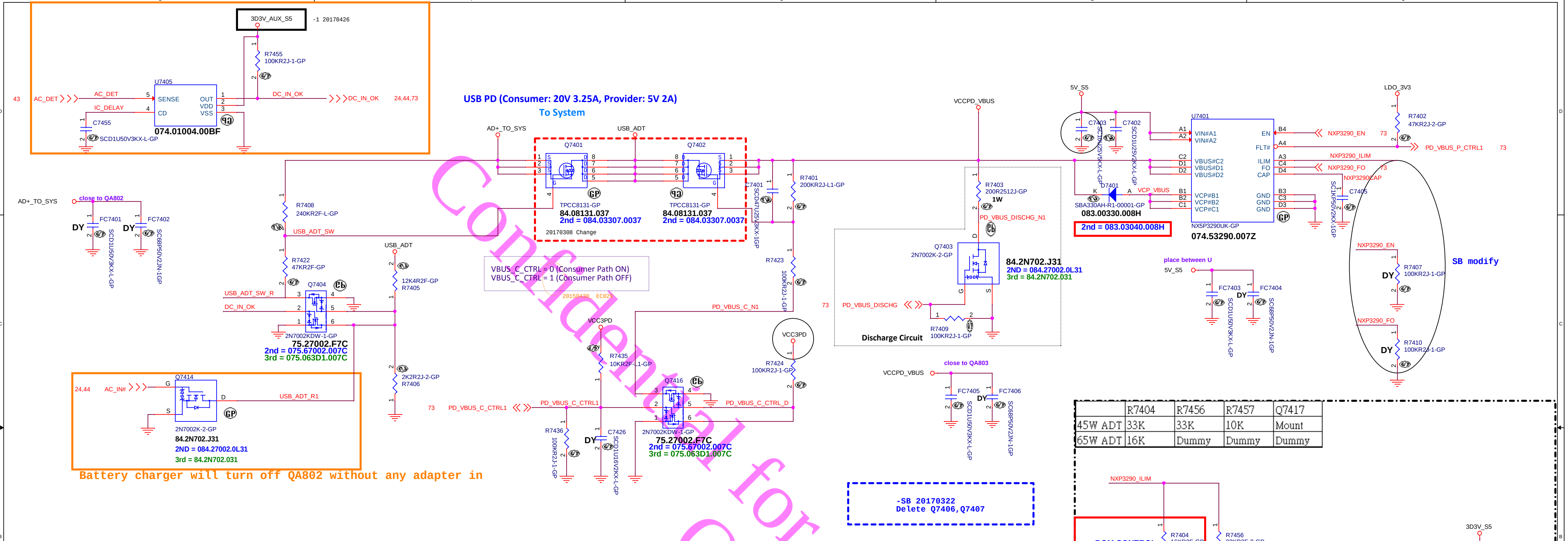

	R7404	R7456	R7457	Q7417
45W ADT	33K	33K	10K	Mount
65W ADT	16K	Dummy	Dummy	Dummy

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	
					Q7402	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT

Count

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Size / Project Name	**Woody/Buzz_KBL**
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Title	GPU_POWER/GND(Reserved)		
Size	Project Name: Woody/Buzz_KBL		Rev: -2
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Title: GPU-VRAM3,4(Reserved)		
Size: A4	Document Number: Woody/Buzz_KBL	Rev: -2
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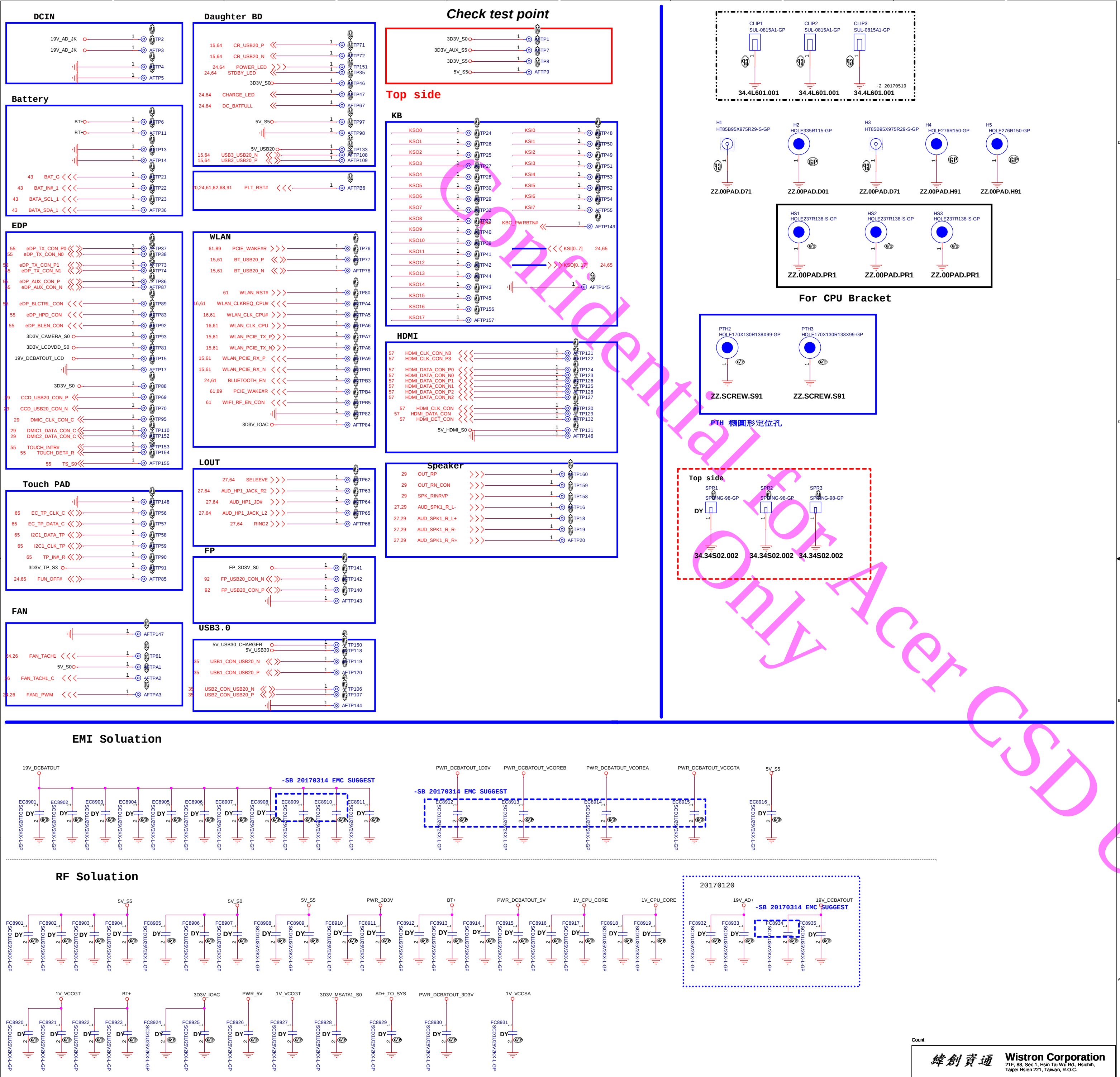

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Title	**UNUSED PARTS/EMI Capacitors**	
Size: Custom	Document Number: **Woody/Buzz_KBL**	Rev: -2
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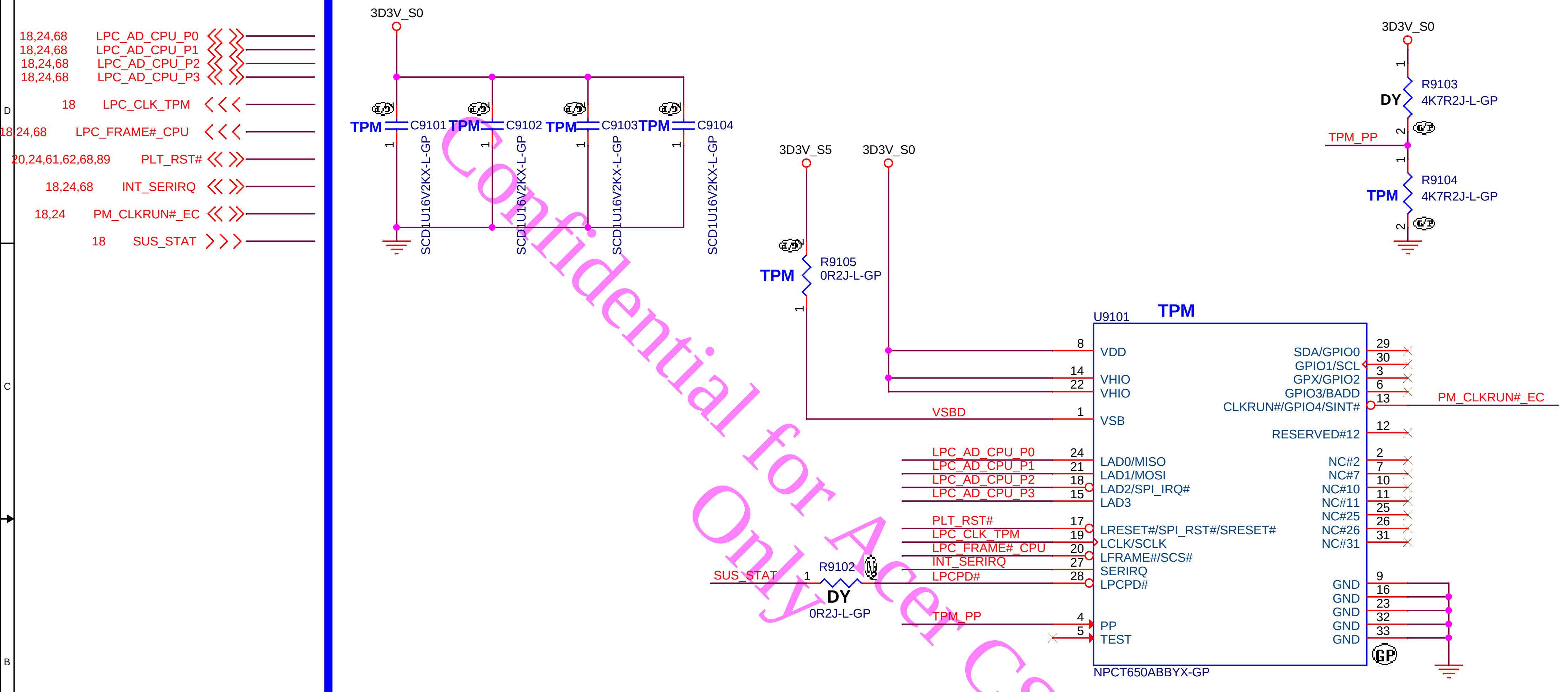

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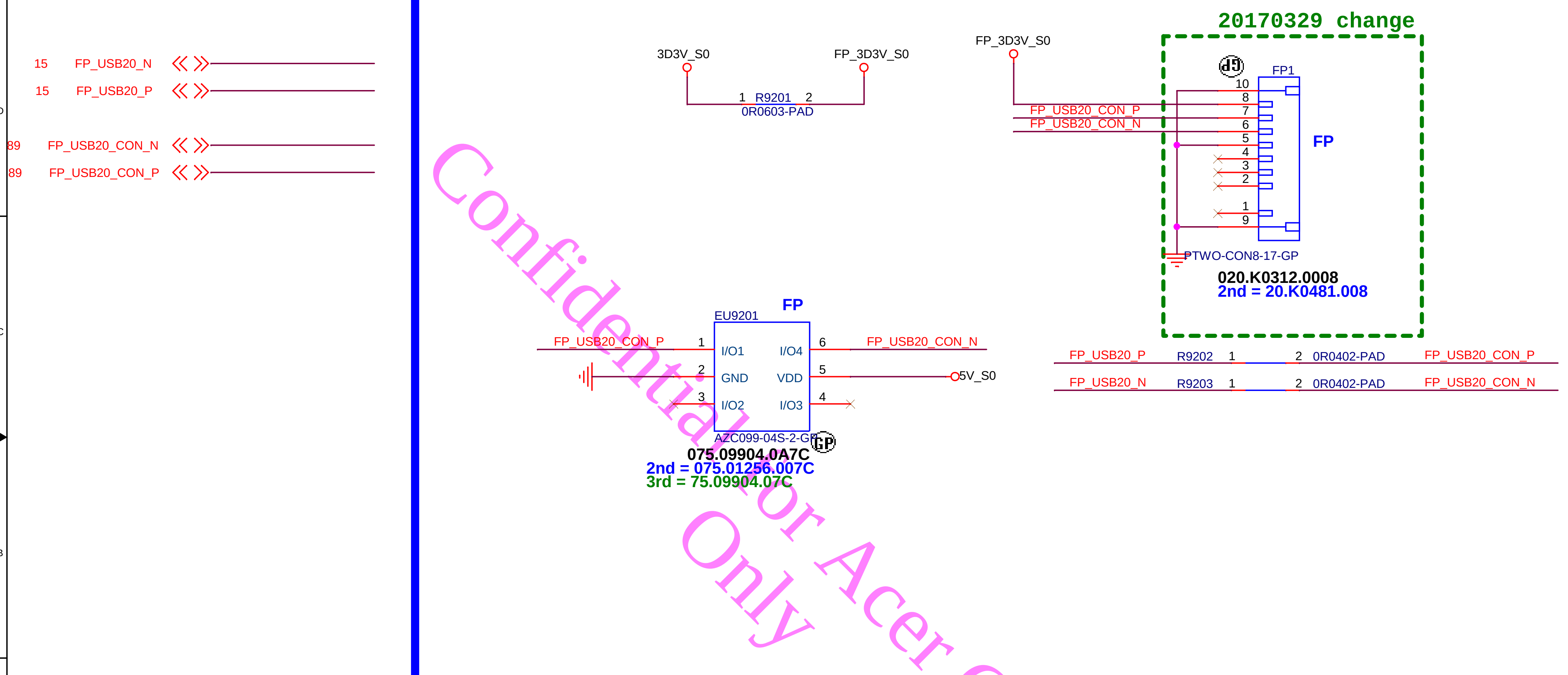

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Title	***Express_Card(Reserved)***
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Title	***Smart Card scoket(Reserved)***
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Title	***GFX eDP(Reserved)***
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Title	***CPU_CFG STRAP(Reserved)***
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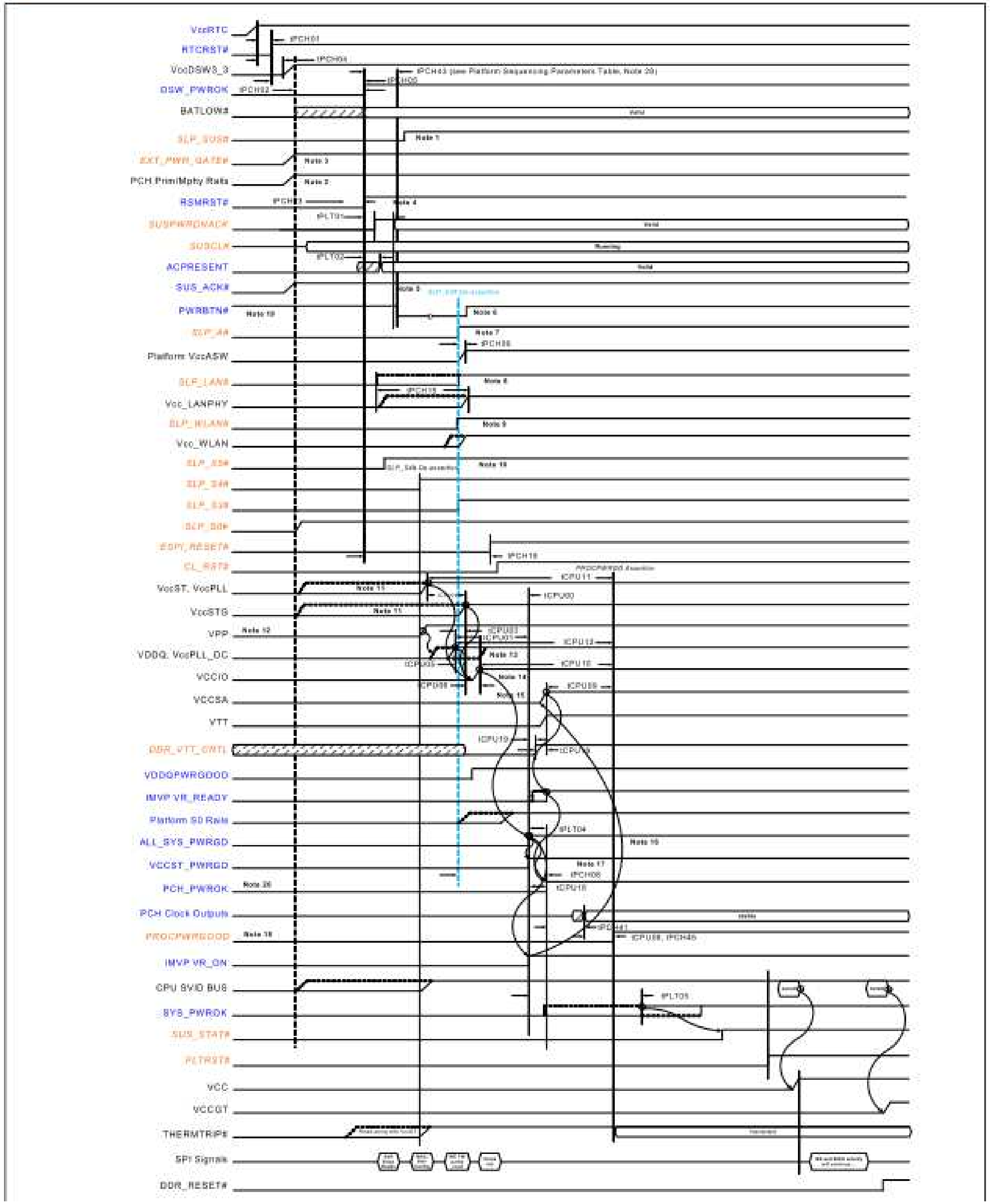
Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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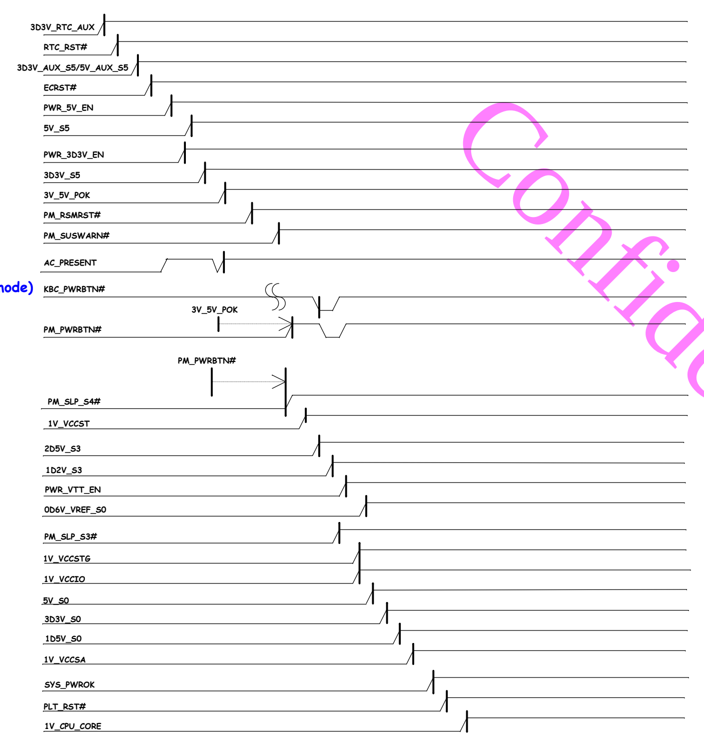
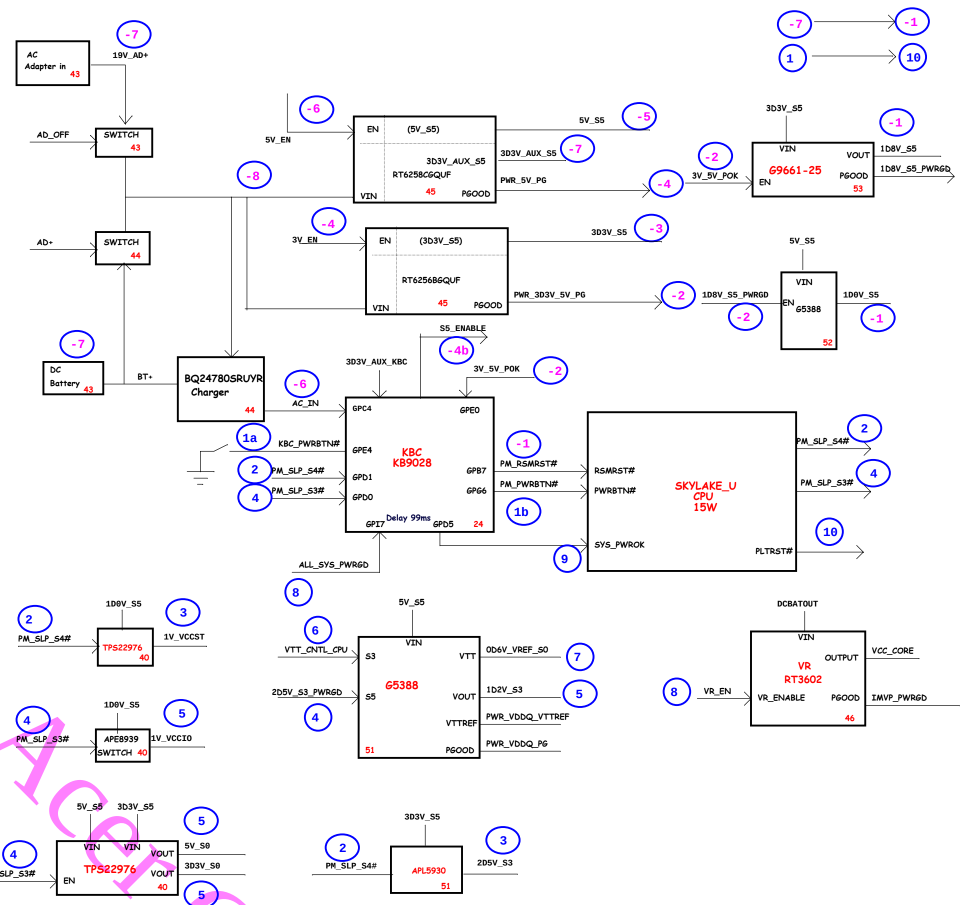
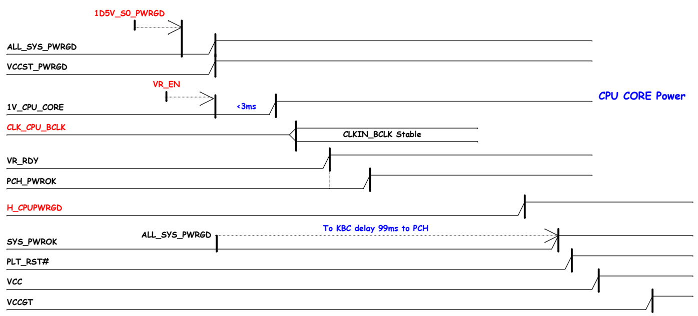
Intel-Power Up Sequence







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Title: Power Sequence
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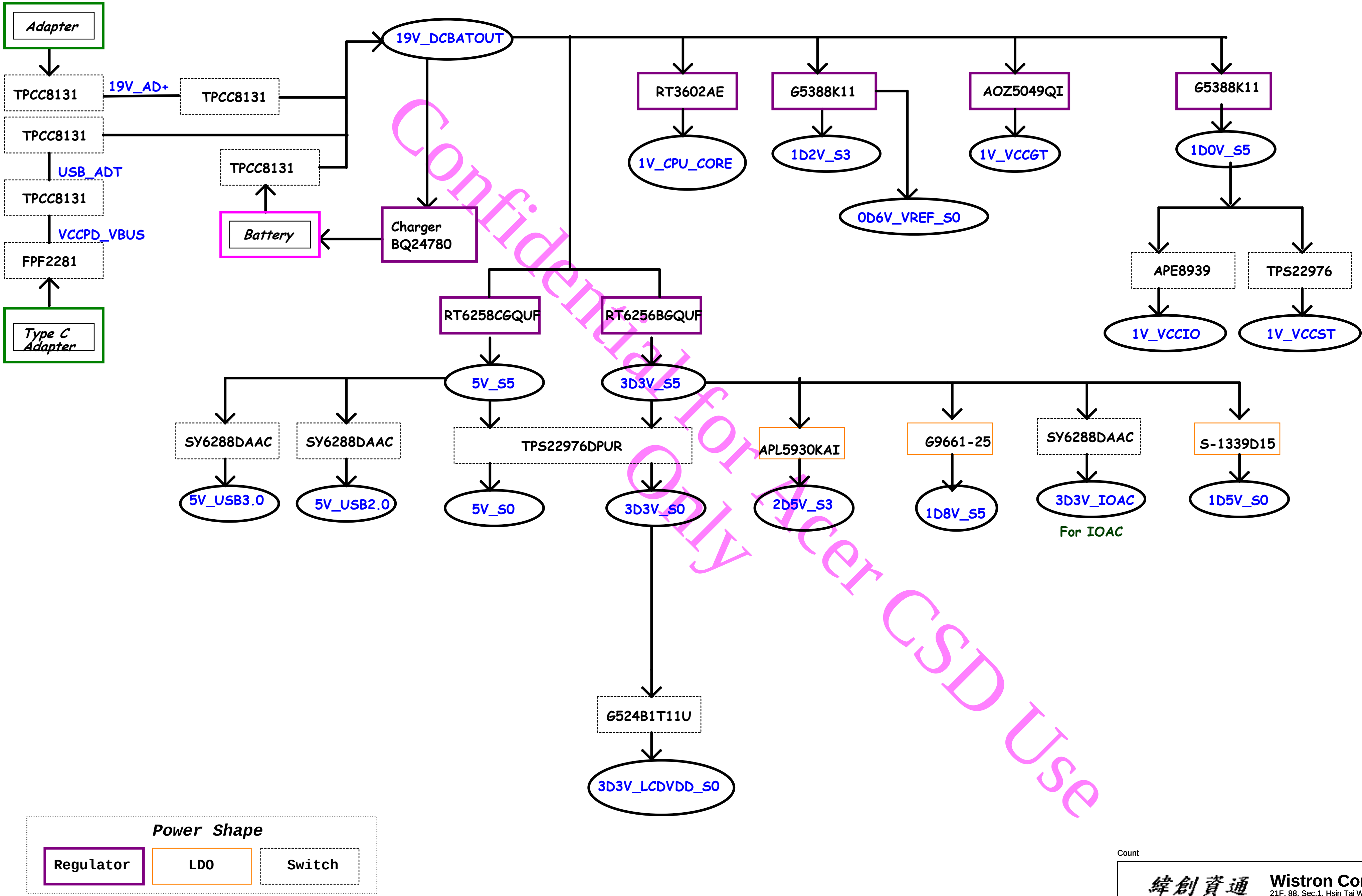

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Title: ***Power Block Diagram***

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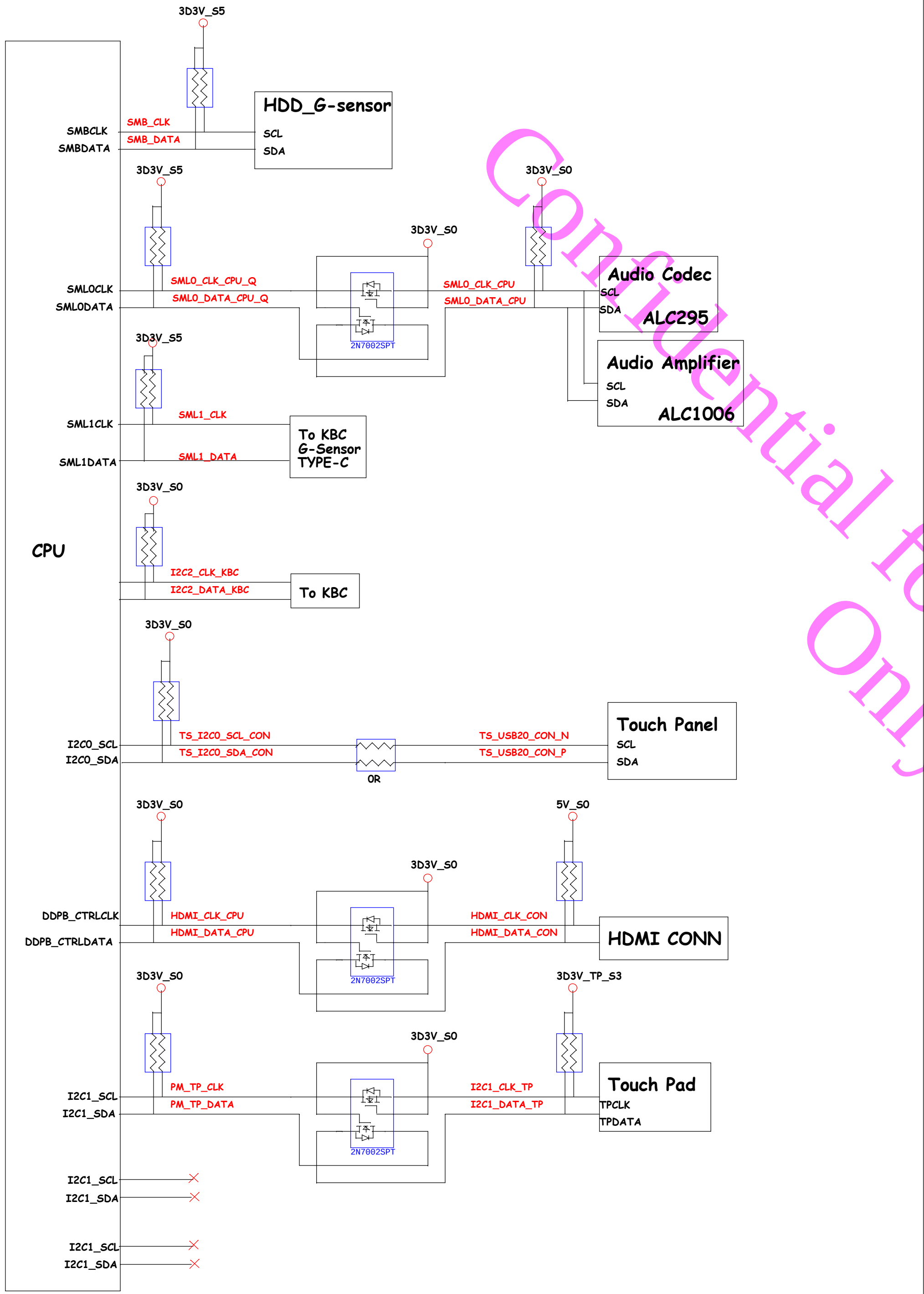
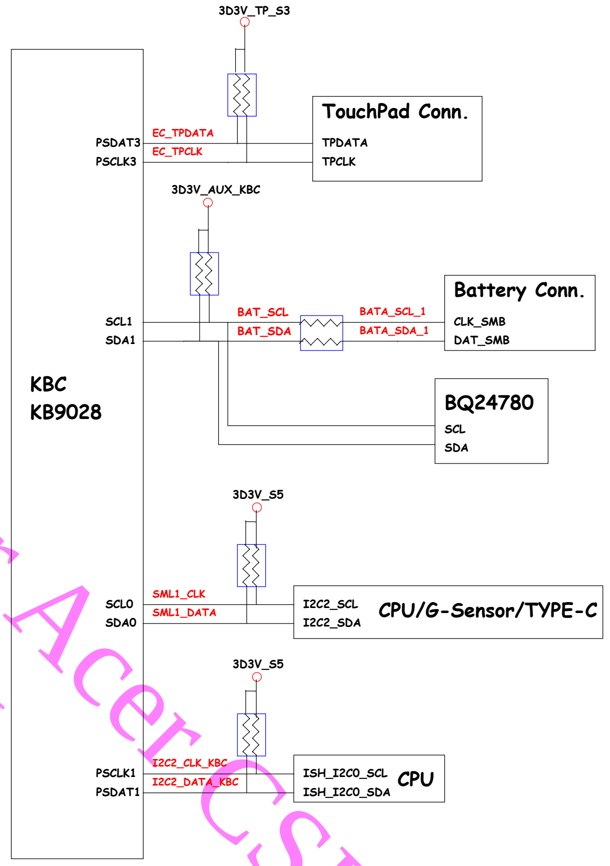
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title	SMBUS BLOCK DIAGRAM
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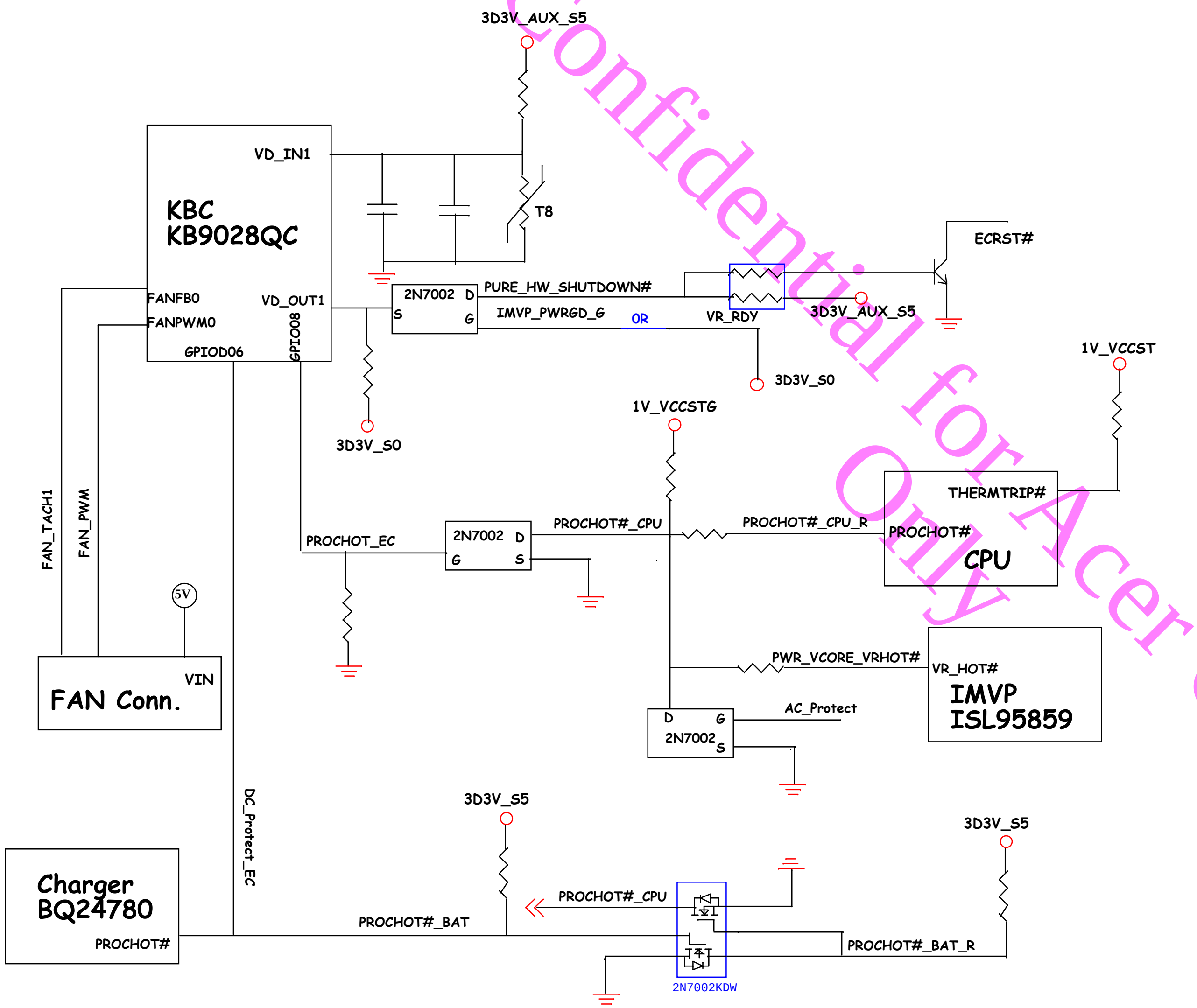
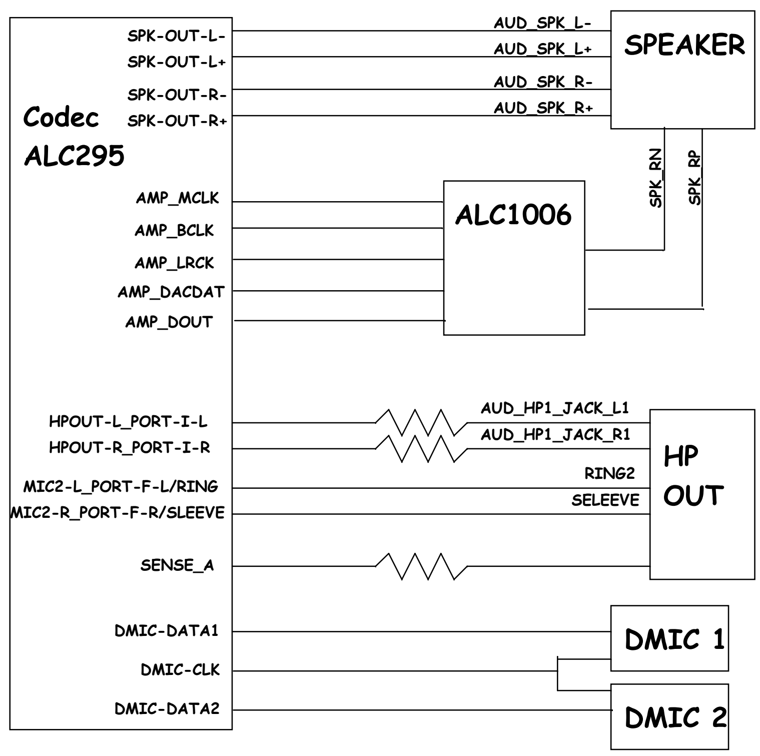
Thermal Block Diagram



Audio Block Diagram



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Title **THERMAL/AUDIO BLOCK DIAGRAM**

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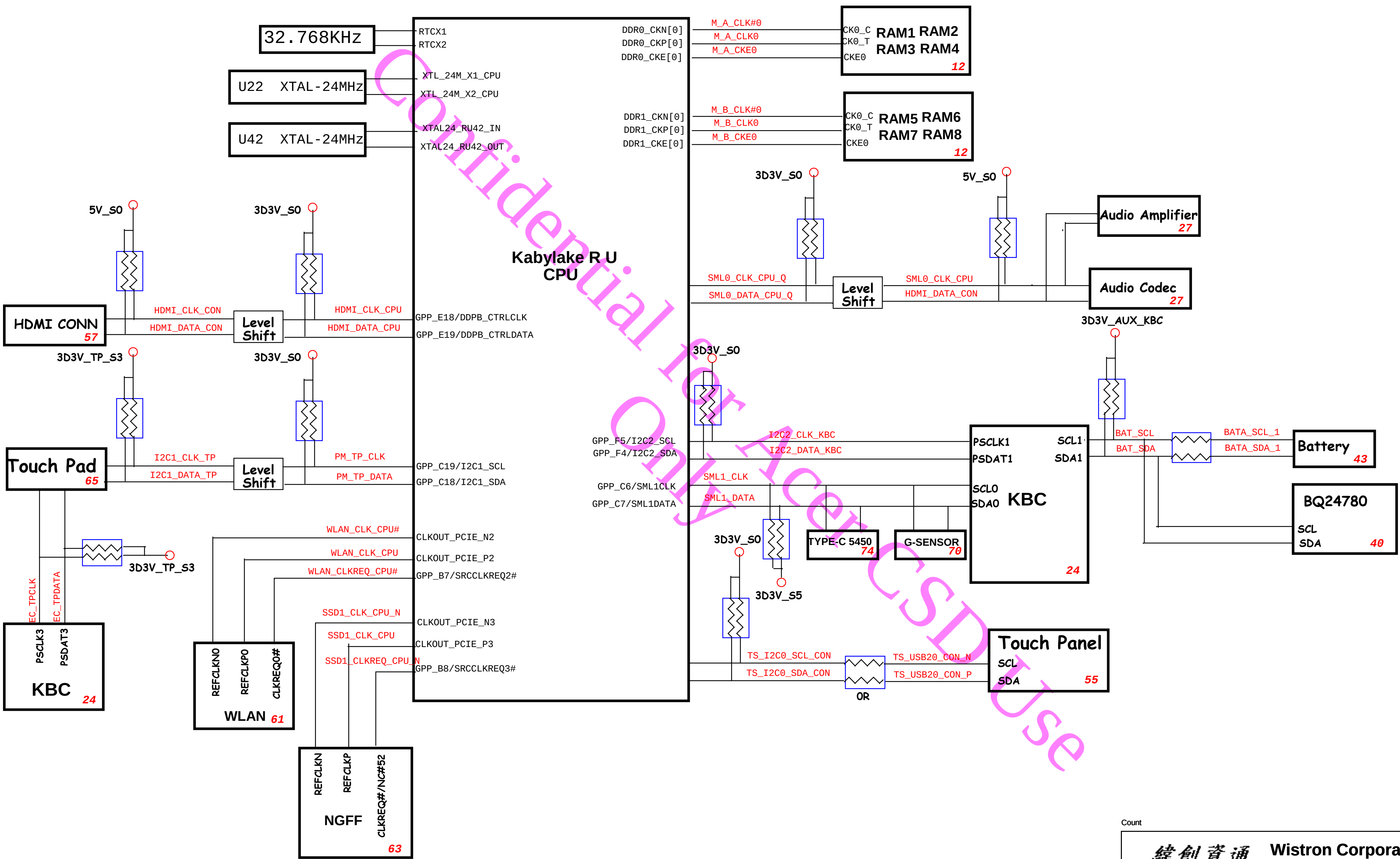
CLOCK BLOCK DIAGRAM



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Title	CLK Block	
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