16924 Woody/Buzz_UMA KBL

Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

Count

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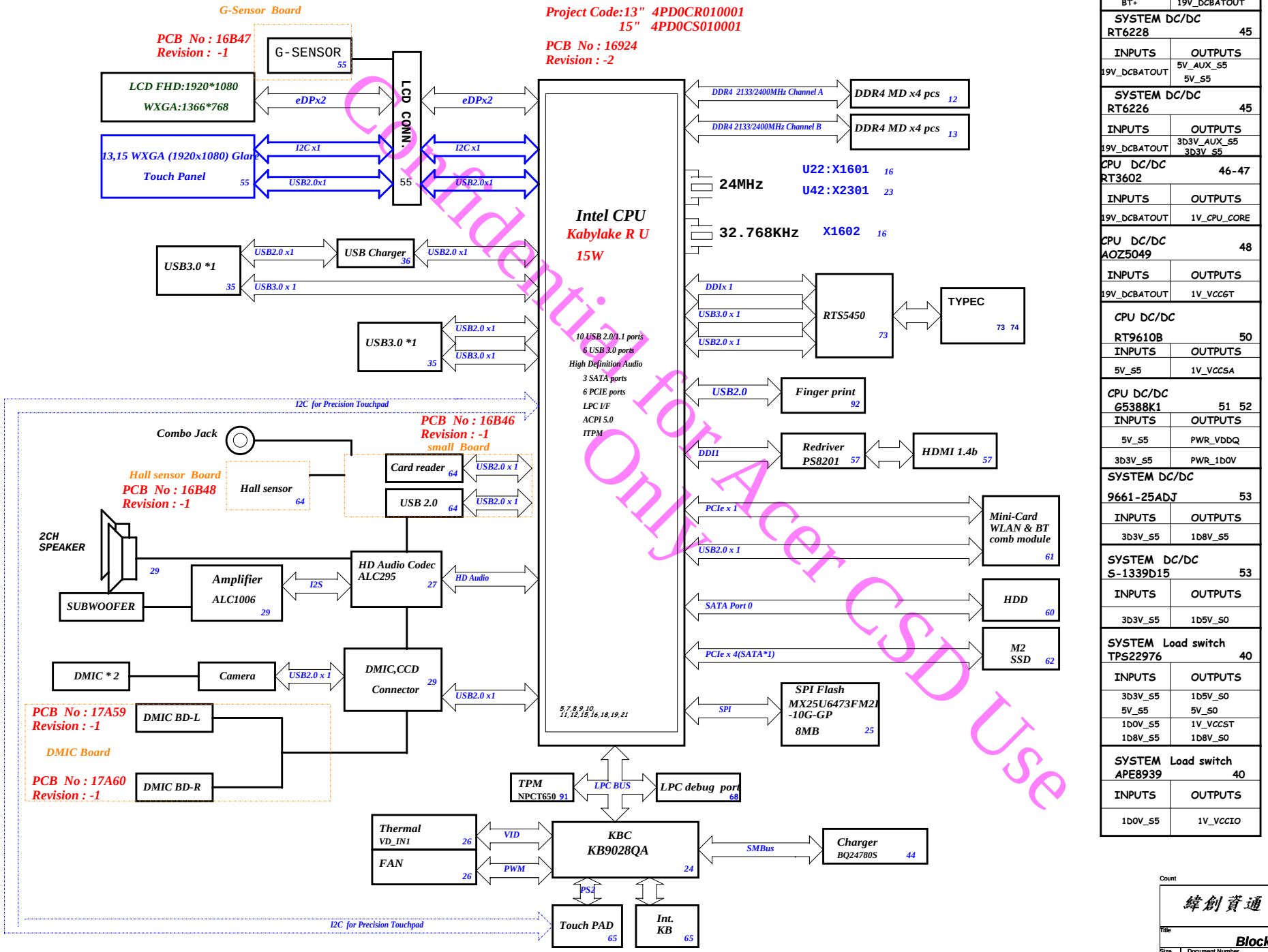
Title: Cover Page		
Size: A3	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 1 of 106	



CHARGER BQ24780S	44
INPUTS	OUTPUTS
AD+ BT+	19V_DCBATOUT

SYSTEM DC/DC RT6228	45
INPUTS	OUTPUTS
19V_DCBATOUT	5V_AUX_S5 5V_S5

SYSTEM DC/DC RT6226	45
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 3D3V_S5

CPU DC/DC RT3602	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC AOZ5049	48
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VCCGT

CPU DC/DC RT9610B	50
INPUTS	OUTPUTS
5V_S5	1V_VCCSA

CPU DC/DC G5388K1	51 52
INPUTS	OUTPUTS
5V_S5	PWR_VDDQ
3D3V_S5	PWR_1D0V

SYSTEM DC/DC 9661-25ADJ	53
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM DC/DC S-1339D15	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

SYSTEM Load switch TPS22976	40
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
5V_S5	5V_S0
1D0V_S5	1V_VCCST
1D8V_S5	1D8V_S0

SYSTEM Load switch APE8939	40
INPUTS	OUTPUTS
1D0V_S5	1V_VCCIO

Count

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Title: Block Diagram

Size	Document Number	Rev
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Main Func = CPU

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU
24 eDP_BLEN_CPU
55 eDP_BLCTRL_CPU
55 eDP_VDDEN_CPU

HDMI

57 HDMI_DATA_CPU_N2
57 HDMI_DATA_CPU_P2
57 HDMI_DATA_CPU_N1
57 HDMI_DATA_CPU_P1
57 HDMI_DATA_CPU_N0
57 HDMI_DATA_CPU_P0
57 HDMI_DATA_CPU_N3
57 HDMI_DATA_CPU_P3

14,57 HDMI_CLK_CPU
14,57 HDMI_DATA_CPU

57 HDMI_DET_CPU

TYPEC

73 DP_DDI_TX_N0
73 DP_DDI_TX_P0
73 DP_DDI_TX_N1
73 DP_DDI_TX_P1
73 DP_DDI_TX_N2
73 DP_DDI_TX_P2
73 DP_DDI_TX_N3
73 DP_DDI_TX_P3

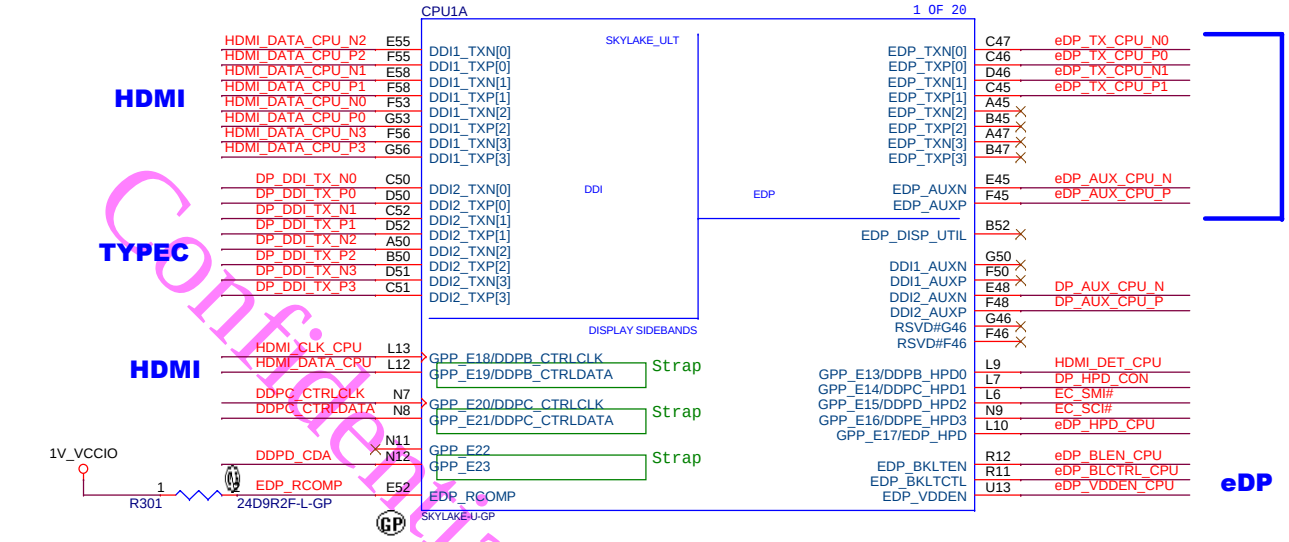
73 DP_AUX_CPU_N
73 DP_AUX_CPU_P

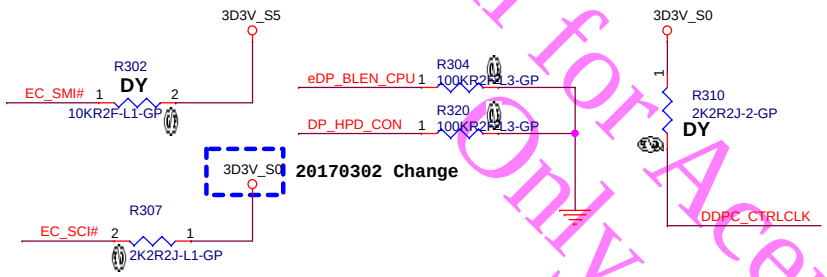
14 DDPC_CTRLDATA
73 DP_HPD_CON

OTHER

14 DDPD_CDA

24 EC_SMI#
24 EC_SCI#





(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

Count

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Title: CPU_(DISPLAY)

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Date: Tuesday, July 25, 2017 | Sheet 3 of 106

Main Func = CPU

DDR4 ball type:NON Interleaved Type

CPU 071.SKYLA.000U

Count

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Title: CPU_(DDR)

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Date: Tuesday, July 25, 2017 | Sheet 4 of 106

Main Func = CPU

DDR4 ball type:NON Interleaved Type

CPU1C — 3 OF 20 — SKYLAKE_ULT — SKYLAKE-U-GP

M_B_DQ[0:7]
M_B_DQ[8:15]
M_B_DQ[16:23]
M_B_DQ[24:31]
M_B_DQ[32:39]
M_B_DQ[40:47]
M_B_DQ[48:55]
M_B_DQ[56:63]

B-CLK
B-CTRL-CKE
B-CTRL-CS
B-CTRL-ODT
B-CMD-MA
B-CMD-MA
B-CMD-MA
B-CMD-MA

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

close CPU

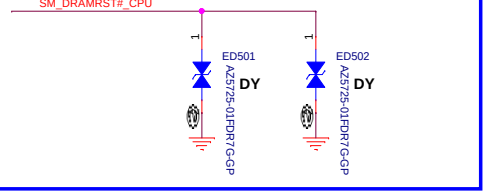
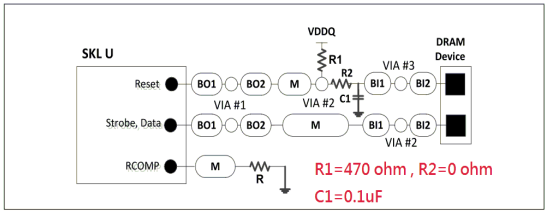


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down Strobe/Data/Reset/RCOMP Signal Topologies



1D2V_S3
R506 470R2F-GP
SM_DRAMRST# 12,13
R501 SDP 200R2F-L-GP
R510 DDP 121R2F-GP
R504 0R0402-PAD
R502 80D6R2F-L-GP
R503 100R2F-L3-GP
C501 SC100P50V2JN-L-GP
Sensitive trace cap

Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

	R501
DDP	121ohm(64.12105.6DL)
SDP	200ohm(64.20005.6DL)

071.SKYLA.000U

#543016

CPU

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Main Func = PCH

DETECT&RESET

55 TOUCH_DET#
25 RTC_DET#
55 TOUCH_S_RST#

DEBUG PORT

68 LPSS_UART1_RXD
68 LPSS_UART1_TXD
68 LPSS_UART1_RTS#
68 LPSS_UART1_CTS#
68 LPSS_UART2_RXD
68 LPSS_UART2_TXD
68 LPSS_UART2_RTS#
68 LPSS_UART2_CTS#

I2C

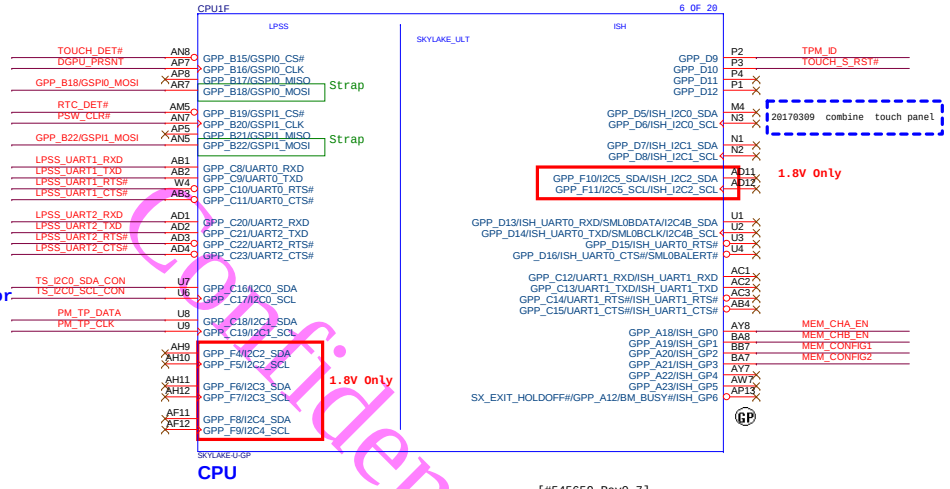
24,55 TS_I2C0_SDA_CON
24,55 TS_I2C0_SCL_CON
65 PM_TP_DATA
65 PM_TP_CLK

OTHER

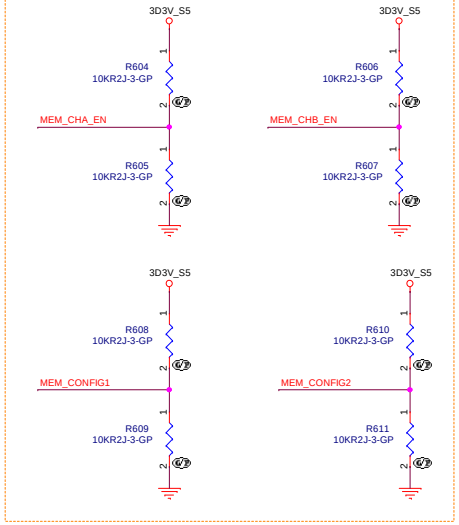
14 GPP_B18/GSPI0_MOSI
14 GPP_B22/GSPI1_MOSI

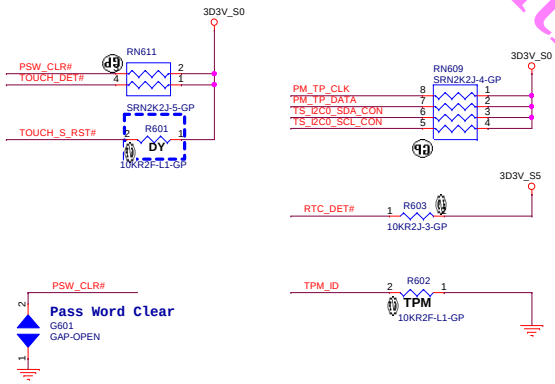
Touch Panel/G-Sensor

Touch Pad



[#545659 Rev0.7]





GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

Vendor	GONFIG4 (GPP_A19)	CONFIG3 (GPP_A18)	CONFIG2 (GPP_A21)	CONFIG1 (GPP_A20)	Mfr.PN	Wistron PN	Capacity	DDP/SDP
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	KN.8GB0G.049	8Gb	SDP
MICRON	0	0	0	1	MT40A512M16JY-083E:B	KN.8GB04.013	8Gb	SDP
SAMSUNG	0	0	1	0	K4A8G165WB-BCRC	KN.8GB0B.048	8Gb	SDP
HYNIX	0	0	1	1	H5AN4G6NAFR-TF	KN.0040G.015	4Gb	SDP
HYNIX	0	1	0	0	H5AN4G6NAFR-UHC	KN.0040G.016	4Gb	SDP
MICRON	0	1	0	1	MT40A256M16GE-083E:B	KN.00404.010	4Gb	SDP
SAMSUNG	0	1	1	0	K4A4G165WE-BCRC	KN.0040B.014	4Gb	SDP
HYNIX	0	1	1	1	H5ANAG6NAMR-UHC	KN.0160G.010	16Gb	DDP
MICRON	1	0	0	0	MT40A1G16WBU-083E:B	KN.01604.001	16Gb	DDP

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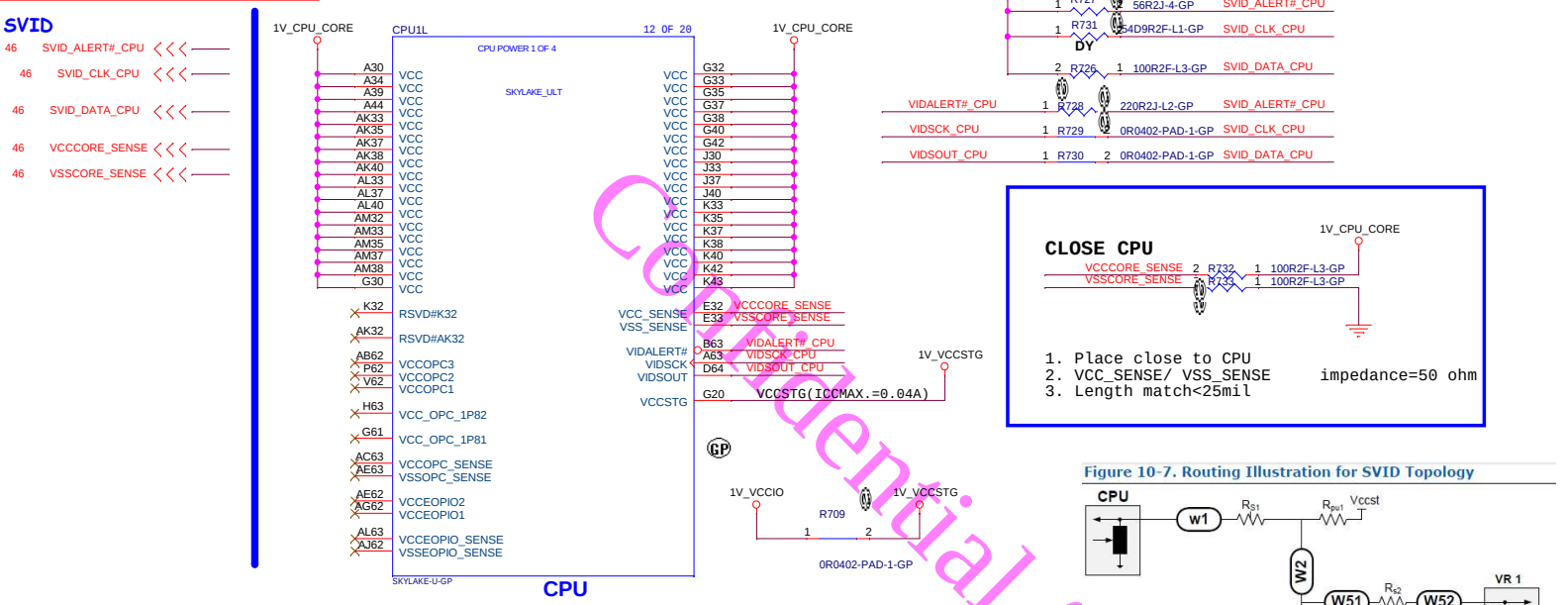
Main Func = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology

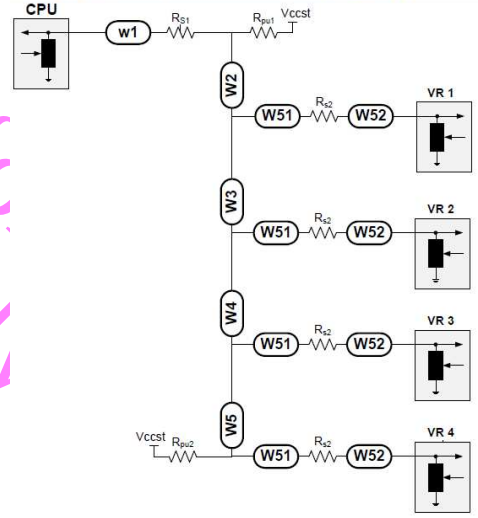


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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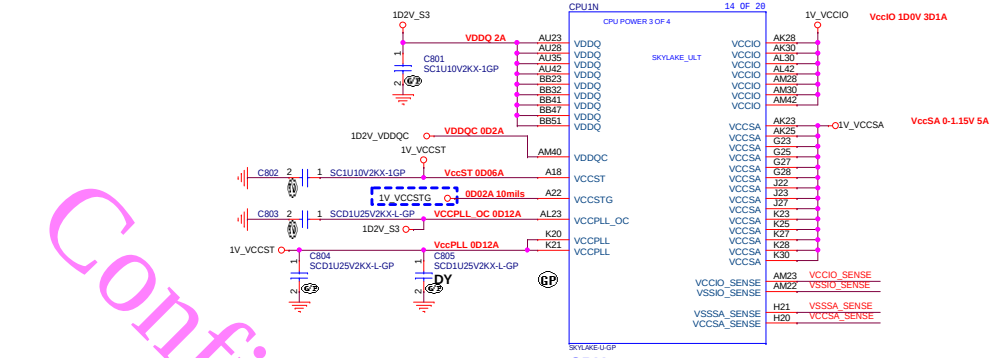
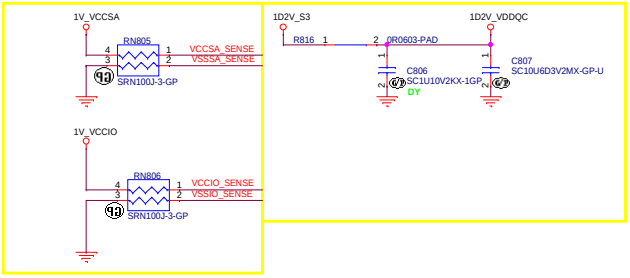
Main Func = CPU

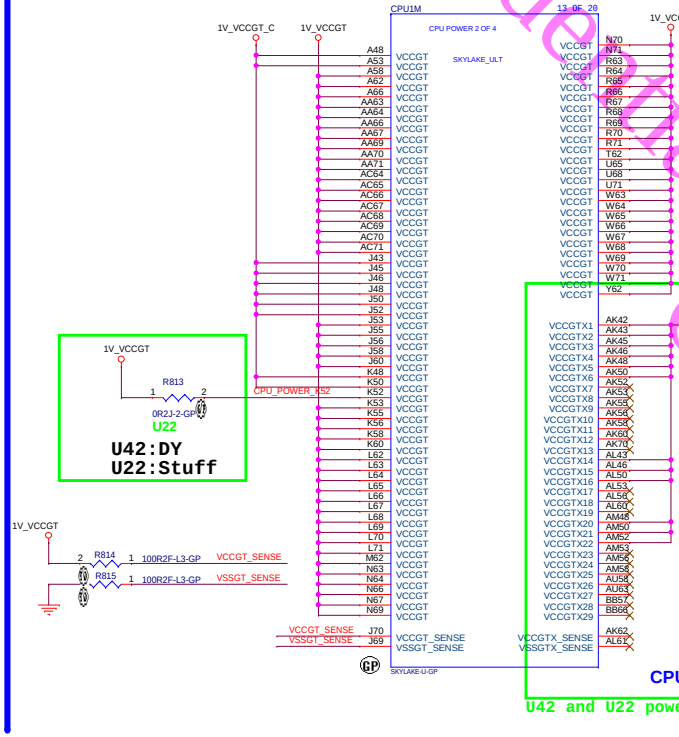
46 VSSSA_SENSE
46 VCCSA_SENSE
46 VCCGT_SENSE
46 VSSGT_SENSE



CPU



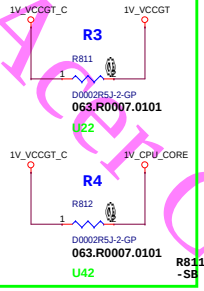
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 44, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.



CPU

If no plan to use U 2+3e in the same platform. These balls can be connected to VccCore. No shunting resistor needed.

20170208 ENG R811 Change to 063.R0007.0161



R811,R812 change PN -SB 20170324

KBL U42 Board Compatibility with KBL U22/23e

- 4 Rshunts Required
  - R1 – between VCCGTU VR and VCCGTU
  - R2 – between VCCGTU and VCCCORE
  - R3 – between VCCGT and VCCGT VR
  - R4 – between VCCGT and VCCCORE
- Stuff R1 and R3 when U22 or U23e mount on board
- Stuff R2 and R4 and de-pop R1 and R3 when U42 mount on board

U22	R1	X	R3	X
U42	X	R2	X	R4

Count

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Blanking

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Title

Reserved

Size	Document Number	Rev
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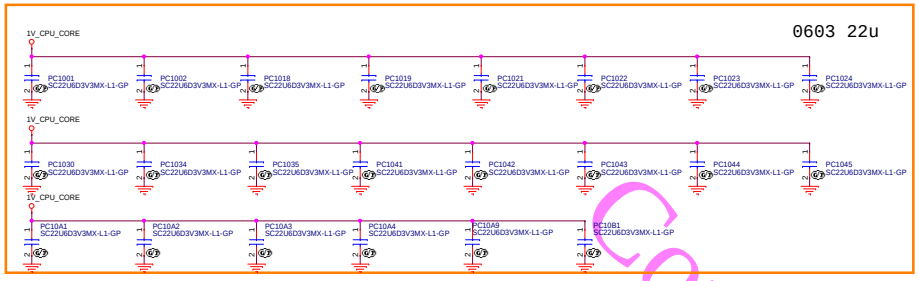
Date: Tuesday, July 25, 2017 Sheet 9 of 106

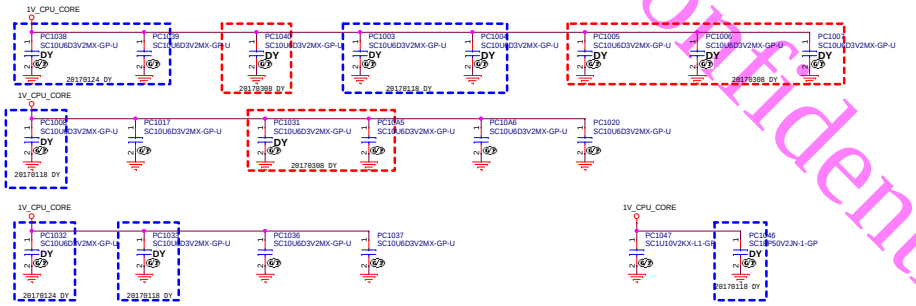
Main Func = CPU

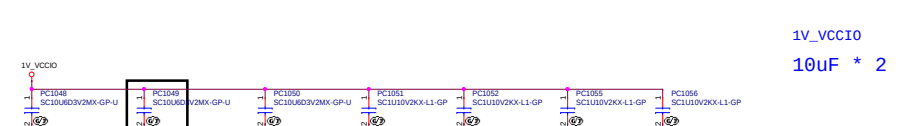


1V_CPU_CORE

U22 0603 22uF *22 , 0402 10uF*11 , 1uF*1

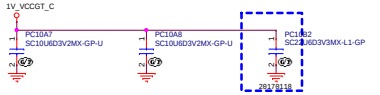
U42 0603 22uF *4 , 0402 10uF*15





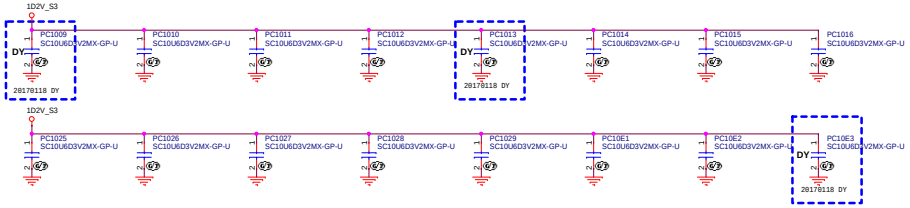
1V_VCCIO

10uF * 2 1uF *4

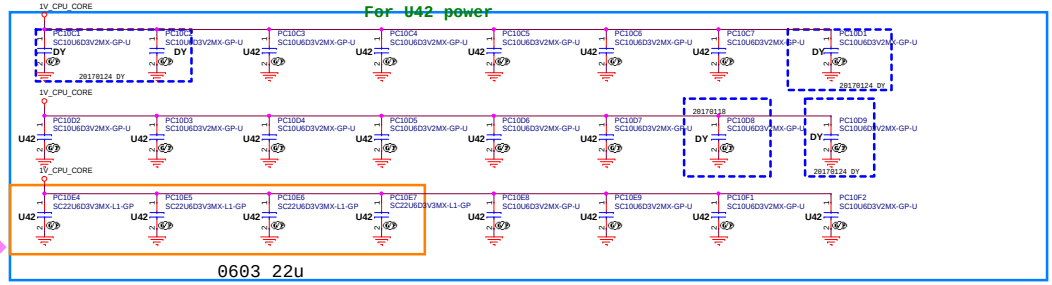


1D2V_S3

0402 10uF*13



For U42 power



Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)		Placed at backside side near to VR output
V_{CCGT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V_{CCIO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V_{CCSA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V_{CCPLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

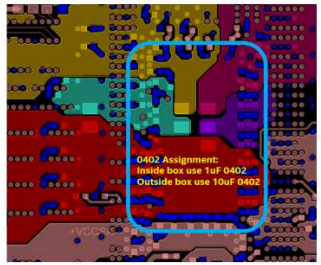
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/V_{CCGT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
V_{CCGT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
V_{CCSA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
V_{CCIO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
V_{CCPLL}		1x 1 uF 0402	Place as close to the package as possible.
V_{CCPLL_OC}		1x 1 uF 0201	Do not route V_{CCPLL}, V_{CCPLL_OC}, V_{CCST} closest adjacent layer over any power net other than ground.
V_{CCST}		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.



Count

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Title: CPU_(Power CAP1)

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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Main Func = CPU

SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

0603 22u

1V_VCCGT
PC1101 SC22U6D3V3MX-L1-GP
PC1102 SC22U6D3V3MX-L1-GP
PC1112 SC22U6D3V3MX-L1-GP
PC1116 SC22U6D3V3MX-L1-GP
PC1134 SC22U6D3V3MX-L1-GP
PC1135 SC22U6D3V3MX-L1-GP
PC1137 SC22U6D3V3MX-L1-GP
PC1138 SC22U6D3V3MX-L1-GP

1V_VCCGT
PC1167 SC22U6D3V3MX-L1-GP
PC10B3 SC22U6D3V3MX-L1-GP
PC10B4 SC22U6D3V3MX-L1-GP
PC10B5 SC22U6D3V3MX-L1-GP
PC10B6 SC22U6D3V3MX-L1-GP
PC10B7 SC22U6D3V3MX-L1-GP

1V_VCCGT
PC1121 SC10U6D3V2MX-GP-U
PC1122 SC10U6D3V2MX-GP-U
PC1123 SC10U6D3V2MX-GP-U
PC1124 SC10U6D3V2MX-GP-U
PC1125 SC10U6D3V2MX-GP-U
PC1126 SC10U6D3V2MX-GP-U
PC1127 SC10U6D3V2MX-GP-U
PC1128 SC10U6D3V2MX-GP-U

1V_VCCGT
PC1133 SC10U6D3V2MX-GP-U DY
PC1107 SC10U6D3V2MX-GP-U
PC1108 SC10U6D3V2MX-GP-U
PC1136 SC10U6D3V2MX-GP-U
PC1103 SC10U6D3V2MX-GP-U
PC1104 SC10U6D3V2MX-GP-U
PC1105 SC10U6D3V2MX-GP-U
PC1168 SC10U6D3V2MX-GP-U DY

1V_VCCGT
PC1109 SC10U6D3V2MX-GP-U
PC1110 SC10U6D3V2MX-GP-U
PC1111 SC10U6D3V2MX-GP-U DY
PC1141 SC10U6D3V2MX-GP-U
PC1113 SC10U6D3V2MX-GP-U
PC1114 SC10U6D3V2MX-GP-U
PC1115 SC10U6D3V2MX-GP-U
PC1171 SC10U6D3V2MX-GP-U

1V_VCCGT
PC1165 SC10U6D3V2MX-GP-U
PC1166 SC10U6D3V2MX-GP-U

1V_VCCGT
0603 22uF *14 , 0402 10uF*26

1V_VCCSA
0402 10uF*12

1V_VCCSA
-1 20170505
PC1117 SC22U6D3V3MX-L1-GP
PC1119 SC22U6D3V3MX-L1-GP
PC1120 SC10U6D3V2MX-GP-U

1V_VCCSA
-1 20170505
PC1129 SC22U6D3V3MX-L1-GP
PC1130 SC22U6D3V3MX-L1-GP
PC1132 SC22U6D3V3MX-L1-GP

1V_VCCSA
20170118
PC1139 SC10U6D3V2MX-GP-U
PC1170 SC10U6D3V2MX-GP-U
PC1152 SC10U6D3V2MX-GP-U
PC1140 SC10U6D3V2MX-GP-U

U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								0r	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								0r	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

1D0V_S5
PC1142 DY
CLOSE CPU AB19

1D0V_S5
PC1143
20170708
CLOSE CPU AF18

1D0V_S5
PC1144
CLOSE CPU K17

1D0V_S5
PC1145
PC1146
20170706
CLOSE CPU N15

1D0V_S5
PC1147
20170706
CLOSE CPU K15

1D0V_S5
PC1148
20170706
CLOSE CPU AF20

1D0V_S5
PC1149
CLOSE CPU N18

1D0V_S5
PC1150
20170708
CLOSE CPU A10

1D0V_VCCDSW
PC1163
CLOSE CPU AL1

VCCRTCEXT
PC1164
CLOSE CPU BB10

3D3V_S5
PC1153
CLOSE CPU AJ19

3D3V_S5
PC1154 DY
CLOSE CPU V19

3D3V_S5
PC1155 DY
CLOSE CPU AG15

3D3V_S5
PC1156 DY
CLOSE CPU Y16

3D3V_S5
PC1157 DY
CLOSE CPU T16

3D3V_S5
PC1158
PC1159
CLOSE CPU AK17

3D3V_RTC_AUX
PC1160
PC1161
CLOSE CPU AK19

1D8V_S5
PC1162
CLOSE CPU AA1

Count

緯創資通 Wistron Corporation
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Title: CPU_(Power CAP2)

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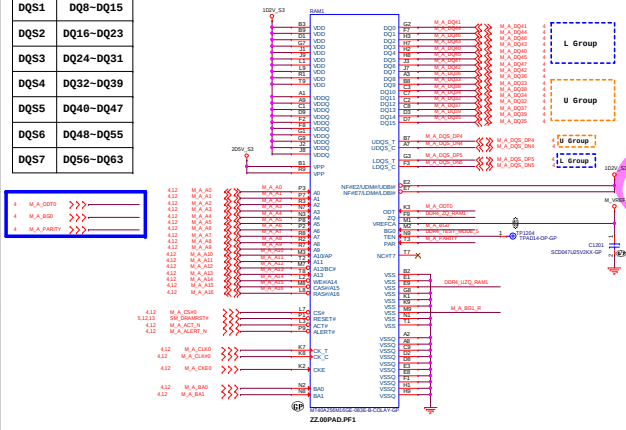
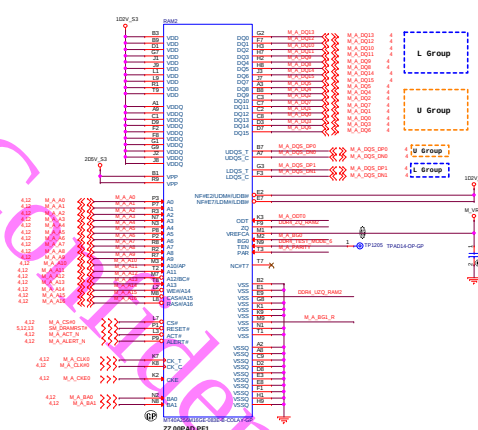
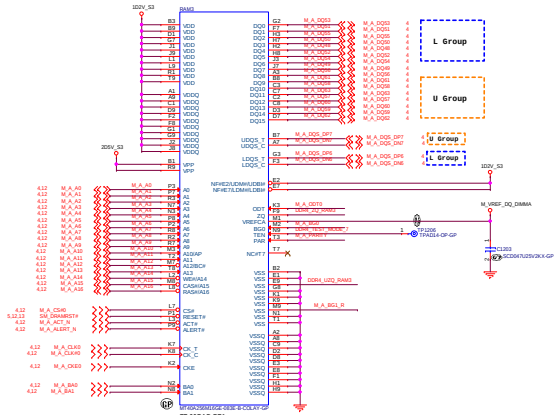
SSID = LPDDR3 CHA

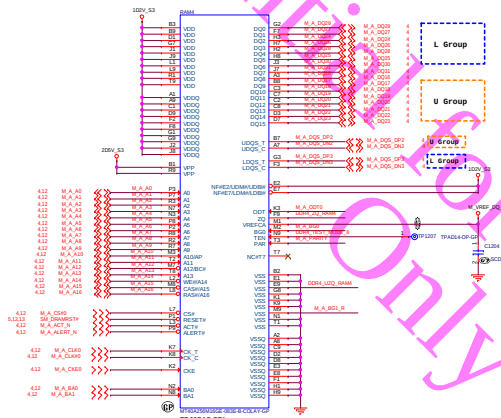
DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required









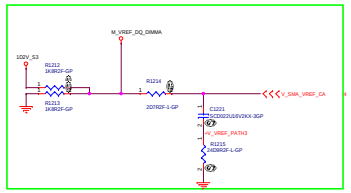
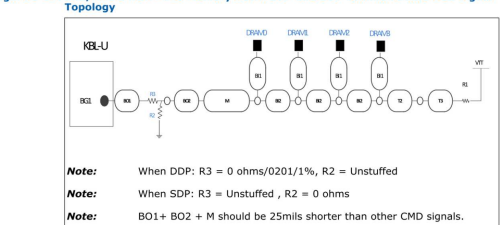


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology

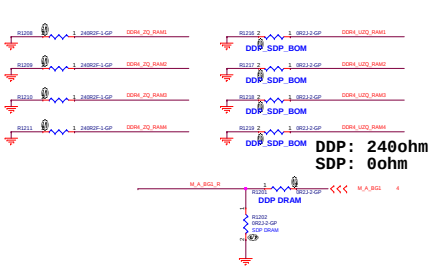


Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed

Note: When SDP: R3 = Unstuffed , R2 = 0 ohms

Note: BO1+ BO2 + M should be 25mils shorter than other CMD signals.

SDP & DDP SETTING



DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

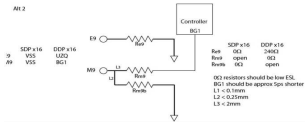
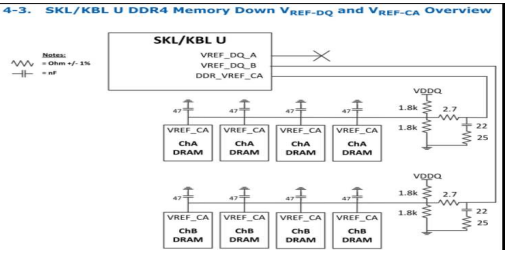
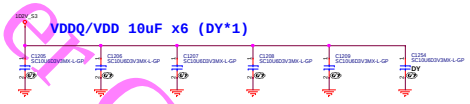


Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF-DQ} and V_{REF-CA} Overview

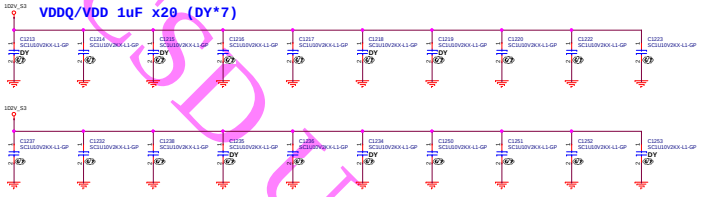


DDR4 On Board RAM Power Decouple Cap

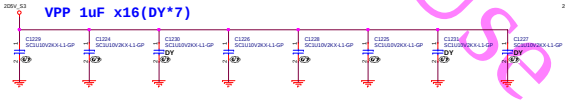
VDDQ/VDD 10uF x6 (DY*1)



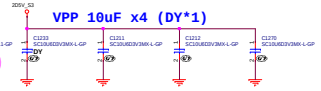
VDDQ/VDD 1uF x20 (DY*7)



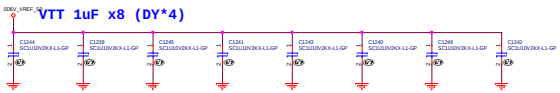
VPP 1uF x16(DY*7)



VPP 10uF x4 (DY*1)

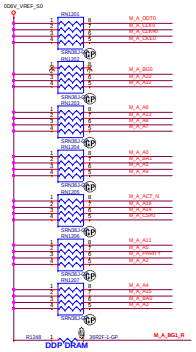


VTT 1uF x8 (DY*4)



VTT 10uF x2 (DY*1)

For RAM1,RAM2,RAM3,RAM4



Wistron Corporation	Size	Document Number	Rev
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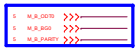
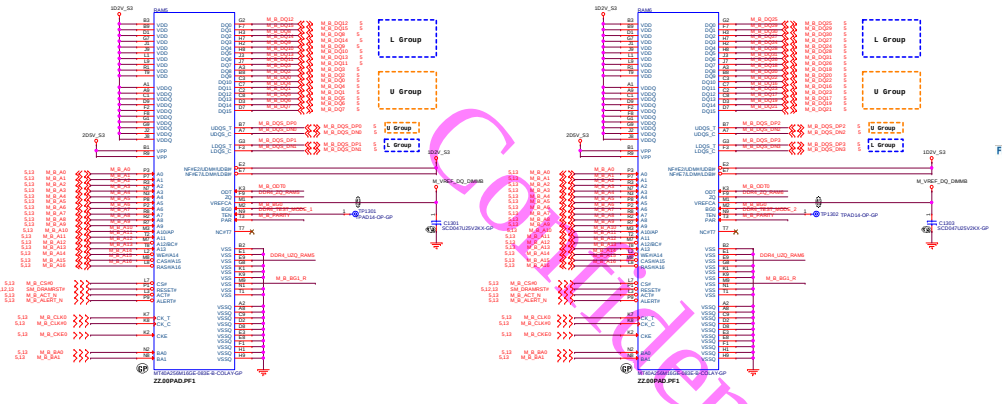
DDR4 MD_CHA	Date: Monday, July 23, 2018	Sheet 12 of 108	

SSID = LPDDR3 CHB

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63



please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required



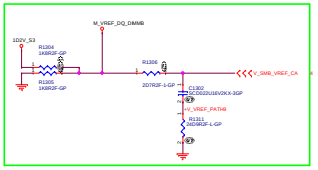
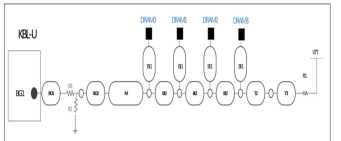


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology

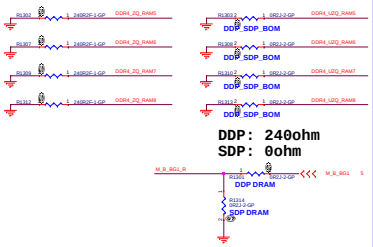


Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed

Note: When SDP: R3 = Unstuffed , R2 = 0 ohms

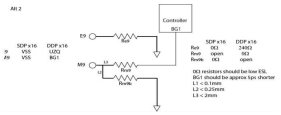
Note: BO1+ BO2 + M should be 25mils shorter than other CMD signals.

SDP & DDP SETTING



DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little



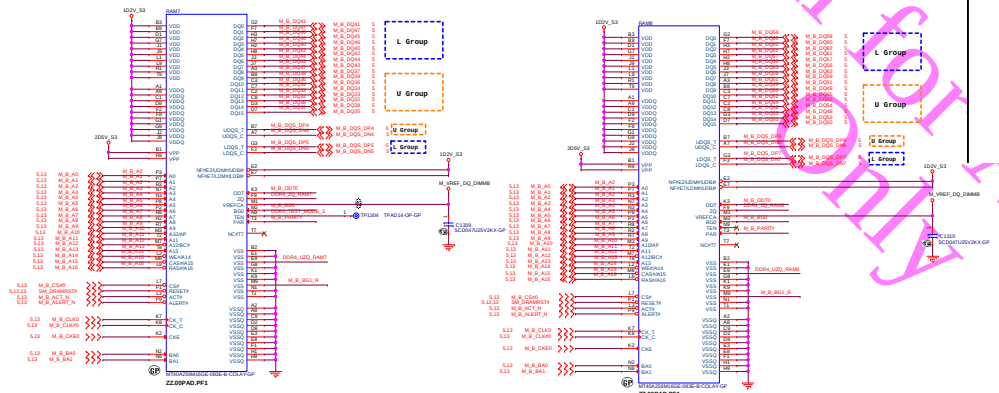
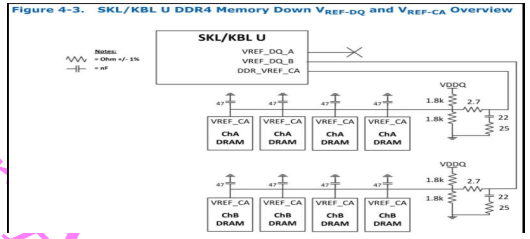
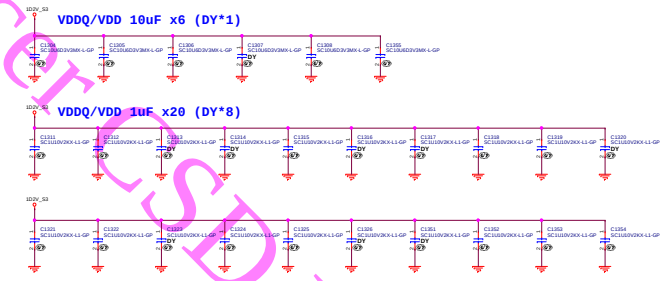
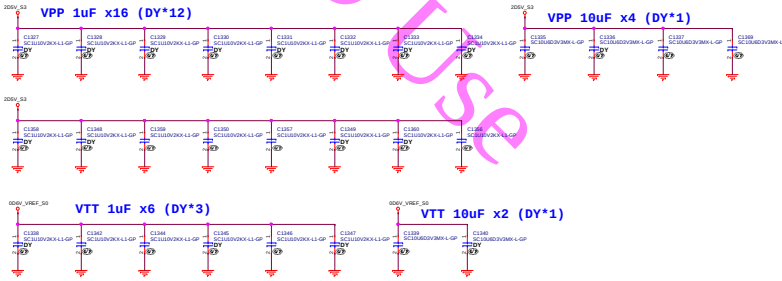


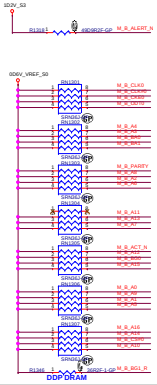
Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



DDR4 On Board RAM Power Decouple Cap







4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

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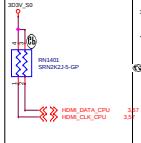
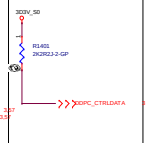
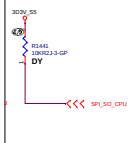
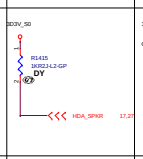
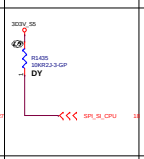
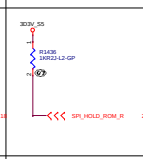
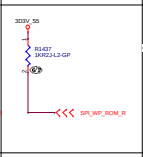
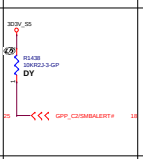
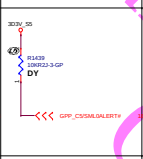
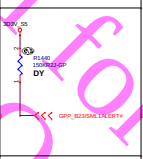
Date: Tuesday, July 21, 2015 Sheet 14 of 60
Woody/Buzz_KBL

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit 10 — Boot BIOS Destination 0 — SPI 1 — LPC *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. 1 = **eSPI** Is selected for EC. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2) Input	De-Glitch (Note 2) Output	Multiplexed With	Default	NMI or SMI Capable	Note
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts
GPP_B23	20K PD (see note)	Yes	No	SML1ALERT#/ PCHHOT#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio Interface					
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLK	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Driven Low		OFF
HDA_SDI[1:0]	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	Off
SPI0_MOSI	Primary	Internal Pull up/ Pull-down (See Note 1 &2)	Driven Low	Driven Low	Off
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	Off
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	Off
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	Off
SPI1_CLK	Primary	Undriven	Undriven	Undriven	Off
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	Off
SPI1_MISO	Primary	Undriven	Undriven	Undriven	Off
SPI1_CS#	Primary	Undriven	Undriven	Undriven	Off
SPI_IO[2:3]	Primary	Undriven	Undriven	Undriven	Off

Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

Count

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Title: (Reserved)_SODIMM_SODIMM4

Size: A1 | Document Number: Woody/Buzz_KBL | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 14 of 105

Main Func = PCH

USB3 port1

35 USB1_USB30_RX_N
35 USB1_USB30_RX_P
35 USB1_USB30_TX_N
35 USB1_USB30_TX_P
35 USB1_USB20_N
35 USB1_USB20_P

USB3 port2

35 USB2_USB30_RX_N
35 USB2_USB30_RX_P
35 USB2_USB30_TX_N
35 USB2_USB30_TX_P
36 USB2_USB20_N
36 USB2_USB20_P

USB Type-C

73 USB30_RX_CPU_N3
73 USB30_RX_CPU_P3
73 USB30_TX_CPU_N3
73 USB30_TX_CPU_P3
73 TYPEC_USB20_N
73 TYPEC_USB20_P

USB2.0

64,89 USB3_USB20_N
64,89 USB3_USB20_P
61,89 BT_USB20_N
61,89 BT_USB20_P
55 TS_USB20_N
55 TS_USB20_P
29 CCD_USB20_N
29 CCD_USB20_P
64,89 CR_USB20_N
64,89 CR_USB20_P
92 FP_USB20_N
92 FP_USB20_P

M.2

62 PCIE_RX_CPU_N11
62 PCIE_RX_CPU_P11
62 PCIE_TX_CON_N11
62 PCIE_TX_CON_P11
62 PCIE_RX_CPU_N12
62 PCIE_RX_CPU_P12
62 PCIE_TX_CON_N12
62 PCIE_TX_CON_P12
62 DEVSLP1

HDD

60 HDD_SATA_TX_P
60 HDD_SATA_TX_N
60 HDD_SATA_RX_P
60 HDD_SATA_RX_N

WLAN

61,89 WLAN_PCIE_RX_N
61,89 WLAN_PCIE_RX_P
61,89 WLAN_PCIE_TX_N
61,89 WLAN_PCIE_TX_P

WLAN

HDD/SATA

M.2 SSD1

Layout Note:
1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

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USB1(USB 3.0)
USB2(USB 3.0)
USB3(Type-C)
USB1(USB 2.0)
USB2(USB 2.0)
TYPEC
SMALL BOARD(USB2.0)
BT
Touch Panel
CCD
Card Read
FP

071.SKYLA.000U

CPU

M.2 auto detection

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

	KBL PremiumU		Acer 2015		2017R15(Premium)		2017R15(base)
Lane1	USB3 Port1		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane2	USB3 Port2		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane3	USB3 Port3		USB 3 (I/O)		USB 3 Type-C (I/O)		USB 3 Type-C (I/O)
Lane4	USB3 Port4						
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU		dGPU		dGPU
Lane6	USB3 Port6 (Premium)	PCIe Port2					
Lane7		PCIe Port3					
Lane8		PCIe Port4					
Lane9		PCIe Port5	LAN				
Lane10		PCIe Port6	WIFI		WIFI		WIFI
Lane11	SATA0 (Base/Premium)	PCIe Port7 (Premium)	HDD		HDD		HDD
Lane12	SATA1 (Base/Premium)	PCIe Port8 (Premium)	ODD				
Lane13		PCIe Port9	NA	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal		M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal
Lane14		PCIe Port10					
Lane15	SATA1 (Premium)	PCIe Port11					
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x1)		M.2 SSD SATA		
	USB2 Port1		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port2		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port3		USB 3 (I/O)		USB 2 Type-C (I/O)		USB 2 Type-C (I/O)
	USB2 Port4		USB 2 (I/O) / SensorHub		USB 2 (I/O)		USB 2 (I/O)
	USB2 Port5		BT		BT		BT
	USB2 Port6		TS		TS		TS
	USB2 Port7		CCD		CCD		CCD
	USB2 Port8		CR (USB) / FP		CR		CR
	USB2 Port9		3G		FP		FP
	USB2 Port10						

CPU1I — SKYLAKE_ULT — 9 OF 28

GPP_F: VCCPGPPF = 1.8V Only

CPU

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(PCIE/SATA/USB)
Size: Custom
Document Number: Woody/Buzz_KBL
Rev: -2
Date: Tuesday, July 25, 2017
Sheet 15 of 106

Main Func = PCH

WLAN
61,89 WLAN_CLK_CPU#
61,89 WLAN_CLK_CPU
61,89 WLAN_CLKREQ_CPU#

NGFF1
62 SSD1_CLK_CPU_N
62 SSD1_CLK_CPU
62 SSD1_CLKREQ_CPU_N

KBC
24 RTCRST_ON

WLAN
61 SUS_CLK_CPU

CPU1J
10 OF 20
CLOCK SIGNALS
SKYLAKE_ULT
SKYLAKE-U-GP

WLAN
NGFF1
CPU

PEG_CLKREQ_CPU# D42 C42 AR10 CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
LAN_CLKREQ_CPU# B42 A42 AT7 CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
WLAN_CLK_CPU# D41
WLAN_CLK_CPU C41
WLAN_CLKREQ_CPU# AT8 CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#
SSD1_CLK_CPU_N D40
SSD1_CLK_CPU C40
SSD1_CLKREQ_CPU_N AT10 CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#
SRCCLKREQ4# B40 A40 AU8 CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#
SRCCLKREQ5# E40 E38 AU7 CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17 SUS_CLK_CPU
XTAL24_IN E37 XTL_24M_X1_CPU
XTAL24_OUT E35 XTL_24M_X2_CPU
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 XTL_32K_X1_CPU
RTCX2 AM20 XTL_32K_X2_CPU
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST#

1D0V_S5
R1603 2K7R2F-GP

RTC Reset

For AFR
RTCRST_ON
Q1603 2N7002K-2-GP
RTC_RST#_R
RTC_RST#
R1618 100KR2F-L3-GP
R1621 2K2R2J-L1-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1615 10MR2J-L-GP
20170210 change
X1602 XTAL-32D768KHZ-91-GP
082.30003.0221
2ND = 082.30003.0301
3RD = 082.30003.0191
C1603 SC15P50V2JN-L-GP
C1604 SC15P50V2JN-L-GP
-SB 20170314 VENDOR SUGGEST

3D3V_RTC_AUX
RN1601 SRN20KJ-1-GP
SRTC_RST#
RTC_RST#
C1606 SC1U50V3KX-GP
G1601 GAP-OPEN
C1605 SC1U50V3KX-GP

XTL_24M_X1_CPU
U22 C1601 SC15P50V2JN-L-GP
R1602 1MR2F-L-GP
INPUT/OUTPUT#1
NC#2
INPUT/OUTPUT#3
X1601 XTAL-24MHZ-135-GP
082.30006.0041
2nd = 82.30004.A01
U22
XTL_24M_X2_CPU
U22 C1602 SC15P50V2JN-L-GP

X1601 P/N:082.30006.0041

close to CPU
3D3V_S0
RN1608 SRN10KJ-12-GP
SSD1_CLKREQ_CPU_N
PEG_CLKREQ_CPU#
WLAN_CLKREQ_CPU#
LAN_CLKREQ_CPU#
RN1609 SRN10KJ-L-GP
SRCCLKREQ4#
SRCCLKREQ5#

Count

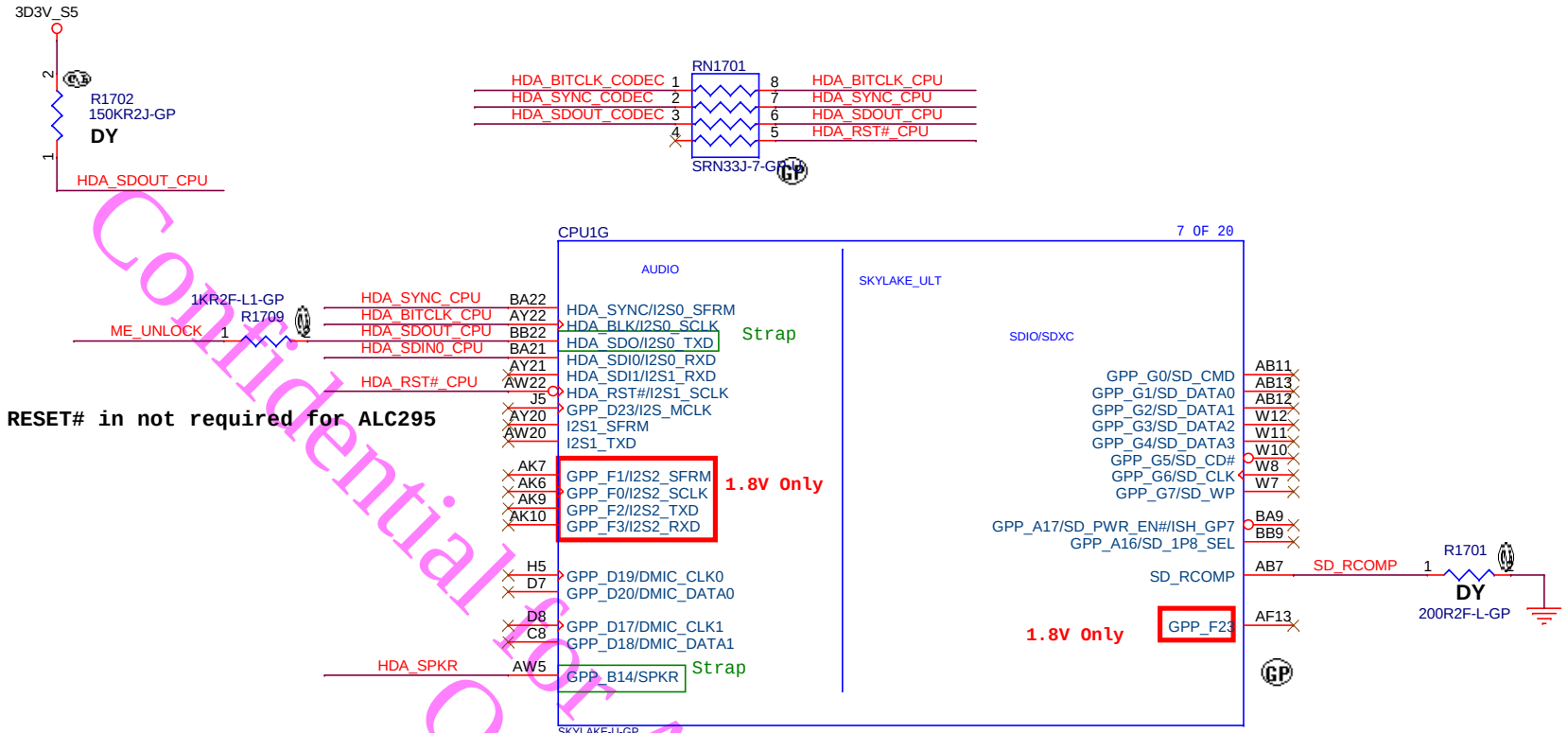
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MCP_CLOCK
Size: Custom	Document Number: Woody/Buzz_KBL
Rev	-2
Date: Tuesday, July 25, 2017	Sheet 16 of 106

Main Func = PCH

Audio Code

27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
27 HDA_SDIN0_CPU
14,27 HDA_SPKR

24 ME_UNLOCK



RESET# in not required for ALC295

CPU

18.3 Terminating Unused SDXC Signals

SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

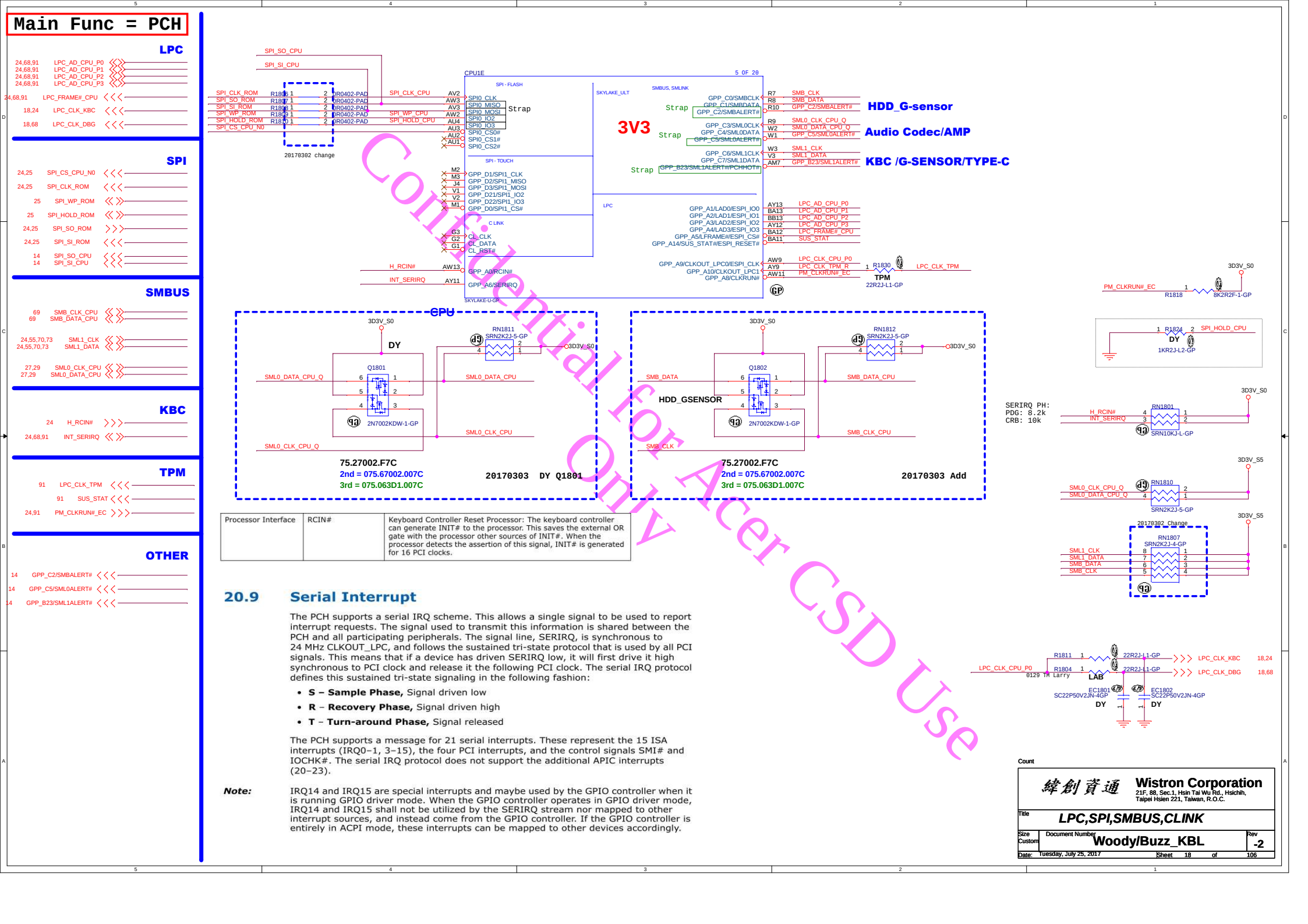
Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 17 of 106



Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

Count

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	LPC,SPI,SMBUS,CLINK	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 18 of 106	

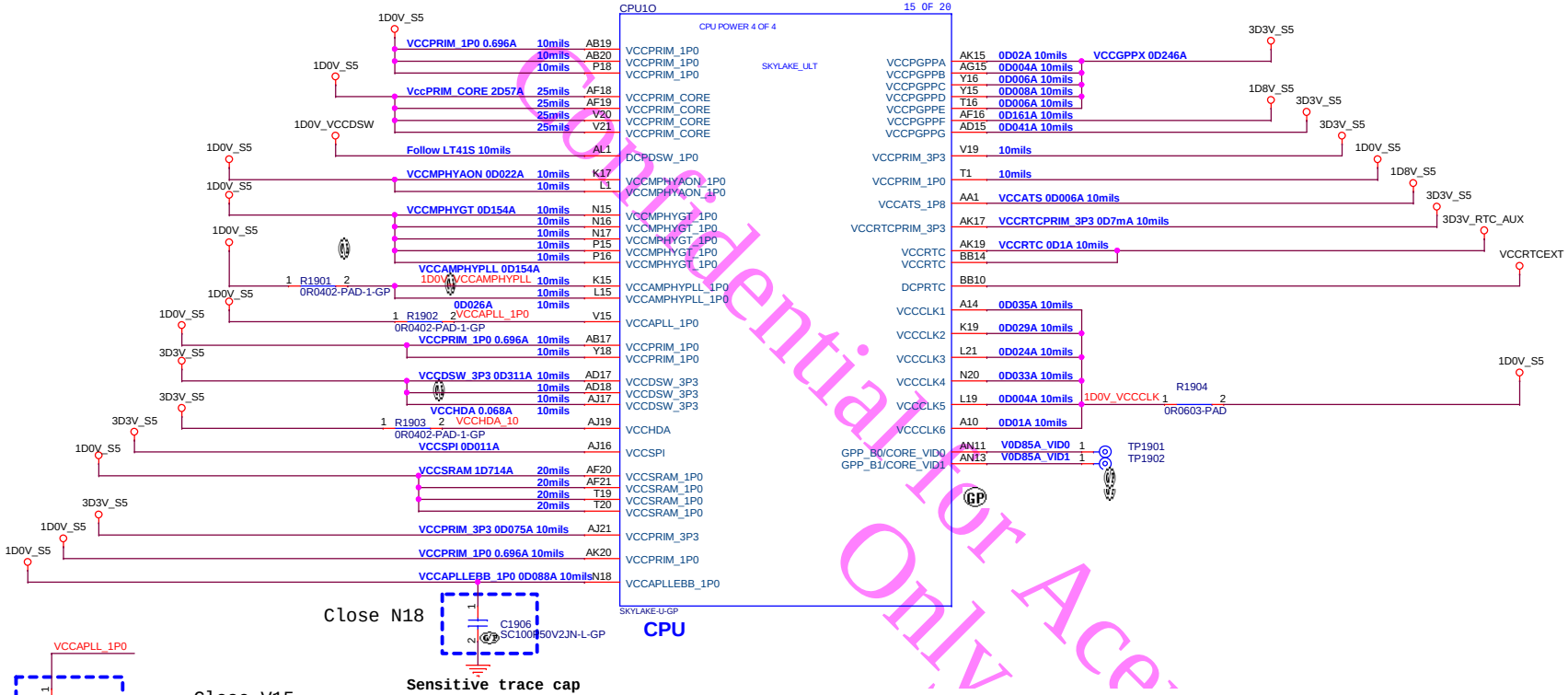


Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SMLOALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

Count

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_(CS-2/EMMC)	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 19 of 106	

Main Func = PCH

24	SYS_PWROK
40	PCH_PWROK
24,61,62	PCIE_WAKE#
24,40	ALL_SYS_PWRGD
24,61,62,68,89,91	PLT_RST#
24	RSMRST#_KBC
45,53,73	3V_5V_POK
24,40,53,60	PM_SLP_S3#
24,40,51	PM_SLP_S4#
24	PM_PWRBTN#
24	AC_PRESENT

CPU1K — SYSTEM POWER MANAGEMENT — SKYLAKE_ULT — SKYLAKE-U-GP — 11 OF 20

GPP_B13/PLTRST# (AN10) ← PLT_RST#
SYS_RESET# (B5) ← XDP_DBRESET#
RSMRST# (AY17) ← PM_RSMRST#
PROCPWRGD (A68) → VCCST_PWRGD
VCCST_PWRGD (B65)
SYS_PWROK (B6) ← SYS_PWROK
PCH_PWROK (BA20) ← PM_PCH_PWROK
DSW_PWROK (BB20) ← PCH_DPWROK
GPP_A13/SUSWARN#/SUSPWRDNACK (AR13) ← PM_SUSWARN#
GPP_A15/SUSACK# (AP11) ← PM_SUSACK#
WAKE# (BB15) ← PCIE_WAKE#
GPD2/LAN_WAKE# (AM15) ← GPD2/LAN_WAKE#
GPD11/LANPHYPC (AW17)
GPD7/RSVD#AT15 (AT15)

GPP_B12/SLP_S0# (AT11) → PM_SLP_S3#
GPD4/SLP_S3# (AP15) → PM_SLP_S4#
GPD5/SLP_S4# (BA16)
GPD10/SLP_S5# (AY16)
SLP_SUS# (AN15)
SLP_LAN# (AW15)
GPD9/SLP_WLAN# (BB17)
GPD6/SLP_A# (AN16)
GPD3/PWRBTN# (BA15) → PM_PWRBTN#
GPD1/ACPRESENT (AY15) → AC_PRESENT
GPD0/BATLOW# (AU13) → BATLOW#
GPP_A11/PME#/INTRUDER# (AU11) → SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# (AM10) → EXT_PWR_GATE#
GPP_B2/VRALERT# (AM11)

PCH_PWROK — R2008 0R0402-PAD-1-GP — PM_PCH_PWROK
PM_RSMRST# — R2006 0R0402-PAD-1-GP — PCH_DPWROK

BATLOW#:
Pull-up required even if not implemented.

3D3V_S5
BATLOW# / GPD2/LAN_WAKE# — RN2005 SRN10KJ-L-GP
PCIE_WAKE# / AC_PRESENT — RN2006 SRN10KJ-L-GP
PM_PWRBTN# — R2009 10KR2F-L1-GP

CPU

PM_SUSACK# — R2017 DY 0R2J-2-GP — PM_SUSWARN#

3D3V_S0 — R2024 1KR2F-L1-GP — 分壓 — ALL_SYS_PWRGD — R2020 10KR2F-L1-GP — VCCST_PWRGD
R2021 4K7R2J-L-GP
C2001 SC100P50V2JN-L-GP
Sensitive trace

-SB 20170316

U2001 U74LVC1G08GW-R-GP-U
RSMRST#_KBC, 3V_5V_POK → PM_RSMRST#
C2002 SCD1U25V2KX-L-GP
73.01G08.EHG
2nd = 73.7SZ08.DAH

3D3V_AUX_S5
R2004 100KR2J-3-GP
R2005 10KR2F-L1-GP
Q2001 2N7002KDW-1-GP
3V_5V_POK_# → 3V_5V_POK_C
R2001 1KR2F-L-GP — PM_RSMRST# → RSMRST#_KBC
R2002 0R0402-PAD-1-GP — 3V_5V_POK_C → 3V_5V_POK
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

3D3V_S5
PM_SUSWARN# — R2030 DY 10KR2F-L1-GP
EXT_PWR_GATE# — R2031 DY 20KR2F-L3-GP
20170217 Change 20k
3D3V_RTC_AUX
SM_INTRUDER# — R2019 1MR2F-L-GP
PM_RSMRST# — R2010 10KR2F-L1-GP
PM_PCH_PWROK — R2011 DY 10KR2J-L-GP

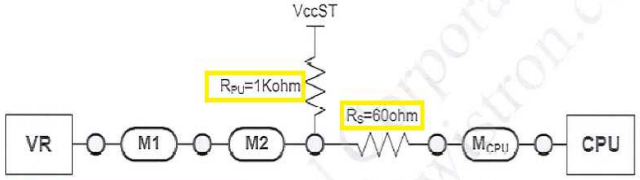
3D3V_S0
R2014 10KR2F-L1-GP — XDP_DBRESET#

PLT_RST# — DY EC2020 SC22P50V2JN-L-GP
PM_PCH_PWROK — DY EC2002 SC10P50V2JN-L-GP

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

VCCST_PWRGD / HWM201:

VCCST_PWRGOOD



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

GPP_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

Count

Wistron Corporation 緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2
Date: Tuesday, July 25, 2017 | Sheet 20 of 106

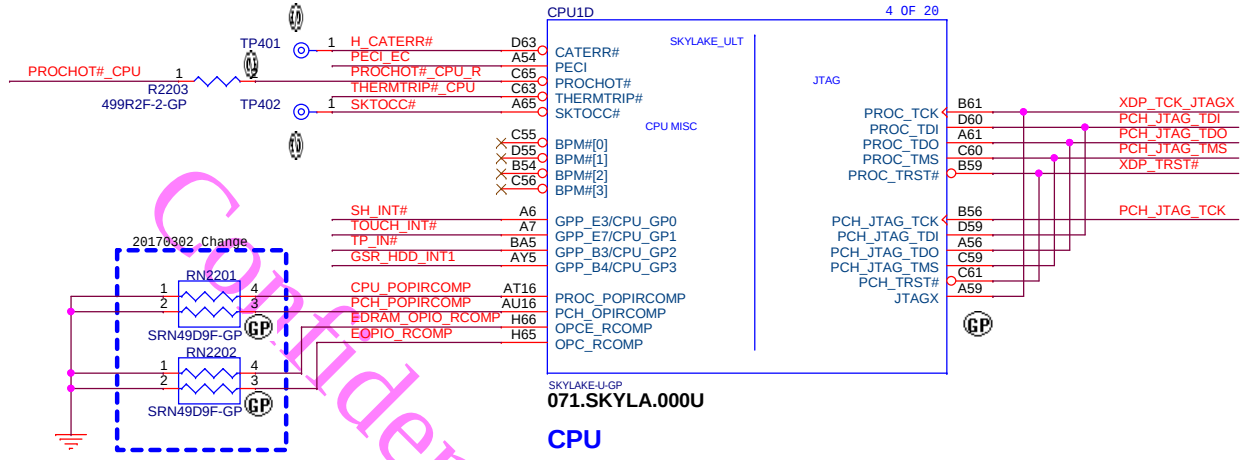
Main Func = PCH

Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CPU_(VSS)*		
Size: Custom	Document Number: **Woody/Buzz_KBL**	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 21 of 106	

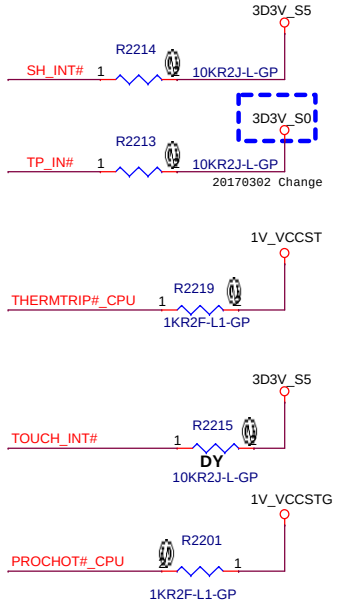
Main Func = CPU

24 PECI_EC
24,44,46 PROCHOT#_CPU
24 SH_INT#
55 TOUCH_INT#
65 TP_IN#
69 GSR_HDD_INT1



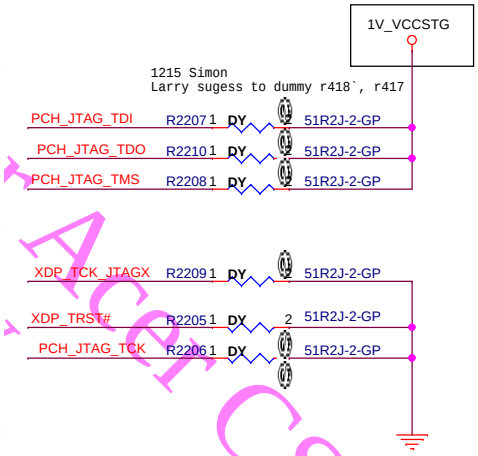
071.SKYLA.000U

CPU



PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

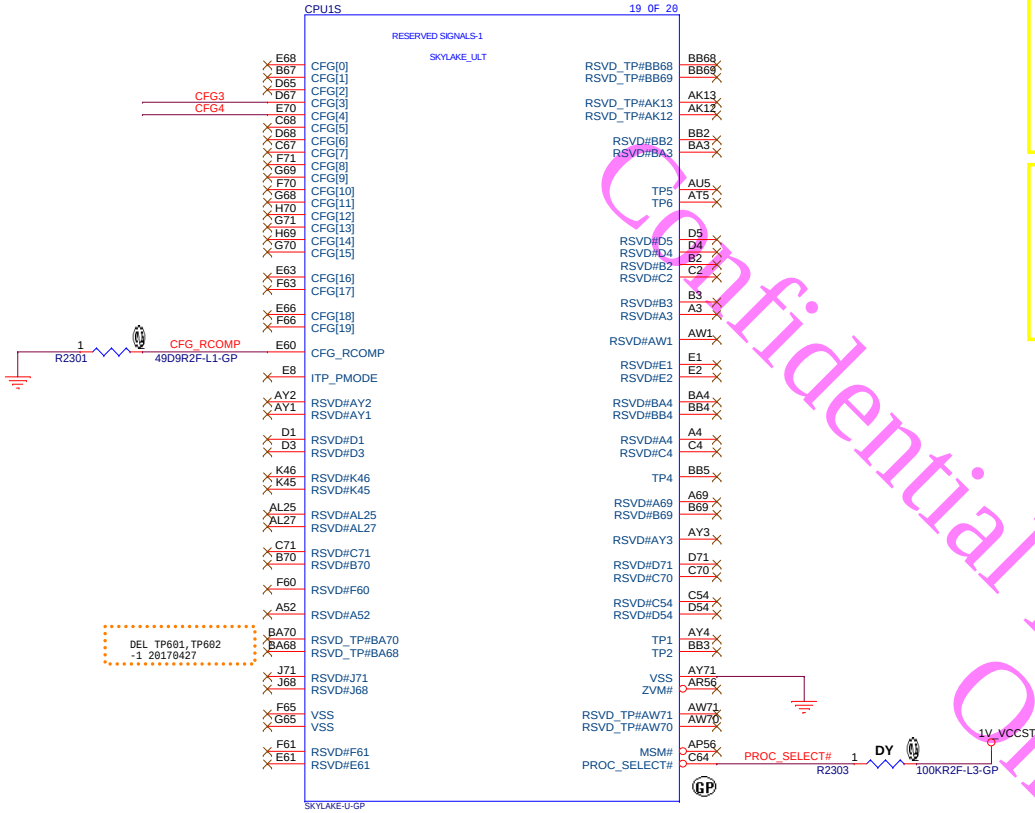
+VCCSTG = 1.0 V



Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_(JTAG/CPU SIDE BAND)		
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 22 of 106	

Main Func = CPU



CPU

PCH strap pin:

CFG3 — R2305 1KR2J-1-GP — DY

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

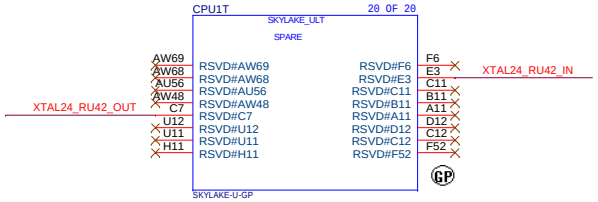
PCH strap pin:

CFG4 — R2304 1KR2J-1-GP

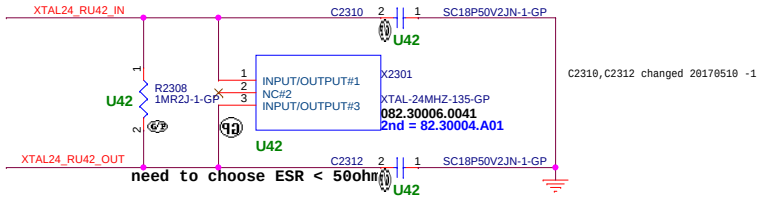
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines



CPU



P/N: 082.30006.0041

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_RESERVED,CFG***

Size	Document Number	Rev
Custom	Woody/Buzz_KBL	-2

Date: Tuesday, July 25, 2017 Sheet 23 of 106

SSID = KBC

Power

- 3D3V_AUX_S5
- 3D3V_S0
- 3D3V_RTC_AUX

Signal

- H_RCIN# 18
- FUN_OFF# 65,89
- LPC_FRAME# CPU 18,68,91
- LPC_AD_CPU_P3 18,68,91
- LPC_AD_CPU_P2 18,68,91
- LPC_AD_CPU_P1 18,68,91
- LPC_AD_CPU_P0 18,68,91
- LPC_CLK_KBC 18
- PLT_RST# 20,61,62,68,89,91
- WLAN_PCIE_WAKE# 24,61
- LID_CLOSE# 64
- LID_CLOSE2# 64
- PTP_PWR_EN# 65
- PURE_HW_SHUTDOWN# 26,40
- PM_CLKRUN# EC 18,91
- ES1_TXD 61,68
- SH_INT# 22
- EC_TP_IN# 24,65
- KBC_BEEP 27
- KB_BL_DET 65
- FAN1_PWM 26,89
- FAN_TACH1 26,89
- Value+ 64
- Value- 64
- KSI0 65,89
- KSI1 65,89
- KSI2 65,89
- KSI3 65,89
- KSI4 65,89
- KSI5 65,89
- KSI6 65,89
- KSI7 65,89
- KSO0 65,89
- KSO1 65,89
- KSO2 65,89
- KSO3 65,89
- KSO4 65,89
- KSO5 65,89
- KSO6 65,89
- KSO7 65,89
- KSO8 65,89
- KSO9 65,89
- KSO10 65,89
- KSO11 65,89
- KSO12 65,89
- KSO13 65,89
- KSO14 65,89
- KSO15 65,89
- KSO16 65,89
- KSO17 65,89
- AC_IN# 44,74
- DC_Protect_EC 44
- KBC_PWRBTN# 64,89
- BAT_IN# 43,44
- DC_IN_OK 44,73,74
- AD_IA 44
- BT_IA 44
- ALL_SYS_PWRGD 20,40
- MODEL_ID_AD 55
- STDBY_LED 64,89
- POWER_LED 64,89
- CHARGE_LED 64,89
- DC_BATFULL 64,89
- SMI1_CLK 18,55,70,73
- SMI1_DATA 18,55,70,73
- BAT_SCL 43,44
- BAT_SDA 43,44
- SPI_WP_ROM 18,25
- EC_TPCLK 65
- EC_TPDATA 65
- ME_UNLOCK 17
- EC_TP_IN# 24,65
- RTCRST_ON 16
- BLON_OUT 55
- AD_OFF 43
- VD_IN1 26
- VD_OUT1 26
- PROCHOT# CPU 22,44,46
- RSMRST# KBC 20
- AMP_MUTE# 27
- 5V_EN 40,45
- KB_BL_PWM 65
- TOUCH_EN 55
- 3V_5S_ENABLE 40

- AC_PRESENT 20
- eDP_BLEN_CPU 3
- PM_PWRBTN# 20
- PCIE_WAKE# 20,61,62

- INT_SERIRQ 18,68,91
- EC_SMI# 3
- EC_SCI# 3

3.3V

- PM_SLP_S3# 20,40,53,60
- PM_SLP_S4# 20,40,51

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

- PD_INT# 73

Type_C

- USB_CHARGER_EN 36
- USB_CHAR_SEL 36
- USB_CHAR_CT1 36

Charger

- WIFI_RF_EN 61
- BLUETOOTH_EN 61,89
- USB_PWR_EN# 35,64
- WLAN_PCIE_WAKE# 24,61
- CHG_ON# 44
- PECI_EC 22
- WLAN_PERST# 61
- WLAN_PWR_EN# 61

- TS_I2C0_SCL_CON 6,55
- TS_I2C0_SDA_CON 6,55
- SYS_PWROK 20

- SPI_SO_ROM 18,25
- SPI_SI_ROM 18,25
- SPI_CLK_ROM 18,25
- SPI_CS_CPU_N0 18,25

Close to the EC

VCC_LPC(Pin9)

For EC power consumption reserver

CPU/G-sensor/Type_C --->
BATTER /CHARGER --->
CPU<---
Touch Pad--->

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

071.09028.000G

GPIOO High Active

Sensitive trace cap

close RN2407

Woody 45W,Buzz UMA 65W Setting

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0K	10.0K	3.000V	3.005V	>=2.875V	
SB	100.0K	20.0K	2.750V	2.759V	>=2.616V	<2.875V
SC	100.0K	33.0K	2.481V	2.493V	>=2.363V	<2.616V
-1	100.0K	47.0K	2.245V	2.259V	>=2.123V	<2.363V
-2	100.0K	64.9K	2.001V	2.017V	>=1.934V	<2.123V
Reserved for project use	100.0K	76.8K	1.867V	1.883V	>=1.758V	<1.934V
Reserved for project use	100.0K	100.0K	1.650V	1.667V	>=1.504V	<1.758V
Reserved for project use	100.0K	143.0K	1.358V	1.374V	>=1.281V	<1.504V
Reserved for project use	100.0K	174.0K	1.204V	1.220V	>=1.126V	<1.281V
Reserved for project use	100.0K	215.0K	1.048V	1.062V	>=0.524V	<1.126V

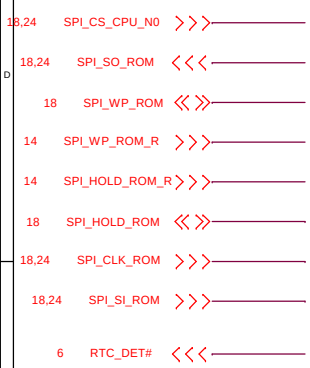
ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0K	3.300V		>= 3.000V	
90W	100.0K	N/A	0.000V			< 0.153 V
30W	10.0K	100.0K	0.300V	0.305 V	>=0.150 V	< 0.425 V
45W	20.0K	100.0K	0.559 V	0.569 V	>=0.425 V	< 0.694 V
120W	33.0K	100.0K	0.819 V	0.831 V	>=0.694 V	< 0.937 V
135W	47.0K	100.0K	1.055 V	1.070 V	>=0.937 V	< 1.177 V
150W	64.9K	100.0K	1.298 V	1.315 V	>= 1.177 V	< 1.399 V
Reserved	76.8K	100.0K	1.453 V	1.470 V	>= 1.399 V	< 1.542 V
Reserved	100.0K	100.0K	1.659 V	1.667 V	>= 1.542 V	< 1.942 V

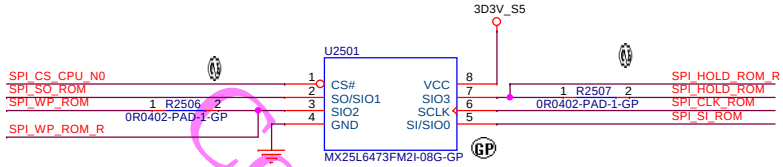
Wistron Corporation	21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC_KB9028
Size	Document Number: Woody/Buzz_KBL
Rev	-2
Date: Tuesday, July 25, 2017	Sheet 24 of 106

Main Func = SPI Flash

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



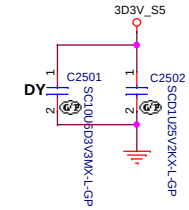


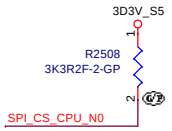
072.25647.000D

2nd = 072.25Q64.0H01 20170308 Change

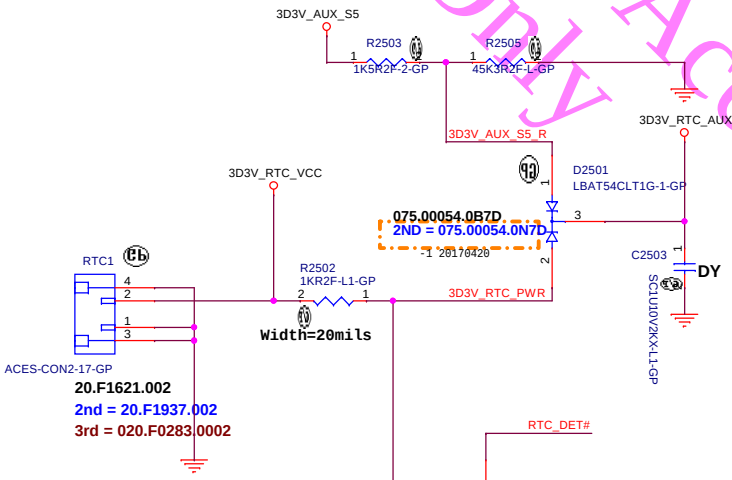
072.25647.000D_MX25L6473FM2I-08G_MXIC
072.25Q64.0H01_W25Q64FVSSIQ_WINBOND

20170215 Delete U2504 For ENG





Main Func = RTC



RTC BATTERY
1st= 023.21212.0001
2nd= 023.22032.0621

Count

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Flash(KBC+PCH)/RTC*

Size: Custom | Document Number: Woody/Buzz KBL | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 25 of 106

24 VD_IN1

24,26,89 FAN1_PWM

24,89 FAN_TACH1

24,40 PURE_HW_SHUTDOWN#

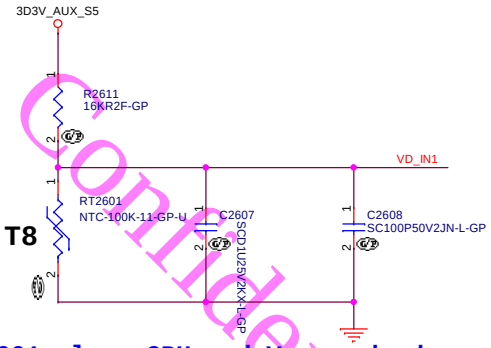
24 VD_OUT1

40,46 VR_RDY

89 FAN_TACH1_C

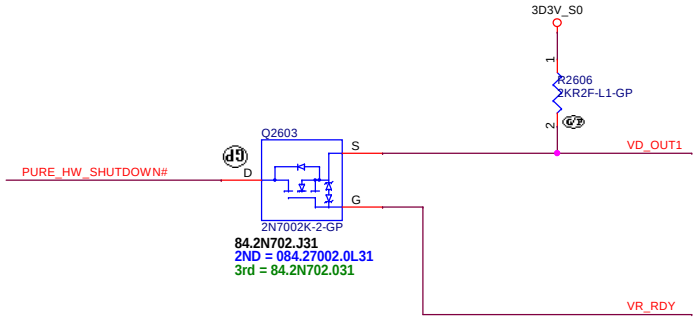
24,26,89 FAN1_PWM

SSID = Thermal

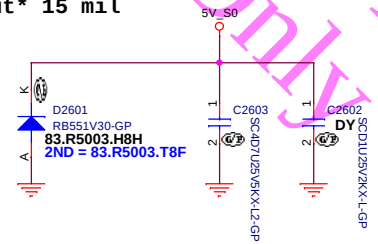


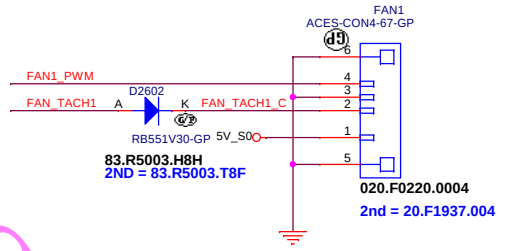
RT2601 close CPU and Vcore chock

VD_IN1 trace 10 mli



Layout 15 mil





Count

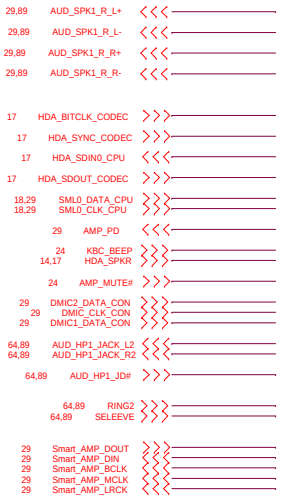
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

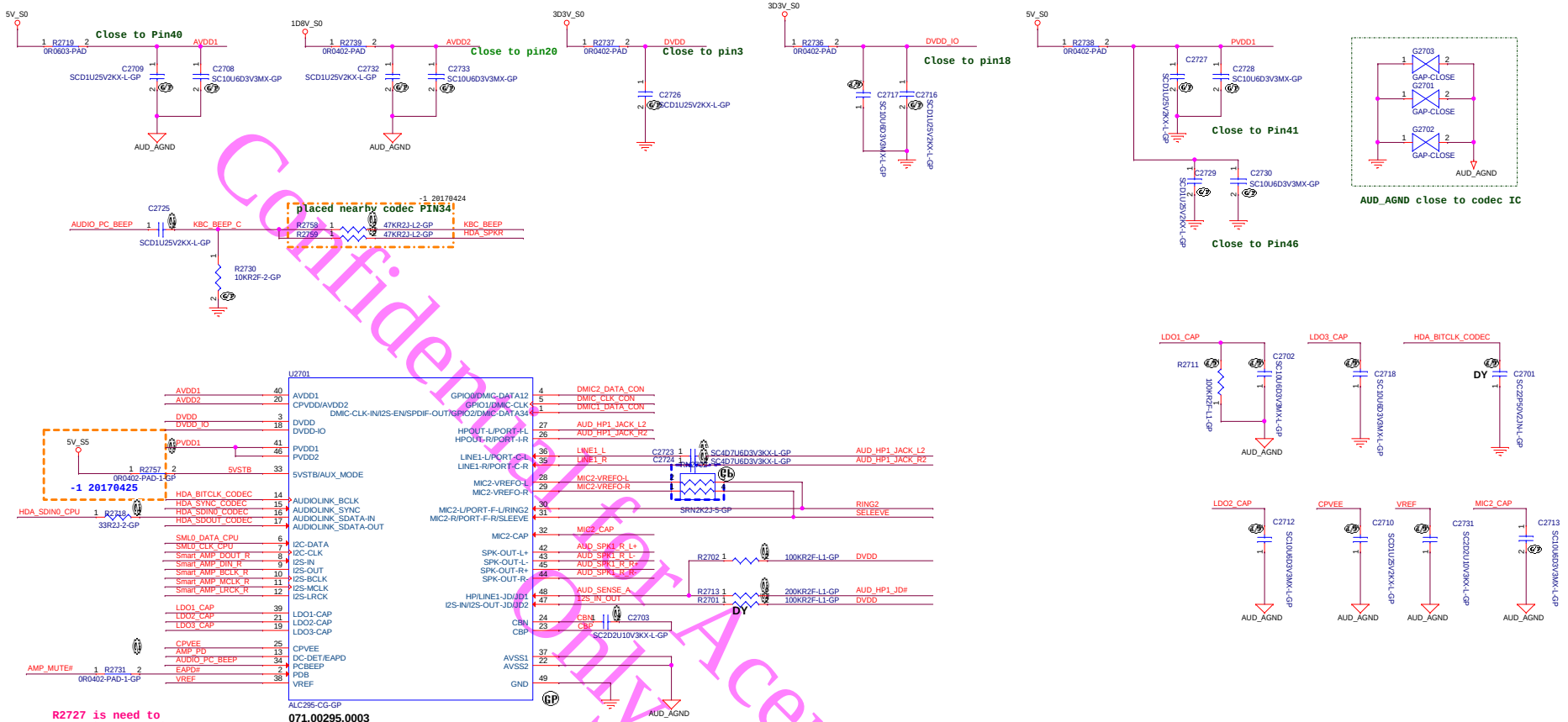
Title: Thermal 7718/Fan Controllor P2793

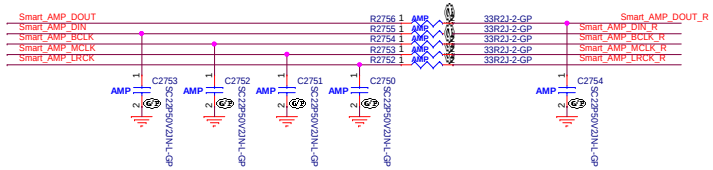
Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 26 of 106

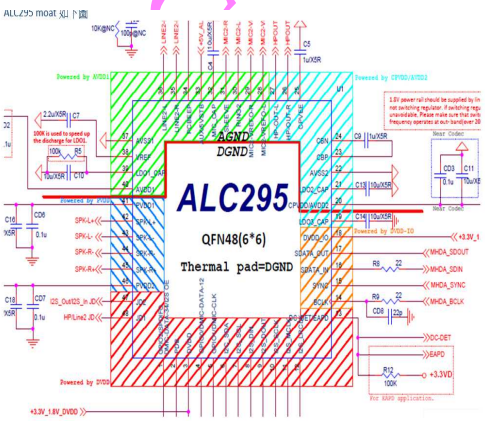
SSID = AUDIO

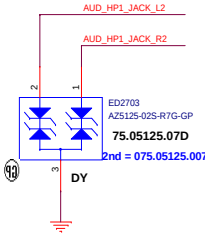


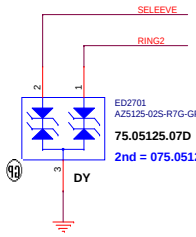




Closed U2701







Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Audio Codec ALC295**
Size: Custom	Document Number: **Woody/Buzz_KBL** Rev: **-2**
Date: Tuesday, July 25, 2017	Sheet 27 of 106

Blanking

Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **Woody/Buzz KBL**	Rev: **-2**
Date: Tuesday, July 25, 2017	Sheet 28 of 106	

SSID = AUDIO

Amplifiers

18,27 SML0_CLK_CPU
18,27 SML0_DATA_CPU
27 Smart_AMP_MCLK
27 Smart_AMP_BCLK
27 Smart_AMP_LRCK
27 Smart_AMP_DIN
27 Smart_AMP_DOUT
27 AMP_PD
27,89 AUD_SPK1_R_L-
27,89 AUD_SPK1_R_L+
27,89 AUD_SPK1_R_R-
27,89 AUD_SPK1_R_R+
89 OUT_RN_CON
89 OUT_RP
89 SPK_RINRVP

CCD

15 CCD_USB20_P
15 CCD_USB20_N
89 CCD_USB20_CON_P
89 CCD_USB20_CON_N

DMIC

27 DMIC_CLK_CON
27 DMIC1_DATA_CON
27 DMIC2_DATA_CON
89 DMIC_CLK_CON_C
89 DMIC1_DATA_CON_C
89 DMIC2_DATA_CON_C

SML0_CLK_CPU R2917 1 2 0R0402-PAD AMP_SCL
SML0_DATA_CPU R2918 1 2 0R0402-PAD AMP_SDA
Smart_AMP_MCLK R2916 1 2 0R0402-PAD AMP_MCLK
Smart_AMP_BCLK R2915 1 2 0R0402-PAD AMP_BCLK
Smart_AMP_LRCK R2914 1 2 0R0402-PAD AMP_LRCK
Smart_AMP_DIN R2913 1 2 0R0402-PAD AMP_DACDAT
Smart_AMP_DOUT R2940 1 2 0R0402-PAD

3P3A_DVDD_IO
AMP_PD
AMP_VDD1V8
AMP_AVDD2_1V8
I2C Address Select ion Low:0x24 Hi :0x26
R2932 1 DY 2 10KR2F-L1-GP
R2933 1 AMP 10KR2F-L1-GP
AUDIO_AMP_ASEL
LDO_A1_5_R
AMP_VREF

U2905 ALC1006-VB-CGT-GP
SPDIF_IN DACDAT LRCK BCLK MCLK SCL SDA BYPASS
SPDIF_OUT/I2S_DATOUT PDB_JD DVDD_IO DVDD ASEL DGND AGND AVDD2 LDO_A1D5 VREF AGND LISENSE+ LISENSE-/LVSENSE+ LVSENSE-
GND NC#48 PGND_R OUT_RN OUT_RP PVDD_R AVDD1 AVDD1 PVDD_L OUT_LP OUT_LN PGND_L NC#37 NC#36 NC#35
RSENSE RVSENSE+ RVSENSE- NC#27 BYPASS_2 GAIN_BTL NC#29 GND NC#31 NC#32 NC#33 NC#34

AMP

SPK_RIP R2928 1 2 0R0402-PAD
SPK_RINRVP R2927 1 2 0R0402-PAD
SPK_RVN R2926 1 2 0R0402-PAD

074.01006.0A13
Output Mode Selection LOW:STL Hi :BTL

-SB 20170314 EMC SUGGEST
Main source:68.00230.041
Seocnd source:68.00206.021
Change main source 20170330

AUD_SPK1_R_L- ER2914 1 HCB1608KF121T30-GP
AUD_SPK1_R_L+ ER2915 1 HCB1608KF121T30-GP
AUD_SPK1_R_R- ER2916 1 HCB1608KF121T30-GP
AUD_SPK1_R_R+ ER2917 1 HCB1608KF121T30-GP
OUT_RN
OUT_RP

Trace width=40mil

AUD_SPK1_L- CON
AUD_SPK1_L+ CON
AUD_SPK1_R- CON
AUD_SPK1_R+ CON
OUT_RN_CON
R2921 0R0402-PAD
R2923 0R0402-PAD
R2922 0R0402-PAD
SPK_RIP
SPK_RINRVP
SPK_RVN

Speaker 20170314 SB Change
SPK1 HR-CON5-6-GP
020.F000M.0006
2nd = 020.F1038.0006
Need change 20170405
Main:020.F000M.0006
2nd:020.F1038.0006
PIN5: SUBWOOFER -
PIN6: SUBWOOFER +

SPK_VDD5V
C2912 C2913 C2914 C2915 SC2D2U10V3KX-L-GP

Figure 30. Application Diagram With Speaker Protection

3P3A_DVDD_IO R2960 100KR2F-L3-GP AMP_PD
BYPASS C2911 SC2D2U10V3KX-L-GP
BYPASS_2 C2916 SC2D2U10V3KX-L-GP
AMP_BTL R2925 0R0402-PAD

3D3V_S0 R2934 0R0402-PAD 3P3A_DVDD_IO
AMP_VDD1V8 R2936 0R0402-PAD AMP_AVDD2_1V8
1D8V_S0 R2935 0R0402-PAD AMP_VDD1V8
5V_S0 R2937 0R0402-PAD SPK_VDD5V
R2938 20KR2F-L3-GP DY

Wait Check

AUD_SPK1_R_L+ AUD_SPK1_R_L- ED2901 AZ5125-02S-R7G-GP 75.05125.07D 2nd = 075.05125.007D
AUD_SPK1_R_R- AUD_SPK1_R_R+ ED2902 AZ5125-02S-R7G-GP 75.05125.07D 2nd = 075.05125.007D
OUT_RP OUT_RN DY ED2903 AZ5125-02S-R7G-GP 75.05125.07D 2nd = 075.05125.007D

A. Pin define

Note

CCD Module

MB Connecter		CCD connector pin	MIC-R PCB	MIC-L PCB
Pin 1	3D3V_CAMERA_S0	1		
Pin 2	3D3V_CAMERA_S0		1	
Pin 3	3D3V_CAMERA_S0			1
Pin 4	CCD_USB20_CON_N	2		
Pin 5	CCD_USB20_CON_P	3		
Pin 6	GND	4		
Pin 7	DMIC2_DATA_CON	6		
Pin 8	DMIC_CLK_CON	5		
Pin 9	DMIC_CLK_CON		3	
Pin 10	DMIC_CLK_CON			3
Pin 11	GND		4	
Pin 12	DMIC1_DATA_CON		2	
Pin 13	DMIC1_DATA_CON			2
Pin 14	GND			4
MB Connecter				CCD Connecter

3D3V_CAMERA_S0
MICBD1 ACES-CON14-9-GP
20.F1633.014
2nd = 20.F1261.014
DMIC2_DATA_CON_C ER2957 33R2J-L1-GP DMIC2_DATA_CON
DMIC_CLK_CON_C ER2955 BLM15AG121SN1-GP DMIC_CLK_CON
68.00084.921 2nd = 68.00217.401
-1 20170505 EMC SUGGEST
DMIC1_DATA_CON_C ER2956 33R2J-L1-GP DMIC1_DATA_CON

Camera Power

3D3V_S0 F2901 POLYSW-1D1A6V-9-GP-U 69.48001.081 2nd = 69.50011.081
3D3V_CAMERA_S0 C2958 C2959 SC2D2U10V3KX-L-GP

-SB 20170314 EMC SUGGEST
CCD_USB20_CON_P CCD_USB20_CON_N EL2901 FILTER-4P-137-GP-U CCD_USB20_P CCD_USB20_N
68.01012.20B 2nd = 68.00396.001 3rd = 068.24900.2001

CCD_USB20_CON_N CCD_USB20_CON_P EU2905 AZC099-04S-2-GP 5V_S0
075.09904.0A7C 2nd = 075.01256.007C 3rd = 75.09904.07C

DMIC_CLK_CON_C DMIC1_DATA_CON_C DMIC2_DATA_CON_C EC2961 EC2962 EC2963 SC2D2U10V3KX-L-GP
-SB 20170314 MOUNT EMC SUGGEST

Count

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Title: Speaker/AMP/DMIC

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USB1

15 USB1_USB20_N
15 USB1_USB20_P
15 USB1_USB30_RX_N
15 USB1_USB30_RX_P
15 USB1_USB30_TX_N
15 USB1_USB30_TX_P
89 USB1_CON_USB20_N
89 USB1_CON_USB20_P

USB2

36 USB2_CHAR_N
36 USB2_CHAR_P
15 USB2_USB30_RX_N
15 USB2_USB30_RX_P
15 USB2_USB30_TX_N
15 USB2_USB30_TX_P
89 USB2_CON_USB20_N
89 USB2_CON_USB20_P

USB Power enable

24,64 USB_PWR_EN#

Low Active 2A

5V_S5 → C3501 SC1U10V2KX-L1-GP → U3501 SY6288DAAC-GP (IN, EN#, OUT, GND, OC#) → 5V_USB30 → C3502 SCD1U25V2KX-L-GP

074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

5V_USB30 → C3504 SC100U6D3V6MX-GP
5V_USB30_CHARGER → C3516 SC100U6D3V6MX-GP

USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

EU3501 L05ESDL5V0NA-4-GP
USB1_USB30_RX_N / RX_P / TX_N / TX_P ↔ USB1_USB30_RX_N / RX_P / TX_CON_N / TX_CON_P
SCD1U25V2KX-L-GP: C3508, C3509

075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30 → USB1 SKT-USB13-348-GP-U
20170309 Change
20170324 Change symbol
USB1_CON_USB20_N/P, USB1_USB30_RX_N/P, USB1_USB30_TX_CON_N/P
VBUS, D-, D+, GND-DRAIN, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, CHASSIS#12, CHASSIS#13, GND, USB3.0

022.10005.08R1
2nd = 022.10005.08Q1
3rd = 022.10005.08W1

EL3501 FILTER-4P-137-GP-U
USB1_USB20_N/P ↔ USB1_CON_USB20_N/P

68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

EU3503 AZC099-04S-2-GP
USB1_CON_USB20_N/P, USB2_CON_USB20_N/P, I/O1, I/O2, I/O3, I/O4, GND, VDD, 5V_S5

075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

EU3502 L05ESDL5V0NA-4-GP
USB2_USB30_RX_N / RX_P / TX_N / TX_P ↔ USB2_USB30_RX_N / RX_P / TX_CON_N / TX_CON_P
SCD1U25V2KX-L-GP: C3510, C3511

075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30_CHARGER → USB2 SKT-USB13-348-GP-U
20170309 Change
20170324 Change symbol
USB2_CON_USB20_N/P, USB2_USB30_RX_N/P, USB2_USB30_TX_CON_N/P
VBUS, D-, D+, GND-DRAIN, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, CHASSIS#12, CHASSIS#13, GND, USB3.0

022.10005.08R1
2nd = 022.10005.08Q1
3rd = 022.10005.08W1

EL3502 FILTER-4P-137-GP-U
USB2_CHAR_N/P ↔ USB2_CON_USB20_N/P

68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

Count

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Title: **USB 3.0**

Size	Document Number	Rev
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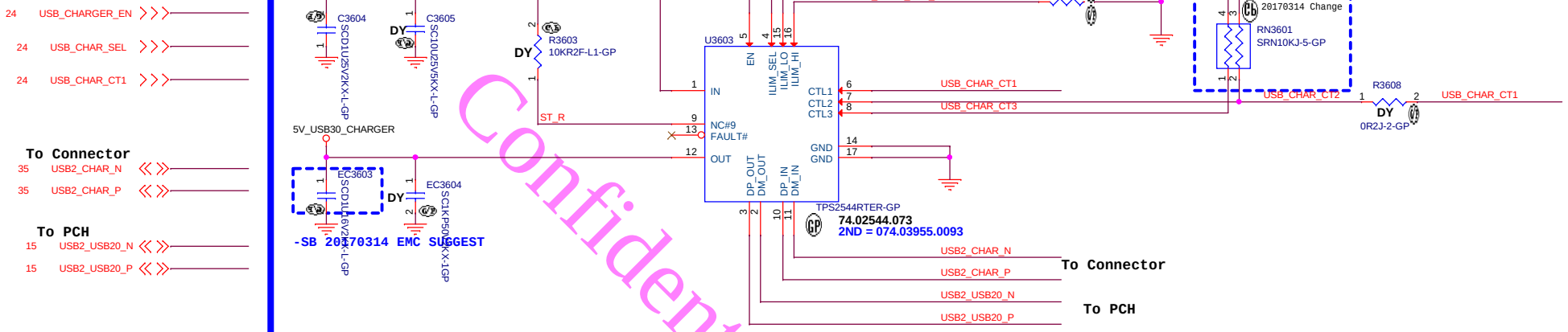

CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

Count

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Title: USB CHARGER

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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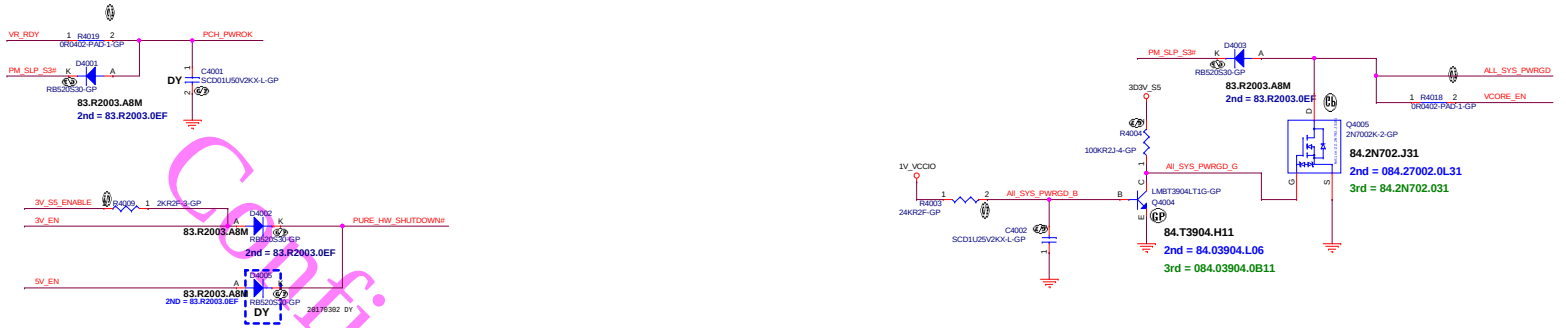
Power Sequence

- 26,46 VR_RDY
- 20 PCH_PWROK
- 20,24,40,53,60 PM_SLP_S3#
- 24 3V_S5_ENABLE
- 45 3V_EN
- 24,45 5V_EN
- 34,26 PURE_HW_SHUTDOWN#
- 20,24 ALL_SYS_PWRGD
- 46 VCORE_EN

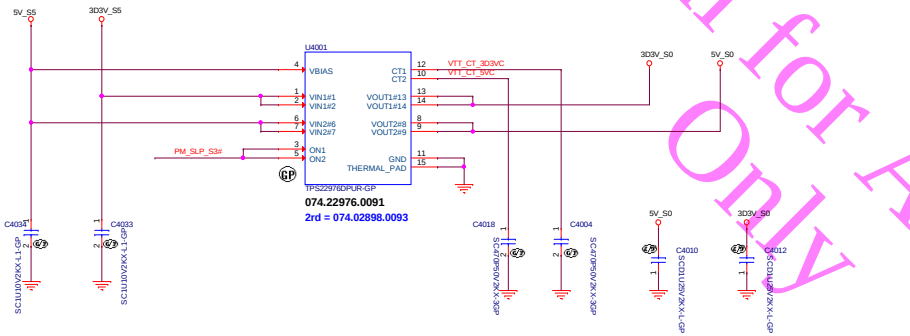
Run Power

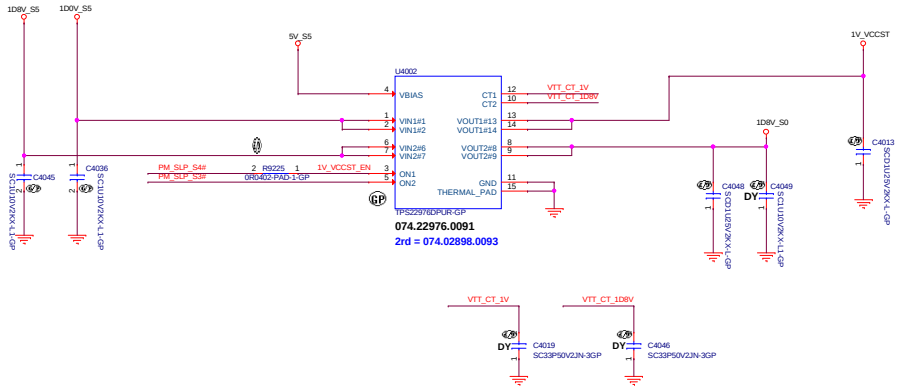
- 20,24,51 PM_SLP_S4#
- 20,24,40,53,60 PM_SLP_S3#

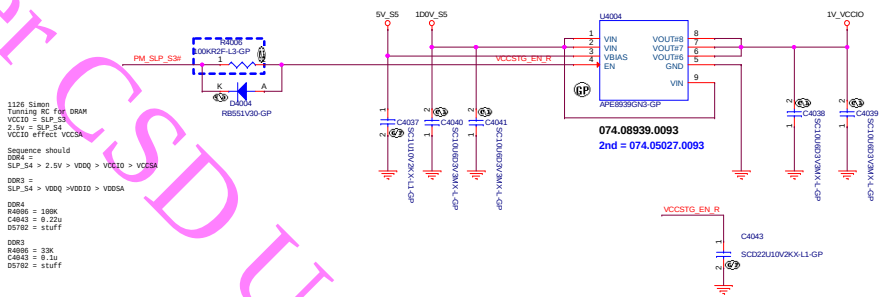
Power Sequence



ANNIE Run Power







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Title	Power Plane Enable & SEQUENCE	
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
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Title: ***Reserved***		
Size: A4	Document Number: **Woody/Buzz KBL**	Rev: **-2**
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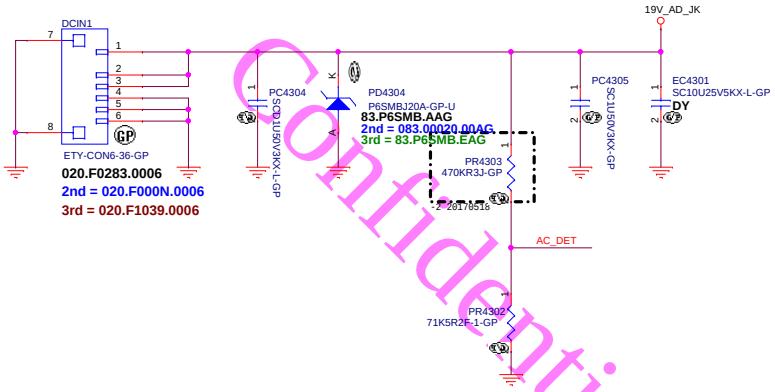
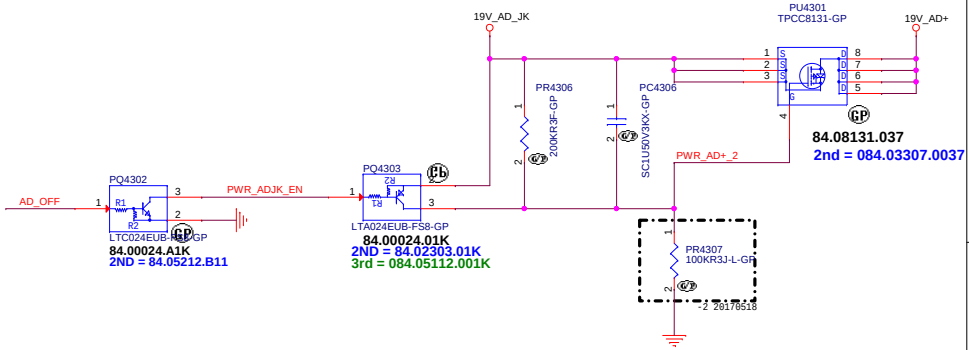
24 AD_OFF
24,44 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA
89 BAT_G
89 BAT_IN#_1
89 BATA_SCL_1
89 BATA_SDA_1
64 BAT_RST
74 AC_DET

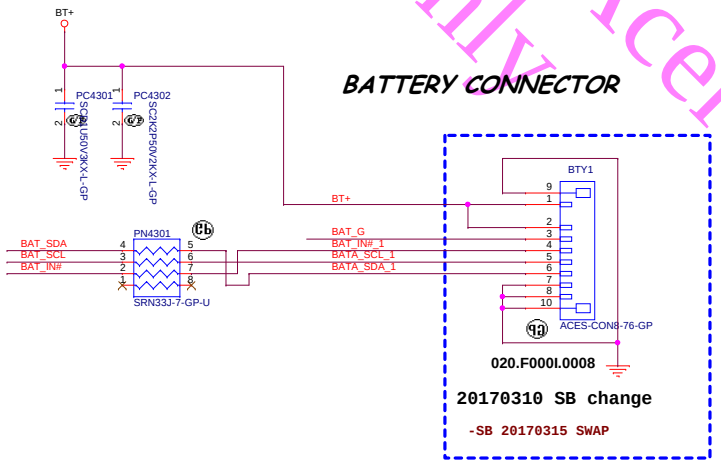
ANNIE solution

Adaptor in to generate DCBATOUT

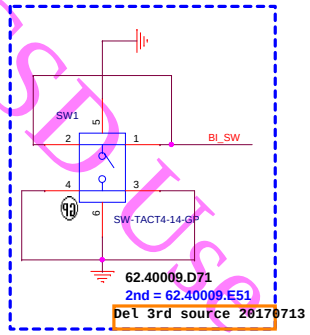




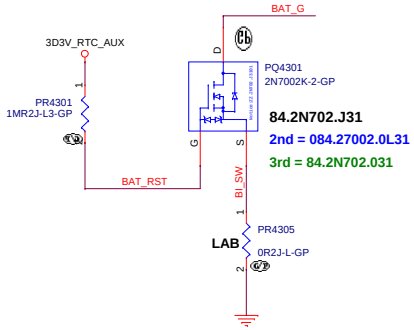
BATTERY CONNECTOR



Battery Insert



20170210 change



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Title: BATT CONN		
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
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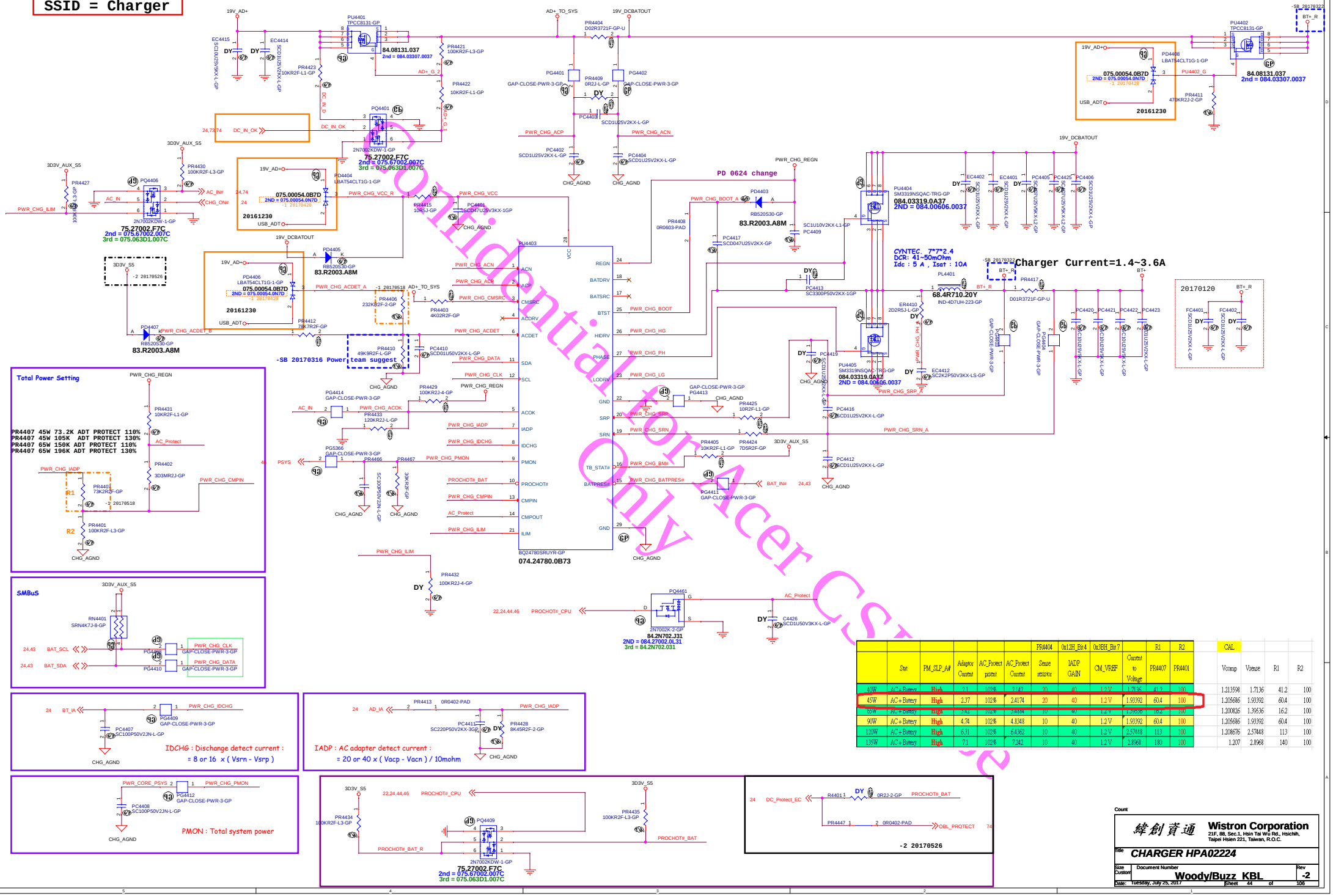
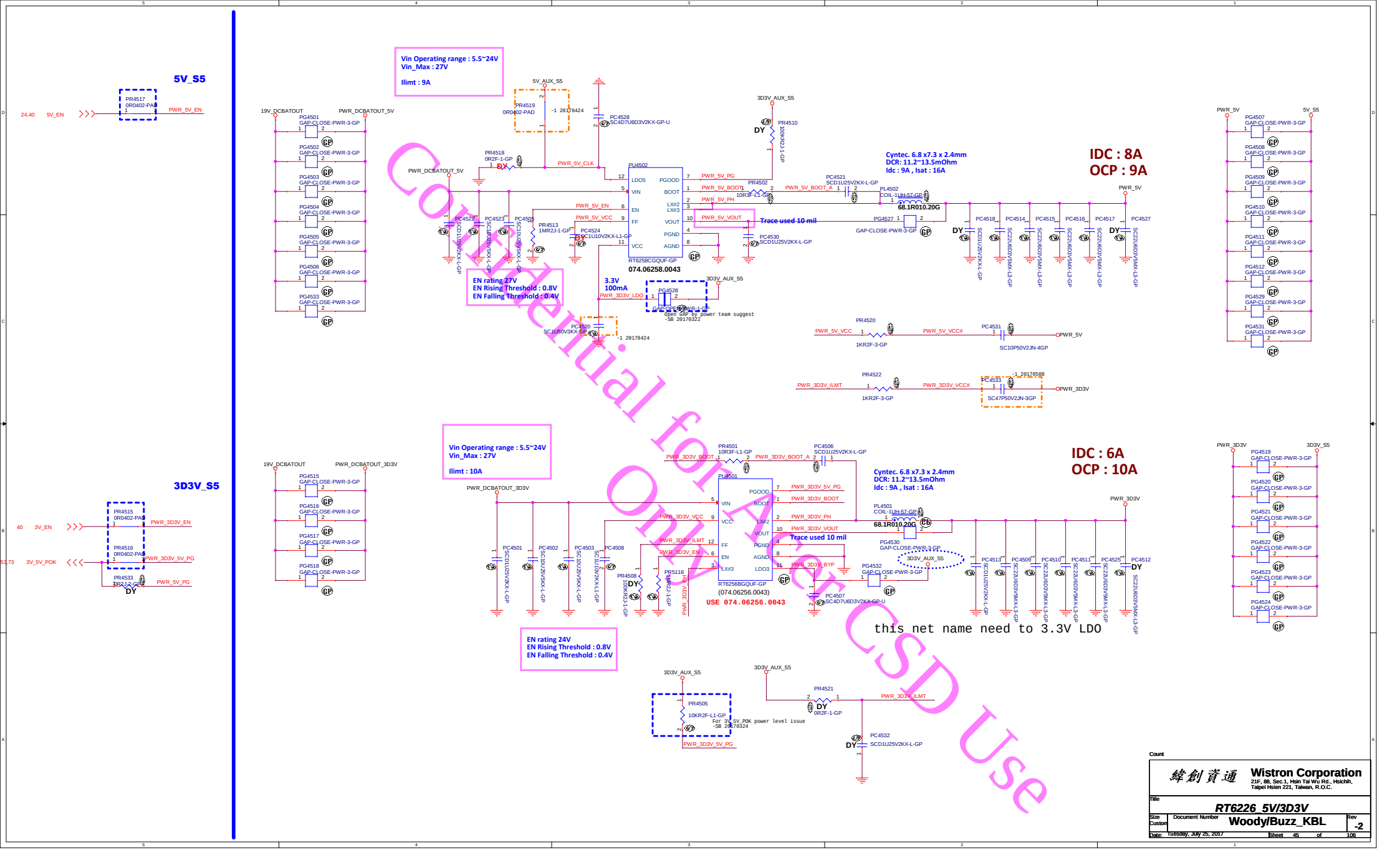
SSID = Charger



	Stat	PM_SLP_A#	Adaptor Current	AC_Protect protect	AC_Protect Current	PR4404 Sense resistor	0x12H_Bit 4 IADP GAIN	0x3BH_Bit 7 CM_VREF	Current to Voltage	R1 PR4407	R2 PR4401	CAL Vcomp	Vsense	R1	R2
40W	AC + Battery	High	2.1	102%	2.142	20	40	1.2 V	1.7136	41.2	100	1.213598	1.7136	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10	40	1.2 V	1.39536	16.2	100	1.200826	1.39536	16.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
120W	AC + Battery	High	6.31	102%	6.4362	10	40	1.2 V	2.57448	113	100	1.208676	2.57448	113	100
135W	AC + Battery	High	7.1	102%	7.242	10	40	1.2 V	2.8968	180	100	1.207	2.8968	140	100


5V_S5
24.40 5V_EN
PR4517 0R0402-PAD
PWR_5V_EN
Vin Operating range : 5.5~24V
Vin_Max : 27V
Ilimt : 9A
19V_DCBATOUT
PWR_DCBATOUT_5V
5V_AUX_S5
PR4519 0R0402-PAD
PC4528 SC4D7U6D3V2KX-GP-U
3D3V_AUX_S5
PR4510 10KR2J-1-GP
DY
PR4518 0R2F-1-GP
PWR_5V_CLK
PU4502
RT6258CGQUF-GP
074.06258.0043
LDO5
VIN
EN
FF
PGOOD
BOOT
LX#2
LX#3
VOUT
PGND
AGND
VCC
PWR_5V_PG
PWR_5V_BOOT
PWR_5V_PH
PWR_5V_VOUT
PWR_5V_EN
PWR_5V_VCC
PR4513 1MR2J-1-GP
PC4524 SC1U10V2KX-L1-GP
PR4502 10R3F-L1-GP
PWR_5V_BOOT_A
PC4521 SCD1U25V2KX-L-GP
PL4502 COIL-1UH-57-GP
68.1R010.20G
Cyntec. 6.8 x7.3 x 2.4mm
DCR: 11.2~13.5mOhm
Idc : 9A , Isat : 16A
Trace used 10 mil
IDC : 8A
OCP : 9A
PG4527 GAP-CLOSE-PWR-3-GP
PC4518
PC4514
PC4515
PC4516
PC4517
PC4527
SC22U6D3V5MX-L3-GP
PWR_5V
EN rating 27V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
3.3V
100mA
PWR_3D3V_LDO
PG4528 GAP-CLOSE-PWR-1-GP
Open GAP by power team suggest -SB 20170322
PC4520 SC1U50V3KX-GP
-1 20170424
PR4520 1KR2F-3-GP
PWR_5V_VCC#
PC4531 SC10P50V2JN-4GP
PR4522 1KR2F-3-GP
PWR_3D3V_ILMT
PWR_3D3V_VCC#
PC4533 SC47P50V2JN-3GP
-1 20170508
PG4507 GAP-CLOSE-PWR-3-GP
PG4508
PG4509
PG4510
PG4511
PG4512
PG4529
PG4531
3D3V_S5
40 3V_EN
53.73 3V_5V_POK
PR4515 0R0402-PAD
PR4516 0R0402-PAD
PR4533 0R2J-2-GP
PWR_3D3V_EN
PWR_3D3V_5V_PG
PWR_5V_PG
Vin Operating range : 5.5~24V
Vin_Max : 27V
Ilimt : 10A
19V_DCBATOUT
PWR_DCBATOUT_3D3V
PG4515 GAP-CLOSE-PWR-3-GP
PG4516
PG4517
PG4518
PWR_3D3V_BOOT
PWR_3D3V_BOOT_A
PC4506 SCD1U25V2KX-L-GP
PR4501 10R3F-L1-GP
PU4501
RT6256BGQUF-GP
(074.06256.0043)
USE 074.06256.0043
PGOOD
BOOT
LX#2
VOUT
PGND
AGND
LDO3
PWR_3D3V_5V_PG
PWR_3D3V_BOOT
PWR_3D3V_PH
PWR_3D3V_VOUT
PWR_3D3V_VCC
PWR_3D3V_ILMT
PWR_3D3V_EN
PWR_3D3V_BYP
PL4501 COIL-1UH-57-GP
68.1R010.20G
Cyntec. 6.8 x7.3 x 2.4mm
DCR: 11.2~13.5mOhm
Idc : 9A , Isat : 16A
Trace used 10 mil
IDC : 6A
OCP : 10A
PG4530 GAP-CLOSE-PWR-3-GP
PG4532 GAP-CLOSE-PWR-3-GP
PC4507 SC4D7U6D3V2KX-GP-U
PC4501
PC4502
PC4503
PC4508
PR5116
PR4508 100KR2J-1-GP
PC4513
PC4509
PC4510
PC4511
PC4525
PC4512
SC22U6D3V9MX-L3-GP
PWR_3D3V
this net name need to 3.3V LDO
EN rating 24V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
PR4505 10KR2F-L1-GP
For 3V_5V_POK power level issue -SB 20170324
PR4521 0R2F-1-GP
PC4532 SCD1U25V2KX-L-GP
PG4519 GAP-CLOSE-PWR-3-GP
PG4520
PG4521
PG4522
PG4523
PG4524
Confidential for ACER CSD Use Only
Count
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RT6226_5V/3D3V
Size Custom
Document Number Woody/Buzz_KBL
Rev -2
Date: Tuesday, July 25, 2017
Sheet 45 of 106

Main Func = CPU_CORE

OFFPAGE

22,24,44 PROCHOT#_CPU
7 SVID_ALERT#_CPU
7 SVID_CLK_CPU
7 SVID_DATA_CPU
26,40 VR_RDY
40 VCORE_EN
7 VSSCORE_SENSE
7 VCCCORE_SENSE
8 VCCGT_SENSE
8 VSSGT_SENSE
8 VSSSA_SENSE
8 VCCSA_SENSE
44 PSYS

50 PWR_VCCSA_ISUMP
50 PWR_VCCSA_ISUMN
48 PWR_VCCGT_ISUMP
48 PWR_VCCGT_ISUMN
47 PWR_VCORE_ISUMP_A
47 PWR_VCORE_ISUMN_A
47 PWR_VCORE_ISUMP_B
47 PWR_VCORE_ISUMN_B

50 PWR_VCCSA_PWM
48 PWR_VCCGT_PWM
47 PWR_VCORE_PWMA
46,47 PWR_VCORE_PWMB
46,47 PWR_VCORE_PWMB
47,48,50 PWR_VCORE_FCCM#

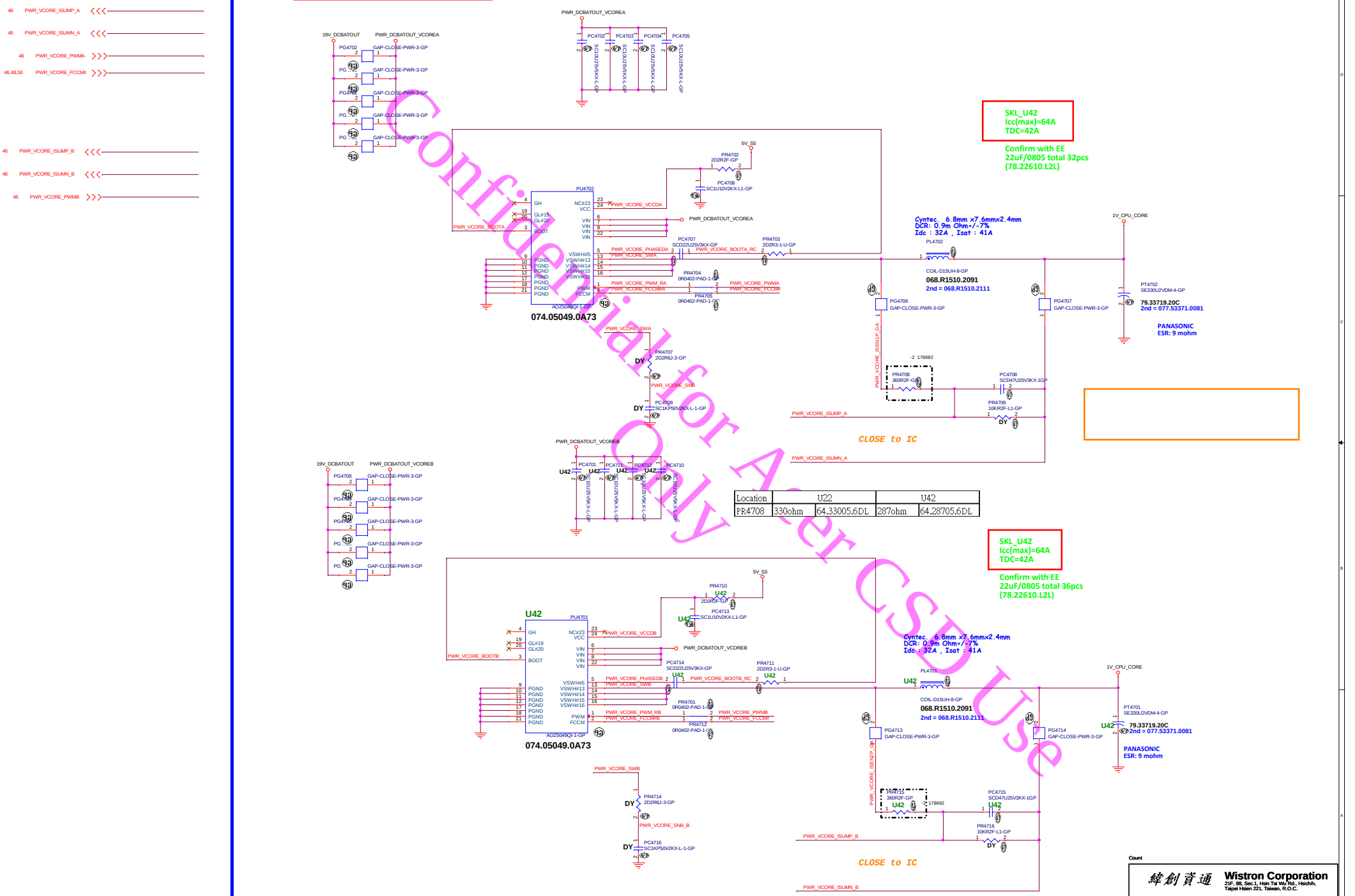
BOM control				
Location	U22		U42	
PR4604	4.42K	64.44215.6DL	4.42K	64.44215.6DL
PR4605	9.53K	64.95315.6DL	26.1K	64.26125.6DL
PR4606	18K	64.18025.55L	18K	64.18025.55L
PR4615	665ohm	64.66505.6DL	665ohm	64.66505.6DL
PC4616	220PF	78.22124.2FL	220PF	78.22124.2FL
PR4620	4.32K	64.43215.6DL	4.32K	64.43215.6DL
PR4621	9.1K	64.91015.6DL	5.62K	64.56215.6DL
PR4622	8.66K	64.86615.6DL	8.66K	64.86615.6DL
PR4624	27.4K	64.27425.6DL	27.4K	64.27425.6DL
PR4635	42.2K	64.42225.6DL	42.2K	64.42225.6DL
PR4640	28K	64.28025.6DL	31.6K	64.31625.6DL
PR4650	28.7K	64.28725.6DL	28.7K	64.28725.6DL
PR4655	8.45K	64.84515.6DL	8.45K	64.84515.6DL
PR4659	47.5k	64.47525.6DL	52.3K	64.52325.6DL
PR4668	76.8K	64.76825.6DL	76.8K	64.76825.6DL
PR4671	178K	64.17835.6DL	178K	64.17835.6DL

	PR4652	PR4682
U22	0	0
U42	DY	DY

	PR4684
U22	DY
U42	1R

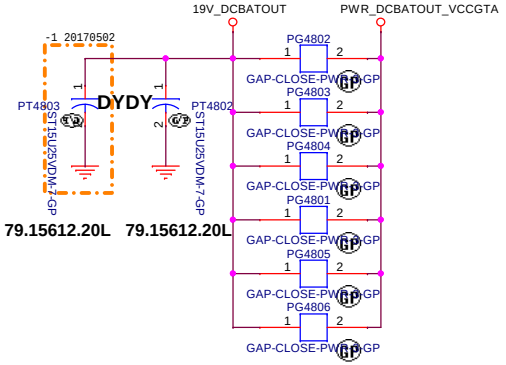
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_VCORE(1/3)
Size: Custom	Document Number: Woody/Buzz_KBL
Rev	-2
Date: Tuesday, July 25, 2017	Sheet 46 of 106

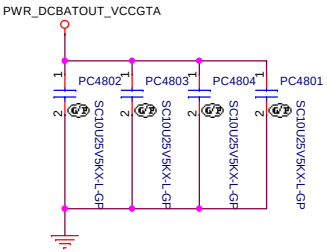
Main Func = CPU_CORE

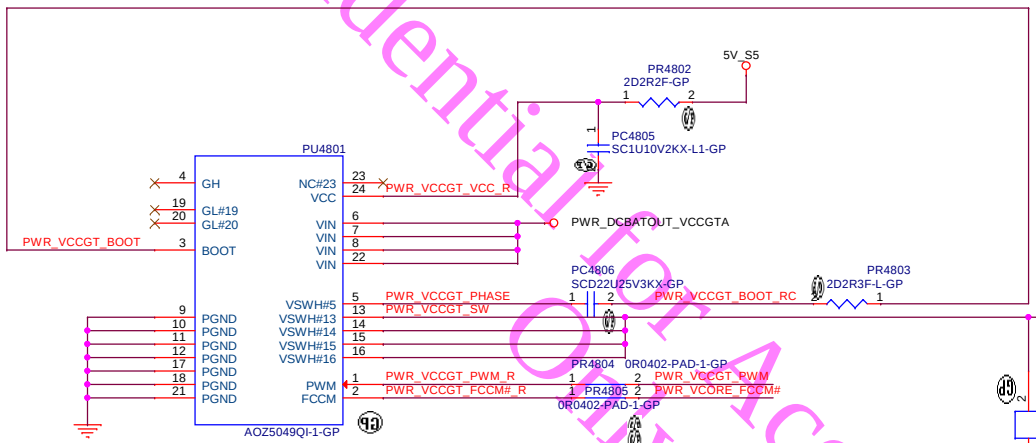


Main Func = CPU_CORE

46 PWR_VCCGT_ISUMP
46 PWR_VCCGT_ISUMN
46 PWR_VCCGT_PWM
46,47,50 PWR_VCORE_FCCM#



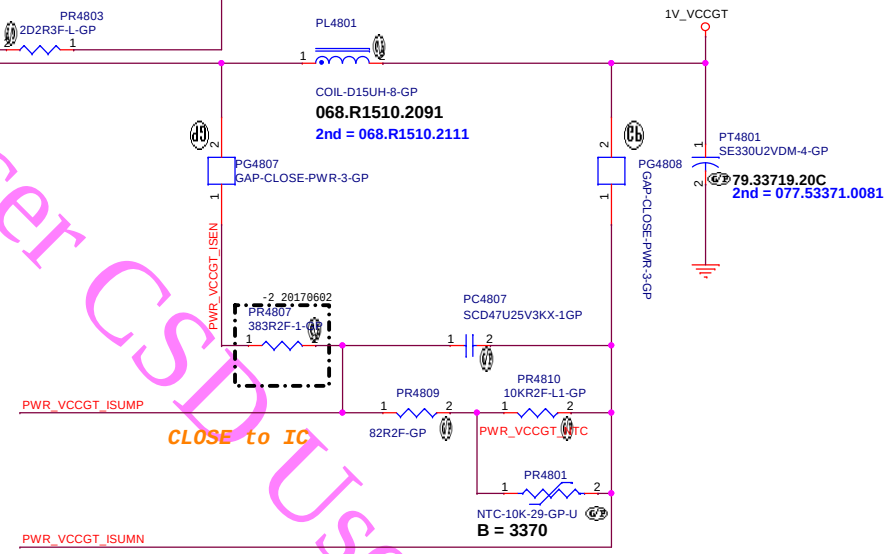


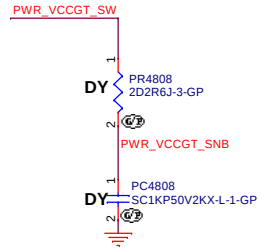


SKL_U42
Icc(max)=28A
TDC=12A

Confirm with EE
22uF/0805 total 26pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A





Location	U22		U42	
PR4807	430ohm	64.43005.6DL	324ohm	64.32405.6DL

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCCGT(3/3)
Size: A3
Document Number: Woodly/Buzz_KBL
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Date: Tuesday, July 25, 2017
Sheet 48 of 106

Blanking

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Woody/Buzz_KBL	-2

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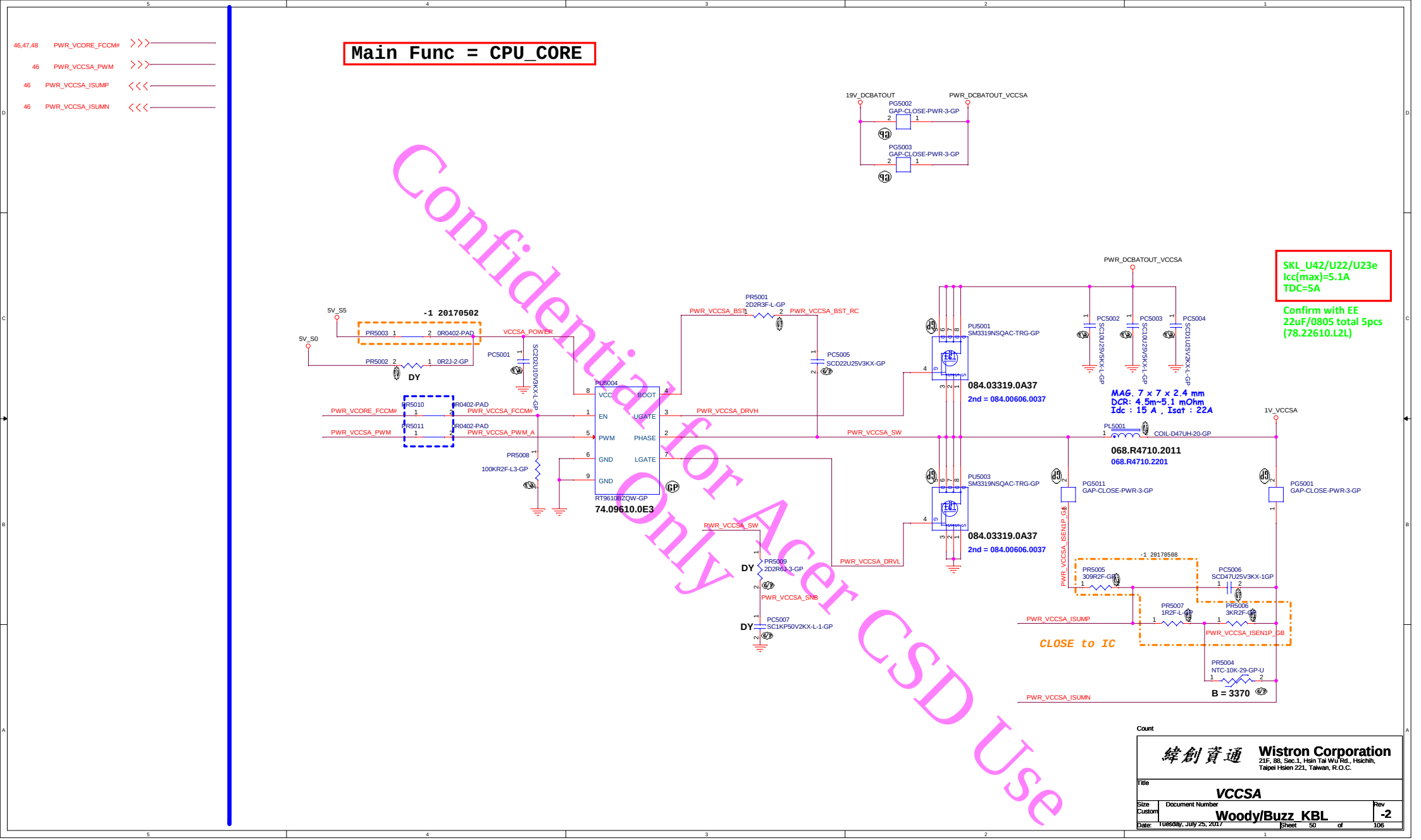
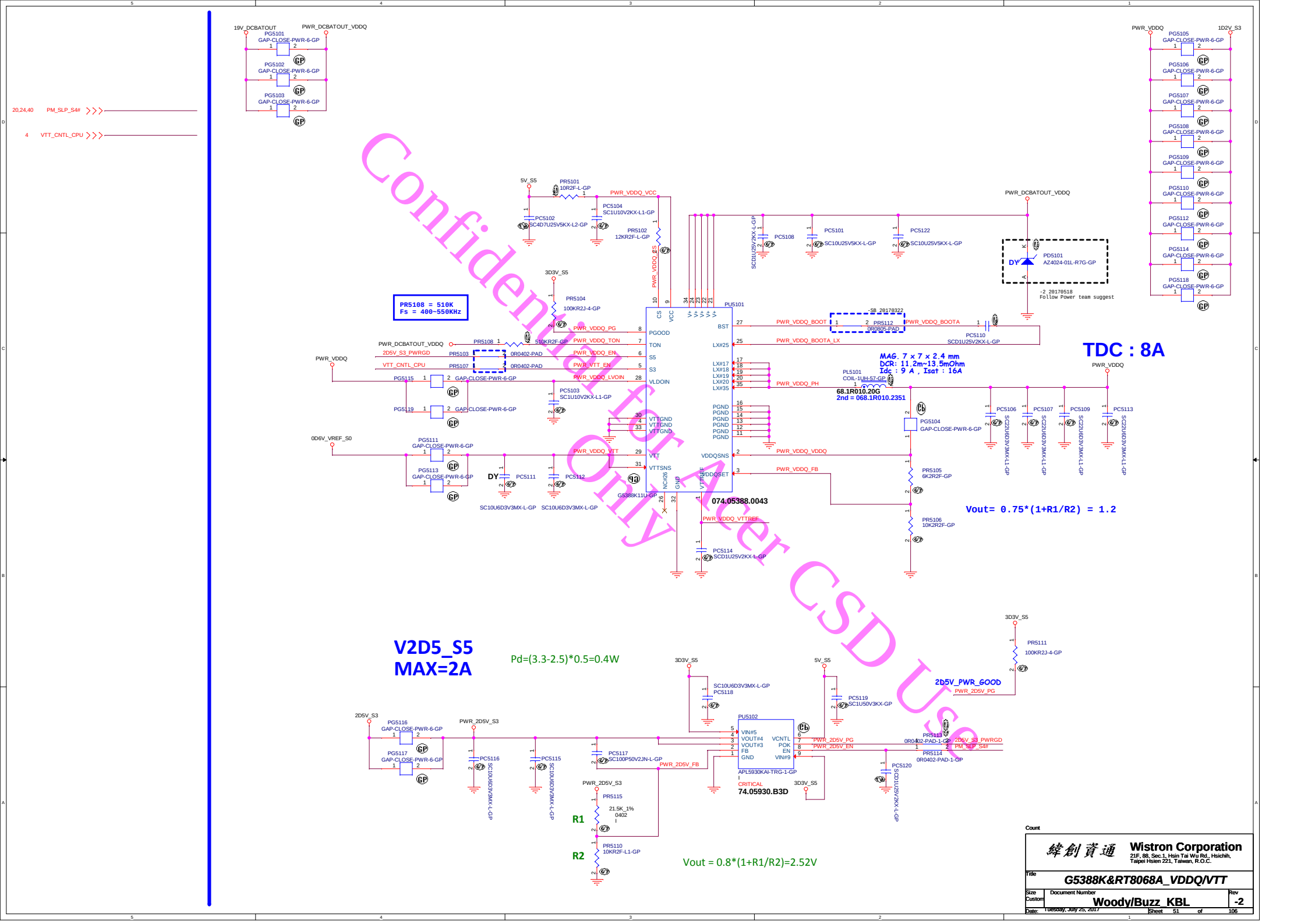




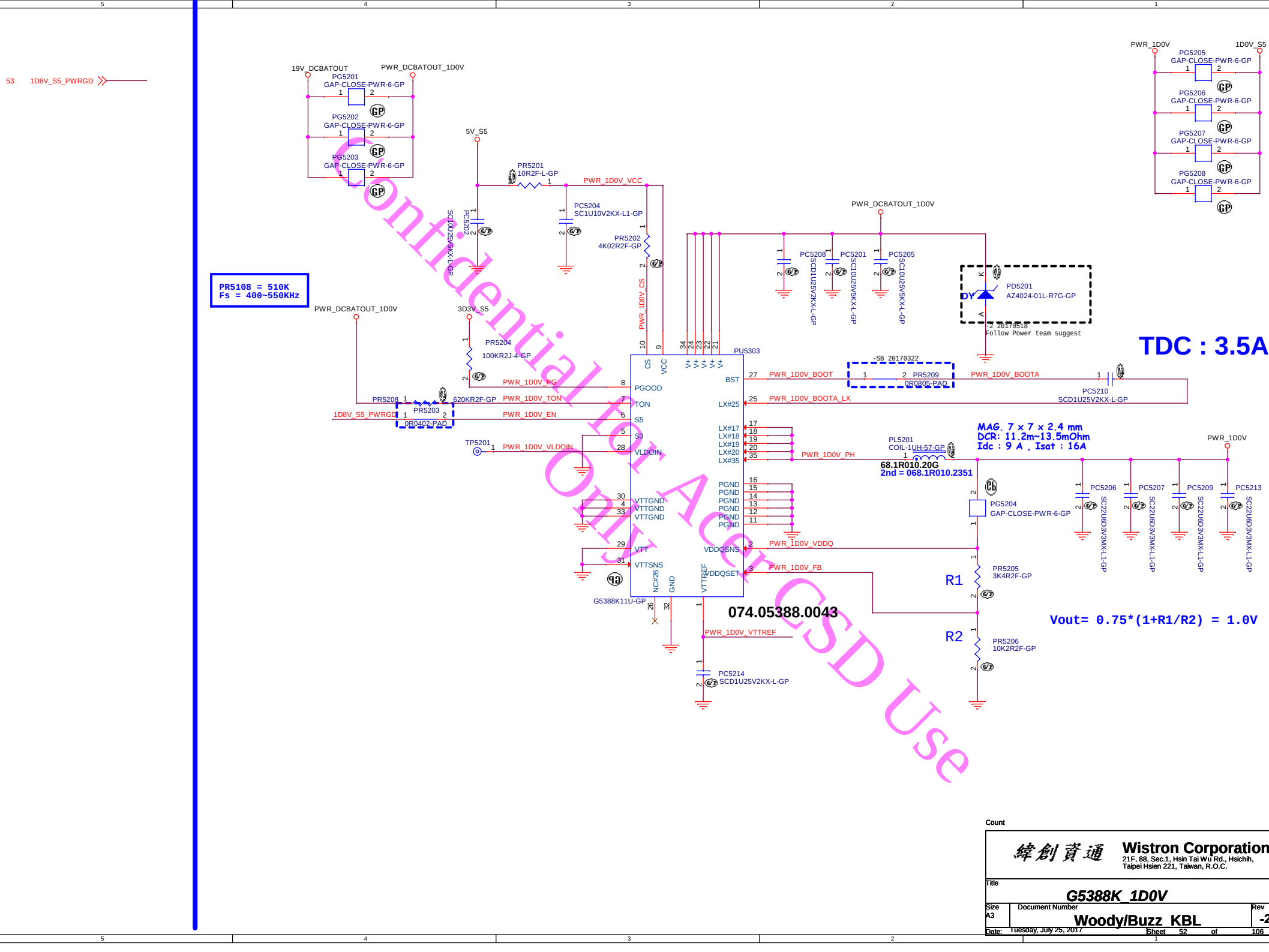
Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: G5388K&RT8068A_VDDQ/VTT

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

Date: Tuesday, July 25, 2017 | Sheet 51 of 106


53 1D8V_S5_PWRGD
19V_DCBATOUT
PWR_DCBATOUT_1D0V
PG5201 GAP-CLOSE-PWR-6-GP
PG5202 GAP-CLOSE-PWR-6-GP
PG5203 GAP-CLOSE-PWR-6-GP
5V_S5
PR5201 10R2F-L-GP
PWR_1D0V_VCC
PC5204 SC1U10V2KX-L1-GP
PR5202 4K02R2F-GP
PC5202 SC10U25V5KX-L-GP
PR5108 = 510K
Fs = 400~550KHz
PWR_DCBATOUT_1D0V
3D3V_S5
PR5204 100KR2J-4-GP
PWR_1D0V_PG
PR5208 620KR2F-GP
PWR_1D0V_TON
1D8V_S5_PWRGD
PR5203 0R0402-PAD
PWR_1D0V_EN
TP5201
PWR_1D0V_VLDOIN
PU5303
CS
VCC
PGOOD
TON
S5
S3
VLDOIN
VTTGND
VTT
VTTSNS
NC#26
GND
VTTREF
V+
BST
LX#25
LX#17
LX#18
LX#19
LX#20
LX#35
PGND
VDDQSNS
VDDQSET
G5388K11U-GP
PWR_1D0V_VTTREF
PC5214 SCD1U25V2KX-L-GP
PWR_DCBATOUT_1D0V
PC5208 SCD1U25V2KX-L-GP
PC5201 SC10U25V5KX-L-GP
PC5205 SC10U25V5KX-L-GP
PD5201 AZ4024-01L-R7G-GP
2 20170518
Follow Power team suggest
-SB 20170322
PR5209 0R0805-PAD
PWR_1D0V_BOOT
PWR_1D0V_BOOTA
PWR_1D0V_BOOTA_LX
PC5210 SCD1U25V2KX-L-GP
PWR_1D0V_PH
PL5201 COIL-1UH-57-GP
68.1R010.20G
2nd = 068.1R010.2351
MAG. 7 x 7 x 2.4 mm
DCR: 11.2m~13.5mOhm
Idc : 9 A , Isat : 16A
PWR_1D0V_VDDQ
PWR_1D0V_FB
PG5204 GAP-CLOSE-PWR-6-GP
PC5206 SC22U6D3V3MX-L1-GP
PC5207 SC22U6D3V3MX-L1-GP
PC5209 SC22U6D3V3MX-L1-GP
PC5213 SC22U6D3V3MX-L1-GP
R1
PR5205 3K4R2F-GP
R2
PR5206 10K2R2F-GP
074.05388.0043
Vout= 0.75*(1+R1/R2) = 1.0V
TDC : 3.5A
PWR_1D0V
1D0V_S5
PG5205 GAP-CLOSE-PWR-6-GP
PG5206 GAP-CLOSE-PWR-6-GP
PG5207 GAP-CLOSE-PWR-6-GP
PG5208 GAP-CLOSE-PWR-6-GP
Confidential for Acer CSD Use Only
Count
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G5388K_1D0V
Size A3
Document Number
Woody/Buzz_KBL
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Date: Tuesday, July 25, 2017
Sheet 52 of 106

20160608 -1M

1D8V_S5

PD = (Vin_Vout) x Iout
= (3.3 - 1.8) x 0.3A = 0.45W
PD de-rating(%) = 0.45W/1.33W = 33.8%

1125 Simon
Vendor suggest to replace 74.09025.A3D by 74.09025.D3D

PU5301
G9661-25ADJF11U-GP-U
74.09661.07D

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

# TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

Iomax=120mA

PU5302
S-1339D15-M5001-GP
74.01339.B3F
2nd = 074.09078.0A3F
-SB 20170324

Fix Vout=1D5V
Imax=300mA
OCP = 400mA

Count

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT8068_1D8V
Size: Custom	Document Number: Woody/Buzz_KBL
Rev	
Date: Tuesday, July 25, 2017	Sheet 53 of 106

Blanking

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A4	Woody/Buzz_KBL	-2

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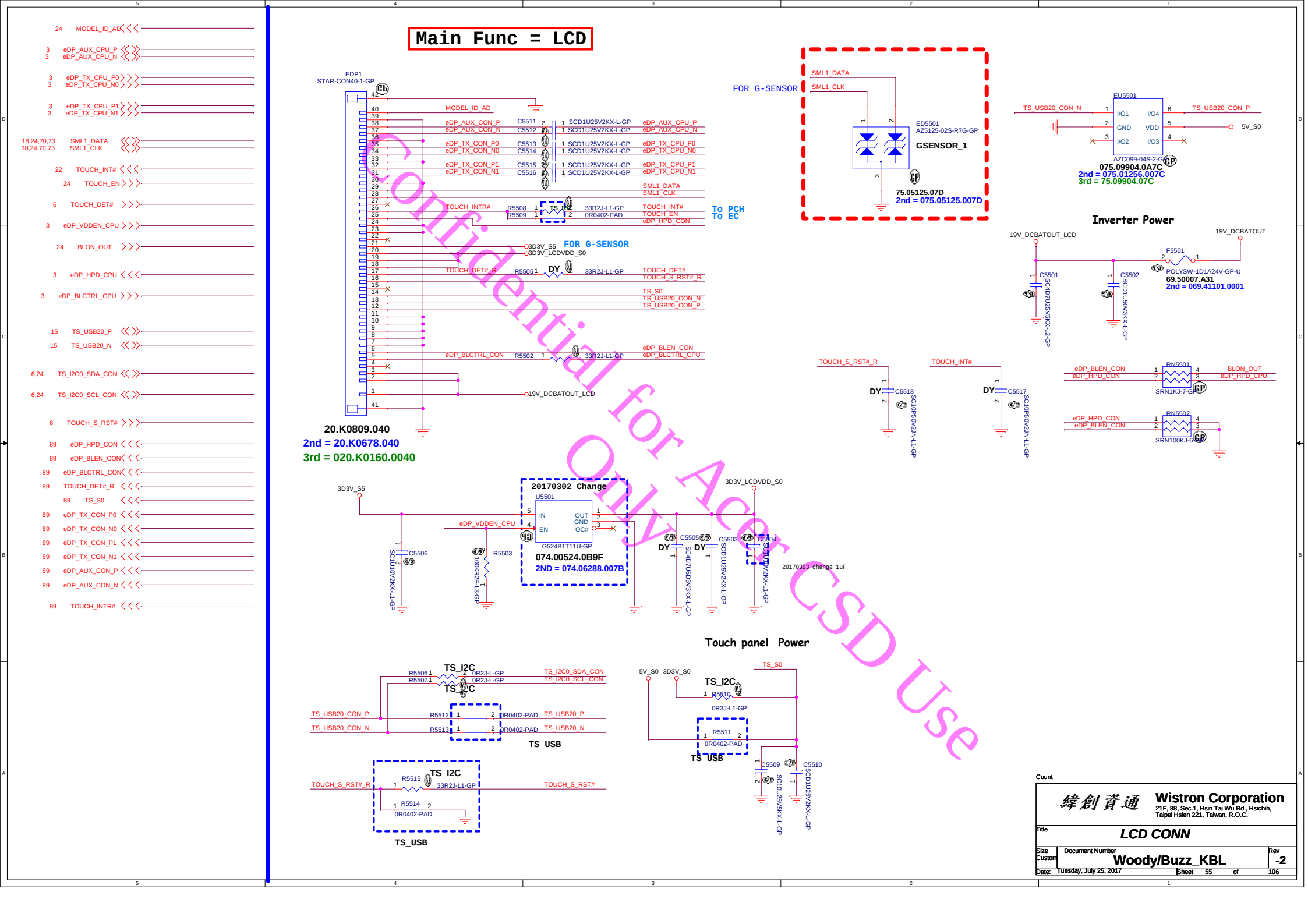
Main Func = LCD



Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size	Document Number	Rev
Custom	Woody/Buzz_KBL	-2

Date: Tuesday, July 25, 2017 Sheet 55 of 106

Blanking

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

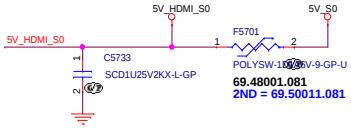
Size	Document Number	Rev
A4	Woody/Buzz_KBL	-2

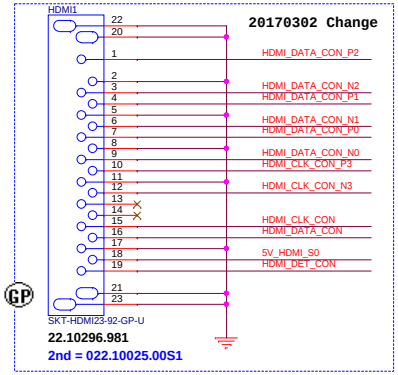
Date: Tuesday, July 25, 2017 Sheet 56 of 106

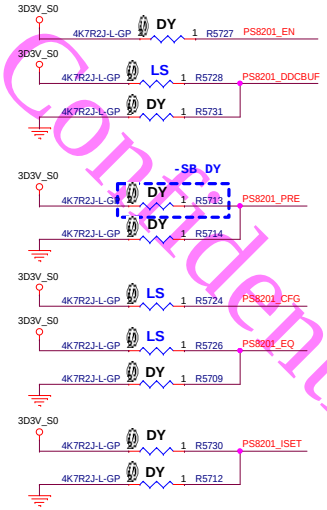
SSID = VIDEO

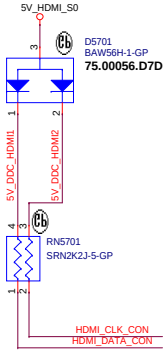
HDMI Level Shifter & CONNECTOR

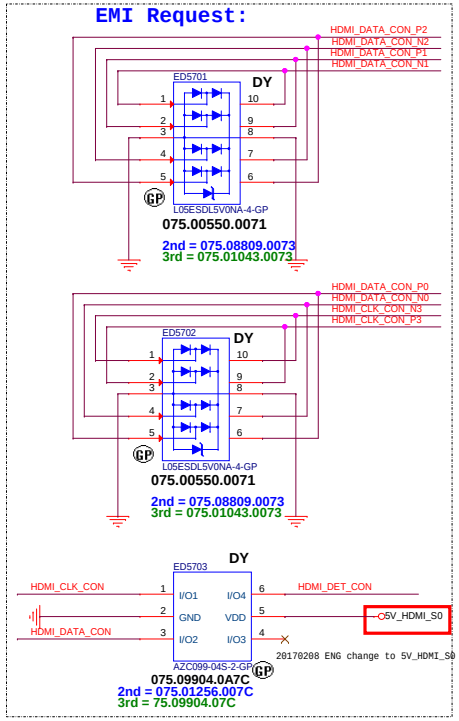
HDMI CONN

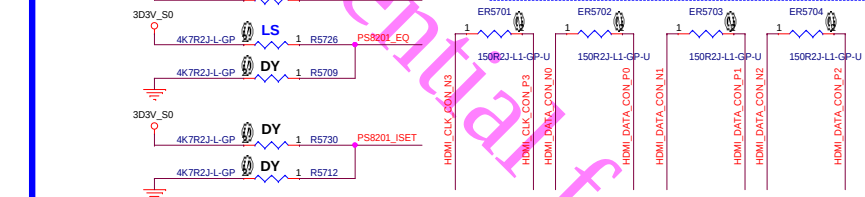


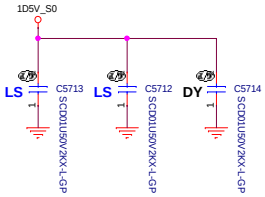


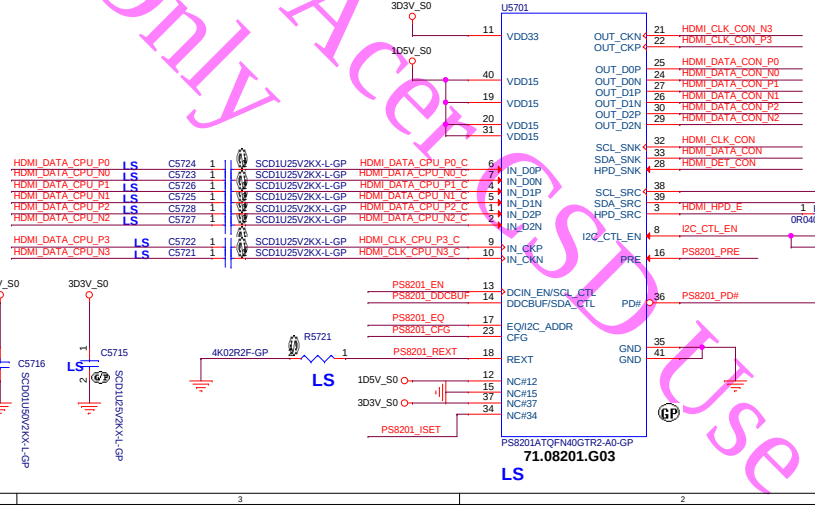


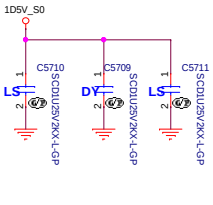












Count			
Wistron Corporation 緯創資通 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: HDMI Level Shifter/Connector			
Size: Custom	Document Number: Woody/Buzz_KBL		Rev: -2
Date: Tuesday, July 25, 2017	Sheet 57 of 106		

Blanking

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A	Woody/Buzz_KBL	-2

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Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DVI(Reserved)***	
Size: A4	Document Number: **Woody/Buzz_KBL**	Rev: **-2**
Date: Tuesday, July 25, 2017	Sheet 59 of 106	

SSID = SATA

SATA HDD Connector

HDD_SATA_RX_P 15
HDD_SATA_RX_N 15
HDD_SATA_TX_N 15
HDD_SATA_TX_P 15
HDD_UNLOAD 69
PM_SLP_S3# 20,24,40,53

5V_S0
C6005 HDD C10U25V5KX-L-GP
C6006 HDD SCD1U25V2KX-L-GP
HDD_UNLOAD
HDD_SATA_RX_C_P
HDD_SATA_RX_C_N
HDD_SATA_TX_C_N
HDD_SATA_TX_C_P
HDD1 HRS-CON12-8-GP HDD

20170210 change

20.K0824.012
2ND = 020.K0125.0012
3RD = 020.K0190.0012

3D3V_S5 R6025 DY 0R2J-L-GP 3D3V_HDD_S0
3D3V_S0 R6026 0R0402-PAD 3D3V_HDD_S0

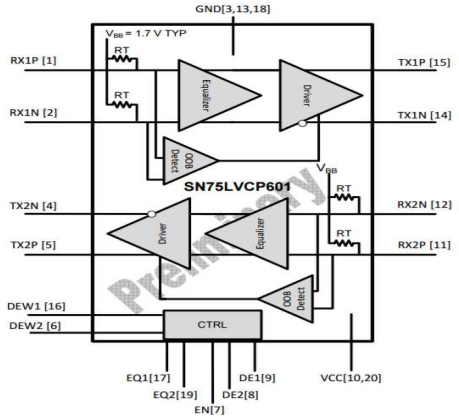
U6001 HDD SN75LVCP601RTJR-GP
71.75601.003

HDD_SATA_TX_P HDD SCD01U50V2KX-L-GP C6018 HDD_SATA_TX_RE_P
HDD_SATA_TX_N HDD SCD01U50V2KX-L-GP C6019 HDD_SATA_TX_RE_N
HDD_SATA_RX_C_P HDD SCD01U50V2KX-L-GP C6020 SATA_RX_REO_P0
HDD_SATA_RX_C_N HDD SCD01U50V2KX-L-GP C6021 SATA_RX_REO_N0
SATA_TX_REO_P0 C60221 SCD01U50V2KX-L-GP HDD HDD_SATA_TX_C_P
SATA_TX_REO_N0 C60231 SCD01U50V2KX-L-GP HDD HDD_SATA_TX_C_N
HDD_SATA_RX_RE_P C60241 SCD01U50V2KX-L-GP HDD HDD_SATA_RX_P
HDD_SATA_RX_RE_N C60251 SCD01U50V2KX-L-GP HDD HDD_SATA_RX_N
EQ1 EQ2 3D3V_HDD_S0
HDD_EN R6033 10KR2J-3-GP HDD
PM_SLP_S3# R6035 0R2J-L-GP DY

EU6001 DY L05ESDL5V0NA-4-GP
HDD_SATA_RX_C_P
HDD_SATA_RX_C_N
HDD_SATA_TX_C_N
HDD_SATA_TX_C_P

075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

3D3V_HDD_S0
R60101 DY 10KR2J-3-GP EQ1 R60161 DY 10KR2J-3-GP
R60111 DY 10KR2J-3-GP EQ2 R60171 DY 10KR2J-3-GP
R60121 DY 10KR2J-3-GP DE1 R60181 DY 10KR2J-3-GP
R60131 DY 10KR2J-3-GP DE2 R60191 DY 10KR2J-3-GP
R60141 DY 10KR2J-3-GP DEW1 R60201 HDD 10KR2J-3-GP
R60151 DY 10KR2J-3-GP DEW2 R60211 HDD 10KR2J-3-GP



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Wistron Corporation
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Title: HDD_GSENSOR

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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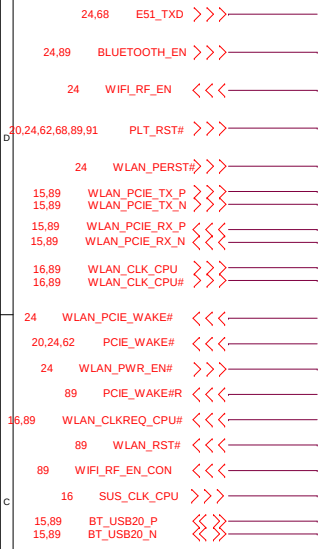
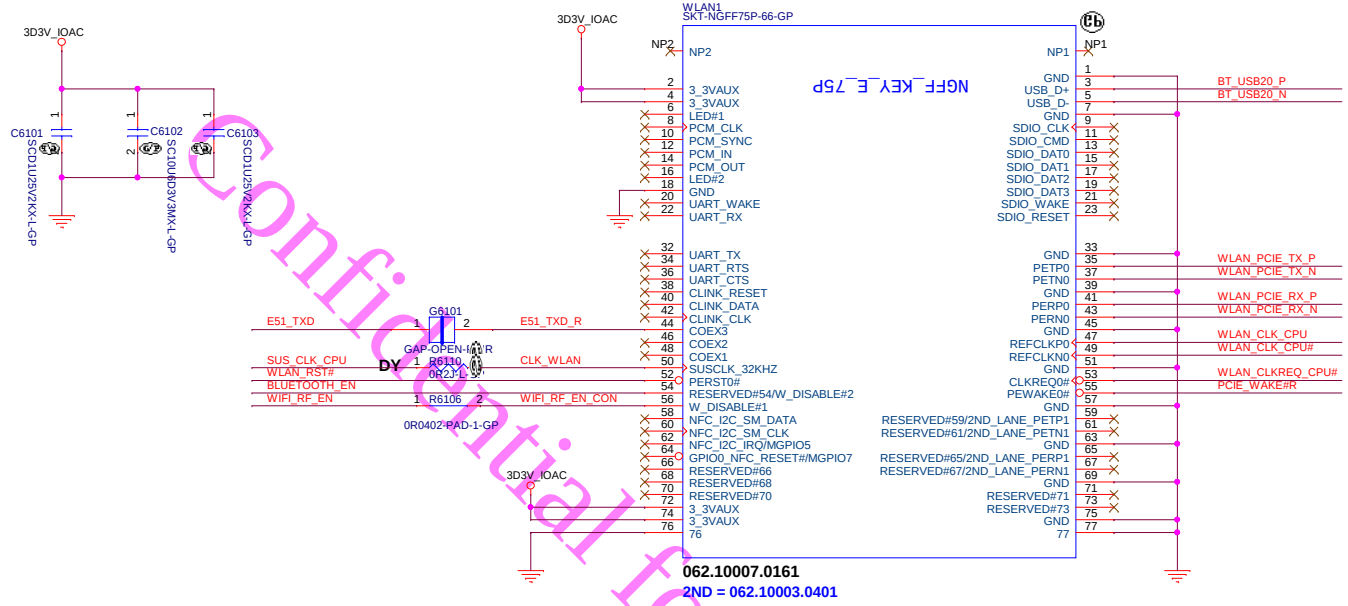
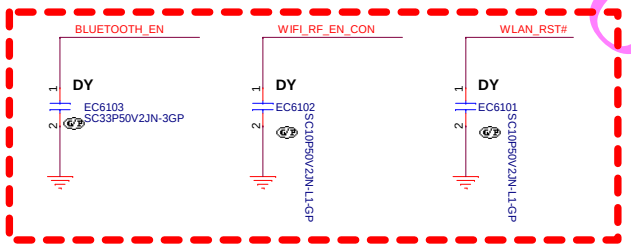
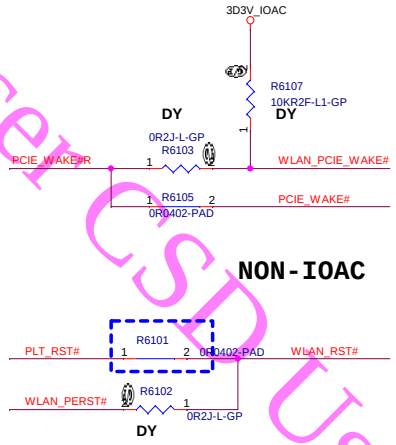
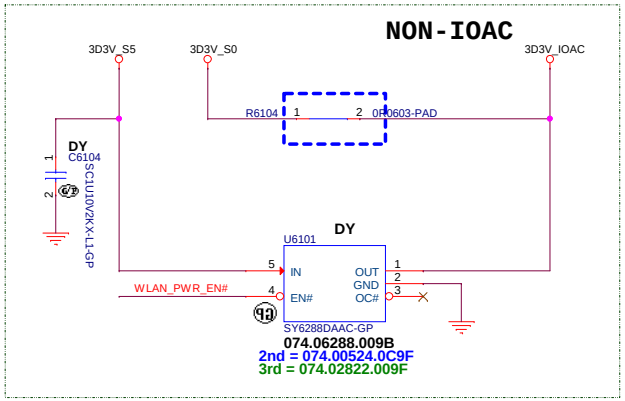
SSID = Wireless Mini Card Connector(802.11a/b/g/n)











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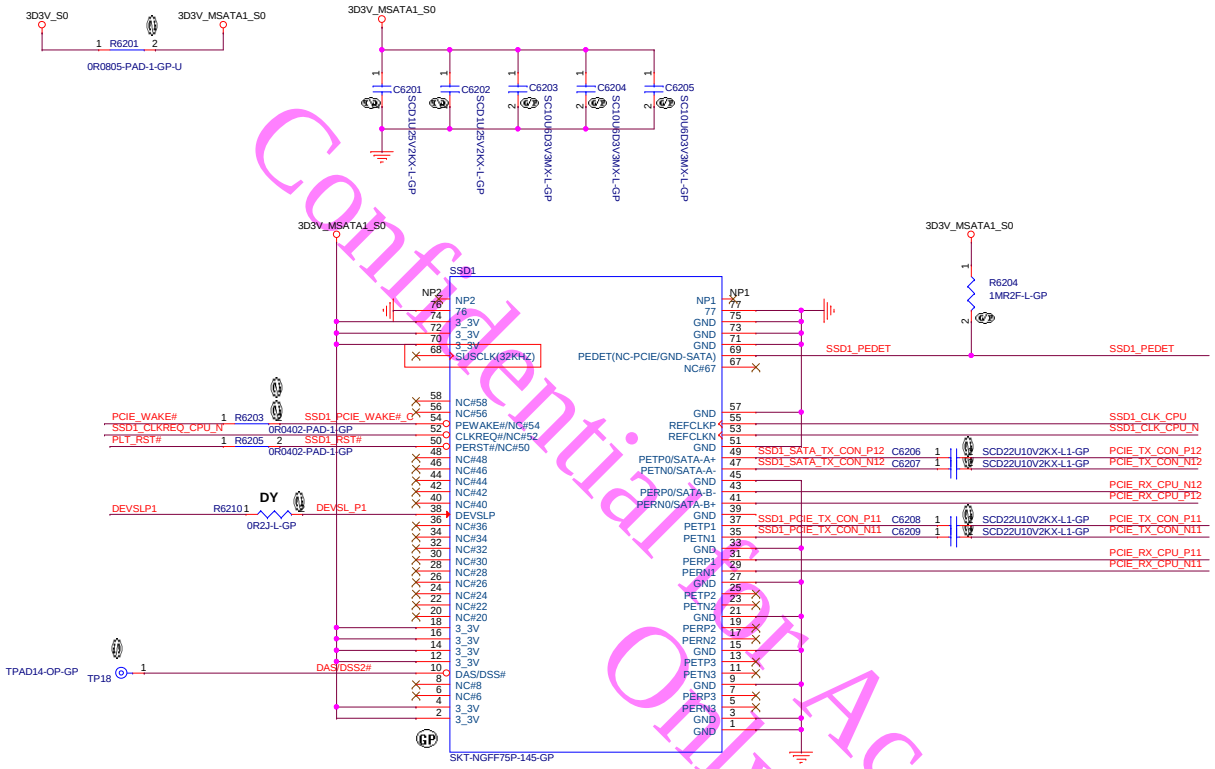
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Mini Card-WLAN		
Size: Custom	Document Number: Woody/Buzz_KBL	Rev: -2
Date: Tuesday, July 25, 2017	Sheet 61 of 106	

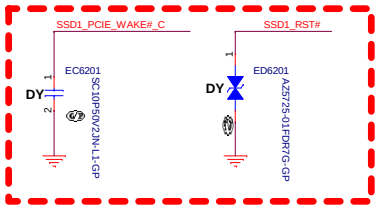
SSID = mSATA

Mini Card Connector(mSATA)



062.10003.0991

2ND = 062.10003.00A1



Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

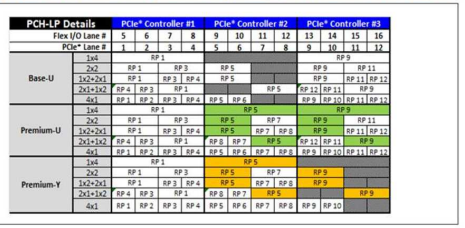


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Count

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Title: mSTATA

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Title: ***Reserved***		
Size: A4	Document Number: **Woody/Buzz_KBL**	Rev: **-2**
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24,89 STDBY_LED
24,89 POWER_LED
24,89 CHARGE_LED
24,89 DC_BATFULL
24 Value+
24 Value-
24 LID_CLOSE#
24 LID_CLOSE2#
15,89 USB3_USB20_N
15,89 USB3_USB20_P
15,89 CR_USB20_N
15,89 CR_USB20_P
43 BAT_RST
24,89 KBC_PWRBTN#
24,35 USB_PWR_EN#
27,64,89 RING2
27,64,89 RING2
27,64,89 SELEEVE
27,64,89 SELEEVE
27,89 AUD_HP1_JACK_R2
27,89 AUD_HP1_JACK_L2
27,89 AUD_HP1_JD#

SSID = User.Interface

Low Active 2A

5V_S5
C6408 SC1U10V2KX-L1-GP
U6401
USB_PWR_EN#
IN
EN#
OUT
GND
OC#
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
5V_USB20
C6409 SCD1U25V2KX-L-GP

Close connector

EU6402
USB3_USB20_N
CR_USB20_N
I/O1
GND
I/O2
I/O4
VDD
I/O3
USB3_USB20_P
5V_USB20
CR_USB20_P
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

20170309 change
PWRBT1
KBC_PWRBTN#
SW-TACT-124-GP
62.40078.001
LAB

5V_AUX_S5
-1 20170424
Del R6401 LED_POWER OPTION(3D3V-AUX_S5)
R6402 1
2 0R0402-PAD
LED_POWER

KBC_PWRBTN#
ED6401
DY
AZ5725-01FDR7G-GP
3D3V_S5
RN6401
Value-
Value+
SRN100KJ-6-GP

Close SMB1

SMB1
STAR-CON40-1-GP
3D3V_S0
RN6427
Value+
Value-
SRN2K2J-5-GP
USB3_USB20_N
USB3_USB20_P
CR_USB20_N
CR_USB20_P
Value+_R
Value-_R
BAT_RST
KBC_PWRBTN#
LID_CLOSE#
LID_CLOSE2#
5V_USB20
RING2
RING2
SELEEVE
SELEEVE
AUD_HP1_JACK_R2
AUD_HP1_JACK_L2
AUD_HP1_JD#
3D3V_AUX_S5
5V_S5
STDBY_LED
POWER_LED
DC_BATFULL
LED_POWER
CHARGE_LED
PIN1,PIN5 SWAP
-SB 20170324
AUD_AGND
20.K0809.040
2ND = 20.K0678.040
3rd = 020.K0160.0040

Count

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Title: LED Bard/Power Button

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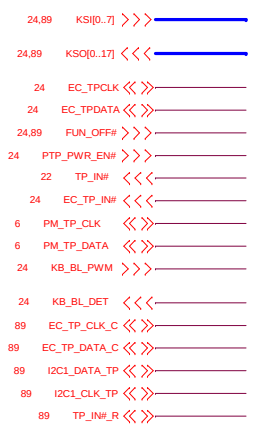
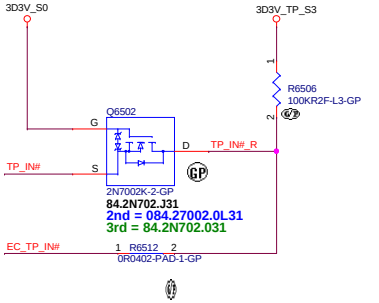
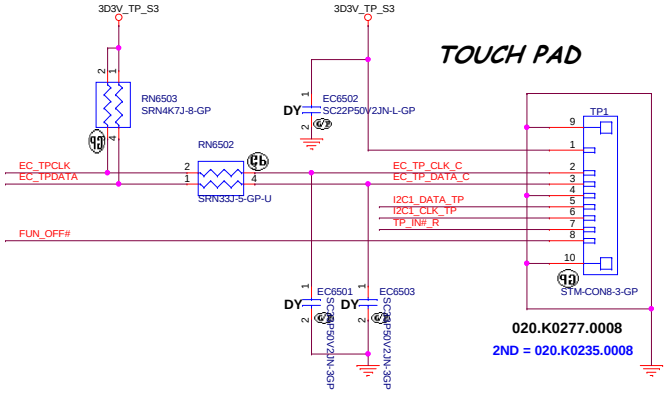
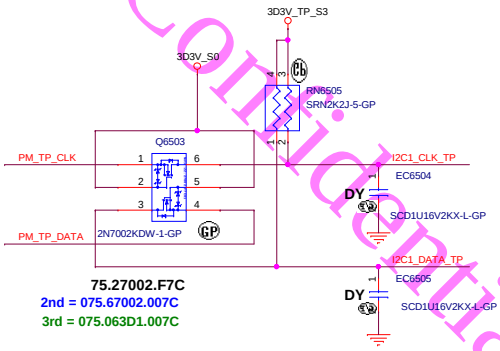
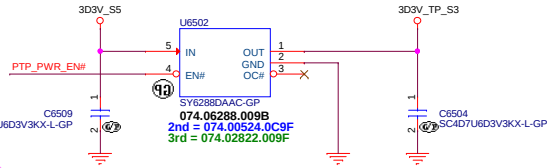
SSID = KBC

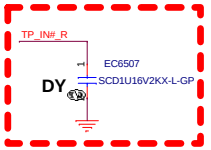




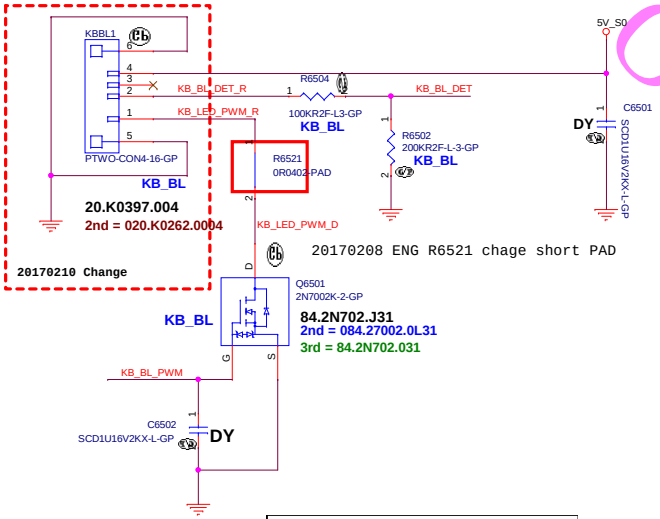


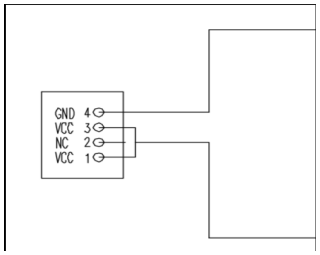


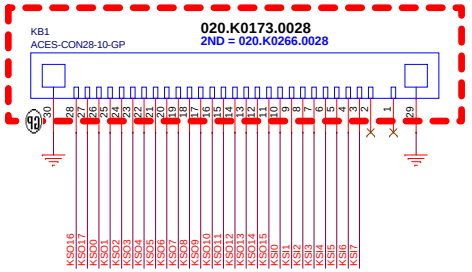


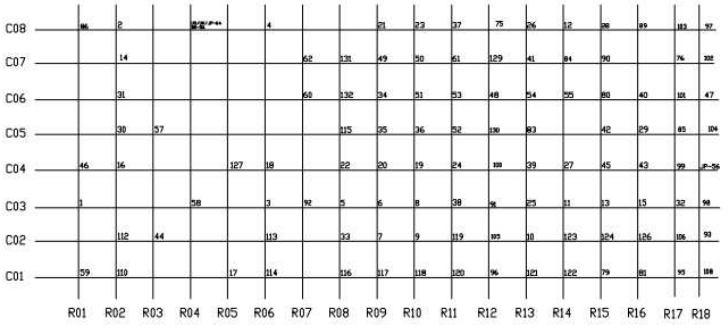


Internal KeyBoard Connector









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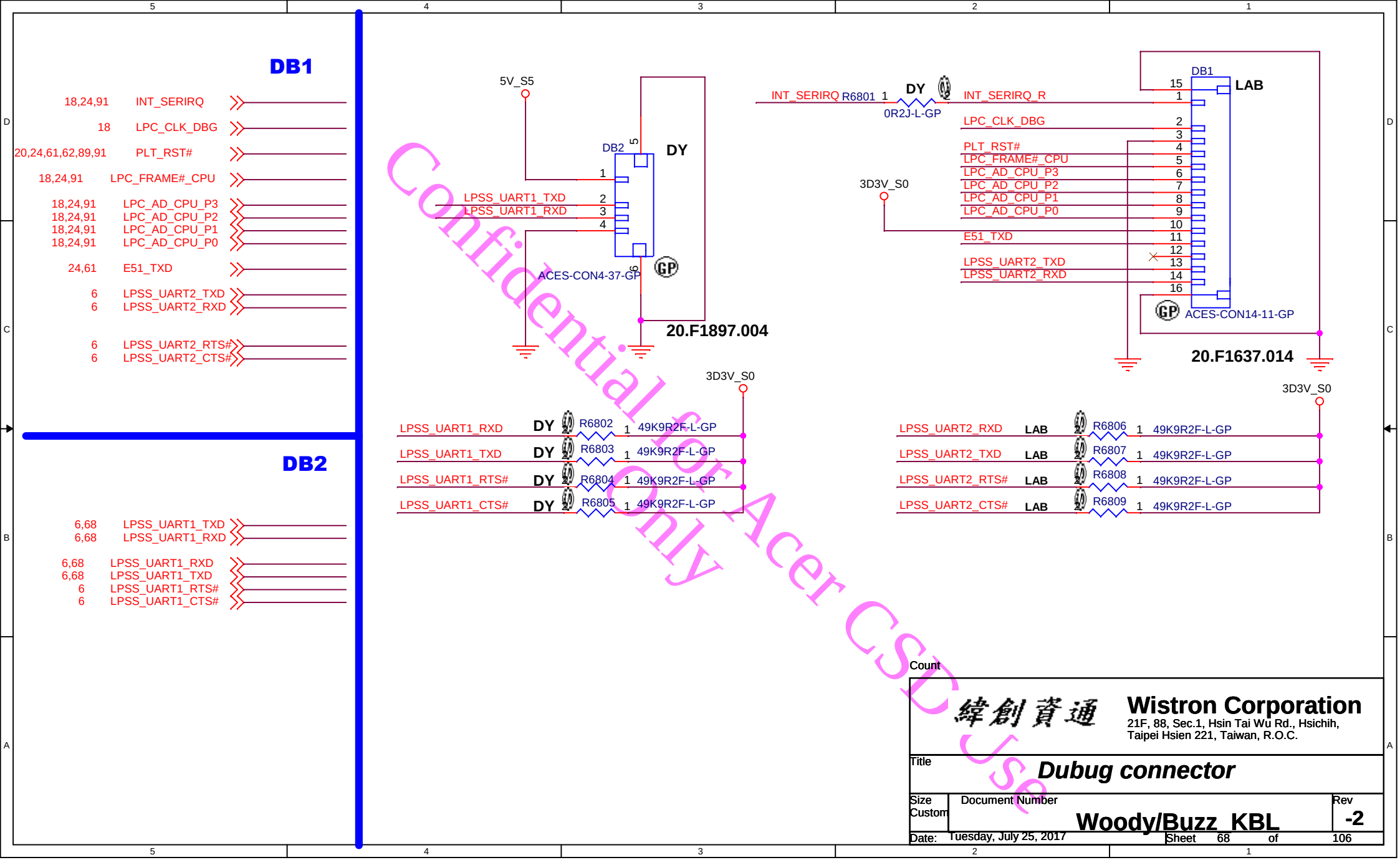
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18,24,91 INT_SERIRQ
18 LPC_CLK_DBG
20,24,61,62,89,91 PLT_RST#
18,24,91 LPC_FRAME#_CPU
18,24,91 LPC_AD_CPU_P3
18,24,91 LPC_AD_CPU_P2
18,24,91 LPC_AD_CPU_P1
18,24,91 LPC_AD_CPU_P0
24,61 E51_TXD
6 LPSS_UART2_TXD
6 LPSS_UART2_RXD
6 LPSS_UART2_RTS#
6 LPSS_UART2_CTS#
DB2
6,68 LPSS_UART1_TXD
6,68 LPSS_UART1_RXD
6,68 LPSS_UART1_RXD
6,68 LPSS_UART1_TXD
6 LPSS_UART1_RTS#
6 LPSS_UART1_CTS#
5V_S5
DB2
DY
LPSS_UART1_TXD
LPSS_UART1_RXD
ACES-CON4-37-GP
GP
20.F1897.004
3D3V_S0
LPSS_UART1_RXD DY R6802 1 49K9R2F-L-GP
LPSS_UART1_TXD DY R6803 1 49K9R2F-L-GP
LPSS_UART1_RTS# DY R6804 1 49K9R2F-L-GP
LPSS_UART1_CTS# DY R6805 1 49K9R2F-L-GP
INT_SERIRQ R6801 1 DY 2 0R2J-L-GP INT_SERIRQ_R
DB1
LAB
LPC_CLK_DBG
PLT_RST#
LPC_FRAME#_CPU
LPC_AD_CPU_P3
LPC_AD_CPU_P2
LPC_AD_CPU_P1
LPC_AD_CPU_P0
3D3V_S0
E51_TXD
LPSS_UART2_TXD
LPSS_UART2_RXD
GP
ACES-CON14-11-GP
20.F1637.014
3D3V_S0
LPSS_UART2_RXD LAB R6806 1 49K9R2F-L-GP
LPSS_UART2_TXD LAB R6807 1 49K9R2F-L-GP
LPSS_UART2_RTS# LAB R6808 1 49K9R2F-L-GP
LPSS_UART2_CTS# LAB R6809 1 49K9R2F-L-GP
Confidential for Acer CSD Use Only
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Title
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-2
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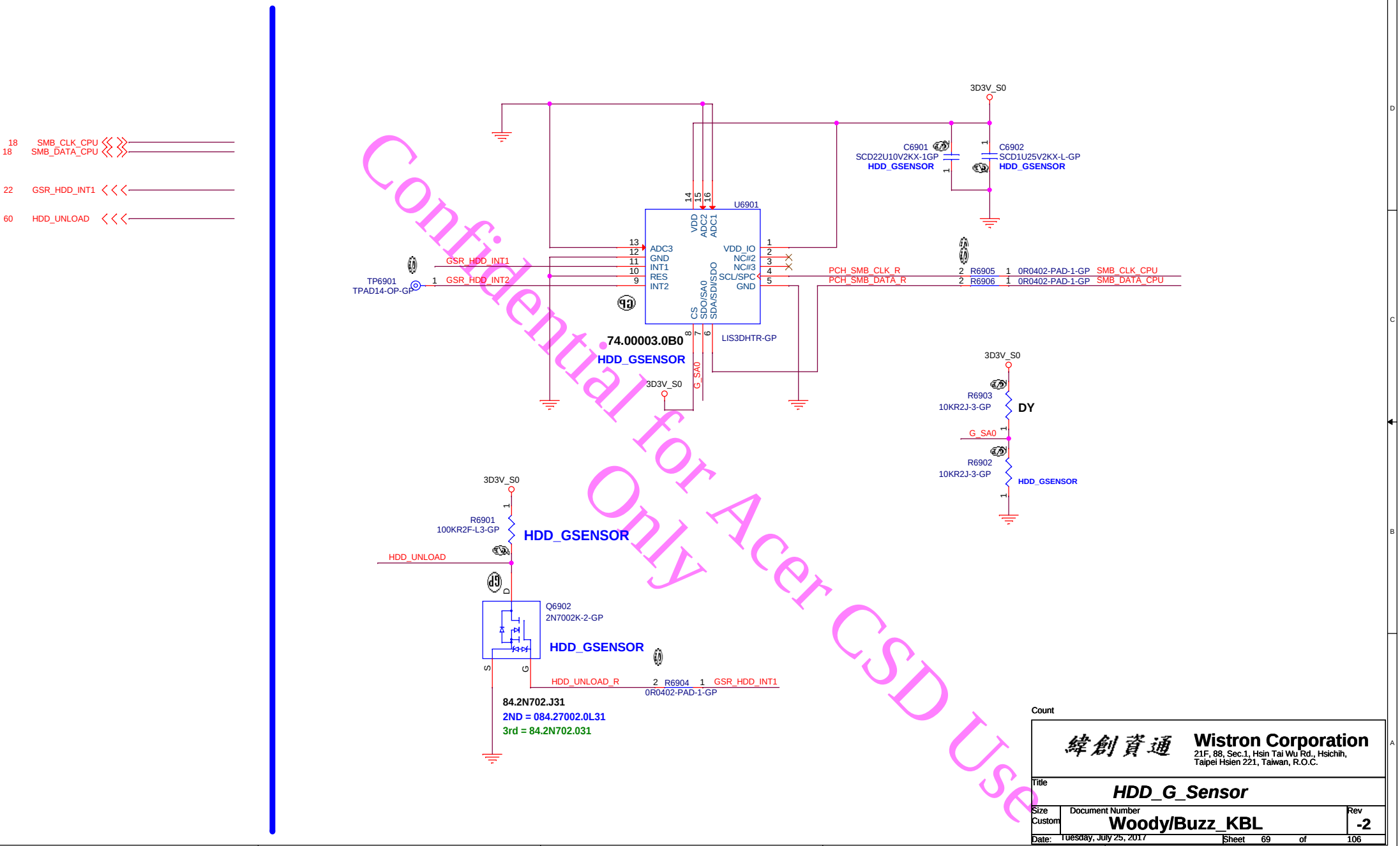

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Title	HDD_G_Sensor
Size: Custom	Document Number: Woody/Buzz_KBL
Rev	-2
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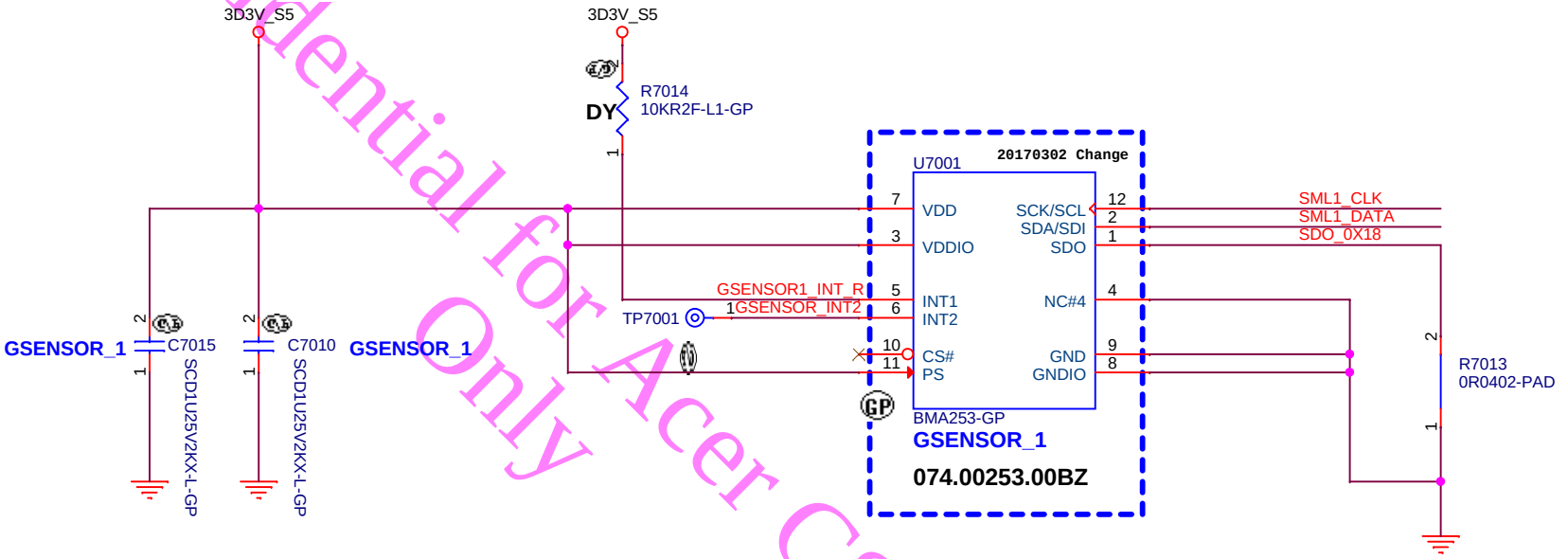
18,24,55,73 SML1_CLK
18,24,55,73 SML1_DATA

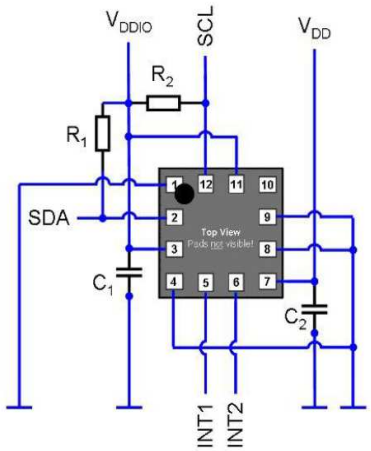
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SSID = User.Interface

G Sensor

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.





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Title: ***G SENSOR***

Size	Document Number	Rev
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Title: ***Reserved***

Size	Document Number	Rev
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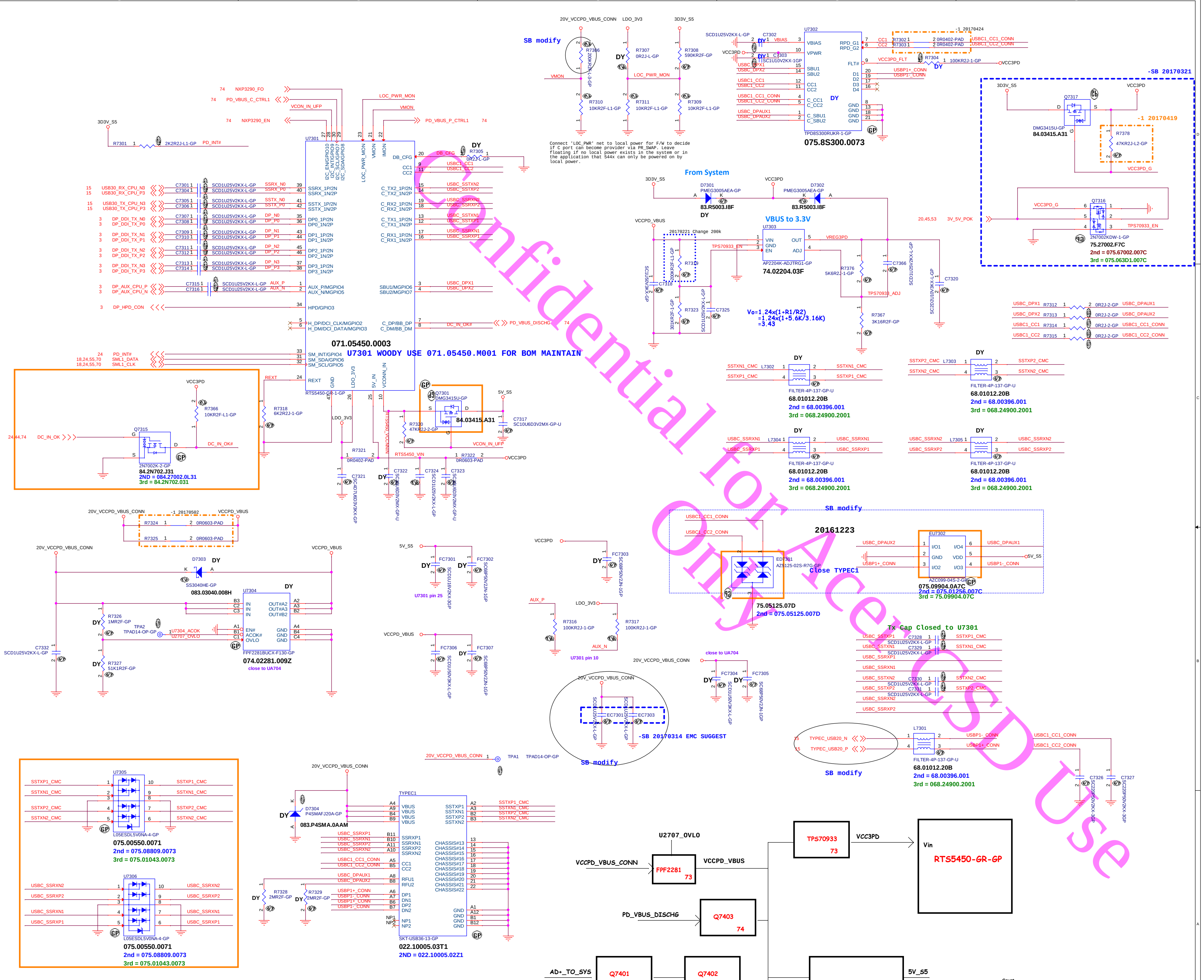

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Size: Custom	Document Number: Woody/Buzz_KBL
Rev	-2
Date	Tuesday, July 25, 2017
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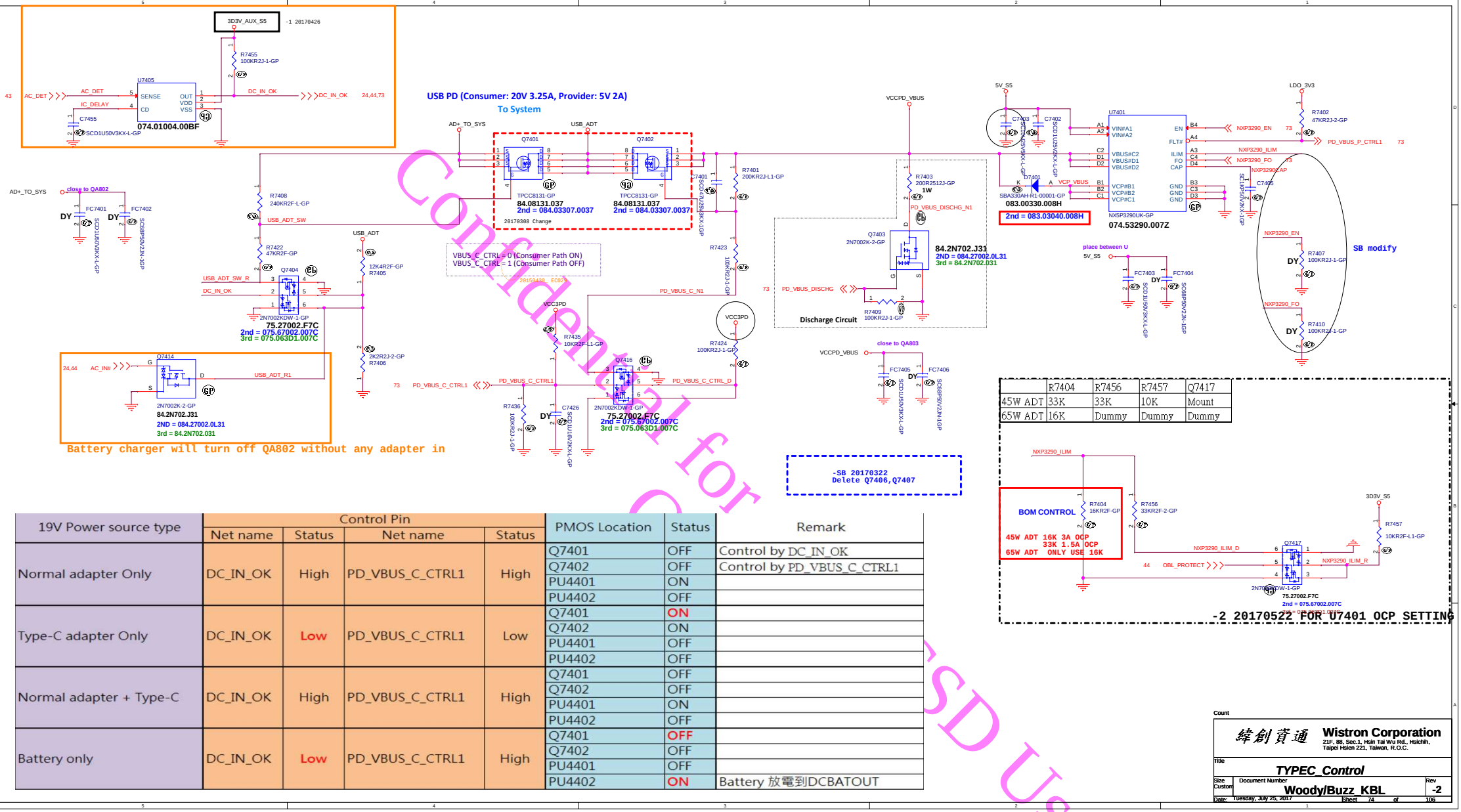

	R7404	R7456	R7457	Q7417
45W ADT	33K	33K	10K	Mount
65W ADT	16K	Dummy	Dummy	Dummy

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	
					Q7402	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT

Count

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Title: TYPEC_Control

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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Count

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **Woody/Buzz KBL**	Rev: **-2**
Date: Tuesday, July 25, 2017	Sheet 75 of 106	

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU_PEG(Reserved)*

Size | Project Name: **Woody/Buzz_KBL** | Rev: *-2*

Date: Tuesday, July 25, 2017 | Sheet 76 of 106

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Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *GPU_DIGITALOUT(Reserved)*		
Size: A4	Document Number: **Woody/Buzz_KBL**	Rev: **-2**
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Title	***Reserved***
Size	Project Name: **Woody/Buzz_KBL** — Rev: *-2*
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Title: ***GPU_GPIO/STRAP(Reserved)***

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Title	*GPU-VRAM3,4(Reserved)*	
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Title	*GPU-VRAM5,6(Reserved)*	
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Title: *GPU-VRAM7,8(Reserved)*		
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Title	*VGA_CORE(Reserved)*	
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Title: ***DIS VGA POWER(Reserved)***

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Title: *GFX_LCD(1/2)(Reserved)*

Size	Document Number	Rev
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Title: *GFX_LCD(2/2)(Reserved)*		
Size: A4	Document Number: **Woody/Buzz_KBL**	Rev: **-2**
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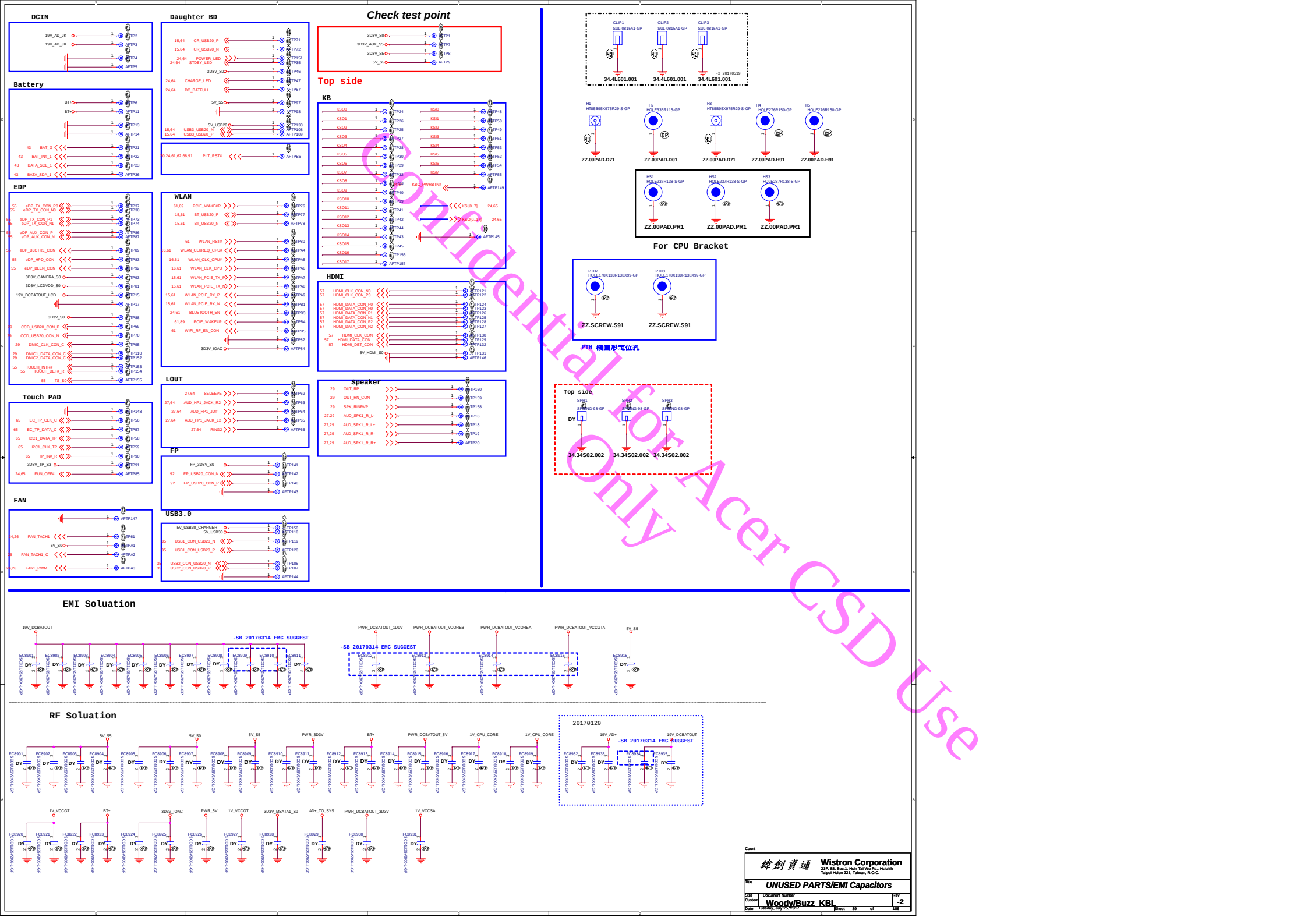
DCIN
Daughter BD
Check test point
Top side
Battery
KB
EDP
WLAN
HDMI
Touch PAD
LOUT
Speaker
FP
FAN
USB3.0
CLIP1 SUL-0815A1-GP
CLIP2 SUL-0815A1-GP
CLIP3 SUL-0815A1-GP
34.4L601.001
34.4L601.001
34.4L601.001
H1 HT85B95X975R29-S-GP
H2 HOLE335R115-GP
H3 HT85B95X975R29-S-GP
H4 HOLE276R150-GP
H5 HOLE276R150-GP
ZZ.00PAD.D71
ZZ.00PAD.D01
ZZ.00PAD.D71
ZZ.00PAD.H91
ZZ.00PAD.H91
HS1 HOLE237R138-S-GP
HS2 HOLE237R138-S-GP
HS3 HOLE237R138-S-GP
ZZ.00PAD.PR1
ZZ.00PAD.PR1
ZZ.00PAD.PR1
For CPU Bracket
PTH2 HOLE170X130R138X99-GP
PTH3 HOLE170X130R138X99-GP
ZZ.SCREW.S91
ZZ.SCREW.S91
PTH 橢圓形定位孔
Top side
34.34S02.002
34.34S02.002
34.34S02.002
EMI Soluation
-SB 20170314 EMC SUGGEST
-SB 20170314 EMC SUGGEST
RF Soluation
20170120
-SB 20170314 EMC SUGGEST
Confidential for Acer CSD Use Only
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UNUSED PARTS/EMI Capacitors
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Title: *NFC(Reserved)*		
Size: A4	Document Number: Woody/Buzz_KBL	Rev: -2
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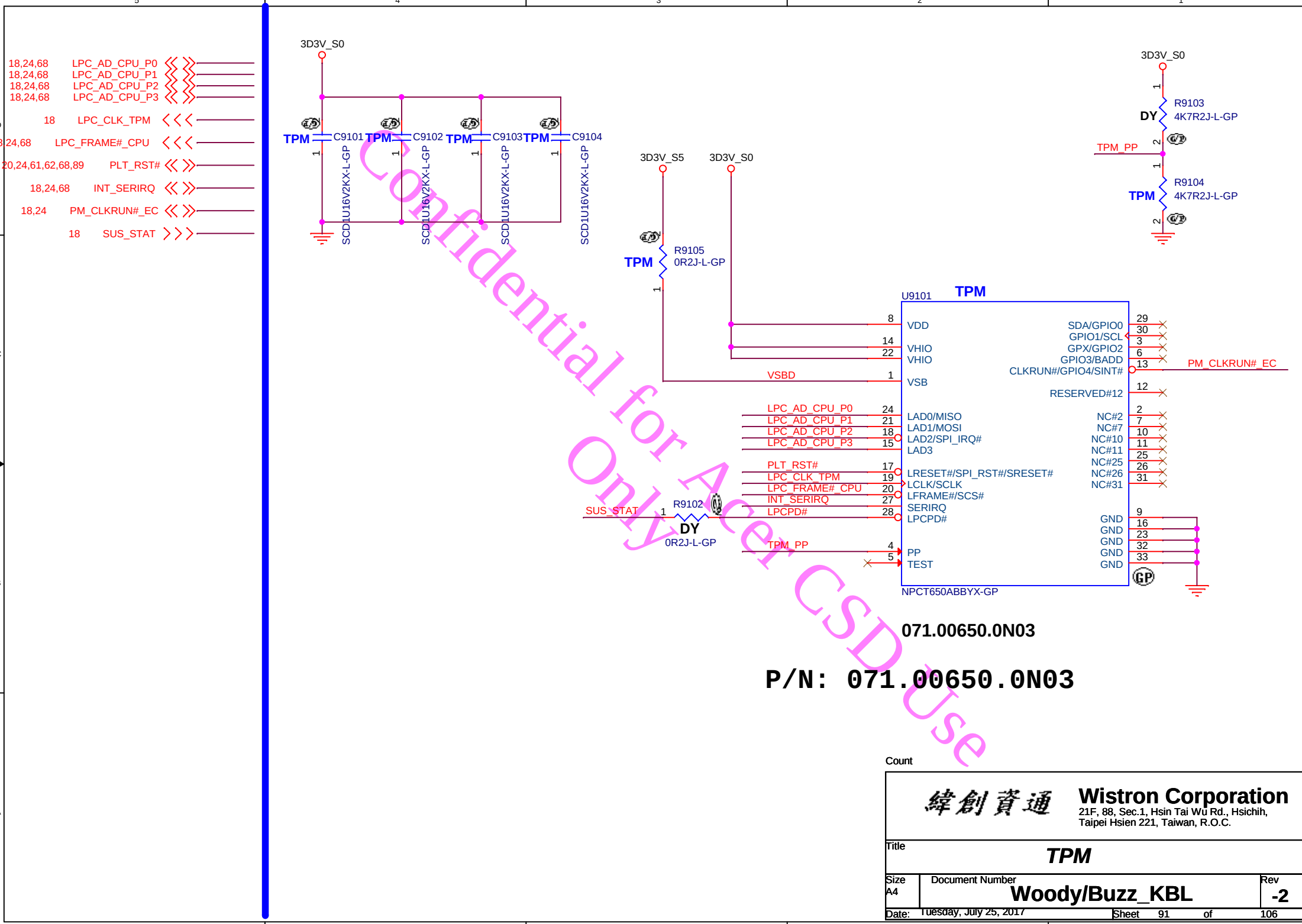

15 FP_USB20_N

15 FP_USB20_P

89 FP_USB20_CON_N

89 FP_USB20_CON_P

3D3V_S0 — R9201 1 2 0R0603-PAD — FP_3D3V_S0

FP_3D3V_S0

20170329 change

FP_USB20_CON_P

FP_USB20_CON_N

FP1

10 8 7 6 5 4 3 2 1 9

FP

PTWO-CON8-17-GP

020.K0312.0008

2nd = 20.K0481.008

FP

EU9201

FP_USB20_CON_P 1 I/O1 I/O4 6 FP_USB20_CON_N

2 GND VDD 5 5V_S0

3 I/O2 I/O3 4

AZC099-04S-2-GP

075.09904.0A7C

2nd = 075.01256.007C

3rd = 75.09904.07C

FP_USB20_P R9202 1 2 0R0402-PAD FP_USB20_CON_P

FP_USB20_N R9203 1 2 0R0402-PAD FP_USB20_CON_N

Count

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Title: ***Finger Print***

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Title	*Express_Card(Reserved)*	
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Title	*Smart Card scoket(Reserved)*	
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Title	*GFX eDP(Reserved)*	
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Title: ***Bottom Docking(Reserved)***

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Title	*Inter LAN WG1217LM(Reservrd)*	
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Title	*CPU_CFG STRAP(Reserved)*	
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Title: *CPU_XDP(Reserved)*		
Size: A4	Document Number: **Woody/Buzz_KBL**	Rev: **-2**
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Title	*table of content*	
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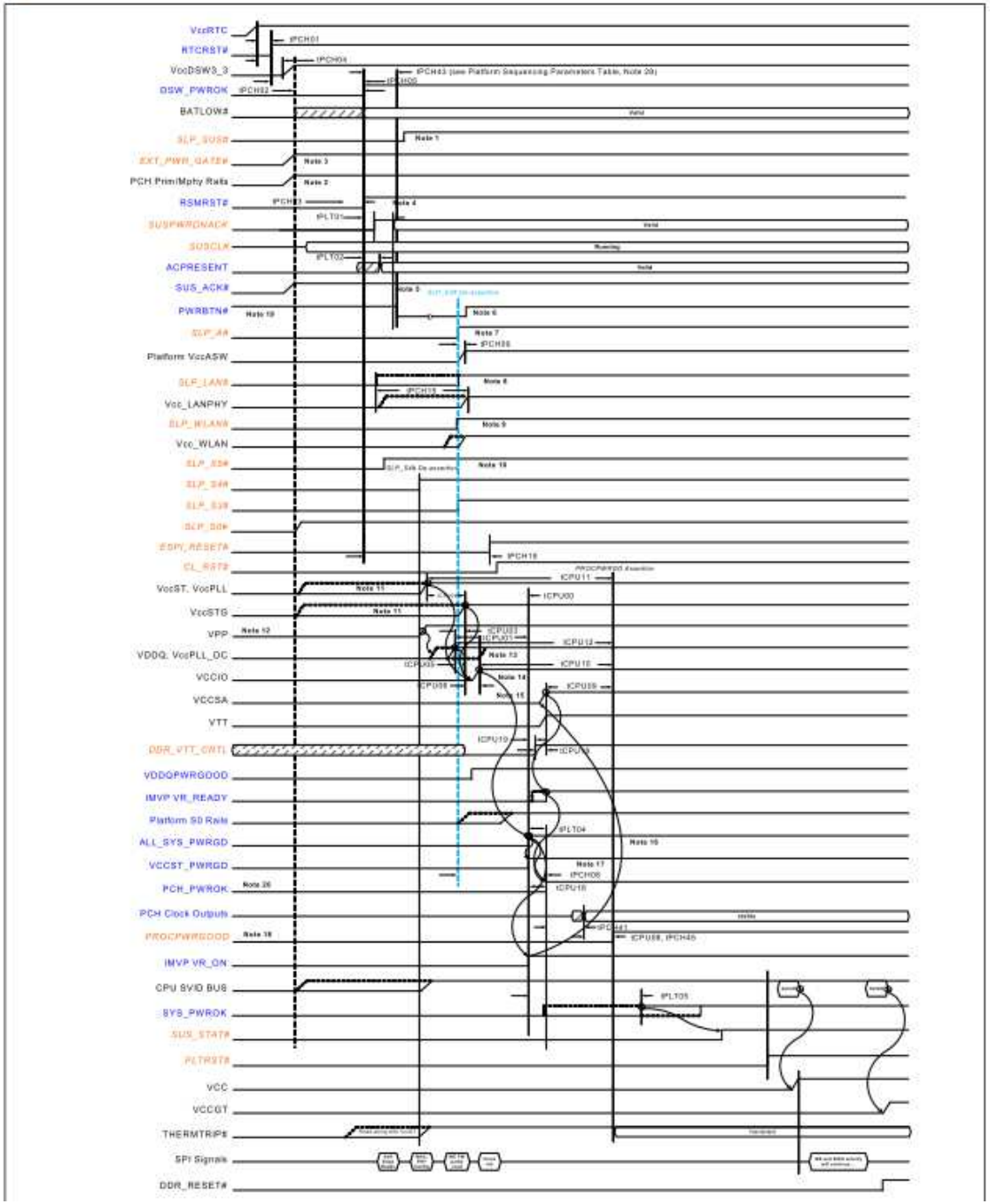
Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Change History***
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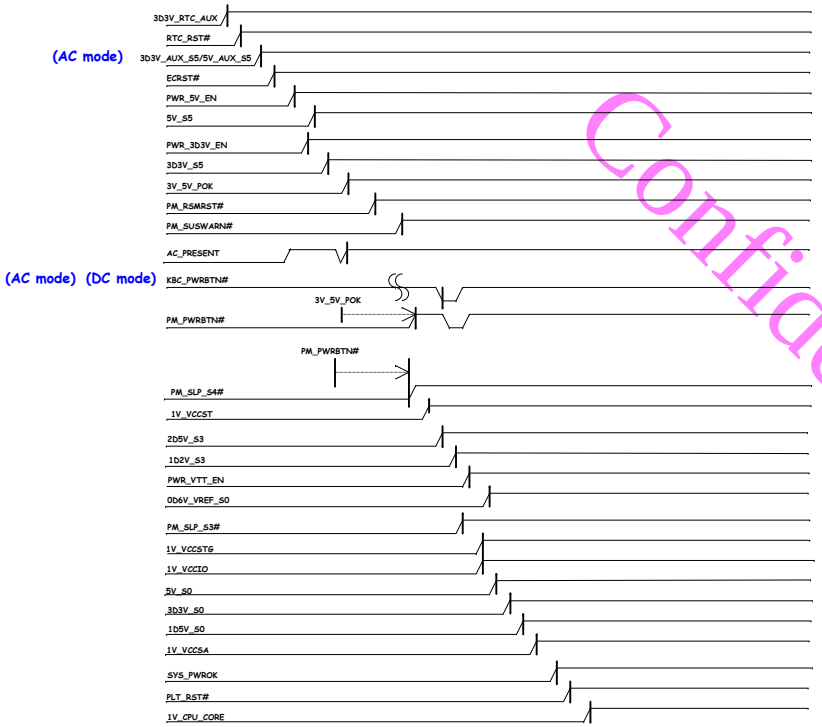
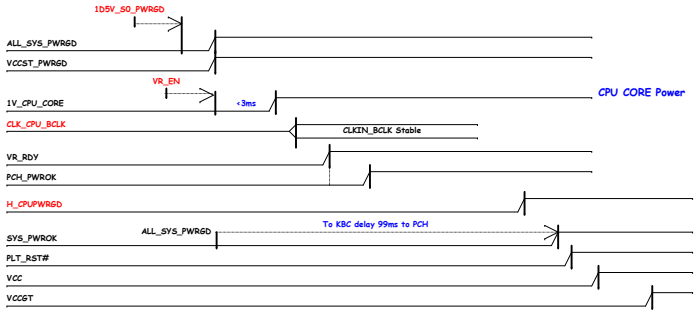
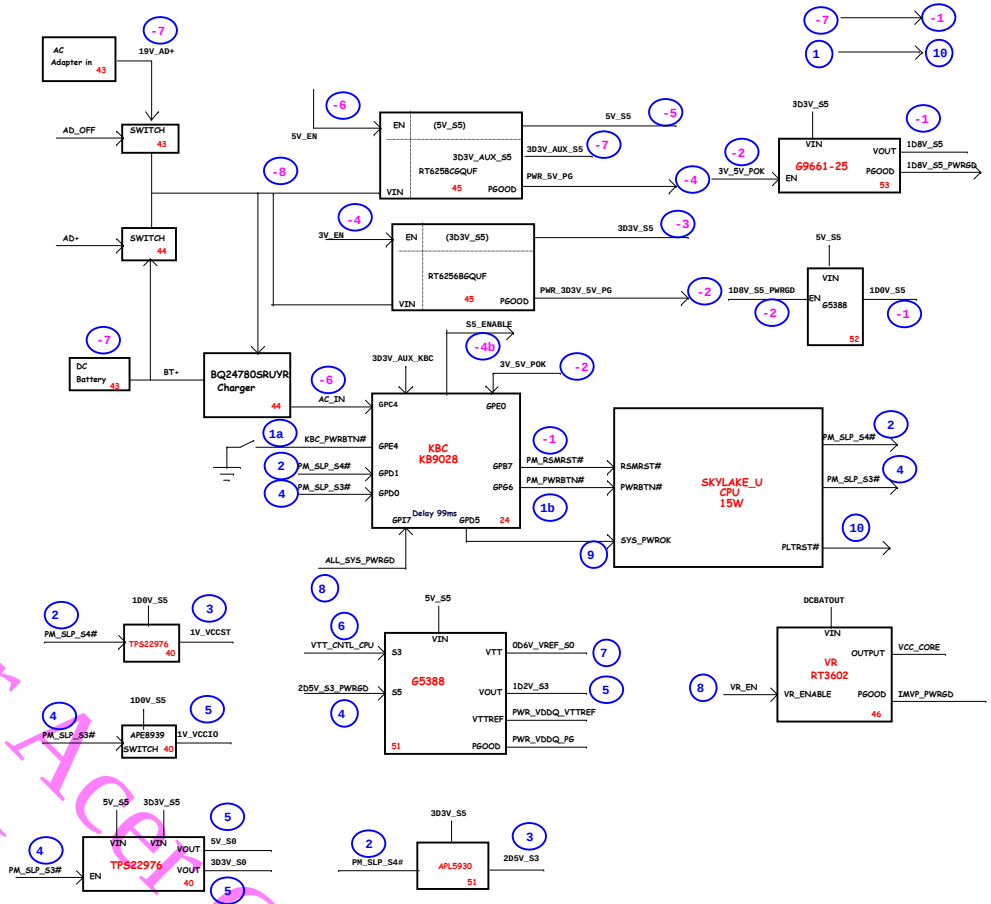
Intel-Power Up Sequence







Wistron Corporation			
Power Sequence			
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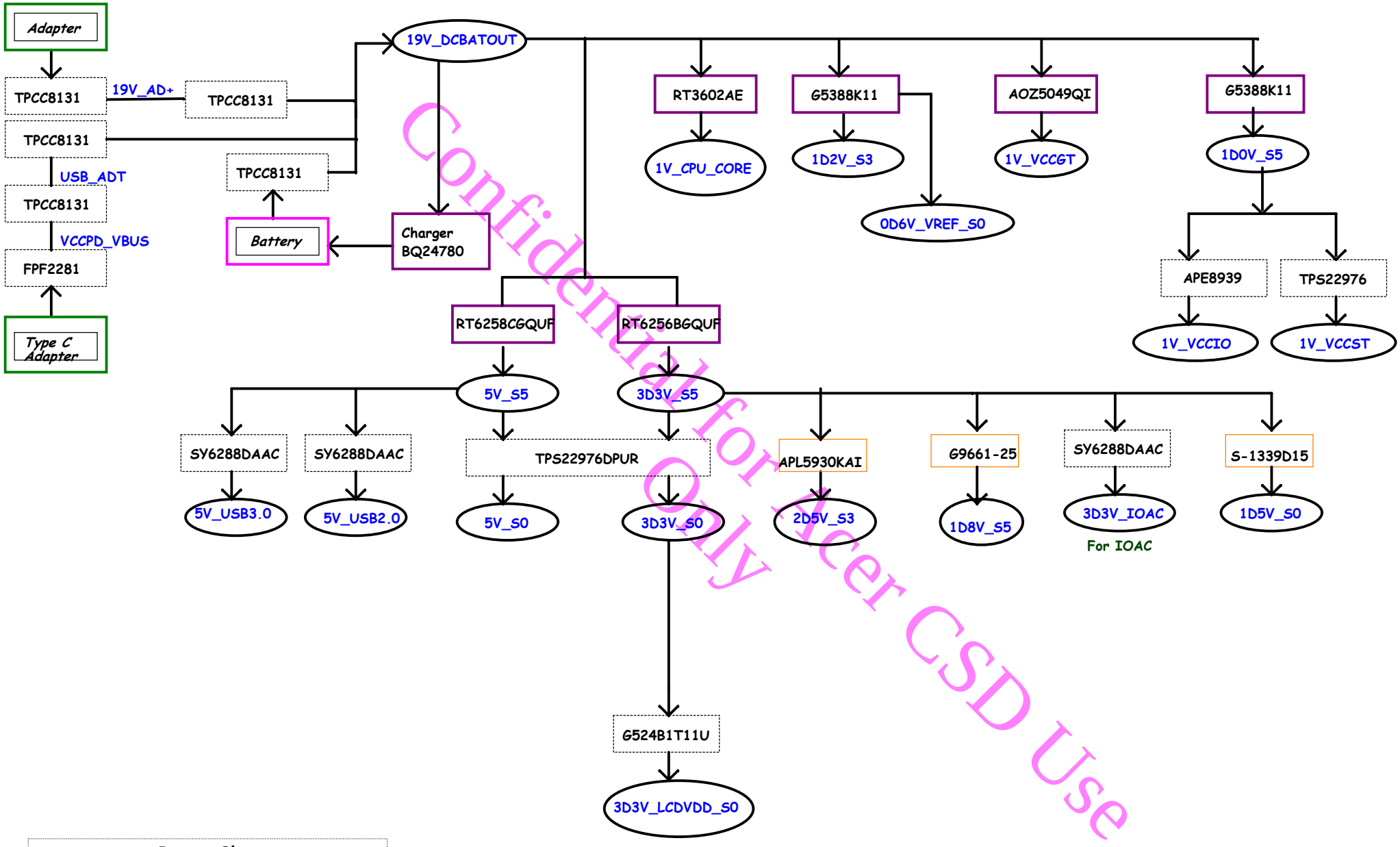

Power Shape

Regulator	LDO	Switch

Count

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Title: Power Block Diagram

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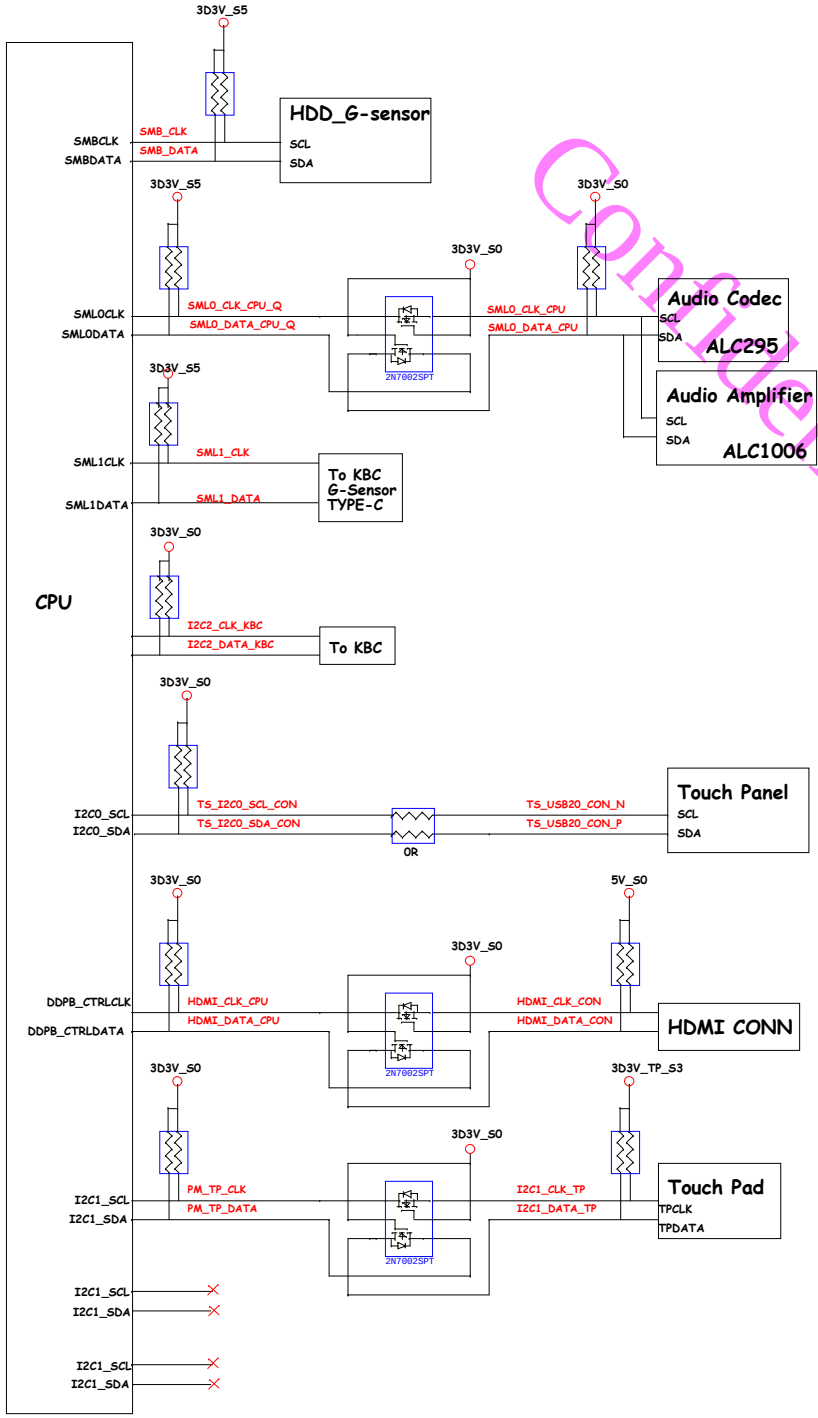
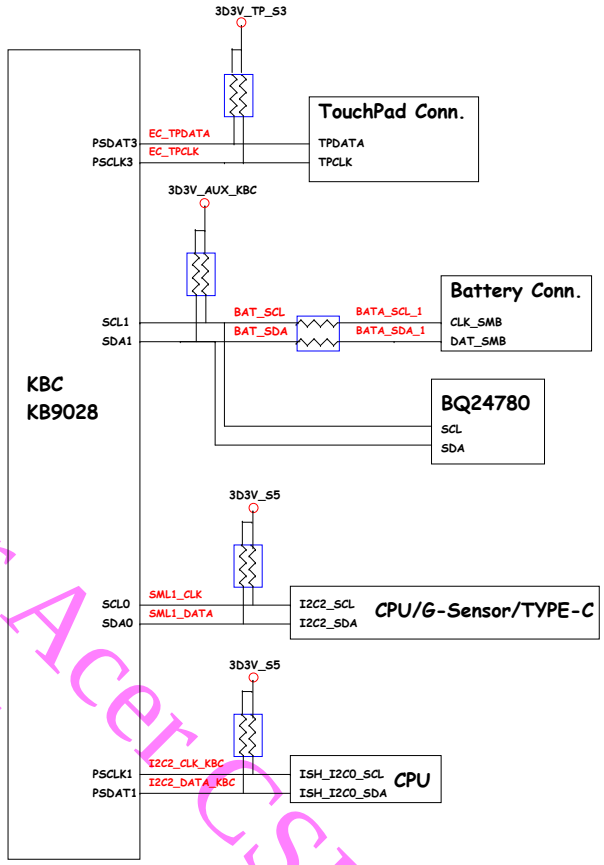
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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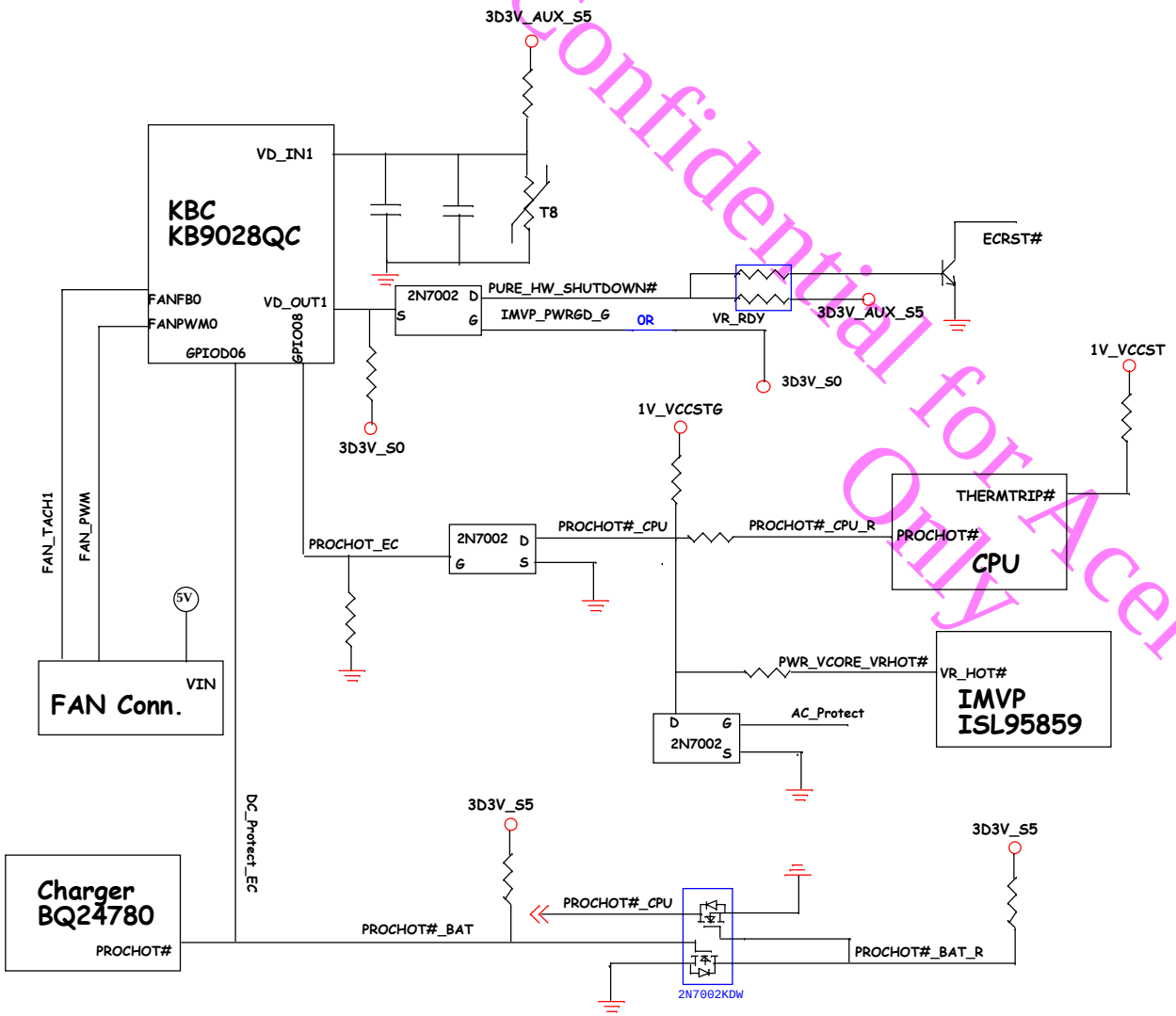
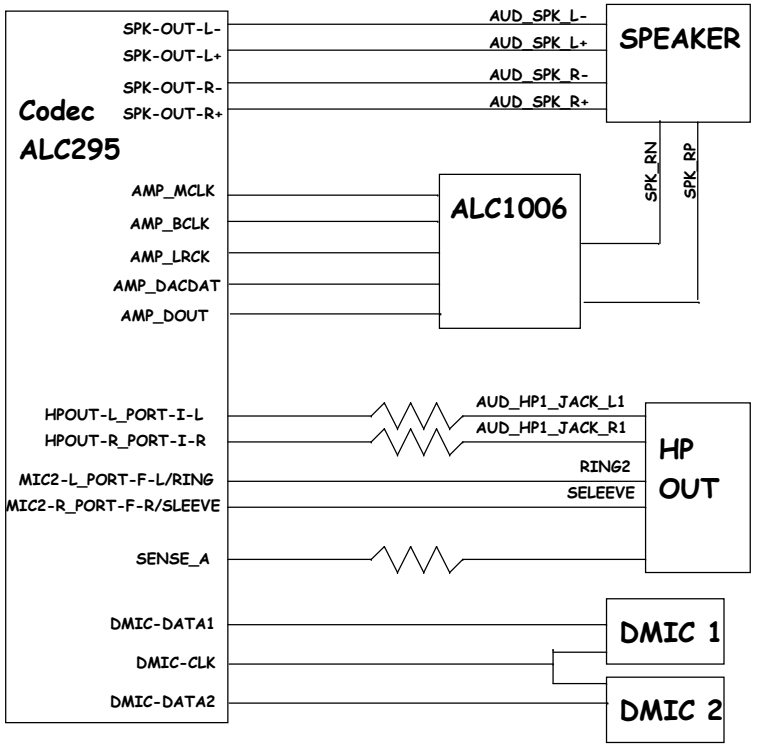
Thermal Block Diagram



Audio Block Diagram



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Title: **THERMAL/AUDIO BLOCK DIAGRAM**

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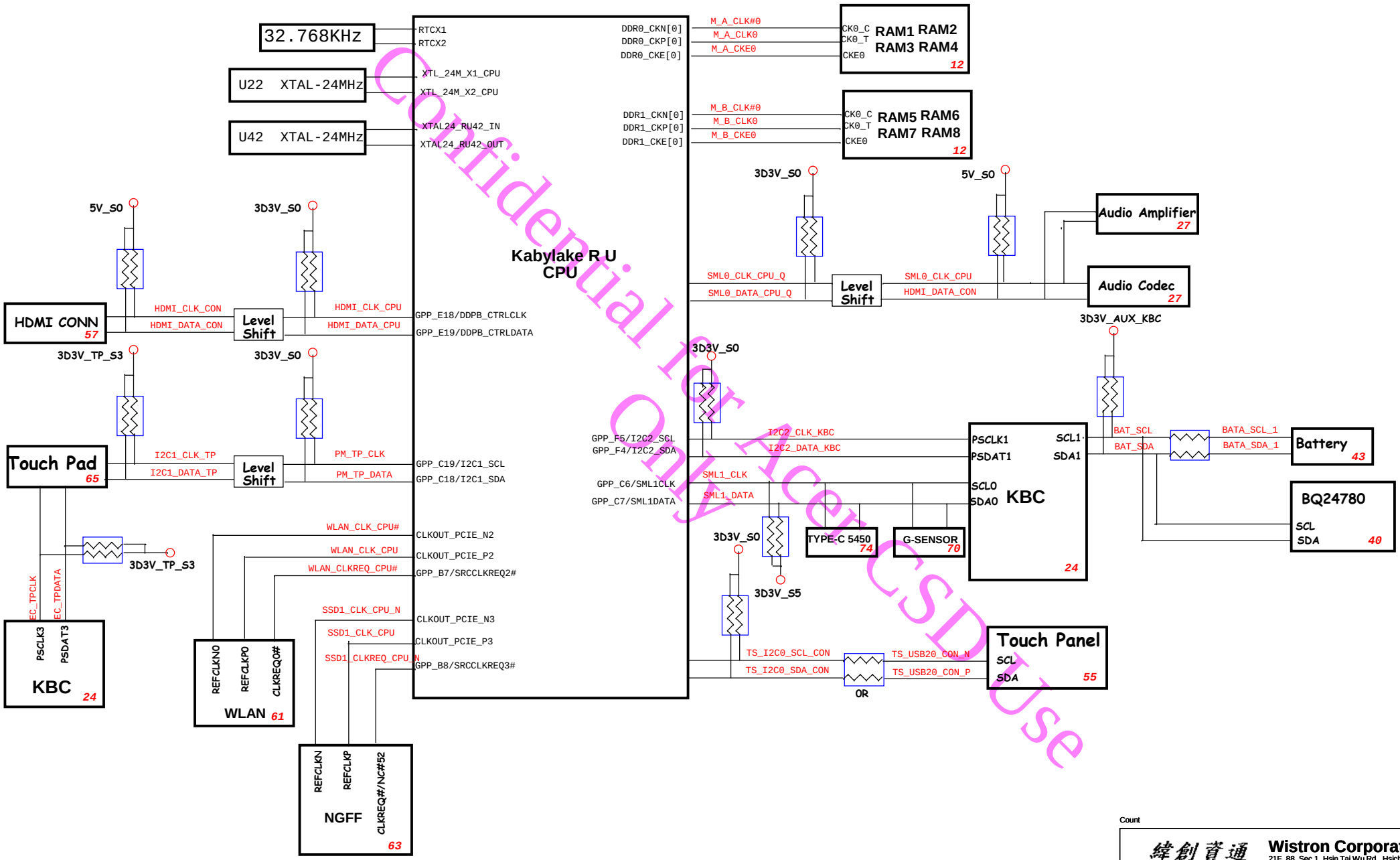
CLOCK BLOCK DIAGRAM



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Title: CLK Block

Size: Custom | Document Number: Woody/Buzz_KBL | Rev: -2

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