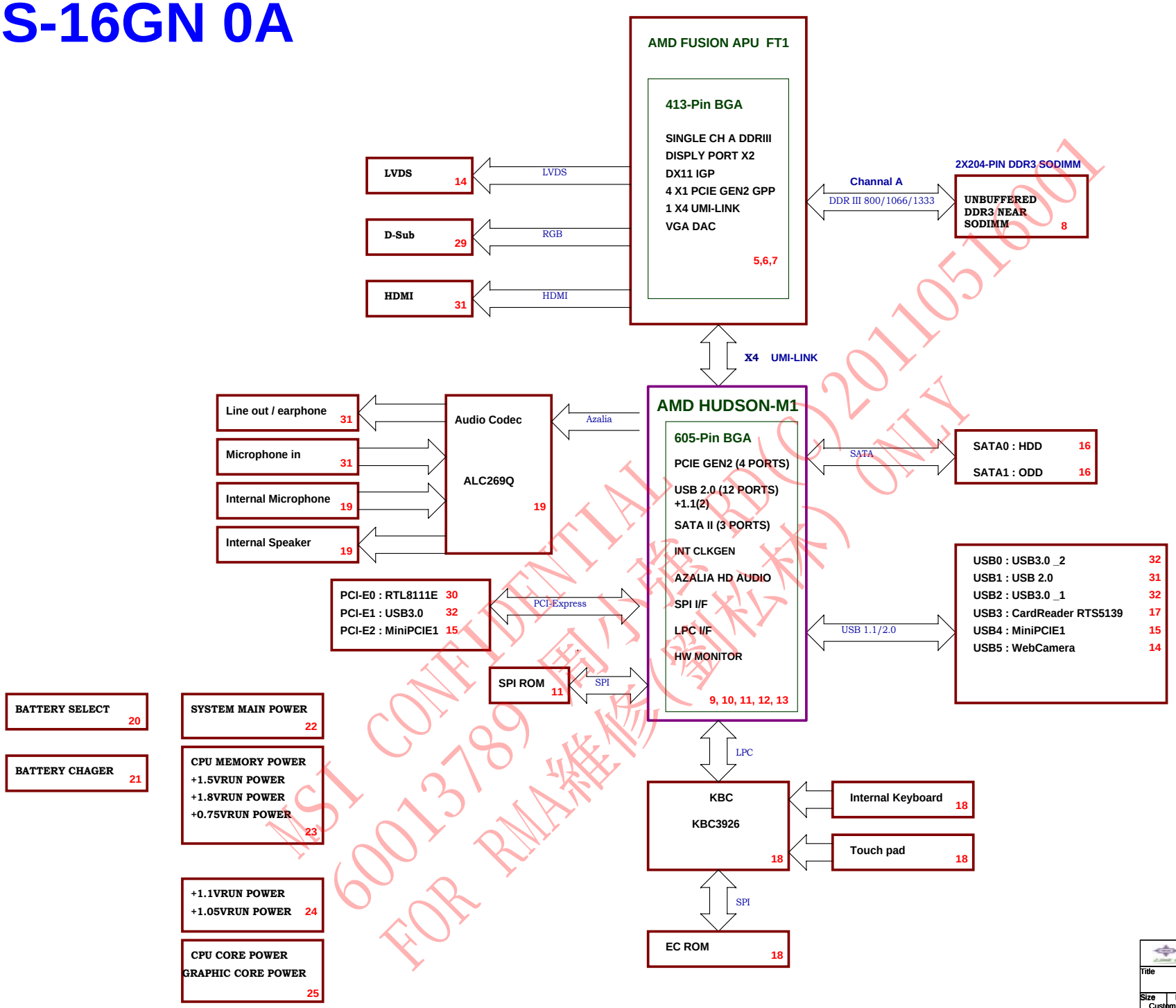
MS-16GN 0A

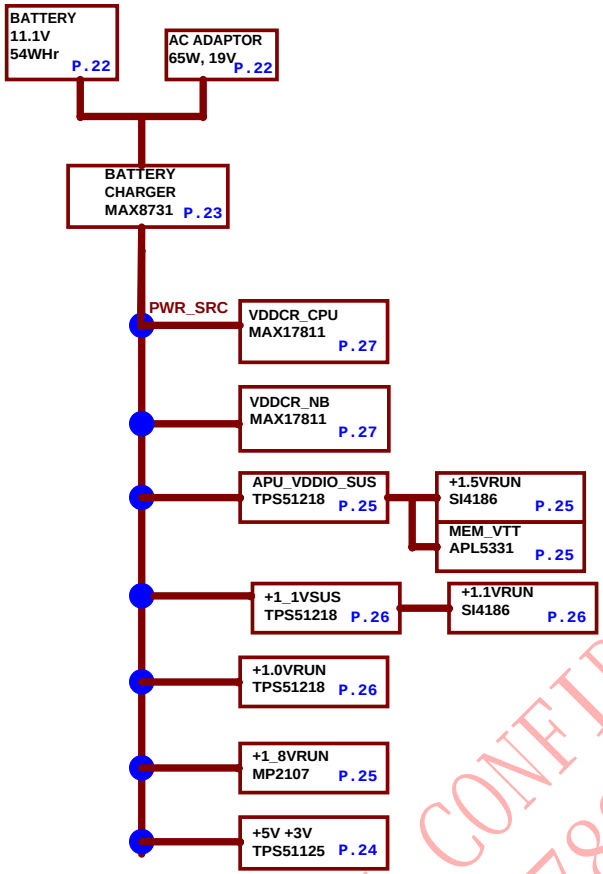


MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-16GN | Rev: 0.A

Date: Thursday, September 30, 2010 | Sheet 1 of 41



AMD FT1

VDDCR_CPU	VDDCR_CPU 0.85V---1.25V 11A
VDDCR_NB	VDDCR_NB 0..85V~0.9V 10A
APU_VDDIO_SUS	APU_VDDIO_SUS 2A
+1.8VRUN	VDD18 2A ;VDD_18_DAC 0.15A
+1.0VRUN	VDD_10 5.5A;VDDPL_10 0.2A
+3VRUN	VDD33 0.5A

HUDSON-M1

+3VRUN	VDDIO_33_PCIGP 3.3V 0.042A
+1_8VRUN	VDDIO_18_FC 1.8V 0.050A
+1.1VRUN	VDDAN_11_PCIE 1.1V 1.115A
+3VRUN	VDDPL_33_PCIE 3.3V 0.022A
+1.1VRUN	VDDAN_11_SATA 1.1V 1.3A
+3VRUN	VDDPL_33_SATA 3.3V 0.015A
+3VSUS	VDDAN_33_USB_S 3.3V 0.53A
+1_1VSUS	VDDAN_11_USB_S 1.1V 0.09A
+1.1VRUN	VDDCR_11 1.1V 0.79A
+1.1VRUN	VDDAN_11_CLK 1.1V 0.4A
+1_1VSUS	VDDRF_GBE_S
+3.VSUS	VDDIO_33_GBE_S 3.3V
+1_1VSUS	VDDCR_11_GBE_S 1.1V
+1_1VSUS	VDDIO_GBE_S 3.3V
+3VSUS	VDDIO_33_S 3.3V 0.049A
+1_1VSUS	VDDCR_11_S 1.1V 0.165A
+1_1VSUS	VDDCD_11_USB 1.1V 0.05A
AZ_VDDIO_DUAL	VDDIO_AZ_S 3.3V OR 1.5V 0.015A
+1_1VSUS	VDDCR_11_USB_S 1.1V
+3VRUN	VDDPL_33_SYS 3.3V SYS PLL 0.065A
+1.1VRUN	VDDPL_11_SYS 1.1 V SYS PLL 0.06A
+3VSUS	VDDPL_33_USB_S 3.3 V USB PLL 0.01A
+3VSUS	VDDAN_33_S 3.3V HWM 0.01A
+3VSUS	VDDXL_33_S 3.3V 0.005A

DDRIII SODIMMX2--SYSTEM

+1_5VDIMM	VDD MEM 4A
MEM_VTT	VTT_MEM 0.5A

LCD PANEL

+3VRUN	3.3V 1.5A
PWR_SRC	5V 0.3A

USB 3.0

+5VSUS	5VDual 0.9A
+3VSUS	VDD33 0.05A
+1.05VSUS_LDO	VDD11 0.6A

USB X2 FR

+5VSUS	5VDual 0.5A*2

MINI PCIE SLOT0,1

+1_5VRUN	1.5V (S0, S1) 0.5A each
+3VRUN	3.3V (S0, S1) 1.5A each

SATA HD0,1

	3.3V (S0, S1) TBD
+5VRUN	5V (S0, S1) 0.9A

CPU FAN

+5VRUN	5.0V (S0, S1) 0.5A

GIGA LAN

+1_0V_SWITCH	1.0V CORE 0.3A
+3VSUS	3V ANALOG 0.16A

HD CODEC

+5VRUN	5V CORE 0.3A
+3VRUN	3V ANALOG 0.1A

AUDIO OP

CARDREADER

+3VRUN	3V CORE 0.45A
+3.3V_CARD_SWITCH	3V_CARD 0.25A

MICRO-STAR INT'L CO.,LTD.

Title: POWER DELIVERY

Size: Custom | Document Number: MS-16GN | Rev: 0.A

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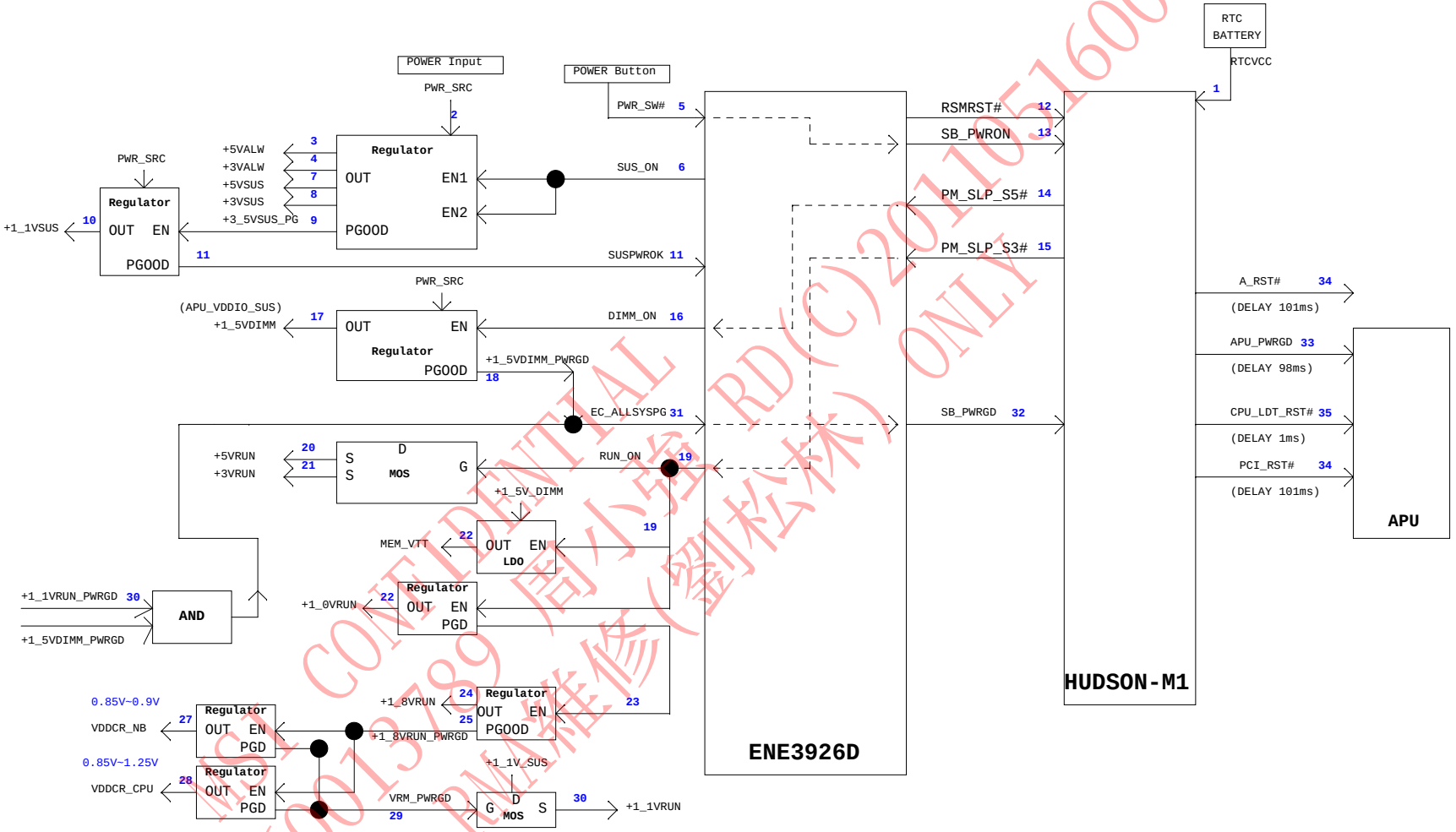

MSI MICRO-STAR INT'L CO.,LTD.

Title: POWER ON BLOCK

Size: C | Document Number: MS-16GN | Rev: 0.A

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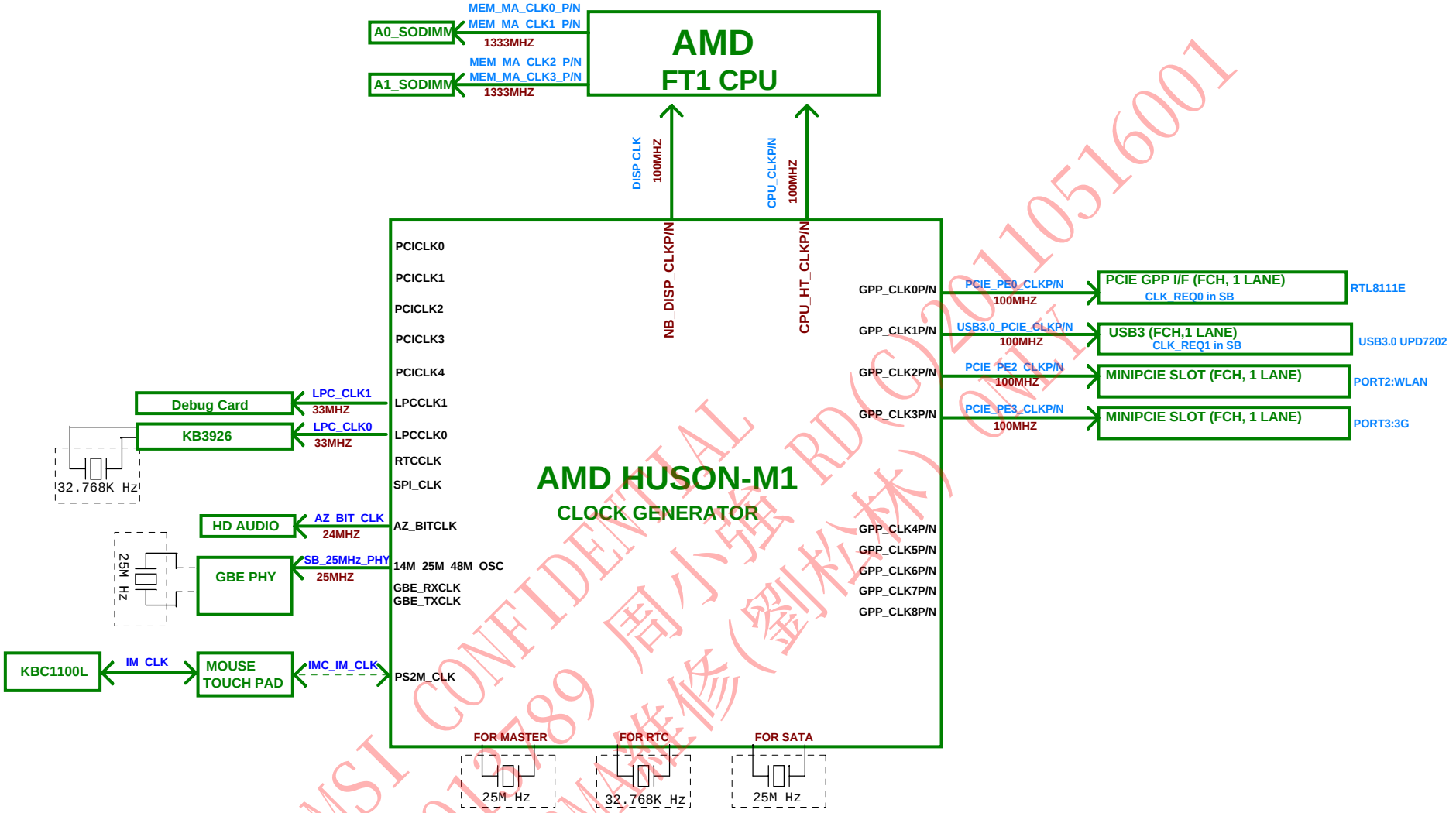
INTERNAL CLOCK MODE

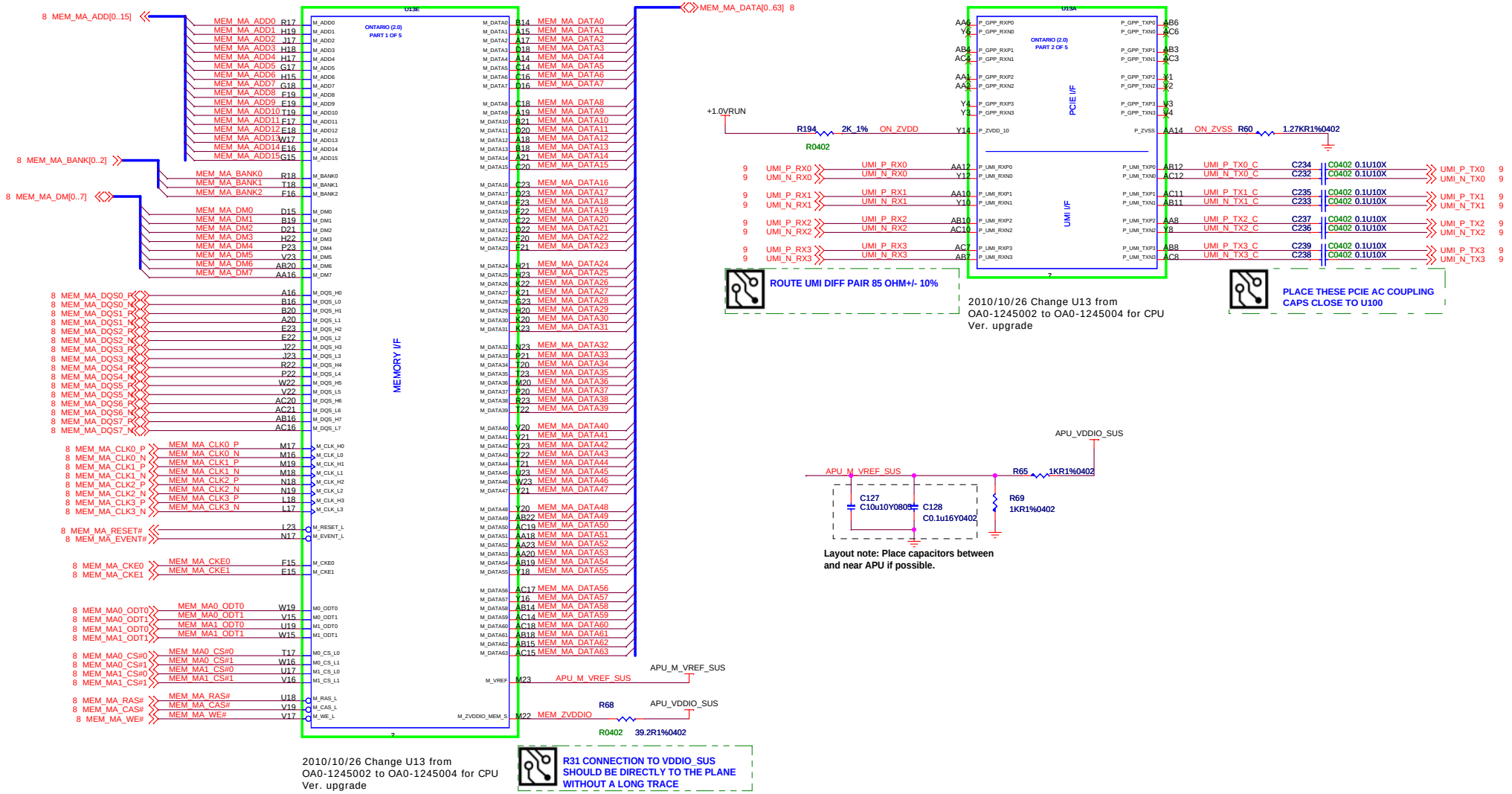


MICRO-STAR INT'L CO.,LTD.

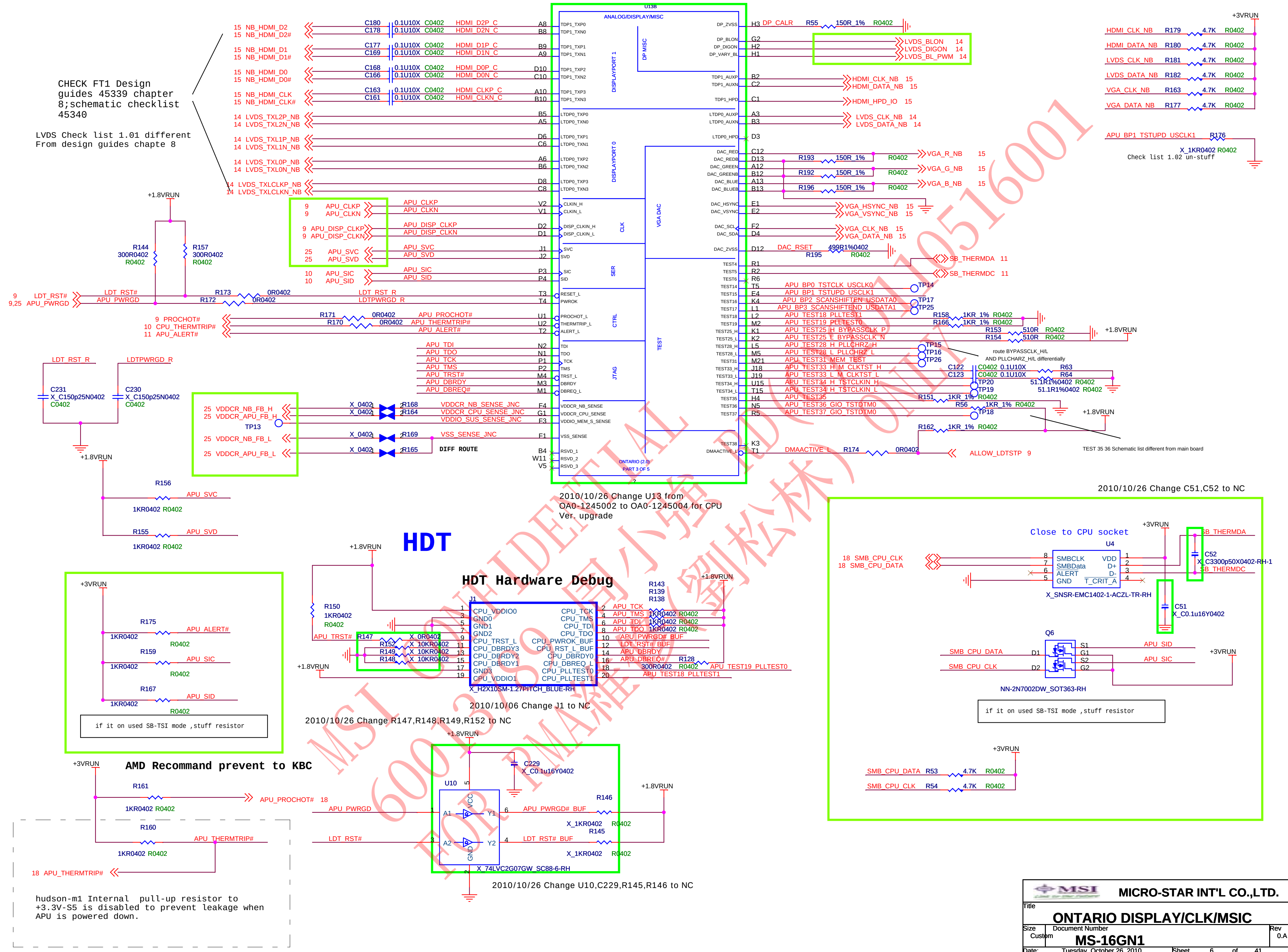
Title: CLOCK Distribution

Size: Custom | Document Number: MS-16GN | Rev: 0.A

Date: Thursday, September 30, 2010 | Sheet 4 of 41



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	ONTARIO MEM & PCIE	
Size: Custom	Document Number: MS-16GN1	Rev: 0.A
Date: Tuesday, October 26, 2010	Sheet 5 of 41	


CHECK FT1 Design guides 45339 chapter 8;schematic checklist 45340
LVDS Check list 1.01 different From design guides chapte 8
Check list 1.02 un-stuff
route BYPASSCLK_H/L AND PLLCHARZ_H/L differentially
TEST 35 36 Schematic list different from main board
DIFF ROUTE
ONTARIO (2.0) PART 3 OF 5
2010/10/26 Change U13 from OA0-1245002 to OA0-1245004 for CPU Ver. upgrade
2010/10/26 Change C51,C52 to NC
Close to CPU socket
HDT
HDT Hardware Debug
2010/10/06 Change J1 to NC
2010/10/26 Change R147,R148,R149,R152 to NC
if it on used SB-TSI mode ,stuff resistor
AMD Recommand prevent to KBC
hudson-m1 Internal pull-up resistor to +3.3V-S5 is disabled to prevent leakage when APU is powered down.
2010/10/26 Change U10,C229,R145,R146 to NC

MICRO-STAR INT'L CO.,LTD.

Title	ONTARIO DISPLAY/CLK/MSIC		
Size: Custom	Document Number: MS-16GN1		Rev: 0.A
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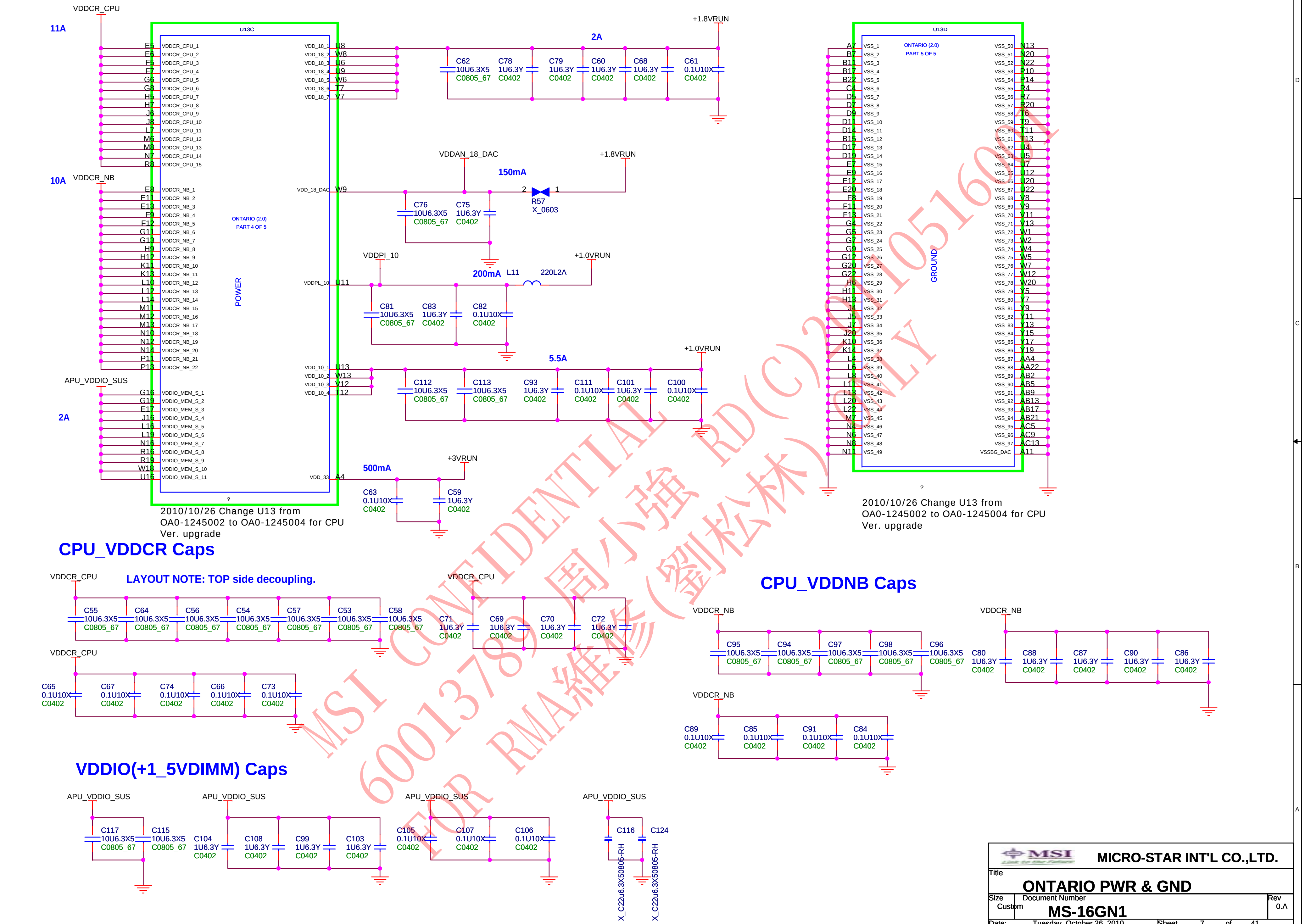
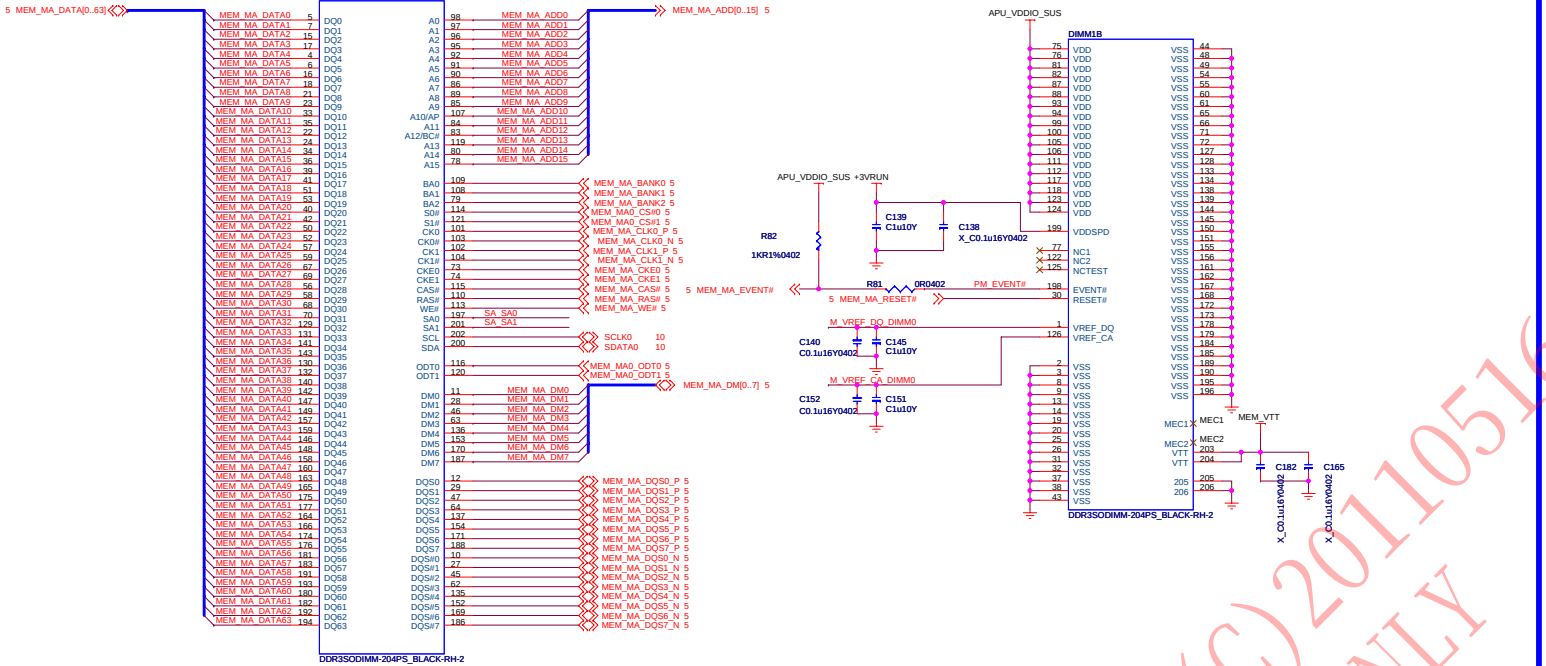
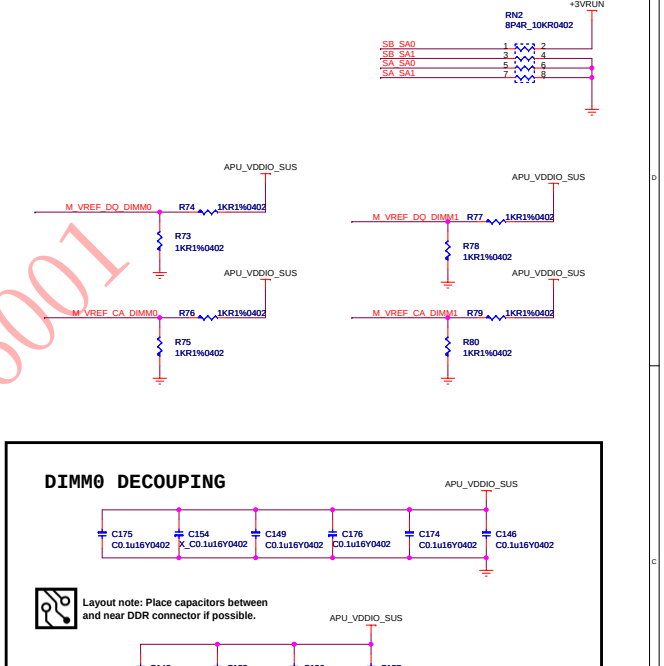


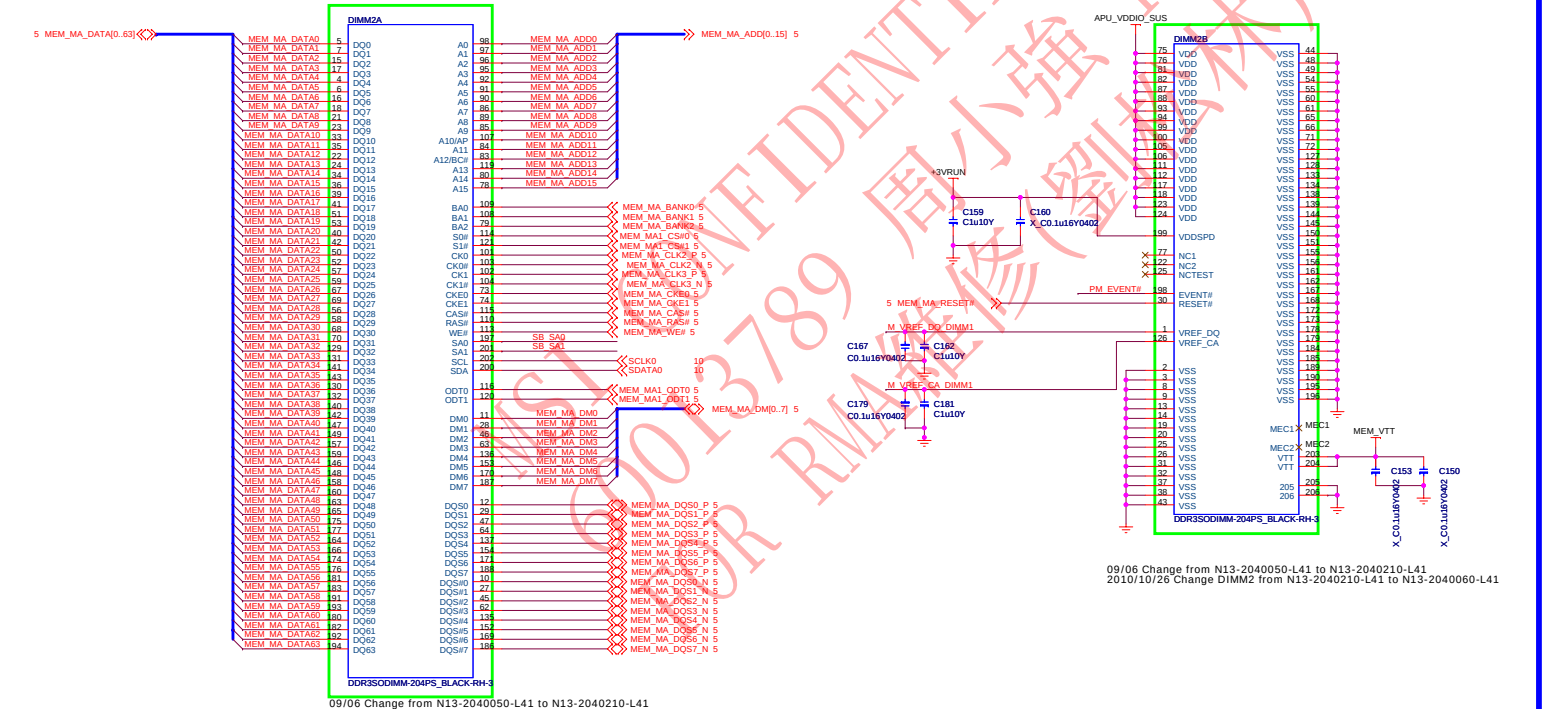
VDDCR_CPU
11A
U13C
ONTARIO (2.0)
PART 4 OF 5
POWER
+1.8VRUN
2A
C62 10U6.3X5 C0805_67
C78 1U6.3Y C0402
C79 1U6.3Y C0402
C60 1U6.3Y C0402
C68 1U6.3Y C0402
C61 0.1U10X C0402
VDDAN_18_DAC
150mA
R57 X_0603
C76 10U6.3X5 C0805_67
C75 1U6.3Y C0402
10A
VDDCR_NB
VDDPI_10
+1.0VRUN
200mA
L11 220L2A
C81 10U6.3X5 C0805_67
C83 1U6.3Y C0402
C82 0.1U10X C0402
5.5A
C112 10U6.3X5 C0805_67
C113 10U6.3X5 C0805_67
C93 1U6.3Y C0402
C111 0.1U10X C0402
C101 1U6.3Y C0402
C100 0.1U10X C0402
APU_VDDIO_SUS
2A
+3VRUN
500mA
C63 0.1U10X C0402
C59 1U6.3Y C0402
2010/10/26 Change U13 from OA0-1245002 to OA0-1245004 for CPU Ver. upgrade
U13D
ONTARIO (2.0)
PART 5 OF 5
GROUND
2010/10/26 Change U13 from OA0-1245002 to OA0-1245004 for CPU Ver. upgrade
CPU_VDDCR Caps
LAYOUT NOTE: TOP side decoupling.
C55 C64 C56 C54 C57 C53 C58 10U6.3X5 C0805_67
C71 C69 C70 C72 1U6.3Y C0402
C65 C67 C74 C66 C73 0.1U10X C0402
CPU_VDDNB Caps
VDDCR_NB
C95 C94 C97 C98 C96 10U6.3X5 C0805_67
C80 C88 C87 C90 C86 1U6.3Y C0402
C89 C85 C91 C84 0.1U10X C0402
VDDIO(+1_5VDIMM) Caps
C117 C115 10U6.3X5 C0805_67
C104 C108 C99 C103 1U6.3Y C0402
C105 C107 C106 0.1U10X C0402
C116 C124 X_C22u6.3X50805-RH

MICRO-STAR INT'L CO.,LTD.

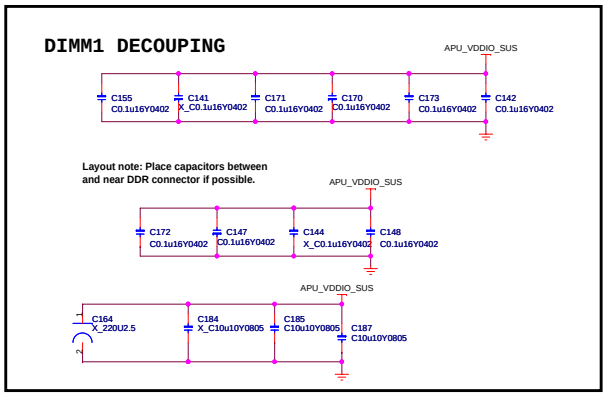
Title	ONTARIO PWR & GND
Size: Custom	Document Number: MS-16GN1
Rev	0.A
Date:	Tuesday, October 26, 2010
Sheet	7 of 41







09/06 Change from N13-2040050-L41 to N13-2040210-L41
2010/10/26 Change DIMM2 from N13-2040210-L41 to N13-2040060-L41



09/06 Change from N13-2040050-L41 to N13-2040210-L41
2010/10/26 Change DIMM2 from N13-2040210-L41 to N13-2040060-L41

MICRO-STAR INT'L CO.,LTD.

Title: DDRIII SODIMM

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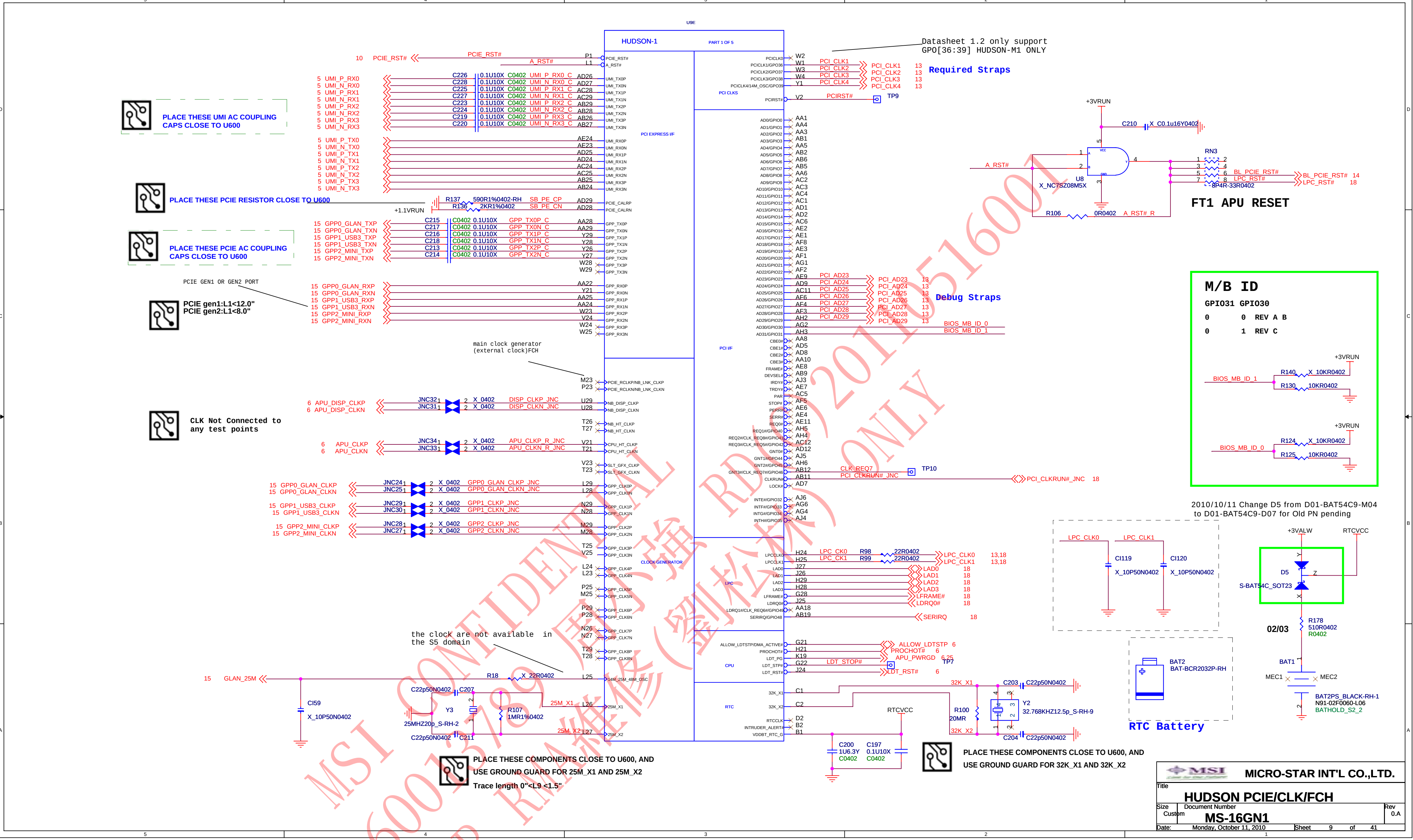
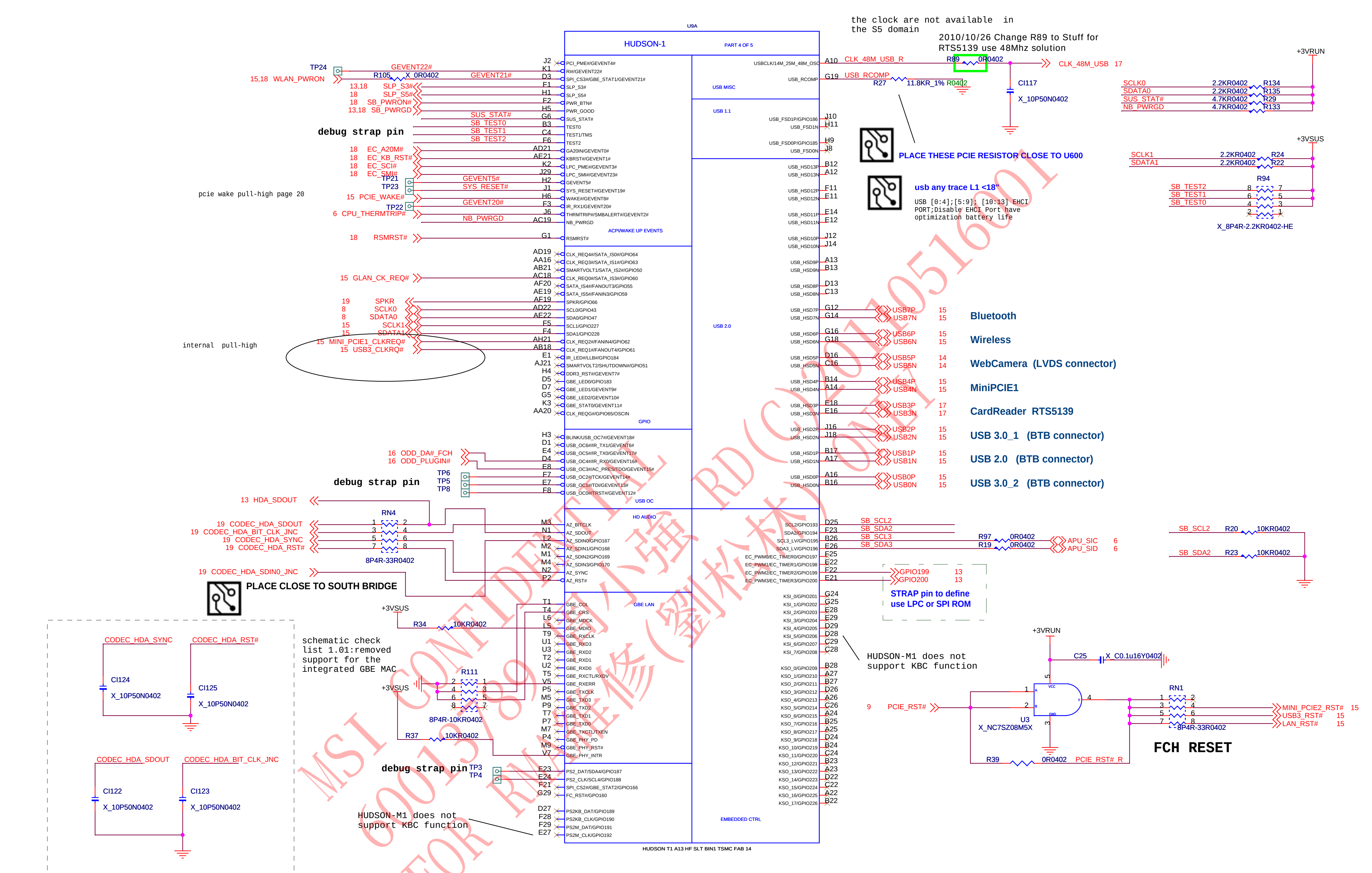

HUDSON-1
PART 1 OF 5
Datasheet 1.2 only support
GPO[36:39] HUDSON-M1 ONLY
Required Straps
PLACE THESE UMI AC COUPLING CAPS CLOSE TO U600
PLACE THESE PCIE RESISTOR CLOSE TO U600
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600
PCIE GEN1 OR GEN2 PORT
PCIE gen1:L1<12.0"
PCIE gen2:L1<8.0"
main clock generator
(external clock)FCH
CLK Not Connected to any test points
the clock are not available in the S5 domain
PCI EXPRESS I/F
PCI CLKS
PCI I/F
CLOCK GENERATOR
LPC
CPU
RTC
FT1 APU RESET
Debug Straps
M/B ID
GPIO31 GPIO30
0 0 REV A B
0 1 REV C
2010/10/11 Change D5 from D01-BAT54C9-M04
to D01-BAT54C9-D07 for Old PN pending
RTC Battery
PLACE THESE COMPONENTS CLOSE TO U600, AND
USE GROUND GUARD FOR 25M_X1 AND 25M_X2
Trace length 0"<L9 <1.5"
PLACE THESE COMPONENTS CLOSE TO U600, AND
USE GROUND GUARD FOR 32K_X1 AND 32K_X2
MICRO-STAR INT'L CO.,LTD.
Title
HUDSON PCIE/CLK/FCH
Size Custom
Document Number
MS-16GN1
Rev 0.A
Date: Monday, October 11, 2010
Sheet 9 of 41



U9A
HUDSON-1
PART 4 OF 5
the clock are not available in the S5 domain
2010/10/26 Change R89 to Stuff for RTS5139 use 48Mhz solution
CLK_48M_USB_R
R89 0R0402
CLK_48M_USB 17
USB_RCOMP
R27 11.8KR_1% R0402
CI117
X_10P50N0402
+3VRUN
SCLK0 2.2KR0402 R134
SDATA0 2.2KR0402 R135
SUS_STAT# 4.7KR0402 R29
NB_PWRGD 4.7KR0402 R133
+3VSUS
SCLK1 2.2KR0402 R24
SDATA1 2.2KR0402 R22
R94
SB_TEST2
SB_TEST1
SB_TEST0
X_8P4R-2.2KR0402-HE
PLACE THESE PCIE RESISTOR CLOSE TO U600
usb any trace L1 <18"
USB [0:4];[5:9]; [10:13] EHCI PORT;Disable EHCI Port have optimization battery life
TP24
15,18 WLAN_PWRON
R105 X_0R0402
GEVENT22#
GEVENT21#
13,18 SLP_S3#
18 SLP_S5#
18 SB_PWRON#
13,18 SB_PWRGD
SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
debug strap pin
18 EC_A20M#
18 EC_KB_RST#
18 EC_SCI#
18 EC_SMI#
TP21
TP23
GEVENT5#
SYS_RESET#
pcie wake pull-high page 20
15 PCIE_WAKE#
TP22
GEVENT20#
6 CPU_THERMTRIP#
NB_PWRGD
18 RSMRST#
15 GLAN_CK_REQ#
19 SPKR
8 SCLK0
8 SDATA0
15 SCLK1
15 SDATA1
internal pull-high
15 MINI_PCIE1_CLKREQ#
15 USB3_CLKRQ#
USB MISC
USB 1.1
USB 2.0
ACPI/WAKE UP EVENTS
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
USB7P 15 / USB7N 15 Bluetooth
USB6P 15 / USB6N 15 Wireless
USB5P 14 / USB5N 14 WebCamera (LVDS connector)
USB4P 15 / USB4N 15 MiniPCIE1
USB3P 17 / USB3N 17 CardReader RTS5139
USB2P 15 / USB2N 15 USB 3.0_1 (BTB connector)
USB1P 15 / USB1N 15 USB 2.0 (BTB connector)
USB0P 15 / USB0N 15 USB 3.0_2 (BTB connector)
16 ODD_DA#_FCH
16 ODD_PLUGIN#
debug strap pin
TP6
TP5
TP8
13 HDA_SDOUT
RN4
19 CODEC_HDA_SDOUT
19 CODEC_HDA_BIT_CLK_JNC
19 CODEC_HDA_SYNC
19 CODEC_HDA_RST#
8P4R-33R0402
19 CODEC_HDA_SDIN0_JNC
PLACE CLOSE TO SOUTH BRIDGE
SB_SCL2
SB_SDA2
SB_SCL3
SB_SDA3
R97 0R0402
R19 0R0402
APU_SIC 6
APU_SID 6
SB_SCL2 R20 10KR0402
SB_SDA2 R23 10KR0402
GPIO199 13
GPIO200 13
STRAP pin to define use LPC or SPI ROM
+3VSUS
R34 10KR0402
schematic check list 1.01:removed support for the integrated GBE MAC
CODEC_HDA_SYNC
CODEC_HDA_RST#
CI124
X_10P50N0402
CI125
X_10P50N0402
R111
8P4R-10KR0402
R37 10KR0402
CODEC_HDA_SDOUT
CODEC_HDA_BIT_CLK_JNC
CI122
X_10P50N0402
CI123
X_10P50N0402
debug strap pin
TP3
TP4
HUDSON-M1 does not support KBC function
HUDSON-M1 does not support KBC function
+3VRUN
C25 X_C0.1u16Y0402
9 PCIE_RST#
U3
X_NC7SZ08M5X
RN1
MINI_PCIE2_RST# 15
USB3_RST# 15
LAN_RST# 15
8P4R-33R0402
R39 0R0402 PCIE_RST#_R
FCH RESET
HUDSON T1 A13 HF SLT BIN1 TSMC FAB 14

MICRO-STAR INT'L CO.,LTD.

Title: **HUDSON GPIO/USB/AUDIO**

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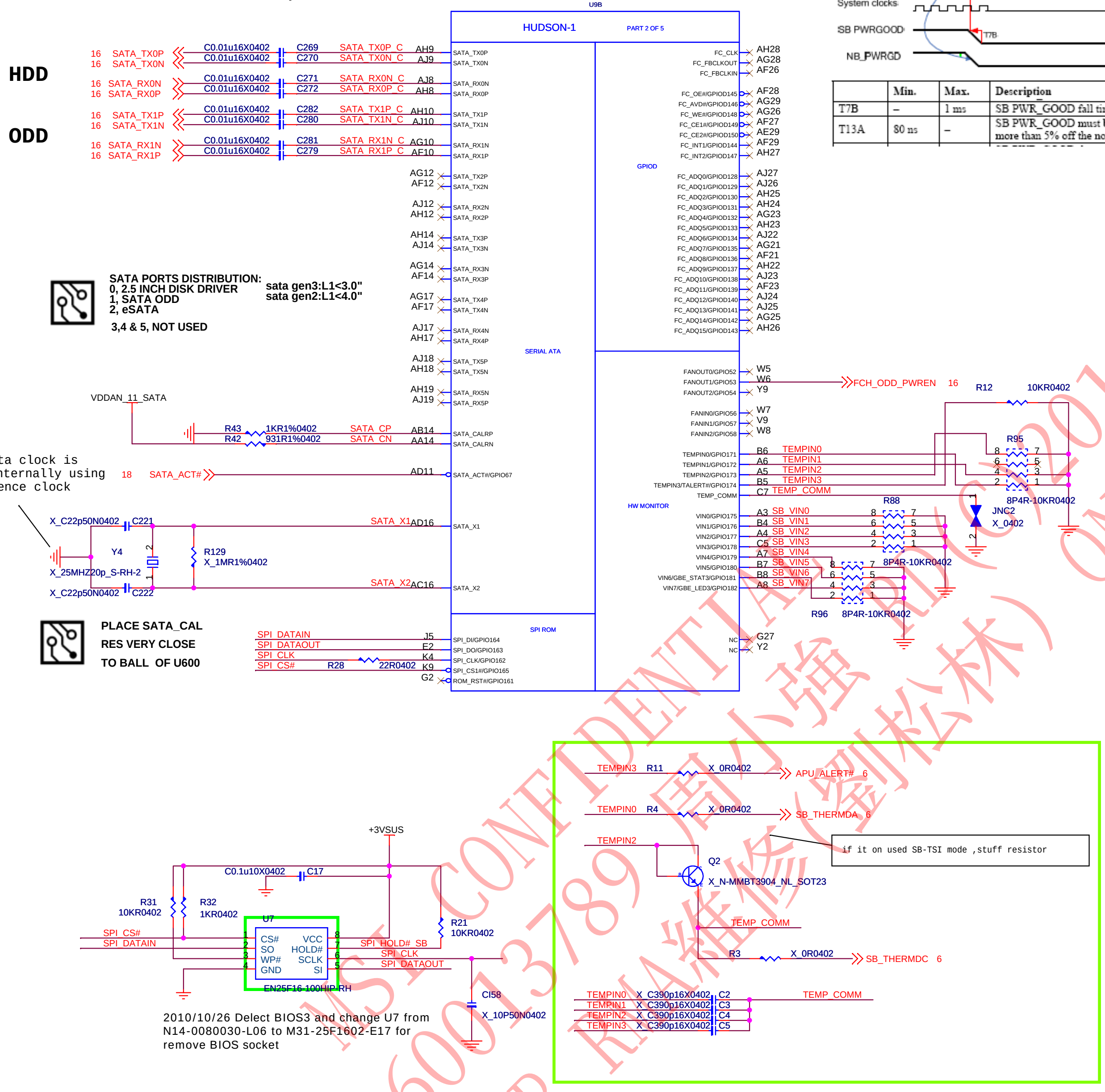
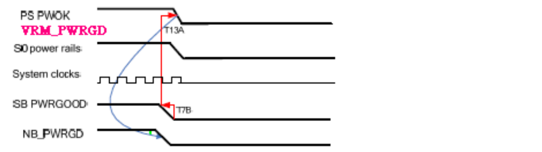
Date: Tuesday, October 26, 2010 Sheet 10 of 41

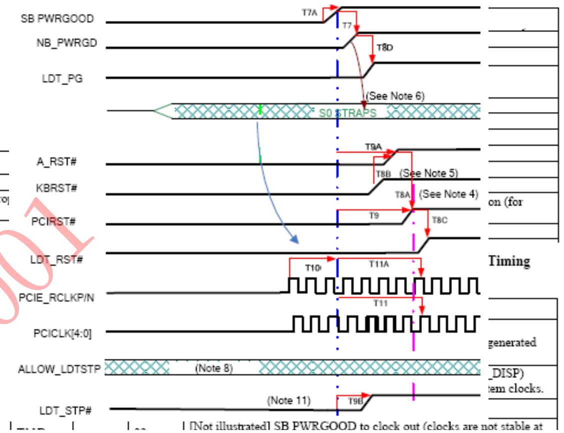
SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only



U9B
HUDSON-1
PART 2 OF 5
HDD
ODD
16 SATA_TX0P
16 SATA_TX0N
16 SATA_RX0N
16 SATA_RX0P
16 SATA_TX1P
16 SATA_TX1N
16 SATA_RX1N
16 SATA_RX1P
C0.01u16X0402
C269
C270
C271
C272
C282
C280
C281
C279
SATA_TX0P_C
SATA_TX0N_C
SATA_RX0N_C
SATA_RX0P_C
SATA_TX1P_C
SATA_TX1N_C
SATA_RX1N_C
SATA_RX1P_C
SERIAL ATA
GPIOD
SATA PORTS DISTRIBUTION:
0, 2.5 INCH DISK DRIVER
1, SATA ODD
2, eSATA
3,4 & 5, NOT USED
sata gen3:L1<3.0"
sata gen2:L1<4.0"
VDDAN_11_SATA
R43 1KR1%0402
R42 931R1%0402
SATA_CP
SATA_CN
not used.sata clock is
generated internally using
25mhz reference clock
18 SATA_ACT#
X_C22p50N0402
C221
C222
Y4
X_25MHZ20p_S-RH-2
R129
X_1MR1%0402
SATA_X1
SATA_X2
PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600
SPI ROM
SPI_DATAIN
SPI_DATAOUT
SPI_CLK
SPI_CS#
R28 22R0402
HW MONITOR
FCH_ODD_PWREN 16
R12 10KR0402
R95
8P4R-10KR0402
TEMPIN0
TEMPIN1
TEMPIN2
TEMPIN3
TEMP_COMM
R88
SB_VIN0
SB_VIN1
SB_VIN2
SB_VIN3
SB_VIN4
SB_VIN5
SB_VIN6
SB_VIN7
JNC2
X_0402
R96 8P4R-10KR0402
+3VSUS
C0.1u10X0402
C17
R31 10KR0402
R32 1KR0402
U7
CS# VCC
SO HOLD#
WP# SCLK
GND SI
EN25F16-100HIP-RH
SPI_HOLD#_SB
R21 10KR0402
CI58
X_10P50N0402
2010/10/26 Delect BIOS3 and change U7 from
N14-0080030-L06 to M31-25F1602-E17 for
remove BIOS socket
TEMPIN3 R11 X_0R0402 APU_ALERT# 6
TEMPIN0 R4 X_0R0402 SB_THERMDA 6
if it on used SB-TSI mode ,stuff resistor
Q2
X_N-MMBT3904_NL_SOT23
R3 X_0R0402 SB_THERMDC 6
X_C390p16X0402
C2
C3
C4
C5



	Min.	Max.	Description
T7B	–	1 ms	SB PWR_GOOD fall time.
T13A	80 ns	–	SB PWR_GOOD must be de-asserted before VDD (PS PWOK) drop more than 5% off the nominal value. See Note 9.



	Min.	Max.	Description
T7			See Table 33 and Table 34 below.
T7A	–	50 ms	SB PWR_GOOD rise time (10% to 90 %). See Note 3.
T8A	0 ns Note 4	100 ns	A_RST# (PCI host bus reset) to PCIRST#.
T8B	–	Note 5	KBRST# to A_RST#.
T8C	1.0 ms	2.3 ms	PCIRST# to LDT_RST#.
T8D	77 ms	108 ms	NB_PWRGD to LDT_PG.
T9	101 ms	113 ms	SB PWR_GOOD to PCIRST#.
T9A	101 ms	113 ms	SB PWR_GOOD to A_RST# (T9-T8A).
T9B	31 ms	–	SB PWR_GOOD to LDT_STP#.
T10	-31 ms	–	PCIE_CLKP/N stable time before SB PWRGOOD assertion (for external clock mode only).
T11	36 ms	41 ms	SB PWR_GOOD to stable PCICLK 33 MHz. See Note 8.

Table 33. Power Sequence SB PWRGOOD, NB_PWRGOOD, and System Clock Timing (For Internal Clock Mode Only)

Symbol	Min.	Max.	Description
T7	40ms	42ms	SB PWRGOOD assertion to NB_PWRGD assertion delay. **Note:** This timing only applies to the NB_PWRGD signal generated from SB820M.
T11A	-	38 ms	SB PWRGOOD to stable system clocks (CPU, PCI-E, NB_DISP) when SB820M clock function is enabled to provide all system clocks.
Symbol	**Min.**	**Max.**	**Description**
T11B	-	32 ms	[Not illustrated] SB PWRGOOD to clock out (clocks are not stable at this point).
T8D	58 ms	108 ms	NB_PWRGD to LDT_PG.

Table 34. Power Sequence SB PWRGOOD, NB_PWRGD, and System Clock Timing (For External Clock Mode Only)

Symbol	Min.	Max.	Description
T7	0ns	30ns	SB PWRGOOD assertion to NB_PWRGD assertion delay when using the SB820M NB_PWRGD output.

Note 4: Typical time between A_RST# and PCIRST# is 75 ns. The measurement should be done at 10% of both signals. Loading on the motherboard may cause the measurement at 90% be more than the spec.

Note 5: The KBRST# should be de-asserted before A_RST# (LDT_RST#) is de-asserted.

Note 6: Type II Standard and Debug straps will be latched after SB PWR_GOOD is asserted. Type I straps are latched on resume reset rising edge.

Note 8: The PCI Clock may be stable before T11 min. under some conditions; however in all cases, the PCI Clock is guaranteed to be stable only between T11 min. and max.

MICRO-STAR INT'L CO.,LTD.

Title: HUDSON SATA/DEBUG

Size: Custom | Document Number: MS-16GN1 | Rev: 0.A

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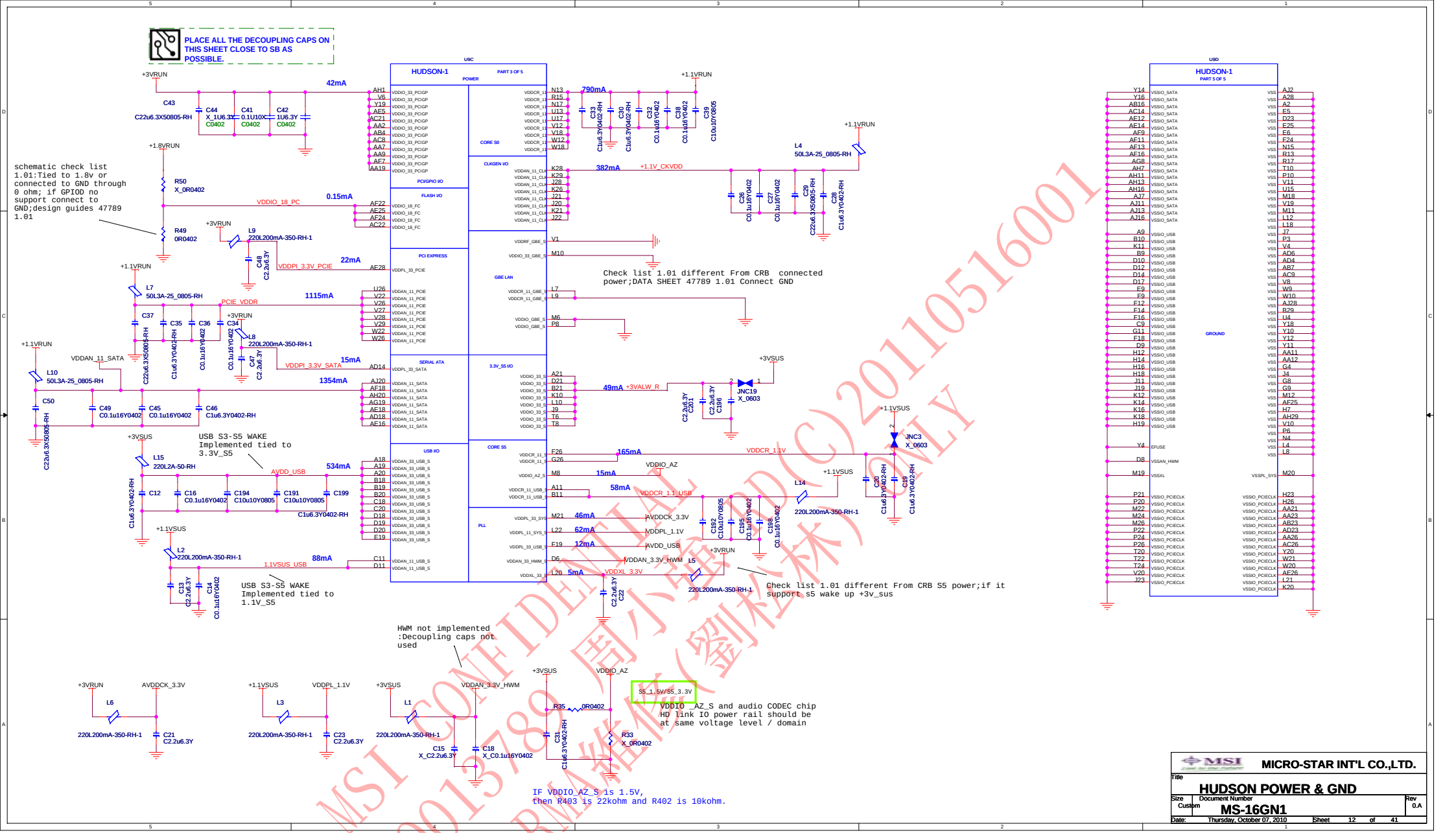
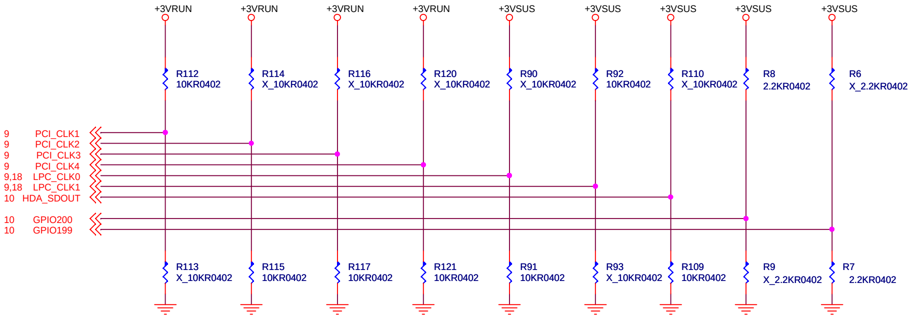
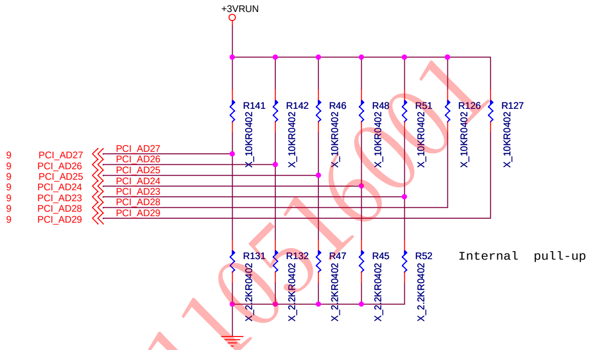



+3VRUN
+3VSUS
R112 10KR0402
R114 X_10KR0402
R116 X_10KR0402
R120 X_10KR0402
R90 X_10KR0402
R92 10KR0402
R110 X_10KR0402
R8 2.2KR0402
R6 X_2.2KR0402
9 PCI_CLK1
9 PCI_CLK2
9 PCI_CLK3
9 PCI_CLK4
9,18 LPC_CLK0
9,18 LPC_CLK1
10 HDA_SDOUT
10 GPIO200
10 GPIO199
R113 X_10KR0402
R115 10KR0402
R117 10KR0402
R121 10KR0402
R91 10KR0402
R93 X_10KR0402
R109 10KR0402
R9 X_2.2KR0402
R7 2.2KR0402


+3VRUN
R141 X_10KR0402
R142 X_10KR0402
R46 X_10KR0402
R48 X_10KR0402
R51 X_10KR0402
R126 X_10KR0402
R127 X_10KR0402
9 PCI_AD27
9 PCI_AD26
9 PCI_AD25
9 PCI_AD24
9 PCI_AD23
9 PCI_AD28
9 PCI_AD29
R131 X_2.2KR0402
R132 X_2.2KR0402
R47 X_2.2KR0402
R45 X_2.2KR0402
R52 X_2.2KR0402
Internal pull-up

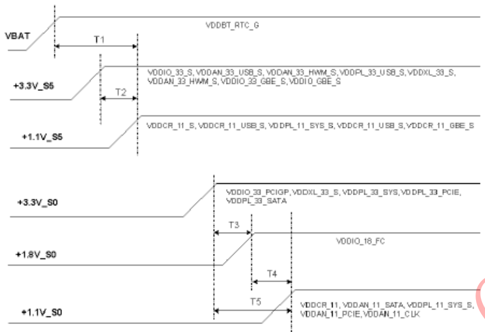
REQUIRED STRAPS

PCI CLK4;Applicable to internal clock gen mode only check list 1.01

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM

DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT


VBAT
VDDBT_RTC_G
T1
+3.3V_S5
VDDIO_33_S, VDDAN_33_USB_S, VDDAN_33_HWM_S, VDDPL_33_USB_S, VDDXL_33_S, VDDAN_33_HWM_S, VDDIO_33_GBE_S, VDDIO_GBE_S
T2
+1.1V_S5
VDDCR_11_S, VDDCR_11_USB_S, VDDPL_11_SYS_S, VDDCR_11_USB_S, VDDCR_11_GBE_S
+3.3V_S0
VDDIO_33_PCIGP, VDDXL_33_S, VDDPL_33_SYS, VDDPL_33_PCIE, VDDPL_33_SATA
T3
+1.8V_S0
VDDIO_18_FC
T4
T5
+1.1V_S0
VDDCR_11, VDDAN_11_SATA, VDDPL_11_SYS_S, VDDAN_11_PCIE, VDDAN_11_CLK

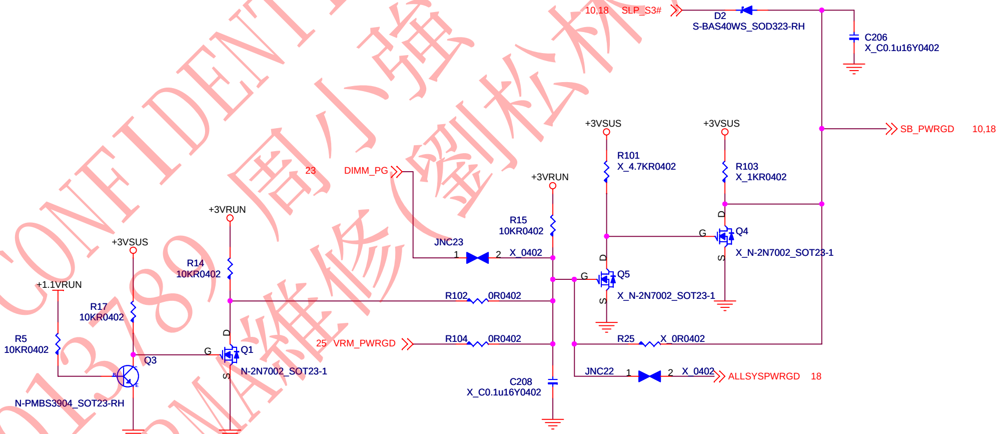
Symbol	Parameter	Voltage Difference During Ramping	
		Minimum (V)	Maximum (V)
T1	VBAT ramps high relative to the S5 rails.	See Note 1	No restrictions
T2	+3.3V_S5 rails ramp high relative to +1.1V_S5 rails.	0	No restrictions
T3	+3.3V_S0 rails ramp high relative to +1.8V_S0 rails.	0	No restrictions
T4	+1.8V_S0 rail ramps high relative to +1.1V_S0 rails.	0	No restrictions
T5	+3.3V_S0 rails ramp high relative to +1.1V_S0 rails.	0	No restrictions

Note 1: VBAT (VDDBT_RTC_G) must ramp at least 5 seconds before the S5 rails to allow start time for the internal RTC.

Note 2: For power down, the rails should either be turned off simultaneously or in the reverse of the order shown above. Variations in speeds of decay due to different capacitor discharge rates can be safely ignored. The VDDIO_33_S (S5_3.3V) power-rail ramp-down time must be more than 300 µs.

Note 3: Power rails from the same group are assumed to be generated from the same regulator. However, they can be generated from different regulators if all other requirements are met.

Note 4: The ramp-up time for all power rails except VDDIO_33_S must be in the 50 µs to 40 ms range (50 µs ≤ All power rails except VDDIOS_33_S ≤ 40 ms). However, the ramp-up time for VDDIO_33_S must be in the 100 µs to 40 ms range (100 µs ≤ VDDIOS_33_S ≤ 40 ms).


10,18 SLP_S3#
D2 S-BAS40WS_SOD323-RH
C206 X_C0.1u16Y0402
SB_PWRGD 10,18
+3VSUS
R101 X_4.7KR0402
R103 X_1KR0402
23 DIMM_PG
+3VRUN
R15 10KR0402
JNC23
X_0402
Q4 X_N-2N7002_SOT23-1
Q5 X_N-2N7002_SOT23-1
+3VRUN
R14 10KR0402
+3VSUS
+1.1VRUN
R17 10KR0402
R102 0R0402
R5 10KR0402
Q3
N-PMBS3904_SOT23-RH
Q1
N-2N7002_SOT23-1
25 VRM_PWRGD
R104 0R0402
R25 X_0R0402
C208 X_C0.1u16Y0402
JNC22
X_0402
ALLSYSPWRGD 18

MICRO-STAR INT'L CO.,LTD.

Title: HUDSON-STRAPS

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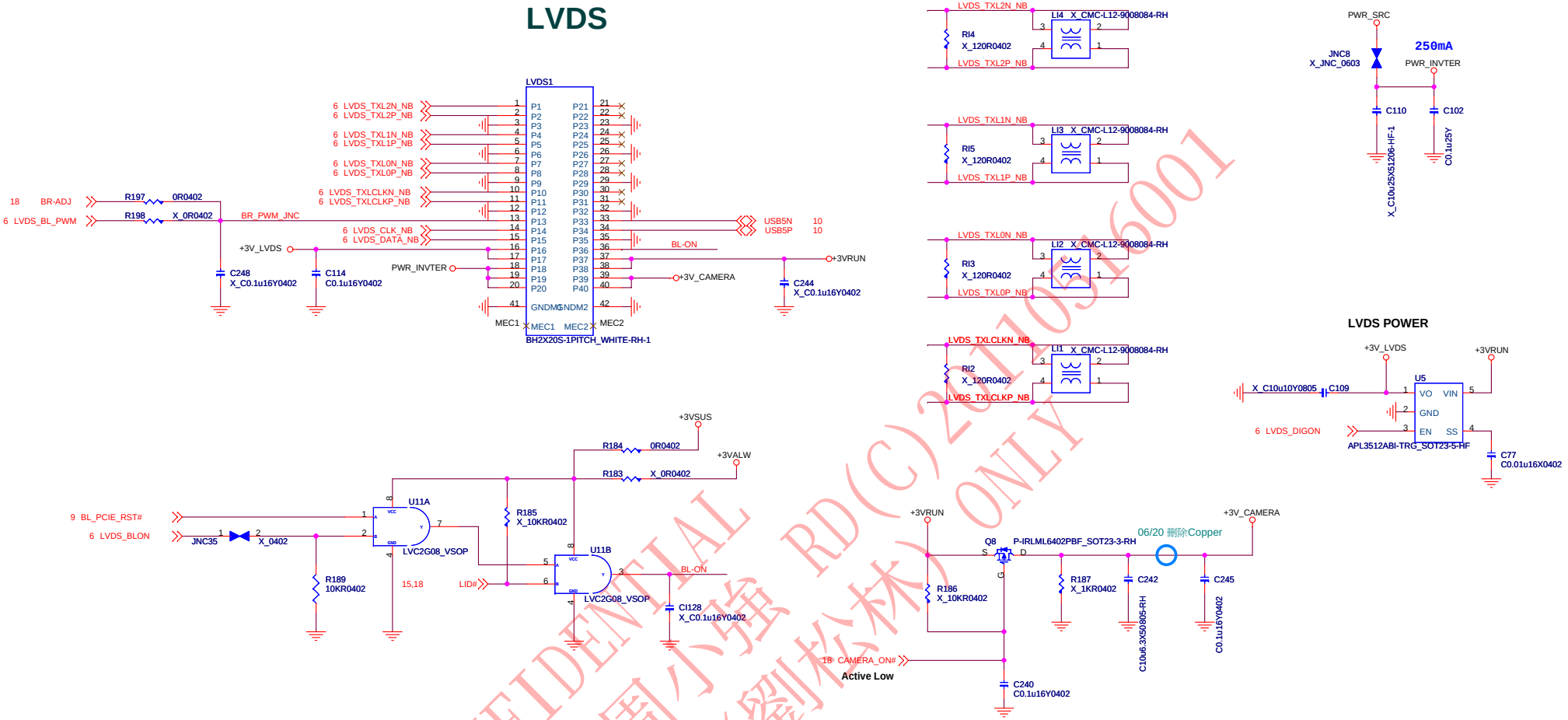
LVDS



MSI	MICRO-STAR INT'L CO.,LTD.	
Title: LVDS		
Size: Custom	Document Number: MS-16GN1	Rev: 0.A
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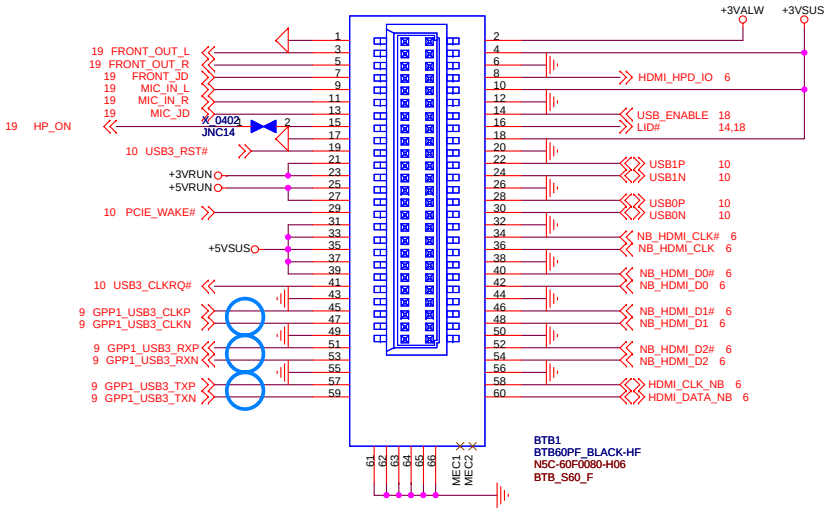
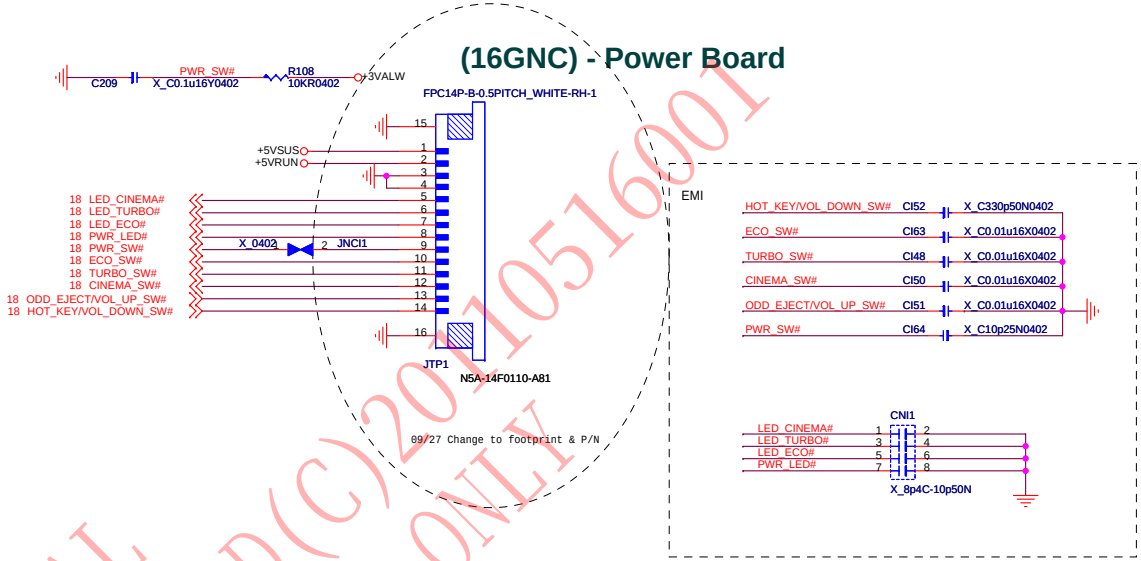
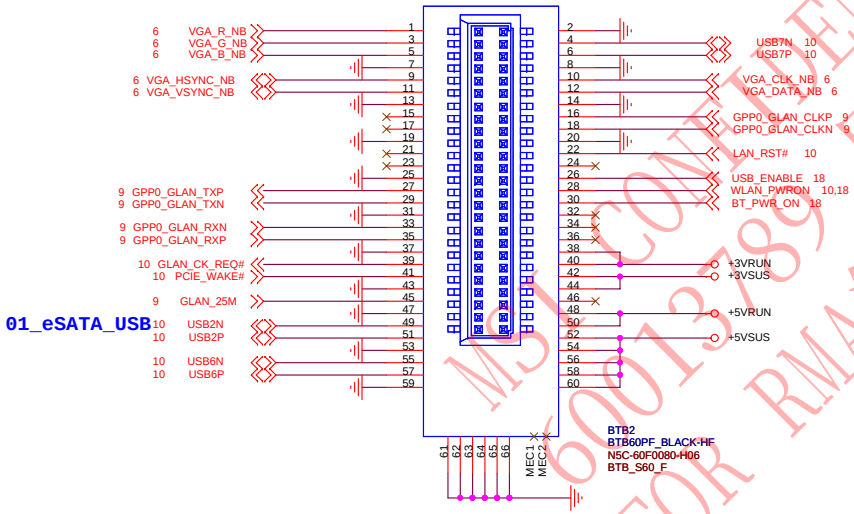
(16GNB) - HDMI/Audio/USB3.0



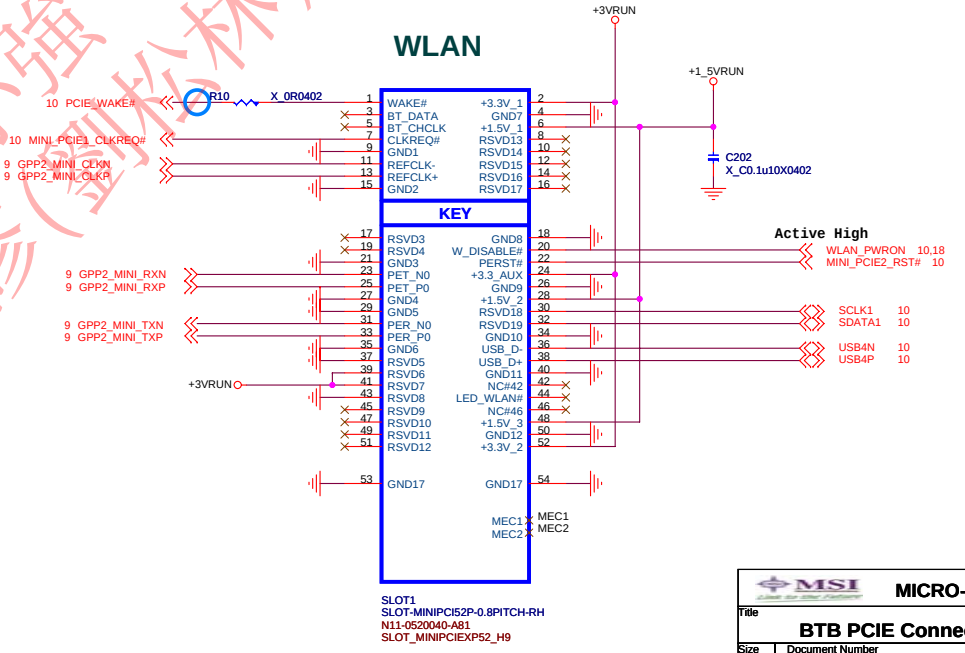
(16GNC) - Power Board



(16GNA) - CRT/USB2.0/GLAN



WLAN



MICRO-STAR INT'L CO.,LTD.

Title: BTB PCIE Connector

Size: Custom | Document Number: MS-16GN1 | Rev: 0.A

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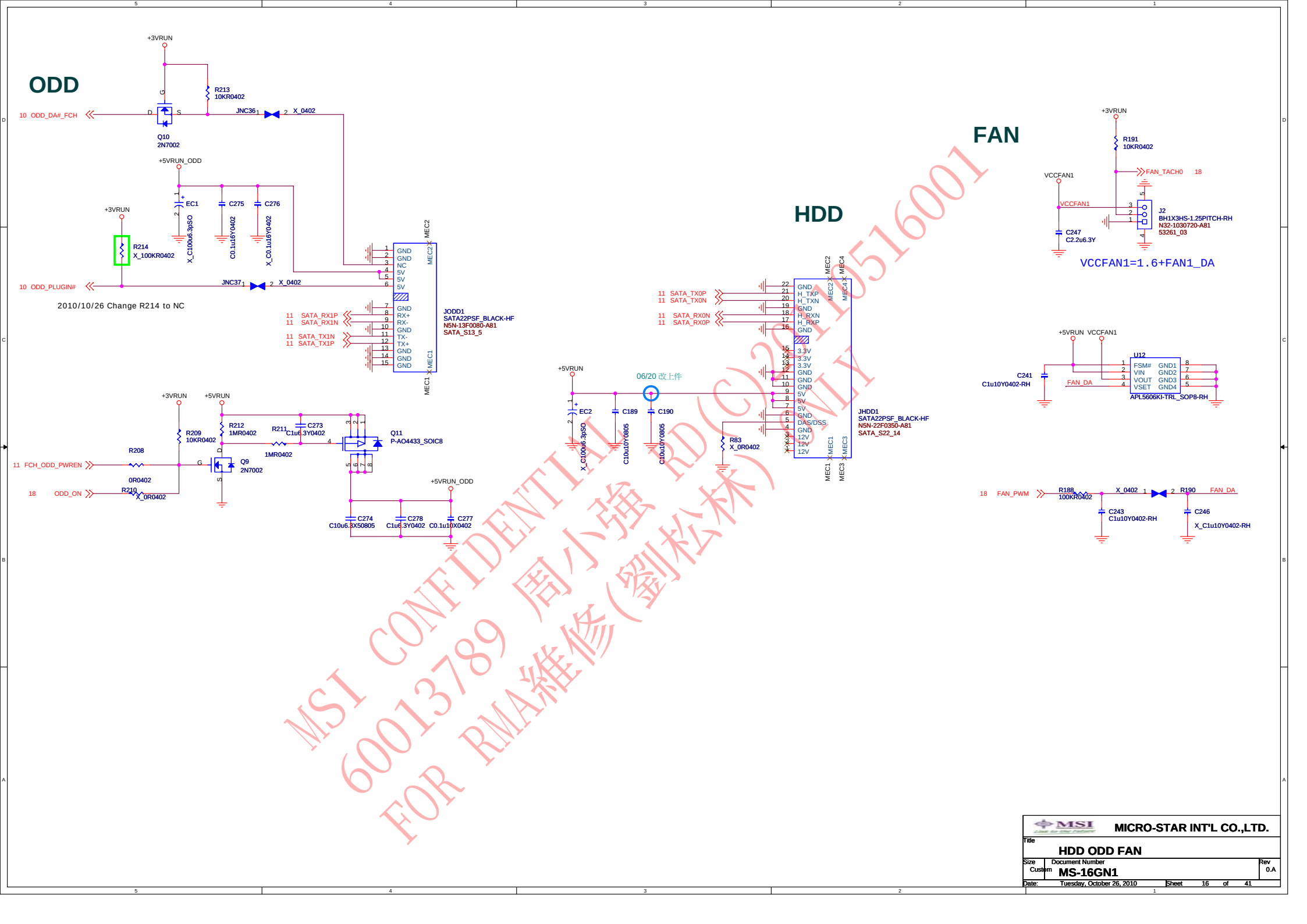

MICRO-STAR INT'L CO.,LTD.

Title: HDD ODD FAN

Size: Custom | Document Number: MS-16GN1 | Rev: 0.A

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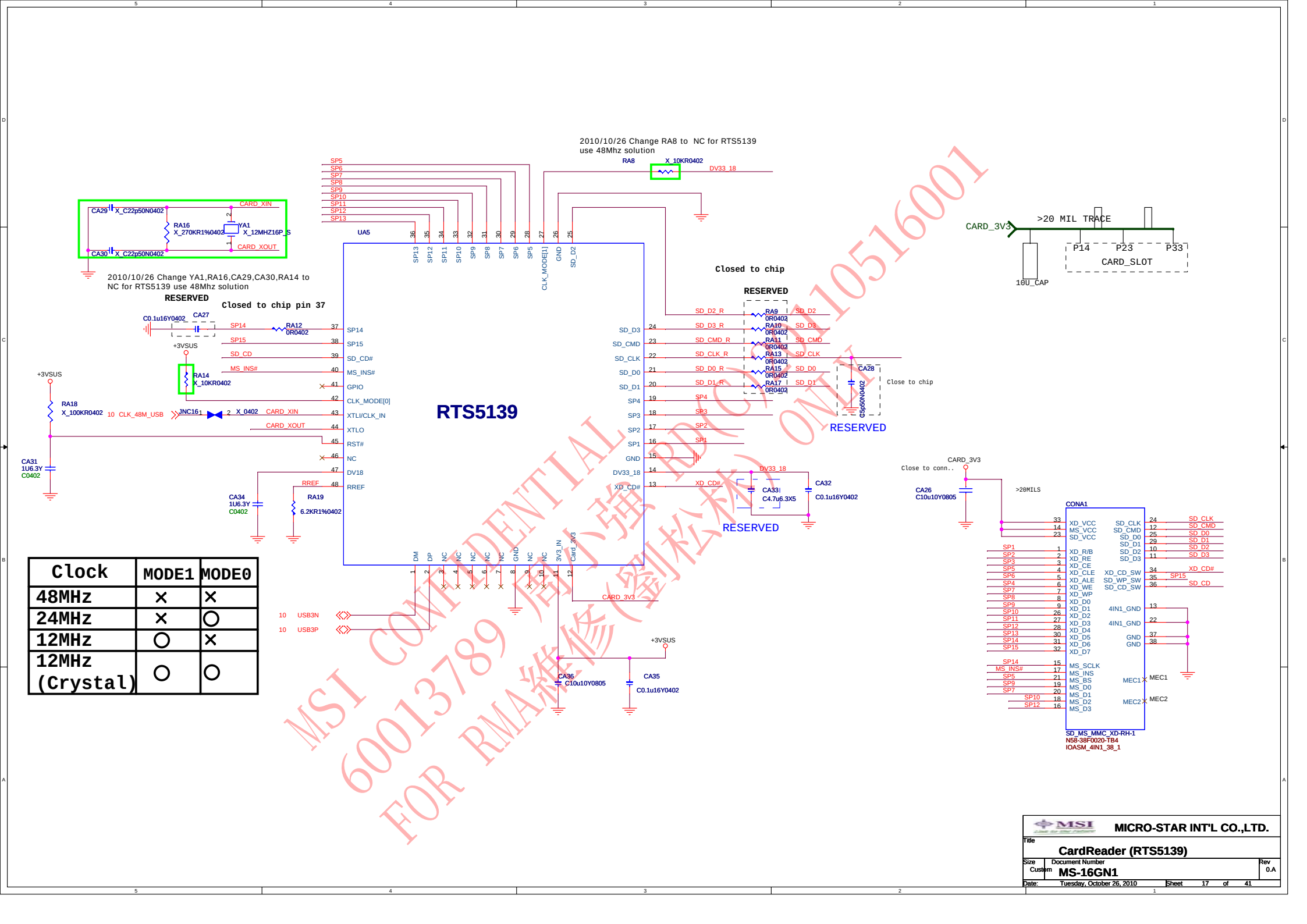

Clock	MODE1	MODE0
48MHz	✕	✕
24MHz	✕	○
12MHz	○	✕
12MHz (Crystal)	○	○

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	CardReader (RTS5139)		
Size: Custom	Document Number: MS-16GN1		Rev: 0.A
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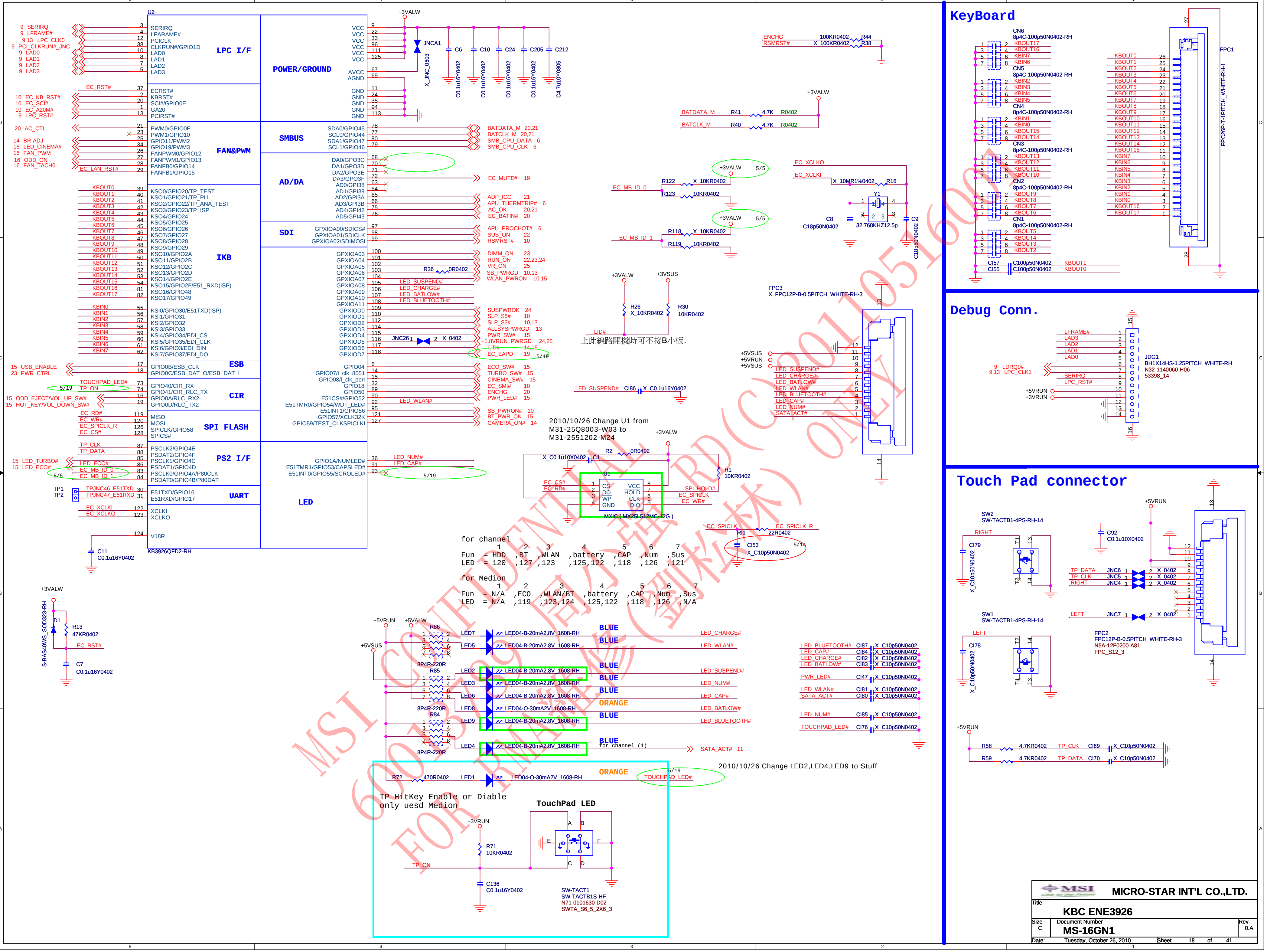

KeyBoard
Debug Conn.
Touch Pad connector
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
U2
KB3926QFD2-RH
CN6 8p4C-100p50N0402-RH
CN5 8p4C-100p50N0402-RH
CN4 8p4C-100p50N0402-RH
CN3 8p4C-100p50N0402-RH
CN2 8p4C-100p50N0402-RH
CN1 8p4C-100p50N0402-RH
FPC1
FPC26P-T-1PITCH_WHITE-RH-1
FPC3
X_FPC12P-B-0.5PITCH_WHITE-RH-3
JDG1
BH1X14HS-1.25PITCH_WHITE-RH
N32-1140060-H06
53398_14
FPC2
FPC12P-B-0.5PITCH_WHITE-RH-3
N5A-12F0200-A81
FPC_S12_3
SW2 SW-TACTB1-4PS-RH-14
SW1 SW-TACTB1-4PS-RH-14
Y1 32.768KHZ12.5p
上此線路開機時可不接B小板.
2010/10/26 Change U1 from
M31-25Q8003-W03 to
M31-2551202-M24
MXIC (MX25L512MC-12G)
for channel
1 2 3 4 5 6 7
Fun = HDD ,BT ,WLAN ,battery ,CAP ,Num ,Sus
LED = 120 ,127 ,123 ,125,122 ,118 ,126 ,121
for Medion
1 2 3 4 5 6 7
Fun = N/A ,ECO ,WLAN/BT ,battery ,CAP ,Num ,Sus
LED = N/A ,119 ,123,124 ,125,122 ,118 ,126 ,N/A
2010/10/26 Change LED2,LED4,LED9 to Stuff
TP HitKey Enable or Diable
only uesd Medion
TouchPad LED
SW-TACT1
SW-TACTB1S-HF
N71-0101630-D02
SWTA_S6_5_2X6_3
MICRO-STAR INT'L CO.,LTD.
Title
KBC ENE3926
Size C
Document Number
MS-16GN1
Rev 0.A
Date: Tuesday, October 26, 2010
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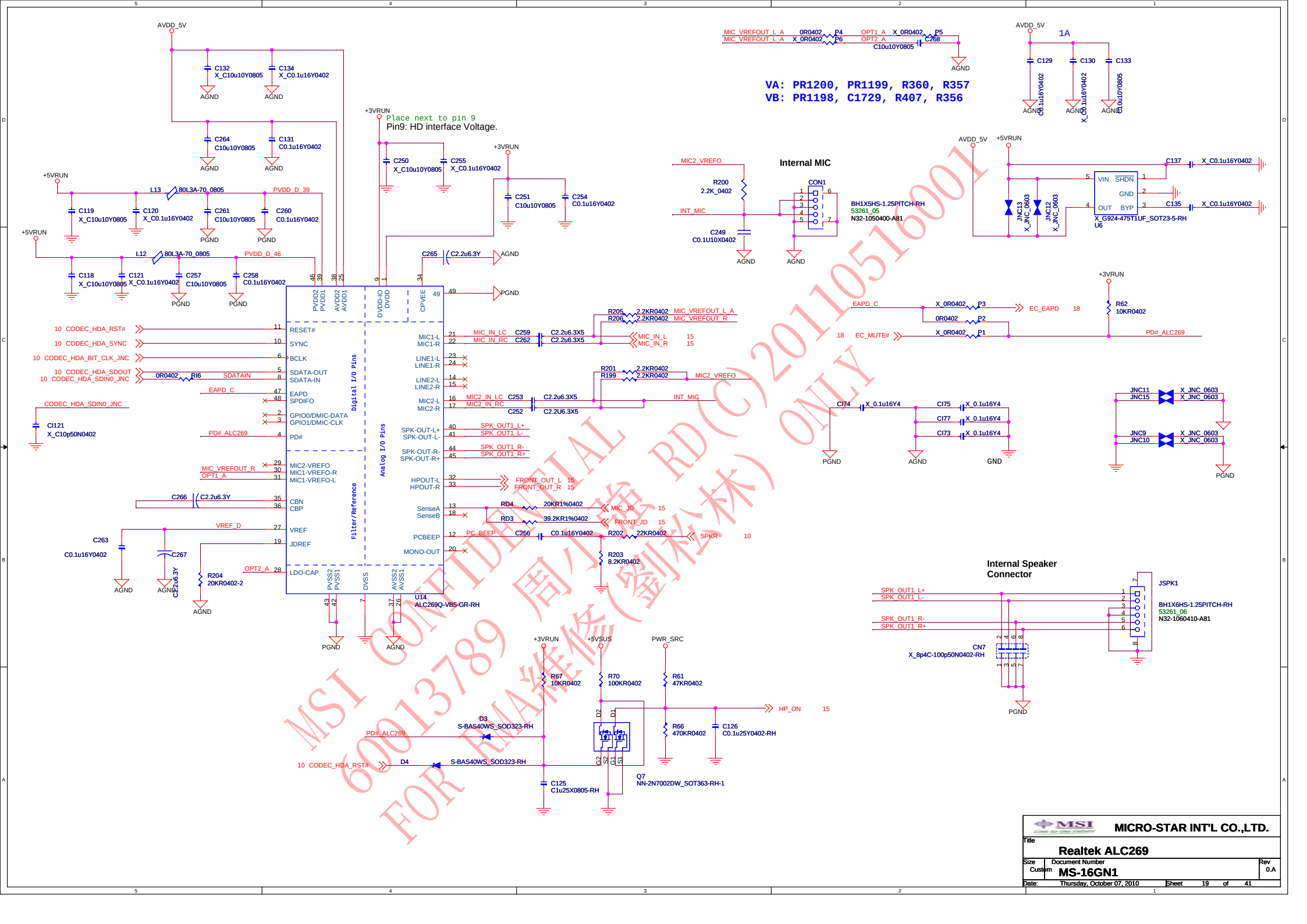
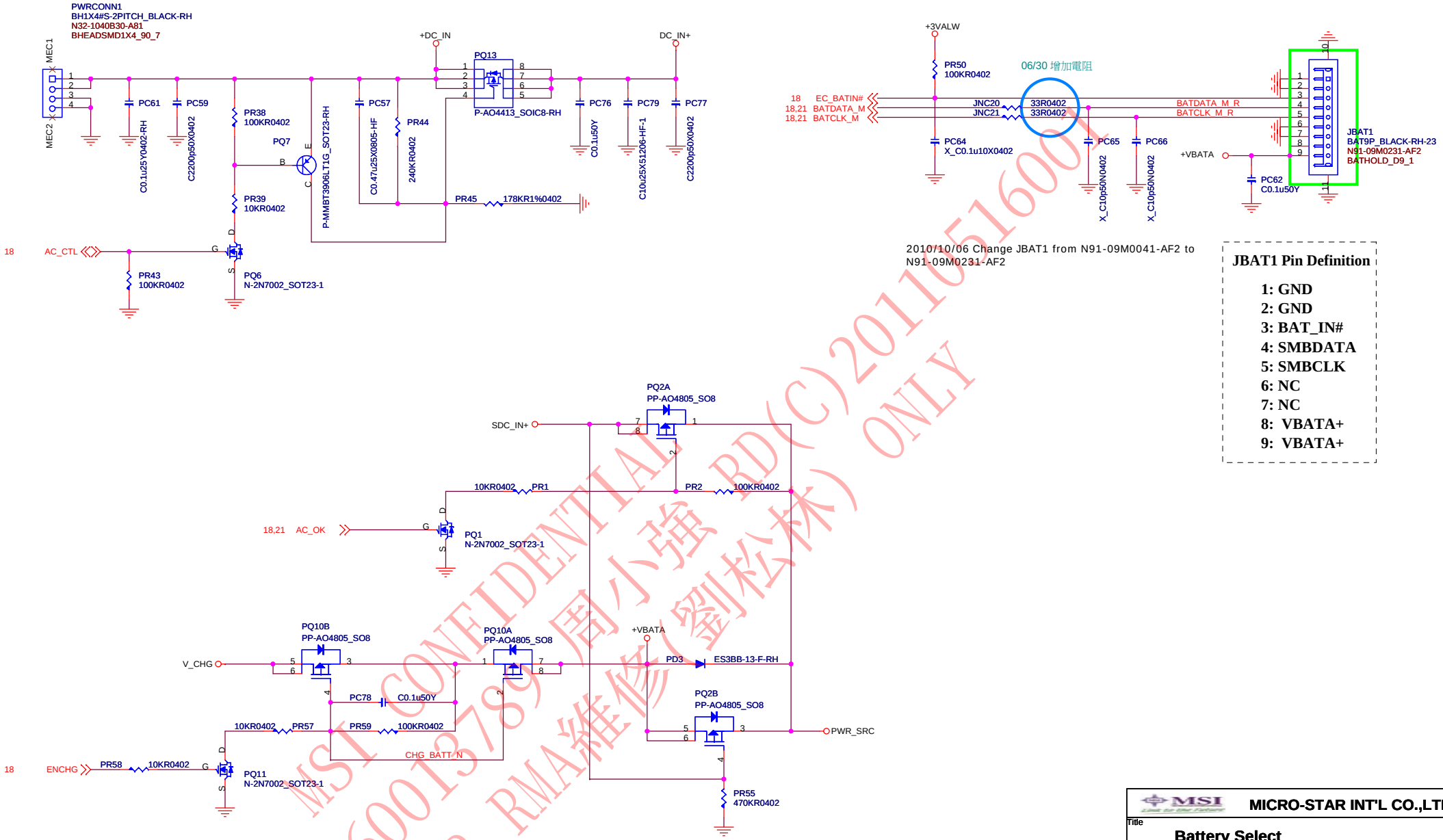

VA: PR1200, PR1199, R360, R357
VB: PR1198, C1729, R407, R356
Place next to pin 9
Pin9: HD interface Voltage.
Internal MIC
Internal Speaker Connector
U14
ALC269Q-VB5-GR-RH
Q7
NN-2N7002DW_SOT363-RH-1
MSI CONFIDENTIAL
60013789 周小锋 RD(C)20110516001
FOR RMA维修(刘松林) ONLY
MICRO-STAR INT'L CO.,LTD.
Realtek ALC269
MS-16GN1
Thursday, October 07, 2010



MICRO-STAR INT'L CO.,LTD.

Title: Battery Select

Size: Custom | Document Number: MS-16GM | Rev: 1.0

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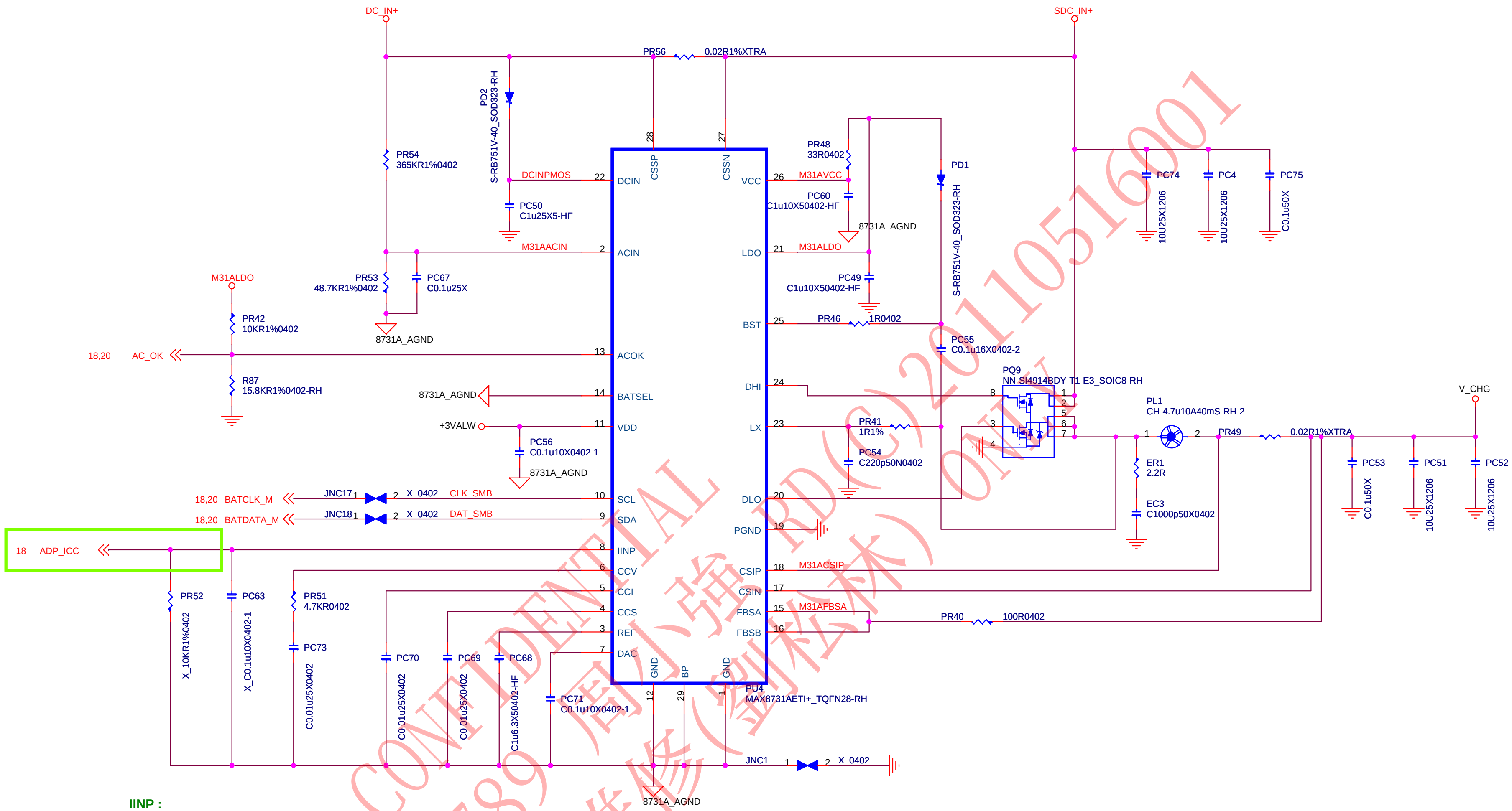

DC_IN+
SDC_IN+
PR56 0.02R1%XTRA
PD2 S-RB751V-40_SOD323-RH
PR54 365KR1%0402
DCINPMOS
PC50 C1u25X5-HF
M31AACIN
PR53 48.7KR1%0402
PC67 C0.1u25X
8731A_AGND
M31ALDO
PR42 10KR1%0402
18,20 AC_OK
R87 15.8KR1%0402-RH
8731A_AGND
+3VALW
PC56 C0.1u10X0402-1
18,20 BATCLK_M
18,20 BATDATA_M
JNC17 X_0402 CLK_SMB
JNC18 X_0402 DAT_SMB
18 ADP_ICC
PR52 X_10KR1%0402
PC63 X_C0.1u10X0402-1
PR51 4.7KR0402
PC73 C0.01u25X0402
PC70 C0.01u25X0402
PC69 C0.01u25X0402
PC68 C1u6.3X50402-HF
PC71 C0.1u10X0402-1
DCIN ACIN ACOK BATSEL VDD SCL SDA IINP CCV CCI CCS REF DAC
CSSP CSSN GND BP GND
VCC LDO BST DHI LX DLO PGND CSIP CSIN FBSA FBSB
PU4 MAX8731AETI+_TQFN28-RH
JNC1 X_0402
8731A_AGND
PR48 33R0402
M31AVCC
PC60 C1u10X50402-HF
M31ALDO
PC49 C1u10X50402-HF
PR46 1R0402
PC55 C0.1u16X0402-2
PD1 S-RB751V-40_SOD323-RH
PR41 1R1%
PC54 C220p50N0402
M31ACSIP
M31AFBSA
PR40 100R0402
PQ9 NN-SI4914BDY-T1-E3_SOIC8-RH
PC74 10U25X1206
PC4 10U25X1206
PC75 C0.1u50X
PL1 CH-4.7u10A40mS-RH-2
PR49 0.02R1%XTRA
V_CHG
ER1 2.2R
EC3 C1000p50X0402
PC53 C0.1u50X
PC51 10U25X1206
PC52 10U25X1206

IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. V_IINP = IINPUT x RS1 x 3mA/V x PR25

MICRO-STAR INT'L CO.,LTD.

Title	Battery Charger
Size	Custom
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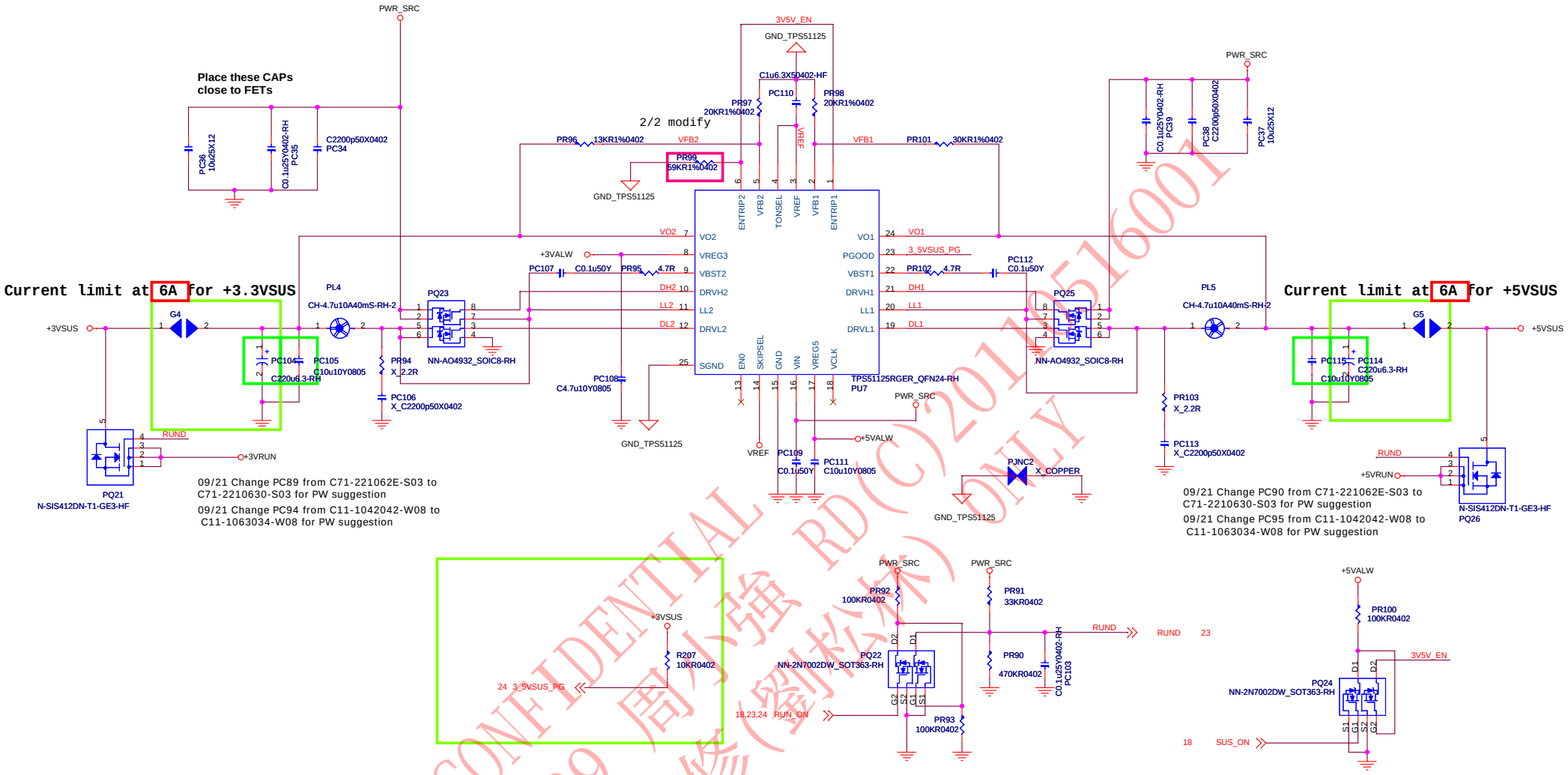

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	M_System Power		
Size: Custom	Document Number: MS-16GN1	Rev: 0.A	
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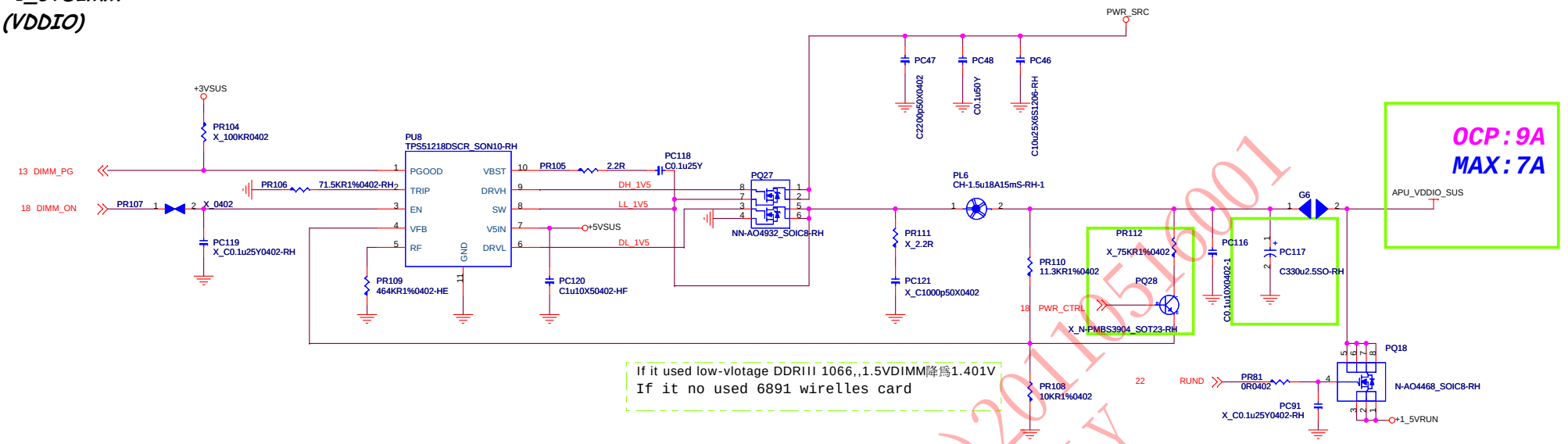
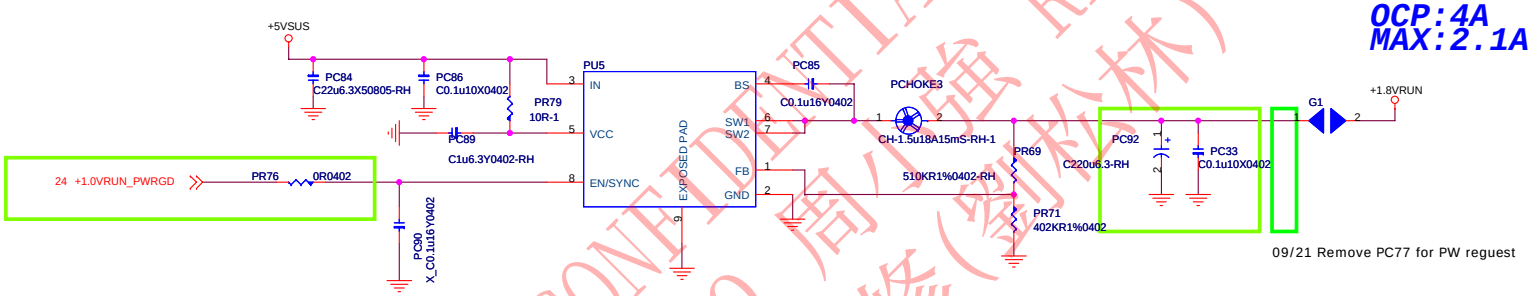
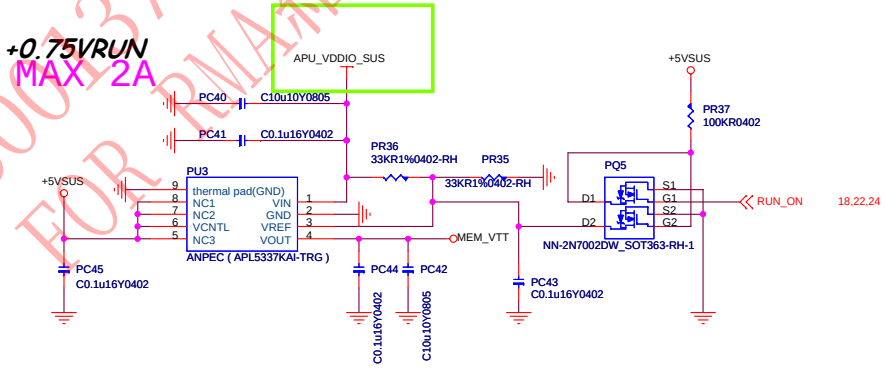
+1_5VDIMM (VDDIO)





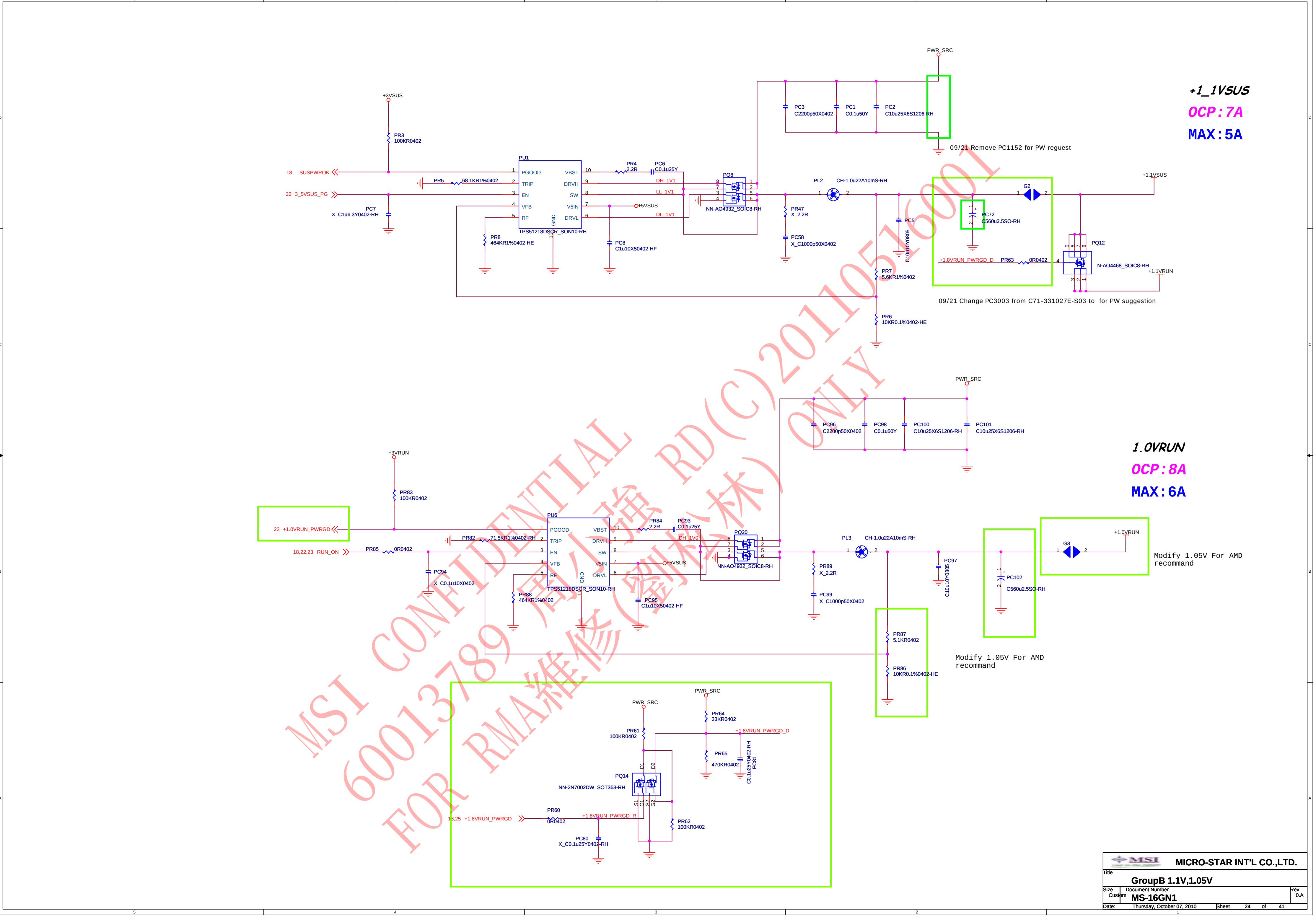


MICRO-STAR INT'L CO.,LTD.

Title: GroupA 1.8V 1.5V 0.75V

Size: Custom | Document Number: MS-16GN1 | Rev: 0.A

Date: Thursday, October 07, 2010 | Sheet 23 of 41



+1_1VSUS
OCP:7A
MAX:5A
PWR_SRC
PC3 C2200p50X0402
PC1 C0.1u50Y
PC2 C10u25X6S1206-RH
09/21 Remove PC1152 for PW reguest
+3VSUS
PR3 100KR0402
PU1
18 SUSPWROK
22 3_5VSUS_PG
PR5 68.1KR1%0402
PC7 X_C1u6.3Y0402-RH
PGOOD
TRIP
EN
VFB
RF
GND
VBST
DRVH
SW
V5IN
DRVL
TPS51218DSCR_SON10-RH
PR4 2.2R
PC6 C0.1u25Y
DH_1V1
LL_1V1
DL_1V1
+5VSUS
PR8 464KR1%0402-HE
PC8 C1u10X50402-HF
PQ8
NN-AO4932_SOIC8-RH
PL2 CH-1.0u22A10mS-RH
PR47 X_2.2R
PC58 X_C1000p50X0402
PC5 C10u10Y0805
PR7 5.6KR1%0402
PR6 10KR0.1%0402-HE
G2
PC72 C560u2.5SO-RH
+1.8VRUN_PWRGD_D
PR63 0R0402
PQ12
N-AO4468_SOIC8-RH
+1.1VSUS
+1.1VRUN
09/21 Change PC3003 from C71-331027E-S03 to for PW suggestion
1.0VRUN
OCP:8A
MAX:6A
PWR_SRC
PC96 C2200p50X0402
PC98 C0.1u50Y
PC100 C10u25X6S1206-RH
PC101 C10u25X6S1206-RH
+3VRUN
PR83 100KR0402
PU6
23 +1.0VRUN_PWRGD
PR82 71.5KR1%0402-RH
18,22,23 RUN_ON
PR85 0R0402
PC94 X_C0.1u10X0402
PR88 464KR1%0402
TPS51218DSCR_SON10-RH
PR84 2.2R
PC93 C0.1u25Y
DH_1V0
PC95 C1u10X50402-HF
PQ20
NN-AO4932_SOIC8-RH
PR89 X_2.2R
PC99 X_C1000p50X0402
PL3 CH-1.0u22A10mS-RH
PC97 C10u10Y0805
PR87 5.1KR0402
PR86 10KR0.1%0402-HE
PC102 C560u2.5SO-RH
G3
+1.0VRUN
Modify 1.05V For AMD recommand
Modify 1.05V For AMD recommand
PWR_SRC
PR64 33KR0402
PWR_SRC
PR61 100KR0402
+1.8VRUN_PWRGD_D
PR65 470KR0402
PC81 C0.1u25Y0402-RH
PQ14
NN-2N7002DW_SOT363-RH
D1 D2 S1 G1 S2 G2
18,25 +1.8VRUN_PWRGD
PR60 0R0402
+1.8VRUN_PWRGD_R
PR62 100KR0402
PC80 X_C0.1u25Y0402-RH

MSI MICRO-STAR INT'L CO.,LTD.

Title: GroupB 1.1V,1.05V

Size	Document Number	Rev
Custom	MS-16GN1	0.A

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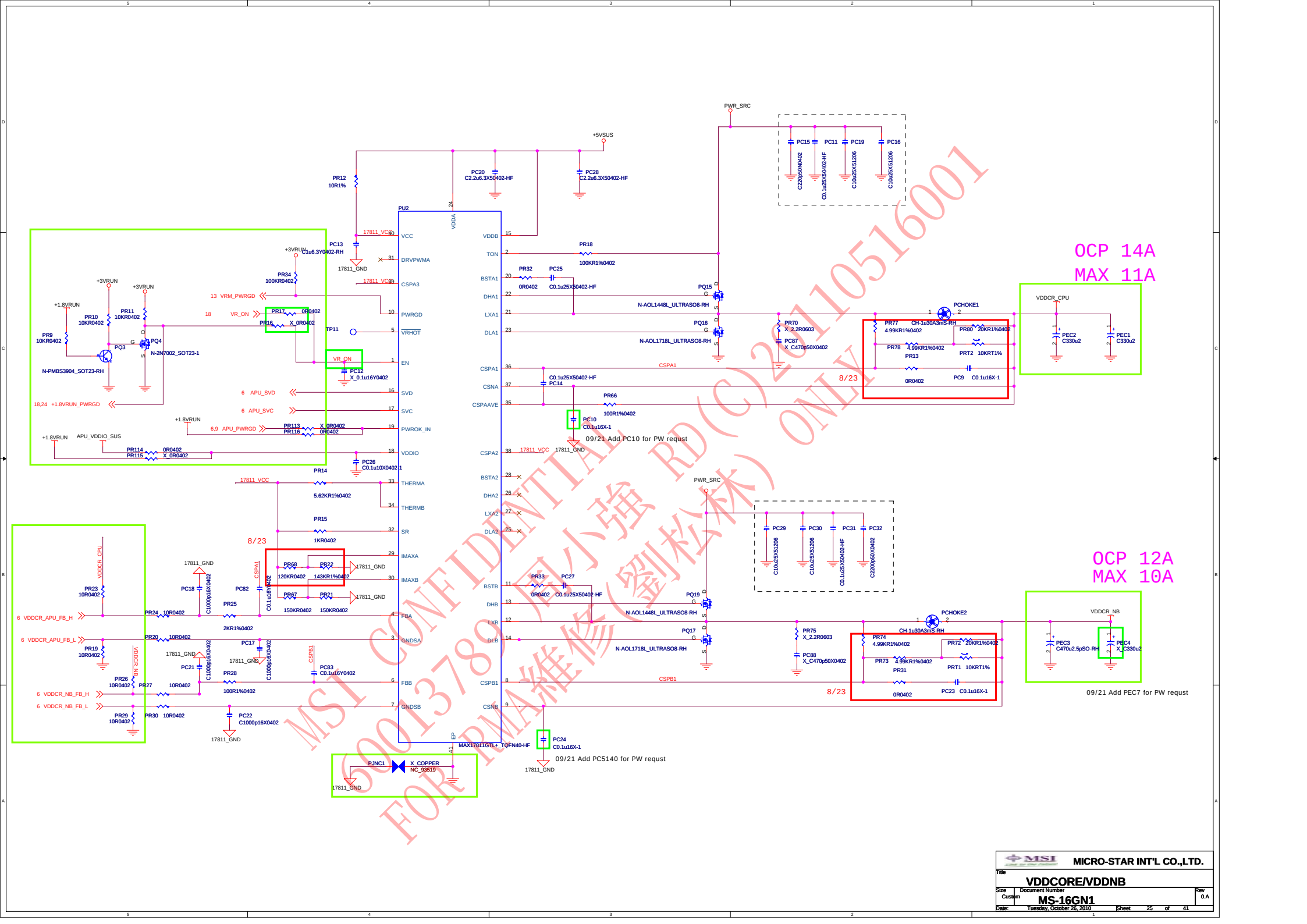

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	VDDCORE/VDDNB		
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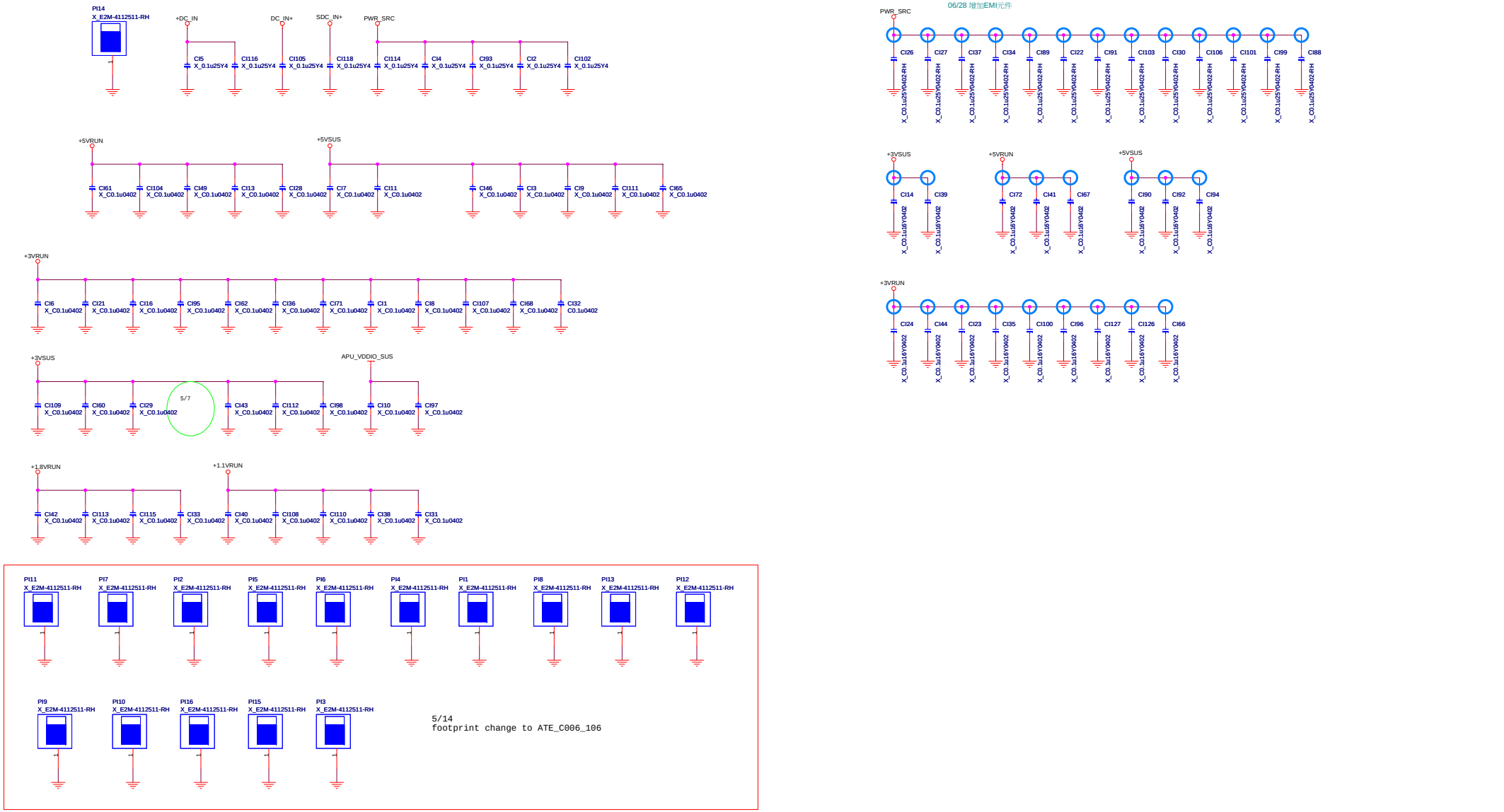

MICRO-STAR INT'L CO.,LTD.

Title: EMI

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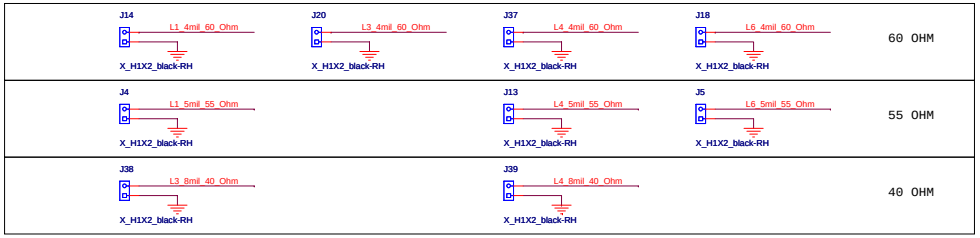

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Title: IMPEDANCE JUMP

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CPU Thermal Hole

CPU Thermal Model
ASM CFG = 60

PCB
PCB1
P30-16GN10A-D05

P30-16GN10A-H73,瀚宇博德(薩摩亞),
P30-16GN10A-D05,昆騰(定穎大陸),
P30-16GN10A-T53,健鼎無錫

for HDMI Logo charge
UME1
PCB
X_HDMI ROYALTY
Y01-RHDMI03-000

MVT後記得上件

NB STANDOFF

APU STANDOFF
2010/10/27 Change GPU_H1 and NB_H1 from
E2B-1221010-L63 to E2B-16GM010-A89 for Thermal request

GPU_H1
Spacer
Support
E2B-16GM010-RH
HOLES_R236D91_PT
E2B-16GM010-A89

NB_H1
Spacer
Support
E2B-16GM010-RH
HOLES_R236D91_PT
E2B-16GM010-A89

Mylar for SAFETY
MYLAR_1 6/18 E2Y-6G12211-Y42
MYLAR_2 6/18 E2Y-6G12211-Y42
MYLAR_3 6/18 E2P-6G14011-Y42

Mylar for M/E
MYLAR_8 6/18 E2P-6G14611-Y42
MYLAR_9 6/18 E26-1022220-Y42
RUBBER_1 6/18 E2Y-6G11311-Y40
RUBBER_2 6/18 E2Y-6G11311-Y40
RUBBER_3 6/18 E2Y-6G11211-Y40
MYLAR_10 6/18 E2P-6G12811-Y42
RUBBER_4 6/18 E2Y-6G10911-Y42
MYLAR_12 6/21 E2Y-Z001711-Y42
MYLAR_13 6/21 E2Y-Z001711-Y42
MYLAR_14 10/06 E26-1022220-Y42

FCH STANDOFF
PCH_ SCREW HOLE
HOLES_R193D138_PT
E2B-163B010-L63
SB_H2

PCH_ SCREW HOLE
HOLES_R193D138_PT
E2B-163B010-L63
SB_H1

FCH Thermal Model
ASM CFG = 60

SB_HEAT1
SB_HEATSINK
E31-0403231-TA9

SCREW_SB1
SCREW_M2X0.4,4.5mm,3mm
E43-1203003-H29

SCREW_SB2
SCREW_M2X0.4,4.5mm,3mm
E43-1203003-H29

Mylar for EMI
MYLAR_7 6/18 E2M-6G13111-Y42

FM4 X_F_PAD_M100
FM16 X_F_PAD_M100
FM18 X_F_PAD_M100
FM20 X_F_PAD_M100
FM15 X_F_PAD_M100
FM19 X_F_PAD_M100
FM6 X_F_PAD_M120
FM21 X_F_PAD_M100
FM17 X_F_PAD_M120
FM7 X_F_PAD_M120
FM8 X_F_PAD_M120
FM5 X_F_PAD_M120

BTB3 SCREW HOLE (16GKA)
MH12 X_HOLES236D118_P
MH11 X_HOLES236D118_P

BTB1 STANDOFF (16GKB)
SP2 Spacer Support E2B-1371010-RH
SP1 Spacer Support E2B-1371010-RH

PCIE STANDOFF (Mini PCIE Card)
SP4 Spacer Support E2B-1010010 HOLES_R177D91 E2B-1010010-L63
SP3 Spacer Support X_E2B-1010010 HOLES_R177D91 E2B-1010010-L63

FM9 X_F_PAD_M120
FM22 X_F_PAD_M120
FM10 X_F_PAD_M120
FM23 X_F_PAD_M120
FM3 X_F_PAD_M120
FM14 X_F_PAD_M120

8/06 增加板邊光學測試點7顆

MH1 X_8x8 (PTH)
MH8 X_8x8 (PTH)
MH6 HOLES_8X8_D3MM_VIA8
MH5 HOLES_8X8_D3MM_VIA8
MH10 HOLES_8X8_D3MM_VIA8
MH3 X_8x8 (PTH)
MH7 HOLES_8X8_D3MM_VIA3
AGND
MH4 HOLES_8X8_D3MM_VIA3
MH9 HOLES_8X8_D3MM_VIA3
MH2 HOLES_8X8_D3MM_VIA8

NPTH (only hole)
NPTH118 H1
NPTH118 H2

HDD Connector SCREW
ASM CFG = 60

SCREW_HDD1
SCREW_M2,4.5mm,4.0mm
E43-1204005-H29

SCREW_HDD2
SCREW_M2,4.5mm,4.0mm
E43-1204005-H29

HDD Connector SCREW
ASM CFG = 60

SCREW_ODD1
SCREW_M2,4.5mm,4.0mm
E43-1204005-H29

SCREW_ODD2
SCREW_M2,4.5mm,4.0mm
E43-1204005-H29

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Title	ME	
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